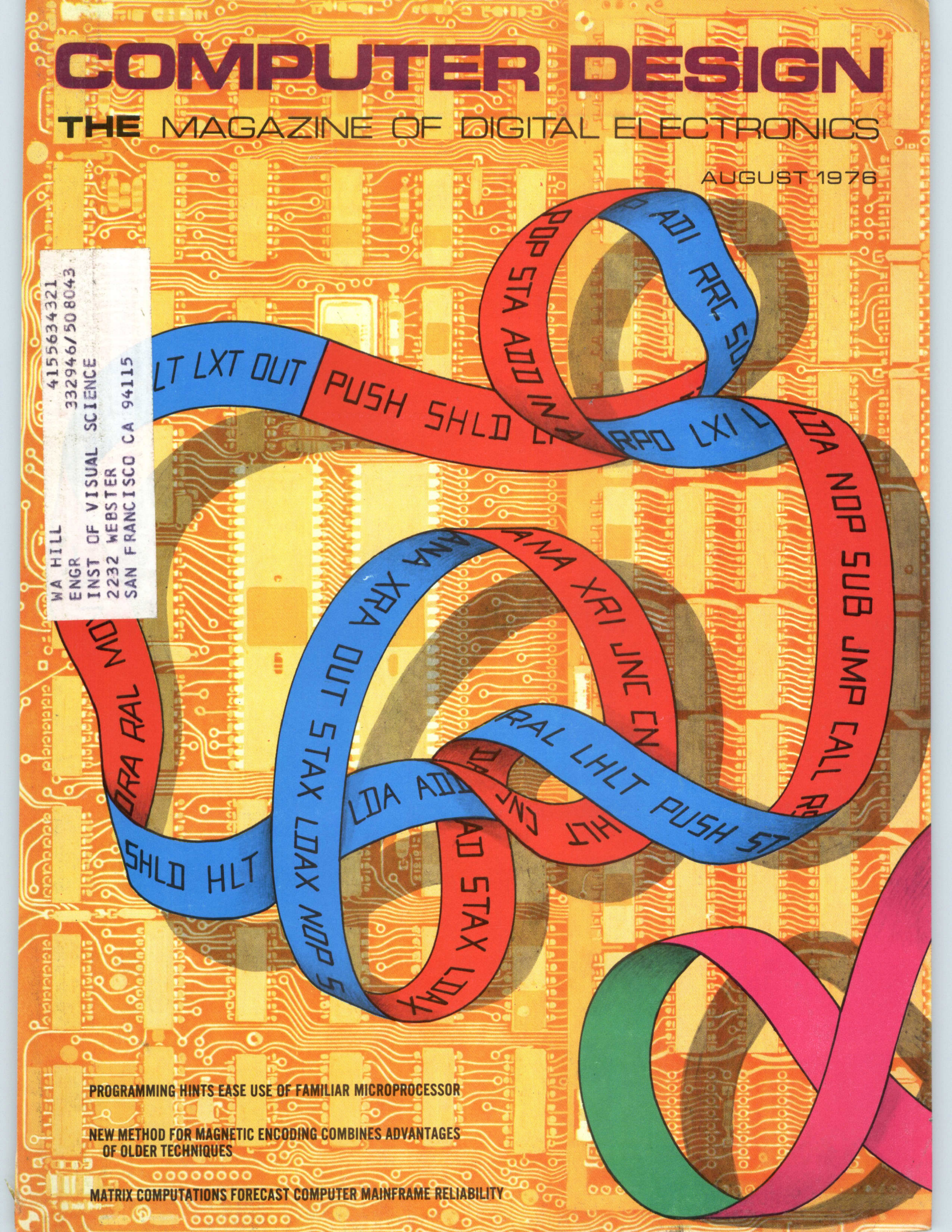
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

AUGUST 1976



PROGRAMMING HINTS EASE USE OF FAMILIAR MICROPROCESSOR

NEW METHOD FOR MAGNETIC ENCODING COMBINES ADVANTAGES OF OLDER TECHNIQUES

MATRIX COMPUTATIONS FORECAST COMPUTER MAINFRAME RELIABILITY

Intro-. ducing the amaz- ing EECO

machine: in one end
you put your raw,
un-annotated logic diagram,
and out of the other comes
your fully wire wrapped
socket board/frame/drawer/system—
your choice.
Together with
a Final Exception Report,
a Final String List,
an IC Location List,
lists for IC Type and Socket Size,
a Wire Loop List,
a Pin Assignment List,
an Unused Circuit Elements and Pins List,
a Pin by Pin Wire List,
and your diagram back, fully annotated.

This machine uses
a computer,
and people,
and hardware
all under the same root,
and gives you a chance
to correct or change
your circuitry
before we go to hardware.
We deliver in as little as two weeks,
including time for you
to review.
We've been doing this
for more than five years,
almost in secret.
Now we're telling you
and the world because
it's about time.
Write or phone
the keeper of the EECO machine,
Dick Hunter.

EECO
PACKAGING/SWITCHES/READERS
1441 East Chestnut Avenue, Santa Ana, California 92701
Phone 714/835-6000
CIRCLE 1 ON INQUIRY CARD

Introducing Model 9300
Quality that's Quick & Quiet

Model 9300 Vacuum Column digital tape transport has characteristics common to all Kennedy recorders — and a few new ones. It's quick (125ips); quiet (noise level of less than 70db), and it has the built-in quality of all Kennedy products.

Utilizing side-by-side vacuum columns and a capacitive tape-location detector for improved tape life; air bearings and Tribaloy coated read-after-write heads to reduce tape wear and improve data integrity, Model 9300 is ideal for minicomputer and data collection applications requiring complete reliability at high tape speeds.

Model 9300 comes complete with all the operational features of the 9000 Series. Performance is guaranteed by crystal controlled timing, read threshold scanning, our read-after-write shortened skew gate and other exclusive Kennedy features. Operation is simplified by such operator-oriented features as a front-accessible test panel, quick-release hubs and simplified tape loading.

Model 9300 has a standard tape speed of 125ips, with data densities of 200/556cpi or 556/800 on the 7-track unit and 800cpi, 1600cpi or 800/1600cpi on the 9-track transport. The format is NRZI/PE.

Model 9300 is not only quick and quiet — it's very competitive. That's quite a lot, considering the Kennedy quality.

KENNEDY CO.

540 W. WOODBURY RD., ALTADENA, CALIF. 91001
(213) 798-0953

KENNEDY · QUALITY · COUNT ON IT

CIRCLE 2 ON INQUIRY CARD

This Tally printer knows the shortest way to double or triple your throughput.

You get there faster if you don't have as far to go. Tally's Model T-1202 optimized bi-directional serial printer prints left to right and right to left while its microprocessor looks ahead for the shortest path to the next line of print. These short cuts add up fast to slash your throughput time by two to three fold. (Of course, throughput savings are tied directly to the amount of white space in your format.)

"Optimized" means moving the print head—left or right—to pick up the closest character on the next print line. There's no lost time with conventional carriage returns. And coupled with a 7 ips slew speed, the T-1202 moves the print head at an accelerated rate to the next print position.

And remember, you get this bonus throughput without taxing the machine—the printing rate remains at 120 characters per second so you haven't sacrificed reliability or increased wear.

The Model T-1202 is the newest member of the T-1000 Series —Tally's fine line of serial printers that offer microprocessor electronics, low acoustic noise level, digitally controlled print head advancement, dual tractor engagement and a convenient snap-in ribbon cartridge.

There's more to tell, so call your nearest Tally sales office.
Tally Corporation, 8301 S. 180th Street, Kent, WA 98031.
Phone (206) 251-5524.

OEM Sales Offices:
New York (516) 694-8444
Boston (617) 742-9558
Chicago (312) 956-0690
Seattle (206) 251-6730
Los Angeles (213) 378-0805
San Francisco (408) 245-9224
Business Systems Sales Offices:
Eastern Region (201) 671-4636
Western Region (415) 254-8350

TALLY

CIRCLE 3 ON INQUIRY CARD

THE
MAGAZINE
OF DIGITAL
ELECTRONICS

COMPUTER DESIGN

AUGUST 1976 • VOLUME 15 • NUMBER 8

DEPARTMENTS

BPA CIRCULATION OVER 55,000

FEATURES

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Editorial manuscripts should be addressed to Editor, Computer Design, 221 Baker Ave, Concord, MA 01742. For details on the preparation and submission of manuscripts, request a copy of the "Computer Design Author's Guide."

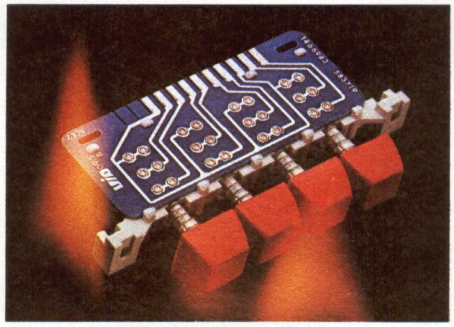
UID introduces the push-button switch you don't have to mount on a PC board. UID did it for you.

Put down your soldering iron and send your switch inspectors out for a leisurely lunch.

AMF/UID announces a new single and four-station push-button switch mounted to its own integral printed circuit board for quick connection. That means you can drop some time-consuming steps from your manufacturing process and avoid flux contamination and related problems.

This switch is enclosed and practically immune to the elements. Since it was expressly designed to operate in low-energy, high-reliability, long-life circuits, over one million trouble-free operations can be expected. UID's switch will add quality and durability to your product.

These switches are available with any combination of standard momentary, push-push, or interlock actuations with operating forces as low as 7 oz. All materials meet UL Flammability specs of 94VO. Any circuit interconnection can be made on the integral PC board.



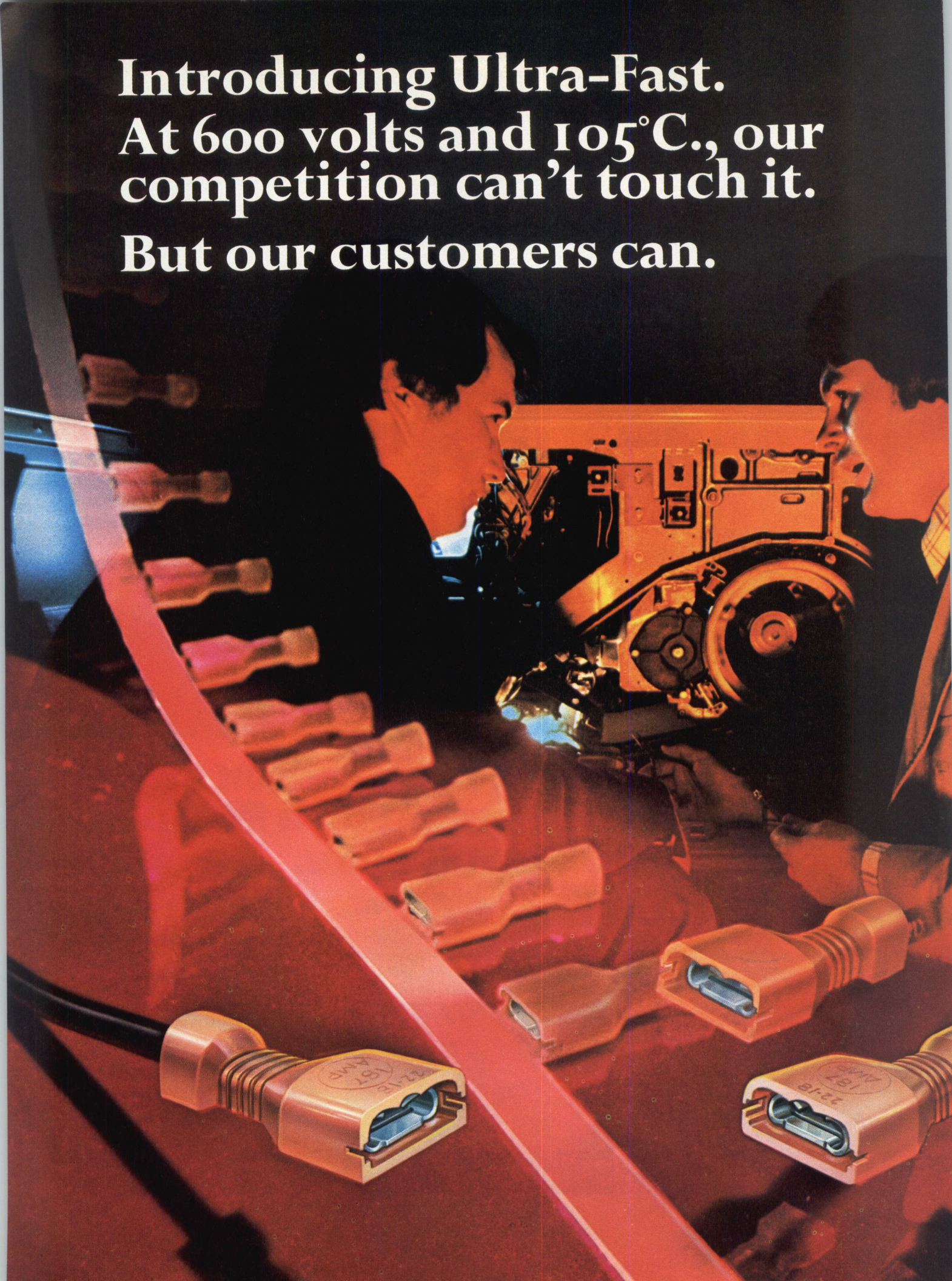
Silver-plated contacts are standard, but gold-plated or other precious metals may be specified. If the standard edge connections don't meet your needs, PC or wire wrap terminals can be provided.

Challenge UID's design engineers to meet your specific requirements. For more information, call or write: Dean R. Venator, UID Electronics Division, AMF Incorporated, 4105 Pembroke Road, Hollywood, Florida 33021. Telephone (305) 981-1211. TWX #510-954-9810.

AMF
UID Electronics

Introducing Ultra-Fast. At 600 volts and 105°C., our competition can't touch it.

But our customers can.



Our new Ultra-Fast fully-insulated FASTON terminals are UL Recognized at 600 volts and 105°C.

Which is volts—or degrees—ahead of other fully-insulated quick disconnects.

But while Ultra-Fast delivers plenty of electricity to your product, it won't deliver any to you—or whoever services your product. Because it's shockproof. And shortproof.

And its design is evidence of AMP leadership in the manufacture of safe, high-performance connectors.

Consider the pre-insulated one-piece housing design, for example. It takes the place of costly interlocks, shields, and post-insulation. And the unique, consistently-controlled, insulation overhang is sufficient to keep stray leads —or fingers—from making contact.

Ultra-Fast also has front-end slotted membranes. They provide clearance at the base of the tab so that the receptacle and tab dimple detents can be fully seated.

Of course, Ultra-Fast offers you the engineering expertise you'd expect from AMP. Things like funnel entry to prevent lead stubbing. Thicker housing walls. Wire size color coding. Visual inspection of the wire, before and after the crimp.

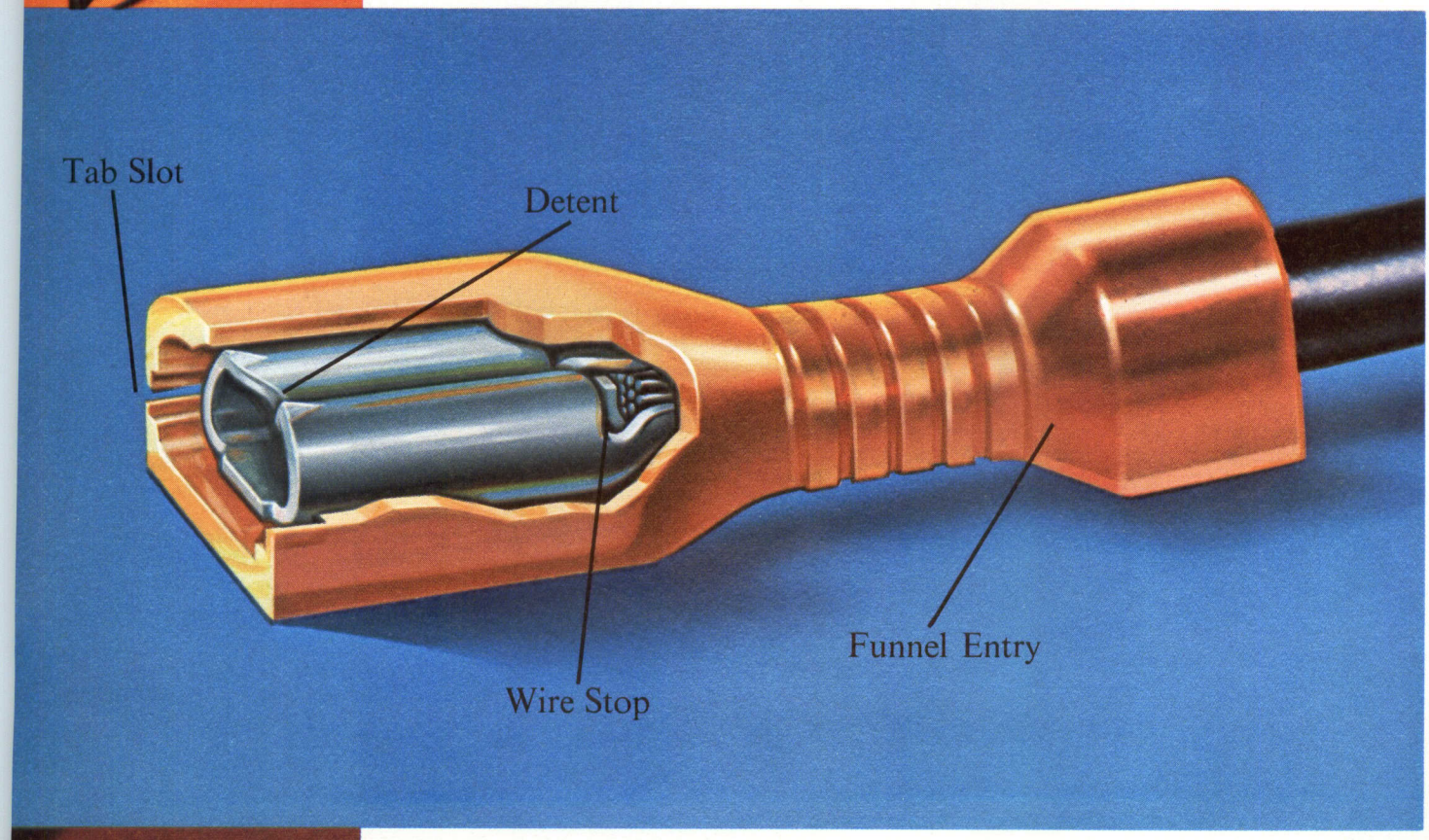
And Ultra-Fast—like all AMP connectors—comes with the quality advantages of AMP tooling: fully- and semiautomatic machines that can turn out as many finished leads per hour as production demands. And AMP technical assistance: knowledgeable, experienced technical assistance that's there when you need it. Where you need it.

Find out more about how our new Ultra-Fast can give you fully-insulated connection for your products.

And fully-insulated protection for the people who handle them.

Call Customer Service at (717) 564-0100, or write: AMP Incorporated, Harrisburg, Pa. 17105.

AMP
INCORPORATED



CALENDAR

CONFERENCES

SEPT 8—The Invitational Computer Conf, Marriott Hotel, Newton, Mass. INFORMATION: B. J. Johnson & Assoc. 2503 Eastbluff Dr, Suite 204, Newport Beach, CA 92660. Tel: (714) 644-6037

SEPT 20-22—Convergence 76, Internat'l Sym on Automotive Electronics and Electric Vehicles, Hyatt Regency Hotel, Dearborn, Mich. INFORMATION: J. M. Leahy, Micro Switch Div, Honeywell Inc, 17515 W Nine Mile Rd, Southfield, MI 48075. Tel: (313) 424-3744

SEPT 22-24—APL76 Conf, Ottawa, Ontario. INFORMATION: Comshare Ltd, 304-11 Adelaide St W, Toronto, Ontario M5H 1M2 Canada

SEPT 26-29—EASCON-76 (Electronics and Aerospace Systems Conf), Stouffer's Nat'l Center Inn, Arlington, Va. INFORMATION: EASCON-76, Suite 636, 821 15th St, NW, Washington, DC 20005. Tel: (202) 347-7088

SEPT 28-30—Canadian Computer Show-Salon De l'Ordinateur, Place Bonaventure, Montreal. INFORMATION: Show Mgr, Derek A. Tidd, Industrial and Trade Shows of Canada, 481 University Ave, Toronto, Ontario M5W 1A7 Canada

OCT 4-5 and 19-20—Instrumentation and Computer Fair, Philadelphia Marriott, Philadelphia, Pa and Sheraton Inn/Washington-Northeast, Lanham, Md. INFORMATION: Instrumentation and Computer Fair, Marketing Ventures, Inc, 5012 Herzel Pl, Beltsville, MD 20705. Tel: (301) 937-7177

OCT 10-14—ISA-76 (Instrument Society of America Internat'l Conf and Exhibit, Houston, Texas. INFORMATION: Instrument Society of America, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

OCT 12-14—EUROMICRO, Second Sym on Micro Architecture, Venice, Italy. INFORMATION: Jan Wilmink, Program Chm, Euromicro Symposium, Twente U of Technology, PO Box 217, Enschede 7801, Netherlands

OCT 12-15—Micro/Minicomputer Exhibit, U.S. Trade Center, Frankfurt, Germany. INFORMATION: Bureau of International Commerce, U.S. Dept. of Commerce, Washington, DC 20230. Tel: (202) 377-3748

OCT 13-15—Second Internat'l Conf on Software Engineering, San Francisco, Calif. INFORMATION: Dr C. V. Ramamoorthy, Program Chm, Dept of Electrical Engineering and Computer Sciences, U of California-Berkeley, Berkeley, CA 94720

OCT 19-21—1976 Mini/Micro Computer Conf and Exposition, Brooks Hall/Civic Auditorium, San Francisco, Calif. INFORMATION: Mini/Micro Computer Conf and Exposition, 5544 E La Palma Ave, Anaheim, CA 92807. Tel: (714) 528-2400

OCT 19-21—1976 IEEE Semiconductor Test Equipment Sym, Cherry Hill Inn, Cherry Hill, NJ. INFORMATION: Annual Test Symposium Committee, IEEE Philadelphia Section, U of Pennsylvania, Moore School of EE, Philadelphia, PA 19174

OCT 20-21—9th Annual Connector Sym, Hyatt House, Cherry Hill, NJ. INFORMATION: Electronic Connector Study Group, Inc, PO Box 1428, Camden, NJ 08101. Tel: (609) 424-4014

OCT 25-27—17th Annual Sym on Foundations of Computer Science, Houston, Texas. INFORMATION: Prof Michael J. Fischer, Program Chm, Dept of Computer Science, FR-35, U of Washington, Seattle, WA 98195

OCT 26, OCT 28, and NOV 18—1976/77 Invitational Computer Conferences, Chicago, Ill; Minneapolis, Minn; and Dallas, Texas. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 204, Newport Beach, CA 92660. Tel: (714) 644-6037

NOV 1-3—Cybernetics and Society Internat'l Conf, Mayflower Hotel, Washington, DC. INFORMATION: W. H. vonAlven, FCC, 1919 M St, NW, Washington, DC 20554

NOV 8-11—Third Internat'l Joint Conf on Pattern Recognition, Del Coronado Hotel, Coronado, Calif. INFORMATION: A. Rosenfeld, U of Maryland, Computer Science Center, College Park, MD 20742

NOV 8-11—Mini- and Microcomputers, Hotel Toronto, Toronto, Canada. INFORMATION: Mini- and Microcomputers—Hamza, PO Box 3243, Station B, Calgary, Alberta T2M 4L8 Canada

NOV 8-12—Exhibition of U.S. Computers and Peripheral Equipment, U.S. Trade Center, Sydney, Australia. INFORMATION: Irwin D. Nathanson, Office of International Marketing, DIB-233, U.S. Dept of Commerce, Washington, DC 20230. Tel: (202) 377-4957

NOV 17—Computer Networks: Trends and Applications, Gaithersburg, Md. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

NOV 23-25—COMPEC'76 (Computer Peripheral, Small Computer, and Systems Exhibition), Wembley Conf Centre, Wembley, Middlesex, England. INFORMATION: Trident Conferences and Exhibitions Ltd, Abbey Mead House, 23a Plymouth Rd, Tavistock, Devon PL19 8AU England

NOV 23-27—Conf-Exhibition of Automation and Instrumentation, Milan, Italy. INFORMATION: Federation of Scientific and Technical Associations, Piazzale Rodolfo Morandi, 2 (Piazza Cavour)-20121 Milano, Italy

NOV 25-DEC 1—electronica 76 (7th Internat'l Trade Fair for Components and Production Facilities), Munich Fairgrounds, Munich, Germany. INFORMATION: Münchener Messe- u. Ausstellungsgesellschaft mbH, München 12, Postfach 12 10 09, Messegelände, Germany

SEMINARS

AUG 16-20 and SEPT 20-24—Digital Systems Engineering, Holiday Inn, Boston, Mass and Sheraton-Gatehouse, Rochester, NY. INFORMATION: InfoScope, Inc, 157-159 Whitehead Ave, PO Box 227, South River, NJ 08882. Tel: (201) 238-2220

SEPT 20-22—Input/Output Systems Seminar, New York Sheraton Hotel, New York City. INFORMATION: Input/Output Systems Association, 999 Bedford St, Stamford, CT 06905. Tel: (203) 323-3143

SHORT COURSES

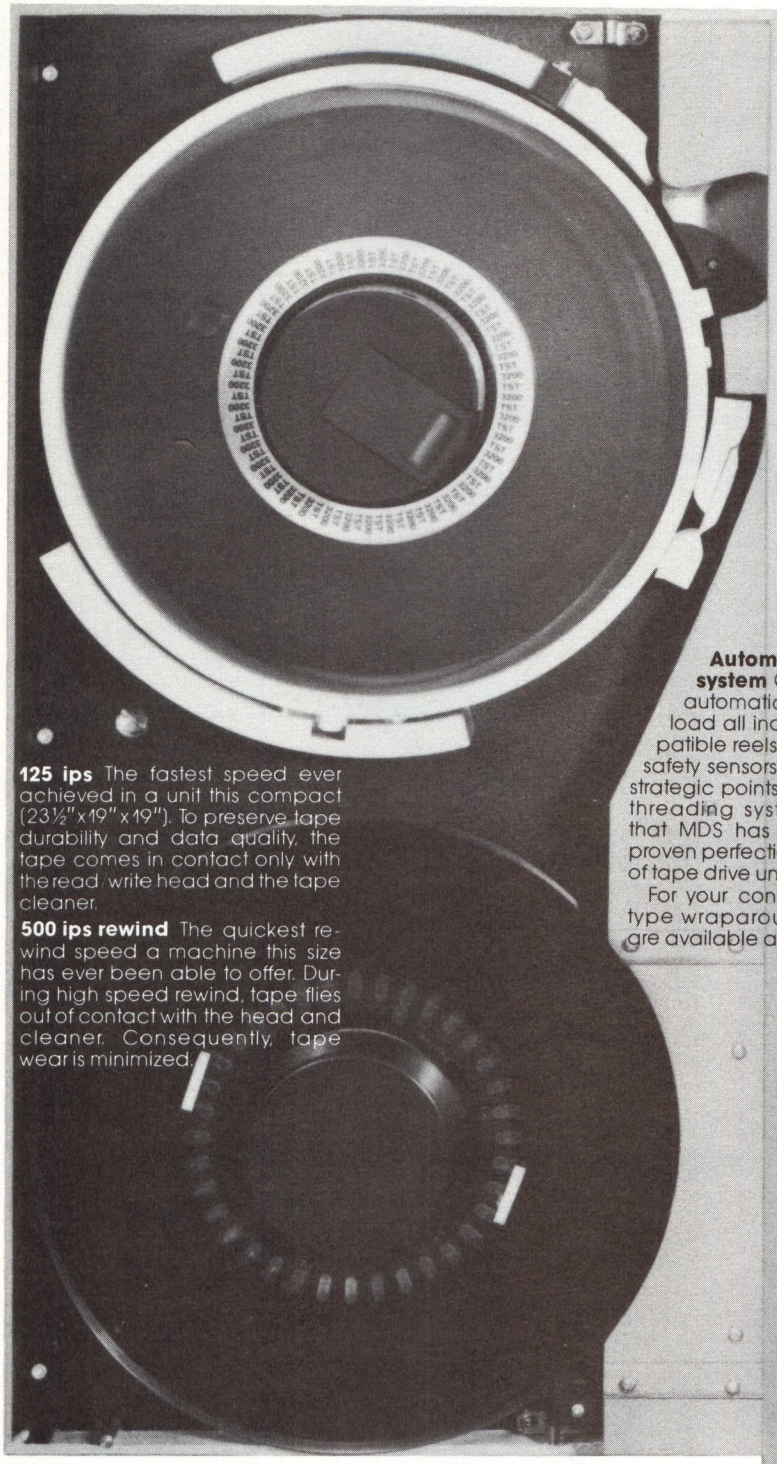
AUG 16-20—CRT and Matrix Display Systems Design, U of Wisconsin-Extension, Madison. INFORMATION: John T. Snedeker, Dept of Engineering, U of Wisconsin-Extension, 929 N Sixth St, Milwaukee, WI 53203. Tel: (414) 224-4193

AUG 30-SEPT 3—Data Compression: Theory and Applications; Software Design for Data Communication Systems, SEPT 13-17—Computer Architecture, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC. Tel: (202) 676-6106

SEPT 12-17—Microprocessors and Minicomputers—Interfacing and Applications Using the DEC LSI-11, Virginia Polytechnic Institute and State U, Blacksburg, Va. INFORMATION: Harold Walsh, American Chemical Society, 1155 16th St, NW, Washington, DC 20036

Six smart reasons that make the MDS 4025 Tape Drive the Intelligent Choice.

Just a few of the reasons why over 5000 units are satisfying customers around the world.



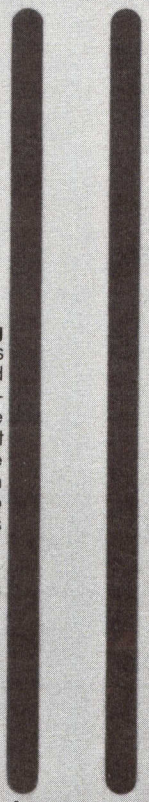
125 ips The fastest speed ever achieved in a unit this compact (23½"x19"x19"). To preserve tape durability and data quality, the tape comes in contact only with the read/write head and the tape cleaner.

500 ips rewind The quickest rewind speed a machine this size has ever been able to offer. During high speed rewind, tape flies out of contact with the head and cleaner. Consequently, tape wear is minimized.

Air bearings The MDS 4025 features air bearings at all tape turnaround points. The tape travels on a pillow of air, so the edge wear and tape friction commonly produced by roller bearings are eliminated.

Automatic threading system Quick. Transports automatically thread and load all industry hub-compatible reels. Error-free. Tape safety sensors are located at strategic points throughout the threading system—a system that MDS has engineered to proven perfection in thousands of tape drive units world-wide.

For your consideration, IBM-type wraparound cartridges are available as an option.



Linear reel servo sensor system Molded vacuum column sensor rails and photoelectric sensors create the simplest (and therefore, most reliable) reel servo sensor system on the market today. Linear photoelectric solid state limit sensing in the vacuum columns results in precise tape position indication. In addition, gentle, stable program-restriction-free tape handling is provided at all speeds, including high speed rewind.

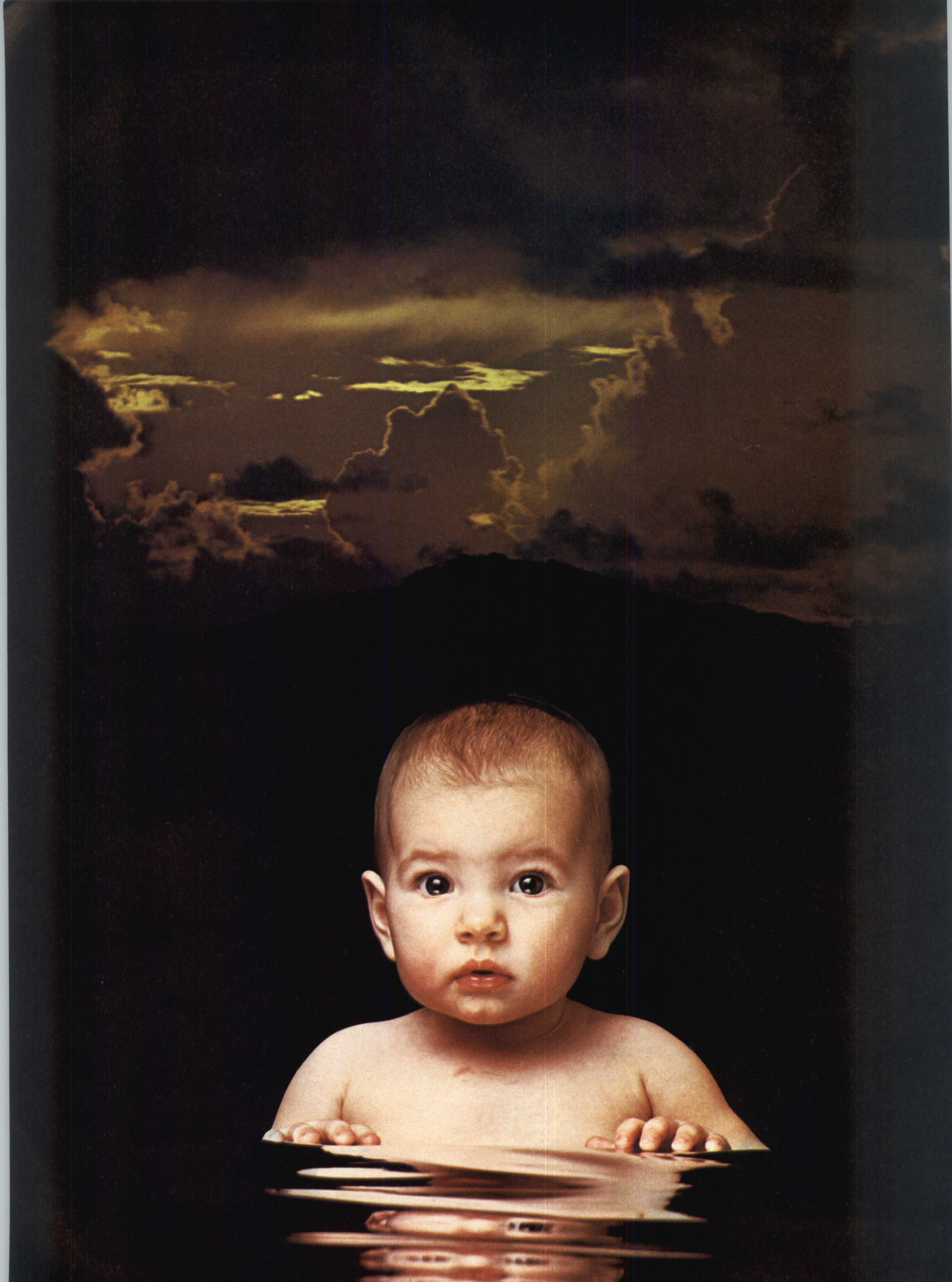
Volume production Mohawk Data Sciences is recognized as a leader in the OEM equipment field. Our 4025 Tape Drives are highly regarded for their unsurpassed quality and performance record. It's no wonder that the largest OEM companies have installed over five thousand 4025 Systems to date. Proven quality. Proven capability. MDS turns smart reasons into many intelligent choices.

For more smart reasons about the MDS 4025 Tape Drive, call or write your nearest MDS OEM Sales Office.

Boston	Herkimer	Los Angeles
460 Totten Pond Rd.	Palisade St.	901 E. Cerritos Av.
Waltham, Ma. 02154	Herkimer, N.Y. 13350	Anaheim, Ca. 92805
(617) 890-5870	(315) 867-6472	(714) 772-0803

Mohawk MDS Data Sciences
The Intelligent Choice.

CIRCLE 8 ON INQUIRY CARD



The emergence of a new thinking machine.

The SEL 32/35.

Twice the power for half the price.

If your computing needs could be answered by such machines as Data General's Eclipse, or DEC's PDP 11 series or Interdata's 7/32, consider the SEL 32/35.

Rather than get into bits and bytes, there's really only one thing you need to know about the SEL 32/35: You get two to four times the power for every "compute" dollar spent. Period.

That's a pretty powerful statement. But the SEL 32/35 is a very powerful machine.

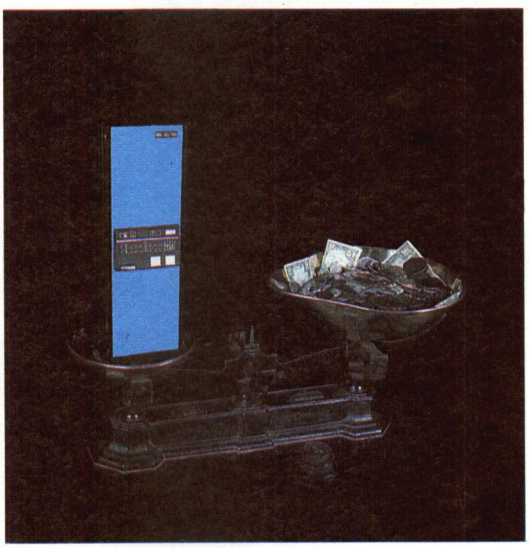
Extra power can go a long way to maintain the balance you need in your computer system, so essential for reliable, peak performance.

And extra power, for fewer dollars, can do wonders when you're trying to balance a corporate budget.

For more information about the new arrival in our family of computers, just circle our number on the Reader Service Card. Or, for faster action, call us direct.

Either way, we'll see that you get all the vital statistics on our new baby.

SYSTEMS
ENGINEERING LABORATORIES



6901 West Sunrise Boulevard
Fort Lauderdale, Florida 33313
(305) 587-2900

European Inquiries: 85 bis Avenue Albert 1er 92500/Rueil, France

LETTERS TO THE EDITOR

To the Editor:

The American National Standards Institute (ANSI) X3A1 ad hoc committee on dot matrix printing is studying OCR-A and OCR-B characters as currently being printed using dot matrix techniques.

Manufacturers who believe that they are capable of printing these characters using a dot matrix technique are invited to contact the committee chairman, Bruce Norlund. He can be reached by writing to him at 150 Congress St, Keene, NH 03431, or by calling him at (603) 352-1130, X2203.

Bruce K. Norlund
Keene, NH

To the Editor:

In the May 1976 issue of *Computer Design* a software product announcement was run for Sofco, Inc concerning PDP-11 cross assemblers for various microprocessors. Your readers should be advised that similar cross assemblers have been developed at government expense by Battelle-Northwest, and are public domain.

The Intel 8080 and the Motorola 6800 are two examples used in a report available through the National Technical Information Service, 5285 Port Royal Rd, Springfield, VA 22151 (report number BNWL-SA-5701). This report discusses the techniques involved in constructing cross assemblers using macro definitions. The macro sets for the 4004, 8008, and 8080 are also available from the Intel program library. I have also developed a macro set for the Computer Automation LSI/2, but this is unavailable through published references.

Thomas A. Seim
Battelle
Pacific Northwest Laboratories
Richland, Wash

Letters to the Editor should be addressed:

Editor, Computer Design
Professional Building
221 Baker Avenue
Concord, MA 01742

You asked for an easily configurable mini.

You've got it.

It's a snap to put together Honeywell's Level 6 mini to do the things you want. For example, suppose you want a system for data capture, storage and retrieval. Here's how you configure it.

1. Start with a rack-mountable Model 6/34 with 24K words of MOS parity memory, multiply/divide, realtime clock, 64 vectored interrupts, and bootstrap loader.

Now let's say you need four local entry stations and an operator's console with supporting peripheral capability. So you add:

- A Multiple Device Controller board to which you attach a console CRT, serial printer, and 512K byte dual diskette.
- A Multiple Device Controller board to which you attach 4 CRTs.

Now your configuration is complete, including all cables, mounting hardware and GCOS/BES1 software. And it's only **$19,978.***

2. If you want communications and disk capability, here's what you do. Start with the basic Model 6/36 processor with 32K words of memory. Then add:

- A Multiple Device Controller board to which you attach a console CRT and serial printer.
- A Mass Storage Controller board to which you attach a 2.5 megabyte cartridge disk.
- A Multiple Line Communications Processor board to which you attach 6 CRTs on full duplex lines and a host processor communications link.
- GCOS/BES2 software.

Again, your system is complete, and the price is only **$30,147.***

There's lots more. Besides those mentioned, we offer a variety of central processor, communications, and peripheral options, plus additional software. And it's all backed by the extensive know-how, experience, and worldwide service organization of Honeywell.

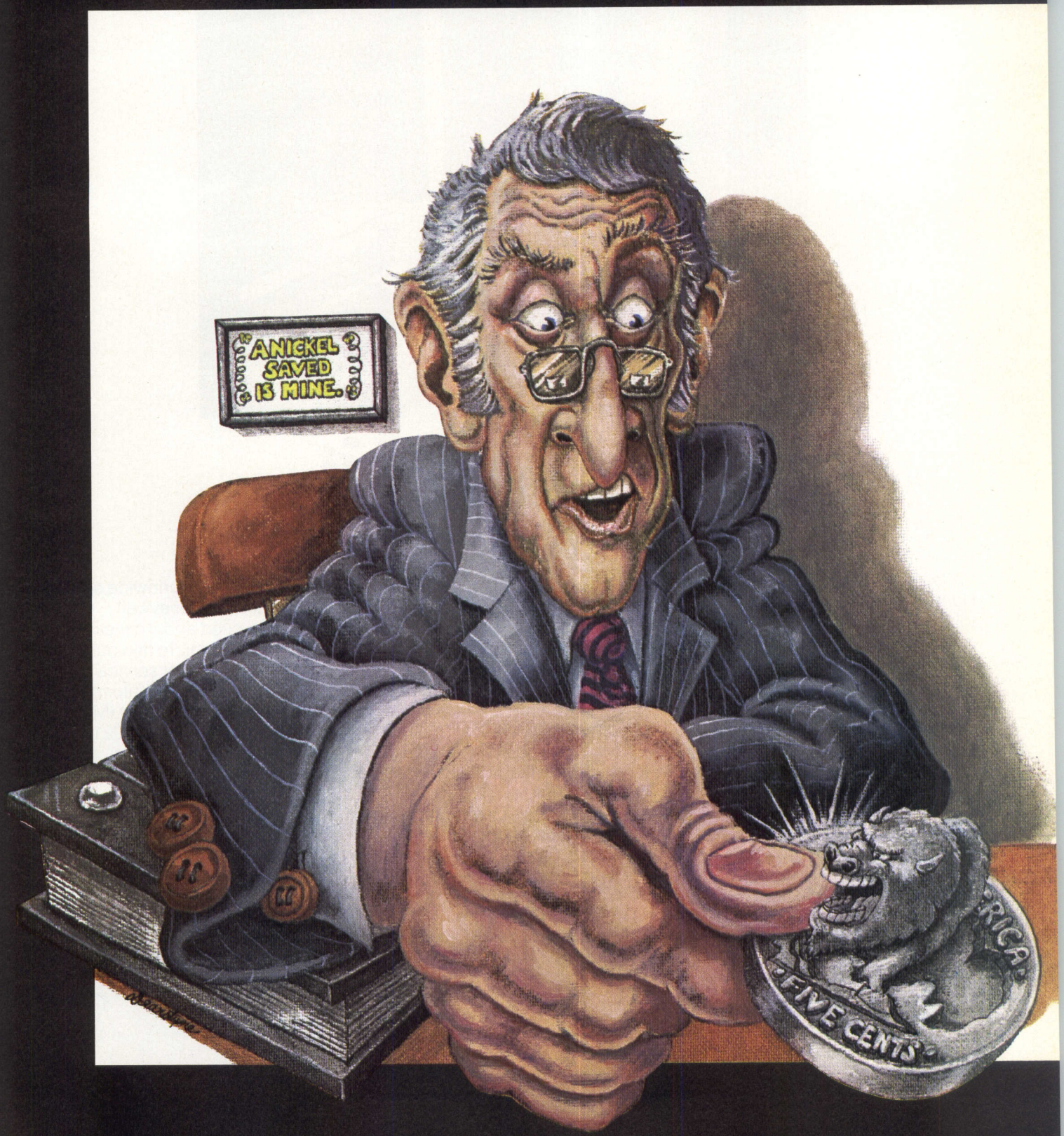
We're excited about our easily configurable mini. To find out more, just circle the reader service card. Or write us. Honeywell Information Systems, 200 Smith Street (MS487), Waltham, Massachusetts 02154.

Honeywell

*U.S. price in quantities of 50.

CIRCLE 11 ON INQUIRY CARD

"Itchy Palms" to buy all his mini



Palmer used peripherals on price

Ebenezer "Itchy Palms" Palmer.

Born prematurely in the bargain basement of a discount department store.

Shortened his first name to "Eb" to save writing time.

Once used a borrowed tea bag for 126 consecutive days.

Prided himself on always buying his minicomputer peripherals on price: rock-bottom.

But "Itchy Palms" Palmer's penchant for parsimonious peripheral purchasing was beginning to cost him a lot in returned devices, repairs, headaches and lost customers.

Until one day, while eating his way through a bag of day-old fortune cookies, "Itchy Palms" came across the following message:

"The truly wise man pays for his mini peripherals only once. Plessey Microsystems can expand your minicomputer systems with a complete line of highly-reliable, hard-working mini peripherals that won't come back to haunt you. And Plessey Microsystems is part of an international billion dollar corporation which prides itself on providing complete and comprehensive product support services."

"Pay only once," smiled Palmer. "Won't come back to haunt me. Comprehensive product support."

They were talking *his* language.

So from that day on, Eb Palmer bought all his mini peripherals from Plessey Microsystems.

He ended up spending much less in the long run.

And he rewarded himself with a cup of well-aged tea.

If you'd like to find out how Plessey add-on core memories, single and dual disc drives and punched tape readers can expand your mini without depleting your resources, just call us today.

Miser's Delight

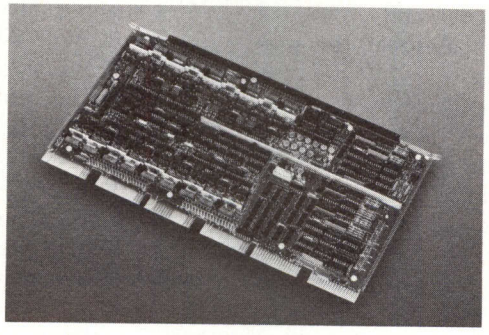
Plessey has delivered thousands of reliable low-cost memories which are being used in a variety of applications around the world.

Our latest offering is more of the same: 32K words on a single plug compatible card.

The PM-1132 core memory has an access time of 350 ns, is available with or without parity, and occupies just two slots in your PDP-11 series mainframe. The PM-1132 is plug compatible in either the standard or new modified unibus backplane, and can be selected on any 4K address boundary. Also available is the new PM-S1132, an NMOS semiconductor memory which is plug compatible with the DEC MS11-EP, FP, and JP M05 modules. The PM S1132 contains up to 32K x 18 on a single hex board with a 400 ns access time and a 500 ns cycle time.

Or if 32K is more than you need, try one of our 8K or 16K modules with your DEC, Data General, and Interdata minis. They're all plug compatible and can be mixed and matched with memories from the mini manufacturers.

It's a new high in mini memory performance. And a new low in minicomputer data storage costs.



CIRCLE 12 ON INQUIRY CARD

Plessey Microsystems
(714) 540-9945

by John E. Buckley
Telecommunications Management Corp
Cornwells Heights, Pa.

In-WATS System Access

The majority of today's information processing systems operate with some element of interactive or time-sharing processing. Those remote terminals which use this method of system access typically dial the central computer site for processing access. The advantage of using dial access is the ability to avoid any communications cost until actual data exchange is to take place. Dialed services are charged by telephone companies on a basis of connection duration as well as distance between connected points. Terminal sites which have occasional or infrequent access requirements, such as with an inquiry application, cannot cost justify the monthly charge of leased line. Even when the leased line is a multiplexed facility or multipoint line, the proportional part of the shared facility allocated to each terminal also can be prohibitive.

Time-sharing systems that provide processing services to a number of different company clients have been confronted continually with the problem of providing the lowest cost access to their various users. Common access schemes include installation of extensive leased line networks which are multiplexed into low speed, 30-char/s channels with each channel having a local dial access telephone number. When typical interactive terminals were unbuffered direct keyboard entry devices limited to a 300-bit/s transmission rate, such multiplexed networks were adequate.

Today's technology for remote terminals embodies the capabilities of microprocessors and local data storage. Operating philosophy of these newer and future terminals is to perform assembly of data entry at the terminal location and then to transmit completed data at rates of 2400 bits/s. These more recent terminal devices can be used effectively for both data base entry and inquiry functions. While more comprehensive remote terminals provided a significant increase in transmission and processing efficiency, they preclude any application of traditional multiplex networks.

In order to realize some form of direct communications access cost control, many companies have resorted to one of three methods of billing communications access costs. Most common method is to have the telephone bill associated with the remote terminal charged directly to the processing center. This provides a separate bill each month for each terminal. Direct cost allocation is therefore readily performed.

A second method is to instruct all remote terminal sites to call collect to the computer center. In this way, the remote user is not charged directly; total communication access cost is master billed to the processing center. However, direct cost allocation is still possible by analyzing direct toll charges and sorting them by calling number.

Third method is to assign a credit card number to each remote terminal site. Each dialed access to the computer center uses the credit card number which provides a master bill to the center; this bill is subdivided by each remote site's usage.

All these methods are applicable to dialed or switched network access, and are intended to provide the least possible and most visible communications access cost to the remote user and/or the central computer site.

Users of even the more traditional lower speed terminals have found that direct dial access can provide operational and reliability advantages over a leased line multipoint or multiplex network. One of the major advantages of dealing with a switched network is virtual immunity to line failure. Leased line network, whether multipoint or multiplex, is always susceptible to significant downtime in the event of common network failure. Because of inherent characteristics of switched network within the U.S., every time a connection is dialed a totally different configuration of network components is interconnected to establish the connection. If a particular connection therefore exhibits an incompatible error rate, the abnormal network component can be bypassed by redialing.

March 1976 tariff changes for switched network usage created a significant low cost access method for these systems. These increases raised rates for station dialed toll charges and, most significantly, instituted a major increase for any dialed connection (such as credit

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high density DIP sockets from R-N

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Slim, low body design—actually 26% lower—cuts packaging space needs drastically.

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of socket leads permit maximum board density in either end-to-end or side-by-side arrangement. Cuts PC board drilling costs as well.

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Self-lock leads hold socket firmly during high speed wave soldering.

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Unique R-N contact design assures that your IC lead maintains solid contact—even in most punishing applications.

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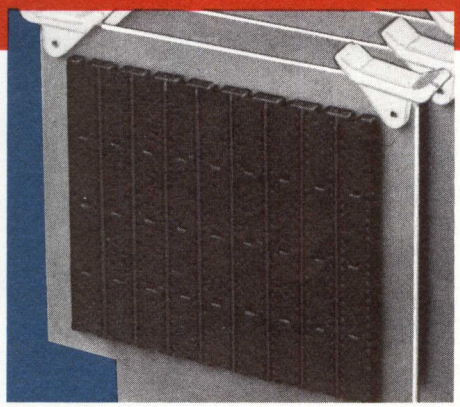
with these new ICL low-profile DIP sockets from Robinson-Nugent. Designed for high speed automatic assembly and maximum shock and vibration resistance. Has famous R-N "side-wipe" single leaf contacts, body meets UL94V-0 flammability rating. 8 thru 40 leads available.

Check the advantages of these high density sockets today! Write for complete specifications on this new R-N low-profile ICL DIP socket now.



For maximum package density with traditional R-N reliability, specify this new low cost, low-profile ICL DIP socket.

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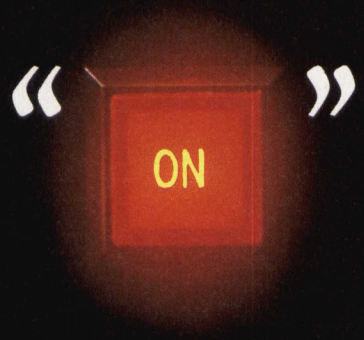
CIRCLE 13 ON INQUIRY CARD

A Statement of Our Objectives:



In a word—that's it.

And nothing else could so eloquently express our intent:

To provide the people and companies we serve with products and services as absolutely reliable as possible; helping them achieve greater system availability than ever before possible.

We're AMCOMP. A company actively engaged in manufacturing fixed-head discs and tape drives, video recording and display equipment, and clustered terminal systems—an industry leader in future development within these product areas.

We are headquartered in Sunnyvale, California in a ninety-three thousand square foot complex; with additional manufacturing in Singapore, and sales and service centers in major U.S. and European markets.

In our thirteen years to date (under the banners of Data Disc and Bright), we have served an ever-widening spectrum of clientele, both large and small—computer systems manufacturers, prime users, and military and governmental organizations.

We would sincerely welcome the opportunity to be of service to you, too.

AMCOMP Inc.
686 West Maude Avenue,
Sunnyvale, CA 94086
(408) 732-7330.

AMCOMP

card or collect) which involves a telephone company operator.

Available under AT&T tariff FCC#259 is In-WATS service. While this service also experienced recent rate increases, the proportion of increase was far less than those imposed on other switched tariffs.

Many *voice* communication applications have implemented In-WATS service, providing lower communications costs for customer service and customer inquiry applications such as hotel and rent-a-car reservations. All use the In-WATS tariff to allow customers to reach a centralized reservation center. However, use of the In-WATS tariff in *data* communications applications has been extremely limited. In the past, rate differential between In-WATS service and other switched network services has not been significant. In view of the recent increases, however, In-WATS service for switched connections offers major cost advantages to data communications users.

TABLE 1

Interstate In-WATS

Total Interstate Incoming Data Calls		
Data Calls	Connection Minutes	Collect Calling Costs
2184	13,039	$7398.95
Recommended In-WATS (Band 5)		
Total Monthly Minutes	13,039	
Average Hour Usage	46.6 CCS	
Grade of Service	P04	
Line 1	5413 minutes FBD	
Line 2	4239 minutes MT (FBD)	
Line 3	2673 minutes MT	
Line 4	714 minutes MT	
One Band 5 FBD Service (two lines)		$1675.00
One Band 5 MT Service (two lines)		$1099.06
Total In-WATS Cost		$2774.06
Net Monthly Savings		$4624.89

In-WATS service is easily recognized by the unique 800 area code designation, which remote users can dial without a toll call penalty to access a centralized facility at which the service is installed. The present In-WATS tariff reflects a configuration revision implemented in the spring of 1975 which provides a minimum of two In-WATS lines for each unique In-WATS service ordered. Prior to this, an In-WATS customer was charged for each individual line.

Most costs incurred by the telephone company in establishing a switched network connection occur during initial setup of the actual connection. Telephone system users who experience excessive busy signals create an adverse revenue situation for the telephone companies. If a remote location in California calls a number in New York City only to find that it is busy, the California caller will hang up and attempt to place the call later. In effect, the phone company already incurred the majority of the cost by establishing the connection only to find a busy condition. The call was then disconnected without the telephone companies' obtaining revenue.

When In-WATS service is installed, volume of calls attempting to establish connection to that In-WATS number is significantly higher than volume of calls being placed to a normal dial access number. As a result, the incidence of calls experiencing busy signals is higher. In order to minimize this adverse situation, the phone company decided to increase the probability that a call attempting to reach an In-WATS number would be completed successfully. With the present tariff, two lines are installed when a single initial In-WATS service is ordered, even though the customer is charged for only one line. Therefore, two calls can be in progress simultaneously, significantly reducing both the number of busy signals and the number of redialed calls.

Key to this advantage of In-WATS service is the definition of a unique In-WATS service. As with the more familiar Out-WATS service, Interstate In-WATS service is divided into five bands. Band 1 typically provides access from states that are adjacent to the state in which the service is installed. Band 2 provides access from states that are adjacent to those adjacent states, etc. Band 5 In-WATS service can accept calls from any telephone in the continental U.S. with the exception of calls originating from within the state in which the service is installed.

In addition, there are two billing procedures for In-WATS. A full Business Day (FBD) charges a fixed price per month for each In-WATS service and permits up to 240 hours of usage each month on each line. Usage beyond this is charged at a minimal per hour rate. Measured Time (MT) In-WATS establishes a minimal monthly billing for each In-WATS line for the first ten hours of actual usage. Any usage beyond that is charged on a per hour rate.

In-WATS service therefore is a combination of a unique band designation and unique billing procedure. If a user needs four band 5 In-WATS lines (two FBD lines and two MT lines), the telephone company will install the four lines, but will bill for one band 5 FBD and one band 5 MT In-WATS service. If another band 5 MT line were required, the additional In-WATS service would be installed with only one line since it is no longer unique to this particular installation.

Table 1 is an example of savings potential available with Interstate In-WATS. Data for Table 1 have been compiled from a computer center accessed by collect calls from remote terminals; this was designed to avoid calling costs to the remote user. In a typical month sampled, 13,039 minutes of data transmission incurred a collect calling cost of $7398.95. As these remote terminals are located throughout the U.S., it

Hughes' low-cost C-9 display terminal makes a minicomputer work like a giant.

Here's an interactive graphic terminal that does with hardware what most terminals need software to do. It needs only a mini-computer or telecommunications coupler and a 110-volt outlet to give you a ready-to-work system. And it costs less than $10,000.

More for your money

The new C-9 terminal offers high resolution, selective erase, serial interface (standard), and several other features otherwise offered only by units costing almost twice as much—like 17-inch diagonal, 1029-line-scan, cathode-ray-tube video monitor with high light output screen for easy daylight viewing....computer independent zoom and pan....a joystick for graphics and alpha-numerics interaction....a hardware graphic processor for scaling and rotating graphics and alpha-numerics.

The architecture of the terminal embodies a micro-processor driven by micro-programs contained in read-only memories. A serial interface connecting the detached keyboard to the CRT display eliminates restrictions imposed by parallel interfaces used in other models.

Optional features

You can extend the C-9's capability even further with options like enhanced graphic hardware package with rotations, reflections, and line-texturing features or programmable gray levels for graphics (16 levels) and digital raster continuous tone images (256 levels). We also offer parallel interfaces for a variety of minicomputers and interfaces to popular digitizers for local data input and control of the interactive CRT cursor.

The new C-9 offers a continuous writing mode and a new capability which guarantees that writing occurs only during vertical retrace time.

Smoother curves and lower costs

The patented Conographic™ generator, using conic curves to plot curvilinear information, produces smoother curves from much less data, thus requiring less computer memory, simpler software, less computer or telecommunications time. Result: The lowest *total cost of ownership* of any graphic terminal available today.

Many FORTRAN IV software programs are available, including a new set of Tektronix-compatible subroutines. The basic software package, called CONO-PAC, is available at no extra cost.

To find out how your minicomputer can work like a giant for much less cost, contact your local representative, or Hughes Image and Display Products, 6155 El Camino Real, Carlsbad, California 92008. Or call (714) 438-9191.

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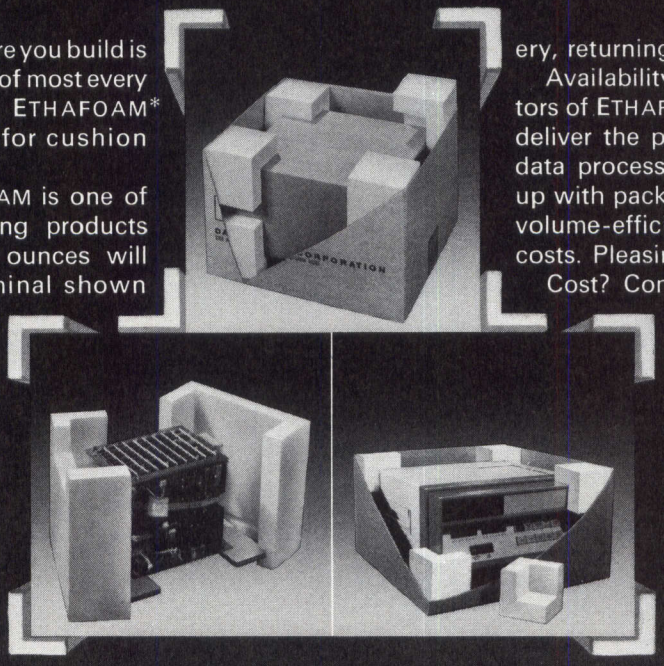
CIRCLE 11 ON INQUIRY CARD

Why cushion packaging for data processing hardware? Because only a couple lbs. keeps more than 200 lbs. in its place.



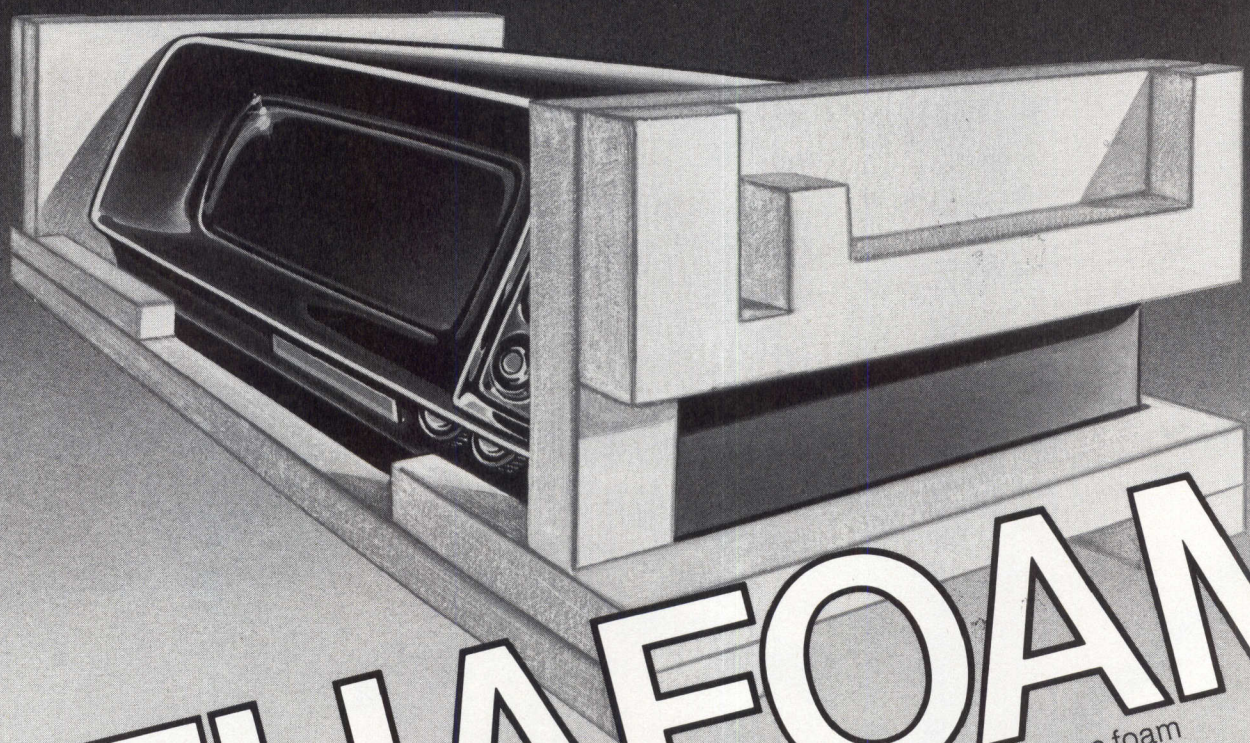
If the data processing hardware you build is subjected to the hard knocks of most every transportation mode, then ETHAFOAM* brand polyethylene foam for cushion packaging is for you.

Pure and simple, ETHAFOAM is one of the most efficient packaging products you can use. Only a few ounces will protect the computer terminal shown here from impact shock, vibration and abrasion. You often get better protection than corrugated inserts provide because ETHAFOAM is a resilient closed-cell plastic foam. Often better protection than molded foam parts, too, because ETHAFOAM won't shatter and boasts excellent recovery, returning to shape after impact.

Availability? Glad you asked. Fabricators of ETHAFOAM can readily design and deliver the parts needed to protect your data processing equipment. You'll wind up with packaging that's lightweight and volume-efficient for low transportation costs. Pleasing in appearance, too.

Cost? Competitive in cushioning, but thanks to its design versatility and other cost-cutting features, ETHAFOAM brand polyethylene foam will probably wind up costing you less.

For more information, check with your nearby fabricator of ETHAFOAM. He's listed on the following page..



ETHAFOAM

brand polyethylene foam

DOW*

DOW CHEMICAL U.S.A.

*Trademark of The Dow Chemical Company

TABLE 2

Interstate In-WATS

Total Interstate Incoming Data Calls		
Data Calls	Connection Minutes	Station Dialed Calling Costs
2184	13,039	$4630.47

Recommended In-WATS (Band 5)		
Total Monthly Minutes	13,039	
Average Hour Usage	46.6 CCS	
Grade of Service	P04	
Line 1	5413 minutes FBD	
Line 2	4239 minutes MT (FBD)	
Line 3	2673 minutes MT	
Line 4	714 minutes MT	
One Band 5 FBD Service (two lines)		$1675.00
One Band 5 MT Service (two lines)		$1099.06
Total In-WATS Cost		$2774.06
Net Monthly Savings		$1856.41

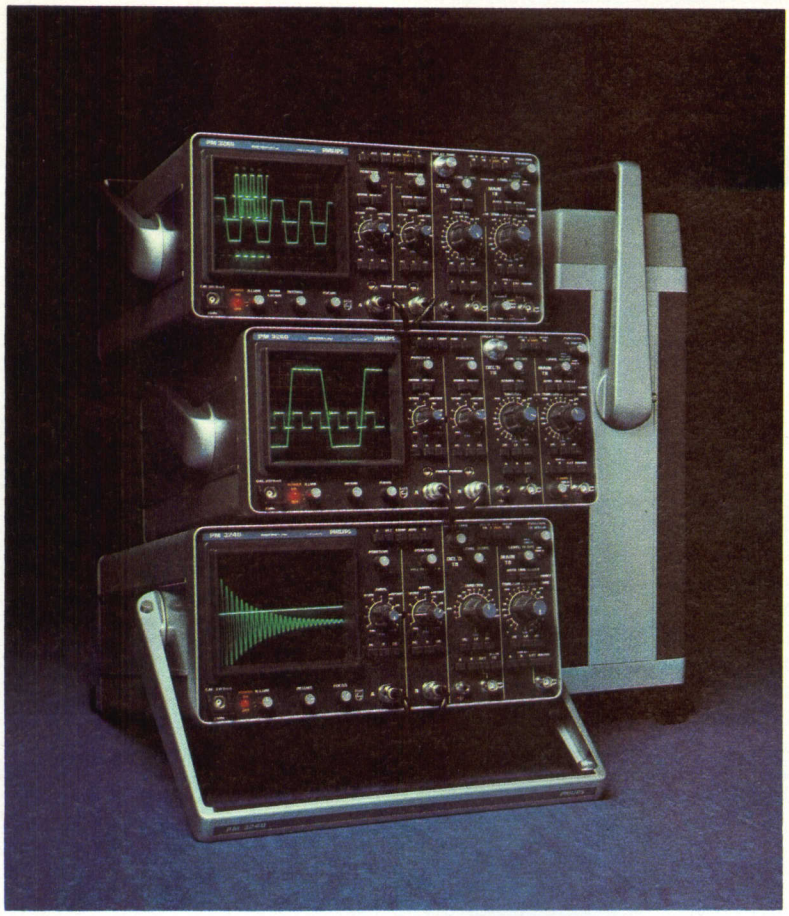
would typically require that band 5 In-WATS service be considered.

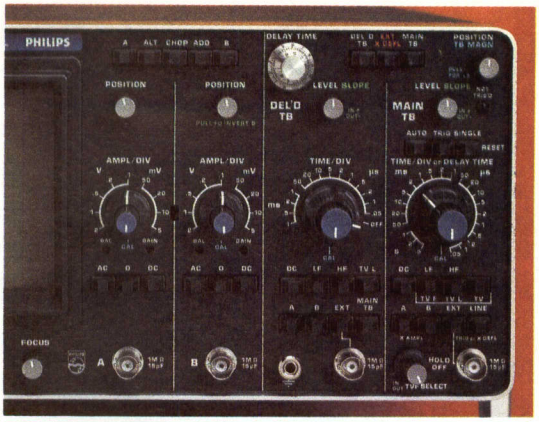
Based on average hourly use, P04 grade of service was established as the required quality of access. P04 is a designation using a Poisson Distribution which indicates number of lines required in an average hour with a busy or blocking factor of no more than four busy calls for each 100 calls attempted. As shown in Table 1, this grade of service can be realized for volume measured with four band 5 In-WATS lines. Recognizing the unique provisions of the In-WATS tariff, the customer would order one band 5 FBD In-WATS Service and one band 5 MT In-WATS service which would provide the desired four lines. Based on Poisson Distribution, total In-WATS monthly cost is estimated to be $2774.06. Net monthly savings of over $4600.00 can be realized in this one application area with use of Interstate In-WATS service.

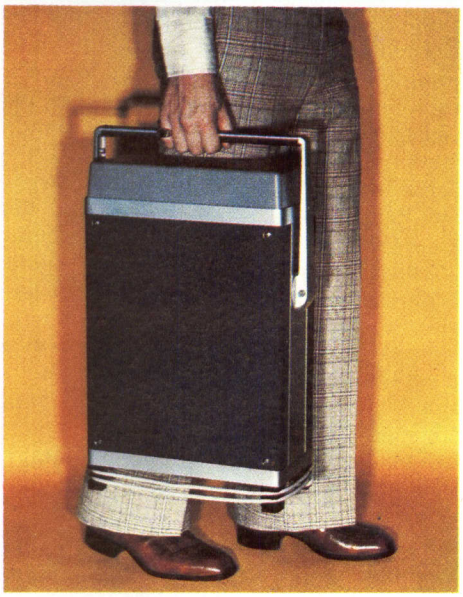
Assuming these same collect calls had been placed as station dial calls, thereby avoiding the telephone company operator-assist charge, they would incur a toll cost of only $4630.47 for the same number of minutes (Table 2). Each remote terminal would be instructed to direct dial the central computer and either pay for their toll call completely or have unique billing rendered by the telephone company for each remote terminal dial access line. Even though direct dial calls produce a significant cost reduction, the same In-WATS network can still provide savings of over $1800.00 a month.

For applications utilizing more sophisticated remote data terminals capable of transmitting at higher rates (such as 2400 bits/s), use of switched network connections can offer significant advantages with respect to transmission efficiency, as well as associated central processing costs. Too often system designers are content merely to emulate previous relationships between various tariffs in determining their network design. Use of In-WATS tariff for data transmission has never received significant application because of the post minimal economic advantage between In-WATS and other switched network services.

Due to the recent rate increases and to the unique provisions of the Interstate In-WATS tariff, the tariff in general provides the most reliable and most cost-effective means of interactive or time-sharing system access. Any computer communications system which uses a number of remote terminals on an interactive or time-sharing basis should evaluate their present transmission loading with respect to the tariff. The majority of existing systems will no doubt discover a significantly lower cost common access method while also realizing unlimited network reliability of dialed connection. □







The reasons to buy Philips are ALL IN THE FAMILY!

All the important elements of waveform measurements that you need . . . accuracy, flexibility, ease of use to minimize human error and low cost, are in the Philips family of compacts.

Just as circuits and systems get smaller and faster, so too, do our oscilloscopes.

The 50 MHz model, PM3240, for example, weighs in at a mere 18 1/2 pounds. And because it's used as much outside the lab as in, we've given it a logical front panel layout where every control falls naturally to hand. The PM3240 has also been designed to operate from almost any supply, including DC; to have a bright 8 x 10 cm display and good circuit access for short service down-times on the oscilloscope itself.

MOVING UP TO 120 MHz

For higher bandwidth applications, the 120 MHz model, PM3260 is available. This 19.8 pounds light instrument therefore keeps you well ahead of Schottky TTL speeds and at the same time goes on triggering to over 200 MHz to meet the great majority of ECL applications.

Like the 50 MHz model, the PM3260 includes layout features such as clear separation of the main and delayed timebase, as well as operation from DC plus 100 - 240 V supply having frequencies from 46 - 440 Hz.

DIGITAL DELAY

Find and display the n th bit in a data stream from 1 to 99,999 with a presettable digital delay counter. A TTL-window trigger enables the oscilloscope to display exactly what the tested circuitry reacts to. The PM3261, at 120 MHz, will solve many digital measurement problems with easy to use capabilities never provided in one oscilloscope before.

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For further information, circle 17 on Inquiry Card. For a demonstration, circle 100 on Inquiry Card.

Network Processor Provides Capability for Flexible, Modular Growth

System 4100 Network Processor, an intelligent time division multiplexer, is the first member of the series 4000, which is intended to provide growth flexibility and modularity without cost penalties. The system provides users with dynamic reconfiguration, network performance statistics accumulation, and centralized network control.

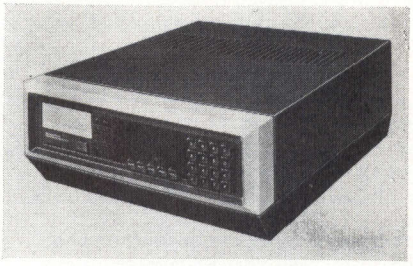
Available from Western Union Information Systems, 82 McKee Dr, Mahwah, NJ 07430, the network processor allows multiple terminals to be multiplexed onto one line operating in point-to-point configurations at a throughput of up to 9600 bits/s in each direction simultaneously. It terminates synchronous terminal lines with speeds to 7200 bits/s, asynchronous lines with speeds to 1200 bits/s; and will handle dedicated or dial-in lines.

The system is controlled by a monolithic 8-bit microprocessor which addresses up to 64K bytes of ROM, p/ROM, or RAM with 16-bit address lines. Its instruction repertoire includes 72 variable length instructions, seven addressing modes, a variable length stack in memory, vectored restart, and markable interrupt. Cycle time is 1 μs and average instruction execution requires from 2 to 4 μs.

Users have the ability to structure communications networks without worrying about obsolescence. As the network grows, new configurations can be down-loaded either from the host processor or from the keypad on the system's operator panel. Through the panel, system personnel can monitor the equipment, analyze internal operations, and localize hardware and network malfunctions.

Options include autospeed control which permits line speed to be determined for dial-in terminals, with a maximum of four speeds being used on any line; a tandem operation option permits drop, insert, and bypass features at each node. Using a line contention option, dedicated lines on different system units may operate on a common slot in a multiplexer network. Low traffic lines may share trunk capacity without dedication of a needed time slot to a single line source. When a line completes transmission, the slot is released automatically for assignment to the next request.

Circle 140 on Inquiry Card

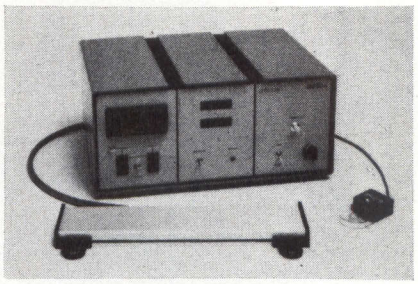


Western Union Information Systems' model 4100 intelligent time-division multiplexer allows users to restructure configurations either from the host processor or the keypad on its operator panel. Panel functions also permit the operator to monitor equipment, analyze internal operations, and localize hardware and network malfunctions

Sonic Digitizer Locates Points Through Triangulation

NT series sonic digitizers produce triangular coordinates, rather than orthogonal, using two solid-state point sensors mounted at the ends of a single bar. Since sensors are mounted along only one side of the display, they allow free movement anywhere on the surface. Units, available from Science Accessories Corp, 970 Kings Hwy W, Southport, CT 06490, provide 0.01" or 0.1-mm/count resolution and 0.1% of full scale accuracy, without requiring a special digitizing surface.

Sonic digitizers locate points on a plane by generating a supersonic pulse at the end of a stylus or cursor placed over the point in question. Using air as the ranging medium, the time required for the pulse to reach the sensors is measured to determine the distance of the point from the sensors. While previously available units used two linear microphones located at right angles to one another as sensors, and produced orthogonal coordinates, the NT series uses two solid-state point sensors (ears) mounted at the ends of a single bar, and produces triangular coordinates.



NT series sonic digitizers consist of sensor bar, containing two point sensors and preamplifiers, electronics package, and cursor or stylus. Measuring the time required for sonic pulses to travel from the point in question to the sensors, the unit provides the location of the point in binary or BCD code

NT-101, basic model in the series, consists of stylus or cursor, electronics package, and sensor bar. The stylus is used where speed is important or where hardcopy trace is required; the cursor where accuracy is necessary. Each incorporates a source for the supersonic ranging pulses. The stylus has a pressure switch which is automatically activated when the point is touched to the display surface; cursor has a hand-operated button to signal when digitization is desired.

Electronics package generates the power for a supersonic pulse each time a signal is received from an external source or the stylus touches the surface. It also signals "ready" to external controls, signals when sonic energy reaches the sensor, and provides a "busy" signal during digitization.

Sensor bar can vary in length from 8½ to 48" permitting digitization over a 36 x 48" area with stylus or 17 x 24" with cursor or stylus. It contains two point sensors and preamplifier electronics. If necessary the bar can be eliminated and the sensors mounted separately.

Outputs from the -101 are in the form of two gating signals; the -201's output consists of ranges to each sensor in binary form. In addition to digital output, the -211 also incorporates compensation to correct for minor differences in the speed of sound which occur with air temperature variations.

(Continued on p 35)

INNOVATIONS FROM

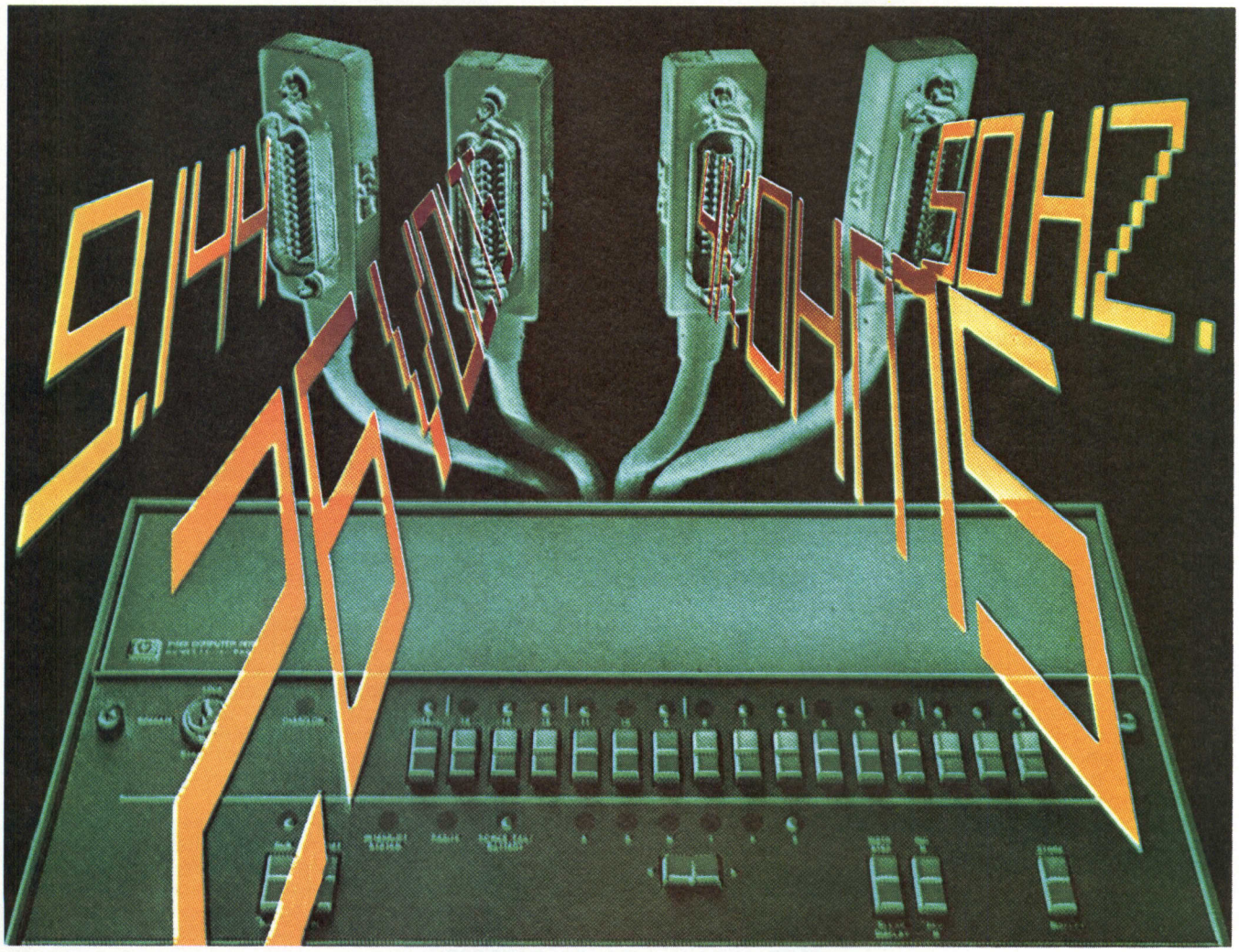
HEWLETT-PACKARD

COMPUTER ADVANCES

DATA BUS STANDARD SIMPLIFIES INTERFACING.

An essential "missing link" which will help the measurement and computation industries achieve their combined growth potential is a new standardized, digital, data bus interface. Today, non-standard interface links are costly and complex. The movement toward distributed processing with minicomputers, and distributed intelligence in peripherals and instruments, is being accelerated by new LSI and microprocessor technology. These trends compound the interface problem and demand a digital data bus standard for interfacing computers, calculators, instruments, and peripherals. The new IEEE-488 standard meets this demand simply and effectively.

Standards are important as technology evolves. Think how standard lightbulb sockets have allowed the electrical industry to lower costs and provide inexpensive lighting to millions. Think how standardizing highway traffic flow has encouraged entire new



HEWLETT-PACKARD'S HP-IB/21MX MINICOMPUTER. SIMPLICITY AND POWER FOR AUTOMATIC TESTING.

vehicle industries and has made satellite communities practical. Think how standard telephone addressing and electronics has stimulated worldwide communication.

These elements of mechanical connections, traffic paths and message protocols are the same elements key to standardizing the three main categories of digital data communications interfaces. It is encouraging to see new standards in some of these categories beginning to emerge.

First is the digital data path between computers and local terminals. It is low speed (up to 2 Kilobytes/sec) and today the industry generally favors EIA RS232C as the mechanical and electrical standard with ASCII characters for data formats.

Slightly higher speed data transmission (up to 6 Kilobytes/sec) and longer distance transmission such as phone lines require modems and message communication protocols. Today EIA RS232C/RS422/RS423 are the emerging mechanical and electrical standards; also the synchronous, bit oriented protocols (e.g., SDLC/HDLC/ADCCP) are growing in acceptance.

The most recent important standard to emerge, IEEE 488, is in response to a need for medium speed (up to 1 megabyte/sec), local interfacing of instruments, controllers and peripherals.

This IEEE-488 interface bus standardizes several characteristics. The mechanical interface is standardized much like the light bulb socket, i.e., cables and metric connectors are specified. It includes electrical characteristics, and traffic path standards analogous to highway flow regulations. And there the functional message protocol standards such as those which enable direct telephone dialing. The result is an interface bus that allows interconnected system components to communicate effectively and in an orderly, unambiguous manner.

By standardizing on the IEEE-488, industry users are free to focus their creative energies on higher level problems. Training and explanation becomes easier, and users benefit through multiple vendor availability and mass production. Cooperation on such standards can provide the catalyst for increased synergism between computers, calculators measurement instruments and peripherals and can help stimulate the explosive growth and efficiencies seen in other industries that profited from standardization.

EVOLUTION OF A STANDARD

Often at Hewlett-Packard, the definition of a new product results from an engineer's frustration at not having the right instrument to solve his problem. The solution, i.e., the design of a new instrument, comes either from that engineer or one at the next bench. This historically is known as the "next bench" phenomenon. Many HP products have resulted from an engineer solving his specific need, only to discover that he has designed a solution to a industry wide problem.

Such was the case several years ago. Hewlett-Packard engineers observed that other HP divisions were producing instruments that were difficult to interface together. The interface problem these engineers experienced was exactly the same problem encountered by engineers at nearby benches. Engineers in several divisions worked together to solve this local device interface problem. Their work in turn helped create the original interface concepts which served as the basis for discussion at national and international standard activities. European and American manufacturers and users were aware of the problems and worked toward common solutions. Their four years of joint efforts resulted in a medium speed digital interface standard. This was adopted as IEEE Standard 488-1975. It was subsequently adopted by the American National Standards Institute as ANSI Standard MC1.1. There is the possibility that the interface system concept will soon be internationally accepted by the IEC to serve manufacturers and users regardless of national origin. HP has implemented this standard as the HP-IB "Hewlett-Packard Interface Bus."

PUTTING THE HP-IB* TO WORK

New HP-IB/21MX Minicomputer Controls Multiple Instrument Clusters, Accesses Data and Develops New Programs—All at the same time.

In the past, interfacing instrumentation systems for measurement and test applications has been complex and costly. Not any more. With the HP-IB/21MX Minicomputer, automatic test systems for production, and laboratory research; and automatic data acquisition systems can be implemented more easily and simply. HP offers for the first time a minicomputer with a multi-programming operating system as a controller for instruments which conform to the IEEE-488 standard.

Take the simplicity of HP-IB interfacing. Add HP's 21MX Minicomputer and Real-Time Executive (RTE) software for the power and control. Choose from over 100 HP and non-HP IEEE-488 compatible instruments, calculators and peripherals to handle test and measurement. Within hours, flexible and powerful measurement and test systems can be up and running. OEM's, freed from device interface problems, can focus their resources on the customer interface.

Controls multiple instrument clusters. Because the Real-Time HP-IB Minicomputer supports multi-programming, it can simultaneously control several HP-IB clusters of up to 14 instruments each. Test/measurement equipment can be organized into multiple physical or functional groups—each connected to the HP-IB/21MX Minicomputer by its own HP-IB interface bus.

New instrument clusters can be added or reconfigured without downtime or affect on existing clusters.

Systems can grow as needs grow. And, because of the new Real-Time HP-IB Minicomputer's speed as an HP-IB controller, throughput is increased in high volume or production testing.

Consolidates test measurement data. The Real-Time HP-IB Minicomputer's multi-priority program scheduling allows highest priority and alarm tasks to run immediately and devotes "idle" time to other chores such as correlating and analyzing data, or producing timely management reports.

HP's new IMAGE/1000 data base management software adds a complete set of "software tools" for consolidating files into a single data base. Once the data base is established, IMAGE/1000's English-like QUERY language lets users interactively find any stored information by searching under multiple "key values" such as a part number, vendor code or failure type. IMAGE/1000 permits easy report generation with automatic sorting, summation, pagination and averaging.

Allows concurrent program development in multiple languages. While the Real-Time HP-IB/21MX Minicomputer is busy controlling instruments and consolidating data, it can also be used for program development.

For the first time engineers can readily access instruments and devices

*HP-IB is Hewlett-Packard's implementation of IEEE Standard 488 and identical ANSI Standard MC1.1—Digital Interface for Programmable Instrumentation.

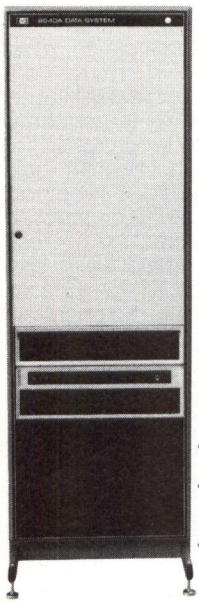
via the IEEE-488 and with the popular scientific language FORTRAN IV. HP's Multi-User Real-Time BASIC, which can be learned in a few hours, and HP's assembly language are available. This Multi-lingual approach brings the utilization of HP-IB to a wider cross section of users.

Supports Multiple Terminals. The Real-Time HP-IB Minicomputer also offers multi-terminal accessiblity. Several people can use the system immediately and simultaneously—for program development, data entry or system control. As a result, testing and production data such as quality assurance information is available when needed for decisions.

Augments data networks. Finally, the Real-Time HP-IB/21MX Minicomputer extends the data gathering capabilities of today's computer networks. Off-the-shelf hardware/software data communications packages make it easy to connect the HP-IB/21MX Minicomputer to other HP 21MX computers or to link it upwards to a central HP 3000 or IBM 360/370.

Simple HP-IB interfacing plus 21MX power: That's the Real-Time HP-IB/21MX Minicomputer story. For more information on how these systems can help you gain management control over your automated testing, circle A on the attached reply card.

HP-IB/21MX JUST MADE AUTOMATED TESTING EASIER AND FASTER



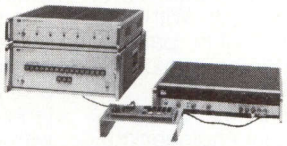
Multiple Instrument Clusters
Each independent cluster of up to 14 instruments is connected to the 21MX Minicomputer via a separate HP-IB interface cable.

Add New Clusters Easily
With on-line configuration capability, new independent instrument clusters can be added or changed without downtime or affect on existing clusters. Programming test procedures are simple BASIC "PRINT/READ" FORTRAN "WRITE/READ" statements.

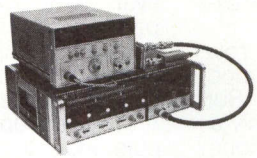
HP-IB

HP-IB

HP-IB



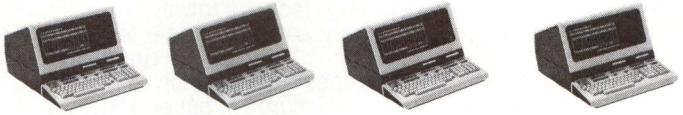
Component Test Clusters
A monolithic DAC is tested with an HP multiprogrammer and digital volt meter.



Subassembly Test Cluster
At the same time C-band microwave amplifiers can be tested with a sweep oscillator and an RF power meter.

Instrument Test Cluster
And, at the same time, a sweep oscillator can be tested with a frequency counter.

BASIC FORTRAN IV QUERY HP ASSEMBLY



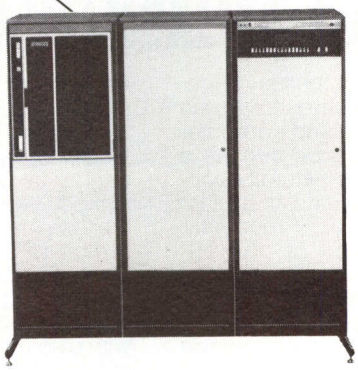
Multiple Terminals for Concurrent Program Development or Data Base Access
The Real-Time HP-IB/21MX Minicomputer permits fast multi-lingual program development or data access with new IMAGE/1000 by several users simultaneously.

New Real-Time HP-IB/21MX Minicomputer
The HP-IB/21MX Minicomputer which automates test/measurement procedures, and permits concurrent program development and data retrieval consists of a 21MX Minicomputer and cartridge disc memory, managed by HP's RTE-II or RTE-III Real-Time Executive software. Prices are $19,000 for non-disc and $34,000 for disc based systems. Each HP-IB interface can be added to a 21MX Minicomputer for $1,000 U.S.*

For a demonstration of the Real-Time HP-IB/21MX Minicomputer, check A on the reply card.

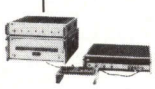
*Domestic Prices FOB California.

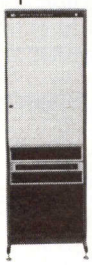
Computer Network Connections



Central EDP
HP supported hardware and software connect the HP-IB/21MX Minicomputer to other 21MX Minicomputers or to an HP 3000 or IBM 360/370 in a distributed management information network.

HP-IB





Incoming Inspection Satellite
A remote HP-IB/21MX Minicomputer in the nearby incoming components inspection department consolidates test data via the network connection system.

IMPROVING THE TESTING OF COMPLEX PRINTED CIRCUIT BOARDS...

Due to the astronomical numbers of circuit elements and interconnections on today's PCB's, the production of perfect boards is rare. Therefore, automated fault finding methods that are comprehensive and fast are of central importance to economy-minded production managers. Low quality boards that leave the company mean high warranty costs.

In just a few years, the digital printed circuit board has exploded in size and complexity so dramatically that boards with 200 integrated circuits or 10,000 logic gates are not uncommon. Testing boards can make life difficult for designers, production managers and customer service managers alike.

The design engineer needs to be totally sure that the design on the drawing board is testable, and to what extent.

The production manager's role in life is to produce quantities of good boards, faster and economically. But the common practice of testing only a typical 50 percent of a board's functions falls far short of a rigorous production test.

An industry rule of thumb is that each IC on a board will account for a 1 percent failure rate. A 100-IC board, would average one failure per board. If only 50 percent of a board is tested, a large percentage of passed boards will still have faults. The use of manual or semi-manual fault locating techniques costs precious troubleshooting hours.

Then, there is the customer service department! Here, the pressure especially builds to have faster and more accurate testing methods.

And ultimately, this deteriorating situation is an anathema to company executives who are aware that fully 30 to 40 percent of production costs for today's digital PCB's is attributable to testing them and assuring their quality.

Some good news . . . While the complexity of printed circuit boards has exponentially increased, the price of powerful minicomputers has sharply decreased. Consider the advantages of testing PCB's with a computerized system.

At the earliest design stages, the board's component connections are entered into the system by a simple and standard format. The minicomputer's stored memory incorporates a comprehensive library of commercially available IC's and other circuit components and how they work. With this data, and employing built-in pattern generating procedures, the minicomputer "simulates" the board.

Is the board testable? The computer indicates to the test engineer the quality of the test, that is, the percentage of all possible faults on the board that can be detected as presently designed.

Knowing quantitatively how testable the new design is, is extremely valuable. It indicates to the designer whether a need exists to add test points and test paths to increase the testability. The judicious placement of a single test point can sometimes lead to a dramatic increase in board testability. With the design still only on paper, the cost of the change is only slightly more than the cost of a pencil equipped with an eraser.

At the same time that the computer software programs check the design, the test program is produced. This will be used in the production stage and later for customer service. The board is now ready for production.

Using a minicomputer-based dedicated system, the production managers test tools can be the same software programs generated by the computer automatically from the design stage circuit descriptions.

The board is placed in an easy-to-operate fixture adaptable to most PCB's without expensive or time consuming construction of special fixtures.

Throughput is key to economy. A board tester should be designed for throughput. Testing the board's logic takes place in a matter of seconds. Then the tester directs the operator to move a probe to areas that are not testable from the edge connectors, to precisely diagnose faults. Simple English language commands enable operators with little technical training to perform the job.

The customer service manager can use the same test programs so software costs, amortized over three departments, are minimized. There may be hundreds of different PCB's handled by the service department, so testing software must allow for efficient on-line recall of the board testing programs.

The prime cost of running the customer service department is troubleshooting. The system must find faults and find them fast. Tests must be thorough so that faulty boards are not returned to the field. The "no trouble found cycle," where faulty boards cycle between customer and service center, will then be broken. Engineers in the lab, production areas and customer service centers benefit from this PC Board testing approach.

THE DTS-70 DIGITAL TEST SYSTEM THROUGHPUT, RELIABILITY AND SIMPLICITY

Hewlett-Packard builds thousands of complex PC boards for use in instruments, calculators and computer systems. Each HP division run as a small company itself, is naturally concerned with the design and manufacture of fault free boards. Frequently, problems encountered at one HP manufacturing factory are the same as the next. The familiar "next bench" phenomenon has evolved to a grander scale to the "next factory" phenomenon. Engineers in the Automatic Measurement Division knew that a system designed to solve their own and other HP Divisions PC board test problems would be a solution for other companies as well. The system they designed—the new DTS-70 Digital Test System—represents a new dimension in digital PC board testing.

The DTS-70 system permits up to three test stations to operate with a single 21MX Minicomputer equipped with disc memory. This lowers the cost of production testing significantly. Concurrent with one test station, a preparation station can be used by designers to enter new circuits for initial design analysis. Optional test generation software called TESTAID-III simplifies and speeds PC board test preparation.

The DTS-70 system will test large circuit boards in a few seconds. If a fault is present, the operator is given information necessary to locate it in about one to two minutes. A "guided probe" is used for diagnoses. The minicomputer provides information as to

where and how the probe should be placed by the operator.

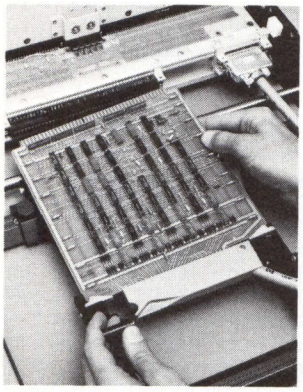
For efficient system design the HP-IB interface bus is used as the DTS-70 interface bus. For example the HP-IB interfaces the DTS-70 to the repair-ticket printer which produces hardcopy fault isolation information that can be conveniently attached to fault boards sent for repair.

The DTS-70 system was designed with production problems in mind and it can be used by unskilled operators. Dialogue instructions are easily and quickly communicated by the system through an HP-2640 keyboard-video terminal.

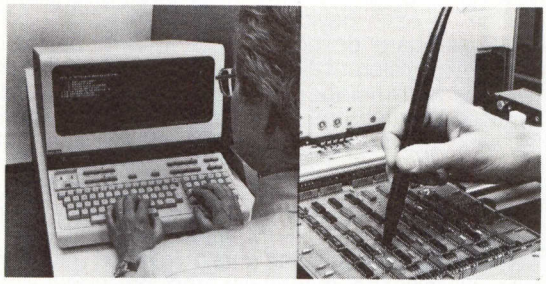
When not being used for testing, the powerful minicomputer system can perform tasks such as production scheduling, inventory control, shop-loading and materials requirements planning analyses.

For more information on the DTS-70 circle B on the reply card.

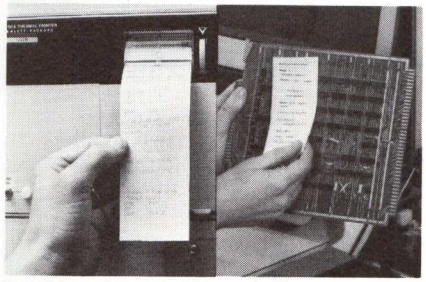
HP 21MX BASED DTS-70 SPEEDS PC BOARD TESTING



The board under test rides smoothly on guides and is secured in position with lever action designed to minimize operator fatigue.



Fault isolation is made easy for operators with a minimum of training. Instruction messages appear on the display indicating precisely where the probe should be placed to isolate the faulty circuit.



Simply worded repair instructions are produced on a hardcopy ticket. This ticket is attached to the faulty board for use at the repair station.

FAST, ACCURATE FAULT LOCATION

Determining if a PC board is good or not, is only a first step. The really important next step is to actually locate the fault so the board can be repaired. DTS-70's FASTRACE software searches for these faults using two techniques. When used in conjunction with each other, **Fault Signature Search and Guided Probing work much the same as do the famous sleuth team of Sherlock Holmes and Dr. Watson.**

When a crime occurs, Sherlock, with his keen power of deduction, evaluates people even remotely associated with the crime. He then obtains a "criminal profile" and comes up with a list of prime suspects who match this profile. If there is only one prime suspect matching the profile then the crime has been solved. More likely, there are several prime suspects remaining after Sherlock's initial investigation.

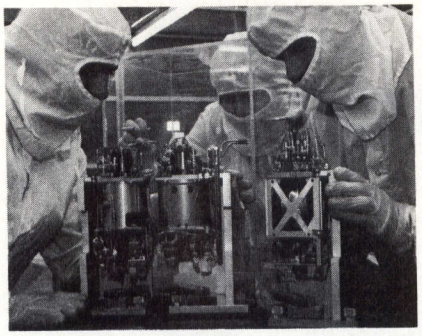
DTS-70 first uses an Automatic Fault Dictionary Look Up technique which consists of searching through a list of faulty output patterns generated by the TESTAID Simulator for a match with the output pattern measured from the board being tested. If a match is found, then a list of "fault candidates" associated with the measured faulty output pattern is noted. This is analogous to Sherlock Holmes' contribution to solving the mystery. Then Dr. Watson questions each prime suspect and in turn goes through an exhaustive evaluation of every clue. Dr. Watson leaves no stone unturned in his pursuit of the criminal and when he is convinced of the culprit's identity, he is always right!

Then a technique takes over which guides the operator to probe for additional information. When a bad signal is measured, its driving signals are also measured in a logic "backtrace" sequence. Final isolation of the fault occurs by actually measuring the point at which the failure exists. Using the Fault Signature/Guided Probe approach, the DTS-70 locates faults with unprecedented speed, typically less than a minute and, with Sherlock Holmes accuracy.

For more information on fast, accurate fault location circle C on the reply card.

USER TESTED PERFORMANCE

HP-IB improves testing efficiency for TRW
Computer testing debugs new model cars for Ford



TRW's advanced technology will be applied this summer when a computer life detection instrument package they designed will probe for life on Mars.

At TRW, the design of a computerized life detection instrument package that will probe for biological signs of life on Mars this summer, is an example of the technology applied by this designer and manufacturer of scientific, military and commercial space craft systems. Precise measurement and testing is a critical aspect of activities at their Space Pack facility in Redondo Beach, California. There the company's Defense and Space Systems Group relies on 25 HP 2100/21-MX computer based Scientific and Measurement Systems for engineering and manufacturing testing.

Don Broutt, who manages TRW's automatic test systems department, adopted the HP Interface Bus to link numerous test instruments to his HP computers and to numerous HP calculators.

"Many of our programs involve extremely limited production runs . . . some products, for example, are one of a kind. Before adopting the interface bus, our efforts to reestablish test stations for each program was like reinventing the wheel. Now when setting up a new test station with the HP-IB, we can easily add or reconfigure instruments in a computerized network with minimal set up time," explains Broutt.

With improved flexibility comes improved cost, according to Broutt. Pre HP-IB testing required specially engineered printed circuit board interfaces for each unique test device. If a device served as both a "listener" and "talker" it required two boards. Now one board within a computer allows interfacing with up to 14 devices meeting the IEEE-488 standard. Similarly a single standard cable now replaces specially-engineered cables formerly required for each unique test instrument.

"In our pre-HP-IB testing, we wrote special driver software for each unique device. This consumed excessive amounts of computer memory. Now our engineers simply use a subroutine for each device to access an HP-IB standard driver. Gone is time consuming reference to hand books for device translation. Once a subroutine is written, the device interface is transparent to our engineers," relates Broutt.

Now, with the growing availability of test devices using IEEE-488 and the expanding use of the HP Interface Bus, TRW, is able to reduce the cost of interface design. The manpower and resources formerly allocated to this function, can now be applied to other priority projects.

A Hewlett-Packard Minicomputer monitors Ford's Shaker System which simulates the stress and strains of normal and extreme driving conditions.

Ford Motor Company's debugging of prototype cars increases in complexity from one year's model to the next. Electrical and mechanical systems are enhanced to help control product cost, more stringent emission control and safety standards are mandated yearly, and an extremely competitive market places emphasis on product innovation and reliability.

At Ford Motor Company, a comprehensive computerized testing program enables the Car Engineering and Product Development Groups to meet these challenges.

Key to the testing programs are six HP 2100 based Scientific and Measurement Systems computers, combined with an innovative mix of analog measuring devices, torture chambers, testing apparatus and high speed minicomputer data acquisition stations.

With computerization, test results are now available four times faster than previously, and in some tests, data is processed as it is captured.

Prior to Ford's marriage of HP computers with measuring devices, constant operator intervention was required to set calibrations and adjust measuring instruments. Tests were not nearly as comprehensive as with its computerized system.

One test called the Shaker System involves computer testing of model cars that simulates driving upon a variety of surface conditions—from normal driving to extremes such as speeding a car down a tortuous pair of railroad tracks.

When tested under the Shaker System, each wheel of the car is placed on a hydraulic ram. The front wheels are excited in phase and 180 degrees out of phase. Vibrations sensed from accelerometers attached to critical points, like the steering column, are converted digitally for the computer's analysis. The HP minicomputer controls the programmable generator and the two-channel digital to analog converter. Resulting signals activate the ram's servo control mechanisms.

Each discrete point monitored contains a natural or built-in frequency. As the exercised frequency implanted by the HP 9600 approaches the natural frequency, a resonance effect appears, in effect magnifying the vibration.

Computerized statistics and plots enable Ford engineers to design automobiles with natural frequencies attenuated to an accepted level or moved out of the driving range of normal operations to preclude the resonance effect.

When asked to compare the preciseness of his company's computerized testing to prior methods, a Ford engineer replied: "Like measuring something with a micrometer instead of a ruler."

HEWLETT hp PACKARD

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HEWLETT-PACKARD COMPUTER ADVANCES

The programmable NT-501 is preprogrammed to convert dimensions according to a preselected scale, measure length of a line, establish an origin on a plane, provide digital coordinates for a point on a plane, or calculate the area beneath or within a figure on the plane. Choice of program is made by manipulating a thumbwheel switch.

Outputs are in the users' choice of binary or BCD coding. A display indicates which operating mode has been selected. The unit is capable of interfacing with magnetic tape, punched paper tape, or punched card units; with RS-232 or current-loop communications; or with minicomputers, programmable calculators, or analog devices.

Prices for the units range from $800 for the -101 (single unit) to $4950 for the -501.

Circle 141 on Inquiry Card

Band Printer, Rotating Memory Products Aimed at Minicomputer Systems

Horizontal-font band printers which produce 300, 600, or 900 lines/min., and rotating memory equipment aimed at minicomputer and small business system applications represent the contribution that Control Data Corp, Minneapolis, MN 55400 is making to the minicomputer systems market. Printers use a thin stainless steel band and print on a horizontal surface to provide high quality characters at 10 or 15 char/in.; disc units include a mini-module drive using "Winchester" technology, a fixed disc drive, and a floppy disc subsystem.

Band Printers

Using a horizontally moving character band, 9380 series printers maintain vertical alignment of characters, and produce uniform density from top to bottom of characters because print hammers impact the band's flat character surface. Operators can change bands in less than 30 s without removing the ribbon; eleven different bands are available with 48-, 64-, 96-, or 128-char sets. Once the band is in place, the printer automatically adjusts to the size of the character set.

A patented control circuit maintains ribbon travel at constant speed and tension, allowing the 2"-wide ribbon length to be increased to 48 yards for longer life. Fast document throughput is provided by a servomotor-controlled form-feed mechanism that reaches peak paper speed of 20 in./s as the first line advances. Paper motion is monitored photoelectrically, preventing the loss of data if a forms failure occurs. Basic controller used in the printers contains a full line buffer memory. It includes single-ended transmitters and receivers, and allows communications on an input/output cable that can be up to 50 feet long.

Models in the series all provide 132 columns and 64 characters at 10 char/in. in the standard configuration. Model 9383 operating at 300 lines/min., and 9386 at 600 lines/min. are available with a 15-char/in. option. Model 9389 prints at 900 lines/min.

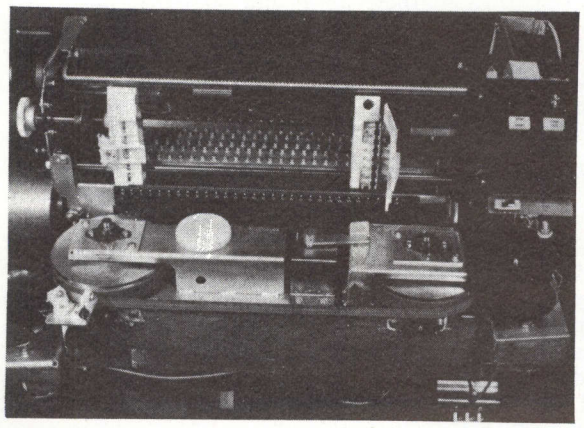
Disc Drives

Rotating memory products include the 24M-byte 9730 mini-module drive. Evolved from the Winchester disc technology, the sealed module contains spindle, recording media, rotary actuator, and read/write heads, making the unit tolerant of various operating environments and virtually maintenance free. Claimed MTBF is 8000 hours. Using fixed-sealed modules for the storage medium, the basic drive accommodates horizontal or vertical mounting.

The smaller capacity Falcon 9414 fixed-disc drive offers 6M- and 12M-byte capacities at a low price because the one or two recording discs are not removable. Basic unit consists of a direct-driven spindle and dc drive motor, head-positioning mechanism, logic chassis, and air filtration system. The read/recovery circuit will operate with or without missing clock patterns such as are found in variable sector formats. Read/write heads are positioned over the discs using a closed-loop proportional servo system.

Using an Intel 8080 microprocessor to control one or two floppy disc drives in a single chassis, 9471 and 9472 flexible disc subsystems provide simple interfaces and handle all complex format and error checking functions internally, for minimal impact on standard hardware and software designs. 3740-formatted data are stored by transferring track and sector addresses of data to the units. The subsystem handles writing and detection of overhead areas, such as record synchronization and check characters for each record.

Circle 142 on Inquiry Card

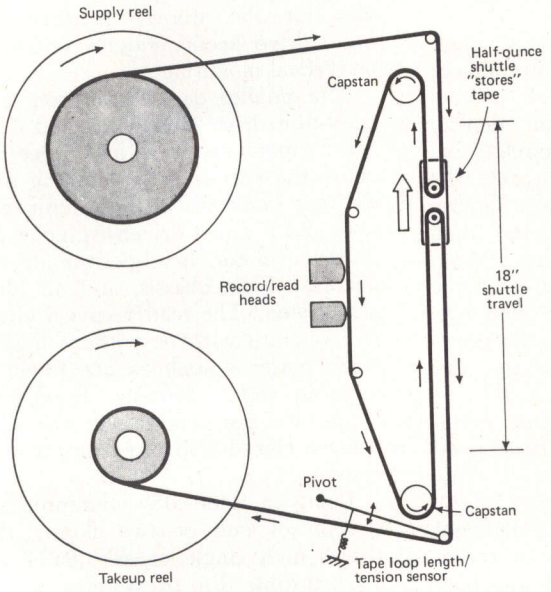


Control Data's 9380 series printer uses a print character band that moves horizontally to provide quality print. Microprocessor control offers applications flexibility

75-in./s Tape Transport Replaces Vacuum Columns With Floating Shuttle

The 75-in./s Floating Shuttle™ tape transport avoids complexities and limitations of current vacuum column transports through use of a lightweight shuttle which buffers tape during start/stop operations. According to its developer, Qantex Div of North Atlantic Industries, Inc, 200 Terminal Dr, Plainview, NY 11803, the electromechanically-buffered digital tape transport incorporates 30% fewer parts than vacuum column transports, resulting in lower weight, simpler design, lower power consumption, improved MTBF, and quieter operation.

During normal start/stop operations, the control capstan of a tape transport brings the tape up to speed or to a complete halt within 5 ms. Since the large take-up and supply reels cannot accelerate or decelerate at this rate, some kind of tape



75-in./s tape transport uses a lightweight "flying shuttle" to buffer tape during start/stop operations, replacing vacuum column and complex tension arm mechanisms. Electromechanical buffering allows Qantex to use 30% fewer parts, and provides low power consumption, improved MTBF, and quiet operation

reservoir or buffer is needed to permit fast acceleration at the capstan and more gradual movement at the reels. Historically, mechanical tension arms have provided the necessary buffering to tape velocities of 45 in./s; at higher speeds vacuum column buffering became necessary because of the ceiling imposed by the mass of the tension arm structure. The flying shuttle concept preserves mechanical simplicity without imposing the limitations on velocity that are introduced by tension arms.

Evolving from the mechanical tension arm concept, the 0.5-oz shuttle is moved up and down by tape pull during acceleration and deceleration, affording the capstan dynamic independence from the slower accelerating supply and takeup reels. In essence, the shuttle replaces the tension arms, thereby eliminating its mass, instead arranging the two tape idlers on a lightweight framework that is constrained to travel up and down in response to capstan acceleration and deceleration.

On read or record command the two capstans will accelerate to full speed within 5 ms. Since the supply reel is stationary, the upper capstan can draw tape only from the shuttle. Consequently, the shuttle is pulled upward, delivering tape at the same time, by capstan rotation. By moving upward, the shuttle also absorbs tape pulled from the downstream side of the record/playback heads by the lower capstan. The shuttle continues its upward displacement, simultaneously increasing the reel motor's drive signals, until the supply and takeup tape reels attain full speed. At dynamic equilibrium, the shuttle remains displaced from its central or neutral position just enough to develop the reel drive signals required for 75-in./s tape velocity.

During deceleration, the shuttle moves downward to absorb tape from the still turning supply reel, which feeds tape out to the gradually decelerating takeup reel.

The floating shuttle tape transport (FSTT) handles tape reels to 10½", recording and reading bidirectionally at 75 in./s, and rewinding at 300 in./s. Standard recording modes are 800 bits/in. NRZI, or 1600 bits/in. phase encoded, providing either 7- or 9-track operation.

Circle 143 on Inquiry Card

Product Line Extensions Include Tape Drive for Uninterruptible Systems

Products introduced by Pertec Corp, Peripheral Equipment Div, 9600 Irondale Ave, Chatsworth, CA 91311, encompass an advanced design series of vacuum column magnetic tape transports, tape drives that operate from batteries for use with uninterruptible systems, 25M- and 50M-byte extensions of D3000 series disc drives, and 12M- and 24M-byte fixed disc drives. Basic features include systems parts commonality, modularity, and high reliability. Interfaces are industry compatible to allow plug replaceable installation. All are geared toward minicomputer applications.

Tape Drives

T1000 vacuum column tape drives incorporate dual 1600/800-bit/in. read-after-write hard-coated heads and feature speeds from 75 to 125 in./s, autoload tape threading, modular electronics, and built-in self-test. Air bearings are designed in at all turnaround points along with ceramic guides; a vacuum capstan provides precise, positive tape handling, and maximum reliability. Among the features that enable the unit to provide the 0.3" interrecord gap necessary for high density group code recording are digital capstan servo, minibuffer vacuum column system, and 1½-hp pneumatic package.

Based on T7000 and T8000A magnetic tape transports, and incorporating a 48-V dc-to-dc converter as well as formatters, two transport series operate with 48-Vdc batteries for use in uninterruptible systems. The converter accepts raw battery power and, through a switching regulator that operates above 20 kHz, converts battery voltage to unregulated dc voltages to supply the regular or buffered formatter as well as the tape transports. Both drive and formatter regulate the dc input into required dc voltages.

The converter provides high "white noise" immunity for reliable operation in hostile noise-producing environments. Options include an input line which remotely synchronizes the converter and minimizes the site noise spectrum, and a remote/local LED display which indicates which fuse has blown when a power failure occurs.

Disc Drives

Designated D3400E and D3600E, these 25M- and 50M-byte units offer four platters, three fixed and one removable cartridge; each platter can be individually write protected. An optical positioning system provides fast, reliable positioning. Sectoring can be mechanical or electronic.

Extending the D1000 family are 24M-byte D1660 and 12M-byte D1460, which use two IBM-3336-type and 2316-type nonremovable platters and provide 4400 and 2200 bits/in., respectively. Moving coil linear motor positioners controlled by electronic servos accomplish reliable positioning

Design with the complete flat cable/connector system.

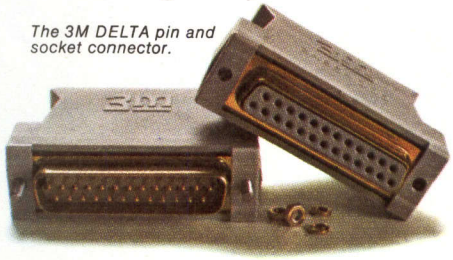
trimming the cable after assembly.

Connector units provide positive alignment with precisely spaced conductors in 3M's flat, flexible PVC cable. The connector contacts strip through the insulation, capture the conductor, and provide a gas-tight pressure connection.

With cable, connectors and assembly tools from one design and manufacturing source, you have added assurance the connection will be made surely, with no shorts or "opens."

And "Scotchflex" now offers you more design freedom than ever. From stock you can choose shielded and non-shielded 24-30 AWG cable with 10 to 50 conductors, and an ever-increasing variety of more than 100 connectors to interface with standard DIP sockets, wrap posts on standard grid patterns, printed circuit boards, or headers for de-pluggable applications. 3M's DELTA "D" type pin and socket connectors are now also available. For full information, write Dept. EAH-1, 3M Center, St. Paul, MN 55101.

The 3M DELTA pin and socket connector.



Assembly-cost savings are built in when you design a package with "Scotchflex" flat cable and connectors. But more important, 3M Company offers you the full reliability of a one-source system: cable *plus* connectors *plus* the inexpensive assembly aids that crimp the connections quickly and securely (with no special operator training required).

The fast, simple "Scotchflex" assembly sequence makes as many as 50 simultaneous multiple connections in seconds, without stripping, soldering or

3M COMPANY

3M's "Scotchflex" line.

See our catalog in EEM—Page 1056.

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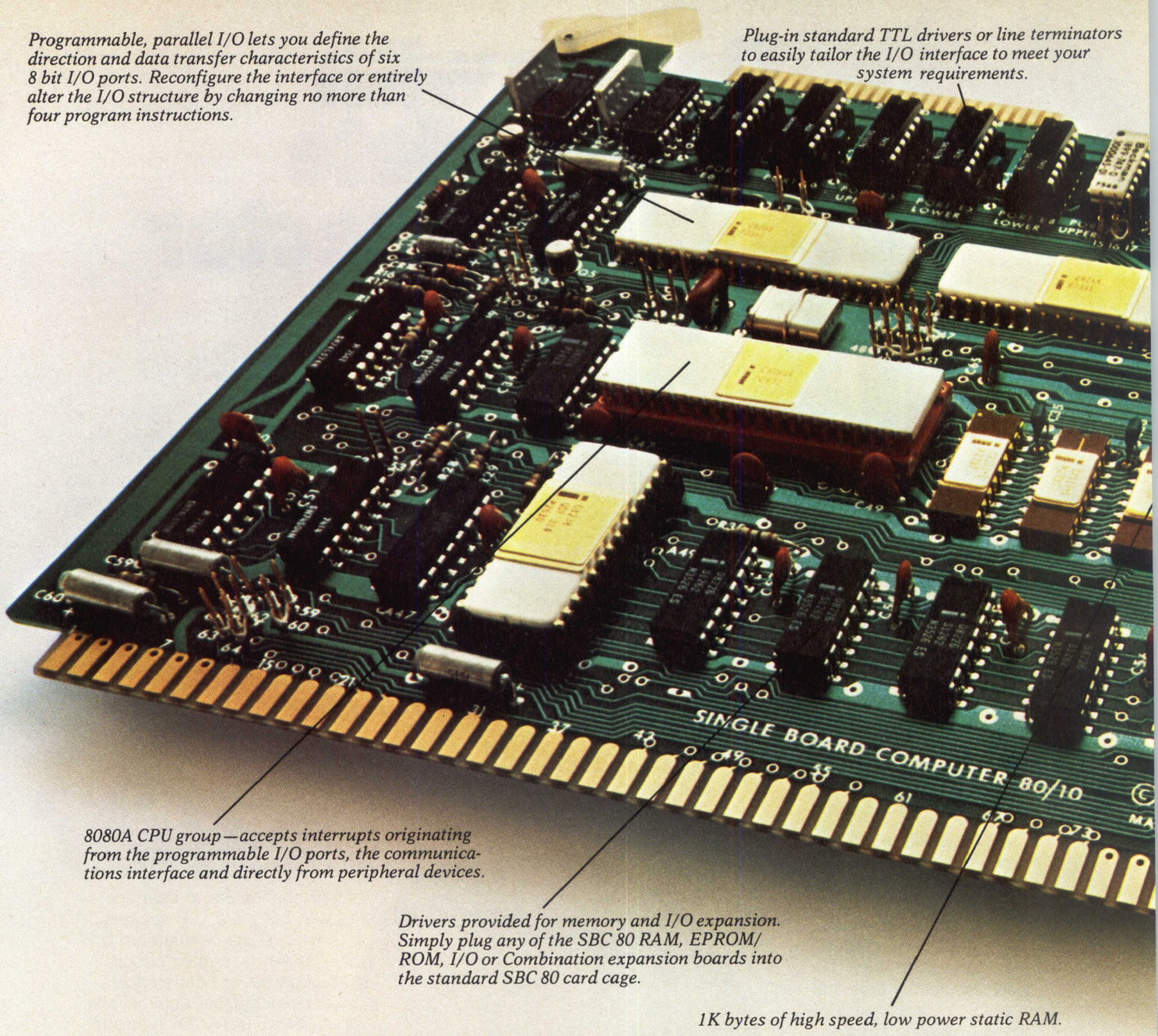
CIRCLE 18 ON INQUIRY CARD



Programmable, parallel I/O lets you define the direction and data transfer characteristics of six 8 bit I/O ports. Reconfigure the interface or entirely alter the I/O structure by changing no more than four program instructions.

Plug-in standard TTL drivers or line terminators to easily tailor the I/O interface to meet your system requirements.

8080A CPU group—accepts interrupts originating from the programmable I/O ports, the communications interface and directly from peripheral devices.

Drivers provided for memory and I/O expansion. Simply plug any of the SBC 80 RAM, EPROM/ROM, I/O or Combination expansion boards into the standard SBC 80 card cage.

1K bytes of high speed, low power static RAM.

The first complete single

The Intel® SBC 80/10 Single Board Computer, with programmable I/O, is designed for the profit conscious OEM in a hurry. The SBC 80/10 is the fastest and lowest cost way of getting your products to market. And when your equipment sales increase to the point where it makes sense to build your own Single Board Computer, we'll make arrangements for you to use our bill of material, fab and assembly drawings, and artwork.

Now it's possible to standardize on one computer board for all your products. Everything you need—CPU, ROM, RAM and I/O is on a single 6.75" x 12" board. And since we've extended the programmable nature of the CPU to the I/O interface you can use the same board even when you make an interface change or completely redesign your product's input/output section. Just initialize the programmable I/O devices with the appropriate program instructions and you have individually defined the direction and data transfer characteristics of the six on-board ports. Programmable I/O makes your products more versatile and cuts parts cost and development time.

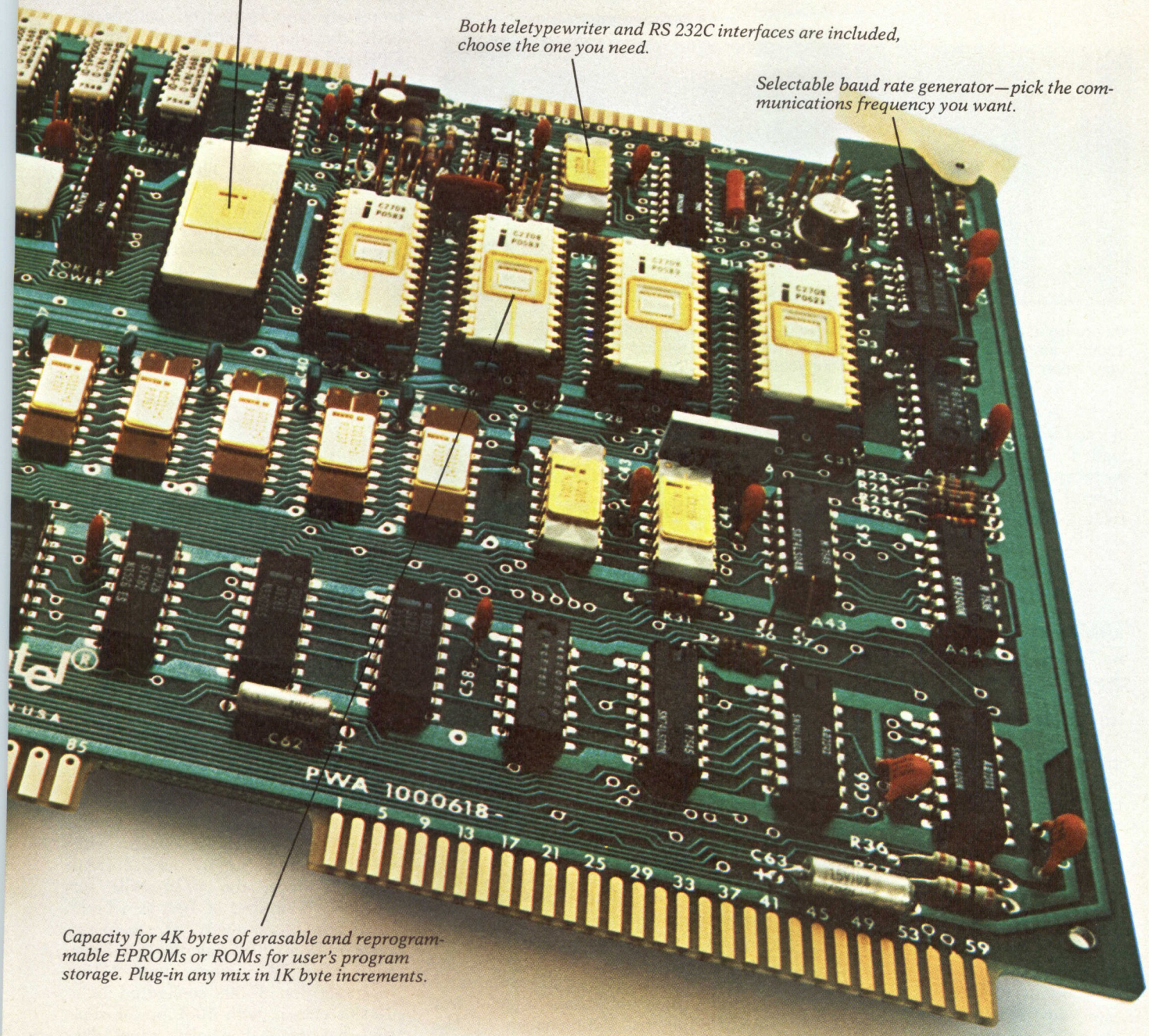
Cut development costs even more with the Intellec

*100 quantity, domestic USA price only. I/O drivers, terminators, EPROMs or ROMs not included.

Programmable serial interface lets you choose virtually any asynchronous or synchronous communications technique. Data format, control character format, parity, and asynchronous serial transmission rates are all under program control.

Both teletypewriter and RS 232C interfaces are included, choose the one you need.

Selectable baud rate generator—pick the communications frequency you want.



Capacity for 4K bytes of erasable and reprogrammable EPROMs or ROMs for user's program storage. Plug-in any mix in 1K byte increments.

board computer for $295.*

MDS™ Microcomputer Development System with optional Diskette Operating System and unique ICE-80 In-Circuit-Emulator. Develop and debug your system software directly on the SBC 80/10 using the symbolic debugging capability of ICE-80.

The 80/10 is supported by macroassemblers, text editor, Intel's PL/M™ compiler, a user's library with over 150 programs, and comprehensive documentation.

Training is available at training centers or scheduled at your plant. For additional technical assistance contact your Intel Field Applications Engineer.

The Intel® SBC 80/10 is available from distributor stock. To order contact: Almac/Stroum, Component Specialties, Components Plus, Cramer, Elmar, Hamilton/Avnet, Industrial Components, Liberty, Pioneer, Sheridan, or L.A. Varah.

For your copy of the SBC 80/10 brochure, use the bingo card or write: Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051.

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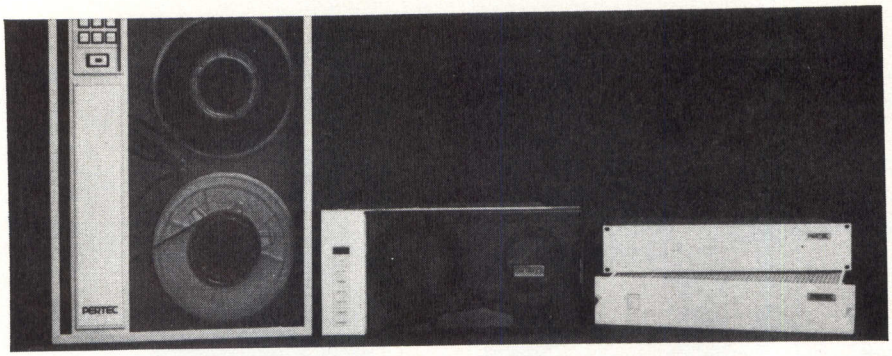
CIRCLE 19 ON INQUIRY CARD



Incorporating a 48-V dc-to-dc converter as well as formatters, Pertec's T7000 and T8000A magnetic tape drives operate with batteries for use in uninterruptible systems such as those in the telecommunications industry

of read/write heads. Heads are ramp loaded with a load force established by a spring integral with the head support arm, eliminating complicated mechanisms and adjustments associated with other approaches. A 0.3-micron filter system assures protection against disc or head contamination.

Circle 144 on Inquiry Card

16M-Byte Add-On Memory Remains Continuously Available to CPU

Advanced techniques used in the in-7168 solid-state memory system permit up to 16M-byte capacity to remain continuously available to the IBM 3168 CPU. Intel Corp's Memory Systems Div, 1302 N Mathilda Ave, Sunnyvale, CA 94086 designed the add-on memory in a standalone frame and incorporated a microprocessor powered maintenance panel and a modular power supply scheme, to provide this continuous availability.

Basic storage element is Intel's 4096-bit n-MOS RAM. Sixty-four of these devices are organized 32K x 8 on a PC memory module; 36 modules make up an incremental storage unit (ISU). Each ISU is divided into two independent halves and each megabyte of storage is spread between two ISUs, allowing the memory to operate in 4-way or serial interleave mode. From 1M to 8M bytes of memory are stored in a single standalone frame which connects through cables in parallel with the CPU memory port. When used with the minimum allowable 1M-byte of IBM memory, the unit stores up to 7M bytes. A second unit can be used to increase total memory to 16M bytes, which is considered the maximum main memory usable by the CPU.

The power distribution system provides raw ac power to individual power supply modules which power the ICUs; the maintenance panel also has its own power supply. This concept allows the system to be powered down in 1M-byte increments, while all other 1M-byte increments remain online to the CPU. This avoids the possibility of an overall system failure due to failure of a centralized ac-dc converter or dc voltage regulator, allows potential power problems to be isolated to a 1M-byte increment, and conserves power in systems with less than full storage capacity.

Containing an 8080 microcomputer system, the maintenance panel not only expedites maintenance of the Intel memory but identifies any failing memory in the 370/168. It provides the operator with error logs for total memory and a power supply display.

Circle 145 on Inquiry Card

Single-Board Processor's Dual Bus Allows Interface to Mini/Micro I/O Devices

A dual I/O bus system in the single-board 5/16 processor bridges the gap between microprocessors and minicomputers, allowing interfacing with both minicomputer peripherals and the low cost I/O devices being supplied for microprocessors. Interdata, Inc, Oceanport, NJ 07757 based the processor's dual bus design on the increased importance of peripheral costs that has resulted from lower CPU and memory costs.

Housed on a single circuit board, the model 5/16 incorporates a full 16-bit processor with 16 general-purpose registers, 114 instructions, line frequency clock input, and built-in self-test. It has 8K bytes of n-MOS dynamic R/W memory (expandable up to 64K bytes) with a 600-ns memory cycle time, and directly addresses up to 64K bytes. Up to 48K bytes of ROM replacement for main memory is available as an option.

The dual I/O bus system has both a standard Interdata multiplexer bus and an industry standard Micro Bus. The multiplexer bus assures compatibility with the company's software and peripherals while the Micro Bus permits interfacing with low cost microprocessor I/O devices. The Micro Bus is compatible with I/O buses of both the Intel 8080 and the Motorola 6800.

Extending the top of the company's 16-bit family, the 8/16, announced in conjunction with the 5/16, is claimed to be faster and less expensive than either DEC's PDP-11/35 or Data General's Nova 3. It includes 16 general-purpose registers, direct memory addressing, and support for up to 64K bytes of 750-ns core memory. Options include hardware multiply/divide, single and double precision floating-point hardware, power fail/auto restart, and bootstrap loader.

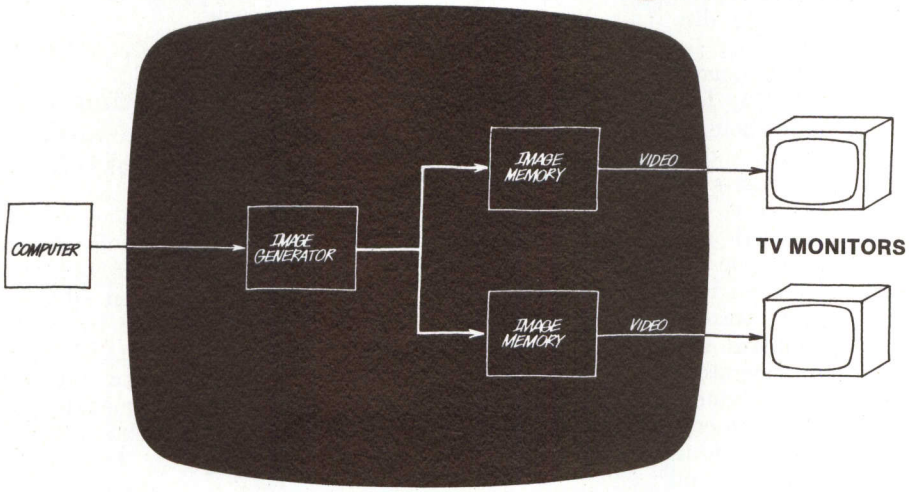
Enclosed in a 5-slot chassis with a 25-A power supply and current loop interface, the 5/16 sells for $1395 in quantities of 100; as a basic processor board with 8K memory, price is $868 (100 quantity). A basic 8/16 with 32K memory costs $4160 in quantities of 50; configured in a 16-slot chassis with 50-A power supply, hexadecimal display panel, 60-Hz clock, power fail/auto restart, bootstrap loader, disc and teletypewriter interfaces, and single and double precision floating-point hardware, the unit sells for $16,761 (quantity 10).

Circle 146 on Inquiry Card

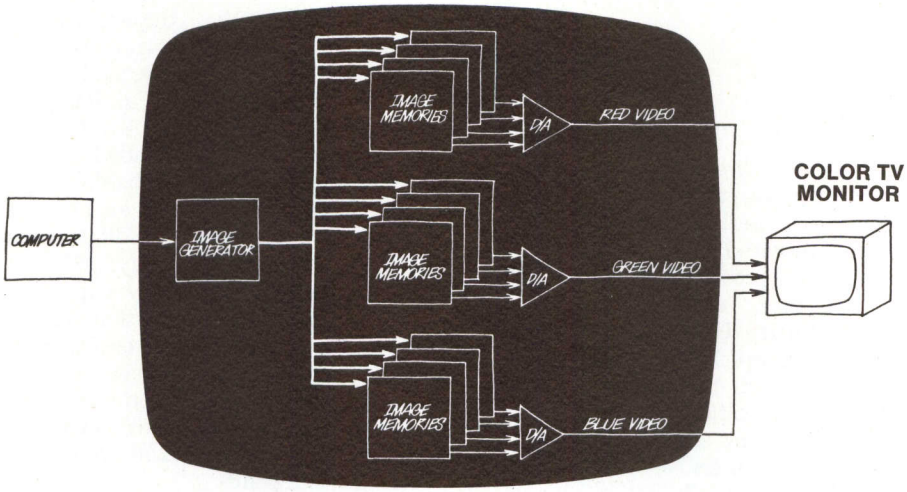
256K-Byte Memory Boards Fabricated from 16K Chips Form 8M-Byte Memory

Large capacity main and disc memories intended for use with its 300 and 400 central processors have been

You've seen display systems like these... but not at these prices!



2 channel B/W: $5,700



12 channel, 16 shades in each of 3 colors: $9,450

How about RGB color with half intensity blink, or high resolution B/W graphics, for only $6,450?

These aren't stripped down either. They're complete operating systems with a standard interface, and quantity discounts are available.

Those are just a few examples of how we've changed the graphic television display market. All of our systems work with standard TV monitors, and have these standard features:

- 3.0 μsec access to any point on the screen
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- Up or down scroll
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CIRCLE 20 ON INQUIRY CARD

introduced by Prime Computer, Inc, 145 Pennsylvania Ave, Framingham, MA 01701. Providing four times greater capacity on a single 16 x 18" board than its predecessor using 4K chips, the 256K-byte MOS memory board is fabricated from Intel's 16K memory chips. The 300M-byte disc unit, a complete subsystem that includes disc drive, 12-platter removable disc pack, and controller, features automatic error corrections.

For use primarily with the model 400 processor, which can address up to 8M bytes of main memory, the 256K boards can be packaged in a memory extender unit to provide 8M bytes in a 27-slot chassis. Access time is 400 ns. Automatic error correcting code (ECC) is a standard feature. The ECC system appends a special 5-bit code to all data stored in memory. This code is used in conjunction with error checking firmware to automatically detect and correct all single-bit errors without interrupting CPU activity. Most multiple-bit errors can be detected as well. To further enhance memory integrity, the operating system is capable of testing each page of memory and automatically paging around detected malfunctions.

Augmenting main memory capacities on model 300 and 400 processors, the 300M-byte disc subsystem can be expanded by adding up to three more disc drives per controller for maximum 1.2G-byte capacity. Reliable operation and error-free data transfers are provided by system integrity features that include automatic header label checking, cyclic checkword calculation, and an automatic error correction feature. Implemented in a combination of hardware and system software, the error correction feature automatically corrects up to 11 bits in one burst error.

Circle 147 on Inquiry Card

System Architecture Divides Workload Within CPU Complex

ECL logic, multilayer printed circuit boards, semiconductor memory, and independent instruction and peripheral processors are incorporated in the 90/80 virtual system to provide high performance, reliability, and efficiency. Introduced by Sperry Univac, a div of Sperry Rand Corp, PO Box 500, Blue Bell, PA 19422, the virtual system allows easy transition from 90/60 and 90/70 systems as well as from series 70 computers. Conversion aids for the IBM 370/145 are offered to provide an alternative to those planning to upgrade to the 370/158.

Designed such that instruction processor and peripheral processor have separate processing capabilities, the system architecture allows work to be distributed within the CPU complex. Functions proceed in each unit without interference from or with that of the other processor.

Processing and control portion of the system, the instruction processor contains sequencing and processing controls for interrupt action timing facilities, initial program loading, and instruction execution. Its 32 32-bit general-purpose registers are arranged in two sets: one reserved for executive or privileged mode, the other for use by user programs. This design reduces the interrupt processing time overhead required when only a single set of general registers is used.

The microprogrammed peripheral processor provides I/O processing facilities. Permitting eight I/O channels, with a minimum of one byte multiplexer (one optional) and one block multiplexer (six optional), the peripheral processor transfers data to main storage at 8M bytes/s; byte multiplexer transfer rate is 183K bytes/s. Both processors can initiate requests for main storage independent of one another.

Main memory is made up of 4K n-MOS storage devices. Capacity ranges from 524K to 4129K in 524K increments. Providing 280-ns read access time with a cycle time of 450 ns/8 bytes, the memory uses an error correction code technique to correct single bit loss and detect double bit loss, ensuring data reliability. The technique reduces the incidence of "stops" due to main storage failures and allows most failures to be repaired during nondisruptive maintenance periods.

Other reliability features include an online fault analysis technique provided via microprograms. Multiple level hardware instruction re-try is aided by software fail-safe techniques, error logging, and dynamic reconfiguration around failed devices.

The system handles a full complement of peripheral equipment including disc subsystems, magnetic tape units, card reader, and printers. A multichannel communication controller integrates hardware and software functions to optimize communication capabilities.

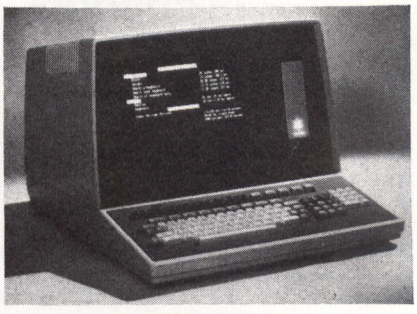
Circle 148 on Inquiry Card

Video Display Terminals Designed for Cost/Benefit Ratio

A low cost remote video display and a fully featured user programmable unit with detachable keyboard have been added to the B series terminal line by Beehive Medical Electronics, Inc, 870 W 2600 South, Salt Lake City, UT 84125. Both units are designed to provide many features yet retain economy.

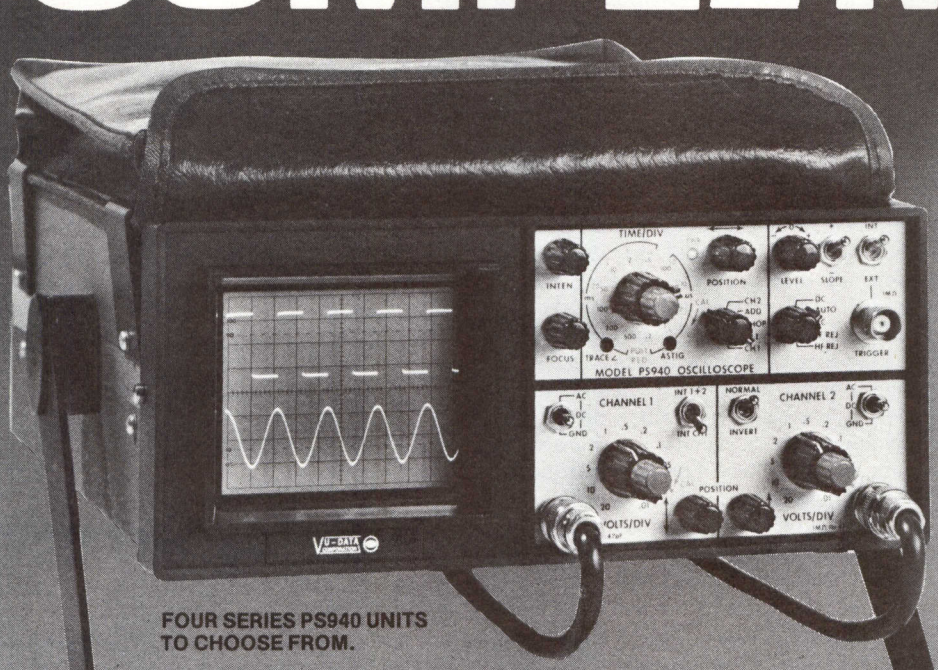
The user-programmable B500 features an expandable program memory, down-load capability from the CPU, data transmission at rates to 19,200 bits/s, and full- or half-duplex online operation. This unit incorporates 4K RAM display memory, and provides program storage in 4K p/ROM or 8K ROM; up to 48K of RAM is available to permit expanded editing capabilities. The detachable typewriter-style keyboard has an 11-key numeric pad.

Edit functions, RS-232-C compatibility, 25-line x 80-character display capacity, line and block transmission, addressable cursor, upper and lower case characters, scrolling, and 4-level video are standard features. Optionally available are flexible disc unit, expanded software capability, 256 programmable characters, and



User-programmable B500 video display terminals from Beehive Medical Electronics incorporate 4K R/W display memory, and provide p/ROM or ROM program storage. Detachable typewriter-style keyboard has 11-key numeric pad in addition to function keys

TAKE IT AS A COMPLEMENT



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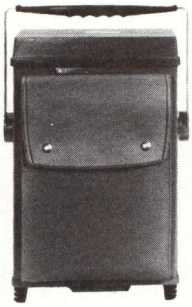

Typical Portable
Wt. 25 lbs.
Size 1300 in.³
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"Complement" means to add to or enhance. So, complement your "big scope" inventory with a Series PS940 Mini-scope the next time your field service requirements call for small size and light weight. These rugged units offer the best performance for the price you pay. All the basic features required for servicing today's sophisticated electronics are included—things like dual trace, delay line, selectable DC coupled triggering, algebraic addition and substraction, composite trigger, battery operation and many others. With a 20 MHz bandwidth, these scopes are plenty to trouble-shoot to the sub-assembly level. And they'll trigger as well as, or better, than any 100 MHz scopes around.

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edit features that include word search, word delete, sentence delete, and block move.

Accommodating strict budget limitations by providing low cost, variety of options, and diverse features, the B100 is a self-contained, operator/computer-accessible terminal with 12″ digital type monitor formatted to display 12 or 24 lines of 80 characters each. Transmission rates are switch-selectable from 110 to 19,200 bits/s. Erase mode and hardcopy capability with printer interface are standard features; options allow formatting, blink, editing, and function keys.

List price for the B500 is $2695; the B100 sells for $1495. OEM discounts are available.

Circle 149 on Inquiry Card

Character Clip/Cartridge Printer Offers Flexibility, Low Cost

Character clip/cartridge technology is used in the model 5560 printer to enhance character registration as well as offer flexibility and lower costs. Data 100 Corp, 6110 Blue Circle Dr, Minneapolis, MN 55435 developed the concept to provide high quality output by allowing the operator to replace defective characters.

Producing 600 lines/min., the standard unit is furnished with a 132-col print line and 64-character ASCII font. Printing is performed in a horizontal position to permit smooth paper movement and provide extremely even lines.

Character set is contained on 96 individually replaceable clips to provide flexibility and versatility. Holding four characters, each clip is a metal plug that mounts on two rubber belts, riding between them. 96 clips mounted on the belts comprise the character belt which fits into the cartridge. A steel guide rail at the front of the cartridge, and two guides that curve in front of the clips maintain positioning during movement. The entire cartridge is easily removed to change or replace the font; individual clips can be operator replaced to fix defective characters, guaranteeing high quality print.

Housed in one leg of the cantilevered unit, the electronics package is configured around a processor that provides printer control, emulation capability, and printer diagnosis routines. The bipolar LSI processor has a 130-ns cycle time, and is partitioned into CPU, which handles arithmetic tasks; interface, which provides path to customer equipment and data storage for the processor; and an auxiliary section which handles all high voltage functions (eg, motor on/off). p/ROM is used to store the program that runs the printer; RAM holds data necessary for housekeeping duties and computer input.

Hammer driver boards are located underneath the printing head. Hammers (one per column) are fired dynamically in time as characters pass the hammer. The hammer bank can compensate for any feed variation dynamically within a print line, character to character.

Horizontal print surface both enhances smooth paper movement and allows easy operator access for paper loading and forms setup functions. Paper movement is handled by a servomotor driving four large tractors. There is a paper puller at the rear to get paper out of the machine. Both velocity feedback and an optical encoder are used to keep track of line spacing.

Circle 150 on Inquiry Card

512K-Byte Add-On Memory Allows Reconfiguration, Use of Multiple Systems

The ECOM® 70 core memory system, from Standard Memories, 4120 Birch St, Suite 105, Newport Beach, CA 92660, provides up to 512K bytes of add-on or replacement memory for PDP-11/70® computers. Electrically connected to the computer's memory bus via four controlled-impedance flat cables, the unit incorporates reconfiguration controls which allow DEC memory to be totally disconnected; a memory bus continuity feature permits multiple systems to be used for large storage applications.

Memory modules are 3D, 3-wire coincident current core memories using planar large card construction. MM-122 provides 16K x 18 bits or 32K bytes; MM-124, 32K x 18 bits or 64K bytes. The 12¼″ high, rackmount chassis assembly houses up to 16 memory modules and one control card. Capacity ranges from 64K to 512K bytes in 64K increments (MM-122), and from 128K to 1024K in 128K increments with MM-124 modules. Maximum system execution times are: 800-ns read/write cycle, 100-ns write access, and 425-ns read access.

Electrical interface between the CPU memory bus and memory modules is accomplished with four controlled-impedance flat cables. Eight flat cable connectors on the control card permit the user to either terminate the memory bus at the memory system chassis or provide memory bus continuity to other memory units, permitting the use of multiple memory systems, since the PDP-11/70 is capable of addressing up to 4M bytes of memory.

A remote programming box fitting directly under the enclosure chassis contains on/offline switch, reconfiguration controls, chassis cooling fans, and ac power controls which allow the memory system to automatically power up/down with the computer system. On/offline switch permits the memory system to be electrically removed from the memory bus. Reconfiguration controls allow the user to easily move the starting address and ending address of the memory system to any location on the bus.

Circle 151 on Inquiry Card

Simple Modular Makeup Enhances Reliability, Service of Printer

Four major modular assemblies make up the 9232 matrix printer. Achieved through incorporating a simple mechanical design and using integrated electronic circuitry to control and move printhead and tractor mechanisms, the printer design increases reliability, and provides processing capability.

Heart of the printer, developed and manufactured by Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284, is a processor which controls both the flow of data and the printer mechanism. An additional function is running built-in diagnostics which check and demonstrate all control functions and generate a complete character set. The processor also permits bidirectional printing for high throughput, high speed spacing, and line feed slewing.

Maintenance is eased by both the unit's mechanical simplicity and its modularity. The unit disassembles easily into subassemblies: paper tractor, printhead, carriage, and electronics assemblies are easily replaced. No special tools or align-

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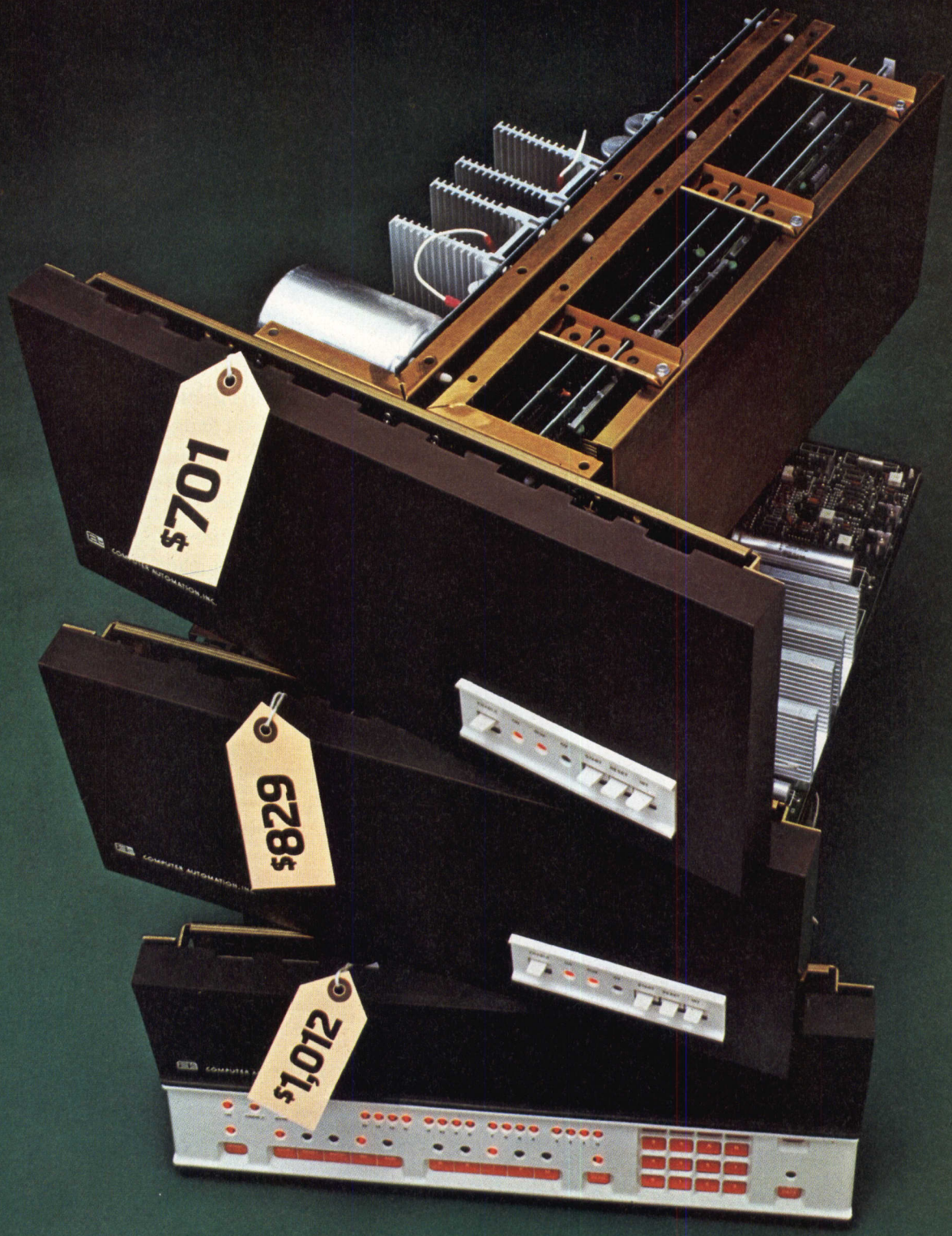
What our bottom-of-the-line



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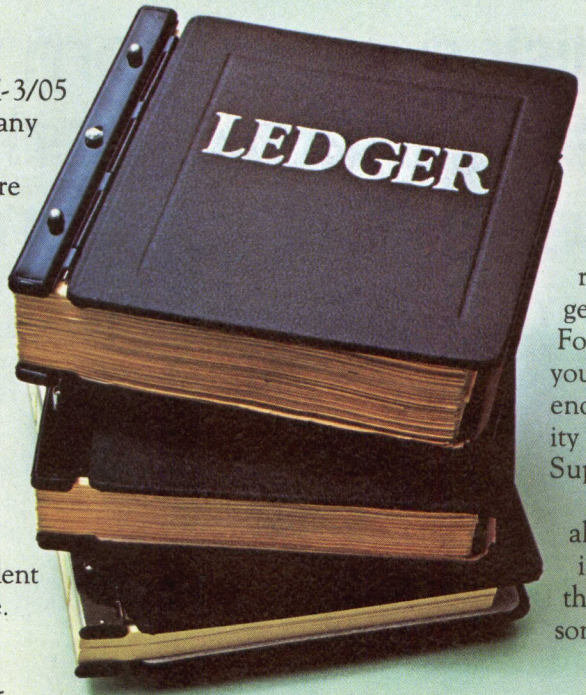
ComputerAutomation's low-cost line of 16-bit, full-scale, fully compatible computers.

can do for your bottom line.



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Ready? $701 total packaged price. And that's complete with 256 words of MOS RAM, and a CPU that offers a really powerful instruction set, Power Fail Restart, Real-Time Clock and Autoload capability.

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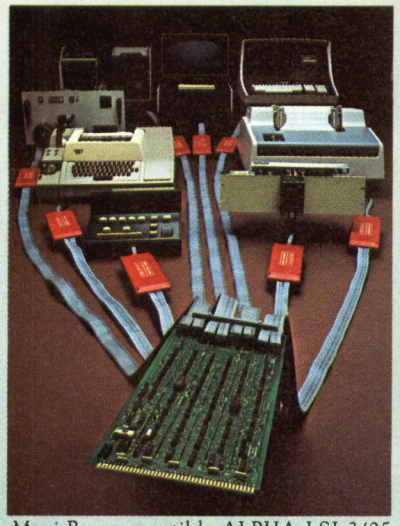
You also get the capability to configure your computer pretty well the way you want it. A choice of packaging, of course, that includes either the Operator's or the Programmer's Console, power supplies and so on.

A choice of two standard I/O options.

And a choice of optional memory configurations that include RAM/ROM, RAM/EPROM and RAM-only in sizes from 256 words all the way up to 32K words. Totally addressable.



Maxi-Bus compatible ALPHA LSI-3/05 achieves unprecedented cost-effectiveness with ComputerAutomation's new Distributed I/O System.

Family connections save you still more money.

So far, what we've been talking about could easily add another five or six figures to the bottom line of your ledger.

But there's more. Really big savings on off-the-shelf software, peripheral controllers and I/O interfaces.

The reason is that the ALPHA LSI-3/05 millicomputer is a full-fledged member of ComputerAutomation's LSI Family... Maxi-Bus compatibility and the whole works. So, every piece of Family hardware we've ever developed will work like it was made for the ALPHA LSI-3/05. Including ComputerAutomation's exclusive new Distributed I/O System... just like you see it in the picture.

With this versatile interface system, you can interface virtually any kind or combination of peripherals. Parallel or serial. Just by plugging them in.

Your cost? Probably less than $200 per interface.

The pros know.

Computer-wise OEM's will tell you that product requirements sooner or later get ahead of the hardware. For instance, the computer you buy today may not have enough I/O or memory capacity for tomorrow's Mark II Super Widget.

Then you'll have to scrap all your software and your interface designs, because they're not about to work on some other machine.

You lose.

Of course, with our LSI Family of compatible computers you don't.

You can switch to a different CPU or a different memory anytime. Faster, slower, bigger, smaller. The electrical interface will still be the same; the original programming will still work.

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From the people who brought you the NAKED MINI.®

And the NAKED™ MILLI. And the Distributed I/O System. And the PICOPROCESSOR.

And now the ALPHA LSI-3/05 millicomputer.

One cost breakthrough after another. Breakthroughs that didn't just happen... a lot of profits got plowed back into R&D.

But then, that's the price of leadership.

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NAKED MINI Division

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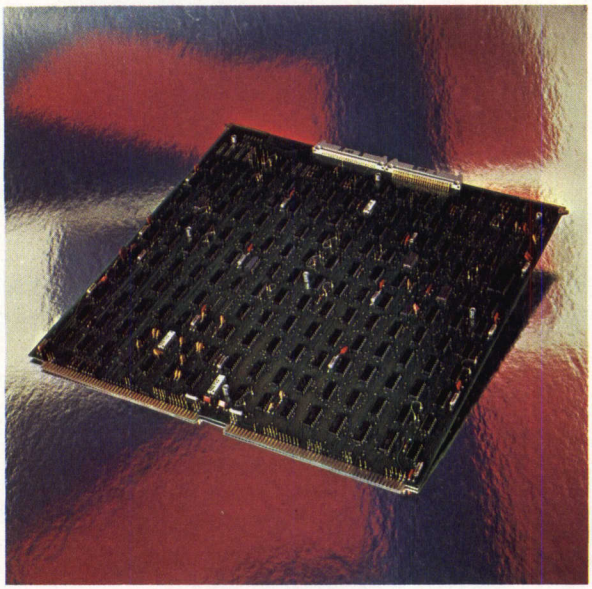
Please have a salesman call—circle 24 on Inquiry Card.

All prices shown are for lots of 100 (U.S.A. only).

Don't be decked by all of the general data about only buying your disk system from your mainframe manufacturer! DATUM's 4091 Series Disk Systems will do the job for less. We guarantee it!

Take, for example, the DATUM embedded disk controller for the Data General Nova® 2, Nova® 3, Eclipse® minicomputers: • Embedded in NOVA® chassis • Looks like Data General 4234 Controller • Detached header mode included • Completely media-compatible • Runs under RDOS-4 or RDOS-5 • Accesses up to four 10-Megabyte drives such as Diablo 44 or the Pertec 3442 • Will perform overlap seeks • No special software required • Complete data error checking

All DATUM controllers and systems are developed using the minicomputer and software with which they are to function. This assures that they are compatible with (and transparent to) the system in which they will be used. Your processor will think that it is dealing with a member of its own family. You will thus have service compatibility at all levels. DATUM diagnostics, supplied with every installation, will check out machine performance.



Once your DATUM disk controller is up and running, once we have trained your people, your operating problems will disappear. And remember, DATUM warrants and services all of the equipment that it supplies.

Only DATUM has designed, built and installed over 6500 controllers and systems for use with most minicomputers and so many different peripheral devices.

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☐ I have an urgent need for a disk system and would appreciate your circumventing normal response time and phoning me now.

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Street Address _____ City, State, Zip _____

Telephone No. _____ Position _____

Computer and Model Number _____

ment equipment are required. Where synchronization with other printer components is necessary, light emitting diodes are provided to indicate when the assemblies are correctly aligned.

Since the equipment is intended for use by office personnel, controls are simple to use. By moving the ribbon along with the print mechanism, the ribbon path is kept short, facilitating ribbon changes. Each tractor assembly features its own line spacing, form feed, and vertical alignment controls. Forms length is controlled by a removable plastic chain. Each link in the chain represents ¼" of paper; small plastic flags inserted between links set the forms length from 1 to 24".

Functionally, the machine prints 132-col lines at 80 char/s; and provides from 25- to 425-line/min. throughput. Line spacing is 6 to 8 lines/in., individually selectable on each tractor. Character set is the 96-char ASCII upper and lower case font. Underscore, super, and subscripts are possible.

Circle 152 on Inquiry Card

32-Bit Computer Offers 1M-Byte Memory, Pipelined Instruction Execution

A low price, 32-bit computer, the IV/35 offers 1M-byte memory, double the capacity of its predecessors, to permit increased operating system services, larger user tasks, and extended global libraries. In addition, the unit has 32 direct memory processor I/O channels, eight virtual memory context environments, and computation capability for standalone measurement, control, and communications real-time tasks. It doubles virtual memory addressing, multiprogramming environments by implementing eight 128-byte memory mapping files.

Introduced by Modular Computer Systems, Inc, 1650 W McNab Rd, Fort Lauderdale, FL 33309, the processor is intended for use as a host or intermediate element in distributed communication network configurations. A communications processor version adapts to byte-string processing applications.

The IV/35 CPU performs pipeline instruction execution operations using parallel data buses and adders in combination with 2- and 4-way memory operand interleaving and operation lookahead access. Instruction execution times are variable due to the effects of pipeline execution. Many register-to-register instructions can be executed in a minimum of 320 ns, if the instruction is available in the lookahead pipeline when execution of the preceding instruction is completed.

Increased efficiency in the multiprogramming operating system results from implementation of eight 128-byte memory mapping files. These eight virtual program environments are controlled by a memory management system which provides high speed hardware for all memory allocation/deallocation and memory context switching functions.

Increasing the number of direct memory processor channels to 32 allows high speed peripheral block data transfers into the multiported memory system. The four simultaneous memory access paths provide simultaneous CPU and I/O access capability. The 4-port memory interface enables up to four transfers to be made during the same cycle time.

A basic IV/35, priced at $42,500, includes 32-bit parallel bus and arithmetic unit, 128K-byte 1-μs core memory, memory expansion capability to 1024K bytes, 4-port memory interface, control console, memory parity, and cabinet.

Circle 153 on Inquiry Card

Modular Control System Simplifies Newspaper Production Processes

Embodying the copy management concept for automated newspaper copy control and production, model 6000 is a computer-based system that simplifies copy entry and editing, filing, typesetting, including hyphenation and justification, and copy classification. Developed by Amcomp, Inc (formerly Data Disc), 686 W Maude Ave, Sunnyvale, CA 94086, the system features fully redundant architecture for reliability, as well as modular hardware and software.

The system uses DEC PDP-11 CPUs, Amcomp 6800 clustered terminal controllers, UNIX operating system, and special programming techniques to support systems having small single processors or large multiple processor systems having over 100 terminals. Configurations may contain moving head and head per track discs, magnetic tape units, printers, and visual display terminals.

Entered directly from the wire service, from terminal keyboard, or OCR unit, copy can be edited from a visual display terminal, and then maintained on the system in three versions: original input, latest filed version, and a working copy for actual editing. Directory mode is highly interactive; directories can be maintained by any number of user-selected criteria and their structure can be changed online.

After selecting a story from the directory, editing is accomplished via the display's keyboard. Capabilities include block definition and manipulation, string replacement, and character editing.

Composition facilities accommodate both straight and display matter. Nested format capability permits nested usage as well as online display, edit, and update. Hyphenation and justification are interactive.

Circle 154 on Inquiry Card

Hand-Held Calculator Performs Functions on Fractional Entries

The AL-8, an 8-digit calculator designed to calculate fractions, has been introduced by Casio Inc's Computer Products Div, 15 Gardner Rd, Fairfield, NJ 07006. In addition to four basic arithmetic functions, the unit provides full 4-key independent memory, which allows subtraction, addition, recall, and clearing of memory, and a percent key for calculating markups and discounts.

A small slide switch under the unit's display allows results to be cut off or rounded off to two decimal places. A second more sophisticated switch selects six different modes featuring various symbols, each allowing the user to perform a different function. These functions include square root, grand total, remainder (allows user to divide one number by another, and display the remainder), arithmetic on numbers expressed in fractions, measuring time intervals expressed in hours, minutes, and seconds, and standard deviation. The AL-8 operates on two penlight batteries or on ac with an optional adapter; price is $24.95.

Circle 155 on Inquiry Card □

DEVELOPMENTS

16- x 16-Bit Multipliers Meet Military/Commercial High Speed Applications

Ability to multiply two 16-bit words to generate a 32-bit word makes the MPY-16 family applicable for both military and commercial high speed processing. A, B, and C versions can perform a complete double-precision 16- x 16-bit parallel multiplication in 300 ns or less. The military grade, high reliability units will also be made available in radiation hard configurations.

Developed by TRW Inc's Defense and Space Systems Group, Redondo Beach, Calif, the circuits incorporate more than 18,000 components on a single ¼-in. sq silicon chip that is housed in a 64-lead flat package. Multiplication is carried out by an array of adder cells using the successive-add algorithm. Each of 60 devices in a cell contains about 3 mils² of chip area for a total of approximately 200 mils² for a cell. Only a single 5-V power supply is used.

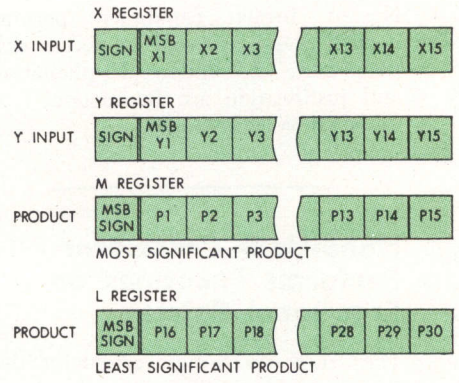
Dual-railed emitter follower logic (EFL) used in the full adder cells results in both the high speed and low power consumption (1.4 mW/gate). Total power consumption is 5.1 W. Non-inverting AND-OR gates eliminate delay times in logics requiring signal inversion. The major multiplier array logic achieves speed-power performance of <3 pJ.

Inputs and outputs are fully TTL compatible, and outputs have 3-state control. A data bus under program control provides several time-shared input and output options. I/O signal leads are reduced to as few as 25. The 3-port chip offers separate inputs and outputs for single precision operation or combined for double.

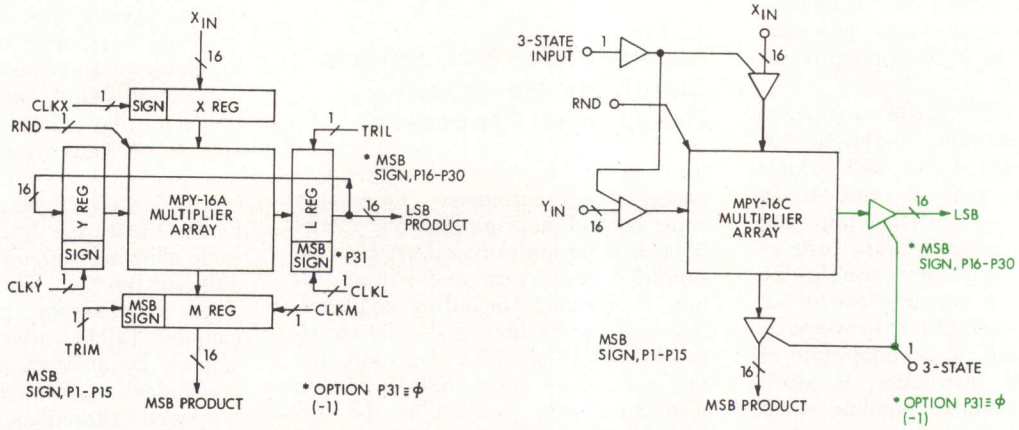
Two control signals load the input latches and begin multiplication. The 32-bit product is read out in two steps by the control signal directly to the 16-wire data bus.

Of the three configurations, the most complex—MPY-16A—has both input and output registers under separate clock control. These registers are D-type flip-flops using a single phase TTL clock input. A double precision product is available. Configurations B and C operate with less power and do not incorporate registers; both operate in a continuous asynchronous multiply mode. B has single precision most-significant product (MSP) available; C has both MSP and LSP available. Three-state control on the outputs is available on all three configurations. Three-state control on inputs is available on B and C. (Three-state input control reduces the input load current for bus operation, inhibits the inputs, and zero fills the multiplier.)

The multipliers are expected to be offered for sale by the end of 1976. Probable price will be about $250 in small quantities.



Input and output parallel format of MPY-16, a 16- x 16-bit, 2's complement parallel multiplier. Sign and 15 bits form the most significant product



Variations in configuration complexity of MPY-16 family. B version is same as C except that area shown in color is not included

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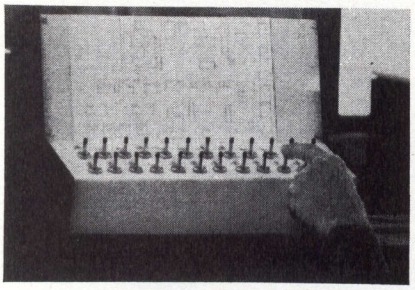
Manual Control Device Cuts Computer System Energy Consumption

Power control interface for computer systems such as the IBM/360 and 370 utilizes the central processing unit (CPU) as the source and ultimate receiver of power sequence control signals. Under standard procedures, the power-on sequence to satellite devices is automatic. A single switch turns on all interconnected machines and places the entire system in operational mode. When system power is on, I/O devices such as discs, tapes, and control units are on. These peripherals consume energy whether or not they are needed for a given computer operation.

However, because all power control signals do emanate from the CPU, designers attempting to remedy this energy waste situation need work with only a single source. Disconnecting power control cables from the CPU and reconnecting them to an external switching device can be accomplished without altering either the CPU or the I/O devices or affecting the emergency power-off controls.

Personnel at International Business Machine Corp's General Products Div in San Jose, Calif did just that. A proposal from the Product Assurance Laboratory for a remote I/O power control station was implemented on a System/370 at the Product Test Laboratory. The result is a reduction in the electrical energy consumed by the system. Only the peripherals required for the project being run at any given time need now be on and using power. All others can be turned off.



Remote I/O power control station. Operator can "power down" unneeded machines of a computer installation by locating desired machine on diagram (above control box), noting its identifying number, and flipping toggle switch correspohding to that number

Introduction of the remote I/O power control station appropriately reroutes the peripherals' power supply cables from the CPU and, in effect, converts the normally automatic power-on process to a manual procedure. The operator can switch power selectively.

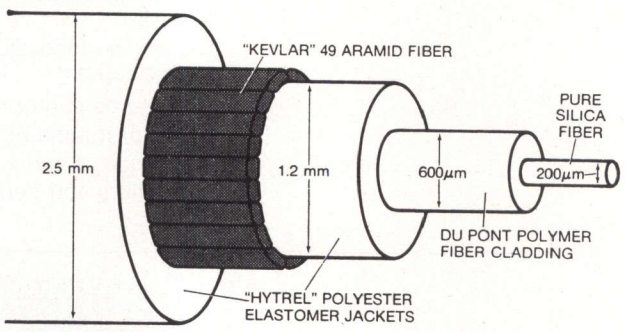
In the IBM unit (see photo), power control cables are connected to switches on a small control box. These switches energize or de-energize the various machines individually, based on the operator's decision as to which are needed at any given time.

Installation of the control station is quite simple: the power sequence control cable is disconnected at the satellite device, a special tee connector is inserted, and the sequence control cable is run to the centrally located control station.

Operation is just as simple. The system operator locates the desired satellite device on the locator map above the switches on the control station, correlates the device location number with the control station switch number, and momentarily operates the appropriate toggle switch. The associated lamp then lights, indicating that power-on has begun. When the operator no longer requires the satellite device, he momentarily operates the same toggle switch, dropping power to the device. If the operator tries to use a device that is not powered-on, Operating System/360 or 370 alerts him.

The control station developed for the San Jose Test Laboratory computer installation involves 16 satellite devices but can be expanded to control 24. Only 14 parts are required.

Fiber Optics Cable Has High Resistance To Mechanical Stresses



DuPont PFX-S fiber optics cable. Minimum bending radius of 3 mm is only slightly greater than the cable's 2.5-mm diameter

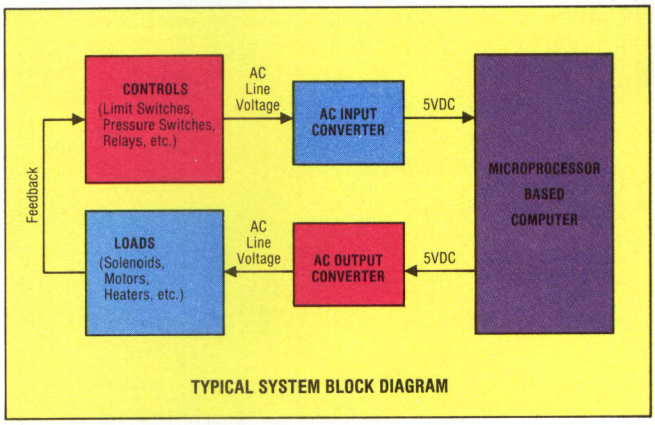
A plastic-clad, pure silica core cable for data transmission, PFX-S features attenuation of 80 dB/km at a wavelength of 800 nm. Cable-to-cable splices and connections to LEDs can be made with little transmission loss as a result of the large numerical aperture of the single fiber cable (calculated at 0.4). At 700 nm, attenuation is 60 dB/km.

According to tests conducted during test marketing, the fiber optics materials resist radiation better than glass bundles, and are resistant to vibration, microbends, impact, water immersion, and temperature cycling from −80 to 150°C. Applications are expected to be in computer interconnections, medium-run-length transmission where fiber ruggedness is important, and military systems.

Developer of the cable, E. I. duPont de Nemours & Co, Wilmington, Del, claims the extremely tough fiber optics material "will resist mechanical stresses better than other glass or silica fiber optics currently available." It can be bent around a 3-mm diameter without breaking.

Other specifications of the material include: exit numerical aperture 0.27 (−10 dB), core dia 200 μm (0.008″), clad fiber dia 600 μm (0.024″), inner jacket dia 1.25 mm (0.049″), outer jacket dia 2.5 mm (0.098″), min bending radius 3.0 mm (0.118″), and tensile strength 30 kg (66 lb). □

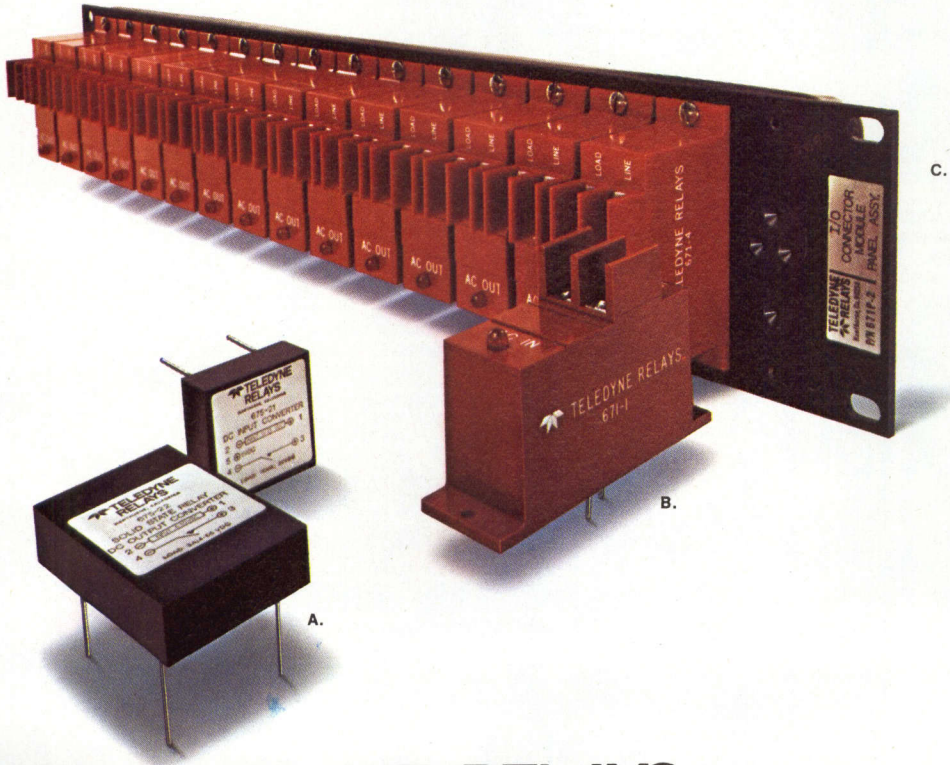
Microprocessors take control with Teledyne I/O converters



TYPICAL SYSTEM BLOCK DIAGRAM

Modular packaging of input/output interface circuitry. That's what Teledyne I/O Converter Modules provide microprocessor based industrial controls for maximum I/O flexibility and expandibility. This single circuit modular concept features all-solid-state circuitry, 1500V optical isolation, and high noise immunity. Our 671 Series modules plug directly into a low cost custom-designed mounting panel, which physically isolates service wiring from logic connections. For pc boards, we offer the same circuitry in our 675 Series low profile package. Both series include ac and dc input/output converters.

So for the best in I/O interface circuitry for microprocessor based industrial controls, contact the people who know the "ins and outs" of this business — Teledyne Relays.



A. B. C.

A. 675 Series — Low profile I/O converter modules for pc board mounting

B. 671 Series — Panel mounted I/O converter modules (with integral LED status indicators)

C. 671P Series — Custom-designed mounting panel

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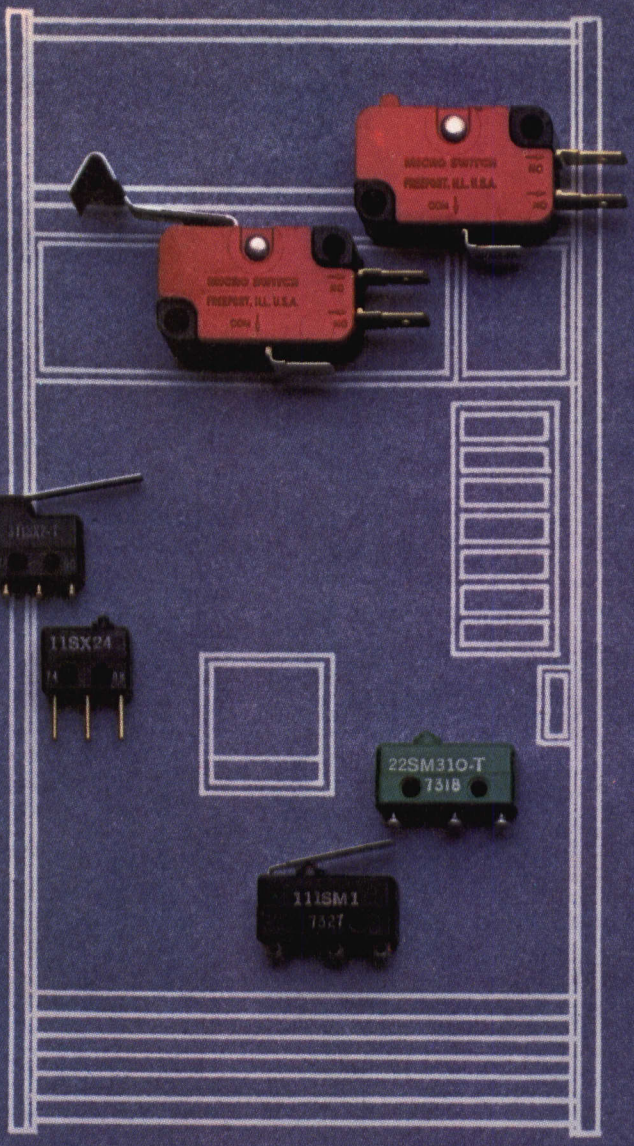
3155 West El Segundo Boulevard, Hawthorne, California 90250
Telephone (213) 973-4545

CIRCLE 27 ON INQUIRY CARD

Some of these components will probably



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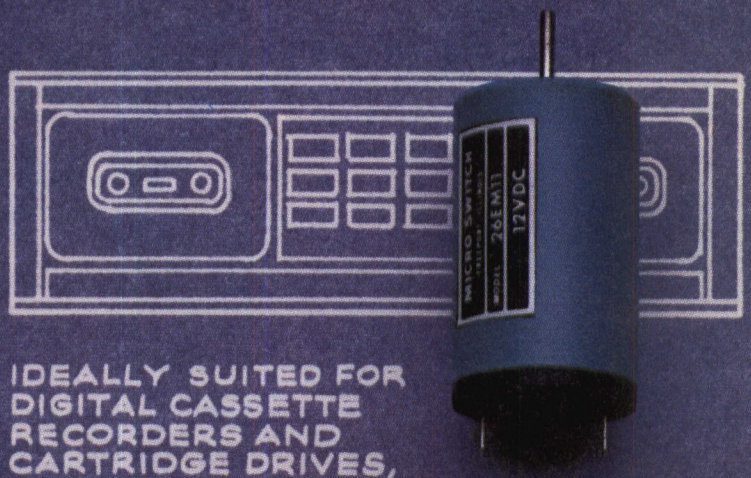

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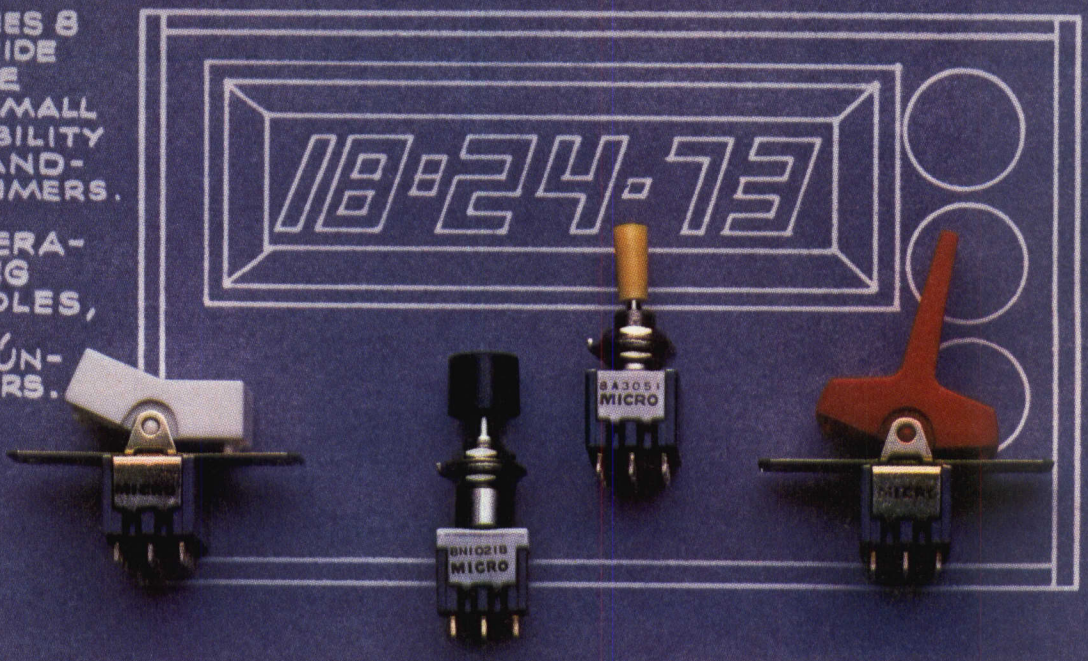
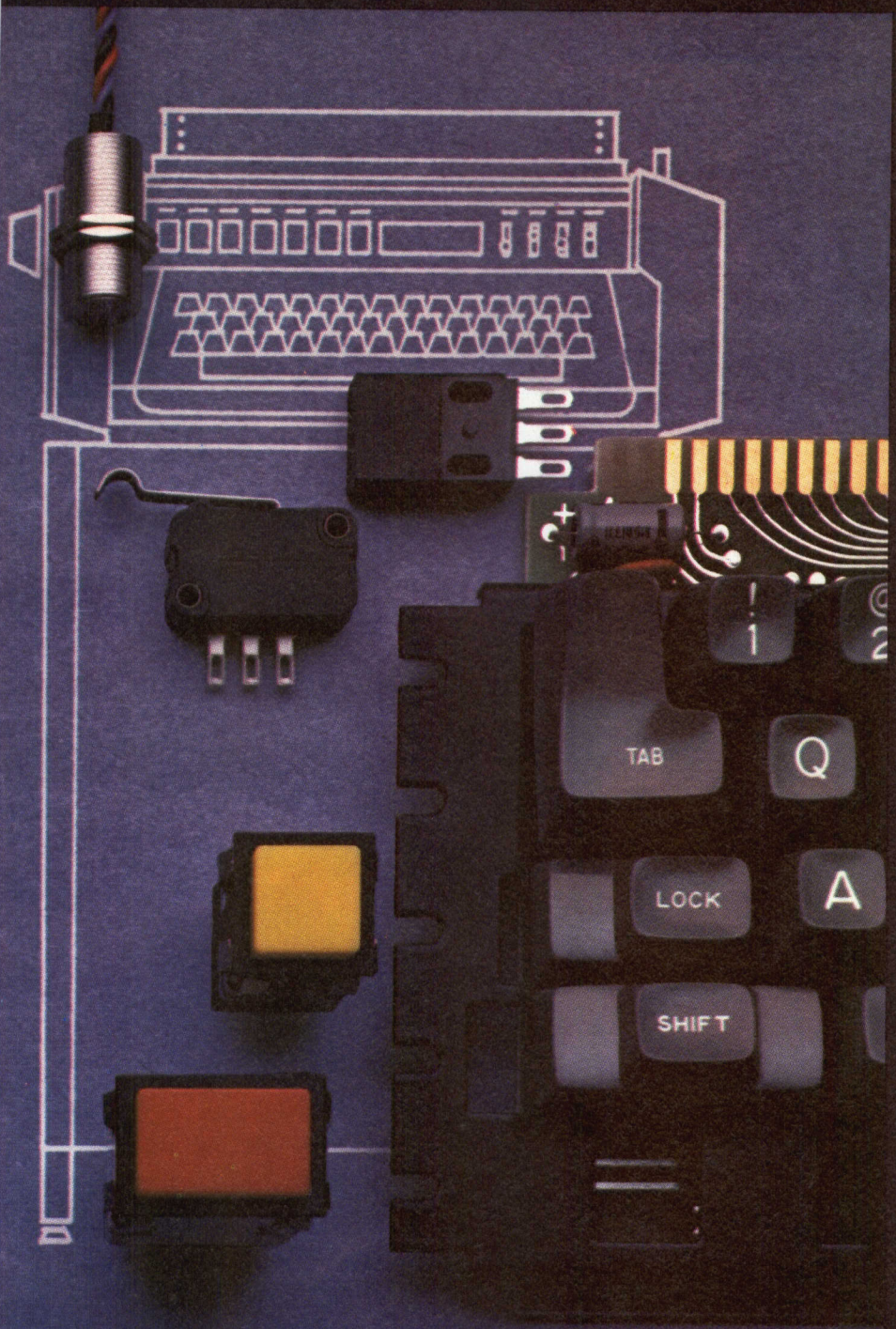


never wear out. The others will just come close.



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The solid state keyboard, AML lighted pushbuttons and solid state position sensors you see here will probably never wear out. Because they're all solid state.

Each is based on a Hall effect integrated circuit. A circuit that's been tested through billions of operations without failing. Even once. And proven by performance in a variety of applications. The other components you see here come close. Simply because of the way they're designed and put together.

Like the long-life versions of our snap-action V3, SM and SX precision switches. Available in a wide variety of sizes, electrical capabilities and ratings, terminals, actuators, contact forms and operating characteristics—they've been tested to a mechanical life of over 10,000,000 operations.

Or the Series 8 miniature manual switches. Designed with epoxy-sealed terminals on most versions for extra reliability. And offered with virtually any operator you might need. Plus terminals that include solder, quick-connect, printed circuit or wire-wrap.

The same standards of quality and product flexibility go into the 26EM DC motor. It's a miniature motor designed with low inertia operational characteristics. And just one of a line that ranges up to the 500VM, a motor capable of accelerating to 4000 RPM and stopping over 1000 times per second.

If you'd like more information on any of these components, contact your nearest MICRO SWITCH Branch Office or Authorized Distributor.

And find out how you can get a component that goes on forever. Or at least comes very, very close.

MICRO SWITCH

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And they'll be pin compatible with the industry standard 22-pin dynamic part.

The μPD410 series of 4K static RAMS.

For people into terminals, add-on memories, mainframes, and minis, it's quite a coming attraction.

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DIGITAL CONTROL AND AUTOMATION SYSTEMS

Microcomputers Replace Gas Station Attendants

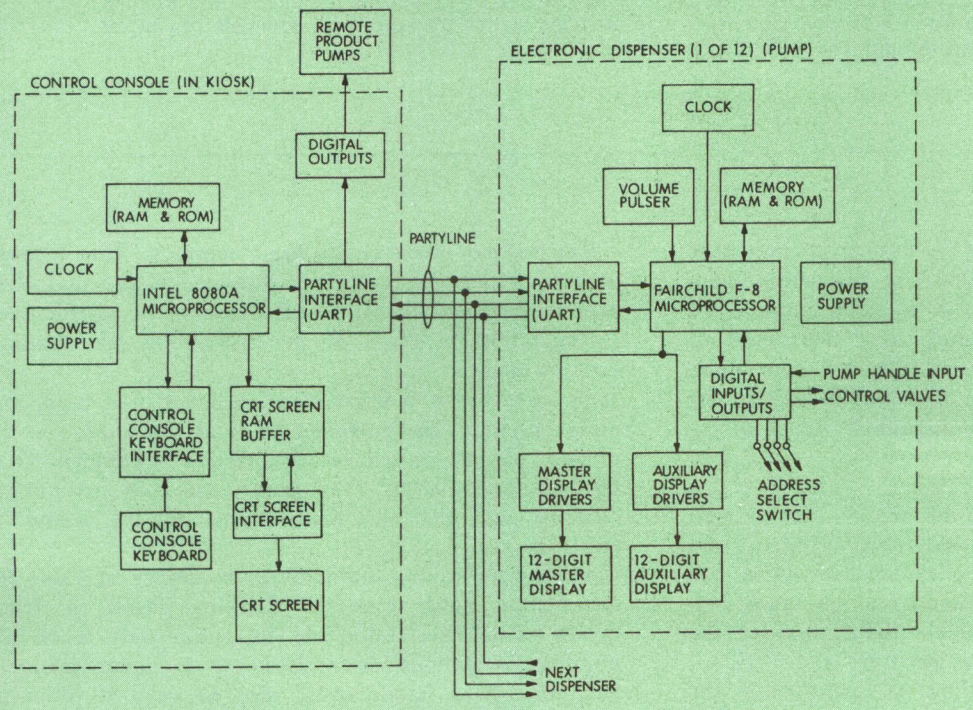
Remember the man to whom you used to trust your car? Remember how he used to offer to check your oil when you bought gas? Remember even farther back to when he would clean your windshield while your tank was being filled?

If the present trend continues, that trusted man will eventually become as obsolete as the car he used to fill with leaded gasoline. The movement now is to self-service gasoline pumps from which customers will fill their own tanks. Station personnel will be present only to be certain the pumps operate properly and to collect payment.

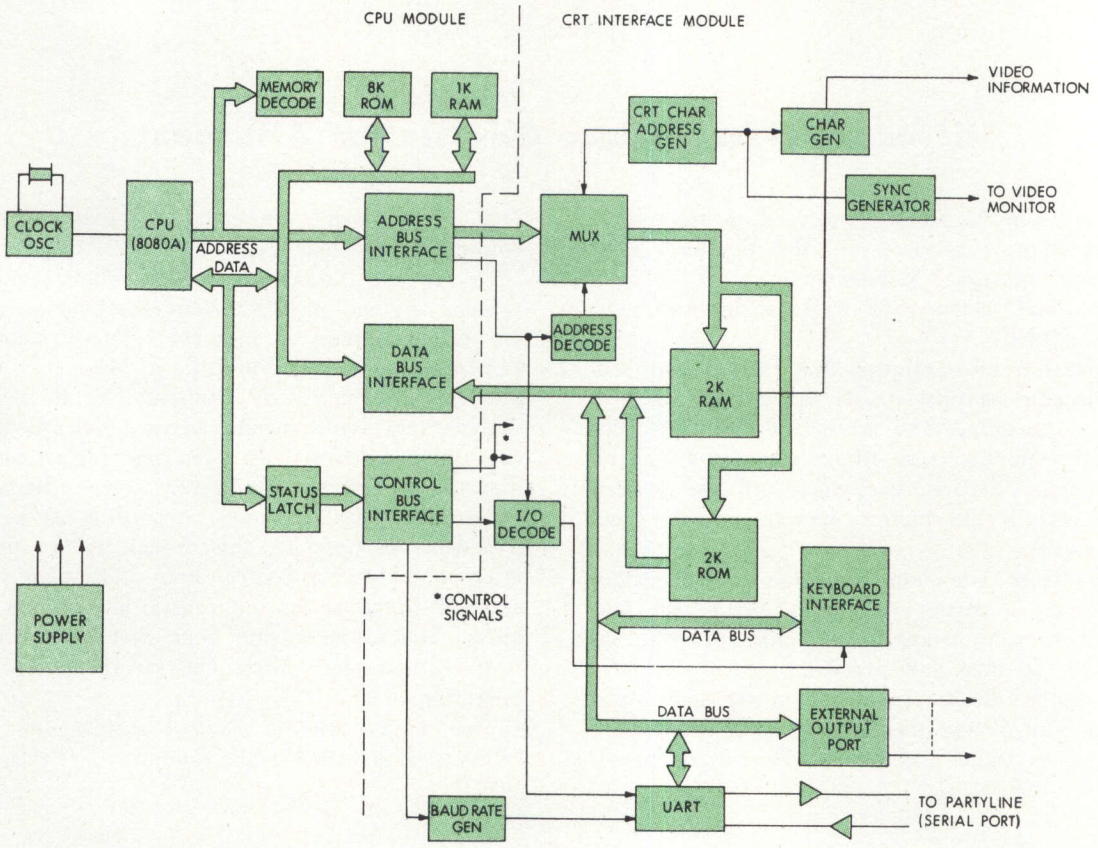
Conversion from attendant operation to self-service is not, however, a matter of simply laying off personnel and putting up signs with pump operating instructions. Both pumps and procedures must be automated to simplify the actions that the customer must perform, ease any qualms the customer may have about operating a gas pump, and assure the station owner that full payments are made and that all records are continually updated.

Degree of automation varies among available dispensing systems or those being designed—even within the product lines of individual pump manufacturers. For instance, Bennett Pump Co of Muskegon, Mich markets two systems: Baby Benn and Gentle Benn, covering low and high capacity systems. Baby Benn, a lower cost unit, works on only three hoses at a time for three dispensers (pumps). However, Gentle Benn operates on as many as 12 pumps. According to Bennett vice president Al Raschke, this system is the first to use microcomputers to control both individual gas pumps and all functions at the central attandant's booth or kiosk. The initial Gentle Benn system installation was in Grand Rapids, Mich but several others are now operating.

This microcomputer control system was developed in association with Process Computer Systems, Inc, 5467



Gentle Benn microcomputer-controlled gas dispensing system. Single 8080A microprocessor in kiosk attendant's control console interfaces with an F-8 microprocessor in each of up to 12 pumps. Microcomputers based on those processors control all aspects of gas dispensing in single mode or in any combination of four modes: full attendant operation, or self-service in postpay, prepay by dollars, or prepay by volume



Details of control console electronics. Console microcomputer not only controls signals to and obtains data from microcomputers at individual pumps, it also provides station manager with complete privileged bookkeeping information through the CRT display

Hill 23 Drive, Flint, MI 48507. Two microprocessor types are involved: an Intel 8080A in the central control console and a Fairchild F-8 in each pump. The microcomputers developed around these two types of microprocessors provide the versatility to meet both current requirements and those that would likely exist if rationing or control were to be instituted.

Gentle Benn at Work

Four modes of operation—all the modes that a self-service station can have—are available. First, if desired, an attendant can operate the station in a full service mode with no intervention from the kiosk central console. This justifies possible installation of the system in an area that does not yet have self-service—such as Ohio—but where it might be instituted in the near future.

The second mode is the most common. This is post-pay, in which the customer pumps the gas and then goes to the kiosk to pay for the amount of gas pumped. Probably 90 to 95% of the self-service gas stations use this mode.

In some areas, a third mode is being used more and more: prepay. The customer pays at the kiosk for the amount of gas wanted before any gas is pumped. Then the attendant "arms" the pump for that amount of gasoline and the customer returns to the island to pump the gas.

Prepay by volume—the fourth mode—is of value for commercial sales such as trucking fleets. A truck driver would be authorized to pump only a certain number of gallons as opposed to a dollar-worth of gas. This basic mode could also be used if rationing or a maximum delivery system were to become neces-

sary. An allocation limit would be set for each station and it would be impossible for anyone to obtain more than the legal limit on a single pump operation. The pump would automatically stop at the preset transaction level.

Modes can be changed very easily to meet changing requirements. For instance, a station might be on postpay during the day but change to prepay during the evening when attendants can't note license numbers on cars at distant islands where drivers might leave without paying. Also, this would eliminate the need to make change during high crime hours.

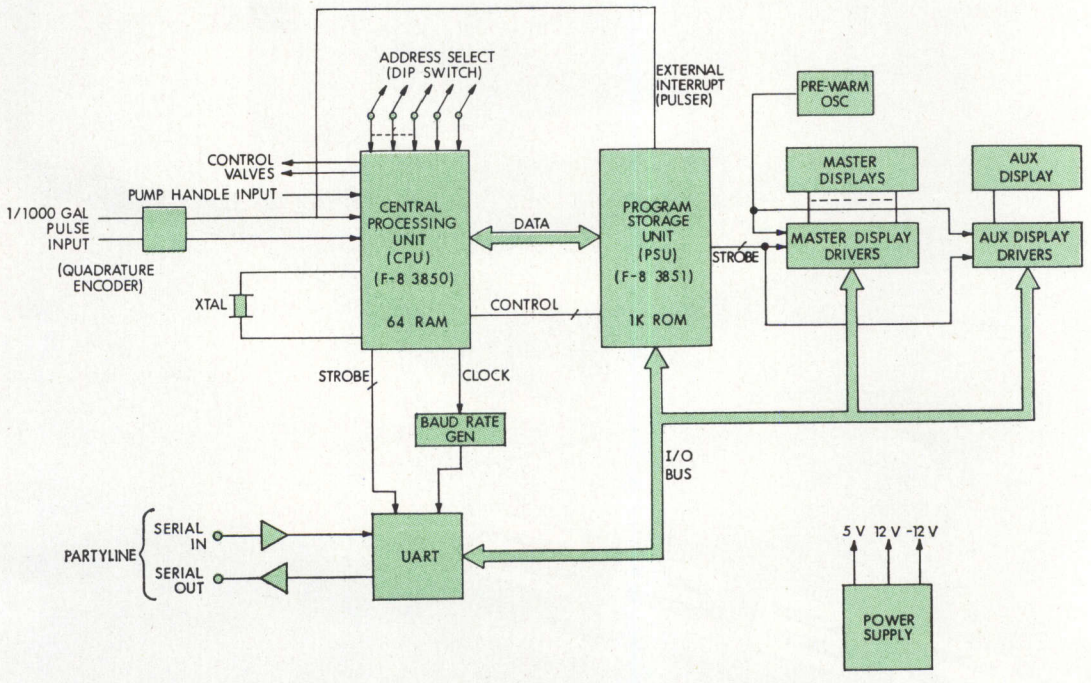
It is also possible to mix modes among islands at a station at the same time. Stations might prefer to have attendants serve some islands but set up other hoses for self-service. Customers could then choose between full attendant service at the regular price and self-serve at a reduced price.

Another option for the station manager is the ability to switch hoses (or pumps) from one tank to another. If, for example, the manager found that customers were being delayed at "no lead" pumps but "regular" pumps were idle, some hoses could be switched from "regular" to "no lead" by moving a few controls in the kiosk console.

Communication between control console and dispensers is bit serial on a partyline basis. Conversion to microprocessor compatible parallel format is performed by a universal asynchronous receiver transmitter (UART) that is tied into the partyline (see diagrams).

R. H. (Tim) Mendelsohn, Process Computer Systems project manager for gasoline dispensing systems, noted that a poll and select type protocol is used for the dispensers. Each dispenser controller has a separate address. When the control console microprocessor polls the pump microprocessors, each of those microprocessors responds only to its individual address. Data from each pump are then displayed on the console CRT. Present constraint of 12 dispensers to a system results from the maximum amount of display room on the console CRT rather than the number of units that could otherwise be connected to the partyline.

Pump displays—price per gallon, number of gallons dispensed, and total dollar amount of a transaction—are flat pack incandescent devices that fit directly on the microcomputer printed circuit board. Each pump has two identical 12-digit displays, the master display on the front of the PC board and an auxiliary display



Gas dispenser electronic details. Two-chip microprocessor controls operation of pump and reports to control console microcomputer which polls all pumps sequentially. Universal asynchronous receiver transmitter (UART) tied to partyline converts bit serial communication protocol to microprocessor compatible parallel format

Handling analog signals with any mini...Using RTP

Let's say you have to measure signals that originate from low level transducers, like thermocouples, and some higher level signals that have been pre-conditioned by a transducer amplifier. These signals may range from ±2.5mV to ±10.24V, full scale.

This application can be handled by an RTP Bus Converter for your mini, an RTP Wide-Range Analog Input Controller, and sufficient 8-channel gate cards to accommodate the signals to be measured.

The RTP Bus Converter interfaces the Wide-Range Controller to your mini by converting your mini's parallel I/O bus to the standard RTP parallel bus. Appearing transparent to your computer, it allows the Wide-Range Controller to be directly programmed, as if it were one of the computer's peripherals. Best of all, RTP Bus Converters are available for all popular minicomputers.

The Wide-Range Controller provides the logic, power, and space for up to 16 gate cards, or 128 channels of input. Need more? With expansion chassis, you can handle up to 512 channels with one controller. Still more? Simply daisy-chain controllers with the RTP parallel bus.

The Wide-Range Controller also allows random selection of both channel and gain at rates up to 200 sps, and uses proven reed relay scanning techniques.

There's more to RTP than our Wide-Range, though. RTP is a complete line of standard products that allows direct input and output of analog and digital signals to any popular minicomputer.

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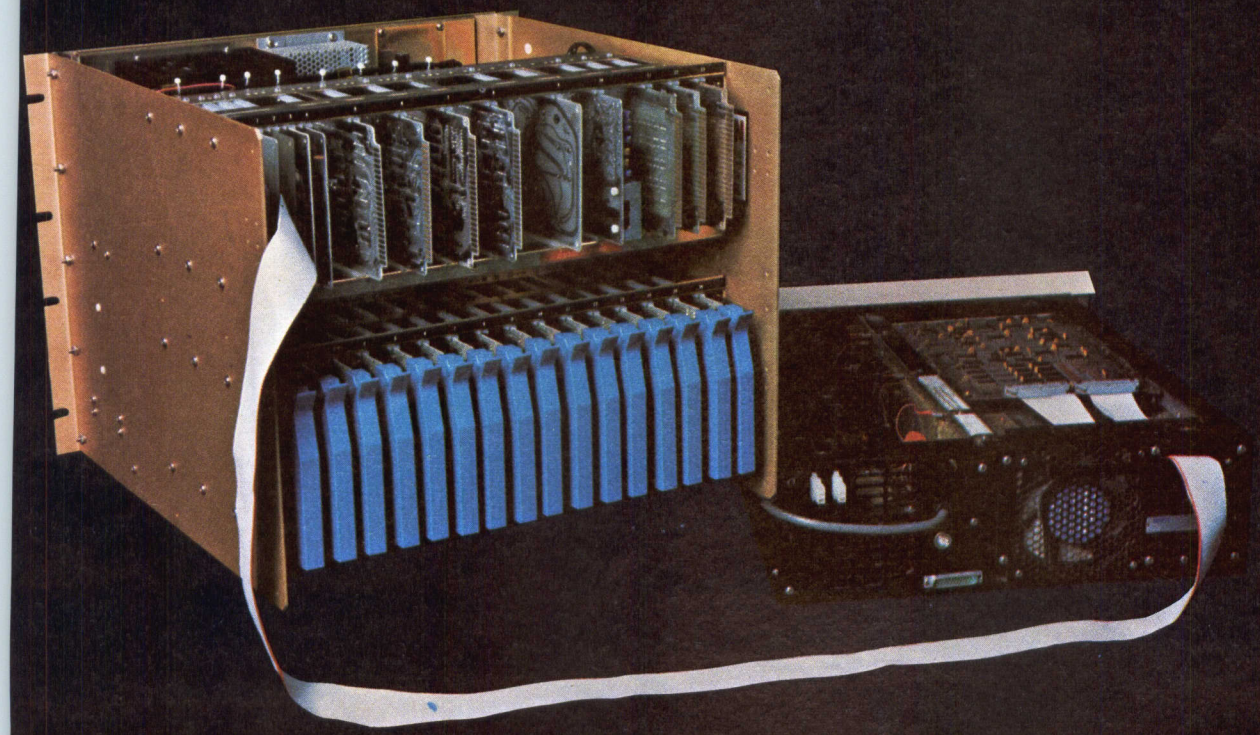

Wide-Range

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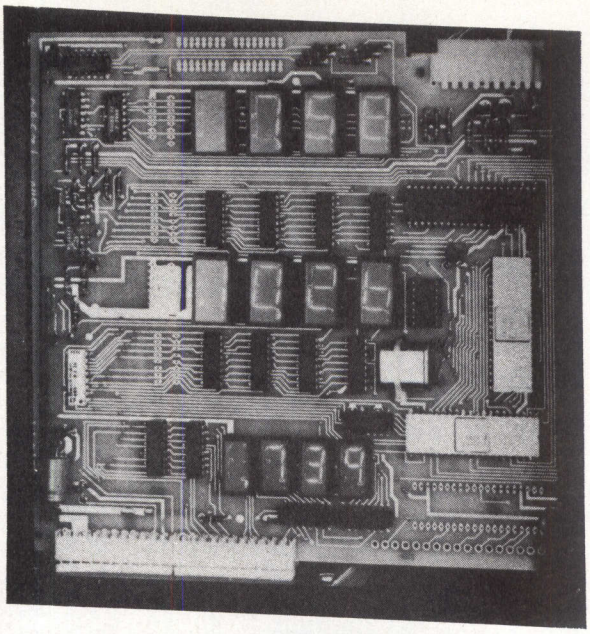
g3

on the rear. A prewarm oscillator strobes the display driver inputs to keep the segments slightly on but below the incandesce point at which they become visible. This eliminates the potentially damaging high in-rush currents associated with cold filaments.

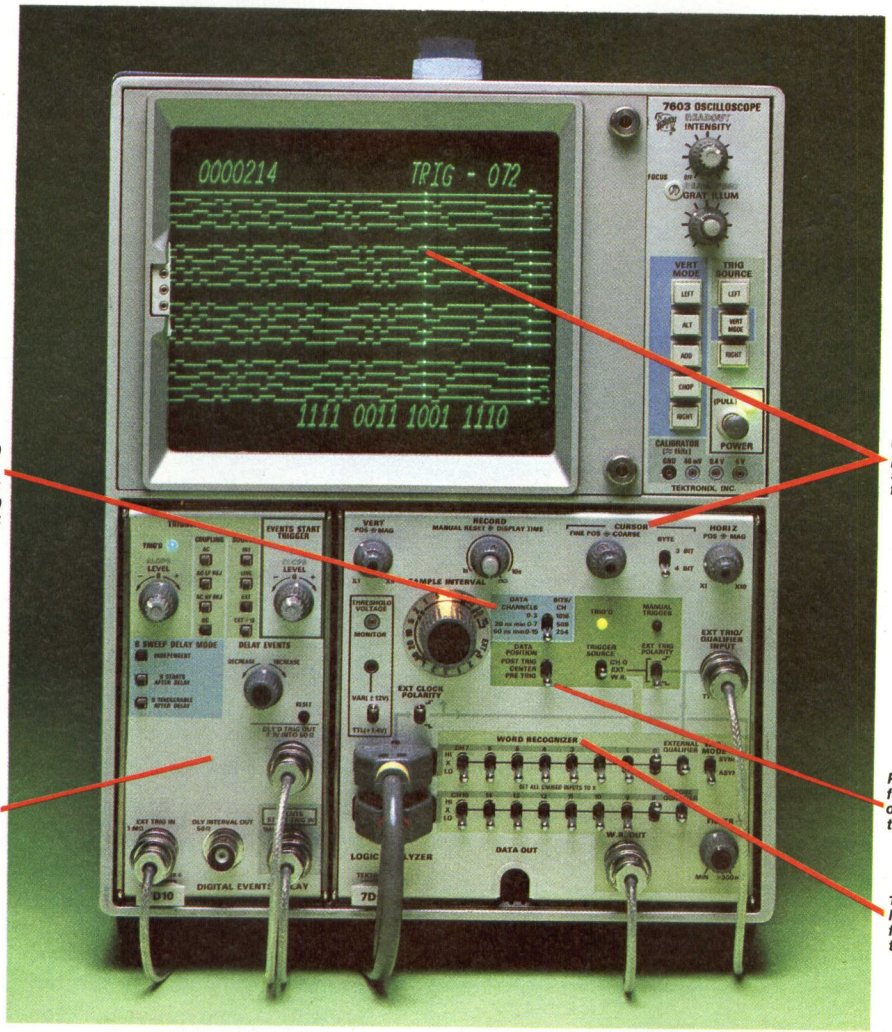
A ferroresonant power supply for the dispenser electronics provides 5, 12, and −12 V. Fairly wide voltage fluctuations can be tolerated by the associated regulators. The CRT in the kiosk uses a switching power supply that has battery backup. Gel cells, sealed lead-acid batteries, are constantly trickle charged so that they are fully charged and ready to operate the system for up to 15 minutes in case of ac line failure. That time is sufficient for the attendant to clear out sales.

Status of each pump is shown on the CRT in the kiosk control console. In normal online mode, the attendant knows if there is a customer in the process of pumping, if there is a customer at a dispenser who is not yet pumping, or if the customer has filled his tank and hung up the hose—and therefore should go to the kiosk to pay. In offline mode the attendant can accomplish bookkeeping duties normally associated with the sale of gasoline. Instantly available data include station totals in dollars, gallons, and



Gas dispenser PC board. Incandescent displays (duplicated for front and back of pump) show price per gallon, number of gallons dispensed, and total dollar amount for transaction. Prewarm unit keeps display filaments constantly just below illumination point until signal causes segments to incandesce for proper readout

Timing and state displays in one logic analyzer from Tektronix



FORMATTABLE MEMORY. 16 channels x 256 bits at 20 MHz
8 channels x 512 bits at 50 MHz
4 channels x 1024 bits at 100 MHz asynchronously; 50 MHz synchronous sampling.

CURSOR. For easy visual interpretation and timing comparisons. Converts selected word from timing to binary format.

DIGITAL DELAY. Use the 7D10 to delay by 99,999 events or words to access virtually any location in a data stream.

PRE-TRIGGER. For viewing faults before the trigger. Also offers center-trigger and post-trigger modes.

16-CHANNEL WORD RECOGNITION. Two additional qualifiers provide 18-bit parallel pattern recognition.

The 7D01 gives you both logic timing and state information in the same display. And many other features you'll probably need in a logic analyzer. The display is large and easy to read, as you can see from the photograph. It's easy to interpret, too: the trigger marker identifies the pre, center, or post-trigger point; the cursor you position yourself for binary readout of a particular word. You also get some other important logic analysis capabilities. Formattable 16-channel data acquisition plus a formattable 4k memory: acquire 4, 8, or 16 channels and store 1024, 512, or 256 bits at a time. Asynchronous timing resolution to 15 ns, synchronous operation with external clock rates to 50 MHz. Built-in word or pattern recognition. Active 1 MΩ/5 pF probes that won't load down the circuit under test.

One possible logic analysis system, the 7D01, the 7603 mainframe, and the 7D10 delay-by-events units, allows you to delay by up to 99,999 events (or words) and lets you access virtually any point in a data stream.

The 7D01 operates in any 7000-Series mainframe. If you already own a 7000-Series lab oscilloscope, you're that much closer to moving into high-performance logic analysis. For example, in a 4 compartment mainframe you can have a logic analyzer and a real-time oscilloscope in the same instrument mainframe. Either way, you benefit from the ongoing expansion of the 7000-Series line, both in the analog world and the digital domain.

Buy the 7D01 Logic Analyzer for $3,195 and the 7603 Oscilloscope mainframe for $1,850. Add digital delay with the 7D10 for $925.

Send for the technical details in our brochure, "Tektronix Logic Analyzers." Call or write Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077.

U.S. sales prices F.O.B. Beaverton, OR. The 7D01 Logic Analyzer is currently available only in the U.S.A.

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gallons per shift; shift totals, for 3-shift operation; cash and credit totals; and inventory totals.

The attendant can remotely control the price assigned by product at each dispenser. One input at the control console for one type of gasoline sets the price at all dispensers for that gasoline. It is no longer necessary—as with mechanical dispensers—to remove the skins from each pump and change price per gallon individually.

One key feature of the microcomputer-based system is the diagnostic procedure. Digits on all incandescent displays on each island are cycled from 0 through 9 and a corresponding visual test is run on the kiosk CRT. This permits the attendant to determine that all displays are working properly, that there are no burnt-out digits, and that displays are decoding correctly. It is also a check of the serial partyline.

A "return" test of the 2-way communications checks that the correct response is obtained from each dispenser microprocessor when it is polled by the console microprocessor. If a dispenser does not respond properly, the CRT will spell out "down" in the column assigned to that dispenser. In addition, the keyboard can be completely checked out by another test. In most cases a serviceman will know the exact trouble at the time he is called.

Influence on Tomorrow's Installations

Self-service gas pumps are not new. Over 25 years ago customers fed coins into slots in a box and then were able to pump a few gallons of gas into a glass cylinder or globe on top of the tank. Then the gas was drained by gravity into the automobile's tank. (Reporting how many gallons the customer could pump for a couple of quarters would serve only as a tormenting digression.) Through the years other systems have been put into use but none were particularly advanced technologically until the development of the microcomputer-based systems. None previously provided the flexibility and control features of Gentle Benn.

Even beyond the standard features noted for this automated gas dispenser, other capabilities are likely to be added in future microcomputer-based systems. The ability to mix grades of gas from two pumps to produce a third grade that meets the customer's specific desires—popular now in Europe—is one example. Others include printing receipts, validating credit card charges, and providing hardcopy printouts for the station manager's bookkeeping. In addition, because the dispenser microcomputer does not need to be mechanically attached to the pumping mechanism, a configuration feature feasible now would permit the electronics cabinet to be placed any distance away from the hose stanchion—a capability that conceivably could result in an entirely different look for future gas stations.

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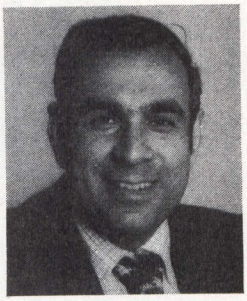
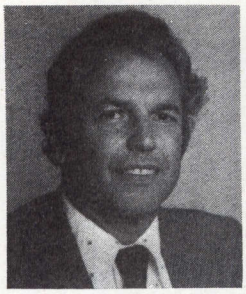
CIRCLE 35 ON INQUIRY CARD

Wescon/76 Silver Celebration

September 14-17
Los Angeles Convention Center



Louis H. Kurkjian
Chairman
Professional Program



Albert Eschner, Jr
Vice-Chairman
Professional Program

Dr Ruben F. Mettler
Keynote
Speaker

In observance of the 25th anniversary, Western Electronic Show and Convention's "Silver Celebration" will be highlighted by a full 35-session Professional Program. Organized by Chairman Louis H. Kurkjian, Hughes Aircraft, and Vice-Chairman Albert Eschner, Jr, Hoffman Electronics Corp, the program will consist of presentations and panel discussions covering varied aspects of the use, developments, and trends of computers, electronic and peripheral equipment, and technology. Current marketing areas, manufacturing views, and professional needs of engineers will be special considerations.

Wescon/76, co-sponsored by the Los Angeles Council and San Francisco Bay Area Council of IEEE and the Southern and Northern California Chapters of the Electronic Representatives Association, will concurrently present 725 exhibit booths in the Los Angeles Convention Center during the 4-day celebration.

Registration

Two areas have been planned for computerized registration, which will take place during show hours. Main registration will be at Petree Hall, located just off the main Convention Center promenade. Auxiliary registration services will be available at the opposite end of the Center (off Sentous St), adjacent to a separate parking garage. The $5 registration fee for the full week will cover both the exhibits and the Professional Program.

Exhibits

Exhibits from 400 companies occupying 725 booths will be presented on the Convention Center floor; they will be arranged in product-interest categories featuring Components and Microelectronics; Instruments and Instrumentation; Production and Packaging Equipment; and Computers, Peripherals, and Communications. Show hours will be from 9:30 am to 5 pm on Tuesday and Thursday, from 9:30 am to 9 pm on Wednesday, and from 9:30 am to 4 pm on Friday.

Special Activities

On Monday, Sept 13 (the day preceding Wescon), the 22nd annual Distributor-Manufacturer-Representative Conference will be held during the morning at the Los Angeles Hilton, which has been designated as convention hotel headquarters. About 500 marketing executives will take part in the DMR Conference. Dr Ruben F. Mettler, president of TRW Inc, will deliver the Keynote Address at the Wescon Luncheon which will also be held Monday at the Los Angeles Hilton.

Other activities will include the all-industry cocktail reception to be held on Tuesday evening at the Hilton; and the continuous Technical Film Theater, available daily to all visitors at no charge.

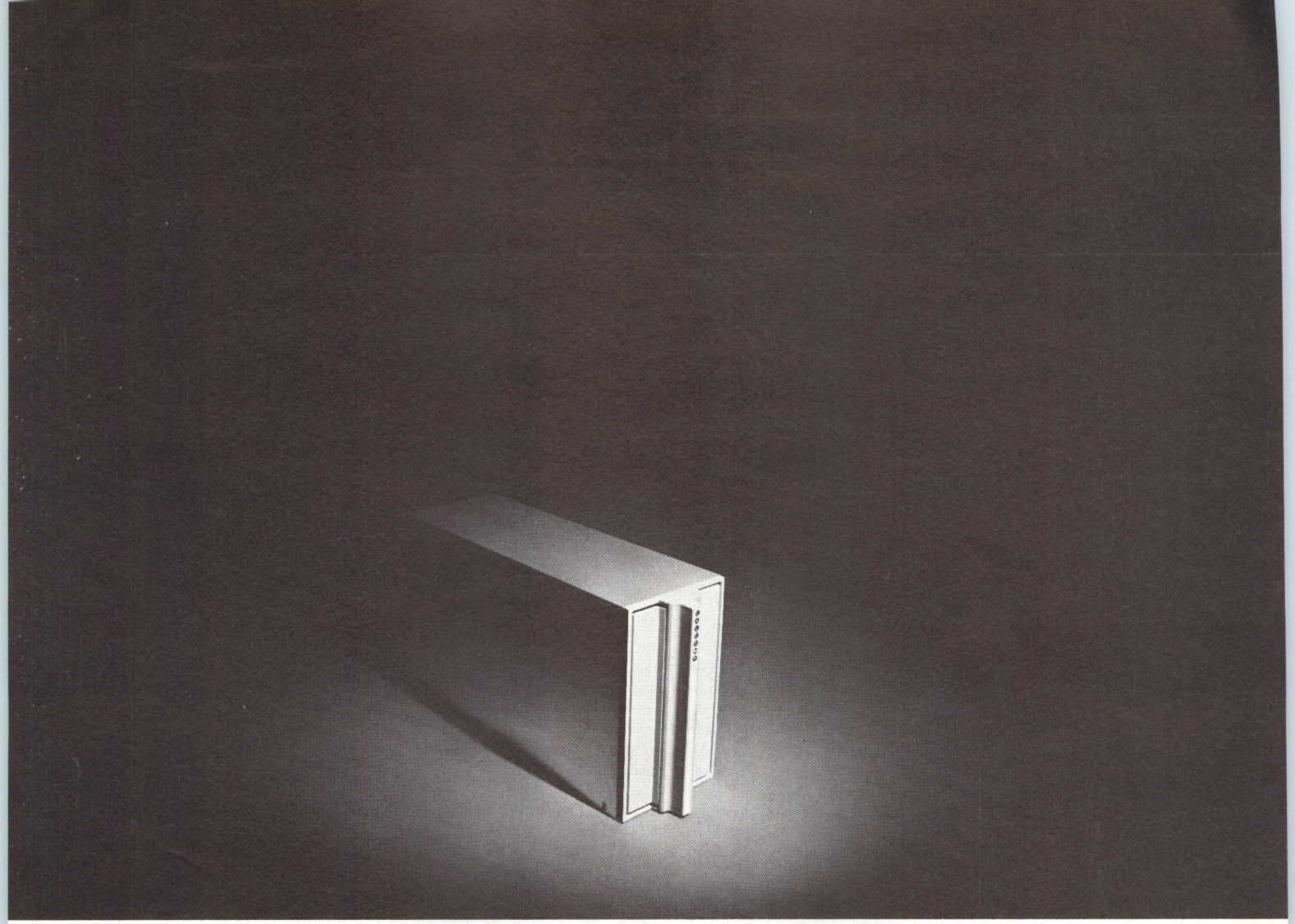
The Convention Center has parking facilities for 5000 cars. In addition, two park and ride commuter bus services will be established, operating on continuous schedules throughout the show. One terminal will be located at the TRW parking lot in the Los Angeles International Airport area; the other will be a parking facility near Hollywood-Burbank Airport in San Fernando Valley. A nominal round-trip fee will be charged.

Professional Program

Five sessions will be held concurrently at 10 am and 1:30 pm on Tuesday, Wednesday, and Thursday, and at 10 am on Friday, in meeting rooms located on the mezzanine of the Convention Center. The full program of 35 half-day sessions will concentrate on applications, advances, developments, and future speculations, as well as the needs and viewpoints of engineers and users. Among the areas of major interest will be sessions dealing with mini and microcomputers, design aids, communications, LSI technology, medical electronics, manufacturing, and marketing.

Approximately 160 speakers and panelists will be participating in the program. Full manuscript preprints and audio tapes of most sessions will be available.

Only sessions of particular interest to *Computer Design* readers are covered here; information is limited to that available at press time.



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TECHNICAL PROGRAM EXCERPTS

Tuesday Morning

Session 1 10 am-12:30 pm Room 217A

Microcomputer Applications

Organizer/Chairman: Robert Van Naarden, Digital Equipment Corp

Session demonstrates how various companies have implemented microcomputers into their products. It is important to understand not only the product, but also the design criteria for choosing a microcomputer as well as problems which can arise during implementation.

"Microprocessor Simplifies Impedance Measurements," M. A. Gipe, H. B. Hall, and R. Sullivan, GenRad

"The Microcomputer and Photographic Printing System," Robert C. Davis, Bremson Photo Industries

"Microcomputers In Voice Input Systems," Marvin B. Herscher, Threshold Technology

Session 2 10 am-12:30 pm Room 217B

Mini Computer Power Supplies

Organizer/Chairman: Cle Riggins, Hewlett-Packard Data Systems

Demands and requirements of computer power supplies are increasing even in today's world of semiconductor memories and stringent safety requirements. Session is targeted to cover designer and user interests and to provide safety requirements and power source characteristics.

"User Needs of Mini Computer Power Supplies," Rudolf Severns, Magnavox

"The U.L. Approach to Safety for the Minicomputer Power Supply," Robert Harris, Underwriters Laboratories

"Interfacing Utility Supplied Power with Critical Loads," P. L. Wheeler, Southern California Edison Co

"Designing Today's Minicomputer Power Supply," Kenneth Check, Hewlett-Packard Data Systems Div

Session 3 10 am-12:30 pm Room 212A

Automated Microcircuit Interconnections Clinic

Organizers/Chairmen: Stanley M. Stuhlbarg, Hughes Aircraft Co; and Ralph Redemske, Teledyne Microelectronics

This latest in a continuing series of Hybrid Microelectronics Clinics examines timely and increasingly controversial questions related to production cost of multi-chip digital and analog hybrid microcircuits as emerging technologies, in competition with conventional DIL packaging approaches. Topics include semiconductor assembly from tape-chip carriers, automatic wire bonding, and manufacturing technology involving beam-leaded or flip-chip device usage.

Panelists: Francois Gallet, Honeywell Bull, Paris, France; H. Khajezadeh, RCA Solid State; C. Scott Kulicke, Kulicke and Soffa Industries; Rudy Oswald, Honeywell Inc; William Meder, Motorola Semiconductor; and James M. Smith, Intel Corp

Session 5 10 am-12:30 pm Room 216

The Engineer After 40

Organizer/Chairman: Harold S. Goldberg, Data Precision Co

Panel debates such statements as: Continuing education does not help the engineer, employer, or job security; If you are not in management by age 35 or have not made your reputation technically by that time, take a course in selling insurance; The engineer after 40 is living on borrowed time; The needs of over-40 engineers are different: they need counseling, not technical training.

Panelists: James J. Rago, Jr, Cleveland State University; Albert J. Morris, Genesys Systems; Robert Anderson, Purdue University; and Raymond Price, Stanford University

Tuesday Afternoon

Session 6 1:30-4 pm Room 217A

Microprocessor Design Aids—The μP Manufacturer's Viewpoint

Organizer/Chairman: David N. Kaye, *Electronic Design* Magazine

Hardware and software design aids for microprocessors and microcomputer systems have come a long way in the last year. These range from learning modules and kits to sophisticated microprocessor-based computer systems complete with CRT terminals, printers, and floppy discs. Several systems are described, with a glimpse of what the future may bring.

"Fairchild Microprocessor Design Aid Philosophy," Anthony R. Beccia, Micro Systems

"Design Aids for the 6800," Don Kesner, Motorola Semiconductor

"Design Aids for National Microprocessors," Philip M. Roybal, National Semiconductor Corp

"Design Aids for Intel Microprocessors," Bill Broderick, Intel Corp

Session 7 1:30-4 pm Room 217B

Pocket Calculator Update

Organizer/Chairman: Rudolph Panholzer, Naval Postgraduate School

Emphasizing question-and-answer dialogue, session has 5-minute formal presentations by authors. Most of the time is devoted to discussion of the impact and importance of sophisticated pocket calculators on professional engineering and science education.

"The Multiple Dimensions of Programmable Calculator Comparisons," Ed Lybrand, Texas Instruments

"The Programmable Pocket Calculator's Impact on Our Professional Lives," Robert B. Johnson, National Semiconductor Corp

"Closing the Gap Between Calculator Users and Manufacturers," Richard J. Nelson, Statek Corp

"Science Education and the Calculator—A Perfect Marriage," George McCarty, University of California, Irvine

(Paper title to be announced), Glenn Theodore, Hewlett-Packard Co

Session 8 1:30-4 pm Room 212A

ATE Hardware/Software Developments to Reduce Set-Up Costs

Organizer/Chairman: Robert T. Szpila, GenRad

Papers cover the different aspects of the ATE set-up problem. Both functional and in-circuit testing are explored with a description of the costs of hardware (fixtures and interfaces) and software (test program generation) associated with each method.

"Testing Using Automatic Pattern Generation," Noel P. Lyons, Fluke-Trendar Corp

"New Test Generation Techniques for Minicomputer-Based Digital Circuit Test Systems," Pat T. Harding and R. Wade Williams, GenRad

"Automatic In-Circuit Program Generation Reduces Printed Wiring Board Test Costs," Charles M. Hults and Fred A. Schwedner, Faultfinders Inc

"Improvements in Fixture Design Reduce the Cost of Complex ATE Interfaces," L. E. Wysocki, Everett/Charles Inc

Session 10 1:30-4 pm Room 216

Reliability Comparisons of Manufacturing Process —Military and Commercial

Organizer/Chairman: James E. Bridgers, Jr, Hoffman Electronics

Standard military parts have several reliability levels to choose from, definable in terms of price, schedule, and assigned numbers for procurement identity. Standard commercial parts are also definable in terms of price and schedule by each supplier, but procurement identity is not an industry standard. Describing standard manufacturing processes that determine the delivered reliability attributes for various levels of standard commercial and military parts, each presentor also provides some procurement tips for commercial parts.

"Motorola Military Vs Commercial Semiconductor Reliability," Steve Stephens, Motorola Semiconductor

"Diode Manufacturing Processes; Military Vs Commercial," Gary Penny, Siemens Corp

"Sprague Filter Capacitor Processing; Military Vs Commercial," Ed Geissler, Sprague Electric Co

Panelists: Link White, Rockwell International; and Robert Hunn, King Radio

Wednesday Morning

Session 11 10 am-12:30 pm Room 217A

Microprocessor/Microcomputer Standardization Schemes in Industry and Government

Organizer/Chairman: C. E. Holland, Jr, Naval Electronics Laboratory

Material covers existing and proposed microprocessor/microcomputer standardization schemes within several electronics/computer companies and government military agencies. Schemes which influence design of military systems, computer mainframes and peripherals, and consumer products are presented, with their advantages and disadvantages, especially design time and cost savings.

"An Approach to Microprocessor/Microcomputer Standardization in Navy Systems," Ralph Martinez and Reeve Peterson, Naval Electronics Laboratory Center

"Military Distributed Processor for Global Positioning System," Leo Chamberlin, Texas Instruments

"Microcomputer for Multiple Applications," C. D. May, Jr, and R. E. Mellott, Control Data Aerospace Div

(Paper title to be announced), Hank Molloy, Intel Corp

Session 12 10 am-12:30 pm Room 217B

Interfacing Microprocessor Instrumentation to the GPIB (General Purpose Interface Bus)

Organizer/Chairman: John P. Brady, Jr, Dana Laboratories

Session explores the IEEE 488 GPIB from an equipment manufacturer's viewpoint, as well as from that of the systems designer and user. The first paper presents an overview of this IEEE standard, while the remaining papers concentrate on advantages and disadvantages of the GPIB as seen by those who presently are working with it.

"IEEE 488—A General-Purpose Means of Providing Measurement and Stimulus Instrument Communication," Norbert Laengrich, Dana Laboratories

"Design Advantages and Limitations in Connecting Computational Readout Equipment to the GPIB," Steve Baunach, Tektronix Inc

"GPIB Command Structures," Pete Silvernale, Wavetek Corp

"The Systems Designer Looks at the GPIB as a User," Eugene Fisher, Lawrence Livermore Laboratory

Session 13 10 am-12:30 pm Room 212A

Pattern Recognition Systems

Organizer/Chairman: Demetrios A. Michalopoulos, California State University

This survey and applications session is designed to update activity in the field, predict trends, and indicate specific applications in medicine (chromosome analysis), forestry, data management, and law enforcement.

"Human Chromosome Automatic Recognition," Mike Merritt, Rockwell Air Monitoring Center

"The Use of Statistical and Texture Measures in Automatic Tree Recognition," Robert P. Chiralo, Aerospace Corp

"Data Base Considerations After Pattern Recognition," Albert L. Zobrist and Nevin A. Bryant, Jet Propulsion Laboratory

"Pattern Recognition Applied to Law Enforcement," John Riganati, Rockwell International

Session 14 10 am-12:30 pm Room 212B

Optical Fiber Communication, How, Why, When

Organizer/Chairman: William M. Caton, TRW Systems Group

Session is designed to show how optical fiber technology is applied to communications systems, why this technology is being selected over competing technologies, and when optical fiber systems will see wide-spread use.

"Transmission of Common Signals Via Optical Fibers," Jim E. Goell and Tom A. Eppes, ITT Electro-Optical Products

"Optical Fibers for Communications," Eric N. Randle, Valtec Corp

"U.S. Navy Fiber Optics Applications," Don N. Williams, Naval Electronics Laboratory Center

"Interchange Digital Links Using Optical Fiber Cables," Gerald Aaronson and J. E. Fulenwider, GTE Sylvania and GTE Laboratories

"Role of Fiber Optics in the Army," Louis Coryell and Larry U. Dworkin, Army Electronics Command

Session 15 10 am-12:30 pm Room 216

The Electron and the Mind—Probing and Controlling the Human Mind with Electronics

Organizer/Chairman: Erich A. Pfeiffer, Veterans Administration Hospital

Electronic methods and devices have long been used to probe the functioning of the human mind and even to control some aspects of human behavior. In this session, some aspects of the use of electronics in neuropsychological research and therapy are described, and future developments are explored.

"Human Memory Testing," Walter H. Riege, VA Hospital and UCLA

"Manipulation of EEG through Biofeedback Methods and its Effect on Epilepsy," M. B. Sterman, VA Hospital and UCLA

"Biofeedback Therapies for Migraine Headache," Michael J. Cohen, VA Hospital and UCLA

"Psychotechnology: Building a Smart Environment for Dumb People," Robert L. Schwitzgebel, Claremont Graduate School

Wednesday Afternoon

Session 16 1:30-4 pm Room 217A

Universal Microprocessor Design Aids

Organizer/Chairman: Zoltan Tarczy-Hornoch, Systron-Donner Corp

To solve the problems of multi-family microprocessor users, new universal design aids, development systems, and debugging tools begin to emerge, usable with all or most present and anticipated microprocessor systems. Four such universal approaches, all new and different, and their applications, advantages, and limitations are explored.

"Hardware and Software Trade-Off in a Universal Microprocessor Development System," Bruce Gladstone, Microkit Inc

"A Universal Instrument for Software/Hardware Troubleshooting," Zoltan Tarczy-Hornoch, Systron-Donner

"Visibility of a Universal Bus for 8, 12, 16 Bit Microprocessors in a Development System," Bryan G. Moonier, Micro Specialists

"Universal Emulation Using Bus Intercept," Roger Doering, Digital Electronics Co

Session 17 1:30-4 pm Room 217B

Logic Analyzers: What Are They, and Where Are They Going?

Organizer/Chairman: Stanley Runyon, *Electronic Design* Magazine

Logic analyzers have formed an important new class of instrument. Some industry observers feel that the analyzer's contribution is so important that it may one day replace the oscilloscope. Session provides a forum for discussion, and attempts to answer questions such as: What form should an analyzer take? What functions should it perform? Can present analyzers handle all digital and μP test problems? What will analyzers look like in the future?

"Logic Analyzers Are Growing Up," Don Wilkin, Hewlett-Packard

"Uses and Performance Levels of Current Logic Analyzers and their Future Trends," Roy Tottingham, Biomation Corp

"The Logic Analyzer: The Compleat System Instrument," Carver Hill, E-H Research Laboratories

"The Coming Logic Analyzer Explosion," Rick Watkins, Tektronix Inc

Session 18 1:30-4 pm Room 212A

Graphic Display of Information—A Discipline That Has Come Of Age

Organizer/Chairman: Jerry Wasserman, Arthur D. Little Inc

Relevance of graphic display technology to the electronics industry is quite apparent, with much activity among hardware suppliers to develop soft and hard copy graphic display terminals and systems. Subjects covered will help the engineer, marketing man, and general manager to react to and comprehend the implications of, and participate in, the emerging arena of graphic information display.

"Graphic Technology and Its Relationship to the Display of Spatial Data Software," Eric Teicholz, Harvard University Graduate School of Design

"Computer Graphics Hardware," Lewis McFarland, Tektronix Inc

"Computer Graphics in Business Decision Making," Erik Albarda, Arthur D. Little Inc

Session 19 1:30-4 pm Room 216

Application of Charge Transfer Devices to Sampled-Data Signal Processing

Organizer/Chairman: Gene P. Weckler, Reticon Corp

Charge transfer devices are available which offer a cost-effective way of performing real-time sampled data signal processing, the basis of which is the summation of lagged products of one signal relative to a second signal. A comparison is made of digital, analog, and sampled-data analog signal processing as implemented with various charge transfer devices.

"An Introduction to Sampled Data Analog Signal Processing," Robert W. Brodersen, University of California

"Implementation of Discrete-Time-Lag-Product Systems," Satoru C. Tanaka and Robert R. Buss, Reticon Corp

"A CCD Lens for Ultrasonic Imaging Applications," R. D. Melen, J. D. Shott, and J. D. Meindl, Stanford University

"A Programmable Binary-Analog Correlator," Udo S. Strasilla, Reticon Corp

Session 20 1:30-4 pm Room 216

Telecommunications for Civic and Social Services

Organizer/Chairman: S. H. Durrani, NASA/Goddard Space Flight Center

A considerable amount of current work is aimed at defining and meeting the telecommunications requirements for civic and social services of the 1980s. The next few years will see the development of many new systems. Results of experiments and pilot projects in the areas of telemedicine, teleconferencing, telecommunications for law-enforcement, satellite-aided systems for automatic vehicle monitoring, direct TV broadcasting, and search and rescue are presented in this session.

"The Cleveland Telemedicine Project," J. S. Gravenstein, University Hospital

"Teleconferencing: Status and Outlook," P. Polishuk, Horizon House International Div

"Innovative Telecommunications Systems for Law Enforcement," Robert Sohn, Jet Propulsion Laboratory

"Automated Vehicle Monitoring Via Satellites," Joseph Bravman, Fairchild Space & Electronics; and S. H. Durrani, NASA/Goddard Space Flight Center

"Making It Happen: The Feasibility of Satellite Communications for Public Service," J. P. Witherspoon, Public Service Satellite Consortium

"Search and Rescue Programs Using Satellites," J. Trudell and D. L. Brandel, NASA/Goddard Space Flight Center

Thursday Morning

Session 21 10 am-12:30 pm Room 217A

Microcomputers for Fun and Profit

Organizer/Chairman: Frank J. Burge, Regis McKenna Advertising

Every other Wednesday evening about 300 people, all members of the Homebrew Computer Club, a collection of computer hobbyists, gather at the Stanford Linear Accelerator auditorium to swap stories about microcomputer kits, new games, or programs. The average hobbyist invests $1000 to $1500 in a computer. Session covers the hobby market for microcomputer systems, which some estimate at $10M and growing rapidly.

"The Significance of the Non-Professional Market for Microcomputers," Bob Wickham, Vantage Research

"What Are Hobbyists Doing with Microcomputers?" Eddie Currie, MITS

"The Microcomputer for the Home," Manfred Peschke, *Byte* Magazine

"The Future of the Neighborhood Computer Store," Paul Terrell, The Byte Shop

Session 22 10 am-12:30 pm Room 217B

Needs and Trends in Medical Electronics—1976

Organizer/Chairman: Morton D. Schwartz, California State University

Objective of session is to present new engineering concepts, technologies, and techniques which will impact the field of medical electronics during the 1976-1978 period.

"Electronics in Medicine: An Overview," Morton D. Schwartz, California State University

"Biomedical Engineering—Cost Effectiveness and Patient Care Implications After Five Years of Operation in a Community Hospital," B. H. Barkalow, Sutter Community Hospitals

"Microprocessor Monitor for the EKG and Blood Pressure, Part I," Wayne Darchuk, Paul Hsue, and Martin Graham, University of California

"Microprocessor Monitor for the EKG and Blood Pressure, Part II," Tim Conway, M. S. Roger Dwinelle, Curt Skytte, and J. R. Singer, University of California

"Impact of Complex Technological Systems in the Intensive Care Environment," George I. Hickey, George Hickey and Associates

"Application of FET Semiconductor Technology to Biochemically Specific Transducers," S. Moss, J. Janata, and C. Johnson, University of Utah

"Use of Minicomputers in Hospitals," Brewer W. Ward, St. Mary Medical Center

Session 23 10 am-12:30 pm Room 212A

Future LSI Technologies

Organizer/Chairman: B. Dunbridge, TRW Systems Group

Session focuses on a selected cross-section of future technological developments in LSI, with an overview of the promising areas. Both technologists and users have come to expect efficiencies through LSI utilization, in regard to various parameters—complex functions, high density, high frequency, and low

It takes a lot of guts to get ahead.

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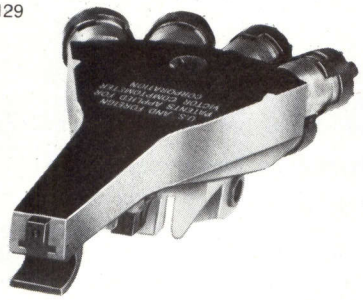

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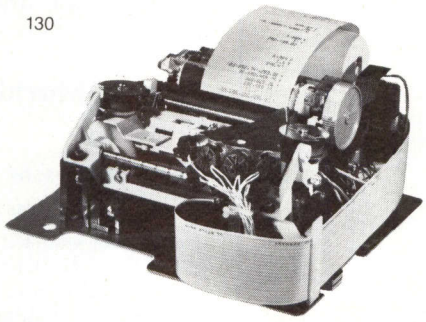

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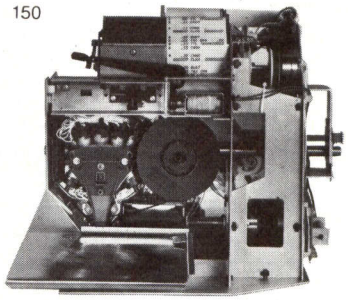

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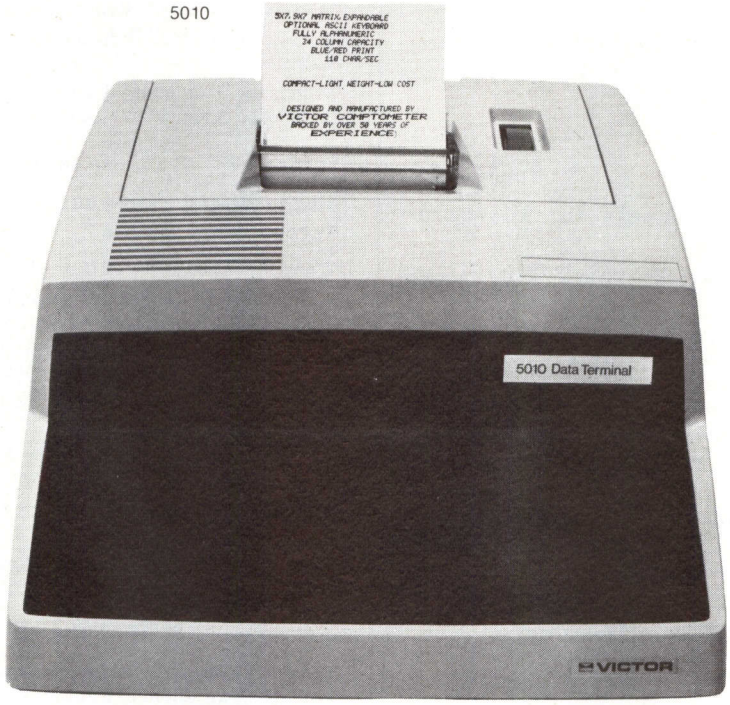

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The 5010 allows interfacing with RS232C, 8-bit parallel or TTY current loop. With Intel MCS-40 you have a data terminal with a mind of its own.

The 5005 terminal comes complete with a matrix printing mechanism, integrated power supply, and driver circuitry. It's designed so you can add your own control logic, and is ideal for special applications like ticket or label printing.

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power. This trend is still continuing in the form of bipolar VLSI, CCD memory, RF LSI, and I^2L.

"CCD Large Scale Memory," Robert W. Bower, Mnemonics Inc

"VLSI Bipolar Technology," James L. Buie, TRW Defense & Space Systems Group

"RF Goes LSI," David R. Breuer, TRW Defense & Space Systems Group

"I^2L/LSI for Complex Logic Arrays," Donald E. Romeo and Klaus Schuegraf, Northrop Research & Technology Center

Session 25 10 am-12:30 pm Room 216

High Speed Logic Interconnection Techniques

Organizer/Chairman: R. J. Clark, General Electric Co

Available high speed logic circuits can meet the need for lower cost, faster, and more complex processing. Increased speed also poses a new set of design problems: control of line impedances, crosstalk, reflections due to discontinuities in signal lines and connectors, thermal problems due to higher density assemblies, and need for cost-effective interconnection and assembly techniques.

"High Speed Logic Packaging Using Multiwire™ Interconnection Technology," J. Hammond, Photocircuits Div, Kollmorgen Corp

"High Speed Logic Packaging Using Stitch Weld Interconnection Technology," D. Moore, Moore Systems

"High Speed Logic Packaging Using Solder Wrap® Interconnection Technology," R. Whitehead, United Wiring & Manufacturing Co

"High Speed Logic Packaging Using Wrapped Wire Interconnection Panels," Len Doucet, Augat Inc

Thursday Afternoon

Session 26 1:30-4 pm Room 217A

High Performance Building Blocks for Microprogrammed Systems

Organizer/Chairman: Rudolph Panholzer, Naval Post-Graduate School

Microprocessors and microcomputers have captured the attention of just about every electronics engineer. However, many engineers overlook the fact that there exist attractive and superior solutions to their problems in the form of high performance functional blocks for implementing microprogrammed systems. This session balances and complements those offered on microprocessors and microcomputers.

"Overview—Various High Performance Bipolar Bit Slices," Peter Alfke, Fairchild Microsystems

"Microprogramming for the Hardware Engineer," John R. Mick, Advanced Micro Devices

"Bit Slices, Fact or Fancy," Rob Walker, Intel Corp

"The Bipolar Microprocessor Revolution of 1976," John Birkner, Monolithic Memories

Session 27 1:30-4 pm Room 217B

TV Games

Organizer/Chairman: Dave Uimari, Signetics Corp

Session focuses on the rapidly developing games market, highlighting technical considerations for both coin-operated and home video games, together with the economic aspects of each. Predictions are made on the future of games, and other roles electronics will play in the personal entertainment industry.

"Technical Aspects of Video Games," Kam Li, Signetics Corp

"Home Video Games," John Sluzarski, Magnavox Co

"The Future of Games," Jerry Lawson, Fairchild Semiconductor

Session 28 1:30-4 pm Room 212A

Next Generation—The LSI Computer System

Organizer/Chairman: William J. Thomas, Four-Phase Systems

Utility of an LSI processor is determined by the cost of the software and I/O interface; future development will be to expand the LSI computer system to decrease these costs. The next generation will involve processors that execute at the language (BASIC, PLM, XPL) level; self-sufficient LSI systems on which software can be developed in a more cost-effective manner; powerful LSI I/O support chips; and LSI RAM systems with much larger capacities, negating the need to minimize software RAM utilization.

"Semiconductor LSI and Computers of the Future," Bob Wickham, Vantage Research Services

"Emerging Trends to Reduce the High Cost of Microcomputer Utilization," Manny Lemas, Microcomputer Associates

"Microprocessor Vs LSI Computer Systems," John Stidd, Four-Phase Systems

"Microprocessor Architecture Vs High-Level Language Execution," Charlie Bass, Zilog

Friday Morning

Session 31 10 am-12:30 pm Room 217A

Microprocessor Tools and Techniques

Organizer/Chairman: Mike Paige, Science Applications Inc

Beyond conventional assemblers, compilers, and development systems, there are numerous new tools of tremendous utility to the microprocessor user/designer. Session reviews three ideas used by experienced designers to economically produce reliable products.

"A Survey of Kits," Robert Grossman, *EDN* Magazine

"RAID: A Radical Debugging Tool," Terry L. Dollhoff, Acuity Systems

"Automatic Validation of Program Correctness," Edward F. Miller, Jr, Science Applications Inc

Session 32 10 am-12:30 pm Room 217B

Single-Board Computers: The Emerging Micro Versus Mini Battle

Organizer/Chairman: Dave Bursky, *Electronic Design* Magazine

Session covers problems of selecting a low-cost computer, discussing both differences and advantages. Should you use a minicomputer on a board, such as the LSI-11 or MicroNova, or a microprocessor system on a board, such as the SBC80 or SC/MP? In some applications there is almost no difference between them; in others, the boards may be worlds apart.

"Hardware Aspects: Micros vs Minis," Bob Pecotich, National Semiconductor

"Packing Capability Into Microcomputers and Minis," George Adams, Intel Corp

"Software Development Tools Needed for Microcomputers," Bob Brick, Digital Equipment Corp

"The Capabilities of Micros and Minis," Ed Zanders, Data General Corp

"Should You Use a Microcomputer to Replace Hard Wired Logic?" Matt Biewer, Pro-Log Corp

Session 35 10 am-12:30 pm Room 216

The ATE Role in Field Service for Printed Circuit Boards

Organizer/Chairman: Richard L. Stein, Computer Automation

This session identifies problems facing field service organizations today, and suggests solutions which integrate various manufacturing philosophies into cost-effective field service approaches.

"Overview: Planning a Field Service Philosophy," Richard L. Stein, Computer Automation

"Translating Factory Test Programs for Field Service Use," Robert E. Anderson, Omnicomp

"Comparison Testing for Field Service," Donald P. Allen, Fluke-Trendar Corp

"Digital Field Maintenance: A Practical Approach," Roger M. Boatman, Testline Instruments

"Impact of Manufacturing ATE Approach on Field Service," David A. Crocker, GenRad □

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Now you can replace small, fast access, disc and drum memories with Intel's new solid state CCD memory called IN-65 Megachassis.™ Each Megachassis contains 2 megabytes of CCD serial memory with expansion in 2 megabyte increments up to 16 megabytes or more.

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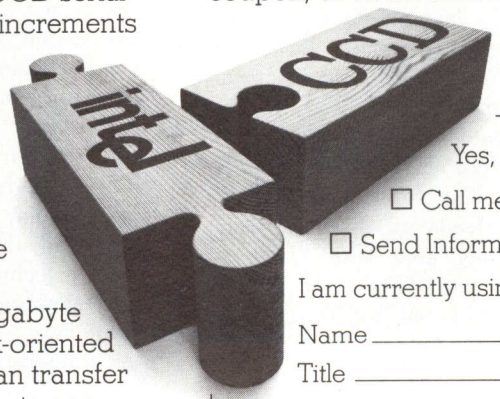

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IEEE Computer Society International Conference

Mayflower Hotel, Washington, DC, September 8-10

Under the theme "Computers . . . by the millions, for the millions," which attempts to point up the increasing pervasiveness of computers, the IEEE Computer Society's 13th International Conference will present a Great Debates series, an applied tutorial workshop, and a full technical program. Combining a state-of-the-art roundup of "what's happening" by acknowledged technical leaders with "hands-on" engineering-oriented sessions, COMPCON'76 Fall will consist of 29 technical sessions under the direction of General Chairman Walter R. Beam, Deputy to the Assistant Secretary for Advanced Technology, and Technical Program Chairman, Paul L. Hazan, Applied Physics Laboratory, Johns Hopkins University.

On Tuesday preceding the formal conference opening, an applied tutorial workshop, "Designing With Microprocessors," will cover basic concepts and recent advances in microprocessors and microprocessor interconnection, and provide a hands-on demonstration of the concepts discussed. Also on Tuesday, the tutorial "Structured Programming" introduces basic ideas of technique and their theoretical and practical foundations, and goes on to detail the development of simple and application programs.

Keynote sessions in all major areas will be held at 11, 11:30, and 12 noon on Wednesday as a forecast of what is to come. Dr Frederico Faggin, president of Zilog Corp, sets the pace for sessions in the microprocessor area with "Trends in Microcomputers." "New Management and Technology Horizons" introduces sessions dealing with software, and "Real-Time Systems . . . Undefined But Understood," presented by Daniel G. O'Connor, technical director for The Singer Co, points the direction for following sessions under the heading of Real-Time Systems. Dr H. Dean Toombs, technical director at Texas Instruments, will keynote the Components and Memory Technology area with "Semiconductors and Memories . . . The Pace is Accelerating"; Richard J. Clayton, vice president for computer systems, Digital Equipment Corp, leads off discussions in the Computer System Technology area with "Innovations in System Architecture"; and "The Applications Programmer of the Future," delivered by Prof Frederick B. Thompson, California Institute of Technology, focuses interest on the Computer Applications area.

Great Debates scheduled for Wednesday afternoon and Thursday evening focus on Centralized vs Distributed Processing, and on The Limits of Software Reliability.

In the mainstream of the Technical Program, sessions on *Microcomputers* relate details of single-chip processor design and give specifics of the Z80 microprocessor system design; also discussed are federated microprocessor systems, medium-sized systems constructed from multiple computers, and centralized computing. A panel discussion presents viewpoints of manufacturer, designer, and user on the microcomputer development process and available design aids.

Those more interested in *software* can attend a session dealing with specification analysis and validation of software requirements, which will review the techniques available and present both prime and subcontractors' views on validation requirements. Software design for hardware interaction of real-time systems and data state design are considered in "Software Design Methodology." A macro-estimating methodology for ADP resource estimating, and the development of a software cost methodology are scrutinized during "Software Cost Estimating and Sizing." "Software Visibility and Control" will consist of papers relating how software development on the Viking-Mars program was controlled; describing a software development facility for mini and microcomputers; and introducing a high level human/machine interface language processor for interactive information retrieval.

The series dealing with *Computer System Technology* will be led off by "Innovation in System Architecture," with an analysis of queueing models for multiprocessor systems, and details of virtual machine research on the Honeywell 6000. "Practical Applications of Performance Evaluation" features papers dealing with hierarchies of models and predicting time-sharing performance.

Modular structures for protocols, design requirements for practical general-purpose multiprocessors, and a case study of DFMP are topics to be discussed during one session on Distributed Systems and Networks; problem partitioning in distributed systems is taken up in another session which focuses on partitioning in time and space, partitioning of workloads, and measurement of parallel programs on a multi-mini system.

Sessions devoted to *Components and Technology* highlight bipolar and MOS components, and semiconductor and solid-state memories. Highlights of the session on bipolar technology include an overview of semiconductor technology trends, and a review of advances in IIL technology. The MOS-related session contains a paper on state-of-the-art high speed n-channel MOS technology, and the development of nonvolatile MNOS memory. Applicability of semiconductor memories to use as add-on memory and in high performance computer applications as well as in microcomputers are subjects of "State-of-the-Art Semiconductor Memory Technology." Magnetic bubbles, CCD, and electron beam-addressable memory technologies are reviewed during a session which attempts to detect trends that may appear in solid-state memory technology. □

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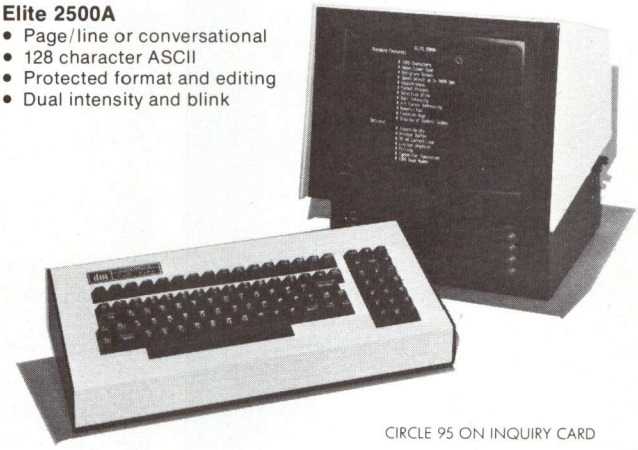

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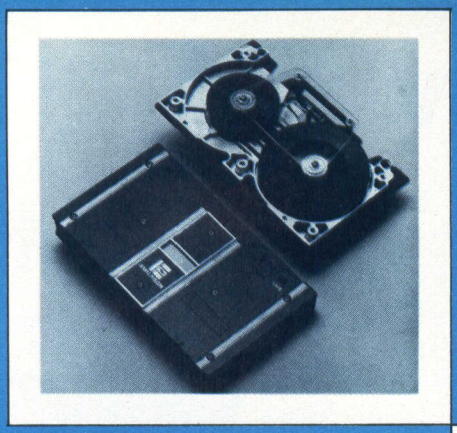

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Contrary to some reports, the 8080 is quite powerful, requiring only appropriate programming to serve many applications; some useful programming hints that are not obvious are described here

Programming Hints Ease Use of Familiar Microprocessor

Bruce Gladstone and Paul D. Page

Microkit, Incorporated
Santa Monica, California

Although many programmers feel that the Intel 8080 microprocessor and compatible devices from other sources lack some capabilities they have been accustomed to, the 8080 is more than adequate in most microcomputer applications. Programming techniques are available and can be applied to make it look more like conventional minicomputers. These techniques will have to be applied more and more, because the decision as to which processor to buy is usually made on the basis of the suppliers' competence, price of the part, availability of peripheral chips, and other non-architectural considerations. On this basis, many large manufacturers have selected it for use, and five vendors are supplying equivalent parts. Thus the 8080 seems about to become an industry standard microprocessor; with this status, innovative programming acquires new importance.

One of the most frequently voiced criticisms of the 8080 is that it lacks an indirect addressing mode. An indirect address appears as part of an instruction, and specifies the location of the address of the operand to be used with that instruction, as opposed to the location of the operand (a direct address) or the operand itself (an immediate address). Significant advantages are to be gained with indirect addressing in certain applications, such as calculation of addresses as the program runs and thus their specification as a result of program execution. This allows a series of processes to use the same block of program code, eases the processing of lists or tables of data, and extends the on-chip registers for addressing purposes.

The 8080 has a rather generous complement of on-chip index registers, for such double-addressing processes as moving a block of data from one memory space to another. An extension of the registers would be useful, for example, where each of many buffers in memory is being filled by a different input device (Fig. 1). A series of pointers (indirect addresses) in memory would be most helpful in keeping track of the buffer locations for the next entries, even at the cost of a small reduction in processing speed—provided, of course, the system has adequate read/write memory for the pointers.

Indirect addressing capability for five classes of instructions can be provided in the 8080 at a small expense in speed and memory space (Table 1). All instruction sequences are quite short, so that execution times are not seriously lengthened. All sequences rest on the use of the LHLD instruction—Load the H and L registers Direct—which was not in the predecessor 8008 microprocessor. In both 8008 and 8080 the H and L registers are the preferred locations for memory address pointers; with the LHLD instruction, the programmer can load H and L registers from a pair of memory locations. If these locations are in read/write memory they can be an indirect address source.

Once that indirect address is in the H and L registers, a variety of instructions can use it. For example, PCHL puts the contents of H and L registers into the program counter; thus if LHLD is followed by PCHL, the program executes an indirect jump. The LHLD instruction transfers the indirect address from memory,

TABLE 1

Indirect Addressing

Function	Instruction Sequence	Execution Time (μs)	Memory Required
JMP @ ADDR	LHLD ADDR PCHL	8 2.5 10.5	6 bytes
CALL @ ADDR	LHLD ADDR CALL VECTOR . . . VECTOR PCHL	8 8.5 2.5 19	9 bytes
LDr @ ADDR	LHLD ADDR MOV r, M	8 3.5 11.5	6 bytes
STr @ ADDR	LHLD ADDR MOV M, r	8 3.5 11.5	6 bytes
OPR @ ADDR	LHLD ADDR OPR M	8 3.5 11.5	6 bytes
LDr @ ADDR(B)	LHLD ADDR DAD B MOV r, M	8 5 2.5 15.5	7 bytes

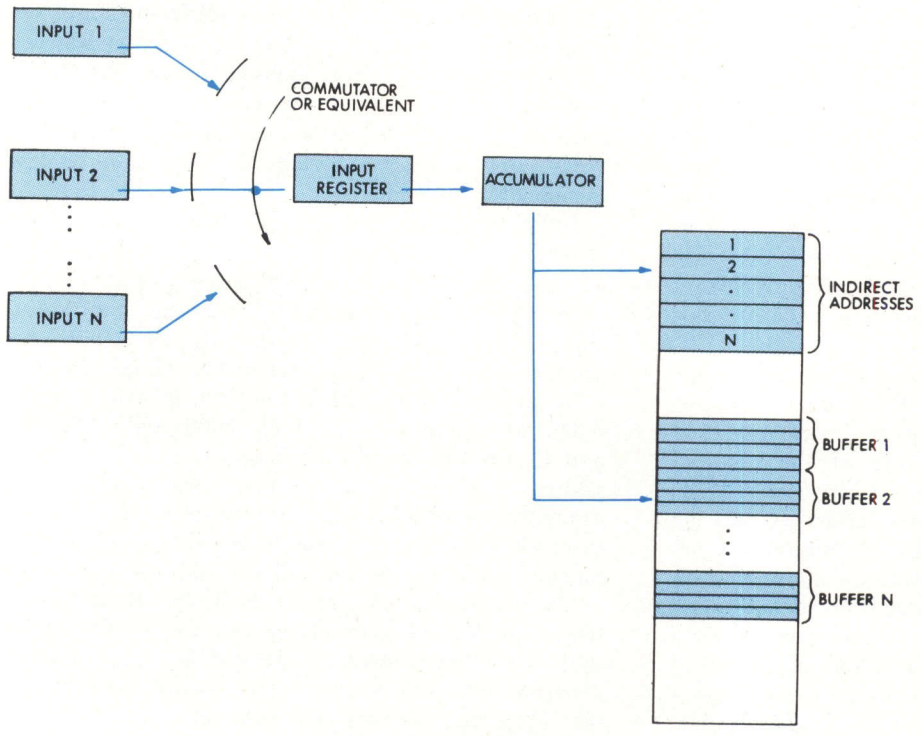

Fig. 1 Indirect addressing. Input devices 1 through N put data into their respective input buffers. Each buffer's address is stored at an indirect address for that input; the indirect address serves as a pointer into the buffer. After each word is received, the indirect address is incremented to point to the next free location in the buffer. One program serves all inputs

into the H and L registers; PCHL then transfers that address from the H and L registers into the program counter, thus forcing a jump to the indirect address location.

The indirect CALL is slightly more complicated. Ordinarily the CALL instruction jumps to a subroutine, automatically storing a return address in the microprocessor's last-in first-out stack so that the main routine can be resumed after the subroutine execution is complete. The last instruction in the subroutine fetches this return address. For an indirect CALL, again the indirect address is loaded with the LHLD instruction. A CALL is made to a routine (VECTOR in Table 1) that contains only the single instruction PCHL. The CALL stores the return address on the stack and PCHL performs the indirect jump.

LOAD and STORE indirect are very straightforward. As before, LHLD loads the indirect address, and the move instructions transfer the contents between memory and the specified register.

Finally, indirect instructions can include all of the arithmetic and logical operators (add, add with carry, subtract, subtract with borrow, AND, OR, exclusive OR, compare, increment, and decrement). In the Table, the instruction OPR stands for any one of these operations. Operand M is an address specified by the H and L registers.

Indirect addressing with indexing is useful where the indirect address contains a pointer to a table and an index register contains an offset in that table. In the example (last line of Table 1), another pair of scratchpad registers, the B and C registers, contains the index. The sequence of instructions loads the H and L registers with the indirect address (LHLD ADDR), then adds the B and C registers as a single quantity to the H and L registers, leaving the result in the H and L registers (DAD is a double-precision add). Thus, the M in the MOV r, M instruction now refers to ADDR + B. Obviously, this indexing technique can be applied to all other instruction forms listed in Table 1.

Logical Instructions

Among the powerful features of the 8080 is its complement of logical instructions: OR, exclusive OR, and AND. These instructions are ordinarily used in conjunction with one of the scratchpad registers, the operand of an immediate instruction, or a word in memory (Fig. 2): ORA to set accumulator bits, ANA to clear bits, and XRA to complement bits. Wherever the specified register, r, contains a 1, ORA r places a 1 in the corresponding position in the accumulator; where the specified register contains a 0, the accumulator contents are undisturbed. Conversely, where the specified register contains a 0, ANA r places a 0 in the accumulator, and leaves it undisturbed for each 1. Finally, an XRA r complements the accumulator bits wherever the specified register contains a 1. ORI, ANI, and XRI are corresponding immediate instructions.

However, when the register specified is itself the accumulator, so that the logical step is performed by an operand upon itself, other useful results are obtained. Instruction XRA A clears the accumulator and the carry, sign, and zero flags, which warn of conditions arising from a certain preceding operation; while ORA A is the general flag-setting instruction (except carry, which it clears). It does not disturb the contents of the accumulator, but sets flags based on those contents.

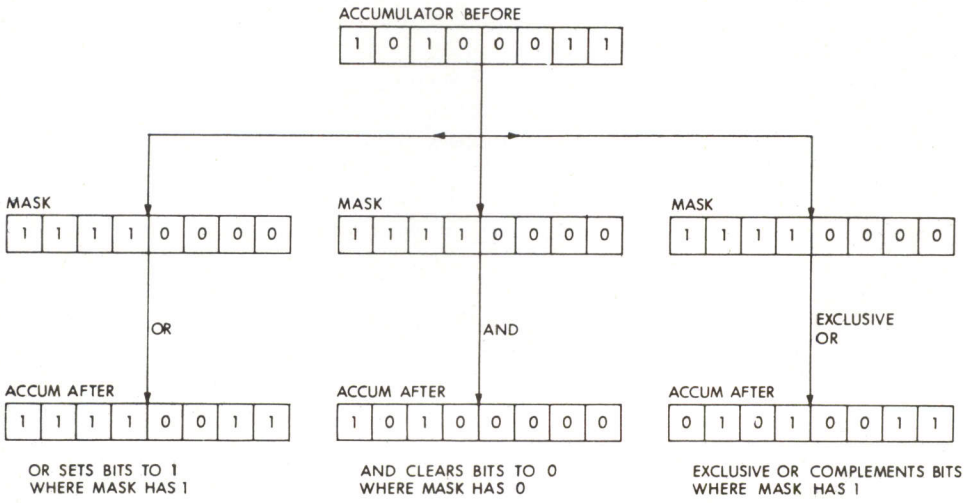

Fig. 2 Bit manipulation. Logical instructions OR, AND, and exclusive-OR set and clear bits in the accumulator in accordance with the mask, which is the operand of the instruction. Operand can be immediate, register, or indirect (part of the instruction, in a register, or addressed by the contents of the H and L registers, respectively)

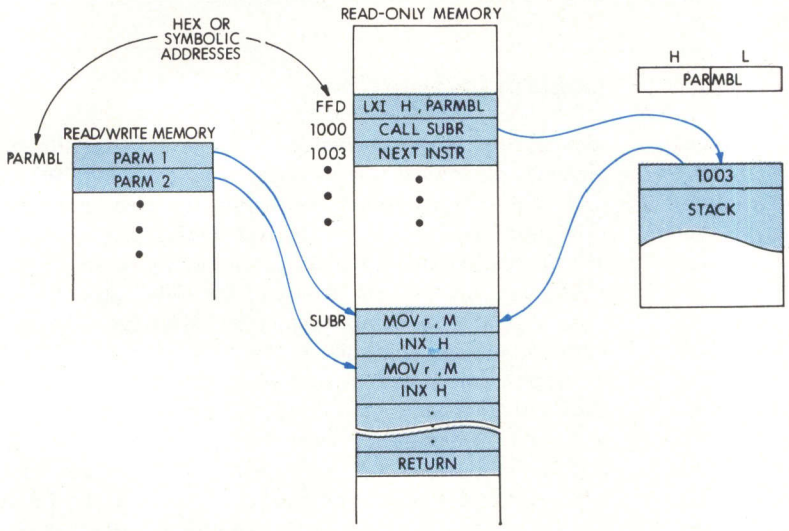

Fig. 3 Parameter passing via common area. When program and subroutine are in read-only memory, parameters in general are not; however, they must be accessible by the read-only subroutine. Scratchpad registers in main memory are useful for this purpose

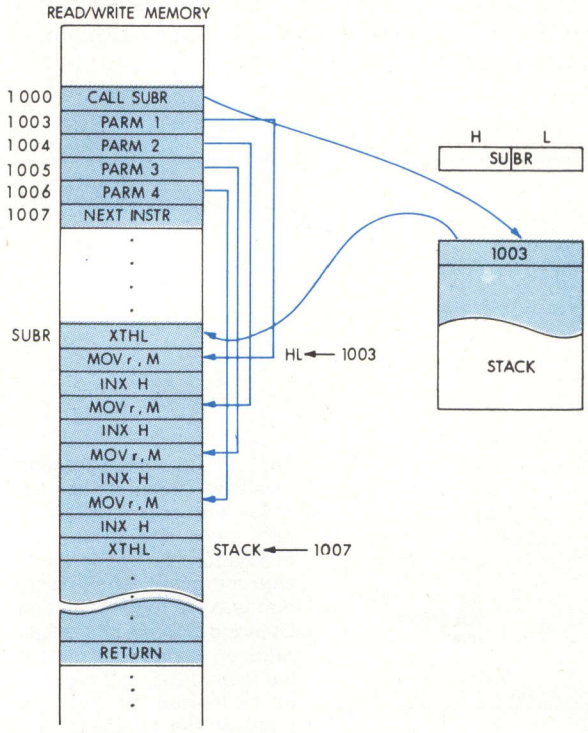

Fig. 4 Parameter passing via local area. When program and subroutine are in read/write memory, parameters can follow subroutine call. They are then addressed by exchanging the words at the top of the stack with the contents of two scratchpad registers

Subroutines and Parameter Passing

Memory implementation affects a program's method of passing parameters to a subroutine. Frequently in microcomputer applications, program memory is in a read-only memory, masked or programmable, and data memory is in a read/write memory. Thus, in general, parameters passed to a subroutine are put in a common area in read/write memory (Fig. 3). This technique calls for a load immediate (LXI), which puts the address of this common area into the H and L registers (LXI H, PARMBL), and calls the subroutine. The CALL stores the return address in the stack and jumps to the beginning of the subroutine. Information about the storage location of the parameters is available to the subroutine because the H and L registers were preset to point at the common area (PARMBL).

In an increasing number of cases, both program and data are in read/write memory, as a result of the low cost of this memory and the availability of high speed nonvolatible storage such as floppy discs and cassette recorders. In such applications another technique may be desirable to pass parameters to and from a subroutine; the program carries its parameters along with it. In this technique there is less opportunity for errors where two programmers' common areas interfere with one another. An individual programmer can be responsible for a section of a program, and has to manage both his program area and his data area. It is fairly easy for him to work in the space between two given addresses, when he must figure out how to fit both program and data into that space. It is a little more difficult to work in one block for program and another block, usually much smaller, for parameter storage.

Thus the availability of all read/write memory permits a more minicomputer-like method for passing parameters to a subroutine (Fig. 4). All parameters to be passed to the subroutine are stored immediately after the CALL instruction. When the CALL is executed, the return address, which points to the first parameter, is put on the stack. The first instruction in the subroutine is an XTHL instruction, which exchanges the first byte in the stack with the H and L registers. This puts the address of the first parameter into the H and L registers, which point to the parameter table. Each time a parameter is fetched, the H and L registers are incremented to point to the next parameter. In the figure, these fetches are consecutive; but they need not be, if intervening instructions do not affect the H and L registers. Finally, after the last parameter has been passed to the subroutine, the H and L registers are incremented once more, followed by another XTHL instruction. This puts back into the stack the address of the next instruction in the main program. It also restores the contents of H and L before the call, but this is probably no longer significant. Later at the end of the subroutine, the RETURN instruction picks up the value at the top of the stack and jumps to the instruction following the parameters, resuming the main program.

16-Bit Instructions

Still another architecture-associated feature relates to the problem of 8- and 16-bit microcomputers. In many applications a 16-bit microcomputer is very valuable. Although the 8080 is itself an 8-bit unit, its instruction set includes a series of instructions (Table 2) that allows it to look like a 16-bit microcomputer. Some of these are not obvious.

A 16-bit microcomputer is particularly valuable in data acquisition. Data are acquired from analog transducers through analog-to-digital converters (ADCs), which typically are precise to within 10 to 12 bits (0.1 to 0.025%). Users, having purchased this precision at significant cost, would not be wise to use only eight bits of it in the microcomputer. Likewise, pulling in the data eight bits at a time and processing them in that form is painful. Thus 16-bit instructions are very valuable.

A digression into organization of input and output (I/O) structures is appropriate here. Some manufacturers advertise that their microcomputers treat I/O as part of memory and that this simplifies design of I/O structures. Obviously this is quite possible with the 8080—and, as a matter of fact, with any micro- or minicomputer, whether or not it has special I/O instructions. In fact, many of the simpler 8080 systems do exactly this. They require only that the I/O device registers recognize main memory addresses and perform load and store operations when these addresses are activated.

This ability to make I/O registers part of main memory address space allows the use of the first two 16-bit instructions. One of these is Load H and L Direct (LHLD), previously encountered in connection with indirect addressing; the other is its dual, Store H and L Direct (SHLD). The "direct" part of these instructions refers to memory addresses; but if the addresses are actually I/O registers, the LHLD instruction can read up to 16 bits from an ADC, while the SHLD instruction can put out up to 16 bits to a digital-to-analog converter (DAC). Thus, with very little programming pain, the 8080 can be turned into a 16-bit I/O machine. Actual transfers, to and from the I/O devices, occur eight bits at a time, but from the programmer's viewpoint the transfer is 16 bits.

Further, a series of instructions, including double-precision adds, increments, and decrements, allows the programmer to do some 16-bit arithmetic. For example, to generate an analog output function, approximated by a series of ramps, the INX H and DCX H instructions can increment and decrement the H and L registers at fixed time intervals. Following this the SHLD instruction transfers the new value from the H and L registers to the DAC, the output of which is a linear ramp. For less than 16-bit precision, some bits in the 8080 will be unused.

Some 16-bit arithmetic can be performed with double-precision adds between H and L registers, containing

TABLE 2

8080 16-Bit Instructions

Instruction	16-Bit Function	Execution Time (μs)
LHLD INPUT	Input	8
SHLD OUTPUT	Output	8
LHLD MEMORY	Load	5
SHLD MEMORY	Store	5
DAD H	Left Shift	5
DAD B	Add	5
DAD D		
DAD SP		
INX H	Increment	2.5
INX D		
INX B		
INX SP		
DCX H	Decrement	2.5
DCX D		
DCX B		
DCX SP		
PUSH B	Stack Operations	5
PUSH D		
PUSH H		
POP B		
POP D		
POP H		
XTHL	Exchange	9
XCHG		2
SPHL	Register Transfer	2.5
PCHL	Jump Indirect	2.5

TABLE 3

Jump Table Linking

```
                Equivalences
A  JTBL   EQU X'50'          Jump table
   SUBR1  EQU JTBL           equivalences,
   SUBR2  EQU JTBL+3         assemble with
   SUBR3  EQU JTBL+6         each module
            .
            .
            .
   SUBRN  EQU JTBL+3(N-1)
                Module 1
C           ORG X'106'
            .
            .
            .
            CALL SUBR3       Calls a subroutine
            .                that is part of
            .                Module N
            .
A  JTBL    EQU X'50'
   SUBR1   EQU JTBL
            .
            .
            .
            END ENTRY1
                Module N
D           ORG X'1000'
            .
            .
            .
            _____
   SUBR3L   _____            Actual location of
            _____            subroutine in
            _____            Module N
            .
            .
            .
A  JTBL    EQU X'50'
   SUBR1   EQU JTBL
   SUBR2   EQU JTBL+3
            .
            .
            .
B           ORG SUBR3        This builds the jump
            JMP SUBR3L       to SUBR3L in the
            END ENTRYN       jump table
```

addend and sum, and D and E or B and C registers, containing the augend. The instruction DAD H also provides a left shift of all 16 bits by one bit position. It adds the contents of H and L to itself; doubling is equivalent to the left shift.

While doing these 16-bit conversions, LHLD and SHLD still work with real memory addresses, doing 16-bit loads and stores.

Jump Tables and Module Linkage

Finally, one last programming technique, although it is not closely associated to the 8080's architecture, is useful because it relates to how programs are written. Generally a good technique is to write programs in modules, which are individually written and tested and then brought together. However, a frequent

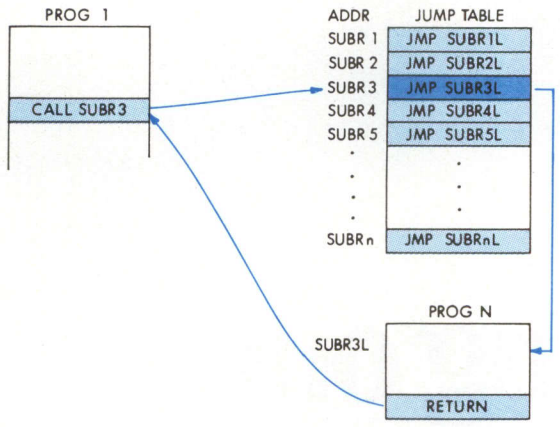

Fig. 5 Jump table. When programs and subroutines are in different modules subject to independent modification, jump table offers a convenient way to keep track of their changing locations

problem is providing linkages between the program's various modules. For instance, suppose module 3 calls a subroutine in module 7. Each time module 7 is modified, the location of this subroutine is likely to change, making it necessary to change module 3 each time module 7 changes. Obviously, for a program made up of a reasonable number of modules, a great deal of time is spent continually updating the linkages as individual modules are modified.

Jump tables offer one easy way around this difficulty (Fig. 5). For example, suppose program 1 wants to make use of the subroutine SUBR3 in program N. Linkage between program 1 and the subroutine in program N is made through the jump table, which contains starting addresses of all the subroutines that the program uses.

To organize the table, at the outset of program design, the programmer divides the problem into a series of modules, and decides which module will have which utility subroutines. Subroutines need not all be in one module. The programmer assigns a name and a jump table address to each routine. The jump table is in a fixed area; in the 8080, a good place is in low memory, somewhere around address 50 (hexadecimal notation) right after the area reserved for use by the RESTART instructions. Since the length of each JUMP instruction is fixed at three bytes and its place in the table has been preassigned, its address will not change. Thus, each CALL from any program is to a fixed location in the jump table.

When any module is coded and ready for assembly or reassembly, it must include a list of jump table entries that it refers to (A in Table 3) and correct references to subroutines which it includes (B in Table 3). These must be assembled along with the straight coding in the modules (C and D). Pseudoinstructions ORG and EQU are useful for this purpose. ORG defines a specific address at which the assembler must begin assigning locations as it translates the program; EQU equates one symbolic address with another or with a numeric address. In Table 3 the jump table begins at 50, as suggested earlier; since a JUMP instruction in the 8080 occupies three bytes, successive entries in the jump table must be at 53, 56, 59, and so on. Modules call subroutines by names that correspond to jump table entries. With each module is a group of EQU instructions which assign real addresses to the subroutines *called by* that module. Collectively these real addresses make up the section shown as A in the listing; this section never changes. There is also an ORG for each subroutine *contained in* that module, placing in the table a jump to the subroutine (shown as B in the listing); this can change every time the module is modified.

All that is necessary to link the modules is to load them one after another in any order into the system, each one bringing in its part of the jump table and automatically putting it together. The only unusual facility that is necessary is the ability to load discontinuous parts of memory.

This technique automatically maintains linkages. The same technique can provide linkages to data areas and buffers. Ordinarily, during the debugging phase, modules must be assigned fixed areas in memory, and must not expand outside these areas. However, when debugging is complete, all modules can be reassembled to compact the program.

The 8080, whatever its shortcomings may be, has more than enough power to solve a great many problems as long as the full power of its instruction set is recognized. Obviously, this is not an exhaustive listing of all the programming techniques possible with the 8080; however it does at least represent a partial answer to some objections that have been raised.

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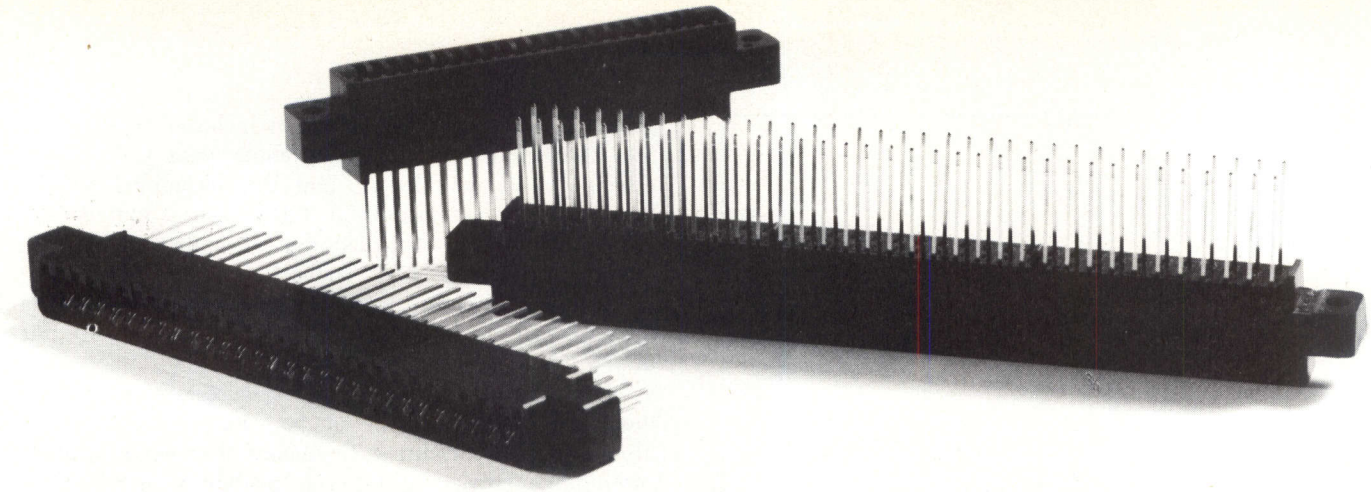

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High performance in magnetic media demands much from conventional encoding methods, but each method has its own disadvantages; yet a simple encoding technique for mass storage has a number of attractive characteristics distinctly its own

New Method for Magnetic Encoding Combines Advantages of Older Techniques

Arvind M. Patel

General Products Division
IBM Corporation
San Jose, California

A unique method of magnetic recording combines two advantages not both found in previous methods—absence of a dc component in the signal read from tape, and maintenance of a high recording efficiency on the tape itself. In addition, the method retains principal advantages of previous methods in that it is self-clocking for any pattern of recorded data and is not seriously affected by baseline or peak shift in the read-back signal.

Called zero modulation or ZM, the method is used in the IBM 3850 Mass Storage System (see box at right). This machine reads and writes on a magnetic surface with a rotating read/write head. Rotation requires transformer coupling, which cannot handle a dc component; therefore an encoding method that imposes neither a dc component nor the disadvantages of other techniques is required. ZM is a significant improvement over earlier encoding methods, some of which merely assigned transitions of magnetic polarity to bits in some more or less straightforward way and often achieved a new advantage at the expense of an old one. These methods included non-return-to-zero inverted (NRZI), phase encoding (PE), group-coded recording (GCR), frequency modulation (FM), and modified frequency modulation (MFM), sometimes called delay modulation. Zero modulation uses sophisticated coding of data to match idiosyncracies of the magnetic recording channel with waveform properties of the recorded signal.

Importance of efficiency and the absent dc component is brought out when ZM is compared with some earlier codes. NRZI, for example, is the simplest en-

Honeycomb Storage

The IBM 3850 is a mass storage system that serves as a virtual storage medium supporting magnetic disc files, in much the same way as the discs serve as virtual storage supporting main memory. It consists of an array of data cartridges about 2 in. in diameter and 4 in. long with a capacity of 50 million characters each. Although the cartridge contains a length of magnetic tape, stored data are organized in cylinders analogous to those of a disc file, and can be transferred to the disc file a cylinder at a time—that is, without moving the disc read/write heads during the transfer. Up to 4720 cartridges are stored in hexagonal compartments in a honeycomb-like apparatus that includes a mechanism for fetching cartridges from the compartments, reading or writing data on them, and replacing them.

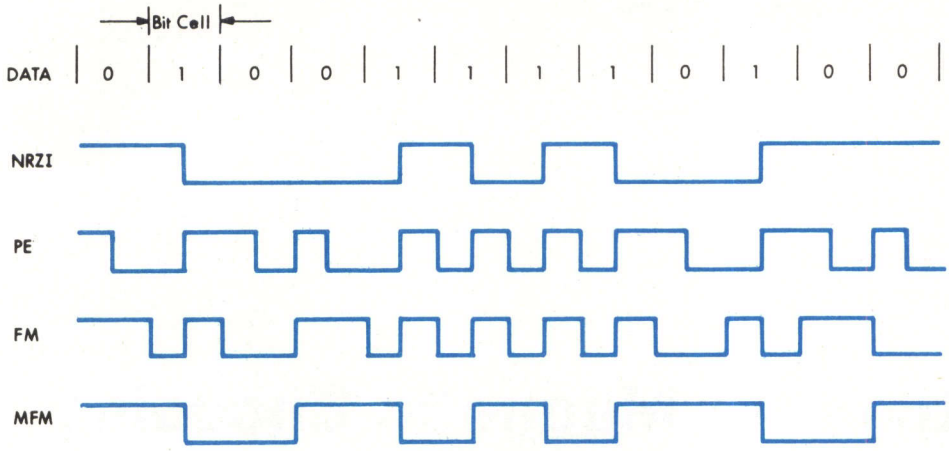


Fig. 1 Conventional waveforms. NRZI is the simplest waveform, but requires a wideband amplifier for processing, since it has a substantial dc component. This and other difficulties are overcome with PE and FM encoding, at the cost of high transition density—up to two transitions per bit. Variations on FM reduce number of transitions, but reintroduce the dc component

coding method, used on ½-in. wide magnetic tape at data recording densities up to 800 bits/in.[1] Presence or absence of a transition in the NRZI magnetic waveform corresponds to 1 or 0 respectively in the binary data stream (Fig. 1); successive magnetic transitions, which alternate in polarity, produce alternately positive and negative electric pulses in the readback signal, nominally symmetric about a base line. Principal drawback of NRZI is that long strings of 0s are recorded as correspondingly long periods with no magnetic transitions, and hence no pulses in the readback signal; the read clock can lose synchronization during those periods. Furthermore, wideband circuits with dc response are required for signal processing and data detection.

NRZI is also subject to a more subtle difficulty: baseline and peak shift, alluded to previously. At high densities, the readback pulses produced by a string of consecutive 1s tend to interfere with one another. When such a string of 1s is preceded or followed by a string of consecutive 0s, this interference is asymmetrical, causing the first or last few pulses to have larger amplitudes; thus the base line appears to drift. A similar shift can arise from a string of consecutive 0s if the dc response of the electronic circuitry is slightly off specification. Interference also causes the pulses to seem to slide into the signal-free zone occupied by the 0s, creating a displacement in time of the pulse peaks. This peak shift can be a significant fraction of the nominal time between bits.

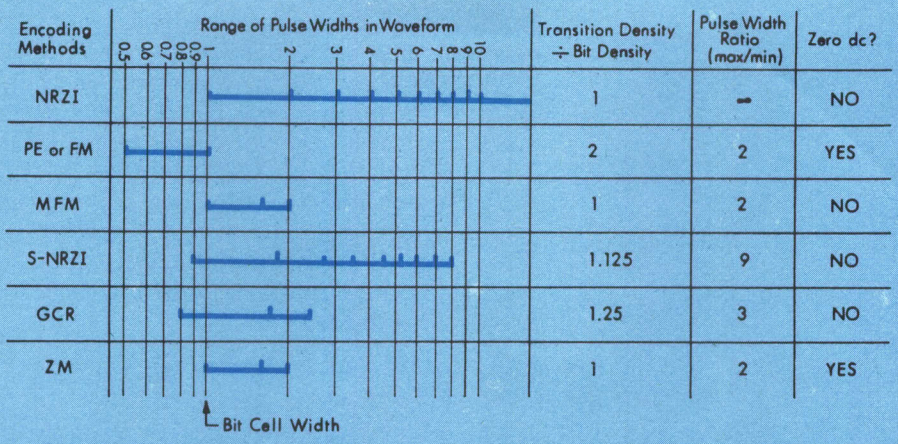
Phase encoding (PE)[2] was devised to alleviate these problems, and is used on ½-in. tapes recorded at 1600 bits/in. In PE a 1 corresponds to an up-going transition and a 0 to a down-going transition at the center of the bit cell. Where two or more 1s or 0s occur in succession, extra transitions are inserted at the bit-cell boundaries. Resulting waveform is self-clocking and has no dc component, since the waveform in each bit cell has up (positive) and down (negative) signal levels of equal duration. However, PE requires twice the transition density of the NRZI method for a random data pattern. Thus recording efficiency is poor.

Frequency modulation has transitions at every bit-cell boundary. However, although FM is similar to PE in all waveform properties, the 1 and 0 correspond to a presence or absence, respectively, of any transition at the center of the corresponding bit cell, rather than to an up or down transition. In the IBM 3330 disc file FM has been supplanted by MFM, or delay modulation, which provides enough clocking transitions without doubling the transition density.[3] In MFM (as in FM) a 1 and a 0 correspond to the presence or absence, respectively, of a transition in the center of the corresponding bit cell. However, additional transitions at the cell boundaries occur only between bit cells that contain consecutive 0s. This method retains an adequate minimum rate of transitions for clock synchronization without exceeding the maximum transition density of NRZI, but at the cost of a more complex data detection process. An additional disadvantage is the dc component, with indefinitely large accumulated dc charge for some data patterns such as 0110110110 . . . .

Modified forms of NRZI include synchronized NRZI (S-NRZI), and group-coded recording (GCR) used to record magnetic tape at 6250 bits/in.[4] In these methods, the data stream is precoded by adding bits to break up long strings of 0s. In S-NRZI, a 1 extends each 8-bit group to nine bits and establishes a synchronization transition. In GCR, each 4-bit group is mapped into five bits using a fixed assignment that guarantees that the coded data stream never contains more than two consecutive 0s. Detection process for both methods is the same as for NRZI, but maximum transition density is necessarily higher, and the dc component can be quite prominent.

TABLE 1

Encoding Methods: Parameters



Advantages of ZM

Zero modulation encoding produces waveforms that closely match characteristics of the magnetic recording channel. Among these characteristics (Table 1) are:

Minimum energy at low frequencies—achieved because the long-term dc component is 0, and maximum accumulated unbalance between positive and negative pulse durations of the waveform is small. This helps alleviate base-line shift of high density read signals.

Narrow bandwidth—conserved by constraining pulse width and ratio of maximum to minimum pulse width. This helps reduce the problem of peak shift. Resulting read signal amplitude is relatively uniform—that is, it has a small dynamic range for any kind of data stream.

Adequate transition rate—as a consequence of the constraint on the maximum pulse width, a clock signal can be derived from the transition rate.

High efficiency—ratio of highest transition density to bit density is close to 1. With NRZI and MFM the ratio is exactly 1, and with other codes it is fractionally higher, rising to 2 for PE and FM.

Reliable Error Checking—as a consequence of these characteristics and various other constraints of the method, the code structure of ZM is such that error checking is easy and reliable.

Zero Modulation Algorithm

The ZM algorithm can be readily implemented by a practicing engineer with the information that follows. Theoretical details and proofs have been published elsewhere.[5] The ZM algorithm maps every data bit sequentially into two binary digits in such a way that any two consecutive 1s are separated by at least one and at the most three 0s. This sequence is recorded in NRZI. Consequently, the narrowest pulse in the ZM waveform spans two digits in the coded sequence, and this is the width of the data-bit cell. Similarly the widest pulse spans four digits, which is twice the narrowest pulse width. The resulting waveform is similar to that of MFM.

This limited range of pulse widths corresponds to a narrow bandwidth for the waveform, and the narrow bandwidth has obvious electronic advantages. Short "pieces" of the waveform of one polarity are always balanced very soon by equally short pieces of the waveform with the opposite sign. Two such sections taken together make up a section with a zero dc component, and the waveform made up of such balanced sections contains minimal energy at low frequencies.

A quick way to estimate the amount of dc in a train of rectangular pulses representing data encoded in ZM or any other code is to count positive- and negative-going excursions, giving a value of ± 1 to the narrowest pulses, ± 2 to pulses twice as wide, and so on. This corresponds to integrating the waveform mathematically, or collecting charge on a capacitor fed by a current with the given waveform. If the total strays far from 0, the dc component is present. Under the zero modulation algorithm, the total changes sign frequently and never exceeds ± 3, corresponding to the limit of three 0s between any pair of 1s.

Two-for-one mapping is a nonlinear function of the preceding and following data sequences and requires an encoder with memory. In a practical implementation, amount of memory can be limited as desired by adding a small amount of redundancy. In its functional form, however, the ZM algorithm, in general, requires unlimited memory.

The algorithm can be described in terms of a data bit to be encoded, one preceding and one following data bit, and the two coded digits corresponding to the preceding data bit; and in terms of two parity functions that look ahead and back relative to the

TABLE 2

Encoding and Decoding Algorithms

ENCODING ALGORITHM

$d_0 \rightarrow a_0 b_0$	CONDITION
$0 \rightarrow 10$	$d_{-1} = 0$
$0 \rightarrow 10$	$d_{-1} = 1$ and $a_{-1}b_{-1} = 00$
$0 \rightarrow 00$	$d_{-1} = 1$ and $a_{-1}b_{-1} \neq 00$
$1 \rightarrow 10$	$d_{-1} = 0$ and $P(A) = 0$ and $P(B) = 1$
$1 \rightarrow 10$	$d_{-1} = 1$ and $a_{-1}b_{-1} = 00$
$1 \rightarrow 00$	$d_{-1} = 1$ and $a_{-1}b_{-1} = 10$
$1 \rightarrow 01$	otherwise

$$a_0 = \bar{d}_0\bar{d}_{-1} + d_0\bar{d}_{-1}\,\overline{P(A)}\,P(B) + d_{-1}\bar{a}_{-1}\bar{b}_{-1}$$
$$b_0 = d_0[P(A)\,\bar{d}_{-1} + \overline{P(B)} + b_{-1}]$$

DECODING ALGORITHM

$a_0b_0 \rightarrow d_0$	CONDITION
$10 \rightarrow 1$	$a_{+1}b_{+1} = 00$
$10 \rightarrow 0$	$a_{+1}b_{+1} \neq 00$
$00 \rightarrow 1$	$a_{-1}b_{-1} = 10$
$00 \rightarrow 0$	$a_{-1}b_{-1} \neq 10$
$01 \rightarrow 1$	none

$$d_0 = b_0 + a_0\bar{a}_1\bar{b}_{+1} + \bar{a}_0a_{-1}\bar{b}_{-1}$$

bit being encoded. Look-ahead parity, P(A), is the count modulo 2 of 1s in the data stream beginning with the data bit being encoded and counting forward to the next 0 bit; look-back parity, P(B), is the count modulo 2 of all 0s in the data stream from its beginning up to the present bit. For example, in the data sequence 01011110, P(A) = 1 at the second, fifth, and seventh bits from the left, P(A) = 0 at all 0 bits and all the other 1 bits; while P(B) = 1 at the first, second, and eighth bits and 0 elsewhere.

These rules can be translated into encoding and decoding functions expressed either in the form of tables or as equations (Table 2). In both, the symbol d represents a data bit; a and b, coded digits; and subscripts −1, 0, and +1, preceding, current, and following bits, respectively. For convenience, the nonexistent bit preceding the first data bit is assumed to be 1 and its look-back parity is 0; the nonexistent bit following the last bit is 0.

The example (Fig. 2) illustrates the relationships among the various parameters of the data sequence and the corresponding ZM waveforms.

Although the ZM waveform looks similar to the MFM, or delay modulation, waveform, the important difference is that the MFM waveform contains a dc component, and the accumulated charge often increases indefinitely, whereas the maximum accumulated charge in the ZM waveform is ±3 units.

ZM Algorithm With Limited Memory

Look-back parity is accumulated from the number of 0s simply by updating a 1-bit storage cell as data bits are encoded. However, look-ahead parity depends on the length of a string of 1s in the following data sequence. Since the algorithm imposes no limit on the length of this string, memory requirement for computation of P(A), in general, is unlimited. However, a variant of the basic ZM algorithm limits the memory requirement to any specified number of bits.

When accumulated look-back parity P(B) = 0, encoding functions become independent of the look-ahead sequence:

$$\left.\begin{aligned} a_0 &= \bar{d}_0\bar{d}_{-1} + d_{-1}\bar{a}_{-1}\bar{b}_{-1} \\ b_0 &= d_0 \end{aligned}\right\} \text{if } P(B) = 0.$$

To force P(B) to 0, a digit, P, can be inserted in a continuous data stream at fixed intervals of f bits. This insertion implies that look-ahead parity, P(A), of the sequence of 1s at the end and beginning of any section of f + 1 bits has no effect on ZM mapping in the modified data sequence. In Fig. 3, some values of P(A) are denoted by ϕ indicating a "don't care" value when P(B) = 0. The only sequences of 1s affecting the mapping, then, are those between two 0s in the same section of f + 1 digits. The longest such sequence is f − 1 digits long. Thus, the memory required to compute P(A) is f − 1 bits.

Thus, to limit the amount of memory, the ZM algorithm is given two important modifications: First, an extra P-bit with the value of P(B) at position f is inserted at the end of every section of f data

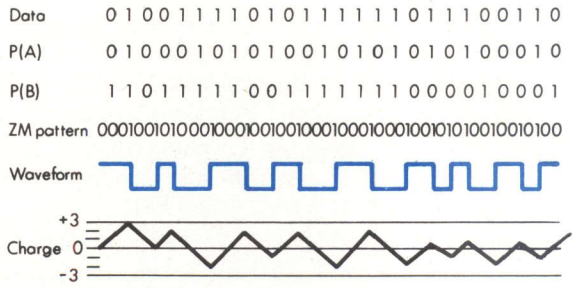


Fig. 2 Basic zero modulation. Substituting two encoded bits for each data bit on the basis of information in preceding and following bits, and recording the encoded bits in NRZI form, eliminates the dc component without other waveforms' disadvantages. However, since it places no constraints on the data pattern, it can require an infinitely large memory for implementation

bits. Second, computation of P(A) at any data bit extends only to the following f − 1 data bits, as a binary logic function of the data stored in f bits of memory:

$$P(A) = d_0\bar{d}_1 + d_0d_2\bar{d}_3 + d_0d_2d_4\bar{d}_5 + \ldots + d_0d_2d_4 \ldots d_{t-4}\bar{d}_{t-3} + d_0d_2d_4 \ldots d_{t-4}d_{t-2}$$

where t = f if f is even and t = f − 1 if f is odd. Look-back parity is merely a count of 0s as in the case for unlimited memory.

Encoding process is delayed by f bit periods in a continuous stream of data, while the memory is loaded for computing P(A), but the decoding process is delayed by only one bit period. Thus decoding errors in ZM do not propagate.

In the diagram, a value of f = 8 is assumed for illustrative purposes; but in fact, the value of f has no theoretical limits. As described later, a shift register delays each bit while look-ahead parity is generated. Small values of f require short shift registers and encode data quickly; however they add a larger proportion of redundancy in the form of the extra P-bit than do large values. Nevertheless, they may be convenient in some applications. For efficient utilization of the magnetic recording medium, large values of f—eg, 100 or more—are mandated. Although they impose substantial encoding delays, these are still negligible compared to the access time of a mass storage system, which is measured in seconds. Large values of f do not necessarily imply complex encoding logic; the look-ahead parity generator merely counts the bits as they pass, and a monolithic shift register is relatively inexpensive.

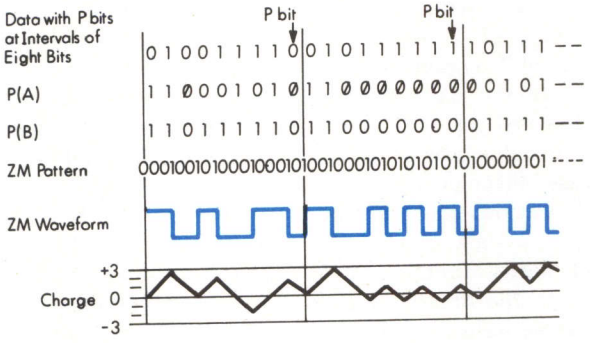


Fig. 3 Practical zero modulation. Adding an extra bit to the data stream at regular intervals in accordance with a prescribed pattern permits the two-for-one substitution of ZM to be made with a memory of realizable capacity. In the waveform, dc component is still 0, transition density is low, yet added redundancy is minor

Synchronization Signal

When reading, a ZM waveform is decoded into a data sequence with the help of a clock, which is usually derived from the waveform. A synchronizing signal of sufficient length and recognizable ending is useful in marking the beginning of data. A similar resynchronizing signal may also be inserted at predetermined intervals in the waveform, such as at ZM memory boundaries, for protection in case of temporary loss of synchronization in magnetic defects.

Several characteristics are required of the synchronization signal:

(1) It must be distinctive enough not to be confused with the normal data waveform in its original or shifted position.

(2) It must satisfy the ZM constraints of maximum and minimum pulse widths.

(3) It must have no net dc component over its length, although unlike the encoded data, the integrated total may exceed three units within itself. The accumulation may be four, five, or six units (or even more if the synchronization signal is short and infrequent).

(4) Basic synchronization signal should be reasonably short and the endings compatible with the ZM algorithm for insertion at the memory boundary without modification.

These specifications could be easily satisfied if some binary sequence were known to be inadmissible as data. However, no such sequence is possible for serial data. Alternatively, a synchronizing signal can be chosen from inadmissible sequences in ZM-coded patterns. These sequences must satisfy the ZM pulse-width constraint but may exceed the maximum charge constraint.

Among the sequences that satisfy the ZM run-length constraints, 0 0 1 0 1 0 0 0 1 0 1 0 0 0, either forward or backward, is the shortest that does not occur in any ZM pattern. Any pattern containing one of these sequences can be used as a synchronizing pattern. Two examples are:

$W_1 = 0\,1\,0\,0\,0\,1\overline{0\,0\,1\,0\,1\,0\,0\,0\,1\,0\,1\,0\,0\,0}\,1\,0\,0\,0\,1\,0\,1\,0\,0\,1$

$W_2 = 0\,1\overline{0\,0\,0\,1\,0\,1\,0\,0\,0\,1\,0\,1\,0\,0\,0}\,1$

The second of these does not satisfy specification 3. Both examples begin and end with 01, and can be padded by any number of 01 digit pairs if desired for clocking. These endings also allow the synchronization signal to be placed at the ZM memory boundary without modification.

In actual application, the synchronization pattern is placed at predetermined intervals at ZM memory boundaries. In case of synchronization loss, the clock is regenerated by the read waveform as soon as the defect or other cause has passed. With the clock running, the signal detector can produce the binary ZM pattern, but the pattern cannot be decoded until the synchronization pattern re-establishes the ZM pair relation with respect to the clock. If the clock is found to be out of synchronization, ie, one ZM digit out of step with the read signal, its complement may be used for decoding.

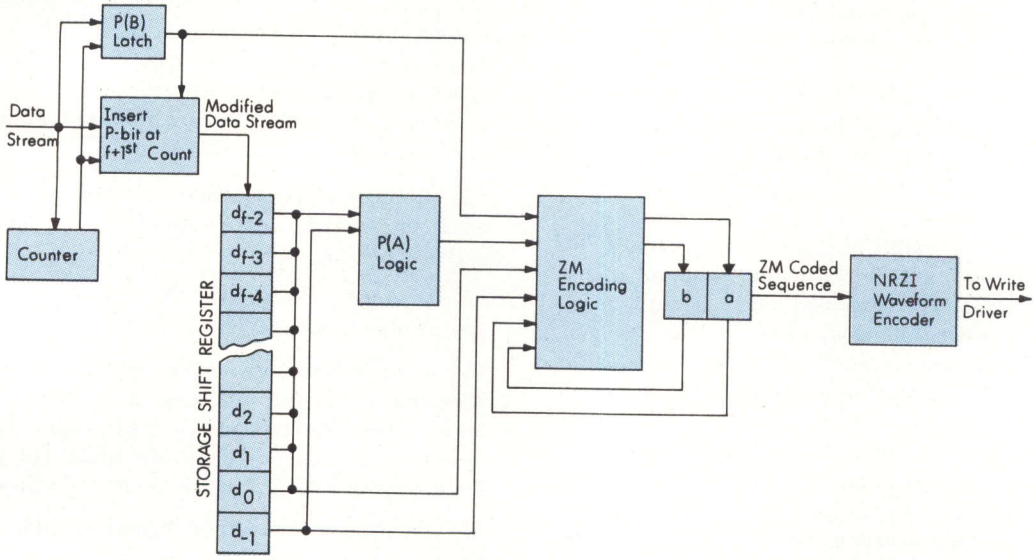


Fig. 4 ZM encoder. Principal feature is a shift register from which data bits are fed to encoding logic, which is straightforward implementation of equations in text

Error Check in ZM Patterns

Patterns of digits generated by the ZM algorithm satisfy various constraints, including parity in the case of ZM with limited memory. These constraints provide a powerful check capability for bit-detection errors and synchronization errors at the receiver.

Because error-free ZM patterns possess run lengths of one, two, or three 0s between two 1s, two consecutive 1s indicate a pick-up, or a 0 incorrectly read as 1, while four or more consecutive 0s signal a drop-out error. Acquisition of excessive dc charge can be detected with an up-down counter that increments for every code bit position recorded with a positive level, decrements likewise when the level is negative, and signals an error if the total exceeds ± 3 at any time. An alternative method of implementing this check has been worked out.[5] Finally, value of P(B) and charge value must both be 0 at the memory boundary—a simple but effective check on both synchronization and random errors. These two checks at the memory boundary are equivalent in the sense that neither detects any error missed by the other as long as the checking circuits are working properly. Error checking of ZM patterns at the receiver, an additional benefit derived from the stringent ZM constraints, need be implemented only to enhance reliability even further.

Implementation of ZM Algorithm

In a ZM encoder (Fig. 4), the first step is to modify the binary data sequence by inserting the P-bit at fixed intervals of f bits. The P-bit is the value of P(B) at count f, computed by a simple latch triggered by each 0 in the data stream. At count f + 1, the P-bit is inserted in the data stream, and the P(B)-latch and counter are reset to 0. The modified data stream passes through a shift register f bits long, which stores the previous and current data bits and the following f − 2 data bits. From these stored bits the look-ahead parity function P(A) is generated in accordance with the binary logic function given previously. From these values of P(A) and P(B), the current and next previous bits, and the just-computed ZM bits, the ZM code sequence is generated. Two feedback latches store each pair of bits of the ZM pattern as they are computed, for use in the next bit cycle. These latches are updated continually as the data bits are sequentially encoded into ZM patterns.

Initially, look-back parity is set to 0 and feedback latches are set to 01. Encoding starts after a delay of f − 1 clock periods during which the first data bits are shifted into the storage register. This puts d_o in the next to last cell of the shift register, from which it

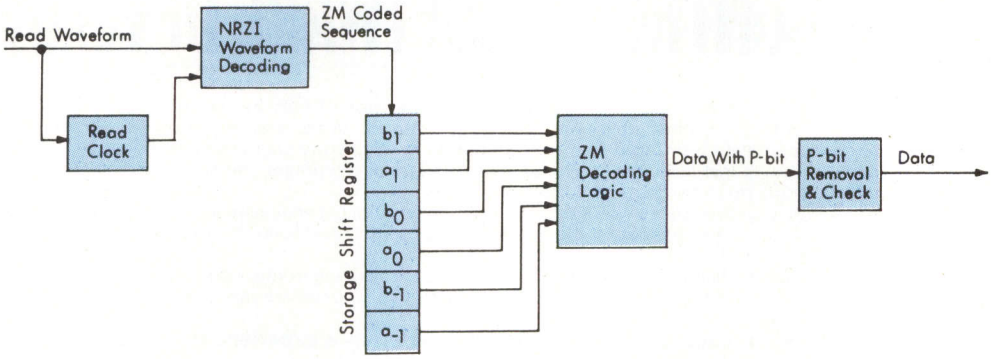


Fig. 5 ZM decoder. Data bits are defined in terms of pairs of code bits, taking into account preceding and following pair along with current pair. Hence the key element is a 6-bit shift register that shifts two bits at a time and feeds code information to decoding logic

is encoded into the first pair of code bits. The "previous" bit, assumed to be 1 and initialized accordingly, either has been inserted in the shift register just ahead of the first real data bit or can be gated to the ZM encoder during the first encoding cycle. Alternatively it can be initialized simply by placing all 1s in the shift register. This sequential encoding process is continued for the ZM coded sequence which is converted into a conventional NRZI waveform. ZM synchronization pattern, if necessary, may be inserted in the coded pattern at selected $(f + 1)$-bit boundaries.

ZM decoder (Fig. 5) converts the received waveform into a ZM pattern by means of conventional NRZI clocking and detection circuits. This ZM pattern passes sequentially through a 6-bit storage register which stores three pairs of pattern bits. As in encoding, for the first pair of bits, the "preceding" pair is set to 01. Decoding starts after the second pair arrives in the storage register. The decoder generates each data bit as a function of the preceding, current, and following bit pairs, as described previously.

Coded sequence received at the decoder satisfies all ZM constraints, and every $(f + 1)$st bit in the decoded data stream is the correct P-bit. Any departure from the constraints or an incorrect P-bit clearly indicates an error. Some or all of these checks can easily be implemented for error checking.

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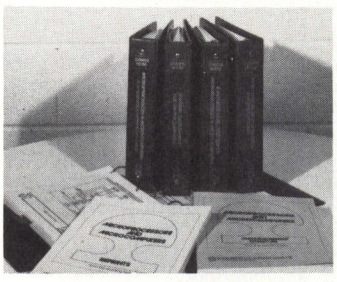

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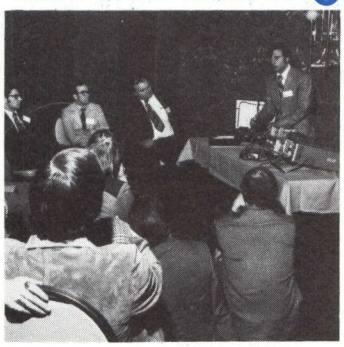

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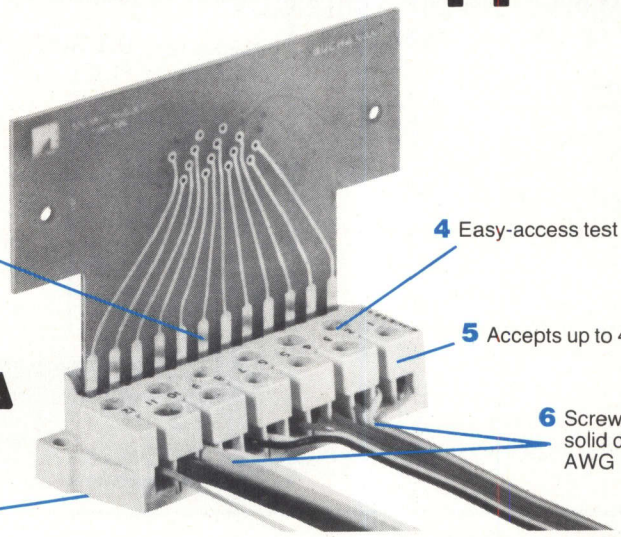

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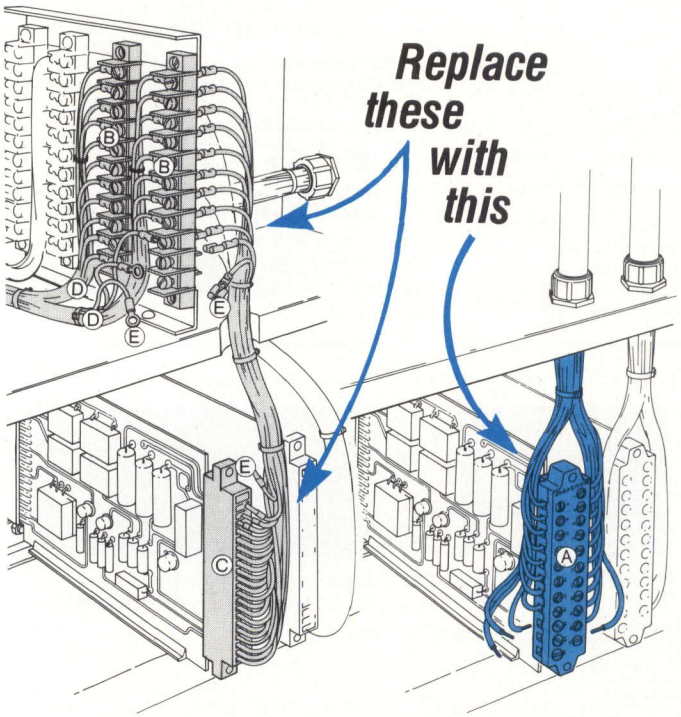

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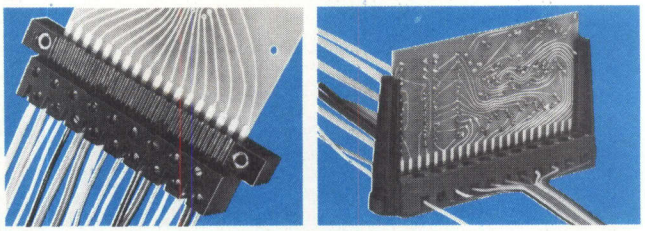

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As computer applications expand, reliability becomes ever more critical, and predicting and improving it more important. Predicting, measuring, and improving reliability are straightforward using the algorithm and two computer programs discussed here

Matrix Computations Forecast Computer Mainframe Reliability

Ramanuj Sharan

Control Data Corporation
St. Paul, Minnesota

More and more designers are becoming aware of the importance of reliability. As computers are being used in increasing numbers of vital functions the need for their reliability is being more strongly felt.

Reliability, in general terms, when applied to computers, means that a system should perform what it is designed to do, over a period of time, without any degradation. Often reliability is quantitatively measured as the number of hours a system would operate on the average without failing; this is known as the mean time between failures (MTBF). Reliability can also be expressed as failure rate, which is the inverse of MTBF. Failure rate is the statistical mean of the number of failures of a system per unit of time.

An MTBF of X hours is no guarantee that the system will be operational for that many hours. It means only that the mean of the time interval between successive failures of a large number of such systems observed over a long period of time approaches X hours. Similarly the number of failures per unit of time would approach the failure rate.

Reliability theory distinguishes three characteristic types of failures (Fig. 1). These failures are inherent to the equipment or component and occur without any fault on the part of the operator. First, some failures occur very early in the life of a component. These early life failures, generally caused by poor quality control, occur during the first few hours of system operation; components subject to such failures can usually be eliminated by an initial debugging or burn-in—that is, operating the equipment for a number of hours under conditions simulating actual use.

Second type of failure is caused by wearout resulting from improper equipment maintenance. Most wearout failures can be prevented by proper maintenance or by replacing worn-out parts before they fail.

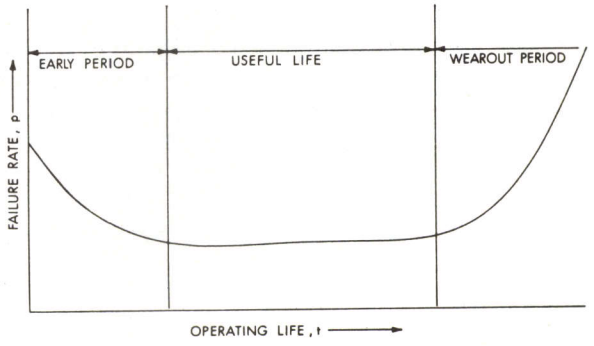

Fig. 1 Failure profile. When plotted against the lifetime, for a very large homogeneous population, the failure rate is high to start with. It quickly decreases to its probabilistic failure rate as substandard and weak specimens are eliminated, then goes up as old age and wearout set in

Third are so-called probabilistic or chance failures. Neither good debugging nor proper maintenance practice can eliminate them. These failures occur unexpectedly at random intervals. It is very difficult to predict when such a failure will occur. However, as all random occurrences, they follow certain rules of collective behavior which are approximately constant.

This last kind of failure is the subject of this article. Later sections discuss probabilistic failure, describe its nature, and show how to measure it, predict it, and improve upon it.

Life period of a piece of equipment, during which it is subject only to probabilistic failures, is conventionally called its "useful life." Reliability of such apparatus can be mathematically defined by the exponential formula $R(t) = e^{-pt}$ where p is the failure rate, and t is the operating time for which the reliability, R(t), is to be calculated. Reliability can now be defined as the probability that a device with a constant failure rate will not fail in the given operating time. This formula is correct for all equipment that has been properly debugged so that it is not subject to early failures, but not operated long enough to suffer any aging or wearout damage. The latter condition implies that the operating time in the formula should never exceed the useful life of the equipment, because after this time the machine becomes subject not to probabilistic failure, but to wearout failure.

Sometimes the MTBF, measured directly in hours, is used in the reliability formula, which then becomes $R(t) = e^{-t/m}$ where m is the MTBF.

In both versions of the formula, time is not a measure of the life or the accumulated operating time of the device. It measures only the span elapsed since the beginning of an arbitrary operation period, sometimes called mission time. The device is understood to have possibly participated in earlier missions and is not expected to reach the end of its useful life during the mission under consideration. Thus reliability at the beginning of the mission is 1—that is, non-failure is certain.

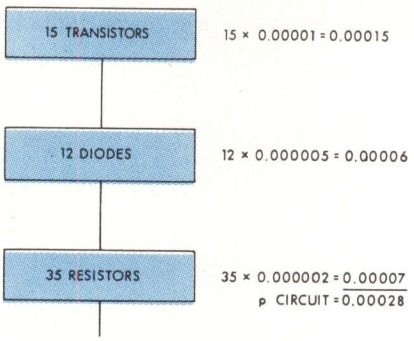

Fig. 2 Series system reliability. Failure rate of each component type is multiplied by the number of components, and the products are added to give system failure rate. The reciprocal is the mean time between failures (MTBF)

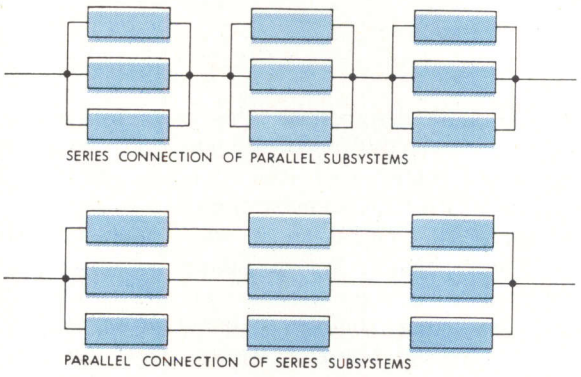

Fig. 3 Complex system reliability. If a large system is divided into smaller pieces, basic reliability formulas can be applied to the pieces and recombined to yield a measure for the system as a whole. Each block in these diagrams may itself be a series or parallel subsystem

Series and Parallel Systems

As stated, the reliability formula applies primarily to single components. Most of the time engineers are more concerned with evaluating the reliability of many components grouped in a system. System reliability can be calculated; two cases are significant.

When components are joined in series to form a system, all are necessary for the functioning of the system. If a single component fails, the whole system fails. Reliability for a series system is the product of individual component reliabilities.

$$R_s = e^{-p_1 t} \cdot e^{-p_2 t} \cdot e^{-p_3 t} \cdots e^{-p_n t}$$
$$= e^{-(p_1 + p_2 + p_3 + \cdots + p_n)t}$$
$$= \exp\left(-\sum_{i=1}^{n} p_i t\right)$$

Thus system failure rate is the sum of all individual component failure rates, assuming that all components have exponential reliability (Fig. 2).

In a series system, each component is critical to the system's proper functioning. System reliability can thus be greatly affected by having even one component that is less reliable than the others. One way to improve system reliability in such a situation is to backup the less reliable component by parallel components and increase system reliability by parallel redundancy.

Reliability, previously defined as the probability that a device will not fail during a time, t, has a complement, unreliability, or the probability that the device will fail:

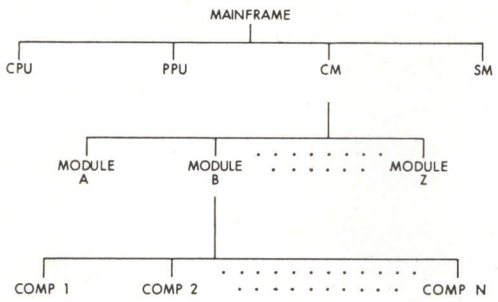

Fig. 4 Data base structure. Mainframe can be divided into subsystems (CPU, PPU, CM), subsystems into modules, and modules into components. This 3-level subdivision is suitable for most mainframes; sometimes a fourth level (chassis or unit) is necessary between subsystem and module

$$Q(t) = 1 - R(t) = 1 - e^{-pt}$$

Unreliability of a parallel system is the product of the components' unreliabilities, and likewise the system's reliability is the complement of this product:

$$\begin{aligned} R_p(t) &= 1 - Q_p(t) = 1 - Q_1(t)\,Q_2(t)\,Q_3(t) \ldots Q_n(t) \\ &= 1 - [1 - R_1(t)][1 - R_2(t)]\,[1 - R_3(t)] \\ &\quad \ldots [1 - R_n(t)] \\ &= 1 - (1 - e^{-p_1 t})\,(1 - e^{-p_2 t})\,(1 - e^{-p_3 t}) \ldots (1 - e^{-p_n t}) \end{aligned}$$

where $p_1, p_2, \ldots, p_n$ are failure rates of various system components.

Reliability of complex systems with both series and parallel connections can be evaluated by considering each parallel section as one subsystem, then combining the various subsystems in series, repeating the process as required in more complex systems to reduce everything to a system consisting of subsystems connected one way or the other (Fig. 3).

Reliability Prediction

Any mainframe reliability prediction program has two integral parts: procedure and data base. To keep computation simple, assume that the mainframe is a series system. This means that all components are necessary for the functioning of the mainframe; there is no redundancy or standby mode of operation. This assumption presents no serious handicap, because most mainframes encountered in practice are of this type. Those that have any form of redundancy or standby mode have it only in very small subsystems; the error introduced by treating them as series systems is insignificant.

Another simplification excludes mechanical hardware, such as compressors and condensers, from the basic mainframe, and includes only electrical circuits, components, and conductors. This takes in all transistors, diodes, microcircuits, printed circuit boards, connector pins, backpanels, and wiring, but not nuts, bolts, and other mechanical parts of the chassis.

Reliability prediction procedure uses the formula for series reliability computation, the sum of products of the number of components, and the failure rate for each component type. The inverse of the computed sum is the MTBF.

The mainframe can be divided into many levels of subsystems. A possible division is into central processor, central memory, peripheral processors, and secondary storage. Each of these subsystems can then be further divided into modules or cards, with a third subdivision into components (Fig. 4). This 3-level breakdown is suitable for most mainframe reliability applications. Sometimes, however, especially in large systems, a fourth level is necessary—chassis or unit—between subsystems and modules; for example, dividing the central memory into its control logic and two or more banks of storage cells.

No hard and fast rule governs the number of levels. The number chosen depends upon the system's structure and the proposed use of the reliability prediction.

The data base to be used by the prediction program has two parts: failure rate information for each component, and structural relationship between various hierarchical levels. Organization of the data base should take the language of the prediction program into account; for example, if the latter is written in APL, as is a particular Control Data reliability prediction program, the data base should be organized as arrays and matrices, which APL handles easily.

A linear array contains failure rate data as elemental entries, whose positions associate them with their respective component types. A 2-dimensional matrix contains structural information at each level. Number of rows represents the number of items above the level, while number of columns represents the number of items below that level; the entry in a particular position represents the number of lower-level items of that particular type contained in each upper-level item of a type. For example, if a subsystem contains 10 different kinds of modules, with 27 different types of integrated circuits, resistors, diodes, and so on, interconnected on the modules, the module-versus-components structure matrix at this level would contain 10 rows and 27 columns. If module type 3 contains seven quad 2-way NOR gates (7402s) and 15 resistors of 4.7 kΩ, 7 and 15 are entered in the third row, in the columns corresponding to these components.

Computation starts at the hierarchical level at which the reliability prediction is desired and progresses downward through the lower levels, accumulating component count. At the lowest level the array contains the total number of components of each type used. If only two levels are involved, the result is a matrix of component counts; a deeper analysis generates a matrix at each step, which multiplies the matrix at the previous step for a cumulative total. Using the numbers in the previous example, if the 27 component types on the 10 modules were distributed in various ways in three chassis, the first two levels would yield a matrix of three rows and 10 columns,

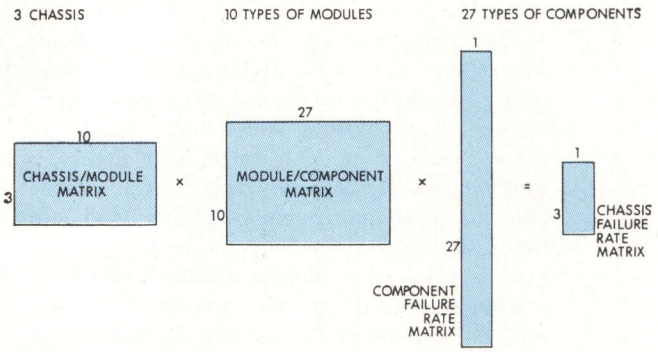

Fig. 5 Matrix computation. At each level of analysis a matrix reflects the failure rate information at that level. Multiplying successive matrices together and by the component failure rate array yields a failure rate matrix for the system as a whole

while the second and third levels would yield another matrix of 10 rows and 27 columns (Fig. 5). Subsystem total would then be represented by the product of these two matrices taken in this order, which is a matrix of three rows and 27 columns. (The product in the reverse order is not defined in matrix algebra.) Each entry in this product matrix represents total count of one component type in one chassis, without regard to which module types use it; column totals give the count of that component for the subsystem.

This position information matches the one in the linear array of component failure rates, which, taken as a 1-column matrix, has as many rows as the component count matrix has columns. The latter is multi-

Sensitivity Analysis of Module

Component	Component Count	Component Failure Rate	Total Failure Rate	Percentage Contribution
Transistor A	15	0.0001000	0.001500	26.04
Transistor B	25	0.0000500	0.001250	21.70
Transistor C	30	0.0000700	0.002100	36.46
Resistor A	50	0.0000020	0.000100	1.74
Resistor B	65	0.0000050	0.000325	5.64
Diode	32	0.0000090	0.000288	5.00
Capacitor A	25	0.0000030	0.000075	1.30
Capacitor B	15	0.0000040	0.000060	1.04
Solder joint	550	0.0000001	0.000055	0.95
PC Board	2	0.0000010	0.000002	0.03
Connector	1	0.0000050	0.000005	0.10
Total			0.005760	100.00

plied by the former; the product is another linear array, a 1-column matrix with as many rows as the count matrix has rows (three in the example). Each element of this product matrix is the failure rate of one chassis (or whatever the structural level is); the sum of the elements is the failure rate of the subsystem, and the inverse of the sum is the MTBF for that subsystem.

Sensitivity Analysis

Being able to predict reliability of computer mainframes is not very useful in itself. Satisfaction may follow if the prediction is better than was expected; however, the story does not have a happy ending if the prediction is substantially better than what is experienced. The obvious next question is: "What can be done to improve reliability?" The answer is "Very little," unless the cause of unreliability is known—that is, which component is contributing how much to the unreliability. Sensitivity analysis answers those questions.

Sensitivity analysis can be performed at any structural level—on the entire mainframe, on any subsystem, or on any module. Sensitivity analysis program begins with the component count array. Column totals in the count array are multiplied by the corresponding element in the failure-rate array. The product, expressed as a percentage of the total, is printed out (see Table for example). A quick glance at the Table shows the contribution various components made to the unreliability. Those components having the highest contributions are targets for reliability improvement.

A second part of the analysis program plots a graph of the MTBF of the subsystems under analysis versus the failure rate of one component. This plot shows how much improvement would appear in the subsystem, if any one particular component were improved. Cost of achieving this improvement can then be compared to the benefits expected from overall system reliability improvement.

Reliability Enhancement Techniques

To bring about the desired improvement in component failure rates, a number of methods are available. Most common enhancement technique is burn-in, which consists of operating the components at or around the system environment for some time before testing or using them in the system. This process eliminates most weak and substandard components which would cause the previously mentioned early-life failures. Duration of burn-in is usually determined by engineering experience.

Disadvantages of a long burn-in period include increased inventory expenses, larger capital expenditure in burn-in equipment, and longer time between receipt of materials and shipment of finished products. One way to minimize these disadvantages is to use accelerated burn-in, operating the components at elevated temperatures and voltages. This increases the effective stress on the components and eliminates the potential failures sooner.

Many variations of these accelerated tests are used. Some common ones are high temperature reverse bias, high temperature power-on, temperature cycling, voltage cycling, and thermal shock. More sophisticated tests include mechanical shock, vibration sweeps, humidity life tests, and tests in salt spray and other chemical corrosive agents. A lot of work in accelerated burn-in has been done by the military; results are available to the general public in military standard handbooks on reliability.

It is very difficult to establish a relationship between the accelerating factor, and increased stress, other than from experience and engineering judgement.

Conclusion

Reliability predictions are based on probability and statistics. Many assumptions must be made during the model building process. In reality the model is only as good as the assumptions on which it is based. The closer the assumptions are to actuality, the better will be the prediction. The model described here is based on the assumption of exponential distribution of failure rates; most electronic components correlate reasonably well with this distribution, but distributions of actual samples rarely fit model curves exactly.

Accurate predictions of reliability also depend on accurate failure rate data. When component reliability characteristics are known, analytical methods can predict system reliability very realistically. However, quite often failure rates are based on intelligent guesses or intuition and the resulting reliability analyses are wrong by orders of magnitude. Great care should be taken in this respect, and an effort should be made to determine the failure rates by running tests on samples.

Many manufacturers supply high reliability components at high prices, but not all of them furnish analytical data to back up their claims. Therefore failure rate data supplied by manufacturers should be taken with utmost reservation, especially when they are not supported by verifiable tests.

Ramanuj Sharan is a diagnostic engineer with Control Data Corp. A graduate of the Indian Institute of Technology at Kanpur, India, he also holds an MSEE degree from the University of Minnesota.

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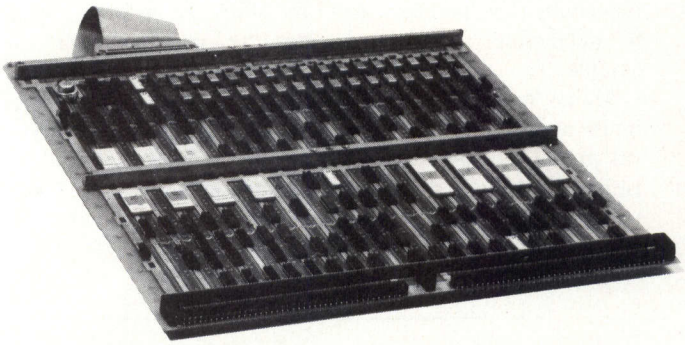

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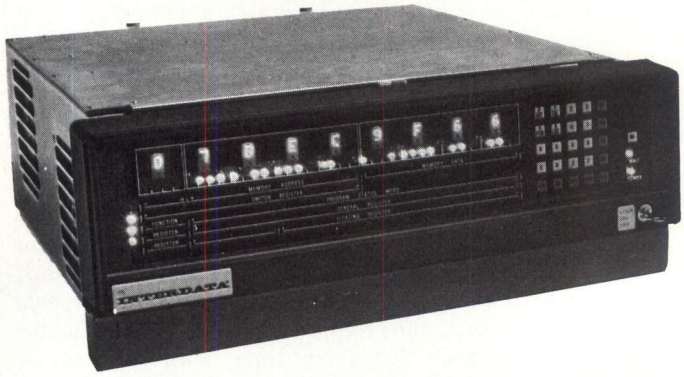

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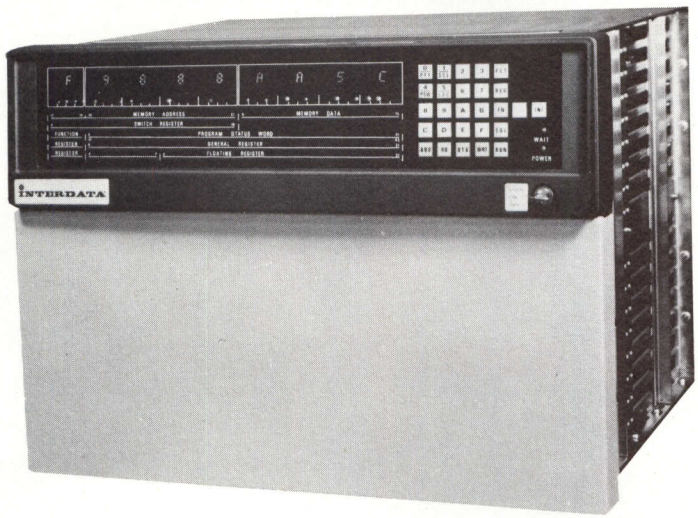

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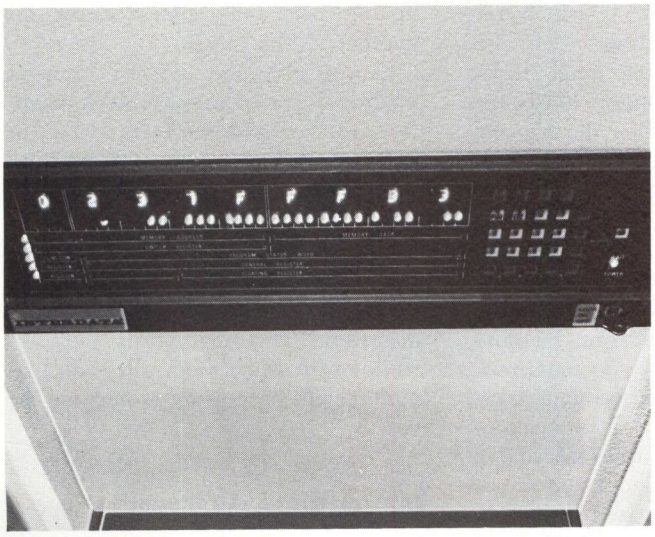

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CIRCLE 43 ON INQUIRY CARD

DESIGN NOTE

Hardware Versus Software For Microprocessor I/O

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Mountain View, California

Selecting the proper engineering trade-offs among hardware, software, I/O, memory, and speed requires use of both old and new techniques, some of which are outlined here

In considering how to implement input/output interfaces to a microcomputer, the designer deals with three primary resources in addition to his own time. These are memory size, processing speed, and special input/output hardware.

Most programs to perform a given reasonably complex input/output (I/O) function can be written in a number of different ways. In most cases the program is written to execute faster, even though more memory is required to store instructions; if speed is not an important factor, memory is conserved but the function is performed more slowly. (A third option is a program that takes a lot of memory and runs rather slowly, but takes less time to write. Programmers often overlook this option.) Similarly, when designing peripheral interfaces to the microcomputer, the amount and type of external logic required to support the I/O program is also a factor. I/O operations can be performed faster (transfer more bytes per second) and require fewer processor resources, by adding external logic.

Most common external logic for high speed I/O operations is direct memory access (DMA), which imposes the least reduction in processing time available for other tasks, but requires the most hardware. DMA is necessary when the transfer rate is higher than can otherwise be sustained, or when the transfer rate in conjunction with necessary concurrent processing is greater than can be maintained with an interrupt operation. In the DMA approach, data transfers to and from memory occur at the memory's maximum rate, if no other processing takes place. When using a 1-μs memory with an 8080 microprocessor and a 2-MHz processor clock, the memory-limited transfer rate is 1M byte/s. Thus a 300K-byte/s I/O transfer takes up only about one-third of the available time; during the other two-thirds the processor is free to perform other tasks. If a sequence that takes 4 μs (eight cycles) without interference is ready to start just as a DMA cycle takes place, it will finish in 6 μs, or 50% later than normal, having been interrupted again for another DMA cycle.

Conversely, the slowest transfer method is programmed block transfer, which performs I/O operations under complete program control, including any handshaking operation required. Not only is this method the slowest, but without interrupt logic the processor cannot execute any other function during the I/O operation. This method is the best choice when data rate is low and simultaneous processing would not be useful.

Intermediate Approaches

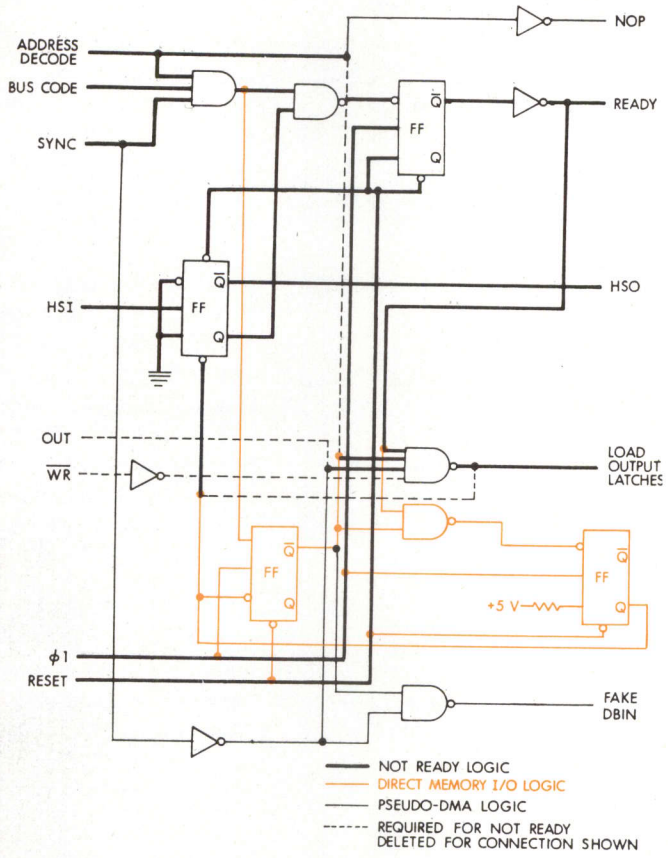
Tradeoffs among speed, memory (software), and hardware are illustrated by intermediate approaches between DMA and programmed block

transfer. Some are applicable to many different microprocessors and some can be used only with an Intel 8080 or similar microprocessor. First, as a reference point, is an 8080 program for a synchronous block transfer. Then techniques for eliminating instructions from this program by adding external control logic are illustrated. Finally, the program is replaced altogether by a technique that uses the program counter for the I/O data pointer.

To move data from a peripheral device to a buffer area in memory, the first two instructions of the synchronous block transfer program specify the starting point of the buffer area and the length of the data block, respectively. The transfer is initiated by setting one bit of the control output port. This signals the peripheral to start operation. Then one bit of the input status port is tested for a 0 to 1 transition which indicates that the peripheral has one byte ready at the input data port. This process continues until the last byte, determined by the bit counter, is transferred. After the last byte transfer, the output port control bit is reset, terminating the transfer.

In the program, bit 7 is used for all three of these functions (represented by the symbol 80H, or 80 in hexadecimal notation). At the design stage, any bit could be specified, within possible constraints imposed by the particular components or devices used. Furthermore, any of several techniques could be applied in setting and checking the bit specified; eg, instead of the AND Immediate used here, the program might use an OR Accumulator, to check the accumulator against itself and permit the sign bit to be used as the basis for a jump.

An image of the port's status/control register is kept in memory. Following initialization (lines 1-2) this image is updated with the current control word, which is then sent to the port (lines 3-6). A tight loop (lines 7-10) waits for bit 7 to be reset; a second loop (lines 11-13) waits for it to be set again. At that point a byte is in the data register; it is stored, and the memory address and byte count are changed (lines 14-17). Byte counter is a 16-bit word stored in two registers, D and E, which are decremented and tested independently (lines 18-22). When both reach 0, transfer is complete; the control word image is corrected, read operation is stopped, and the processor moves on to another operation.



Hardware for software. Logic blocks in heavy lines supply NOT READY signal, effectively relieving processor of need to test for I/O instruction completion. Additional logic transfers data directly to memory (color) and uses program counter as data pointer (light lines)

Logic Substitution

Maximum execution time of this transfer loop is 50 μs, or 20,000 bytes/s. This is relatively slow, partly because testing the synchronizing signal requires 27 μs, or more than half the byte time. However, adding the control logic to supply a NOT READY signal to the processor (heavy lines in figure) delays completion of I/O instruction execution until the peripheral is ready for the next transfer, so that the program need not make this test. Six instructions are deleted from the program. This not ready logic increases the transfer rate to 1 byte/23 μs, or 43,478 bytes/s, allowing use of a floppy disc (transfer rate of 1 byte/32 μs) without loss of any flexibility of programmed I/O.

Synchronous Block Transfer Program

Line		Instruction	Comments	Cycle Count	
1		LXI H,SADD	;Initialize starting address	10	
2		LXI D,-BCNT	;Initialize byte counter	10	
3	INPUT	LDA CNTLI	;Get image of control output port	13	
4		ORI 80H	;Set bit 7 to enable read	7	
5		STA CNTLI	;Update image in memory	13	
6		OUT CNTL	;Set bit 7 in output port	10	
7	LOOP1	IN CNTL	;Get status input word	10	Sync
8		ANI 80H	;Mask all but bit 7	7	Test
9		JNZ LOOP1	;If read synchronizer input is not 0		Loop
10			;go back and read input again	10	Data
11	LOOP2	IN CNTL	;After synchronizer input is low . . .	10	Transfer
12		ANI 80H	;start testing for a high level	7	Loop
13		JZ LOOP2	;Loop until high level appears	10	
14		IN DATA	;When synchronizing signal is high	10	
15		MOV M,A	;Read data and store in memory	7	
16		INX H	;Increment memory address	5	
17		DCX D	;Decrement byte counter	5	
18		MOV A,E	;Test if DE register	10	
19		ORA D	;is 0 by ORing		
20			;together Reg D and Reg E	5	
21		JNZ LOOP1	;If not 0		
22			;return to wait for another byte	10	
23		LDA CNTLI	;Get image from memory	13	
24		ANI 7FH	;Clear bit 7	7	
25		STA CNTLI	;Update image	13	
26		OUT CNTL	;Update output, turn off read	10	

Other hardware can eliminate one other instruction by transferring data directly between memory and I/O port. In the program, data being transferred appear on the data bus once for the transfer between memory and accumulator, and again for the transfer between I/O port and accumulator. However, the technique works only if the application requires less than 32K bytes of memory.

The technique removes the most significant address line from the memory decoding. Normally, a 16-bit address can locate any one of 65,536 bytes in the memory; but if the application requires less than 32,768 bytes, the most significant address bit is always 0. Removing it thus establishes two addresses for each physical memory location. Lower of these two (MSB = 0) is used for normal access to all locations; higher is used for I/O operations. When most significant address bit, ready line, and DBOUT (data bus out) are all high, data on the bus are loaded directly into the output port register, instead of being placed first in the accumulator. Similarly, for an input, the accumulator is bypassed and data go directly to memory. The logic is simply added to the not ready handshaking logic (colored part of figure).

Although this logic does not greatly improve the I/O transfer rate (only 5 μs/byte faster), the margin may make the difference between success and failure, at a very small increase in the amount of control logic.

Pseudo-DMA

If even faster data transfer rates are required, a Pseudo-DMA (PDMA) method can achieve up to 1 byte/2 μs, using much less logic than a full DMA capability. The method utilizes the program counter as a data pointer during the I/O operation, by disconnecting the processor from the data bus and the $\overline{\text{WR}}$ and DBIN control signals. Then, forcing NOP instructions into the processor during data transfer executes the transfers at the same speed as NOPs, or 500K/s. Data transfer can be synchronized to slower speeds with the READY signal.

As in the accumulator bypass, initiation and termination of a PDMA operation are controlled by removing two address lines, causing a block of

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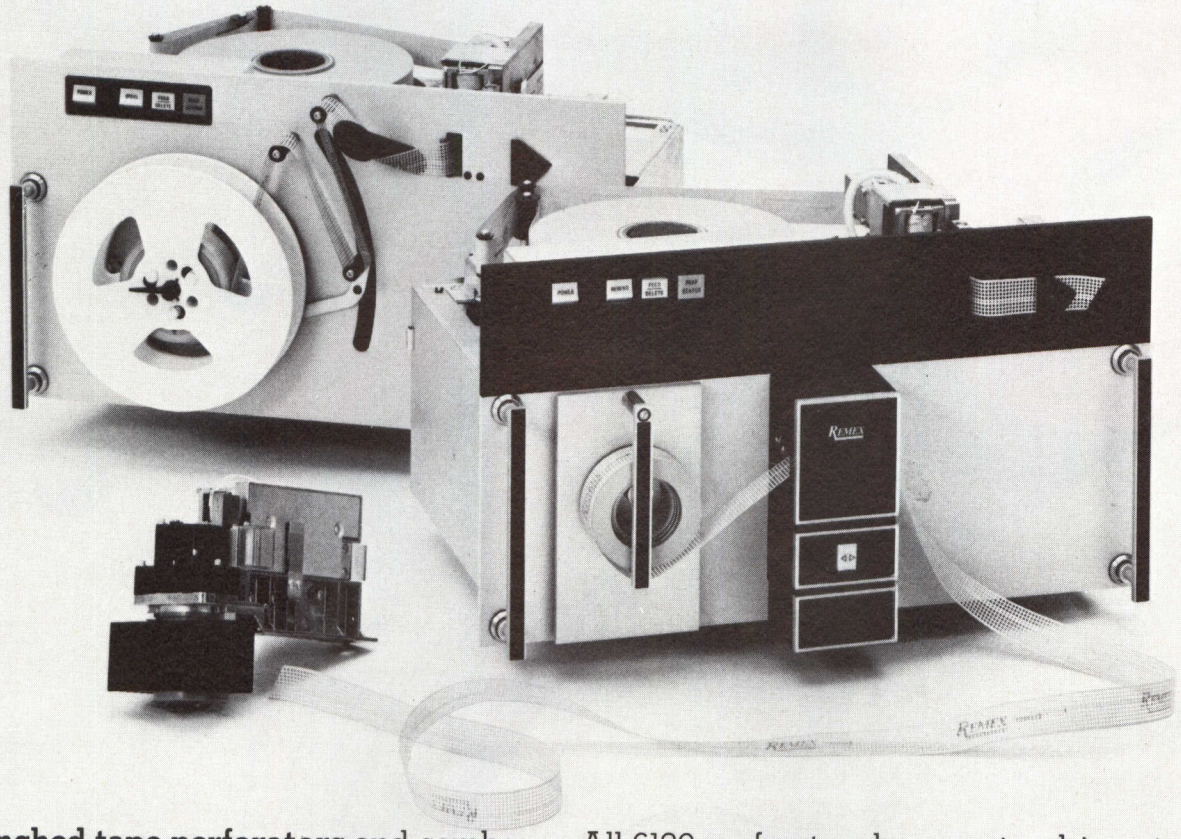

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memory to have four addresses. For example, suppose that 4K words in a 16K memory are set aside for PDMA. If the processor generates a 16-bit address, normally the two most significant bits are always 00.

However, PDMA can force them to 11. Then, when the PDMA controller (light lines in figure) sees that the most significant address bits are 1100, it forces NOPs and performs PDMA output from the 4K block addressed by the other 12 bits. When the most significant bits are 1110, a PDMA input operation is performed into the same 4K block. For these operations, the controller supplies the DBIN or WR signal as required. When the bits are 1111 or 1101, or when one or both of the highest bits are 0, normal memory access occurs in the 4K block or elsewhere.

Before performing a PDMA operation, a return instruction must be placed in the first location in the memory block, and when using PDMA, the last address of the data buffer area for input or output must be the last address in the memory block.

To initiate a PDMA data transfer, interrupts are disabled and a subroutine call executed to the beginning of the data buffer, setting the high-order address bits as just described. When the most significant address digit advances to D or F, the NOP insertion signal drops and the next instruction executed will be a subroutine return.

Conclusion

The designer who has thoroughly specified his requirements, studied the market for available solutions, and updated his rules of thumb as required by the new technology should find the most economical solution to his problem using techniques like those described here.

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DESIGN NOTE

Macro Processor Simplifies Microcomputer Programming

Nari Sohrabji*

Brand-Rex Company, Teltronics Division
Lakeland, Florida

Macroinstructions save time for the programmer while using the computer efficiently; but they require a special software processor for use together with existing assembler program

Macros are a powerful tool for producing control programs of microcomputers. These control programs are usually fixed, and are stored in read-only memories (ROMs). Size therefore has direct bearing on system cost. The system designer's task is to obtain required performance with a program of reasonable size. Also, cost of writing the program is a major part of development costs; hence the system designer must implement his optimum program within a reasonable time.

The designer generally can optimize the size of his program by writing it in the machine's assembly language; however, this program will take longer to write than one written in a higher level language. On the other hand, programming in high level language usually produces longer machine code than assembly language does. Yet, high level languages, usually derived from PL/1, are available for many microcomputer systems.

System programmers would like to have a language which produces code with the efficiency of assembly language and is as easy to use as high level language. Although this requirement existed before the advent of large scale integration (LSI) microcomputers, their small size and dedicated nature have increased its importance.

One approach toward these dissimilar goals is through use of macro language. Macros were originally devised by programmers of general-purpose computers as shorthand notation for blocks of code repeated several times in a program. Since then, macros have been developed to solve many programming problems. For example, they can help resolve the conflict between cost of programming and cost of program memory.

Some macro processors (preprocessors) produce an assembly language program; others are integrated with the assembler to produce machine code. Comprehensive macro facility permits the programmer both to call on a macro library and to define macros; it can be a considerable asset. A library of macros oriented toward a particular application enables engineers who are not software specialists to program effectively. Since a macro processor permits use of assembly language statements in source program, the programmer retains control over the structure of the program.

Basic Macro Concepts

Basic concept of a macro is text replacement. As an example, consider the following macro definition:

```
MACRO COMP      *START OF
                 DEFINITION
        PUL A   *LOAD ACCUMU-
                 LATOR FROM
                 STACK
        EOR A Q *EXCLUSIVE OR
                 WITH CONTENTS
                 OF Q
        STA A R *STORE RESULT
                 IN LOCATION R
MACND           *END OF
                 DEFINITION
```

This macro may be defined in the source program or may be available in a library. It is called in the source program by inserting the single macroinstruction "COMP" in instruction sequence rather than three assembly language instructions shown in the definition. When the macro processor translates the source program, it produces an object program containing the replacement text:

```
PUL A
EOR A Q
STA A R
```

An object program which consists solely of assembly language statements may now be assembled.

"Source program" and "object program" are defined as input and output of a translator. Thus the object program of the macro processor becomes the source program for the assembler, whose object program is the machine code.

*Mr Sohrabji is currently employed by A. C. Nielsen Co, Dunedin, Fla.

Macro Facilities

Power of the system is fully exploited when refinements are added to the basic concept. Among facilities which can be provided are:

Definitions with formal parameters (replaced by actual arguments during expansion)

Use of labels and opcodes as macro parameters

Macro calls within macro definitions, which ease definition of complex macros

Conditional macro definitions (expansion depends on the arguments of the call)

Recursiveness, which allows a macro to call itself

Optional arguments, which permit calls to be made with fewer arguments than specified in the definition

Argument lists of arbitrary length

Dynamically created definitions, created by macro calls

Design of Source Language

Source languages use three types of statements: assembly language statements, macro definitions, and macro calls. In a language and processor designed for the Motorola M6800 microcomputer system, format of a definition is

```
MACRO       (macro name)
            (macro body)
MACND
```

and format of a call is

```
(macro name)    (argument list)
```

Macro body consists of assembly language statements and formal parameters. For example, the macro COMP previously described could have been defined with Q and R as variables; it would then be written

```
MACRO       COMP
            PUL A
            EOR !1
            STA A !2
MACND
```

!1 and !2 are formal parameters which are replaced in the expansion by the actual arguments of the call. Then COMP can be called

```
COMP        M;N;
```

M, listed first, replaces the first parameter and N replaces the second.

Assembly language uses one statement per record of the input medium; this format has been retained in the macro language. Definitions, calls, and expansions are illustrated in Figs. 1 and 2, which list typical source and object programs. The actual importance of these programs is that they illustrate use of macros. Fig. 1 contains a number of assembly language instructions, and two macro definitions, each preceded by a comment identified by asterisks; the second definition calls the first macro, so that this example describes nested macros.

Fig. 2 is the result of processing instructions in Fig. 1. Assembly language statements and comments are identical with those in Fig. 1. Definitions of macros SWPIFM and SORT have been deleted. The call to SORT is replaced by expansion of SORT, with arguments of the call replacing parameters of the definition. Since SORT itself calls another macro, SWPIFM, three times, these calls to SWPIFM are replaced by the expansion of SWPIFM. Thus Fig. 2 lists instructions of SWPIFM three times, substituting arguments specified in the original call, SORT.

Design of Processor

Flow chart for the processor program (Fig. 3) shows that the processor reads a record from the source program and classifies it. Comments are immediately passed, unchanged, to the object file, thus avoiding the possibility that strings of characters that may be inadvertently meaningful to the processor are incorrectly recognized. Then if the record cannot be identified as part of a definition, macro call, or end statement, it can only be an assembly language statement and is also forwarded to the object file.

When a definition is encountered, the name is entered in a string array, MACNAME, and definition count, NMAC, is incremented. MACNAME keeps track of macros that have been defined and NMAC tells how many there are. The body is recorded in another string array, MACBDY, one statement at a time; indexes to start and finish of the body are entered in arrays BDYSTR and BDYSTP. These indexes are transferred to registers to control macro processing as part of the initialization following a macro call.

SFILE

```
100   ORG 0
110   A RMB 1
120   B RMB 1
130   C RMB 1
140   ORG 00FF
150   LDA A #4
160   STA A A
170   LDA A #5
180   STA A B
190   LDA A #6
200   STA A C
210 *MACRO SWPIFM PUTS THE LARGER
220 *NO. IN THE FIRST LOCATION.
230 MACRO SWPIFM
240    LDA A !1
250    SUB A !2
260    BPL L1
270    LDA A !1
280    LDA B !2
290    STA A !2
300    STA B !1
310 L1 NOP
320 MACND
330 *MACRO SORT SORTS 3 NOS. INTO
340 *A DESCENDING SEQUENCE.
350 MACRO SORT
360    SWPIFM !1;!2;
370    SWPIFM !1;!3;
380    SWPIFM !2;!3;
390 MACND
400    SORT A;B;C;
410    END
```

Fig. 1 Source program for macro processor. Macro definitions are basis for expanding macro call (line 400) into assembly language listing

OFILE

```
100   ORG 0
110   A RMB 1
120   B RMB 1
130   C RMB 1
140   ORG 00FF
150   LDA A #4
160   STA A A
170   LDA A #5
180   STA A B
190   LDA A #6
200   STA A C
210 *MACRO SWPIFM PUTS THE LARGER
220 *NO. IN THE FIRST LOCATION.
230 *MACRO SORT SORTS 3 NOS. INTO
240 *A DESCENDING SEQUENCE.
250    LDA A A
260    SUB A B
270    BPL ZZBA
280    LDA A A
290    LDA B B
300    STA A B
310    STA B A
320 ZZBA    NOP
330    LDA A A
340    SUB A C
350    BPL ZZCA
360    LDA A A
370    LDA B C
380    STA A C
390    STA B A
400 ZZCA    NOP
410    LDA A B
420    SUB A C
430    BPL ZZDA
440    LDA A B
450    LDA B C
460    STA A C
470    STA B B
480 ZZDA    NOP
490    END
```

Fig. 2 Object program of macro processor. Single macroinstruction of Fig. 1 expands according to definition to yield 24 assembly language instructions. This approach can save much time for user of microcomputers

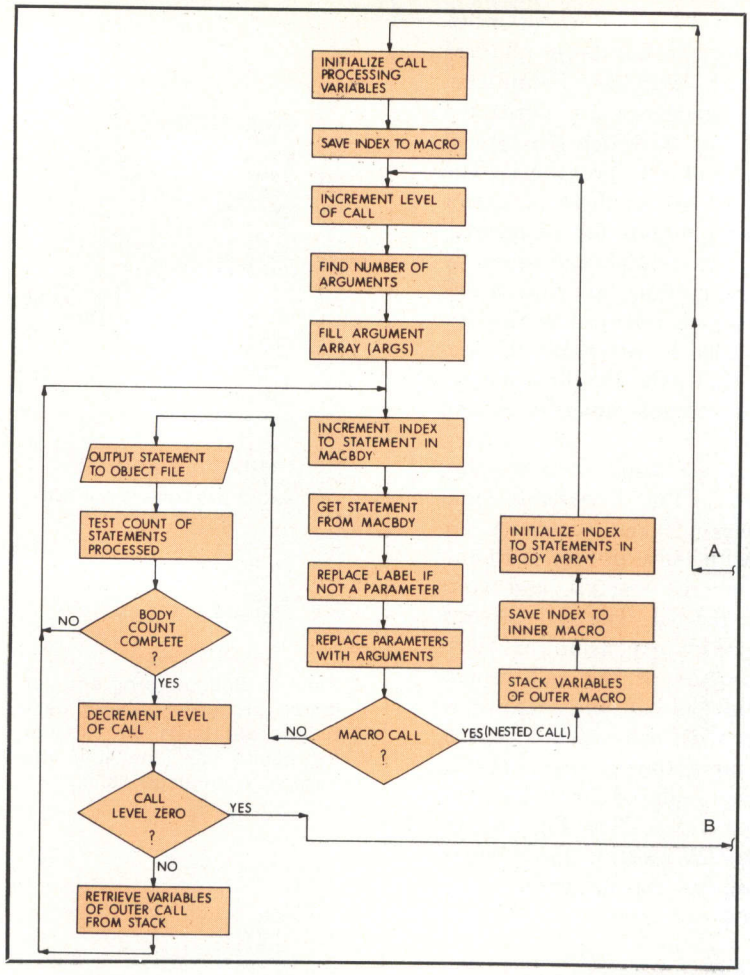
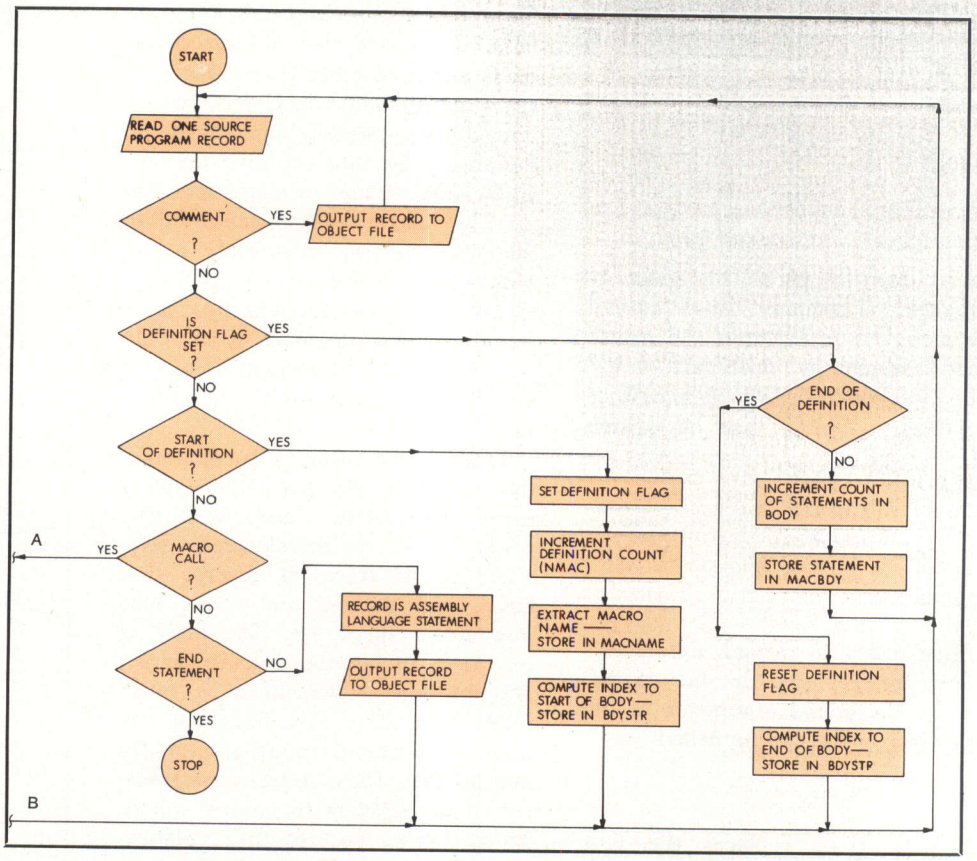


Fig. 3 Macro processor operation. Five basic types of statements—comment, start definition, end definition, macro call, and macro end—direct operation through various paths of flow chart



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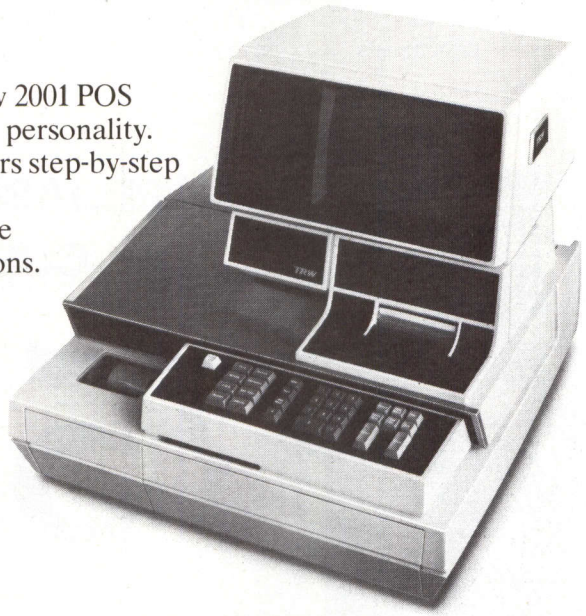

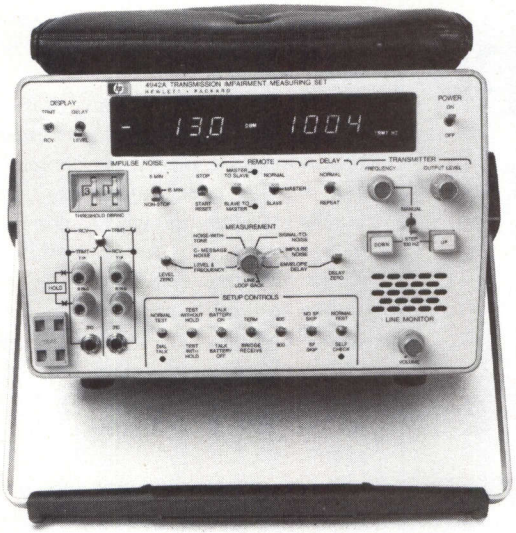

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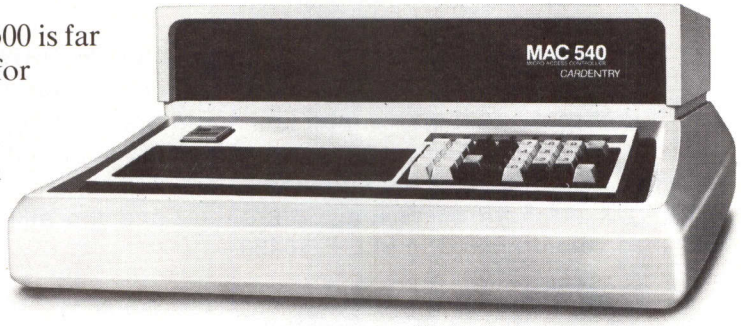

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Processor keeps track of nested macro calls by means of a level indicator which it increments with every call and decrements after processing that call. On identifying a call, arguments are entered into a string array, ARGS, in sequence. Statements are retrieved in succession from MACBDY, beginning and ending at the addresses specified by the index numbers in BDYSTR and BDYSTP. Since a macro may be called more than once, statements with labels must be given new labels at every call, unless the label is a parameter. Character representation of a label counter is appended to the characters ZZ to create a new label, and the counter is incremented. Labels beginning with ZZ are prohibited in the source program.

Formal parameters in the definition are now replaced by the corresponding arguments. Correspondence is established by position of the argument in the list.

If the statement obtained from the array MACBDY is not a macro call, it is passed on to the object file. If it is a macro call, processing of the outer call is suspended and variables required for processing this call are stored temporarily in two stacks. When the inner macro has been processed, the level indicator shows that an outer macro remains to be processed. Corresponding variables are now pulled from the stacks. Calls may be nested to the extent of stack capacity. The macro processor developed for the M6800 microcomputer system has capacity to nest 10 macro calls. Two stacks occupy 200 words of memory.

This macro processor has been implemented as a preprocessor to a separate assembler which is available for this system. Macro processor program is written in FORTRAN and uses string manipulation routines extensively; it may be run on any general-purpose computer or time-shared system that has a FORTRAN IV compiler. It produces an object file that is a source file to the cross-assembler, which also runs on a large computer and produces machine code.

An integrated system that combines macro processing and assembly functions can be quite efficient and can provide special facilities such as macro expansions which depend on the context of the assembly language program.

Macro facility provides a means for resolving conflict between ease of programming and efficiency of the program. The facility may be used to the extent desired by the programmer. Language is designed to resemble assembly language, providing a familiar format. The processor provides facilities useful for programming microcomputers, including facility for nesting macro calls. Source and object program listings illustrate features such as label handling, nested macros, and repeated macro calls.

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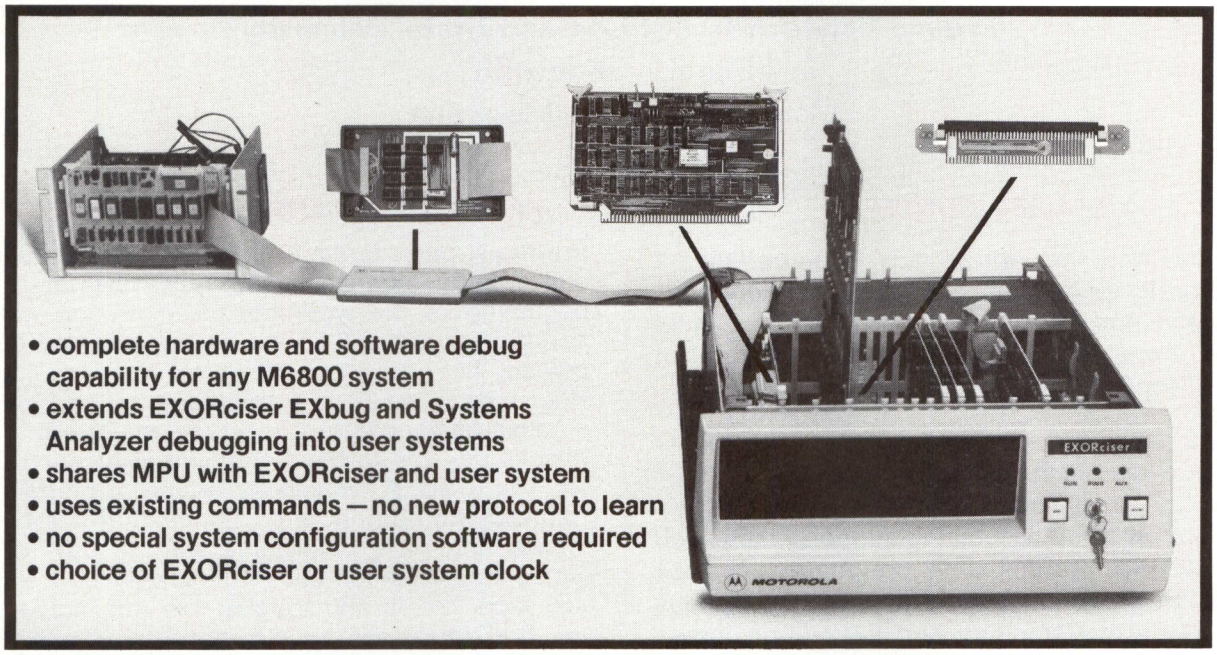
Motorola creates new debugging power for M6800 systems



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Some experience in digital electronics, minicomputers, and programming would be helpful but is not necessary. In digital electronics, useful topics to know beforehand include the 74154 decoder, 7474 flip-flop, 3-state busing, and the use of gates as gating elements to counters and other digital devices. Technical questions should be addressed directly to the course instructors, David G. Larsen, (703) 951-6478, Dr. Peter R. Rony, (703) 951-6756, or Dr. Paul E. Field, (703) 951-5385.

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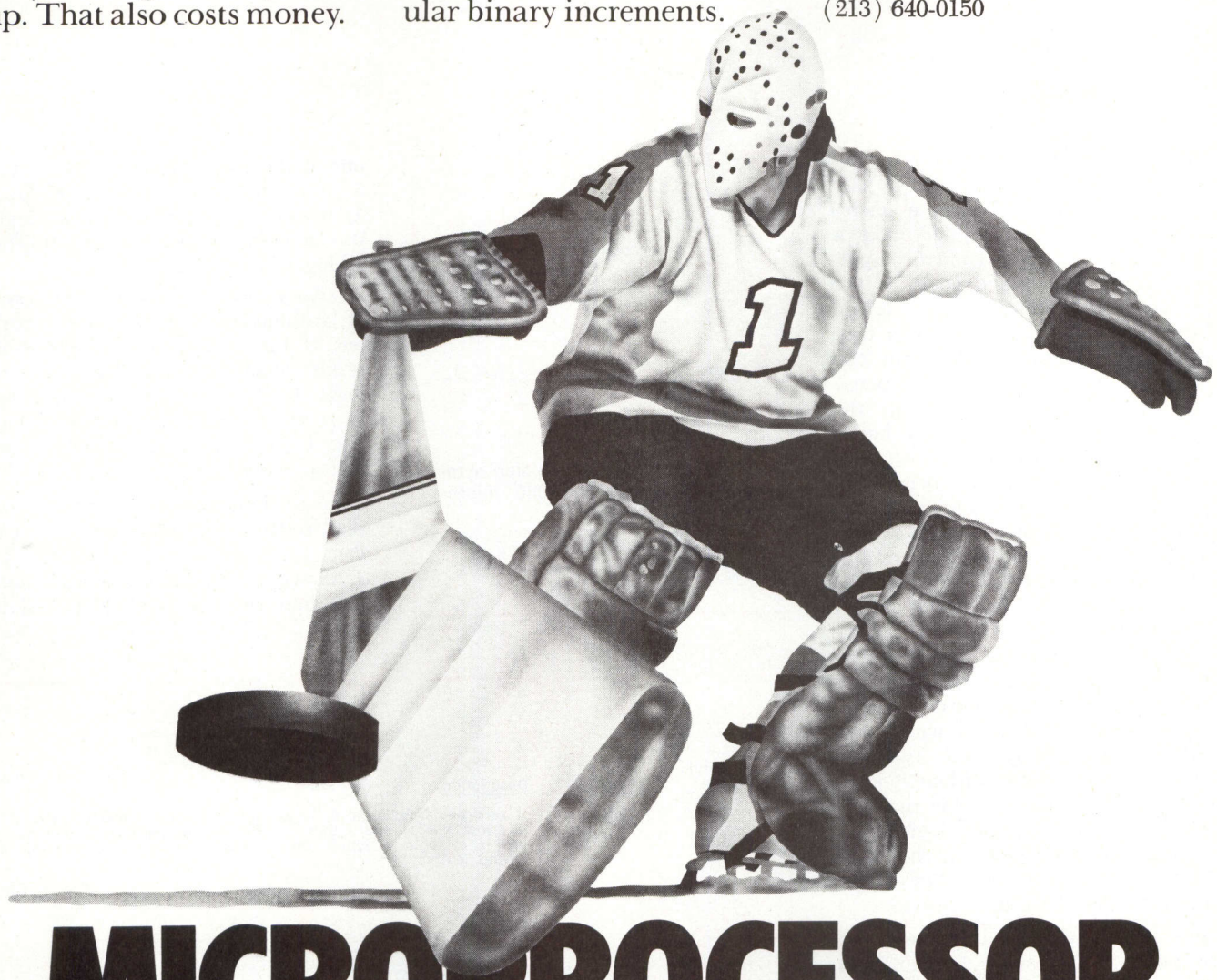

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Peter R. Rony
Virginia Polytechnic Institute & State University

One of the most important programming characteristics possessed by any digital computer, including a microcomputer, is the ability to make a decision. For a typical microcomputer, decision can be defined as the process of determining further action based upon the logic state of a flag. A flag is a single flip-flop that can be either set or cleared in response to operations occurring within the microcomputer system. A flag's change of state usually indicates either that a particular operation has been completed or that a certain condition exists as a result of a microcomputer operation. Flags can be located internal or external to the microprocessor chip; ones that we shall discuss are internal flags, which are set or cleared in response to specific types of microprocessor instructions such as arithmetic and logical instructions.

Flags that are located within the microprocessor chip are typically associated with the arithmetic-logic unit (ALU), a region within the chip where all arithmetic and logical operations are performed. In the 8080 chip, for example, five flags exist indicating the following conditions:

Zero flag—If the result of arithmetic or logical operation is zero, zero flag is set to logic 1; if non-zero, zero flag is reset to logic 0

Sign flag—If the result of arithmetic or logical operation is negative, sign flag is set to logic 1; if positive, sign flag is reset to logic 0

Parity flag—If the result of arithmetic or logical operation has even parity, parity flag is set to logic 1; if odd parity, parity flag is reset to logic 0

Carry flag—If the result of arithmetic or rotate operation has a carry out of the most significant bit of the 8-bit result, carry flag is set to logic 1; if not, carry flag is reset to logic 0. Carry flag is reset to logic 0 after all logical operations

Auxiliary carry flag—If the result of arithmetic operation has a carry out of bit 3 into bit 4 of the 8-bit result, auxiliary carry flag is set to logic 1; if not, auxiliary carry flag is reset to logic 0. Auxiliary carry flag is reset to logic 0 after most logical operations

Due to limited column space, we shall restrict our attention to the zero flag.

Shown in Fig. 1 is the traditional flowchart decision symbol applied to

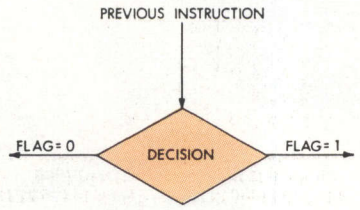

Fig. 1 Flow chart decision symbol as applied to 8080 microprocessor decision

Instruction Code	Mnemonic	Description
302 <B2> <B3>	JNZ	If zero flag is at logic 0, jump to 16-bit memory address given in bytes <B2> and <B3> of this 3-byte instruction; if zero flag is at logic 1, ignore this instruction and proceed to following instruction

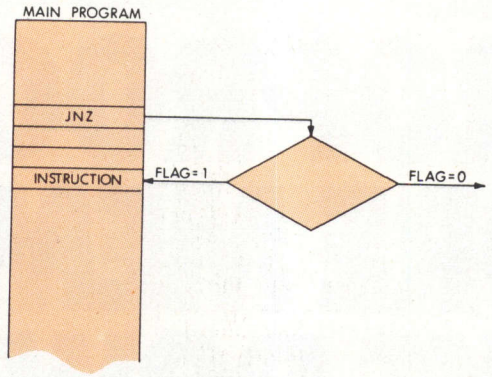

Fig. 2 JNZ instruction. If zero flag is at logic 1, instruction is ignored and program control passes to the following instruction

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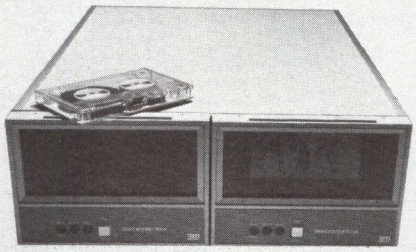

It adds up to this: now the system designer has a reasonably-priced peripheral that delivers both data reliability and data interchange capability. We're certain our competitors are going to be very interested in this new system. And if you are too, just write 3M Company Data Products, Dept. 129, Mincom Division, Bldg. 223-5E, 3M Center, St. Paul, Minnesota 55101.

All our competitors can do is follow us.

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CIRCLE 52 ON INQUIRY CARD

TABLE 1

Time Delay Loop

LO Memory Address	Instruction Byte	Mnemonic	Clock Cycles	Description
000	006	MVI B	7	Move following timing byte into register B
001	*	—	—	Timing byte for register B
002	323	OUT 2	10	Generate device-select pulse that sets the SN7474 flip-flop
003	002	—	—	Device code for set input to SN7474 flip-flop
004	005	DCR B	5	Decrement contents of register B by 1
005	302	JNZ	10	If zero flag is at logic 0, jump to memory address given by the following two address bytes; otherwise ignore this instruction
006	004	—	—	LO memory address byte
007	000	—	—	HI memory address byte
010	323	OUT 3	10	Generate device-select pulse that clears SN7474 flip-flop
011	003	—	—	Device code for clear input to SN7474 flip-flop
012	166	HLT	7	Halt microcomputer

TABLE 2

Output Pulse Widths

Timing Byte at LO Memory Address 001	Number of Clock Cycles	Pulse Width, ms
000	3850	1.925
001	25	0.0125
002	40	0.02
003	55	0.0275
004	70	0.035
005	85	0.0425
010	130	0.065
020	250	0.125
050	610	0.305
100	970	0.485
200	1930	0.965
300	2890	1.445
350	3490	1.745
377	3835	1.9175

an 8080 microprocessor decision. The next instruction that is executed depends upon logic state of the flag that is associated with this specific decision. For example, consider the JNZ instruction, where JNZ means "Jump If Not Zero" (Fig. 2). This statement refers to the 8-bit result of a preceding instruction, not the logic state of the zero flag. When this result is zero, the zero flag is set at logic 1 and program control passes to the next instruction, as shown in Fig. 2.

JNZ instruction is widely used in creating programmed time delay loops, an example of which is provided in Table 1. In this program, both address and instruction bytes are in octal code; it is assumed that HI memory address byte is 000. The program first moves an 8-bit timing byte into register B; this byte, indicated by an asterisk, has any value between 000 and 377. Value of the byte will determine the duration of time delay.

At LO memory address 002, device-select pulse is generated to set the SN7474 flip-flop shown in Fig. 3. Contents of register B are then decreased by 1. JNZ instruction immediately tests the logic state of the zero flag; if contents of register B

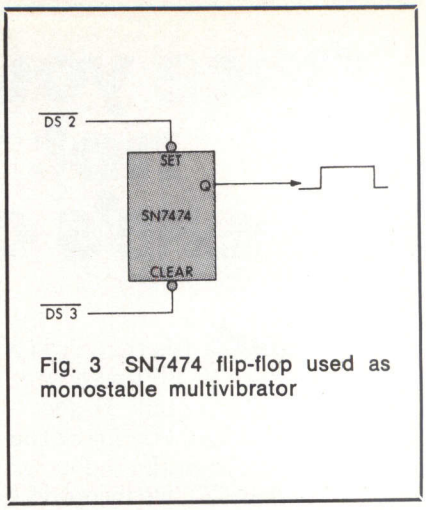

Fig. 3 SN7474 flip-flop used as monostable multivibrator

are not zero, flag is at logic 0 and a jump occurs back to LO memory address 004. DCR B and JNZ instructions are executed repeatedly until content of register B becomes zero, at which time the zero flag becomes logic 1. JNZ instruction tests the flag for the last time and shifts program control to the OUT 3 instruction at LO memory address 010. This output instruction generates a device-select pulse that clears the SN7474 flip-flop. Once this has been done, the microcomputer comes to a halt.

Program shown in Table 1 generates single output pulse, duration of which can take any value between 0.0125 and 1.925 ms in 0.0075-ms steps. Some typical pulse widths generated by the program in Table 1 are summarized in Table 2 for an 8080-based microcomputer that operates at a clock rate of 2 MHz. Calculations associated with conversion of clock cycles to pulse widths have been discussed in Ref. 1. Number of clock cycles is a measure of the actual time that it takes the microcomputer to execute a single instruction or group of instructions. For a 2-MHz microcomputer, a single clock cycle has a 500-ns duration. Program in Table 1 and associated SN7474 flip-flop provide an example of "substitution of hardware by software," *viz.*, a simple program and single flip-flop replace a much more complicated hardwired programmable monostable circuit.

Reference

1. *Bugbook III, Microcomputer Interfacing, Experiments Using the Mark 80 Microcomputer, an 8080 System,* E & L Instruments, Inc, Derby, Conn, 1975

This article is based, with permission, on a column appearing in *American Laboratory* magazine.

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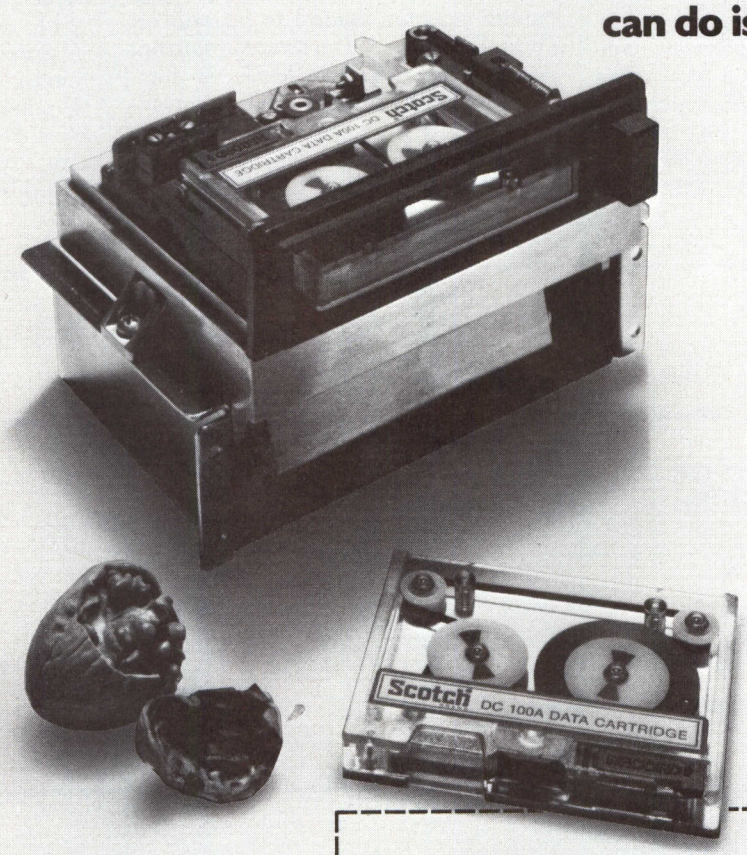

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CIRCLE 53 ON INQUIRY CARD

Microcomputer Package Provides High Speed Processing Capabilities

A complete microcomputer system based on a 6502 CPU manufactured by MOS Technology, the ETC-1000 comprises a 40-key keyboard, programmable 8-digit display, I/O interfaces, power supply, and memory. All systems are fully assembled, tested and ready to run; no external attachments, such as teletypewriters, power supplies, or memory expansions, are needed to provide basic programming capability and computer operation. Available expansion options include communications, real-time and DMA interfaces, memory expansions, and various add-on CPUs.

Designed by Electronic Tool Co, 4736 W El Segundo Blvd, Hawthorne, CA 90250, the package is intended for system development, control, and small-scale data processing applications. As a development system, it provides full support for hardware and software design work; as a control system, it offers inexpensive high speed computing capability in rack-mountable package; and for standalone and communications-oriented data processing, it offers memory expansion, I/O capacity, and programming flexibility.

Keyboard, mounted on front, includes full set of hexadecimal keys for data and address entry, and system function keys such as load, reset, and examine memory. Eight special function keys which may be sensed under program control by the user are available for assignment to user-specified functions. An 8-digit LED panel display is contained in the control unit to display memory contents, system status, and user-programmed information.

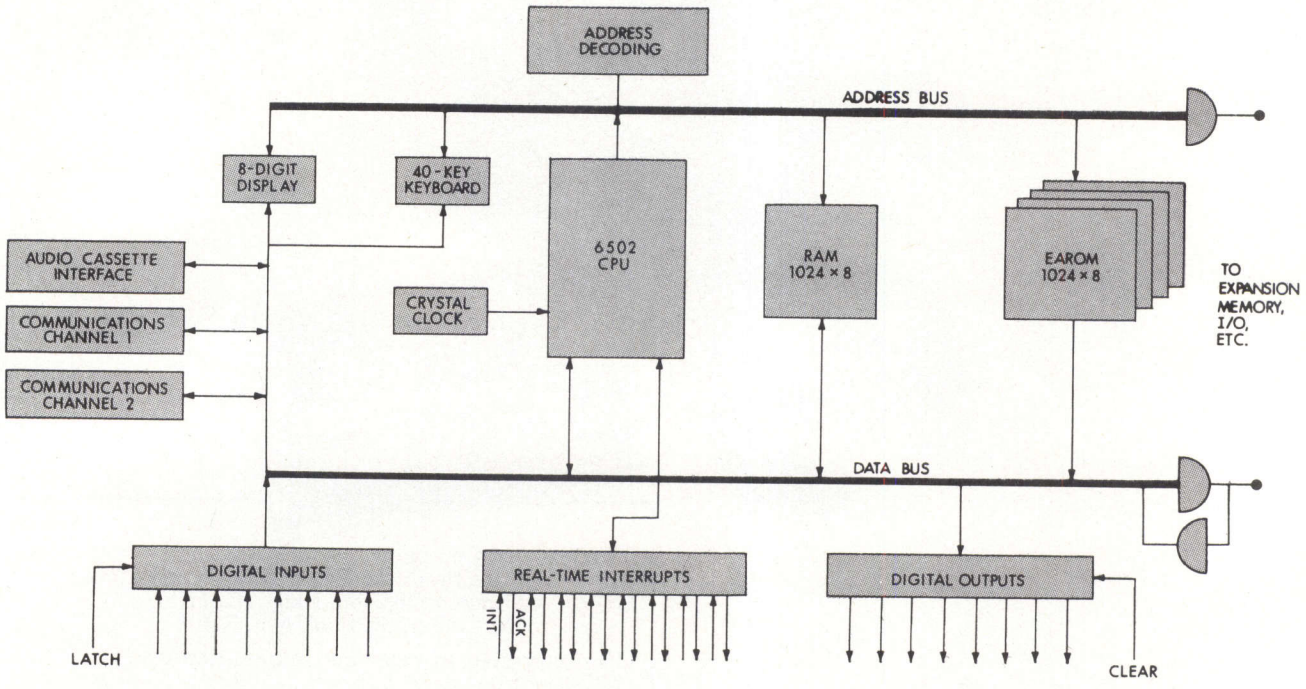
System contains direct I/O of eight latched output lines and eight latching input lines which may be used under program control to operate external devices. Hardware interrupt capability with two levels is standard; eight additional levels are available.

It is claimed that one or two independent full-duplex communications streams at speeds between 110 and 1200 bits/s are supported by the basic system when appropriate p/ROMs are included. Speed selection is accomplished automatically by hardware. Provided as standard are 20-mA dc current loop interfaces, with EIA RS-232-C capability available as an option.

CPU consists of 8-bit CPU, clocks, control logic, interface buffers, 1024 bytes of high speed R/W memory, and 256 bytes of EAROM containing system control functions. ROM and R/W memory may be added in increments of 4K and 8K bytes per module, up to 64K bytes for the basic package. Using memory map option, total storage capacity can be increased to over 4M bytes.

Additional CPUs, such as 8080A, M6800, 6502, and F8, can be added on a plug-in basis. Most additional processors consist of a single module and include the processor, its private read-only and writable memory, and interface circuits to the ETCBUS, which is the common communication path among all system elements.

Software currently available includes a resident assembler, I/O handlers, diagnostics, and other support tools. BASIC and PLM support are expected to be available during the third quarter of 1976.



ETC-1000 microcomputer system configuration. Ready to use, high performance, self-contained modular digital computer features memory, keyboard, display, and direct I/O system

Circle 170 on Inquiry Card

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DR-180	4K x 8 8K x 8	750/250 ns 750/250 ns	9.2" x 6.3" (233.4 mm x 160 mm)	+5V, +12V	30 Watts	8080 Microprocessor
DR-121	1K x 10 2K x 8 2K x 10	900/350 ns 900/350 ns 900/350 ns	11.7" x 11.5" (297 mm x 292 mm)	+5V, −12V	25 Watts	Cambridge Memories' 1K x 9 Unicore
DR-104	4K x 9 8K x 9 16K x 9 32K x 9	750/350 ns 750/350 ns 750/300 ns 800/300 ns	13.5" x 8.3" (343 mm x 211 mm)	+5V, −12V	32 Watts	National Semiconductors' MOSRAM 104

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CIRCLE 54 ON INQUIRY CARD

μComputer-Compatible Analog Output Cards Have Up to 8 D-A Channels

Eight D-A output channels are now available on a standalone peripheral card which is pin-compatible to the Intel SBC-80/10 and MDS CPU bus. Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021 offers this card for industrial process control applications which use an A-D input channel to monitor a particular parameter and require a D-A output channel to supply analog feedback voltage to an actuator, servo, solenoid, or other power handling device.

Model ST-800-DA4 offers a modular encapsulated dc-dc converter on the same card with four D-A converters. The dc-dc converter generates ±15-Vdc power by drawing less than 1 A from the 5-V CPU power bus. However, because model ST-800-DA8 uses external ±15-Vdc power, it does not require a dc-dc converter and therefore contains eight D-A converters on the same size card.

Basic settling time of each D-A converter, including register loading, is 4 μs. Depending on programming mode, two or more 2-byte instruction sequences are required for updating each D-A output channel.

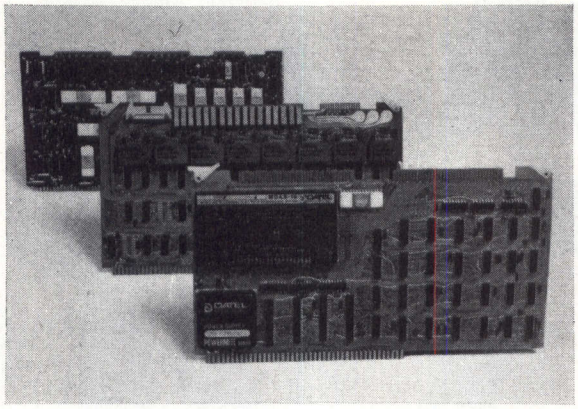
Both 4- and 8-channel analog output peripherals are complete, standalone, addressable I/O systems. They include hard-wired 8-bit base address decoder and jumper-programmable interrupt level. Programming flexibility is enhanced by on-board first and last channel registers which steer incoming data words to individual word registers associated with each D-A converter. The processor, therefore, does not have to supply new channel addresses with each new channel register update. A word counter is automatically incremented with data output cycle and is compared to the preloaded last channel. When last channel is reached, processor is notified by way of a hard-wired interrupt level.

An additional feature on both boards is an interval clock which initiates update scans by flagging the interrupt level. This scan timer uses a logic clock which is adjustable up to 1 s.

Output systems are organized around the company's miniature hybrid 12-bit D-A converters, which have hard-wired full scale voltage output ranges of 0 to 5 V, 0 to 10 V, ±2.5, ±5, or ±10 V. Input coding is hard-wired as straight binary unipolar, offset binary bipolar, or 2's complement bipolar.

Both systems can be directly expanded up to 256 channels using complementary ST-800-DAX slave boards. Additional backplane connectors, card cages, and power supplies are required. The 8- and 4-channel systems are built on 12 x 6.75 x 0.375" cards.

Circle 171 on Inquiry Card



Compatible with Intel microcomputers, series of D-A analog output cards are available with either four or eight channels, expandable to 256 channels

Companies Announce Joint Effort to Penetrate Microcomputer Market

Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006, and Zilog, 170 State St, Suite 260A, Los Altos, CA 94022, announced an agreement that combines the two companies' resources and technologies in a major 'cooperative effort to capture a significant part of the microcomputer market. Under terms of the agreement, Mostek will second-source Zilog's Z-80 microcomputer family of components, and the two companies will "jointly define and develop memories suitable for the microcomputer market and additional peripheral chips for the Z-80 family." (Full description of the Z-80 microcomputer can be found in the Feb 1976 issue of *Computer Design*, p 132.)

The agreement involves long-term financial commitments from Mostek for rights to certain Zilog technology, representing a major commitment from Mostek. According to Ralph Ungermann, executive vice president for Zilog, the agreement is unique in the industry: "Zilog is a generation ahead in microcomputer technology, and Mostek is an acknowledged leader in the MOS/LSI field, with high volume production capacity. Both companies are viable in the business, and in production."

Acting as active partners in going after the microcomputer market, Mostek will concentrate on memories, while Zilog will focus on peripherals. Due to Mostek's production capacity and marketing strength, and to Zilog's technological and developmental depth in the microcomputer field, the companies expect to have an immediate impact on the market.

Circle 172 on Inquiry Card

Slice Processor Family Will Use ECL Technology To Increase System Speed

A bipolar arithmetic logic unit (ALU), described as the first LSI component of a new high performance 4-bit slice processor family, is claimed to be the industry's first LSI application of high speed ECL technology. According to Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036, the basic family of four LSI components (4-bit ALU slice, microprogram control function, timing function, and memory interface function) will be in production by January 1977. Family of com-

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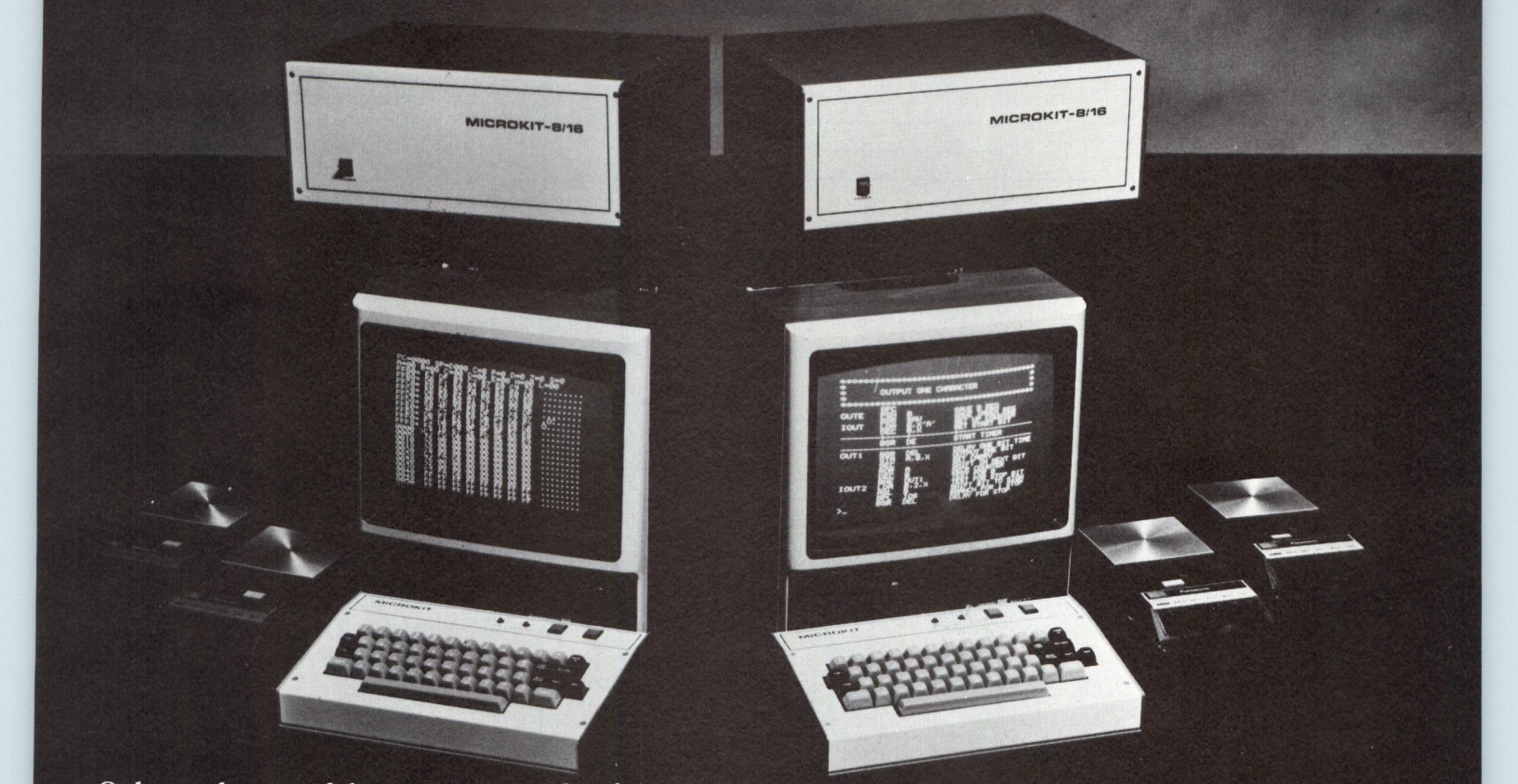

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To match our fast debugger we have a screen based editor that is quickly learned and easy to use, because it lets you see the changes you make instantly and in full context on the CRT display. Rounding out our outstanding software package is a complete microcomputer resident assembler.

Any system without a display as fast as ours and without software like ours cannot possibly match the powerful debugging and editing features we offer.

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But how is it that the MICROKIT-8/16 has everything (keyboard, display, tape units, and software) included in the basic price? We keep your cost low by using a standard television set for the high-speed display, and by using audio cassette units for mass storage. And with MICROKIT's proprietary recording technique, you get data reliability comparable to digital cassette units while data is transferred to the casettes at the rate of 2000 bps — 20 times faster than TTY paper tape.

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The MICROKIT-8/16 can be ordered as either an 8080 or a 6800 based system. At $3,850 either system is the best buy in microcomputer development systems today because they both include the 8K memory, the display and keyboard, the two audio cassette units, and the full complement of development software — debugger/monitor, editor, and assembler. Furthermore, either system can be easily switched to the other processor with our conversion packages that consist of a plug-in processor module and software.

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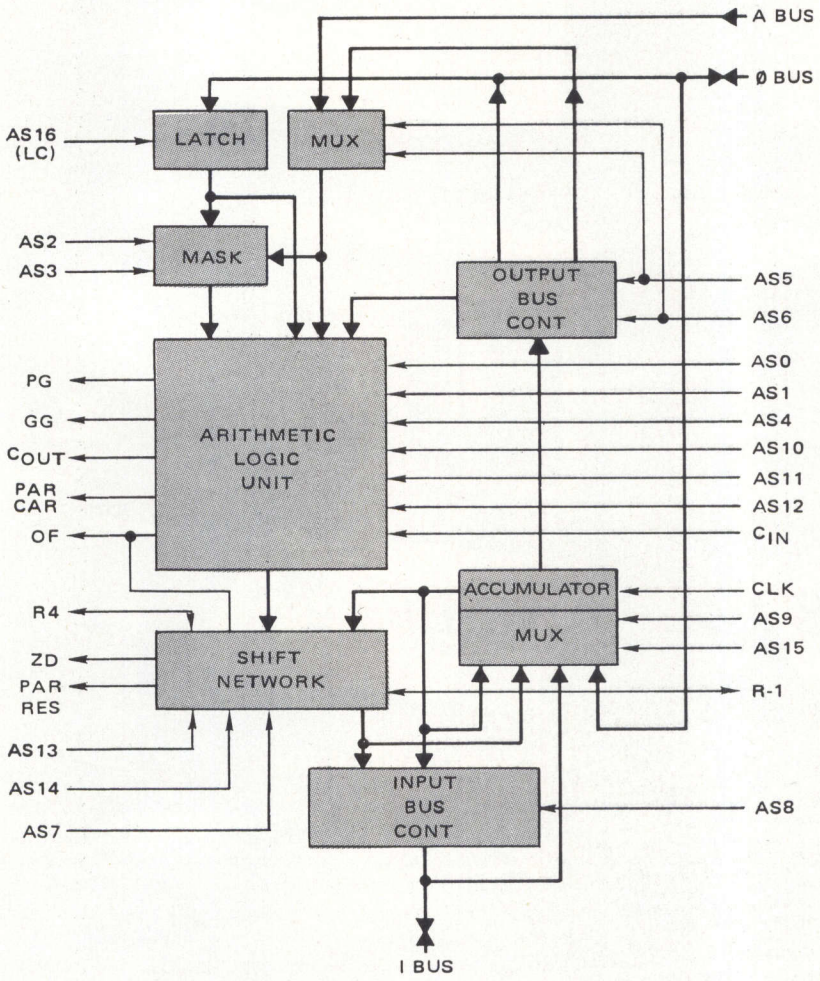


4-bit slice contains latch/mask logic, ALU, shift network, accumulator, and bus control logic in single bipolar circuit; 17 select lines are used to control all operations within the part

ponents for the bit slice processor also includes a number of associated memories.

Designated as the M10800 system, the family is applicable to the high performance controller and processor field. It consists of a number of compatible building blocks with parallel orientation to make them fully expandable to larger word lengths. Two 4-bit slice circuits in parallel constitute an 8-bit system used in many controller applications; four circuits result in the 16-bit machine word size; and eight circuits give a 32-bit word length which is preferred in many high performance computers being designed today.

Regardless of size, the system retains microprogrammability by means of which a block of high speed memory can be programmed to house the system's instruction set. Microprogram control, like word length, is expandable. It is possible to configure special-purpose machines from 256 words (or less) of control storage, to highly sophisticated systems with thousands of control words.

Advantages of microprogramming are usually offset by system speed, since each processor instruction requires several microprogram steps. MECL 10000 circuit technology and interfacing are used to attain fast microprogram cycle times. Operation with worst case system microinstruction cycle times is less than 100 ns. In addition, other features (such as powerful ALU function set) minimize the number of microprogram steps per system instruction.

Only 1.0 square inch of circuit board area is required for the 48-lead quad-in-line "QUIL" IC package; a matching socket has been developed and is available.

The processor family initially will not be supported with a given instruction set and associated assembler or simulator software, as the company feels that most users will configure the family to emulate an existing machine and supporting software.

Circle 173 on Inquiry Card

Processing System Minimizes Time of Design and Programming

The μP series is a modular microcomputer system designed with major subsystems on individual logic cards to allow the designer flexibility in configuring memory and I/O structure. Card size is directly compatible with the existing company logic card line, allowing for interface development and packaging in the same card file with the microcomputer system.

An available interface to the DEC PDP-11 allows the computer to exercise full control over the microprocessor address, control, and I/O buses. This, along with a proprietary Microprocessor On-Line Development System (MODS) and cross assembler for the series, permits the user to develop and debug microcomputer software utilizing the larger system. RAM/ROM memory module is available for program development directly on the microcomputer system. Series communications features also allow the system to function as a remote data acquisition or control device under supervisory control of a host computer.

Several modules are included in the series introduced by Wyle Computer Products, 3200 Magruder Blvd, Hampton, VA 23666: an 8-bit microcomputer CPU based on the Intel 8080A, which interfaces directly with memory and I/O modules, requiring no buffering; up to 64K of memory in 1K- and 4K-word increments of

Let's talk about a way for you to save hours in microprocessor software debugging.

HP's 1600S Logic State Analyzer, in the MAP mode, lets you examine the unique "fingerprint" of every logic system.

In the TABLE mode, the 1600S displays up to 16 lines of code, with their sequential relationships in familiar logic notation.

I mean many hours of savings if you've ever had this problem: You've just finished your prototype microprocessor-based system, made the preliminary checks on the hardware, and loaded the program in RAM. You hit the start button. Everything's running smoothly, then wham! You're out of business. Things are out of sequence and the system is doing things you never intended. Now you could be in for hours – or even days – of troubleshooting.

But let me tell you about a much faster way to spot software problems... with HP's 1600S Logic State Analyzer. This instrument lets you look inside your operating circuit – right on the buses and qualifier lines – and see program implementation. That's the fastest way I know to locate software problems in operating circuits. Actually, the 1600S gives you two ways to view program flow:

Mapping. This is a dynamic view of your system's operation... a pattern of dots and lines that are unique for each program. Each dot is a specific data word. It's location indicates binary magnitude, and its brightness indicates relative frequency of occurence.

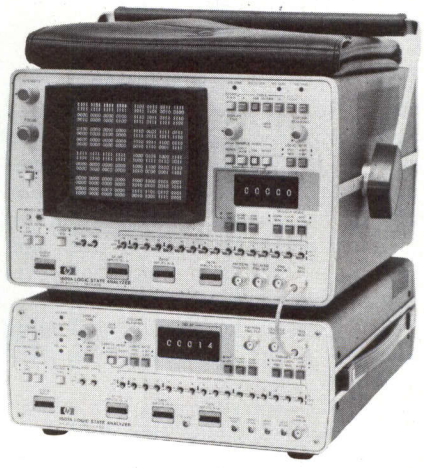
You might call the map a personal fingerprint. It's different for every program. With a little practice, you can easily spot a suspicious pattern and locate the word or group of words that could be the trouble source. Then you simply position a cursor over the word in question and push a front-panel switch to go to the Table display mode.

Table. The CRT now gives you a display of word flow using the word you selected as the trigger point. It displays up to sixteen 32-bit words at one time... in familiar One's and Zero's. You can look at events leading up to, surrounding, or following the trigger word. And even delay up to 99,999 clock cycles beyond the trigger point to view events anywhere in your program.

Suppose your problem is an erroneous data word that causes an unwanted jump. Mapping helps you spot the jump, and the Table mode lets you quickly compare each data word leading up to the jump with your written program.

That's just a simple example. HP's 1600S Logic State Analyzer, priced at $6800*, can speed more complex software debugging problems too. We'd like to tell you more. And HP has arranged a number of seminars to make that possible. Find out how to attend one in your area by calling your local HP field engineer. He can also supply you with complete spec sheets and application notes detailing the use of mapping for troubleshooting minicomputer and microprocessor systems. You'll discover an exciting new concept in digital troubleshooting.

*Domestic U.S.A. price only.



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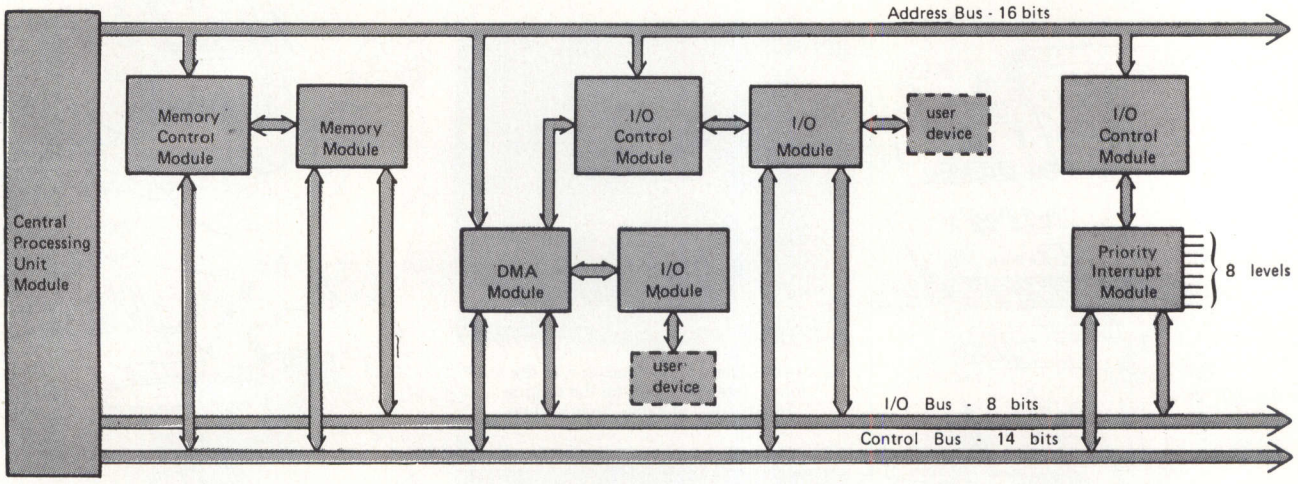

Typical configuration of μP series. Microcomputer system may include any combination of from one to five memory and/or I/O control modules without additional buffering; any combination of up to eight 1K or 4K RAM, or 256 RAM/1K ROM modules may be interfaced to a single memory control module

RAM, and RAM/ERPROM modules, with maximum read/write time of 1.05 or 0.50 μs; and memory and I/O control.

Among the other modules are analog I/O variations, all adjustment free over the normal commercial operating temperature range (0 to 70°C). They feature 8-channel programmable gain, 8- or 12-bit ADC; 8-channel programmable gain differential amplifier, with internal calibration feature; and 8- or 12-bit DAC. Digital I/O module features include RS-232-C interface for remote serial communications, general-purpose instrument bus per IEEE Std 488-1975, and 8-bit buffered I/O. Still other modules include program maskable priority interrupt with eight discrete levels, and DMA for direct transfer of data to or from memory without CPU intervention.

Circle 174 on Inquiry Card

μComputer Package Serves as Training/ Evaluating Device

Offered as a complete package consisting of an assembled and tested microcomputer employing the RCA COSMAC 1802 processor, training aids, and user manual, UC 1800 is completely self-contained and designed to allow maximum ease of use. Unit can be used as a training device in construction and use of computers, as well as a device for evaluating microprocessor applications in new products.

An OEM version also is available from Infinite Inc, PO Box 906, Dept CPNR, 151 Center St, Cape Canaveral, FL 32920 as a single board microcomputer with or without onboard power supply. It includes full military temperature range, low power CMOS, single 3- to 15-V supply, and TTL compatibility.

Features of the processor include bidirectional 8-bit common bus for I/O and memory, crystal-controlled single phase clock, software usable flags for I/O operations without interrupt, 91-instruction capability with variations to 226 instructions for efficient data movement, and 5-μs instruction execution time. Microcomputer also has built-in keyboard programming.

Expansion to 65K bytes is possible with 16-bit multiplexed address; 256 bytes of R/W memory are provided on board. Direct control feature allows simple control of 14 I/O devices; four I/O flag capability and direct memory access allow data transfer rates of 400K bytes/s. There also is parallel and serial I/O data line capability.

Bus structure of the unit features memory address bus (8-bit multiplexed to 16-bit), and 8-bit memory and I/O data bus. Timing, clock, state codes, I/O command, and memory R/W lines are buffered. Display is LED digital (hexadecimal) for address, memory contents, and I/O port.

Operating from a single power supply, unit requires 120 Vac, 50 to 60 Hz, 25 W; 120/230 Vac, 50 to 500 Hz input power is available as an option. Price of complete package is $495; CPU board alone is $179.

Circle 175 on Inquiry Card

Multiprocessing Capability Features Shared Memory

In the multiprocessing technique introduced by IMS Associates, Inc, San Leandro, Calif for use with the IMSAI 8080 computer, as many as six processors can be connected to

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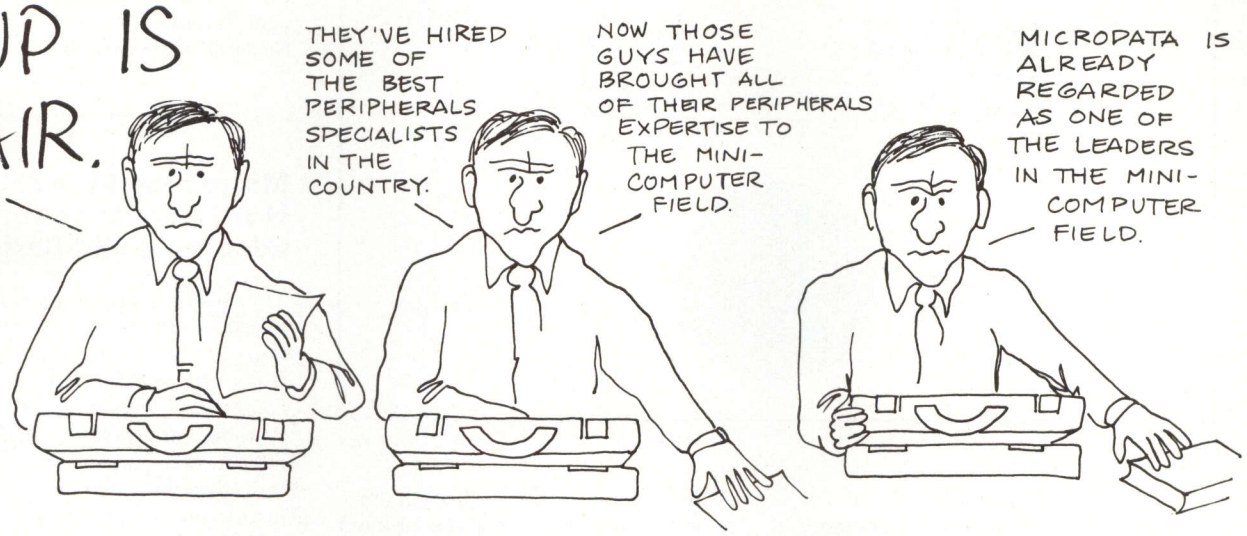

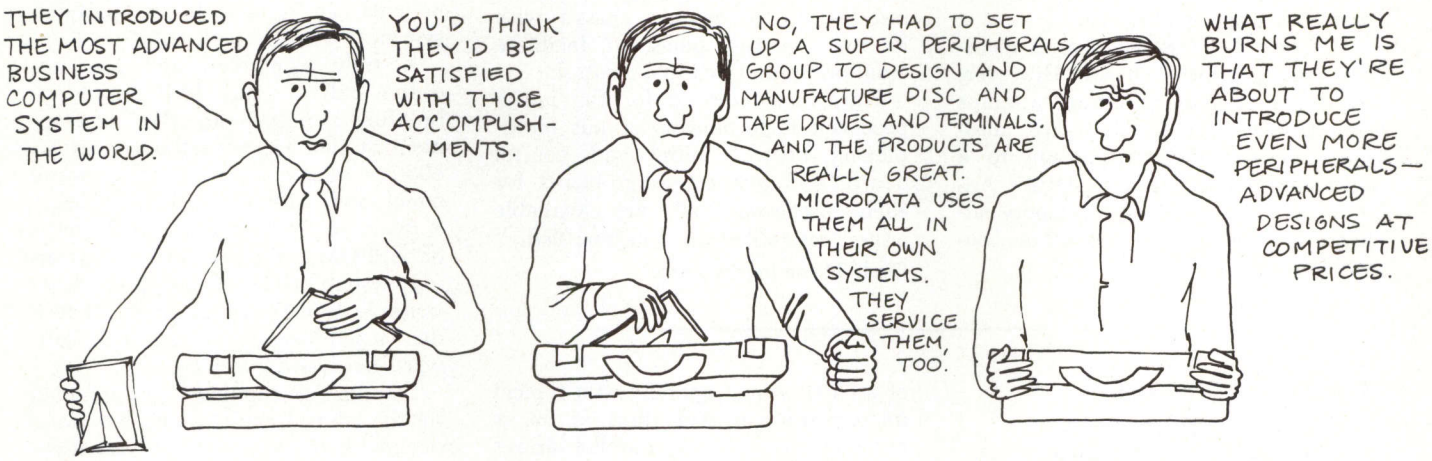

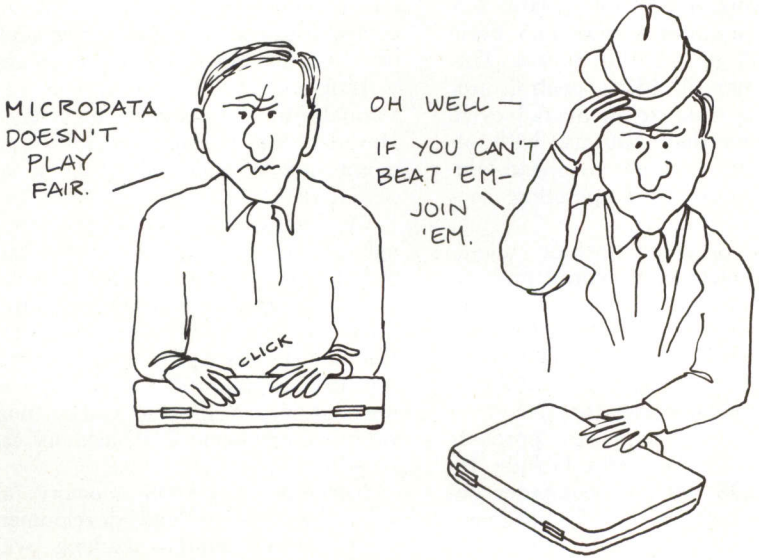

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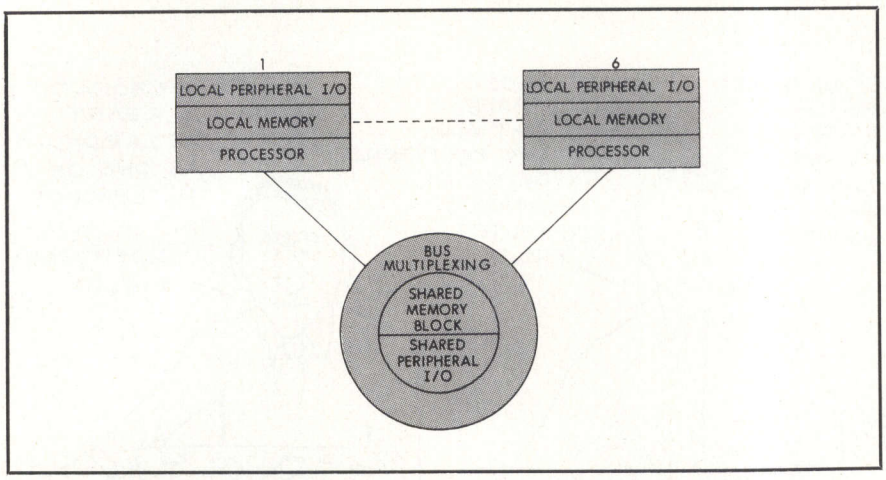


a single shared memory block (or several non-contiguous memory blocks) of the computer. Each processor can operate either independently or on a shared basis with one or more I/O peripheral devices.

Processors access the shared memory on a priority basis. However, when two or more processors attempt simultaneous access, they are automatically sequenced according to a preprogrammed priority status. Another feature of shared memory allows for semaphore resolution between processors.

Total memory allowed each processor is 64K bytes, less the amount of the shared memory block. The computer chassis has room for several processors, or each processor may be installed in a separate chassis with its own control panel to facilitate monitoring and manual control.

Hardware required for the multiprocessor logic consists of bus multiplexing board, timing and control board, and bus extension board for each processor; all are available either assembled or unassembled.

Circle 176 on Inquiry Card

Family of Bipolar Computing Elements Meets Military Specs

Series 3000 family of bipolar computing elements is now available in three full military temperature series: standard full military temperature range; MIL-STD-883, Level B; and MIL-STD-883, Level C. Standard military series, tested to many of the 883 requirements, also can be used for many severe-environment industrial applications. Level B and C series conform exactly to MIL-STD-883, Levels B and C, respectively. Specifications for all three series are guaranteed for a supply voltage of V_{cc} = 5 V ±10% over the −55 to 125°C range.

Series consists of a family of Schottky bipolar, microprogrammable devices used by systems manufacturers to build high performance central processing and control subsystems. Processing element is a 2-bit slice of a CPU, which operates at a typical microinstruction cycle time of 60 ns and can be used in parallel arrays to process data with any desired word length.

The manufacturer, Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, guarantees a minimum cycle time of 95 ns for the device. This allows a typical 16-bit central processor to operate at an overall cycle time of less than 190 ns, with allowances for system overhead delays and worst case operating conditions.

Devices provided include microprogram control unit, central processing element, look-ahead carry generator, multi-mode latch buffer, interrupt control unit, parallel bidirectional bus driver, and 4096-bit Schottky bipolar p/ROMs.

Development support products available with the series include Intellec™ MDS-800 microcomputer development system, ICE-30 in-circuit emulator, bipolar ROM simulator, universal p/ROM programmer, and other MDS-800 peripherals. Software includes the CROMIS cross microassembler, ICE-30, ROM-SIM, and Intellec resident packages. Training courses for engineers and programmers are also provided.

Circle 177 on Inquiry Card

Microcomputer Provides Hardware Base for Both Education and Design

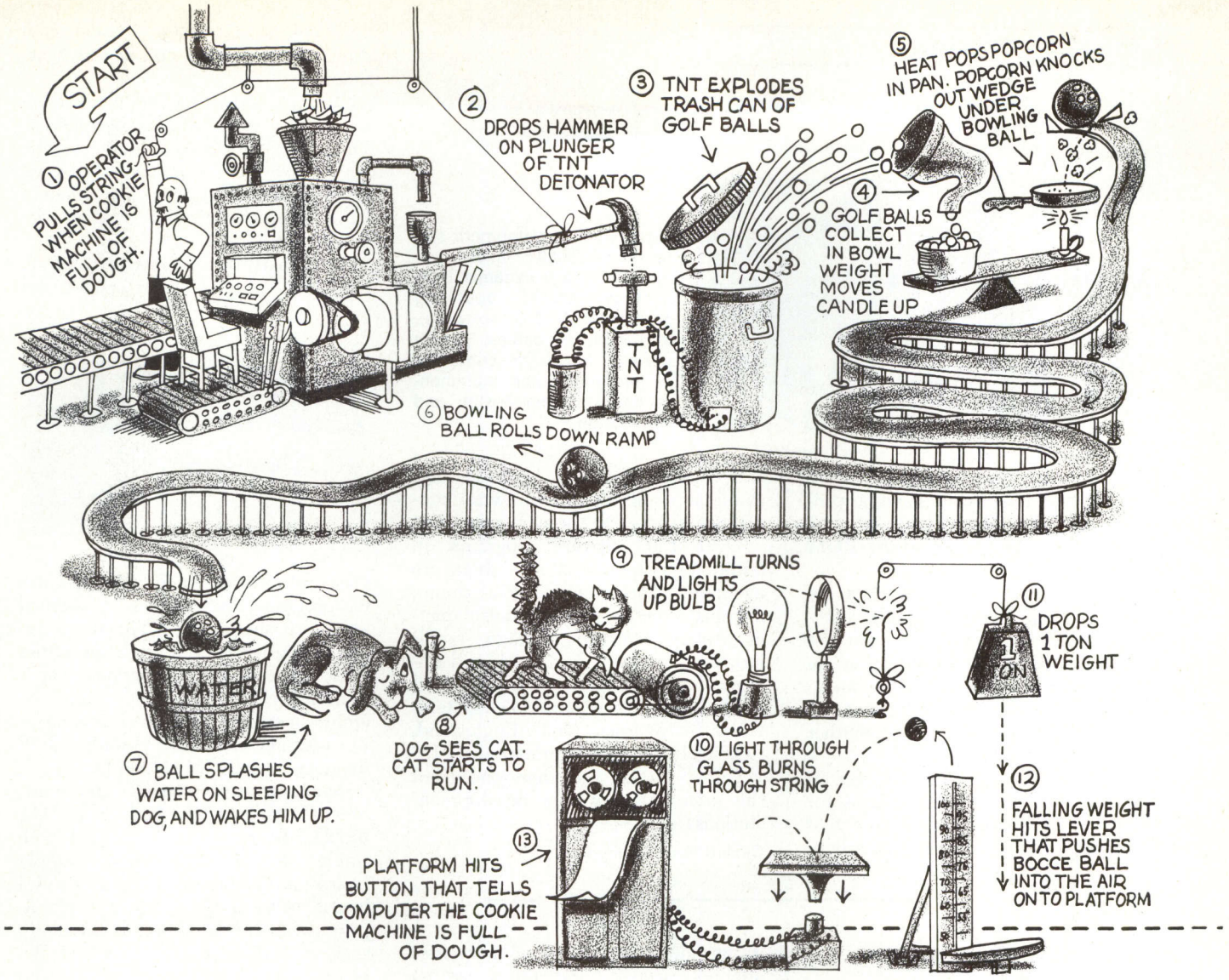
The 8080+ Development Station, a microcomputer system, gives the system designer hardware continuity from the earliest phases of microcomputer implementation through systems production. Based on the 8080A microprocessor, it allows system designers to gain an education in microprocessors, experiment in the lab, develop a prototype system, and go into production using the same basic hardware throughout. All components can be used in an upgraded system.

A fully assembled unit that requires only 5- and 12-V supply to be fully operational, the development station includes the company's 8080+ microcomputer with control panel and wirewrap section, 16K x 8 dynamic R/W memory, 512 words of EPROM, and the 8080+ operating system (loaded in 4K x 8 of writable ROM), which includes resident assembler, editor, and TTY software/hardware interface.

Debugging capability is provided by the control panel which has hexadecimal-entry keyboard, 16 function-control keys, status indicators, and 4-digit hexadecimal address/data display. The user can load any register or memory location with op codes, addresses or data; access and/or alter memory and registers; run a program at full speed; or step through one instruction at a time. Hexadecimal readout provides easy monitoring of either loaded or accessed data.

By adding a teletypewriter terminal (interface is provided on the control panel), programs can be loaded by paper tape, and the user can program in mnemonic codes. Standard station provides 14K of usable memory (2K is required for the operating system). Additional CMOS nonvolatile or dynamic R/W memory can be added up to 64K.

Non-volatile CMOS memory allows the user to load development programs as though working with



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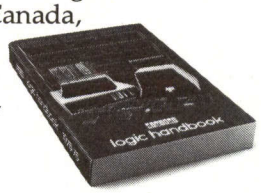

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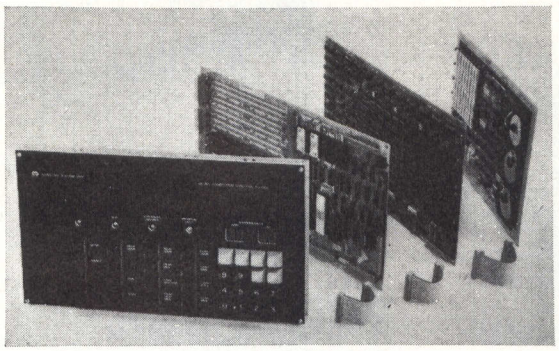


Included in development station are 8080+ microcomputer, 16K x 8 dynamic R/W memory, 8080+ operating system (with TTY software), and three I/O cables. System permits hardware continuity of microcomputer implementation in system design and production

R/W memory, then strap out "write access," and effectively have a programmed ROM. Memory also can be divided into strappable RAM/ROM combination.

Battery backup provides data retention for up to three months without system power, so power outages and system shutoff do not result in data loss. Additionally, CMOS memory can be programmed in one location and transported to another without data loss.

The single board microcomputer includes a 5 x 7" wirewrap area for customizing designs in development or production. All address/data lines and signal lines are buffered and available on six 26-pin wirewrap connectors adjacent to the wirewrap area.

Over 150 software programs, in addition to the operating system, are available. They include load/dump, memory exerciser, page, control panel display, start-up package, familiarization package, and math and numerical subroutines.

Designed by Monolithic Systems Corp, 14 Inverness Dr E, Englewood, CO 80110, system is priced at $1976 (claimed to be less than one third the price of equivalent development stations).

Circle 178 on Inquiry Card

Dedicated µProcessor Is Designed for Industrial Control Use

Dedicated program principle of the 7150 microprocessor allows complete automation of industrial controls and home appliances. Designed in p-channel silicon gate MOS technology, the device controls machine events in a sequential manner.

It combines advantages of electronic control with flexibility gained from using ROM techniques. Memory is factory programmed to specific user needs; up to 10 machine functions can be controlled through as many as 20 different program steps. A wide variety of systems can be controlled by the same basic circuit through program changes.

Functionally, the device fits between a general-purpose microprocessor and a custom designed circuit but with a lower component count than a general-purpose microprocessor. It also includes some input and output logic and linear circuits for sensing. There are no complex clock generators to set up, as its operation is partially static. External memories are not needed, and there are no software development costs.

Working with a timing diagram, ITT Semiconductors, Commerce Way, Woburn, MA 01801 can design a memory for the microprocessor to fit user needs. Circuit is available in plastic or ceramic 24- or 18-pin DIPs.

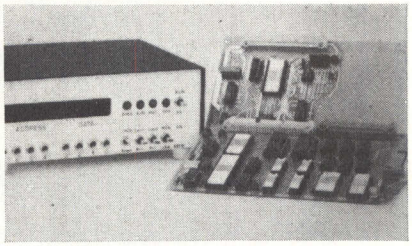
Circle 179 on Inquiry Card

Single-Card Controller Includes µProcessor, p/ROM, and R/W Memory

Designed for dedicated applications such as process control, instrumentation, and communications systems, the MC80 microcontroller utilizes an 8080 microprocessor and is contained on a single card. It includes 256 words of static R/W memory (expandable to 512 words) and up to 2K of custom application p/ROM storage. Other features include buffered address and data lines, two 8-bit parallel I/O ports, crystal clock designed to facilitate division into standard baud rates, and 488-ns cycle time.

System's structure and compatibility allow full use of I/O peripherals. This also permits simulation of the device by the company's full-scale microprocessor system for efficient hardware and software systems development.

Total hardware support is offered, including plug-in front panel for



checkout, maintenance, and diagnostic programs that permit operational access to such control signals as reset, DMA, ready, and interrupt. Other front panel module functional capabilities include run, single step, examine memory, and load memory—in addition to 1K of static R/W memory for p/ROM simulation.

Available from Gnat Computers, 8869-C Balboa Ave, San Diego, CA 92123, the device is supported with single voltage source power supply board and communications control board. Also available is a general-purpose board laid out for wirewrap sockets and designed to speed development of custom interface and controller prototypes, with sockets numbered, and power and ground busing in.

Circle 180 on Inquiry Card

Evaluation Board Features Built-in Programmable Memory

A microprocessor prototyping board for hardware and software evaluation of the 6800-based microcomputer systems family in specific applications features a built-in programmer for the S6834 EPROM microcircuitry. This feature, not offered on competitive prototyping systems, provides capability in developing prototype microcomputer programs.

Available from American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051, the board can serve as a general-purpose microcomputer for low volume systems with use of up to 58 I/O lines and

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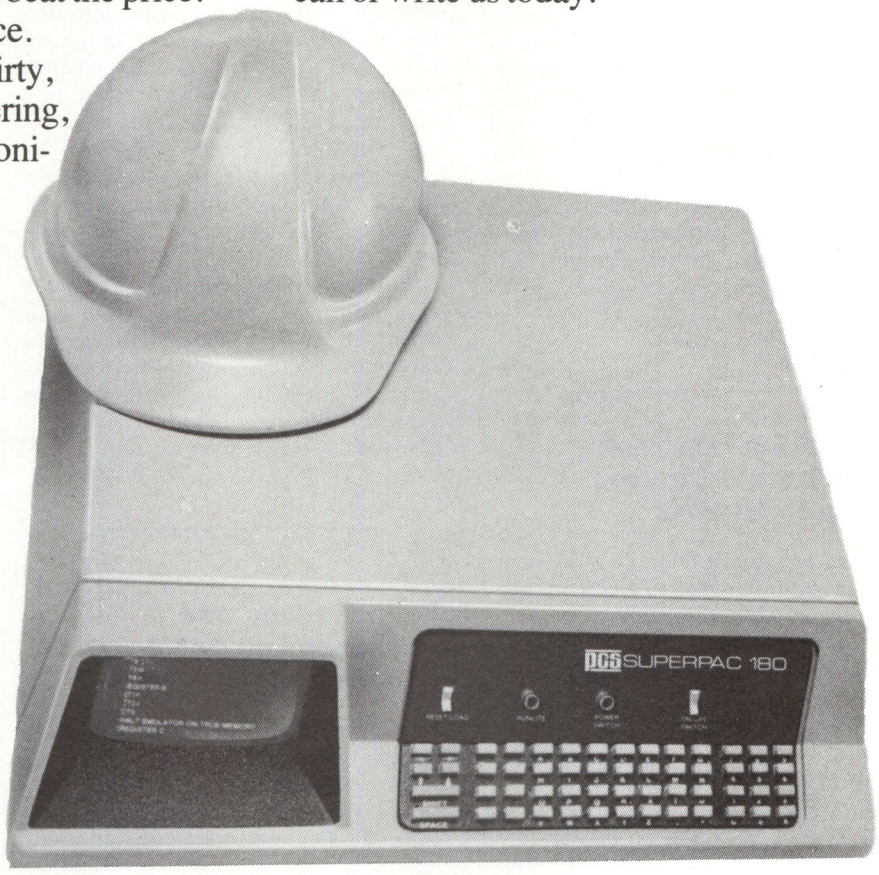

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expansion of up to 56K bytes of user-available memory. Measuring 10½ x 12″ and having two 86-pin edge connectors, it can also be used for evaluating incoming microcircuits and for programming EPROMs on a limited production basis. Communication to the board is through a teletypewriter. Computer time-sharing facilities are used to translate source-to-object code.

High level interpretive computer language called Tiny BASIC, residing in the EPROM, is furnished at no extra charge; prototyping operating system program (PROTO), residing in the ROM, is supplied with the board.

Board is available in three package options: in kit form with printed circuit board and minimum quantity of parts (EVK100—$295); expanded kit with 512-byte EPROM (EVK200—$595); and expanded kit, fully assembled and tested, having 2K-byte EPROM with Tiny BASIC (EVK-300—$950).

Circle 181 on Inquiry Card

120-Pin System Tests Complex LSI Devices At Up to 10 MHz

A computer-controlled, 120-pin semiconductor test system designed specifically for testing high complexity LSI devices such as microprocessors, calculators, and high density memories, Sentry IV offers extra power, versatility, and growth potential for advanced development programs. With the capability of testing up to 120 pins at speeds up to 10 MHz, the system facilitates testing and characterization of advanced semiconductor devices regardless of technology—bipolar TTL, DTL, ECL or MOS static or dynamic p-channel or n-channel, or CMOS.

System, introduced by Fairchild Camera and Instrument Corp, Systems Technology Div, 1725 Technology Dr, San Jose, CA 95110, offers up to 12 timing generators for data and clock timing; four additional timing generators for output strobe, each programmable from 10 ns to 10 ms with 160-ps resolution; and test periods ranging from 100 ns (10 MHz) to 40 ms (25 Hz). Using the company's 24-bit word CPU (with 16K words of main memory and 18M-bit disc) to provide power, system can accommodate complex test pattern generation and control requirements.

Extra word length (compared with 16-bit CPUs) allows reduced test time and higher system throughput. Compatible with full line of standard features, peripherals, and options, the system is functional and ready for use immediately after installation.

Two special-purpose processors are available to minimize the need for additional memory and attendant software. Sequence processor handles addresses and timing sequences for the largest devices whose range of test states and conditional branches can exceed the power of other test systems. Pattern processor can evaluate large-scale memory devices including RAMs, ROMs, and p/ROMs up to 64K bits with extensive cell patterns that must be fully exercised.

Software designed specifically for IC testing is provided. Operating software handles all system control functions, and applications software is available for virtually any type of device evaluation.

Circle 182 on Inquiry Card

Performance and Economy Are Achieved With Interface Products

A wide range of interface and logic module products for DEC LSI-11 microprocessor has been introduced by MDB Systems, Inc, 1995 N Batavia St, Orange, CA 92665. Present company products for the LSI-11 MPU include general-purpose interface, general-purpose direct memory module, and universal dual and quad wirewrap modules. Peripheral controllers are available for line printers, card readers, and paper tape equipment, as well as asynchronous and synchronous single line adapters. A programmable real-time clock is also available.

Dynamic RAM modules are in 4K, 8K, 12K, and 16K by 16 sizes, and EPROM, p/ROM, and ROM modules are available. Hardware accessories include backplane/card guide assembly, jumper cable assembly, bus terminator module, and systems monitoring unit.

Circle 183 on Inquiry Card

Low Cost Single Card Logic System Serves Control Applications

PLS-881 single-card 8-bit 8080A programmed logic system comes complete with an 8080A microprocessor, 1K of RAM storage, sockets for 4K bytes of ROM program memory, interrupt input, crystal clock, power-on and external reset, three 8-bit TTL output ports, and two 8-bit TTL input ports. Design features include simplicity and small size; cards measure 4.5 x 6.5″ with 56-pin card edge connectors on 0.125″ centers and will fit into standard card racks.

According to Pro-Log Corp, 852 Airport Rd, Monterey, CA 93940, all parts used in system construction are either currently second-sourced or soon will be. After purchasing 250 cards, customers receive a free set of manufacturing plans allowing them to build the system in-house.

Circle 184 on Inquiry Card

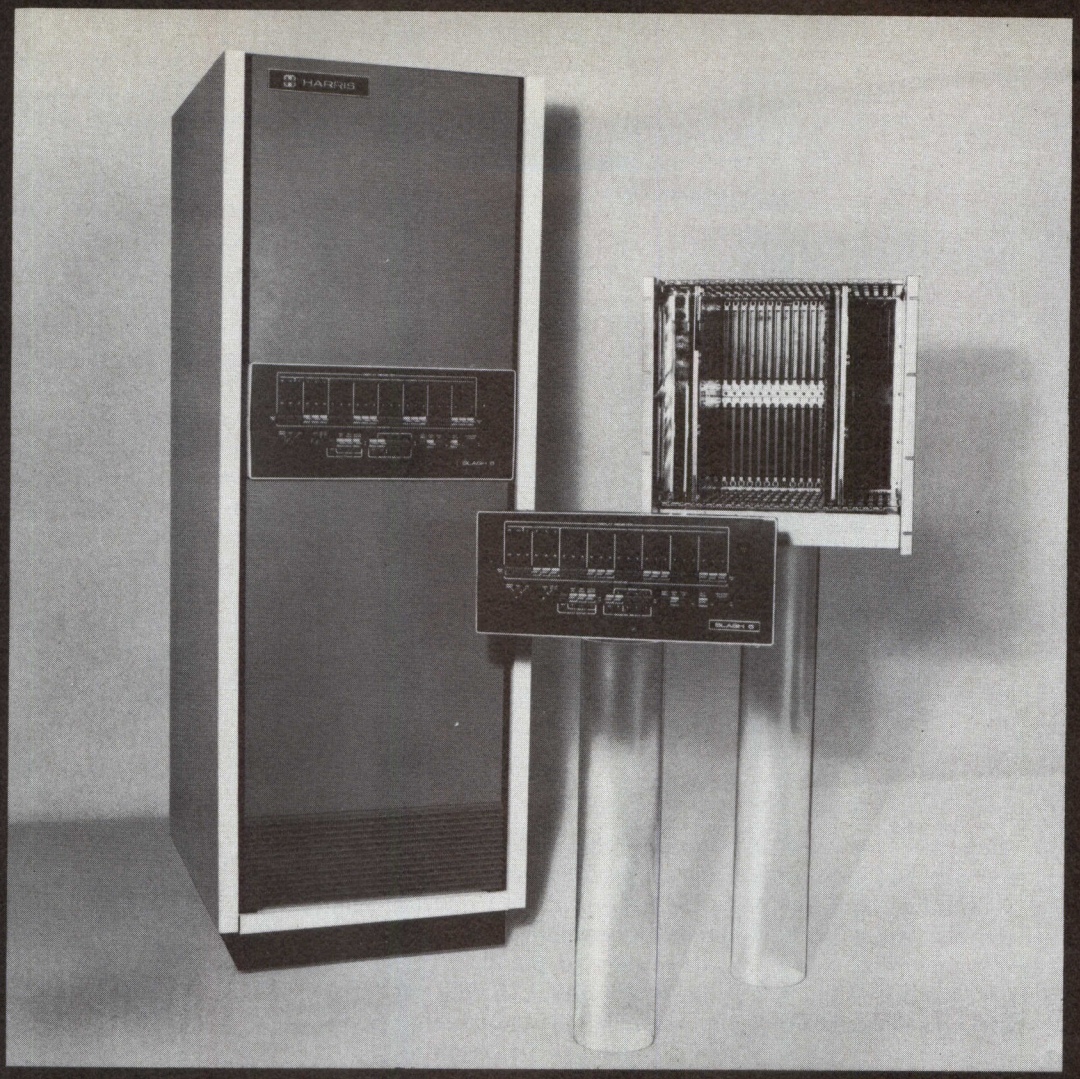
Static RAM Is Designed for Byte-Oriented CPU System

A 64 x 8-bit n-MOS static RAM, TMS 4036 is designed to provide minimum cost per package count for terminal and controller systems requiring 128 words or less of RAM. Organization of the device matches needs of byte-oriented CPU systems such as TMS 8080 or 9900. Like those systems, the RAM has a common I/O bus which is fully TTL compatible. Address, R/W control, output enable, and chip enable are TTL compatible.

Unit, from Texas Instruments Inc, PO Box 5012, Dallas, TX 75222, interfaces directly with the 8080. Providing easy memory expansion in a convenient 64-word increment, 3-state output buffers provide a fan-out of one series 74 TTL load and OR-tie capability.

RAM is rated for operation over the 0 to 70°C temperature range, and is supplied in a compact 20-pin 300-mil wide plastic or ceramic DIP. Three speed ranges (1-μs, 650-ns, and 450-ns access and read or write cycle time) optimize performance for a variety of system needs.

Circle 185 on Inquiry Card □



Announcing the Harris Slash 6. Supermini performance. At super minicost.

If you recognize optimum price/performance value when you see it, you should see our new SLASH 6. It outperforms most 32-bit minis, at a price that's better than many 16-bit minis.

The Harris Slash 6 costs only $14,500*. You get 600 nanosecond cycle time; 48KB of MOS memory with error correction; hardware multiply, divide, and square root; 8 priority interrupts; and a turnkey control panel.

You get building-block architecture that lets you expand your systems as your needs expand. And sophisticated real-time software that no other machines offer in this price/performance range.

The Harris Slash 6. The first truly low-cost/high performance computer for all of you who were waiting for optimum price performance value. Harris Computer Systems, 1200 Gateway Dr., Ft. Lauderdale, FL. 33309. Europe: Techmation N.V., Gebouw 105/106, Schiphol-Oost, The Netherlands.

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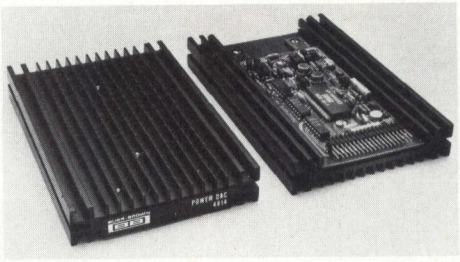
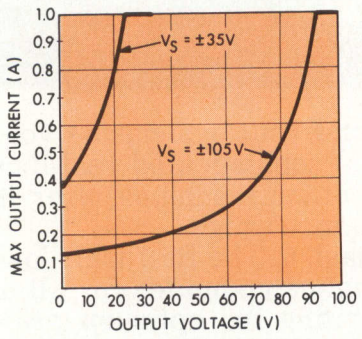
PRODUCT FEATURE

Power DACs Provide Programmable Voltages for Minicomputer-Controlled Test Equipment



Digitally programmable voltages required for automatic test equipment or servo applications can be supplied cost-effectively by a pair of devices that combine digital-to-analog converters with power output stages. Power DAC models 4814 (binary input coding) and 4815 (BCD input coding) can provide a ±100-V output swing with a minimum of 100 mA at all output levels and up to 1.0 A at higher output levels. Variations in output voltage within the rated range can be obtained by changing the input code. Typical applications are in testing PC board assembly or discrete semiconductor breakdown voltage.



As shown here for supply voltages (V_s) of ±35 and ±105 V, the power DACs deliver a minimum of 100 mA over the entire output range with current capability increasing as output voltage increases. Maximum current of 1.0 A is reached at full output voltage

Resolution of the Burr-Brown devices is 13 bits (12 data bits plus sign bit), allowing the output absolute value to be retained while reversing its polarity with only one input change. Digital input storage eliminates critical timing requirements. Data are transferred to the digital-to-analog converter (DAC) on the positive-going edge of a strobe pulse; to eliminate output glitches, digital input and sign bit are separately strobed.

Description

Each device is made up of a 13-bit digital input buffer (storage register) with strobed input, 12-bit DAC, and power output amplifier. Interfaces are provided for minicomputer control.

The digital input storage register consists of 13 IC, positive-edge-triggered flip-flops using TTL circuits. Although logic level transfer from the register inputs to the DAC occurs on positive-going edges of the strobe pulses, strobing occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When strobe inputs are at either high or low level, inputs have no effects on DAC inputs. Strobe and register are fully compatible with TTL or DTL circuits.

Digital output from the storage register is accepted by the DAC in 12-bit increments and converted to a unipolar output signal. Total accuracy is ±0.025% of full scale reading on the ±100-V scale; gain drift is <±70 ppm/°C. Maximum settling time to within 0.01% of final value for any input change is 100 μs. Offset error is ±10 mV. If improved performance is desired—beyond these specified guaranteed accuracies—trim potentiometers on the DAC may be externally adjusted to null offset and gain errors.

Full scale output ranges of less than ±100 V—still with 13-bit resolution—can be obtained by adding one external resistor. A factory-limited typical current output of 120 mA can be altered by changing two accessible resistors.

Maximum power dissipation is 10 W in free air without heat sink. At the 120-mA current limit, the power DAC is short circuit protected indefinitely at 25°C ambient temperature. Chance of damage and equipment downtime in the event a shorted device is found during test is eliminated.

Specifications

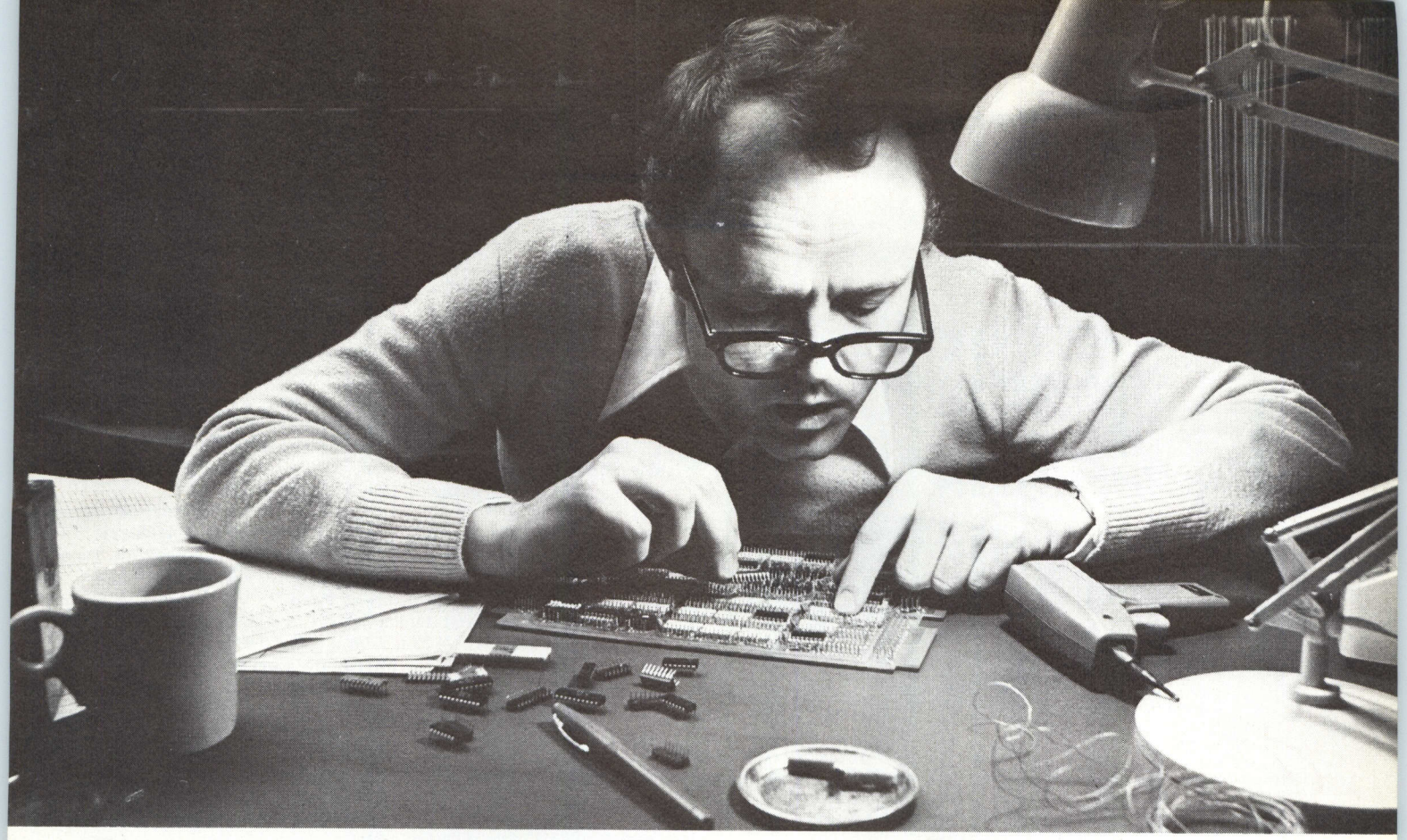
At the operating temperature range of 0 to 70°C, linearity error is ±½ LSB max, max output offset voltage is ±10 mV, and max gain error is ±0.05% of reading. Drifts are: gain, 70 ppm/°C max; output offset voltage, 160 μV/°C max; differential linearity, ±2 ppm/°C max; and current limit, ±2 mV/°C typ. Power supply sensitivities are ±0.02% of FSR/%V_S for 15 V; 0.002% of FSR/%V_S for −15, 5, and ±105 V.

Units are 0.88″ high and designed for PC board mounting. From 10 to 15 units can be mounted on a single 19″ rack.

Price and Delivery

Pricing for the 4814/4815 power DACs is $249 each for quantity 1 to 24, $224 for 25 to 99, and $198 for 100 to 249. Delivery for production quantities is 4 weeks ARO. Burr-Brown Research Corp, International Airport Industrial Park, Tucson, AZ 85734. Tel: (602) 294-1431

For additional information circle 199 on inquiry card.



Buy our boards now if you want to stop buying them later.

If you're thinking of making your own microcomputer boards sometime in the future, ours are the only boards to buy right now.

Because the chips on our microNOVA boards are the same ones you can buy in the microNOVA chip set.

Which means you can switch from microNOVA boards to our microNOVA chips anytime you want.

The microNOVA board is a full 4K microcomputer. With a number of standard features. Like power-fail/auto-restart. Real-time clock. NOVA instruction set with hardware stack. Hardware multiply/divide. Data channel logic.

Yet all the above computer costs only $589, in OEM quantities of 100.*

Which is a lot of computer for a little money.

Because it's a NOVA computer, the microNOVA board comes with powerful run-time software. Like RTOS, our NOVA-compatible, field proven realtime executive. And it runs both Assembler and FORTRAN.

And because the microNOVA board comes from Data General, it comes with the manuals, technical publications, services, training courses and seminars you'd expect from a large minicomputer company.

Yet the microNOVA 4K board is only one member of an entire family. Besides the board (and all the supporting boards), you can get complete development systems. Or you can get completely packaged MOS minicomputers. Or chip sets that include the mN601 CPU, plus all the supporting chips.

So if you want to end up in the chips, call our toll free number, **800-225-9497.** (Unless you're in Massachusetts. In which case, call 1-617-485-9100, EXT. 2509.)

microNOVA:
A giant reduction in the NOVA line.

DataGeneral

Data General, Route 9, Southboro, Mass. 01772 (617) 485-9100. Data General (Canada) Ltd., Ontario.
Data General Europe, 15 Rue Le Sueur, Paris 75116, France. Data General Australia, Melbourne (03) 82-1361
*Prices quoted are FOB Southboro and apply to the U.S. Taxes excluded. NOVA is a registered trademark of Data General Corporation.

CIRCLE 61 ON INQUIRY CARD

PRODUCTS

Cartridge Tape Drive for Microcomputer Applications Offers 11.6M-Byte Storage Capacity

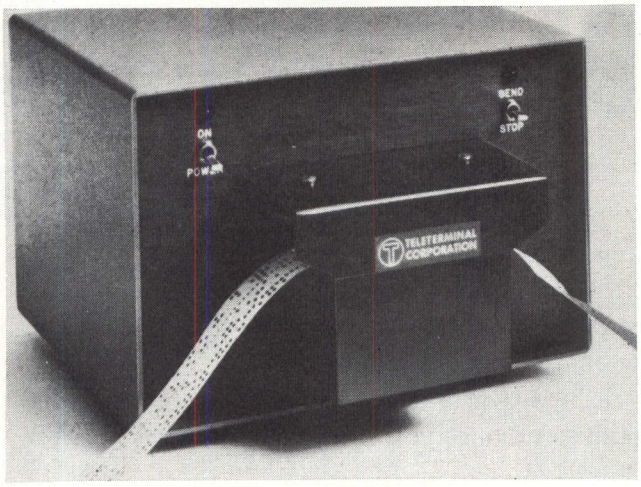
Serial 4-track recording density of 6400 bits/in. on the Lodestar™ drive, claimed to be more than double that previously offered, provides 11.6M-byte storage capacity on a 3M-type data cartridge. The drive features an industry standard interface, and an available formatter provides plug and software compatibility with existing controllers designed for reel-to-reel transports. Write and read occur at 30 in./s and search is at 90 in./s. Data transfer rate at 6400 bits/in. is 192 kHz. Reverse read capability is std. Full tape write requires 10 min.; full tape read requires 8 min. bidirectional, 10 min. forward only. Nom start/stop times are 25 ms at 30 in./s and 75 ms at 90 in./s. Interrecord gap is 1.2″ min, 48″ max. Error rate is <1 bit in 1 x 10^8 bits. Able to meet military specs, the 4.25 x 6.96 x 10″ drive has a MTBF of 2000 h and MTTR of ½ h. **Microdata Corp,** 17481 Red Hill Ave, Irvine, CA 92714.

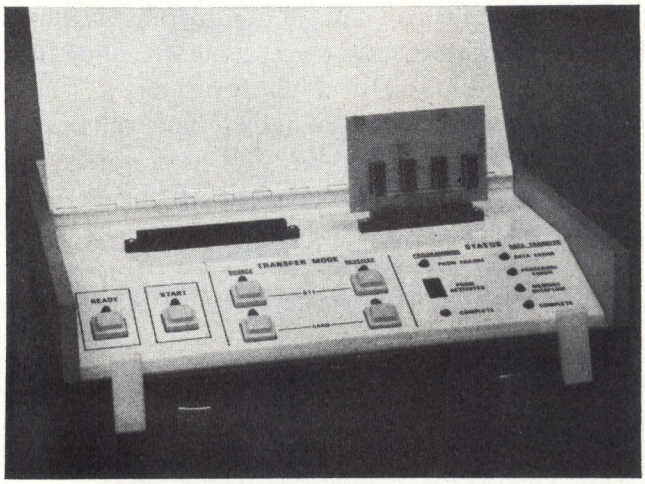
Circle 200 on Inquiry Card

Paper Tape Reader Interfaces With Most Mini or Microcomputers

A 300-char/s paper tape reader which will read any std 1″ tape having a transmissivity of <60%, Fly Reader 232 can be plugged directly into the RS-232 or TTY port of most mini or microcomputers. Using the computer's TTY loader software, the reader will load programs 30 times faster than the TTY. In addition, it can be used with serial TTL interface. PC board jumpers permit the TTY interface to be either passive or 20-mA active, enabled or disabled, and permit choice of remote control modes. Positive traction and gentle handling of a 7-tooth precision sprocket allow >1M passes without noticeable tape wear or tearing. The integral stepper motor/sprocket tape drive has a bearing life of >50kh. A bank of back panel programming switches permits selection of any one of 16 baud rates; 5-, 6-, 7-, or 8-bit char length; parity number of stop bits; and inhibiting or enabling of the RS-232 control signals. **Teleterminal Corp,** 12 Cambridge St, Burlington, MA 01803.

Circle 201 on Inquiry Card





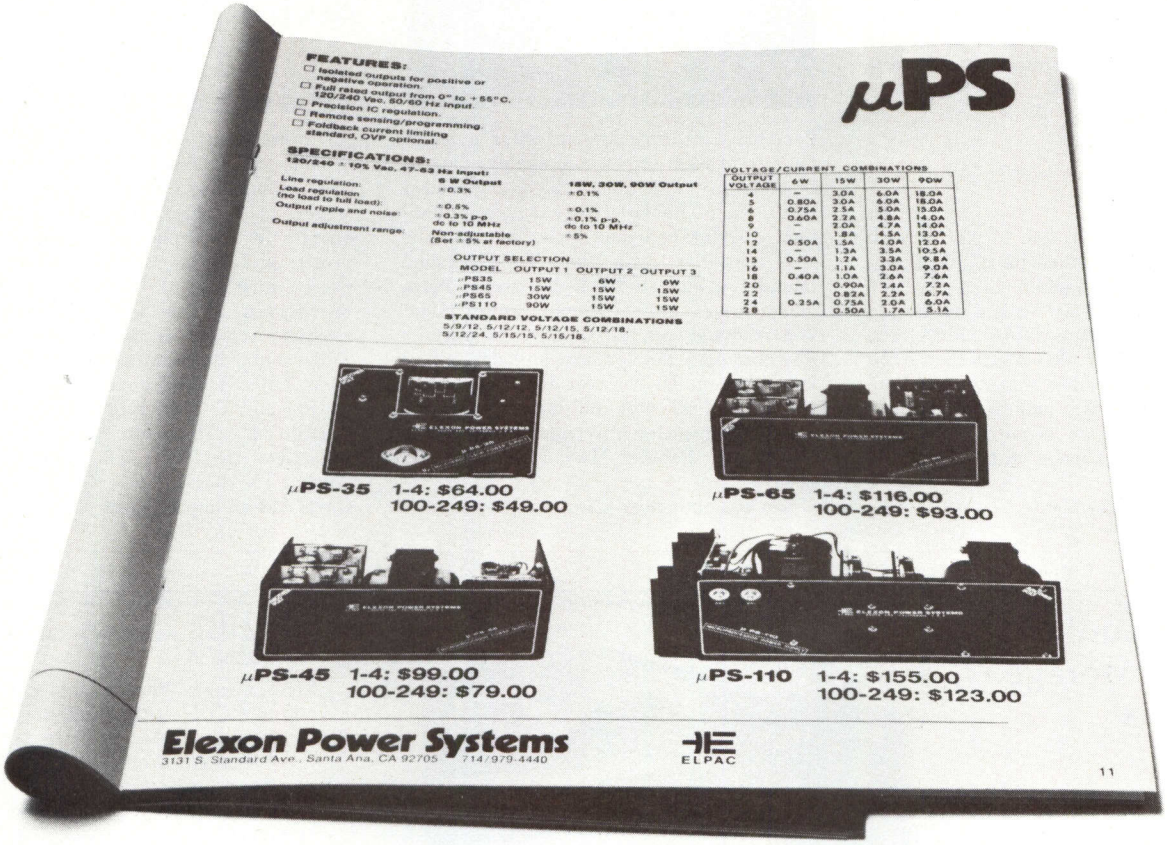
Programmable Control System Sequencer Performs All Functions of Conventional Relay Control Panel

Expansion of the company's programmable control system family to include a larger sequencer with a memory capacity of 1K words enables replacement of control systems having up to 200 relays. Sequencer 5TI 102 handles all functions performed by conventional relay control panels including sequencing, timing, and counting, and processes logic functions internally. Industrial users familiar with relay logic will be able to enter instructions directly from a relay ladder diagram. The sequencer will also accept logic elements or Boolean algebra. Fewer words of memory are used than by programmable controllers. Up to 50 timers and counters are programmable; instructions require only three words of memory. Counters have up/down capability with a max capacity of 32K counts each; timers can be incremented at intervals of 8.3 ms or 0.1 s with a max capacity of 54.6 min. each. **Texas Instruments Inc, Control Products Div,** Attleboro, MA 02703.

Circle 202 on Inquiry Card

49 REASONS TO GET UGLY™

1. Intel 4004
2. Intel 4040
3. National 4040
4. Rockwell PPS-4
5. National PPS-4
6. Rockwell PPS-4/2
7. Rockwell PPS-4/1
8. Fairchild F-8
9. Mostek F-8
10. Intel 8008-1
11. Intel 8080 A
12. AMD 8080 A
13. T.I. 8080 A
14. NEC 8080 A
15. Siemens 8080 A
16. Intel 8048
17. Mostek 5065
18. Motorola 6800
19. AMI 6800
20. National SCAMP
21. RCA 1801
22. RCA 1802
23. Rockwell PPS-8
24. National PPS-8
25. Rockwell PPS-8/2
26. Signetics 2650
27. Motorola 2901
28. Raytheon 2901
29. Fairchild 9400
30. Intel 3002
31. Signetics 3002
32. Zilog Z-80
33. Intersil 6100
34. Harris 6100
35. Toshiba TLCS-12
36. National IMP-16
37. National PACE
38. PanaFacom PFL-1600A
39. Texas Instruments TM-9900
40. Advanced Micro Devices 2901
41. MOS Technology 6502
42. Texas Instruments TM-1000
43. Electronic Arrays EA 9002
44. Scientific Micro Systems 300
45. General Instruments CP 1600
46. Western Digital MCP-1600
47. Monolithic Memories 6701
48. Motorola 10800
49. Texas Instruments SBP0400



By now, you've probably got the idea:

If you've got a microprocessor chip, kit or system, one of our UGLY dc supplies was made for you.

They've got the right voltages. The right currents. The right specifications.

And definitely the right price, because we've concentrated on making them perform instead of making them pretty. All our modular dc supplies are fabricated in a manufacturing plant that meets the quality requirements of MIL-I-45208A. Raw materials and components are full-rated to 85°C. Electrostatically-shielded transformers are all vacuum varnish-impregnated and 100% tested for high-voltage breakdown. Semiconductors are given a 100% burn-in. Reflow-soldered subassemblies are all subjected to 500 V "Hi-Pot" tests. And the finished supplies are then tested to spec under worst-case line conditions.

It all adds up to the prettiest price/performance ratio you've ever seen.

And another couple of reasons to get UGLY. Now.

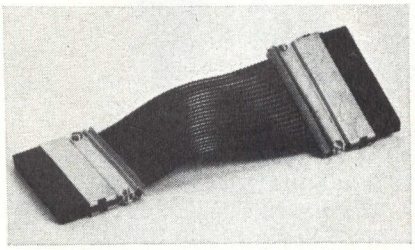
ELPAC

Elexon: the ugliest dc supplies on earth.

Get UGLY at Cramer, Newark, MIL-COMM, QPL, Ultronics, Shap Electronics, Technico, Integrated Electronics. Or call 714/979-4440 today.

PRODUCTS

COAX RIBBON CABLE ASSEMBLIES



Assemblies consist of individual coaxial cables each encased in a PVC jacket, allowing the cable to be cut to any length, maintaining exact positioning of the center conductor and drain wire. Preterminated assemblies are available in lengths from 6" to 10 ft with 0.100 x 0.100" receptacle connector centers for 50, 75, and 93 Ω. Multiposition connectors are made of V-0 rated, flame retardant, glass-filled nylon with gold over nickel plated beryllium copper contacts. **AMP Special Industries,** Valley Forge, PA 19482.
Circle 203 on Inquiry Card

16K ROM

Featuring max access time of 550 ns with ±10% tolerance on the single 5-V power supply, ROM is organized in a 2K x 8 configuration. MK 31000P-3 is a pin-for-pin replacement for Intel 2316A/8316A and General Instrument RO-3-8316A. Circuit is TTL compatible, has max power dissipation of 330 mW, and is completely static (no clocks are required). **Mostek Corp,** 1215 W Crosby Rd, Carrollton, TX 75006.
Circle 204 on Inquiry Card

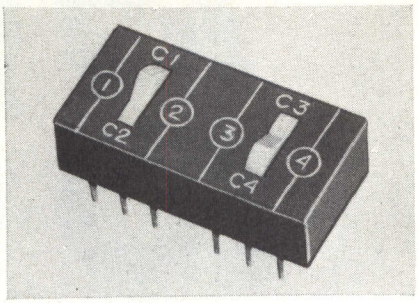
MINIATURE SLIDE SWITCHES

PC mounted switches use switch mechanism with a difficult tease which provides 4-A/125-Vac rating. Fully insulated blue diallyl phthalate low profile case occupies minimal space. PC terminals, spaced on 0.1" centers, are epoxy sealed to prevent solder flux wicking. Contacts and terminals are supplied in silver with gold flash; gold plate for dry circuit applications is available. MSS-104 (spdt) or MSS-204 (dpdt) series is available with top or side actuator lever. **Alco Electronic Products, Inc,** 1551 Osgood St, North Andover, MA 01845.
Circle 205 on Inquiry Card

PORTABLE MASS STORAGE SYSTEM

Portable Linc tape system offers a transfer rate of 8400 bits/s, and enables data to be edited, compiled, assembled, and loaded in the field. Enclosed in a rugged aluminum carrying case and including a single-slot controller card, the PDP-11 model includes a built-in ROM bootstrap; Nova model uses auto program feature. Total system weight is 21 lb. System permits filed program development utilizing either LTOS/SOS on the Nova or RT-11 on PDP-11, as well as program loading of diagnostics. **Computer Operations, Inc,** 9700-B George Palmer Hwy, Lanham, MD 20801.
Circle 206 on Inquiry Card

DPDT DIP SWITCHES

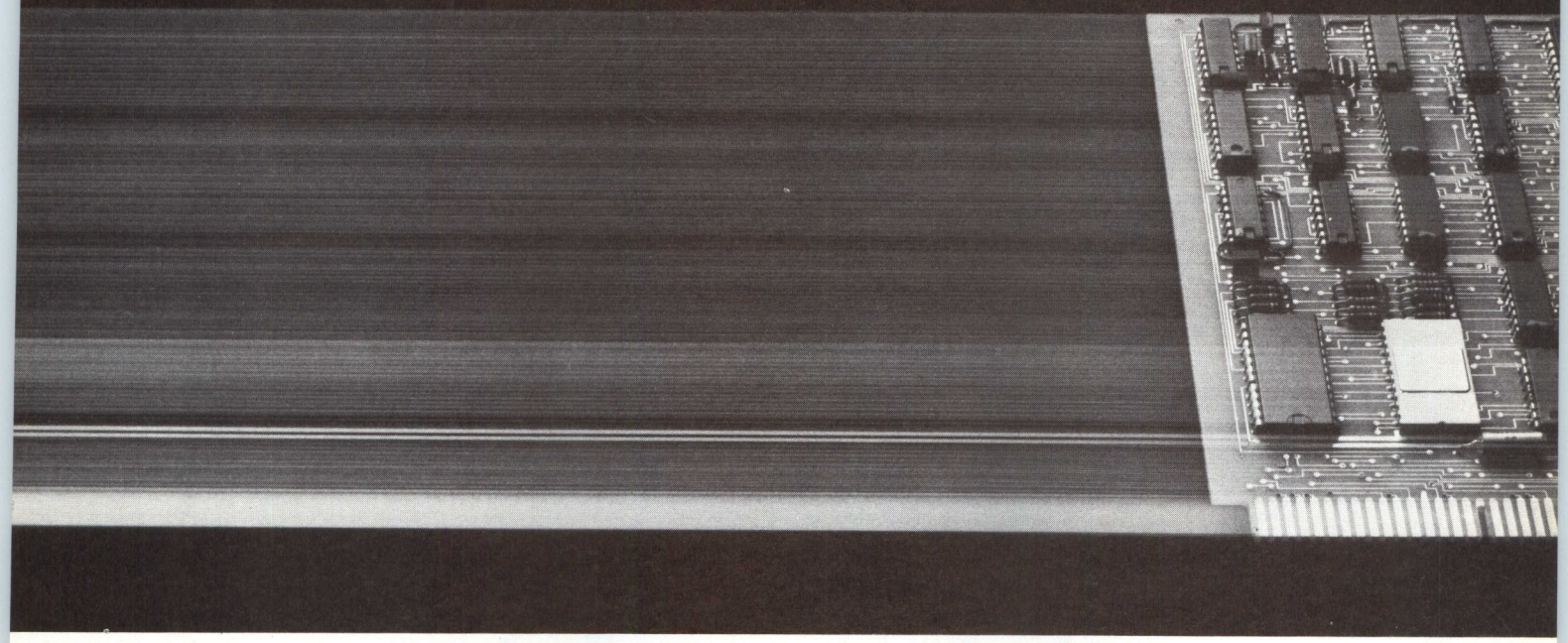


Double-Dip™, a rocker-actuated DIL switch featuring dpdt contact configuration under each rocker, is available in 1- and 2-rocker versions, both with terminals on 0.100 x 0.300" centers for compatibility with IC sockets and conventional PC board layouts. Single rocker unit is housed in a std 6-pin DIP, 2-rocker version in a 14-pin package with the two center terminals omitted. Rocker actuators are on 400-mil centers in the 2-rocker version. Switches are rated for 50,000 operations at logic levels. **Grayhill, Inc,** 561 Hillgrove Ave, La Grange, IL 60525.
Circle 207 on Inquiry Card

CMOS DIVIDE-BY-N COUNTER

A presettable counter, MC14018B is capable of dividing by any number from two through 10. Five Johnson counter stages comprising most of the circuit operate in synchronous mode but can be preset or reset asynchronously. Improved clock input circuit eliminates rise-time restrictions. Pulses with extremely long rise-time ramps can be counted reliably. Fully static, it operates up to 6.5 MHz at 10 V. Three- to 18-V operational limits, and 5-, 10-, and 15-V operation parameters are standard. **Motorola Semiconductor Products Inc,** 3501 Ed Bluestein Blvd, Austin, TX 78721.
Circle 208 on Inquiry Card

The fastest microcomputer known to man



Want to see it again?

Just call Plessey and ask about the 16-bit MIPROC 16, the first microcomputer fast enough for your real-time systems.

It has faster hardware (350 ns full cycle time).

Faster software (most instructions take only a single cycle at a throughput rate of 2.8 megahertz).

And it's months faster to get on line (no microprogramming, no hardware design and development).

For just $760 (100-qty), you get a complete high-speed computer-on-a-card that's ready to go the day you get it.

For starters, the Plessey MIPROC 16 has 82 powerful 16-bit instructions, a versatile prototype development kit and a FORTRAN IV cross-assembler/simulator for use on the Tymshare and GE Mark III networks.

Options include 75 more instructions, a DEC and Data General cross-assembler, a 1.4 μs hardware multiplier, serial and parallel I/O ports, priority interrupts, an extended temperature range (−55° to +125°C), and a ruggedized version for military applications.

So if you're still paying the price of hardwired logic just to get speed, ask for details and a demonstration of the Plessey MIPROC 16.

We've just brought microcomputing up to speed.

Plessey Microsystems

United States, Irvine, CA (714) 540-9945
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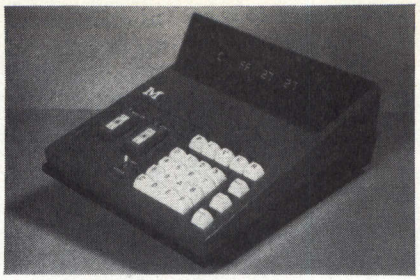
CHECK OUT THE MIPROC 16 IN OUR HOSPITALITY SUITE AT THE HOLIDAY INN ACROSS FROM THE CONVENTION CENTER DURING WESCON

PRODUCTS

p/ROM PROGRAMMER

Microprocessor-controlled series 1000 offers fully interactive operation in any of three programming modes: keyboard entry, terminal control, or remote computer control. A 32K-bit buffer RAM permits reliable data transfer and allows the user to edit data in RAM from the keyboard prior to actual programming. A 14-digit hexadecimal display gives four digits each of

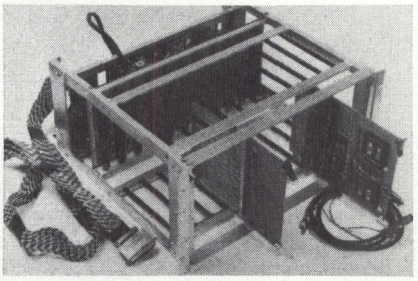


address, copy p/ROM data, and master p/ROM data, plus a 2-digit entry and error code. **International Microsystems, Inc,** 122 Hutton St, Gaithersburg, MD 20760.
Circle 209 on Inquiry Card

BAR CODE PRINTING SYSTEM

A turnkey label printing system, model 7605 is capable of generating sequential bar codes either manually or remotely on command from a host computer. System consists of impact printer with microprocessor-based controller/communication interface, keyboard, and miniperipheral options. With the keyboard, an operator can enter desired label/forms information and numeric components of the initial bar code; the printer uses automatic incrementing to generate as many sequential codes as are requested. **Micro-Pro, Inc,** 122 S Taft Ave, Chalfont, PA 18914.
Circle 210 on Inquiry Card

COMPUTER INTERFACE KIT



Kit allows interfacing any Data General Nova or Eclipse computers through a chassis containing customer designed boards, company's boards, or a combination of the two. Basic kit consists of 21-slot chassis with motherboard and set of in/out connectors for daisy chaining; cable for computer to chassis connection; cable terminator assembly; two universal wire-wrap boards for customer designed interfaces; 5-V, 12-A power supply; and computerized wire list aids. **Data Engineering Associates,** 6330 Alder St, Houston, TX 77081.
Circle 211 on Inquiry Card

FLOPPY DISC

FD-30, a floppy disc for the Hewlett-Packard 9830A, emulates the 9830 cassette system so that no changes in existing software are required. Control commands and syntax of the cassette are obeyed, and all such programs operate without modification. Storing five to seven cassettes at the cost of one cassette, and at a much faster rate, disc provides 305K bytes of user area. Four-inch high unit is based on the latest technology microprocessor for the controller/formatter. **Infotek Systems,** 733 E Edna Pl, Covina, CA 91723.
Circle 212 on Inquiry Card

THE LOGICAL CHOICE: Third in a series

SYMMETRICAL AND UNSYMMETRICAL PULSES 0.5Hz-5MHz.

CONTINUOUS, MANUAL ONE-SHOT & EXTERNAL TRIGGER OPERATION
External triggering to 10MHz

INDEPENDENTLY-CONTROLLABLE PULSE WIDTH & SPACING
100 nanosec-1 sec in 7 overlapping ranges 10^7:1 duty cycle range

INDEPENDENT CMOS AND TTL OUTPUTS Fan-out to 40 TTL loads

SYNCHRONOUS OUTPUT GATING

100mV-10V POSITIVE OUTPUT Less than 30 nanosec rise/fall times

CSC'S DESIGN-MATE™ 4: $124.95. NO OTHER DIGITAL PULSE GENERATOR GIVES YOU SO MUCH, FOR SO LITTLE.

Sounds hard to believe... but even a brief look at Design-Mate 4's specifications proves CSC's engineers have done it again. Whatever your application—whether you're looking for precision, flexibility or just plain economy—this compact source of fast, clean digital pulses offers the performance you need... at a price that discourages procrastination.

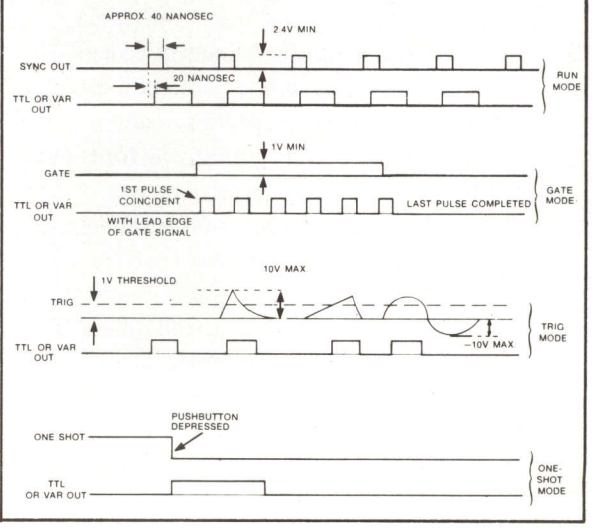
Use it as a clock source, delayed pulse generator, synchronous clock, manual system stepper, pulse stretcher, clock burst generator or in dozens of other applications. Use it alone or in tandem with other DM-4's for gated control. The wide range of controls and multiple outputs give you enormous versatility... plus compatibility with all major logic families, for research, design, development, quality control, production testing, maintenance, troubleshooting... you name it.

Now, read the specs that follow... and check the price again. Or better yet, try DM-4 for yourself at your local CSC distributor. Once you do, we think you'll find it's as hard to do without as it is easy to own.

For more information about CSC's other fine products, and a list of distributors, please call or write.

DM-4 SPECIFICATIONS

Frequency Range:	0.5 Hz to 5 MHz
Pulse Width and Spacing Controls:	100 nanosec to 1 sec. in 7 overlapping decade ranges. A single-turn vernier control provides continuous adjustment between ranges.
Duty Cycle:	10^7-to 1 Range: adjustable over entire pulse width/spacing range, 100 nanosec "ON" 1 sec "OFF" to 1 sec "ON" and 100 nanosec "OFF".
Operating Modes:	
RUN	0.5 Hz to 5 MHz as per width/spacing and amplitude control settings.
TRIG	DC to approx. 10 MHz.
Input requirements:	Sine waves 2 VP-P; pulses 1 V peak, >40 nanosec wide; maximum input ± 10 V. (Input Impedance: Approx. 10KΩDC coupled.)
GATE	Synchronous gating. Leading edge of gate signal turns generator "ON". Last pulse is completed, even if gate ends during pulse.
Input requirements:	Same as "TRIG" Mode.
ONE-SHOT	Pushbutton for single pulse. Output pulse occurs each time push-button is pressed.
OUTPUTS:	
VAR OUT	
Amplitude	0.1-10 V positive
Rise/fall time	Less than 30 nanosec
Impedance	400Ωmax.
TTL OUT	
Fan-out	40 TTL Loads
Sink	160 milliamps—0.8 V max.
Rise/fall time	Less than 20 nanosec
SYNC OUT	
Pulse width	Approx. 40 nanosec. Other sync pulse spec's same as TTL out.
Pulse lead time	Sync pulse leads outputs by approx. 20 nanosec.
POWER	117 VAC ± 10%, 50/60 Hz, 5 watts (220 VAC, 50/60 Hz also available, at slightly higher cost.)
SIZE (WxLxH)	7.5 x 6.5 x 3.25" 191 x 165 x 83 mm
WEIGHT	2 lbs. (0.91 Kg)



CONTINENTAL SPECIALTIES CORPORATION
EASY DOES IT

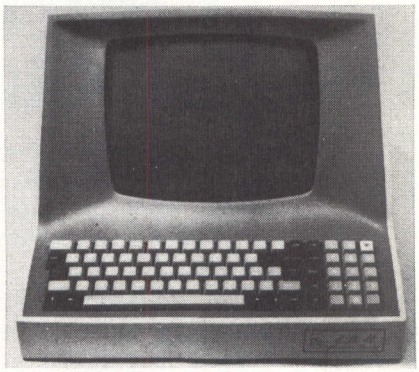
44 Kendall Street, Box 1942 New Haven, CT 06509 • 203-624-3103 TWX: 710-465-1227
West Coast office: Box 7809, San Francisco, CA 94119 • 415-421-8872 TWX: 910-372-7992
Canada: Len Finkler Ltd., Ontario

PRODUCTS

DIGITAL INDUSTRIAL CONTROLLER

A 6-decade "Decitrak" bidirectional counter-controller for caustic industrial environments, unit contains CMOS circuits and special internal filters to allow use in areas of high electrical noise. Long life LED displays, BCD outputs, and 6-decade presets are std; 6-decade setpoint control is an option. Inputs can be sine wave—300 mV pk-pk to 30 V pk-pk symmetrical to zero axis with max offset of 50 mV; square wave—150 mV to 150 Vdc positive; or pulse—150 mV to 15 Vdc positive. **Theta Instrument Corp,** 24 Dwight Pl, Fairfield, NJ 07006.
Circle 213 on Inquiry Card

CRT TERMINAL



ADM-1A has a numeric pad with period, comma, and plus and minus signs in addition to a 138-char alpha keyboard, which includes u/lc letters, punctuation, and control keys. Numeric pad is adjacent to and immediately to the right of the std keyboard to allow natural operator hand movement and facilitate numeric data entry. Keys are arranged in std calculator keypad positions. Additional features include a display format of 960 char arranged 80 char/line x 12 lines. **Lear Siegler, Inc, EID/Data Products,** 714 N Brookhurst St, Anaheim, CA 92803.
Circle 214 on Inquiry Card

QUARTER-INCH DATA CARTRIDGE

Cartridge contains Quadronix I virgin computer tape that is certified write-skip free, and assures uniform output on all four tracks by long-life edge guides. Precision rollers and improved roller and hub retaining system reduce skew and jitter. Drive elements are protected by high-impact plastic cover mated to precision-machined metal base-plate. Further protection is given by plastic door that automatically closes over tape head opening when cartridge is removed from transport. **Wabash Tape Corp,** 2700 Des Plaines Ave, Des Plaines, IL 60018.
Circle 215 on Inquiry Card

Ask CONTROL DATA for the new low cost, problem-free OEM companion to Cartridge Disk Drives.

The CDC® Model 9414 "Falcon" Fixed-Media Disk Drive offers 6000- hour MTBF. And you can pass the low-price-per-box advantage on to your customers! Available in 6 or 12 megabyte capacities.

We have it.

"Falcon" offers superior reliability (6000-hour MTBF) and maintainability. Here are just a few of the reasons why:

- No electrical adjustments anywhere in the unit! No operator intervention needed; the entire unit is software activated.
- Only four minor mechanical adjustments are possible—they may never be needed.
- No blower to make noise or use energy. Instead, the oversized air filter and dynamic air flow design provide a generous air supply—and greater reliability.
- Modular construction plus reliable "Winchester"-type spindle and carriage.

Use the "Falcon" Fixed Media Disk Drive in modules as your sole memory source with low-cost cassette or diskette input. Or, daisy chain it into your present system alongside more expensive removable-media drives.

But first, test evaluate it... compare it with competitive drives. Whether large OEM or small, you'll discover you can offer incredible reliability at lower cost—and that's a good offer any time!

Call (405) 946-5421 or return coupon to: Terry J. Hardie, Manager, Product Sales, Control Data Corporation, 4000 NW 39th Street, Oklahoma City, OK 73112.
Tell me more about your OEM Falcon Fixed-Media Double-Density Disk Drive.

Ask the CDC OEM people

NAME_____ TITLE_____

COMPANY_____ ADDRESS_____

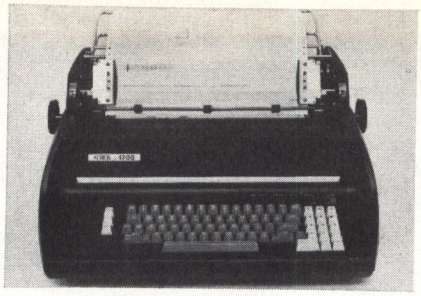
CITY_____ STATE_____ ZIP_____ AREA CODE_____ PHONE_____

CONTROL DATA CORPORATION

CIRCLE 67 ON INQUIRY CARD

PRODUCTS

COMMUNICATIONS TERMINAL

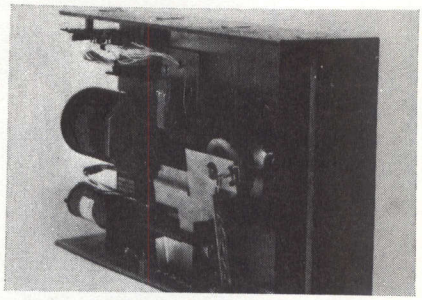


Printing at speeds to 45 char/s, the microprocessor-driven 1700 terminal uses Diablo HyType II printer mechanism. The typewriter-paired keyboard provides direct compatibility for APL applications, placing special characters in industry-standard locations for use with an APL printwheel. When used with a computer-aided text-processing system, the terminal automatically creates, edits, and prints documents according to instructions stored in the computer. **Xerox Corp,** 701 S Aviation Blvd, El Segundo, CA 90245.
Circle 216 on Inquiry Card

DISC SUBSYSTEMS

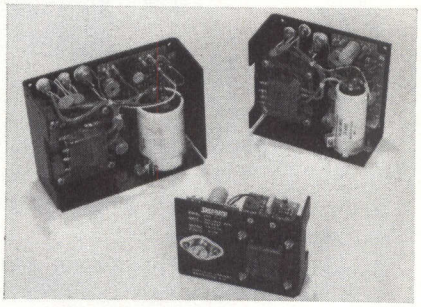
Featuring four drives per controller, 30-ms average access time, 603-MHz word transfer rate, and 8.33-ms average latency, 40M-, 80M-, and 300M-byte disc subsystems are plug-to-plug compatible with Data General Nova minicomputers. Systems include controller, drives, power supply, interface, and all necessary cables and mounting hardware. **Tri-Star Computer Systems, Inc,** 304 Harper Dr, Moorestown, NJ 08057.
Circle 217 on Inquiry Card

DISKETTE DRIVE



Model 70 features voice coil positioning, a large disc design characteristic which assures positioning accuracy and speeds access time. It will accomplish a full stroke 76-track seek in 100 ms; track-to-track access is 10 ms and avg seek is 33 ms. There is no head settling time. A direct-drive dc motor makes the unit burn-out proof and insures accurate diskette rotational speed. Total power consumption is 24 W with heat dissipation of 82 BTU/h. **PerSci Inc,** 4087 Glencoe Ave, Marina del Rey, CA 90291.
Circle 218 on Inquiry Card

OPEN CONSTRUCTION POWER SUPPLIES



SOC series covers voltages from 2 to 28 V. Design features include an exclusive current limit circuit which produces lower total dissipation and higher temp stability, remote sensing to automatically compensate for line drops, fusible resistor in dc load line, and optional overvoltage protection for models over 2 V. SOC transformers are tapped to permit operation from nom 115/208/230-Vac inputs. **Sorensen Co,** 676 Island Pond Rd, Manchester, NH 03103.
Circle 219 on Inquiry Card

Punch it out on Paper.

Get it back on Disk.

To Replace High Speed Paper Tape.

The FlexiFile 10 requires NO software modifications in your present system. Average transfer rates can exceed 1700 bytes per second across an entire disk. 98,113 bytes per side.

A single floppy disk translates to 816 feet of paper tape ... and front panel switching allows manual access to any track on the disk.

For Data Communications Interface.

The FlexiFile 10's RS 232 coupler offers selectable baud rates of up to 9600. Simple use of the correct cable allows this 18 lb. package to replace either a terminal or a data set. And the FlexiFile 10 can be connected between the terminal and modem to serve as a recording device for both units.

Total Systems Versatility.

Program loading and on-line storage for less than $1000 in quantity. Stand alone or rack-mount options.

Mail To: **Tri-Data**
800 Maude Avenue
Mountain View, CA 94043

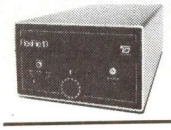
Name _____

Address _____

Company _____

City _____ State _____ Zip code _____

Application _____



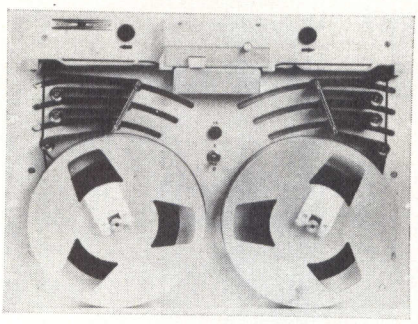
Tri-Data
800 Maude Avenue
Mountain View, California 94043
(415) 969-3700

Mountain View, CA **415-969-3700**
New York, NY **201-947-2092**
TWX: **910-379-6978**

CIRCLE 69 ON INQUIRY CARD

PRODUCTS

PAPER TAPE READERS



Combining speeds up to 600 char/s with gentle tape handling, Infranor readers use a brake/clutch capstan drive with no sprockets to provide gentle tape handling. This feature permits paper tape to have equivalent damage resistance and long life of more costly mylar/aluminum tapes. Series 2061 reads 130 char/s, rewinds at 9 ft/s avg, and has 325-ft tape capacity; 2063 reads 300 char/s, rewinds at 15 ft/s, and has 750-ft capacity; and 2066 reads 600 char/s (continuous), has 350-char/s step mode, rewinds at 25 ft/s, and handles 750 ft of tape. **Summit Engineering Corp,** 2311 S Seventh Ave, PO Box 938, Bozeman, MT 59715.
Circle 220 on Inquiry Card

SCHEDULE CONTROL SOFTWARE

Critical path management (CPM) reporting/charting system provides close control over job scheduling. Most of a typ mainframe CPM package is supported in 8K words and two floppies on a DEC Datasystem 310. The package accommodates 999 activities and calculates earliest start and end, latest start and end, and total and free floats. In addition to computing optimum job scheduling, it supports printing of scheduling charts, either complete or partial by type of activity or time period within total duration. **Compas, Inc,** 413 Kellogg Ave, PO Box 687, Ames, IA 50010.
Circle 221 on Inquiry Card

8-BIT A-D CONVERTER

The MM5357, combining classical circuit techniques with a high-yielding ion-implanted p-channel MOS process, contains a chain of 256 identical resistors connected in series, 255 analog switches, high impedance input comparator, output latches, and control logic on a single monolithic chip. Conversion is performed using the successive approximation technique. Linearity is $\pm\frac{1}{2}$ LSB, input impedance is >100 MΩ, and conversion rate is as low as 20 μs. The device operates from 5 and −12 V and dissipates approx 170 mW. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

500-LINE/MIN. PRINTER

Model LP6351 uses the exclusive helical platen concept: printing is accomplished with the only moving parts being the hammers and platen. There are 22 hammers plus spiralling platen, with all hammers set in a single accessible bank. Microprocessor logic provides char generation and print control. Operating at 500 full length (132 col) lines/min., 1100 char/s or 66,000 char/min. are produced. Reduced size print is also available. Std 64-char font is generated in 9 x 7 matrix pattern. **Potter Instrument Co, Inc,** 151 Sunnyside Blvd, Plainview, NY 11803.
Circle 222 on Inquiry Card

PERIPHERAL DRIVERS

The 55/75470 family of monolithic ICs features output current capability of 300 mA with no latch-up problems at 55 Vdc, and are pin-for-pin replacements of 55/75450 and 55/75460 series drivers. Fully compatible with TTL and DTL logic, with typical ac switching speeds of 45 ns, military and commercial grades are available. Military device is supplied either as ceramic DIP (55470DM) or flatpack (55470-FM); commercial unit is available in either ceramic (75470DC) or plastic DIP (75470-PC). **Fairchild Camera and Instrument Corp, Analog Div,** 464 Ellis St, Mountain View, CA 94042.
Circle 223 on Inquiry Card

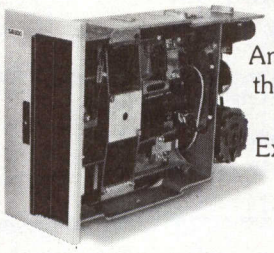
3 years, 12 patents, and 30,000 installations back every Shugart floppy disk.

No wonder two out of three OEM's specify Shugart floppy disks. They get more exclusive features, more product support, and more responsive delivery schedules. So can you.

A SA800/801 diskette storage drive gives your system more salable features: □ Single density, or double density for the same price. □ A patented diskette clamping/registration design that prevents diskette damage from misregistration over 30,000 interchanges. □ A proprietary ceramic read/write head that extends media life to over 3.5 million passes per track with a head life exceeding 15,000 hours. □ Extras like patented pop-out diskette retrieval, drive activity indicator light, and die cast cartridge guide and base plate.

If your system needs more data storage, you can easily convert from single to double density on the same drive. And you have a wide selection of product configurations—standard or compact "skinny" drive options, controller kits, and complete storage sub-systems.

Shugart gives you more daily support—systems design, technical service, documentation and applications help.



And Shugart is responsive. We will give you the delivery schedule you want, and we'll meet that schedule. Ask our customers.

Experience. Technology. Responsiveness. No wonder two out of three OEM's specify Shugart.

The leader in low-cost disk storage.

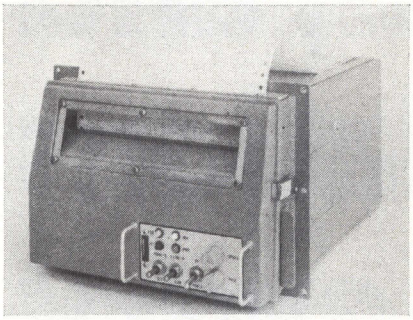
SHUGART ASSOCIATES

435 Indio Way Sunnyvale, CA 94086 Phone: (408) 733-0100

Europe Sales/Service: 3, Place Gustave Eiffel, Silic 311
94588 Rungis, France Telephone: (1) 686-00-85

PRODUCTS

400-LINE/MIN. MILITARIZED PRINTER



HSP-3609-212 provides 400 line/min. printout on single or multi-part sprocketed fanfold or friction feed paper. Unit meets MIL-E-16400 and NACSEM 5100 requirements. Fourteen voice coil transducers apply pressure against a rotating helical scanner to output 64 ASCII coded char, or an internally programmed graphic subset. The 9 x 7 dot matrix pattern provides high degree of char definition and resolution. Dual format capability also is possible. **Miltope Corp,** 532 Broad Hollow Rd, Melville, NY 11746.
Circle 224 on Inquiry Card

ANALOG-TO-DIGITAL CONVERTER

Model A-856, for use in applications involving a large number of submillivolt data points, yields resolution of 1 part in 65,536, stability of 2 ppm/°C, and 8-μs conversion time. Key to high speed is a 4-phase internal clock for optimizing settling times. The device can quantize 305 μV out of a full scale input voltage of $\pm$10 V into a 16-bit parallel output code of complementary offset binary. An optional onboard sample and hold allows users to resolve data from high frequency signals with min aperture error. **Intech/MFI,** 282 Brokaw Rd, Santa Clara, CA 95050.
Circle 225 on Inquiry Card

SHORT HAUL MODEM

Intended for asynchronous transmission with an interface according to EIA RS-232 and CCITT V24 specs, M-1 can be used as local communication link between computers, displays, or printers. Line driving is performed by 2-way balanced current loop. Transmission and receiving can occur simultaneously (full duplex). Specs include 0 to 9600 baud speeds; max distances are 2, 3, 5, 10, or 10 miles at speeds of 9600, 4800, 2400, 1200, or 600 baud, respectively. Power requirement is 115 Vac, 60 Hz. **bo-sherrel co,** 36443 Shelley Ct, Newark, CA 94560.
Circle 226 on Inquiry Card

RESISTOR NETWORKS

Offering 64 std resistance values, ranging from 33 Ω to 270 kΩ in 4-, 6-, 8-, 10-, and 12-pin SIPs and 14- and 16-pin DIPs, networks occupy only ¼ sq in. on a PC board. Resistor configuration is a "top hat" design—omega shaped resistor path is longer than conventional rectangular path, but necessary space on the alumina ceramic substrate is comparable. DIPs may be interchanged with IC packages for use in automatic insertion equipment. Typ weight is 1.3 g. Std resistance tolerances are $\pm$2, 5, and 10%. **Stackpole Components Co,** PO Box 14466, Raleigh, NC 27610.
Circle 227 on Inquiry Card

LIGHTED PUSHBUTTON SWITCHES

Industry std, flush-mounted switches and indicators in ½ and ¾" square, rectangular, and round lens/button configurations are available on existing snap-in or hard-mount spst to 6pdt switches. Mounted flush with the housing flange or panel surface, lens can be removed only from the rear of the panel. Flush button surface can not be accidentally actuated. Permanently colored or clear acrylic lenses may be specified in solid color, with legends or split screen function indicators. **Electro-Mech Components,** 1826 N Floradale Ave, South El Monte, CA 91733.
Circle 228 on Inquiry Card

We're hot for your BAUD!

And we've got the models to prove it — the Anadex, DP-750 Series of alpha- numeric printers working at Baud rates from 110 to 2400.

They're complete, self-contained drum printers that can print, in red or black, 42 alpha-numeric characters and symbols in 21 columns at 25 characters/second.

With four models, you have a choice of synchronous or asynchronous ASCII compatible inputs with appropriate internal storage and control signals. Input circuitry meets EIA Standard RS232-C for easy interfacing to your minicomputer or modem.

Reliability? Underneath that classy package there's a unit with a MTBF of over five million print cycles . . . the result of conservative design, fewer components to fail, and a few tricks like turning off the drum motor when not actually printing.

A complete package of options lets you tailor the 750 series to your system. For example, there's a form-feed option to automatically position pre-printed paper or gummed labels.

Prices start at $995 for one, with quantity discounts and special configurations to OEM's.

To find out how our hot little models perform, contact us at 7833 Haskell Avenue, Van Nuys, California 91406; telephone (213) 782-9527; TWX 910-495-1762; or call our local rep.

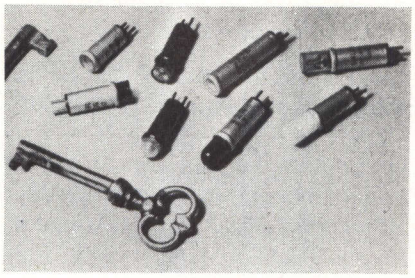
ANADEX INSTRUMENTS, INC. *the instrument people!*

Write for your Free, "hot for your BAUD" poster . . . add a little glamour to your office.

CIRCLE 71 ON INQUIRY CARD

PRODUCTS

ULTRAMINIATURE INDICATOR LAMP CARTRIDGES



Datalamp 507 series includes incandescent, neon, and Diode-Lite® LED cartridges offering a variety of lens colors and configurations. Connection is made by nickel silver pins in nylon-insulated header, offset to provide polarization. Cartridges plug into Datalamp holders or cartridge connectors, or are available in complete Datalite™ indicator light assemblies. LED lamps are interchangeable with incandescent cartridges, and are compatible with RTL, DTL, and TTL ICs. **Dialight, a North American Philips Co,** 203 Harrison Pl, Brooklyn, NY 11237.
Circle 229 on Inquiry Card

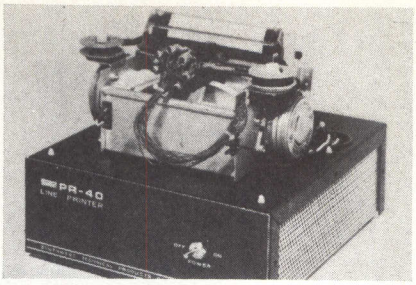
CLUSTER CONTROLLER

With dual-port computer interfacing, GDS 300 permits up to 16 terminals to be interfaced with one or two computers (even with different models). Controller can accommodate any combination of CRT displays and keyboard models, and can mix an outside source video signal with computer data to provide a combined display. Composite video output signal which drives the monitors is RS-170 compatible. Unit has parallel interface at 1.0M bytes/s, as well as serial communications up to 9600 bits/s. **Goodwood Data Systems,** PO Box 768, Ogdensburg, NY 13669.
Circle 230 on Inquiry Card

INCANDESCENT FLATPACK DIGITAL DISPLAYS

Two additions to the Aurora series of 7-segment digital displays operate at 5 Vdc, and are packaged in conventional 14- and 16-pin DIP flatpack configurations. 13K ft-L brightness for easy reading in high ambient lighting or sunlit environments is provided. Slightly inclined (5 deg) chars are 0.47″ high x 0.24″ wide (FFD-41) and 0.61″ x 0.28″ (FFD-51), with right hand decimal formats. Segments are mounted on a single plane in a black ceramic receptacle, sealed with a clear glass screen. **Industrial Electronic Engineers, Inc,** 7720-40 Lemona Ave, Van Nuys, CA 91405.
Circle 231 on Inquiry Card

ALPHANUMERIC PRINTER KIT

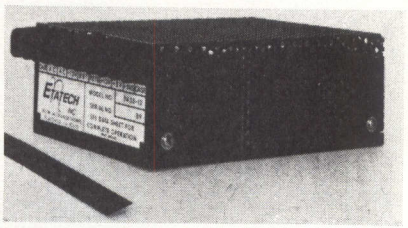


A 5 x 7 dot matrix impact printer, PR-40 prints 64-char upper case ASCII set with 40 char/line at a rate of 75 lines/min. on std 3⅞″-wide rolls of adding machine paper. One complete line is printed at a time from an internal 40-char line buffer memory. Available in kit form only, it includes assembled print mechanism; chassis; circuit boards; components; 120/240-Vac, 50/60-Hz power supply; assembly instructions; one ribbon; and one roll of paper. **Southwest Technical Products Corp,** 219 W Rhapsody, San Antonio, TX 78216.
Circle 232 on Inquiry Card

DATA SET

LDS 120 is suitable for all speeds of asynchronous data transmission up to 9600 bits/s on full-duplex 4-wire or half-duplex 2-wire circuits. Modulation scheme does not require dc continuity, and transmission signal levels are in accordance with Bell Publication 43401. At 9600 bits/s over 26-gauge wire, the unit will transmit at distances up to 5.5 miles. Other features include controlled carrier for multidrop operation with separate LEDs for power and receive carrier indications. **Gandalf Data Inc,** 190 Shepard Ave, Wheeling, IL 60090.
Circle 233 on Inquiry Card

TRIPLE OUTPUT SWITCHER



A 110-W supply in an A series package (6 x 4 x 2¼″), unit uses patented Univerter™ single-switch transistor PWM technique to provide 5 V at 10 A and either ±12 V at 2.5 A each (model 3A5-12) or ±15 V at 2 A each (3A5-15). All outputs are fully regulated for line and load. Ripple is <100 mV pk-pk from all sources for the primary 5-V output and <10 mV pk-pk for series-regulated auxiliary outputs. Min efficiencies are 71% for -2 and 73% for -15. **Etatech, Inc,** 187-M W Orangethorpe Ave, Placentia, CA 92670.
Circle 234 on Inquiry Card

IT'S SORT OF LIKE YOUR KID'S WAGON.

RUGGED. RELIABLE. FUNCTIONAL.

It gets the job done. Right.
The Zentec 9003 isn't just an intelligent terminal, it's a user programmable intelligent terminal. A management system that lets you put the power where you need it... when you need it... dependably, economically, reliably.

Complex problems. Straight answers.
We can supply microcomputer firmware and peripherals. But that won't solve all your problems. That's why we also make the 9003 user programmable. In other words, we play it your way.

Before you get it, we test it.
Maybe it doesn't make sense to tell you that you can't buy a brand new 9003. But you can't. Before we deliver your unit, we test it exhaustively. If the unit gets tired, we send you one that doesn't. That means you can plan on having your 9003 a long, long time. And as your needs expand, remember Zentec's modular peripherals.

We know your problem.
The answer to high line costs, Host CPU overhead or operator and management waiting time is Distributed Processing. And the answer to Distributed Processing is the Zentec 9003: A simple, rugged, dependable system. It's sort of like your kid's wagon. We think that's sort of a good idea.

Distributed Processing From

ZENTEC

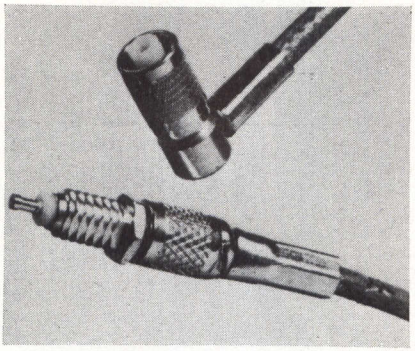
Call us for information:

- Santa Clara (408) 246-7662 • TWX 910-338-0572
- Southern Calif. (714) 998-9680 • TWX 910-593-1339
- Midwest (312) 297-8550
- Boston (617) 879-7530 • TWX 710-380-0105
- New York (914) 949-6476 • TWX 710-568-1335
- Philadelphia (215) 688-7325 • TWX 510-668-2995
- Washington (301) 656-3061 • TWX 710-824-0093
- United Kingdom (0442) 61266 • TLX 851-825629
- West Germany 0611-634037 • TLX 841-416608
- Austria 425451 or 421675 • TLX 847-74737
- Switzerland 041-831043 • TLX 845-72231
- Netherlands 01720-94044 • TLX 844-34111

CIRCLE 75 ON INQUIRY CARD

PRODUCTS

MICROMINIATURE COAX CONNECTOR



Lepra/Con connectors have a voltage standard wave ratio of 1.08 to 1 at a frequency of 1 GHz. Manufactured with Twist/Con contacts and available in 180 styles, the devices are designed for RG178 and RG196. They also come with an optional locking interface which permits the user to lock the coaxial plug, when mated to its receptacle, preventing any axial rotation. Screw-on and slide-on types are adaptable to most common connector series such as BNC-TNC-SMA. **Malco, a Microdot co,** 220 Pasadena Ave, South Pasadena, CA 91030.
Circle 235 on Inquiry Card

INTELLIGENT CONTROLLER

System permits users to enter, edit, format, and transmit transaction-oriented data to a host computer using MDR series optical mark readers as interactive terminals similar to the IBM 3275. Controller system accepts input in the form of punches, pencil marks, preprinted, or computer-generated data, and reads, edits, and preprocesses information prior to transmission to a host computer. Synchronous or asynchronous communications and transfer rates from 110 to 2400 baud are switch-selectable. **Bell & Howell, Business Data Products Div,** 360 Sierra Madre Villa, Pasadena, CA 91109.
Circle 236 on Inquiry Card

VITREOUS ENAMEL RESISTORS

Expanded series of conformal vitreous enamel axial lead wirewound resistors are of rugged construction with a special coating to guard against extreme humidity and temperature cycling with no out-gassing. The all-welded devices are available in 1, 2, 2½, 3, 5, 6, 7, 9, 11, and 12 W, with a ±5% std tolerance (±1% to ±10% are available). Coating is a consistent uniform high performance vitreous enamel, encasing high grade resistance alloy wire, in a single layer winding. Tempco is 0 ±30 ppm/°C typ for ≥10 Ω. **AMF Inc, RCL Electronics Div,** 700 S 21st St, Irvington, NJ 07111.
Circle 237 on Inquiry Card

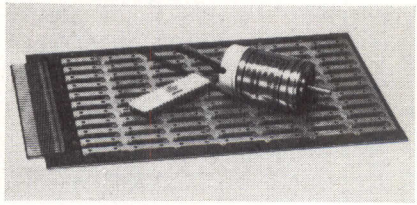
RECEIVE-ONLY DATA TERMINAL

Containing interchangeable, dual-font char sets (upper and lower case), model 1201 features extremely quiet operation, and is hard-wire compatible with CRTs, minicomputers, and CPUs through EIA RS-232 interface. Unit measures 14 x 12.5 x 4.5" and weighs 13 lb. Std features include printing speeds up to 30 char/s; parallel interface; 96 char; offline line feed and carriage return; high speed paper advance; and power-on, online operation, error, and audible bell indicators. **Computer Devices Inc,** 9 Ray Ave, PO Box 421, Burlington, MA 01803.
Circle 238 on Inquiry Card

HIGH RELIABILITY POWER RELAYS

Compact HL-series units are designed to provide high switching capacity. For the spdt version, current rating is 15 A at 125 Vac; for dpdt, 10 A at 250 Vac. Reliability is assured by spot welding all connections, resulting in more uniform connections, and elimination of possible gas contamination and human error. Design features include arc barriers between contacts, debris wells, simultaneous molding, and heat riveting. Typ mechanical life expectancy is $>10^8$ operations. **Arrow-M Corp,** 250 Sheffield St, Mountainside, NJ 07092.
Circle 239 on Inquiry Card

TRANSDUCER



Available in ruggedized or miniature cases as small as 1.1" in diameter, PI/MP transducers provide a complete range of digital formats for direct microprocessor interfacing. Unit is designed to supply position data in real time to microprocessors. Single turn resolutions are available to 12 bits and three decades BCD; multiturn units provide resolutions to 17 bits and five decades BCD. Zero set and preset capability is available. **Astrosystems, Inc,** 6 Nevada Dr, Lake Success, NY 11040.
Circle 240 on Inquiry Card

TERADYNE'S J401: THE FULL CAPABILITY IC TEST SYSTEM EVERY ENGINEER CAN USE.

Until now, the complexities of test programming have kept all but a few specialists from using IC test systems. Everyone else had to queue up at the programmer's desk or do without the kind of information that was really needed.

Now there's a J401. A fully programmable test system for T^2L ICs with up to 24 pins, complete with built-in CRT, printer, and mag tape unit, that any engineer can learn to use in minutes.

For IC producers this means immediate access to vital process control information. For IC users it means the data necessary to choose components and vendors intelligently. And the ability to extract from field returns the information needed to improve product quality and yield.

The performance and flexibility of a large, computer-operated test system.

The J401 delivers the flexibility ordinarily associated only with larger, more expensive systems. It can datalog any forced or measured function and it can generate an x-y plot of any two parameters. The system also operates as a high throughput go/no-go tester for the production line or incoming inspection.

Product data fast. Higher product yield.

For the semiconductor manufacturer, the easy-to-use J401 allows errors to be spotted before they can begin to multiply. QC engineers can use it to evaluate devices, determine test margins, and check device lots.

The electronic equipment manufacturer will find the J401 useful in monitoring vendor-to-vendor and lot-to-lot variations. It enables him to spot device characteristics that could be contributing to problems. And QC personnel can use the system to analyze failures and reduce service costs.

A system for meeting the real objectives of incoming inspection.

The J401 gives you fast go/no-go testing with an important difference. It gives control over the *way* devices are tested. By pushing a few keys you can change test conditions, bin out top-quality ICs, or have datalogging to support returns. All in seconds. This is incoming inspection as it should be.

It's a Teradyne.

Each J401 is built for hard use on the factory floor. Each is supported by Teradyne's ten-year circuit module warranty, a 24-hour telephone trouble-shooting service, and a world-wide field service backed up by local parts stocking centers.

For complete information on the J401, write:
Teradyne, 183 Essex Street, Boston, Massachusetts. In Europe: Teradyne, Ltd., Clive House, Weybridge, Surrey, England.

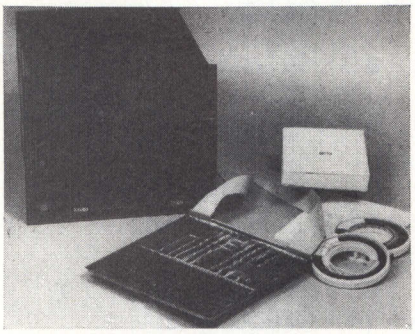
WE SELL PRODUCTIVITY.

TERADYNE

CHICAGO (312) 298-8610/DALLAS (214) 231-5384/NEW ENGLAND (617) 458-1256/NEW YORK (201) 334-9770
SUNNYVALE (408) 732-8770/LONDON (0932) 51431/PARIS 073 16 98/ROME 59 47 62/MUNICH (089) 33 50 61/TOKYO (03) 406-4021

PRODUCTS

PROGRAMMABLE ARRAY PROCESSOR



Ultra-fast, 32-bit floating point MAP processors are offered with complete hardware and software interfacing for Data General's minicomputers. MAP operates as a modular stored program peripheral. FFT, correlation, convolution, filtering, matrix, vector, and other algorithms can be handled efficiently. Processor is assembly language and FORTRAN programmable, enabling processing parameters and algorithms to be readily added or altered. Several models are available. **CSP Inc,** 209 Middlesex Tpk, Burlington, MA 01803.
Circle 241 on Inquiry Card

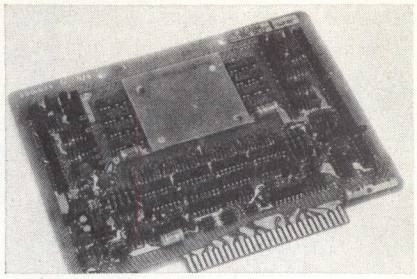
COMPUTER TAPE

"Polisurf" is manufactured by a proprietary process to provide smoother tape surface which improves head-to-tape contact on tape transports, giving improved product reliability and better tape-to-transport interchangeability, as well as lower head wear. A clean tape surface, where embedded surface debris is effectively removed, means a cleaner running tape on the transports. The tape is guaranteed to perform at densities of 800, 1600, and 6250 bits/in. at all speeds. **TRI,** PO Box 318, Dundee, IL 60118.
Circle 242 on Inquiry Card

DMA COMMUNICATIONS MULTIPLEXER

A multiport, dedicated communications I/O channel that accepts up to eight asynchronous lines from terminals or modems, the series 8400 operates under control of an 8-bit microprocessor with its own private memory. Proprietary firmware and reentrant handlers are located in an 8K x 9-bit RAM. The processor concurrently controls char-level protocol, error checking, and buffer maintenance of each port at aggregate data rates up to 76,800 baud. Installed in an I/O channel slot, the device interfaces directly to memory buses. **Harris Corp, Computer Systems Div,** 1200 Gateway Dr, Fort Lauderdale, FL 33309.
Circle 243 on Inquiry Card

MICROCOMPUTER CORE MEMORY

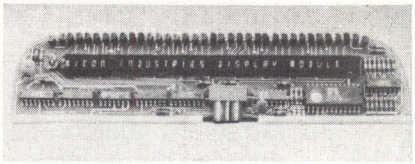


A single card module storing 1024 8-bit words with access within 450 ns, the MCM-8300 is designed to operate in read-modify-write applications and is completely self-contained. 512- and 256-word versions are also available. Temp independent Unibit[R] cores are used for performance over wide temp ranges. A single 5-V power source is required. Each module includes timing and control, data and address registers, decoding and drive circuits, and TTL-compatible interface. **Ampex Corp,** PO Box 33, Marina del Rey, CA 90291.
Circle 244 on Inquiry Card

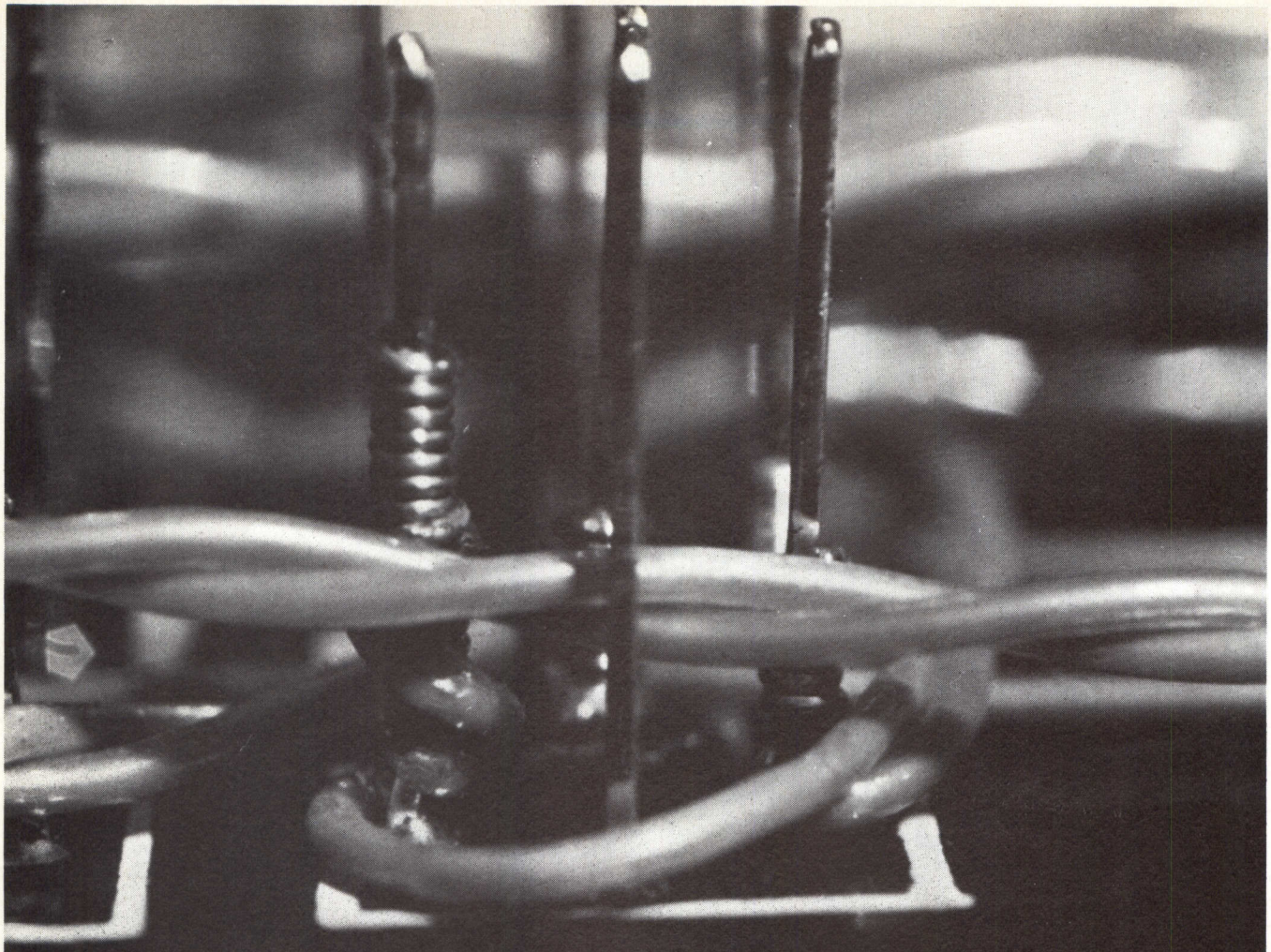
PRIVATE LINE 4800-BIT/s MODEM

Bell 208A-compatible modem features an all-digital adaptive equalizer which affords max convergence and prevents drifts and other analog errors. Model 7208A provides full- or half-duplex, or simplex transmission for point-to-point or multipoint polling applications, and has built-in on/offline test capabilities with front panel controls and diagnostic lights. The equalizer employs mean-square algorithm which allows the local modem to continually reoptimize the equalizer without restarting the remote transmitter. **Tele-Dynamics Div of Ambac Industries, Inc,** 525 Virginia Dr, Fort Washington, PA 19034.
Circle 245 on Inquiry Card

ALPHANUMERIC DISPLAY MODULE



Model 932 features proprietary 9-segment design; complete display contains 32 extra-bright char positions, driving circuitry, and storage register on an 8.2 x 2.0 x 0.5" PC board. Read-out area is 6.4" long, placed slightly above and to the right of center of the board. Display board offers wide viewing angle (90 deg vertical and horizontal) and may be faced with a red glare-proof window. Alphanumeric font displays all ASCII uppercase char and symbols. **Micon Industries,** 252 Oak St, Oakland, CA 94607.
Circle 246 on Inquiry Card



KYNAR* resin... the tough, reliable and economical insulation for computer wires.

Kynar insulated wire has been performing successfully in hundreds of computer installations for over 12 years because Kynar PVF-2 coated wire is resistant to shorts that result from cut-through abrasion.

Yes, Kynar is tough. It resists the abrasion and cut-through that can occur during wire-wrap machine application. Its excellent resistance to cold-flow protects against electrical failures when wires are bent tightly around sharp-cornered posts. Kynar cuts and strips smoothly in automatic wiring machines. It is heat-resistant, lightweight, and has exceptionally high tensile and impact strength.

Kynar is readily available, and at a truly economical price. For a sample, complete specs and a list of wire fabricators, contact the Plastics Department, Pennwalt Corporation, Three Parkway, Philadelphia, PA 19102. (215) 587-7519.

*Kynar is Pennwalt's registered trademark for its polyvinylidene resin.

PENNWALT
ENGINEERING PLASTICS

CIRCLE 79 ON INQUIRY CARD

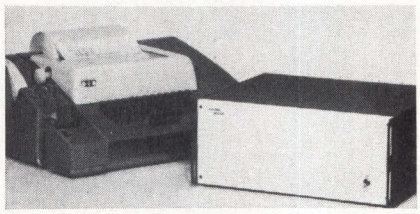
PRODUCTS

LIQUID CRYSTAL DISPLAYS

Liquid crystal displays, referred to as dynamic scattering displays, use less power, and can control reflectivity or transmission of light. Normally viewed as white numerals, filters are available to give a wide range of background color variations. Test units have achieved >40 kh of life. Measured current drain is <300 nA/cm² at 10 V. Switching time has been decreased to <80 ms. **UCE Inc,** 20 North Main, Norwalk, CT 06854.

Circle 247 on Inquiry Card

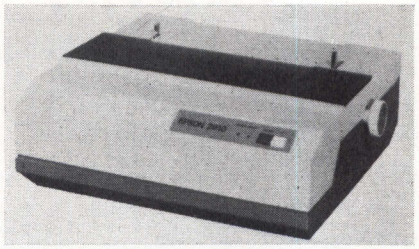
HIGH SPEED DATA ACQUISITION SYSTEM



Model 2000 accommodates from 8 to 160 analog input channels in a single chassis; with expansion chassis, it can process up to 1280 input channels. Internal microprocessor control and teleprinter I/O permit easy reconfiguration to solve specific problems, and allow a wide variety of I/O formats. Data averaging, alarms, linearization, data storage, and calculations are some custom functions that may be implemented. **Electronic Solutions Inc,** 8070 Engineer Rd, San Diego, CA 92111.

Circle 248 on Inquiry Card

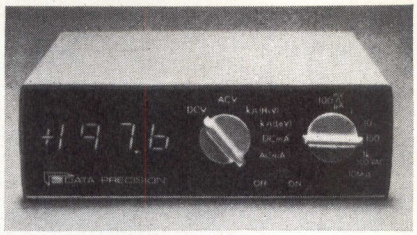
150-LINE/MIN. PRINTER



Using a simple dependable belt-impact printing method, the 2610's printer mechanism further emphasizes reduced size and complexity. Subportions, including print mechanism, power supply, and control electronics, are made for easy incorporation by OEM into a final system. The printer includes ASCII control logic and column buffering in addition to the complete electronic and mechanical chassis. The unit prints at 150 lines/min. with full 64-char set in an 80-col format. **Epson America, Inc,** 2990 W Lomita Blvd, Torrance, CA 90505.

Circle 249 on Inquiry Card

LAB PRECISION HAND-HELD MULTIMETER



Housed in a 1¾ x 5½ x 3½" case, model 175 is a full function, 32-range battery and line operated instrument, with basic sensitivity of 100 μV, both in dc and wide frequency band ac measuring functions. Five ranges of dc voltage measurement and 100% overrange capability per range permit measurements from 100 μV to 1 kV in either polarity, displaying both the plus and minus sign. Dc function is protected to ±1 kV on any range (including 100 mV); basic accuracy is 0.1%. **Data Precision Corp,** Audubon Rd, Wakefield, MA 01880.

Circle 250 on Inquiry Card

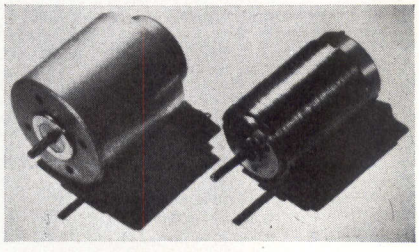
RS-232 SERIAL PRINTER INTERFACE

Interface for the 8200 series line printers makes it possible for the 2400 (8210) and 1400 (8230) line/min. printers to receive asynchronous serial data at rates up to 9600 baud. Internal switches allow baud rate selection, and current loop or RS-232 level inputs. In addition to std buffer memory of full print line, a 192-char FIFO buffer memory is built in to simplify serial transmission control from the data source. Interface mounts inside the printer. **Houston Instrument, Div of Bausch and Lomb,** 8500 Cameron Rd, Austin, TX 78753.

Circle 251 on Inquiry Card

TACH MOTORS

Ironless rotor motors are provided with 72-tooth tachogenerators in 24 and 12 Vdc models, with power inputs of 4.35 and 3.6 W, respectively. Need for preestablished poles is eliminated, resulting in minimal cogging, smooth operation, and low noise levels. Modified double-shaft version with 26-mm rear shaft extension is also available for use on encoders or in similar dual-drive applications. **North American Philips Controls Corp,** Cheshire Industrial Park, Cheshire, CT 06410.



Circle 252 on Inquiry Card

They're here. The industry's most advanced 100/200 megabyte OEM disk drives.

The new ISS 733-10/11 disk drives are the most advanced random access storage devices ever designed for the OEM market. With features that benefit you *and* your customers.

For example, exceptional speed in head positioning and start/stop times. Compactness. Quietness. Easy waist-high pack loading.

The big news, however, is their field-upgrade capabilities. The 100-megabyte 733-10 can be easily field-upgraded to 200 megabytes. Or you can have 200 megabytes immediately with ISS 733-11. And both can be ordered with, or field-upgraded to, dual port.

Advanced interface design
Our interface permits functional compatibility between ISS 733-10/11 and most current 40, 80, 100, 150, 200, and 300-megabyte drives. This means minimal controller modifications, if any.

Performance features
Integral power supply. Tolerates wide power variations, reduces susceptibility to cycle sags and brown-outs.

Module select plug. Permits flexibility in disk address assignments in multi-drive systems.

Data separation and write data precompensation. All data encoding/decoding is performed in the drive.

Absolute cylinder addressing. Disk addressing done in the drive, not the controller. Simplifies programming.

Industry standard media. 3336 and 3336-11 or equivalent disk packs.

Programmable sector mark. Allows user to select sector size to fit his application.

Important options
Dual port. ISS 733-10/11 can be upgraded from single to dual port in the field. Or dual port can be installed prior to delivery.

Sector counter. Signals the system which data sector is approaching the read/write heads.

Rotational position sensing. Signals the system when the desired sector is approaching the read/write heads. Increases system throughput.

Address mark format. Permits variable record lengths.

Daisy chaining. Greatly reduces cabling.

Round-the-clock ISS support
ISS maintains a complete support facility. Not just spares, but also technical assistance is available round-the-clock. Just call.

We'll be glad to send more information about the ISS 733-10/11. Write or call ISS Marketing, 10435 N. Tantau Ave., Cupertino, CA 95014, (408) 257-6220. ISS is an operating unit of Sperry Univac.

ISS

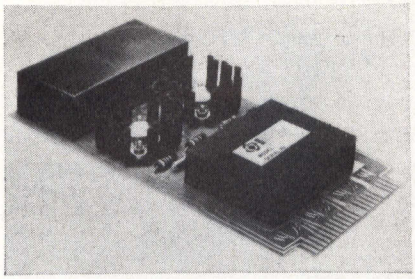
Technological leadership for the generations ahead.

Sperry Univac is a division of Sperry Rand Corporation

CIRCLE 81 ON INQUIRY CARD

PRODUCTS

DIGITAL-TO-SYNCHRO CONVERTER



Series of 14-bit converters can drive up to three size 11 torque receiver synchros with ±6-min. accuracy. Units measuring 4.5 x 9.25 x 1" accept a 14-bit natural binary angle and convert it into 3-wire synchro or 4-wire resolver signals. Output is short circuit protected, and current limited, with std loading of 5 VA. Available output voltages are 90 or 11.8 V rms L-L, 60 or 400 Hz. Digital inputs are TTL/DTL compatible; synchro output and reference is fully transformer isolated. **Computer Conversions Corp,** 6 Dunton Ct, East Northport, NY 11731.
Circle 253 on Inquiry Card

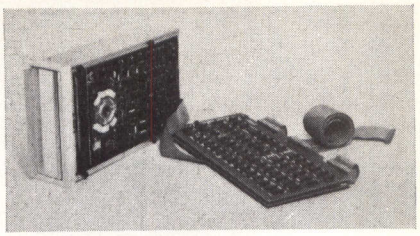
DIGITAL IC TESTER

J133D analogical circuit test instrument is a go/no-go tester optimized for functional and dc parametric inspection of digital devices. Unit tests SSI, MSI, and LSI devices in such technologies as TTL, CMOS, and HTL. Three-state and open-collector devices, timers, monostable multivibrators, ROMs, and RAMs are accommodated in packages with up to 24 pins. Front panel contains four lamps: input, output, supply, and reject. Operator inserts device, watching the pass/fail indicator; other three lamps indicate primary cause for rejection. **Teradyne, Inc,** 183 Essex St, Boston, MA 02111.
Circle 254 on Inquiry Card

CIRCUIT BREAKERS

Mini-Mag series W67 single-, W68 double-, and W69 triple-pole breakers feature circuit clearing time of 9 ms on moderate to heavy overloads. Slight inductance of coil helps limit I^2T on steeply rising fault currents. With trip-current ratings from a fraction to 30 A, breakers interrupt fault currents to 2 kA. Features include wipe-on-make contacts, and trip-free mechanism. Max operating voltages are 250 Vac, 60 or 400 Hz, and 50 Vdc. Models are temp stable between −40 and 85°C. **AMF Inc, Potter and Brumfield Div,** 200 Richland Creek Dr, Princeton, IN 47671.
Circle 255 on Inquiry Card

MICROPROCESSOR FLOPPY DISC SUBSYSTEM

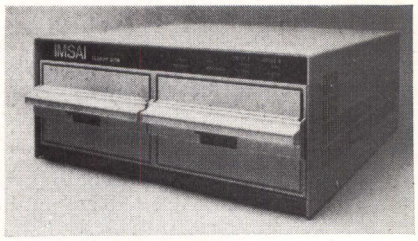


Called Frugal Floppy™, model FF-36 employs the same elements as the company's FD360 system. However, expensive cabinetry, power supply, and system assembly labor have been eliminated. Unit contains a CF360 controller/formatter, floppy disc drive with daisy chain capability, and all required connectors and cables. It can be supplied as a single or dual drive system. The controller/formatter provides auto track and sector seek/verify, full sector I/O buffers, and auto CRC generation and checking. **iCom Inc,** 6741 Variel Ave, Canoga Park, CA 91303.
Circle 256 on Inquiry Card

DATA COMMUNICATION TERMINAL

Featuring a modified General Electric TermiNet™ 30 teleprinter, Quad/Mode offers four choices of transmission. It has dial-up capability for timesharing terminals through DDD at 10-, 20-, or 30-char/s transmission speeds; access to the TWX network; direct hook-up for local computer communications front end; and access to TWX/DDD networks. Switch-selectable printing speeds, 80 or 132 print positions, single or dual mag tape cassettes, and 1200-baud tape transmission are available features. **Info/Products/International,** 1241 I East Chestnut, Santa Ana, CA 92701.
Circle 257 on Inquiry Card

INTELLIGENT FLOPPY DISC



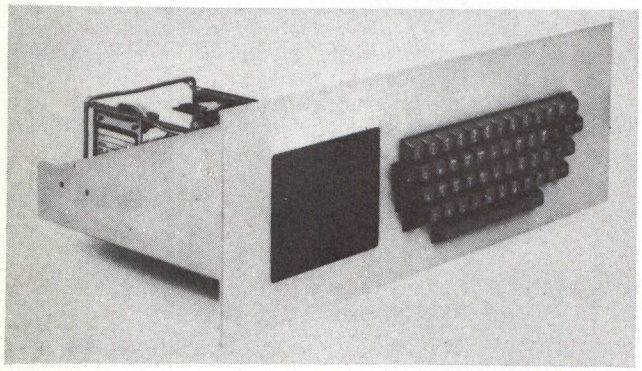
Floppy disc drive with intelligent interface/controller, specifically designed for use with the company's 8080 computer, has a capacity of 243K bytes using the IBM 3740 format. Interface/controller contains its own processor and direct access memory which operate independently but under command of the main processor of the 8080. Program format of the disc can be changed by reprogramming the interface EPROM chips. Up to four floppy disc drives can be controlled by one interface/controller. **IMS Associates, Inc,** 14860 Wicks Blvd, San Leandro, CA 94577.
Circle 258 on Inquiry Card

CACHE MEMORY

Model 45—made up of three PC board modules (cache matrix controller, cache memory matrix, and auxiliary cache matrix controller) and an optional auxiliary 5-Vdc power supply—is specifically designed to increase the speed of DEC PDP-11/45 and /50 computers. The memory is installed by plugging into available Fastbus™ and Unibus™ slots, with no hardware or software changes of any kind. The power supply fits into the lower power supply chassis. Typ overall system speed enhancement is claimed to be about 50%, nearly 100% in number crunching applications. Storage medium is Schottky bipolar RAM, data storage capacity is 1K bytes, word length is 16 bits, and cycle time is 300 ns. Installation physically restricts MOS or bipolar memory to a max of 16K. **Minntronics Co, Inc,** 2975 Furness St, St. Paul, MN 55109.

Circle 259 on Inquiry Card

GENERAL-PURPOSE CRT TERMINALS

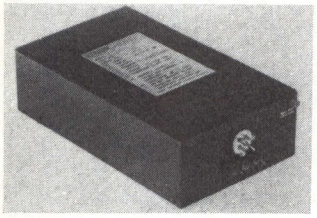


Rack-mounting series 3381 includes three 5" CRT terminals with 512-char, 16-line x 32-char/line formats. -1001 includes std full- or half-duplex RS-232-C interface for 110-, 600-, 2400-, and 9600-baud communications; -1002 provides 60-Vdc, 20-mA current loop interface; and -1012, with current loop interface, is for flush mounting on doors of std NEMA enclosures. Other rack-mounting versions have separate keyboards and 12" monitors. Series 3380 are table-top terminals displaying up to 1920 char in 24-line x 80-char format on 12-in. CRT. -1102 offers std TTY keyboard with numeric key pad, std RS-232-C or current loop communications interfaces for half- or full-duplex operation; -1202 includes u/lc char, editing, block transmission, protected formatting, and graphics. **General Automation, Inc,** 1055 S East St, Anaheim, CA 92805.

Circle 260 on Inquiry Card

DUAL OUTPUT POWER MODULES

One of the few switching regulated power supplies capable of operating over the full military range of −55 to 100°C, the UUN-12A series converts 115-Vac, 400-Hz input to 25, 50, or 100 W of regulated ±12-Vdc output. Load regulation is 0.5% for no load to full load at constant input voltage. Ripple and noise are 25 mV rms, 100 mV pk-pk over the full temperature range. Other features include full rated output current over the −55 to 85°C range, derated to 80% of full load rating at 100°C (baseplate temperature), and temperature effect of 0.03%/°C max. Modules meet environmental requirements of MIL-E-5272 and MIL-E-5400 for Class 2 equipment, are completely protected against short circuits of any duration, and will withstand an input voltage transient of 180 Vac for 0.1 s. **Abbott Transistor Laboratories, Inc,** 5200 W Jefferson Blvd, Los Angeles, CA 90016.

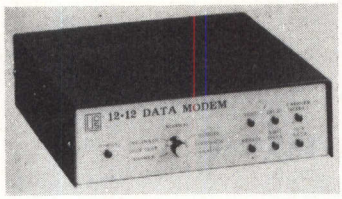


Circle 261 on Inquiry Card

PRODUCTS

2-WIRE, FULL-DUPLEX 1200-BIT/s MODEM

Capability for full-duplex operation using only two wires is a key feature of the model 12•12. This is accomplished by coherent phase shift keyed modulation techniques used in 2400-bit/s modems but at half the bit rate and half the required bandwidth. The 1200-bit/s modem, available in either free-standing or OEM card configurations, can be operated synchronously or asynchronously over either dial-up or leased lines. Variable data rate permits users to select the std rate or transfer data at 600, 300, 150, or 0 to 300 bits/s. No restrapping or adjustments are required to achieve the variations in data rate. Std CMOS circuitry is used; no custom LSI circuits are involved. The modem has an integral provision for automatic remote and local loopback testing. **Universal Data Systems, Inc,** 4900 Bradford Dr, Huntsville, AL 35805.



Circle 262 on Inquiry Card

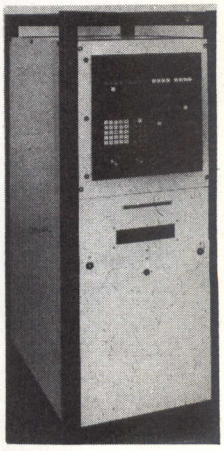
SINGLE-STATION DATA ENTRY/PROCESSING SYSTEM

Model 410—a single 576-char screen display station with typewriter-like keyboard, control unit with 2.5M-char of disc storage, 40K bytes of memory, ECMA cassette interchange for program maintenance, bidirectional 60-char/s printer, and binary synchronous communications at up to 4800 bits/s—is compatible with the company's model 340 and 350 intelligent terminals and its 440 clustered terminal processing system. Options include three other speeds of printers (120/180 char/s and 300 lines/min.), up to 64K bytes of memory, up to 10M char of fixed disc storage, flexible disc interchange, and keypunch-style keyboard. Operation in concurrent mode allows data entry and inquiry/response applications to be performed in the foreground while processing is being performed in the background. **Sycor Inc,** 100 Phoenix Dr, Ann Arbor, MI 48104.

Circle 263 on Inquiry Card

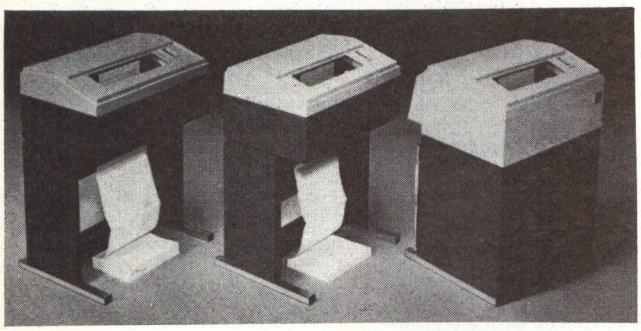
COMPUTER NUMERICAL CONTROL FOR TWO TO SIX AXES

Flexibility and performance of the W2560 CNC line are keyed to a basic 19" cube building block. Of 33 slots available, two are for a W2500 CPU, one for a memory protect card, six for 65K of memory, and one for memory control; the remaining 23 are open for customer I/O requirements. Specialized operator controls can be modified for special customer requirements and a CRT can be included as an option. A remote diagnostic program is offered to help customers with maintenance problems. Extensive standard software programs and engineering are available for a small one-time charge. Units have self-contained heat exchanger for cooling and are totally enclosed for use in environmentally harsh areas. **Westinghouse Electric Corp, Computer and Instrumentation Div,** 1200 W Colonial Dr, Orlando, FL 32804.



Circle 264 on Inquiry Card

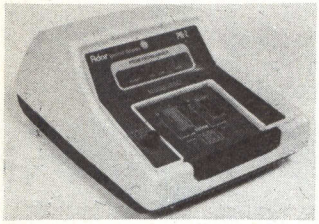
LOW TO HIGH SPEED LINE PRINTERS



Members of the 2200 family include the 300-line/min. model 2230, 600-line/min. 2260, and 900-line/min. 2290. All feature friction-free Mark IV hammer-actuator which has only one adjustment, as well as servo-controlled ribbon and paper systems which achieve single-line advance and slew rates of >30 in./s. Format of the 2290 is 136 char/line, 10 char/in. horizontal, and 6/8 lines/in. vertical. It uses a 64-char ASCII set and std code. Communication rate is 9600 baud. Electronics include full line buffering, TTL I/O, power supplies, control and logic circuits, and optional self-test code generator. An optional 12-channel direct access VFU allows software-controlled forms handling without operator intervention. **Dataproducts Corp,** 6219 DeSoto Ave, Woodland Hills, CA 91364.
Circle 265 on Inquiry Card

p/ROM DUPLICATOR/TESTER/PROGRAMMER

PR-2, claimed to be the first commercially available programmer incorporating basic parametric tests as part of the program/verification cycle, tests output leakage and verifies programmed parts with worst case fanout loads, V_{cc}, V_{ol}/V_{oh} levels, and simulated temperature testing. Each of several versions can program all parts in a particular generic p/ROM family and meets the manufacturer's recommended specifications for programming and testing. As a duplicator, it has high throughput and is capable of being interfaced with automatic handlers; as a programmer it is available with a hexadecimal or octal keyboard, to be used in preparation of prototype devices, pattern alteration, and field service applications. **Spectrum Dynamics,** 11B North Ave, Burlington, MA 01803.



Circle 266 on Inquiry Card

DMA INPUT/OUTPUT DISTRIBUTOR

High speed interfacing of up to four peripherals to the company's LSI family of minicomputers can be accomplished with the DMA I/O Distributor. Throughput of 250K bytes/s can be maintained without CPU intervention. The device is fully compatible with all other distributors in the company's I/O product family. Its main advantage is in applications where the combined throughputs involving a number of slow and medium speed devices exceed a computer's programmed I/O or interrupt bandwidth. If higher performance is required, mag tape units or other high speed devices or computer-to-computer communication can be supported. The distributor also supports programmed and interrupt I/O. It is packaged on a 7½ x 15" PC card. **Computer Automation, Inc,** 18651 Von Karman, Irvine, CA 92713.
Circle 267 on Inquiry Card

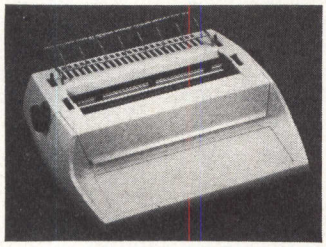
PRODUCTS

FLOPPY DISC CONTROLLER

IBM-compatible data formatting and control for one to six individual drives is provided by the MLP-8065 which interfaces directly to the company's MLP-8080 system bus. The controller responds to all standard disc commands including read, write, and seek. A data address register allows data transfers to and from any portion of system memory. After the specified command is executed, the controller generates a processor interrupt and returns a completion status word. During read or write, data transfer occurs automatically through a DMA process. Systems are available standalone or as a component in the HIT-5000 intelligent terminal system. Software support is available for command execution and error recovery. **Heurikon Corp,** 700 W Badger Rd, Madison, WI 53713.
Circle 268 on Inquiry Card

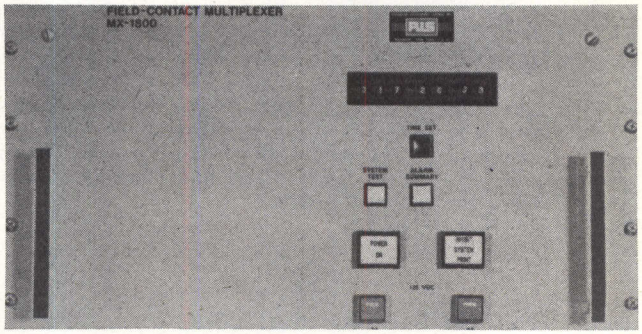
200-CHAR/s MATRIX PRINTER

One of the key features of the microprocessor-controlled model 2300 is its ability to stop within one print position even when operating at its full 200-char/s print speed. Because it uses a 9 x 7 dot matrix it can also print both u and lc char. Other features include high speed vertical and horizontal tabbing, bidirectional printing, incremental printing, internal power supply, self test, full LSI, and full line of paper handling accessories. Cartridge-type ribbons permit rapid change. Ballistic head design allows wire strikers to be in free flight, eliminating critical field head adjustments. The unit is compatible with the company's HyType serial printer. **Diablo Systems Inc,** 24500 Industrial Blvd, Hayward, CA 94545.



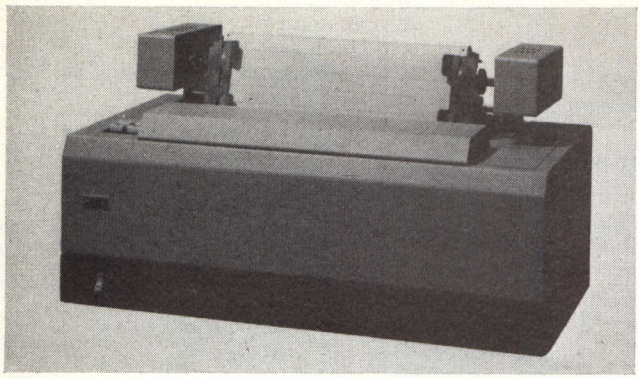
Circle 269 on Inquiry Card

FIELD-CONTACT MULTIPLEXER



A data-output-based field contact multiplexer for computer interfacing, supervisory control and data acquisition systems, or output to a common printer, the MX-1800 can present data to virtually any make computer or printer in serial ASCII through either 20-mA current loop or RS-232-C interface. Up to 1000 N.O. or N.C. type inputs are continuously scanned, state change and sequence of inputs are stored, and data are forwarded in computer acceptable format. Std 64-level buffer is expandable to a total of 320 levels. Modular design permits system expansion after installation. Multiple units may be arranged for data transmission to a central computer or for sharing a single optional remote printer. **Rochester Instrument Systems, Inc,** 275 N Union St, Rochester, NY 14605.
Circle 270 on Inquiry Card

MODULAR REMOTE MATRIX LINE PRINTER

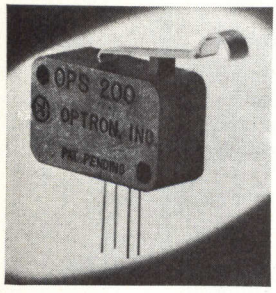


A variety of interface kits and options allows the model 6440 to operate in a number of communications systems. The std 132-col tabletop unit can print an original plus up to four copies on continuous forms, using a 7 x 7 dot matrix technique for generating a 64-char set (9 x 7 matrix and 128-char set optional). One-line-at-a-time printing is at a nom speed of 173 char/s at 60 Hz (180 char/s at 50 Hz); line rate is 55/min. at 132 char/line, 70/min. at 80, and 150/min. at 20. Slew speed is 7.5 in. (190 mm)/s. Available communication/terminal interfaces are serial and parallel for the company's 796 CRT terminals, and standalone for remote or in-house use with selectable or non-selectable communications protocol. **NCR Corp,** Dayton, OH 45479.
Circle 271 on Inquiry Card

COMPUTER-CONTROLLED MEMORY TEST SYSTEM

Primary elements of the Xincom III RAM/ROM test system consist of Nova 3 host computer with 32K words of MOS memory (expandable to 128K words), up to eight dual test-head model 5551 mainframes which communicate with the host computer in foreground/background mode, and one local microprocessor controller for each mainframe to provide program debug and software controlled communication. Software package provides access to Xintol high level programming language. All utility software routines are written in FORTRAN IV. Complete system diagnostics plus all std Data General software modules, including ALGOL and BASIC, are included. 10M-byte disc storage, HP 2644A command terminal, high speed printer, and 9-track mag tape drive are also provided. **Fairchild Camera and Instrument Corp, Instrumentation Systems Group,** 1725 Technology Dr, San Jose, CA 95110.
Circle 272 on Inquiry Card

OPTICALLY COUPLED LIMIT SWITCHES



Shutter control of OPS 200 and 200A solid-state switches is maintained by a snap-action mechanism to interrupt the light path between a GaAs IR LED and a Si photosensor. Condition of photosensor, either illuminated or dark, determines on (closed) or off (open) state of the switch. Since there are no contacts, there is no contact bounce or contact contamination. The 200 has a high gain npn phototransistor output. In on state with a LED drive current of 30 mA, a min output of 1.6 mA at 0.4 V assures TTL compatibility. Max output in off state is 20 μA at 12 V. The 200A contains a photodiode sensor followed by a Schmitt trigger circuit with 140-mA output sink capability, eliminating the need for amplifiers in most applications. **Optron, Inc,** 1201 Tappan Circle, Carrollton, TX 75006.
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LITERATURE

Solid-State Keyswitches

Describing design advantages of series 54, bulletin and application notes explain physical, electrical, and mechanical operating parameters. **Licon, Div Illinois Tool Works Inc,** Chicago, Ill.
Circle 300 on Inquiry Card

Power Supplies

Complete with charts and dimensional diagrams, bulletin provides specs, mounting and technical information, and custom design capabilities for each series. **Trio Laboratories, Inc,** Plainview, NY.
Circle 301 on Inquiry Card

DIP Reed Relays

Catalog features tables which present application data for static and dynamic characteristics, plus engineering data on high performance, low level, high voltage, and mercury wetted DIPs. **Magnecraft[R] Electric Co,** Chicago, Ill.
Circle 302 on Inquiry Card

Pushbutton Switches

Complete with specs, dimensional drawings, and wiring diagrams, catalog describes line of std lighted and non-lighted switches. **Centralab Distributor Products, Centralab Electronics Div, Globe-Union Inc,** Milwaukee, Wis.
Circle 303 on Inquiry Card

Integrated Circuits

Guide to converters, amplifiers, multiplexers, and multiplier/dividers in IC form consists of functional diagrams, drawings, and tables of specs. **Analog Devices, Inc,** Norwood, Mass.
Circle 304 on Inquiry Card

Tape Pac[R] System

Design and performance features, and digital, instrumentation, and audio recording specs on the 2000 series are covered in illustrated brochure. **Emerson Electric Co, Industrial Controls Div,** Santa Ana, Calif.
Circle 305 on Inquiry Card

Optoelectronics

Including seven sections, manual furnishes information relating to emitters, detectors, couplers, theory, system design, reliability measurements, circuits, symbols and terms, and specs. Send $3 plus applicable tax to **GE Semiconductor,** Electronics Park, Bldg 7-49, Syracuse, NY 13201.

Memory Modules and Systems

Literature package offers separate technical bulletins and general bulletin covering specs of replacement and add-on memory modules and systems. **Standard Memories, Inc,** Newport Beach, Calif.
Circle 306 on Inquiry Card

D-A Converter

Detailed tables, diagrams, and charts in booklet supply specs including transfer and electrical characteristics, ratings, operations information, and performance curves. **Precision Monolithics, Inc,** Santa Clara, Calif.
Circle 307 on Inquiry Card

Shaft Encoders

Including design features, applications, and electrical, mechanical, and environmental specs, bulletin describes the RS23 series of encoders. **Data Technology, Inc,** Woburn, Mass.
Circle 308 on Inquiry Card

Potentiometers/Networks

Summary specs are features of short-form catalog which covers expanded line of resistive components. **Bourns Trimpot Products Div, Bourns, Inc,** Riverside, Calif.
Circle 309 on Inquiry Card

Bus Interconnect Devices

Complete with design guide for bus bars and technical information, catalog concentrates on std line of miniature solderless, PC board, and DIP buses. **Bussco Engineering, Inc,** El Segundo, Calif.
Circle 310 on Inquiry Card

Switches

Highlighting slide, toggle, and rocker switches, 48-page design guide includes dimensional drawings; listings of types, shapes, sizes, colors, and part numbers; and engineering data. **CW Industries,** Warminster, Pa.
Circle 311 on Inquiry Card

Microcomputer Reliability

Covering test results, field reliability data, and failure mechanisms on the 8080 and 8080A microcomputer, "Reliability Report RR-10" includes device descriptions, block diagrams, and test curves. Write on company letterhead to Marketing Services, **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95050.

ASCII Code

Wall chart presents detailed description of all 128 ASCII characters, with alphanumeric name, and octal, hex, and other code designations. **Termiflex Corp,** Nashua, NH.
Circle 312 on Inquiry Card

Serial Printer

Brochure highlights technical specs and features of design and use of series T-1000 serial impact matrix printer. **Tally Corp,** Kent, Wash.
Circle 313 on Inquiry Card

Switches

Specs for the various types and sizes of switches are presented in catalog which gives information on mounting, hardware, accessories, and options. **C&K Components, Inc,** Watertown, Mass.
Circle 314 on Inquiry Card

Gate Turn-Off SCR

Operation, advantages, and applications of GTO-SCR are discussed in 8-page application note which also contains electrical specs and package description. **Unitrode Corp,** Watertown, Mass.
Circle 315 on Inquiry Card

Crystal Oscillators

Brochure details clock, oven controlled crystal, temperature compensated crystal, and voltage controlled crystal oscillators, as well as frequency stds. **Vectron Laboratories, Inc,** Norwalk, Conn.
Circle 316 on Inquiry Card

Plastic Optics

Applications, user advantages, and optical, physical, thermal, and chemical performance specs of components are discussed in illustrated technical bulletin. **Applied Products Corp,** Horsham, Pa.
Circle 317 on Inquiry Card

Aluminum Knobs

Features of various styles and sizes of knobs are pointed out in foldout catalog which provides photos, descriptions, and engineering specs. **Kurz-Kasch, Inc,** Wilmington, Ohio.
Circle 318 on Inquiry Card

Solid-State Devices

SSD-200D series databooks, one on power devices and the other on ICs, contain technical data on std line and abstracts on application notes. Price is $6 per volume; $10 for the set. Send check or purchase order to **RCA Solid State Div,** PO Box 3200, Somerville, NJ 08876.

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

GUIDE TO PRODUCT INFORMATION

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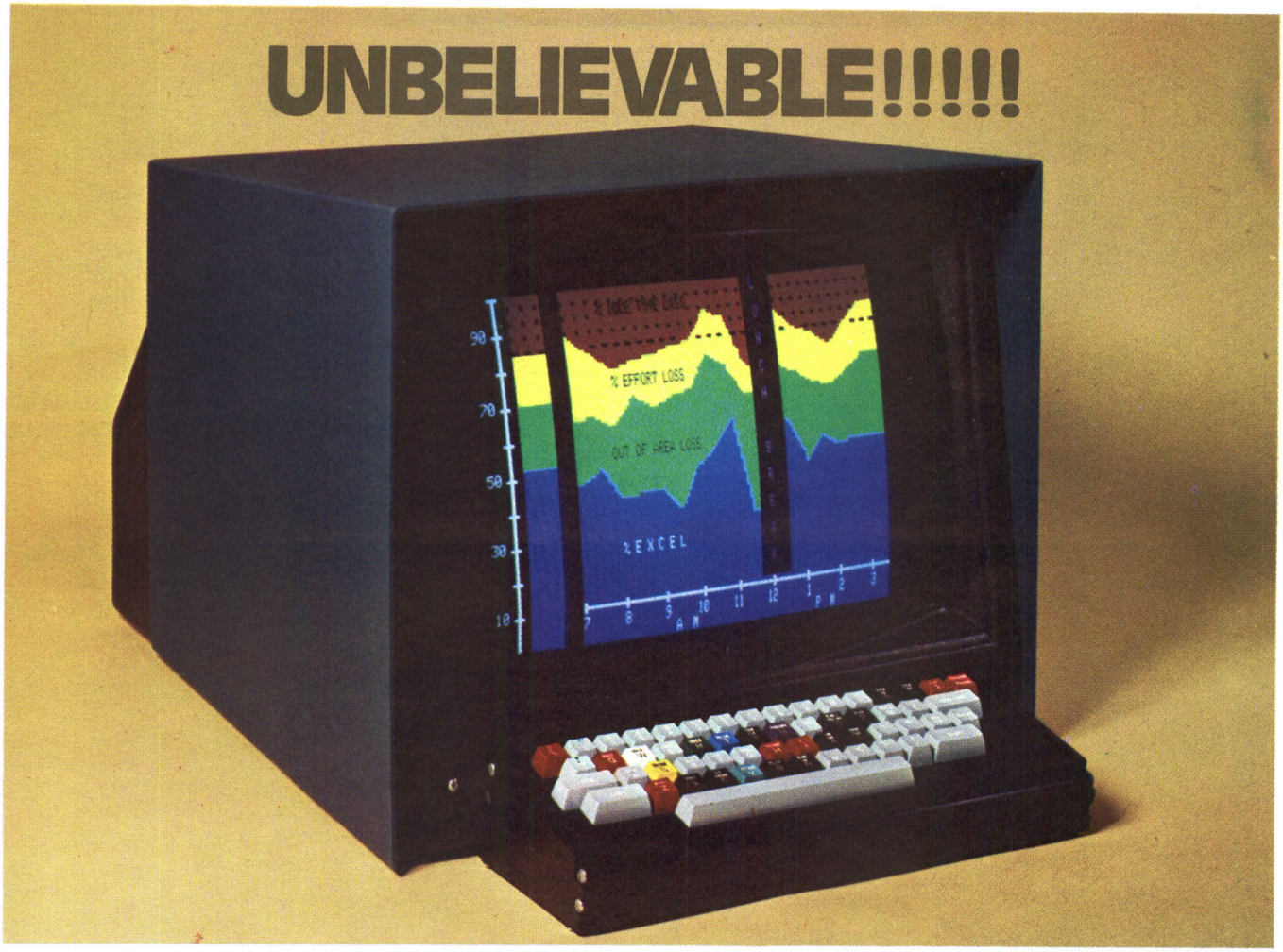

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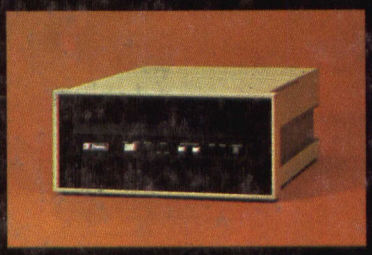

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