

# COMPUTER DESIGN

THE MAGAZINE OF MODERN DIGITAL ELECTRONICS

JANUARY 1967



HARDWARE FEATURES THAT AID PROGRAMMING

FOUR YEAR INDEX TO COMPUTER DESIGN

COMPARATIVE ANALYSIS OF IC LOGIC

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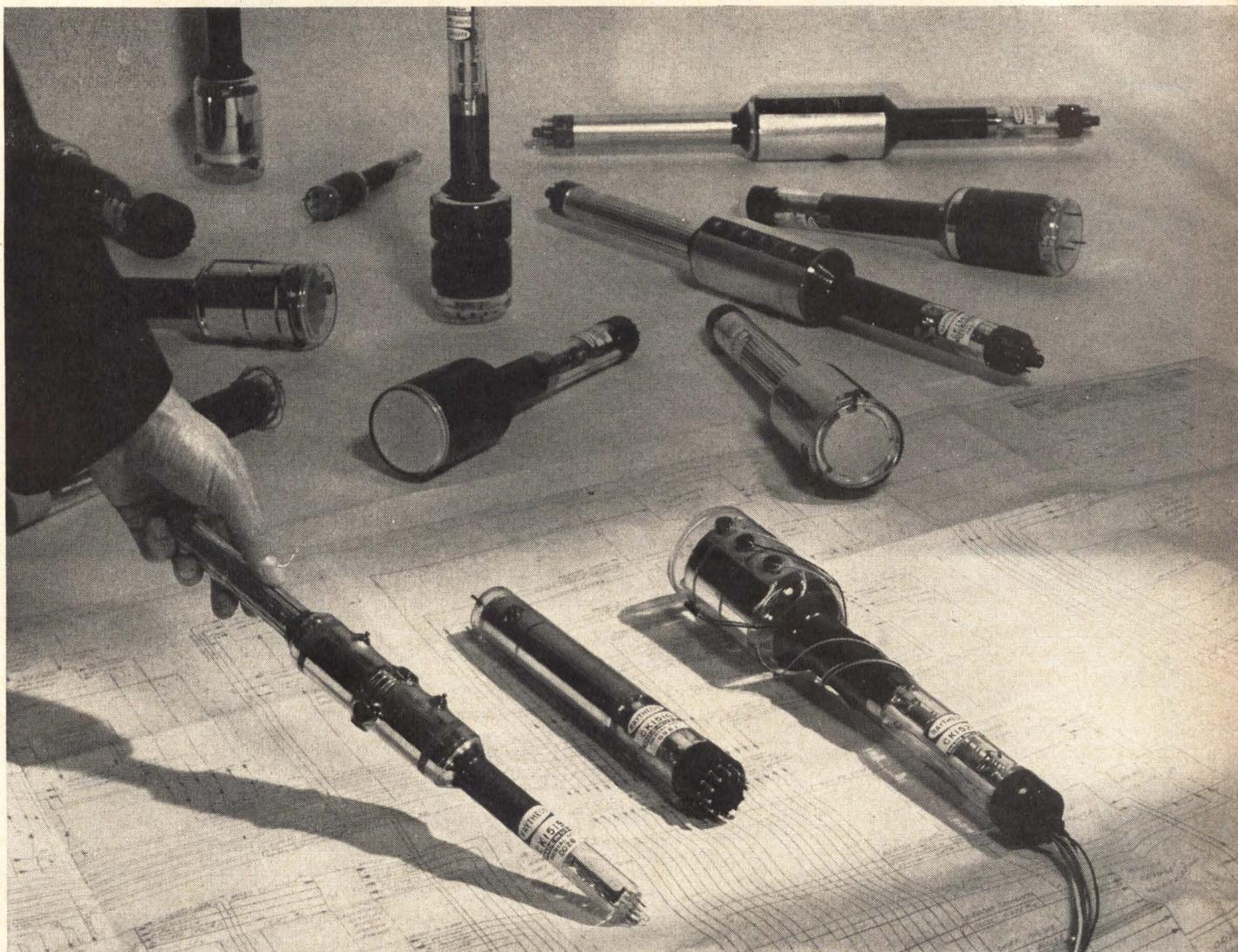
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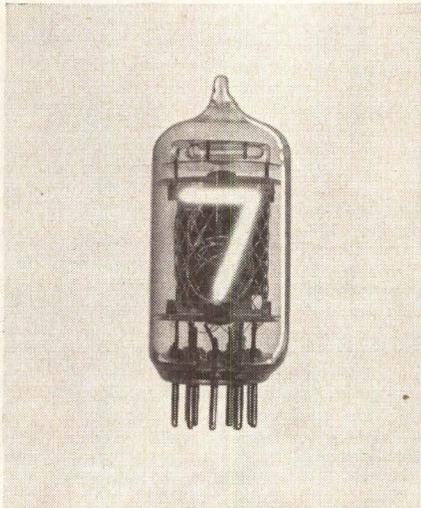
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devices which feature: fast write, immediate and nondestructive read, long storage, high resolution, and fast erase. Information can be written and stored using sequential scan techniques or by random access writing. Erasure can be complete or selective. Dual and single gun types are available.

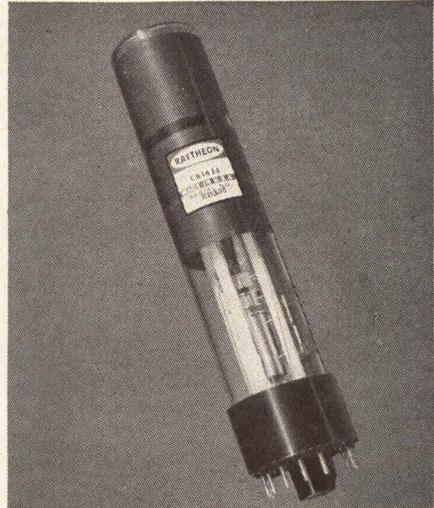
For more information or demonstrations, contact your Raytheon Regional Sales Office.



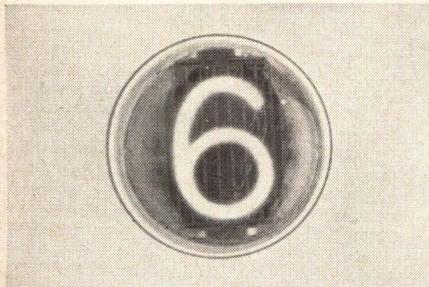
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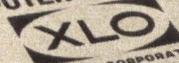


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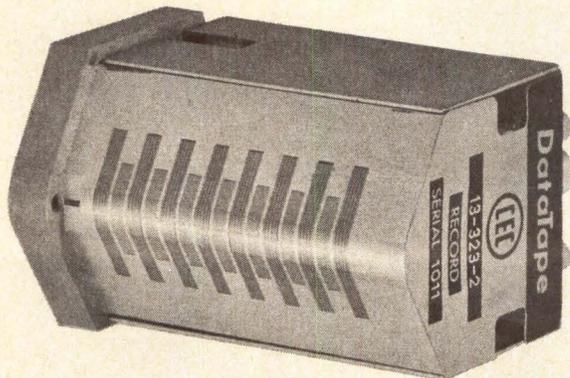
On Nov. 8, 9 and 10 at the Fall Joint Computer Conference, we'll triple the memory of a Bryant Series 4000 Disc File. Right before your eyes. It'll progress from an eight-disc single-positioner unit to 24 discs and dual positioners. Capacity—better than a billion and a half bits. We'll do it without a clean room. Without wasting time. Without a fuss. Want to watch? Visit the Bryant Exhibit. In addition, our famous Positioning Head Drum System (PhD) will also be in operation. They're the best memories you'll have of San Francisco.

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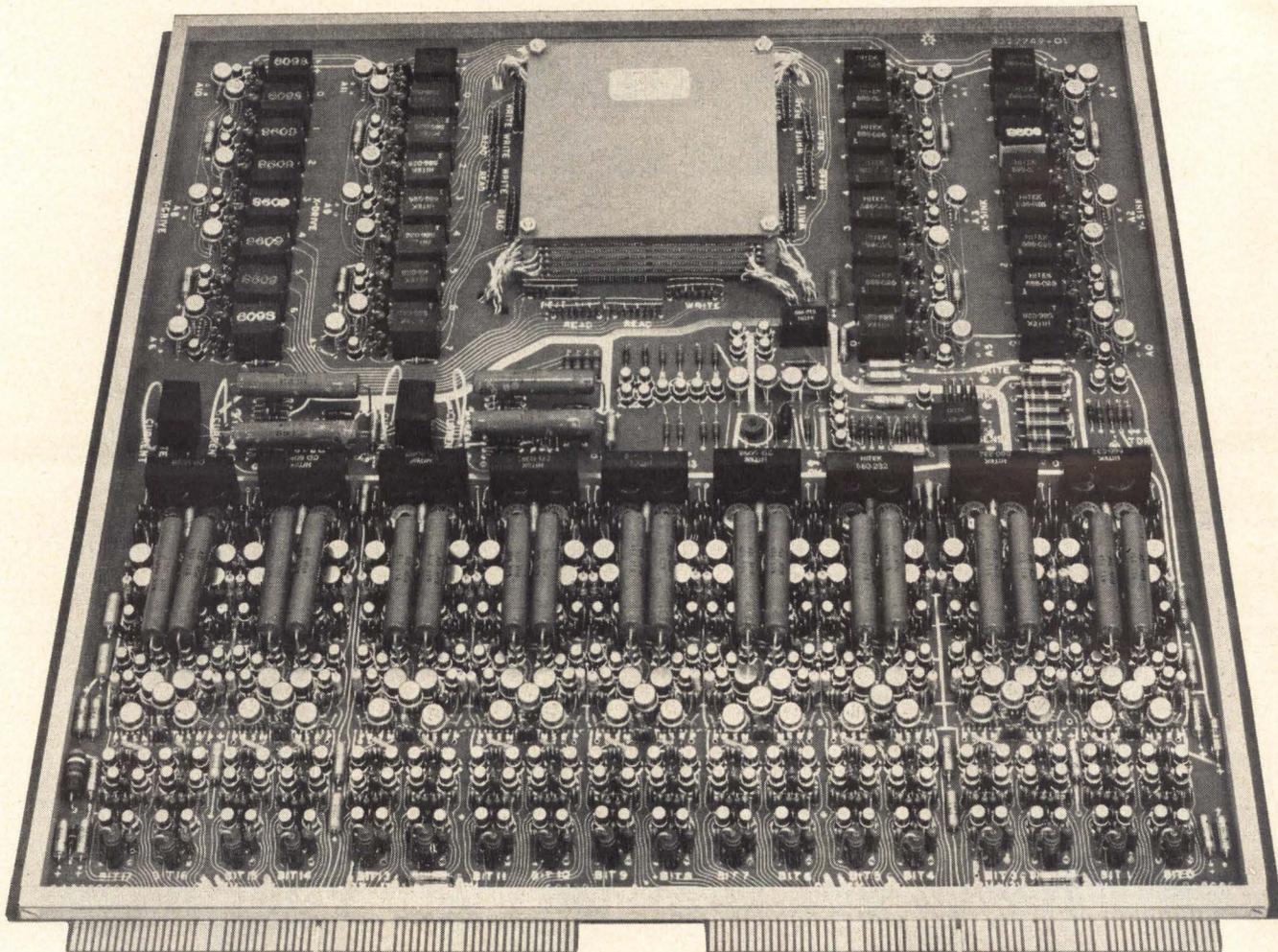
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**The extra plus you receive is speed.**  
CIRCLE NO. 11 ON INQUIRY CARD

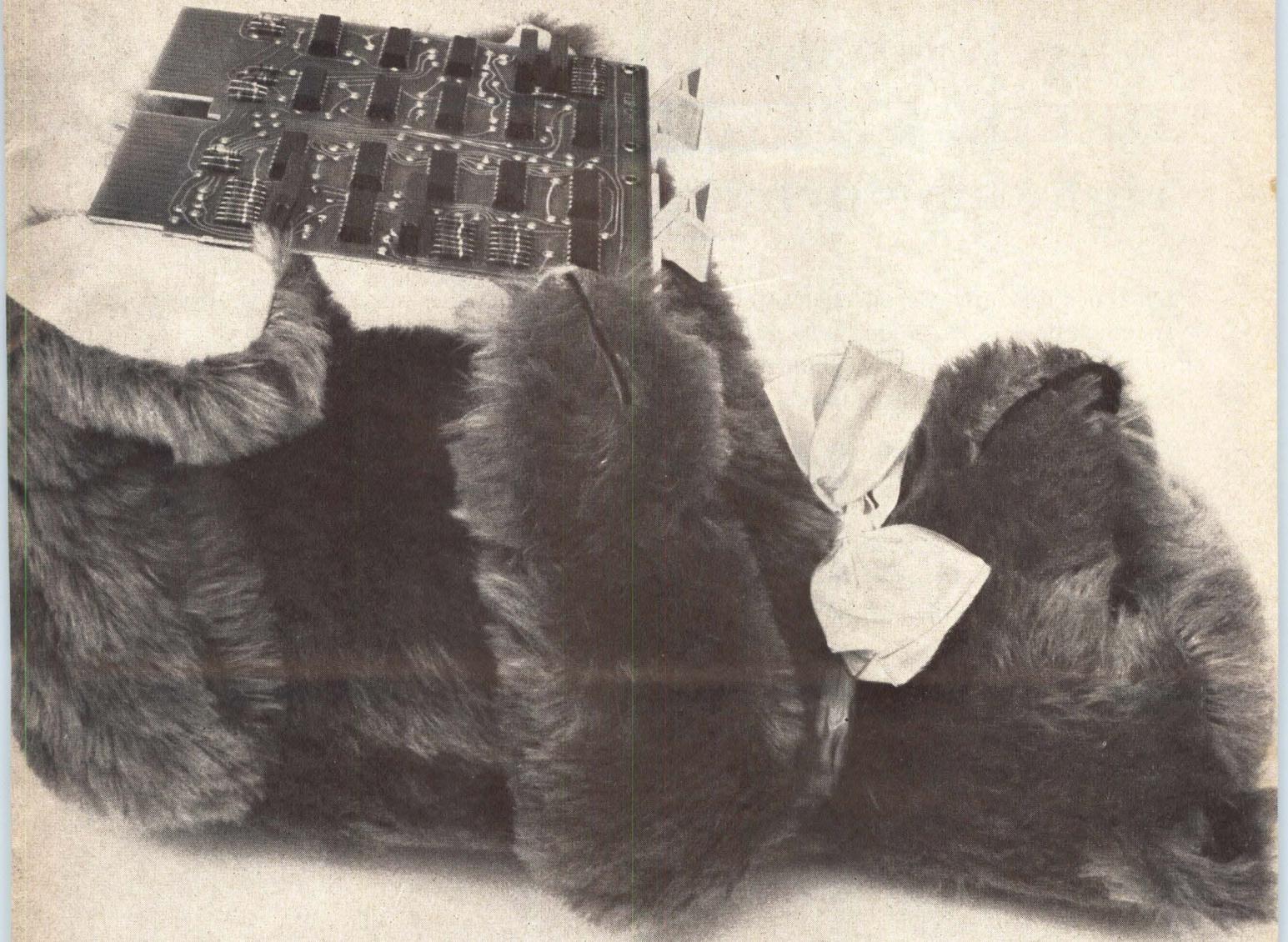
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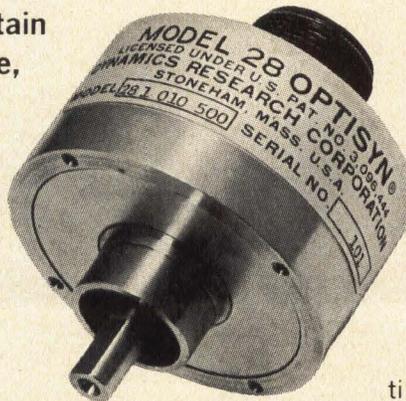
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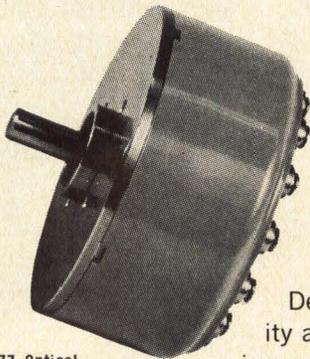
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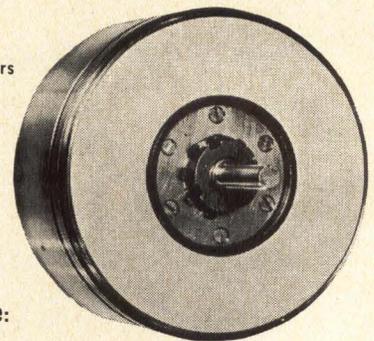


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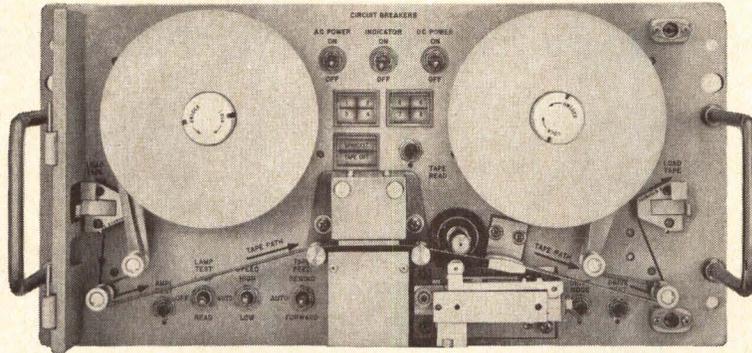
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\*18"W x 9"H x 8"D

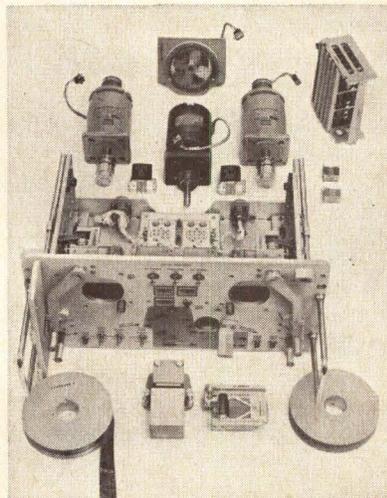
# MTBF=30000 hrs

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CIRCLE NO. 14 ON INQUIRY CARD

## LOGIC SYMBOLS STANDARDS —

### A Statement from the Editors of *COMPUTER DESIGN*

The interest of Computer Design in logic symbology has dated from the early days of our existence. In July, 1964, we published a lengthy article on the "Military Standards, Graphic Symbols for Logic Diagrams," MIL-STD-806B, then only two years old. In May, 1965, we published extracts from the dual ASA standard "Graphic Symbols for Logic Diagrams," ASA Y32.14. At that time, we made the point that no standard was generally accepted or in widespread use, and comments were invited from the readership.

In September, 1965, the CD Readers' Forum was established as a department of the magazine, with the logic symbology controversy as its first topic of discussion. CD went on record as agreeing that a universal standard is necessary and desirable for our dynamic industry, and offered its services in the effort towards getting a standard universally accepted. Comments, opinions, and enlightening information were invited. Comments, opinions, and enlightening information were received, and this month we review the activity to-date.

#### SUMMARY OF RESPONSES

Of the opinions received from CD readers, 64% unequivocally favored the universal adoption of MIL-STD-806B, and another 14% expressed the opinion that either 806B or the ASA standard would suffice, so long as standardization was achieved. One reader, on the other hand, voted to do away with all logic symbols. Some facts about the sample of readers who responded should be noted: no manufacturer of digital logic modules was represented; with the exception of IBM and RCA, the computer

manufacturers were also not represented; military contractors and government installations were heavily represented. Selected comments from the Forum response follow.

- No respondent disputed the need for a universally-accepted standard.

- The following arguments were advanced for the adoption of 806B:

1. 806B is required on military contracts; it is therefore certain to receive some use, and a rival standard would have to be greatly superior to justify retaining both standards within the same company, and changing between military and non-military contracts.

2. Y34.14 is not superior to 806B in any important respect; a U.S. Air Force study showed 806B to be superior at the level where most labor dollars are consumed.

3. 806B represents, in a straightforward manner, electrical logic and circuit functions, and is therefore useful to manufacturing and field personnel. Y32.14 introduces mathematical logic, with its associated complexities, but makes no contribution to the prime users of the diagram.

4. Drawings conforming to 806B pass easily and unchanged from engineering through production and publications.

5. The open right triangle in the ASA standard can be easily and accidentally changed to a filled right triangle.

- 806B has been adopted as a corporate standard or is in general use by at least fourteen companies, including RCA, Sanders, G. E., T. I., Signetics, Fairchild, EECO, and Sierra Research.

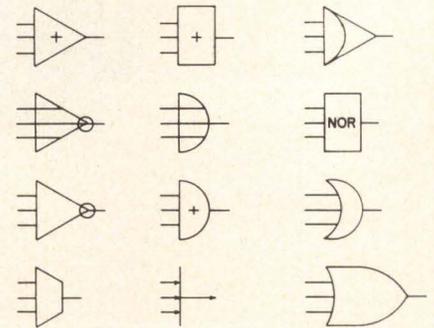


Fig. 1. These 12 different methods of representing an OR or NOR function were taken from brochures put out by 30 manufacturers of digital modules or integrated logic circuits.

- A variant of the uniform-shape set of Y32.14 has been adopted as the standard throughout IBM. Their stated reasons and precepts are as follows:

1. Rectangular blocks with internal mnemonic labelling are easier to handle for various drafting and presentation techniques; they are easily recognizable, easily recalled, and lend themselves to compact diagram structure; they are especially suited to the requirements of automation in the production of machine-printed diagrams.

2. Utility by the man who services the equipment is the most important factor. The IBM version of Y32.14 produces a logic diagram which can be used and understood by the field maintenance man without an intimate knowledge of the circuitry of which the blocks are comprised.

3. The standard provides a rigorous relationship between voltage level and function.

- IBM has had considerable success in getting their standard accepted on military contracts, because, apparently the government has accepted non-MIL drawings rather

than pay the price of conversion to MIL-STD.

- As more functional elements are integrally packaged (e.g., on an IC chip), the meaningfulness of logic diagrams on a Boolean element level will decrease; a case can thus be made for the demise of the logic diagram as we now know it.

- CDC, Univac, and Buships are also understood to be using the ASA standard.

### SURVEY RESULTS

A CD survey of the literature published on 35 lines of digital modules and circuits by 30 different manufacturers yielded the following data.

- Of 16 manufacturers of discrete-component logic cards, not one uses a "standard" method of logic symbology representation.

- Of 9 manufacturers of IC logic cards, two use 806B representation, one uses no symbology, the rest use some non-standard convention.

- Of 10 manufacturers of integrated logic circuits, eight use 806B representation.

The extent to which non-standardization creates chaos among logic diagrams can be seen in Fig. 1, which shows, as an example, twelve different methods which were used in 35 brochures (from the above module and circuit manufacturers) to represent an OR or NOR function. Clearly any reasonable standard is superior to this.

### WHERE DO WE GO FROM HERE?

Technically, there appears to be no reason why either 806B or Y32.14 would not make an adequate standard if universally adopted. Conversely, there is no real technical or economic reason for choosing one over the other. This also indicates that no third standard could be concocted which would be demonstrably superior to both 806B and Y32.14, and thus achieve universal acceptance. We have, therefore, in the abstract, a coin-toss choice between the two standards.

But we do not operate in the abstract, and a standard will not



## HIGH-SPEED PRINTERS Shepard\*

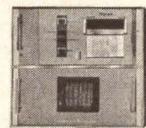
Pioneers in the design and fabrication of High-Speed Printers since 1950. The development of patented unique features, combined with computer technical experience, enables Shepard to offer one of the finest High-Speed Printers available. Proven installations for commercial and military systems such as POLARIS, MINUTEMAN, and MOBIDIC confirm the reliability of Shepard units.

The above illustrated Shepard Model 400 provides up to 200 characters per print line; and it, together with other standard models shown below, have printing speeds of up to 2,400 lines per minute — Data logging as well as computer printout — Extremely low RFI factor — Mounting for office, test bench, and rack — Life guarantee for hammers and print wheels.

Application limited only to your imagination. Whatever your needs may be for High-Speed Printers, consult our staff of qualified personnel.



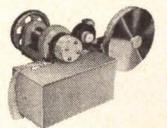
COMMUNICATIONS  
TERMINAL  
PRINTER 990



RACK MOUNTED  
"MINITYPER"\* 848



DRAWER MOUNTED  
"MINITYPER"\* 824



STRIP PRINTER  
SHEPARD\* 802

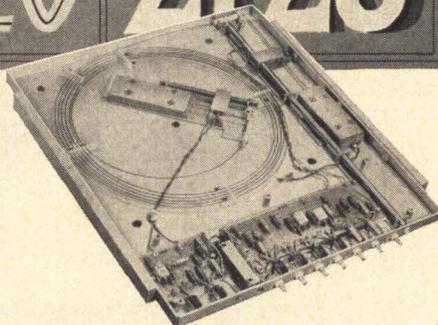
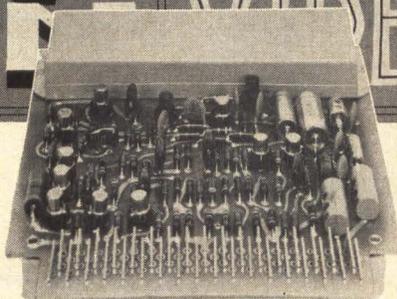
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CIRCLE NO. 15 ON INQUIRY CARD

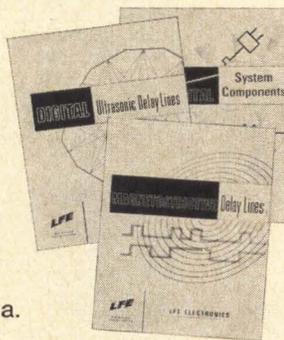
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delay lines for digital applications**

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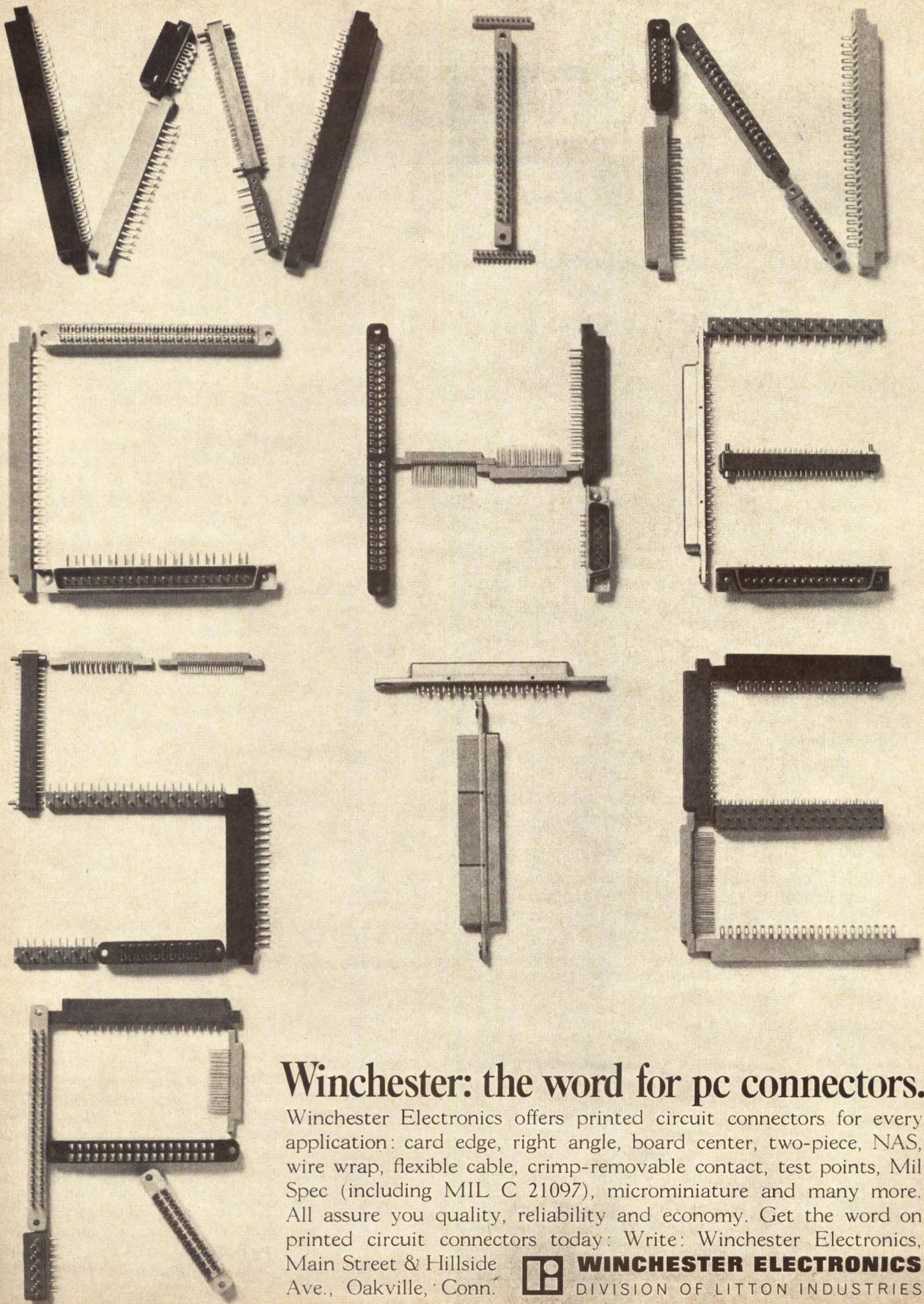
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CIRCLE NO. 16 ON INQUIRY CARD

be established through open debate, by secret ballot, or by the toss of a coin by the president of the IEEE (or the editor of Computer Design). A standard will probably come to be in general use through economic pressure somewhat similar to the magnetic tape standards of 200/556/800 bpi with 3/4-inch gaps.

Based on the response to this Forum to date, one could conclude that 806B is evolving as the de facto logic symbol standard. But we have yet to hear from many of the major computer manufacturers, all of the smaller computer manufacturers, the logic suppliers, and the peripheral equipment companies. With the single exception of IBM's Mr. Boden, we have yet to hear from those who strongly advocate the ASA standard. (One might conclude from this that there are few such advocates, or that they either lack the courage of their convictions or are unable to present a convincing case for Y32.14.) We recognize that the contest between Y32.14 and 806B has become an emotional one in some quarters, personalities have become involved, and political cliques have formed. We deplore this as unprofessional, unwise, and deleterious to the efficient practice of the digital art, and we shall not be a part of it. Computer Design advocates only one thing: that there be a generally-accepted standard for logic symbology. We have no preconceived bias towards either 806B or Y32.14. Neither is perfect, but from them will come the standard.

Ideally, a compromise between the two standards might be indicated, but the basic and apparently irreconcilable matter of the right triangle vs the circle presently prevents such a compromise. We offer the pages of the CD Readers' Forum for the presentation of further opinions, statements of policy by companies who have not yet been heard, and constructive suggestions for resolving the 806B vs Y32.14 conflict and developing a true standard. Our editorial staff will solicit the views of key men in the industry, and we offer our presence to any gathering of persons devoted to resolving the problem. Let us put this facet of our professional house in order.

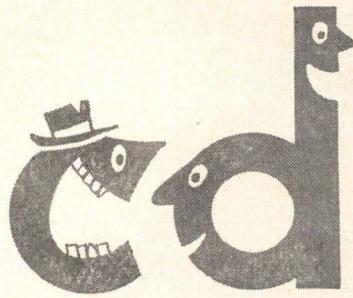


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## commentary

Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of T. PAUL BOTHWELL, Contributing Editor.

# DIAGNOSTIC PROGRAMS: GREAT EXPECTATIONS?

JOHN E. THRON

Once its measure is taken in an actual test or maintenance environment, a computer-system test program all too often falls far short of the expectations of both the program designer and test or maintenance technician. **Why?** Generally, because the expectations are unrealistic. This is nearly always true with computer diagnostic programs, where expectations are based on an oversimplified view of the diagnostic process, in which the impossible is looked upon as an objective to be somehow approximated. Both user and designer set their goals on the unattainable, and inevitable shortcomings of a program are innocently obscured by the designer. Thus, a program becomes an unpredictable tool, and its value is thereby far more limited than either designer or user expected it to be.

The development of economically justifiable diagnostic programs depends upon a realistic definition of each program's function within the over-all test or maintenance procedure. This definition must be thoroughly understood by both the designer and user. Realistically, there are three major functions that might be programmed in the test and maintenance procedure: (1) exhibition of symptoms, (2) detection of failure, and (3) isolation of faulty component. Let's look at these one at a time.

### Not Every Symptom Can Be Programmed

Although a computer system exhibits the symptoms of its own failings, it cannot be programmed to exhibit all those failings it may possibly have. The number of discrete states a computer system may

The author of this month's CD Commentary, John E. Thron, is a staff engineer at Honeywell's Computer Control Division. He is responsible for computer systems design.

assume is staggering; the number of sequences of such states is infinite. Yet a fault **may** occur only within **one** sequence of states. Although it is advantageous to exhibit symptoms under controlled conditions, it is unrealistic to expect that, should any system exhibit the symptom of a failure, the diagnostic program should exhibit some symptom of the failure. There **are** going to be failure situations in which the repair technician is on his own.

### Failure To Detect

The detection of failure, i.e., the recognition of symptoms **as** symptoms, is quite different from their exhibition. And detection is surely a function that cannot be entirely programmed, if only because the symptoms themselves are not available to the program. For example, a missing ink ribbon in a line printer is a fault whose symptoms may be easily exhibited under program control, but are not available for programmed test — at least in a normal computer system. Again, impermissible variations in basic computer clock frequency can usually be exhibited, but not detected, by program.

Thus, even assuming that the symptoms of a fault can be exhibited under controlled conditions, it is unreasonable to expect that diagnostic programs should, in all cases, detect the presence of a fault. An exchange of information between technician and computer program is a necessity at this stage.

### Isolating The Fault

Even if symptoms are exhibited and failures are detected, it still isn't easy to identify a faulty system component through programmed analysis. Although fault identification is the analytical process which presumably characterizes the diagnostic program, there are fundamental limitations to the program that reduce the probability of achieving this goal. For one thing, several replaceable components may be logically indistinguishable. Their functions may have to do with pure power amplification, transient storage, interconnection, etc. In such cases, isolation must be performed by trial replacement. Also,

# Does your present custom power supply give you...

70% to 90% efficiency?

?

Instant fault repair by plug-in module replacement?

?

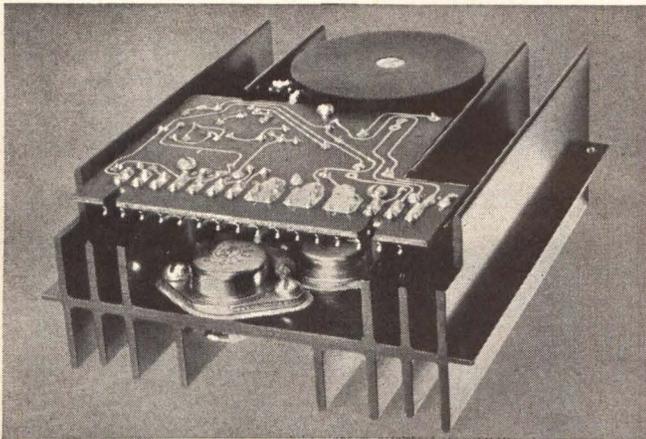
Add-on power capability by using more modules?

?

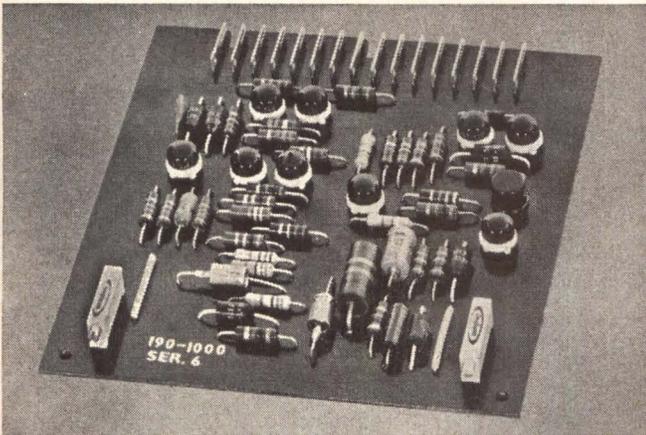
Ability to handle full load steps while maintaining output in regulation band?

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## New Omnimod does!



Omnimod power control module.



Omnimod control amplifier.

OMNIMOD gives you all these features—and more—and at a lower price! Want to know more?

OMNIMOD is a dc to dc converter using transistors in a CONSTANT PULSE WIDTH, variable repetition rate switching mode to regulate output voltage or current. Two small plug-in units make-up the OMNIMOD concept—a power control module and a control amplifier.

Output can be regulated between  $\pm 2$  and  $\pm 60$  dc at up to 20 amperes using the OMNIMOD family of modules WITHOUT MODIFICATION OR ADJUSTMENT. Higher current ratings are obtained by paralleling power control modules.

Any number of power controller modules can be controlled by one amplifier. OMNIMOD has a current limiting parameter, over voltage protection, voltage sequencing, and remote sensing.

To design a custom power supply, one must simply

1. design one input power converter to change unregulated line ac power to unregulated dc power
2. select the number of plug-in OMNIMOD power control modules to supply the power needed for each output
3. package these elements with filter capacitors and a plug-in amplifier module for each output

All the power used by every element in a typical data processing system could be supplied by custom power supplies constructed with interchangeable OMNIMOD modules.

Isn't this enough to consider OMNIMOD for your custom requirement? We will design an OMNIMOD custom power supply to your specs, or will help you design your own system using our plug-in OMNIMOD modules.

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**μVL** same MicroVersaLOGIC

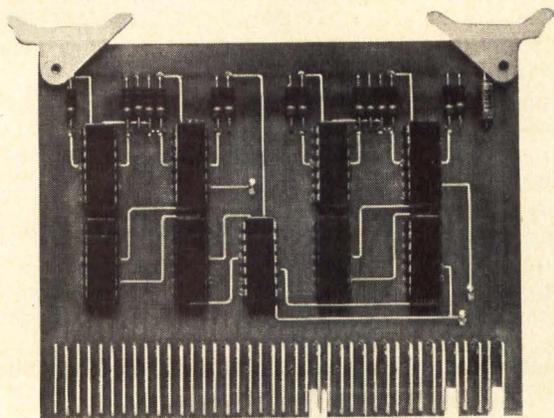
**μVL** same performance

**μVL** same reliability

**μVL** from Decision Control

**μVL** now costs . . .

**33%** less!\*



We've reduced MicroVersaLOGIC prices sharply, thanks to lower microcircuit prices.

Get the same reliable performance—same proven DTL circuits—5 v. logic levels—plenty of output drive—single power supply—complete mounting hardware available.

If you're building a digital system, build it with MicroVersaLOGIC and really save time and money. We'll show you how—in our uVL applications brochure. Send for it today.

*\*average module price reduction*

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a necessary step in the diagnostic process may result in loss of programmed control of the system, producing unpredictable, spurious diagnoses, or at least prematurely terminating the test.

But a more serious problem exists: the diagnostic program must cope with improper variations in the **quantity**, as well as quality, of components. This problem, most frequently found in the manufacturing test environment, persists in some degree throughout the life of a complex system. It follows that neither the equipment tested, nor the programmed equipment being used as a tool, is a known quantity. A single wire, installed where it should not be, may affect only an obscure sequence of computer states, appearing in one use of one computer system. Yet the diagnostic anticipation of the effects of all possible "extra" wires is impossible.

#### Precise Definition Of Tasks

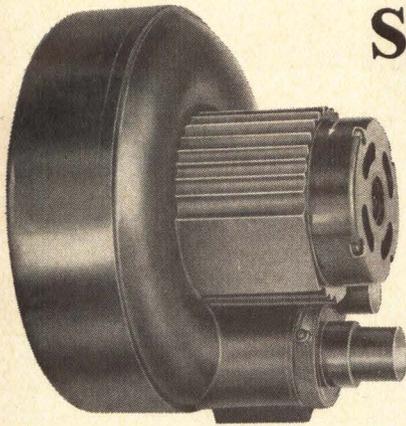
Obviously, none of the three major functions in the test and maintenance procedure can categorically be assigned to the diagnostic program. Instead, although it is a complicated task, the exact functions such a program is to perform have to be specified. It must be determined which functions must be program-assisted, and which will benefit the user. The expected limitations, as well as the skills of the user, must be determined, too. His understanding may set the upper limit on justifiable programming effort.

False expectations of designer and users are the price paid for failure to define precisely the selected, limited tasks of programs designed for use in the test and maintenance procedure. Don't set your sights higher than they should be, and you won't be disappointed.

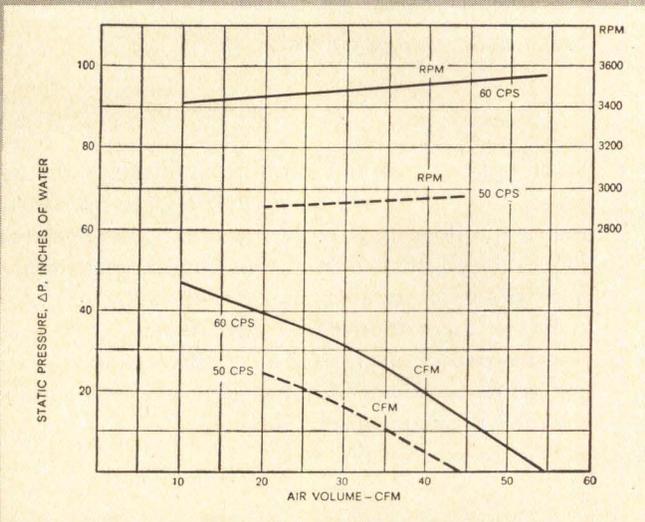
#### CALL FOR PAPERS — 1967 FJCC

A call for papers has been issued by the Program Committee of the 1967 Fall Joint Computer Conference to be held Nov. 14-16 at the new Anaheim Convention Center, Anaheim, Cal. Harry T. Larson, Technical Program Committee Chairman, is requesting papers covering significant advances in any aspect of the information processing field, including hardware, software, systems, applications, and analog/hybrid systems. Mr. Larson also added that a \$500 prize will be awarded by the American Federation for Information Processing Societies, the sponsor of FJCC, for the best paper presented at the conference. Deadline for papers is April 17, 1967. A complete manuscript is requested in addition to a 100-word abstract. Five copies should be sent to Mr. Larson, 1967 FJCC, P.O. Box 457, Costa Mesa, Cal. 92627

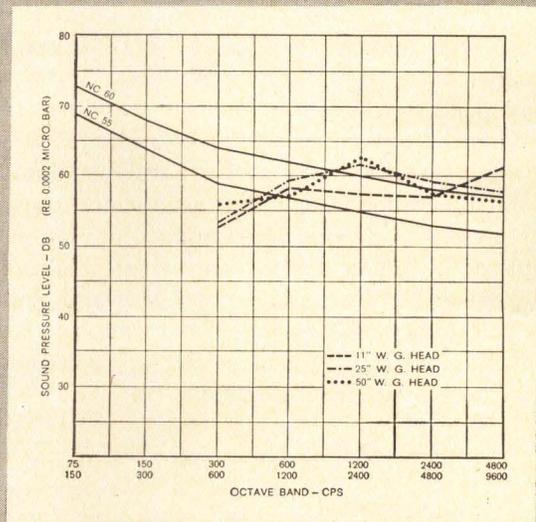
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ACOUSTIC DATA (60 CPS)

## You can now—from the new Diehl Series 925 vortex blower.

For the first time it is possible to get high pressure or vacuum air delivery in a single stage blower at low rpm. Getting this performance from a single stage instead of two or more means: less weight, less bulk, lower cost, lower noise, longer life and easier servicing. The blower that offers these advantages is the new Series 925 Diehl Vortex Blower.

In this blower the air is made to flow in a forced ring vortex, leaving and re-entering the impeller several times during the course of a single rotation. Its high performance is achieved at low rpm without positive displacement of

the air, thus insuring long life. Noise levels are generally below the N.C. 65 curve through resonant sound absorbers which permit direct inlet and outlet of air from the unit. The open finned motor is self cooled by forced convection. Throughout its design this vortex blower has a minimum of working parts to assure reliability. For applications of up to 34" of head of water the Series 915 Diehl Vortex Blower should be considered.

Clip the attached coupon for a copy of Diehl's new 8-page Bulletin 514 which describes both the 925 and 915 blowers.

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- Please send a copy of Bulletin 514.
- Please have a salesman call.

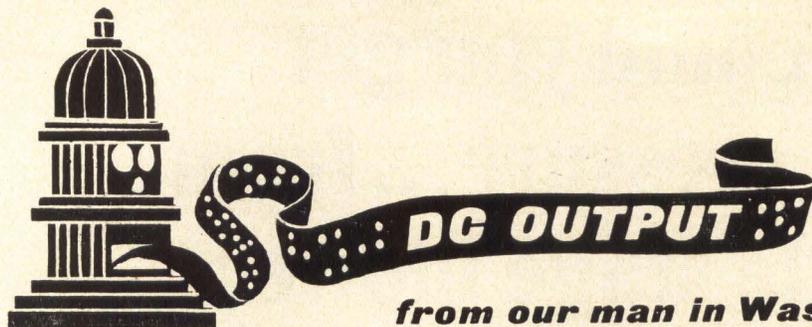
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D-122



The Federal Communications Commission has started a public inquiry into the regulatory and policy questions raised by the growing interdependence of computer services and communications services of common carriers. FCC is seeking answers to a number of policy and regulatory questions which come under its authority. Specifically, FCC wants to know whether legislation is needed for government regulation of computer service or is required to protect the privacy and proprietary nature of data; if, and under what respect, public policy requires regulation of computer services or whether those services will evolve better in a free, competitive market; if the services and facilities offered by communications common carriers are compatible with present and anticipated communication requirements of computer usage; and what measures are being taken by the computer industry and communications common carriers to protect the privacy and proprietary nature of data stored in computers and transmitted over communications facilities.

.....

A National Data Center to be responsible for assembling in a single facility all large-scale systematic bodies of demographic economic, and social data generated by the data collection or administrative processes of the Federal Government has been urged by a Bureau of Budget task force. The task force made it clear that even with a National Data Center it is obvious that every policy agency, as well as many administrative units, will require analytical capabilities for program planning and program evaluation. But, they add, current technologies, including distant consoles connected with a central computer facility by telephone links, make compatible decentralized use of data for analytical purposes with highly centralized data storage and processing.

.....

Japanese buyers have a strong interest in U. S. advanced electronic equipment, reports an export mar-

ket survey of the Commerce Department. The survey shows a heavy demand for industrial instrumentation, especially automation and process control equipment tied into digital and analog computers. Reliability and multi-function capability are stressed, with emphasis on solid-state and non-contact devices. Instruments with high sales potential include those capable of monitoring steady value control as well as proportional and variable control.

.....

Small businessmen will profit from efforts of the Senate Select Committee on Small Business to spread information on how they might use EDP. The Senate group is working with the Small Business Administration on a program for small businessmen in the use of computers as tools to improve management. These activities are expected to result in a SBA handbook, accompanied by seminars and other aids, to provide guidance to small business on the subject.

#### Recent Government Contracts .....

**SYSTEM DEVELOPMENT CORP.**, Santa Monica, Cal., received a \$2,000,000 increment to a previously-awarded contract for the procurement of satellite control computer systems. The Headquarters, Air Force Satellite Control Facility, L. A., Cal., is issuing the contract.

**LEAR SIEGLER, INC.**, Grand Rapids, Mich., has been awarded a \$3,528,183 fixed-price contract for loft bomb computer systems. The Naval Air Systems Command is issuing the contract following competition in which two bids were received.

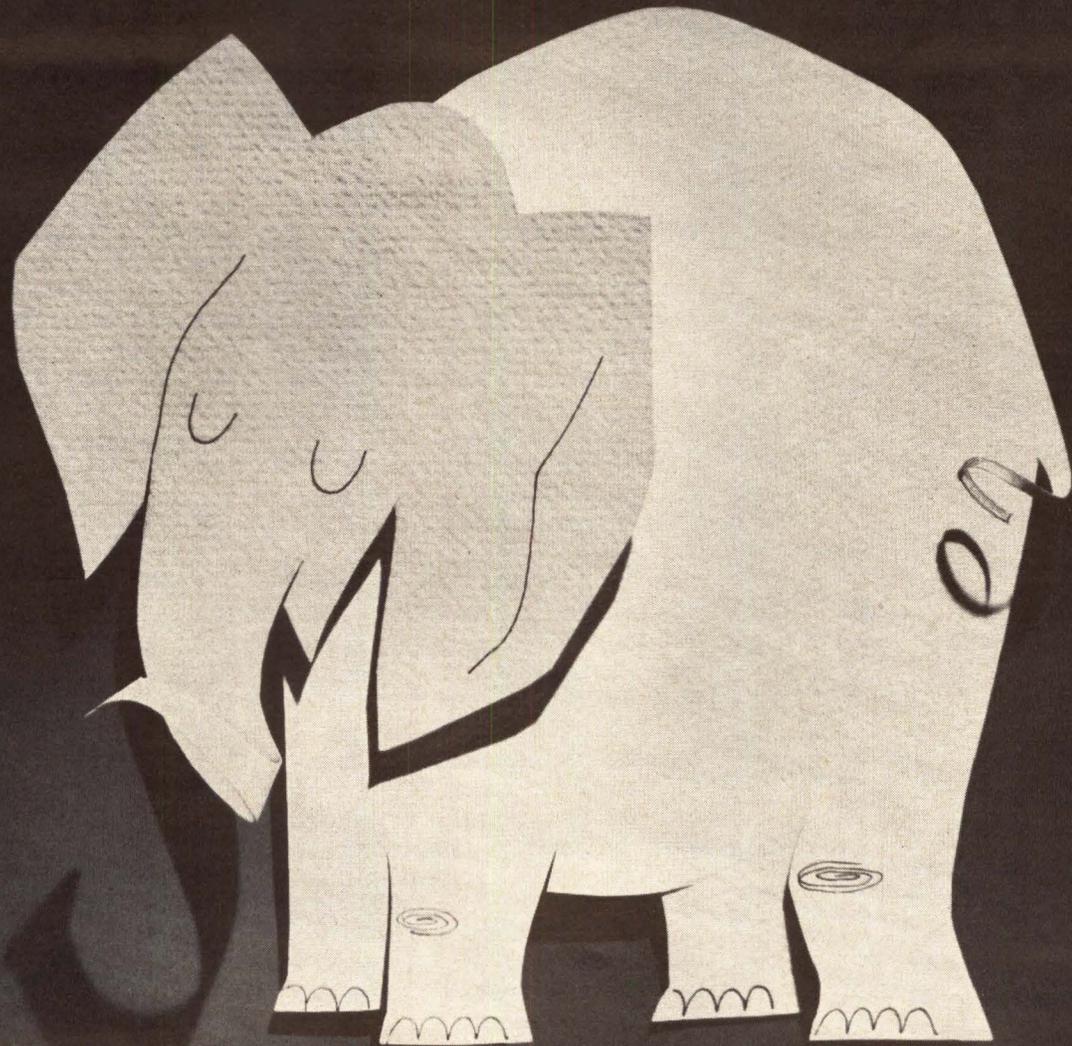
**LITTON INDUSTRIES, INC.**, Guidance and Control Systems Division, Woodland Hills, Cal., has been selected by NASA for negotiations on a contract for the design, fabrication, and checkout of the data automation subsystem (DAS) for the unmanned Mariner flights to Mars in 1969. Total value of the work on the subsystem is estimated at \$3 million.

Memory core testers bought more on price than performance are a lot like white elephants. Nice to look at, maybe. But darn expensive to have around. They have a nasty habit of letting bad cores slip by every now and then. And one bad core on the loose in a plane or stack spells high cost trouble. This kind of hit and miss testing never happens with CTC systems. They deliver driving pulses with unmatched precision and controllability; detect and measure core response with the kind of accuracy that weeds out even the borderline baddies. □ White elephants are the big reason you can't afford cheap core testers. You never really stop paying for them. With CTC memory core test systems you pay just once. And in the long run that's peanuts.

**COMPUTER TEST CORPORATION**  
Cherry Hill, New Jersey



**a  
white  
elephant  
is just  
a trunkful  
of bad cores**



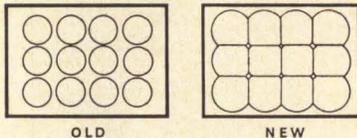
# Why the most readable readouts have a new lens system.



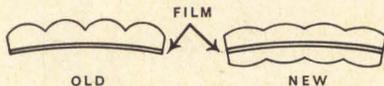
SERIES 120  
3/4 ACTUAL SIZE

We've just designed a totally new lens system for our miniature rear-projection readouts, the Series 120 and the Series 220 (front plug-in model). Since we already had the most readable readouts made—even with the old lens system—why all the effort?

Frankly, the most important thing we (or any other readout manufacturer) have to sell is readability. That's why we keep on working to make the best just a little bit better. This time it really paid off. Our new lens system delivers a significant increase in character sharpness and a 50% increase in brightness! Here's what we did:



First we squared our circular lenses. That gives us greater usable lens area for a two-fold effect: the new larger lenses collect more light; magnification required is reduced. Both factors increase brightness and sharpness.



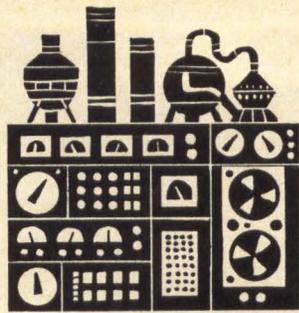
Second, we split the old single condenser lens and made a lens-film-lens sandwich. The old lens refracted light rays toward the projection lens before the rays passed through the film. Of necessity, the lens had steep curvature which limited the usable size of film. The new split-lens condenser refracts light in two stages: before it passes through film and after. By comparison, the new lenses are practically flat, permitting use of larger film and reducing aberration associated with thick lenses. The effect builds up: larger film means less magnification which in turn means greater brightness and sharpness.

So that's why the most readable readouts have their new lens system. Frankly, this new lens system may not seem earthshaking to you, unless you happen to be using readouts. In any case, send us your inquiry. We'll give you the reading on readability!

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CIRCLE NO. 21 ON INQUIRY CARD



## INDUSTRY NEWS

"THE SPRAWLING TEXTILE INDUSTRY HAS SAMPLED THE IMPACT OF THE COMPUTER REVOLUTION and is taking an active part in it." "Process computer automation is receiving the direct attention of textile companies." These statements were made during the recent Southern Textile Show by R. C. Berendsen, Manager of General Electric Company's Process Computer Business Section, Phoenix, Ariz. "The nation's textile industry, like other basic industries, is experiencing rapid technological change and growth, and has many opportunities to make economical use of the process computer," he said. "The industry is changing physically from thousands of small, highly-specialized companies to a number of large companies. Although there are many textile firms in operation today, the market share of the 10 largest has climbed dramatically in the last decade," he added. Berendsen listed several reasons why he believes that the technological revolution is having an impact in textiles. For example, teams of professional managers are entering the textile industry in increasing numbers and are bringing with them management techniques developed in highly-automated industries. "Research and development turn ideas into radically-new products whose manufacture often requires new plants and processes, which in turn offers

management new opportunities to design the new mills around various control mechanisms and instrumentation tied into process computers such as the GE/PAC 4000 line," he said. He named the areas in which GE process computers can make substantial contributions to the industry's efficiency and profits: regulating and timing process conditions on the batch dyeing (dye beck) machine and the finishing (range) machine; production accounting and malfunction analysis in weaverrooms and fiber spinning plants; dope preparation or chemical recovery systems; color control for synthetic fibers; monitoring and tensile testing of yarn; non-woven fabric manufacturing; waste reduction in pattern-cutting; pattern scaling; and production scheduling.

WESTERN UNION ANNOUNCED THAT IT HAS PLACED A \$500,000 ORDER FOR 80 HIGH-SPEED DATA TRANSMISSION TERMINALS WITH THE TALLY CORP. The equipment will be incorporated into the communications company's broadband service for domestic and international data transmission, and will be leased directly to subscribers. The Tally System 311 transmits and receives computer-ready data at speeds up to 1,200 words-per-minute and provides fully-automatic error detection and retransmission of corrected data.

Circle No. 22 on Inquiry Card →

# First come first served.

You can have all the SDS T Series integrated circuit modules you want now. We're in full production.

All T Series active elements are integrated circuits and guarantee reliable operation at clock rates to 10 mc. Each circuit output drives 14 unit loads, even after generous allowances for wiring capacitance.

Outputs switch 60 ma (4 times more than standard IC's). Noise rejection is at least 1.5 volts at the 0 and 4-volt logic levels.

SDS Natural Logic gives you AND and OR as well as NAND and NOR —

Each card uniquely keyed for proper installation.

Test points.

Ground plane laminated through middle of entire glass-epoxy board.

Load resistors separate from IC's for heat isolation.

Discrete diode-resistor inputs for gating flexibility, high noise rejection.

Four pins reserved for ground lines.

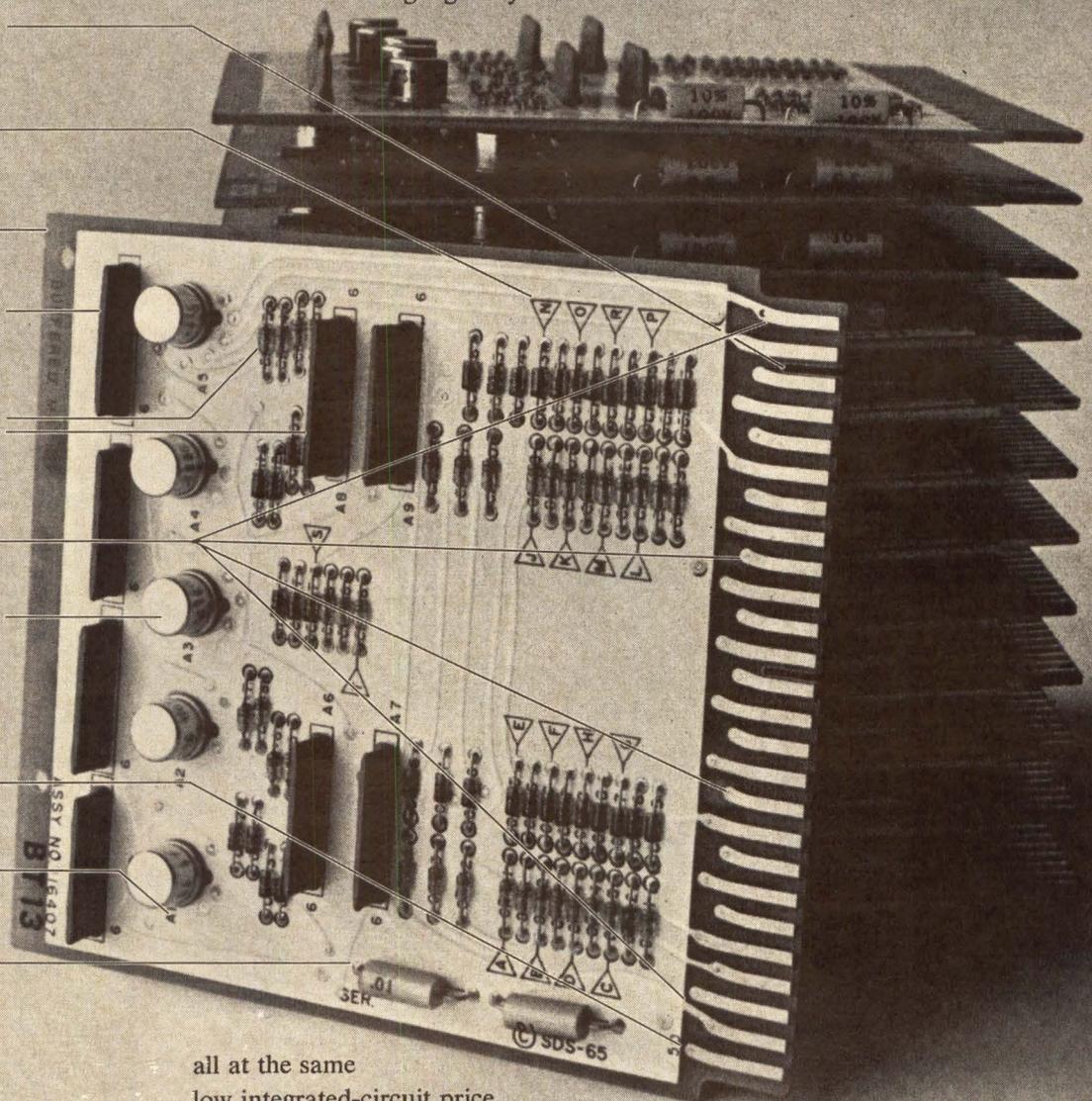
Four integrated-circuit buffer amplifiers in each hermetically sealed TO-5 can.

52 ribbon connectors (26 each side) for easy access to all circuits.

All components clearly identified.

Individual power line filters.

Actual size 4¼ x 4¾.



all at the same low integrated-circuit price.

We designed these modules for our new Sigma computers, but we also intend to become the largest manufacturer of logic modules for system designers.

We don't want to give away any of our Sigma secrets. But we'll sell them pretty cheap.

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Scientific Data Systems,  
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## INDUSTRY NEWS

THE WORLD'S LARGEST FILE OF PUBLIC OPINION DATA, COVERING NEARLY 400 MILLION ANSWERS TO QUESTIONS ASKED IN POLLS SINCE 1936, WILL BE MEMORIZED FOR INSTANT RECALL by a high-speed computer at the Roper Public Opinion Research Center at Williams College. Within the year, the computer will be linked experimentally by telephone line with 3 other academic institutions, giving scholars at widely separated locations direct access to a fund of social science information. The computer, an RCA 301, was donated to the Roper Public Opinion Research Center by the Radio Corporation of America, whose President, Robert W. Sarnoff, called the project "a dramatic illustration of the immense versatility of computers in providing entirely new services of social, economic, and political importance."

A SECOND-SOURCE AGREEMENT COVERING THE PRODUCTION OF TTL INTEGRATED CIRCUITS HAS BEEN ENTERED INTO BETWEEN MOTOROLA AND SYLVANIA ELECTRIC PRODUCTS, INC. According to S. L. Levy (Asst. General Manager), Integrated Circuits, Motorola's Semiconductor Products Division plans to manufacture and make available TTL integrated circuits equivalent to and interchangeable with the Sylvania SUHL family, and for this purpose will be licensed under applicable Sylvania patents. According to A. B. Phillips, General Manager for Sylvania's integrated circuits, the agreement was based on the mutual recognition by both companies of the rapidly growing military and commercial markets for these TTL integrated circuits.

THE NATIONAL LIBRARY OF MEDICINE HAS AWARDED THE AUERBACH CORP. A CONTRACT TO DEVELOP SYSTEMS SPECIFICATIONS FOR IMPROVING AND EXPANDING THE MEDLARS SYSTEM, known as the Medical Literature Analysis and Retrieval System. The MEDLARS system provides computerized bibliographic control over the world's medical literature. Over 175,000 articles are indexed and entered into the system annually. The MEDLARS system compiles and typesets automatically Index Medicus, a monthly index to current medical literature. In addition, users throughout the world are provided with computer-generated bibliographies on demand. The Auerbach contract will involve the examination of new areas of application for the computer. Of key importance is the mechanization of card catalog and serial record; on-line indexing and citation input; a special drug information module; and graphic image retrieval. In addition, a key aspect of the Auerbach effort will be a careful analysis of the requirements for further decentralization of MEDLARS search centers.

A CORNELL UNIVERSITY PROFESSOR CLAIMS TO HAVE SOLVED A PROBLEM THAT HAS PERPLEXED THE COMPUTER INDUSTRY: HOW TO KEEP AN INFORMATION TAPE WOUND AND FLAT AT THE SAME TIME. After several years study in conjunction with engineers from IBM, Harry D. Conway, professor of theoretical and applied mechanics at Cornell's College of Engineering, reports an answer to the problem. In order to make a wound tape flat, make an unwound tape uneven. Where, and how, and exactly to what extent the tape should be made uneven is the subject of a scholarly paper prepared by Conway and two IBM engineers, Wayne E. Nickola

and Keith A. Farnham of the firm's Systems Development Division in Endicott. The problem is one most people would think doesn't exist even after their attention is drawn to it. Take any roll of tape and one glance is sufficient proof that the width across the tape is a perfectly flat surface as it is wrapped around a perfectly round core. It's not so. The instant the flat tape is wound around the core the apparent flat width becomes dished. Need proof? Conway suggests this: take any long flat eraser and bend it in a semi-circle. The outside, that is the convex length of the eraser, becomes concave or dished across its width. This experiment magnifies what occurs on the super-thin information tapes in complex computers.

The phenomenon causes a number of problems, Conway said. As the tape is traversed by the reading head, the outside edges of the tape may rub and the inner portion may not even make contact. Three things may then result: the tapes wear, information is erased, and other information is not picked up by the computer. The solution basically is to taper the edges of the inside of the tape. Thus as the tape is wound, the resulting stresses that caused the tape previously to dish on its outside are compensated for and the tape becomes flat across its width.

The general formulas for determining how, where, and to what extent the tape should be tapered in any specific case are contained in the trio's paper entitled "Moire Study of Anticlastic Deformation of Tapes with Tapered Edges." Conway and the two IBM engineers presented the paper at the annual meeting of the Society for Experimental Stress Analysis in Pittsburgh, Pa.

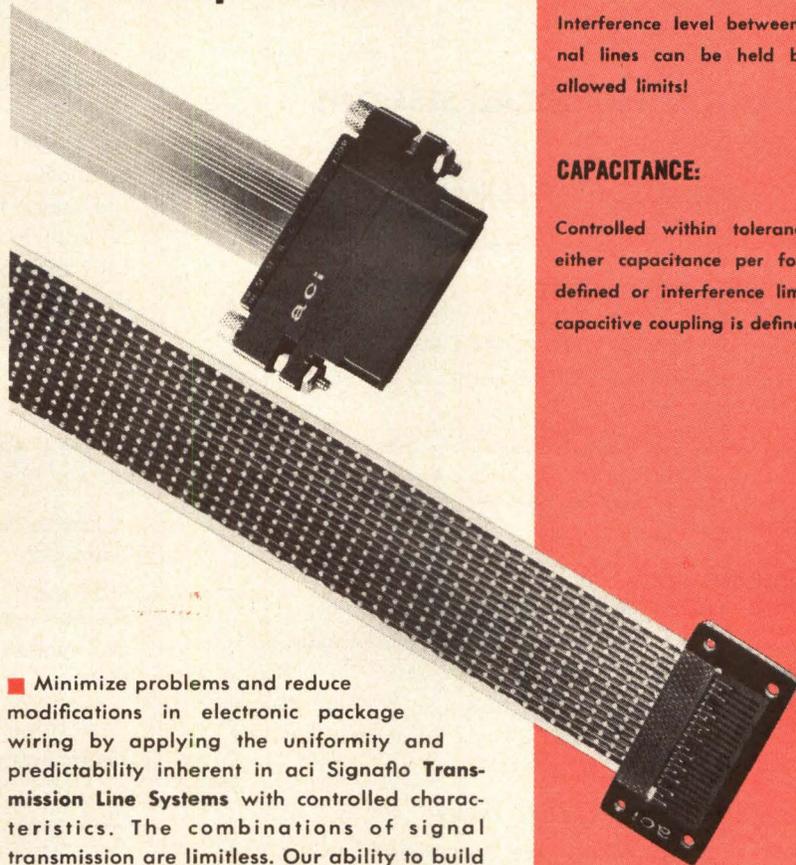
DATA MACHINES, INC. OF NEWPORT BEACH, CAL. ANNOUNCED THE RECENT SHIPMENT OF A COMPUTER SYSTEM WHICH IS TO BECOME A LINK IN THE BILLION DOLLAR AQUEDUCT CONTROL SYSTEM that will supply water to Southern California. The control system will consist of a central computer at Sacramento, and a number of remote computers at control sites along the aqueduct. Each remote computer will send (through a telephone link) status information to Sacramento telling of water level, flow rate, flood gate positions, and other pertinent data. The central computer will act on this information automatically and send back commands which will control the valve gates. Data Machines' computer the Data/620 will be installed at a South Bay site in Southern California.

EQUITABLE TIME DISTRIBUTION AMONG MAJOR USERS OF A SINGLE COMPUTER HAS BEEN SIMPLIFIED BY THE USE OF A TIME-SHARING MONITORING DEVICE at the Westinghouse Computer Center in East Pittsburgh. The unique monitoring unit consists of three electric clock timers, similar to the type used to control appliances. Manual setting of a three-position switch by the computer operator indicates work is being performed for user "A", "B", or "C". The switch setting triggers the relays to power the corresponding clock in the main unit. Each clock can be set to flash a warning light when a predetermined maximum time limit has been reached. Resetting the clocks to a dial indication of 12 at the start of each day provides a way for direct reading of accumulation of user hours during the day shift. The device was constructed from components totaling less than \$50.

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- Cross-talk
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# 1967 INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

Univ. of Penn. — Sheraton Hotel, Philadelphia, Pa.  
Feb. 15-16-17, 1967

## MAJOR TECHNICAL SESSIONS

WEDNESDAY, FEBRUARY 15

SESSION 1 ..... 9-11:45 A.M.

### LINEAR INTEGRATED CIRCUITS

#### INSULATED GATE FET LINEAR INTEGRATED CIRCUITS

P. M. Thompson, University of Ottawa and G. H. Hantusch, Northern Electric Co., Ottawa, Canada.

This paper will survey circuit techniques applicable to MOS and related devices in linear integrated circuits. Methods of controlling and stabilizing the dc operating point and sheet resistance will be discussed.

#### A HIGH-PERFORMANCE 3-WATT MONOLITHIC CLASS-B POWER AMPLIFIER

T. M. Frederiksen and J. E. Solomon, Motorola Semiconductor Products, Phoenix, Ariz.

An integrated class-B power amplifier which delivers 3 W to a direct-coupled load with a total harmonic distortion of less than 0.2% has been fabricated using all npn technology.

#### D/A and A/D INTEGRATED CIRCUITS FAMILY

M. B. Rudin, R. O'Day, and R. Jenkins, Fairchild Semiconductor, Palo Alto, Cal.

Low-cost digital data-processing analog interface equipment implies low-cost D/A and A/D converters. System/circuit/device studies in defining and developing a compatible set of linear IC's for D/A's and A/D's will be reported.

#### IC's for PROFESSIONAL COMMUNICATIONS SYSTEMS

M. J. Gay, D. Moore, and J. Skingley, Allen Clark Res. Centre/The Plessey Company Ltd., Northants, England.

A compatible family of silicon integrated circuits has been developed for use in radio communication systems.

#### A MONOLITHIC INTEGRATED VARIABLE ATTENUATOR

J. A. Mataya and S. B. Marshall, Sprague Electric Co., North Adams, Mass. and A. A. Gaash, Israeli Ministry of Defense, Jerusalem, Israel.

This paper will describe a monolithic integrated variable attenuator which performs the functions of AGC, chopper, and modulator.

As in the recent past Solid-State Circuits Conferences, integrated circuit technology will be the major topic in the 1967 sessions. A total of 58 contributed and invited papers make up the formal program. In addition, 13 evening discussion panels are scheduled. The state-of-the-art in large-scale integration will highlight many sessions and panel discussions.

All daytime sessions will be held at the University. All evening panel discussions will be held at the Sheraton Hotel.

Pre-conference registration fees are \$13.00 for members, \$15.00 for non-members; at conference, fees are \$15.00 for members and \$18.00 for non-members. **Pre-meeting registration forms are available from Lewis Winner, 152 W. 42 St., N. Y., N. Y. 10036.**

A brief summary of some of the scheduled papers and panel discussions is presented here.

SESSION 2 ..... 2:50-5:30 P.M.

### LARGE-SCALE INTEGRATION — PRESENT AND FUTURE

#### LSI — THE FABRICATOR'S VIEWPOINT

R. D. Lohman, R. C. A., Somerville, N. J.

This paper will discuss the problems which LSI poses to the device manufacturer as well as some possible solutions to these problems.

#### LSI — DIGITAL ELECTRONICS

T. R. Finch, Bell Telephone Laboratories, Murray Hill, N. J.

Gains in bits per-second/per-dollar are expected through LSI. Device technology is here; system exploitation is ahead. LSI in high-speed memory electronics will be reported.

## LSI — IMPACT ON DIGITAL SYSTEMS

R. Rice, Fairchild Semiconductor, Palo Alto, Cal.

Large arrays will not pay off as merely replacements for integrated circuits. This paper will discuss a philosophy for integrating software and hardware to reduce total costs.

### PANEL DISCUSSION ..... 8:00 P.M.

#### LOGIC PARTITIONING IN LSI

The status and problems of logic partitioning will be discussed from the standpoint of natural partitions existing in traditional computer systems, gross system redesign for improved partitions, algorithms for computer-aided partitioning, and test sequence simplification.

### PANEL DISCUSSION ..... 8:00 P.M.

#### SOLID-STATE IMAGE SENSORS AND DISPLAYS

A variety of solid-state techniques currently being studied for image sensing and display will be presented. The problems of integrated fabrication and of appropriate addressing and driving circuitry will be discussed.

### PANEL DISCUSSION ..... 8:00 P.M.

#### LSI PROBLEMS AND PAYOFF IN PERIPHERAL EQUIPMENT FOR TIMESHARING

The potential for more electronics and LSI in the huge timesharing peripheral equipment market is poorly defined. This panel will appraise four key areas: distribution of electronics in timesharing computing systems; size of the peripheral equipment timesharing market; potential for LSI in peripheral electronics; and applying LSI processing to peripheral electronics.

## THURSDAY, FEBRUARY 16

### SESSION 5 ..... 9 A.M.-12 NOON

#### LARGE-SCALE INTEGRATION

##### LARGE-SCALE INTEGRATION: APPLICATION CONSIDERATIONS

W. H. Puterbaugh, National Cash Register Co., Dayton, O.

LSI raises questions concerning the interface between the user and supplier that presently burdens the cost in packaging and testing. A different interface which provides optimum cost and flexibility from the systems viewpoint will be discussed.

##### COMPUTER-AIDED DESIGN for LARGE-SCALE INTEGRATION

C. H. Mays, Fairchild Semiconductor, Palo Alto, Cal.

The large number of unique LSI designs forecast for the 70's requires both design and manufacturing process automation. This paper will discuss computer-aided design of LSI and the impact of such aids on the customer-vendor interface.

##### ACTIVE MEMORY DESIGNS USING DISCRETIONARY WIRING for LSI

R. Dunn and J. Jeansonne, Texas Instrument, Inc., Dallas, Tex.

Active main memory design criteria will be presented. The memory is formed from interconnecting the good circuits on a slice containing 3900 cells. Interconnection requires a second level lead pattern routed by a computer.

#### PARTITIONING for LARGE-SCALE INTEGRATION

H. R. Beelitz and H. S. Miiller, RCA Laboratories, Princeton, N. J. and R. J. Linhardt and R. D. Sidnam, RCA, Camden, N. J.

Functional partitioning and a distributed control approach to computer design yields a dramatic solution to the partitioning problem. Now arrays can have 60% to 80% fewer connections than were required by conventional designs.

#### COMPLEMENTARY-MOS INTEGRATED BINARY COUNTER

H. Borken, A. K. Rapp, L. P. Wennik, and K. R. Keller, RCA, Somerville, N. J.

A twelve-stage binary counter, capable of arbitrarily-low counting rates, was fabricated as a monolithic array of P- and N-channel MOS transistors. A circuit design based on complementary transmission gates produced efficient component utilization.

### SESSION 7 ..... 1:30-5:00 P.M.

#### COMPUTER-AIDED CIRCUIT DESIGN

##### SCOPE and AVAILABILITY of PROGRAMS for COMPUTER-AIDED CIRCUIT DESIGN

W. W. Happ, ERC/NASA, Cambridge, Mass.

Hundreds of computer-aided programs are now available. The scope, input-output format, compatibility, and availability idiosyncrasies of the programs will be examined from the user's point of view. The need for standardization will be discussed.

##### PS SILICON MONOLITHIC CURRENT-SWITCHING CIRCUIT USING PN JUNCTION ISOLATION and DIFFUSED RESISTORS

B. P. F. Wu, V. A. Dhaka, and C. Y. Chen, IBM Corp., East Fishkill, New York.

The delay of a digital silicon monolithic circuit can be calculated. Current-switching circuits using pn junction isolation, diffused resistors, and multilayer interconnections have been fabricated. The measured delay which ranged from 320 to 540 ps agreed closely with design values.

##### A DIRECT-VIEW CRT CONSOLE for REMOTE COMPUTING

H. S. McDonald, W. H. Ninke, and D. R. Weller, Bell Telephone Laboratories, Murray Hill, N. J.

A low-cost computer console capable of presenting a wide range of graphical displays will be described. The concurrent cost-performance features are achieved by combining a simple terminal and buffer with computer software line and letter generation.

##### A DISTRIBUTED MODEL of the SATURATION CHARACTERISTICS of INTEGRATED TRANSISTORS

L. B. Dickson, Motorola Semiconductor Products, Phoenix, Ariz.

A distributed model for the saturation characteristics and internal currents of an integrated circuit transistor will be described. The model can be used to predict accurately the saturation voltage of an integrated circuit transistor.

##### AN APPLICATION EXPERIMENT with ON-LINE GRAPHICS-AIDED ECAP

G. R. Hogsett and D. A. Nisewanger, IBM Corp., L. A., Cal. and A. C. O'Hara, Jr., IBM Corp., Kingston, N. Y.

An experimental version of the Electronic Circuit Analysis Program (ECAP) with a graphic man-machine interface for circuit input and analysis output has been used successfully by circuit designers. This paper will summarize experience in a design environment and consider future implications.

## Solid-State Circuits Conf. (Cont'd.)

SESSION 8 ..... 1:30-5:00 P.M.

### MEMORY TECHNIQUES

#### NEW IMPLEMENTATION of BIPOLAR SEMICONDUCTOR MEMORY

D. J. D'Stefan, J. E. Iwersen, and J. H. Wuorinen, Bell Telephone Laboratories, Murray Hill, N. J.

A 100-ns nondestructively-read memory with 16 bipolar flip-flops has been integrated on a 30 x 38-mil beam-leaded chip. Arrays of 64 words (16 bits-per-word) have been produced by bonding chips on large-area substrates.

#### SILICON on SAPPHIRE COMPLEMENTARY MOS MEMORY SYSTEMS

J. F. Allison, J. R. Burns, and F. P. Heiman, RCA Laboratories, Princeton, N. J.

A 10-transistor one-bit memory cell exhibiting a pair-delay of less than 12 ns with a standby power dissipation of 10 microwatts has been fabricated. The cells have integrated into a 9-bit word on an 80-mil square chip.

#### A HIGH-SPEED ASSOCIATIVE MEMORY

A. W. Bidwell, IBM Corp., Poughkeepsie, N. Y. and W. D. Pricer, IBM Corp., East Fishkill, N. Y.

This paper will describe a simple associative memory cell as used in a high-speed 8-word experimental model with 15-ns interrogate delay and in an experimental timesharing system of 64 words.

#### A NEW MAGNETIC READ-ONLY MEMORY

E. B. Barcaro, D. T. Best, and J. S. Zajackowski, Univac Div./Sperry Rand Corp., Blue Bell, Pa.

A read-only memory technique using plated-wire transducers and a sheet of magnetic recording material has been developed. The memory does not require relative mechanical motion between the transducer and the sheet.

#### NOVEL LOW-COST DESIGN for 2-1/2D STORAGE SYSTEMS

P. A. Harding and M. W. Rolund, Bell Telephone Laboratories, Naperville, Ill.

Two difficult problems associated with 2 1/2D memories will be considered: economical bit access design and minimization of bit current noise. A multi-state core analysis determines optimum current values and indicates desirable circuit configurations.

PANEL DISCUSSION ..... 8:00 P.M.

### COMPUTER-AIDED DESIGN

This discussion will consider computer aids to successful modeling, analysis, and design of integrated devices, circuits, and subsystems.

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### CD REFRESHER SERIES:

#### Mathematics Revisited

continues in the February issue with

#### PART 8 — Descriptive Statistics

(Part 7 appeared in last month's issue.)

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PANEL DISCUSSION ..... 8:00 P.M.

### THE NEXT STEP IN LARGE-SCALE MEMORY

Requirements for main-frame memory in future digital machines will be discussed. Effects of present system-circuit-device interactions on the next generation memory systems will be assayed.

PANEL DISCUSSION ..... 8:00 P.M.

### HIGH-SPEED CIRCUITS

The discussion will emphasize the fundamental relationships and limiting factors of various approaches to subnanosecond speeds. Delay measurement techniques and tradeoffs between germanium and silicon, smaller devices and higher integration, density and power dissipation will be considered.

## FRIDAY, FEBRUARY 17

SESSION 11 ..... 1:30-4:30 P.M.

### DIGITAL CIRCUIT TECHNIQUES

#### AN INTEGRATED CURRENT MODE FULL ADDER

U. Priel and J. W. Hively, Motorola Semiconductor Products, Phoenix, Arizona.

A transistor tree has been utilized in the design of a current mode high-speed full adder. Following a discussion of design philosophy, the adder will be thoroughly analyzed and compared with state-of-the-art implementations.

#### PICOSECOND PULSE RESPONSE of INTERCONNECTIONS in a COMMON SUBSTRATE MONOLITHIC SYSTEM

P. A. Brennan, IBM Corp., Yorktown Heights, N. Y. and H. Guckel, Washington University, St. Louis, Mo.

Interconnections in a common substrate monolithic system are essentially microstrip transmission lines loaded by a two-material medium. These structures have been found to exhibit pulse delays equivalent to a relative dielectric constant of 2500.

#### SILICON VS. GERMANIUM in PICOSECOND LOGIC CIRCUITS

F. H. Dill, A. S. Farber, and H. N. Yu, IBM Corp., Yorktown Heights, New York.

A theoretical and experimental comparison of basic materials, properties, and actual performance in planar picosecond logic circuits shows considerable advantage for germanium over silicon transistors in this speed range.

#### AN INTEGRATED THRESHOLD GATE

J. J. Amodei and R. O. Winder, RCA Laboratories, Princeton, N. J. and D. Hampel and T. R. Mayhew, RCA, New York, N. Y.

A threshold gate has been integrated which is fully compatible with standard current mode OR/NOR gates. Based on some examples, the cost reduction of typical logic systems using these gates is estimated at 50%.

#### VHF SAMPLE & HOLD

R. E. Fisher, Bell Telephone Laboratories, Murray Hill, N. J.

A very-high frequency Sample and Hold (S&H) circuit operating at a 120-MHz sampling rate will be described. When driving a companion analog-digital converter, the circuit makes possible a 720 mbit/s, 6-bit Gray code PCM system.

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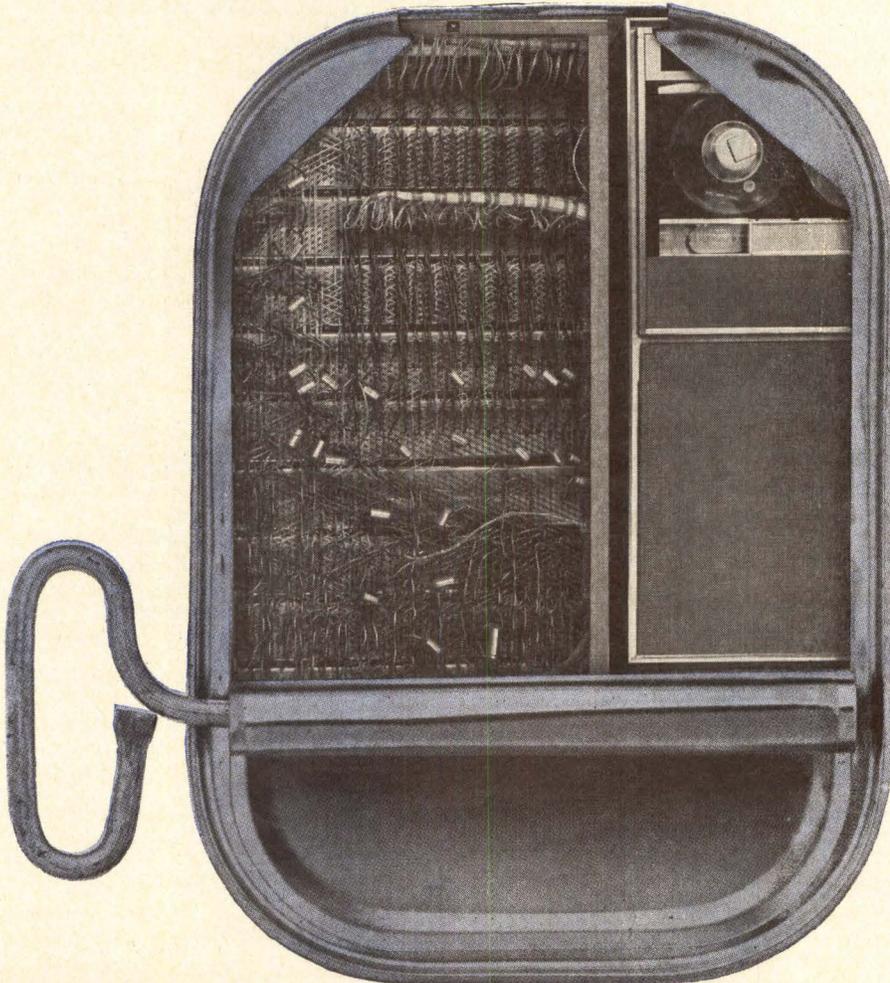
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CIRCLE NO. 24 ON INQUIRY CARD

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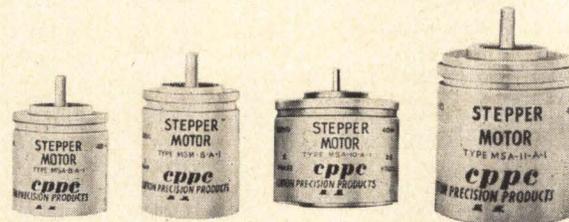
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INERTIA (GM-CM <sup>2</sup> )	0.19	0.19	0.77	0.37	0.18	0.45	0.19	0.77	0.10	2.4
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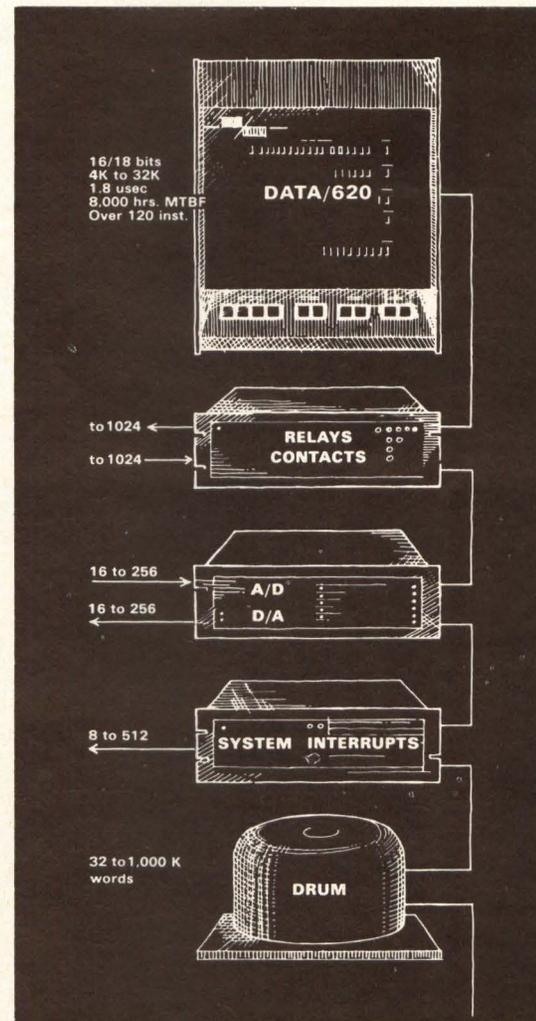
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CIRCLE NO. 29 ON INQUIRY CARD

# INTEGRATED LOGIC CIRCUITS: A Comparative Evaluation

DR. WILLIAM B. HUGLE, Contributing Editor

It has been estimated that approximately 95 per cent of all digital circuit functions can now be accomplished by integrated circuitry — with a list of advantages over discrete circuitry which far outweigh the list of disadvantages. It has become an accepted fact that the IC package offers an economic attraction for digital functions, a probable advantage in terms of performance, and an undisputed advantage in terms of size. Mingle with designers of digital equipment at any trade show, or in the privacy of their own laboratories, and you will soon conclude that no such designer today approaches a new project without giving serious consideration to integrated circuits.

The problem has thus become less a question of whether to use ICs than a question of which ICs to use. Unfortunately, it has been a difficult question for many design engineers to answer for themselves. It is the nature of business that marketing

men from one firm will try to sell the engineer on the advantages of its approach and its logic package. In some cases, this has left a few scars with the engineer who was led down the garden path to a digital logic form completely wrong for his application, the result being that he is now reluctant to try again.

The time has come, then, for a comprehensive look at the logic forms available to the designer so that he might choose wisely the type to suit his own purposes. Certainly no one logic form is superior to all others for all applications. For each application, the user must select the form which meets his total system requirements, with the decision based upon such factors as power consumption, operating environment, and cost.

The basic trade-offs for each logic line must be taken into account. If the system requires extreme speed or low power dissipation, the designer

must determine which logic lines supply these needs and then compare what he must give up with each one in terms of logic swing, power consumption, and noise immunity.

## Resistor-Transistor Logic

Resistor-Transistor Logic (RTL), also identified frequently as Direct-Coupled-Transistor Logic (DCTL), was the pioneer form of integrated circuit logic and is the most direct translation of discrete design into integrated form. Although they are the same basic logic form, RTL and DCTL do differ somewhat, in that the RTL is modified to include a resistor in the base lead. With direct-coupled circuits, a problem arises when several base-emitter junctions are driven from the same output. The input with the lowest base-emitter junction forward potential can limit the drive current to the

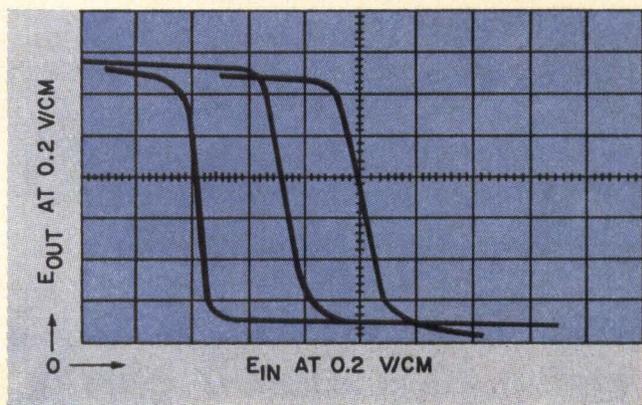


Fig. 1 Transfer characteristic of typical RTL gate circuit.

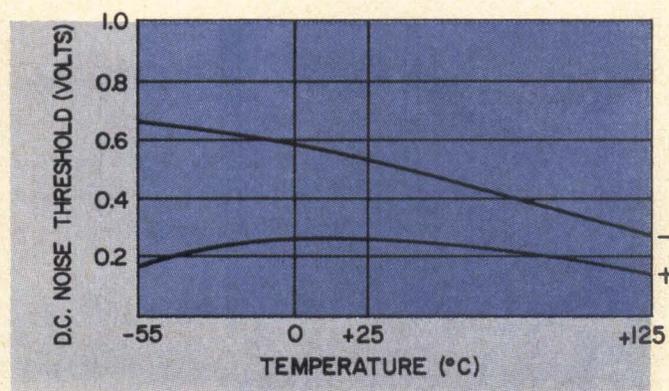


Fig. 2 Typical input dc noise threshold vs. temperature for RTL circuit.

**No one integrated logic circuit form is superior to all others for all applications. For each application, the system designer should analyze the basic trade-offs of each logic line. To help in this type of analysis, a comparative evaluation of available IC logic circuits is given here.**

other transistor bases. A resistor added to the base circuit increases the input impedance to assure proper operation when more than one load is being driven.

The basic RTL circuitry, which is available from all the major integrated circuit suppliers, has the advantages of being useful for a wide range of digital applications and being highly reliable. It also is easy for design engineers to adapt this type of IC logic for their use since its design parallels that of discrete circuitry. Even with these advantages, however, the potential user should carefully study the performance characteristics of RTL.

The number of load circuits that can be driven by an output is limited to five in a basic RTL gate. Larger fan-out drivers are available, capable of driving up to 25 gate circuits, but fan-out is still limited because logic swing and noise immunity are both dependent upon it.

Another limitation is that RTL's noise immunity degrades rapidly with an increase in temperature. The transfer characteristic of a typical RTL gate circuit (Fig. 1) indicates that the logic swing is about 1.2 to 1.3 V, operating at 3 V with a fan-out of three. The voltage level required to switch an RTL circuit shifts considerably with variations in the operating temperature and fan-out.

A similar transfer characteristic for the DCTL circuit (without the base resistor) would show a reduced logic swing in the order of 0.6 to 0.7 V. The high level operating point

would lie closer to the active region of the transfer curve, resulting in a reduced noise margin and relatively poor dc stability.

Typical input dc noise threshold vs. temperature for the RTL circuit is illustrated in Fig. 2. The top curve in Fig. 2 indicates the amount of noise immunity that a circuit has when the input is in the high logic

state (or the logic 1 condition) and a negative noise pulse is injected on the input signal line. The lower curve describes the noise immunity values during the input logic 0 condition when a positive signal pulse is injected on the input.

In a plot of a typical input ac noise threshold vs. pulse width (Fig. 3), it is shown that at an input pulse width

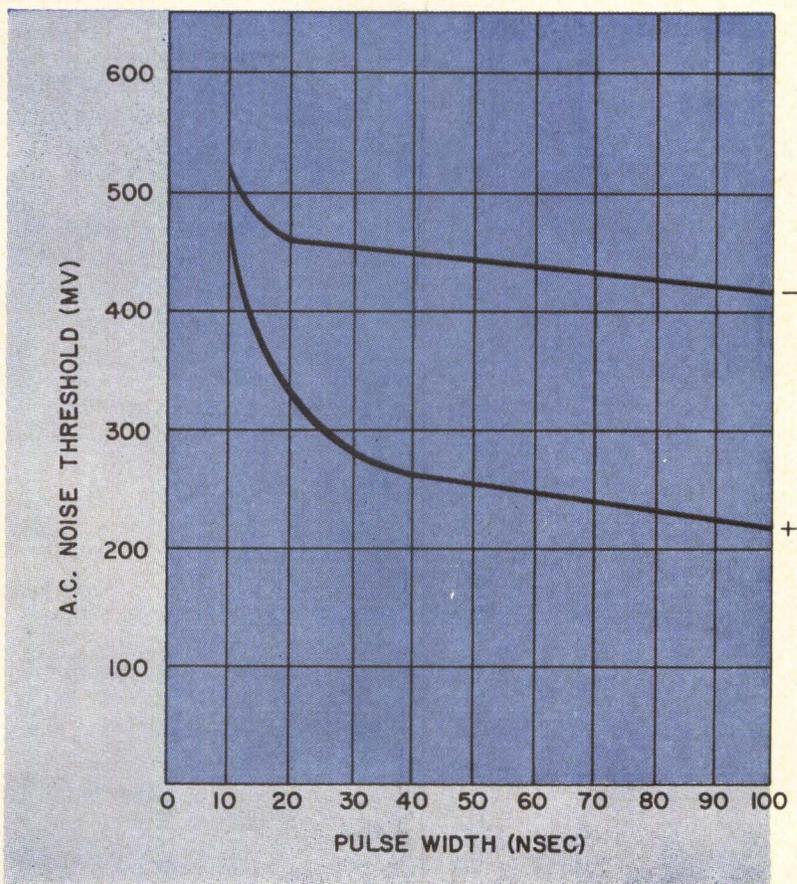


Fig. 3 Typical input ac noise threshold vs. pulse width for RTL circuit at 25°C.

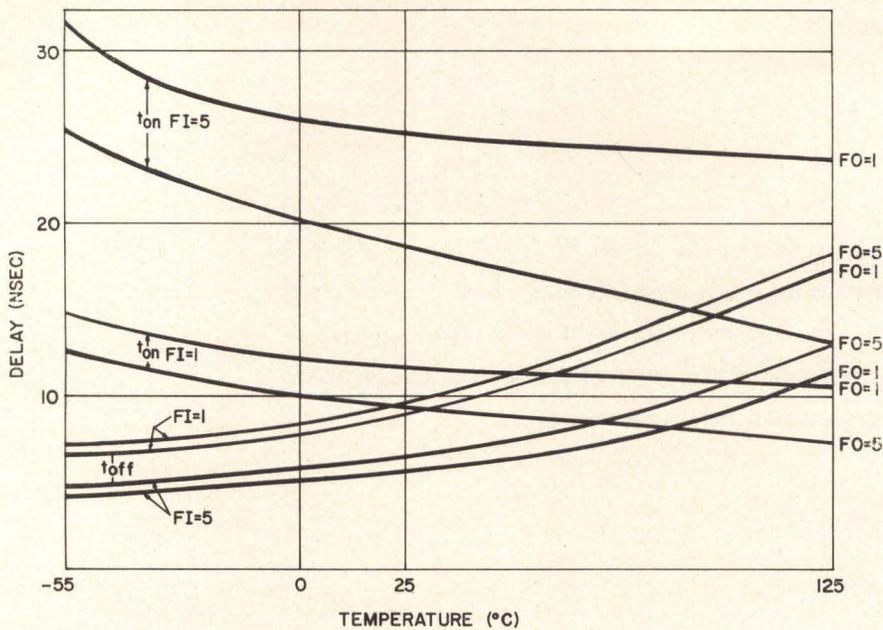


Fig. 4 RTL turn-on and turn-off delay times vs. temperature and fan-out.

of roughly 50 to 100 ns, the noise immunity levels off and approaches the dc condition. At smaller pulse widths, noise margins on the input signal line are appreciable. For example, with pulse widths on the order of 10 to 20 ns, the noise margin will be greater than 0.5 V.

The turn-on and turn-off delay times of RTL are also affected by temperature and fan-out variations, as shown in Fig. 4. At any given temperature, an increase in fan-out results in a slower turn-off time but a faster turn-on time. As variations in fan-out put more or less load on the circuit, there is a corresponding increase or decrease in the time required to turn off the output inverter.

For RTL applications that require low power dissipation, a line has been developed known as milliwatt-RTL. In this modified version, the base resistors and the collector load resistor are increased significantly to reduce the power dissipated in a typical gate circuit to about 2 mW. Consequently, if power dissipation is a main consideration, milliwatt-RTL offers an advantage. The basic milliwatt-RTL circuit is shown in Fig. 5.

#### Diode-Transistor Logic

Diode-Transistor Logic (DTL) is also familiar to the designer of discrete circuitry. The diodes provide

additional threshold in the circuit and increase the input impedance over the RTL circuit. Therefore, DTL became the second integrated logic type on the market.

The advantages of DTL circuits over RTL include larger logic swings and improved noise immunities, with input signal line noise margin running typically in excess of 1 volt. The basic DTL circuit, shown in Fig. 6, requires two power supplies: a positive supply, and a negative supply used to improve the turn-off time of the output inverter. Although the circuit would operate with only one supply, an undesirable compromise in the design would be necessitated to provide fairly symmetrical turn-on and turn-off times. If a single power supply were used, the charge could be pulled out of the base of the inverter when the input goes to a low logic state, allowing the inverter to turn-off, by either putting a small resistor between base and emitter or by making diodes  $D_1$  and  $D_2$  special slow recovery diodes. In the basic DTL circuit, a negative power supply is used to turn-off the output inverter, even though this added supply is somewhat of a disadvantage in itself.

The need for a dual power supply is one of the undesirable features that has been corrected in some DTL circuits, such as the basic 930 Series DTL. This series, originated by Fair-

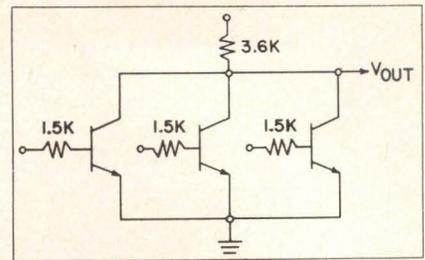


Fig. 5 Milliwatt-RTL gate circuit.

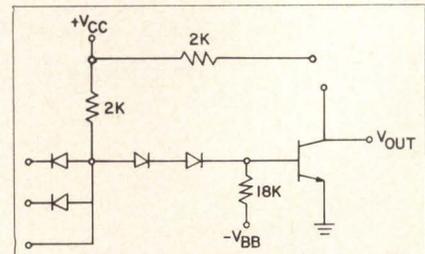


Fig. 6 Basic DTL gate circuit.

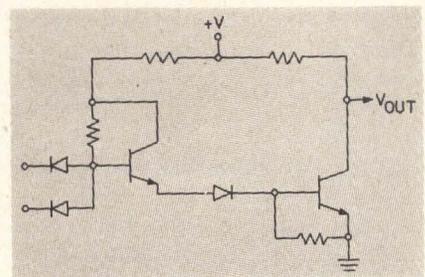


Fig. 7 Basic gate circuit of the 930 DTL series.

child Semiconductor and also offered by a number of other companies, dominates the DTL market at present.

The basic gate circuit of the 930 DTL series is shown in Fig. 7. The circuit features an input transistor that replaces one of the input offset diodes in conventional DTL. The transistor supplies the turn-on drive to the output inverter, allowing for potential increase in loading with the DTL design. The input current source in the gate allows for a much smaller base resistance, and so a negative supply is not required for rapid transistor turn-off.

A close evaluation of the design requirements for the 930 Series DTL circuit indicates that less demand is made on resistor tolerances,  $h_{FE}$ , fan-out, and power dissipation than in the conventional DTL circuit. Therefore, although the performance characteristics of DTL and 930 DTL circuits are similar, the latter offers a number of advantages. These include, in addition to the single power

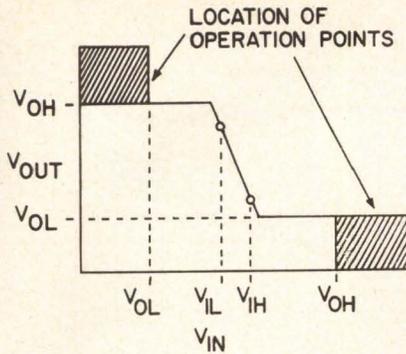


Fig. 8 Transfer characteristic of typical 930 Series DTL gate.

supply operation, lower power dissipation, larger drive capability, higher speed operation, and better noise immunity.

The transfer characteristic of the typical 930 Series DTL gate is given in Fig. 8.  $V_{IL}$  is the minimum low threshold on the input, while  $V_{IH}$  is the maximum high threshold on the input. The worst-case specified noise margins with a low level input and high level input are  $V_{IL}$  and  $V_{IH}$ , respectively. The low level noise margin will always be in excess of 350 mV while the high level noise margin will be greater than 400 mV over the full temperature range of  $-55^{\circ}$  to  $125^{\circ}\text{C}$ . Increased noise margins are obtained when circuits are not fully loaded. Worst-case noise thresholds generally are better than 600 mV in systems that do not employ the maximum drive capability of each circuit.

Some applications will require better noise immunity than that available from most logic types discussed above. Amelco Semiconductor's DTL line is noted particularly for its high noise margin, and has been found by many designers to work best in high noise DTL applications.

For IC applications which require exposure to high radiation levels, it should be noted that most standard logic lines made by conventional techniques have been generally limited in operation. The types of devices which have proved most successful are those which use dielectric isolation of active elements combined with monolithic silicon chip fabrication using passivated epitaxial techniques.

Radiation, Inc. pioneered the use of dielectric isolation in digital applications and Norden explored its early use in the linear field. The technique

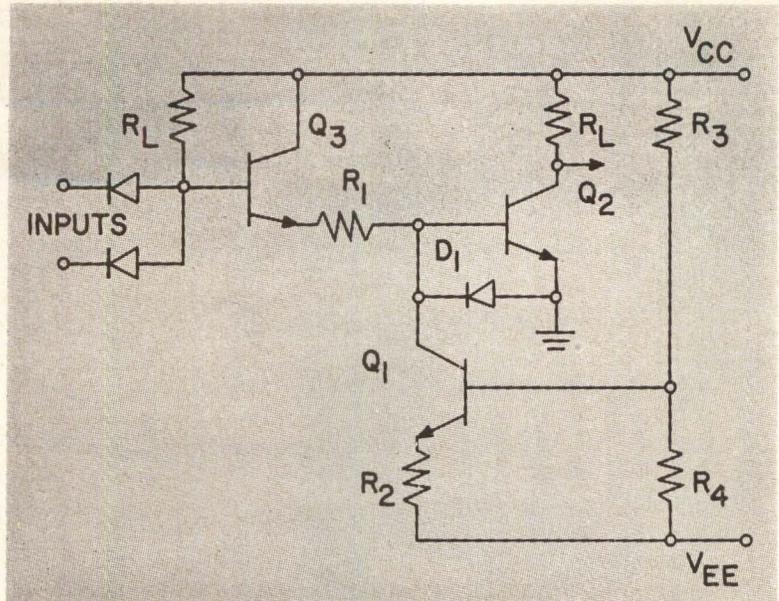


Fig. 9 Basic VTL gate circuit.

is also used by Motorola in what they call their Epic process.

These manufacturers believe that dielectric isolation provides parasitic-free operation with electrical performance surpassing that of conventionally constructed ICs. For its DTL gates, for example, Radiation, Inc. specifies propagation delay of 7 ns, power dissipation of 10 mW, noise immunity of  $>800$  mV, and fan-out of 8.

### Variable Threshold Logic

In an effort to improve noise margins, Motorola Semiconductor Products further modified the basic DTL circuit and came up with a logic type known as Variable Threshold Logic (VTL).

Although VTL is not primarily designed for use in "computer" logic, it has applications in certain computer peripheral equipment, such as when integrated circuits must operate to close solenoids, relays, and high-voltage testing devices that create noise spikes far in excess of the noise immunity levels of conventional logic gates.

It must be kept in mind that VTL has two primary disadvantages, however, in that it has a poor power-speed ratio and it requires two power supplies. On the plus side, it can remove the need for bulky packaging and shielding which has not always been effective in high-noise applications.

The basic VTL gate circuit is shown in Fig. 9. This circuit differs

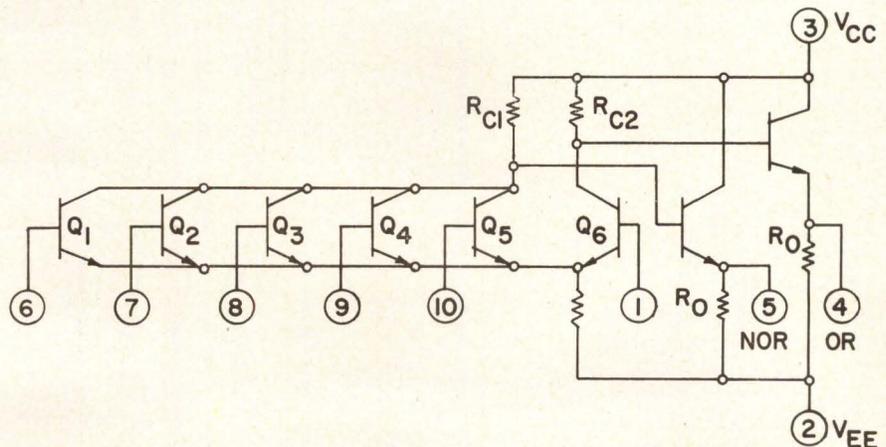
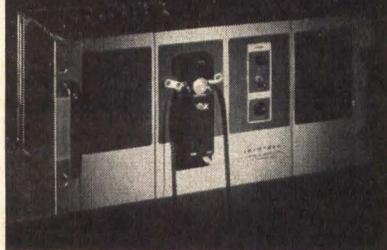


Fig. 10 Basic ECL gate circuit.

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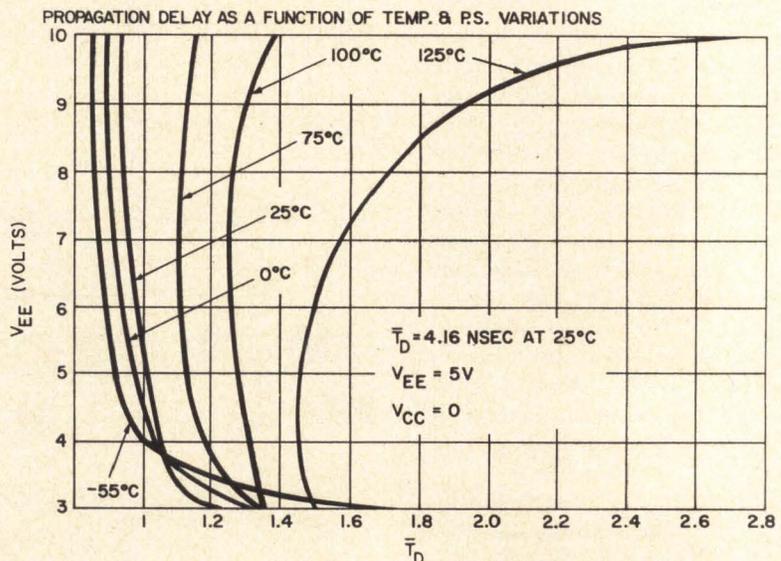
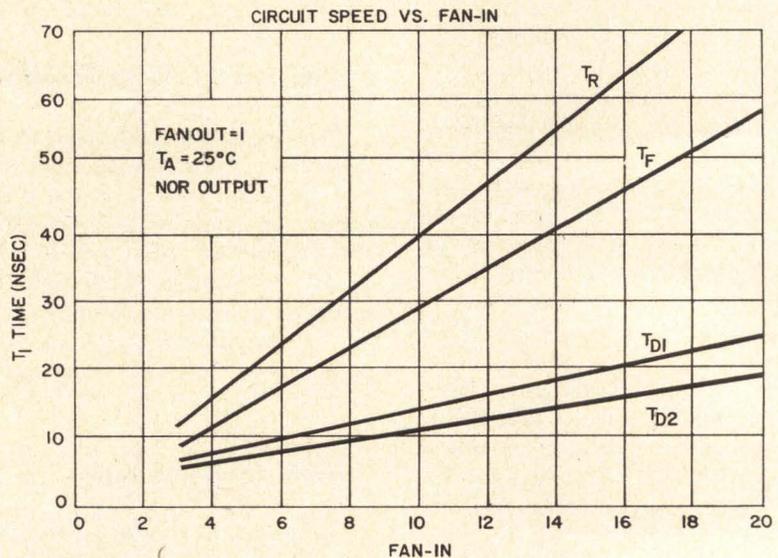
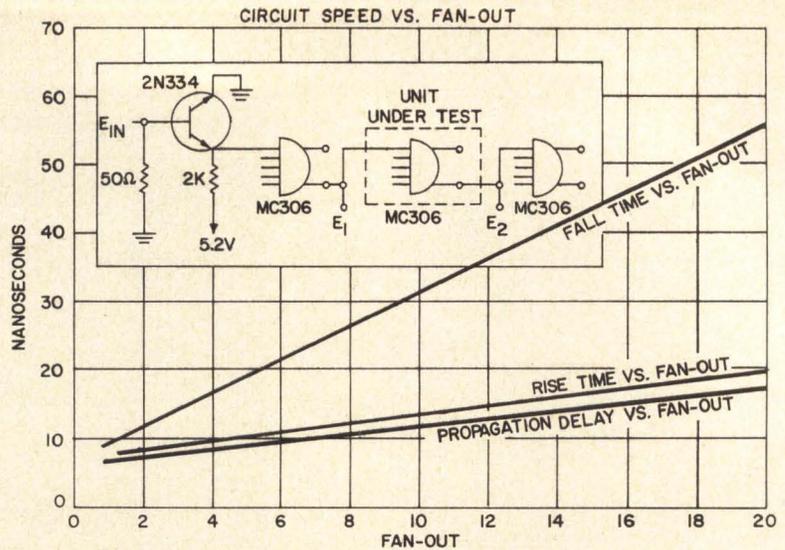


Fig. 11 Performance characteristics of ECL circuitry.

from the conventional DTL gate in that one of the input offset diodes has been replaced by a voltage dropping resistor. Also, a current source transistor,  $Q_1$ , is used, whereas in DTL there is a pull-down resistor in the base of the output inverter. The designer with these special needs will find that these changes provide additional noise immunity.

Ground noise rejection capability is an important feature of the VTL logic family. While not as high as input noise margins, the ground noise margin is considerable and offers some advantage over what is presently available in other integrated logic lines.

At 10 V operation, the Motorola VTL circuits exhibit a typical dc ground line noise immunity of 3.7 V, and additional ground noise immunity can be picked up by adjusting the  $V_{EE}$  bias below the value of  $V_{CC}$ .

The power consumed by a single VTL gate circuit will vary from 82 mW with 10 V supplies to 12 mW with 4 V supplies. Typical propagation delay of the VTL gate will vary from 60 ns with 4 V supplies to 48 ns with 10 V supplies at 25°C. Thus, the speed, power dissipation, and noise immunity of VTL circuits are quite flexible. However, a maximum fan-out of five is specified with VTL, and use of a larger number of load circuits than five will give some loss in noise margin.

### Emitter-Coupled Logic

Another logic type introduced by Motorola was the ECL family of circuitry. This resulted from a development program aimed at disregarding approaches used in discrete circuitry upon which the earlier types of circuits had been based. The result is called current-mode logic and it features propagation delays as low as 1 to 2 ns, high fan-in and fan-out, and high noise immunity with a minimum of crosstalk.

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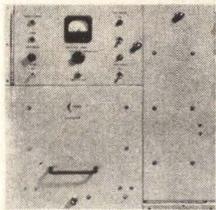
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sistor ratios, not absolute values. The ECL line of circuits provides essentially all the necessary circuitry required for the arithmetic and control portions of a computer.

The basic ECL logic circuit, a 5-input gate, is shown in Fig. 10. It consists principally of an NPN current-mode followed by emitter followers serving as output stages. The current switch is composed of five input transistors having common collectors ( $Q_1 - Q_5$ ) and a fixed bias transistor ( $Q_6$ ). The fixed bias driver insures that the threshold point is always in the center of the transition region and is designed to track with temperature in order to compensate for threshold changes with temperature. Bias furnished to the gate will always lie midway between a logical 0 and a logical 1. Thus, almost perfect tracking is obtained from  $-55^\circ$  to  $125^\circ\text{C}$  with power supply variations to  $\pm 20\%$ .

The typical ECL circuit is designed with a differential amplifier input and emitter-follower output to restore dc levels and provide a large output drive capability. In circuit operation with a negative supply, a fixed bias is applied to one side of the differential amplifier and the logic signals are applied to the other inputs resulting in the following two different "states" of the circuit:

1. With a logical 0 input applied, the current through  $R_E$  is supplied by the fixed biased transistor. A drop of 800 mV occurs across  $R_{C2}$ . The OR output is  $-1.55$  V, or one  $V_{BE}$  drop below 800 mV. Since no current flows in the input transistor, the NOR output is a  $V_{BE}$  drop below ground, or  $-0.75$  V.
2. When a logical 1 level is applied to the input, the current through  $R_E$  is switched to the input transistor, and a drop of 800 mV occurs across  $R_{C1}$ . The OR output becomes  $-0.75$  V and the NOR is  $-1.55$  V.

The high speed of ECL circuitry results from a number of design features. First, since most of the logical decisions are performed at the low-impedance level of the common-emitter node, and since the output impedance of the gate is low, deteriorating effects of parasitics are minimized. Secondly, the signal paths are essentially through emitter-followers and grounded-base stages which are inherently fast. Finally, since the gates are designed to prevent the

transistors from saturating, storage time delay is completely eliminated.

ECL circuitry offers a relatively large number of fan-ins as well as fan-outs without seriously degrading circuit performance. This is largely due to the high input impedance and low output impedance of the circuits. Fig. 11 depicts how the propagation delay varies as a function of temperature and power supply. It will be noted that the propagation delay is practically independent of the power supply over a wide range of voltages and that it increases only about 100 per cent as the temperature is varied from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

The transfer characteristics for both the OR and the NOR outputs of the ECL gate are shown in Fig. 12. The transition region is about 100 mV wide, the logic swing is 800 mV, and the noise immunity of the circuit is 50 per cent which means that the circuit can tolerate noise signals of almost 400 mV at any of the input terminals.

In ECL circuitry, noise generated internally in ground and power supply lines is practically non-existent because the current demand of the circuits is constant, being independent of the on or off state of the gate. On the other hand, ECL circuits are susceptible to noise generated externally because of their limited logic swing. Therefore, it is generally necessary to shield the circuits themselves to keep out as much external noise as possible.

Since logical operations in ECL circuits are performed at the collector nodes, disturbances that appear on the ground line are critical in establishing logic levels and system stability. Worst-case noise margins for ground line disturbances as they vary with changes in supply voltage and fan-out at  $25^\circ\text{C}$  are shown in Fig. 13. The manner in which input signal line noise pulse thresholds vary with noise pulse width and temperature is shown in Fig. 14. The ac noise margins with noise pulses less than about 35 ns generally are in excess of 250 mV. Smaller pulse widths that would not affect a DTL or RTL circuit do affect the non-saturated logic circuit because of its higher speed.

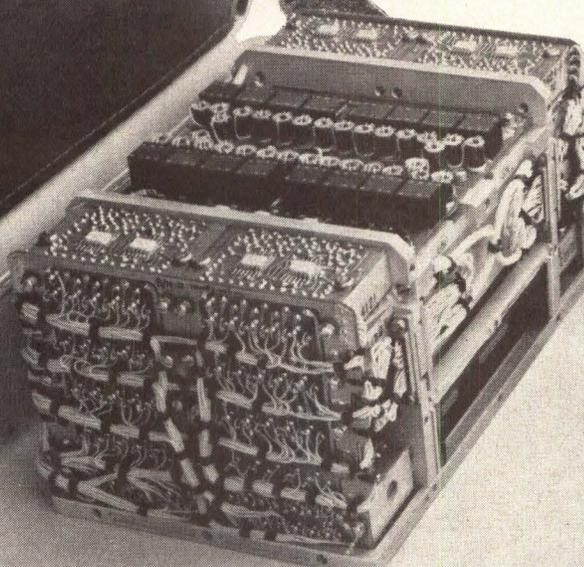
In addition to ECL circuitry's other attractions, the fact that the logical function and its complement are both available simultaneously at the outputs is a further advantage in systems design. It not only decreases

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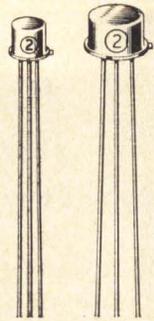
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BV <sub>CEO</sub>	I <sub>C</sub> = 10mA	30V min.	30V min.	30V min.	30V min.
I <sub>CBO</sub>	V <sub>CB</sub> = 30V	10nA max.	10nA max.	10nA max.	10nA max.
I <sub>EBO</sub>	V <sub>EB</sub> = 5V	10nA max.	10nA max.	—	—
h <sub>FE</sub>	V <sub>CE</sub> = 5V, I <sub>C</sub> = 1 μA	60 min.	60 min.	—	—
h <sub>FE</sub>	V <sub>CE</sub> = 5V, I <sub>C</sub> = 10 μA	100 min.	100 min.	40 min.	40 min.
h <sub>FE</sub>	V <sub>CE</sub> = 5V, I <sub>C</sub> = 1mA	120 min.	120 min.	100 min.	100 min.
NF	V <sub>CE</sub> = 5V, I <sub>C</sub> = 10 μA, r <sub>g</sub> = 10KΩ, Bandwidth = 10 Hz to 15.7 kHz	2db max.	2db max.	3db max.	3db max.

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the processing time of the system, but also reduces up to 30 per cent the number of modules necessary to achieve a given processing function.

### Complementary Transistor Logic

Complementary Transistor Logic (CTL) circuits were developed and introduced by Fairchild for high-speed logic applications similar to those for which Motorola markets the ECL circuits. The CTL circuits utilize PNP emitter followers to perform the input diode (AND diode) gating function. The gate is controlled by very small amounts of current at the input. The system features low output impedance coupled with high input impedance. Most of the system operating current is utilized in charging or discharging capacitance during switching.

In these non-inverting, non-saturating emitter-follower gates the output follows the input almost immediately. Delay time is small since unnecessary charging of transition capacitance has been eliminated. The output follows the most negative input, so that all inputs must be high for the outputs to be high. If any input is low, the output is low.

Oscillation from emitter-follower circuits can be a problem in both CTL and ECL but Fairchild has attempted to overcome this problem in CTL in several ways.

- The PNP transistors have been designed to have a relatively low  $f_T$  of about 30mC.
- The internal node common to the PNP emitters and the NPN base is not made available. This fixes the PNP capacitance and reduces inductance at the NPN base.
- The PNP has a built-in collector resistance.
- Damping resistors have been added to help stability further and provide pulldown current proportional to the fan-out of the driving element to improve its fall-time.

The advantages stressed by Fairchild for CTL include:

1. High speeds without costly subsystem packaging and sacrifice of noise immunity;
2. Average delays per logical decision

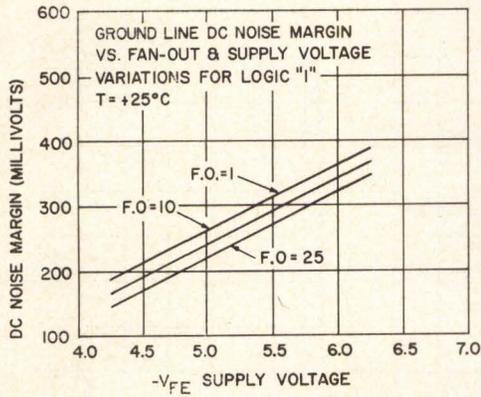


Fig. 12 Ground line dc noise margin vs. fan-out and supply voltage variations in ECL circuitry.

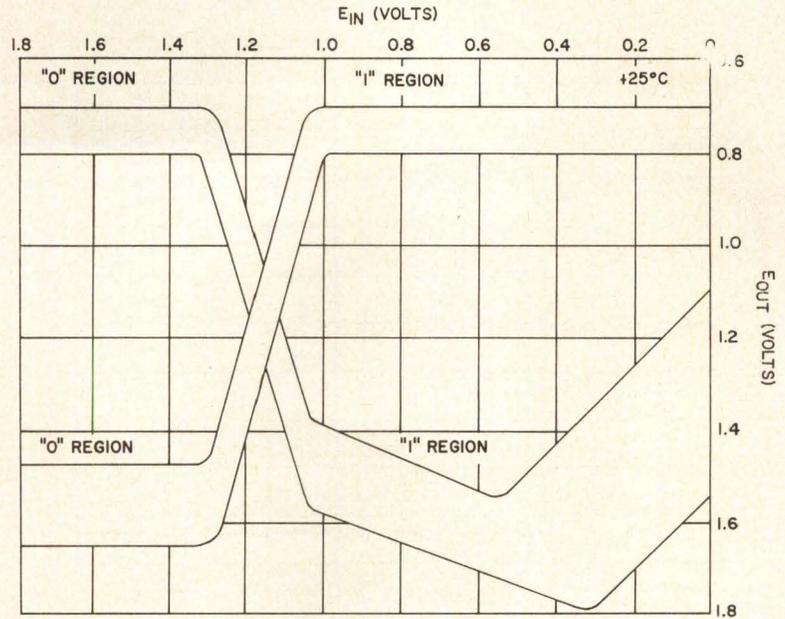


Fig. 13 ECL worst-case noise margins for ground line disturbances as they vary with variations in supply voltage and fan-out at 25°C.

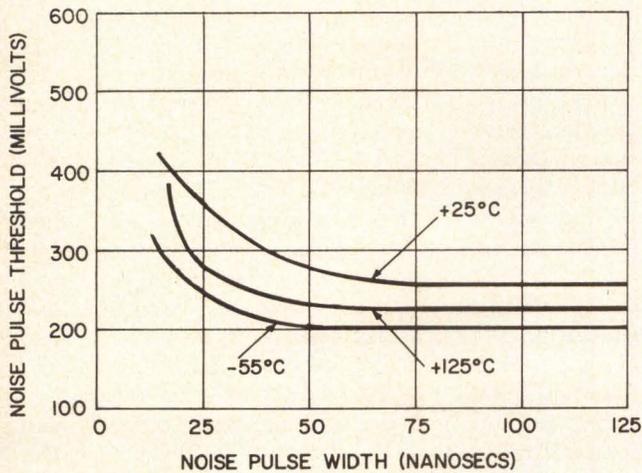


Fig. 14 ECL input signal line noise pulse thresholds vs. noise pulse width and temperature (90% distribution level) at fan-out of 1.

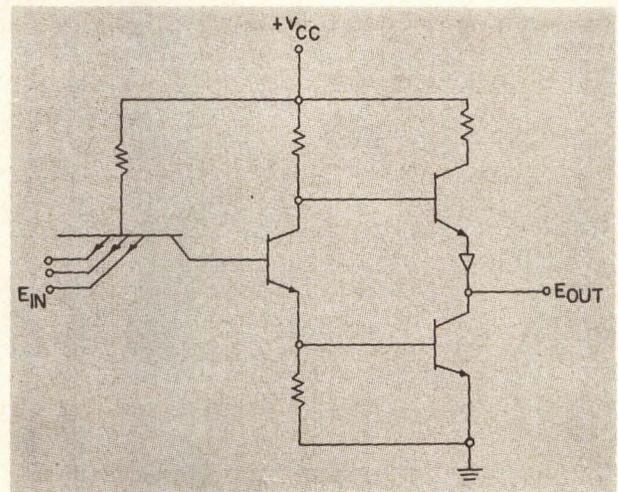


Fig. 15 Basic TTL circuit.

of 5-7 nsec using conventional non-laminated printed circuit boards;

3. Operation with wide power supply tolerances of  $\pm 10$  per cent.

Industry experience with CTL circuits indicates that while CTL is slower than ECL, it eliminates many of the problems experienced with ECL. The type of circuitry involved is very similar to the original AND/OR gating.

Critics of CTL have found some disadvantages worth noting.

1. While the emitter-follower exists in both CTL and ECL, the stability problem of having one emitter-follower driving another one, as in CTL, may be worse than the stability problem of one emitter-follower, as in ECL.

2. The gain through the AND/OR circuits is less than unity, thus limiting the number of such stages that can be cascaded.

3. An application where a string of AND/OR operations might be beneficial is in low-speed desk calculators

where the AND/OR module communicates with shift registers directly, but this feature is a disadvantage in most other systems.

### Transistor-Transistor Logic

The logic line which most closely approaches the speed of ECL circuits is known as Transistor-Transistor Logic (TTL or T<sup>2</sup>L). This circuitry was originally known as Transistor-Coupled Logic and was developed to solve the problems of capacitive

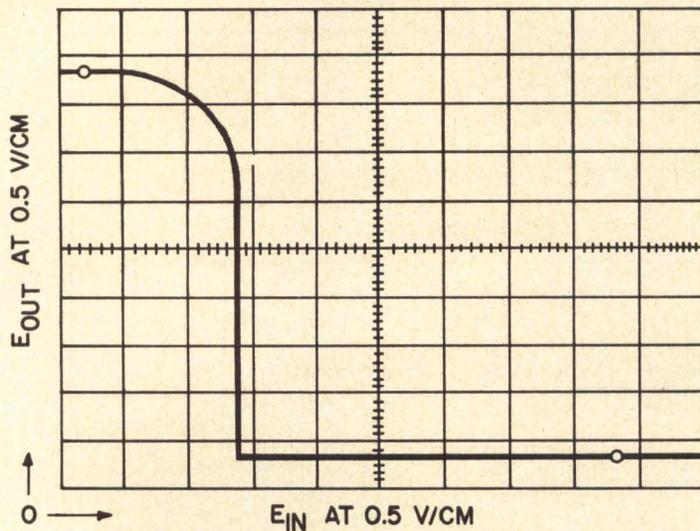


Fig. 16 Transfer characteristic of TTL gate circuit.

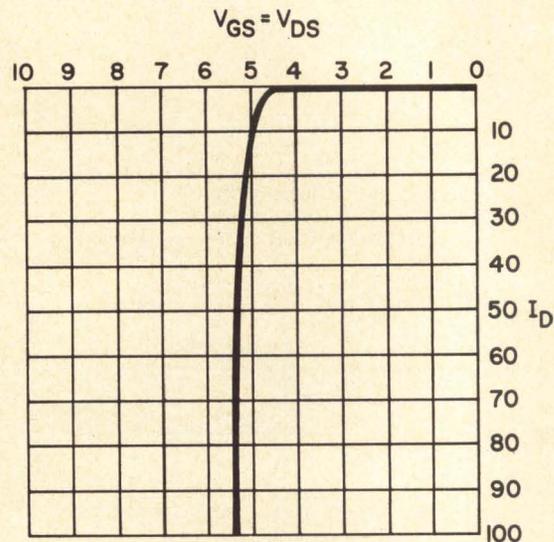


Fig. 17 MOS turn-on characteristics at 25°C.

loading resulting from some packaging schemes, such as flat-packs on multi-layer printed circuit boards.

T<sup>2</sup>L is another modification of DTL, in this case using faster responding transistors at the input rather than diode elements. Also, the T<sup>2</sup>L output typically has an active pull-up as well as pull-down, permitting high-speed operation to be maintained while driving long lines or capacitive loads. The basic T<sup>2</sup>L circuit is shown in Fig. 15. There are two basic approaches to the fabrication of T<sup>2</sup>L — the output threshold diode is located either in the emitter leg or in the base of the output pull-up transistor. When the diode is located in the base circuit, its associated substrate capacitance is added at the collector node of Q<sub>2</sub>, reducing response time at that node. Locating the diode in the emitter removes this capacitance and gives an improved speed characteristic.

The diode's location is also critical in establishing the turn-off time of the output pull-up device. If the diode were located in the base circuit, its recovery time would have to be slow to allow the charge to be pulled out of the base circuit. This need for a special slow recovery diode can be eliminated by placing the diode in the emitter circuit, thereby reducing the turn-off time for the output pull-up device. This time-saving feature also helps to keep the T<sup>2</sup>L circuit's internal noise to a mini-

mum, which is particularly important because this type of circuit tends to generate a large amount of internal noise. When the input logic levels are changing the outputs to the low logic state, the upper output device turns off and the lower device turns on. During this operation, there is a short period of time when both outputs are ON at the same time. This causes a low impedance across the power supply, resulting in a surge of current in the supply line. The width of the current spike depends on the length of overlap, and the overlap can be reduced by improving the turn-off time of the output pull-up device. This is accomplished by locating the output threshold diode in the emitter leg.

Typical T<sup>2</sup>L circuitry has a power dissipation of 14 mW and a propagation delay of 3 ns. The dc noise margins are comparable to those of DTL circuits and are approximately 400 to 500 mV. The transfer characteristic is shown in Fig. 16.

In addition to T<sup>2</sup>L's other advantages, the fact that requirements on the individual components within the circuit are not very stringent leads to good yields in production.

#### Metal Oxide-Silicon Devices

Metal Oxide-Silicon Devices (MOS) are particularly useful where large arrays of logic devices are indicated.

In very large arrays the MOS devices use only 3 masks, one of which is used twice. It has one shallow diffusion. The normal bi-polar circuits require 6 or 7 different masks. The number of process steps is approximately 120 to 150 which is about half the number required by a typical bi-polar device. MOS devices, as presently offered, have a frequency limit of one megacycle whereas, bi-polar circuits are in excess of 10 megacycles. Speeds within the MOS arrays have been measured at much higher levels. In fact, Fairchild has reportedly observed propagation delays of one nanosecond or less within large arrays. The external buffering required for these arrays makes it impossible to take full advantage of this speed unless extremely complex circuits are used. In the MOS devices there are essentially two types — the enhancement mode and the depletion mode. A single MOS device, as manufactured by Philco, is an enhancement mode device which requires approximately -5 V for a conduction of 10 microamps of current. See Fig. 17 for turn-on characteristics.

A MOS device has characteristics very similar to those of a pentode tube and, consequently, its transconductance is a measure of gain and not beta or h<sub>FE</sub> as for conventional bi-polar transistors. The average transconductance of single devices is approximately 1,000 micro ohms. A

**Table 1**

**MANUFACTURERS' LITERATURE**

A complete set of manufacturers' literature on integrated logic circuits can be obtained by circling, on the reader inquiry card, the numbers listed below.

COMPANY	INQUIRY CARD NO.
Amelco Semiconductor, Mt. View, Cal. ....	110
Fairchild Semiconductor, Mt. View, Cal. ....	111
General Instrument Corp., Hicksville, N. Y. ....	112
ITT Semiconductor, West Palm Beach, Fla. ....	113
Motorola Semiconductor Products, Scottsdale, Ariz. ....	114
National Semiconductor Corp., Danbury, Conn. ....	115
Philco Micro-Electronics, Santa Clara, Cal. ....	116
Radiation, Inc., Melbourne, Fla. ....	117
RCA Electronic Components & Devices, Harrison, N. J. ....	118
Ravtheon Co., Lexington, Mass. ....	119
Signetics Corp., Sunnyvale, Cal. ....	120
Siliconix, Inc., Sunnyvale, Cal. ....	121
Sperry Semiconductor, Norwalk, Conn. ....	122
Sprague Electric, No. Adams, Mass. ....	123
Stewart-Warner Microcircuits, Sunnyvale, Cal. ....	124
Sylvania Electric, Woburn, Mass. ....	125
Texas Instruments, Inc., Dallas, Texas ....	126
Transitron Electronic Corp., Wakefield, Mass. ....	127
Westinghouse Molecular Electronics, ElkrIDGE, Md. ....	128

circuit design using MOS differs greatly from those using conventional bi-polar transistors. A circuit is much easier to design using MOS. For example, a designer of digital circuits knows that a MOS can operate as a relay tree and can, consequently, base his designs on this model.

The breakdown voltage of a conventional MOS is identical to that of a bi-polar transistor using the same resistivity materials. This is approximately 50 volts.

The principal advantages of MOS devices can be summarized as follows.

- More functions per dollar in suitable arrays can be designed.
- Low power.

The gate has an input impedance of greater than  $10^{15}$  ohms. Therefore, in applying 10 or 20 volts to  $10^{15}$  or  $10^{16}$  ohms, very little power is dissipated in a typical circuit. This permits a design of a device that has minimum current-carrying capacity. Generally speaking, the faster the device must operate, the more power it is going to take to perform the function.

The principal disadvantages of MOS devices are:

- Sensitivity to noise due to a relatively poor noise margin;

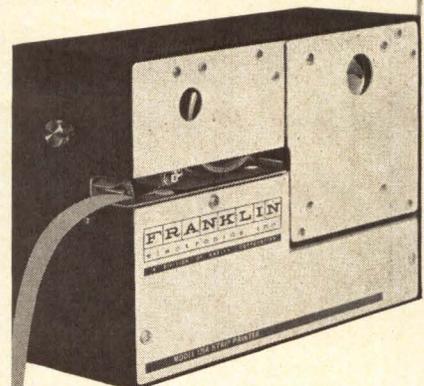
- Limited speed capability in most applications;
- Difficulty in obtaining circuits.

The manufacturing advantages of MOS in terms of the relative simplicity has already been described. On the other hand, the fact that the device depends on an oxide layer makes it more sensitive to surface impurities. Therefore, much greater precautions must be taken in manufacturing MOS devices. Only two or three manufacturers are now offering a significant number of MOS devices and delivery, at best, has been unreliable (with the exception, perhaps, of shift registers). It is expected that this problem will clear up with time.

**Summary**

The foregoing was a brief evaluation of the major integrated circuit logic forms that are now available from IC manufacturers. It is recommended that the reader supplement this article with specification data from these manufacturers. Complete literature on each manufacturer's logic families can be obtained by using the Reader Inquiry Card in this issue. Table 1 is keyed with the appropriate inquiry numbers.

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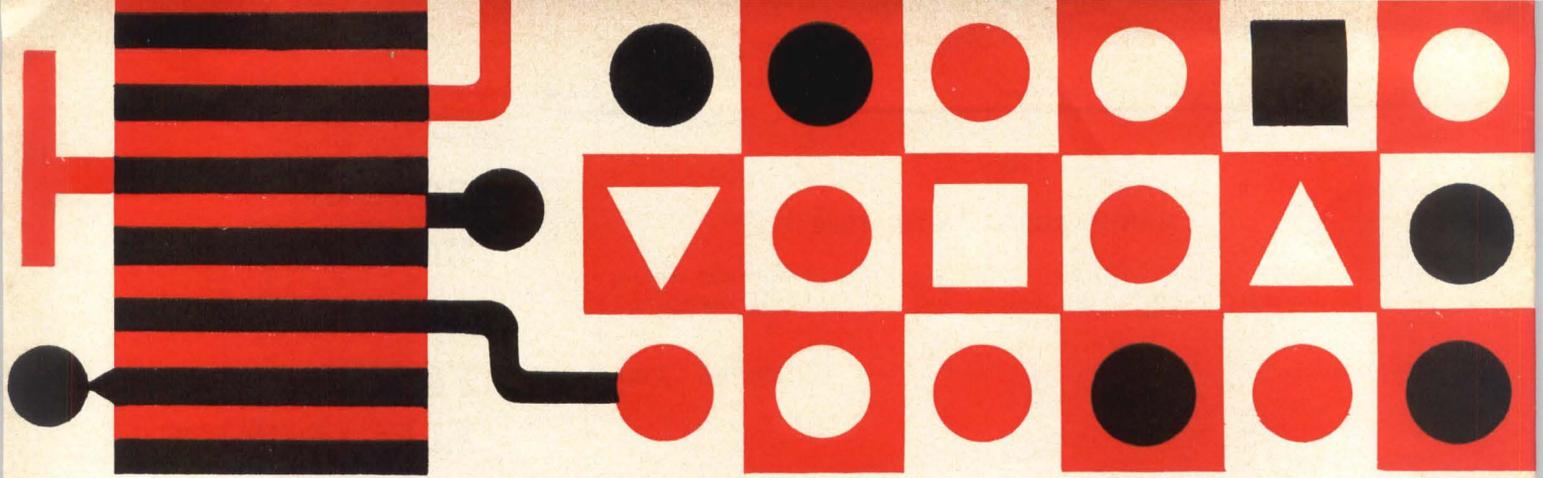
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# Hardware Features That

**DR. IVAN FLORES,**  
Associate Professor of E. E.,  
Stevens Institute,  
Hoboken, N.J.

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Editor's Note: Noting that only lately are hardware designers beginning to examine how computers could be better constructed to help the user, Dr. Flores explores some hardware features that can facilitate software operation and programming.

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One of the leading experts in computer technology, Dr. Flores is best known for his

series of text books on both hardware and software. Such books as **Computer Logic** (1960), **Logic of Computer Arithmetic** (1963), **Computer Software** (1965), and **Computer Programming** (1966) are among the industry's standard references. All are published by Prentice-Hall, Englewood, N. J. As Associate Prof. of EE at Stevens Institute, Dr. Flores is now conducting research in the effective use of mass memories, as well as teaching programming design courses. His consulting work includes a wide range of associations from manufacturers to software designers.

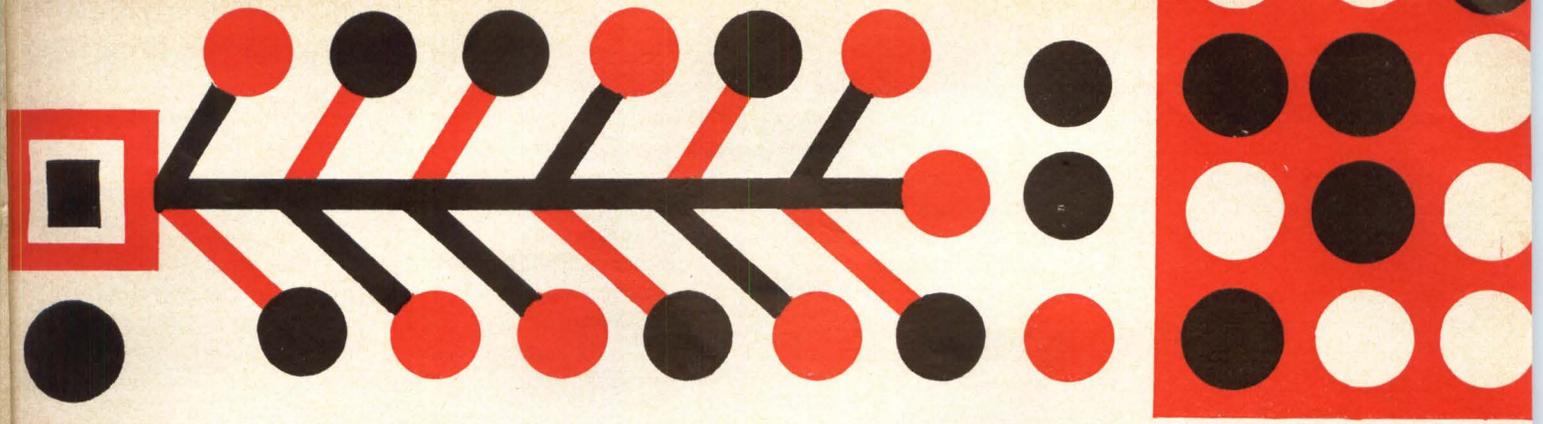
This is a blue sky discussion. It investigates hardware concepts which should be considered for inclusion in computer hardware in order to facilitate certain programming operations. These hardware concepts are:

- Pushdown lists or pushdown stacks.
- Threaded lists and their manipulation.
- The associative memory.
- Level control to keep track of what portion of a program is being used.

## PUSHDOWN LISTS

The pushdown list is a list structure where new items are constantly placed on the end; items are accessed serially in the reverse order from how they were placed on the list. Pushdown lists are sometimes called stacks because they work like stacks or plate lifters that you find in cafeterias; take one plate from the top and the stack of plates pops up, revealing the next plate. If you want to insert more plates, you put them on top — a last-in-first-out pushdown stack.

A pushdown list can be implemented in several different fashions. Burroughs has implemented it in their B5000 and B5500 with two active registers plus a number of cells in memory. New words are entered into the two active registers until they are filled and then words are placed in successive cells in memory. The difficulty is that when the two registers get full, use of the cells in memory to form the list requires a relatively long time. In order to make a pushdown list more effective and to provide a substantial gain in hardware manipulation of information, we may place the entire list in very high-speed memory (100 or less nanoseconds per word). With such a high-speed memory, manipulation



## Aid Programming

of information in the list can be masked by other machine operations.

*Why are we interested in pushdown lists?* Here are a few reasons, some of which we will further discuss:

- Keeping track of lists of data;
- Assembling and compiling;
- Level control;
- Implementing hierarchies of memory;
- Information retrieval.

One specific application used by Burroughs involves programming in Polish notation at machine language level. A program is made of syllables placed in a sequence; some syllables are operation codes, others are addresses. For each formula, these syllables are entered into a pushdown list and they appear in the program in the same sequence in which they are placed in the pushdown list. Then, as the list is "popped" up, operand addresses are scanned and operands brought from memory. Operations are performed also in sequence from the list.

This may seem like just another way to program. However, in order for it to work, the program information had to be in proper sequence, and once we get the problem construction broken up in this fashion it is a simple matter for a computer with a pushdown list to execute the program without further translation. The steps required to convert a formal programming language such as ALGOL into Polish notations are indeed brief, and it is very easy to construct a compiler to go from ALGOL or FORTRAN into Polish notation.

### Addressing The Pushdown List

Control operations and the program itself may address the list directly. We use "may" in the sense that

the designer may or may not make these facilities available to the programmer. It may be more effective for some lists to be addressed implicitly. When a particular control operation is called for, then the list implied by that operation is automatically addressed. For instance, the program could be stored in list and an "instruction-fetch" operation would always imply the use of that pushdown list. For list addressing, we use simple addressing logic which keeps track of the cell used; to memorize, it increments the memory address counter to get the address of the next cell. To recall information from the pushdown stack, we refer to the item just placed there — hence, we use the memory address register as it stands. After recall, we push up the stack automatically by decrementing the memory address counter. We might have tags in a command which suspend pushup. Further, we can make our pushdown lists more elaborate by enabling multiple pushups.

Another feature which could be incorporated is a small high-speed memory for storage of a program loop (repeated subroutine) in progress. The loop memory would be addressed by the program, which would store the next (for example) eight commands in the loop memory, or a repeat command would automatically store the next group of commands in the loop memory, from which it would be executed.

### THREADED LISTS

The threaded list has enabled the computer to perform thinking and conceptualization processes, and to attack problems by association in the way that humans do. It made possible, for instance, the work by Weizenbaum<sup>1</sup> at MIT in programming a machine to do Rogerian psychotherapy. The threaded list concept is not just a laboratory scheme; it offers a wealth of new modes of

performance in practical field applications.

A threaded list structure provides one means for having a computer react like a human whose associations can be reconstructed as list processes. How this function is performed in the human brain is another question, but we can certainly empower the computer to associate if we furnish it with threaded list structure manipulation capability. Playing games, checkers, chess, etc., requires associative ability. All kinds of accounting and processing procedures, such as inventory control, information retrieval, depend upon manipulations of immensely large lists of information. Retrieval of a multi-topic bibliography requires manipulation of lists. If these are threaded lists it should be possible to manipulate them easier. (There are, of course, other problems to information retrieval, but if we provide a computer with a list manipulation facility then maybe we can get to work on the other problems.)

### Threaded List Operation<sup>2</sup>

Each word of the threaded list stores three things: a datum of interest; a pointer to the next word in the list; and a tag which indicates whether this is a data word or a branch word. There is no need to place sequential words of the list in sequential cells in memory, which is why the list is called threaded; a word connects to another word which may be physically very distant or very close and the list just meanders back and forth among words in the memory. The datum part of the threaded list word may be a complete record or it may be simply an address, in which case, a list word points to the address of the desired record. To establish a correspondence during the list search, some specifier (the key), which is part of the record, is also in the data part of our link word. To review, in the word we have:

- Complete datum — the key and the address of the data record;
- The pointer — the address of the next word;
- A tag which specifies whether this is a data word or a branch word.

A branch word contains the tag which tells us that it is a branch word and two pointers (addresses), which enable us to branch into two sublists. We shall explore the usefulness of this.

### Automatic List Search Hardware

If the program directed a list search with automatic hardware it would be delegated to a search unit. This unit would receive the list starting word location and the key of the desired item. The search hardware would work with the main memory just as the rest of the computer does, and memory access for list manipulation would be shared with access by the rest of the computer. This might be done by interspersing memory requests among the various units. Alternatively, the list search unit might have its own memory address register and memory data register which would operate in parallel with the main memory registers. In this case, we would

have one bank of cores with two memory address registers, two memory data registers, and two controllers. We would not have to worry about locking out information if we check that addresses in the two memory address registers are not identical, and arrange for priority operation if they were. There would be no other conflict situations.

Another alternative is to provide a separate automatic list search memory; all threaded lists are kept in this list memory. This might be better since the main frame would not be delayed during any list lookup. None of these schemes should delay the computer; even without multiprogramming we could look ahead, i.e., when we want an item we would request it a number of steps beforehand so it will be ready by the time we really need it.

### Hardware Operation

- Place the key (of the desired item) in a key register.
- Place start of list in the list register and in the present pointer register.
- A use register exists but is not occupied initially.

The pointer register contents are transferred to the memory address register and the first list word is brought to the use register. The contents of the key register are compared with the key portion of the use register. If they are equal, our job is done — we have located the desired list entry and we stop. The use register now contains the datum (or its address). If the contents of the key register do not equal the key portion of the use register, we have not found the item. We then extract the address pointer of the next word from the use register and put it in the pointer register. With a new pointer, we go to the indicated address, pull out the next word, put it into the use register, and continue as before.

### Antecedent Linkage

When there is a word in the use register it contains a link to its successor. However, there are times when we also need the antecedent (predecessor) to the present word. Let us pass the contents of the pointer register to an antecedent register, and then renew the pointer from the use register. This is useful when searching for an item less than, or equal to, a given item, for example, to enter an item onto a threaded list. If we wish to file an item with key 29, and have found an item whose key is 27, followed by an item whose key is 30, we know that the item with key 29 must be inserted between 27 and 30. Therefore, we must link from the antecedent of 30, which is 27, to 29; then we link from 29 to the successor of 27, which is 30. A similar process is used for deletion of entries from the list. We search for the item to be deleted, and when it is found we link its antecedent with its successor. The insertion and deletion processes may require the provision of a space list to keep track of available memory locations.

With the addition of the antecedent register, we may establish both these links after reaching the item with key 30:

- The antecedent register points at 27;
- The pointer register points to 30.

### Branched List

When we come to a branch point while searching a threaded list we have to make two searchers, one down the right side of the list, and another down the left side of the list. But, in addition, the right side may have a right and left side, etc. We solve this problem by introducing a pushdown list. When we reach a branch item, we store that branch item address into a "branch pushdown list", tagging it to indicate whether the right or left side is being explored. We then update the pointer from (for example) the right side of the branch item, which takes us down the right side of the list. We continue searching as before. At the next branch item we similarly tag it, put it in the branch pushdown list, and continue. If we search all the right sides and do not find the item, the search is not complete. We "pop" up the pushdown list and get the address of the branch item last used. Since the right side was used, we extract the left side address and go down the lefthand side of this last branch. When that is exhausted we know that the item is not in the bottom right or lefthand branch so we again pop up the pushdown list. Since we have used both sides of this branch item, we throw it away and pop up the list again, continuing until the desired item is found or we have exhausted all branches of the list.

### A Special Record Memory

We could incorporate the threaded list in a special record memory with self-contained controls, capable of executing commands such as "search", "append", and "delete". The command would be carried to completion, and the record memory subsystem would then either interrupt or wait for the central control subsystem to remove the information. The record memory subsystem would contain two storage areas — the threaded list structure, and a larger area for the storage of large data records.

For example, a "search" through a file in the record memory requires the file starting address and the key. The list hardware would sequence the threaded list for that file, match the key, and store the datum (or the data record) in a buffer area of the computer memory for posting or other processing, under control of the program.

### ASSOCIATIVE MEMORY

The record memory described above represents an associative memory. To summarize briefly, the associative memory is supplied with a portion of a datum for which we are searching. The memory lookup hardware then finds the datum for which the portion, the key, was supplied, and places this information in the memory data register. The uses of associative memory are almost unlimited. We could supply all kinds of tables to a large enough associative memory, and, later, look-up

of an item in these tables is accomplished with a single recall operation.

### Translators

There are two kinds of translators, the assembler and the compiler. For either kind of translation the programmer writes out, in source language, a description of the program to be translated. This generally includes symbolic addressing: quantities are given names which are later translated into cell locations by the assembler or compiler. The translator takes symbolic addresses as they occur in the source program and stores them in a list. In so doing, a cell assignment is made, usually starting from the top of memory and assigning sequential cells to the symbols as they occur. When a symbol is detected in the program, we check to see whether it has been previously encountered. If it is an old symbol, it appears in the dictionary and is replaced in the program step by the assignment that was made previously by the translator. The way translators work today, as each new item is added to the dictionary it is kept in order, perhaps by an insertion sort; the next symbol that the translator picks up can then be looked up more easily by going through this dictionary, not from beginning to end, but by a systematic search.

We can see how useful the associative memory would be in this application. We make up our symbol dictionary sequentially. Each symbol is entered, as it arises, in the next slot in memory and the assignment itself is recorded immediately. To examine each symbol to determine if it has already been assigned, we put the symbol in the key register and search the associative memory. If the symbol is absent an assignment is made. If there is already a cell number for that symbol, it is provided by the associative memory.

To make the assignment of a symbol in the key register, we enter the symbol into the first empty memory cell, providing with it the assignment that the assembler makes. This methodology is possible for not only simple symbols as used with the assembler but symbol sequences, blocks of symbols, and arrays (made, for instance, in FORTRAN with a dimension statement). Here we put the name of the array variable into the associative memory, with not only an assignment of the first cell but also an indication of the number of the cells in the array. Whenever this symbol is encountered again we access the associative memory and determine if the symbol is present and, if it is present, whether the assigned limits have been obeyed. For instance, if the array is JOHN and we have assigned 10 cells to it, then JOHN + 6 is certainly in the array but JOHN + 11 is not, and this can be verified, very simply, with our associative memory.

### Loaders

The loader is furnished by the program with the names of a number of subroutines upon which the program will be calling. The loader then must bring in each subroutine from the subroutine library, when it is called out by the program. The loader locates the location of the subroutine from the subroutine table where all sub-

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routines are listed in order. If this table of contents of the subroutine library were available in associative form, then any call could be looked up and the subroutine location in the library found immediately. Also, if the subroutine call table at the front of the program was placed in an associative memory, use of the subroutine calls within the program might be made easier.

### Supervisor

A supervisor also has a number of subroutines which it calls upon when a crisis is at hand — for instance, if the program gets into chaotic trouble which cannot be remedied, a dump is called for. The dump routine is found by going to a particular location within the supervisor proper and then, from there, getting the present location of the dump routine. This list of important routine locations could be stored in associative memory along with other information, for instance, the program re-entry point when exit is made to an interrupt or other program or assemblers. All this information is available by requesting it by its symbolic name, and it is also stored in a manner which makes it easier to update.

### Input-Output Control System

The input-output control system manages all I/O operations, and usually contains a large number of subroutines, whose jump joints could be stored in an associative memory. Further, as in the translator, files and I/O devices could be given symbolic names. As these are introduced they could be posted into an associative memory so that reference to a file can be done symbolically and names retrieved through association. Also, the buffering of I/O devices is done by buffer pools which are threaded lists of buffers — our threaded list concept has already been applied. An associative memory can provide further aid to our buffering. If we want to locate buffers for a given file, we go to the associative memory, look up the file names, and pick out the pointer to the string of buffers for that file. The threaded list structure enables us to search only this buffer list to find a free buffer or a desired full buffer.

### LEVEL CONTROL

A level control is a method for keeping track of where the program is. Hardware facilities have already been implemented for handling interrupts so that a program can go off to another routine, service I/O, and then return at a later time to where it left off in the program. We also have techniques which we call linkages for leaving the program to go to subroutines. We use index registers or the like to keep track of where we leave the main program. Level control, on the other hand, uses a pushdown list to keep track of where we are in the main program. Additionally, it provides great facility for doing this in depth — for skipping around among many subroutines and then returning to the main program.

### Nesting

A subroutine may call upon another subroutine which may in turn call on a third subroutine; this is multiple nesting. To get from one subroutine to the next we leave a trail and provide communication between inner and outer subroutine.

With a pushdown list, each time we leave a program segment we enter the absolute address of the jump point into that list. We handle data in a similar fashion, placing it either in the same pushdown list or, possibly, into a separate list. Now when we go into an inner subroutine, we simply enter the absolute address, at which we leave the first subroutine, in the stack. When we go to the third inner subroutine we leave an address in the pushdown list indicating where we left the second. To go back to the second subroutine, we push up the stack to find the place. To go back to the first one, we push up the stack and find the place. To go back to the main program, we push up the stack once more.

Not only does this technique permit keeping track of jump points, it also allows data to be stacked right on top of the jump point information; however, a separate data stack simplifies data handling.

### Interrupts

The above technique can be used for handling interrupts. We can even handle a system of priorities for the interrupts. Thus, while one interrupt is being handled another one may come along; if the second interrupt

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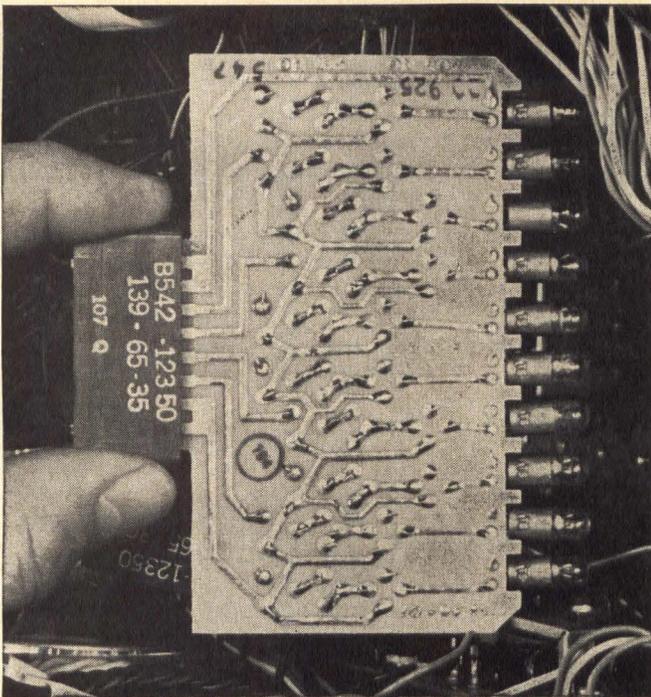
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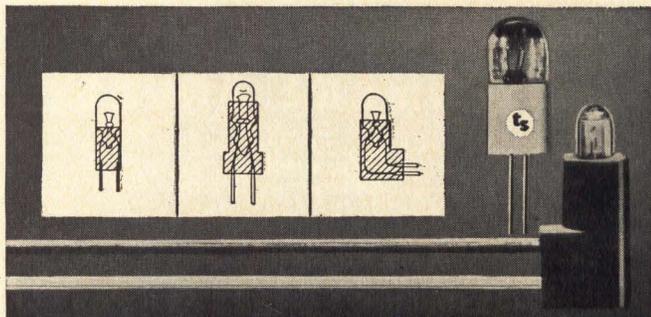
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ranks higher in our priority scheme, it interrupts the first interrupt. We enter the departure point from the first interrupt into the level pushdown list. We service the second interrupt, and, when finished, go back to the first interrupt via the level stack. Finally, we push up the stack again to go back to the main program. If, on the other hand, the second interrupt, which just came in, is to be postponed, we can put it in a "postponed pushdown list" to wait until the first interrupt is serviced.

### Multiprogramming

Another use for the level control is for multiprogramming. If we are running several programs, a clock can interrupt one program to explore if other programs require servicing. To service a new program, information about the one interrupted is placed in a pushdown level control list. Priorities of multiprogramming can also be set up in a priority list which can be looked at when changing levels or going from a lapsed program to a new one.

### SUMMARY

We have examined several hardware features for facilitating programming and software operation, with the intent of making the hardware designer aware of the needs of the software user and the program user, so that he can make innovations in the hardware which will materially aid the actual users. As an analogy, audio equipment design should be based on the better enjoyment of music by the listener. Similarly, computer design should be based on the computer user, the problem poser, and the operator.

This objective has been notably lacking in past years. For example, take the order codes and mnemonics used in a typical computer. They were designed for ease of implementation by the computer hardware. Consequently, when the user came around to programming with them he found little, if any, relation to the problems with which he had to deal. Only lately are we beginning to examine how computers could be constructed to help the user. Those who determine what features are to be incorporated into a computer must balance the cost of a feature against its projected usefulness to the consumer. The inputs to this decision-making process must come from the marketing man (who should know most about the consumer), the computer engineer, and the programmer. To get all these people together, properly communicating, is certainly an awesome task but one which must be performed if attention is to be paid to the role that hardware design can play in facilitating software operation and programming.

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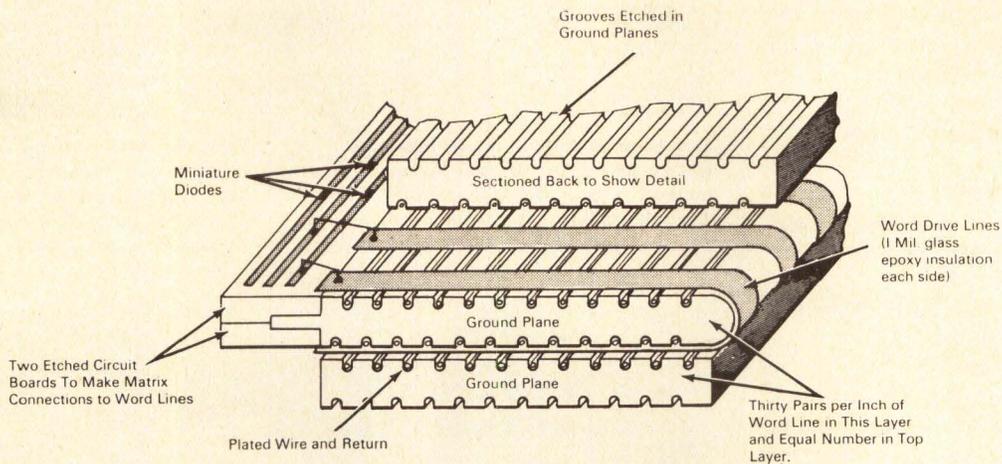
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1. Weizenbaum, Joseph, "ELIZA — A Computer Program for the Study of Natural Language Communication between Man and Machine," *Comm ACM*, Vol. 9, No. 1, Jan. 1966.
2. *Computer Programming*, Ivan Flores, Prentice-Hall, 1966, Ch. 8.

## NASA TECH BRIEF

A SUMMARY OF A SPECIFIC TECHNICAL INNOVATION DERIVED FROM THE SPACE PROGRAM. ISSUED BY THE TECHNOLOGY UTILIZATION DIVISION OF NASA.

# Improved Wire Memory Matrix Uses Very Little Power



### THE PROBLEM

To design a compact, rugged memory matrix for applications where available power is a limiting factor. Ferrite core memories draw 10 to 15 watts of average power and, in certain applications, this is intolerable.

### THE SOLUTION

A thin-film, plated-wire memory matrix that requires little power yet has higher speed and greater storage capacity than ferrite core memories of the same size.

### HOW IT'S DONE

A conducting ground plane of copper, magnesium, or aluminum has grooves etched in it to receive insulated plated wires. The wires are placed in the grooves and are held by a coating of varnish or other suitable material. Etched word lines, each supported between two flexible one-mil glass epoxy

dielectric sheets, are wrapped around the ground plane and connected to the matrix connections on etched circuit boards bonded to the ground plane. Two additional ground planes, with plated wires in etched grooves, are placed on top of and beneath the first ground plane to enable one word line to serve many more bit lines.

### NOTES

1. Placing the plated wire in this coaxial cable type structure reduces its surge impedance.
2. This configuration quadruples the number of bits per inch of word line over previous devices of the same size.

### PATENT STATUS

Title to this invention has been waived under the provisions of the National Aeronautics and Space Act (42 U.S.C. 2457 (f)), to Univac Division of Sperry Rand Corp., P.O., Box 500, Blue Bell, Pa. **END**

# DEVELOPMENT OF A LOW-COST TUNNEL DIODE

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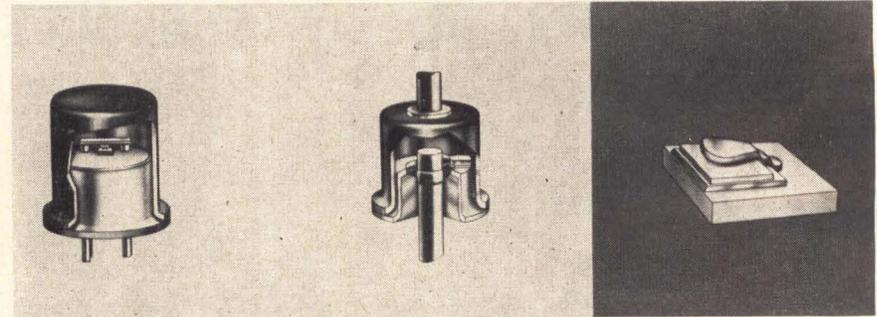
The first practical low-cost tunnel diode — priced as low as \$.50 in large volume — is now available from the General Electric Company. Designated the "TD700 Line" of tunnel diodes, the devices are available either in an axial leaded package for conventional circuits or in pellet form for use in hybrid integrated circuits. A combination of planar and thin-film fabrication techniques is the basis for the new, low-cost TD700 Line. The key development is a new technique used to form the tunnel junction with the germanium. The new batch processing techniques for manufacturing tunnel diodes are significant for two reasons. Not only can tunnel diodes now be priced at practical levels, but the devices can be supplied in pellet form for use with hybrid circuits.

Significantly reduced power levels, inherent with tunnel diode circuits, have become increasingly important as digital system designers increase their emphasis on speed. Higher speeds are limited by the interconnection delay times and can only be achieved with high packing density; in these cases, a low-power tunnel diode circuit is attractive.

Tunnel diodes offer advantages over other semiconductors in both speed and power consumption. Hybrid tunnel diode logic circuits have already achieved clock rates of over 400 megahertz at power dissipation levels under 40 microwatts. A hybrid scheme for current mode logic is believed to be ten times faster than its transistor counterpart.

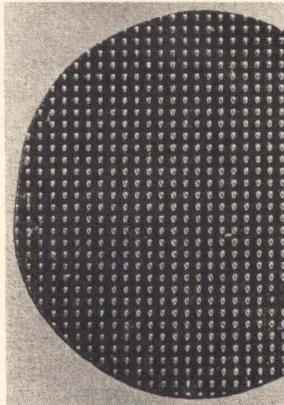
## Earlier Tunnel Diodes

The original tunnel diode, first introduced in 1958, was a small device that could act as a switch for steering circuits and shift registers at speeds approaching 100 megacycles. However, this early tunnel diode was extremely expensive, with an average price of \$75 per unit. High cost was

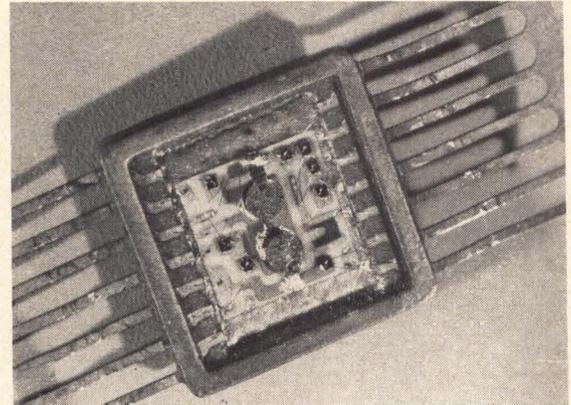


Evolution of tunnel diode fabrication is shown here. On the left is the original method where the sphere of semiconducting material is balanced on a pinnacle of germanium. The sphere wedged

between the germanium chip and the header lead technique is in the center. The right hand view shows General Electric's new, low-cost TD700 batch planar development.



Germanium wafer illustrates the results of batch processing techniques with over 1000 individual units per wafer.



Hybrid circuit application of new tunnel diodes in pellet form. This type of hybrid logic circuit can achieve clock rates of over 400 megahertz at power dissipation levels under 40 microwatts.

inevitable since each tunnel diode was made almost entirely by hand. This diode consisted of a pinnacle of germanium upon which the technician would place a sphere of semiconductor material. The operating junction would be between the point of the pinnacle and the sphere. Early construction techniques were analogous to balancing a golf ball on the point of a golf tee. This tunnel diode

was unable to withstand even minor shocks or temperature changes and its cost was very high, making it impractical for many applications.

New methods of construction were developed that solved some of these problems. The sphere was wedged between a germanium chip and a header lead. This dual support of a sphere between the germanium chip and the header was further aided by

potting the entire device in a special material developed by General Electric, making the device more reliable than its predecessor. Technical developments helped to lower the unit price to an average of \$2.80 per unit. In spite of these improvements, the device was still impractical for large-volume applications.

### New Batch Fabrication Method

The TD700 line is a breakthrough in mass production techniques. Working with several whole wafers of germanium, a thin film of silicon oxide is applied on each wafer by selective masks. With the same technique, a thin film of chromium is placed over the oxide. The junction-forming metal is then applied, overlapping the chromium and the exposed germanium. The wafers are passed through an oven which simultaneously alloys all of the junctions. After pelletizing the wafers, the pellets are mounted to headers, the leads are attached, and the units are etched to the proper peak current values. To complete the unit, a cap is welded to the header. The new tunnel diodes can operate at clock rates of 100 megacycles, with some functions approaching 400 megacycles. Tunnel diode power dissipation, a nominal 40 microwatts per unit, will allow the designer to develop logic systems with many more functions within a given space. The integrated circuit revolution has contributed significantly to high speed by permitting very close spacing of transistors, minimizing interconnection delays. High heat dissipation and slower switching speeds of IC's are said to create a market for the TD700 Line of hybrid tunnel diodes. The TD700 pellets in an IC function couple the short delays of IC's with the tremendously higher switching speeds of tunnel diodes.

### New High-Temperature Line

A special material development now allows General Electric to offer a line of germanium tunnel diodes that can operate at 125°C. Designated the "TD700H Line" of tunnel diodes, these devices can now meet military specifications. Both the TD700 and the 700H tunnel diodes are available with peak currents of 0.5, 1.0, 2.2, 4.7, and 10 milliamperes.

### Rigorous Test Procedures

Special classifiers and test systems have been developed to handle the particular testing requirements of the TD700 Line for production, engineering, and quality control. One example is a tunnel diode digital classifier. This classifier is completely digital in operation, using digital programming of test conditions, an analog-to-digital converter for parameter measurements, digital programming of classification limits, and a digital comparator for minimum and maximum limit determination.

The classifier will perform up to 30 tests in any order for any of the six static parameters of the tunnel diodes. Static tests include peak current and voltage, valley current and voltage, and maximum forward-and-reverse voltage, all of which can be classified by the analog-to-digital converter. A digital readout of the parameters of the tunnel diodes is used to classify them into any of twenty types.

Average time for each test is about 70 milliseconds except where several tests are made at the same test condition. In this case, the time required for each repeat test is less than 15 milliseconds. Peak point current can be measured over the range of 10 microamperes to 120 milliamperes with an accuracy of  $\pm 0.25$  percent, a reproducibility of  $\pm 0.05$  percent, and a resolution selectable to either three or four digits.

The same system can be used to measure the tunnel diode parameters for quality control or engineering purposes. It provides a digital readout of one individual parameter or all the parameters in a programmed test sequence. The entire TD700 Line undergoes strict testing and measurement procedures in order that the failure rate of the devices will be as close to zero as possible.

### Summary

With tunnel diodes competitively priced with other semiconductors, designers will be free to use the device where it offers advantages over other alternatives. Also, tunnel diodes available in pellet form for use in IC arrays allow the designer to exploit the distinct advantages of both the IC and the tunnel diode.

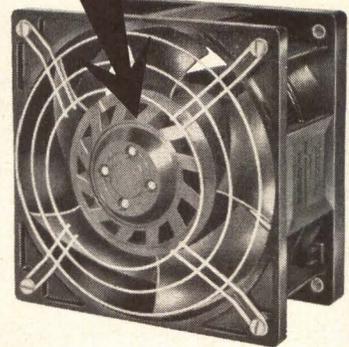
For more information on these new tunnel diodes:

Circle No. 103 on Inquiry Card.

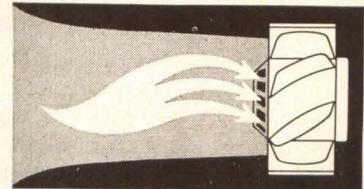
**350 cfm  
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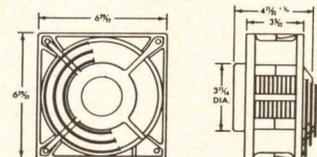
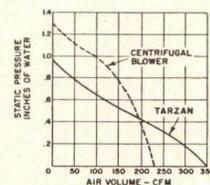
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CIRCLE NO. 39 ON INQUIRY CARD



## NEW PRODUCTS

### COUNTER/CONTROLLER

New counter/controller offers add-subtract capabilities said to be heretofore not available. The new unit accepts without error, simultaneous and overlapping add-subtract pulses. Count rate is 120/min add, 120/min subtract with rates up to 600/min available. Total count above or below preset always displayed. Decitek, Inc., Worcester, Mass.

Circle No. 211 on Inquiry Card

### COORDINATE MEASURING SYSTEM

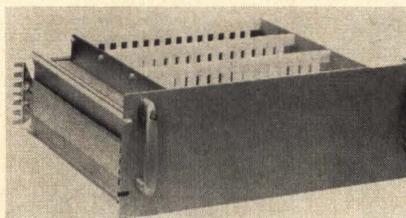
A coordinate recording and measuring system eases the programming load on production NC machines. The system employs a "Trav-A-Dial" precision measuring instrument as the basic transducer to detect motion in increments as small as 0.0005". This motion is translated into electrical signals by a shaft encoder housed inside the Trav-A-Dial. The electrical signals are then translated to a clear, front panel numerical display of encoder position. Simultaneously, this information is received by the punch control unit which operates the paper tape punch directly. The proper tape word format is provided with a programming plug inserted on the punch control unit front panel. The two digital Trav-A-Dials are mounted so as to measure two plane coordinate information (X-Y). The operator, in preparing his work piece tape drilling program, moves a sighting crosshair in an X-Y scanning motion until the desired point or artwork is brought under the crosshair. The operator then presses a button which enters the location automatically, in proper code, on the tape. An NC tape is thereby developed without interruption of machine production schedules. IKL Inc., Newport Beach, Cal.

Circle No. 251 on Inquiry Card

### INCREMENTAL PLOTTER

A Model 6650 bi-directional incremental plotter operates from a wide variety of driving signals. Both the pen and paper move independently in discrete or incremental steps at speeds up to 18,000 increments per minute following an input which supplies change of state information. These inputs may include digital computers, incremental encoders, pulsers, four-wire commutated encoders, pulse generators, stepper motor drive circuits, or contact closures. The pen will draw a continuous trace or plot points utilizing the programming inputs to the pen lift circuitry. The Model recorder uses fan-fold paper which can be separated at perforated lines to yield 8½" x 11" or 11" x 17" notebook size records. Because the paper is of a fan-fold variety all portions of the record may be read as one would read a book. The recorder accuracy is 0.002" and it may be either powered from ac or dc sources. Houston Omnigraphic Corp., Bellaire, Texas

Circle No. 239 on Inquiry Card



### CIRCUIT CARD DRAWER

A horizontal equipment drawer with a capacity of up to 60 circuit cards is said to feature an unusual suspension system that allows complete access to circuit cards, connectors, and wiring. Designated the Model 500 "Tilt-File" Drawer, the unit accom-

### SWITCHING/DRIVER DIODE

A new silicon planar epitaxial diode featuring a whiskerless construction and subminiature size, was designed to provide high mechanical strength and long-term stability in critical circuits. In addition, electrical characteristics are maintained under high temperature reverse bias conditions. Called W-O-W for "without whiskers," the diode is a high conductance type for high speed switching and core driver applications. Specifications include low junction capacity of 2 picofarads. The hermetically-sealed package is a dual stud, fused glass-to-metal design. Hughes Semiconductor Devices, Newport Beach, Cal.

Circle No. 250 on Inquiry Card

### TAPE-TO-TAPE CONVERTER

A tape-to-tape converter, Model TTU can be programmed to convert any 5 to 8 level input code to any output code. The TTU consists of a paper tape reader, electronics package, and paper tape punch for the code conversions or reproduction of paper tape. The unit is offered in 2 models, one-way conversion or two-way conversion. Applications include code conversion for subsequent transmission, computer input, or numeric control of machine tools. Digital Electronic Machines, Inc., Kansas City, Mo.

Circle No. 273 on Inquiry Card

modates 3 full-depth card files holding up to 20 circuit cards each. Additional storage space is provided for front-panel mounted accessories, switch gear, and other equipment and components. The hinged tilting mechanism lifts to expose card connectors and wiring for assembly, servicing, or system checkout without removal of the drawer from a standard 19" equipment rack. The open construction of the drawer provides maximum ventilation area for system cooling. Scanbe Mfg. Corp., Monterey Park, Cal.

Circle No. 247 on Inquiry Card

## VIDEO DISC RECORDERS

Magnetic disc recorders will store 525-line video frames, one per concentric track, with high density. Frames can be stored in the form of analog video at frequencies up to 4.2 Mc, or digital video at 200,000 bits per frame. One type, the F Video Disc Buffer, stores up to 20 tracks (frames) of video. There is a fixed read-write head on each track, so that any selection of recorded frames can be simultaneously displayed on separate consoles. Any frame can be updated without disturbing the other displays. High resolution black-and-white and color video can be displayed by using more than one track to store the frame. A second type, the M Video Disc Recorder, uses interchangeable cartridge discs, which store 131 tracks (frames) of video on each side. The single movable head can be positioned by digital control signals to record or reproduce any frame on any selected side in an average time of  $\frac{1}{3}$  second. High storage density is achieved by a proprietary technique of placing the magnetic head in actual contact with a thin-film plated disc without causing significant wear. A single track can be scanned continuously for thousands of hours with negligible degradation in the quality of the reproduced picture. Data Disc, Inc., Palo Alto, Cal.

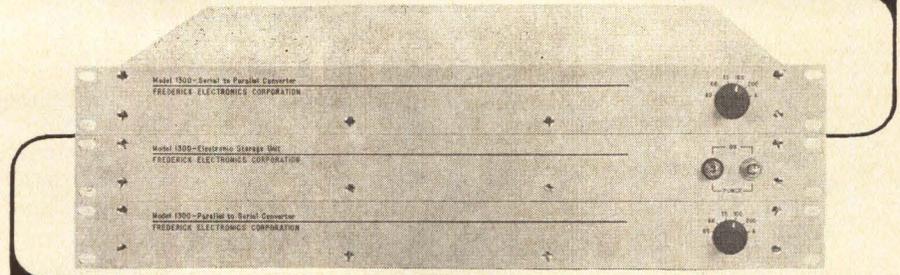
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## PUSHBUTTON SWITCHES

A snap-action, 2-position, momentary pushbutton switch is described by the manufacturer as the "smallest pushbutton switch with the highest ratings on the market today." This single-pole, double-throw, snap-action, pushbutton switch has inductive and resistive ratings of 7 amps, 125 volts, ac; 5 amps, 250 volts, ac; and 5 amps, 29 volts. The dc minimum rating for low energy circuit applications is 10 micro-amps at 50 mw. Two different terminals types are offered: combination solder, quick connect, single turret terminals; and printed circuit terminals for direct mounting to printed circuit boards. The Arrow-Hart & Hegeman Electric Co., Hartford, Conn.

Circle No. 228 on Inquiry Card

## AN INTERFACE BETWEEN TELEPRINTER CIRCUITS



## REQUIRING TEMPORARY OR BUFFER STORAGE...

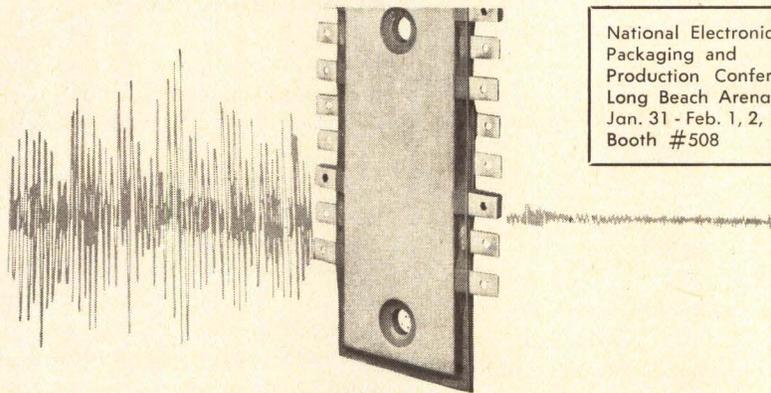
- Uses magnetostrictive delay line with 2400 character minimum storage for accepting, regenerating and temporary storage of signals
- Input is standard 5 level teleprinter code, 7.0 units or longer in length, 60-200 wpm
- Output is standard 5 level teleprinter code, 60-200 wpm
- Packaged on plug-in circuit cards
- Three separate assemblies
  - (a) Serial to parallel converter
  - (b) Electronic storage unit
  - (c) Parallel to serial converter
- Solid-state digital packaged for mounting in standard 19" relay racks.

Model 1300 Electronic Storage Unit / \$2400.00 F.O.B. Frederick, Md. / 90 days delivery



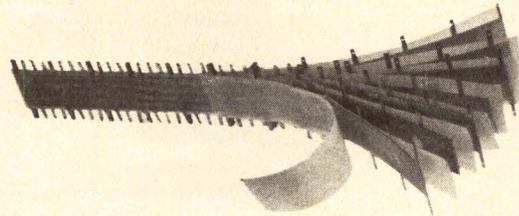
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Flat bus conductors laminated with Eldre's thin, rugged insulation will reduce electrical noises which cause havoc in high speed, solid state equipment. Lower the inductance and control the capacitance of your vital power distribution lines. Ground shields are interleaved with the voltage-carrying conductors so that effective shielding can be adequately provided. The terminations of each conductor, as shown, are for soldering but other types can be incorporated into the bus design. This compact and completely molded bus can replace a bulky harness and repetitive wiring.

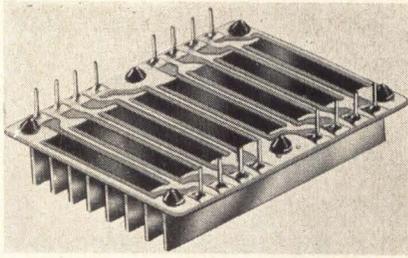
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## NEW PRODUCTS



### RESISTOR MODULES

Precision, high-power, cermet resistor modules are said to be ideally suited for use as a terminating resistor module in digital circuitry. Power is 9 watts per module with each resistor capable of dissipating over 100 watts per square inch of resistor area through a copper heat sink bonded to an aluminum substrate. Combinations up to 24 output pins on 0.125" centers are available on a single module. Accordingly, assembly costs are reduced because only the single module need be handled instead of many separate resistors. Resistance range is 20 ohms to 1 megohm, resistive tolerance is only  $\pm 1.0\%$  and TC  $\pm 200\text{PPM}/\text{C}$ . Special low resistance values are available down to 10 ohms. Inductance is less than 10 nanohenries. CTS Research, Inc., Lafayette, Ind.

Circle No. 234 on Inquiry Card

### DISPLAY TUBES

Feature of a new display tube is the envelope width — a maximum of 0.75" — allowing the tubes to be arranged at less than 0.80" center-to-center. Optimum use of panel space is thereby permitted, providing more attractive displays. The Model BA-840 is a 10-character display tube, numerals 0 to 9; the BA-841 is a 10-character display tube, numerals 0 to 9 with an independent decimal point to the left of the numerals; the BA-842 is a 10-character display tube, numerals 0 to 9 with an independent decimal point to the right of the numerals; and the BA-843 is a 2-character display tube, symbols plus and minus. Baird-Atomic, Inc., Cambridge, Mass.

Circle No. 277 on Inquiry Card

### LDX COMPUTER SYSTEM

Xerox Corp. moved into the EDP field with a new unit for graphic input to and printout from computers. The new equipment, known as the LDX/Computer Adapter, provides a totally new capability for LDX (Long Distance Xerography), the company's high-speed facsimile transmission equipment. Graphic data such as charts, graphs, or grids can be fed into an LDX scanner, much as they would be into an office copier. Through the use of the adapter, located near a computer anywhere in the country, the information is converted into computer language and either stored on magnetic tape or combined with other information already in the computer. Revised or up-dated information is then reconverted through the adapter and the LDX printer which reproduces the data on ordinary paper at speeds up to 500 pages (8½" x

11") per hour. The printer can be located near the adapter and computer or at a point anywhere across the nation. Since the LDX computer system needs no intermediate, it can operate on-line (no time lag), giving immediate graphic response to the demand for information from the computer. Model I is designed to operate with the IBM System/360 Series, although adapters compatible with computers manufactured by other companies may soon be available. Since the LDX units can operate over broadband communications links, it's possible that a number of company locations could share the same computer using LDX scanners and printers as the input and output devices. Lease price for the LDX/Computer Adapter Model I has been set at \$1050 per month plus a basic monthly charge of \$1200 for an LDX scanner and printer. Xerox Corp., Rochester, N. Y.

Circle No. 258 on Inquiry Card

### COMPLEX-FUNCTION IC

Five new complex-function digital integrated circuits include a dual adder, a quadruple adder, a divide-by-12 counter, a 4-bit binary counter, and a BCD-to-decimal decoder/driver. Two of the complex ICs are available in a new molded dual in-line package featuring 16 pins. The five new bipolar ICs are additions to a family of TTL circuits. The SN7482N dual adder performs the addition of two 2-bit binary numbers. Sum outputs are provided for each bit, and the resultant carry is obtained from the second bit. The monolithic dual adder is designed for high-speed, multiple-bit, parallel-add/serial-carry applications. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. Speed is 15 nanoseconds carry time through two stages, and 35 nanoseconds add time. Price is \$5.75 in 100-999 quantity range. Texas Instruments, Dallas, Texas.

Circle No. 256 on Inquiry Card



### SHAFT ENCODER

A Model SC-24-7 shaft encoder converts position angles into sine and cosine for input to a digital computer for computation of position coordinates. Both quadrant and sign information are also supplied. Encoder output code is V-scan binary. There are 128 readouts of the sine function and cosine function per revolution. Angular resolution is arc sine 1/128 (57'52") or the equivalent of approximately one part in 775 for a single turn. Unit is a synchro-type mounting, size 24 with a length of 2.085 inches. Litton Industries Encoder Div., Chatsworth, Cal.

Circle No. 248 on Inquiry Card

## CORE MEMORY SYSTEM

A new product line of core memory systems covers the cycle time range of 0.6 usec to 1.0 usec. The basic modular building block in the memory is 8,192 words by 20 bits using 20 mil ferrite cores in a 2½D organization. Up to 4 memory modules which include the core memory, sense amplifiers, driver circuits, and information registers can be accommodated vertically in a standard 19" rack by 26" panel height. Monolithic integrated circuits are used for all the logic and the information and address registers. The line drivers and sense amplifiers utilize hybrid microcircuits. Overall power consumption for 8,192 word by 20 bit module is only 295 w (for the 0.6 usec system). An associated memory control module which includes the timing circuits, address register, and decode logic is also available. One control module is capable of servicing up to 4 memory modules and can be packaged in one of two mechanical configurations. One mounts horizontally in the standard 19" rack. The other has identical dimensions of the basic memory module and may be mounted vertically, adjacent to the memory module (s). The latter may be employed when less than 4 memory modules are used. Power supplies capable of driving 4 memory modules and one control module are also available for 19" rack mounting. Burroughs Corp., Electronics Components Div., Plainfield, N. J.

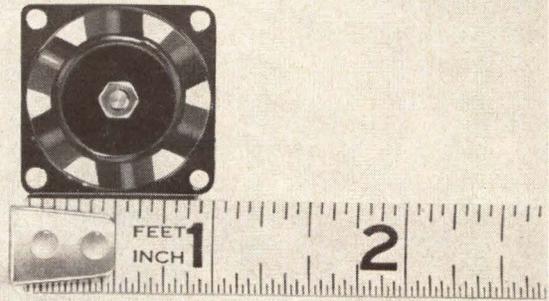
Circle No. 221 on Inquiry Card

## TAPE TRANSPORT

New series of digital magnetic tape transports was designed for on-line operation with medium and high performance computers. These "end-user" units are direct replacements for digital magnetic tape transports operating on computers currently in use with a greatly reduced cost to the end-user, according to the company. Average cost of this end-user transport is said to be less than 50% of the manufactured equipment currently in use on computers. Midwestern Instruments, Tulsa, Okla.

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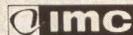
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## NEW PRODUCTS

### COMPUTER TAPE

A new magnetic tape is reported to be three to five times as durable as any present computer tape. Designated MRX-III computer tape, it has been extensively field tested under the most adverse conditions in more than 50 different computer installations. According to the manufacturer, all results showed MRX-III superior not only in extra-long-life before permanent failure, but in dropout activity. The new tape is available in bit-per-inch densities of 556, 800, full-width 800, and 1600 (3200 fci). It is compatible with all computers and tape handlers. Memorex Corp., Santa Clara, Cal.

Circle No. 214 on Inquiry Card

### CATHODE RAY TUBE

A new, large-screen, flat-face, high-resolution cathode ray tube was designed primarily for the scanning of, or recording on, film. According to the company Model L-4192's large screen affords, for a given film size, reduced screen loading with resulting longer phosphor life, reduced phosphor noise, and greater resolution than can be achieved with smaller tubes. A special phosphor deposition process is said to produce an exceptionally blemish-free screen. The tube is electromagnetically focused and deflected, and has a 40-degree deflection angle. Spot size is 38 microns. The tube has a minimum useful screen diameter of 8 $\frac{3}{8}$ ", overall length of 26", and an outside diameter of 9 $\frac{1}{4}$ ". Litton Industries' Electron Tube Div., San Carlos, Cal.

Circle No. 213 on Inquiry Card

### ELECTRONIC CALCULATOR

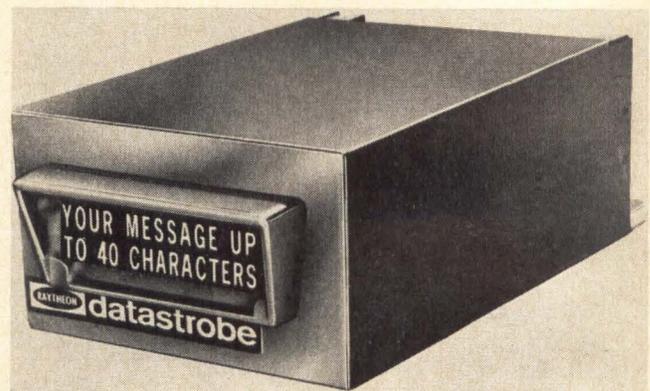
Second generation electronic calculator is three times faster than its predecessor. Dubbed the IME-86, it is said to be the first to offer up to seven random access working/accumulating registers. Because of this exclusive ability, the user for the first time can solve mathematical problems, both commercial and scientific, just as they are normally written on paper without re-sequencing or re-arranging them to "fit" the machine. The new machine also offers fully-automatic re-entry from all registers — said to be another exclusive feature. The IME-86 stores 16 digits, plus sign and decimal in each of its registers. Keyboarded data may be verified after calculating without reference to a printed tape. Another unique feature is the ability to raise whole or decimal numbers to a power with continuous visual proof of the power index. Square root extraction of whole or decimal numbers is instantaneous by the touching of a single key. The calculator is priced from \$1,445.00 to \$1,995.00 depending upon features. IME, U. S. A., Inc., Los Angeles, Cal.

Circle No. 232 on Inquiry Card

### IC TESTER

The need for widely-varying capabilities in an integrated circuit tester is said to be answered in a new modular-design test set. The Model 800 IC Tester can be ordered with varied combinations of modules to give it optional features or greater or lesser degrees of test capability. The basic unit is a housing with a base, test socket, and switches, to which can be added, in several combinations: a 10x20 or 10x40 crossbar matrix, which allows sequential testing of similar parameters without reprogramming; provision for up to five external inputs or outputs; five analog or digitally-programmable power supplies; panel readout meter and ranging switches; connection for hook-up of external DVM or oscilloscope; internal resistance and capacitance loading; and a pulse generator. The Model 800 tests all present IC configurations, and is said to be designed to accommodate any foreseeable future developments in the field. The Birtcher Corp./Instrument Div., Monterey Park, Cal.

Circle No. 276 on Inquiry Card

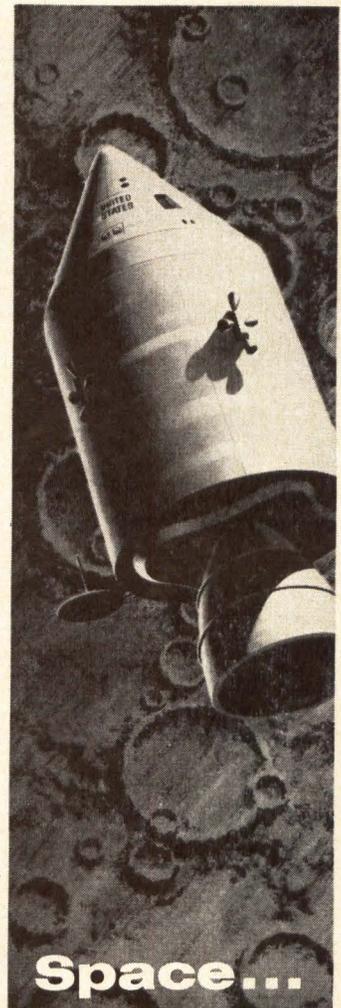
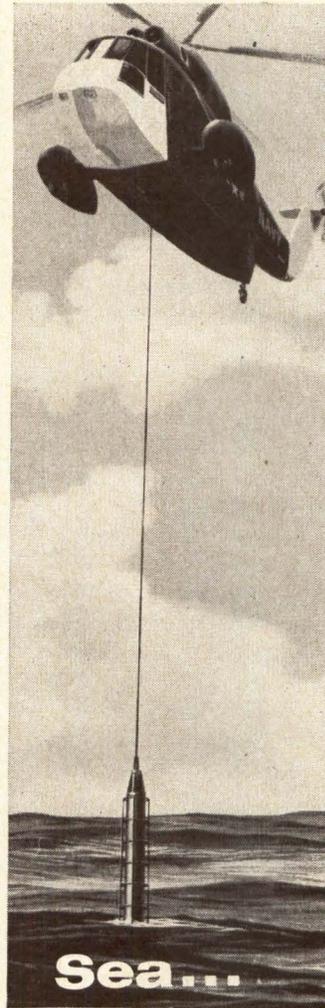


### MESSAGE DISPLAY

Message display subsystems include decoding, driving, and display functions in a single package for less than \$5.00 per message in moderate production quantities. A typical message unit displays 8 or 10 high-contrast, white-on-black letters one-half inch high. These are presented in continuous line without breaks or separations. Where more information must be presented a subsystem is available with a total of 40 characters on two lines or 105 characters on three lines. Displays with heights from one-quarter to one inch or more are also obtainable. In addition, any other line information, such as symbols and schematics, that is photographically reproducible can be displayed. In effect, these new units are random access memory banks with display capability. The message units have logic input requirements compatible with integrated circuitry and are interfaced easily with most computers. Storage or electronic latching is optional. Models are available for parallel or serial BCD 4-bit or 6-bit input. As complementary inputs are not required, these message units are especially well-suited for readout at remote locations. Components Division, Raytheon Company, Lexington, Mass.

Circle No. 220 on Inquiry Card

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## AREAS

**LAND:** *Equipment Division* — Radar and display systems; communications and commercial data processing equipment and systems.

**AIR:** *Missile Systems Division* — Ground-to-air and air-to-air weapons systems and tracking radars.

**SEA:** *Submarine Signal Division* — Airborne, surface, underwater systems.

**SPACE:** *Space & Information Systems Division* — Space systems, subsystems and equipment for military and non-military programs.

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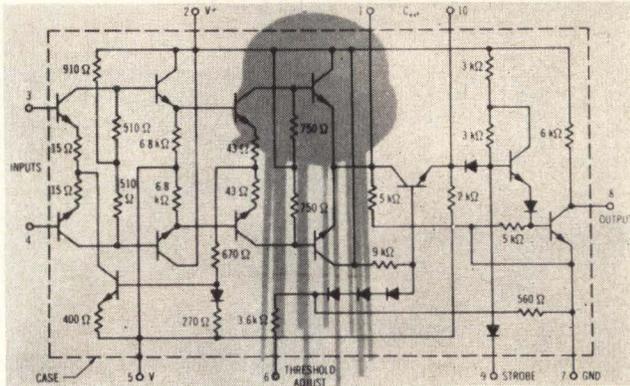
Send resume with salary requirements to: Manager of Executive Placement,  
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## NEW PRODUCTS



### MONOLITHIC SENSE AMPLIFIER

Improved integrated circuit techniques have made possible a new monolithic sense amplifier. These improvements, according to the manufacturer, allow greater gain stability with large variations in temperature, a narrow "uncertainty region" over a wide temperature range, a fast response time of 40 ns plus short recovery times of 50 ns with a 2 v common mode signal, and 80 ns with a 400 mv differential mode signal. The sense amplifier was designed to detect bipolar differential signals derived by a core memory with cycle times as low as 0.5 microseconds and to translate these signals into saturated logic output signals. This MC15406 integrated circuit package stage, differential amplifier — a dc restoration circuit with facilities to adjust externally the input threshold level from 10 to 25 mv without changing the width of the transition region. When pin 6 of the 10-pin TO-5 package is held to -6 volts, the nominal threshold is 17 mv. Also included on this same monolithic die is a DTL output gate which makes strobing the sense amplifier possible from any saturated logic family. Motorola Semiconductor Products Inc., Phoenix, Ariz.

Circle No. 233 on Inquiry Card

### DC POWER SOURCE

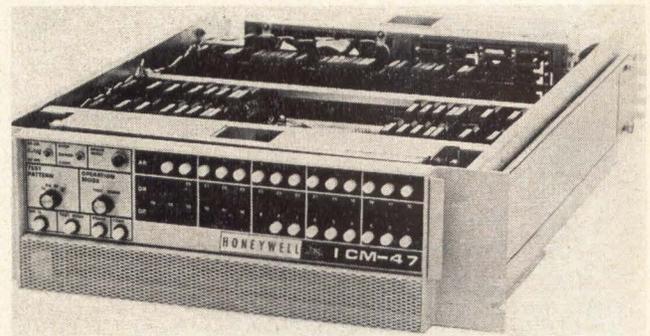
Compact 10-amp source of 3, 4, 5, or 6 volts dc is furnished in a package which plugs into a standard card bin and requires no external heat sinking or blowers. It employs what is called the Redule principle of output voltage programming by connection of jumpers or transformer taps. The supply provides a regulation of 0.01% plus 2 mv, a ripple below 1 mv peak-to-peak, and output voltage adjustment of plus or minus 1/2 volt of programmed value, and a stability better than 1 mv per 8 hours. The high stability is achieved by using a high-voltage, temperature-compensated zener diode voltage reference and an integrated differential amplifier input. The power supply is available with an optional built-in overvoltage protection circuit. Power Designs Inc., Westbury, N. Y.

Circle No. 222 on Inquiry Card

### CRT DISPLAY

A high-speed, real-time modular CRT display system permits user to "build his own" functional configuration. Designated Series 9000 modular display console, the new system features customer options of a customized or any standard keyboard, five other control devices, four display devices, and four different memory subsystems. The console's building-block design allows it to be interfaced with any digital computer installation and to provide exactly the control elements required for the specific display application. Typical random position access time is 4.0 ms to traverse and settle on any part of the 23-inch CRT. Formatted characters are function-generated at the rate of 4.0 ms each, including spacing. An optional display device generates vectors at a constant line writing rate of 0.75 inch per microsecond, including full-screen diagonal vectors. Four types of store/refresh memories are available: delay line, drum, disc, or core. Choice of memory depends primarily on amount of data to be handled. Tasker Instruments Corporation, Van Nuys, Cal.

Circle No. 210 on Inquiry Card



### IC MEMORY

New integrated circuit core memory system, the  $\mu$ -STORE ICM-47, features a full-cycle time of 750 nanoseconds and 400 nanoseconds access time. For 4,096 and 8,192 word memories, the maximum word length is 28-bits per memory module. In 16,384 word systems, word lengths up to 14-bits are available. For greater word capacity and extended word lengths, a number of ICM-47's may be "stacked." The unit uses a 2 1/2 D, three-wire coincident current magnetic core array, and employs integrated circuits for all logic, addressing, decoding, timing and control, line driving, and sensing functions. Operating ambient temperature range is 0C to 40C. Standard operating modes include clear/write, read/restore, and read/modify/write cycles. Output marker signals include memory busy, information available, and end-of-cycle. Circuit modules and wiring are easily accessible from the front of the memory system which can be installed in 5 1/4" of rack space. An optional power supply requires an additional 5 1/4" of rack space. The design of the memory system is said to result in the elimination of the numerous adjustments and controls normally required by other memories. Honeywell, Computer Control Div., Framingham, Mass.

Circle No. 268 on Inquiry Card

# When high performance peripheral equipment means a whole new ball game in the computer field

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## NEW PRODUCTS

### DECADE COUNTER/DISPLAY

A bright, clear in-line numerical display (plus decimal point), base preset, and 8-4-2-1 bipolar BCD outputs are some of the features of a new high-speed, forward-backward decade counter. The Model IC-803 will accept forward, backward, and reversing signals, either periodic or aperiodic, over the range of 0 to 3 MHz and requires no additional circuitry or modules for reversing. Since the unit has no reversing delay, it will change count directions at the full 3-MHz counting rate. Packaged in modular form, the 3" x 1" x 6¾" unit is available individually or mounted, with other similar units, in complete modular packages for OEM instrumentation applications. Janus Control Corp., Waltham, Mass.

Circle No. 201 on Inquiry Card

### MULTILAYER PRINTED CIRCUITS

A multilayer printed circuit board of 15 layers is intended for use in EDP applications. It retains compact dimensions due to precision techniques which allows 7000 holes to be placed in a area only 10" x 18". This board, which is 0.125" in thickness, is fabricated to the Institute of Printed Circuit Specifications. Methode Electronics, Inc., Printed Circuit Division, Chicago, Ill.

Circle No. 266 on Inquiry Card

### BINARY CONVERTER

With a new high-speed binary to BCD converter binary inputs with any number of bits up to 30 can be converted to the BCD equivalent in 25 to 45 usec. The converted binary data can be displayed on the front panel in decimal form with Nixie display tubes or with incandescent lamps in BCD form. The input binary code can be either in serial or parallel format. Electronic Engineering Co., Santa Ana, Cal.

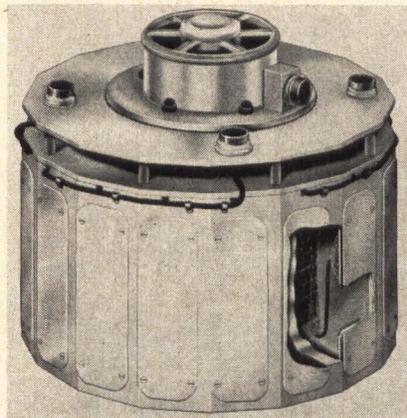
Circle No. 200 on Inquiry Card

### TAPE VERIFICATION

A new high-speed perforated tape verification and duplication station, the System 800, verifies and duplicates tapes from one through eight channels in any code structure at a speed of 120 characters per second. Two readers, a perforator, and a logic module are combined to form the System 800. The system can be used to verify or duplicate tape automatically or verify two tapes and perforate a third tape simultaneously. Errors can be corrected through use of the bit insert switch. There are 5 modes of operation: Duplicate — direct duplication of the prepunched tape in the master reader on a bit-for-bit basis at 120 characters per second; Verify — a bit-for-bit comparison of two tapes using both

readers to insure that the tapes are identical (if the tapes are not identical the reader will stop on the character in error and the bit indicator lights display the data characters in each reader); Verify/Duplicate — verification between two tapes and duplication of a third tape; Bit Echo/Duplicate — duplication of tape in the master reader with simultaneous verification of the duplicated tape as it is being punched in the perforator; and Bit Echo-Verify/Duplicate — duplication of tape in the master reader after verification against a second tape in the verify reader with simultaneous verification of the duplicated tape as it is being punched in the perforator. Tally Corp., Seattle, Wash.

Circle No. 249 on Inquiry Card



### MEMORY DRUMS

New magnetic memory drums can be modified to any application or specification for memory storage. Individual units are custom built,

modified from the basic design to meet customer specifications. Current memory capacity is 1200 tracks of 50,000 bits/track (Manchester) with two flux reversals/bit. Speeds range from 720 to 12,000 rpm. Synchronous, nonsynchronous, and variable-speed drums are available in all sizes to operate at all basic speeds. Additional specifications include a clock frequency of up to 2 MHz, a bit packing density of up to 1000/in., a track pitch down to 0.020 in., a track width down to 0.010 in. Flying heads require no radial adjustments and can be installed, removed, or tangentially adjusted without stopping drum. Western Magnetics, Glendale, Cal.

Circle No. 224 on Inquiry Card

### IC MULTIPLEXER

New multiplexer switch was constructed using hybrid integrated circuit manufacturing techniques. Contained in a standard 12-pin TO-8 can, it is designed to plug into miniature sockets which eliminates the necessity of soldering. The plug-in design is said to reduce maintenance time and cost to a minimum. The switch has a high off impedance of

100 megohms with less than 0.5 nano-amps leakage at full scale input. The device uses a Fet as a switch and contains a two-term AND gate. The switch plugs into a mother board capable of accepting from 1 to 32 multiplexer switches. The mother board is 8.0" by 12" in size and contains attenuators and filters for 32 switches. Redcor Corp., Canoga Park, Cal.

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## "TELETYPEWRITER FUNDAMENTALS HANDBOOK"

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## NEW PRODUCTS

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Circle No. 269 on Inquiry Card

### COMPUTER TAPE

A new computer tape is said to offer a major advance in long-term reliability. Called "Scotch" Brand No. 777, the new tape is certified error-free at all bits-per-inch densities up to and including 1600 bpi (3,200 FCI). A special oxide binder formula enables the product to deliver greatly extended error-free performance under heavy usage as well as the temperature and humidity extremes encountered during shipping or long time storage. 3M Co., Magnetic Prods., St. Paul, Minn.

Circle No. 216 on Inquiry Card

### X-Y PLOTTER

A single range 11" x 17" X-Y recording system is said to be particularly suited for displaying outputs from special-purpose systems. Access to data input connections and certain controls is from the rear to facilitate system application. All primary controls are accessible from the front. Features of the new plotter include a  $\pm 0.1\%$  of full-scale static accuracy, a 10" x 15" plotting area, and a 20 in./sec slewing speed on each axis. Any sensitivity between 1 mv/in. and 20V/in. may be specified by the customer for each axis; otherwise, 100 mv/in. is standard. Electronic Associates, Incorporated, W. Long Branch, N. J.

Circle No. 203 on Inquiry Card

## POWER SUPPLY MODULE

A new universal regulated dc power supply is said to be capable of replacing over 102 equivalent slot modules. The Model UPM-11 contains two independent sources, each providing 0 to 16 VDC at 1 amp. Output voltages and operating modes are determined by the wiring of the mating connector. No addition of components or shifting of internal jumpers or transformer taps is required. Output voltage may be selected by the mating connector in discrete 1-volt steps from each source. Two 25-turn interpolation potentiometers provide intermediate settings. The sources may be connected in series for double output voltage, in parallel for double output current, or symmetrical to ground for operational amplifiers. Each source has a regulation better than 0.01% plus 1 mV, ripple less than 1 mV peak-to-peak, response time less than 30 ms, operating temperature range of 0 to 50C (0 to 60C with derating) and temperature coefficient less than 0.015% plus 1 mV per C. Power Designs, Inc., Westbury, N. Y.

Circle No. 252 on Inquiry Card

## PUSHBUTTON SWITCHES

Panel mounted pushbutton switches feature a building-block concept for design and application versatility. Each unit may be ordered with a choice of colored, removable push-buttons in  $\frac{7}{8}$ " or  $\frac{5}{16}$ " diameter, colored facing nuts with convex or concave front surface, and snap-on switch modules in 2PDT or 4PDT, alternate or momentary action. Parts may be ordered separately or as completely assembled units. Designated the Series 19, these new switches are said to be easily mounted to a panel through a single cut-out. They are provided with a keying washer which locks them in place to prevent rotation. Switch modules can be wired separately and then snapped into place on the mounting bracket for ease of installation. It can also be easily removed for wiring changes without disturbing the panel mounting. Master Specialties Co., Costa Mesa, Cal.

Circle No. 237 on Inquiry Card

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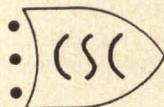
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**LITERATURE**

**Magnetic Recording**

Copies of a technical article entitled "Skew and Its Effect Upon Magnetic Recording" are available from a magnetic recording equipment manufacturer. The 12-page report covers the definition of skew, its effect on magnetic recording, the causes of skew, and techniques for the measurement of skew. Dartex, Inc., Santa Ana, Cal.

Circle No. 325 on Inquiry Card

**Incremental Recording**

An 8-page bulletin describes incremental magnetic recording and its place in modern data acquisition systems. Beginning with incremental recording fundamentals, the bulletin compares the relative costs, reliability, speed, and other important factors between various recording methods. Continuous and incremental reading options as well as a new "Flux-Check" method of verification of data from the tape are described in detail. Pointers to be remembered in the selection of incremental recorders and a partial list of users are included. Kennedy Company, Pasadena, Cal.

Circle No. 313 on Inquiry Card

**Control Computer System**

New intermediate-size process control computer system is described in a 4-page brochure. Designated the Prodac 250, it is a high-speed real-time control system with typical applications in the steel, electric utility, and petro-chemical industries as well as in automatic warehousing and repetitive manufacturing. The brochure describes the capabilities of the new system, lists hardware and software features including simplified control programming using Fortran IV, and also includes application information, dimensions, and specs. Westinghouse Electric Corp., Pittsburgh, Pa.

Circle No. 330 on Inquiry Card

**Miniature Components**

A 52-page engineering catalog presents a wide selection of miniature pushbutton and rotary switches, binding posts, test jacks, sockets, and module cases. Included is such technical reference data as useful life and failure criteria; contact and insulation resistance; rotational torque or actuating force; effect of ambient temperature; effects of altitude; etc. Grayhill, Inc., La Grange, Ill.

Circle No. 309 on Inquiry Card

**Megabit Core Memory**

A 10-page brochure describes a random-access large-scale memory system with access and cycle times of 300 and 650 nanoseconds, respectively, and a storage capacity of over 1 million bits — 16,384 words of up to 84 bits. Called the Nanomemory 650, the system is intended for real-time or high speed computers and checkout systems. Among items covered are the use of 2½D selection techniques, input and output pulses and levels, electrical characteristics and timing requirements, timing and worst case power consumption charts, self-test capabilities, and a functional diagram. Electronic Memories, Hawthorne, Cal.

Circle No. 310 on Inquiry Card

**Integrated Circuits**

A 16-page condensed catalog on digital and linear integrated circuits includes typical performance characteristics, schematic, power supply requirements, packaging, operating temperature range, and primary area of application. Also included is a full description of a systematic uniformity and reliability evaluation program that is said to assure specified performance, uniformity, and reliability in the ICs. Signetics Corp., Sunnyvale, Cal.

Circle No. 320 on Inquiry Card

## Core Memory Stack

Technical data sheet describes an economical core memory stack for military and space applications in which both a fixed program nondestructive readout (NDRO) and a destructive readout (DRO) scratch-pad memory are required. The approach is compared with the normal rope-core memory combination, with discussion of such advantages as reduction of selection and drive circuitry, unlimited ratio of DRO to NDRO storage and cycle times, volume, and power requirements that are equal to or less than conventional DRO-only coincident current stack. Data sheet covers construction, operation, and performance. A wiring diagram illustrates typical x and y drive line wiring for DRO and NDRO sections. Electronic Memories, Hawthorne, Cal.

Circle No. 326 on Inquiry Card

## Electronic Hardware

"Product Information for Design Engineers," a 28-page booklet covers a full line of products and fabricating services. Products include industrial laminates, electronic hardware assemblies, vulcanized fibre, fibreboards, specialty papers, and materials-handling products. In addition to typical product applications which are used to highlight material properties and characteristics, case histories in the problem-solution format show how product use can cut manufacturing costs or increase value. Spaulding Fibre Co., Inc., Tonawanda, N. Y.

Circle No. 329 on Inquiry Card

## Digital Modules

A 48-page technical catalog includes physical characteristics, operating specifications, related equipment, design aids, and application notes for a line of 28 encapsulated digital modules. Typical modules include most configurations of flip-flops, NAND/NOR gates, relay and indicator drivers, voltage comparators, power drivers, and multicircuits. Engineered Electronics, Santa Ana, Cal.

Circle No. 332 on Inquiry Card

## Data Communications

An 8-page engineering bulletin explains the equalization of telephone lines to make them suitable for high speed data communications. The bulletin discusses the basic problem of delay distortion and delay equalizers and considers various methods of employing equalization devices. Rixon Electronics, Inc., Silver Spring, Md.

Circle No. 331 on Inquiry Card

## Thumbwheel Switches

New 54-page thumbwheel switch catalog includes descriptions of company's complete line. The catalog contains truth tables showing codes and electrical output configurations, dimensional sketches, standard performance specifications, new revised prices, order blanks, and typical applications. Digitran Company, Pasadena, Cal.

Circle No. 306 on Inquiry Card

## Hybrid Computers

A family of totally integrated, general-purpose hybrid computers is described in a new 16-page technical bulletin. Featured is an in-depth discussion of how a hybrid computer has been used to solve a complex chemical processing problem, concerned with the refinement of chemical processes involving the interaction of a number of different chemical and petro-chemical compounds. Systems Div. of Beckman Instruments, Inc., Fullerton, Cal.

Circle No. 315 on Inquiry Card

## Low Voltage Lamps

A new condensed lamp catalog describes popular line of lamps for low voltage lighting uses. The incandescent lamps listed in this catalog include miniature, subminiature, and micro-miniature styles. Ready-reference tables give quick specification data such as lamp number, style of base and bulb, as well as voltage, current, candlepower, and life ratings. Hudson Lamp Co., Kearny, New Jersey.

Circle No. 312 on Inquiry Card

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# think faster think Burroughs memory systems

**IN MEMORY SYSTEMS THE FASTEST BIT  
MAKES THE DIFFERENCE . . . AND  
BURROUGHS MAKES ITS OWN BITS  
(BOTH CORE AND THIN FILM).**

The new Burroughs line of core Memory Systems is fast . . . as fast as 0.6  $\mu$ sec. full cycle time. You can also have a "not-so-fast" model at lower cost if you don't need the speed.

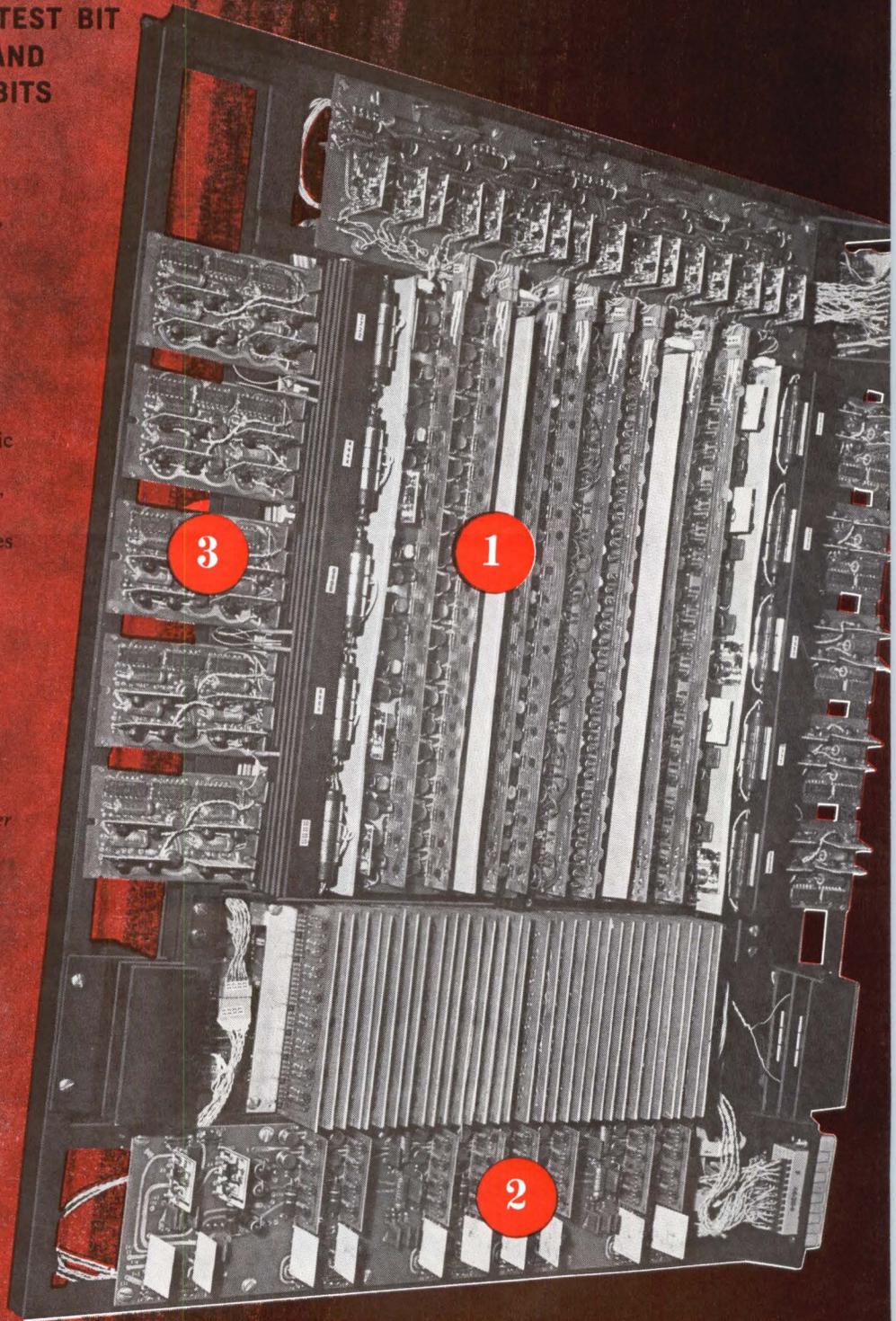
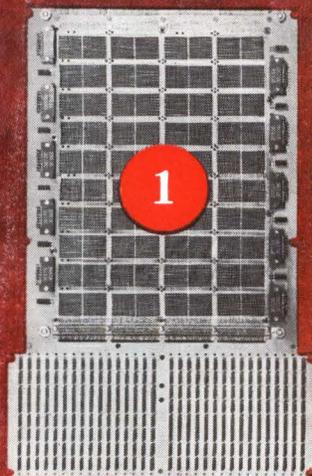
Now, Burroughs 14 years of experience is available to provide you with the Memory System you need for your data handling equipment.

- System cycle times of 0.6 and 1.0  $\mu$ sec.
- Modular building block construction—basic module is 8192 words by 20 bits and contains the core-memory, sense amplifiers, driver circuits and information registers.
- Associated memory control module includes timing circuits, address register and decode logic.

## FEATURES:

1. 20 mil, 2-1/2D ferrite core memory—manufactured by Burroughs.
2. Driver Circuits and sense amplifiers use Burroughs hybrid microcircuits.
3. Monolithic integrated circuits used for all logic and registers.

*If you would like your system to think faster write or call for further information on Burroughs memory systems.*



Testing integrated circuits is a key step in their production. At the Molecular Electronics Division of Westinghouse Electric Corporation, Tally perforators are used to log data as each module is run through a series of parameter checks. Data logged on the tape is then analyzed by computer.

According to W. DeLauder, Foreman of the Instrumentation Section at Westinghouse, the five Tally Model 420 perforators worked extremely well

during a fifteen month period just ended. Fewer than eight calls per perforator were made to keep all five perforators on duty over the entire period. The average time per call was 2.23 hours with an average cost for parts of \$3.05.

During the fifteen month period, the five perforators punched with precision over 478 miles of tape. There are a lot of good solid engineering reasons why Tally perforators are extraordi-

narily reliable. For all of them, please address Ken Crawford, Tally Corporation, 1310 Mercer Street, Seattle, Washington 98109. In the U.K. and Europe, address Tally Europe, Ltd., Radnor House, 1272 London Road, London, S. W. 16, England.



**There are five hard working  
Tally perforators on the job  
around the clock at Westinghouse.  
During one 15 month period, these  
perforators were ready for work  
99.9% of the time...and work they  
did, knocking perfect chad out of  
2,520,000 feet of tape!**

**How's that for reliability?**

*Here is the latest Westinghouse integrated circuit test console  
with a new Tally P-120 Perforator which turns out twice the work of the Tally 420.*