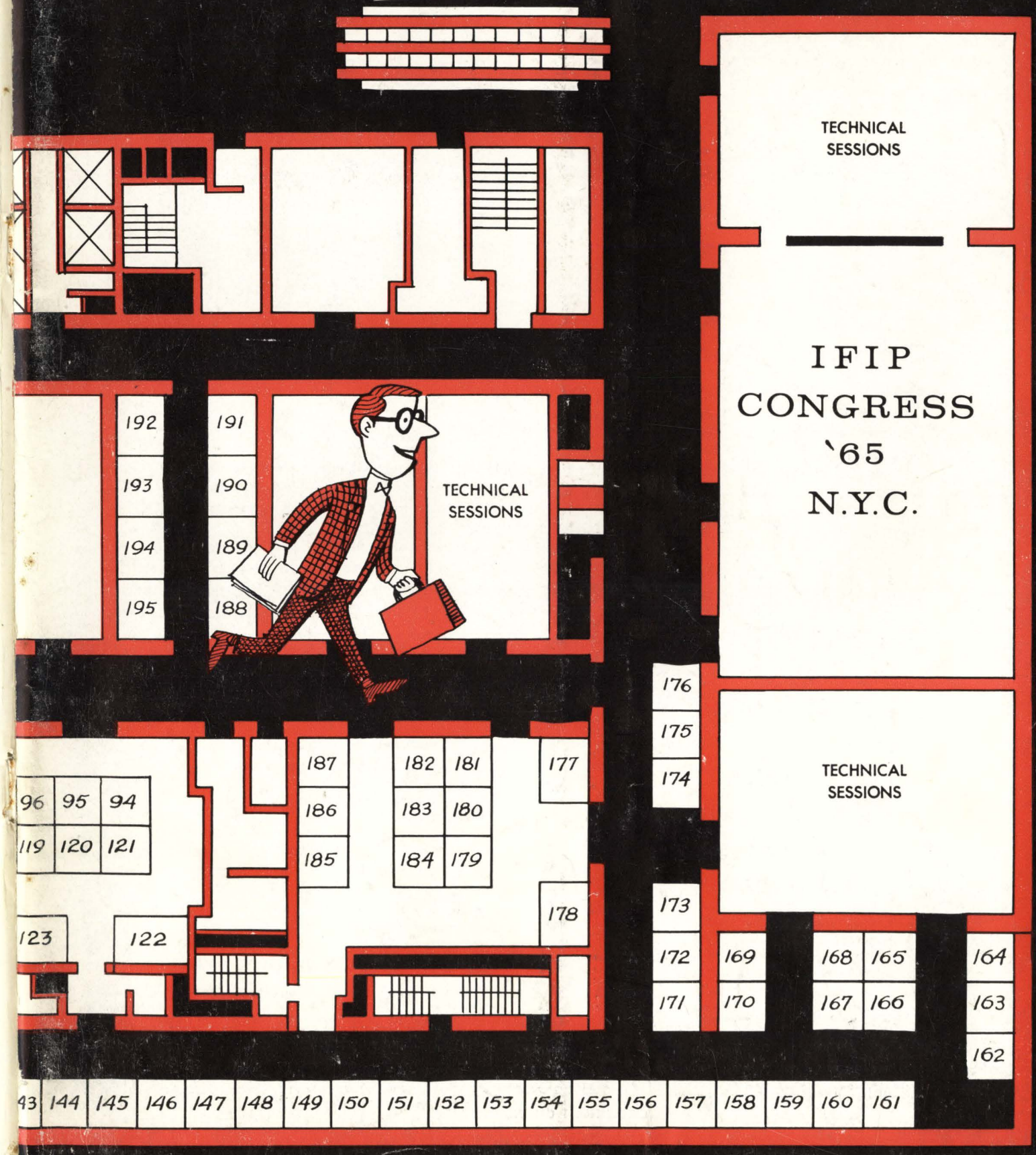
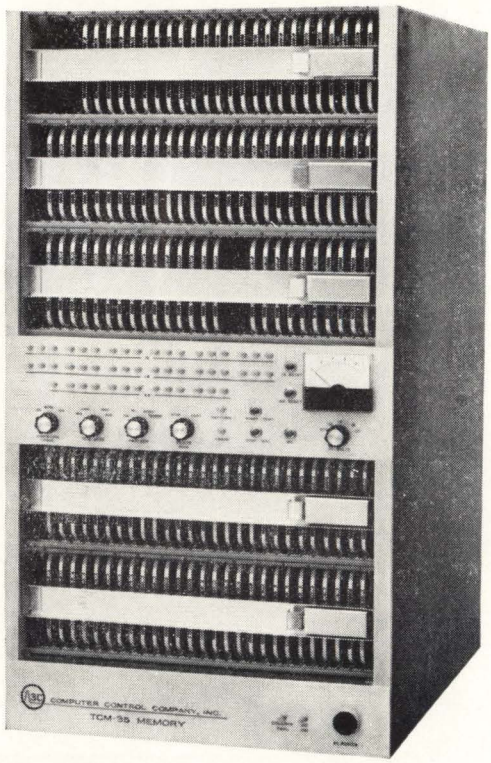
COMPUTER DESIGN

THE DESIGN AND APPLICATION OF ... UIPMENT & SYSTEMS

MAY 1965



1.4-2 μSEC
CORE MEMORY



General Purpose Front Access TCM-35

New TCM-35 family of coincident current core memories offers 1.4 to 2 μsec full cycle times, 1.2 μsec maximum half cycle time, and 0.75 μsec maximum access time. Capacities up to 8,192 words; word lengths to 36 bits. All silicon circuitry. Advanced system design. Extremely compact packaging. Low input power. System height is 24¼ inches to 35 inches, including self-contained power supply, depending upon storage capacity and options. TCM-35, like the 5 microsecond TCM-32, has pull-out, front-of-rack access. Operating temperature is from 0°C to +50°C with broad margins. 3C quality is built in. Modular design allows custom selection of desired performance and interface characteristics from an extensive list of standard options at volume production prices. Write for TCM-35 brochure (for 5 μsec memories, ask for TCM-32 brochure).

BASIC TCM-35 FEATURES*
Choice of Input/Output Logic Levels and Polarity

OPERATING MODES
Clear/Write
Read/Restore
Load
Unload
Read/Modify/Write

CONTROL INPUTS
Address Register Clear
Information Register Clear
Full Cycle/Half Cycle
Hold Address

CONTROL OUTPUTS
Memory Busy
Information Available
End of Cycle

NON-DESTRUCTIVE START-UP/SHUT-DOWN
BUILT-IN MARGINAL TEST
VOLTAGE FAILURE SENSING
BUILT-IN COOLING SYSTEM

* no extra cost

STANDARD OPTIONS**

INFORMATION REGISTER CONTROL
Shift Input
Count
Partition (up to 4 zones)

ADDRESS REGISTER CONTROL
Sequential
Sequential Up/Down
Sequential Interlace
Shift Input
Marker Pulses (up to 3)

DATA OUTPUT
Address Register

MEMORY CLEAR
MEMORY TESTER
VOLTMETER
REGISTER DISPLAYS
400 CPS POWER INPUT

** at extra cost

3C

3C DISTRICT SALES OFFICES: NEEDHAM, MASS.; SYRACUSE, N.Y.; COMMACK, L.I., N.Y.; LEVITTOWN, PA.; CLEVELAND, OHIO; SILVER SPRING, MD.; DES PLAINES, ILL.; ORLANDO, FLA.; ALBUQUERQUE, N.M.; PALO ALTO, CALIF.; LOS ANGELES, CALIF.; HOUSTON, TEX.; HUNTSVILLE, ALA.

COMPUTER CONTROL COMPANY, INC.
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Produces the most complete line of Optical Shaft-Angle Encoders

DIGISEC® Highest Accuracy Direct Reading Encoders . . . .

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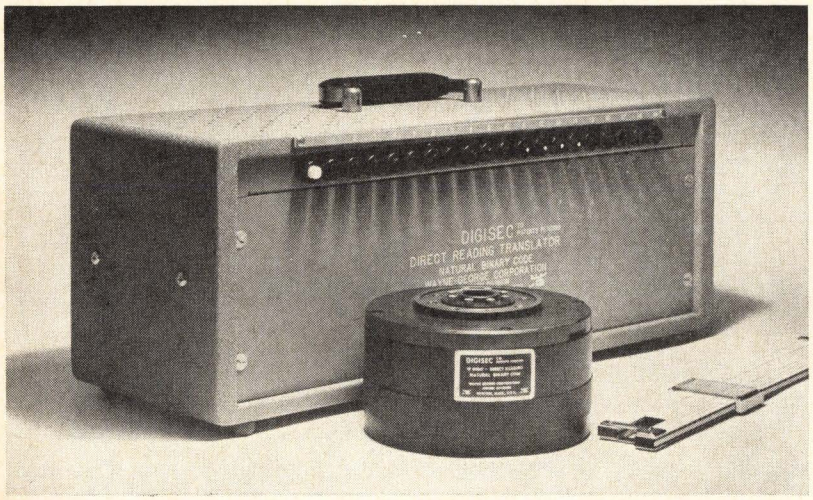

1 Arcsecond, Peak and Better

DIGISEC achieves highest accuracy in small case sizes with direct reading, continuous outputs — without code conversion, gears, brushes or reference rotor.

Optical Unit Diameter	Resolution
2.25″	to 40 arcseconds
3.5″	to 10 arcseconds
5.5″	to 2 arcseconds
10″	to 1 arcsecond

Outputs available in decimal or natural binary codes. Accuracy is ±1 quantum, peak. For example a 2^{20} DIGISEC provides resolution of 1.24 arcseconds and accuracy of ±1.24 arcseconds, peak. Complete system consists of Optical Unit and Translator containing electronics and display. The standard Translator weighs 15 lbs., is 6.5″ x 17″ x 7.5″, and can be miniaturized. Total input power for standard system is 30 watts. Bulletin 6310-1.

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CYCLIC CODE
2^{10} to 2^{15} Digits
Case Diameter: 3.5″
Bulletin 760-1C
(photo: RD-15)

CYCLIC CODE
2^{16} to 2^{17} Digits
Case Diameter: 10″
Bulletin 162-1
(photo: RD-17)

NATURAL BINARY
2^{5} to 2^{17} Digits
Case Diameters: 2.625″ to 10″
Bulletin 6302-2
(photo: NB-10)

DIGITAK® Incremental Encoders for rate measurement, angle counting, machine control, inertial platform systems — available with direction sensing and zero reset signal.

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Case Diameter: 1.437″
Bulletin 6212-1
(photo: RI-12M)

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2^{13} to 2^{15} Digits
Case Diameter: 3.5″
Bulletin 861-1C
(photo: RI-20K)

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(photo: RI-15S)

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CIRCLE NO. 2 ON INQUIRY CARD

MAY 1965 • VOLUME 4 • NUMBER 5

COMPUTER DESIGN

FOR ENGINEERING PERSONNEL RESPONSIBLE FOR THE DESIGN & APPLICATION OF DIGITAL CIRCUITS, EQUIPMENT, AND SYSTEMS IN COMPUTING, DATA PROCESSING, CONTROL AND COMMUNICATIONS.

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FEATURES

DEPARTMENTS

CALL YOUR WIFE...YOU'LL BE HOME LATE FOR DINNER!

Just read these "worst-case" specs on the new NAVCOR 1mc module line* and you'll want to revise the specifications on your new design. We realize that your wife won't appreciate your excuse for working late, but your new "brainchild" deserves the best...

And if you want to put the blame on someone . . . BLAME NAVCOR!

* **Input noise immunity of 2.5v at frequencies of 1mc to 5mc.**
- **True 1mc speed through the use of parallel logic.**
- **Parallel operation of 120 binary counter stages at 1mc clock rate . . . with all outputs settling within 150 nanoseconds after the count pulse.**
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- **Complete ground shielding and ringing clamps to cut backplane "debugging" expense.**

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CIRCLE NO. 3 ON INQUIRY CARD

Editorial Notes

THE IFIP CONGRESS 65

The international conference on the "information sciences," sponsored by the International Federation on Information Processing (IFIP), is shaping up to be a "must" event for engineers working on data processing and related equipment. The technical program is not only well-balanced in content but in form as well.

Covering just about every area of significant progress in the development of modern information processing systems, the program is divided into general and special sessions, symposia, and panel sessions. In general sessions, formal papers will view important research trends and examine the general state-of-the-art in information processing. Special sessions will consist of formal papers discussing in-depth important problems in specific areas. Shorter papers, with more time for informal discussion, will be presented in symposia and panel sessions.

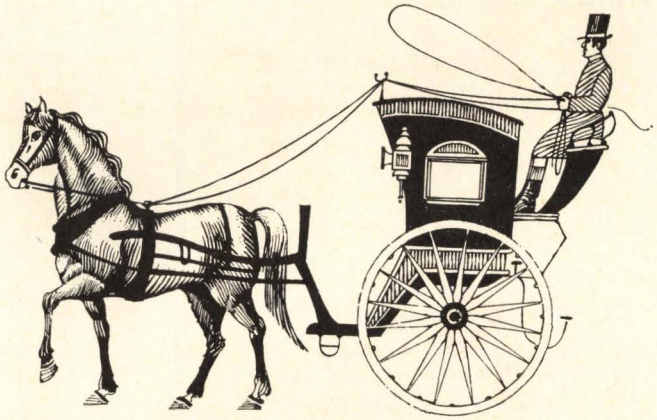
Many of the program participants are from outside the U.S. Thus, to some extent, the program offers the attendees a global picture of the state-of-the-art.

A partial listing of scheduled topics is presented in this issue.

Plan now to attend the conference; we will be there at our booth No. 226, drop in and see us.

S. Henry Sacks

Editor



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CIRCLE NO. 5 ON INQUIRY CARD

Letters to Editor

LOGIC SYMBOL STANDARDS

To the Editor:

I read the article "Designing Shift Counters" in your December issue and was disturbed by the non-conformance to the generally accepted logic symbol standard, MIL-STD-806 or the IEEE equivalent. I feel that technical periodicals must pioneer in the use of this standard to aid in the elimination of the existing variations in logic symbology.

Very truly yours,

Harry D. Young
R.C.A.
Defense Electronic Products
Moorestown, N.J.

Editor's Reply:

The IEEE logic symbol standard is the "American Standard Graphic Symbols for Logic Diagrams," approved by the American Standards Association on September 26, 1962. The task group which developed this standard was unable to agree upon a single standard, and thus two sets of symbols are presented, with no preference given between the two. Neither of these sets of symbols can presently be classified as "generally accepted," and there is apparently no technical periodical (including the IEEE Transactions on Electronic Computers) which adheres rigidly to either.

Extracts from the Standard are presented in the accompanying table; we invite our readers to comment generally upon this Standard, and the extent to which it is accepted in the industry.

PROPOSED ASA STANDARDS
GRAPHICAL SYMBOLS FOR LOGIC DIAGRAMS

3.4 States in Binary Logic — The two physical states on each terminal of each signal line shall be referred to as the 0-state and the 1-state. The 0-state may be called the reference (inactive, antifiducial) state, and the 1-state the significant (active, fiducial) state.

The above must not be construed as implying that the 1-state requires more power, contains more energy, or is at a higher potential than the 0-state. The state designations are purely arbitrary as far as the physical interpretation is concerned.

3.5 Kinds of Logic. If all signal line terminals in a logic diagram of a system or device have the same pair of physical states, and if both are electric potentials (currents), and if the more positive potential (current) is consistently selected as the 1-state, the resultant system, or device, is said to have positive logic.

If the less positive potential (current) is consistently selected as the 1-state, the resultant system, or device, is said to have negative logic.

4.1 Consider a circuit whose output (F) is a function of two variables (A, B), and whose output and input levels are capable of assuming only +2 volts and −3 volts. Assume that the circuit behaves according to the following table of combinations:

INPUTS		OUTPUT
A	B	F
−3v	−3v	−3v
−3v	+2v	−3v
+2v	−3v	−3v
+2v	+2v	+2v

4.1.1 In positive logic the −3v level is the 0-state and +2v is the 1-state (see paragraph 3.5). Substitution of the logic values for the voltage levels results in the following table:

INPUTS		OUTPUT
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

This is the truth table for the AND function. Therefore, the circuit is said to perform the AND operation.

4.1.2 In negative logic the −3v level is the 1-state and +2v is the 0-state (see paragraph 3.5). Substitution of the logic values for the voltage levels results in the following table:

INPUTS		OUTPUT
A	B	F
1	1	1
1	0	1
0	1	1
0	0	0

This is the truth table for the OR function. Therefore, the circuit is said to perform the OR operation.

4.3 Given a physical device characterized by a table of combinations, the logic function performed by the device is determined by the specified choices of the 1-states at its inputs and outputs.

Each choice of the 1-states at each input and each output of a logic circuit shall be specified on the detailed logic diagram in a manner that correctly represents the logic function designated by the logical designer.

4.4 In a diagram where positive logic, negative logic, or both is used, the state choices on the signal lines shall be identified as follows.

4.4.1 A small, open, right triangle at the point where a signal line joins a logic symbol indicates that the line's 1-state (activating) with respect to that logic symbol is the less positive potential.

4.4.2 A small, filled, right triangle at the point where a signal line joins a logic symbol indicates that the line's 1-state (activating) with respect to that logic symbol is the more positive potential.

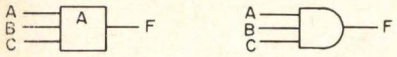
4.4.3 The right triangle shall be so oriented as to point in the direction of signal flow.

4.4.4 Either of the two kinds of right triangles, open or filled, may be omitted providing the convention is suitably noted on the diagram. In diagrams in which both kinds of right triangles would appear, only one kind may be omitted.

6.1 Use of Symbols — In the following listing of graphical symbols the Uniform Shape symbols are shown on the left and the Distinctive Shape symbols on the right. Logic diagrams must use symbols from one list or the other, not a mixture of the two. Symbols to be used on either list are shown in the center. The lines indicating input and output connections are not part of the symbol.

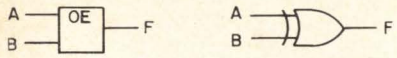
(Taken from AIEE No. 91 published by the American Institute of Electrical Engineers)

6.2.1 The output of an AND assumes the 1-state if and only if all of the inputs assume the 1-state. An example of the symbols for an AND with three inputs is:



6.3.1 The output of an OR assumes the 1-state if one or more of the inputs assume the 1-state. An example of the symbols for an OR with three inputs is:

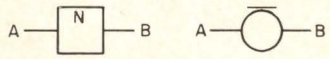
6.4.1 The output of an EXCLUSIVE OR with two inputs assumes the 1-state if one and only one input assumes the 1-state.



6.5.1 Symbol for LOGIC NEGATION ○

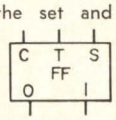
The output of a LOGIC NEGATION operation takes on the 1-state if and only if the input does not take on the 1-state. A small circle drawn at the point where a signal line joins a logic symbol indicates a LOGIC NEGATION.

6.5.3.1 The output of an ELECTRIC INVERTER assumes the 1-state if and only



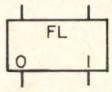
if the input assumes the 1-state. An example of the symbols for an ELECTRIC INVERTER is:

6.6.1 Flip-Flop Complementary — has outputs which are always of opposite states. This flip-flop has a third input, toggle (trigger) (T). The application of a 1-state signal to the toggle (T) input, or of simultaneous 1-state signals to the set and clear inputs, reverses the state of this flip-flop.



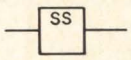
(The inputs are not required to be identified with S, T, and C, as shown.) The internal numbers, 1 and 0, are part of the symbol, and shall be in close proximity to their respective outputs. The set input shall be in proximity to the 1 output; the clear input shall be in proximity to the 0 output.

6.6.2 Flip-Flop Latch — has outputs which are not necessarily of opposite states. The application of simultaneous 1-state signals to the set and clear inputs causes both outputs to assume the same state for the duration of the inputs (both assume the 1-state or both assume the 0-state, depending upon the design of the circuit.

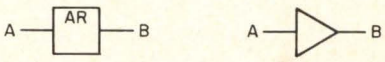


6.7 Single Shot — is activated by the indicated significant transition of the input signal. Output signal shape, amplitude, duration, and polarity are determined by the circuit characteristics of the SINGLE SHOT, not by the input signal.

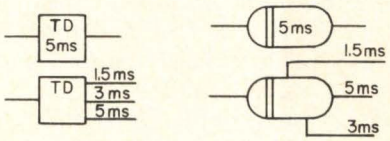
The normal (inactive) state of the SINGLE SHOT output is the 0-state. When activated, it changes to the indicated 1-state, remains there for the characteristic time of the device, and returns to the 0-state. The duration of the on time of the SINGLE SHOT will normally need to be included on a tagging line inside the symbol. When required, stylized waveforms indicating duration, amplitude, and rise and fall time may be used.



6.9.1 The output of an AMPLIFIER assumes the 1-state if and only if the input assumes the 1-state. An example of the symbols for an AMPLIFIER is:

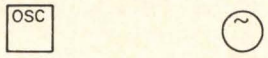


6.10 Symbol for Time Delay — the duration of the delay is included with the symbol. If the delay is tapped, the delay

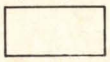


time with respect to the input shall be included adjacent to the tap output.

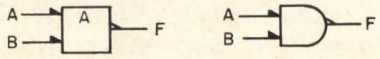
6.11 Symbol for OSCILLATOR



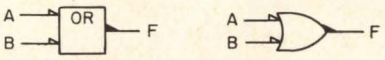
6.12 Symbol for functions not elsewhere specified. The symbol shall be adequately labeled to identify the function performed. It is not intended that this symbol be used for functions which can be logically expressed by a single symbol established in this Standard.



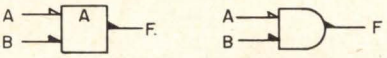
6.13 Relative Level Indicators below represent an AND with input 1-state at the more positive potential (current) level and an output with the 1-state at the less positive potential (current) level.



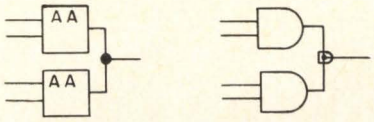
6.13.2 The symbols shown below represent the same device as paragraph 6.13. They depict an OR with input 1-state at the less positive potential (current) level and an output with the 1-state at the more positive potential (current) level.



6.13.4 The symbols shown below represent an AND with mixed inputs.



7.2 Use of Separate Circuits — Where circuits have the capability of being combined according to the AND (or OR) function, simply by having the outputs connected, that capability shall be shown by having an additiinal A (or OR) inside the Uniform Shape symbol. If needed for clarity, an additional A (or OR) shall be



added as a note adjacent to the connection (for the uniform shape). The Distinctive Shape symbol representation shall show this capability by enveloping the branched connection with a smaller sized AND or OR symbol.

INDUSTRY NEWS

THE AIR FORCE HAS ACCEPTED AND PLACED IN OPERATIONAL STATUS CONTROL DATA CORP.'S 3600 REAL-TIME COMPUTER SYSTEM (RTCS) for missile impact prediction and tracking on the Eastern Test Range. The computer system will furnish the range safety officer with instant information in regard to a missile's track, possible point of impact, and other missile flight data from launch to "burn out". On the basis of the visual presentation of the missile's flight pattern and other data, the range safety officer will be able to make a "go-or-destruct" decision vital both to range safety and to the investment in the missile system of many millions of dollars. The system also will aid materially in the recovery of missiles thousands of miles down range.

A SYSTEM FOR THE DIGITAL PROCESSING OF SEISMIC RECORDS HAS BEEN ORDERED BY A MAJOR OIL COMPANY from Advanced Scientific Instruments of Minneapolis. The system, using an ASI Advance Series 6040 computer and some special seismic-oriented "black boxes", will be used to convert, correct, and correlate seismic records. Because of the capabilities of the Advance 6040 and the special hardware and software seismic package, the system is said to offer digital seismic processing faster and at a purchase cost up to $120,000 less than currently available seismic data processing systems.

NASA'S MARSHALL SPACE FLIGHT CENTER HAS INSTALLED THREE GENERAL-PURPOSE PDP-5 COMPUTERS built by Digital Equipment Corp. The three computers and peripheral equipment form part of a ground-based testing complex for use in NASA's Saturn V program. The three PDP-5 computers will function as central control elements in an on-line data acquisition system in the center's Astrionics Laboratory. The system will test inertial components for the Saturn guidance system in a controlled laboratory environment.

THE NUMBER OF DIGITAL COMPUTER INSTALLATIONS IN EUROPE INCREASED NEARLY 50% DURING 1964 according to a comprehensive study just released by Computer Consultants Ltd., a leading European consulting firm. This remarkable increase, representing a jump from 3919 computers installed at the end of 1963 to 5889 computers installed at the end of 1964, makes Europe the most rapidly growing market for computer systems in the world today, according to the report. During this same period existing orders for computer systems also increased by nearly 50%, from 2335 to 3485 according to the "European Computer Survey in 1965." The leading computer user in Europe is Germany with 1413 systems installed. Second is France with 1084 computers installed, followed by Great Britain with 948, and Italy with 882, according to figures provided in the report.

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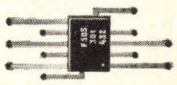
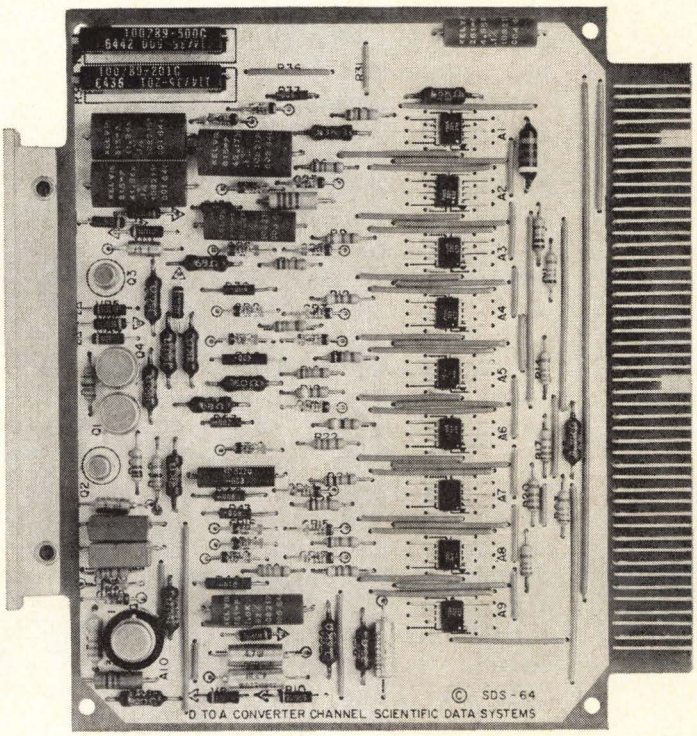


Get this Assembly Register Free



with this $395 D to A Converter

With an SDS D to A Converter, you get two registers per channel: A holding register like everybody else and an assembly register like only us. So what? So now, in addition to sequential conversion, you can simultaneously convert all of your system channels on demand. And it doesn't cost a penny more.

About the register shown above: You're right. It is an integrated circuit. All of our new analog system components utilize them to cram more reliability into less space. They also allow new systems set up flexibility (our 9-bit D to A, for example, is fully contained on a single card).

So add up our D to A converter advantages: both assembly and holding registers; integrated circuits; 5 microsecond speeds; 200 Kc conversion rates; 9, 12 and 15-bit models; off-the-shelf delivery of individual channels or complete multi-channel systems. You'd get more for your money even if our prices weren't so low.

May we send you a brand new brochure on our complete digital and analog component line?

SDS SCIENTIFIC DATA SYSTEMS
1649 Seventeenth Street, Santa Monica, Calif.

Sales offices in: Santa Monica, New York City, Boston, Washington, D.C., Philadelphia, Pittsburgh, Wilmington, Houston, Huntsville, Orlando, Dallas, Chicago, Detroit, Albuquerque, Denver, San Francisco, San Diego, Seattle. Foreign representatives: CECIS, Paris, France, Geneva, Switzerland; Kanematsu, Tokyo, Japan; RACAL, Sydney, Australia; Instronics, Ltd., Stittsville, Ontario, Canada.

CIRCLE NO. 6 ON INQUIRY CARD

INDUSTRY NEWS

NATIONAL CASH REGISTER, IN RETURN FOR THE USE OF CERTAIN PATENTS, has paid Navigation Computer Corp. a fixed amount of cash, plus an advance on royalties which will be paid over the five year span of the agreement. J. Paul Jones, president of Navigation Computer Corp. (NAVCOR) pointed out that NCR's exclusive rights to manufacture and sell the patented special input-output equipment are in the business machine field. The patents include an all electronic coding keyboard which has no mechanical levers or parts, high-speed printing techniques, and methods for simplified printing directly on punched paper tape. Additional patents cover tape perforation and simplified spool servo systems. Mr. Jones also stressed that one of the most important considerations in the signing of the agreement was that the International Service Organization of NCR will be equipped to service all machines, whether they are sold directly through NCR sales or through NAVCOR.

THE CONTROL SYSTEMS DIVISION OF RADIATION INC. AND DATA SYSTEMS, INC. WILL PURSUE MARKETING OPPORTUNITIES IN THE AUTOMATION OF CHEMICAL PROCESSING PLANTS, according to a recent agreement signed by the two companies. Data Systems, Inc., a subsidiary of Union Carbide Corporation, will provide a series of modern, high-speed, digital computers for chemical process control. Radiation Inc. will furnish data acquisition and signal conditioning products.

COMPUTER CONTROL COMPANY, INC., HAS RECEIVED AN ORDER FROM SANDERS ASSOCIATES, INC., FOR SEVEN DDP-224 GENERAL PURPOSE DIGITAL COMPUTERS in a contract totaling over one million dollars. The DDP-24's will be the digital computer portion of seven Saturn V operational display systems Sanders is building for NASA. The DDP-224's will collect data, format information, and distribute critical booster measurements to associated displays, thereby enabling personnel to evaluate the Saturn V vehicle's operational performance.

SYLVANIA ELECTRONIC SYSTEMS HAS INSTALLED A CONTROL DATA 3200 COMPUTER SYSTEM FOR ITS WESTERN OPERATION AT MOUNTAIN VIEW, Cal. The 3200 computer system is used to acquire, process, reduce and analyze real-time data, as well as a scientific processor for engineering applications. The 3200 accepts information from a five-stage, 24-bit, cascaded buffer built by Sylvania and attached to the 3207 Data Channel. Sylvania engineers estimate that this buffer will accept 24-bit words at burst rates up to 5 million words per second. In addition to the five-stage cascaded buffer, Sylvania engineers have attached to the data buss a register to allow 15 bits of information to be sent in or out of the computer in one computer cycle. This data buss register extension provides a means of communication between special input/output equipment and the computer. With the addition of these two devices, Sylvania has extended the over-all system capability in accepting and analyzing the high rate real-time input data.

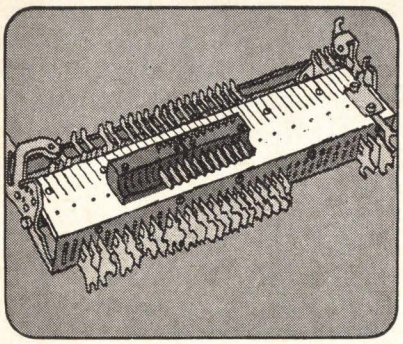
DATA COMMUNICATIONS

equipment for on-line, real-time processing

stunt box...your communication's girl friday*

An important component of all Teletype Model 35 page printers and automatic send-receive sets is the stunt box. This is an automatic switching device which performs remote control functions usually expected only of larger, costlier, and more complex equipment.

The stunt box handles anything that can be electrically controlled—ranging from performing such non-typing functions as automatic carriage return and horizontal tabulation . . . to activating remote apparatus, including tape punches and readers, business machines, and computers.



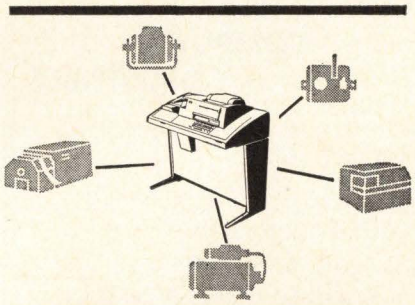
Basically, the stunt box does three things—mechanically initiates internal functions, electrically controls internal functions, and electrically controls external equipment.

STATION CALLER

Remote stations can be selectively called through the stunt box. Thus, one station can call others simultaneously, individually, or in predetermined groups. In this way, specific information can be selectively directed only to the stations specifically concerned with the information being transmitted. For example: an operator types out a sales order on a Teletype Model 35 page printer. Such information as the order number is received by all departments, while cost information is directed by the stunt box only to accounting, billing, and management departments.

AUTOMATIC BACK TALK

Teletype Model 35 sets can be equipped with an answer-back drum, which stores up to 20 characters. In on-line uses, the stunt box at a remote unattended station can trigger the answer-back mechanism so that the station automatically returns its identification call letters to the sending station.



The stunt box can activate the mechanism that automatically feeds the information needed to program a computer so that it can accept the input data which follows.

The versatility that the stunt box gives to Teletype Model 35 page printers and automatic send-receive sets is another reason why they are made for the Bell System and others who require the most reliable communications equipment at the lowest possible cost. For more detailed information on the real-time uses of Teletype equipment, write to: Teletype Corporation, Dept. 71E, 5555 Touhy Avenue, Skokie, Illinois 60078.

*This device is used in Teletype machines to perform non-printing functions such as carriage return, line feed, etc.

machines that make data move

TELETYPE

CIRCLE NO. 8 ON INQUIRY CARD

INDUSTRY NEWS

A "DO-IT-YOURSELF" COMPUTER SERVICE THAT ALLOWS CUSTOMERS TO DRIVE IN AND PROCESS INFORMATION MUCH AS A HOUSEWIFE DRIVES TO A LAUNDROMAT was inaugurated recently in Chicago. Originated by Statistical Tabulating Corp., the unusual service, which is called Data-Mat, permits a customer to bring unprocessed data to a mid-town center, obtain free parking, and the use of a private office to sort and prepare information, and perform all necessary computations on any of four computer systems, including a new, high-speed system — just as if he were using one of a battery of washing machines. Like a laundromat, cost of the service is based upon the number of hours the computer equipment is used. The center — located in modern quarters at 2 North Riverside Plaza — is open around-the-clock, seven days a week. Attendants are available at all times to assist customers. Prices for the new service start at $20 an hour. Scheduled time is sold on a guaranteed basis, and customers may contract for as little as three hours a month.

FOR THE DEVELOPMENT OF A COMPUTER-BASED INFORMATION PROCESSING AND RETRIEVAL SYSTEM, System Development Corp. has been awarded an $85,000 contract by the Job Corps' Office of Program Development and Analysis, Washington, D.C. SDC scientists and information processing technicians will adapt existing computer programs — originally designed for and currently in use by military organizations — to allow Job Corps' personnel to accumulate, organize, retrieve and analyze information relative to the Job Corps' program. The information system will serve the early needs of the Job Corps' program and will be able to accommodate changes in the Corps' size, organization, functions, problems, relationship with other organizations, and other aspects of the program.

WHAT HAS BEEN TERMED THE STEEL INDUSTRY'S FIRST COMPUTERIZED OPERATOR GUIDE CONTROL FOR ELECTRIC FURNACE STEELMAKING has been put into operation at Lukens Steel Co. in Coatesville, Pa. W. E. Mullestein, Lukens vice-president and general manager, said, "We are using computer equipment now to guide production of carbon steels in the company's two electric furnaces, while developing programs for alloy steels and improving existing programs. Results during two months of operation convince us we can anticipate achieving all goals set for the equipment." The IBM Operator Guide Control System doesn't activate any portion of the furnace facility. Instead, it issues guide instructions for furnace operators to follow during the steelmaking processes. This feature of the equipment emphasizes the continued responsibility of the operator for production results. In addition to information fed to the computer through manual entry units, precisely detailed process information concerning such things as a temperature of the molten steel in the furnace, oxygen injection, pressure in the furnace, power input, etc., is picked up automatically by instrument sensors wired to the computer.

DATA COMMUNICATIONS

equipment for on-line, real-time processing

the shift-less keyboard that isn't!

Shifting between letters and numbers is no longer necessary as a result of the new 4-row keyboard on Teletype Models 33 and 35 page printers and automatic send-receive sets. However, when used in real-time data communications, these machines are anything but shiftless on the job.

"COMPUTER" SPOKEN HERE

Operating on the same permutation code approved by the American Standards Association for information interchange, this Teletype equipment can communicate with most business machines and computers. It is being used as input/output terminal gear in such applications as communications between branch offices and a centralized computer, making a data processing center available to all company offices.

machines that make data move

b_7 →	0	0	0	0	1	1	1	1
b_6 →	0	0	1	1	0	0	1	1
b_5 →	0	1	0	1	0	1	0	1
b_4 b_3 b_2 b_1 ↓								
0 0 0 0	NULL	DC_0	b	0	@	P		
0 0 0 1	SOM	DC_1	!	1	A	Q		
0 0 1 0	EOA	DC_2	"	2	B	R		
0 0 1 1	EOM	DC_3	#	3	C	S		
0 1 0 0	EOT	DC_4 (STOP)	$	4	D	T		
0 1 0 1	WRU	ERR	%	5	E	U		
0 1 1 0	RU	SYNC	&	6	F	V		
0 1 1 1	BELL	LEM	' (APOS)	7	G	W		
1 0 0 0	FE_0	S_0	(	8	H	X		
1 0 0 1	HT/SK	S_1	)	9	I	Y		
1 0 1 0	LF	S_2	*	:	J	Z		
1 0 1 1	V_{TAB}	S_3	+	;	K	[		
1 1 0 0	FF	S_4	, (COMMA)	<	L	\		ACK
1 1 0 1	CR	S_5	—	=	M	]		ⓘ
1 1 1 0	SO	S_6	.	>	N	↑		ESC
1 1 1 1	SI	S_7	/	?	O	←		DEL

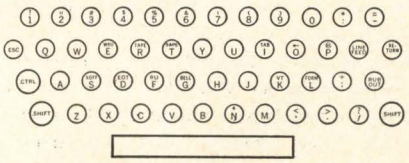
UNASSIGNED

UNASSIGNED

The American Standard Code is composed of eight columns of 16 characters each. Control characters, found in the first two columns, include those required for the control of terminal devices, input and output devices, format, or transmission and switching operations. Common punctuation symbols are found in the third column, numbers in the fourth, and the alphabet in the fifth and sixth columns. The final columns are reserved for future standardizations. Teletype Models 33 and 35 sets generate an even parity in the eighth level.

PRINTS ON BUSINESS FORMS

Any business form, such as invoices, payroll checks, sales orders, freight records, and reservations, can be typed on these Teletype sets and transmitted directly to various departments. This minimizes recopying errors. The 4-row keyboard further reduces the possibility of errors, because it isn't necessary to shift when typing numbers. Notice the similarity to a regular typewriter keyboard, which is why any typist can easily learn to use these new machines.



VERSATILITY PLUS

Added to the versatility of the 4-row keyboard is the complete reliability and economy of Teletype equipment. It's built to last, with pneumatic shock absorbers, nylon pulleys and gears, and all-steel clutches that keep maintenance down to a bare minimum. And, these sets are surprisingly low in cost.

That's why Teletype Models 33 and 35 page printers and automatic send-receive sets are made for the Bell System and others who insist on the most reliable communications equipment at the lowest possible cost. For more details on the capabilities of the Teletype 4-row keyboard in real-time data communications, write to: Teletype Corporation, Dept. 71E, 5555 Touhy Avenue, Skokie, Illinois 60078.

TELETYPE®

CIRCLE NO. 9 ON INQUIRY CARD

GOVERNMENT REPORTS ★ ★

PROPAGATION-LIMITED COMPUTER NETWORKS

The assumption of significant and indeterminate signal propagation delay between logic blocks in a computer system introduces uncertainties in the timing of logical operations. This condition sets limits to computation speed independently of the speed of the switching elements. Such uncertainties require careful design of timing and physical layout so as not to cause excessive loss in operation speed. The anti-parallel scheme, a new mode of coupling, has been developed. In this scheme the loss of a control pulse due to the accumulation of delay variations results only in the introduction of spaces into a symbol stream.

Order from the Office of Technical Services, U.S. Dept. of Commerce, Washington, D.C. 20230. Order No. AD603165N. Price: $4.00.

INFORMATION SYSTEMS SUMMARIES

Second edition prepared by the Office of Naval Research covers general information sciences, machine interaction with humans, and improved machines. The ONR report represents an effort to acquaint interested personnel with their Information Systems Branch program and with a sampling of current significant research in the information sciences. Three distinct classes of interest exist, each having its own requirements. Development and engineering personnel need new ideas and techniques to solve their technical problems or to suggest new approaches. Members of the scientific community need detailed knowledge of both new research findings and also new research tools and techniques. And R&D management personnel need current and projected status information on the state of technology and the cost in time, dollars, and manpower of pushing it forward. ONR aims its report at each of these classes who have a need-to-know.

Order from the Office of Technical Services, U.S. Dept. of Commerce, Springfield, Va. 22151. AD606772N. Price: $3.00.

VARIABLE DISPLAY SYSTEM

With a light pen and an electronic display linked to a central computer, a user may perform tasks on-line that are usually done off-line with card sorting and reproduction machinery, electronic engineers report. A new variable display system drastically shortens response time and enables changing part or all of the stored information. The system will accommodate any set of tabular data arranged in proper format and placed on magnetic tape. Tabular data may be retrieved from up to 59,000 categories and manipulated on the display by application of the light pen to the surface of the cathode-ray tube. Data may be added, modified and deleted, rows sorted, columns added, columns and rows exchanged, deleted and compressed. Users require only a few minutes of training and practice to gain speed and confidence.

Order from the Office of Technical Service, U.S. Dept. of Commerce, Springfield, Va. 22151. AD 606179N. Price: $1.00.

MICROMINIATURE PROGRAMMABLE LOGIC ELEMENTS

A microminiaturized, highly repetitive logic structure is feasible where microprogramming of elements individually or in groups is a characteristic of the structure. Air Force-sponsored researchers demonstrated feasibility in the successful miniaturization of the digital section of a pattern recognition system which they designated "Parapropagation Pattern Classifier." Major difficulties were encountered in obtaining isolation in homogeneous silicon wafers, but the researchers developed a promising isolation process and indicate process variations as well as results through following the recommended procedure.

Order from Clearinghouse, U.S. Dept. of Commerce, Springfield, Va. 22151. AD608525N. Price: $3.00.

SOVIET TRANSLATION ON MANUFACTURE OF COMPUTERS

Report discusses overall planning and certain organizational and technical measures recommended for securing reliability. The author indicates that controllability of the manufacturing process at all stages is the basis for obtaining specified reliability. For each manufacturing process and operation, tolerances must be set, that is, limits of errors within which the item produced is considered to be sound.

Order from Clearinghouse, U.S. Dept. of Commerce, Springfield, Va. 22151. TT-64-41944N. Price: $3.00.

FJCC 1965
Call for Papers

The call for papers for the 1965 Fall Joint Computer Conference, to be held November 30-December 2 in Las Vegas, Nevada, has been issued by S. Nissim and T. B. Steel, Jr., co-chairmen of the technical program committee. No restrictions are placed on subject matter for the papers. In addition to state-of-the-art surveys and original research and development reports in the traditional areas of hardware and software, contributions emphasizing the design, selection, installation and management of information processing systems are invited.

Notification of intention to submit a paper is requested. Deadline for full papers is June 15. One complete draft copy, together with a 150-word abstract, should be sent to:

Mr. Robert Gray, Secretary, Program Committee, 1965 FJCC; P.O. Box 49, Santa Monica, Cal.

DATA COMMUNICATIONS

equipment for on-line, real-time processing

put punch in your communications...with paper tape

The continuous evolution of data processing systems has brought new uses for punched paper tape. In fact, paper tape has become an important communications link, and is still the most inexpensive and reliable continuous recording medium available.

Paper tape is easy to handle and accommodates data of any length. In addition, Teletype paper tape units can transmit most recognized codes, including the permutation code approved by the American Standards Association for information interchange. This makes Teletype sets capable of communicating directly with business machines and computers.

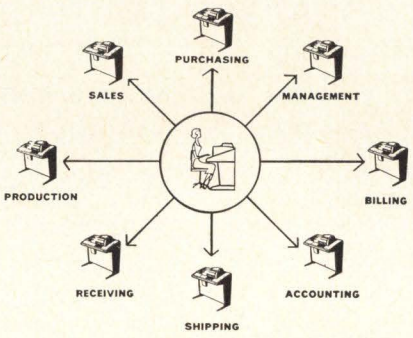
COLLECTION AGENT

Teletype punched paper tape units are versatile, flexible, and capable of collecting and distributing data from a large number of machines and transmitting to computers at high speeds. There is a paper tape unit for every need—from 60 to 2000 wpm.

Many business operations have been improved through the use of Teletype punched paper tape equipment within integrated data processing systems. This list includes: order entry, shipping, and invoicing for the accounts receivable procedure; production control; payroll computation; banking operations, insurance processes, etc. An important advantage of punched paper tape is that it can store fixed information, such as customers' names and addresses, which can be used over and over again to save retyping.

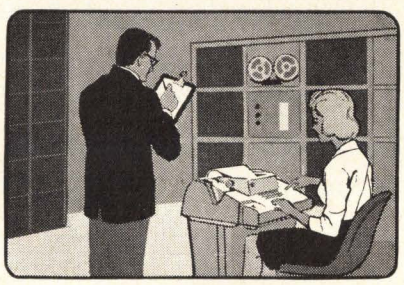
INDEPENDENT OPERATOR

On the Teletype Model 35 ASR (automatic send-receive) set, the tape punch and reader can operate independently of the page printer. Thus, messages can be received by the page printer, while the operator is preparing a tape for later transmission. This independent operation also means the keyboard can be used to prepare one tape, while the tape reader transmits the message of another tape.



VOICE OF A COMPUTER

Applications of Teletype equipment as input/output terminals for computers and other business machines are numerous. For example: a national insurance company has demonstrated a system that will link a large multiprocessing computer with more than 900 district offices. Teletype Model 33 ASR sets will be used in this system to print out premium information from the district offices, and as tape output equipment for a centralized computer in order to update all premium transactions.

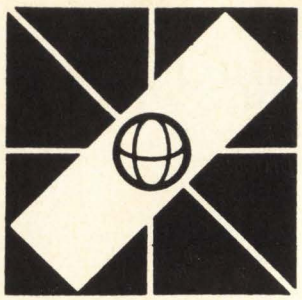


This is another indication why these Teletype paper tape units and automatic send-receive sets are made for the Bell System and others who insist on the most reliable communications equipment at the lowest possible cost. To find out more on how they can be an important part in your data processing systems, write to: Teletype Corporation, Dept. 71E, 5555 Touhy Avenue, Skokie, Illinois 60078.

machines that make data move

TELETYPE®

CIRCLE NO. 10 ON INQUIRY CARD



IFIP CONGRESS 65

INTERNATIONAL CONFERENCE ON INFORMATION PROCESSING

NEW YORK HILTON · MAY 24-29, 1965

Combined with an exciting technical program, the largest international exposition of information processing equipment will convene at the New York Hilton on May 24, 1965. More than 15,000 people from 50 countries are expected at the show.

The formal program will run from May 24 through May 29; the exhibition, called Interdata 65, will be open from May 24 through May 27. A number of special events will be held during and after the week as part of the total official activity of the Congress.

The first Congress of this type was held in Paris in 1959 and at that meeting the International Federation for Information Processing (IFIP) was born. Its formation was subsequently ratified by the national societies of 13 countries. By 1962, when IFIP Congress 62 was held in Munich, IFIP had become a 20-nation federation. Today IFIP represents professional societies of 23 member countries. Because the triennial meeting is being held in the United States, the American Federation of Information Processing Societies (AFIPS) has cancelled its own national meeting (The Spring Joint Computer Conference) so that its members may act as U. S. hosts and participate in the Congress.

The technical program will provide a comprehensive view of significant progress in techniques and development in the information sciences. Formal papers will be presented in general and special sessions. Shorter papers with more time for informal discussion will be presented in symposia and panel sessions. The opening and closing sessions, on May 24 and 29, will be single plenary sessions. Other sessions will run in parallel. The schedule presented here represents only a partial listing of proposed topics; the complete program will be available at the Congress registration booth.

TECHNICAL PROGRAM

MONDAY, MAY 24

A1 GENERAL SESSION 10:00 AM–GRAND BALLROOM
OPENING SESSION

Chairman: W. R. Lonergan, Congress Vice Chairman

WELCOME:
I. L. Auerbach, **IFIP President**

THE TECHNICAL PROGRAM:
B. Langefors, **Program Chairman**

THE CONGRESS:
W. Buchholz, **Congress Chairman**

KEYNOTE SPEECH:
(Speaker to be announced)

B1 GENERAL SESSION . . . 2:00 PM–EAST BALLROOM
ORGANIZATION
OF LARGE STORAGE SYSTEMS — I

Chairman: J. A. Postley (USA)
Vice Chairman: H. D. Huskey (USA)

HANDLING OF VERY LARGE PROGRAMS
M. N. Perry (USA)

ADVANCED CONCEPTS OF UTILIZATION OF MASS STORAGE
C. B. Poland (USA)

CONSIDERATIONS ON RANDOM AND SEQUENTIAL ARRANGEMENTS OF LARGE NUMBERS OF RECORDS
A. I. Dumey (USA)

B2 SPECIAL SESSION . . . . 2:00 PM–WEST BALLROOM
MATHEMATICAL METHODS OF OPTIMIZATION

Chairman: H. W. Kuhn (USA)

SEMIGROUP THEORY AND CONTROL THEORY
A. V. Balakrishnan (USA)

SEQUENTIAL OPTIMIZATION ALGORITHMS AND THEIR APPLICATIONS
V. S. Mikhalevitch (USSR)

OPTIMIZATION IN OPERATIONS RESEARCH
G. B. Dantzig (USA)

B3 SYMPOSIUM . . . . . 2:00 PM–BALLROOM FOYER
GENERAL PURPOSE PROGRAMMING LANGUAGES

Chairman: A. van Wijngaarden (Netherlands)

RECENT DEVELOPMENTS IN THE CONSTRUCTION OF A NEW ALGOL
W. L. Van der Poel (Netherlands)

A GENERALIZATION OF ALGOL AND ITS FORMAL DESCRIPTION
N. Wirth and H. Weber (USA)

SYNALGOL — AN ALGORITHMIC LANGUAGE CAPABLE OF GROWING
H. J. Hauer (USA)

DAJA — A PROPOSED LANGUAGE FOR DATA PROCESSING
J. Vlcek, E. Outrata, and E. Kindler (Czechoslovakia)

RECENT APPLICATIONS OF A UNIVERSAL PROGRAMMING LANGUAGE
K. Iverson (USA)

SPECIAL EVENTS

Participants in IFIP Congress 65 and especially their wives are invited to enjoy a number of special events being planned:

- IFIP-UNITED NATIONS EVENING
- PRINCETON TOUR AND COMMUNITY THEATER
- IFIP BANQUET
- INFORMATION SCIENCES DAY AT THE WORLD'S FAIR
- MAJOR BROADWAY MUSICAL
- CONCERT
- SPORTS NIGHT
- SUNDAY OUTING (All day MAY 30)
- DAYTIME TRIPS

IFIP PEOPLE-TO-PEOPLE PROGRAM

To encourage an informal exchange of technical information on an individual basis, as well as to provide a more personal look at life in the USA and Canada, visitors to IFIP Congress 65, from outside North America, will be put in touch with hosts from a wide geographic area. Questionnaires for visitors residing in IFIP member countries are available from the national information processing societies. Other visitors, and those desiring to be hosts in the USA and Canada, can obtain questionnaires from the People-to-People Program, IFIP Congress Office, 345 East 47th Street, New York, N.Y. 10017.

REGISTRATION

Registration Fee: By April 1, 1965 . . $25
At Congress $35
Wife (or husband) . Free

Each registrant will receive a two-volume conference proceedings at no charge.

For registration forms write:

IFIP CONGRESS 65
345 East 47th St. (at UN Plaza)
New York, N.Y. 10017

IFIP Congress 65 (Continued)

B4 SYMPOSIUM. . . . .2:00 PM–TRIANON BALLROOM
PARALLEL AND CONCURRENT COMPUTER SYSTEMS

Chairman: D. L. Slotnick (USA)

THE SOLOMON II COMPUTING SYSTEM
A. B. Carroll, J. G. Gregory, W. H. Leonard, and D. L. Slotnick (USA)

A REAL TIME MULTI-COMPUTER SYSTEM FOR TRAIN SEAT RESERVATION
M. Hosaka and T. Tani (Japan)

A METHOD FOR THE SIMULTANEOUS PROCESSING OF SEVERAL PROGRAMS
W. Rekowski and K. Leipold (Germany)

LARGE PARALLEL COMPUTERS
J. Schwartz (USA)

AN APPROACH TO PARALLEL COMPUTING
J. H. Pomerene (USA)

ORGANIZATION OF MULTIPROCESSING BY HARDWARE
J. Oblonsky (Czechoslovakia)

B5 SYMPOSIUM. . . . . .2:00 PM–LE PETIT TRIANON
MECHANIZATION OF THEOREM PROVING

Chairman: J. A. Robinson (USA)

A MULTIPURPOSE THEOREM-PROVING HEURISTIC PROGRAM THAT LEARNS
J. R. Slagle (USA)

REALIZATION OF A PROGRAM WHICH CHOOSES THE THEOREMS IT PROVES
J. Pitrat (France)

A SOLUTION TO THE TRANSLATION PROBLEM AND THE IMPORTANCE OF THE SET OF SUPPORT STRATEGY IN THEOREM PROVING
L. T. Wos, G. A. Robinson, and D. Carson (USA)

ASPECTS OF MECHANICAL THEOREM PROVING
M. Davis (USA)

COMPUTER REALIZATION OF A DECISION PROCEDURE IN LOGIC
Joyce Friedman (USA)

B6 SYMPOSIUM. . . . .2:00 PM–MERCURY BALLROOM
PATTERN RECOGNITION AND SELF-ORGANIZING SYSTEMS — I

Chairman: G. S. Sebestyen (USA)

ISODATA — A SELF-ORGANIZING COMPUTER PROGRAM FOR DESIGN OF PATTERN RECOGNITION PREPROCESSING
G. H. Ball and D. J. Ball (USA)

ADAPTIVE PATTERN RECOGNIZERS SYNTHESIZED WITH WIENER CANONICAL FORMS
D. B. Brick (USA)

AN ITERATIVE REALIZATION OF ADAPTIVE PATTERN RECOGNITION NETWORKS
K. Fukunaga and T. Ito (Japan)

LEARNING ALGORITHMS FOR SEQUENTIAL DECISION GRAPHS
M. Nadler (France)

LANGUAGE LEARNING, CONTINUOUS PATTERN RECOGNITION, AND CLASS FORMATION
L. Uhr (USA)

TUESDAY, MAY 25

C1 SPECIAL SESSION. . . .9:00 AM–EAST BALLROOM
THE FUTURE OF SWITCHING ELEMENTS

Chairman: J. R. Pasta (USA)

THE INFLUENCE OF COMPUTER DESIGN ON SEMICONDUCTORS
S. L. H. Clarke (UK)

CRYOGENICS — ACHIEVEMENT AND POTENTIAL
V. L. Newhouse (USA)

ELECTRO-OPTICAL INFORMATION PROCESSING
W. J. Poppelbaum (USA)

C2 SPECIAL SESSION. . . .9:00 AM–WEST BALLROOM
PARTIAL DIFFERENTIAL EQUATIONS

Chairman: A. A. Dorodynicyn (USSR)
Vice Chairman: A. Ghizzetti (Italy)

ON USE OF MODIFIED SUCCESSIVE OVERRELAXATION METHOD WITH SEVERAL RELAXATION FACTORS
D. M. Young, Jr., Mary F. Wheeler, and J. A. Downing (USA)

SOME UNUSUAL PROBLEMS IN NUMERICAL ANALYSIS
S. V. Parter (USA)

ESTIMATIONS IN NONLINEAR EQUATIONS
J. Schroeder (Germany)

C3 SYMPOSIUM. . . . . .9:00 AM–BALLROOM FOYER
METHODS FOR DESCRIBING INFORMATION SYSTEMS

Chairman: M. M. Pacelli (Italy)
Organizer: L. A. Lombardi (Italy)

NON-PROCEDURAL FILE PROCESSING: A PROCEDURE GENERATOR
M. M. Pacelli and G. M. Palermo (Italy)

THE REPRESENTATION OF STRUCTURED INFORMATION
G. Salton (USA)

A GENERAL PURPOSE SYSTEM FOR THE STRUCTURING ON-LINE OF INFORMATION AND DECISION PROCESSES
M. Greenberger (USA)

NOTATION, INSIGHT, AND PROBLEM DEFINITION METHODS
M. S. Montalbano (USA)

ON THE REPRESENTATION OF LOGIC BLOCKS AND THEIR INTERCONNECTION IN SEQUENTIAL SWITCHING CIRCUITS
H. Goerling (Germany)

SYSTEMS ANALYSIS IN AN ECONOMIC MANAGEMENT AUTOMATION PROJECT
J. Vlcek (Czechoslovakia)

C4 SYMPOSIUM. . . .9:00 AM–TRIANON BALLROOM
REQUIREMENTS AND PROSPECTS FOR COMMERCIAL PROGRAMMING

Chairman: J. A. Gosden (USA)

THE GRADUAL ACCEPTANCE OF A VARIETY OF COMMERCIAL ENGLISH LANGUAGES
R. M. Paine (UK)

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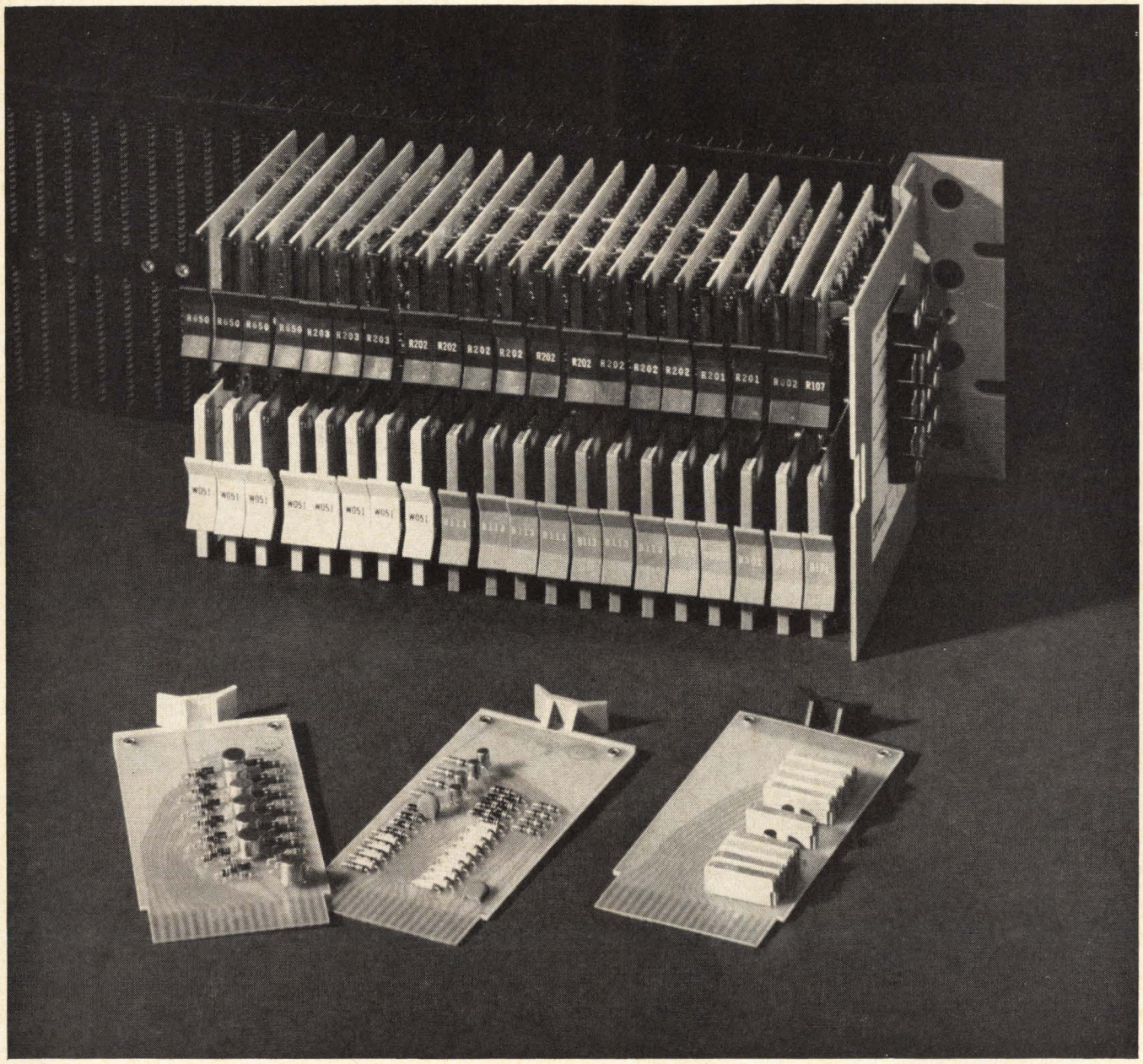

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CIRCLE NO. 11 ON INQUIRY CARD

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2N 3793 2N 3794	**Medium Power NPN** Silicon Transistors	2N 2219 2N 2222 2N 697 2N 1613	2N 1302 2N 1304 2N 1306 2N 1308	.42

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CIRCLE NO. 12 ON INQUIRY CARD

IFIP Congress 65 (Continued)

USA ACTIVITY IN CONVENTIONAL COMMERCIAL LANGUAGES
H. Bromberg (USA)

FURTHER USA ACTIVITY AFFECTING COMMERCIAL PROGRAMMING LANGUAGES
C. J. Shaw (USA)

C5 SYMPOSIUM.....9:00 AM–LE PETIT TRIANON
PATTERN RECOGNITION DEVICES

Chairman: B. H. McCormick (USA)

STAR — A MACHINE TO RECOGNIZE SPOKEN WORDS
D. R. Hill (UK)

AN ASYNCHRONOUS CHARACTER RECOGNITION SYSTEM AND DEVICE
T. Sakai, M. Nagao, K. Nagamori, S. Sekiguchi, and K. Kiji (Japan)

ILLIAC III: A PROCESSOR OF VISUAL INFORMATION
B. H. McCormick (USA)

A PATTERN RECOGNITION FACILITY WITH A COMPUTER-CONTROLLED LEARNING MACHINE
J. H. Munson, A. E. Brain, G. E. Forsen, D. J. Hall, N. J. Nilsson, and C. A. Rosen (USA)

C7 PANEL.....9:00 AM–MERCURY ROTUNDA
TRENDS IN COMPUTER LOGIC FOR NON-ARITHMETIC PROCESSORS

Chairman: J. P. Anderson (USA)
Panel Members: A. R. Barnum (USA), R. S. Barton (USA), and J. Weizenbaum (USA)

C8 SYMPOSIUM.....9:00 AM–GIBSON SUITE
MONTE CARLO METHODS

Chairman: B. Jansson (Sweden)

ANALYTICAL STUDIES OF PSEUDO-RANDOM NUMBER GENERATORS OF CONGRUENTIAL TYPES
B. Jansson (Sweden)

MONTE CARLO METHODS AND SOME MULTIVARIATE PROBLEMS
T. Tsuda (Japan)

MONTE CARLO METHODS AND STATISTICAL MECHANICS
L. D. Fosdick (USA)

THE SIMULATION OF CONFLICT SITUATIONS
J. L. Jenkins (USA)

C9 PANEL.....9:00 AM–GREEN ROOM
TESTING, CORRECTION, AND DOCUMENTATION OF PROGRAMMING

Chairman: J. C. Harwell (UK)

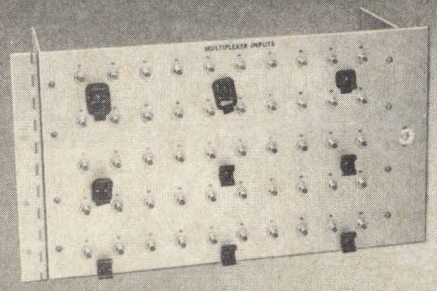
Panel Members: K. Bhagwandin (Sweden), G. E. Felton (UK), D. N. Freeman (USA), M. I. Halpern (USA), R. Rossheim (USA), and W. Turski (Poland).

D1 GENERAL SESSION....2:00 PM–EAST BALLROOM
COMPUTER PROGRAMMING

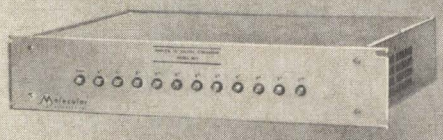
Chairman: C. C. Gotlieb (Canada)
Vice Chairman: M. Woodger (UK)

THE PLACE OF PROGRAMMING IN A WORLD OF PROBLEMS, TOOLS, AND PEOPLE
P. Naur (Denmark)

THE CHANGING BASIS OF PROGRAMMING
S. Gill (UK)



LOW-LEVEL RELAY MULTIPLEXER



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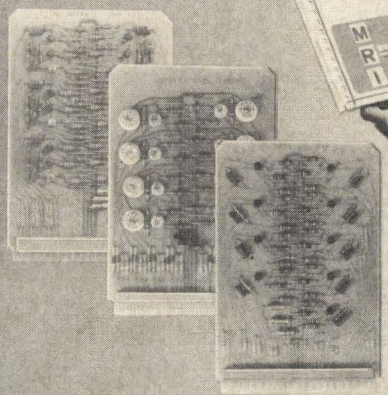
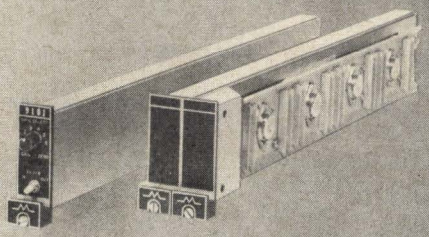


DIGITAL LOGIC MODULES



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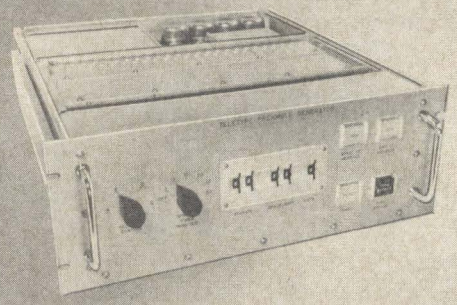
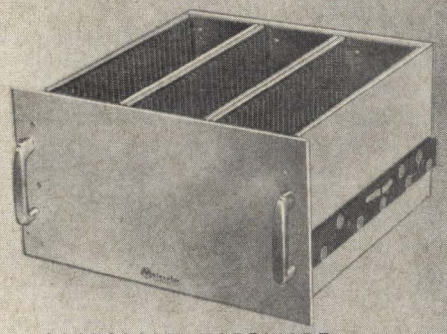
AMPLIFIER/MULTIPLEXER



TELETYPE MESSAGE GENERATOR



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CIRCLE NO. 14 ON INQUIRY CARD

PROGRAMMING IMPLICATIONS OF HARDWARE TRENDS
R. F. Clippinger (USA)

D2 SPECIAL SESSION....2:00 PM–WEST BALLROOM
OUTLOOK IN THE MEMORY AREA

Chairman: A. P. Speiser (Switzerland)
Vice Chairman: B. Langefors (Sweden)

INTEGRATED MAGNETIC AND SUPERCONDUCTIVE MEMORIES
J. A. Rajchman (USA)

FUTURE OF MAGNETIC MEMORIES
G. Kohn (Switzerland)

THE EFFICIENT USE OF MULTI-LEVEL STORAGE
G. G. Scarrott (UK)

D3 PANEL.....2:00 PM–BALLROOM FOYER
BATCH PROCESSING AND DIRECT PROCESSING

Chairman: K. R. Wright (USA)
Panel Members: C. W. Bachman (USA), R. H. Hill (USA), M. Kory (USA), R. C. McGee (USA), L. R. Pickel (USA), and H. Tellier (USA)

D4 SYMPOSIUM.....2:00 PM–TRIANON BALLROOM
DIGITAL AUTOMATIC CONTROL

Chairman: T. Moto-Oka (Japan)

DIRECT DIGITAL CONTROL SYSTEMS FROM THE CONTROL-ORIENTED POINT OF VIEW
A. S. Robinson (USA)

THE DIGITAL COMPUTER FOR PROCESS CONTROL APPLICATIONS
H. T. Marcy (USA)

DETERMINATION OF PROCESS STABILITY BY LEARNING ALGORITHM
W. Turski (Poland)

NUMERICAL CONTROL OF CAM-SHAFT GRINDING
S. Inaba and T. Moto-Oka (Japan)

A DIGITAL CONTROL VALVE AND ITS USE
H. H. Ernyei (France)

D5 SYMPOSIUM.....2:00 PM–LE PETIT TRIANON
AUTOMATED SOFTWARE PRODUCTION

Chairman: R. W. Bemer (France)

COMPILER CONSTRUCTION THROUGH MODELING
J. R. Dunlap (USA)

AUTOMATED PROGRAM DOCUMENTATION FOR LARGE COMMAND AND CONTROL SYSTEMS
R. J. Kot (USA)

A POSSIBLE FUTURE SYSTEM FOR AUTOMATING CONTROL OF THE DEVELOPMENT, DISTRIBUTION, AND MAINTENANCE OF PROGRAMMING SYSTEMS
W. R. Crowley (USA)

SOFTWARE SYSTEMS CUSTOMIZED BY COMPUTER
R. W. Bemer (France)

D7 SYMPOSIUM.....2:00 PM–MERCURY ROTUNDA
HYBRID DIGITAL-ANALOG COMPUTATION IN THE AEROSPACE INDUSTRY

Chairman: M. S. Mason (USA)
Organizer: R. Vichnevetsky (USA)

SATELLITE ORBITAL STABILITY PROGRAM WITH AN ANALOG-HYBRID COMPUTER
J. Stricker and W. W. Miessner (USA)

LONGITUDINAL OSCILLATION INSTABILITY STUDY OF THE GEMINI LAUNCH VEHICLE
W. W. Miessner and R. L. Goldman (USA)

INSTANT FLIGHT — JUST ADD DATA
D. E. Fought and W. G. McClintock (USA)

SPACECRAFT MISSION SIMULATION
J. J. Clancy (USA)

A HYBRID SIMULATION OF AN ABLATING NOSE CONE
E. H. Hochman and A. J. Hanawalt (USA)

D8 SYMPOSIUM.....2:00 PM–GIBSON SUITE
SYSTEM SIMULATION BY COMPUTERS

Chairman: H. S. Krasnow (USA)

SIMULATION FOR ELECTRIC POWER SYSTEMS
S. Miki (Japan)

GENERIC FEATURES OF MILITARY SIMULATIONS
E. Levine (USA)

A PROCESS-ORIENTED APPROACH TO SIMULATION MODELING
M. R. Lackner (USA)

STRUCTURE OF SEQUENCING ALGORITHMS FOR SIMULATION
B. M. Leavenworth and R. J. Parente (USA)

SIMULATION OF SOCIAL ACTION PROGRAMS
S. S. Ackerman (USA)

PROBLEMS IN THE DESIGN AND IMPLEMENTATION OF A SIMULATION LANGUAGE
K. D. Tocher (UK)

WEDNESDAY, MAY 26

E1 SPECIAL SESSION....9:00 AM–EAST BALLROOM
ORGANIZATION OF LARGE STORAGE SYSTEMS — II

Chairman: J. Carteron (France)

Vice Chairman: J. C. McPherson (USA)

E2 SPECIAL SESSION....9:00 AM–WEST BALLROOM
ARTIFICIAL INTELLIGENCE

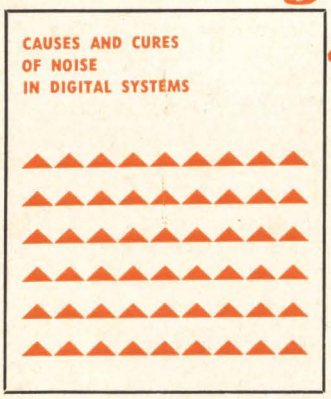
Chairman: C. K. Chow (USA)
Vice Chairman: H. R. Ciancaglini (Argentina)

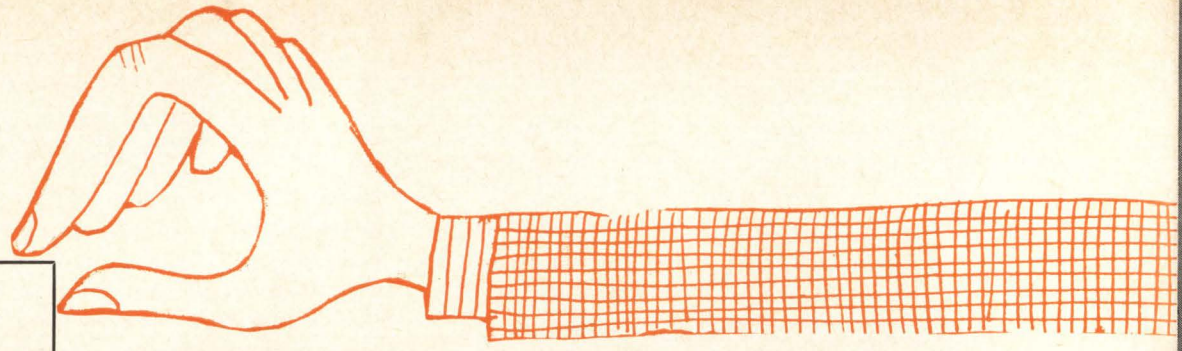
PRESENT AND FUTURE OF PATTERN RECOGNITION THEORY
V. A. Kovalevsky (USSR)

DYNAMIC CONTROL OF CORE MEMORY IN A REAL TIME SYSTEM
W. B. Elmore and G. J. Evans, Jr. (USA)

GENERAL PURPOSE EXTERNAL MEMORY SYSTEM FOR DATA BASE PROCESSING
J. M. Unk (Netherlands)

DYNAMIC FLOW OF PROGRAMS AND DATA THROUGH HIERARCHICAL STORAGE
A. Opler (USA)





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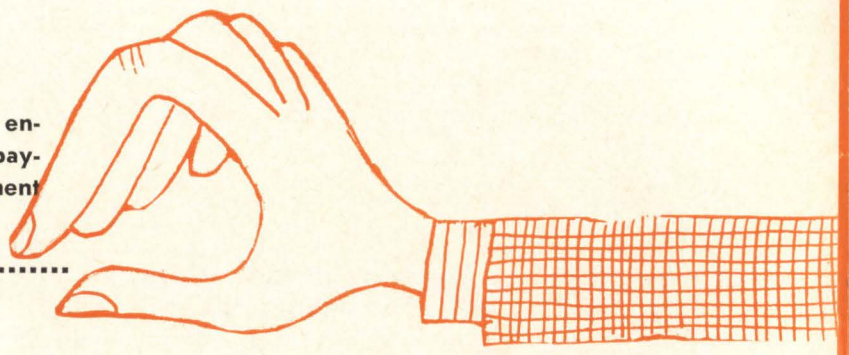

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MATTER, MIND, AND MODELS
M. L. Minsky, (USA)

FORMAL PROOFS AND AUTOMATIC THEOREM PROVING
H. Wang (USA)

E4 SYMPOSIUM.....9:00 AM–TRIANON BALLROOM
MICROELECTRONICS AND INTEGRATED CIRCUITS

Chairman: I. A. Lesk (USA)

INTEGRATED CIRCUIT PROCESSING TECHNOLOGY
I. A. Lesk (USA)

INTEGRATED CIRCUIT HIGH SPEED LOGIC CONSIDERATIONS
J. A. Narud (USA)

INTEGRATED CIRCUITS — COMMERCIAL COMPUTER APPLICATION
E. M. Davis (USA)

CUSTOM INTEGRATED CIRCUITS — A MILITARY COMPUTER APPLICATION
J. S. Kilby and R. C. Platzek (USA)

E5 SYMPOSIUM.....9:00 AM–LE PETIT TRIANON
HYBRID ANALOG-DIGITAL APPLICATIONS

Chairman: R. J. A. Paul (UK)

APPLICATIONS OF FAST ANALOG-HYBRID COMPUTERS TO RANDOM PROCESS SIMULATION (MONTE CARLO METHODS)
G. A. Korn (USA)

ERROR ANALYSIS OF DIGITAL COMPUTER ORIENTED HYBRID SYSTEMS
W. J. Karplus (USA)

HYBRID SOLUTION OF INITIAL VALUE PROBLEMS FOR PARTIAL DIFFERENTIAL EQUATIONS
H. Witsenhausen (USA)

AN INVESTIGATION OF NUMERICAL INTEGRATION AND MULTIPLE VARIABLE UPDATING RATES USING THE DES-1
L. Levine (USA)

THE APPLICATION OF HYBRID ANALOG DIGITAL TECHNIQUES TO THE STUDY OF PREDICTIVE CONTROL
J. F. Coales (UK)

DESIGN OF A HYBRID COMPUTER FOR THE CALCULATION OF SIGNAL STATISTICS
B. P. T. Veltman (Netherlands)

E7 SYMPOSIUM.....9:00 AM–MERCURY ROTUNDA
COMPUTER ARITHMETIC — I

Chairman: A. Svoboda (USA)

SOME ASPECTS OF THE DESIGN OF A SIMULTANEOUS MULTIPLIER FOR A PARALLEL BINARY DIGITAL COMPUTER
T. Lamdan and D. Aspinall (Israel)

ANALYSIS OF INHERENT ERRORS IN MATRIX DECOMPOSITION USING UNNORMALIZED ARITHMETIC
N. C. Metropolis (USA)

PRELIMINARY LOGICAL DESIGN OF A TERNARY DIGITAL COMPUTER
J. Santos and H. Arango (Argentina)

METHODS OF SELECTION OF QUOTIENT DIGITS DURING DIVISION
J. E. Robertson (USA)

A LOW COST PARALLEL BINARY ADDER
B. G. Utley (USA)

F1 GENERAL SESSION....2:00 PM–EAST BALLROOM
AUTOMATA THEORY AND SIMULATION OF THOUGHT PROCESS

Chairman: H. Zemanek (Austria)
Vice Chairman: J. Kryze (Czechoslovakia)

AUTOMATA THEORY AND ITS APPLICATION
V. M. Gloushkov (USSR)

AUTOMATIC PROCESSING OF NATURAL AND FORMAL LANGUAGES
A. G. Oettinger (USA)

THE SEARCH FOR GENERALITY
A. Newell (USA)

F3 SYMPOSIUM.....2:00 P.M.–BALLROOM FOYER
LIST PROCESSING

Chairman: J. Weizenbaum (USA)

ALGEBRAIC FORMULA MANIPULATION IN ALGOL
A. J. Perlis (USA)

LIST PROCESSING AND THE SIMSCRIPT WORLD VIEW
P. Kiviat (USA)

STORAGE ALLOCATION FOR A SYSTEM OF MIXED DATA TYPES
M. Levin (USA)

FORMAL MANIPULATION OF SYMBOLIC EXPRESSIONS WITH AN ALGORITHMIC LANGUAGE
M. Engeli (Switzerland)

TITLE TO BE ANNOUNCED
C. Strachey (UK)

F5 SYMPOSIUM.....2:00 PM–LE PETIT TRIANON
OPTICAL AND ELECTRO-OPTICAL INFORMATION PROCESSING

Chairman: D. K. Pollock (USA)
Organizers: D. F. Pollock, Mary E. Stevens, and J. Tippett (USA)

COMPUTERS AND OPTICS
L. Clapp, J. Tippett, and Mary E. Stevens (USA)

ASPECTS OF OPTICAL INFORMATION PROCESSING
L. J. Cutrona (USA)

RECENT PROGRESS IN DOUBLE DIFFRACTION FILTERING
A. Marechal and S. Lowenthal (France)

QUANTUM ELECTRONIC LOGIC
C. J. Koester (USA)

OPTICAL DEVICES AND INFORMATION PROCESSING
N. S. Kapany (USA)

F7 PANEL.....2:00 PM–MERCURY ROTUNDA
CONTENT ADDRESSABLE MEMORIES

Chairman: R. R. Seeber (USA)
Reporter: B. Lindquist (USA)
Panel Members: P. M. Davies, R. J. Ferris, R. H. Fuller, J. E. McAteer, and J. P. Pritchard, Jr. (USA)

SUMMARY: To throw some light on past difficulties and future possibilities of content addressable memories, the panel will discuss system organizations, arithmetic algorithms, magnetic and cryogenic fabrication technology, and potential applications.

IFIP Congress 65 (Continued)

THURSDAY, MAY 27

G3 SYMPOSIUM.....9:00 AM–BALLROOM FOYER
ULTRA-HIGH SPEED COMPUTERS

Chairman: O. H. Bartlett (USA)

THE X03 TUNNEL DIODE COMPUTER
P. Kellett (UK)

500 MC MICROLOGIC CIRCUITS IN AN EXPERIMENTAL DIGITAL ASSEMBLY
Y. Cho, J. B. Connolly, and E. P. Edelson (USA)

ULTRA-HIGH FREQUENCY LOGIC CIRCUITS IN EXPERIMENTAL MACHINES
W. Piel (USA)

SYSTEM 360 AND THE HIGH-PERFORMANCE MODEL 92
G. M. Amdahl (USA)

G4 SYMPOSIUM....9:00 AM–TRIANON BALLROOM
MAN-MACHINE INTERACTION: REMOTE CONSOLES AND DISPLAYS

Chairman: J. C. R. Licklider (USA)

GRAPHICAL COMMUNICATION IN A TIME SHARING ENVIRONMENT
L. G. Roberts (USA)

A UNIVERSAL DISPLAY CONSOLE
R. Stark, R. Mallebrein, and D. Matejka (Germany)

THE ULTIMATE DISPLAY
I. E. Sutherland (USA)

PROBLEMS AND PRINCIPLES OF CONSOLE DESIGN
J. C. R. Licklider (USA)

G6 SYMPOSIUM.....9:00 AM–MERCURY BALLROOM
COMPUTER-CONTROLLED MESSAGE SWITCHING SYSTEMS

Chairman: A. B. Shafritz (USA)

IMPROVEMENTS AFFORDED STORE-FOREWARD MESSAGE SWITCHING NETWORK NODES USING DIGITAL COMPUTERS
R. Thomas (USA)

SPECIAL SYSTEMS OR COMPUTER CONTROL FOR MESSAGE SWITCHING
K. Gosslau (Germany)

COMPUTATION OF CAPABILITY AND PERFORMANCE CURVES FOR COMPUTER-CONTROLLED MESSAGE SWITCHING SYSTEMS
R. L. Sharma (USA)

MESSAGE SWITCHING AS A SUBSIDIARY FUNCTION OF CENTRALIZED INFORMATION PROCESSING
J. F. Dudas, C. E. Skidmore, and R. C. Cheek (USA)

CONSIDERATIONS OF BASIC PROCESSOR AND REAL-TIME COMMUNICATIONS INTERFACE
S. Tucker and E. Hillman (USA)

H1 GENERAL SESSION....2:00 PM–EAST BALLROOM
TRENDS IN COMPUTER DESIGN

Chairman: J. G. Santesmases (Spain)
Vice Chairman: C. V. L. Smith (USA)

COMPUTERS IN THE USA — TODAY AND TOMORROW
S. Fernbach (USA)

THE FUTURE OF COMPUTER ARCHITECTURE
F. P. Brooks (USA)

INTERNATIONAL COMPUTER APPLICATIONS AND THEIR IMPACT ON SYSTEMS DESIGN
J. G. Miles (USA)

FRIDAY, MAY 28

J1 SPECIAL SESSION.....9:00 AM–EAST BALLROOM
DESIGN OF INFORMATION SYSTEMS

Chairman: W. S. Humphrey, Jr. (USA)

THE AUTOMATIC DESIGN OF A DATA PROCESSING SYSTEM
C. B. Greenberger (USA)

DESIGN OF A GENERAL PURPOSE SCIENTIFIC COMPUTING FACILITY
F. V. Wagner and J. W. Granholm (USA)

DESIGN OF A REAL-TIME DATA PROCESSING SYSTEM
E. C. Svendsen and D. L. Ream (USA)

CONCEPT OF A REAL-TIME SYSTEM AUTOMATING AIR TRAFFIC CONTROL
J. Villiers (France)

J6 SYMPOSIUM.....9:00 AM–MERCURY BALLROOM
MASS MEMORIES

Chairman: R. A. Shahbender (USA)

MASS RANDOM ACCESS CORE MEMORY
R. W. Staats and E. E. Hanson (USA)

RANDOM ACCESS CARD MASS MEMORY
J. F. Gates (USA)

A MASS MEMORY CENTERED PROCESSOR
G. W. King (USA)

PERMALLOY SHEET RANDOM ACCESS MASS MEMORY
H. W. Fuller (USA)

LARGE CAPACITY, LOW COST CORE MEMORY
R. J. Petschauer (USA)

J7 PANEL.....9:00 AM–MERCURY ROTUNDA
MECHANIZATION OF CREATIVE PROCESSES

Chairman: E. A. Feigenbaum (USA)
Panel Members: G. I. Marchuk (USSR), J. McCarthy, U. Neisser, A. Newell (USA), and G. Pask (UK)

K2 SPECIAL SESSION....2:00 PM–WEST BALLROOM
AUTOMATA THEORY AND SWITCHING THEORY

Chairman: F. L. Bauer (Germany)

THE REALIZATION OF BOOLEAN FUNCTIONS WITH THE AID OF DIAGRAM AND FORMULAS
Ju. Zhuravlev (USSR)

CLASSIFICATION OF COMPUTATIONS BY TIME AND MEMORY REQUIREMENTS
P. M. Lewis II, J. Hartmanis, and R. E. Stearns (USA)

ON THE ALGEBRAIC THEORY OF AUTOMATA
M. P. Schutzenberger (France)

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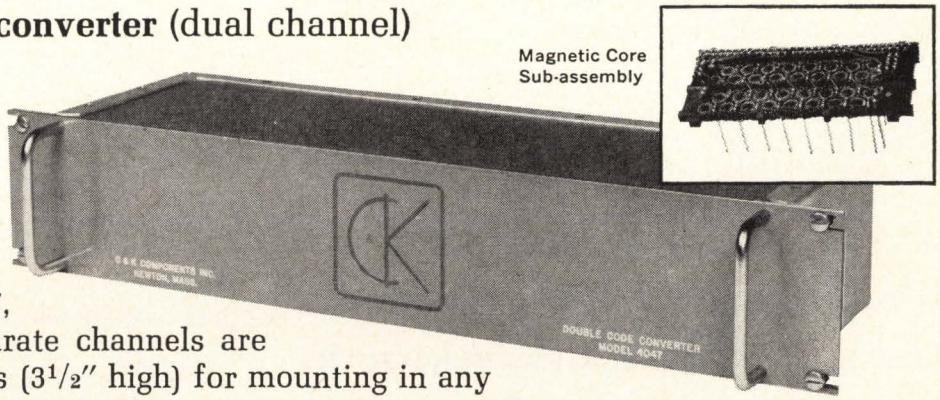
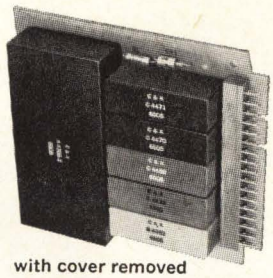
Magnetic Code Converters

model 4047 magnetic code converter (dual channel)



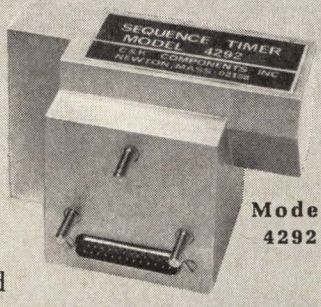
C & K's **Model 4047** Magnetic Code Converter is designed for use in data processing operations for the conversion of **one** 7, 8 or 9-bit code to **another** 7, 8 or 9-bit code. **Two** separate channels are provided in a single chassis ($3\frac{1}{2}$" high) for mounting in any standard relay rack. **Model 4047** utilizes magnetic tape-wound cores (see insert) and silicon circuitry to provide readouts of arbitrary binary functions.

model 4043 magnetic code converter


with cover removed

Model 4043 Magnetic Code Converter accepts a parallel 8-bit "argument" as an **input** and produces a parallel 8-bit function as an **output.** The 256 binary "function" numbers are completely arbitrary — they are specified by the user and permanently wired into the 32-bit core matrix.

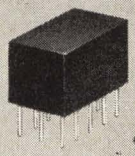
magnetic Timers



Model 4292

C & K Magnetic Timers provide long counting intervals with very economical power consumption, small size and light weight; they are encapsulated in epoxy resin for maximum mechanical stability.

magnetic Logic Elements


Model 4333
(approx. actual size)

C & K Magnetic Logic Elements may be combined to produce magnetic timing and control systems. A complete line of compatible pulse drivers, output code detectors and gating circuits are available!

C&K COMPONENTS, INC.

low power digital/magnetic timing and control devices
101 Morse Street, Newton, Massachusetts 02158
Telephone: 617 926-0800

CIRCLE NO. 15 ON INQUIRY CARD

IFIP Congress 65 (Continued)

K3 SYMPOSIUM. . . . . 2:00 PM–BALLROOM FOYER HIGH-SPEED AND READ-ONLY MEMORIES

Chairman: H. E. Billing (Germany)

SYNOPSIS ON CONVENTIONAL MAGNETIC FILM MEMORIES
E. M. Bradley (UK)

TWENTY-NANOSECOND MAGNETIC FILM MEMORY
W. W. Davis (USA)

FLUTED FILMS USED FOR STORAGE DEVICES
A. Ruediger and H. E. Billing (Germany)

HIGH-SPEED THIN-FILM WOVEN MEMORY: CONSTRUCTION AND USE
M. Nitta, H. Nishino, M. Maeda, and A. Matsushita (Japan)

A SEMIPERMANENT HIGH-SPEED STORE USING THICK MAGNETIC FILMS
L. M. Terman, P. Pleshko, and C. Sie (USA)

SATURDAY, MAY 29

L1 GENERAL SESSION. . 9:00 AM–GRAND BALLROOM CLOSING SESSION: MAN AS AN INFORMATION PROCESSING SYSTEM

Chairman: I. L. Auerbach (USA)

Traditionally, it is the objective of the Closing Session of an IFIP Congress to identify an area of frontier research that might point the way toward significant technological achievements in the coming years. In the constantly increasing effort to achieve more sophistication in the design of machines to emulate man's capabilities, we must pursue our exploration and understanding of man himself. Man has been the model around which we have tried to pattern computer system design. It is interesting that recent system design concepts have been moving away from totally centralized control concepts toward decentralized control concepts. Man's nervous system is, in fact, a decentralized system. His sensors transmit information rather than raw data to the brain. Therefore a certain amount of data reduction must take place at these sensors. Otherwise his communication links would be perpetually overloaded with background data rather than information.

This session will present some of the exciting work going on in the field of identification of man's structure, to achieve a better understanding of man and his interaction with his environment. These studies may show how we can further emulate man in our future system design — that is, until we find a more sophisticated organism to emulate.

At the end of the session the newly elected President of IFIP will be introduced and the outgoing President will close the Congress.

HOW TO TELL THE BIRDS FROM THE BEES: THE ONTOGENESIS OF INFORMATION
H. von Foerster (USA)

THE COMMAND AND CONTROL SYSTEM OF THE VERTEBRATES
W. S. McCulloch and W. L. Kilmer (USA)

INFORMATION IN BRAINS AND MACHINES
D. M. MacKay (UK)

INTRODUCTION OF THE NEWLY ELECTED IFIP PRESIDENT

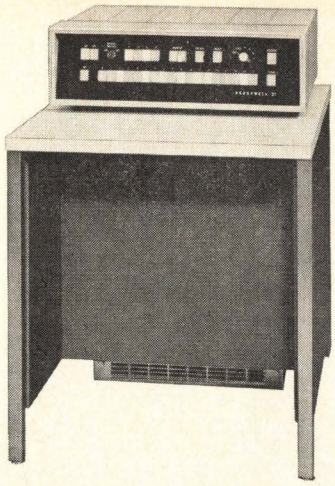
CLOSING OF IFIP CONGRESS 65
I. L. Auerbach

NEW BOOKS

TRANSISTOR REFERENCE BOOK

International Resistance Co. is now marketing the second edition of DATADEX, the first transistor reference book to feature functional coding of transistors. Published by M. W. Lads Publishing Co. of Philadelphia, the new edition contains more than 5000 types of transistors, 1500 more than the first edition, indexed by parameters, and cross-indexed by JEDEC and DATADEX numbers. Another significant change is the addition of field effect transistors in the theory, circuit and data sections. Other features are the "Interchangeability Guide" covering all current domestic semiconductors and many foreign types, and relative price information on all domestic types. The 300-page book is priced at $3.95 per copy. Order from:

International Resistance Co., 414 N. 13th Street, Philadelphia, Pa. 19108.



if you can find a better main frame for the price . . . get it!

We're talking about the H21 – central processor for the new Honeywell 20 Digital Control System. The main frame price, starting at $21,000* is one of many features which make it an attractive component for real-time systems.

Some other features are:

Word Length: 18 bits plus parity and memory guard bits. Single word instructions provide 8192 directly addressable core locations.

Priority Interrupts: Up to 16 hardware levels.

Memory: Magnetic core, random access; 2,048 to 16,384 words capacity; prewired for field expansion; non-volatile on power failure.

Memory Guard: Gives "padlocked" protection against accidental modification of guarded core locations.

Direct Memory Access: Independent path to memory for external I/O operations on a fully buffered, cycle-steal basis.

Silicon Hybrid Circuits with low active component count insure reliable system operation from 32 to 120° F.

Indexing may be combined with indirect addressing.

Three-Address Register Commands allow three-address arithmetic and/or logical operations with single word, one cycle instructions.

Double Length Accumulator facilitates 36-bit arithmetic.

Parallel I/O Channels — designed to provide efficient and convenient interface with user's system equipment.

Typical Operating Speeds (in microseconds, including accessing and indexing): register arithmetic/logical operations, 6.0; load/store, 12.0; multiply, 54.0.

Options: Auxiliary drum memory, magnetic tape unit, high speed paper tape punch and tape reader, priority interrupts, DMA.

Software—An extensive software package includes CONTRAN, the new compiler-level programming system for real-time control; FORTRAN IV with linkage capability to executive programs; and CAP assembly system plus arithmetic, utility, and diagnostic programs.

The H22 central processor with a cycle time of 1.75 microseconds is available at a slightly higher price.

For additional information . . .
call or write A. L. Rogers, Sales Manager
Special Systems Division, Queen & South Bailey Sts.,
Pottstown, Pa. 19464. Telephone: 215-FA 3-4000

*Basic price of $21,000 includes H21 central processor with 2K core and input/output typewriter with integral tape punch and reader.

Honeywell

CIRCLE NO. 17 ON INQUIRY CARD

THE ELIMINATION OF FALSE DIGIT DISPLAY IN SEGMENTED-TYPE READOUTS

Segmented-type digital readouts have many obvious advantages over other types of readouts. First, the illuminating devices, being very close to the surface of the display, produce digits which are all in the same plane and free from annoying obstructions. This also allows the segmented type display to be comfortably viewed from wide angles without the image washout which occurs in readouts which project a digit onto a front diffuser and are best viewed head-on. Another advantage is the high brightness obtainable with segmented readouts due to the direct illumination of each segment without the light losses of complicated optical systems. However, a major disadvantage of segmented readouts is the occurrence of false digit display.

This disadvantage has been overcome in a new segmented-type digital readout developed by M.B. Associates of Philadelphia. As explained by H. L. Martins, Director of Engineering at M.B., lamp failures cannot cause false digits to be displayed on this readout.

Designated Type NSDFS, the readout consists of seven segments, each illuminated by a lamp. Fig. 1 shows the ten digits as they normally appear on the readout. One or more lamp failures in any digit except the 1, 2, or 5 could cause a false digit to be displayed on a conventional segmented display. However, in the NSDFS readout, a lamp failure in **any** segment causes the lamps in the lower right and bottom segments to remain out. An examination of the ten digits will show that without these two segments illuminated a normal digit cannot be displayed. This is illustrated in Fig. 2. At the left of Fig. 2 are shown two digits, 6 and 8, as they normally appear. In the center are the digits as they would appear on a conventional segmented readout in the event of certain lamp failures. A failure of the lower left segment when a 6 is to be displayed results in a 5 instead. Failures of the upper left and lower left segments when an 8 is to be displayed result in a 3. At the right of Fig. 2 are the digits as they would appear on the NSDFS readout in the event of the same lamp failures. It is impossible for the segments remaining lit to be interpreted as a normal digit.

Fig. 1 The ten digits as they normally appear on the NSDFS segmented-type readout.

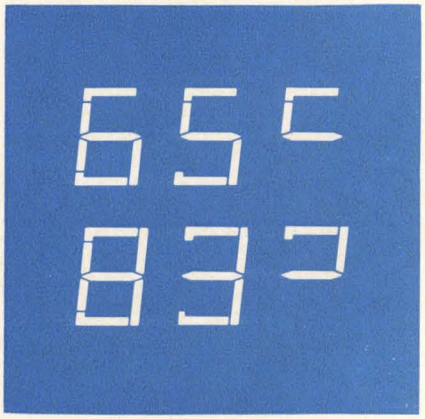


Fig. 2 Digits at the left have normal appearance. Lamp failures cause false digits to appear in conventional segmented readouts, as shown in center. With the fail-safe readout discussed here, any segment lamp failure causes the bottom and right leg segments to drop out, thus, as shown at the right, the failures produce unintelligible characters.

The NSDFS readout, shown in Fig. 3, is the latest addition to M.B. Associates' line of NSD digital readouts. All of the readouts in this line use high brightness neon lamps for illumination. These lamps are operated to give 60,000 hours life so that for most applications the fail-safe feature is not required. However, in certain critical applications, the additional reliability afforded by the NSDFS display is desirable.

The failure mode of high brightness neon lamps is such that at the end of life their firing voltage rises and exceeds the circuit voltage available to operate them. They then appear to the driving source as an open circuit. This fact is used in sensing and correcting for a lamp failure.

Martins looks for a wider acceptance of segmented-type readouts as the result of eliminating false digit presentation.

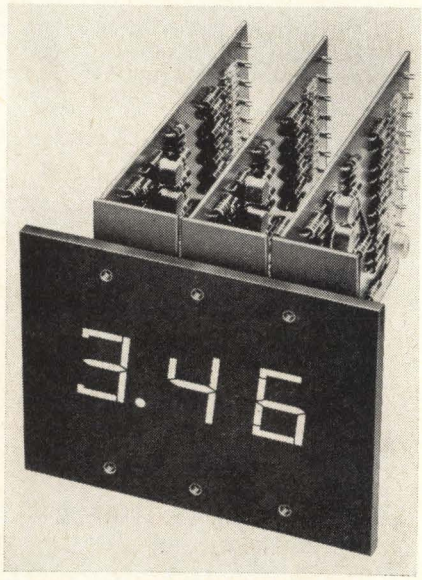
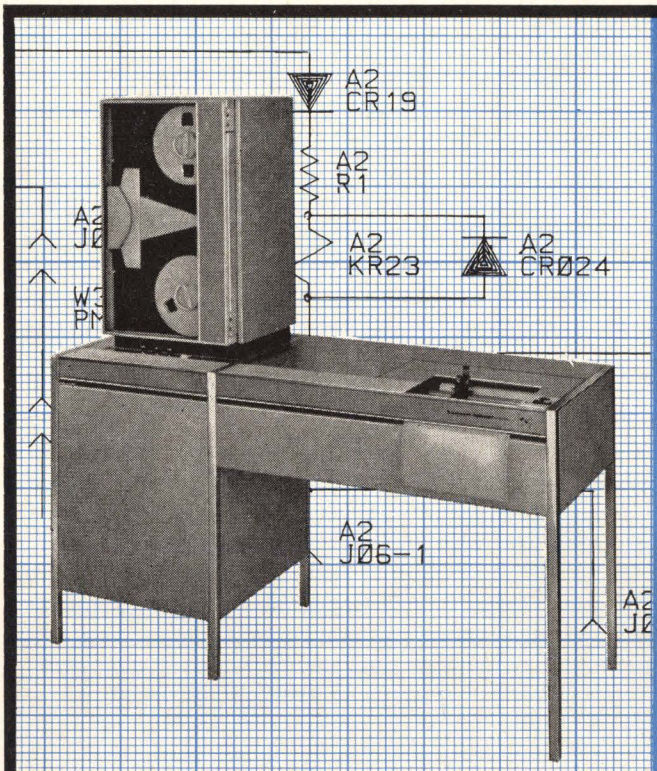


Fig. 3 M.B. Associates' NSDFS readout assembly. Decoder-driver and circuitry which provides fail-safe indication are integrally mounted with readout. Cost is $49 per digit.

Circle No. 105 on Inquiry Card



DIGITAL PLOTTING *Is The Difference*

There is a great deal of difference in digital plotting when you consider the dramatic advantages found only in Benson-Lehner's new 30 - inch DRAFTOMATIC System.

1. Dual density (200 and 556 bpi) tape handling capability
2. High speed (300 steps/sec.)
3. High resolution (.005 inches)
4. Modular construction
5. Wide range of flexibility
6. Compatible with all digital computers
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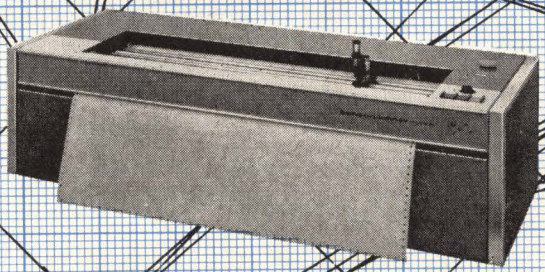
9. 120 ft. paper roll capability*

*** 30 inch plotting paper is available with any desired pre-printed grid, or, if more economical, 12 - inch plotting paper can also be used.**

Many computer sub-routines are available in our library for your use. Programming assistance is readily available.

Our warranty service is backed by the nation's largest field service organization specializing in computer-graphic equipment.



benson lehner

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CIRCLE NO. 18 ON INQUIRY CARD

Multiaperture Core Testing System

By providing high speed 100% testing of two-hole ferrite cores, this new system might change the status of multiaperture core memories from experimental to volume production items.

One major obstacle to the widespread use of multiaperture core devices has been the difficulty of high-speed testing. Automatic testing of this type of device is complicated by the number of holes and lack of symmetry with respect to these holes. This latter fact makes it necessary to orient the device physically so that the proper probe can be applied to the proper hole. Also, a multiaperture device requires a more complex test program than the conventional ferrite core.

In the past, several limited tests were applied to each multiaperture core in a number of successive passes only a small sample from a batch was used for evaluation purposes. This entailed repeated physical handling — positioning and probe insertion — of the device as well as recalibrating and reprogramming after each test. These procedures have been time-consuming and costly.

The need for an advanced test system became critical with the development of the Phoenix Computer, being built by Litton Industries under a subcontract from Hughes Aircraft. This computer features a modular expandable memory in which the program section contains as many as 800,000 multiaperture devices. Since fourteen of these systems are on order with the eventual possibility of 200 systems, the testing problem became sizeable. Lockheed is currently producing the multiaperture cores used in these memories. To meet the requirement for volume production and stringent quality control for this type of device, Lockheed specified what has been termed the industry's first fully-automatic multiaperture device tester. A team of memory test equipment specialists — Computer Test Corp. and Ramsey Engineering — designed, built, checked-out, and delivered the test system on schedule. It is now in full service, testing two-hole MADs destined for use in the TFX fighter.

The system, the CTC Model 2046, is a sophisticated tool which provides complete physical handling of the devices, applies a series of complex electrical tests to each one, automatically analyzes the performance of the device under test, and sorts it accordingly — at a rate of up to 60 units per minute. Compared to previous testing techniques, which adapted conventional toroidal core test systems, the new system is said to represent a sizeable increase in speed and reliability (of better than an order of magnitude) and practically eliminates physical handling. In addition, the new system automatically checks its own calibration while testing the ferrites. It will stop operation and indicate the cause, if there is a malfunction, or if the system needs recalibration.

System Description

The CTC Model 2046 consists of two racks of electronic test instrumentation and a self-contained mechanical handler with its own electronic controls. It has been designed for testing two-hole rectangular ferrites 0.098″ × 0.086″ × 0.015″ having holes 0.040″ and 0.015″ in diameter. The system will apply a programmed series of tests which closely simulate the conditions to which the device will be subjected in its dynamic application. Fig. 1 illustrates and explains the main elements of the system which basically consist of a Ramsey MAH-10 Mechanical Handler and an electronic test station built by Computer Test Corp.

In actual operating conditions the multiaperture core is subjected to various kinds of writing and reading pulses. In addition, there are half-write pulses which are insufficient to switch the ferrite or to cause a read-out signal. Since this is a nondestructive readout component, information may be written into the ferrite and then read out many times before anything else is written into it. To be acceptable, a multiaperture device must be able to undergo this constant reading out without changing state.

The system provides a series of tests to check the behavior of the ferrite under simulated operating conditions. Fig. 2 shows the test used at Lock-

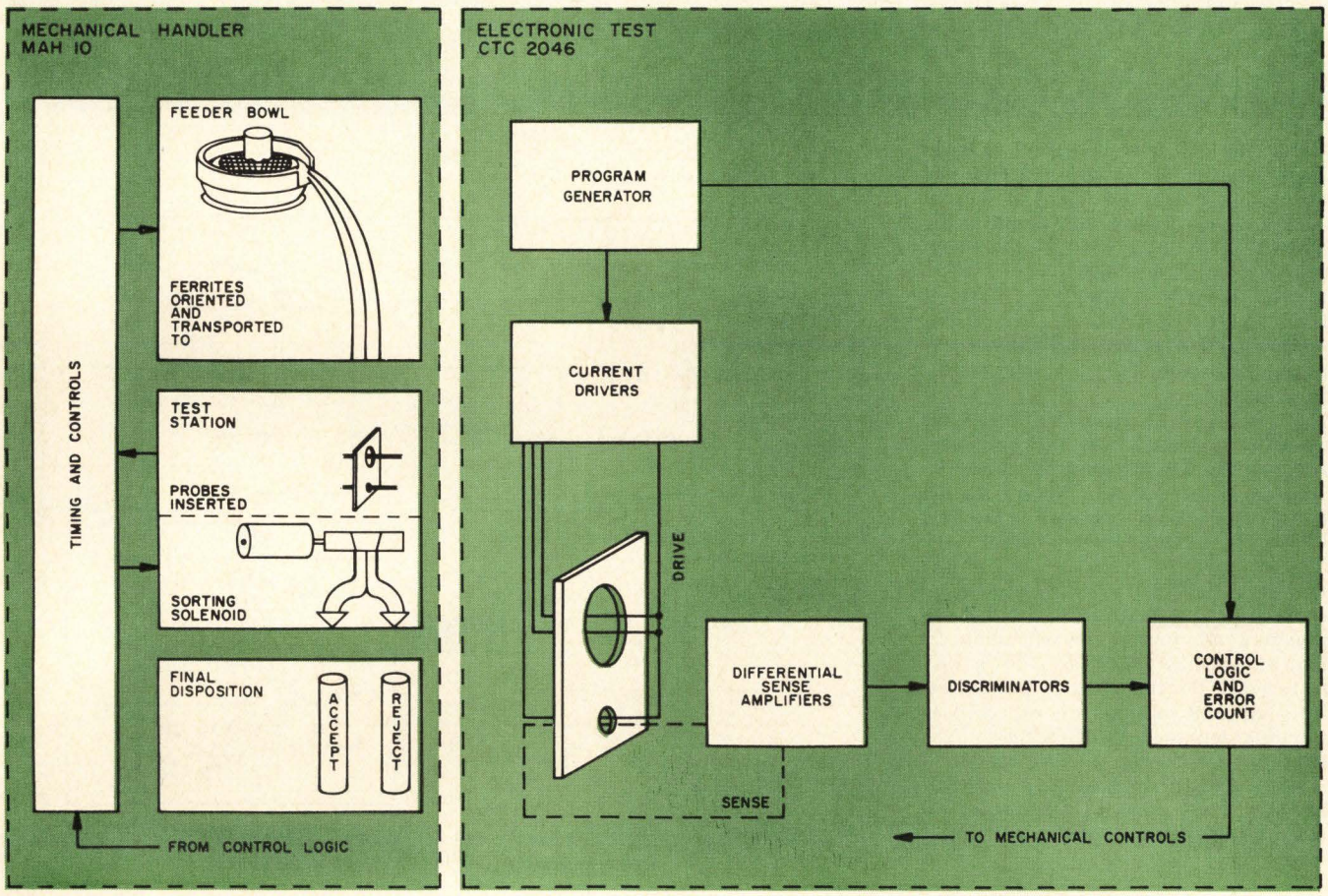


Fig. 1 The automatic test system for testing multiaperture cores consists of a Ramsey Engineering MAH-10 Mechanical Handler and Computer Test Corp.'s Model 2046 Electronic Test Station. As shown in the diagram, the handler consists of a vibrating feed bowl in which ferrites are placed to screen out chips and oversize units. The screened ferrites are vibrated up a spiral raceway and enter a feed chute where they undergo two stages of physical orientation to insure proper alignment. At the lower end of the chute the ferrites are transported, one at a time, to the Test Station. Here the device is held in place by vacuum techniques and two reciprocating dual conductor probes are inserted, one into each hole. Wiping contacts mate to the probes and complete the separate drive and sense circuits through the ferrite. At the end of the test a signal indicating acceptance or rejection instructs the handler to actuate a sorting solenoid, thus directing the ferrite into the proper receptacle. A new ferrite is then placed in position and the cycle is repeated. The test station provides the test patterns and the precisely-controlled current pulses for driving the multiaperture core being tested. It also receives the output from the core, amplifies it, and at certain points in the program, compares it against preset levels by means of precise voltage discriminators. Depending on the results of this comparison, the decision is made to accept or reject the ferrite. A signal is then sent to the control section of the handler for the final disposition of the device. Counters are used to record the numbers of accepts and rejects as well as the cause for rejection. Another feature of the system is a fail-safe technique which employs a reference device. Simultaneously with each device under test the same tests are applied to the reference device. If the reference device fails to respond within very narrow limits, the device under test is rejected.

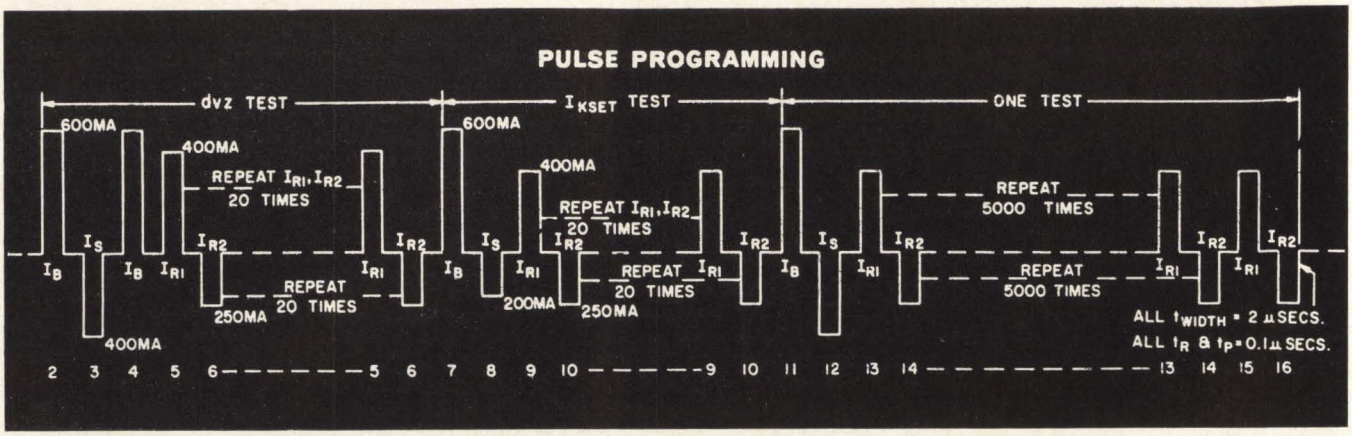


Fig. 2 The test procedure used at Lockheed consists of a basic 16 step sequence of 5 different types of current pulses. These pulses correspond to the READ-WRITE pulse used in the memory system. They are:
I_B = I_{BLOCK} (WRITE ZERO);
I_S = I_{SET} (WRITE ONE);
I_K = $I_{K\ SET}$ (HALF-WRITE ONE);
I_{RI} = READ; and
I_{R2} = RESET.
The sequence is generated twice for each ferrite tested. The first sequence is called the Conditioning Cycle and its purpose is to provide a history for the ferrite. The second sequence is the Test Cycle and provides three different tests. The dV_z test checks the ferrite's ability to retain a ZERO after a number of readouts. Note that steps 5 and 6 are repeated 20 times, corresponding to that many READ-RESETS. The I_K SET test checks the threshold of the device. Here steps 9 and 10 are repeated to simulate repeated READ-RESETS. The ONE test checks the ferrite's ability to retain a ONE after a number of READ-RESETS. Here steps 13 and 14 are repeated more than 5,000 times.

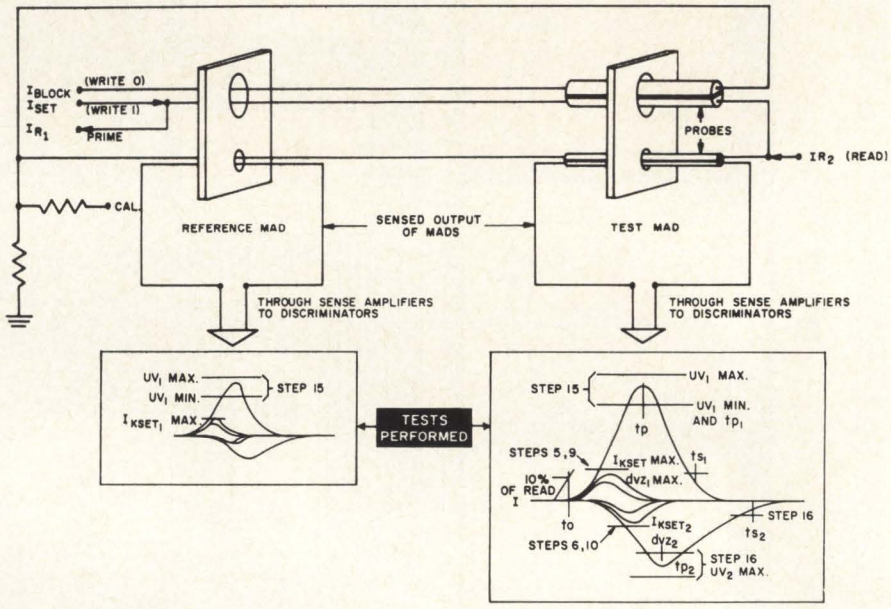


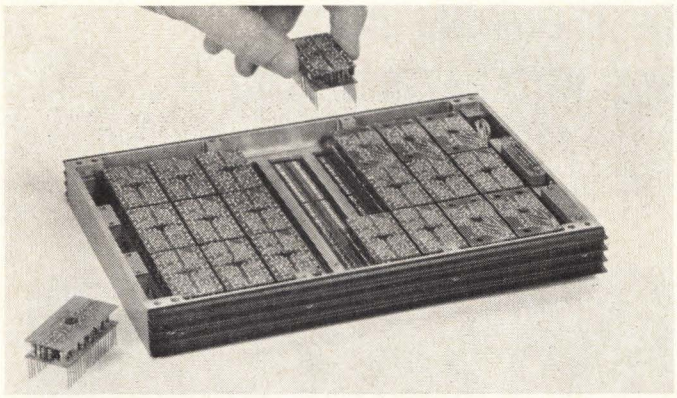
Fig. 3 Various inputs are applied to both the reference ferrite and to the ferrite under test.

heed. It consists of a basic 16 step sequence of five different types of current pulses. Fig. 3 shows how the various inputs are applied to both the reference ferrite and to the ferrite under test. The behavior of the core is described in terms of the pulse induced on the sense winding. Evaluation of the output pulse is accomplished by comparing certain of its parameters against acceptance criteria. The parameters of this pulse which are important are the amplitude and the switching time. In the Lockheed system, these parameters are checked under simulated operating conditions by sampling of the sensed output of the ferrite at specific times during the test. The sample is compared to a preset acceptable value by means of a precision discriminator which will indicate whether a given voltage is within a certain prescribed range. The Lockheed test measures the output not only after the first readout pulse, but also after the repeated READ-RESET sequence; thus providing a more comprehensive picture of the ferrite's behavior.

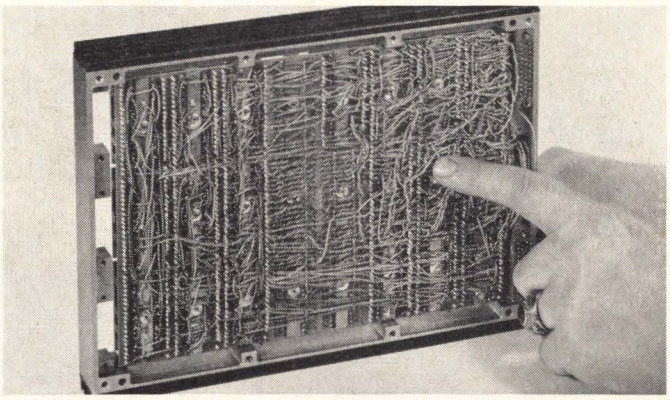
If the sample of the sensed output pulse falls outside the limits prescribed by any of the discriminators, a signal is sent to the control logic section where a decision is made as to the type of failure and to reject the ferrite. If the discriminators associated with the reference core show a failure, the test is invalidated. Sixteen cumulative invalidated tests will cause the system to shut down and indicate system failure.

The system used at Lockheed is characterized by a number of instrumentation advances which permit new levels of precision and reliability both in controlling the test input signal and in the analysis of the output. Some of the obvious ones are the ability to insert a two-conductor probe in an 0.015″ aperture at high speeds, allowing compensating circuitry to overcome the problems of common mode signals; a broad test pattern capability with simplified programming techniques; wide bandpass differential sense amplifiers with unusually high common mode to differential signal rejection ratios; and highly-accurate core signal discriminators which permit the precise analysis of output voltage during a strobe interval as short as 10 nanoseconds.

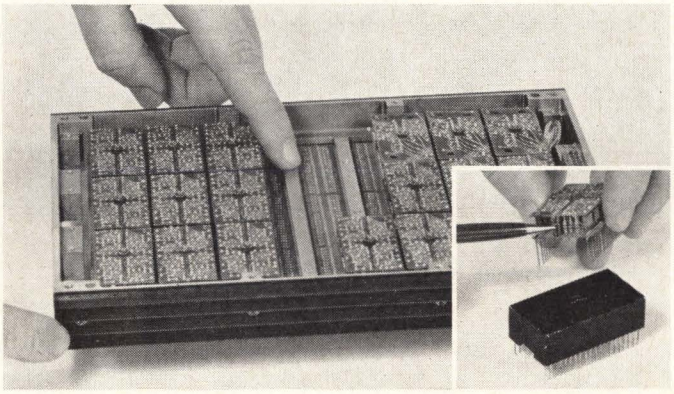
Circle No. 102 on Inquiry Card



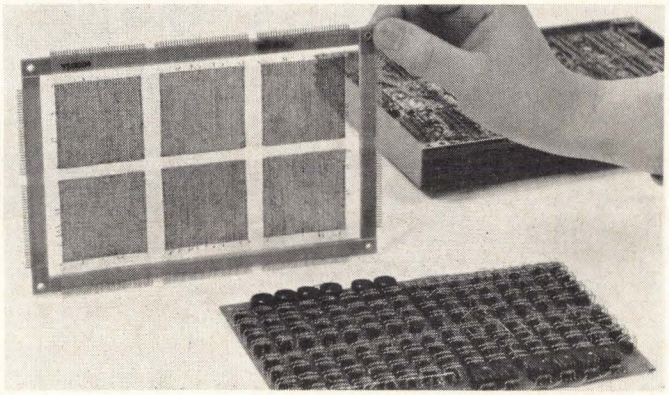
Economical circuit modules, mated directly through a parent-board assembly can be potted with light-closed cell foam if desired.



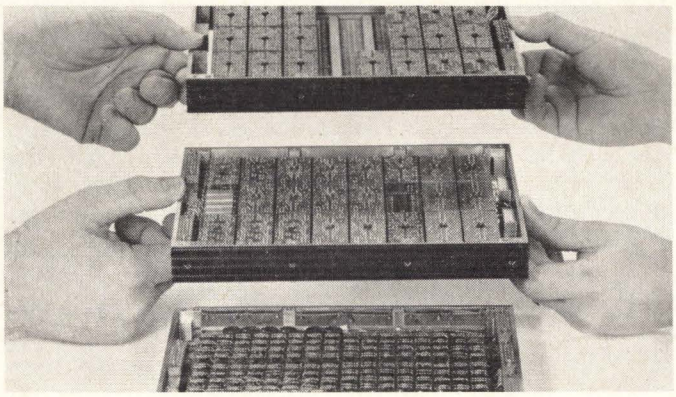
Wrapped wiring of circuit module terminations eliminates connectors, increases reliability, and yet retains easy replacement features.



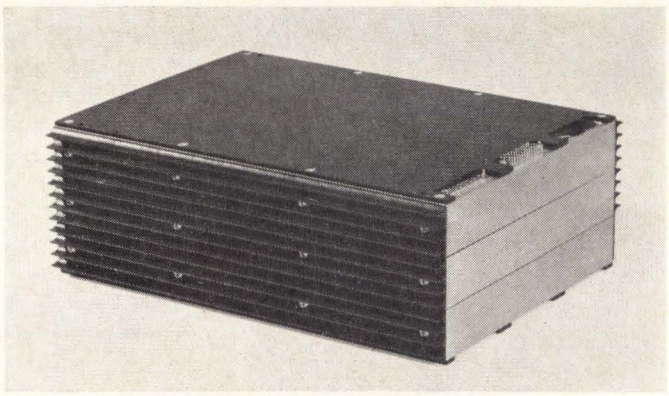
All heat-producing components mount directly to heat sinks. Inset shows how circuit modules each contain individual heat conductors.



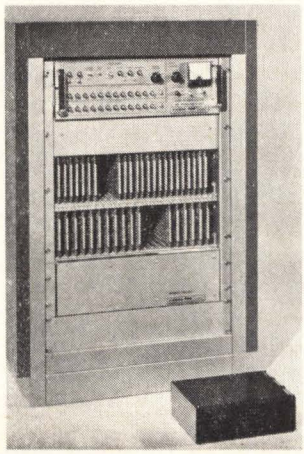
Memory stack consists of 64 x 64 core arrays mounted on rugged, laminated frames. Wide temperature cores are used. Planes can be potted.



System is composed of stacked modules. Number of modules depends upon memory capacity. This typical system has 3 modules and a capacity of 4,096 x 12.



This typical Series MC memory is 7.25″ x 9.375″ and weighs approximately 8 pounds. Max. power dissipation is less than 48 watts. Operating temperature range is —55° to 71°C.



A COMPACT, RUGGEDIZED MEMORY FOR SPECIAL-PURPOSE APPLICATIONS

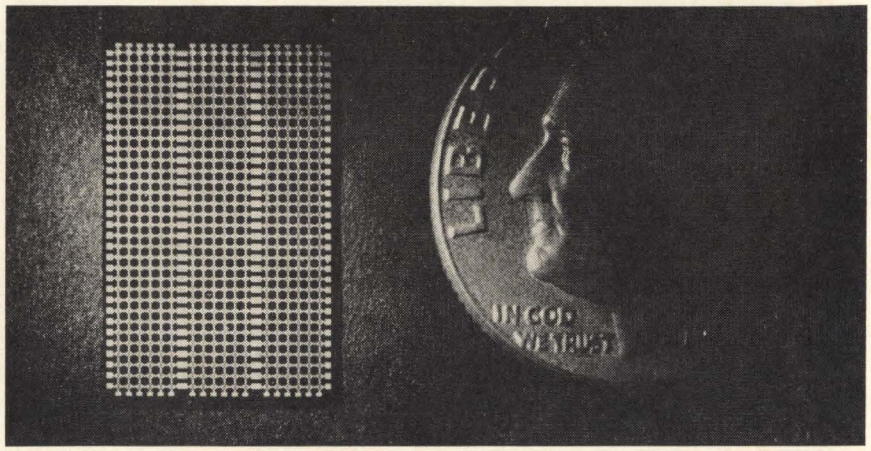
Two Fabri-Tek 4,096 x 12 memories. The larger one is the 1 usec. Series MF. Dwarfed is the 4 usec. Series MC compact memory. Of course, the big one has integral power supply, self-test, and many other features.

This Fabri-Tek memory incorporates high-reliability packaging techniques intended to extend the MTBF to from 7,000 to 10,000 hours. Typical applications for this memory are: use in industrial atmospheres, geophysical van-mounted systems, special-purpose aircraft, and military applications. Fabri-Tek has used MIL-E-16400 and MIL-E-5400 as development criteria. Ask for information about the Series MC memory system. Write: Fabri-Tek Incorporated, Amery, Wisconsin. Call: 715-268-7155. TWX: 510-376-1710.

FABRI-TEK INCORPORATED

CIRCLE NO. 19 ON INQUIRY CARD

DIGITAL DATA RECORDING HEAD AS ONE LARGE INTEGRATED CIRCUIT



Light emitting diode array, designed for application as a digital data recording head, contains 576 separate diodes on a single monolithic silicon chip.

Integrated circuit technology has been applied to the digital data recording field by scientists at Fairchild Semiconductor's research and development laboratory resulting in the fabrication of a monolithic silicon array of 576 separate light-emitting diodes on a single chip of material barely 5/8" square. The array of light-emitting diodes is believed to represent the largest integrated circuit ever delivered and contains more active elements than any other circuit described in current reports.

Designed to record digital data on photographic film, the diodes in the array are operated in the reverse bias mode. With a dc voltage source between 5.8 and 13.3 volts, the maximum pulse length is 160 msec at 25 ma or 10 msec at 100 ma. Duty cycle is 50%. Approximate black-body-equivalent color temperature of the emitted light is 2500°K. Intensity is sufficient to expose panchromatic type film to saturation with a 3-msec pulse when the diode-to-film space is 0.001". Light emission can be seen with the unaided eye in a dimly-lighted room. Geometry of the diode array conforms to the standard military reconnaissance data bloc pattern (Mil. Std. 782). Diodes are arranged in three adjacent 6-column, 32-row arrays to form an 18 by 32 diode matrix. Center-to-center spacing of the diodes is 0.018" each way, and the individual diodes are 0.002" square. Electrical connection is made via 18 anode leads and 32 cathode leads which are brought out of the sensor head assembly via multiple-conductor cable and terminated in a plug.

First deliveries of the new light-emitting diode array, called the Fairchild FLPA-200, have been made to Fairchild Space and Defense Systems for photographic reconnaissance equipment in which the array records required digital data in a corner of each frame of film as it passes through the camera's optical system. Previous methods of accomplishing this data recording task involved cathode-ray tubes and close-tolerance optical systems which were subject to many alignment and interference problems. With the new solid-state array, which uses no optical systems at all, alignment and adjustment problems are said to have been eliminated and system reliability has increased.

Fairchild is prepared to fabricate appropriate sensor arrays to match the light-emitting array, should a potential user desire that type of operation.

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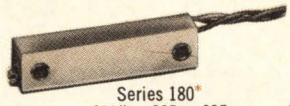

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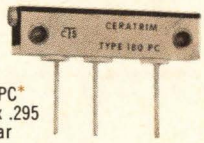

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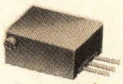
Rectilinear

Series 170*
½" Square



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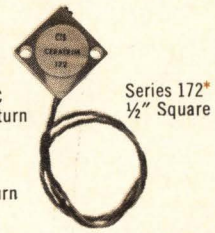
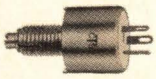
½" Square

Series 660PC
⅜" dia., single turn



Series 172*
½" Square



Series 600LT*
½" dia., single turn,
locking bushing

Series 630
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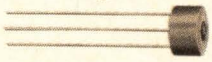

Series 385*
11/32" dia., single turn

Wirewound Trimmers

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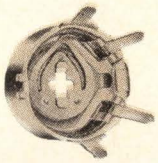
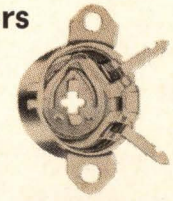
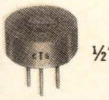


Series 110*
¾" dia., single turn

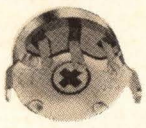


Series 112*
¾" dia., single turn



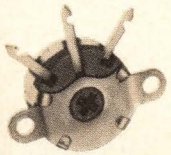
Series 350*
½" dia., single turn

Series XPC110
¾" dia., single turn



Series P115*
¾" dia., single turn

Series 115
¾" dia., single turn



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Series IRW
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spiral infinite resolution

Series 160
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Rectilinear

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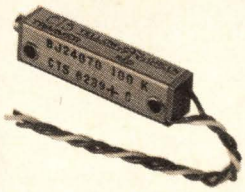
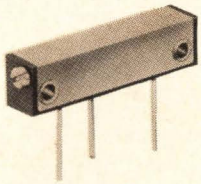


Series C140*
1¼" x .325 x .295
Rectilinear



Series C140PC*
1¼" x .325 x .295
Rectilinear

Series 220*
7/16" x ½" single turn

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19/32" dia., knob operated,
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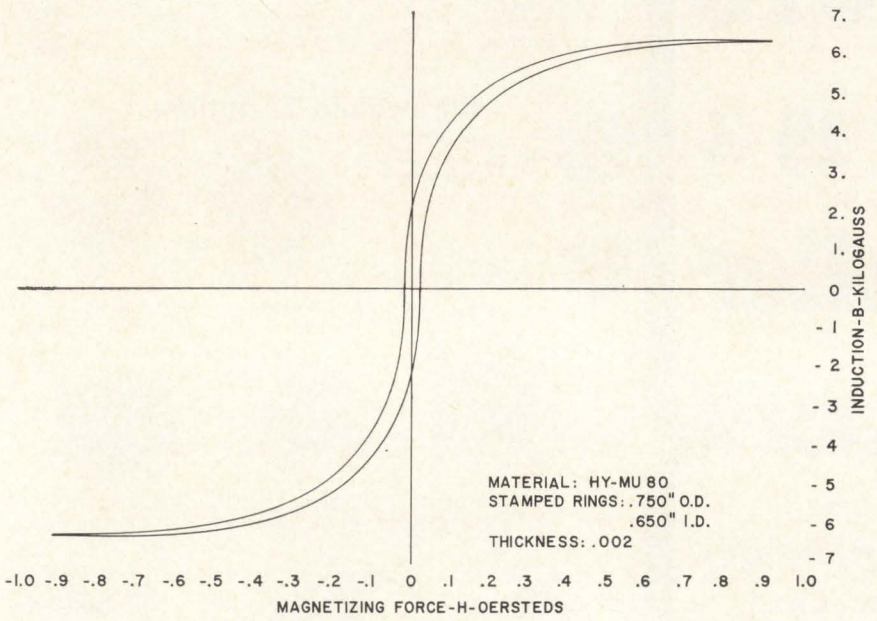
CIRCLE NO. 21 ON INQUIRY CARD

Considerations on the Use of Laminated Cores for Computer Reproducer Heads

The Lamination Approach Is Said to Permit Smaller Designs While Increasing the Number of Channels

Melvin L. Fraley, *Chief Engineer*
Haddon Tool & Manufacturing Co., Pennsauken, New Jersey



Hysteresis loop of Hi-Mu 80.

The recent use of laminated cores for computer reproducer heads has indicated that these new cores can provide the design engineer with several desirable performance, testing, and production features. After an extensive study of the various core materials, it has been found that high nickel alloy exhibits several beneficial characteristics, such as very high permeabilities at very low values of magnetizing force and very low hysteresis losses.

A high nickel alloy, such as Hi-Mu "80", can be chemically analyzed as 0.05% carbon, 0.15% silicon, 0.50% manganese, 4.0% molybdenum, and 79% nickel, with the remainder being iron. The important magnetic properties of Hi-Mu "80" are a coercive force, from saturation, of 0.02 to 0.05 oersted, and a hysteresis loss, from saturation of 34 to 41 ergs/gm^3/cycle.

Lamination Solves Eddy-Current Losses

Nickel alloys have lower resistivity values than other materials, such as silicon steel, and, therefore, higher eddy-current losses. But these losses can be significantly reduced through lamination. The lamination planes are parallel to the direction of the flux and individual laminations are electrically-insulated. By reducing the thickness of each lamination section and increasing the number of sections, so as to keep a steady volume, eddy-current losses are substantially reduced. Under these conditions, the eddy-current loss varies as the square of the lamination thickness.

For example, a recommended thickness of a single Hi-Mu lamination for use in a computer reproducer head is 0.002". This includes the nominal thickness of the electrically-insulating surface. If the thickness of the reproducer head is to be 0.010, then five laminations would be utilized. This would reduce the eddy-current loss of the lamination (in comparison to a solid core of the same material) by the factor of 25, yet would retain the advantages of high permeability at low magnetizing force and low hysteresis loss.

In addition to the performance advantages, there are many other beneficial features offered to the design engineer when he incorporates a laminated core into a system. The efficiency of a laminated core approach permits smaller design packages and increases the number of channels for a given reproducer head size. From the viewpoint of design development work, a single die can fabricate dimensionally identical cores of different alloy materials, permitting experimental comparison of reproducer heads and design trade-off considerations with the core material as the parameter.

Looking at laminated cores from a production standpoint, quick-reaction reproducer head improvements can be accomplished as new alloys become available, without additional tooling or altering of dies. With the use of laminated cores, new core materials can be incorporated into test equipment for final evaluation with a minimum of delay and expense. And working with strip material offers the advantage of being able to determine certain electromagnetic characteristics using a standard shape, such as a ring, before the expense of producing more complicated shapes for final "in equipment" tests.

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Rugged, durable gallium arsenide light sources are used in the new Litton solid-state optical encoders, guaranteeing exceptional reliability under extreme environments. Tungsten lamp instabilities and failures—a chronic problem with conventional photoelectronic shaft-to-digital encoding devices—are eliminated. Both power consumption and heat dissipation are far less than for comparable ordinary optical devices. MTBF—very conservatively rated—is 30,000 hours. ■ ■ The high reliability of all Litton solid-state encoders under adverse conditions is exemplified by the 2^{11} incremental Model No. IN35-11G1 shown. It operates dependably and accurately during 70-g shocks and recovers from 105-g shocks. The case, including associated electronics, is size 35. Operating speed is 480 rpm. Other environmental characteristics meet or exceed applicable military specifications. ■ ■ While especially well suited to applications employing incremental positioning devices, the Litton solid-state optical encoding technique can be applied to absolute position encoders and any code pattern. ■ ■ For details, write: 7942 Woodley Ave., Van Nuys, California. Phone 213-781-2111. New York: 212-524-4727. Chicago: 312-775-6697. ■ ■ ■ ■ ■ ■ ■

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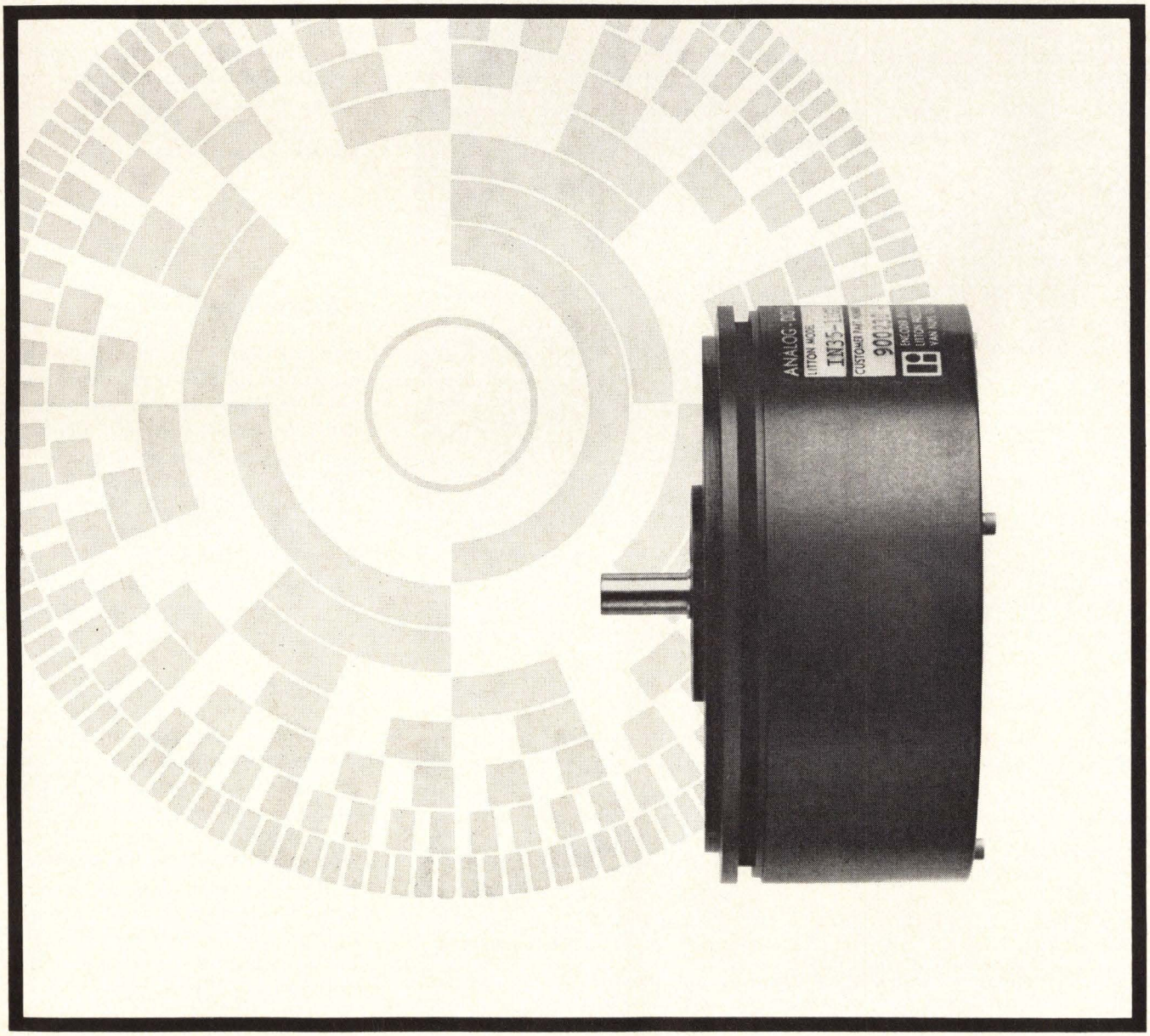

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Dr. A. Mary Tropper,
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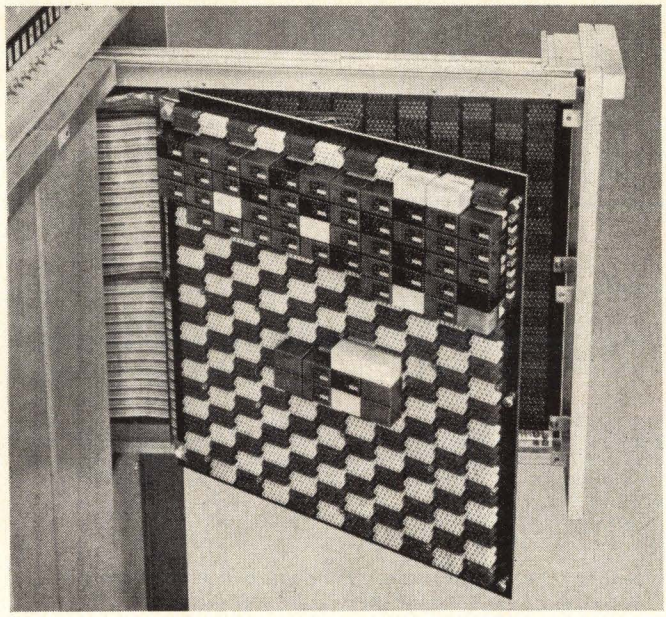
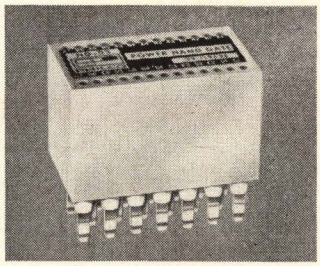


(In the field, the response to the standard 26-pin module is almost invariably "Beautiful!") The modules are available in a variety of standard-function circuits and can be designed for custom-circuit needs. Support hardware includes racks that will accommodate up to 3,420 modules...over 10,000 circuits. We are prepared to furnish complete software, including computer tapes for automatic wiring of your system. We think it's an unbeatable modular system for ground computers, command, timing, input/output, data acquisition and processing, automated check-out, safety monitoring, and mobile equipment.



We recognize, however, that no single modular system, however versatile and cunningly conceived, can possibly be *the* optimum system for every possible user need.

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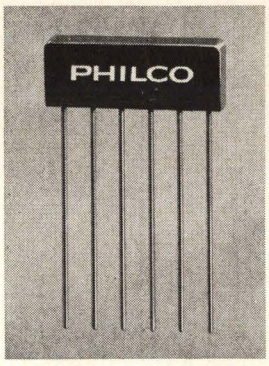

We are not wedded, either, to a single technology. If your concept hinges upon integrated circuits, fine. But if hybrid circuits better meet your needs—in terms of cost, performance of quantity—we're happy to oblige.

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CIRCLE NO. 24 ON INQUIRY CARD

By providing an output that represents both the amount and position of light on its surface, an experimental unit may extend the use of optical scanning in remote data collection terminals as well as simpler, less expensive central scanning installations.

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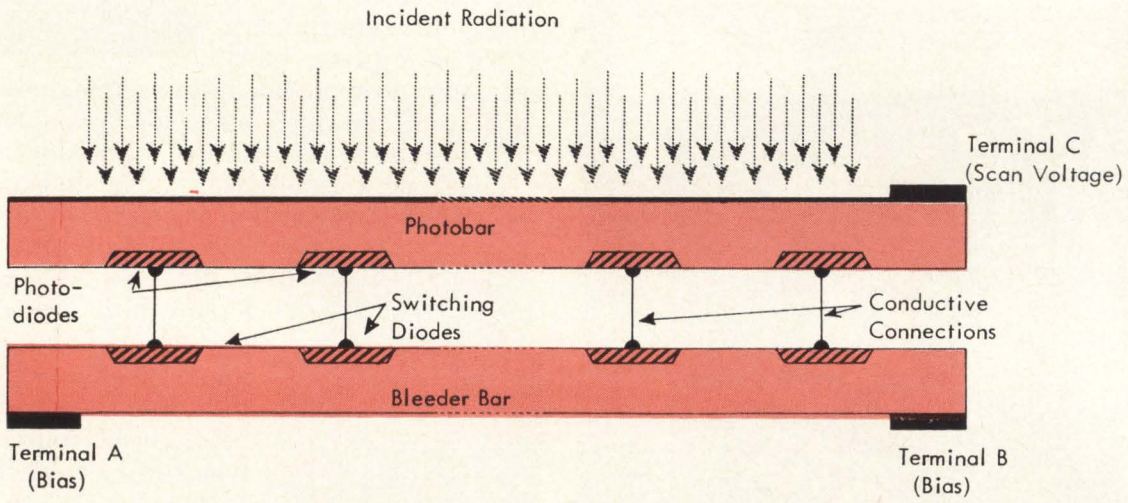

Fig. 1. Two bars of germanium, silicon, or other semiconductor material form the Scanistor's top and bottom surfaces. These are the photobar and bleeder bar shown in the drawing. Dots of opposite type (P or N) semiconductor, alloyed or diffused into the inner surfaces of the bars, form diodes which are connected in pairs. One diode in each pair acts as a photodiode to measure the light intensity on that part of the Scanistor. The other diode is a switching diode which connects its photodiode to the output circuit at a particular value of scanning voltage. Scanistors can be fabricated in a wide range of sizes, shapes, resolutions, and spectral sensitivities. Sensitivity depends on the materials of which the Scanistor is made, the scanning speed, and the wavelength of the radiation being sensed. The sensitivity of experimental silicon photodiode Scanistors is equivalent to that of a good silicon photocell. These Scanistors give an output of 0.5 ampere per watt of incident light with a wavelength of 9,000 angstroms. For very low light applications, an experimental super-sensitive Scanistor has been developed which makes use of the greater sensitivity of photoconductive materials. This version substitutes photoresistors made of materials such as cadmium sulphide for the photodiodes. IBM silicon Scanistors are sensitive to visible and near infrared radiation with wavelengths between about 4,000 and 11,000 angstroms. Other units, designed especially for best response to near infrared radiation might employ indium antimonide photodiodes or lead sulphide photoresistors. By choosing suitable materials, other Scanistors could be made sensitive to far infrared or even to x-rays. Scanistor response rates of several million resolvable elements per second have been demonstrated in the laboratory. For example, units with 75 diode-pairs have been operated successfully with scan durations as short as 10 microseconds.

An experimental solid-state optical scanning device which converts images into electrical signals has been developed by IBM Corp. The dime-size device, called the Scanistor, combines high resolution and fast response with other advantages of solid-state electronics — low power operation, small size and weight, long life, and simple circuitry.

The Scanistor differs significantly from earlier solid-state light-sensitive devices such as the photocells used in electric-eye cameras. Because these cells sense only the total amount of light falling on their surface, detecting a pattern requires many cells, arranged in-line or in a mosaic pattern, and a corresponding number of output amplifiers.

In contrast, the Scanistor provides, on a single output wire, an analog voltage that represents both the amount and position of light shining on its surface. Or, with different operating voltages, the Scanistor can provide a series of corresponding electrical pulses for entry into a digital computer. The construction of the Scanistor and its operation are described in Figs. 1 and 2. A photo of the device is shown in Fig. 3.

All of the Scanistors built to date have been one-dimensional, detecting the light pattern along a single line such as one scan line of a television picture. However, there are several ways that the Scanistor concept could be extended to detect a two-dimensional image such as a whole television picture.

In reading punched cards or tape, or printed documents, it is possible to move the image itself past the Scanistor to provide a complete scan of the image area. For example, IBM has experimented with a simple Scanistor system which converts typed text into electrical signals and displays the text on a TV-like screen. In this experiment, a card carrying a line of text is mounted on a rotating drum beneath a single-line Scanistor. Then, as the characters are swept past the Scanistor by drum rotation, the Scanistor electronically scans them from top to bottom.

To scan a stationary image, a moving mirror can be used to reflect the image, line-by-line, onto a Scanistor. Another approach is to mount

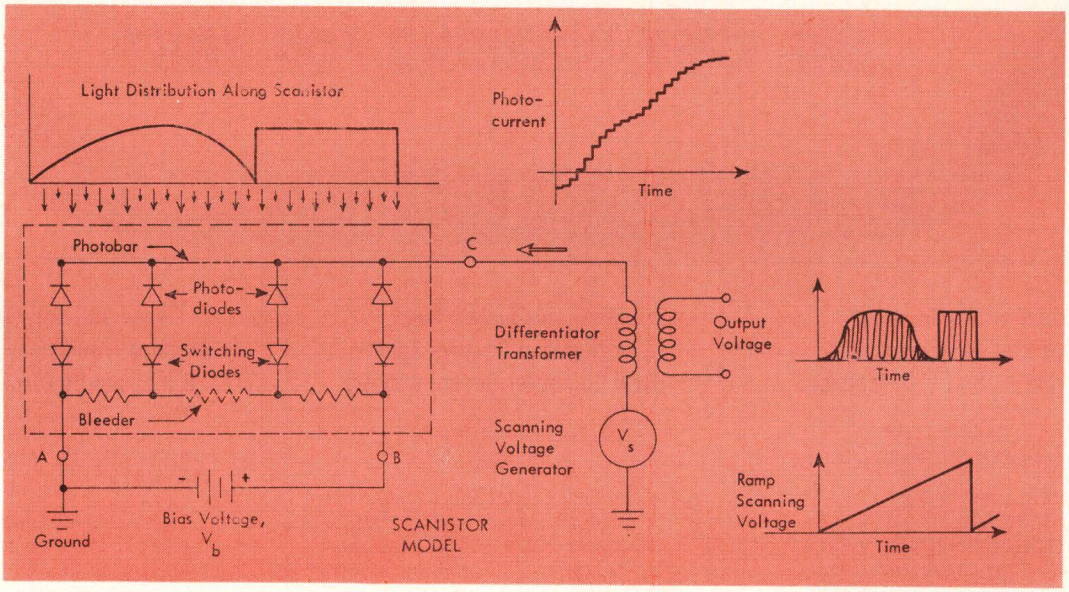

Fig. 2. A Scanistor can be thought of as a row of back-to-back diode-pairs, arranged so that one end of each pair is connected to a conducting "photobar", and the other end is connected to a resistive "bleeder". The diodes connected to the photobar act as photo-diodes and receive light from an image projected onto the upper surface of the Scanistor. The diodes connected to the bleeder act as blocking, or switching, diodes to control the scanning of the image. Two terminals attached to the ends of the bleeder receive a fixed bias voltage V_b (typically six volts). The bleeder acts as a voltage divider, and each blocking diode is returned to a different voltage, ranging from zero to V_b. A third terminal attached to the photobar receives a scanning voltage V_s. Electronic scanning is performed by making V_s a linear ramp voltage that increases at a constant rate from zero to the value of V_b. At the start of a scan, when the scanning voltage is zero, all of the blocking diodes are reverse-biased by the bias voltage, and only a small leakage current flows through them. But as the scanning voltage increases, the blocking diodes are forward-biased for easy conduction, one after another. As each additional blocking diode is switched on by the scanning voltage, the amount of additional current flowing through it from the photobar to the bleeder depends on that state of the associated back-biased photodiode. The leakage current through this diode is proportional to the amount of light falling on its active surface. Thus the amount of additional current switched between the photobar and the bleeder depends on the amount of light falling on that part of the Scanistor. Since it is the change in current that is proportional to the light, the photobar current is passed through a differentiator circuit which can be a series inductor or transformer. With relatively large values of bias voltage V_b, the output from the differentiator is a series of pulses, the height of each being proportional to the light on one of the photo-diodes. Lower values of V_b give a smooth output voltage representing the light distribution along the Scanistor.

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For information check Motorola type MC352-MC361 MECL integrated circuits.

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For information check Motorola PNP type 2N3743 and NPN type 2N3742.

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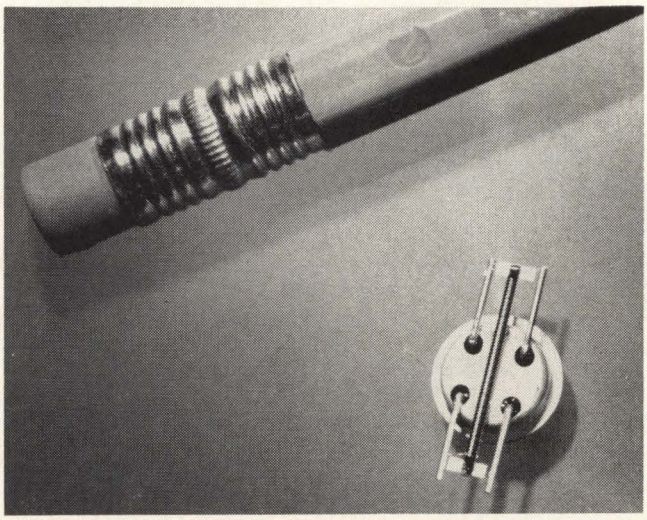

Fig. 3. The Scanistor shown here is one-half inch long, and contains 100 light-sensitive diodes paired with 100 switching diodes. These diode-pairs are spaced 0.005 inch apart to give a resolution of 200 image elements per inch.

several Scanistors side-by-side and combine their outputs into one picture.

IBM engineers believe it may eventually be possible to fabricate a folded Scanistor that provides a TV-like raster scan, or a mosaic Scanistor that scans in two directions at once.

To illustrate one approach to a character recognition application, eight Scanistors have been assembled into a special pattern to recognize constrained handwriting — both numbers and letters. For reading, cards on which characters have been written are fed into a converted card punch machine which projects each character image onto the Scanistors. Characters are recognized by determining which Scanistors their image intersects.

IBM engineers believe that Scanistors could also be used in other types of character recognition machines that scan the entire text area or trace out character patterns. With simple Scanistor scanners to convert printed or handwritten characters into electrical signals, one set of recognition logic at a central location could serve many input terminals in remote locations.

IBM Scanistors made of silicon are sensitive to both ordinary light and near infrared radiation. Similar units fabricated from other semiconductor materials could be made sensitive to far infrared, thus overcoming a limitation of vacuum tube scanners, as orthicons and vidicons.

Although the Scanistor is experimental and not commercially available, IBM has tested sample units in such applications as document and film scanning, character recognition, and reading punched and mark-sense cards.

Looking ahead, here are a few of the possible future uses for Scanistors that IBM engineers have suggested:

- A hand-held "reading" device which could be passed over a line of printed text to enter data into a computer
- Small remote terminals at which information could be written directly into a data processing system
- A simple position sensor requiring no standby electrical power to relay the readings of thermometers or other instruments to a central location
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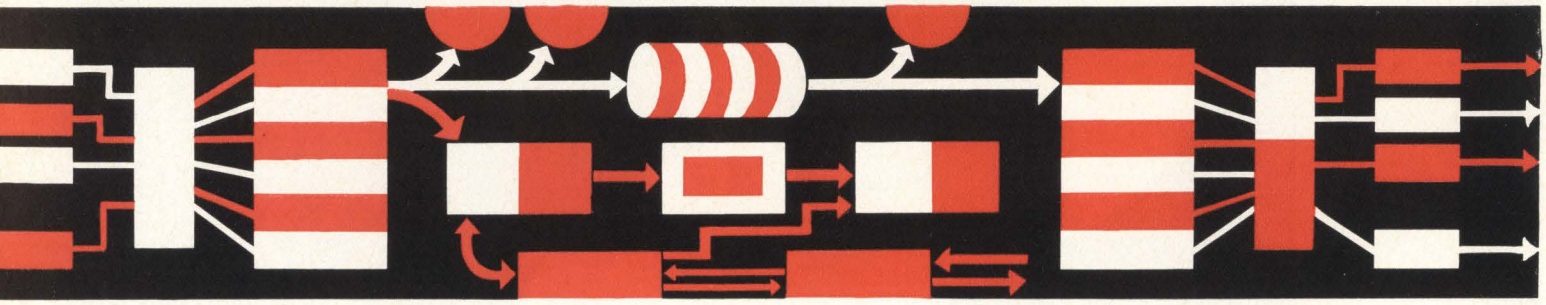
Design Guide For Computer-Communications Systems



PART 2 – EQUIPMENT SELECTION CONSIDERATIONS

Selection of an equipment configuration is a major milestone in the design of any data processing system. The decision to choose a particular equipment configuration is not made lightly because it involves a major financial commitment. Errors in equipment selection, unlike programming errors, are very visible.

The equipment selection problem is complex since many types of factors must be considered. The primary technical problem is the determination of the capability of a configuration to handle the expected traffic load. Such a determination is usually made by selecting a candidate system and developing the programming of that system for the expected traffic load until it is reasonably clear whether or not the equipment can handle the job. Time permitting, this process is applied to several different systems and a final choice made from all systems that qualify, depending on such factors as safety margin, expandability, cost, standardization, etc.

The foregoing remarks imply that equipment selection is primarily a problem in programming analysis. In today's computer market with broad product lines of compatible processors and peripheral equipment, this is largely so. The equipment is generally available for most applications, and it is sufficient to "size" a system for a problem with a reasonable safety margin. There is, however, an important element of the equipment configuration of computer-communications systems for which this is not so: The Communications Interface Sub-System.

The Communications Interface is a collection of equipment and programs that generally serve to integrate the data lines with the central processor of the computer system. While all computer manufacturers today furnish equipment to implement this function, there are almost as many different approaches as there are computers. Furthermore, the differences between these approaches are definitely significant to the potential user. It is, therefore, necessary for the system designer to evaluate the internal design of alternative Communications Interface Sub-Systems with great care or run the risk of selecting a grossly inefficient or perhaps inoperable system.

Editor's Note: *Part 1 of this series, in the March 1965 issue, introduced the basic system concepts of computer-communications systems. Here in Part 2, the authors describe the functions of the Communications Interface Sub-System and evaluate the techniques available for implementing them.*

Here in Part 2 of this series, the functions, primary economic problems, and implementation techniques for the Communications Interface Sub-System will be discussed in generic terms.

Computer-communications systems require equipment configurations that are generally more complex than required for off-line applications. A typical system usually contains at least one of each basic type of computer system component found in off-line applications plus a number of special purpose components found only in on-line systems. In the former category are found proces-

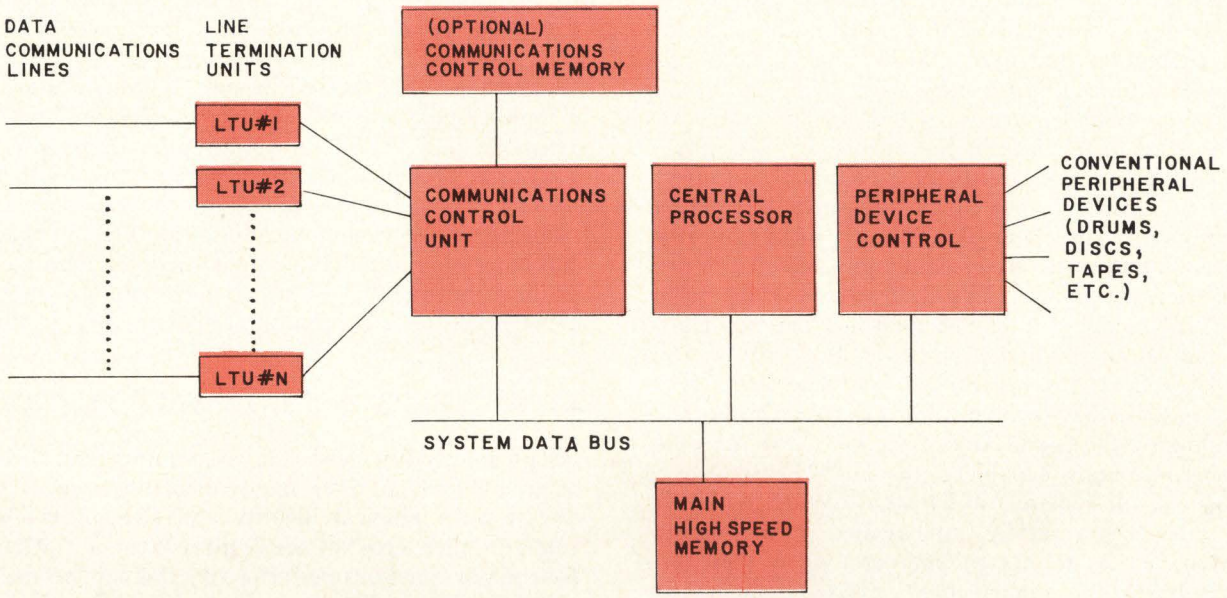


Fig. 1 Basic organization of a computer-communications center (simplex system — no redundancy).

sors, core memories, drums or discs, tape stations, printers, card or paper tape reader/punches, etc. In the latter category are found special inquiry and display devices and, of primary importance, the elements of the Communications Interface.

Fig. 1 is a highly simplified block diagram of a generic computer-communications system. In this simple system, the Communications Interface consists of the Line Termination Units, the Communications Control Unit with its optional Control Memory, and a portion of the time and memory of the Central Processor.

In a very simple sense, the Communications Interface is a device that makes a collection of data lines appear to the programs of the Central Processor as another set of conventional computer peripheral devices. To the extent that this concept is valid, the Communications Interface can be viewed as analogous to the Peripheral Device Control Unit at the other end of the system data bus. However, this analogy holds only at a very high level of abstraction because the detailed requirements of the Communications Interface are quite unique.

COMPONENTS OF THE COMMUNICATIONS INTERFACE

The Communications Interface consists of four basic elements. Two of them — the **Line Termination Units** and the **Communications Control Unit** — are always physically distinct from the remainder of the system. The other two elements are sometimes distinct and sometimes exist only as portions of the Central Processor's capability. They are the **Control Memory** and the **High Level Control Procedures.**

The Line Termination Units (LTU) provide the electrical and logical connection with the data lines. One LTU is normally provided for each line. Its functions are the most elementary ones possible in order for the computer system to exchange data with the communications lines. As a minimum, the LTU has the capability for exchanging bits between the computer and the data line. At maximum, it may have storage capacity for one or two characters, independent clocking control for the data line, and some elementary channel control ability.

The Communications Control Unit (CCU) is a scanning device which sequentially inspects each LTU to determine if activity is required and, when necessary, causes appropriate data processing functions to be executed. In its simplest form, the CCU acts as a scanning switch between the LTUs and the Central Processor. The CCU's capability is limited to generating a program interrupt in the Central Processor whenever it detects an LTU in need of service. In its more complex forms, the CCU may have substantial internal processing ability including such functions as code conversion, data block assembly or disassembly, and initiation of channel control procedures. The CCU may be a fixed function logic-net sub-system or a stored program processor. In either case, for the CCU to execute functions of any reasonable degree of complexity, it requires a Control Memory.

The Communications Control Memory may be physically implemented either as an independent storage subsection of the CCU or as a reserved area in the Main

Memory of the system. In either case, its basic task is to hold a small quantity of information about the status of each communications channel. This information is conveniently thought of as a list of Control Words, one for each communications line. Each time the CCU investigates the status of a particular LTU (and hence the data line itself) it first obtains the proper control word from the list, uses that word to determine the allowable set of actions for that particular channel, performs the correct data processing function, updates the contents of the control word if necessary, and finally returns the control word to its place in the memory.

The CCU is usually restricted functionally to operations that are simple but highly repetitive. Communications control functions that are complex and used relatively infrequently are generally implemented in programs that run in the Central Processor. Such infrequent and complex functions, which typically include Bulk Data Buffering and Channel Control, are referred to as High Level Control Procedures. The term "High Level" is somewhat relative from one system to another depending on the complexity of the CCU. If the CCU has stored-program capability, the High Level Control Procedures will generally all be implemented within it; if not, they are generally implemented in the Central Processor. There are exceptional cases where these procedures have been implemented in fixed logic in the CCU, but they are not of general interest.

The CCU communicates with the Central Processor through the same type of mechanism as is normally used for peripheral device control: memory access requests interlaced with the normal running program (called "interrupts") and signals to the Processor calling for program termination. From this viewpoint the CCU is analogous to a peripheral device control that never stops. The constant presence of demands for Main Memory accesses due to the CCU, combined with the generally high level of peripheral device activity, creates significant problems in system design. Traffic jams can develop at the Main Memory and unless care is exercised in both equipment design and programming, breakdowns can occur from peripheral devices losing data because of excessive delay in getting access to the memory.

In most data-communications systems, the cost of the Communications Interface is quite substantial. Attempts to minimize this cost have led to a variety of implementation schemes. Each of these schemes involves a tradeoff between the four previously-defined elements of the Communications Interface. In the past, there has been a tendency to design these sub-systems so as to achieve cost minimization for a particular set of problems. While this is acceptable for custom projects, it has tended to produce a wide variety of sub-systems, each of which was very efficient for a particular type of communications problem but none of which was best (or even near best) for all types of these problems.

The most common cost tradeoff is that which occurs by making frequent use of the Communications Control Memory to eliminate components in the LTU's. It is a tradeoff between components replicated through a large number of LTU's and the time of the Control Memory. Since this Control Memory is usually a portion of the Main Memory of the system, the Central Processor is effectively deprived of time to perform its functions because of this tradeoff. To the extent that the Central Processor can afford to lose the time, the tradeoff is desirable, but in cases where the time is not available it may be the wrong approach.

It is particularly important to note that using a system design with an inappropriate cost tradeoff as previously suggested not only causes the Communications Interface to be inefficient, but may degrade the performance of the entire system. From the foregoing it should be clear that there are no simple rules for selection of a Communications Interface. The system design problem is therefore one of understanding techniques and their combinations and making the appropriate selection for a particular problem. The next section of this article will provide a detailed description of the functions of the elements of the Communications Interface, methods for mechanization of these functions, and considerations that go into the question of which technique (or combination) is best for a particular problem.

COMMUNICATIONS INTERFACE FUNCTIONS

As previously discussed, the Communications Interface is an assembly of four major elements, two of which always have physical identity and two of which may often be "alter egos" of the Central Processor. There are four major functions performed by this sub-system. Each of these functions listed below has a number of important sub-functions.

- Line Termination: clocking, scanning, and storage
- Code Recognition and Conversion: character sensing, and response generation
- Data Block Assembly and Disassembly
- Channel Control
- Bulk Data Buffering

There are a variety of ways to implement each of these functions and sub-functions and, considering the physical division of the elements of the system, there are a very large number of possible combinations of implementations. It is therefore desirable to first examine each of these functions and sub-functions separately and establish clearly what it does and what methods are individually available for its implementation before proceeding to a discussion of combinations. This examination is provided in the following sections.

LINE TERMINATION

The basic exchange of data between communications lines and the computer is called Line Termination. The Communications Interface must provide this function for a large number of lines simultaneously. The need to service a number of communication lines which operate independently of each other and of the processor timing brings up three problems:

- When to look at each incoming line to recognize each bit? (clocking)
- How often to service each line to accept incoming data? (scanning)
- How and where to store incoming data? (storage)

Similar or corresponding operations have to be performed on outgoing lines.

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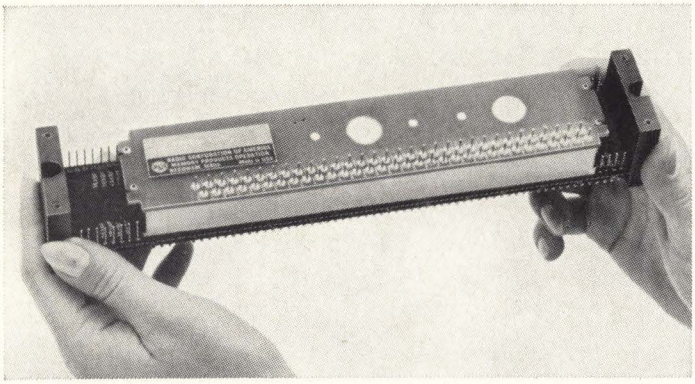

Vibration—10 g (0 to peak) 5 to 2000 to 5 cps at 1 minute/octave logarithmic sweeps, once along each of 3 mutually perpendicular axes.

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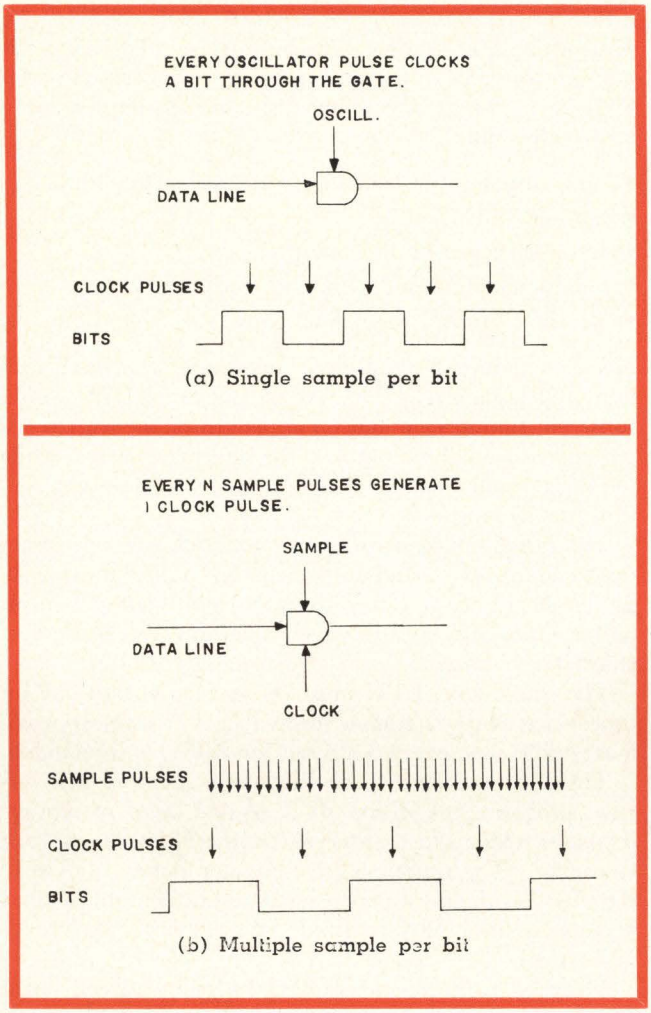
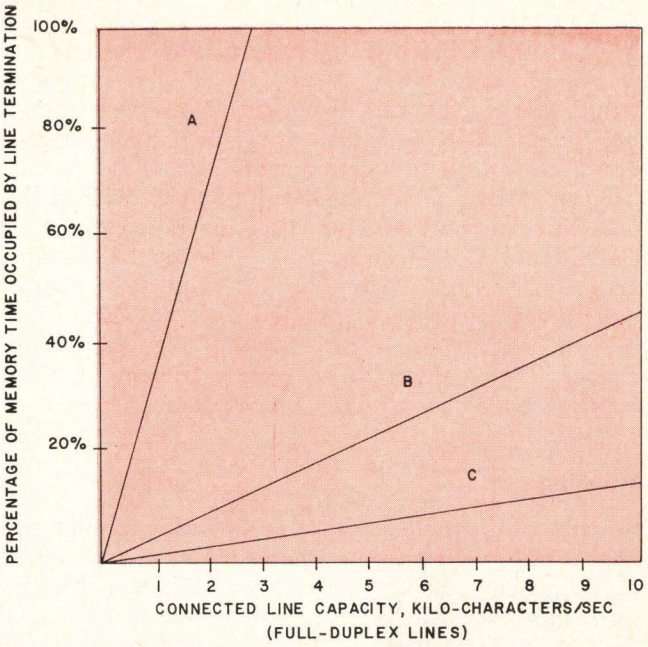


Fig. 2 Clocking techniques



A = Multiple scan per bit (20X) with direct bit transfer to memory

B = Single scan per bit with direct bit transfer to memory

C = Single or double character shift register storage with transfer of characters to or from memory

Fig. 3 Memory time requirements for various Line Termination techniques. Percentage time requirements are based on a 2 microsecond read/write memory cycle. For other cycle times, adjust figures in direct proportion.

The choice of techniques for performing these functions depends on technical as well as economical considerations, especially on the amount and complexity of service required and whether one prefers to pay for hardware rather than processor time.

Clocking

Clocking basically refers to the act of sampling each incoming line at a proper rate to recognize reliably each data bit. One or more samples per bit may be employed.

If a single sample per bit is used, the single sample pulse must be positioned at or close to the center of each bit to allow for the unavoidable signal distortion which results in transition shift, possibly over a large percentage of a bit interval. Two types of clocking are used: asynchronous or synchronous. Asynchronous clocking is employed on low-speed data lines where the terminal device is mechanical; usually a teletypewriter machine. Each character is individually framed with bits which convey no information. No common clock is required to synchronize the equipment at the ends of the data link. Synchronous clocking is used on higher performance data links. It employs either a common clock, or more usually, highly stable clocks at the terminal. As bit-by-bit synchronization is maintained between both ends of the data link for very long periods of time, no framing bits are required. More costly terminal equipment is required for synchronous transmission than for asynchronous, but greater line utilization can be obtained.

One of the main problems of single sample pulse generation is the need to provide the necessary circuitry and control logic separately for each line. For a system with a large number of lines, the cost of these replicated oscillators or counters is substantial. Multiple sampling techniques represent one method for reducing this cost.

The multiple sampling per bit technique requires the generation of a large number of sample pulses per bit, usually in the order of ten to twenty. They may be obtained from a common oscillator per speed group or from processor timing circuits. A count of the number of pulses sent to each line is maintained, starting from a given reference point (e.g., from the start transition in start-stop channels or from data transitions in synchronous channels).

Each time the Common Control logic inspects the data channel, the count is advanced. When the count is equal to the desired value, the system samples the data line and resets the count to zero. This high-frequency counting principle is illustrated in Fig. 2 which contrasts it with the more conventional single sampling technique.

To use this technique as a means for eliminating large amounts of hardware, it is necessary to store the counters (one per data line) in a memory. Since the counter has to be extracted from storage for every sample, a very high rate of memory accesses is required, e.g., about 1500

accesses/sec for a single 75 baud line sampled 20 times per bit, under the assumption that only one memory access per sample is needed. One hundred such lines would, therefore, require about 150,000 memory accesses per second, which is a major portion of the processor time for even the fastest computers available.

Since memory time is the key restriction on use of this otherwise attractive technique, consideration has been given to use of a special memory solely for the sampling operation. Since a separate memory with its own set of independent control logic is costly, the approach tends to be most appropriate for relatively large-scale applications. Fig. 3 shows the effect of different sampling techniques on memory time requirements.

Scanning

Scanning is the function of connecting each communication channel with the data storage and common control of the system sufficiently often to permit data transfer to be made without loss of incoming data or producing gaps on outgoing data. In its simplest form, a scanner might consist of a stepping switch which connects one channel at a time with the memory and control interchange of the processor. A fixed scan sequence which is simple to mechanize is acceptable only when all channel speeds are equal or within a narrow range. If there are wide speed differences, low speed lines would be inspected unnecessarily in such a scanning scheme, possibly resulting in substantial waste of machine time, or interfere with other requirements for memory accesses. In cases of wide speed differences, a proportional or differential scan is generally necessary. The differential scan provides line inspection at a rate which is related to the channel speed.

Line Termination Storage

Data collected from inbound lines must be stored until significant quantities are available for higher level processing. On outbound lines, a complementary requirement exists. Several techniques are available for providing this storage. They differ in the time vs. hardware tradeoff. The two most common techniques — bit buffering and character buffering — are illustrated in Fig. 4.

The requirement for line termination hardware is minimized when single data bits are transferred between line and computer memory. No individual hardware storage per incoming line is required when multiple bit samples are used. Each bit is directly stored in the processor memory when the proper sample count is recognized. Outgoing lines, however, need some hardware storage to eliminate bit jitter.

When single-sample per bit is used, one hardware flip-flop is required for holding the bit until scan time, and one for storing the fact that a bit has arrived.

Line termination in the form of bit buffers is relatively simple and inexpensive as far as individual channel hardware is concerned. This simplicity, however, is obtained at the expense of complex communications control logic and, even more, at the expense of processor time because of the numerous memory accesses required for assembling bits to characters for incoming lines and disassembling characters to bits for outgoing lines.

Assembly or disassembly of bits to characters in transistor shift register buffers is a widely used technique for line terminating storage. The buffers are relatively costly but do not take much processor time for servicing. A single level character buffer consists, in its simplest form, of six elements:

- Shift register for accepting or transmitting data
- Sample pulse source
- Level changer or line adapter
- Character start and complete recognition logic
- Transfer control logic and gates

Fig. 4(b) shows a simplified diagram of the input section of a single level LTU. An output of an LTU would consist of similar elements. The length of the shift register depends on the length of the character codes, while the sample pulse source is determined by line speed and transmission mode.

The sample pulse sources, one for each line, are practically identical to those used in bit buffer units with single bit sampling. They are major cost elements in bit buffer units and contribute considerably to the cost of character buffers.

The single level LTU must be serviced within one bit time, once every character interval, e.g., within approximately 400 usec every 3.3 msec for 2400 baud channels.

This short response time can cause memory interference problems. Addition of a second level of storage increases the surface interval to the duration of one character. The double-level character buffer, shown in Fig. 4(c), is the most expensive type but is quite popular because of its ability to minimize memory interference problems.

To give an impression of the tradeoff between hardware and processor time for the three main LTU types, consider a system with 100 simplex teleprinter channels operating at 100 wpm, corresponding to a bit duration of approximately 13.4 msec and a character duration of 100 msec. This group of teleprinter channels imposes a load on the system of 1000 char./sec. or 7500 bits/sec. The hardware estimates for the various LTU types given below are "ballpark" figures based on existing equipment.

Item	Character Buffer	Bit Buffers	Multiple Sample (20 Samples/Bit)
No. of services/sec.	1000	7500	150,000
Msec. between services	1	0.13	0.0066
Transistor modules	4000-6000	2500-3500	400-600

It is quite obvious that from the standpoint of hardware requirements, the technique of multiple sampling per bit is very attractive but the demand on processor and memory time are rather extravagant. This technique will therefore be found only in such cases where special design considerations can reduce the impact of the high service rate of the communication lines and leave sufficient processor time to perform the main function of processing the data that enter and leave the system, or where the cost justifies a separate memory for the Line Termination storage functions.

CODE CONVERSION AND RECOGNITION

Although there is a trend toward universal use of the ASCII 8-bit code, there still exists a large quantity of

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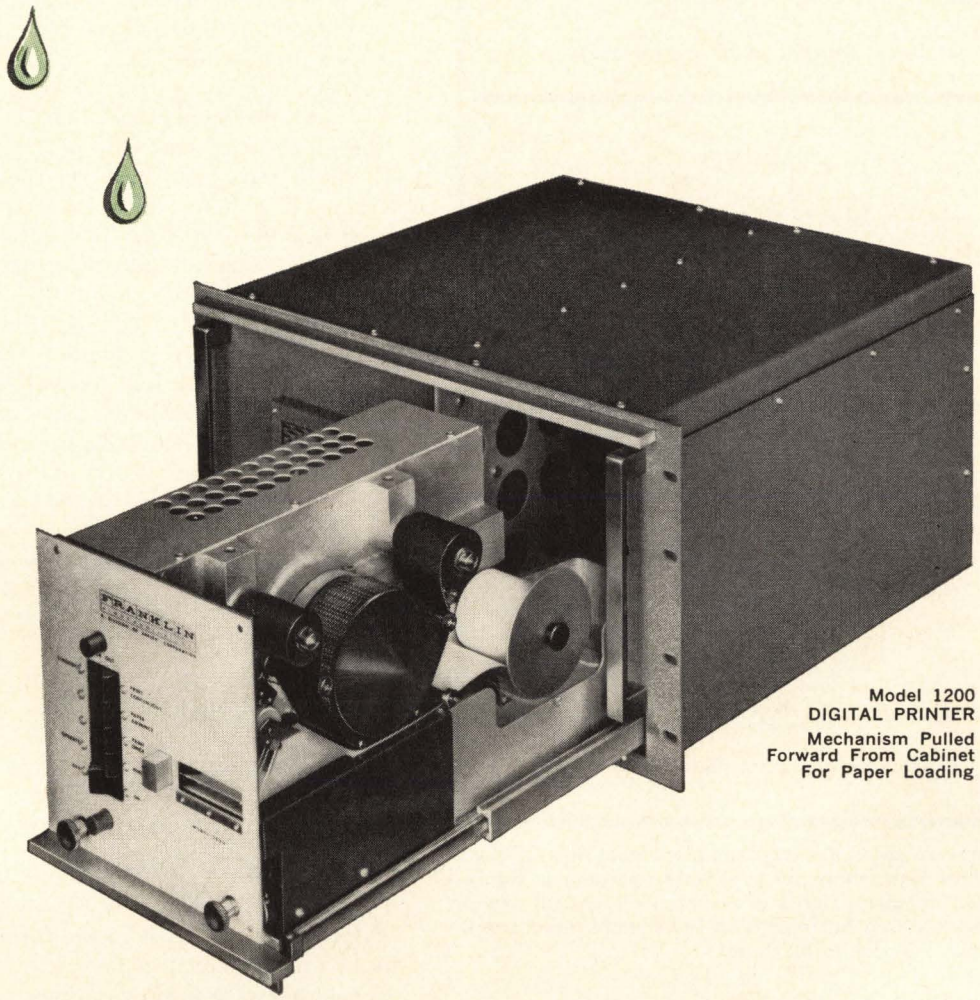

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COMMAND SIGNAL PROVISIONS: A wide range of input control and output command signals are provided for.

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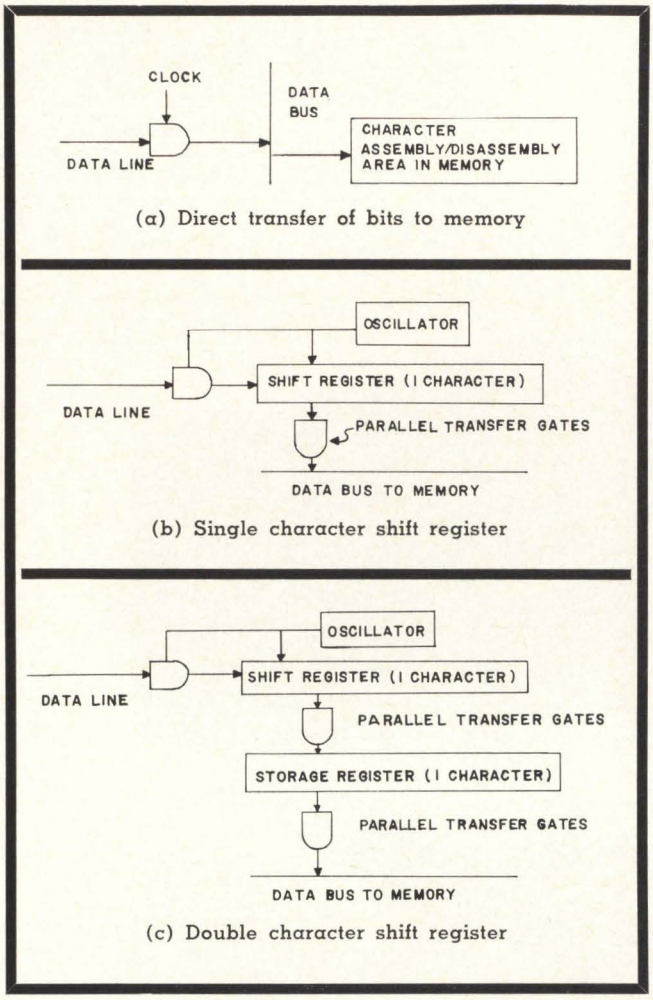

Fig. 4 Character assembly/disassembly techniques. (These drawings show only character assembly operations. Equipment required for disassembly is essentially identical except for the presence of a 2 bit register in the case of direct transfer of bits from memory to the line.)

terminal equipment utilizing a variety of other codes which must be accommodated. The most popular code is the 5-level Baudot code found in teleprinter equipment. This code is quite difficult to convert because each code group has two different meanings depending on the last preceding case shift character.

Code conversion can be accomplished by equipment in the Communication Interface or by program. Where time is at a premium, code conversion by logic networks is preferable. It is extremely fast but rather costly and inflexible, especially if a number of different codes must be converted, each requiring a different network. Additional hardware per line is required to store case shift conditions when Baudot codes have to be converted.

Table look-up techniques are considerably more flexible and change-of-code assignment or expansion can usually be done without great difficulty. The code to be converted is used directly to address a high speed memory location from which the corresponding converted character is obtained. This approach is economical in such cases where a sufficiently large memory is available which the conversion tables can share, otherwise, it might become quite costly in view of the high cost per bit of small memory systems.

When the system permits holding off the conversion process until data handling by the central processor can begin, code conversion by program may be considered. Code conversion instructions are available in certain computers, such as the RCA 301 and 3301, which make the process very efficient. In machines without any character handling instructions, code conversion by program can be prohibitively long.

Special problems exist when conversion between Baudot and other codes has to be performed. In this situation, the last received case shift character must be stored for each data line until the next case shift character occurs. The stored shift character may, for example, be used to address a different location in the code conversion table. The case shift characters are no longer present in the converted data.

Conversion to Baudot code from another code is even more difficult since it requires that shift characters be inserted. Original and converted data fields occupy memory areas of different size. Fig. 5 shows, in a simplified form, the flow diagram of a conversion from Baudot to another code. If this program were to operate on a data block already stored in memory it would take somewhere between 10 to 50 memory cycles per character, depending on processor features. This requirement is large enough to justify the cost of code conversion hardware.

CODE RECOGNITION

In order to maintain control over the proper operation of communication channels, data transmitted by a terminal station or a communication center:

- are coded for recognition of a majority of possible errors introduced on the transmission path
- have control signals in the form of special characters, or character sequences, inserted in appropriate positions of each message to provide some means of co-ordinating the operation of sender and receiver.

It is possible, in principle, to perform the necessary code and control character generation at the transmitter and their recognition at the receiving station by wired logic. This procedure is costly and inflexible; but more rapid than any other procedure. It is considerably more flexible, although more time consuming, to perform these functions by stored program in both the transmitter and receiver.

This problem is similar to Code Conversion since the same functions are required. It differs in that the computer is expected to take special action when certain characters are found in the data stream and this type of action is usually required without delay. In particular, code recognition for control purposes in dealing with high speed data channels (2400 bits/sec and up) generally requires implementation in the logic of the Communications Control Unit because of the delay that results from programmed inspection of the data in blocks.

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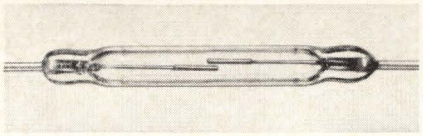

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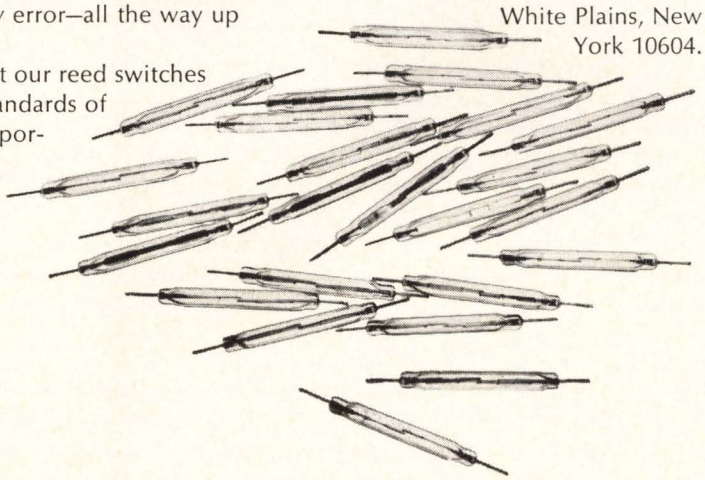

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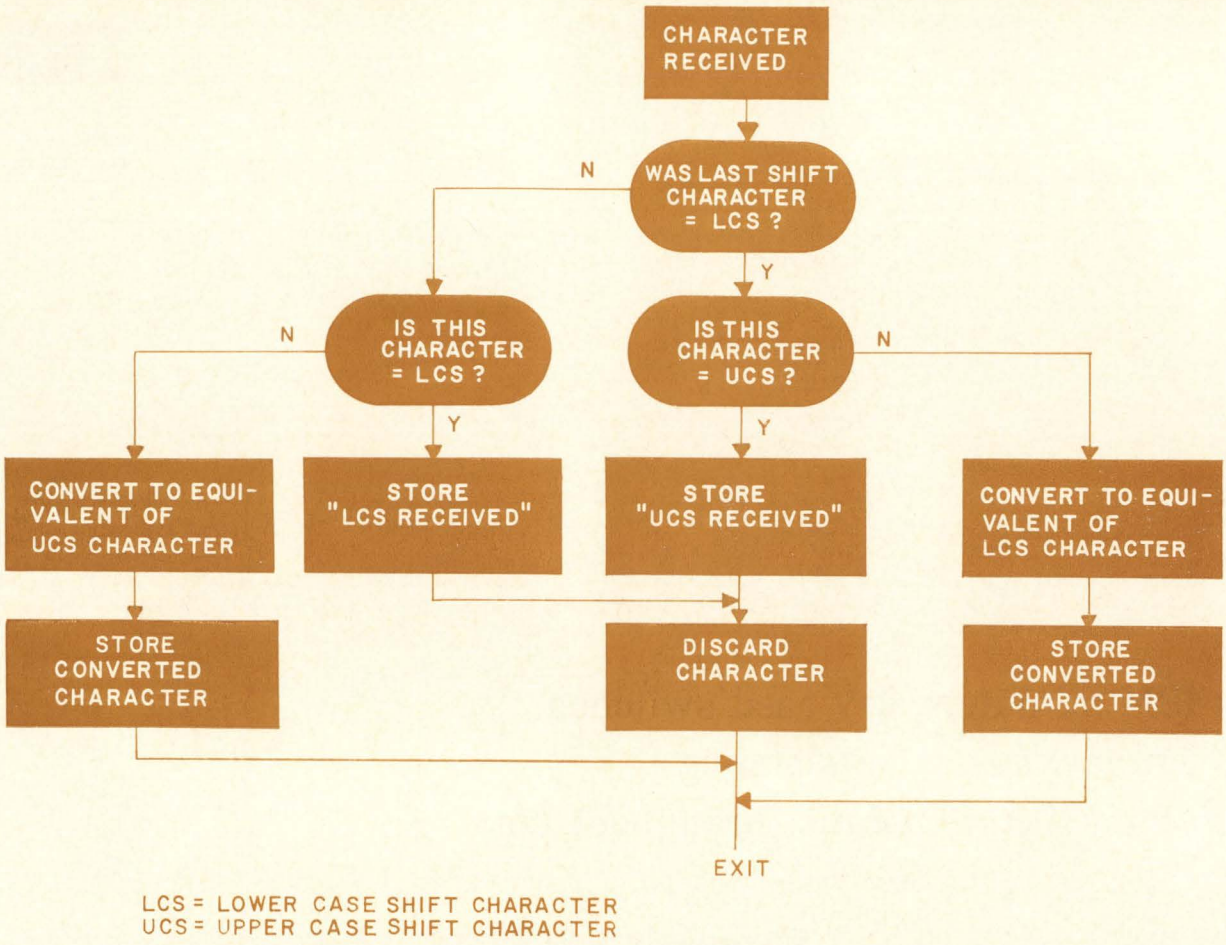

Fig. 5 Flowchart of programmed conversion from Baudot code (5-level) to code with 6 or more levels.

• Assembly/disassembly of bits to/from characters in either hardware registers or a memory location

• Assembly/disassembly of characters to/from data blocks in a bulk storage area in high speed memory.

The location of the block assembly/disassembly area is either in the high speed memory of the central processor or in a separate Communication Control memory.

Special hardware requirements are minimized if all data assembly/disassembly functions are performed by stored program in the central processor. The saving in hardware has to be paid for by a substantial amount of processor time. A somewhat more complex Communication Control directly controls the transfer of characters to and from the assembly/disassembly area. In the simplest case, there is a fixed memory area assigned to each line. This may be rather wasteful of memory space since these "line slots" are permanently occupied whether they are used or not. The transfer to and from these areas, however, requires only very simple logic, mostly for indexing and some means for informing the main processor when the assigned area needs to be cleared or refilled.

In more sophisticated systems, memory space for data assembly/disassembly is assigned on demand and is generally done by a program which informs the Communications Control which memory area it can use next. This method requires only a slight increase in control logic for the Communication Control Unit.

CHANNEL CONTROL

The data channel between the computer and the remote user is itself a complex system. As such, it requires control procedures, thus placing another requirement on the Communications Interface.

Control of data transmission is a major problem for communications channels for a number of specific reasons:

• Errors occur relatively frequently in transmission of data over long distances through a variety of facilities and transmission media

• As the computer system operator cannot see the remote terminal, he must rely completely on machine procedures to coordinate operation of the two equipments on either end of the data link.

• The remote terminal is often of a different manufacture than the computer and the latter must accept the burden of complementing the functions that exist in the terminal to achieve coordination. Furthermore, the computer may have to exchange data with several different

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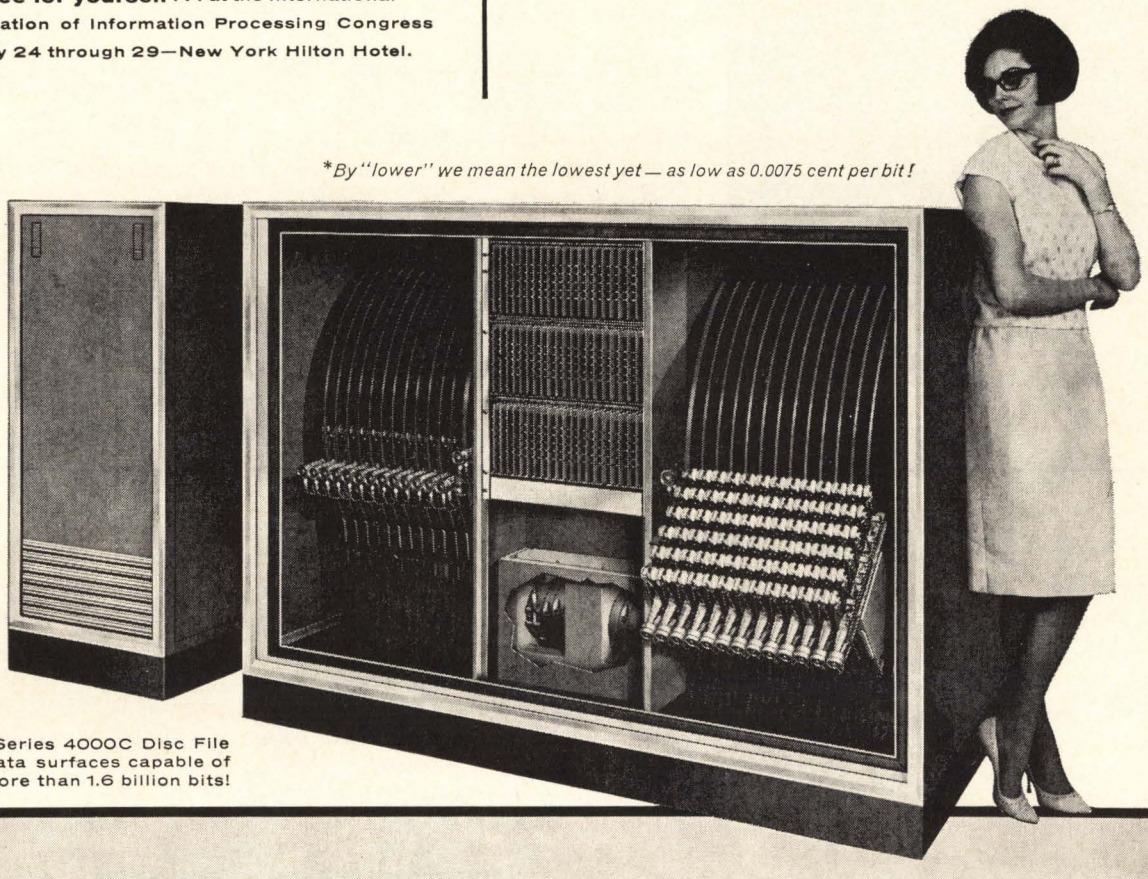

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types of terminals, each of which has a different set of functional requirements.

• The computer system is generally not in a position to schedule data exchanges with individual channels; it must honor service requests when demanded by the channels.

CHANNEL CONTROL FUNCTIONS

There are a large number of different channel control systems in existence today. While they have many principles in common, the specific differences are significant in their effect on the design of the computer system. Data channels can generally be classified by the degree of automatic control used. At the extremes of this scale are the "Fully-Controlled Channel" and the "Uncontrolled Channel." From the description of the principles of the two extreme cases, the characteristics of the intermediate type, the "Partially-Controlled Channel," can be easily inferred.

Fully-Controlled Channel Characteristics

Data transmission on a fully-controlled channel is subject to thorough checking and coordination. Error detection coding is usually applied to the data. The data is transmitted in short blocks and the recipient must acknowledge each block before the next one is sent. Each block of data is thus subject to either acknowledgement or rejection. The terminals at either end of the link are required to maintain positive control over the channel through the exchange of suitable coordinating signals. Control is applied on a character, data block, message, and channel basis. Every action is subject to positive acknowledgement before it can be considered successfully executed. The system is expensive but virtually foolproof and error-free.

Uncontrolled Channel Characteristics

Data transmission on an uncontrolled channel receives no checking or coordination. The data is not subjected to protective coding. It is transmitted in messages of indeterminant length and is not controlled through any type of acknowledgement procedure. The system is "cheap and dirty."

A more detailed examination of the problem of Channel Control reveals two basic classes of operations:

1. Operations performed on the data being transmitted
2. Operations performed because of the conditions of the data or the channel itself.

Operations performed on the data generally include:

• Inspection of the inbound data stream for errors and generation of appropriate signals upon recognition of an error

• Editing the inbound data stream to delete control

symbols that are not required by the next level of data processing

- Generation of control symbols to create the necessary format and error coding for outbound data transmission.

Operations performed because of the condition of the data or the channel include:

- Exchanging control information with the remote terminal, thereby causing it to perform certain operations. These control messages generally acknowledge successful receipt of a block or message or, conversely, reject it; call for repetition of a block or message, or if transmitting, indicate that a repetition is to be attempted; and direct the remote terminal to stop or start or, perhaps, change its mode of operation.
- Exchanging control information with the common carrier facilities in order to establish or break the data link; this type of procedure is required, for example, if the dial network is being used and dialing and line availability tests are necessary.

Implementation of Channel Control Procedures

There are a wide variety of techniques available for implementation of Channel Control procedures. At one extreme, these procedures may be accomplished fully by stored program control in the Central Processor. At the other extreme, they may be implemented by special purpose logic in the Communications Control Unit. Between these extremes there are many possible combinations.

The Fully-Programmed approach is very flexible and implies a low cost Communications Control. However, it is also very time-consuming and can become unworkable for this reason. With this approach it is possible for appreciable delays to build up between the time that a channel control function is required and the time it is executed. This characteristic can, again, make the approach unworkable except for relatively low-speed data transmission.

The Fully-Wired-Logic approach has the opposite characteristics of the Fully-Programmed approach. It is very fast, places practically no load on the Central Processor, but requires an expensive special-purpose Communications Control. This approach is virtually mandatory for very high speed data transmission. Its disadvantage, aside from the high cost of the Communications Control Unit, is lack of flexibility. Procedural changes may require physical modification to the Communications Control Unit and, to the extent that there are other ways to implement channel control procedures, this should be avoided.

The Combination approach attempts to find a judicious compromise between the Fully-Programmed and Fully-Wired approaches. The compromise is achieved by distribution of the functions between logic in the Communications Control Unit and programs that operate in the Central Processor. The basic principle of the compromise is to implement simple but frequently needed functions in the logic, and complex but low-frequency functions in the program. The major technical problem in using this approach is achievement of a balance of functions which is desirable for a wide variety of applications.

To provide a firmer understanding of the contrast be-

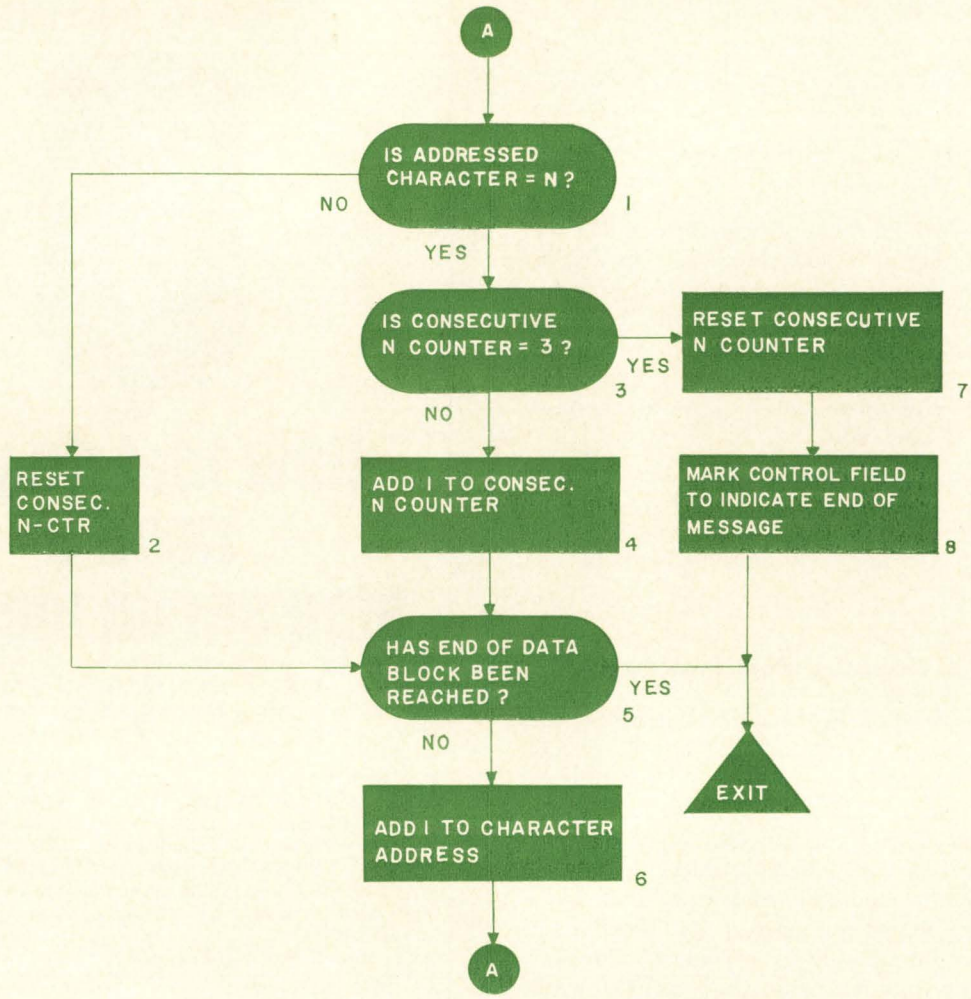


Fig. 6 (b) Flowchart of program necessary to detect "NNNN" sequence in data block stored memory.

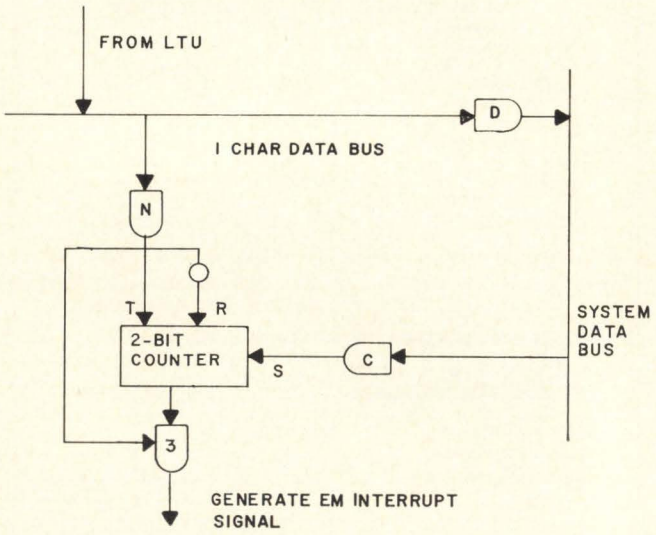
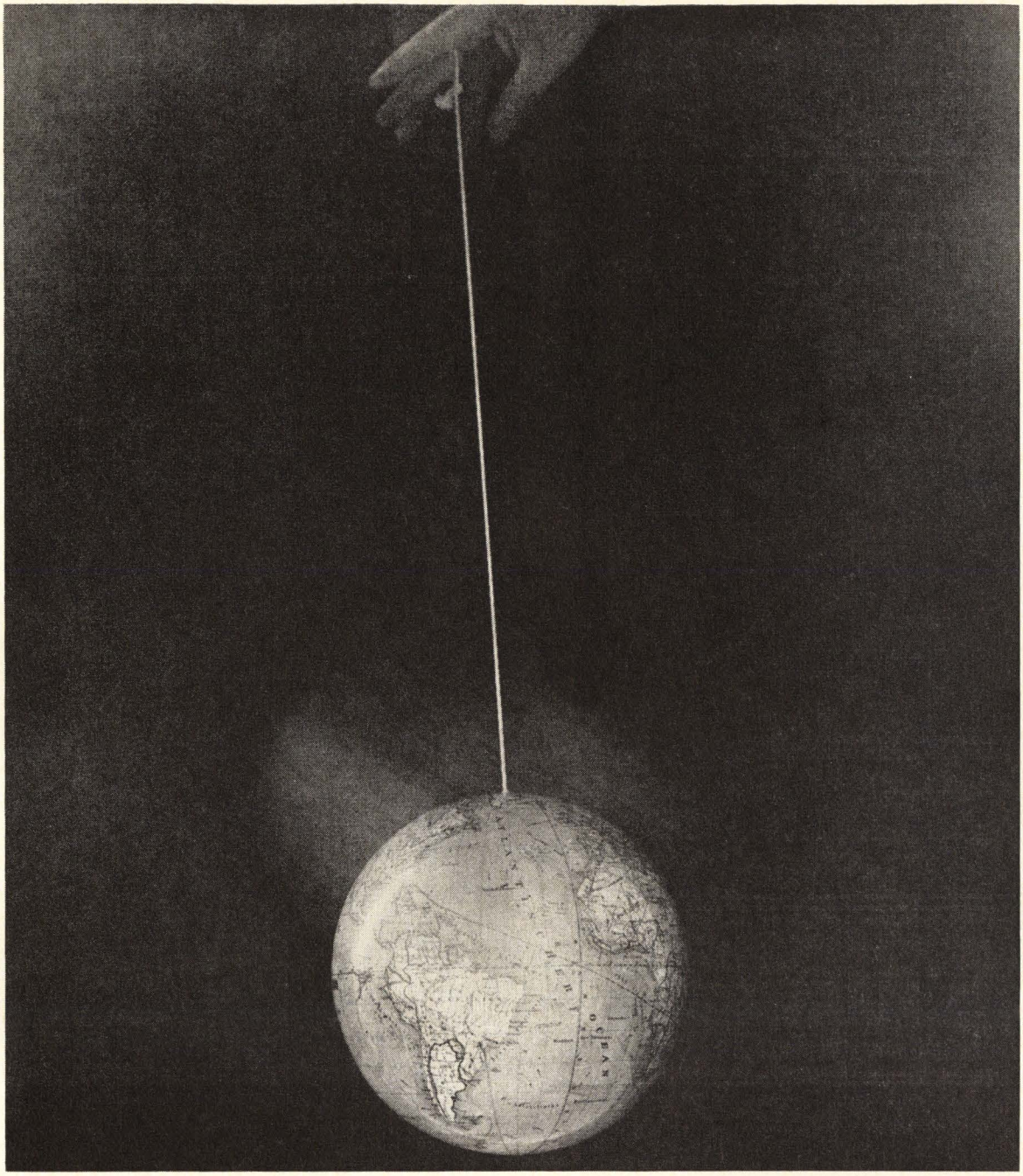


Fig 6 (a) Logic necessary in Communication Control to detect "NNNN" sequence.

tween these approaches, consider examples in Figs. 6 (a) and (b). Examples illustrate the two extreme approaches to one particular channel control function: the detection of an inbound End-of-Message sequence, "NNNN," commonly used in teletypewriter transmission. The problem arises because teletypewriter traffic is not transmitted in fixed length blocks so the computer must inspect each character of an inbound message to see if it is an "N" and, if so, start checking for a sequence of four consecutive "N"s.

Fig. 6(a) shows a simple logic sketch for implementation of this function in the Communications Control Unit. Each time the Communications Control Unit scans each data line to acquire an inbound character, it must check for the possibility that the character is an "N" and keep a record of a possible run of "N"s. If it finds four "N"s in a row, it must generate a signal to the Central Processor indicating an End-of-Message. The diagram in Fig. 6(a) shows a portion of the logic necessary for this function. Included is a gate, "N," which is wired to recognize the character, and trigger a counter. The counter is preset to a value indicating the number of "N"s previously accumulated through the gate "C"; the information for this value is stored in a control word in the memory. If the character received is an "N," and the counter is set to "3," then this logic net generates a



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signal which causes the necessary Processor interrupt. If the character is not an "N," then the counter is reset, and its previous setting deleted from the control word (logic for this function is not shown), and the control word returned to memory. There is a very substantial investment in transistors for this function but it takes virtually no time from the Central Processor. Fetching and restoring of the control word are the only operations that take significant time and they serve other useful purposes.

The other extreme approach is illustrated in Fig. 6(b) which shows a flow chart of a computer program that performs the same functions as the logic net of Fig. 6(a). The operation of the program occurs as sequential scanning of a block of characters stored in the Central Processor's memory by a block assembly operation. This is a very time-consuming operation. Each time the program inspects a character it must go through at least steps 1, 2, 5, and 6. Since "N" is a popular character, it will often occur singly and doubly in ordinary text so the program will frequently go through steps 1, 3, 4, 5, and 6. Only rarely will the program actually find an "End-of-Message, but it must faithfully go through 4 to 5 steps per character anyhow. Depending on the characteristics of the computer (primarily, the character handling and indexing), these 4 to 5 program steps will take 12 to 30 memory cycles, a very substantial price to pay for a routine check. (To put some numbers on this statement, if a particular computer takes 20 memory cycles for this routine, has a 5 microsecond memory, and has to handle an expected load of 1000 characters/second, the End-of-Message check will occupy 10% of the system's time.)

In the case of this particular example, a combination approach would essentially involve relieving the computer program of the necessity for scanning all text in search of "N"s. The Communications Control Unit would be provided with a simple "N" recognition gate, but no memory for sequences of "N"s, and would generate a processor interrupt whenever an "N" was detected. The program would still have to find the sequence, if it was present, but at least it would not have to check every data character.

The above simple example illustrates the complexity of the problem. Each Channel Control function must be subjected to the same type of analysis and an acceptable compromise found. The problem is clearly sensitive to the particular requirements of each application, and design tradeoffs that are attractive in one case may be unsuitable in another.

BULK DATA BUFFERING

Data communication centers generally accumulate complete messages before they are further processed. With heavy traffic, this may lead to a demand for storage space for a substantial amount of data, possibly in the order of several million characters. Core memory storage is too costly for these large quantities so that magnetic drums or discs are used to store "in-transit" traffic. The access time for these devices is several orders of magnitudes slower than the access time of core memories. While access times are relatively high, in the order of 30 to 200 msec, transfer times are often directly compatible with core memory access times. This means that once an addressed storage area of the drum or disc has been located, transfer to or from high speed core memories is quite rapid. Data transfer between core memory and disc or drum becomes more efficient when larger batches of data are transferred during each access. This in turn leads to a demand for large areas of core memory for data buffering, and a compromise is usually required between the size of the batches and efficient data transfer. The result of such considerations is the need of some amount of bulk data buffering for accumulating data coming from data lines, and for distributing data received from the main processor.

Transfer to and from these bulk data buffer areas can be performed by hardware in the Communication Control section or by programmed operation. The same tradeoff between hardware and programmed approach applies here as for the other functions that have already been discussed. The simplest storage allocation scheme assigns a fixed portion of core memory to each data line. Control logic for gaining access to these areas is very simple but a substantial portion of the memory is permanently tied up regardless of whether it is really used or not. A much more efficient use of memory space can be achieved when a pool of memory areas is provided which can be assigned to the various lines on demand. The statistical distribution of traffic must be known reasonably well to reserve adequate memory space for all or almost all traffic conditions. The procedures for assigning memory space to a communication line is somewhat complex but easily manageable by a program which does not have to be called up at too frequent intervals.

When a sufficiently large memory is available in the main processor and access demand is not too high — essentially in relatively small systems with mostly low speed traffic and simple channel control procedures — a portion of the main memory can be used for bulk data buffering. Large systems with heavy traffic loads and complex channel control procedures usually require separate memories for Bulk Data Buffering which is under direct control of the Communication Control Unit. Transfer between this memory and the main processor memory, however, is controlled by the processor which initiates the transfer as soon as the Communication Control signals the need for buffer clearing or refilling. With either of these arrangements, circumstances may arise that prevent the buffer areas from being cleared sufficiently often so that a number of lines will overflow their allocated buffer area or cannot get a buffer location assigned. Incoming data will then be lost unless provisions can be made to throttle traffic by causing the remote transmitter to halt transmission temporarily. If this is not possible, lost messages must be recovered by operator intervention, mostly by using manual operations and in any case by rather tedious means. This is partly the reason why automatic data communication systems tend more and more to use at least a minimum amount of automatic channel control procedures.

In applications where large quantities of data traffic have to be moved, the bulk data buffer requirements are potentially a major cost element of the system. Specific design methods are available for optimizing this storage requirement. These methods, which are based on Queueing Theory, will be discussed in Part 5 of this series.

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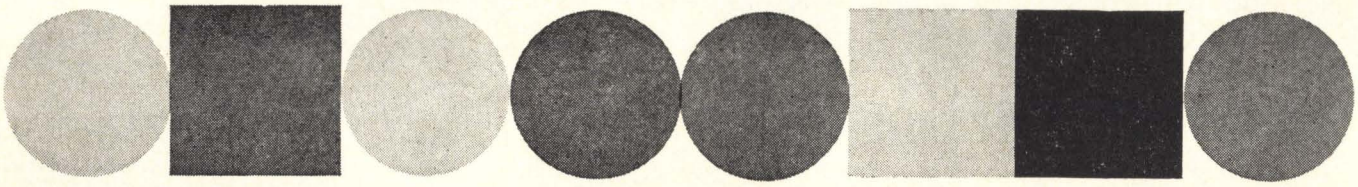
CONCLUSIONS

A variety of approaches exist for implementation of the Communications Interface portion of computer-communications systems. The most appropriate selection for a given system depends on a careful review of particular aspects of the communications load. Here in Part 2 of this series, we have tried to illustrate the functions of the Communications Interface and the techniques available for their implementation.

The major variable between Communications Interface approaches is the tradeoff made between components in the Communications Control Unit or Line Termination Units and program execution time. There is no tradeoff which is good for all applications but attempts to save hardware by use of memory time should become more commonly used in future systems, as the only argument against this approach is machine time, and computers are continually getting faster.

NEXT IN THIS SERIES:

Part 3—Types of Operational Communications Interface



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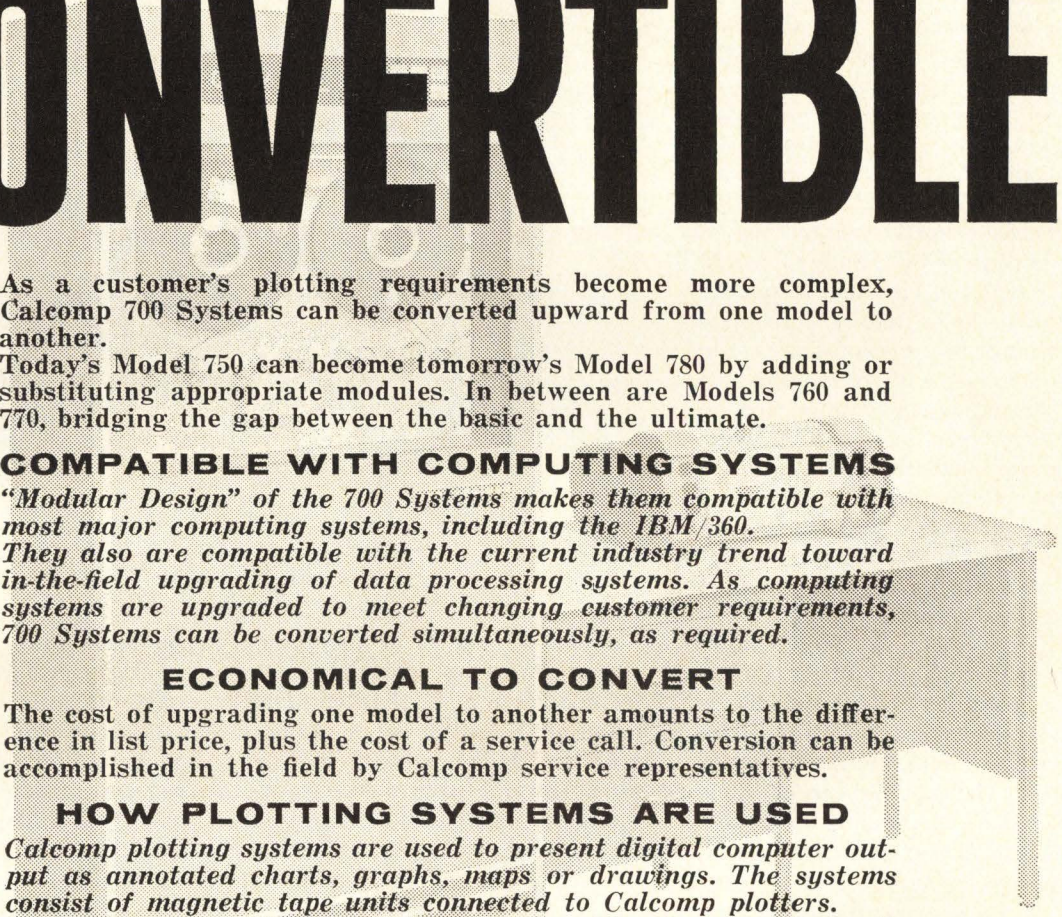

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GENERAL PURPOSE MILITARY COMPUTER

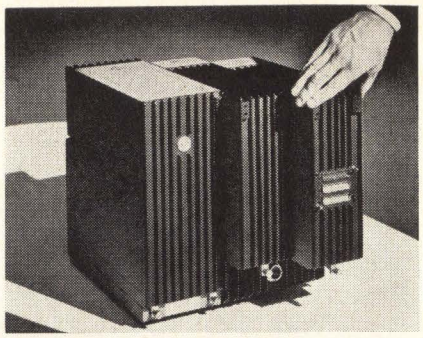
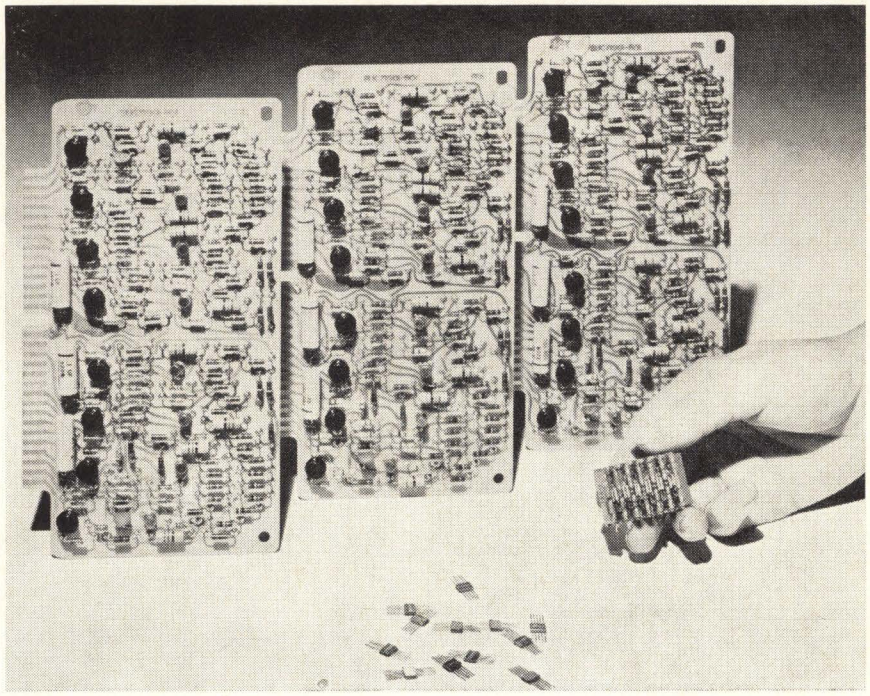


Photo at right shows modular construction of new system; photo below illustrates size reduction obtained with integrated circuits.



General purpose military computer system combines the use of the most advanced microcircuitry and the advantages of modular growth capability. The new system, called D84, occupies only 1.4 cubic feet, weighs 100 pounds, operates on 110 watts of power and is fully transportable. The computer can withstand temperatures from −62C to +75C. The D84's compact, rugged design is made possible by the use of monolithic integrated circuits. Its modular system design allows it to grow — without re-programming — to match the capacity of all but the very largest systems announced to date. This combination of features is said to make the D84 ideal for tactical command and control; ground, airborne, and naval data systems; fire control; automatic message processing, missile checkout and general purpose data processing. Key element in the versatility and growth capability of the D84 is its use of functionally and physically independent central data processor, memory and input/output modules. The modules can be interconnected in any combination to fit the particular application. Up to 16 memory modules (4,096 words each) and a "floating" quantity (system dependent) of input/output modules may be added as the system requirements grow without affecting the central data processor. For multi-processing applications, additional central data processor modules can be added to the system. Users have a wide choice of memory modules in the D84 system; DRO and NDRO, ferrite core or magnetic thin-film. Memory speed is determined by the type selected. For example, a typical DRO core memory would have a read/write cycle time of 2 microseconds while an NDRO thin-film memory can be read out in only 200 nanoseconds. A measure of the computer's I/O capabilities is its maximum combined data rate of 6 million bits per second (250 kc word rate) with 12 million bits per second being permissible in short bursts. Software packages available with the D84 include an assembler and a simulator written in Fortran IV, a diagnostic program, and an automatic operating and scheduling program as well as a full library of D84 routines including: floating point arithmetic, double precision arithmetic, square root, trigonometric and inverse trigonometric functions, exponent functions, logarithmic functions, BCD to binary conversion, and a confidence check. Burroughs Corp., Paoli, Pa.

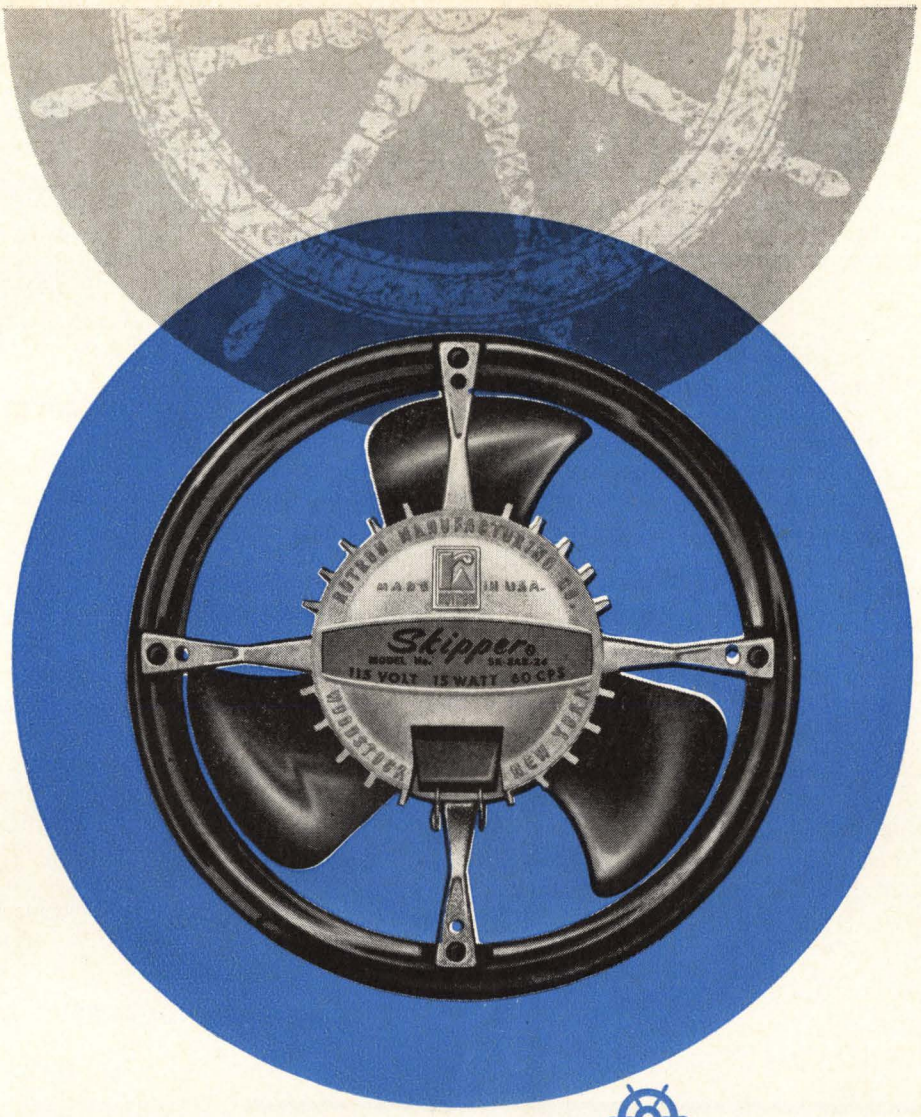
Circle No. 189 on Inquiry Card

"CAUSES AND CURES OF NOISE IN DIGITAL SYSTEMS"

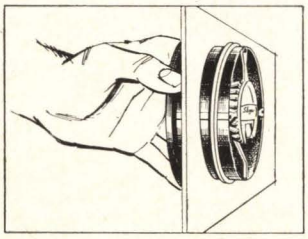
SEE PAGE 24

"TELETYPEWRITER FUNDAMENTALS"

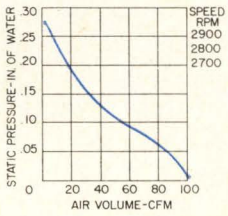
SEE PAGE 92



You can buy the amazing new *Skipper* for less than $4.00 in quantities!



- Time and money saving installation—just cut out hole for fan and slide neoprene rubber mounting ring over venturi—and the Skipper is instantly secured in position. No mounting holes to drill... no nuts and bolts to handle.
- Complete selection of matching accessories available—line cord and plug, finger guards, etc.
- Styling and reliability—unmistakably ROTRON.
- Designed to meet U.L. Approval.
- Impedance Protected.
- And it's quiet! Only 39 db SIL.
- Constructed of unbreakable polymer and die cast aluminum.
- Built-in heat sink for cool running motor and longer life.
- For operation at ambient temperatures up to 140°F (60°C).
- Measures just 5¼" in diameter by only 1 13/16" in depth.
- Just 5/6 lb.—lightweight.
- Alternate mounting arrangements.
- Mounts easily anywhere—on any panel thickness (even glass).
- Available in 115V—60CPS-1φ (other ratings available).



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Visit Rotron NEPCON Booth 550-552, Long Beach, June 8-9-10.

CIRCLE NO. 37 ON INQUIRY CARD

NEW PRODUCTS

SILICON TRANSISTORS

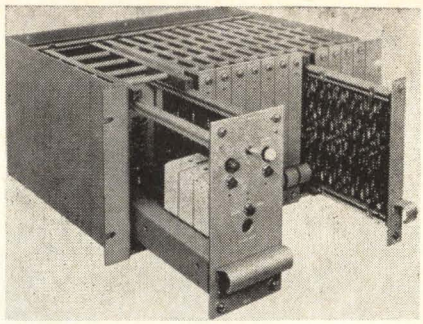
A new family of epitaxial planar transistors were designed specifically to operate at very low collector current in applications requiring a high current gain. They will deliver a minimum dc current gain of 140 with a collector current of only 0.1 ma and a V_{ce} of 5 volts. The T_s on all devices in the family is typically 20 nanoseconds in standard test circuits. Junction capacitance is less than 2 pfd. F_t is typically 1000 megacycles. The price on these units vary from $5 to $10 depending on the specification and the quantity. Solid State Labs. Vector Dept., Norden Div. U.A.C., Southampton, Pa.

Circle No. 177 on Inquiry Card

MATRIX PROGRAM BOARDS

Standard matrix program boards allow stock delivery of matrices to customers requiring rapid service, and the modular construction of larger matrices when time does not allow for a special matrix board. These program boards can function as patchboards, variable diode matrices, systems interfaces, memories, function generators, circuit selectors, data loggers, numeric control boards, breadboard panels, and variable process programmers. Crosspoints are on ¼" centers and accept 0.10" diameter pins (shorting or coaxial type). Units with 2, 3, 4, or 5 decks are available. Prices start at $0.15/crosspoint. Co-Ord Switch, Corona, N. Y.

Circle No. 181 on Inquiry Card



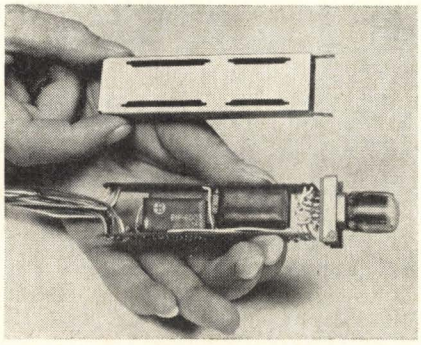
MODULE RACKS

New 5¼" x 11" module rack can be used with any combination of 1", 2", 4" or 8" modules, and will also accept printed circuit cards in combination modules. This arrangement together with other 7" and 8¾" high module units makes possible over 450 assembly combinations. The 5¼" module rack makes it possible to package a power supply and circuit boards or a memory unit and logic boards into one compact unit which is available from stock. Vero Electronics Inc., Farmingdale, N.Y.

Circle No. 128 on Inquiry Card

NIXIE DRIVER MODULES

BCD to decimal decoder/driver for miniature rectangular Nixie tubes, is said to be the smallest BCD input decimal display with memory. The new module, designated the BIP-9402, is designed to accept 8-wire, 8421 BCD code inputs on command. The BIP- 9402 is one of the first in a series of Nixie tube driver-modules which uses new hybrid microcircuits containing single-sided, glassivated semiconductor devices. According to the company, use of the hybrid circuits makes possible important reductions in both module size and cost. The BIP-9402 measures only 0.950" x 0.450" x 4.5" and is priced at $49.00 including a long-life rectangular miniature Nixie tube in thousand piece quantities. Functionally, the miniature decoder-modules consist of a 12-diode decoder and 12 SCS's in a



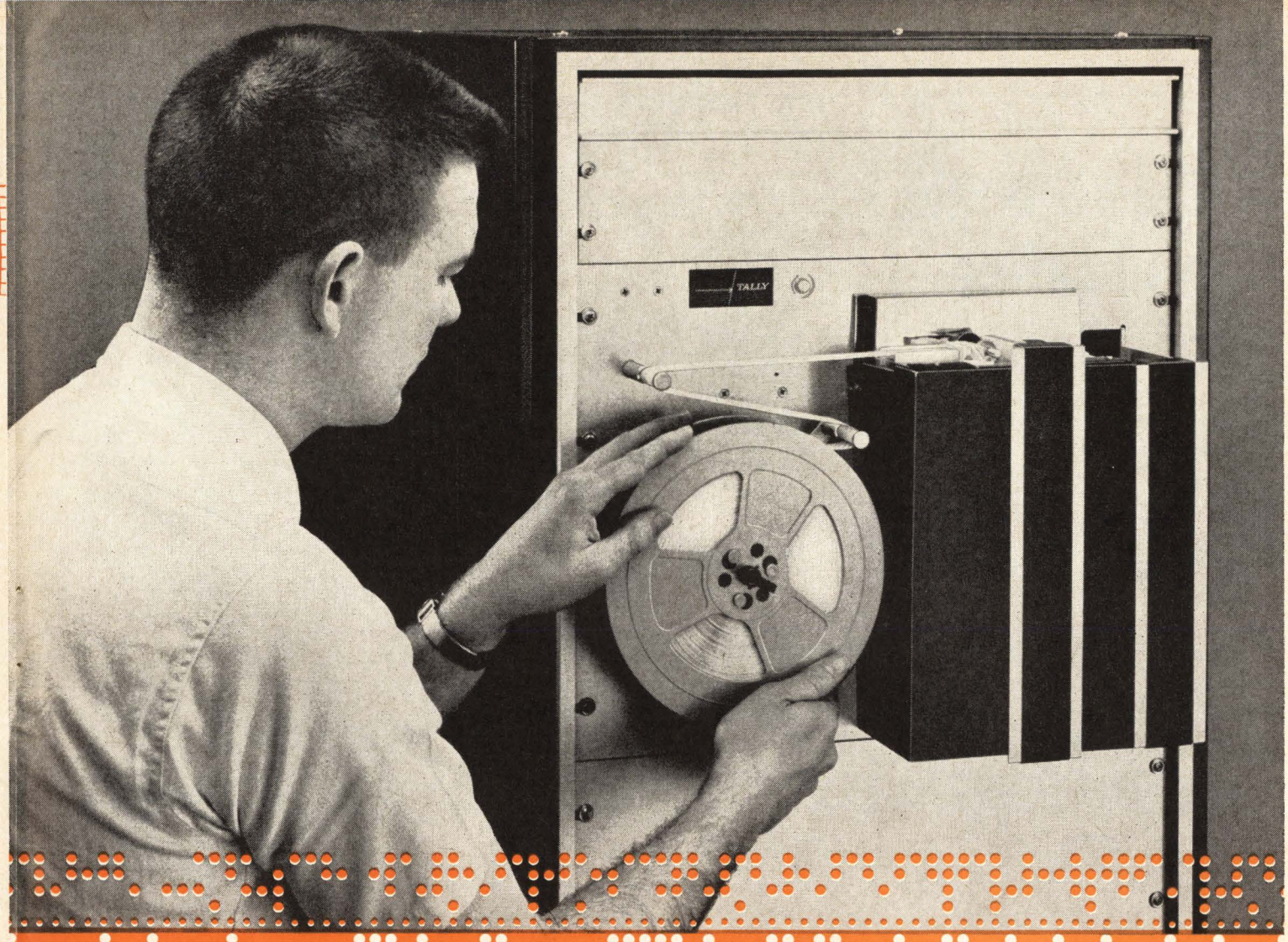
memory-driver circuit. The diodes convert the BCD input into biquinary to select one of five odd-even number pairs. Two SCS's select odd or even from the selected pair under the control of the least significant binary input to yield the final decimal selection. Burroughs Corp., Electronic Components Div., Plainfield, N.J.

Circle No. 138 on Inquiry Card

COMMERCIAL DTL CIRCUITS

Line of DTL integrated circuits were developed for commercial computer applications. Designated the WC-200 series, the circuits are patterned closely after company's standard line of military DTL circuits. Typical performance characteristics of the new line include switching times of 25 nanoseconds, power consumption of 7.5 milliwatts, and fan out of 11 per gate function. The operating temperature range of the new commercial WC-200 line is 0 degrees C to 75 degrees C. Circuit functions initially being offered in the WC-200 line are: dual 3-input and 4-input NAND gates, triple NAND gate with node, quad NAND gate, 6-input NAND gate with node, 8-input NAND gate with node, dual line driver, R-S flip-flop (3-inputs with node per side), pulse binary counter, shift bit, and high-speed seven and ten array. Prices of the commercial integrated circuits are in the range from $3.70 to $9.50 per unit, depending on their complexity. Westinghouse Electric Corp., Molecular Electronics Div. Pittsburgh, Pa.

Circle No. 155 on Inquiry Card



NEW P-120 PERFORATOR...

...puts down data at 120 char/sec, catches errors, and prices out at $975 in quantity

Once in a while, a new product comes along which fits the functional needs of a market to a "T". Tally's new P-120 Perforator is just such a device. The P-120 embodies more useful features and better performance specifications than any perforator ever offered at this price (or even several times the price).

This compact, panel-mounted perforator features integral tape supply and take-up reeling.

The P-120 is designed for quick, easy, front tape loading. Using a limited number of moving parts in a highly accessible frame gives exceptional reliability and speeds maintenance. Operation is asynchronous. Error control and remote tape backup options are offered at modest extra cost. Error checking is accomplished by contacts which sense the mechanical motion of each punch pin. If an error is sensed, a delete code can be punched **before** the tape advances.

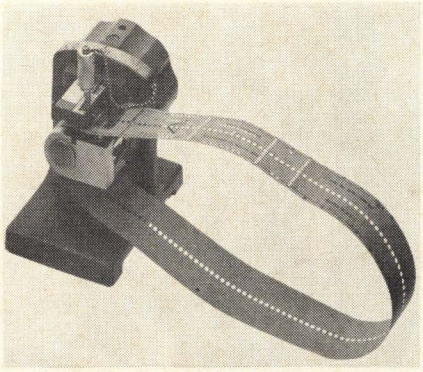
A new bulletin, yours for the asking, tells all. Write our Mr. Ken Crawford, Tally Corporation, 1310 Mercer Street, Seattle, Washington 98109. In the U.K. and Europe, address our man in London, H. Ulijohn, Tally Europe Ltd., Radnor House, 1272 London Road, Norbury, S.W. 16, Surrey, England.

*See it at the IFIP Congress #138-139

TALLY®

CIRCLE NO. 38 ON INQUIRY CARD

NEW PRODUCTS



FORMAT TAPE PUNCH

New format tape punch for the vertical control of pre-printed forms was designed to punch 6 or 8 lines per inch or a combination of both on flat or looped 12 channel tape. The simple mechanism may be used on paper, Mylar or pre-printed paper-backed Mylar tape. A sprocket guides the tape forward or backward for easy tape stepping and perfect control. Positioning devices assure accurate placement and printed tapes are easily read in the punching position. Unit is priced at $90.00. Anelex Corp., Boston, Mass.

Circle No. 145 on Inquiry Card

CONSTANT-CURRENT REGULATOR

Miniature constant-current regulator provides unique current regulation of 1% over a wide range of input voltages and operating temperatures. Unit is a solid-state device combining silicon transistors and diodes in a welded cordwood assembly. A 2-terminal regulator, it can be in series with the current line, hence needs no reference to ground. According to the manufacturer, unit is priced lower than the cost of building current-regulating circuits. Temperature coefficient is 0.03% per degree C; threshold voltage 9 volts; and current stability with voltage −1%. Maximum power dissipation ranges from 1 watt to 3 watts at 25C case, and from 0.4 watt to 0.87 watt at 25C ambient. Electronic Modules, Inc., Pasadena, Cal.

Circle No. 123 on Inquiry Card

TABLE ELECTROPLOTTER

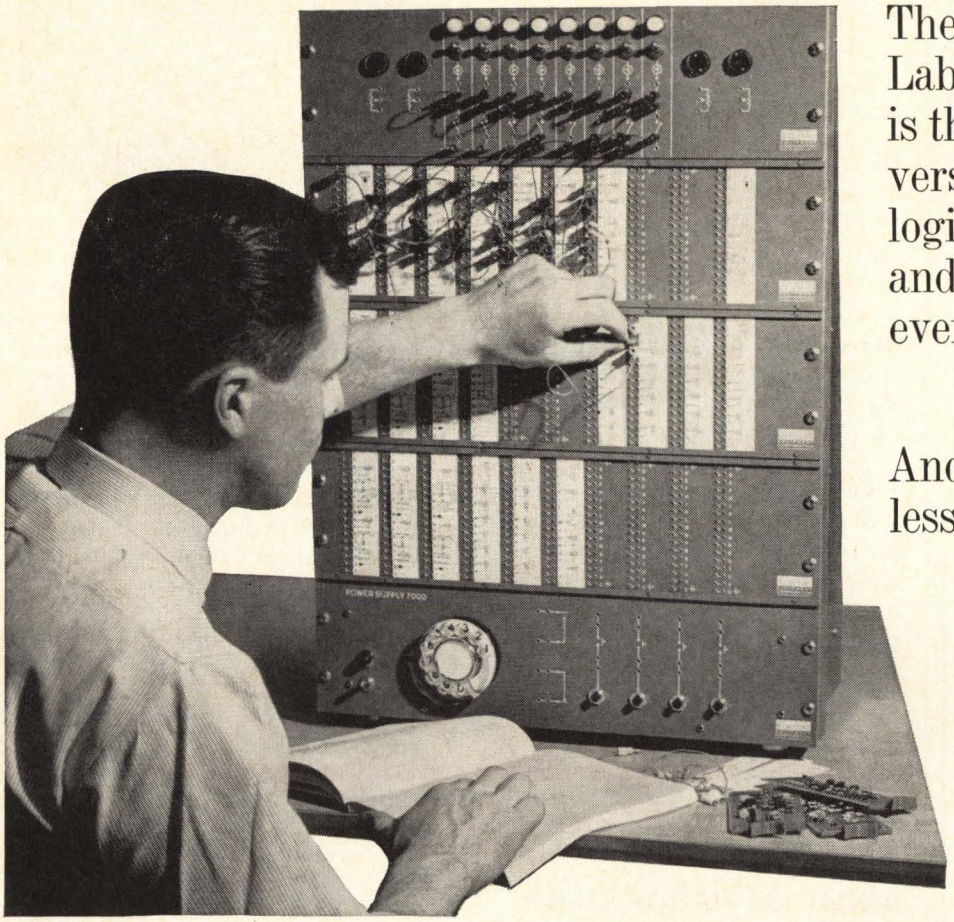
Solid-state "Large Table Electroplotter" affords a complete contouring package for large-scale computer applications for exact delineations in minute detail of surface contours, weather maps, and topographical features. It produces report-quality graphs and maps rapidly and accurately from computer-generated output tapes. From either program or operator control, it plots points, symbols, or alphanumeric characters, and draws straight or contour graphs from digital input data. Inputs can include magnetic tape (200/556/800 bits per inch), gap or "gapless" formatting; punched cards (via summary punch) or control panel switches. Plotting area is 42″ x 58″. Benson-Lehner, Van Nuys, Cal.

Circle No. 126 on Inquiry Card

100 MC PULSE GENERATOR

New Model 216A pulse generator delivers continuous pulses or internally regulated pulse bursts with rise time under 2½ nanoseconds, at repetition rates up to 100 mc. It is expected that this instrument will be especially useful in the design and testing of high clock-rate computer systems. With rapid rise time and ability to deliver 10 volts into 50 ohms, Model 216A also exhibits nearly ideal pulse shape. The output circuit constitutes a true 50 ohm source, even during the generation of the pulse. Reflections which would otherwise interfere with accurate measurements are thus eliminated. The instrument may be set up to generate pulse bursts, either on external trigger command or at selected successive intervals, each burst consisting of any desired number of internally-generated pulses. This pulse train feature will facilitate logic circuit testing. Hewlett-Packard Co., Palo Alto, Cal.

Circle No. 129 on Inquiry Card



The Digital Laboratory System is the most versatile digital logic design tool and training device ever made.

And it costs less than $1000.

With the Digital Laboratory System, you or your technicians can build operating digital systems...complete with logic elements, power supply, controls, indicators and mounting hardware. The plug-in FLIP CHIP™ logic modules are the same used in production digital equipment, including Digital's own remarkable PDP-8 Computer.

You quickly learn to build digital testers, simulators, or breadboard systems using front-mounted logic-circuit diagrams and patch cords. Plug in additional FLIP CHIP modules to build more sophisticated systems. Connect more standard digital panels to construct systems with expanded computing capability.

The Digital Laboratory System is an excellent training device, too. Students, technicians, or staff members who want to familiarize themselves with digital techniques can learn quickly using our free workbook. It contains detailed experiments in 2- and 3-hour laboratory sessions.

For a demonstration, call any Digital Equipment office or the main office: DIGITAL EQUIPMENT CORPORATION, Maynard, Massachusetts 01754. Telephone: 617 897-8821.

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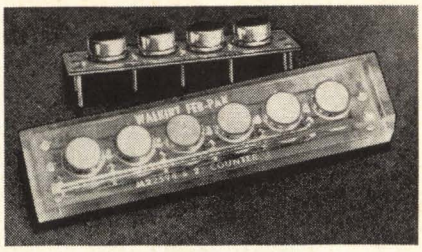
digital

CIRCLE NO. 39 ON INQUIRY CARD

NEW PRODUCTS

IC RIPPLE COUNTER



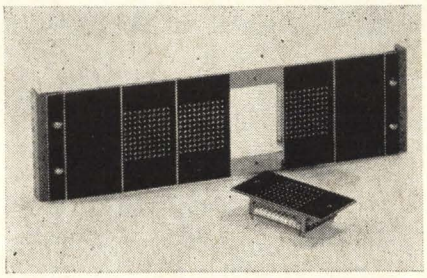
New addition to a "FEB-pak" line of integrated circuit modules is a "Soft-Pot" ripple counter. The "Soft-Pot" module is said to be a new innovation — a repairable potted module. The modules are fully encapsulated in clear, soft silicone resin which provides complete environmental protection. The unique qualities of the silicone resin permit a defective integrated circuit to be easily replaced in the field without special tools or curing ovens. All interconnects are visible through the clear encapsulant allowing test probes to be easily inserted through the soft resin. The ripple counter has a maximum frequency of 10mc and will operate in a temperature range from 15C to 55C with extended temperature range available in other modules. The counter is referred to as a "2^n counter" with "n" being any number from 2 to 8 binary stages. The cross-section of the module is 0.437″ x 0.406″ and the length varies from 1.375″ to 4.000″ depending on the value of "n". The Walkirt Co., Los Angeles, Cal.

Circle No. 141 on Inquiry Card

DIGITAL LABORATORY SYSTEM

A versatile digital-logic training device and design tool allows the designer or student to build an operating digital system, complete with logic elements, power supply, controls, indicators, and mounting hardware. By changing simple front panel connections, dozens of different, basic logic circuits can be made. Priced at less than $1000, the desk-top unit is built around company's recently introduced "Flip-Chip" modules, a line of computer circuit packages with both integrated and discrete components. Two or more of these laboratory systems connected together provide full scale computing ability. As a training device, students, technicians, and engineers can learn all basic digital logic techniques. A workbook contains detailed experiments in 2- and 3-hour lab sessions. As a design tool, engineers can breadboard their designs on the laboratory system, experimenting with different configurations for optimum system performance. The laboratory system can also be used in simulation and testing. Digital Equipment Corp., Maynard, Mass.

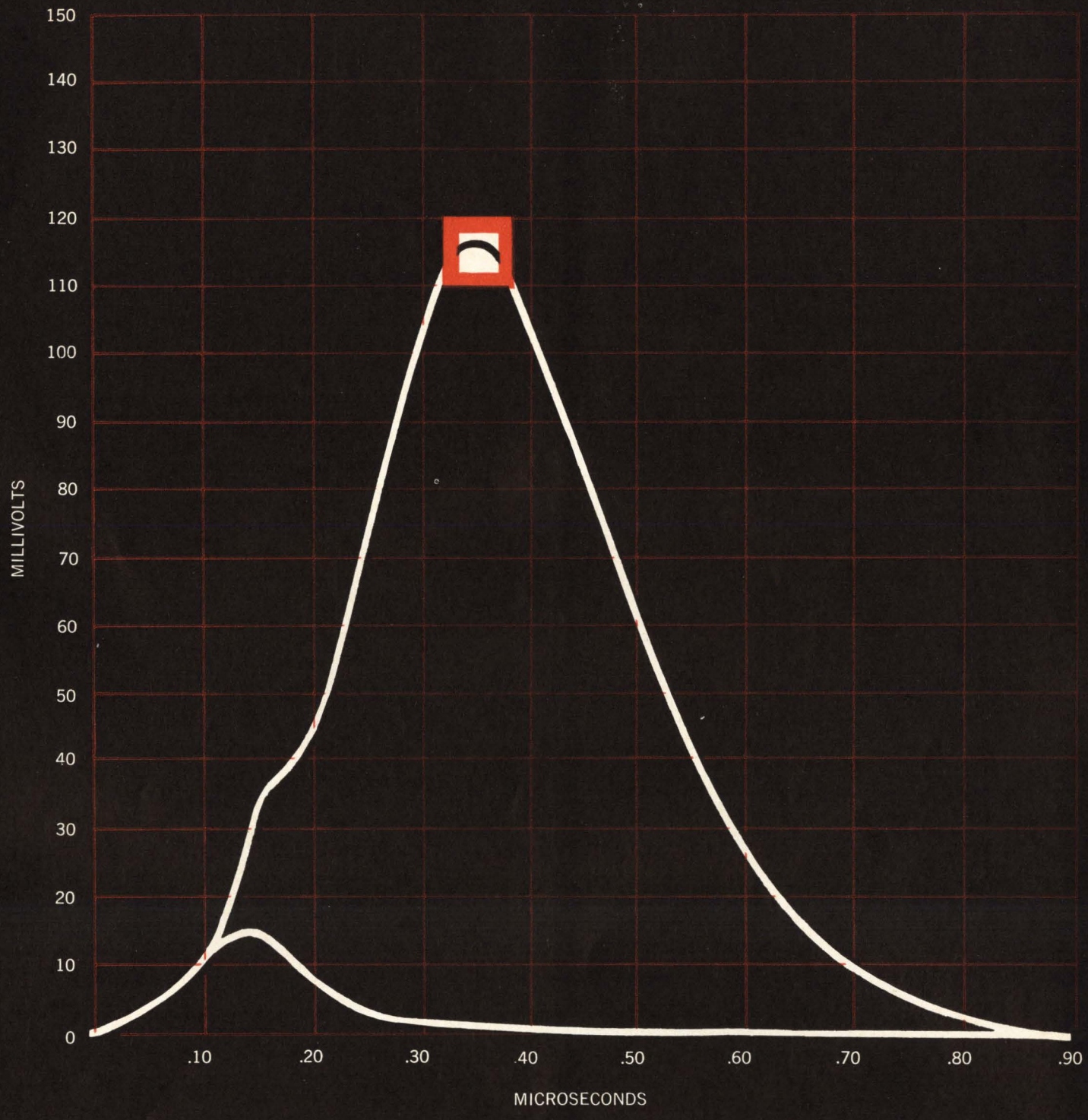
Circle No. 182 on Inquiry Card



MODULAR PROGRAM BOARD

Standard program board modules enable the user to make up configurations to suit his specific requirements. The modular unit is so designed that it may be mounted in standard EIA 19″ relay rack or bench cabinets. The system consists of 10 × 10 matrixes, blank filler panels, end pieces, mounting rails, and buss jumpers. With the jumpers, the user can buss either horizontally or vertically to any electrical pattern required. The blank filler panels can be employed to mount associated components and also allow expansion of the matrix system at any future time by merely replacing with matrix modules. All units are held in place with screws threaded into the mounting rails. Sealectro Corp., Mamaroneck, N.Y.

Circle No. 158 on Inquiry Card



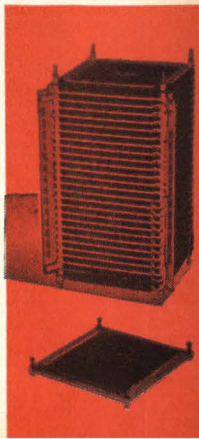
peaking in the window

We're peaking electronically, of course. The chart shown is typical of a sampling of cores manufactured to specification by Burroughs, all produced and tested with infinite care *at no extra cost to you.* This "peaking in the window" is run-of-the-mill for us, throughout our entire range of ferrite cores (20, 30, 50, and 80 mil). The 100% uniformity of Burroughs cores is the best possible guarantee of reliability in assembled planes and stacks. All of our memory products are consistently manufactured to meet the most stringent specifications for military and industrial systems.

And we're in the unique position at Burroughs of having used our own memory products in our equipment, proving them year after year on several continents. Whatever your memory requirements, individual cores, assembled planes or stacks, Burroughs is the logical source.

Write for typical specifications today.

- CORES
- PLANES
- STACKS



Burroughs Corporation / ELECTRONIC COMPONENTS DIVISION
PLAINFIELD, NEW JERSEY

CIRCLE NO. 40 ON INQUIRY CARD

NEW PRODUCTS

SYSTEM POWER SUPPLIES

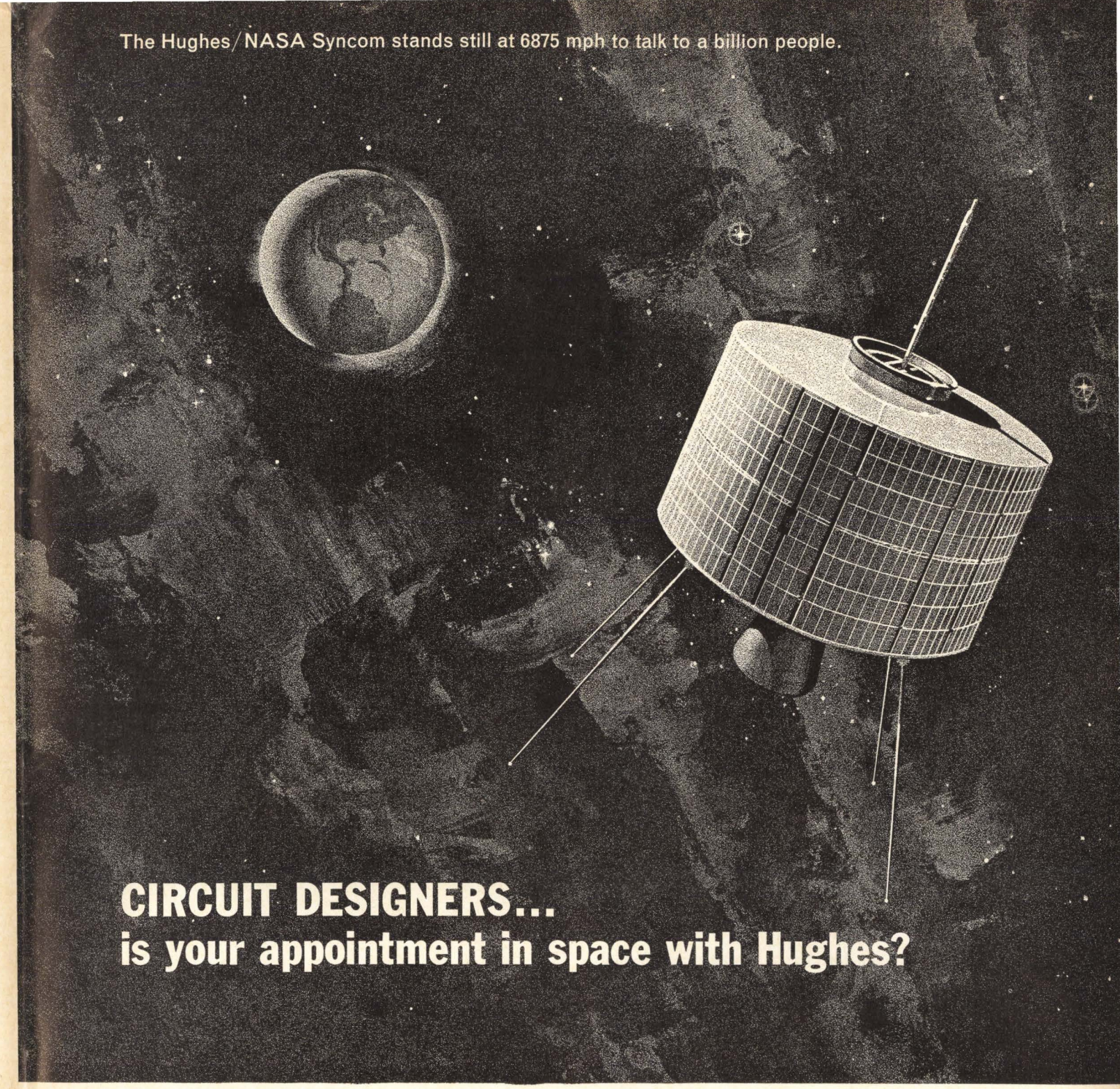
Series of supplies feature precision regulation at high power levels in a 3½" rack mount. With 0.01% regulation at power levels up to 500 watts, units are available in a series of models up to 160 volts. To provide maximum application versatility, the units include both constant voltage and constant current operation, with automatic current limiting, remote programming, and remote sensing. A front panel mode indicator light indicates when unit is operating in the current limiting mode. Automatic overvoltage protection is available as an option. Trygon Electronics, Inc., Roosevelt, L.I., N.Y.

Circle No. 198 on Inquiry Card

VARIABLE DELAY LINE

Microminiature variable delay line, with a total volume of 0.072 cubic inches and a size of 0.3 x 0.3 x 0.8 inches is considered to be the smallest unit of its type ever produced. Although designed for use as a trim delay in various computer circuits, it has many potential applications in all digital and analog applications where time-coordination is critical. The unit is housed in a plastic case with a miniature seal "O" ring on the shaft and is constructed to meet military as well as commercial requirements. Four delay ranges are offered, with the −1 unit having a range of 3 to 25 nanoseconds at an impedance of 1000 ohms, to the −4 unit with a range of 5 to 100 nanoseconds at an impedance of 50 ohms. Resolution of all units is less than 1/100, temperature coefficient is less than 50 ppm/°C, and attenuation is less than 1db. Unit is priced at $50.00 in single quantities with substantial discounts for larger quantities. Computer Devices Corp., Huntington Station, N. Y.

Circle No. 146 on Inquiry Card



CIRCUIT DESIGNERS...
is your appointment in space with Hughes?

Today, Hughes is one of the nation's most active aerospace/electronics firms: Projects include: F-111B PHOENIX Guided Missile System, TOW Anti-Tank Missile, SURVEYOR Lunar Spacecraft, SYNCOM, POLARIS, VATE, Hard Point Defense and others.

This vigor will assist the qualified engineers and scientists towards more and better opportunities for both professional and personal growth.

Many immediate openings exist. The engineers selected for these positions will be assigned to the following design tasks: the development of high power airborne radar transmitters, the design of which involves use of the most advanced components; the design of low noise radar receivers using parametric amplifiers; solid state masers and other advanced microwave components; radar data processing circuit design, including range and speed trackers, crystal filter circuitry and a variety of display circuits; high efficiency power supplies for airborne and space electronic systems; telemetering and command circuits for space vehicles, timing, control and display circuits for the Hughes COLIDAR (Coherent Light Detection and Ranging).

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For immediate consideration, please airmail your resume to:

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NEW PRODUCTS

MILITARY DIGITAL PRINTER

Militarized version of a digital printer mechanism is now being shipped for use in the Minuteman Missile Program. The Model M-1000, as it is designated, is a basic printer mechanism which can be used with a wide variety of circuitry. The standard military version prints 40 alphanumeric characters per column at a rate of 20 lines per second or the 10 decimal digits (and several signs and symbols at a rate of 40 lines per second). One of the innovations of the M-1000 is the absence of an inked ribbon with its associated drive mechanism. Self-inking, pressure-sensitive paper is used. Impressions are created when the paper is directly struck by the character hammers. Franklin Electronics, Inc., Bridgeport, Pa.

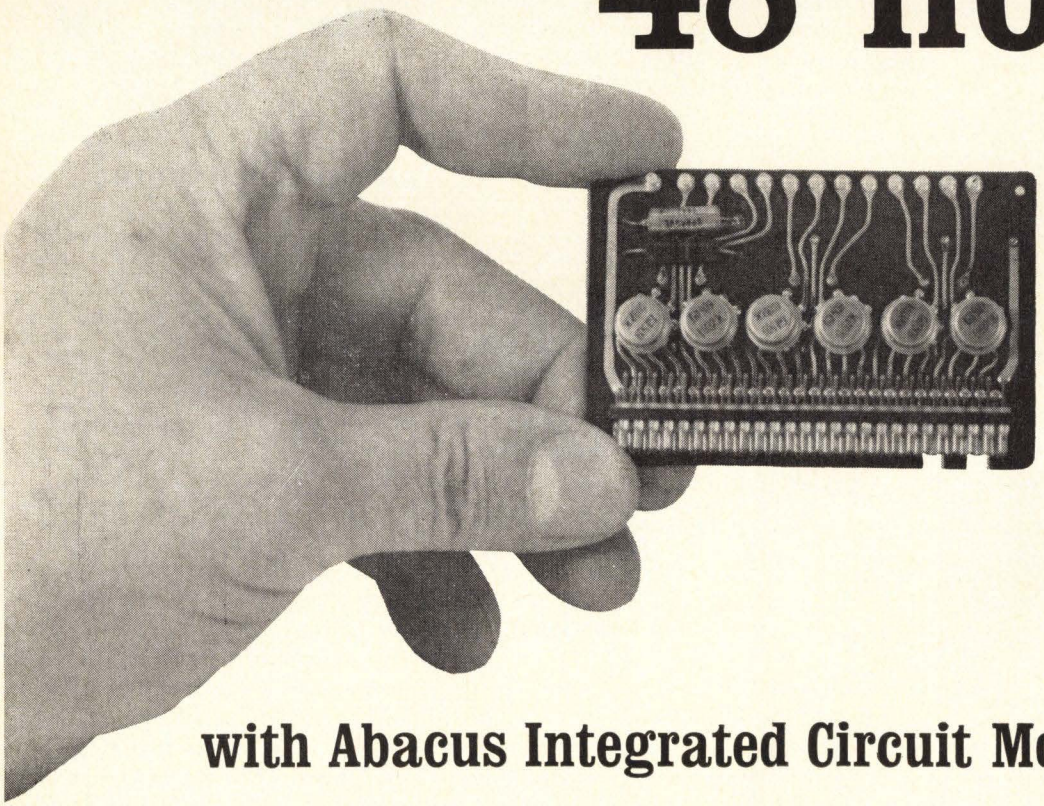
Circle No. 191 on Inquiry Card

BRUSH-TYPE SHAFT ENCODER

Shaft angle encoder is said to exhibit an exceptionally long life, 6 x 10^6 revolutions at 200 rpm. Accurate read-out is available at 500 rpm, where interrogation is required while slewing. Momentary speeds to 1500 rpm do not damage the encoder. Accuracy of the standard unit is guaranteed over the temperature range of $-65°C$ to $+85°C$. Where required, the brush-disc design may be adapted to continuous operation at $+125°C$ for the full guaranteed life. This high temperature performance is believed to be unique for encoders of this type. Type VBE 18-SB13 generates a natural binary output using a self-selecting U-Scan logic. Thirteen bits are generated in 64 turns of the input shaft, resolution being 128 counts/turn. A variety of other outputs-codes, resolutions, scans, etc., are available in the same package. Vernitron Corp., Farmingdale, L. I., N.Y.

Circle No. 154 on Inquiry Card

From equations to complete system in 48 hours



with Abacus Integrated Circuit Modules

Abacus Pre-packaged Engineering offers: ☐ system operation to 5 mc. ☐ noise rejection margins in excess of 1 volt ☐ typical drive: 12 NAND gates and 200 pf stray c. ☐ packing density: over 4000 NAND gates/cu. ft. ☐ packaging hardware, racks and power supplies provided ☐ interconnections by wire wrap, solder or weld ☐ peripheral & interfacing circuits available.

48 HOUR DELIVERY

Whittaker CORPORATION

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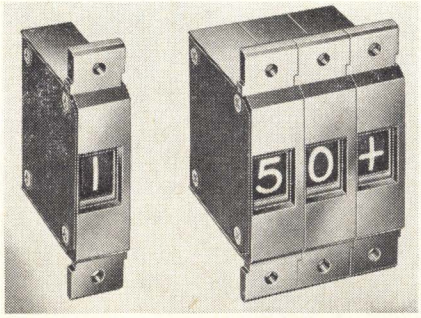
CIRCLE NO. 44 ON INQUIRY CARD

NEW PRODUCTS

TYPEWRITER-TRANSMITTER/ RECEIVER

New typewriter-transmitter/receiver using IBM basic Selectric typewriter is an input-output device for transmission and reception of 6-bit coded data and is said to be ideally suited for use with computers and communications equipment and in data processing, information retrieval systems, and as a data logger for process control data collection and checkout systems. Features include the use of a photoelectric technique to eliminate metallic switch and contact bounce, and to minimize RFI; printing rate of 15.5 characters per second; all solid-state circuits — interface problems simplified; and stationary carriage for minimum space requirements. Basic unit is for 60 cycle operation, 50 and 400 cps units available. Invac Corp., Waltham, Mass.

Circle No. 132 on Inquiry Card



COMMUNICATIONS INDICATOR

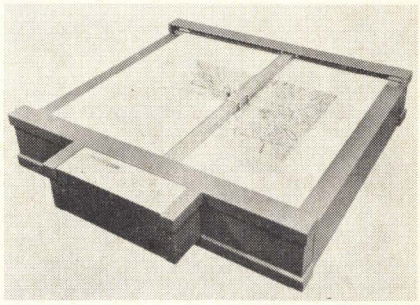
New 26000 Series indicators operate directly from any of the "2 out of 5" codes which are commonly used in communication equipment. In these applications expensive decoding and driving circuits can be eliminated. The new series is offered in a 10-position unit. Digit size is 5/16″ high by ¼″ wide and units operate on 1.5 to 2 watts per bit. Patwin Electronics, Waterbury, Conn.

Circle No. 122 on Inquiry Card

BI-DIRECTIONAL STEPPER MOTOR

New stepper motor features directional reversibility and high step rate. The motor, designated the 44100 series, responds to dc input pulses in discrete 15° steps of angular rotation with positive magnetic detenting at each increment. It will operate from 0 to 80 pulses per second with a corresponding rotor speed of 0-200 rpm. Pulse duration can be in the order of milliseconds or sustained for long periods without damage to the windings. Reversal is obtained by a simple reversing switch. Operating voltage is 27 vdc ± 10%. A. W. Haydon Co., Waterbury, Conn.

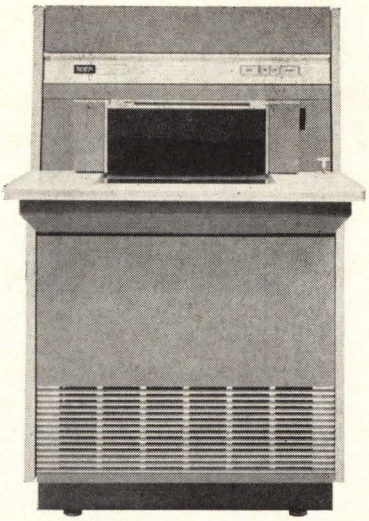
Circle No. 174 on Inquiry Card



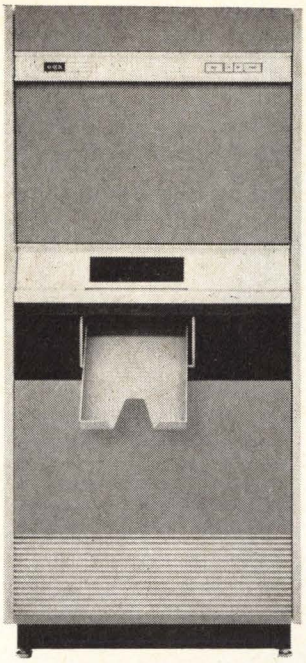
FLATBED DIGITAL PLOTTER

Digital incremental plotter, with a plotting area of 31″ x 34″, is a flatbed version of company's drum plotter series. It is designed for high-speed, high resolution plotting of computer output where decision making requires full and continuous view of the plotting area in situations such as real-time tracking, navigation, or testing. It may be used either on-line or off-line with most digital computers. The digital incremental principle incorporated into the Model 502 Flatbed is said to provide long term, stable, drift-free operation. Alphanumerical and special symbols may be drawn at full plotter speed (18,000 steps/minutes, 0.01 inches/step). Setup time is reduced as there are no scale factors to adjust and origin setting is completely under program control. A wide range of existing charts or maps (up to size 35″ x 38″) may be used with the Model 502, without pre-printing special paper. Base price is $17,000. California Computer Prod., Anaheim, Cal.

Circle No. 164 on Inquiry Card



We sent an 8½″ x 11″ xerographic image 3,450 miles over broadband telephone lines in less than 7 seconds and held the resolution to 135 scans per inch.



Suddenly data systems engineers are noticing us.

On the surface, LDX stands for Long Distance Xerography. In its simplest configuration, it means a pair of ingenious electronic/electromechanical/optical machines—a transmitter and a receiver—linked by coaxial cable, telephone lines, microwave radio relay nets, or any combination of the three media. From a fact-of-life, functional viewpoint, LDX is the most advanced remote imaging system in existence today.

Yet these are surely not the most important reasons why systems engineers are noticing (and joining) Xerox today.

The more profound answers are still in our laboratories, where scientists and engineers steeped in computer technology, data systems engineering, information science and operations research are exploring LDX as one element of an approach to an entirely new regime of graphic communication and information systems.

For the moment, think of networks of LDX systems, fully integrated with real-time computers and a wide variety of peripheral equipment—capable of sensing, storing, retrieving, queueing, transmitting, receiving and translating data from one form to another... and then displaying it automatically not only in alphanumerics, but with equal facility in fully formed diagrams, drawings or pictures.

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XEROX

NEW PRODUCTS

ELECTROLUMINESCENT DISPLAY SYSTEM

An electroluminescent display system that traces a missile on its way to intercept an airplane in mid-air was demonstrated at the recent IEEE convention. The system, which converts coded computer data into light patterns, contains more than 60,000 elements that are selectively-activated to form numbers, letters, symbols and map outlines. Called a crossed-grid display, the system also depicts written messages and military symbols imposed on map outlines. The system employs a high-speed electronic memory constructed of paper-thin perforated sheets of copper-coated plastic. The sheets are hole-punched and stacked on magnetic cores in one-inch deep cartridges. Up-to-date information on targets, troop locations, gun emplacements and the like can be stored and displayed when needed by inserting the cartridge into the system Built to withstand considerable shock and vibrations, the system is suitable for use with airborne computers. Sylvania Electronic System, New York, N. Y.

Circle No. 170 on Inquiry Card

MAGNETIC SEQUENCE TIMER

Specifically designed to provide contact closures (in proper sequence) to separate a satellite from its launch vehicles, a magnetic sequence timer is a completely self-contained unit with an internal mercury battery and internal relays. In operation, the Model 4292 requires no connection other than the contact control circuitry and the start command. Further, it provides 3 separate outputs. For special applications, a variety of basic oscillators — RC, LC, or crystal-controlled — can be supplied to meet particular accuracy requirements. C&K Components, Newton, Mass.

Circle No. 156 on Inquiry Card

PRINTING/PLOTTING DEVICE

High-speed, magnetic tape-driven plotting and printing device, operating off or on-line, converts digital data to contours, line plots, bar charts, engineering drawings, and tone shades for half-tone representation. Continuous, dotted, and dashed lines of varying width provide multiple plot capability with no degradation in intelligibility. Alpha-numerics for annotation and text are provided in any type font, in any size, at any angle. The system, called COMPIX, will produce fifty 12″ × 18″ products per hour regardless of complexity, and simultaneously transmit duplicate products to remote locations via standard facsimile circuits. United Aircraft Corp. Systems, Farmington, Conn.

Circle No. 172 on Inquiry Card

HARD COPY GENERATOR

New data system is a small, rack-mounted, hard copy generator that converts transient information displayed on the face of a CRT tube into dry, permanent, hard copy suitable for storage and subsequent reference. The system, called Datastat II, generates photographic images containing as many as seven shades of gray in addition to providing high contrast copies of alphanumeric data. A self-contained monitor/camera/processor/printer, the system combines the high speed and sensitivity of silver halide recording with the economy and simplicity of operation of electrostatic printing. The system performs all recording and printing functions automatically so it can be operated remote and unattended for long periods. It can, therefore, be fitted easily into any on- or off-line system where data is generated continuously or intermittently and hard copy is required with a minimum delay. It will accept input data at any rate up to 4 frames per second. The first hard copy print is produced with a total time lag of 30 seconds and succeeding 8½ x 11 hard copy prints are produced at the rate of one every five seconds. Photomechanisms, Inc. Huntington Station, N. Y.

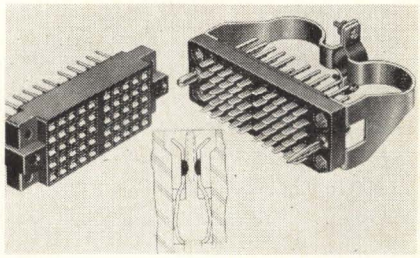
Circle No. 149 on Inquiry Card

NEW PRODUCTS

DIGITAL LOGIC MODULES

New 25kc digital logic modules are available from stock in a wide variety of standard circuit configurations and are suitable for applications where ultra-high speeds are not required. Extensive usage of the new line of digital logic modules is anticipated as a result of the greatly extended component life resulting from encapsulation and low cost. Typically, an all-silicon counter register flip-flop costs only $4.97 in volume. Roback Corp., Huntington Valley, Pa.

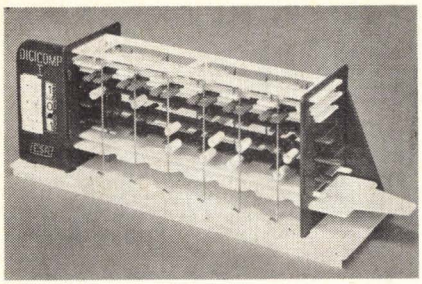
Circle No. 176 on Inquiry Card



GOLD BUTTON CONNECTOR

Multiple contact connector contains a welded gold button on the contact surface. The gold-plated button covers only the contact area of the female receptacle, thus, reducing the area of gold coverage over 95% Although fabrication costs for the new contact are higher than plating costs, there is a substantial savings in the amount of gold used. This results, according to the company, in an approximate reduction of up to 20% in overall connector costs. This, of course, will vary with the size and number of contacts in the connector. The gold button technique is being used initially in a contact with wrappost terminations. However, it can be applied to a broad range of connector and termination styles for printed circuit board as well as rack and panel types. Cinch Mfg., Chicago, Ill.

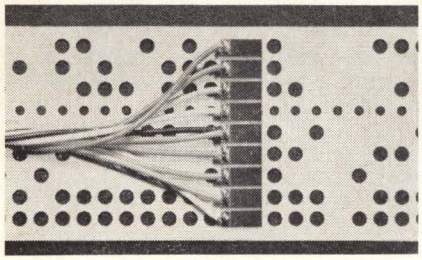
Circle No. 180 on Inquiry Card



TOY COMPUTER

Intended primarily as a teaching aid and game, a do-it-yourself toy computer not only will add, subtract and multiply, but can be programmed to solve many different problems. Called Digi-Comp I, the computer is a faithful mechanical analog of an electron computer. Designed in plastic it comes in kit form and can be assembled in about one half-hour with the included assembly chart. A 28-page operations manual shows how to check the unit out, program problems, solve riddles, tell fortunes, and perform experiments such as simulated automatic elevator sequencing. Fully assembled the unit is 12″ long and 4½″ high.

The kit can be ordered by mail for $5.98 including postage. E.S.R. Inc., 34 Label Street, Montclair, N. J.



SILICON READOUT CELLS

Silicon readout cells feature small size and fast response time for punch tape and/or punch card reader systems. All units have #32 AWG color coded leads 6″ in length. Each readout has an active area of 0.080″ x 0.160″ and the light sensitive surfaces are coated with a special plastic encapsulant. The center-to-center spacing is 0.100″ with an overall length of 0.880″. Response time is less than 10 microseconds. Prices range from $26.35 for 1 to 2 pieces to less than $15.00 in quantities. Datasensors, Inc., Addison, Ill.

Circle No. 161 on Inquiry Card

TAPE TRANSPORT SYSTEM

New, high-performance tape transport is described as "the industry's highest performing and world's most advanced digital magnetic tape transport system". The new transport, Model SC-1150, is a high-speed, single, single-capstan digital tape transport having the capability of operating at bidirectional tape speeds to 150 ips at 800 bpi with no program restrictions. The SC-1150 is 7- or 9-channel (System 360 or ASCII) compatible and can be adapted to all major computer formats. A new tape drive design utilizes a single capstan to pass the tape through a low friction tape path. Tape is threaded directly from the supply reel to the take-up reel. From this point, loading is accomplished automatically at the touch of a button. The oxide side of tape touches no surface except the read/write head, greatly increasing tape life and data reliability. The read/write head is retractable and does not contact the tape during rewind. Control of the tape path is maintained by a precision trough guide system. A low inertia drive permits rapid linear acceleration while maintaining tape contact with the capstan at all times. No restricting pinch rollers, valves, guide rollers, or air guides are used. Complicated mechanical adjustments are eliminated. Constant vacuum results in uniform tape pressure on the reels. The capstan drive system is synchronous motor-controlled to give long motor life and maintenance-free operation. Highly reliable photoelectric sensors, long-life lamps, and all solid-state servo controls are employed. Basic specs include a bidirectional operating speed of 150 ips with fast forward and reverse of 225 ips; a start and stop time of 3.0 milliseconds; and a stop and start distance of ±0.030″. Potter Instrument Co., Plainview, L.I., New York.

Circle No. 163 on Inquiry Card

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By Wm. D. Rexroad

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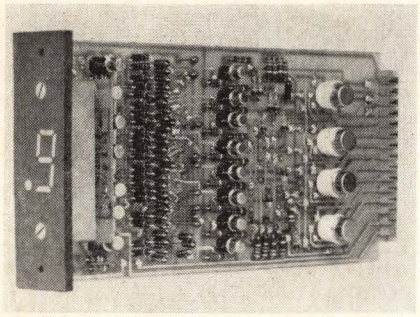
NEW PRODUCTS

ANALOG/DIGITAL RECORDER

New instrument scans up to ten channels of analog input data and produces punched or magnetic tape records ready for digital computation. Bipolar signal selection, measurement, and recording are all in one portable package operating from ac line or battery pack. Operation cycles may be controlled from internal or remote timers, with automatic verification of zero and calibration points. Information Machines Corp., El Cajon, Cal.

Circle No. 144 on Inquiry Card



HYBRID DECADE COUNTER

Decade counter uses a hybrid combination of integrated circuits, transistors, and silicon controlled rectifiers to obtain fast counting rates, high reliability, and versatility. An unusual feature of Model BCD8 is that it can be used as a 3 megacycle decade counter, or an 8-line BCD to decimal display, or a 1 megacycle shift register. To go from one operational mode to another, only the connector wiring has to be changed — no changes are required on the module board. Internal logic memory is part of Model BCD8. The display features wide angle viewing and is seven segment in-plane with 100,000 hour bright lamps. Supply requirements are 12 volts at 260 ma for logic circuit and 5 volts at 60 cycles for lamp display. Size is 1″ wide by 3″ high by 6″ deep. Robotomics Research Div., MB Electronics, Phoenix, Ariz.

Circle No. 162 on Inquiry Card

NEW PRODUCTS

HYBRID CIRCUITS

Cermet film resistor networks and custom cermet film hybrid circuits are fired onto aluminum oxide substrate at temperatures exceeding 800° centigrade. In completed form, the reverse surfaces of the substrate act as covers for the epoxy cases. Typical of units in the series, the Model 15008 measures 0.150 by 0.320 by 0.060 inches and has as many as twelve pure nickel flat leads, each 0.006 by 0.013 inches, on 0.050 inch centers. The resistor networks are capable of continuous operation over a temperature range of $-65°$ to $+150°$C. Tolerances of typical units range from $\pm 1\%$ to $\pm 10\%$. Units with temperature co-efficients of less than ± 200 ppm/°C are available. Columbia Technical Corp., Woodside, N. Y.

Circle No. 190 on Inquiry Card

MULTICURRENT REFERENCES

A new family of multicurrent, temperature-compensated voltage references are said to be unique in three respects. Their low, rated temperature coefficient holds, not merely at a single current value, but across their full current range. For this reason they are considered true multicurrent devices. This significant characteristic provides the designer with substantially increased flexibility. Units are available with any of four different nominal Zener voltages: 6.2, 8.4, 9.0 or 11.7 volts. The three standard, off-the-shelf current ranges are extremely broad, extending from 1 to 15 ma, 2 to 15 ma, and 3 to 12 ma, respectively. The company claims that no other reference diodes presently available provide performance specifications even approximately comparable to those of the new series. Transitron Electronic Corp., Wakefield, Mass.

Circle No. 169 on Inquiry Card

FIELD EFFECT TRANSISTORS

Two new field effect transistors are enhancement mode, P-channel, insulated gate devices. One unit, the FN-1034, is said to outperform any other device for chopping, switching, analog-to-digital and digital-to-analog converting, and multiplexing applications. It features zero offset voltage, low turn-on voltage, low on resistance and high stability. Typical specs for critical characteristics are: gate threshold voltage 1.5 volts; channel resistance of only 200 ohms at −10 volts applied gate voltage; and gate-to-source capacitance of only 2.8 pico-farads. Raytheon Co., Comp. Div., Lexington, Mass.

Circle No. 134 on Inquiry Card

REAL-TIME COMPUTER

A new digital computer, ITI 4900 Real-time Computer, was designed from the users point-of-view aiming at the market of real-time system control and engineering computations. According to the company, one of the most unique and novel approaches of the machine is the integrated software-hardware system. The basic machine language of the computer is based on symbolic coding. A repertoire of over thirty commands is built into machine hardware, requiring no programming translator. With this approach, the user has the command of the flexibility and capability of a stored program computer without the burden found in programming conventional computers. The ITI 4900 is a decimal machine with a word length of six decimal digits or four alphanumeric characters. There are basically three models available, differing only in memory types. Both delay line and core memories are offered. The memory size is expandable with a minimum size of 100 words. The basic computer is housed in a chassis which measures only 18″ x 21″ x 9″. A control console with full alphanumeric display is included in the basic computer. The minimum computer configuration uses Selectric keyboard printer for man-machine communication. The basic ITI 4900 computer is offered at a sale price of $6995. Information Technology, Inc. Sunnyvale, Cal.

Circle No. 136 on Inquiry Card

LITERATURE

Software Packages

Computer software packages, ranging from automatic checkout systems for spacecraft through automatic typesetting to the most advanced Fortran compilers, are described in a new 8-page brochure. The brochure also discusses development of a hyphenation algorithm believed to be the most accurate ever devised for automatic typesetting. Mesa Scientific Corp., Santa Ana, Cal.

Circle No. 217 on Inquiry Card

Power-Plant Automation

A 20-page brochure entitled "Power Plant Automation" describes a multi-computer control system and how it accomplishes a highly-automated attended power plant. The system minimizes and upgrades operator participation to the degree that one man can properly supervise several units, simplifies the man/machine interface, automates many functions now performed manually, and utilizes independent sub-loops that may operate simultaneously. The brochure explains in detail the unit-management concept incorporated, the various types of computers and computing functions involved, and the simplified but upgraded activity of the operator. Bailey Meter Co., Wickliffe, Ohio.

Circle No. 216 on Inquiry Card

Logic/Display Module

A 4-page catalog describes micrologic combination decade, BCD display, shift register module. It offers high-speed 3 megacycle operation with choice of multi-colored wide-angle viewing display. Robotomics Research, Div. of MB Electronics, Phoenix, Ariz.

Circle No. 222 on Inquiry Card

Magnetic Tape

Detailed description and specifications of magnetic tape for RCA 301 and Univac computers are presented in two data sheets. Ampex Corp., Redwood City, Calif.

Circle No. 208 on Inquiry Card

Frequency Counters

A 4-page short-form catalog describes firm's line of solid-state frequency and time interval counters, and radar/laser ranging equipment. The catalog places special emphasis on the more advanced instruments such as 110 mc and 6.4 Gc frequency counters, 10, 1.0, and 0.1 nsec time interval counters, and a 1.0 nsec digital delay generator. Eldorado Electronics, Concord, Cal.

Circle No. 228 on Inquiry Card

Logic Module Manual

A new 202-page catalog describes a complete line of "Flip Chip" digital logic modules including extensive material explaining their use. It covers more than 100 digital logic circuits and their accessories, with particular emphasis on 2 megacycle and 10 megacycle modules. A 37-page introduction explains basic digital logic. No experience in logical design is assumed and numerous examples of typical circuits are presented. A 27-page appendix provides relevant background and reference material, such as explanations of digital and octal number systems, Boolean algebra, and a bibliography of literature on digital logic. Both numerical and alphabetical indexes provide quick access to all information. Digital Equipment Corp., Maynard, Mass.

Circle No. 230 on Inquiry Card

Modular Computing System

A new low-cost modular computer is described in a 16-page brochure which highlights different types of peripheral equipment available for configurations ranging from a modest first system to a more sophisticated system. National Cash Register Co., Dayton, Ohio.

Circle No. 221 on Inquiry Card

Display Driver

Data sheet describes a transistorized display driver for controlling 6, 12, or 28 vdc incandescent lamps projection readouts. The unit permits low current signals — as low as one milliamp — to switch the display's incandescent lamps on and off. Decoder circuitry, for 1, 2, 4, 8 code input and other popular codes, is an optional part of this compact module. Built-in memory is also available. Transistor Electronics Corp., Minneapolis, Minn.

Circle No. 220 on Inquiry Card

Cooling Primer

A third edition of a pocket size handbook, "Forced-Air Cooling Primer", is intended primarily for the engineer who must design a forced air cooling system for electronic equipment. The primer provides a basic design outline and check lists of factors that should be considered to achieve a sound cooling system for reliability. The information will aid in determining the quantity of air required for cooling. It also gives directions on how to calculate accurately the pressure drops through densely packaged electronic equipment by performing tests on mockups using any available air source for determination of final design values. Other important information includes air and temperature measurements, determining size of blower wheel, effects of speed changes on blower performance, effects of density, and effects of altitude. The Henry G. Dietz Co., Long Island City, N.Y.

Circle No. 202 on Inquiry Card

LITERATURE

Connectors

A 12-page catalog lists a full line of rack and panel connectors for data processing, communications equipment, and related applications. Specs are given for 14, 24, 36, and 50-contact microminiature ribbon connectors for rack and panel, cable-to-chassis, and cable-to-cable applications. Cinch Manufacturing Co., Chicago, Ill.

Circle No. 231 on Inquiry Card

Trimming Potentiometers

A 6-page catalog covering the line of square trimming potentiometers calls out and describes every standard and many special models of microminiature trimmers. Included are both humidity-proof and commercial versions of the 3/8" and 1/4" square size. The fold-out brochure has been prepared to facilitate rapid trimmer selection. A picture of each model's configuration with corresponding physical dimensions makes the choice of the proper model for a specific application simple and easy. Techno-Components Corp., Van Nuys, Cal.

Circle No. 219 on Inquiry Card

Constant-Voltage Transformers

Engineering and design data on constant-voltage transformers is contained in a new 12-page manual. Although the units function primarily as voltage regulators, the manual also points out their value in protecting circuit components and reducing circuit costs. The manual presents well-illustrated information on how to design the transformer into an electrical or electronic circuit, and lists the particular type and rating to be selected for a specific job. Sola Electric Co., Elk Grove Village, Ill.

Circle No. 215 on Inquiry Card

Incremental Digital Recorders

New literature details the one-step production of computer compatible magnetic tapes from randomly acquired data by the use of incremental digital tape recorders. The literature includes an 8-page brochure describing three series of incremental recorders, with specs on 200 and 556-bit per inch packing density models, write only and read/write versions, and portable or rack-mounted configurations. The technical material also contains circuit diagrams for interfacing the digital recorders with common data sources including six-bit parallel character sources, serial-by-bit sources, and parallel word sources. Interfacing circuit diagrams also cover incremental readout from the recorder to such devices as plotters, typewriters, and numerical tool controls. Precision Instrument Co., Palo Alto, Cal.

Circle No. 218 on Inquiry Card

Readout Lamps

Most significant new development described in a 16-page catalog is a microminiature multi-filament lamp. An array of filaments within a single lamp can be lighted collectively or individually as specific requirements demand. Readout devices with up to 40 individually controlled lamps per inch for diversified applications, or readout heads that spell out any letter or number as small as ⅛" high within a single multi-filament lamp, and a new "flat-top Pinlite" are among other new developments described in the catalog. Pinlite Div., Kay Electric Co., Fairfield, N.J.

Circle No. 214 on Inquiry Card

Printing Counters

Designed to assist engineers in specifying printing counters for all types of applications, a 4-page bulletin contains complete specifications, operating characteristics, dimensions, and typical installation diagrams. Landis and Gyr, Inc., N.Y., N.Y.

Circle No. 207 on Inquiry Card

LITERATURE

Computer Abstracts

Abstracts of significant articles on topics from aerospace and computer technology, computers and data processing to automation and automatic controls are offered in a publication. As a time-saving service "to those interested in computer engineering, data processing and related subjects," the abstracts are taken from a wide range of current periodicals, and include publication names, dates, and page numbers for convenient reader reference. Mesa Scientific Corp., Santa Ana, Cal.

Circle No. 212 on Inquiry Card

Rack and Panel Connectors

Nine different rack and panel connector series for every standard application are listed in a 32-page catalog. The brochure describes each connector's mechanical, electrical and environmental characteristics. Full-size diagrams illustrate the exact dimensions of the connector, and where applicable, the varieties of inserts available for it. Block diagrams or charts simplify ordering. Amphenol Connector Div., Amphenol-Borg Electronics Corp., Chicago, Ill.

Circle No. 205 on Inquiry Card

Disc Files

A 24-page technical article contains historical background material relating to the development of company's random-access disc files. Also included are notes relating to the philosophy that was used in the development of the disc file, a description of the elements making up the file, statistics on the ability of the file's digital actuator to enable precise repeatability in gaining access to data that is stored in the file, and the reliability concept employed during file design. Bryant Computer Products, Walled Lake, Mich.

Circle No. 223 on Inquiry Card

ADVERTISERS' INDEX

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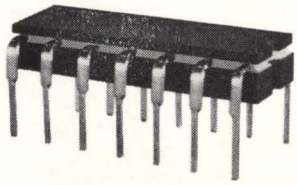

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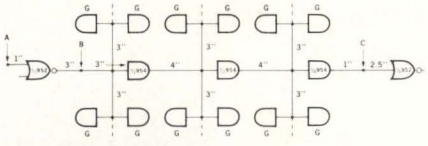
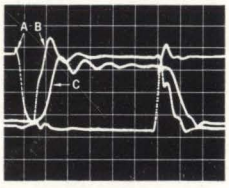
For complete specifications, write for the comprehensive six-page data sheet.

CTμL SPEED

Typical Propagation Delay Test Set-Up (16" open transmission lines)





t_{pd} WAVEFORMS AT FAN-OUT = 5 PER NODE, 16" OPEN TRANSMISSION LINE

VERT = 1.0V cm

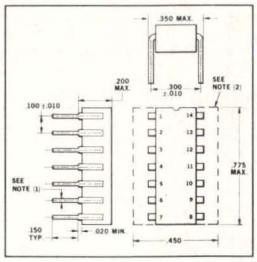
HORIZ = 20 nsec/cm

This test configuration may have as many as 8 logic levels for an average propagation delay of 2.6 to 3.1 nsec per logic decision. The t_{pd} measurements are taken at +1.0V from inverter to inverter.

CTμL PACKAGE

The CTμL package accommodates low-cost commercial assembly methods, including

- flow soldering
- two-sided printed circuit boards
- manual or automatic insertion
- loose drill tolerances
- wide printed circuit lines



1. Leads are a modified hexagon in cross section. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

2. Max. envelope for all planned packages of this design family.

CTμL PRICES	1-24	25-99	100-999 mixed type	100-999 same type
Dual 2-Input Inverter Gate—CTμL 952	$7.50	$6.00	$5.25	$5.00
2-2-3-Input AND Gate—CTμL 953	7.50	6.00	5.25	5.00
Dual 4-Input AND Gate—CTμL 954	7.50	6.00	5.25	5.00
Single 8-Input AND Gate—CTμL 955	7.50	6.00	5.25	5.00
Buffer—CTμL 956	7.50	6.00	5.25	5.00
Dual Rank Flip-Flop—CTμL 957	14.00	11.20	9.80	9.40

FAIRCHILD SEMICONDUCTOR

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