Winbond Electronics Corp.

KEYBOARD CONTROLLER

GENERAL DESCRIPTION

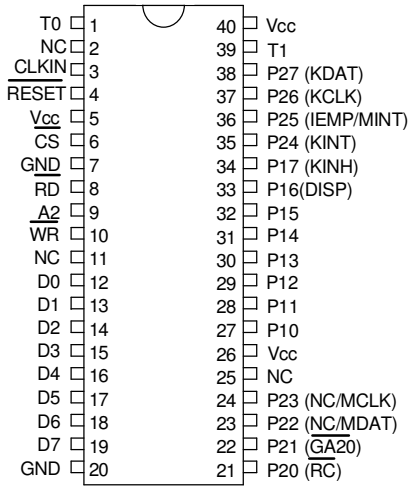
The W83C45 is an 80C42 based keyboard and mouse controller. It is designed to provide the functions needed to interface a CPU to a keyboard or to a PS/2 mouse, and can be used with IBM®-compatible personal computers or PS/2-based systems. The W83C45 incorporates 2K byte software ROM BIOS, and 256 byte data RAM. The W83C45 controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. The controller will interrupt the system when data are placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until the acknowledge signal is received for the previous byte sent.

FEATURES

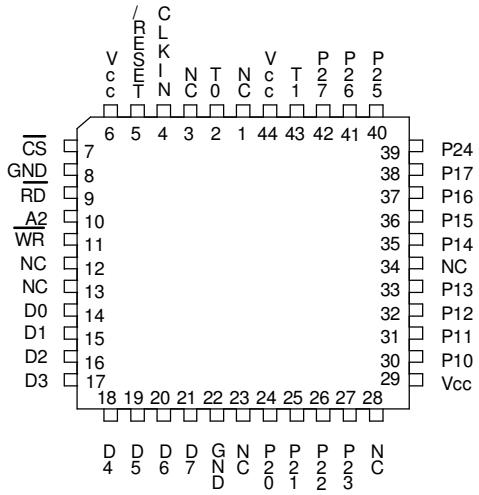
- Supports keyboards of AT mode and PS/2 mode
- Automatically detects PS/2 mode or AT mode
- Supports PS/2 Mouse
- Built in 2 KB Programmable ROM, 256 Byte data RAM
- Programmable ROM code licensed from Phoenix® MultiKey/42
- Operating frequency from 6 MHz to 12 MHz
- IRQ12 can be released when PS/2 mouse is not installed
- Enhanced ESD protection
- 5V operation
- Packaged in 40-pin DIP or 44-pin PLCC

PIN CONFIGURATIONS

40-pin DIP



44-pin PLCC



1.0 PIN DESCRIPTION

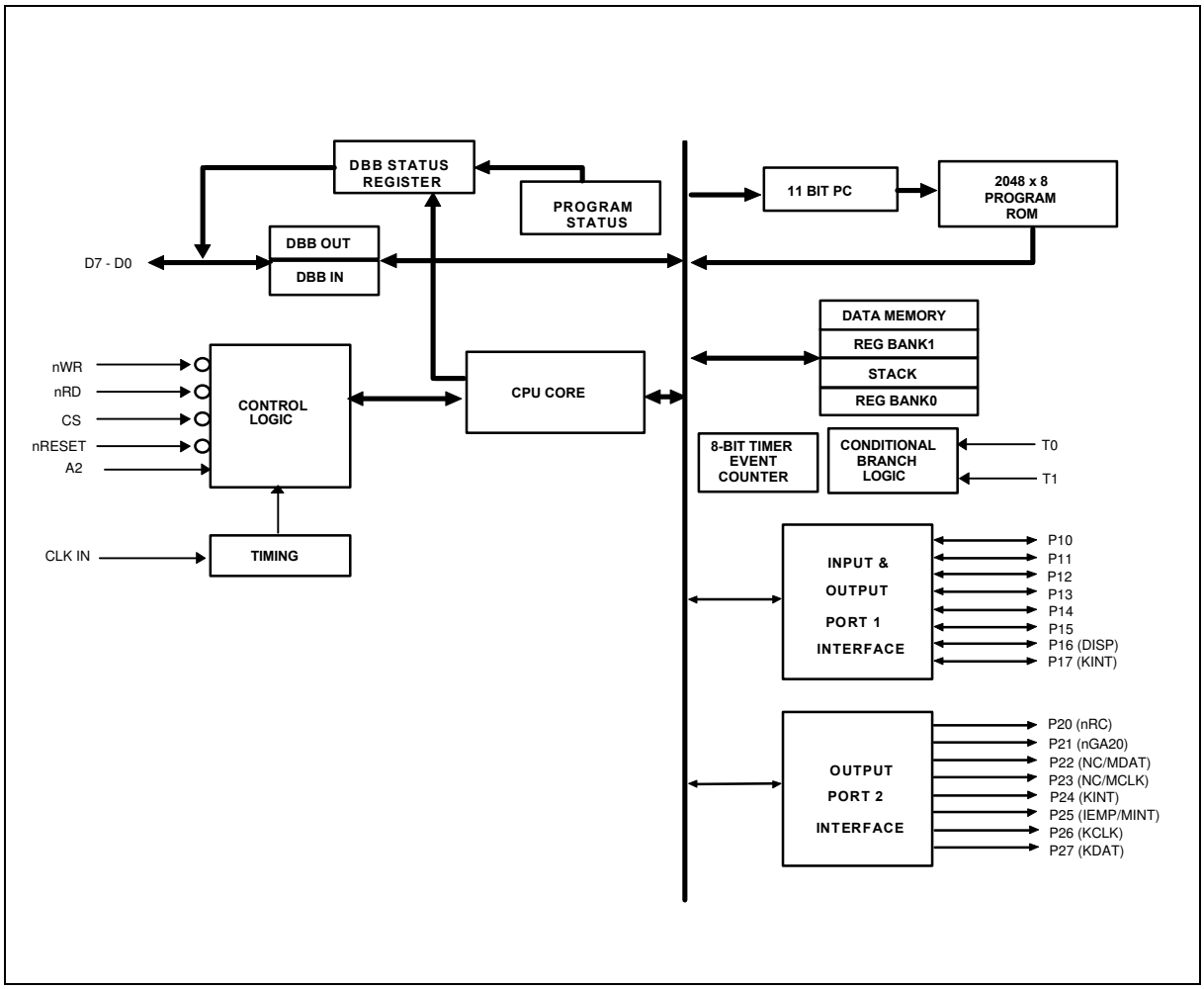
PIN NO.		I/O	NAME	FUNCTION	
(40-pin DIP)	(44-pin PLCC)			AT MODE	PS/2 MODE
1	2	I	T0	K/B Clock Input	K/B Clock Input
2	3	-	NC		
3	4	I	CLKIN	Clock I/P	Clock I/P
4	5	I	$\overline{\text{RESET}}$	Chip Reset	Chip Reset
5	6	-	VCC	Optional +5V Power Supply	Optional + 5V Power Supply
6	7	I	$\overline{\text{CS}}$	Chip Select	Chip Select
7	8	-	GND	Optional Ground Power	Optional Ground Power
8	9	I	$\overline{\text{RD}}$	I/O Read	I/O Read
9	10	I	A2	Connect to Address A2	Connect to Address A2
10	11	I	$\overline{\text{WR}}$	I/O Write	I/O Write
11, 25	1, 12, 13, 23, 28, 34	-	NC	Reserved	Reserved
12, 13, 14, 15, 16, 17, 18, 19	14, 15, 16, 17, 18, 19, 20, 21	I/O	D0–D7	Data Bus D0–D7	Data Bus D0–D7
20	22	-	GND	Ground Power Supply	Ground Power Supply
21	24	O	P20	Bit 0 of Port2 ($\overline{\text{RC}}$: System Reset)	Bit 0 of Port2 ($\overline{\text{RC}}$: System Reset)
22	25	O	P21	Bit 1 of Port2 ($\overline{\text{GA20}}$: GATE A20)	Bit 1 of Port2 ($\overline{\text{GA20}}$: GATE A20)
23	26	I/O	P22	Bit 2 of Port2 (NC: User-defined I/O)	Bit 2 of Port2 (MDAT: Mouse Data Output)
24	27	I/O	P23	Bit 3 of Port2 (NC: User-defined I/O)	Bit 3 of Port2 (MCLK: Mouse Clock Output)
26	29	-	VCC	Optional +5V Power Supply	Optional + 5V Power Supply

PIN DESCRIPTION, continued

PIN NO.		I/O	NAME	FUNCTION	
(40-pin DIP)	(44-pin PLCC)			AT MODE	PS/2 MODE
27	30	I/O PU*	P10	Bit 0 of Port1 (User-defined I/O)	Bit 0 of Port1 (K/B Data Input)
28	31	I/O PU*	P11	Bit 1 of Port1 (User-defined I/O)	Bit 1 of Port1 (Mouse Data Input)
29	32	I/O PU*	P12	Bit 2 of Port2 (User-defined I/O)	Bit 2 of Port2 (User-defined I/O)
30	33	I/O PU*	P13	Bit 3 of Port1 (User-defined I/O)	Bit 3 of Port1 (User-defined I/O)
31	35	I PU*	P14	Bit 4 of Port1 (User-defined I/O)	Bit 4 of Port1 (User-defined I/O)
32	36	I PU*	P15	Bit 5 of Port1 (User-defined I/O)	Bit 5 of Port1 (User-defined I/O)
33	37	I PU*	P16	Bit 6 of Port1 (DISP: Display Select)	Bit 6 of Port1 (DISP: Display Select)
34	38	I PU*	P17	Bit 7 of Port1 (KINH: K/B Inhibit Switch)	Bit 7 of Port1 (KINH: K/B Inhibit Switch)
35	39	O PU*	P24	Bit 4 of Port2 (KINT: K/B OBF O/P Interrupt)	Bit 4 of Port2 (KINT: K/B OBF O/P Interrupt)
36	40	O	P25	Bit 5 of Port2 (IEMP: I/P Buffer Empty)	Bit 5 of Port2 (MINT: Mouse OBF O/P Interrupt)
37	41	O PU*	P26	Bit 6 of Port2 (KCLK: K/B Clock Output)	Bit 6 of Port2 (KCLK: K/B Clock Output)
38	42	O PU*	P27	Bit 7 of Port2 (KDAT: K/B Data Output)	Bit 7 of Port2 (KDAT: K/B Data Output)
39	43	I	T1	K/B Data Input	Mouse Clock Input
40	44	-	Vcc	+5V Power Supply	+5V Power Supply

* Internal pull-up resistor

2.0 BLOCK DIAGRAM



3.0 ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Ambient Operating Temperature	-0 to + 85	°C
Storage Temperature	-65 to + 150	°C
Supply Voltage to Ground Potential	-0.3 to + 7.0	V
Applied Input/Output Voltage	-0.3 to + 7.0	V
Power Dissipation	30	mW

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

4.0 ELECTRICAL CHARACTERISTICS

(Ta = 0° C to + 70° C, V_{DD} = +5V ± 5%)

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTE
V_{DD}	Power Supply	4.75	5.0	5.25	V	
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	3.5			V	
V_{OH}	Output High Voltage	4			V	I_{OH} = - 8 mA
V_{OL}	Output Low Voltage	0.4			V	I_{OH} = - 16 mA
R_{IP}	Min. I/P Resist	10K			Ω	I_{OL} = 8 mA
I_{OFL}	O/P Leakage Current	-10		10	µA	
I_{IH}	I/P Leakage Current	-10		10	µA	
I_{IL}	I/P Leakage Current (Except P10, P11, P12, P13, P14, P15, P16, P17)	-10		10	µA	V_{DD} = 5.5V, V_{IN} = V_{DD}
I_{IL1}	I/P Leakage Current (P10, P11, P12, P13, P14, P15, P16, P17)	-10		550	µA	V_{DD} = 5.5V, V_{IN} = V_{SS}
C_L	O/P Load Capacity	15		50	pF	V_{DD} = 5.5V, V_{IN} = V_{SS}

5.0 OUTPUT BUFFER

The output buffer is an 8-bit read-only register at I/O address hex 60. The keyboard controller uses the output buffer to send the scan code received from the keyboard and data bytes required by commands to the system. The output buffer should be read only when the output buffer full bit in the register is 1.

6.0 INPUT BUFFER

The input buffer is an 8-bit write-only register at I/O address hex 60 or 64. Writing to address hex 60 sets a flag that indicates a data write; writing to address hex 64 sets a flag that indicates a command write. Data written to I/O address hex 60 are sent to the keyboard (unless the keyboard controller is expecting a data byte) following the controller's input buffer only if the input buffer full bit in the status register is set to 0.

7.0 AT MODE OPERATION

7.1 STATUS REGISTER (AT MODE)

The status register is an 8-bit read-only register at I/O address hex 64 that holds information about the status of the keyboard controller and interface. It may be read at any time.

BIT	BIT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag (F0)	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It is set to 0 after a power-on reset
3	Command/data (F1)	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited This bit is cleared when Password is enabled or if P17=0
5	Transmit Time-out	0: No transmit time-out error 1: Transmit time-out error
6	Receive Time-out	0: No receive time-out error 1: Receive time-out error
7	Parity Error	0: Odd parity (no error) 1: Even parity (error)

7.2 Output Port Definition (AT Mode)

BIT	FUNCTION
0	System Reset
1	Gate A20
2	Undefined
3	Undefined
4	Output Buffer Full
5	Input Buffer Empty
6	Keyboard Clock (Output)
7	Keyboard Data (Output)

7.3 Input Port Definition (AT Mode)

BIT	FUNCTION
0	Undefined
1	Undefined
2	Undefined
3	Undefined
4	Undefined
5	Undefined
6	Display Type Switch 0: Primary display attached to color/graphics 1: Primary display attached to monochrome
7	Keyboard Inhibit Switch 0: Keyboard inhibited 1: Keyboard not inhibited

7.4 Test-input Port Definition (AT Mode)

BIT	FUNCTION
0	Keyboard Clock (Input)
1	Keyboard Data (Input)

8.0 PS/2 MODE OPERATION

8.1 Status Register (PS/2 Mode)

BIT	BIT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writting to the system flag bit in the command byte of the keyboard controller. It is set to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte

Status Register (PS/2 Mode), continued

BIT	BIT FUNCTION	DESCRIPTION
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Auxiliary Device Output Buffer	0: Auxiliary device output buffer empty 1: Auxiliary device output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

8.2 Input Port Definition (PS/2 Mode)

BIT	FUNCTION
0	Keyboard Data Input
1	Mouse Data Input
2	Undefined
3	Undefined
4	Undefined
5	Undefined
6	Display Type Switch 0: Primary display attached to color/graphics 1: Primary display attached to monochrome
7	Keyboard Input Switch 0: Keyboard inhibited 1: Keyboard not inhibited

8.3 Output Port Definition (PS/2 Mode)

BIT	FUNCTION
0	System Reset
1	Gate A20
2	Mouse Data Output
3	Mouse Clock Output
4	Keyboard Output Buffer Full Interrupt
5	Mouse Output Buffer Full Interrupt
6	Keyboard Clock Output
7	Keyboard Data Output

8.4 Test-input Port Definition (PS/2 Mode)

BIT	FUNCTION
0	Keyboard Clock Input
1	Mouse Clock Input

9.0 AT MODE COMMANDS (I/O ADDRESS HEX 64)

COMMAND	FUNCTION
20h	Read Command Byte of Keyboard Controller
60h	Write Command Byte of Keyboard Controller
A4h	Test Password Returns 0FAh if Password is loaded Returns 0F1h if Password is not loaded
A5h	Load Password Load Password until a '0' is received from the system
A6h	Enable Password Enable the checking of keystrokes for a match with the password
AAh	Self-test Return 055h if successful self test

BIT	BIT DEFINITION
7	Reserved
6	IBM PC Compatible Mode
5	IBM PC Mode
4	Disable Keyboard
3	Inhibit Override
2	System Flag
1	Reserved
0	Enable Output Buffer Full Interrupt

AT MODE Commands (I/O Address HEX 64), continued

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>ABh</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>K/B Clock Line is Stuck Low</td></tr>
<tr><td>02</td><td>K/B Clock Line is Stuck High</td></tr>
<tr><td>03</td><td>K/B Data Line is Stuck Low</td></tr>
<tr><td>04</td><td>K/B Data Line is Stuck High</td></tr>
</table></td></tr>
<tr><td>ADh</td><td>Disable Keyboard Feature</td></tr>
<tr><td>AEh</td><td>Enable Keyboard Interface</td></tr>
<tr><td>C0h</td><td>Read the input Port(P1) and send data to the system</td></tr>
<tr><td>C1h</td><td>Continuously puts the lower four bits of Port1 into STATUS register</td></tr>
<tr><td>C2h</td><td>Continuously puts the upper four bits of Port1 into STATUS register</td></tr>
<tr><td>C3h</td><td>Make P25(MIRQ) tri-state by writing this command twice consecutively</td></tr>
<tr><td>C4h</td><td>Make P25(MIRQ) released from tri-state by writing this command twice consecutively</td></tr>
<tr><td>D0h</td><td>Send Port2 value to the system</td></tr>
<tr><td>D1h</td><td>Only set/reset GateA20 line based on the system data bit 1</td></tr>
<tr><td>D2h</td><td>Send data back to the system as if it came from keyboard</td></tr>
<tr><td>E0h</td><td>Reports the state of the test inputs</td></tr>
<tr><td>FXh</td><td>F0h-FFh, Pulse only RC(the reset line) low for 6µS if Command byte is even</td></tr>
</table>

10.0 PS/2 MODE COMMANDS (I/O ADDRESS HEX 64)

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte of Keyboard Controller</td></tr>
<tr><td>60h</td><td>Write Command Byte of Keyboard Controller
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>7</td><td>Reserved</td></tr>
<tr><td>6</td><td>IBM Keyboard Translate Mode</td></tr>
<tr><td>5</td><td>Disable Auxiliary Device</td></tr>
<tr><td>4</td><td>Disable Keyboard</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>2</td><td>System Flag</td></tr>
<tr><td>1</td><td>Enable Auxiliary Interrupt</td></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
</table></td></tr>
<tr><td>A4h</td><td>Test Password
Returns 0Fah if Password is loaded
Returns 0F1h if Password is not loaded</td></tr>
<tr><td>A5h</td><td>Load Password
Load Password until a ‘0’ is received from the system</td></tr>
<tr><td>A6h</td><td>Enable Password
Enable the checking of keystrokes for a match with the password</td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Auxiliary Device "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Auxiliary Device "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
</table></td></tr>
<tr><td>AAh</td><td>Self-test
Returns 055h if successful self test</td></tr>
</table>

PS/2 MODE Commands (I/O Address HEX 64), continued

COMMAND	FUNCTION
ABh	Interface Test BIT 00: No Error Detected BIT 01: Keyboard "Clock" line is stuck low BIT 02: Keyboard "Clock" line is stuck high BIT 03: Keyboard "Data" line is stuck low BIT 04: Keyboard "Data" line is stuck high
ADh	Disable Keyboard Interface
AEh	Enable Keyboard Interface
C0h	Read Input Port(P1) and send data to the system
C1h	Continuously puts the lower four bits of Port1 into STATUS register
C2h	Continuously puts the upper four bits of Port1 into STATUS register
C3h	Make P25(MIRQ) tri-state by writing this command twice consecutively
C4h	Make P25(MIRQ) released from tri-state by writing this command twice consecutively
D0h	Send Port2 value to the system
D1h	Only set/reset GateA20 line based on the system data bit 1
D2h	Send data back to the system as if it came from Keyboard
D3h	Send data back to the system as if it came from Auxiliary Device
D4h	Output next received byte of data from system to Auxiliary Device
E0h	Reports the status of the test inputs
FXh	F0h-FFh, Pulse only RC(the reset line) low for 6μS if Command byte is even

11.0 AC TIMING

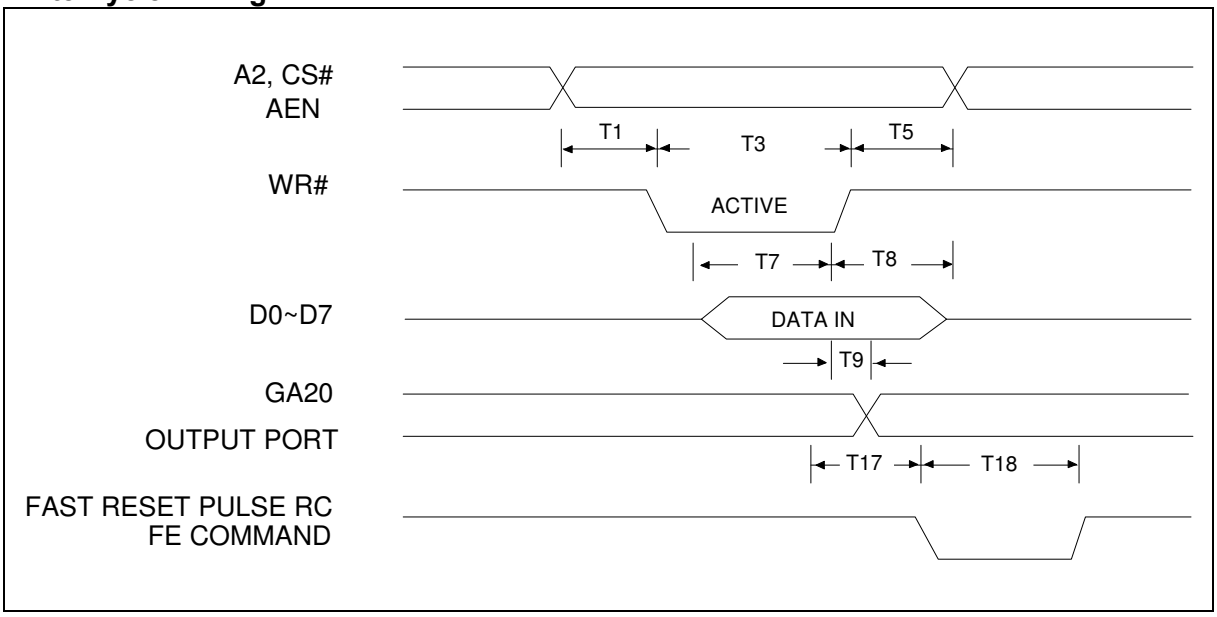
ITEM	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS

AC TIMING, continued

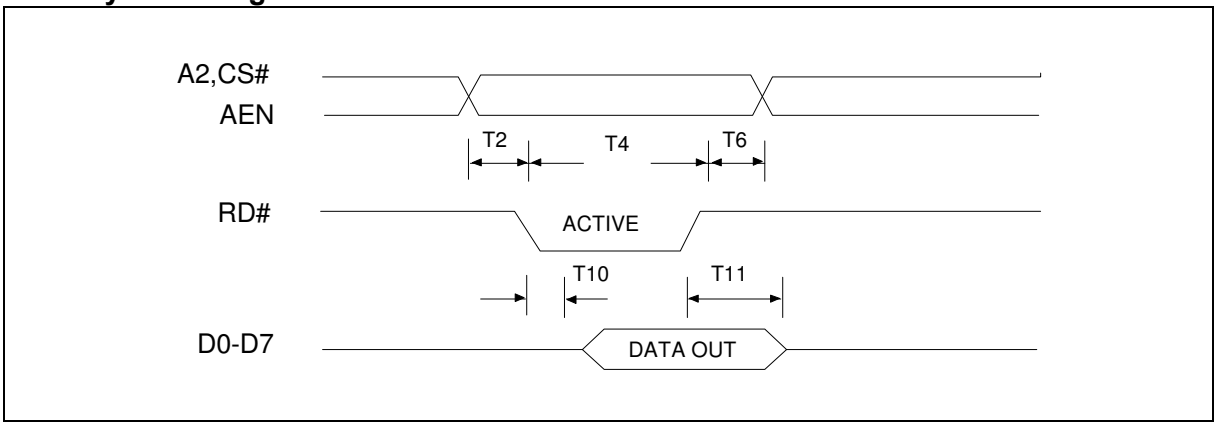
ITEM	DESCRIPTION	MIN.	MAX.	UNIT
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay		40	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	µS
T13	K/B Clock Period	20		µS
T14	K/B Clock Pulse Width	10		µS
T15	Data Valid Before Clock Falling (RECEIVE)	4		µS
T16	K/B ACK After Finish Receiving	20		µS
T17	RC Fast Reset Pulse Delay (8 MHz)	2	3	µS
T18	RC Pulse Width (8 MHz)	6		µS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		µS
T21	Input Clock Period (6–12 MHz)	83	167	nS
T22	Duration of CLK inactive	30	50	µS
T23	Duration of CLK active	30	50	µS
T24	Time from inactive CLK transition, used to time when the auxiliary device sample DATA	5	25	µS
T25	Time of inhibit mode	100	300	µS
T26	Time from rising edge of CLK to DATA transition	5	T28-5	µS
T27	Duration of CLK inactive	30	50	µS
T28	Duration of CLK active	30	50	µS
T29	Time from DATA transition to falling edge of CLK	5	25	µS
T30	Mode detect signal after P10 goes high	Typical 1 mS		
T31	High pulse of mode detect signal	Typical 220 µS		
T32	Low pulse of mode detect signal	Typical 220 µS		
T33	Mode detect signal after RESET goes high	Typical 1 mS		
T34	Time out of AT mode‘ s mode detect signal	Typical 64 mS		

12.0 TIMING WAVEFORMS

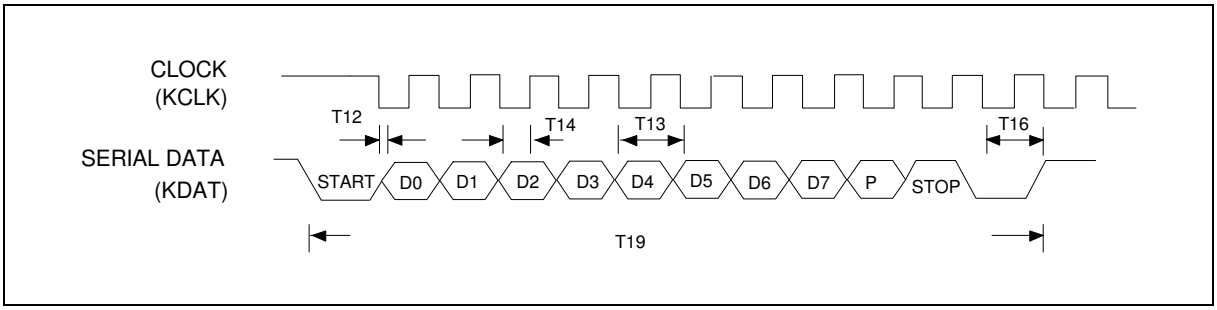
Write Cycle Timing



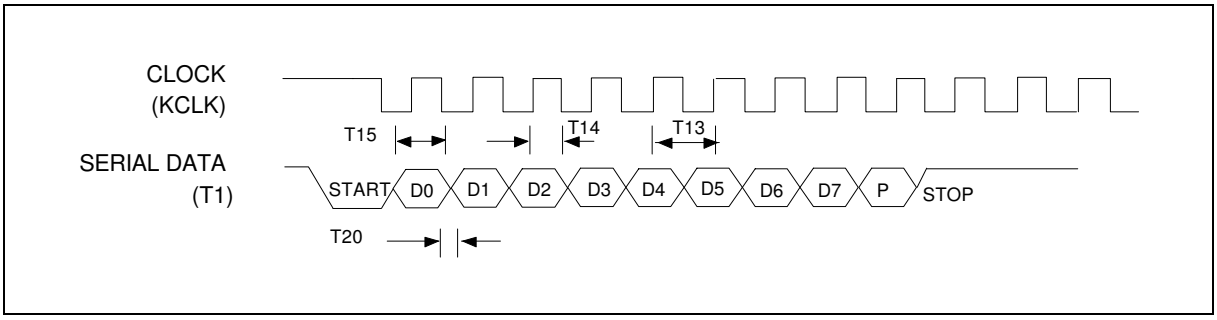
Read Cycle Timing



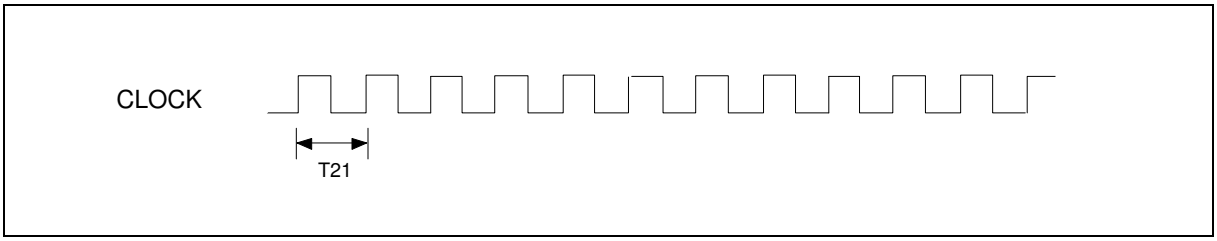
Send Data to K/B



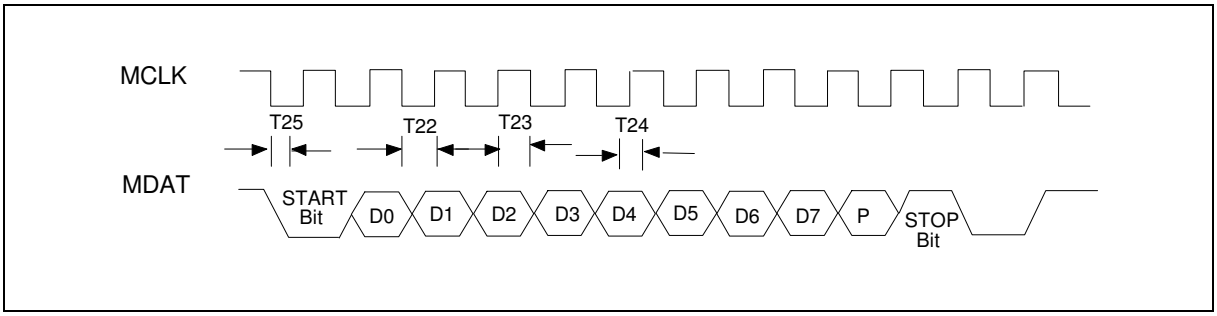
Receive Data from K/B



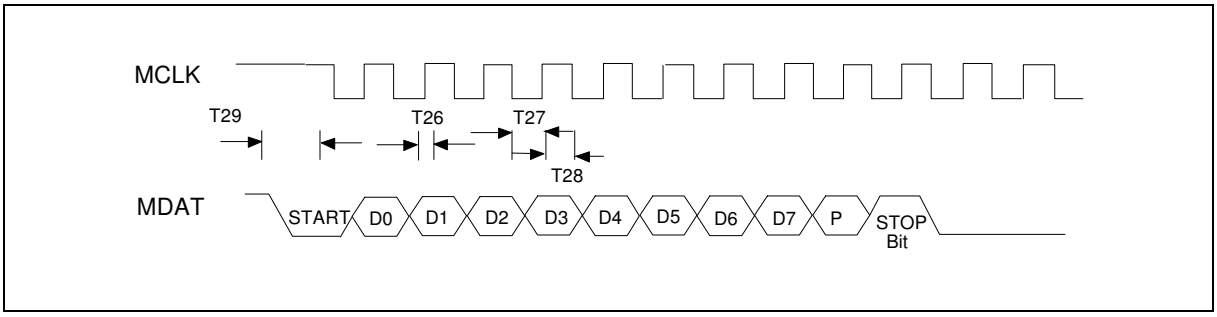
Input Clock



Send Data to Mouse

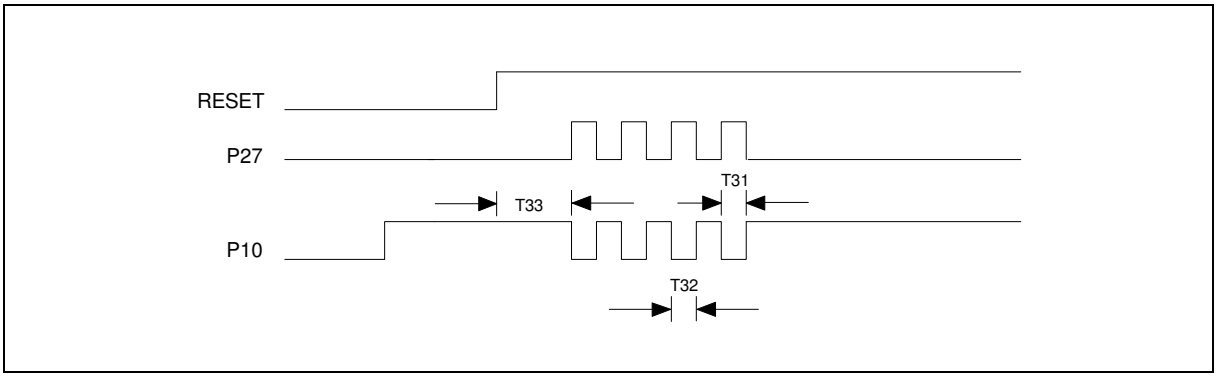


Receive Data from Mouse



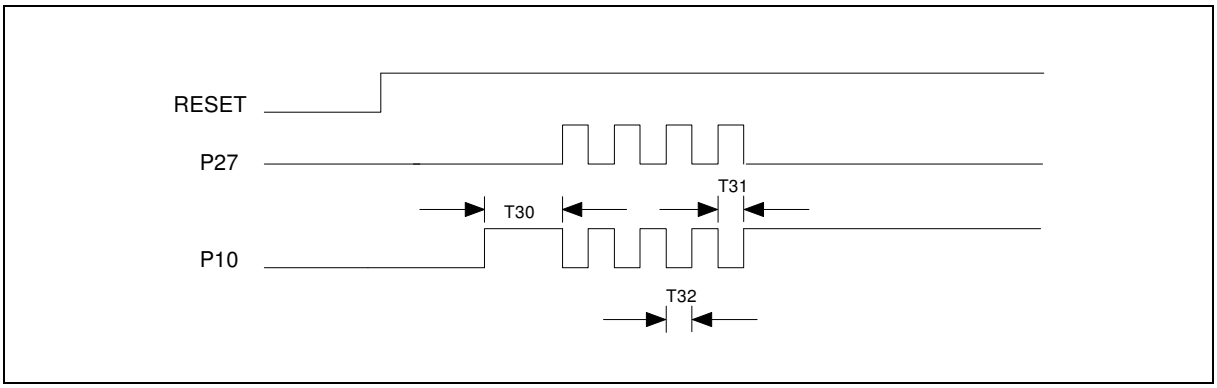
PS2 Mode's Mode Detect

(P10 will be released to high by keyboard before RESET goes high.)



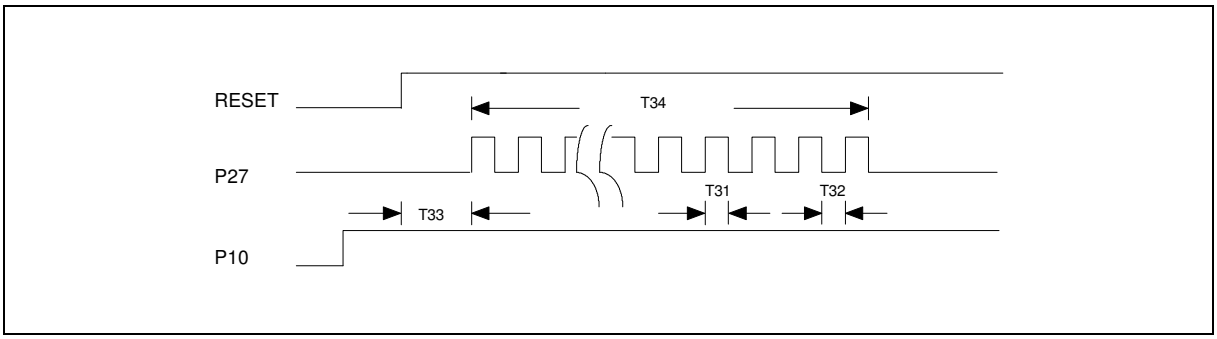
PS2 Mode's Mode Detect

(P10 will be released to high by keyboard after RESET goes high.)



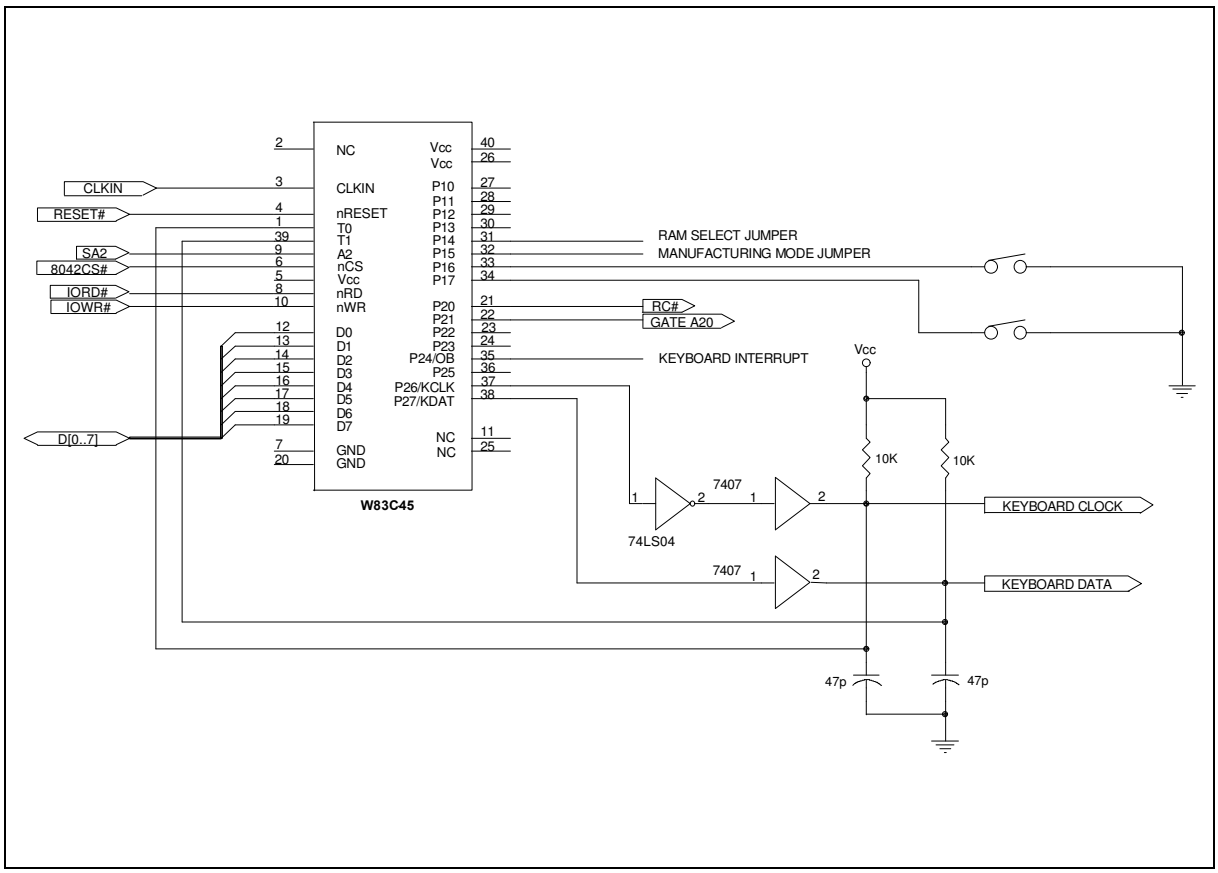
AT Mode's Mode Detect

(P10 is internal pulled high. As there is no external loop between P27 and P10, P27 issues pulse until time out.)

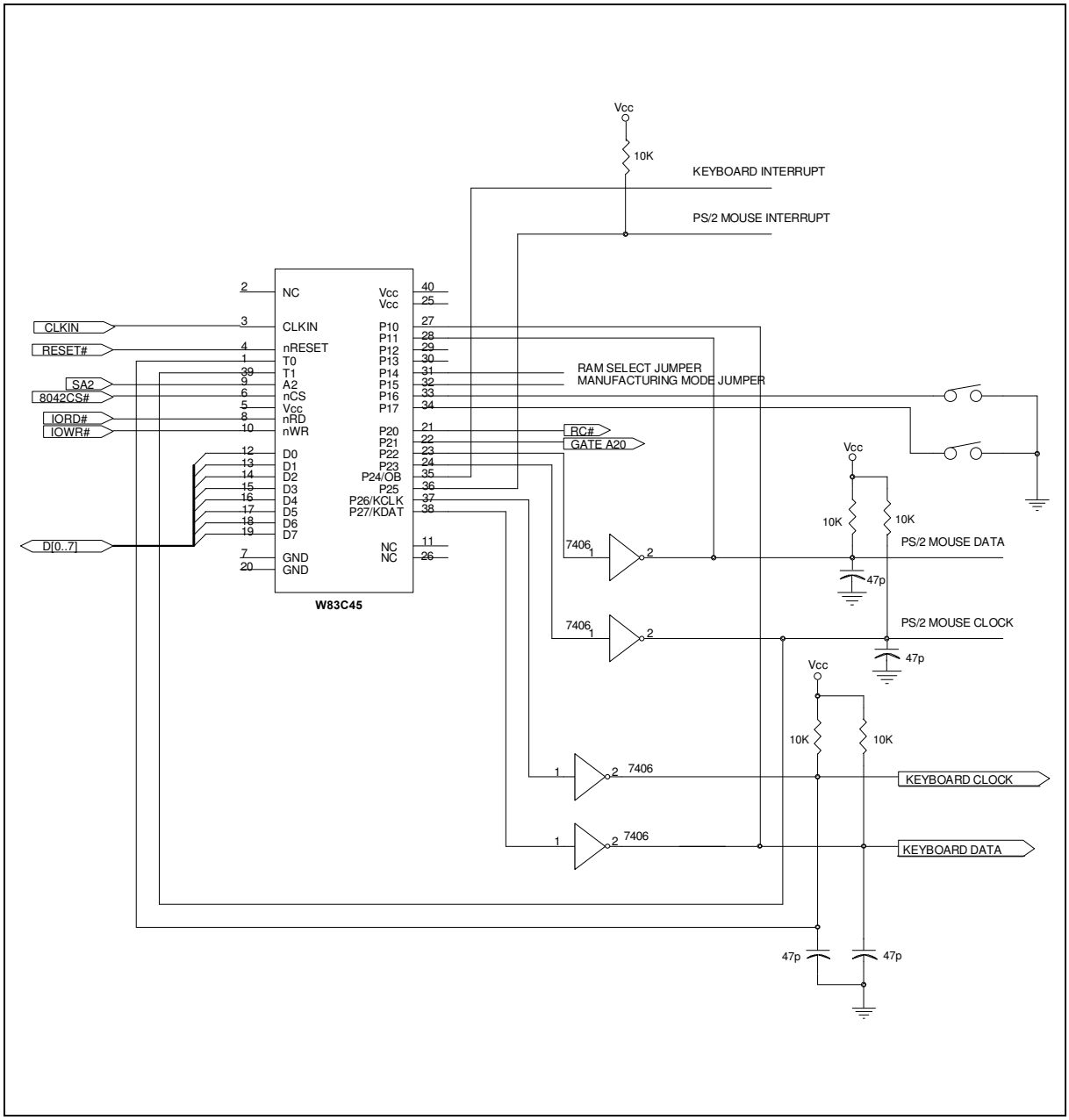


13.0 TYPICAL APPLICATION CIRCUITS

Application for AT Mode

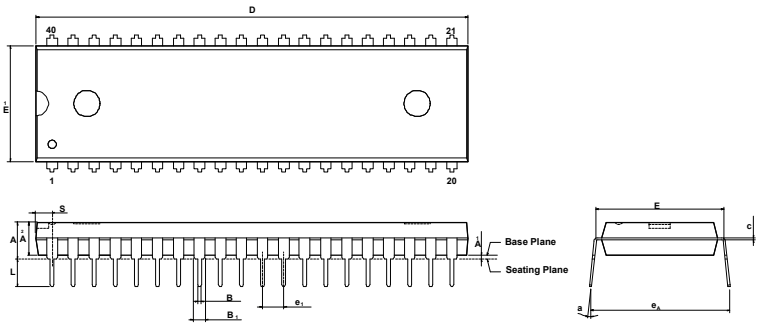


Application for PS/2 Mode



14.0 PACKAGE DIMENSIONS

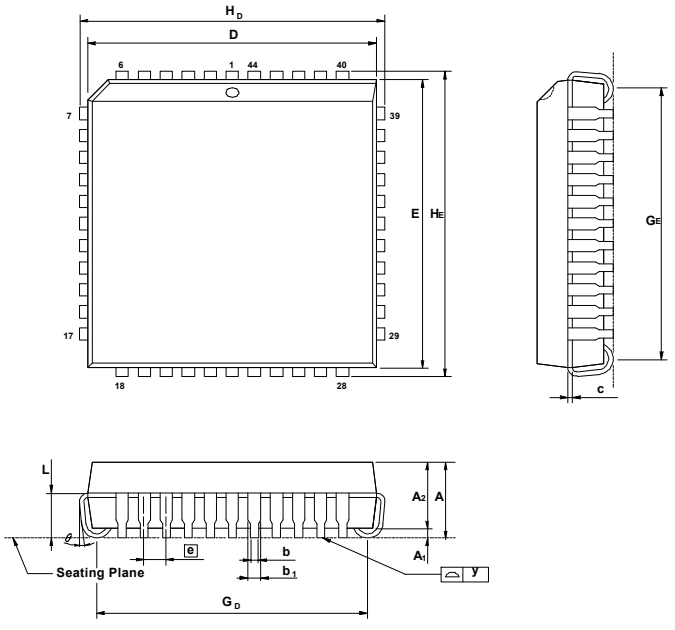
40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

Notes:
1. Dimensions D Max & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

44-pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.70
A_1	0.020	—	—	0.51	—	—
A_2	0.145	0.150	0.155	3.68	3.81	3.94
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
y	—	—	0.004	—	—	0.10

Notes:
1. Dimensions D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

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