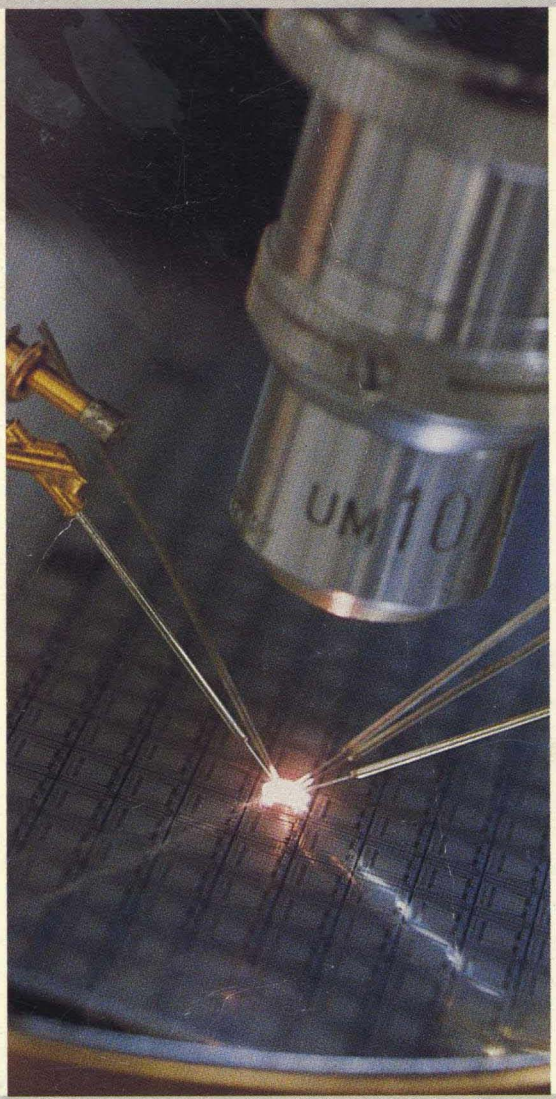
Supertex

Supertex



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Supertex Inc. Life Support Policy

As a general policy, Supertex Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the Supertex product can be reasonably expected to cause failure of the life support device or to significantly affect its safety or effectiveness. Supertex will not knowingly sell its products for use in such applications unless it receives an adequate "products liability indemnification insurance agreement", satisfactory to Supertex, stating that the risks of injury or damage have been minimized, that the customer assumes all such risks, and that the liability of Supertex is adequately covered in the customer's insurance policy.

Examples of devices considered to be life support devices are neonatal oxygen analyzers, nerve stimulators (for any use), autotransfusion devices, blood pumps, defibrillators, arrhythmia detectors and alarms, pacemakers, hemodialysis systems, peritoneal dialysis systems, ventilators of all types, infusion pumps, and any other devices designated as "critical" by the FDA. The above are representative examples only and are not intended to be conclusive on any other life support device.

General

This catalog has been carefully checked and is believed to be reliable; however, no responsibility is assumed for possible omissions or inaccuracies. Specifications are subject to change without notice.

Supertex cannot assume responsibility for use of circuitry described; no circuit patent licenses are implied; and Supertex reserves the right to change said circuity at any time without notice. Liability of Supertex to circuits it manufactures is limited to the replacement of such circuits if they are determined to be defective due to workmanship and not due to misuse or mishandling.

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Product Nomenclature/Ordering Information

DMOS Proprietary Products

V N 0 1 0 9 N 3

FAMILY TYPE	POLARITY	FAMILY NUMBER	BVDSS DIVIDED BY 10	PACKAGE TYPE
A = Lateral DMOS Arrays	N = N-Channel	01	02	N1 = TO-3
		02	04	N2 = TO-39
		03	06	N3 = TO-92
T = Low Threshold DMOS Discretes	P = P-Channel	05	09	N5 = TO-220
		06	10	N6 = 14-Pin Plastic DIP
		11	16	N7 = 14-Pin Ceramic DIP
V = Vertical DMOS Discretes & Quads	C = Complementary (2N & 2P)	12	20	N9 = TO-52
		13	24	NA = 18-Pin Plastic DIP
		21	30	NB = 18-Pin Ceramic DIP
	Q = Arrays	22	35	NE = 16-Terminal Ceramic LCC
			40	NF = 20-Terminal Ceramic LCC
			45	WG = 20 Lead SOW
			50	ND = Die in Waffle Pack
			55	NW = Die in Wafer Form
			60	
			(e.g., 09 = 90V)	

CMOS Products

Encoder / Decoder

E D - 5 P

FAMILY TYPE	NUMBER OF ADDRESS BITS	PACKAGE TYPE
ED = Programmable Encoder/Decoder	ED-5 = 5	PJ = Molded Plastic Surface Mount J-Lead Chip Carrier
DC = Data Coder	DC-7 = 7	P = Molded Plastic DIP
ET = Encoder/Transmitter	ED-9 = 9	X = Dice
	ED-11 = 11	WG = Small Outline Surface Mount
	ET-13 = 13	
	ED-15 = 15	

Smoke Detectors

S D 2 P

FAMILY TYPE	PRODUCT DESIGNATOR	PACKAGE TYPE
SD = Smoke Detectors	2 3A	P = Molded Plastic DIP X = Dice

HVIC Products

R B H V 0 1 0 6 C

HI-REL	FAMILY TYPE	PRODUCT DESIGNATOR	ABSOLUTE MAX VOLTAGE DIVIDED BY 10	PACKAGE TYPE
RB = Hi-Rel 883 type processing RC = Mil-Temp Testing only	HV = High Voltage IC	01 46 02 51 03 52 04 53 05 54 06 55 10 56 12 57 13 58 14 60 15 341 16 343 17 345 18 348 30 500 41 501 42 6810 45	04 14 25 06 16 27 08 18 30 10 20 12 22 (e.g., 22 = 220V)	P = Plastic DIP C = Ceramic Side Brazed D = CERDIP X = Dice LC = LCC Ceramic CF = Ceramic Leaded Chip Carriers with Flat Leads CS = Ceramic Chip Carrier-STD Bent Leads CR = Ceramic Chip Carrier-Reverse Bent Leads DG = CERDIP Gullwing PG = Plastic Gullwing WG = SOW Gullwing DJ = Quad CERDIP J Lead PJ = Quad Plastic J Lead

Supertex inc.

Company Profile

Success Through Innovation

Founded in 1976, Supertex designs and manufactures complex proprietary and industry-standard integrated circuits (ICs) and discrete components for a select range of diverse markets, including the medical, data processing, military, telecommunications, instrumentation, and consumer product industries. Throughout the years the company has developed advanced technologies utilizing high-performance Complementary Metal Oxide Semiconductors (CMOS) and Double-Diffused MOS (DMOS) processes.

In 1980, Supertex pioneered SMART POWER high voltage integrated circuitry with its proprietary HVCMOS® technology, a merging of the CMOS and DMOS process technologies onto one chip. SMART POWER chips have the "brains" and low power consumption of CMOS ICs and the high-voltage output of DMOS power transistors. These advanced HVCMOS ICs, as well as Supertex's families of CMOS and DMOS products, provide performance and cost benefits to give customers a competitive edge in developing new products.

Supertex now focuses on two process technologies, DMOS and HVCMOS, which allow for a varied product mix of integrated circuits and MOS power field effect transistors (FETs) and arrays. The company's products are targeted for application-specific markets, such as ultrasound imaging for medical electronics, flat-panel display terminals, and high reliability products for military systems. Supertex has demonstrated technological leadership in specific product areas that has earned the company international as well as domestic recognition.

Product Development Milestones

Supertex has continued the commitment to new product and technology development that enhances and complements existing product lines. Supertex is recognized as a world leader in SMART POWER and POWER MOSFET innovations. While responding to market demands for current products, the company is also maintaining a leadership position as an industry innovator in our product niches as evidenced by the product development milestones listed below:

Introduced

1976 Industry leader in CMOS Wafer Foundry technology and production.

1977 Forerunner in VMOS Silicon-gate technology development.

Patent filed for High Power VMOS process.

First U.L. approved Smoke Detector IC.

First in the industry to introduce P-Channel VMOS Power FETs.

1978 State-of-the-art High Voltage (500V) Power Fet introduced.

1979 Widest product offering CMOS Encoder/Decoder ICs, using Manchester coding.

Development of combined Bipolar and DMOS technologies (Superfet™).

World's first 32K CMOS ROM commercially available.

High Voltage DMOS/CMOS IC technology developed for Ultra Sonic Imaging.

1980 Industry Leader in Photo Electric Smoke Detection IC.

Introduction of High Voltage DMOS Lateral Arrays.

Highest density 64K and 128K CMOS ROMs introduced.

1981 First to develop fully TTL compatible High Speed CMOS HCT Octal Interface Logic Family of 22 ICs.

1982 First fully integrated Electroluminescent (EL) Flat Panel Display Drive chip set (HVO1/HVO2).

CMOS Encoder/Decoder with byte-wide Data Capacity (DC-7) introduced.

1983 First to introduce 64-line density EL Display Drivers (HVO3/HVO4).

1984 First major printer HVIC design win.

First Hi-Rel HCT in leadless chip carriers.

MVIC (40-Volt) and HVIC technologies developed for wafer foundry production.

1985 First Hi- Rel HVCMOS display drivers in industry (RB HVO1/HVO2).

Registered HVCMOS trademark.

1986 First to introduce 32-Channel high voltage Matrix-addressed LCD Driver (HV60) with three state outputs.

Introduction of 32-Channel HV51 through HV54 low power flat panel display drivers, suitable for portable applications.

1986 Introduction of industry's first low-threshold P-Channel power MOSFET family.

First to introduce 8-Channel high voltage level translator chip (HTO1).

Introduction of 84-lead, surface-mount gullwing packaged for EL flat panel display drivers.

1987 Introduction of 32-Channel P-Channnel EL row driver, HV41 and 42 to be used for high voltage, high current push-pull applications in conjunction with HV51 and 52.

Expanding the 32-channel display driver product line to a total of 12 products.

Introduction of low power 32-Channel AC plasma flat panel display drivers (HV500 and HV501).

Custom Wafer Foundry

Supertex specializes in CMOS and DMOS Wafer Foundry production providing state-of-the-art wafer fabrication for Customer-Owned-Tooling (C.O.T.) production. Standard as well as modified processes can be produced per specific customer requirements thus providing the highest possible yields and quality. Engineering runs and preproduction volumes can be run with very short throughput time (i.e., 3 weeks typically). In addition Supertex can also support back-end packaging and testing needs.

The following table lists the process types that can be accommodated by Supertex in Custom Wafer Foundry production:

Process Type	Preferred Data Format	Minimum Feature Size
Metal-Gate CMOS	Masks	4μm
Metal-Gate PMOS	Masks	4μm
High Voltage Silicon-Gate HVCMOS	Masks	4μm

Power MOS Transistor Electrical Performance

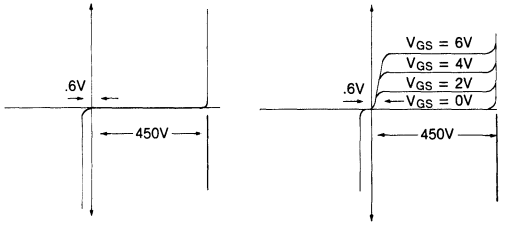
The electrical behavior of power MOS transistors has been explained by numerous authors. A different, and non-traditional way of viewing their behavior arises when the device structure is closely examined. The source and body regions comprise one side of a diode, with the drain region being the other side. A voltage on the gate allows carriers to flow from source to drain through an induced surface channel. Figure 1A shows the forward and reverse current vs. voltage characteristics of a diode, while Figure 1B shows the current vs. voltage characteristics of a power MOS transistor.

A power MOS transistor is characterized by a set of parameters different in many ways from a bipolar transistor. The parameters specified in a power MOS transistor data sheet are defined and briefly explained below:

A. $V_{GS(TH)}$ – The gate threshold voltage. It is defined as the voltage from gate to source required to produce a specified drain current. For ease of measuring, the drain is commonly shorted to the gate. (The measurement circuit is shown in Figure 2.)

Threshold current is usually measured at a current in the range of 1 to 10mA. (Threshold voltage measurement can be normalized to the amount of source perimeter when comparing different size transistors. Full current is usually obtained at $V_{GS} = V_{GS(TH)} + 8$ volts (N-channel). The threshold voltage is a function of temperature as shown in Figure 3 for a 500 volt Supertex VN03 transistor. The decrease in the measured value of $V_{GS(TH)}$ is primarily caused by thermally generated carriers or leakage current that add to the induced surface current flow, thus decreasing the amount of applied voltage needed to obtain a specified current.

B. I_{GSS} – The gate to body leakage current. It is measured with drain and source at ground, and gate biased to specified voltage. NOTE: Due to input capacitance, large die size MOS transistors may prove difficult to measure with automatic test equipment, unless a preconditioning test is performed to charge the gate capacitance prior to test. (See Figure 4 for the measurement circuit.)



A. Diode characteristics B. Gated diode characteristics

Figure 1.

This leakage current results from current flow through the insulating layer of silicon dioxide surrounding the gate. Typical DC-leakage currents are in the picoampere range between the temperatures of -55°C and +200° C. This value is well below the level of concern in most power conversion circuits. When an on-chip diode is incorporated between the gate and the source, the leakage current, which is that of a reverse-biased diode, doubles approximately every 10°C.

C. I_{DSS} – The zero gate voltage drain current or offstate leakage current. It is determined by applying specified voltage from drain to source (with gate shorted to source) and measuring the resulting current. (See Figure 5 for the measurement circuit.)

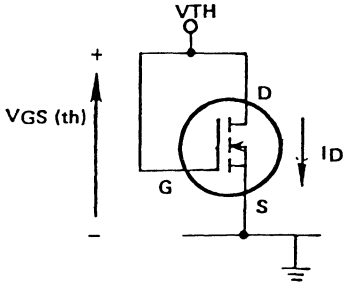


Figure 2. N-Channel $V_{GS(th)}$ Measurement

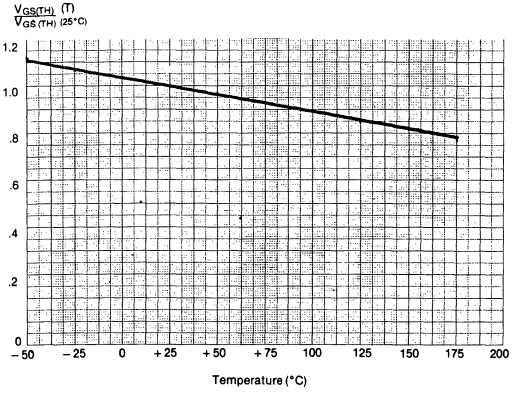


Figure 3. Normalized $V_{GS(th)}$ vs. Temperature for the VN03 Transistor

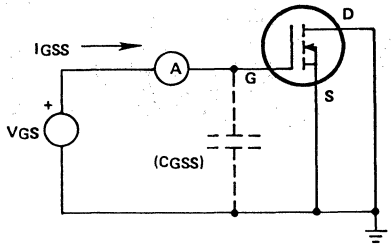


Figure 4. N-Channel I_{GSS} Measurement

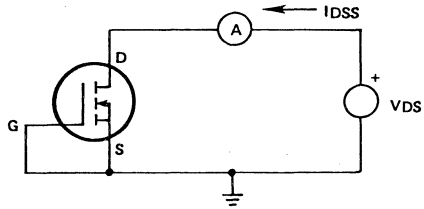


Figure 5. N-Channel I_{DSS} Measurement

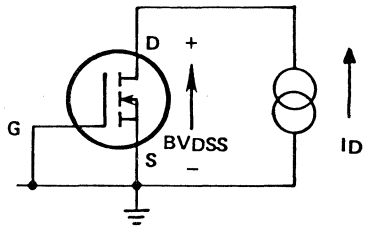


Figure 6. N-Channel BV_{DSS} Measurement

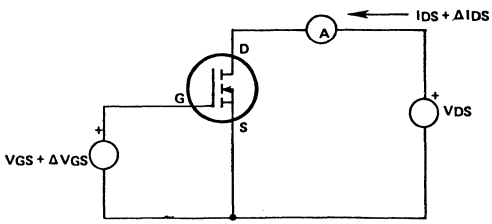


Figure 7. N-Channel G_{fs} Measurement

This leakage current is that of a reverse-biased diode. As with a reverse-biased diode, this current is a measure of the integrity of the structure and may degrade under extremes of voltage and temperature.

D. BV_{DSS} – The breakdown voltage of drain to source with gate shorted to source. It is determined by forcing a specified current from drain to source and measuring the resulting voltage. Properly designed DMOS transistors should not have a latchback breakdown and a low current measurement is sufficiently accurate. (See Figure 6 for the measurement circuit.)

This parameter is most likely to degrade if exceeded for an extended period of time in high voltage applications, because of the large current (and, hence, high power dissipation that may occur). A lower clamping breakdown voltage diode from source-to-drain will prevent degradation of the parameter.

E. g_{fs} or g_m – The small signal forward transconductance. It is the ratio of $\Delta I_D/\Delta V_{GS}$ measured for a 10% change in drain current at a specified quiescent drain bias point.

This parameter depends on device structure as shown in the equation below (see Figure 7 for measurement circuit):

$$g_m = \frac{\mu off \; Z \epsilon_{OX}}{Lt_{OX}} (V_{GS} - V_{GS(TH)})$$

where $\frac{Z}{L} = \frac{\text{Source perimeter}}{\text{Channel length}}$

V_{off} = Effective carrier mobility

ϵ_{OX} = Gate Dielectric constant

t_{OX} = Gate oxide thickness

These parameters are shown in Figure 8. The forward transconductance is proportional to source perimeter, hence proportional to chip area. For a given device area, maximizing the source perimeter results in a maximum value of gm. This parameter is also increased by decreasing the gate dielectric thickness, but this approach limits the total voltage swing on the gate because of the dielectric strength of silicon dioxide (60V/1000Å of SiO_2). Typical gate oxide thicknesses are in the 1000Å range. In power MOS structures, the transconductance vs. V_{GS} varies as shown in Figure 9 for a 500 Volt VNO3 power MOSFET.

F. $R_{DS(ON)}$ – The static drain-source on-state resistance. It is measured as the drain-source voltage divided by the drain current at specified values of drain current and gate source voltage. (See Figure 10 for the measurement circuit.)

The on-state resistance of a high voltage MOS transistor is dominated by the resistance of the drain region. For a given breakdown voltage and device area, there is a minimum value of $R_{DS(ON)}$. The variations in source geometrics and body-to-drain breakdown structures discussed earlier are all aimed at realizing this minimum $R_{DS(ON)}$ value. In device operation, $R_{DS(ON)}$ may appear to be considerably higher than at room temperature. This behavior occurs because the heating of the device decreases the carrier mobility, thus reducing the current for a given voltage. This

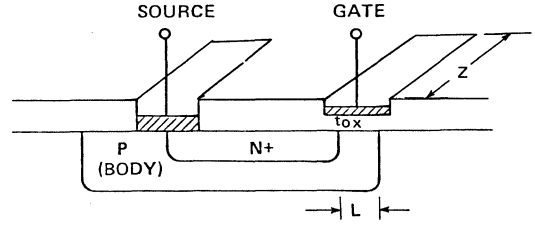


Figure 8. Parameters Affecting MOSFET Transconductance

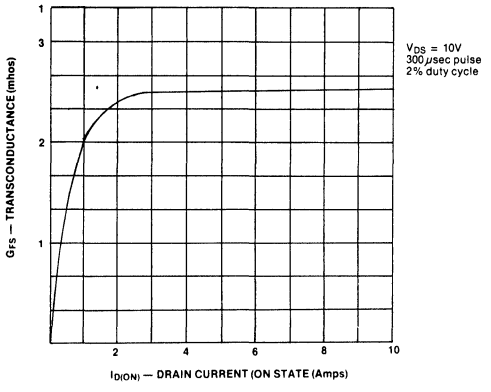


Figure 9A.

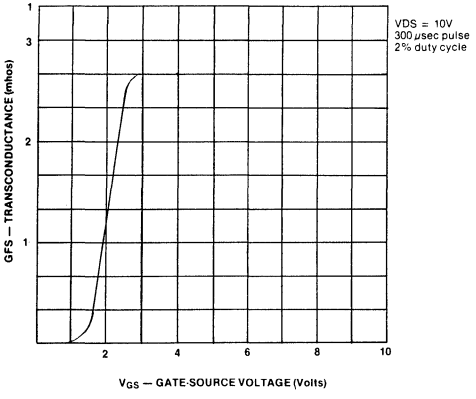


Figure 9B.

Figure 9. Transconductance vs. Drain Current or Gate-Source Voltage for the VN03

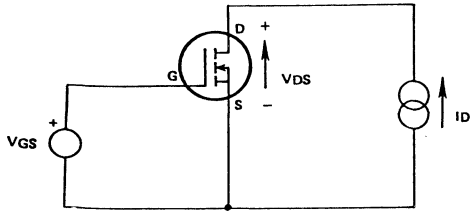


Figure 10. N-Channel $R_{DS(ON)}$ Measurement

behavior for a 500 volt VNO3 transistor is shown in Figure 11. This negative feedback characteristic is the key to power MOSFETs thermal stability.

G. $I_{D(ON)}$ – The on-state drain current. It is measured at specified values of drain-source and gate-source voltage. NOTE: To reduce heating of the device, this should be performed in a pulse mode, or with an adequate heat sink. (See Figure 12 for measurement circuit.)

The on-state drain current is proportional to the amount of source perimeter and the total chip area. Since current flow causes device heating, the pulsed value of $I_{D(ON)}$ is considerably greater than the steady state value because of the increasing value of $R_{DS(ON)}$ with temperature. This specific behavior is shown by the dotted line for the VNO3 in Figure 13.

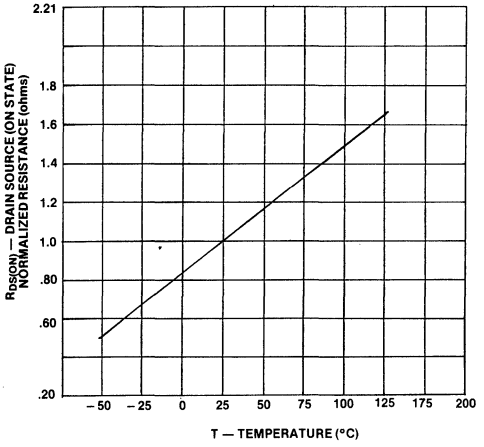


Figure 11. $R_{DS(ON)}$ as a Function of Temperature for the VN03

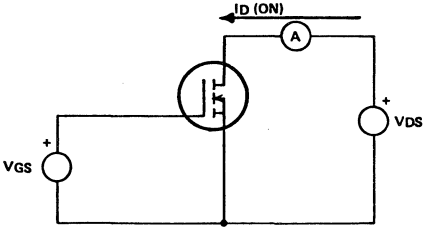


Figure 12. N-Channel $I_{D(ON)}$ Measurement

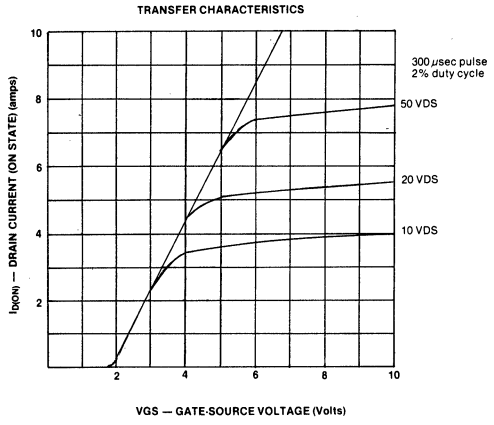


Figure 13. $I_{D(ON)}$ as a Function of Gate-Source Voltage for the VN03

H. Capacitances – Power MOSFETs are characterized by three capacitances:

1. C_{ISS}: Input capacitance
2. C_{OSS}: Common source capacitance
3. C_{RSS}: Reverse transfer capacitance

These measured capacitances are related to device structure as shown in Figure 14. We see from this figure that the value of C_{ISS} for a dual layer access structure will be correspondingly greater per unit area than an interdigitated structure. With these capacitances, a simple small signal equivalent circuit may be derived as shown in Figure 15. This equivalent circuit is also useful in more elaborate transient analysis. These three capacitances have been measured over temperature, with no appreciable temperature dependence found.

Conclusion

The power MOS transistor is a device with its own set of electrical parameters. These parameters depend on the device structure. The success with which power MOS transistors are used will depend on a designer's understanding of these electrical parameters and their limits. This article has attempted to link the performance of power MOS transistors to their optimum design and processing and to establish some physical limits for optimum performance.

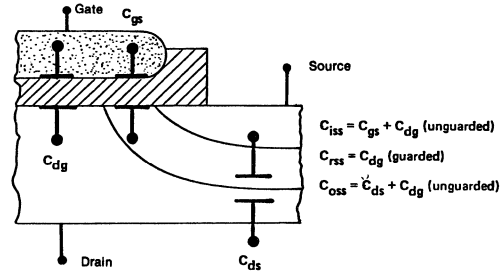


Figure 14. VMOS Transistor Capacitance

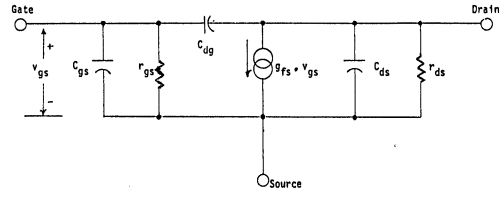


Figure 15. FET Equivalent Circuit—Small Signal

Low-Threshold MOSFETs: Structure, Performance and Applications

Since an increasing amount of attention is being focused on system interface from low-level logic, the need for higher current and/or low on-resistance at drive levels of only 3-5 volts has become a major concern. Supertex has always known of the importance of the gate drive consideration and has been offering N-channel low-threshold devices with threshold voltages of 2.4 and 1.6 volts for many years. Additionally, standard and low-threshold versions of P-channel DMOS devices are available. To understand the reasons that low-threshold processing requires very specialized techniques, one needs to understand the DMOS structure.

DMOS Structure

Most double-diffused MOS (DMOS) structures have very similar cross-section characteristics, as shown in Figure 1. For conduction to occur, a channel of electrons is needed between the gate and the source. This potential produces an inversion layer called the channel. The depth of this layer is the limiting factor in allowing current flow between the drain and source terminal. The greater the voltage applied, the deeper the induced channel; resulting in more current flow. The voltage needed to invert the channel region is called the threshold voltage $V_{GS(th)}$. However, when examining most manufacturers data books, one finds $V_{GS(th)}$ defined as the voltage needed to produce a specified drain current (I_D). This differs from the theoretical definition of knowing when a channel is produced, which is of little interest to power MOSFET users. Comparing $V_{GS(th)}$ at the same I_D simplifies the analysis of databook parameteric guarantees, allowing the designer to compare the product to actual needs.

The control of the threshold voltage is dependent on many factors, such as dopant concentration, gate-to-silicon work function and surface change. The greater the body dopant concentration, the larger the applied voltage needed to produce a channel, which translates to a higher threshold voltage. One method of reducing threshold voltage is to reduce the body dopant concentration until the required $V_{GS(th)}$ is met. This technique by itself is dangerous because it degrades other device parameters. The first and most important of these is drain-source breakdown (B_{VDSS}), which is a result of certain conditions, most commonly punch-through. Punch-through is defined as the drain voltage needed to create an electric field connecting the drain and source, as shown in Figure 2, at voltages less than the actual B_{VDSS} rating.

The susceptibility to punch-through increases dramatically as the body dopant concentration is lowered. There is an optimum body dopant level that is needed in order to stay away from the punch-through mechanism, but this concentration is too high for low thresholds. This is one of the reasons why P-channel devices typically have higher thresholds, because the optimum body dosage is higher than N-channel FETs.

Another technique, used by some manufacturers, is to lower threshold by reducing the gate oxide thickness. Again, there are tradeoffs using this method: (1) The input capacitance increases which will effect the switching speed efficiency and (2) the maximum gate voltage rating is decreased, making it more susceptible to input voltage spikes.

Supertex has developed a proprietary technique to successfully lower threshold voltage without these major tradeoffs. This method mainly depends on modifying the diffusion profile and altering the charge distribution to produce low-threshold N- and P-channel devices. This process, which makes use of Supertex's interdigitated design structure, allows typical thresholds of 1.1

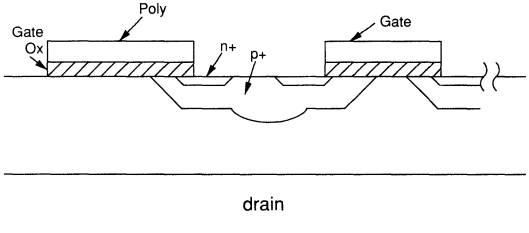


Figure 1. Double Diffused MOS (DMOS)

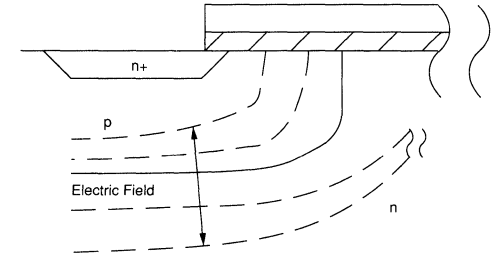


Figure 2. Electric Field Connecting Drain and Source

Part Number	IRF 520			VN1210N5			
Parameter	**Min**	**Max**	**Conditions**	**Min**	**Max**	**Conditions**	**Unit**
$V_{GS(th)}$ Gate Threshold Voltage	2.0	4.0	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	0.8	2.4	$V_{DS} = V_{GS}$, $I_D = 10mA$	V
$ID_{(ON)}$ On-State Drain Current	8.0		$V_{DS} > I_{D(ON)} \times R_{DS(ON)}$ max $V_{GS} = 10V$	20.0		$V_{DS} = 25V$ $V_{GS} = 10V$	A
				5.0		$V_{DS} = 25V$ $V_{GS} = 5V$	A
$R_{DS(ON)}$ State Drain-to-Source On Resistance		0.3	$V_{GS} = 10V$ $I_D = 4.0A$		0.3	$V_{GS} = 10V$ $I_D = 10.0A$	Ω
					0.45	$V_{GS} = 5V$ $I_D = 2.0A$	Ω

Table 1. Comparison between power MOSFET and standard threshold Supertex device

volts for N-channel and 1.8 volts for P-channel, DMOS devices.

An added benefit of Supertex's design is the lower input capacitance achieved by the interdigitated geometry, rather than the more conventional closed cell approach. "The Ideal Interface," an article published in Supertex's DMOS applications booklet, discusses these geometric considerations. As stated in the article, less charge is needed to control the device input. Therefore, it can be concluded that a lower threshold device will start conducting earlier for a given gate drive and allow control of larger drain current than a higher threshold device.

The availability of such low-threshold DMOS devices insures the performance needed to be driven by low level logic systems, in which the maximum voltage available is only 3-5 volts.

Performance Advantages

With the first device shipped in 1982, Supertex was the pioneer in low-threshold DMOSFET technology and still maintains a performance edge over other manufacturers. Supertex currently supplies the lowest threshold power MOSFETS in the industry. A threshold voltage of 1.6 volts for N-channel and 2.4 volts maximum for P-channel clearly supports this claim.

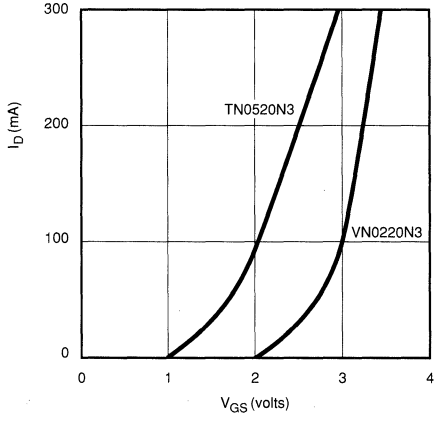


Figure 3. Typical Transfer Characteristics

Supertex measures threshold voltages at I_D = 1mA, 2.5mA, and 10mA for small, medium and large-sized devices, respectively. Although some manufacturers use test conditions as low as I_D = 250μA for large devices, Supertex devices, in comparison, still have lower values of threshold voltages at higher values of I_D. See Table 1 for a comparison between a popular power MOSFET and a standard-threshold Supertex device.

A true comparison can be made by normalizing the value of the I_D test condition. The threshold voltage for VN1210N5 will be lower than 2.4 volts, maximum, when it is tested at I_D = 250μA. Supertex's test conditions therefore portray a realistic picture of the device's capabilities at low V_{GS} conditions.

The threshold voltage is an important indicator of performance at low V_{GS} conditions because a device that starts conducting at a very low bias will exhibit good characteristics under such conditions. In fact, $R_{DS(ON)}$, maximum, and $I_{D(ON)}$, minimum, at low V_{GS} conditions are much more important than just the threshold voltage value because quiescent gate voltage conditions are usually at least a few volts above the $V_{GS(th)}$ value. Figure 3 shows the transfer characteristics of a standard-threshold and a low-threshold device. For example, if the drain current requirement is 100mA, TN0520N3 will typically need V_{GS} = 1.8 volts and VN0220N3 will require 2.8 volts to achieve this value. In case a 2.8 volts drive is not available, as in many applications, a VN0220N3 will be incapable of functioning in the circuit. In spite of the TN05 die being half the size of a VN02, the TN0520N3 performance is far superior at low gate to source voltages.

When confronted by low gate drive voltage, a designer basically has two choices:

Approach 1: Use a large industry-standard-threshold device to obtain the required low $R_{DS(ON)}$, maximum, and $I_{D(ON)}$, minimum, values. $I_{D(ON)}$ can be obtained from the transfer characteristics and $R_{DS(ON)}$ values will be read off the typical saturation or output characteristics.

Approach 2: Compared to the device used in Approach 1, use a relatively small (die size), low-threshold device to achieve the desired $I_{D(ON)}$ and $R_{DS(ON)}$ at the given minimum gate-to-source voltage.

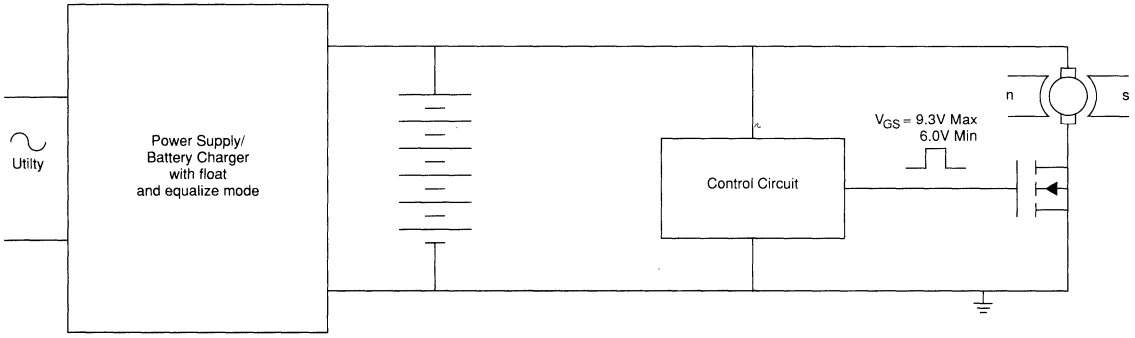


Figure 4. Motor of a Fluid Injection Pump

Comparison of Approach 1 and 2

1. Large die always have larger parasitic capacitance and consequently slower switching speeds. This could pose a restriction in many applications, where limited gate drive charging current is available.
2. Large die must be accommodated in large packages, and this may result in unnecessary waste of board space. For example, the total volume occupied by a TO-220 package including stand off could be 8 to 10 times more than a TO-92 package.
3. A judicious choice using smaller die in a smaller package can result in considerable cost savings. With more silicon and several times the raw material content for packaging, a low-threshold TO-92 will definitely be a much more cost-effective alternative.

Supertex publishes $R_{DS(ON)}$, maximum, and $I_{D(ON)}$ minimum, specifications at V_{GS} = 5 volts (see Table 1). This data is very useful to a designer because it is always desirable to rely on guaranteed values instead of typical curves. Typical curves are based on a high statistical probability of the majority of devices closely meeting values on the curves. They do not 100% guarantee performance of all devices. Manufacturing tolerances and some variations from one fabrication lot to another are likely to cause lower than expected values of these parameters. Depending entirely on curves tends to be risky for production runs even if prototypes built earlier perform satisfactorily.

The combined effect of low-threshold voltage and low-input capacitance is ease of drive, which is a key consideration in most circuits employing power MOSFETs. What better trait can a designer expect than a small amount of charge controlling high voltages and large currents? These low-threshold FETs from Supertex are ideally suited to interface low-voltage logic to the outside world.

Applications

Low-threshold power MOSFETs play a key role in circuit design whenever there is a low gate-to-source voltage situation. Conventional devices are often very inefficient and sometimes unusable in some applications as follows:

- Handheld, battery-operated equipment requiring satisfactory operation at low/end-of-discharge voltages. This is necessary for complete utilization of battery energy. Inadequate turn-on of a FET can cause two problems: A) loss of control signal or data; or B) loss of power due to resistive losses. Supertex TN/TP series devices are being used for a variety of data acquisition and remote-control applications.
- Medical equipment with battery back up is another popular application. Figure 4 shows the motor of a fluid injection pump powered by the utility supply and backed by a NiCad battery. The V_{GS} = 6 volts condition demands carefully attention, because the $R_{DS(ON)}$ has to be low in order to ensure a low drain to source voltage drop. A large voltage drop can A) affect motor performance, and B) cause high I^2R losses, reducing system efficiency and battery back-up time.

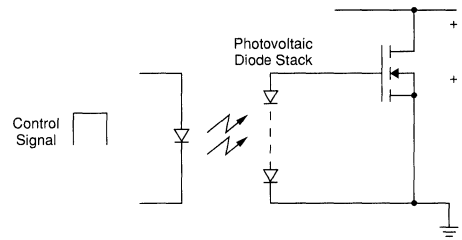


Figure 5. Photovoltaic Drive Scheme

- Solid-state relays utilize optically-isolated drive schemes for isolation purposes. Figure 5 shows a commonly-used photovoltaic drive scheme. Usually a low voltage is available to turn on the FET to meet the relay's assured $R_{DS(ON)}$ specifications. Precautions are taken to avoid excessive drive since the charge applied during turn-on must be quickly discharged during turn-off. Turn-off circuitry is not shown in this simplified schematic.
- Figure 6 shows a simple charge pump converting 5vdc to 12vdc. The key parameter for efficient functioning of this circuit is $R_{DS(ON)}$ at V_{GS} = 5 volts.

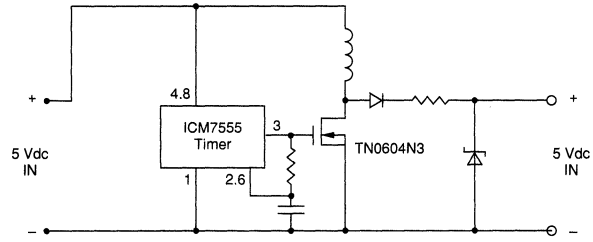


Figure 6. Charge Pump Converting 5vdc to 12vdc

- Telephone handsets encounter wide variations of voltage during normal operation (Figure 7). While the DC voltage appearing across the unit may vary from approximately 3 to 25 volts when the phone is off the hook, high voltage AC ringer signals and associated transients have to be handled safely. Moreover, atmospheric disturbances (e.g., lightening and RF radiations) are picked up by the lines, inducing high voltages which are suppressed by MOVs, gas discharge tubes, etc. (not shown in the figure).

Supertex low-threshold TN05 devices used for the pulser and mute switch operate satisfactorily, even at voltages as low as 3 volts. A TN0524N3's guaranteed $I_{D(ON)}$ minimum = 100mA at V_{GS} = 3 volts is more than adequate for this purpose.

Advances in low-threshold power MOSFET technology offers several useful choices to a designer. Circuit design for many applications are simplified and use of components minimized. Consequently, system complexity is reduced and reliability enhanced. All these benefits combined with the cost-effectiveness of the devices makes the low-threshold FETs an excellent choice.

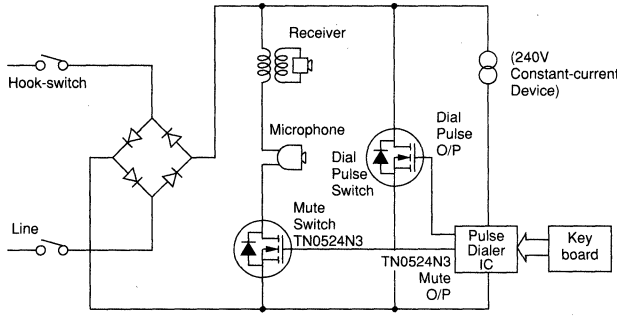


Figure 7. MOSFETs in a Telephone Handset

Basics of EL Panel Drive Techniques

Thin film electroluminescent (EL) panels operate on a principle of successive pulses of opposite polarity. These pulses must exceed a threshold of approximately 200V for the panel to emit light.

A flat panel display is a sandwich of phosphor material with dielectric coating on either side; transparent ITO (indium Tin Oxide) row electrodes on one side and column electrodes on the opposite side. These layers are built up on a sheet of glass to form a very thin, lightweight display panel.

Since the drive electrodes are dielectrically isolated from the phosphor material, and each other, the display panel exhibits a capacitive load to the drive electronics. On larger panels this capacitance can be quite high. Surge currents can be large, therefore coupling from the row to the column electrodes should be considered.

The drive electronics used to operate the panel are organized in a manner to surround the display panel with contacts as shown in Figure 1.

Generally, the row electrode electronics supply the major portion of the threshold voltage, called the scan pulse, and the opposite polarity "refresh" pulse , which is necessary for the panel to emit light. The refresh pulse is usually applied to all rows at one time while the scan pulse is applied to one row at a time (starting with row #1), similar to a television raster scan.

Depending on the data to be displayed in each column, the column electrode electronics supply a voltage of opposite polarity to the row scan pulse. This combination of row and column voltage across the phosphor will exceed the threshold and cause the phosphor in areas between the energized row electrodes and the energized column electrodes to glow. This sequence, applied to successive rows, causes certain portions of the display to be illuminated.

Because the phosphor requires successive pulses of opposite polarity to operate, an opposite polarity refresh pulse is applied to all row electrodes simultaneously while the column drivers are kept at ground. The sequence then begins again at row #1 with the next frame of data. Figure 2 is a representative timing diagram of the signals applied to a TFEL panel showing the first four rows and the first column.

Due to the fact that the phosphor illumination threshold has a slope of illumination versus applied voltage within a short range, the column drive electronics can be made to vary the applied voltage within this range, dictated by the intensity of light desired for a particular element on the display. By this means, a grey shade image can be created using the EL display.

Row Drivers (HV02, HV03, HV05)

To allow the open drain outputs to provide the opposite polarity pulses to the panel, the sources of the output MOSFETs must be switched between the different voltages required for the panel.

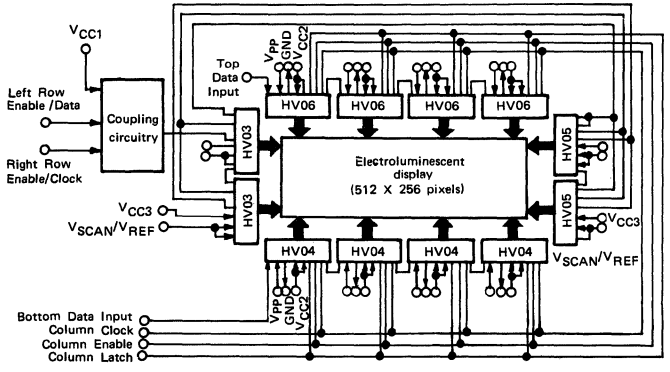


Figure 1. Block diagram of the driver system for a TFEL (Thin Film Electroluminescent) panel. Note that the column drivers have two data lines with interleaved pixel data.

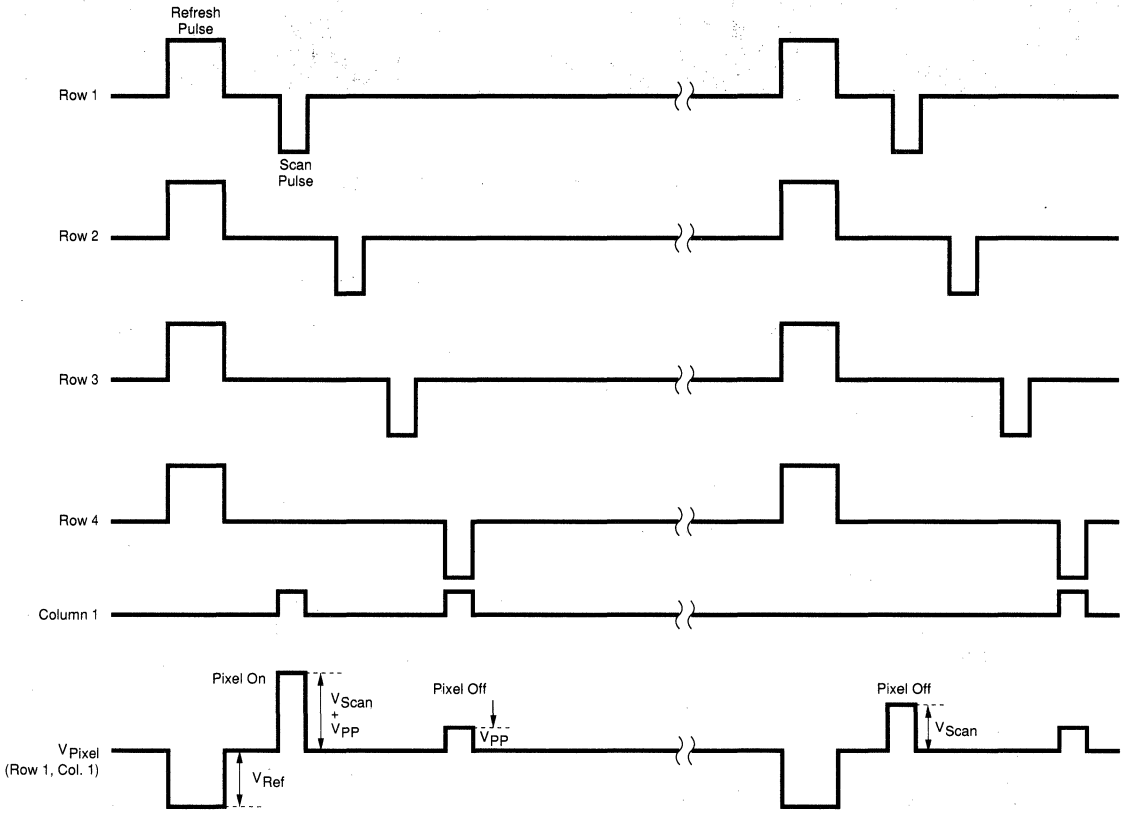


Figure 2. Simplified diagram illustrating row and column timing to operate an EL Panel. V_{REF} only lights pixels that were turned on by V_{SCAN} and V_{PP} pulses in the previous frame of information.

Since these MOSFET source connections are connected to chip ground, the entire device needs to be isolated or "floated" from the system ground. The control signals to the row driver chips therefore must be opto-isolated from the system ground. Figure 3 shows a simplified way to accomplish this.

The two high voltage supplies are switched to the row substrate (driver chip ground) using MOSFET switches. Application of the voltages to the panel is as follows: the refresh pulse is applied to the entire panel at the same time by pulsing on "C," forward biasing the body-drain diodes on all row outputs. The panel is returned to ground by pulsing "D" while having all the row driver outputs on. The scan pulse is applied, one row at a time, by pulsing on "A" while the selected row output is on. The selected row is returned to ground by turning on "B." The next row to be scanned is then selected, and the scan is repeated; first "A," then "B." When the entire panel has been scanned, the refresh sequence is executed; first "C," then "D." The scan cycle then begins again. In this way the proper voltages and sequences are applied to the panel for operation.

Monolevel Column Driver (HV04, HV06)

The column drivers are used to apply the data to be displayed onto the panel. The data for each row of picture elements (pixels) is loaded into all the column drivers serially and latched into the output latches. The outputs are thus turned to their desired state, and then the high voltage (V_{PP}) is applied. Columns selected for data display are connected to V_{PP} through the CMOS output and are pulled up to V_{PP}. The combination of the column V_{PP} and the selected row voltage will cause selected pixels to light in that particular row.

During the time that the data for one row is being displayed, the data for the next row is being loaded into the shift registers, awaiting the display of the next row. When a row is completed, the column driver V_{PP} is brought low and the data waiting in the shift register is loaded into the output latches. The cycle then begins again for each successive row.

The column drivers are designed with a serial shift register output for use in cascading the column drivers together. This allows the data for one row to be loaded serially, using one serial input at the first column driver device.

Grey Scale Column Driver (HV01)

This device is designed to take four data inputs in parallel into four shift registers. The data is then taken from equivalent stages of each shift register and converted to an analog level, 1 of 16 between ground and V_{PP}. this is done by a digital counter using four bits of input data. The counter is preset with data counting down to turn off a transistor. This transistor isolates a ramp input (VR) from an internal storage capacitor, which controls a CMOS output stage. The output voltage therefore represents the value of the ramp voltage (VR) at the time the counter for each output counted down. This voltage, applied to the column of the panel, combines with the row scan voltage to vary the light output from each pixel in the selected row.

Panel Brightness

The varying brightness of an EL panel by voltage variation can only achieve a limited range. Dramatically increased panel output, such as required by panels to be operated in direct sunlight, requires another method of increasing output. This is done by increasing the panel frame rate, or refresh rate. Normal CRT based systems work on a 60Hz frame rate. Most applications of EL panels replacing CRTs, then, also operate at this rate. This is fine for office and home use but does not provide enough brightness to accommodate most military applications. By increasing the refresh rate up to tenfold, a dramatic increase in brightness can be achieved.

This increase in refresh rate requires some changes in the column driver configuration. Instead of cascading all the column drivers together, each column driver shift register input is driven in parallel by the controlling system at the same time. This increases the number of data lines required but allows the data to be loaded much faster, enabling the faster frame rates desired. The row drivers are used at a much slower rate, so no changes are required to achieve faster operation.

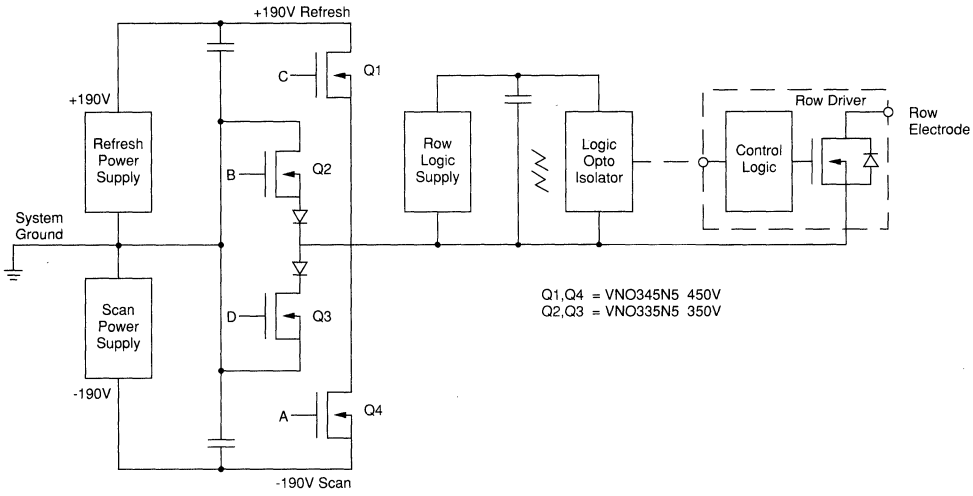


Figure 3. Row driver panel switching block diagram.

Cascading Encoder-Decoder

The Supertex family of Encoder-Decoder devices allows address matching of up to 32,768 different codes. Four bits of data can be sent to up to 2048 different receive devices. This has been adequate for the vast majority of applications. Some applications, however, require even more addressing capability than the largest part can offer.

A cable TV control system, with which a cable company would want to control operation of all the decoders in their area, is one application in which the possible remote addresses could number more than 32,768. Another possible use is remote meter reading of domestic and industrial power meters by the local utility company. This offers tremendous savings in labor costs over manual meter reading. Both of these applications require a low cost, simple means of implementing single unit identity coding of a large number of remote devices. The Supertex ED devices offer this capability.

Mode of Operation

Figure 1 shows a simple means of cascading two ED devices to allow more than 1.07×10^9 addresses. The basic requirement for using this design is that the transmission into the receiver consists of two ED-style data packets (preamble and data) separated by a short interval. The first data packet will go to the primary ED device (ED #1) and the second data packet will go to the secondary ED device (ED #2). These groups of two data packets must be separated by a much longer delay. Figure 2 is a timing diagram of the operation of this cascaded receiver.

On initial condition, in which the receiver is waiting for an address group to arrive, one-shot IC #1 enables the incoming signal into the Start/Data Input (SDI) of ED #1 while disabling the path to ED #2. When the group arrives, the first data packet is input into ED #1. When this data packet, both preamble and data, have been

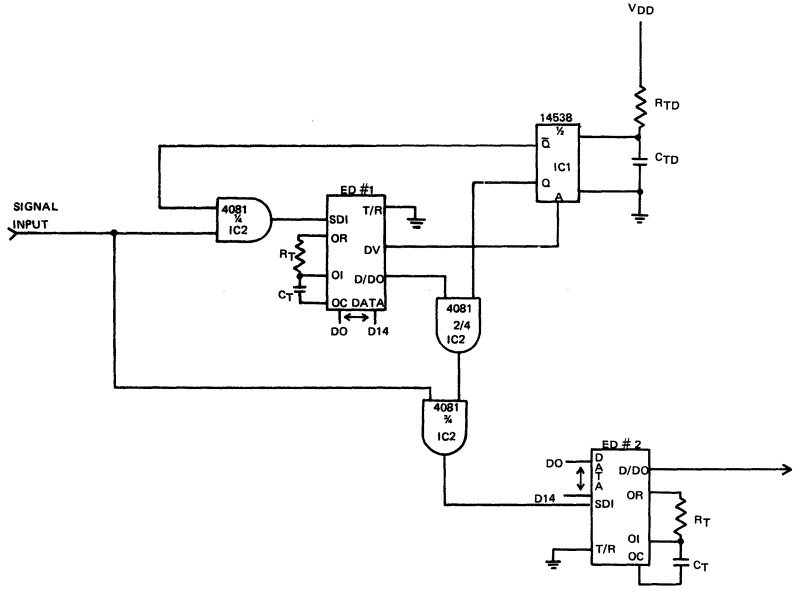


Figure 1.

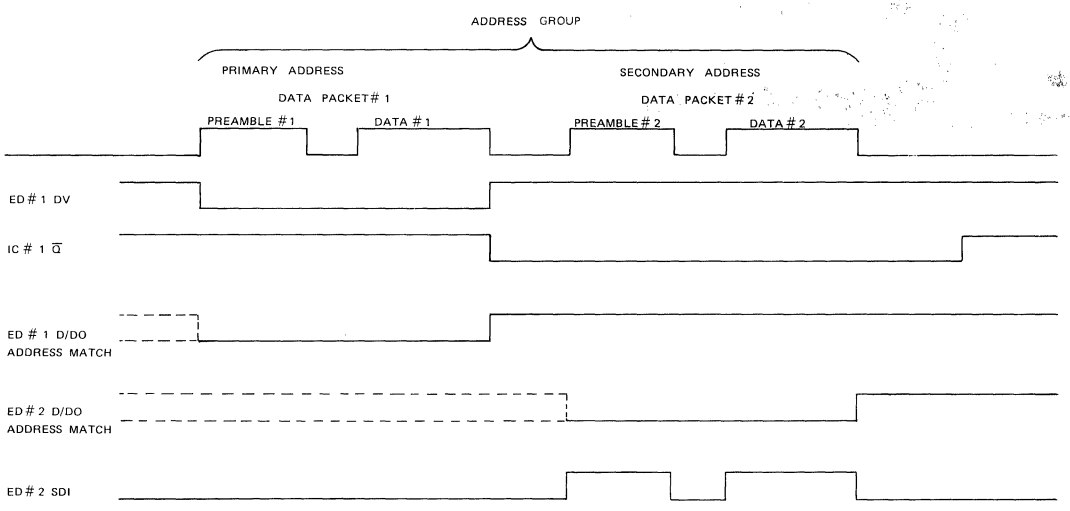


Figure 2.

received by ED #1, the Data Valid (DV) signal will go high, triggering the one-shot. This will disable the SDI input to ED #1. If the data in data packet 1 matched the address data on the ED #1 data pins, then ED #1 Decode/Data Output (DDO) pin will also go high. This and the triggered one-shot enables the path from the signal input to the SDI pin of ED #2. The second data packet will then be received by ED #2 and compared to the data input pins. If the address matches, the ED #2 DDO will go high.

The one-shot timing must be set to allow data packet 2 to be completely received before the one-shot times out and returns to the off condition. This time period will vary depending on the transmission speed of the communication link and the ED speed used. After both data packets have been received and the one-shot has timed out on all the receivers in the system, the transmitter can then send out a new address group.

Address Decode

The circuit shown in Figure 1 and described in the previous section implements the address decode function. The DDO pin on ED #2 should be connected to a device that operates on a positive going edge to signal the correct addressing of both ED #1 and ED #2.

Different combinations of ED devices can give a different number of possible addresses. The following table illustrates these possibilities:

ED #1	ED #2	# of possible addresses
ED-15	ED-15	1,073,741,824
ED-15	ED-9	16,777,220
ED-15	ED-5	1,048,576

The ED-9 cannot be used in the ED #1 position because it does not have a DV output available.

Address and Data

Often it is necessary not only to address a particular device within a large number of devices in a system, but also to send some amount of data only to that device. The ED-11 and DC-7 devices easily implement this capability in the cascaded design. Figure 3 illustrates a data transmission variation of the cascade circuit.

The input controls for ED #1 and #2 operate the same as for the address matching case. In this case, however, the Serial Data Output (SDO) and Data Clock (DC) of ED #2 are connected to a 4094 serial to parallel shift register. The SDO is connected to the Data In pin, while the DC is connected to the Clock pin to clock the data into the shift register. The rising edge of the ED #2 DDO signal is converted to a pulse and used to transfer the data from the shift register to the parallel output latches of the 4094 if the address match is detected. The DDO pulse is also available from the receiver system as an interrupt to the external circuitry signalling the arrival of data from the transmitter.

ED #1	ED #2	Data Bits	Address Combinations
ED-15	ED-11	4	67,108,864
ED-15	DC-7	8	4,194,304
ED-15	ED-5	15	32,768 *special case
ED-5	ED-11	4	65,536
ED-5	DC-7	8	4,098
ED-5	ED-5	15	32 *special case

* The special cases noted above represent a situation in which 15 data bits must be received. This is implemented by using ED #1 only for address matching and using ED #2 only for data reception. To receive 15 bits, two 4094s must be serially connected to form a 16 bit shift register. The Data Valid (DV) output of ED #2 would be connected in place of the DDO output to strobe the data into the latches of the 4094s.

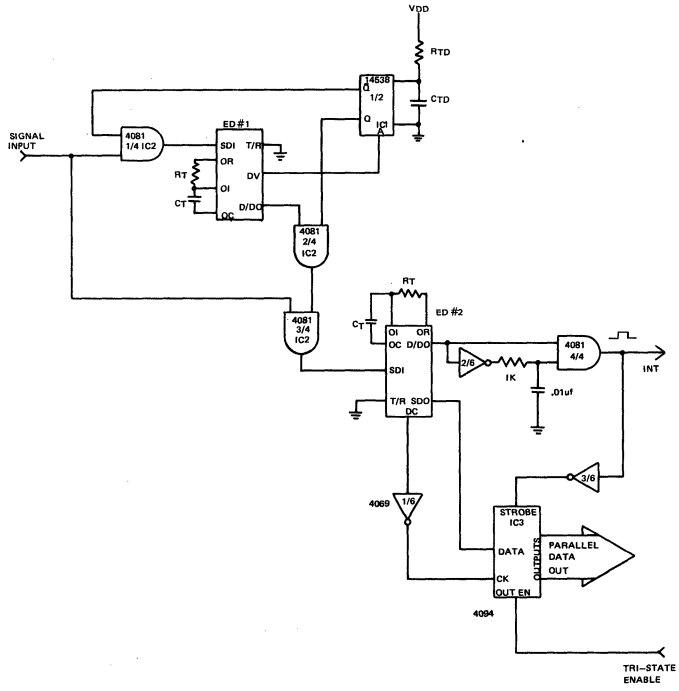


Figure 3.

Transmitter

The transmitter used to address this receiver design would normally be microprocessor controlled, with a peripheral adapter port connected to the data pins of an ED-15 device. The data pins could be changed to implement the data packet #1 and #2 by the much faster microprocessor. Alternatively, two ED-15s could be OR-gated to a transmission media and controlled by normal logic.

Conclusion

This application should help implement a simple low cost means to address a large number of remote devices in an addressing system. If there are any questions or suggestions for improvement, please contact the applications engineering department at Supertex.

DC-7, ED-5, ED-9, ED-11 Applications

The Supertex "ED Family" of remote control encoder/decoder chips has almost unlimited uses. To make the user aware of some of the salient features of these unique ICs, we have put together this application note. When used in conjunction with the data sheet for these parts, most of the questions that may arise from attempts to design systems around them may be answered.

Remote Control Systems

As electronic systems become increasingly more sophisticated, the need to perform certain functions at a distance becomes increasingly important. In many cases, the need arises for central automatic control of remote operations. Here, too, remote control devices are necessary. Until recently, remote control of various functions required a plethora of discrete circuits, raising the cost, in many cases, to prohibitive levels. Recently the MOS LSI industry has responded with integrated circuits of varying usefulness and complexity. Most of these ICs are geared to perform a single task such as opening garage doors, controlling TV functions, and the like. Until now, all remote control ICs were sold in a set; i.e., a separate encoder and decoder. The Supertex EDs on the other hand are a single chip. The encode/ decode function is determined by a programming pin, which is tied to V_{DD} for the encode function and V_{SS} for the decode function. Having only one chip reduces the complexity of purchasing remote control. Spares are easier to stock, and reliability is enhanced.

The Supertex EDs

In addition to the "lock-and-key" feature of ED codability, the ED-11 has the feature of being able to transmit and receive 4 additional bits of binary data which are available at the decoder's output. The DC-7 has 8 bits of data. These can be used to perform tasks such as channel recognition (with digital readouts), microprocessor interface and event sequencing. This feature makes the ED family of encoders/decoders extremely versatile.

Simple, Two-Wire Interface Utilizing ED-15s

The basic application for the ED-15 is the simple two wire interface. This configuration is useful for optimizing ED parameters such as encoder/decoder frequency stability, and lockup time. It is also a useful way of observing waveforms and can be invaluable for troubleshooting a more complicated system using other transmission media.

In Figure 1, the output is not latched and will stay high only so long as the trigger circuit keeps cycling the encoder. The CMOS oscillator is necessary to produce the start pulse. By utilizing an oscillator, it is possible to get a continuous data stream. This is useful for observing all waveforms involved. The start pulse oscillator can even be used to trigger the scope, making the waveforms easy to sync. The wire used can be just a jumper when

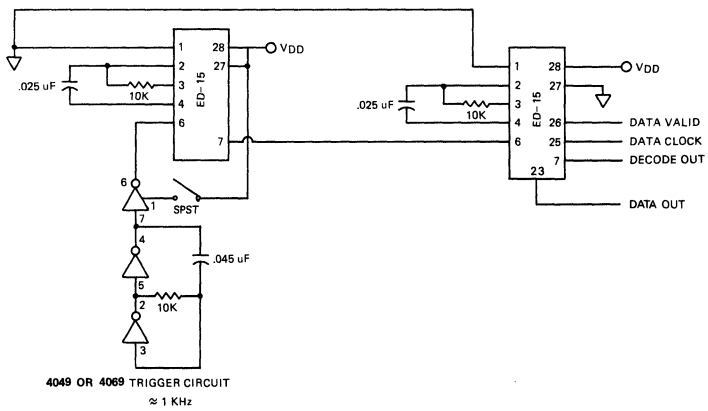


Figure 1. Basic Two-Wire ED System

both encoder and decoder are on the same breadboard, but twisted pair or shielded cable should be used for long runs.

ED-11, DC-7 System Utilizing Hardwire Transmission and Output Latches for Additional Data

As stated earlier, one of the great features of the ED family of encoder/decoders is the ability of the ED-11 and ED-5 to transmit 4 bits of binary code along with the "lock-and-key" recognition bits, the DC-7 to transmit 8 bits of binary code along with the "lock-and-key" recognition bits, and these 4 or 8 bits to appear at the data clock output of the receiver. This feature allows the transmission of useful data instead of just the "code valid" output common to other so-called remote control encoder/decoders. The following is an adaptation of the hard-wired system seen above. The difference is that even though an ED-15 is used for the encoder, an ED-11 is used for the receiver, and this data is decoded for use as a parallel latched data bus. Of course, since the last 4 bits in the ED-11 are used as actual transmitted non-dedicated data, it has only 2048 different possible code combinations instead of the 32,768 combinations possible with the ED-15 system. The trigger circuit is the same as above and will be represented from here on only as a block diagram.

In Figure 2, an ED-11 can be used for the transmitter as well as for the receiver. An ED-15 is shown to illustrate the compatibility of the ED family of encoder/decoders. The 4015 in the circuit is a serial to parallel converter and the 4042 is a quad 4-bit latch. The data valid pin is used to clock the parallel data into the latch and Q as well as $\overline{Q}$ outputs are available on this IC. The bit sequence chart is given below the schematic to show the relationship of the "key-code" bits to the last 4 data bits.

In Figure 3, a DC-7 can be used for the transmitters as well as for the receiver. An ED-15 is shown to illustrate the compatibility of the ED family of encoder/decoders. The 4094 in the circuit is a serial to parallel converter and an 8-bit latch. This circuit demonstrates the use of the DC-7 in which both the data and address can be transmitted from one location to another and both the data and address of the transmitter recovered. In an application in which only the data is to be recovered and a special address assigned to the receiver, the D/DO signal should be connected to the 4094 and only the TOP 4094 used. In a system in which all incoming data and addresses are to be decoded the DV signal would be connected to both 4094s as shown. The bit sequence chart is given below the schematic to show the relationship of the "key-code" bits to the last 8 data bits.

Infrared Transmission

Often it is necessary to transmit data over some distance without wires. In such an instance it is necessary to couple the data (in this case from ED-series encoder/decoders) by way of some transmission media. Here is a simple but effective way to use IR as a medium for signalling between two EDs.

The circuit in Figure 4 is designed so that the ED-15 is operating at 25KHz. The output of the chip (Pin 7) is applied to an NPN transistor gated with a 3.3KΩ base resistor to act as a switch. The data stream turns the 2N4401 hard on or off depending upon the coded state. This in turn switches on and off the Monsanto MV5000 series infrared LEDs. Three of the LEDs are used to make aiming at the receiver easier.

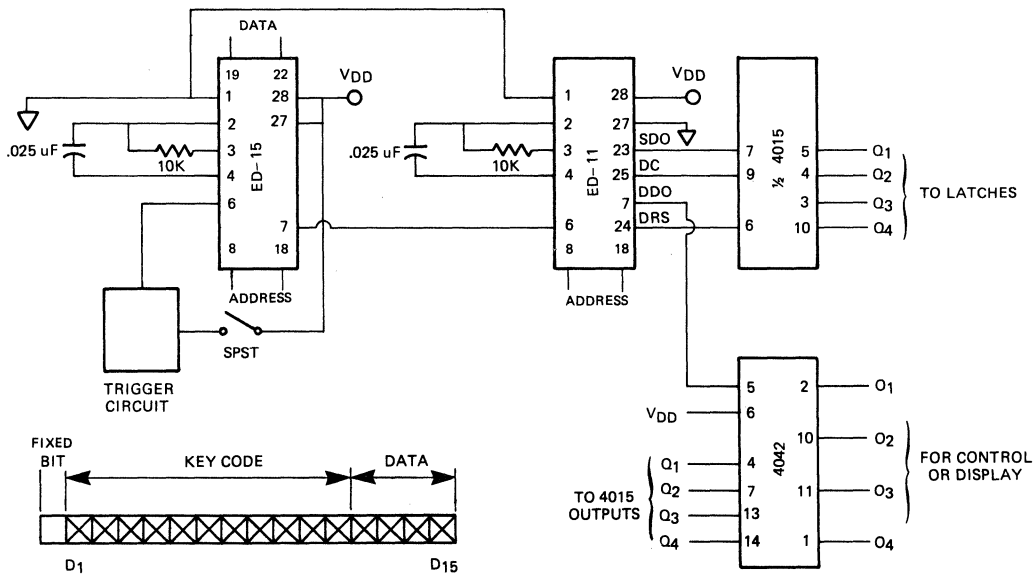


Figure 2. ED System with Latched Parallel Data Out

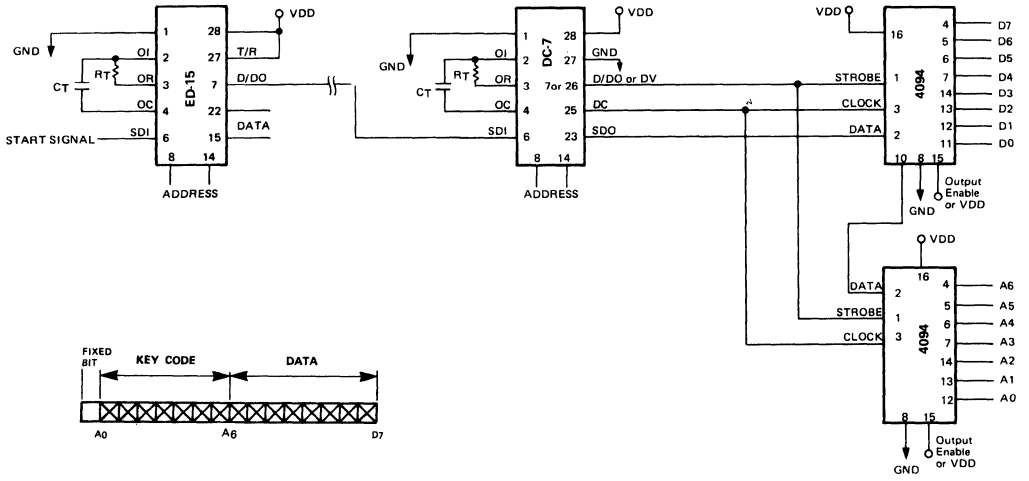


Figure 3. DC-7 System with Latched Parallel Data Out

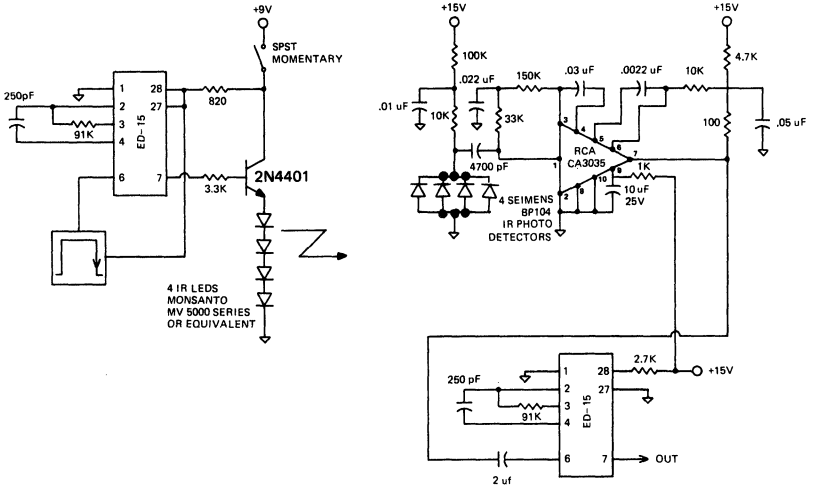


Figure 4. IR Remote Control Transmitter/Receiver

The receiver circuit consists of a three-stage amplifier (the CA 3035) with Siemens Bp104IR photo diodes arrayed for maximum coverage of the reception area. The output of the CA3035 is then applied to the ED-15 receiver chip and the signal is decoded in the normal way. The range of this set-up should be about 10 meters.

Even though in this application the ED-15 is shown, it will work equally well with any of the other ED ICs. This application can be combined with the application in Figure 2 to provide 4 bits of parallel data or Figure 3 to provide 8 bits of parallel data to operate displays, relays, etc.

Microprocessor Interface to ED-11, ED-5

It is possible to use the ED-11 and the ED-5 in conjunction with an 8-bit microprocessor to remotely control functions at a distance.

Because of the Supertex ED system's "single chip" approach to encode-decode remote control, it is possible to use these ICs in a "hand-shaking" arrangement, allowing for 2-way communication between 2 or more microprocessors with a 4-bit data word. To do this, an 8-bit µp is required, 4 bits are used as data, and the remaining bits control the EDs and and associated logic required to change the system from a data transmission system to a data receiving system.

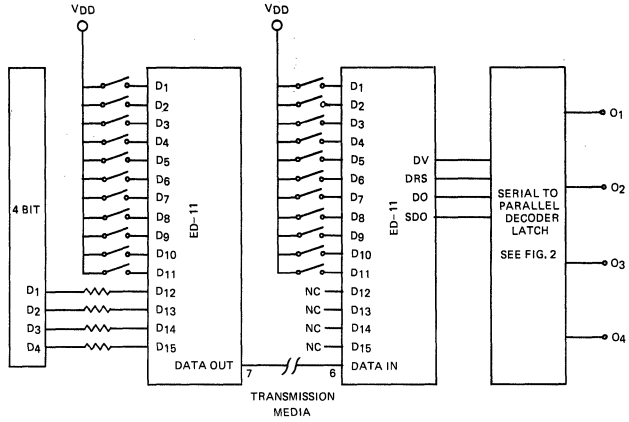


Figure 5. Block Diagram Showing Basic Configuration for Transmitting Microprocessor Data over Remote Control System Using ED-11s as Encode/Decode

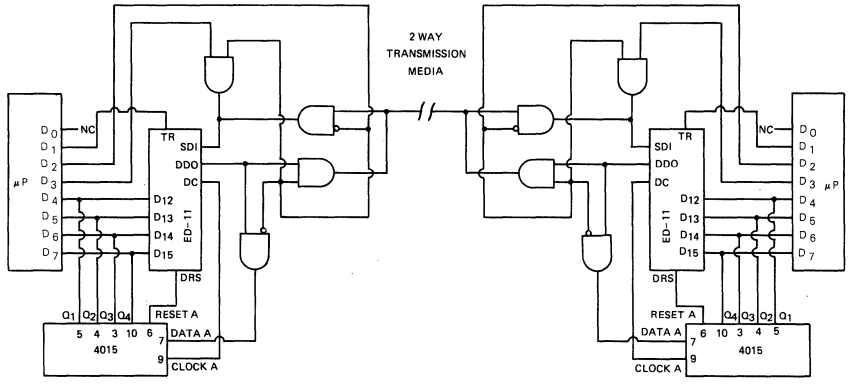


Figure 6. ED System Illustrating "Handshaking" Capabilities of Supertex ED-11s

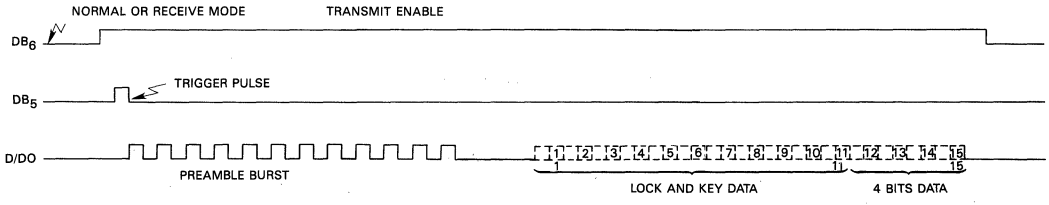


Figure 7. Possible Timing Diagram for Circuit Shown in Figure 5.

In Figure 6, an 8-bit microprocessor such as a 6502 or 6800 is used to enable the ED-11 or ED-5 to transmit data to another 8-bit microprocessor telling it to perform some function. When the transmitting μP is finished sending its message, it returns to the "receiver" mode. The interrogated μP then performs its function and switches itself to the "transmit" mode and sends confirmation back to the first μP.

In Figure 7, a "possible" timing diagram is shown for such an application. One can see that DB6 or transmit enable is actuated first. With all of the gates shown in Figure 6 now in the "transmit" mode, DB5 sends out a trigger pulse to the ED chip. This initiates a data transmission (shown as D/DO in the timing diagram). At the end of this data transmission DB6 drops back low, returning the ED and data systems to the "receive" mode. For RF transmission the DB6 signal can also be used (via a buffer) to drive a relay to key the RF transceiver to the transmit mode. The μP software for such an application would have to be developed by the user, and the circuit diagram shown here is only a suggestion. Microprocessor information used in this circuit is from the 6502 or 6800 literature and assumes its use.

ED "Carrier Current" One-Way Remote Control System

In the following application (Figure 8), the AC power lines running through a house or office building are used to transmit data from one ED to another. Such a system is an ideal way to interconnect multiple smoke alarms, turn on or off appliances from a central location, or monitor energy use in the home or plant.

This particular circuit (Figure 9) utilizes 160KHz as the transmission frequency. The reason that this frequency is used is that it has been shown that "around" 160KHz is the best compromise between noise and capacitive attenuation of typical building wiring. One of the major problems with "carrier current" communication devices is that house wiring is a very difficult transmission medium. Most building codes require that buildings be wired with a large two-conductor solid wire called "ROMEX." Since both conductors are jacketed together, the capacitance between them is quite high and the attenuation of high frequencies is considerable. To compound this problem many building codes require that the wiring be conduited. This will be found mostly in commercial

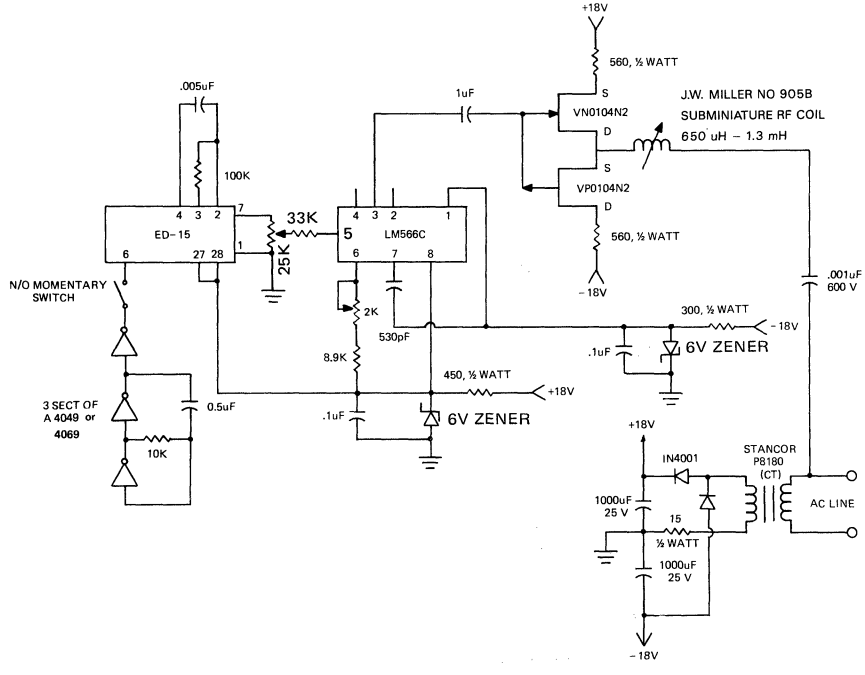


Figure 8. Carrier Current Transmitter

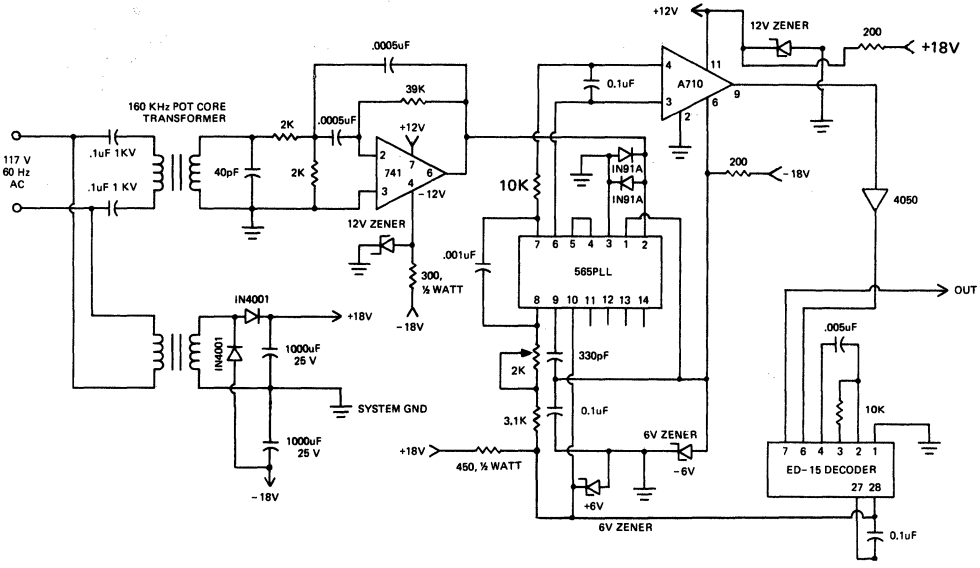


Figure 9. Carrier Current Receiver. 160KHz transformer consists of a 18 x 11mm ungapped pot core (Siemens, ferrocube, etc.) utilizing magnetics incorporated type "F" material wound with 80-1/2 turns of No. 35 wire for the secondary and 4-1/2 turns for the primary. This gives a turns ratio of approximately 15 to 1.

and multiple-dwelling buildings, but since the conduit is ground, the capacitance is even greater. Another problem with building wiring as a communication medium is the fact that many appliances hooked to the wiring are large inductive loads (motors, power transformers, etc.). When these inductors are in parallel with the ROMEX, very effective high frequency filters are formed.

External Oscillator for ED-15, ED-11, ED-5, DC-7

Often it is desired to drive the ED-series devices with an external clock. Due to external considerations it is not recommended in the general case.

However, the ED-15, ED-11, ED-5 and DC-7 device types may be externally driven in the transmission mode if certain precautions are taken. Using the circuit in Figure 10 will allow driving of the transmitter chip. The external oscillator MUST be gated on only during the transmission time after the START pulse. During all other times the O/I pin MUST be held high. The DRS signal in the transmit mode is a convenient signal to use as a gate for this purpose. A 1KΩ resistor in series will minimize possible current spikes inside the device. The gates shown in Figure 10 should be CMOS logic and share the same V_{DD} used on the ED device.

The synchronizing characteristics of the ED series in the receive mode do not allow an external oscillator to be used. The use of the data sheet curves will allow calculation of the resistor and capacitor network to use on the receiver to match frequencies with the external clock of the transmitter.

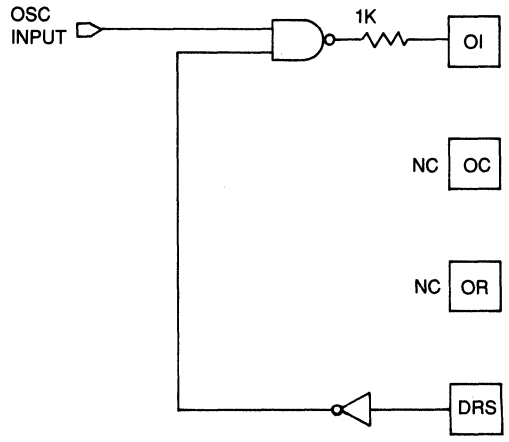


Figure 10. External Oscillator Gate for ED-15, ED-11, ED-15, DC-7A Transmission mode only.

Encoder-Decoders for Power Line Carrier Remote Control

Power Line Carrier Communication is starting to emerge as a viable, cost effective means for control and information exchange in both consumer and industrial applications.

Energy Management Systems for heating, air conditioning and lighting control are obvious examples of the use of the power line as a communication link. A system is shown in Figure 1 using Supertex Encoders and Decoders for transmitting and receiving control information over the power line. The prototype system was designed to allow remote On/Off and brightness control for a fluorescent lighting fixture using a dimming ballast. The design was simple and implemented in about a week's time.

System Description

The system uses an ED Encoder-Decoder chip set to generate the Power Line control messages and to decode the messages for appropriate action. The system transmitter is able to selectivity address 32 different receivers and transmit 16 different control commands to the receivers that are connected to the AC power line.

The control message is coupled to the AC power line by a Signetics NE5050 Power Line Modem. The modem takes a serial bit stream, generated by the ED-9, and turns it into a series of 125KHz bursts. Each burst represents a digital "1" in the serial bit stream. This series of 125KHz bursts is transmitted over the AC power line to any receiver that is coupled to the AC line.

The series of 125KHz bursts are received by a second Power Line Modem and translated back into the original serial bit stream generated by the ED-9. This serial bit stream message contains address and control information. The message is decoded by an ED-5 to determine address match and control command. If the address does not match, then the rest of the message is ignored.

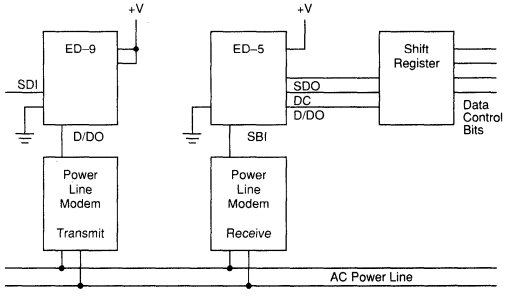


Figure 1. System Diagram

When there is an address match at the receiver, the ED-5 will serially transmit the data information into the serial to parallel shift register. The data can then be decoded to determine which of the 16 control commands was transmitted.

Transmitter (Figure 2)

The ED-9 performs address matching only. In this application, the 9 bits that are available for addressing are split into 5 bits of address (D4,D5,D6,D7,D9) and 4 bits of control data (D12-D15). The 5 bits of address are set with dip switches, and the 4 data bits can be set with dip switches or a rotary selector switch.

The transmission of a message is initiated by a pulse on the Start/Data input (SDI). The message baud rate, f_c, is determined by the RC combination of 10K ohms and .039uf at the OI, OR, and OC pins of the ED-9.

$f_c = 0.375/RC = .961KHz$
$T_c = 1/f_c = 1.04ms$
Data Bit Width $= 2T_c = 2.08ms$
Data Clock Width $= 0.5T_c = .52ms$

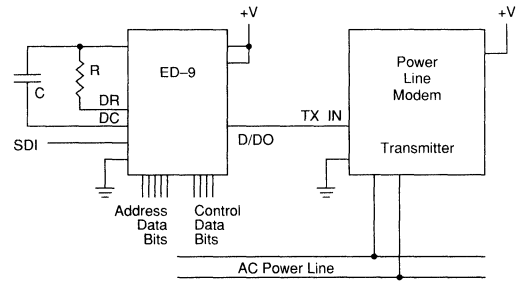


Figure 2. Transmit Circuit

Message Format (Figure 3)

The message (shown in Figure 3) consists of a preamble burst and a data transmission. The preamble burst is used to synchronize the receiver with the transmitter.

The data transmission consists of 15 bits of information. In this application only 5 bits are used for address information and 4 bits for control information. The data transmission is Manchester encoded. Manchester coding uses the transition from low to high to represent a binary "1" and a transition from high to low to represent a binary "0". With this technique, the first half of each data bit time is always the logical inverse of the second half. This

provides for a level transition during each data-bit time, and allows a synchronized receiver to easily read the correct data, even when large noise spikes are present.

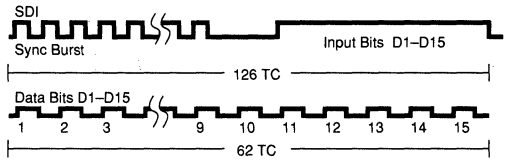


Figure 3. Message Format

Receiver (Figure 4)

The receiver uses an ED-5 in the receive mode by first checking the address of the incoming message against the preset 5-bit address in the receiver unit. If the address in the message matches the receiver address, then the 4-bit control data is serially shifted into the serial-to-parallel shift register. This 4-bit word is now available for further decoding and control.

The message enters the device on the Start/Data Input (SDI) pin. the ED-5 then matches the message address information with the address of the receiver, and if the bits match, the Decode/Data Out (D/DO) pin goes high until the next stream of serial data arrives at the SDI pin. D/DO going high pulses the strobe input to the CD4094. This action resets the shift register, and the DC output from the ED-5 clocks the entire message into the shift register. The last four bits of the message (D12-D15) contain the control information (refer to Figure 5). The control information will be at the outputs of the shift register (Q1-Q4) at the completion of the receive sequence.

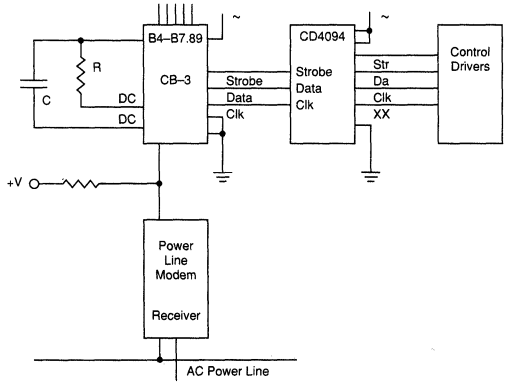


Figure 4. Receive Circuit

Power Line Interface

The Power Line Modem was calibrated to transmit a 125KHz burst at a signal level of 7.5 volts p-p into a 50 ohm load. Impedances of residential wiring may be over 50 ohms while industrial impedances may be less than 1 ohm, with the receiver sensitivity set at 15 millivolts.

The AC Power Line

The constraints imposed by the power line interface dictate the overall system operation. The power lines are a hostile environment for signals. The noise on the power line can be put into two categories: broad band and impulse. The broad band noise levels vary from a few to hundreds of millivolts. Impulse noise levels can range from millivolts to tens of volts. Examples of noise sources are light dimmers, universal motors, hair dryers, induction motors, radio and television receivers, and fluorescent lights. In general, noise levels in a factory environment will be much greater than in a residential environment.

The system described in this application note can, depending on the noise level, be affected by impulse noise on the power line. The communication link between the transmitter and receiver is an open loop one way command link. An impulse could cause false command decode if the impulse happened at the time when the receiver was decoding the control data section of the data transmission. The receiver would have to have properly received and decoded the address for the command to be improperly executed.

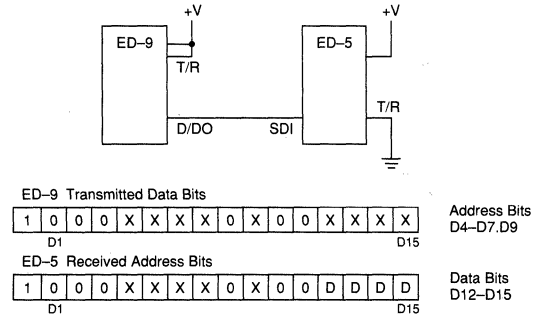


Figure 5. Data Patterns

Impulse noise could also cause errors in the address section of the data transmission, in which case the control command would be ignored due to improper address match. The effect of impulse noise on the operating system is not as much a problem with the encoder/decoder section but with the power line modem, which is improperly decoding the 125KHz bursts.

The impedance of the line is likewise ill-defined. It may be resistive, inductive or capacitive. Line attenuation is difficult to estimate because it is extremely load dependent. A high-power load can significantly reduce the impedance of the line at the point of connection and thus dominate attentuation for all points of communication that occur beyond the offending load unless that load is isolated with chokes. Capacitive loads can be equally troublesome and are not necessarily associated with high-power loads. Another large component of the net attenuation can be the signal loss incurred in coupling across the multiple windings of a power distribution transformer. This alone can amount to 20 to 40 db, depending on carrier frequency and transformer construction. The system described in this application will have problems communicating to the receiver units if the line attenuation is large enough to load the transmitted signal to a level below the receive sensitivity of the power line modem.

Designing for the Power line Environment

The application described in this paper is a relatively simple use of existing technology to achieve a low cost means of control communication over the AC power line. The system is very flexible with regards to the ability to add microprocessor intelligence to the transmit and receive ends of the communication link. This added intelligence may be used to overcome some of the problems associated with power line noise.

The microprocessor could be used to allow both receive and transmit at the same location. The microprocessor would enable the use of a closed-loop communication link with the unit that is to be controlled. This ability could be used to obtain status reports from the control unit, to make sure the unit properly responded to control information. In the case of a unit not properly responding to control messages, the controller would simply resend the control message until the unit properly responds. The microprocessor software could also include algorithms that detect power line noise or other power line communication. When noise or communication is detected, the microprocessor would simply wait until the power line was quiet enough for it to transmit its control message.

There are numerous methods for overcoming the problems associated with power line impedance. If the problem is due to the transmitted signal level, then line drivers can be added to boost the transmitted signal level. If the problem is due to cross phase attenuation caused by transformers, then a capacitor can be used to couple the communication signal across the windings.

The primary problem that everybody is faced with when interfacing to the power line is that the communication media (power line) is different at each installation. The key is to offer a system that is flexible enough to adapt to the demands of the environment.

Summary

Flexibility of the Supertex Encoder-Decoder devices can be utilized to make practical a simple power line interface design that has the capability to transmit data bidirectionally as well as the simple address match On/Off function. This design is only a representation of the many possible new product designs that can result from the use of the Supertex Encoder-Decoder in power line systems.

Supertex inc.

Static Handling and Testing Techniques For MOS Devices

CAUTION MUST BE USED WHEN HANDLING AND TESTING MOS DEVICES. STANDARD PROCEDURES SHOULD INCLUDE THE FOLLOWING TECHNIQUES IN ORDER TO AVOID POSSIBLE STATIC DAMAGE:

1. Store MOS devices in conductive carbon or nickel shipping bags, conductive foam, or conductive tote bins.
2. The person handling the device should be grounded by the use of a 0.5 to 1.5MΩ wrist-strap.
3. Workstations should have grounded conductive mats over non-conducting surfaces.
4. All conductive surfaces and equipment must be connected to earth ground.
5. Rubber gloves and clothing that do not generate static are recommended to be worn by any person handling parts.
6. All parts should be handled by their packages and not by the leads.
7. Relative room humidity should be kept between 45 to 60% since static generation increases exponentially as humidity decreases.
8. Work, testing and storage areas should be mopped monthly with staticide solution or equivalent.
9. For further details refer to DOD Handbook 263 and DOD Standard 1686.

FOR YOUR CONVENIENCE, THE FOLLOWING IS A PARTIAL LIST OF COMPANIES THAT SUPPLY ANTISTATIC PRODUCTS:

1. 3M Nuclear Products 3M Center St. Paul, MN 55101	Conductive Bags, Grounding Mats, Tote Bins and Other Material
2. Wescorp/DAL Industries, Inc. 1155 Terra Bella Ave. Mountain View, CA 94043	Wrist Straps
3. Biggam Enterprises, Inc. 2124 Bering Dr. San Jose, CA 95131	Wrist Straps, Staticide and Other Antistatic/Conductive Material
4. Free-Flow Packaging Corp. 2500 Middlefield Rd. Redwood City, CA 94063	Anti-Static Packaging Material

Quality Assurance

The Management of Supertex Incorporated is committed to the continued enhancement of product excellence and service through the dynamics of its Reliability and Quality Assurance System, through the integrity of its people, and through the many professional disciplines engaged in new product development and process innovation.

It is the chartered responsibility of the Reliability and Quality Assurance Manager to oversee and ensure enforcement of Supertex's Quality System. A formal yearly review is undertaken to ensure continued development of a Quality System that maintains a competitive stance with the marketplace and meets customer requirements.

Primary Job Charter of the R & QA Departments:

In-Process QC – The primary responsibilities of the Quality Control department are to establish and maintain effective controls for monitoring manufacturing processes and equipment; to provide information concerning the state-of-control; and to initiate statistically valid techniques to further improve Quality and Reliability levels. This concept is used extensively in, but not limited to, the following major Quality Control functions:

- Incoming Raw Materials Qualification
- Wafer Fabrication Monitors/Audits
- Assembly Monitors/Audits
- Test Monitors/Audits

Quality Assurance (Standard and Hi-Reliability) – The primary responsibilities of the Quality Assurance department are to ensure that the delivered product meets appropriate workmanship standards and any special customer requirements. This is accomplished through a program of process controls and gates designed so that all devices are properly tested and sampled prior to shipment. Control/inspection data keeps all relevant personnel fully informed on the quality level of product going through final test operations. Major Quality Assurance functions include:

- Incoming Contract Subassemblies Inspection
- Wafer Electrical Test
- Product Assurance Electrical Test
- Outgoing Plant Clearance

Reliability – The primary responsibility of the Reliability function is to assure that a high and consistent level of product reliability is maintained. Reliability establishes, defines and maintains evaluation programs to determine process/product reliability. Major Reliability activities include:

- Failure Analysis
- Hi-Reliability Programs
- Process/Product Qualifications
- New Product Design Evaluations
- Reliability Assurance Monitors

Document Control – The primary responsibilities of the Document Control department are to translate and format internal operating procedures and customer requirements into a system of regulatory written instructions. Document Control functions to ensure documentation integrity by establishing and maintaining procedures for:

- Initiating, revising, approving, distributing, recalling, and archiving documents.

Organization

The Manager of Quality Assurance/Quality Control reports directly to executive staff level of Management.

Reliability Assurance maintains a dual level of reporting — to the QA/QC Manager for R & QA program coordination, Reliability Assurance monitor and control, failure analysis, and to the Product Vice President for Reliability Assurance and qualification of product/process. This type of structure provides for the autonomy and direction that is needed to successfully manage the Reliability functions and maintain technological awareness in specific product support areas.

It is the responsibility of the R & QA Manager to administer the planning, organization, execution, surveillance, appraisal, corrective action and documentation of Quality Programs within the chartered responsibility. The character, responsibility and authority vested with the R & QA Manager will establish the means to attain the necessary Quality and Reliability objectives in all aspects of manufacturing.

Quality programs administered by the R & QA Department support the following functions:

Operator Training – Supertex maintains a System of Operator Training and Qualification specific to the nature and complexity of each manufacturing operation, inspection, or test requirement. The basic training approach used by Supertex is supervised on-the-job training assisted by experienced/qualified personnel to provide a "buddy system" of training.

Training is typically performed with the same equipment and tools used in the normal manufacturing environment. The use of training aids, such as films, photographs and demonstrations of equipment and tools, is typical.

Each department manager is responsible for the training and evaluation of the workmanship performance to manufacturing norms.

The R & QA department maintains a System of Audits/Monitors for evaluating Operator's adherence to specification and quality of workmanship.

Raw Material Procurement and Qualification – Supertex maintains a system that ensures economical control and conformance to detailed technical and quality requirements of purchased materials (direct and critical indirect). Material procurement is performed through regulated specifications and drawings. R & QA functions within this system by providing the following services:

- Documented instructions for material evaluation, procedures, flow, workmanship standards, test methods and statistical sampling.
- Incoming inspection of raw materials.
- Identification and segregation of qualified and nonconforming material.
- Vendor qualification and ongoing vendor performance appraisal.
- Feedback of inspection results and informing suppliers of new design changes on raw materials.
- Formal review for disposition of nonconforming materials.

Equipment Calibration – Supertex maintains a Calibration System that ensures measurement accuracy of equipment used to determine product workmanship and acceptability.

The Calibration System conforms to MIL-STD-45662. Major provisions of the R & QA program are described as follows:

- Qualification of external calibration services.
- Traceability of references to National Bureau of Standards. Identifications of measurement and test equipment (electrical, mechanical, and optical) for type and frequency of calibration.
- Document file certifying equipment calibration and recall history.
- Management report on recall status.
- R & QA audits of equipment calibration (date stickers and recall designation).

Manufacturing Flow, Inspection, and Test Points – Supertex maintains Flow Charts that describe the sequential steps of semiconductor processing and associated documentation for Wafer Fabrication, Assembly, and Post Assembly Finishing through Final Outgoing Plant Clearance. Flow charts are prepared for each product family and associated manufacturing technology.

Flow charts that delineate Fabrication processing are regarded as proprietary and are not available for external dissemination without prior approvals from the R & QA Manager and respective Product/Operations Vice President. Applicable Assembly Packaging Flow Charts are Available upon request.

Flow charts for Customer Hi-Reliability Products are documented by a detailed lot traveler which defines all sequential operations, manufacturing inspection points, Customer Source Inspection points, and Quality Assurance product sample acceptance points.

In-Process Quality Control — Quality Control is a system of measurement and surveillance. The System is comprised of visual, dimensional, structural, and electrical characterization of material from incoming receipt of raw goods to outgoing finished product. Information obtained provides management with an overview on the state-of-the-process by specifically quantifying position of product yield, quality, and reliability.

Major elements found in Supertex's Quality Control Program are summarized by, but not limited to, the following:

- Environmental monitors (Airborne Particle counts, % RH and temperature).
- Routine Scanning Electron Micrography (SEM) of semiconductor devices.
- Specification compliance audits.
- Random monitor of wafers in-process.
- Electrostatic discharge prevention/monitor.
- Product lot sample qualification at critical manufacturing points.
- Wafer/die electrical sort monitor.
- Quality performance/trend data reporting.
- Return material analysis reporting.
- Monitoring of storage, handling, packaging, and identification of raw materials, of work-in-process, and of finished product.

Product Assurance Inspection – Supertex maintains a system of Product Qualification through inspection and test of finished product prior to customer shipment.

The Quality Assurance department provides inspection based on statistical sampling to ensure that outgoing product quality meets internal workmanship standards and customer procurement requirements.

The following process controls, inspections, tests, and documentation requirements are assured prior to submission of product to Customer Source Inspection and prior to final Outgoing Plant Clearance:

- Test equipment correlation and qualification.
- Monitor manufacturing test operations.
- Ensure conformance of product lots to detailed customer test requirements (Electrical, External Visual, and Mechanical).
- Assure proper and complete documentation for each product lot, both in-process and at-plant clearance.

Reliability Assurance – At Supertex the Reliability Concept is introduced at the design phase of all new products. The factors that may affect product reliability are: compatibility of fabrication process, circuit layout and characteristics, assembly process, package materials, and application. Hence, Reliability Engineering is involved in evaluating all critical factors of reliability, starting with the design and first prototype functional circuit. From analysis, modification of design, wafer fabrication, and assembly, process changes can be implemented to enhance the reliability of the product. Approval is given for the release of new product to manufacturing only after the reliability of the product is established as acceptable within standard norms.

The Reliability department provides the Product group with a number of programs to define product reliability levels. Among these programs are: 1) Qualification, 2) Reliability, 3) Failure Analysis, and 4) Data Collection and Presentation.

Qualification Program of New Products and Processes:

- Procedures for qualification of new product designs require Reliability participation and approval in design reviews, documentation, characterization, and reliability stress studies.

- New package qualification is approved and released for production by Reliability after prescribed environmental tests have been successfully completed.
- Qualification of a new product is granted only after Quality and Reliability have completed evaluation of process control studies. Significant modifications to existing processes are treated as new processes for the purpose of qualification.
- Proper documentation of all changes to process steps and procedure, and of any new or improved designs or material, is assured by Reliability's approval.

Reliability Monitor Programs:

- Device and Package Reliability Monitor Programs are effected for all packages using a variety of device types to maximize data usefulness and to evaluate cost effectiveness of equipment.
- Packages are evaluated using all applicable methods of MI STD-883; Level B, or MIL-STD-750, as appropriate. Data are reported, as specified, in detailed procedures for each package-chip combination. Package Monitor programs include, but are not limited to, the following general tests, using the appropriate conditions specified in MIL-STD-883, Level B, Method 5005:

Condition	Method
Operating Life (HTRB)	1005
Steam Pressure (Molded packages)	N/A
Temperature Cycling	1010
Package Hermeticity	1014
Intermittent Opens (Molded package)	N/A
Salt Atmosphere (Initial Qual, only)	1009
Constant Acceleration	2001
Mechanical Shock (Initial Qual, only)	2002
Solderability	2003
Lead Integrity	2004
Vibration (Initial Qual, only)	2007
Biased Temperature Humidity (Molded packages)	N/A

- Accelerated Stress Monitor Programs are conducted to obtain timely feedback for process evaluations, as well as for ultimate device capability studies.

Failure Analysis:

- It is the policy of Supertex to perform analysis of defective product and utilize the resulting findings to improve product yield and integrity.
- Reliability Engineeering also performs failure analysis in mode and the mechanism of all failures (both from routine reliability tests and customer returns).

Failure Analysis Support Activities Include:

- Qualification of existing products for new applications.
- Customer Qualifications. Reliability is responsible for review and acceptance of all customer requirements. When qualification programs or special testing is required, Reliability designs and implements appropriate test plans and coordinates with customer.
- Failure analysis, in support of In-Process Quality Control monitors, is handled by Reliability through Failure Report Requests. This support includes such services as visual inspection, metallography, thickness measurements, selective etching, and die probing.
- Customer's requests for failure analysis are filled by Reliabiltiy, which coordinates all replies to customers and approves all correspondence outside the Company.
- Where Reliability has determined that corrective action is necessary prior to the release of product for shipment, or to proceed further in production processing, a Corrective Action Request is generated by Reliability. No shipment may occur if the integrity of product reliability would be jeopardized.

Reporting and Publication of Data:

Qualification test reports are prepared and distributed by Reliability for all certified products and processes which have been formally qualified and released for manufacturing.

Reliability is responsible for assisting the Marketing department in the preparation of publications for distribution to field sales locations and to customers.

Presently, the in-house Reliability Assurance testing is supplemented by testing done at outside Test Laboratories that have been approved by D.E.S.C. for performing MIL-STD testing.

In addition, Reliability Assurance maintains a routine monitor of commercial grade finished product to evaluate reliability attributes against internally published norms. Products and packages are deliberately selected to represent typical characteristics and conditions of manufacturing – with the following considerations given:

- Design complexity and fabrication processing technology.
- Package type/assembly construction and materials.
- Assembly plant location.

Supertex reliability data for standard product is published for internal use. Specific reliability information is made available to customers upon request.

Plant Clearance Inspection – Supertex maintains a Final Outgoing Inspection on Finished asssembled/tested product to ensure that all conditions of processing have been satisfied and that support documentation, as specified by contract, is maintained for each shipped lot.

Provisions for the control of shipped product during the Outgoing Plant Clearance Final Acceptance Program are structured to ensure product workmanship guarantees are met.

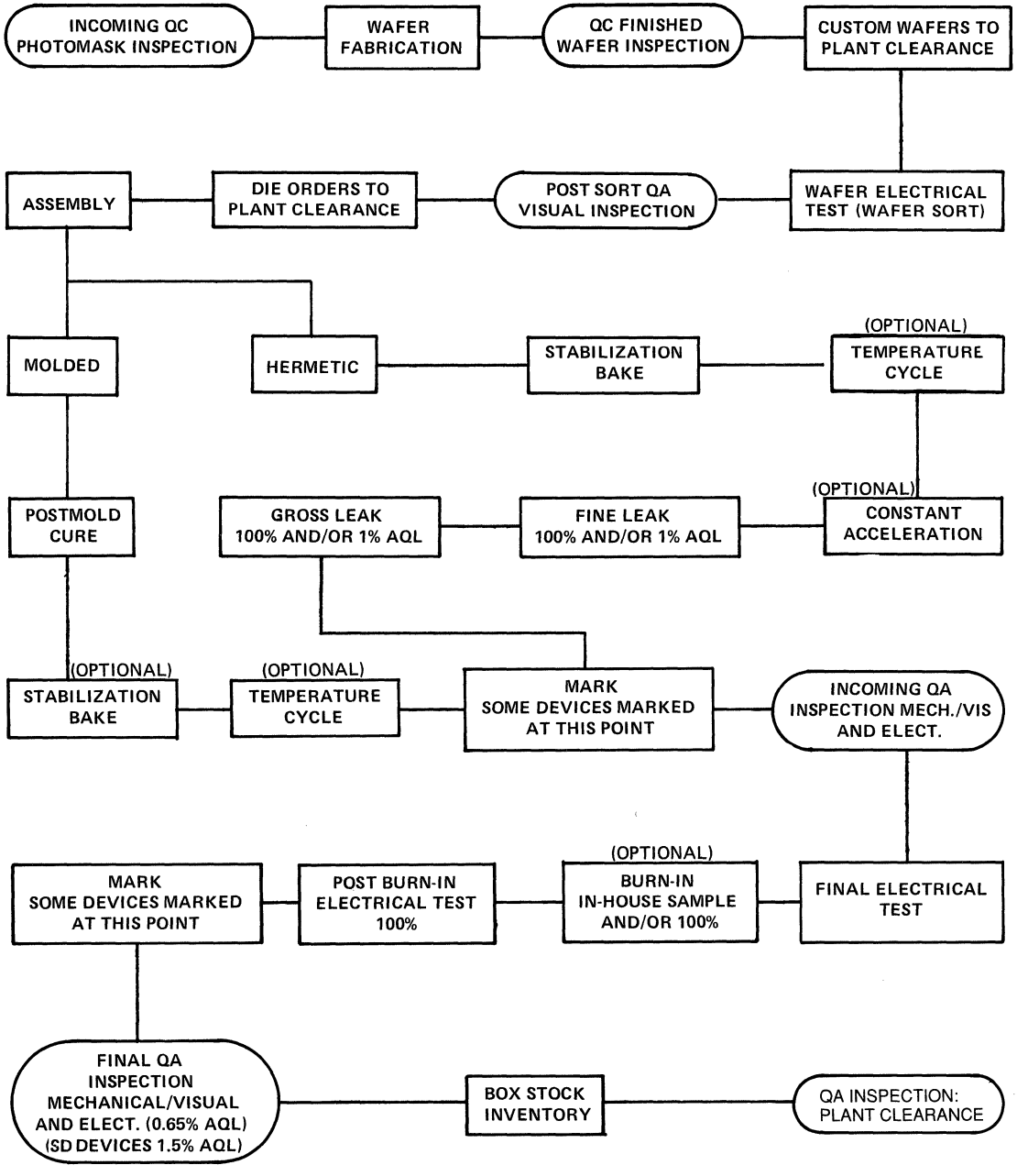
Summary

Supertex maintains R & QA Programs at critical operations to assure that products are manufactured under a documented and controlled system for consistency in workmanship standards (fit, form, function, and reliability).

The following Standards and Specifications have been integrated into Supertex's manufacturing operations and process control programs:

- FED-STD-209 Clean Room and Work Station Requirements, Controlled Environments.
- MIL-M-38510 Microcircuits, General Specification For.
- MIL-Q-9858 Quality Program Requirements.
- MIL-I-45208 Inspection Systems.
- MIL-S-19500 Semiconductor Devices, General Specification For.
- MIL-STD-105 Sampling Procedures and Tables for Inspection by Attributes.
- MIL-STD-750 Test Methods for Semiconductor Devices.
- MIL-STD-883 Test Method and Procedures for Microelectronics.
- MIL-STD-202 Test Methods for Electronic and Electrical Component Parts.
- MIL-STD-45662 Calibration System Requirements.
- Special Customer Specifications

HVCMOS Standard Product Flow



Note: Quality Assurance shall exercise the option to incorporate this screen to assure quality workmanship and conformance guarantees.

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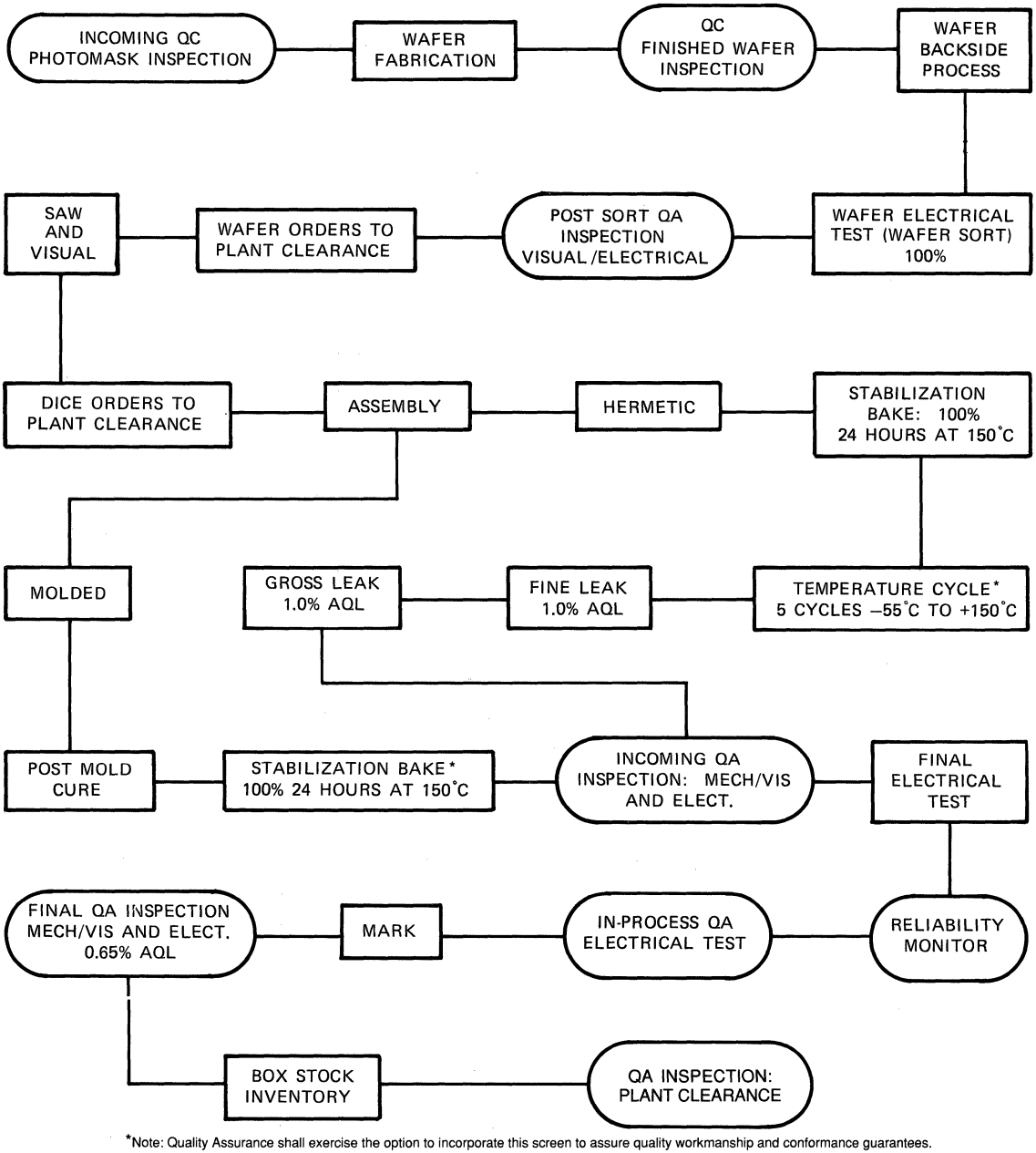
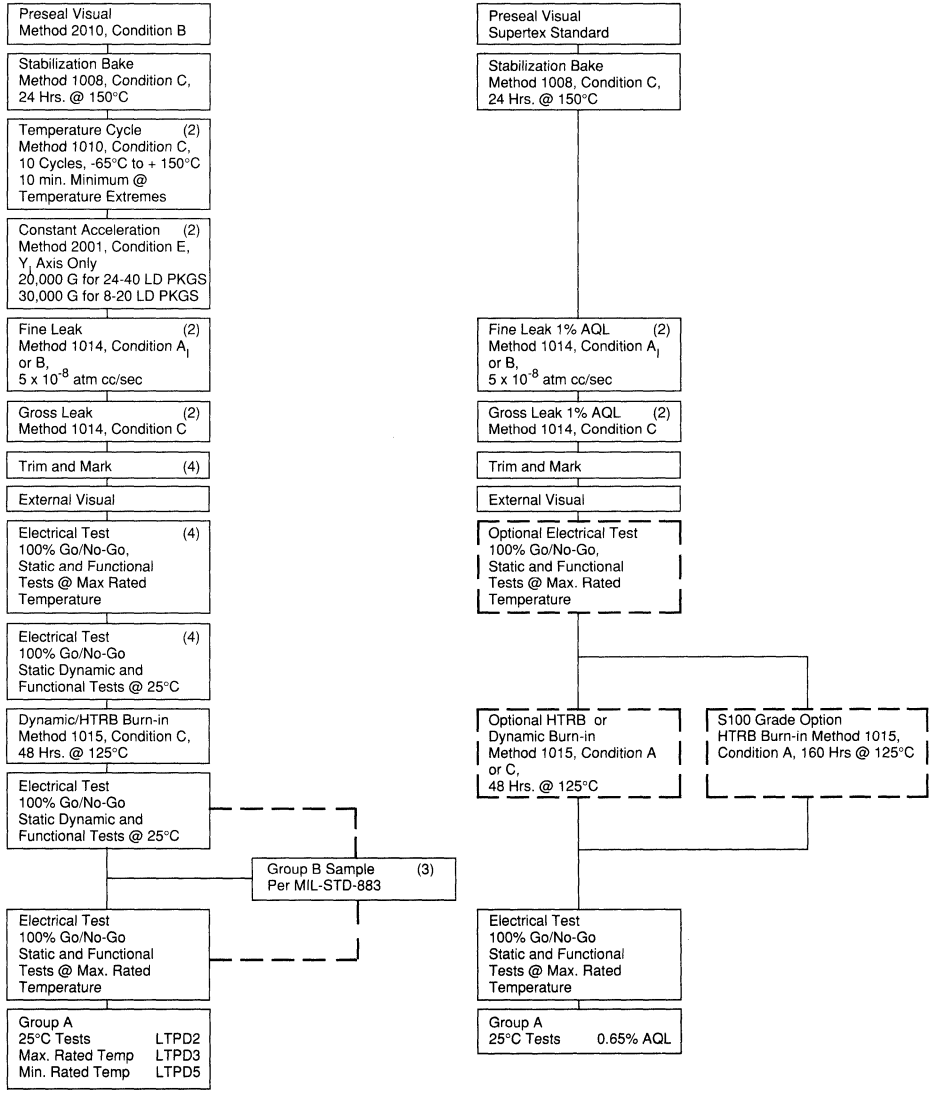
DMOS Standard Product Flow



*Note: Quality Assurance shall exercise the option to incorporate this screen to assure quality workmanship and conformance guarantees.

HVCMOS IC Process Option Flow Chart



Note 1: Processing consists of 100% screening and Group A. Generic data available on request.
Note 2: Hermetic packages only.
Note 3: Group C & D periodic lot sampling per MIL-STD-883.
Note 4: As required.
All test methods are per MIL-STD-883 unless specified otherwise.

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DMOS Process Option Flow Chart

DMOS ARRAY RB FLOW (SIMILAR TO MIL-STD-83 CLASS B) (1)	**SX FLOW** (SIMILAR TO JAN TX) **SXV FLOW** (SIMILAR TO JAN TXV) (1)	**COMMERCIAL BURN-IN SC FLOW**	**STANDARD PRODUCTS**	**SJ FLOW** (SIMILAR TO JAN)
Preseal Visual Method 2010, Condition B	Preseal Visual Method 2072			
Stabilization Bake Method 1008, Condition C, 24 Hrs. @ 150°C	Stabilization Bake Method 1032, 24 Hrs. @ 150°C	Stabilization Bake Method 1032, 24 Hrs. @ 150°C	Stabilization Bake Method 1032, 24 Hrs. @ 150°C	Stabilization Bake Method 1032, 24 Hrs. @ 150°C
Temperature Cycle Method 1010, Condition C, 10 Cycles, -65°C to +150°C	Temperature Cycle Method 1051 20 Cycles, -65°C to + 150°C			
Constant Acceleration (2) Method 2001, Condition E, Y_1 Axis Only	Constant Acceleration (2) Y_1 Axis, TO-3 – 10,000 G, Others – 20,000 G			
Fine Leak (2) Method 1014, Condition A or B, 5×10^{-8} atm cc/sec	Fine Leak (2) Method 1071, Condition G or H, Maximum Leak Rate TO-3 – 5×10^{-7} atm cc/sec Others – 5×10^{-8} atm cc/sec	Fine Leak 1% AQL (2) Method 1071, Condition G or H, Maximum Leak Rate TO-3 – 5×10^{-7} atm cc/sec Others – 5×10^{-8} atm cc/sec	Fine Leak 1% AQL (2) Method 1071, Condition G or H, Maximum Leak Rate TO-3 – 5×10^{-7} atm cc/sec Others – 5×10^{-8} atm cc/sec	Fine Leak 1% AQL (2) Method 1071, Condition G or H, Maximum Leak Rate TO-3 – 5×10^{-7} atm cc/sec Others – 5×10^{-8} atm cc/sec
Gross Leak (2) Method 1014, Condition C	Gross Leak (2) Method 1071, Condition C	Gross Leak (2) Method 1071, Condition C	Gross Leak (2) Method 1071, Condition C	Gross Leak (2) Method 1071, Condition C
Electrical Test (5) 100% Go/No-Go, 25°C D.C. Parameters	Electrical Test (4) 100% Go/No-Go, 25°C D.C. Parameters	Electrical Test 100% Go/No-Go, 25°C D.C. Parameters	Electrical Test 100% Go/No-Go, 25°C D.C. Parameters	Electrical Test 100% Go/No-Go, 25°C D.C. Parameters
HTRGB Burn-in (5) Method 1015, Condition A, 48 Hrs. @ 150°C	HTRGB Burn-in (3) Method 1039, Condition A, 48 Hrs. @ 150°C			
Electrical Test (4) 100% Go/No-Go 25°C D.C. Parameters	Electrical Test (4) 100% Read and Record, 25°C D.C. Parameters			
HTRB Burn-in Method 1015, Condition A, 160 Hrs. @ 125°C	HTRB Burn-in Method 1039, Condition A, 168 Hrs. @ 150°C	HTRB Burn-in Method 1039, Condition A, 96 Hrs. @ 150°C		
Electrical Test (4) 100% Go/No-Go 25°C D.C. Parameters	Electrical Test (4) 100% Read and Record, 25°C D.C. Parameters	Electrical Test 100% Go/No-Go 25°C D.C. Parameters		
	Electrical Test 100% Go/No-Go, Group A, Subgroup 2			
Group A Subgroup 1 VIS/MEC, LTPD 5, Subgroup 2 D.C. @ 25°C LTPD 5, Subgroup 3 D.C. Min./Max., LTPD 5, Subgroup 4 A.C. LTPD 5	Group A Subgroup 1 VIS/MEC, LTPD 5, Subgroup 2 D.C. @ 25°C LTPD 5, Subgroup 3 D.C. Min./Max., LTPD 5, Subgroup 4 A.C. LTPD 5	Group A Subgroup 1 VIS/MEC, LTPD 5, Subgroup 2 D.C. @ 25°C LTPD 5, Subgroup 3 D.C. Min./Max., LTPD 5, Subgroup 4 A.C. LTPD 5	Group A Subgroup A 0.65% AQL Subgroup 1 VIS/MEC, Subgroup 2 D.C. @ 25°C	Group A Subgroup 1 VIS/MEC, LTPD 5 Subgroup 2 D.C. @ 25°C, LTPD 5 Subgroup 3 D.C. Min./Max., LTPD 5 Subgroup 4 A.C. LTPD 5

Note 1: Processing consists of 100% screening and Group A only. Preseal Visual applies to "SXV" version only.
Note 2: Hermetic packages only.
Note 3: HTRGB-High temperature reverse gate bias.
Note 4: Read and Record with delta and percent values is optional.
Note 5: Optional.
All test methods are per MIL-STD-750 unless specified otherwise.

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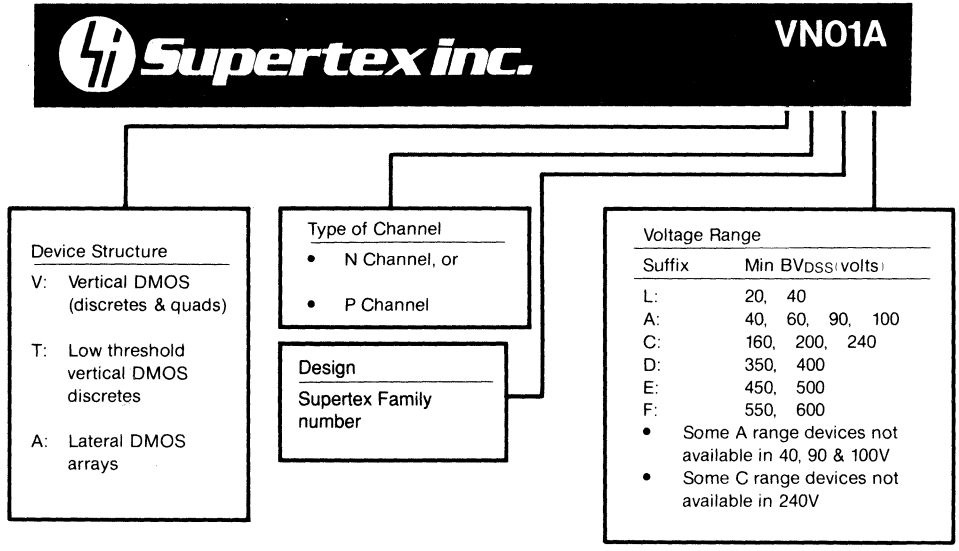
Understanding MOSFET Data

The following outline explains how to read and use Supertex MOSFET data sheets. The approach is simple and care has been taken to avoid getting lost in a maze of technical jargon.

The VN01A data sheet was chosen as an example because this is one of the most popular devices and has the largest choice of packages. The product nomenclature shown applies only to Supertex proprietary products.



Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speed are desired.

This section outlines main features of the product

Product Summary

N-Channel Enhancement-Mode Vertical DMOS Power FETs

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package							
			TO-39	TO-92	TO-52	TO-220	Quad P-DIP	Quad C-DIP	Quad C-LCC	DICE
40V	3Ω	2.0A	VN0104N2	VN0104N3	VN0104N9	VN0104N5	VN0104N6	VN0104N7	—	VN0104ND
60V	3Ω	2.0A	VN0106N2	VN0106N3	VN0106N9	VN0106N5	VN0106N6	VN0106N7	VN0106NE	VN0106ND
90V	3Ω	2.0A	VN0109N2	VN0109N3	VN0109N9	VN0109N5	—	—	VN0109NE	VN0109ND

Drain to source breakdown voltage & drain to gate breakdown voltage

Maximum resistance from drain to source when device is fully turned on

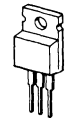
Minimum drain current when device is fully turned on

Package Options

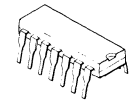
TO-39
Hermetic metal can
- Moderate power dissipation
- Industrial/Military applications

TO-92
Plastic
- Low power
- Mainly commercial applications
- Cost effective

TO-52
Hermetic metal can
Low power
Industrial/Military applications



TO-220
Plastic
- High power
- Commercial/Industrial applications

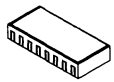


14-LEAD DIP
Dual in line plastic
- 4 dice in one package
- Commercial/Industrial applications

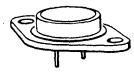
Product Summary

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package							
			TO-39	TO-92	TO-52	TO-220	Quad P-DIP	Quad C-DIP	Quad C-LCC	Dice
40V	3Ω	2.0A	VN0104N2	VN0104N3	VN0104N9	VN0104N5	VN0104N6	VN0104N7	—	VN0104ND
60V	3Ω	2.0A	VN0106N2	VN0106N3	VN0106N9	VN0106N5	VN0106N6	VN0106N7	VN0106NE	VN0106ND
90V	3Ω	2.0A	VN0109N2	VN0109N3	VN0109N9	VN0109N5	—	—	VN0109NE	VN0109ND

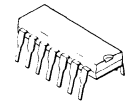
ND: Die in waffle pack
Die can be visually inspected to commercial (standard) or military visual criteria (specify while ordering).



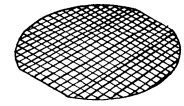
16-TERMINAL LCC
Ceramic Leadless Chip Carrier
- 4 dice in one package



TO-3
Hermetic metal can
- Very high power
- Commercial/Industrial/Military requirements



14-LEAD DIP
Dual in line ceramic
- 4 dice in one package Industrial/Military requirements



NW: Die in wafer form
- 4" diameter wafers
- Reject die are inked

6

Extreme conditions a device can be subjected to electrically and thermally. Stress in excess of these ratings will usually cause permanent damage.

Ratings given in product summary

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate	BV_{DGS}
Gate-to-Source Voltage	±20V
Operating and Storage Temperature	−55°C to +150°C
Soldering Temperature	300°C

V_{GS}
- All Supertex FETs are rated for ±20V
- ± voltage handling capability allows quick turn off by reversing bias.
- External protection should be used when there is a possibility of exceeding this rating. Stress exceeding ±20V will result in gate insulation degradation and eventual failure.

- All Supertex devices can be stored and operated satisfactorily within these junction temperature (T_J) limits
- Appropriate derating factors from curves and change in parameters due to reduced/elevated temperatures have to be considered when temperature in not 25°C
- Operation at T_J below maximum limit can enhance operating life

Maximum allowable temperature at leads while soldering, 1.6mm away from case for 10 seconds.

Thermal Characteristics

Device characteristics affecting limits of heat produced and removed from device. Die size, $R_{DS(ON)}$, and packaging type are the main factors determining these thermal limitations.

θ_{ja}

Thermal resistance from junction to air.

- Depends mainly on package and die size.

θ_{jc}

Thermal resistance from junction to case.

- Depends mainly on package and die size
- To determine T_J use equation $T_J = P_D \times \theta_{jc} + TA$

Package	I_D (continuous) (Note 3)	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}
TO-39	0.8A	2.5A	3.5W	125	35	.08A	2.5A
TO-92	0.5A	2.0A	1.0W	170	125	0.5A	2.0A
TO-52	0.5A	2.0A	1.0W	170	125	0.5A	2.0A
TO-220	1.5A	2.5A	15.0W	70	8	1.5A	2.5A
Plastic DIP Ceramic DIP	See DMOS Arrays and Special Functions section.						

I_{DRM}

300 μS, 2% duty cycle pulsed Current handling capability of drain to source diode.

- Factors affecting this parameter same as ID (pulsed)

I_{DR}

Continuous current handling capability of drain to source diode.

- Factors affecting value same as ID (continuous)

I_D (continuous)

Maximum Continuous current carrying capability of device.

- Depends mainly on:
  - A. $R_{DS(ON)}$ — on state resistance
  - B. PD — maximum power dissipation for package
  - C. Die size
  - D. Maximum junction temperature

I_D (pulsed)

Maximum non-continuous pulse current carrying capabilty for a 300 μS 2% duty cycle pulse.

- Depends mainly on:
  - A. $R_{DS(ON)}$
  - B. P_D max.
  - C. Diameter of bonding wire
  - D. Die size
  - E. Maximum junction temperature

Power Dissipation

- Maximum power package can dissipate when case temperature is 25° C.
- When case temperature is higher than 25° C, use PD vs. Tc curve to determine dissipation permissible.

The following DC parameters are 100% tested with 300 μS, 2% duty cycle pulse at 25°C; BV_{DSS}, $V_{GS(TH)}$, I_{DSS}, $I_{D(ON)}$ & $R_{DS(ON)}$.

- $\Delta V_{GS(TH)}$ and $\Delta R_{DS(ON)}$ are guaranteed by design ie., when device is functional for other DC parameters, these two parameters will not deviate from published values.
- Since a representative sample is adequate to assure consistency of specs, A.C. parameters are sample tested on a lot/batch basis.
- High temperature testing on sample basis when requested with hi-rel processing.
- Refer to section 3 "power MOS structures" for test circuits used for measurement.

Electrical Characteristics (@ 25° C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage VN0109	90			V	I_D = 1mA, V_{GS} = 0
	VN0106	60				
	VN0104	40				
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.4	V	V_{GS} = V_{DS}, I_D = 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.8	-5.5	mV/°C	I_D = 1mA, V_{GS} = V_{DS}
I_{GSS}	Gate Body Leakage		0.1	100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			1	uA	V_{GS} = 0, V_{DS} = Max Rating
				100		V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	0.5	1.0		A	V_{GS} = 5V, V_{DS} = 25V
		2	2.50			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	3	4.50	5	Ω	V_{GS} = 5V, I_D= 250mA
		2.3	2	3		V_{GS} = 10V, I_D = 1A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.70	1	%/°C	I_D = 1A, V_{GS} = 10V
G_{FS}	Forward Transconductance	300	400		m℧	V_{DS} = 25V, I_D = 0.5A
C_{ISS}	Input Capacitance		45	60	pF	V_{GS} = 0, V_{DS} = 25V f = 1MHz
C_{OSS}	Common Source Output Capacitance		20	25		
C_{RSS}	Reverse Transfer Capacitance		2	5		
$t_{d(ON)}$	Turn-ON Delay Time		3	5	ns	V_{DD} = 25V, I_D = 1A, R_S = R_L = 50Ω
t_r	Rise Time		5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time		6	9		
t_f	Fall Time		5	8		
V_{SD}	Diode Forward Voltage Drop		1.2	1.8	V	I_{SD} = 2.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time		400		ns	I_{SD} = 1A, V_{GS} = 0

BV_{DSS}

- Please see product summary (part 1)
- Positive temperature coefficient. See curve BV_{DSS} VS. T_J.

$V_{GS(TH)}$

- Voltage required from gate to source to turn on device to certain I_D current value given in "condition" column
- I_D measurement condition is low for small die and higher for larger die

$\Delta V_{GS(TH)}$

- Threshold voltage reduces when temperature increases and vice versa.
- Value at temperature other than 25°C can be determined by $V_{GS(TH)}$ (normalized) VS. T_J curve.

I_{GSS}

- Since the gate is insulated from the rest of the device by a silicon dioxide insulating layer, this parameter depends on thickness/integrity of layer and size of device.
- Measured at maximum permissible voltage from gate to source: ±20V.
- Values of this parameter are often tens/hundreds of times less than published maximum value.
  Electrical screening is done at 100nA since test equipment functions slowly at lower values, which is not practical for mass production.
  Consult factory for screening lower values.

I_{DSS}

- This is the leakage current from drain to source when device is fully turned off.
- Measured by applying maximum permissible voltage between drain and source (BV_{DSS}) and gate shorted to source (V_{GS}=0)
- Special electrical screening possible at lower values since max. published values are higher to achieve practical testing speeds.

$\Delta R_{DS(ON)}$

- Positive temperature coefficient.
- Enhances stability due to current sharing during parallel operation.

$R_{DS(ON)}$

- Drain to source resistance measured when device is partially turned on at V_{GS} = 5V, and fully turned on at V_{GS} = 10V.
- Designers should use maximum values for worst case condition.
- When better turn on characteristics (ie., low $R_{DS(ON)}$) is required for logic level inputs, Supertex's low threshold TN & TP devices may be used.
- Typical value of $R_{DS(ON)}$ can be calculated at various V_{GS} conditions by using output characteristics or saturation characteristics family of curves (V_{GS} Vs I_D).
- $R_{DS(ON)}$ increases with higher drain currents.
  $R_{DS(ON)}$ Vs. $I_{D(ON)}$ curve has a slight slope for values low values of I_D, but rises rapidly for high values.

$I_{D(ON)}$

- Defined as the minimum drain current when device is turned on.
- Supertex measures $I_{D(ON)}$ min. at two test conditions:
  V_{GS} = 5V and V_{GS} = 10V, to give the designer a look at both logic level turn on and full turn on.
  Although Supertex specifies a typical value of $I_{D(ON)}$, the designer should use minimum value as the worst case.

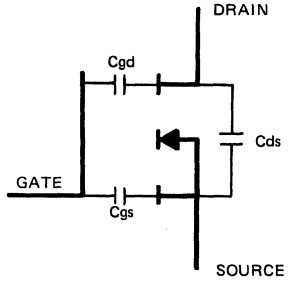
SWITCHING CHARACTERISTICS

- Extremely fast switching compared to bipolar transistors, due to absence of minority carrier storage time during turn off.
- Switching times depend almost totally on interelectrode capacitance, R_S (source impedance) and R_L (load impedance) as shown on test circuit.

C_{ISS}, C_{RSS}, C_{OSS}

- Please see section 3 in data book "power MOSFET Electrical Performance" for interelectrode capacitances and equivalent circuit.
- Supertex interdigitated structures have lowest C_{ISS} in the industry for comparable die sizes and exhibit excellent switching characteristics.
- Values of these capacitances are high at low voltages across them. Please see capacitance vs. V_{DS} curves for details.
- Negligible effect of temperature on capacitances.
- The following equation may be used for calculating effective value of C_{ISS} with "Miller Effect":

$$C_{ISS} = C_{GS} + (1 + G_{FS} R_L) C_{GD}$$



Ciss = Cgd + Cgs

Coss = Cgd + Cds

Crss = Cgd

G_{FS}

- Represents gainof the device and can be compared to H_{FE} of a bipolar transistor.
- Value is the ratio of change in I_D for a change in V_{GS}

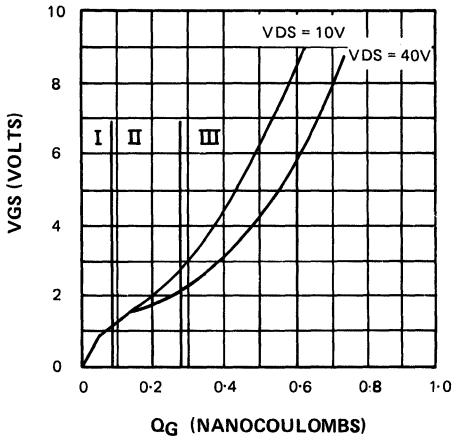
$$G_{FS} = \frac{\Delta I_D}{\Delta V_{GS}}$$

- Rises rapidly with increasing I_D, and then becomes constant in the saturation region. See V_{GS} vs. I_D curve.

$TD_{(ON)}$

- During this period, the drive circuit changes C_{ISS} to up to $V_{GS(TH)}$. Since no drain current flows prior to turn on, V_{DS} and consequently C_{ISS} remain constant. Region I on the V_{GS} vs. Q_G curve shows linear change in voltage with increasing Q_G.

Gate Drive Dynamic Characteristics



Electrical Characteristics (@ 25° C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BVDSS	Drain-to-Source Breakdown Voltage VN0109	90			V	ID = 1mA, VGS = 0
	VN0106	60				
	VN0104	40				
VGS(th)	Gate Threshold Voltage	0.8		2.4	V	VGS = VDS, ID = 1mA
ΔVGS(th)	Change in VGS(th) with Temperature		-3.8	-5.5	mV/°C	ID = 1mA, VGS = VDS
IGSS	Gate Body Leakage		0.1	100	nA	VGS = ±20V, VDS = 0
IDSS	Zero Gate Voltage Drain Current			1	uA	VGS = 0, VDS = Max Rating
				100		VGS = 0, VDS = 0.8 Max Rating TA = 125°C
ID(ON)	ON-State Drain Current	0.5	1.0		A	VGS = 5V, VDS = 25V
		2	2.50			VGS = 10V, VDS = 25V
RDS(ON)	Static Drain-to-Source ON-State Resistance	3	4.50	5	Ω	VGS = 5V, ID= 250mA
		2.3	2	3		VGS = 10V, ID = 1A
ΔRDS(ON)	Change in RDS(ON) with Temperature		0.70	1	%/°C	ID = 1A, VGS = 10V
GFS	Forward Transconductance	300	400		m℧	VDS = 25V, ID = 0.5A
CISS	Input Capacitance		45	60	pF	VGS = 0, VDS = 25V f = 1MHz
COSS	Common Source Output Capacitance		20	25		
CRSS	Reverse Transfer Capacitance		2	5		
td(ON)	Turn-ON Delay Time		3	5	ns	VDD = 25V, ID = 1A, RS = RL = 50Ω
tr	Rise Time		5	8		
td(OFF)	Turn-OFF Delay Time		6	9		
tf	Fall Time		5	8		
VSD	Diode Forward Voltage Drop		1.2	1.8	V	ISD = 2.5A, VGS = 0
trr	Reverse Recovery Time		400		ns	ISD = 1A, VGS = 0

TR

- When CISS is driven to a voltage exceeding VGS(TH), conduction from drain to source begins. GFS increases causing increase in CISS due to "Miller Effect". Charge requirements for Region II increase considerably. Gain stabilizes in Region III and Miller Effect is nullified, resulting in a linear change in VGS for increase in QG.

TRR

- The reverse recovery time is the time needed for the carrier gradient, formed during forward biasing, to be depleted when the biasing is reversed.
- An external fast recovery diode may be connected from drain to source to improve recovery time.

TD(OFF)

- The sequence of events now begins to reverse. CISS discharges through RS and the 50 Ω resistor. The rise of VDS is initally slowed by increase of output capacitance.

TF

- VDS rises rapidly as the output capacitance falls.

VSD

- This is the forward voltage drop of the parasitic diode between drain and source.
- Diode my be used as a commutator in H bridge configurations or in a synchronous rectifier mode. Excessive fly back voltages may be clamped by this diode in a totem pole configuration.

Supertex inc.

DMOS Products

The Supertex DMOS Power MOSFET family utilizes both vertical and lateral, double-diffused MOS processes. These DMOS Power MOSFETs are ideally suited for a wide range of switching, driving, and amplifying applications. They feature high input impedance, fast switching speeds, and low threshold voltages. Available in a wide variety of packages types, they give the designer flexibility using state-of-the-art power semiconductor technology.

N-Channel Low Threshold MOSFETs

Device Family	BV_{DSS} Min (V)	$RDS_{(ON)}$ Max (ohms)	$I_{D(ON)}$ Min (A)	C_{ISS} Typ (pf)	$V_{GS(th)}$ Max (V)	Package Options				
						TO-39	TO-92	TO-220	Quad[1]	Die
TN01	20, 40	1.8	2.0	45	1.6	•	•			•
TN01	60, 100	3.0	2.0	50	1.6	•	•			•
TN02	20, 40	0.75	4.0	85	1.6	•	•			•
TN05	200, 240	10.0	0.3	45	1.5	•	•			•
TN06	20, 40	0.75	4.0	85	1.6	•	•			•
TN06	60, 100	1.50	3.0	85	1.6	•	•	•	•	•
TN06	200, 240	6.0	1.0	85	1.6	•	•	•		•

Note 1: Refer to Arrays and Special Functions section for packages available.

P-Channel Low Threshold MOSFETs

Device Family	BV_{DSS} Min (V)	$RDS_{(ON)}$ Max (ohms)	$I_{D(ON)}$ Min (A)	C_{ISS} Typ (pf)	$V_{GS(th)}$ Max (V)	Package Options				
						TO-39	TO-92	TO-220	Quad[1]	Die
TP01	20, 40	4.0	0.85	45	2.4	•	•			•
TP02	20, 40	2.0	2.0	85	2.4	•	•			•
TP06	20, 40	2.0	2.0	85	2.4	•	•			•
TP06	60, 100	3.5	1.5	85	2.4	•	•	•	•	•
TP06	160, 200	12.0	0.75	85	2.4	•	•	•		•

Note 1: Refer to Arrays and Special Functions section for packages available.

N-Channel DMOS Power FETs

Device Family	BV_{DSS} Min (V)	$RDS_{(ON)}$ Max (ohms)	$I_{D(ON)}$ Min (A)	C_{ISS} Typ (pf)	Package Options						
					TO-3	TO-39	TO-52	TO-92	TO-220	Quad[1]	Die
VN01	40,60,90	3.0	2.0	45		•	•	•	•	•	•
VN01	160, 200	10.0	0.4	45		•		•	•		•
VN02	40,60,100	2.0	3.0	85		•		•	•	•	•
VN02	160, 200	6.0	1.0	75		•		•	•		•
VN03	350, 400	2.5	3.0	550	•	•			•		•
VN03	450, 500	4.0	2.0	550	•	•			•		•
VN03	550,600	6.0	1.5	550	•				•		•
VN05	350, 400	35.0	0.25	45		•		•			•
VN05	450, 500	60.0	0.15	45		•		•			•
VN06	350, 400	10.0	0.75	85		•		•	•		•
VN06	450, 500	16.0	0.50	85		•		•	•		•
VN06	550, 600	20.0	0.25	85		•		•	•		•
VN11	60, 100	0.7	8.0	300	•	•			•		•
VN11	160, 200	3.0	2.0	300	•	•			•		•
VN12	40,60,100	0.3	20.0	600	•	•			•		•
VN12	160, 200	1.0	6.0	600	•	•			•		•
VN13	40,60,100	8.0	0.50	25		•		•		•	•
VN13	160, 200	40.0	0.25	25		•		•			•
VN21	60, 100	3.0	0.5	45						•	•
VN22	60, 100	0.3	8.0	400							•
R520[2]	100	0.3	8.0	500				•			
R521[2]	60	0.3	8.0	500				•			
R531[2]	60	0.18	12.0	600				•			

Note 1: Refer to Arrays and Special Functions section for packages available.
Note 2: TO-220 compatible lead bend available.

P-Channel DMOS Power FETs

Device Family	BV_{DSS} Min (V)	$RDS_{(ON)}$ Max (ohms)	$I_{D(ON)}$ Min (A)	C_{ISS} Typ (pf)	Package Options						
					TO-3	TO-39	TO-52	TO-92	TO-220	Quad[1]	Die
VP01	40,60,90	8.0	0.50	40		•	•	•	•	•	•
VP01	160, 200	25.0	0.35	40		•		•	•		•
VP02	40,60,100	4.0	2.0	75		•		•	•	•	•
VP02	160, 200	16.0	0.75	75		•		•	•		•
VP03	350, 400	6.0	1.5	600	•	•			•		•
VP03	450, 500	7.5	1.0	500	•	•			•		•
VP05	350, 400	75.0	0.25	45		•		•			•
VP05	450, 500	125.0	0.10	45		•		•			•
VP06	350, 400	25.0	0.40	75		•		•	•		•
VP06	450, 500	25.0	0.20	75		•		•	•		•
VP11	60, 100	2.0	5.0	325	•	•			•		•
VP11	160, 200	5.0	1.5	325	•	•			•		•
VP12	40,60,100	0.8	6.0	600	•	•			•		•
VP12	160, 200	2.5	4.0	600	•	•			•		•
VP13	40,60,100	25.0	0.25	25		•		•		•	•
VP13	160, 200	100.0	0.10	25		•		•			•
R9521[2]	60	0.6	6.0	400				•			
R9522[2]	100	0.8	5.0	400				•			
R9523[2]	60	0.8	5.0	400				•			

Note 1: Refer to Arrays and Special Functions section for packages available.
Note 2: TO-220 compatible lead bend available.

Supertex inc.

DMOS Power FETS

The following table represents an industry cross–reference for power MOSFETs. The Supertex devices are a "form, fit, and function" replacement for the industry standard part types, but subtle differences in charateriestics and/or specifications may exist.

Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number
2N6659	2N6659	2SK176	VN1220N1	AN0110NA	AN0120NA	BUZ60B	VN0340N5
2N6660	2N6660	2SK176H	VN1220N1	AN0120NA	AN0120NA	BUZ63B	VN0340N1
2N6661	2N6661	2SK196H	VN0116N2	AN0130NA	AN0130NA	BUZ72	VN1210N5
2N6755	VN1206N1	2SK213	VN0216N5	AN0140NA	AN0140NA	BUZ72A	VN1210N5
2N6756	VN1210N1	2SK214	VN0216N5	BS107P	VN1320N3	BUZ73A	VN1220N5
2N6757	VN1216N1	2SK215	VN0220N5	BS107PT	VN1320N3	BUZ74	VN0350N5
2N6757	VN1216N5	2SK216	VN0220N5	BS170	VN0106N3	BUZ74A	VN0350N5
2N6759	VN0335N1	2SK216K	VN0220N5	BS170P	VN0106N3	BUZ76	VN0340N5
2N6761	VN0345N5	2SK220	VN1216N1	BS250	VP0106N3	BUZ76A	VN0340N5
2N6761	VN0345N1	2SK221	VN1220N1	BS250P	VP0106N3	D80AK2	VN0206N3
2N7000	2N7000	2SK259	VN0335N1	BSR78	TP0604N3	D80AL2	VN0210N3
2N7000	VN0106N3	2SK260	VN0340N1	BSS100	VN0210N3	D80AM2	VN0216N3
2N7007	2N7007	2SK294	VN1210N5	BSS101	VN0120N3	D80AN2	VN0220N3
2N7008	2N7008	2SK295	VN1210N5	BSS110	VP0106N3	D84BK2	VN1206N5
2N7009	VN0550N3	2SK296	VN0335N5	BSS88	TN0524N3	D84BL2	VN1210N5
2N7014	VN1110N5	2SK298	VN0340N1	BSS89	VN0220N3	D84BM2	VN1216N5
2SJ101	VP1204N5	2SK310	VN0340N5	BSS98	VN0106N3	D84BN2	VN1220N5
2SJ102	VP1206N5	2SK311	VN0345N5	BST70A	VN0109N3	D84BQ1	VN0335N5
2SJ117	VP0340N5	2SK319	VN0340N5	BST72	VN1310N3	D84BQ2	VN0340N5
2SJ121	VP1204N5	2SK345	VN1204N5	BST72A	VN1310N2	D84CK2	VN1206N5
2SJ48	VP1216N1	2SK346	VN1206N5	BST74	VN0220N3	D84CL2	VN1210N5
2SJ49	VP1216N1	2SK382	VN0350N5	BST74A	VN0220N3	D84CM2	VN1216N5
2SJ50	VP1216N1	2SK383	VN1210N5	BST76	VN0220N3	D84CN2	VN1220N5
2SJ55	VP1220N1	2SK398	VN1210N1	BST76A	VN0220N3	D84CQ1	VN0335N5
2SJ56	VP1220N1	2SK399	VN1210N1	BUZ171	VP1206N5	D84CQ2	VN0340N5
2SJ56H	VP1220N1	2SK400	VN1220N1	BUZ172	VP1210N5	D84CR1	VN0345N5
2SJ76	VP0116N5	2SK402	VN0340N1	BUZ173	VP1220N5	D84CR2	VN0350N5
2SJ77	TP0616N5	2SK408	VN0220N5	BUZ20	VN1210N5	D84DK2	VN1206N5
2SJ78	VP1220N5	2SK409	VN0220N5	BUZ23	VN1210N1	D84DL2	VN1210N5
2SJ79	VP0120N5	2SK411	VN0360N1	BUZ30	VN1220N5	D86DK2	VN1206N1
2SJ79K	VP0120N5	2SK413	VN1216N1	BUZ33	VN1220N1	D86DL2	VN1210N1
2SK133	VN1216N1	2SK414	VN1216N1	BUZ40	VN0350N5	IRF120	VN1210N1
2SK134	VN1216N1	2SK428	VN1206N5	BUZ42	VN0350N5	IRF121	VN1206N1
2SK135	VN1216N1	2SK440	VN1220N5	BUZ43	VN0350N1	IRF122	VN1210N1
2SK175	VN1220N1	2SK441	VN0650N2	BUZ46	VN0350N1	IRF123	VN1206N1

Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number
IRF130	VN1210N1	IRF722	VN0340N5	IRFF220	VN1220N2	IVN5200TNE	VN1206N2
IRF131	VN1206N1	IRF723	VN0335N5	IRFF221	VN1216N2	IVN5200TNH	VN1210N2
IRF132	VN1210N1	IRF732	VN0340N5	IRFF222	VN1220N2	IVN5201CND	VN1204N5
IRF133	VN1206N1	IRF733	VN0335N5	IRFF223	VN1216N2	IVN5201CNE	VN1206N5
IRF220	VN1220N1	IRF820	VN0350N5	IRFF232	VN1220N2	IVN5210CNF	VN1210N5
IRF221	VN1216N1	IRF821	VN0345N5	IRFF233	VN1216N2	IVN5210CNH	VN1210N5
IRF222	VN1220N1	IRF822	VN0350N5	IRFF310	VN0340N2	IVN5210KND	VN1204N1
IRF223	VN1216N1	IRF823	VN0345N5	IRFF311	VN0335N2	IVN5210KNE	VN1206N1
IRF232	VN1220N1	IRF832	VN0350N5	IRFF312	VN0340N2	IVN5210KNF	VN1210N1
IRF233	VN1216N1	IRF833	VN0345N5	IRFF313	VN0335N2	IVN5210KNH	VN1210N1
IRF320	VN0340N1	IRF9132	VP1210N1	IRFF320	VN0340N2	IVN5210TND	VN1204N2
IRF321	VN0335N1	IRF9133	VP1206N1	IRFF321	VN0335N2	IVN5210TNE	VN1206N2
IRF322	VN0340N1	IRF9232	VP1220N1	IRFF322	VN0340N2	IVN5210TNF	VN1210N2
IRF323	VN0335N1	IRF9233	VP1216N1	IRFF323	VN0335N2	IVN5210TNH	VN1210N2
IRF332	VN0340N1	IRF9510	VP1210N5	IRFF332	VN0340N2	IVN6000CNE	VN1206N5
IRF333	VN0335N1	IRF9511	VP1206N5	IRFF333	VN0335N2	IVN6000CNF	VN1210N5
IRF420	VN0350N1	IRF9512	VP1210N5	IRFF420	VN0350N2	IVN6000CNH	TN0610N5
IRF421	VN0345N1	IRF9513	VP1206N5	IRFF421	VN0345N2	IVN6000CNR	VN0340N5
IRF422	VN0350N1	IRF9520	IRF9520	IRFF422	VN0350N2	IVN6000CNS	VN0340N5
IRF423	VN0345N1	IRF9521	IRF9521	IRFF423	VN0345N2	IVN6000CNT	VN0345N5
IRF432	VN0350N1	IRF9522	IRF9522	IRFG9113	TP0606N7	IVN6000CNU	VN0350N5
IRF433	VN0345N1	IRF9523	IRF9523	IVN5000AND	TN0104N3	IVN6000KNE	VN1206N1
IRF510	IRF510	IRF9532	VP1210N5	IVN5000AND	TN0104N3	IVN6000KNF	VN1210N1
IRF511	IRF511	IRF9533	VP1206N5	IVN5000ANE	VN0206N3	IVN6000KNH	VN1210N1
IRF512	IRF512	IRF9610	VP1220N5	IVN5000ANF	VN0210N3	IVN6000KNR	VN0340N1
IRF513	IRF513	IRF9611	VP1216N5	IVN5000ANF	VN0210N3	IVN6000KNS	VN0340N1
IRF520	IRF520	IRF9612	VP1120N5	IVN5000ANH	VN0210N3	IVN6000KNT	VN0345N1
IRF521	IRF521	IRF9613	VP1116N5	IVN5000ANH	VN0210N3	IVN6000KNU	VN0350N1
IRF522	IRF522	IRF9620	VP1220N5	IVN5000SND	VN0104N9	IVN6000TNE	TN0606N2
IRF523	IRF523	IRF9621	VP1216N5	IVN5000SND	VN0109N9	IVN6000TNF	VN0610N2
IRF530	VN1210N5	IRF9622	VP1220N5	IVN5000SNE	VN0106N9	IVN6000TNH	TN0610N2
IRF531	IRF531	IRF9623	VP1216N5	IVN5000SNF	VN0109N9	IVN6000TNR	VN0340N2
IRF532	VN1210N5	IRF9632	VP1220N5	IVN5000SNF	VN0109N9	IVN6000TNS	VN0340N2
IRF533	VN1206N5	IRF9633	VP1216N5	IVN5000SNH	VN0109N9	IVN6000TNT	VN0345N2
IRF610	VN1220N5	IRFF110	VN1210N2	IVN5000TND	TN0104N2	IVN6000TNU	VN0350N2
IRF611	VN1216N5	IRFF111	VN1206N2	IVN5000TND	TN0104N2	IVN6001CNE	VN1206N5
IRF612	VN1120N5	IRFF112	VN1110N2	IVN5000TNE	VN0206N2	IVN6001CNF	VN1210N5
IRF613	VN1216N5	IRFF113	VN1106N2	IVN5000TNF	VN0210N2	IVN6001CNH	TN0610N5
IRF620	VN1220N5	IRFF120	VN1210N2	IVN5000TNF	VN0210N2	IVN6001KNE	VN1206N1
IRF621	VN1216N5	IRFF121	VN1206N2	IVN5000TNH	VN0210N2	IVN6001KNF	VN1210N1
IRF622	VN1220N5	IRFF122	VN1210N2	IVN5000TNH	VN0210N2	IVN6001KNH	VN1210N1
IRF623	VN1216N5	IRFF123	VN1206N2	IVN5200HND	VN1204N5	IVN6001TNE	VN1206N2
IRF632	VN1220N5	IRFF130	VN1210N2	IVN5200HNE	VN1206N5	IVN6001TNF	VN1210N2
IRF633	VN1216N5	IRFF131	VN1206N2	IVN5200HNF	VN1210N5	IVN6001TNH	VN1210N2
IRF710	VN0340N5	IRFF132	VN1210N2	IVN5200HNH	VN1210N5	IVN6002CND	VN1204N5
IRF711	VN0335N5	IRFF133	VN1210N2	IVN5200KND	VN1204N5	IVN6002KND	VN1204N1
IRF712	VN0340N5	IRFF210	VN1220N2	IVN5200KNE	VN1206N5	IVN6002TND	TN0104N2
IRF713	VN0335N5	IRFF211	VN1216N2	IVN5200KNF	VN1210N5	IVN6100TNS	VN0640N2
IRF720	VN0340N5	IRFF212	VN1120N2	IVN5200KNH	VN1210N5	IVN6100TNT	VN0645N2
IRF721	VN0335N5	IRFF213	VN1216N2	IVN5200TND	VN1204N2	IVN6100TNU	VN0650N2

Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number
IVN6200ANE	VN1206N5	MTM5N18	VN1220N1	MTP8N08	VN1210N5	RFL1N10	VN1110N2
IVN6200ANF	VN1210N5	MTM5N20	VN1220N1	MTP8N10	VN1210N5	RFL1N12	VN1216N2
IVN6200ANH	VN1210N5	MTM7N12	VN1216N1	MTP8N12	VN1216N5	RFL1N15	VN1216N2
IVN6200ANM	VN1220N5	MTM7N15	VN1216N1	MTP8N15	VN1216N5	RFL1N18	VN1120N2
IVN6200ANS	VN0340N5	MTM7N18	VN1220N1	MTP8P08	VP1210N5	RFL1N20	VN1120N2
IVN6200CND	VN1204N5	MTM7N20	VN1220N1	MTP8P10	VP1210N5	RFL1P08	TP0610N2
IVN6200CNE	VN1206N5	MTM8N08	VN1210N1	PM1001L	VN0210N3	RFL1P10	TP0610N2
IVN6200CNF	VN1210N5	MTM8N10	VN1210N1	PM1002L	VN0210N3	RFL2N05	VN1106N2
IVN6200CNH	VN1210N5	MTM8N12	VN1216N1	PM1003P	VN1110N5	RFL2N06	VN1106N2
IVN6200CNM	VN1220N5	MTM8N15	VN1216N1	PM1004P	VN1110N5	RFM12N08	VN1210N1
IVN6200CNR	VN0340N5	MTM8P08	VP1210N1	PM1006M	VN1210N1	RFM12N10	VN1210N1
IVN6200CNS	VN0340N5	MTM8P10	VP1210N1	PM1006P	VN1210N5	RFM15N05	VN1206N1
IVN6200CNU	VN0350N5	MTP10N05	VN1206N5	PM1010M	VN1210N1	RFM15N06	VN1206N1
IVN6200KNE	VN1206N1	MTP10N06	VN1206N5	PM1010P	VN1210N5	RFM3N45	VN0345N1
IVN6200KNH	VN1210N1	MTP10N08	VN1210N5	PM1201L	VN0216N3	RFM3N50	VN0350N1
IVN6200KNM	VN1220N1	MTP10N10	VN1210N5	PM1203P	VN1216N5	RFM4N35	VN0335N1
IVN6200KNR	VN0340N1	MTP12N05	VN1206N5	PM1206P	VN1216N5	RFM4N40	VN0340N1
IVN6200KNS	VN0340N1	MTP12N06	VN1206N5	PM1503P	VN1216N5	RFM6P08	VP1210N1
IVN6200KNU	VN0350N1	MTP12N08	VN1210N5	PM1504P	VN1216N5	RFM6P10	VP1210N1
IVN6300ANE	VN1306N3	MTP12N10	VN1210N5	PM1506M	VN1216N1	RFM8N18	VN1220N1
IVN6300ANF	VN1310N3	MTP15N05	VN1206N5	PM1506P	VN1216N5	RFM8N20	VN1220N1
IVN6300ANH	VN0210N3	MTP15N06	VN1206N5	PM503L	TN0606N3	RFM8P08	VP1210N1
IVN6300ANM	VN1320N3	MTP1N45	VN0645N5	PM506L	TN0606N3	RFM8P10	VP1210N1
IVN6300ANP	VN0635N3	MTP1N50	VN0350N5	PM509P	VN1206N5	RFP12N08	VN1210N5
IVN6300ANS	VN0540N3	MTP1N55	VN0355N5	PM510P	VN1206N5	RFP12N10	VN1210N5
IVN6300ANT	VN0545N3	MTP1N60	VN0360N5	PM512M	VN1206N1	RFP15N05	VN1206N5
IVN6300ANU	VN0545N3	MTP20N08	VN1210N5	PM512P	VN1206N5	RFP15N06	VN1206N5
IVN6300SNE	VN0106N9	MTP20N10	VN1210N5	PM601L	VN0106N3	RFP1N35	VN0635N5
IVN6300SNF	VN0109N9	MTP2N18	VN1220N5	PM602L	TN0606N3	RFP1N40	VN0640N5
IVN6300SNH	VN0109N9	MTP2N20	VN1220N5	PM603L	VN0206N3	RFP2N08	TN0610N5
IVN6660	VN0106N2	MTP2N35	VN0335N5	PM604P	VN1106N5	RFP2N10	VN1110N5
IVN6661	VN0109N2	MTP2N40	VN0340N5	PM605P	VN1206N5	RFP2N12	VN1216N5
MTM10N05	VN1206N1	MTP2N45	VN0345N5	PM606L	TN0606N3	RFP2N15	VN1216N5
MTM10N06	VN1206N1	MTP2N50	VN0350N5	PM608M	VN1206N1	RFP2N18	VN1120N5
MTM10N08	VN1210N1	MTP2P45	VN0345N5	PM608P	VN1206N5	RFP2N20	VN1120N5
MTM10N10	VN1210N1	MTP2P50	VN0350N5	PM609P	VN1206N5	RFP2P08	TP0610N5
MTM12N05	VN1206N1	MTP3N12	VN1216N5	PM609R	VN1206N5	RFP2P10	TP0610N5
MTM12N06	VN1206N1	MTP3N15	VN1216N5	PM610P	VN1206N5	RFP3N45	VN0345N5
MTM12N08	VN1210N1	MTP3N35	VN0335N1	PM612M	VN1206N1	RFP3N50	VN0350N5
MTM12N10	VN1210N1	MTP3N40	VN0340N5	PM612P	VN1206N5	RFP4N05	VN1106N5
MTM15N05	VN1206N1	MTP4N08	VN1110N5	PM614M	VN1206N1	RFP4N06	VN1106N5
MTM15N06	VN1206N1	MTP4N10	VN1110N5	PM614P	VN1206N5	RFP4N35	VN0335N5
MTM20N08	VN1210N1	MTP5N05	VN1106N5	PM801L	VN0109N3	RFP4N40	VN0340N5
MTM20N10	VN1210N1	MTP5N06	VN1206N5	PM802L	TN0610N3	RFP6P08	VP1210N5
MTM2N45	VN0345N1	MTP5N18	VN1220N5	PM805P	VN1210N5	RFP6P10	VP1210N5
MTM2N50	VN0350N1	MTP5N20	VN1220N1	PM808M	VN1210N1	RFP8N18	VN1220N5
MTM2P45	VP0345N1	MTP7N12	VN1216N5	PM808P	VN1210N5	RFP8N20	VN1220N5
MTM2P50	VP0350N1	MTP7N15	VN1216N5	PM814M	VN1210N1	RFP8P08	VP1210N5
MTM3N35	VN0335N1	MTP7N18	VN1220N5	PM814P	VN1210N5	RFP8P10	VP1210N5
MTM3N40	VN0340N1	MTP7N20	VN1220N5	RFL1N08	TN0610N2	SD1100HD	VN0545N2

Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number
SD1101BD	VN0640N3	SGSP311	VN1210N5	UFN423	VN0345N1	UFNF122	VN1210N2
SD1101HD	VN0640N2	SGSP312	VN1210N5	UFN432	VN0350N1	UFNF123	VN1206N2
SD1102BD	VN0635N3	SGSP317	VN1220N5	UFN433	VN0345N1	UFNF130	VN1210N2
SD1102BD	VN0635N3	SGSP318	VN0355N5	UFN441	VN1106N1	UFNF131	VN1206N2
SD1102HD	VN0635N2	SGSP319	VN0350N5	UFN510	VN1210N5	UFNF132	VN1210N2
SD1104BD	VN0210N3	SGSP330	VN0345N5	UFN511	VN1206N5	UFNF133	VN1206N2
SD1104DD	VN0109N9	SGSP331	VN0340N5	UFN512	VN1110N5	UFNF210	VN1220N2
SD1104HD	VN0210N2	SGSP351	VN1210N5	UFN513	VN1106N5	UFNF211	VN1216N2
SD1105BD	VN0210N3	SGSP352	VN1210N5	UFN520	VN1210N5	UFNF212	VN1110N2
SD1105DD	VN0109N9	SGSP354	VN0345N5	UFN521	VN1206N5	UFNF213	VN1216N2
SD1105HD	VN0210N2	SGSP355	VN0340N5	UFN522	VN1210N5	UFNF220	VN1220N2
SD1106AD	VN0106N3	SGSP367	VN1220N5	UFN523	VN1206N5	UFNF221	VN1216N2
SD1106AD	VN0106N3	SGSP511	VN1210N1	UFN530	VN1210N5	UFNF222	VN1220N2
SD1106DD	VN0106N9	SGSP512	VN1210N1	UFN531	VN1206N5	UFNF223	VN1216N2
SD1107BD	VN0210N3	SGSP517	VN1220N1	UFN532	VN1210N5	UFNF232	VN1220N2
SD1107BD	VN0210N3	SGSP519	VN0350N1	UFN533	VN1206N5	UFNF233	VN1216N2
SD1107DD	VN0109N9	SGSP530	VN0345N1	UFN610	VN1220N5	UFNF310	VN0340N2
SD1107HD	VN0210N2	SGSP531	VN0340N1	UFN611	VN1216N5	UFNF311	VN0335N2
SD1107N	VN0210N6	SGSP579	VN1106N1	UFN612	VN1110N5	UFND312	VN0340N2
SD1112BD	VN0220N3	SN0120NB	AN0120NB	UFN613	VN1216N5	UFNF313	VN0335N2
SD1112BD	VN0220N3	SN0130NB	AN0130NB	UFN620	VN1220N5	UFNF320	VN0340N2
SD1112HD	VN0220N2	SN0140NB	AN0140NB	UFN621	VN1216N5	UFNF321	VN0335N2
SD1113BD	VN0120N3	TN0106N3	VN0106N3	UFN622	VN1220N5	UFNF322	VN0340N2
SD1113BD	VN0120N3	TN0110N3	VN0210N3	UFN623	VN1216N5	UFNF323	VN0335N2
SD1113HD	VN0120N2	TZ402BD	VN1304N3	UFN632	VN1220N5	UFNF332	VN0340N2
SD1114BD	VN0109N3	TZ403BD	VN1304N3	UFN633	VN1216N5	UFNF333	VN0335N2
SD1114DD	VN0109N9	TZ404BD	VN1304N3	UFN710	VN0340N5	UFNF420	VN0350N2
SD1114HD	VN0109N2	UFN120	VN1210N1	UFN711	VN0335N5	UFNF421	VN0345N2
SD1115BD	VN0109N3	UFN121	VN1206N1	UFN712	VN0340N5	UFNF422	VN0350N2
SD1115DD	VN0109N9	UFN122	VN1210N1	UFN713	VN0335N5	UFNF423	VN0345N2
SD1115HD	VN0109N2	UFN123	VN1206N1	UFN720	VN0340N5	UFNF432	VN0350N2
SD1117BD	VN0206N3	UFN130	VN1210N1	UFN721	VN0335N5	UFNF433	VN0345N2
SD1117DD	VN0106N9	UFN131	VN1206N1	UFN722	VN0340N5	VN01000A	VN1210N1
SD1117HD	VN0206N2	UFN132	VN1210N1	UFN723	VN0335N5	VN01000D	VN1210N5
SD1117N	VN0206N6	UFN133	VN1206N1	UFN732	VN0340N5	VN0104N3	VN0104N3
SD1122BD	VN0120N3	UFN220	VN1220N1	UFN733	VN0335N5	VN0106N3	VN0106N3
SD1122BD	VN1320N3	UFN221	VN1216N1	UFN820	VN0350N5	VN0109N3	VN0109N3
SD1124BD	VN0106N3	UFN222	VN1220N1	UFN821	VN0345N5	VN0300B	VN0300B
SD1124BD	VN0106N3	UFN223	VN1216N1	UFN822	VN0350N5	VN0300D	VN0300D
SD1127BD	VN0106N3	UFN232	VN1220N1	UFN823	VN0345N5	VN0300L	VN0300L
SD1137BD	VN0206N3	UFN233	VN1216N1	UFN832	VN0350N5	VN0300M	VN0300L
SD1202BD	VN1320N3	UFN320	VN0340N1	UFN833	VN0345N5	VN0400A	VN1204N1
SD1202BD	VN1320N3	UFN321	VN0335N1	UFNA11	TN0606N3	VN0401A	VN1204N1
SD1500BD	VN0660N3	UFN322	VN0340N1	UFNA12	TN0610N3	VN0401D	VN1204N5
SD1501BD	VN0655N3	UFN323	VN0335N1	UFNF110	VN1210N2	VN0601A	VN1206N1
SD5101N	VN1304N6	UFN332	VN0340N1	UFNF111	VN1206N2	VN0601D	VN1206N5
SGSP111	VN1210N2	UFN333	VN0335N1	UFNF112	VN1110N2	VN060M	VN0606L
SGSP112	VN1210N2	UFN420	VN0350N1	UFNF113	VN1106N2	VN0610LL	VN0610LL
SGSP151	VN1210N2	UFN421	VN0345N1	UFNF120	VN1210N2	VN0800A	VN1210N1
SGSP152	VN1210N2	UFN422	VN0350N1	UFNF121	VN1206N2	VN0800D	VN1210N5

Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number
VN0801A	VN1210N1	VN46AD	VN0104N5	ZVN0104B	VN0104N2	ZVN0210M	VN1110N1
VN0801D	VN1210N5	VN5002A	VN0350N1	ZVN0104L	VN0104N5	ZVN0214B	VN0216N2
VN0808M	VN0808L	VN5002D	VN0350N5	ZVN0106A	VN0106N3	ZVN0214L	VN1216N5
VN1001A	VN1210N1	VN6035L	VN6035L	ZVN0106B	VN0106N2	ZVN0214M	VN1116N1
VN10KE	VN0106N9	VN64GA	VN1206N1	ZVN0106L	VN0106N5	ZVN0216B	VN0216N2
VN10KM	VN10KN3	VN66AD	VN0106N5	ZVN0108A	VN0109N3	ZVN0216L	VN0216N5
VN10KMA	VN10KN3	VN66AK	VN0106N2	ZVN0108B	VN0109N2	ZVN0216M	VN0216N1
VN10KN3	VN10KN3	VN67AA	VN0106N5	ZVN0108L	VN0109N5	ZVN0220B	VN0220N2
VN10LE	VN0106N9	VN67AB	VN0106N2	ZVN0109A	VN0109N3	ZVN0220L	VN0220N5
VN10LM	VN10KN3	VN67ABA	VN0106N2	ZVN0109A	VN0109N3	ZVN02A2B	TN0602N2
VN10LM	VN10KN3	VN67AD	VN0106N5	ZVN0109B	VN0109N2	ZVN02A2L	VN0300D
VN10LP	VN1306N3	VN67AK	VN0106N2	ZVN0109L	VN0109N5	ZVN02A2M	VN1106N1
VN1206B	VN1206B	VN88AD	VN0109N5	ZVN0110A	VN1310N3	ZVN02A3B	TN0604N2
VN1206D	VN1206D	VN89ABA	VN0109N2	ZVN0110B	VN1310N2	ZVN02A3L	VN0300D
VN1206L	VN1206L	VN89AD	VN0109N5	ZVN0110L	VN0210N5	ZVN02A3M	VN1106N1
VN1206M	VN1206L	VN90AA	VN1110N1	ZVN0114A	VN0216N3	ZVN0330B	VN0335N2
VN1210L	VN1210L	VN90AB	VN0109N2	ZVN0114B	VN0216N2	ZVN0330L	VN0335N5
VN1210M	VN1210L	VN90ABA	VN0109N2	ZVN0114L	VN0216N5	ZVN0330M	VN0335N1
VN1216B	VN1216N2	VN98AK	VN0109N2	ZVN0116A	VN0116N3	ZVN0335B	VN0335N2
		VN99AB	VN0109N2	ZVN0116B	VN0116N2	ZVN0335L	VN0335N5
VN1706B	VN1706B						
VN1706D	VN1706D	VN99AK	VN0109N2	ZVN0116L	VN0115N5	ZVN0335M	VN0335N1
VN1706L	VN1706L	VP0104N3	VP0104N3	ZVN0117TA	VN0120N3	ZVN0340B	VN0340N2
VN1706M	VN1706L	VP0106N3	VP0106N3	ZVN0120A	VN0120N3	ZVN0340L	VN0340N5
VN1710L	VN1710L	VP0109N3	VP0109N3	ZVN0120A	VN0120N3	ZVN0340M	VN0340N1
VN1710M	VN1710L	VP0300B	VP0300B	ZVN0120B	VN0120N2	ZVN0345B	VN0345N2
VN2010L	VN2010L	VP0300L	VP0300L	ZVN0120B	VN0120N2	ZVN0345L	VN0345N5
VN2222KM	VN1306N3	VP0300M	VP0300L	ZVN0120L	VN0120N5	ZVN0345M	VN0345N1
VN2222L	VN2222LL	VP0540L	VP0640N5	ZVN0120L	VN0120N5	ZVN0350L	VN0350N5
VN2222LL	VN2222LL	VP0808B	VP080B	ZVN0124A	TN0524N3	ZVN0350M	VN0350N1
VN2222LM	VN1306N3	VP0808L	VP0808L	ZVN0124B	TN0524N2	ZVN0355B	VN0355N2
VN2222LM	VN1306N3	VP0808M	VP0808L	ZVN0124L	TN0624N5	ZVN0355L	VN0355N5
VN2406B	VN2406B	VP1008B	TP0610N2	ZVN01A2A	TN0102N3	ZVN0355M	VN0355N1
VN2406D	VN2406D	VP1008M	TP0610N3	ZVN01A2B	TN0602N2	ZVN0360B	VN0360N2
VN2406L	VN2406L	VQ1000J	VQ1000N6	ZVN01A2L	VN0300D	ZVN0360L	VN0360N5
VN2406M	VN2406L	VQ1000P	VQ1000N7	ZVN01A3B	TN0604N2	ZVN0360M	VN0360N1
VN2410L	VN2410L	VQ1001J	TN0606N6	ZVN01A3L	VN0204N5	ZVN0450M	VN0350N1
VN2410M	VN2410L	VQ1001P	VQ1001P	ZVN0204B	TN0104N2	ZVN0530A	VN0535N3
VN30ABA	VN0104N2	VQ1004J	VQ1004J	ZVN0204L	VN0204N5	ZVN0530B	VN0535N2
VN3501A	VN0335N1	VQ1004P	VQ1004P	ZVN0204M	VN120N1	ZVN0535A	VN0535N3
VN3501D	VN0335N5	VQ2001J	TP0604N6	ZVN0206B	VN0206N2	ZVN0535A	VN0635N3
VN3515L	VN3515L	VQ2001P	TP0604N6	ZVN0206L	VN0206N5	ZVN0535B	VN0635N2
VN35AA	VN1106N1	VQ2004J	TP0606N6	ZVN0206M	VN1106N1	ZVN0535L	VN0635N5
VN35AB	VN0204N2	VQ2004P	TP0606N7	ZVN0208B	VN0210N2	ZVN0540A	VN0540N3
VN35AK	VN0204N2	VQ2006J	TP0606N6	ZVN0208L	VN0210N5	ZVN0540B	VN0540N2
VN4001A	VN0340N1	VQ2006P	TP0606N7	ZVN0208M	VN1110N1	ZVN0540L	VN0640N5
VN4001D	VN0340N5	VQ3001J	VQ3001N6	ZVN0209B	TN0610N2	ZVN0545A	VN0545N3
VN4012L	VN4012L	VQ3001P	VQ3001N7	ZVN0209L	TN0610N5	ZVN0545B	VN0545N2
VN40AD	VN0104N5	VQ7254J	VQ7254N6	ZVN0209M	VN1110N1	ZVN0545L	VN0645N5
VN4502A	VN0345N1	VQ7254P	VQ7254N7	ZVN0210B	VN0210N2	ZVN1104B	TN0604N2
VN4502D	VN0345N5	ZVN0104A	VN0104N3	ZVN0210L	VN0210N5	ZVN1104L	VN1106N5

Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number
ZVN1104M	VN1106N1	ZVN1206M	VN1206N1	ZVN1408B	VN1310N2	ZVP0120L	VP0120N5
ZVN1106B	VN1106N2	ZVN1208B	VN1210N2	ZVN1409A	VN1310N3	ZVP0535A	VP0535N3
ZVN1106L	VN1106N5	ZVN1208L	VN1210N5	ZVN1409A	VN1310N3	ZVP0535B	VP0535N2
ZVN1106M	VN1106N1	ZVN1208M	VN1210N1	ZVN1409B	VN1310N2	ZVP0535L	VP0635N5
ZVN1108B	VN1110N2	ZVN1209B	VN1210N2	ZVN1410A	VN1310N3	ZVP0540A	VP0540N3
ZVN1108L	VN1110N5	ZVN1209L	VN1210N5	ZVN1410B	VN1310N2	ZVP0540B	VP0540N2
ZVN1108M	VN1110N1	ZVN1209M	VN1210N1	ZVN1414A	VN1316N3	ZVP0545A	VP0545N3
ZVN1109B	VN1110N2	ZVN1210B	VN1110N2	ZVN1414B	VN1316N2	ZVP0545B	VP0545N2
ZVN1109L	VN1110N5	ZVN1210L	VN1110N5	ZVN1416A	VN1316N3	ZVP0545L	VP0645N5
ZVN1109M	VN1110N1	ZVN1210M	VN1110N1	ZVN1416B	VN1316N2	ZVP1320A	VP1320N3
ZVN1110B	VN0210N2	ZVN1214B	VN1216N5	ZVN1420A	VN0120N3	ZVP1320B	VP1320N2
ZVN1110L	VN0210N5	ZVN1214B	VN1216N2	ZVN1420B	VN0120N2	ZVP2106A	TP0606N3
ZVN1110M	VN1110N1	ZVN1214L	VN1216N5	ZVN2106A	VN0206N3	ZVP2106B	TP0606N2
ZVN1114B	VN1216N2	ZVN1214M	VN1216N1	ZVN2106B	VN0206N2	ZVP2106L	TP0606N5
ZVN1114L	VN1216N5	ZVN1216L	VN1216N5	ZVN2106L	VN0206N5	ZVP2110A	VP0109N3
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ZVN1116L	VN0216N5	ZVN1220L	VN1220N5	ZVN2110L	VN0210N5	ZVP2120A	VP0120N3
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ZVN1120B	VN1120N2	ZVN12A2B	VN1204N2	ZVN2120B	VN0120N2	ZVP2120L	VP0120N5
ZVN1120L	VN1120N5	ZVN12A2M	VN1204N1	ZVN2120L	VN0120N5	ZVP2206B	VP1206N2
ZVN1120M	VN1120N1	ZVN12A3B	VN1204N2	ZVN2206B	VN1206N2	ZVP2206L	VP1206N5
ZVN1130B	VN0335N2	ZVN12A3L	VN1204N5	ZVN2206L	VN1206N5	ZVP2210B	VP1110N2
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ZVN1135M	VN0335N1	ZVN1306B	VN1306N2	ZVN2224B	TN0624N2	ZVP3306B	VP0106N2
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ZVN1140L	VN0340N5	ZVN1308B	VN1310N2	ZVN2535A	VN0535N3	ZVP3310B	VP1310N2
ZVN1140M	VN0340N1	ZVN1309A	VN1310N3	ZVN2535B	VN0535N2		
ZVN1145B	VN0345N2	ZVN1309B	VN1310N2	ZVN2535L	VN0535N5		
ZVN1145L	VN0345N5	ZVN1310A	VN1310N3	ZVN3210L	VN1210N5		
ZVN1145M	VN0345N1	ZVN1310B	VN1310N2	ZVN3220L	VN1220N5		
ZVN11A2B	VN1204N2	ZVN1314A	VN0116N2	ZVN3306A	VN0106N3		
ZVN11A2L	VN1204N5	ZVN1314B	VN0116N2	ZVN3306B	VN0106N2		
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ZVN11A3B	VN1204N2	ZVN1316B	VN1316N2	ZVN3310B	VN1310N2		
ZVN11A3L	VN1204N5	ZVN1320A	VN1320N3	ZVN3320A	VN1320N3		
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ZVN1204L	VN1204N5	ZVN1404B	VN1304N2	ZVNL120A	VN0120N3		
ZVN1204M	VN1204N1	ZVN1406A	VN1306N3	ZVNL535A	VN0535N3		
ZVN1206B	VN1206N2	ZVN1406B	VN1306N2	ZVP0120A	VP0120N3		
ZVN1206L	VN1206N5	ZVN1408A	VN1310N3	ZVP0120B	VP0120N2		

Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package		
				TO-39	TO-92	DICE
60V	3Ω	2A	1.6V	TN0106N2	TN0106N3	TN0106ND
100V	3Ω	2A	1.6V	TN0110N2	TN0110N3	TN0110ND

Features

- ☐ Low threshold
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Freedom from secondary breakdown
- ☐ Low input and output leakage

Advanced DMOS Technology

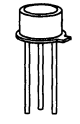
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

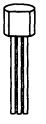
Applications

- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switch
- ☐ General purpose line driver

Package Options (Notes 1 and 2)



TO-39



TO-92

Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-92	0.5A	2.0A	1.0W	170	125	1.0A	4.0A
TO-39	0.8A	2.5A	3.5W	125	35	2.5A	5.0A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

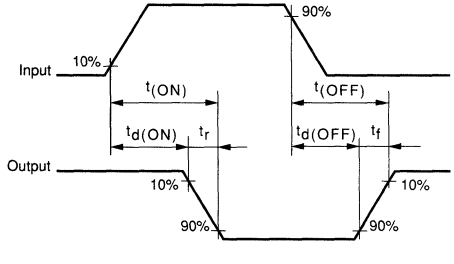
(Notes 1 and 2)

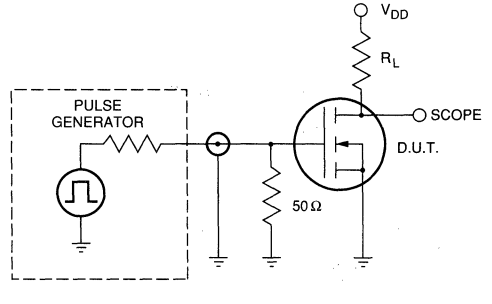
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0110	100			V	I_D = 1mA, V_{GS} = 0
		TN0106	60				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	V_{GS} = V_{DS}, I_D = 0.5mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.2	-5.0	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	V_{GS} = 0, V_{DS} = Max Rating
					500		V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		0.75	1.5		A	V_{GS} = 5V, V_{DS} = 25V
			2.0	3.5			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			2.5	4.5	Ω	V_{GS} = 5V, I_D = 250mA
				2.0	3.0		V_{GS} = 10V, I_D = 500mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.6	1.1	%/°C	I_D = 0.5A, V_{GS} = 10V
G_{FS}	Forward Transconductance		225	400		m℧	V_{DS} = 25V, I_D = 500mA
C_{ISS}	Input Capacitance			50	60	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			25	35		
C_{RSS}	Reverse Transfer Capacitance			4	8		
$t_{d(ON)}$	Turn-ON Delay Time			2	5	ns	V_{DD} = 25V, I_D = 1.0A, R_S = 50Ω
t_r	Rise Time			3	5		
$t_{d(OFF)}$	Turn-OFF Delay Time			6	7		
t_f	Fall Time			3	5		
V_{SD}	Diode Forward Voltage Drop			1	1.5	V	I_{SD} = 0.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			400		ns	I_{SD} = 0.5A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

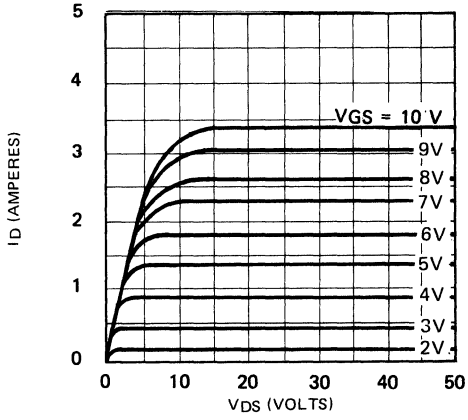
Switching Waveforms and Test Circuit



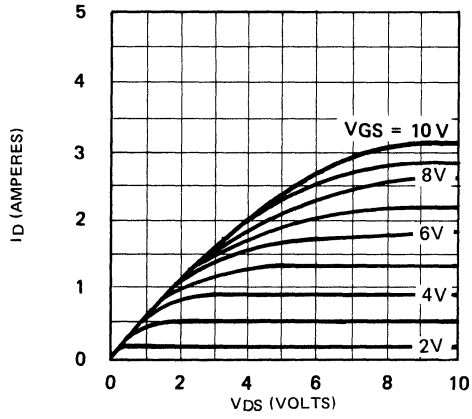


Typical Performance Curves

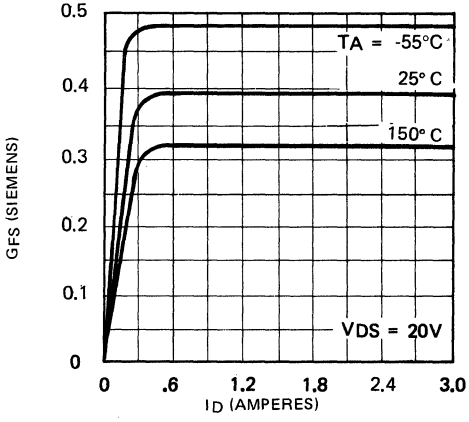
Output Characteristics



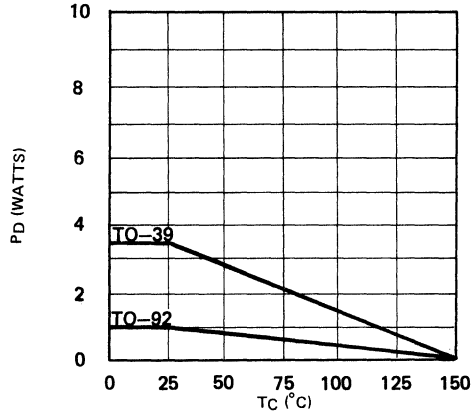
Saturation Characteristics



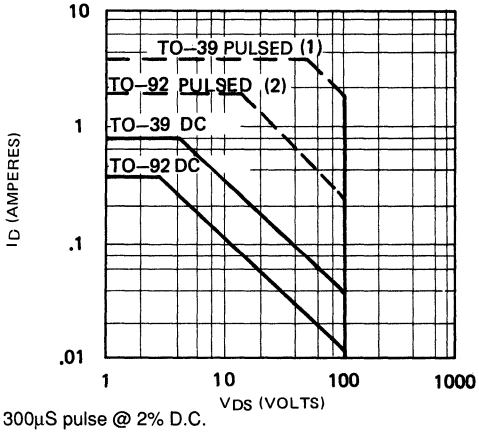
Transconductance Vs. Drain Current



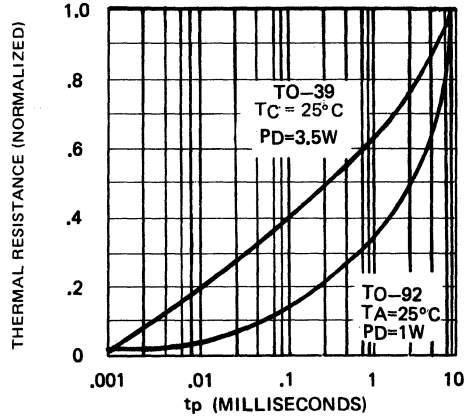
Power Dissipation Vs. Case Temperature



Maximum Rated Safe Operating Area



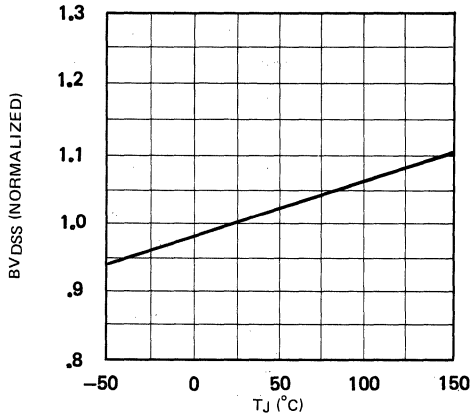
Thermal Response Characteristics



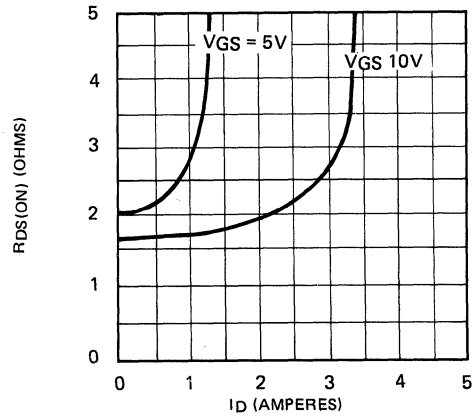
(1) 300μS pulse @ 2% D.C.
(2) 10μS pulse @ 2% D.C.

Typical Performance Curves

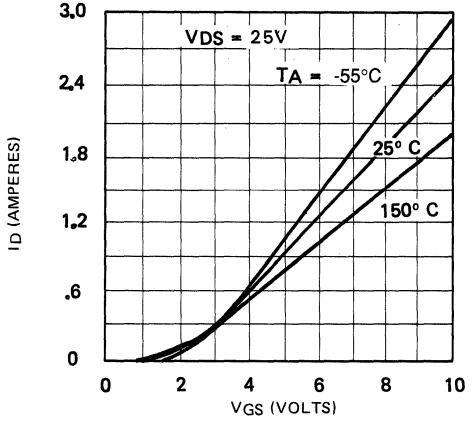
BVDSS Variation with Temperature



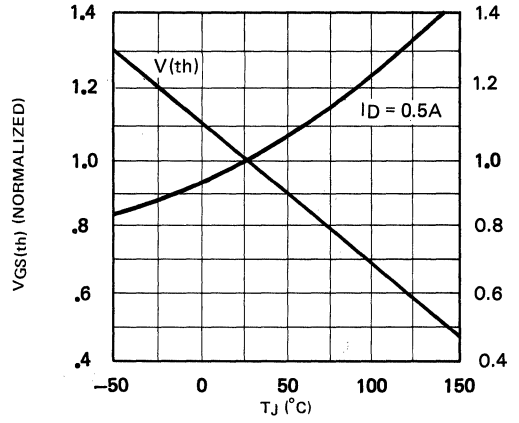
ON - Resistance Vs. Drain Current



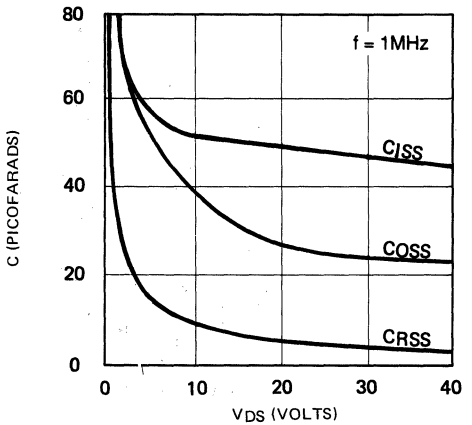
Transfer Characteristics



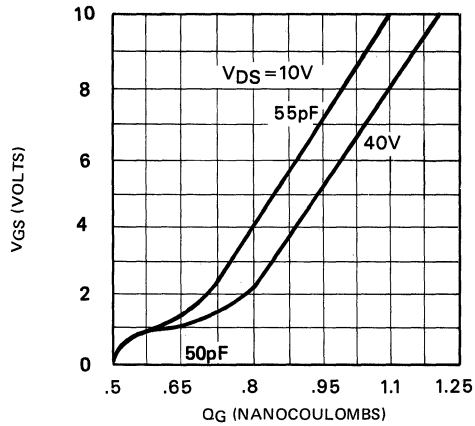
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	DICE
20V	1.8Ω	2.0A	TN0102N2	TN0102N3	TN0102ND
40V	1.8Ω	2.0A	TN0104N2	TN0104N3	TN0104ND

Features

- ☐ Low threshold
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Freedom from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Advanced DMOS Technology

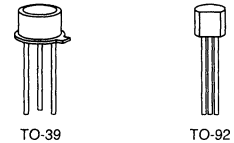
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Logic level interface
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switch
- ☐ General purpose line driver

Package Options (Note 1)



TO-39 TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	1.25A	2.90A	3.5W	125	35	1.25A	2.90A
TO-92	0.80A	2.40A	1.0W	170	125	0.80A	2.40A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

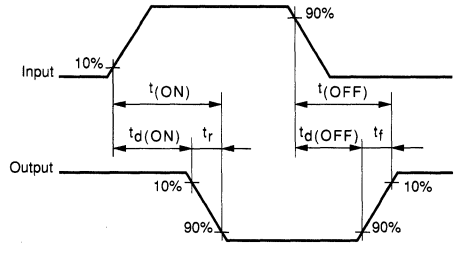
(Notes 1 and 2)

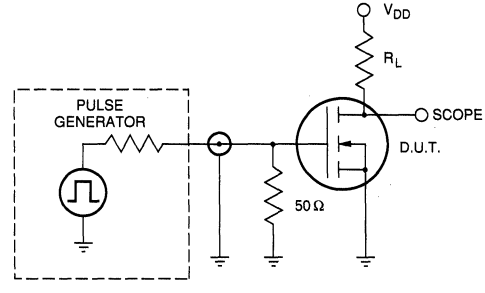
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0104	40			V	V_{GS} = 0, I_D = 1.0mA
		TN0102	20				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	V_{GS} = V_{DS}, I_D = 500µA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.0	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate Body Leakage			0.1	100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				1	µA	V_{GS} = 0, V_{DS} = Max Rating
					100	µA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			0.5		A	V_{GS} = 3V, V_{DS} = 25V
			0.5	0.8			V_{GS} = 5V, V_{DS} = 25V
			2.0	2.8			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5.0		Ω	V_{GS} = 3V, I_D = 50mA
				2.3	2.5		V_{GS} = 5V, I_D = 250mA
				1.5	1.8		V_{GS} = 10V, I_D = 1A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.7	1.0	%/°C	I_D = 1A, V_{GS} = 10V
G_{FS}	Forward Transconductance		0.34	0.45		℧	V_{DS} = 25V, I_D = 0.5A
C_{ISS}	Input Capacitance			45	60	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			20	25		
C_{RSS}	Reverse Transfer Capacitance			2	5		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	V_{DD} = 25V, I_D = 1A, R_S = 50Ω
t_r	Rise Time			7	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			6	9		
t_f	Fall Time			5	8		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	I_{SD} = 2.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			300		ns	I_{SD} = 1A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

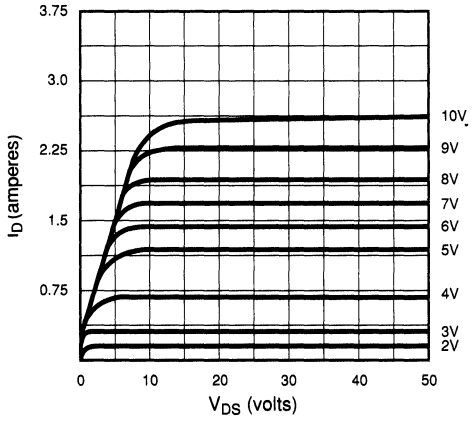
Switching Waveforms and Test Circuit



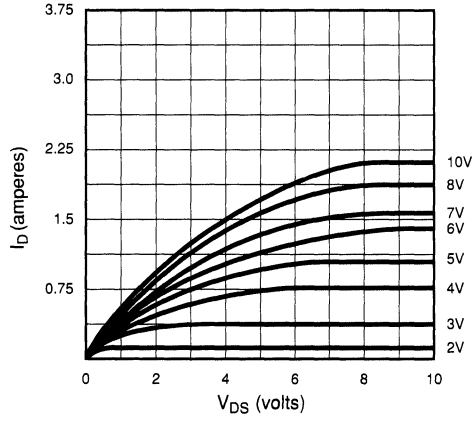


Typical Performance Curves

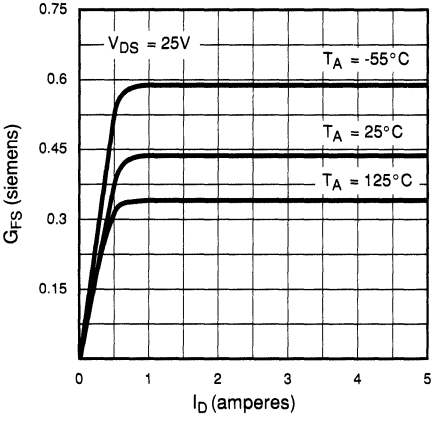
Output Characteristics



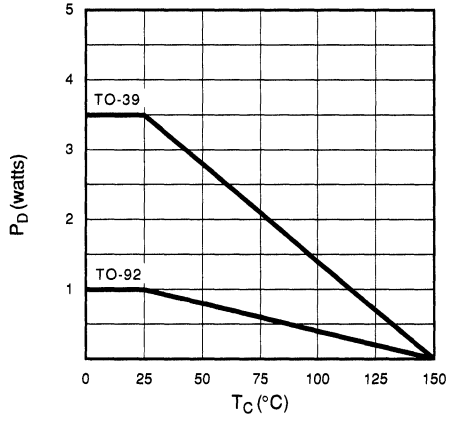
Saturation Characteristics



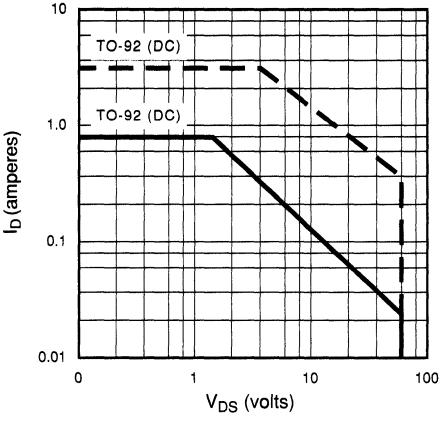
Transconductance vs. Drain Current



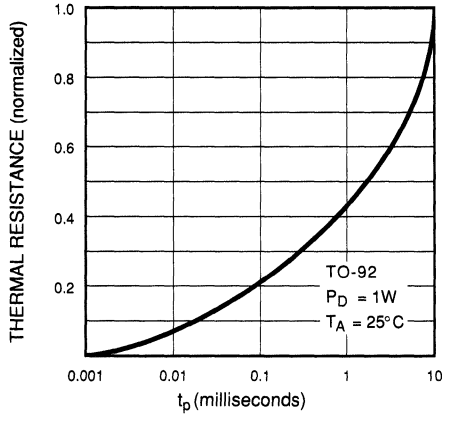
Power Dissipation vs. Case Temperature



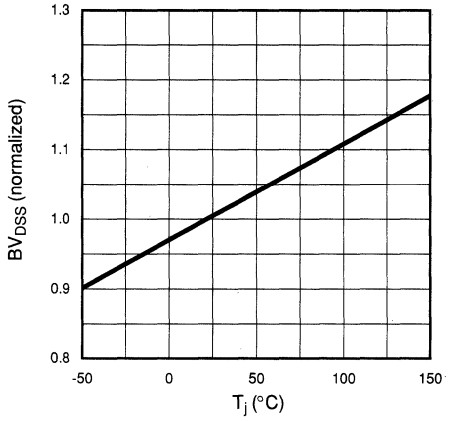
Maximum Rated Safe Operating Area



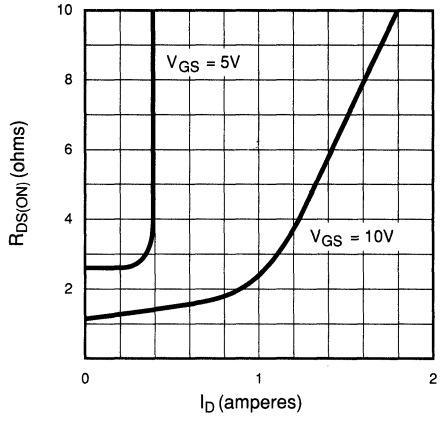
Thermal Response Characteristics



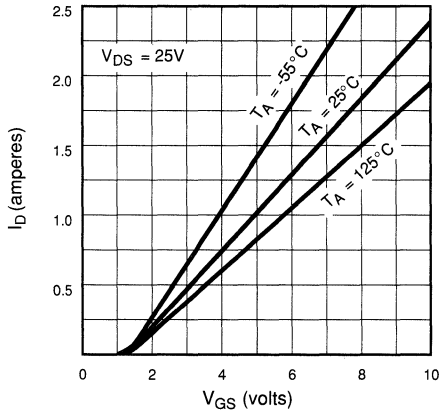
BV_{DSS} Variation with Temperature



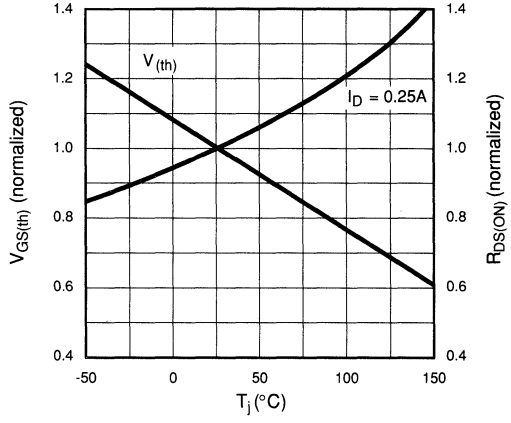
On-Resistance vs. Drain Current



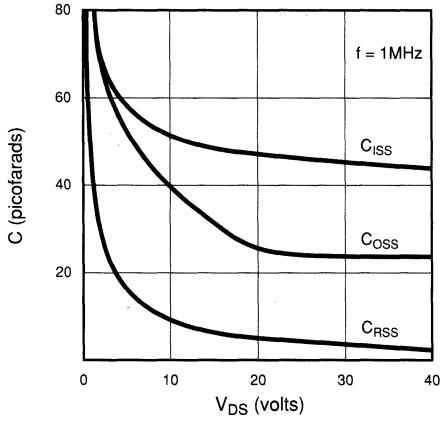
Transfer Characteristics



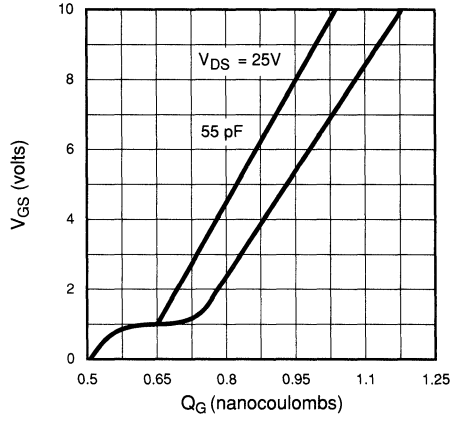
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
20V	1.0Ω	4.0A	TN0202N2	TN0202N3
40V	1.0Ω	4.0A	TN0204N2	TN0204N3

Features

- ☐ Low threshold
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Freedom from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Logic level interface
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switch
- ☐ General purpose line driver

Package Options

(Note 1)

TO-39 TO-92

Note 1: See Package Outline section for discrete pinouts.

Ratings and Characteristics

TN02L not recommended for new designs. Refer to TN06L data sheet for all ratings and characteristics.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package		
				TO-39	TO-92	DICE
200V	10Ω	300mA	1.5V	TN0520N2	TN0520N3	TN0520ND
240V	10Ω	300mA	1.5V	TN0524N2	TN0524N3	TN0524ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Very low threshold voltage

Advanced DMOS Technology

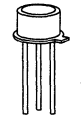
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Telecommunications: Outpulsing switch
  Muting switch
- ☐ Battery operated systems
- ☐ Solid state relays

Package Options (Notes 1 and 2)



TO-39

TO-92

Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	0.7A	1.5A	3.5W	35	125	0.7A	1.5A
TO-92	0.3A	1.0A	1.0W	125	170	0.3A	1.0A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

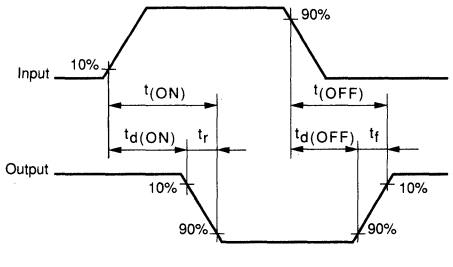
(Notes 1 and 2)

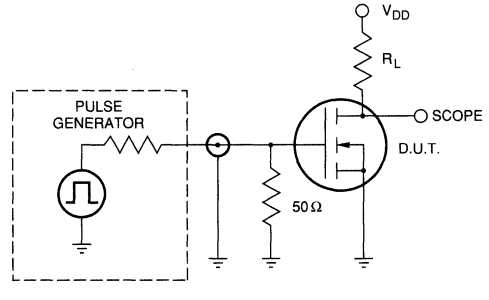
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0524	240			V	V_{GS}= 0, I_D =1mA
		TN0520	200				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.5	V	V_{GS} = V_{DS}, I_D = 1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.0	-4.0	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	V_{GS} = 0, V_{DS} = Max Rating
					500		V_{DS} = 0, V_{GS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		100	390		mA	V_{GS} = 3V, V_{DS} = 25V
			300	800			V_{GS} = 5V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			9	15	Ω	V_{GS} = 3V, I_D = 50mA
				7	10		V_{GS} = 5V, I_D = 100mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.9	1.5	%/°C	V_{GS} = 5V, I_D = 0.2A
G_{FS}	Forward Transconductance		0.15	0.3		℧	V_{DS} = 25V, I_D = 0.2A
C_{ISS}	Input Capacitance			45	60	pF	V_{GS} = 0, V_{DS} = 25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			15	35		
C_{RSS}	Reverse Transfer Capacitance			3	8		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	V_{DD} = 25V I_D = 0.2A R_S = 50Ω
t_r	Rise Time			3	5		
$t_{d(OFF)}$	Turn-OFF Delay Time			5	7		
t_f	Fall Time			3	5		
V_{SD}	Diode Forward Voltage Drop			1.1	2.5	V	V_{GS} = 0, I_{SD} = 100mA
t_{rr}	Reverse Recovery Time			400		ns	V_{GS} = 0, I_{SD} = 100mA

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

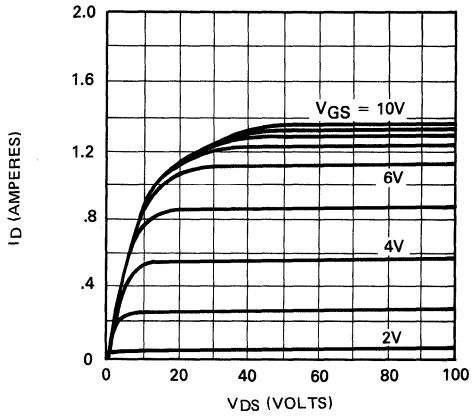
Switching Waveforms and Test Circuit



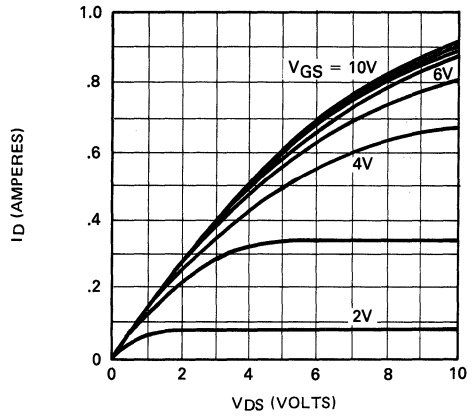


Typical Performance Curves

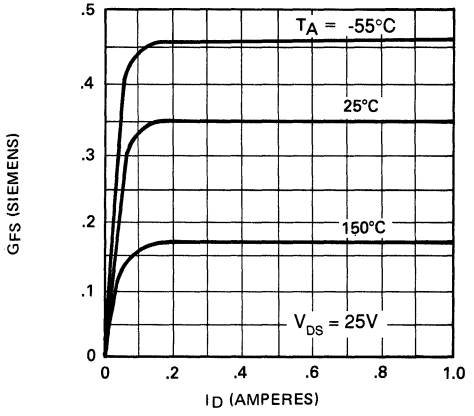
Output Characteristics



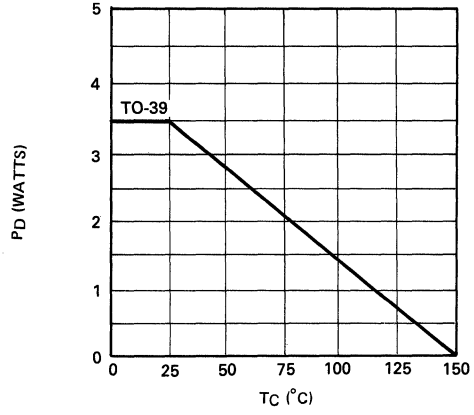
Saturation Characteristics



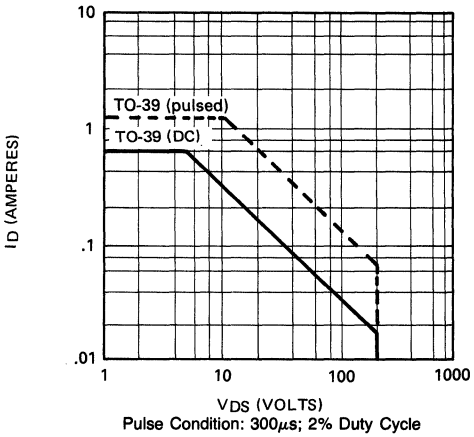
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

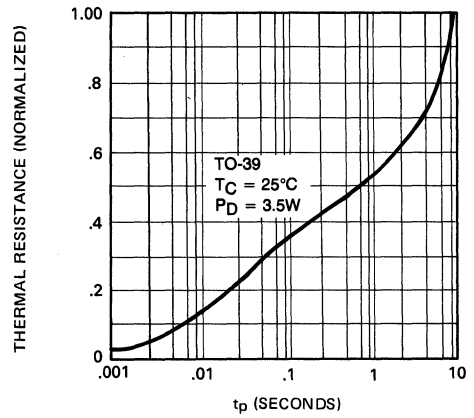


Maximum Rated Safe Operating Area



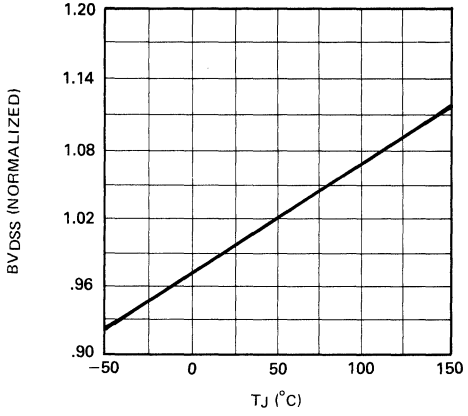
Pulse Condition: 300μs; 2% Duty Cycle

Thermal Response Characteristics

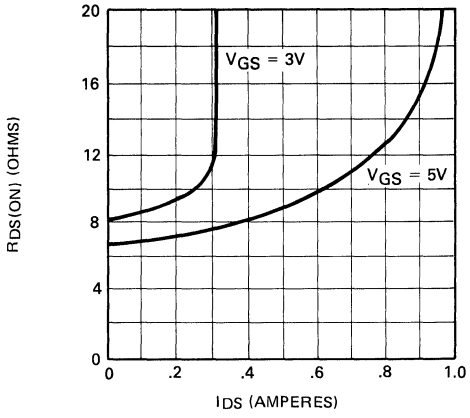


Typical Performance Curves

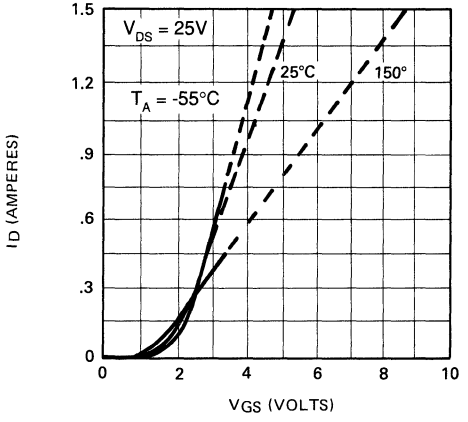
BVDSS Variation with Temperature



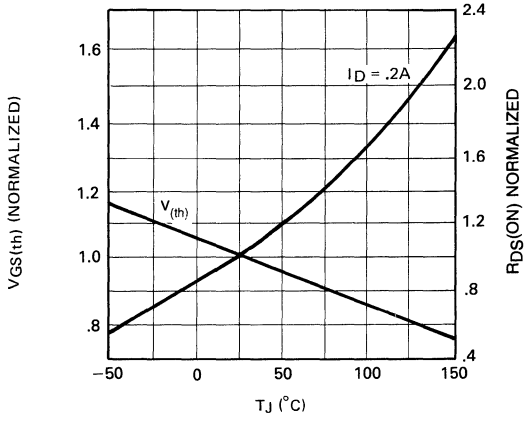
On-Resistance Vs. Drain Current



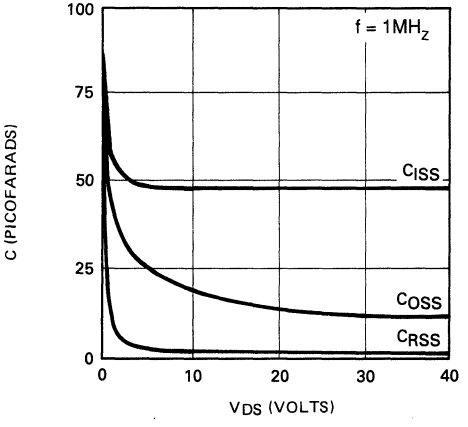
Transfer Characteristics



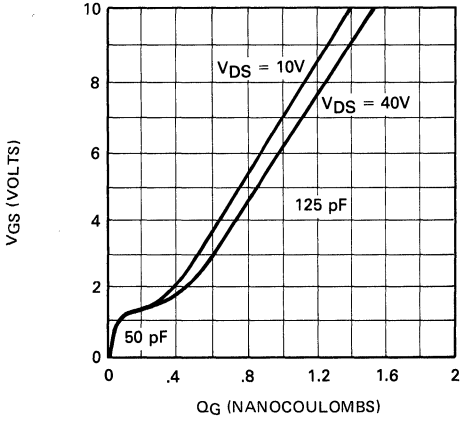
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package					
				TO-39	TO-92	TO-220	Quad P-DIP	Quad C-DIP	DICE
60V	1.5Ω	3.0A	1.6V	TN0606N2	TN0606N3	TN0606N5	TN0606N6	TN0606N7	TN0606ND
100V	1.5Ω	3.0A	1.6V	TN0610N2	TN0610N3	TN0610N5	—	—	TN0610ND

Features

- ☐ Low threshold
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Freedom from secondary breakdown
- ☐ Low input and output leakage

Advanced DMOS Technology

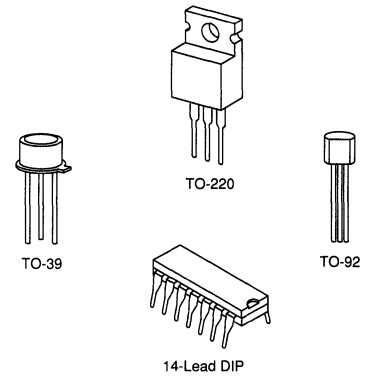
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Logic level interface
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switch
- ☐ General purpose line driver

Package Options (Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-92	0.8A	4A	1W	125	170	0.8A	4.0A
TO-39	1.5A	4A	—	20	125	1.5A	4.0A
T0-220	3.0A	4A	28W	2.7	70	3.0A	4.0A
PLASTIC DIP	Refer to Arrays & Special Functions Section.						
CERAMIC DIP							

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

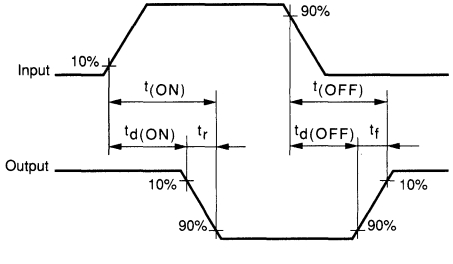
(Notes 1 and 2)

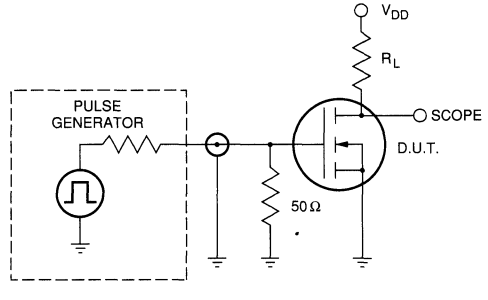
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0610	100			V	V_{GS} = 0, I_D = 1mA
		TN0606	60				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	V_{GS} = V_{DS}, I_D = 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-4.5	mV/°C	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	μA	V_{GS} = 0, V_{DS} = Max Rating
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C (note 2)
$I_{D(ON)}$	ON-State Drain Current		1.2	2.0		A	V_{GS} = 5V, V_{DS} = 25V
			3.0	6.0			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			1.5	2.0	Ω	V_{GS} = 5V, I_D = 0.75A
				1.0	1.5		V_{GS} = 10V, I_D = 0.75A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	
G_{FS}	Forward Transconductance		0.4	0.6		℧	V_{DS} = 25V, I_D = 1.0A
C_{ISS}	Input Capacitance			85	150	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	85		
C_{RSS}	Reverse Transfer Capacitance			10	35		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = 25V, I_D = 1.5A, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				10		
V_{SD}	Diode Forward Voltage Drop			0.8	1.8	V	V_{GS} = 0, I_{SD} = 1.5A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = 1.5A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

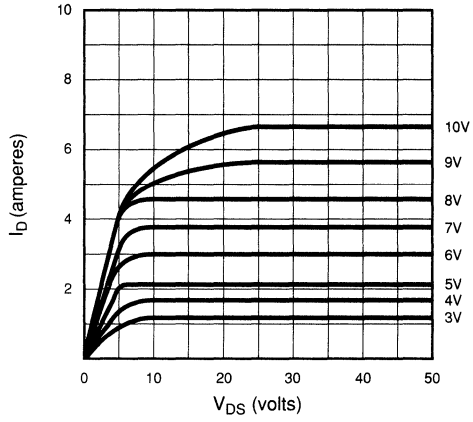
Switching Waveforms and Test Circuit



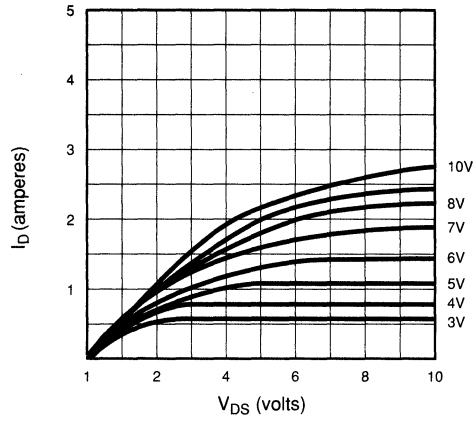


Typical Performance Curves

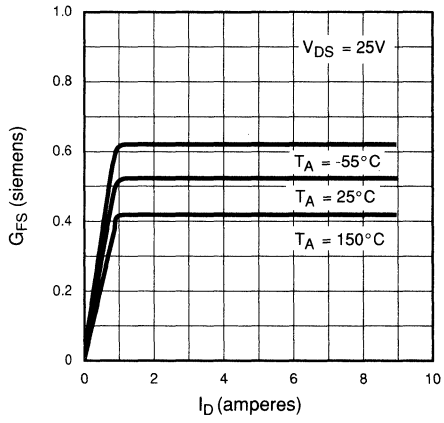
Output Characteristics



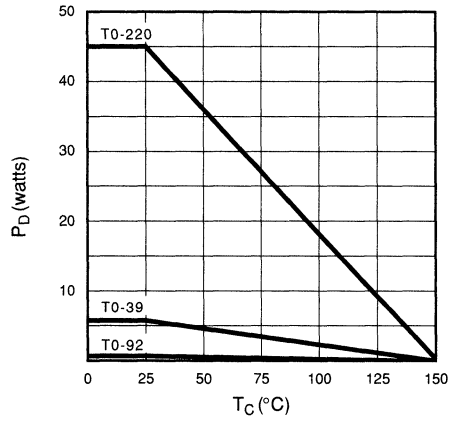
Saturation Characteristics



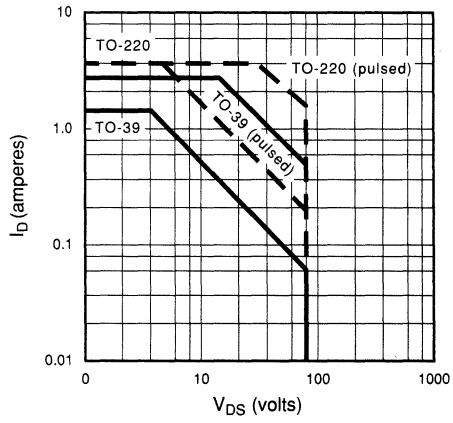
Transconductance vs. Drain Current



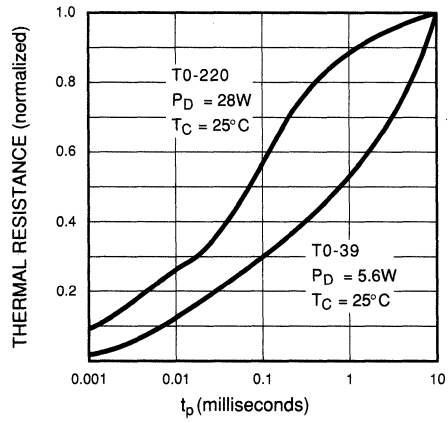
Power Dissipation vs. Case Temperature



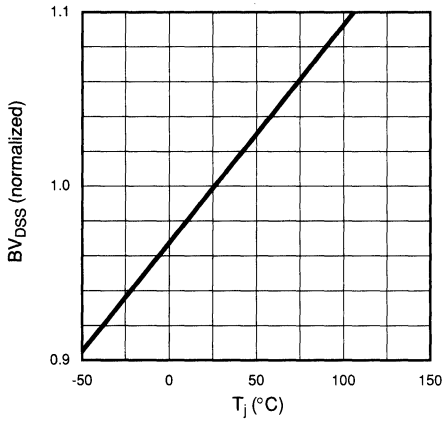
Maximum Rated Safe Operating Area



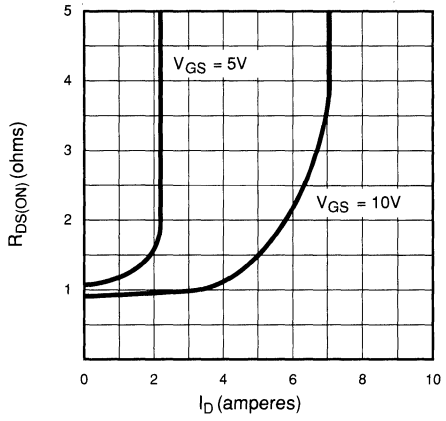
Thermal Response Characteristics



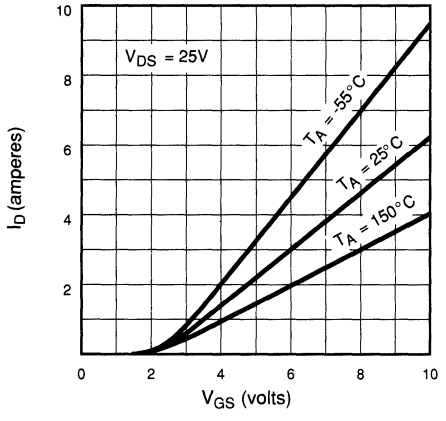
BV$_{DSS}$ Variation with Temperature



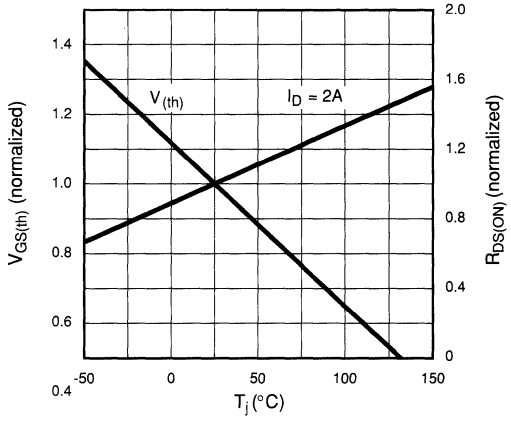
On-Resistance vs. Drain Current



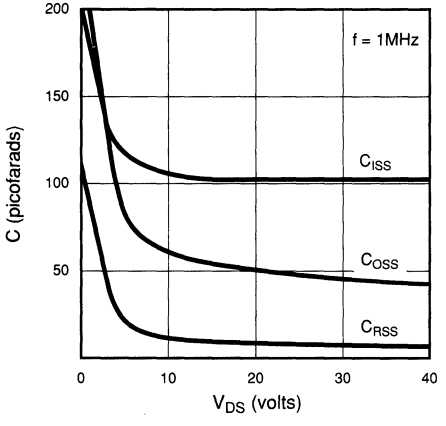
Transfer Characteristics



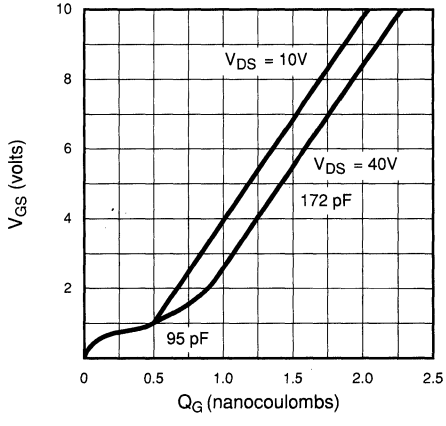
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package			
				TO-39	TO-92	TO-220	DICE
200V	6Ω	1.0A	1.6V	TN0620N2	TN0620N3	TN0620N5	TN0620ND
240V	6Ω	1.0A	1.6V	TN0624N2	TN0624N3	TN0624N5	TN0624ND

Features

- ☐ Low threshold
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Freedom from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Advanced DMOS Technology

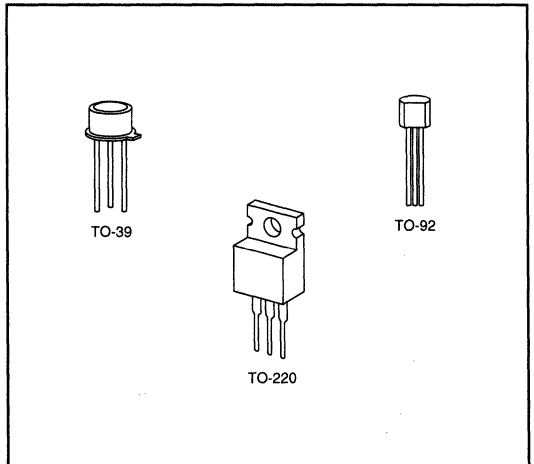
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Logic level interface
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switch
- ☐ General purpose line driver

Package Options (Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	0.7A	2.5A	6W	20	125	0.7A	2.5A
TO-92	0.4A	2.0A	1W	125	170	0.4A	2.0A
TO-220	1.5A	2.5A	28W	4.5	70	1.5A	2.5A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

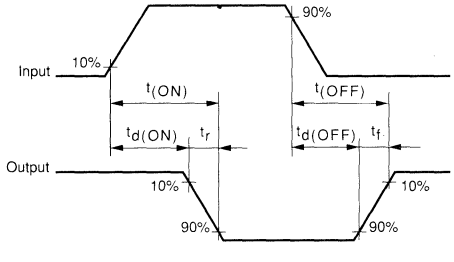
(Notes 1 and 2)

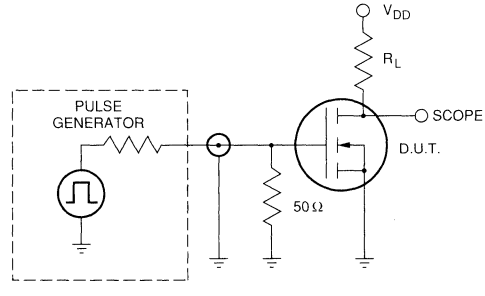
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0624	240			V	V_{GS} = 0, I_D = 2.0mA
		TN0620	200				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	V_{GS} = V_{DS}, I_D = 1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-5.0	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	V_{GS} = 0, V_{DS} = Max Rating
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		0.5			A	V_{GS} = 5V, V_{DS} = 25V
			1.0				V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			6	8	Ω	V_{GS} = 5V, I_D = 0.25A
				4	6		V_{GS} = 10V, I_D = 0.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				1.4	%/°C	V_{GS} = 10V, I_D = 0.5A
G_{FS}	Forward Transconductance		300			m℧	V_{DS} = 25V, I_D = 0.5A
C_{ISS}	Input Capacitance			85	150	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	85		
C_{RSS}	Reverse Transfer Capacitance			10	35		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = 25V, I_D = 1.0A, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				20		
V_{SD}	Diode Forward Voltage Drop				1.8	V	V_{GS} = 0, I_{SD} = 1.0A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = 1.0A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

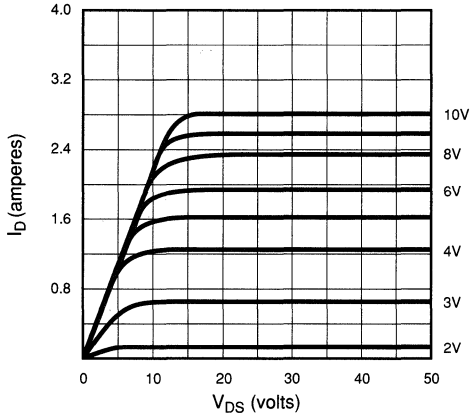
Switching Waveforms and Test Circuit



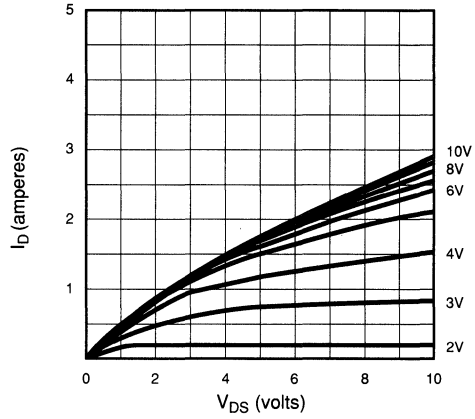


Typical Performance Curves

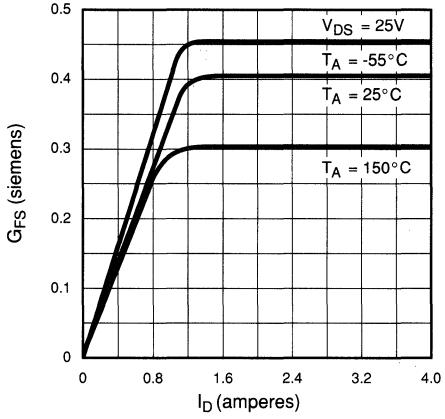
Output Characteristics



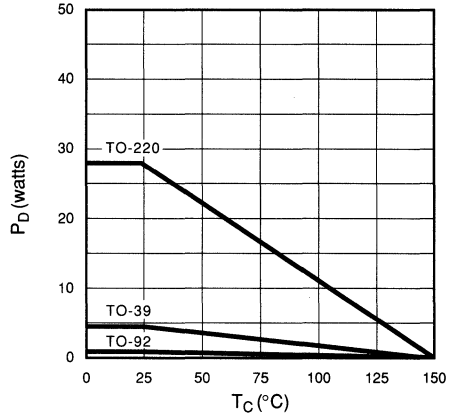
Saturation Characteristics



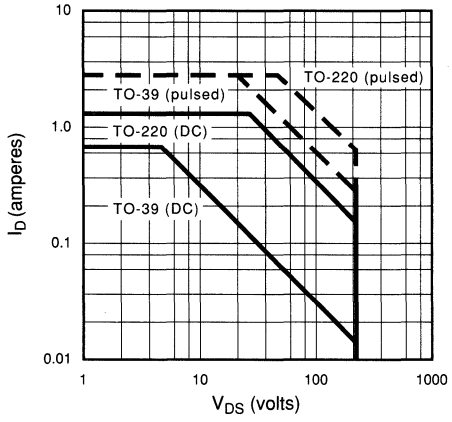
Transconductance vs. Drain Current



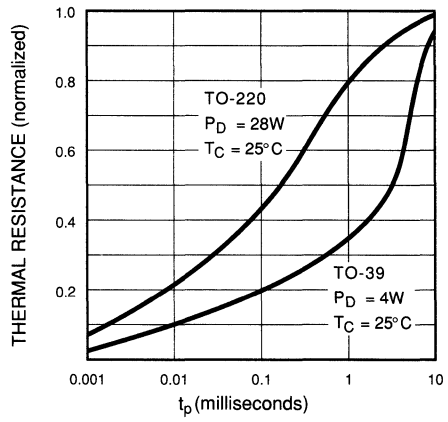
Power Dissipation vs. Case Temperature



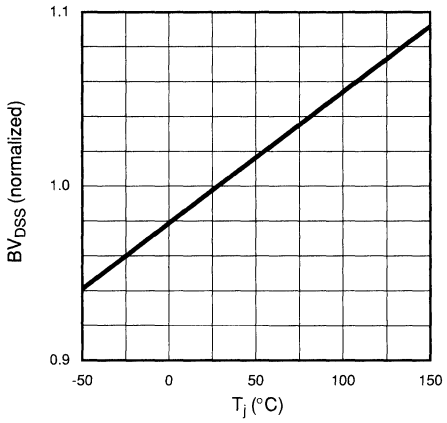
Maximum Rated Safe Operating Area



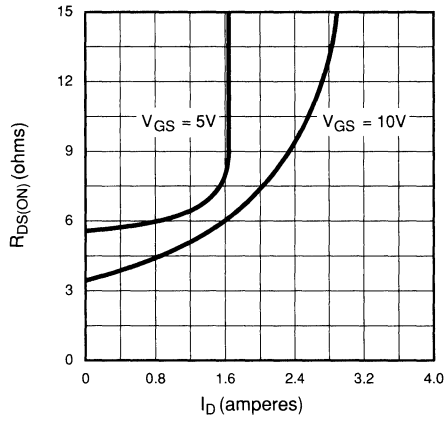
Thermal Response Characteristics



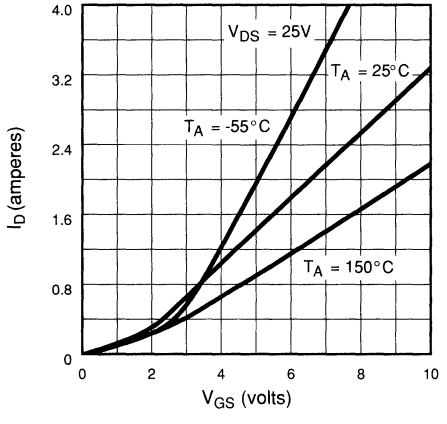
BV$_{DSS}$ Variation with Temperature



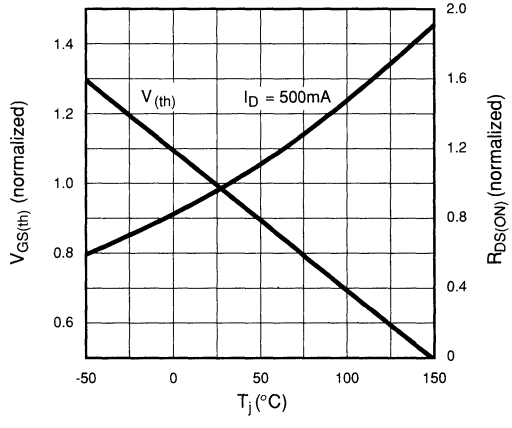
On-Resistance vs. Drain Current



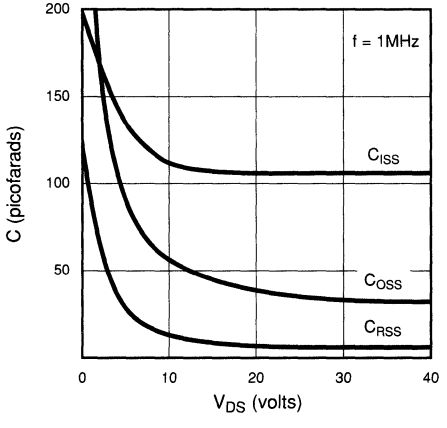
Transfer Characteristics



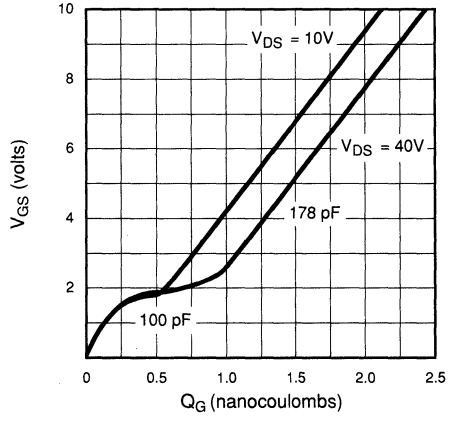
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package			
				TO-39	TO-92	SOW-20*	DICE
20V	0.75Ω	4.0A	1.6V	TN0602N2	TN0602N3	—	TN0602ND
40V	0.75Ω	4.0A	1.6V	TN0604N2	TN0604N3	TN0604WG	TN0604ND

*Same as SO-20 with 300 mil wide body.

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

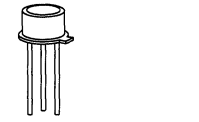
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

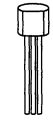
Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps Memories, Displays, Bipolar Transistors, etc.)

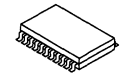
Package Options (Notes 1 and 2)



TO-39



TO-92



SOW-20

Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	2.5A	4.6A	4W	35	125	2.5A	4.6A
TO-92	1.0A	4.6A	1W	125	170	1.0A	4.6A
SOW-20	Refer to Arrays & Special Functions Section.						

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

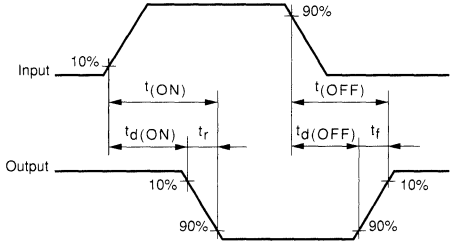
(Notes 1 and 2)

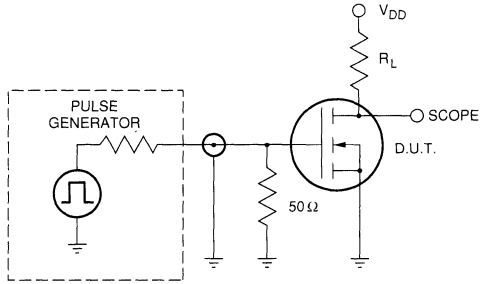
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0604	40			V	V_{GS}= 0, I_D = 2.0mA
		TN0602	20				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	V_{GS} = V_{DS}, I_D = 1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-4.5	mV/°C	V_{GS} = V_{DS}, I_D = 2.5mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Crain Current				10	µA	V_{GS} = 0, V_{DS} = Max Rating
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		1.5	2.1		A	V_{GS} = 5V, V_{DS} = 25V
			4.0	7.0			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			0.8	1.5	Ω	V_{GS} = 5V, I_D = 0.75A
				0.60	0.75		V_{GS} = 10V, I_D = 1.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.5	0.75	%/°C	V_{GS} = 10V, I_D = 2.0A
G_{FS}	Forward Transconductance		0.5	1.0		℧	V_{DS} = 25V, I_D = 2.0A
C_{ISS}	Input Capacitance			85	150	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	85		
C_{RSS}	Reverse Transfer Capacitance			12	35		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = 25V, I_D = 0.5A, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				25		
t_f	Fall Time				13		
V_{SD}	Diode Forward Voltage Drop			-1.2	-1.8	V	V_{GS} = 0, I_{SD} = 1.5A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = 1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

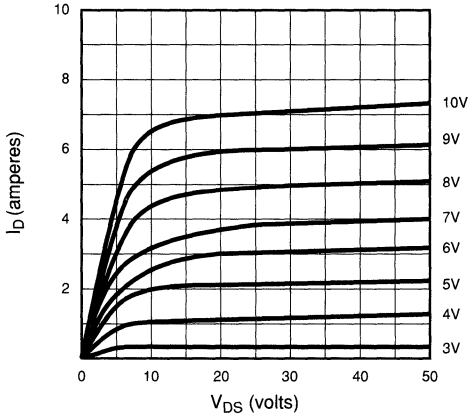
Switching Waveforms and Test Circuit



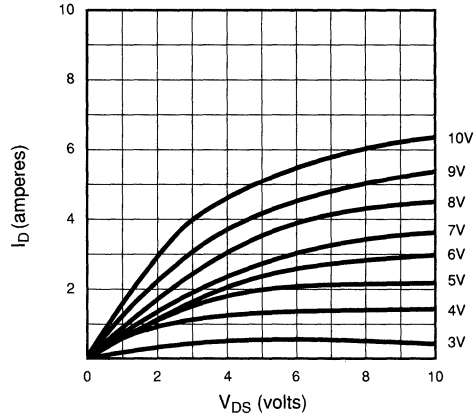


Typical Performance Curves

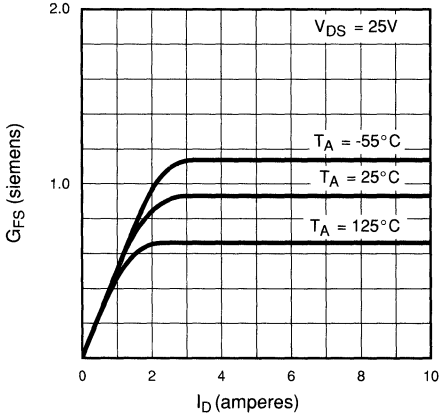
Output Characteristics



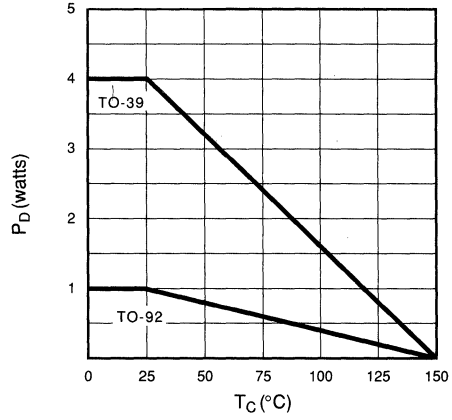
Saturation Characteristics



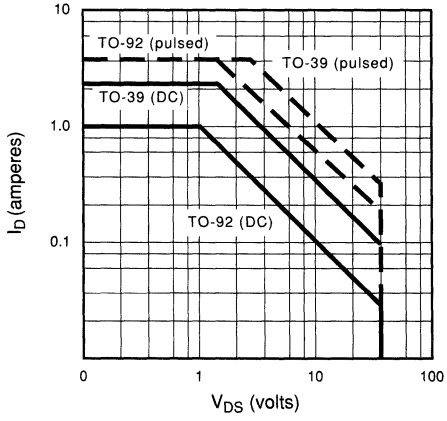
Transconductance vs. Drain Current



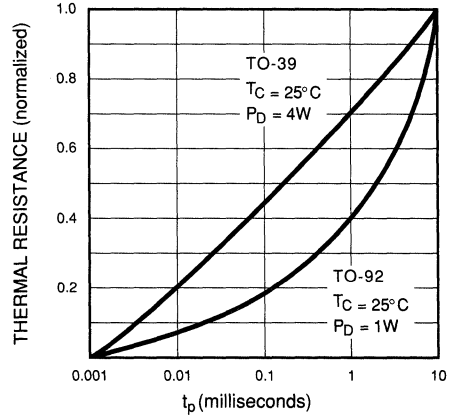
Power Dissipation vs. Case Temperature



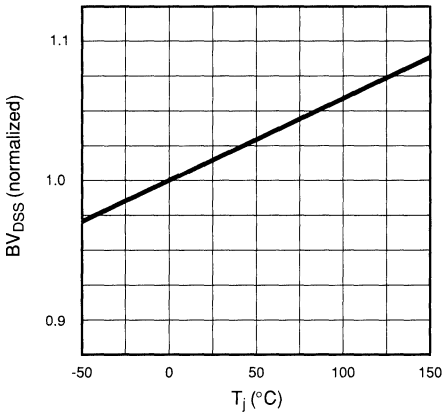
Maximum Rated Safe Operating Area



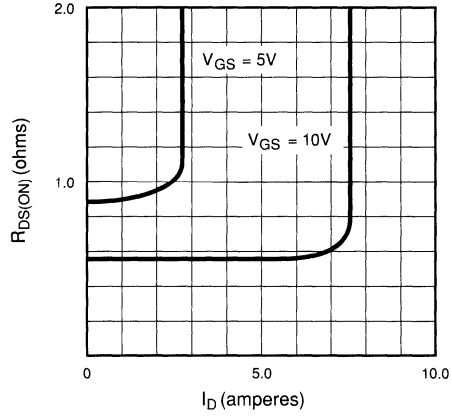
Thermal Response Characteristics



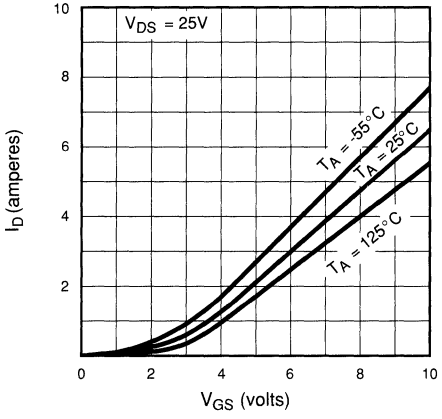
BV$_{DSS}$ Variation with Temperature



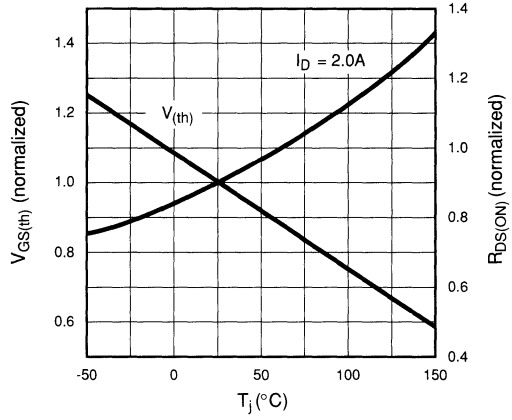
On-Resistance vs. Drain Current



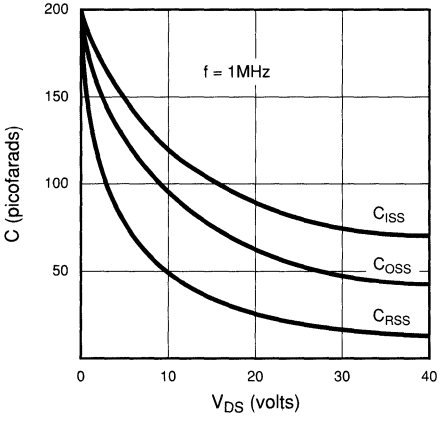
Transfer Characteristics



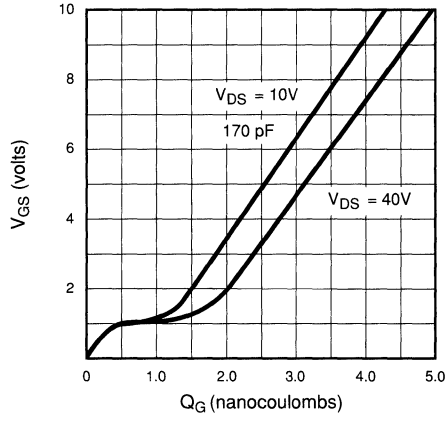
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	DICE
-20V	4.0Ω	-0.85A	TP0102N2	TP0102N3	TP0102ND
-40V	4.0Ω	-0.85A	TP0104N2	TP0104N3	TP0104ND

Features

- ☐ Low threshold
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Freedom from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Advanced DMOS Technology

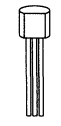
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

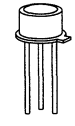
Applications

- ☐ Logic level interface
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switch
- ☐ General purpose line driver

Package Options (Note 1)



TO-92



TO-39

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	-0.9A	-2.6A	3.5W	35	125	-0.9A	-2.6A
TO-92	-0.5A	-2.4A	1.0W	125	170	-0.5A	-2.4A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

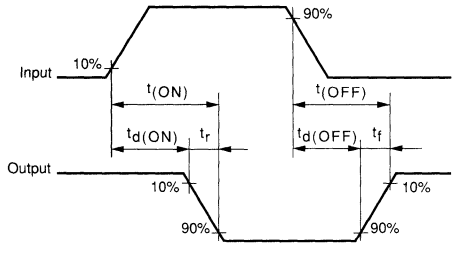
(Notes 1 and 2)

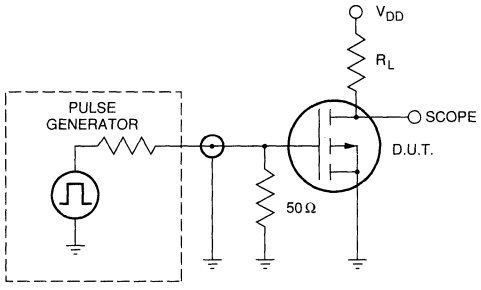
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP0104	-40			V	V_{GS} = 0, I_D = -1.0mA
		TP0102	-20				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-5.8	-6.5	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate Body Leakage			-1.0	-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			0.08			V_{GS} = -3V, V_{DS} = -25V
			-0.25	-0.40		A	V_{GS} = -5V, V_{DS} = -25V
			-0.85	-1.70			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			15			V_{GS} = -3V, I_D = -25mA
				5.5	7.5	Ω	V_{GS} = -5V, I_D = -0.1A
				2.5	4.0		V_{GS} = -10V, I_D = -0.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.55	1.0	%/°C	I_D = -0.5A, V_{GS} = -10V
G_{FS}	Forward Transconductance		225	300		m℧	V_{DS} = -25V, I_D = -0.5A
C_{ISS}	Input Capacitance			45	60	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			22	30		
C_{RSS}	Reverse Transfer Capacitance			3	8		
$t_{d(ON)}$	Turn-ON Delay Time			4	6	ns	V_{DD} = -25V, I_D = -1A, R_S = 50Ω
t_r	Rise Time			7	10		
$t_{d(OFF)}$	Turn-OFF Delay Time			3	5		
t_f	Fall Time			4	6		
V_{SD}	Diode Forward Voltage Drop			-1.2	-2.0	V	I_{SD} = -0.25A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			300		ns	I_{SD} = -1.0A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

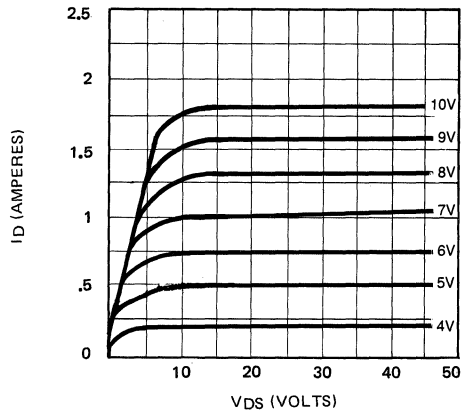
Switching Waveforms and Test Circuit



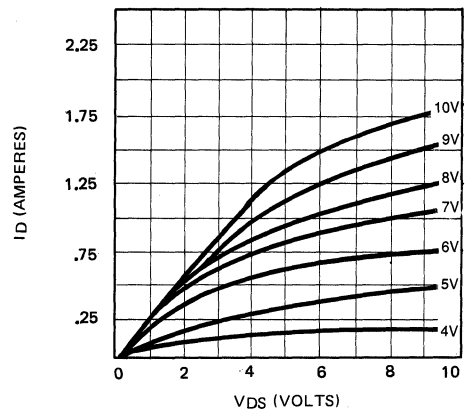


Typical Performance Curves

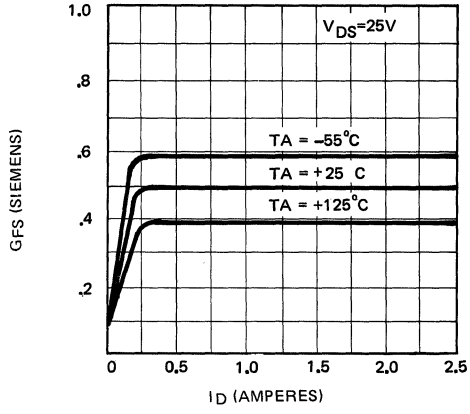
Output Characteristics



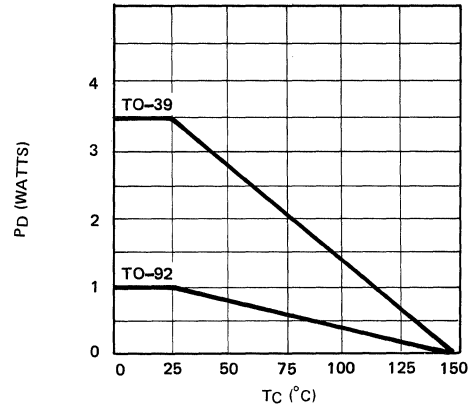
Saturation Characteristics



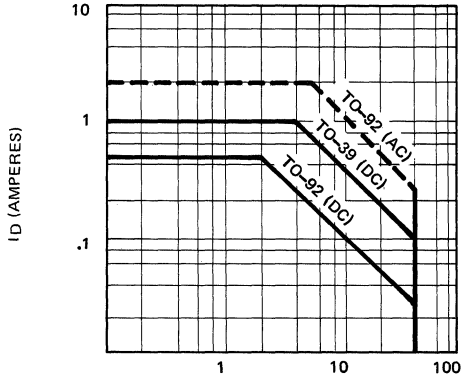
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

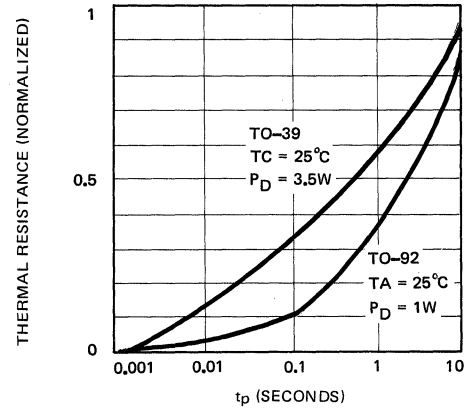


Maximum Rated Safe Operating Area



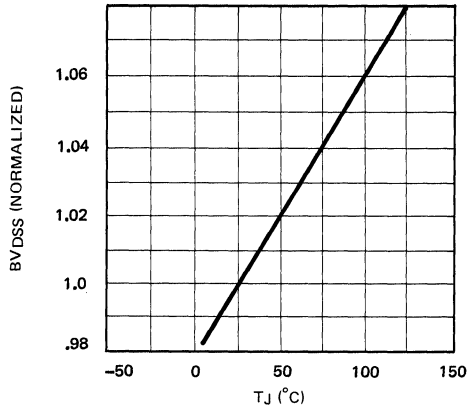
10mS Pulse @ 2V DC

Thermal Response Characteristics

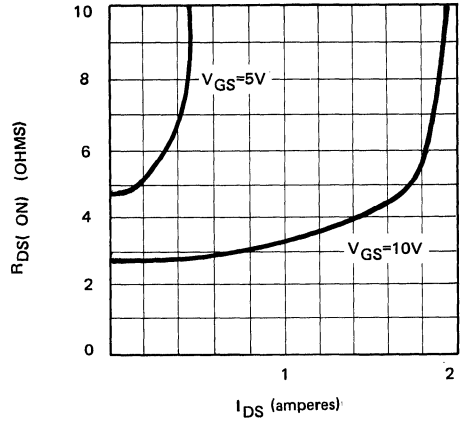


Typical Performance Curves

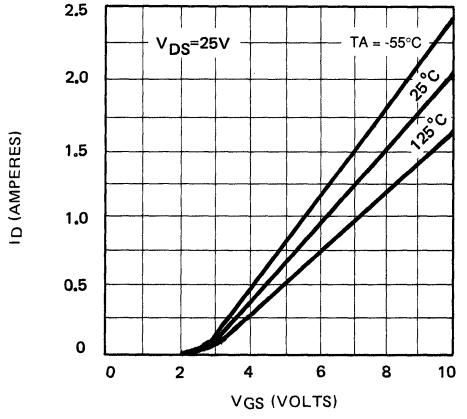
BVDSS Variation with Temperature



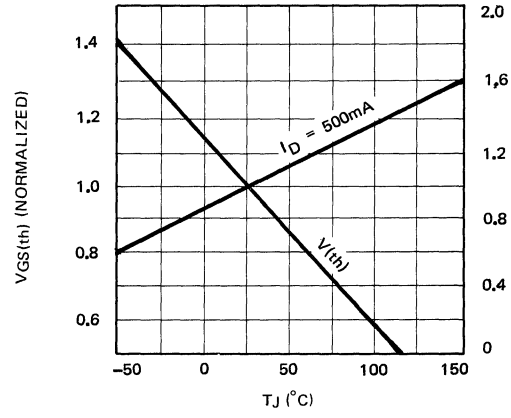
ON-Resistance Vs. Gate-to-Source Voltage



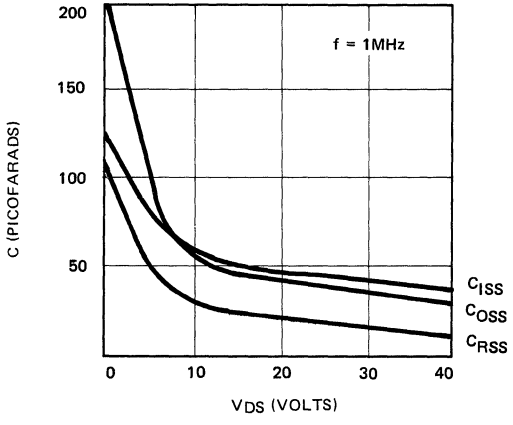
Transfer Characteristics



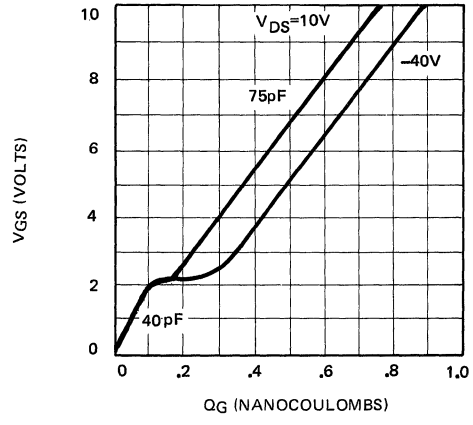
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
-20V	2.0Ω	-2.0A	TP0202N2	TP0202N3
-40V	2.0Ω	-2.0A	TP0204N2	TP0204N3

Features

- ☐ Low threshold
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Freedom from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

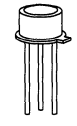
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

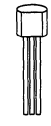
- ☐ Logic level interface
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switch
- ☐ General purpose line driver

Package Options

(Note 1)



TO-39



TO-92

Note 1: See Package Outline section for discrete pinouts.

Ratings and Characteristics

TP02L not recommended for new designs. Refer to TP06L data sheet for all ratings and characteristics.

Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package					
				TO-39	TO-92	TO-220	Quad P-DIP	Quad C-DIP	DICE
-60V	3.5Ω	-1.5A	-2.4V	TP0606N2	TP0606N3	TP0606N5	TP0606N6	TP0606N7	TP0606ND
-100V	3.5Ω	-1.5A	-2.4V	TP0610N2	TP0610N3	TP0610N5	—	—	TP0610ND

Features

- ☐ Low threshold
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Freedom from secondary breakdown
- ☐ Low input and output leakage

Advanced DMOS Technology

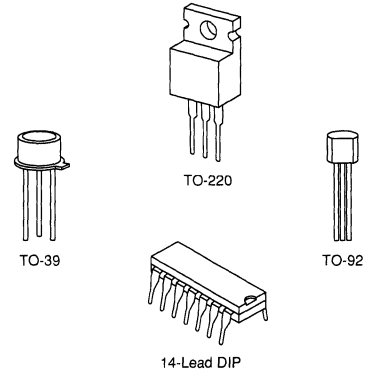
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Logic level interface
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switch
- ☐ General purpose line driver

Package Options (Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	-1.0A	-4.0A	6W	125	20	-0.8A	-4.0A
TO-92	-0.5A	-3.5A	1W	170	125	-0.4A	-3.5A
T0-220	-2.0A	-4.5A	28W	70	2.7	-2.0A	-4.5A
Plastic Dip	Refer to Arrays & Special Functions Section.						
Ceramic Dip							

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

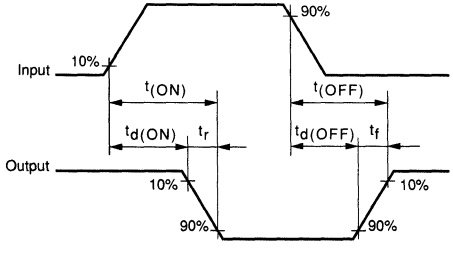
(Notes 1 and 2)

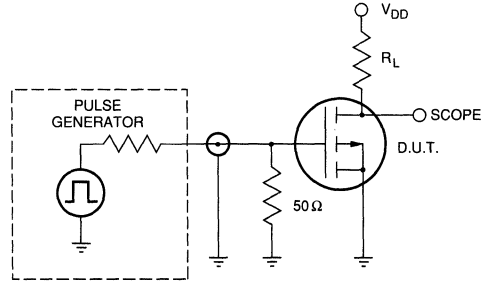
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP0610	-100			V	V_{GS} = 0, I_D = -2.0mA
		TP0606	-60				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-5.0	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-0.4	-0.6		A	V_{GS} = -5V, V_{DS} = -25V
			-1.5	-2.5			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5	7	Ω	V_{GS} = -5V, I_D = -250mA
				3	3.5		V_{GS} = -10V, I_D = 0.75A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				1.7	%/°C	V_{GS} = -10V, I_D = 0.75A
G_{FS}	Forward Transconductance		300			m℧	V_{DS} = -25V, I_D = 0.75A
C_{ISS}	Input Capacitance			85	150	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	85		
C_{RSS}	Reverse Transfer Capacitance			10	35		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = -25V, I_D = -1.0A, R_S = 50Ω
t_r	Rise Time				15		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				15		
V_{SD}	Diode Forward Voltage Drop				-1.8	V	V_{GS} = 0, I_{SD} = -1.0A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = -1.0A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

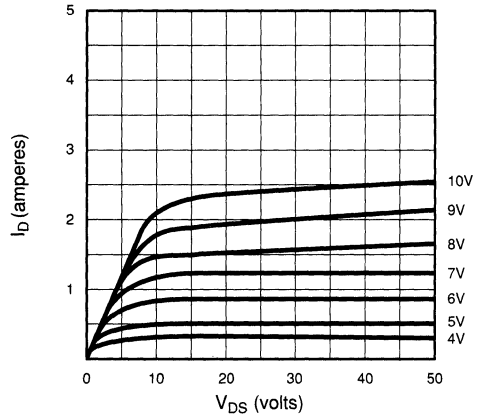
Switching Waveforms and Test Circuit



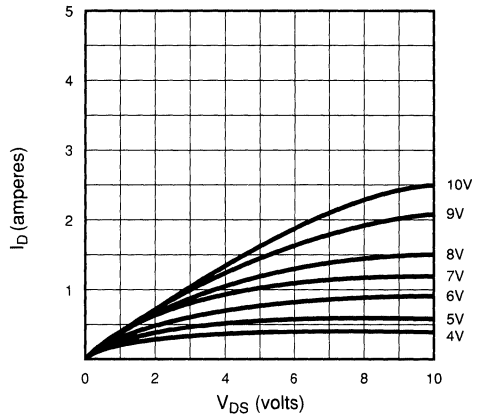


Typical Performance Curves

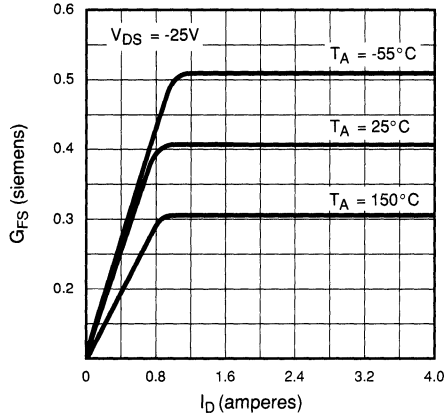
Output Characteristics



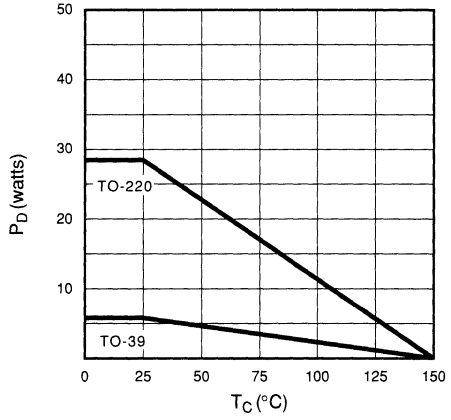
Saturation Characteristics



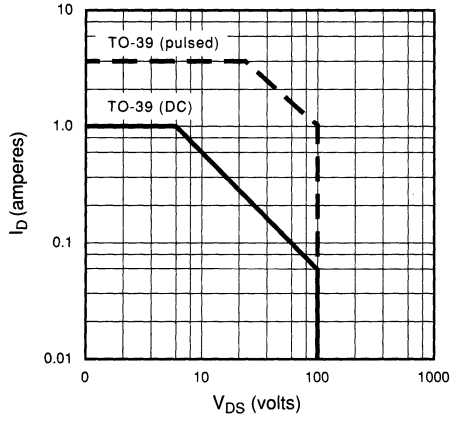
Transconductance vs. Drain Current



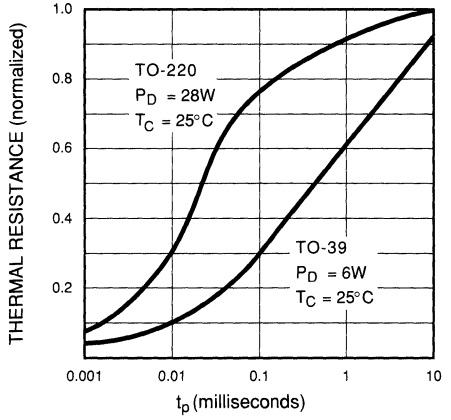
Power Dissipation vs. Case Temperature



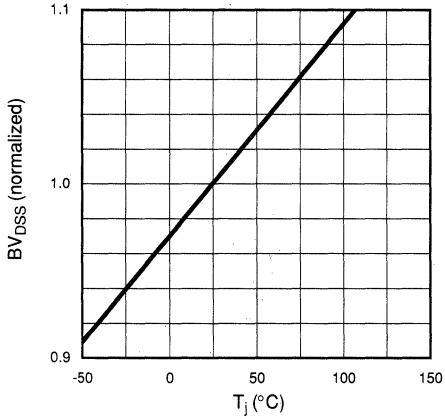
Maximum Rated Safe Operating Area



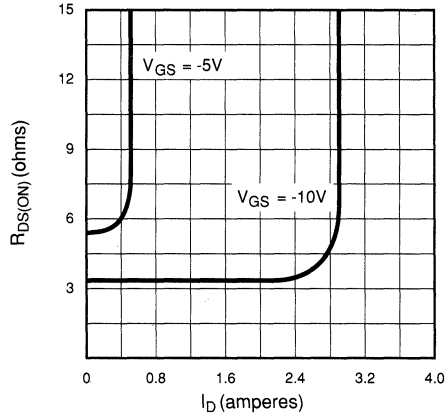
Thermal Response Characteristics



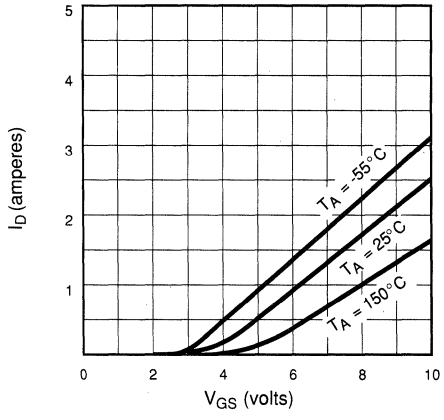
BV$_{DSS}$ Variation with Temperature



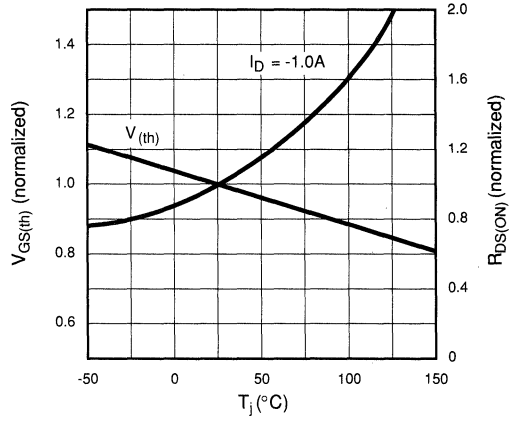
On-Resistance vs. Drain Current



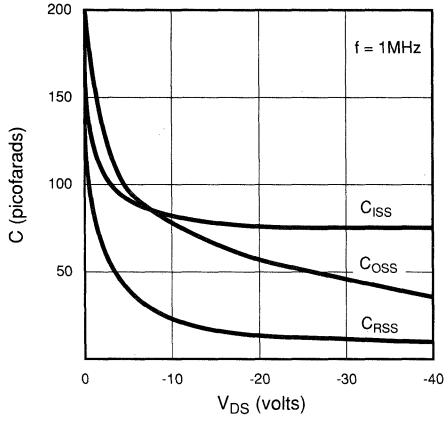
Transfer Characteristics



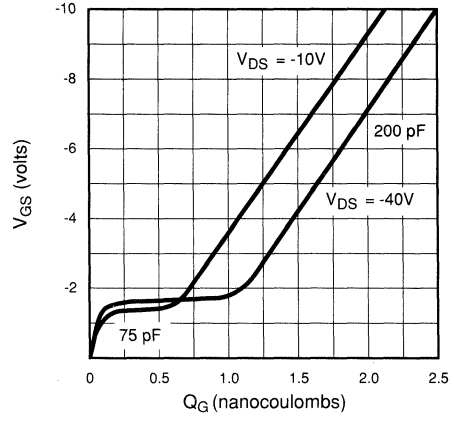
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package			
				TO-39	TO-92	TO-220	DICE
-160V	12Ω	-0.75A	-2.4A	TP0616N2	TP0616N3	TP0616N5	TP0616ND
-200V	12Ω	-0.75A	-2.4A	TP0620N2	TP0620N3	TP0620N5	TP0620ND

Features

- ☐ Low threshold
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Freedom from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Advanced DMOS Technology

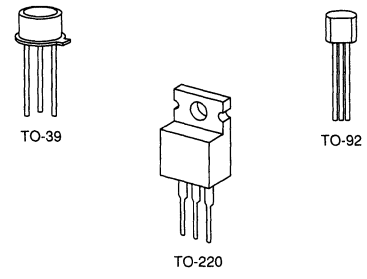
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Logic level interface
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switch
- ☐ General purpose line driver

Package Options (Note 1)



Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	-1.0A	-1.5A	6W	21	125	-1.0A	-1.5A
TO-92	-0.4A	-0.8A	1W	125	170	-0.4A	-0.8A
TO-220	-1.0A	-2.5A	28W	2.7	70	-1.0A	-2.5A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

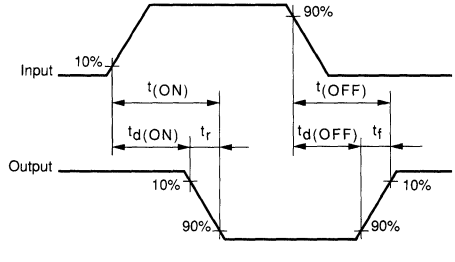
(Notes 1 and 2)

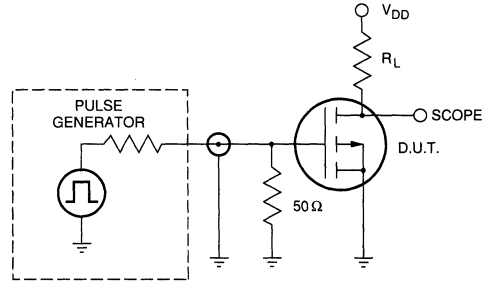
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP0620	-200			V	V_{GS} = 0, I_D = -2.0mA
		TP0616	-160				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-4.5	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-0.25			A	V_{GS} = -5V, V_{DS} = -25V
			-0.75				V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			12	15	Ω	V_{GS} = -5V, I_D = -0.1mA
				9	12		V_{GS} = -10V, I_D = -0.2A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				1.7	%/°C	V_{GS} = -10V, I_D = -0.2A
G_{FS}	Forward Transconductance		100			m℧	V_{DS} = -25V, I_D = -0.2A
C_{ISS}	Input Capacitance			85	150	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	85		
C_{RSS}	Reverse Transfer Capacitance			10	35		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = -25V, I_D = -1.0A, R_S = 50Ω
t_r	Rise Time				15		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				15		
V_{SD}	Diode Forward Voltage Drop				-1.8	V	V_{GS} = 0, I_{SD} = 0.5A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = 0.5A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

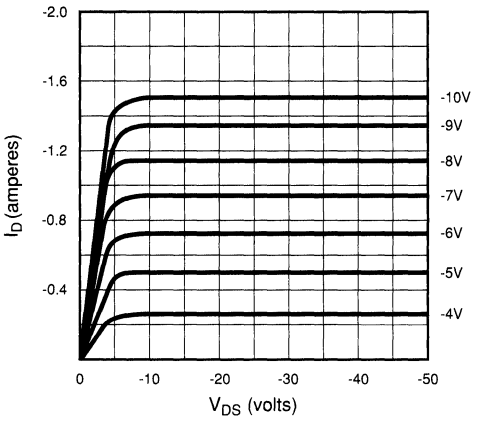
Switching Waveforms and Test Circuit



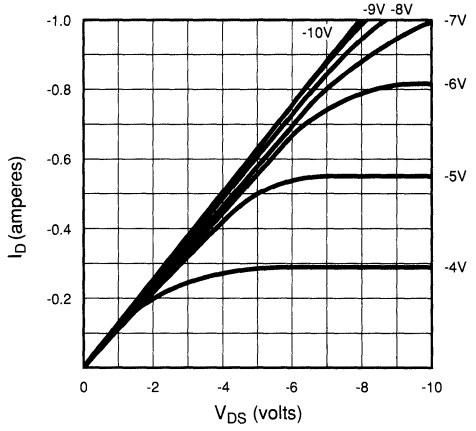


Typical Performance Curves

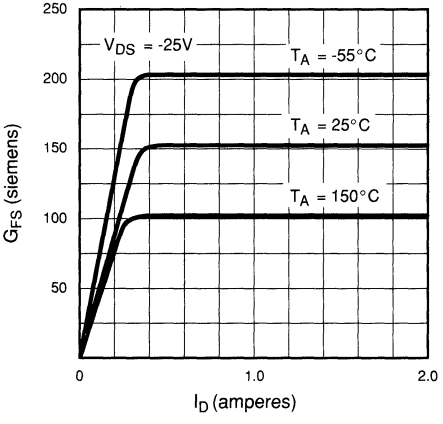
Output Characteristics



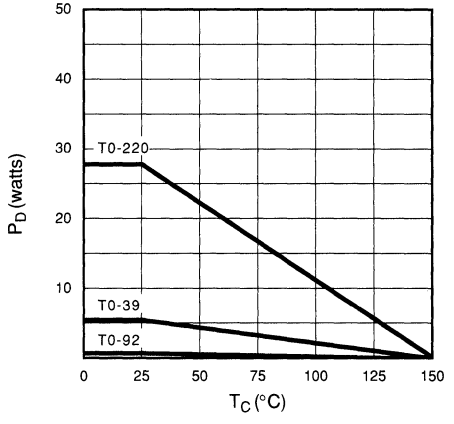
Saturation Characteristics



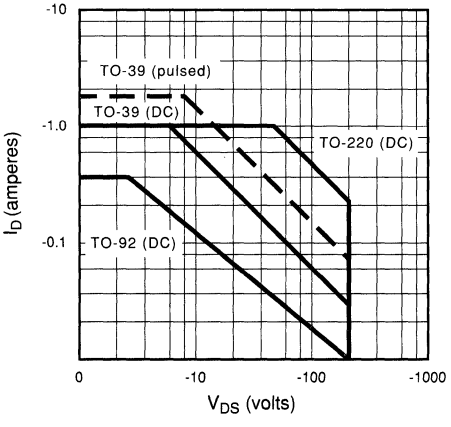
Transconductance vs. Drain Current



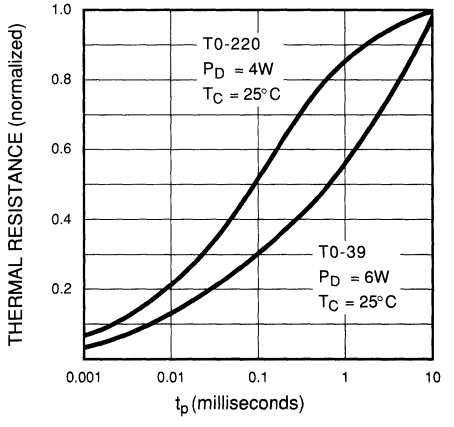
Power Dissipation vs. Case Temperature



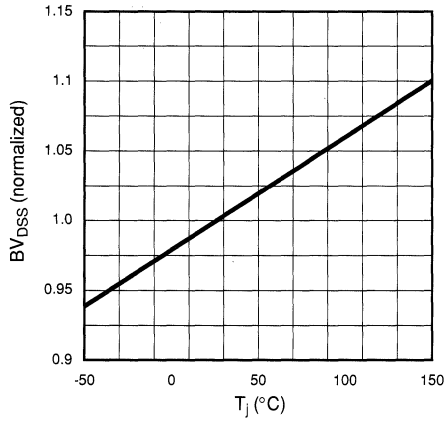
Maximum Rated Safe Operating Area



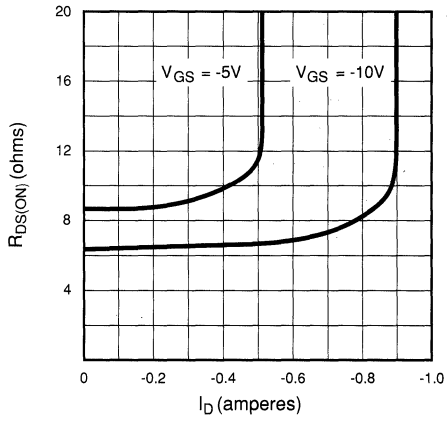
Thermal Response Characteristics



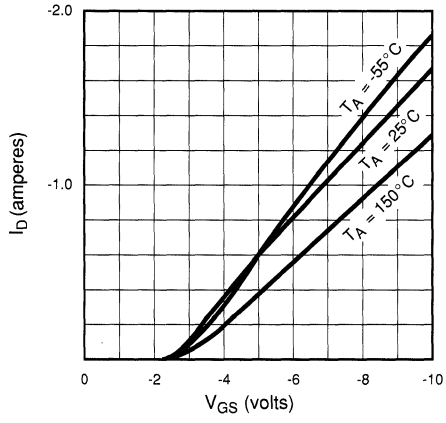
BV$_{DSS}$ Variation with Temperature



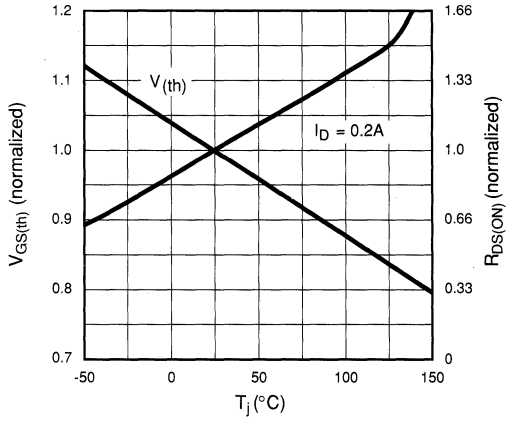
On-Resistance vs. Drain Current



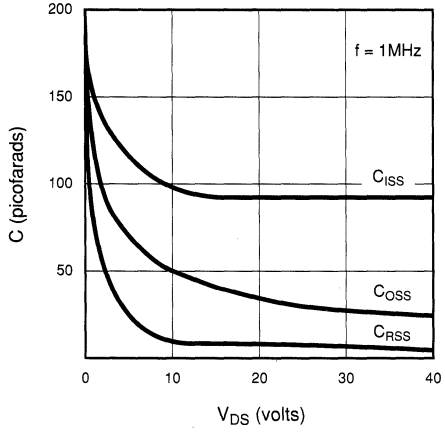
Transfer Characteristics



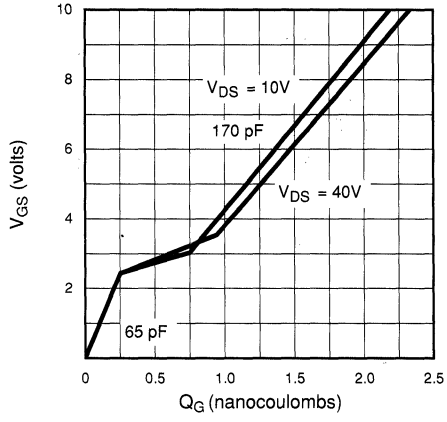
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package			
				TO-39	TO-92	SOW-20*	DICE
-20V	2.0Ω	-2.0A	-2.4V	TP0602N2	TP0602N3	—	TP0602ND
-40V	2.0Ω	-2.0A	-2.4V	TP0604N2	TP0604N3	TP0604WG	TP0604ND

*Same as SO-20 with 300 mil wide body.

Features

- ☐ Low threshold
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Freedom from secondary breakdown
- ☐ Low input and output leakage

Advanced DMOS Technology

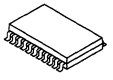
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Logic level interface
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switch
- ☐ General purpose line driver

Package Options (Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	-2.0A	-4.8A	6W	20	125	-2.0A	-4.8A
TO-92	-0.75A	-4.2A	1W	125	170	-0.75A	-4.2A
SOW-20	Refer to Arrays & Special Functions Section						

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

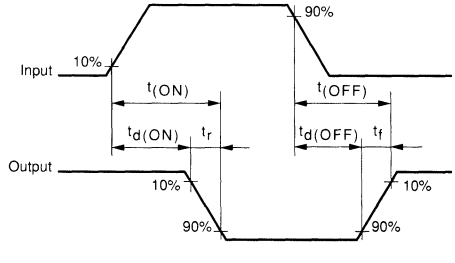
(Notes 1 and 2)

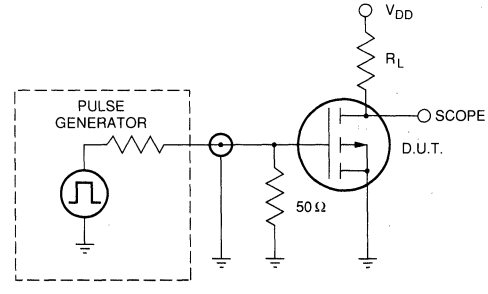
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP0604	-40			V	V_{GS} = 0, I_D = -2.0mA
		TP0602	-20				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.0	-4.5	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-0.4	-0.7		A	V_{GS} = -5V, V_{DS} = -25V
			-2.0	-3.3			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			2.0	3.5	Ω	V_{GS} = -5V, I_D = -250mA
				1.5	2.0		V_{GS} = -10V, I_D = -1.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.75	1.2	%/°C	V_{GS} = -10V, I_D = -1.0A
G_{FS}	Forward Transconductance		0.4	0.65		℧	V_{DS} = -25V, I_D = -1.0A
C_{ISS}	Input Capacitance			85	150	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			55	85		
C_{RSS}	Reverse Transfer Capacitance			15	35		
$t_{d(ON)}$	Turn-ON Delay Time			5	10	ns	V_{DD} = -25V, I_D = -1.0A, R_S = 50Ω
t_r	Rise Time			7	10		
$t_{d(OFF)}$	Turn-OFF Delay Time			10	15		
t_f	Fall Time			6	10		
V_{SD}	Diode Forward Voltage Drop			-1.3	-2.0	V	V_{GS} = 0, I_{SD} = -1.5A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = -1.5A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

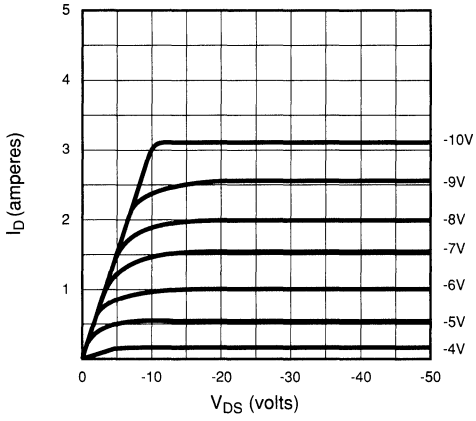
Switching Waveforms and Test Circuit



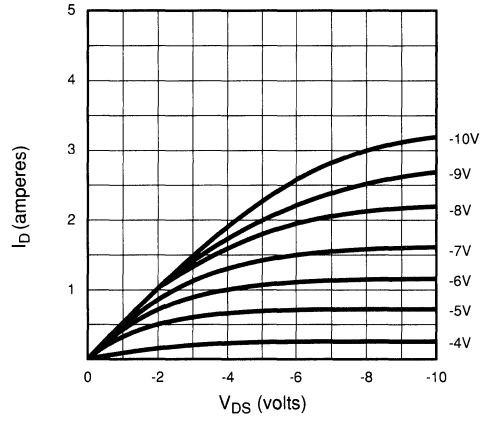


Typical Performance Curves

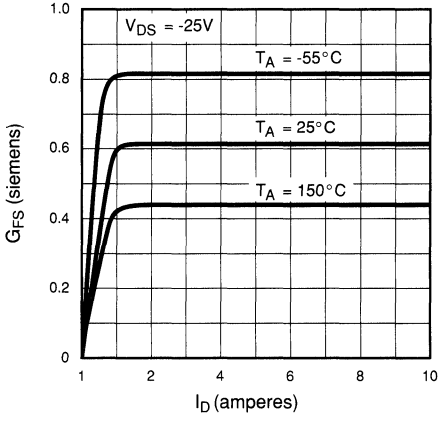
Output Characteristics



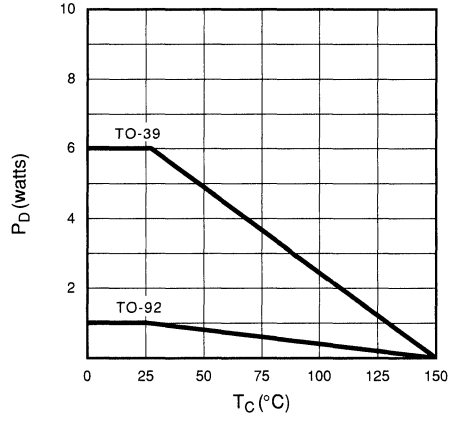
Saturation Characteristics



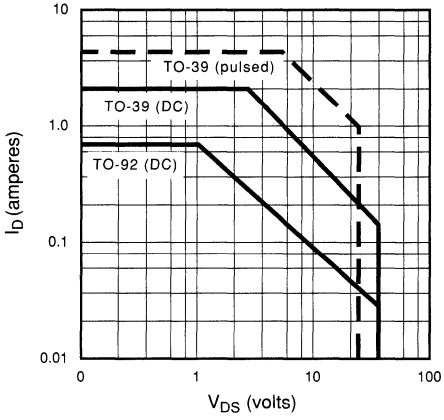
Transconductance vs. Drain Current



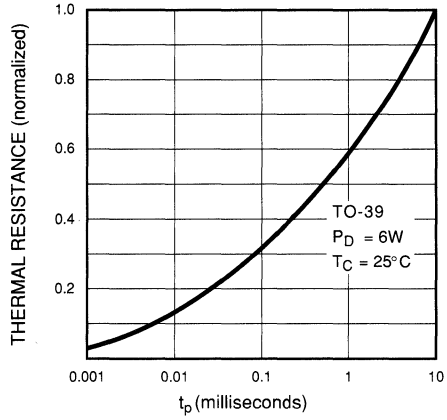
Power Dissipation vs. Case Temperature



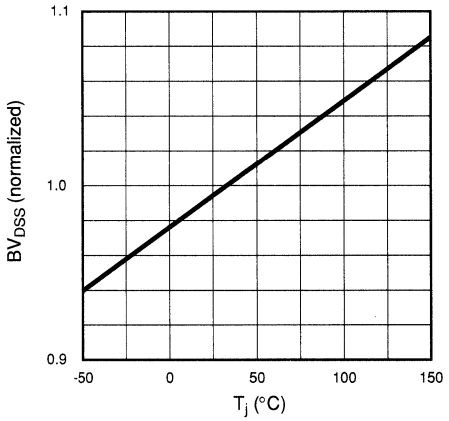
Maximum Rated Safe Operating Area



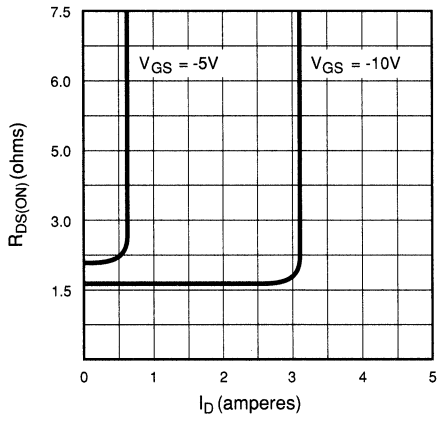
Thermal Response Characteristics



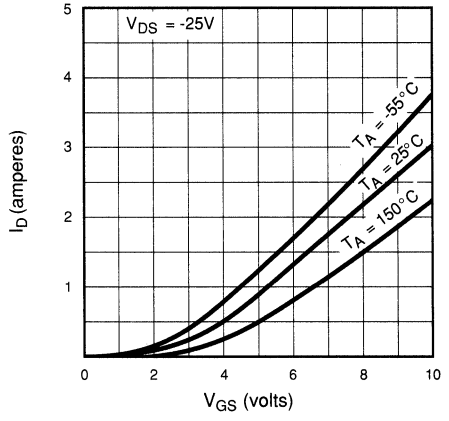
BV$_{DSS}$ Variation with Temperature



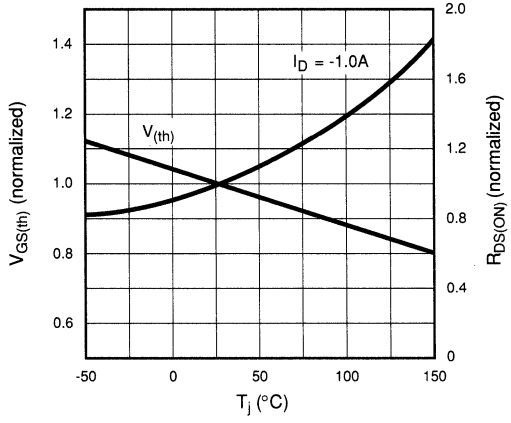
On-Resistance vs. Drain Current



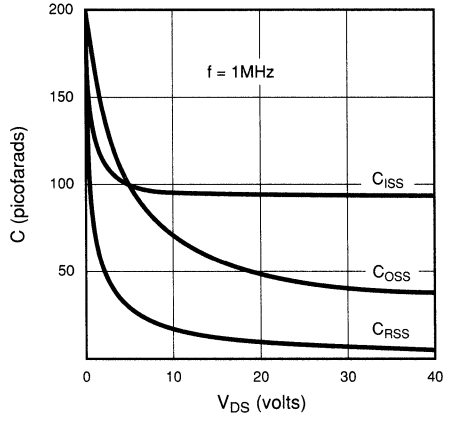
Transfer Characteristics



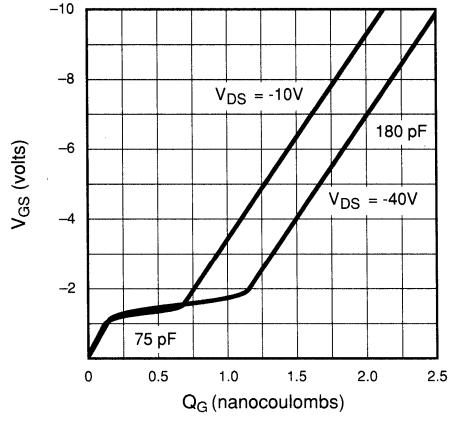
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FET

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			TO-39
35V	1.8Ω	1.5A	2N6659

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

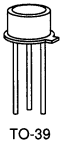
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-39

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W
TO-39	1.4A	3A	6.25	170	20

*I_D (continuous) is limited by max rated T_j.

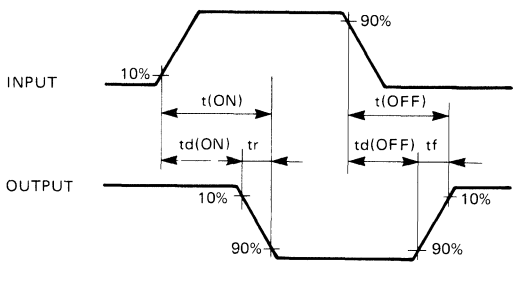
Electrical Characteristics (@ 25°C unless otherwise specified)

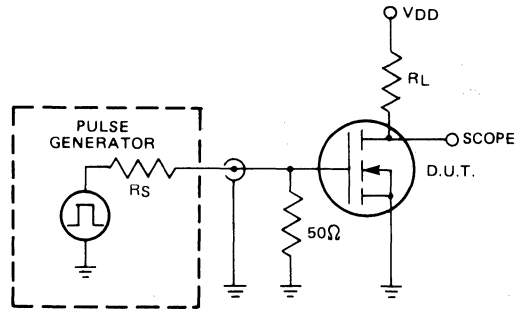
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	35			V	I_D = 10μA, V_{GS} = 0
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage			100	nA	V_{GS} = ±15V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			10		V_{GS} = 0, V_{DS} = Max Rating
				500	μA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	1.5			A	V_{GS} = −10V, V_{DS} ≥ 2 $V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5.0	Ω	V_{GS} = 5V, I_D = 0.3A
				1.8		V_{GS} = 10V, I_D = 1A
G_{FS}	Forward Transconductance	170			m℧	V_{DS} = 24V, I_D = 0.5A
C_{ISS}	Input Capacitance			50	pF	V_{GS} = 0, V_{DS} = 25V, f = 1MHz
C_{OSS}	Common Source Output Capacitance			65		
C_{RSS}	Reverse Transfer Capacitance			10		
$t_{(ON)}$	Turn-ON Time			10	ns	V_{DD} = 25V, I_D = 1A, R_S = 50Ω
$t_{(OFF)}$	Turn-OFF Time			10		
V_{SD}	Diode Forward Voltage Drop		0.9		V	I_{SD} = −1.4A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			TO-39
60V	3.0Ω	1.5A	2N6660
90V	4.0Ω	1.5A	2N6661

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

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These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

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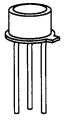
Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-39

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
2N6660	1.1A	3A	6.25W	125	20	2.5A	5.0A
2N6661	0.9A	3A	6.25W	125	20	2.5A	5.0A

*I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BVDSS	Drain-to-Source Breakdown Voltage	2N6660	60			V	VGS = 0, ID = 10μA
		2N6661	90				
VGS(th)	Gate Threshold Voltage		0.8		2.0	V	VDS = VGS, ID = 1mA
ΔVGS(th)	Change in VGS(th) with Temperature			−3.8	−5.5	mV/°C	VGS = VDS, ID = 1mA
IGSS	Gate Body Leakage				100	nA	VGS = 15V, VDS = 0
					500		VGS = 15V, VDS = 0, TA = 125°C
IDSS	Zero Gate Voltage Drain Current				10	μA	VGS = 0, VDS = Max Rating
					500		VGS = 0, VDS = 0.8 Max Rating TA = 125°C
ID(ON)	ON-State Drain Current		1.5			A	VDS = 25V, VGS = 10V
RDS(ON)	Static Drain-to-Source ON-State Resistance	ALL			5.0	Ω	VGS = 5V, ID = 0.3A
		2N6660			3.0		VGS = 10V, ID = 1A
		2N6661			4.0		VGS = 10V, ID = 1A
GFS	Forward Transconductance		170			m℧	VDS = 25V, ID = 0.5A
CISS	Input Capacitance				50	pF	VDS = 25V, VGS = 0 f = 1MHz
COSS	Common Source Output Capacitance				40		
CRSS	Reverse Transfer Capacitance				10		
td(ON)	Turn-ON Delay Time				10	ns	VDD = 25V, RL = 23Ω' RS = 25Ω
tr	Rise Time						
td(OFF)	Turn-OFF Delay Time				10		
tf	Fall Time						
VSD	Diode Forward Voltage Drop			1.2		V	VGS = 0, ISD = 1A
trr	Reverse Recovery Time			350		ns	VGS = 0, ISD = 1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

N-Channel Enhancement-Mode Vertical DMOS Power FET

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			TO-92
60V	5Ω	75mA	2N7000

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

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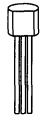
Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation	θ_{ja} °C/W	θ_{jc} °C/W
TO-92	200mA	500mA	400mW	312.5	40

*I_D (continuous) is limited by max rated T_j.

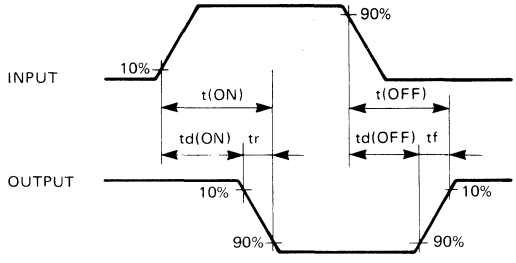
Electrical Characteristics (@ 25°C unless otherwise specified)

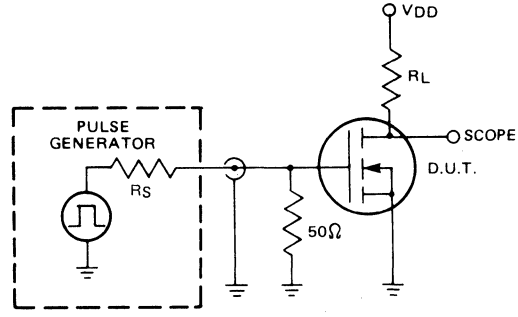
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60			V	I_D = 10μA, V_{GS} = 0
$V_{GS(th)}$	Gate Threshold Voltage	0.8		3.0	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage			10	nA	V_{GS} = ±15V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			1	μA	V_{GS} = 0, V_{DS} = 48V
				1	mA	V_{GS} = 0, V_{DS} = 48V T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	75			mA	V_{GS} = 4.5, V_{DS} = 10V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5	Ω	V_{GS} = 10V, I_D = 0.5A
G_{FS}	Forward Transconductance	100			m℧	V_{DS} = 10V, I_D = 0.2A
C_{ISS}	Input Capacitance			60	pF	V_{GS} = 0, V_{DS} = 25V f = 1MHz
C_{OSS}	Common Source Output Capacitance			25		
C_{RSS}	Reverse Transfer Capacitance			5		
$t_{(ON)}$	Turn-ON Time			10	ns	V_{DD} = 15V, I_D = 0.5A R_S = 50Ω
$t_{(OFF)}$	Turn-OFF Time			10		
V_{SD}	Diode Forward Voltage Drop		−0.85		V	I_{SD} = −0.2A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





N-Channel Enhancement-Mode Vertical DMOS Power FET

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			TO-92
240V	45Ω	150mA	2N7007

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Note 1)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation	θ_{ja} °C/W	θ_{jc} °C/W
TO-92	65mA	260mA	400mW	312.5	40

* I_D (continuous) is limited by max rated T_j.

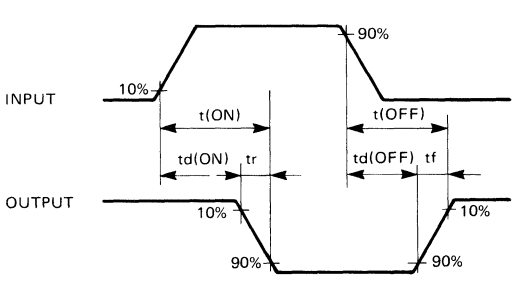
Electrical Characteristics (@ 25°C unless otherwise specified)

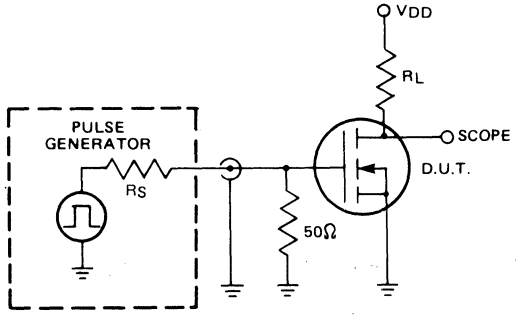
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	240			V	I_D = 100μA, V_{GS} = 0
$V_{GS(th)}$	Gate Threshold Voltage	1		2.5	V	V_{GS} = V_{DS}, I_D = 250 μA
I_{GSS}	Gate Body Leakage			10	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			100		V_{GS} = 0, V_{DS} = 120V
				1	μA	V_{GS} = 0, V_{DS} = 120V T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	50			mA	V_{GS} = 4.5V, V_{DS} ≥ 2 $V_{DS(ON)}$
		150				V_{GS} = 10V, V_{DS} ≥ 2 $V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			45	Ω	V_{GS} = 4.5V, I_D = 20mA
				45		V_{GS} = 10V, I_D = 50mA
G_{FS}	Forward Transconductance	30			m℧	V_{DS} ≥ 2 $V_{DS(ON)}$, I_D = 50mA
C_{ISS}	Input Capacitance			30	pF	V_{GS} = 0, V_{DS} = 25V f = 1MHz
C_{OSS}	Common Source Output Capacitance			15		
C_{RSS}	Reverse Transfer Capacitance			10		
$t_{(ON)}$	Turn-ON Time			30	ns	V_{DD} = 60V, I_D = 50mA R_S = 50Ω
$t_{(OFF)}$	Turn-OFF Time			20		
V_{SD}	Diode Forward Voltage Drop			−1.2	V	I_{SD} = −65mA, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			TO-92
60V	7.5Ω	500mA	2N7008

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

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Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Note 1)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation	θ_{ja} °C/W	θ_{jc} °C/W
TO-92	150mA	1A	400mW	312.5	40

*I_D (continuous) is limited by max rated T_j.

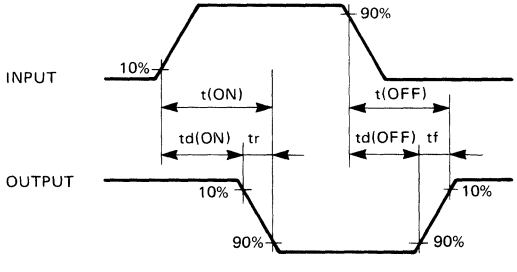
Electrical Characteristics (@ 25°C unless otherwise specified)

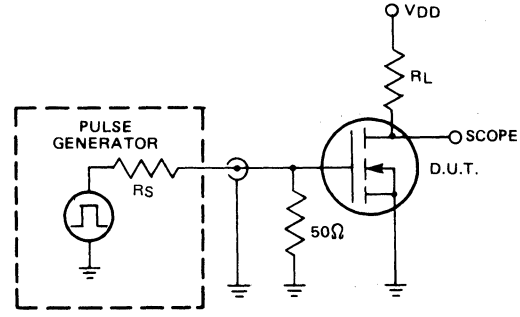
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60			V	I_D = −10μA, V_{GS} = 0
$V_{GS(th)}$	Gate Threshold Voltage	1		2.5	V	V_{GS} = V_{DS}, I_D = 250μA
I_{GSS}	Gate Body Leakage			100	nA	V_{GS} = ±30V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			1	μA	V_{GS} = 0V, V_{DS} = 50V
				500		V_{GS} = 0V, V_{DS} = 50V, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	500			mA	V_{GS} = 10V, V_{DS} ≥ 2 $V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			7.5	Ω	V_{GS} = 5V, I_D = 50mA
				7.5		V_{GS} = 10V, I_D = 500mA
G_{FS}	Forward Transconductance	80			m℧	V_{DS} ≥ 2 $V_{DS(ON)}$, I_D = 200mA
C_{ISS}	Input Capacitance			50	pF	V_{GS} = 0, V_{DS} = 25V, f = 1MHz
C_{OSS}	Common Source Output Capacitance			25		
C_{RSS}	Reverse Transfer Capacitance			5		
$t_{(ON)}$	Turn-ON Time			20	ns	V_{DD} = 30V, I_D = 200mA, R_S = 50Ω
$t_{(OFF)}$	Turn-OFF Time			20		
V_{SD}	Diode Forward Voltage Drop			−1.5	V	I_{SD} = −150mA, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			TO-220
100V	0.6Ω	4.0A	IRF510
60V	0.6Ω	4.0A	IRF511
100V	0.8Ω	3.5A	IRF512
60V	0.8Ω	3.5A	IRF513

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

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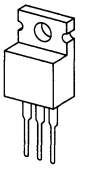
Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



G D S
TO-220

Note 1: See Package Outline section fro discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
IRF510	4.0A	16.0A	20W	80	6.4	4.0A	16.0A
IRF511	4.0A	16.0A	20W	80	6.4	4.0A	16.0A
IRF512	3.5A	14.0A	20W	80	6.4	3.5A	14.0A
IRF513	3.5A	14.0A	20W	80	6.4	3.5A	14.0A

*I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRF510, IRF512	100			V	V_{GS} = 0, I_D = 250µA
		IRF511, IRF513	60				
$V_{GS(th)}$	Gate Threshold Voltage		2.0		4.0	V	V_{GS} = V_{DS}, I_D = 250µA
I_{GSS}	Gate Body Leakage				500	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				250	µA	V_{GS} = 0, V_{DS} = Max Rating
					1000		V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_C = 125°C
$I_{D(ON)}$	ON-State Drain Current	IRF510, IRF511	4.0			A	V_{GS} = 10V, V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max Rating
		IRF512, IRF513	3.5				
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	IRF510, IRF511			0.6	Ω	V_{GS} = 10V, I_D = 2.0A
		IRF512, IRF513			0.8		
G_{FS}	Forward Transconductance		1.0	1.5		℧	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max Rating, I_D = 2.0A
C_{ISS}	Input Capacitance				150	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance				100		
C_{RSS}	Reverse Transfer Capacitance				25		
$t_{d(ON)}$	Turn-ON Delay Time				20	ns	V_{DD} = 0.5BV_{DSS}, I_D = 2.0A, R_S = 50Ω
t_r	Rise Time				25		
$t_{d(OFF)}$	Turn-OFF Delay Time				25		
t_f	Fall Time				20		
V_{SD}	Diode Forward Voltage Drop	IRF510,IRF511			2.5	V	V_{GS} = 0, I_{SD} = 4.0A
		IRF512,IRF513			2.0		V_{GS} = 0, I_{SD} = 3.5A
t_{rr}	Reverse Recovery Time			230		ns	T_j = 150°C, I_{SD} = 4.0A, $dI_{F/dt}$ = 100A/µS

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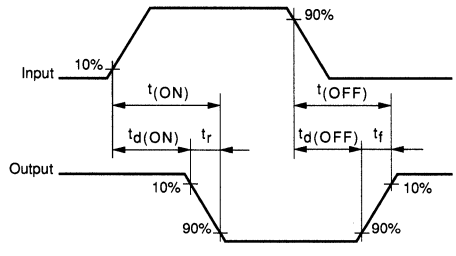
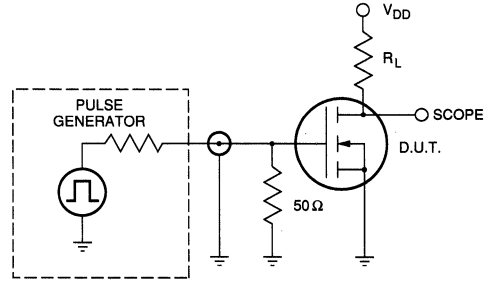
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Preliminary

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-220	TO-92
100V	0.3Ω	8.0A	IRF520	R520
60V	0.3Ω	8.0A	IRF521	R521
100V	0.4Ω	7.0A	IRF522	—
60V	0.4Ω	7.0A	IRF523	—

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
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8

Applications

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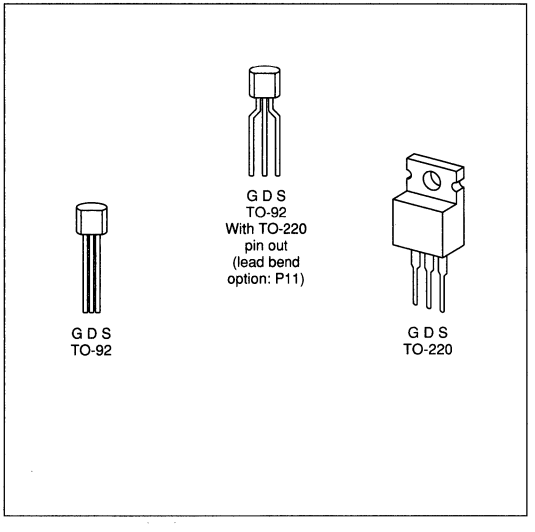
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options



Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
IRF520, IRF521	8.0A	32.0A	40W	80	3.12	8.0A	32.0A
IRF522, IRF523	7.0A	32.0A	40W	80	3.12	8.0A	32.0A
R520, R521	1.0A	9.0A	1W	170	125	1.0A	9.0A

*I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRF520, IRF522, R520	100			V	V_{GS} = 0, I_D = 250µA
		IRF521, IRF523, R521	60				
$V_{GS(th)}$	Gate Threshold Voltage		2.0		4.0	V	V_{GS} = V_{DS}, I_D = 250µA
I_{GSS}	Gate Body Leakage				500	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				250	µA	V_{GS} = 0, V_{DS} = Max Rating
					1000		V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_C = 125°C
$I_{D(ON)}$	ON-State Drain Current	IRF520, IRF521, R520, R521	8.0			A	V_{GS} = 10V, V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max Rating
		IRF522, IRF523	7.0				
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	IRF520, IRF521 R520, R521			0.3	Ω	V_{GS} = 10V, I_D = 4.0A
		IRF522, IRF523			0.4		
G_{FS}	Forward Transconductance		1.5	2.9		℧	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max Rating, I_D = 4.0A
C_{ISS}	Input Capacitance				600	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance				400		
C_{RSS}	Reverse Transfer Capacitance				100		
$t_{d(ON)}$	Turn-ON Delay Time				40	ns	V_{DD} = 0.5BV_{DSS}, I_D = 4.0A, V_{DS} = 0.8 Max Rating
t_r	Rise Time				70		
$t_{d(OFF)}$	Turn-OFF Delay Time				100		
t_f	Fall Time				70		
V_{SD}	Diode Forward Voltage Drop	IRF520, IRF521 R520, R521			2.5	V	V_{GS} = 0V, I_{SD} = 1A
		IRF522, IRF523			2.3		V_{GS} = 0V, I_{SD} = 8A
t_{rr}	Reverse Recovery Time			280		ns	T_j = 150°C, I_F = 8.0A, $dI_{F/dt}$ = 100A/µS

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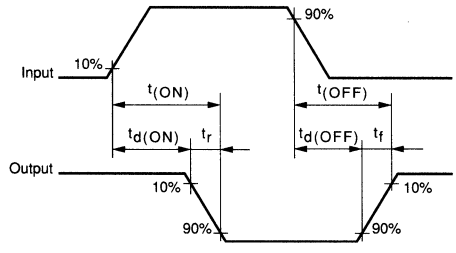
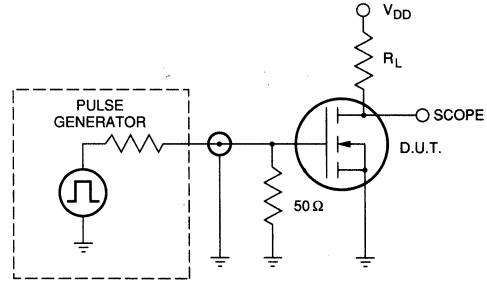
Switching Waveforms and Test Circuit





Preliminary

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
60V	0.18Ω	12.0A	IRF531	R531

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
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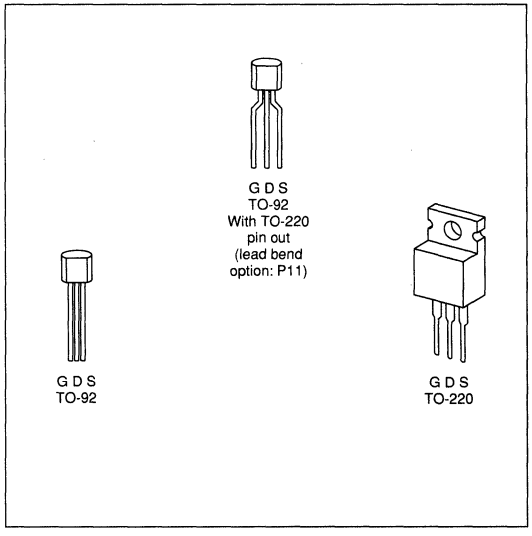
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options



Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
IRF531	14.0A	56.0A	75W	80	3.12	14.0A	56.0A
R531	1.5A	15.0A	1W	170	125	1.5A	15.0A

*I_D (continuous) is limited by max rated T_j.

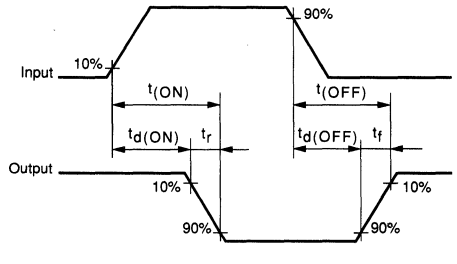
Electrical Characteristics (@ 25°C unless otherwise specified)

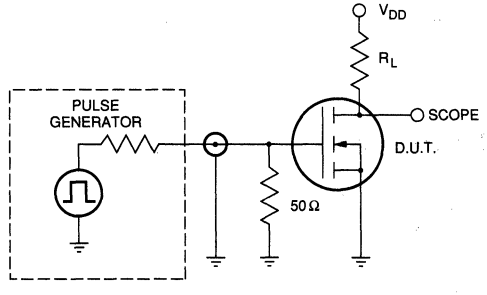
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60			V	V_{GS} = 0, I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	2.0		4.0	V	V_{GS} = V_{DS}, I_D = 250μA
I_{GSS}	Gate Body Leakage			500	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			250	μA	V_{GS} = 0, V_{DS} = Max Rating
				1000		V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	12.0			A	V_{GS} = 10V, V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max Rating
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			0.18	Ω	V_{GS} = 10V, I_D = 8.0A
G_{FS}	Forward Transconductance	4.0			℧	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max Rating, I_D = 8.0A
C_{ISS}	Input Capacitance			800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			500		
C_{RSS}	Reverse Transfer Capacitance			150		
$t_{d(ON)}$	Turn-ON Delay Time			30	ns	V_{DD} = 0.5BV_{DSS}, I_D = 4.0A, V_{DS} = 0.8 Max Rating
t_r	Rise Time			75		
$t_{d(OFF)}$	Turn-OFF Delay Time			40		
t_f	Fall Time			45		
V_{SD}	Diode Forward Voltage Drop			2.5	V	V_{GS} = 0V, I_{SD} = 1A
				2.3		V_{GS} = 0V, I_{SD} = 8A
t_{rr}	Reverse Recovery Time		360		ns	T_j = 150°C, I_F = 8.0A, $dI_{F/dt}$ = 100A/μS

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package							
			TO-39	TO-92	TO-52	TO-220	Quad P-DIP	Quad C-DIP	Quad C-LCC	DICE
40V	3Ω	2.0A	VN0104N2	VN0104N3	VN0104N9	VN0104N5	VN0104N6	VN0104N7	—	VN0104ND
60V	3Ω	2.0A	VN0106N2	VN0106N3	VN0106N9	VN0106N5	VN0106N6	VN0106N7	VN0106NE	VN0106ND
90V	3Ω	2.0A	VN0109N2	VN0109N3	VN0109N9	VN0109N5	—	—	VN0109NE	VN0109ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

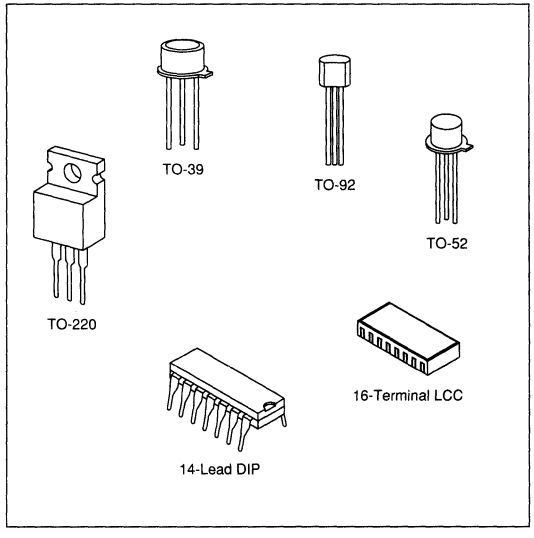
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options



Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-39	0.8A	2.5A	3.5W	125	35	0.08A	2.5A
TO-92	0.5A	2.0A	1.0W	170	125	0.5A	2.0A
TO-52	0.5A	2.0A	1.0W	170	125	0.5A	2.0A
TO-220	1.5A	2.5A	15.0W	70	8	1.5A	2.5A
Plastic DIP Ceramic DIP Ceramic LCC	See DMOS Arrays & Special Functions section						

* I_D (continuous) is limited by max rated T_j.

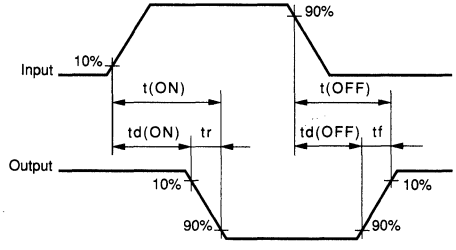
Electrical Characteristics (@ 25°C unless otherwise specified)

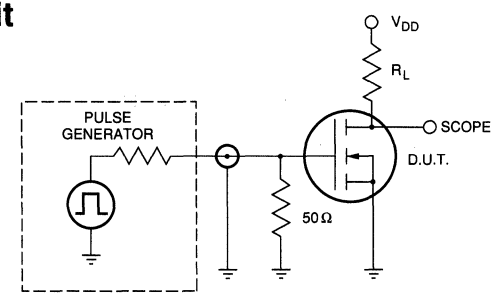
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0109	90			V	V_{GS} = 0, I_D = 1mA
		VN0106	60				
		VN0104	40				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	V_{GS} = V_{DS}, I_D = 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.5	mV/°C	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage			0.1	100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				1	µA	V_{GS} = 0, V_{DS} = Max Rating
					100		V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		0.5	1.0		A	V_{GS} = 5V, V_{DS} = 25V
			2.0	2.50			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			4.50	5	Ω	V_{GS} = 5V, I_D = 250mA
				2	3		V_{GS} = 10V, I_D = 1A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.70	1	%/°C	V_{GS} = 10V, I_D = 1A
G_{FS}	Forward Transconductance		300	400		m℧	V_{DS} = 25V, I_D = 0.5A
C_{ISS}	Input Capacitance			45	60	pF	V_{GS} = 0, V_{DS} = 25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			20	25		
C_{RSS}	Reverse Transfer Capacitance			2	5		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	V_{DD} = 25V I_D = 1A R_S = R_L = 50Ω
t_r	Rise Time			5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			6	9		
t_f	Fall Time			5	8		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	V_{GS} = 0, I_{SD} = 2.5A
t_{rr}	Reverse Recovery Time			400		ns	V_{GS} = 0, I_{SD} = 1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

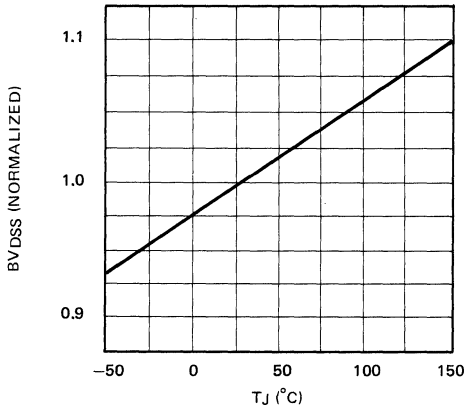
Switching Waveforms and Test Circuit



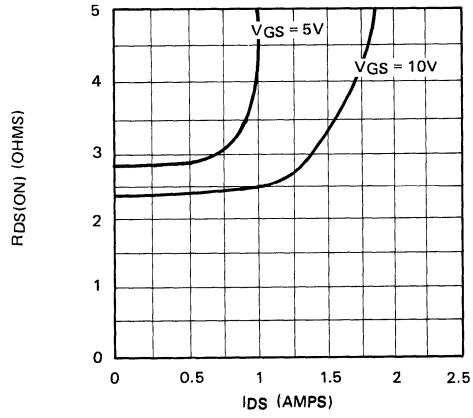


Typical Performance Curves

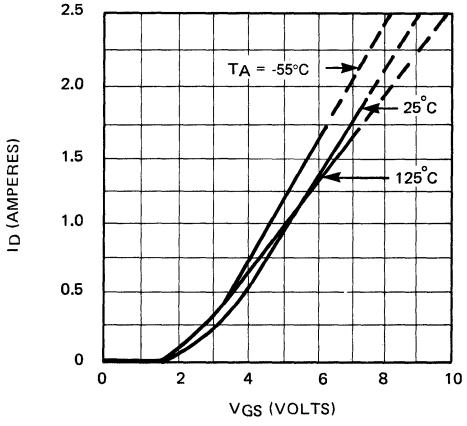
BVDSS Variation with Temperature



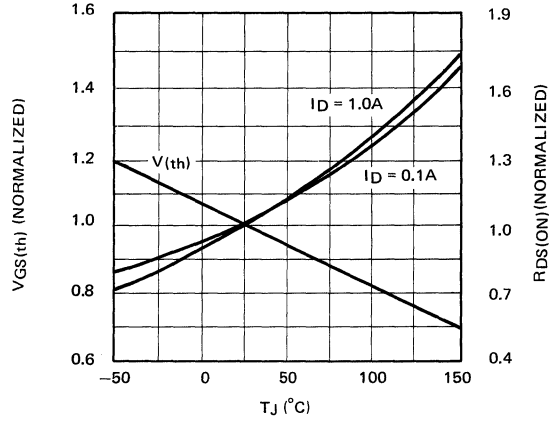
ON – Resistance Vs. Drain Current



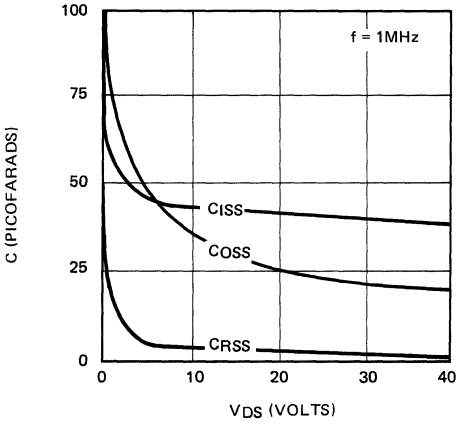
Transfer Characteristics



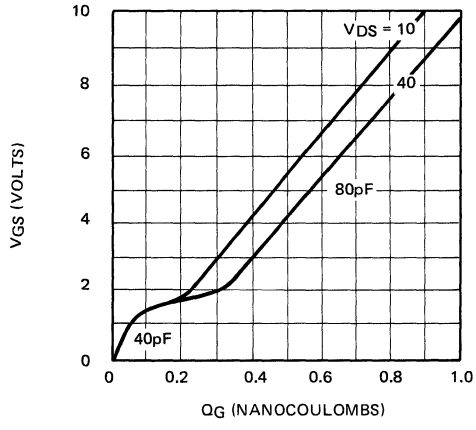
V(th) and RDS Variation with Temperature



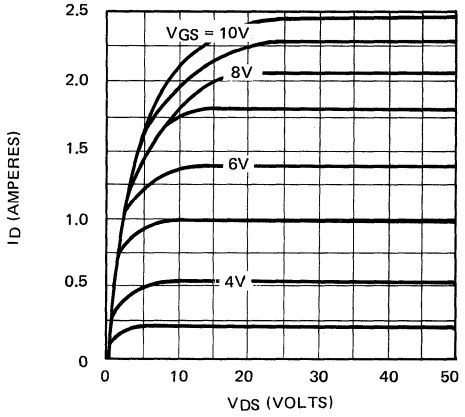
Capacitance Vs. Drain-to-Source Voltage



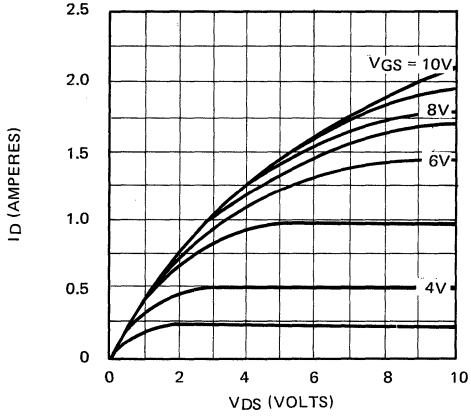
Gate Drive Dynamic Characteristics



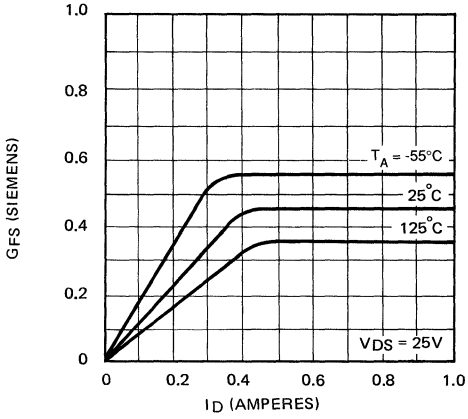
Output Characteristics



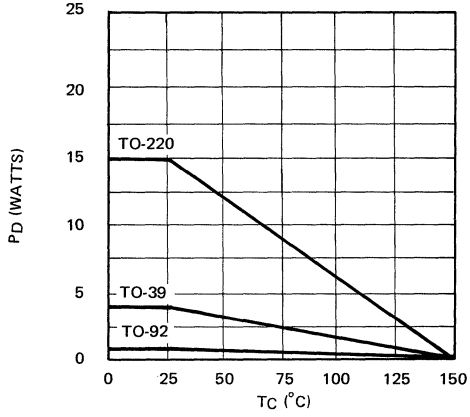
Saturation Characteristics



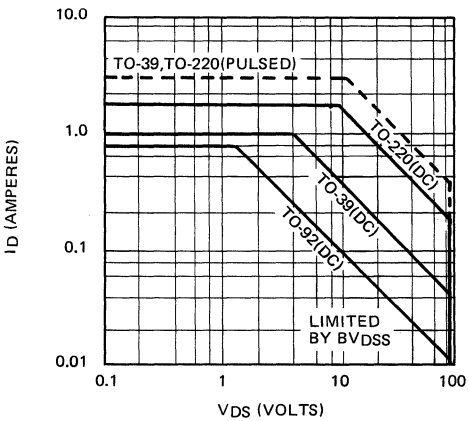
Transconductance Vs. Drain Current



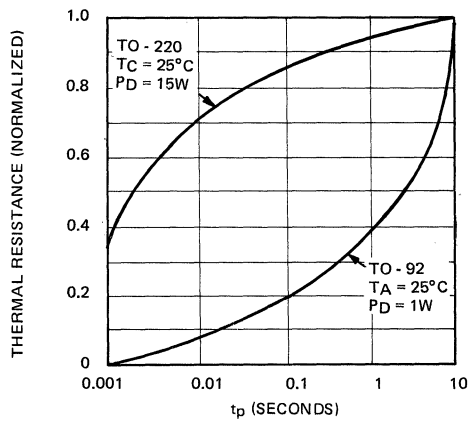
Power Dissipation Vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-39	TO-92	TO-220	Dice
160V	10Ω	0.4A	VN0116N2	VN0116N3	VN0116N5	VN0116ND
200V	10Ω	0.4A	VN0120N2	VN0120N3	VN0120N5	VN0120ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

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These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

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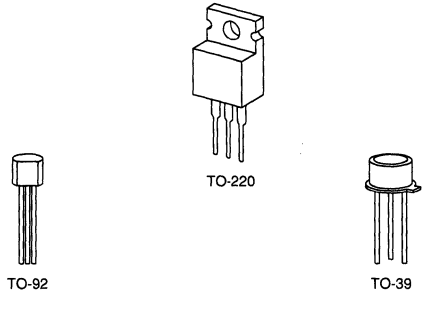
Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-39	350mA	1.0A	3.5W	125	35	350mA	1.0A
TO-92	250mA	0.9A	1.0W	170	125	250mA	0.9A
TO-220	700mA	1.2A	15.0W	70	8.3	700mA	1.2A

* I_D (continuous) is limited by max rated T_j.

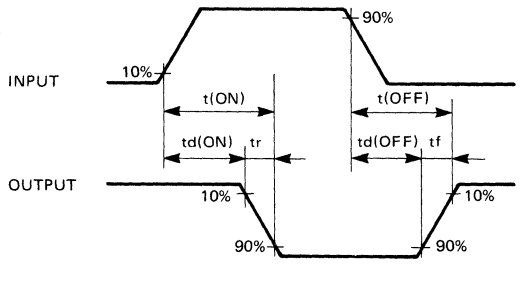
Electrical Characteristics (@ 25°C unless otherwise specified)

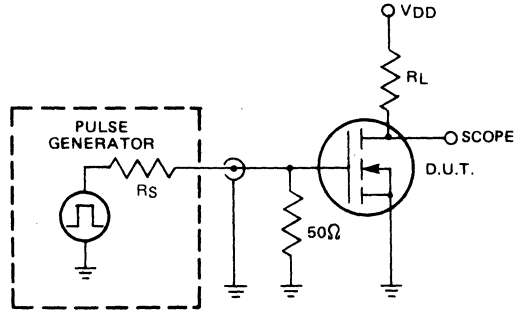
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BVDSS	Drain-to-Source Breakdown Voltage	VN0120	200			V	ID = 1mA, VGS = 0
		VN0116	160				
VGS(th)	Gate Threshold Voltage		1		3	V	VGS = VDS, ID = 1mA
ΔVGS(th)	Change in VGS(th) with Temperature			−5.1	−6.0	mV/°C	VGS = VDS , ID = 1mA
IGSS	Gate Body Leakage			0.1	100	nA	VGS = ±20V, VDS = 0
IDSS	Zero Gate Voltage Drain Current				10	μA	VGS = 0, VDS = Max Rating
					1	mA	VGS = 0, VDS = 0.8 Max Rating, TA = 125°C
ID(ON)	ON-State Drain Current		0.3	0.5		A	VGS = 5V, VDS = 25V
			0.4	0.8			VGS = 10V, VDS = 25V
RDS(ON)	Static Drain-to-Source ON-State Resistance			10	15	Ω	VGS = 5V, ID = 100mA,
				8	10		VGS = 10V, ID = 100mA,
ΔRDS(ON)	Change in RDS(ON) with Temperature			1.0	1.2	%/°C	ID = 500mA, VGS = 10V
GFS	Forward Transconductance		100	150		m℧	VDS = 25V, ID = 250mA
CISS	Input Capacitance			40	55	pF	VGS = 0, VDS = 25V, f = 1MHz
COSS	Common Source Output Capacitance			20	30		
CRSS	Reverse Transfer Capacitance			5	8		
td(ON)	Turn-ON Delay Time			3	5	ns	VDD = 25V, ID = 250mA, RS = 50Ω
tr	Rise Time			5	8		
td(OFF)	Turn-OFF Delay Time			6	9		
tf	Fall Time			5	8		
VSD	Diode Forward Voltage Drop			1.2	1.8	V	ISD = 2.5A, VGS = 0
trr	Reverse Recovery Time			400		ns	ISD = 1A, VGS = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

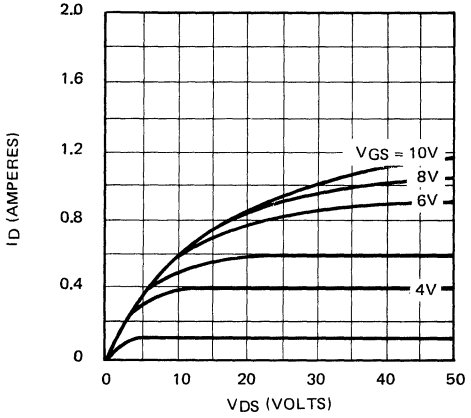
Switching Waveforms and Test Circuit



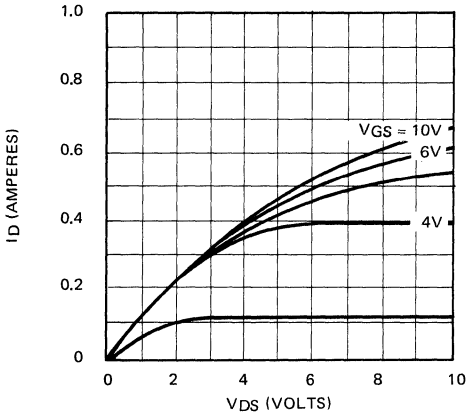


Typical Performance Curves

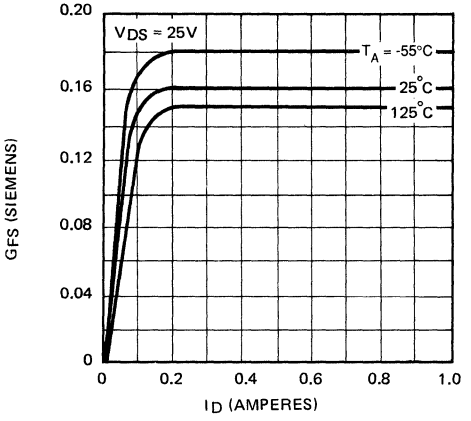
Output Characteristics



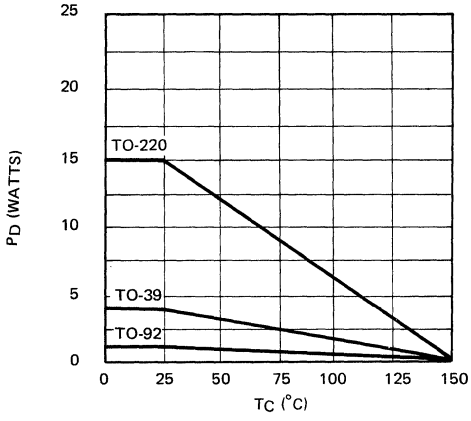
Saturation Characteristics



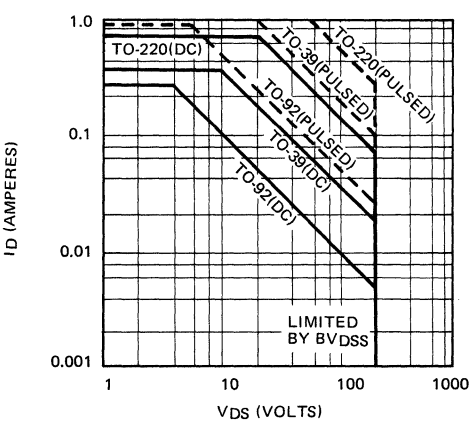
Transconductance Vs. Drain Current



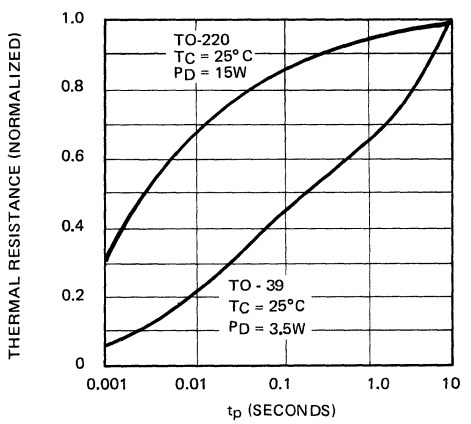
Power Dissipation Vs. Case Temperature



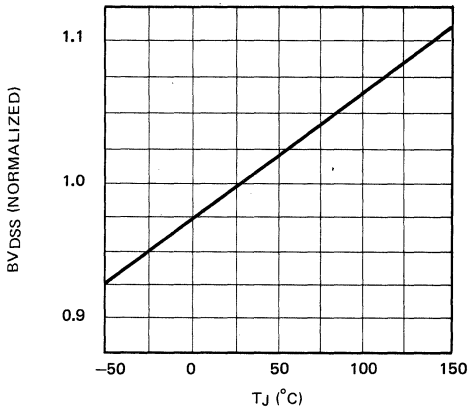
Maximum Rated Safe Operating Area



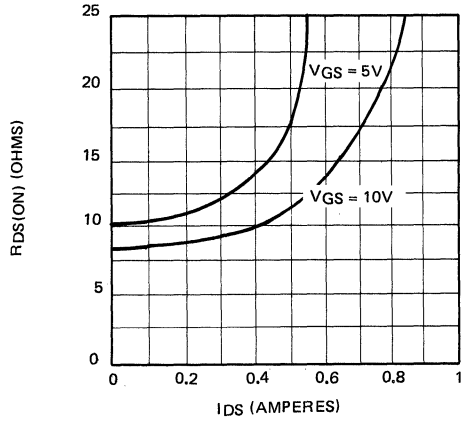
Thermal Response Characteristics



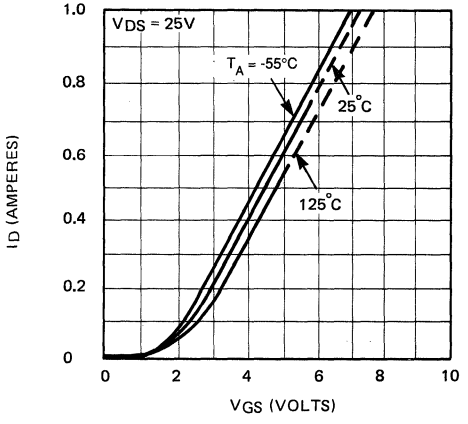
BVDSS Variation with Temperature



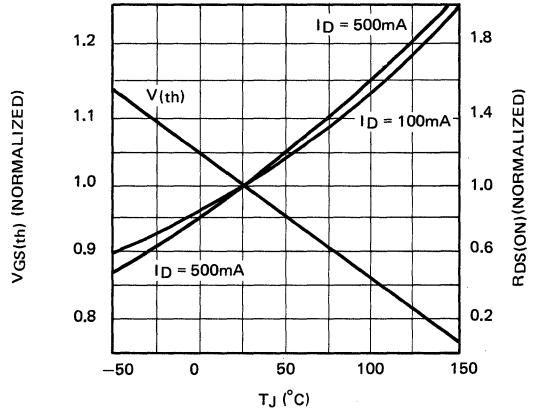
ON - Resistance Vs .Drain Current



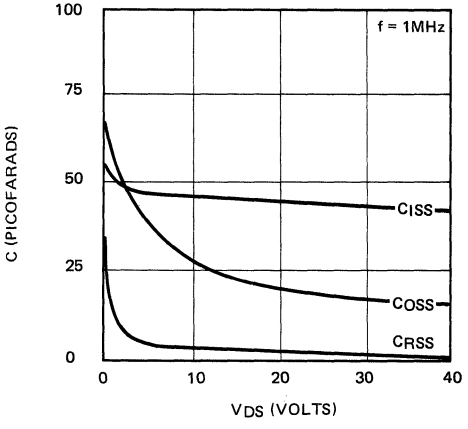
Transfer Characteristics



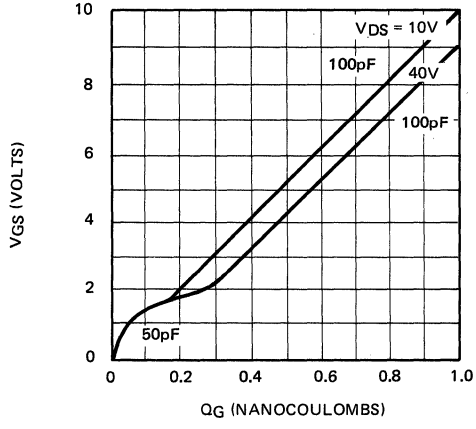
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package				
			TO-39	TO-92	TO-220	Quad P-DIP	Quad C-DIP
40V	2Ω	3.0A	VN0204N2	—	VN0204N5	VN0240N6	VN0204N7
60V	2Ω	3.0A	VN0206N2	VN0206N3	VN0206N5	VN0206N6	VN0206N7
100V	2Ω	3.0A	VN0210N2	VN0210N3	VN0210N5	—	—

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

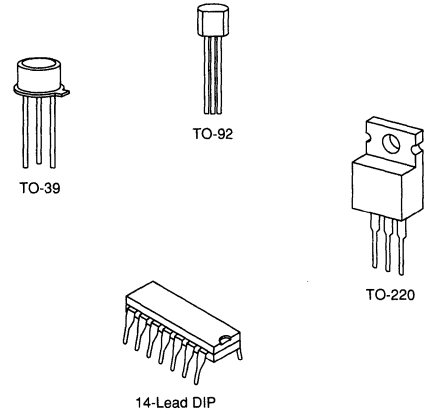
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	1.5A	4A	4W	25	125	2A	4A
TO-92	0.8A	4A	1W	125	170	0.8A	4A
TO-220	3.0A	4A	28W	4.8	70	3A	4A
Plastic Dip	Refer to Arrays and Special Functions section.						
Ceramic Dip							

*I_D (continuous) is limited by max rated T_j.

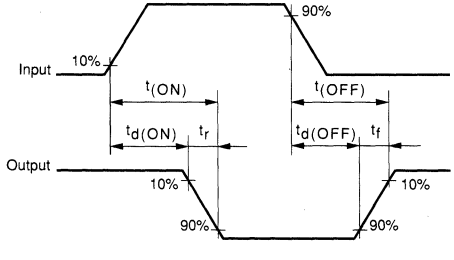
Electrical Characteristics (@ 25°C unless otherwise specified)

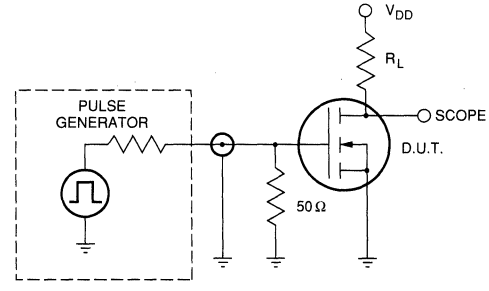
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0204	40			V	V_{GS} = 0, I_D = 2.5mA
		VN0206	60				
		VN0210	100				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	V_{GS} = V_{DS}, I_D = 2.5mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-4.5	mV/°C	V_{GS} = V_{DS}, I_D = 2.5mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				25	µA	V_{GS} = 0, V_{DS} = Max Rating
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		1.2	1.6		A	V_{GS} = 5V, V_{DS} = 25V
			3.0	4.0			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			1.6	2.5	Ω	V_{GS} = 5V, I_D = 1A
				1.5	2		V_{GS} = 10V, I_D = 2A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.5	0.75	%/°C	V_{GS} = 10V, I_D = 2A
G_{FS}	Forward Transconductance		0.4	0.65		℧	V_{DS} = 25V, I_D = 2A
C_{ISS}	Input Capacitance			85	150	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	85		
C_{RSS}	Reverse Transfer Capacitance			12	35		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = 25V, I_D = 0.5A, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				25		
t_f	Fall Time				13		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	V_{GS} = 0, I_{SD} = 1.5A
t_{rr}	Reverse Recovery Time			330		ns	V_{GS} = 0, I_{SD} = 1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

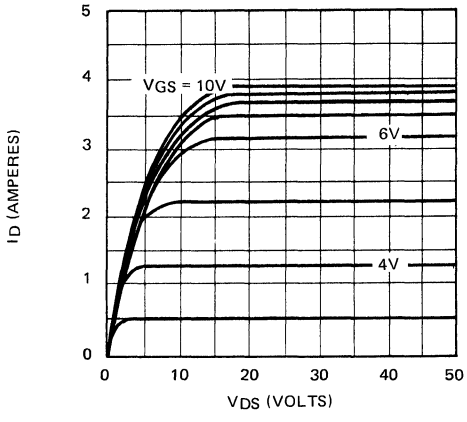
Switching Waveforms and Test Circuit



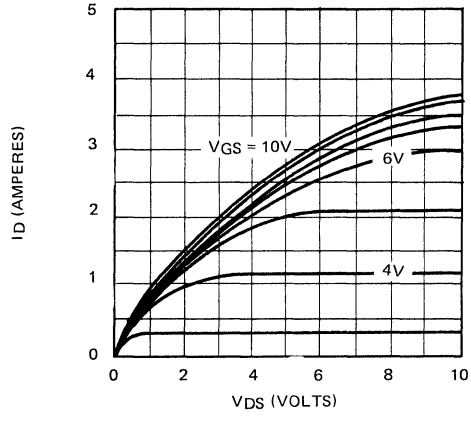


Typical Performance Curves

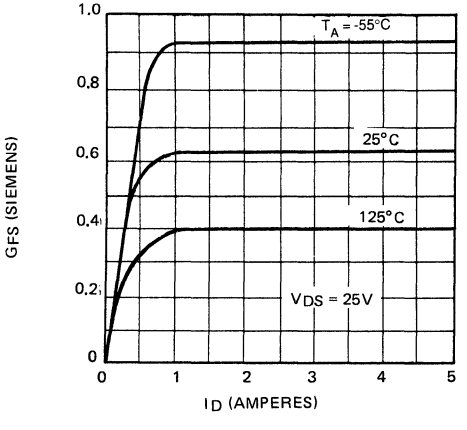
Output Characteristics



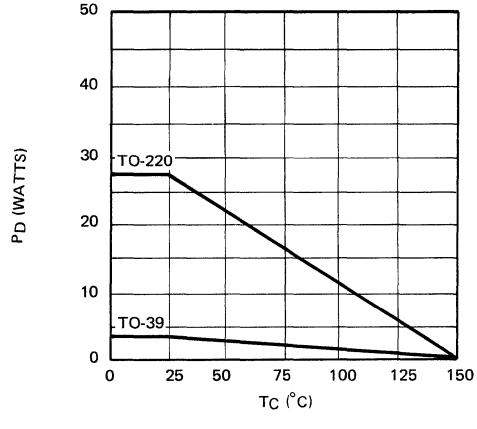
Saturation Characteristics



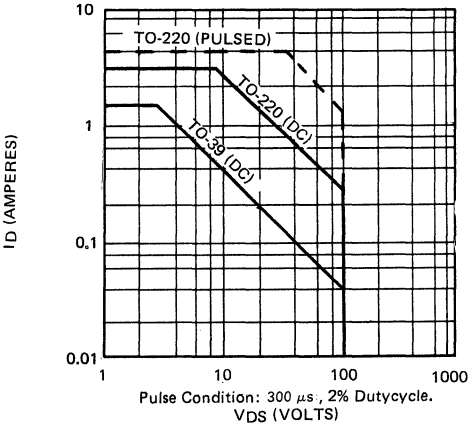
Transconductance Vs. Drain Current



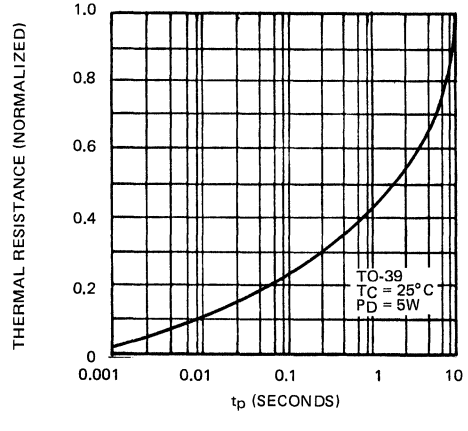
Power Dissipation Vs. Case Temperature



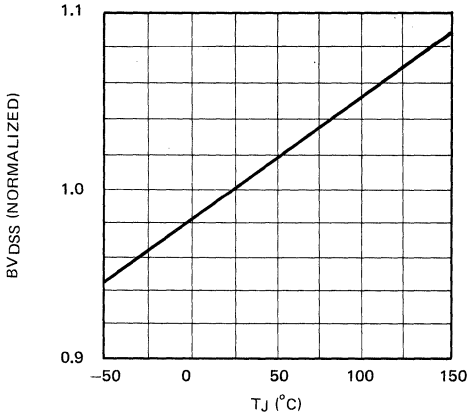
Maximum Rated Safe Operating Area



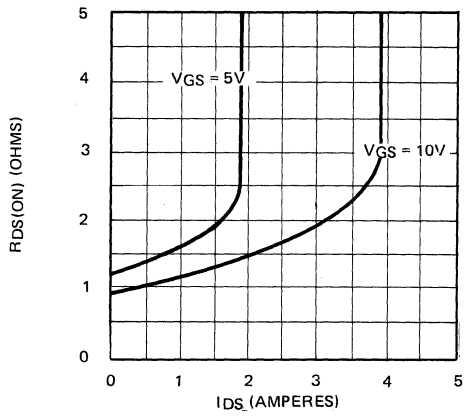
Thermal Response Characteristics



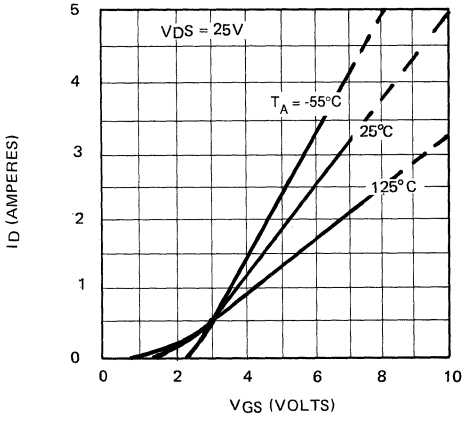
BVDSS Variation with Temperature



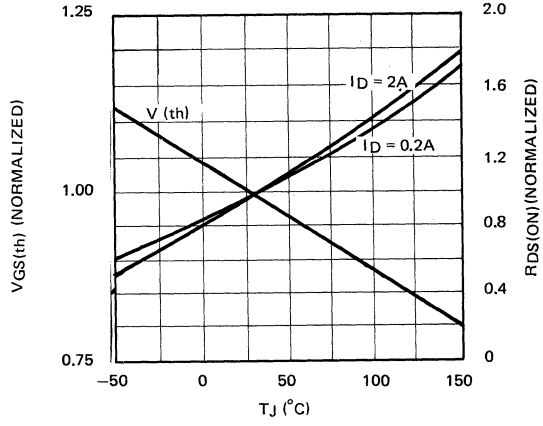
ON - Resistance Vs. Drain Current



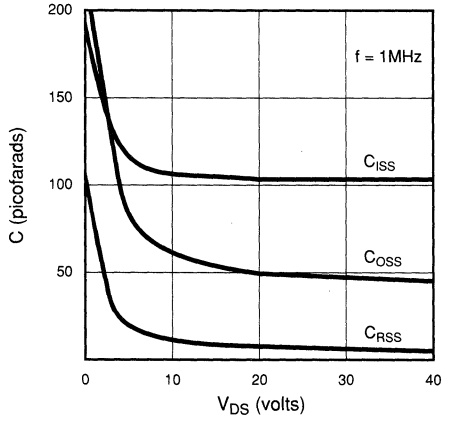
Transfer Characteristics



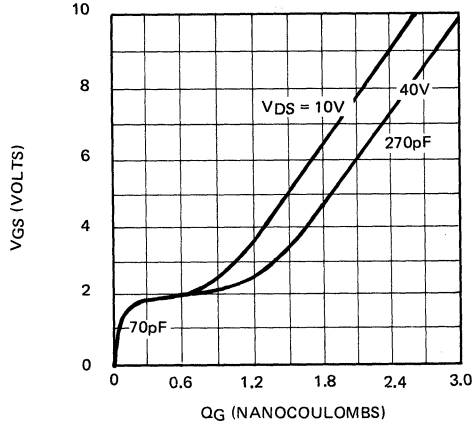
V(th) and RDS Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	TO-220
160V	6Ω	1A	VN0216N2	VN0216N3	VN0216N5
200V	6Ω	1A	VN0220N2	VN0220N3	VN0220N5

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

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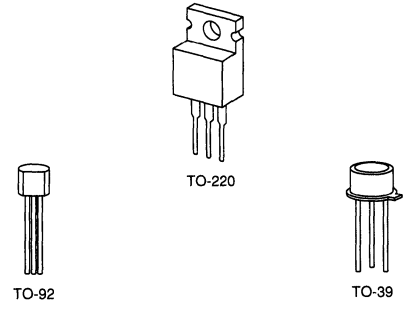
Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-39	0.7A	2.5A	4W	125	32	0.7A	2.5A
TO-92	0.4A	2.5A	1W	170	125	0.5A	2.5A
TO-220	1.5A	2.5A	28W	70	4.6	1.7A	2.5A

* I_D (continuous) is limited by max rated T_j.

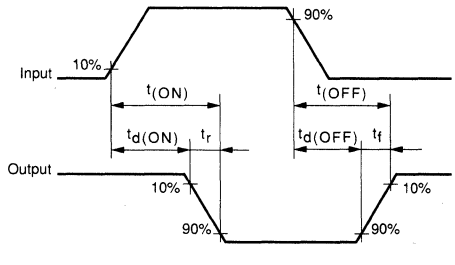
Electrical Characteristics (@ 25°C unless otherwise specified)

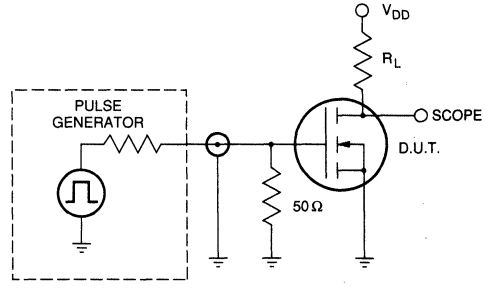
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0216	160			V	V_{GS} = 0, I_D = 2.0mA
		VN0220	200				
$V_{GS(th)}$	Gate Threshold Voltage		0.75		3	V	V_{GS} = V_{DS}, I_D = 2.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.6	-5.5	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				25	µA	V_{GS} = 0, V_{DS} = Max Rating
					2.5	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		0.5	1.3		A	V_{GS} = 5V, V_{DS} = 25V
			1.0	2.2			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5.0	8	Ω	V_{GS} = 5V, I_D = 0.5A
				4.0	6		V_{GS} = 10V, I_D = 0.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.8	1.4	%/°C	V_{GS} = 10V, I_D = 500mA
G_{FS}	Forward Transconductance		0.3	0.7		℧	V_{DS} = 25V, I_D = 1A
C_{ISS}	Input Capacitance			75	150	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			34	85		
C_{RSS}	Reverse Transfer Capacitance			15	35		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = 25V, I_D = 0.5A, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				20		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	V_{GS} = 0, I_{SD} = 1A
t_{rr}	Reverse Recovery Time			430		ns	V_{GS} = 0, I_{SD} = 1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

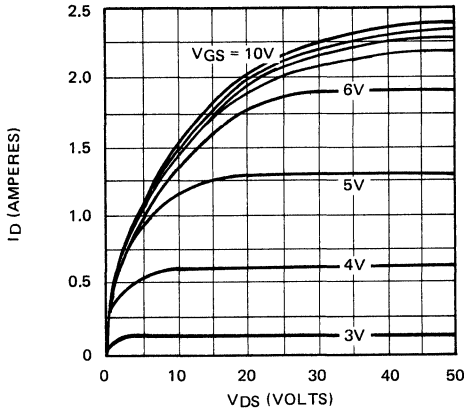
Switching Waveforms and Test Circuit



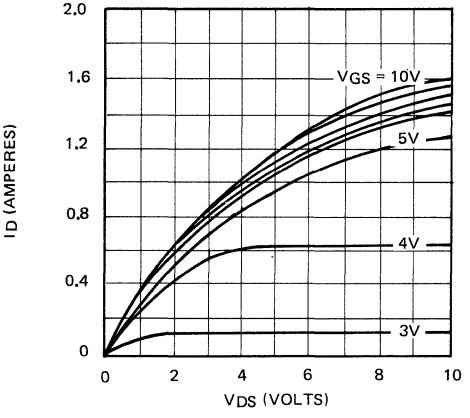


Typical Performance Curves

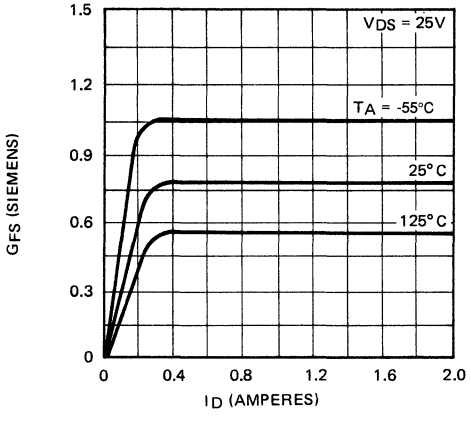
Output Characteristics



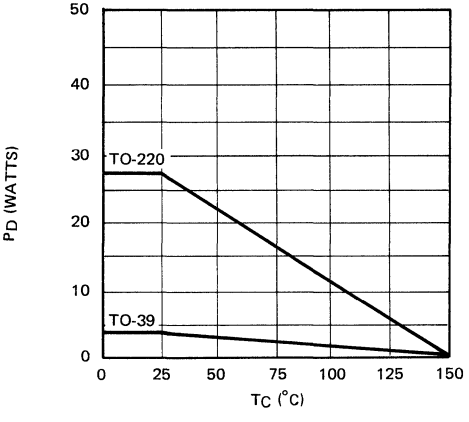
Saturation Characteristics



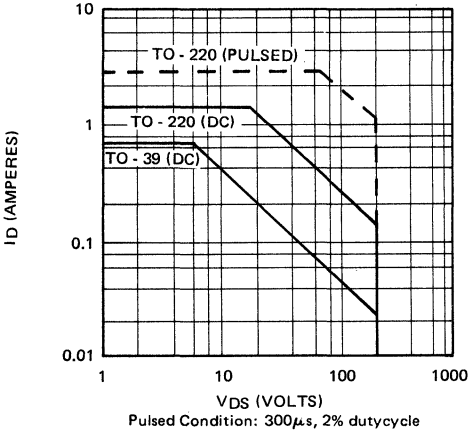
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

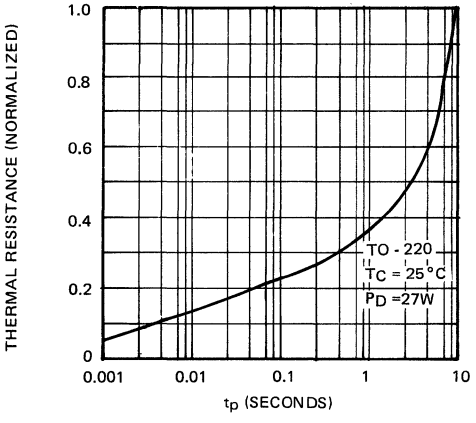


Maximum Rated Safe Operating Area

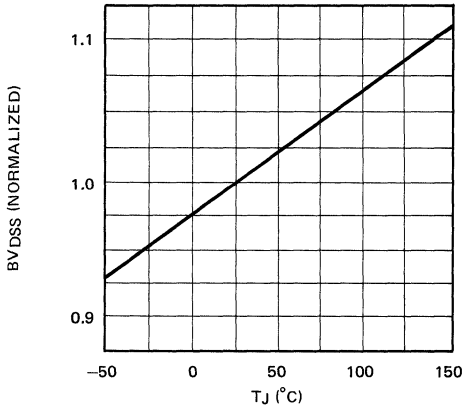


Pulsed Condition: 300μs, 2% dutycycle

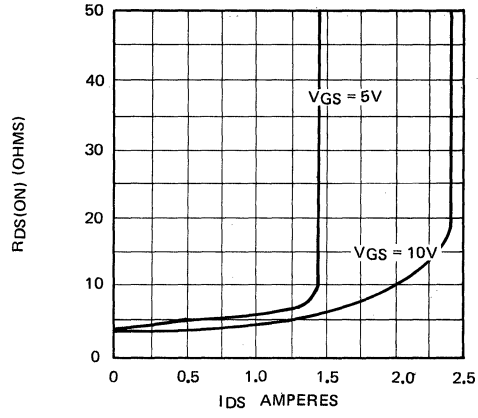
Thermal Response Characteristics



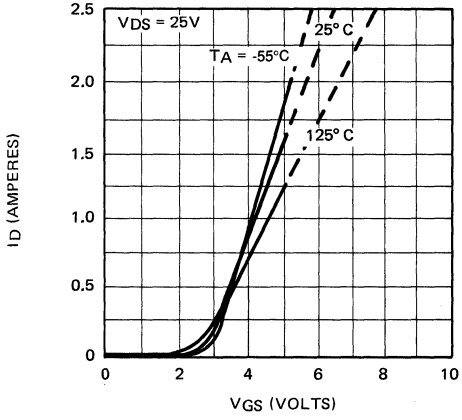
BVDSS Variation with Temperature



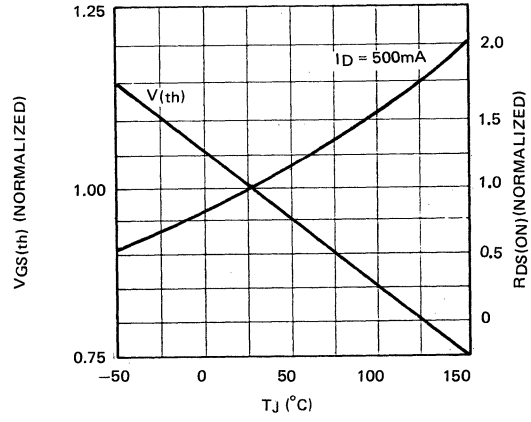
ON - Resistance Vs. Drain Current



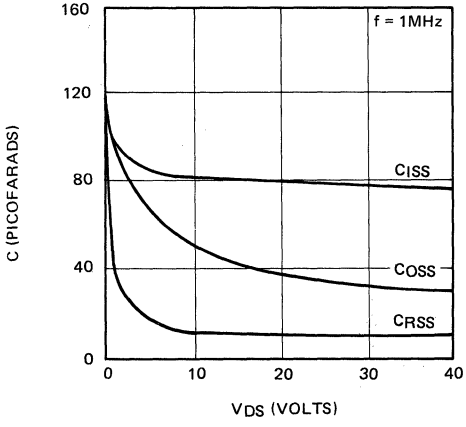
Transfer Characteristics



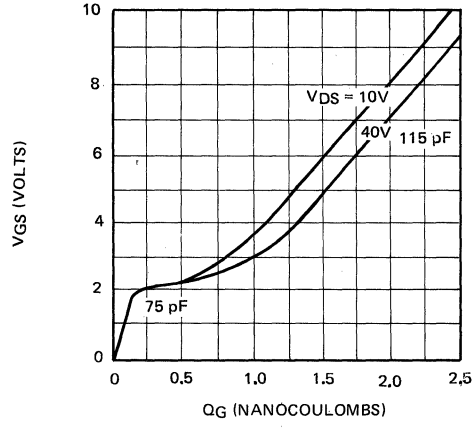
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	Dice
350V	2.5Ω	3A	VN0335N1	VN0335N2	VN0335N5	VN0335ND
400V	2.5Ω	3A	VN0340N1	VN0340N2	VN0340N5	VN0340ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

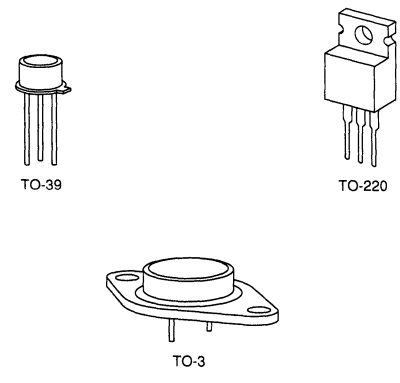
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-3	3.5A	8A	100W	30	1.25	3.5	8A
TO-39	1.0A	7A	6W	125	20.8	1.0	7A
TO-220	2.1A	8A	50W	40	2.5	2.1	8A

*I_D (continuous) is limited by max rated T_j.

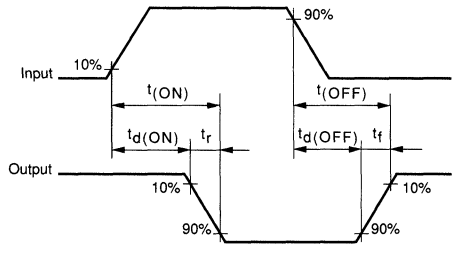
Electrical Characteristics (@ 25°C unless otherwise specified)

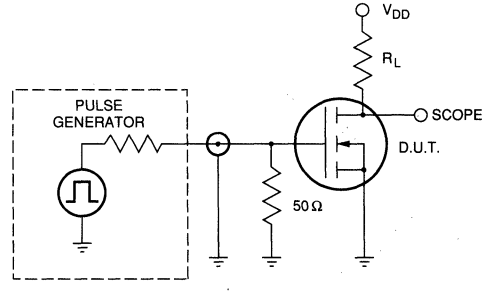
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0340	400			V	V_{GS} = 0, I_D = 10mA
		VN0335	350				
$V_{GS(th)}$	Gate Threshold Voltage		2		4	V	V_{GS} = V_{DS}, I_D = 10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.8	-6	mV/°C	V_{GS} = V_{DS}, I_D = 10mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				100	µA	V_{GS} = 0, V_{DS} = Max Rating
					2	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			4.5		A	V_{GS} = 5V, V_{DS} = 25V
			3	6			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			2.2		Ω	V_{GS} = 5V, I_D = 0.5A
				1.8	2.5		V_{GS} = 10V, I_D = 1A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1	2	%/°C	V_{GS} = 10V, I_D = 1A
G_{FS}	Forward Transconductance		1	1.5		℧	V_{DS} = 25V, I_D =1A
C_{ISS}	Input Capacitance			550	650	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			75	125		
C_{RSS}	Reverse Transfer Capacitance			25	50		
$t_{d(ON)}$	Turn-ON Delay Time			12	20	ns	V_{DD} = 25V, I_D = 1A, R_S = 50Ω
t_r	Rise Time			12	20		
$t_{d(OFF)}$	Turn-OFF Delay Time			65	100		
t_f	Fall Time			20	30		
V_{SD}	Diode Forward Voltage Drop			1.1	1.5	V	V_{GS} = 0, I_{SD} = 5A
t_{rr}	Reverse Recovery Time			450		ns	V_{GS} = 0, I_{SD} = 1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

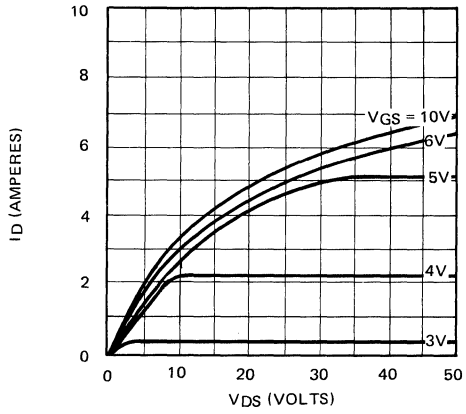
Switching Waveforms and Test Circuit



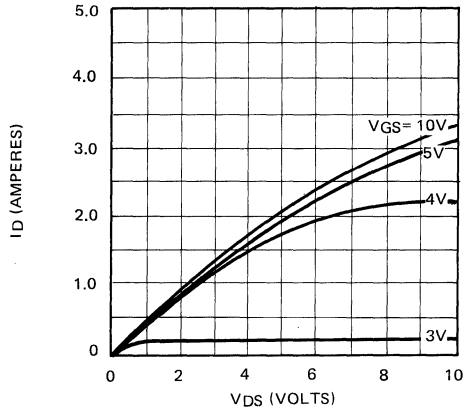


Typical Performance Curves

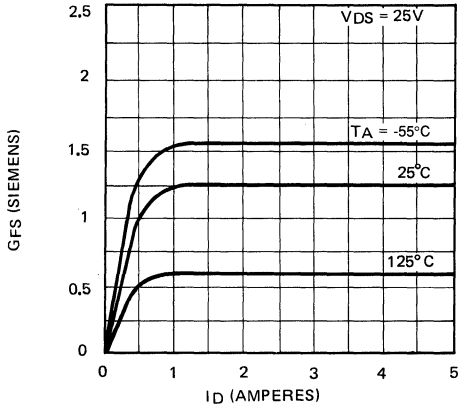
Output Characteristics



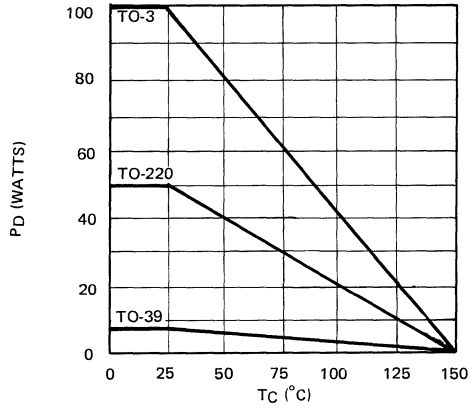
Saturation Characteristics



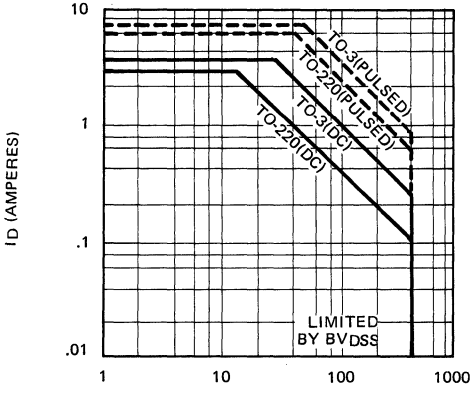
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

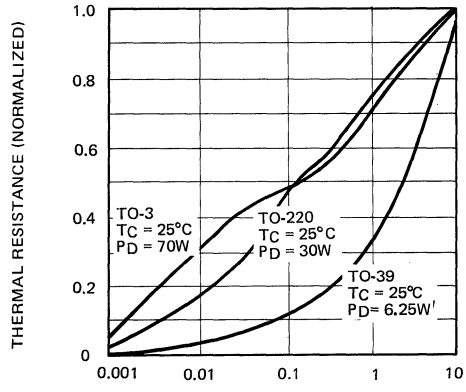


Maximum Rated Safe Operating Area



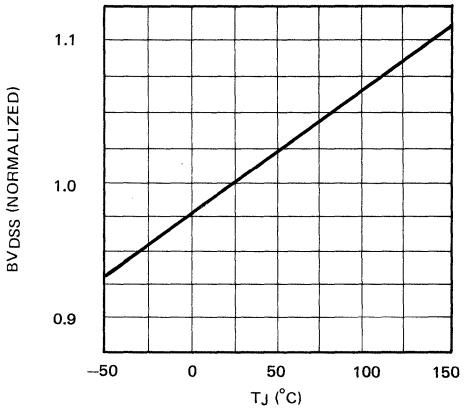
Pulse Condition: 300μs, 2% dutycycle.

Thermal Response Characteristics

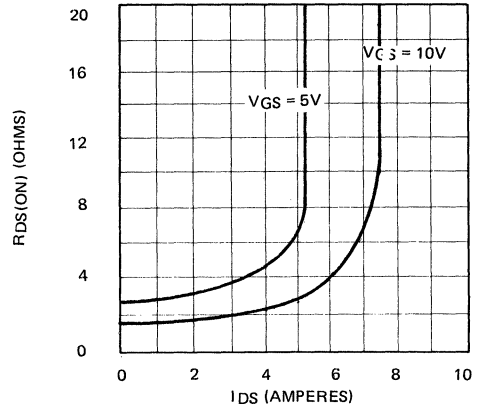


8

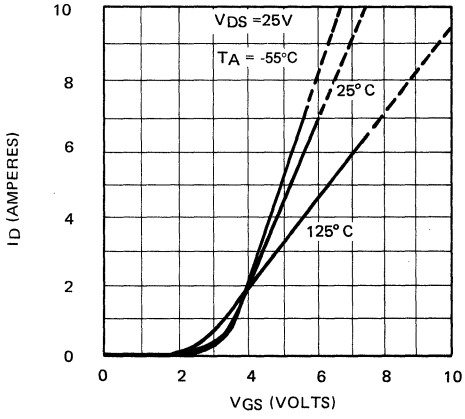
BVDSS Variation with Temperature



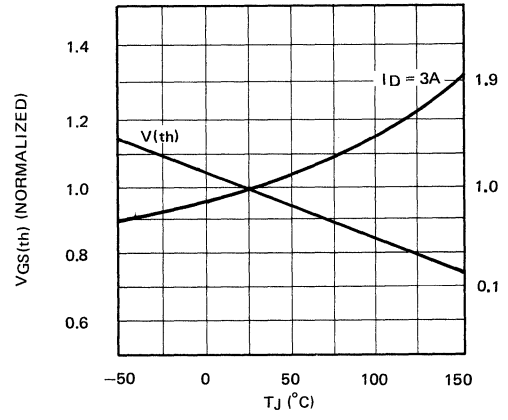
ON - Resistance Vs. Drain Current



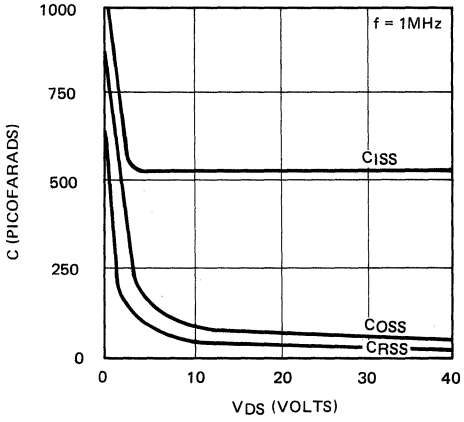
Transfer Characteristics



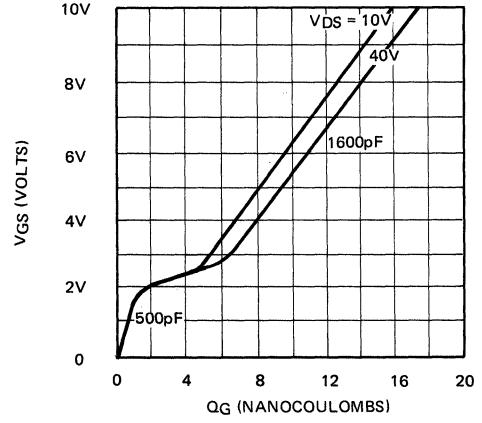
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	Dice
450V	4Ω	2A	VN0345N1	VN0345N2	VN0345N5	VN0345ND
500V	4Ω	2A	VN0350N1	VN0350N2	VN0350N5	VN0350ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

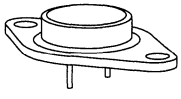
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

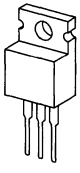
Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

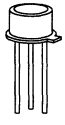
Package Options (Note 1)



TO-3



TO-220



TO-39

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-3	2.5A	5.0A	100W	1.25	30	2.5A	5.0A
TO-39	0.35A	4.5A	6W	20.8	125	0.35A	4.5A
TO-220	1.5A	5.0A	50W	2.5	40	1.5A	5.0A

*I_D (continuous) is limited by max rated T_j.

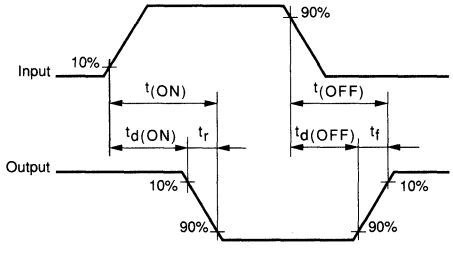
Electrical Characteristics (@ 25°C unless otherwise specified)

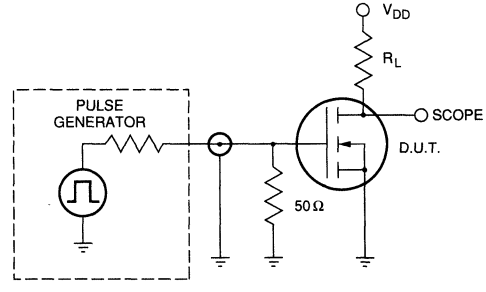
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0350	500			V	V_{GS} = 0, I_D = 10mA
		VN0345	450				
$V_{GS(th)}$	Gate Threshold Voltage		2		4	V	V_{GS} = V_{DS}, I_D = 10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-7	-9	mV/°C	V_{GS} = V_{DS}, I_D = 10mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				100	µA	V_{GS} = 0, V_{DS} = Max Rating
					2	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			3.5		A	V_{GS} = 5V, V_{DS} = 25V
			2	4.5			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.5		Ω	V_{GS} = 5V, I_D = 0.5A
				2.8	4		V_{GS} = 10V, I_D = 0.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1	1.5	%/°C	V_{GS} = 10V, I_D = 0.5A
G_{FS}	Forward Transconductance		500	1000		m℧	V_{DS} = 25V, I_D =0.5A
C_{ISS}	Input Capacitance			550	650	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	75		
C_{RSS}	Reverse Transfer Capacitance			15	25		
$t_{d(ON)}$	Turn-ON Delay Time			8	15	ns	V_{DD} = 25V, I_D = 1A, R_S = 50Ω
t_r	Rise Time			8	15		
$t_{d(OFF)}$	Turn-OFF Delay Time			65	100		
t_f	Fall Time			15	25		
V_{SD}	Diode Forward Voltage Drop			1.3	1.8	V	V_{GS} = 0, I_{SD} = 1A
t_{rr}	Reverse Recovery Time			450		ns	V_{GS} = 0, I_{SD} = 0.5A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

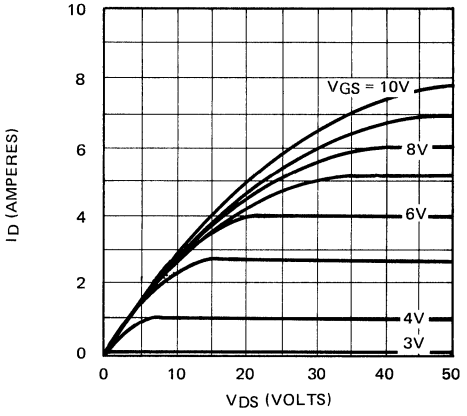
Switching Waveforms and Test Circuit



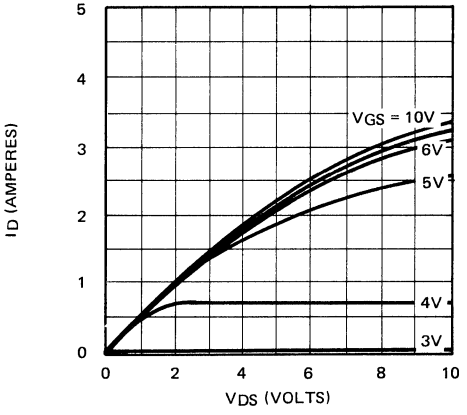


Typical Performance Curves

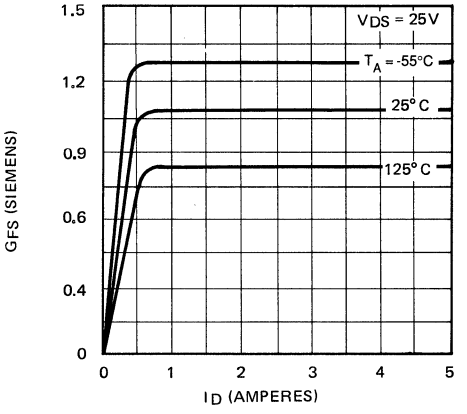
Output Characteristics



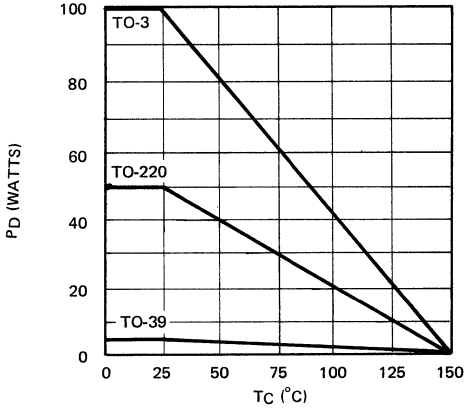
Saturation Characteristics



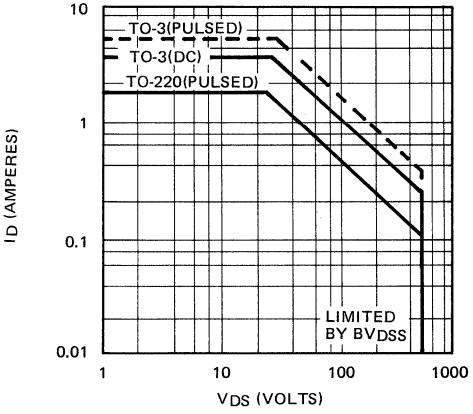
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

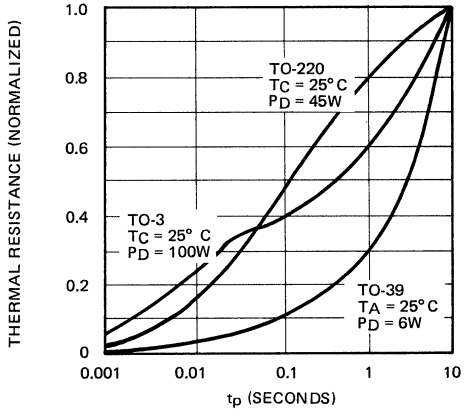


Maximum Rated Safe Operating Area

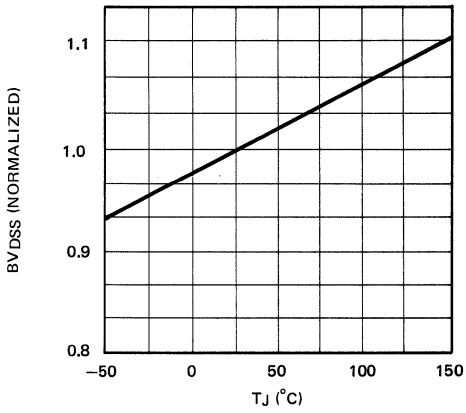


Pulse Condition: 300 μs, 2% dutycycle.

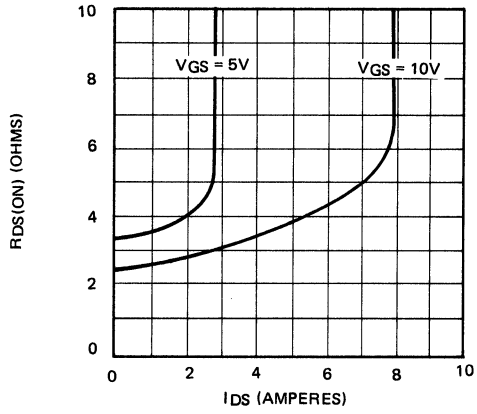
Thermal Response Characteristics



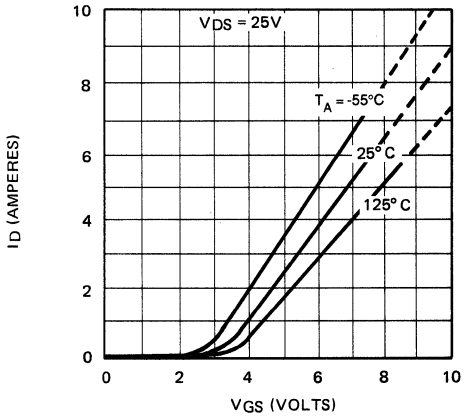
BVDSS Variation with Temperature



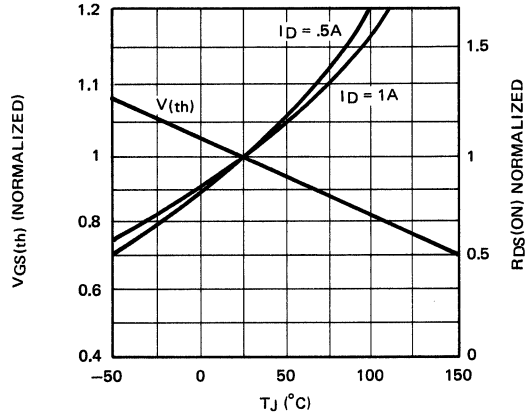
ON - Resistance Vs. Drain Current



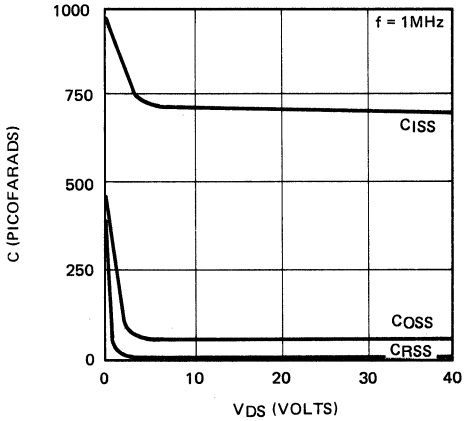
Transfer Characteristics



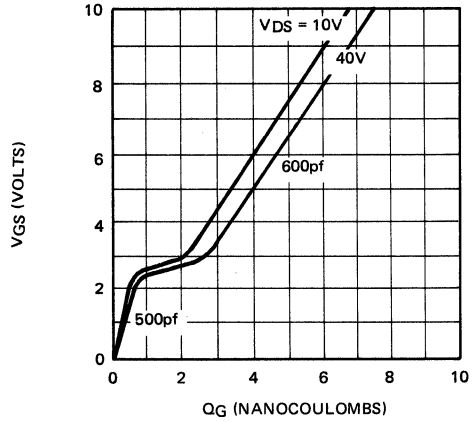
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-3	TO-220	Dice
550V	6Ω	1.5A	VN0335N1	VN0335N5	VN0335ND
600V	6Ω	1.5A	VN0360N1	VN0360N5	VN0360ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

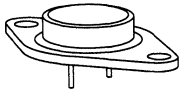
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

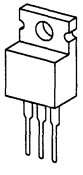
Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-3



TO-220

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-3	2.5A	6A	100W	1.25	30	2.5A	6A
TO-220	1.5A	6A	50W	40	40	1.5A	6A

*I_D (continuous) is limited by max rated T_j.

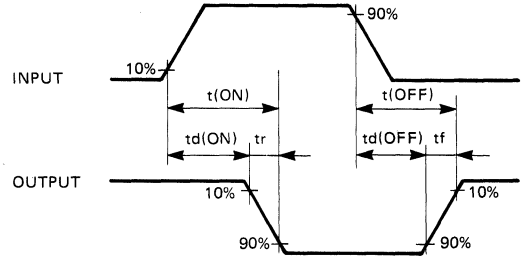
Electrical Characteristics (@ 25°C unless otherwise specified)

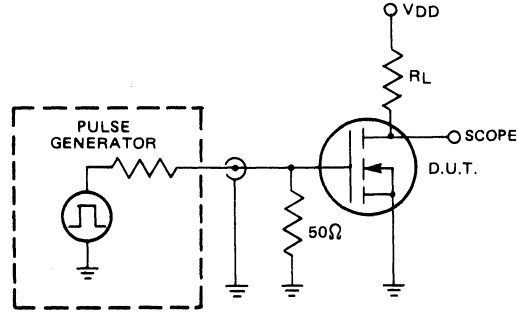
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BVDSS	Drain-to-Source Breakdown Voltage	VN0360	600			V	VGS= 0, ID = 10mA
		VN0355	550				
VGS(th)	Gate Threshold Voltage		2		4	V	VGS = VDS, ID = 10mA
ΔVGS(th)	Change in VGS(th) with Temperature			-4.8	-6.0	mV/°C	VGS = VDS, ID = 10mA
IGSS	Gate Body Leakage				100	nA	VGS = ±20V, VDS = 0
IDSS	Zero Gate Voltage Drain Current				100	μA	VGS = 0, VDS = Max Rating
					2	mA	VGS = 0, VDS = 0.8 Max Rating, TA = 125°C
ID(ON)	ON-State Drain Current			1.3		A	VGS = 5V, VDS = 25V
			1.5	3.0			VGS = 10V, VDS = 25V
RDS(ON)	Static Drain-to-Source ON-State Resistance			5.5		Ω	VGS = 5V, ID = 0.25A
				4.5	6.0		VGS = 10V, ID = 0.5A
ΔRDS(ON)	Change in RDS(ON) with Temperature			1	2	%/°C	VGS = 10V, ID = 0.5A
GFS	Forward Transconductance		0.5	1		℧	VDS = 25V, ID = 0.5A
CISS	Input Capacitance			550	650	pF	VGS = 0, VDS = 25V, f = 1MHz
COSS	Common Source Output Capacitance			75	125		
CRSS	Reverse Transfer Capacitance			25	50		
td(ON)	Turn-ON Delay Time			8	15	ns	VDD = 25V, ID = 0.5A, RS = 50Ω
tr	Rise Time			8	15		
td(OFF)	Turn-OFF Delay Time			65	100		
tf	Fall Time			12	25		
VSD	Diode Forward Voltage Drop			1.1	1.5	V	VGS = 0, ISD = 5A
trr	Reverse Recovery Time			450		ns	VGS = 0, ISD = 5A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

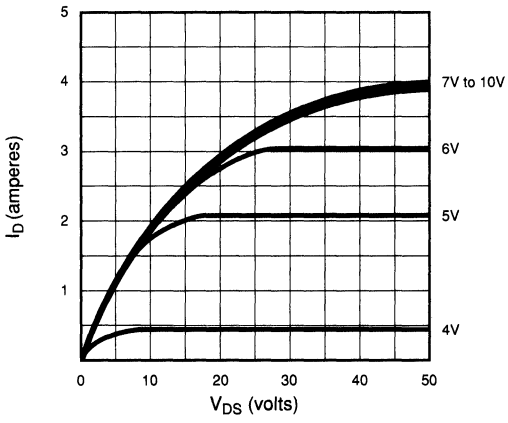
Switching Waveforms and Test Circuit



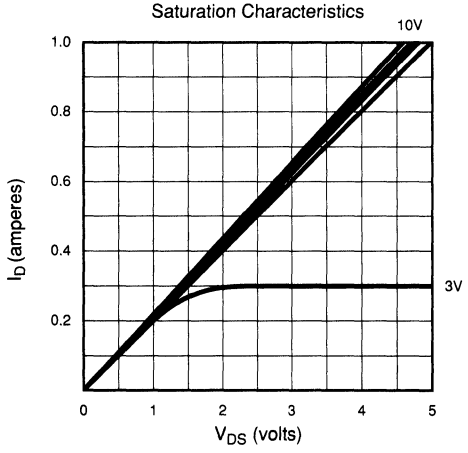


Typical Performance Curves

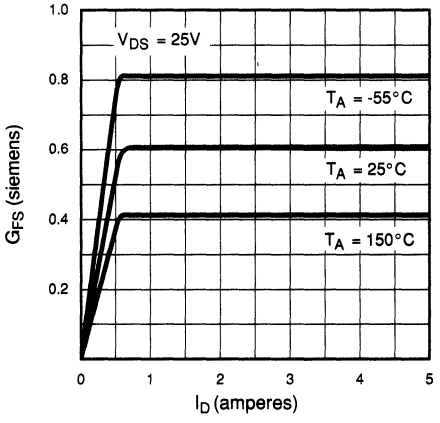
Output Characteristics



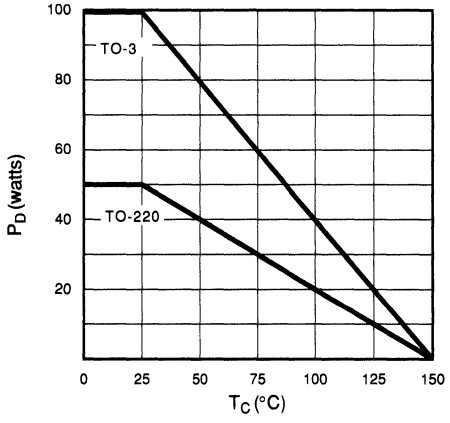
Saturation Characteristics



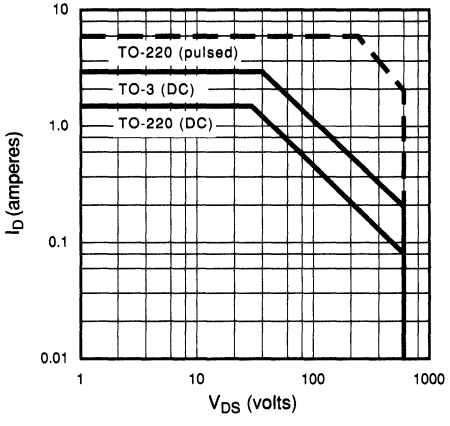
Transconductance vs. Drain Current



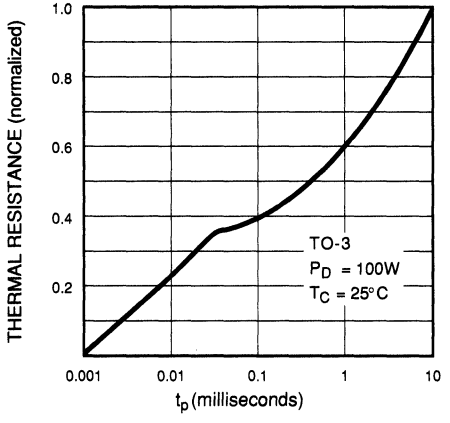
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

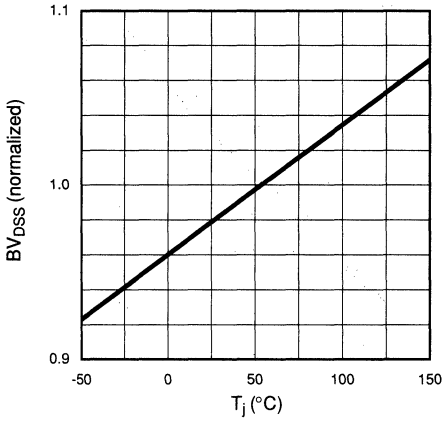


Thermal Response Characteristics

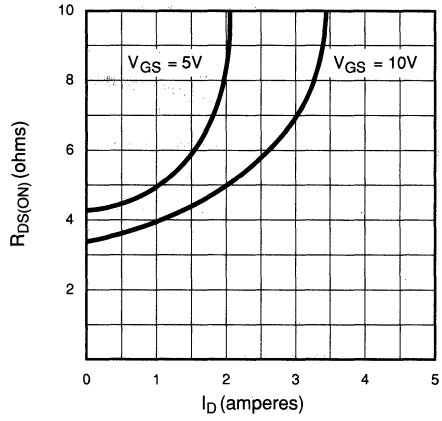


8

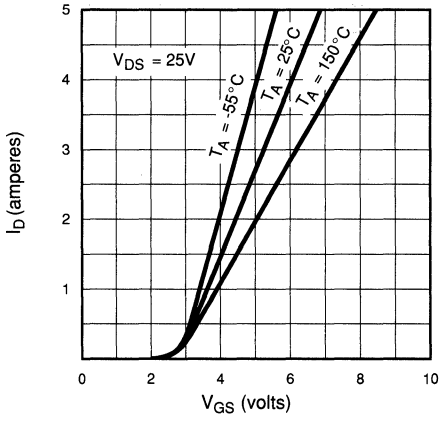
BV$_{DSS}$ Variation with Temperature



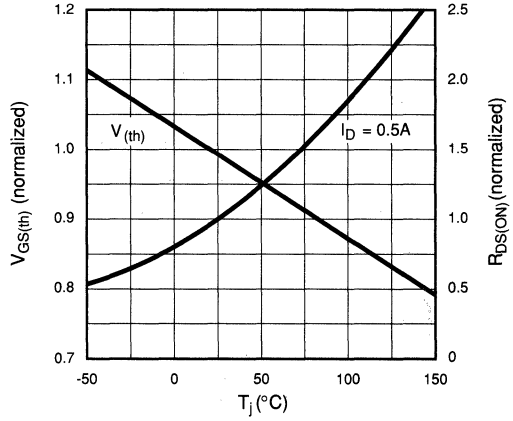
On-Resistance vs. Drain Current



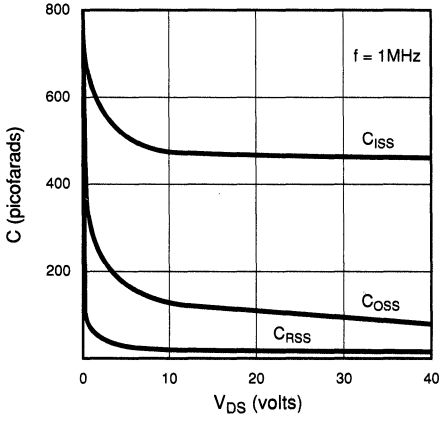
Transfer Characteristics



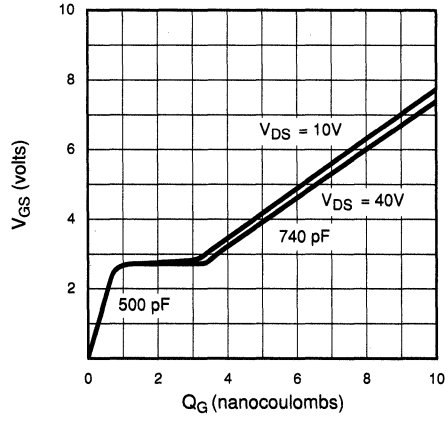
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	TO-220
30V	1.2Ω	2.0A	VN0300B	VN0300L	VN0300D

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

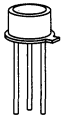
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

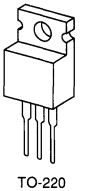
- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-39

TO-92



TO-220

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation	θ_{ja} °C/W	θ_{jc} °C/W
TO-39	1.2A	3A	6.25W	170	20
TO-92	.4A	3A	.4W	312.5	43.5
TO-220	2.11A	6A	20W	80	6.25

* I_D (continuous) is limited by max rated T_j.

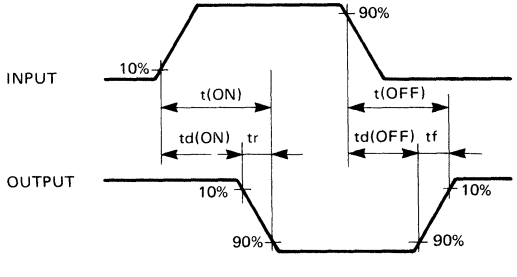
Electrical Characteristics (@ 25°C unless otherwise specified)

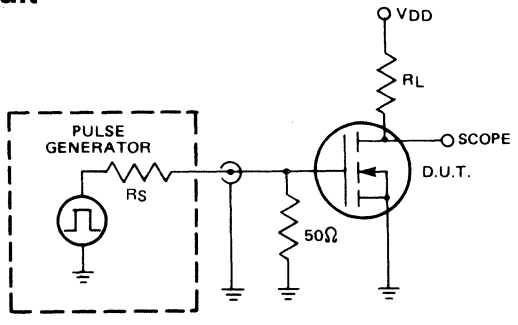
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30			V	I_D = 10μA, V_{GS} = 0
$V_{GS(th)}$	Gate Threshold Voltage	.8		2.5	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage			100	nA	V_{GS} = ±30V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{GS} = 0V, V_{DS} = Max Rating
				500		V_{GS} = 0V, V_{DS} = Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	2			A	V_{GS} = .10V, V_{DS} ≥ 2 $V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.3	Ω	V_{GS} = 5V, I_D = .3A
				1.2		V_{GS} = 10V, I_D = 1A
G_{FS}	Forward Transconductance	200			m℧	V_{DS} ≥ 2 $V_{DS(ON)}$, I_D = 0.5A
C_{ISS}	Input Capacitance			100	pF	V_{GS} = 0, V_{DS} = 15V, f = 1MHz
C_{OSS}	Common Source Output Capacitance			95		
C_{RSS}	Reverse Transfer Capacitance			25		
$t_{(ON)}$	Turn-ON Time			30	ns	V_{DD} = 25V, I_D = 1.0, R_S = 50Ω
$t_{(OFF)}$	Turn-OFF Time			30		
V_{SD}	Diode Forward Voltage Drop		-0.9		V	I_{SD} = 0.63A V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	Dice
350V	35Ω	250mA	VN0535N2	VN0535N3	VN0535ND
400V	35Ω	250mA	VN0540N2	VN0540N3	VN0540ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
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Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

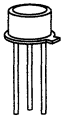
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)

TO-92



TO-39

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-39	250mA	500mA	6.0W	125	20.8	250mA	500mA
TO-92	100mA	400mA	1.0W	170	125	100mA	400mA

* I_D (continuous) is limited by max rated T_j.

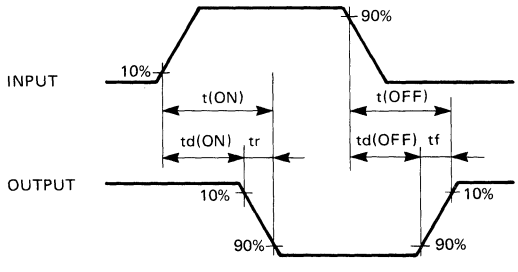
Electrical Characteristics (@ 25°C unless otherwise specified)

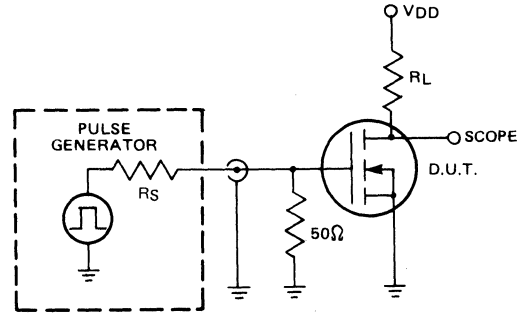
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BVDSS	Drain-to-Source Breakdown Voltage	VN0540	400			V	ID = 1mA, VGS = 0
		VN0535	350				
VGS(th)	Gate Threshold Voltage		2.0		4.0	V	VGS = VDS, ID = 1mA
ΔVGS(th)	Change in VGS(th) with Temperature			−3.5	−4.5	mV/°C	
IGSS	Gate Body Leakage				100	nA	VGS = ±20V, VDS = 0
IDSS	Zero Gate Voltage Drain Current				10	μA	VGS = 0, VDS = Max Rating
					500		VGS = 0, VDS = 0.8 Max Rating, TA = 125°C
ID(ON)	ON-State Drain Current			200		mA	VGS = 5V, VDS = 25V
			250	300			VGS = 10V, VDS = 25V
RDS(ON)	Static Drain-to-Source ON-State Resistance			30		Ω	VGS = 5V, ID = 20mA
				25	35		VGS = 10V, ID = 0.1A
ΔRDS(ON)	Change in RDS(ON) with Temperature			0.9	1.5	%/°C	ID = 0.1A, VGS = 10V
GFS	Forward Transconductance		100	200		m℧	VDS = 25V, ID = 0.1A
CISS	Input Capacitance			45	55	pF	VGS = 0, VDS = 25V, f = 1MHz
COSS	Common Source Output Capacitance			8	10		
CRSS	Reverse Transfer Capacitance			2	5		
td(ON)	Turn-ON Delay Time			3	5	ns	VDD = 25V, ID = 50mA, RS = 50Ω
tr	Rise Time			3	5		
td(OFF)	Turn-OFF Delay Time			3	5		
tf	Fall Time			3	5		
VSD	Diode Forward Voltage Drop			0.8		V	ISD = 0.5A, VGS = 0
trr	Reverse Recovery Time			400		ns	ISD = 0.5A, VGS = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

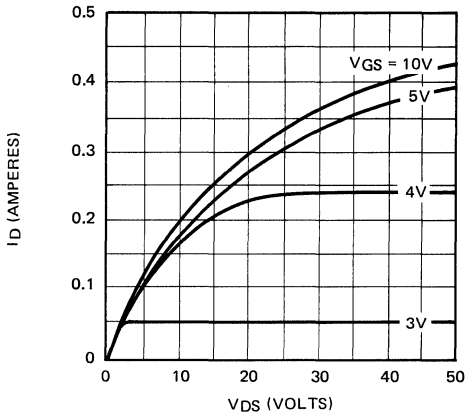
Switching Waveforms and Test Circuit



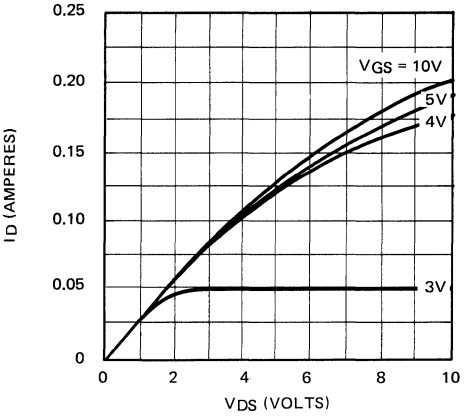


Typical Performance Curves

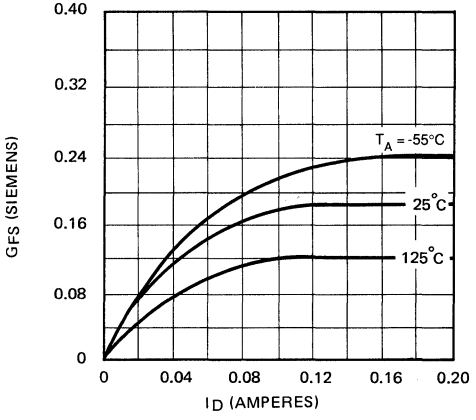
Output Characteristics



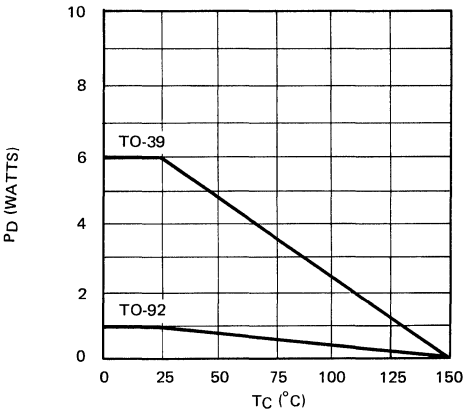
Saturation Characteristics



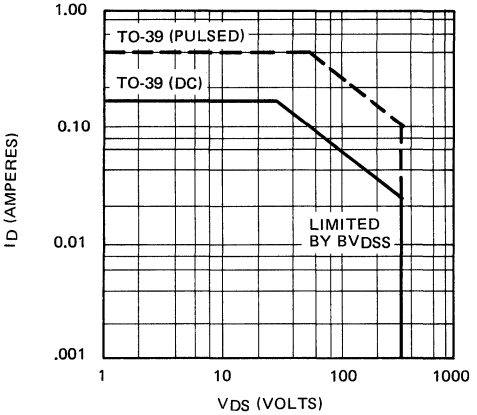
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

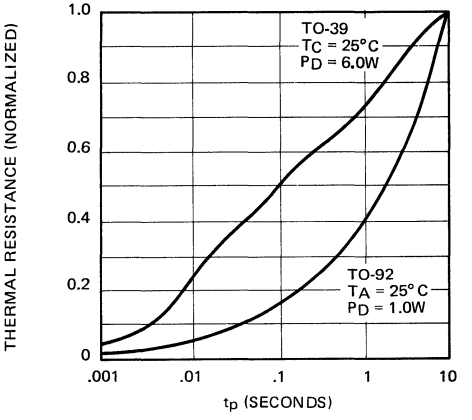


Maximum Rated Safe Operating Area

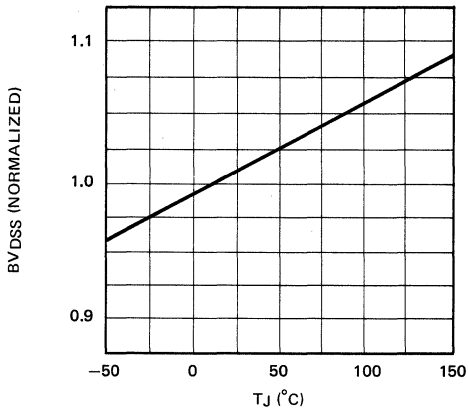


Pulse Condition: 300 μs, 2% dutycycle.

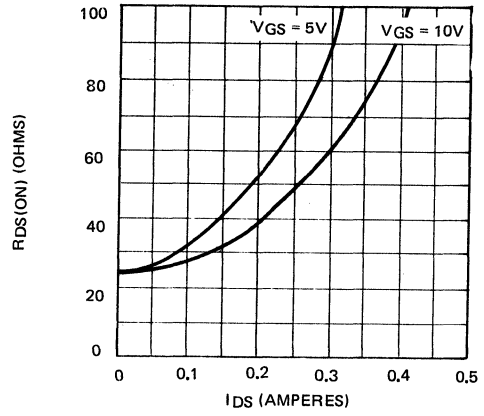
Thermal Response Characteristics



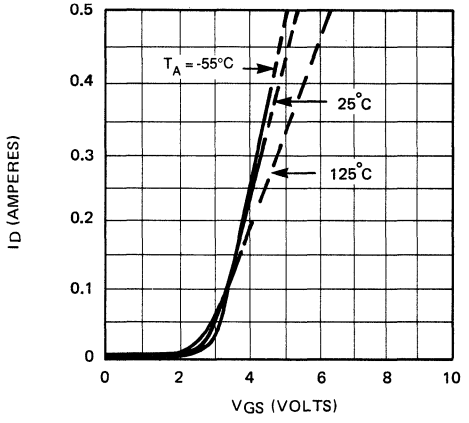
BVDSS Variation with Temperature



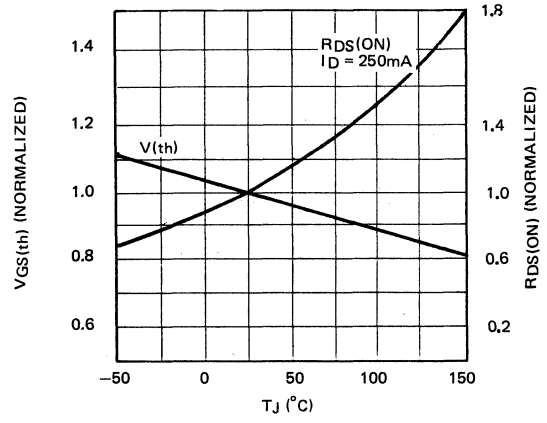
ON-Resistance Vs. Drain Current



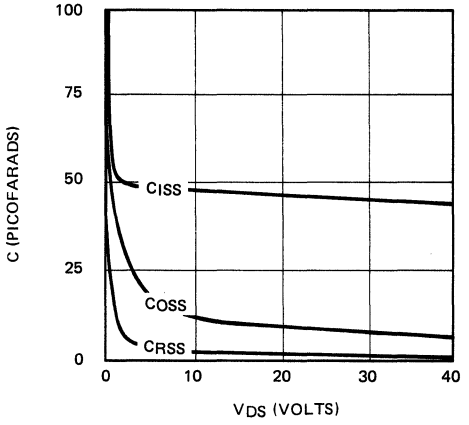
Transfer Characteristics



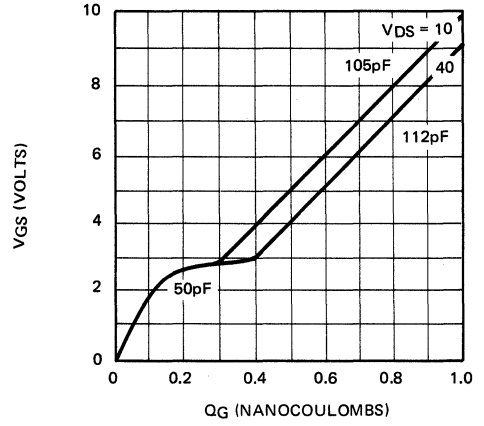
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	Dice
450V	60Ω	150mA	VN0545N2	VN0545N3	VN0545ND
500V	60Ω	150mA	VN0550N2	VN0550N3	VN0550ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Notes 1 and 2)

TO-39

TO-92

Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	100mA	300mA	6W	20	125	100mA	300mA
TO-92	50mA	250mA	1W	125	170	50mA	250mA

*I_D (continuous) is limited by max rated T_j.

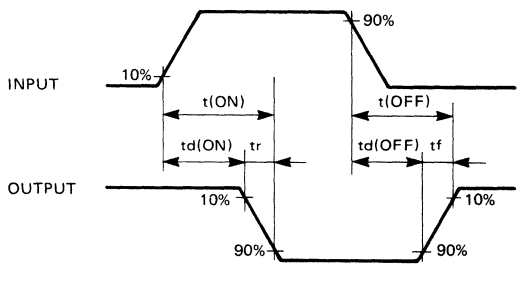
Electrical Characteristics (@ 25°C unless otherwise specified)

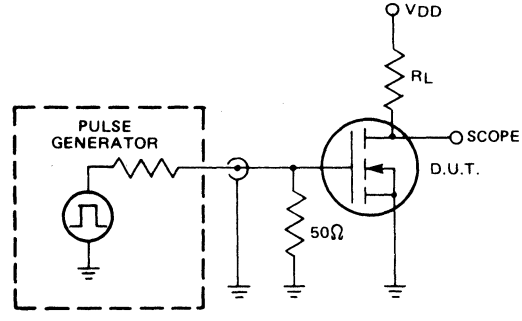
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BVDSS	Drain-to-Source Breakdown Voltage	VN0550	500			V	V_{GS} = 0, I_D = 1mA
		VN0545	450				
VGS(th)	Gate Threshold Voltage		2		4	V	V_{GS} = V_{DS}, I_D = 1mA
ΔVGS(th)	Change in VGS(th) with Temperature			–3.8	–5	mV/°C	V_{GS} = V_{DS}, I_D = 1mA
IGSS	Gate Body Leakage				100	nA	VGS = ±20V, VDS = 0
IDSS	Zero Gate Voltage Drain Current				10	μA	VGS = 0, VDS = Max Rating
					1000		VGS = 0, VDS = 0.8 Max Rating TA = 125°C
ID(ON)	ON-State Drain Current			100		mA	V_{GS} = 5V, V_{DS} = 25V
			150	200			V_{GS} = 10V, V_{DS} = 25V
RDS(ON)	Static Drain-to-Source ON-State Resistance			50		Ω	V_{GS} = 5V, I_D = 50mA
				45	60		V_{GS} = 10V, I_D = 50mA
ΔRDS(ON)	Change in RDS(ON) with Temperature			1	1.7	%/°C	V_{GS} = 10V, I_D = 50mA
GFS	Forward Transconductance		50	75		m℧	V_{DS} = 25V, I_D = 50mA
CISS	Input Capacitance			45	55	pF	V_{GS} = 0, V_{DS} = 25V f = 1 MHz
COSS	Common Source Output Capacitance			8	10		
CRSS	Reverse Transfer Capacitance			2	5		
td(ON)	Turn-ON Delay Time			3	5	ns	V_{DD} = 25V I_D = 50mA R_S = 50Ω
tr	Rise Time			3	5		
td(OFF)	Turn-OFF Delay Time			3	5		
tf	Fall Time			3	5		
VSD	Diode Forward Voltage Drop			0.8		V	V_{GS} = 0, I_{SD} = 0.5A
trr	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = 0.5A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-39	TO-92	TO-220	Dice
350V	10Ω	0.75A	VN0635N2	VN0635N3	VN0635N5	VN0635ND
400V	10Ω	0.75A	VN0640N2	VN0640N3	VN0640N5	VN0640ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
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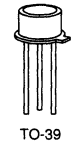
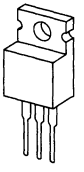
Package Options (Note 1)



TO-39

TO-92



TO-220

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-3	0.25A	1.5A	1W	125	170	0.25A	1.5A
TO-39	0.6A	2.5A	6W	21	125	.6A	2.5A
TO-220	1.6A	2.5A	28W	2.7	70	1.6A	2.5A

*I_D (continuous) is limited by max rated T_j.

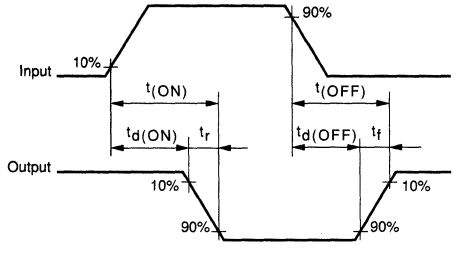
Electrical Characteristics (@ 25°C unless otherwise specified)

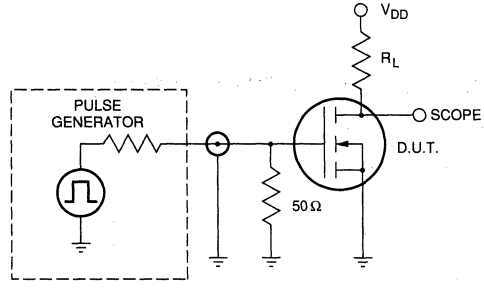
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0635	350			V	V_{GS} = 0, I_D = 2mA
		VN0640	400				
$V_{GS(th)}$	Gate Threshold Voltage		2		4	V	V_{GS} = V_{DS}, I_D = 2mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-4.0	mV/°C	V_{GS} = V_{DS}, I_D = 2mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	V_{GS} = 0, V_{DS} = Max Rating
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			0.6		A	V_{GS} = 5V, V_{DS} = 25V
			0.75	1.3			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			8		Ω	V_{GS} = 5V, I_D = 100mA
				8	10		V_{GS} = 10V, I_D = 500mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	V_{GS} = 10V, I_D = 500mA
G_{FS}	Forward Transconductance		0.1			℧	V_{DS} = 25V, I_D = 500mA
C_{ISS}	Input Capacitance			85	130	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	75		
C_{RSS}	Reverse Transfer Capacitance			10	20		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = 25V, I_D = 0.5A, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				10		
V_{SD}	Diode Forward Voltage Drop				1.8	V	V_{GS} = 0, I_{SD} = 0.5A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = 0.5A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

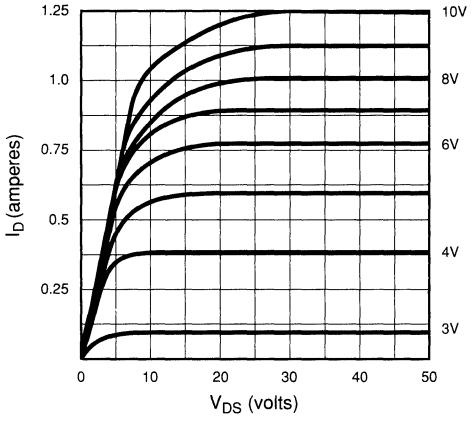
Switching Waveforms and Test Circuit



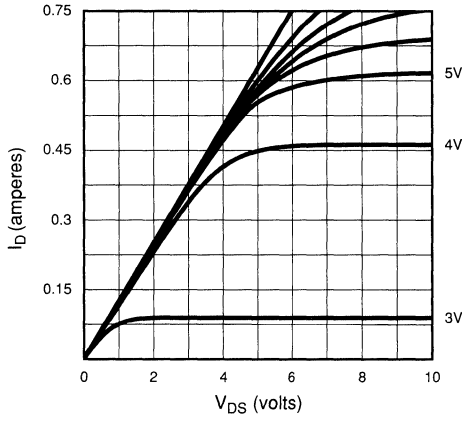


Typical Performance Curves

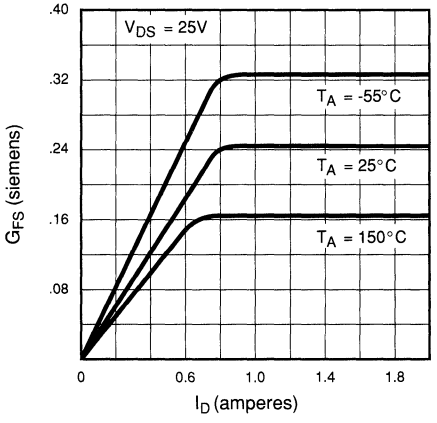
Output Characteristics



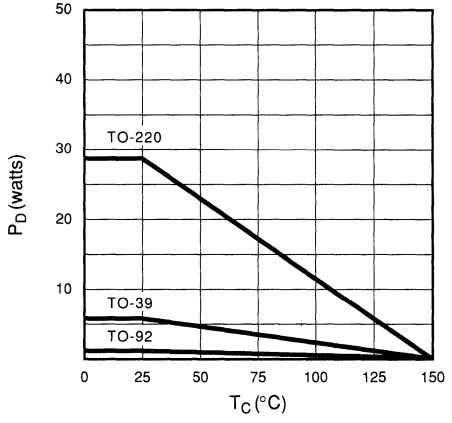
Saturation Characteristics



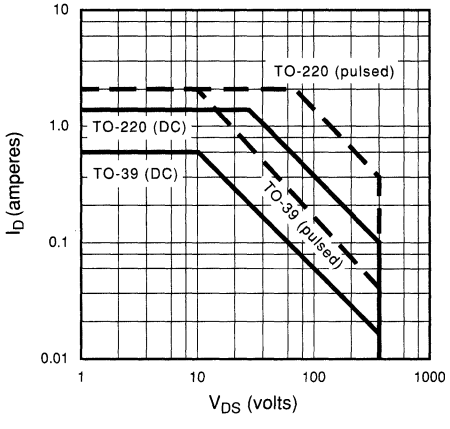
Transconductance vs. Drain Current



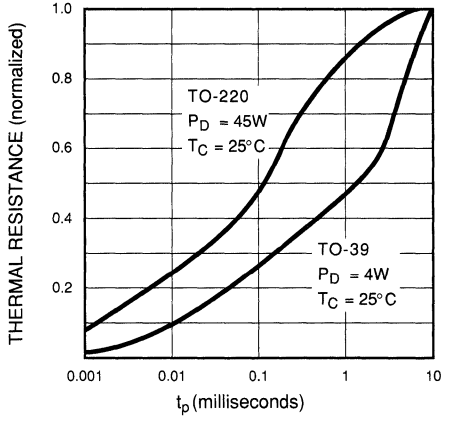
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

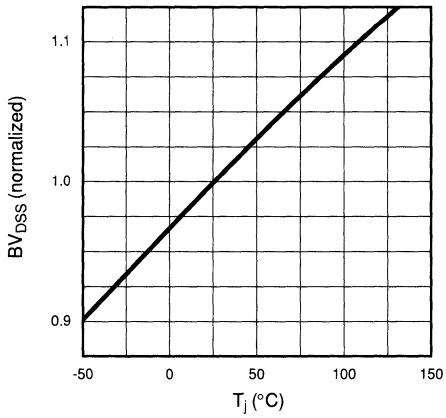


Thermal Response Characteristics

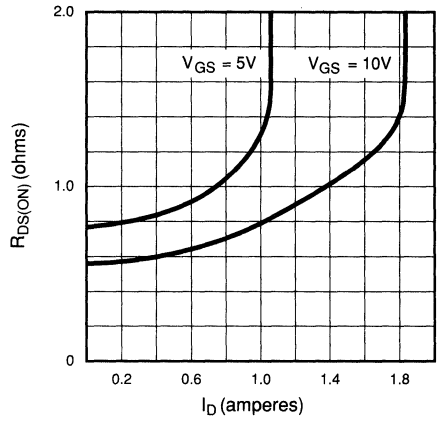


8

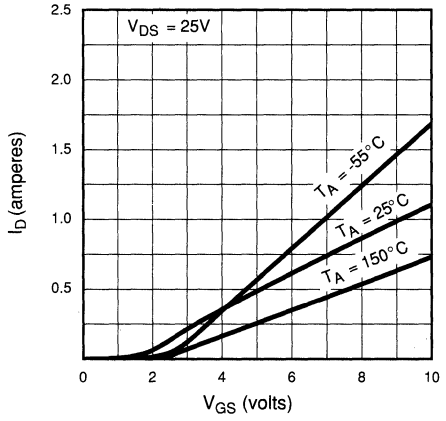
BV_{DSS} Variation with Temperature



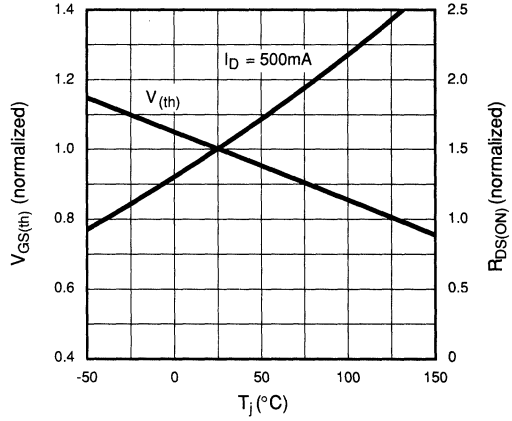
On-Resistance vs. Drain Current



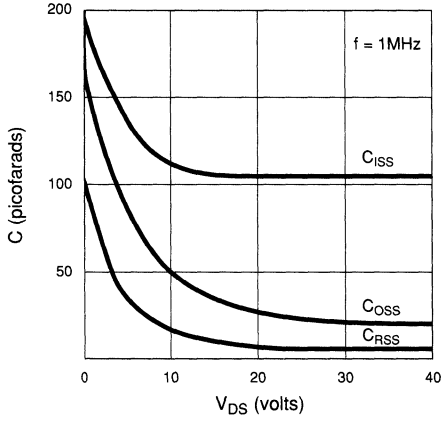
Transfer Characteristics



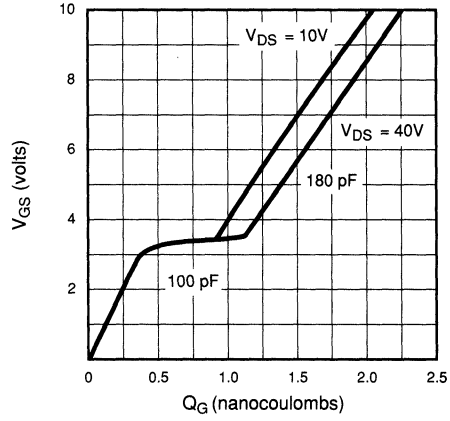
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-39	TO-92	TO-220	Dice
450V	16Ω	0.5A	VN0645N2	VN0645N3	VN0645N5	VN0645ND
500V	16Ω	0.5A	VN0650N2	VN0650N3	VN0650N5	VN0650ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

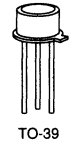
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

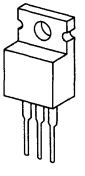
- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-39

TO-92



TO-220

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-92	0.2A	1.0A	1W	125	170	0.2A	1.0A
TO-39	0.4A	1.5A	6W	21	125	0.4A	1.5A
TO-220	1.0A	1.5A	28W	2.7	70	1.0A	1.5A

*I_D (continuous) is limited by max rated T_j.

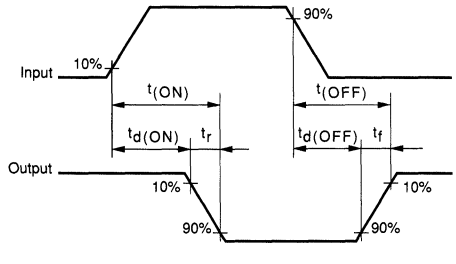
Electrical Characteristics (@ 25°C unless otherwise specified)

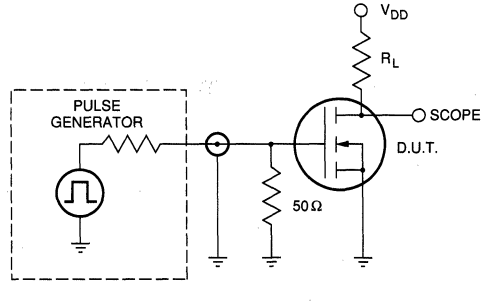
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0645	450			V	V_{GS} = 0, I_D = 2mA
		VN0650	500				
$V_{GS(th)}$	Gate Threshold Voltage		2		4	V	V_{GS} = V_{DS}, I_D = 2mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-4.5	mV/°C	V_{GS} = V_{DS}, I_D = 2mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	V_{GS} = 0, V_{DS} = Max Rating
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			0.7		A	V_{GS} = 5V, V_{DS} = 25V
			0.5	1.1			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			15		Ω	V_{GS} = 5V, I_D = 100mA
				13	16		V_{GS} = 10V, I_D = 400mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	V_{GS} = 10V, I_D = 400mA
G_{FS}	Forward Transconductance		100			m℧	V_{DS} = 25V, I_D = 400mA
C_{ISS}	Input Capacitance			85	130	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	75		
C_{RSS}	Reverse Transfer Capacitance			10	20		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = 25V, I_D = 0.4A, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				10		
V_{SD}	Diode Forward Voltage Drop				1.8	V	V_{GS} = 0, I_{SD} = 0.4A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = 0.4A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

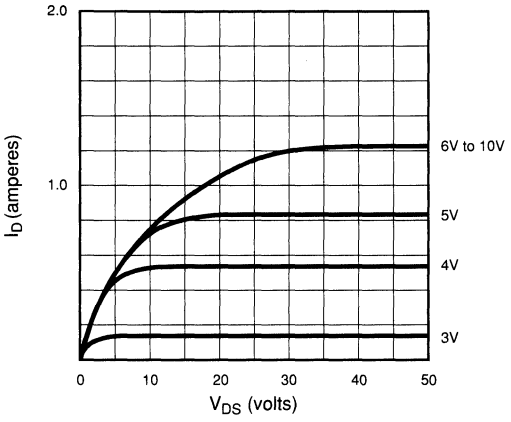
Switching Waveforms and Test Circuit



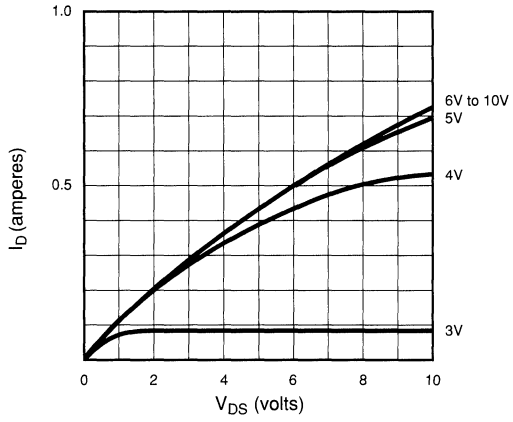


Typical Performance Curves

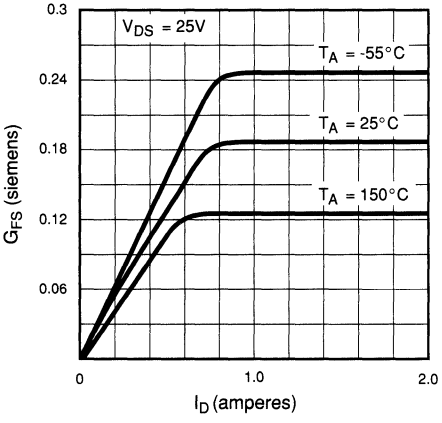
Output Characteristics



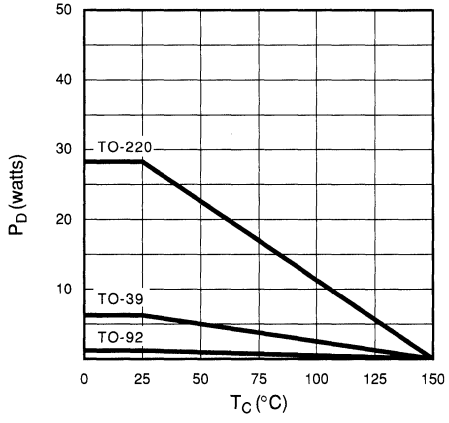
Saturation Characteristics



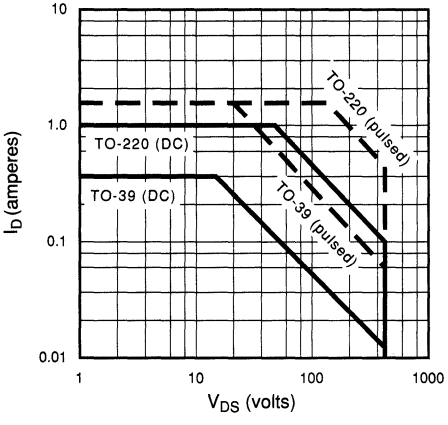
Transconductance vs. Drain Current



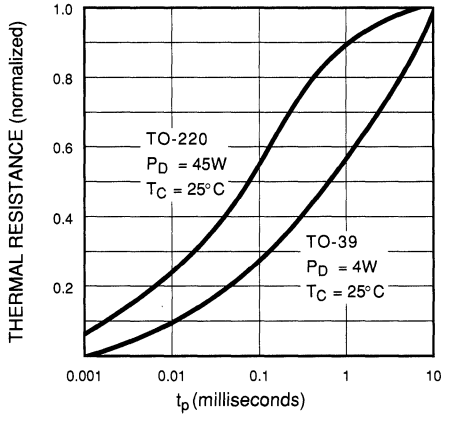
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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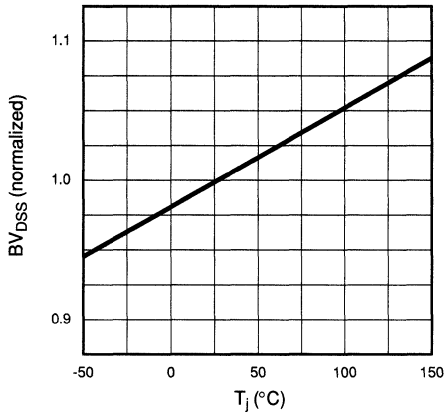
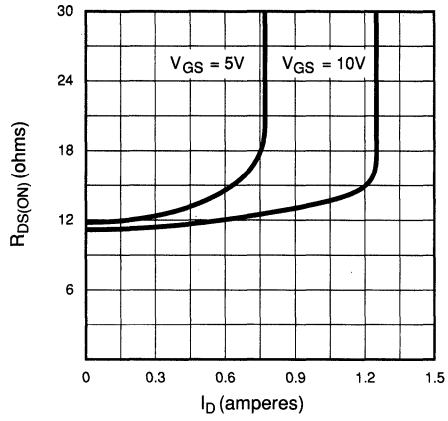
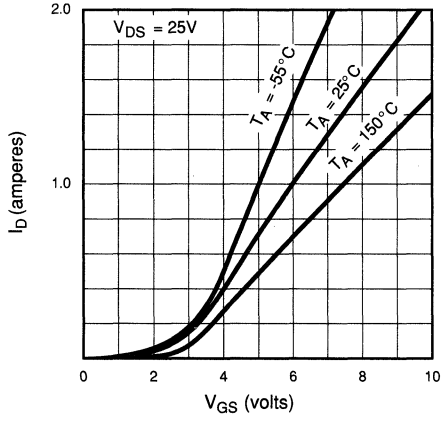
BV$_{DSS}$ Variation with Temperature



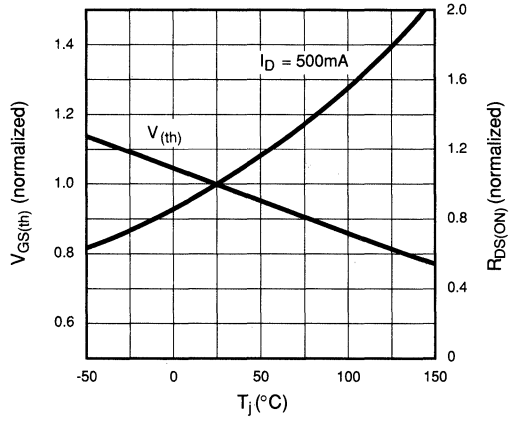
On-Resistance vs. Drain Current



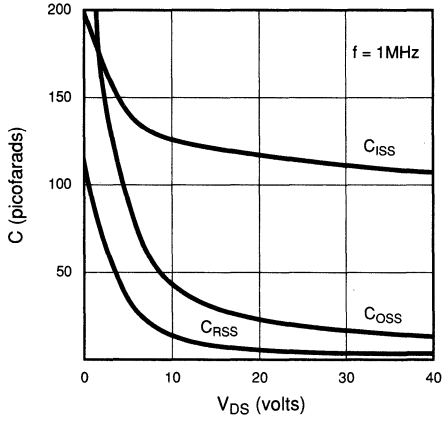
Transfer Characteristics



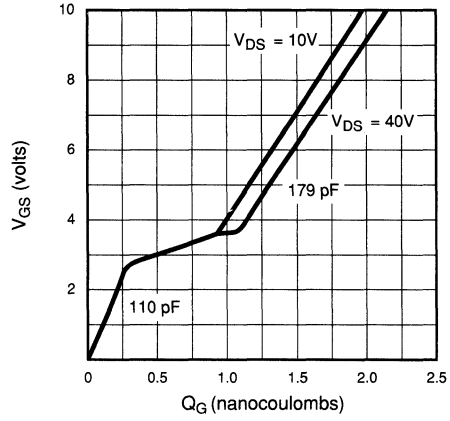
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-39	TO-92	TO-220	Dice
550V	20Ω	0.25A	VN0655N2	VN0655N3	VN0655N5	VN0655ND
600V	20Ω	0.25A	VN0660N2	VN0660N3	VN0660N5	VN0660ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

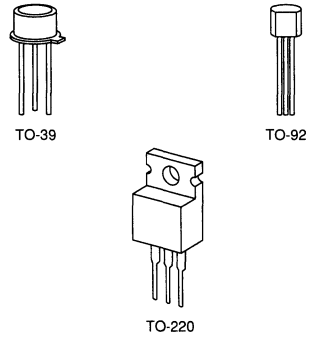
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-92	0.15A	0.5A	1W	125	170	0.15A	0.5A
TO-39	0.35A	1.0A	6W	21	125	0.25A	1.0A
TO-220	0.75A	1.0A	25W	3.1	70	0.6A	1.0A

*I_D (continuous) is limited by max rated T_j.

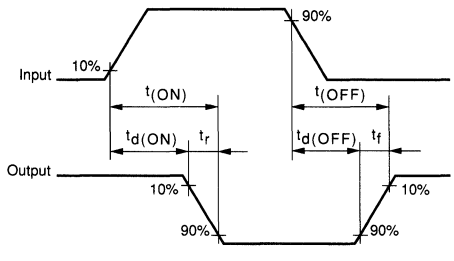
Electrical Characteristics (@ 25°C unless otherwise specified)

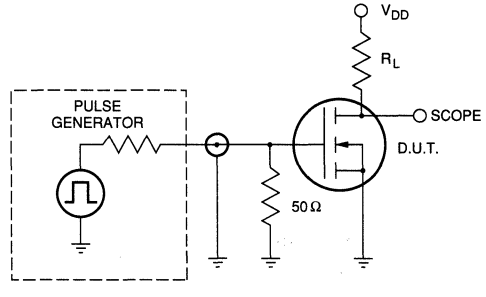
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0655	550			V	V_{GS} = 0, I_D = 2mA
		VN0660	600				
$V_{GS(th)}$	Gate Threshold Voltage		2		4	V	V_{GS} = V_{DS}, I_D = 2mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-4.5	mV/°C	V_{GS} = V_{DS}, I_D = 2mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	V_{GS} = 0, V_{DS} = Max Rating
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			700		mA	V_{GS} = 5V, V_{DS} = 25V
			250	900			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			19		Ω	V_{GS} = 5V, I_D = 100mA
				15	20		V_{GS} = 10V, I_D = 100mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	V_{GS} = 10V, I_D = 100mA
G_{FS}	Forward Transconductance		50			m℧	V_{DS} = 25V, I_D = 100mA
C_{ISS}	Input Capacitance			85	130	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	75		
C_{RSS}	Reverse Transfer Capacitance			10	20		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = 25V, I_D = 0.1A, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				10		
V_{SD}	Diode Forward Voltage Drop				1.8	V	V_{GS} = 0, I_{SD} = 100mA
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = 100mA

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

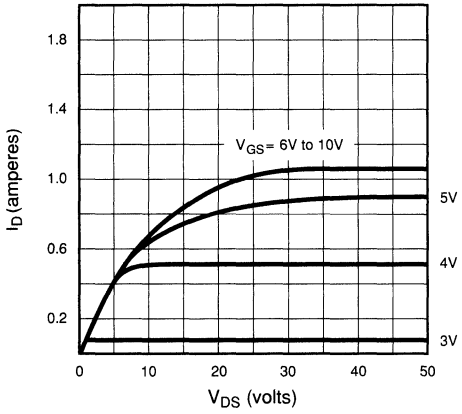
Switching Waveforms and Test Circuit



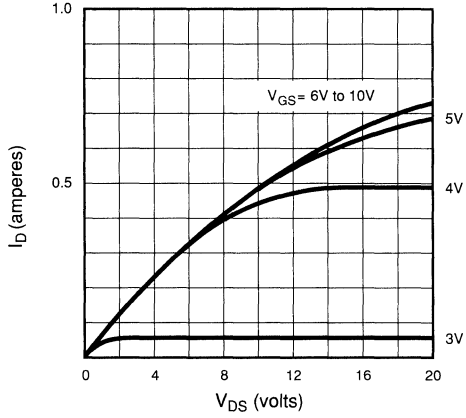


Typical Performance Curves

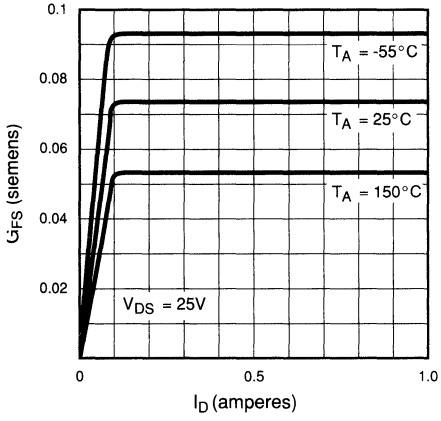
Output Characteristics



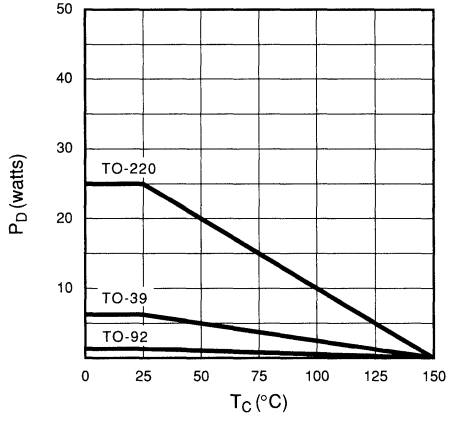
Saturation Characteristics



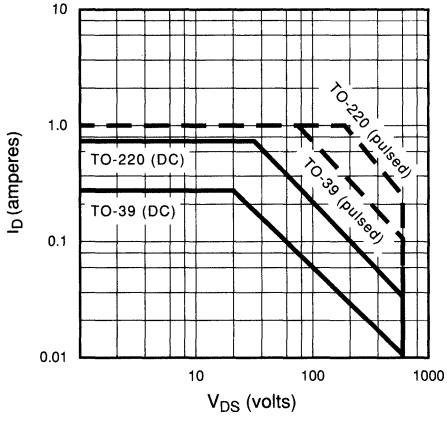
Transconductance vs. Drain Current



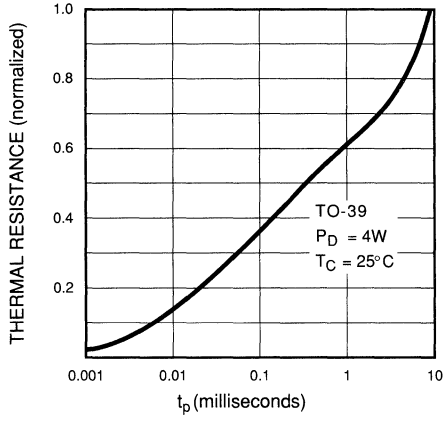
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

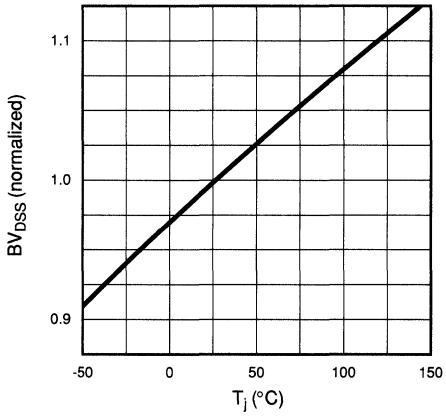


Thermal Response Characteristics

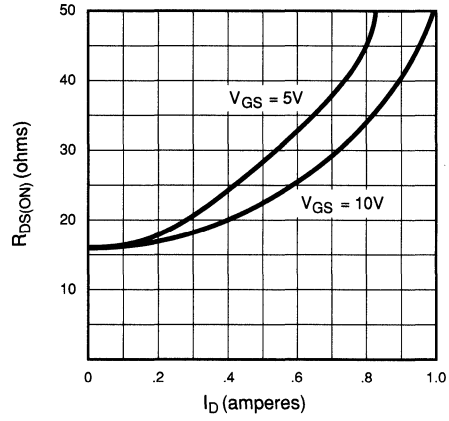


8

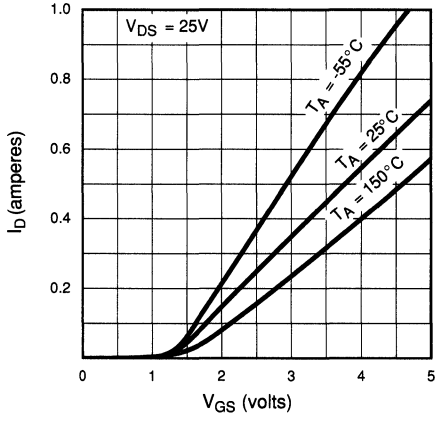
BV$_{DSS}$ Variation with Temperature



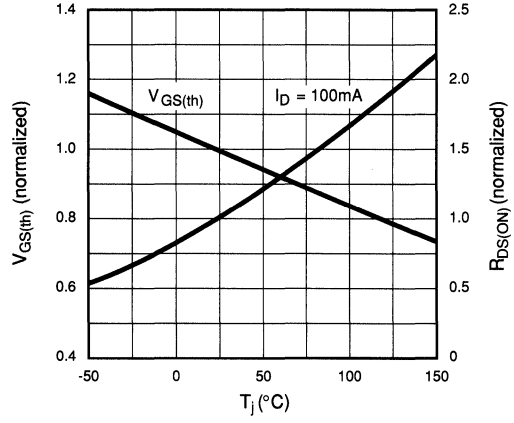
On-Resistance vs. Drain Current



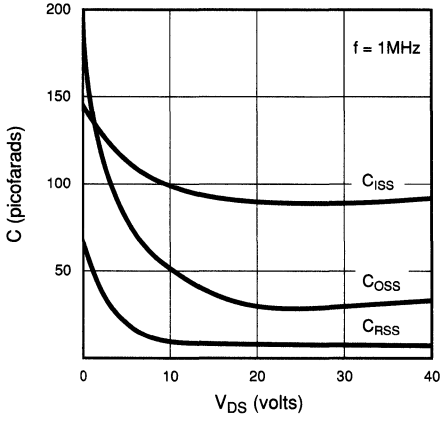
Transfer Characteristics



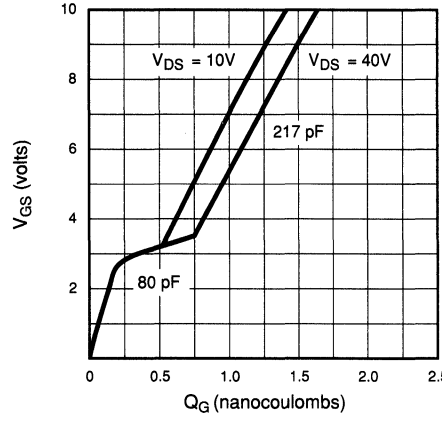
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			TO-92
60V	3Ω	1.5A	VN0606L
60V	5Ω	0.75A	VN0610LL

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Note 1)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W
TO-92	0.3A	2.0A	.4W	312.5	51

*I_D (continuous) is limited by max rated T_j.

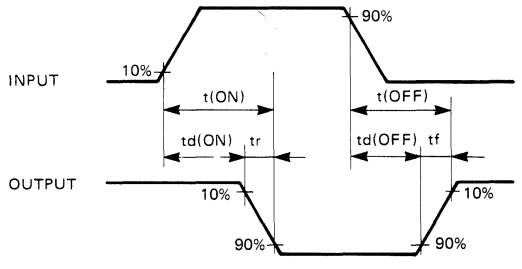
Electrical Characteristics (@ 25°C unless otherwise specified)

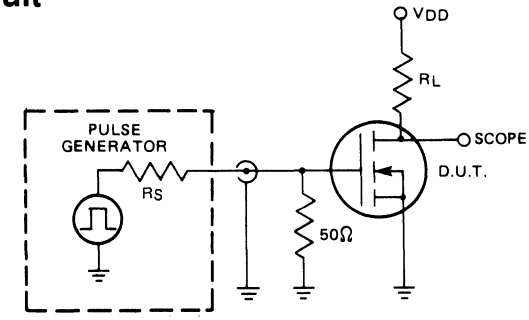
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0610	60			V	I_D = 100μA, V_{GS} = 0
		VN0606	60			V	I_D = 10μA, V_{GS} = 0
$V_{GS(th)}$	Gate Threshold Voltage	VN0610	0.8		2.5	V	V_{GS} = V_{DS}, I_D = 1mA
		VN0606	0.8		2.0	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ±15V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	μA	V_{GS} = 0V, V_{DS} = Max Rating
					500		V_{GS} = 0V, V_{DS} = Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	VN0610	0.75			A	V_{GS} = 10V, V_{DS} ≥ 2 $V_{DS(ON)}$
		VN0606	1.5				V_{GS} = 10V, V_{DS} ≥ 2 $V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	VN0610			7.5	Ω	V_{GS} = 5V, I_D = 0.2A
		VN0610			5		V_{GS} = 10V, I_D = 0.5A
		VN0606			3		V_{GS} = 10V, I_D = 1A
G_{FS}	Forward Transconductance		170			m℧	V_{DS} ≥ 2 $V_{DS(ON)}$, I_D = 0.5A
C_{ISS}	Input Capacitance				50	pF	V_{GS} = 0, V_{DS} = 25V, f = 1MHz
C_{OSS}	Common Source Output Capacitance				25		
C_{RSS}	Reverse Transfer Capacitance				5		
$t_{(ON)}$	Turn-ON Time				10	ns	V_{DD} = 25V, I_D = 1A, R_S = 50Ω
$t_{(OFF)}$	Turn-OFF Time				10		
V_{SD}	Diode Forward Voltage Drop	VN0610		−1.2		V	I_{SD} = −0.47A, V_{GS} = 0
		VN0606		−.85			I_{SD} = −0.2A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			TO-92
80V	4Ω	1.5A	VN0808L

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W
TO-92	.26A	±2A	1W	125	26.4

*I_D (continuous) is limited by max rated T_j.

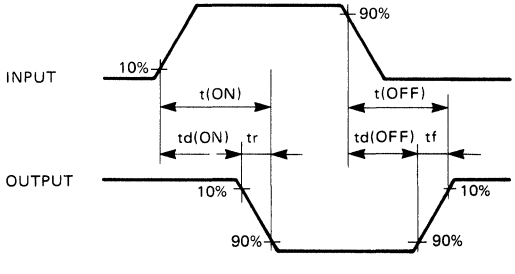
Electrical Characteristics (@ 25°C unless otherwise specified)

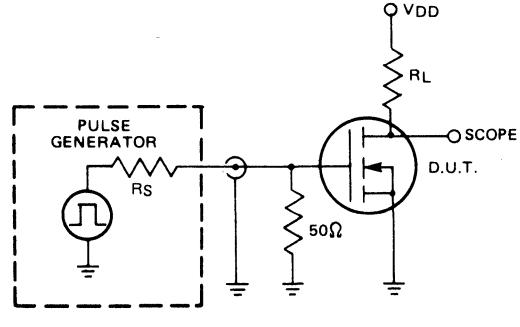
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	80			V	I_D = 10μA, V_{GS} = 0
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage			100	nA	V_{GS} = ±15V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{GS} = 0V, V_{DS} = Max Rating
				500		V_{GS} = 0V, V_{DS} = Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	1.5			A	V_{GS} = 10V, V_{DS} ≥ 2 $V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			4.0	Ω	V_{GS} = 10V, I_D = 1A
G_{FS}	Forward Transconductance	170			m℧	V_{DS} ≥ 2 $V_{DS(ON)}$, I_D = 0.5A
C_{ISS}	Input Capacitance			50	pF	V_{GS} = 0, V_{DS} = 25V, f = 1MHz
C_{OSS}	Common Source Output Capacitance			40		
C_{RSS}	Reverse Transfer Capacitance			10		
$t_{(ON)}$	Turn-ON Time			10	ns	V_{DD} = 15V, I_D = 0.6A, R_S = 50Ω
$t_{(OFF)}$	Turn-OFF Time			10		
V_{SD}	Diode Forward Voltage Drop		−1.2		V	V_{GS} = 0, I_{SD} = −0.35A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
60V	5Ω	0.5A	VN10KN9	VN10KN3

Features

- ☐ Freedom from secondary breakdown
- ☐ TTL/CMOS compatibility
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Reliable TO-92 package compatible with auto-insertion
- ☐ Complements VP01A P-Channel devices

Advanced DMOS Technology

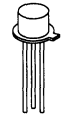
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Inductive load driver
- ☐ Display driver
- ☐ Line driver
- ☐ Analog switch
- ☐ Alternative to VN0106N3

Package Options (Note 1)



TO-52

TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	ID (continuous) (Notes 1 and 2)	ID (pulsed)	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}
TO-92	0.3A	1.0A	1.0W	170	125	1.5A	3.0A

Note 1: I_D (continuous) is limited by max rated T_j.
Note 2: VN0106N3 can be used if an I_D (continuous) of 0.5A is needed.

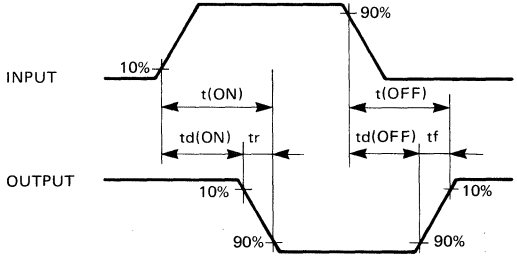
Electrical Characteristics (@ 25°C unless otherwise specified)

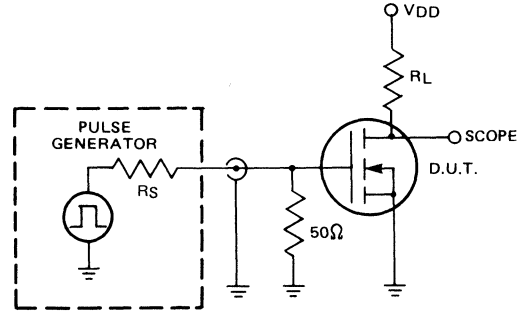
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BVDSS	Drain-to-Source Breakdown Voltage VN10K	60			V	VGS = 0, ID = 100uA
VGS(th)	Gate Threshold Voltage	0.8		2.5	V	VDS = VGS, ID = 1mA
ΔVGS(th)	Change in VGS(th) with Temperature		−3.8		mV/°C	
IGSS	Gate Body Leakage			100	nA	VGS = 10V, VDS = 0
IDSS	Zero Gate Voltage Drain Current			10	μA	VGS = 0, VDS = 40V
ID(ON)	ON-State Drain Current	0.25			A	VDS = 25V, VGS = 5V
		0.75				VDS = 25V, VGS = 10V
RDS(ON)	Static Drain-to-Source ON-State Resistance			5	Ω	VGS = 10V, ID = 0.5A
ΔRDS(ON)	Change in RDS(ON) with Temperature		0.7		%/°C	ID = 500mA, VGS = 10V
GFS	Forward Transconductance	100			m℧	VDS = 15V, ID = 0.5A
CISS	Input Capacitance		48	60	pF	VDS = 25V, f = 1MHz
COSS	Common Source Output Capacitance		16	25		
CRSS	Reverse Transfer Capacitance		2	5		
td(ON)	Turn-ON Delay Time			5	ns	VDD = 25V, ID = 0.5A, RS = 50Ω
tr	Rise Time			5		
td(OFF)	Turn-OFF Delay Time			5		
tf	Fall Time			5		
VSD	Diode Forward Voltage Drop		0.8		V	ISD = .5A, VGS = 0
trr	Reverse Recovery Time		160		ns	ISD = .5A, VGS = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

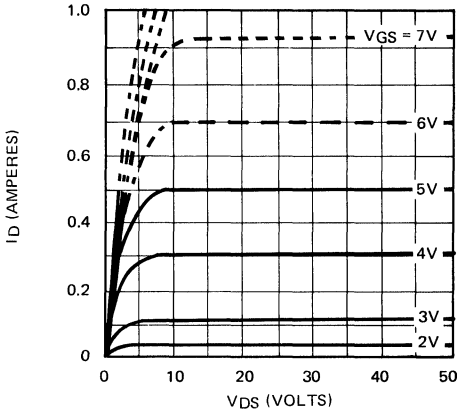
Switching Waveforms and Test Circuit



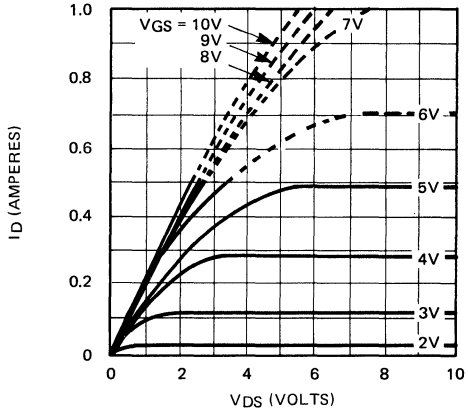


Typical Performance Curves

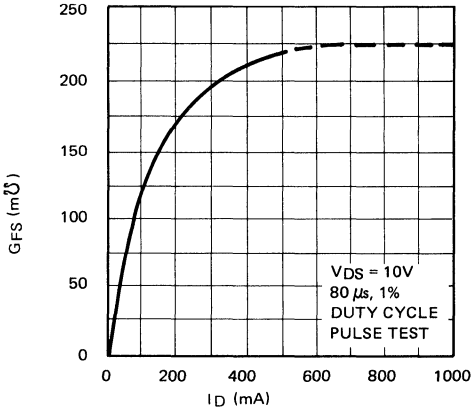
Output Characteristics



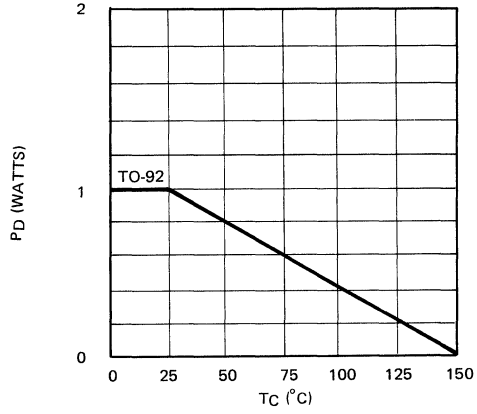
Saturation Characteristics



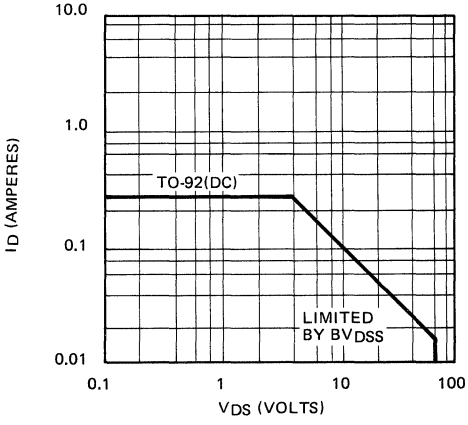
Transconductance Vs. Drain Current



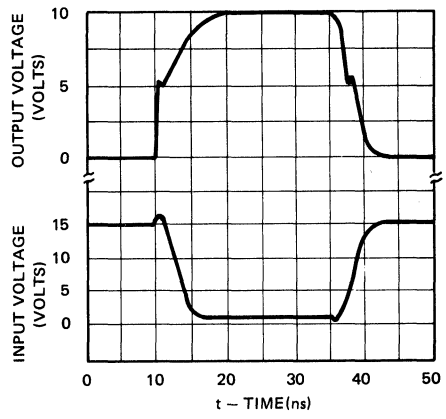
Power Dissipation Vs. Case Temperature



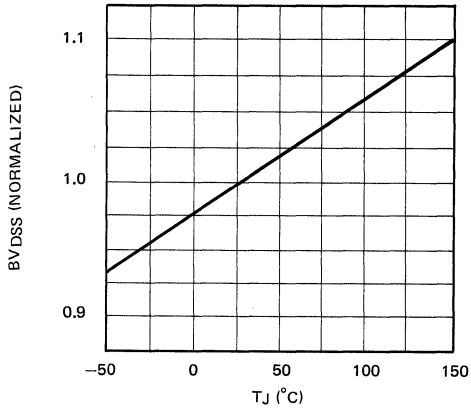
Maximum Rated Safe Operating Area



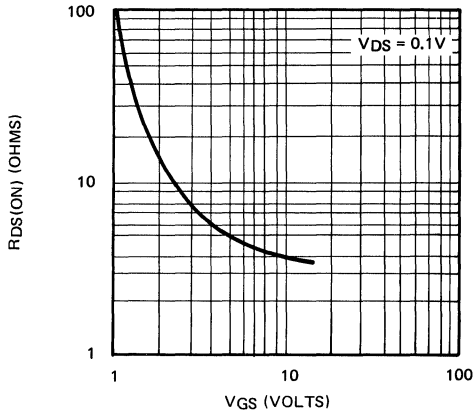
Switching Waveforms



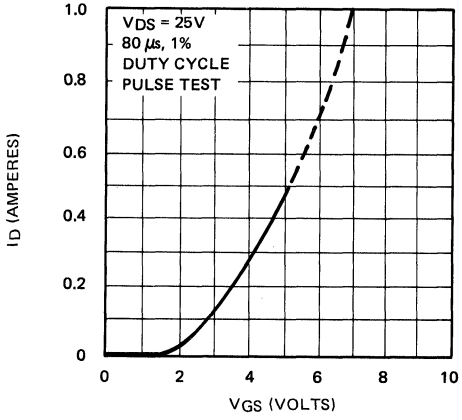
BVDSS Variation with Temperature



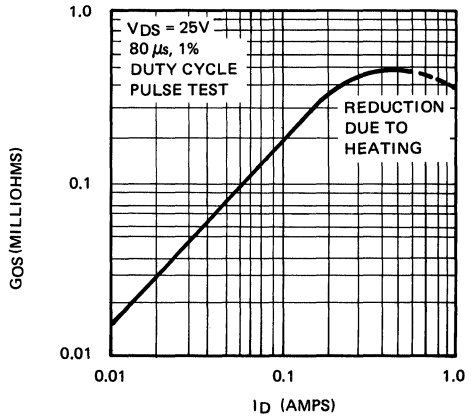
ON-Resistance Vs. Gate-to-Source Voltage



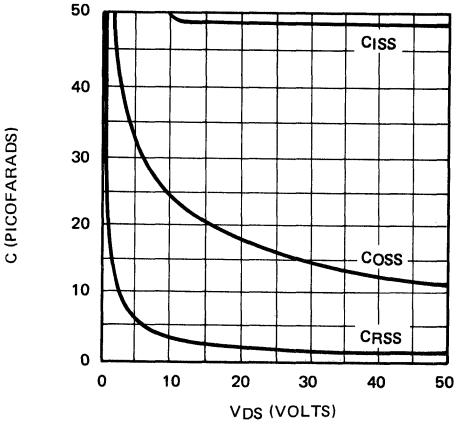
Transfer Characteristics



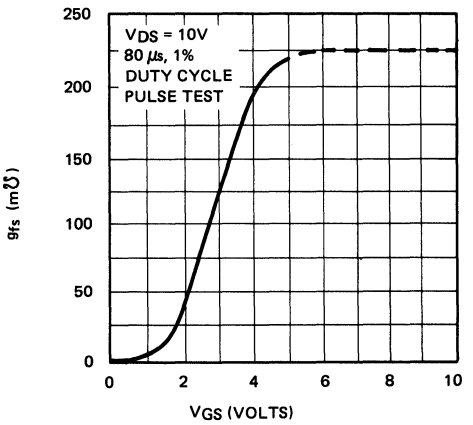
Output Conductance vs Drain Current



Capacitance Vs. Drain-to-Source Voltage



Transconductance vs Gate-Source Voltage



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	Dice
60V	0.7Ω	8.0A	VN1106N1	VN1106N2	VN1106N5	VN1106ND
100V	0.7Ω	8.0A	VN1110N1	VN1110N2	VN1110N5	VN1110ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

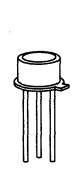
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

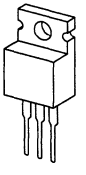
Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

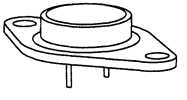
Package Options (Note 1)



TO-39



TO-220



TO-3

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO - 3	9.0A	20A	75W	41	1.6	9A	20A
TO - 39	2.5A	6A	6W	125	20.8	2.5A	6A
TO - 220	7.0A	18A	45W	70	2.7	7A	18A

*I_D (continuous) is limited by max rated T_j.

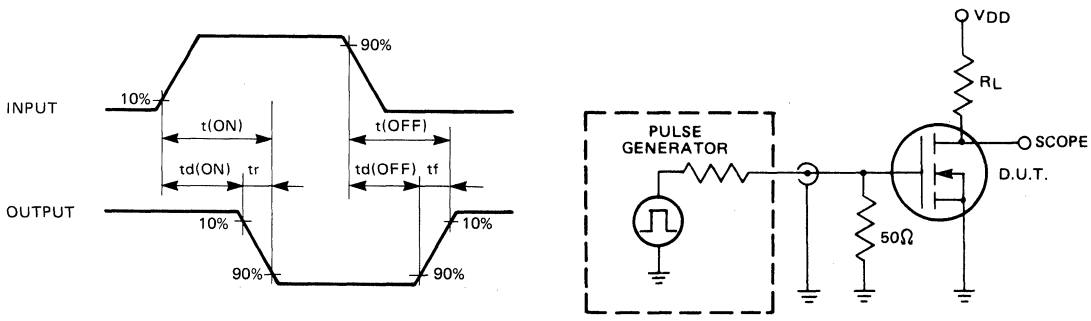
Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BVDSS	Drain-to-Source Breakdown Voltage	VN1110	100			V	VGS = 0, ID = 5mA
		VN1106	60				
VGS(th)	Gate Threshold Voltage		0.8		2.4	V	VGS = VDS, ID = 5mA
ΔVGS(th)	Change in VGS(th) with Temperature			–4	–6	mV/°C	VGS = VDS, ID = 5mA
IGSS	Gate Body Leakage				100	nA	VGS = ±20V, VDS = 0
IDSS	Zero Gate Voltage Drain Current				50	μA	VGS = 0, VDS = Max Rating
					1	mA	VGS = 0, VDS = 0.8 Max Rating, TA = 125°C
ID(ON)	ON-State Drain Current		3	5		A	VGS = 5V, VDS = 25V
			8	15			VGS = 10V, VDS = 25V
RDS(ON)	Static Drain-to-Source ON-State Resistance			0.7	1.0	Ω	VGS = 5V, ID = 3A
				0.4	0.7		VGS = 10V, ID = 5A
ΔRDS(ON)	Change in RDS(ON) with Temperature			0.3	0.8	%/°C	VGS = 10V, ID = 5A
GFS	Forward Transconductance		1	2		℧	VDS = 25V, ID = 3A
CISS	Input Capacitance			240	350	pF	VGS = 0, VDS = 25V, f = 1 MHz
COSS	Common Source Output Capacitance			150	200		
CRSS	Reverse Transfer Capacitance			16	25		
td(ON)	Turn-ON Delay Time			10	45	ns	VDD = 25V, ID = 3A, RS = 50Ω
tr	Rise Time			5	10		
td(OFF)	Turn-OFF Delay Time			35	45		
tf	Fall Time			20	35		
VSD	Diode Forward Voltage Drop			1.2	1.6	V	VGS = 0, ISD = 5A
trr	Reverse Recovery Time			300		ns	VGS = 0, ISD = 1A

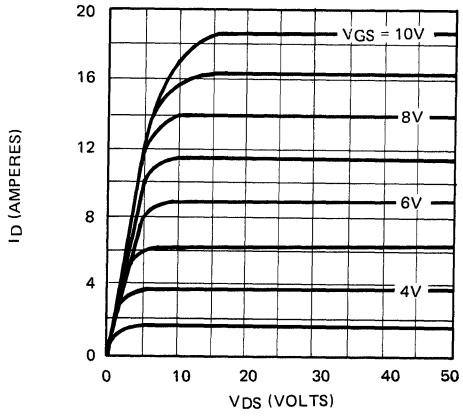
Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

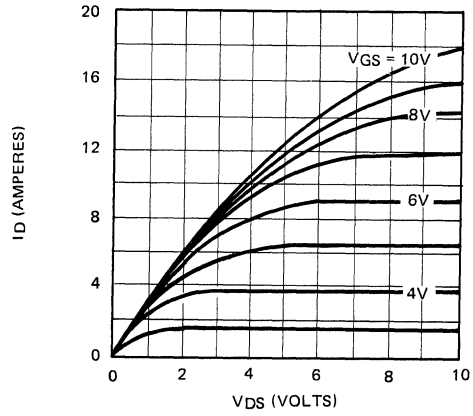


Typical Performance Curves

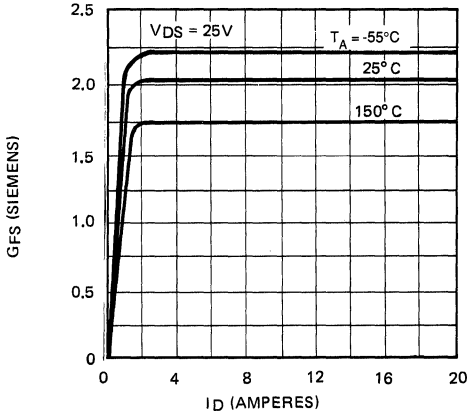
Output Characteristics



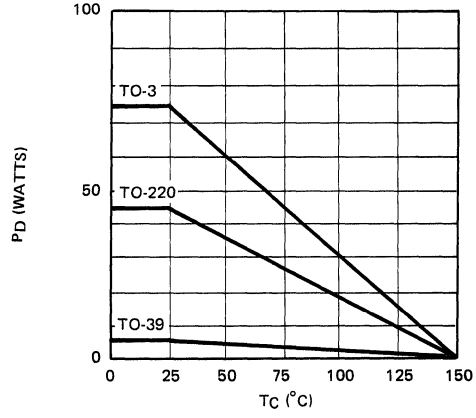
Saturation Characteristics



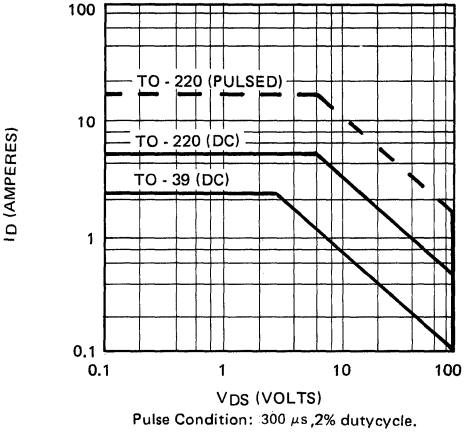
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

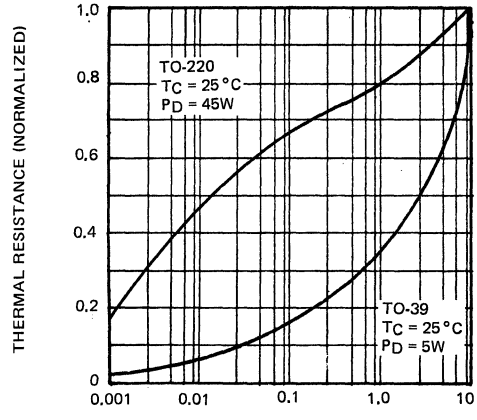


Maximum Rated Safe Operating Area

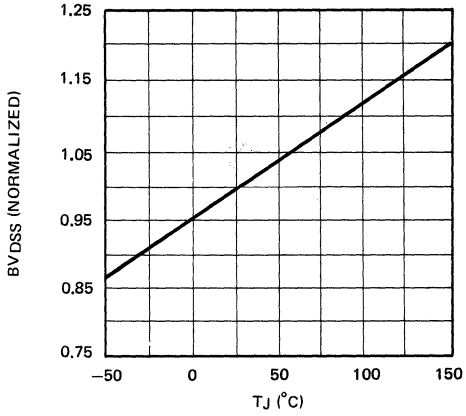


Pulse Condition: 300 μs,2% dutycycle.

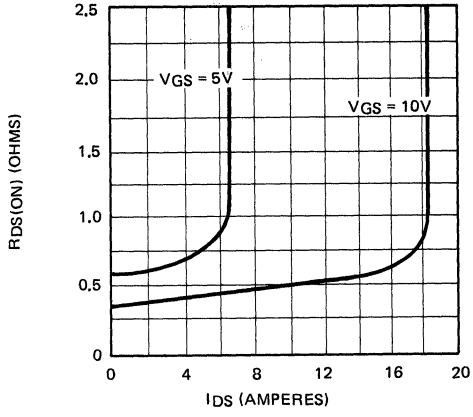
Thermal Response Characteristics



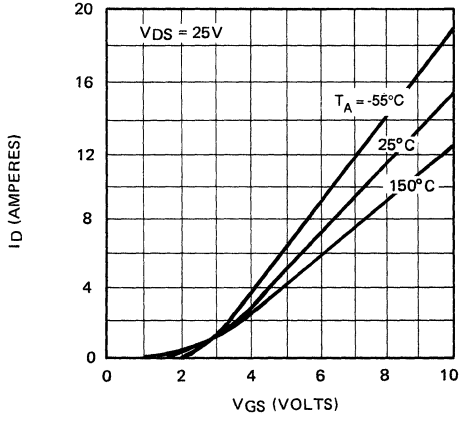
BVDSS Variation with Temperature



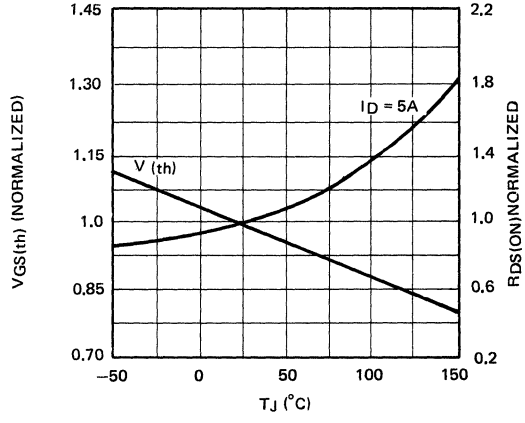
ON - Resistance Vs. Drain Current



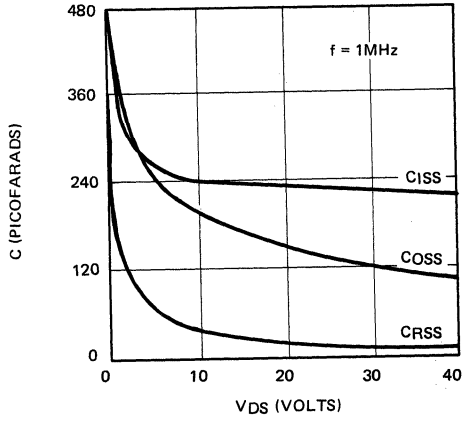
Transfer Characteristics



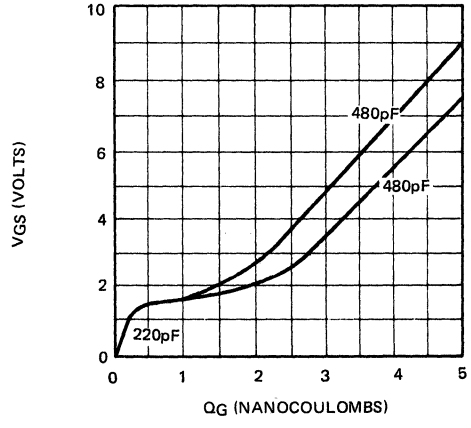
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	Dice
160V	3Ω	2.0A	VN1116N1	VN1116N2	VN1116N5	VN1116ND
200V	3Ω	2.0A	VN1120N1	VN1120N2	VN1120N5	VN1120ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

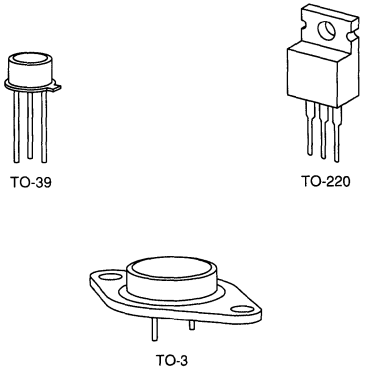
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-3	3A	4.5A	100W	9.1	1.25	3A	4.5A
TO-39	1A	2.5A	4W	33	31	1A	2.5A
TO-220	2A	3.5A	45W	11.4	2.7	2A	3.5A

*I_D (continuous) is limited by max rated T_j.

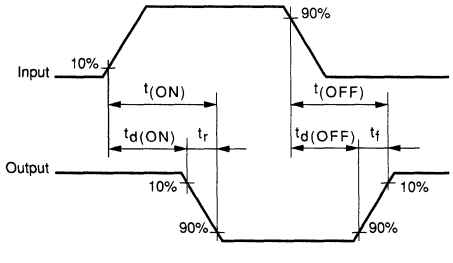
Electrical Characteristics (@ 25°C unless otherwise specified)

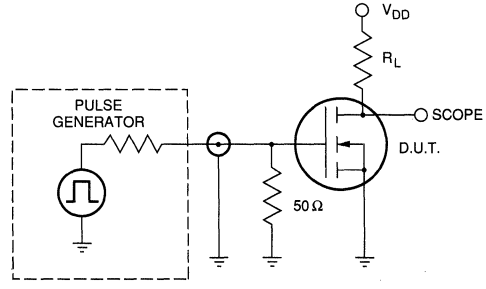
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN1116	160			V	V_{GS} = 0, I_D = 5mA
		VN1120	200				
$V_{GS(th)}$	Gate Threshold Voltage		1		3	V	V_{GS} = V_{DS}, I_D = 5mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.5	-6	mV/°C	V_{GS} = V_{DS}, I_D = 5mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				50	µA	V_{GS} = 0, V_{DS} = Max Rating
					5	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		1	1.5		A	V_{GS} = 5V, V_{DS} = 25V
			2	2.5			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.5	4	Ω	V_{GS} = 5V, I_D = 0.5A
				2.5	3		V_{GS} = 10V, I_D = 1A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.6	1	%/°C	V_{GS} = 10V, I_D = 1A
G_{FS}	Forward Transconductance		0.2	0.4		℧	V_{DS} = 25V, I_D = 0.5A
C_{ISS}	Input Capacitance			300	350	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			75	150		
C_{RSS}	Reverse Transfer Capacitance			20	30		
$t_{d(ON)}$	Turn-ON Delay Time			20	30	ns	V_{DD} = 25V, I_D = 2A, R_S = 50Ω
t_r	Rise Time			3	10		
$t_{d(OFF)}$	Turn-OFF Delay Time			32	40		
t_f	Fall Time			8	15		
V_{SD}	Diode Forward Voltage Drop			0.7	1.0	V	V_{GS} = 0, I_{SD} = 100mA
t_{rr}	Reverse Recovery Time			400		ns	V_{GS} = 0, I_{SD} = 0.1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

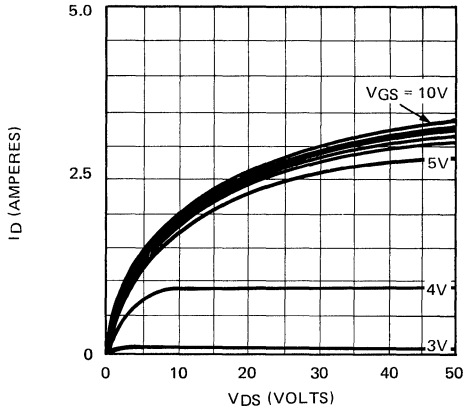
Switching Waveforms and Test Circuit



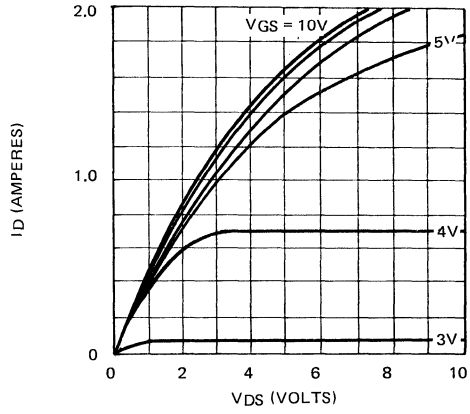


Typical Performance Curves

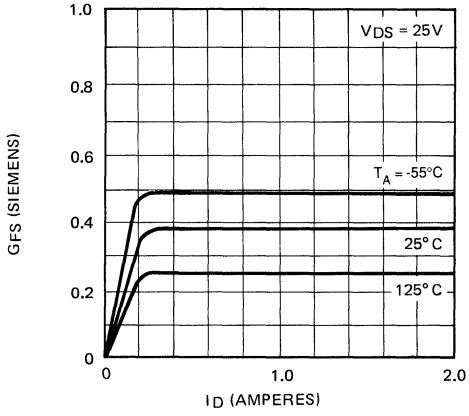
Output Characteristics



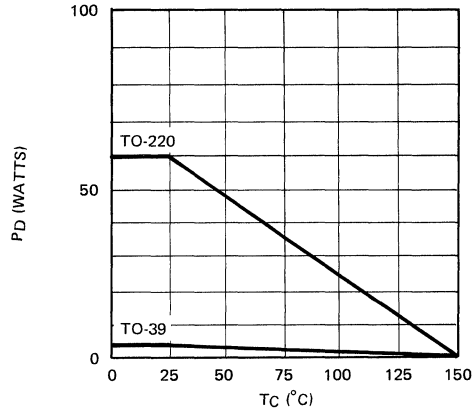
Saturation Characteristics



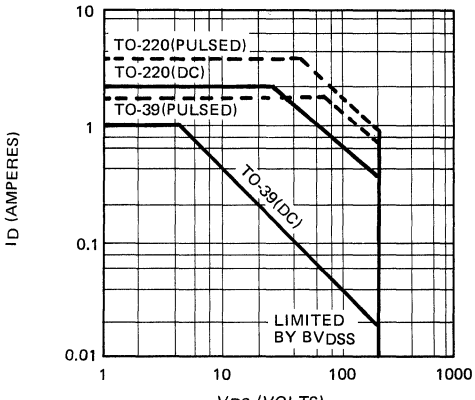
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

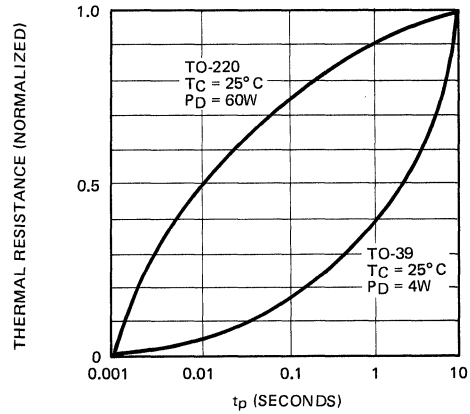


Maximum Rated Safe Operating Area



Pulse Condition: 300 μs, 2% dutycycle.

Thermal Response Characteristics



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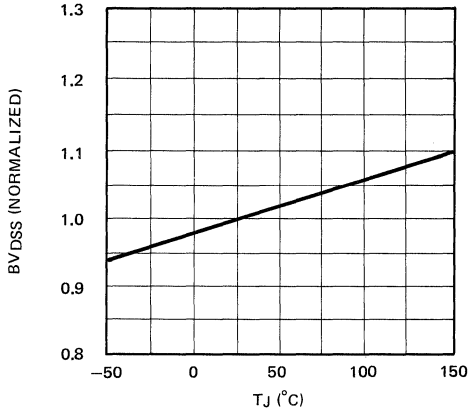
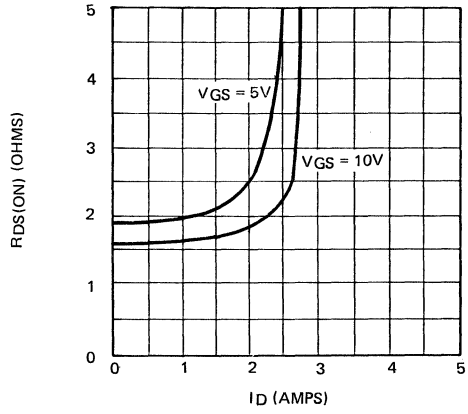
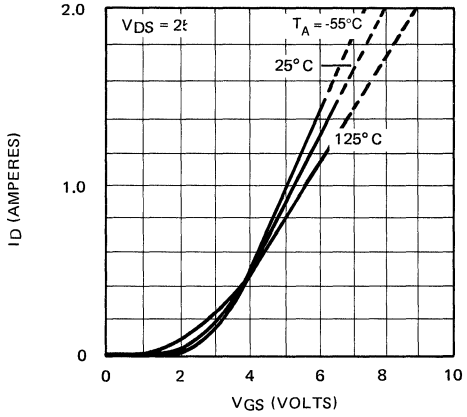
BVDSS Variation with Temperature



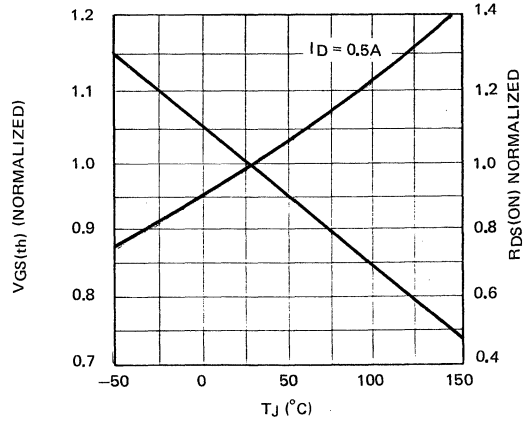
ON-Resistance Vs. Drain Source Current



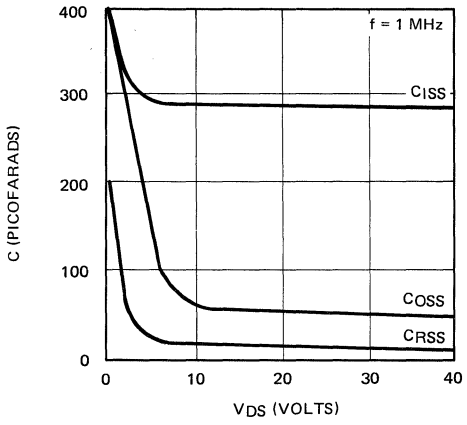
Transfer Characteristics



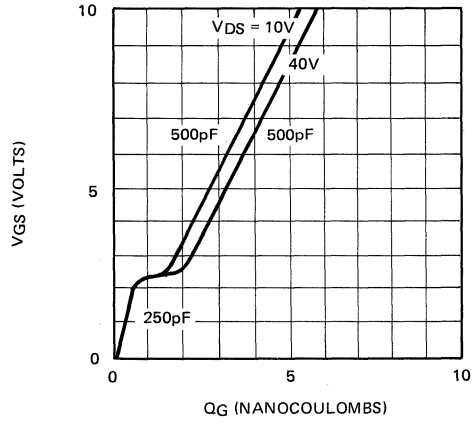
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	Dice
40V	0.3Ω	20A	VN1204N1	VN1204N2	VN1204N5	VN1204ND
60V	0.3Ω	20A	VN1206N1	VN1206N2	VN1206N5	VN1206ND
100V	0.3Ω	20A	VN1210N1	VN1210N2	VN1210N5	VN1210ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

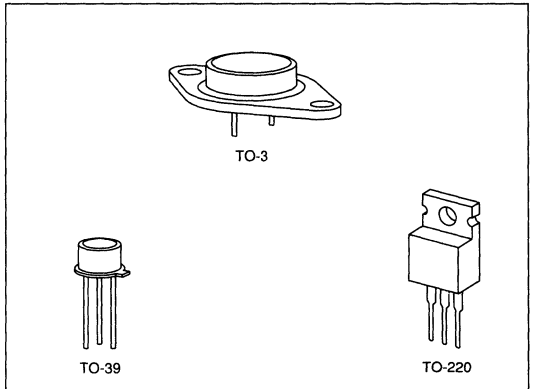
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-3	12A	35A	100W	30	1.25	12A	35A
TO-39	3.5A	15A	6.5W	125	20	3.5A	15A
TO-220	9A	35A	45W	70	2.75	9A	35A

*I_D (continuous) is limited by max rated T_j.

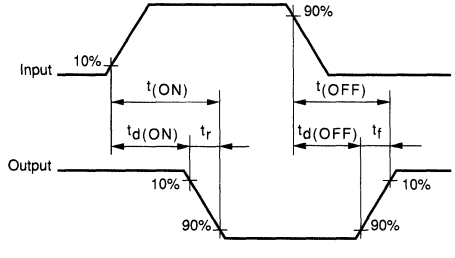
Electrical Characteristics (@ 25°C unless otherwise specified)

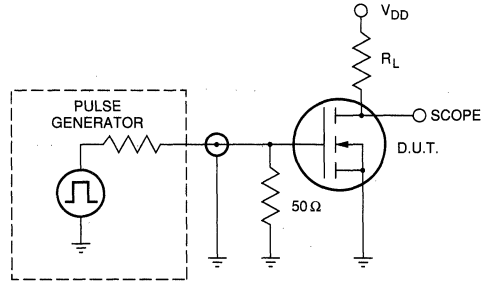
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN1210	100			V	V_{GS} = 0, I_D = 10mA
		VN1206	60				
		VN1204	40				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	V_{GS} = V_{DS}, I_D = 10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.3	-5.5	mV/°C	V_{GS} = V_{DS}, I_D = 10mA
I_{GSS}	Gate Body Leakage			1	100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				100	µA	V_{GS} = 0, V_{DS} = Max Rating
					10	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		5	10		A	V_{GS} = 5V, V_{DS} = 25V
			20	35			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			0.22	0.45	Ω	V_{GS} = 5V, I_D = 2A
				0.2	0.3		V_{GS} = 10V, I_D = 10A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.85	1.2	%/°C	V_{GS} = 10V, I_D = 10A
G_{FS}	Forward Transconductance		4.0	4.5		℧	V_{DS} = 25V, I_D = 2A
C_{ISS}	Input Capacitance			600	650	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			300	350		
C_{RSS}	Reverse Transfer Capacitance			50	75		
$t_{d(ON)}$	Turn-ON Delay Time			8	20	ns	V_{DD} = 25V, I_D = 5A, R_S = 50Ω
t_r	Rise Time			8	20		
$t_{d(OFF)}$	Turn-OFF Delay Time			70	90		
t_f	Fall Time			40	60		
V_{SD}	Diode Forward Voltage Drop			1.2	1.4	V	V_{GS} = 0, I_{SD} = 10A
t_{rr}	Reverse Recovery Time			500		ns	V_{GS} = 0, I_{SD} = 1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

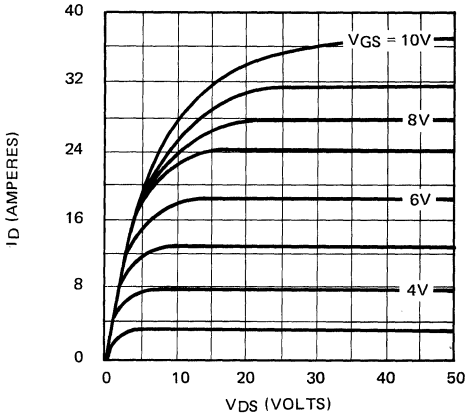
Switching Waveforms and Test Circuit



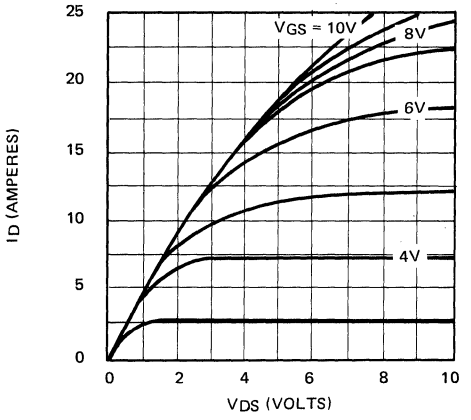


Typical Performance Curves

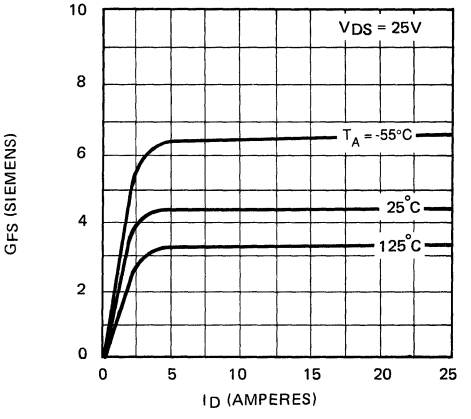
Output Characteristics



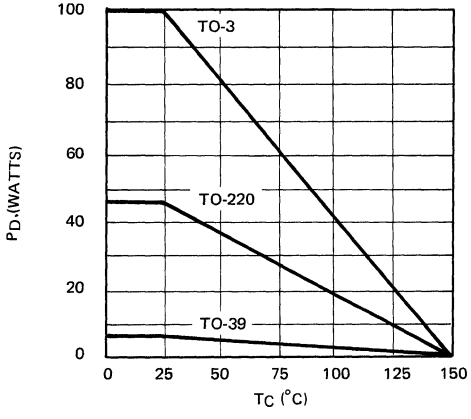
Saturation Characteristics



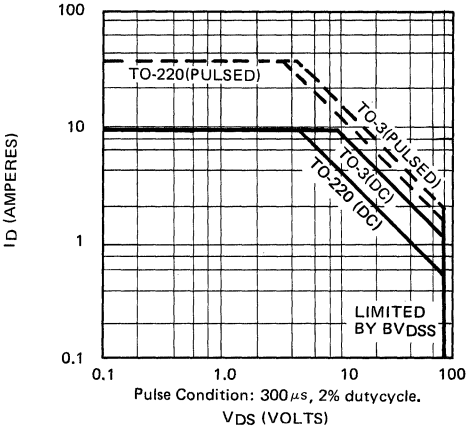
Transconductance Vs. Drain Current



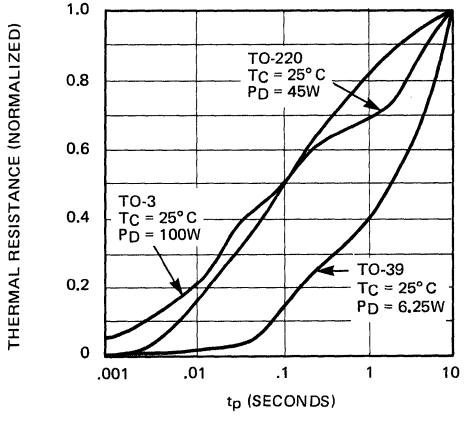
Power Dissipation Vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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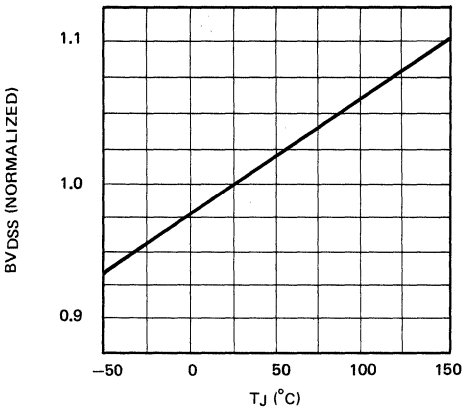
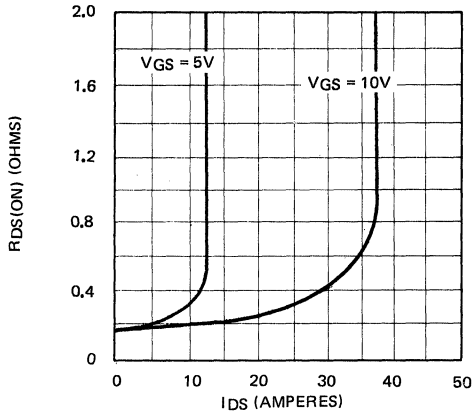
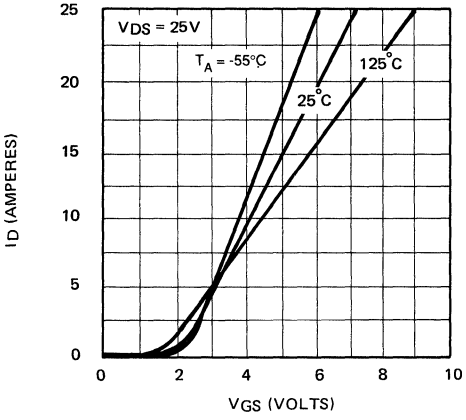
BVDSS Variation with Temperature



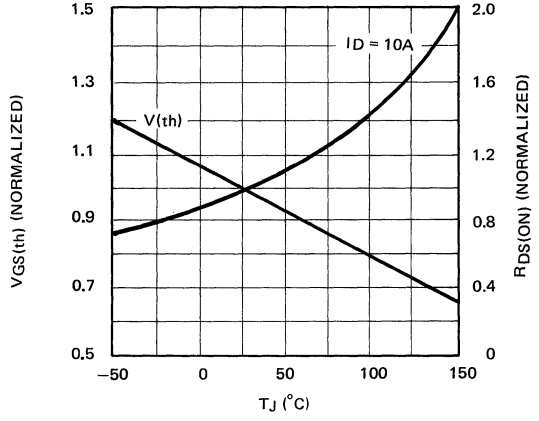
ON - Resistance Vs. Drain Current



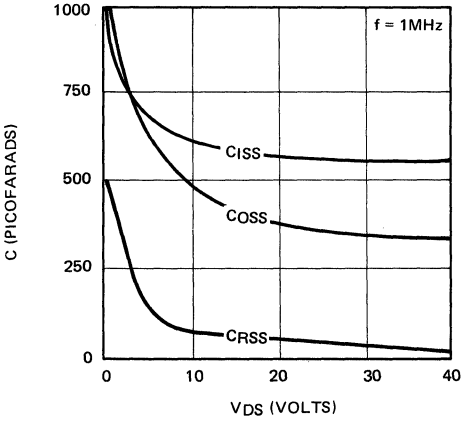
Transfer Characteristics



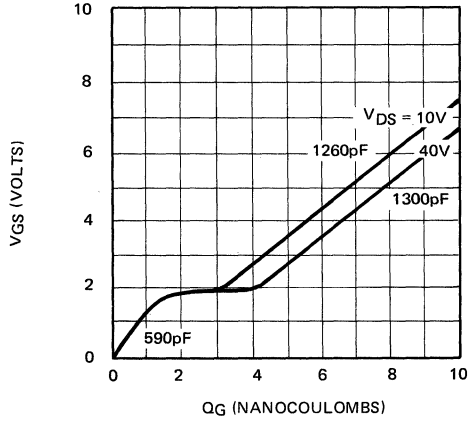
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	Dice
160V	1Ω	6.0A	VN1216N1	VN1216N2	VN1216N5	VN1216ND
200V	1Ω	6.0A	VN1220N1	VN1220N2	VN1220N5	VN1220ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

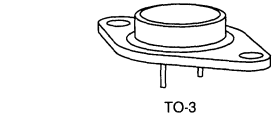
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

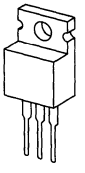
- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-3

TO-39



TO-220

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-3	6.0A	14.0A	100W	30	1.25	6A	14A
TO-39	3.0A	11.0A	6.5W	125	20	3A	11A
TO-220	4.5A	13.0A	45W	70	2.75	4.5A	13A

*I_D (continuous) is limited by max rated T_j.

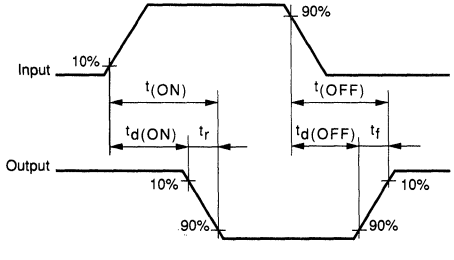
Electrical Characteristics (@ 25°C unless otherwise specified)

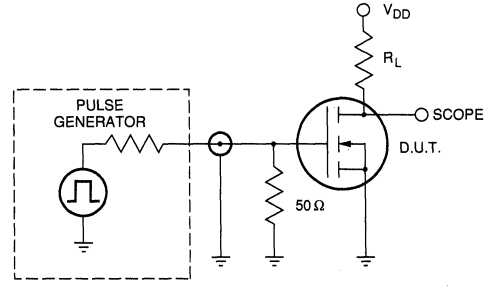
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN1220	200			V	V_{GS} = 0, I_D = 10mA
		VN1216	160				
$V_{GS(th)}$	Gate Threshold Voltage		1		3	V	V_{GS} = V_{DS}, I_D = 10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.7	-4.5	mV/°C	V_{GS} = V_{DS}, I_D = 10mA
I_{GSS}	Gate Body Leakage			1	100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				100	µA	V_{GS} = 0, V_{DS} = Max Rating
					10	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		4	8		A	V_{GS} = 5V, V_{DS} = 25V
			8	12			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			0.7	1.5	Ω	V_{GS} = 5V, I_D = 2A
				0.6	1		V_{GS} = 10V, I_D = 2A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.0	1.4	%/°C	V_{GS} = 10V, I_D = 5A
G_{FS}	Forward Transconductance		2.0	3.2		℧	V_{DS} = 25V, I_D = 5A
C_{ISS}	Input Capacitance			550	650	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			180	250		
C_{RSS}	Reverse Transfer Capacitance			12	20		
$t_{d(ON)}$	Turn-ON Delay Time			8	20	ns	V_{DD} = 25V, I_D = 2A, R_S = 50Ω
t_r	Rise Time			10	20		
$t_{d(OFF)}$	Turn-OFF Delay Time			30	90		
t_f	Fall Time			30	60		
V_{SD}	Diode Forward Voltage Drop			1.3	2.5	V	V_{GS} = 0, I_{SD} = 2A
t_{rr}	Reverse Recovery Time			500		ns	V_{GS} = 0, I_{SD} = 1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

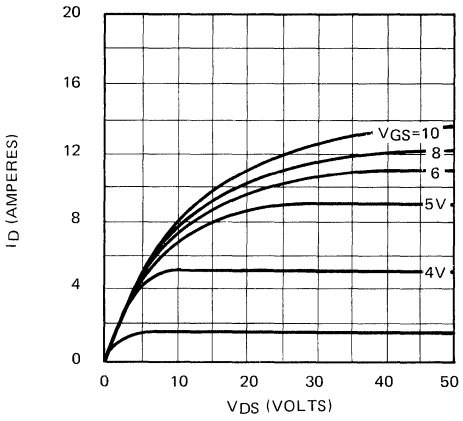
Switching Waveforms and Test Circuit



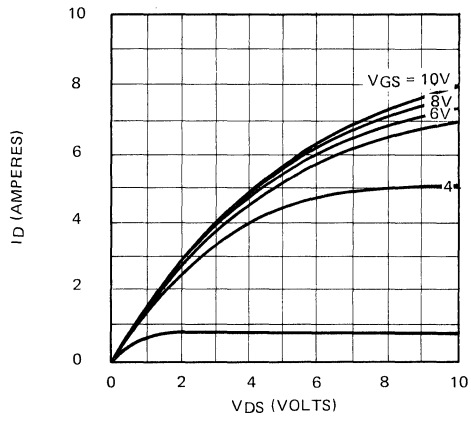


Typical Performance Curves

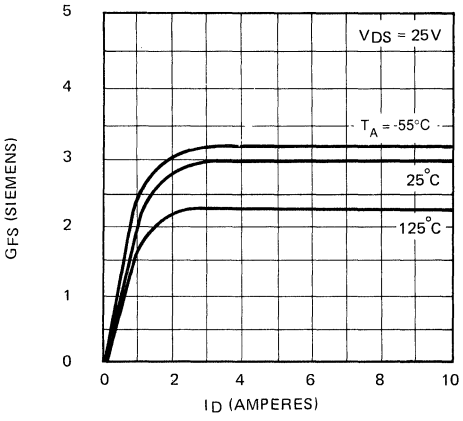
Output Characteristics



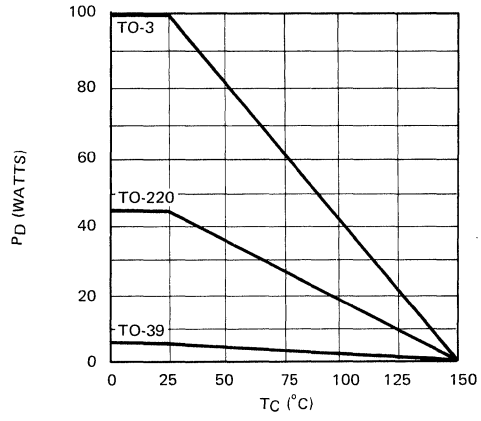
Saturation Characteristics



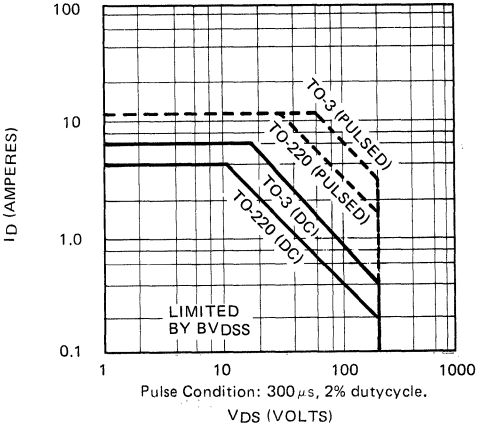
Transconductance Vs. Drain Current



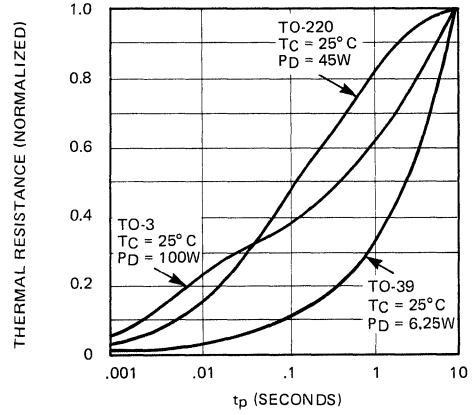
Power Dissipation Vs. Case Temperature



Maximum Rated Safe Operating Area

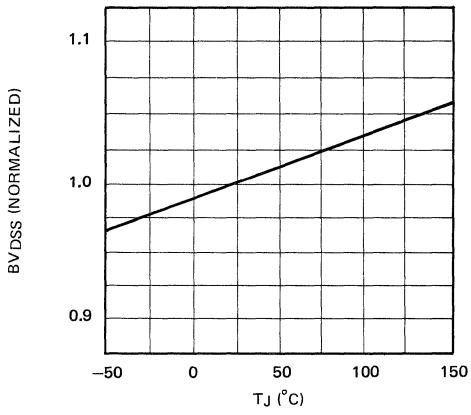


Thermal Response Characteristics

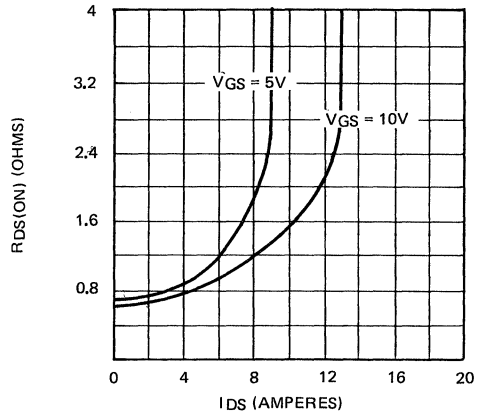


8

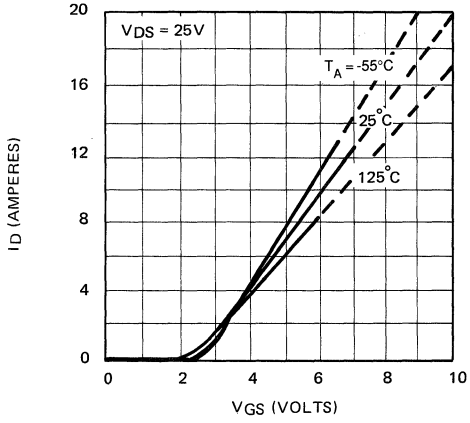
BVDSS Variation with Temperature



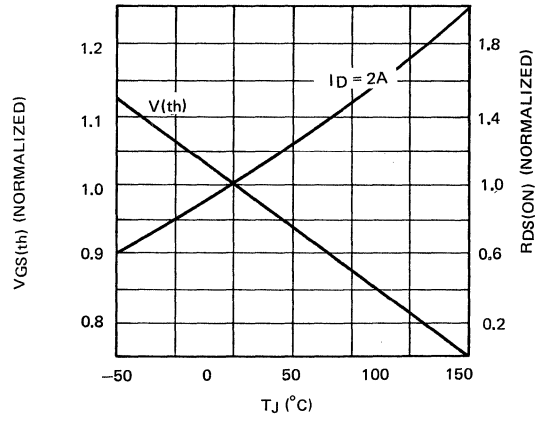
ON-Resistance Vs. Drain Current



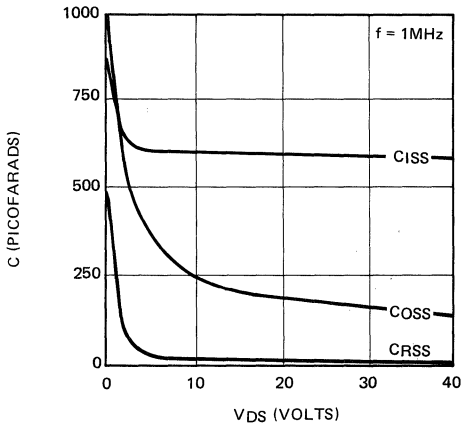
Transfer Characteristics



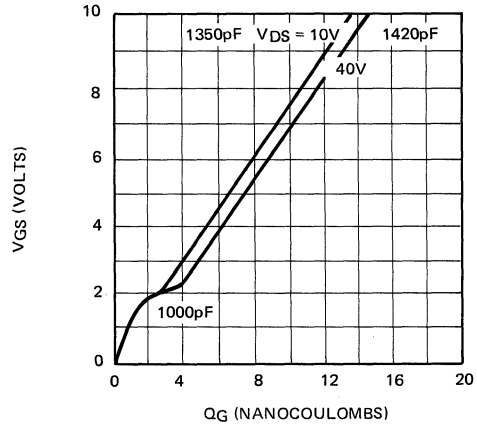
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	TO-220
120V	6Ω	1.0A	VN1206B	VN1206L	VN1206D
120V	10Ω	1.0A	VN1210B	VN1210L	VN1210D

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

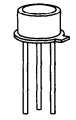
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

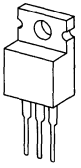
- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-39

TO-92



TO-220

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation	θ_{ja} °C/W	θ_{jc} °C/W
TO-39	0.7A	3.0A	6.25W	170	21
TO-92	0.1A	0.6A	.4W	312.5	21.3
TO-220	1.5A	3.0A	45W	80	6.25

*I_D (continuous) is limited by max rated T_j.

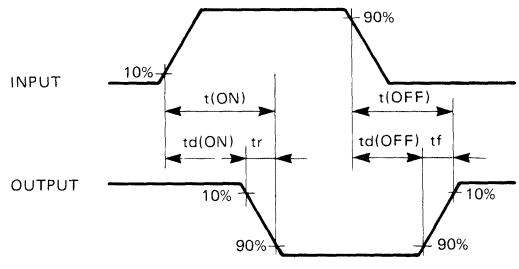
Electrical Characteristics (@ 25°C unless otherwise specified)

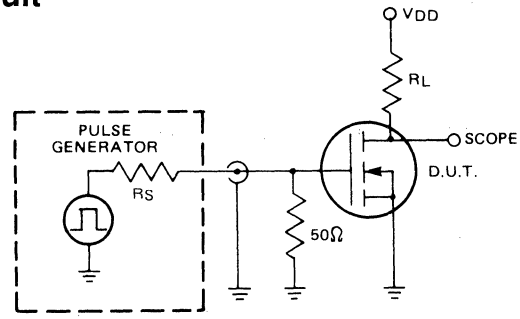
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage		120			V	I_D = 100μA, V_{GS} = 0
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.0	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ±15V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	μA	V_{GS} = 0, V_{DS} = 120V
					500		V_{GS} = 0, V_{DS} = 120V, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		1.0			A	V_{GS} = I0V, V_{DS} ≥ 2 $V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	ALL			10	Ω	V_{GS} = 2.5V, I_D = 0.1A
		VN1206			6		V_{GS} = 10V, I_D = 0.5A
		VN1210			10		I_D = 0.5A, V_{GS} = 10V
G_{FS}	Forward Transconductance		300			m℧	V_{DS} ≥ 2 $V_{DS(ON)}$, I_D = 0.5A
C_{ISS}	Input Capacitance				125	pF	V_{GS} = 0, V_{DS} = 25V, f = 1MHz
C_{OSS}	Common Source Output Capacitance				50		
C_{RSS}	Reverse Transfer Capacitance				20		
$t_{(ON)}$	Turn-ON Time				16	ns	V_{DD} = 60V, I_D = 0.1A, R_S = 50Ω
$t_{(OFF)}$	Turn-OFF Time				57		
V_{SD}	Diode Forward Voltage Drop	VN1210		−1.2		V	I_{SD} = −.12A, V_{GS} = 0
		VN1206		−1.2		V	I_{SD} = −.25A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
40V	8Ω	0.5A	VN1304N2	VN1304N3
60V	8Ω	0.5A	VN1306N2	VN1306N3
100V	8Ω	0.5A	VN1310N2	VN1310N3

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

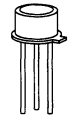
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

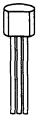
Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-39



TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-39	0.4A	1.4A	3.0W	125	41.5	0.4A	1.4A
TO-92	0.25A	1.3A	1.0W	170	125	0.25A	1.3A

*I_D (continuous) is limited by max rated T_j.

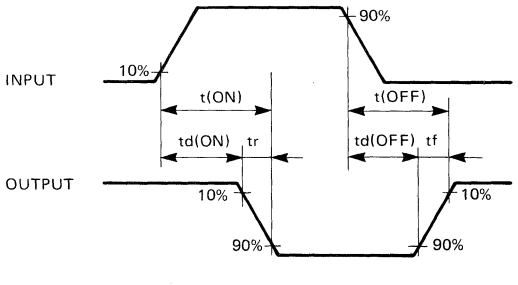
Electrical Characteristics (@ 25°C unless otherwise specified)

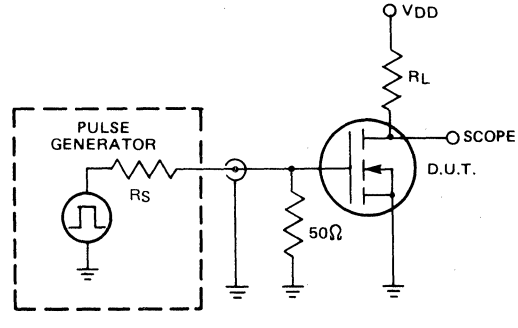
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BVDSS	Drain-to-Source Breakdown Voltage	VN1310	100			V	ID = 1mA, VGS = 0
		VN1306	60				
		VN1304	40				
VGS(th)	Gate Threshold Voltage		0.8		2.4	V	VGS = VDS, ID = 1mA
ΔVGS(th)	Change in VGS(th) with Temperature			−3.9	−5	mV/°C	ID = 1mA, VDS = VGS
IGSS	Gate Body Leakage			0.1	100	nA	VGS = ±20V, VDS = 0
IDSS	Zero Gate Voltage Drain Current				1	uA	VGS = 0, VDS = Max Rating
					100		VGS = 0, VDS = 0.8 Max Rating, TA = 125°C
ID(ON)	ON-State Drain Current		0.25	0.6		A	VGS = 5V, VDS = 25V
			0.50	1.4			VGS = 10V, VDS = 25V
RDS(ON)	Static Drain-to-Source ON-State Resistance			5	15	Ω	VGS = 5V, ID = 50mA
				5	8		VGS = 10V, ID = 500mA
ΔRDS(ON)	Change in RDS(ON) with Temperature			0.8	2	%/°C	ID = 500mA, VGS = 10V
GFS	Forward Transconductance		200	250		m℧	VDS = 25V, ID = 500mA
CISS	Input Capacitance			27	35	pF	VGS = 0V, VDS = 25V, f = 1 MHz
COSS	Common Source Output Capacitance			13	15		
CRSS	Reverse Transfer Capacitance			3	5		
td(ON)	Turn-ON Delay Time			2	5	ns	VDD = 25V, ID = 500mA, RS = 50Ω
tr	Rise Time			2	5		
td(OFF)	Turn-OFF Delay Time			2	5		
tf	Fall Time			2	5		
VSD	Diode Forward Voltage Drop			1.0	1.3	V	ISD = 1.0A, VGS = 0
trr	Reverse Recovery Time			350		ns	ISD = 1.0A, VGS = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

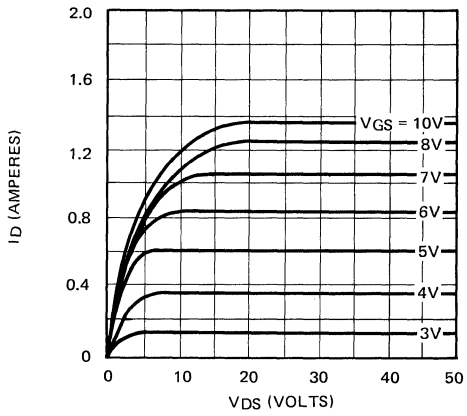
Switching Waveforms and Test Circuit



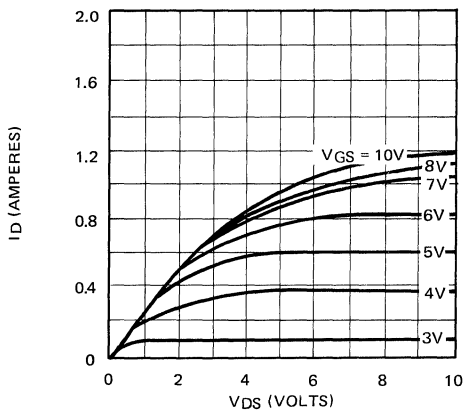


Typical Performance Curves

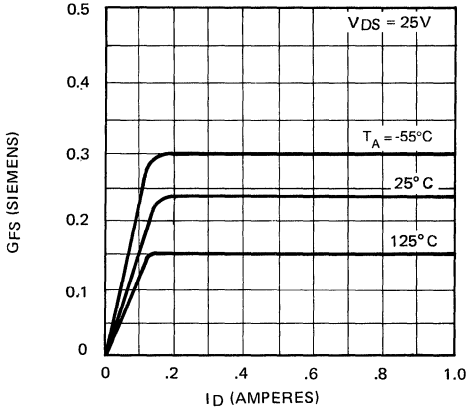
Output Characteristics



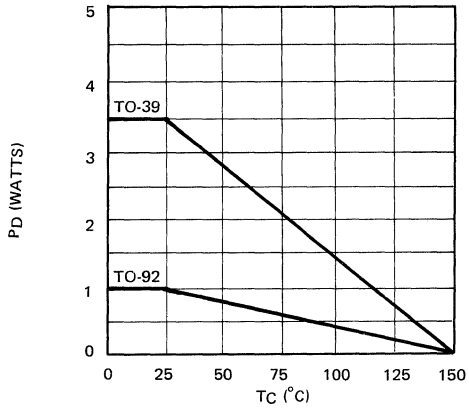
Saturation Characteristics



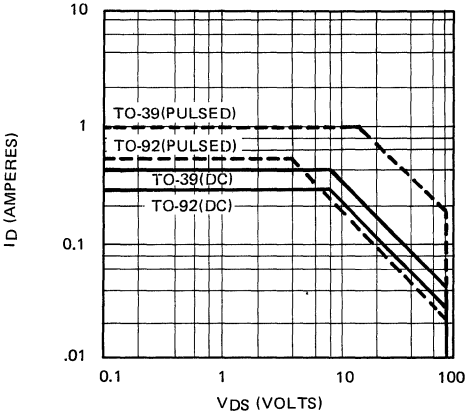
Transconductance Vs. Drain Current



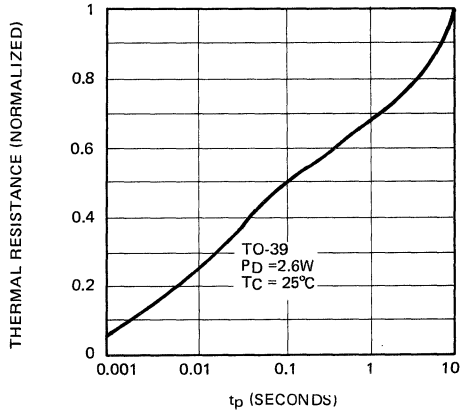
Power Dissipation Vs. Case Temperature



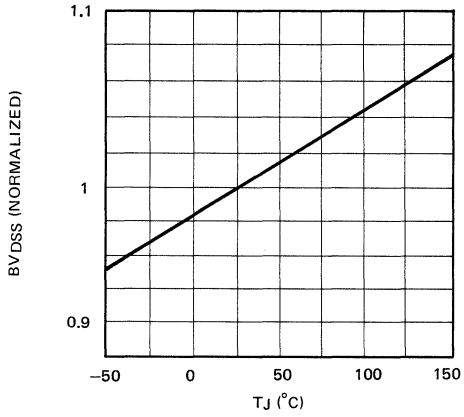
Maximum Rated Safe Operating Area



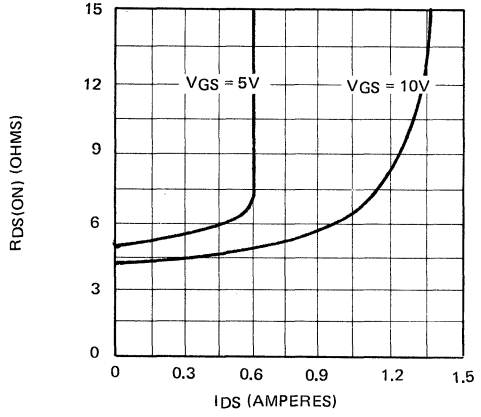
Thermal Response Characteristics



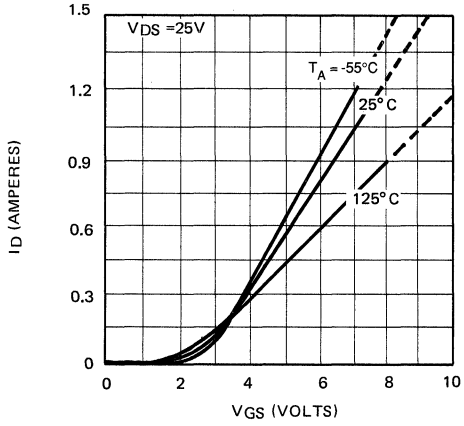
BVDSS Variation with Temperature



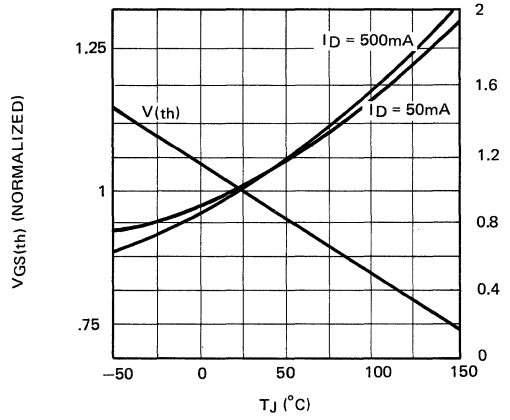
ON - Resistance Vs. Drain Current



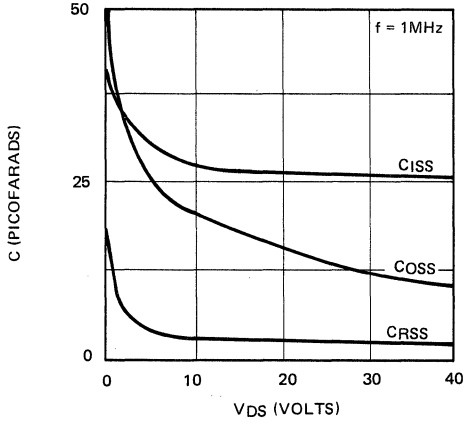
Transfer Characteristics



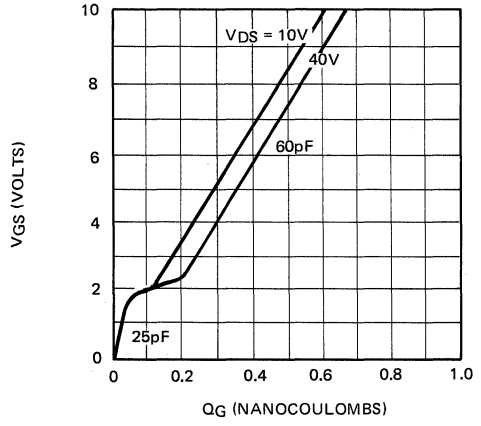
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
160V	40Ω	250mA	VN1316N2	VN1316N3
200V	40Ω	250mA	VN1320N2	VN1320N3

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
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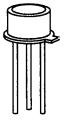
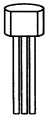
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-39



TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-39	150mA	450mA	3.0W	125	41.5	150mA	450mA
TO-92	100mA	400mA	0.8W	155		100mA	400mA

*I_D (continuous) is limited by max rated T_j.

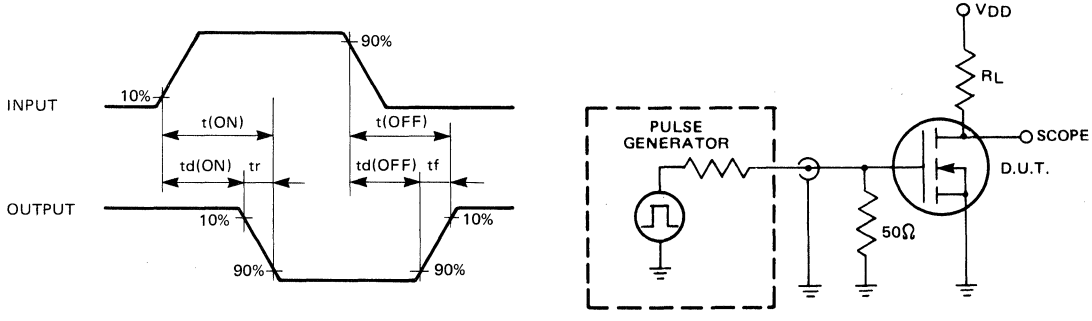
Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BVDSS	Drain-to-Source Breakdown Voltage	VN1320	200			V	ID = 1mA, VGS = 0
		VN1316	160				
VGS(th)	Gate Threshold Voltage		1.5		3.5	V	VGS = VDS, ID = 1mA
ΔVGS(th)	Change in VGS(th) with Temperature			– 2.0	-4.0	mV/°C	VGS = VDS, ID = 1mA
IGSS	Gate Body Leakage				100	nA	VGS = ±20V, VDS = 0
IDSS	Zero Gate Voltage Drain Current				10	μA	VGS = 0, VDS = Max Rating
					500		VGS = 0, VDS = 0.8 Max Rating, TA = 125°C
ID(ON)	ON-State Drain Current		50	160		mA	VGS = 5V, VDS = 25V
			250	300		mA	VGS = 10V, VDS = 25V
RDS(ON)	Static Drain-to-Source ON-State Resistance			30	40	Ω	VGS = 5V, ID = 50mA
				25	40		VGS = 10V, ID = 100mA
ΔRDS(ON)	Change in RDS(ON) with Temperature			0.8	2.0	%/°C	ID = 100mA, VGS = 10V
GFS	Forward Transconductance		50	70		m℧	VDS = 25V, ID = 100mA
CISS	Input Capacitance			25	35	pF	VGS = 0, VDS = 25V, f = 1 MHz
COSS	Common Source Output Capacitance			10	15		
CRSS	Reverse Transfer Capacitance			3	5		
td(ON)	Turn-ON Delay Time			1.5	5	ns	VDD = 25V, ID = 0.2A, RS = 50Ω
tr	Rise Time			2	5		
td(OFF)	Turn-OFF Delay Time			1.5	5		
tf	Fall Time			2	5		
VSD	Diode Forward Voltage Drop			1.2	2.0	V	ISD = 1A, VGS = 0
trr	Reverse Recovery Time			300		ns	ISD = 1A, VGS = 0

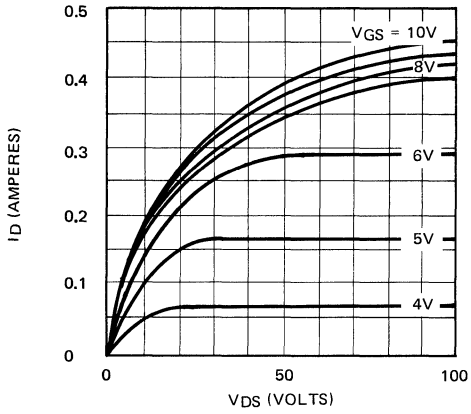
Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

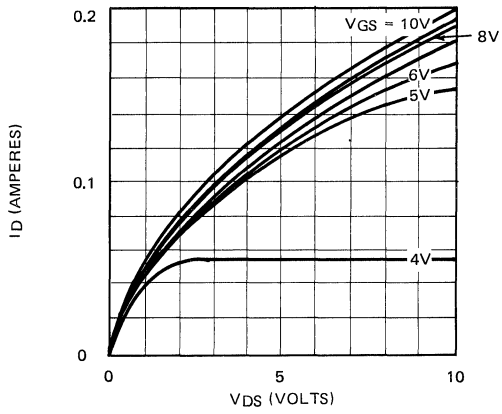


Typical Performance Curves

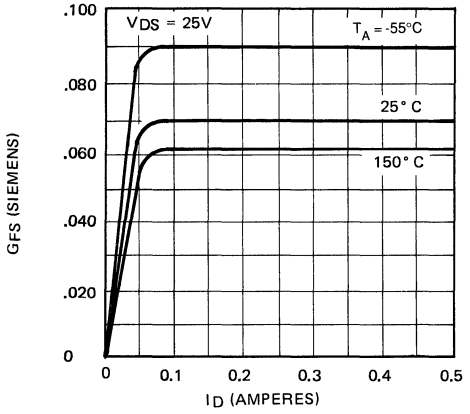
Output Characteristics



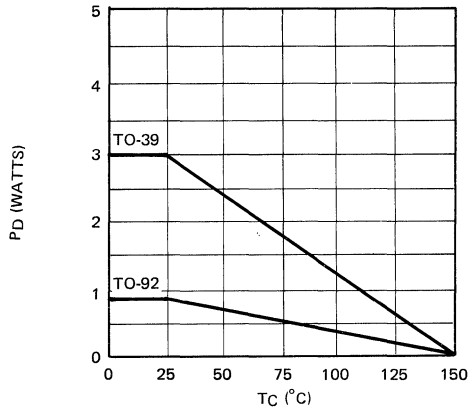
Saturation Characteristics



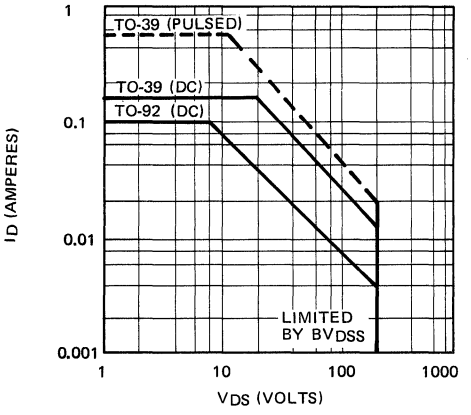
Transconductance Vs. Drain Current



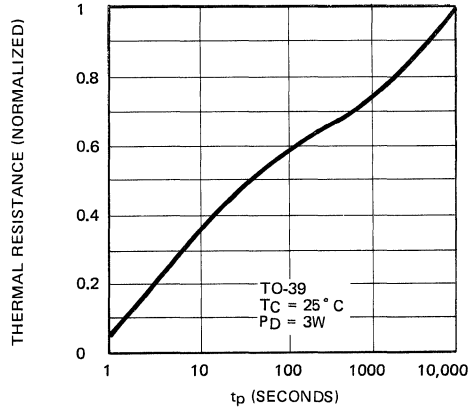
Power Dissipation Vs. Case Temperature



Maximum Rated Safe Operating Area

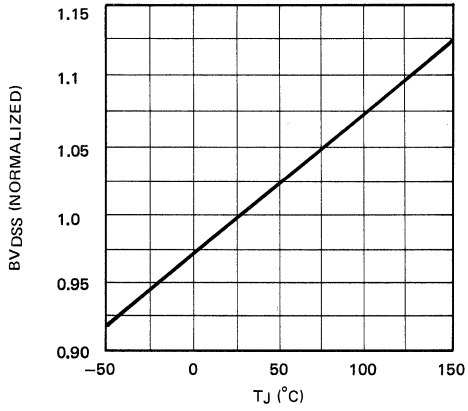


Thermal Response Characteristics

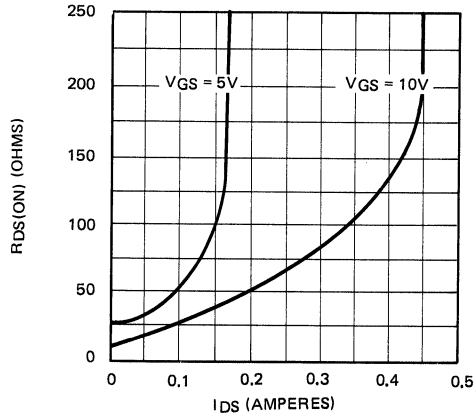


8

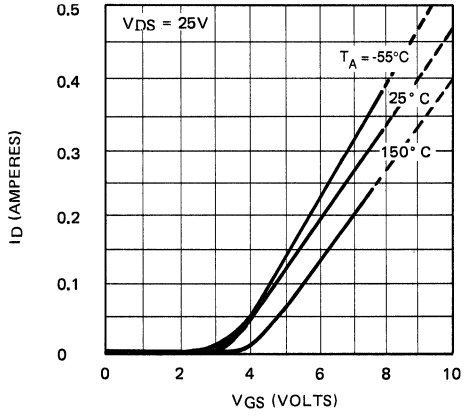
BVDSS Variation with Temperature



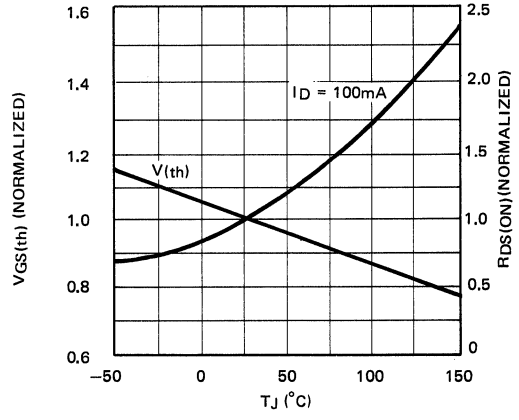
ON - Resistance Vs .Drain Current



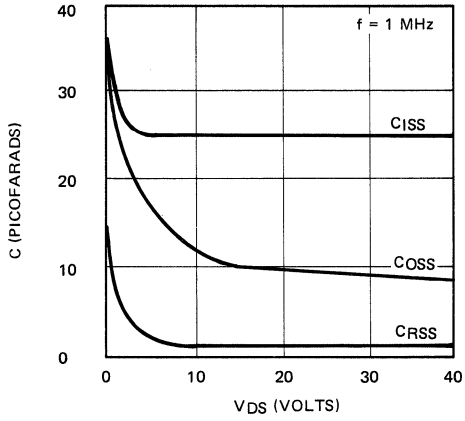
Transfer Characteristics



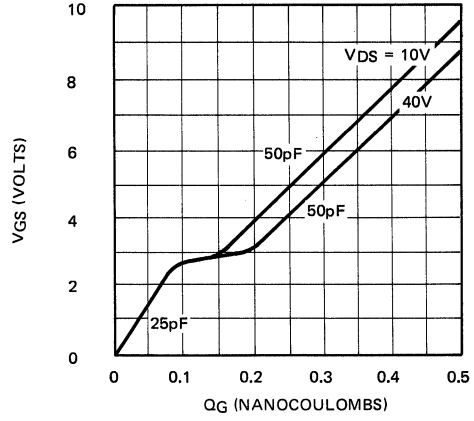
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	TO-220
170V	6Ω	1.0A	VN1706B	VN1706L	VN1706D
170V	10Ω	1.0A	VN1710B	VN1710L	VN1710D

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

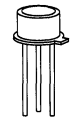
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

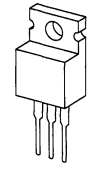
- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-39

TO-92



TO-220

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation	θ_{ja} °C/W	θ_{jc} °C/W
TO-39	0.63A	3.0A	6.25W	170	20
TO-92	0.158A	0.6A	0.4W	312.5	21.3
TO-220	0.7A	3A	20W	80	6.25

*I_D (continuous) is limited by max rated T_j.

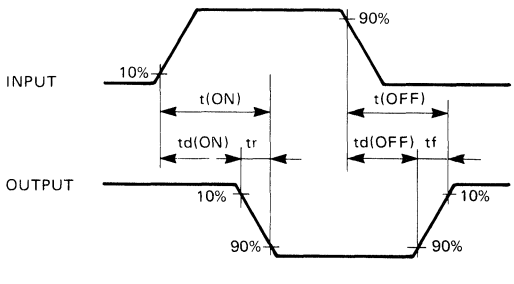
Electrical Characteristics (@ 25°C unless otherwise specified)

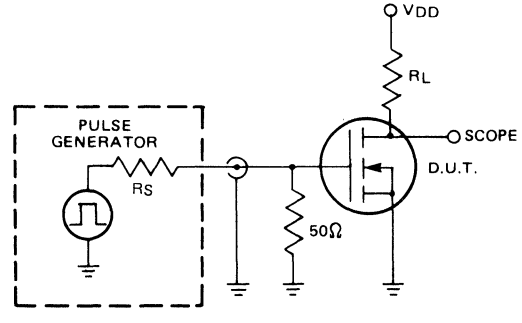
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage		170			V	I_D = 100μA, V_{GS} = 0
$V_{GS(th)}$	Gate Threshold Voltage		.8		2	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = 15V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	μA	V_{GS} = 0V, V_{DS} = 120V
					500		V_{GS} = 0V, V_{DS} = 120V, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		1.0			A	V_{GS} = −10V, V_{DS} ≥ 2 $V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	ALL			10	Ω	V_{GS} = 2.5V, I_D = 0.1A
		VN1710			10		V_{GS} = 10V, I_D = 0.5A
		VN1706			6		I_D = 0.5A V_{GS} = 10V
G_{FS}	Forward Transconductance		300			m℧	V_{DS} ≥ 2 $V_{DS(ON)}$, I_D = 0.5A
C_{ISS}	Input Capacitance				125	pF	V_{GS} = 0, V_{DS} = 25V, f = 1MHz
C_{OSS}	Common Source Output Capacitance				50		
C_{RSS}	Reverse Transfer Capacitance				20		
$t_{(ON)}$	Turn-ON Time				8	ns	V_{DD} = 60V, I_D = 0.1A, R_S = 50Ω
$t_{(OFF)}$	Turn-OFF Time				17		
V_{SD}	Diode Forward Voltage Drop	VN1710		−1.2		V	I_{SD} = −0.19, V_{GS} = 0
		VN1706		−1.2			I_{SD} = −1.4A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Preliminary

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	Order Number / Package
			TO-92
200V	10Ω	1.5V	VN2010L

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)
- ☐ Telecom Switching

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options (Note 1)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-92	250mA	1.0A	1W	125	170	250mA	1.0A

*I_D (continuous) is limited by max rated T_j.

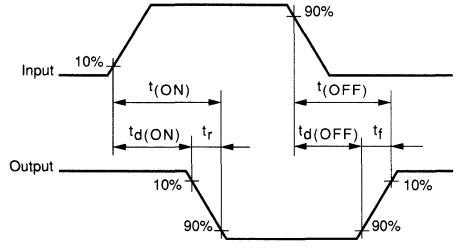
Electrical Characteristics (@ 25°C unless otherwise specified)

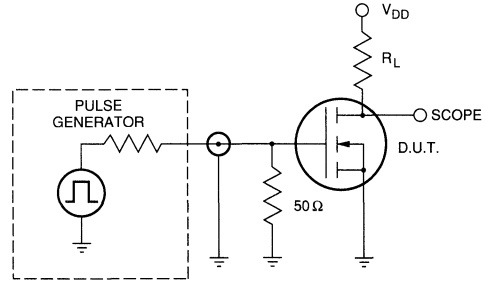
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	200			V	V_{GS} = 0, I_D = 100µA
$V_{GS(th)}$	Gate Threshold Voltage	0.6		1.5	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage			10	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			10	µA	V_{GS} = 0, V_{DS} = Max Rating
				100		V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$V_{DS(ON)}$	Static Drain-Source ON-State Voltage			0.5	V	V_{GS} = 4.5V, I_D = 50mA
				1	V	V_{GS} = 10V, I_D = 100mA
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			10	Ω	V_{GS} = 4.5V, I_D = 50mA
				10	Ω	V_{GS} = 10V, I_D = 100mA
G_{FS}	Forward Transconductance	125			m℧	V_{DS} = 25V, I_D = 100mA
C_{ISS}	Input Capacitance			60	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			30		
C_{RSS}	Reverse Transfer Capacitance			15		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	V_{DD} = 25V, I_D = 100mA, R_S = 50Ω
$t_{d(OFF)}$	Turn-OFF Delay Time			30	ns	V_{DD} = 25V, I_D = 100mA, R_S = 50Ω
V_{SD}	Diode Forward Voltage Drop			1.2	V	V_{GS} = 0, I_{SD} = 250mA

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

Preliminary

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			DIE	WAFER
60V	0.3Ω	10A	VN2206ND	VN2206NW
100V	0.3Ω	10A	VN2210ND	VN2210NW

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

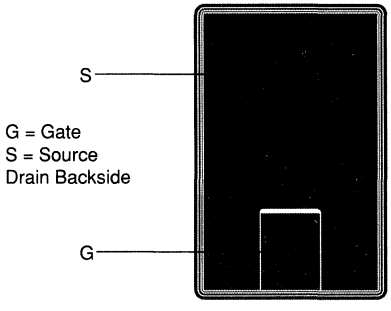
Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Specifications

- ☐ Die Size: 70 X 105 Mil
- ☐ Die Thickness: 11 ± 1.5 Mil
- ☐ Bonding Pad Size: Gate = 20 X 27 Mil
  Source = 20 X 27 Mil
- ☐ Recommended Bonding Wire Size: 8 Mil
- ☐ Backside Metal: Au (CrAg optional)

Die Geometry



Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics (@ θ_{jc} = 1.25°C/W)

I_D (continuous)*	I_D (pulsed)*	I_{DR}	I_{DRM}*
8A	15A	8A	15A

*I_D (continuous) is limited by max rated T_j.

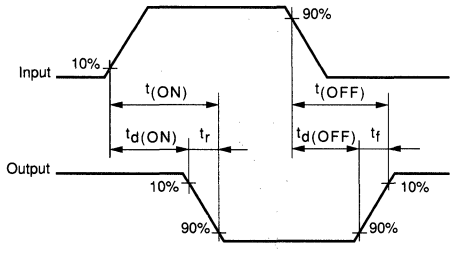
Electrical Characteristics (@ 25°C unless otherwise specified)

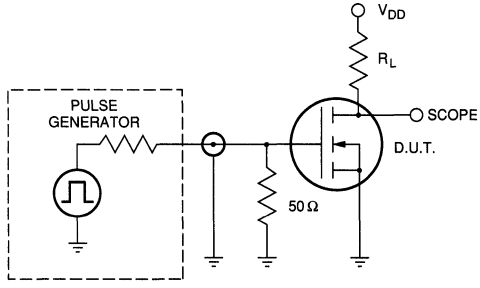
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN2206	60			V	V_{GS} = 0, I_D = 10mA
		VN2210	100				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	V_{GS} = V_{DS}, I_D = 10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.3	-5.5	mV/°C	V_{GS} = V_{DS}, I_D = 10mA
I_{GSS}	Gate Body Leakage			1	100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				50	µA	V_{GS} = 0, V_{DS} = Max Rating
					10	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		3	5		A	V_{GS} = 5V, V_{DS} = 25V
			8				V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			0.22	0.45	Ω	V_{GS} = 5V, I_D = 1A
				0.2	0.3		V_{GS} = 10V, I_D = 4A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.85	1.2	%/°C	V_{GS} = 10V, I_D = 10A
G_{FS}	Forward Transconductance		2.0	3.0		℧	V_{DS} = 25V, I_D = 2A
C_{ISS}	Input Capacitance				500	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance				300		
C_{RSS}	Reverse Transfer Capacitance				125		
$t_{d(ON)}$	Turn-ON Delay Time			8	15	ns	V_{DD} = 25V, I_D = 5A, R_S = 50Ω
t_r	Rise Time			8	15		
$t_{d(OFF)}$	Turn-OFF Delay Time			70	90		
t_f	Fall Time			40	60		
V_{SD}	Diode Forward Voltage Drop			1.2	1.4	V	V_{GS} = 0, I_{SD} = 4A
t_{rr}	Reverse Recovery Time			500		ns	V_{GS} = 0, I_{SD} = 1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





N-Channel Enhancement-Mode Vertical DMOS Power FET

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			TO-92
60V	7.5Ω	0.75A	VN2222LL

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Note 1)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)* T_C = 100°C	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W
TO-92	±.099A	±1A	.4W	312.5	51

* I_D (continuous) is limited by max rated T_j.

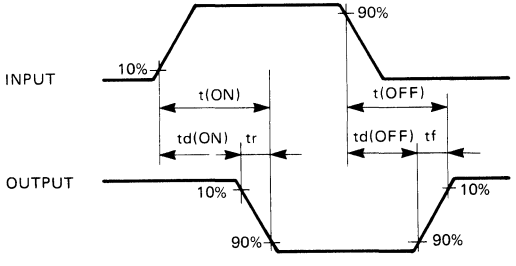
Electrical Characteristics (@ 25°C unless otherwise specified)

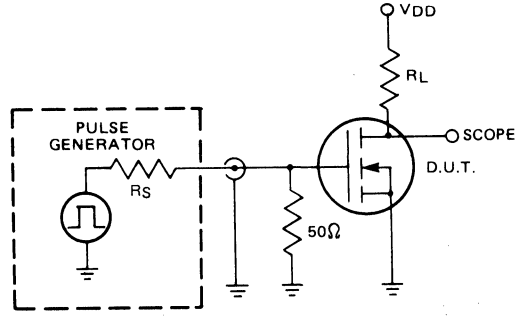
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60			V	I_D = 100μA, V_{GS} = 0
$V_{GS(th)}$	Gate Threshold Voltage	0.6		2.5	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage			100	nA	V_{GS} = 15V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{GS} = 0, V_{DS} = 50V
				500		V_{GS} = 0, V_{DS} = 50V T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	.75			A	V_{GS} = −10V, V_{DS} ≥ 2 $V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			7.5	Ω	V_{GS} = 5V, I_D = .2A
				7.5		V_{GS} = 10V, I_D = .5A
G_{FS}	Forward Transconductance	100			m℧	V_{DS} ≥ 2 $V_{DS(ON)}$, I_D = 0.5A
C_{ISS}	Input Capacitance			60	pF	V_{GS} = 0, V_{DS} = 15V f = 1MHz
C_{OSS}	Common Source Output Capacitance			25		
C_{RSS}	Reverse Transfer Capacitance			5		
$t_{(ON)}$	Turn-ON Time			10	ns	V_{DD} = 15V, I_D = 0.6A R_S = 50Ω
$t_{(OFF)}$	Turn-OFF Time			10		
V_{SD}	Diode Forward Voltage Drop		−.85		V	I_{SD} = −.2A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	TO-220
240V	6Ω	1.0A	VN2406B	VN2406L	VN2406D
240V	10Ω	1.0A	VN2410B	VN2410L	VN2410D

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

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Applications

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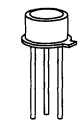
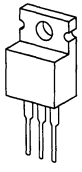
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-39

TO-92



TO-220

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation	θ_{ja} °C/W	θ_{jc} °C/W
TO-39	0.7A	3.0A	6.25W	170	21
TO-92	0.158A	0.6A	0.4W	312.5	21.3
TO-220	1.5A	3.0A	45W	80	6.25

*I_D (continuous) is limited by max rated T_j.

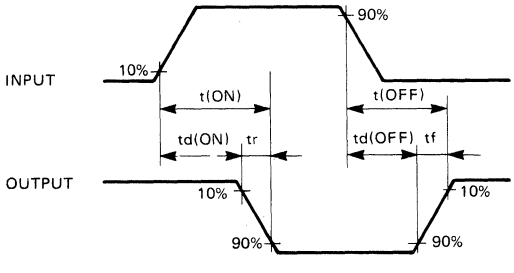
Electrical Characteristics (@ 25°C unless otherwise specified)

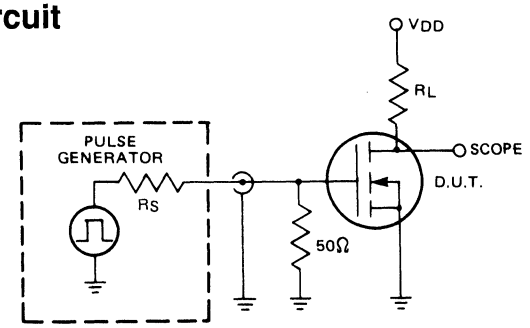
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage		240			V	I_D = 100μA, V_{GS} = 0
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.0	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = 15V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	μA	V_{GS} = 0V, V_{DS} = 120V
					500		V_{GS} = 0V, V_{DS} = 120V, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		1.0			A	V_{GS} = −10V, V_{DS} ≥ 2$V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	ALL			10	Ω	V_{GS} = 2.5V, I_D = 0.1A
		VN2410			10		V_{GS} = 10V, I_D = 0.5A
		VN2406			6		V_{GS} = 10V, I_D = 0.5A
G_{FS}	Forward Transconductance		300			m℧	V_{DS} ≥ 2 $V_{DS(ON)}$, I_D = 0.5A
C_{ISS}	Input Capacitance				125	pF	V_{GS} = 0, V_{DS} = 25V, f = 1MHz
C_{OSS}	Common Source Output Capacitance				50		
C_{RSS}	Reverse Transfer Capacitance				20		
$t_{d(ON)}$	Turn-ON Delay Time				8	ns	V_{DD} = 60V, I_D = 0.1A, R_S = 50Ω
t_r	Rise Time				8		
$t_{d(OFF)}$	Turn-OFF Delay Time				18		
t_f	Fall Time				12		
V_{SD}	Diode Forward Voltage Drop	VN2410		−1.2		V	I_{SD} = 0.19A, V_{GS} = 0
		VN2406		−1.2		V	I_{SD} = 0.8A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	Order Number / Package
			TO-92
350V	15Ω	1.5V	VN3515L
400V	12Ω	1.5V	VN4012L

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

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Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Telecom Switching
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Note 1)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
VN3515L	180mA	720mA	1W	125	170	180mA	720mA
VN4012L	200mA	800mA	1W	125	170	200mA	800mA

*I_D (continuous) is limited by max rated T_j.

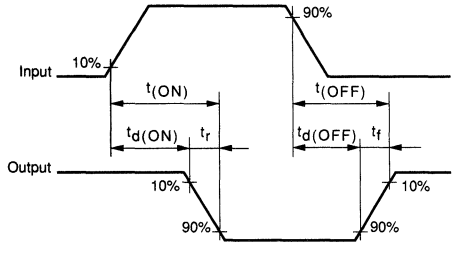
Electrical Characteristics (@ 25°C unless otherwise specified)

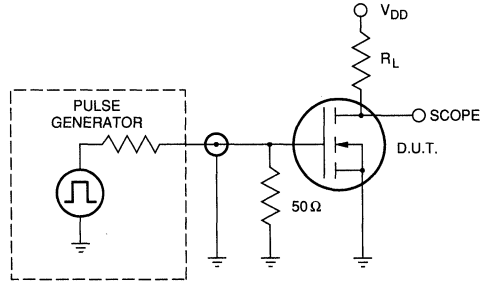
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN3515	350			V	V_{GS} = 0, I_D = 100μA
		VN4012	400				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.5	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage				10	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	μA	V_{GS} = 0, V_{DS} = Max Rating
					100		V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$V_{DS(ON)}$	Static Drain-Source ON-State Voltage	VN3515			1.5	V	V_{GS} = 4.5V, I_D = 100mA
		VN4012			1.2		
		VN3515			1.5	V	V_{GS} = 10V, I_D = 100mA
		VN4012			1.2		
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	VN3515			15	Ω	V_{GS} = 4.5V, I_D = 100mA
		VN4012			12		
		VN3515			15	Ω	V_{GS} = 10V, I_D = 100mA
		VN4012			12		
G_{FS}	Forward Transconductance		125			m℧	V_{DS} = 25V, I_D = 100mA
C_{ISS}	Input Capacitance				90	pF	V_{GS} = 0, V_{DS} = 25V
C_{OSS}	Common Source Output Capacitance				20		
C_{RSS}	Reverse Transfer Capacitance				5		
$t_{d(ON)}$	Turn-ON Delay Time				20	ns	V_{DD} = 25V, I_D = 100mA, R_S = 50Ω
$t_{d(OFF)}$	Turn-OFF Delay Time				65	ns	V_{DD} = 25V, I_D = 100mA, R_S = 50Ω
V_{SD}	Diode Forward Voltage Drop				1.2	V	V_{GS} = 0, I_{SD} = 180mA

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

Objective

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	Order Number / Package
			TO-92
600V	35Ω	2.8V	VN6035L

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

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8

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Telecom Switching
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-92	110mA	500mA	1W	125	170	110mA	500mA

*I_D (continuous) is limited by max rated T_j.

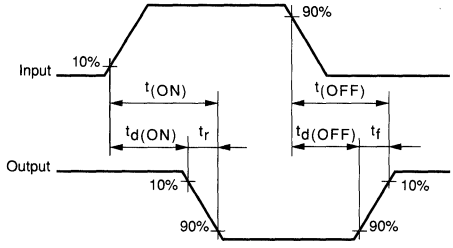
Electrical Characteristics (@ 25°C unless otherwise specified)

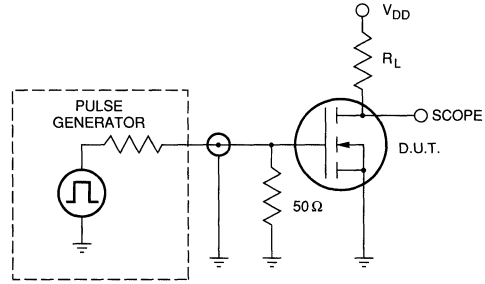
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	600			V	V_{GS} = 0, I_D = 100µA
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.8	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage			10	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			50	µA	V_{GS} = 0, V_{DS} = Max Rating
				200		V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$V_{DS(ON)}$	Static Drain-Source ON-State Voltage			1.75	V	V_{GS} = 10V, I_D = 50mA
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			35	Ω	V_{GS} = 10V, I_D = 50mA
G_{FS}	Forward Transconductance	0.100			℧	V_{DS} = 25V, I_D = 50mA
C_{ISS}	Input Capacitance			80	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			20		
C_{RSS}	Reverse Transfer Capacitance			10		
$t_{d(ON)}$	Turn-ON Delay Time			20	ns	V_{DD} = 25V, I_D = 50mA, R_S = 50Ω
$t_{d(OFF)}$	Turn-OFF Delay Time			100	ns	V_{DD} = 25V, I_D = 50mA, R_S = 50Ω
V_{SD}	Diode Forward Voltage Drop			1.2	V	V_{GS} = 0, I_S = 110mA, T_A = 25°C

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Preliminary

P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-220	TO-92
-60V	0.6Ω	-6.0A	IRF9521	R9521

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain

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Applications

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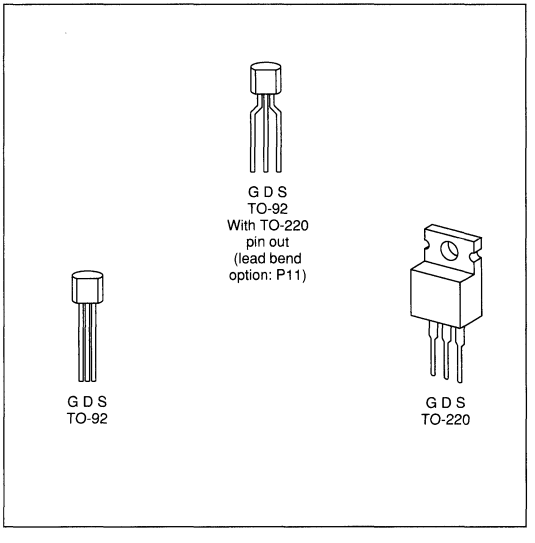
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options



Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
IRF9521	-6.0A	-24.0A	40W	80	3.12	-6.0A	-24.0A
R9521	-0.8A	-7.5A	1W	125	170	-0.8A	-7.5A

*I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

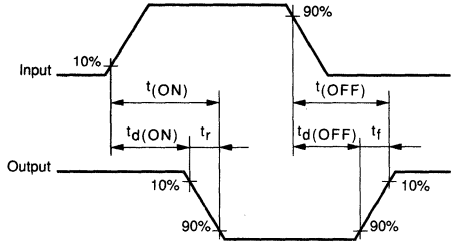
(Notes 1 and 2)

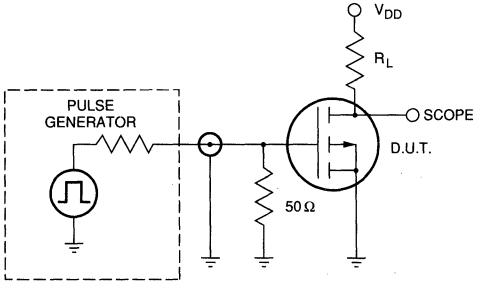
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60			V	V_{GS} = 0, I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	-2.0		-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate Body Leakage			-500	nA	V_{GS} = ± 20V, V_{DS} = Max Rating
I_{DSS}	Zero Gate Voltage Drain Current			-250	μA	V_{GS} = 0, V_{DS} = Max Rating
				-1000		V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	-6.0			A	V_{GS} = -10V V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max Rating
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			0.8	Ω	V_{GS} = -10V, I_D = -3.5A
G_{FS}	Forward Transconductance	0.9			℧	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max I_D = -3.5A
C_{ISS}	Input Capacitance			450	pF	V_{GS} = 0V, V_{DS} = -25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			350		
C_{RSS}	Reverse Transfer Capacitance			100		
$t_{d(ON)}$	Turn-ON Delay Time			50	ns	V_{DD} = 0.5BV_{DSS} I_D = -3.5A R_S = 50Ω
t_r	Rise Time			100		
$t_{d(OFF)}$	Turn-OFF Delay Time			100		
t_f	Fall Time			100		
V_{SD}	Diode Forward Voltage Drop			6.3	V	V_{GS} = 0V, I_S = -6.0A, T_C = 25°C
t_{rr}	Reverse Recovery Time		230		ns	T_j = 150°C, I_F = -6.0A, $dI_{F/dt}$ = 100A/μS

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Objective

P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-220	TO-92
-100V	0.8Ω	-5A	IRF9522	R9522
-60V	0.8Ω	-5A	IRF9523	R9523

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

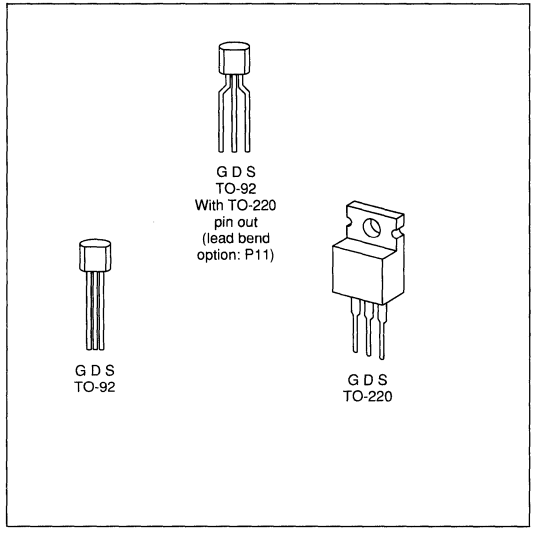
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

9

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options



Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
IRF9522 IRF9523	-5.0A	-20.0A	40W	80	3.12	-5.0A	-20.0A
R9522 R9523	-0.55A	-7.0A	1W	125	170	-0.55A	-7.0A

* I_D (continuous) is limited by max rated T_j.

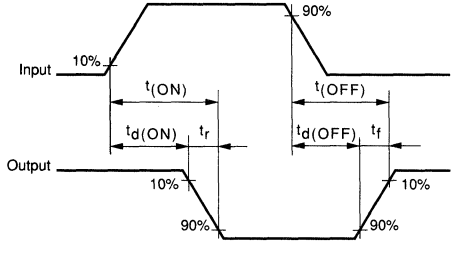
Electrical Characteristics (@ 25°C unless otherwise specified)

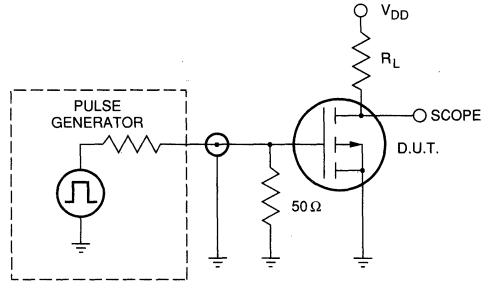
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRF9522 R9522	-100			V	V_{GS} = 0V, I_D = -250µA
		IRF9523 R9523	-60				
$V_{GS(th)}$	Gate Threshold Voltage		-2.0		-4.0	V	V_{DS} = V_{GS}, I_D = -250µA
I_{GSS}	Gate Body Leakage				-500	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-250	µA	V_{GS} = 0, V_{DS} = Max Rating
					-1000		V_{GS} = 0, V_{DS} = 0.8 Max Rating T_C = 125°C
$I_{D(ON)}$	ON-State Drain Current		-5.0			A	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max Rating V_{GS} = -10V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance				0.8	Ω	V_{GS} = -10V, I_D = -3.5A
G_{FS}	Forward Transconductance		0.9			℧	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max I_D = -3.5A
C_{ISS}	Input Capacitance				450	pF	V_{GS} = 0, V_{DS} = -25V f = 1.0 MHz
C_{OSS}	Common Source Output Capacitance				350		
C_{RSS}	Reverse Transfer Capacitance				100		
$t_{d(ON)}$	Turn-ON Delay Time				50	ns	V_{DD} = 0.5BV_{DSS} I_D = -3.5A R_S = 50Ω
t_r	Rise Time				100		
$t_{d(OFF)}$	Turn-OFF Delay Time				100		
t_f	Fall Time				100		
V_{SD}	Diode Forward Voltage Drop				-6.0	V	T_C = 25°C, I_S = -5.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time			230		ns	T_j = 150°C, I_F = -6.0A, $dI_{F/dt}$ = 100A/µS

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package						
			TO-39	TO-52	TO-92	TO-220	Quad P-DIP	Quad C-DIP	DICE
-40V	8Ω	-0.5A	VP0104N2	VP0104N9	VP0104N3	VP0104N5	VP0104N6	VP0104N7	VP0104ND
-60V	8Ω	-0.5A	VP0106N2	VP0106N9	VP0106N3	VP0106N5	VP0106N6	VP0106N7	VP0106ND
-90V	8Ω	-0.5A	VP0109N2	VP0109N9	VP0109N3	VP0109N5	—	—	VP0109ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

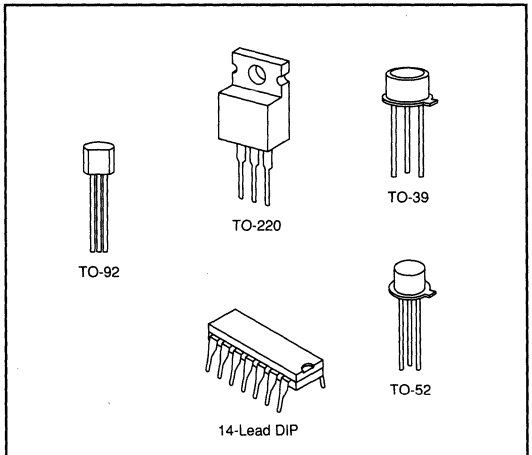
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-39	-0.45A	-1.0A	3.5W	125	35	-0.5A	-1.0A
TO-52	-0.25A	-1.0A	1.0W	170	125	-0.4A	-1.0A
TO-92	-0.25A	-0.8A	1.0W	170	125	-0.4A	-0.8A
TO-220	-1.0A	-1.0A	15.0W	70	8.3	-1.0A	-1.0A
Plastic Dip Ceramic Dip	Refer to Arrays & Special Functions Section.						

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

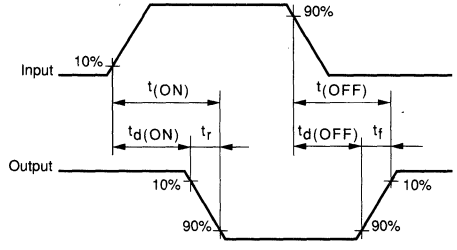
(Notes 1 and 2)

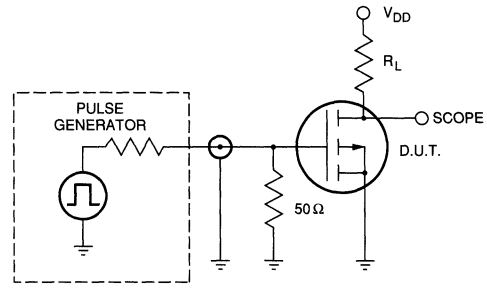
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0109	-90			V	I_D = -1.0mA, V_{GS} = 0
		VP0106	-60				
		VP0104	-40				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-5.8	-6.5	mV/°C	I_D = -1.0mA, V_{GS} = V_{DS}
I_{GSS}	Gate Body Leakage			-1.0	-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-0.15	-0.25		A	V_{GS} = -5V, V_{DS} = -25V
			-0.50	-1.0			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			11	15	Ω	V_{GS} = -5V, I_D = -0.1A
				5	8		V_{GS} = -10V, I_D = -0.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.55	1.0	%/°C	I_D = -0.5A, V_{GS} = -10V
G_{FS}	Forward Transconductance		150	200		m℧	V_{DS} = -25V, I_D = -0.5A
C_{ISS}	Input Capacitance			45	60	pF	V_{GS} = 0, V_{DS} = -25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			22	30		
C_{RSS}	Reverse Transfer Capacitance			3	8		
$t_{d(ON)}$	Turn-ON Delay Time			4	6	ns	V_{DD} = -25V I_D = -1A R_S = 50Ω
t_r	Rise Time			7	10		
$t_{d(OFF)}$	Turn-OFF Delay Time			3	5		
t_f	Fall Time			4	6		
V_{SD}	Diode Forward Voltage Drop			-1.2	-2.0	V	I_{SD} = -2.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			400		ns	I_{SD} = -1A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

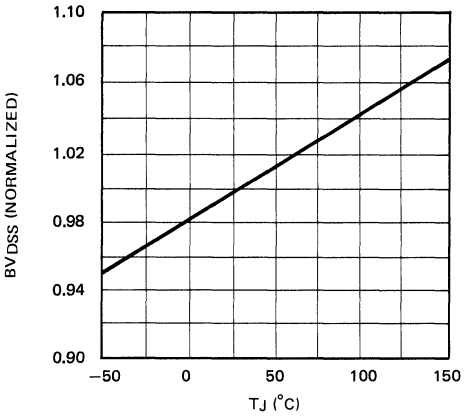
Switching Waveforms and Test Circuit



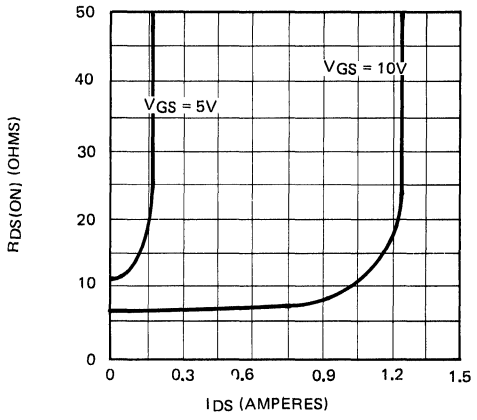


Typical Performance Curves

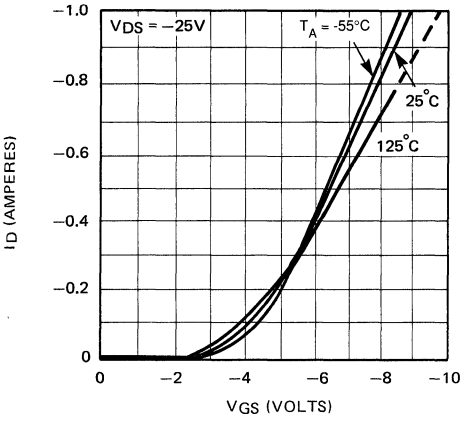
BVDSS Variation with Temperature



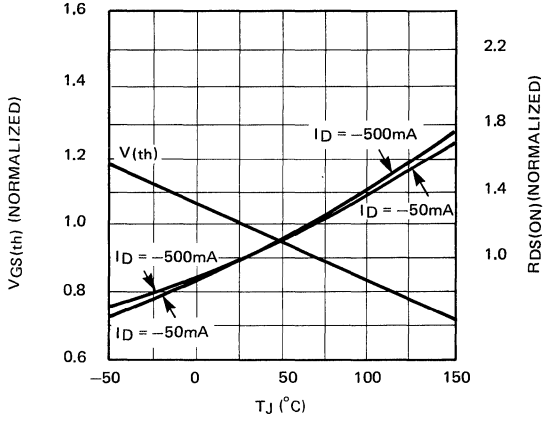
ON-Resistance vs. Drain Current



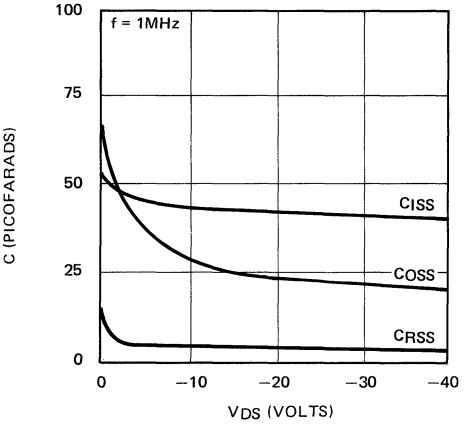
Transfer Characteristics



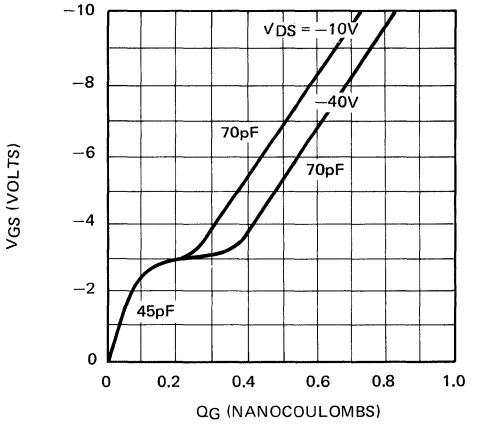
V(th) and RDS Variation with Temperature



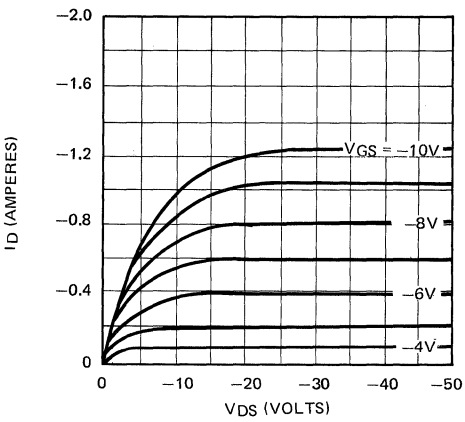
Capacitance Vs. Drain-to-Source Voltage



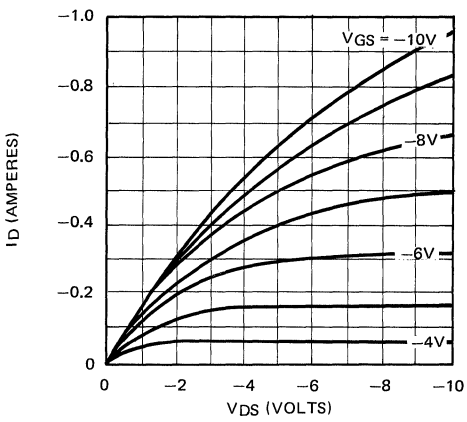
Gate Drive Dynamic Characteristics



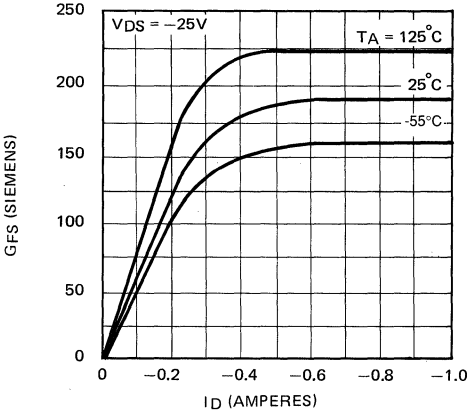
Output Characteristics



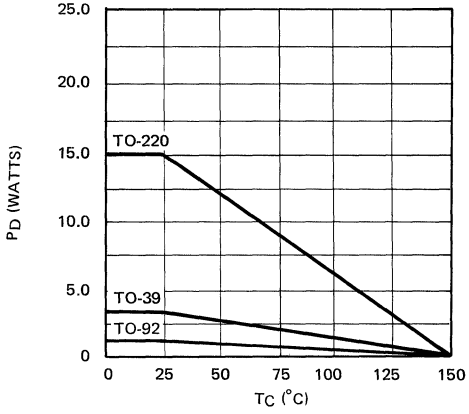
Saturation Characteristics



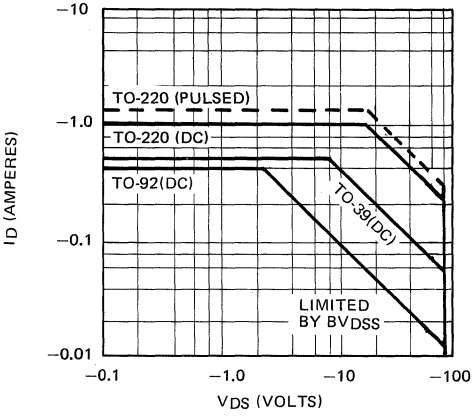
Transconductance Vs. Drain Current



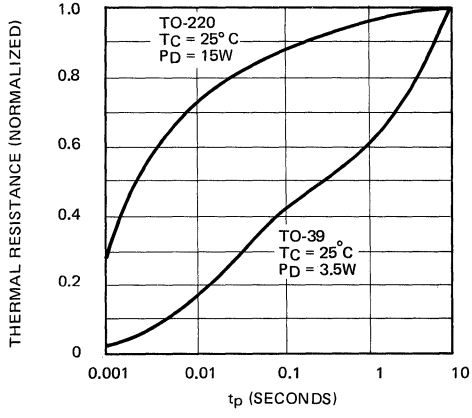
Power Dissipation Vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-39	TO-92	TO-220	DICE
-160V	25Ω	-250mA	VP0116N2	VP0116N3	VP0116N5	VP0116ND
-200V	25Ω	-250mA	VP0120N2	VP0120N3	VP0120N5	VP0120ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

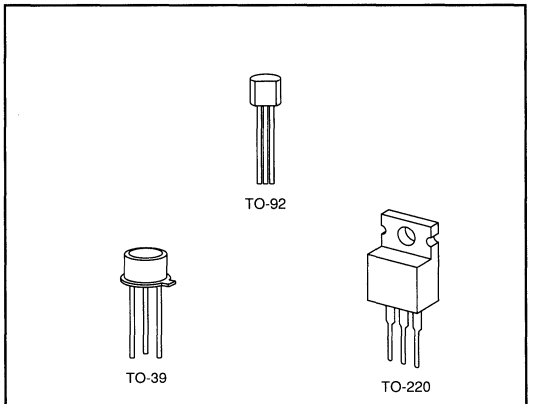
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Note 1)



Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-39	-0.2A	-0.65A	3.5W	125	35	-0.2A	-0.65A
TO-92	-0.1A	-0.35A	1.0W	170	125	-0.1A	-0.35A
TO-220	-0.425A	-1.0A	15.0W	70	8.3	-0.425A	-1.0A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

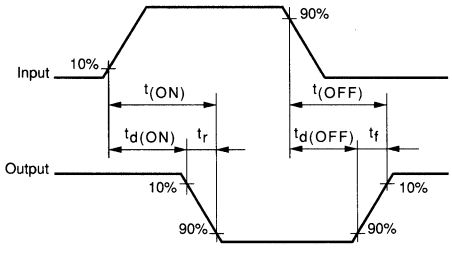
(Notes 1 and 2)

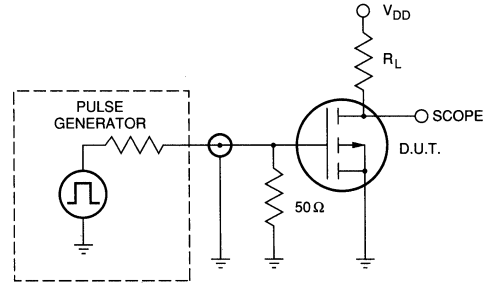
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0120	-200			V	I_D = -1.0mA, V_{GS} = 0
		VP0116	-160				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-6.0		mV/°C	I_D = -1.0mA, V_{GS} = V_{DS}
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-100	-400		mA	V_{GS} = -5V, V_{DS} = -25V
			-350	-700			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			25	40	Ω	V_{GS} = -5V, I_D = -50mA
				15	25		V_{GS} = -10V, I_D = -100mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.6		%/°C	I_D = -100mA, V_{GS} = -10V
G_{FS}	Forward Transconductance		50	70		m℧	V_{DS} = -25V, I_D = -100mA
C_{ISS}	Input Capacitance			50	60	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			20	30		
C_{RSS}	Reverse Transfer Capacitance			5	10		
$t_{d(ON)}$	Turn-ON Delay Time			4	10	ns	V_{DD} = -25V, I_D = -100mA, R_S = 50Ω
t_r	Rise Time			4	10		
$t_{d(OFF)}$	Turn-OFF Delay Time			4	10		
t_f	Fall Time			4	10		
V_{SD}	Diode Forward Voltage Drop			1.0		V	I_{SD} = -0.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			500		ns	I_{SD} = -0.5A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

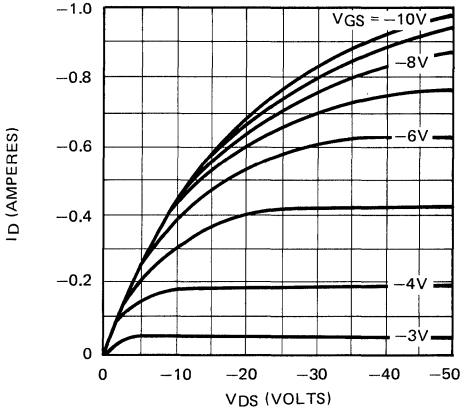
Switching Waveforms and Test Circuit



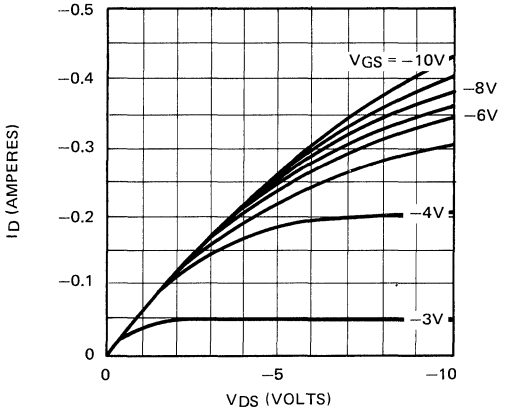


Typical Performance Curves

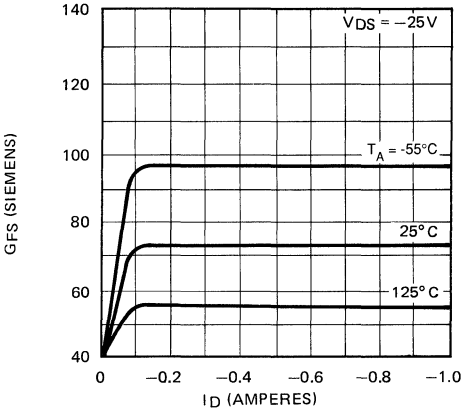
Output Characteristics



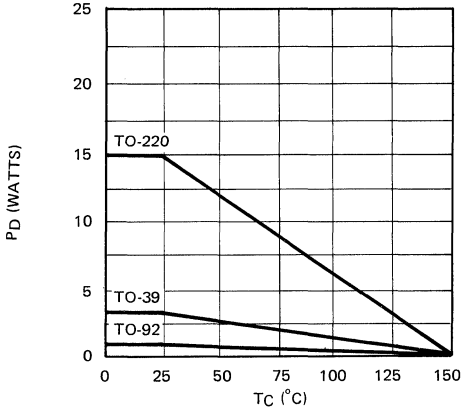
Saturation Characteristics



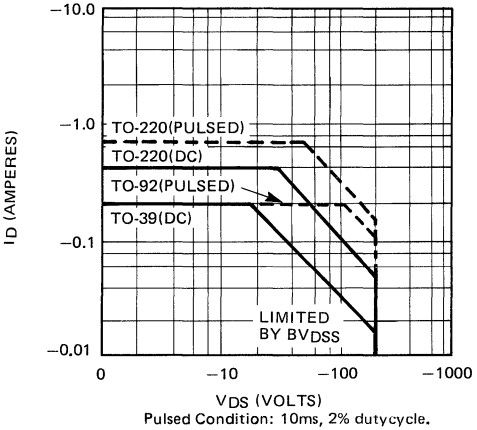
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

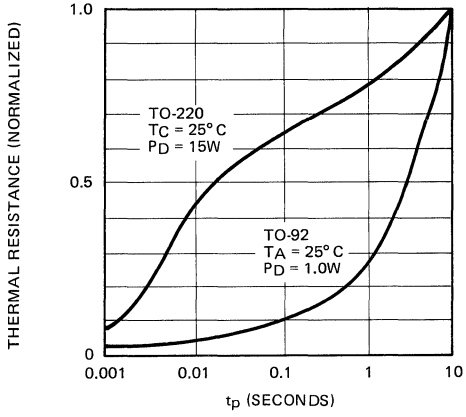


Maximum Rated Safe Operating Area

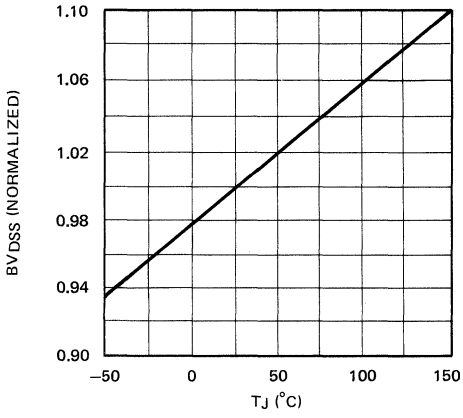


Pulsed Condition: 10ms, 2% dutycycle.

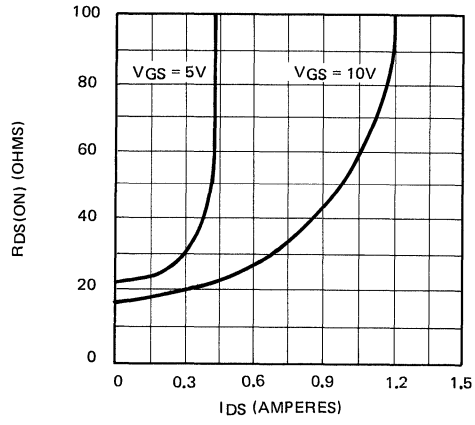
Thermal Response Characteristics



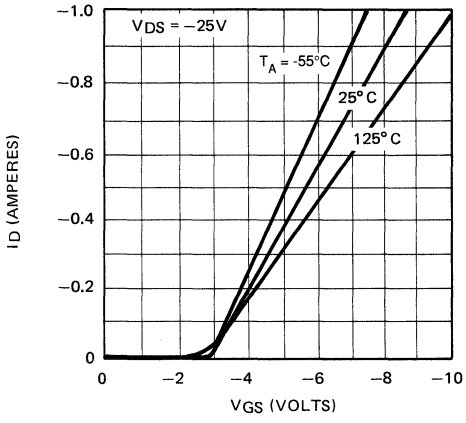
BVDSS Variation with Temperature



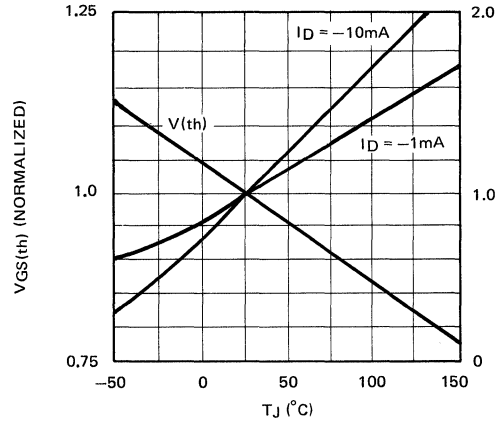
ON - Resistance Vs .Drain Current



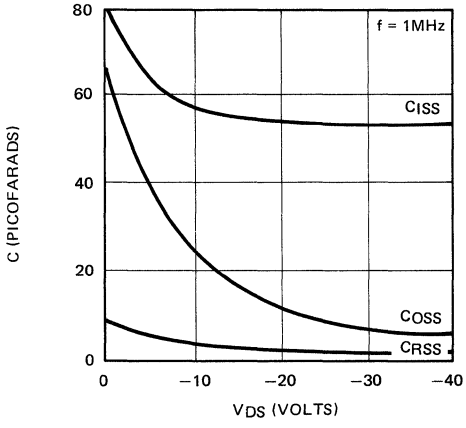
Transfer Characteristics



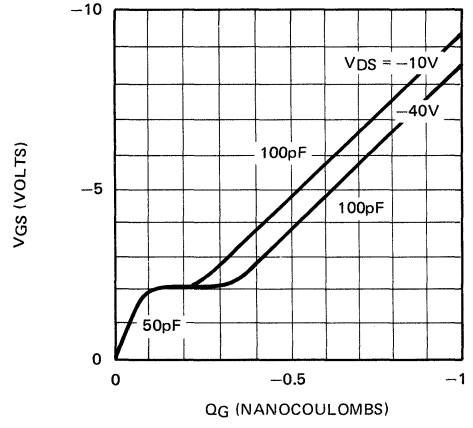
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package				
			TO-39	TO-92	TO-220	Quad P-DIP	Quad C-DIP
-40V	4Ω	1.5A	VP0204N2	—	VP0204N5	VP0204N6	VP0204N7
-60V	4Ω	1.5A	VP0206N2	VP0206N3	VP0206N5	VP0206N6	VP0206N7
-100V	4Ω	1.5A	VP0210N2	VP0210N3	VP0210N5	—	—

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

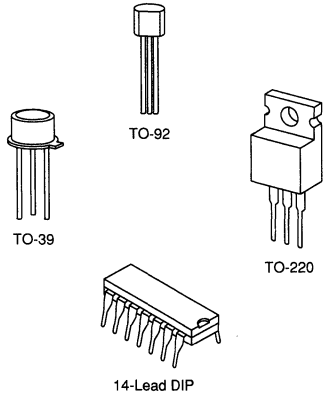
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	-0.8A	-4.0A	6W	125	20	-0.8A	-4.0A
TO-92	-0.4A	-3.5A	1W	170	125	-0.4A	-3.5A
TO-220	-2.0A	-4.5A	27W	70	4.7	-2.0A	-4.5A
Plastic Dip	Refer to Arrays & Special Functions Section.						
Ceramic Dip							

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

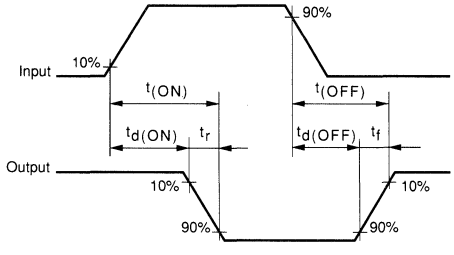
(Notes 1 and 2)

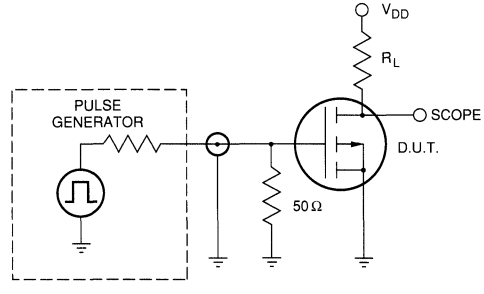
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0210	-100			V	I_D = -2.5mA, V_{GS} = 0
		VP0206	-60				
		VP0204	-40				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-3.5	V	V_{GS} = V_{DS}, I_D = -2.5mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.0	-3.5	mV/°C	I_D = -2.5mA, V_{GS} = V_{DS}
I_{GSS}	Gate Body Leakage			-1.0	-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-25	µA	V_{GS} = 0, V_{DS} = Max Rating
				-0.6	-1.0	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-0.4			A	V_{GS} = -5V, V_{DS} = -25V
			-1.5	-2.5			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.5	8.0	Ω	V_{GS} = -5V, I_D = -0.25A
				3	4.0		V_{GS} = -10V, I_D = 500mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.75	1.2	%/°C	I_D = -1.0A, V_{GS} = -10V
G_{FS}	Forward Transconductance		0.3	0.5		℧	V_{DS} = -25V, I_D = -1.0A
C_{ISS}	Input Capacitance			90	150	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			65	85		
C_{RSS}	Reverse Transfer Capacitance			15	20		
$t_{d(ON)}$	Turn-ON Delay Time			5	10	ns	V_{DD} = -25V, I_D = -1A, R_S = 50Ω
t_r	Rise Time			7	10		
$t_{d(OFF)}$	Turn-OFF Delay Time			10	15		
t_f	Fall Time			6	10		
V_{SD}	Diode Forward Voltage Drop			-1.3	-2.0	V	I_{SD} = -1A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			430		ns	I_{SD} = -1A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

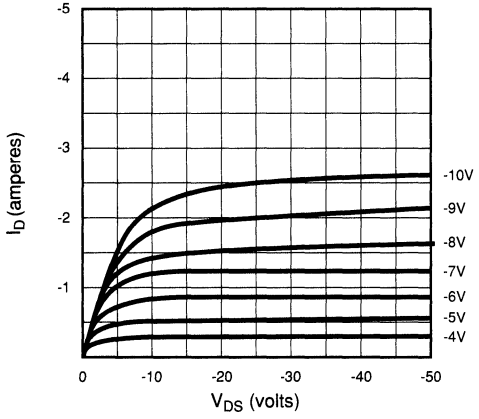
Switching Waveforms and Test Circuit



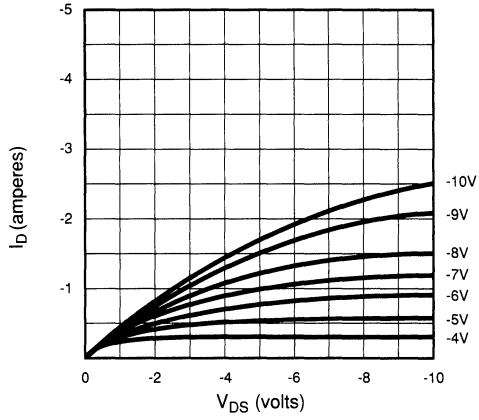


Typical Performance Curves

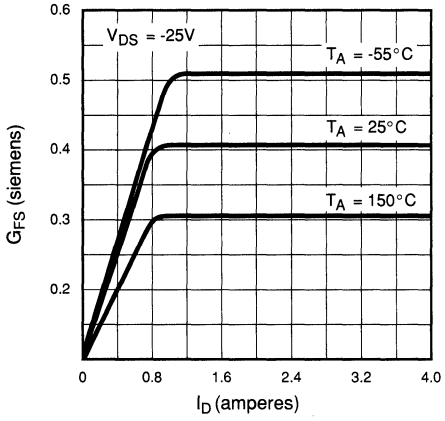
Output Characteristics



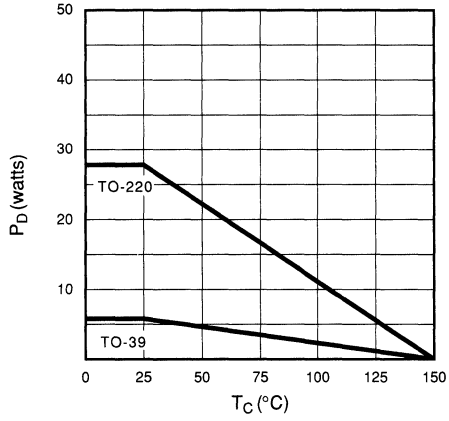
Saturation Characteristics



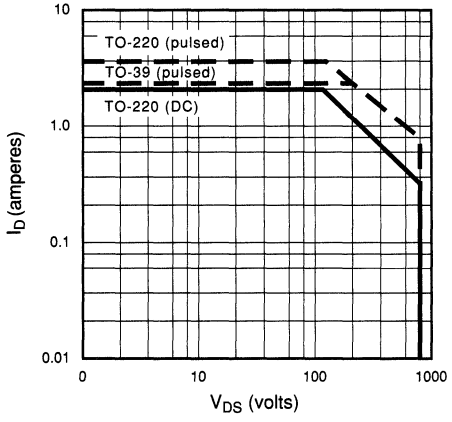
Transconductance vs. Drain Current



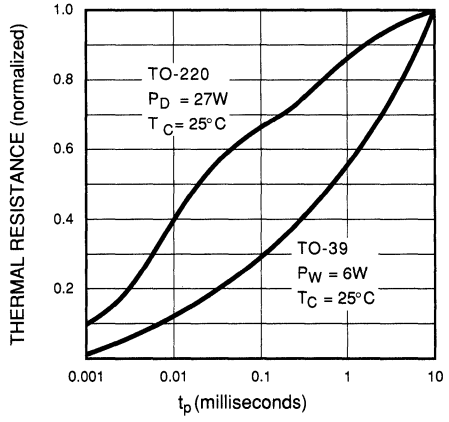
Power Dissipation vs. Case Temperature



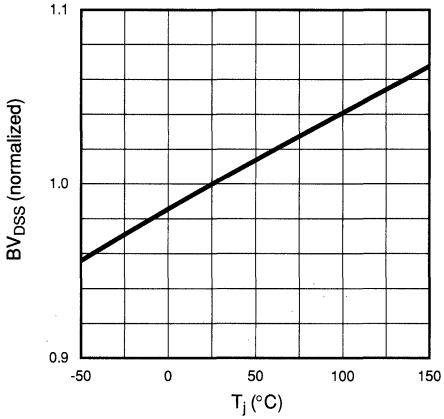
Maximum Rated Safe Operating Area



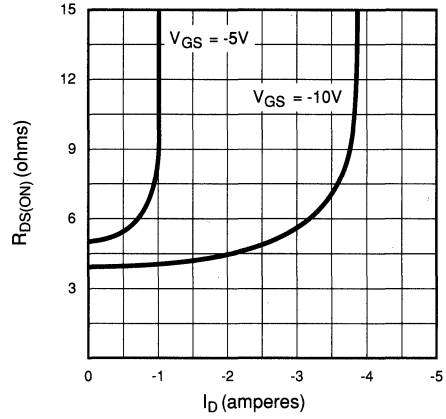
Thermal Response Characteristics



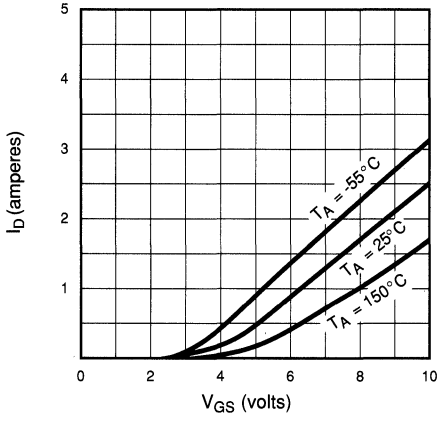
BV$_{DSS}$ Variation with Temperature



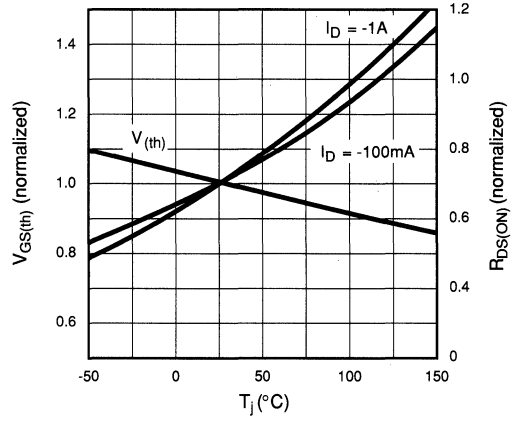
On-Resistance vs. Drain Current



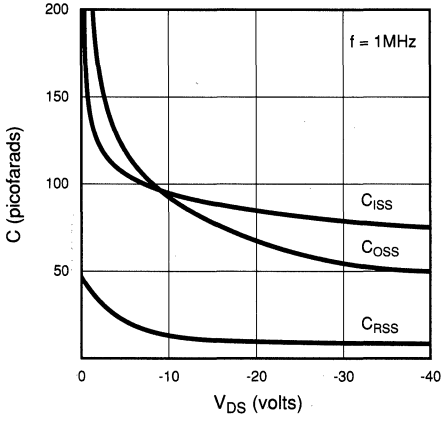
Transfer Characteristics



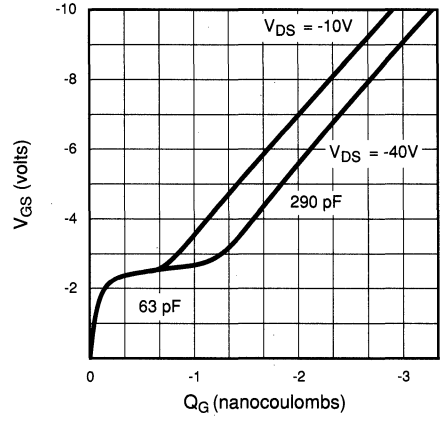
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	TO-220
-160V	16Ω	0.75A	VP0216N2	VP0216N3	VP0216N5
-200V	16Ω	0.75A	VP0220N2	VP0220N3	VP0220N5

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

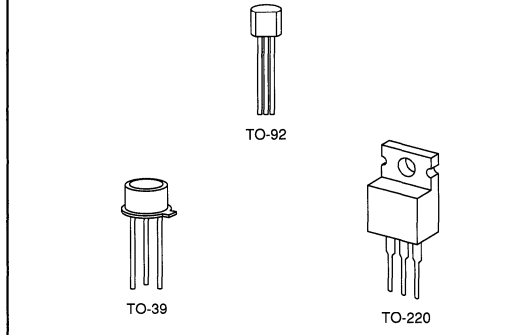
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Note 1)



Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	-0.35A	-1.0A	4W	32	125	-0.35A	-1.0A
TO-92	-0.2A	-1.0A	1W	125	170	-0.2A	-1.0A
TO-220	-0.8A	-2.5A	27W	4.7	70	-0.8A	-2.5A

* I_D (continuous) is limited by max rated T_j

Electrical Characteristics (@ 25°C unless otherwise specified)

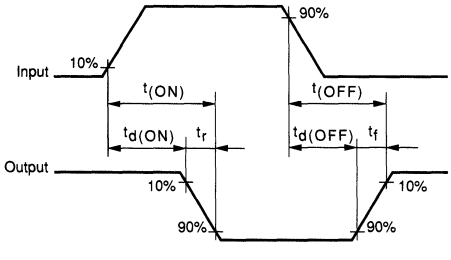
(Notes 1 and 2)

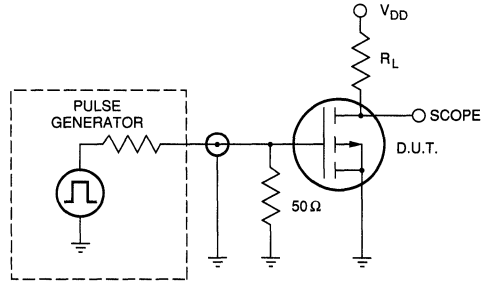
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0220	-200			V	V_{GS} = 0, I_D = -2.5mA
		VP0216	-160				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-3.5	V	V_{GS} = V_{DS}, I_D = -2.5mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.5	-6.0	mV/°C	V_{GS} = V_{DS}, I_D = -2.5mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-25	µA	V_{GS} = 0, V_{DS} = Max Rating
					-2	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-0.25	-0.4		A	V_{GS} = -5V, V_{DS} = -25V
			-0.75	-0.85			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			9	16	Ω	V_{GS} = -5V, I_D = -0.1A
				7	16		V_{GS} = -10V, I_D = -0.25A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.5	1.2	%/°C	V_{GS} = -10V, I_D = -0.25A
G_{FS}	Forward Transconductance		0.1	0.2		℧	V_{DS} = -25V, I_D = -0.25A
C_{ISS}	Input Capacitance			85	150	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			60	85		
C_{RSS}	Reverse Transfer Capacitance			10	35		
$t_{d(ON)}$	Turn-ON Delay Time			8	10	ns	V_{DD} = -25V, I_D = -1.0A, R_S = 50Ω
t_r	Rise Time			10	15		
$t_{d(OFF)}$	Turn-OFF Delay Time			15	20		
t_f	Fall Time			10	15		
V_{SD}	Diode Forward Voltage Drop			-1.2	-1.8	V	V_{GS} = 0, I_{SD} = -0.5A
t_{rr}	Reverse Recovery Time			400		ns	V_{GS} = 0, I_{SD} = -0.5A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

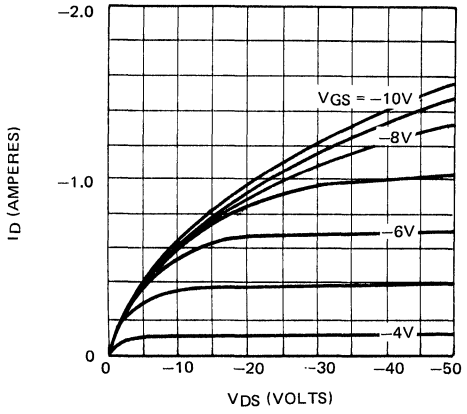
Switching Waveforms and Test Circuit



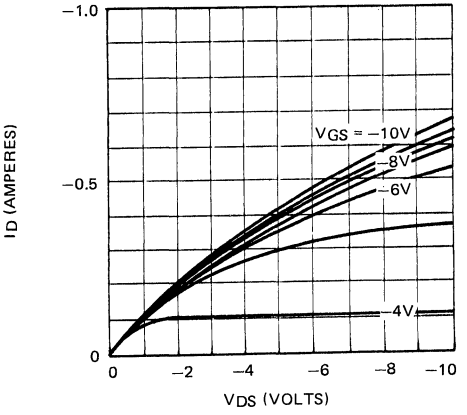


Typical Performance Curves

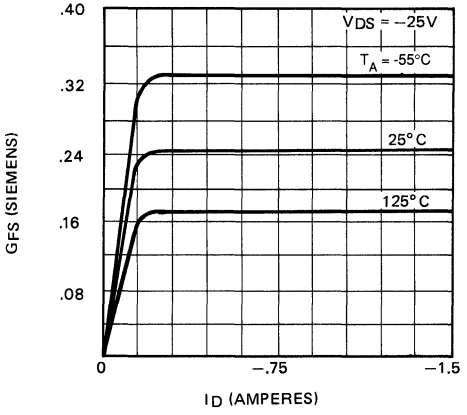
Output Characteristics



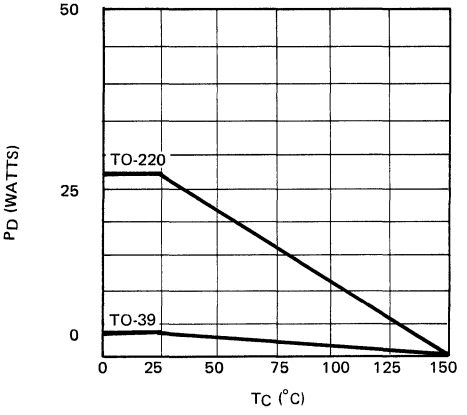
Saturation Characteristics



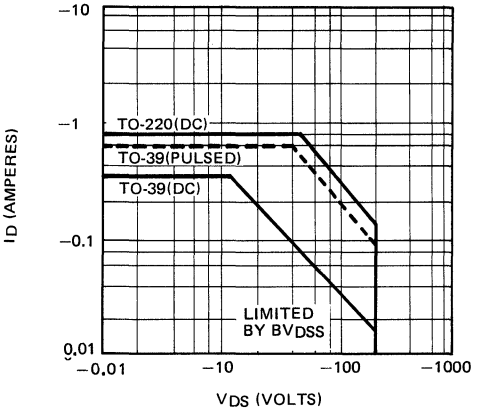
Transconductance Vs. Drain Current



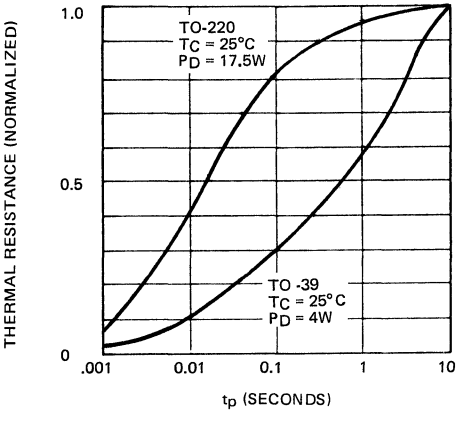
Power Dissipation Vs. Case Temperature



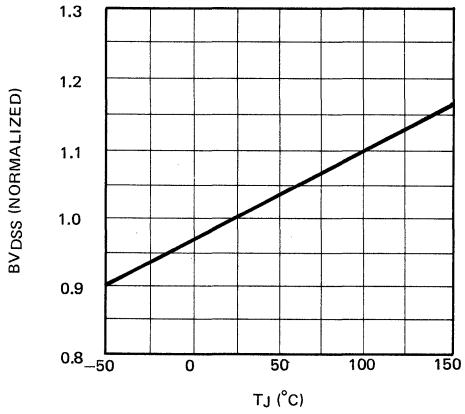
Maximum Rated Safe Operating Area



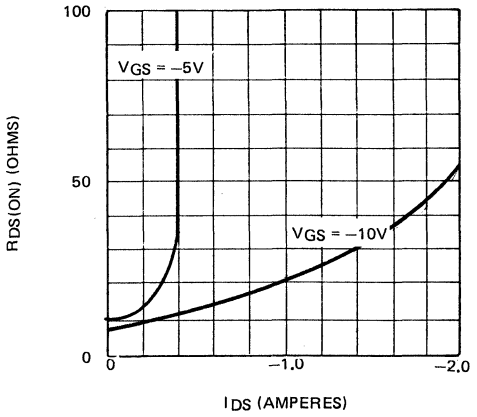
Thermal Response Characteristics



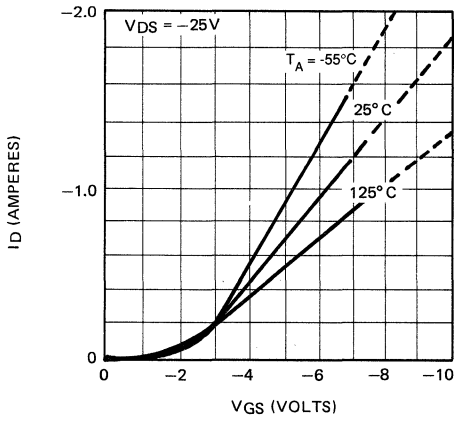
BVDSS Variation with Temperature



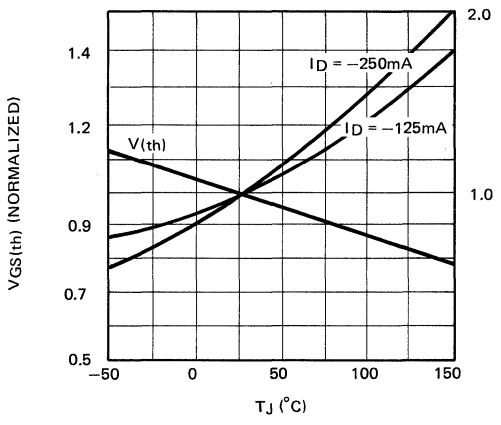
ON-Resistance Vs. Drain Current



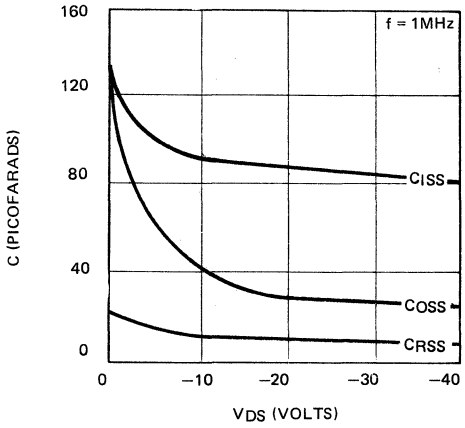
Transfer Characteristics



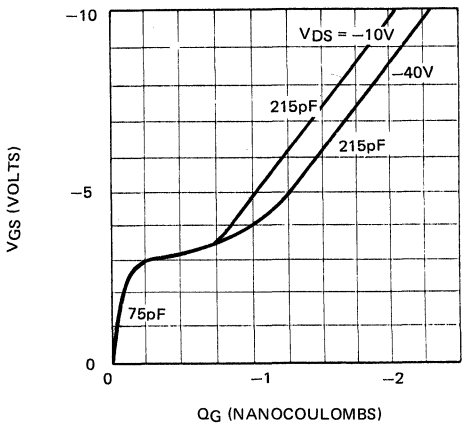
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	DICE
-350V	6Ω	-1.5A	VP0335N1	VP0335N2	VP0335N5	VP0335ND
-400V	6Ω	-1.5A	VP0340N1	VP0340N2	VP0340N5	VP0340ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

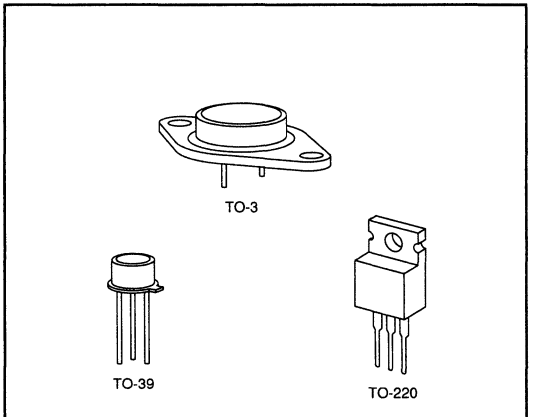
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-3	-2.7A	-5.0A	100W	1.25	30	-2.7A	-5.0A
TO-39	-0.7A	-5.0A	6W	20.8	125	-0.7A	-5.0A
TO-220	-1.6A	-5.0A	50W	2.5	40	-1.6A	-5.0A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

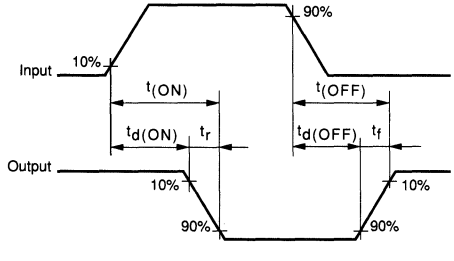
(Notes 1 and 2)

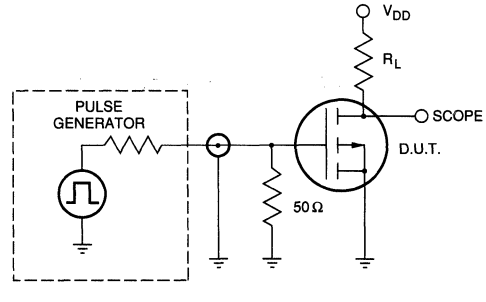
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0340	-400			V	V_{GS} = 0, I_D = -10mA
		VP0335	-350				
$V_{GS(th)}$	Gate Threshold Voltage		-2.5		-4.5	V	V_{GS} = V_{DS}, I_D = -10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.8	-6.0	mV/°C	V_{GS} = V_{DS}, I_D = -10mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-200	µA	V_{GS} = 0, V_{DS} = Max Rating
					-2	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			-1.5		A	V_{GS} = -5V, V_{DS} = -25V
			-1.5	-3.5			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5		Ω	V_{GS} = -5V, I_D = -0.25A
				4	6		V_{GS} = -10V, I_D = -0.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.7	1.2	%/°C	V_{GS} = -10V, I_D = -0.5A
G_{FS}	Forward Transconductance		0.5	1		℧	V_{DS} = -25V, I_D = -0.5A
C_{ISS}	Input Capacitance			550	700	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			90	120		
C_{RSS}	Reverse Transfer Capacitance			20	50		
$t_{d(ON)}$	Turn-ON Delay Time			25	40	ns	V_{DD} = -25V, I_D = -1A, R_S = 50Ω
t_r	Rise Time			25	40		
$t_{d(OFF)}$	Turn-OFF Delay Time			65	110		
t_f	Fall Time			20	40		
V_{SD}	Diode Forward Voltage Drop			-1	-1.3	V	V_{GS} = 0, I_{SD} = -0.5A
t_{rr}	Reverse Recovery Time			500		ns	V_{GS} = 0, I_{SD} = -0.5A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

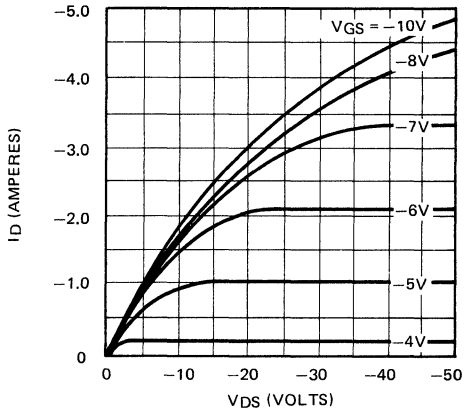
Switching Waveforms and Test Circuit



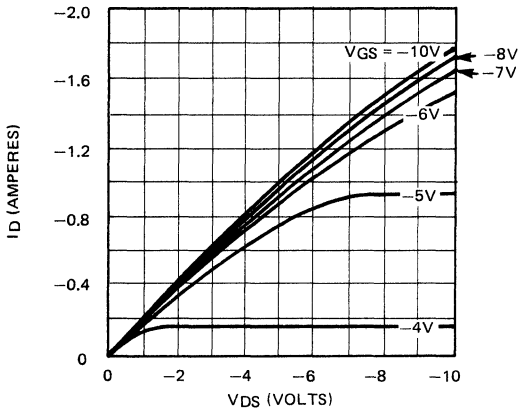


Typical Performance Curves

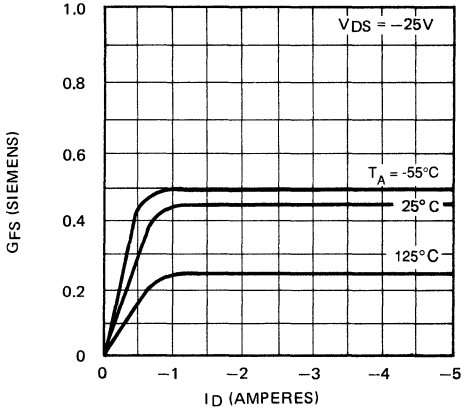
Output Characteristics



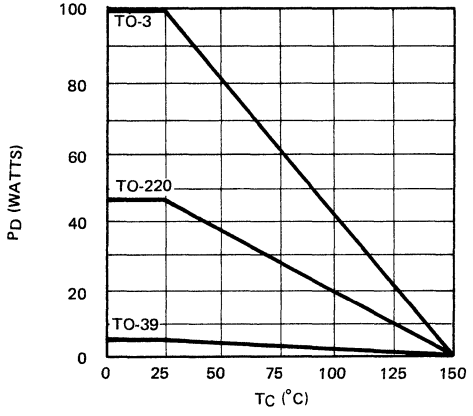
Saturation Characteristics



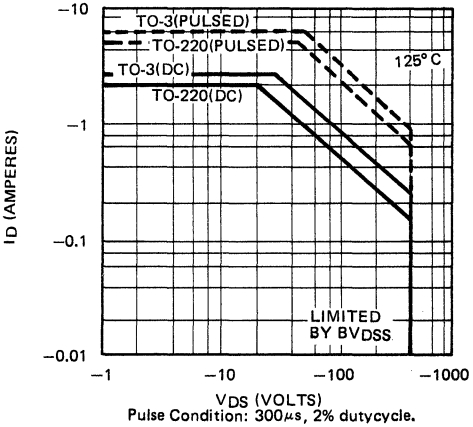
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

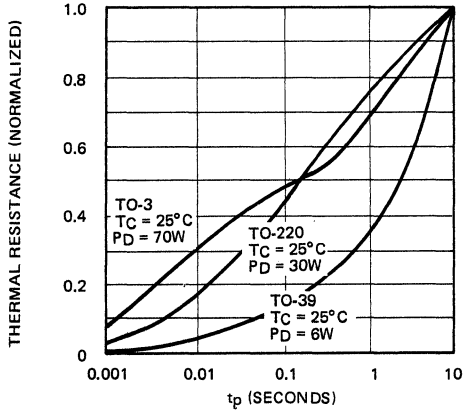


Maximum Rated Safe Operating Area

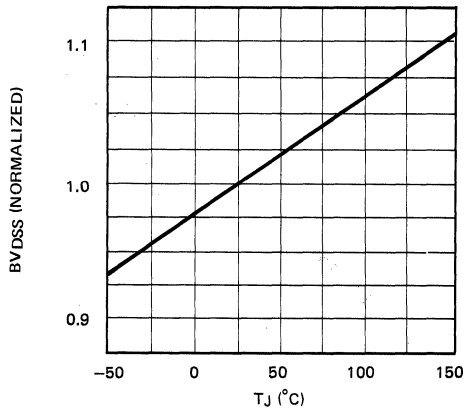


Pulse Condition: 300μs, 2% dutycycle.

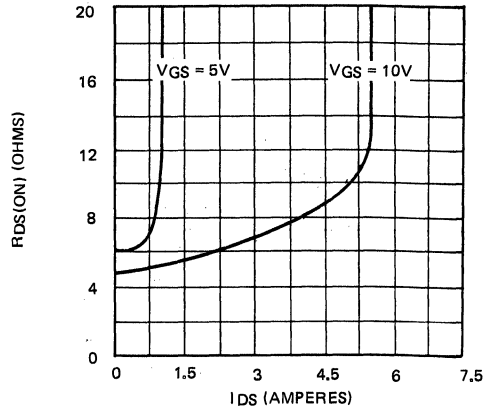
Thermal Response Characteristics



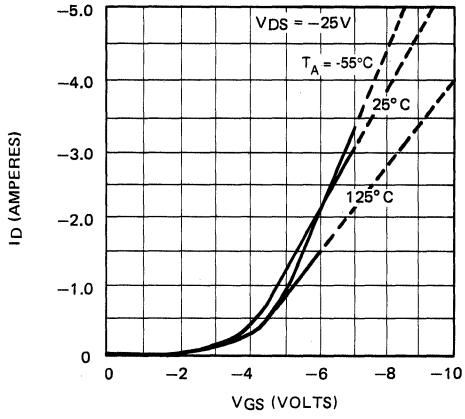
BVDSS Variation with Temperature



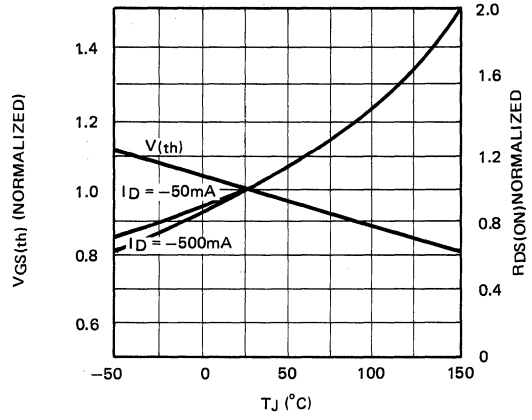
ON - Resistance Vs. Drain Current



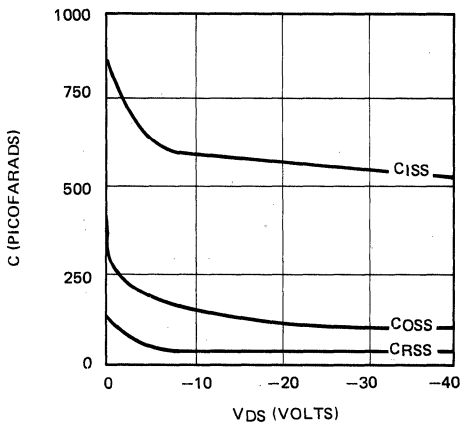
Transfer Characteristics



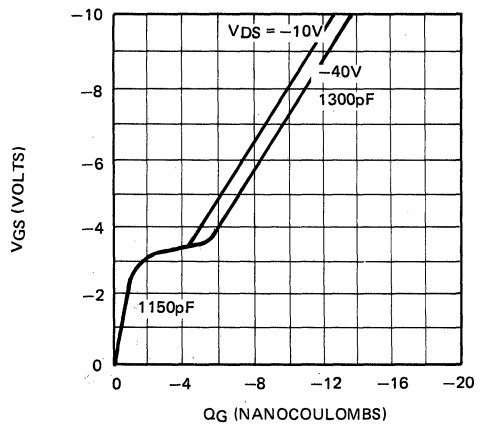
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	DICE
-450V	7.5Ω	-1A	VP0345N1	VP0345N2	VP0345N5	VP0345ND
-500V	7.5Ω	-1A	VP0350N1	VP0350N2	VP0350N5	VP0350ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

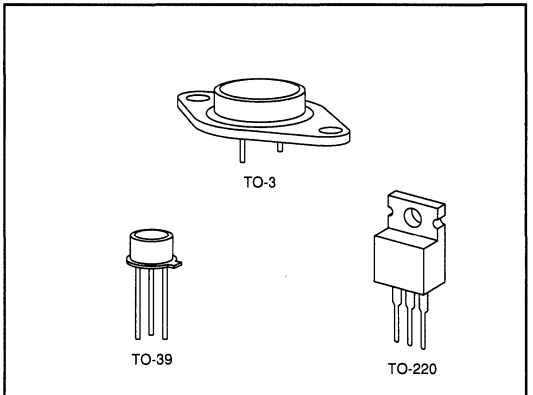
9

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-3	-1.5A	-3.0A	100W	1.25	30	-1.5A	-3.0A
TO-39	-0.4A	-3.0A	6W	20.8	125	-0.4A	-3.0A
TO-220	-1.0A	-3.0A	50W	2.5	40	-1.0A	-3.0A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

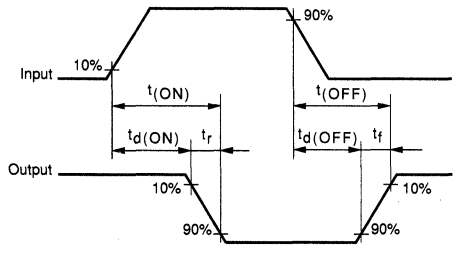
(Notes 1 and 2)

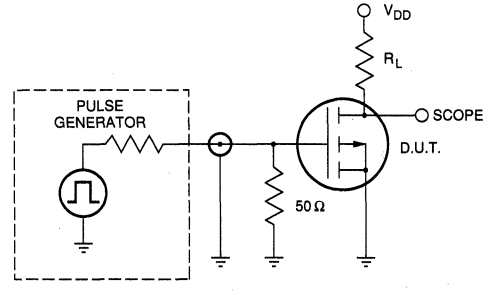
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0350	-500			V	V_{GS}= 0, I_D =-10mA
		VP0345	-450				
$V_{GS(th)}$	Gate Threshold Voltage		-2.5		-4.5	V	V_{GS} = V_{DS}, I_D = -10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.8	-6.0	mV/°C	V_{GS} = V_{DS}, I_D = -10mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-200	µA	V_{GS} = 0, V_{DS} = Max Rating
					-2	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			-0.75		A	V_{GS} = -5V, V_{DS} = -25V
			-1.0	-2.5			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			6.0		Ω	V_{GS} = -5V, I_D = -0.25A
				5.5	7.5		V_{GS} = -10V, I_D = -0.25A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.7	1.2	%/°C	V_{GS} = -10V, I_D = -0.25A
G_{FS}	Forward Transconductance		0.25	0.75		℧	V_{DS} = -25V, I_D = -0.5A
C_{ISS}	Input Capacitance			550	700	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			90	120		
C_{RSS}	Reverse Transfer Capacitance			20	50		
$t_{d(ON)}$	Turn-ON Delay Time			11	30	ns	V_{DD} = -25V, I_D = -0.5A, R_S = 50Ω
t_r	Rise Time			11	30		
$t_{d(OFF)}$	Turn-OFF Delay Time			70	100		
t_f	Fall Time			22	30		
V_{SD}	Diode Forward Voltage Drop			-1.0	-1.3	V	V_{GS} = 0, I_{SD} = -0.25A
t_{rr}	Reverse Recovery Time			550		ns	V_{GS} = 0, I_{SD} = -0.25A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

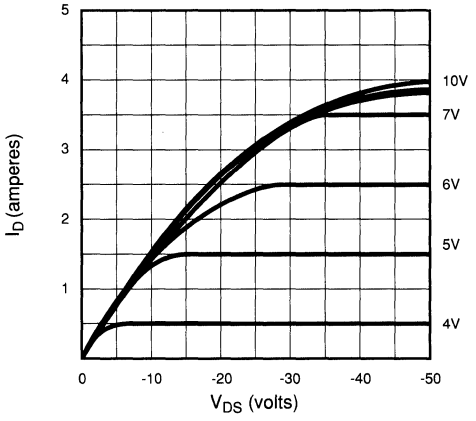
Switching Waveforms and Test Circuit



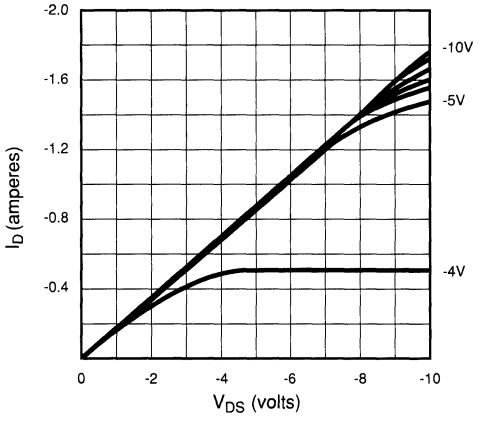


Typical Performance Curves

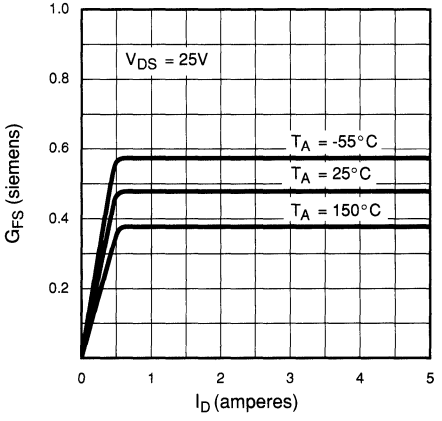
Output Characteristics



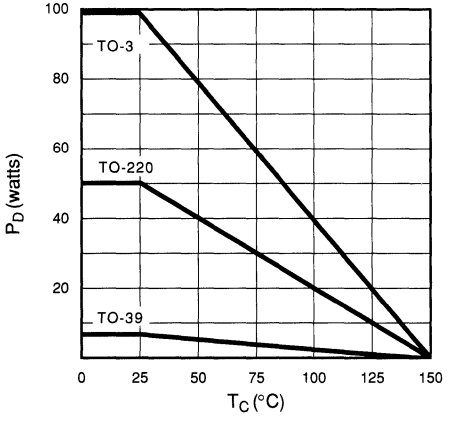
Saturation Characteristics



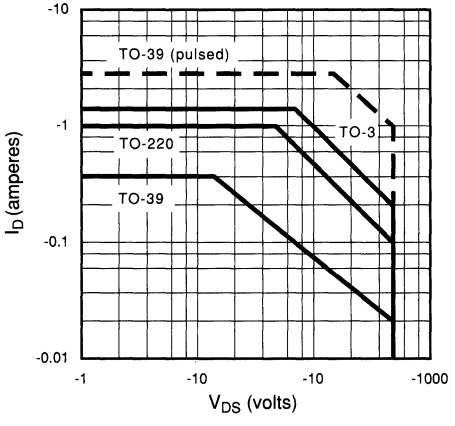
Transconductance vs. Drain Current



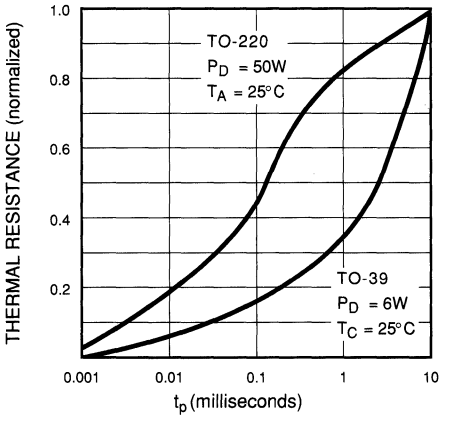
Power Dissipation vs. Case Temperature



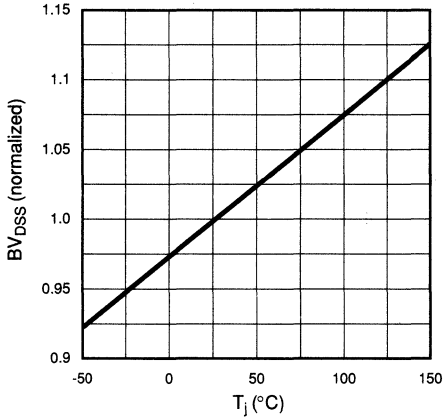
Maximum Rated Safe Operating Area



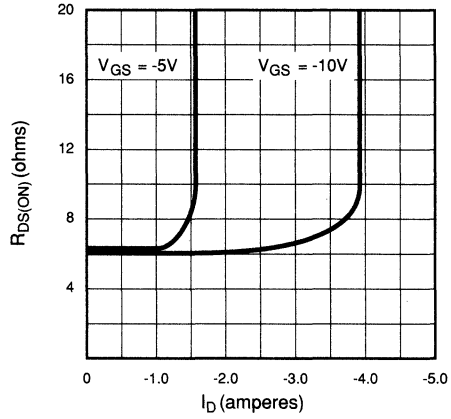
Thermal Response Characteristics



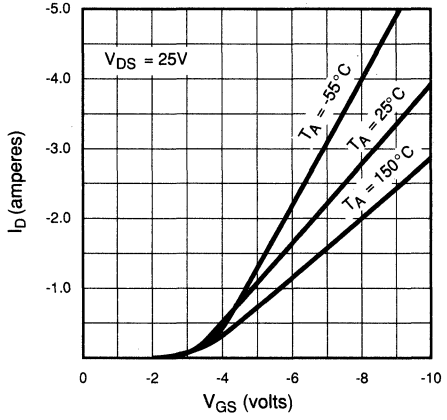
BV_{DSS} Variation with Temperature



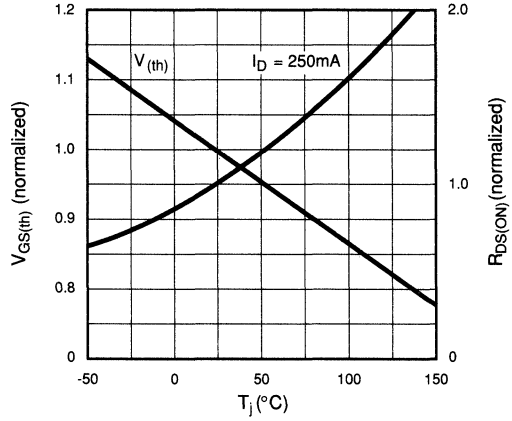
On-Resistance vs. Drain Current



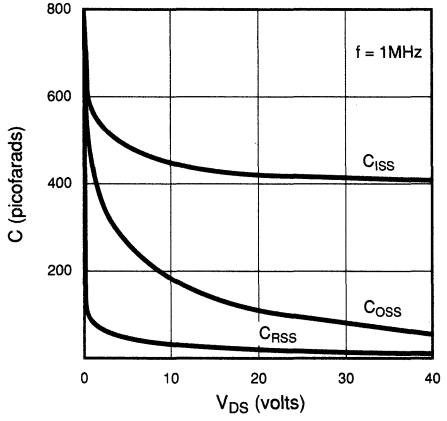
Transfer Characteristics



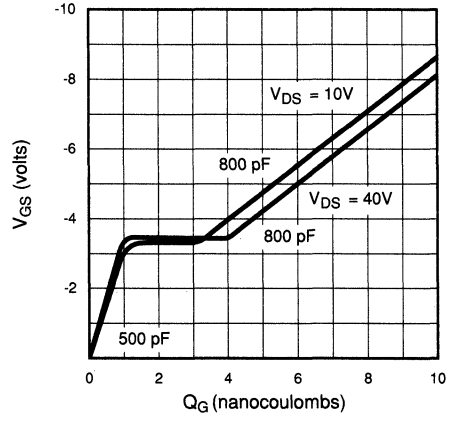
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
-30V	2.5Ω	-1.5A	VP0300B	VP0300L

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

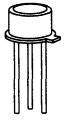
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

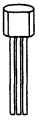
Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-39



TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation	θ_{ja} °C/W	θ_{jc} °C/W
TO-39	1.25A	3.0A	6.25W	170	20
TO-92	0.32A	0.87A	0.4W	41	312.5

* I_D (continuous) is limited by max rated T_j.

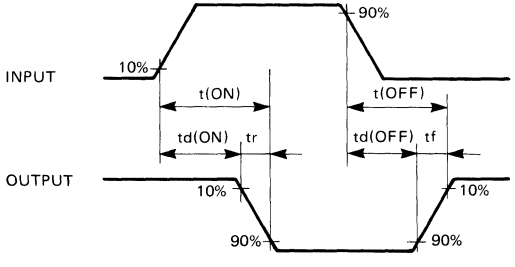
Electrical Characteristics (@ 25°C unless otherwise specified)

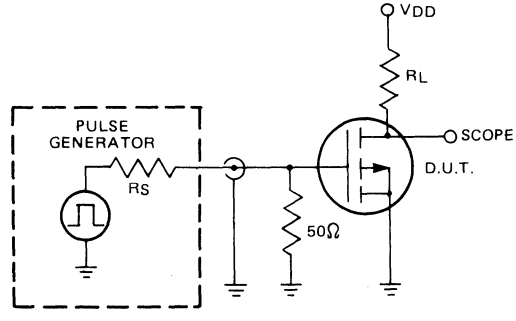
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	−30			V	I_D = 10μA, V_{GS} = 0
$V_{GS(th)}$	Gate Threshold Voltage	−2	−3.4	−4.5	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage			100	nA	V_{GS} = ±30V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			−10	μA	V_{GS} = 0V, V_{DS} = −25V
				−500		V_{GS} = 0V, V_{DS} = −25V, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	−1.5	−1.7		A	V_{GS} = −12V, V_{DS} ≥ 2 $V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			2.5	Ω	V_{GS} = −12V, I_D = −1A
G_{FS}	Forward Transconductance	200			m℧	V_{DS} ≥ 2 $V_{DS(ON)}$, I_D = 0.5A
C_{ISS}	Input Capacitance			150	pF	V_{GS} = 0, V_{DS} = −15V, f = 1MHz
C_{OSS}	Common Source Output Capacitance			100		
C_{RSS}	Reverse Transfer Capacitance			60		
$t_{(ON)}$	Turn-ON Time			30	ns	V_{DD} = −25V, I_D = −1A, R_S = 50Ω
$t_{(OFF)}$	Turn-OFF Time			30		
V_{SD}	Diode Forward Voltage Drop		1.2		V	I_{SD} = −1.5A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	DICE
-350V	75Ω	-200mA	VP0535N2	VP0535N3	VP0535ND
-400V	75Ω	-200mA	VP0540N2	VP0540N3	VP0540ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

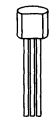
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

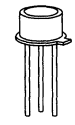
Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Notes 1 and 2)



TO-92



TO-39

Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO - 39	−0.2A	−0.5A	3.5W	35	125	−0.2A	−0.5A
TO - 92	−0.1A	−0.5A	1.0W	125	170	−0.1A	−0.5A

* I_D (continuous) is limited by max rated T_j.

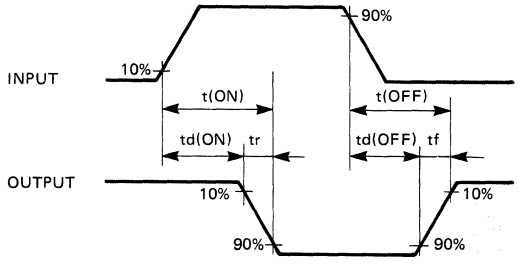
Electrical Characteristics (@ 25°C unless otherwise specified)

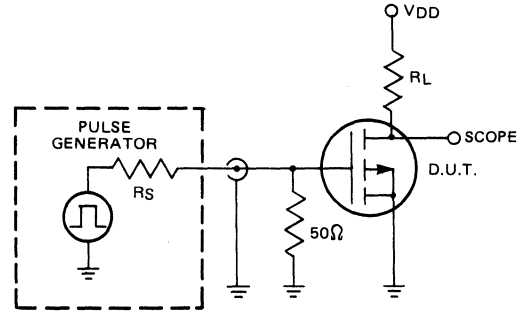
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BVDSS	Drain-to-Source Breakdown Voltage	VP0540	−400			V	VGS = 0, ID = −1mA
		VP0535	−350				
VGS(th)	Gate Threshold Voltage		−2.5		−4.5	V	VGS = VDS, ID = −1mA
ΔVGS(th)	Change in VGS(th) with Temperature			−3.5	−6.0	mV/°C	VGS = VDS, ID = −1mA
IGSS	Gate Body Leakage				−100	nA	VGS = ±20V, VDS = 0
IDSS	Zero Gate Voltage Drain Current				−10	μA	VGS = 0, VDS = Max Rating
					−500		VGS = 0, VDS = 0.8 Max Rating, TA = 125°C
ID(ON)	ON-State Drain Current			−80		mA	VGS = −5V, VDS = −25V
			200	−250			VGS = −10V, VDS = −25V
RDS(ON)	Static Drain-to-Source ON-State Resistance			60		Ω	VGS = −5V, ID = −10mA
				45	75		VGS = −10V, ID = −50mA
ΔRDS(ON)	Change in RDS(ON) with Temperature			0.8	1.5	%/°C	VGS = −10V, ID = −50mA
GFS	Forward Transconductance		50	70		m℧	VDS = −25V, ID = −50mA
CISS	Input Capacitance			40	60	pF	VGS = 0, VDS = −25V, f = 1 MHz
COSS	Common Source Output Capacitance			11	20		
CRSS	Reverse Transfer Capacitance			3	5		
td(ON)	Turn-ON Delay Time				10	ns	VDD = −25V, ID = −50mA, RS = 50Ω
tr	Rise Time				15		
td(OFF)	Turn-OFF Delay Time				15		
tf	Fall Time				10		
VSD	Diode Forward Voltage Drop			−0.8	−1.5	V	VGS = 0, ISD = −0.1A
trr	Reverse Recovery Time			200		ns	VGS = 0, ISD = −0.1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

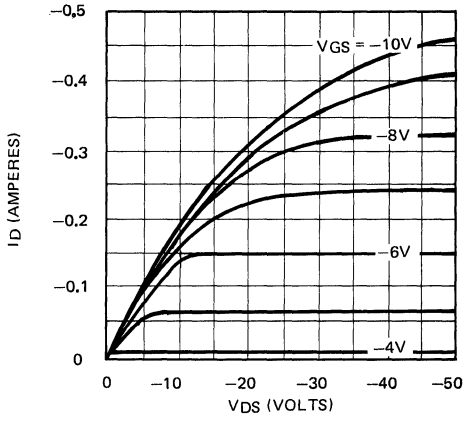
Switching Waveforms and Test Circuit



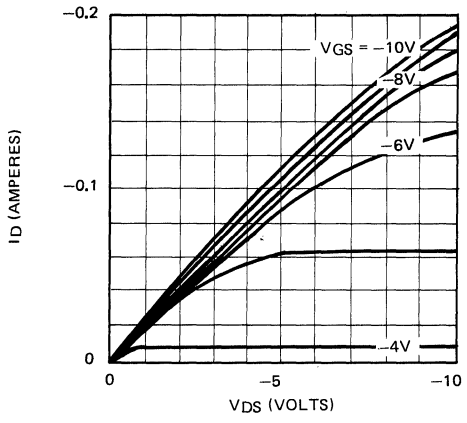


Typical Performance Curves

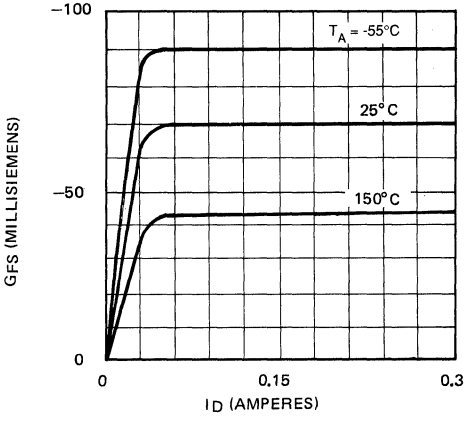
Output Characteristics



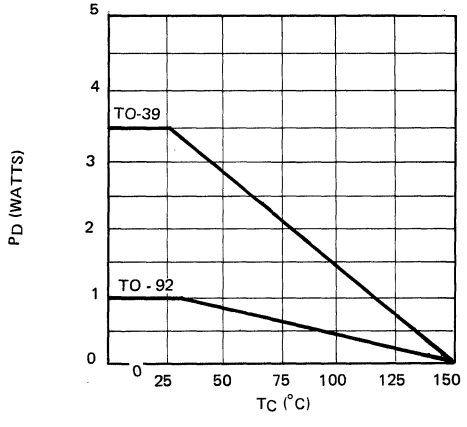
Saturation Characteristics



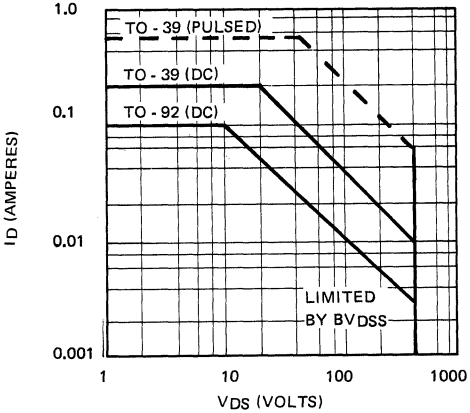
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

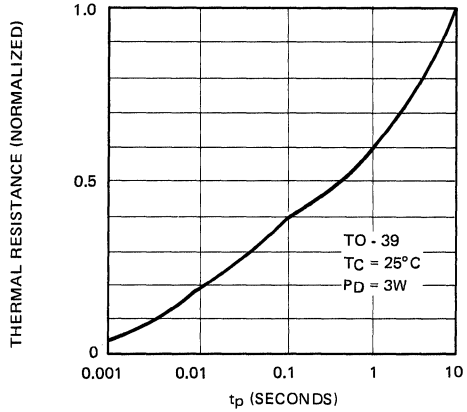


Maximum Rated Safe Operating Area

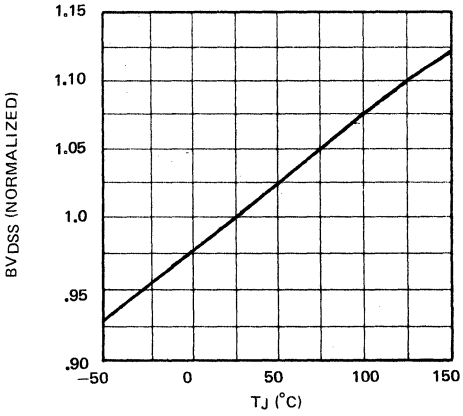


Pulsed Condition: 300μs, 2% Dutycycle

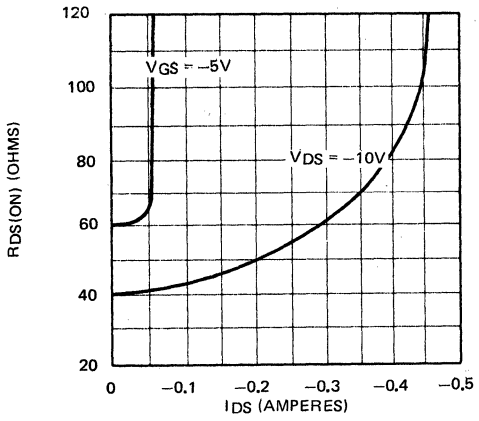
Thermal Response Characteristics



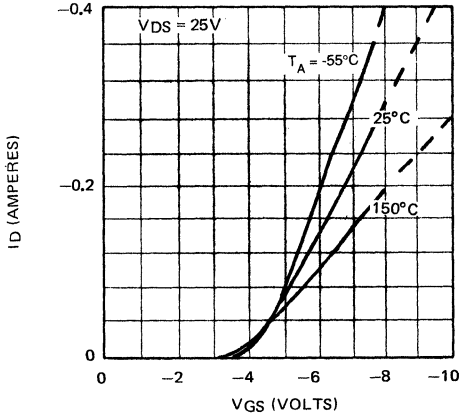
BVDSS Variation with Temperature



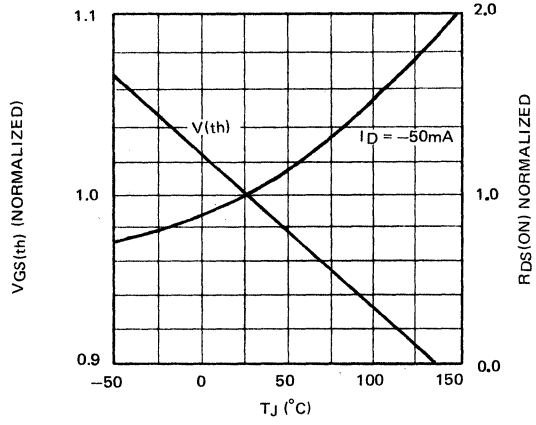
ON - Resistance Vs . Drain Current



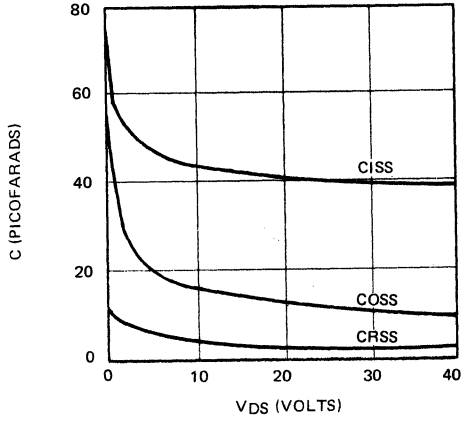
Transfer Characteristics



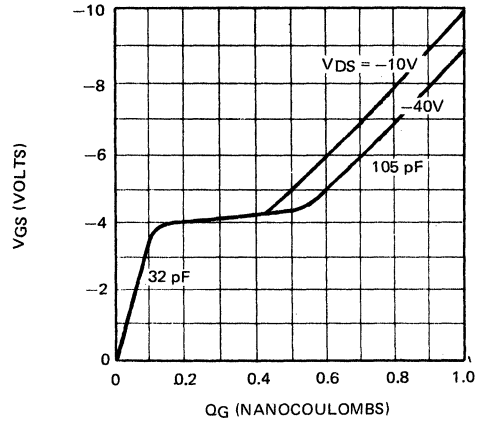
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	DICE
-450V	125Ω	100mA	VP0545N2	VP0545N3	VP0545ND
-500V	125Ω	100mA	VP0550N2	VP0550N3	VP0550ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

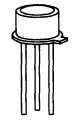
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Notes 1 and 2)



TO-39

TO-92

Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	-125mA	-0.25A	3.5W	35	125	-125mA	-0.25A
TO-92	-70mA	-0.25A	1W	125	170	-70mA	-0.25A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

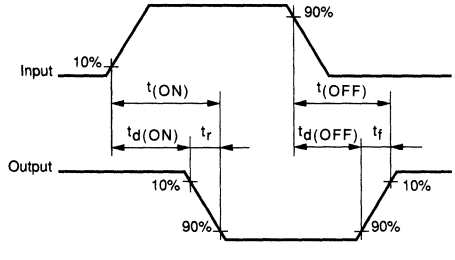
(Notes 1 and 2)

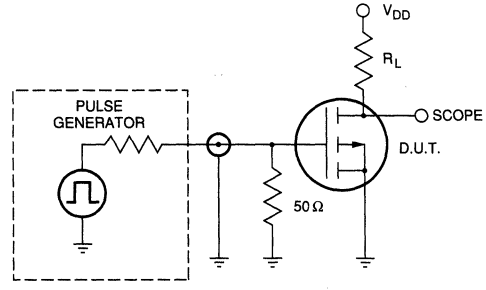
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0550	-500			V	V_{GS} = 0, I_D = -1mA
		VP0545	-450				
$V_{GS(th)}$	Gate Threshold Voltage		-2.5		-4.5	V	V_{GS} = V_{DS}, I_D = -1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.5	-6	mV/°C	V_{GS} = V_{DS}, I_D = -1mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-1000		V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			-50		mA	V_{GS} = -5V, V_{DS} = -25V
			-100	-150			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			85		Ω	V_{GS} = -5V, I_D = -5mA
				75	125		V_{GS} = -10V, I_D = -10mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.85		%/°C	V_{GS} = -10V, I_D = -10mA
G_{FS}	Forward Transconductance		25	40		m℧	V_{DS} = -25V, I_D = -10mA
C_{ISS}	Input Capacitance			35	60	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			10	20		
C_{RSS}	Reverse Transfer Capacitance			3	10		
$t_{d(ON)}$	Turn-ON Delay Time			5	10	ns	V_{DD} = -25V, I_D = -10mA, R_S = 50Ω
t_r	Rise Time			8	15		
$t_{d(OFF)}$	Turn-OFF Delay Time			8	15		
t_f	Fall Time			5	10		
V_{SD}	Diode Forward Voltage Drop			-0.8	-1.5	V	V_{GS} = 0, I_{SD} = -0.1A
t_{rr}	Reverse Recovery Time			200		ns	V_{GS} = 0, I_{SD} = -0.1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

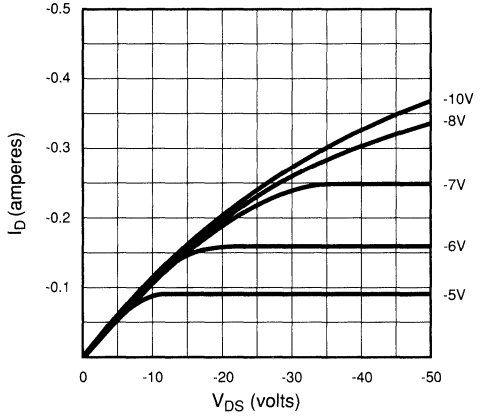
Switching Waveforms and Test Circuit



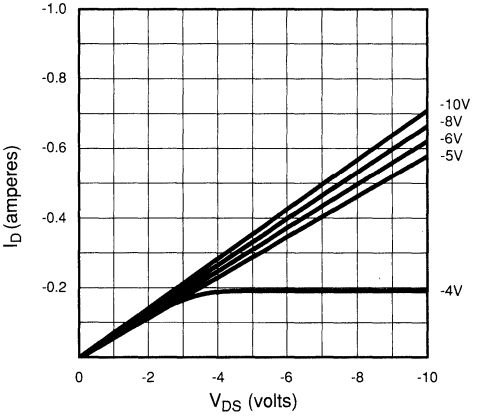


Typical Performance Curves

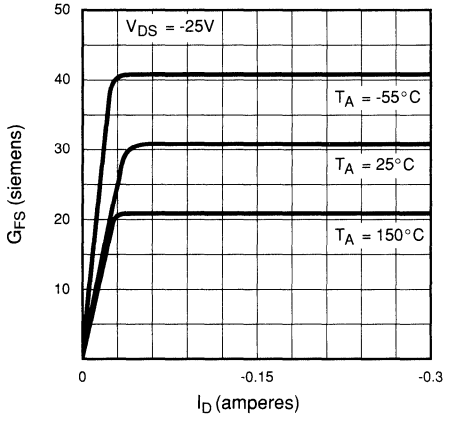
Output Characteristics



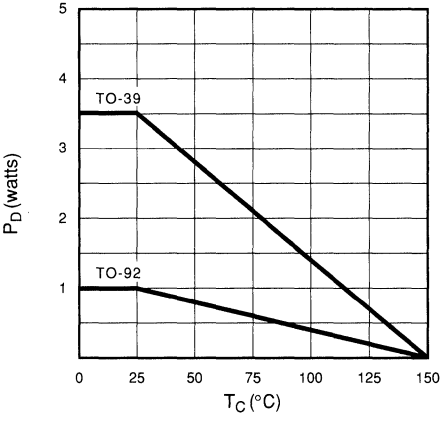
Saturation Characteristics



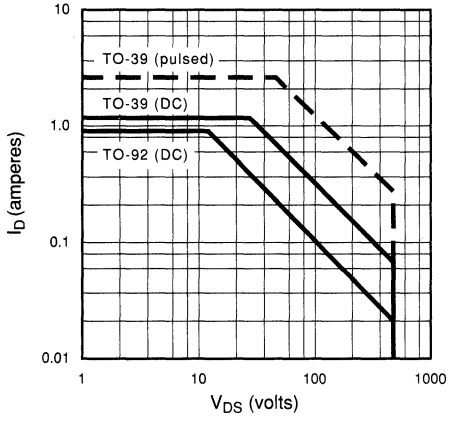
Transconductance vs. Drain Current



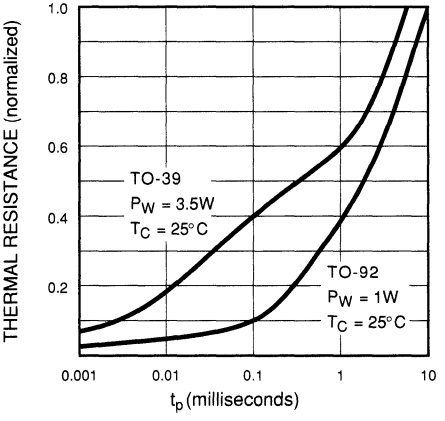
Power Dissipation vs. Case Temperature



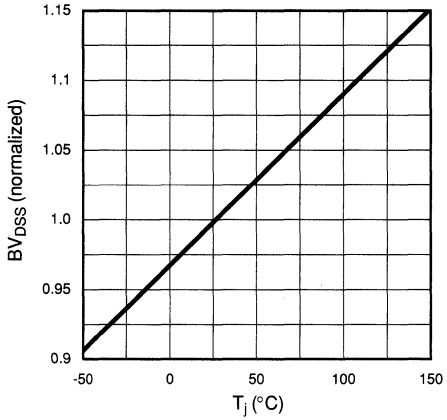
Maximum Rated Safe Operating Area



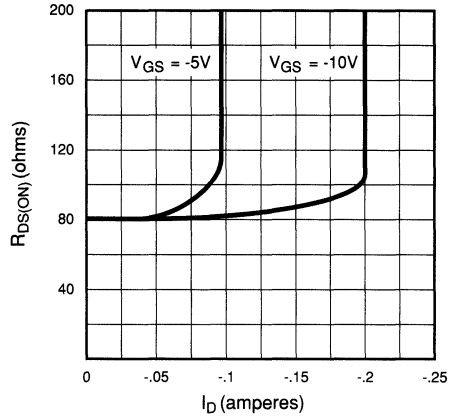
Thermal Response Characteristics



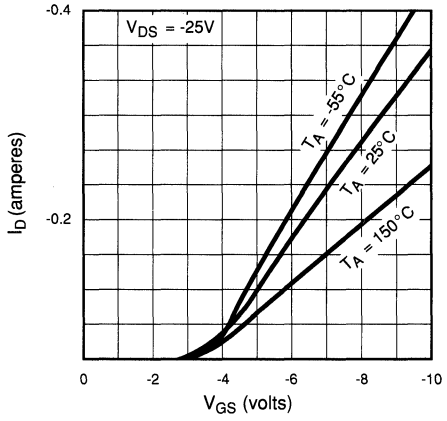
BV_{DSS} Variation with Temperature



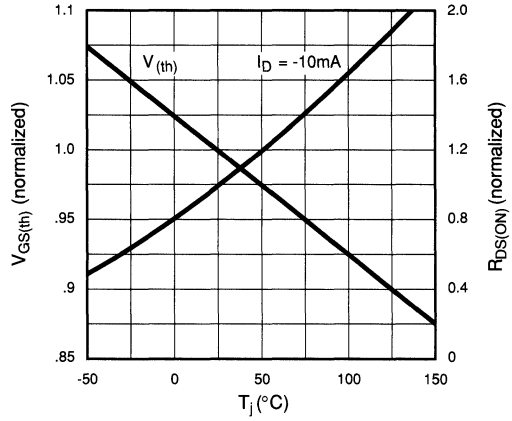
On-Resistance vs. Drain Current



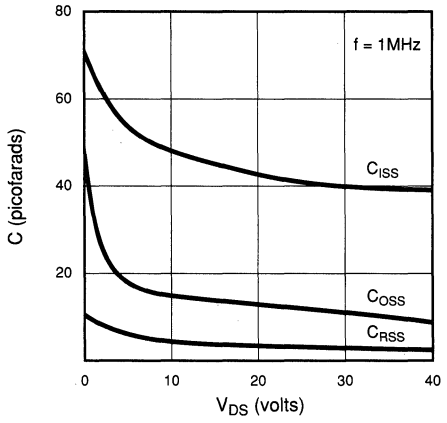
Transfer Characteristics



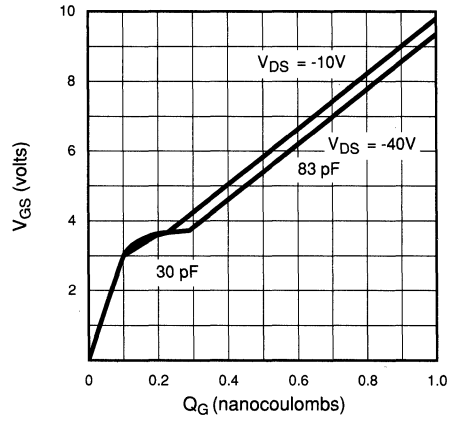
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-39	TO-92	TO-220	DICE
-350V	25Ω	-0.4A	VP0635N2	VP0635N3	VP0635N5	VP0635ND
-400V	25Ω	-0.4A	VP0640N2	VP0640N3	VP0640N5	VP0640ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

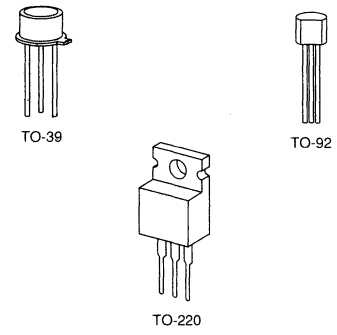
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-92	-0.30A	-0.6A	1W	125	170	-0.30A	-0.6A
TO-39	-0.40A	-0.75A	6W	21	125	-0.40A	-0.75A
TO-220	-0.40A	-0.75A	28W	2.7	70	-0.40A	-0.75A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

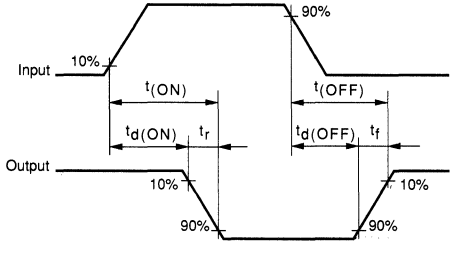
(Notes 1 and 2)

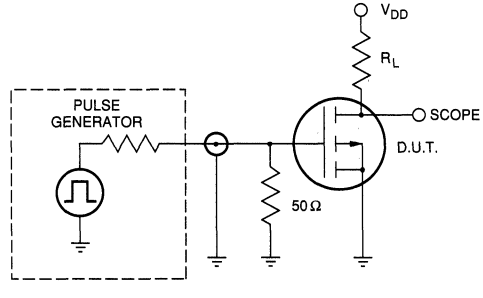
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0640	-400			V	V_{GS} = 0, I_D = -2mA
		VP0635	-350				
$V_{GS(th)}$	Gate Threshold Voltage		-2		-4	V	V_{GS} = V_{DS}, I_D = -2mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-4.8	mV/°C	V_{GS} = V_{DS}, I_D = -2mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			-300		mA	V_{GS} = -5V, V_{DS} = -25V
			-400	-550			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			20		Ω	V_{GS} = -5V, I_D = -100mA
				19	25		V_{GS} = -10V, I_D = -100mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	V_{GS} = -10V, I_D = -100mA
G_{FS}	Forward Transconductance		100			m℧	V_{DS} = -25V, I_D = -100mA
C_{ISS}	Input Capacitance			75	130	pF	V_{GS} = 0, V_{DS} = -25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	75		
C_{RSS}	Reverse Transfer Capacitance			10	20		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = -25V I_D = -100mA R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				10		
V_{SD}	Diode Forward Voltage Drop				1.8	V	V_{GS} = 0, I_{SD} = -100mA
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = -100mA

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

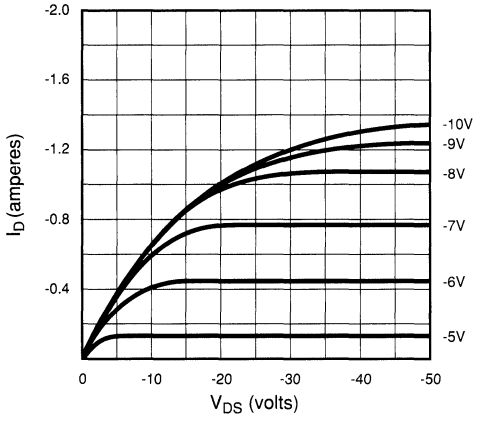
Switching Waveforms and Test Circuit



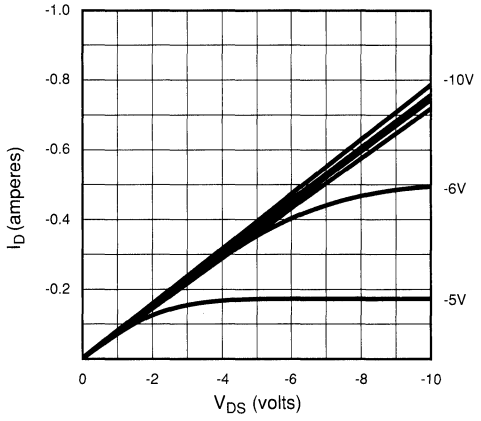


Typical Performance Curves

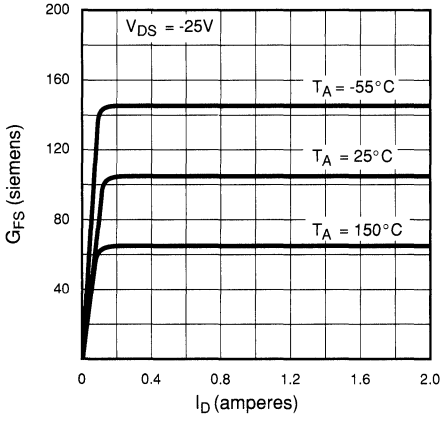
Output Characteristics



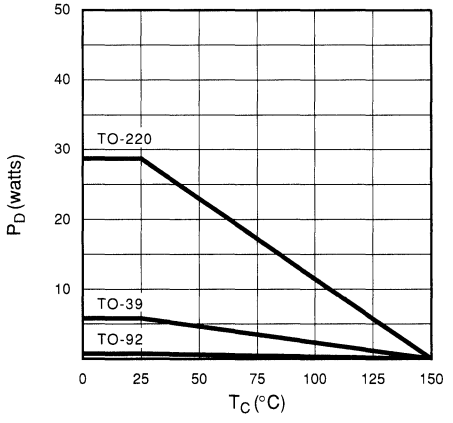
Saturation Characteristics



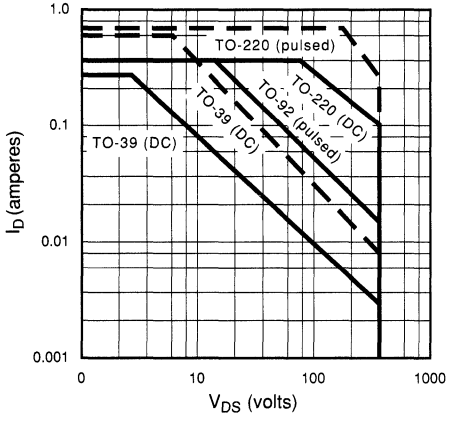
Transconductance vs. Drain Current



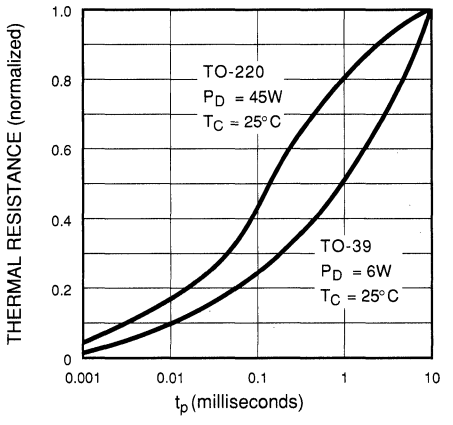
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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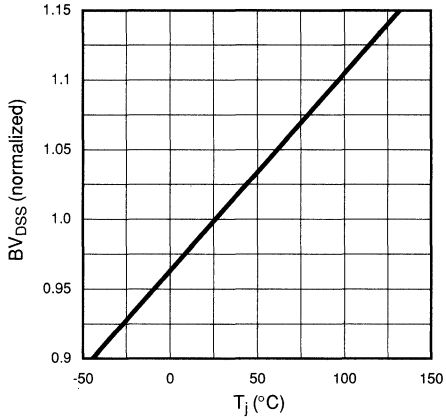
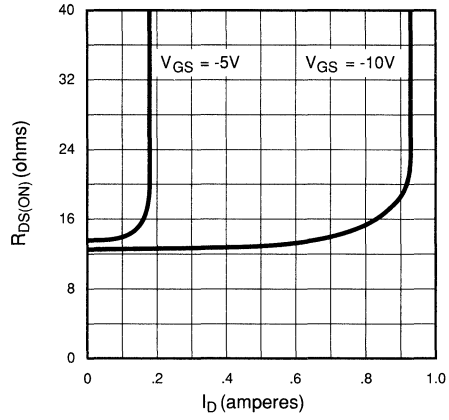
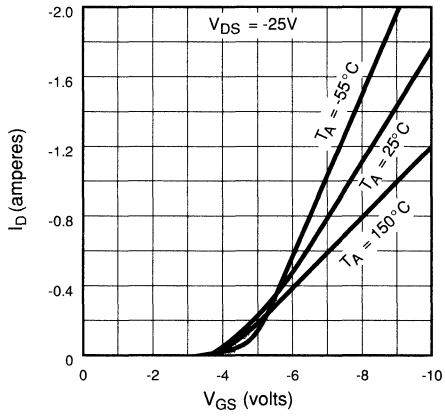
BV$_{DSS}$ Variation with Temperature



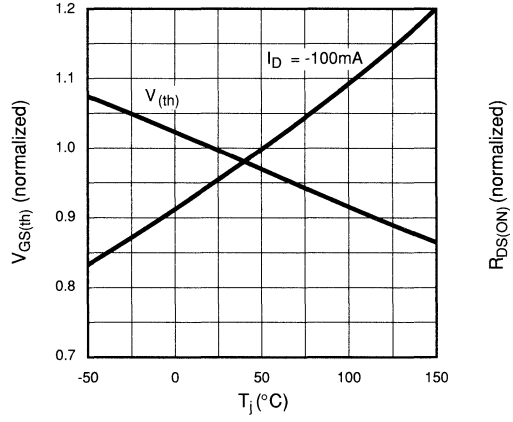
On-Resistance vs. Drain Current



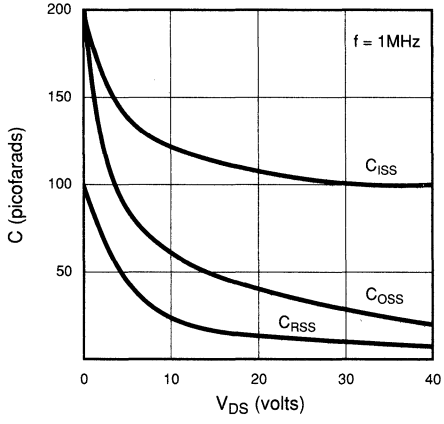
Transfer Characteristics



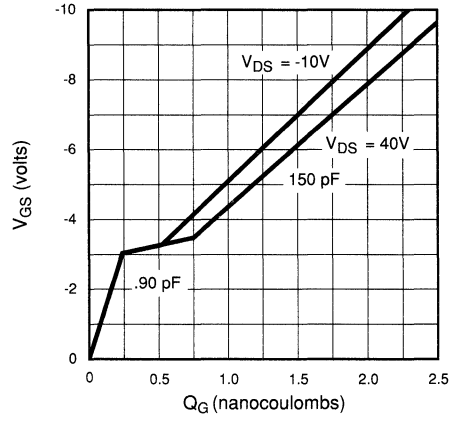
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-39	TO-92	TO-220	DICE
-450V	20Ω	-0.2A	VP0645N2	VP0645N3	VP0645N5	VP0645ND
-500V	20Ω	-0.2A	VP0650N2	VP0650N3	VP0650N5	VP0650ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

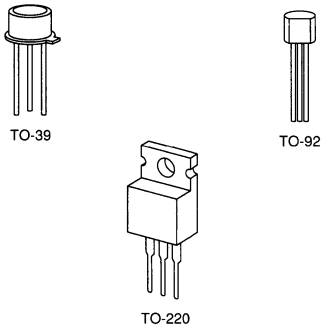
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-92	-0.1A	-0.3A	1W	125	170	-0.1A	-0.3A
TO-39	-0.25A	-0.5A	6W	21	125	-0.25A	-0.5A
TO-220	-0.25A	-0.5A	45W	2.7	70	-0.25A	-0.5A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

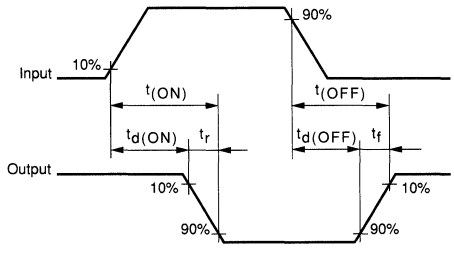
(Notes 1 and 2)

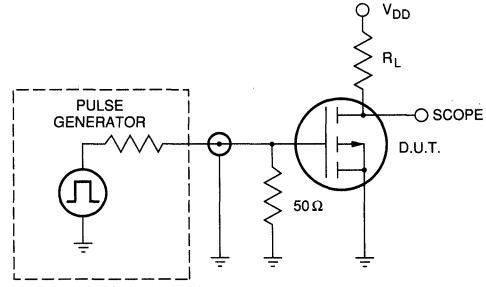
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0650	-500			V	V_{GS} = 0, I_D = -2mA
		VP0645	-450				
$V_{GS(th)}$	Gate Threshold Voltage		-2		-4	V	V_{GS} = V_{DS}, I_D = -2mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-4.8	mV/°C	V_{GS} = V_{DS}, I_D = -2mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			-100		mA	V_{GS} = -5V, V_{DS} = -25V
			-200	-300			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			30		Ω	V_{GS} = -5V, I_D = -100mA
				22	30		V_{GS} = -10V, I_D = -100mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	V_{GS} = -10A, I_D = -100mA
G_{FS}	Forward Transconductance		50			m℧	V_{DS} = -25V, I_D = -100mA
C_{ISS}	Input Capacitance			75	130	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	75		
C_{RSS}	Reverse Transfer Capacitance			10	20		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = -25V, I_D = -100mA, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				15		
V_{SD}	Diode Forward Voltage Drop				1.8	V	V_{GS} = 0, I_{SD} = -50mA
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = -50mA

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

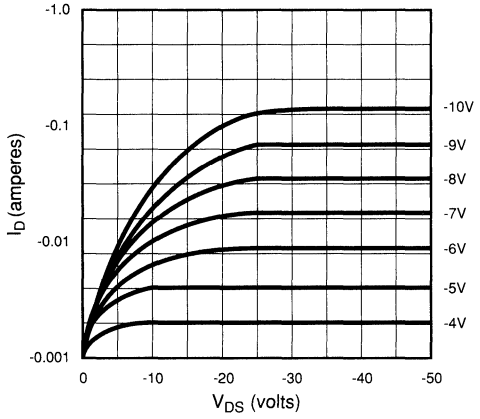
Switching Waveforms and Test Circuit



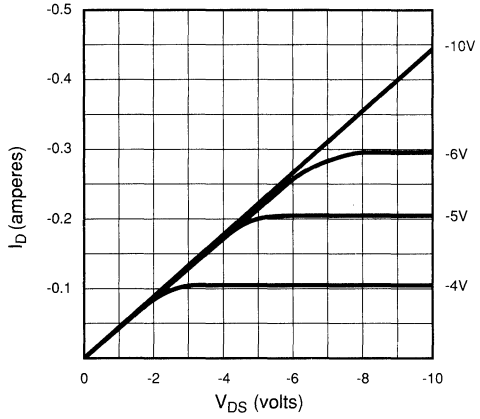


Typical Performance Curves

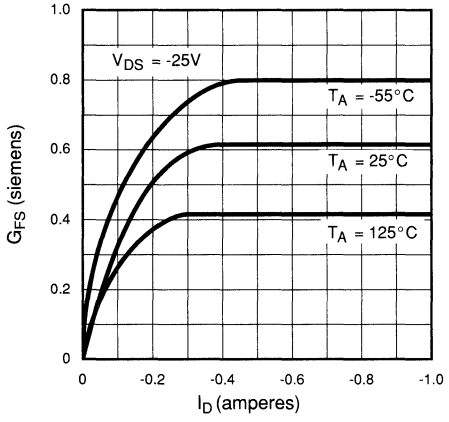
Output Characteristics



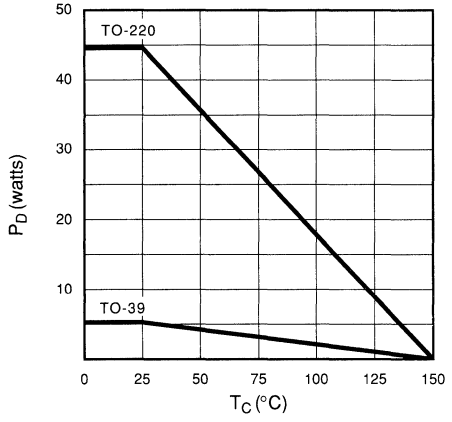
Saturation Characteristics



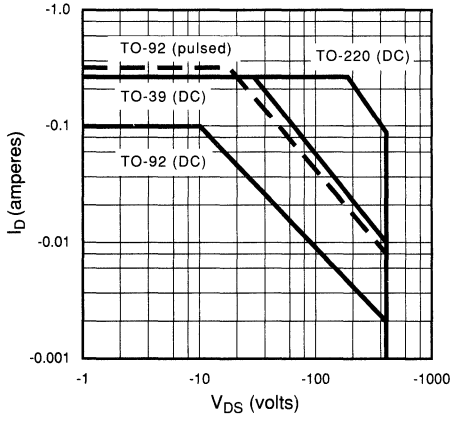
Transconductance vs. Drain Current



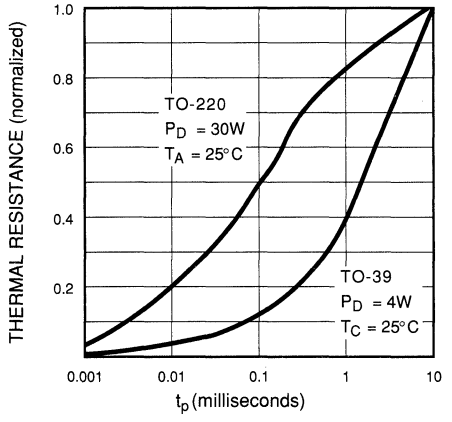
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

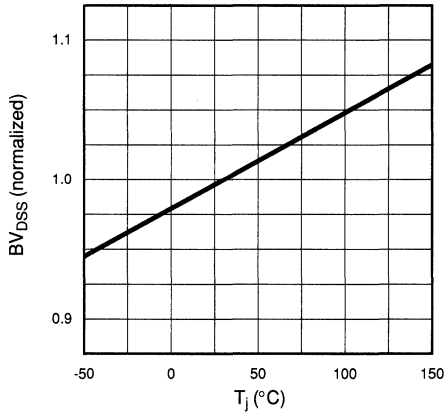


Thermal Response Characteristics

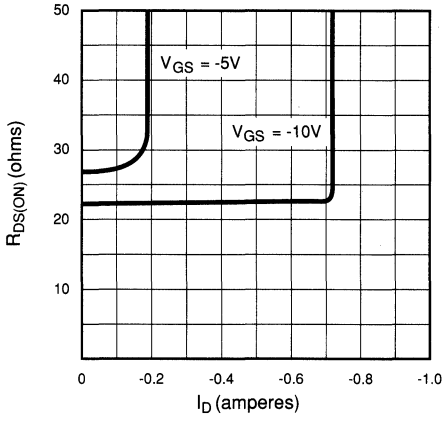


9

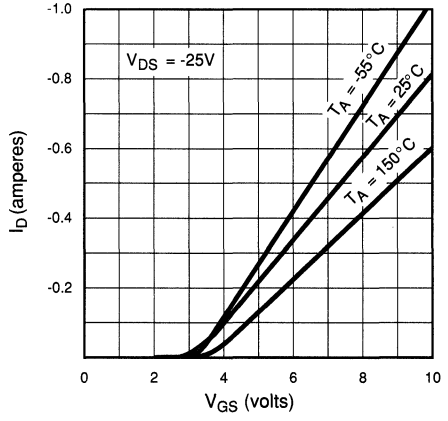
BV$_{DSS}$ Variation with Temperature



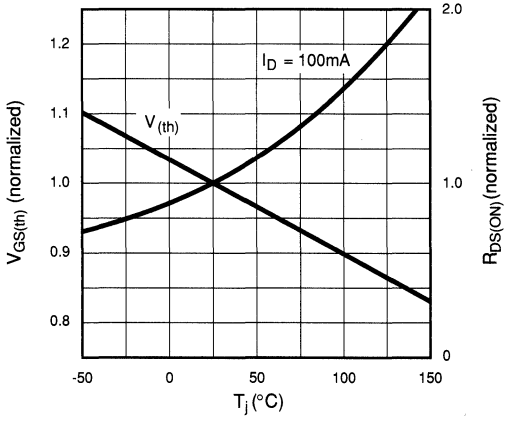
On-Resistance vs. Drain Current



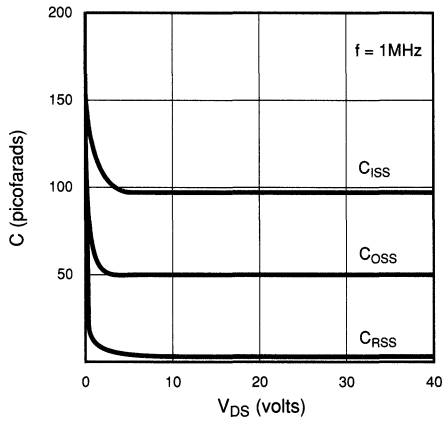
Transfer Characteristics



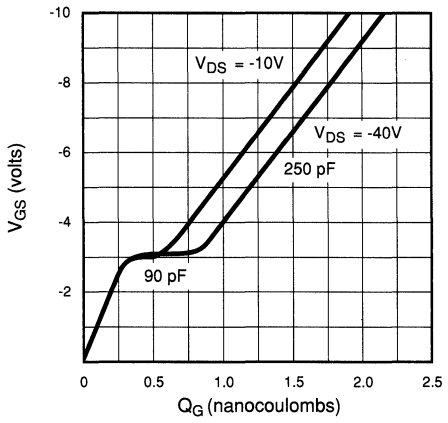
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
-80V	5Ω	-1.1A	VP0808B	VP0808L
-100V	5Ω	-1.1A	VP1008B	VP1008L

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

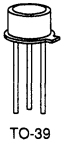
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

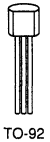
Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-39



TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation	θ_{ja} °C/W	θ_{jc} °C/W
TO-39	−0.88A	−3A	6.25W	170	20
TO-92	−0.21A	−3A	0.4W	312.5	41

*I_D (continuous) is limited by max rated T_j.

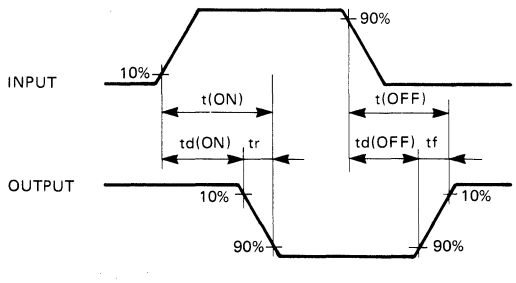
Electrical Characteristics (@ 25°C unless otherwise specified)

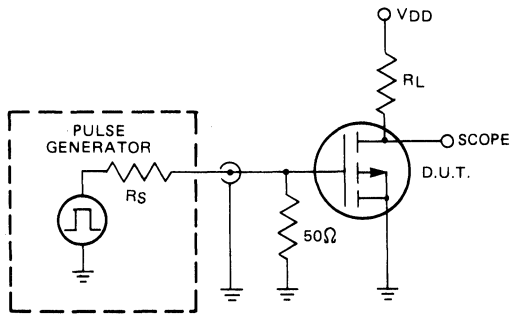
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1008	−100			V	I_D = −10μA, V_{GS} = 0
		VP0808	−80				
$V_{GS(th)}$	Gate Threshold Voltage		−2		−4.5	V	V_{GS} = V_{DS}, I_D = −1mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = 30V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				−10	μA	V_{GS} = 0V, V_{DS} = Max Rating
					−500		V_{GS} = 0V, V_{DS} = Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		−1.1			A	V_{GS} = −10V, V_{DS} ≥ 2 $V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance				5	Ω	V_{GS} = −10V, I_D = −1A
G_{FS}	Forward Transconductance		200			m℧	V_{DS} ≥ 2 $V_{DS(ON)}$, I_D = −0.5A
C_{ISS}	Input Capacitance				150	pF	V_{GS} = 0, V_{DS} = 25V, f = 1MHz
C_{OSS}	Common Source Output Capacitance				60		
C_{RSS}	Reverse Transfer Capacitance				25		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = −25V, I_D = −0.5A, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				10		
t_f	Fall Time				10		
V_{SD}	Diode Forward Voltage Drop	VP1008		1.2		V	I_{SD} = 0.21A, V_{GS} = 0
		VP0808		1.2			I_{SD} = 0.9A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	DICE
-60V	2Ω	-5A	VP1106N1	VP1106N2	VP1106N5	VP1106ND
-100V	2Ω	-5A	VP1110N1	VP1110N2	VP1110N5	VP1110ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

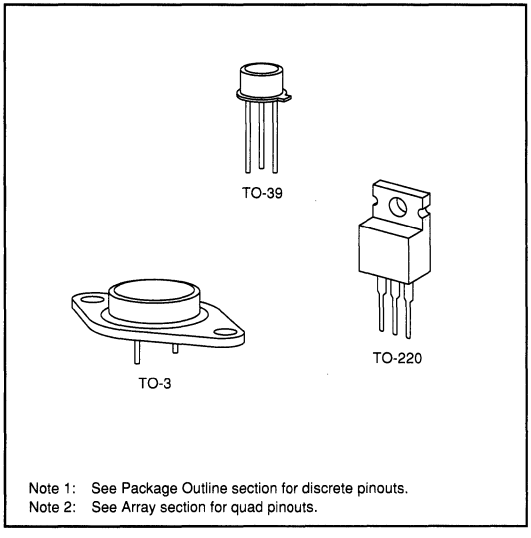
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-3	-6.0A	-15A	75W	50	1.66	-6A	-15A
TO-39	-1.5A	-7A	6W	125	20.8	-1.5A	-7A
TO-220	-4.0A	-12A	45W	70	2.78	-4A	-12A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

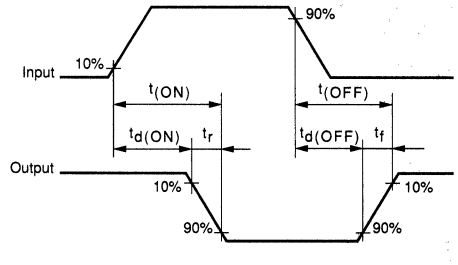
(Notes 1 and 2)

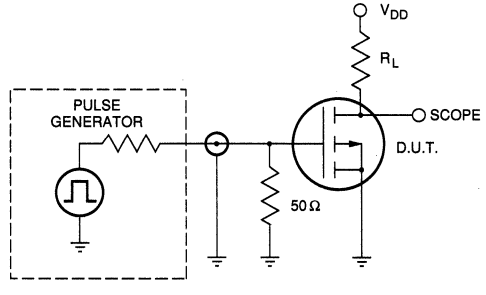
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1110	-100			V	I_D = -5mA, V_{GS} = 0
		VP1106	-60				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	V_{GS} = V_{DS}, I_D = -5mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.0		mV/°C	I_D = -5mA, V_{GS} = V_{DS}
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-50	µA	V_{GS} = 0, V_{DS} = Max Rating
					-5	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-1.0			A	V_{GS} = -5V, V_{DS} = -25V
			-5.0				V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			2	5	Ω	V_{GS} = -5V, I_D = -0.5A
				1.5	2		V_{GS} = -10V, I_D = -2.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.7	1.0	%/°C	I_D = -1.0A, V_{GS} = -10V
G_{FS}	Forward Transconductance		0.9	1.3		℧	V_{DS} = -25V, I_D = -2.0A
C_{ISS}	Input Capacitance			300	350	pF	V_{GS} = 0, V_{DS} = -20V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			100	150		
C_{RSS}	Reverse Transfer Capacitance			20	35		
$t_{d(ON)}$	Turn-ON Delay Time			35	40	ns	V_{DD} = -18V, I_D = -2.0A, R_S = 50Ω
t_r	Rise Time			20	30		
$t_{d(OFF)}$	Turn-OFF Delay Time			40	50		
t_f	Fall Time			10	20		
V_{SD}	Diode Forward Voltage Drop			-1.4	-2.5	V	I_{SD} = -1.0A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			400		ns	I_{SD} = -1.0A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

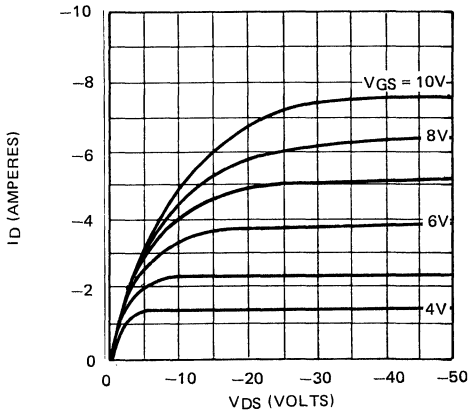
Switching Waveforms and Test Circuit



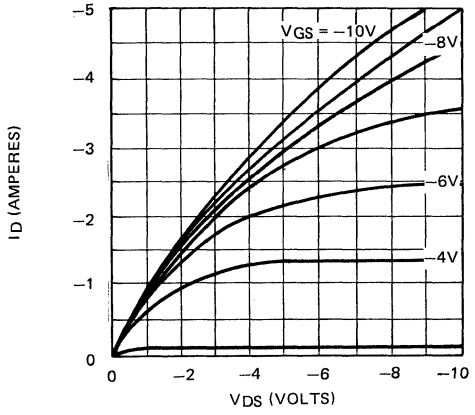


Typical Performance Curves

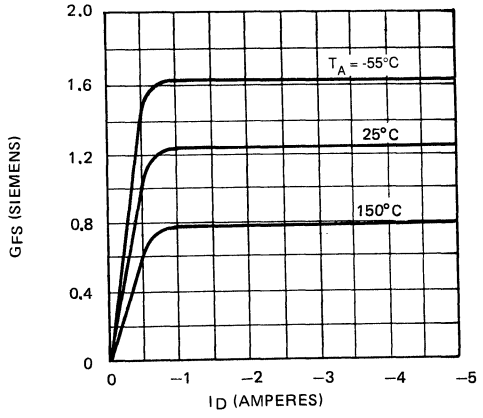
Output Characteristics



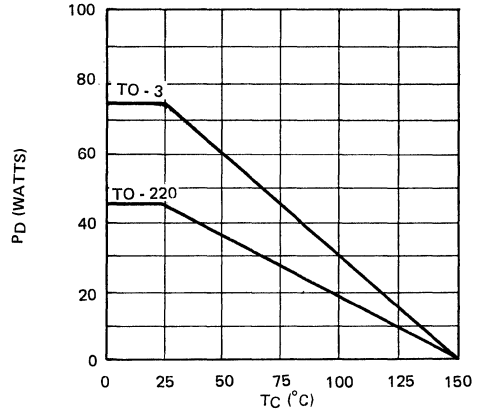
Saturation Characteristics



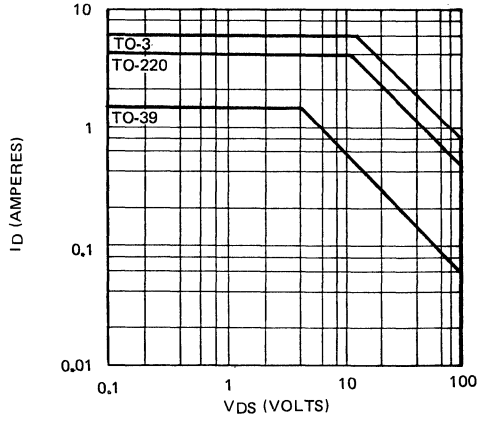
Transconductance Vs. Drain Current



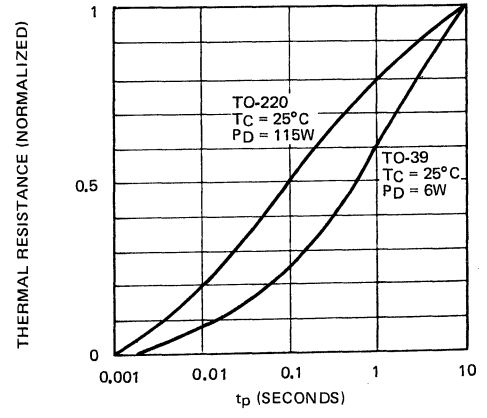
Power Dissipation Vs. Case Temperature



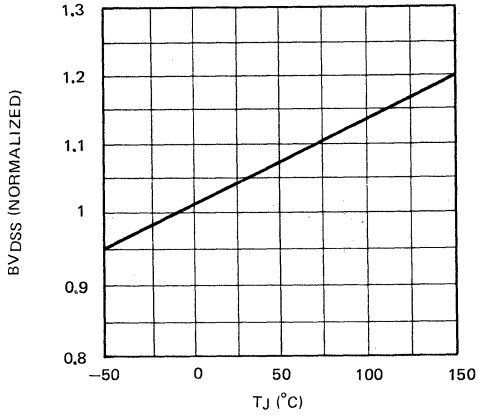
Maximum Rated Safe Operating Area



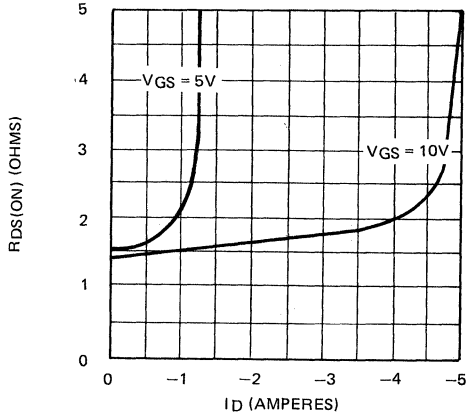
Thermal Response Characteristics



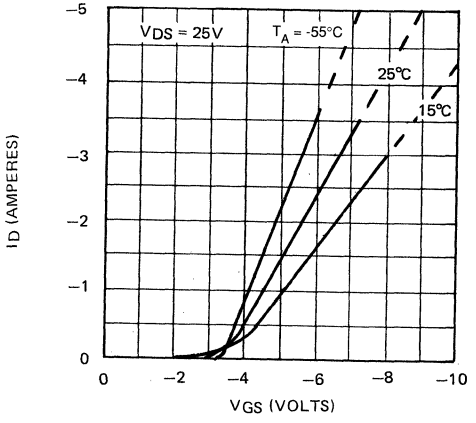
BVDSS Variation with Temperature



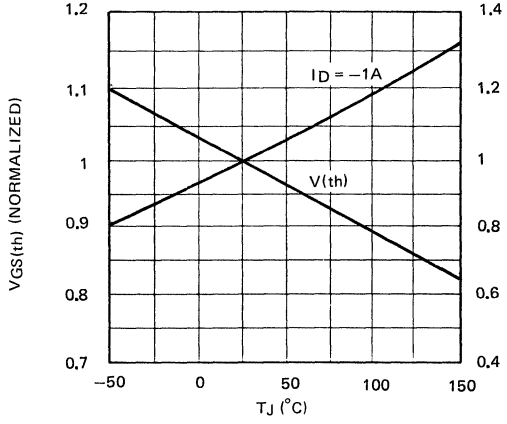
ON-Resistance Vs. Drain Source Current



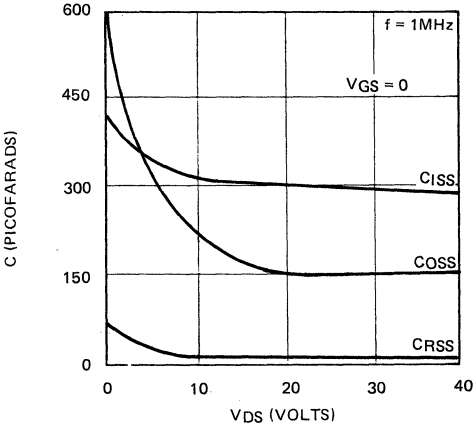
Transfer Characteristics



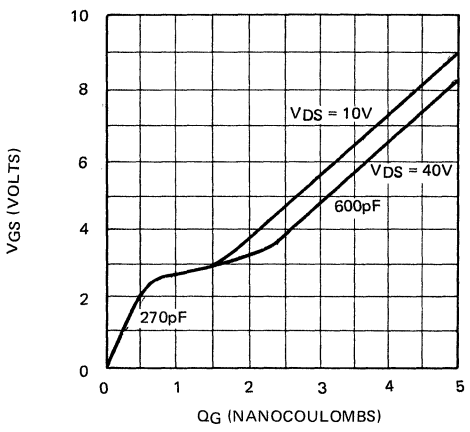
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	DICE
-160V	5Ω	-1.5A	VP1116N1	VP1116N2	VP1116N5	VP1116ND
-200V	5Ω	-1.5A	VP1120N1	VP1120N2	VP1120N5	VP1120ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

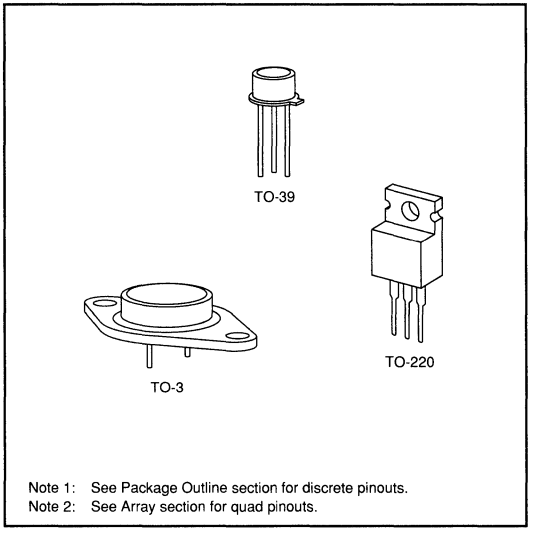
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-3	-2.5A	-7.5A	75W	50	1.6	-2.5A	-7.5A
TO-39	-0.8A	-3A	6W	125	20.8	-0.8A	-3A
TO-220	-1.8A	-7A	45W	70	2.7	-1.8A	-7A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

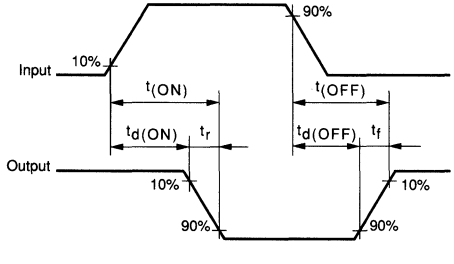
(Notes 1 and 2)

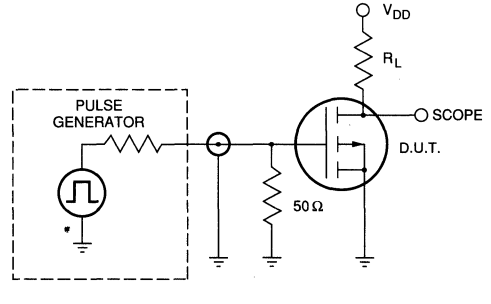
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1120	-200			V	I_D = -5mA, V_{GS} = 0
		VP1116	-160				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	V_{GS} = V_{DS}, I_D = -5mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.5	-6	mV/°C	I_D = -5mA, V_{GS} = V_{DS}
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-50	µA	V_{GS} = 0, V_{DS} = Max Rating
					-10	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		0.5	1.5		A	V_{GS} = -5V, V_{DS} = -25V
			1.5	4			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.3	7	Ω	V_{GS} = -5V, I_D = -0.5A
				3	5		V_{GS} = -10V, I_D = -1.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.8	1.2	%/°C	I_D = -1.0A, V_{GS} = -10V
G_{FS}	Forward Transconductance		0.5	0.75		℧	V_{DS} = -25V, I_D = -1.0A
C_{ISS}	Input Capacitance			300	350	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			60	80		
C_{RSS}	Reverse Transfer Capacitance			10	25		
$t_{d(ON)}$	Turn-ON Delay Time			8	25	ns	V_{DD} = -25V, I_D = -1.0A, R_S = 50Ω
t_r	Rise Time			4	20		
$t_{d(OFF)}$	Turn-OFF Delay Time			24	40		
t_f	Fall Time			8	20		
V_{SD}	Diode Forward Voltage Drop			-1.2	-2.0	V	I_{SD} = -1.0A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			350		ns	I_{SD} = -1.0A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

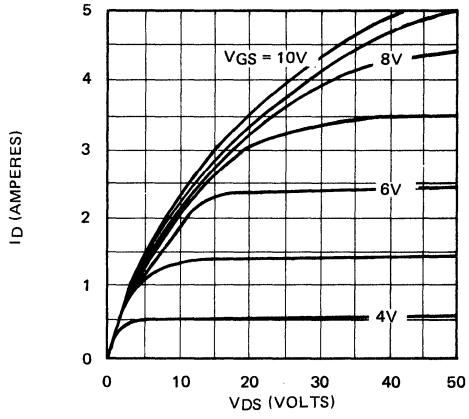
Switching Waveforms and Test Circuit



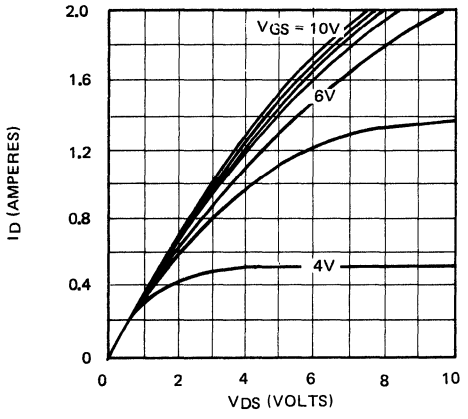


Typical Performance Curves

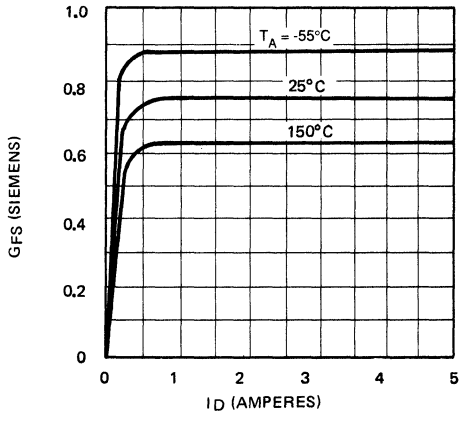
Output Characteristics



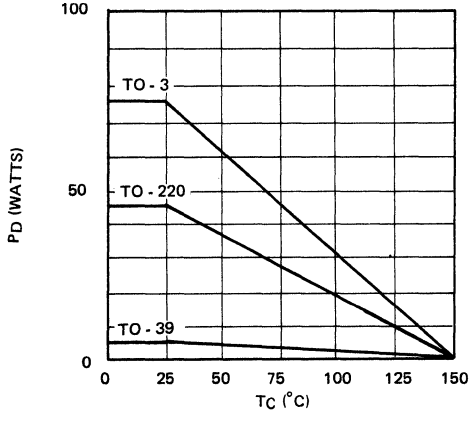
Saturation Characteristics



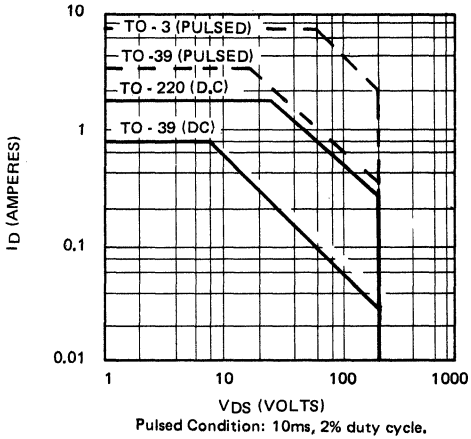
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

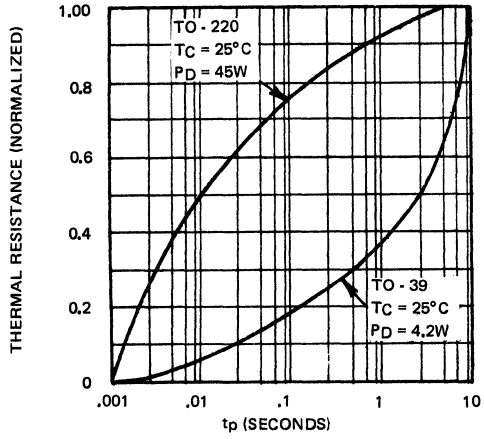


Maximum Rated Safe Operating Area

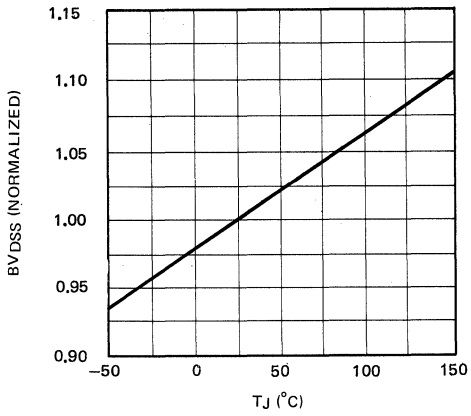


Pulsed Condition: 10ms, 2% duty cycle.

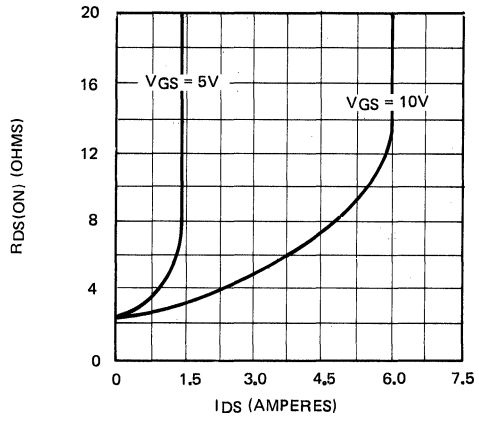
Thermal Response Characteristics



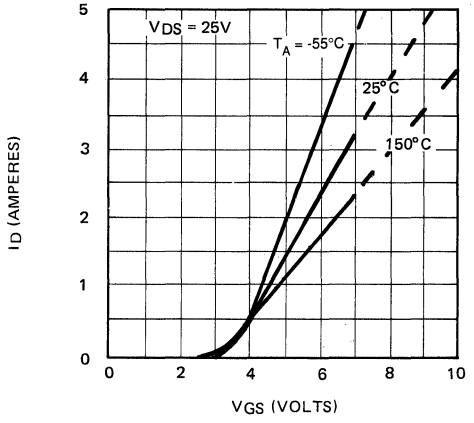
BVDSS Variation with Temperature



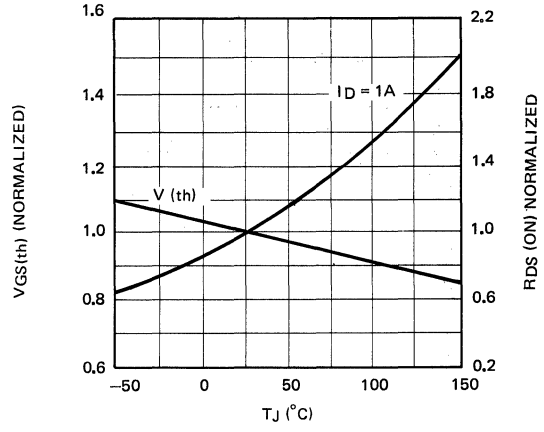
ON - Resistance Vs. Drain Current



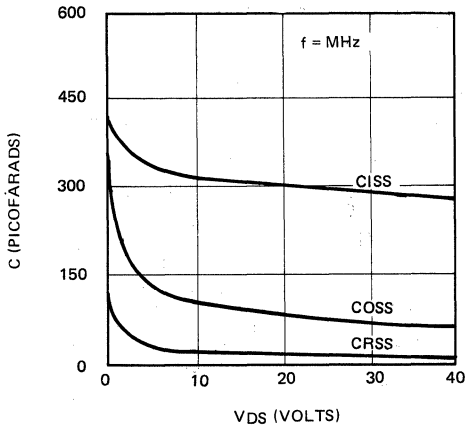
Transfer Characteristics



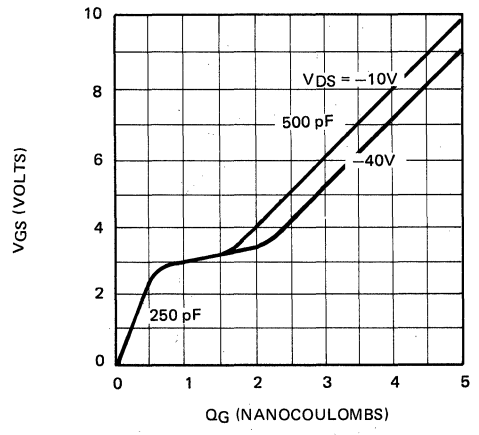
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	DICE
-40V	0.8Ω	-6A	VP1204N1	VP1204N2	VP1204N5	VP1204ND
-60V	0.8Ω	-6A	VP1206N1	VP1206N2	VP1206N5	VP1206ND
-100V	0.8Ω	-6A	VP1210N1	VP1210N2	VP1210N5	VP1210ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

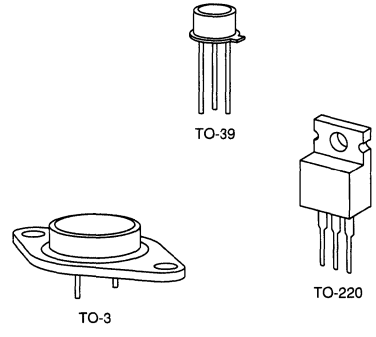
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-3	-7.0A	-14A	100W	30	1.25	-7A	-14A
TO-39	-2.5A	-11A	6.5W	125	20	-2.5A	-11A
TO-220	-5.0A	-14A	45W	70	2.75	-5A	-14A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

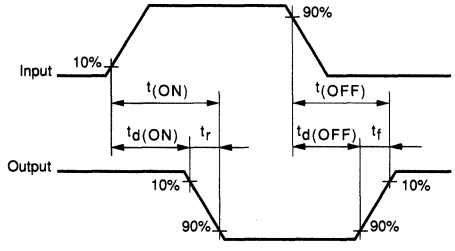
(Notes 1 and 2)

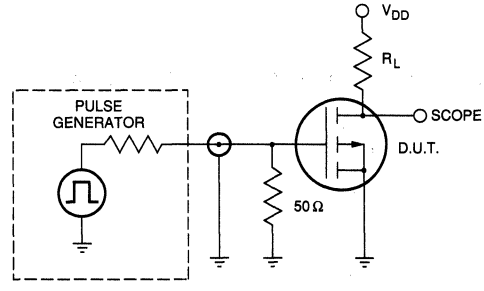
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1210	-100			V	I_D = -10mA, V_{GS} = 0
		VP1206	-60				
		VP1204	-40				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	V_{GS} = V_{DS}, I_D = -10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.7	-5.5	mV/°C	I_D = -10mA, V_{GS} = V_{DS}
I_{GSS}	Gate Body Leakage			-1.0	-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-100	µA	V_{GS} = 0, V_{DS} = Max Rating
					-10	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-1.5	-2.0		A	V_{GS} = -5V, V_{DS} = -25V
			-6.0	-12.0			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			1.0	1.4	Ω	V_{GS} = -5V, I_D = -1A
				0.5	0.8		V_{GS} = -10V, I_D = -3A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.0	1.5	%/°C	I_D = -10A, V_{GS} = -10V
G_{FS}	Forward Transconductance		1	2		℧	V_{DS} = -25V, I_D = -3A
C_{ISS}	Input Capacitance			550	650	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			250	275		
C_{RSS}	Reverse Transfer Capacitance			25	40		
$t_{d(ON)}$	Turn-ON Delay Time			10	30	ns	V_{DD} = -25V, I_D = -4A, R_S = 50Ω
t_r	Rise Time			17	40		
$t_{d(OFF)}$	Turn-OFF Delay Time			70	105		
t_f	Fall Time			35	60		
V_{SD}	Diode Forward Voltage Drop			-1.2	-1.6	V	I_{SD} = -5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			500		ns	I_{SD} = -1A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

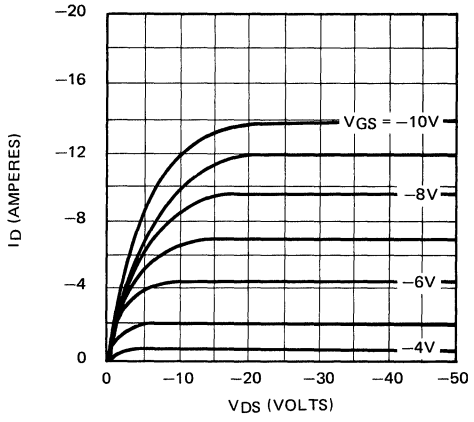
Switching Waveforms and Test Circuit



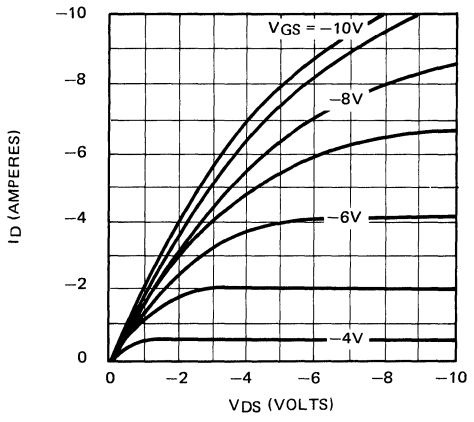


Typical Performance Curves

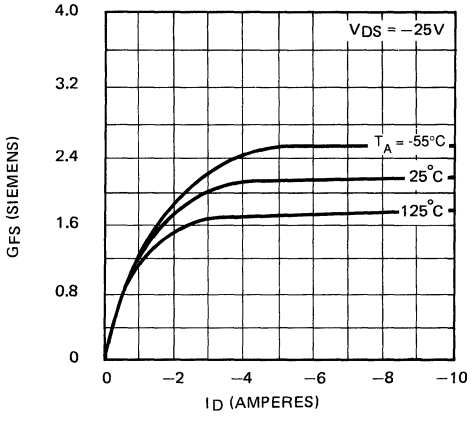
Output Characteristics



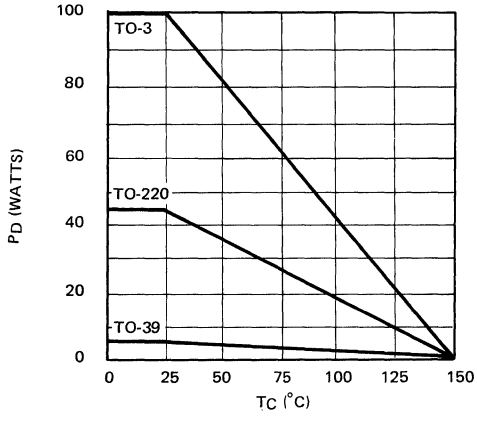
Saturation Characteristics



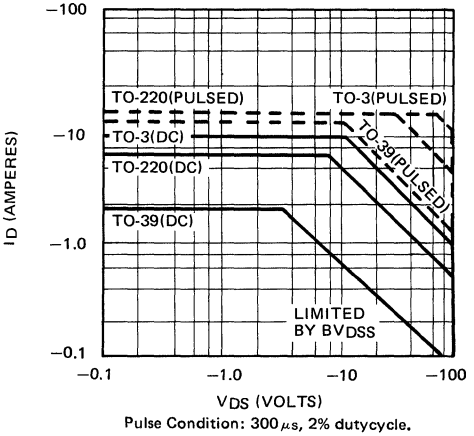
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

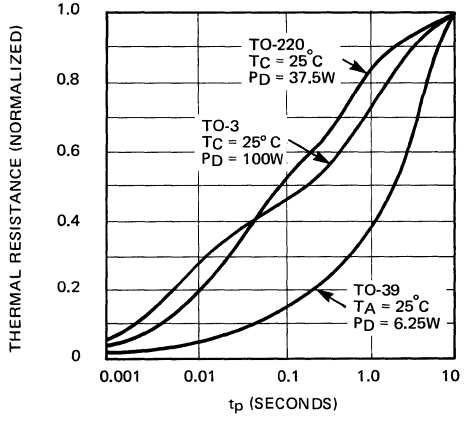


Maximum Rated Safe Operating Area

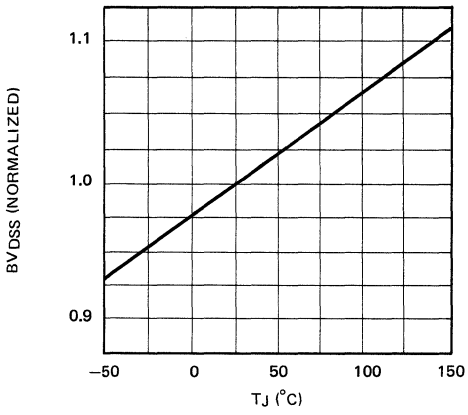


Pulse Condition: 300μs, 2% dutycycle.

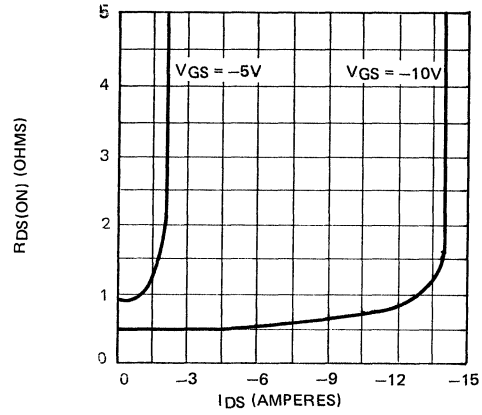
Thermal Response Characteristics



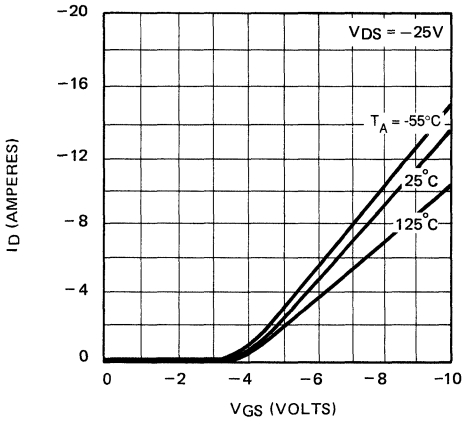
BVDSS Variation with Temperature



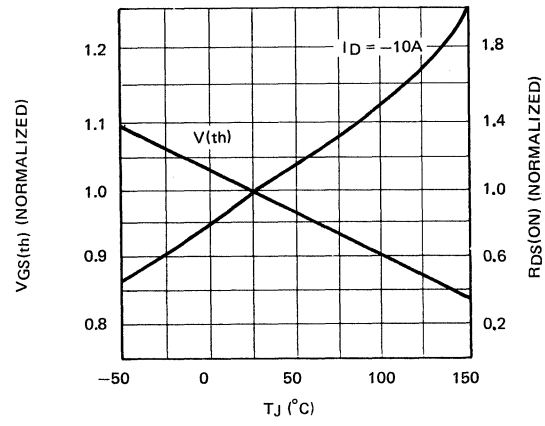
ON-Resistance Vs. Drain Current



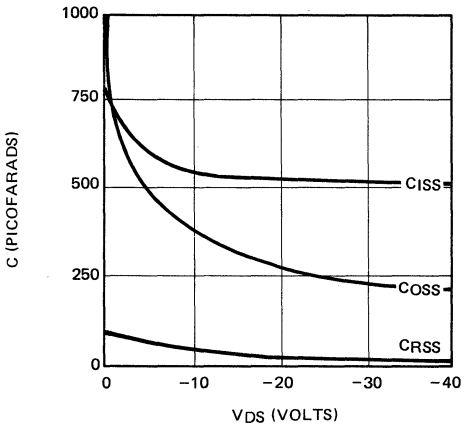
Transfer Characteristics



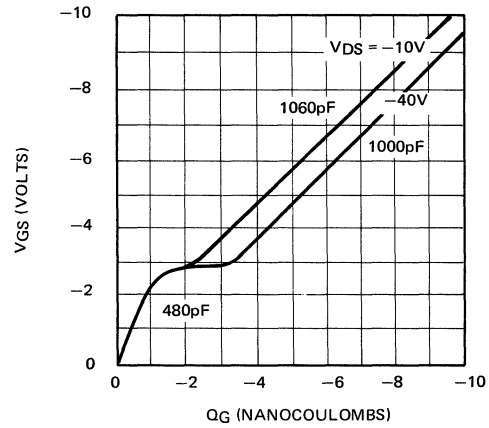
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	DICE
-160V	2.5Ω	-4.0A	VP1216N1	VP1216N2	VP1216N5	VP1216ND
-200V	2.5Ω	-4.0A	VP1220N1	VP1220N2	VP1220N5	VP1220ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

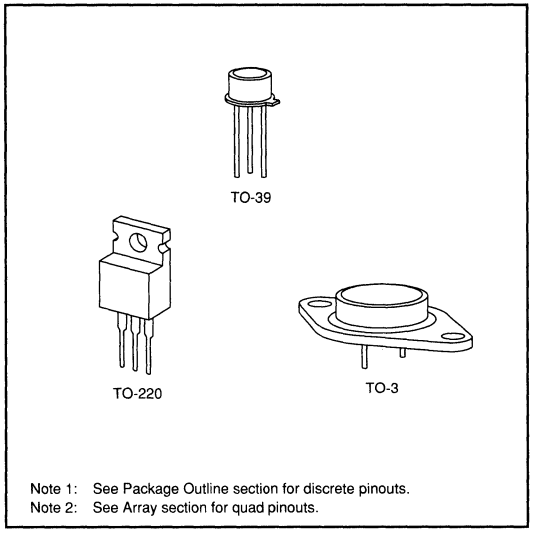
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-3	-4.5A	-8.0A	100W	30	1.25	-4.5A	-8.0A
TO-39	-2.0A	-4.5A	6.5W	125	20	-2.0A	-4.5A
TO-220	-3.5A	-6.0A	45W	70	2.75	-3.5A	-6.0A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

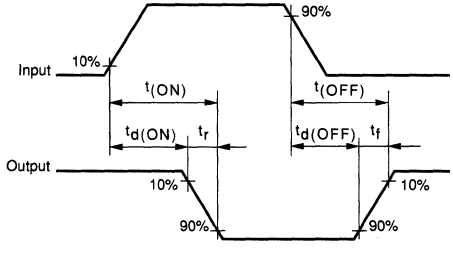
(Notes 1 and 2)

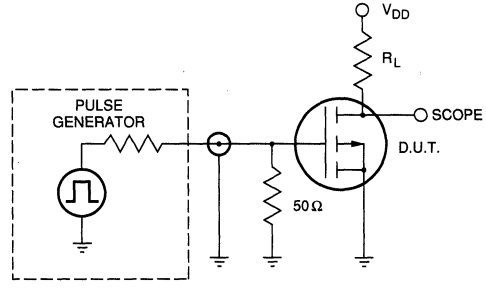
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1220	-200			V	I_D = -10mA, V_{GS} = 0
		VP1216	-160				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	V_{GS} = V_{DS}, I_D = -10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.5	-4.5	mV/°C	V_{GS} = V_{DS}, I_D = -10mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			-1.0	-100	µA	V_{GS} = 0, V_{DS} = Max Rating
					-10	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-.0.5	-1.0		A	V_{GS} = -5V, V_{DS} = -25V
			-4.0	-7.0			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			2.0	4.0	Ω	V_{GS} = -5V, I_D = -0.5A
				1.6	2.5		V_{GS} = -10V, I_D = -1.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.5	1.0	%/°C	I_D = -1A, V_{GS} = -10V
G_{FS}	Forward Transconductance		0.8	1.2		℧	V_{DS} = -25V, I_D = -3.0A
C_{ISS}	Input Capacitance			600	650	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			200	250		
C_{RSS}	Reverse Transfer Capacitance			20	30		
$t_{d(ON)}$	Turn-ON Delay Time			30	40	ns	V_{DD} = -15V, I_D = -2.0A, R_S = 50Ω
t_r	Rise Time			26	35		
$t_{d(OFF)}$	Turn-OFF Delay Time			45	90		
t_f	Fall Time			20	40		
V_{SD}	Diode Forward Voltage Drop			-1.4	-2.0	V	I_{SD} = -0.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			500		ns	I_{SD} = -0.5A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

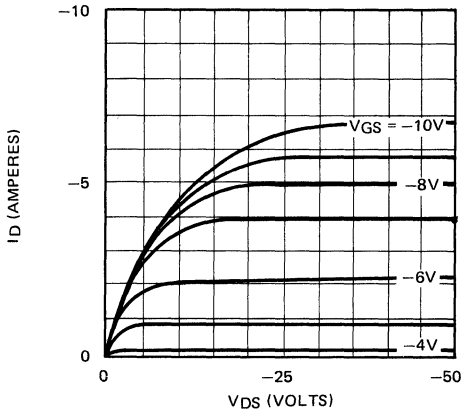
Switching Waveforms and Test Circuit



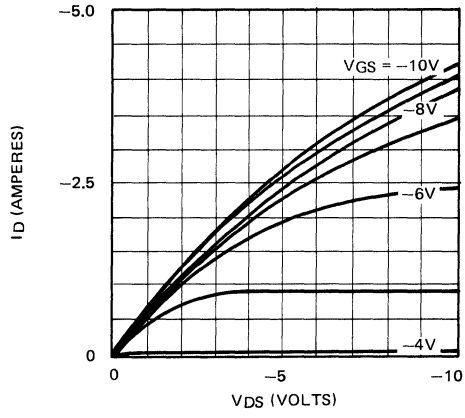


Typical Performance Curves

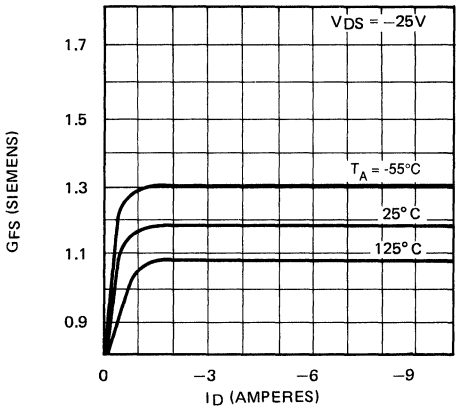
Output Characteristics



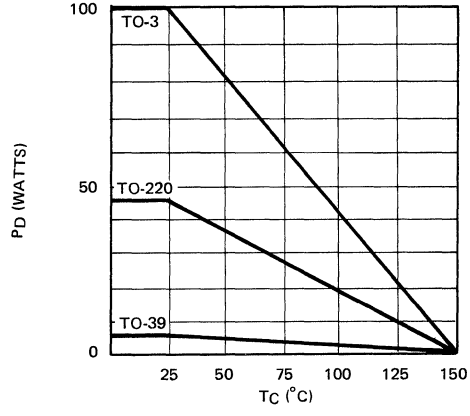
Saturation Characteristics



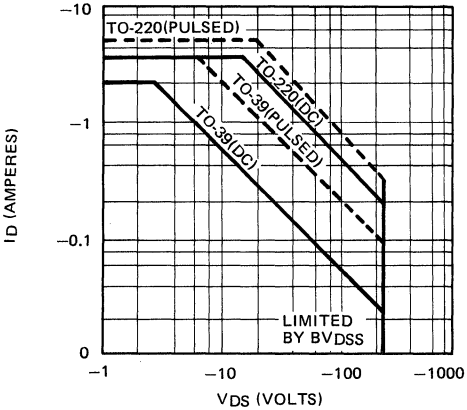
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

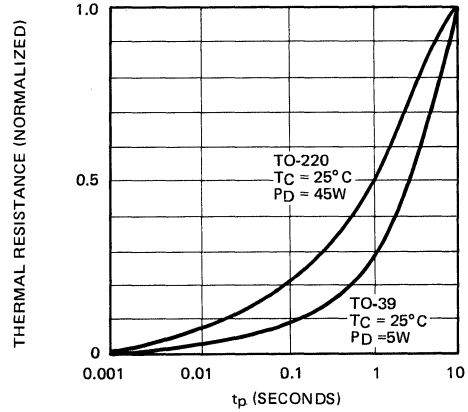


Maximum Rated Safe Operating Area

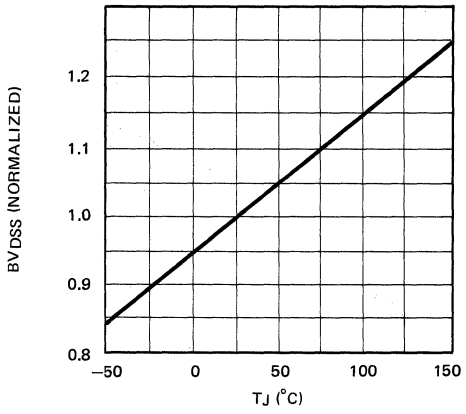


Pulse Condition: 300 μs,2% dutycycle.

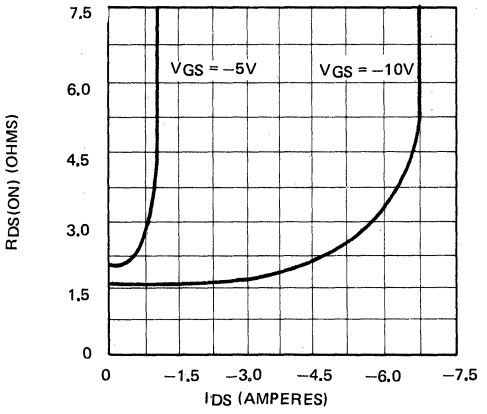
Thermal Response Characteristics



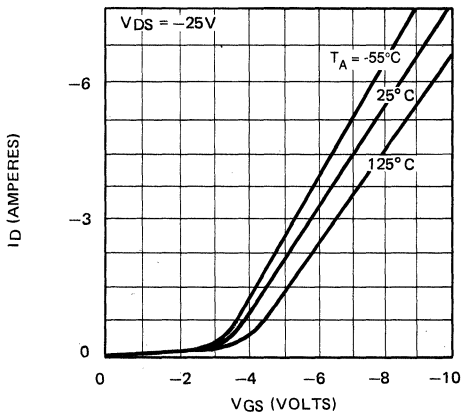
BVDSS Variation with Temperature



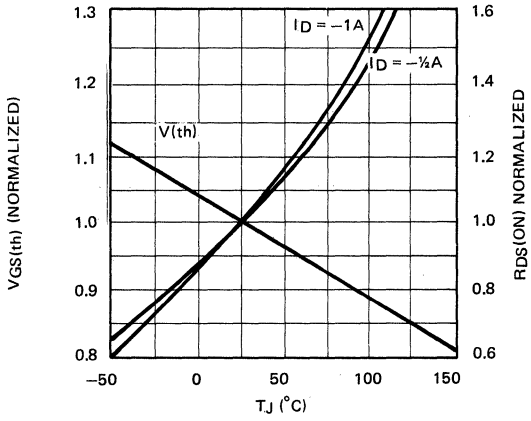
ON-Resistance Vs. Drain Current



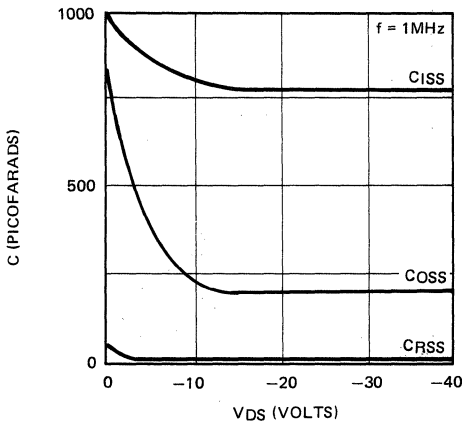
Transfer Characteristics



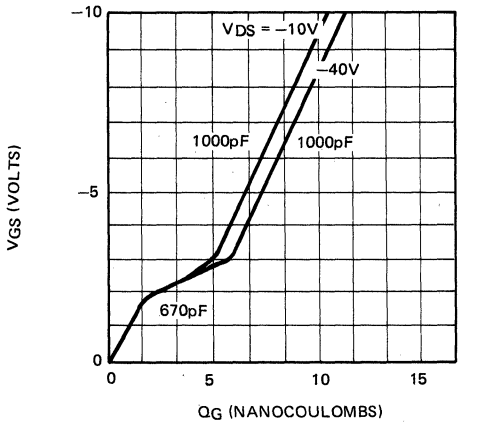
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
-40V	25Ω	-0.25A	VP1304N2	VP1304N3
-60V	25Ω	-0.25A	VP1306N2	VP1306N3
-100V	25Ω	-0.25A	VP1310N2	VP1310N3

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

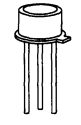
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-39

TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-39	-0.25A	-0.8A	3.0W	125	41	-0.25A	-0.8A
TO-92	-0.15A	-0.65A	0.8W	170	155	-0.15A	-0.65A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

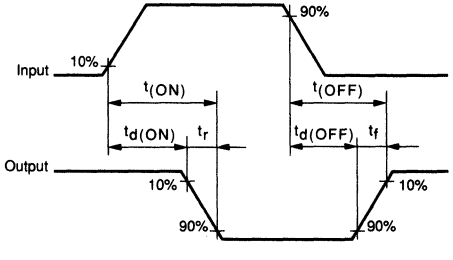
(Notes 1 and 2)

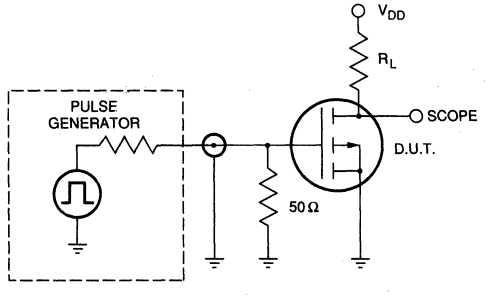
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1310	-100			V	I_D = -1mA, V_{GS} = 0
		VP1306	-60				
		VP1304	-40				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	V_{GS} = V_{DS}, I_D = -1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.2	-3.85	mV/°C	V_{GS} = V_{DS}, I_D = -1mA
I_{GSS}	Gate Body Leakage			-0.1	-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	μA	V_{GS} = 0, V_{DS} = Max Rating
					-500		V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-.08	-0.2		A	V_{GS} = -5V, V_{DS} = -25V
			-0.25	-0.45			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			30	40	Ω	V_{GS} = -5V, I_D = -50mA
				16	25		V_{GS} = -10V, I_D = -250mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.8	1.1	%/°C	I_D = -250mA, V_{GS} = -10V
G_{FS}	Forward Transconductance		75	120		m℧	V_{DS} = -25V, I_D = -200mA
C_{ISS}	Input Capacitance			20	35	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			12	15		
C_{RSS}	Reverse Transfer Capacitance			3	5		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	V_{DD} = -25V, I_D = -200mA, R_S = 50Ω
t_r	Rise Time			3	5		
$t_{d(OFF)}$	Turn-OFF Delay Time			3	5		
t_f	Fall Time			3	5		
V_{SD}	Diode Forward Voltage Drop			-1.2	-1.7	V	I_{SD} = -1A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			350		ns	I_{SD} = -1A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

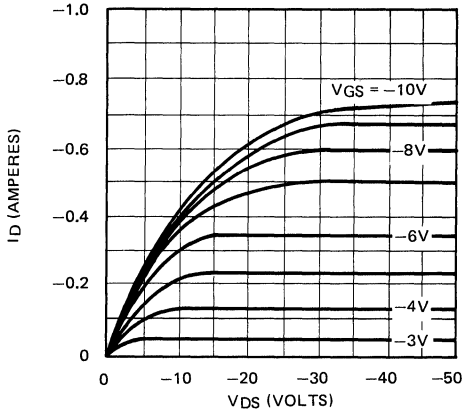
Switching Waveforms and Test Circuit



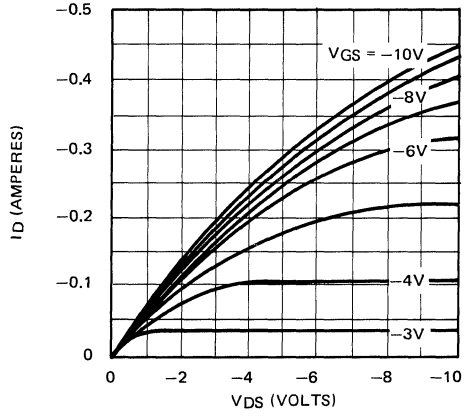


Typical Performance Curves

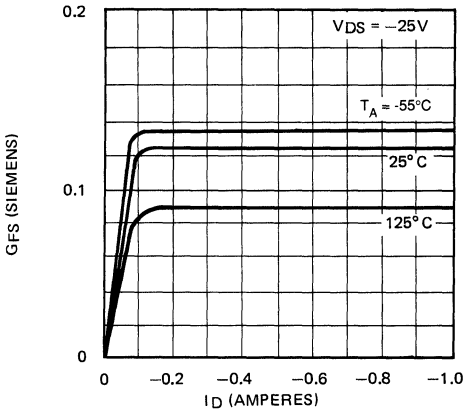
Output Characteristics



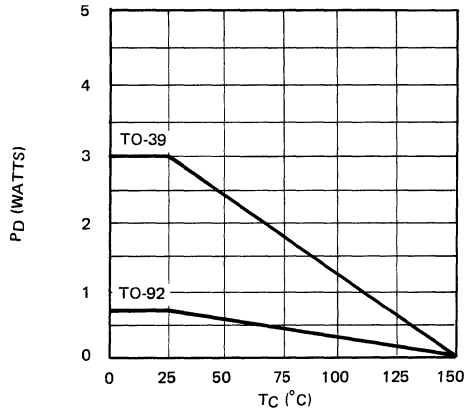
Saturation Characteristics



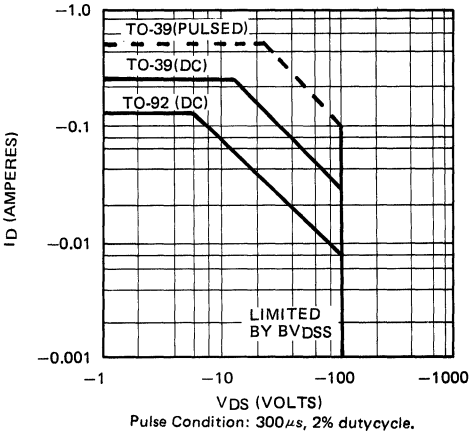
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

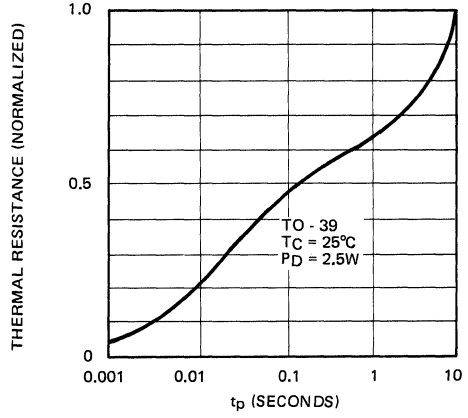


Maximum Rated Safe Operating Area

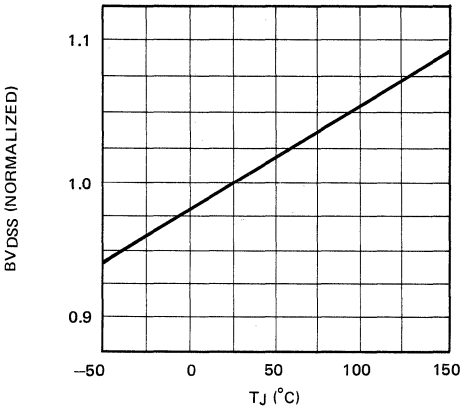


Pulse Condition: 300μs, 2% dutycycle.

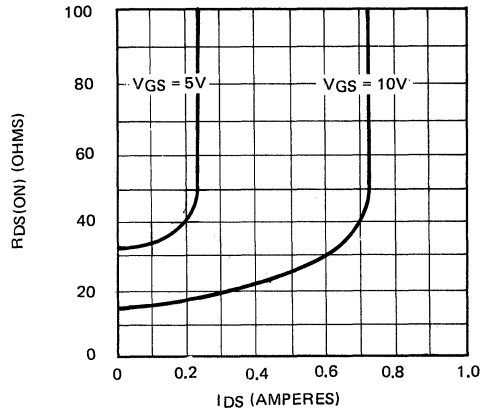
Thermal Response Characteristics



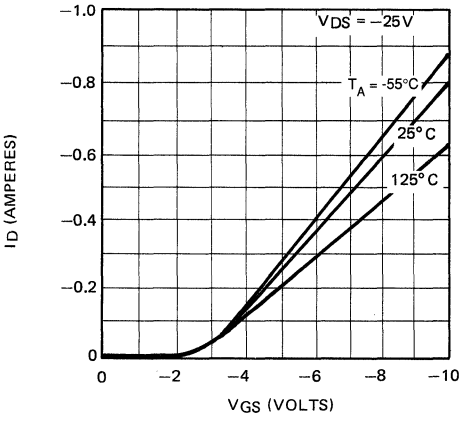
BVDSS Variation with Temperature



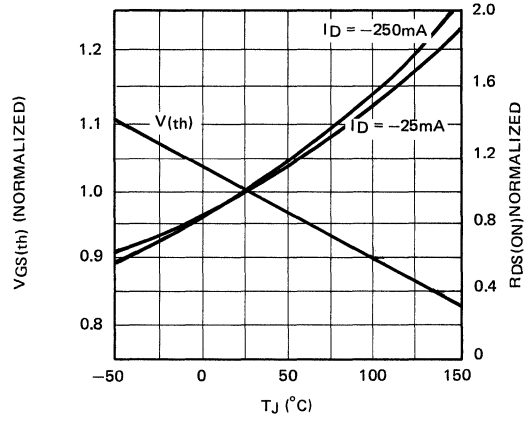
ON - Resistance Vs .Drain Current



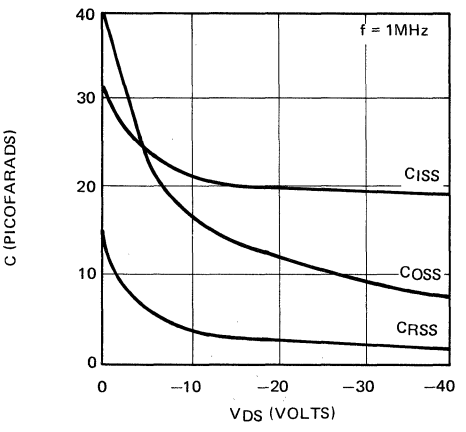
Transfer Characteristics



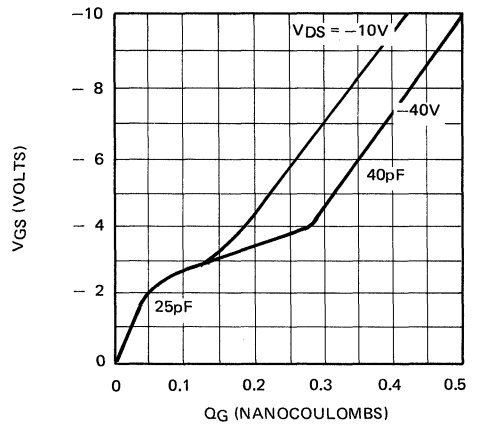
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
-160V	100Ω	-100mA	VP1316N2	VP1316N3
-200V	100Ω	-100mA	VP1320N2	VP1320N3

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Note 1)

TO-39 TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-39	-0.10A	-0.40A	3.0W	125	41	-0.1A	-0.4A
TO-92	-0.06A	-0.30A	0.8W	170	155	-0.06A	-0.3A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

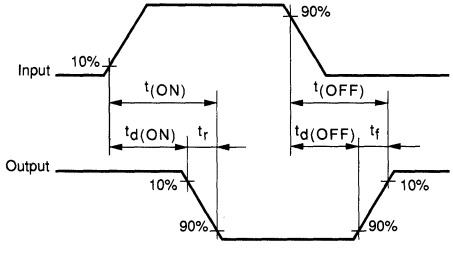
(Notes 1 and 2)

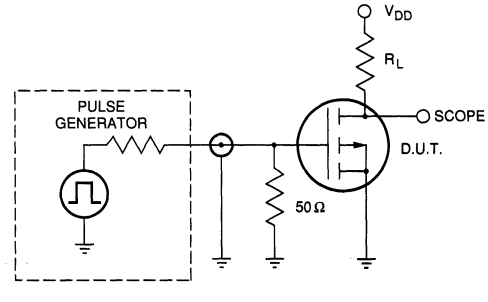
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1320	-200			V	I_D = -1mA, V_{GS} = 0
		VP1316	-160				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	V_{GS} = V_{DS}, I_D = -1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.0	-5.0	mV/°C	V_{GS} = V_{DS}, I_D = -1mA
I_{GSS}	Gate Body Leakage			0.1	100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-500		V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-50	-100		mA	V_{GS} = -5V, V_{DS} = -25V
			-100	-400		mA	V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			65	100	Ω	V_{GS} = -5V, I_D = -40mA
				60	100	Ω	V_{GS} = -10V, I_D = -150mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.6	1.0	%/°C	I_D = -50mA, V_{GS} = -10V
G_{FS}	Forward Transconductance		20	30		m℧	V_{DS} = -25V, I_D = -150A
C_{ISS}	Input Capacitance			35	40	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			10	15		
C_{RSS}	Reverse Transfer Capacitance			2	5		
$t_{d(ON)}$	Turn-ON Delay Time			1.5	5	ns	V_{DD} = -25V, I_D = -200mA, R_S = 50Ω
t_r	Rise Time			2.5	5		
$t_{d(OFF)}$	Turn-OFF Delay Time			1.5	5		
t_f	Fall Time			2.5	5		
V_{SD}	Diode Forward Voltage Drop			1.6	2.0	V	I_{SD} = -1A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			350		ns	I_{SD} = -1A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

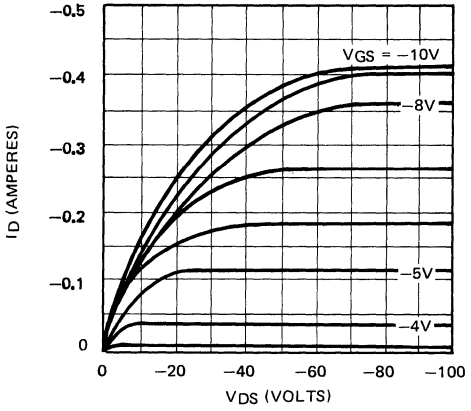
Switching Waveforms and Test Circuit



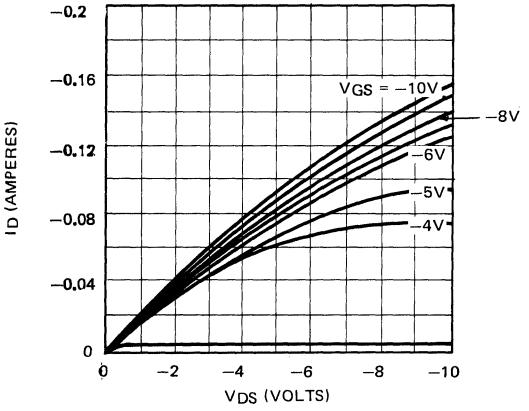


Typical Performance Curves

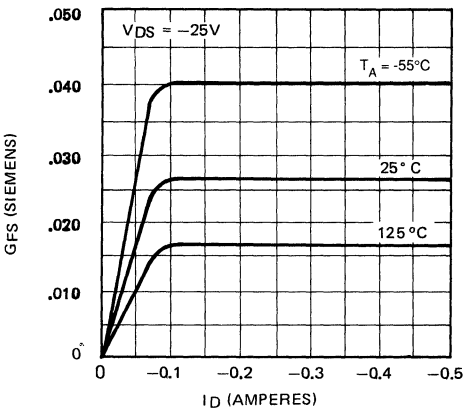
Output Characteristics



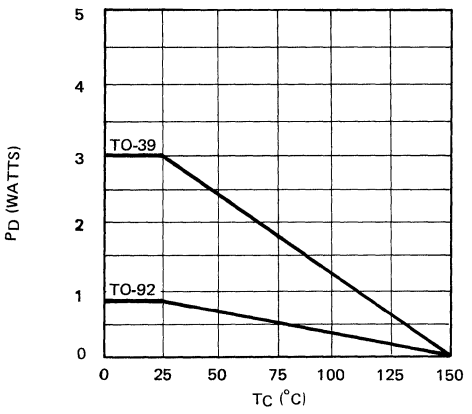
Saturation Characteristics



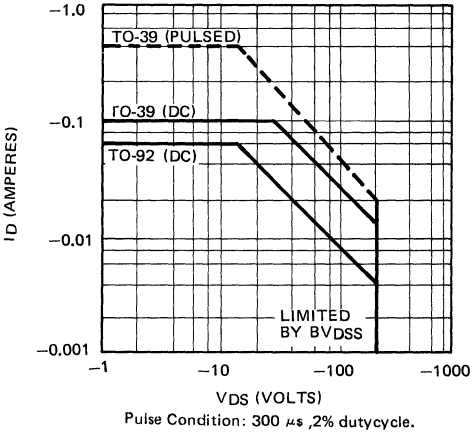
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

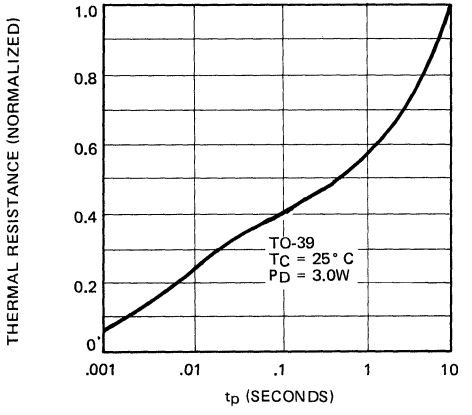


Maximum Rated Safe Operating Area

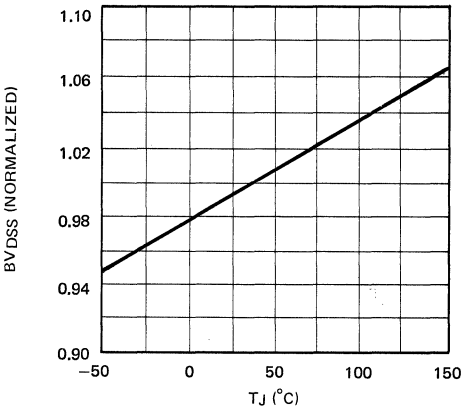


Pulse Condition: 300 μs ,2% dutycycle.

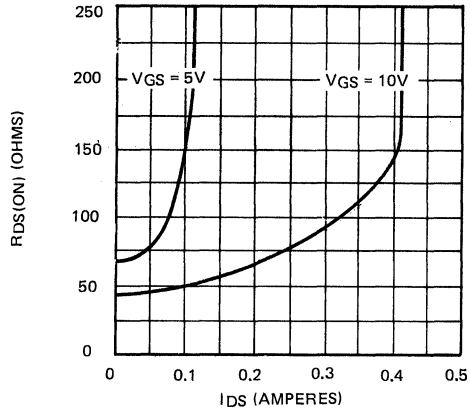
Thermal Response Characteristics



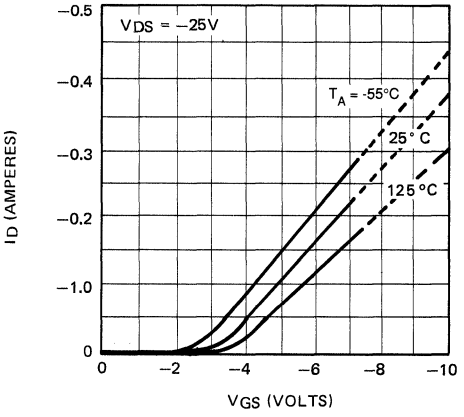
BVDSS Variation with Temperature



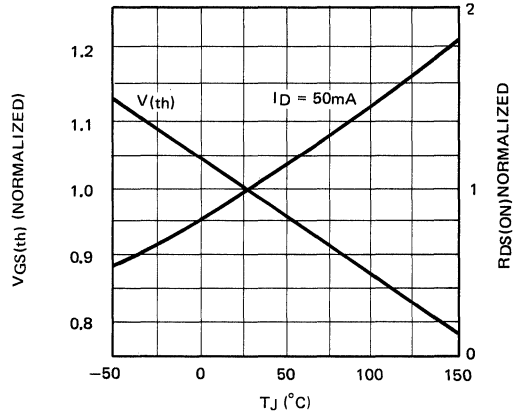
ON- Resistance Vs .Drain Current



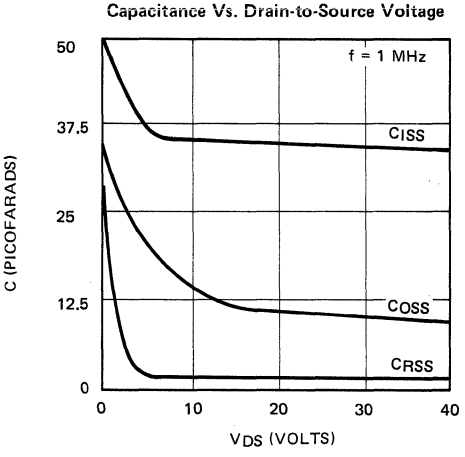
Transfer Characteristics



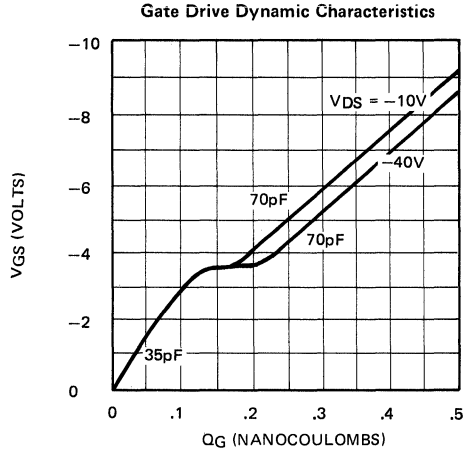
V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

MOSFET Array Selector Guide

Low Voltage N-Channel

Device No.[1]	Number of Channels/Type	BV_{DSS} Min (V)	$R_{DS\ (ON)}$ Max (Ω)	Package Options				
				Plastic Dip	Ceramic Dip	SOW-20	Ceramic LCC	Die
VN0104	4N	40	3	•	•		•	•
VN0106	4N	60	3	•	•			•
VN0204	4N	40	2	•	•			•
VN0206	4N	60	2	•	•			•
TN0604	4N	40	0.75			•		•
TN0606	4N	60	1.5	•	•			•
VN2106	4N	60	3				•	•
VN2110	4N	100	3				•	•
VQ1000	4N	60	5.5	•	•			•
VQ1001	4N	60	1		•			•
VQ1004	4N	60	3.5	•	•			•

Note 1: Excluding package suffix.

Low Voltage P-Channel

Device No.[1]	Number of Channels/Type	BV_{DSS} Min (V)	$R_{DS(ON)}$ Max (Ω)	Package Options				
				Plastic Dip	Ceramic Dip	SOW-20	Ceramic LCC	Die
VP0104	4P	40	8	•	•			•
VP0106	4P	60	8	•	•			•
VP0204	4P	40	4	•	•			•
VP0206	4P	60	4	•	•			•
TP0604	4P	40	2			•		•
TP0606	4P	60	3.5	•	•			•

Note 1: Excluding package suffix.

Low Voltage Complementary

Device No.[1]	Number of Channels/Type	BV_{DSS} Min (V)	$R_{DS\ (ON)}$ Max (Ω)	Package Options				
				Plastic Dip	Ceramic Dip	SOW-20	Ceramic LCC	Die
TC0604	2N + 2P	40	2.75[2]			•		•
VC0106	2N + 2P	60	11.0[2]	•	•			•
VC0206	2N + 2P	60	6.0[2]	•	•			•
TQ3001	2N + 2P	40	3.0[2]	•	•		•	•
VQ3001	2N + 2P	40	3.0[2]	•	•		•	•
VQ7254	2N + 2P	20	3.0[2]	•	•			•

Note 1: Excluding package suffix.
Note 2: One N-channel plus one P-channel.

Supertex inc.

MOSFET Array Selector Guide

High Voltage [2]

Device No.[1]	Number of Channels/Type	BV_{DSS} Min (V)	$R_{DS(ON)}$ Max (Ω)	Package Options				
				Plastic Dip	Ceramic Dip	SOW-20	Ceramic LCC	Die
AN0120	8N	200	300	•	•			•
AN0130	8N	300	300	•	•			•
AN0140	8N	400	350	•	•	•		•
AP0120	8P	200	600	•	•			•
AP0130	8P	300	600	•	•			•
AP0140	8P	400	700	•	•	•		•

Note 1: Excluding package suffix.
Note 2: Monolithic 8 Channel Array.

High Voltage Low Leakage [2,3]

Device No.[1]	Number of Channels/Type	BV_{DSS} Min (V)	$R_{DS(ON)}$ Max (Ω)	Package Options				
				Plastic Dip	Ceramic Dip	SOW-20	Ceramic LCC	Die
AN0116	8N	160	350	•	•	•		•
AN0132	8N	320	350	•	•	•		•
AP0116	8P	160	700	•	•	•		•
AP0132	8P	320	700	•	•	•		•

Note 1: Excluding package suffix.
Note 2: Monolithic 8 Channel Array.
Note 3: Low I_{DSS} Leakage (refer to data sheet for details).

High Voltage Level Translators

Device No.[1]	Number of Channels	V_{PP} Max (V)	I_{SOURCE} Min (mA)	I_{SINK} Min (mA)	Package Options				
					Plastic Dip	Ceramic Dip	SOW-20	Ceramic LCC	Die
HT0130	8	300	0.2	0.1	•	•	•	•	•
HT0240[2]	1	400	300	300	•	•			•

Note 1: Excluding package suffix.
Note 2: Available September 1988.

Supertex inc.

8 Channel Power MOSFET Array
Monolithic N-channel Enchancement Mode

Ordering Information

BV_{DSS}/ BV_{DGS} (min)	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	I_{DSS}** @ V_{DS} = 100V Max	I_{DSS}** @ V_{DS} = 250V Max	Order Number / Package			
					18-Lead Ceramic DIP	18-Lead Plastic DIP	Plastic SOW-20*	Die
160V	350Ω	25mA	1nA	—	AN0116NB	AN0116NA	AN0116WG	AN0116ND
200V	300Ω	25mA	—	—	AN0120NB	AN0120NA	—	AN0120ND
300V	300Ω	25mA	—	—	AN0130NB	AN0130NA	—	AN0130ND
320V	350Ω	25mA	—	1nA	AN0132NB	AN0132NA	AN0132WG	AN0132ND
400V	350Ω	25mA	—	—	AN0140NB	AN0140NA	AN0140WG	AN0140ND

*Same as SO-20 with 300 mil wide body.
**Average current per channel, measured with all eight channels connected in parallel.

Features

- ☐ Low drain to source leakage for AN0116 and AN0132
- ☐ 200-volt to 400-volt capability
- ☐ Interfaces directly to CMOS logic
- ☐ 8 independent channels
- ☐ Low crosstalk between channels
- ☐ Low power dissipation
- ☐ Pin compatible with industry standard driver array
- ☐ Freedom from secondary breakdown

General Description

The Supertex AN01 series of high voltage arrays is designed to provide the interface between MOS logic and loads requiring high voltages and intermediate currents. Each circuit consists of eight channels in a common-source configuration with open drains. This design minimizes the number of package leads needed.

The AN0116 and AN0132 are ideally suited for low leakage/high impedance measurement, providing excellent accuracy and resolution for Automatic Test Equipment.

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Applications

- ☐ High impedance/low leakage measurements for Bare Board Testers
- ☐ High voltage piezoelectric transducer drivers
- ☐ High voltage electroluminescent panel drivers
- ☐ High voltage electrostatic array drivers
- ☐ General multi-channel driver array

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C
Channel-to-Channel Crosstalk	10mV/V

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
18 lead plastic	30mA	75mA	1.5W	135	83	30mA	75mA
18 lead ceramic	40mA	75mA	2.0W	85	62	40mA	75mA

* I_D (continuous) is limited by max rated T_j.

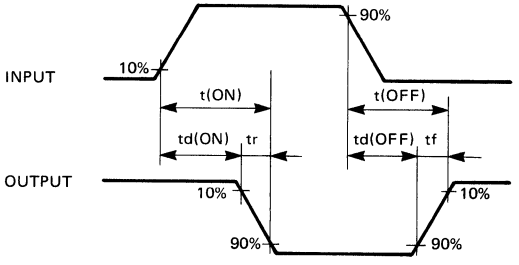
Electrical Characteristics (@ 25°C unless otherwise specified)

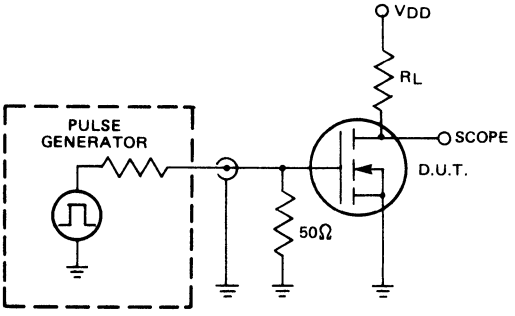
(Notes 1, 2 and 3)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	AN0116 AN0120 AN0130 AN0132 AN0140	160 200 300 320 400			V	I_D = 100μA, V_{GS} = 0V
$V_{GS(th)}$	Gate Threshold Voltage		2		5	V	V_{GS} = V_{DS}, I_D = 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			−3.5		mV/°C	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage	AN0120 AN0130 AN0140			10	nA	V_{GS} = ±20V, V_{DS} = 0
		AN0116 AN0132			1	nA	V_{GS} = ±20V, V_{DS} = 0 (Note 3)
I_{DSS}	Zero Gate Voltage Drain Current	AN0120			1	μA	V_{GS} = 0, V_{DS} = Max Rating
		AN0130 AN0140			1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
		AN0116			1	nA	V_{GS} = 0, V_{DS} = 100V (Note 3)
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
		AN0132			1	nA	V_{GS} = 0, V_{DS} = 250V (Note 3)
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		25			mA	V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	AN0120 AN0130			300	Ω	V_{GS} = 10V, I_D = 10mA
		AN0116 AN0132 AN0140			350	Ω	V_{GS} = 10V, I_D = 10mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.8		%/°C	V_{GS} = 10V, I_D = 10mA
G_{FS}	Forward Transconductance		4.0	8.0		m℧	I_D = 10mA, ΔV_{GS} = 1V
C_{ISS}	Input Capacitance			5.0	7.5	pF	V_{DS} = 25V, V_{GS} = 0 f = 1 MHz
C_{OSS}	Common Source Output Capacitance			3.0	5.0		
C_{RSS}	Reverse Transfer Capacitance			0.8	1.5		
$t_{d(ON)}$	Turn-ON Delay Time			3		ns	V_{DS} = 25V I_D = 10mA 50Ω drive, $V_{GS(ON)}$ = 10V
t_r	Rise Time			3			
$t_{d(OFF)}$	Turn-OFF Delay Time			5			
t_f	Fall Time			3			
V_{SD}	Diode Forward Voltage Drop				1.3	V	V_{GS} = 0, I_{SD} = 50mA

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.
Note 3: Average current per channel, measured with all 8 channels connected in parallel.

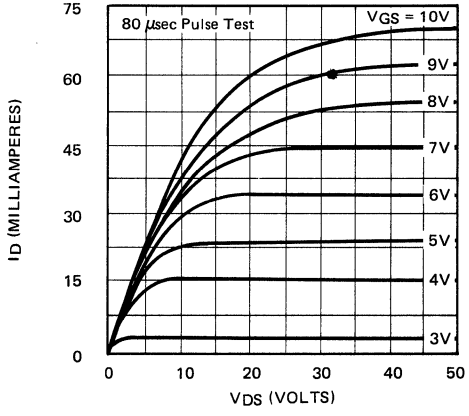
Switching Waveforms and Test Circuit



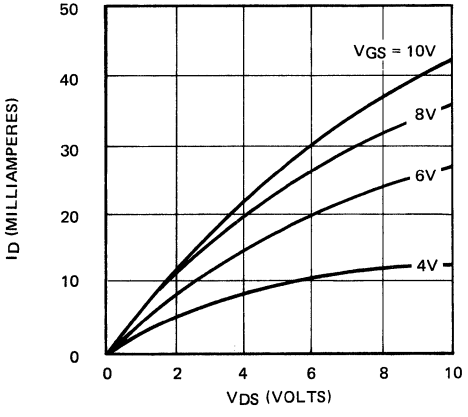


Typical Performance Curves

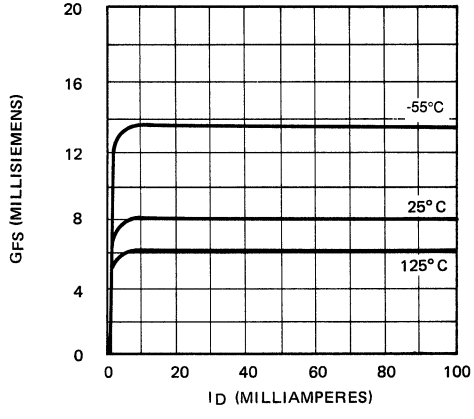
Output Characteristics



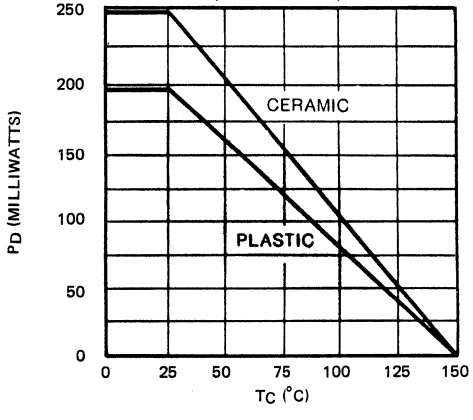
Saturation Characteristics



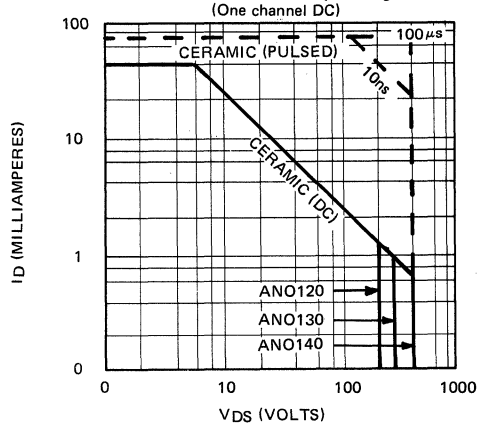
Transconductance Vs. Drain Current



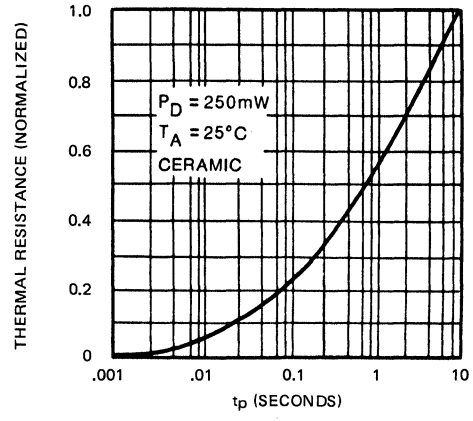
Power Dissipation Vs. Case Temperature
(For one channel)



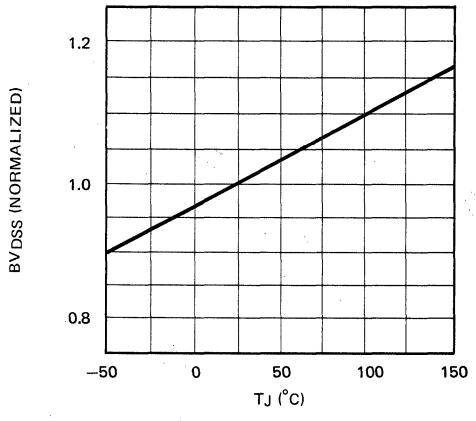
Maximum Rated Safe Operating Area
(One channel DC)



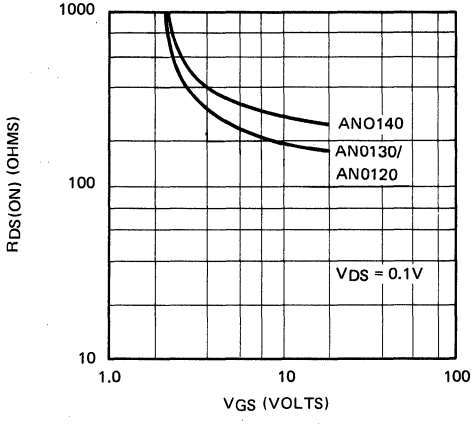
Thermal Response Characteristics



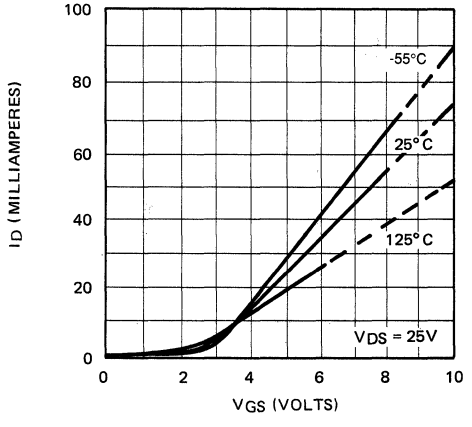
BVDSS Variation with Temperature



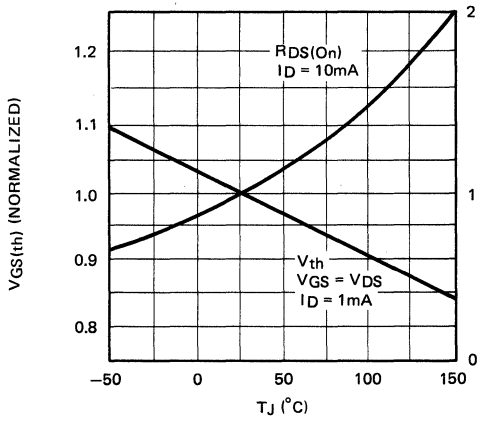
ON-Resistance Vs. Gate-to-Source Voltage



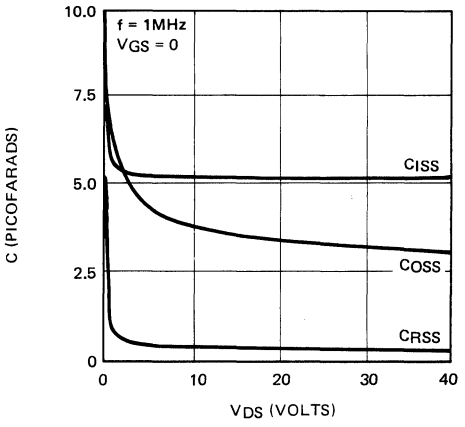
Transfer Characteristics



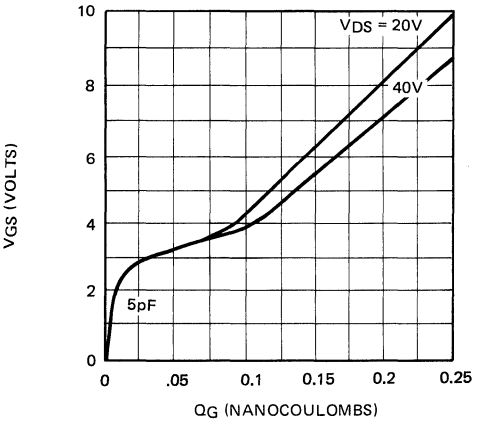
V(th) and RDS Variation with Temperature



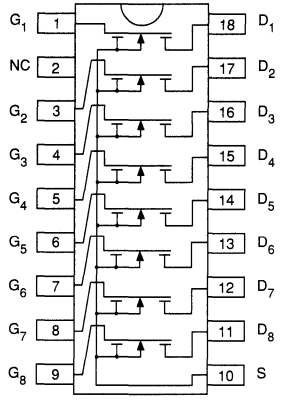
Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

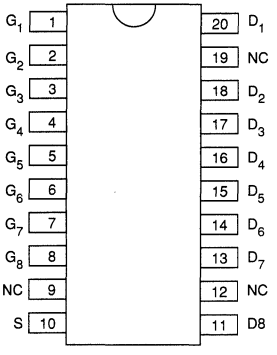


Pin Configuration and Schematic



top view

18-pin DIP



top view

SOW-20

8 Channel Power MOSFET Array
Monolithic P-channel Enchancement Mode

Ordering Information

BV_{DSS}/ BV_{DGS} (min)	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	I_{DSS}** @ V_{DS} = -100V Max	I_{DSS}** @ V_{DS} = -250V Max	Order Number / Package			
					18-Lead Ceramic DIP	18-Lead Plastic DIP	Plastic SOW-20*	Die
-160V	700Ω	-15mA	-1.5nA	—	AP0116NB	AP0116NA	AP0116WG	AP0116ND
-200V	600Ω	-15mA	—	—	AP0120NB	AP0120NA	—	AP0120ND
-300V	600Ω	-15mA	—	—	AP0130NB	AP0130NA	—	AP0130ND
-320V	700Ω	-15mA	—	-1.5nA	AP0132NB	AP0132NA	AP0132WG	AP0132ND
-400V	700Ω	-15mA	—	—	AP0140NB	AP0140NA	AP0140WG	AP0140ND

*Same as SO-20 with 300 mil wide body.
**Average current per channel, measured with all eight channels connected in parallel.

Features

- ☐ Low drain to source leakage for AP0116 and AP0132
- ☐ 200-volt to 400-volt capability
- ☐ Interfaces directly to CMOS logic
- ☐ 8 independent channels
- ☐ Low crosstalk between channels
- ☐ Low power dissipation
- ☐ Pin compatible with industry standard driver array
- ☐ Freedom from secondary breakdown

General Description

The Supertex AP01 series of high voltage arrays is designed to provide the interface between MOS logic and loads requiring high voltages and intermediate currents. Each circuit consists of eight channels in a common-source configuration with open drains. This design minimizes the number of package leads needed.

The AP0116 and AP0132 are ideally suited for low leakage/high impedance measurement, providing excellent accuracy and resolution for Automatic Test Equipment.

Applications

- ☐ High voltage electroluminescent panel drivers
- ☐ High voltage electrostatic array drivers
- ☐ General multi-channel driver array

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C
Channel-to-Channel Crosstalk	10mV/V

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
18 lead plastic	−15mA	−40mA	1.5W	135	83	−15mA	−40mA
18 lead Ceramic	−15mA	−40mA	2.0W	85	62	−15mA	−40mA

* I_D (continuous) is limited by max rated T_j.

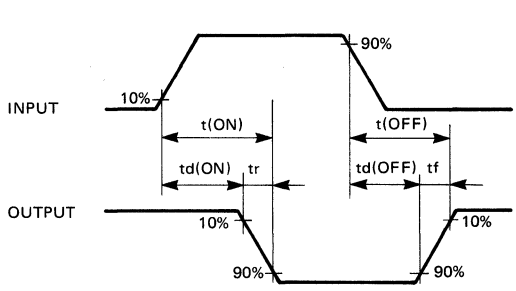
Electrical Characteristics (@ 25°C unless otherwise specified)

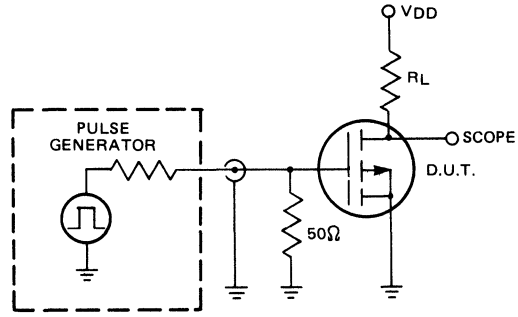
(Notes 1, 2 and 3)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	AP0116 AP0120 AP0130 AP0132 AP0140	−160 −200 −300 −320 −400			V	I_D = −100μA, V_{GS} = 0V
$V_{GS(th)}$	Gate Threshold Voltage		−2		−5	V	V_{GS} = V_{DS}, I_D = −1mA
$\triangle V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			−3.5		mV/°C	V_{GS} = V_{DS}, I_D = −1mA
I_{GSS}	Gate Body Leakage	AP0120 AP0130 AP0140			−10	nA	V_{GS} = ±20V, V_{DS} = 0
		AP0116 AP0132			−1	nA	V_{GS} = ±20V, V_{DS} = 0 (Note 3)
I_{DSS}	Zero Gate Voltage Drain Current	AP0120			−1	μA	V_{GS} = 0, V_{DS} = Max Rating
		AP0130 AP0140			−1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125 °C
		AP0116			−1.5	nA	V_{GS} = 0, V_{DS} = −100V (Note 3)
					−1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125 °C
		AP0132			−1.5	nA	V_{GS} = 0, V_{DS} = −250V (Note 3)
					−1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125 °C
$I_{D(ON)}$	ON-State Drain Current		−15			mA	V_{GS} = −10V, V_{DS} = −25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	AP0120 AP0130			600	Ω	V_{GS} = −10V, I_D = −10mA
		AP0116 AP0132 AP0140			700	Ω	V_{GS} = −10V, I_D = −10mA
$\triangle R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.8		%/°C	V_{GS} = −10V, I_D = −10mA
G_{FS}	Forward Transconductance		3.0	5.0		m℧	V_{DS} = −25V, I_D = −5mA
C_{ISS}	Input Capacitance			5.0	7.5	pF	V_{DS} = −25V, V_{GS} = 0 f = 1 MHz
C_{OSS}	Common Source Output Capacitance			3.0	5.0		
C_{RSS}	Reverse Transfer Capacitance			1.0	2.0		
$t_{d(ON)}$	Turn-ON Delay Time			3		ns	V_{DS} = −25V I_D = −10mA R_S = 50Ω, $V_{GS(ON)}$ = −10V
t_r	Rise Time			3			
$t_{d(OFF)}$	Turn-OFF Delay Time			5			
t_f	Fall Time			3			
V_{SD}	Diode Forward Voltage Drop				1.5	V	V_{GS} = 0, I_{SD} = −25mA

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.
Note 3: Average current per channel, measured with all 8 channels connected in parallel.

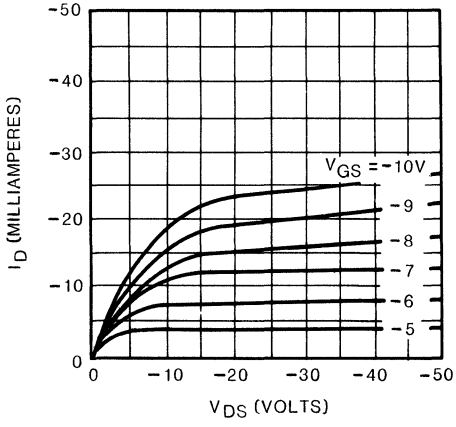
Switching Waveforms and Test Circuit



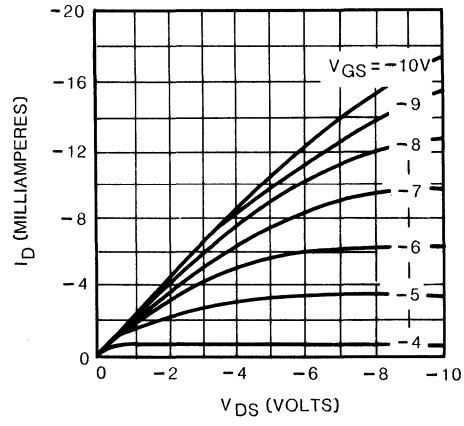


Typical Performance Curves

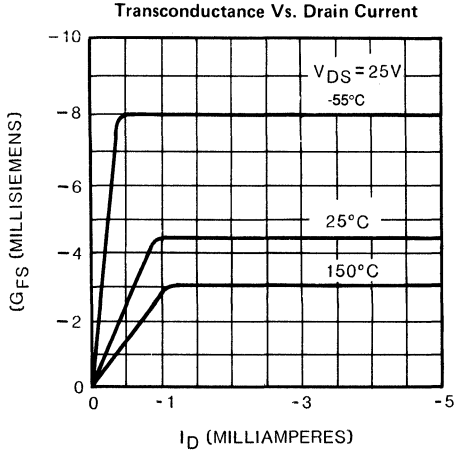
Output Characteristics



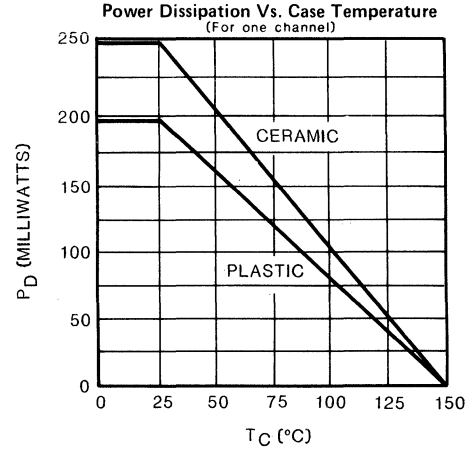
Saturation Characteristics



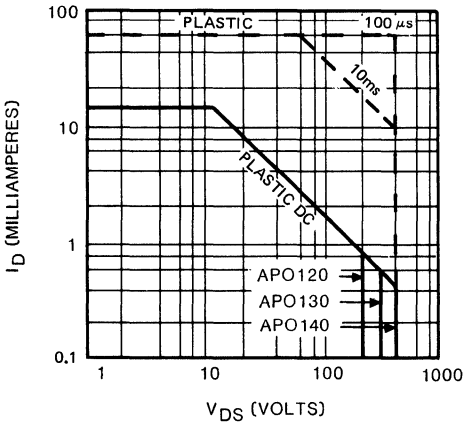
Transconductance Vs. Drain Current



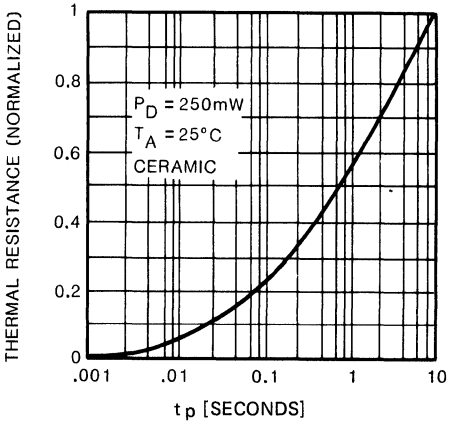
Power Dissipation Vs. Case Temperature
(For one channel)



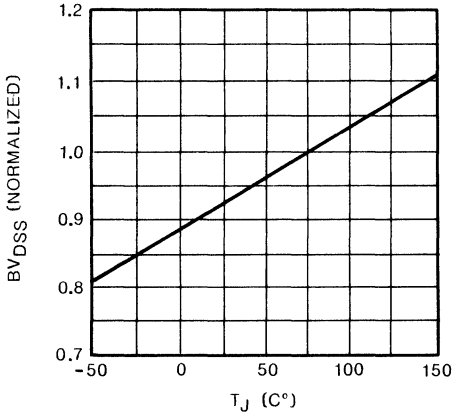
Maximum Rated Safe Operating Area



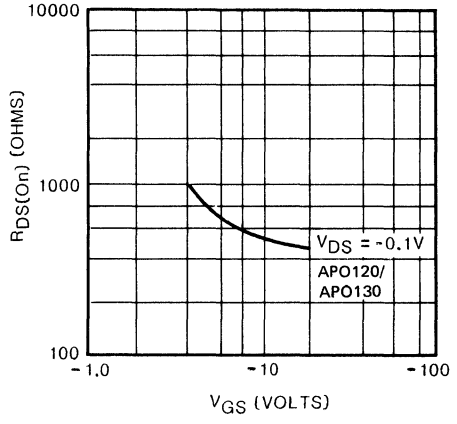
Thermal Response Characteristics



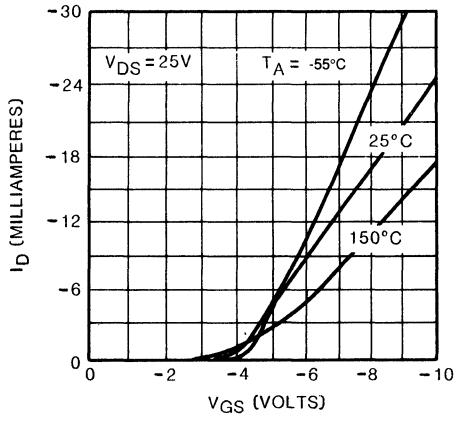
BV_{DSS} Variation with Temperature



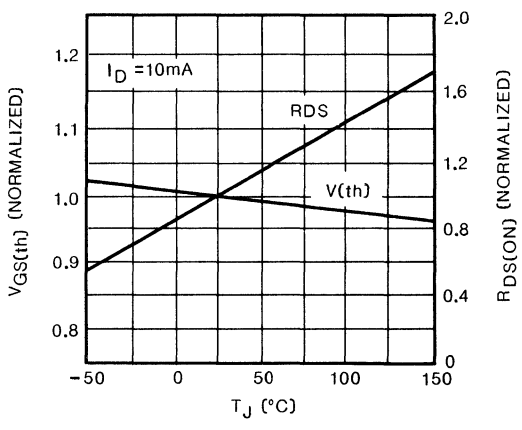
ON-Resistance Vs. Gate-to-Source Voltage



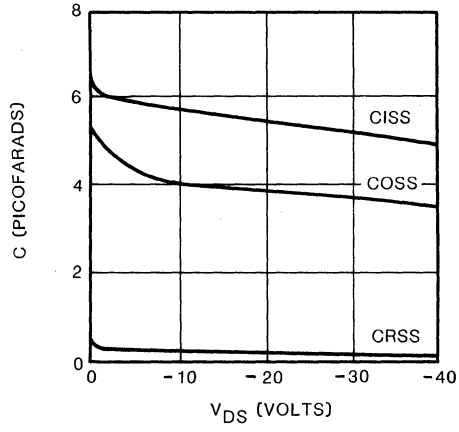
Transfer Characteristics



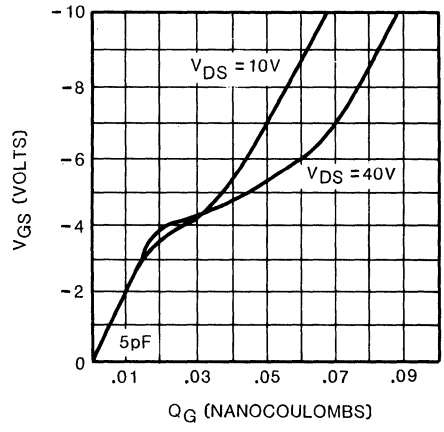
V(th) and RDS Variation with Temperature



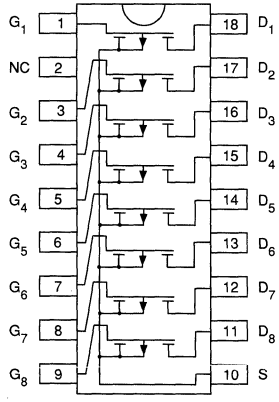
Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

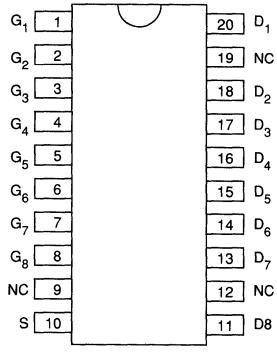


Pin Configuration and Schematic



top view

18-pin DIP



top view

SOW-20

8-Channel Logic To High-Voltage Level Translator

Ordering Information

Part Number/Package				
20 Lead CERDIP	**20 Lead Plastic DIP**	**20 Terminal Ceramic LCC**	**Plastic SOW-20***	**Die in waffle pack**
HT0130D	HT0130P	HT0130LC	HT0130WG	HT0130X

*Same as SO-20 0.300 mil wide body.

Features

- ☐ Operating voltage up to 300V
- ☐ 5V to 15V logic input capability
- ☐ Output swings below GND if required
- ☐ Drives high-voltage P-Channel MOS from logic level signal
- ☐ Surface mount packaging available
- ☐ No "floating logic" required
- ☐ 8 independent channels

Applications

- ☐ ATE systems
- ☐ Printers/plotters
- ☐ P-Channel MOSFET control

Absolute Maximum Ratings[1,2]

Supply voltage, V_{DD}		V_{NN} - 0.3V to +16V
Supply Voltage, V_{PP}		V_{NN} - 0.3V to + 300V
Supply Voltage, V_{NN}		-16V to 0.3V
Logic inputs levels	V_{IN}	V_{NN} - 0.3V to V_{DD} + 0.3V
	V_{OUTPUT}	V_{PP} + 0.3V max
I_{OUT} — DC per Channel		30mA
Continuous total power dissipation[2]		700mW
Operating temperature range		0°C to 70°C
Storage temperature range		-65°C to + 150°C

Note 1: All voltages are referenced to chip ground.

Note 2: For operation above 25°C ambient derate lineraly to 85°C at 8mW/°C.

General Description

The Supertex HT01 8-channel Level Translator is designed to implement the necessary level translation between logic level signals and voltage swings required to drive high-voltage P-Channel MOSFET transistors. This device is intended to provide gate drive signals to devices such as the Supertex AP01 P-Channel MOSFET Array in applications requiring active pull-up to a high-voltage (V_{PP}) line of up to 300 volts. Logic input can be from 5 volts to 15 volts and is referenced to the logic supply (V_{DD}).

When an input is switched to 4.2 volts below the V_{DD} supply, the corresponding output will typically switch from V_{PP} to V_{PP} -14 volts. If the V_{PP} supply remains above 12 volts, the negative supply (V_{NN}) would be connected to system ground (GND). If variations of the V_{PP} supply level require the P-Channel MOSFET gate drive to swing below GND in order to turn on, connect the V_{NN} pin to a negative supply of up to -15 volts. The logic inputs can remain between V_{DD} and system ground (GND) and still provide correct operation.

In an OFF condition, the HT01 is a low power device. In an ON condition, each channel will dissipate power determined by the V_{PP} and V_{NN}voltage. Internal power dissipation must be considered when the application requires that more than one channel be active at one time, especially at higher V_{PP} voltage values.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current			0.001	mA	All OFF
			0.6	3.50	mA	1 ch ON, no load
I_{PP}	V_{PP} Supply Current			0.001	mA	All OFF
			0.4	1.0	mA	1 ch ON, no load
I_{NN}	V_{NN} Supply Current			0.001	mA	All OFF
			1.0	4.50	mA	1 ch ON, no load
I_{SOURCE}	Output current	135	200		µA	Capacitive load
I_{SINK}	Output current	66	100		µA	Capacitive load
V_{ON}	Output voltage	V_{PP} - 17		V_{PP} - 10	V	V_{DD} = 4.75V
		V_{PP} - 17		V_{PP} - 12.5	V	V_{DD} = 15V
V_{OFF}	Output voltage	V_{PP} - 0.5			V	
V_Z	Zener voltage	11	14	17	V	Output to V_{PP}

AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{ON}	Turn on time, any channel		5		µs	V_{DD} = 10V, V_{NN} = GND
Δt_{ON}	Variation in t_{ON}, any 2 channels		5		%	V_{DD} = 10V, V_{NN} = GND
t_{OFF}	Turn off time, any channel		3		µs	V_{DD} = 10V, V_{NN} = GND
Δt_{OFF}	Variation in t_{OFF}, any 2 channels		5		%	V_{DD} = 10V, V_{NN} = GND

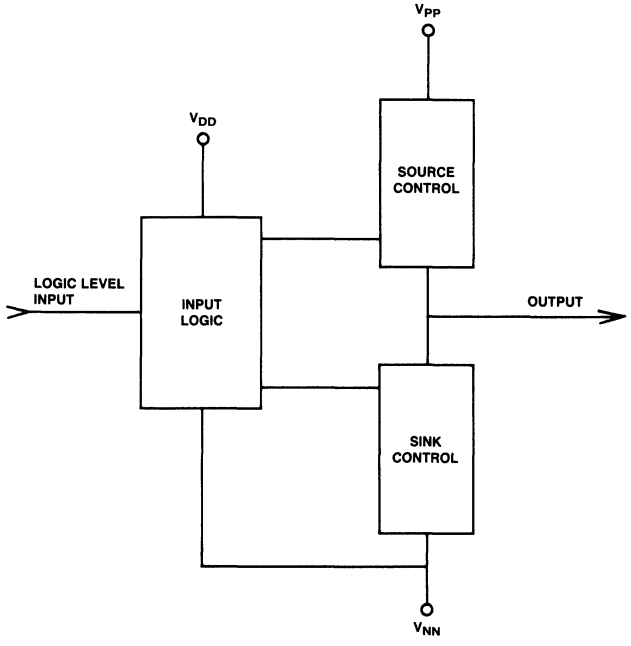
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	4.75		15	V
V_{PP}	Positive high voltage supply	V_{NN} + 12		275	V
V_{NN}	Negative supply	-15		0	V
V_{IH}	High-level input voltage	V_{DD} - 1.2		V_{DD}	V
V_{IL}	Low-level input voltage	0		V_{DD} - 4.2	V
T_A	Operating free-air temperature	0		+70	°C

Function Table

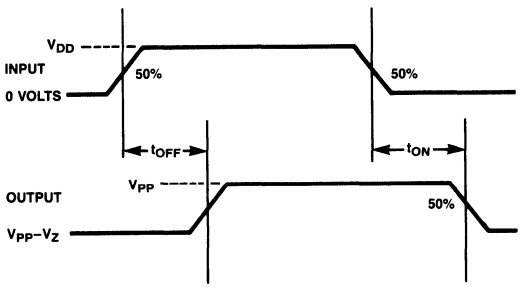
Input Condition	Output Stage
High level	V_{PP}
Low level	V_{PP} - V_Z

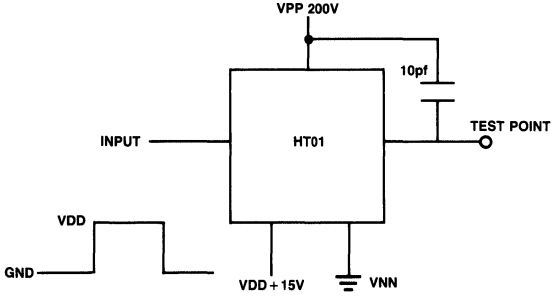
Functional Block Diagram



(One of eight channels within the HT01)

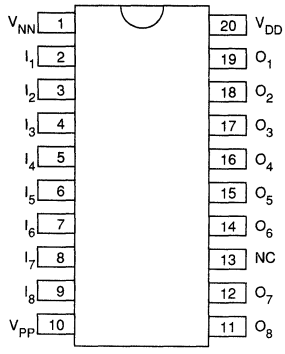
Switching Waveforms and Test Circuit





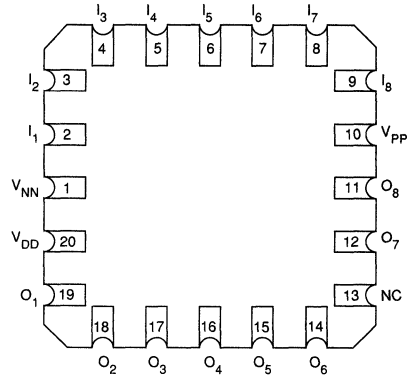
(One of eight channels within the HT01)

Pin Configuration



top view

20-pin DIP/SOW-20



bottom view

20-pin LCC

Preliminary

Complementary Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ Max $Q_1 + Q_2$ or $Q_3 + Q_4$	Order Number / Package SOW-20*
40V	2.75Ω	TC0604WG

*Same as SO-20 with 300 mil wide body.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and Military versions available
- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Thermal Characteristics

Package		Plastic SOW-20
I_D continuous & I_{DR} (single die)	N-Channel	1.0A
	P-Channel	0.6A
I_D pulsed* & I_{DRM}*	N-Channel	4.0A
	P-Channel	2.0A
Power Dissipation @ T_C = 25°C‡		1.5W
θ_{ja} (°C/W)		85
θ_{jc} (°C/W)		—

* Pulse test 300 μS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

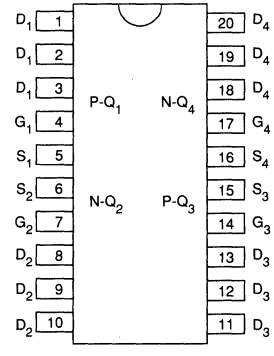
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to TN06L and TP06L Data Sheets for detailed characteristics of N- and P-channel devices.

10

Pin Configuration



top view

SOW-20

Preliminary

N-Channel Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ Max	Order Number / Package
		SOW-20*
40V	0.75Ω	TN0604WG

*Same as SO-20 with 300 mil wide body.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and Military versions available
- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Thermal Characteristics

Package	Plastic SOW-20
I_D continuous & I_{DR} (single die)	1.0A
I_D pulsed+ & I_{DRM}+	4.0A
Power Dissipation @ T_C = 25°C‡	1.5W
θ_{ja} (°C/W)	85
θ_{jc} (°C/W)	—

+ Pulse test 300 µS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

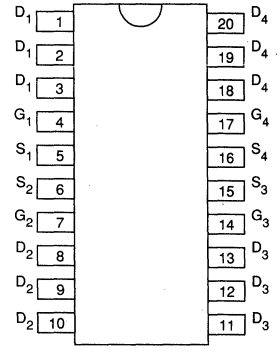
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to TN06L Data Sheet for detailed characteristics.

Pin Configuration



top view

SOW-20

N-Channel Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	Order Number / Package	
		14-Pin P-Dip	14-Pin C-Dip*
60V	1.5Ω	TN0606N6	TN0606N7

*14-pin Side Brazed Ceramic Dip.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and Military versions available
- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Thermal Characteristics

Package	Plastic DIP	Ceramic DIP
I_D continuous & I_{DR} (single die)	1.4A	1.60A
I_D pulsed* & I_{DRM}*	6.0A	6.0A
Power Dissipation @ T_C = 25°C‡	3W	4W
θ_{ja} (°C/W)	83.3	62.5
θ_{jc} (°C/W)	41.6	31.2

* Pulse test 300 µS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

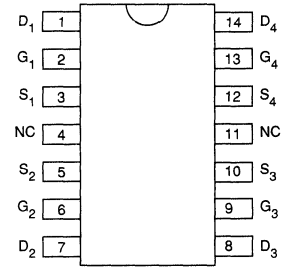
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to TN06A Data Sheet for detailed characteristics.

Pin Configuration



top view

14-pin DIP

Preliminary

P-Channel Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ Max	Order Number / Package
		SOW-20*
-40V	2.0Ω	TP0604WG

*Same as SO-20 with 300 mil wide body.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and Military versions available
- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Thermal Characteristics

Package	Plastic SOW-20
I_D continuous & I_{DR} (single die)	2.0A
I_D pulsed* & I_{DRM}*	0.6A
Power Dissipation @ T_C = 25°C‡	1.5W
θ_{ja} (°C/W)	85
θ_{jc} (°C/W)	—

* Pulse test 300 μS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

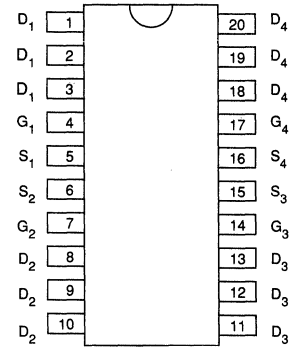
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to TP06L Data Sheet for detailed characteristics.

Pin Configuration



top view

SOW-20

P-Channel Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	Order Number / Package	
		14-Pin P-Dip	14-Pin C-Dip*
-60V	3.5Ω	TP0606N6	TP0606N7

*14-pin Side Brazed Ceramic Dip.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and Military versions available
- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Thermal Characteristics

Package	Plastic DIP	Ceramic DIP
I_D continuous & I_{DR} (single die)	0.65A	0.75A
I_D pulsed* & I_{DRM}*	3.5A	3.5A
Power Dissipation @ T_C = 25°C‡	3W	4W
θ_{ja} (°C/W)	83.3	62.5
θ_{jc} (°C/W)	41.6	31.2

* Pulse test 300 μS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

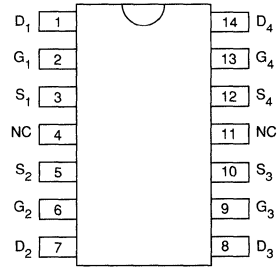
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to TP06A Data Sheet for detailed characteristics.

10

Pin Configuration



top view

14-pin DIP

N- and P-Channel Quad Power MOSFET Arrays

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max) Q1 + Q2 or Q3 + Q4	$V_{GS(th)}$ (max)		Order Number / Package		
		N-Channel	P-Channel	14-Pin P-Dip	14-Pin C-Dip	20 Terminal LCC Quad
40V	3Ω	2.0V	3.0V	VQ3001N6	VQ3001N7	VQ3001NF
40V	3Ω	1.6V	2.4V	TQ3001N6	TQ3001N7	TQ3001NF
20V	3Ω	2.0V	3.0V	VQ7254N6	VQ7254N7	—

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices
- ☐ Low Threshold version available

Applications

- ☐ Bubble/Memory drivers
- ☐ General purpose complementary drivers and switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Thermal Characteristics

Package	I_D (continuous)*		I_D (pulsed)*		Power Dissipation	θ_{ja}	θ_{jc}	I_{DR}		I_{DRM}*	
	N	P	N	P	@ T_C = 25°C	°C/W	°C/W	N	P	N	P
Ceramic Dip	850mA	-600mA	3.0A	3.0A	2.0†	—	62.5	850mA	-600mA	3.0A	-3.0A
Plastic Dip	640mA	-450mA	3.0A	3.0A	1.5†	—	83.3	640mA	-450mA	3.0A	-3.0A
20 Terminal LCC	410mA	-300mA	3.0A	3.0A	1.0†	—	125.0	410mA	-300mA	3.0A	-3.0A

*Total for 4 die. †Each die.

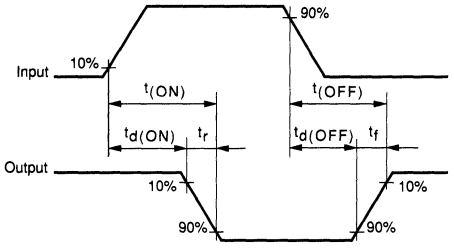
Electrical Characteristics (@ 25°C unless otherwise specified)

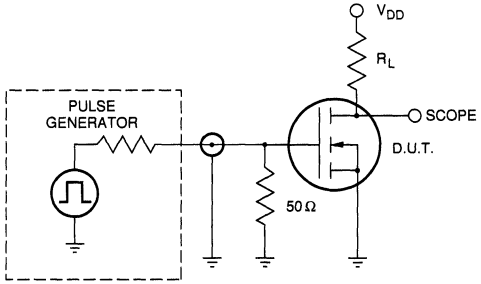
(Notes 1, 2, and 3)

Symbol	Parameter		N-Channel Min	N-Channel Max	P-Channel Min	P-Channel Max	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TQ3001 VQ3001	40		-40		V	V_{GS} = 0, I_D = 10μA
		VQ7254	20		-20			
$V_{GS(th)}$	Gate Threshold Voltage	VQ3001 VQ7254	0.8	2.0	-0.8	-3.0	V	V_{GS} = V_{DS}, I_D = 1mA T_A = 25°C
		TQ3001	0.6	1.6	-1.0	-2.4	V	
		VQ3001 VQ7254	0.5		-0.65		V	V_{GS} = V_{DS}, I_D = 1mA T_A = 85°C
I_{GSS}	Gate Body Leakage			100		-100	nA	V_{GS} =16V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			0.5		-0.5	μA	V_{GS} = 0, V_{DS} = 0.8 Min Rating
$V_{DS(ON)}$	Total Static Drain-to-Source ON-State Resistance Q_1 + Q_2 or Q_3 + Q_4	VQ3001 TQ3001		3.0		3.0	V	V_{GS} = 11.4V, I_D = 1A
		VQ7254	2.0	3.0	2.0	3.0		
$R_{DS(ON)}$	Total Static Drain-to-Source ON-State Resistance Q_1 + Q_2 or Q_3 + Q_4	TQ3001		5.0		5.0	Ω	V_{GS} = 5.0V, I_D = 250mA
		VQ3001 TQ3001		3.0		3.0		V_{GS} = 11.4V, I_D = 1A
		VQ7254	2.0	3.0	2.0	3.0		
G_{FS}	Forward Transconductance		200		200		m℧	V_{DS} ≥ 2$V_{DS(ON)}$, I_D = 0.5A
C_{ISS}	Input Capacitance			175		195	pF	V_{GS} = 0, V_{DS} = 12V f = 1Mz
C_{OSS}	Output Capacitance			95		100		
C_{RSS}	Reverse Transfer Capacitance			25		60		
$t_{d(ON)}$	Turn-ON Delay Time			30		30	ns	V_{DD} = 17V, R_S = 50Ω
$t_{d(OFF)}$	Turn-OFF Delay Time			30		30	ns	R_L = 15Ω
V_{SD}	Forward ON Voltage	VQ7254		-0.75		0.75	V	V_{GS} = 0, I_F = 50mA
				-1.20		1.2		V_{GS} = 0, I_F = 1A

Note 1: All D.C. parameters 100% tested (pulse test: 300μs pulse, 2% duty cycle).
Note 2: All A.C. parameters sample tested.
Note 3: Refer to device types TN06L and TP06L for characteristic curves.

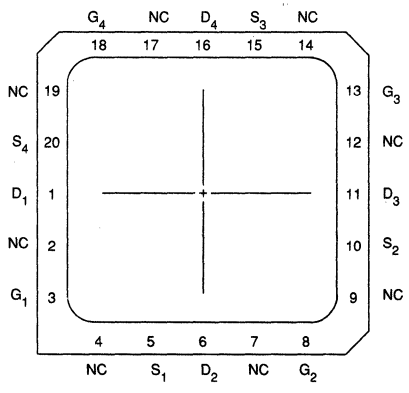
Switching Waveforms and Test Circuit





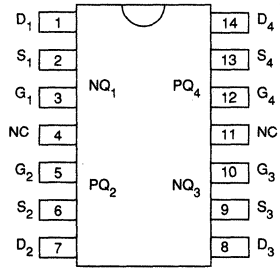
FET polarity in test circuit is N-channel only.

Pin Configuration and Schematic



top view

20-pin Ceramic LCC



top view

14-pin DIP

Complementary Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max) Q1 + Q2 or Q3 + Q4	Order Number / Package	
		14-Pin P-Dip	14-Pin C-Dip*
60V	11Ω	VC0106N6	VC0106N7

*14-pin Side Brazed Ceramic Dip.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and Military versions available
- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Thermal Characteristics

Package		Plastic DIP	Ceramic DIP
I_D continuous & I_{DR} (single die)	N-Channel	0.56A	0.7A
	P-Channel	0.35A	0.4A
I_D pulsed* & I_{DRM}*	N-Channel	2.0A	2.0A
	P-Channel	1.0A	1.0A
Power Dissipation @ T_C = 25°C‡		2W	3W
θ_{ja} (°C/W)		110	83.3
θ_{jc} (°C/W)		62.5	41.6

* Pulse test 300 μS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

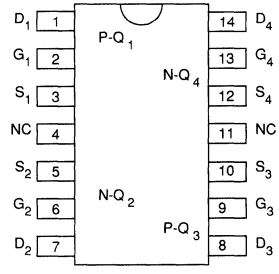
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to VN01A and VP01A Data Sheets for detailed characteristics of N- and P-Channel devices.

10

Pin Configuration



top view

14-pin DIP

Complementary Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max) Q1 + Q2 or Q3 + Q4	Order Number / Package	
		14-Pin P-Dip	14-Pin C-Dip*
60V	6Ω	VC0206N6	VC0206N7

*14-pin Side Brazed Ceramic Dip.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and Military versions available
- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Thermal Characteristics

Package		Plastic DIP	Ceramic DIP
I_D continuous & I_{DR} (single die)	N-Channel	0.86A	1.0A
	P-Channel	0.6A	0.7A
I_D pulsed† & I_{DRM}†	N-Channel	4.0A	4.0A
	P-Channel	2.5A	2.5A
Power Dissipation @ T_C = 25°C‡		3W	4W
θ_{ja} (°C/W)		83.3	62.5
θ_{jc} (°C/W)		41.6	31.2

† Pulse test 300 μS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

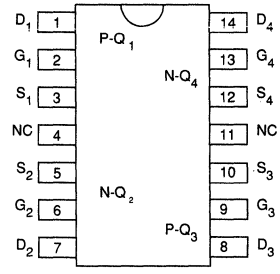
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to VN02A and VP02A Data Sheets for detailed characteristics of N- and P-Channel devices.

Pin Configuration



top view

14-pin DIP

N-Channel Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	Order Number / Package	
		14-Pin P-Dip	14-Pin C-Dip*
40V	3Ω	VN0104N6	VN0104N7
60V	3Ω	VN0106N6	VN0106N7

*14-pin Side Brazed Ceramic Dip.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and Military versions available
- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Thermal Characteristics

Package	Plastic DIP	Ceramic DIP
I_D continuous & I_{DR} (single die)	0.56A	0.7A
I_D pulsed* & I_{DRM}*	2.0A	2.0A
Power Dissipation @ T_C = 25°C‡	2W	3W
θ_{ja} (°C/W)	110	83.3
θ_{jc} (°C/W)	62.5	41.6

* Pulse test 300 µS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

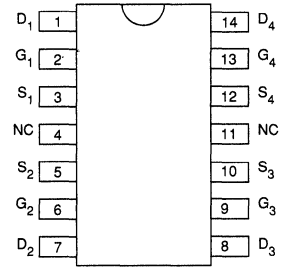
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to VN01A Data Sheet for detailed characteristics.

10

Pin Configuration



top view

14-pin DIP

N-Channel Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ Max	Order Number / Package
		16 Terminal Ceramic LCC
60V	3Ω	VN0106NE
90V	3Ω	VN0109NE

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and Military versions available
- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Thermal Characteristics

Package	Ceramic LCC
I_D continuous & I_{DR} (single die)	0.32A
I_D pulsed* & I_{DRM}*	1.75A
Power Dissipation @ T_C = 25°C‡	0.6W
θ_{ja} (°C/W)	275
θ_{jc} (°C/W)	208

* Pulse test 300 μS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

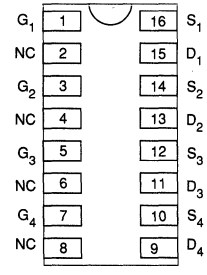
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to VN01A Data Sheet for detailed characteristics.

Pin Configuration



top view

16-pin LCC

N-Channel Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	Order Number / Package	
		14-Pin P-Dip	14-Pin C-Dip*
40V	2Ω	VN0204N6	VN0204N7
60V	2Ω	VN0206N6	VN0206N7

*14-pin Side Brazed Ceramic Dip.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and Military versions available
- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Thermal Characteristics

Package	Plastic DIP	Ceramic DIP
I_D continuous & I_{DR} (single die)	0.86A	1.0A
I_D pulsed* & I_{DRM}*	4.0A	4.0A
Power Dissipation @ T_C = 25°C‡	3W	4W
θ_{ja} (°C/W)	83.3	62.5
θ_{jc} (°C/W)	41.6	31.2

* Pulse test 300 μS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

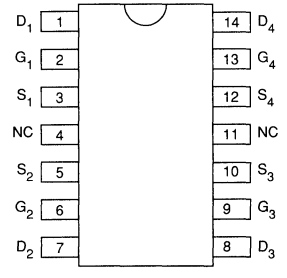
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to VN02A Data Sheet for detailed characteristics.

Pin Configuration



top view

14-pin DIP

N-Channel Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	Order Number / Package	
		20 Terminal Ceramic LCC	Die
60V	3Ω	VN2106NF	VN2106ND
100V	3Ω	VN2110NF	VN2110ND

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and Military versions available
- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain

Applications

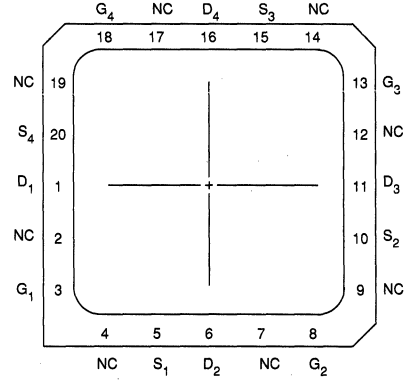
- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Pin Configuration



top view

20-pin Ceramic LCC

Thermal Characteristics

Package	I_D (continuous)†	I_D (pulsed)	Power Dissipation* @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}
20 Terminal LCC	0.46A**	2.0A	1.25W	170	100	0.46A**	2.0A

† I_D (continuous) is limited by max rated T_j.

* Total for package.

** Single die.

Electrical Characteristics (@ 25°C unless otherwise specified)

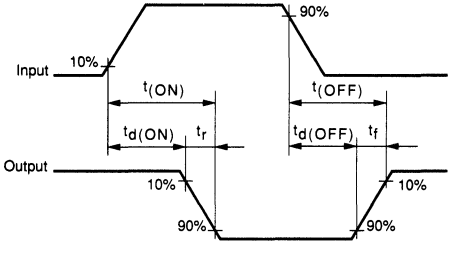
(Notes 1 and 2)

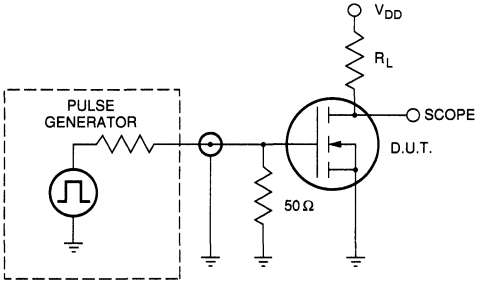
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN2110	100			V	I_D = 1mA, V_{GS} = 0
		VN2106	60				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	V_{GS} = V_{DS}, I_D = 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.5	mV/°C	I_D = 1mA, V_{GS} = V_{DS}
I_{GSS}	Gate Body Leakage			0.1	100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				1		V_{GS} = 0, V_{DS} = Max Rating
					100	µA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		0.5	1.0		A	V_{GS} = 5V, V_{DS} = 25V
			1.0	2.50			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			4.50	5	Ω	V_{GS} = 5V, I_D = 250mA
				2	3		V_{GS} = 10V, I_D = 1.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.70	1.0	%/°C	I_D = 1A, V_{GS} = 10V
G_{FS}	Forward Transconductance		300	400		m℧	V_{DS} = 25V, I_D = 0.5A
C_{ISS}	Input Capacitance				50	pF	V_{GS} = 0, V_{DS} = 25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance				25		
C_{RSS}	Reverse Transfer Capacitance				5		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	V_{DD} = 25V I_D = 1.0A R_S = R_L = 50Ω
t_r	Rise Time			5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			6	9		
t_f	Fall Time			5	8		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	I_{SD} = 2.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			400		ns	I_{SD} = 1.0A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





P-Channel Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	Order Number / Package	
		14-Pin P-Dip	14-Pin C-Dip*
-40V	8Ω	VP0104N6	VP0104N7
-60V	8Ω	VP0106N6	VP0106N7

*14-pin Side Brazed Ceramic Dip.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and Military versions available
- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Thermal Characteristics

Package	Plastic DIP	Ceramic DIP
I_D continuous & I_{DR} (single die)	0.35A	0.4A
I_D pulsed* & I_{DRM}*	1.0A	1.0A
Power Dissipation @ T_C = 25°C‡	2W	3W
θ_{ja} (°C/W)	110	83.3
θ_{jc} (°C/W)	62.5	41.6

* Pulse test 300 μS pulse, 2% duty cycle.

‡ Total for package.

Advanced DMOS Technology

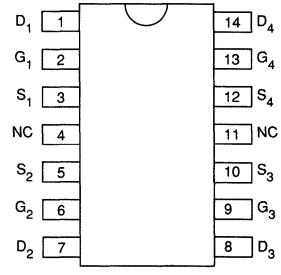
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to VP01A Data Sheet for detailed characteristics.

Pin Configuration



top view

14-pin DIP

P-Channel Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	Order Number / Package	
		14-Pin P-Dip	14-Pin C-Dip*
-40V	4Ω	VP0204N6	VP0204N7
-60V	4Ω	VP0206N6	VP0206N7

*14-pin Side Brazed Ceramic Dip.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and Military versions available
- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Thermal Characteristics

Package		Plastic DIP	Ceramic DIP
I_D continuous & I_{DR} (single die)	N-Channel	0.6A	0.7A
	P-Channel		
I_D pulsed+ & I_{DRM}+	N-Channel	2.5A	2.5A
	P-Channel		
Power Dissipation @ T_C = 25°C‡		3W	4W
θ_{ja} (°C/W)		83.3	62.5
θ_{jc} (°C/W)		41.6	31.2

+ Pulse test 300 µS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

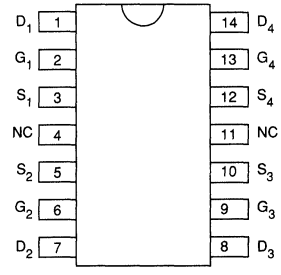
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to VP02A Data Sheet for detailed characteristics.

10

Pin Configuration



top view

14-pin DIP

N-Channel Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			14-Pin P-DIP	14-Pin C-DIP
60V	5.5Ω	0.5A	VQ1000N6	VQ1000N7

Features

- ☐ Very high input impedance
- ☐ Very high speed
- ☐ Low on-resistance
- ☐ No secondary breakdown
- ☐ High reliability

Applications

- ☐ Logic to high current interface
- ☐ High speed line driver
- ☐ LED digit strobe driver
- ☐ Linear amplifiers
- ☐ Stepper motor drive

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 15V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

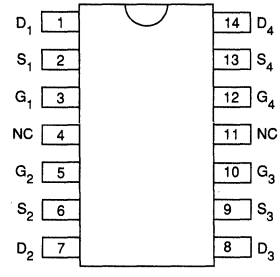
*Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Pin Configuration



top view

14-pin DIP

Thermal Characteristics (@ T_A = 25°C)

Test	Unit	Each Transistor	All four Transistors
			VQ1000N7
Total Power Dissipation	Watts	1.30	2.0
Linear Derating Factor	mW/ °C	10.5	16
Thermal Resistance	°C/W	96	62.5
Thermal Coupling Factor (K)			
Q_1 - Q_4 or Q_2 - Q_3	%	60	
Q_1 - Q_2, Q_3 - Q_4, Q_1 - Q_3 or Q_4 - Q_2	%	50	
Continuous Drain Current [2,3]	A	0.225	—
Pulsed Drain Current [1,3]	A	1.0	—

Note 1: All D.C. parameter 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs, 2% duty cycle.)
Note 2: I_D (continuous) is limited by max rated T_j.
Note 3: T_C = 25°C.

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60			V	V_{GS} = 0, I_D = 100µA
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.5	V	V_{GS} = V_{DS}, I_D = 1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.0	-5.0	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate Body Leakage			100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			10	µA	V_{GS} = 0, V_{DS} = Max Rating
				500		V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	0.2			A	V_{GS} = 5V, V_{DS} = 25V
		0.5				V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			7.5	Ω	V_{GS} = 5V, I_D = 0.2A
				5.5		V_{GS} = 10V, I_D = 0.3A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.6	1.1	%/°C	V_{GS} = 10V, I_D = 0.3A
G_{FS}	Forward Transconductance	100			m℧	V_{DS} = 15V, I_D = 0.5A
C_{ISS}	Input Capacitance			60	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			25		
C_{RSS}	Reverse Transfer Capacitance			5		
$t_{d(ON)}$	Turn-ON Delay Time			5	ns	V_{DD} = 15V, I_D = 0.6A, R_S = 50Ω
t_r	Rise Time			5		
$t_{d(OFF)}$	Turn-OFF Delay Time			5		
t_f	Fall Time			5		
V_{SD}	Diode Forward Voltage Drop		-0.85		V	V_{GS} = 0, I_{SD} = 0.5A
t_{rr}	Reverse Recovery Time		165		ns	V_{GS} = 0, I_{SD} = 0.3A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Thermal Coupling and Effective Thermal Resistance

In multiple chip devices, coupling of heat between die occurs. The junction temperature can be calculated as follows:

$$\Delta T_{J1} = R_{\theta 1} P_{D1} + R_{\theta 2} K_{\theta 2} P_{D2} + R_{\theta 3} K_{\theta 3} P_{D3} + R_{\theta 4} K_{\theta 4} P_{D4} \quad (1)$$

where ΔT_{J1} is the change injunction temperature of die 1.

$R_{\theta 1}$ thru 4 is the thermal resistance of die 1 through 4.

P_{D1} thru 4 is the power dissipated in die 1 through 4.

$K_{\theta 2}$ thru 4 is the thermal coupling between die 1 and die 2 through 4.

An effective package thermal resistance can be defined as follows:

$$R_{\theta (EFF)} = \Delta T_{J1}/P_{DT} \quad (2)$$

where P_{DT} is the total package power dissipation.

Assuming equal thermal resistance for each die, equation (1) simplifies to:

$$\Delta T_{J1} = R_{\theta 1}(P_{D1} + K_{\theta 2} P_{D2} + K_{\theta 3} P_{D3} + K_{\theta 4} P_{D4}) \quad (3)$$

For conditions where $P_{D1} = P_{D2} = P_{D3} = P_{D4}$, $P_{DT} = 4P_D$, equation (3) can be further simplifed and, by substituting into equation (2), results in:

$$R\theta_{(EFF)} = R_{\theta 1}\,(1 + K_{\theta 2} + K_{\theta 3} + K_{\theta 4})/4 \quad (4)$$

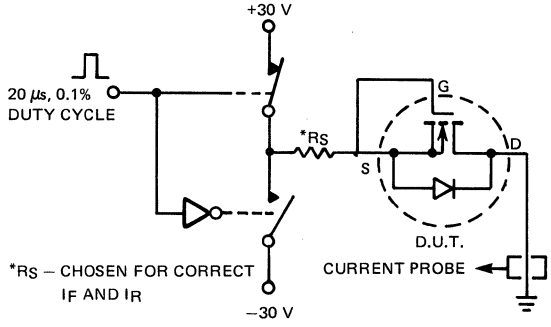
Values for the coupling factors when the ambient is used as a reference are given in the previous table. If significant power is to be dissipated in two die, die at the opposite ends of the package should be used so that lowest position junction temperatures will result.

Drain-Source Diode (t_{rr} - Reverse Recovery Time)

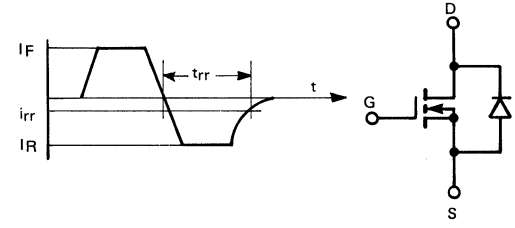
The internal drain-source diodes of DMOS Power FETs may be used as catch diodes or free-wheeling diodes. Current ratings for these diodes are the same as the contnuous and peak drain current ratings for the DMOS FET.

Reverse recovery time is measured using the circuit below. Forward and reverse current I_F and I_R are equal and are tested at the continuous and peak current ratings of the DMOS FET.

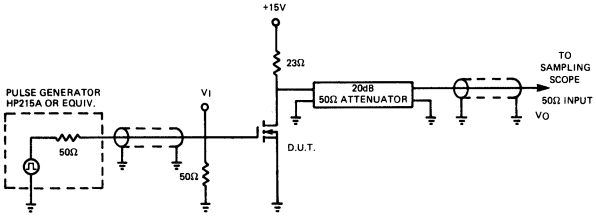
Switching Waveforms and Test Circuits



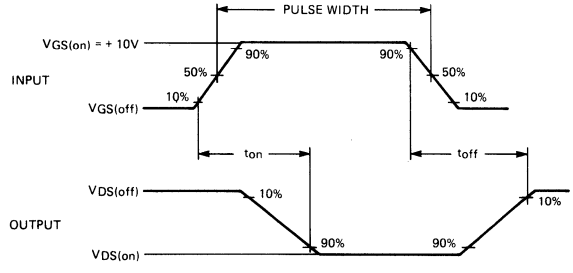
T_{RR} Test Circuit



T_{RR} Test Waveforms



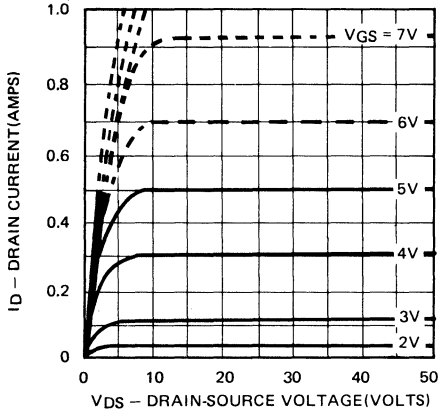
Switching Time Test Circuit



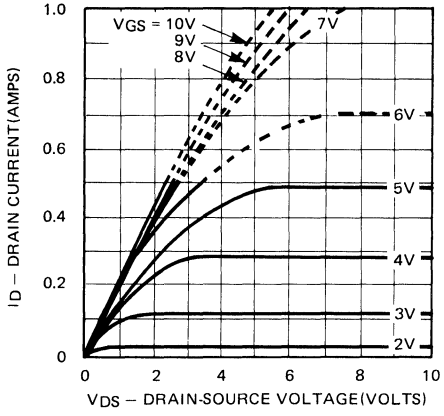
Switching Time Test Waveform

Typical Performance Curves

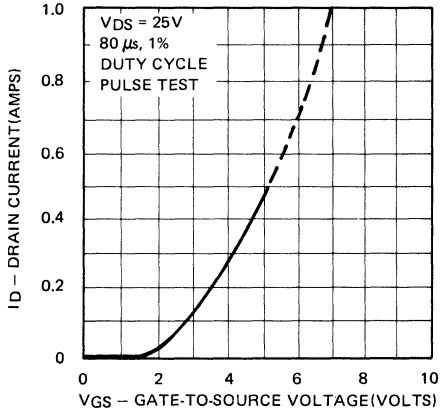
Output Characteristics



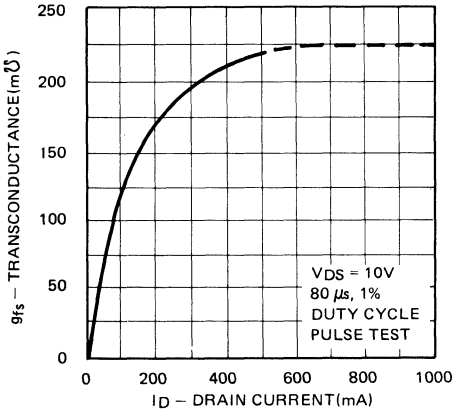
Saturation Characteristics



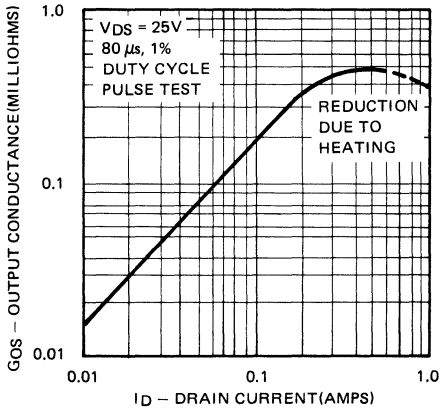
Static
Transfer Characteristics



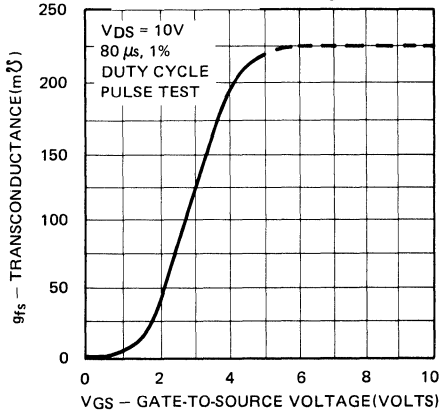
Transconductance vs Drain
Current



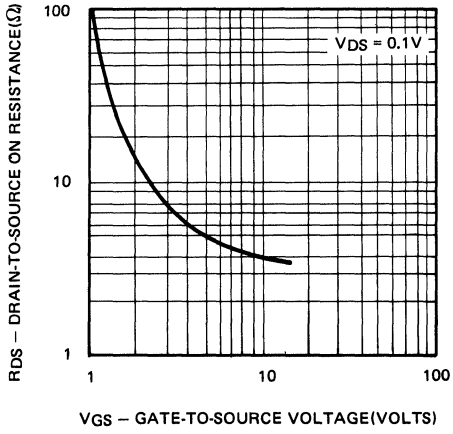
Output Conductance vs
Drain Current



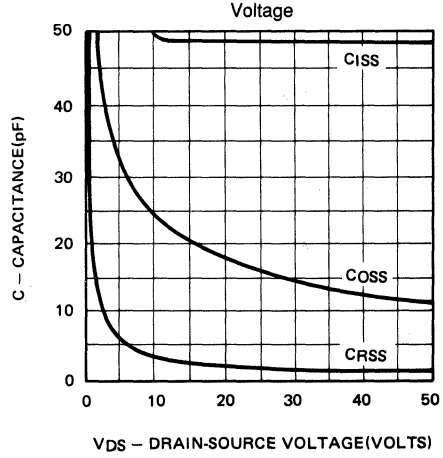
Transconductance vs
Gate-Source Voltage

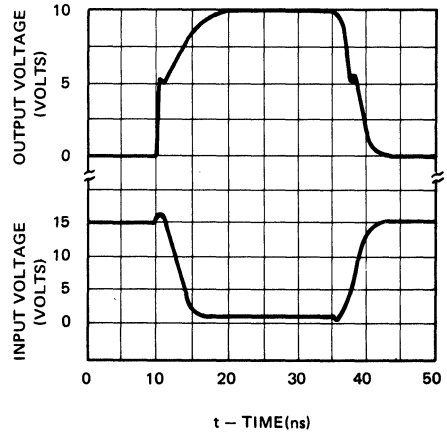


Drain-to-Source ON Resistance
vs Gate-to-Source Voltage



Capacitance vs Drain-to-Source
Voltage





N-Channel Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			Quad Ceramic DIP*
30V	1.0Ω	2.0A	VQ1001P

*14-pin side-brazed ceramic DIP.

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

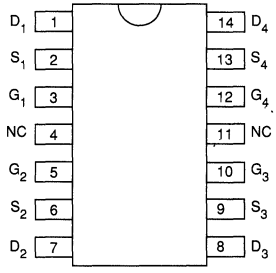
*Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Pin Configuration



top view

14-pin DIP

Thermal Characteristics (T_A = 25°C)

Test	Unit	Each Transistor	All Four Transistors
		VQ1001P	VQ1001P
Total Power Dissipation	Watts	1.3	2.0
Linear Derating Factor	mW/°C	10.4	9.6
Thermal Resistance	°C/W	250	104
Continuous Drain Current	A	.85	
Pulsed Drain Current	A	3.0	

Electrical Characteristics (@ 25°C unless otherwise specified)

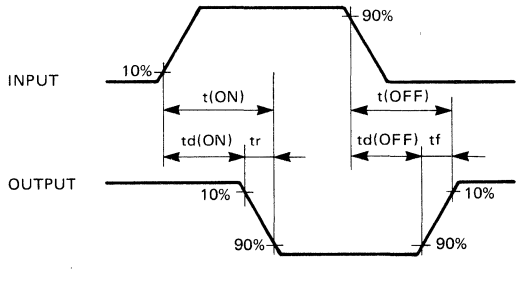
(Notes 1 and 2)

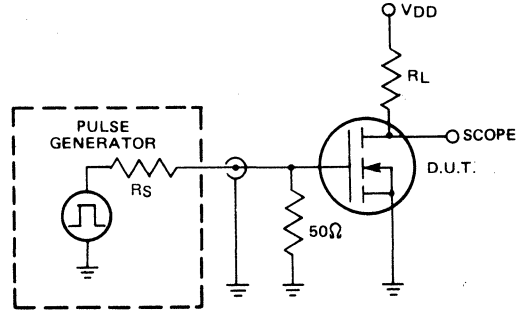
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30			V	V_{GS} = 0, I_D = 10 μA
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.5	V	V_{GS} = V_{DS} I_D = 1mA
I_{GSS}	Gate Body Leakage			100	nA	V_{GS} = ±15V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{GS} = 0, V_{DS} = Max Rating
				500		V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	2			A	V_{GS} = 12V, V_{DS} ≥ $2V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			1.75	Ω	V_{GS} = 5V, I_D = 0.2A
				1		V_{GS} = 12V, I_D = 1.0A
G_{FS}	Forward Transconductance	200			m℧	V_{DS} ≥ $2V_{DS(ON)}$, I_D = 0.5A
C_{ISS}	Input Capacitance			110	pF	V_{GS} = 0, V_{DS} = 15V f = 1MHz
C_{OSS}	Common Source Output Capacitance			110		
C_{RSS}	Reverse Transfer Capacitance			35		
$t_{(ON)}$	Turn-ON Time			30	ns	V_{DD} = 15V, I_D = .6A R_S = 50Ω
$t_{(OFF)}$	Turn-OFF Time			30		
V_{SD}	Diode Forward Voltage Drop		−0.85		V	V_{GS} = 0, I_{SD} = 1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			Quad Ceramic DIP*	Quad Plastic DIP
60V	3.5Ω	1.5A	VQ1004P	VQ1004J

*14-pin side-brazed ceramic DIP.

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

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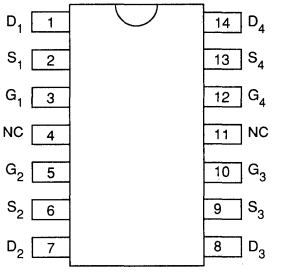
Pin Configuration



top view

14-pin DIP

Thermal Characteristics (T_A = 25°C)

Test	Unit	Each Transistor		All Four Transistors	
		VQ1004P	VQ1004J	VQ1004P	VQ1004J
Total Power Dissipation	Watts	1.3	1.3	2.0	2.0
Linear Derating Factor	mW/°C	10.4	10.4	16	16
Thermal Resistance	°C/W	96.2	96.2	62.5	62.5
Continuous Drain Current	A	.46	.46		
Pulsed Drain Current	A	2.0	2.0		

Electrical Characteristics (@ 25°C unless otherwise specified)

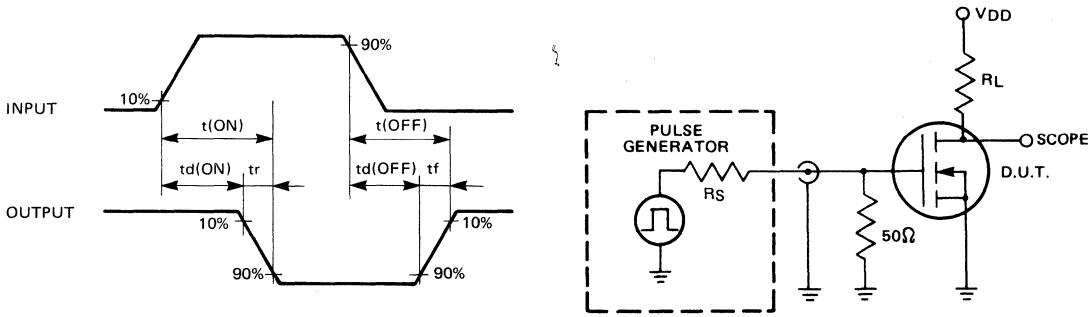
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60			V	V_{GS} = 0, I_D = 10 μA
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.5	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage			100	nA	V_{GS} = ±15V, V_{DS} = O
I_{DSS}	Zero Gate Voltage Drain Current			1	μA	V_{GS} = O, V_{DS} = Max Rating
				500		V_{GS} = O, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	1.5			A	V_{GS} = 10V, V_{DS} ≥ 2 $V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5	Ω	V_{GS} = 5V, I_D = 0.3A
				3.5		V_{GS} = 10V, I_D = 1A
G_{FS}	Forward Transconductance	170			m℧	V_{DS} ≥ 2$V_{DS(ON)}$, I_D = .5A
C_{ISS}	Input Capacitance			60	pF	V_{GS} = 0, V_{DS} = 25V f = 1MHz
C_{OSS}	Common Source Output Capacitance			50		
C_{RSS}	Reverse Transfer Capacitance			10		
$t_{(ON)}$	Turn-ON Time			10	ns	V_{DD} = 25V I_D = 1A R_S = 50Ω
$t_{(OFF)}$	Turn-OFF Time			10		
V_{SD}	Diode Forward Voltage Drop		0.9		V	V_{GS} = 0, I_{SD} = 1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



Supertex inc.

HVCMOS Selector Guide

High-Voltage Source/Sink Outputs (Push-Pull)

Device Number	Out-puts	Logic Configuration	Output Operating Voltage	Output Current Per Channel	Similar Devices	Applications
HV6810	10	Serial to parallel converter w/latches	80V	+25mA -4mA	TI TL4810 Sprague UCN5810	Vacuum Fluorescent display drivers
HV01	16	Grey shade driver with 16 analog levels	60V	±40mA	None	Video and grey shade displays EL and LCD
HV08	24	Grey shade driver with 16 analog levels	70V	±40mA	None	Video and grey shade displays EL and LCD
HV53/ HV54	32	Serial to parallel converter w/latches, output enable	80V	±20mA	*Siliconix SI 9553/9554 *TI SN75555/75556 *Sprague UCN5853/5854	EL column drivers and non-impact printers LCD Drivers
HV57/ HV58	32	Serial to parallel converter w/latches, polarity and blanking	80V	±20mA	Siliconix SI9553/9554 TI SN75555/75556 Sprague UCN5853/5854	Non-impact printers and plotters, EL displays, LCD drivers
HV60	32	LCD driver w/active return to ground	±40V	±15mA	None with return to GND capability	High voltage LCD displays
HV500	32	AC plasma driver with multiplexed 8-bit shift register	100V	±15mA	*TI SN75500/55500	AC plasma display drivers, printer
HV501	32	Serial to parallel AC plasma driver with shift register	100V	±15mA	*TI SN75501/55501	AC plasma display drivers, printer
HV04/ HV06	64	Serial to parallel converter w/latches, polarity and blanking	80V	±20mA	None	EL column drivers, non-impact printers, LCD displays
HV04H/ HV06H	64	Serial to parallel converter w/latches, polarity and blanking w/hotswitch capability	80V	+20mA -12mA	None	EL column drivers, non-impact printers, LCD displays

*Pin compatible direct replacement.

High-Voltage Sink Only Outputs (Open Drain N-Channel)

Device Number	Out-puts	Output Logic Configuration	Output Operating Voltage	Current Per Channel	Direct Competitive Devices	Applications
HV02	16	Serial to parallel converter	250V	-250mA	None	EL row driver
HV51 HV52	32	Serial to parallel converter w/output enable and strobe	220V	-100mA	*TI 75551/75552 *Siliconix Si9551/9552 *Sprague UCN5851/5852	EL row driver, non-impact printers/ plotters
HV55 HV56	32	Serial to parallel converter w/latches, polarity and blanking	300V	-100mA	TI 75551/75552 Siliconix Si9551/9552 Sprague UCN5851/5852	Non-impact printers/ plotters, EL row drivers
HV03 HV05	64	Serial to parallel converter w/latches, Supertex logic	300V	-100mA	None	EL row drivers, non-impact printers/plotters
HV30	8	7 segment decoder/driver	200V	-5mA	None	EL 7 segment displays

*Pin compatible direct replacement

High-Voltage Source Only Outputs (Open Drain P-Channel)

Device Number	Out-puts	Logic Configuration	Output Operating Voltage	Output Current Per Channel	Similar Devices	Applications
HV41 HV42	32	Serial to parallel converter w/output enable and strobe	-220V	+80mA	Sharp	EL row drivers, non-impact printers
HV45 HV46	32	Serial to parallel converter w/latches, polarity and blanking	-300V	+60mA	Sharp	Non-impact printers and plotters, EL display row drivers

High-Voltage Analog Switches

Device Number	Switches	Switch Operating Configuration	Maximum Switch Resistance	Similar Devices	Applications
HV341	Dual SPST	100V P-P	100 ohms	MAX 341	High voltage switching, mil electronics & insturmentation
HV343	Dual SPDT	100V P-P	100 ohms	MAX 343	High voltage switching, mil electronics & instrumentation
HV345	Dual DPST	100V P-P	100 ohms	MAX 345	High voltage switching, mil electronics & instrumentation
HV348	Dual SPST	100V P-P	55 ohms	MAX 348	High voltage switching, mil electronics & instrumentation

High-Voltage Bilateral Switches

Device Number	Swit-ches	Logic Configuration	Maximum Switch Voltage	Peak Switch Current	Similar Devices	Applications
HV10 HV17	4	Individual inputs with/without latches	160V P-Supp 130V P-P Sig	±3.0A	Siliconix DG568/569 Intersil H9108	Medical ultrasound HV multiplexers, Ink jet printers
HV12-16 HV18	8	Shift register or decoders, latches & chip selects	160V P-Supp 130V P-P Sig	±1.5A	Siliconix DG568/569 Intersil H9108	Medical ultrasound HV multiplexers, Ink jet printers

16-Channel Matrix TFEL Panel Display Column Driver

Ordering Information

Device	Package Options					
	40-Pin Ceramic DIP	36-Pin Leadless Chip Carrier	36-Pin Leaded Chip Carrier Flat Leads	36-Pin Leaded Chip Carrier Std. Bent Leads	36-Pin Leaded Chip Carrier Reverse Bent Leads	Die
HV01	HV01C	HV01LC	HV01CF	HV01CS	HV01CR	HV01X

Features

- ☐ Up to 60V modulation supply voltage
- ☐ Drives up to 1000 lines
- ☐ Capability of 16 levels of gray shading
- ☐ 15µS per conversion and output cycle
- ☐ Integrated high voltage DMOS and CMOS technology
- ☐ Available in 40-pin DIP, 36 LCC pkg., or in die form

General Description

The HV01 is a 16 channel column driver IC designed for general purpose electroluminescent display use. The chip contains a D to A converter and a push-pull output driver for each channel. Input data is clocked in on the Hi to Low transition of the Clock input and stored in shift registers. This data feeds into the respective 4-bit polynomial counter, which serves as a time measuring device. The output of this counter controls a charging device allowing a ramp signal to set the analog driver to the desired voltage level corresponding to one of the 16 possible gray shades.

Absolute Maximum Ratings

Low Voltage Supply V_{DD}	-0.5V to 14V
High Voltage Supply V_{PP}	-0.5V to 65V
Ramp Voltage V_R	-0.5 to V_{PP} +0.3V
Logic Input Voltage	-0.5V to V_{DD} +0.5V
Storage Temperature	-65°C to 150°C
Power Dissipation[1]	1.6 Watt

Note 1: For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage Logic Inputs	V_{DD} - 1			V	
V_{IL}	Input Low Voltage Logic Inputs			1	V	
I_{DD}	V_{DD} Supply Current		4	13	mA	V_{DD} = 13.2V, f_{SC} = 3mHz
I_{DDS}	STDBY V_{DD} Supply Current			8	mA	V_{DD} = 13.2V
I_{PP}	V_{PP} (Driver) Supply Current		12		mA	V_{PP} = 60V, t_{CR} = 50µS
I_{PPS}	STDBY V_{PP} Supply Current			5.5	mA	V_{PP} = 60V
I_{IL}, I_{IH}	Input Leakage Current		±1	±50	µA	V_{IN} = 0V or V_{DD}
I_{OH}	Logic Output Source Current	-50			µA	V_{OH} = V_{DD} - 1.0V
I_{OL}	Logic Output Sink Current	50			µA	V_{OL} = 1.0V
I_{AOH}	HV Analog Output Source Current	-8	-40		mA	V_{PP} = 60V, V_R = 60V V_{AOH} = 50V
I_{AOL}	HV Analog Output Sink Current	8	40		mA	V_{PP} = 60V, V_R = 60V V_{AOL} = 10V

AC Characteristics (V_{DD} = 12V, T_A = 25°C)

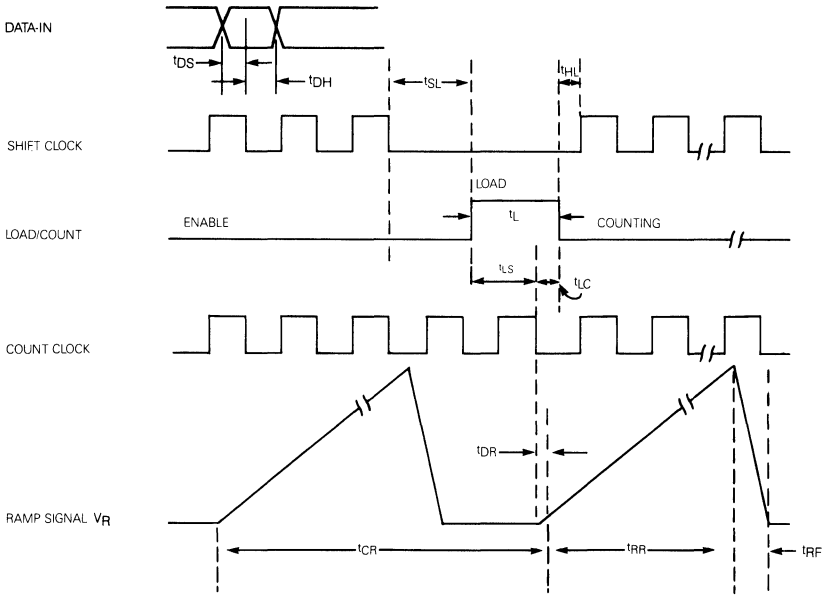
Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{SL}	Set up time before load (Shift Clock)	200			ns	
t_{HL}	Hold time after load (Shift Clock)	100			ns	
t_L	Load/Count Pulse Width	100			ns	
t_{LS}	Load set up before Count Clock	20			ns	
t_{LC}	Load hold after Count Clock	20			ns	
t_{DR}	Count to Ramp Delay			100	ns	
t_{CR}	Cycle Time of Ramp Signal	8			µs	
t_{RR}	Rise Time of Ramp Signal	3			µs	
f_{SC}	Operating Frequency (Shift Clock)			6	MHz	V_{DD} = 10.8V
t_{DS}	Data set up to shift clock ↓	35			ns	
t_{DH}	Data hold from shift clock ↓	20			ns	
C_H	Internal holding capacitance per part		50		pF	
t_{RF}	Ramp voltage fall time	5			µs	

Recommended Operating Conditions*

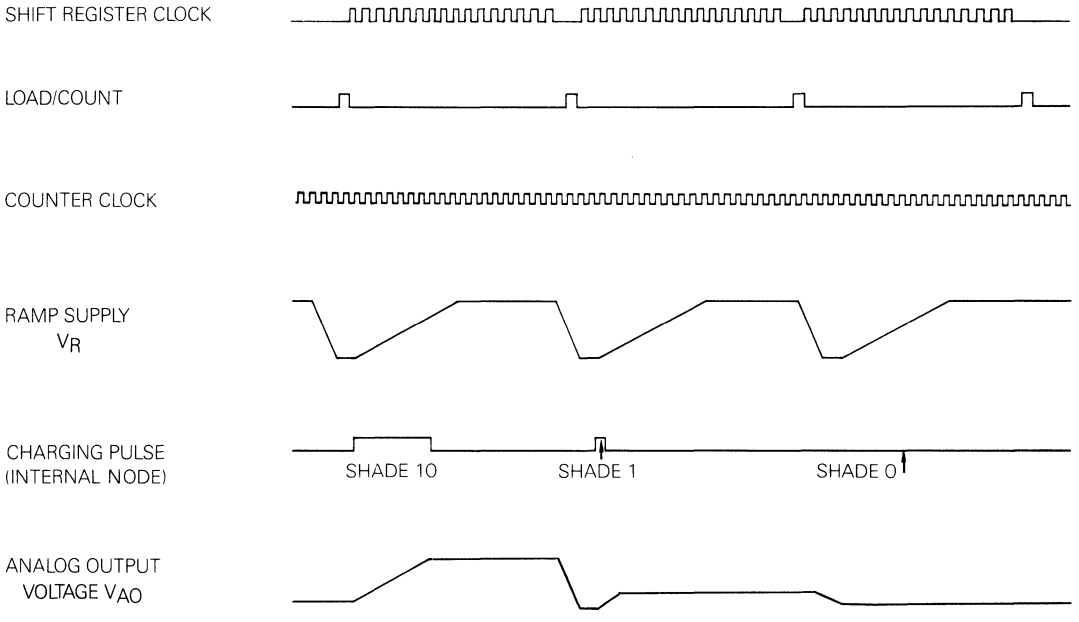
Parameter	Value
Low Voltage Supply V_{DD}	12V ± 10%
High Voltage Supply V_{PP}	40V to 60V
Logic Input Voltage	0 to V_{DD}
Operating Temperature (T_A)	-40°C to 85°C

* Recommended Power Up Sequence: V_{DD}, V_{PP}, Logic, V_R

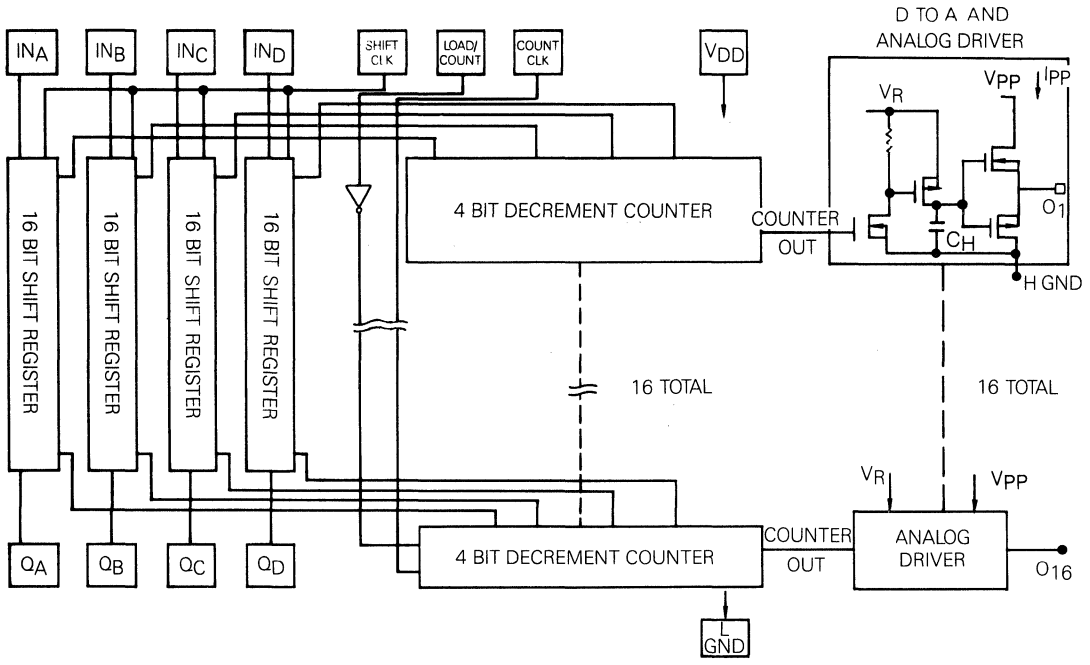
Switching Waveforms



Timing Diagram



Functional Block Diagram



Function Table

Function	Control Inputs				Shift Registers	Counters	Outputs	
	Shift Clock	Counter Clock	Load/ Count	V_R			Serial	Parallel
Load Shift Register	↓	X	L	X	Normal Shift Op.	X	Delayed Data-In	X
Load Counter	No↓	↓	H	X	No Change	Load Data From S/R to Counter	No Change	Low
Counting	X	↓	L	Initiates Ramp	X	Translates Data To Time	X	D/A Conversion
Voltage Conversion	X	Pulsing	L	Volt. Ramping Up	X	Counting	X	Follows Ramp

L = Low level, H = High level, X = Irrelevant, ↓ = Hi to Low Transition

Operation of the Column Driver

Operation of the Column Driver can be understood by looking at the logic and timing diagrams. The shift registers store four bits of data for each column to be driven. The four bits are used to program a counter for sixteen possible values (0-15) which generate the sixteen gray shades. Since the shift registers have serial outputs, the chips can be connected in sequence. To load the shift registers we need n times sixteen pulses (where n = the # of chips connected serially). After the last shift clock, we need a short set up time (t_{SL}) before we can load the data of the register into the counter. The loading is performed by the Hi level of a Load/ Count Enable Pulse (t_L). At the end of this pulse the load count enable goes low and the transfer gates which connect the shift registers to the counters turn off and the counter inputs are enabled. The counting will start at the negative going edge of the first count clock pulse (t_{LC}). Concurrently, a positive going ramp signal is initiated whose rise time is equal to the length of 16 count clocks. The output of the counter is, in effect, a pulse width with a termination time controlled by the shift register digital value. The analog storage stage follows the value on the voltage ramp input for the duration of that pulse, and then holds that voltage value. As the timing diagram indicates, each pulse width will specify a different voltage level. In effect a digital to analog converter stage was implemented. If at any time the difference in voltage stored in the analog storage stage and the output voltage differs by more than one transistor threshold (typically 2 to 3 volts), one of the two output transistors will turn on to set the correct voltage on the column.

Programming the Column Driver

The Supertex HV01 Column Driver was built to generate 16 different shades on a thin film electroluminescent panel. These 16 shades are achieved by having 1 of 16 possible voltage levels on the analog outputs.

Depending on the 4 digital inputs fed into the 4 shift registers, data is loaded into each of the 16 counters. These counters will interpret the data and produce a pulse whose width is determined by the data. The output of each drive line is basically a D/A conversion of the timing signal generated by the polynomial counter.

The shade voltages are specified by the digital input according to the table shown. In the table we designate the various shade voltages by numbers. Shade No. 16 is the brightest, while Shade

Gray Shade Decoding Scheme

Brightest Shade No.	INA	INB	INC	IND	
16	1	0	0	1	Brightest
15	1	1	0	1	
14	1	1	1	1	
13	1	1	1	0	
12	0	1	1	1	
11	1	0	1	0	
10	0	1	0	1	
9	1	0	1	1	
8	1	1	0	0	
7	0	1	1	0	
6	0	0	1	1	
5	1	0	0	0	
4	0	1	0	0	
3	0	0	1	0	
2	0	0	0	1	
1	0	0	0	0	Dimmest

Pin Configurations

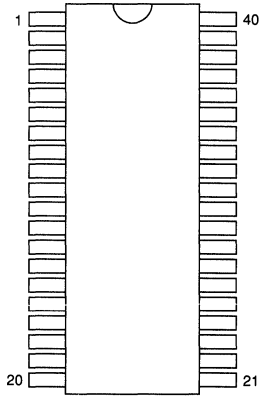
40-Pin DIP

Pin	Function	Pin	Function
1	L GND	21	HVout 8
2	Load Count	22	HVout 7
3	N/C	23	HVout 6
4	O_A	24	HVout 5
5	O_B	25	HVout 4
6	O_C	26	HVout 3
7	O_D	27	HVout 2
8	V_R	28	HVout 1
9	V_{PP}	29	H GND
10	N/C	30	N/C
11	N/C	31	N/C
12	H GND	32	V_{PP}
13	HVout 16	33	V_R
14	HVout 15	34	IN_D
15	HVout 14	35	IN_C
16	HVout 13	36	IN_B
17	HVout 12	37	IN_A
18	HVout 11	38	Shift CLK
19	HVout 10	39	Count CLK
20	HVout 9	40	V_{DD}

36-Pin LCC

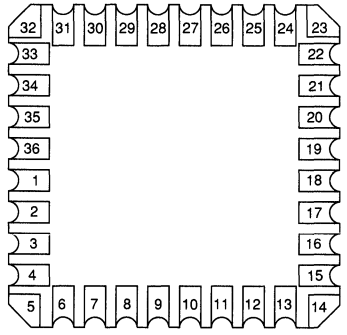
Pin	Function	Pin	Function
1	L GND	19	HVout 8
2	Load Count	20	HVout 7
3	N/C	21	HVout 6
4	O_A	22	HVout 5
5	O_B	23	HVout 4
6	O_C	24	HVout 3
7	O_D	25	HVout 2
8	V_R	26	HVout 1
9	V_{PP}	27	H GND
10	H GND	28	V_{PP}
11	HVout 16	29	V_R
12	HVout 15	30	IN_D
13	HVout 14	31	IN_C
14	HVout 13	32	IN_B
15	HVout 12	33	IN_A
16	HVout 11	34	Shift CLK
17	HVout 10	35	Count CLK
18	HVout 9	36	V_{DD}

Package Outlines



top view

40-pin DIP



top view

36-pin LCC

16-Channel Matrix TFEL Panel Display Row Driver

Ordering Information

Device	Package Options					
	40-Pin Ceramic DIP	36-Pin Leadless Chip Carrier	36-Pin Leaded Chip Carrier Flat Leads	36-Pin Leaded Chip Carrier Std. Bent Leads	36-Pin Leaded Chip Carrier Reverse Bent Leads	Die
HV02	HV02C	HV02LC	HV02CF	HV02CS	HV02CR	HV02X

Features

- ☐ HVCMOS® Technology
- ☐ Up to 200V output voltage
- ☐ Can drive up to 1000 lines
- ☐ 250mA surge current sink capability
- ☐ TYP R_{ON} of 25 ohms
- ☐ High performance – up to 200 KHz scan rate
- ☐ Integrated high voltage DMOS and CMOS technology
- ☐ Available in 40-pin DIP, 36 Pin Ceramic Chip Carrier and Leaded Chip Carrier packages

Absolute Maximum Ratings

Low Voltage Supply V_{DD}	-0.5V to 14V
BV_{DS} Driver output transistor voltage	-0.5V to 250V
Total Drive Current (Unison Mode) I_{OLU}	1.6 AMP
Logic Input Voltage	-0.5V to V_{DD} +0.5V
Storage Temperature	-65°C to 150°C
Power Dissipation[1]	1.6 Watt

Note 1: For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

General Description

The HV02 is a 16 Channel Row Drive IC designed for general purpose electroluminescent display use. The chip provides the scanning voltage to each row output in sequence and, in unison, generates the refresh pulse and two sinking pulses (scan and refresh sink) which are required for the operation of the TFEL panel. The intrinsic source-drain diodes on the outputs can handle surge currents up to 250mA for charging of the capacitive loads.

Serial Data is entered into a 16-bit shift register on the Hi to Low transition of the clock input. Data is outputted if enable is Hi and the "ALL ON" input is Low. If the "ALL ON" input goes Hi, all parallel outputs turn on in unison to refresh the Row lines on the panel. Expansion is possible by using the serial output (data out). This output is not controlled by the enable and "ALL ON" inputs. To make the system design versatile, the HV02 has an initialization feature which allows setting or resetting the first bit and resetting the other bits of the shift register.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage	V_{DD} - 1			V	
V_{IL}	Input Low Voltage			1	V	
I_{DD}	V_{DD} Supply Current		1	6.5	mA	V_{DD} = 13V, f_{SC} = 100KHz
I_{OLH}	High Voltage Output Sink Current (Single Driver)	250	300		mA	V_{DD} = 10.8V V_O = 15V
I_{IL}, I_{IH}	Input Leakage Current		±1	±50	µA	V_{IN} = 0V or V_{DD}
R_{ON}	Output driver transistor On-resistance		25	60	Ω	V_{DD} = 10.8V
BV_{DS}	Output driver transistor Drain-Source Breakdown voltage	200	250		V	High Voltage Outputs Off I_O = 200µA
I_{OL}	Shift Register Data Out Source Current	50			µA	V_{DD} = 10.8V V_{OL} = 1.0V
I_{OH}	Shift Register Data Out Source Current	-50			µA	V_{DD} = 10.8 V_{OH} = V_{DD} - 1.0V

AC Characteristics (V_{DD} = 12V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_C	Max shift Clock Frequency	6	10		MHz	V_{DD} = 10V
S_R	Driver Ground Slew Rate			50	V/µsec	

Recommended Operating Conditions

Parameter	Value
Low Voltage Supply V_{DD}	10.8V to 13.2V
Driver ouput transistor voltage	up to 200V
Logic Input Voltage	0V to V_{DD}
Operating Temperature (T_A)	-40°C to 85°C

Operation of the Row Driver

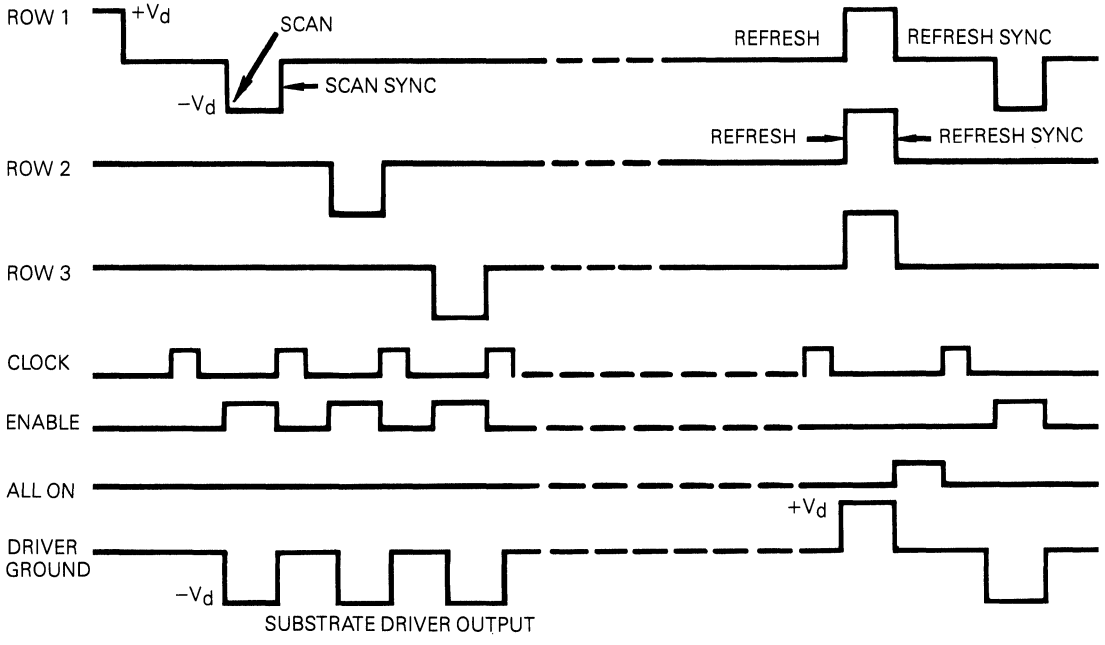
The operation of the row driver can be understood by looking at the Logic Diagram and Output Waveform states. In normal operation, a row driver selects out a single line on the electroluminescent panel by pulling it down to a negative voltage ($-V_d$). This selection is called scan. Since the EL panel has a large capacitance that was charged, eventually it has to be discharged. This operation is called refresh, and is performed by connecting these to a positive voltage ($+V_d$).

The driver ground (DR GND) is not tied to the system ground, but rather is a floating node. It is connected to the substrate driver, whose output varies as shown on the Waveform Diagram. The combination of the Row Drivers and the Substrate Drivers gives the required four functions which are called scan, scan sync, refresh and refresh sync. The first mode of the scan must be applied individually since it is by definition a single line selection. The refresh sync on the other hand, must be applied in unison. The other two modes, scan sync and refresh, can be applied either way according to the designer's discretion.

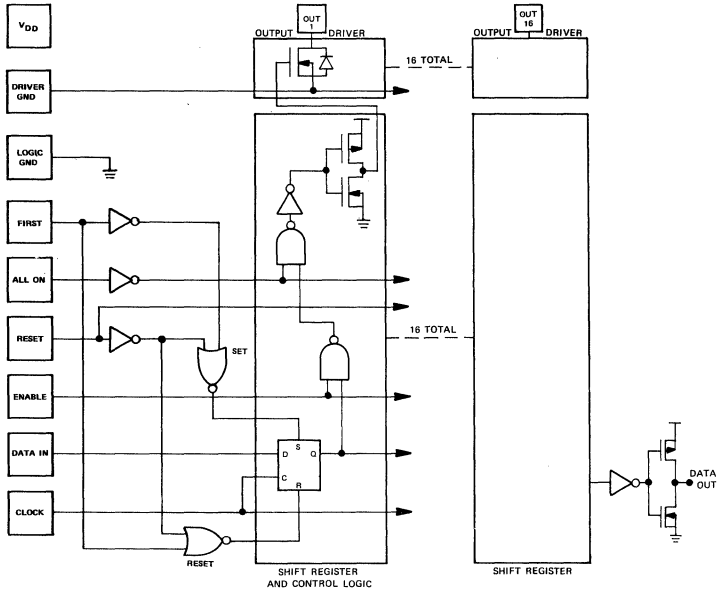
Serial data is entered into the registers on the Hi to Lo transition of the clock input. Normal operation calls for a single logic "high" to be clocked through the shift register via the serial output. To create a scan function, the enable must be pulsed at each time. For the refresh sync mode, the ALL ON input must be high, since this function has to be done in unison for all row lines.

The Row Driver was designed with an added feature of a mode control input. The flip-flops of the shift registers are made with a reset control. By pulling the "RESET" input high, they will be reset to zero with the exception of the first. This stage can be high or low during the reset depending on the control input called "First." If this input is high, the "RESET" command will be interpreted as a "SET" command for the first flip-flop. This feature is important in the normal scanning function when a group of these row drivers are interconnected to form a long string of shift registers. By utilizing this function, a single "ONE" can be placed into any of the selected chips, and the row drivers in the system can be initialized in a very flexible way.

Switching Waveforms



Logic Diagram



Function Table

Function	Control Inputs					Internal Shift Registers		Outputs	
	First	Reset	Clock	Enable	All On	1	2-16	Serial Output	1-16 Parallel
First	H	H	X	X	X	Set to "1"	RESET to "0"	"0"	Determined by Enable and ALL ON
Reset	L	H	X	X	X	Reset to "0"		"0"	Determined by ALL ON
Load Data/Shift	X	L	↓	X	X	LOAD & SHIFT		R 16	Determined by ENABLE and ALL ON
Output Enable	X	L	X	H	L	X		R 16	Determined by R_1 through R_{16}
Output Disable	X	X	X	L	L	As determined above		R 16	All Parallel Outputs "OFF"
All On	X	X	X	X	H	As determined above		R 16	All Parallel Outputs are "ON"

L = Low level, H = High level, X = irrelevant, ↓ = Hi to Low Transition, R 16 = State of register 16, R_1 = State of Register 1.

Pin Configurations

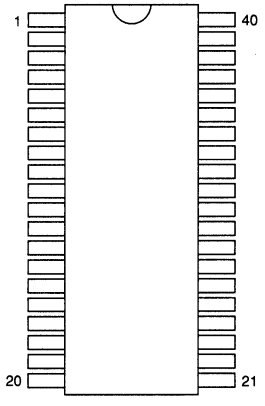
40-Pin DIP

Pin	Function	Pin	Function
1	N/C	21	HVout 8
2	All On	22	HVout 7
3	Enable	23	HVout 6
4	N/C	24	HVout 5
5	Data Out	25	N/C
6	L GND	26	N/C
7	DR GND	27	N/C
8	HVout 16	28	HVout 4
9	HVout 15	29	HVout 3
10	N/C	30	N/C
11	N/C	31	N/C
12	HVout 14	32	HVout 2
13	HVout 13	33	HVout 1
14	N/C	34	DR GND
15	N/C	35	L GND
16	N/C	36	Data In
17	HVout 12	37	Clock
18	HVout 11	38	Reset
19	HVout 10	39	V_{DD}
20	HVout 9	40	First

36-Pin LCC

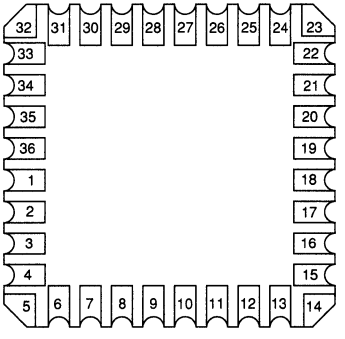
Pin	Function	Pin	Function
1	First	19	HVout 8
2	All On	20	HVout 7
3	Enable	21	HVout 6
4	Data Out	22	HVout 5
5	L GND	23	N/C
6	DR GND	24	N/C
7	HVout 16	25	N/C
8	HVout 15	26	N/C
9	HVout 14	27	HVout 4
10	HVout 13	28	HVout 3
11	N/C	29	HVout 2
12	N/C	30	HVout 1
13	N/C	31	DR GND
14	N/C	32	L GND
15	HVout 12	33	Data In
16	HVout 11	34	Clock
17	HVout 10	35	Reset
18	HVout 9	36	V_{DD}

Package Outlines



top view

40-pin DIP



top view

36-pin LCC

64-Channel Serial To Parallel Converter With Open Drain Outputs

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options					
		84-Pad Ceramic Leadless Chip Carrier	84-J Lead Plastic Chip Carrier	80-Lead Quad Cerpak Gullwing	80-Lead Quad Plastic Gullwing	80-Lead 35mm TAB Tape	Die
HV03	220V	HV0322LC	HV0322PJ	HV0322DG	HV0322PG	HV0322T	HV0322X
	300V	HV0330LC	HV0330PJ	HV0330DG	HV0330PG	HV0330T	HV0330X
HV05	220V	HV0522LC	HV0522PJ	HV0522DG	HV0522PG	HV0522T	HV0522X
	300V	HV0530LC	HV0530PJ	HV0530DG	HV0530PG	HV0530T	HV0530X

Features

- ☐ HVCMOS® Technology
- ☐ Output voltages up to 300V using a ramped supply
- ☐ Sink current minimum 100 mA
- ☐ Shift register speed 8 MHz
- ☐ Latched outputs
- ☐ Output polarity and blanking
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}	-0.5V to +15V
Supply voltage, V_{PP}[2]	-0.5V to +225V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current[3]	6.0A
Continuous total power dissipation[4]	1900mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Notes: 1. All voltages are referenced to V_{SS}.
2. These devices have been designed to be used in applications which either switch the V_{PP} supply to ground before changing the state of the high voltage outputs or limit the current through each output.
3. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

General Description

The HV03 and HV05 are low voltage serial to high voltage parallel converters with open drain outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic printheads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the shift register on the high to low transition of the clock. The HV03 shifts in the counterclockwise direction when viewed from the top of the package and the HV05 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

The HV03 and HV05 have been designed to be used in systems which either switch off the high voltage supply before changing the state of the high voltage outputs or limit the current through each output.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current				25	mA	f_{CLK} = 8MHz, f_{DATA} = 4MHz $\overline{LE}$ = LOW
I_{DDQ}	Quiescent V_{DD} Supply Current				0.25	mA	All V_{IN} = 0V
$I_{O(OFF)}$	Off State Output Current				100	µA	All outputs high, All SWS parallel
I_{IH}	High-Level Logic Input Current				10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-Level Logic Input Current				-10	µA	V_I = 0V
V_{OH}	High-Level Output Data Out		V_{DD} -1V			V	ID_{OUT} = -100µA
V_{OL}	Low-Level Output	HV_{OUT}			15	V	IHV_{OUT} = +100mA
		Data Out			1	V	ID_{OUT} = +100µA
V_{OC}	HV_{OUT} Clamp Voltage				-1.5	V	I_{OL} = -100mA

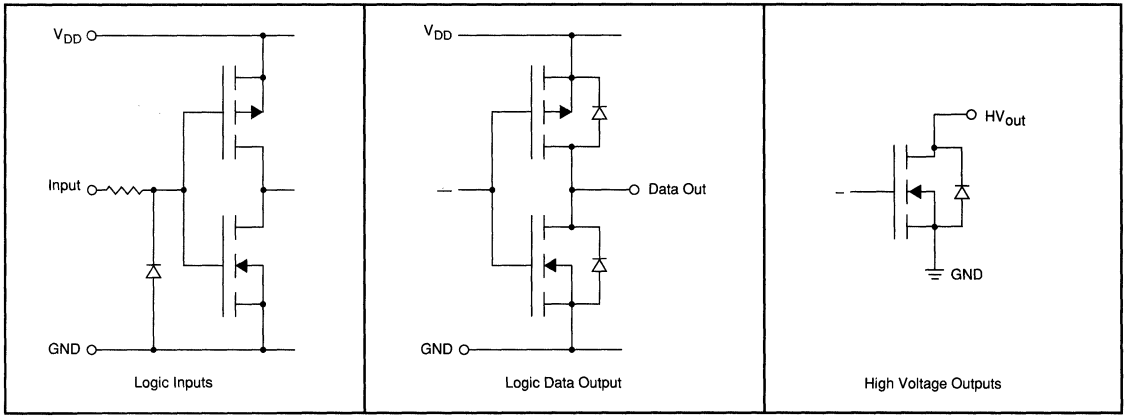
AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency			8	MHz	
t_W	Clock Width High or Low	62			ns	
t_{SU}	Data Setup Time Before Clock Falls	25			ns	
t_H	Data Hold Time After Clock Falls	10			ns	
t_{WLE}	Width of Latch Enable Pulse	62			ns	
t_{DLE}	LE Delay Time Falling Edge of Clock	25			ns	
t_{SLE}	LE Setup Time Before Falling Edge of Clock	30			ns	
t_D	Delay Time from V_{PP} Low Until Change in LE, $\overline{POL}$, $\overline{BL}$ Is Allowed	100			ns	
t_{SL}	Setup Time from Falling Edge $\overline{LE}$ to V_{PP} Rise	200			ns	
t_{SB}	Setup Time from $\overline{BL}$ Selected to V_{PP} Rise	150			ns	
t_{SP}	Setup Time from $\overline{POL}$ Selected to V_{PP} Rise	100			ns	
t_{DHL}	Delay Time Clock to Data High to Low			100	ns	
t_{DLK}	Delay Time Clock to Data Low to High			100	ns	

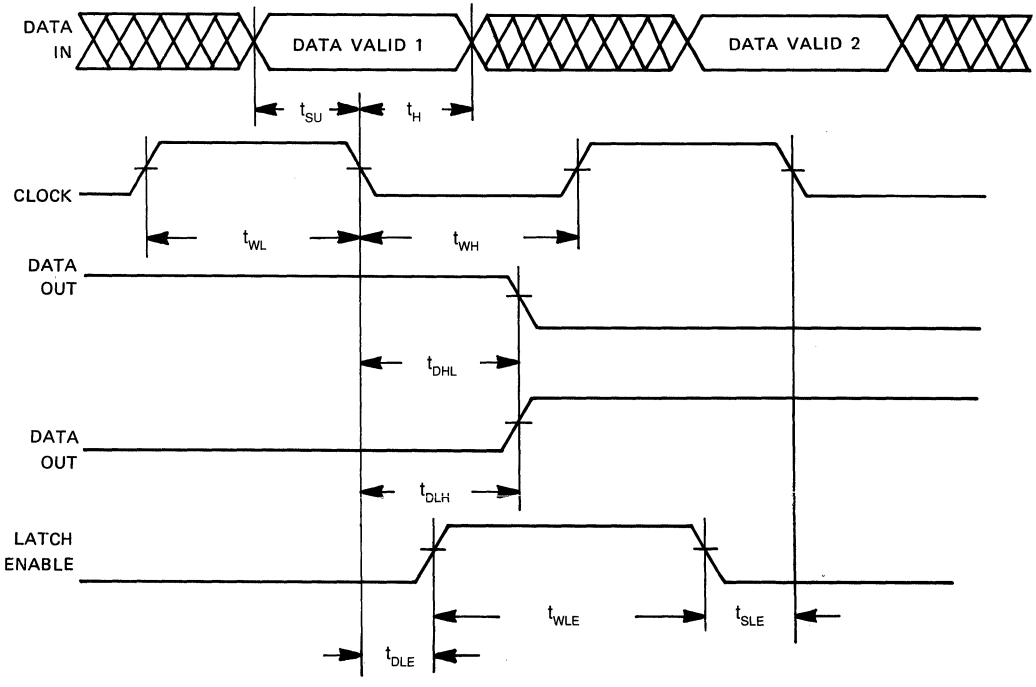
Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{DD}	Logic supply voltage		10.8	12	13.2	V
V_{PP}	High voltage supply	HV0320/HV0520	-0.3		200	V
		HV0330/HV0530	-0.3		300	V
V_{IH}	High-level input voltage		V_{DD} - 2V		V_{DD}	V
V_{IL}	Low-level input voltage		0		2.0	V
dV/dt	V_{PP} ramp rate				80	V/µs
T_A	Operating free-air temperature		-40		+85	°C

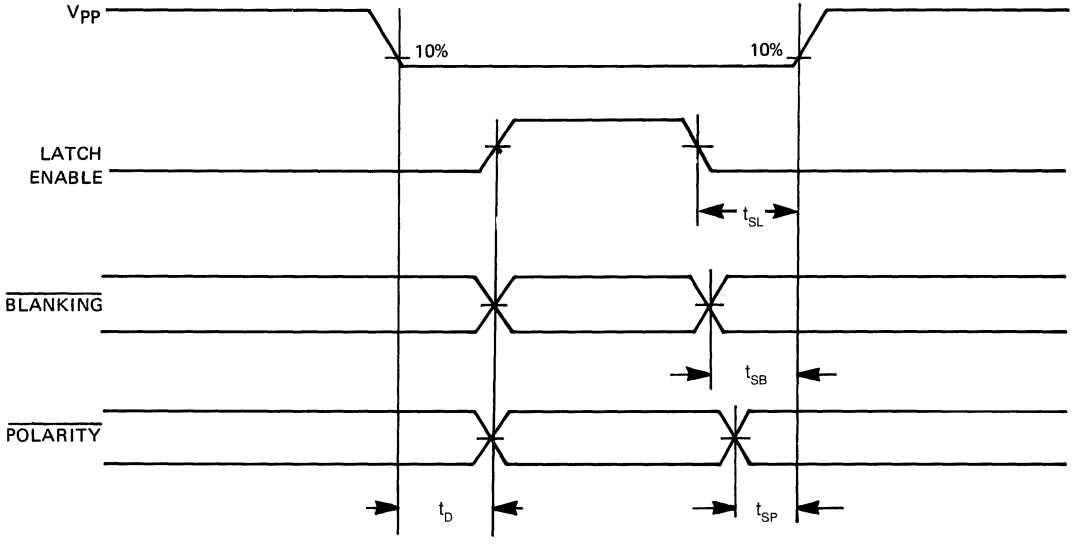
Input and Output Equivalent Circuit



Switching Waveforms

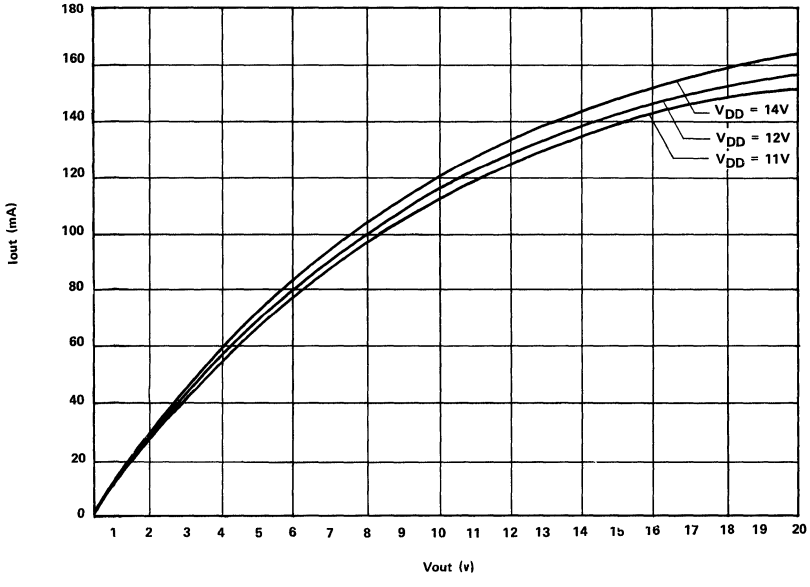


Output Control Waveforms

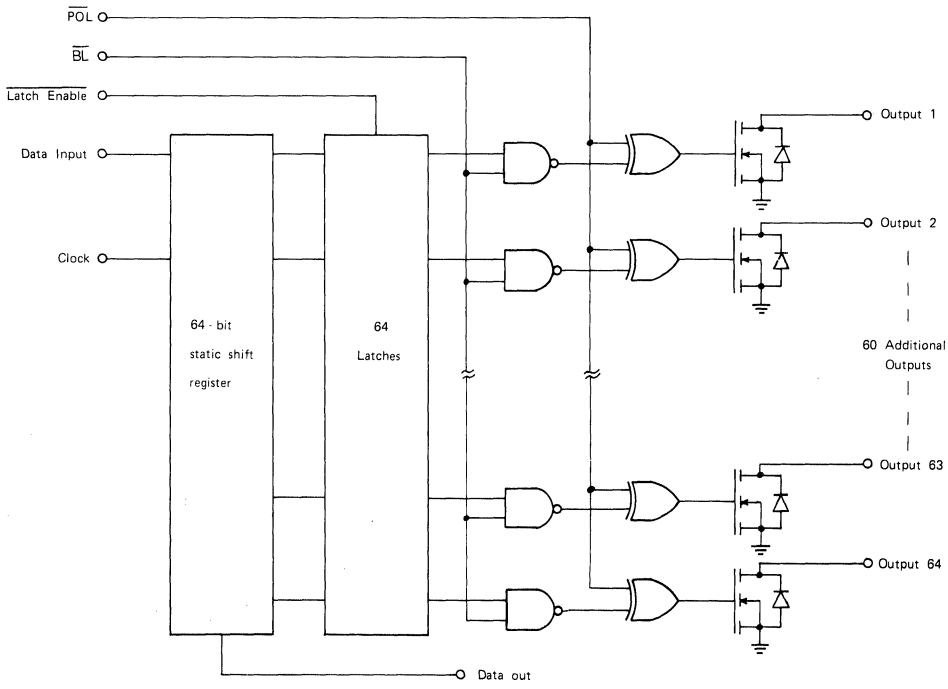


Typical Operating Conditions

SINK CURRENT @ 25C



Functional Block Diagram



Function Table

Function	Inputs					Outputs			
	DI	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1 2.....64	Latch 1 2.....64	HV Outputs 1 2.....64	Data Out
All on	X	X	X	L	L	* *..... *	* *..... *	L L..... L	*
All off	X	X	X	L	H	* *..... *	* *..... *	H H..... H	*
Invert mode	X	X	L	H	L	* *..... *	* *..... *	$\overline{*}$ $\overline{*}$..... $\overline{*}$	*
Load S/R	HorL	↓	L	H	H	HorL *..... *	* *..... *	* *..... *	*
Load latches	X	X	H	X	X	* *..... *	* *..... *	* *..... *	*
Transparent Latch mode	L	↓	H	H	H	L *..... *	L *..... *	H *..... *	*
	H	↓	H	H	H	H *..... *	H *..... *	L *..... *	*

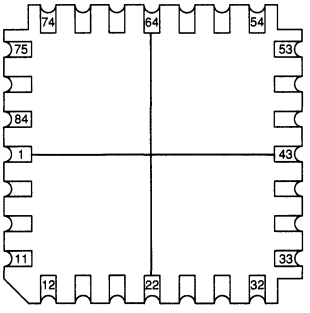
X = Don't care
* = Dependent on previous stage's state before the last CLK : or last LE high
↓ = High to low transition
H = High level
L = Low level

Pin Configurations

PJ and LC Packages

HV03				HV05			
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	V_{DD}	43	HVout 33	1	V_{DD}	43	HVout 32
2	$\overline{LE}$	44	HVout 34	2	$\overline{LE}$	44	HVout 31
3	Data In	45	HVout 35	3	Data In	45	HVout 30
4	$\overline{BL}$	46	HVout 36	4	$\overline{BL}$	46	HVout 29
5	HVout 1	47	HVout 37	5	HVout 64	47	HVout 28
6	HVout 2	48	HVout 38	6	HVout 63	48	HVout 27
7	HVout 3	49	HVout 39	7	HVout 62	49	HVout 26
8	HVout 4	50	HVout 40	8	HVout 61	50	HVout 25
9	HVout 5	51	HVout 41	9	HVout 60	51	HVout 24
10	HVout 6	52	HVout 42	10	HVout 59	52	HVout 23
11	N/C	53	N/C	11	N/C	53	N/C
12	GND	54	GND	12	GND	54	GND
13	GND	55	GND	13	GND	55	GND
14	HVout 7	56	HVout 43	14	HVout 58	56	HVout 22
15	HVout 8	57	HVout 44	15	HVout 57	57	HVout 21
16	HVout 9	58	HVout 45	16	HVout 56	58	HVout 20
17	HVout 10	59	HVout 46	17	HVout 55	59	HVout 19
18	HVout 11	60	HVout 47	18	HVout 54	60	HVout 18
19	HVout 12	61	HVout 48	19	HVout 53	61	HVout 17
20	HVout 13	62	HVout 49	20	HVout 52	62	HVout 16
21	HVout 14	63	HVout 50	21	HVout 51	63	HVout 15
22	HVout 15	64	HVout 51	22	HVout 50	64	HVout 14
23	HVout 16	65	HVout 52	23	HVout 49	65	HVout 13
24	HVout 17	66	HVout 53	24	HVout 48	66	HVout 12
25	HVout 18	67	HVout 54	25	HVout 47	67	HVout 11
26	HVout 19	68	HVout 55	26	HVout 46	68	HVout 10
27	HVout 20	69	HVout 56	27	HVout 45	69	HVout 9
28	HVout 21	70	HVout 57	28	HVout 44	70	HVout 8
29	HVout 22	71	HVout 58	29	HVout 43	71	HVout 7
30	GND	72	GND	30	GND	72	GND
31	GND	73	GND	31	GND	73	GND
32	N/C	74	N/C	32	N/C	74	N/C
33	HVout 23	75	HVout 59	33	HVout 42	75	HVout 6
34	HVout 24	76	HVout 60	34	HVout 41	76	HVout 5
35	HVout 25	77	HVout 61	35	HVout 40	77	HVout 4
36	HVout 26	78	HVout 62	36	HVout 39	78	HVout 3
37	HVout 27	79	HVout 63	37	HVout 38	79	HVout 2
38	HVout 28	80	HVout 64	38	HVout 37	80	HVout 1
39	HVout 29	81	$\overline{POL}$	39	HVout 36	81	$\overline{POL}$
40	HVout 30	82	Data Out	40	HVout 35	82	Data Out
41	HVout 31	83	CLK	41	HVout 34	83	CLK
42	HVout 32	84	GND	42	HVout 33	84	GND

Package Outline



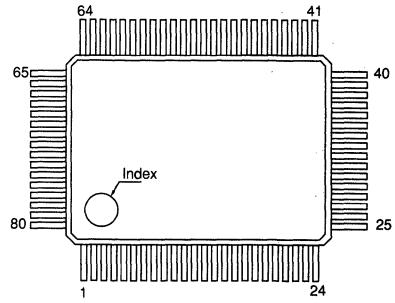
84-Pin Ceramic LCC

Pin Configurations

PG and DG Packages

HV03				HV05			
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	GND	41	GND	1	GND	41	GND
2	GND	42	GND	2	GND	42	GND
3	HVout 59	43	HVout 23	3	HVout 6	43	HVout 42
4	HVout 60	44	HVout 24	4	HVout 5	44	HVout 41
5	HVout 61	45	HVout 25	5	HVout 4	45	HVout 40
6	HVout 62	46	HVout 26	6	HVout 3	46	HVout 39
7	HVout 63	47	HVout 27	7	HVout 2	47	HVout 38
8	HVout 64	48	HVout 28	8	HVout 1	48	HVout 37
9	POL	49	HVout 29	9	POL	49	HVout 36
10	Data Out	50	HVout 30	10	Data Out	50	HVout 35
11	CLK	51	HVout 31	11	CLK	51	HVout 34
12	GND	52	HVout 32	12	GND	52	HVout 33
13	V_{DD}	53	HVout 33	13	V_{DD}	53	HVout 32
14	LE	54	HVout 34	14	LE	54	HVout 31
15	Data In	55	HVout 35	15	Data In	55	HVout 30
16	$\overline{BL}$	56	HVout 36	16	$\overline{BL}$	56	HVout 29
17	HVout 1	57	HVout 37	17	HVout 64	57	HVout 28
18	HVout 2	58	HVout 38	18	HVout 63	58	HVout 27
19	HVout 3	59	HVout 39	19	HVout 62	59	HVout 26
20	HVout 4	60	HVout 40	20	HVout 61	60	HVout 25
21	HVout 5	61	HVout 41	21	HVout 60	61	HVout 24
22	HVout 6	62	HVout 42	22	HVout 59	62	HVout 23
23	GND	63	GND	23	GND	63	GND
24	GND	64	GND	24	GND	64	GND
25	HVout 7	65	HVout 43	25	HVout 58	65	HVout 22
26	HVout 8	66	HVout 44	26	HVout 57	66	HVout 21
27	HVout 9	67	HVout 45	27	HVout 56	67	HVout 20
28	HVout 10	68	HVout 46	28	HVout 55	68	HVout 19
29	HVout 11	69	HVout 47	29	HVout 54	69	HVout 18
30	HVout 12	70	HVout 48	30	HVout 53	70	HVout 17
31	HVout 13	71	HVout 49	31	HVout 52	71	HVout 16
32	HVout 14	72	HVout 50	32	HVout 51	72	HVout 15
33	HVout 15	73	HVout 51	33	HVout 50	73	HVout 14
34	HVout 16	74	HVout 52	34	HVout 49	74	HVout 13
35	HVout 17	75	HVout 53	35	HVout 48	75	HVout 12
36	HVout 18	76	HVout 54	36	HVout 47	76	HVout 11
37	HVout 19	77	HVout 55	37	HVout 46	77	HVout 10
38	HVout 20	78	HVout 56	38	HVout 45	78	HVout 9
39	HVout 21	79	HVout 57	39	HVout 44	79	HVout 8
40	HVout 22	80	HVout 58	40	HVout 43	80	HVout 7

Package Outline



top view

80-pin Gullwing Package

64-Channel Serial To Parallel Converter With High Voltage CMOS Outputs

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options					
		84-Pad Ceramic Leadless Chip Carrier	84-J Lead Plastic Chip Carrier	80-Lead Quad Cerpak Gullwing	80-Lead Quad Plastic Gullwing	80-Lead 35mm TAB Tape	Die
HV04	60V	HV0406LC	HV0406PJ	HV0406DG	HV0406PG	HV0406T	HV0406X
	80V	HV0408LC	HV0408PJ	HV0408DG	HV0408PG	HV0408T	HV0408X
HV06	60V	HV0606LC	HV0606PJ	HV0606DG	HV0606PG	HV0606T	HV0606X
	80V	HV0608LC	HV0608PJ	HV0608DG	HV0608PG	HV0608T	HV0608X

Features

- ☐ HVCMOS® Technology
- ☐ Output voltages up to 90V using a ramped supply
- ☐ Low power level shifting
- ☐ Source/sink current minimum 20 mA
- ☐ Shift register speed 8 MHz
- ☐ Latched data outputs
- ☐ Output polarity and blanking
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}	-0.5V to +15V
Supply voltage, V_{PP}[2]	-0.5V to +90V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current[3]	3.0A
High voltage supply current[3]	2.6A
Continuous total power dissipation[4]	1900mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Notes: 1. All voltages are referenced to V_{SS}.
2. These devices have been designed to be used in applications which either switch the V_{PP} supply to ground before changing the state of the high voltage outputs or limit the current through each output.
3. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

General Description

The HV04 and HV06 are low voltage serial to high voltage parallel converters with push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. HVout1 is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the low to high transition of the clock. The HV04 shifts in the counterclockwise direction when viewed from the top of the package and the HV06 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HVout64). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

The HV04 and HV06 have been designed to be used in systems which either switch off the high voltage supply before changing the state of the high voltage outputs or limit the current through each output.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current				25	mA	f_{CLK} = 8MHz, f_{DATA} = 4MHz $\overline{LE}$ = LOW
I_{DDQ}	Quiescent V_{DD} Supply Current				0.25	mA	All V_{IN} = 0V
I_{PP}	High Voltage Supply Current				0.50	mA	V_{PP} = 80V All outputs high
					0.50	mA	V_{PP} = 80V All outputs low
I_{IH}	High-Level Logic Input Current				10	µA	V_{IH} = V_{DD}
I_{IL}	Low-Level Logic Input Current		-10			µA	V_I = 0V
V_{OH}	High-Level Output	HV_{OUT}	74			V	V_{PP} = 80V, IHV_{OUT} = -20mA
		Data Out	V_{DD} - 1V			V	ID_{OUT} = -100µA
V_{OL}	Low-Level Output	HV_{OUT}			6	V	V_{PP} = 80V, IHV_{OUT} = +20mA
		Data Out			1	V	ID_{OUT} = +100µA
V_{OC}	HV_{OUT} Clamp Voltage				V_{PP} + 1.5	V	I_{OL} = +20mA
					-1.5	V	I_{OL} = -20mA

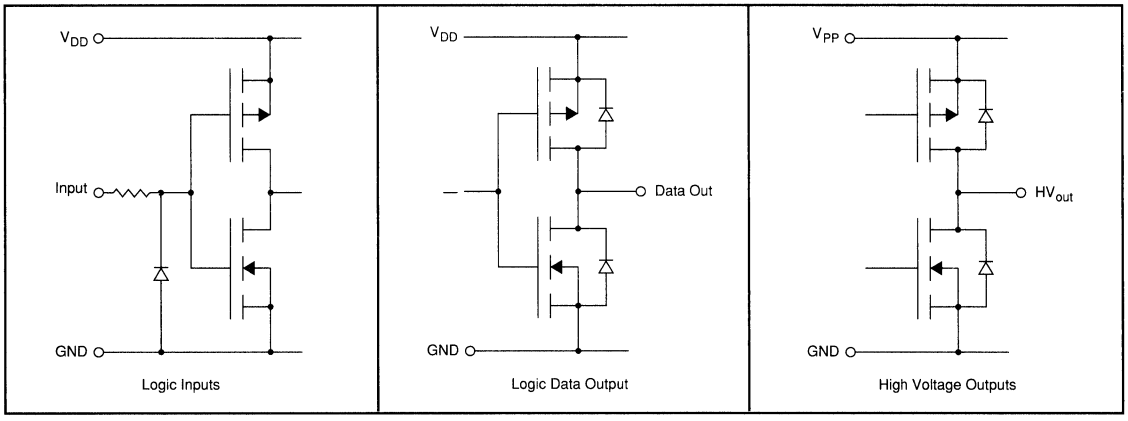
AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency			8	MHz	
t_W	Clock Width High or Low	62			ns	
t_{SU}	Data Setup Time Before Clock Rises	25			ns	
t_H	Data Hold Time After Clock Rises	10			ns	
t_{WLE}	Width of Latch Enable Pulse	62			ns	
t_{DLE}	$\overline{LE}$ Delay Time Rising Edge of Clock	25			ns	
t_{SLE}	$\overline{LE}$ Setup Time Before Rising Edge of Clock	30			ns	
t_D	Delay Time from V_{PP} Low Until Change in $\overline{LE}$, $\overline{POL}$, $\overline{BL}$ Is Allowed	100			ns	
t_{SL}	Setup Time from $\overline{LE}$ Rise to V_{PP} Rise	200			ns	
t_{SB}	Setup Time from $\overline{BL}$ Selected to V_{PP} Rise	150			ns	
t_{SP}	Setup Time from $\overline{POL}$ Selected to V_{PP} Rise	100			ns	
t_{DHL}	Delay Time Clock to Data High to Low			100	ns	
t_{DLH}	Delay Time Clock to Data Low to High			100	ns	

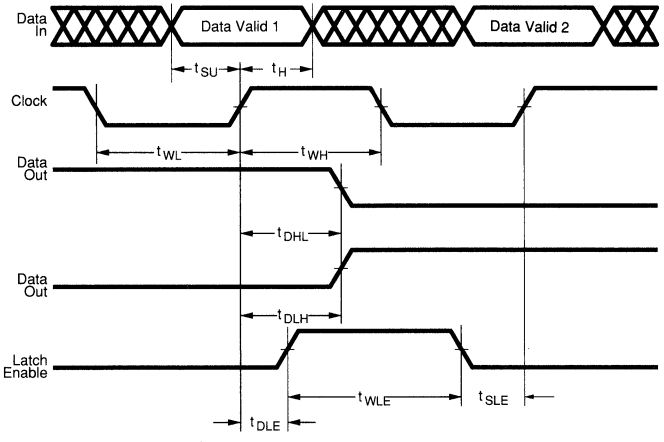
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	10.8	12	13.2	V
V_{PP}	High voltage supply	-0.3		80	V
V_{IH}	High-level input voltage	V_{DD} - 2V		V_{DD}	V
V_{IL}	Low-level input voltage	0		2.0	V
dV/dt	V_{PP} ramp rate			80	V/µs
T_A	Operating free-air temperature	-40		+85	°C

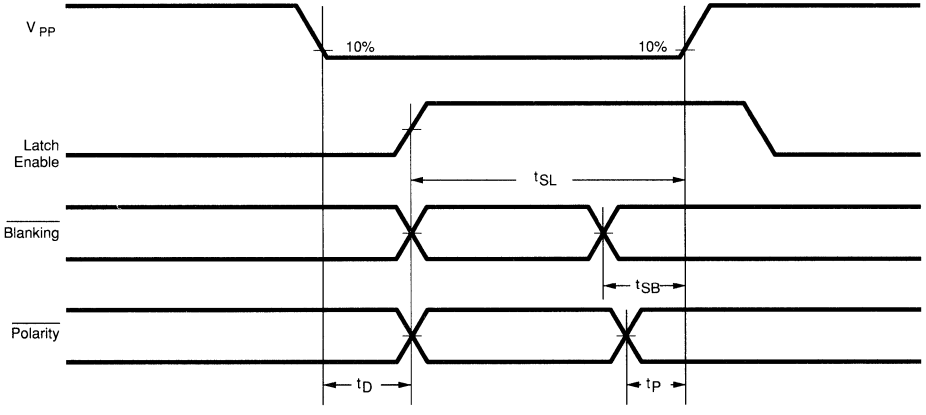
Input and Output Equivalent Circuits



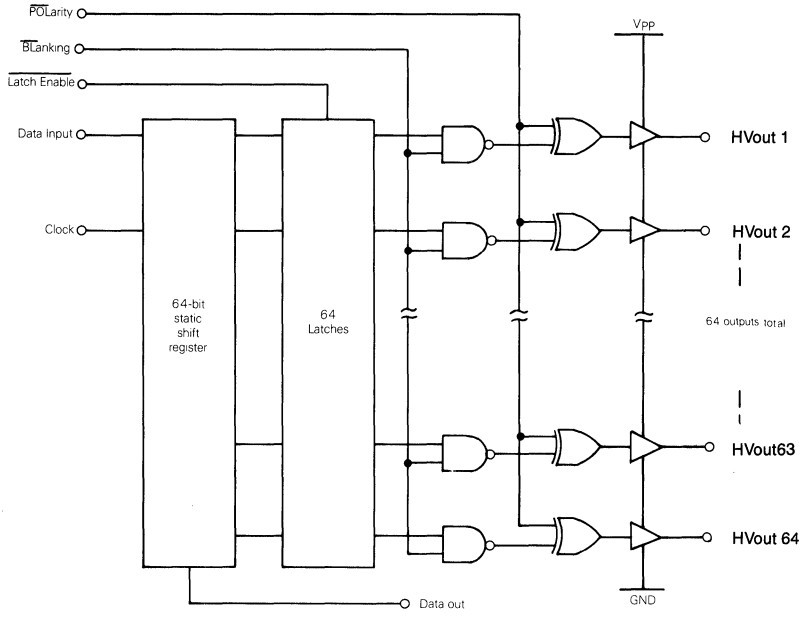
Switching Waveforms



Output Control Waveforms



Functional Block Diagram



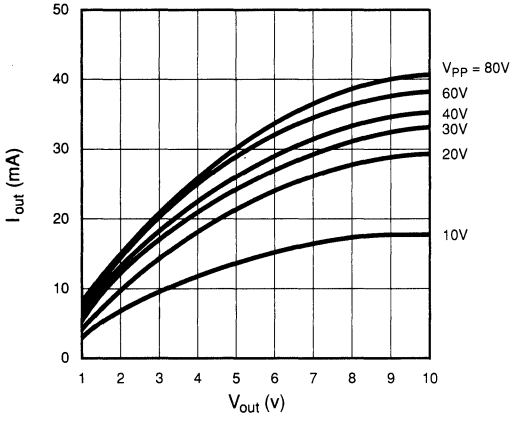
Function Table

Function	Inputs					Outputs		
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1 2...64	HV Outputs 1 2...64	Data Out *
All on	X	X	X	L	L	* *...*	H H...H	*
All off	X	X	X	L	H	* *...*	L L...L	*
Invert mode	X	X	L	H	L	* *...*	$\overline{*}$ $\overline{*...*}$	*
Load S/R	H or L	↑	L	H	H	H or L *...*	* *...*	*
Load Latches	X	H or L	↑	H	H	* *...*	* *...*	*
	X	H or L	↑	H	L	* *...*	$\overline{*}$ $\overline{*...*}$	*
Transparent Latch mode	L	↑	H	H	H	L *...*	L *...*	*
	H	↑	H	H	H	H *...*	H *...*	*

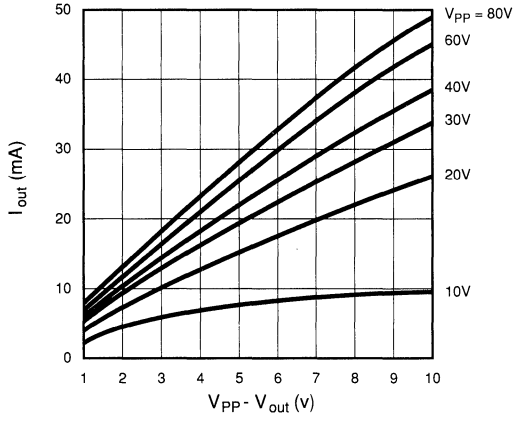
Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
* = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high,

Typical Performance Curves

Typical HV04/06 Sink Current @ 25°C



Typical HV04H/06H Source Current @ 25° C

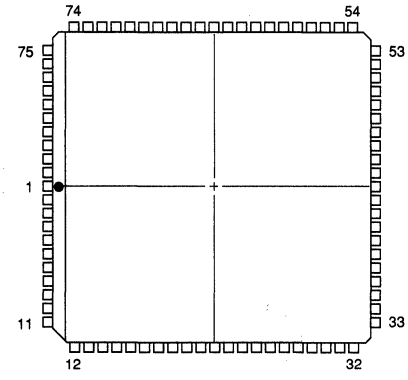


Pin Configurations

PJ and LC Packages

HV04				HV06			
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	V_{DD}	43	HVout 33	1	V_{DD}	43	HVout 32
2	$\overline{LE}$	44	HVout 34	2	$\overline{LE}$	44	HVout 31
3	Data in	45	HVout 35	3	Data in	45	HVout 30
4	$\overline{BL}$	46	HVout 36	4	$\overline{BL}$	46	HVout 29
5	HVout 1	47	HVout 37	5	HVout 64	47	HVout 28
6	HVout 2	48	HVout 38	6	HVout 63	48	HVout 27
7	HVout 3	49	HVout 39	7	HVout 62	49	HVout 26
8	HVout 4	50	HVout 40	8	HVout 61	50	HVout 25
9	HVout 5	51	HVout 41	9	HVout 60	51	HVout 24
10	HVout 6	52	HVout 42	10	HVout 59	52	HVout 23
11	N/C	53	N/C	11	N/C	53	N/C
12	V_{PP}	54	V_{PP}	12	V_{PP}	54	V_{PP}
13	GND	55	GND	13	GND	55	GND
14	HVout 7	56	HVout 43	14	HVout 58	56	HVout 22
15	HVout 8	57	HVout 44	15	HVout 57	57	HVout 21
16	HVout 9	58	HVout 45	16	HVout 56	58	HVout 20
17	HVout 10	59	HVout 46	17	HVout 55	59	HVout 19
18	HVout 11	60	HVout 47	18	HVout 54	60	HVout 18
19	HVout 12	61	HVout 48	19	HVout 53	61	HVout 17
20	HVout 13	62	HVout 49	20	HVout 52	62	HVout 16
21	HVout 14	63	HVout 50	21	HVout 51	63	HVout 15
22	HVout 15	64	HVout 51	22	HVout 50	64	HVout 14
23	HVout 16	65	HVout 52	23	HVout 49	65	HVout 13
24	HVout 17	66	HVout 53	24	HVout 48	66	HVout 12
25	HVout 18	67	HVout 54	25	HVout 47	67	HVout 11
26	HVout 19	68	HVout 55	26	HVout 46	68	HVout 10
27	HVout 20	69	HVout 56	27	HVout 45	69	HVout 9
28	HVout 21	70	HVout 57	28	HVout 44	70	HVout 8
29	HVout 22	71	HVout 58	29	HVout 43	71	HVout 7
30	GND	72	GND	30	GND	72	GND
31	V_{PP}	73	V_{PP}	31	V_{PP}	73	V_{PP}
32	N/C	74	N/C	32	N/C	74	N/C
33	HVout 23	75	HVout 59	33	HVout 42	75	HVout 6
34	HVout 24	76	HVout 60	34	HVout 41	76	HVout 5
35	HVout 25	77	HVout 61	35	HVout 40	77	HVout 4
36	HVout 26	78	HVout 62	36	HVout 39	78	HVout 3
37	HVout 27	79	HVout 63	37	HVout 38	79	HVout 2
38	HVout 28	80	HVout 64	38	HVout 37	80	HVout 1
39	HVout 29	81	$\overline{POL}$	39	HVout 36	81	$\overline{POL}$
40	HVout 30	82	Data Out	40	HVout 35	82	Data Out
41	HVout 31	83	CLK	41	HVout 34	83	CLK
42	HVout 32	84	GND	42	HVout 33	84	GND

Package Outline



top view

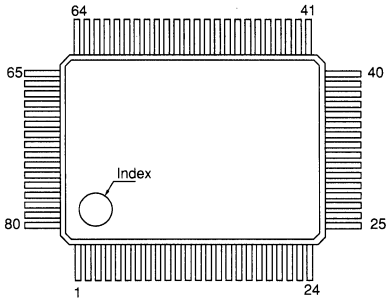
84-pin J-lead Package

Pin Configurations

PG and DG Packages

HV04				HV06			
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	GND	41	GND	1	GND	41	GND
2	V_{PP}	42	V_{PP}	2	V_{PP}	42	V_{PP}
3	HVout 59	43	HVout 23	3	HVout 6	43	HVout 42
4	HVout 60	44	HVout 24	4	HVout 5	44	HVout 41
5	HVout 61	45	HVout 25	5	HVout 4	45	HVout 40
6	HVout 62	46	HVout 26	6	HVout 3	46	HVout 39
7	HVout 63	47	HVout 27	7	HVout 2	47	HVout 38
8	HVout 64	48	HVout 28	8	HVout 1	48	HVout 37
9	$\overline{POL}$	49	HVout 29	9	$\overline{POL}$	49	HVout 36
10	Data Out	50	HVout 30	10	Data Out	50	HVout 35
11	CLK	51	HVout 31	11	CLK	51	HVout 34
12	GND	52	HVout 32	12	GND	52	HVout 33
13	V_{DD}	53	HVout 33	13	V_{DD}	53	HVout 32
14	$\overline{LE}$	54	HVout 34	14	$\overline{LE}$	54	HVout 31
15	Data In	55	HVout 35	15	Data In	55	HVout 30
16	$\overline{BL}$	56	HVout 36	16	$\overline{BL}$	56	HVout 29
17	HVout 1	57	HVout 37	17	HVout 64	57	HVout 28
18	HVout 2	58	HVout 38	18	HVout 63	58	HVout 27
19	HVout 3	59	HVout 39	19	HVout 62	59	HVout 26
20	HVout 4	60	HVout 40	20	HVout 61	60	HVout 25
21	HVout 5	61	HVout 41	21	HVout 60	61	HVout 24
22	HVout 6	62	HVout 42	22	HVout 59	62	HVout 23
23	V_{PP}	63	V_{PP}	23	V_{PP}	63	V_{PP}
24	GND	64	GND	24	GND	64	GND
25	HVout 7	65	HVout 43	25	HVout 58	65	HVout 22
26	HVout 8	66	HVout 44	26	HVout 57	66	HVout 21
27	HVout 9	67	HVout 45	27	HVout 56	67	HVout 20
28	HVout 10	68	HVout 46	28	HVout 55	68	HVout 19
29	HVout 11	69	HVout 47	29	HVout 54	69	HVout 18
30	HVout 12	70	HVout 48	30	HVout 53	70	HVout 17
31	HVout 13	71	HVout 49	31	HVout 52	71	HVout 16
32	HVout 14	72	HVout 50	32	HVout 51	72	HVout 15
33	HVout 15	73	HVout 51	33	HVout 50	73	HVout 14
34	HVout 16	74	HVout 52	34	HVout 49	74	HVout 13
35	HVout 17	75	HVout 53	35	HVout 48	75	HVout 12
36	HVout 18	76	HVout 54	36	HVout 47	76	HVout 11
37	HVout 19	77	HVout 55	37	HVout 46	77	HVout 10
38	HVout 20	78	HVout 56	38	HVout 45	78	HVout 9
39	HVout 21	79	HVout 57	39	HVout 44	79	HVout 8
40	HVout 22	80	HVout 58	40	HVout 43	80	HVout 7

Package Outline



top view

80-pin Gullwing Package

64-Channel Serial To Parallel Converter With Ruggedized High Voltage CMOS Outputs

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options					
		84-Pad Ceramic Leadless Chip Carrier	84-J Lead Plastic Chip Carrier	80-Lead Quad Cerpak Gullwing	80-Lead Quad Plastic Gullwing	80-Lead 35mm TAB Tape	Die
HV04H	60V	HV04H06LC	HV04H06PJ	HV04H06DG	HV04H06PG	HV04H06T	HV04H06X
	80V	HV04H08LC	HV04H08PJ	HV04H08DG	HV04H08PG	HV04H08T	HV04H08X
HV06H	60V	HV06H06LC	HV06H06PJ	HV06H06DG	HV06H06PG	HV06H06T	HV06H06X
	80V	HV06H08LC	HV06H08PJ	HV06H08DG	HV06H08PG	HV06H08T	HV06H08X

Features

- ☐ HVCMOS® Technology
- ☐ Output voltages up to 80V
- ☐ Low power level shifting
- ☐ Shift register speed 8 MHz
- ☐ Latched data outputs
- ☐ Output polarity and blanking
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}	-0.5V to +15V
Supply voltage, V_{PP}[2]	-0.5V to +80V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current[3]	3.0A
High voltage supply current[3]	2.6A
Continuous total power dissipation[4]	1900mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Notes: 1. All voltages are referenced to ground.
2. These devices have been designed to be used in applications which either switch the V_{PP} supply to ground before changing the state of the high voltage outputs or limit the current through each output.
3. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

General Description

The HV04H and HV06H are low voltage serial to high voltage parallel converters with push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. HVout1 is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the low to high transition of the clock. The HV04H shifts data in the counterclockwise direction when viewed from the top of the package and the HV06H shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HVout64). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) is high. The data in the latch is stored when $\overline{LE}$ is low.

The HV04H and HV06H devices are ruggedized versions of our standard HV04 and HV06. They are designed to be used in circuits where ramping of the high voltage supply is not feasible. Care must be taken to limit the load capacitance and surge current in any particular application.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current				25	mA	f_{CLK} = 8MHz, f_{DATA} = 4MHz LE = LOW
I_{DDQ}	Quiescent V_{DD} Supply Current				0.25	mA	All V_{IN} = 0V or V_{DD}
I_{PP}	High Voltage Supply Current				0.50	mA	V_{PP} = 80V All outputs high
					0.50	mA	V_{PP} = 80V All outputs low
I_{IH}	High-Level Logic Input Current				10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-Level Logic Input Current		-10			µA	V_{IL} = 0V
V_{OH}	High-Level Output	HV_{OUT}	74			V	V_{PP} = 80V, IHV_{OUT} = -20mA
		Data Out	V_{DD} - 1V			V	ID_{OUT} = -100µA
V_{OL}	Low-Level Output	HV_{OUT}			6.0	V	V_{PP} = 80V, IHV_{OUT} = +10mA
		Data Out			1.0	V	ID_{OUT} = +100µA
V_{OC}	HV_{OUT} Clamp Voltage				V_{PP} + 1.5 -1.5	V V	I_{OL} = +20mA I_{OL} = -20mA

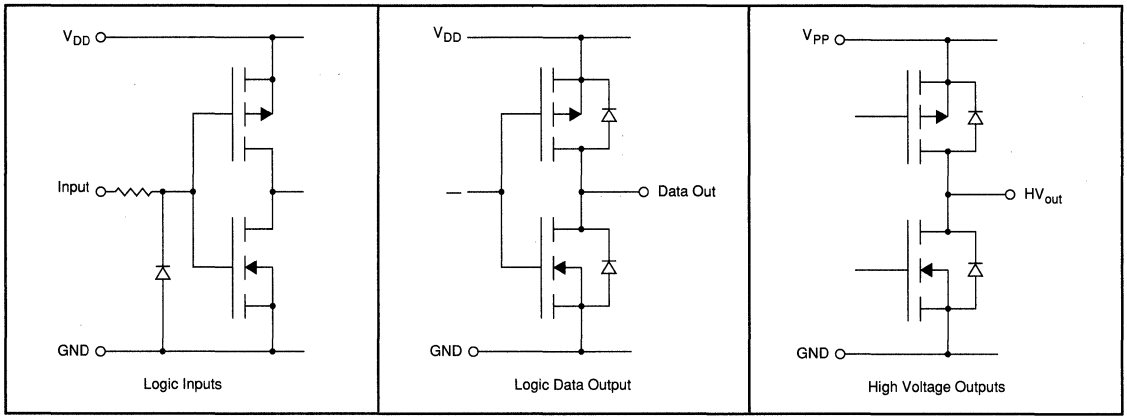
AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency			8	MHz	
t_W	Clock Width High or Low	62			ns	
t_{SU}	Data Setup Time Before Clock Rises	25			ns	
t_H	Data Hold Time After Clock Rises	10			ns	
t_{WLE}	Width of Latch Enable Pulse	62			ns	
t_{DLE}	$\overline{LE}$ Delay Time Rising Edge of Clock	25			ns	
t_{SLE}	$\overline{LE}$ Setup Time Before Rising Edge of Clock	30			ns	
t_{ON}, t_{OFF}	Time from Latch Enable to HV_{OUT}			500	µs	
t_{DHL}	Delay Time Clock to Data High to Low			100	ns	
t_{DLH}	Delay Time Clock to Data Low to High			100	ns	

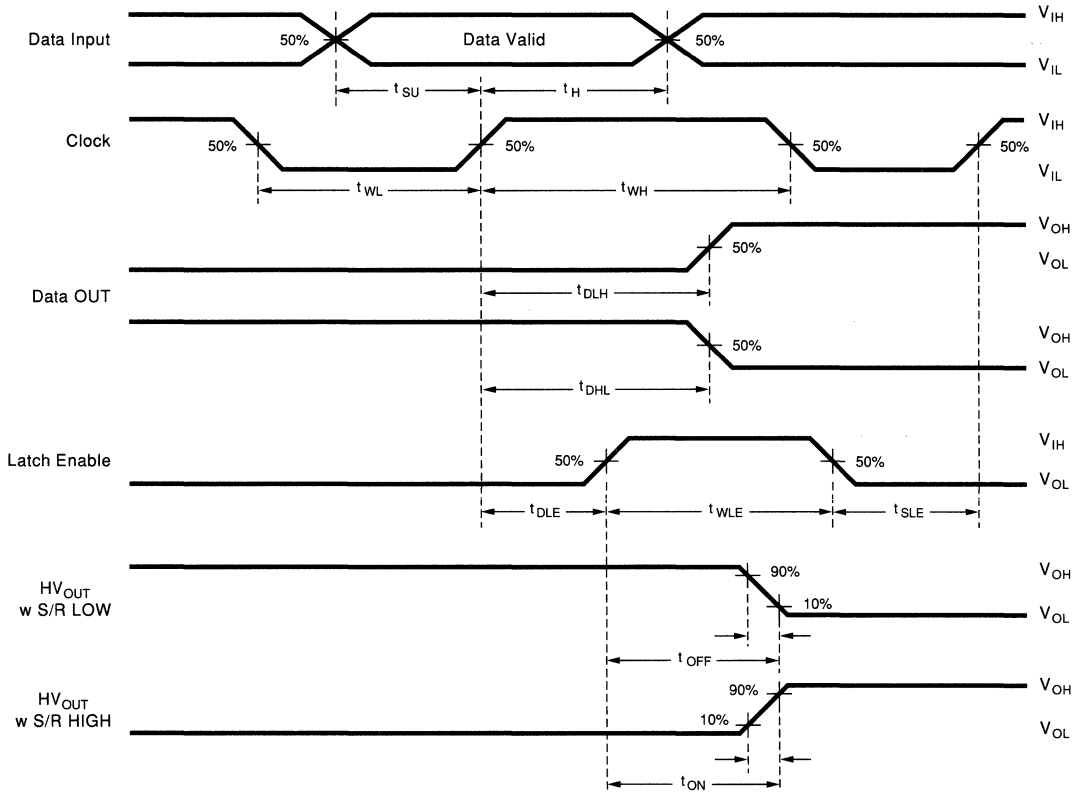
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	10.8	12	13.2	V
V_{PP}	High voltage supply	-0.3		80	V
V_{IH}	High-level input voltage	V_{DD} - 2V		V_{DD}	V
V_{IL}	Low-level input voltage	0		2.0	V
dV/dt	V_{PP} ramp rate			80	V/µs
T_A	Operating free-air temperature	-40		+85	°C

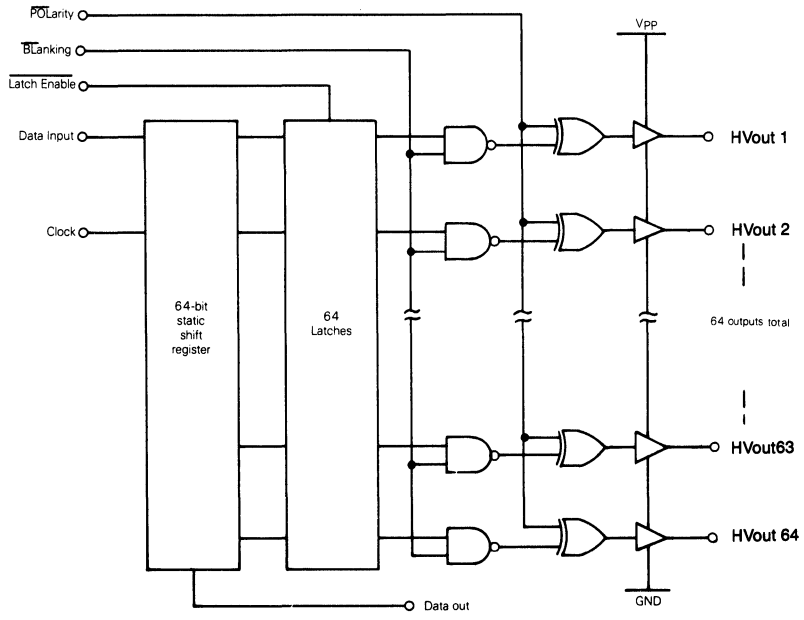
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



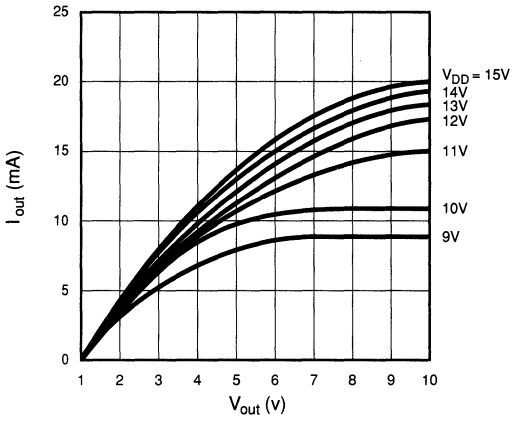
Function Table

Function	Inputs					Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1	Shift Reg 2...64	HV Outputs 1	HV Outputs 2...64	Data Out *
All on	X	X	X	L	L	*	*...*	H	H...H	*
All off	X	X	X	L	H	*	*...*	L	L...L	*
Invert mode	X	X	L	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Load S/R	H or L	↑	L	H	H	H or L	*...*	*	*...*	*
Load Latches	X	H or L	↑	H	H	*	*...*	*	*...*	*
	X	H or L	↑	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Transparent Latch mode	L	↑	H	H	H	L	*...*	L	*...*	*
	H	↑	H	H	H	H	*...*	H	*...*	*

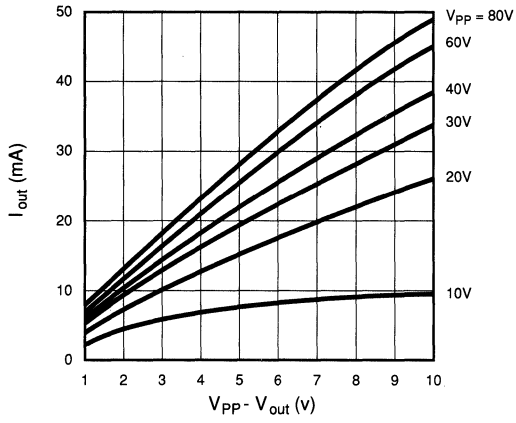
Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
* = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high,

Typical Performance Curves

Typical HV04H/06H Source Current @ 25° C



Typical HV04H/06H Source Current @ 25° C

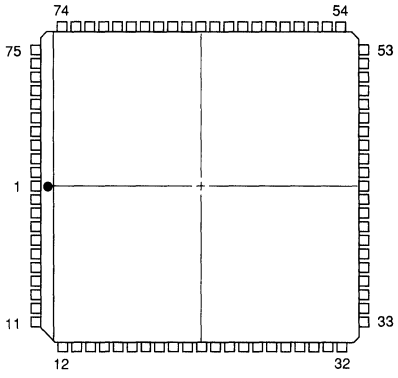


Pin Configurations

PJ and LC Packages

HV04H				HV06H			
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	V_{DD}	43	HVout 33	1	V_{DD}	43	HVout 32
2	$\overline{LE}$	44	HVout 34	2	$\overline{LE}$	44	HVout 31
3	Data in	45	HVout 35	3	Data in	45	HVout 30
4	$\overline{BL}$	46	HVout 36	4	$\overline{BL}$	46	HVout 29
5	HVout 1	47	HVout 37	5	HVout 64	47	HVout 28
6	HVout 2	48	HVout 38	6	HVout 63	48	HVout 27
7	HVout 3	49	HVout 39	7	HVout 62	49	HVout 26
8	HVout 4	50	HVout 40	8	HVout 61	50	HVout 25
9	HVout 5	51	HVout 41	9	HVout 60	51	HVout 24
10	HVout 6	52	HVout 42	10	HVout 59	52	HVout 23
11	N/C	53	N/C	11	N/C	53	N/C
12	V_{PP}	54	V_{PP}	12	V_{PP}	54	V_{PP}
13	GND	55	GND	13	GND	55	GND
14	HVout 7	56	HVout 43	14	HVout 58	56	HVout 22
15	HVout 8	57	HVout 44	15	HVout 57	57	HVout 21
16	HVout 9	58	HVout 45	16	HVout 56	58	HVout 20
17	HVout 10	59	HVout 46	17	HVout 55	59	HVout 19
18	HVout 11	60	HVout 47	18	HVout 54	60	HVout 18
19	HVout 12	61	HVout 48	19	HVout 53	61	HVout 17
20	HVout 13	62	HVout 49	20	HVout 52	62	HVout 16
21	HVout 14	63	HVout 50	21	HVout 51	63	HVout 15
22	HVout 15	64	HVout 51	22	HVout 50	64	HVout 14
23	HVout 16	65	HVout 52	23	HVout 49	65	HVout 13
24	HVout 17	66	HVout 53	24	HVout 48	66	HVout 12
25	HVout 18	67	HVout 54	25	HVout 47	67	HVout 11
26	HVout 19	68	HVout 55	26	HVout 46	68	HVout 10
27	HVout 20	69	HVout 56	27	HVout 45	69	HVout 9
28	HVout 21	70	HVout 57	28	HVout 44	70	HVout 8
29	HVout 22	71	HVout 58	29	HVout 43	71	HVout 7
30	GND	72	GND	30	GND	72	GND
31	V_{PP}	73	V_{PP}	31	V_{PP}	73	V_{PP}
32	N/C	74	N/C	32	N/C	74	N/C
33	HVout 23	75	HVout 59	33	HVout 42	75	HVout 6
34	HVout 24	76	HVout 60	34	HVout 41	76	HVout 5
35	HVout 25	77	HVout 61	35	HVout 40	77	HVout 4
36	HVout 26	78	HVout 62	36	HVout 39	78	HVout 3
37	HVout 27	79	HVout 63	37	HVout 38	79	HVout 2
38	HVout 28	80	$\overline{HVout}$ 64	38	HVout 37	80	$\overline{HVout}$ 1
39	HVout 29	81	$\overline{POL}$	39	HVout 36	81	POL
40	HVout 30	82	Data Out	40	HVout 35	82	Data Out
41	HVout 31	83	CLK	41	HVout 34	83	CLK
42	HVout 32	84	GND	42	HVout 33	84	GND

Package Outline



top view

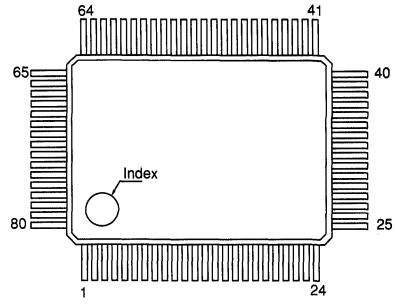
84-pin J-lead Package

Pin Configurations

PG and DG Packages

HV04H				HV06H			
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	GND	41	GND	1	GND	41	GND
2	V_{PP}	42	V_{PP}	2	V_{PP}	42	V_{PP}
3	HVout 59	43	HVout 23	3	HVout 6	43	HVout 42
4	HVout 60	44	HVout 24	4	HVout 5	44	HVout 41
5	HVout 61	45	HVout 25	5	HVout 4	45	HVout 40
6	HVout 62	46	HVout 26	6	HVout 3	46	HVout 39
7	HVout 63	47	HVout 27	7	HVout 2	47	HVout 38
8	HVout 64	48	HVout 28	8	HVout 1	48	HVout 37
9	$\overline{POL}$	49	HVout 29	9	$\overline{POL}$	49	HVout 36
10	Data Out	50	HVout 30	10	Data Out	50	HVout 35
11	CLK	51	HVout 31	11	CLK	51	HVout 34
12	GND	52	HVout 32	12	GND	52	HVout 33
13	V_{DD}	53	HVout 33	13	V_{DD}	53	HVout 32
14	$\overline{LE}$	54	HVout 34	14	$\overline{LE}$	54	HVout 31
15	Data Out	55	HVout 35	15	Data Out	55	HVout 30
16	$\overline{BL}$	56	HVout 36	16	$\overline{BL}$	56	HVout 29
17	HVout 1	57	HVout 37	17	HVout 64	57	HVout 28
18	HVout 2	58	HVout 38	18	HVout 63	58	HVout 27
19	HVout 3	59	HVout 39	19	HVout 62	59	HVout 26
20	HVout 4	60	HVout 40	20	HVout 61	60	HVout 25
21	HVout 5	61	HVout 41	21	HVout 60	61	HVout 24
22	HVout 6	62	HVout 42	22	HVout 59	62	HVout 23
23	V_{PP}	63	V_{PP}	23	V_{PP}	63	V_{PP}
24	GND	64	GND	24	GND	64	GND
25	HVout 7	65	HVout 43	25	HVout 58	65	HVout 22
26	HVout 8	66	HVout 44	26	HVout 57	66	HVout 21
27	HVout 9	67	HVout 45	27	HVout 56	67	HVout 20
28	HVout 10	68	HVout 46	28	HVout 55	68	HVout 19
29	HVout 12	69	HVout 47	29	HVout 54	69	HVout 18
30	HVout 13	70	HVout 48	30	HVout 53	70	HVout 17
31	HVout 14	71	HVout 49	31	HVout 52	71	HVout 16
32	HVout 15	72	HVout 50	32	HVout 51	72	HVout 15
33	HVout 16	73	HVout 51	33	HVout 50	73	HVout 14
34	HVout 17	74	HVout 52	34	HVout 49	74	HVout 13
35	HVout 18	75	HVout 53	35	HVout 48	75	HVout 12
36	HVout 19	76	HVout 54	36	HVout 47	76	HVout 11
37	HVout 20	77	HVout 55	37	HVout 46	77	HVout 10
38	HVout 21	78	HVout 56	38	HVout 45	78	HVout 9
39	HVout 22	79	HVout 57	39	HVout 44	79	HVout 8
40	HVout 23	80	HVout 58	40	HVout 43	80	HVout 7

Package Outline



top view

80-pin Gullwing Package

Advance Information

24-Channel Matrix TFEL Panel Display Column Driver

Ordering Information

Device	Package Options	
	44-Lead Ceramic J-Bend	Die
HV08	HV08DJ	HV08X

Features

- ☐ TTL-compatible imputs
- ☐ Up to 70V modulation voltage
- ☐ Capability of 16 levels of gray shading
- ☐ 6MHz data shift rate
- ☐ 24 Outputs per device (can be cascaded)
- ☐ Minimum 40mA high-voltage output source/sink capability
- ☐ Pin-programmable shift direction
- ☐ D/A conversion can be performed in as little as 3μS
- ☐ Diodes in output structure allow usage in energy recovery systems (non-gray shaded)
- ☐ Integrated high-voltage CMOS technology
- ☐ Available in 44-lead ceramic J-bend package or in die form

General Description

The HV08 is a 24-channel column driver IC designed for general purpose electroluminescent display use. Each channel of the HV08 consists of a 4-bit wide shift register, a 4-bit counter, and a high voltage sample and hold circuit to perform a D/A conversion to one of 16 arbitrary voltage levels. The output of each channel is buffered by a source-follower structure which allows both sourcing and sinking of output current.

DIR is a shift direction select pin which has been provided to allow the user to reverse shift direction between channels and to interchange the function of the shift register data input and output pins. When the DIR input is high, data is shifted in a clockwise direction. Data is accepted at pins I/01 through I/04 and output at O/I1 through O/I4. When the DIR input is low, data is shifted in a counterclockwise direction. Data is accepted at pins O/I1 through O/I4 and output at pins I/01 through I/04.

D/A conversion is accomplished by means of a high-voltage sample and hold circuit which is controlled by a 4-bit counter. For each channel, data is serially shifted through the (4-bit wide) shift register by the rising edge of SCLK. With the MODE signal high, the data in the shift register is transferred to a polynomial counter by the rising edge of CCLK. The mode signal is then brought low and the counter is down-counted to zero; again, the rising edge of CCLK. During the period that the counter is not zero, a sample switch is held closed which allows a storage capacitor to be charged to voltage at the V_R (ramp voltage) input to the device. The high voltage output also follows V_R during this period. When the counter reaches zero, the sample switch is opened. The output then holds at the value of V_R that was present when zero count occurred. A diode provides for the discharge of the storage capacitor once V_R is less than the voltage on the capacitor.

Electrical Characteristics

Low-Voltage DC Characteristics

Symbol	Parameter	Min	Typ[2]	Max	Units	Conditions
V_{DD}	Low-voltage supply	4.5	5.0	5.5	V	
I_{DD}	V_{DD} supply current (active)		6.0	10.0	mA	f_{SCLK} = 6MHz[1] f_{CCLK} = 6MHz F_{DATA} = 3MHz
I_{DDS}	V_{DD} supply current (standby)			1.0	mA	All V_{IN} = 0V
V_{IH}	High-level input voltage	2.4		V_{DD}	V	
V_{IL}	Low-level input voltage	0		0.8	V	
I_{IH}	High-level input current		1.0	50	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level input current		-1.0	-50	µA	V_{IL} = 0V
C_{IN}	Input capacitance (data, mode, SCLK, CCLK)			10	pF	V_{IN} = 0V, f = 1MHz
T_A	Operating free-air temperature	-55		125	C	
V_{OH}	High-level output voltage	2.8			V	I_{OH} = -4mA, V_{DD} = min
V_{OL}	Low-level output voltage			0.4	V	I_{OL} = 4mA, V_{DD} = min
I_{OH}	High-level output current			-4.0	mA	
I_{OL}	Low-level output current			4.0	mA	

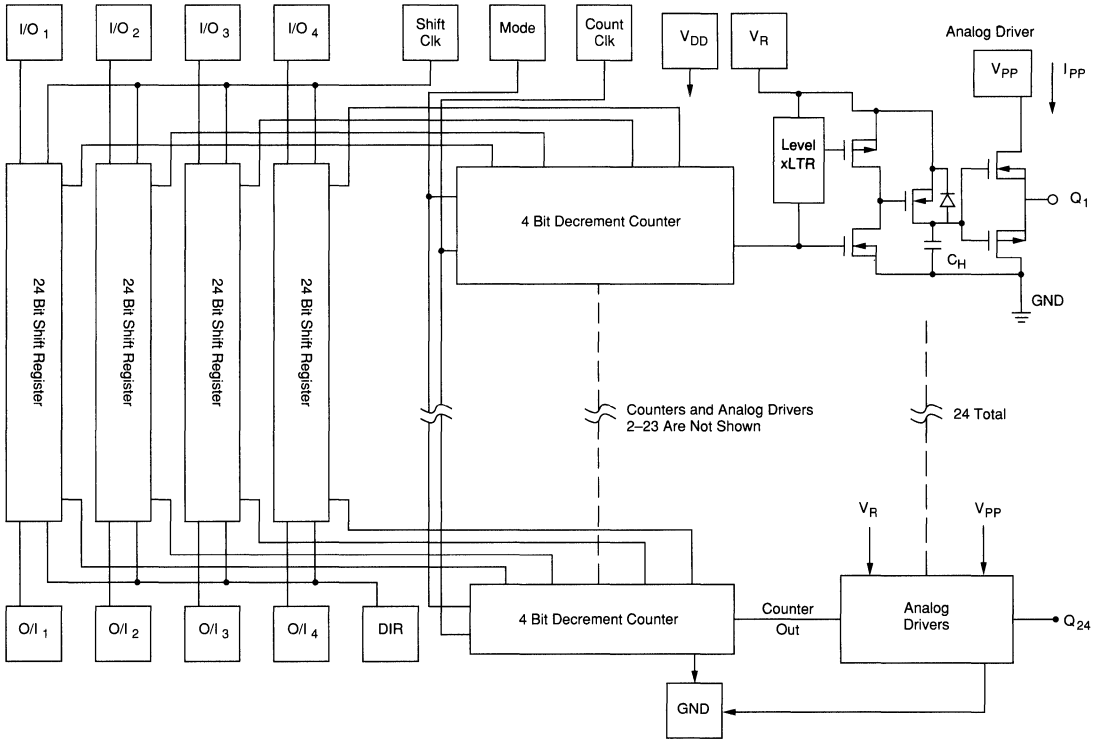
Notes: 1. SCLK, CCLK are continuous.
2. All typical values are at V_{DD} = 5.0V.

High-Voltage DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{PP}	High-voltage supply	-0.3		70	V	
I_{PP}	V_{PP} supply current			100	µA	V_{PP} = 70V, outputs high or low, no load
V_R	Ramp voltage	0		V_{PP}	V	
I_{AOH} max	Maximum high-voltage analog output source current[1]	-40			mA	V_{PP} = 70V
I_{AOH}	High-voltage analog output source current[1]	-10			mA	V_{PP} = 70V V_R = 30V V_{AO} = 28V
I_{AOL} max	Maximum high-voltage analog output sink current[2]	40			mA	V_{PP} = 70V
I_{AOL}	High-voltage analog output sink current[2]	10			mA	V_{PP} = 70V V_R = 30V V_{AO} = 32V

Notes: 1. Either by N-CH transistor or P-CH output diode.
2. Either by P-CH transistor or N-CH output diode.

Functional Block Diagram



Function Table

Function	Control Inputs				Shift Registers	Counters	Outputs	
	Shift Clock	Counter Clock	Mode	V_R			Serial	Parallel
Load Shift Register	↑	X	L	X	Normal Shift Op.	X	Delayed Data-In	X
Load Counter	No ↑	↑	H	X	No Change	Load Data from S/R to Counter	No Change	Low
Counting	X	↑	L	Initiates Ramp	X	Translates Data to Time	X	D/A Conversion
Voltage Conversion	X	Pulsing	L	Volt Ramping Up	X	Counting	X	Follows Ramp

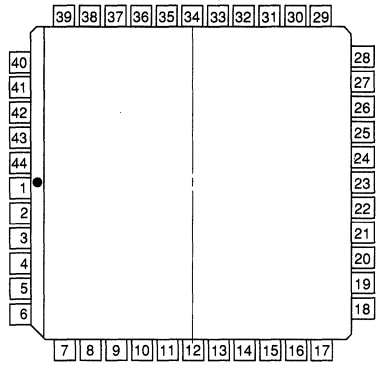
L = Low level, H = High level, X = Irrelevant, ↑ = Low to Hi Transition

Pin Configuration

44-Pin J-Lead

Pin	Function	Pin	Function
1	GND	23	HVout 13
2	DIR	24	HVout 12
3	V_{DD}	25	HVout 11
4	Mode	26	HVout 10
5	O/I_1	27	HVout 9
6	O/I_2	28	HVout 8
7	O/I_3	29	HVout 7
8	O/I_4	30	HVout 6
9	V_R	31	HVout 5
10	V_{PP}	32	HVout 4
11	GND	33	HVout 3
12	HVout 24	34	HVout 2
13	HVout 23	35	HVout 1
14	HVout 22	36	GND
15	HVout 21	37	V_{PP}
16	HVout 20	38	V_R
17	HVout 19	39	I/O_4
18	HVout 18	40	I/O_3
19	HVout 17	41	I/O_2
20	HVout 16	42	I/O_1
21	HVout 15	43	SC
22	HVout 14	44	CC

Package Outline



top view

44-pin J-lead Package

Gray Shade Decoding Scheme

Brightest Shade No.	I/O_1	I/O_2	I/O_3	I/O_4	
16	1	0	0	1	Brightest
15	1	1	0	1	
14	1	1	1	1	
13	1	1	1	0	
12	0	1	1	1	
11	1	0	1	0	
10	0	1	0	1	
9	1	0	1	1	
8	1	1	0	0	
7	0	1	1	0	
6	0	0	1	1	
5	1	0	0	0	
4	0	1	0	0	
3	0	0	1	0	
2	0	0	0	1	
1	0	0	0	0	Dimmest

4-Channel High Voltage Switch

Ordering Information

V_{PP}	V_{NN}	V_{SIG}	Order Number / Package		
			18-pin ceramic side-brazed DIP	18-pin Plastic DIP	Die in waffle pack
+70V	-70V	110V P-P	HV1014C	HV1014P	HV1014X
+80V	-80V	130V P-P	HV1016C	HV1016P	HV1016X

Features

- ☐ HVCMOS® Technology
- ☐ Up to 130V peak to peak switching capability
- ☐ Output On-resistance typically 25 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10MHz analog signal frequency
- ☐ 45 dB typical output off isolation at 5 MHz
- ☐ CMOS logic circuitry for low power and excellent noise immunity
- ☐ On-chip latch and chip select logic circuitry

Absolute Maximum Ratings*

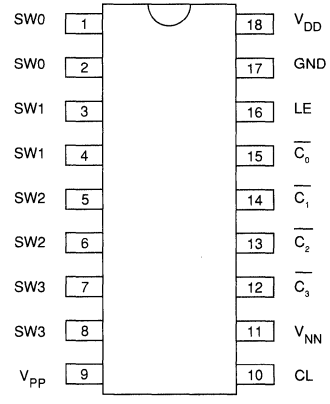
V_{DD} logic power supply voltage	-0.5V to +18V
V_{PP} positive high voltage supply	-0.5V to +90V
V_{NN} negative high voltage supply	+0.5V to -90V
Logic input voltages	-0.5 to V_{DD} +0.3V
Peak analog signal current/channel	3A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

General Description

This device is a 4-channel high-voltage integrated circuit (HVIC) intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. On-chip latches are provided for the data inputs. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Pin Configuration



top view

18-pin DIP

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{SW}		25		25	40		45	ohms	I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		15		15	30		35	ohms	I_{SW} = 200mA
Switch (ON) Resistance	R_{SW}		28		28	40		50	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		30		18	35		40	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 200mA
Switch (ON) Resistance Matching (0-3)	R_{SW}		15			15		15	%	I_{SW} = 5mA V_{PP} = +50V, V_{NN} = -50V
Switch Off Leakage	I_{SWL}		50		0.5	50		150	µA	V_{OUT} = V_{PP} -10V thru 10K with 4 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	RL = 100K
DC Offset Switch On			500		100	500		500	mV	RL = 100K
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current	I_{PPQ}		200		50	200		200	µA	ALL SWS OFF
Neg. HV Supply Current	I_{NNQ}		-200		-50	-200		-200	µA	
Pos. HV Supply Current	I_{PP}				1.6	3.2			mA	1 SW ON
Neg. HV Supply Current	I_{NN}				-1.6	-3.2			mA	I_{SW} = 5mA
Pos. HV Supply Current	I_{PP}				1.2	2.4			mA	V_{PP} = +50V
Neg. HV Supply Current	I_{NN}				-1.2	-2.4			mA	V_{NN} = -50V 1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					2.5				A	
Logic Supply Current	I_{DD}				0.001	0.5			mA	

AC Characteristics

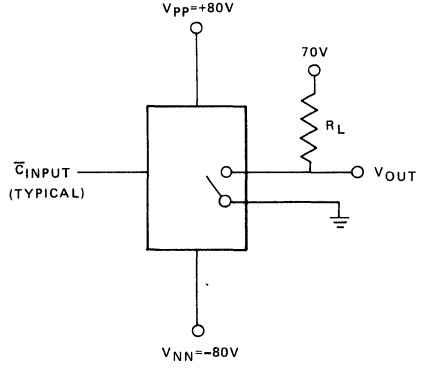
Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Data Hold Time After LE Rises	t_{HD}			5					ns	
Set Up Time Before LE Rises	t_{SD}			260					ns	
Time Width of LE	t_{WLE}			300					ns	
Time Width of $\overline{CL}$	t_{WCL}			100					ns	
Turn On Time	t_{ON}		5		2.5	5		5	µs	
Turn Off Time	t_{OFF}		10		5.0	10		10	µs	
Off Isolation	KO			35	45				dB	f = 5MHz

Recommended Operating Conditions

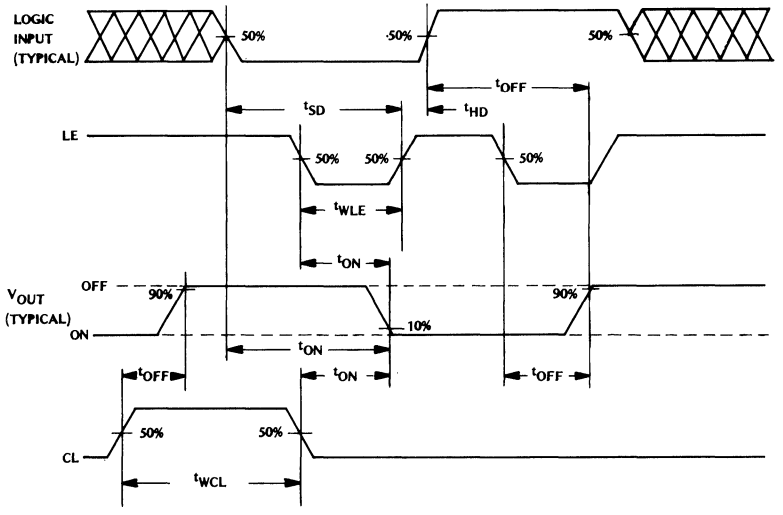
Symbol	Parameter	Device		Value
		HV1014	HV1016	
V_{DD}	Logic power supply voltage	X	X	+10.0V to +15.5V
V_{PP}	Positive high voltage supply	X		+50.0V to +70.0V
			X	+50.0V to +80.0V
V_{NN}	Negative high voltage supply	X		-50.0V to -70.0V
			X	-50.0V to -80.0V
V_{IH}	High level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free air-temperature	X	X	0° to 70°C

Note: For non-ground referenced systems the following must be used:
Power up sequence: GND VNN VDD VPP
Power down sequence: VPP VDD VNN GND

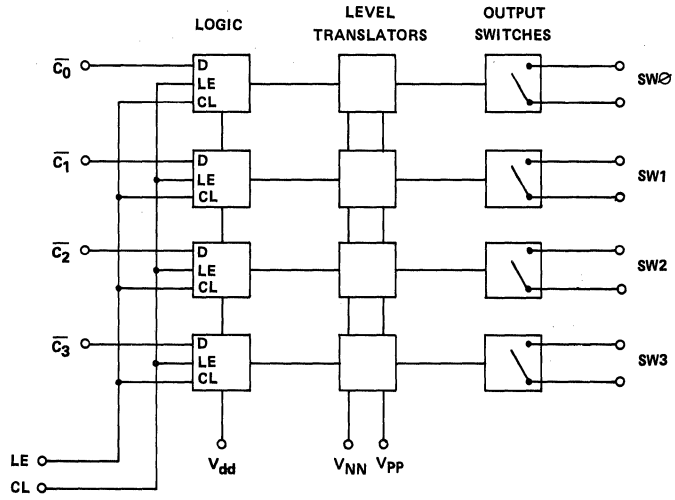
T_{ON}/T_{OFF} Measurement Circuit



Logic Timing Waveforms



Logic Diagram



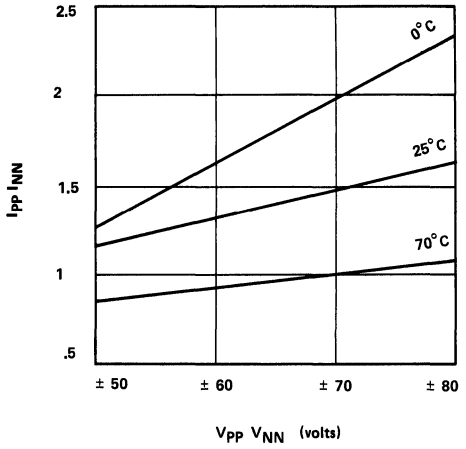
Truth Table

$\overline{C_0}$	$\overline{C_1}$	$\overline{C_2}$	$\overline{C_3}$	LE	CL	SW0	SW1	SW2	SW3
H				L	L	OFF			
L				L	L	ON			
	H			L	L		OFF		
	L			L	L		ON		
		H		L	L			OFF	
		L		L	L			ON	
			H	L	L				OFF
			L	L	L				ON
X	X	X	X	X	H	OFF	OFF	OFF	OFF
X	X	X	X	H	L	HOLD			

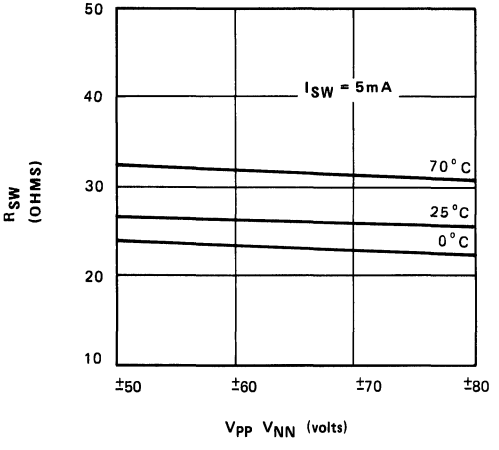
Notes: 1. The four switches operate independently.
2. The clear input overrides all other inputs.
3. The switches go to a state retaining their present condition at the rising edge of LE. When LE is low, the switch control data flows through the latch.

Typical Performance Curves

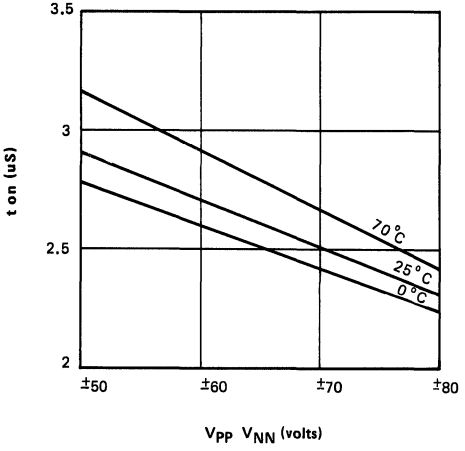
TYPICAL
I_{PP} I_{NN} vs. V_{PP} V_{NN} (ONE SWITCH ON)



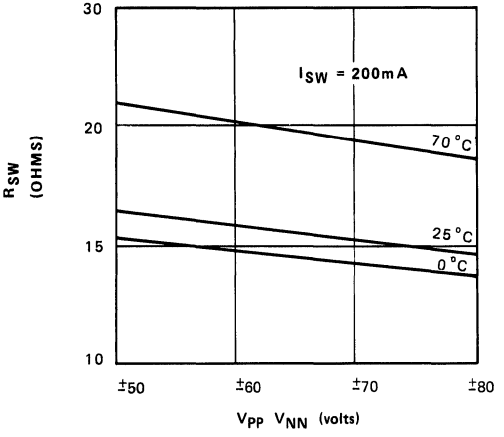
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



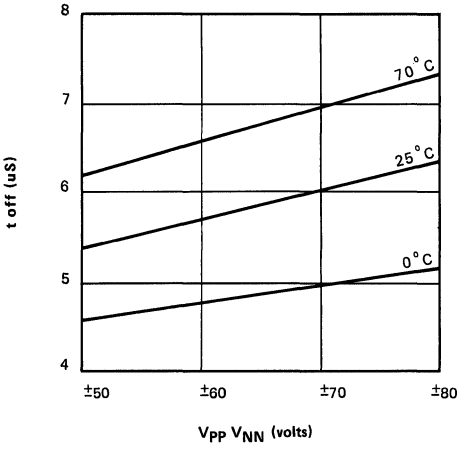
TYPICAL
t on (uS) vs. V_{PP} V_{NN}



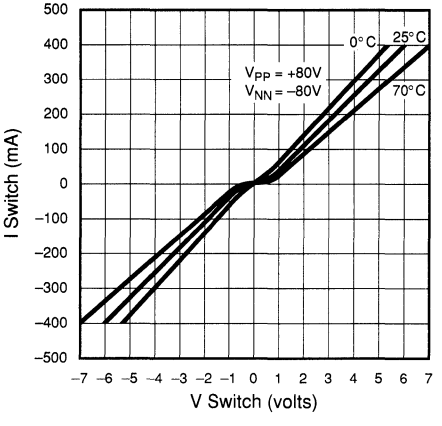
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



TYPICAL
t_{off} vs. V_{PP} V_{NN}



Typical
Switch Current vs. Voltage



8-Channel High Voltage Switch

Ordering Information

V_{PP}	V_{NN}	V_{SIG}	Package Options		
			18-pin ceramic side-brazed DIP	18-pin Plastic DIP	Die in waffle pack
+70V	-70V	110V P-P	HV1214C	HV1214P	HV1214X
+80V	-80V	130V P-P	HV1216C	HV1216P	HV1216X

Features

- ☐ HVCMOS® Technology
- ☐ Up to 130V peak to peak switching capability
- ☐ Output On-resistance typically 40 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10MHz analog signal frequency
- ☐ 45 dB typical output off isolation at 5 MHz
- ☐ CMOS logic circuitry for low power and excellent noise immunity
- ☐ On-chip shift register, latch and chip select logic circuitry

Absolute Maximum Ratings*

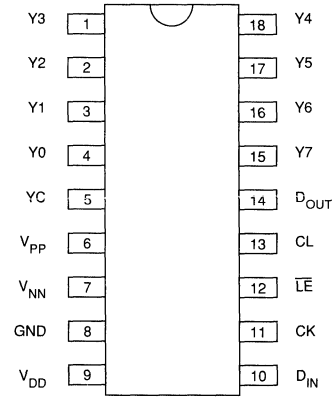
V_{DD} Logic power supply voltage	-0.5V to +18V
V_{PP} Positive high voltage supply	-0.5V to +90V
V_{NN} Negative high voltage supply	+0.5V to -90V
Logic input voltages	-0.5V to V_{DD} +0.3V
Peak analog signal current/channel	1.5A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

General Description

This device is an 8-channel high-voltage integrated circuit (HVIC) intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Pin Configuration



top view

18-pin DIP

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{SW}		40		40	50		60	OHMS	I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		35		25	35		45	OHMS	I_{SW} = 200mA
Switch (ON) Resistance	R_{SW}		55		45	55		65	OHMS	V_{PP} = +50V V_{NN} = -50V I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		40		25	40		50	OHMS	V_{PP} = +50V V_{NN} = -50V I_{SW} = 200mA
Switch (ON) Resistance Matching	R_{SW}		30		10	30		30	%	I_{SW} = 5mA V_{PP} = +50V, V_{NN} = -50V
Switch Off Leakage	I_{SWL}		50		0.5	50		150	µA	V_{OUT} = V_{PP} -10V thru 10K with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	RL = 100K
DC Offset Switch On			500		100	500		500	mV	RL = 100K
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current Neg. HV Supply Current	I_{PPQ} I_{NNQ}		200 -200		50 -50	200 -200		200 -200	µA µA	ALL SWS OFF
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				0.8 -0.8	1.6 -1.6			mA mA	1 SWS ON I_{SW} = 5mA
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				0.6 -0.6	1.2 -1.2			mA mA	V_{PP} = +50V V_{NN} = -50V 1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					1.5				A	
Logic Supply Current	I_{DD}				4	6			mA	f_{CLK} = 3 MHz
Logic Supply Current	I_{DD}					5			mA	
Data Out Source Current	I_{SOR}	0.7		0.8	0.9		0.7		mA	V_{OUT} = V_{DD} -0.7V
Data Out Sink Current	I_{SINK}	1.5		1.6	1.8		1.5		mA	V_{OUT} = 0.7V

AC Characteristics

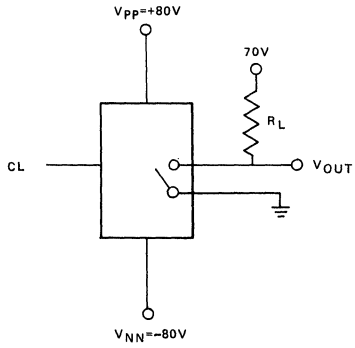
Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Clock Frequency	f_{CLK}					3			MHz	f_{DATA} = f_{CLK}/2
Set Up Time Data to Clock	t_{SU}			0					ns	
Hold Time Data from Clock	t_h			5					ns	
Set Up Time Before LE Rises	t_{SD}			260					ns	
Time Width of LE	t_{WLE}			300					ns	
Clock Delay Time Data Out	t_{DO}				250	330			ns	
Turn On Time	t_{ON}		5		2.5	5		5	µs	
Turn Off Time	t_{OFF}		10		5.0	10		10	µs	
Time Width of CL	t_{WCL}			100					ns	
Off Isolation	KO			35	45				dB	f = 5MHz

Recommended Operating Conditions

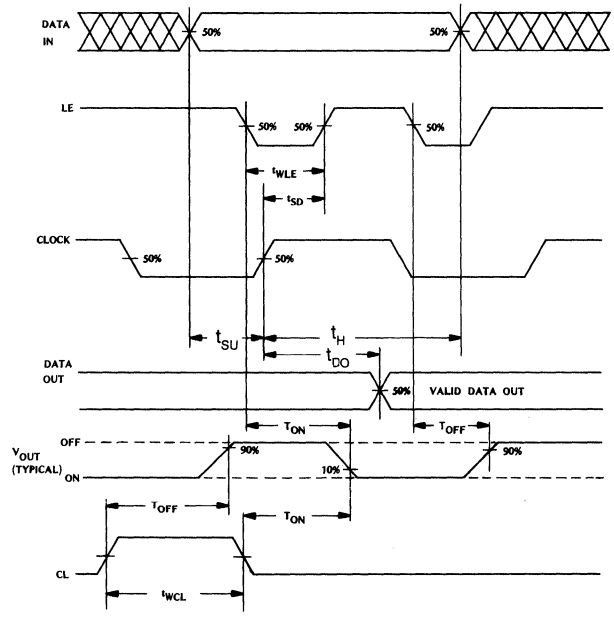
Symbol	Parameter	Device		Value
		HV1214	HV1216	
V_{DD}	Logic power supply voltage	X	X	+10.0V to +15.5V
V_{PP}	Positive high voltage supply	X		+50.0V to +70.0V
			X	+50.0V to +80.0V
V_{NN}	Negative high voltage supply	X		-50.0V to -70.0V
			X	-50.0V to -80.0V
V_{IH}	High level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free air-temperature	X	X	0° to 70°C

Note: For non-ground referenced systems the following must be used:
Power up sequence: GND VNN VDD VPP
Power down sequence: VPP VDD VNN GND

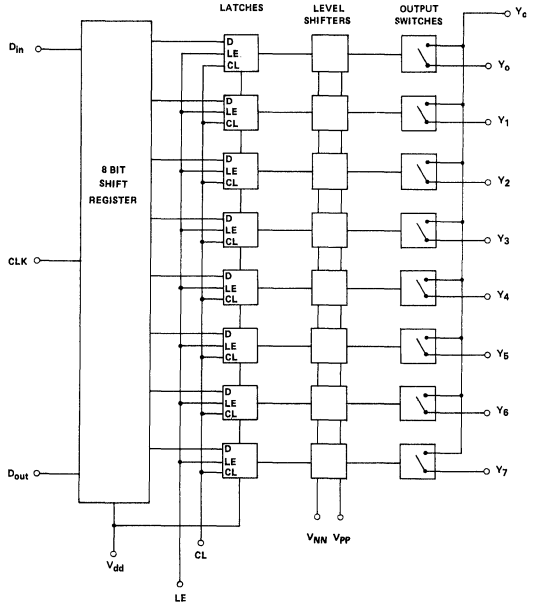
T_{ON}/T_{OFF} Measurement Circuit



Logic Timing Waveforms



Logic Diagram



HV12 Truth Table

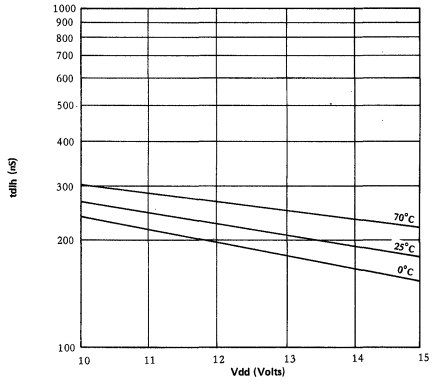
D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	$\overline{CL}$	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							

Notes:

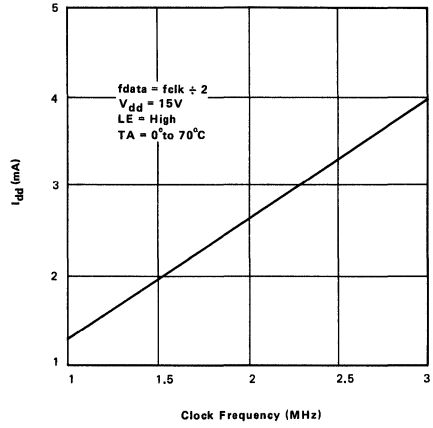
1. The eight switches operate independently, but connect to a common Z line.
2. Serial data is clocked in on the L→H transition of CK.
3. The clear input overrides all other inputs.
4. The switches go to a state retaining their present condition at the rising edge of LE. When LE is low, the shift register data flows through the latch.
5. D_{OUT} is high when switch 7 is on.
6. Shift register clocking has no effect on the switch states if LE is H.

Typical Performance Curves

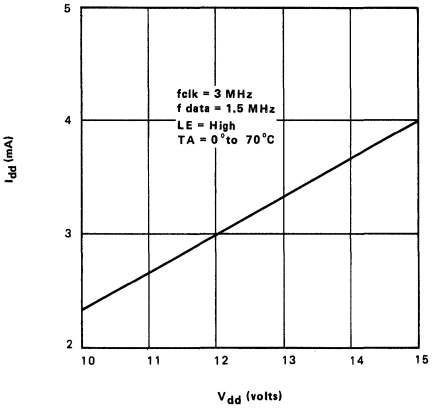
TYPICAL
tdlh vs Vdd



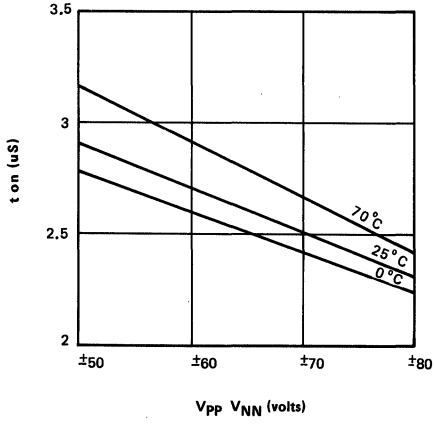
TYPICAL
Idd vs. Frequency



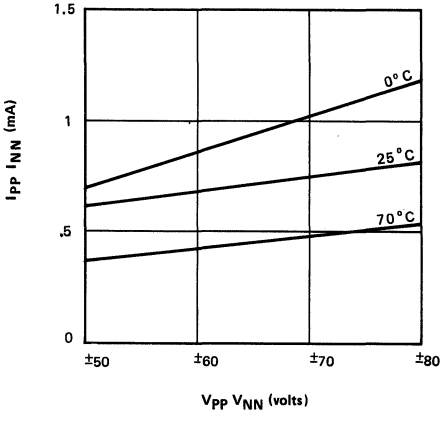
TYPICAL
Idd vs. Vdd



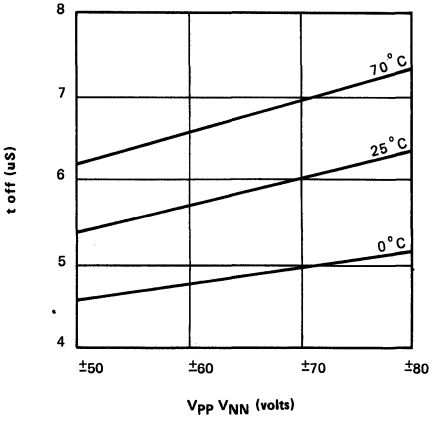
TYPICAL
t on (uS) vs. V_{PP} V_{NN}



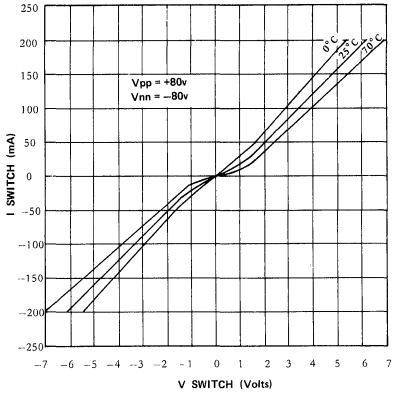
TYPICAL
I_{PP} I_{NN} vs. V_{PP} V_{NN} (ONE SWITCH ON)



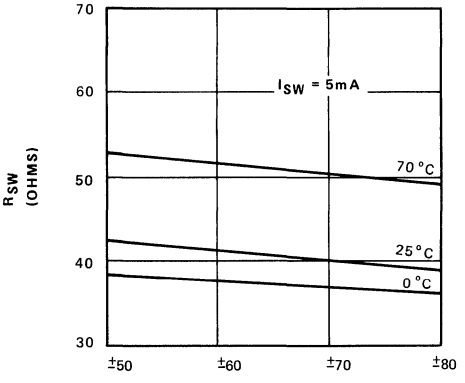
TYPICAL
t_{off} vs. V_{PP} V_{NN}



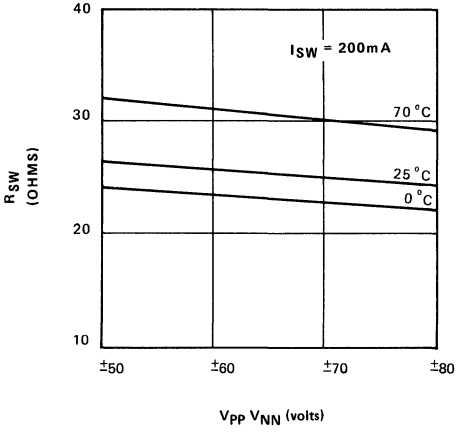
TYPICAL
SWITCH CURRENT vs VOLTAGE



TYPICAL
R_{SW} vs. V_{PP} V_{NN}



TYPICAL
R_{SW} vs. V_{PP} V_{NN}



Dual 4-Channel High Voltage Switch with Decode

Ordering Information

V_{PP}	V_{NN}	V_{SIG}	Order Number / Package		
			20-pin ceramic side-brazed DIP	20-pin Plastic DIP	Die in waffle pack
+70V	-70V	110V P-P	HV1314C	HV1314P	HV1314X
+80V	-80V	130V P-P	HV1316C	HV1316P	HV1316X

Features

- ☐ HVCMOS® Technology
- ☐ Up to 130V peak to peak switching capability
- ☐ Output On-resistance typically 40 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10MHz analog signal frequency
- ☐ 45 dB typical output off isolation at 5 MHz
- ☐ CMOS logic circuitry for low power and excellent noise immunity
- ☐ On-chip decode, latch and chip select logic circuitry

Absolute Maximum Ratings*

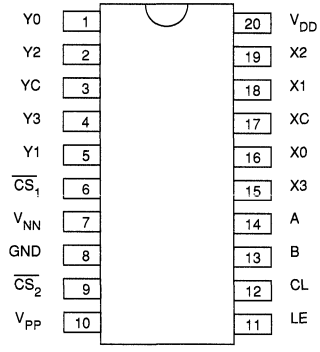
V_{DD} Logic power supply voltage	-0.5V to +18V
V_{PP} Positive high voltage supply	-0.5V to +90V
V_{NN} Negative high voltage supply	+0.5V to -90V
Logic input voltages	-0.5V to V_{DD} +0.3V
Peak analog signal current/channel	1.5A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

General Description

This device is an 8-channel high-voltage integrated circuit (HVIC) configured as dual 4 channel switches with decode, intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. On-chip latches are provided for the decoded data. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Pin Configuration



top view

20-pin DIP

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{SW}		50		40	50		60	ohms	I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		35		25	35		45	ohms	I_{SW} = 200mA
Switch (ON) Resistance	R_{SW}		55		45	55		65	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		40		25	40		50	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 200mA
Switch (ON) Resistance Matching x and y (0-3)	R_{SW}		20			20		20	%	I_{SW} = 5mA V_{PP} = +50V, V_{NN} = -50V
Switch Off Leakage	I_{SWL}		50		0.5	50		150	µA	V_{OUT} = V_{PP} -10V thru 10K with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	RL = 100K
DC Offset Switch On			500		100	500		500	mV	RL = 100K
Pole to Pole Switch Capacitance	C_{SW}		100		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current Neg. HV Supply Current	I_{PPQ} I_{NNQ}		200 -200		50 -50	200 -200		200 -200	µA µA	ALL SWS OFF
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				1.6 -1.6	3.2 -3.2			mA mA	1 SW ON I_{SW} = 5mA
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				1.2 -1.2	2.4 -2.4			mA mA	V_{PP} = +50V V_{NN} = -50V 1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					1.5				A	
Logic Supply Current	I_{DD}				0.001	0.5			mA	

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AC Characteristics (VDD = 12V, TC = 25°C)

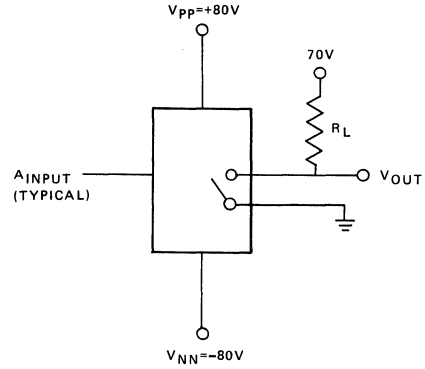
Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Data Hold Time After LE Rises	t_{HD}			5					ns	
Set Up Time Before LE Rises	t_{SD}			260					ns	
Time Width of LE	t_{WLE}			300					ns	
Time Width of CL	t_{WCL}			100					ns	
Turn On Time	t_{ON}		5		2.5	5		5	µs	
Turn Off Time	t_{OFF}		10		5.0	10		10	µs	
Off Isolation	KO			35	45				dB	f = 5MHz

Recommended Operating Conditions

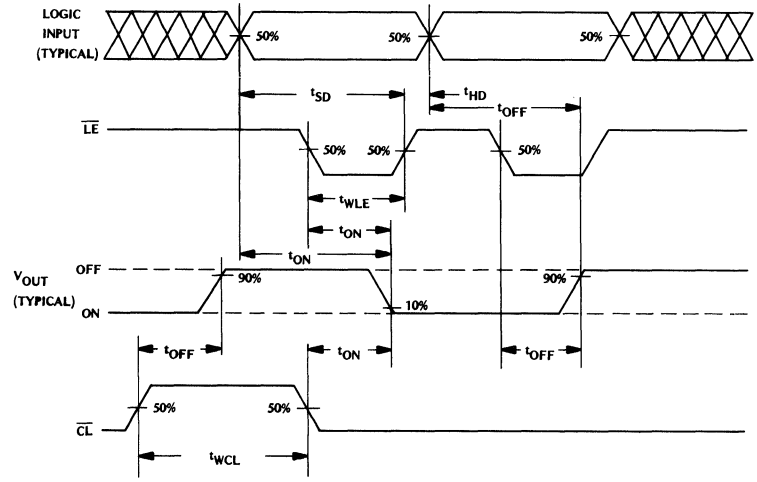
Symbol	Parameter	Device		Value
		HV1314	HV1316	
V_{DD}	Logic power supply voltage	X	X	+10.0V to +15.5V
V_{PP}	Positive high voltage supply	X		+50.0V to +70.0V
			X	+50.0V to +80.0V
V_{NN}	Negative high voltage supply	X		-50.0V to -70.0V
			X	-50.0V to -80.0V
V_{IH}	High level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free air-temperature	X	X	0° to 70°C

Note: For non-ground referenced systems the following must be used:
Power up sequence: GND VNN VDD VPP
Power down sequence: VPP VDD VNN GND

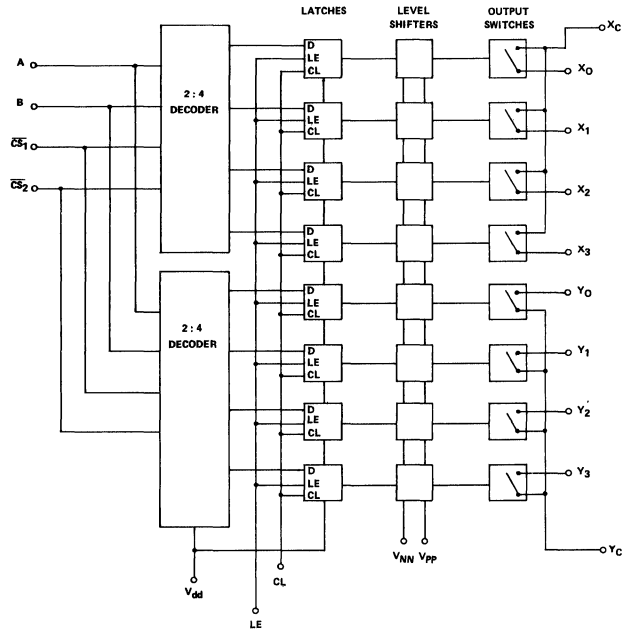
T_{ON}/T_{OFF} Measurement Circuit



Logic Timing Waveforms



Logic Diagram



Truth Table

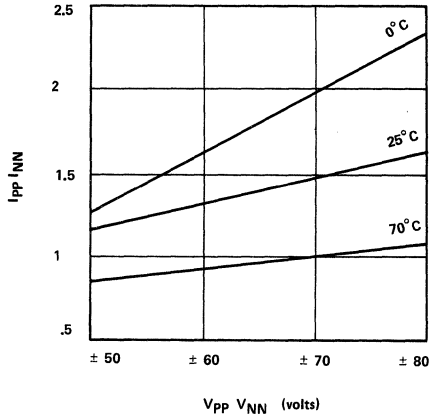
B	A	$\overline{CS}_1$	$\overline{CS}_2$	LE	CL	X0	X1	X2	X3	Y0	Y1	Y2	Y3
L	L	L	L	L	L	ON				ON			
L	H	L	L	L	L		ON				ON		
H	L	L	L	L	L			ON				ON	
H	H	L	L	L	L				ON				ON
X	X	H	X	L	L	ALL OFF							
X	X	X	H	L	L	ALL OFF							
X	X	X	X	X	H	ALL OFF							
X	X	X	X	H	L	HOLDS PREVIOUS STATE							

Notes:

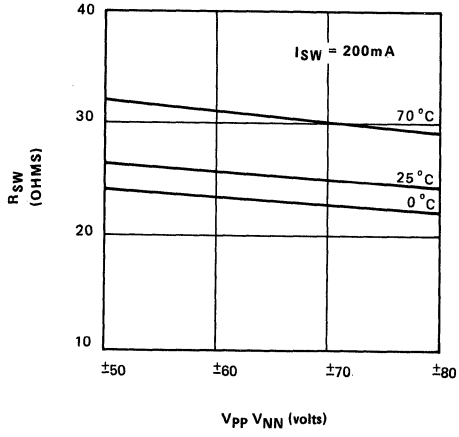
1. Address data at A and B cause one switch in each group of four to be selected for connection to the common busses XC or YC.
2. The clear input CL overrides all other inputs.
3. Since the latch follows the decoder, only the CL input matters when LE is H.
4. The switches go to a state retaining their present condition at the rising edge of LE. When LE is low, the decoded selection address information flows through the latch.

Typical Performance Curves

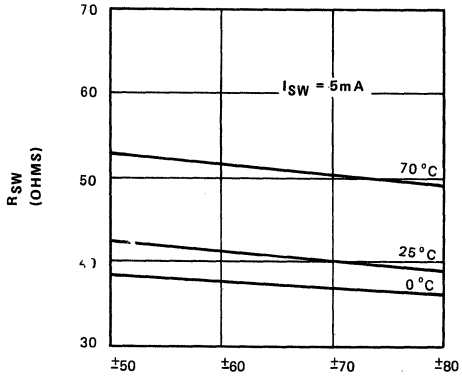
TYPICAL
I_{PP} I_{NN} vs. V_{PP} V_{NN} (ONE SWITCH ON)



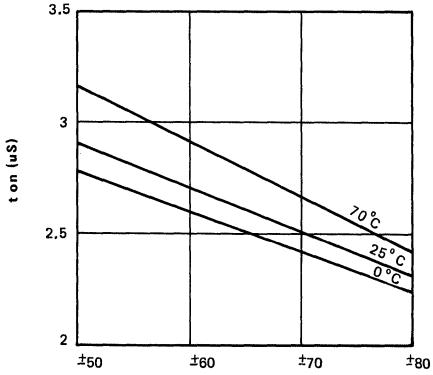
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



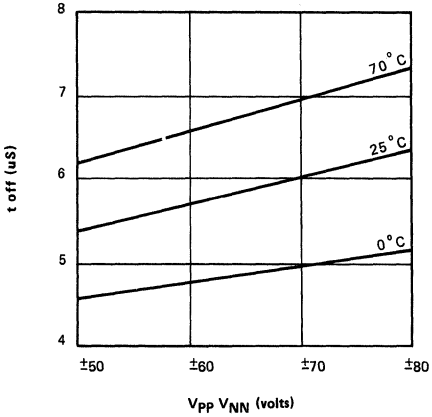
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



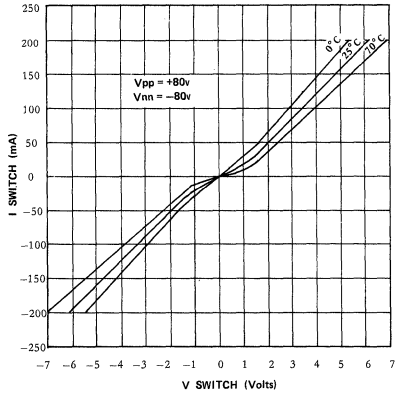
TYPICAL
t on (uS) vs. V_{PP} V_{NN}



TYPICAL
t_{off} vs. V_{PP} V_{NN}



TYPICAL
SWITCH CURRENT vs VOLTAGE



8-Channel High Voltage Switch with Decoded Switch Selection

Ordering Information

V_{PP}	V_{NN}	V_{SIG}	Package Options		
			20-pin ceramic side-brazed DIP	20-pin Plastic DIP	Die in waffle pack
+70V	-70V	110V P-P	HV1414C	HV1414P	HV1414X
+80V	-80V	130V P-P	HV1416C	HV1416P	HV1416X

Features

- ☐ HVCMOS® Technology
- ☐ Up to 130V peak to peak switching capability
- ☐ Output On-resistance typically 40 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10MHz analog signal frequency
- ☐ 45 dB typical output off isolation at 5 MHz
- ☐ CMOS logic circuitry for low power and excellent noise immunity
- ☐ On-chip decode, latch and chip select logic circuitry

Absolute Maximum Ratings*

V_{DD} Logic power supply voltage	-0.5V to +18V
V_{PP} Positive high voltage supply	-0.5V to +90V
V_{NN} Negative high voltage supply	+0.5V to -90V
Logic input voltages	-0.5V to V_{DD} +0.3V
Peak analog signal current/channel	1.5A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

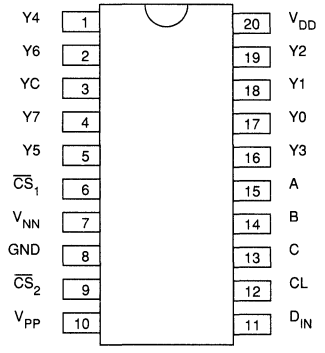
* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

General Description

This device is an 8-channel high-voltage integrated circuit (HVIC), configured as a 1 of 8 decode function, intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. On-chip latches are provided for the decoded data.

The unique control logic on this device provides individual control of each switch, allowing more than one switch to be turned on at a time. The clear function turns off all switches simultaneously. The chip select inputs control the latches, holding the output stable while the address and data are changed. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Pin Configuration



top view

20-pin DIP

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{SW}		50		40	50		60	ohms	I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		35		25	35		45	ohms	I_{SW} = 200mA
Switch (ON) Resistance	R_{SW}		55		45	55		65	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		40		25	40		50	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 200mA
Switch (ON) Resistance Matching	R_{SW}		30		10	30		30	%	I_{SW} = 5mA V_{PP} = +50V, V_{NN} = -50V
Switch Off Leakage	I_{SWL}		50		0.5	50		150	µA	V_{OUT} = V_{PP} -10V thru 10K with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	RL = 100K
DC Offset Switch On			500		100	500		500	mV	RL = 100K
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current Neg. HV Supply Current	I_{PPQ} I_{NNQ}		200 -200		50 -50	200 -200		200 -200	µA µA	ALL SWS OFF
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				0.8 -0.8	1.6 -1.6			mA mA	1 SW ON I_{SW} = 5mA
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				0.6 -0.6	1.2 -1.2			mA mA	V_{PP} = +50V V_{NN} = -50V 1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					1.5				A	
Logic Supply Current	I_{DD}				0.001	0.5			mA	

AC Characteristics

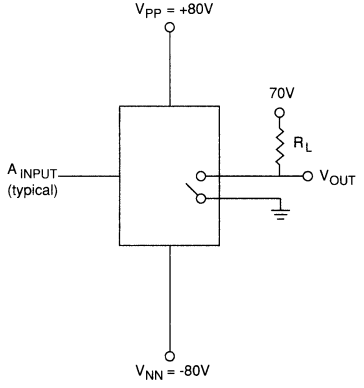
Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
D_{IN} Set Up Time Before $\overline{CS}$ Rises	t_{DSU}			260					ns	
Address Set Up Time Before $\overline{CS}$ Falls	t_{ASU}			120					ns	
Hold Time After $\overline{CS}$ Rises	t_h			35					ns	
Minimum Clear Pulse Width	t_{WCL}			150					ns	
Minimum Chip Select Low Pulse Width	t_{WCS}			300					ns	
Turn On Time	t_{ON}		5		2.5	5		5	µs	
Turn Off Time	t_{OFF}		10		5.0	10		10	µs	
Off Isolation	KO			35	45				dB	f = 5MHz

Recommended Operating Conditions

Symbol	Parameter	Device		Value
		HV1414	HV1416	
V_{DD}	Logic power supply voltage	X	X	+10.0V to +15.5V
V_{PP}	Positive high voltage supply	X		+50.0V to +70.0V
			X	+50.0V to +80.0V
V_{NN}	Negative high voltage supply	X		-50.0V to -70.0V
			X	-50.0V to -80.0V
V_{IH}	High level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free air-temperature	X	X	0° to 70°C

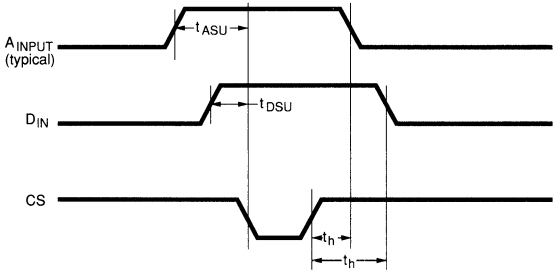
Note: For non-ground referenced systems the following must be used:
Power up sequence: GND VNN VDD VPP
Power down sequence: VPP VDD VNN GND

T_{ON}/T_{OFF} Measurement Circuit

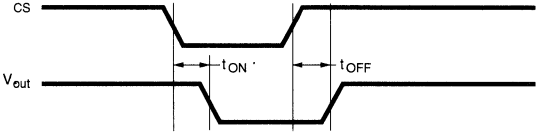


Switching Waveforms

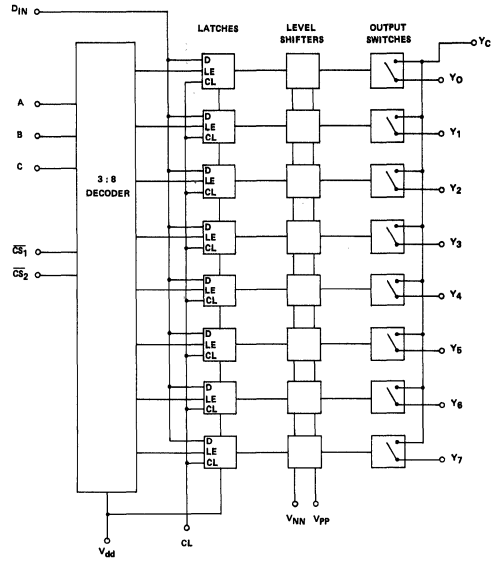
Logic Timing Waveforms



Output Timing Waveforms



Logic Diagram



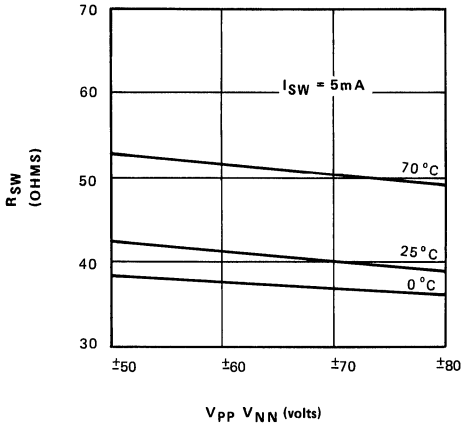
Truth Table

C	B	A	$\overline{CS}_1$	$\overline{CS}_2$	D_{IN}	CL	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L	L	L	L	L	L	L	OFF							
L	L	L	L	L	H	L	ON							
L	L	H	L	L	L	L		OFF						
L	L	H	L	L	H	L		ON						
L	H	L	L	L	L	L			OFF					
L	H	L	L	L	H	L			ON					
L	H	H	L	L	L	L				OFF				
L	H	H	L	L	H	L				ON				
H	L	L	L	L	L	L					OFF			
H	L	L	L	L	H	L					ON			
H	L	H	L	L	L	L						OFF		
H	L	H	L	L	H	L						ON		
H	H	L	L	L	L	L							OFF	
H	H	L	L	L	H	L							ON	
H	H	H	L	L	L	L								OFF
H	H	H	L	L	H	L								ON
X	X	X	H	X	X	L	HOLDS PREVIOUS STATE							
X	X	X	X	H	X	L	HOLDS PREVIOUS STATE							
X	X	X	X	X	X	H	ALL OUTPUTS OFF							

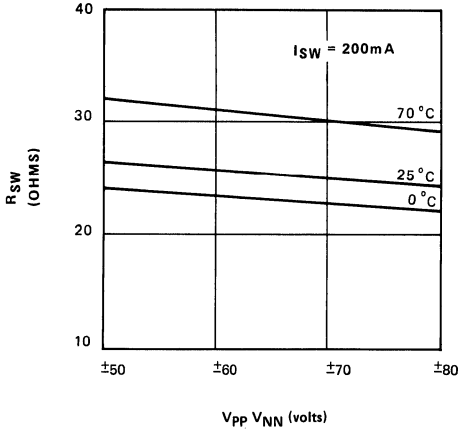
Notes: 1. D_{IN} controls the switches through flow-through latches, which are clocked (enabled) by an 8-way decoder controlled by A, B, C, $\overline{CS}_1$, and $\overline{CS}_2$. Therefore, the latch for a particular switch goes into the HOLD state when any of the above inputs prevents selection. $\overline{CS}_1$ or $\overline{CS}_2$ can be used as an active LOW clock input.
2. Spurious clocking may occur if A, B, or C is changed with $\overline{CS}_1$ and $\overline{CS}_2$ both low.
3. The clear input CL overrides all other inputs.
4. The eight switches operate independently.

Typical Performance Curves

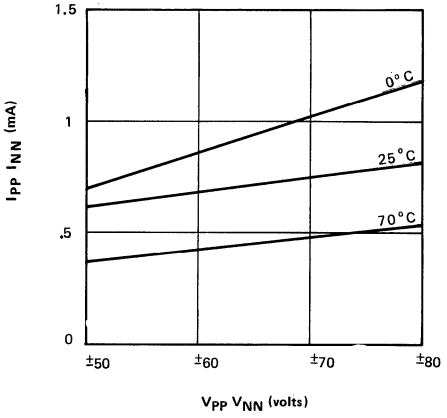
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



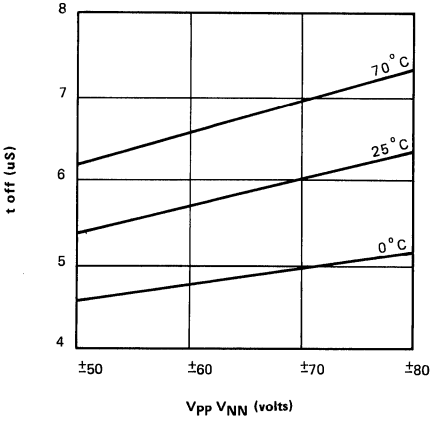
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



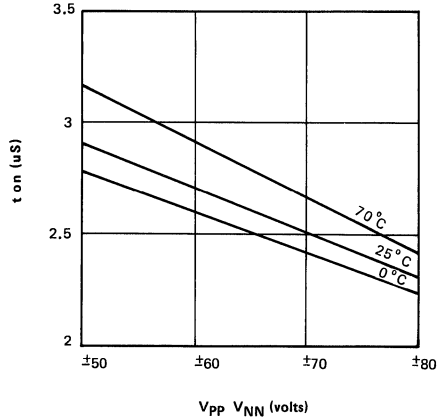
TYPICAL
I_{PP} I_{NN} vs. V_{PP} V_{NN} (ONE SWITCH ON)



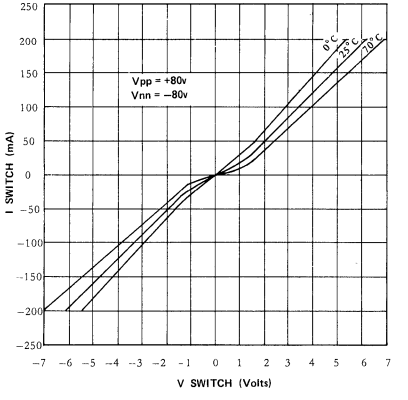
TYPICAL
t_{off} vs. V_{PP} V_{NN}



TYPICAL
t on (uS) vs. V_{PP} V_{NN}



TYPICAL
SWITCH CURRENT vs VOLTAGE



1 of 8 Decode 8-Channel High Voltage Switch

Ordering Information

V_{PP}	V_{NN}	V_{SIG}	Package Options		
			20-pin ceramic side-brazed DIP	20-pin Plastic DIP	Die in waffle pack
+70V	-70V	110V P-P	HV1514C	HV1514P	HV1514X
+80V	-80V	130V P-P	HV1516C	HV1516P	HV1516X

Features

- ☐ HVCMOS® Technology
- ☐ Up to 130V peak to peak switching capability
- ☐ Output On-resistance typically 40 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10MHz analog signal frequency
- ☐ 45 dB typical output off isolation at 5 MHz
- ☐ CMOS logic circuitry for low power and excellent noise immunity
- ☐ On-chip decode, latch and chip select logic circuitry

Absolute Maximum Ratings*

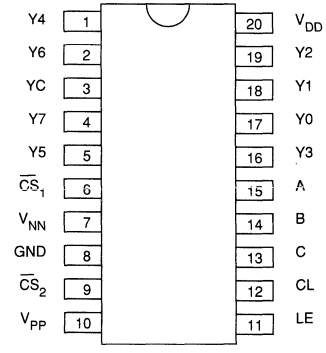
V_{DD} Logic power supply voltage	-0.5V to +18V
V_{PP} Positive high voltage supply	-0.5V to +90V
V_{NN} Negative high voltage supply	+0.5V to -90V
Logic input voltages	-0.5V to V_{DD} +0.3V
Peak analog signal current/channel	1.5A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

General Description

This device is an 8-channel high-voltage integrated circuit (HVIC), configured as a 1 of 8 decode functions, intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. ON-chip latches are provided for the decoded data. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Pin Configuration



top view

20-pin DIP

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{SW}		50		40	50		60	ohms	I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		35		25	35		45	ohms	I_{SW} = 200mA
Switch (ON) Resistance	R_{SW}		55		45	55		65	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		40		25	40		50	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 200mA
Switch (ON) Resistance Matching x and y (0-3)	R_{SW}		30		10	30		30	%	I_{SW} = 5mA V_{PP} = +50V, V_{NN} = -50V
Switch Off Leakage	I_{SWL}		50		0.5	50		150	µA	V_{OUT} = V_{PP} -10V thru 10K with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	RL = 100K
DC Offset Switch On			500		100	500		500	mV	RL = 100K
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current Neg. HV Supply Current	I_{PPQ} I_{NNQ}		200 -200		50 -50	200 -200		200 -200	µA µA	ALL SWS OFF
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				0.8 -0.8	1.6 -1.6			mA mA	1 SW ON I_{SW} = 5mA
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				0.6 -0.6	1.2 -1.2			mA mA	V_{PP} = +50V V_{NN} = -50V 1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					1.5				A	
Logic Supply Current	I_{DD}				0.001	5			mA	

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AC Characteristics

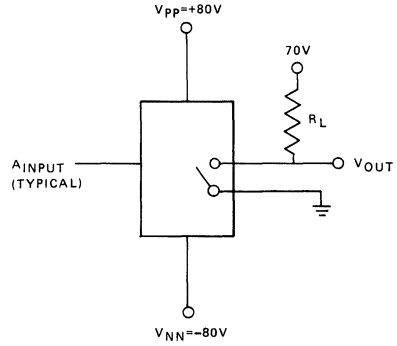
Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Data Hold Time After LE Rises	t_{HD}			5					ns	
Set Up Time Before LE Rises	t_{SD}			260					ns	
Time Width of LE	t_{WLE}			300					ns	
Time Width of CL	t_{WCL}			100					ns	
Turn On Time	t_{ON}		5		2.5	5		5	µs	
Turn Off Time	t_{OFF}		10		5.0	10		10	µs	
Off Isolation	KO			35	45				dB	f = 5MHz

Recommended Operating Conditions

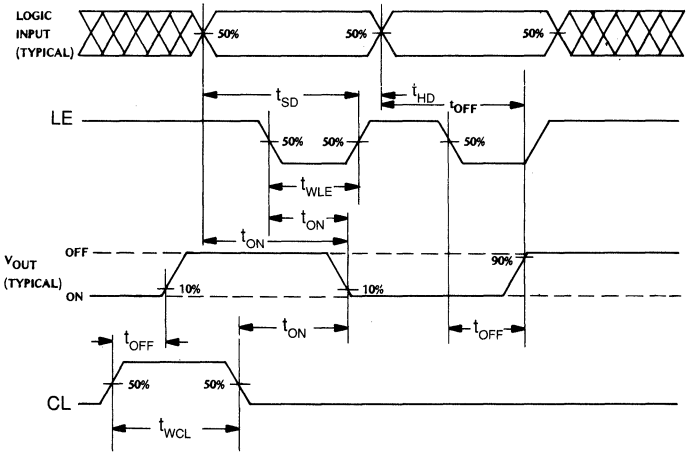
Symbol	Parameter	Device		Value
		HV1514	HV1516	
V_{DD}	Logic power supply voltage	X	X	+10.0V to +15.5V
V_{PP}	Positive high voltage supply	X		+50.0V to +70.0V
			X	+50.0V to +80.0V
V_{NN}	Negative high voltage supply	X		-50.0V to -70.0V
			X	-50.0V to -80.0V
V_{IH}	High level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free air-temperature	X	X	0° to 70°C

Note: For non-ground referenced systems the following must be used:
Power up sequence: GND VNN VDD VPP
Power down sequence: VPP VDD VNN GND

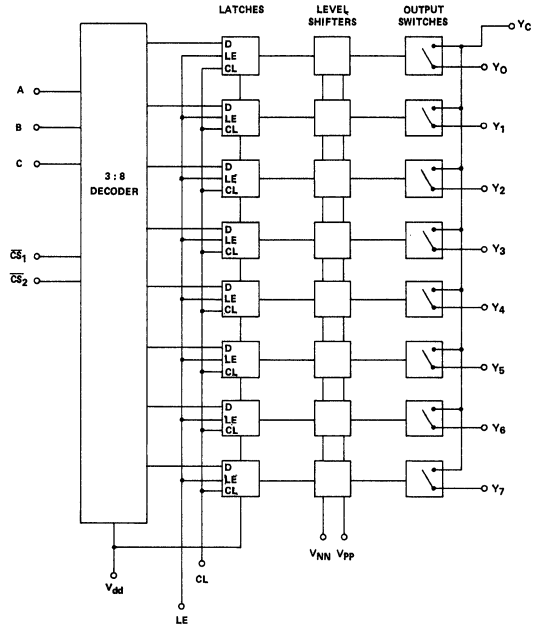
T_{ON}/T_{OFF} Measurement Circuit



Logic Timing Waveforms



Logic Diagram



Truth Table

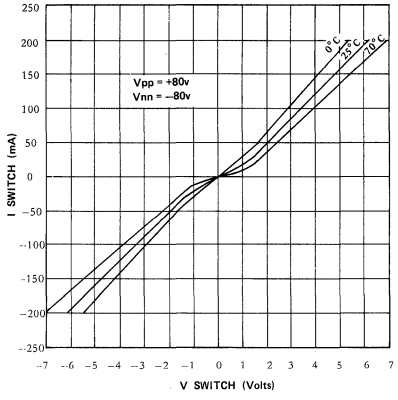
C	B	A	$\overline{CS}_1$	$\overline{CS}_2$	LE	CL	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L	L	L	L	L	L	L	ON							
L	L	H	L	L	L	L		ON						
L	H	L	L	L	L	L			ON					
L	H	H	L	L	L	L				ON				
H	L	L	L	L	L	L					ON			
H	L	H	L	L	L	L						ON		
H	H	L	L	L	L	L							ON	
H	H	H	L	L	L	L								ON
X	X	X	H	X	L	L	ALL OUTPUTS OFF							
X	X	X	X	H	L	L	ALL OUTPUTS OFF							
X	X	X	X	X	X	H	ALL OUTPUTS OFF							
X	X	X	X	X	H	L	HOLDS PREVIOUS STATE							

Notes:

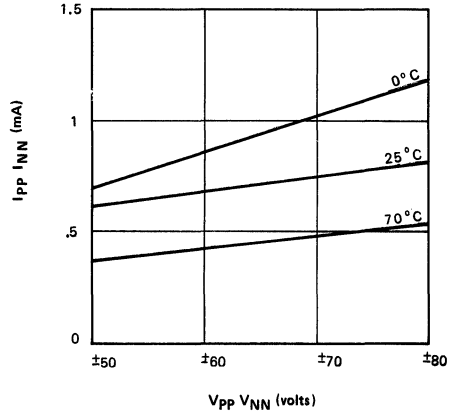
1. Address data at A, B, C cause one of the eight switches to be selected for connection to the common bus C.
2. The clear input CL overrides all other inputs.
3. Since the latch follows the decoder, only the CL input matters when LE is H.
4. The switches go to a state retaining their present condition at the rising edge of LE. When LE is low, the decoded selection address information flows through the latch.

Typical Performance Curves

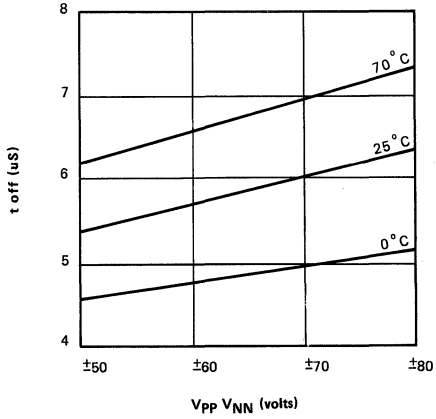
TYPICAL
SWITCH CURRENT vs VOLTAGE



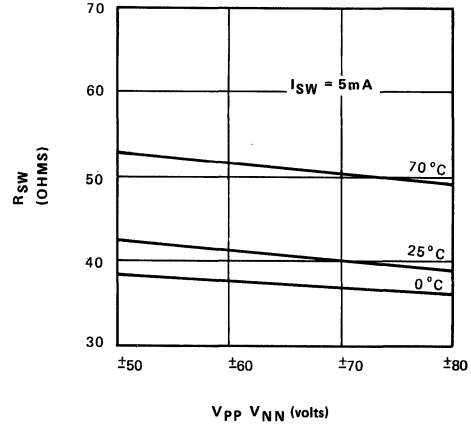
TYPICAL
I_{PP} I_{NN} vs. V_{PP} V_{NN} (ONE SWITCH ON)



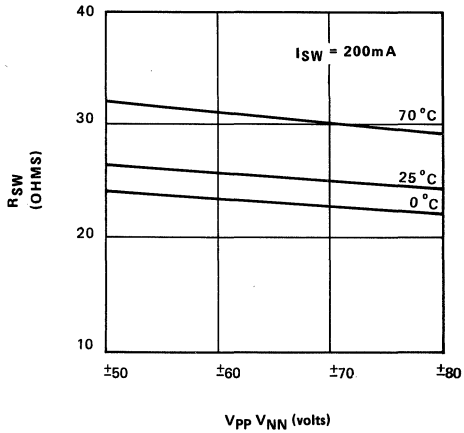
TYPICAL
t_{off} vs. V_{PP} V_{NN}



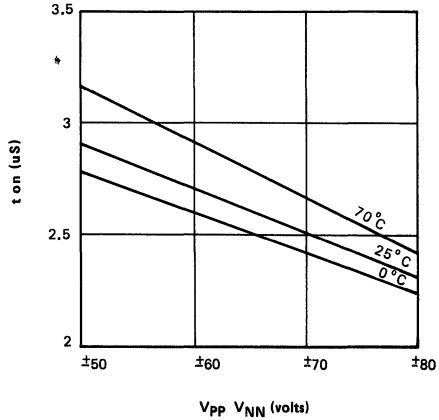
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



TYPICAL
R_{SW} vs. V_{PP} V_{NN}



TYPICAL
t on (uS) vs. V_{PP} V_{NN}



8-Channel High Voltage Switch

Ordering Information

V_{PP}	V_{NN}	V_{SIG}	Package Options				
			24-pin ceramic side-brazed DIP	Die in waffle pack	36-pin leaded ceramic chip carrier	24-pin plastic DIP	28-lead plastic chip carrier
+70V	-70V	110V P-P	HV1614C	HV1614X	HV1614CS	HV1614P	HV1614PJ
+80V	-80V	130V P-P	HV1616C	HV1616X	HV1616CS	HV1616P	HV1616PJ

Features

- ☐ HVCMOS® Technology
- ☐ Up to 130V peak to peak switching capability
- ☐ Output On-resistance typically 40 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10MHz analog signal frequency
- ☐ 45 dB typical output off isolation at 5 MHz
- ☐ CMOS logic circuitry for low power and excellent noise immunity
- ☐ On-chip shift register, latch and chip select logic circuitry
- ☐ Surface mount package available

General Description

This device is an 8-channel high-voltage integrated circuit (HVIC) intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Absolute Maximum Ratings*

V_{DD} Logic power supply voltage	-0.5V to +18V
V_{PP} Positive high voltage supply	-0.5V to +90V
V_{NN} Negative high voltage supply	+0.5V to -90V
Logic input voltages	-0.5V to V_{DD} +0.3V
Peak analog signal current/channel	1.5A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{SW}		50		40	50		60	ohms	I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		35		25	35		45	ohms	I_{SW} = 200mA
Switch (ON) Resistance	R_{SW}		55		45	55		65	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		40		25	40		50	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 200mA
Switch (ON) Resistance Matching	R_{SW}		15			15		15	%	I_{SW} = 5mA V_{PP} = +50V, V_{NN} = -50V
Switch Off Leakage	I_{SWL}		50		0.5	50		150	µA	V_{OUT} = V_{PP} -10V thru 10K with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	RL = 100K
DC Offset Switch On			500		100	500		500	mV	RL = 100K
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current Neg. HV Supply Current	I_{PPQ} I_{NNQ}		200 -200		50 -50	200 -200		200 -200	µA µA	ALL SWS OFF
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				0.8 -0.8	1.6 -1.6			mA mA	1 SW ON I_{SW} = 5mA
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				0.6 -0.6	1.2 -1.2			mA mA	V_{PP} = +50V V_{NN} = -50V 1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					1.5				A	
Logic Supply Current	I_{DD}				4	6			mA	f_{CLK} = 3MHz
Logic Supply Current	I_{DD}				0.001	5			mA	
Data Out Source Current	I_{SOR}	0.7		0.8	0.9		0.7		mA	V_{OUT} = V_{DD} - 0.7V
Data Out Sink Current	I_{SINK}	1.5		1.6	1.8		1.5		mA	V_{OUT} = 0.7V

AC Characteristics

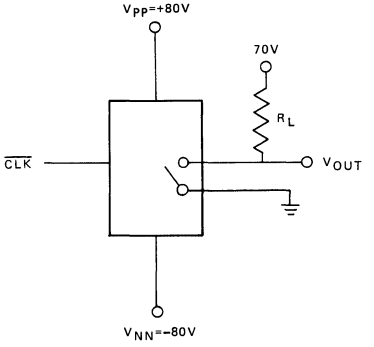
Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Set Up Time Before LE Rises	t_{SD}			260					ns	
Time Width of LE	t_{WLE}			300					ns	
Clock Delay Time to Data Out	t_{DO}				250	330			ns	
Turn On Time	t_{ON}		5		2.5	5		5	µs	
Turn Off Time	t_{OFF}		10		5.0	10		10	µs	
Off Isolation	KO			35	45				dB	f = 5MHz
Max Clock Freq	t_{CLK}					3			MHz	f_{DATA} = f_{CLK}/2
Set Up Time Data to Clock	t_{SU}			0					ns	
Hold Time Data from Clock	t_h			35					ns	

Recommended Operating Conditions

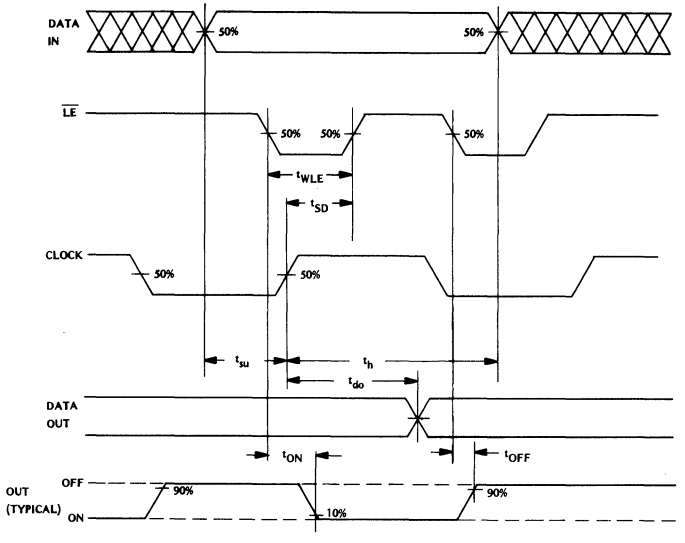
Symbol	Parameter	Device		Value
		HV1614	HV1616	
V_{DD}	Logic power supply voltage	X	X	+10.0V to +15.5V
V_{PP}	Positive high voltage supply	X		+50.0V to +70.0V
			X	+50.0V to +80.0V
V_{NN}	Negative high voltage supply	X		-50.0V to -70.0V
			X	-50.0V to -80.0V
V_{IH}	High level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free air-temperature	X	X	0° to 70°C

Note: For non-ground referenced systems the following must be used:
Power up sequence: GND VNN VDD VPP
Power down sequence: VPP VDD VNN GND

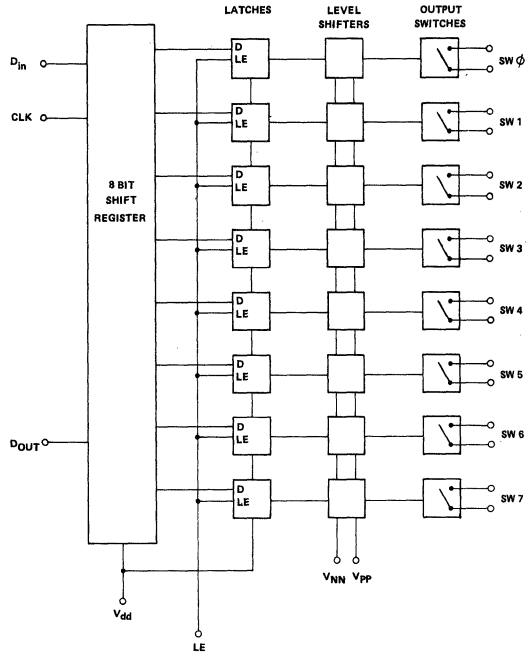
T_{ON}/T_{OFF} Measurement Circuit



Logic Timing Waveforms



Logic Diagram



Truth Table

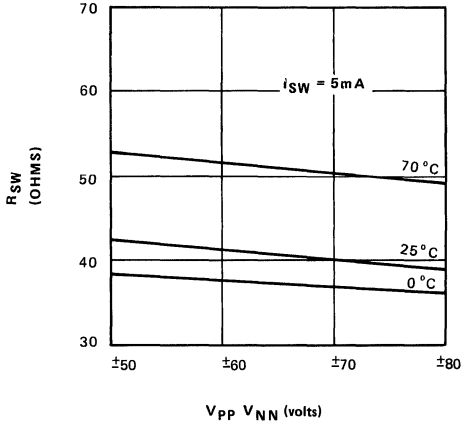
D0	D1	D2	D3	D4	D5	D6	D7	LE	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	OFF							
H								L	ON							
	L							L		OFF						
	H							L		ON						
		L						L			OFF					
		H						L			ON					
			L					L				OFF				
			H					L				ON				
				L				L					OFF			
				H				L					ON			
					L			L						OFF		
					H			L						ON		
						L		L							OFF	
						H		L							ON	
							L	L								OFF
							H	L								ON
X	X	X	X	X	X	X	X	H	HOLD PREVIOUS STATE							

Notes:

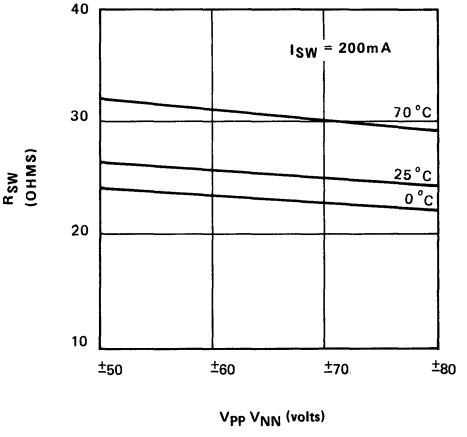
1. The eight switches operate independently
2. Serial data is clocked in on the L→H transition of CK.
3. The switches go to a state retaining their present condition at the rising edge of LE. When LE is low, the shift register data flows through the latch.
4. D_{OUT} is high when switch 7 is on.
5. Shift register clocking has no effect on the switch states if LE is H.

Typical Performance Curves

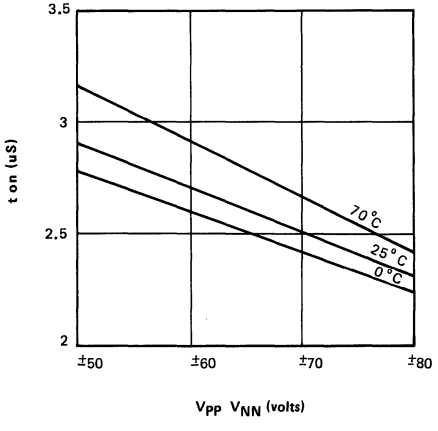
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



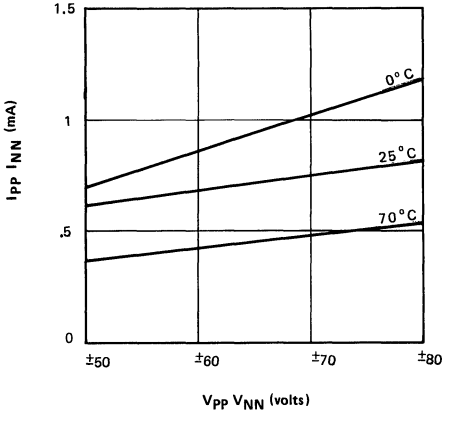
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



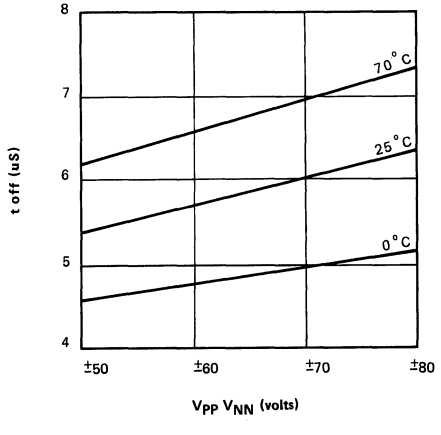
TYPICAL
t on (uS) vs. V_{PP} V_{NN}



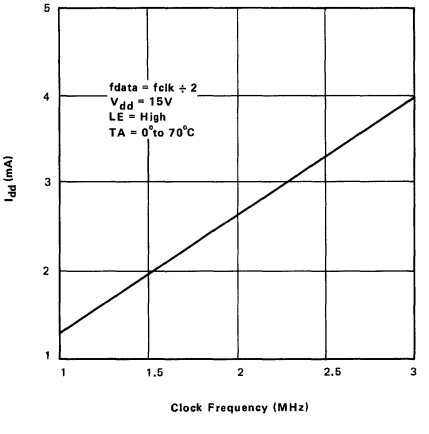
TYPICAL
I_{PP} I_{NN} vs. V_{PP} V_{NN} (ONE SWITCH ON)



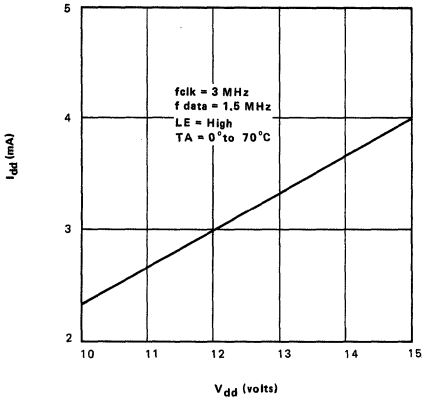
TYPICAL
t_{off} vs. V_{PP} V_{NN}



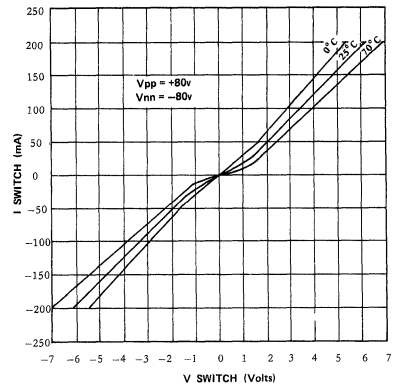
TYPICAL
Idd vs. Frequency



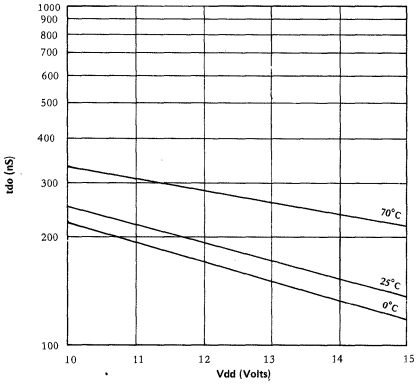
TYPICAL
Idd vs. Vdd



TYPICAL
SWITCH CURRENT vs VOLTAGE



TYPICAL
tdo vs Vdd



Pin Configurations

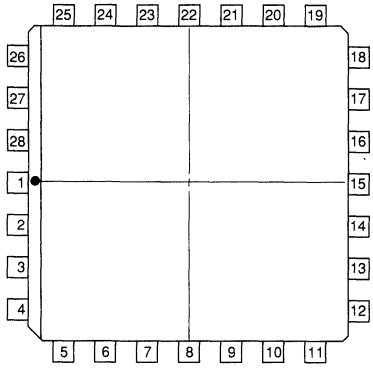
28-Pin J-Lead

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	LE
5	N/C	19	D_{OUT}
6	N/C	20	SW7
7	SW1	21	SW7
8	SW1	22	SW6
9	SW0	23	SW6
10	SW0	24	N/C
11	V_{PP}	25	SW5
12	V_{NN}	26	SW5
13	GND	27	SW4
14	V_{DD}	28	SW4

24-Pin DIP

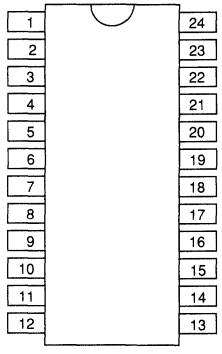
Pin	Function	Pin	Function
1	SW3	13	D_{IN}
2	SW3	14	CK
3	SW2	15	LE
4	SW2	16	D_{OUT}
5	SW1	17	SW7
6	SW1	18	SW7
7	SW0	19	SW6
8	SW0	20	SW6
9	V_{PP}	21	SW5
10	V_{NN}	22	SW5
11	GND	23	SW4
12	V_{DD}	24	SW4

Package Outlines



top view

28-pin J-lead Package



top view

24-pin DIP

4-Channel High Voltage Switch

Ordering Information

V_{PP}	V_{NN}	V_{SIG}	Package Options		
			16-pin ceramic side-brazed DIP	16-pin Plastic DIP	Die in waffle pack
+70V	-70V	110V P-P	HV1714C	HV1714P	HV1714X
+80V	-80V	130V P-P	HV1716C	HV1716P	HV1716X

Features

- ☐ HVCMOS® Technology
- ☐ Up to 130V peak to peak switching capability
- ☐ Output On-resistance typically 25 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10MHz analog signal frequency
- ☐ 45 dB typical output off isolation at 5 MHz
- ☐ CMOS logic circuitry for low power and excellent noise immunity

Absolute Maximum Ratings*

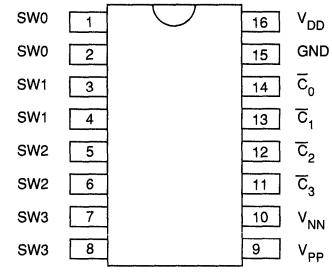
V_{DD} Logic power supply voltage	-0.5V to +18V
V_{PP} Positive high voltage supply	-0.5V to +90V
V_{NN} Negative high voltage supply	+0.5V to -90V
Logic input voltages	-0.5V to V_{DD} +0.3V
Peak analog signal current/channel	3A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

General Description

This device is a 4-channel high-voltage switch intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Pin Configuration



top view

16-pin DIP

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{SW}		35		25	40		45	ohms	I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		25		15	30		35	ohms	I_{SW} = 200mA
Switch (ON) Resistance	R_{SW}		35		28	40		50	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		30		18	35		40	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 200mA
Switch (ON) Resistance Matching	R_{SW}		15		5	15		15	%	I_{SW} = 5mA
Switch Off Leakage	I_{SWL}		50		0.5	50		150	µA	V_{OUT} = V_{PP} -10V thru 10K with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	RL = 100K
DC Offset Switch On			500		100	500		500	mV	RL = 100K
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current Neg. HV Supply Current	I_{PPQ} I_{NNQ}				50 -50	200 -200			µA µA	ALL SWS OFF
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				1.6 -1.6	3.2 -3.2			mA mA	1 SW ON
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				1.2 -1.2	2.4 -2.4			mA mA	V_{PP} = +50V V_{NN} = -50V 1 SW ON
Switch Output Peak Current					3				A	
Logic Supply Current	I_{DD}				0.001	0.5			mA	

AC Characteristics

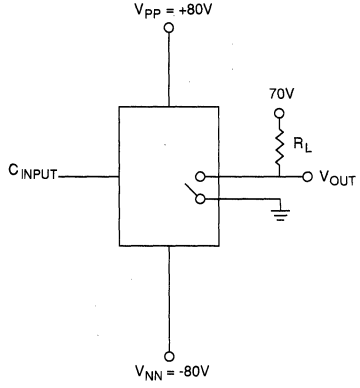
Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Turn On Time	t_{ON}	2.5	5		2.5	5	2.5	5	µs	
Turn Off Time	t_{OFF}	5.0	10		5.0	10	5.0	10	µs	
Off Isolation	KO			35	45				dB	f = 5MHz

Recommended Operating Conditions

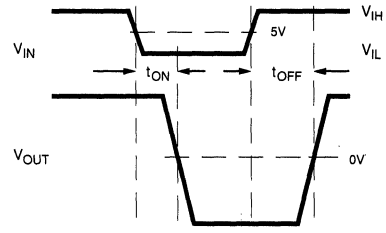
Symbol	Parameter	Device		Value
		HV1714	HV1716	
V_{DD}	Logic power supply voltage	X	X	+10.0V to +15.5V
V_{PP}	Positive high voltage supply	X		+50.0V to +70.0V
			X	+50.0V to +80.0V
V_{NN}	Negative high voltage supply	X		-50.0V to -70.0V
			X	-50.0V to -80.0V
V_{IH}	High level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free air-temperature	X	X	0° to 70°C

Note: For non-ground referenced systems the following must be used:
Power up sequence: GND VNN VDD VPP
Power down sequence: VPP VDD VNN GND

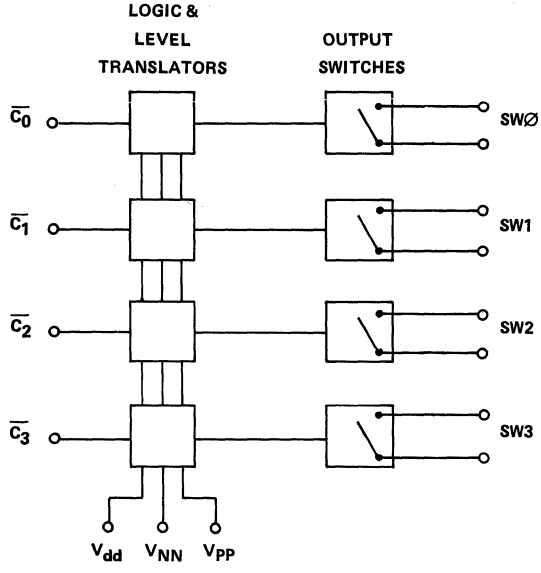
T_{ON}/T_{OFF} Measurement Circuit



Switching Waveforms

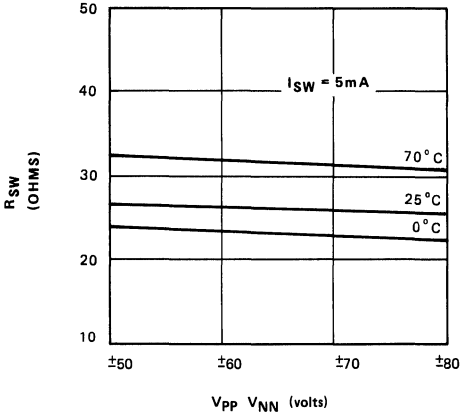


Logic Diagram

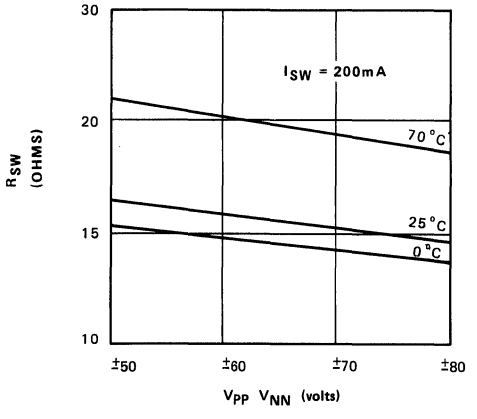


Typical Performance Curves

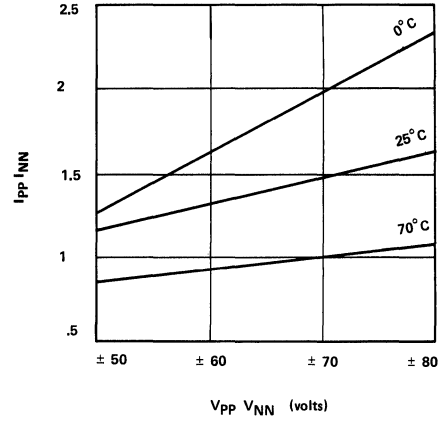
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



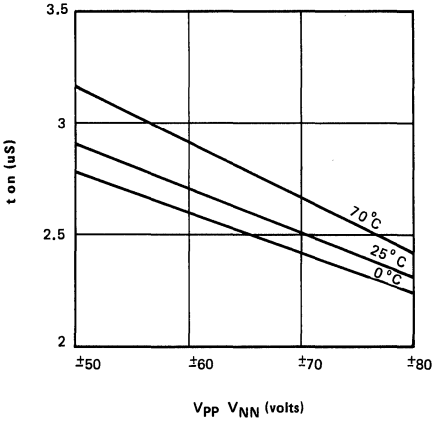
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



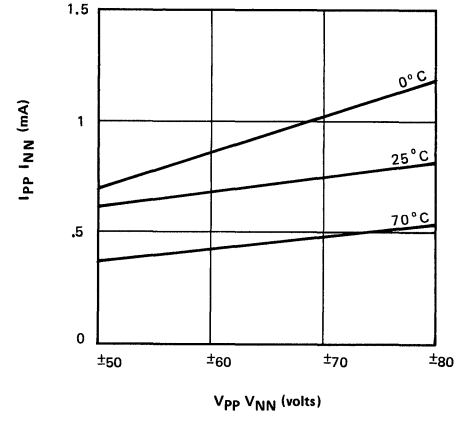
TYPICAL
I_{PP} I_{NN} vs. V_{PP} V_{NN} (ONE SWITCH ON)



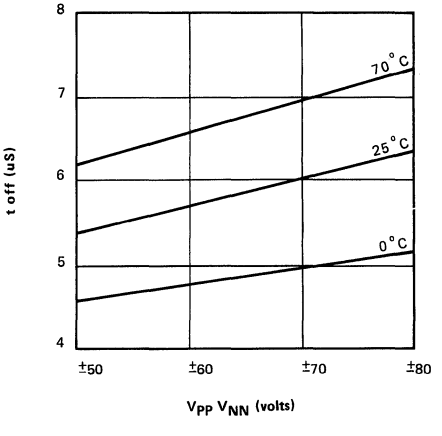
TYPICAL
t on (uS) vs. V_{PP} V_{NN}



TYPICAL
I_{PP} I_{NN} vs. V_{PP} V_{NN} (ONE SWITCH ON)

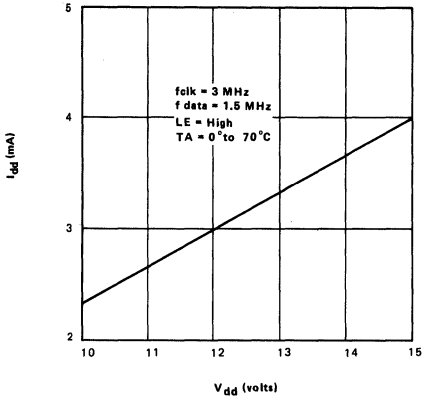


TYPICAL
t_{off} vs. V_{PP} V_{NN}

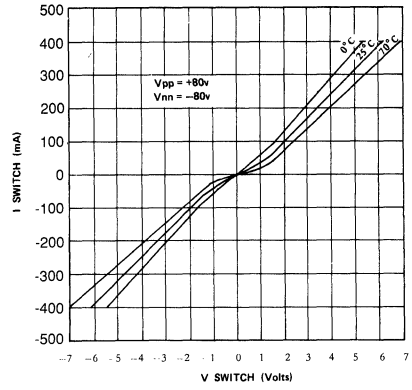


11

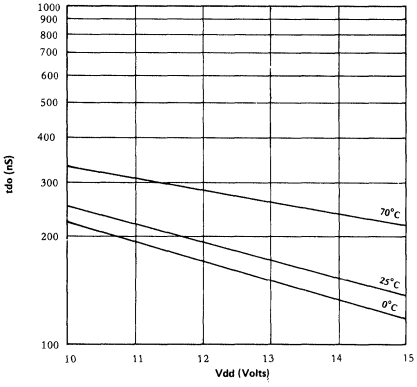
TYPICAL
Idd vs. Vdd



TYPICAL
SWITCH CURRENT vs VOLTAGE



TYPICAL
tdo vs Vdd



Preliminary

8-Channel High Voltage Switch

Ordering Information

V_{PP}	V_{NN}	V_{SIG}	Package Options				
			28-Pin Ceramic Side-Brazed DIP	Die in Waffle Pack	36-Pin Leaded Ceramic Chip Carrier	28-Lead Plastic Quad "J" Bend	28-Pin Plastic DIP
+70V	-70V	110V P-P	HV1814C	HV1814X	HV1814CS	HV1814PJ	HV1814P
+80V	-80V	130V P-P	HV1816C	HV1816X	HV1816CS	HV1816PJ	HV1816P

Features

- ☐ HVCMOS® Technology
- ☐ Up to 130V peak to peak output switching
- ☐ Output On-resistance typically 40 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10 MHz analog signal frequency
- ☐ 45 dB typical output off isolation at 5 MHz
- ☐ CMOS logic circuitry for low power and excellent noise immunity
- ☐ On-chip shift register, latch with clear function and chip select logic circuitry

General Description

This device is an 8-channel high-voltage integrated circuit (HVIC) intended for use in applications requiring high voltage switching controlled by low voltage signals: e.g., ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Absolute Maximum Ratings*

V_{DD} Logic power supply voltage	-0.5V to +18V
V_{PP} Positive high voltage supply	-0.5V to +90V
V_{NN} Negative high voltage supply	+0.5V to -90V
Logic input voltages	-0.5V to V_{DD} + 0.3V
Peak analog signal current/channel	1.5A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

Electrical Characteristics (over recommended operating conditions unless otherwise noted)

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{SW}		50		40	50		60	ohms	I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		35		25	35		45	ohms	I_{SW} = 200mA
Switch (ON) Resistance	R_{SW}		55		45	55		65	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		40		25	40		50	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 200mA
Switch (ON) Resistance Matching (0-7)	R_{SW}		15			15		15	%	I_{SW} = 5mA V_{PP} = 50V, V_{NN} = -50V
Switch Off Leakage	I_{SWL}		50		0.5	50		150	µA	V_{OUT} = V_{PP} -10V thru 10K with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	RL = 100K
DC Offset Switch On			500		100	500		500	mV	RL = 100K
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current Neg. HV Supply Current	I_{PPQ} I_{NNQ}		200 -200		50 -50	200 -200		200 -200	µA µA	ALL SWS OFF
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				0.8 -0.8	1.6 -1.6			mA mA	1 SW ON I_{SW} = 5mA
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				0.6 -0.6	1.2 -1.2			mA mA	V_{PP} = +50V V_{NN} = -50V 1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					1.5				A	
Logic Supply Current	I_{DD}				4	6			mA	f_{CLK} = 3MHz
Logic Supply Current	I_{DD}				0.001	0.5			mA	
Data Out Source Current	I_{SOR}	0.7		0.8	0.9		0.7		mA	V_{OUT} = V_{DD} - 0.7V
Data Out Sink Current	I_{SINK}	1.5		1.6	1.8		1.5		mA	V_{OUT} = 0.7V

AC Characteristics

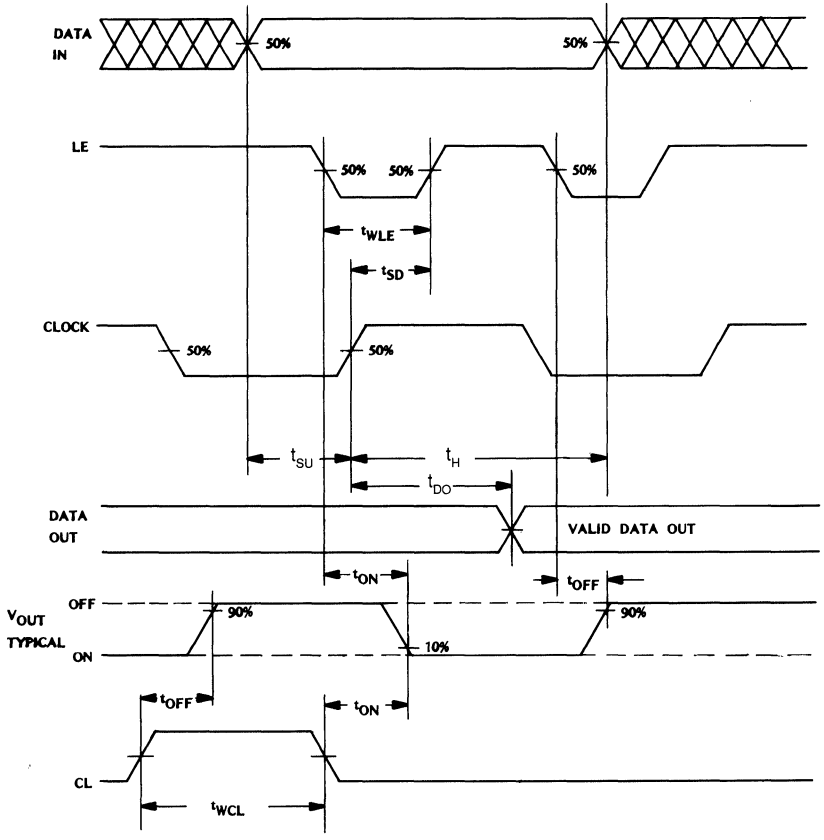
Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Max Clock Freq	f_{CLK}					3			MHz	f_{DATA} = f_{CLK}/2
Set Up Time Data to Clock	t_{SU}			0					ns	
Hold Time Data to Clock	t_h			35					ns	
Set Up Time Before LE Rises	t_{SD}			260					ns	
Time Width of LE	t_{WLE}			300					ns	
Clock Delay Time to Data Out	t_{DO}				250	330			ns	
Turn On Time	t_{ON}		5		2.5	5		5	µs	
Turn Off Time	t_{OFF}		10		5	10		10	µs	
Time Width of CL	t_{WCL}			100					ns	
Off Isolation	KO			35	45				dB	f = 5MHz

Recommended Operating Conditions

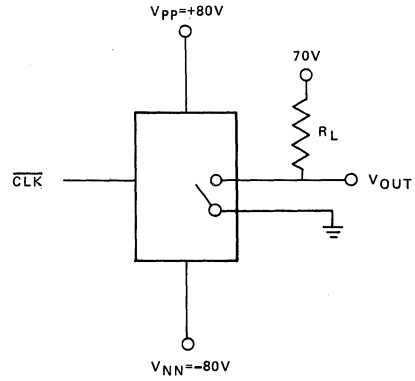
Symbol	Parameter	Device		Value
		HV1814	HV1816	
V_{DD}	Logic power supply voltage	X	X	+10.0V to +15.5 V
V_{PP}	Positive high voltage supply	X		+50.0V to +70.0V
			X	+50.0V to +80.0V
V_{NN}	Negative high voltage supply	X		-50.0V to -70.0V
			X	-50.0V to -80.0V
V_{IH}	High-level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free-air temperature	X	X	0°C to 70°C

Note: For non-ground referenced systems the following must be used:
Power up sequence: GND VNN VDD VPP
Power down sequence: VPP VDD VNN GND

Logic Timing Waveform



T_{ON}/T_{OFF} Measurement Circuit



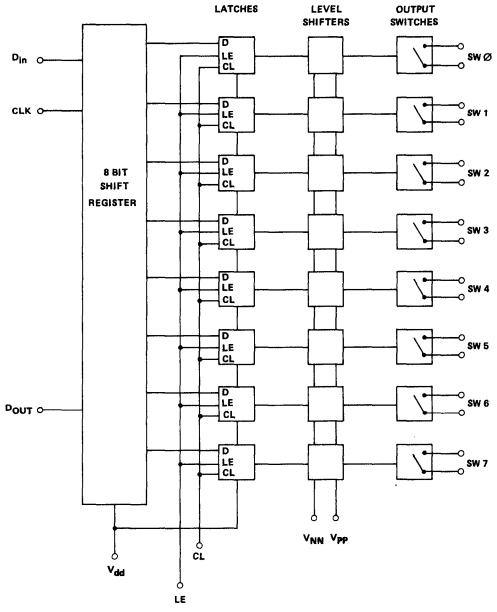
Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	LE	CL	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							

Notes:

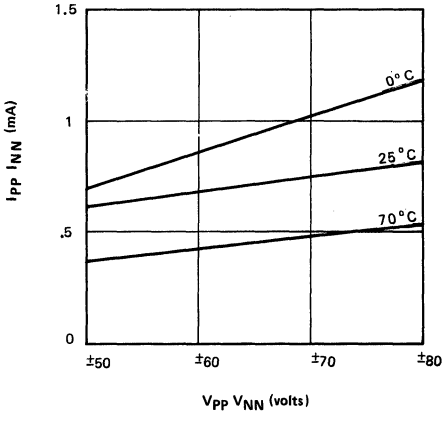
1. The eight switches operate independently.
2. Serial data is clocked in on the L→H transition of CK.
3. The clear input overrides all other inputs.
4. The switches go to a state retaining their present condition at the rising edge of LE. When LE is low, the shift register data flows through the latch.
5. D_{OUT} is high when switch 7 is on.
6. Shift register clocking has no effect on the switch states if LE is H.

Logic Diagram

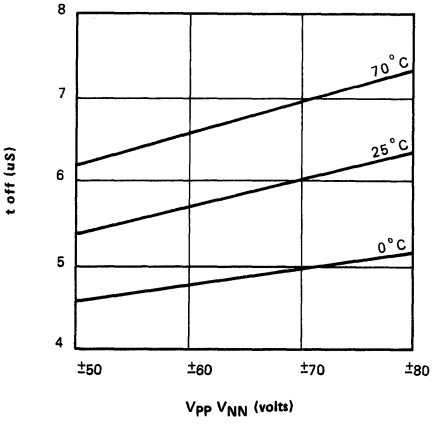


Typical Performance Curves

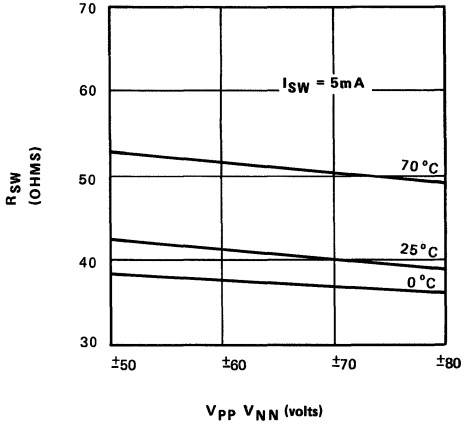
TYPICAL
I_{PP} I_{NN} vs. V_{PP} V_{NN} (ONE SWITCH ON)



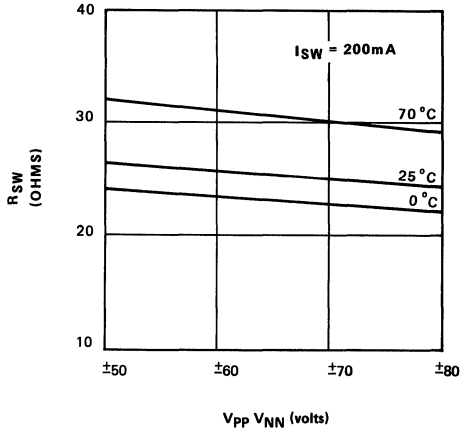
TYPICAL
t_{off} vs. V_{PP} V_{NN}



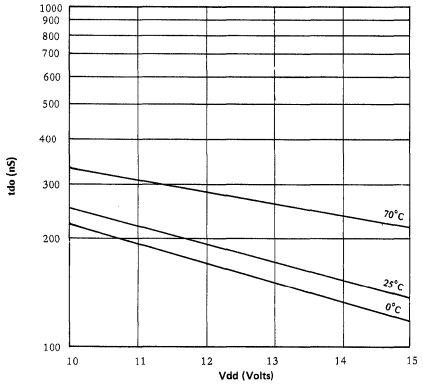
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



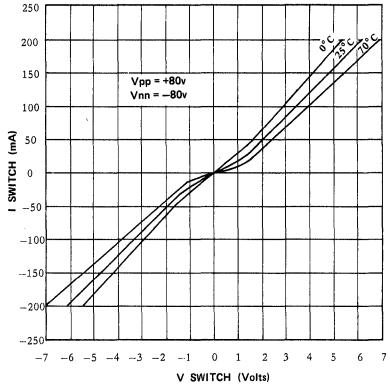
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



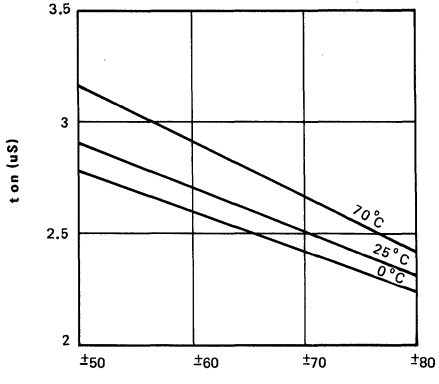
TYPICAL
tdo vs Vdd



TYPICAL
SWITCH CURRENT vs VOLTAGE



TYPICAL
t on (uS) vs. V_{PP} V_{NN}



Pin Configurations

36-Pin Leaded Chip Carrier

Pin	Function	Pin	Function
1	SW3	19	N/C
2	SW3	20	D_{IN}
3	N/C	21	CK
4	SW2	22	LE
5	SW2	23	CL
6	N/C	24	D_{OUT}
7	SW1	25	SW7
8	SW1	26	SW7
9	N/C	27	N/C
10	SW0	28	SW6
11	SW0	29	SW6
12	N/C	30	N/C
13	N/C	31	SW5
14	V_{PP}	32	SW5
15	V_{NN}	33	N/C
16	GND	34	SW4
17	V_{PP}	35	SW4
18	N/C	36	N/C

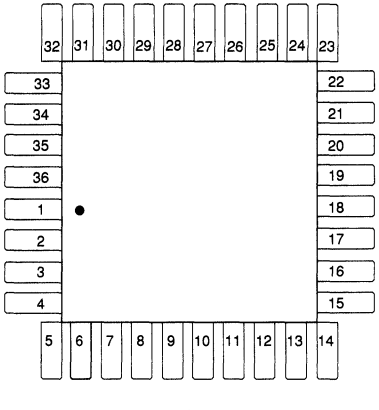
28-Pin DIP

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CK
4	SW2	18	LE
5	SW1	19	CL
6	SW1	20	D_{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	V_{PP}	23	SW6
10	V_{NN}	24	SW6
11	N/C	25	SW5
12	GND	26	SW5
13	V_{DD}	27	SW4
14	N/C	28	SW4

28-Pin J-Lead

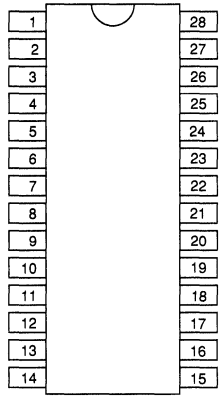
Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CK
4	SW2	18	LE
5	SW1	19	CL
6	SW1	20	D_{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	V_{PP}	23	SW6
10	V_{NN}	24	SW6
11	N/C	25	SW5
12	GND	26	SW5
13	V_{DD}	27	SW4
14	N/C	28	SW4

Package Outlines



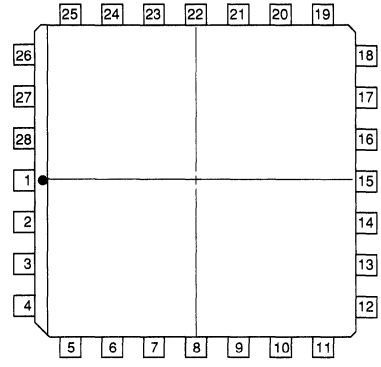
top view

36-pin Leaded Chip Carrier



top view

28-pin DIP



top view

28-pin J-lead Package

Preliminary

High Voltage 7-Segment Latch/Decoder/ EL-Display Driver

Ordering Information

Device	Package Options			
	20-Pin Ceramic	20-Pin CERDIP	20-Pin Plastic	Die
HV30	HV30C	HV30D	HV30P	HV30X

Features

- ☐ High voltage outputs 180V
- ☐ High current capability 50mA peak
- ☐ Wide termperature range -40°C to +85°C
- ☐ Latch storage of code and decimal point
- ☐ Blanking
- ☐ Lamp test capability
- ☐ Leading zero blanking

Absolute Maximum Ratings*

Supply voltage	4.75V to 12V
Input Voltage V_{IN}	-0.5V to V_{CC}
Output Voltage V_O	0V TO 180V
Output current I_O (continuous)	5mA
Output current I_O (peak)	60mA
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to 150°C

*Over operating free-air temperature range unless otherwise noted.

General Description

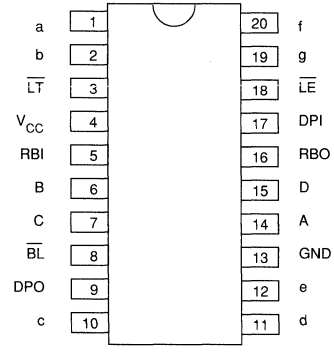
The HV30 is a 7-segment Decoder with decimal point and high voltage open drain outputs. It is specifically designed to drive electroluminescent displays manufactured by the Lohja Corporation but can also be used to drive other displays.

The BCD and decimal point inputs are latched on the trailing edge of the latch enable LE input.

All high voltage outputs can be put in the high impedance state by either the blanking input (BI) or the ripple blanking input (RBI) when the BCD data is all "0".

All outputs can be put in the low impedance state by bringing the lamp test low. There is an internal pull-down resistor on the lamp test input. All other inputs are protected with a zener diode to ground and a series resistor.

Pin Configuration



top view

20-pin DIP

Electrical Characteristics (Over operating free-air temperature range, unless otherwise noted)

DC Characteristic

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{CC}	Supply voltage	4.75	10	12	V	
I_{CC}	Supply current		5	10	mA	V_{CC} = 10V, all inputs low except LT = "1"
V_{IL}	Input low voltage	-0.5		0.8	V	V_{CC} = 10V
V_{IH}	Input high voltage	6.5		V_{CC}	V	V_{CC} = 10V
V_{OL}	Output low voltage, RBO			0.45	V	V_{CC} = 10V, I_{OH} = 0.9mA
V_{OH}	Output high voltage, RBO	2.4			V	V_{CC} = 10V, I_{OH} = 0.9mA
The following specifications are for segment outputs (@ V_{CC} = 10V):						
I_O (continuous)	Output current			5	mA	
I_O (peak)	Output current			50	mA	Note 1
I_O (leakage)	Output current			2	µA	Note 2
I_D (continuous)	Body diode current			-5	mA	
I_D (peak)	Body diode current			-60	mA	Note 1
V_{OBR}	Breakdown voltage	180			V	Note 3
V_{FD}	Forward voltage drop across body diode			2.0	V	Note 4
$R_{DS(ON)}$	Drain to source resistance			1000	Ω	Note 5

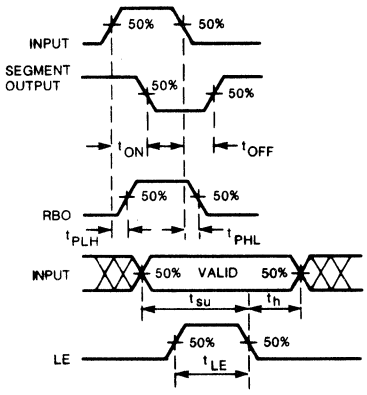
Notes: 1. Peak Current is repetitive; fmax = 1.5KHz, max duty cycle = 8.0%.
2. BL - input at high level V_O = +180V, T_A = +85°C.
3. I_O leakage max 2.0µA.
4. Diode Forward current 30mA.
5. I_O = 10mA.

AC Characteristics (V_{CC} = +10V, T_A = 25°C)

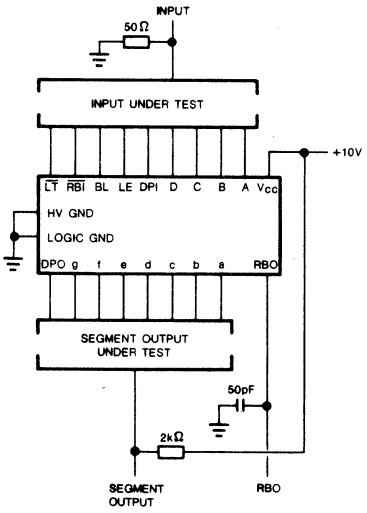
Symbol	Parameter	Min	Max	Units	Conditions
t_{ON}(BCD)	Turn-on time of segment outputs from BCD-inputs		10	µs	Note 1
t_{ON}(DPI)	Turn-on time of decimal point output from decimal point input		10	µs	Note 1
t_{ON}(BL)	Turn-on time of segment outputs from blank input		10	µs	Note 1
t_{OFF}(BCD)	Turn-off time of segment outputs from BCD-inputs		10	µs	Note 1
t_{OFF}(DPI)	Turn-off time of decimal point output from decimal point input		10	µs	Note 1
t_{OFF}(BL)	Turn-off time of segment outputs from blank input		10	µs	Note 1
t_{SU}	Data set-up time		2	µs	
t_H	Data hold time		2	µs	
t_{LE}	Minimum valid latch enable pulse width		2	µs	
t_{PLH}	Propagation delay from RBI to RBO		2	µs	Note 2
t_{PHL}	Propagation delay from RBI to RBO		2	µs	Note 2
t_{ON}(RBI)	Turn-on time of segment outputs from RBI-input		10	µs	Note 3
t_{OFF}(RBI)	Turn-off time of segment outputs from RBI-input		10	µs	Note 3

Notes: 1. $\overline{LE}$ input is at high level.
2. $\overline{LE}$ input is at high level and input BCD code is 0.
3. $\overline{LE}$ input is at high level, input BCD code is 0 and BL input is at low level.

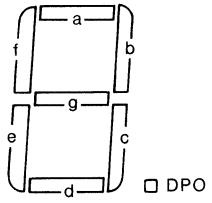
Switching Waveform



Test Circuit



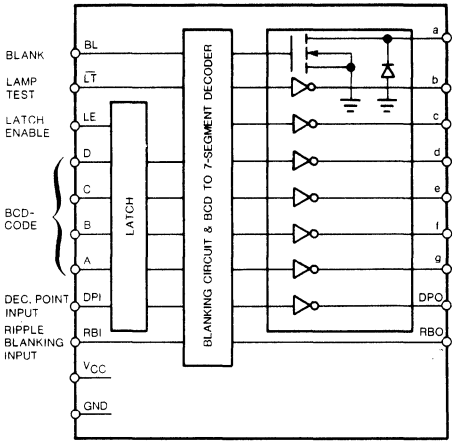
Segment Identification



H = High level
L = Low level
X = Irrelevant

Notes: 1. The segment outputs are ON or OFF according to data present on the input lines during the high to low transition of latch enable signal.
2. If the latched BCD data is 0, RBO is at high level and the segment outputs except DPO are blanked. The state of DPO is determined by the latched DPI data. If the latched BCD data is greater than 0, RBO is at low level and the segment outputs are on or off according to the latched data.
3. If the latched BCD data is 0, RBO is at high level. If the latched BCD data is 0, RBO is at high level. If the latched BCD data is greater than 0, RBO is at low level.

Logic Diagram



Truth Table

INPUTS									OUTPUTS									DISPLAY
$\overline{LT}$	RBI	DP-INPUT	BCD-INPUTS				$\overline{LE}$	BL	RBO	SEGMENT OUTPUTS								
			D	C	B	A				a	b	c	d	e	f	g	DPO	
H	L	X	L	L	L	L	H	L	L	ON	ON	ON	ON	ON	ON	OFF	X	0
H	H	X	L	L	L	L	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
H	X	X	L	L	L	H	H	L	L	OFF	ON	ON	OFF	OFF	OFF	OFF	X	1
H	X	X	L	L	H	L	H	L	L	ON	ON	OFF	ON	ON	OFF	ON	X	2
H	X	X	L	L	H	H	H	L	L	ON	ON	ON	ON	OFF	OFF	ON	X	3
H	X	X	L	H	L	L	H	L	L	OFF	ON	ON	OFF	OFF	ON	ON	X	4
H	X	X	L	H	L	H	H	L	L	ON	OFF	ON	ON	OFF	ON	ON	X	5
H	X	X	L	H	H	L	H	L	L	ON	OFF	ON	ON	ON	ON	ON	X	6
H	X	X	L	H	H	H	H	L	L	ON	ON	ON	OFF	OFF	OFF	OFF	X	7
H	X	X	H	L	L	L	H	L	L	ON	ON	ON	ON	ON	ON	ON	X	8
H	X	X	H	L	L	H	H	L	L	ON	ON	ON	ON	OFF	ON	ON	X	9
H	X	X	H	L	H	L	H	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
H	X	X	H	L	H	H	H	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
H	X	X	H	H	L	L	H	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
H	X	X	H	H	L	H	H	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
H	X	X	H	H	H	L	H	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
H	X	X	H	H	H	H	H	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
H	X	L	X	X	X	X	H	L	X	X	X	X	X	X	X	X	OFF	
H	X	H	X	X	X	X	H	L	X	X	X	X	X	X	X	X	ON	
H	L	X	X	X	X	X	L	L	L	Note 1								
H	H	X	X	X	X	X	L	L	Note 2	Note 2								
H	L	X	X	X	X	X	L	H	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
H	H	X	X	X	X	X	L	H	Note 3	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
H	L	X	X	X	X	X	H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
H	H	X	L	L	L	L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
H	H	X	Greater Than BCD 0				H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
L	X	X	X	X	X	X	X	X	X	ON	ON	ON	ON	ON	ON	ON	ON	8.

High Voltage Analog Switches

Ordering Information

Function			Dual SPST	Dual SPDT	Dual DPST	Dual SPST
Analog Signal Range			V_{NN} to V_{PP}	V_{NN} to V_{PP}	V_{NN} to V_{PP}	V_{NN} to V_{PP}
$RDS_{(ON)}$			100 ohms	100 ohms	100 ohms	55 ohms
Order No. and Part Type	Package Type	Temp Range				
	16-lead CERDIP, Hi-Rel	-55°C to +125°C	RBHV341D	RBHV343D	RBHV345D	RBHV348D
	16-lead CERDIP, Mil-Temp	-55°C to +125°C	HV341D	HV343D	HV345D	HV348D
	16-lead CERDIP	-20°C to + 85°C	HV341MD	HV343MD	HV345MD	HV348MD
	16-lead small outline*	-20°C to + 85°C	HV341MWG	HV343MWG	HV345MWG	HV348MWG
	16-lead small outline*	0°C to + 70°C	HV341WG	HV343WG	HV345WG	HV348WG
	16-lead plastic DIP	0°C to + 70°C	HV341P	HV343P	HV345P	HV348P
	Die in waffle pack	0°C to + 70°C	HV341X	HV343X	HV345X	HV348X

*300 mil wide SO package

Features

- ☐ ±20V to ±50V single and dual supply operation
- ☐ R_{ON} less than 55Ω (HV348)
- ☐ Signal switching from positive to negative rail
- ☐ -50db OFF isolation at 5MHz
- ☐ Withstand +80V to -100 spikes
- ☐ Withstand V_{SIG} with power supply off

Applications

- ☐ Test Equipment and Instruments
- ☐ Diagnostic Systems
- ☐ 48 Volt Telecom Systems
- ☐ Military Electronics

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}		-0.3V to +65V
Supply voltage, V_{NN}		+0.3V to -65V
Data input voltage		V_{NN} to V_{PP}
Input current	Switches	±200mA
	Logic inputs	±30mA
Continuous total power dissipation[2]	Plastic Packages	500mW
	Ceramic Packages	750mW
Storage temperature range		-65°C to +150°C

Notes: 1. All voltages are referenced to V_{SS}.
2. For operation above 25°C ambient, derate linearly to 85°C at 8mW/°C.

General Description

These CMOS/DMOS high voltage analog switches are designed to handle high voltage analog signals. They may be used when analog voltages are low and high voltage immunity is desired. The signal handling capability extends from positive to negative supply voltage; i.e., 100V peak to peak with ±50V power supplies.

Inputs are compatible with CMOS logic, with a zero level turning the switches ON.

Operating supply voltage ranges from ±20V to ±50V with dual output power supplies, with the positive supply current below 300μA and negative supply not exceeding 100μA.

When a single output power supply is used, operating voltage ranges from +20V to +50V, with less than 20μA operating current when logic input signal equals the supply voltage.

With the addition of series diodes on the power supply and ground inputs, the HV341 series drivers will withstand +80V to -100V excursion on the inputs or switch pins without damage, or will withstand signal input with the power supplies OFF.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
V_{SIG}	Analog signal range		V_{NN}		V_{PP}	V	
R_{ON}	HV341/343/345	25°C		40	75	Ω	V_{SIG} = ±50V I_{SIG} = 10mA
		Over temp			100	Ω	
	HV348	25°C		25	50	Ω	
		Over temp			75	Ω	
R_{ON}	ON-Resistance matching			7		%	
V_{IL}	Input low threshold				3.5	V	
V_{IH}	Input high threshold		12			V	
I_{SOL}	Switch OFF leakage	25°C		10	60	nA	V_{SIG} = ±50V
		Over temp		1	5	µA	
I_{PP}	V_{PP} quiescent current			200	600	µA	
I_{NN}	V_{NN} quiescent current			15	100	µA	
I_{IN}	Logic input current			0.1	10	µA	V_{IN} = 0 to 15V
I_{SON}	Switch ON leakage	25°C		10	60	nA	V_{SIG} = ±50V
		Over temp		1	5	µA	

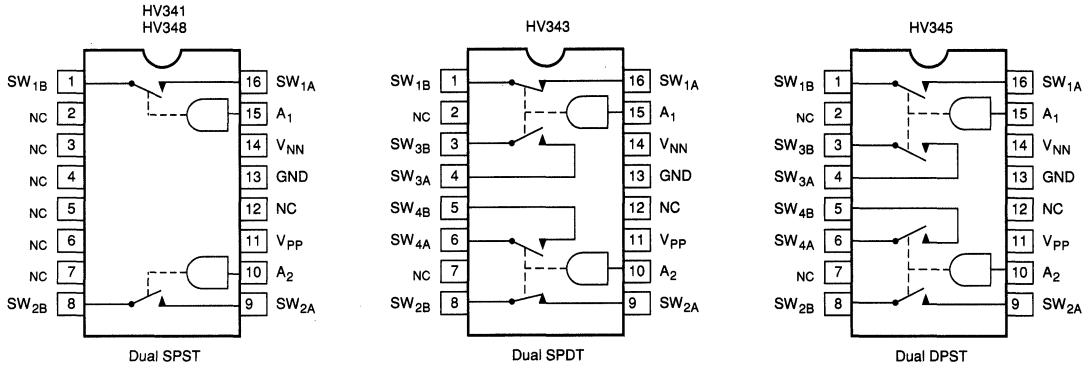
AC Characteristics (@ V_{DD} = 12V, V_{PP} = 60V, T_C = 25°C)

Symbol	Parameter		Min	Typ	Max	Units	Conditions
t_{ON}	Turn-ON time	25°C		0.5	1.0	µs	Figure 7
		Over temp			1.5	µs	
t_{OFF}	Turn-OFF time	25°C		0.4	0.75	µs	
		Over temp			1.0	µs	
K_O	OFF isolation			-70		dB	25°C, 1MHz
K_{CR}	Switch crosstalk			-75		dB	25°C, 1MHz
$C_{SW(OFF)}$	OFF capacitance across switch			1		pF	T_A = 25°C, V_S = 0V
$C_{SG(OFF)}$	OFF capacitance SW to GND			17		pF	
$C_{SG(ON)}$	ON capacitance SW to GND			38		pF	
Q	Charge injection			100		pC	V_{SIG} = +50V
				240		pC	V_{SIG} = 0V
				480		pC	V_{SIG} = -50V

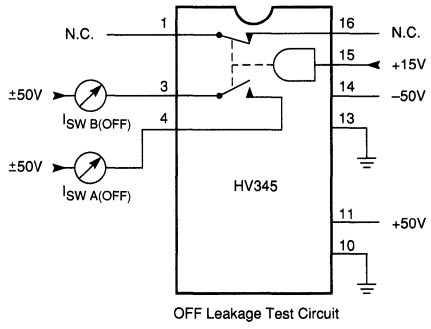
Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{NN}	Negative high voltage supply		-50		0	V
V_{PP}	High voltage supply		+20		+50	V
V_{IH}	High-level input voltage		+12		+50	V
V_{IL}	Low-level input voltage		-50		+3.5	V
Operating temperature range		Commercial	0		+70	°C
		Military Hi-Rel (RB)	-55		+125	°C

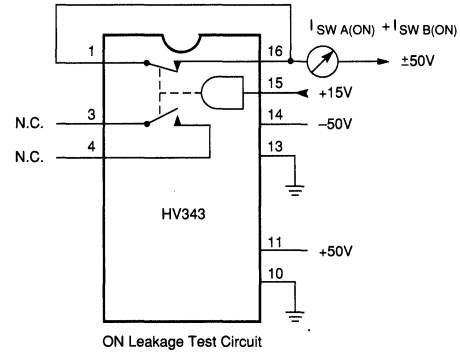
Functional Block Diagrams and Pin Configurations



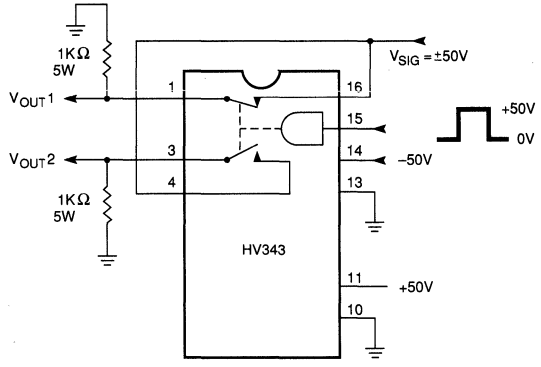
Test Circuits

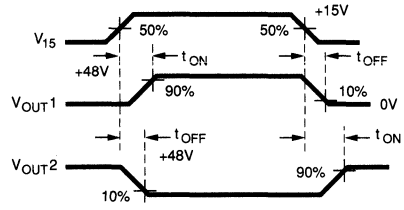


OFF Leakage Test Circuit

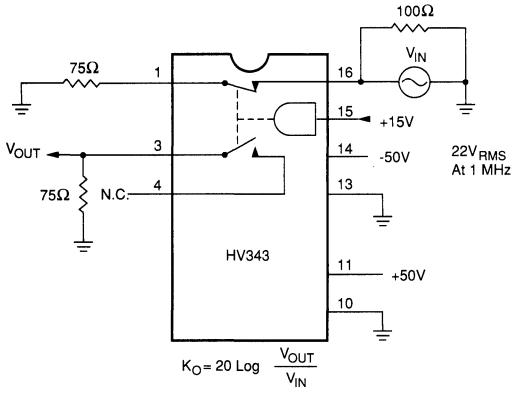


ON Leakage Test Circuit

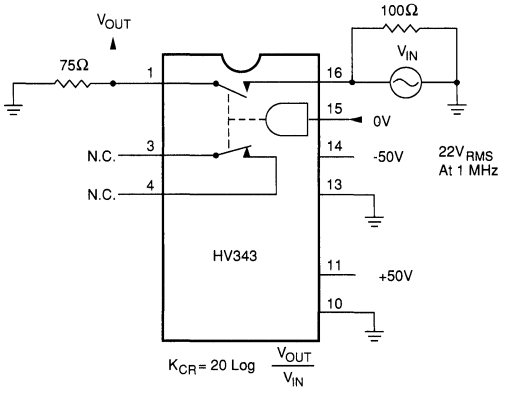




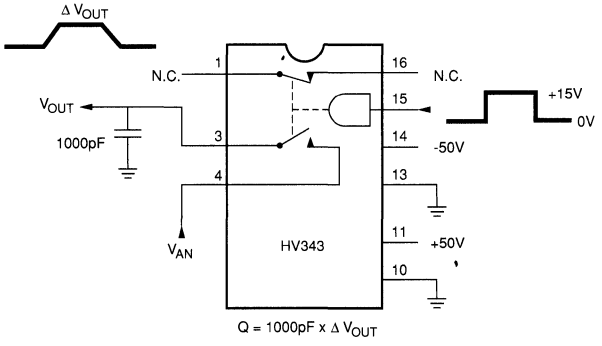
Switching Time Test Circuit



OFF Isolation Test Circuit



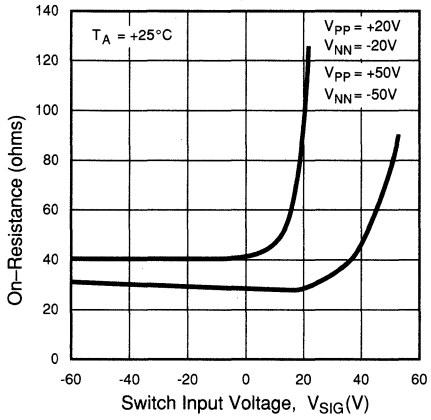
Channel–Channel Crosstalk Test Circuit



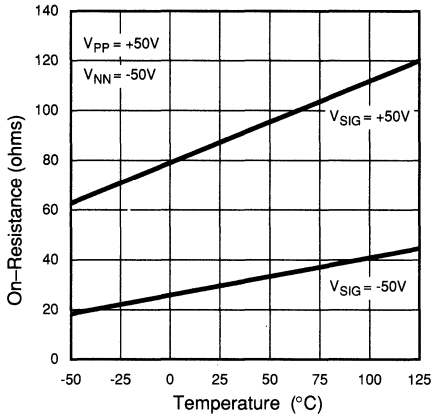
Charge Injection Test Circuit

Typical Operating Characteristics

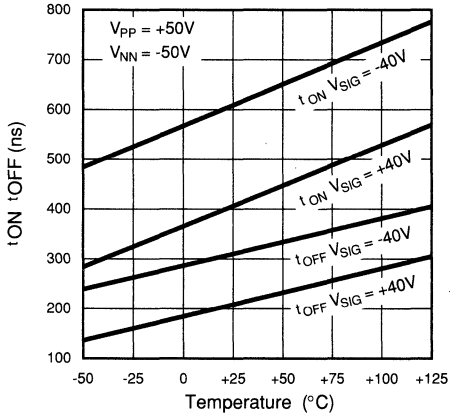
On–Resistance vs. Switch Input Voltage



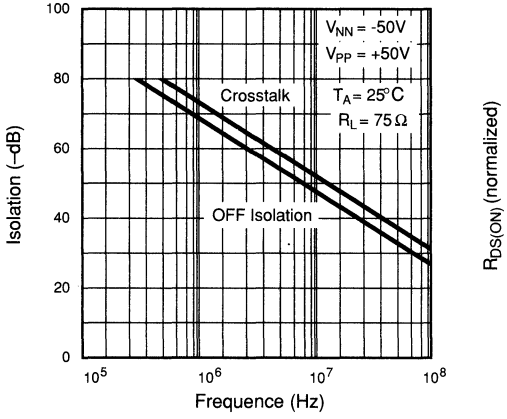
On-Resistance vs. Temperature



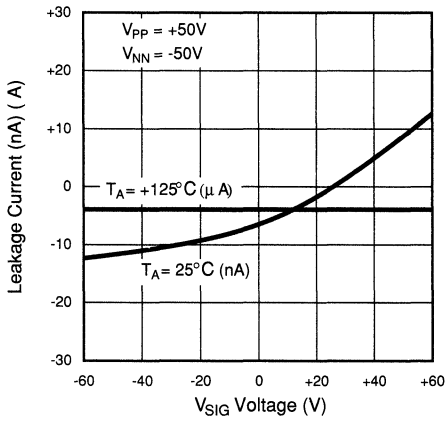
Switching Time vs. Temperature



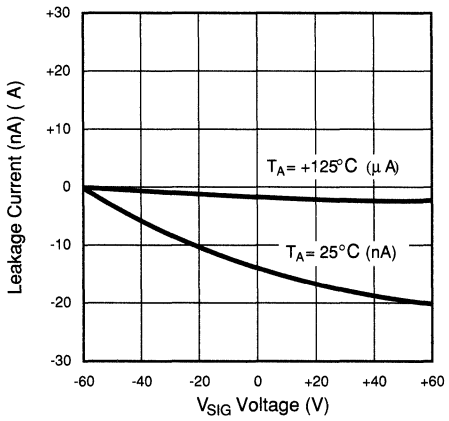
OFF Isolation And Crosstalk vs. Frequency



OFF Leakage vs. Switch Voltage



ON Leakage vs. Switch Voltage



Applications Information

Analog Signal Range

The HV341 family's analog signal range is equal to the power supply value, up to ±50V with split power supplies and +60V with a single power supply (V_{NN} connected to GND). An ON switch is also capable of passing up to 0.5A on a peak current basis. Maximum continuous current is limited only by the package power dissipation (see Absolute Maximum Ratings).

ON Resistance

The ON resistance of the MAX341 series switches is typically 40Ω. R_{ON} does, however, increase as the switch voltage (VSIG) approaches V_{PP}. For example, with ±50V supplies and a +50V analog signal, R_{ON} will be typically less than 100Ω (50Ω for the HV348), and 45Ω (25Ω for the HV348 for -50V signals. With ±50V power supplies , and ±40V switch voltages, R_{ON} is about 40Ω for the +40V case and 30Ω for the -40V case. ON resistance can be reduced and current handling capacity can be increased by connecting switches in parallel. This is especially useful in power switching applications. Table 1 and the graph in the Typical Characteristics section further describe the relation between R_{ON} and V_{PP}.

Power Supply Current

The maximum supply current for V_{PP} and V_{NN} at 25°C is 300µA and 100µA, respectively. However, the positive supply current (1+) is partly dependent on the input logic level and can be reduced if control signals of a larger amplitude than 0V and 15V are used. If the control inputs swing to within 4V of V_{PP} and V_{NN} then 1+ drops to a typical value of 200µA.

Control Inputs

15V logic level inputs are required to turn switches on or off, but the control inputs can also accept levels up to V_{PP} and V_{NN}. An input greater than 12V constitutes a "1" state (switch OFF), and an input less than 3.5V will constitute a "0" state (switch ON).

Standard TTL logic can be used with HV341 series switches if a level shifter such as the MC14504 is used to drive the control inputs as shown in Figure 1. Open collector drivers, with external pull-up resistors, can be used in a similar fashion as well.

Table 1: ON Resistance

V_{PP}/V_{NN}	R_{ON} at $V_{SIG} = V_{PP}$	R_{ON} at $V_{SIG} = V_{NN}$
+20V/-20V	127Ω	39Ω
+30V/-30V	105Ω	36Ω
+40V/-40V	92Ω	32Ω
+50V/-50V	84Ω	30Ω
+40V/GND	127Ω	39Ω
+60V/GND	105Ω	36Ω

Note: Typical R_{ON} for the HV348 is approximately one half of the above values.

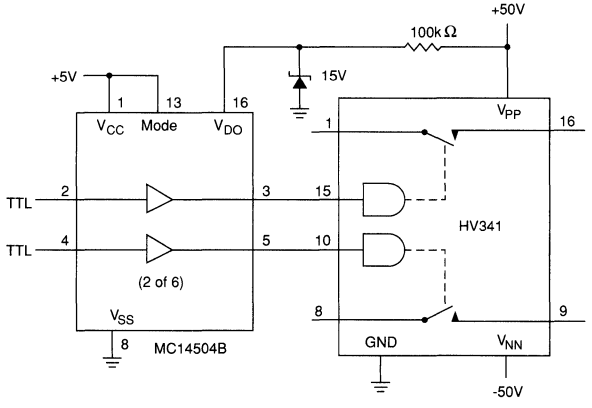


Figure 1. Using TTL Control Levels

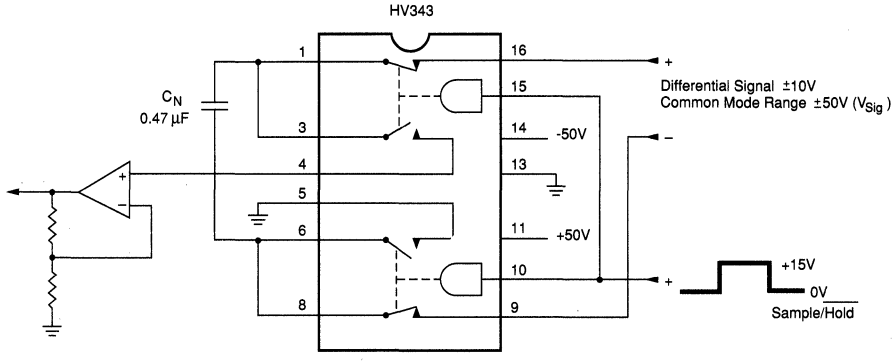


Figure 2. Flying Capacitor Differential to Single-Ended Converter With ±50V Common-Mode Range.

Flying Capacitor Input

A "flying capacitor" differential to single-ended converter takes advantage of the HV343's wide input voltage range, which allows large common mode inputs to be rejected. As shown in figure 2, a capacitor is alternately charged by the differential input signal and then is connected to an op-amp or A-to-D input. An instrumentation amplifier is not required since the output signal can be referenced to ground. Sample-hold operation is also built into the design and the HV343's break-before-make operation ensures that the output sees only the differential portion of the input signal. A similar approach can also be used for single-ended to differential signal conversion as well.

Parallel Switches

In designs where power switching ability is needed, any of the HV 341 series switches can be connected in parallel to increase current handling capability and reduce ON resistance. Applications such as ultrasonics, RF power, and DC motor drive are areas where this is often important. An HV348 is shown in a parallel configuration in Figure 3. The resulting SPST switch has a typical R_{ON} of 12Ω (5Ω for signals more than 10V below V_{PP}) and can handle pulsed loads of up to 0.5 Amps. With ±50V power supplies, the peak-to-peak signal range is still 100V, and 10MHz signals can be switched while maintaining typically -50dB of isolation.

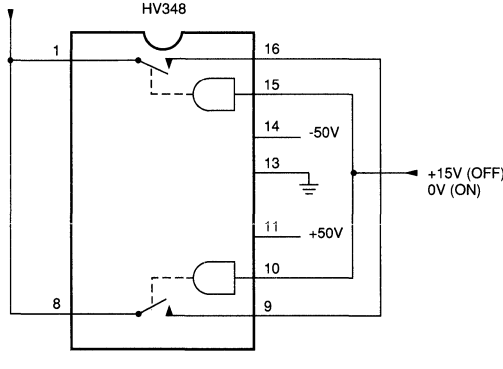


Figure 3. Minimum R_{ON} (5 to 10Ω typ.) High Voltage Switch.

Preliminary

32-Channel Serial To Parallel Converter With P-Channel Open Drain Outputs

Ordering Information

Device	Package Options		
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack
HV41	HV4122DJ	HV4122PJ	HV4122X
HV42	HV4222DJ	HV4222PJ	HV4222X

Features

- ☐ Processed with HVCMOS® technology
- ☐ Output voltages to -225V
- ☐ Source current minimum 80mA
- ☐ Shift register speed 8MHz
- ☐ Strobe and enable inputs
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options
- ☐ 44-lead plastic and ceramic surface mount packages
- ☐ Hi-Rel processing available
- ☐ Can be used with the HV51 and HV52 to provide 200V push-pull operation

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]	+0.5V to -15.5V
Off state output voltage[1]	+0.5V to -250V
Logic input levels[1]	+0.5V to V_{DD} - 0.5V
Ground current[2]	1.5A
Continuous total power dissipation[3]	1200mW
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C

Notes: 1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 85°C at 15mW/°C.

General Description

The HV41 and HV42 are low voltage serial to high voltage parallel converters wtih P-Channel open drain outputs.These devices have been designed for use as drivers for AC electroluminescent displays. They can also be used in any application requiring multiple output high voltage current source capabilities such as driving inkjet and electrostatic print heads, plasma panels, or vacuum fluorescent displays.

These devices consist of a 32-bit shift register and control logic to perform the Output Enable and All-ON functions. Data is shifted through the shift register on the logic high to low transition of the clock. The HV41 shifts in the counterclockwise direction when viewed from the top of the package and the HV42 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the OE (Output Enable) or the STR (Strobe) inputs.

For applications requiring active pull down as well as pull up, the HV41 and HV42 can be paired with the HV52 and HV51 devices, respectively. The footprint of the HV41 output pins matches the HV52 output pin footprint when the parts are mounted on opposite sides of a PC Board. Similarly the HV42 output footprint matches the HV51. The logic control and power pin locations do not match.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics (voltages referenced to V_{SS})

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			-15	mA	f_{CLK} = 4 MHz F_{DATA} = 2 MHz
I_{DDQ}	Quiescent V_{DD} supply current			-50	µA	ALL V_{IN} = 0V
$I_{O(OFF)}$	Off state output current			-50	µA	All SWS parallel
I_{IH}	High-level logic input current			-1	µA	V_{IH} = -12V
I_{IL}	Low-level logic input current			+1	µA	V_{IL} = 0V
V_{OH}	High-level output data out			V_{DD} + 1.0V	V	I_{Dout} = -100µA
V_{OL}	Low-level output voltage	HV_{out}	-30.0		V	I_{HVout} = -80mA
		Data out	-1.0		V	I_{Dout} = -100µA
V_{OC}	HV_{out} clamp voltage			+1.5	V	I_{OL} = +80mA

AC Characteristics (@ V_{DD} = -12V, V_{SS} = 0V)

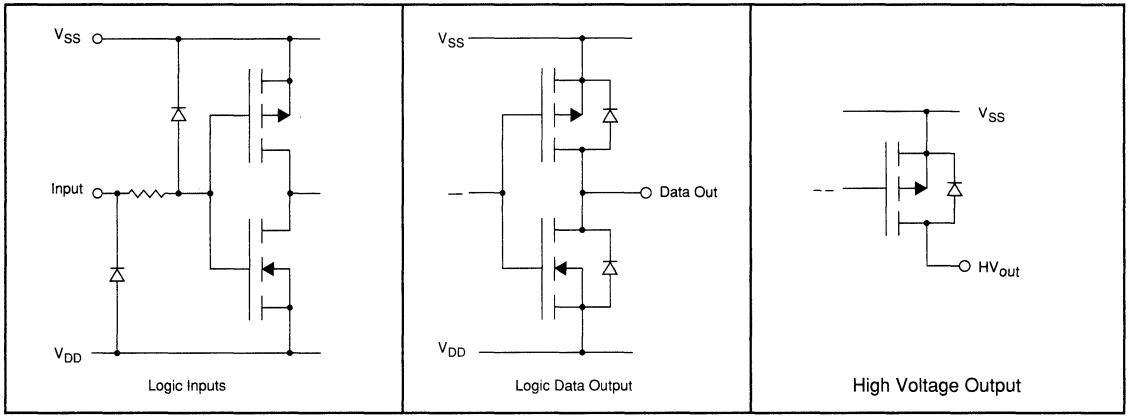
Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_{WH}/t_{WL}	Clock width high or low	125		ns	
t_{SU}	Data set-up time before clock rises	50		ns	
t_H	Data hold time after clock rises	20		ns	
t_{ON}	Turn ON time, HV_{out} from enable		400	ns	R_L = 10K to -225V
t_{DHL}	Delay time clock to data high to low		100	ns	
t_{DLH}	Delay time clock to data low to high		100	ns	

Recommended Operating Conditions

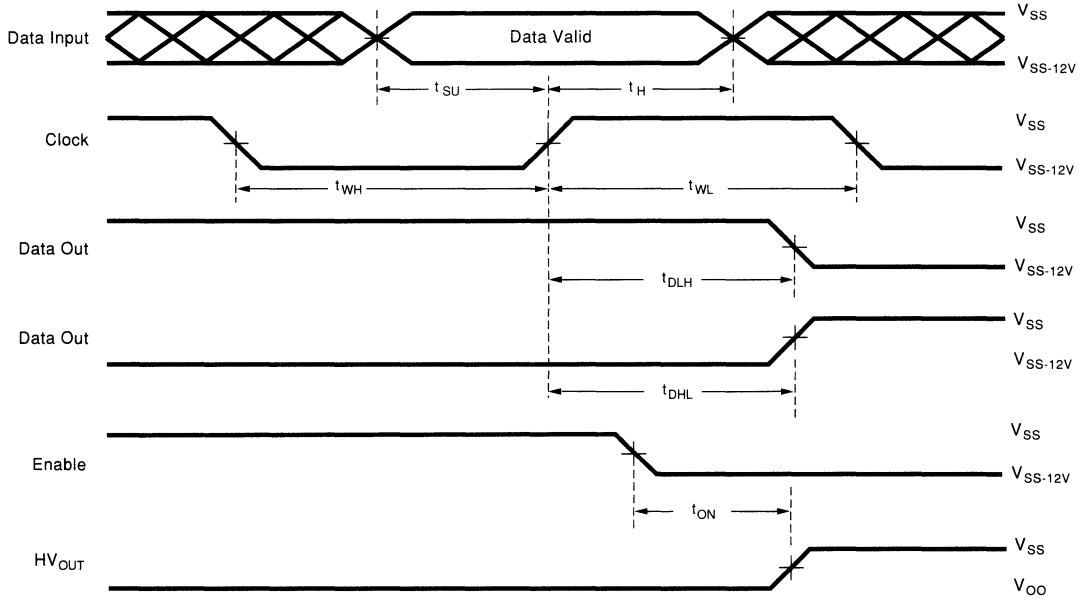
Symbol	Parameter		Min	Nom	Max	Units
V_{DD}	Logic supply voltage		-10.8	-12	-13.2	V
V_{OO}	Output off voltage		+0.3		-225	V
V_{IH}	High-level input voltage (LOGIC "1")		V_{DD} + 2V		V_{DD}	V
V_{IL}	Low-level input voltage (LOGIC "0")		0		-2.0	V
f_{CLK}	Clock frequency				4	MHz
T_A	Operating free-air temperature	Commercial	-40		+70	°C
		Military Hi-Rel (RB)	-55		+125	°C

Note 1: All voltages are referenced to V_{SS}.

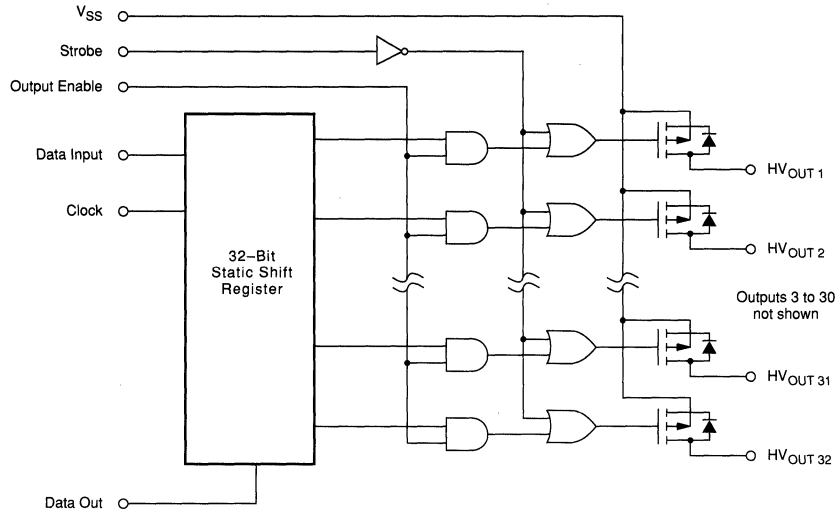
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs				Outputs		
	DI	CLK	OE	STR	Shift Reg 1 2...32	HV Outputs 1 2...32	Data Out *
All on	X	X	X	L	* *...*	All On	*
All off	X	X	L	H	* *...*	All Off	*
Load S/R	H or L	↓	L	H	H or L *...*	On or Off *...*	
Output enable	X	H or L	H	H	* *...*	On or Off *...*	*

Notes:

X = Not relevant to the output state.

* = Dependent on previous stage's state before the last CLK : High to low transition.

A logic high bit in the shift register will turn on the corresponding output when the strobe and output enable inputs are both high.

↓ = High to low transition, -12V to V_{SS}

H = High level = -12V

L = Low level = 0V

Pin Configurations

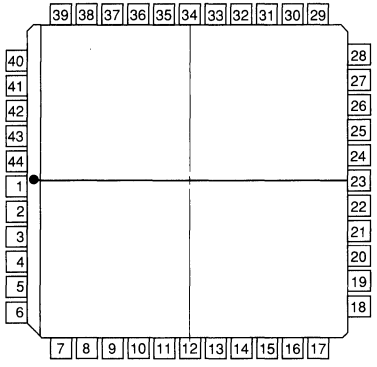
HV41
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 17	23	Output Enable
2	HVout 18	24	Clock
3	HVout 19	25	V_{SS}
4	HVout 20	26	V_{DD}
5	HVout 21	27	Strobe
6	HVout 22	28	Data In
7	HVout 23	29	HVout 1
8	HVout 24	30	HVout 2
9	HVout 25	31	HVout 3
10	HVout 26	32	HVout 4
11	HVout 27	33	HVout 5
12	HVout 28	34	HVout 6
13	HVout 29	35	HVout 7
14	HVout 30	36	HVout 8
15	HVout 31	37	HVout 9
16	HVout 32	38	HVout 10
17	N/C	39	HVout 11
18	Data Out	40	HVout 12
19	N/C	41	HVout 13
20	N/C	42	HVout 14
21	N/C	43	HVout 15
22	N/C	44	HVout 16

HV42
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 16	23	Output Enable
2	HVout 15	24	Clock
3	HVout 14	25	V_{SS}
4	HVout 13	26	V_{DD}
5	HVout 12	27	Strobe
6	HVout 11	28	Data In
7	HVout 10	29	HVout 32
8	HVout 9	30	HVout 31
9	HVout 8	31	HVout 30
10	HVout 7	32	HVout 29
11	HVout 6	33	HVout 28
12	HVout 5	34	HVout 27
13	HVout 4	35	HVout 26
14	HVout 3	36	HVout 25
15	HVout 2	37	HVout 24
16	HVout 1	38	HVout 23
17	N/C	39	HVout 22
18	Data Out	40	HVout 21
19	N/C	41	HVout 20
20	N/C	42	HVout 19
21	N/C	43	HVout 18
22	N/C	44	HVout 17

Package Outline



top view

44-pin J-lead Package

Preliminary

32-Channel Serial To Parallel Converter with P-Channel Open Drain Outputs

Ordering Information

Device	Recommended Operating V_{OO} Max	Package Options		
		44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in Waffle Pack
HV45	-300	HV4530DJ	HV4530PJ	HV4530X
	-220	HV4522DJ	HV4522PJ	HV4522X
HV46	-300	HV4630DJ	HV4630PJ	HV4630X
	-220	HV4622DJ	HV4622PJ	HV4622X

Features

- ☐ Processed with HVCMOS Technology
- ☐ Output voltages to -300V
- ☐ Source current minimum 60 mA
- ☐ Shift register speed 8 MHz
- ☐ Polarity and blanking inputs
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options
- ☐ 44-lead plastic and ceramic surface mount packages
- ☐ Hi-Rel processing available
- ☐ Can be used with the HV55 and HV56 to provide 300V push pull operation

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		+0.5V to -16V
Off state output voltage	HV4530/HV4630	+0.5V to -315V
	HV4522/ HV4622	+0.5V to -220V
Logic input levels[1]		+0.5V to V_{DD} - 0.3V
Ground currrent[2]		1.5A
Continuous total power dissipation[3]		1200mW
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes: 1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV45 and HV46 are low-voltage serial to high-voltage parallel converters with P-Channel open drain outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high-voltage current source capabilities such as driving inkjet and electrostatic print heads, plasma panels, or vacuum fluorescent displays.

These devices consist of a 32-bit shift register, 32 data latches, and control logic to perform polarity and blanking functions. Data is shifted through the shift register on the logic high-to-low transition of the clock. The HV45 shifts in the counterclockwise direction when viewed from the top of the package and the HV46 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. The data in the shift register is latched when the latch enable pin is brought to logic high and then returned to ground. If the latch enable pin is held high, the latch becomes transparent and the shift register data is directly reflected in the outputs.

For applications requiring active pull down as well as pull up, the HV45 and HV46 can be paired with the HV55 and HV56 devices, respectively. The footprint of the HV45 output pins matches the HV55 output pin footprint when the parts are mounted on opposite sides of a PC Board.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			-15	mA	f_{CLK} = 4 MHz F_{DATA} = 2 MHz
I_{DDQ}	Quiescent V_{DD} supply current			-50	µA	$V_{IN} = V_{SS}$ or V_{DD}
$I_{O(OFF)}$	Off state output current			-50	µA	All SWS parallel
I_{IH}	High-level logic input current			-1	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current			+1	µA	$V_{IL} = V_{SS}$
V_{OH}	High-level output data out		V_{DD} + 1.0V		V	I_{Dout} = -100µA
V_{OL}	Low-level output voltage	HV_{out}		-30.0	V	I_{HVout} = -60mA
		Data out		-1.0	V	I_{Dout} = -100µA
V_{OC}	HV_{out} clamp voltage			+1.5	V	I_{OL} = +60mA

AC Characteristics (V_{DD} = 12V, T_C = 25°C)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_{WH}/t_{WL}	Clock width high or low		125	ns	
t_{SU}	Data set-up time before clock rises		50	ns	
t_H	Data hold time after clock rises		20	ns	
t_{ON}	Turn ON time, HV_{out} from enable		400	ns	R_L = 10K to V_{OO} MAX
t_{DHL}	Delay time clock to data high to low		100	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high		100	ns	C_L = 15pF
t_{DLE}	Delay time clock to $\overline{LE}$ low to high	50		ns	
t_{WLE}	Width of $\overline{LE}$ pulse	50		ns	
t_{SLE}	LE set-up time before clock falls	50		ns	

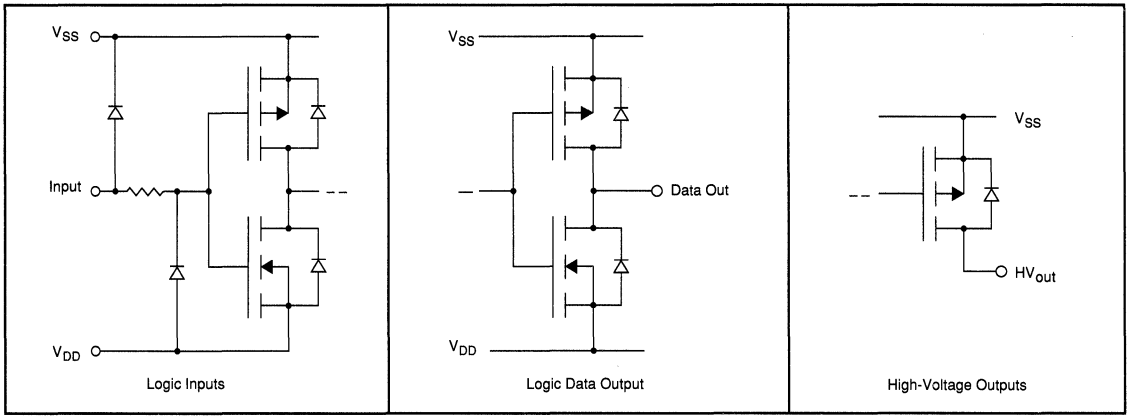
Recommended Operating Conditions

(Note 1)

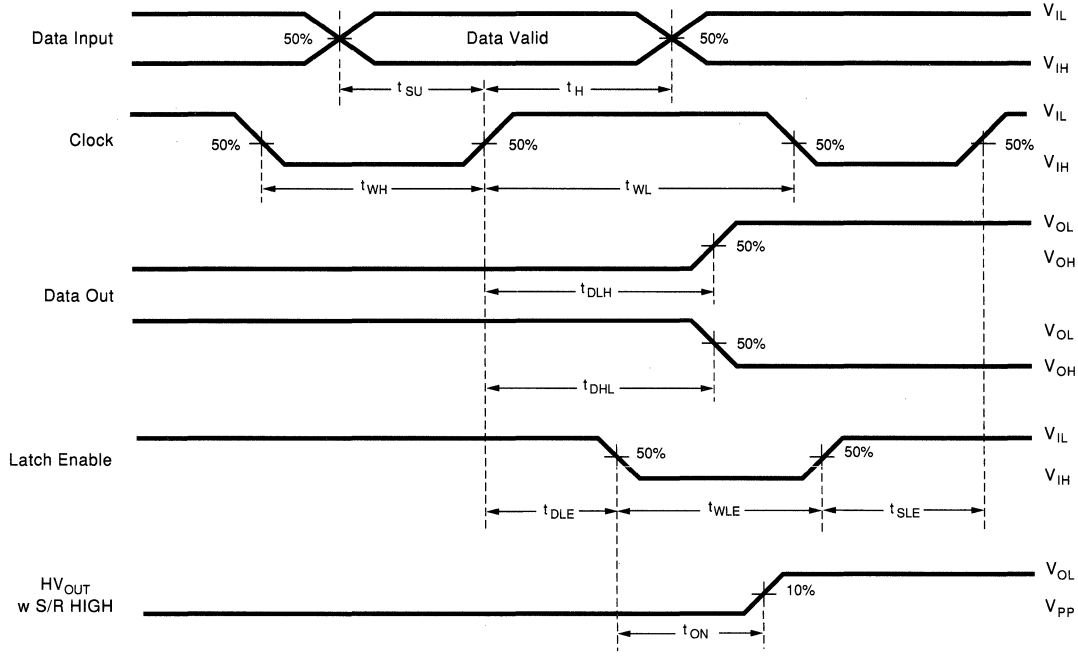
Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		-10.8	-13.2	V
V_{OO}	Output off voltage	HV4530 and HV4630	+0.3	-300	V
		HV4522 and HV4622	+0.3	-200	V
V_{IH}	High-level input voltage (LOGIC "1")		V_{DD} + 2V	V_{DD}	V
V_{IL}	Low-level input voltage (LOGIC "0")		0	-2.0	V
f_{CLK}	Clock frequency			4	MHz
T_A	Operating free-air temperature	Commercial	-40	+70	°C
		Military Hi-Rel (RB)	-55	+125	°C

Note 1: All voltages are referenced to V_{SS}.

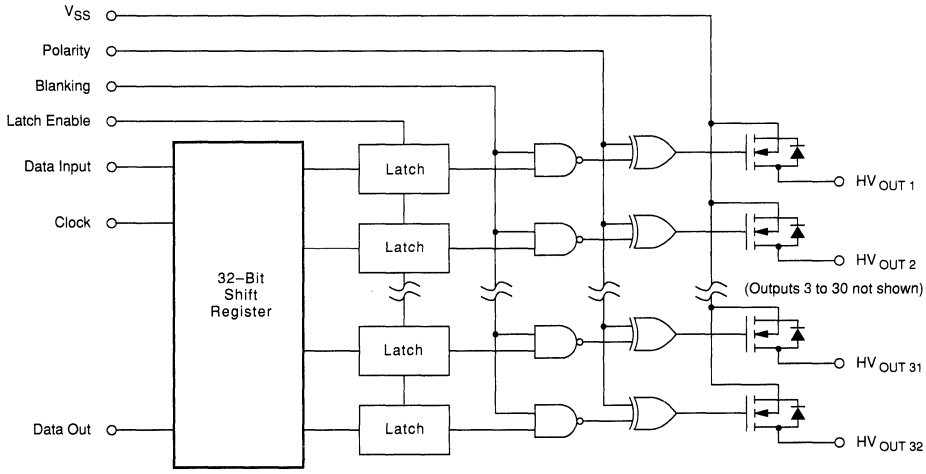
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs				
						Shift Reg		HV Outputs		Data Out
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	1	2...32	1	2...32	*
All on	X	X	X	L	L	*	*...*	H	H...H	*
All off	X	X	X	L	H	*	*...*	L	L...L	*
Invert mode	X	X	L	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Load S/R	H or L	↓	L	H	H	H or L	*...*	*	*...*	*
Load latches	X	H or L	↑	H	H	*	*...*	*	*...*	*
	X	H or L	↑	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Transparent latch mode	L	↓	H	H	H	L	*...*	L	*...*	*
	H	↓	H	H	H	H	*...*	H	*...*	*

Notes:
H = high level, L = low level, X = irrelevant, ↓ = low-to-high transition, -12V to V_{SS}.
* = dependent on previous stage's state before the last CLK ↓ or last LE high.

Pin Configurations

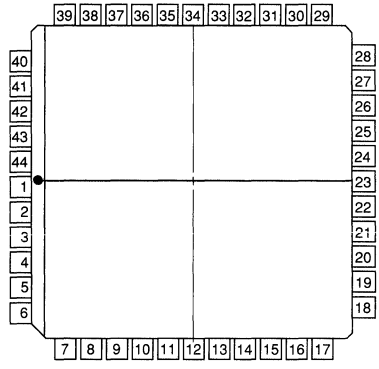
HV45
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 17	23	Clock
2	HVout 18	24	V_{SS}
3	HVout 19	25	V_{DD}
4	HVout 20	26	Latch Enable
5	HVout 21	27	Data In
6	HVout 22	28	Blanking
7	HVout 23	29	HVout 1
8	HVout 24	30	HVout 2
9	HVout 25	31	HVout 3
10	HVout 26	32	HVout 4
11	HVout 27	33	HVout 5
12	HVout 28	34	HVout 6
13	HVout 29	35	HVout 7
14	HVout 30	36	HVout 8
15	HVout 31	37	HVout 9
16	HVout 32	38	HVout 10
17	N/C	39	HVout 11
18	Data Out	40	HVout 12
19	N/C	41	HVout 13
20	N/C	42	HVout 14
21	N/C	43	HVout 15
22	Polarity	44	HVout 16

HV46
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 16	23	Clock
2	HVout 15	24	V_{SS}
3	HVout 14	25	V_{DD}
4	HVout 13	26	Latch Enable
5	HVout 12	27	Data In
6	HVout 11	28	Blanking
7	HVout 10	29	HVout 32
8	HVout 9	30	HVout 31
9	HVout 8	31	HVout 30
10	HVout 7	32	HVout 29
11	HVout 6	33	HVout 28
12	HVout 5	34	HVout 27
13	HVout 4	35	HVout 26
14	HVout 3	36	HVout 25
15	HVout 2	37	HVout 24
16	HVout 1	38	HVout 23
17	N/C	39	HVout 22
18	Data Out	40	HVout 21
19	N/C	41	HVout 20
20	N/C	42	HVout 19
21	N/C	43	HVout 18
22	Polarity	44	HVout 17

Package Outline



top view

44-pin J-lead Package

Preliminary

32-Channel AC Plasma Display Driver

Ordering Information

Device	Package Options				
	40-Pin Ceramic DIP	40-Pin Plastic DIP	44-Pin J-Lead Ceramic Chip Carrier	44-Pin J-Lead Plastic Chip Carrier	Die
HV500	HV500D	HV500P	HV500DJ	HV500PJ	HV500X

Features

- ☐ Processed with HVCMOS® Technology
- ☐ Output voltage of up to 100V
- ☐ CMOS push-pull output buffers
- ☐ Low-power level shifting
- ☐ Source/sink current minimum of 15mA
- ☐ Shift register speed 8MHz
- ☐ CMOS compatible inputs
- ☐ Output clamp diodes to V_{PP} and GND
- ☐ Direct replacement for the SN75500 and SN55500 series devices
- ☐ 44-lead plastic and ceramic surface mount packages available
- ☐ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]	-0.3V to +15V
Supply voltage, V_{PP}[1]	-0.3V to +100V
Logic input levels[1]	-0.3V to V_{DD} + 0.3V
Ground currrent[2]	1.2A
Continuous total power dissipation[3]	1850mW
Operating temperature range	-55°C to +125°C
Storage temperature range	-65°C to +150°C

Notes: 1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C case temperature, derate linearly to 70°C at 15mW/°C.

General Description

The HV500 is a monolithic low-voltage logic to high-voltage output 32-channel driver for AC plasma flat panel displays. It is manufactured using the HVCMOS process, providing the high output voltages and currents possible with DMOS structures and the low power dissipation of CMOS logic.

The HV500 is comprised of an 8-stage DMOS shift register, four groups of eight high-voltage output buffers, and logic to select which group of outputs will reflect the status of the data in the shift register and strobe functions. When the strobe input is high, all outputs are held low independent of any other logic input. When strobe is brought low, the group of outputs selected by the state of the select inputs reflects the data in the shift register, and all non-selected outputs are held low.

The high-voltage output buffers have level shifters which dissipate no DC power. These level shifters also control the rise and fall times of the outputs which have been optimized to lower system noise without compromising the current source and sink capability of the output buffers. Additionally, each output has low V_{fwd} clamp diodes to V_{PP} and GND.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} quiescent supply current			1	mA	
I_{PP}	V_{PP} quiescent supply current			1	mA	HV_{out} H or L
I_{IH}	High-level input current			1	µA	$V_{IN} = V_{DD}$
I_{IL}	Low-level input current			-1	µA	$V_{IN} = V_{SS}$
V_{OH}	High-level output voltage	HV outputs	94		V	I_{OH} = -1mA[1]
			90		V	I_{OH} = -15mA[1]
		Serial out	9		V	I_{OH} = -100µA[2]
V_{OL}	Low-level output voltage	HV outputs		2	V	I_{OL} = 1mA
				5	V	I_{OL} = 15mA
		Serial out		1	V	I_{OL} = 100µA[2]
V_{OK}	High voltage output			2.5	V	I_{OK} = 20mA[3]
	Clamp voltage			-2.5	V	I_{OK} = -20mA[3]

Notes: 1. V_{PP} = 100V
2. V_{DD} = 10.8V
3. V_{PP} = 0V

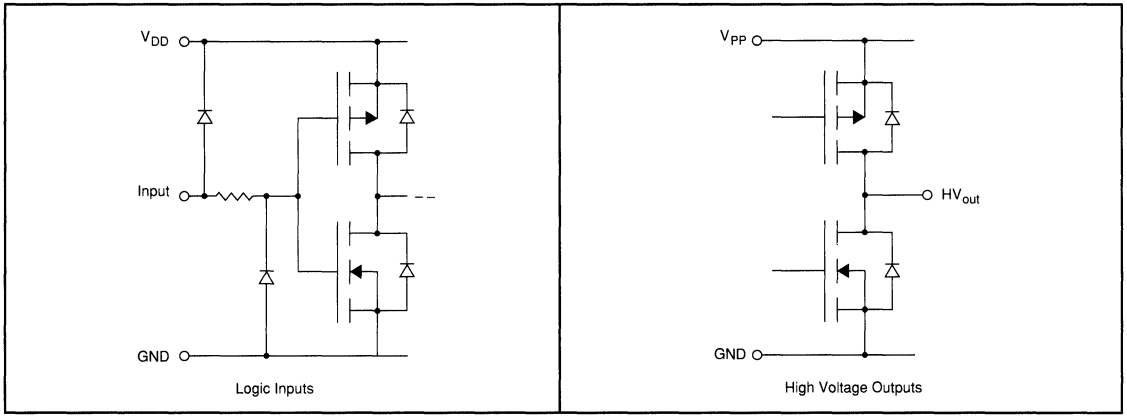
AC Characteristics (V_{DD} = 12V, V_{PP} = 100V, T_C = 25°C)

Symbol	Parameter		Min	Max	Units	Conditions
f_{MAX}	Maximum clock frequency			8	MHz	
t_W	Clock pulse width high or low		62		ns	
t_{DHL}	Delay time strobe to HV_{out} high to low		250		ns	C_L = 30pF
t_{DLH}	Delay time strobe to HV_{out} low to high		250		ns	
t_{SU}	Set-up time	Data in to clock ↑	20		ns	
		Select before strobe ↓	50		ns	
t_H	Hold time	Data after clock ↑	50		ns	
		Strobe high after clock ↑	50		ns	
		Select after strobe ↑	50		ns	
t_R	Rise time low to high HV_{out}			300	ns	C_L = 30pF
t_F	Fall time high to low HV_{out}			200	ns	C_L = 30pF

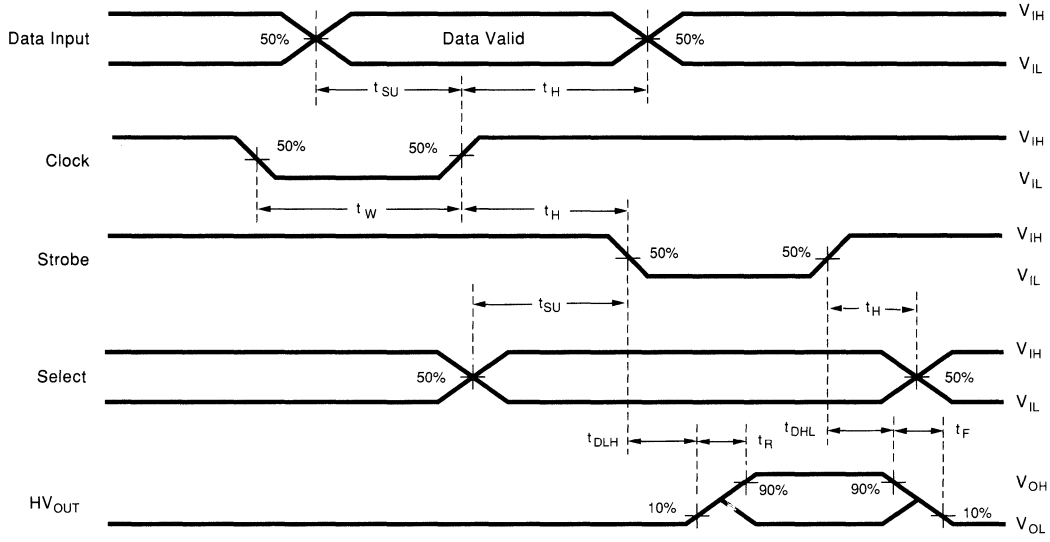
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	13.2	V
V_{PP}	High voltage supply		0	100	V
V_{IH}	High-level input voltage		0.75 V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage		GND	0.25 V_{DD}	V
T_A	Operating free-air temperature	Commercial	-40	+80	°C
		Military Hi-Rel (RB)	-55	+125	°C

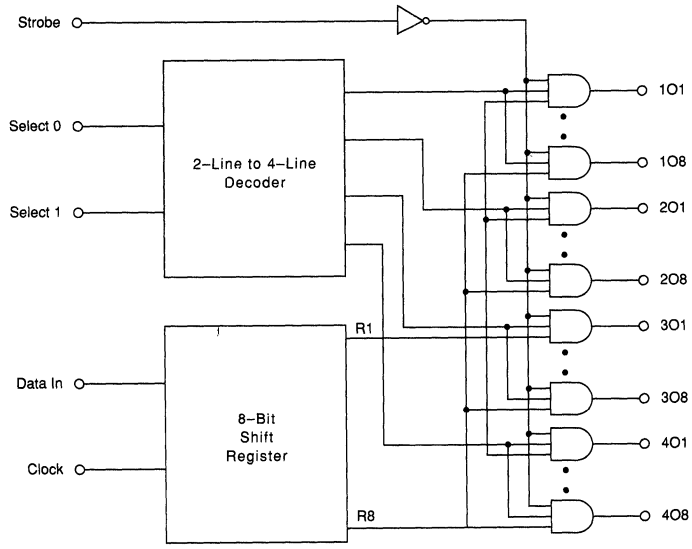
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Internal Levels			HV Outputs			
			Select			Shift Register						
	Data	Clk	S1	S0	Strb	R1	R2	R3...R8	1O1...1O8	2O1...2O8	3O1...3O8	4O1...4O8
Load	H	↑	X	X	H	L	R1n	R2n...R7n	L...L	L...L	L...L	L...L
	L	↑	X	X	H	H	R1n	R2n...R7n	L...L	L...L	L...L	L...L
Strobe	X	X	X	X	H	R1n	R2n	R3n...R8n	L...L	L...L	L...L	L...L
	X	H	L	L	L	R1n	R2n	R3n...R8n	R1...R8	L...L	L...L	L...L
	X	H	L	H	L	R1n	R2n	R3n...R8n	L...L	R1...R8	L...L	L...L
	X	H	H	L	L	R1n	R2n	R3n...R8n	L...L	L...L	R1...R8	L...L
	X	H	H	H	L	R1n	R2n	R3n...R8n	L...L	L...L	L...L	R1...R8

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
R1...R8 = levels currently at internal outputs of shift registers one through eight, respectively.
R1n...R8n = levels at shift-register outputs R1 through R8, respectively, before the most recent ↑ transition of the clock.

Pin Configurations

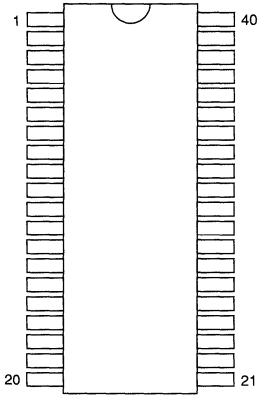
40-Pin Dual-In-Line

Pin	Function	Pin	Function
1	Select 0	21	V_{PP}
2	Data In	22	3O8
3	Clock	23	3O7
4	1O1	24	3O6
5	1O2	25	3O5
6	1O3	26	3O4
7	1O4	27	3O3
8	1O5	28	3O2
9	1O6	29	3O1
10	1O7	30	4O8
11	1O8	31	4O7
12	2O1	32	4O6
13	2O2	33	4O5
14	2O3	34	4O4
15	2O4	35	4O3
16	2O5	36	4O2
17	2O6	37	4O1
18	2O7	38	Strobe
19	2O8	39	Select 1
20	GND	40	V_{DD}

44 Pin J-Lead

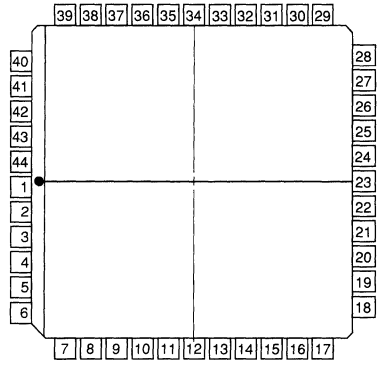
Pin	Function	Pin	Function
1	N/C	23	N/C
2	Select 0	24	V_{PP}
3	Data In	25	3O8
4	Clock	26	3O7
5	N/C	27	3O6
6	1O1	28	3O5
7	1O2	29	3O4
8	1O3	30	3O3
9	1O4	31	3O2
10	1O5	32	3O1
11	1O6	33	4O8
12	1O7	34	4O7
13	1O8	35	4O6
14	2O1	36	4O5
15	2O2	37	4O4
16	2O3	38	4O3
17	2O4	39	4O2
18	2O5	40	4O1
19	2O6	41	N/C
20	2O7	42	Strobe
21	2O8	43	Select 1
22	GND	44	V_{DD}

Package Outlines



top view

40-pin DIP



top view

44-pin J-lead Package

Preliminary

32-Channel AC Plasma Display Driver

Ordering Information

Device	Package Options				
	40-Pin Ceramic DIP	40-Pin Plastic DIP	44-Pin J-Lead Ceramic Chip Carrier	44-Pin J-Lead Plastic Chip Carrier	Die
HV501	HV501D	HV501P	HV501DJ	HV501PJ	HV501X

Features

- ☐ Processed with HVCMOS® Technology
- ☐ Output voltage of up to 100V
- ☐ DMOS push-pull output buffers
- ☐ Low-power level shifting
- ☐ Source/sink current minimum of 15mA
- ☐ Shift register speed 8MHz
- ☐ CMOS compatible inputs
- ☐ Output clamp diodes to V_{PP} and GND
- ☐ Direct replacement for the SN75501 and SN55501 series devices
- ☐ 44-lead plastic and ceramic surface mount packages available
- ☐ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]	-0.3V to +15V
Supply voltage, V_{PP}[1]	-0.3V to +100V
Logic input levels[1]	-0.3V to V_{DD} + 0.3V
Ground currrent[2]	1.5A
Continuous total power dissipation[3]	1850mW
Operating temperature range	-55°C to +125°C
Storage temperature range	-65°C to +150°C

Notes: 1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C case temperature, derate linearly to 70°C at 15mW/°C.

General Description

The HV501 is a 32-channel low-voltage serial to high-voltage parallel converter designed for use in matrix-addressable display applications. It is manufactured with the HVCMOS technology for enhanced ruggedness and performance. This device is a direct replacement for the SN75501 family of devices.

These devices are comprised of a 32-bit shift register with a serial data out, strobe and sustain control logic, and level shifters with high-voltage DMOS output buffers. When the strobe and sustain outputs are held high the outputs are held high. Data can then be clocked into the shift register without changing the state of the outputs. When the strobe input is brought low with the sustain input remaining high, the outputs will change state to reflect the status of the data in each output's corresponding shift register bit. A logic "1" in the shift register will cause the corresponding output to pull up to V_{PP}, and a logic "0" will cause the output to pull to GND. The sustain input is used to bring all the outputs low. When the sustain input is low, all outputs are low, independent of any other control input.

The high-voltage output buffers have low power level shifters which dissipate no DC power. These level shifters also control the rise and fall times of the outputs which have been optimized to lower system noise without compromising the current source and sink capability of the output buffers. Additionally, each output has low V_{fwd} clamp diodes to V_{PP} and GND.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} quiescent supply current			1	mA	
I_{PP}	V_{PP} quiescent supply current			1	mA	HV_{out} H or L
I_{IH}	High-level input current			1	µA	$V_{IN} = V_{DD}$
I_{IL}	Low-level input current			-1	µA	$V_{IN} = V_{SS}$
V_{OH}	High-level output voltage	HV outputs	94		V	I_{OH} = -1mA[1]
			90		V	I_{OH} = -15mA[1]
		Data out	9		V	I_{OH} = -100µA[2]
V_{OL}	Low-level output voltage	HV outputs		2	V	I_{OL} = 1mA
				5	V	I_{OL} = 15mA
		Data out		1	V	I_{OL} = 100µA[2]
V_{OK}	High voltage output			2.5	V	I_{OK} = 20mA[3]
	Clamp voltage			-2.5	V	I_{OK} = -20mA[3]

Notes: 1. V_{PP} = 100V
2. V_{DD} = 10.8V
3. V_{PP} = 0V

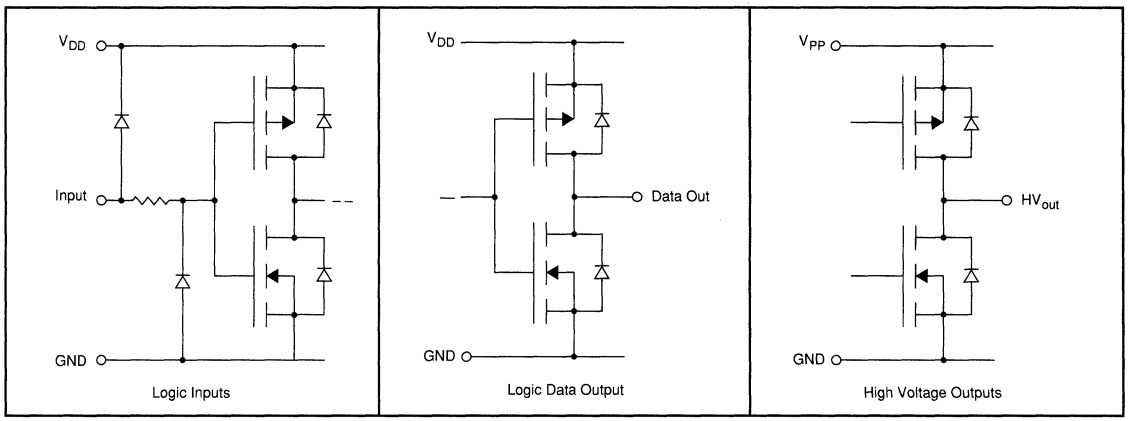
AC Characteristics (V_{DD} = 12V, V_{PP} = 80V)

Symbol	Parameter		Min	Max	Units	Conditions
f_{MAX}	Maximum clock frequency			8	MHz	
t_W	Clock pulse width high or low		62		ns	
t_{SU}	Data input set-up time before CLK		20		ns	
t_H	Data input hold time after CLK		50		ns	
t_{DHL}	Delay time High to low Level outputs	Strobe to HV_{out}		250	ns	C_L = 30pF
		Sustain to HV_{out}		250	ns	C_L = 30pF
		Serial out		147	ns	C_L = 30pF
t_{DLH}	Delay time Low to high Level outputs	Strobe to HV_{out}		450	ns	C_L = 30pF
		Sustain to HV_{out}		450	ns	C_L = 30pF
		Serial out		147	ns	C_L = 30pF
t_R	Rise time low to high HV_{out}			300	ns	C_L = 30pF
t_F	Fall time high to low HV_{out}			200	ns	C_L = 30pF

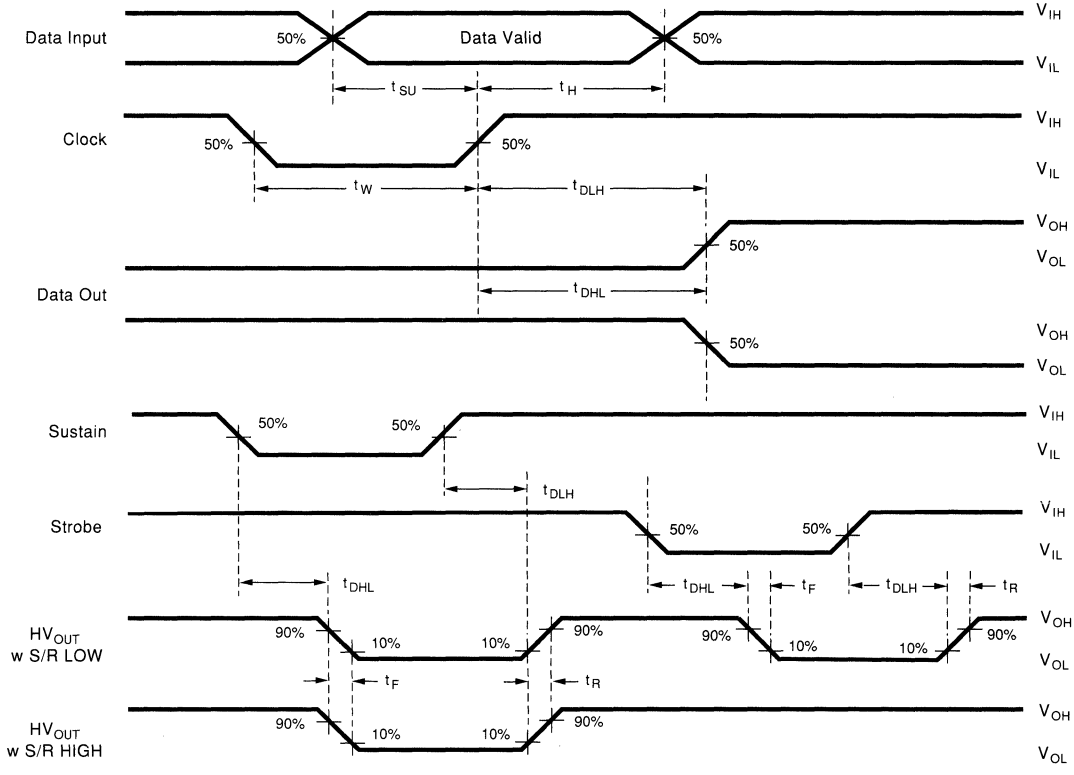
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	13.2	V
V_{PP}	High voltage supply		0	100	V
V_{IH}	High-level input voltage		0.75 V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage		GND	0.25 V_{DD}	V
T_A	Operating free-air temperature	Commercial	-40	+80	°C
		Military Hi-Rel (RB)	-55	+125	°C

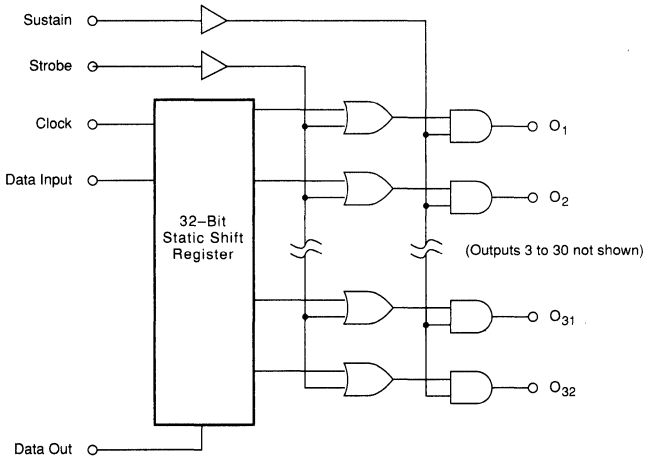
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs				Shift Register			HV Outputs		
	Data	Clock	Strobe	Sustain	R1	R2	R3...R32	1	2	3...32
Load	H	↑	H	H	H	R1n	R2n...R31n	H	H	H...H
	L	↑	H	H	L	R1n	R2n...R31n	H	H	H...H
Strobe	X	X	H	H	R1n	R2n	R3n...R32n	H	H	H...H
	X	H	L	H	R1n	R2n	R3n...R32n	R1	R2	R3...R32
Sustain	X	X	X	L	R1n	R2n	R3n...R32n	L	L	L...L

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
R1...R32 = levels currently at internal outputs of shift registers one through 32, respectively.
R1n...R32n = levels at shift-register outputs R1 through R32, respectively, before the most recent ↑ transition of the clock input.

Pin Configurations

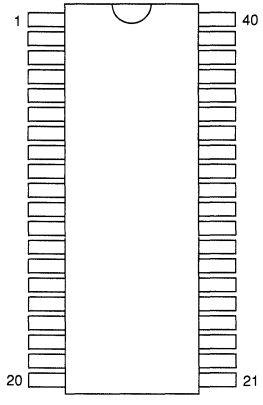
40-Pin Dual-In-Line

Pin	Function	Pin	Function
1	Clock	21	V_{PP}
2	Sustain	22	HVout 17
3	Strobe	23	HVout 18
4	HVout 1	24	HVout 19
5	HVout 2	25	HVout 20
6	HVout 3	26	HVout 21
7	HVout 4	27	HVout 22
8	HVout 5	28	HVout 23
9	HVout 6	29	HVout 24
10	HVout 7	30	HVout 25
11	HVout 8	31	HVout 26
12	HVout 9	32	HVout 27
13	HVout 10	33	HVout 28
14	HVout 11	34	HVout 29
15	HVout 12	35	HVout 30
16	HVout 13	36	HVout 31
17	HVout 14	37	HVout 32
18	HVout 15	38	Data Out
19	HVout 16	39	Data In
20	GND	40	V_{DD}

44 Pin J-Lead Package

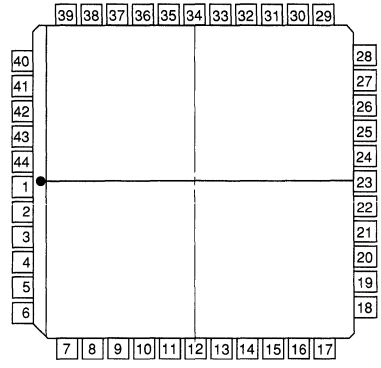
Pin	Function	Pin	Function
1	N/C	23	N/C
2	Clock	24	V_{PP}
3	Sustain	25	HVout 17
4	Strobe	26	HVout 18
5	N/C	27	HVout 19
6	HVout 1	28	HVout 20
7	HVout 2	29	HVout 21
8	HVout 3	30	HVout 22
9	HVout 4	31	HVout 23
10	HVout 5	32	HVout 24
11	HVout 6	33	HVout 25
12	HVout 7	34	HVout 26
13	HVout 8	35	HVout 27
14	HVout 9	36	HVout 28
15	HVout 10	37	HVout 29
16	HVout 11	38	HVout 30
17	HVout 12	39	HVout 31
18	HVout 13	40	HVout 32
19	HVout 14	41	N/C
20	HVout 15	42	Data Out
21	HVout 16	43	Data In
22	GND	44	V_{DD}

Package Outlines



top view

40-pin DIP



top view

44-pin J-lead Package

32-Channel Serial To Parallel Converter With Open Drain Outputs

Ordering Information

Device	Package Options		
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack
HV51	HV5122DJ	HV5122PJ	HV5122X
HV52	HV5222DJ	HV5222PJ	HV5222X

Features

- ☐ Processed with HVCMOS® technology
- ☐ Output voltages to 225V using a ramped supply voltage
- ☐ Sink current minimum 100mA
- ☐ Shift register speed 8MHz
- ☐ Strobe and enable inputs
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options
- ☐ Replacements for SN75551 (HV5122) and SN75552 (HV5222) Row Drivers
- ☐ 44-lead ceramic surface mount package
- ☐ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]	-0.5V to +18V
Output voltage, V_{PP}[2]	-0.5V to +250V
Logic input levels	-0.5V to V_{DD} + 0.5V
Ground currrent[3]	1.5A
Continuous total power dissipation[4]	1500mW
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C

Notes: 1. All voltages are referenced to V_{SS}.
2. These devices have been designed to be used in applications which either switch the V_{PP} supply to ground before changing the state of the high voltage outputs or limit the current through each output.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV51 and HV52 are low voltage serial to high voltage parallel converters wtih open drain outputs. These devices have been designed for use as drivers for AC electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register and control logic to perform the Output Enable and All-ON functions. Data is shifted through the shift register on the high to low transition of the clock. The HV51 shifts in the counterclockwise direction when viewed from the top of the package and the HV52 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the OE (Output Enable) or the STR (Strobe) inputs.

The HV51 and HV52 have been designed to be used in systems which either switch off the high voltage supply before changing the state of the high voltage outputs or which limit the current through each output.

These devices are pin for pin replacements for the SN75551 and SN75552 devices. In addition, Supertex HVCMOS technology provides significantly higher speed and higher sink current capability in the HV51 and HV52 devices.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} supply current				15	mA	f_{CLK} = 8MHz F_{DATA} = 4MHz
I_{DDQ}	Quiescent V_{DD} supply current				0.5	mA	All V_{IN} = 0V
$I_{O(OFF)}$	Off state output current				10	µA	All outputs high All SWS parallel
I_{IH}	High-level logic input current				1	µA	V_{IH} = 12V
I_{IL}	Low-level logic input current				-1	µA	V_{IL} = 0V
V_{OH}	High-level output data out		V_{DD} - 1.0V			V	I_{Dout} = -100µA
V_{OL}	Low-level output voltage	HV_{OUT}			15.0	V	I_{HVout} = +100mA
		Data out			1.0	V	I_{Dout} = +100µA
V_{OC}	HV_{OUT} Clamp Voltage				-1.5	V	I_{OL} = -100mA

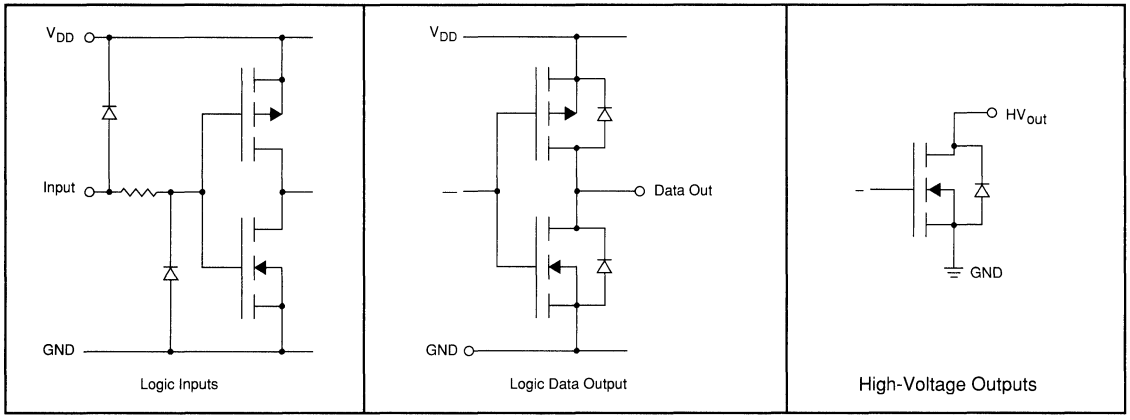
AC Characteristics (V_{DD} = 12V, T_C = 25°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock frequency			8	MHz	
t_W	Clock width high or low	62			ns	
t_{SU}	Data set-up time before clock falls	25			ns	
t_H	Data hold time after clock falls	10			ns	
t_{ON}	Turn ON time, HV_{OUT} from enable			500	ns	R_L = 2KΩ to 200V
t_{DHL}	Delay time clock to data high to low			100	ns	
t_{DLH}	Delay time clock to data low to high			100	ns	

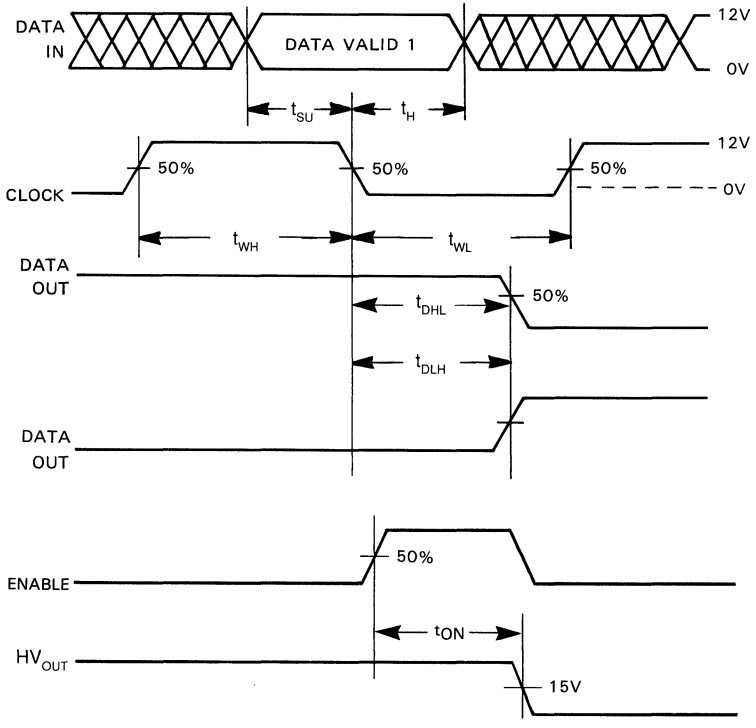
Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{DD}	Logic supply voltage		10.8	12	15	V
V_{PP}	High voltage supply		-0.3		225	V
V_{IH}	High-level input voltage		V_{DD} - 2V		V_{DD}	V
V_{IL}	Low-level input voltage		0		2.0	V
f_{CLK}	Clock frequency				8	MHz
T_A	Operating free-air temperature	Commercial	0		+70	°C
		Military Hi-Rel (RB)	-55		+125	°C

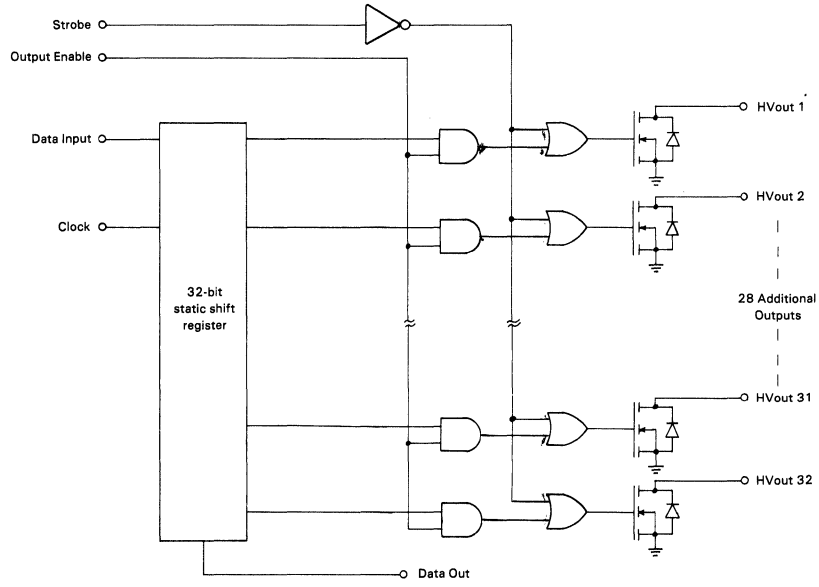
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs				Outputs		
	DI	CLK	OE	STR	Shift Reg 1 2...32	HV Outputs 1 2...32	Data Out *
All on	X	X	X	L	* *...*	L L...L	*
All off	X	X	L	H	* *...*	H H...H	*
Load S/R	H or L	↓	L	H	H or L *...*	H H...H	
Output enable	X	H or L	H	H	H or L *...*	L or H *...*	*

Notes:
X = Don't care
* = Dependent on previous stage's state before the last CLK : High to low transition.
↓ = High to low transition
H = High level
L = Low level

Pin Configurations

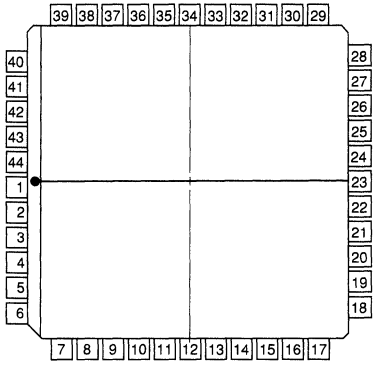
HV51
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 16	23	Output Enable
2	HVout 17	24	Clock
3	HVout 18	25	GND
4	HVout 19	26	V_{DD}
5	HVout 20	27	Strobe
6	HVout 21	28	Data In
7	HVout 22	29	N/C
8	HVout 23	30	HVout 1
9	HVout 24	31	HVout 2
10	HVout 25	32	HVout 3
11	HVout 26	33	HVout 4
12	HVout 27	34	HVout 5
13	HVout 28	35	HVout 6
14	HVout 29	36	HVout 7
15	HVout 30	37	HVout 8
16	HVout 31	38	HVout 9
17	HVout 32	39	HVout 10
18	Data Out	40	HVout 11
19	N/C	41	HVout 12
20	N/C	42	HVout 13
21	N/C	43	HVout 14
22	N/C	44	HVout 15

HV52
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 17	23	Output Enable
2	HVout 16	24	Clock
3	HVout 15	25	GND
4	HVout 14	26	V_{DD}
5	HVout 13	27	Strobe
6	HVout 12	28	Data In
7	HVout 11	29	N/C
8	HVout 10	30	HVout 32
9	HVout 9	31	HVout 31
10	HVout 8	32	HVout 30
11	HVout 7	33	HVout 29
12	HVout 6	34	HVout 28
13	HVout 5	35	HVout 27
14	HVout 4	36	HVout 26
15	HVout 3	37	HVout 25
16	HVout 2	38	HVout 24
17	HVout 1	39	HVout 23
18	Data Out	40	HVout 22
19	N/C	41	HVout 21
20	N/C	42	HVout 20
21	N/C	43	HVout 19
22	N/C	44	HVout 18

Package Outline



top view

44-pin J-lead Package

32-Channel Serial To Parallel Converter With High Voltage Push-Pull Outputs

Ordering Information

Device	Recommended Operating V_{PP} max	Package Options		
		44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack
HV53	60V	HV5306DJ	HV5306PJ	HV5306X
	80V	HV5308DJ	HV5308PJ	HV5308X
HV54	60V	HV5406DJ	HV5406PJ	HV5406X
	80V	HV5408DJ	HV5408PJ	HV5408X

Features

- ☐ Processed with HVCMOS® technology
- ☐ Output voltages up to 80V using a ramped supply voltage
- ☐ Low power level shifting
- ☐ Source/sink current minimum 20mA
- ☐ Shift register speed 8MHz
- ☐ Latched data outputs
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options
- ☐ Diode to VPP allows efficient power recovery
- ☐ Replacements for SN75553 (HV5306), SN75554 (HV5406), SN75555 (HV5308) AND SN75556 (HV5408) Column Drivers
- ☐ 44-lead ceramic surface mount package
- ☐ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]	-0.5V to +18V
Supply voltage, V_{PP}	-0.5V to +250V
Logic input levels[1]	-0.5 to V_{DD} + 0.5V
Ground currrent[2]	1.5A
Continuous total power dissipation[3]	1500mW
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C

Notes: 1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV53 and HV54 are low voltage serial to high voltage parallel converters wtih push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register, 32 latches, and control logic to enable outputs. HVout1 is connected to the first stage of the shift register through the Output Enable logic. Data is shifted through the shift register on the high to low transition of the clock. The HV54 shifts in the counterclockwise direction when viewed from the top of the package and the HV53 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (32). Operation of the shift register is not affected by the LE (latch enable) or the OE (output enable) inputs. Transfer of data from the shift register to the latch occurs when the LE input is high. The data in the latch is retained when LE is low.

These devices are pin for pin replacements for the SN75553 and SN75554, SN75555 and SN75556. In addition, Supertex HVCMOS technology provides significantly iroved power consumption, speed, and source/sink current capability in the HV53 and HV54 devices.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter			Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} supply current					15	mA	f_{CLK} = 8MHz V_{DD} = V_{DD} max
I_{PP}	High voltage supply current					0.5	mA	Outputs High
						0.5	mA	Outputs Low
I_{DDQ}	Quiescent V_{DD} supply current					0.5	mA	All V_{IN} = 0V
V_{OL}	Low-level output	HV_{OUT}	Commercial	52			V	I_O = -20mA
			Military	52			V	I_O = -15mA
			Data out	10.5			V	I_O = -100µA
V_{OH}	High-level output	HV_{OUT}	Commercial			8	V	I_O = 20mA
			Military			8	V	I_O = 15mA
			Data out			1	V	I_O =100µA
I_{IH}	High-level logic input current					1	µA	V_{IH} = V_{DD}
I_{IL}	Low-level logic input current					-1	µA	V_I = 0V

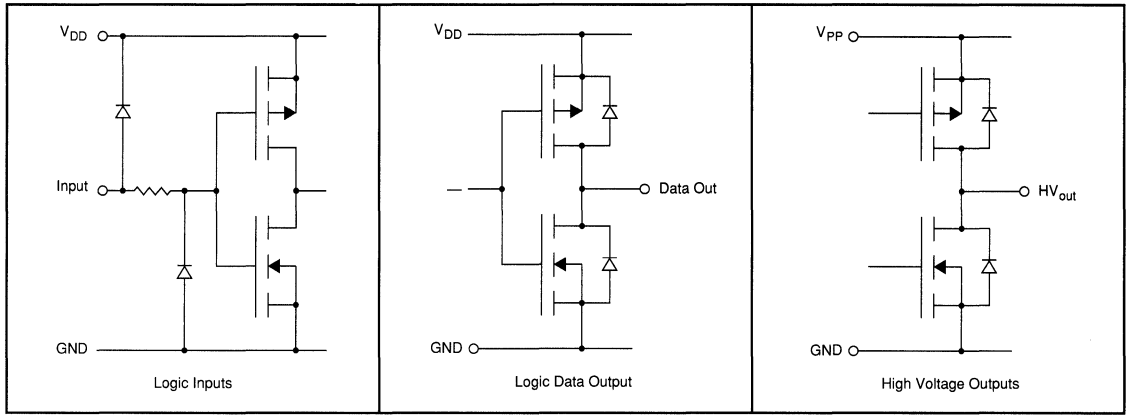
AC Characteristics (@ V_{DD} = 12V, V_{PP} = 60V, T_C = 25°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{DHL}	Delay time, high to low data out from clock			110	ns	C_L = 10pF
t_{DLH}	Delay time, low to high data out from clock			110	ns	C_L = 10pF
t_{SU}	Data set-up time before clock rises	25			ns	C_L = 10pF
t_H	Data hold time after clock rises	10			ns	C_L = 10pF

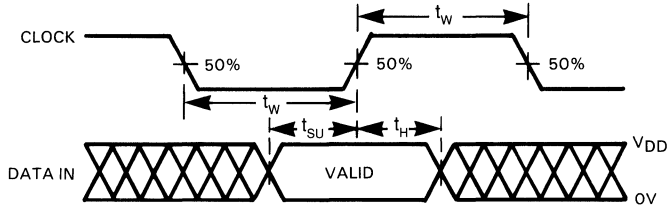
Recommended Operating Conditions

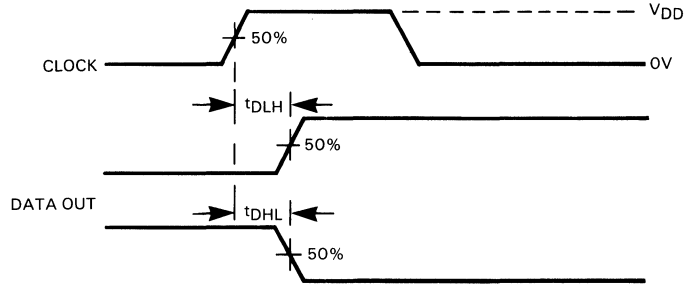
Symbol	Parameter		Min	Typ	Max	Units
V_{DD}	Logic supply voltage		10.8	12	13.2	V
V_{PP}	High voltage supply	HV5306 and HV5406	-0.3		60	V
		HV5308 and HV5408	-0.3		80	V
V_{IH}	High-level input voltage		V_{DD} - 2V		V_{DD}	V
V_{IL}	Low-level input voltage		0		2.0	V
f_{CLK}	Clock frequency		0		8.0	MHz
T_A	Operating free-air temperature	Commercial	0		+70	°C
		Military Hi-Rel (RB)	-55		+125	°C

Input and Output Equivalent Circuits

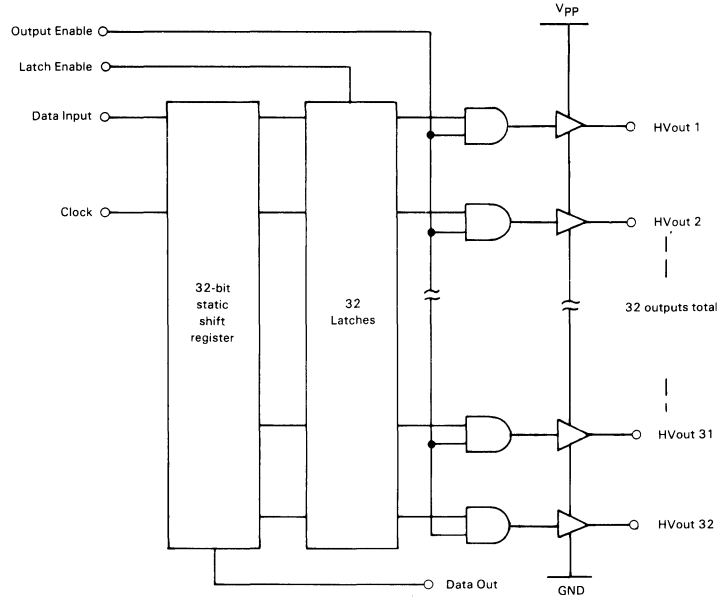


Switching Waveforms





Functional Block Diagram



Function Table

Function	Inputs				Outputs						
	DI	CLK	$\overline{LE}$	OE	Shift Reg		Latch		HV Outputs		Data Out
					1	2...32	1	2...32	1	2...32	
All off	X	X	X	L	*	*...*	*	*...*	L	L...L	2
Load S/R	H or L	↑	X	X	H or L	*...*	*	*...*	*	*...*	2
Load latches	X	H or L	↑	X	*	*...*	New Data		*	*...*	2
Latch mode	X	X	L	H	*	*...*	Stored Data		Stored Data[1]		2

X = Don't care.
* = Dependent on previous stage's state before the last CLK : or last LE high and status of OE.
↑ = low-to-high transition.
H = High level.
L = Low level.
1 = When output enable is high.
2 = Data out takes the same state as the 32nd shift register stage.

Pin Configurations

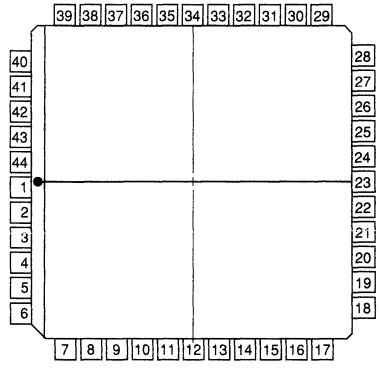
HV53
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 17	23	GND
2	HVout 16	24	V_{PP}
3	HVout 15	25	V_{DD}
4	HVout 14	26	Latch Enable
5	HVout 13	27	Data In
6	HVout 12	28	Output Enable
7	HVout 11	29	N/C
8	HVout 10	30	HVout 32
9	HVout 9	31	HVout 31
10	HVout 8	32	HVout 30
11	HVout 7	33	HVout 29
12	HVout 6	34	HVout 28
13	HVout 5	35	HVout 27
14	HVout 4	36	HVout 26
15	HVout 3	37	HVout 25
16	HVout 2	38	HVout 24
17	HVout 1	39	HVout 23
18	Data Out	40	HVout 22
19	N/C	41	HVout 21
20	N/C	42	HVout 20
21	N/C	43	HVout 19
22	Clock	44	HVout 18

HV54
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 16	23	GND
2	HVout 17	24	V_{PP}
3	HVout 18	25	V_{DD}
4	HVout 19	26	Latch Enable
5	HVout 20	27	Data In
6	HVout 21	28	Output Enable
7	HVout 22	29	N/C
8	HVout 23	30	HVout 1
9	HVout 24	31	HVout 2
10	HVout 25	32	HVout 3
11	HVout 26	33	HVout 4
12	HVout 27	34	HVout 5
13	HVout 28	35	HVout 6
14	HVout 29	36	HVout 7
15	HVout 30	37	HVout 8
16	HVout 31	38	HVout 9
17	HVout 32	39	HVout 10
18	Data Out	40	HVout 11
19	N/C	41	HVout 12
20	N/C	42	HVout 13
21	N/C	43	HVout 14
22	Clock	44	HVout 15

Package Outline



top view

44-pin J-lead Package

Preliminary

32-Channel Serial To Parallel Converter With Open Drain Outputs

Ordering Information

Device	Recommended Operating V_{PP} max	Package Options		
		44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack
HV55	300V	HV5530DJ	HV5530PJ	HV5530X
	220V	HV5522DJ	HV5522PJ	HV5522X
HV56	300V	HV5630DJ	HV5630PJ	HV5630X
	220V	HV5622DJ	HV5622PJ	HV5622X

Features

- ☐ Processed with HVCMOS® technology
- ☐ Output voltages up to 300V using a ramped supply voltage
- ☐ Sink current minimum 100mA
- ☐ Shift register speed 8MHz
- ☐ Polarity and Blanking inputs
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options
- ☐ Diode to VPP allows efficient power recovery
- ☐ 44-lead ceramic surface mount package
- ☐ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.5V to +18V
Output voltage, V_{PP}[1]	HV5530/HV5630	-0.5V to +315V
	HV5522/HV5622	-0.5V to +220V
Logic input levels[1]		-0.5V to V_{DD} + 0.5V
Ground currrent[2]		1.5A
Continuous total power dissipation[3]		1500mW
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes: 1. All voltages are referenced to V_{SS}.
2 Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV55 and HV56 are low-voltage serial to high-voltage parallel converters wtih open drain outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the shift register on the high to low transition of the clock. The HV55 shifts in the counterclockwise direction when viewed from the top of the package, and the HV56 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			15	mA	f_{CLK} = 8MHz F_{DATA} = 4MHz
I_{DDQ}	Quiescent V_{DD} supply current			0.05	mA	V_{IN} = 0V
$I_{O(OFF)}$	Off state output current			10	µA	All outputs high All SWS parallel
I_{IH}	High-level logic input current			1	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current			-1	µA	V_{IL} = 0V
V_{OH}	High-level output data out		V_{DD} - 1.0V		V	I_{Dout} = -100µA
V_{OL}	Low-level output voltage	HV_{OUT}	15.0		V	I_{HVout} = +100mA
		Data out		1.0	V	I_{Dout} = +100µA
V_{OC}	HV_{OUT} clamp voltage			-1.5	V	I_{OL} = -100mA

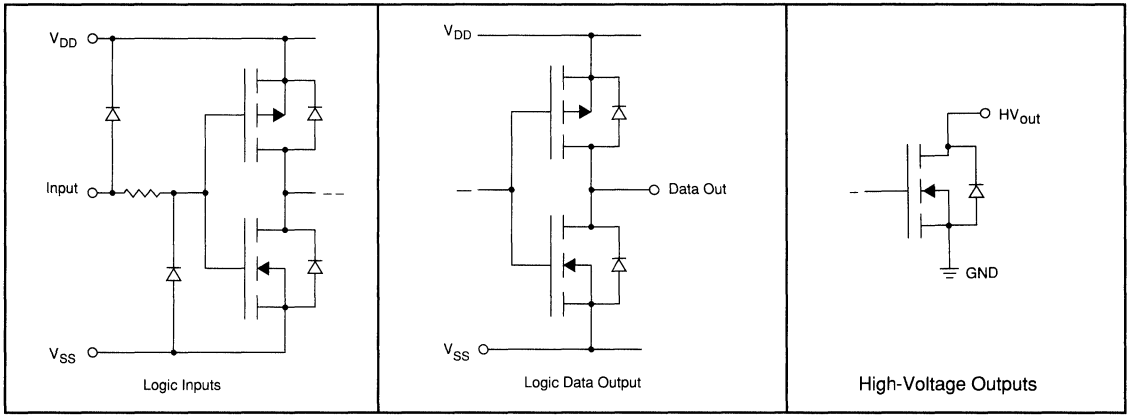
AC Characteristics (V_{DD} = 12V, T_C = 25°C)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_W	Clock width high or low	62		ns	
t_{SU}	Data set-up time before clock falls	25		ns	
t_H	Data hold time after clock falls	10		ns	
t_{ON}	Turn on time, HV_{OUT} from enable		500	ns	R_L = 2KΩ to V_{PP} MAX
t_{DHL}	Delay time clock to data high to low		100	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high		100	ns	C_L = 15pF
t_{DLE}	Delay time clock to LE low to high	50		ns	
t_{WLE}	Width of LE pulse	50		ns	
t_{SLE}	LE set-up time before clock falls	50		ns	

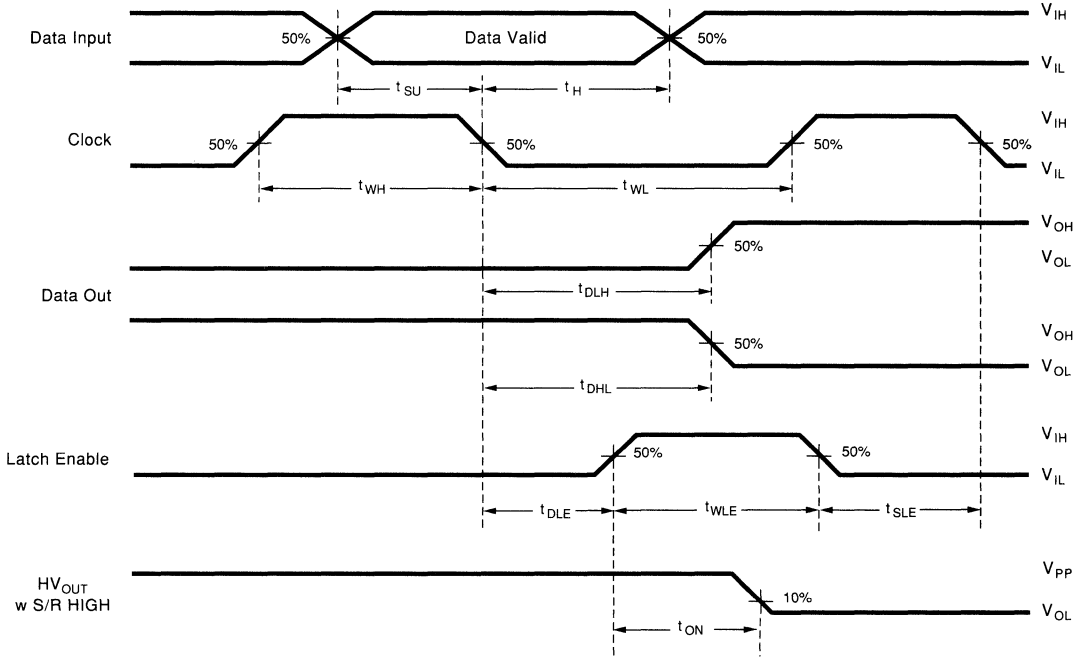
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	15	V
V_{PP}	High voltage supply	HV5530 and HV5630	-0.3	+300	V
		HV5522 and HV5622	-0.3	+200	V
V_{IH}	High-level input voltage		V_{DD} - 2V	V_{DD}	V
V_{IL}	Low-level input voltage		0	2.0	V
f_{CLK}	Clock frequency			8	MHz
T_A	Operating free-air temperature	Commercial	0	+70	°C
		Military Hi-Rel (RB)	-55	+125	°C

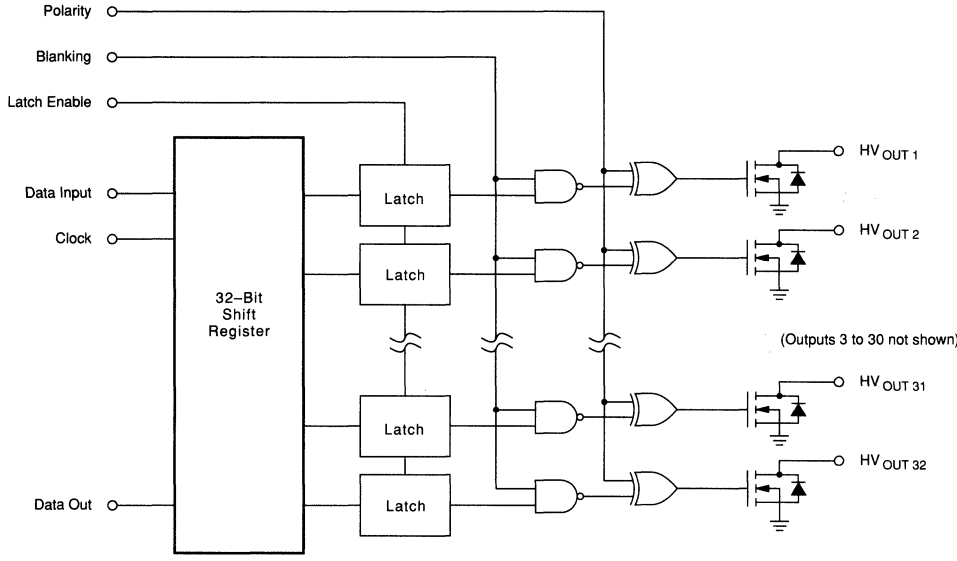
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs				
						Shift Reg		HV Outputs		Data Out
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	1	2...32	1	2...32	*
All on	X	X	X	L	L	*	*...*	On	On...On	*
All off	X	X	X	L	H	*	*...*	Off	Off...Off	*
Invert mode	X	X	L	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Load S/R	H or L	↓	L	H	H	H or L	*...*	*	*...*	*
Load Latches	X	H or L	↑	H	H	*	*...*	*	*...*	*
	X	H or L	↑	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Transparent Latch mode	L	↓	H	H	H	L	*...*	Off	*...*	*
	H	↓	H	H	H	H	*...*	On	*...*	*

Notes:
H = high level, L = low level, X = irrelevant, ↓ = low-to-high transition.
* = dependent on previous stage's state before the last CLK ↓ or last LE high.

Pin Configurations

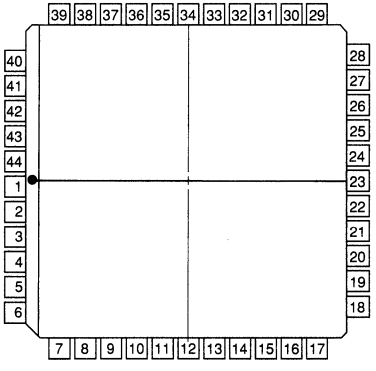
HV55
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 16	23	Clock
2	HVout 17	24	V_{SS}
3	HVout 18	25	V_{DD}
4	HVout 19	26	Latch Enable
5	HVout 20	27	Data In
6	HVout 21	28	Blanking
7	HVout 22	29	N/C
8	HVout 23	30	HVout 1
9	HVout 24	31	HVout 2
10	HVout 25	32	HVout 3
11	HVout 26	33	HVout 4
12	HVout 27	34	HVout 5
13	HVout 28	35	HVout 6
14	HVout 29	36	HVout 7
15	HVout 30	37	HVout 8
16	HVout 31	38	HVout 9
17	HVout 32	39	HVout 10
18	Data Out	40	HVout 11
19	N/C	41	HVout 12
20	N/C	42	HVout 13
21	N/C	43	HVout 14
22	Polarity	44	HVout 15

HV56
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 17	23	Clock
2	HVout 16	24	V_{SS}
3	HVout 15	25	V_{DD}
4	HVout 14	26	Latch Enable
5	HVout 13	27	Data In
6	HVout 12	28	Blanking
7	HVout 11	29	N/C
8	HVout 10	30	HVout 32
9	HVout 9	31	HVout 31
10	HVout 8	32	HVout 30
11	HVout 7	33	HVout 29
12	HVout 6	34	HVout 28
13	HVout 5	35	HVout 27
14	HVout 4	36	HVout 26
15	HVout 3	37	HVout 25
16	HVout 2	38	HVout 24
17	HVout 1	39	HVout 23
18	Data Out	40	HVout 22
19	N/C	41	HVout 21
20	N/C	42	HVout 20
21	N/C	43	HVout 19
22	Polarity	44	HVout 18

Package Outline



top view

44-pin J-lead Package

32-Channel Serial To Parallel Converter With Push-Pull Outputs

Ordering Information

Device	Package Options		
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack
HV57	HV5708DJ	HV5708PJ	HV5708X
HV58	HV5808DJ	HV5808PJ	HV5808X

Features

- ☐ Processed with HVCMOS® technology
- ☐ Output voltages up to 80V
- ☐ Low power level shifting
- ☐ Source/sink current minimum 20mA
- ☐ Shift register speed 8MHz
- ☐ Latched data outputs
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options
- ☐ Diode to V_{PP} allows efficient power recovery
- ☐ 44-lead plastic and ceramic surface mount packages
- ☐ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]	-0.5V to +18V
Output voltage, V_{PP}	-0.5V to +80V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground currrent[2]	1.5A
Continuous total power dissipation[3]	1500mW
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C

Notes: 1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV57 and HV58 are low-voltage serial to high-voltage parallel converters wtih push-pull outputs.These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high-voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays.

These devices consist of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. HVout1 is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the logic high to low transition of the clock. The HV57 shifts data in the rclockwise direction when viewed from the top of the package and the HV58 shifts in the counterclockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HVout32). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			15	mA	$V_{DD} = V_{DD}$ max f_{CLK} = 8MHz
I_{PP}	High voltage supply current			0.5	mA	Outputs high
				0.5	mA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current			0.5	mA	All $V_{IN} = V_{SS}$ or V_{DD}
V_{OH}	High-level output	Q	52		V	I_O= -20mA
		Data out	10.5		V	I_O= -100µA
V_{OL}	Low-level output	Q		8	V	I_O= 20mA
		Data out		1	V	I_O= 100µA
I_{IH}	High-level logic input current			1	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current			-1	µA	V_{IL} = 0V

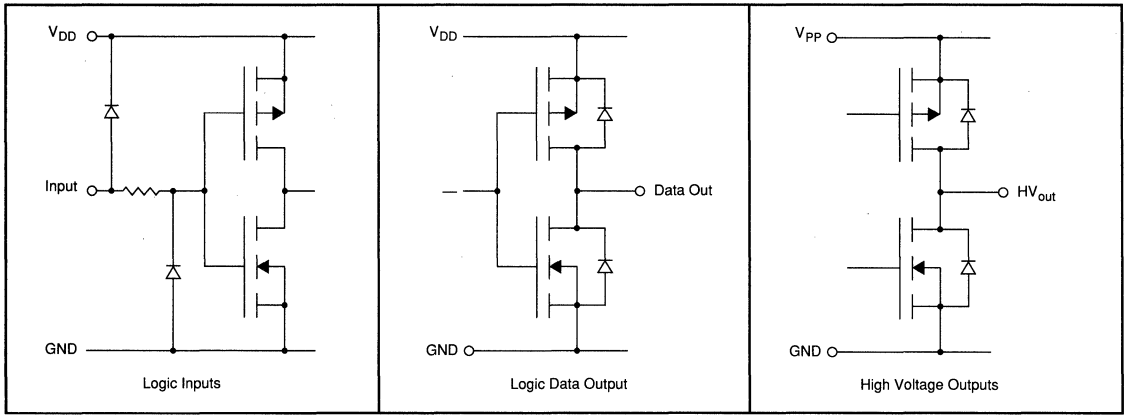
AC Characteristics (V_{DD} = 12V, T_C = 25°C)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_W	Clock width high or low	62		ns	
t_{SU}	Data set-up time before clock rises	25		ns	
t_H	Data hold time after clock rises	10		ns	
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}		500	ns	
t_{DHL}	Delay time clock to data high to low		100	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high		100	ns	C_L = 15pF
t_{DLE}	Delay time clock to $\overline{LE}$ low to high	50		ns	
t_{WLE}	Width of $\overline{LE}$ pulse	50		ns	
t_{SLE}	$\overline{LE}$ set-up time before clock rises	50		ns	

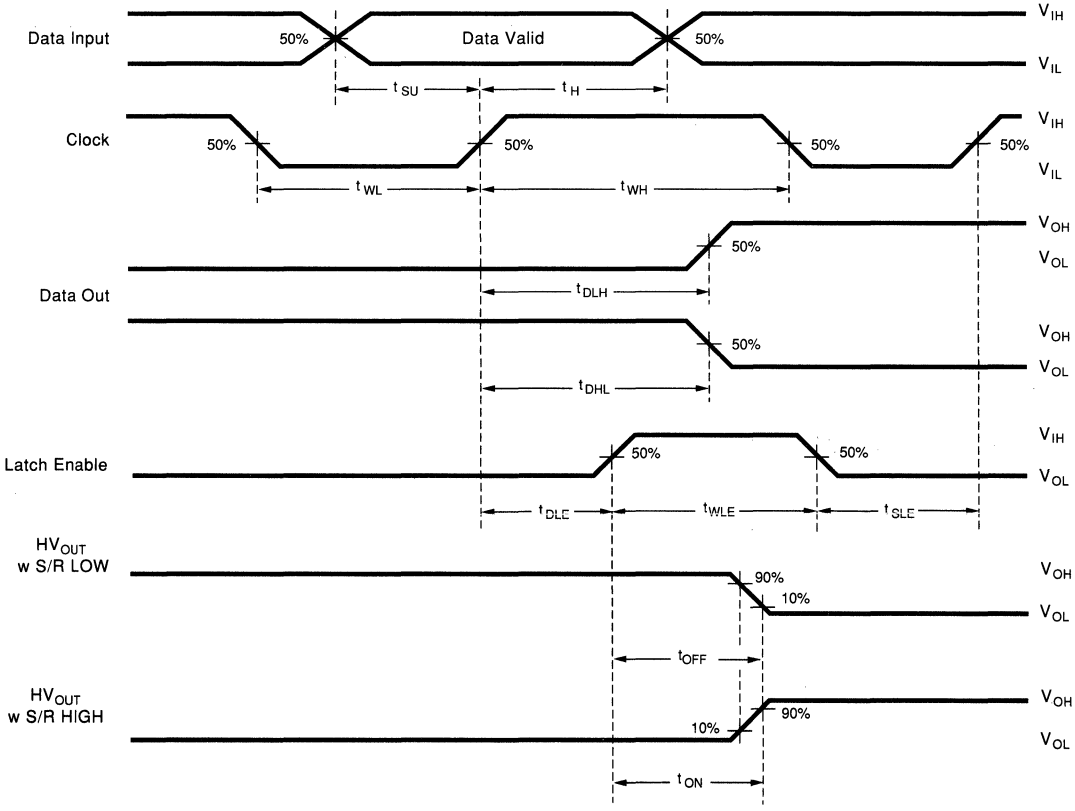
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	15	V
V_{PP}	Output off voltage		-0.3	75	V
V_{IH}	High-level input voltage		V_{DD} - 2V	V_{DD}	V
V_{IL}	Low-level input voltage		0	2.0	V
f_{CLK}	Clock frequency			8	MHz
T_A	Operating free-air temperature	Commercial	0	+70	°C
		Military Hi-Rel (RB)	-55	+125	°C

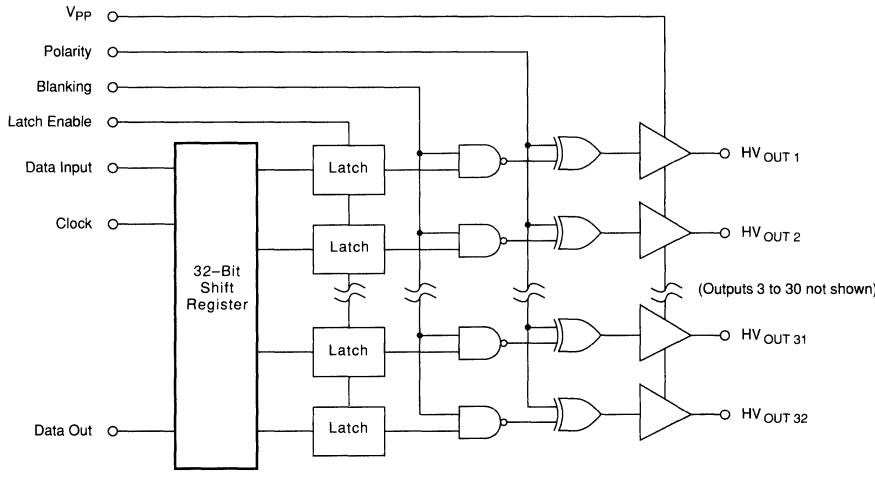
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs				
						Shift Reg		HV Outputs		Data Out
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	1	2...32	1	2...32	*
All on	X	X	X	L	L	*	*...*	H	H...H	*
All off	X	X	X	L	H	*	*...*	L	L...L	*
Invert mode	X	X	L	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Load S/R	H or L	↑	L	H	H	H or L	*...*	*	*...*	*
Load latches	X	H or L	↑	H	H	*	*...*	*	*...*	*
	X	H or L	↑	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Transparent latch mode	L	↑	H	H	H	L	*...*	L	*...*	*
	H	↑	H	H	H	H	*...*	H	*...*	*

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
* = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high,

Pin Configurations

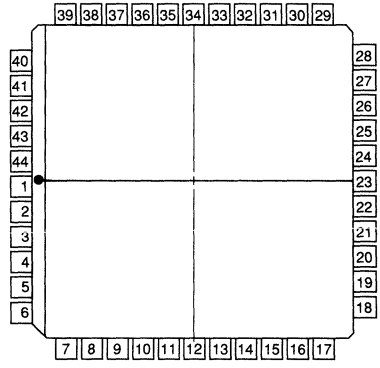
HV53
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 17	23	GND
2	HVout 16	24	V_{PP}
3	HVout 15	25	V_{DD}
4	HVout 14	26	Latch Enable
5	HVout 13	27	Data In
6	HVout 12	28	Blanking
7	HVout 11	29	N/C
8	HVout 10	30	HVout 32
9	HVout 9	31	HVout 31
10	HVout 8	32	HVout 30
11	HVout 7	33	HVout 29
12	HVout 6	34	HVout 28
13	HVout 5	35	HVout 27
14	HVout 4	36	HVout 26
15	HVout 3	37	HVout 25
16	HVout 2	38	HVout 24
17	HVout 1	39	HVout 23
18	Data Out	40	HVout 22
19	N/C	41	HVout 21
20	N/C	42	HVout 20
21	Polarity	43	HVout 19
22	Clock	44	HVout 18

HV58
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 16	23	GND
2	HVout 17	24	V_{PP}
3	HVout 18	25	V_{DD}
4	HVout 19	26	Latch Enable
5	HVout 20	27	Data In
6	HVout 21	28	Blanking
7	HVout 22	29	N/C
8	HVout 23	30	HVout 1
9	HVout 24	31	HVout 2
10	HVout 25	32	HVout 3
11	HVout 26	33	HVout 4
12	HVout 27	34	HVout 5
13	HVout 28	35	HVout 6
14	HVout 29	36	HVout 7
15	HVout 30	37	HVout 8
16	HVout 31	38	HVout 9
17	HVout 32	39	HVout 10
18	Data Out	40	HVout 11
19	N/C	41	HVout 12
20	N/C	42	HVout 13
21	$\overline{\text{Polarity}}$	43	HVout 14
22	Clock	44	HVout 15

Package Outline



top view

44-pin J-lead Package

Preliminary

32-Channel ±40V Liquid Crystal Display Driver

Ordering Information

Device	Package Options			
	Plastic 48-Pin DIP	Ceramic 48-Pin DIP	80-Lead Plastic Quad Gullwing	Die
HV6008	HV6008P	HV6008D	HV6008PG	HV6008X

Features

- ☐ Symmetrical ±40V output swing
- ☐ Active return to GND
- ☐ 15mA peak source/sink/GND current per channel
- ☐ ±5V control logic
- ☐ Special shift register with clear
- ☐ Phase shift control
- ☐ Output enable
- ☐ Data out enable
- ☐ 1MHz shift register
- ☐ Surface mount package available

Absolute Maximum Ratings

Supply voltage, V_{DD1}[1]	-6
Supply voltage, V_{DD2}[1]	+6
Supply voltage, V_{PP}[1,2]	+42V
Supply voltage, V_{NN}[1,2]	-42V
Logic input levels	V_{DD} + 0.3V to V_{DD2} + 0.3V
Ground currrent[2]	700mA
Continuous total power dissipation[3]	1W
Operating temperature range	
Storage temperature range	-65°C to +150°C

Notes: 1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 85°C at 15mW/°C.

General Description

The HV60 is a 32-channel liquid crystal display driver with 3-state DMOS outputs. Each output can be set to +40V, -40V, or ground. A symmetric waveform can be applied to a capacitive load using the phase shift feature of the HV60.

The HV60 consists of a 32-bit shift register with Clear, Enable, and Phase Shift logic, and 32 high voltage output buffers. With the Enable pin held low, all outputs are placed in the return to zero (GND) state. When Enable is high, each output reflects the data in its shift register bit. All outputs with a logic "0" in their shift register will be in the return to zero state. Outputs with a logic "1" in their shift register will reflect the state of the phase shift pin. These outputs will be switched to V_{PP} when phase shift is high and V_{NN} when phase shift is logic "0".

Additional functions provided are shift register clear and data out. All bits of the shift register are changed to logic "0" when clear is pulled low. With clear at a logic "1", normal shift register operation proceeds. The data output reflects the status of the 32nd shift register stage.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
$I_{DD1,2}$	V_{DD} supply current	V_{DD1}			500	µA	V_I = 4V, V_{DD1} = -6V
		V_{DD2}					V_I = 4V, V_{DD2} = +6V
V_{IH}	Logic input high		+2		V_{DD2}	V	V_{DD1} = -4.5V
V_{IL}	Logic input low		V_{DD1}		-2	V	V_{DD2} = +4.5V
V_{OH}	Logic output high		+2			V	V_{DD1} = -4.5V V_{DD2} = +4.5V
V_{OL}	Logic output low				-2	V	I_{OH} = -15µA I_{OL} = 250µA
I_{IH}	High-level logic input current				+3	µA	$V_I = V_{DD}$, $V_{DD1,2}$ = max
I_{IL}	Low-level logic input current				-50	µA	V_I = 0V, $V_{DD1,2}$ = max
I_{PP}	High voltage supply current				+1	mA	Static, no load
I_{NN}	High voltage supply current				+1	mA	Static, no load
V_{OH}	Output voltage high		+39			V	V_{PP}, V_{NN} = ±40 I_{output} = 0.0
V_{CL}	Output voltage clamp		-20		+20	mV	
V_{OL}	Output voltage low				-39	V	
Z_{OH}	Output switch impedence high			1000		Ω	V_{PP}, V_{NN} = ±40 I_O = ±15mA
Z_{CL}	Output switch impedance clamp			500			
Z_{OL}	Output switch impedance low			700			
I_O	DC output current	Output H or L			5	mA	1 output only
		Data out H or L			150	µA	

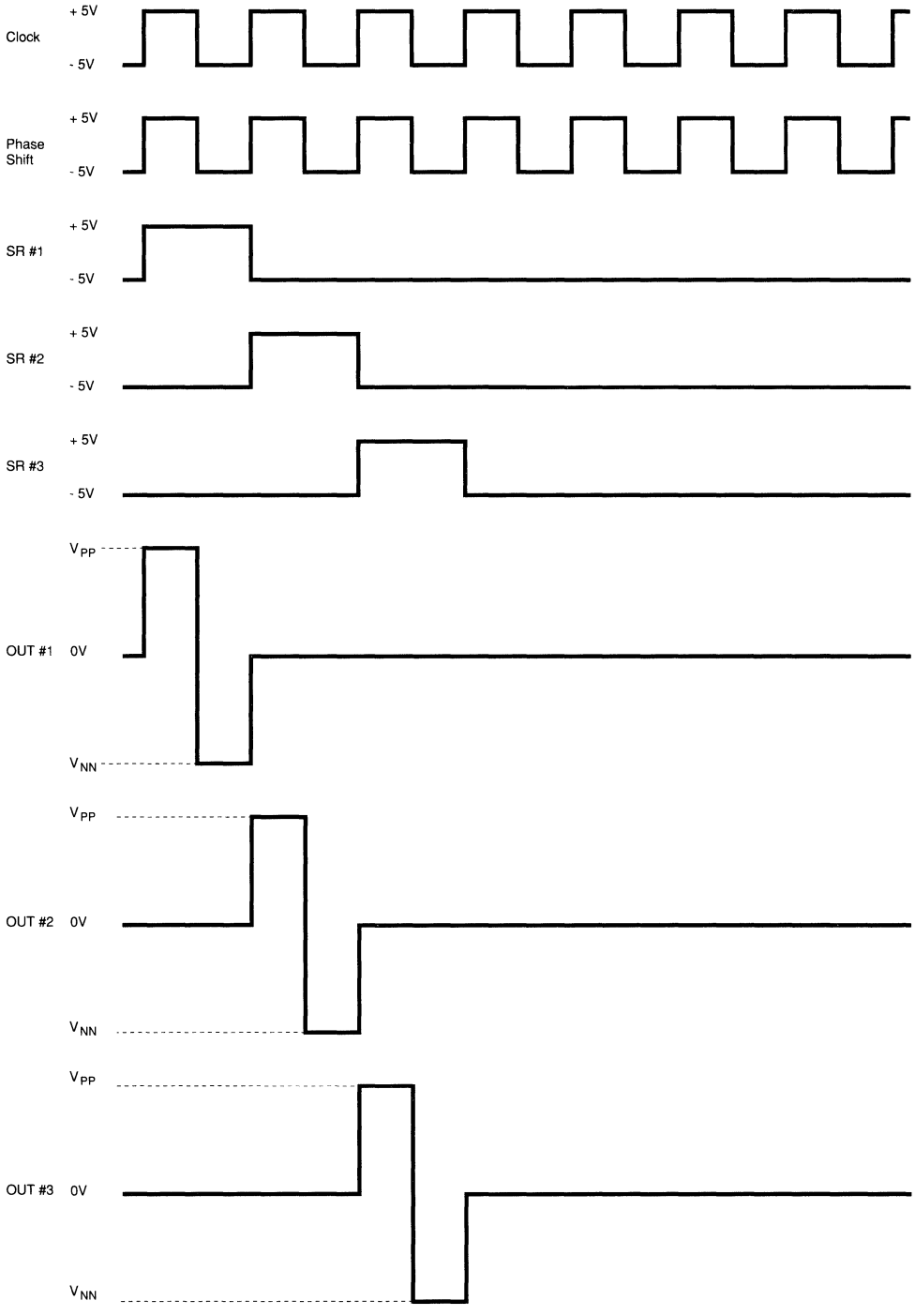
AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{WH}	Width of high clock phase		TBD			
t_{WL}	Width of low clock phase		TBD			
t_{SU}	Data set-up time before clock rises		TBD			
t_H	Data hold time after clock rises	0			ns	
	Phase shift duty cycle		50		%	

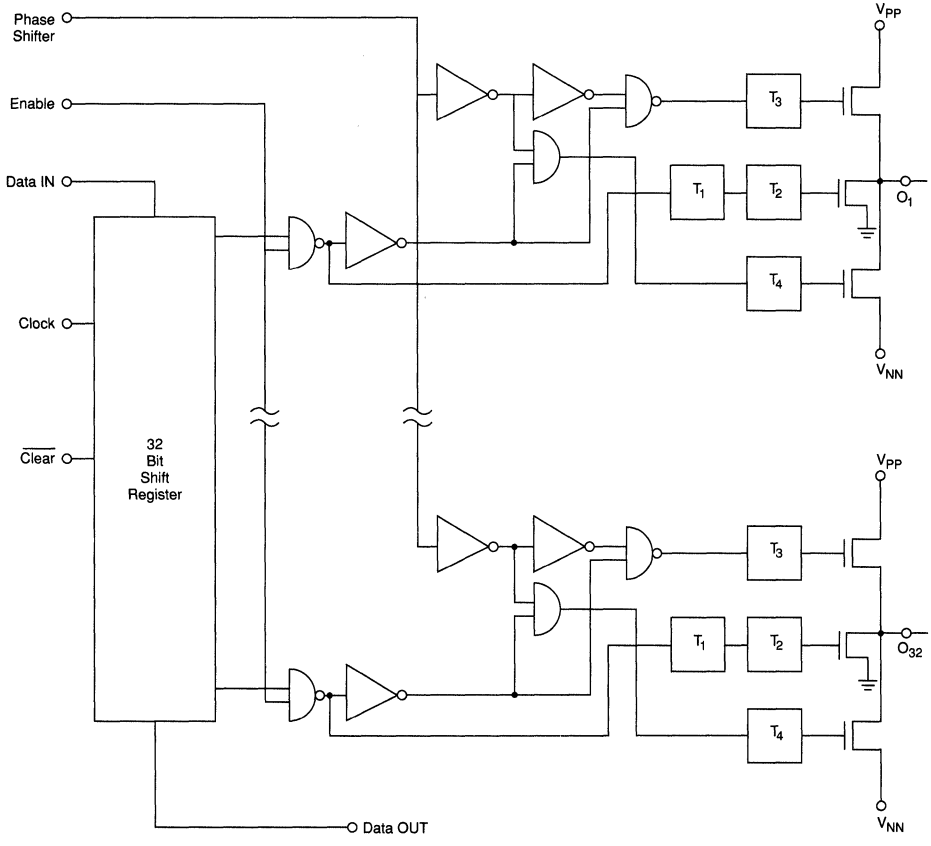
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD1}	Logic supply voltage	-4		-6	V
V_{DD2}	Logic supply voltage	+4		+6	V
V_{PP}	High voltage supply	+10		+40	V
V_{NN}	High voltage supply	-10		-40	V
V_{IH}	High-level input voltage	+2V		V_{DD2}	V
V_{IL}	Low-level input voltage	-2V		V_{DD1}	V
$I_{O\ Pk.}$	Peak output current (any state)			±80	mA
T_A	Operating free-air temperature	-10		+70	°C
f_{DIN}	Input data rate			1	MHz
f_{PS}	Phase shift rate			1	MHz

Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs						Outputs	
	Data In	CLK	$\overline{CLR}$	Enable	Phase Shift	Shift Reg 1 2...32	HV Outputs 1 2...32	Data Out
CLR Reg	X	X	L	X	X	ALL L	ALL GND	L
All output GND	X	X	X	L	X	* *...*	ALL GND	*
Load S/R	H or L	↑	H	L	X	H or L *...*	ALL GND	*
Output State	X	H or L	H	H	X	L L...L	GND GND...GND	*
					H	H H...H	V_{PP} V_{PP}...V_{PP}	*
					L	L L...L	V_{NN} V_{NN}...V_{NN}	*

Notes:
X = Don't care
* = Dependent on previous stage's state before the last CLK
↑ = Low to high transition
H = High level
L = Low level

Pin Configurations

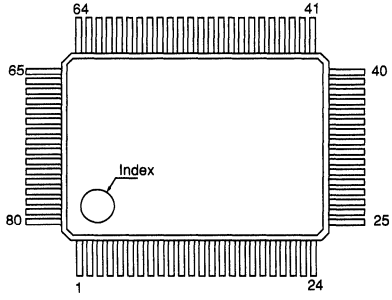
28-Pin J-Lead

Pin	Function	Pin	Function	Pin	Function
1	GND	28	Phase Shift	55	N/C
2	N/C	29	N/C	56	+40V
3	N/C	30	Clock	57	N/C
4	N/C	31	N/C	58	-40V
5	N/C	32	N/C	59	N/C
6	N/C	33	$\overline{\text{Clear}}$	60	N/C
7	-40V	34	N/C	61	N/C
8	N/C	35	-5V	62	N/C
9	+40V	36	Enable	63	N/C
10	N/C	37	N/C	64	GND
11	N/C	38	+5V	65	N/C
12	HVout 9	39	N/C	66	HVout 23
13	HVout 8	40	GND	67	HVout 22
14	HVout 7	41	N/C	68	HVout 21
15	HVout 6	42	Data Out	69	HVout 20
16	HVout 5	43	N/C	70	HVout 19
17	HVout 4	44	N/C	71	HVout 18
18	HVout 3	45	HVout 32	72	HVout 17
19	HVout 2	46	HVout 31	73	HVout 16
20	HVout 1	47	HVout 30	74	HVout 15
21	N/C	48	HVout 29	75	HVout 14
22	N/C	49	HVout 28	76	HVout 13
23	Data In	50	HVout 27	77	HVout 12
24	N/C	51	HVout 26	78	HVout 11
25	GND	52	HVout 25	79	HVout 10
26	N/C	53	HVout 24	80	N/C
27	N/C	54	N/C		

48-Pin DIP

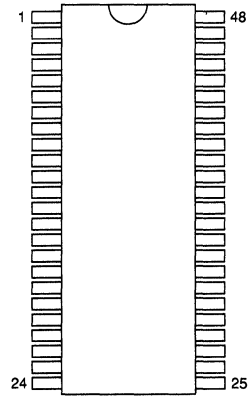
Pin	Function	Pin	Function
1	HVout 16	25	V_{DD1} (-5V)
2	HVout 15	26	Enable
3	HVout 14	27	V_{DD2} (+5V)
4	HVout 13	28	GND
5	HVout 12	29	Data Out
6	HVout 11	30	HVout 32
7	HVout 10	31	HVout 31
8	GND	32	HVout 30
9	V_{NN}	33	HVout 29
10	V_{PP}	34	HVout 28
11	HVout 9	35	HVout 27
12	HVout 8	36	HVout 26
13	HVout 7	37	HVout 25
14	HVout 6	38	HVout 24
15	HVout 5	39	V_{PP}
16	HVout 4	40	V_{NN}
17	HVout 3	41	GND
18	HVout 2	42	HVout 23
19	HVout 1	43	HVout 22
20	Data In	44	HVout 21
21	GND	45	HVout 20
22	Phase Shift	46	HVout 19
23	Clock	47	HVout 18
24	$\overline{\text{Clear}}$	48	HVout 17

Package Outlines



top view

80-pin Gullwing Package



top view

48-pin DIP

Preliminary

10-Channel Serial-Input Latched Display Driver

Ordering Information

Device	Package Options	
	18-Pin Plastic	20-Pin Small Outline Package
HV6810	HV6810P	HV6810WG

Features

- ☐ High output voltage 80V
- ☐ High speed 5MHz @ $5V_{DD}$
- ☐ Low power $I_{BB} \leq 0.1mA$ (All high)
- ☐ Active pull down 2.5mA min
- ☐ Output source current 60mA
- ☐ Each device drives 10 lines
- ☐ High-speed serially-shifted data input
- ☐ 5V CMOS-compatible inputs
- ☐ Latches on all driver outputs
- ☐ Pin-compatible improved replacement for UCN5810A and TL4810A, TL4810B

Absolute Maximum Ratings[1]

Logic supply voltage, V_{DD}[2]	7.5V
Driver supply voltage, V_{BB}	90V
Output voltage	90V
Input voltage	-0.3V to V_{DD} + 0.3V
Continuous total power dissipation at 25°C free-air temperature [3]	
P-Package	875mW

Notes: 1. Over operating free-air temperature.
2. All voltages are referenced to V_{SS}.
3. For operation above 25°C free-air temperature the derating factor is 7.0mW/°C.

General Description

The HV6810 is a monolithic integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). These devices feature a serial data output to cascade additional devices for large display arrays.

A 10-bit data word is serially loaded into the shift register on the positive-going transitions of the clock. Parallel data is transferred to the output buffers through a 10-bit D-type latch while the latch enable input is high and is latched when the latch enable is low. When the blanking input is high, all outputs are low.

Outputs are structures formed by double-diffused MOS (DMOS) transistors with output voltage ratings of 80 volts and 60 milliamperes source-current capability. All inputs are compatible with CMOS levels.

The HV6810 is characterized for operation from 0°C to 70°C.

Electrical Characteristics

DC Characteristics (V_{DD} = 5V ±10%, V_{BB} = 60V, V_{SS} = 0, unless otherwise noted)

Symbol	Parameter		Min	Typ	Max	Units	Conditions
V_{OH}	High-level output voltage	Q outputs	57.5	58		V	I_{OH} = 25mA
		Serial output	4	4.5		V	V_{DD} = 4.5V, I_{OH} = -100µA
V_{OL}	Low-level output voltage	Q outputs		0.15	1	V	I_{OH} = 1mA, Blanking input at V_{DD}
		Serial output		0.05	0.1	V	V_{DD} = 4.5V, I_{OL} = 100µA
I_{OL}	Low-level Q output current (pull-down current)		2.5	3.7		mA	T_A = Max
$I_{O(OFF)}$	Off-state output current			-1	-15	µA	V_O = 0, Blanking input T_A = Max at V_{DD}
I_H	High-level input current				1	µA	$V_I = V_{DD}$
I_{DD}	Supply current from V_{DD} (standby)			10	50	µA	All inputs at 0V, one Q output high
				10	50	µA	All inputs at 0V, all outputs low
I_{BB}	Supply current from V_{BB}			0.5	0.1	µA	All outputs low, all Q outputs open
				0.05	0.1	mA	All outputs high, all Q outputs open

AC Characteristics (Timing requirements over recommended operating conditions)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$t_{W(CKH)}$	Pulse duration, clock high	100			nS	
$t_{W(LEH)}$	Pulse duration, latch enable high	100			nS	
$t_{SU(D)}$	Setup time, data before clock	50			nS	
$t_{H(D)}$	Setup time, data after clock	50			nS	
$t_{CKH-LEH}$	Delay time, clock to latch enable high	50			ns	
t_{pd}*	Propagation delay time, latch enable to output		0.3		µS	

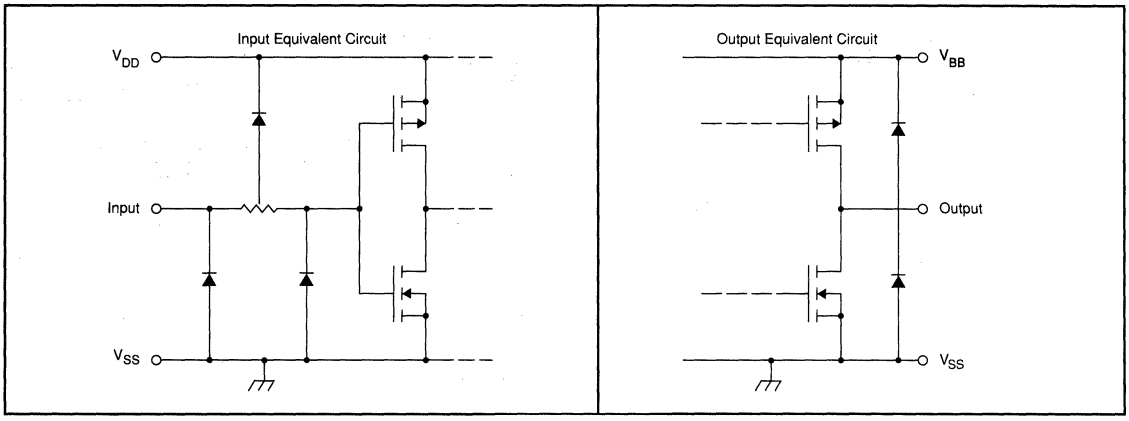
*Switching characteristics, V_{BB} = 60V, T_A = 25°C.

Recommended Operating Conditions

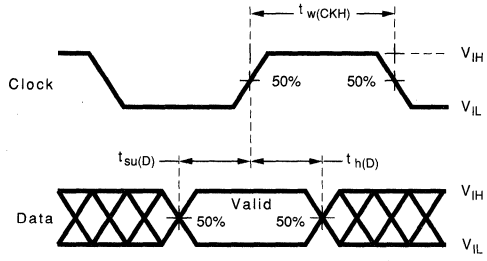
(Note 1)

Symbol	Parameter	Min	Nom	Max	Units
V_{DD}	Supply voltage	4.5		5.5	V
V_{BB}	Supply voltage	20		80	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage (for V_{DD} = 5V)	3.5	0	5.3	V
V_{IL}	Low-level input voltage	-0.3		-0.8	V
I_{OH}	Continuous high-level output current	0		-25	mA
T_A	Operating free-air temperature			70	°C

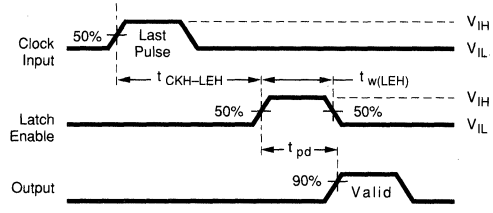
Input and Output Equivalent Circuits



Switching Waveforms

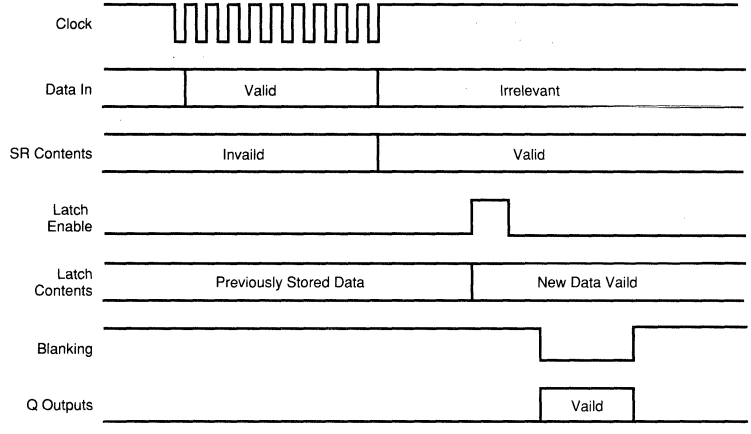


Input Timing



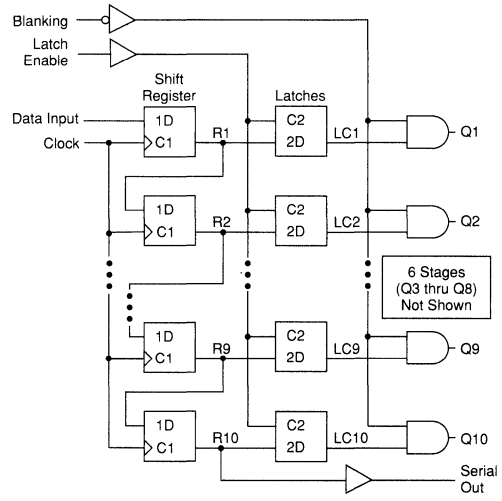
Output Switching Times

Timing Diagram



Functional Block Diagram

Logic Diagram (positive logic)



Function Table

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ... I_{N-1} I_N	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ... I_{N-1} I_N	Blanking Input	Output Contents I_1 I_2 I_3 ... I_{N-1} I_N
H	⎍	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⎍	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	⎎	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low logic level
H = High logic level
X = Irrelevant
P = Present state
R = Previous state

Pin Configurations

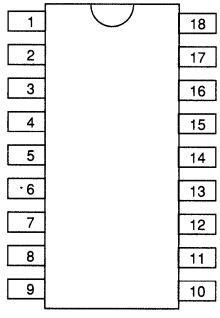
18-Pin DIP

Pin	Function	Pin	Function
1	Q8	10	Q3
2	Q7	11	Q2
3	Q6	12	Q1
4	Clock	13	Blanking
5	V_{SS}	14	Data in
6	V_{DD}	15	V_{BB}
7	LE (strobe)	16	Serial data out
8	Q5	17	Q10
9	Q4	18	Q9

20-Pin SOW

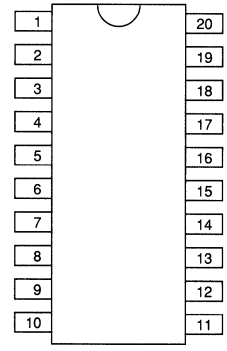
Pin	Function	Pin	Function
1	Q8	11	Q3
2	Q7	12	Q2
3	Q6	13	Q1
4	Clock	14	Blanking
5	V_{SS}	15	Data in
6	N/C	16	V_{BB}
7	V_{DD}	17	Serial data out
8	LE (strobe)	18	N/C
9	Q5	19	Q10
10	Q4	20	Q9

Package Outlines



top view

18-pin DIP



top view

SOW 20

Programmable Data Coder

Ordering Information

Device	28-Pin Plastic DIP	28-Pin Plastic Quad J Lead	28-Pin SO Gullwing	Die
DC-7	DC-7P	DC-7PJ	DC-7WG	DC-7X

Features

- ☐ 8 Data Bits (Byte Wide Data)
- ☐ 7 Address Bits (128 Addresses)
- ☐ Manchester Phase Encoding
- ☐ Transmitter/Receiver in one circuit
- ☐ Schmitt Trigger Input for excellent noise rejection
- ☐ Built-in Oscillator using non-critical RC Components
- ☐ Zener Diode to regulate the power supply
- ☐ Low Power, High Noise Immunity CMOS technology
- ☐ Ability to Decode Original Signals
- ☐ Automatic Preamble Generation

Applications

- ☐ Multi-port Computer I/O
- ☐ Smoke & Fire Alarm Control Systems
- ☐ Pocket Pagers
- ☐ Digital Locks
- ☐ Theft Alarm Systems
- ☐ Security Systems
- ☐ Digital Paging Systems
- ☐ Special Identification Code Systems
- ☐ Remote Sensor Data Acquisition Systems
- ☐ Single Channel Digital Transmission of Information

General Description

The DC-7 is a single monolithic chip using metal gate CMOS technology for low cost, low power, high yield and high reliability. This dual purpose circuit is capable of working either as an encoder or decoder on its own transmission in applications where exclusive recognition of address codes is required in addition to transmission or reception of 8 Data Bits. It will decode 1 of 128 address codes. In the transmit mode this circuit is capable of generating the possible codes by connecting the Address and Data Inputs to V_{DD} or GND for a "1" or a "0". In the receive mode this circuit is capable of decoding the transmitted signals and simultaneously making comparisons to the local address code for identification.

Absolute Maximum Ratings

Supply Voltage with respect to V_{SS}	6.4V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C
Zener Current	100mA

NOTE: All inputs except OI contain protection circuitry to prevent damage due to static charges. Care should be exercised to prevent application of voltages outside of the specification range. The OI has a special input protection circuit and special care should be taken with this input.

Electrical Characteristics

DC Characteristics (V_{DD} = 5.0 ± 5%; GRD = 0V; T_A = 25°C)

Symbol	Parameter	Min	Typ (Note 1)	Max	Unit	Conditions
V_{IH}	Input High Voltage	V_{DD} - 0.3		V_{DD} + 0.3	V	"1" INPUT
V_{IL}	Input Low Voltage	-0.3		0.3	V	"0" INPUT
I_{LKC}	Input Leakage Current		0.1	2.0	µA	V_{IN} = 5.0V for pins T/R, SDI
I_{LC}	Input Load Current	2.0	6.0	20.0	µA	V_{IN} = 5.0V for pins RS, A0 - A6, D0 - D7
V_{OH}	Output High Voltage	V_{DD} - 0.3			V	V_{DD} = 4.75V, I_{LOAD} = -100µA
V_{OL}	Output Low Voltage			0.3	V	V_{DD} = 4.75V, I_{LOAD} = 100µA
I_{OH}	Output High Current (Sourcing)	-1.0	-1.5		mA	V_{OH} = V_{DD} - 1.0V
I_{OL}	Output Low Current (Sinking)	1.0	3.0		mA	V_{OL} = 1.0V
V_Z	Zener Voltage	5.5	6.4	7.0	V	I_Z = 10µA (Note 2)
		6.0	6.7	7.5	V	I_Z = 10mA (Note 2)
C_{IN}	Input Capacitance			10	pF	(Note 2)
C_{ONT}	Output Capacitance			10	pF	(Note 2)
I_{DD}	Drain Current			10	µA	V_{DD} = 5.0V, all inputs = GRD all outputs floating

Note 1: Typical values are those values measured in a production sample at V_{CC} = 5.0V.
Note 2: This parameter is periodcally sampled and is not 100% tested.

AC Characteristics (V_{DD} = 5.0 ± 5%; T_A = 25°C)

Symbol	Parameter	Min	Typ (Note 1)	Max	Unit	Conditions
f_C	Clock Frequency	0		25	kHz	R = 150k, C = 100pF; Clock Period (t_C) = 1/f_c
t_{SDI}	Start Pulse Width	500			ns	
t_{DDO}	DDO Delay from SDI		5		µs	
t_{DC}	Data Clock Pulse Width		$5t_C$		sec	
t_{WORD}	Full Cycle Word Length		$130t_C$		sec	
R_R	Receiver Oscillator Resistor Tolerance from Transmitter Oscillator Resistor		±10		%	
C_R	Receiver Oscillator Capacitor Tolerance from Transmitter Oscillator Capacitor		±10		%	

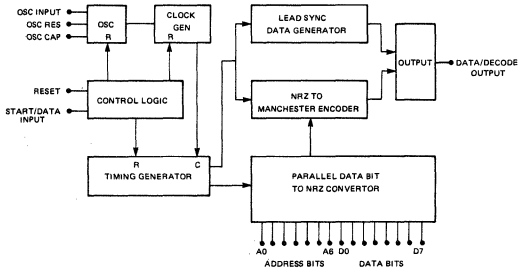
Note 1: Typical values are those values measured on a production sample at V_{CC} = 5.0V.

Pin Definition

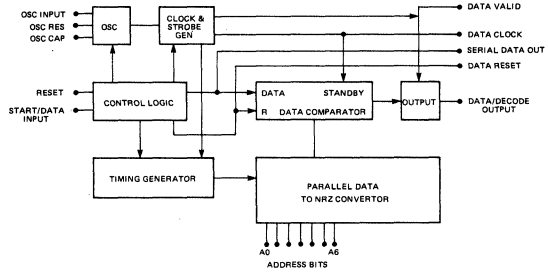
Label	Pin Name	Function
GND	Ground	Supply Potential negative side.
OI	Oscillator Input	This input is to drive the oscillator and is the tie point of the timing resistor (R_T), and the timing capacitor (C_T). It also is connected through a diode to an open drain P-channel device that turns on to V_{DD} when the oscillator is being reset. This input can exceed the power supplies and does during normal oscillator operation.
OR	Oscillator	Provides phase feedback to the RC timing circuit through the connected timing resistor. Note: This Resistor pin is driven high during oscillator reset.
OC	Oscillator Capacitor	Capacitor connection of RC timing circuit provides phased feedback from the oscillator. This pin is driven low during oscillator reset.
RS	Reset	This input pin may be used to override the data transmission cycle or inhibiting a SDI input. It clears the D/DO to a low state and resets the internal oscillator and data comparison circuits. This pin may be left open (No Connection) when not used, or driven as an input, or an external capacitor (100pF) to V_{DD} may be added for power-up reset. The Reset function is activated when this input is connected to V_{DD}.
S/DI	Start/Data Input	Start/Data input is a dual function pin. It is used to start the oscillator which enables the transmission of the encoded word in the transmit mode. And, in the receive mode, this input receives the serial coded information for processing and comparison.
D/DO	Data/Decode Output	Another dual purpose pin, this pin is the encoded sequence data output in the transmit mode and becomes the decode true output in the receive mode. It indicates that the incoming code has matched the local bit data input address.
A0-A6	Address Inputs	These Inputs provide the parallel Address to be sequentially transmitted. In the receive mode, these inputs become the parallel local Address code for comparison with the incoming data.
D0-D7	Data Bit Inputs	These Inputs provide parallel data to be sequentially transmitted. In the receive mode, these Inputs are not used.
SDO	Serial Data Output	This output signal is a buffered S/DI signal after going through the input Schmitt Trigger — a delay circuit, and is the same polarity as the input and can be used to chain a number of receivers together. This output can be connected to the input of a 8-bit shift register (clocked by the DC pin) in a receiver system where data is to be recovered. This output can be connected to the input of a 16-bit shift register (clocked by the DC pin) in a receiver system where Address and data are to be recovered.
DRS	Data Reset Output	Data Reset can be used in the receive mode to reset an external data shift register since this signal pulse indicates that a new word has just begun processing.
DC	Data Clock Outputs	The Data Clock output may be used in a receive system since it is the recovered data sync pulses. Also, this output can be used to clock an external shift register where data is to be recovered.
DV	Data Valid Output	This output is triggered low at the start of any input and will remain low until a complete word has been processed. Note that this output simply signals that a valid word has been received and not that the code received has matched the local address code.
T/R	Transmit/ Receive	This is a control input to determine the operating mode. A logic high applied to this input puts it in the transmit mode, a logic low puts it in the receive mode.
V_{DD}	V_{DD}	Positive Supply Potential — This circuit contains an on-chip zener of approximately 6.7 volts across the supply terminals.

Block Diagrams

TRANSMITTER



RECEIVER



Operation

General

The DC-7 mode of operation is controlled by the Transmit/Receive control input (T/R). When switched for V_{DD} to GND, the circuit will automatically change the oscillator, Start/Data Input, and Data Decoder Output from Transmit to Receive mode.

The DC-7 contains an on-chip zener diode to clamp the power supply to around 6.7 volts. The circuit will operate from 4.0 volts to the zener voltage, but operation is recommended at 5 volts ± 5%, or a regulated power supply in order to stabilize the time constants of the oscillator circuit. In order to use the on-chip zener diode, a current limiting resistor of 1K ohm or greater is required. If pull up resistors are used for the D_1 - D_{15} drivers, the resistors should be tied to a voltage no higher than that on Pin 28 or 6 volts, whichever is lower.

Output drivers are capable of sinking or sourcing 1.0mA minimum at 1.0 volts V_{DS}. All inputs are gate protected to both power supplies by internal diodes. The Address Data inputs of the DC-7 each have pull down resistors to ground so that only a "1" will have to be programmed. This allows the inputs to be programmed by using SPST switches or jumpers to V_{DD} only. The Transmit/Receive input does not have a pull up or pull down resistor. The Start/Data Input also does not have a pull up or pull down resistor, but is applied to a Schmitt Trigger Input circuit to improve noise rejection.

Transmit Function

This function is selected by connecting the Transmit/Receive control input to V_{DD}. This enables the Transmit mode and the circuit to function as an encoder — sampling the 7 Address and 8 Data Input pins digital information and encoding this parallel data in NRZ format, combining it with the clock in Manchester Code (Phase Encoded) and presenting it to the D/DO pin for transmission. (Usually to another DC device used as the decoder circuit). The encoder will transmit the serial data each time the Start/Data input is activated.

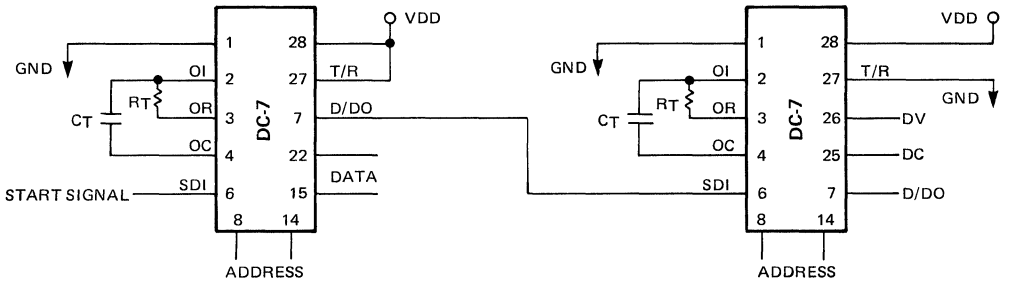
This encoded Data word is transmitted in 2 parts. The first part is the preamble information which is a series of 12 "1"s and then a space indicating that the encoded Data is to follow. This preamble information is intended to be used to synchronize a phase locked loop at the receiver or used as a setting time for receivers that have automatic gain control. The second part contains the 7 bits of address and 8 bits of data.

Receive Function

The receive mode is selected by connecting the Transmit/Receive control input to ground. In this mode the circuit will work as a decoder receiving the serial data in Manchester Coded format and recovering the clock. The incoming data is converted to a 15-bit serial word. It is compared with the local address word by sampling the Address Inputs (7-bits). These bits are usually programmed to the expected Address that will be decoded. If the two Address words match, the decoded output will become logic "1" state, but if the two do not match the decoded output will stay low. Also, if the words do not match but the bit stream was valid (i.e., 15-bits of proper timing) then only the output valid signal will go high. If at any time the bit sequence has the wrong timing, the local oscillator and internal comparison circuits will be reset and any new input pulses will be recognized as a new bit stream. Therefore, as with the receiver processing of the preamble information, the 12-bits will be recognized. But, during the 13th interval where no bit transition occurs, the circuit times-out and awaits the start bit of the address and data sequence.

The DC-7 will only compare the first 7 bits and ignore the state of the last 8 bits — that is, 128 distinct address codes with 8 bits that may be used for data transmission.

Transmit and Receive Address and Data Patterns



Transmitted Bit Sequence

1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
A0						A6	D0								D7

Received Address Code

1	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D
A0						A6	D0								D7

NOTE: Bit Sequence Code Format.

X = Programmable

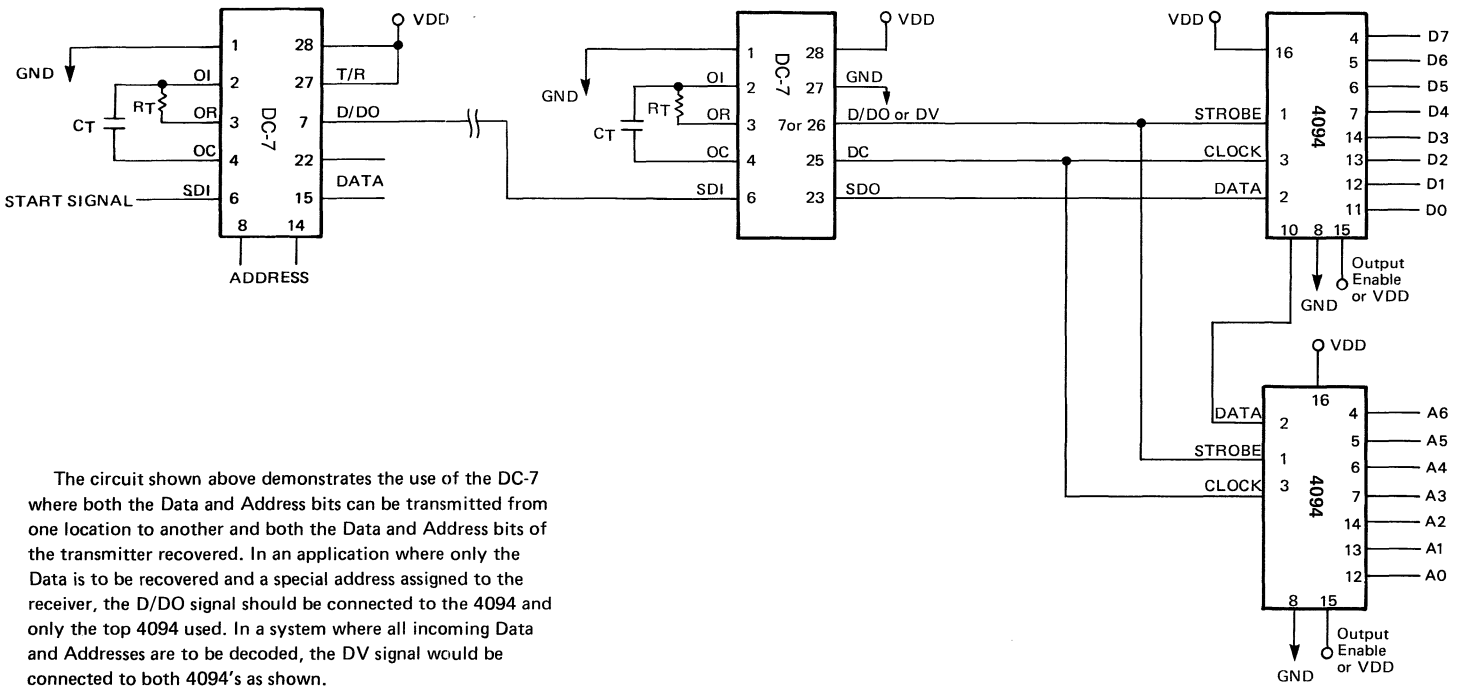
0 = Hardwired Internally Zero

1 = Hardwired Internally One

D = Don't Care in Receive Mode (Data)

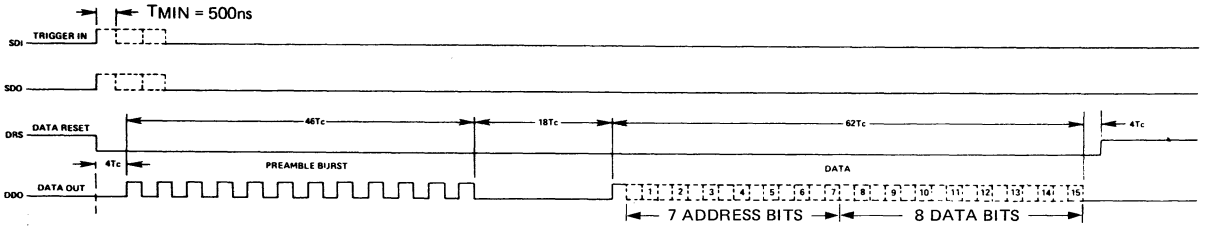
Note: When unused, the DV, DC, DRS and SDO pins should be left floating and *must not* be tied to either a power supply or to ground.

Typical Application



The circuit shown above demonstrates the use of the DC-7 where both the Data and Address bits can be transmitted from one location to another and both the Data and Address bits of the transmitter recovered. In an application where only the Data is to be recovered and a special address assigned to the receiver, the D/DO signal should be connected to the 4094 and only the top 4094 used. In a system where all incoming Data and Addresses are to be decoded, the DV signal would be connected to both 4094's as shown.

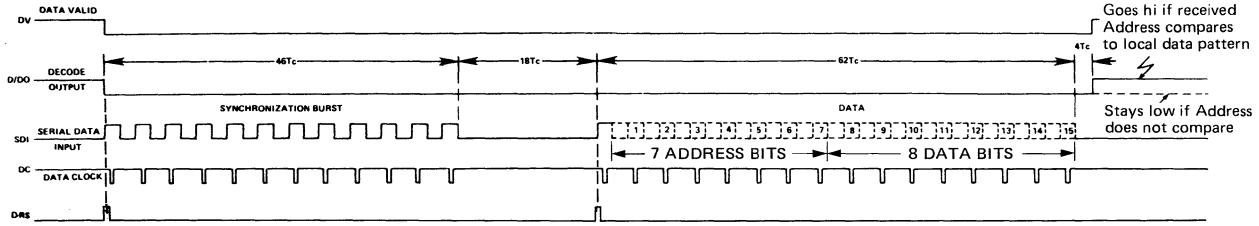
Timing Diagram – Transmit Mode



Total Time Required for Transmission of One Sequence = (DRS – 4Tc) = 130Tc

$$Tc = \frac{1}{\text{CLOCK FREQUENCY}}$$

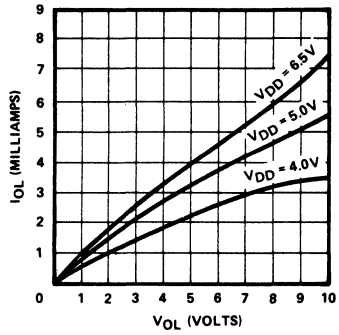
Timing Diagram – Receive Mode



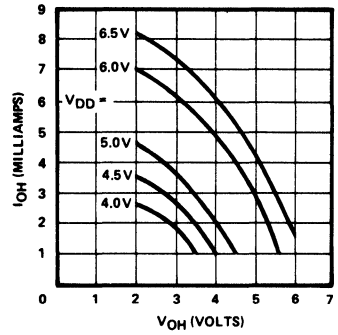
$$Tc = \frac{1}{\text{CLOCK FREQUENCY}}$$

Typical Performance Curves (T_A = 25°C unless otherwise noted)

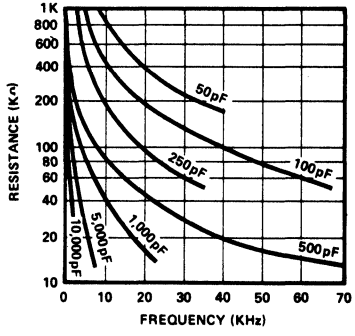
I_{OL} vs V_{DD} vs V_{OL}



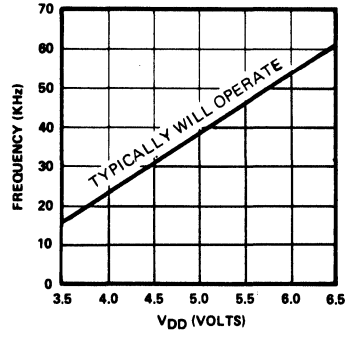
I_{OH} vs V_{DD} vs V_{OH}



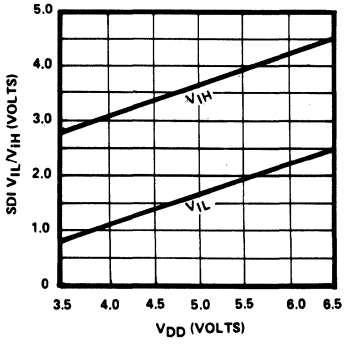
RESISTANCE vs OSCILLATOR FREQUENCY



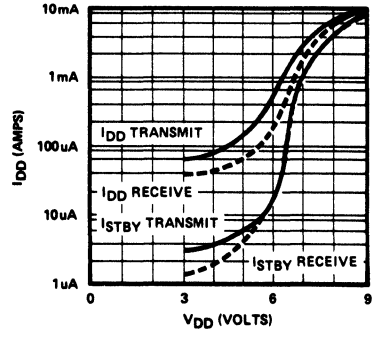
OPERATING FREQUENCY vs V_{DD}



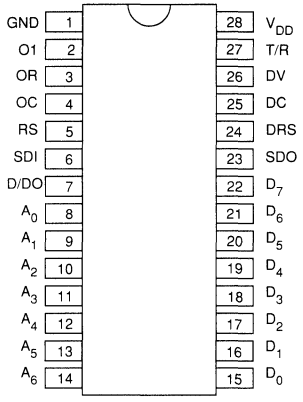
SDI INPUT V_{IL}/V_{IH} vs V_{DD}



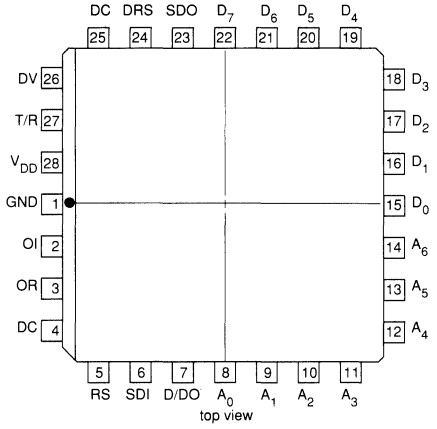
I_{DD} vs V_{DD}



Pin Configuration



28-pin DIP



28-pin J-lead Package

Progammable Encoder/Decoder

Ordering Information

Device	Package	Order No.
ED-15	28-Pin Plastic DIP 28-Pin Plastic Chip Carrier 28-Pin SOW Package	ED-15P ED-15J ED-15WG
ED-11	28-Pin Plastic DIP 28-Pin SOW Package	ED-11P ED-11-WG
ED-9	18-Pin Plastic DIP 20-Pin SOW Package	ED-9P ED-9WG
ED-5	18-Pin Plastic DIP	ED-5P

Features

- ☐ Manchester Phase Encoding
- ☐ Encoder/Decoder in one circuit
- ☐ Schmitt Trigger Input for excellent noise rejection
- ☐ Built-in Oscillator using non-critical RC Components
- ☐ Zener Diode to regulate the power supply
- ☐ Low Power, High Noise Immunity CMOS technology
- ☐ Ability to Decode Original Signals
- ☐ Automatic Preamble Generation

Applications

- ☐ Smoke & Fire Alarm Control Systems
- ☐ Security Systems
- ☐ Theft Alarm Systems
- ☐ Digital Locks
- ☐ Digital Paging Systems
- ☐ Garage Door Openers
- ☐ Systems that require a Special Identification Code
- ☐ Pocket Pagers
- ☐ Recognition or Transmission

General Description

The ED series is a single monolithic chip using metal-gate CMOS technology for low cost, low power, high yield and high reliability. It is a dual purpose circuit, capable of working either as an encoder or as decoder on its own transmissions in applications where exclusive recognition of a special code is required. It will decode 1 of 32,768 codes. In the transmit mode each circuit is capable of generating the possible codes by connecting the Data Inputs to V_{DD} or GRD for a "1" or a "0". In the receive mode each circuit is capable of decoding the transmitted signal and simultaneously making a comparison to the local address code for identification.

Absolute Maximum Ratings

Supply Voltage with respect to V_{SS}	6.4V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C
Zener Current	100mA

Note: All inputs except OI contain protection circuitry to prevent damage due to static charges. Care should be exercised to prevent application of voltages outside of the specification range. The OI has a special input protection circuit and special care should be taken with this input.

Electrical Characteristics

DC Characteristics (V_{DD} = 5.0 ± 5%; GRD = 0V; T_A = 25°C)

Symbol	Parameter	Min	Typ Note 1	Max	Unit	Conditions
V_{IH}	Input High Voltage	V_{DD} - 0.3		V_{DD} + 0.3	V	"1" INPUT
V_{IL}	Input Low Voltage	-0.3		0.3	V	"0" INPUT
I_{LKC}	Input Leakage Current		0.1	2.0	µA	V_{IN} = 5.0V for pins T/R, SDI
I_{LC}	Input Load Current	2.0	6.0	20.0	µA	V_{IN} = 5.0V for pins RS, D1-D15
V_{OH}	Output High Voltage	V_{DD} - 0.3			V	V_{DD} = 4.75V, I_{LOAD} = -100µA
V_{OL}	Output Low Voltage			0.3	V	V_{DD} = 4.75V, I_{LOAD} = 100µA
I_{OH}	Output High Current (Sourcing)	-1.0	-1.5		mA	V_{OH} = V_{DD} - 1.0V
I_{OL}	Output Low Current (Sinking)	1.0	3.0		mA	V_{OL} = 1.0V
V_Z	Zener Voltage	5.5	6.4	7.0	V	I_Z = 10µA (Note 2)
		6.0	6.7	7.5	V	I_Z = 10mA (Note 2)
C_{IN}	Input Capacitance			10	pF	(Note 2)
C_{ONT}	Output Capacitance			10	pF	(Note 2)
I_{DD}	Drain Current			10	µA	V_{DD} = 5.0V, all inputs = GRD all outputs floating

Note 1: Typical values are those values measured in a production sample at V_{CC} = 5.0V.
Note 2: This parameter is periodcally sampled and is not 100% tested.

AC Characteristics (V_{DD} = 5.0 ± 5%; T_A = 25°C)

Symbol	Parameter	Min	Typ Note1	Max	Unit	Conditions
f_c	Clock Frequency	0		25	kHz	R= 150k, C= 100pF; Clock Period (t_c)=1/f_c
t_{SDI}	Start Pulse Width	500			ns	
t_{DDO}	DDO Delay from SDI		5		µs	
t_{DC}	Data Clock Pulse Width		$5t_c$		sec	
t_{WORD}	Full Cycle Word Length		$130t_c$		sec	
R_R	Receiver Oscillator Resistor Tolerance from Transmitter Oscillator Resistor		±10		%	
C_R	Receiver Oscillator Capacitor Tolerance from Transmitter Oscillator Capacitor		±10		%	

Note 1: Typical values are those values measured on a production sample at V_{CC} = 5.0V.

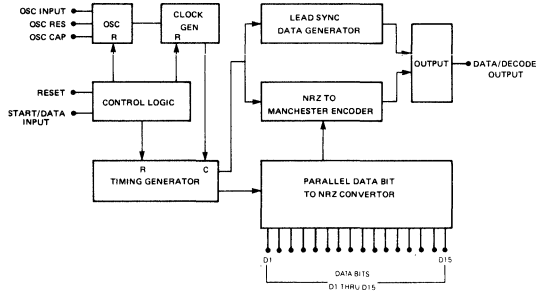
Pin Definition

Label	Pin Name	Function
GND	Ground	Supply Potential negative side.
OI	Oscillator Input	This input is to drive the oscillator and is the tie point of the timing resistor (R_T), and the timing capacitor (C_T). It also is connected through a diode to an open drain P-channel device that turns on to V_{DD} when the oscillator is being reset. This input can exceed the power supplies and does during normal oscillator operation.
OR	Oscillator Resistor	Provides phase feedback to the RC timing circuit through the connected timing resistor. Note: This pin is driven high during oscillator reset.
OC	Oscillator Capacitor	Capacitor connection of RC timing circuit provides phased feedback from the oscillator. This pin is driven low during oscillator reset.

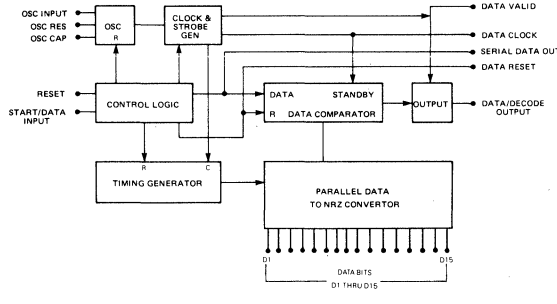
RS	Reset Input	This input pin may be used to override the data transmission cycle or inhibiting an SDI input. It clears the D/DO to a low state and resets the internal oscillator and data comparison circuits. This pin may be left open (No Connection) when not used, or driven as an input, or an external capacitor (100pf) to V_{DD} may be added for power-up reset. The Reset function is activated when this input is connected to V_{DD}.
S/DI	Start/Data Input	Start/Data input is a dual function pin. It is used to start the oscillator which enables the transmission of the encoded word in the transmit mode. And in the receive mode, this input receives the serial coded information for processing and comparison.
D/DO	Data/Decode Output	Another dual purpose pin, this pin is the encoded sequence data output in the transmit mode and becomes the decode true output in the receive mode. It indicates that the incoming code has matched the local bit data input address.
D1-D15	Data Bit Inputs	These Inputs provide parallel input data to be sequentially transmitted. The 18-pin package options have some pins omitted and hence these data positions will have logical zeros transmitted. In the receive mode, these imputs become the parallel local addres code for comparison with the incoming data. Note that with the ED-11 and ED-5 options, the data bits 11-15 are not used in the comparison when in the receive mode.
SDO	Serial Data Output	This output signal is a buffered S/DI signal after going through the input Schmitt Trigger — a delay circuit, and is the same polarity as the input and can be used to chain a number of receivers together. This output can be connected to the input of a 16-bit shift register (clocked by the DC pin) in a receiver system where data is to be recovered regardless of its comparison to a preset address word.
DRS	Data Reset Output	Data Reset can be used in the receive mode to reset an external data shift register since this Output signal pulse indicates that a new word has just begun processing.
DC	Data Clock Output	The Data Clock output may be used in a receive system since it is the recovered data sync pulses. Also, this output can be used to clock an external shift register where data is to be recovered.
DV	Data Valid Output	This output is triggered low at the start of any input and will remain low until a complete word has been processed. Note that this output simply signals that a valid word has been received and not that the code received has matched the local address code.
T/R	Transmit/ Receive	This is a control input to determine the operating mode. A logic high applied to this input puts it in the transmit mode; a logic low puts it in the receive mode.
V_{DD}	V_{DD}	Positive Supply Potential — This circuit contains an on-chip zener of approximately 6.7 volts across the supply terminals.

Block Diagrams

TRANSMITTER



RECEIVER



Operation

ED-15 General Description

The ED-15 series mode of operation is controlled by the Transmit/Receive control input (T/R). When switched for V_{DD} to GND, the circuit will automatically change the oscillator, Start/Data input, and Data/Decoder Output from Transmit to Receive mode.

The circuit contains an on-chip zener diode to clamp the power supply to around 6.7 volts. The circuit will operate from 4.0 volts to the zener voltage, but operation is recommended at 5 volts ± 5% in order to stabilize the time constants of the oscillator circuit. In order to use the on-chip zener diode, a current limiting resistor of 1K ohm or greater is required. If pull up resistors are used for the D_1 - D_{15} drives, the resistors should be tied to voltage no higher than that on Pin 28 or 6 volts, whichever is lower.

Output drivers are capable of sinking or sourcing 1.0 mA minimum at 1.0 volts V_{DS}. All inputs are gate protected to both power supplies by internal diodes. The Data Inputs each have pull down resistors to ground so that only a "1" will have to be programmed. This allows the inputs to be programmed by using SPST switches or jumpers to V_{DD} only. The Transmit/Receive input does not have a pull up or pull down resistor. The Start/Data Input also does not have a pull up or pull down resistor, but is applied to a Schmitt Trigger Input circuit to improve noise rejection.

Encoder Function

This function is selected by connecting the Transmit/Receive control input to V_{DD}. This enables the Transmit mode and the circuit to function as an encoder — sampling the 15 Data Input pins digital information and encoding this parallel data in NRZ format, combining it with the clock in Manchester Code (Phase Encoded), and presenting it to the D/DO pin for transmission (usually to another ED devise used as the decoder circuit). The encoder will transmit the serial data each time the Start/Data input is activated.

This encoded Data word is transmitted in 2 parts. The first part is the preamble information which is a series of 12 "1"'s, then a space indicating that the encoded Data is to follow. This preamble information is intended to be used to synchronize a phase locked loop at the receiver or used as a settling time for receivers that have automatic gain control. The second part contains the 15 bits of addresses and/or controls.

Decoder Function

The receive mode is selected by connecting the Transmit/Receive control input to ground. In this mode the circuit will work as a decoder, receiving the serial data in Manchester Coded format and recover the clock. The incoming data is converted to a 15-bit serial word. Compare it with the local data word by sampling the Data Inputs (15-bits). These bits are usually programmed to the expected Data that will be decoded. If the two data words match, the decoded output will become logic "1" state, but if the two words do not match the decoded output will stay low. Also, if the words do not match but the bit stream was valid (i.e., 15-bits of proper timing) then only the output valid signal will go high. If at any time the bit sequence has the wrong timing, the local oscillator and internal comparison circuits will be reset and any new input pulses will be recognized as a new bit stream. Therefore, as with the receiver processing of the preamble information, the 12 bits will be recognized. But during the 13th interval where no bit transition occurs, the circuit times-out and awaits the start bit of the data sequence.

ED-9 Option

The ED-9 is an 18-pin packaging of the ED-15 die. The operation and function of this circuit is the same as the ED-15; the only difference being the available pins. In the transmit mode the circuit is only capable of encoding 9 bits of data, the other 6 bits are not programmable and remain zeros. The pin configuration also drops DV, DC, DRS, and SDO such that the circuit can now only respond to a data match condition on the only output D/DO. In the receive mode the circuit can decode the same 9 bits of data, enabling up to 512 possible addresses.

ED-11 Option

The ED-11 differs from the ED-15 in that in the receive mode the ED-11 will only compare the first 11 bits and ignore the state of the last 4 bits — that is 2048 distinct address codes with 4 bits may be used for control data transmission.

ED-5 Option

The 18-pin packaging option of the ED-11 die is called ED-5. In the transmit mode it is only capable of 5 bits of programmable code. All the other bits are held at zero. But in the receive mode, the circuit has the five (32) unlock code bits plus the last four transparent bits of the ED-11. The ED-5 also supplies the necessary output signals to process the 4 bits of control data.

Transmit and Receive Data Patterns of ED-Series Devices

NOTE: Bit Sequence Code Format

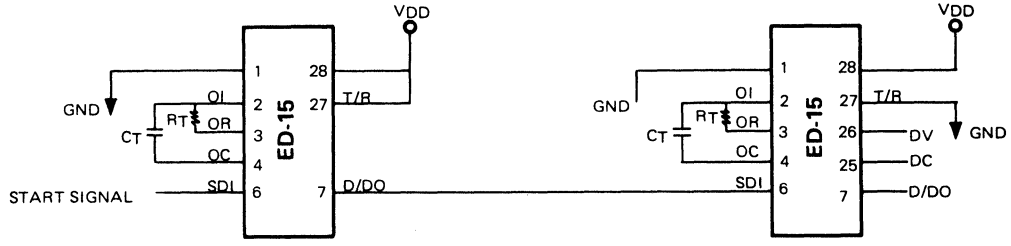
X = Programmable

0 = Hardwired Internally Zero

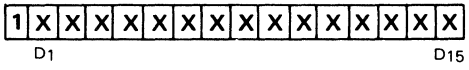
1 = Hardwired Internally One

D = Don't Care in Receive Mode

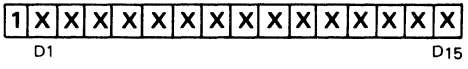
ED-15 to ED-15



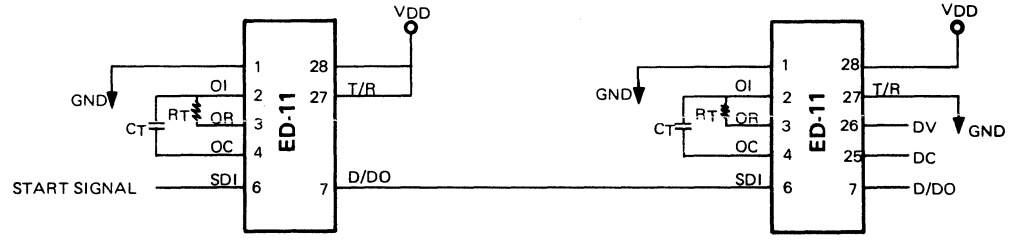
Transmitted Bit Sequence



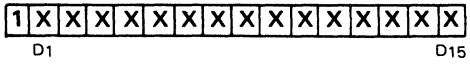
Received Address Code



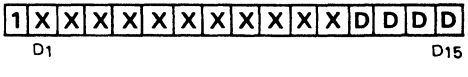
ED-11 to ED-11



Transmitted Bit Sequence

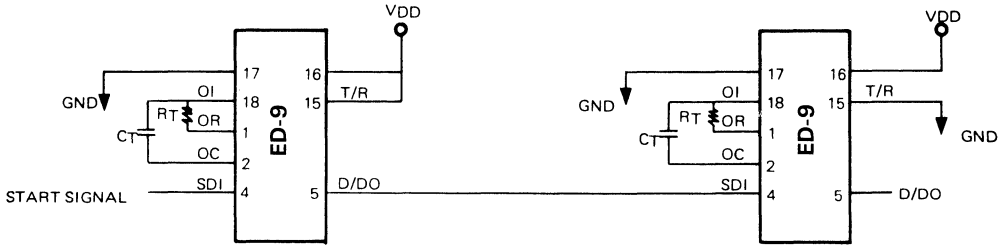


Received Address Code



Note: When unused, the DV, DC, DRS and SDO pins should be left floating and **must not** be tied to either a power supply or to ground.

ED-9 to ED-9



Transmitted Bit Sequence

1	0	0	0	X	X	X	X	0	X	0	0	X	X	X	X

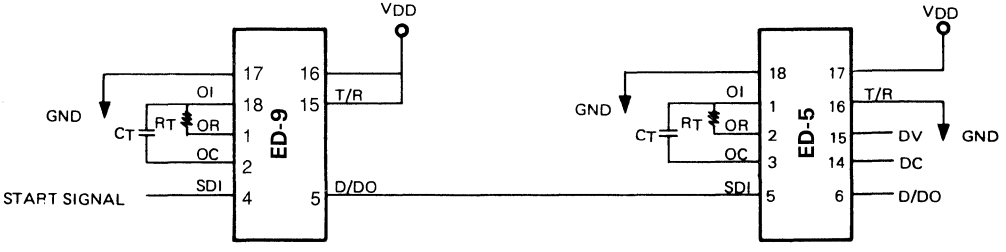
D1 D15

Received Address Code

1	0	0	0	X	X	X	X	0	X	0	0	X	X	X	X

D1 D15

ED-9 to ED-5



Transmitted Bit Sequence

1	0	0	0	X	X	X	X	0	X	0	0	X	X	X	X

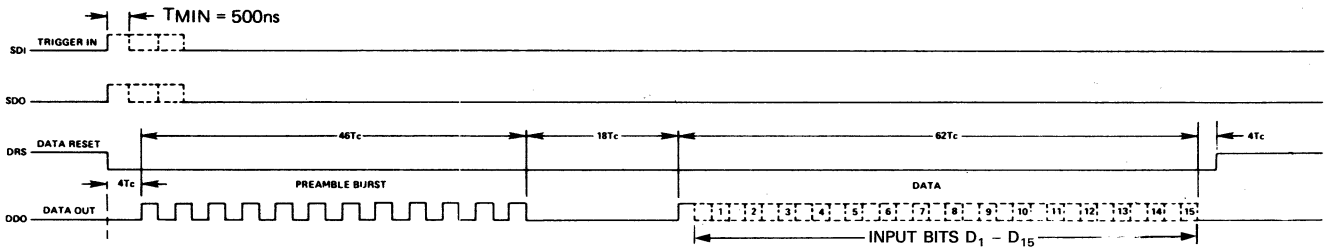
D1 D15

Received Address Code

1	0	0	0	X	X	X	X	0	X	0	0	D	D	D	D

D1 D15

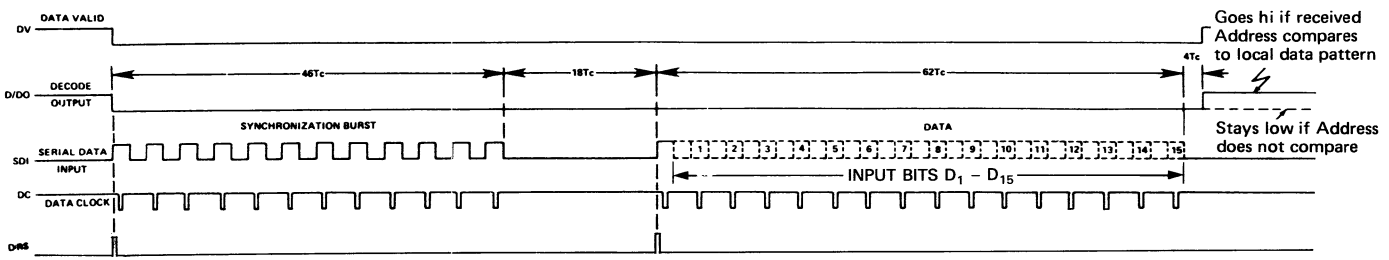
Timing Diagram – Transmit Mode



Total Time Required for Transmission of One Sequence = (DRS – 4Tc) = 130Tc

$$Tc = \frac{1}{\text{CLOCK FREQUENCY}}$$

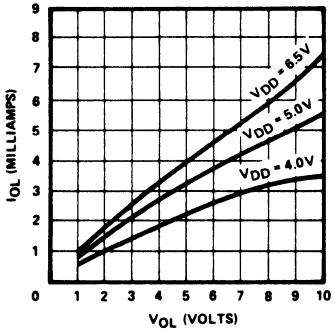
Timing Diagram – Receive Mode



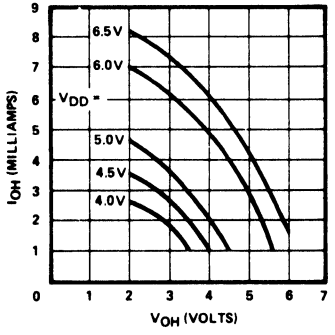
$$Tc = \frac{1}{\text{CLOCK FREQUENCY}}$$

Typical Performance Curves (T_A = 25°C unless otherwise noted)

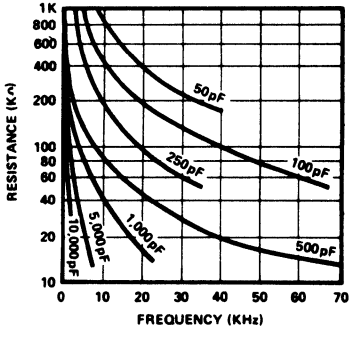
I_{OL} vs V_{DD} vs V_{OL}



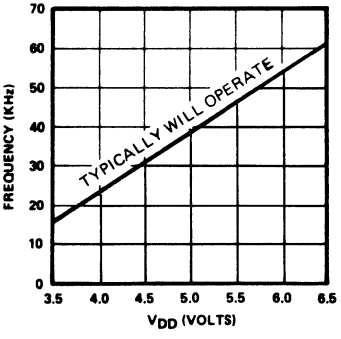
I_{OH} vs V_{DD} vs V_{OH}



RESISTANCE vs OSCILLATOR FREQUENCY

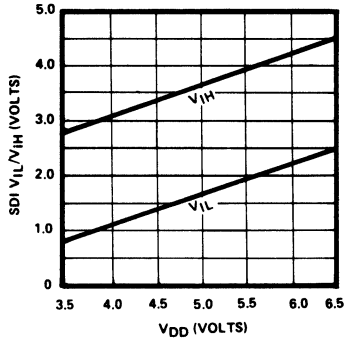


OPERATING FREQUENCY vs V_{DD}

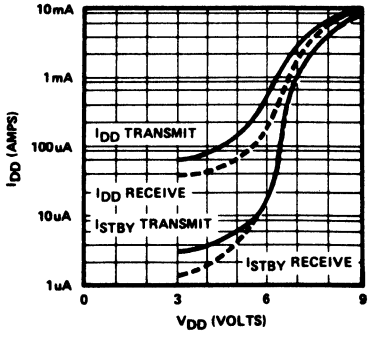


12

SDI INPUT V_{IL}/V_{IH} vs V_{DD}

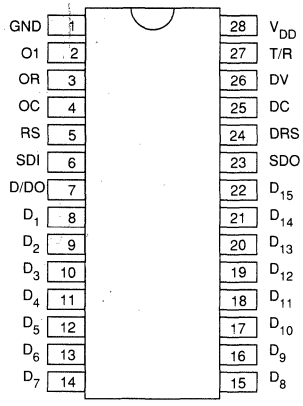


I_{DD} vs V_{DD}



Pin Configuration

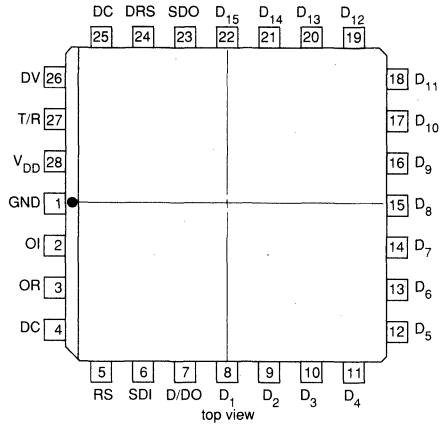
ED-15 & ED-11



top view

28-pin DIP

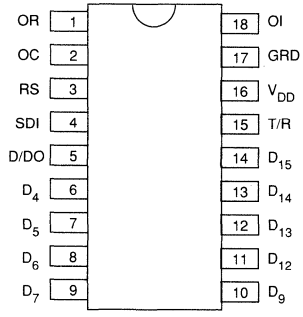
ED-9



top view

28-pin J-lead Package

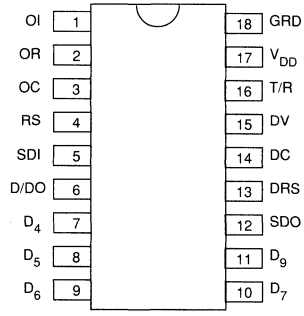
ED-9



top view

18-pin DIP

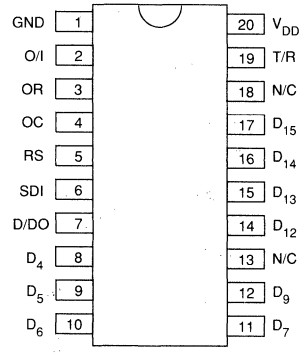
ED-5



top view

18-pin DIP

ED-9



top view

20-pin DIP/SOW 20

Programmable Encoder

Ordering Information

Device	Package	Order No.
ET13	20-Pin Plastic DIP	ET13P
ET13	20-Pin SO Surface Mount	ET13WG

Features

- ☐ High Density Transmit only ED Device
- ☐ 13 Address Bits (8192 Addresses)
- ☐ Manchester Phase Encoding
- ☐ Transmitter Compatible with ED15 Series
- ☐ Schmitt Trigger Input for excellent noise reduction
- ☐ Built-in Oscillator using non-critical RC components
- ☐ Zener Diode to regulate the power supply
- ☐ Low power, High Noise Immunity
- ☐ 20-Pin Surface Mount SO package
- ☐ Automatic Preamble Generation

Applications

- ☐ Smoke and Fire Alarm Systems
- ☐ Pocket Pagers
- ☐ Digital Locks
- ☐ Theft Alarm Systems
- ☐ Security Systems
- ☐ Digital Paging Systems
- ☐ Special Identification Code Systems
- ☐ Remote Sensor Data Acquisition Systems
- ☐ Single Channel Digital Transmission of Information

Absolute Maximum Ratings

Supply Voltage with respect to V_{SS}	6.4V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to +150°
Zener Current	100mA

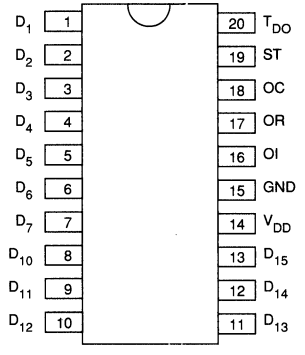
Note: All inputs except OI contain protection circuitry to prevent damage due to static charges. Care should be exercised to prevent application of voltages outside of the specification range. The OI has a special input protection circuit and special care should be taken with this input.

General Information

The ET13 is a single monolithic chip using metal gate CMOS technology for low cost, low power, high yield and high reliability. This circuit is capable of working as an encoder in applications where exclusive recognition of address codes is required. This circuit is capable of generating 8192 codes by connecting the Address Inputs to V_{DD} for a "1", or allowed to Float for a "0".

The ET13 Transmitter is a device in the Supertex ED Series of parts that is communication compatible with any other ED Series device. The ET13 provides the maximum numbers of address codes in a small package which makes them ideally suited for remote security transmitter applications where receiver operation is unnecessary. The ET13 is also available in a new 20-pin surface mount SOW package with .050-inch pitch Gullwing leads, providing high package density for remote transmitter applications.

Pin Configuration



top view

20-pin DIP/SOW 20

Electrical Characteristics

DC Characteristics (V_{DD} = 5.0 ± 5%; GRD = 0.0V; T_A = 25°C)

Symbol	Parameter	Min	Typ (Note 1)	Max	Unit	Conditions
V_{IH}	Input High Voltage	V_{DD} - 0.3		V_{DD} + 0.3	V	"1" INPUT
V_{IL}	Input Low Voltage	-0.3		0.3	V	"0" INPUT
I_{LKC}	Input Leakage Current		0.1	2.0	µA	V_{IN} = 5.0V for ST
I_{LC}	Input Load Current	2.0	6.0	20.0	µA	V_{IN} = 5.0V for pins RS, D1-D15
V_{OH}	Output High Voltage	V_{DD} - 0.3			V	V_{DD} = 4.75V, I_{LOAD} = -100µA
V_{OL}	Output Low Voltage			0.3	V	V_{DD} = 4.75V, I_{LOAD} = 100µA
I_{OH}	Output High Current (Sourcing)	-1.0	-1.5		mA	V_{OH} = V_{DD} -1.0V
I_{OL}	Output Low Current (Sinking)	1.0	3.0		mA	V_{OL} = 1.0V
V_Z	Zener Voltage	5.5	6.4	7.0	V	I_Z = 10µA (Note 2)
		6.0	6.7	7.5	V	I_Z = 10mA (Note 2)
C_{IN}	Input Capacitance			10	pF	(Note 2)
C_{ONT}	Output Capacitance			10	pF	(Note 2)
I_{DD}	Drain Current			10	µA	V_{DD} = 5.0V, all inputs = GRD all inputs floating

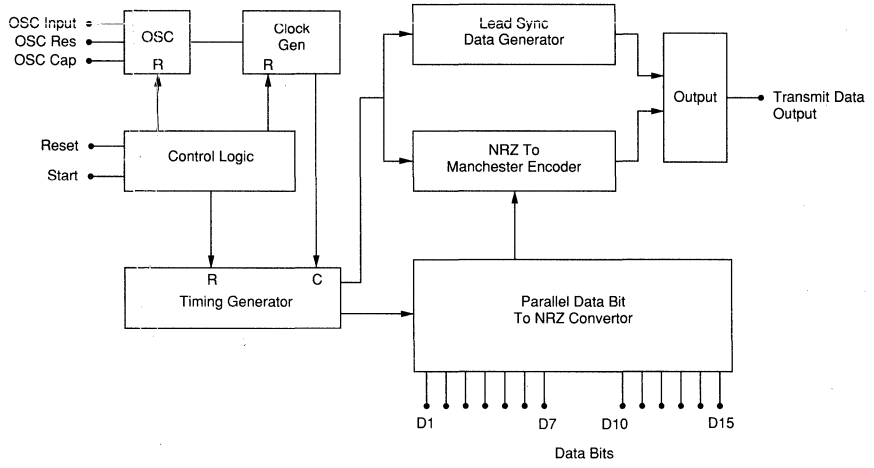
Note 1: Typical values are those values measured in a production sample at V_{CC} = 5.0V.
Note 2: This parameter is periodcally sampled and is not 100% tested.

AC Characteristics (V_{DD} = 5.0 ± 5%; T_A = 25°C)

Symbol	Parameter	Min	Typ (Note 1)	Max	Unit	Conditions
f_c	Clock Frequency	0		25	kHz	R = 150k, C = 100pF; Clock Period (t_c) = 1/f_c
t_{st}	Start Pulse Width	500			ns	
T_{DO}	TDO Delay from SDI		5		µs	
t_{WORD}	Full Cycle Word Length		130t_c		sec	

Note 1: Typical values are those values measured on a production sample at V_{CC} = 5.0V.

Block Diagram



Pin Definition

Label	Pin Name	Function
GND	Ground	Supply Potential negative side.
OI	Oscillator Input	This input is to drive the oscillator and is the tie point of the timing resistor (RT), and the timing capacitor (CT). It also is connected through a diode to an open drain P-channel device that turns on to V_{DD} when the oscillator is being reset. This input can exceed the power supplies and does during normal oscillator operation.
OR	Oscillator Resistor	Provides phase feedback to the RC timing circuit through the connected timing resistor. NOTE: This pin is driven high during oscillator reset.
OC	Oscillator Capacitor	Capacitor connection of RC timing circuit provides phased feedback from the oscillator. This pin is driven low during oscillator reset.
RS	Reset Input	This input pin may be used to override the data transmission cycle or to inhibit an SDI input. It clears the D/DO to a low state and resets the internal oscillator and data comparison circuits. This pin may be left open (No Connection) when not used, or it may be driven as an input, or an external capacitor (100pF) to V_{DD} may be added for power-up reset. The Reset function is activated when this input is connected to V_{DD}.
ST	Start	Start input is used to start the oscillator which enables the transmission of encoded word.
TDO	Transmit Data Output	This pin is the encoded sequence data output.
D1-D15	Data Bit Inputs	In the ED series devices, these inputs provide parallel input data to be sequentially transmitted. The 20-pin ET13 has some pins omitted and, hence, these data positions will have logical zeros transmitted.
V_{DD}	V_{DD}	Positive Supply Potential — This circuit contains an on-chip zener of approximately 6.7 volts across the supply terminals.

Operation

General

The ET13 mode of operation is a programmable transmitter, encoding 13 data bits into a serial Manchester code bit stream.

The ET13 contains an on-chip zener diode to clamp the power supply to around 6.7 volts. The circuit will operate from 4.0 volts to the zener voltage, but operation is recommended at 5 volts ±5%, or a regulated power supply in order to stabilize the time constants of the oscillator circuit. In order to use the on-chip zener diode, a current limiting resistor of 1K ohm or greater is required. If pull-up resistors are used for the Data Inputs, the resistors should be tied to a voltage no higher than that on Pin 14 or 6 volts, whichever is lower.

Output drivers are capable of sinking or sourcing 1.0 mA minimum at 1.0 volts V_{DS}. All inputs are gate protected to both power supplies by internal diodes. The Address Data Inputs of the ET13 each have pull down resistors to ground so that only a "1" will have to be programmed. This allows the inputs to be programmed by using SPST switches or jumpers V_{DD} only. The Start/Data Input also does not have a pull up or pull down resistor, but is applied to a Schmitt Trigger input circuit to improve noise rejection.

Function

The ET13 functions as an encoder, sampling the 13 Data Input pins digital information and encoding this parallel data in NRZ format, combining it with the clock in Manchester Code (Phase Encoded) and presenting it to the TDO pin for transmission (usually to an ED device used as the decoder circuit). The encoder will transmit the serial data each time the Start (ST) input is activated.

This encoded Data word is transmitted in two parts. The first part is preamble information which is a series of 12 "1's" and then a space indicating that the encoded Data is to follow. This preamble information is intended to be used to synchronize a phase locked-loop at the receiver or used as a setting time for receivers that have automatic gain control. The second part contains the 13 bits of Data.

Transmit and Receive Data Patterns of ED-Series Devices

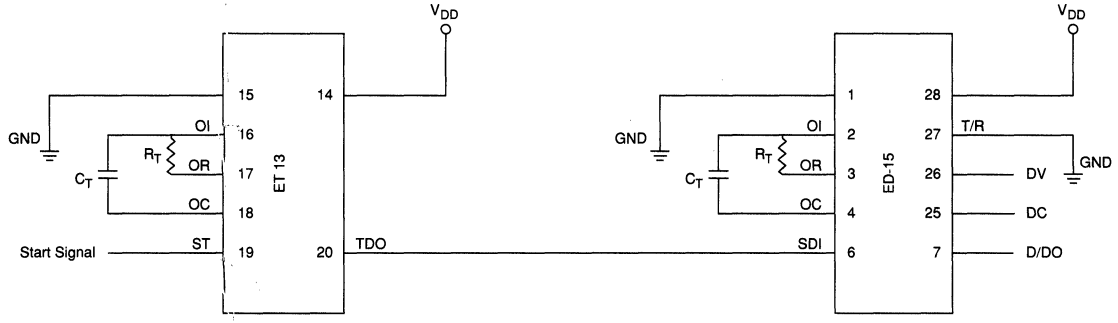
Note: Bit Sequence Code Format

x = Programmable

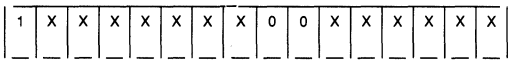
0 = Hardwired Internally Zero

1 = Hardwired Internally One

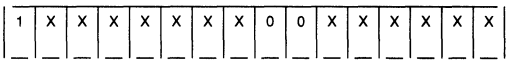
ET-13 to ET-15



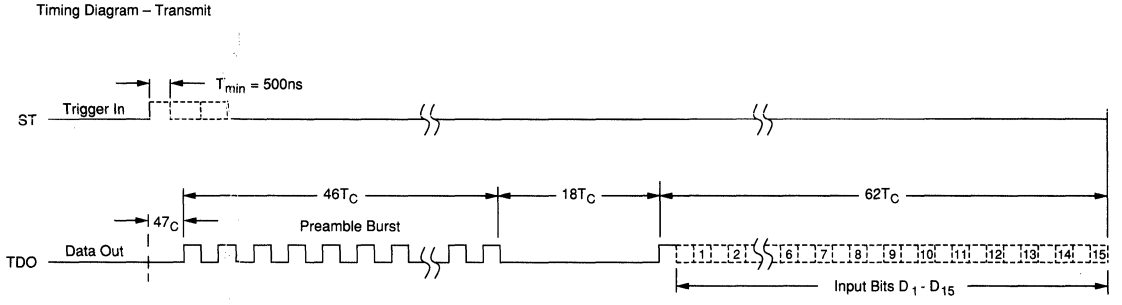
Transmitted Bit Sequence



Received Address Code



Timing Diagram – Transmit

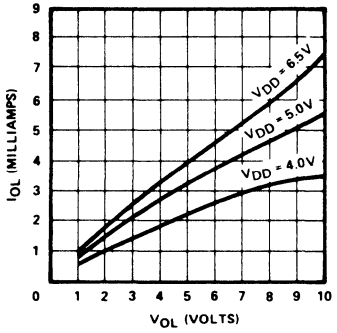


Total Time Required for Transmission of One Sequence = $130T_C$

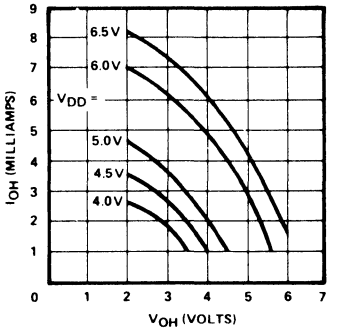
$T_C = \frac{1}{\text{CLOCK FREQUENCY}}$

Typical Performance Curves (T_A = 25°C unless otherwise noted)

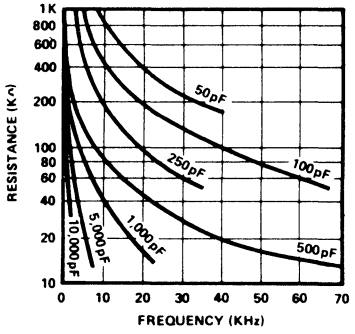
I_{OL} vs V_{DD} vs V_{OL}



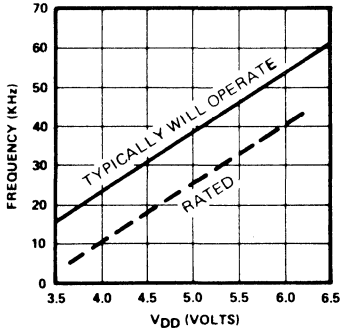
I_{OH} vs V_{DD} vs V_{OH}



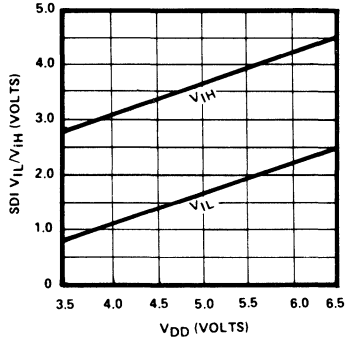
RESISTANCE vs OSCILLATOR FREQUENCY



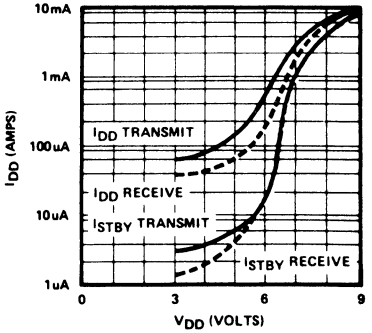
OPERATING FREQUENCY vs V_{DD}



SDI INPUT V_{IL}/V_{IH} vs V_{DD}



I_{DD} vs V_{DD}



Preliminary

Microprocessor Supervisory Circuits

Ordering Information

Device	Temperature Range	Package	Order No.
MP690	0°C to + 70°C	8 Lead Plastic Dip	MP690P
	-40°C to + 85°C	8 Lead Plastic Dip	MP690 MP
	-40°C to + 85°C	8 Lead CERDIP	MP690MD
	-55°C to + 125°C	8 Lead CERDIP	RCMP690D
	-55°C to + 125°C	8 Lead CERDIP HI-REL	RBMP 690D
MP691	0°C to + 70°C	Dice	MP691X
	0°C to + 70°C	16 Lead Plastic DIP	MP691P
	0°C to + 70°C	16 Lead Small Outline	MP691WG
	-40°C to + 85°C	16 Lead Plastic DIP	MP691MP
	-40°C to + 85°C	16 Lead CERDIP	MP691MD
	-40°C to + 85°C	16 Lead Small Outline	MP691MWG
	-55°C to + 125°C	16 Lead CERDIP	RCMP691D
	-55°C to + 125°C	16 Lead CERDIP HI-REL	RBMP691D
MP692	0°C to + 70°C	8 Lead Plastic DIP	MP692P
	-40°C to + 85°C	8 Lead Plastic DIP	MP692MP
	-40°C to + 85°C	8 Lead CERDIP	MP692MD
	-55°C to + 125°C	8 Lead CERDIP	RCMP 692D
	-55°C to + 125°C	8 Lead CERDIP HI-REL	RBMP692D
MP693	0°C to + 70°C	Dice	MP693X
	0°C to + 70°C	16 Lead Plastic DIP	MP693P
	0°C to + 70°C	16 Lead Small Outline	MP693WG
	-40°C to + 85°C	16 Lead Plastic DIP	MP693MP
	-40°C to + 85°C	16 Lead CERDIP	MP693MD
	-40°C to + 85°C	16 Lead Small Outline	MP693MWG
	-55°C to + 125°C	16 Lead CERDIP	RCMP693 D
	-55°C to + 125°C	16 Lead CERDIP HI-REL	RBMP693 D

Features

- ☐ Precision Voltage Monitor:
  4.65V in MP690 and MP691
  4.40V in MP692 and MP693
- ☐ Power OK/Reset Time Delay
- ☐ Watchdog Timer –100ms, 1.6 sec, or adjustable
- ☐ Minimum Component Count
- ☐ 1μA Standby Current
- ☐ Battery Backup Power Switching
- ☐ Onboard Gating of Chip Enable Signals
- ☐ Voltage Monitor for Power Fail or Low Battery Warning

General Description

The MP690 Family of supervisory circuits reduces the complexity and number of components required for power supply monitoring and battery control functions in microprocessor systems.

The MP690 and MP692 are supplied in 8-pin packages and provide four functions:

1) A Reset output during power-up, power down, and brownout conditions.
2) Battery backup switching for CMOS RAM, CMOS microprocessor other low power logic.
3) A Reset pulse if the optional watchdog timer has not been toggled within a specified time.
4) A 1.25V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than +5V.

The MP691 and MP693 are supplied in 16-pin packages and perform all MP690/692 functions, plus:

1) Write protection of CMOS RAM or EEPROM.
2) Adjustable reset and watchdog timeout periods.
3) Separate outputs for indicating a watchdog timeout, battery switchover, and low V_{CC}.

Absolute Maximum Ratings

Terminal Voltage (with respect to GND)	
V_{CC}	-0.3V to 6.0V
V_{BATT}	-0.3V to 6.0V
All other Inputs (Note 1)	-0.3V to (Vout +0.5V)
Input Current	
V_{CC}	200mA
V_{BATT}	50mA
GND	20mA
Output Current	
V_{OUT}	short circuit protected
All other Outputs	20mA
Rate-of-Rise, V_{BATT}, V_{CC}	100V/µs

Power Dissipation	
8 Pin Plastic DIP	
(Derate 5mW/°C above +70°C)	400mW
8 Pin CERDIP	
(Derate 8mW/°C above +85°C)	500mW
16 Pin Plastic DIP	
(Derate 7mW/°C above +70°C)	600mW
16 Pin Small Outline	
(Derate 7mW/°C above +70°C)	600mW
16 Pin CERDIP	
(Derate 10mW/°C above +85°C)	600mW
Storage Temperature Range	-65°C to +160°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

(V_{CC} = full operating range; V_{BATT} = 2.8V; T_A = 25°C, unless otherwise noted.) (Notes 1 and 2)

Parameter	Min	Typ	Max	Unit	Conditions
BATTERY BACKUP SWITCHING					
Operating Voltage Range					
MP690, 691 V_{CC}	4.75		5.5		
MP690, 691 V_{BATT}	2.0		4.25	V	
MP692, 693 V_{CC}	4.5		5.5		
MP692, 693 V_{BATT}	2.0		4.0		
V_{OUT} Output Voltage		V_{CC} - 0.1		V	I_{OUT} = 1mA
		V_{CC} - 0.25		V	I_{OUT} = 50mA
V_{OUT} in Battery Backup Mode	V_{BATT} - 0.1	V_{BATT} - 0.02		V	I_{OUT} = 100µA, V_{CC}< V_{BATT} - 0.2V
Supply Current (excludes I_{OUT})		4		mA	I_{OUT} = 1mA
		10		mA	I_{OUT} = 100mA
Supply Current in Battery Backup Mode		0.6	1	µA	V_{CC} = 0V, V_{BATT} = 2.8V
Battery Standby Charging Current			1	µA	5.5V > V_{CC} > V_{BATT} + 0.2V I_{OUT} = 1mA
			5	µA	5.5V > V_{CC} > V_{BATT} + 0.2V I_{OUT} = 100mA
Battery Switchover Threshold		70		mV	Power Up
V_{CC} - V_{BATT}		50		mA	Power Down
Battery Switchover Hysteresis		20		mV	
BATT ON Output Voltage			0.4	V	I_{SINK} = 3.2mA
BATT ON Output Short		7		mA	BATT ON = V_{OUT}
Circuit Current	0.5	1	25	µA	BATT ON = 0V
RESET AND WATCHDOG TIMER					
Reset Voltage Threshold	4.5	4.65	4.75	V	MP690, 691
	4.25	4.4	4.5	V	MP690, 691
Reset Threshold Hysteresis		40		mV	
Reset Timeout Delay	35	50	70	ms	Figure 6. OSC SEL High
Watchdog Timeout Period,	1.0	1.6	2.25	sec	Long Period
Internal Oscillator	70	100	140	ms	Short Period
Watchdog Timeout Period,	4032		4097	Clock	Long Period
External Clock	960		1025	Cycles	Short Period
Minimum WDI Input Pulse Width	200			ns	V_{IL} = 0.4, V_{IH} = 3.5V

Electrical Characteristics (continued)

(V_{CC} = full operating range; V_{BATT} = 2.8V; T_A = 25°C, unless otherwise noted.) (Notes 1 and 2)

Parameter		Min	Typ	Max	Unit	Conditions
$\overline{RESET}$ and $\overline{LOW\ LINE}$ Output Voltage				0.4	V	I_{SINK} = 1.6mA
		3.5				I_{SOURCE} = 1µA, V_{CC} = 5V
RESET and $\overline{WDO}$ Output Voltage				0.4	V	I_{SINK} = 800µA
		3.5				I_{SOURCE} = 1µA, V_{CC} = 5V
Output Short Circuit Current		1	3	25	µA	$\overline{RESET}$, RESET, $\overline{WDO}$, $\overline{LOWLINE}$
WDI Input Threshold	Logic Low			0.8	V	V_{CC} = 5V (Note 2)
	Logic High	3.0				
WDI Mid-Level Logic Voltage		1.3	1.9	2.5	V	V_{CC} = 5V (Note 2)
WDI Input current			20		µA	WDI = V_{OUT}
			-15		µA	WDI = 0V

POWER FAIL DETECTOR

PFI Input Threshold	1.15	1.25	1.35	V	
PFI Input Current		±0.01	±10	nA	
$\overline{PFO}$ Output Voltage			0.4	V	I_{SINK} = 3.2mA
			3.5	V	I_{SOURCE} = 1µA
$\overline{PFO}$ Short Circuit Source Current	1	3	25	µA	PFI = 0V, $\overline{PFO}$ = 0V

CHIP ENABLE GATING

$\overline{CE}$ IN Thresholds	0.8			V	V_{IL}
			3.0	V	V_{IH}
$\overline{CE}$ IN Pullup Current		3		µA	
$\overline{CE}$ OUT Output Voltage			0.4	V	I_{SINK} = 3.2mA
	V_{CC} -1.5			V	I_{SOURCE} = 3.0mA
$\overline{CE}$ Propagation Delay			50	ns	

OSCILLATOR

OSC IN Input Current		±2		µA	
OSC SEL Input Pullup Current		5		µA	
OSC IN Frequency Range	0		250	kHz	OSC SEL = 0V
OSC IN Frequency with External Capacitor		2		kHz	OSC SEL = 0V, C_{OSC} = 47pF

Note 1: The input voltage limits on PFI and WDI may be exceeded provided the input current is limited to less than 10mA.

Note 2: WDI is guaranteed to be in the mid-level (inactive) state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 38% of V_{CC} with an impedance of approximately 125 kilohms.

Caution - Battery Backup Function

Initial insertion of the back-up battery may cause excessive battery drain (10– 20mA) on early production parts. This condition will not damage the IC, but could prematurely discharge the battery.

CONDITIONS: Two conditions must be present simultaneously for the problem to occur: a voltage rate-of-rise greater that 0.25V/µs at the V_{BATT} terminal (such as can occur when battery is first inserted into the system), and V_{CC} connected to ground with a resistance of less than 10 kilohms.

PREVENTION: Either limit the rate-of-rise of V_{BATT} by inserting a 100 ohm series resistor between the battery and the V_{BATT} terminal and connect a 0.22µF or greater capacitor between V_{BATT} and ground, or insert the battery while V_{CC} is applied to the IC.

CORRECTION: In some instances, it may not be possible to take either of the preventative measures described above. Normal operation can be restored simply by raising V_{CC} above V_{BATT} (i.e., by applying power). The high current mode will not recur, even if V_{CC} subsequently returns to ground.

Pin Description

Name	Pin		Function
	MP690/692	MP 691/693	
V_{CC}	2	3	The +5V input.
V_{BATT}	8	1	Backup battery input. Connect to Ground if a backup battery is not used.
V_{OUT}	1	2	The higher of V_{CC} or V_{BATT} is internally switched to V_{OUT}. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used.
GND	3	4	0V ground reference for all signals.
$\overline{RESET}$	7	15	$\overline{RESET}$ goes low whenever V_{CC} falls below either the reset voltage threshold or the V_{BATT} input voltage. The reset threshold is typically 4.65V for the MP 690 and MP691, and 4.4V for the MP692 and MP693. $\overline{RESET}$ remains low for 50ms after V_{CC} returns to 5V. $\overline{RESET}$ also goes low for 50ms if the Watchdog Timer is enabled but not serviced within its timeout period. The $\overline{RESET}$ pulse width can be adjusted as shown in Table 1.
WDI	6	11	The watchdog input, WDI, is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{RESET}$ pulses low and $\overline{WDO}$ goes low. The Watchdog Timer is disabled when WDI is left floating or is driven to mid-supply. The timer resets with each transition at the Watchdog Timer Input.
PFI	4	9	PFI is the non-inverting input to the Power Fail Comparator. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{OUT} when not used. See Figure 1.
$\overline{PFO}$	5	10	$\overline{PFO}$ is the output of the Power Fail Comparator. It goes low when PFI is less than 1.25V. The comparator is turned off and $\overline{PFO}$ goes low when V_{CC} is below V_{BATT}.
$\overline{CE}$ IN		13	The input to the $\overline{CE}$ gating circuit. Connect to GND or V_{OUT} if not used.
$\overline{CE}$ OUT		12	$\overline{CE}$ OUT goes low only when $\overline{CE}$ IN is low and V_{CC} is above the reset threshold (4.65V for MP691, 4.4V for MP693). See Figure 6.
BATT ON		5	BATT ON goes low when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 7mA and can directly drive the base of an external PNP transistor to increase the output current above the 100mA rating of V_{OUT}.
$\overline{LOW\ LINE}$		6	$\overline{LOW\ LINE}$ goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold. See Figure 6, Reset Timing.
RESET		16	RESET is an active high output. It is the inverse of $\overline{RESET}$.
OSC SEL		8	When OSC SEL is unconnected or driven high, the internal oscillator sets the reset time delay and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3µA internal pullup. See Table 1.
OSC IN		7	OSC IN sets the Reset delay timing and Watchdog timeout period when OSC SEL floats or is driven high. The timing can also be adjusted by connecting an external capacitor to this pin. See Figure 8. When OSC SEL is low, OSC IN selects between fast and slow Watchdog timeout periods.
$\overline{WDO}$		14	The Watchdog Output, $\overline{WDO}$, goes low if WDI remains either high or low for longer than the Watchdog timeout period. $\overline{WDO}$ is set high by the next transition at WDI. If WDI is unconnected or at mid-supply, $\overline{WDO}$ remains high. $\overline{WDO}$ also goes high when $\overline{LOW\ LINE}$ goes low.

Typical Applications

MP691 and MP693

A typical connection for the MP 691/693 is shown in Figure 1. CMOS RAM is powered from V_{OUT}. V_{OUT} is internally connected to V_{CC} when 5V power is present, or to V_{BATT} when V_{CC} is less than the battery voltage. V_{OUT} can supply 100mA from V_{CC}, But if more current is required, an external PNP transistor can be added. When V_{CC} is higher than V_{BATT}, the BATT ON output goes low, providing 7mA of base drive for the external transistor. When V_{CC} is lower than V_{BATT}, an internal 500Ω MOSFET connects the backup battery to V_{OUT}. The quiescent current in the battery backup mode is 1µA maximum when V_{CC} is between 0V and V_{BATT} - 700mV.

Reset Output

A voltage detector monitors V_{CC} and generates a $\overline{\text{RESET}}$ output to hold the microprocessor's Reset line low when V_{CC} is below 4.65V (4.4V for MP693). An internal monostable holds $\overline{\text{RESET}}$ low for 50ms after V_{CC} rises above 4.65V (4.4V for MP693). This prevents repeated toggling of $\overline{\text{RESET}}$ even if the 5V power drops out and recovers with each power line cycle.

The crystal oscillator normally used to generate the clock for microprocessors takes several milliseconds to start. Since most microprocessors need several clock cycles to reset, $\overline{\text{RESET}}$ must be held low until the microprocessor clock oscillator has started. The MP690 Family power-up $\overline{\text{RESET}}$ pulse lasts 50ms to allow for this oscillator start-up time. The manual reset switch and the 0.1µF capacitor connected to the reset bus can be omitted if manual reset is not needed. An inverted, active high, RESET output is also supplied.

Power Fail Detector

The MP691/93 issues a non-maskable interrupt (NMI) to the microprocessor when a power failure occurs. The +5V power line is monitored via two external resistors connected to the Power Fail Input (PFI). When the voltage at PFI falls below 1.25V, the Power Fail Output ($\overline{\text{PFO}}$) drives the processor's NMI input low. If a Power Fail threshold of 4.8V is chosen, the microprocessor will have the time when V_{CC} falls from 4.8V to 4.65V to save data into RAM. An earlier power fail warning can be generated if the unregulated DC input of the 5V regulator is available for monitoring.

RAM Write Protection

The MP691/93 CE OUT line drives the $\overline{\text{Chip Select}}$ inputs of the CMOS RAM, $\overline{\text{CE}}$ OUT follows $\overline{\text{CE}}$ IN as long as V_{CC} is above the 4.65V (4.4V for MP693) reset threshold. If V_{CC} falls below the reset threshold, $\overline{\text{CE}}$ OUT goes high, independent of the logic level at $\overline{\text{CE}}$ IN. This prevents the microprocessor from writing erroneous data into RAM during power-up, power-down, brownouts, and momentary power interruptions. The $\overline{\text{LOW LINE}}$ output goes low when V_{CC} falls below 4.65V (4.4V for MP693).

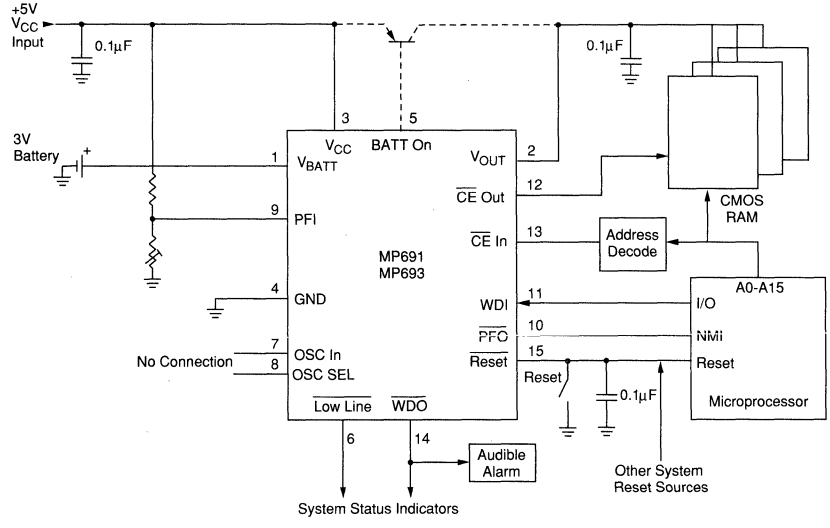


Figure 1. MFP691/693 Typical Application

Watchdog Timer

The microprocessor drives the WATCHDOG INPUT (WDI) with an I/O line. When OSC SEL are connected, the microprocessor must toggle the WDI pin once every 1.6 seconds to verify proper software execution. If a hardware or software failure occurs such that WDI is not toggled, the MP691/93 will issue a 50ms $\overline{\text{RESET}}$ pulse after 1.6 seconds. This typically restarts the microprocessor's power-up routine. A new $\overline{\text{RESET}}$ pulse is issued every 1.6 seconds until WDI is again strobed.

The WATCHDOG OUTPUT ($\overline{\text{WDO}}$) goes low if the watchdog timer is not serviced within its timeout period. Once $\overline{\text{WDO}}$ goes low it remains low until a transition occurs at WDI. The watchdog timer feature can be disabled by leaving WDI unconnected. OSC IN and OSC SEL also allow other watchdog timing options, as shown in Table 1 and Figure 8.

MP690 and MP692

The 8-pin MP690 and MP 692 have most of the features of the MP691 and MP693. Figure 2 shows the MP690/692 in a typical application. Operation is much the same as with the MP691/693 (Figure 1) but in this case the Power Fail Input (PFI) monitors the unregulated input to the 7805 regulator. The MP690 $\overline{\text{RESET}}$ output goes low when V_{CC} falls below 4.65V. The $\overline{\text{RESET}}$ output of the MP692 goes low when V_{CC} drops below 4.4V.

The current consumption of the battery-backed-up power bus must be less than 100mA. The MP690/692 does not have a BATT ON output to drive an external transistor. The MP690/92 also does not include chip enable gating circuitry that is available on the MP691/93. In many systems though, $\overline{\text{CE}}$ gating is not needed since a low input to the microprocessor $\overline{\text{RESET}}$ line prevents the processor from writing to RAM during power-up and power-down transients.

The MP690/92 watchdog timer has a fixed 1.6 second timeout period. If WDI remains either low or high for more than 1.6 seconds., a $\overline{\text{RESET}}$ pulse is sent to the microprocessor. The watchdog timer is disable, if WDI is left floating.

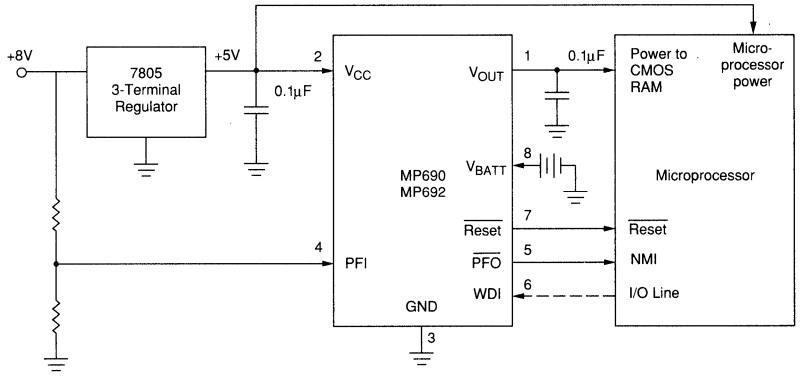


Figure 2. MP690/692 Typical Application

Detailed Description

Battery-Switchover and V_{OUT}

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50mV greater than V_{BATT} as V_{CC} falls, and when V_{CC} is 70mV more than V_{BATT} as V_{CC} rises (see Figure 4). The switchover comparator has 20mV of hystersis to prevent repeated, rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

When V_{CC} is higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} via a low saturation PNP transistor. V_{OUT} has 100mA output current capability and thermal shutdown short circuit protection. Use an external PNP pass transistor in parallel with the internal transistor if the output current requirement at V_{OUT} exceeds 100mA or if a lower V_{CC}-V_{OUT} voltage differential is desired. The BATT ON output (MP691/693 only) can directly drive the base of the external transistor.

It should be noted that the MP690/91/92/93 need only supply the average current drawn by the CMOS RAM if there is adequate filtering. Many RAM data sheets specify a 75mA maximum supply current, but this peak current spike lasts only 100ns. A 0.1µF bypass capacitor at V_{OUT} supplies the high instantaneous current, while V_{OUT} need only supply the average load current, which is much less. A capacitance of 0.1µF or greater must be connected to the V_{OUT} terminal to ensure stability.

A 500 ohm MOSFET connects the V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. When V_{CC} equals V_{BATT} the supply current is typically 12µA. When V_{CC} is between 0V and (V_{BATT} -700mV) the typical supply current is only 600nA typical, 1µA maximum.

The MP690/691 operates with battery voltages from 2.0V to 4.25V while the MP692/693 operates with battery voltages from 2.0V to 4.0V. High value capacitors, either standard electrolytic or the farad-size double layer capacitors, can also be used for short-term

memory backup. The charging resistor for both capacitors and rechargeable batteries should be connected to V_{OUT} since this eliminates the discharge path that exists if the resistor is connected to V_{CC}.

A small charging current of typically 10nA (5µ max) flows out of the V_{BATT} terminal. This current varies with the amount of current that is drawn from V_{OUT} but its polarity is such that the backup battery is always slightly charged, and is never discharged while V_{CC} is in its operating voltage range. This extends the shelf life of the backup battery by compensating for its self-discharging current. Also note that this current poses no problem when lithium batteries are used for backup since the maximum charging current (5µA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, connect V_{BATT} to GND and connect V_{OUT} to V_{CC}. Table 2 shows the state of the inputs and output in the low power battery backup mode.

Reset Output

$\overline{RESET}$ is an active low output which goes low whenever V_{CC} falls below 4.5V (MP690/691) or 4.25V (MP692/693). It will remain low until V_{CC} rises above 4.75V (MP 690/691) or 4.5V (MP692/693) for 50 milliseconds. (See Figures 5 and 6.)

The guaranteed minimum and maximum thresholds of the MP 690/691 are 4.5V and 4.75V, while the guaranteed thresholds of the MP692/693 are 4.25V and 4.5V. The MP690/691 is compatible with 5V supplies with a +10%, -5% tolerance while the MP692/693 is compatible with 5V ±10% supplies. The reset threshold comparator has approximately 50mV of hysteresis, with a nominal threshold of 4.65V in the MP690/691, and 4.4V in the MP692/693.

The response time of the reset voltage comparator is about 100µs. V_{CC} should be bypassed to ensure that glitches do not activate the $\overline{RESET}$ output.

$\overline{RESET}$ also goes low if the Watchdog Timer is enabled and WDI remains either high or low longer than the watchdog timeout period. $\overline{RESET}$ has an internal 3µA pullup, and can either connect to an open collector Reset bus or directly drive a CMOS gate without an external pullup resistor.

$\overline{CE}$ Gating and RAM Write Protection

The MP691 and MP693 use two pins to control the $\overline{Chip\ Enable}$ or $\overline{Write}$ inputs of CMOS RAMs. When V_{CC} is +5V, $\overline{CE}$ OUT is a buffered replica of $\overline{CE}$ IN, with a 50ns propagation delay. If V_{CC} input falls below 4.65V (4.5V min, 4.75V max) an internal gate forces $\overline{CE}$ OUT high, independent of $\overline{CE}$ IN. The MP693 $\overline{CE}$ OUT goes high whenever V_{CC} is below 4.4V (4.25V min, 4.5V max). The $\overline{CE}$ output of both devices is also forced high when V_{CC} is less than V_{BATT}. (See Figure 5.)

$\overline{CE}$ OUT typically drives the $\overline{CE}$, $\overline{CS}$, or $\overline{Write}$ input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level. Similar protection of EEPROMs can be achieved by using the $\overline{CE}$ OUT to drive the Store or Write inputs of an EEPROM, EAROM, or NOVRAM.

If the 50ns typical propagation delay of $\overline{CE}$ OUT is too long, connect $\overline{CE}$ IN to GND and use the resulting second alternative is to AND the $\overline{LOW\ LINE}$ output with the $\overline{CE}$ or $\overline{WR}$ signal. An external logic gate and the $\overline{RESET}$ output of the MAX690/692 can also be used for CMOS RAM write protection.

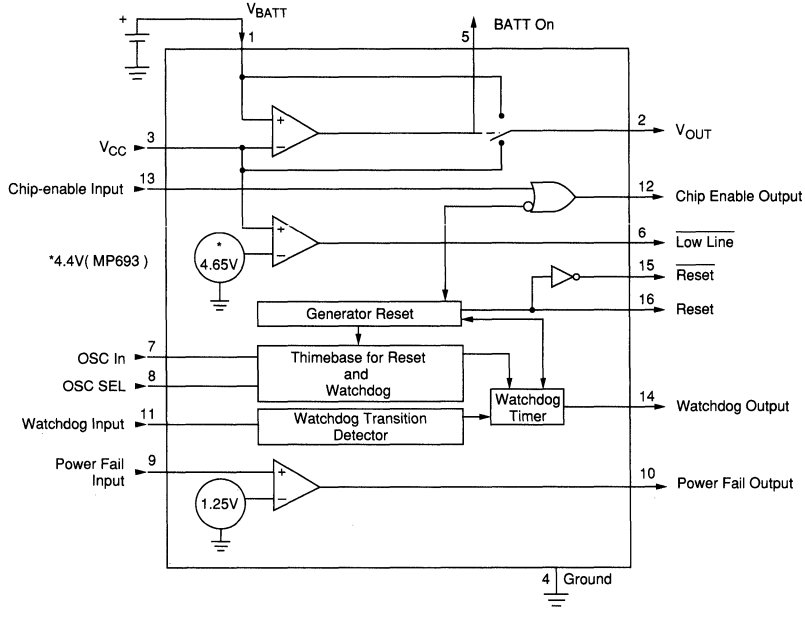


Figure 3. MP691/693 Block Diagram

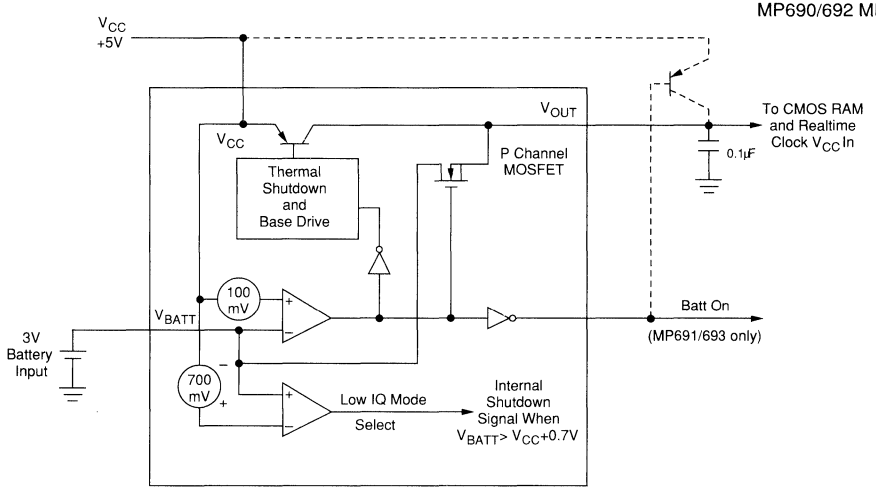


Figure 4. Battery Switchover Block Diagram

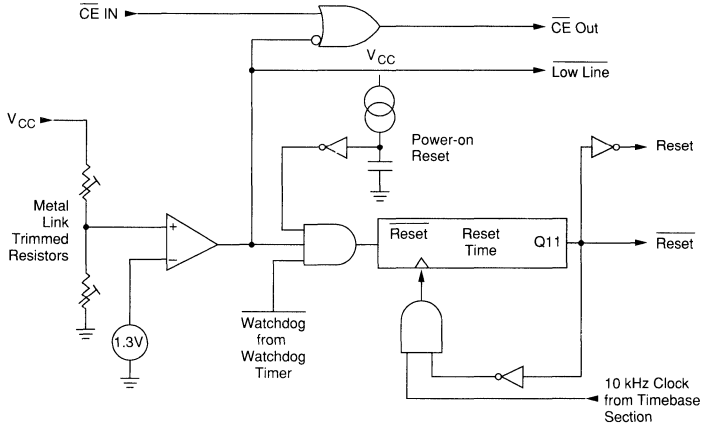


Figure 5. Reset Block Diagram

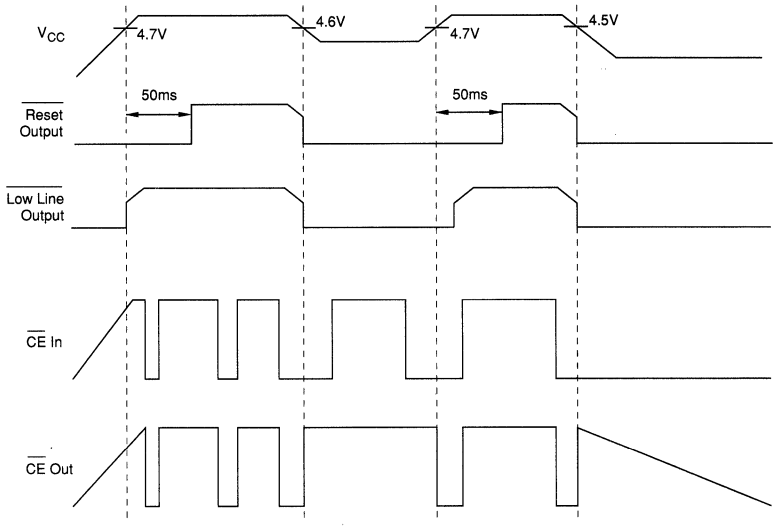


Figure 6. MP691 Reset Timing

1.25V Comparator and Power Fail Warning

The Power Fail Input (PFI) is compared to an internal 1.25V reference. The Power Fail Output ($\overline{PFO}$) goes low when the voltage at PFI is less than 1.25V. Typically PFI is driven by an external voltage divider which senses either the unregulated DC input to the system's 5V regulator or the regulated 5V output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.25V several milliseconds before the +5V supply falls below 4.75V. $\overline{PFO}$ is normally used to interrupt the microprocessor so that data can be stored in RAM before V_{CC} falls below 4.75V and the $\overline{RESET}$ output goes low (4.5V for MP692/93).

The Power Fail Detector can also monitor the backup battery to warn of a low battery condition. To conserve battery power, the Power Fail Detector comparator is turned off and $\overline{PFO}$ is forced low when V_{CC} is lower than the V_{BATT} input voltage.

Watchdog Timer and Oscillator

The watchdog circuit monitors the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within the selected timeout period, a 50 millisecond $\overline{RESET}$ pulse is generated. Since many systems cannot service the watchdog timer immediately after a reset, the MP691/693 has a longer timeout period after a reset is issued. The normal timeout period becomes effective following the first transition of WDI after $\overline{RESET}$ has gone high. The watchdog timer is restarted at the end of Reset, whether the Reset was caused by lack of activity on WDI or by V_{CC} falling below the reset threshold. If WDI remains either high or low, reset pulses will be issued every 1.6 seconds. The watchdog monitor can be deactivated by floating the Watchdog Input (WDI).

The Watchdog Output ($\overline{WDO}$, MP691/693 only) goes low if the watchdog timer "times out", and it remains low until set high by the next transition on the watchdog input. $\overline{WDO}$ is also set high when V_{CC} goes below the reset threshold.

The watchdog timeout period is fixed at 1.6 seconds and the rest pulse width is fixed at 50ms on the 8-pin MP690 and MP692. The MP691 and MP693 allow these times to be adjusted per Table 1. Figure 8 show various oscillator configurations.

The internal oscillator is enabled when OSC SEL is high or floating. In this mode, OSC IN selects between the 1.6 second and 100ms watchdog timeout periods. In either case, immediately after a reset the timeout period is 1.6 seconds. This gives the microprocessor time to reinitialize the system. If OSC IN is low, then the 100ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the I/O port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period to 70ms.

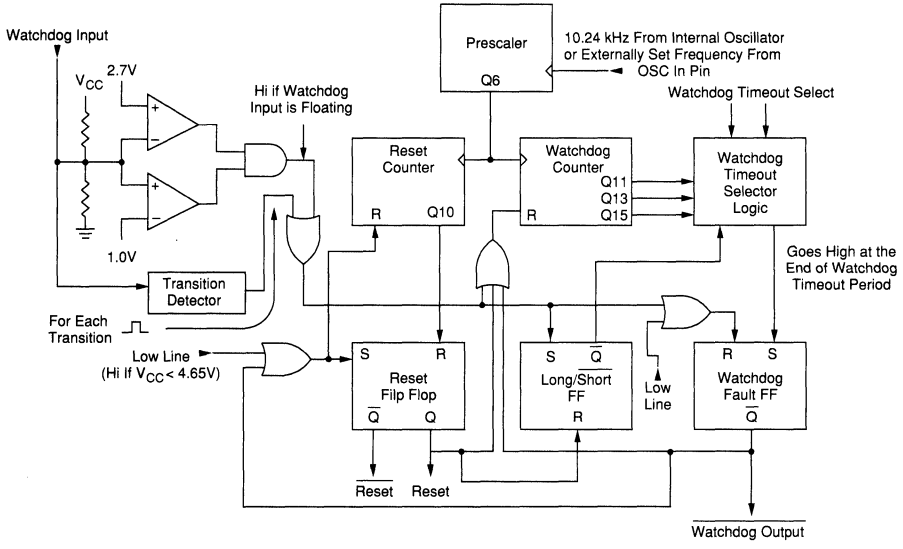


Figure 7. Watchdog Timer Block Diagram

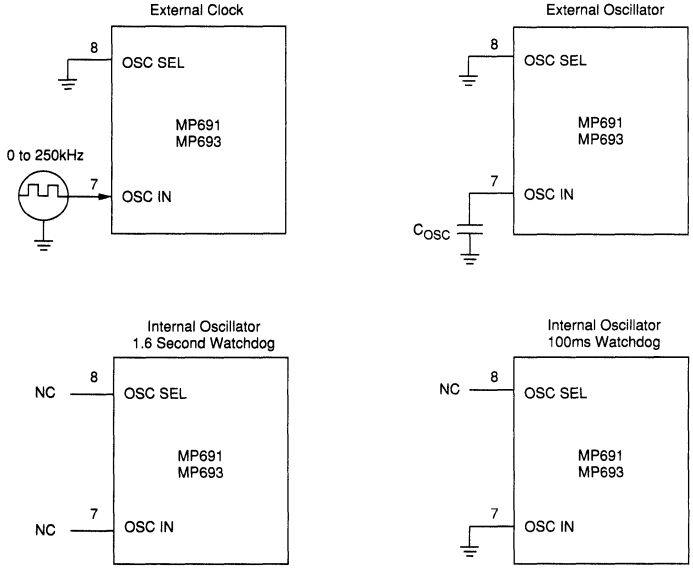


Figure 8. Oscillator Circuits

Table 1. MP691 and MP693 Reset Pulse Width and Watchdog Timeout Selections

OSC SEL	OSC IN	Watchdog Timeout Period		Reset Timeout Period
		Normal	Immediately After Reset	
Low	External Clock Input	1024 clks	4096 clks	512 clks
Low	External Capacitor	$\frac{400ms}{47pF} \times C$	$\frac{1.6\ sec}{47pF} \times C$	$\frac{200ms}{47pF} \times C$
High/Floating	Low	100ms	1.6 sec	50ms
High/Floating	High / Floating	1.6 sec	1.6 sec	50ms

Note 1. The MP690 watchdog timeout period is fixed at 1.6 seconds nominal; the MP690 Reset pulse width is fixed at 50ms nominal.

Note 2. When the MP691 OSC SEL pin is low, OSC IN can be driven by an external clock signal, or an external capacitor can be connected between OSC IN and GND. The nominal internal oscillator frequency is 10.24kHz.
The nominal oscillator frequency with external capacitor is $F_{OSC}\ (Hz) = \frac{1.75 \times 10^7}{C_{OSC}\ (Farads)}$

Note 3. See Electrical Specifications Table for minimum and maximum timing values.

Application Hints

Other uses of the Power Fail Detector

In Figure 9 the Power Fail Detector is used to initiate a system reset when V_{CC} falls to 4.85V. Since the threshold of the Power Fail Detector is not as accurate as the onboard Reset voltage detector, a trimput must be used to adjust the voltage detection threshold. Both the PFO and $\overline{RESET}$ outputs have high sink current capability and only 10µA of source current drive. This allows the two outputs to be connected directly to each other in a "wired or" fashion.

The overvoltage detector circuit in Figure 10 resets the microprocessor whenever the nominal 5V V_{CC} is above 5.5V. The battery monitor circuit (Figure 11) shows the status of the memory backup battery. If desired, the $\overline{CE}$ OUT can be used to apply a test load to the battery. Since $\overline{CE}$ OUT is forced high during the battery backup mode, the test load will not be applied to the battery while it is in use, even if the microprocessor is not powered.

Adding Hysteresis to the Power Fail Comparator

Since the power fail comparator circuit is non-inverting, hysteresis can be added by connecting a resistor between the PFO output and the PFI input as shown in Figure 12. When PFO is low, resistor R3 sinks current from the summing junction at the PFI pin. When PFO is high, the series combination of R3 and R4 source current into the PFI summing junction.

Alternate Watchdog Input Drive Circuits

The Watchdog feature can be enabled and disabled under program control by driving WDI with a 3-state buffer (Figure 13). The drawback to this circuit is that a software fault may erroneously 3-state the buffer, thereby preventing the MP690 from detecting that the microprocessor is no longer working. In most cases a better method is to extend the watchdog period rather than disabling the watchdog. See Figure 14. When the control input is high, the OSC SEL pin is low and the watchdog timeout is set by the external capacitor. A 0.01µF capacitor sets a watchdog timeout delay of 100 seconds. When the control input is low, the OSC SEL pin is driven high, selecting the internal oscillator. The 100ms or the 1.6 sec period is chosen, depending on which diode in Figure 14 is used.

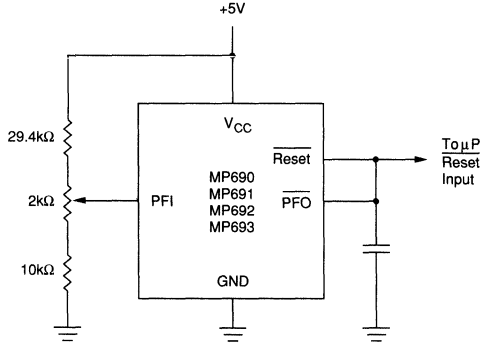


Figure 9. Externally Adjustable V_{CC} Reset Threshold

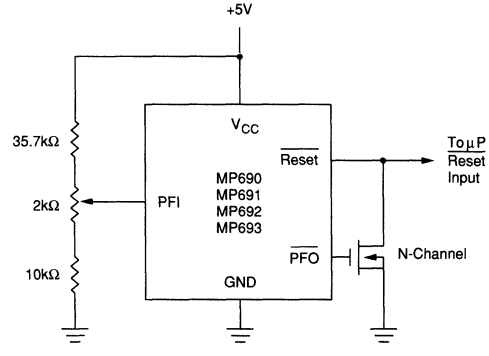


Figure 10. Reset on Overvoltage or Undervoltage

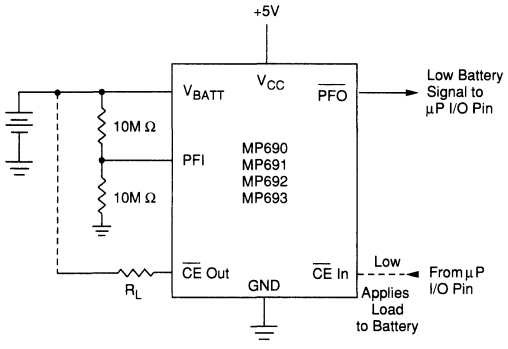


Figure 11. Backup Battery Monitor with Optional Test Load

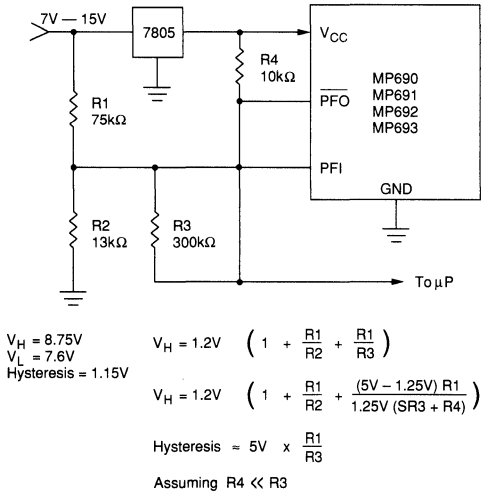


Figure 12. Adding Hysteresis to the Power Fail Voltage Comparator

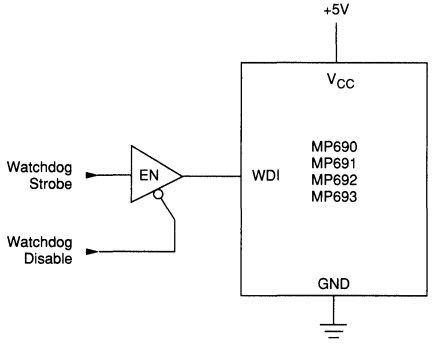


Figure 13. Disabling the Watchdog under Program Control

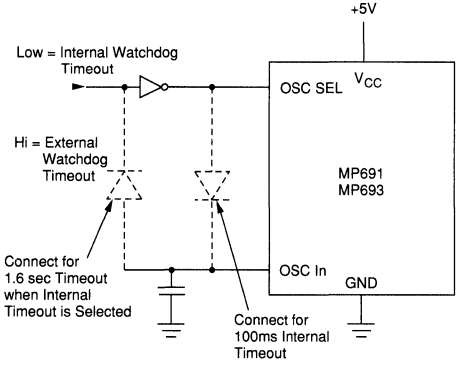
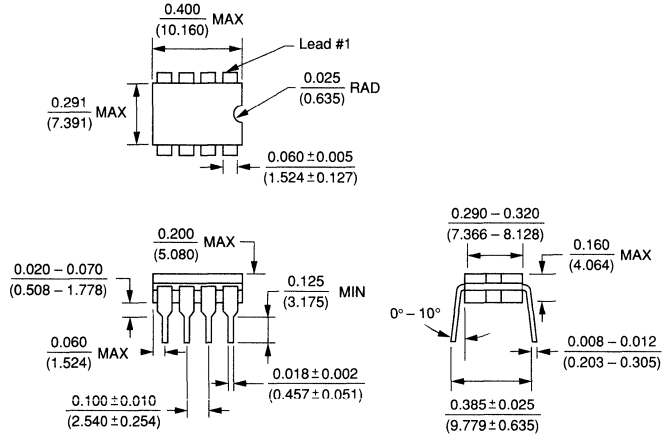


Figure 14. Selecting Internal or External Watchdog Timeout

Table 2. Input and Output Status In Battery Backup Mode

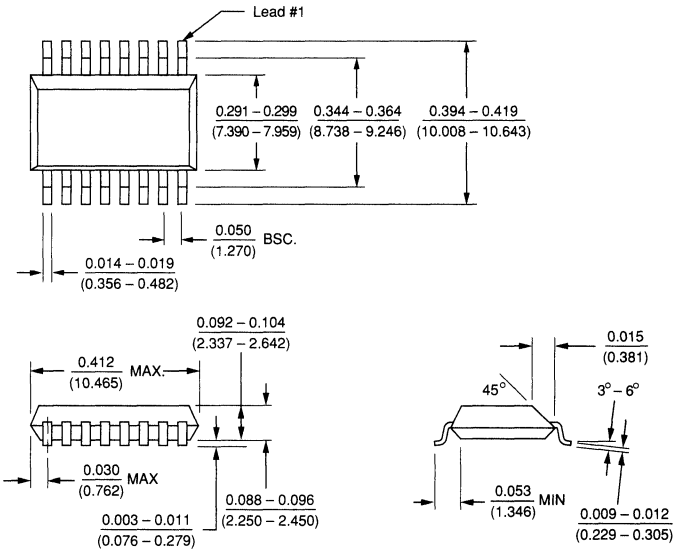
V_{BATT}, V_{OUT}	V_{BATT} is connected to V_{OUT} via internal MOSFET.
$\overline{RESET}$	Logic low.
RESET	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic low.
BATT ON	Logic high.
WDI	WDI is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{WDO}$	Logic high.
PFI	The Power Fail Comparator is turned off and the Power Fail Input voltage has no effect on the Power Fail Output.
$\overline{PFO}$	Logic low.
$\overline{CE}$ IN	$\overline{CE}$ IN has a 2µA input pullup current source. Float or drive high to minimize supply current.
$\overline{CE}$ OUT	Logic high.
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.
V_{CC}	Approximately 12µA is drawn from the V_{BATT} input when V_{CC} is between V_{BATT} + 100mV and V_{BATT} - 700mV. The supply current is 1µA maximum when V_{CC} is less than V_{BATT} - 700mV.

Package Information



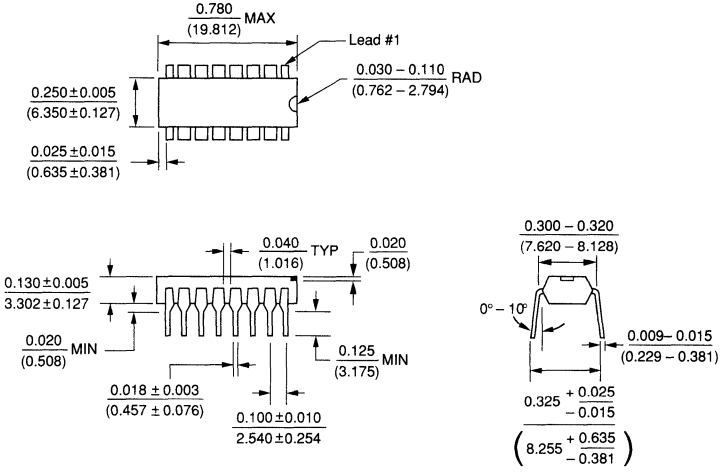
8 LEAD CERDIP (D)

θ_{ja} = 125°C/W
θ_{jc} = 55°C/W



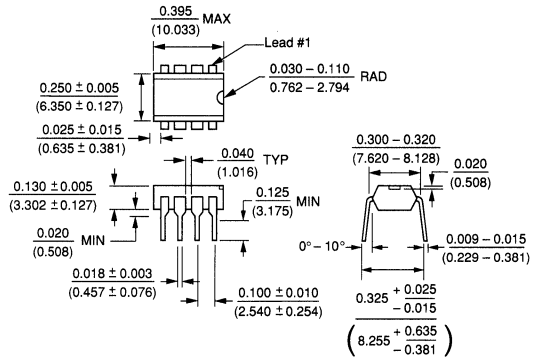
16 Lead Small Outline, Wide (WG)

θ_{ja} = 105° C/W
θ_{jc} = 60° C/W



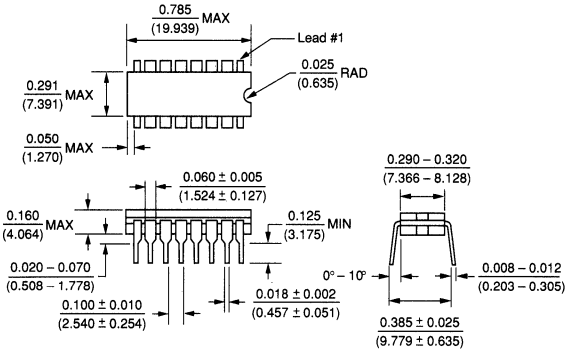
16 Lead Plastic DIP (P)

θ_{ja} = 100° C/W
θ_{jc} = 60°C/W



8 LEAD PLASTIC DIP (P)

θ_{ja} = 120° C/W
θ_{jc} = 70° C/W

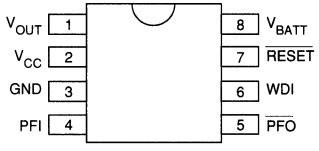


16 LEAD CERDIP (D)

θ_{ja} = 100° C/W
θ_{jc} = 50° C/W

Pin Configuration

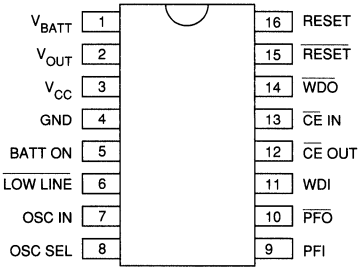
MP690 & MP692



top view

8-pin DIP

MP691 & MP693



top view

16-pin DIP

CMOS Photo-Electric Smoke Detector Integrated Circuit

Ordering Information

Device	Package	Order No.
SD2	16-Pin Plastic	SD2P

Features

- ☐ 6μA – Average Standby Current
- ☐ Minimum Cost of External Components
- ☐ 1mV Sensitivity
- ☐ 8 to 1 Increase of Sample Rate when smoke detected
- ☐ Improved Noise Rejection by multiple sampling
- ☐ Automatic LED Supervisor Alarm
- ☐ Multi-Station Input/Output Capability
- ☐ Horn Modulation Mode Control
- ☐ Piezoelectric Horn Driver
- ☐ Smoke Sensitivity Adjustable by single resistor
- ☐ Self-contained Oscillator requires only a resistor

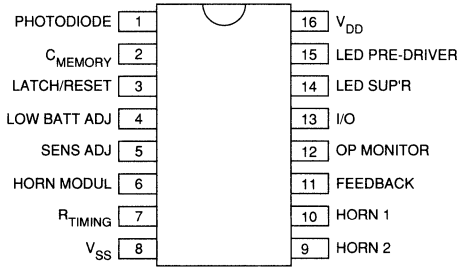
Absolute Maximum Ratings

Supply Voltage	-0.5V to +15.0V
Input Voltage, All inputs	-0.5 to VDD +0.5V
Input Current, Any Input	±10mA
Storage Temperature Range	-40°C to +100°C
Operating Free Air Temperature Range	0°C to +55°C
Power Dissipation (Package)	300mW
Continuous Output Drive Current	25mA
Lead Temperature (Soldering, 10 sec)	300°C
Relative Humidity	90%

General Description

This low power CMOS circuit is intended for use in a pulsed LED/silicon cell smoke detector system. It is designed for use in low power, battery operated, consumer applications with a minimum of external components. This device meets UL217 requirements and is available in a 16-pin plastic DIP.

Pin Configuration



top view

16-pin DIP

Electrical Characteristics

(w/R-(7) = 22 Meg Ω then f_{OSC} = 485 Hz; T_A = 25° C;V_{DD} = 9V, unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IN}	Photodiode Input Leakage Current		0.01	±1.0	nA	
V_{PD}	Photodiode Input Signal Sensitivity	0.5	0.8	1.1	mV	C_{mem} = .05µF C_{input} = 5pF τ_{LED} = 100µ sec
V_{BTH}	Low Battery Threshold Voltage	7.3	7.7	8.2	V	R(4) = ∞
	Horn Modulation Frequency		8		Hz	PIN 6 to V_{DD} R(7) = 22 meg Ω Smoke Detected
	Horn Modulation Duty Cycle		62.5		%	
τ_{TBL}	Low Battery/LED Supervisor Trouble Alarm Pulse Width		17		mSec	@ f_{OSC} = 485 Hz R(7) = 22 Meg Ω
T_{TBL}	Low Battery/LED Supervisor Alarm Period		35		sec	@ f_{OSC} = 485 Hz R(7) = 22 Meg Ω
I_{OUT}	Horn Output Current	± 25			mA	V_O = IV Sink V_O = 8V Source
V_{IN}	Feedback Input Voltage Range	V_{SS} - 15		V_{DD} + 15	V	Typical Min and Max. Not 100% tested
I_{OM}	Operation Monitor Output Current, Source	-2.5	-4.5		mA	V_{OM} = 2.0V
$I_{I/O}$	I/O Output Source Current	-4.0	-10.0		mA	$V_{I/O}$ = V_{DD} -1.0
$V_{I/O}$	Remote Alarm Trigger Voltage	0.6 V_{DD}			V	Sink Current 20mA typical at V_{DD} = 4.5V
V_{IH-ON}	LED Supervisor, upper Threshold Range	V_{DD} - 0.8		V_{DD} - 0.2	V	
V_{I-OFF}	LED Supervisor, Safe Region	V_{DD} - 2.5		V_{DD} - 0.8		
V_{IL-ON}	LED Supervisor, lower Threshold Range	V_{DD} - 4.0		V_{DD} - 2.5		
I_{LED}	LED Output Source Current	-10	-20		mA	V_{LED} = 5V
T_{LED}	Photodiode Sample Pulse Period (Smoke Detected)		1.0		sec	f_{OSC} = 485 Hz
T_{LED}	Photodiode Sample Pulse Period (Smoke Detected)		8.0		sec	f_{OSC} = 485 Hz R(7) = 22 meg Ω
V_{DD}	Supply Voltage	7.0	9.0	10.0	V	
I_{DD}	Average Standby Supply Current		6.0	10.0	µA	R(7) = 22 Meg Ω V_{DD} = 9.0, Non-Alarm Mode

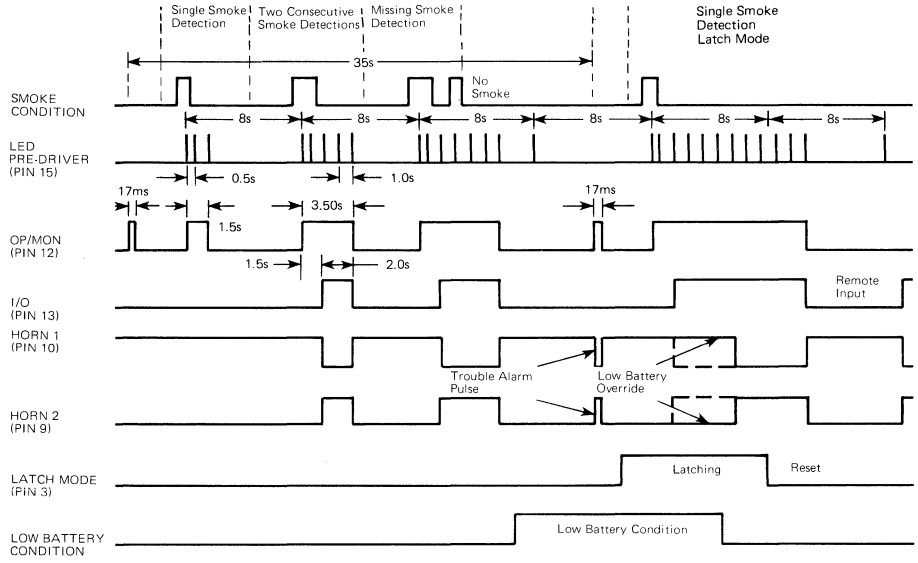
Pin Definition

Pin	Name	Function
1	Photodiode Input	Connect the cathode of a VTS-4085S, or equivalent, to pin 1. Connect the anode to V_{DD}. The typical allowed signal range is from V_{DD} to V_{DD} - 1.0V.
2	Memory Capacitor Input	The capacitor may range from 0.01µF to 0.05µF and should have low leakage. The detector sensitivity increases with increasing capacitance.
3	Latch/Reset Input	When connected to V_{DD}, the detector will latch on at the first detection of smoke alarm. When connected to V_{SS}, the alarm will not latch on detection of smoke and the low battery condition will not override the smoke alarm condition. Reset after latching is accomplished by momentarily connecting this pin to VSS until the horn silences. The Latch/Reset Input only affects the local smoke alarm response.
4	Low Battery Threshold Adjustment	The nominal threshold of the battery alarm is 7.7 volts. The alarm can be raised by connecting a resistor to ground, and lowered by connecting a resistor to V_{DD}.
5	Smoke Sensitivity Adjustment	A resistor or potentiometer to ground is used to adjust the duration of the LED pulse and thereby the Smoke Sensitivity. Pulse duration is proportional to the resistor value and varies approximately 100µsec per megohm.
6	Horn Modulation Control Input	When connected to V_{DD}, the Horn will pulse ON and OFF at approximately 8 Hz, with the ON time exceeding the OFF time. When connected to V_{SS}, the "Smoke" alarm will sound the Horn continuously. This control only affects the "Smoke" alarm condition.
7	Timing Resistor	A nominal resistor value of 22 megohms to V_{SS} sets the oscillator frequency to 485 Hz. Thus: a) The IR LED pulses every 8 seconds in standby. b) The OPERATION MONITOR LED pulses very 35 seconds in standby. c) The Horn modulation (ON-OFF) frequency is approximately 8Hz. d) The Low Battery or LED SUPERVISOR trouble pulse to the Horn will occur every 35 seconds, with 17ms duration. e) The IR LED will pulse every 1 second when smoke is detected. f) The Horn will be silenced just before each IR LED pulse for 4.2 ms, to reduce electro-magnetic interference.
8	V_{SS}	Connect this pin to circuit common, the lowest potential.
9	Horn Output 2	This terminal is connected to the brass electrode of the piezoelectric horn.
10	Horn Output 1	This pin is connected to the large silver electrode of the piezoelectric horn.
11	Horn Feedback	This pin is connected to the small silver electrode of the piezoelectric horn.
12	Operation Monitor	This output is a current source of 4mA for driving a visible LED. The LED will flash for 17ms every 35 seconds under normal conditions. The LED will be ON continuously when smoke is first detected. This occurs before the alarm sounds and indicates that the detector is in speed-up mode (1.0 second LED pulse period). This output indicates which unit is alarming in multiple station applications. When this output is used for both local LED indication and remote logic, a resistor must be placed in series with the LED.
13	Multiple Station Input/Output	This Input/Output may be connected via twisted pairs to at least 20 other units. The output goes high after at least two consecutive smoke detections have been made. The output structure allows units of different operating voltages to be connected together with no impairment of performance or excessive loading of the higher voltage units. There is an active pull-down on the output. Because of the high currents sourcing capability of the output, this pin should never be connected to V_{SS} via a low impedance path. An Input level of greater than $0.6V_{DD}$ volts is required to ensure a local alarm.
14	LED Supervisor	This pin must be connected to the LED circuit as shown. Failures detected are open or shorted conditions in the LED and Driver circuit. A failure is indicated by a local pulsed trouble alarm. To defeat this feature, pin 14 must be tied to a voltage about 1.5-volts below V_{DD}, or to pin 2 in most applications.
15	LED Pre-Driver Output	This terminal can source about 13mA. The output voltage is zener clamped at approximately 6.7V and the current becomes limited. The LED current set resistor may be put in the collector circuit, below the LED, but the LED current and therefore the Sensitivity of the smoke detector will vary with supply voltage.

Pin Definition (cont.)

Pin	Name	Function
16	V_{DD}	This pin is connected to the positive battery terminal. Pin 16 should be solidly connected to the V_{DD} side of both the photodiode and the memory capacitor. A V_{DD} guard-ring type foil path around pins 1 and 2 will enhance noise immunity of the detection circuit. This circuit will operate from 7 to 10 volts, although average standby current will increase with supply voltage. Protect the integrated circuit from polarity reversal.
9,10	Alternate Driver for Electro-Mechanical Horns	When the smoke detector circuit is used to drive either a transistorized mechanical or electro-mechanical horn, the feedback (pin 11) must be connected to V_{DD}. When an alarm condition is not present, pin 10 will be at V_{DD} and pin 9 will be at V_{SS}. When an alarm condition is present, pin 10 will switch from V_{DD} to V_{SS} and pin 9 will switch from V_{SS} to V_{DD}. Both horn outputs are capable of sinking or sourcing more than 100mA at a 9-volt supply voltage. Limit the steady state on current to 25mA.
	Transistorized Mech. Horn	The control tab of the horn is connected to pin 9 and pin 10 is left open.
	Electro-Mechanical Horn	Pin 9 is connected through a resistor to the base of an NPN horn driver transistor. Pin 10 is left open.

Timing Waveform



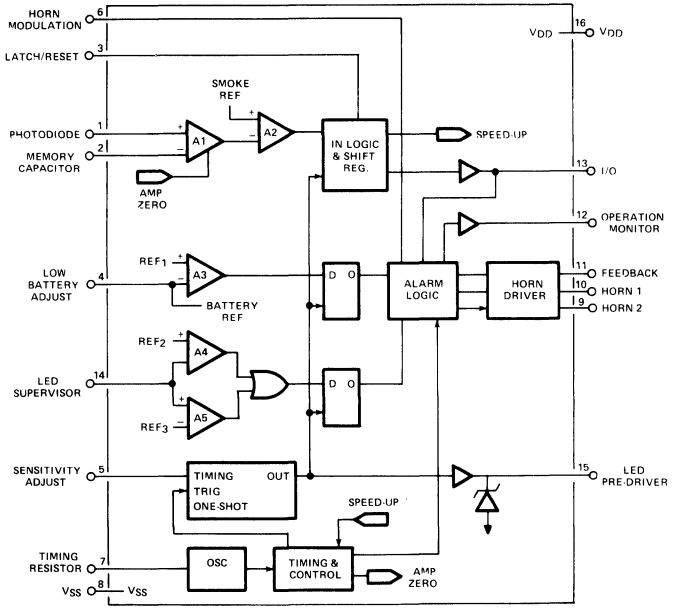
Truth Table

Alarm Status	Input Conditions								Output Conditions				
	Smoke	Low Batt.	LED Sup'r	Pin 3 Latch	Pin 4 Batt	Pin 6 Mod'l	Pin 11 Fdbk	Pin 13 I/O	Pin 9 H2	Pin 10 H1	Pin 12 OP/MO	Pin 13 I/O	Pin 15 LED
Standby	F	F	F	X	N	X	H[4]	N	L	H	P[1]	L	P[2]
Remote	F	X	X	X	N	L	H[4]	H	H[5]	L[5]	P[1]	N	P[2]
Smoke	F	X	X	X	N	H	H[4]	H	H[5.6]	L[5.6]	P[1]	N	P[2]
Local	T (A)	X	X	L	N	L	H[4]	N	H[5]	L[5]	H	H	P[3]
Smoke	T (A)	X	X	L	N	H	H[4]	N	H[5.6]	L[5.6]	H	H	P[3]
Local	T (B)	F	X	H	N	L	H[4]	N	H[5]	L[5]	H	H	P[3]
Smoke	T (B)	F	X	H	N	H	H[4]	N	H[5.6]	L[5.6]	H	H	P[3]
Latched	T (B)	T	X	H	N	X	H[4]	N	L[1]	H[1]	H	H	P[3]
Low Batt	F	T	X	X	N	X	H[4]	N	L[1]	H[1]	P[1]	L	P[2]
LED Sup'r	F	X	T	X	N	X	H[4]	N	L[1]	H[1]	P[1]	L	P[2]
Batt Disable	F	T	F	X	H	X	H[4]	N	L	H	P[1]	L	P[2]
Horn Disable	X	X	X	X	N	X	L	N	L	H	X	X	X

Key:
- T – Logical TRUE, Analog Condition
- F – Logical FALSE, Analog Condition
- H – Logical HIGH, Digital Level or Driver Sourcing
- L – Logical LOW, Digital Level or Driver Sinking
- P – Output PULSE HIGH, Normally LOW
- N – No Signal Applied / Open
- X – Unspecified
- A – After two consecutive smoke detections
- B – After one smoke detection

Notes:
1. Pulsed to opposite state ONCE every fourth PULSE on pin 15.
2. Normal Sample Rate, Typical 8 seconds.
3. 8 Times Normal Sample Rate, Typical 1.0 second.
4. When used with a piezo horn, this signal is oscillating,but considered HIGH.
5. When used with a piezo horn, this signal is oscillating.
6. Signal will be in non-alarm state 37.5% of time.

Block Diagram



Operation

This device utilizes low power CMOS technology to provide all of the necessary functions of a battery operated, photoelectric smoke detector using a minimum of external components.

The LED PRE-DRIVER output pulses an external transistor which in turn, switches on the infrared light emitting diode at a very low duty cycle. The desired IR LED pulse period is determined by the value of the external timing resistor. The Smoke Sensitivity is adjustable through a trimmer resistor which varies the IR LED pulse width.

The light sensing element is a silicon photovoltaic cell which is held at near zero bias to minimize leakage currents. The circuit can detect signals as low as 1mV and generate an alarm. The IR LED pulse repetition rate increases when smoke is detected.

For use with a 9-volt battery, an internal zener is incorporated into the IC. When the minimum battery voltage is reached (tested during the IR LED on pulse), the output produces a short trouble alarm pulse or "blip". The horn is pulsed after every fourth IR LED pulse. When the alarm mode control is set for non-latching operation, the unit will sound a continuous alarm when smoke is detected even during low battery conditions. When the alarm mode control is set for latching operation, the low battery trouble alarm will override the smoke alarm, in accordance with UL217specifications.

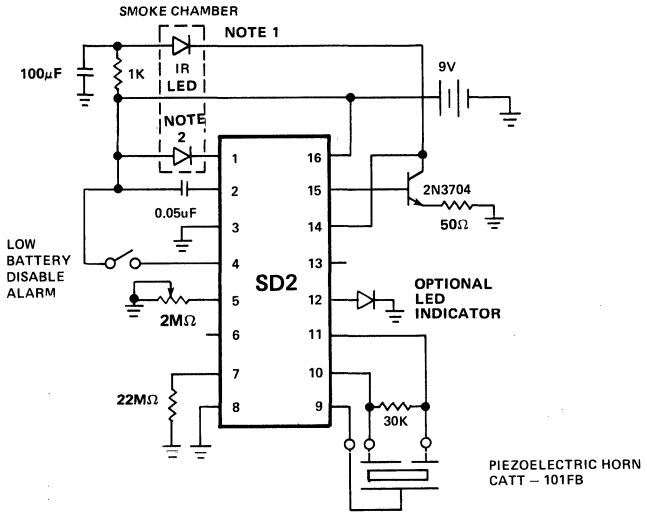
The LED SUPERVISOR tests for open or shorted conditions in the LED and Driver circuit. For either condition of the IR LED when pulsed, failure of the forward voltage to fall between two limits produces a trouble alarm pulse on the Horn after every fourth LED pulse.

The Input/Output terminal (I/O) is used to interconnect SD2 units for multiple station applications.

The OPERATION MONITOR pulses a visible LED after every fourth IR LED pulse to indicate device operation. For a local Smoke detection the LED is driven continuously.

The Horn Driver circuit self-oscillates with a piezoelectric element or enables an electro-mechanical horn when pin 11 is connected to V_{DD}.

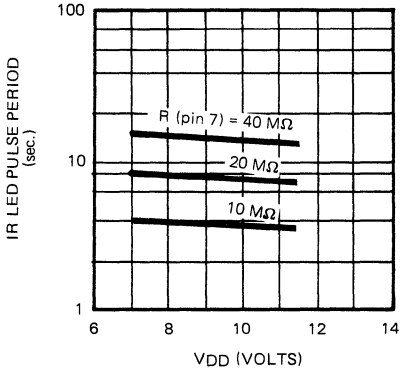
Typical System — Non-Latching Single Station



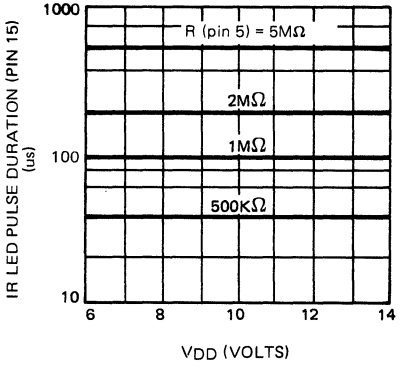
Notes: 1. IR Diode RCA Type SG 1010A or Spectronics Type SE 5455-4
Clairex Type CLED-1
2. IR Photo detectors Vactec VTS4085

Typical Performance Curves (T_A = 25°C unless otherwise noted)

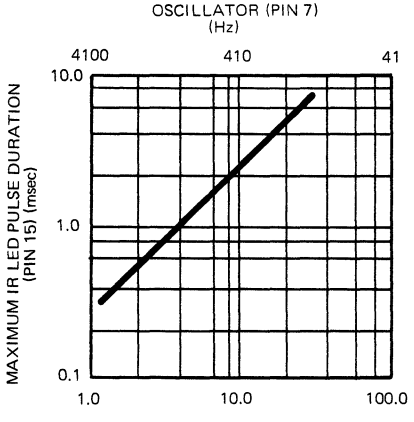
T_{LED} vs V_{DD},



T_{PD} vs V_{DD}

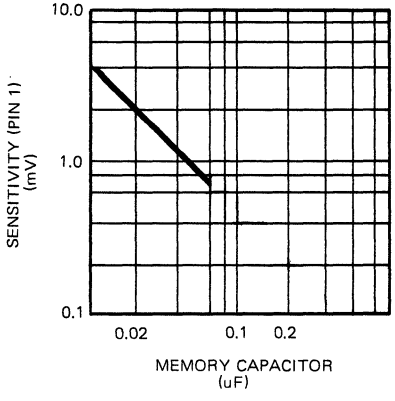


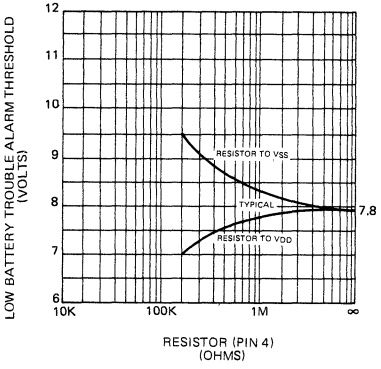
IR LED vs T_{LED} vs Oscillator



$$I_{AVG\ (LED)} = [(I_{OH(15)}) + I_{LED}] \frac{T_{PD}}{T_{LED}}$$

Detector Sensitivity vs C_{MEM}





Ionization Chamber Type Smoke Detector Circuit

Ordering Information

Device	Package	Order No.
SD3A	14 Pin Plastic	SD3AP

Features

- ☐ Capable of Directly Driving Piezoelectric Horn
- ☐ Multiple I/O Station Capability
- ☐ Low Battery Level Beep Alarm
- ☐ Continuous or Intermittent Alarm
- ☐ LowPower Consumption - 10μA Maximum
- ☐ High Noise Immunity CMOS Technology
- ☐ Meets UL217 Requirements
- ☐ Uses Economical Zinc Carbon 9V Battery
- ☐ No Voltage Detection Adjustment Necessary
- ☐ Optional Battery Impedance Check

Absolute Maximum Ratings

Storage Temperature Range	-55°C to +150°C
Operating Temperature	0°C to +50°C
Supply Voltage	+15.0V
Voltage on All Other Pins	-0.3V to V_{DD} + 0.3V
Power Dissipation	300mW
Relative Humidity Range	5% to 95%

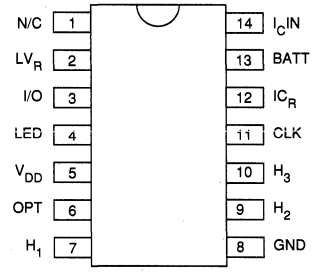
General Description

The SD3A is a CMOS integrated circuit designed for an ionization chamber type smoke detector that directly drives a piezoelectric horn. It satisfies UL217 requirements and is available in a 14-lead plastic DIP.

Designed and built for an efficient, low component count, smoke detector system, the SD3A has numerous features that allow increased alarm effectiveness and reduced false triggering. With an improved offset voltage and built-in hysteresis, this device requires less ion source and has increased sensitivity.

The horn output of this circuit can be a continuous or intermittent alarm. An optional LED indicator can be used to monitor the battery level. The SD3A operates on a single 9-volt alkaline or zinc carbon battery. It also may be used in multiple station connection applications.

Pin Configuration



top view

14-pin DIP

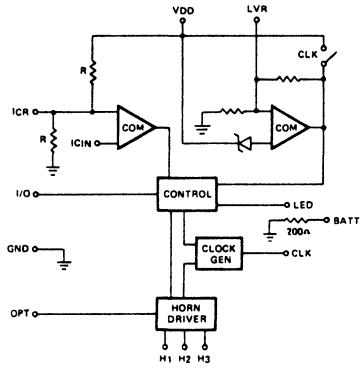
DC Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Operating Voltage	V_{DD}	6.0		10.0	V	
Supply Current	I_{DD}		7.0	10.0	µA	V_{DD} = 9.0V; LED not con't
Ionization Chamber Input Reference Voltage	V_{IR}	$1/2V_{DD}$ - 0.15	$1/2V_{DD}$	$1/2V_{DD}$ + 0.15	V	V_{IR} = floating
		0.5		V_{DD} - 3	V	V_{IR} tied to external resistor
Ionization Chamber Input Leakage Current	I_I			1.0	pA	Input Voltage = 9.0V
Ionization Chamber Input Offset Voltage	V_{OS}		50	150	mV	
Input/Output Alarm Trigger Voltage	$V_{I/O}$	3.0			V	
Input/Output Drive Current	$I_{I/O}$	-3.0	-5.0		mA	V_{DD} = 7.0V; V_{IO} = 6.0V
Operating Voltage Low Voltage Detection	V_{DD}	7.5	7.7	7.9	V	No Adjustment Necessary
Horn Current H2, H3	I_{HORN}	-25			mA	V_{DD} = 7.0V; V_{HORN} = 1.0V
				25	mA	V_{DD} = 7.0V; V_{HORN} = 5.0V
LED Current	I_{LED}	2	4		mA	V_{DD} = 8.0V
Clock Period	i_C	20	40	60	sec	C_L = 1µF; V_{DD} = 8.0V
Clock ON Time	t_{ON}	10	20	30	msec	C_L = 1µF; V_{DD} = 8.0V
LED Flash Period	t_{LED}	10		30	sec	C_L = 1µF; V_{DD} = 8.0V
Horn Pulse ON/OFF Time	t_{OSC}		0.5		sec	Intermittent Mode Only

Pin Definition

Label	SD3A Pin	Function
CLK	11	Clock oscillates with a nominal period of 40 sec when an external 1µF capacitor is connected to the clock lead.
IC_R	12	The Ionization Chamber Reference Input is connected to the other side of the Ionization Chamber comparator. It is set at 1/2 V_{DD} generated by an internal resistor network.
IC_{IN}	14	The Ionization Chamber Input has high input impedence and is connected to one side of the Ionization Chamber comparator.
I/O	3	Input/Output terminal can drive up to 20 units using a simple two wire bus.
LED	4	An optional Light Emitting Diode can be attached to this lead to monitor operation of the SD3A.
V_{DD}	5	Power Supply.
H_1	7	The Horn Driver Feedback Input is used for a piezoelectric horn feedback connection.
GND	8	Ground.
H_2	9	This horn driver output connects to the brass disc of the piezoelectric horn.
H_3	10	This horn driver output connects to the top electrode of the piezoelectric horn.
LV_R	2	For Low Voltage Detection Point Adjustment.
OPT	6	This pin controls the type of horn drive. When tied to V_{DD}, the horn output is continuous. When this pin is left open, the horn output is intermittent.
BATT	13	This lead is for battery Test.

Block Diagram



Operation

The SD3A is specifically designed to directly drive a piezoelectric horn. In this circuit the ionization chamber input (I_{CIN}) is connected to the first input of a voltage comparator which responds to a voltage drop by activating the horn. The other input of the voltage comparator is connected to an internal reference voltage preset at $V_{DD}/2$. This reference voltage can also be adjusted externally by a resistor or potentiometer tied to the ionization chamber reference input (I_{CR}). Adjustment of the bias voltage sets the sensitivity of the chamber to the smoke.

The horn output of this device can be connected to an electromechanical horn through an external resistor. The piezoelectric horn drive provides a feedback lead for resonance oscillation to boost the sound output level at a modulated tone to increase the horn effectiveness.

Low voltage is detected by the internal zener reference and voltage detection circuitry. This design allows either utilization of the preset low voltage detection level or external adjustment using a resistor tied to the low voltage reference (LV_R) lead of SD3A. The preset low battery voltage detection level is at 7.7 volts ± 2.0V. Several connection options are illustrated in Figures 1, 2 and 3.

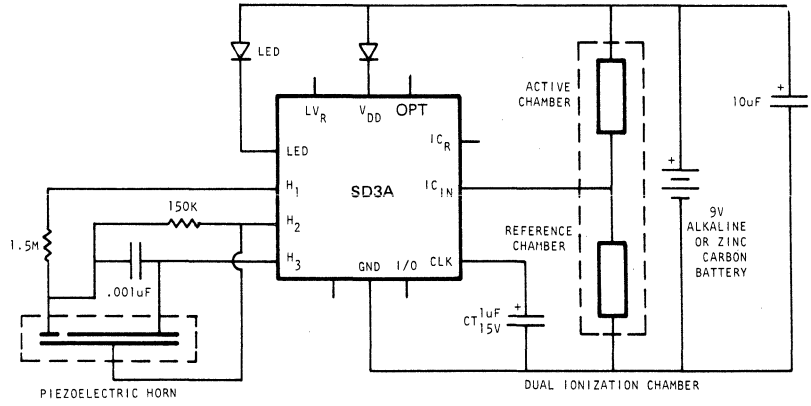


Figure 1. SD3A with a Daul Ionization Chamber and Piezoelectric Horn together with an LED as battery connection indicator.

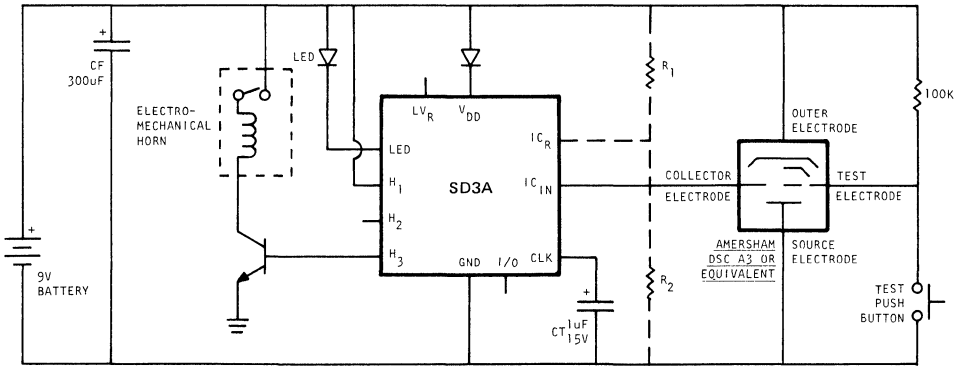


Figure 2. SD3A with an Amersham DSC A3 Concentric Chamber and an electromechanical Horn. Special features are optional R1/R2 resistor network for adjusting comparator trip voltage and built-in test electrode for in-circuit alarm test.

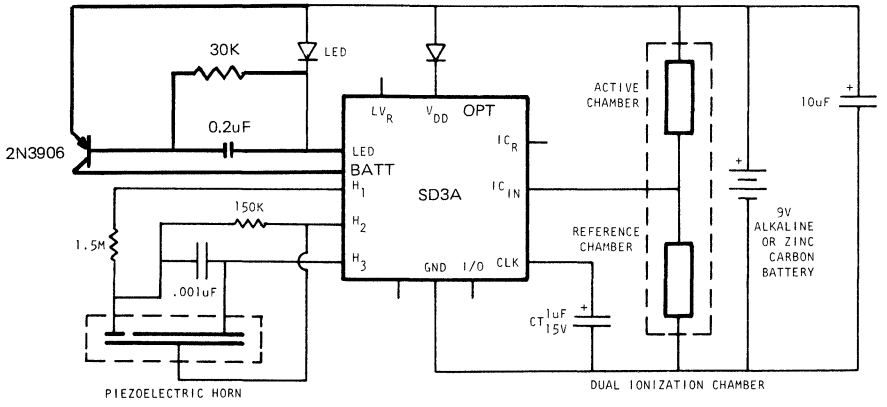
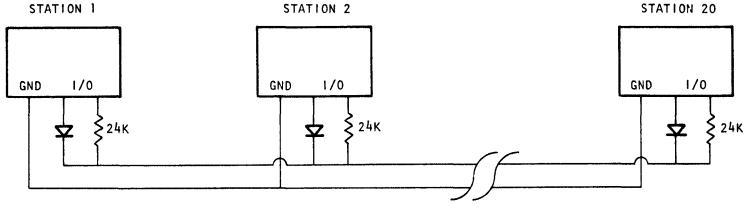


Figure 3. SD3A with a Dual Ion Chamber, Piezoelectric Horn, LED, Battery Impedance Check, and Intermittent Horn.

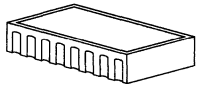
Multiple Station Connection

The SD3A can drive up to 20 units simultaneously. When any unit detects smoke, all the units are triggered. However, when only one unit gives a beep indicating low battery level, only that unit beeps. Multiple station connection of SD3A devices requires only a simple two-wire bus.

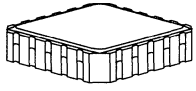


Surface Mount Packages

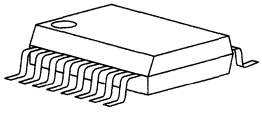
Various surface mount packages are available for HVCMOS, DMOS, and CMOS devices. Refer to the respective product data sheet for availability and package outline for detailed dimensional drawings. This section also includes lead bend and taping options.



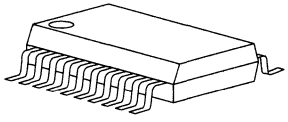
16 Terminal
Ceramic Chip Carrier



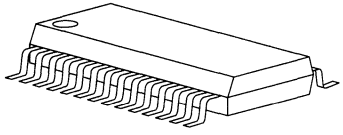
Type "C" Leadless
20 Terminal
Ceramic Chip Carrier



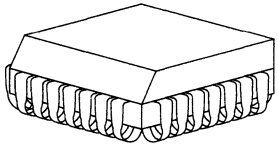
16-Lead *
Small Outline



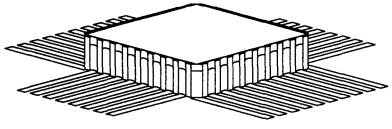
20-Lead *
Small Outline



28-Lead *
Small Outline

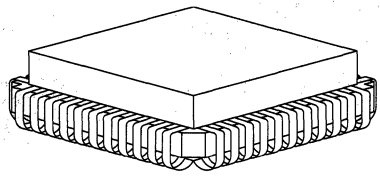


28-Lead Plastic Quad
"J" Bend

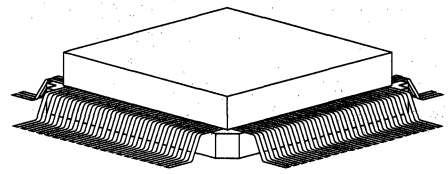


36-Leaded Ceramic Chip Carrier
Available with "CR", "CF", and "CS"
Lead Bend Options

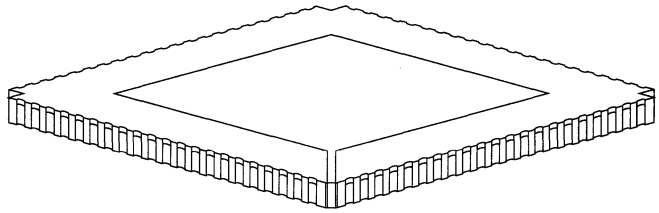
*300 mil wide body.



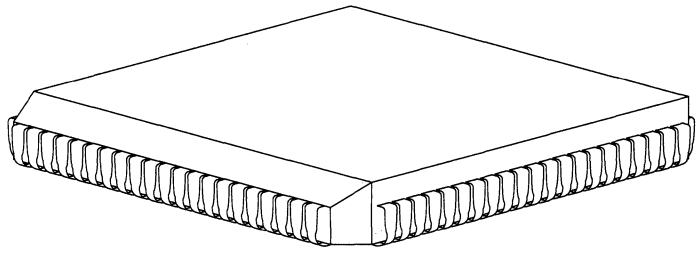
44-Lead Plastic and Ceramic Quads
"J" Bend



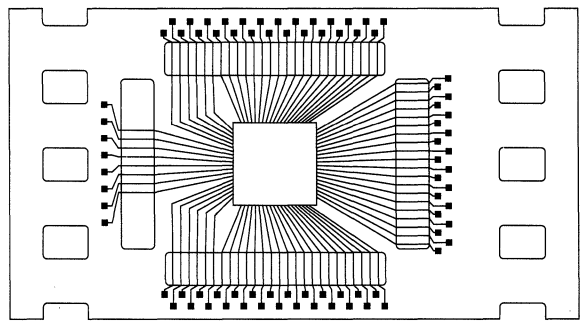
80-Lead Plastic and Ceramic Quads



84-Terminal Ceramic Chip Carrier
Type "B"



84-Lead Plastic Quad
"J" Bend



Die on tape
(for Tape Automated Bonding)

Lead Bend Options

Lead bend options are available in order to retrofit existing boards with small, cost effective, pin-compatible TO-92 packages, or for the purpose of surface mounting.

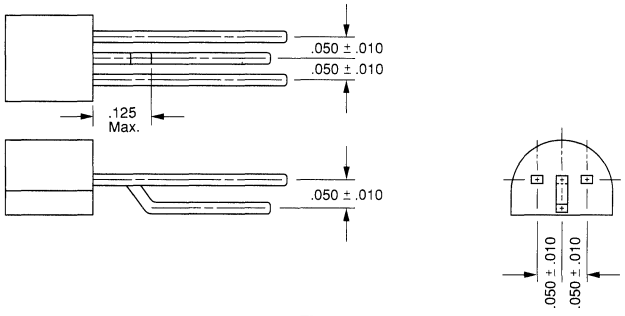


Figure 1
TO-92 leads bent for TO-18 or TO-52 pin circle (Ordering information: Option P015)*

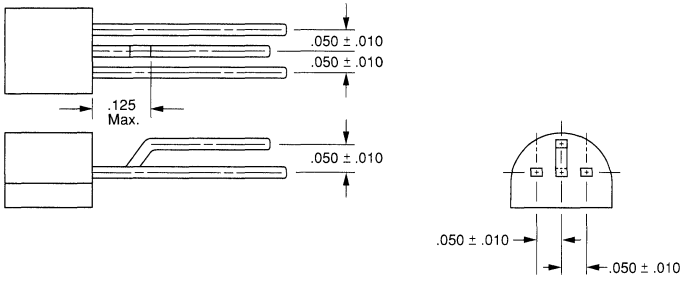


Figure 2
TO-92 leads bent for reversed TO-18 or TO-52 pin circle (Ordering information: Option P016)*

*Lead lengths are those of original components as shown in the Package Outline Section (i.e., uncropped, unless otherwise specified).

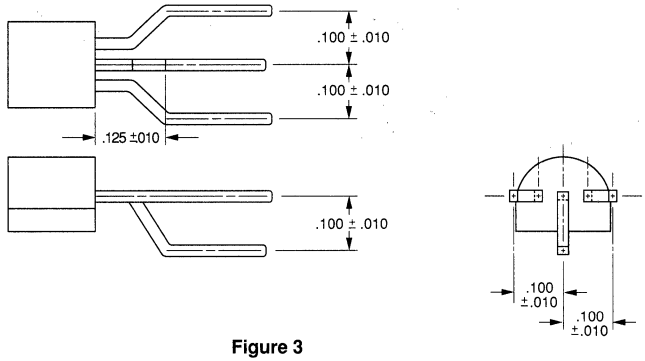


Figure 3
TO-92 leads bent for TO-5 or TO-39 pin circle (Ordering information: Option P017)*

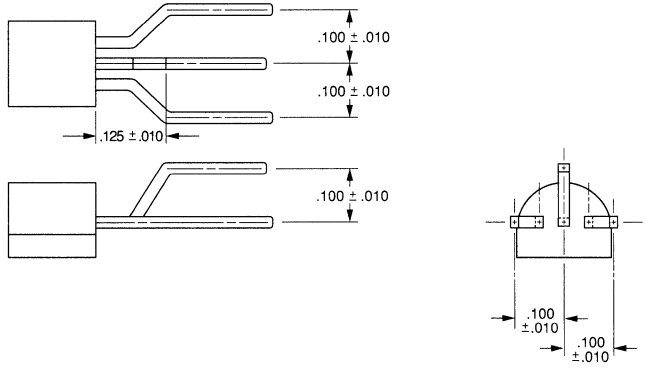


Figure 4
TO-92 leads bent for reversed TO-5 or TO-39 pin circle (Ordering information: Option P018)*

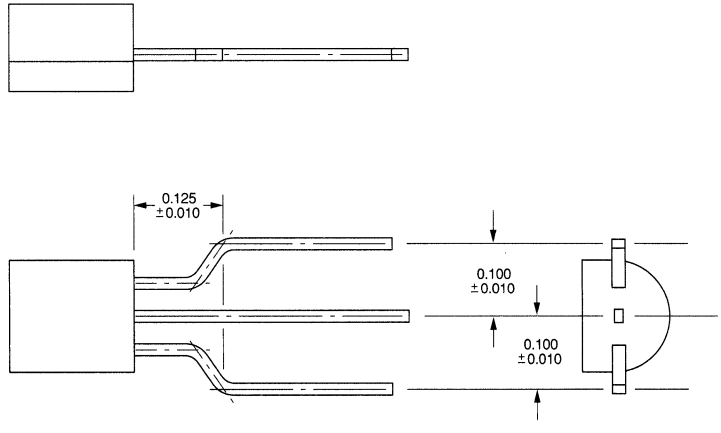


Figure 5
TO-92 leads bent for TO-220 (Ordering information: Option P011)*

*Lead lengths are those of original components as shown in the Package Outline Section (i.e., uncropped, unless otherwise specified).

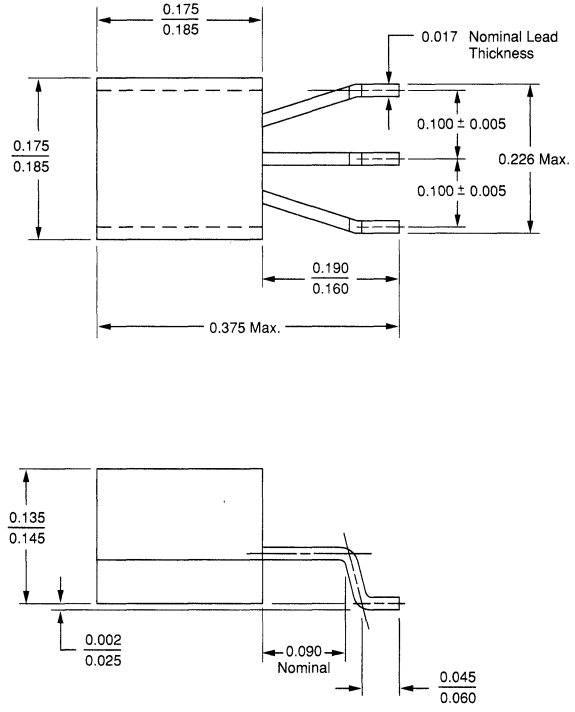


Figure 6
TO-92 for surface mounting. Leads formed for pad spacing of 0.100" center to center (Ordering information: Option P010)

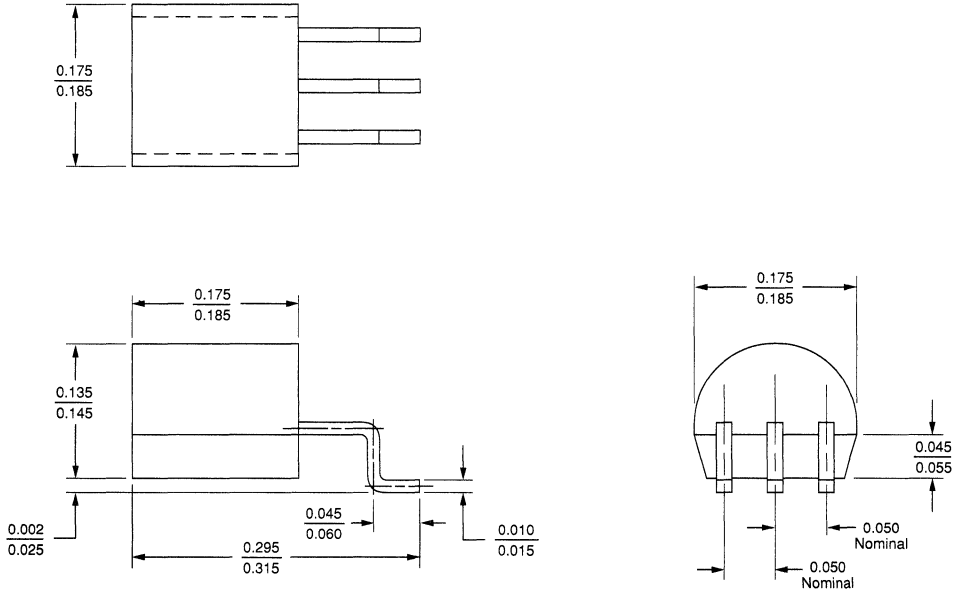
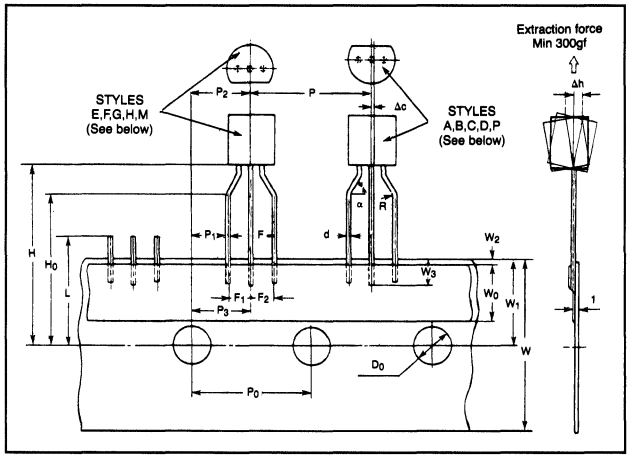


Figure 7
TO-92 for surface mounting. Leads formed for pad spacing of 0.050" center to center (Ordering information: Option P012)

TO-92 Taping Specifications and Winding Styles (per EIA Standard RS468)

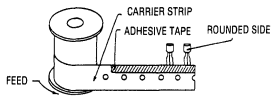


P	12.7 ± 0.5	H_0	16 ± 0.5
P_0	12.7 ± 0.2	F	$5^{+0.8}_{-0.2}$
P_1	3.85 ± 0.5	$F_1 - F_2$	± 0.3
P_2	6.35 ± 0.5	D_0	4 ± 0.2
P_3	6.35	t	0.7 ± 0.2
W	$18^{+1.0}_{-0.5}$	Δ_h	0 ± 1
W_0	6 ± 1	d	$0.50^{+0.06}_{-0.05}$ dia.
W_1	9 ± 0.5	R	0.8
W_2	Max. 0.5	α	45° – 60°
W_3	Min. 4.5	L	Max. 11
H	19.5 ± 0.5	Δ_C	0 ± 0.5

All dimensions in millimeters.

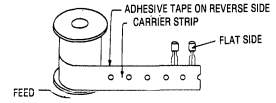
STYLE A

STYLE A IS PREFERRED



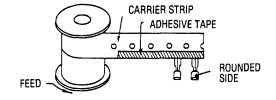
ROUNDED SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

STYLE B



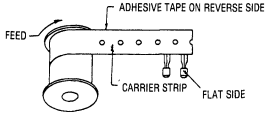
FLAT SIDE OF TRANSISTOR AND CARRIER STRIP VISIBLE
(ADHESIVE TAPE ON REVERSE SIDE)

STYLE C



ROUNDED SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

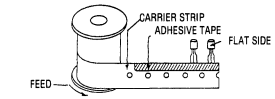
STYLE D



FLAT SIDE OF TRANSISTOR AND CARRIER STRIP VISIBLE
(ADHESIVE TAPE ON REVERSE SIDE)

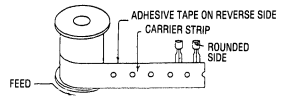
STYLE E

STYLE E IS A PREFERRED STYLE



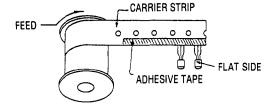
FLAT SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

STYLE F



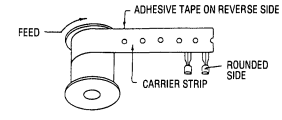
ROUNDED SIDE OF TRANSISTOR AND CARRIER STRIP VISIBLE
(ADHESIVE TAPE ON REVERSE SIDE)

STYLE G



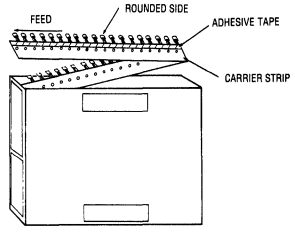
FLAT SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

STYLE H



ROUNDED SIDE OF TRANSISTOR AND CARRIER STRIP VISIBLE
(ADHESIVE TAPE ON REVERSE SIDE)

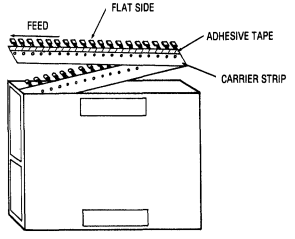
STYLE P



ROUNDED SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

STYLE P IS EQUIVALENT TO STYLES A, B, C, D OF REEL PACK DEPENDING ON WHICH BOX-FLAP IS OPENED AND WHICH END OF THE BOX THE DEVICES ARE FED FROM.

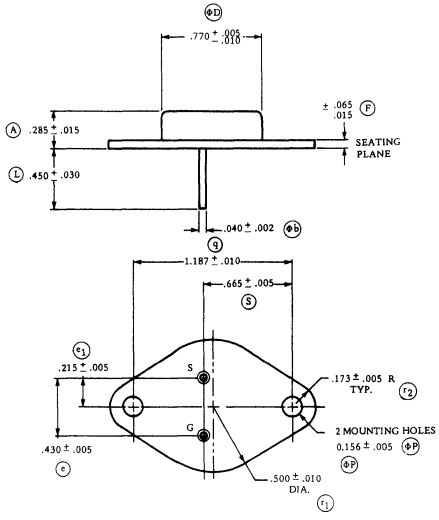
STYLE M



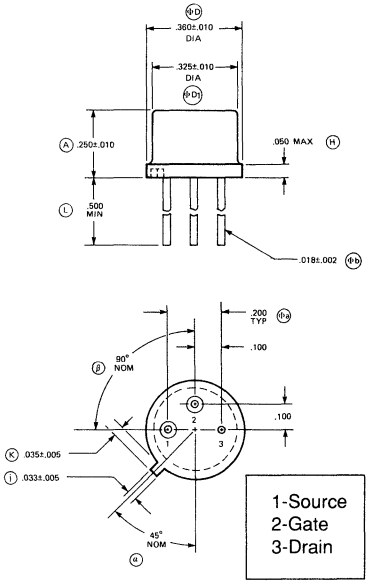
FLAT SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

STYLE M AMMO PACK IS EQUIVALENT TO STYLES E, F, G, H OF REEL PACK DEPENDING ON WHICH BOX-FLAP IS OPENED AND WHICH END OF THE BOX THE DEVICES ARE FED FROM.

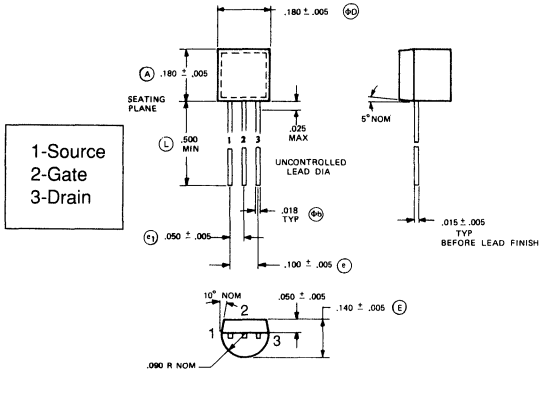
Package Outlines



TO-3 Metal Can Packages
2-Lead (Steel)



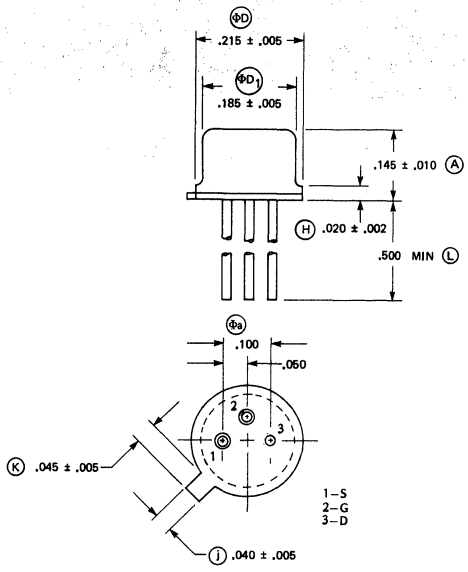
TO-39 Metal Can Package
3-Lead



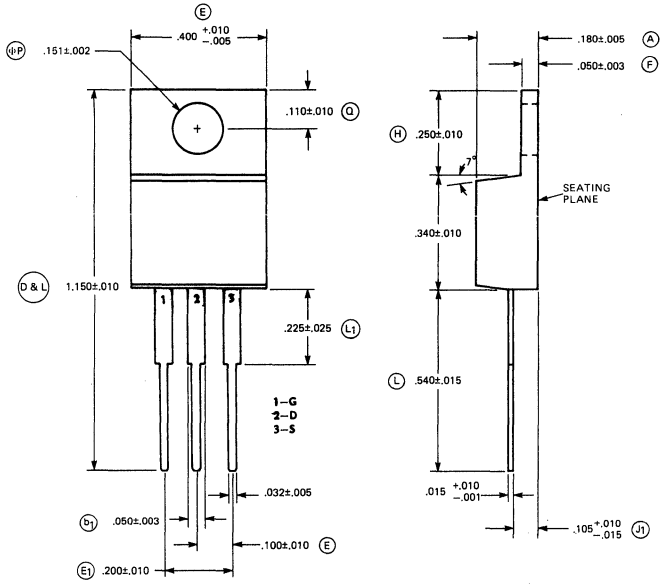
Note: Excludes parts with 'R' prefix.

TO-92 Plastic Package
3-Lead

Note: Circle (i.e., Ⓑ) indicates JEDEC Reference.

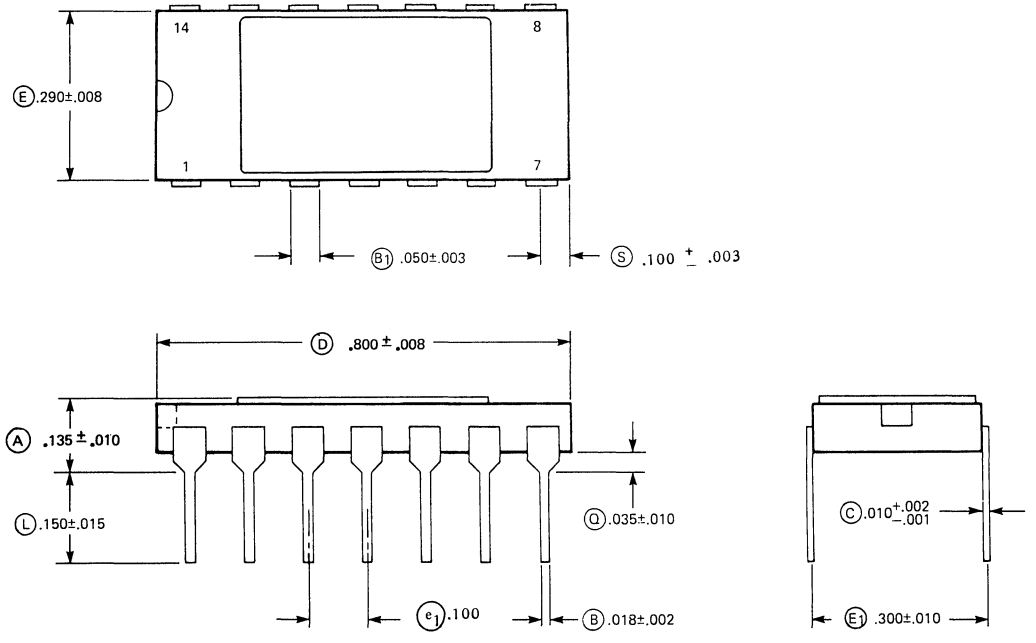


TO-52 Metal Can Package
3-Lead

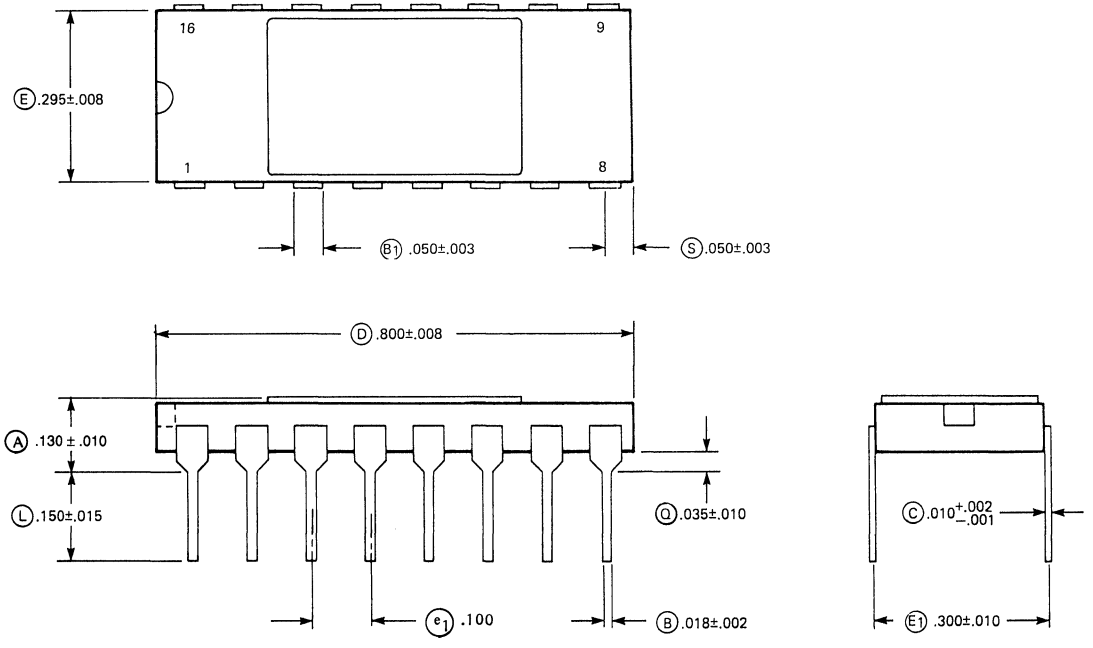


TO-220 Power Package
3-Lead

Note: Circle (i.e., Ⓑ) indicates JEDEC Reference.

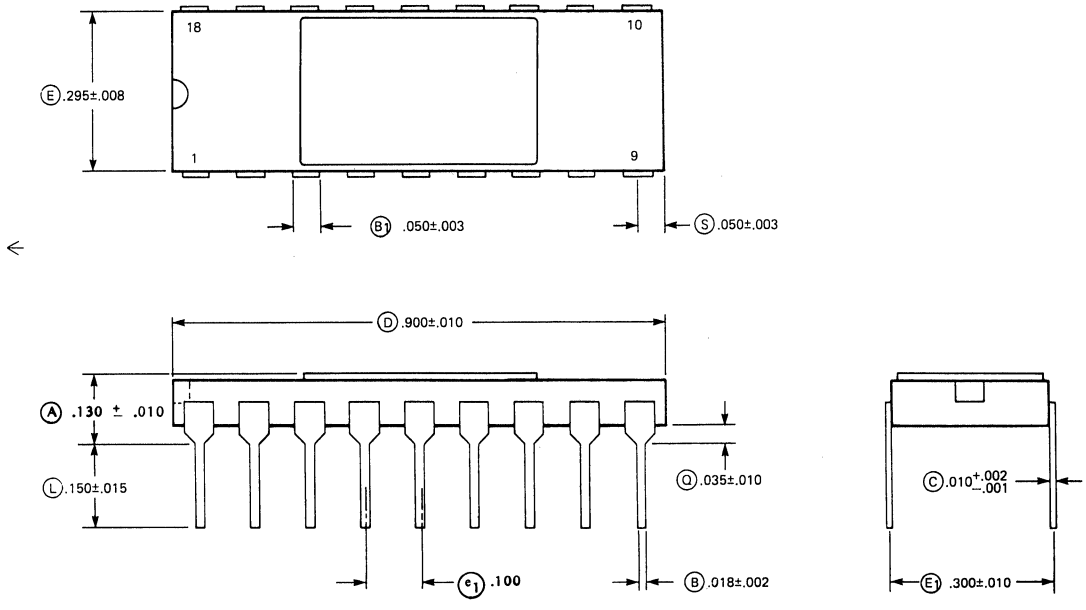


14-Lead Ceramic Side Brazed Package

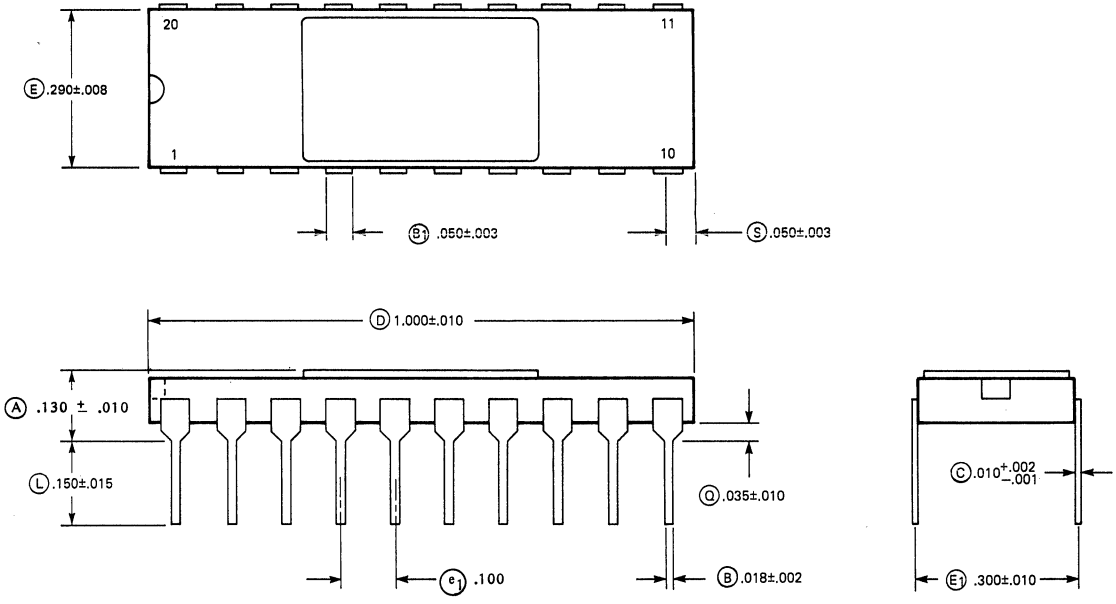


16-Lead Ceramic Side-Brazed Package

Note: Circle (i.e., Ⓑ) indicates JEDEC Reference.

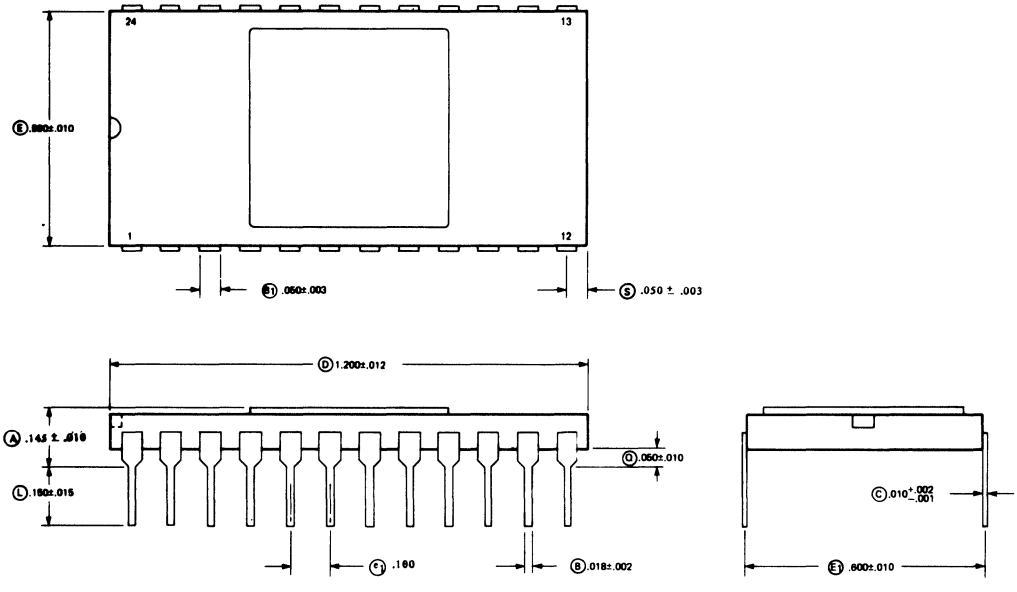


18-Lead Ceramic Side-Brazed Package

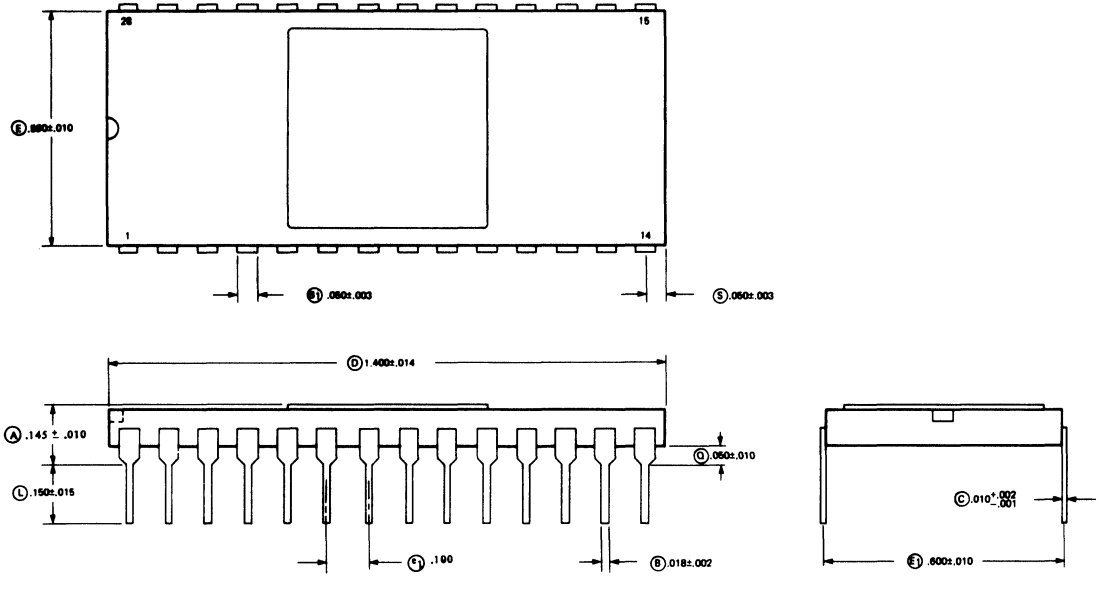


20-Lead Ceramic Side-Brazed Package

Note: Circle (i.e., Ⓑ) indicates JEDEC Reference.

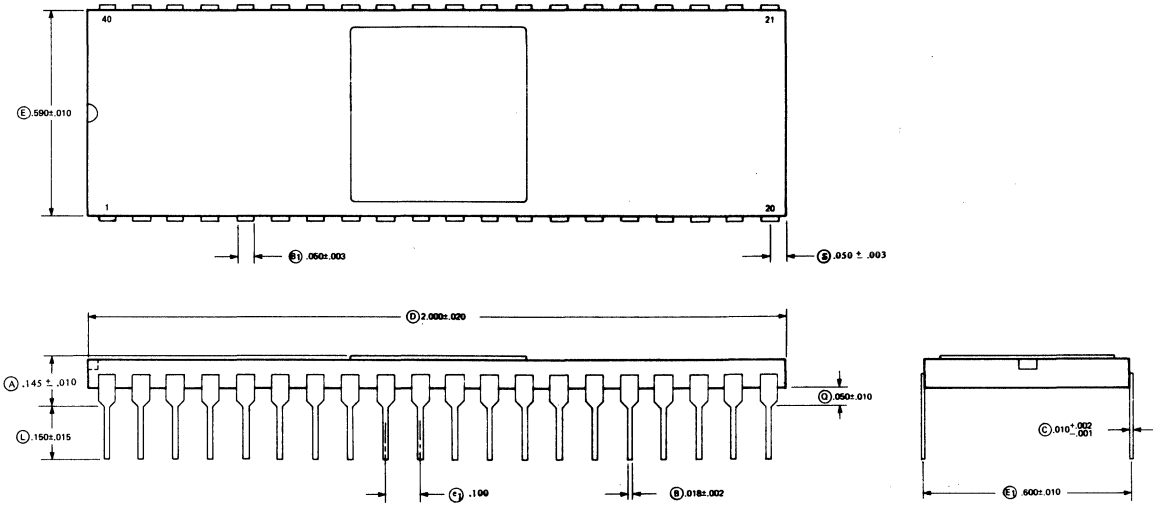


24-Lead Ceramic Side-Brazed Package



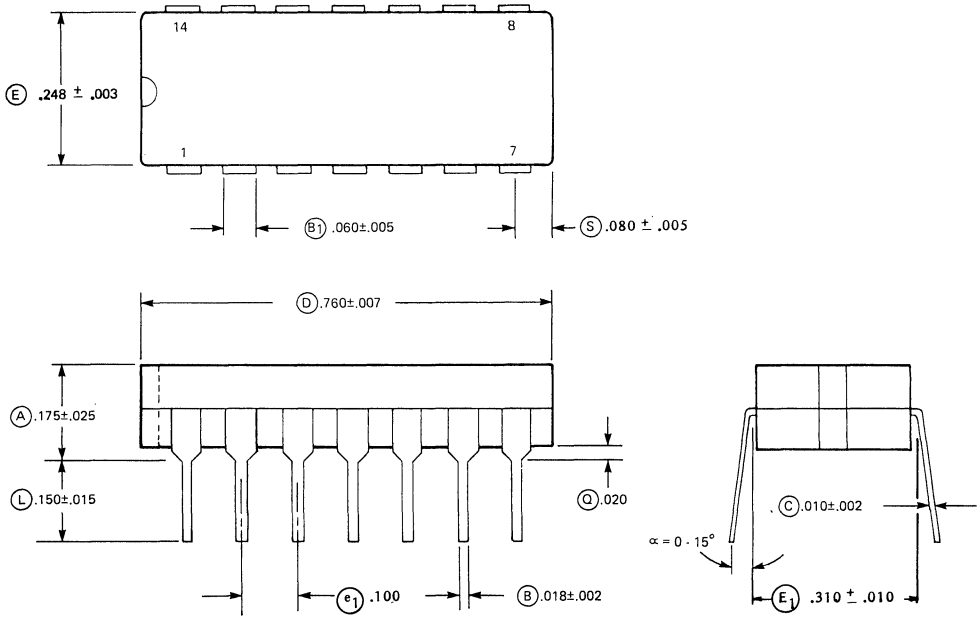
28-Lead Ceramic Side-Brazed Package

Note: Circle (i.e., (B)) indicates JEDEC Reference.

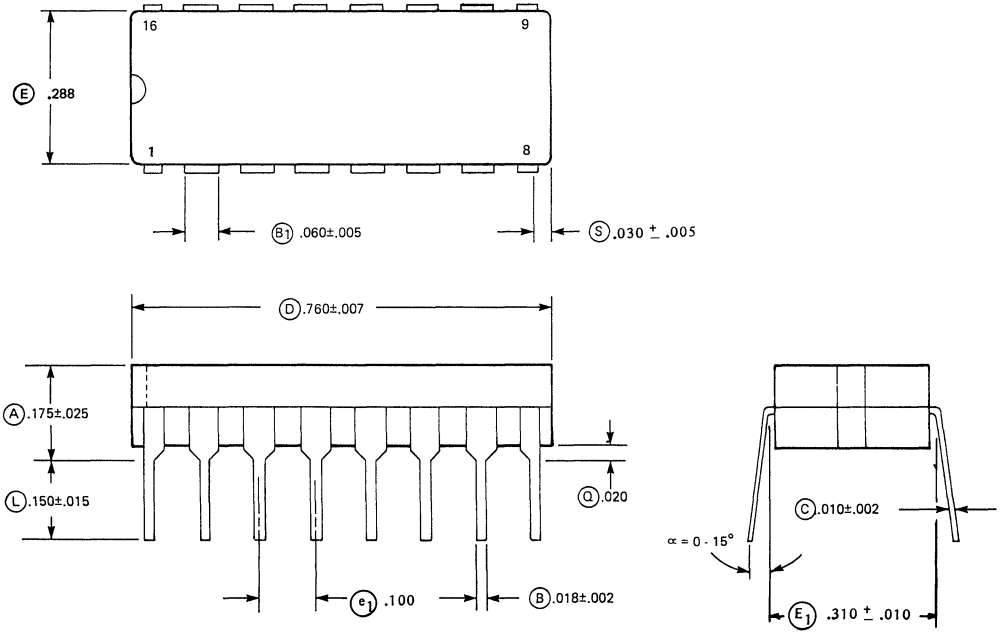


40-Lead Ceramic Side-Brazed Package

Note: Circle (i.e., Ⓑ) indicates JEDEC Reference.

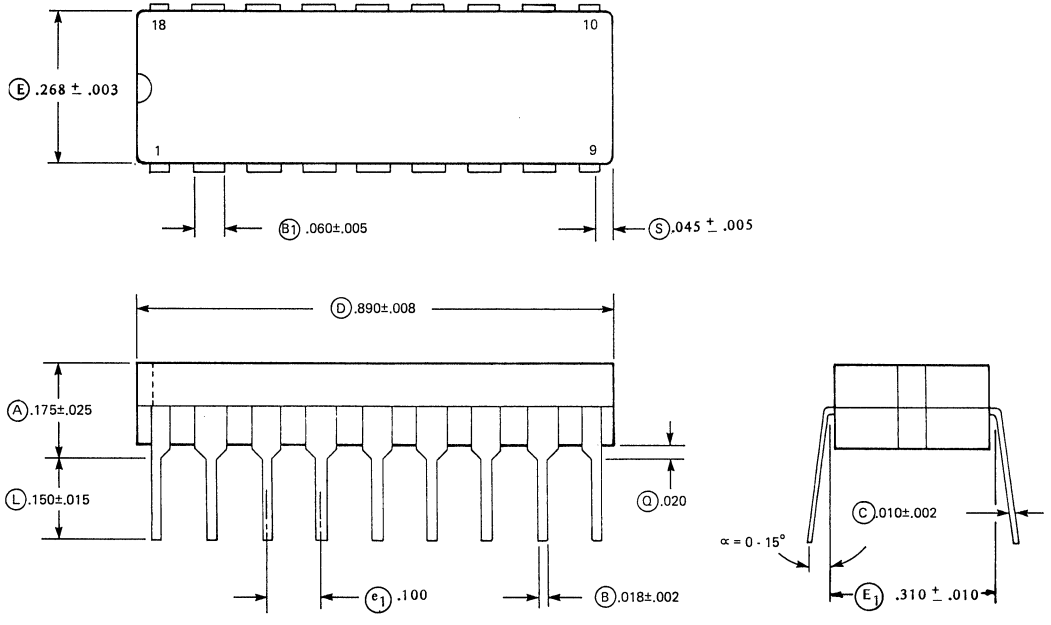


14-Lead CERDIP Package

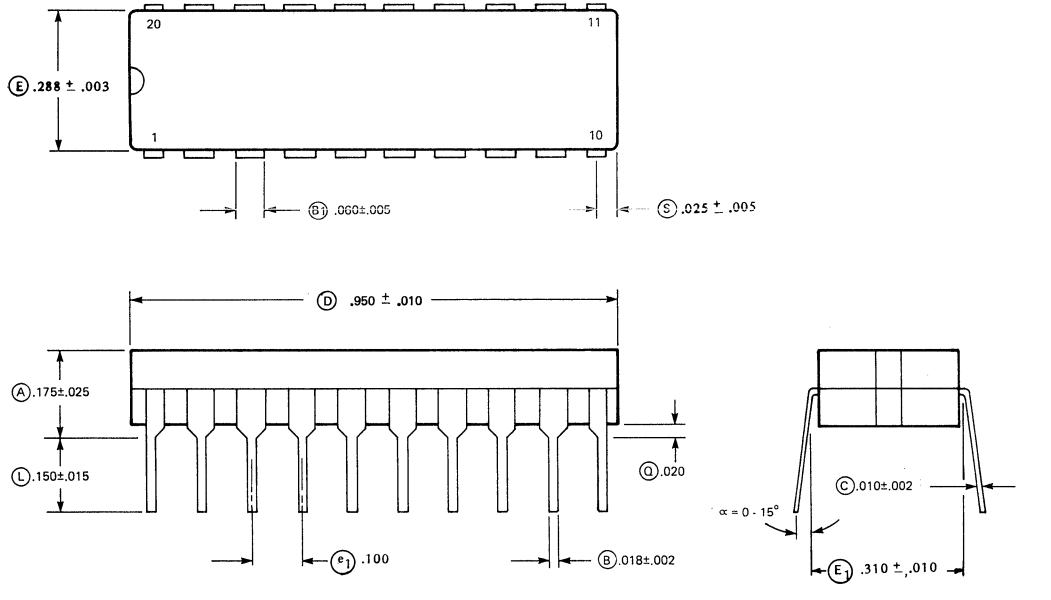


16-Lead CERDIP Package

Note: Circle (i.e., Ⓑ) indicates SEMI-STANDARD G1.1 STD.1.

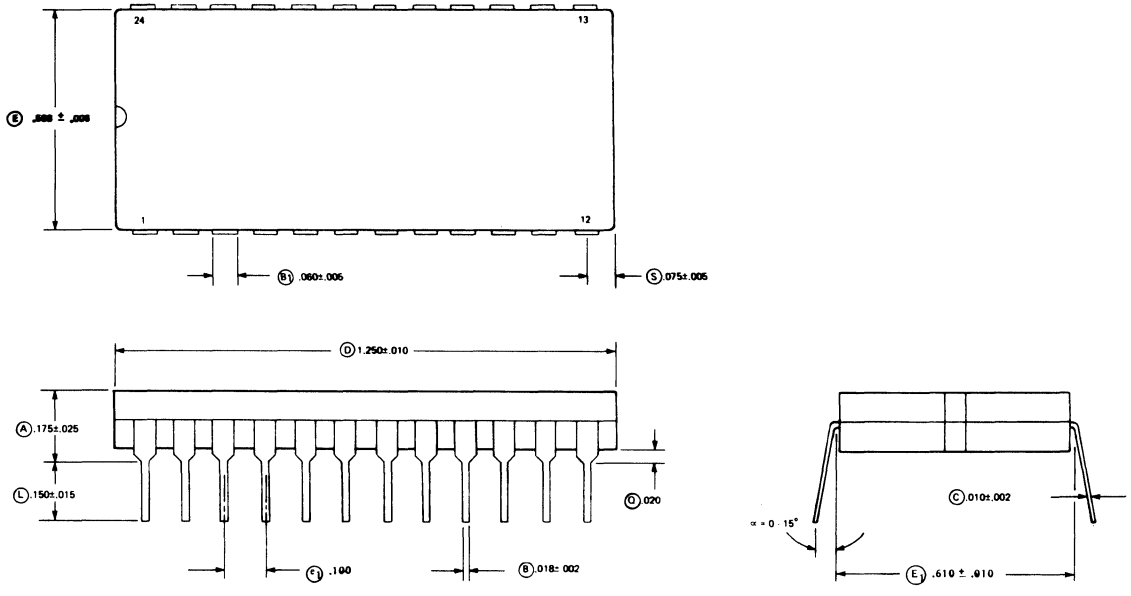


18-Lead CERDIP Package

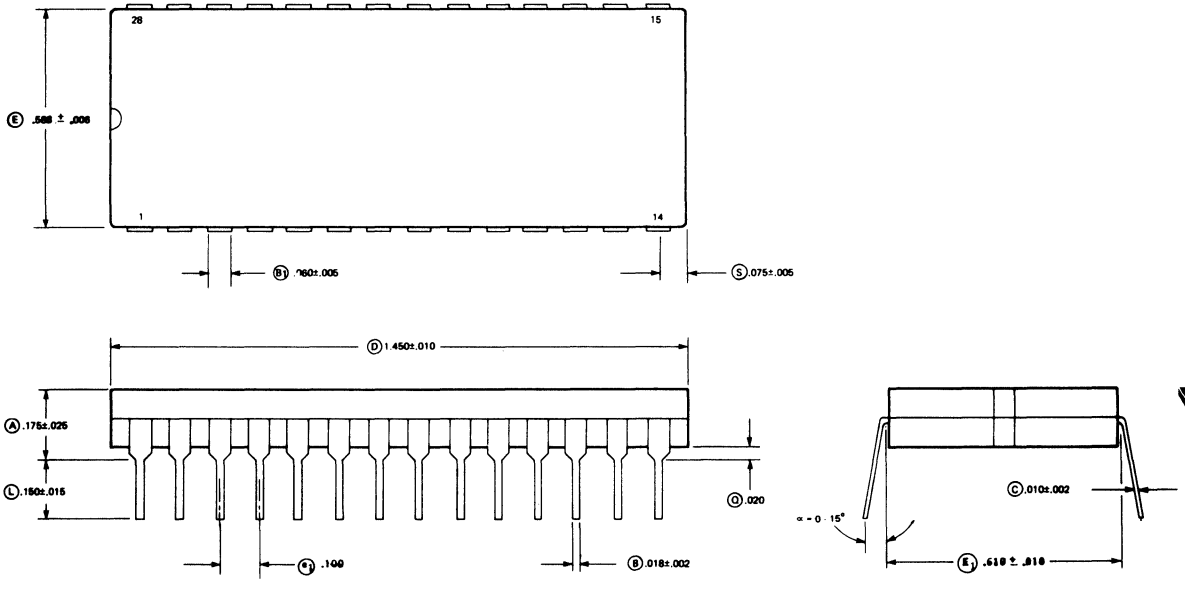


20-Lead CERDIP Package

Note: Circle (i.e., Ⓑ) indicates SEMI-STANDARD G1.1 STD.1.

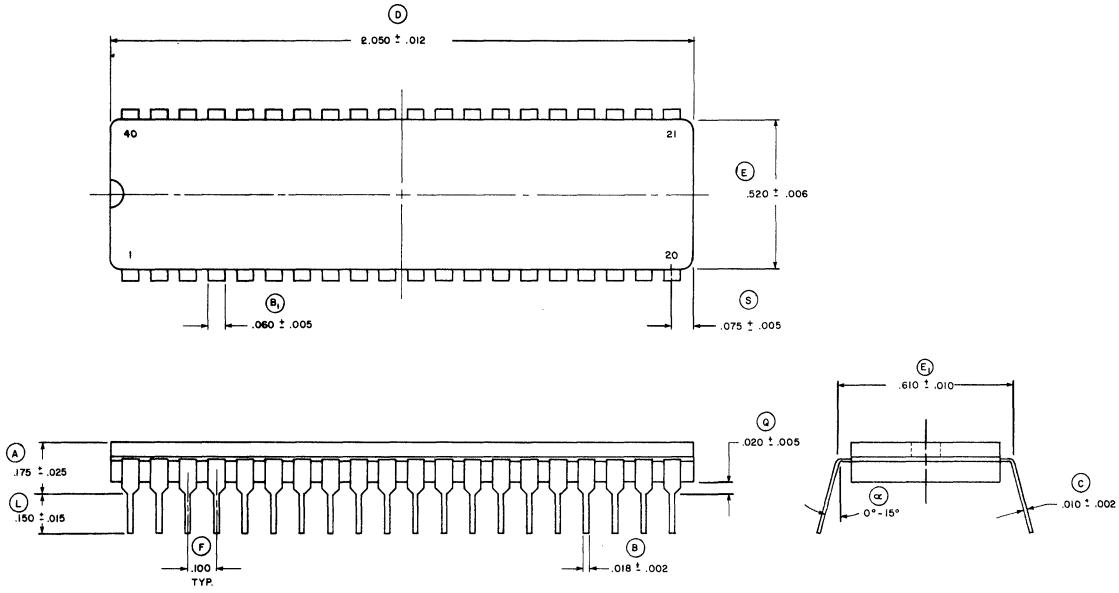


24-Lead CERDIP Package

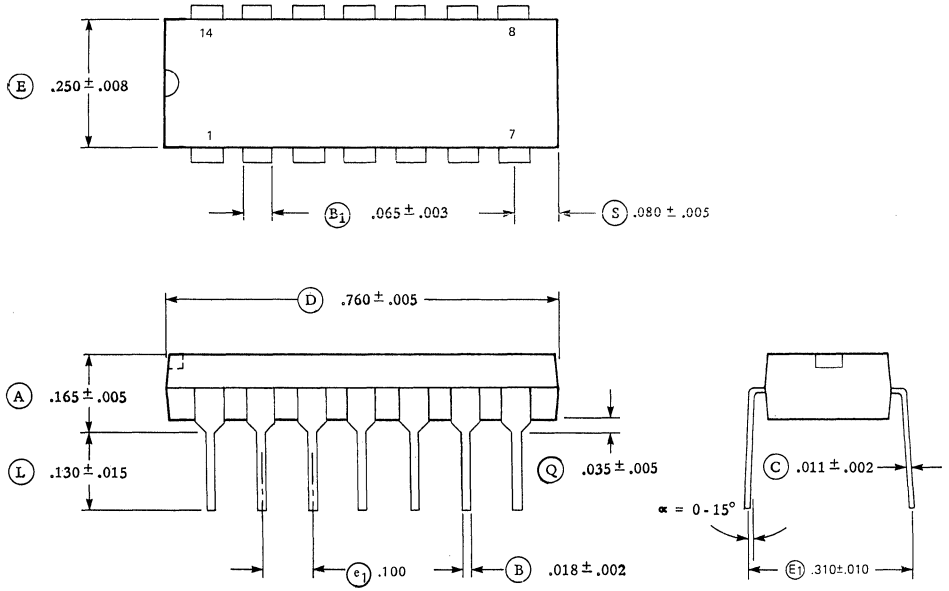


28-Lead CERDIP Package

Note: Circle (i.e., Ⓑ) indicates SEMI-STANDARD G1.1 STD.1.

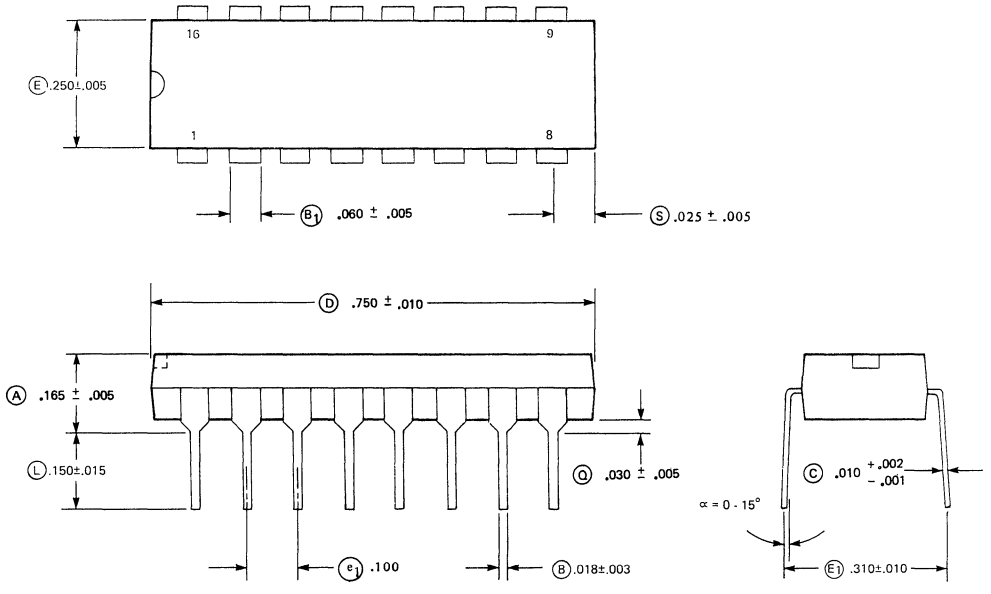


40-Lead CERDIP Package

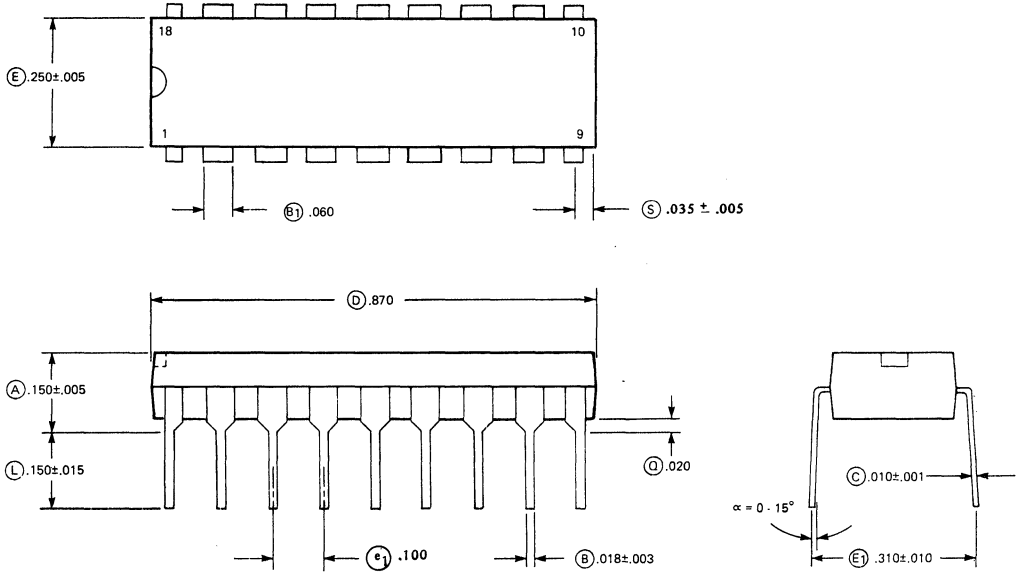


14-Lead Plastic Dual-In-Line Package

Note: Circle (i.e., Ⓑ) indicates JEDEC Reference.

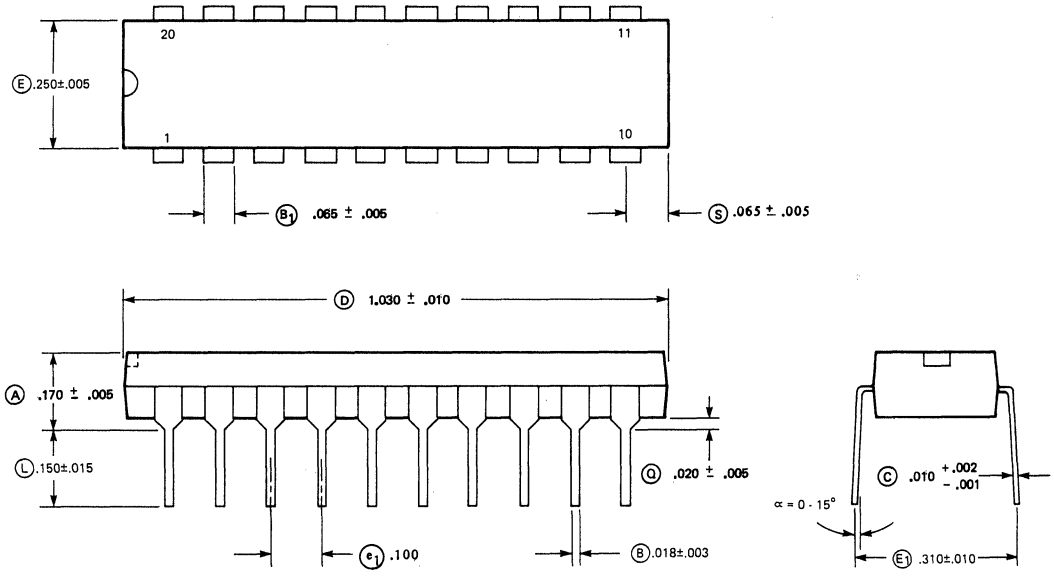


16-Lead Plastic Dual-In-Line Package

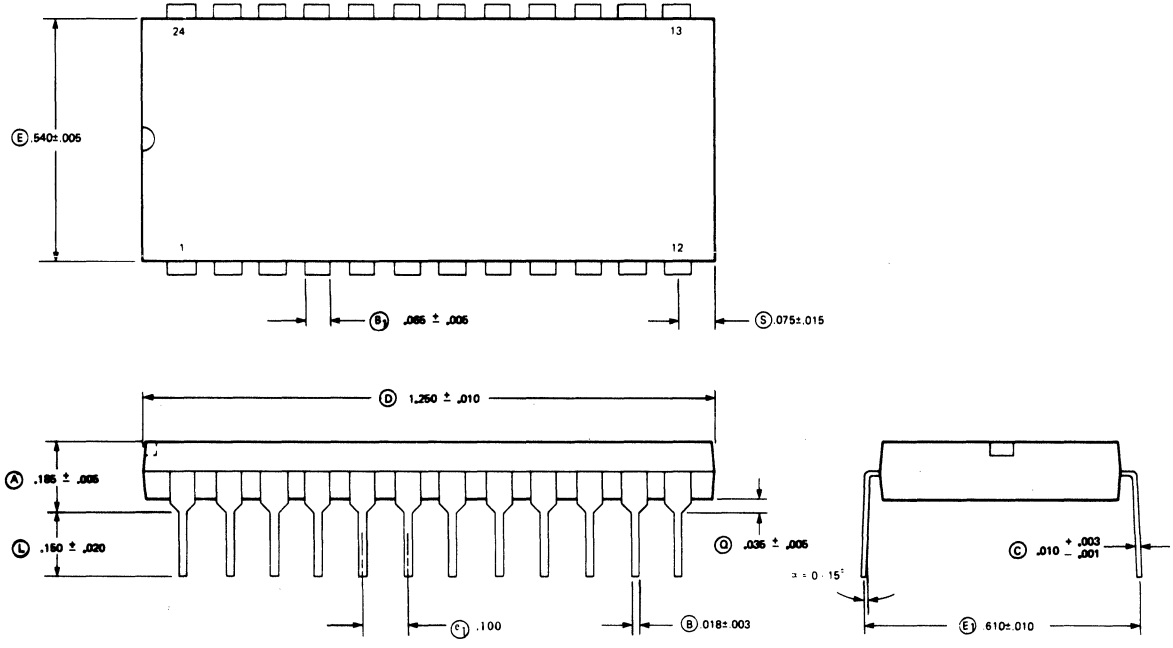


18-Lead Plastic Dual-In-Line Package

Note: Circle (i.e., Ⓑ) indicates JEDEC Reference.

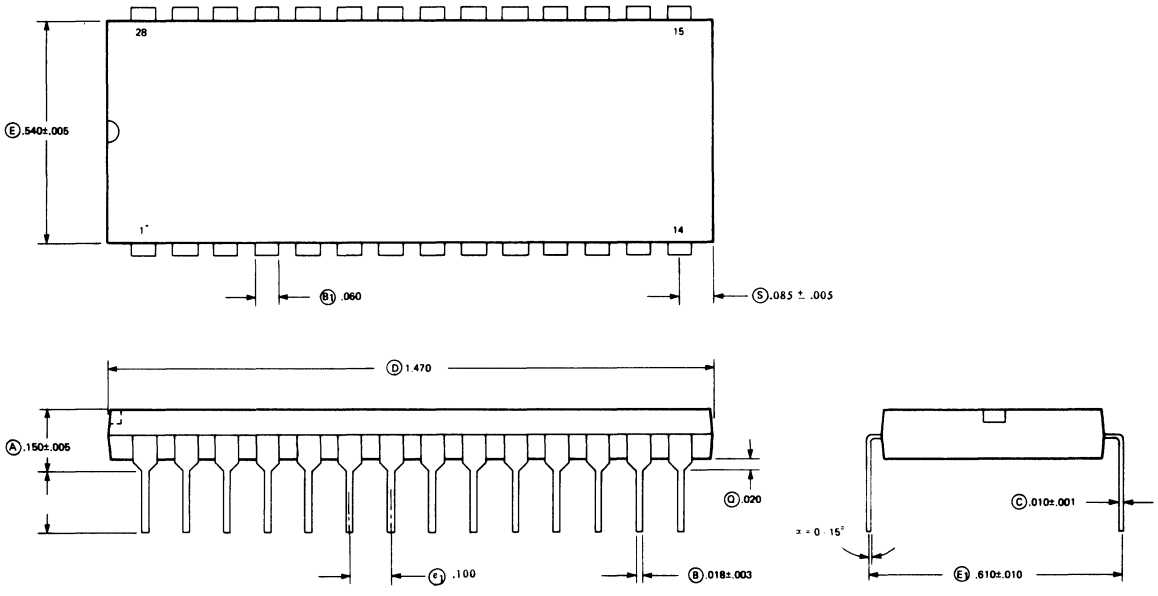


20-Lead Plastic Dual-In-Line Package

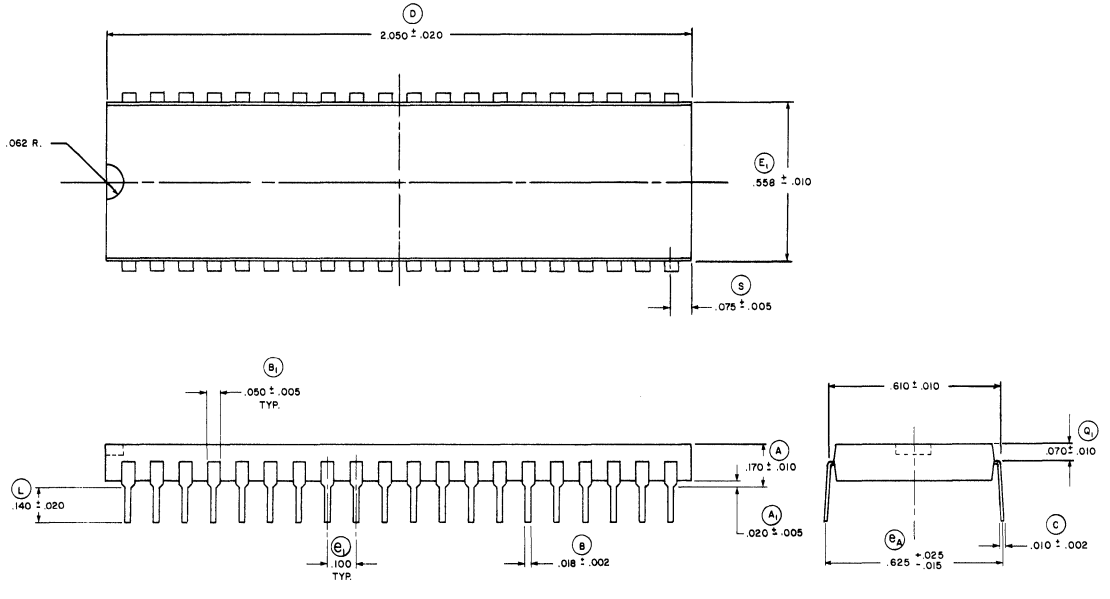


24-Lead Plastic Dual-In-Line Package

Note: Circle (i.e., Ⓑ) indicates JEDEC Reference.

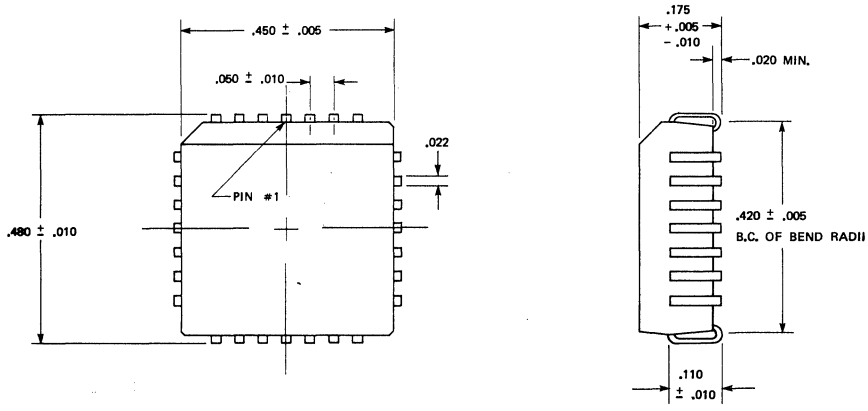


28-Lead Plastic Dual-In-Line Package

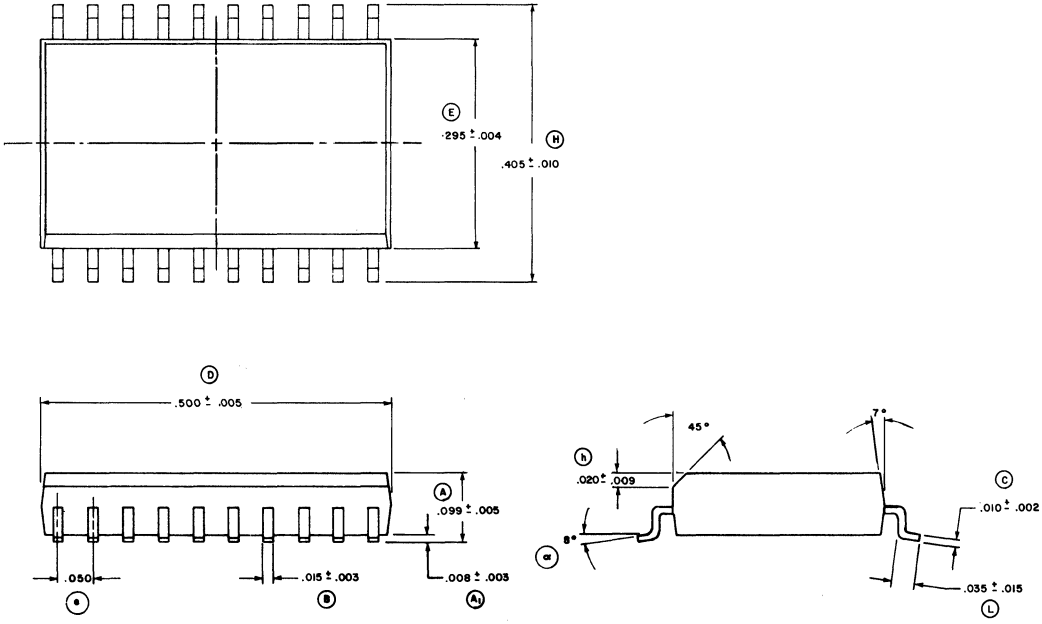


40-Lead Plastic DIP

Note: Circle (i.e., Ⓑ) indicates JEDEC Reference.

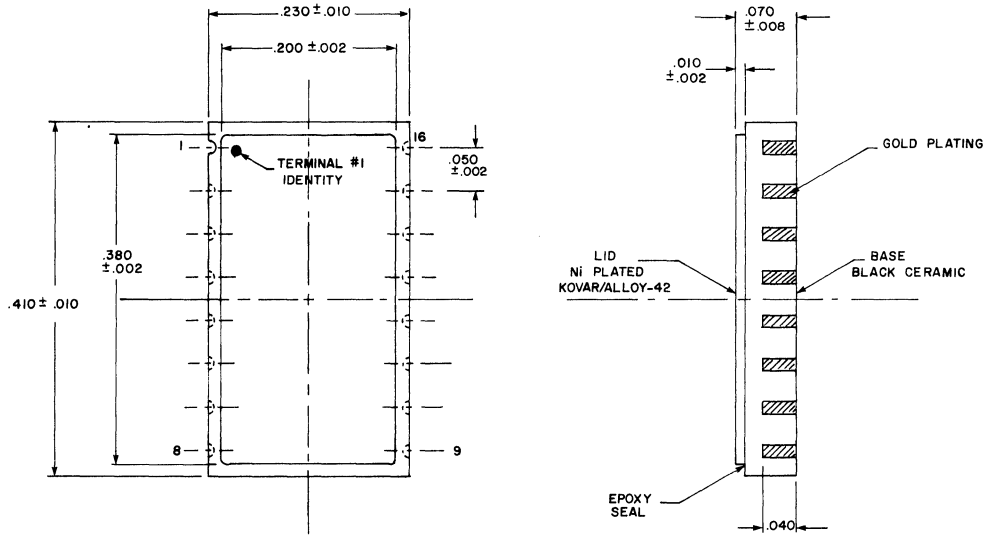


28-Lead Plastic Quad
"J" Bend

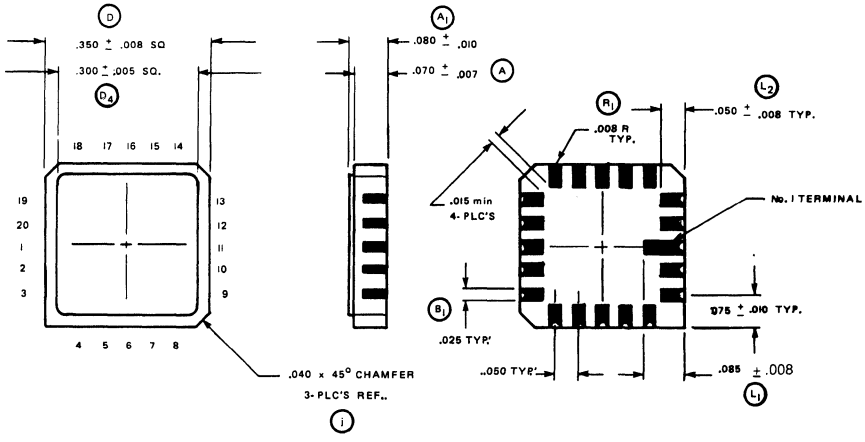


20-Lead SOW Package

Note: Circle (i.e., Ⓑ) indicates JEDEC Reference.

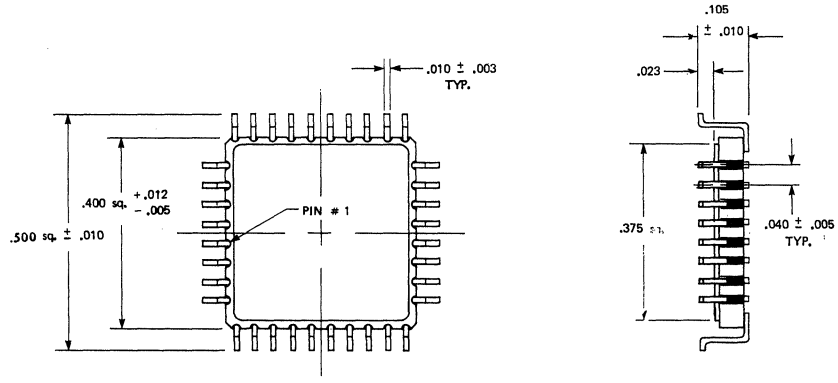


16 Terminal C/C Package

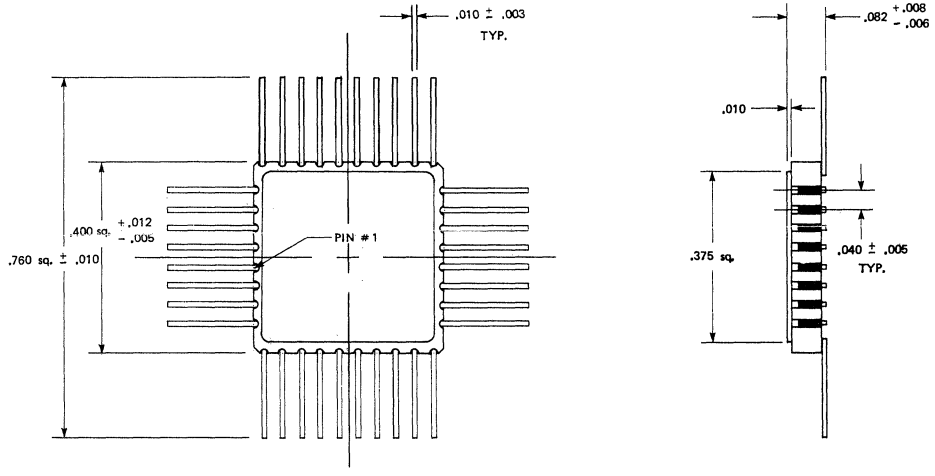


Type "C" Leadless
20-Terminal Chip Carrier

Note: Circle (i.e., Ⓑ) indicates JEDEC Reference.

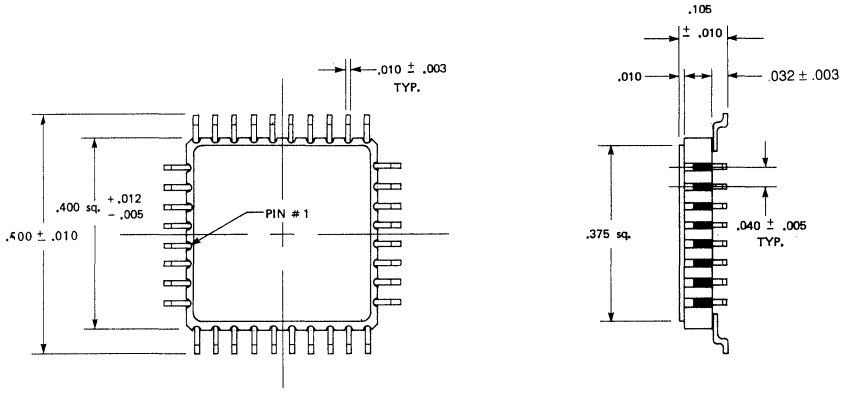


36-Leaded C/C
Bend Option "CR"

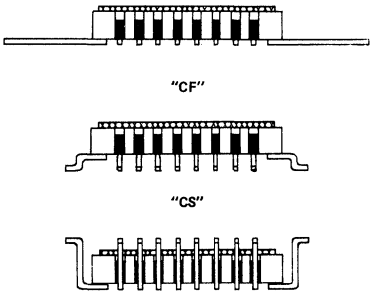


36-Leaded C/C
Bend Option "CF"

Note: Circle (i.e., Ⓑ) indicates JEDEC Reference.



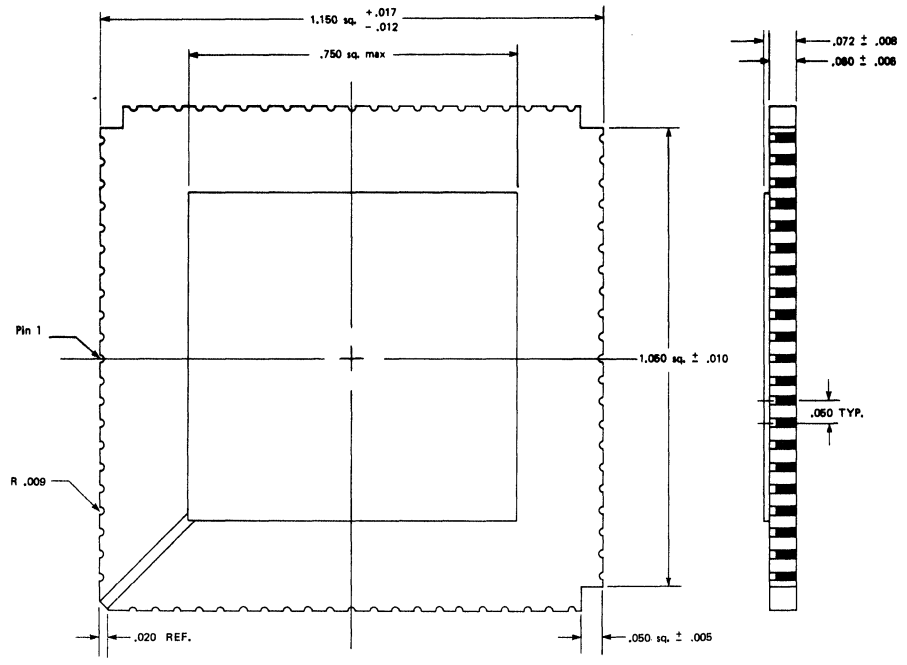
36-Leaded C/C
Bend Option "CS"



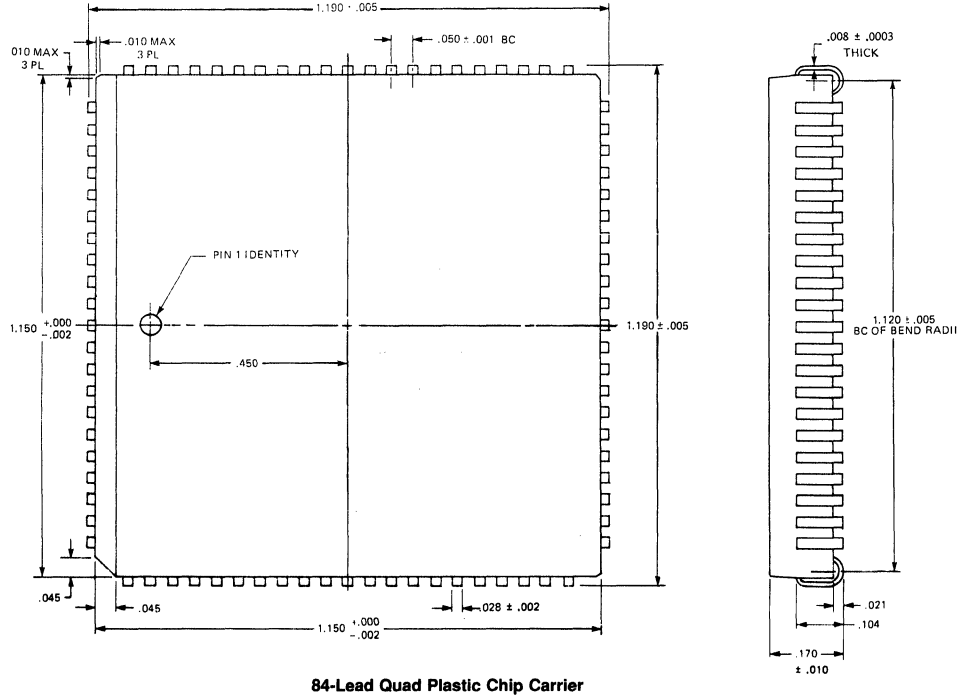
36-Leaded C/C Bend Options
(For detail dimensions refer to package outlines)

14

Note: Circle (i.e., Ⓑ) indicates JEDEC Reference.

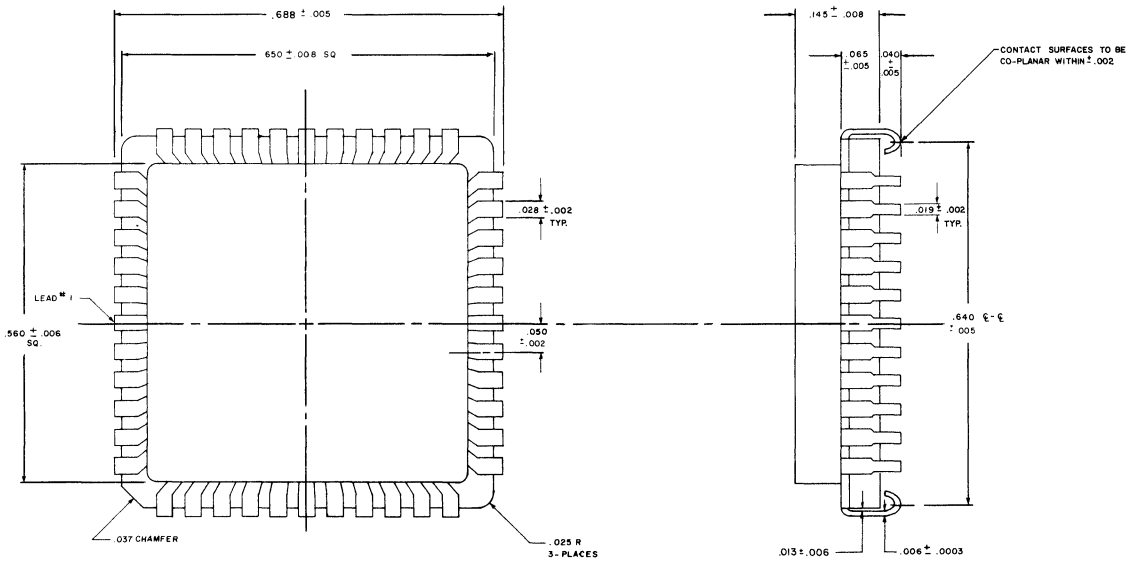


84-Terminal Ceramic C/C
Type "B"

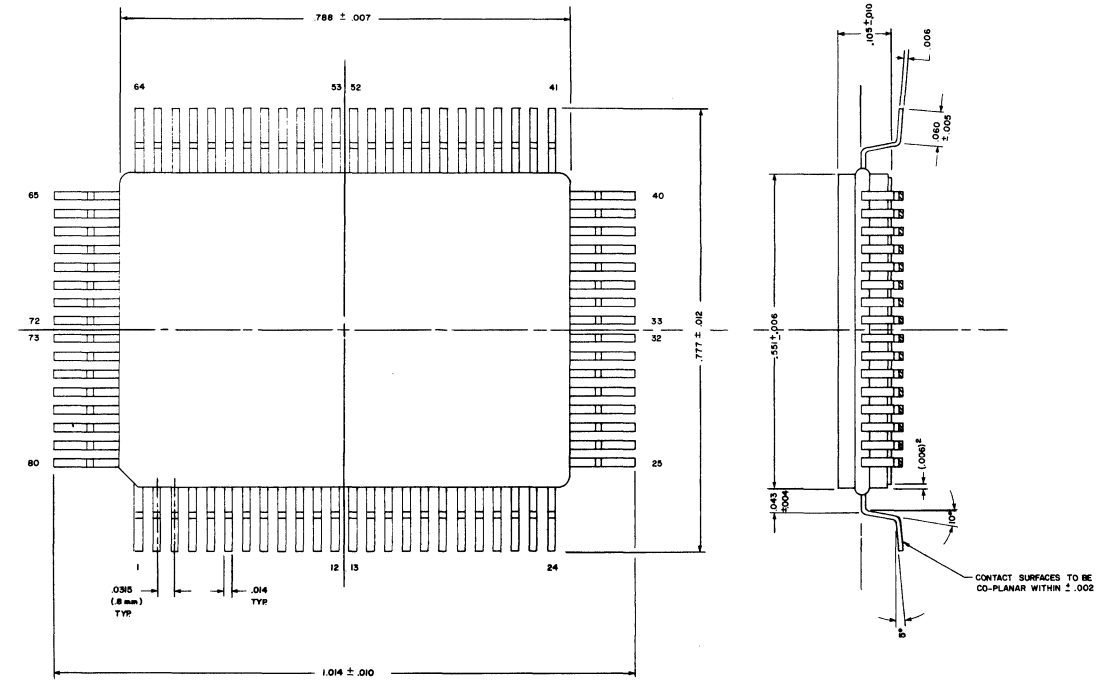


84-Lead Quad Plastic Chip Carrier

Note: Circle (i.e., Ⓑ) indicates JEDEC Reference.



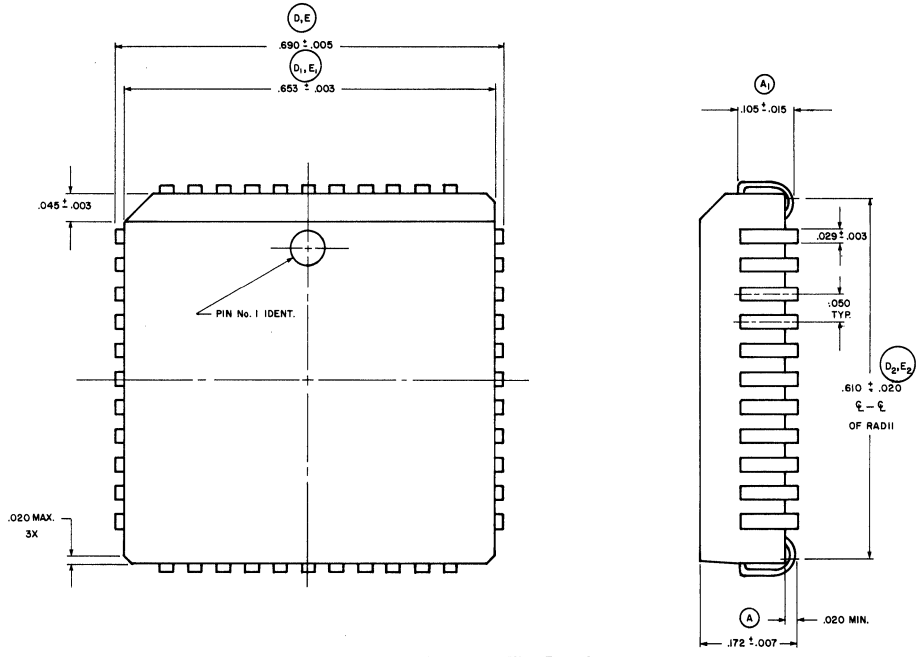
44-Lead Quad CERPAC "DJ" Package



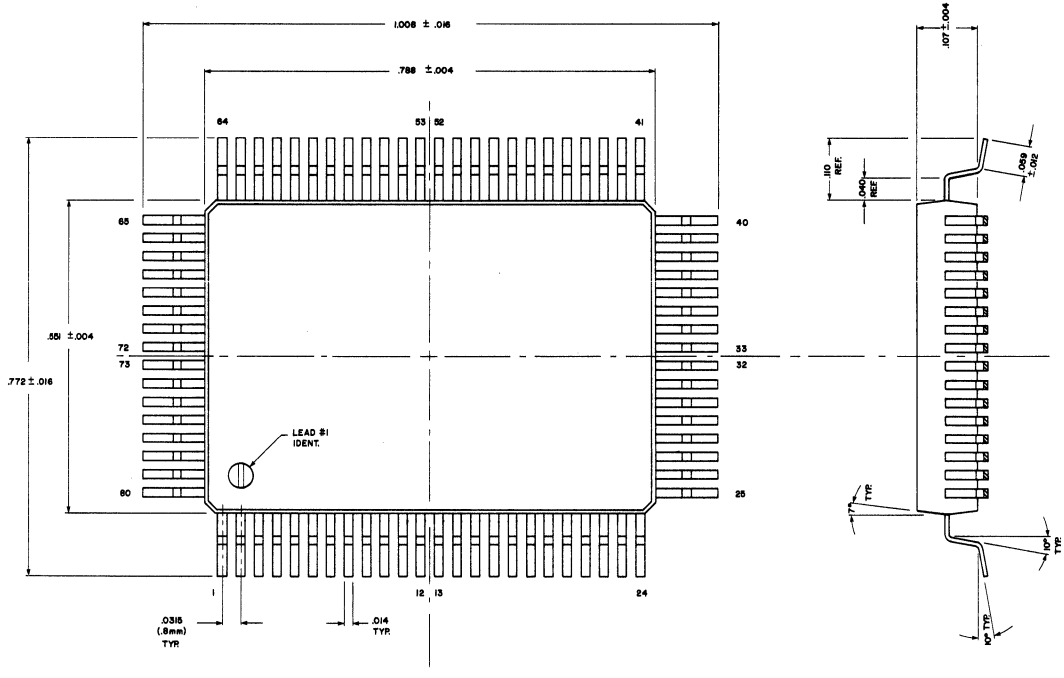
SCALE = 10X

80-Lead Quad CERPAC "DG" Package

Note: Circle (i.e., Ⓑ) indicates SEMI-STANDARD G1.1 STD.1.



44-Lead Plastic "J" - Bend



80-Lead Quad Plastic "PG" Package

Note: Circle (i.e., Ⓑ) indicates JEDEC Reference.

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