16M-Bit (1M X 16/512K X 32) CMOS MASK ROM

FEATURES

- Switchable organization
  524,288 x 32 (double word mode)
  1,048,576 x 16(word mode)
- Fast access time
  Random Access : 100ns (max.)
  Page Access : 30ns(max.)
- Supply voltage : single +5V
- Current consumption
  Operating : 150 mA(max.)
  Standby : 50 μA (max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Polarity programmable chip enable and output enable pin
- Package
  - KM23C16205BSG : 70-SSOP-500

GENERAL DESCRIPTION

The KM23C16205BSG is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 1,048,576x16bit (word mode) or as 524,288x32bit(double word mode) depending on $\overline{WORD}$ voltage level.(See mode selection table)

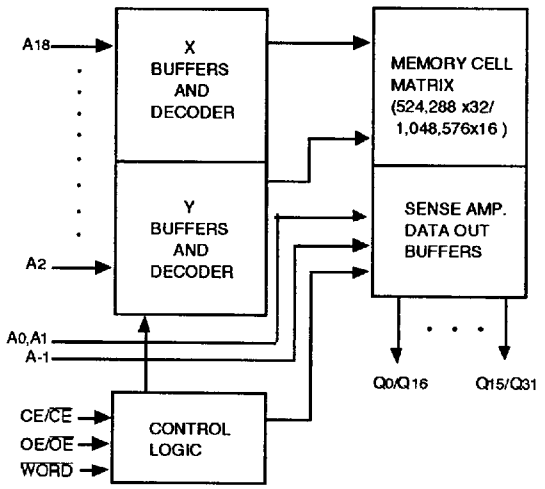
This device includes page read mode function,page read mode allows four to eight words of data to be read fast in the same page,CE and $A_2 \sim A_{18}$ should not be changed.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C16205BSG is packaged in a 70-SSOP and provides polarity programmable CE and OE buffer as user option mode.

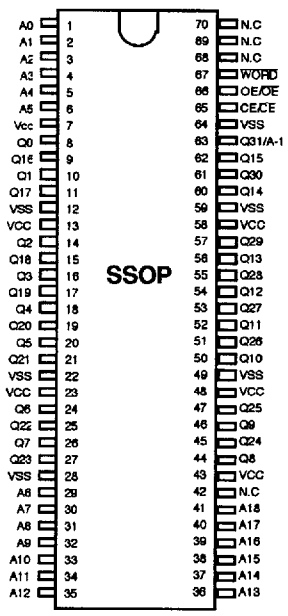
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_1	Page Address Inputs
A_2-A_{18}	Address Inputs
Q_0-Q_{30}	Data Outputs
Q_{31}/A_{-1}	Output 31(Double word mode)/ LSB Address (Word mode)
$\overline{WORD}$	Double word/Word mode selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
Vcc	Power (+5V)
Vss	Ground
N.C	No Connection

* User Selectable Polarity

PIN CONFIGURATION



KM23C16205BSG

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}	-0.3 to +7.0	V
Temperature Under Bias	Tbias	-10 to +85	°C
Storage Temperature	Tstg	-55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	Vss	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}$=$\overline{OE}$=V_{IL}, f=6.7MHz all outputs open	-	150	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}$=V_{IH}, all outputs open	-	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}$=V_{CC}, all outputs open	-	50	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	-	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}	-	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}		-0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}= - 400 μA	2.4	-	V
Output Low Voltage Level	V_{OL}	I_{OL}= 2.1 mA	-	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT} = 0V	-	12	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	-	12	pF

Note : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	WORD	Q_{31}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0~Q_{31}:Dout	Active
		L	Input	Operating	Q_0~Q_{15}:Dout Q_{16}~Q_{30}:Hi-Z	Active

AC CHARACTERISTICS (T_A=0°C to +70°C , Vcc = 5V ±10%, unless otherwise noted.)

TEST CONDITIONS

Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and C_L=100pF

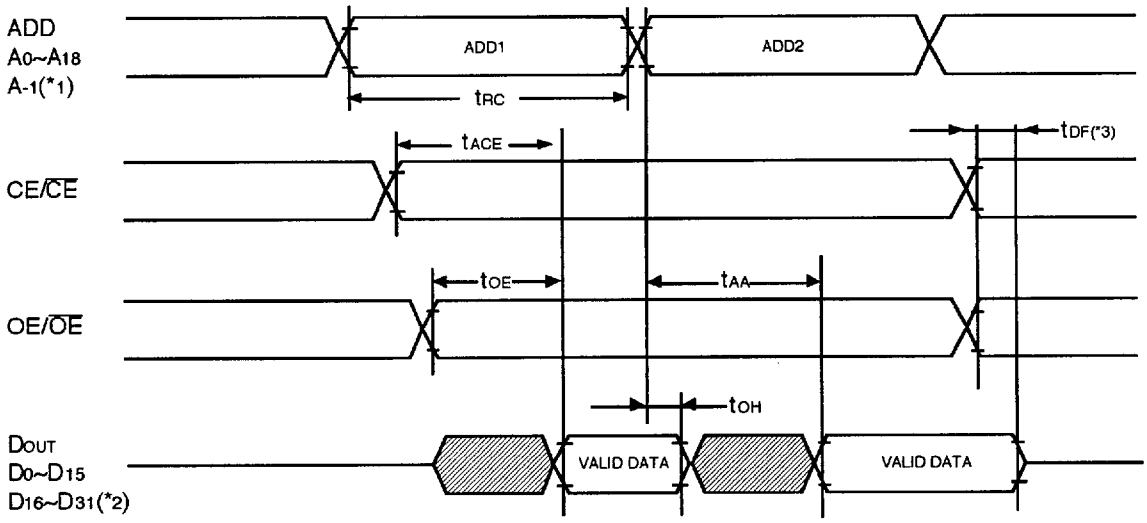
READ CYCLE

Parameter	Symbol	KM23C16205BSG-10		KM23C16205BSG-12		KM23C16205BSG-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	100		120		150		ns
Chip Enable Access Time	tACE		100		120		150	ns
Address Access Time	tAA		100		120		150	ns
Page Address Access Time	tPA		30		50		70	ns
Output Enable Access Time	tOE		30		50		70	ns
Output or Chip Disable to Output High-Z	tDF		20		20		30	ns
Output Hold from Address Change	tOH	0		0		0		ns

* Page Address : A0,A1

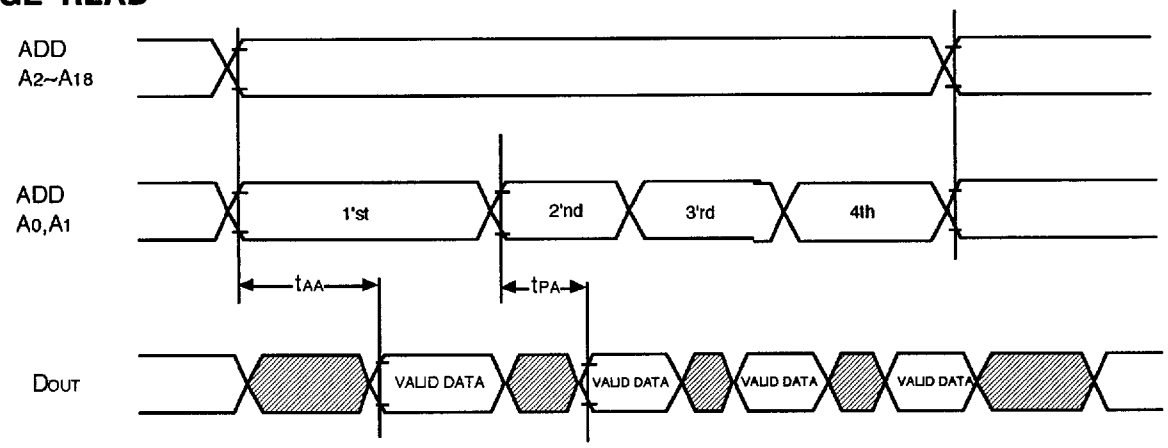
TIMING DIAGRAM

READ



(*1) Word Mode only. A-1 is Least Significant Bit Address.($\overline{WORD}$=VIL)
(*2) Double Word Mode only.($\overline{WORD}$=VIH)
(*3) tDF is defined as the time which the outputs achieve the open circuit condition and is not referenced to VOH or VOL level.

PAGE READ



PACKAGE DIMENSIONS

70 LEAD PLASTIC SHRINK SMALL OUTLINE PACKAGE

Unit : mm/Inches