1996

16M Sync. DRAM

Introduction

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SAMSUNG ELECTRONICS

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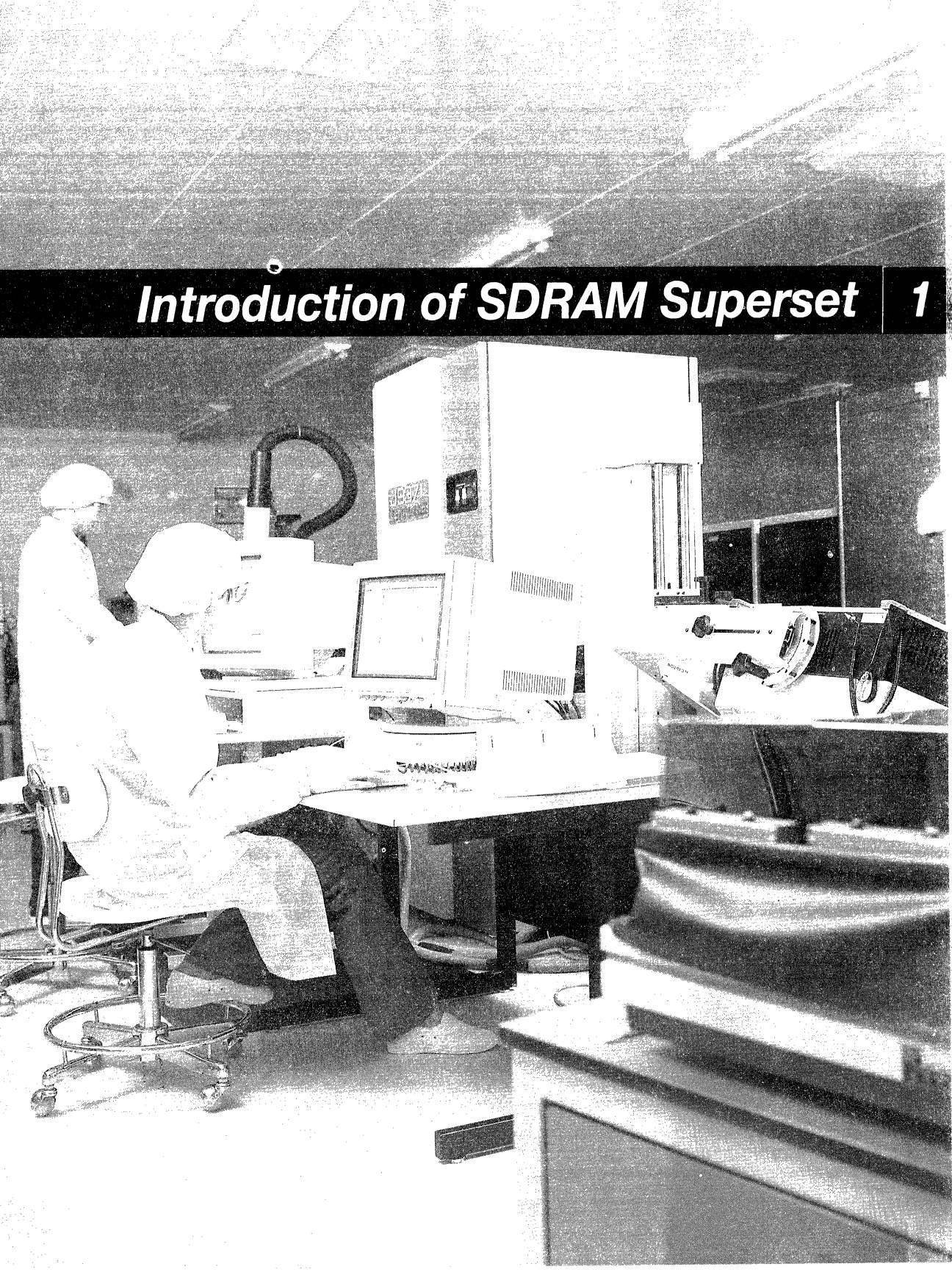
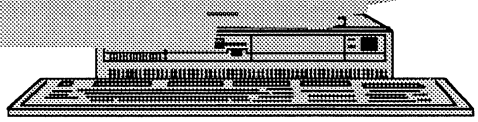
Table of Contents

Introduction of SDRAM Superset 1



SDRAM SUPERSET

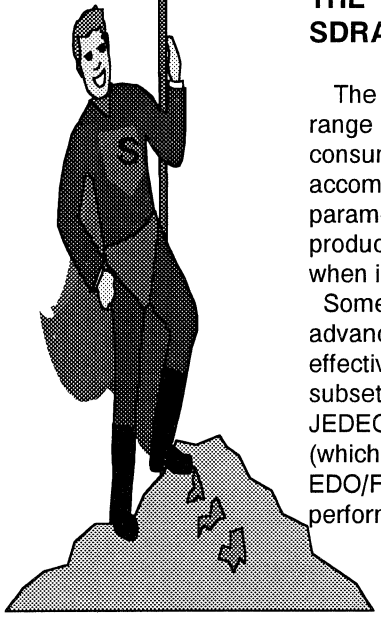


INTRODUCTION

Current PCs are rapidly adopting new technologies such as multi-media, NSP(Native Signal Processing), and UMA(Unified Memory Architecture). Since these technologies require additional memory bandwidth, we have been seeing memory demand shifting away from the long established FP mode DRAM and moving towards EDO.

Lately, several vendors have implemented SDRAM in their systems as the high-bandwidth solution to replace EDO. However, the performance of the current SDRAM (both the "full feature", or JEDEC, version and the "low cost" PC SDRAM version) can not be maximized in today's PCs. Even though SDRAM offers greater functionality and higher frequency operation than EDO, it also has a longer lead-off cycle at 66MHz.

The purpose of this paper is to define the new SDRAM Superset, which revises a few spec parameters to maximize performance. Finally, the infrastructure of the SDRAM is discussed to illustrate the compatibility issues.



THE DEFINITION OF FULL-FEATURE SDRAM AND PC SDRAM

The full-feature SDRAM as defined by JEDEC appeals to a wide range of applications, including mainframe, workstation, PCs, and consumer products. Many programmable options are included to accommodate the various applications (without defining the AC parameters). The added flexibility, however, has resulted in initial products with higher cost and lower speed over alternative solutions when implemented in actual systems.

Some SDRAM manufacturers are introducing the PC SDRAM applied advanced technology and an optimized chip architecture as the cost effective solution for the PC market. This device only offers a specific subset of features and frequency among the full feature set defined by JEDEC. Basically, PC SDRAM eliminates the testing of some features (which are already implemented in silicon) to achieve similar costs as EDO/FP. Unfortunately, PC SDRAM still does not offer significant performance advantages over EDO.

THE DEFINITION OF THE SDRAM SUPERSET

The SDRAM Superset is fully compatible with the full-feature SDRAM while offering improved performance. Also, through advanced manufacturing technology and chip architecture, cost overheads in terms of chip size, test, and yield have been minimized. The SDRAM Superset is intended to be the cost/performance solution for today's high bandwidth requirements.

The SDRAM Superset is obtained from the full feature component by simply modifying certain test parameters. With stable high yields in our current full-feature SDRAM, these parameter modifications result in minimal yield impact. SDRAM Superset test screening is performed with modified values for tRCD, tRP, tSAC and CAS latency. This not only maintains compatibility with the full-feature SDRAM, but also results in a functional superset of both the full-feature and PC SDRAMs. Thus, the SDRAM Superset may be used in all systems that have the ability to control either PC SDRAM or full-feature SDRAM.

The performance of the SDRAM Superset differs from the PC SDRAM and full-feature SDRAM in three specific areas. First, tRCD (RAS to CAS delay time) and tRP (RAS precharge time) of the SDRAM Superset are both equal to 2 clocks, instead of 3 with the others, at 66MHz with the -12 part (run maximally with CAS latency equal to 3). This improvement reduces the number of lead-off cycles during page or row misses.

The second difference is that CAS latency is reduced from 3 to 2 at 66MHz cycle time when given a +10% & -5% V_{DD} tolerance. This maximizes the performance benefits when using the 66MHz bus frequency, which is the mainstream in current PCs.

The third difference is that tSAC (clock to data valid time) is reduced both with and without the reduction of VDD tolerance. The SDRAM Superset makes the speed up for tSAC to allow the system controller to fetch data with sufficient window. This improvement allows additional margin to account for noise and flight time of data. The detailed spec for tSAC is broken down based on CAS latency of the -12 (83MHz) and -10 (100MHz) parts and is shown in table 1.

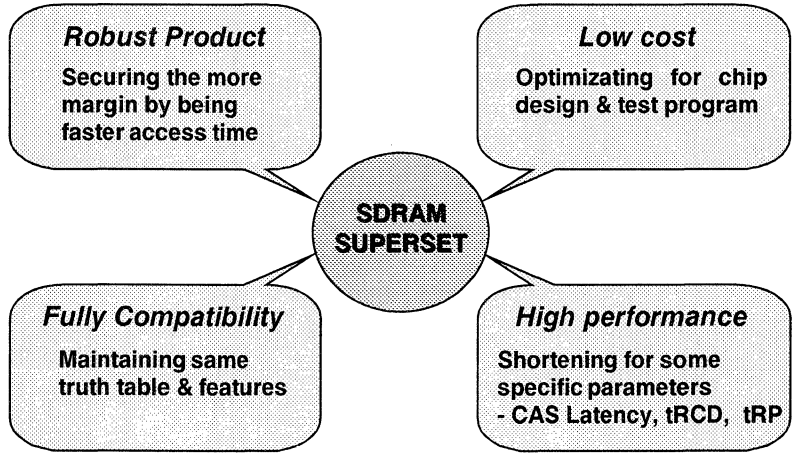


Table 1
SDRAM SUPERSET SPECIFICATION

VDD	Frequency	AC Parameters	**Current SDRAM**	**SDRAM Superset**	Note
3.3V ± 0.3V	-12 (83MHz)	tCC (Min. cycle time)/ Max. Frequency @CL = 2	18ns / 55MHz	15ns / 66.7MHz	*1
		tRP @ CL = 2	36ns (3 Clocks)	30ns (2 Clocks)	*2
		tRCD @ CL = 2	36ns (3 Clocks)	30ns (2 Clocks)	*2
		tSAC @ CL = 2	13ns	10ns	*3
	-10 (100MHz)	tSAC @ CL = 2 tSAC @ CL = 3	11ns 8.5ns	9.5ns 8ns	*3
3.3V +0.3/- 0.15V	-12 (83MHz)	tSAC @CL = 2	13ns	9.5ns	*3
	-10 (100MHz)	tSAC @ CL = 2	11ns	9.0ns	*3

*1 : New -12 part can meet 66MHz Bus @ CL = 2
*2 : New -12 part can meet 2 clocks tRCD and tRP @ 66MHz
*3 : tSAC Speed up for larger data setup time of the contoller in new data sheet

WHY THE SDRAM SUPERSET IS THE BEST SOLUTION FOR PC APPLICATIONS WITH 66MHz BUS FREQUENCY

There are four main advantages that make the SDRAM Superset a superior solution over EDO and PC SDRAM: Higher performance than PC SDRAM and EDO, good compatibility with full-feature SDRAM and PC SDRAM, relaxed timing constraints, and future upgradability.

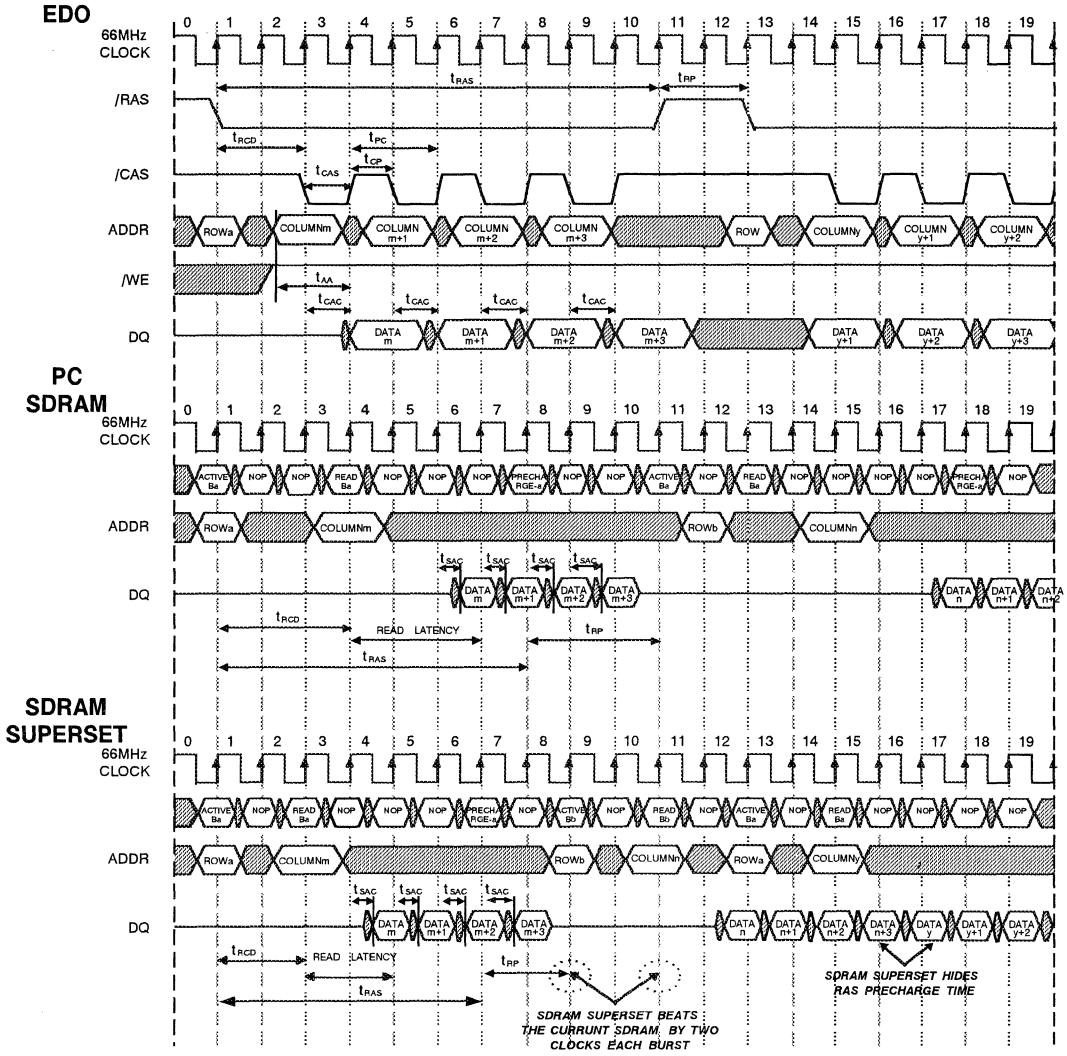
HIGHER PERFORMANCE THAN PC SDRAM AND EDO

When the current SDRAM is used for 66MHz PC main memory applications, the system is able to perform no-wait burst cycles compared to one-wait of EDO. However, the lead-off cycle time for the PC SDRAM and full-feature SDRAM can't be reduced, so the lead-off cycle time of those products are further burdened compared to SDRAM Superset. When the SDRAM Superset is used instead of PC SDRAM or EDO, system performance is improved by five to ten percent because the system is reduced by one, two and three clock cycles for the cases of a Page Hit, Row Miss, and Page Miss, respectively in terms of the lead-off cycle tiem.

Page Hit : Save 1 Clock Cycle → CAS Latency
Row Miss : Save 2 Clock Cycle → CAS Latency + tRCD
Page Miss : Save 3 Clock Cycle → CAS Latency + tRCD + tRP

<Table 2> shows more detail on the performance imporvements obtained with the SDRAM Superset over competing products when implemented in the chipset that supports SDRAM.

Figure 1
TIMING COMPARISON



GOOD COMPATABILITY WITH PC SDRAM AND FULLY COMPATIBLE WITH FULL FEATURE SDRAMS

The SDRAM Superset includes the current SDRAM features and fully supports the JEDEC Truth Table. Some AC parameters have been improved and these can be taken advantage of through appropriate implementation in actual systems. System vendors should easily be able to use the SDRAM Superset with the improved AC parameters if the programmable BIOS is properly set. And since PC SDRAM is a subset of the SDRAM Superset, no change in hardware architechtrure is required.

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Table 2
MEMORY CYCLE ANALYSIS BASED ON 66MHz BUS FREQ.

Chipset		Chipset A		Chipset B
Support MODE		SDRAM / EDO / FP		EDO / FP
Number of Cycle	Mode	SDRAM	EDO	EDO
	Page Hit	7 - 1 - 1 - 1	6 - 2 - 2 - 2	5 - 2 - 2 - 2
	Row Miss	10 - 1 - 1 - 1	9 - 2 - 2 - 2	8 - 2 - 2 - 2
	Page Miss	13 - 1 - 1 - 1	12 - 2 - 2 - 2	11 - 2 - 2 - 2
	Back to Back Page Hit	7 - 1 - 1 - 1 - 2 - 1 - 1 - 1	6 - 2 - 2 - 2 - 3 - 2 - 2 - 2	5 - 2 - 2 - 2 - 2 - 2 - 2 - 2
Based Condition		tRCD = 3, CL = 3	tRCD = 2, CL = 2	tRCD = 2, CL = 2

Easy of implementation

SAMSUNGs Guess

If using -12 part based on new specification @ tSAC = 10ns **(tRCD = 2,** CL = 3, tRP = 2 Clocks)

Page Hit	**7** - 1 - 1 - 1
Row Miss	**9** - 1 - 1 - 1
Page Miss	**11** - 1 - 1 - 1
Back to Back Page Hit	**7** - 1 - 1 - 1 - 2 - 1 - 1 - 1

(Saving the lead-off cycle @ Miss)

If using -12 part based on new specification @ tSAC = 9.5ns **(tRCD = 2, CL = 2, tRP = 2 Clocks)**

Page Hit	**6** - 1 - 1 - 1
Row Miss	**8** - 1 - 1 - 1
Page Miss	**10** - 1 - 1 - 1
Back to Back Page Hit	**6** - 1 - 1 - 1 - 2 - 1 - 1 - 1

(Saving the lead-off cycle @ all case)

If we assume that advanced conto-ller integrated the external data buffer can support SDRAM **(tRCD = 2, CL = 2, tRP = 2 Clocks)**

Page Hit	**5** - 1 - 1 - 1
Row Miss	**7** - 1 - 1 - 1
Page Miss	**9** - 1 - 1 - 1
Back to Back Page Hit	**5** - 1 - 1 - 1 - 2 - 1 - 1 - 1

(Saving the burst cycle)

TIMING CONSTRAINT RELAXATION

Even though EDO, PC SDRAM and the full feature SDRAM can operate with 66MHz cycle time it is very difficult to perform no-wait burst cycles due to timing constraints caused by clock skew and data flight time in actual systems. In order to achieve 66MHz without the wait, reasonable access time, set-up time, and data window margin should be considered. The relationship among these parameters is as follows,

$$tSAC \leq tCC - tSKEW - tSC$$

$$tWindow = tCC - tSAC - tSKEW + tOH$$

* tSKEW : Including the clock skew and data flight time
* tSC : Controller set-up time

When the SDRAM Superset spec value are put in the above equation, the timing constraint is more relaxed than the others due to shortening of the access time from clock.

FUTURE UPGRADABILITY

Currently, SDRAM vendors are introducing the 100MHz SDRAM into the market. The next versions will achieve upto 150MHz by using advanced processes, additional pipelining, and prefetch architectures in combination with a high speed interface such as SSTL.

In the next few years, we can expect to see SDRAMs with frequencies over 200 or 300MHz being introduced by many memory vendors. Therefore, SDRAM has excellent potential to cope with the ever increasing system performance trend.

Table 3
TARGET SPEC FOR BEYOND 100MHz

Item	125MHz	150MHz	200MHz
CL (CAS Latency)	4 Clock	4 Clock	5 Clock
tCC (Clock cycle time)	8ns	7ns	5ns
tSAC (Output valid time)	6ns	5ns	3ns
tSS (Set-up time)	3ns	2.5ns	2ns
tOH (Output hold time)	2ns	2ns	1ns

SDRAM SUPPORT INFRASTRUCTURE

SDRAM is not compatible with EDO/FP DRAM due to different pin configurations and the addition of pins such as Clock, DQM, and others. The compatability issue must be addressed before SDRAM can achieve significant market penetration. SDRAM vendors need to construct an infrastructure that can support not only EDO and FP, but also SDRAM in order to win over system vendors and end-users.

The pinout for the new 168pin DIMM standard supports maximal compatibility among modules with different types of DRAM on board. Consequently, it is necessary for SDRAM to move from SIMM to DIMM and to obtain the needed chipset support. Most of chipset vendors will be shipping controllers that support SDRAM very soon.

SDRAM MODULES

Currently, the 200pin DIMM for WSs have been standardized, while the 144pin SO-DIMM for mobile computers and the 168pin unbuffered DIMM are in the process of standardization. Memory vendors are working on minimizing the signal skew and noise when the 168pin unbuffered DIMM is implemented in systems. This effort should result in a robust and practical SDRAM DIMM. Furthermore, with the addition of SPD (Serial Presence Detect) on the module, system vendors are able to obtain detailed information of the memory on the DIMM. The controller can now read the SPD and then set its internal registers appropriately (with the assistance of information in the BIOS). Configuration settings such as refresh, latency and others may be optimized for each DIMM. Therefore, the end-user can perform Plug & Play through the controller's auto-detection mechanisms. This will make it more convenient for customers to use the SDRAM Superset as well as the full-feature SDRAM to their full advantage.

SDRAM CONTROLLER

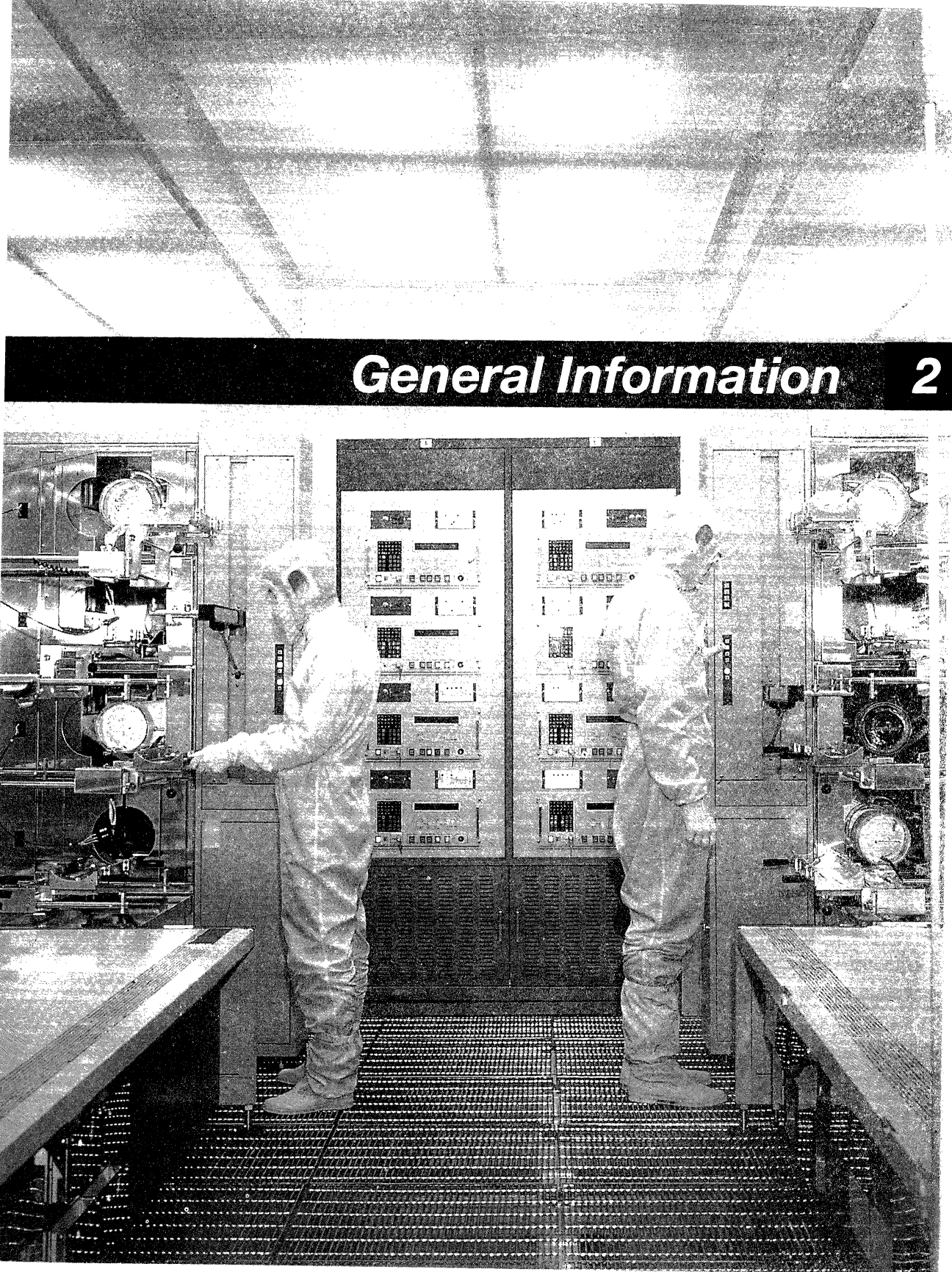
Most of the controller manufactures (Intel, Opti, VLSI, VIA, SIS, UMC, ALI, ACC, PicoPower, and etc.) plan to ship SDRAM controllers starting from 2Q '96. The first SDRAM controllers will be for Pentium class processors and controllers for Pentium Pro will follow. Current DRAM controllers are able to automatically detect the type of memory installed in the system during the initialization cycle, and different types of DRAM can be mixed in different banks because the DRAM controller is fully configurable through a set of control registers .

VHDL AND VERILOG MODEL SUPPORT

Samsung has distributed the VHDL and Verilog models for our current SDRAM to customers and PC core chipset manufacturers. Samsung will also soon make available the revised models for the SDRAM Superset.

The next generation SDRAM should be able to operate in real systems at 100MHz. The higher frequency will place many new design constraints. We are open to close cooperation with customers and chipset manufacturers for definition of a practical and robust SDRAM at 100MHz and beyond. We believe that close cooperation is mandatory to derive the right solution. If you need any assistance or are interested in future discussions, please contact the Samsung sales office or marketing department in your area.

General Information 2



16M SDRAM(2nd Gen.) AC Spec. Change Notice

- Purpose : To improve SDRAM performance compared to EDO DRAM.
  (New data sheet will be available at late March '96).

- AC Parameters revised.

		-10 Part		-12 Part	
		Previous	New	Previous	New
tCC	CL= 3	10ns	10ns	12ns	12ns
	CL= 2	15ns	15ns	18ns	15ns
	CL= 1	30ns	30ns	36ns	30ns
tSAC	CL= 3	8.5ns	8.0ns *1	9.0ns	9.0ns
	CL= 2	11ns	9.5ns *2	13ns	10ns *3
	CL= 1	27ns	27ns	32ns	27ns
tOH		3.5ns	3.0ns	3.5ns	3.0ns
tRP		30ns	26ns	36ns	30ns
tRAS		70ns	60ns	72ns	66ns
tRC		100ns	96ns	108ns	100ns
tRCD		30ns	26ns	36ns	30ns

(Note) *1 : In case of x4 & x8, tSAC is euqal to 7.5ns without change from current Spec.
*2 : tSAC = 9ns in 3.3V +0.3V/-0.15V, tSAC= 9.5ns in 3.3V +/-0.3V
*3 : tSAC = 9.5ns in 3.3V +0.3V/-0.15V, tSAC = 10ns in 3.3V +/-0.3V

⇨ *Samsung -12 part can support 66MHz bus frequency. (with CL=2 & 3)*
Samsung -10 part can support 83MHz & 75MHz bus frequency.

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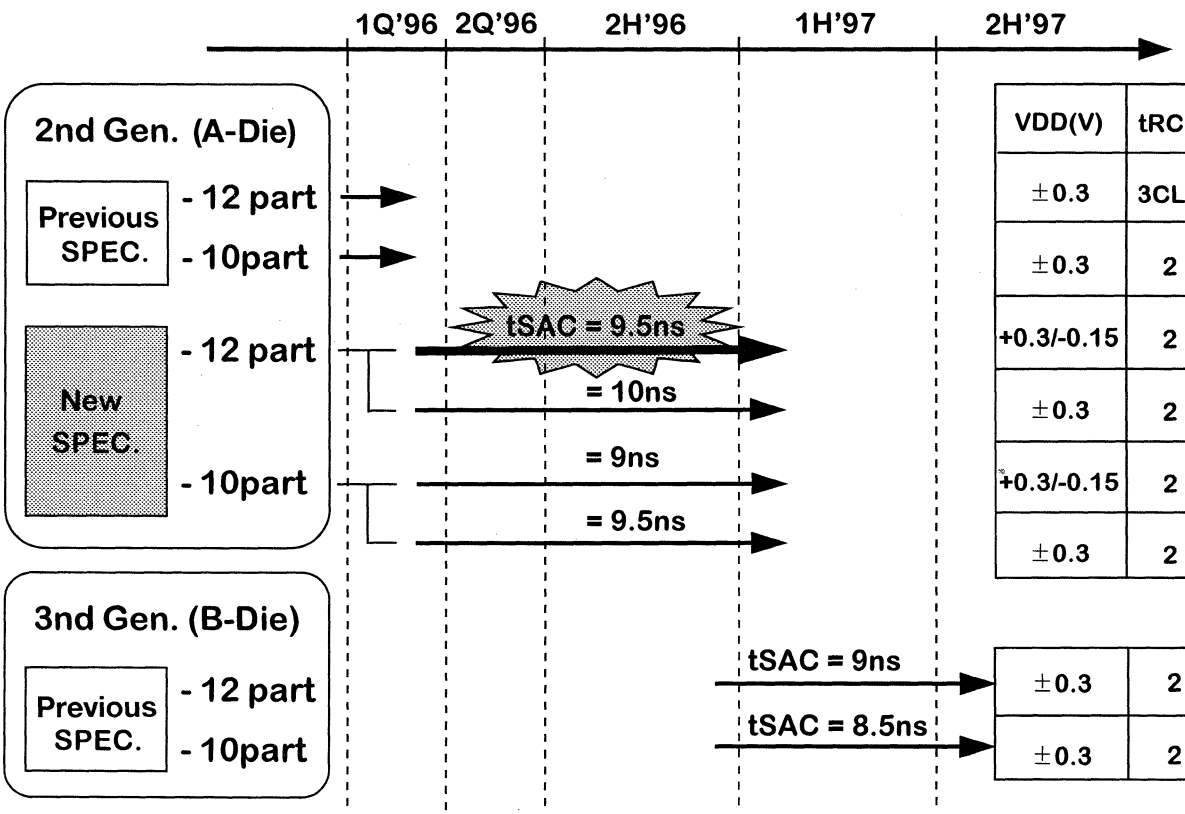
16M SDRAM Support Plan for 66MHz System



VDD(V)	tRCD	CL	tRP
±0.3	3CLK	3CLK	3CLK
±0.3	2	3	3
+0.3/-0.15	2	2	2
±0.3	2	2	2
+0.3/-0.15	2	2	2
±0.3	2	2	2
±0.3	2	2	2
±0.3	2	2	2

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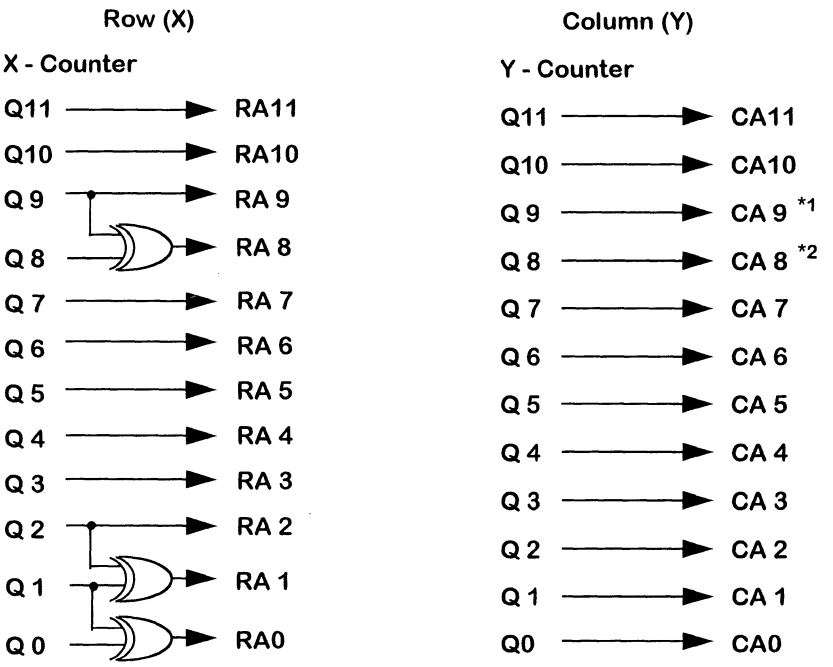
Address Descramble Logic



*1 : N.C in case of x8/x16

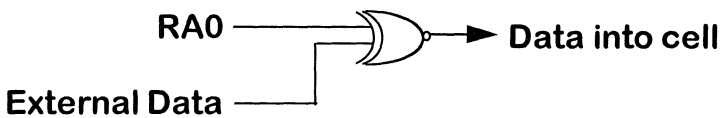
*2 : N.C in case of x16

Data Scramble Logic

RA0	T/C	External Data	Data in cell
0	C	0	1
		1	0
1	T	0	0
		1	1

T : True cell

C : Compliment cell



Product Feature & Line-up Plan

	16M 2nd (A-die)	16M 3rd (B-die)	64M 2nd (A-die)	Note
Organization	x4 / x8 / x16	x4 / x8 / x16	x4 / x8 / x16	
# of Bank	2	2	4	
Address Information	Row : RA0~RA10 (RA11) Col. : CA0~CA9 (CA11) @ x4 CA0~CA8 (CA11) @ x8 CA0~CA7 (CA11) @ x16	Row : RA0~RA10 (RA11) Col. : CA0~CA9 (CA11) @ x4 CA0~CA8 (CA11) @ x8 CA0~CA7 (CA11) @ x16	Row : RA0~RA11 (RA12,RA13) Col. : CA0~CA9 (CA12,CA13) @ x4 CA0~CA8 (CA12,CA13) @ x8 CA0~CA7 (CA12,CA13) @ x16	( ) : Bank Select Address
Min. Cycle time (Max. Frequency)	LVTTL: 12ns (83MHz) LVTTL: 10ns (100MHz) SSTL is not supported.	LVTTL: 12ns (83MHz) LVTTL: 10ns (100MHz) LVTTL: 9ns (111MHz) SSTL: 8ns (125MHz) SSTL: 7ns (143MHz)	LVTTL: 12ns (83MHz) LVTTL: 10ns (100MHz) LVTTL: 9ns (111MHz) SSTL: 8ns (125MHz) SSTL: 7ns (143MHz)	
Refresh (Auto & Self)	4K/64ms @ x4/x8 2K/32ms @ x16	4K/64ms @ x4/x8/x16	4K/64ms @ x4/x8/x16	
Self-refresh current (Icc6)	Normal (-G) : 2mA Low-power(-F) : 250uA	Normal (-G) : 2mA Low-power(-F) : 250uA	Normal (-G) : 2mA Low-power(-F) : 250uA	
Package	44 TSOP II @ x4/x8 50 TSOP II @ x16	44 TSOP II @ x4/x8 50 TSOP II @ x16	54 TSOP II @ x4/x8/x16	
Availability	Production Now	- E/S : 3Q '96 - C/S : 4Q '96	- E/S : 3Q '96 - C/S : 1Q '97	

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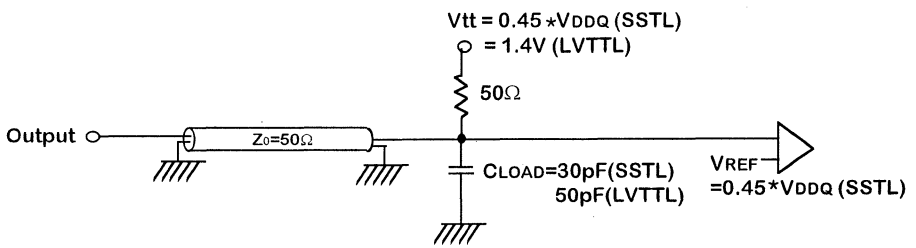
LVTTL vs. SSTL Comparison

Parameter	Symbol	LVTTL			SSTL			Unit	Notes
		Min	Typ	Max	Min	Typ	Max		
Device Supply Voltage	V_{DD}	3.0	3.3	3.6	V_{DDQ}	-	3.6	V	
Output Supply Voltage	V_{DDQ}	3.0	3.3	3.6	3.0	3.3	3.6	V	
Input Reference Voltage	V_{REF}	-	-	-	1.3	1.5	1.7	V	*
Termination Voltage	Vtt	-	-	-	V_{REF}-0.05	V_{REF}	V_{REF}+0.05	V	*
Input Logic High Voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V_{REF}+0.2	-	V_{DDQ}-0.05	V	
Input Logic Low Voltage	V_{IL}	-0.3	0	0.8	-0.3	-	V_{REF}-0.2	V	
Output High Voltage	V_{OH}	2.4	-	-	Vtt+0.8	-	-	V	Ioh = -16mA
Output Low Voltage	V_{OL}	-	-	0.4	-	-	Vtt-0.8	V	Iol = 16mA
Input Leakage Current	I_{IL}	-5	-	5	-5	-	5	uA	
Output Leakage Current	I_{OL}	-5	-	5	-5	-	5	uA	

* : This parameter is defined only for SSTL.



Output Load Circuit

SDRAM Module Line-up Plan

Common Feature

- Damping resistors : 22 Ohm per DQ line.
- Support SPD (Serial Presence Detect), but Need to modify in the next JEDEC.
- Adapt SDRAM component AC specification.

. Line-up Plan

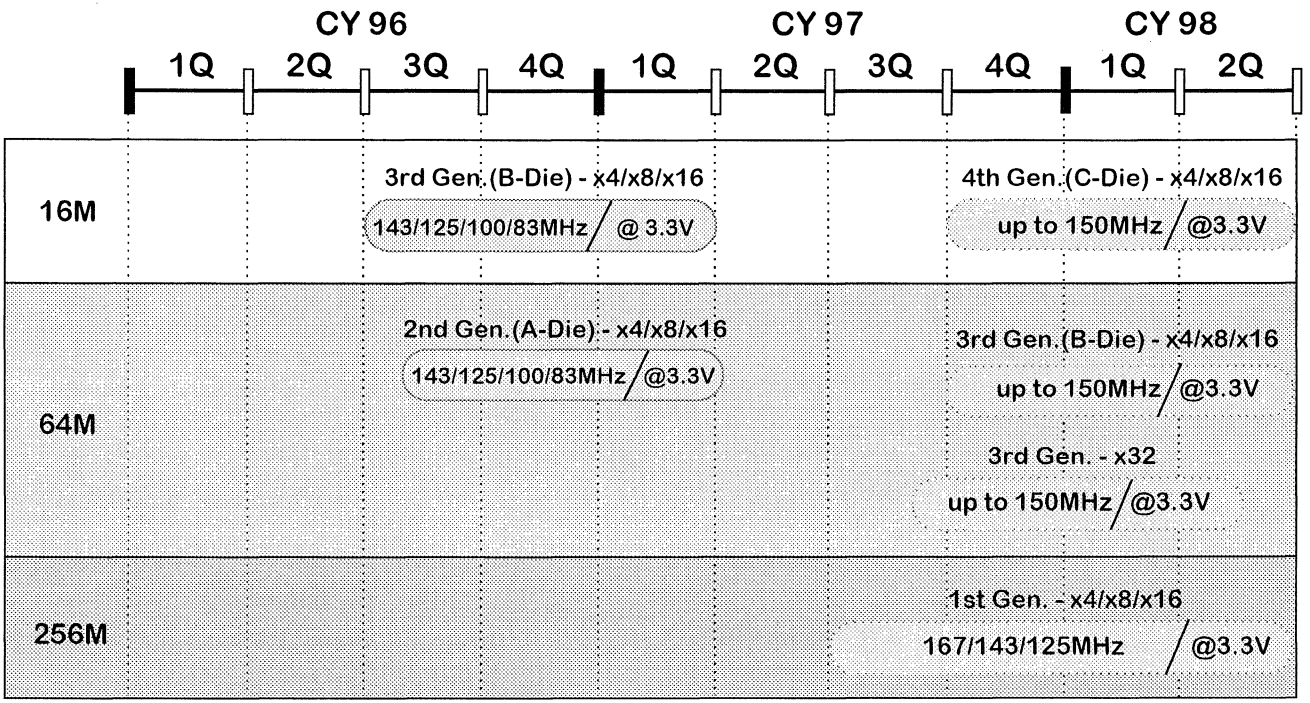
- 8 Byte DIMM

Org.	Part Number	Based Comp.	# of bank	PCB Feature	E/S	C/S
1Mx64	KMM366S114AT-G0/G2	1Mx16	1	Single sided & 1,000mil	Now	Mar.'96
2Mx64	KMM366S203AT-G0/G2	2Mx8	1	Double sided & 1,000mil	Now	Mar.'96
	KMM366S203AT1-G0/G2	2Mx8	1	Single sided & 1,250mil	Now	2Q '96
4Mx64	KMM366S400AT-G0/G2	4Mx4	1	Double sided & 1,250mil	Now	Mar.'96
	KMM366S403AT1-G0/G2	2Mx8	2	Double sided & 1,250mil	Now	Apr.'96
2Mx72/ECC	KMM374S203AT1-G0/G2	2Mx8	1	Single sided & 1,250mil	Now	2Q '96
4Mx72/ECC	KMM374S403AT1-G0/G2	2Mx8	2	Double sided & 1,250mil	Now	2Q '96

- 8 Byte SODIMM

Org.	Part Number	Based Comp.	# of bank	PCB Feature	E/S	C/S
1Mx64	KMM466S114AT-G0/G2	1Mx16	1	Single sided & 1,250mil	Apr.'96	May.'96
2Mx64	KMM466S203AT-G0/G2	2Mx8	1	Double sided & 1,250mil	Apr.'96	May.'96
	KMM466S214AT-G0/G2	1Mx16	2	Double sided & 1,250mil	Apr.'96	May.'96

SDRAM Roadmap



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SDRAM Component Ordering Information

KM	4	XX	S	XX	X	X	X	X	X -	X	XX
		I	II	III	IV	V	VI	VII	VIII	IX	X

I . Organization
4 : x4, 8 : x8, 16 : x16

II . Feature
S : SDRAM

III . Density
1 : 1M, 2 : 2M, 4 : 4M
8 : 8M, 16 : 16M

IV . Refresh
0 : 4K, 1 : 2K, 2 : 8K

V . # of Bank
2 : 2 Banks, 3 : 4 Banks

VI. Interface
0 : LVTTL, 1 : SSTL

VII. Revision
Blank : 1st, A : 2nd, B : 3rd

VIII. Package
T : TSOP II (400mil)

IX . Power
G : Auto & Self refresh
F : Auto & Self refresh with Low-power

X . Min. cycle time (Max. Frequency)
07 : 7ns (143MHz)
08 : 8ns (125MHz)
09 : 9ns (111MHz)
10 : 10ns (100MHz)
12 : 12ns (83MHz)

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SDRAM Module Ordering Information

KM	M	X	XX	X	X	X	X	X	X	X	-	X	XX
		(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)		(10)	(11)

(1) Module type
3 : 8_Byte DIMM, 4 : 8_Byte SODIMM

(2) Data bits
66 : x64 Unbuffered DIMM with SPD
74 : x72ECC Unbuffered DIMM with SPD

(3) Feature
S : SDRAM

(4) Density
1 : 1M, 2 : 2M, 4 : 4M, 8 : 8M

(5) Refresh
0 : 4K, 1 : 2K, 2 : 8K

(6) Composition component
0 : x4, 3 : x8, 4 : x16

(7) Component revision
Blank : 1st, A : 2nd, B : 3rd

(8) Package
T : TSOP II (400mil)

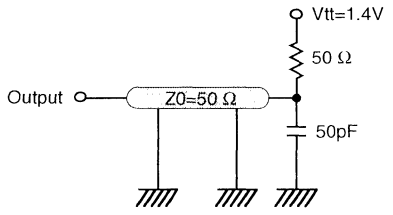
(9) PCB revision
Blank : 1st, 1 : 2nd

(10) Power
G : Auto & Self refresh
F : Auto & Self refresh with Low-power

(11) Min. cycle time (Max. Frequency)
7 : 7ns (143MHz), 8 : 8ns (125MHz)
9 : 9ns (111MHz), 0 : 10ns (100MHz)
2 : 12ns (83MHz)

Specification 3

Revision History

Items	*BEFORE REVISION (Oct. 1995)*	*AFTER REVISION (Mar. 1996)*
Device binning	**-10 / - 12 / - 13**	**-10 / - 12**
Decoupling Cap. guide line	$C_{DC1} = C_{DC2} = 0.1 + 0.01uF$	$C_{DC1} = C_{DC2} = 0.1^*$ 2 uF @x4/x8 $C_{DC1} = C_{DC2} = 0.1^*$ 3 uF @x16
AC output load circuit	RC load (refer to specification)	
AC parameters @ -10 / -12		
tRCD	30 / 36 ns	26 / 30 ns
tRP	30 / 36 ns	26 / 30 ns
tRAS(min)	70 / 72 ns	60 / 66 ns
tRC	100 / 108 ns	96 / 100 ns
tOH @x16	3.5 / 3.5 ns	3 / 3 ns
tSRX	10 / 10 ns	- (Not defined)
tCC CAS Latency = 3	10 / 12 ns	10 / 12 ns
tCC CAS Latency = 2	15 / 18 ns	15 / 15 ns
tCC CAS Latency = 1	30 / 36 ns	30 / 30 ns
tSAC CAS Latency = 3	7.5 [*1] / 9 ns	7.5 [*1] / 9 ns
tSAC CAS Latency = 2	11 / 13 ns	9.5 [*2] / 10 ns [*3]
tSAC CAS Latency = 1	27 / 32 ns	27 / 27 ns
	* Note ; 1. In case of x16, tSAC is 8.5 ns @CL=3. - (Not defined)	* Note ; 1. In case of x16, tSAC is 8 ns @CL=3. 2. If $3.15V \leq V_{DD} \leq 3.6V$, tSAC = 9ns can be met @CAS latency = 2 of -10 part. 3. If $3.15V \leq V_{DD} \leq 3.6V$, tSAC = 9.5ns can be met @CAS latency = 2 of -12 part.

3

Component

- KM44S4020AT-
- KM48S2020AT
- KM416S1120AT

2M x 4Bit x 2 Bank Synchronous DRAM

FEATURES

- JEDEC standard 3.3V Power Supply.
- LVTTL compatible with multiplexed address.
- Dual Bank.
- MRS cycle with address key programs.
  - -. CAS Latency (1, 2, 3)
  - -. Burst Length (1, 2, 4, 8 & Full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst Read Single Bit Write Operation.
- DQM for masking
- Auto & Self Refresh.
- 64ms Refresh Period. (4K cycle)

GENERAL DESCRIPTION

The KM44S4020A is 16,777,216 bits synchronous high data rate Dynamic RAM organized as 2 x 2,097,152 words by 4 bits, fabricated with SAMSUNG's high performance CMOS technology.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle.

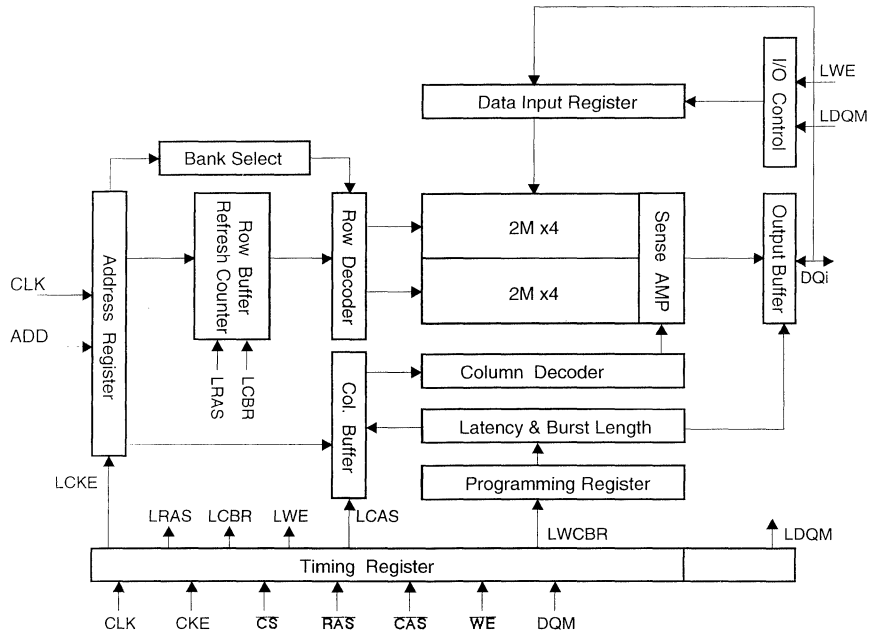
Range of operating frequencies, programmable burst length, and programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

3

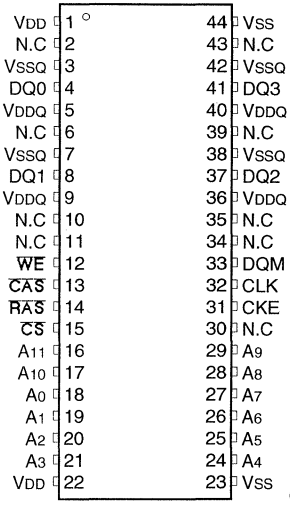
ORDERING INFORMATION

Part NO.	Max Freq.	Package
KM44S4020AT-G/F10	100 MHz	TSOP (II)
KM44S4020AT-G/F12	83 MHz	TSOP (II)

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



44 PIN TSOP (II)
(400mil x 725mil)
(0.8 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE, and DQM
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power down in standby. CKE should be enabled t_{PDE} prior to valid command.
A_0 ~ A_{10}	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{10}, Column address : CA_0 ~ CA_9
A_{11}	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge.
DQM	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
$DQ_{0\sim3}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	Ios	50	mA

Note : Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltages referenced to Vss = 0V, T_A=0°C to 70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Supply voltage	V_{DD},V_{DDQ}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	
Input low voltage	V_{IL}	-0.3	0	0.8	V	Note 1
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} =-2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	Note 2
Output leakage current	IOL	-5	-	5	uA	Note 3

Note : 1. V_{IL}(min.) = -1.5V AC (pulse width ≤ 5 ns)
2. Any input 0≤V_{IN}≤V_{DD} + 0.3V, all other pins are not under test = 0V.
3. Dout is disabled, 0≤V_{OUT}≤V_{DD}.

CAPACITANCE (V_{DD}= 3.3V, T_A= 25°C, f= 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(A_0-A_{11})	C_{IN1}	-	5	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & DQM)	C_{IN2}	-	5	pF
Data input/output capacitance (DQ_0 - DQ_3)	C_{OUT}	-	6	pF

DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitors are added to power line on PCB.

Parameter	Symbol	Value	Unit
Decoupling Capacitance between V_{DD} and Vss	C_{DC1}	0.1 * 2	uF
Decoupling Capacitance between V_{DDQ} and V_{SSQ}	C_{DC2}	0.1 * 2	uF

Note : 1. V_{DD} and V_{DDQ} pins are separated each other.
All V_{DD} pins are connected inside the chip. All V_{DDQ} pins are connected inside the chip.
2. Vss and V_{SSQ} pins are separated each other.
All Vss pins are connected inside the chip.

DC CHARACTERISTICS

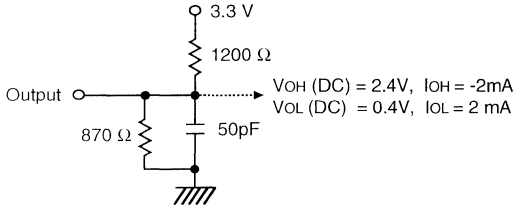
(Recommended Operating Conditions Unless Otherwise Noted, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Version -12	Unit	Note
Operating Current	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA	3	80	75	mA	1
			2	75	70		
			1	70	65		
Precharge Standby Current in Power-down mode	I_{CC2P}	CKE≤V_{IL}(max), t_{CC}=15ns		3		mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), t_{CC}= ∞		2			
Precharge Standby Current in Non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		25		mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		8			
Active Standby Current in power-down mode	I_{CC3P}	CKE≤V_{IL}(max), t_{CC}=15ns		3		mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), t_{CC}= ∞		2			
Active Standby Current in Non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		25		mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		10			
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst All Banks activated t_{CCD}=t_{CCD}(min)	3	120	110	mA	1, 2
			2	85	80		
			1	60	55		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	3	70	65	mA	3
			2	65	60		
			1	60	55		
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		2		mA	4
				250		uA	5

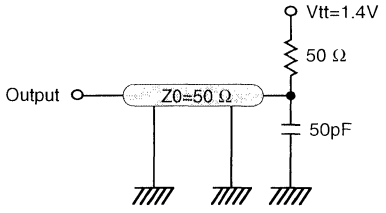
NOTE :
1. Measured with outputs open.
2. Assumes minimum column address update cycle t_{CCD}(min)
3. Refresh period is 64ms.
4. KM44S4020AT-G**
5. KM44S4020AT-F**

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70 °C)

Parameter	Value
AC input levels	V_{IH}/ V_{IL}= 2.4V / 0.4V
Input timing measurement reference level	1.4V
Input rise and fall time	tr / tf = 1ns / 1ns
Output measurement reference level	1.4V
Output load condition	See Fig. 2



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-10	-12		
Row active to Row active delay		tRRD(min)	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	26	30	ns	1
Row precharge time		tRP(min)	26	30	ns	1
Row active time		tRAS(min)	60	66	ns	1
		tRAS(max)	200	200	us	
Row cycle time		tRC(min)	96	100	ns	1
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to Row precharge		tRDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	0		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS Latency= 3		2		ea	4
	CAS Latency= 2		1			
	CAS Latency= 1		0			

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of Row precharge interrupt, Auto precharge and Read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-10		-12		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	12	1000	ns	1
	CAS latency=2		15		15			1
	CAS latency=1		30		30			1
CLK to valid output delay	CAS latency=3	tSAC	-	7.5	-	9	ns	1, 2
	CAS latency=2		-	9.5	-	10		1, 2, 5, 6
	CAS latency=1		-	27	-	27		1, 2
Output data hold time		tOH	3		3		ns	2
CLK high pulse width		tCH	3.5		4		ns	3
CLK low pulse width		tCL	3.5		4		ns	3
Input setup time		tSS	3		3		ns	3
Input hold time		tSH	1		1.5		ns	3
Power down exit set-up time		tPDE	8		10		ns	4
CLK to output in low-Z		tSLZ	2		2		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ	-	8	-	9	ns	
	CAS latency=2		-	10	-	11		
	CAS latency=1		-	15	-	16		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2 - 1] ns should be added to the parameter.
4. A time of tPDE has to elapse after asserting CKE to resume normal operation when exiting both bank precharge power down mode.
5. If 3.15V≤VDD≤3.6V, tSAC = 9ns can be met @CAS latency=2 of - 10 part.
6. If 3.15V≤VDD≤3.6V, tSAC = 9.5ns can be met @CAS latency=2 of -12 part .

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM44S4020AT-10

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		96ns	60ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	10	6	3	2	3	1	1	1
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	2	2	2	1	1	1
66MHz (15.2ns)	2	7	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	1	2	1	1	1
33MHz (30.3ns)	1	4	2	1	1	1	1	1	1
30MHz (33.3ns)	1	3	2	1	1	1	1	1	1

KM44S4020AT-12

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		100ns	66ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	9	6	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	3	2	3	1	1	1
66MHz (15.2ns)	2	7	5	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	6	4	2	2	2	1	1	1
33MHz (30.3ns)	1	4	3	1	1	1	1	1	1
30MHz (33.3ns)	1	3	2	1	1	1	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A11	A10	A9~A0	NOTE
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
				L									3
	Self Refresh	Entry			L	H	H	H	X	X			3
					H	X	X	X					3
		Exit	L	H									
Bank Active & Row Address			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A9~A0)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A9~A0)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Bank									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{11} : Program keys.(@MRS)

2. MRS can be issued only at both bank precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions as same as CBR refresh of DRAM.
The automatical precharge without Row precharge command is meant by "Auto".
Auto/Self refresh can be issued only at both bank precharge state.

4. A_{11} : Bank select address.
If "Low" at read, write, Row active and precharge, bank A is selected.
If "High" at read, write, Row active and precharge, bank B is selected.
If A_{10} is "High" at Row precharge, A_{11} is ignored and both banks are selected.

5. During burst read or write with auto precharge,
new read/write command cannot be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK
masks the data-in at the very CLK (Write DQM latency is 0)
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

1M x 8Bit x 2 Bank Synchronous DRAM

FEATURES

- JEDEC standard 3.3V Power Supply.
- LVTTL compatible with multiplexed address.
- Dual Bank.
- MRS cycle with address key programs.
  - -. CAS Latency (1, 2, 3)
  - -. Burst Length (1, 2, 4, 8 & Full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst Read Single Bit Write Operation.
- DQM for masking.
- Auto & Self Refresh.
- 64ms Refresh Period. (4K cycle)

GENERAL DESCRIPTION

The KM48S2020A is 16,777,216 bits synchronous high data rate Dynamic RAM organized as 2 x 1,048,576 words by 8 bits, fabricated with SAMSUNG's high performance CMOS technology.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle.

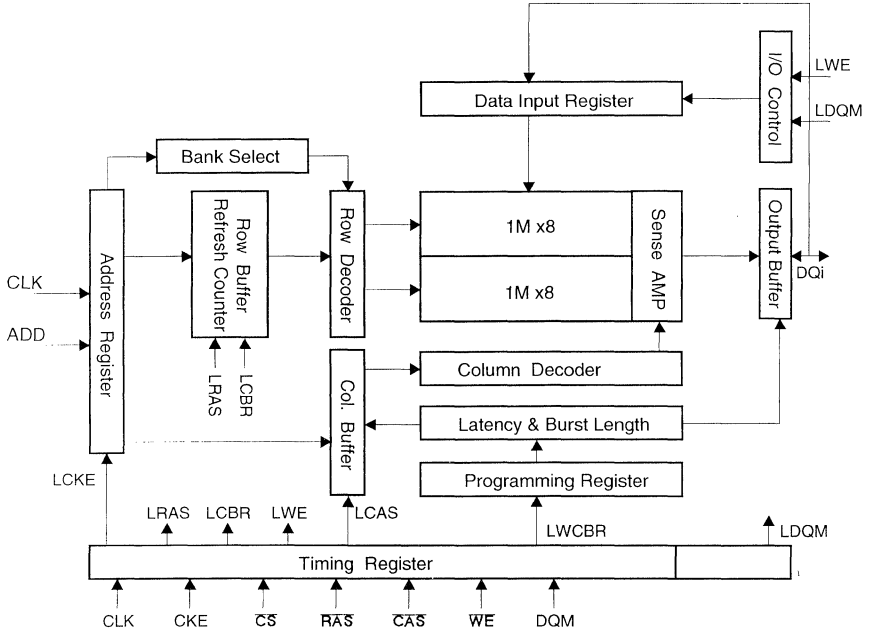
Range of operating frequencies, programmable burst length, and programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

3

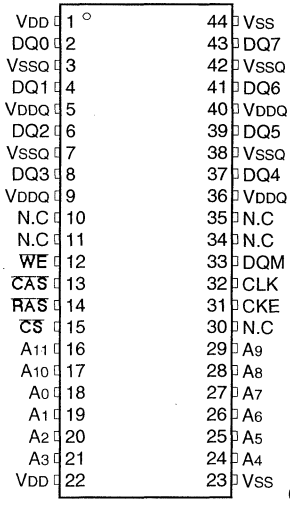
ORDERING INFORMATION

Part NO.	Max Freq.	Package
KM48S2020AT-G/F10	100 MHz	TSOP (II)
KM48S2020AT-G/F12	83 MHz	TSOP (II)

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



44 PIN TSOP (II)
(400mil x 725mil)
(0.8 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE, and DQM
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power down in standby. CKE should be enabled t_{PDE} prior to valid command.
A_0 ~ A_{10}	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{10}, Column address : CA_0 ~ CA_8
A_{11}	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge.
DQM	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
$DQ_{0 \sim 7}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	Ios	50	mA

Note : Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltages referenced to Vss = 0V, T_A=0°C to 70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Supply voltage	V_{DD},V_{DDQ}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	
Input low voltage	V_{IL}	-0.3	0	0.8	V	Note 1
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} =-2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	Note 2
Output leakage current	I_{OL}	-5	-	5	uA	Note 3

Note : 1. V_{IL}(min.) = -1.5V AC (pulse width ≤ 5 ns)
2. Any input 0≤V_{IN}≤V_{DD} + 0.3V, all other pins are not under test = 0V.
3. Dout is disabled, 0V≤V_{OUT}≤V_{DD}.

CAPACITANCE (V_{DD}= 3.3V, T_A= 25°C, f= 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(A_0-A_{11})	C_{IN1}	-	5	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & DQM)	C_{IN2}	-	5	pF
Data input/output capacitance (DQ_0 - DQ_7)	C_{OUT}	-	6	pF

DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitors are added to power line on PCB.

Parameter	Symbol	Value	Unit
Decoupling Capacitance between V_{DD} and V_{SS}	C_{DC1}	0.1 * 2	uF
Decoupling Capacitance between V_{DDQ} and V_{SSQ}	C_{DC2}	0.1 * 2	uF

Note : 1. V_{DD} and V_{DDQ} pins are separated each other.
All V_{DD} pins are connected inside the chip. All V_{DDQ} pins are connected inside the chip.
2. V_{SS} and V_{SSQ} pins are separated each other.
All V_{SS} pins are connected inside the chip.

DC CHARACTERISTICS

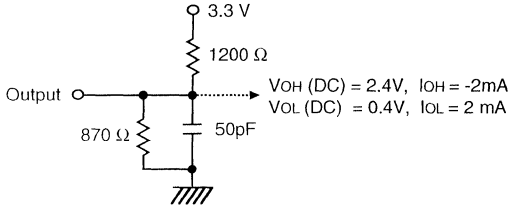
(Recommended Operating Conditions Unless Otherwise Noted, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Version -12	Unit	Note
Operating Current	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA	3	80	75	mA	1
			2	75	70		
			1	70	65		
Precharge Standby Current in Power-down mode	I_{CC2P}	CKE≤V_{IL}(max), t_{CC}=15ns		3		mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), t_{CC}= ∞		2			
Precharge Standby Current in Non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		25		mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		8			
Active Standby Current in power-down mode	I_{CC3P}	CKE≤V_{IL}(max), t_{CC}=15ns		3		mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), t_{CC}= ∞		2			
Active Standby Current in Non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		25		mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		10			
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst All Banks activated t_{CCD}=t_{CCD}(min)	3	120	110	mA	1, 2
			2	85	80		
			1	60	55		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	3	70	65	mA	3
			2	65	60		
			1	60	55		
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		2		mA	4
				250		uA	5

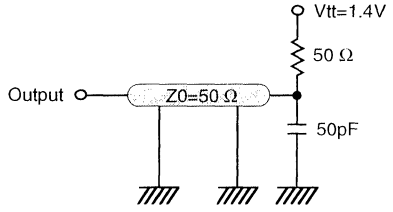
NOTE : 1. Measured with outputs open.
2. Assumes minimum column address update cycle t_{CCD}(min)
3. Refresh period is 64ms.
4. KM48S2020AT-G**
5. KM48S2020AT-F**

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70 °C)

Parameter	Value
AC input levels	V_{IH}/ V_{IL}= 2.4V / 0.4V
Input timing measurement reference level	1.4V
Input rise and fall time	tr / tf = 1ns / 1ns
Output measurement reference level	1.4V
Output load condition	See Fig. 2



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-10	-12		
Row active to Row active delay		tRRD(min)	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	26	30	ns	1
Row precharge time		tRP(min)	26	30	ns	1
Row active time		tRAS(min)	60	66	ns	1
		tRAS(max)	200	200	us	
Row cycle time		tRC(min)	96	100	ns	1
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to Row precharge		tRDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	0		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS Latency= 3		2		ea	4
	CAS Latency= 2		1			
	CAS Latency= 1		0			

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of Row precharge interrupt, Auto precharge and Read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-10		-12		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	12	1000	ns	1
	CAS latency=2		15		15			1
	CAS latency=1		30		30			1
CLK to valid output delay	CAS latency=3	tSAC	-	7.5	-	9	ns	1, 2
	CAS latency=2		-	9.5	-	10		1, 2, 5, 6
	CAS latency=1		-	27	-	27		1, 2
Output data hold time		tOH	3		3		ns	2
CLK high pulse width		tCH	3.5		4		ns	3
CLK low pulse width		tCL	3.5		4		ns	3
Input setup time		tSS	3		3		ns	3
Input hold time		tSH	1		1.5		ns	3
Power down exit set-up time		tPDE	8		10		ns	4
CLK to output in low-Z		tSLZ	2		2		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ	-	8	-	9	ns	
	CAS latency=2		-	10	-	11		
	CAS latency=1		-	15	-	16		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2 - 1] ns should be added to the parameter.
4. A time of tPDE has to elapse after asserting CKE to resume normal operation when exiting both bank precharge power down mode.
5. If 3.15V≤VDD≤3.6V, tSAC = 9ns can be met @CAS latency=2 of - 10 part.
6. If 3.15V≤VDD≤3.6V, tSAC = 9.5ns can be met @CAS latency=2 of -12 part .

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM48S2020AT-10

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		96ns	60ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	10	6	3	2	3	1	1	1
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	2	2	2	1	1	1
66MHz (15.2ns)	2	7	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	1	2	1	1	1
33MHz (30.3ns)	1	4	2	1	1	1	1	1	1
30MHz (33.3ns)	1	3	2	1	1	1	1	1	1

KM48S2020AT-12

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		100ns	66ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	9	6	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	3	2	3	1	1	1
66MHz (15.2ns)	2	7	5	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	6	4	2	2	2	1	1	1
33MHz (30.3ns)	1	4	3	1	1	1	1	1	1
30MHz (33.3ns)	1	3	2	1	1	1	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A11	A10	A9~A0	NOTE
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Address			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A8~A0)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A8~A0)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Bank									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{11} : Program keys.(@MRS)

2. MRS can be issued only at both bank precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions as same as CBR refresh of DRAM.
The automatical precharge without Row precharge command is meant by "Auto".
Auto/Self refresh can be issued only at both bank precharge state.

4. A_{11} : Bank select address.
If "Low" at read, write, Row active and precharge, bank A is selected.
If "High" at read, write, Row active and precharge, bank B is selected.
If A_{10} is "High" at Row precharge, A_{11} is ignored and both banks are selected.

5. During burst read or write with auto precharge,
new read/write command cannot be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK
masks the data-in at the very CLK (Write DQM latency is 0)
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

512K x 16Bit x 2 Bank Synchronous DRAM

FEATURES

- JEDEC standard 3.3V Power Supply.
- LVTTL compatible with multiplexed address.
- Dual Bank.
- MRS cycle with address key programs.
  - -. CAS Latency (1, 2, 3)
  - -. Burst Length (1, 2, 4, 8 & Full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst Read Single Bit Write Operation.
- L(U)DQM for byte masking.
- Auto & Self Refresh.
- 32ms Refresh Period. (2K cycle)

GENERAL DESCRIPTION

The KM416S1120A is 16,777,216 bits synchronous high data rate Dynamic RAM organized as 2 x 524,288 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle.

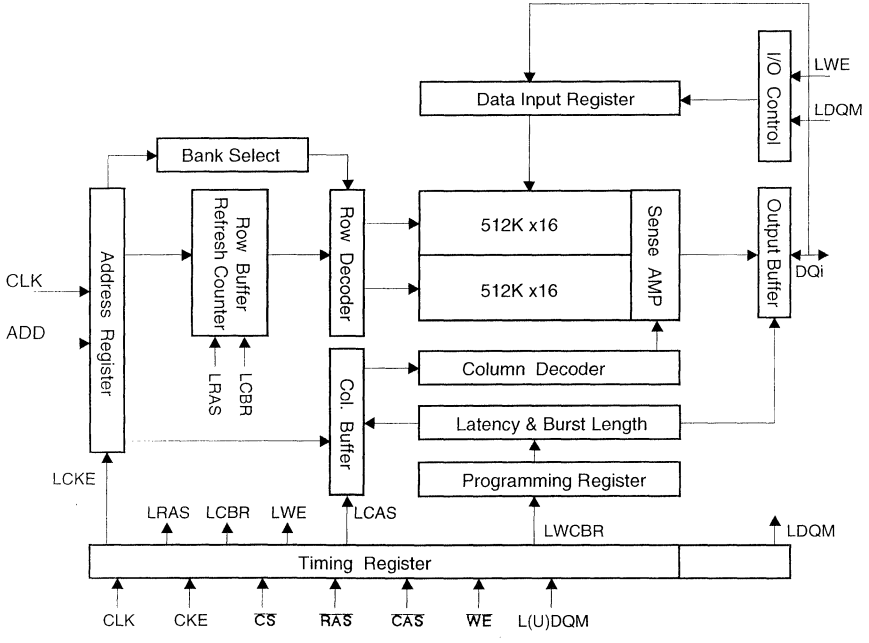
Range of operating frequencies, programmable burst length, and programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

3

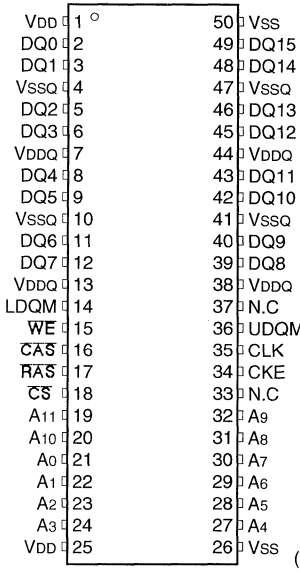
ORDERING INFORMATION

Part NO.	Max Freq.	Package
KM416S1120AT-G/F10	100 MHz	TSOP (II)
KM416S1120AT-G/F12	83 MHz	TSOP (II)

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



50 PIN TSOP (II)
(400mil x 825mil)
(0.8 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE, and L(U)DQM
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power down in standby. CKE should be enabled t_{PDE} prior to valid command.
A_0 ~ A_{10}	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{10}, Column address : CA_0 ~ CA_7
A_{11}	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge.
L(U)DQM	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte Masking)
$DQ_{0 \sim 15}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	Ios	50	mA

Note : Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltages referenced to Vss = 0V, T_A=0°C to 70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Supply voltage	V_{DD},V_{DDQ}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	
Input low voltage	V_{IL}	-0.3	0	0.8	V	Note 1
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} =-2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	Note 2
Output leakage current	I_{OL}	-5	-	5	uA	Note 3

Note : 1. V_{IL}(min.) = -1.5V AC (pulse width ≤ 5 ns)
2. Any input 0≤V_{IN}≤V_{DD} + 0.3V, all other pins are not under test = 0V.
3. Dout is disabled, 0V≤V_{OUT}≤V_{DD}.

CAPACITANCE (V_{DD}= 3.3V, T_A= 25°C, f= 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(A_0-A_{11})	C_{IN1}	-	5	pF
Input capacitance (CLK,CKE,$\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$ & L(U)DQM)	C_{IN2}	-	5	pF
Data input/output capacitance (DQ_0 - DQ_{15})	C_{OUT}	-	6	pF

DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitors are added to power line on PCB.

Parameter	Symbol	Value	Unit
Decoupling Capacitance between V_{DD} and Vss	C_{DC1}	0.1 * 3	uF
Decoupling Capacitance between V_{DDQ} and V_{SSQ}	C_{DC2}	0.1 * 3	uF

Note : 1. V_{DD} and V_{DDQ} pins are separated each other.
All V_{DD} pins are connected inside the chip. All V_{DDQ} pins are connected inside the chip.
2. Vss and V_{SSQ} pins are separated each other.
All Vss pins are connected inside the chip.

DC CHARACTERISTICS

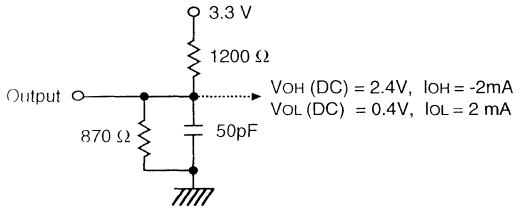
(Recommended Operating Conditions Unless Otherwise Noted, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Version -12	Unit	Note
Operating Current	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA	3	105	100	mA	1
			2	95	90		
			1	90	85		
Precharge Standby Current in Power-down mode	I_{CC2P}	CKE≤V_{IL}(max), t_{CC}=15ns		3		mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), t_{CC}= ∞		2			
Precharge Standby Current in Non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		25		mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		8			
Active Standby Current in power-down mode	I_{CC3P}	CKE≤V_{IL}(max), t_{CC}=15ns		3		mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), t_{CC}= ∞		2			
Active Standby Current in Non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		30		mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		15			
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst All Banks activated t_{CCD}=t_{CCD}(min)	3	145	125	mA	1, 2
			2	105	90		
			1	65	60		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	3	95	90	mA	3
			2	90	85		
			1	85	80		
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		2		mA	4
				250		uA	5

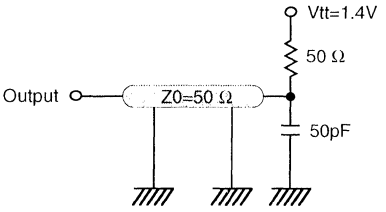
NOTE :
1. Measured with outputs open.
2. Assumes minimum column address update cycle t_{CCD}(min)
3. Refresh period is 32ms.
4. KM416S1120AT-G**
5. KM416S1120AT-F**

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70 °C)

Parameter	Value
AC input levels	V_{IH}/ V_{IL}= 2.4V / 0.4V
Input timing measurement reference level	1.4V
Input rise and fall time	tr / tf = 1ns / 1ns
Output measurement reference level	1.4V
Output load condition	See Fig. 2



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			- 10	- 12		
Row active to Row active delay		t_{RRD}(min)	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		t_{RCD}(min)	26	30	ns	1
Row precharge time		t_{RP}(min)	26	30	ns	1
Row active time		t_{RAS}(min)	60	66	ns	1
		t_{RAS}(max)	200	200	us	
Row cycle time		t_{RC}(min)	96	100	ns	1
Last data in to new col. address delay		t_{CDL}(min)	1		CLK	2
Last data in to Row precharge		t_{RDL}(min)	1		CLK	2
Last data in to burst stop		t_{BDL}(min)	0		CLK	2
Col. address to col. address delay		t_{CCD}(min)	1		CLK	3
Number of valid output data	CAS Latency= 3		2		ea	4
	CAS Latency= 2		1			
	CAS Latency= 1		0			

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of Row precharge interrupt, Auto precharge and Read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-10		-12		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	12	1000	ns	1
	CAS latency=2		15		15			1
	CAS latency=1		30		30			1
CLK to valid output delay	CAS latency=3	tSAC	-	8	-	9	ns	1, 2
	CAS latency=2		-	9.5	-	10		1, 2, 5, 6
	CAS latency=1		-	27	-	27		1, 2
Output data hold time		tOH	3		3		ns	2
CLK high pulse width		tCH	3.5		4		ns	3
CLK low pulse width		tCL	3.5		4		ns	3
Input setup time		tSS	3		3		ns	3
Input hold time		tSH	1		1.5		ns	3
Power down exit set-up time		tPDE	8		10		ns	4
CLK to output in low-Z		tSLZ	2		2		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ	-	8	-	9	ns	
	CAS latency=2		-	10	-	11		
	CAS latency=1		-	15	-	16		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2 - 1] ns should be added to the parameter.
4. A time of tPDE has to elapse after asserting CKE to resume normal operation when exiting both bank precharge power down mode.
5. If 3.15V≤VDD≤3.6V, tSAC = 9ns can be met @CAS latency=2 of - 10 part.
6. If 3.15V≤VDD≤3.6V, tSAC = 9.5ns can be met @CAS latency=2 of -12 part .

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM416S1120AT-10

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		96ns	60ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	10	6	3	2	3	1	1	1
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	2	2	2	1	1	1
66MHz (15.2ns)	2	7	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	1	2	1	1	1
33MHz (30.3ns)	1	4	2	1	1	1	1	1	1
30MHz (33.3ns)	1	3	2	1	1	1	1	1	1

KM416S1120AT-12

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		100ns	66ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	9	6	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	3	2	3	1	1	1
66MHz (15.2ns)	2	7	5	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	6	4	2	2	2	1	1	1
33MHz (30.3ns)	1	4	3	1	1	1	1	1	1
30MHz (33.3ns)	1	3	2	1	1	1	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A11	A10	A9~A0	NOTE
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
				L									3
	Self Refresh	Entry			L	H	H	H	X	X			3
					H	X	X	X					3
		Exit	L	H									
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_7~A_0)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_7~A_0)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Bank									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{11} : Program keys.(@MRS)

2. MRS can be issued only at both bank precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions as same as CBR refresh of DRAM.
The automatical precharge without Row precharge command is meant by "Auto".
Auto/Self refresh can be issued only at both bank precharge state.

4. A_{11} : Bank select address.
If "Low" at read, write, Row active and precharge, bank A is selected.
If "High" at read, write, Row active and precharge, bank B is selected.
If A_{10} is "High" at Row precharge, A_{11} is ignored and both banks are selected.

5. During burst read or write with auto precharge,
new read/write command cannot be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK
masks the data-in at the very CLK (Write DQM latency is 0)
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

Module

- KMM366S114AT
- KMM366S203AT
- KMM366S400AT
- KMM366S403A1T

KMM366S114AT SDRAM DIMM

1Mx64 SDRAM DIMM based on 1Mx16, 2K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S114AT is a 1M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S114AT consists of four CMOS 1Mx16 bit Synchronous DRAMs in TSOP-II 400mil packages and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The KMM366S114AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURES

- Performance Range

	Max Freq. (Speed)
KMM366S114AT - 0	100 MHz (10ns)
KMM366S114AT- 2	83 MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (2048 cycles/32 ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs.
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full Page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, single sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	*A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A14	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A15	160	DQ62
21	NC	49	VDD	77	DQ31	105	NC	133	VDD	161	DQ63
22	NC	50	NC	78	Vss	106	NC	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	NC	80	NC	108	NC	136	NC	164	NC
25	NC	53	NC	81	NC	109	NC	137	NC	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A10	Address input (multiplexed)
A11	Select Bank
DQ0 ~ 63	Data Input/Output
CLK0, *CLK1	Clock input
CKE	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
NC	No Connection
*VREF	Power Supply for Reference
**SDA	Serial Address/Data/I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don't Use

* These pins are not used in this module.

** These pins should be NC in system which does not support SPD.

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE, and DQM
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power down in standby. CKE should be enabled t_{PDE} prior to valid command.
A0 ~ A10	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, Column address : CA0 ~ CA7
A11	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte Masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	

SERIAL PRESENCE DETECT INFORMATION

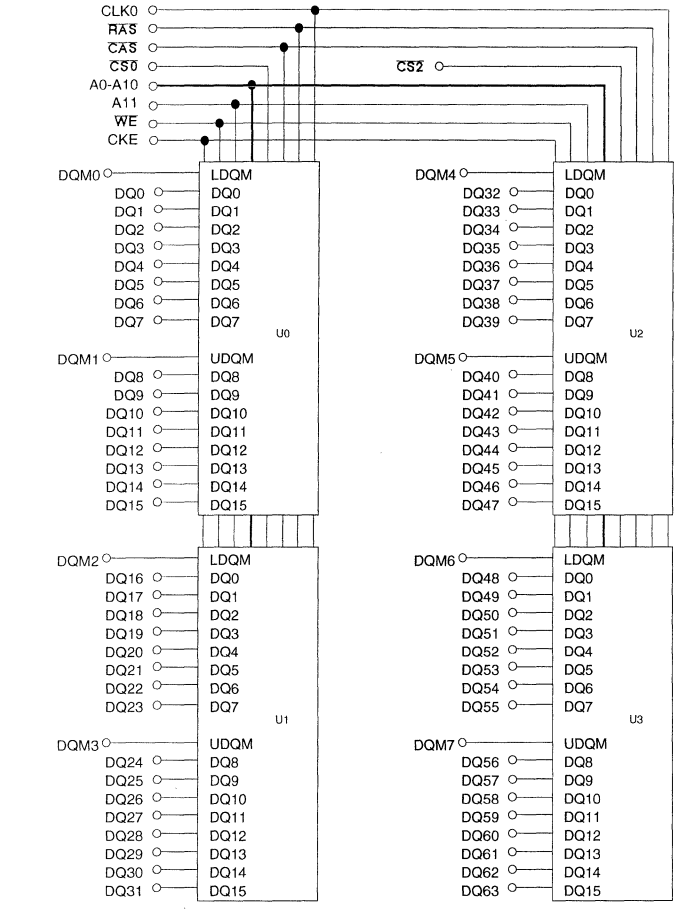
- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver ≤ 3mA
- Maximum clock frequency : 80KHz
- Contents :

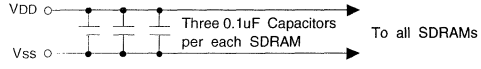
Byte No.	Function described	Function supported	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	12	0Ch	1
4	# of column addresses on this assembly	9	09h	2
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	64 bits	40h	
7	.....Data width of this assembly (Continued)	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	10ns	A0h	3, 8
		12ns	C0h	3, 8
10	SDRAM access time from clock	8ns	80h	4, 8
		9ns	90h	4, 8
11	DIMM configuration type	Non-parity	00h	
12	Refresh rate/type	15.625us, Self-refresh supported	80h	
13	SDRAM module attributes	non-buffered, non-registered	00h	
14	SDRAM device attributes : General	Support Burst Read Single-bit Write, Precharge all & Auto precharge	0Eh	5
15	Minimum clock delay for back-to-back random column address	tCCD = 1 CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	6
17	SDRAM device attributes : # of banks on SDRAM device	2 banks	02h	
18	SDRAM device attributes : CAS latency	CAS latency = 1, 2 & 3	07h	7
19	SDRAM device attributes : CS latency	CS latency = 0	01h	
20	SDRAM device attributes : Write latency	Write latency = 0	01h	
21 ~ 31	Reserved for future offerings	-	00h	
32 ~ 63	Superset information (may be used in future)	-	00h	
64 ~ 127	Manufacturer's information (optional)	-	00h	
128 +	Unused storage locations	-	XX	

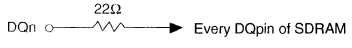
* Above data are based on the SPD specification of JEDEC standard and can be changed.

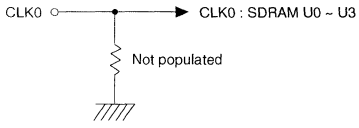
Note :
1. If the bank select address of RA11 is excluded, this byte must be programmed by 0Bh.
2. If the bank select address of CA11 is excluded, this byte must be programmed by 08h.
3. In case of - 10 part, the minimum cycle time is 10ns, 15ns and 30ns @CAS latency = 3, 2 and 1 respectively.
   So, the value of A0h is based on the minimum cycle time @CAS latency = 3.
   In case of - 12 part, the minimum cycle time is 12ns, 15ns and 30ns @CAS latency = 3, 2 & 1 respectively.
   So, the value of C0h is based on the minimum cycle time @CAS latency = 3.
4. In case of - 10 part, the access time is 8ns, 9.5ns and 27ns @CAS latency = 3, 2 and 1 respectively.
   So, the value of 80h is based on the access time @CAS latency = 3.
   In case of - 12 part, the access time is 9ns, 10ns and 27ns @CAS latency = 3, 2 and 1 respectively.
   So, the value of 90h is based on the access time @CAS latency = 3.
5. SEC's SDRAM supports Burst Read Single-bit Write, Precharge all and Auto precharge functions.
   If Burst Read Single-bit Write function is not supported, this byte must be programmed by 06h.
6. SEC's SDRAM supports burst lengths of 1, 2, 4, 8 and full page. If burst lengths of 1 and 4 are only supported, this byte must be programmed by 05h.
7. SEC's SDRAM supports CAS latency of 1, 2 and 3. If CAS latency of 2 and 3 are only supported, this byte must be programmed by 06h.
8. This value is based on the component specification.

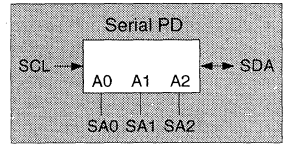
FUNCTIONAL BLOCK DIAGRAM











ABSOLUTE MAXIMUM RATINGS

Paramerter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	4	W
Short circuit current	Ios	50	mA

Note : Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltages referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	
Input low voltage	V_{IL}	-0.3	0	0.8	V	Note 1
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH}=-2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL}= 2mA
Input leakage current	I_{IL}	-20	-	20	uA	Note 2
Output leakage current	I_{OL}	-5	-	5	uA	Note 3

Note : 1. V_{IL}(min.) = -1.5V AC (pulse width ≤ 5 ns)
2. Any input 0 ≤ V_{IN} ≤ V_{DD}+0.3V, all other pins not under test = 0 Volt
3. Dout is disabled, 0V ≤ Vout ≤ V_{DD}

CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11)	C_{IN1}	-	25	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	C_{IN2}	-	25	pF
Input capacitance (CLK0)	C_{IN3}	-	25	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN4}	-	15	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN5}	-	10	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	10	pF

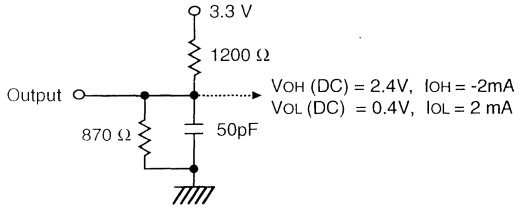
DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Version -12	Unit	Note
Operating Current	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA	3	380	360	mA	1
			2	340	320		
			1	320	300		
Precharge Standby Current in Power-down mode	I_{CC2P}	CKE≤V_{IL}(max), t_{CC}=15ns		10		mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), t_{CC}= ∞		26			
Precharge Standby Current in Non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		100		mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		25			
Active Standby Current in Power-down mode	I_{CC3P}	CKE≤V_{IL}(max), t_{CC}=15ns		12		mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), t_{CC}= ∞		8			
Active Standby Current in Non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		120		mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		45			
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst All Banks activated t_{CCD}=t_{CCD}(min)	3	480	400	mA	1, 2
			2	340	280		
			1	180	160		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	3	340	320	mA	3
			2	320	300		
			1	300	280		
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		6		mA	4
				1		mA	5

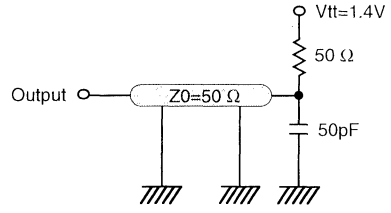
Note : 1. Measured with outputs open.
2. Assumes minimum column address update cycle t_{CCD}(min)
3. Refresh period is 32ms.
4. KMM366S114AT-G*
5. KMM366S114AT-F*

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70 °C)

Parameter	Value
AC input levels	V_{IH}/ V_{IL}= 2.4V / 0.4V
Input timing measurement reference level	1.4V
Input rise and fall time	tr / tf = 1ns / 1ns
Output measurement reference level	1.4V
Output load condition	See Fig. 2



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	Version		Unit	Note
			- 10	- 12		
Row active to Row active delay		tRRD(min)	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	26	30	ns	1
Row precharge time		tRP(min)	26	30	ns	1
Row active time		tRAS(min)	60	66	ns	1
		tRAS(max)	200	200	us	
Row cycle time		tRC(min)	96	100	ns	1
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to Row precharge		tRDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	0		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS Latency= 3		2		ea	4
	CAS Latency= 2		1			
	CAS Latency= 1		0			

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of Row precharge interrupt, Auto precharge and Read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-10		-12		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	12	1000	ns	1
	CAS latency=2		15		15			1
	CAS latency=1		30		30			1
CLK to valid output delay	CAS latency=3	tSAC	-	8	-	9	ns	1, 2
	CAS latency=2		-	9.5	-	10		1, 2, 5, 6
	CAS latency=1		-	27	-	27		1, 2
Output data hold time		tOH	3		3		ns	2
CLK high pulse width		tCH	3.5		4		ns	3
CLK low pulse width		tCL	3.5		4		ns	3
Input setup time		tSS	3		3		ns	3
Input hold time		tSH	1		1.5		ns	3
Power down exit set-up time		tPDE	8		10		ns	4
CLK to output in low-Z		tSLZ	2		2		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ	-	8	-	9	ns	
	CAS latency=2		-	10	-	11		
	CAS latency=1		-	15	-	16		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2 - 1] ns should be added to the parameter.
4. A time of tPDE has to elapse after asserting CKE to resume normal operation when exiting both bank precharge power down mode.
5. If 3.15V≤VDD≤3.6V, tSAC = 9ns can be met @CAS latency=2 of - 10 part.
6. If 3.15V≤VDD≤3.6V, tSAC = 9.5ns can be met @CAS latency=2 of -12 part .

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S114AT-0

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		96ns	60ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	10	6	3	2	3	1	1	1
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	2	2	2	1	1	1
66MHz (15.2ns)	2	7	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	1	2	1	1	1
33MHz (30.3ns)	1	4	2	1	1	1	1	1	1
30MHz (33.3ns)	1	3	2	1	1	1	1	1	1

KMM366S114AT-2

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		100ns	66ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	9	6	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	3	2	3	1	1	1
66MHz (15.2ns)	2	7	5	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	6	4	2	2	2	1	1	1
33MHz (30.3ns)	1	4	3	1	1	1	1	1	1
30MHz (33.3ns)	1	3	2	1	1	1	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A11	A10	A9~A0	NOTE
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A7~A0)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A7~A0)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Bank									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{11} : Program keys.(@MRS)

2. MRS can be issued only at both bank precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions as same as CBR refresh of DRAM.
The automatical precharge without Row precharge command is meant by "Auto".
Auto/Self refresh can be issued only at both bank precharge state.

4. A_{11} : Bank select address.
If "Low" at read, write, Row active and precharge, bank A is selected.
If "High" at read, write, Row active and precharge, bank B is selected.
If A_{10} is "High" at Row precharge, A_{11} is ignored and both banks are selected.

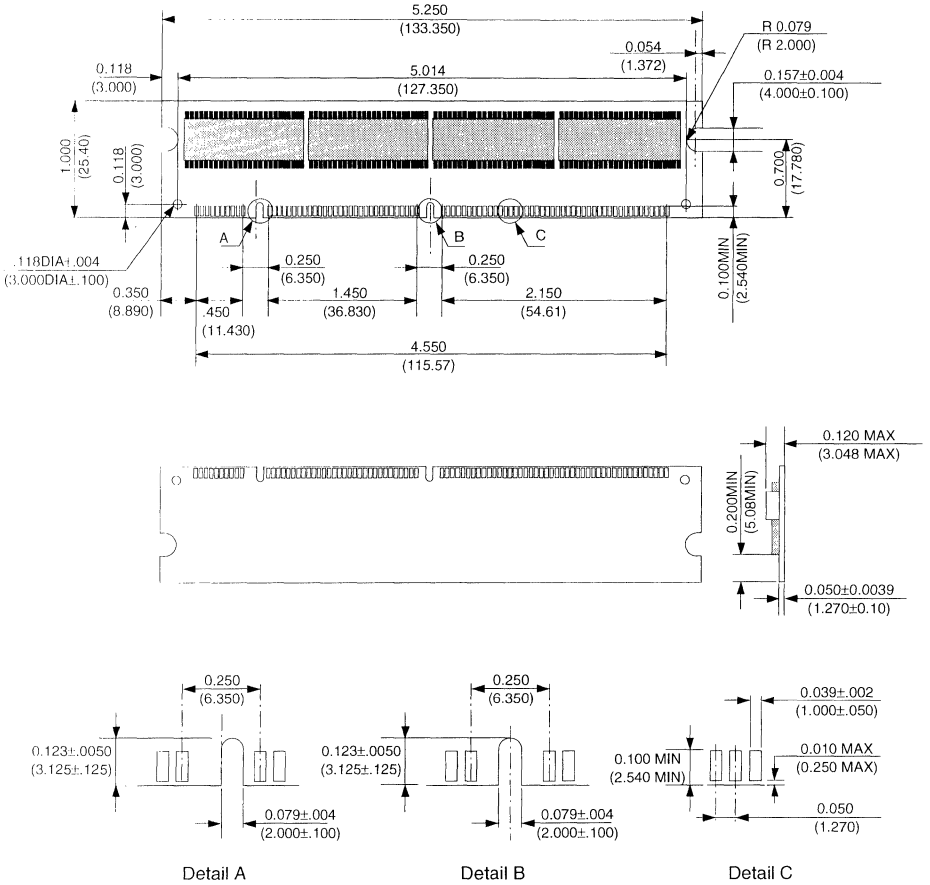
5. During burst read or write with auto precharge,
new read/write command cannot be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK
masks the data-in at the very CLK (Write DQM latency is 0)
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (millimeters)



Detail A Detail B Detail C

Tolerances : ±.005 (.13) unless otherwise specified

The used device is 1Mx16 SDRAM , TSOP
DRAM Part No. : KM416S1120AT .

KMM366S203AT SDRAM DIMM

2Mx64 SDRAM DIMM based on 2Mx8, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S203AT is a 2M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S203AT consists of eight CMOS 2Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The KMM366S203AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURES

- Performance Range

	Max Freq. (Speed)
KMM366S203AT - 0	100 MHz (10ns)
KMM366S203AT- 2	83 MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles/64 ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs.
  Latency(Access from column address)
  Burst Length (1, 2, 4, 8 & Full Page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	*A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A14	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A15	160	DQ62
21	NC	49	VDD	77	DQ31	105	NC	133	VDD	161	DQ63
22	NC	50	NC	78	Vss	106	NC	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	NC	80	NC	108	NC	136	NC	164	NC
25	NC	53	NC	81	NC	109	NC	137	NC	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A10	Address input (multiplexed)
A11	Select Bank
DQ0 ~ 63	Data Input/Output
CLK0, *CLK1	Clock input
CKE	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
NC	No Connection
*VREF	Power Supply for Reference
**SDA	Serial Address/Data/I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don't Use

* These pins are not used in this module.

** These pins should be NC in system which does not support SPD.

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE, and DQM
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power down in standby. CKE should be enabled t_{PDE} prior to valid command.
A0 ~ A10	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, Column address : CA0 ~ CA8
A11	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte Masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	

SERIAL PRESENCE DETECT INFORMATION

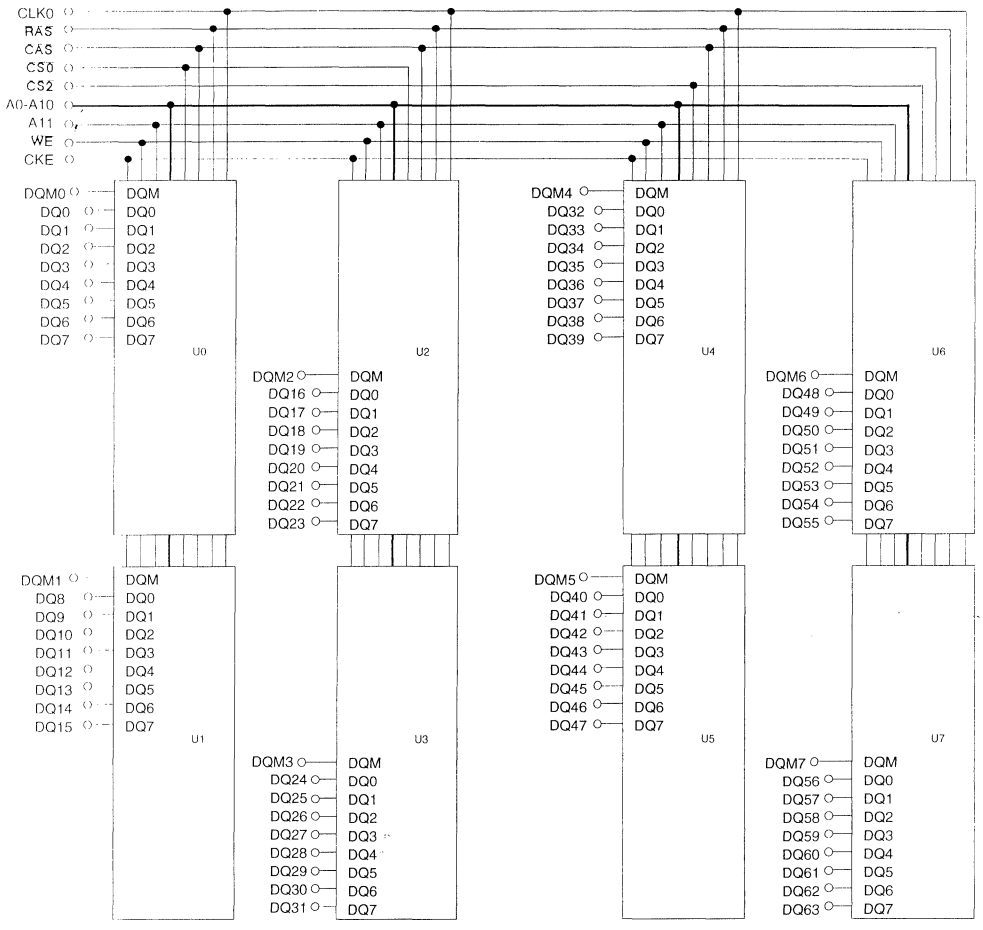
- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver ≤ 3mA
- Maximum clock frequency : 80KHz
- Contents :

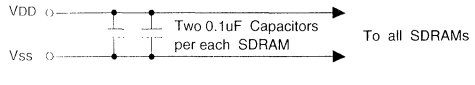
Byte No.	Function described	Function supported	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	12	0Ch	1
4	# of column addresses on this assembly	10	0Ah	2
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	64 bits	40h	
7	.....Data width of this assembly (Continued)	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	10ns	A0h	3, 8
		12ns	C0h	3, 8
10	SDRAM access time from clock	7.5ns	75h	4, 8
		9ns	90h	4, 8
11	DIMM configuration type	Non-parity	00h	
12	Refresh rate/type	15.625us, Self-refresh supported	80h	
13	SDRAM module attributes	non-buffered, non-registered	00h	
14	SDRAM device attributes : General	Support Burst Read Single-bit Write, Precharge all & Auto precharge	0Eh	5
15	Minimum clock delay for back-to-back random column address	t_{CCD} = 1 CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	6
17	SDRAM device attributes : # of banks on SDRAM device	2 banks	02h	
18	SDRAM device attributes : CAS latency	CAS latency = 1, 2 & 3	07h	7
19	SDRAM device attributes : CS latency	CS latency = 0	01h	
20	SDRAM device attributes : Write latency	Write latency = 0	01h	
21 ~ 31	Reserved for future offerings	-	00h	
32 ~ 63	Superset information (may be used in future)	-	00h	
64 ~ 127	Manufacturer's information (optional)	-	00h	
128 +	Unused storage locations	-	XX	

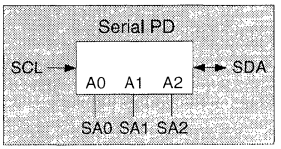
* Above data are based on the SPD specification of JEDEC standard and can be changed.

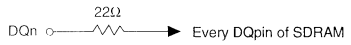
Note : 1. If the bank select address of RA11 is excluded, this byte must be programmed by 0Bh.
2. If the bank select address of CA11 is excluded, this byte must be programmed by 09h.
3. In case of - 10 part, the minimum cycle time is 10ns, 15ns and 30ns @CAS latency = 3, 2 and 1 respectively.
So, the value of A0h is based on the minimum cycle time @CAS latency = 3.
In case of - 12 part, the minimum cycle time is 12ns, 15ns and 30ns @CAS latency = 3, 2 & 1 respectively.
So, the value of C0h is based on the minimum cycle time @CAS latency = 3.
4. In case of - 10 part, the access time is 7.5ns, 9.5ns and 27ns @CAS latency = 3, 2 and 1 respectively.
So, the value of 75h is based on the access time @CAS latency = 3.
In case of - 12 part, the access time is 9ns, 10ns and 27ns @CAS latency = 3, 2 and 1 respectively.
So, the value of 90h is based on the access time @CAS latency = 3.
5. SEC's SDRAM supports Burst Read Single-bit Write, Precharge all and Auto precharge functions.
If Burst Read Single-bit Write function is not supported, this byte must be programmed by 06h.
6. SEC's SDRAM supports burst lengths of 1, 2, 4, 8 and full page. If burst lengths of 1 and 4 are only supported, this byte must be programmed by 05h.
7. SEC's SDRAM supports CAS latency of 1, 2 and 3. If CAS latency of 2 and 3 are only supported, this byte must be programmed by 06h.
8. This value is based on the component specification.

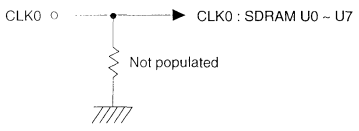
FUNCTIONAL BLOCK DIAGRAM











ABSOLUTE MAXIMUM RATINGS

Paramerter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	Ios	50	mA

Note : Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltages referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	
Input low voltage	V_{IL}	-0.3	0	0.8	V	Note 1
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH}=-2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL}= 2mA
Input leakage current	I_{IL}	-40	-	40	uA	Note 2
Output leakage current	I_{OL}	-5	-	5	uA	Note 3

Note : 1. V_{IL}(min.) = -1.5V AC (pulse width ≤ 5 ns)
2. Any input 0 ≤ V_{IN} ≤ V_{DD}+0.3V, all other pins not under test = 0 Volt
3. Dout is disabled, 0V ≤ Vout ≤ V_{DD}

CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11)	C_{IN1}	-	45	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	C_{IN2}	-	45	pF
Input capacitance (CLK0)	C_{IN3}	-	45	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN4}	-	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN5}	-	10	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	10	pF

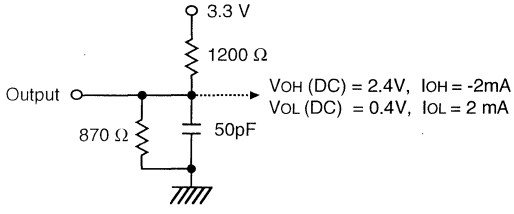
DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Version -12	Unit	Note
Operating Current	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA	3	600	560	mA	1
			2	540	500		
			1	480	440		
Precharge Standby Current in Power-down mode	I_{CC2P}	CKE≤V_{IL}(max), t_{CC}=15ns		20		mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), t_{CC}= ∞		12			
Precharge Standby Current in Non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		200		mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		50			
Active Standby Current in Power-down mode	I_{CC3P}	CKE≤V_{IL}(max), t_{CC}=15ns		25		mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), t_{CC}= ∞		15			
Active Standby Current in Non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		240		mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		80			
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst All Banks activated t_{CCD}=t_{CCD}(min)	3	720	640	mA	1, 2
			2	500	460		
			1	320	280		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	3	480	440	mA	3
			2	440	400		
			1	400	360		
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		12		mA	4
				2		mA	5

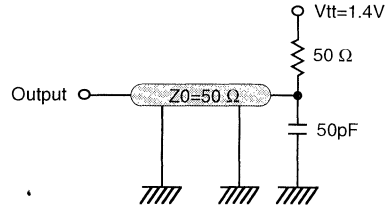
Note : 1. Measured with outputs open.
2. Assumes minimum column address update cycle t_{CCD}(min)
3. Refresh period is 64ms.
4. KMM366S203AT-G*
5. KMM366S203AT-F*

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70 °C)

Parameter	Value
AC input levels	V_{IH}/ V_{IL}= 2.4V / 0.4V
Input timing measurement reference level	1.4V
Input rise and fall time	tr / tf = 1ns /1ns
Output measurement reference level	1.4V
Output load condition	See Fig. 2



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	Version		Unit	Note
			-10	-12		
Row active to Row active delay		tRRD(min)	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	26	30	ns	1
Row precharge time		tRP(min)	26	30	ns	1
Row active time		tRAS(min)	60	66	ns	1
		tRAS(max)	200	200	us	
Row cycle time		tRC(min)	96	100	ns	1
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to Row precharge		tRDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	0		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS Latency= 3		2		ea	4
	CAS Latency= 2		1			
	CAS Latency= 1		0			

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of Row precharge interrupt, Auto precharge and Read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-10		-12		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	12	1000	ns	1
	CAS latency=2		15		15			1
	CAS latency=1		30		30			1
CLK to valid output delay	CAS latency=3	tSAC	-	7.5	-	9	ns	1, 2
	CAS latency=2		-	9.5	-	10		1, 2, 5, 6
	CAS latency=1		-	27	-	27		1, 2
Output data hold time		tOH	3		3		ns	2
CLK high pulse width		tCH	3.5		4		ns	3
CLK low pulse width		tCL	3.5		4		ns	3
Input setup time		tSS	3		3		ns	3
Input hold time		tSH	1		1.5		ns	3
Power down exit set-up time		tPDE	8		10		ns	4
CLK to output in low-Z		tSLZ	2		2		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ	-	8	-	9	ns	
	CAS latency=2		-	10	-	11		
	CAS latency=1		-	15	-	16		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2 - 1] ns should be added to the parameter.
4. A time of tPDE has to elapse after asserting CKE to resume normal operation when exiting both bank precharge power down mode.
5. If 3.15V≤VDD≤3.6V, tSAC = 9ns can be met @CAS latency=2 of - 10 part.
6. If 3.15V≤VDD≤3.6V, tSAC = 9.5ns can be met @CAS latency=2 of -12 part .

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S203AT-0

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		96ns	60ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	10	6	3	2	3	1	1	1
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	2	2	2	1	1	1
66MHz (15.2ns)	2	7	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	1	2	1	1	1
33MHz (30.3ns)	1	4	2	1	1	1	1	1	1
30MHz (33.3ns)	1	3	2	1	1	1	1	1	1

KMM366S203AT-2

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		100ns	66ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	9	6	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	3	2	3	1	1	1
66MHz (15.2ns)	2	7	5	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	6	4	2	2	2	1	1	1
33MHz (30.3ns)	1	4	3	1	1	1	1	1	1
30MHz (33.3ns)	1	3	2	1	1	1	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A11	A10	A9~A0	NOTE
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A8~A0)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A8~A0)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Bank									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H		X				V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A0 ~ A11 : Program keys.(@MRS)

2. MRS can be issued only at both bank precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions as same as CBR refresh of DRAM.
The automatical precharge without Row precharge command is meant by "Auto".
Auto/Self refresh can be issued only at both bank precharge state.

4. A11 : Bank select address.
If "Low" at read, write, Row active and precharge, bank A is selected.
If "High" at read, write, Row active and precharge, bank B is selected.
If A10 is "High" at Row precharge, A11 is ignored and both banks are selected.

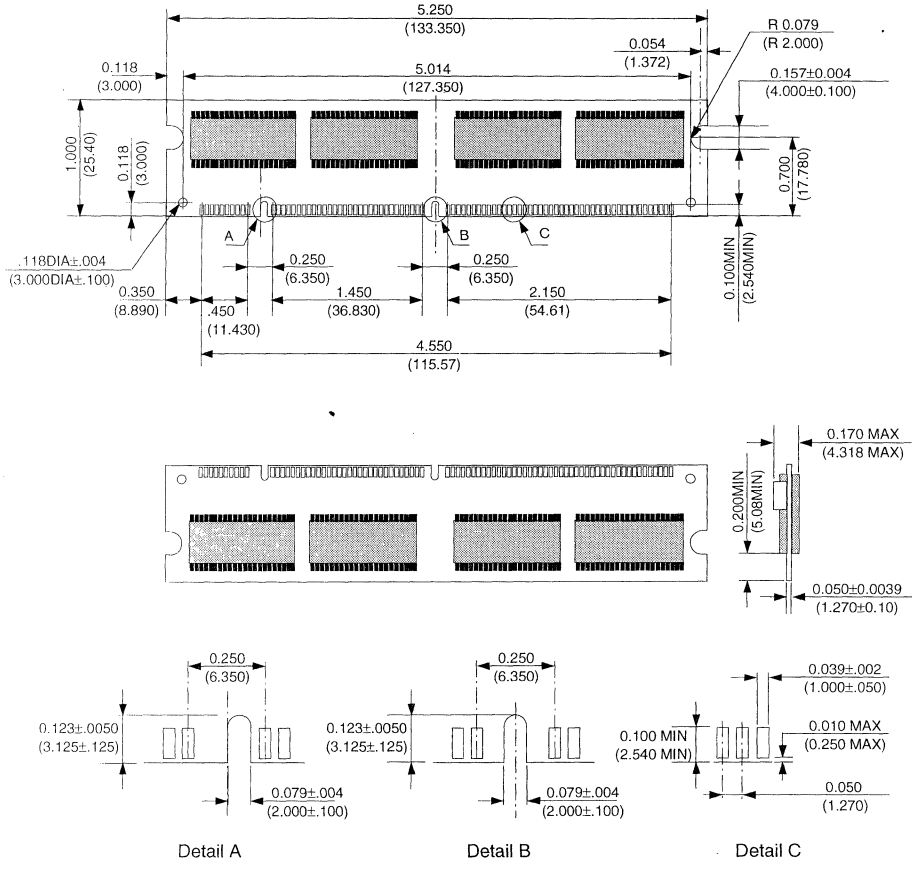
5. During burst read or write with auto precharge,
new read/write command cannot be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK
masks the data-in at the very CLK (Write DQM latency is 0)
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (millimeters)



Detail A Detail B Detail C

Tolerances : ±.005 (.13) unless otherwise specified

The used device is 2Mx8 SDRAM , TSOP
DRAM Part No. : KM48S2020AT .

KMM366S400AT SDRAM DIMM

4Mx64 SDRAM DIMM based on 4Mx4, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S400AT is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S400AT consists of sixteen CMOS 4Mx4 bit Synchronous DRAMs in TSOP-II 400mil packages and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The KMM366S400AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURES

- Performance Range

	Max Freq. (Speed)
KMM366S400AT - 0	100 MHz (10ns)
KMM366S400AT- 2	83 MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles/64 ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs.
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full Page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	*A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A14	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A15	160	DQ62
21	NC	49	VDD	77	DQ31	105	NC	133	VDD	161	DQ63
22	NC	50	NC	78	Vss	106	NC	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	NC	80	NC	108	NC	136	NC	164	NC
25	NC	53	NC	81	NC	109	NC	137	NC	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A10	Address input (multiplexed)
A11	Select Bank
DQ0 ~ 63	Data Input/Output
CLK0, CLK1	Clock input
CKE	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
NC	No Connection
*VREF	Power Supply for Reference
**SDA	Serial Address/Data/I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don't Use

* These pins are not used in this module.

** These pins should be NC in system which does not support SPD.

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE, and DQM
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power down in standby. CKE should be enabled t_{PDE} prior to valid command.
A0 ~ A10	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, Column address : CA0 ~ CA9
A11	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte Masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	

SERIAL PRESENCE DETECT INFORMATION

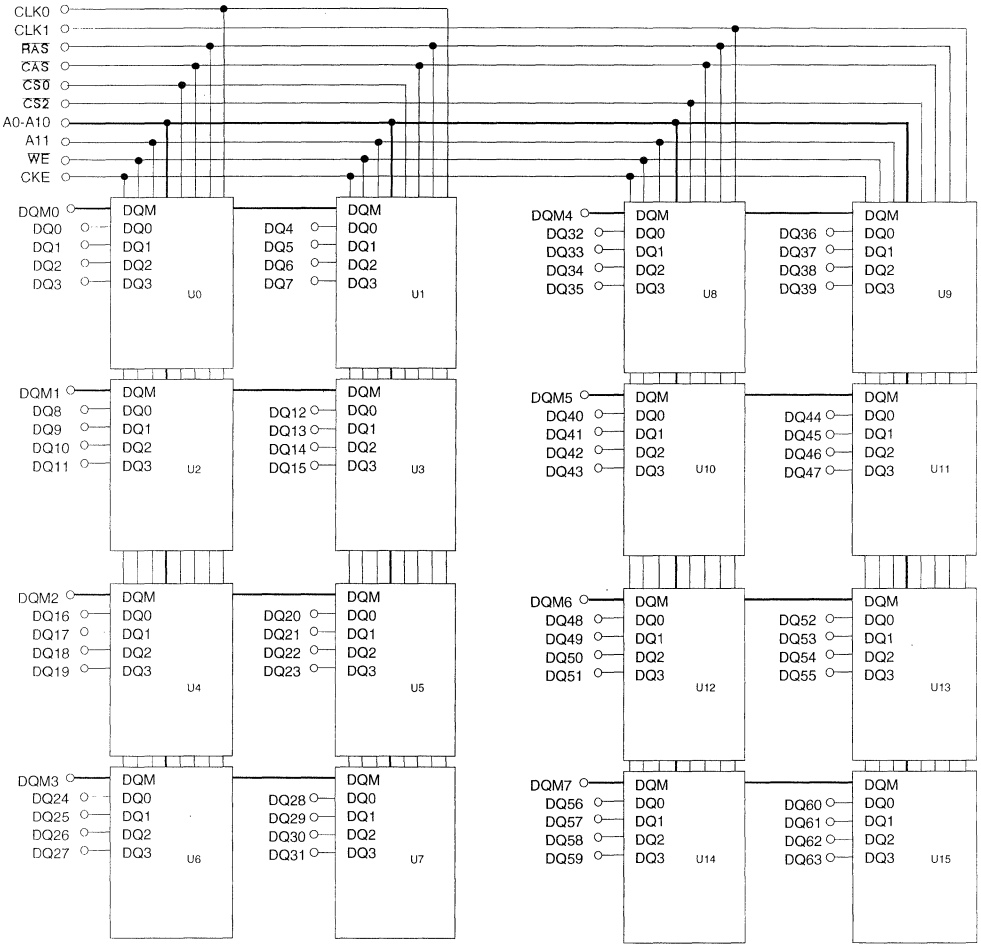
- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver ≤ 3mA
- Maximum clock frequency : 80KHz
- Contents :

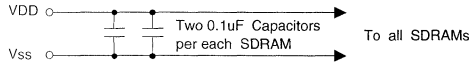
Byte No.	Function described	Function supported	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	12	0Ch	1
4	# of column addresses on this assembly	11	0Bh	2
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	64 bits	40h	
7	.....Data width of this assembly (Continued)	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	10ns	A0h	3, 8
		12ns	C0h	3, 8
10	SDRAM access time from clock	7.5ns	75h	4, 8
		9ns	90h	4, 8
11	DIMM configuration type	Non-parity	00h	
12	Refresh rate/type	15.625us, Self-refresh supported	80h	
13	SDRAM module attributes	non-buffered, non-registered	00h	
14	SDRAM device attributes : General	Support Burst Read Single-bit Write, Precharge all & Auto precharge	0Eh	5
15	Minimum clock delay for back-to-back random column address	t_{CCD} = 1 CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	6
17	SDRAM device attributes : # of banks on SDRAM device	2 banks	02h	
18	SDRAM device attributes : CAS latency	CAS latency = 1, 2 & 3	07h	7
19	SDRAM device attributes : CS latency	CS latency = 0	01h	
20	SDRAM device attributes : Write latency	Write latency = 0	01h	
21 ~ 31	Reserved for future offerings	-	00h	
32 ~ 63	Superset information (may be used in future)	-	00h	
64 ~ 127	Manufacturer's information (optional)	-	00h	
128 +	Unused storage locations	-	XX	

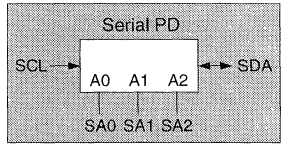
* Above data are based on the SPD specification of JEDEC standard and can be changed.

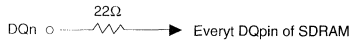
Note :
1. If the bank select address of RA11 is excluded, this byte must be programmed by 0Bh.
2. If the bank select address of CA11 is excluded, this byte must be programmed by 0Ah.
3. In case of - 10 part, the minimum cycle time is 10ns, 15ns and 30ns @CAS latency = 3, 2 and 1 respectively.
   So, the value of A0h is based on the minimum cycle time @CAS latency = 3.
   In case of - 12 part, the minimum cycle time is 12ns, 15ns and 30ns @CAS latency = 3, 2 & 1 respectively.
   So, the value of C0h is based on the minimum cycle time @CAS latency = 3.
4. In case of - 10 part, the access time is 7.5ns, 9.5ns and 27ns @CAS latency = 3, 2 and 1 respectively.
   So, the value of 75h is based on the access time @CAS latency = 3.
   In case of - 12 part, the access time is 9ns, 10ns and 27ns @CAS latency = 3, 2 and 1 respectively.
   So, the value of 90h is based on the access time @CAS latency = 3.
5. SEC's SDRAM supports Burst Read Single-bit Write, Precharge all and Auto precharge functions.
   If Burst Read Single-bit Write function is not supported, this byte must be programmed by 06h.
6. SEC's SDRAM supports burst lengths of 1, 2, 4, 8 and full page. If burst lengths of 1 and 4 are only supported, this byte must be programmed by 05h.
7. SEC's SDRAM supports CAS latency of 1, 2 and 3. If CAS latency of 2 and 3 are only supported, this byte must be programmed by 06h.
8. This value is based on the component specification.

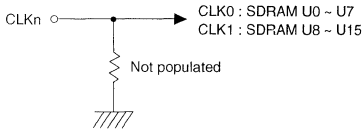
FUNCTIONAL BLOCK DIAGRAM











ABSOLUTE MAXIMUM RATINGS

Paramerter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	16	W
Short circuit current	Ios	50	mA

Note : Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltages referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	
Input low voltage	V_{IL}	-0.3	0	0.8	V	Note 1
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH}=-2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL}= 2mA
Input leakage current	I_{IL}	-80	-	80	uA	Note 2
Output leakage current	I_{OL}	-5	-	5	uA	Note 3

Note : 1. V_{IL}(min.) = -1.5V AC (pulse width ≤ 5 ns)
2. Any input 0 ≤ V_{IN} ≤ V_{DD}+0.3V, all other pins not under test = 0 Volt
3. Dout is disabled, 0V ≤ Vout ≤ V_{DD}

CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11)	C_{IN1}	-	80	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	C_{IN2}	-	80	pF
Input capacitance (CLK0, CLK1)	C_{IN3}	-	45	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN4}	-	45	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN5}	-	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	10	pF

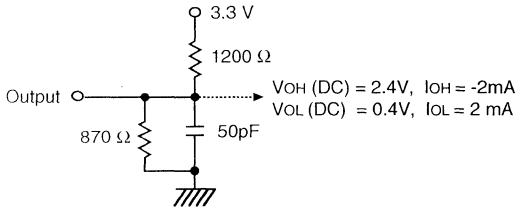
DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Version -12	Unit	Note
Operating Current	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA	3	1180	1100	mA	1
			2	1040	960		
			1	920	840		
Precharge Standby Current in Power-down mode	I_{CC2P}	CKE≤V_{IL}(max), t_{CC}=15ns		40		mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), t_{CC}= ∞		24			
Precharge Standby Current in Non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		400		mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		100			
Active Standby Current in Power-down mode	I_{CC3P}	CKE≤V_{IL}(max), t_{CC}=15ns		50		mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), t_{CC}= ∞		30			
Active Standby Current in Non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		480		mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		150			
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst All Banks activated t_{CCD}=t_{CCD}(min)	3	1320	1160	mA	1, 2
			2	920	840		
			1	580	500		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	3	960	880	mA	3
			2	860	780		
			1	760	680		
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		24		mA	4
				4		mA	5

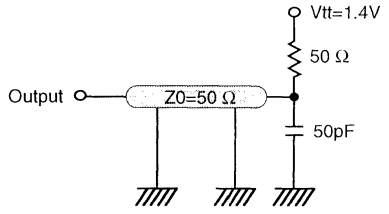
Note : 1. Measured with outputs open.
2. Assumes minimum column address update cycle t_{CCD}(min)
3. Refresh period is 64ms.
4. KMM366S400AT-G*
5. KMM366S400AT-F*

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70 °C)

Parameter	Value
AC input levels	V_{IH}/ V_{IL}= 2.4V / 0.4V
Input timing measurement reference level	1.4V
Input rise and fall time	tr / tf = 1ns / 1ns
Output measurement reference level	1.4V
Output load condition	See Fig. 2



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	Version		Unit	Note
			- 10	- 12		
Row active to Row active delay		tRRD(min)	20	24	ns	1
RAS to CAS delay		tRCD(min)	26	30	ns	1
Row precharge time		tRP(min)	26	30	ns	1
Row active time		tRAS(min)	60	66	ns	1
		tRAS(max)	200	200	us	
Row cycle time		tRC(min)	96	100	ns	1
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to Row precharge		tRDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	0		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS Latency= 3		2		ea	4
	CAS Latency= 2		1			
	CAS Latency= 1		0			

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of Row precharge interrupt, Auto precharge and Read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-10		-12		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	12	1000	ns	1
	CAS latency=2		15		15			1
	CAS latency=1		30		30			1
CLK to valid output delay	CAS latency=3	tSAC	-	7.5	-	9	ns	1, 2
	CAS latency=2		-	9.5	-	10		1, 2, 5, 6
	CAS latency=1		-	27	-	27		1, 2
Output data hold time		tOH	3		3		ns	2
CLK high pulse width		tCH	3.5		4		ns	3
CLK low pulse width		tCL	3.5		4		ns	3
Input setup time		tSS	3		3		ns	3
Input hold time		tSH	1		1.5		ns	3
Power down exit set-up time		tPDE	8		10		ns	4
CLK to output in low-Z		tSLZ	2		2		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ	-	8	-	9	ns	
	CAS latency=2		-	10	-	11		
	CAS latency=1		-	15	-	16		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2 - 1] ns should be added to the parameter.
4. A time of tPDE has to elapse after asserting CKE to resume normal operation when exiting both bank precharge power down mode.
5. If 3.15V≤VDD≤3.6V, tSAC = 9ns can be met @CAS latency=2 of - 10 part.
6. If 3.15V≤VDD≤3.6V, tSAC = 9.5ns can be met @CAS latency=2 of -12 part .

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S400AT-0

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		96ns	60ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	10	6	3	2	3	1	1	1
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	2	2	2	1	1	1
66MHz (15.2ns)	2	7	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	1	2	1	1	1
33MHz (30.3ns)	1	4	2	1	1	1	1	1	1
30MHz (33.3ns)	1	3	2	1	1	1	1	1	1

KMM366S400AT-2

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		100ns	66ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	9	6	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	3	2	3	1	1	1
66MHz (15.2ns)	2	7	5	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	6	4	2	2	2	1	1	1
33MHz (30.3ns)	1	4	3	1	1	1	1	1	1
30MHz (33.3ns)	1	3	2	1	1	1	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	A11	A10	A9~A0	NOTE
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A9~A0)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A9~A0)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Bank									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{11} : Program keys.(@MRS)

2. MRS can be issued only at both bank precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions as same as CBR refresh of DRAM.
The automatical precharge without Row precharge command is meant by "Auto".
Auto/Self refresh can be issued only at both bank precharge state.

4. A_{11} : Bank select address.
If "Low" at read, write, Row active and precharge, bank A is selected.
If "High" at read, write, Row active and precharge, bank B is selected.
If A_{10} is "High" at Row precharge, A_{11} is ignored and both banks are selected.

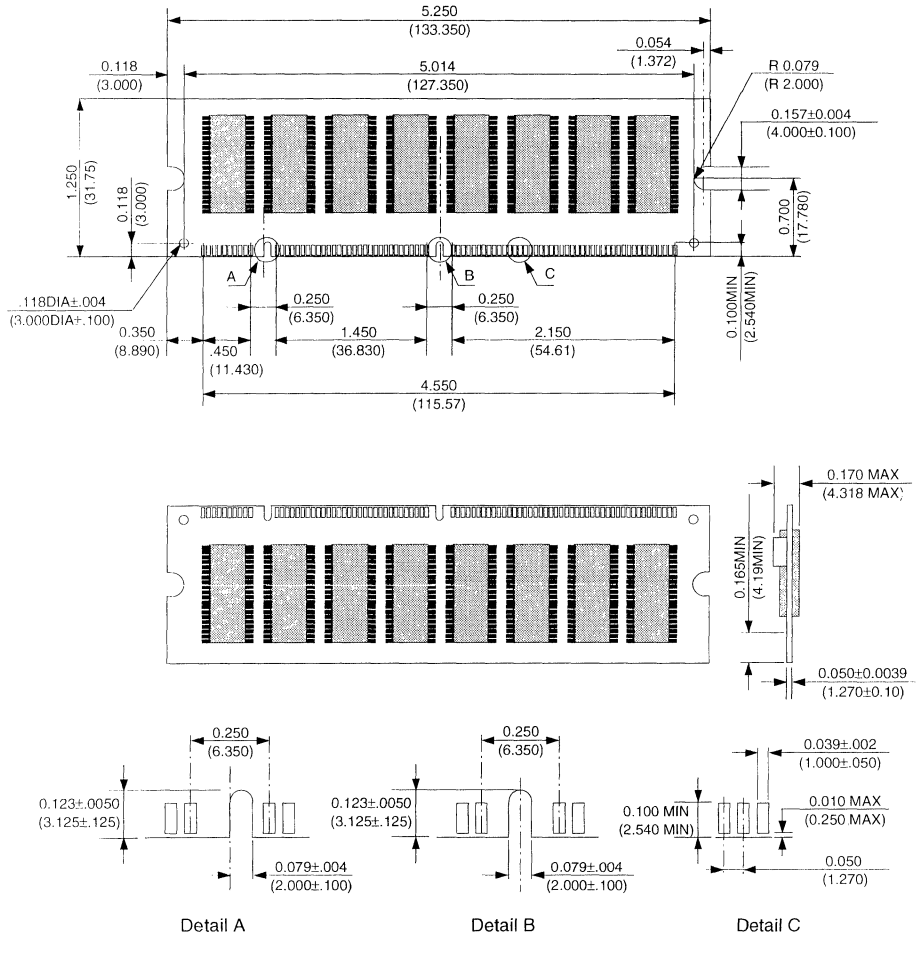
5. During burst read or write with auto precharge,
new read/write command cannot be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK
masks the data-in at the very CLK (Write DQM latency is 0)
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (millimeters)



Detail A Detail B Detail C

Tolerances : ±.005 (.13) unless otherwise specified

The used device is 4Mx4 SDRAM , TSOP
DRAM Part No. : KM44S4020AT .

KMM366S403AT1 SDRAM DIMM

4Mx64 SDRAM DIMM based on 2Mx8, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S403AT1 is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S403AT1 consists of sixteen CMOS 2Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The KMM366S403AT1 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURES

• Performance Range

	Max Freq. (Speed)
KMM366S403AT1 - 0	100 MHz (10ns)
KMM366S403AT1- 2	83 MHz (12ns)

• Burst Mode Operation
• Auto & Self Refresh Capability (4096 cycles/64 ms)
• LVTTL compatible inputs and outputs
• Single 3.3V±0.3V power supply
• WCBR cycle with address key programs.
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full Page)
  Data Scramble (Sequential & Interleave)
• All inputs are sampled at the positive going edge of the system clock
• Serial Presence Detect with EEPROM
• PCB : **Height(1,250mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	*A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A14	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A15	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A10	Address input (multiplexed)
A11	Select Bank
DQ0 ~ 63	Data Input/Output
*CB0 ~ 7	Check bit (Data-in/data-out)
CLK0, *CLK1	Clock input
CKE	Clock Enable Input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip Select Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
NC	No Connection
*VREF	Power Supply for Reference
**SDA	Serial Address/Data/I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don't Use

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE, and DQM
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power down in standby. CKE should be enabled t_{PDE} prior to valid command.
A0 ~ A10	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, Column address : CA0 ~ CA8
A11	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte Masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	

3

SERIAL PRESENCE DETECT INFORMATION

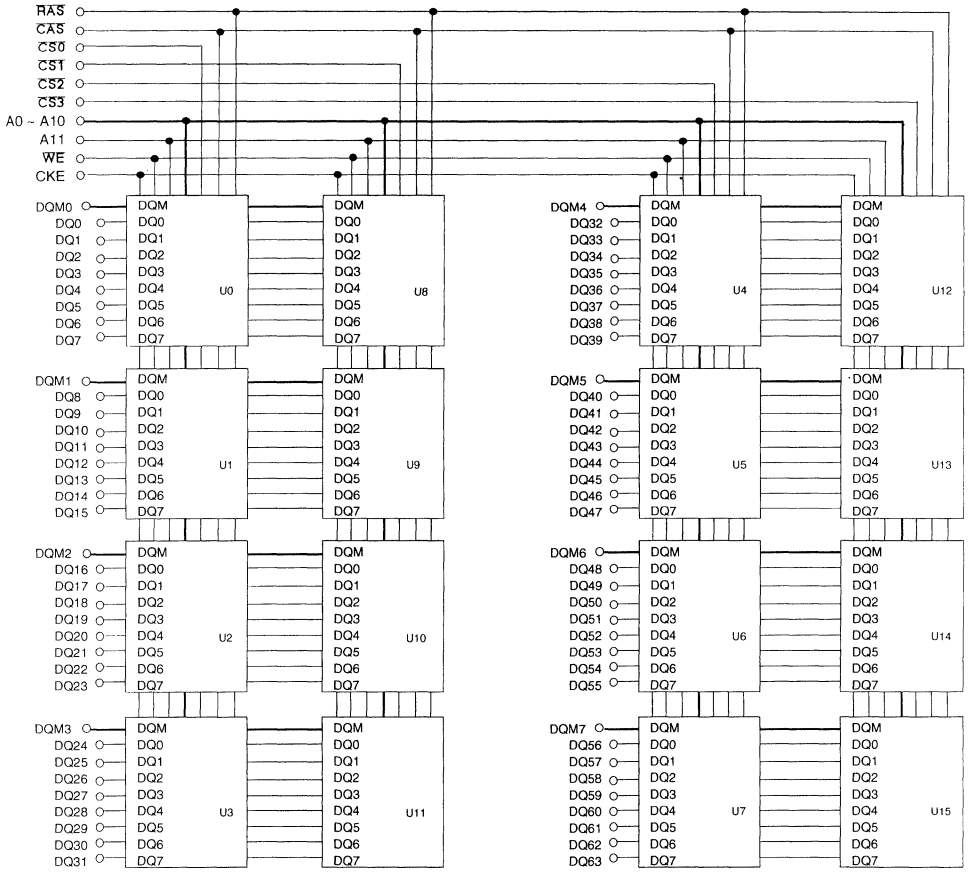
- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver ≤ 3mA
- Maximum clock frequency : 80KHz
- Contents :

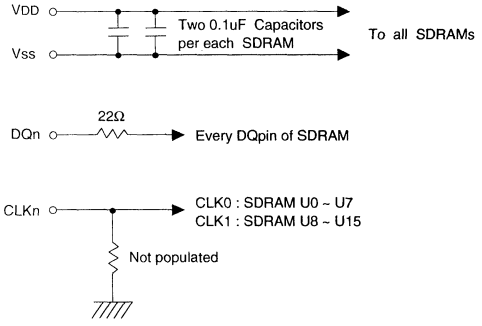
Byte No.	Function described	Function supported	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	12	0Ch	1
4	# of column addresses on this assembly	10	0Ah	2
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	64 bits	40h	
7	.....Data width of this assembly (Continued)	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	10ns	A0h	3, 8
		12ns	C0h	3, 8
10	SDRAM access time from clock	7.5ns	75h	4, 8
		9ns	90h	4, 8
11	DIMM configuration type	Non-parity	00h	
12	Refresh rate/type	15.625us, Self-refresh supported	80h	
13	SDRAM module attributes	non-buffered, non-registered	00h	
14	SDRAM device attributes : General	Support Burst Read Single-bit Write, Precharge all & Auto precharge	0Eh	5
15	Minimum clock delay for back-to-back random column address	tCCD = 1 CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	6
17	SDRAM device attributes : # of banks on SDRAM device	2 banks	02h	
18	SDRAM device attributes : CAS latency	CAS latency = 1, 2 & 3	07h	7
19	SDRAM device attributes : CS latency	CS latency = 0	01h	
20	SDRAM device attributes : Write latency	Write latency = 0	01h	
21 ~ 31	Reserved for future offerings	-	00h	
32 ~ 63	Superset information (may be used in future)	-	00h	
64 ~ 127	Manufacturer's information (optional)	-	00h	
128 +	Unused storage locations	-	XX	

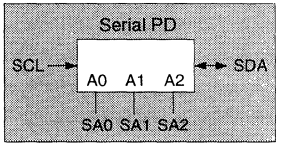
* Above data are based on the SPD specification of JEDEC standard and can be changed.

Note :
1. If the bank select address of RA11 is excluded, this byte must be programmed by 0Bh.
2. If the bank select address of CA11 is excluded, this byte must be programmed by 09h.
3. In case of - 10 part, the minimum cycle time is 10ns, 15ns and 30ns @CAS latency = 3, 2 and 1 respectively.
   So, the value of A0h is based on the minimum cycle time @CAS latency = 3.
   In case of - 12 part, the minimum cycle time is 12ns, 15ns and 30ns @CAS latency = 3, 2 & 1 respectively.
   So, the value of C0h is based on the minimum cycle time @CAS latency = 3.
4. In case of - 10 part, the access time is 7.5ns, 9.5ns and 27ns @CAS latency = 3, 2 and 1 respectively.
   So, the value of 75h is based on the access time @CAS latency = 3.
   In case of - 12 part, the access time is 9ns, 10ns and 27ns @CAS latency = 3, 2 and 1 respectively.
   So, the value of 90h is based on the access time @CAS latency = 3.
5. SEC's SDRAM supports Burst Read Single-bit Write, Precharge all and Auto precharge functions.
   If Burst Read Single-bit Write function is not supported, this byte must be programmed by 06h.
6. SEC's SDRAM supports burst lengths of 1, 2, 4, 8 and full page. If burst lengths of 1 and 4 are only supported, this byte must be programmed by 05h.
7. SEC's SDRAM supports CAS latency of 1, 2 and 3. If CAS latency of 2 and 3 are only supported, this byte must be programmed by 06h.
8. This value is based on the component specification.

FUNCTIONAL BLOCK DIAGRAM







ABSOLUTE MAXIMUM RATINGS

Paramerter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	16	W
Short circuit current	Ios	50	mA

Note : Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltages referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	
Input low voltage	V_{IL}	-0.3	0	0.8	V	Note 1
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH}=-2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL}= 2mA
Input leakage current	I_{IL}	-80	-	80	uA	Note 2
Output leakage current	I_{OL}	-10	-	10	uA	Note 3

Note : 1. V_{IL}(min.) = -1.5V AC (pulse width ≤ 5 ns)
2. Any input 0 ≤ V_{IN} ≤ V_{DD}+0.3V, all other pins not under test = 0 Volt
3. Dout is disabled, 0V ≤ Vout ≤ V_{DD}

CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11)	C_{IN1}	-	80	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	C_{IN2}	-	80	pF
Input capacitance (CLK0, CLK1)	C_{IN3}	-	45	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS3}$)	C_{IN4}	-	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN5}	-	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

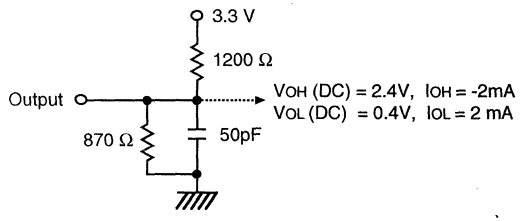
DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Version -12	Unit	Note
Operating Current	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA	3	800	760	mA	1
			2	740	700		
			1	680	640		
Precharge Standby Current in Power-down mode	I_{CC2P}	CKE≤V_{IL}(max), t_{CC}=15ns		40		mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), t_{CC}= ∞		24			
Precharge Standby Current in Non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		400		mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		100			
Active Standby Current in Power-down mode	I_{CC3P}	CKE≤V_{IL}(max), t_{CC}=15ns		50		mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), t_{CC}= ∞		30			
Active Standby Current in Non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		480		mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		160			
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst All Banks activated t_{CCD}=t_{CCD}(min)	3	920	840	mA	1, 2
			2	700	660		
			1	520	480		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	3	680	640	mA	3
			2	640	600		
			1	600	560		
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		24		mA	4
				4		mA	5

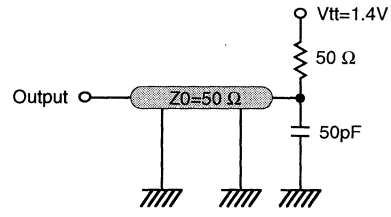
Note : 1. Measured with outputs open.
2. Assumes minimum column address update cycle t_{CCD}(min)
3. Refresh period is 64ms.
4. KMM366S403AT1-G*
5. KMM366S403AT1-F*

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70 °C)

Parameter	Value
AC input levels	V_{IH}/ V_{IL}= 2.4V / 0.4V
Input timing measurement reference level	1.4V
Input rise and fall time	tr / tf = 1ns /1ns
Output measurement reference level	1.4V
Output load condition	See Fig. 2



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	Version		Unit	Note
			-10	-12		
Row active to Row active delay		tRRD(min)	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	26	30	ns	1
Row precharge time		tRP(min)	26	30	ns	1
Row active time		tRAS(min)	60	66	ns	1
		tRAS(max)	200	200	us	
Row cycle time		tRC(min)	96	100	ns	1
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to Row precharge		tRDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	0		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS Latency= 3		2		ea	4
	CAS Latency= 2		1			
	CAS Latency= 1		0			

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of Row precharge interrupt, Auto precharge and Read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-10		-12		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	12	1000	ns	1
	CAS latency=2		15		15			1
	CAS latency=1		30		30			1
CLK to valid output delay	CAS latency=3	tSAC	-	7.5	-	9	ns	1, 2
	CAS latency=2		-	9.5	-	10		1, 2, 5, 6
	CAS latency=1		-	27	-	27		1, 2
Output data hold time		tOH	3		3		ns	2
CLK high pulse width		tCH	3.5		4		ns	3
CLK low pulse width		tCL	3.5		4		ns	3
Input setup time		tSS	3		3		ns	3
Input hold time		tSH	1		1.5		ns	3
Power down exit set-up time		tPDE	8		10		ns	4
CLK to output in low-Z		tSLZ	2		2		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ	-	8	-	9	ns	
	CAS latency=2		-	10	-	11		
	CAS latency=1		-	15	-	16		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2 - 1] ns should be added to the parameter.
4. A time of tPDE has to elapse after asserting CKE to resume normal operation when exiting both bank precharge power down mode.
5. If 3.15V≤VDD≤3.6V, tSAC = 9ns can be met @CAS latency=2 of - 10 part.
6. If 3.15V≤VDD≤3.6V, tSAC = 9.5ns can be met @CAS latency=2 of -12 part .

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S403AT1-0

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		96ns	60ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	10	6	3	2	3	1	1	1
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	2	2	2	1	1	1
66MHz (15.2ns)	2	7	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	1	2	1	1	1
33MHz (30.3ns)	1	4	2	1	1	1	1	1	1
30MHz (33.3ns)	1	3	2	1	1	1	1	1	1

KMM366S403AT1-2

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		100ns	66ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	9	6	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	3	2	3	1	1	1
66MHz (15.2ns)	2	7	5	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	6	4	2	2	2	1	1	1
33MHz (30.3ns)	1	4	3	1	1	1	1	1	1
30MHz (33.3ns)	1	3	2	1	1	1	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A11	A10	A9~A0	NOTE
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A8~A0)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A8~A0)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Bank									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H			X			V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{11} : Program keys.(@MRS)

2. MRS can be issued only at both bank precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions as same as CBR refresh of DRAM.
The automatical precharge without Row precharge command is meant by "Auto".
Auto/Self refresh can be issued only at both bank precharge state.

4. A_{11} : Bank select address.
If "Low" at read, write, Row active and precharge, bank A is selected.
If "High" at read, write, Row active and precharge, bank B is selected.
If A_{10} is "High" at Row precharge, A_{11} is ignored and both banks are selected.

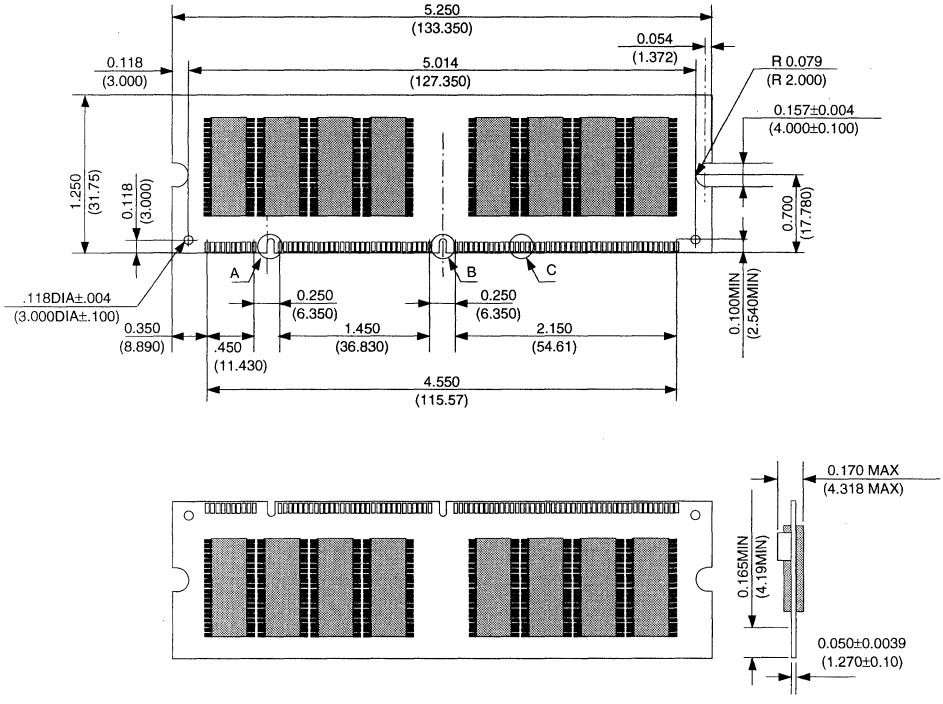
5. During burst read or write with auto precharge,
new read/write command cannot be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

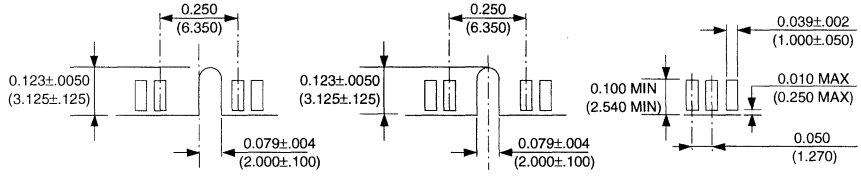
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK
masks the data-in at the very CLK (Write DQM latency is 0)
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (millimeters)

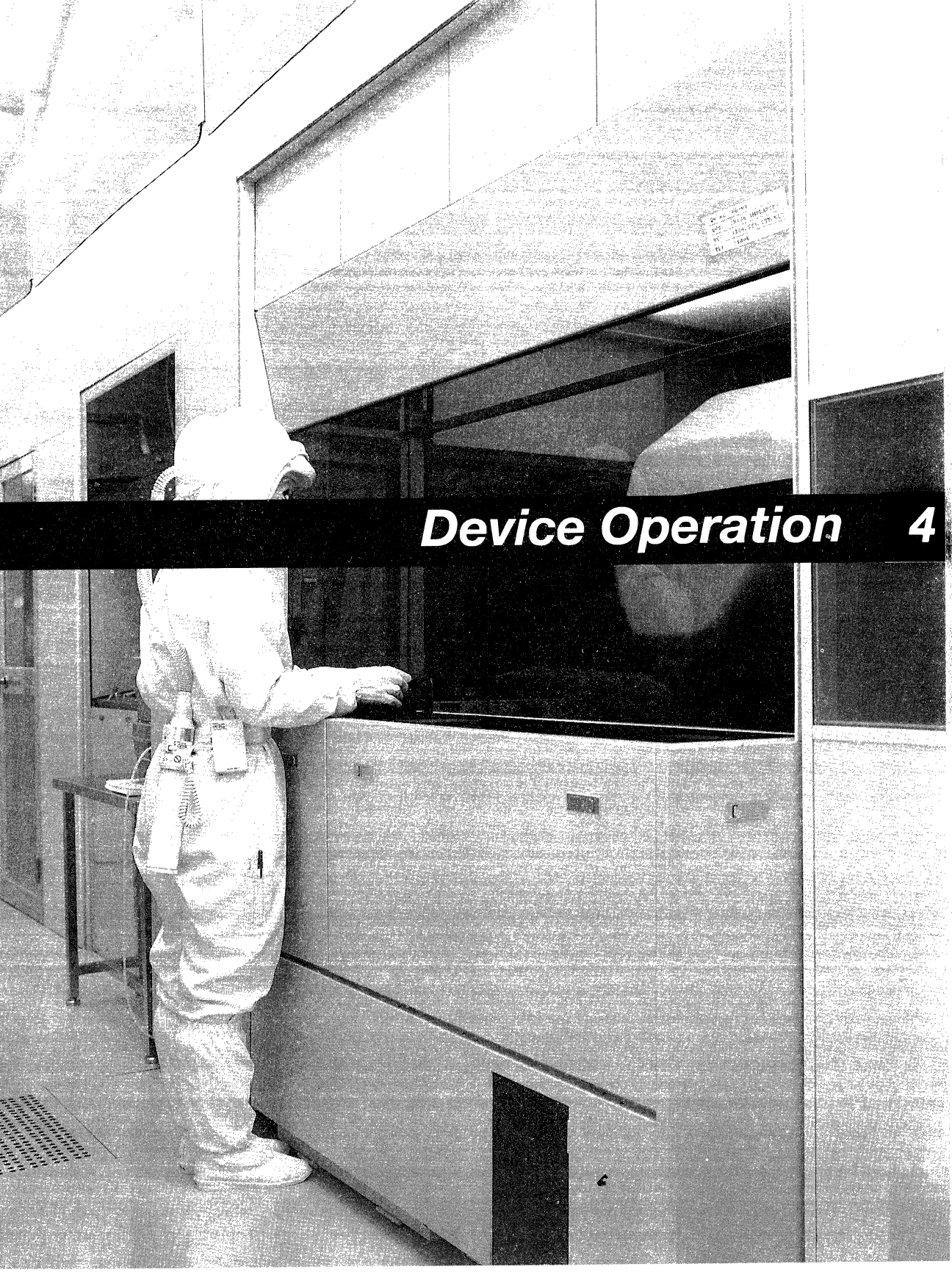




Detail A Detail B Detail C

Tolerances : ±.005 (.13) unless otherwise specified

The used device is 2Mx8 SDRAM , TSOP
DRAM Part No. : KM48S2020AT .



Device Operation 4

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	A11 ~A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU	W.B.L	TM		CAS Latency			BT	Burst Length		
	(Note 2)	(Note 1)									

Test Mode			CAS Latency				Burst Type		Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT = 0	BT = 1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	Reserved
0	1	Reserved	0	0	1	1	1	Interleave	0	0	1	2	Reserved
1	0	Reserved	0	1	0	2			0	1	0	4	4
1	1	Reserved	0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A9		Length	1	0	1	Reserved			1	0	1	Reserved	Reserved
0		Burst	1	1	0	Reserved			1	1	0	Reserved	Reserved
1		Single Bit	1	1	1	Reserved			1	1	1	Full Page	Reserved

Full Page Length : X4 (1024), X8 (512), X16 (256)

4

POWER UP SEQUENCE

1. Apply power and start clock, Attempt to maintain CKE="H", DQM="H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200μs.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

cf.) Sequence of 4 & 5 are regardless of the order.

The device is now ready for normal operation.

NOTE : 1. If A9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
2. RFU (Reserved for future use) should stay "0" during MRS cycle.

BURST SEQUENCE (BURST LENGTH = 4)

Initial address		Sequential				Interleave			
A_1	A_0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

BURST SEQUENCE (BURST LENGTH = 8)

Initial address			Sequential								Interleave							
A_2	A_1	A_0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

DEVICE OPERATIONS

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operation are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high, all inputs are assumed to be in valid state (low or high) for the duration of set-up and hold time around positive edge of the clock for proper functionality and Icc specifications.

CLOCK ENABLE (CKE)

The clock enable(CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When both banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "tPDE" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

BANK SELECT (A_{11})

: In case X4

This SDRAM is organized as two independent banks of 2,097,152 words x 4 bits memory arrays. The A_{11} input is latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. When A_{11} is asserted low, bank A is selected. When A_{11} is asserted high, bank B is selected. The bank select A_{11} is latched at bank activate, read, write, mode register set and precharge operations.

: In case X8

This SDRAM is organized as two independent banks of 1,048,576words x 8 bits memory arrays. The A_{11} input is latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. When A_{11} is asserted low, bank A is selected. When A_{11} is asserted high, bank B is selected. The bank select A_{11} is latched at bank activate, read, write, mode register set and precharge operations.

: In case X16

This SDRAM is organized as two independent banks of 524,288 words x 16 bits memory arrays. The A_{11} input is latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. When A_{11} is asserted low, bank A is selected. When A_{11} is asserted high, bank B is selected. The bank select A_{11} is latched at bank activate, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A_0~A_{10})

: In case X4

The 21 address bits required to decode the 2,097,152 word locations are multiplexed into 11 address input pins (A_0~A_{10}). The 11 bit row address is latched along with $\overline{RAS}$ and A_{11} during bank activate command. The 10 bit column address is latched along with $\overline{CAS}$, $\overline{WE}$ and A_{11} during read or write command.

: In case X8

The 20 address bits required to decode the 1,048,576 word locations are multiplexed into 11 address input pins (A_0~A_{10}). The 11 bit row address is latched along with $\overline{RAS}$ and A_{11} during bank activate command. The 9 bit column address is latched along with $\overline{CAS}$, $\overline{WE}$ and A_{11} during read or write command.

: In case X16

The 19 address bits required to decode the 524,288 word locations are multiplexed into 11 address input pins (A_0~A_{10}). The 11 bit row address is latched along with $\overline{RAS}$ and A_{11} during bank activate command. The 8 bit column address is latched along with $\overline{CAS}$, $\overline{WE}$ and A_{11} during read or write command.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, the SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

POWER-UP

The following sequence is recommended for POWER UP

1. Power must be applied to either CKE and DQM inputs to pull them high and the other pins are NOP condition at the inputs before or along with V_{DD}(and V_{DDQ}) supply. The clock signal must also be asserted at the same time.
2. After V_{DD} reaches the desired voltage, a minimum pause of 200 microseconds is required with inputs in NOP condition.
3. Both banks must be precharged now.
4. Perform a minimum of 2 Auto refresh cycles to stabilize the internal circuitry.
5. Perform a MODE REGISTER SET cycle to program the CAS latency, burst length and burst type as the default value of mode register is undefined.

   At the end of two clock cycles from the mode register set cycle, the device is ready for operation.

DEVICE OPERATIONS

When the above sequence is used for Power-up, all the outputs will be in high impedance state. The high impedance of outputs is not guaranteed in any other power-up sequence.
cf) Sequence 4 & 5 can be changed

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A_0~A_{10} and A_{11} in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as both banks are in the idle state.
The mode register is divided into various fields depending on functionality. The burst length field uses A_0~A_2, burst type uses A_3, CAS latency (read latency from column address) uses A_4~A_6, A_7, A_8, A_{10} and A_{11} are used for vendor specific options or test mode. And the write burst length is programmed using A_9. A_7,A_8,A_{10} and A_{11} must be set to low for normal SDRAM operation.
Refer to table for specific codes for various burst length, burst type and CAS latencies.

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank address a row access is initiated. The read or write operation can occur after a time delay of t_{RCD}(min) from the time of bank activation.
t_{RCD}(min) is an internal timing parameter of SDRAM therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing t_{RCD}(min) with cycle time of the clock and then rounding off the result to the next higher integer. The SDRAM has two internal banks on the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of both banks immediately. Also the noise generated during sensing of each bank of SDRAM is high requiring some time for power supplies to recover before the other bank can be sensed reliably. t_{RRD}(min) specifies the minimum time required between activating different banks. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t_{RAS}(min). Every SDRAM bank activate command must satisfy t_{RAS}(min) specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t_{RAS}(max). The number of cycles for both t_{RAS}(min) and t_{RAS}(max) can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{CAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least t_{RCD}(min) before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of the burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

BURST WRITE

The burst write command is similar to burst read command, and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing may not have been completed yet. The writing can to complete to burst length. The burst write can be terminated by issuing a burst read and DQM for blocking data inputs or burst write in the same or the other active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and precharging the bank "t_{RDL}" after the last data input to be written into the active row. See DQM OPERATION also.

DEVICE OPERATIONS (Continued)

DQM OPERATION

The DQM is used to mask input and output operations. It works similar to $\overline{OE}$ during read operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in the read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock, therefore the masking occurs for a complete cycle. The DQM signal is important during burst interrupts of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is not required. Please refer to DQM timing diagrams also.

PRECHARGE

The precharge operation is performed on an active bank by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A_{10} with valid A_{11} of the bank to be precharged. The precharge command can be asserted anytime after t_{RAS}(min) is satisfied from the bank activate command in the desired bank. "t_{RP}" is defined as the minimum time required to precharge a bank. The minimum number of clock cycles required to complete row precharge is calculated by dividing "t_{RP}" with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by t_{RAS}(max). Therefore, each bank has to be precharged within t_{RAS}(max) from the bank activate command. At the end of precharge, the bank enters the Idle state and is ready to be activated again. Entry to Power Down, Auto refresh, Self refresh and Mode register Set etc. is possible only when both banks are in idle state.

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy t_{RAS}(min) and "t_{RP}" for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst read or burst write by asserting high on A_{10}. If burst read or burst write command is issued with low on A_{10}, the bank is left active until a new command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

BOTH BANK PRECHARGE

Both banks can be precharged at the same time by using precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ with high on A_{10} after both banks have satisfied t_{RAS}(min) requirement, performs precharge on both banks. At the end of t_{RP} after performing precharge all, both banks are in idle state.

AUTO REFRESH

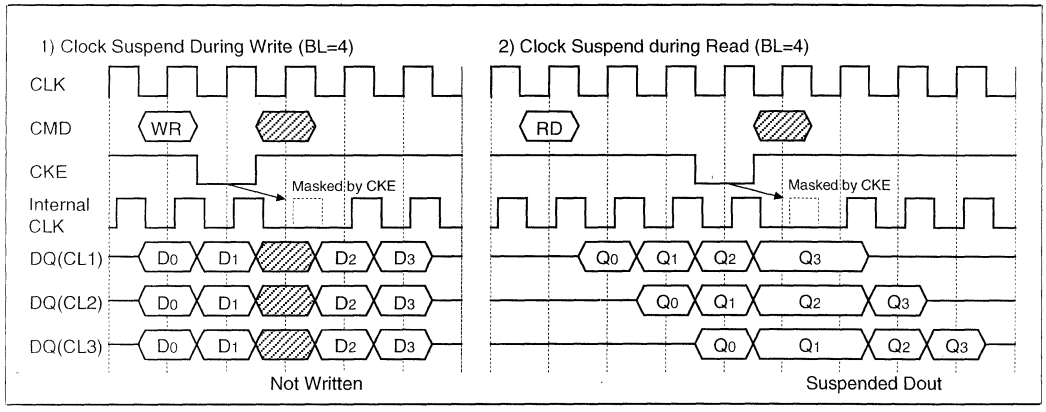
The storage cells of SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by "t_{RC}(min)". The minimum number of clock cycles required can be calculated by dividing "t_{RC}" with clock cycle time and then rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. Both banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6 μs or a burst of 4096 auto refresh cycles once in 64ms.
(x4, x8 : 4096 auto refresh cycles/64ms, x16 : 2048 auto refresh cycles/32ms)

SELF REFRESH

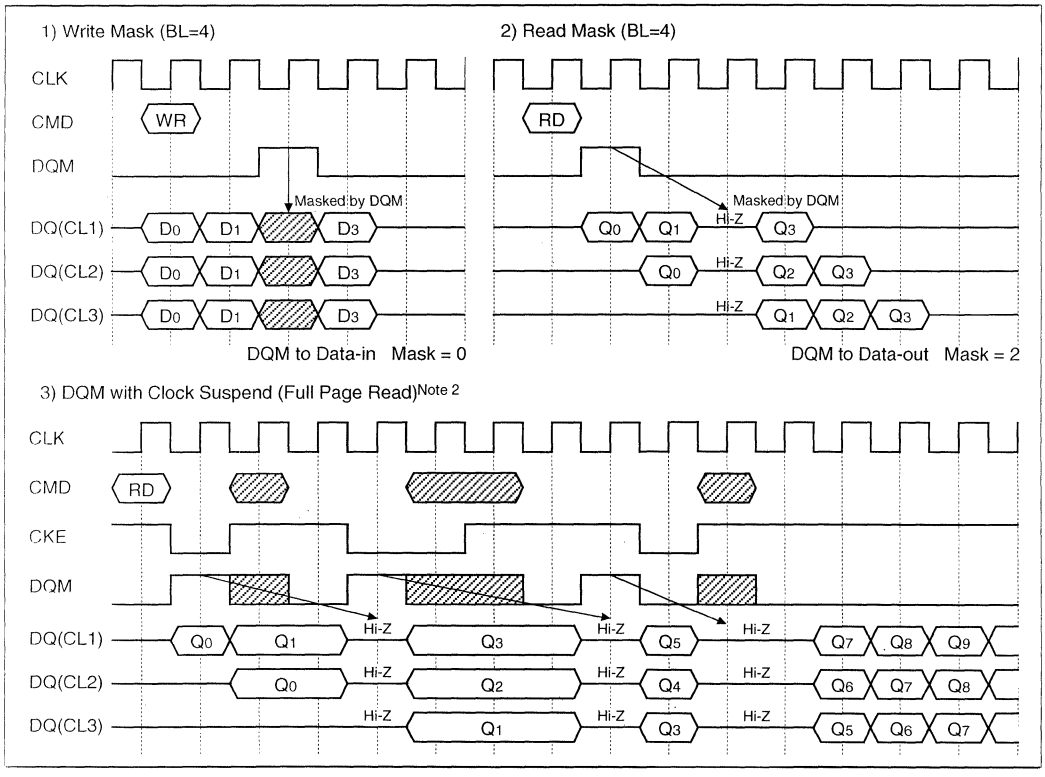
The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption.
The self refresh mode is entered from both bank idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including clock are ignored to remain in the self refresh.
The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of "t_{RC}" before the SDRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 4096 auto refresh cycles immediately after exiting self refresh.

BASIC FEATURE AND FUNCTION DESCRIPTIONS

1. CLOCK Suspend



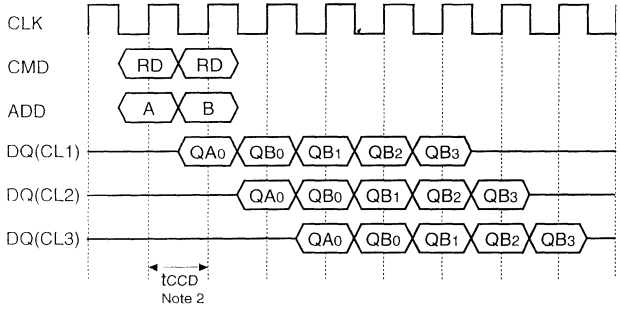
2. DQM Operation



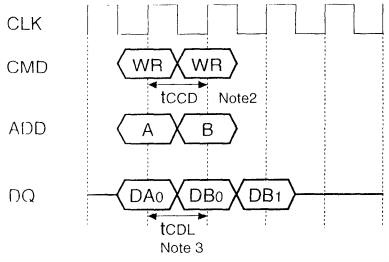
Note : 1. CKE to CLK disable/enable = 1 clock.
2 . DQM makes data out Hi-Z after 2 clocks which should masked by CKE "L".
3. DQM mask both data-in and data-out.

3. $\overline{CAS}$ Interrupt (I)

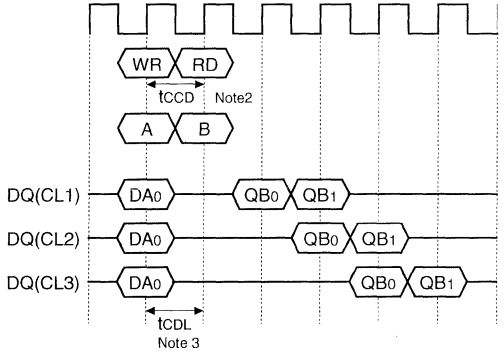
1) Read interrupted by Read (BL=4)[Note 1]



2) Write interrupted by Write (BL=2)



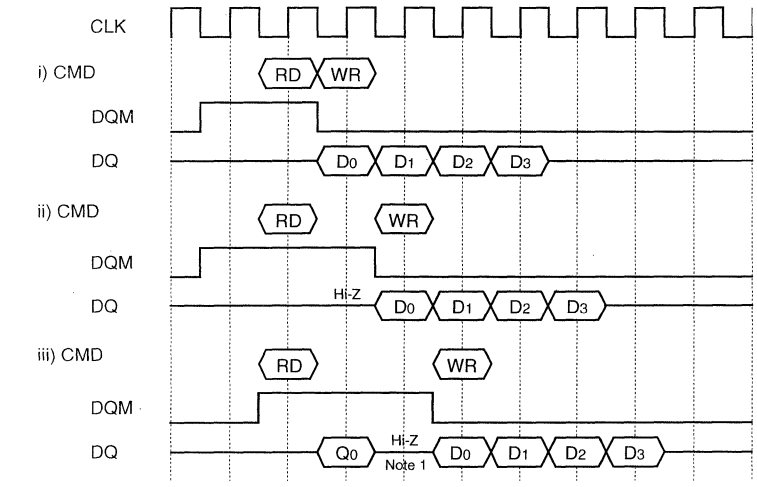
3) Write interrupted by Read (BL=2)



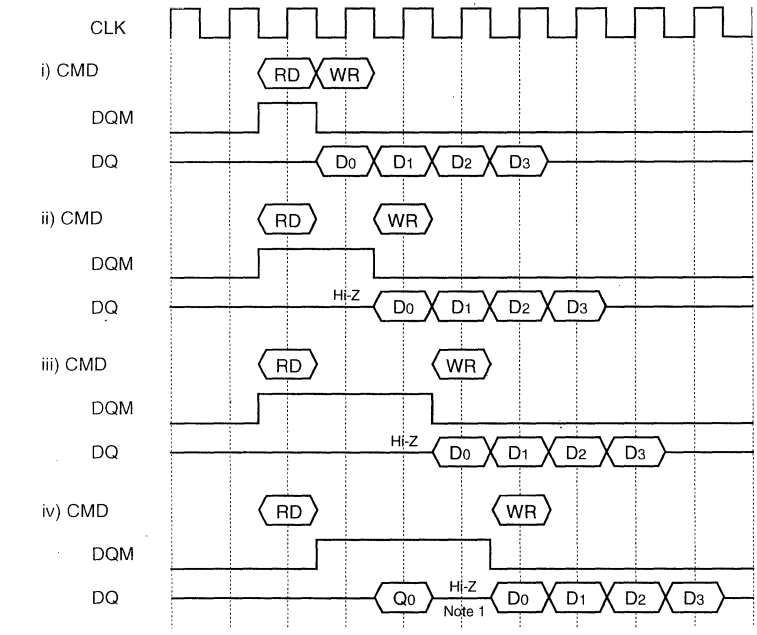
Note : 1. By "Interrupt", It is meant to stop burst read/write by external command before the end of burst.
By "$\overline{CAS}$ Interrupt", to stop burst read/write by $\overline{CAS}$ access ; read and write.
2. tCCD : $\overline{CAS}$ to $\overline{CAS}$ delay. (=1CLK)
3. tCDL : Last data in to new column address delay. (=1CLK)

4. $\overline{CAS}$ Interrupt (II) : Read Interrupted by Write & DQM

(a) CL=1, BL=4

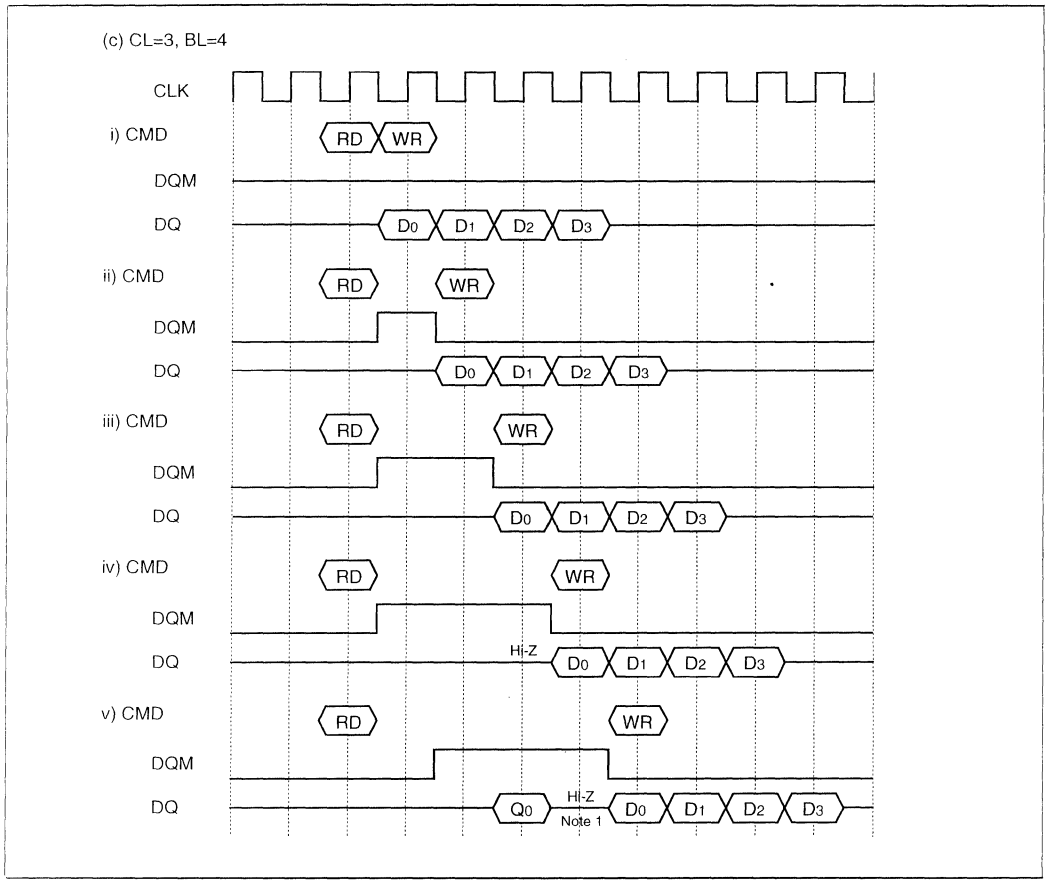


(b) CL=2, BL=4

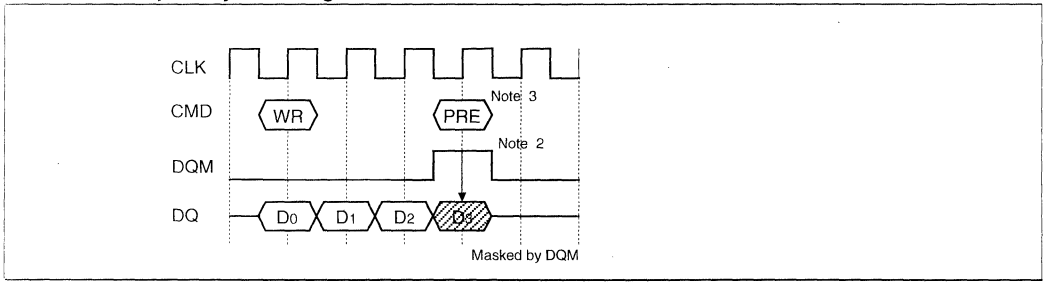


Note : 1. To prevent bus contention, there should be at least one gap between data in and data out.

(Continued)



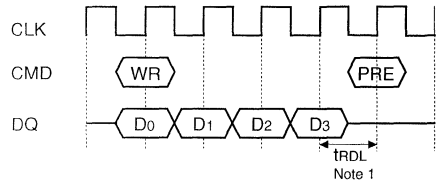
5. Write Interrupted by Precharge & DQM



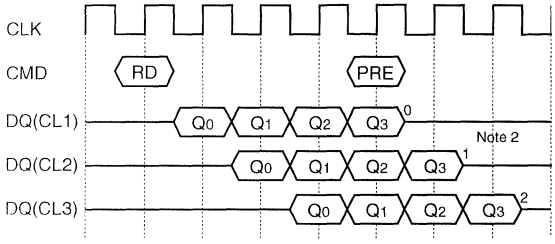
Note : 1. To prevent bus contension, DQM should be issued which makes at least one gap between data in and data out.
2. To inhibit invalid write, DQM should be issued.
3. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of dual bank operation.

6. Precharge

1) Normal Write (BL=4)

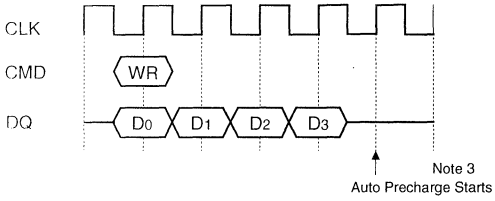


2) Normal Read (BL=4)

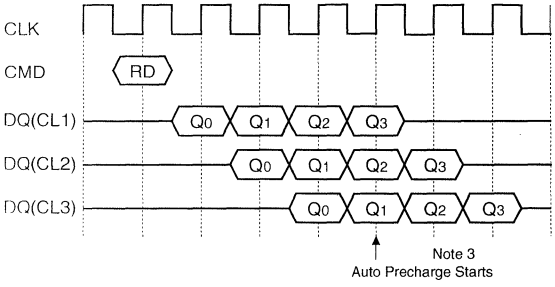


7. Auto Precharge

1) Normal Write (BL=4)



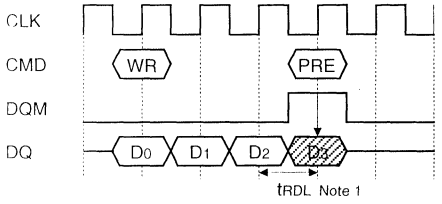
2) Normal Read (BL=4)



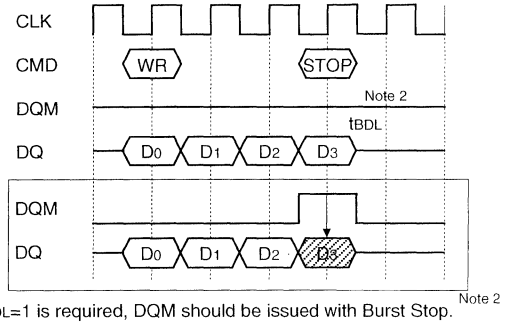
Note : 1. tRDL : Last Data in to Row Precharge Delay
2. Number of valid output data after Row Precharge : 0,1,2, for CAS Latency=1,2,3, respectively.
3. The row active command of the precharge bank can be issued after tRP from this point.
The new read/write command of another activated bank can be issued from this point.
At burst read/write with auto precharge, CAS interrupt of the same/another bank is illegal.

8. Burst Stop & Interrupted by Precharge

1) Normal Write (BL=4)

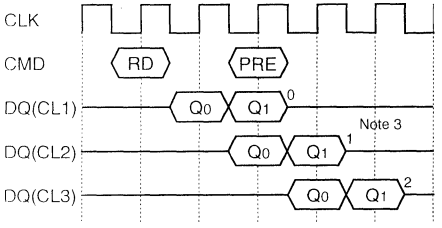


2) Write Burst Stop (BL=8)

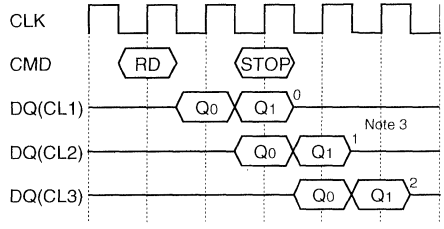


If t_{BDL}=1 is required, DQM should be issued with Burst Stop.

3) Read Interrupted by Precharge (BL=4)

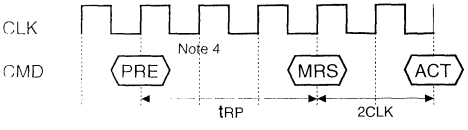


4) Read Burst Stop (BL=4)



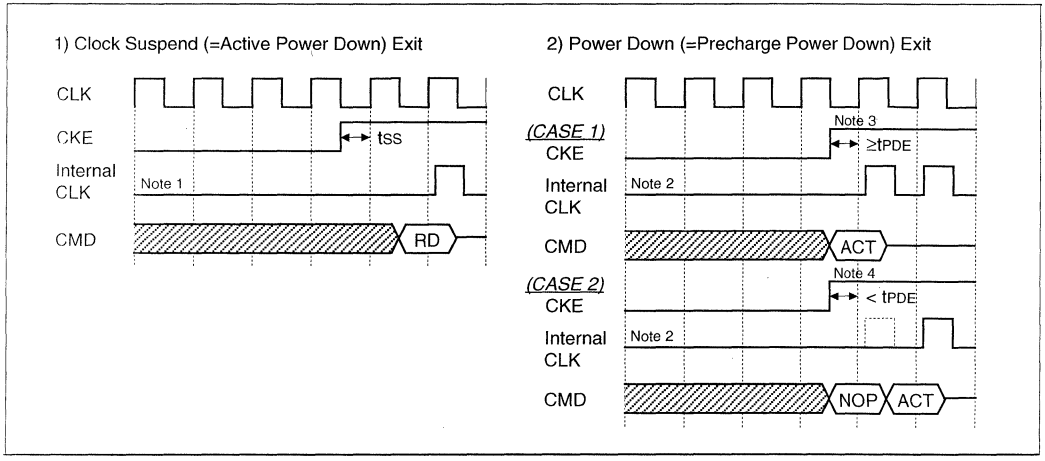
9. MRS

1) Mode Register Set

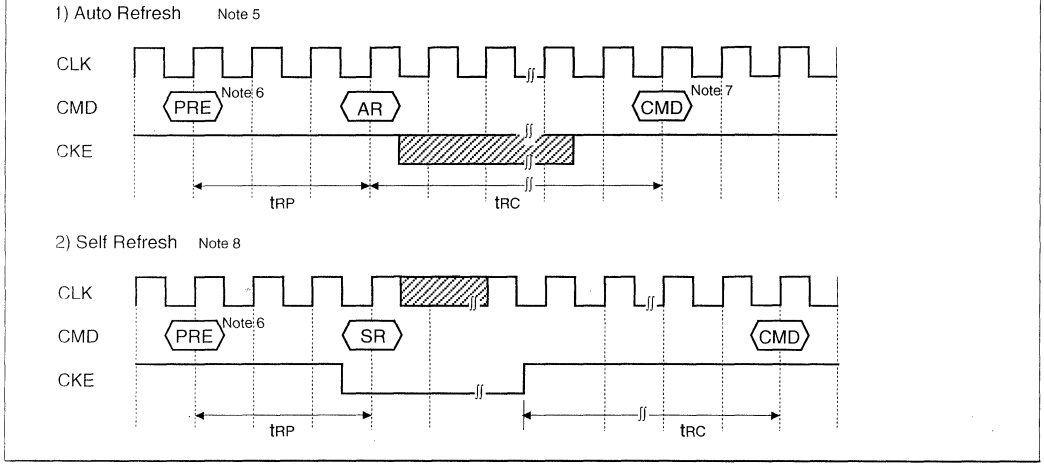


Note : 1. t_{RDL} : 1 CLK
2. t_{BDL} = 0 CLK ; Last Data in to Burst Stop Delay.
To inhibit write at the cycle of burst stop, DQM should be issued.
Read or write burst stop command is valid at every burst length.
3. Number of valid output data after Row precharge or burst stop : 0,1,2, for CAS Latency=1,2,3, Respectively.
4. PRE : Both Bank Precharge if necessary.
MRS can be issued only at both bank precharge state.

10. CLOCK Suspend Exit & Power Down Exit



11. Auto Refresh & Self Refresh



Note : 1. Active power down : one or both bank active state.
2. Precharge power down : both bank precharge state.
3. tPDE : Asynchronous AC parameter. Time for Power Down Exit Setup Time.
Only valid at precharge power down exit.
4. tSS < tPDE, NOP should be issued. And new command can be issued after 1 Clock.
5. The auto refresh is the same as CBR refresh of conventional DRAM.
No precharge commands are required after auto refresh command.
During tRC from auto refresh command, any other command cannot be accepted.
6. Before executing auto/self refresh command, both banks must be idle state.
7. MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
8. During self refresh mode, refresh interval and refresh operation are performed internally.
After self refresh entry, self refresh mode is kept while CKE is LOW.
During self refresh mode, all inputs execept CKE will be don't cared, and all outputs will be in a Hi-Z state.
For the time interval of tRC from self refresh exit command any other command cannot be accepted.
Before/After self refresh mode, burst auto refresh cycle (X4 & X8 : 4K , X16 : 2K cycle) is recommended.

12. About Burst Type Control

Basic MODE	Sequential Counting	At MRS, A_3 = "0". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=1,2,4,8 and full page.
	Interleave Counting	At MRS, A_3 = "1". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=4,8, At BL=1,2 Interleave Counting = Sequential Counting
Pseudo- MODE	*Pseudo-* Decrement Sequential Counting	At MRS, A_3 = "1". (Set to Interleave Counting Mode) Starting Address LSB 3 bits A_{0-2} should be "000" or "111". @BL=8. -- if LSB = "000" : Increment Counting. -- If LSB = "111" : Decrement Counting. For Example, (Assume Addresses except LSB 3 bits are all 0, BL=8) -- @ write, LSB = "000", Accessed Column in order 0-1-2-3-4-5-6-7 -- @ read, LSB = "111", Accessed Column in order 7-6-5-4-3-2-1-0 At BL=4, same applications are possible. As above example, at Interleave Counting mode, by confining starting address to some values, *Pseudo-* Decrement Counting Mode can be realized. See the BURST SEQUENCE TABLE carefully.
Random MODE	Random column Access t_{CCD} = 1CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of conventional DRAM.

13. About Burst Length Control

Basic MODE	1	At MRS, $A_{2,1,0}$ = "000" At auto precharge, t_{RAS} should not be violated.
	2	At MRS, $A_{2,1,0}$ = "001" At auto precharge, t_{RAS} should not be violated.
	4	At MRS, $A_{2,1,0}$ = "010"
	8	At MRS, $A_{2,1,0}$ = "011"
	Full Page	At MRS, $A_{2,1,0}$ = "111" At the end of the burst length, burst will be stop automatically.
Special MODE	BRSW	At MRS, A_9 = "1" Read Burst = 1,2,4,8, full page/Write Burst = 1 At auto precharge of write, t_{RAS} should not be violated.
Random MODE	Burst Stop	t_{BDL}=0, Valid DQ after burst stop is 0,1,2 for CL 1,2,3 respectively Using burst stop command, any burst length control is possible.
Interrupt MODE	$\overline{RAS}$ Interrupt (Interrupted by Precharge)	Before the end of burst, Row precharge command of the same bank stops read/write burst with Row precharge. t_{RDL}=1 with DQM, Vaild DQ after burst stop is 0,1,2 for CL 1,2,3 respectively During read/write burst with auto precharge, $\overline{RAS}$ interrupt cannot be issued.
	$\overline{CAS}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst. During read/write burst with auto precharge, $\overline{CAS}$ interrupt cannot be issued.

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	NOTE
IDLE	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA,A10	ILLEGAL	2
	L	L	H	H	BA	RA	Row (& Bank) Active ; Latch RA	
	L	L	H	L	BA	A10	NOP	4
	L	L	L	H	X	X	Auto Refresh or Self Refresh	5
	L	L	L	L	OP code	OP code	Mode Register Access	5
Row Active	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	BA	CA, A10	Begin Read ; latch CA ; determine AP	
	L	H	L	L	BA	CA, A10	Begin Write ; latch CA ; determine AP	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10	Precharge	
	L	L	L	X	X	X	ILLEGAL	
Read	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A10	Term burst , New read, Determine AP	
	L	H	L	L	BA	CA, A10	Term burst , New write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10	Term burst, Precharge timing for Reads	
	L	L	L	X	X	X	ILLEGAL	
Write	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A10	Term burst, New read, Determine AP	3
	L	H	L	L	BA	CA, A10	Term burst, New write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10	Term burst, Precharge timing for Writes	3
	L	L	L	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A10	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA,A10	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Pre-charging	H	X	X	X	X	X	NOP --> Idle after t_{RP}	
	L	H	H	H	X	X	NOP --> Idle after t_{RP}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10	NOP --> Idle after t_{RP}	4

FUNCTION TRUTH TABLE (TABLE 1, Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	NOTE
Row Activating	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	H	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Refreshing	H	X	X	X	X	X	NOP --> Idle after t_{RC}	
	L	H	H	X	X	X	NOP --> Idle after t_{RC}	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	NOP --> Idle after 2 clocks	
	L	H	H	H	X	X	NOP --> Idle after 2 clocks	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

ABBREVIATIONS :

RA = Row Address BA = Bank Address
NOP = No Operation Command CA = Column Address AP = Auto Precharge

Notes : 1. All entries assume that CKE was active (High) during the preceding clock cycle and the current clock cycle.
2. Illegal to bank in specified state ; Function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA (and A_{10}).
5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE for CKE (TABLE 2)

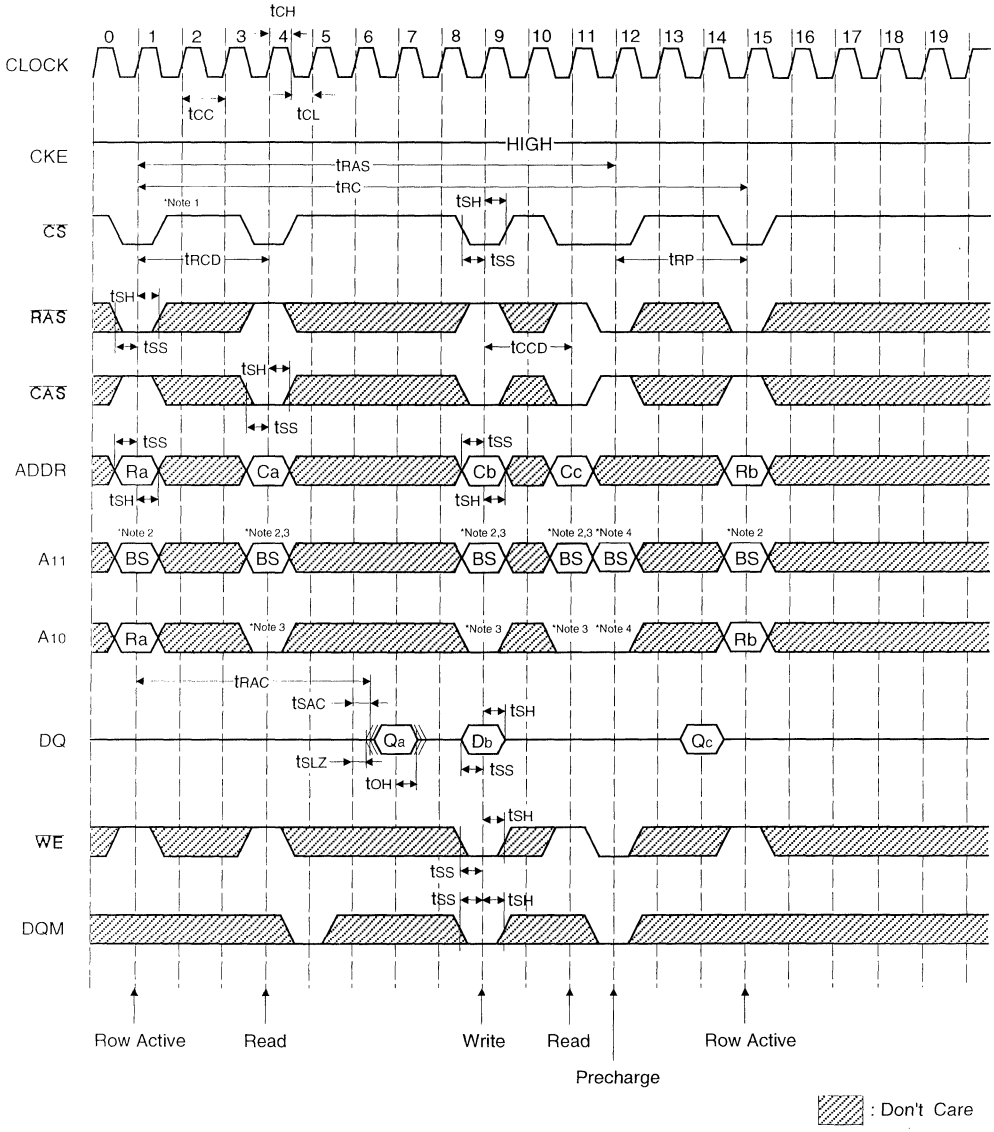
Current State (n)	CKE (n-1)	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	ACTION	NOTE
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh --> Idle after tRC (ABI)	6
	L	H	L	H	H	H	X	Exit Self Refresh --> Idle after tRC (ABI)	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	
Both Bank Precharge Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Power Down --> ABI	7
	L	H	L	H	H	H	X	Exit Power Down --> ABI	7
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL (If tPDE is satisfied, refer to table 1)	
	L	L	X	X	X	X	X	NOP (Maintain Low Power Mode)	
All Banks Idle	H	H	X	X	X	X	X	Refer to Table 1	
	H	L	H	X	X	X	X	Enter Power Down	8
	H	L	L	H	H	H	X	Enter Power Down	8
	H	L	L	H	H	L	X	ILLEGAL	
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row (& Bank) Active	
	H	L	L	L	H	H	X	NOP	
	H	L	L	L	L	L	X	Enter Self Refresh	8
	H	L	L	L	L	L	OP code	Mode Register Access	
	L	L	X	X	X	X	X	NOP	
Any State other than Listed Above	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain clock Suspend	

Abbreviations : ABI = All Banks Idle, RA = Row Address

Notes : 6. CKE low to high transition is asynchronous.
A minimum pulse width time tSRX must be satisfied.
7. CKE low to high transition is asynchronous as if restarts internal clock.
A minimum setup time tPDE must be satisfied before any command other than exit.
8. Power-down and self refresh can be entered only from the all banks idle state.
9. Must be a legal command.

TIMING DIAGRAMS 5

Single Bit Read-Write-Read Cycle(Same Page) @CAS Latency=3, Burst Length=1



*Note : 1. All input can be don't care when $\overline{CS}$ is high at the CLK high going edge.
2. Bank active & read/write are controlled by A11.

A11	Active & Read/Write
0	Bank A
1	Bank B

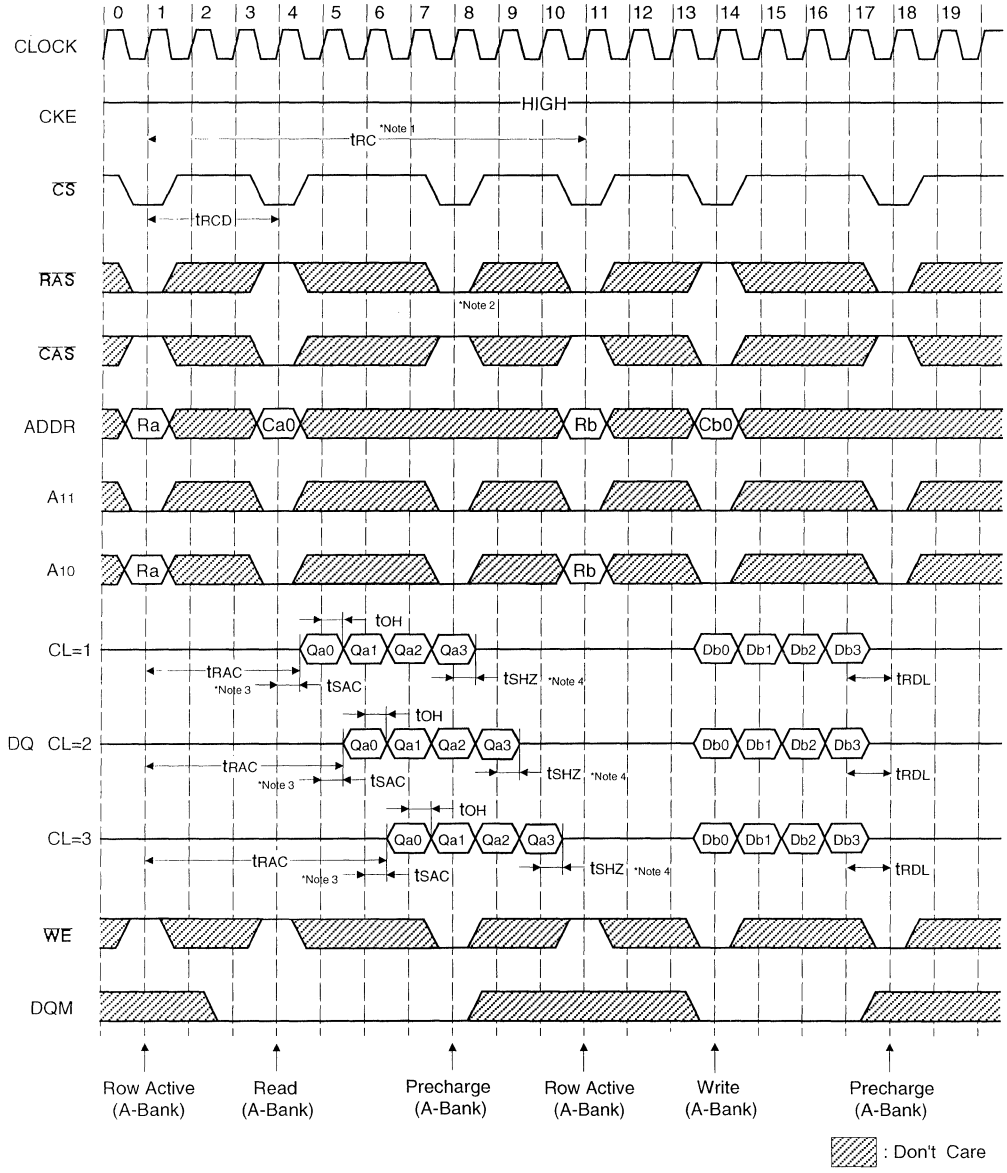
3. Enable and disable auto precharge function are controlled by A10 in read/write command.

A10	A11	Operation
0	0	Disable auto precharge, leave bank A active at end of burst
	1	Disable auto precharge, leave bank B active at end of burst
1	0	Enable auto precharge, precharge bank A at end of burst
	1	Enable auto precharge, precharge bank B at end of burst

4. A10 and A11 control bank precharge when precharge command is asserted.

A10	A11	Precharge
0	0	Bank A
0	1	Bank B
1	X	Both Bank

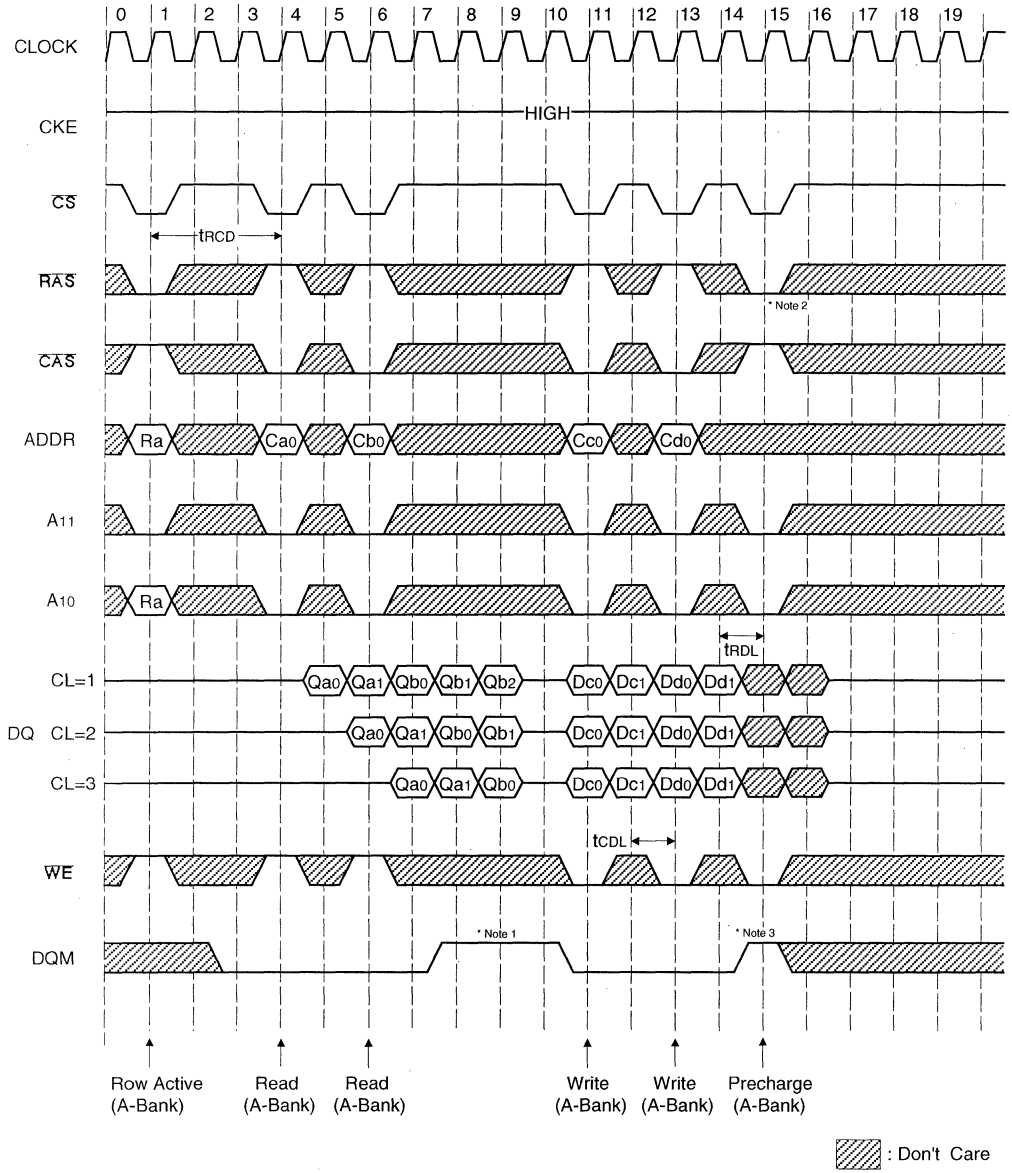
Read & Write Cycle at Same Bank @Burst Length=4



***Note :** 1. Minimum row cycle times is required to complete internal DRAM operation.

2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data. is available after Row precharge. Last valid output will be hi-Z(t_{SHZ}) after the clock.
3. Access time from Row active command. t_{CC} *(t_{RCD} + CAS latency - 1) + t_{SAC}.
4. Output will be Hi-Z after the end of burst. (1, 2, 4, 8 & full page bit burst)

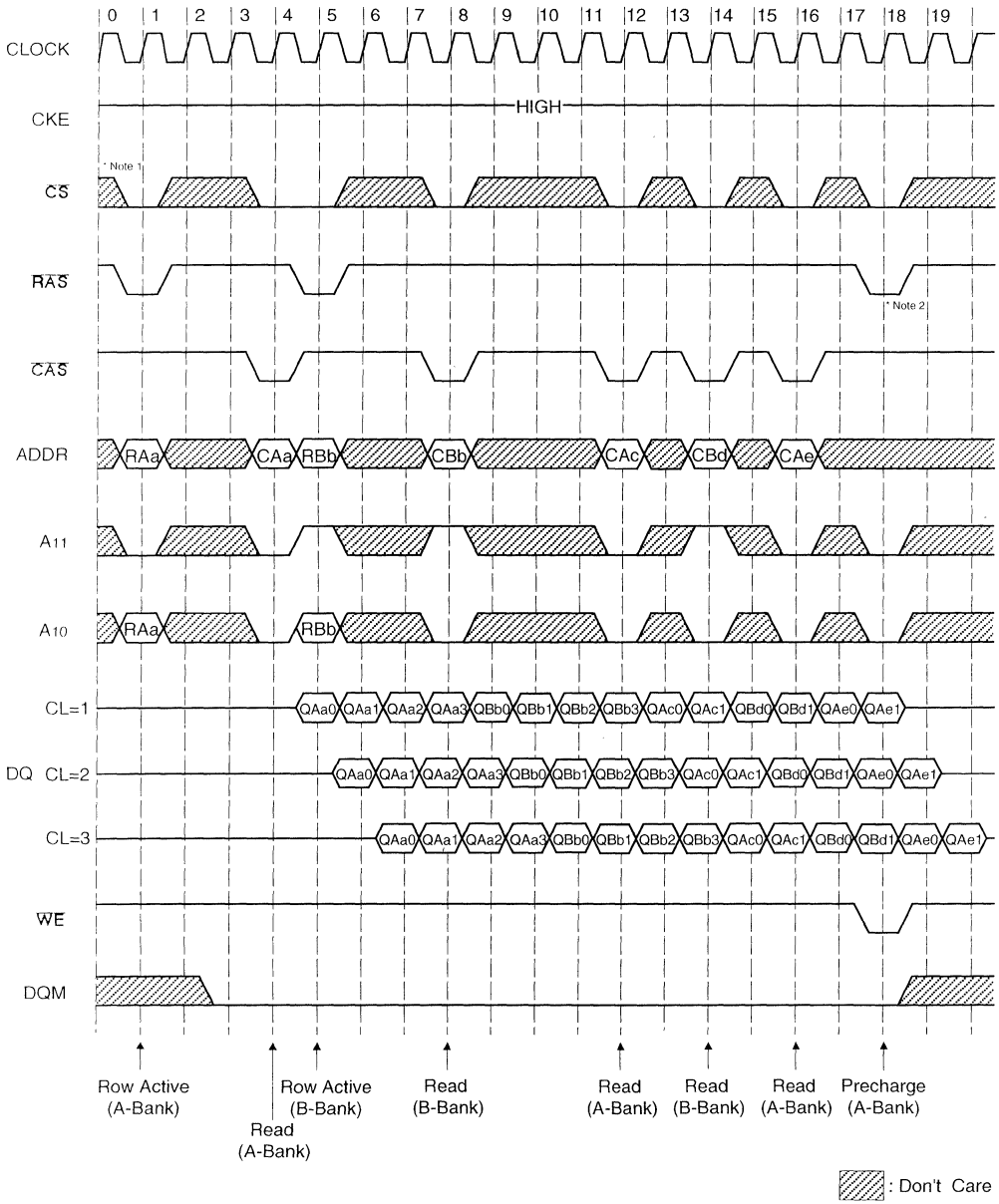
Page Read & Write Cycle at Same Bank @Burst Length=4



***Note :** 1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.

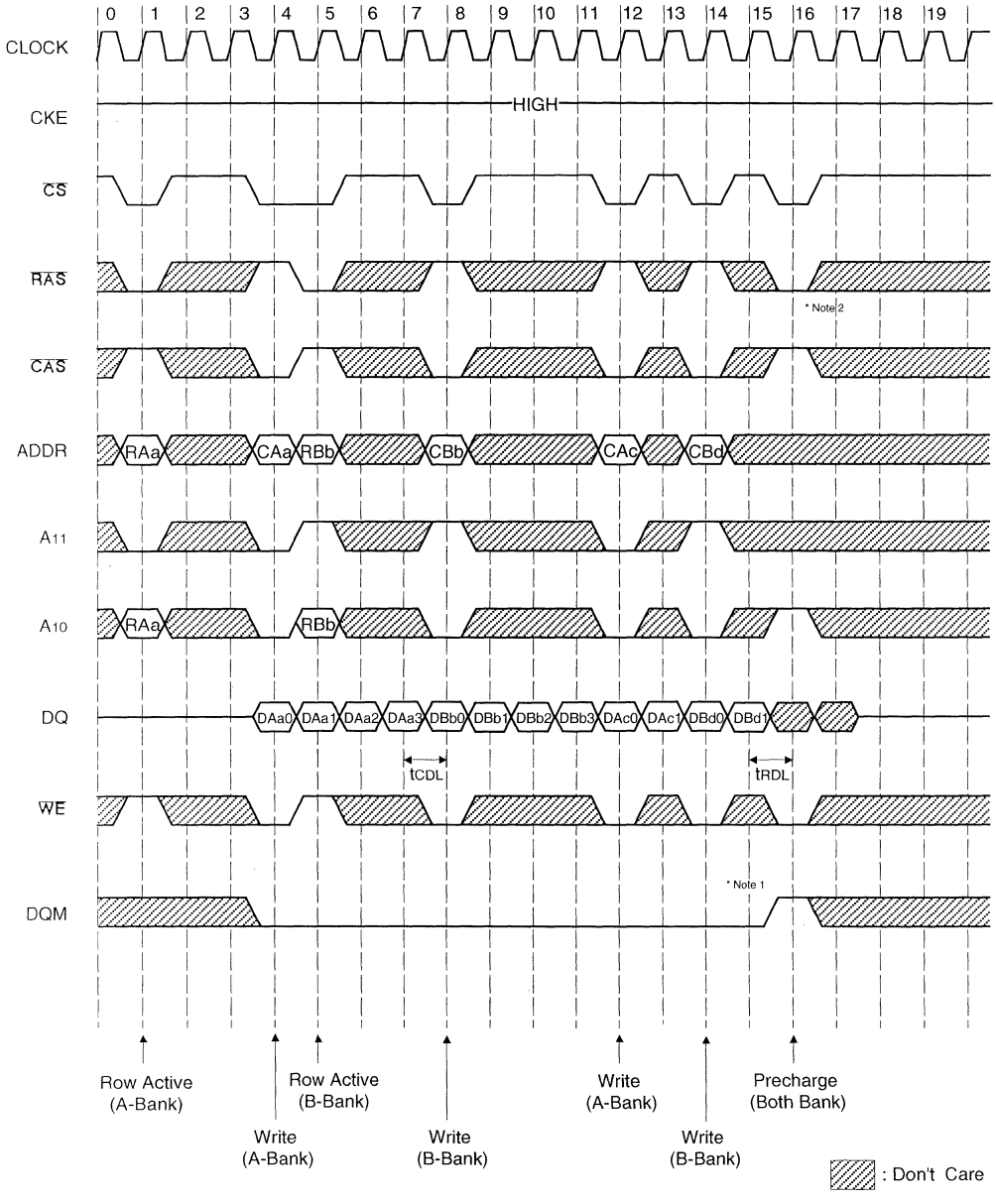
2. Row precharge will interrupt writing. Last data input, tRDL before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

Page Read Cycle at Different Bank @Burst Length=4



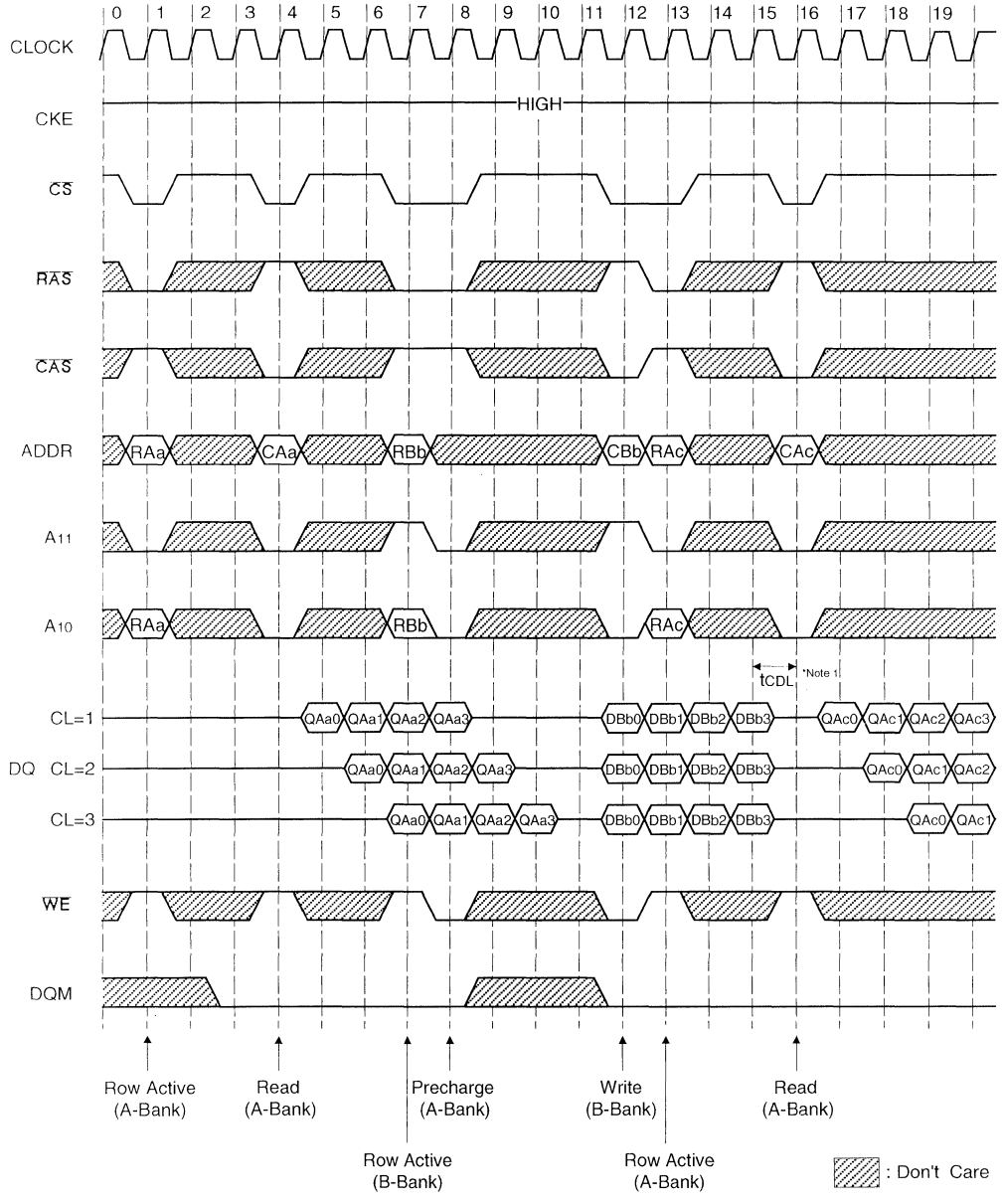
*Note : 1. $\overline{CS}$ can be don't care when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the clock high going edge.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

Page Write Cycle at Different Bank @Burst Length=4



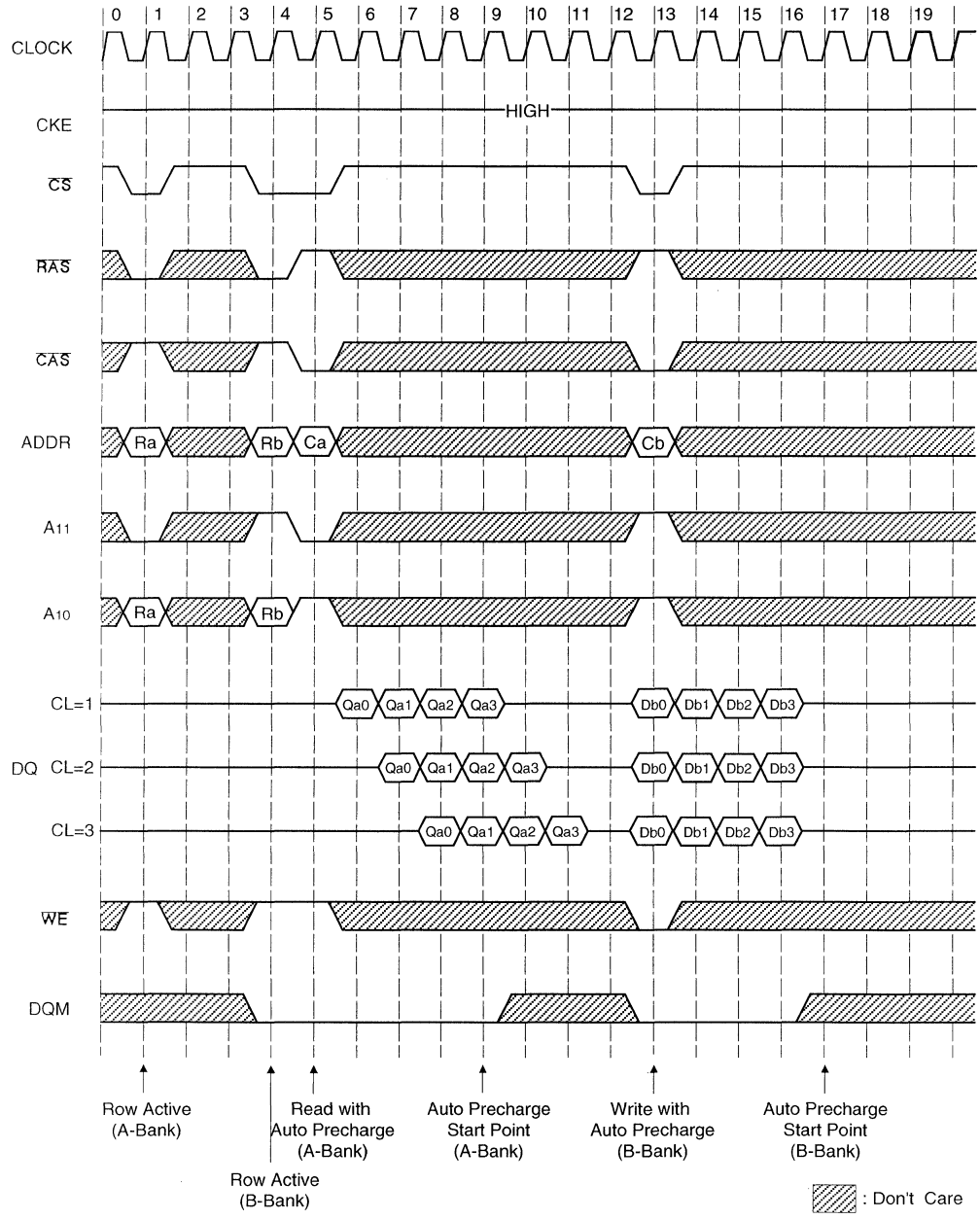
*** Note :** 1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

Read & Write Cycle at Different Bank @Burst Length=4



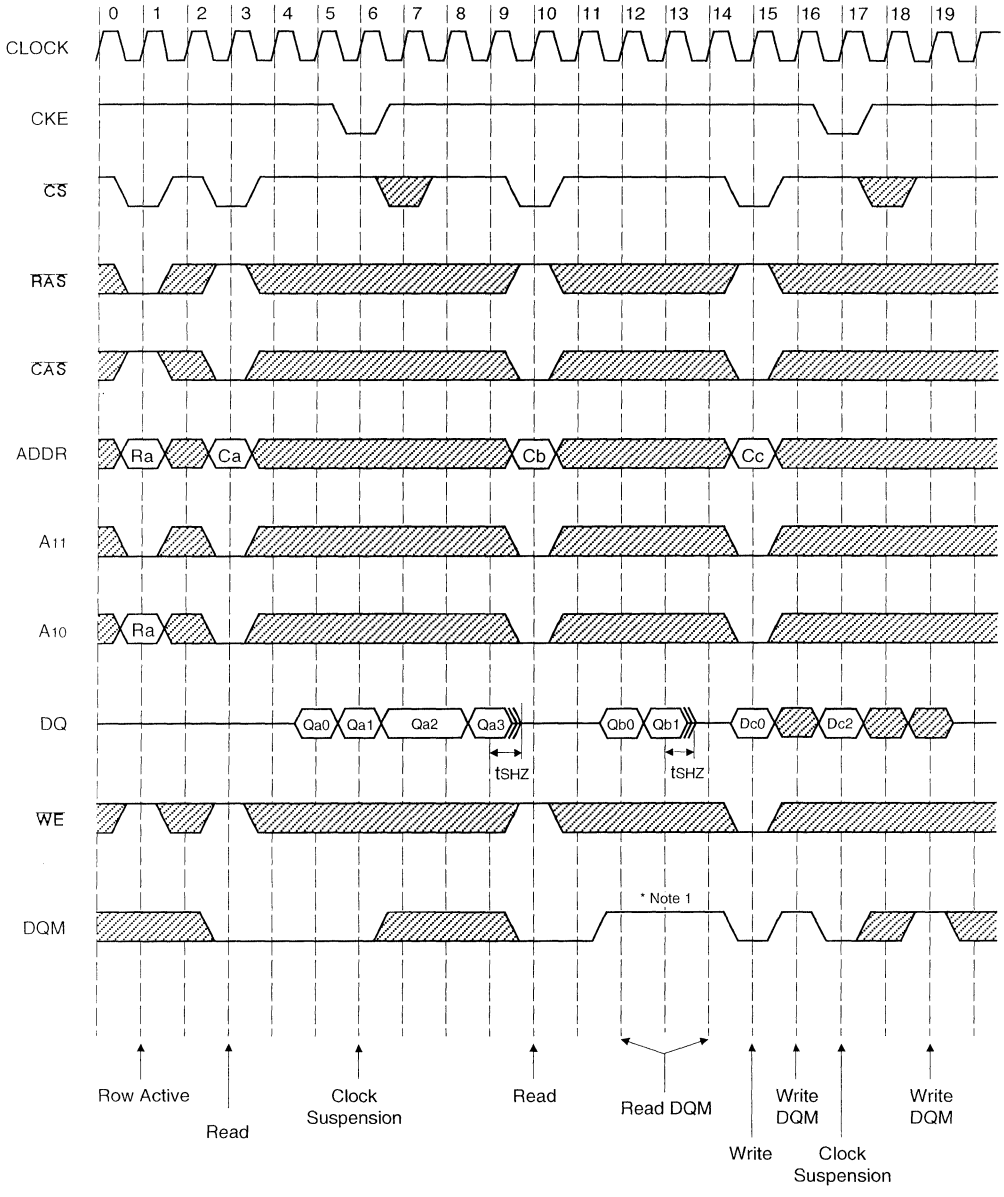
***Note :** 1. tCDL should be met to complete write.

Read & Write Cycle with Auto Precharge @Burst Length=4



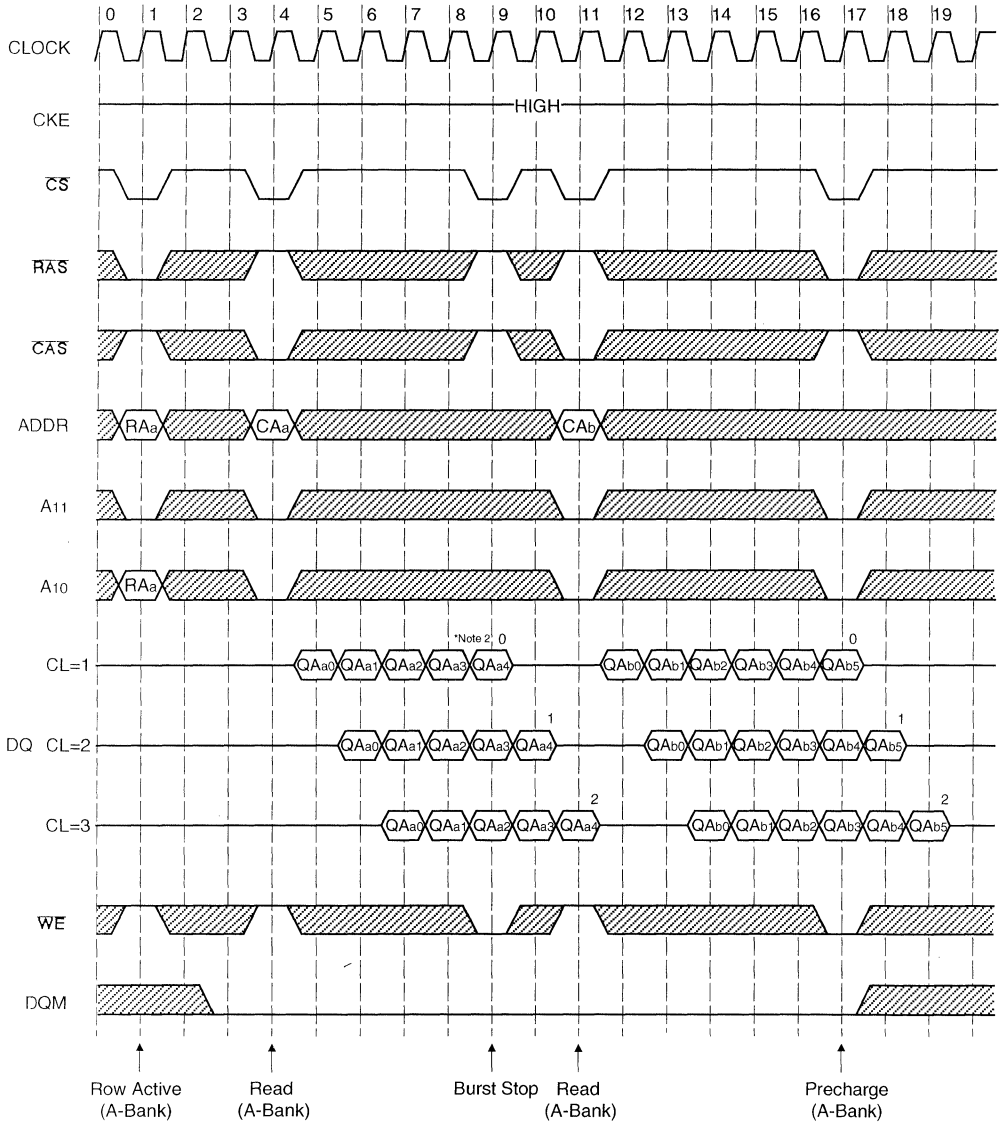
*Note : 1. tRCD should be controlled to meet minimum tRAS before internal precharge start
(In the case of Burst Length=1 & 2 and BRSW mode)

Clock suspension & DQM operation cycle @CAS Latency=2, Burst Length=4



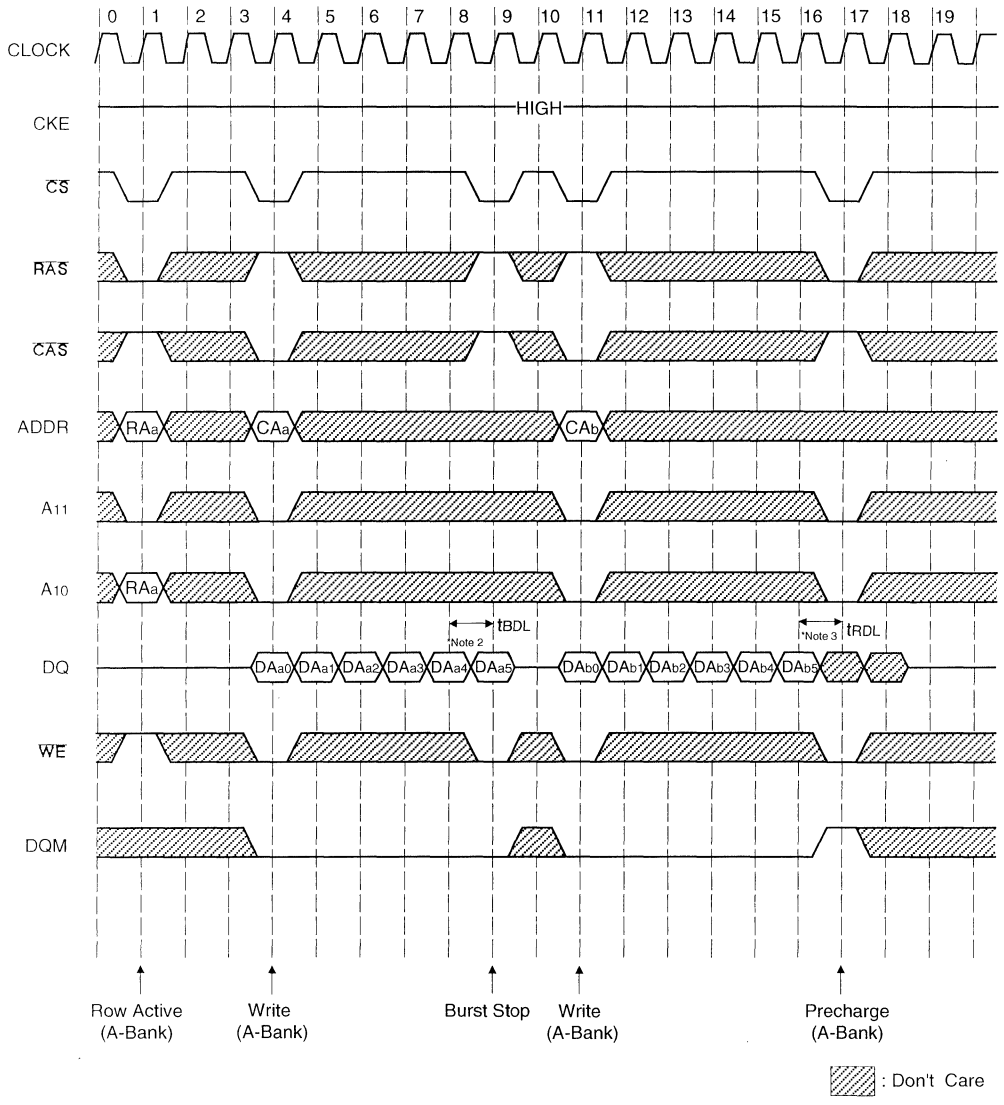
*Note : 1. DQM needed to prevent bus contention.

Read Interrupted by Precharge Command & Read Burst Stop Cycle @ Burst length = Full page



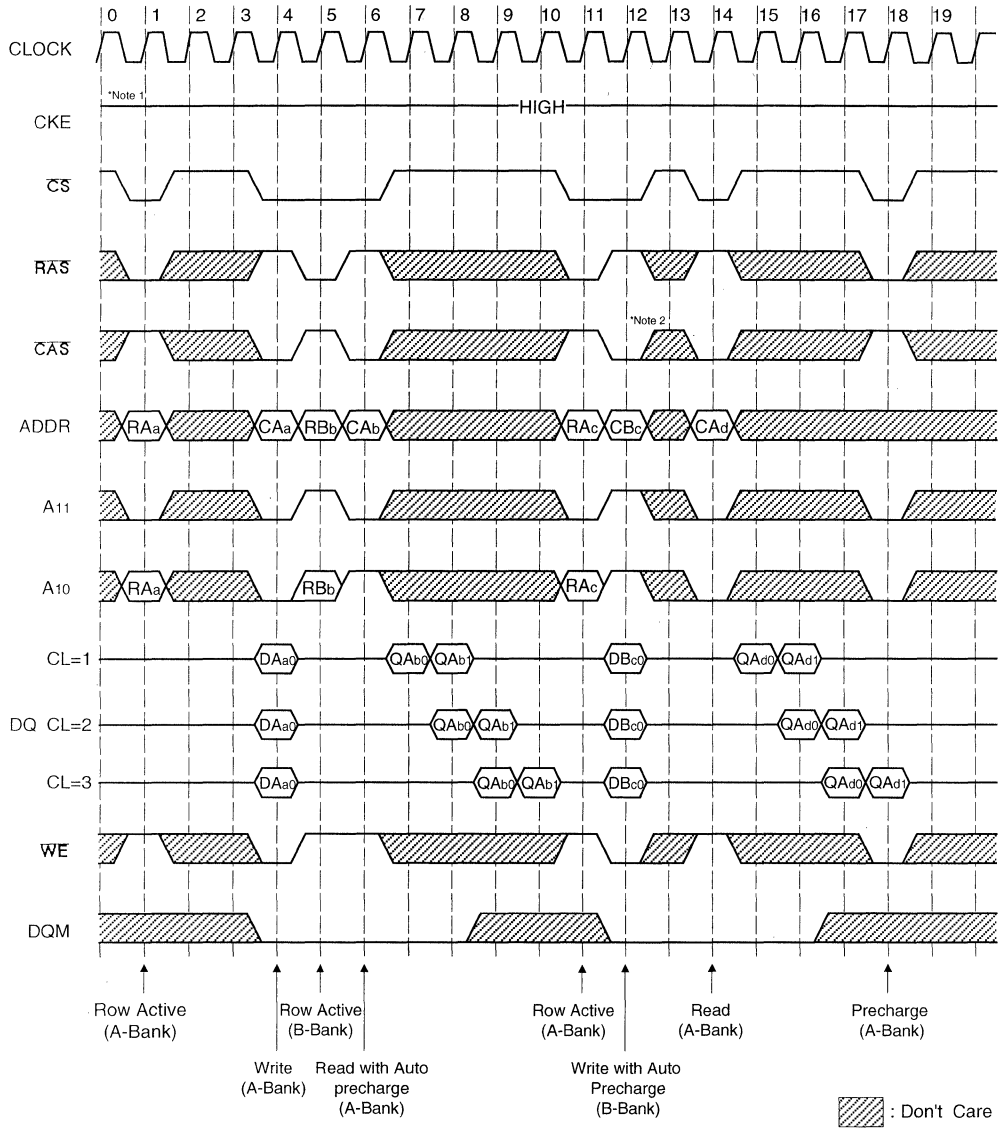
*Note :
1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. About the valid DQ's after burst stop, it is same as the case of $\overline{RAS}$ interrupt.
   Both cases are illustrated above timing diagram. See the label 0, 1, 2 on them.
   But at burst write, Burst stop and $\overline{RAS}$ interrupt should be compared carefully.
   Refer the timing diagram of "Full page write burst stop cycle".
3. Burst stop is valid at every burst length.

Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Burst length = Full page



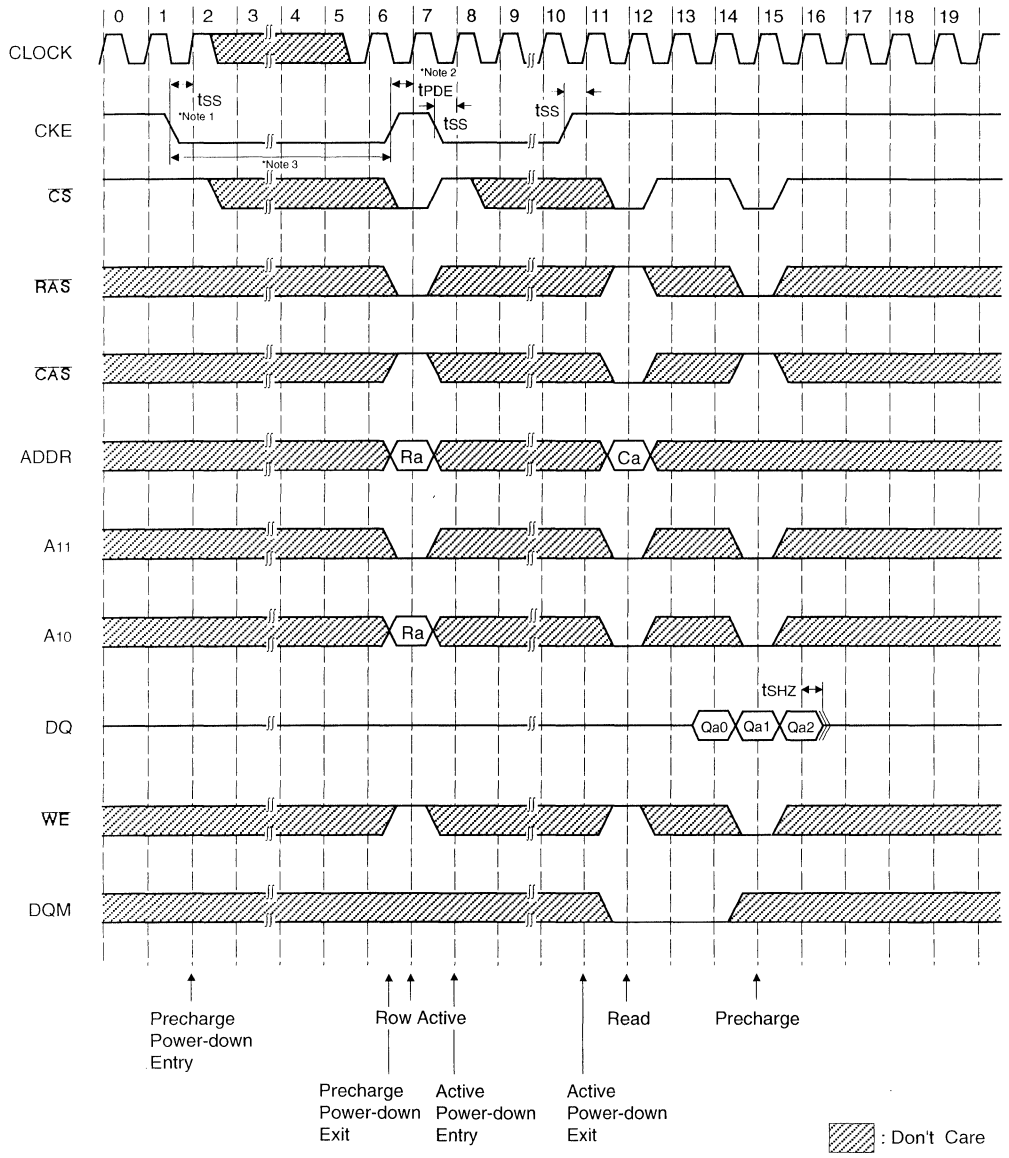
*Note :
1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. Data-in at the cycle of burst stop command is written into the corresponding memory cell (t_{BDL}=0). Compare this with the case of RAS interrupt, refer note 3.
3. Data-in at the cycle of interrupted by precharge cannot be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.
   DQM at write interrupted by precharge command is needed to prevent invalid write.
   DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
4. Burst stop is valid at every burst length.

Burst Read Single bit Write Cycle @Burst Length=2



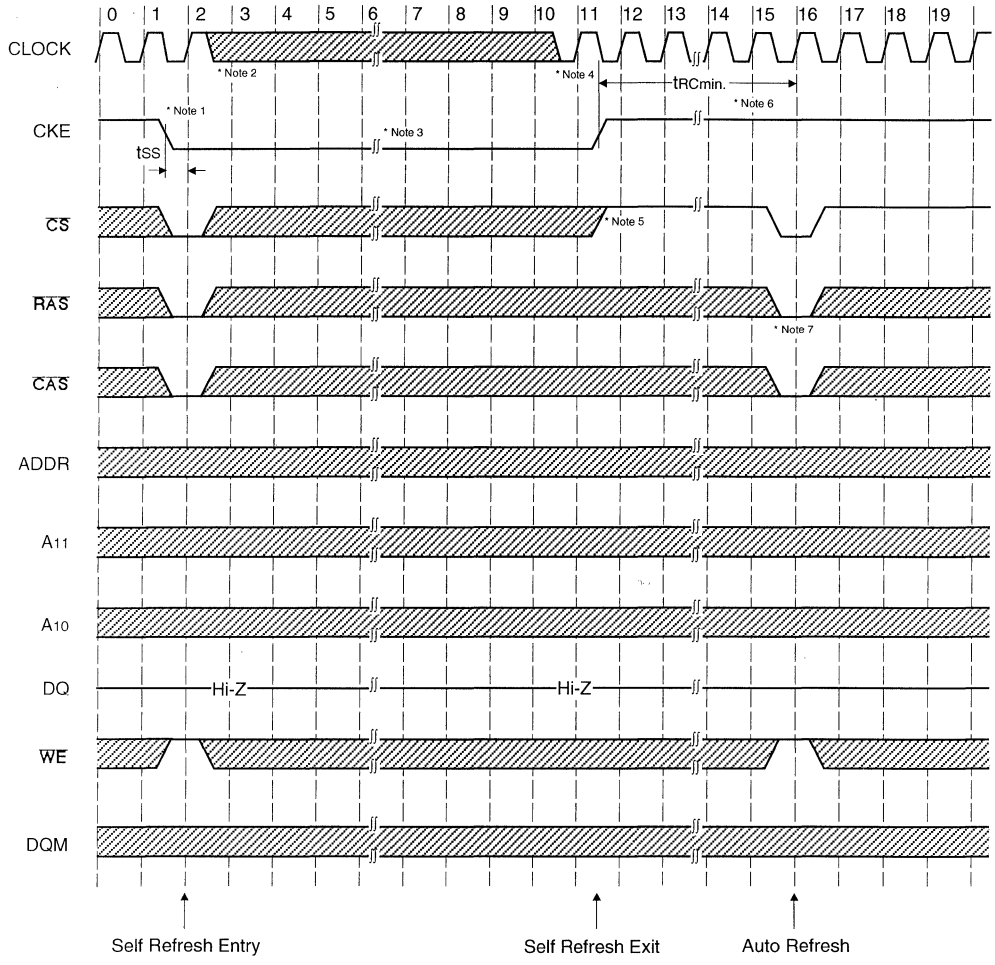
*Note : 1. BRSW mode is enabled by setting A_9 "High" at MRS (Mode Register Set).
At the BRSW mode, the burst length at write is fixed to "1" regardless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.
Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command, the next cycle starts the precharge.

Active/Precharge Power Down Mode @CAS Latency=2, Burst Length=4



*Note : 1. All banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least t_{PDE} prior to Row active command.
cf) If CKE is set high 1 clock prior to Active command, NOP command should be asserted at the previous clock of active command.
3. Can not violate minimum refresh specification. (x4,x8:64ms, x16:32ms)

Self Refresh Entry & Exit Cycle



: Don't Care

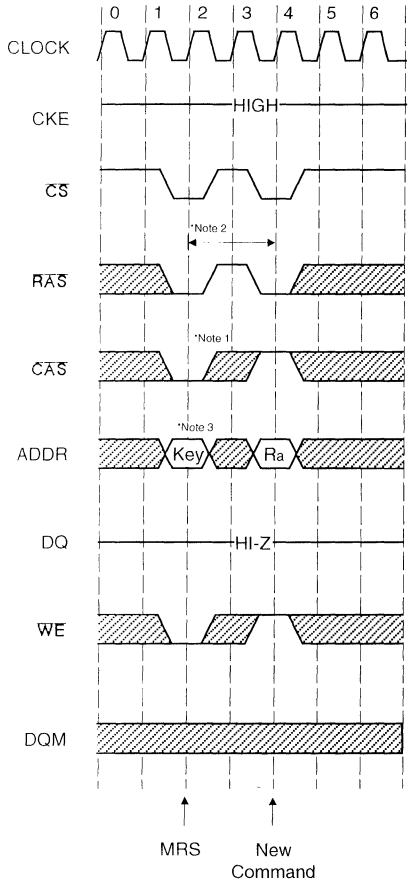
***Note : TO ENTER SELF REFRESH MODE**

1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays " Low ".
   cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

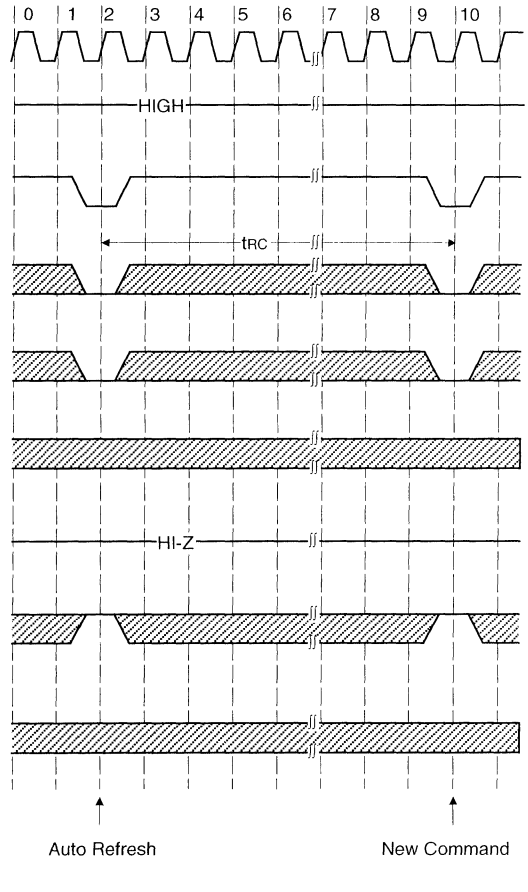
TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.
5. $\overline{CS}$ starts from high.
6. Minimum t_{RC} is required after CKE going high to complete self refresh exit.
7. 4K(x4,x8:4K, x16:2K) cycle of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

Mode Register Set Cycle



Auto Refresh Cycle



: Don't Care

* Both bank precharge should be completed before mode register set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE

***Note :** 1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ & $\overline{WE}$ activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new $\overline{RAS}$ activation.
3. Please refer to mode register set table.

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