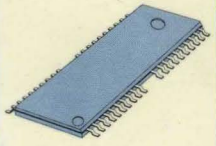
SAMSUNG

1110-4091

MOS Memory

1995



• DRAM

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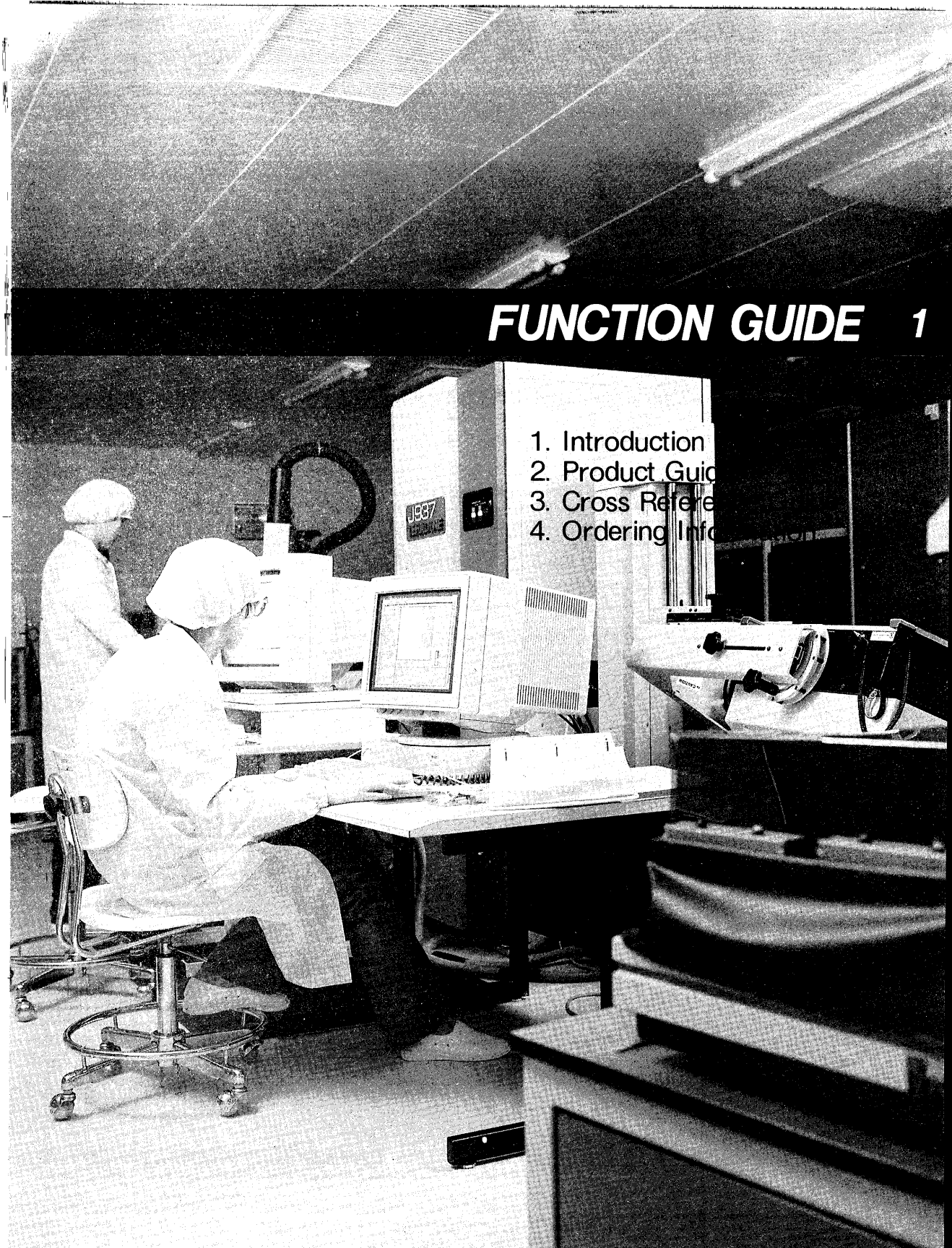
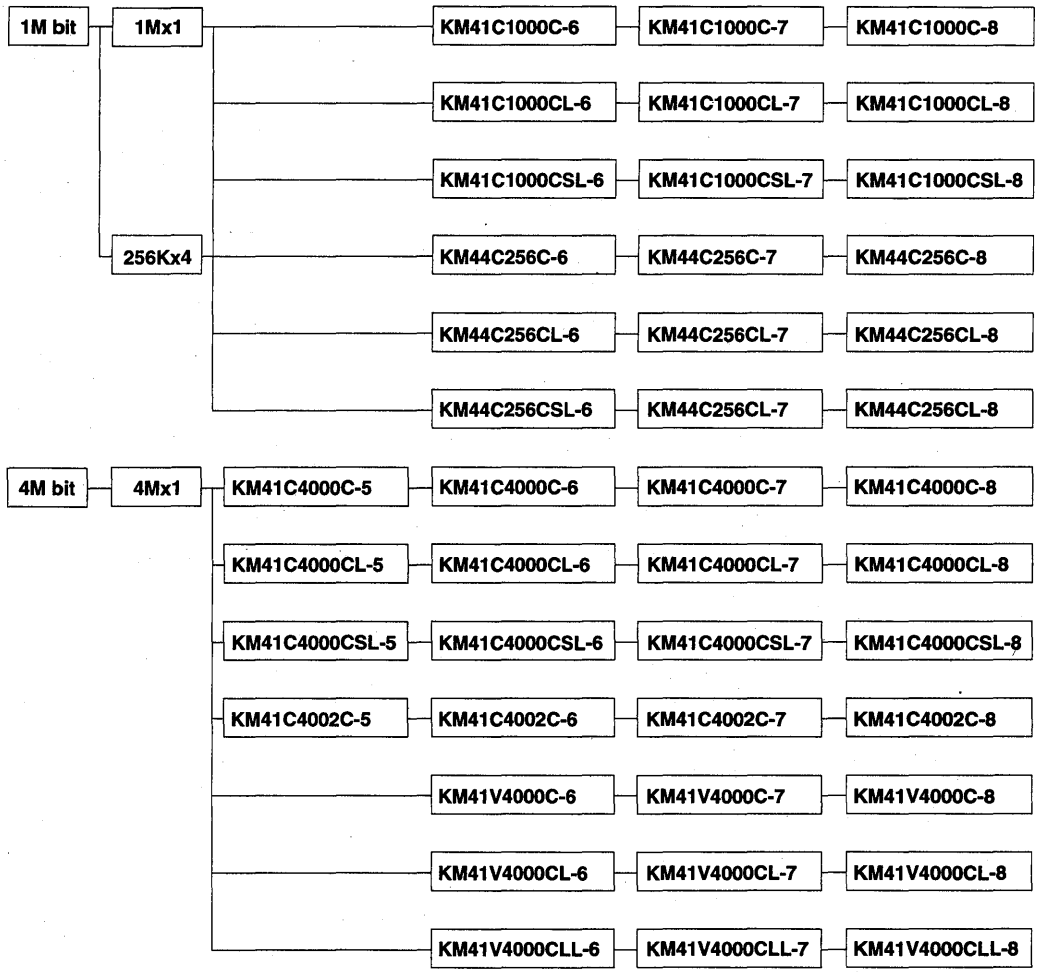
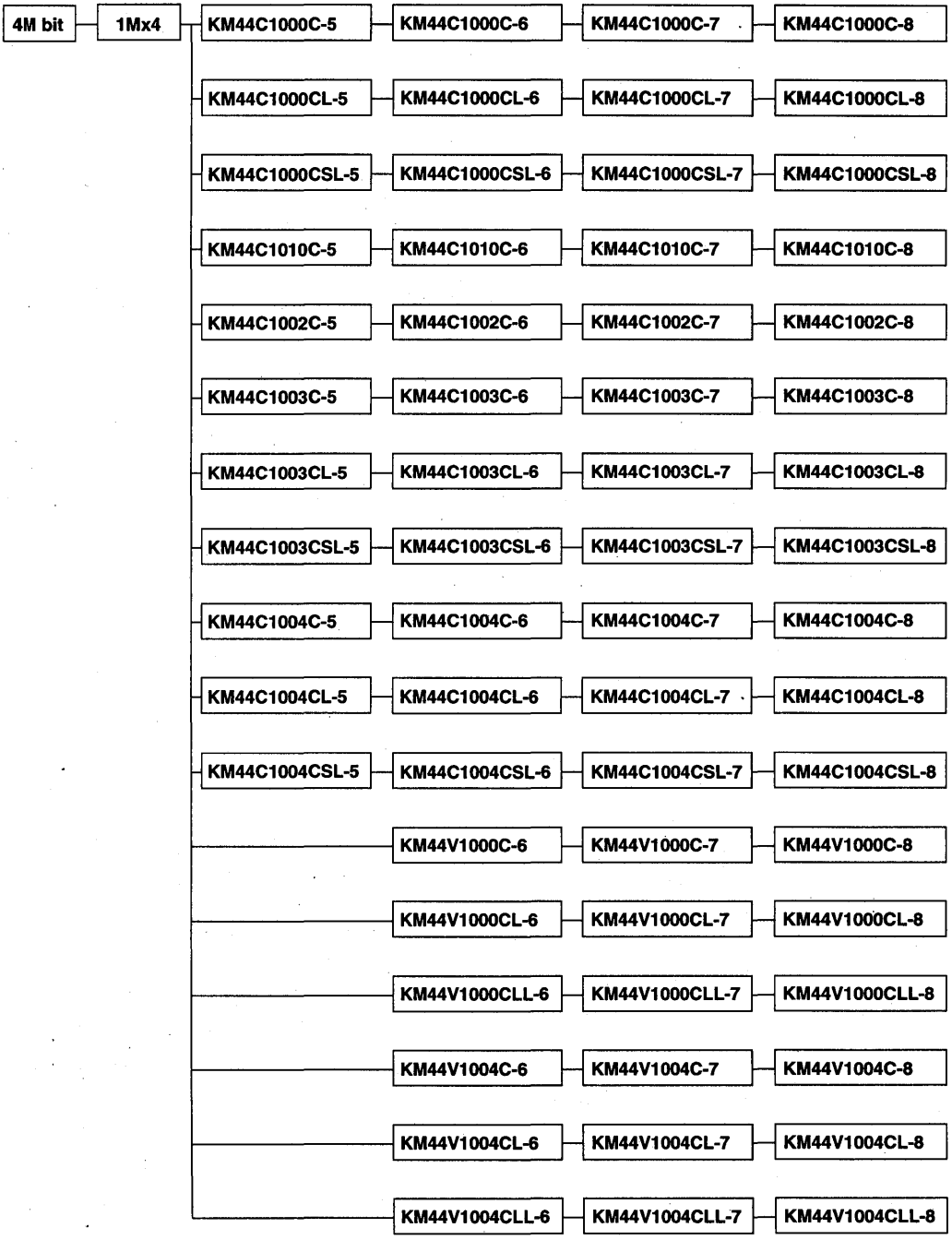


FUNCTION GUIDE 1

1. INTRODUCTION

1.1 Dynamic RAM

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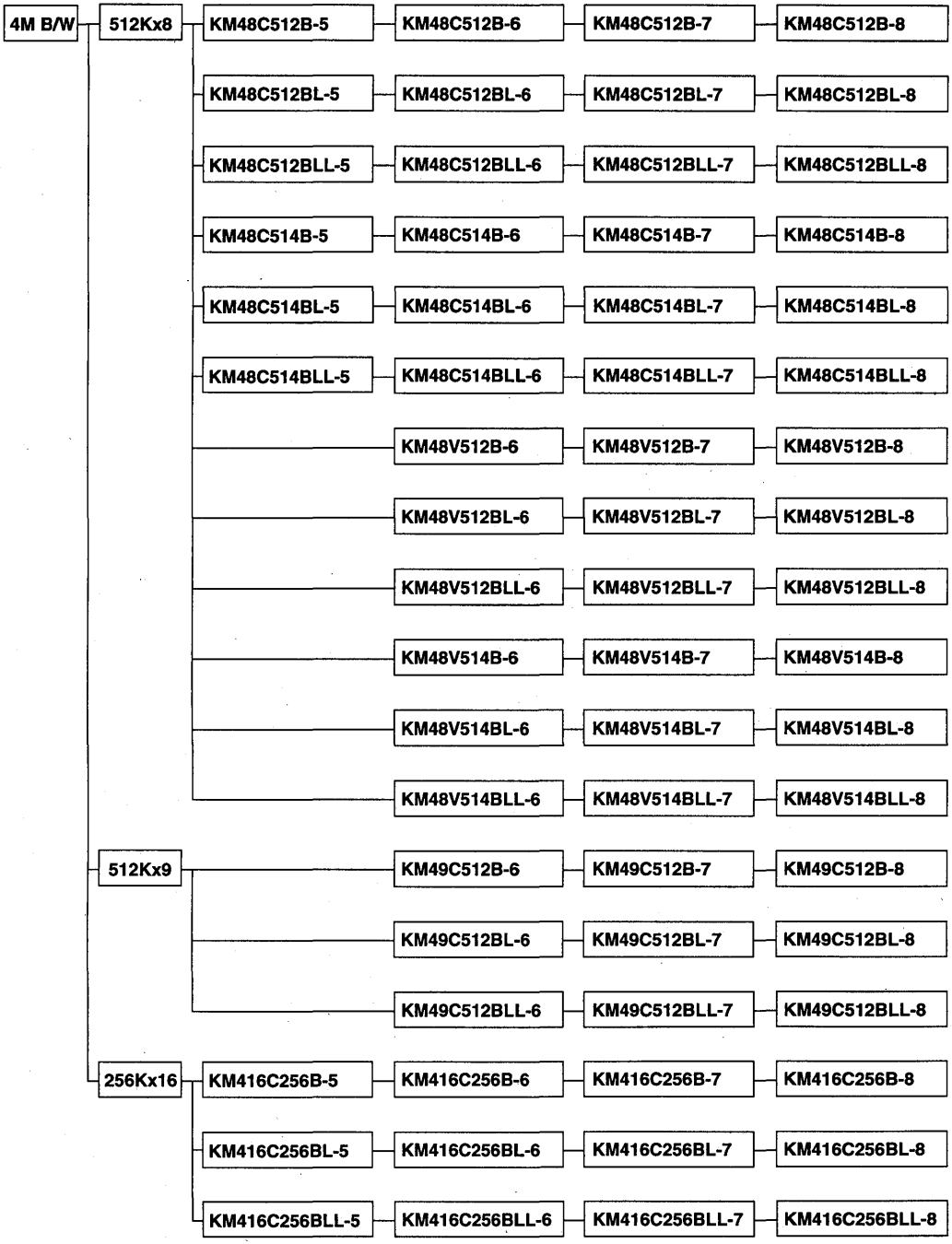
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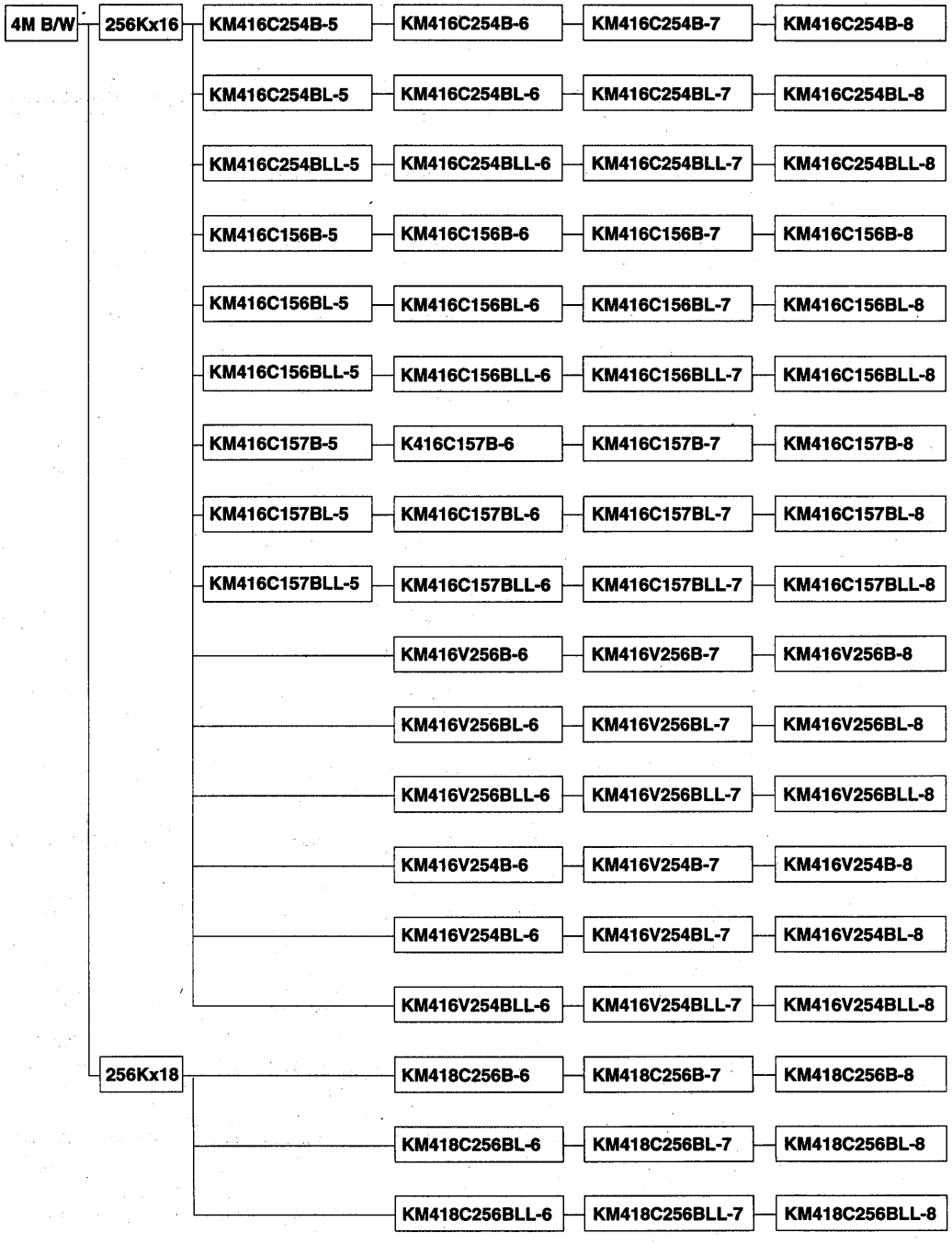
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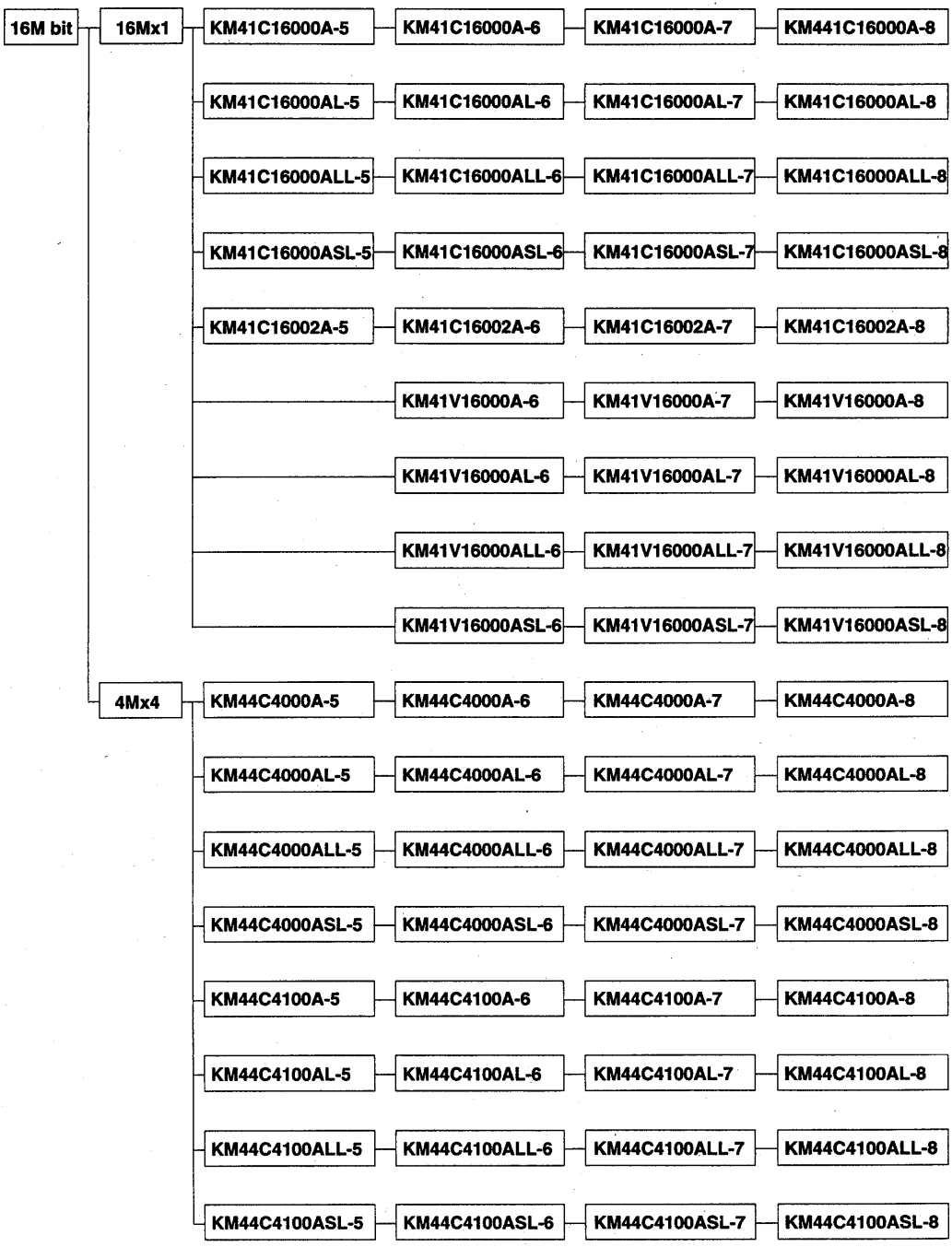
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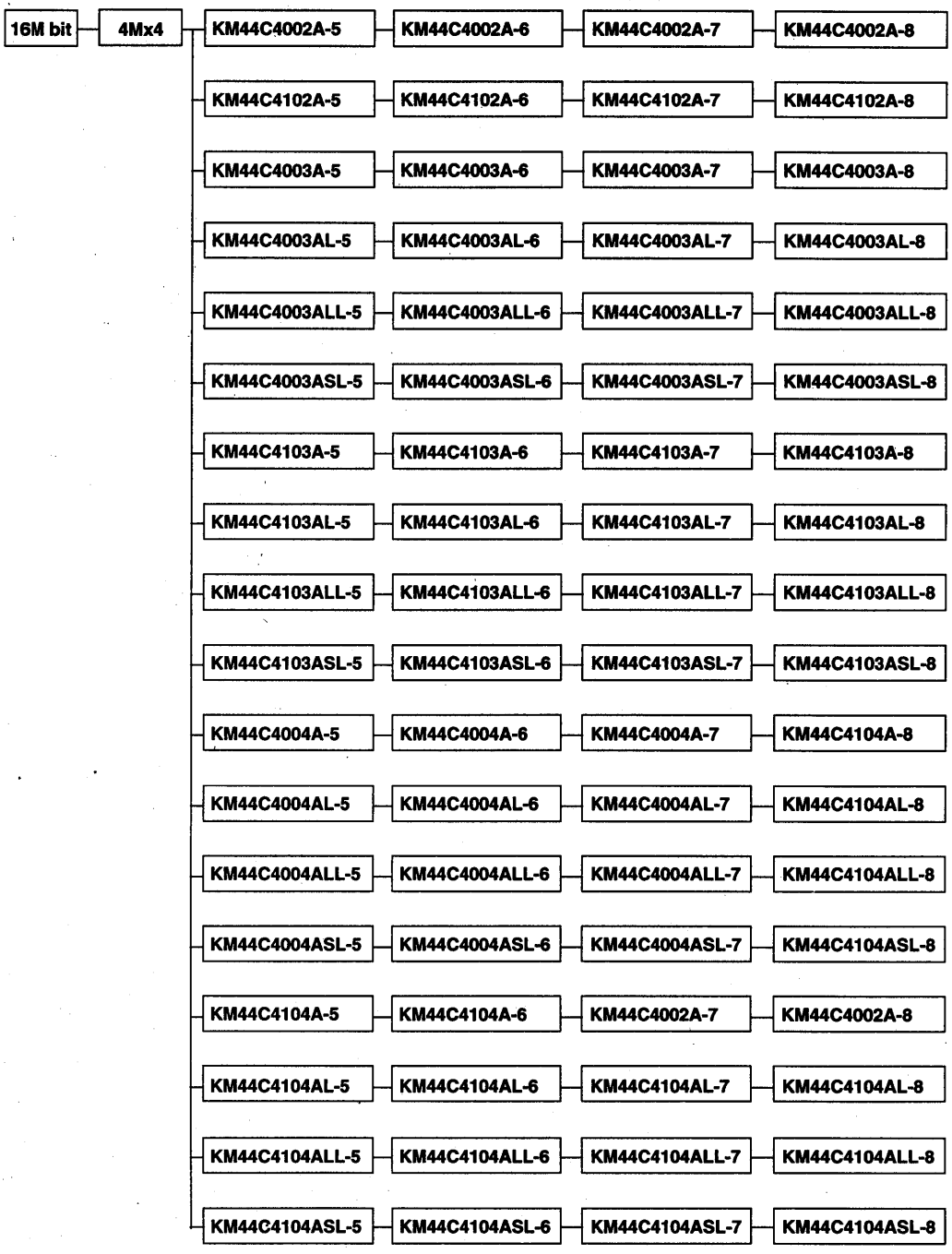
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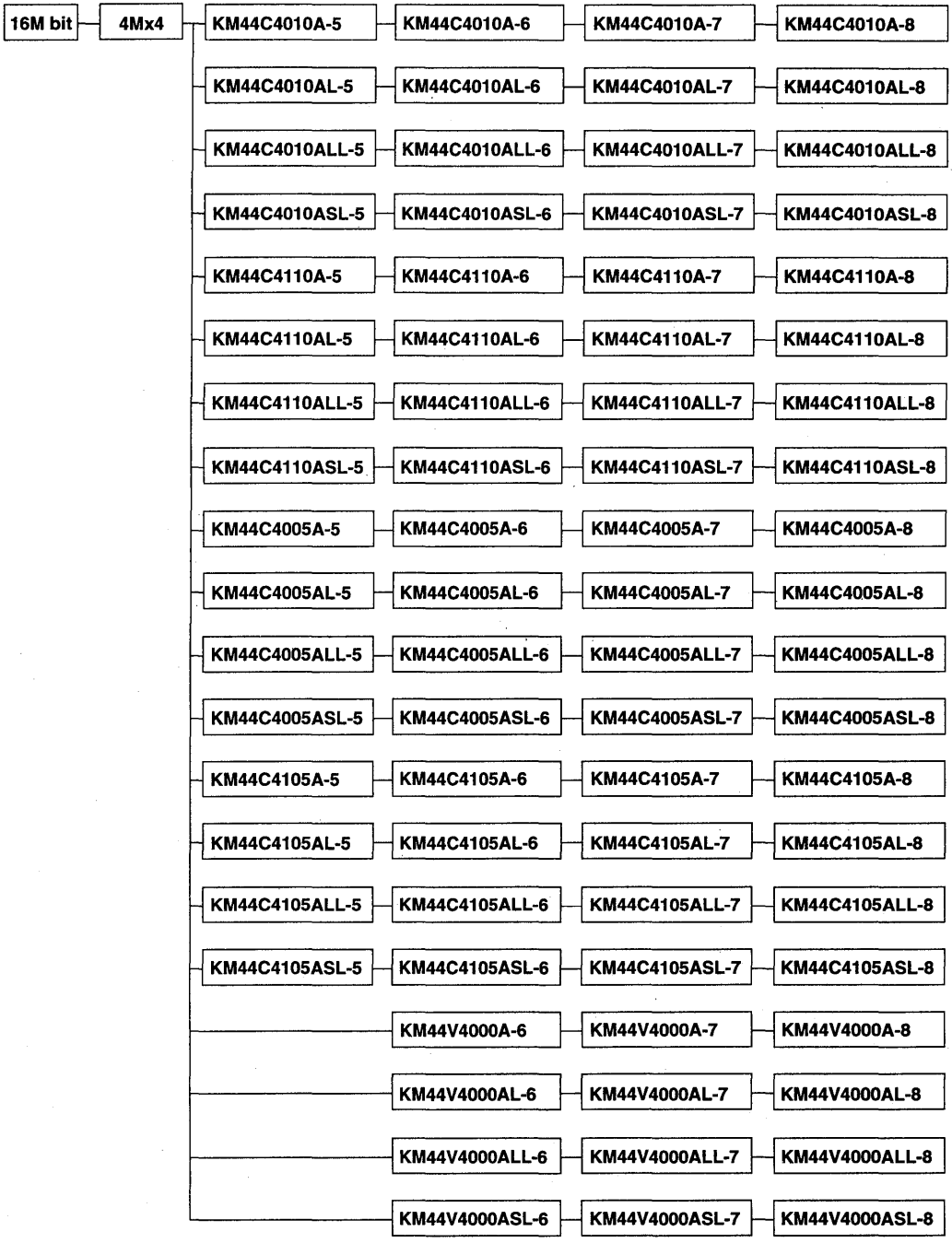
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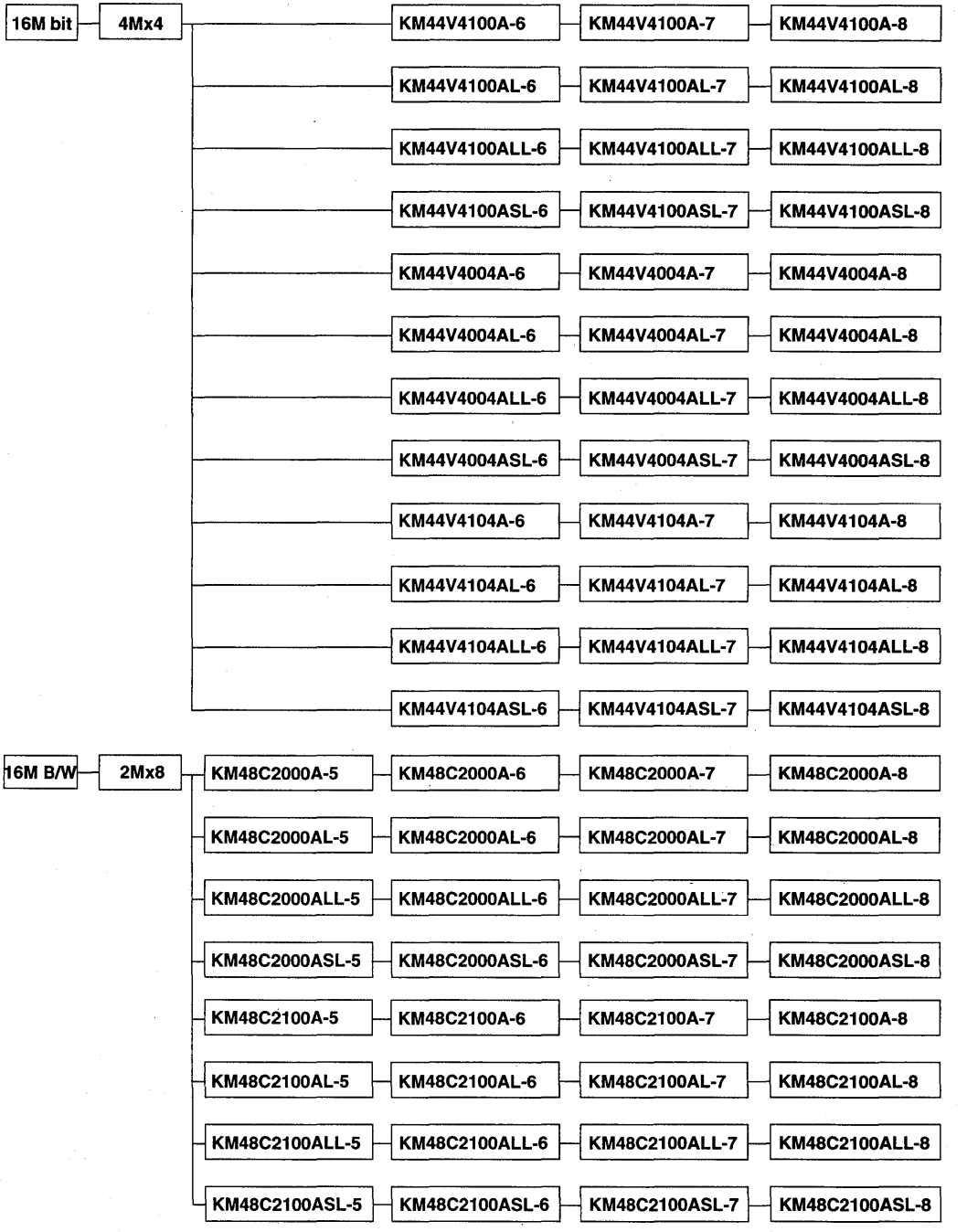
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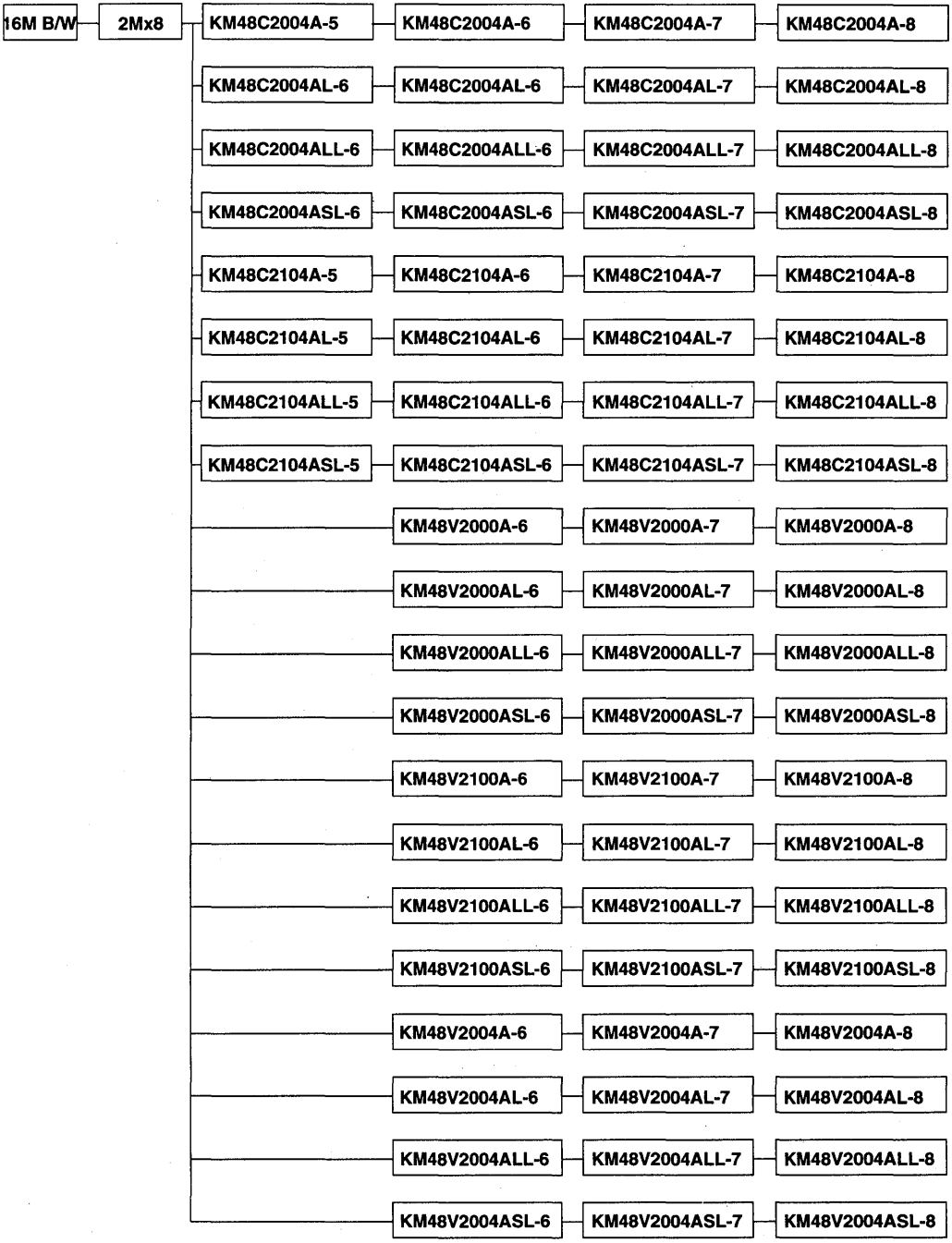
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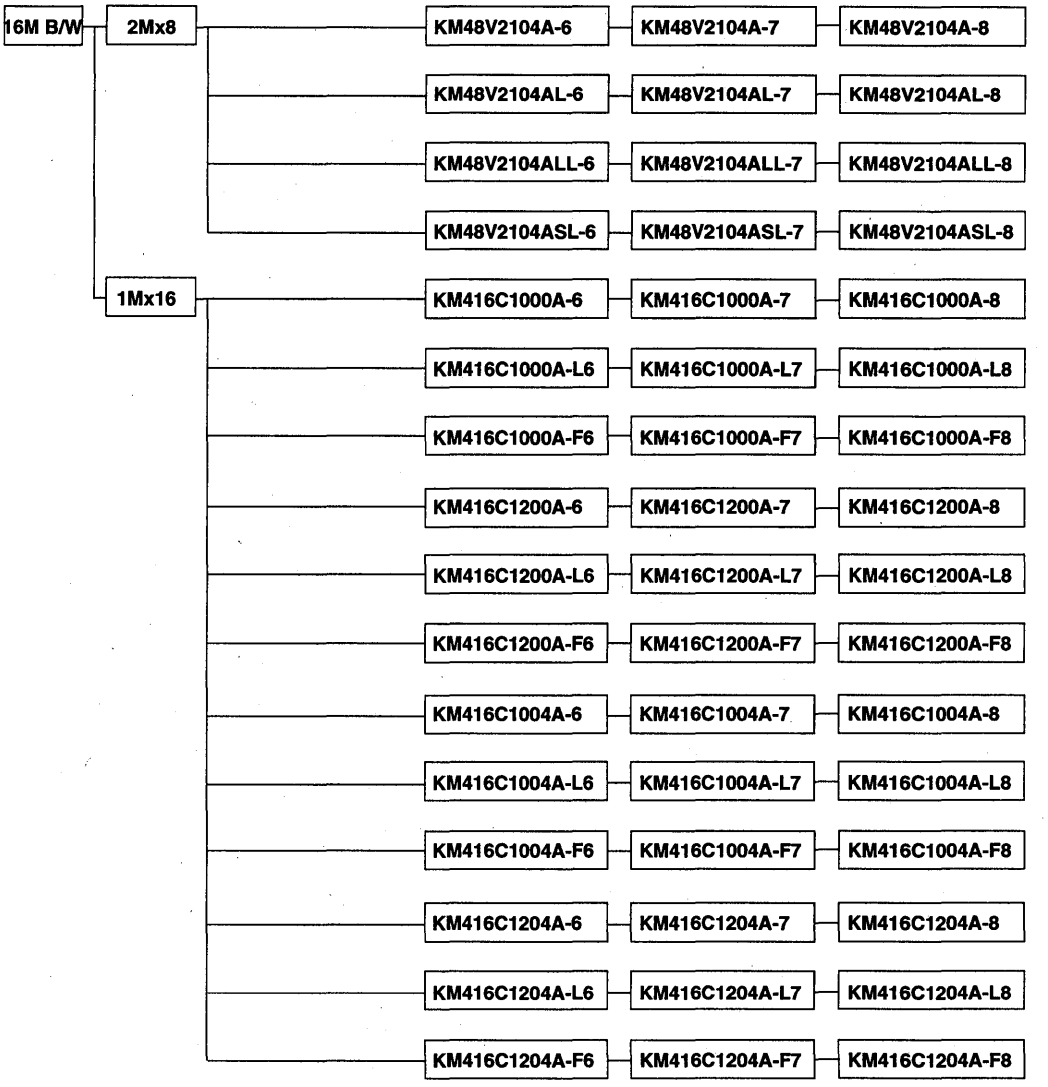
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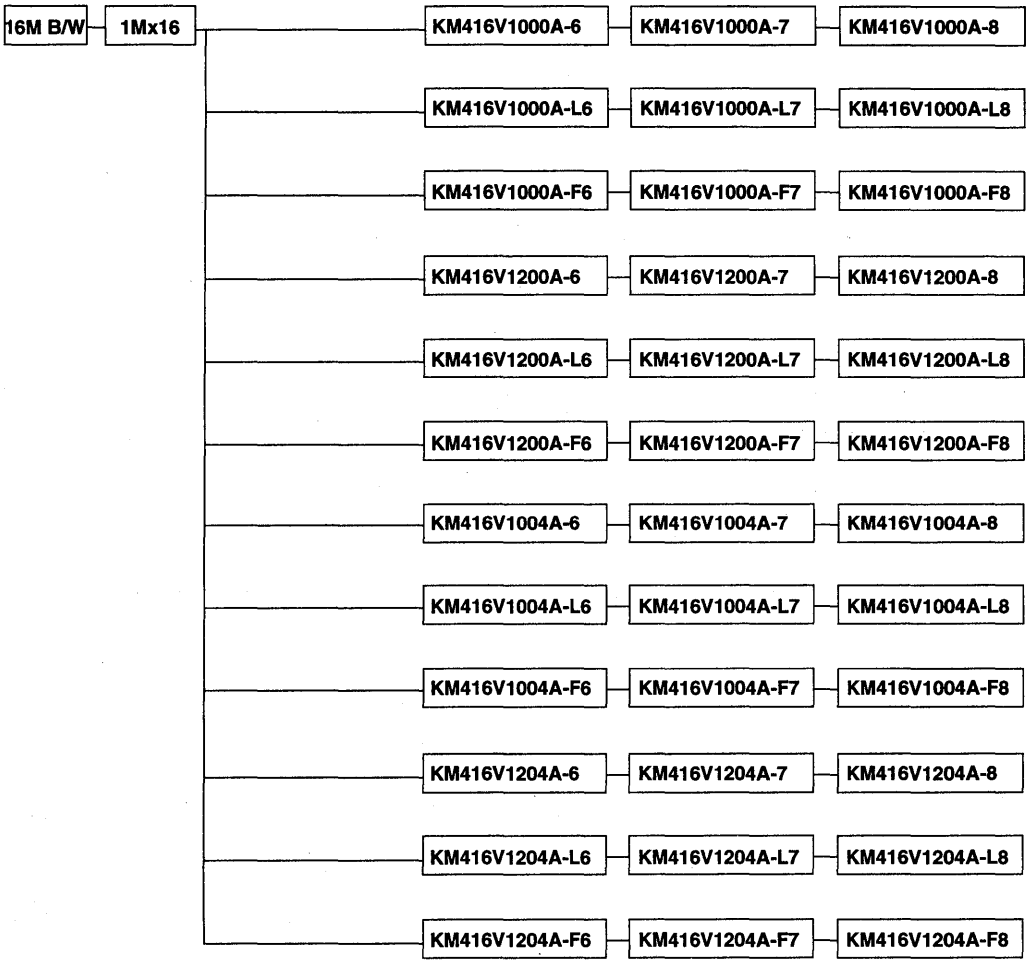
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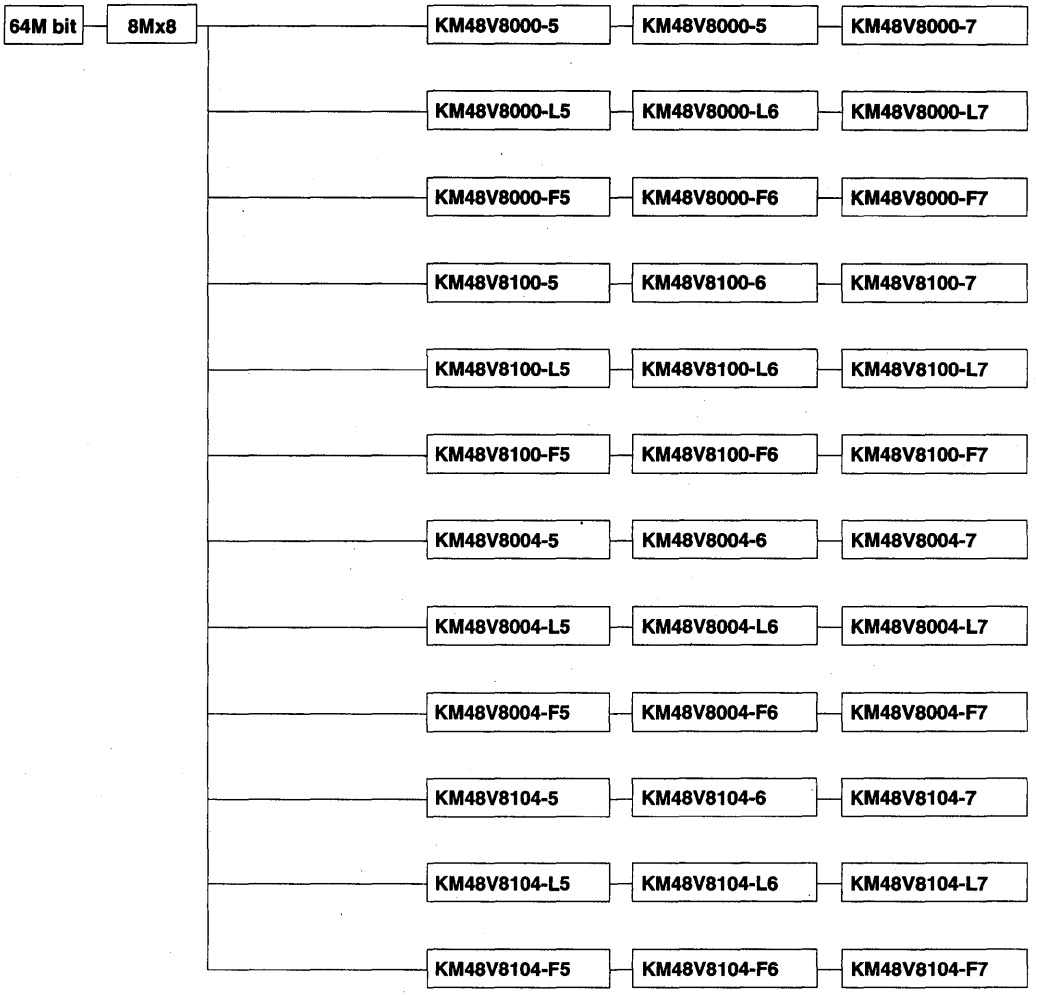
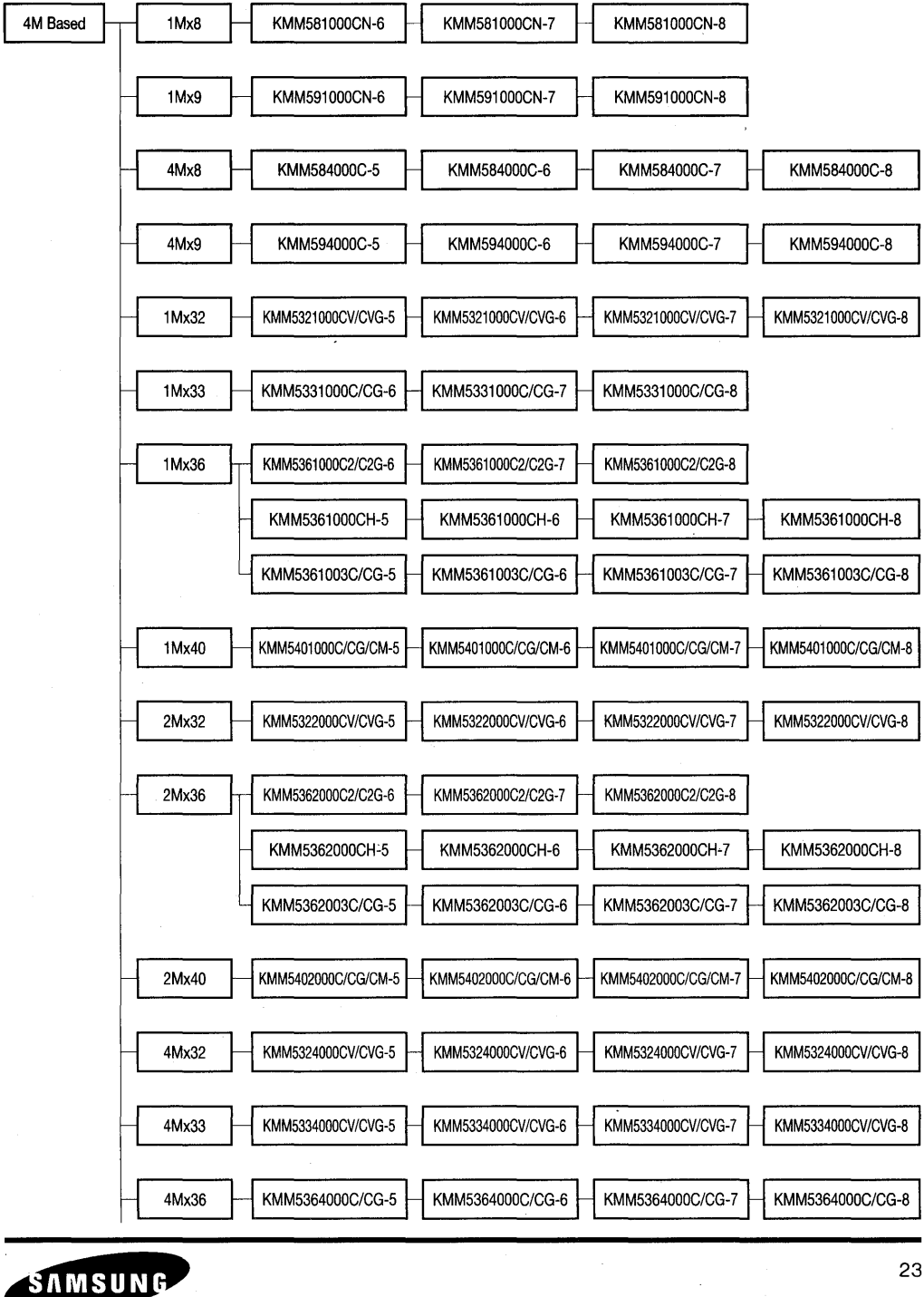
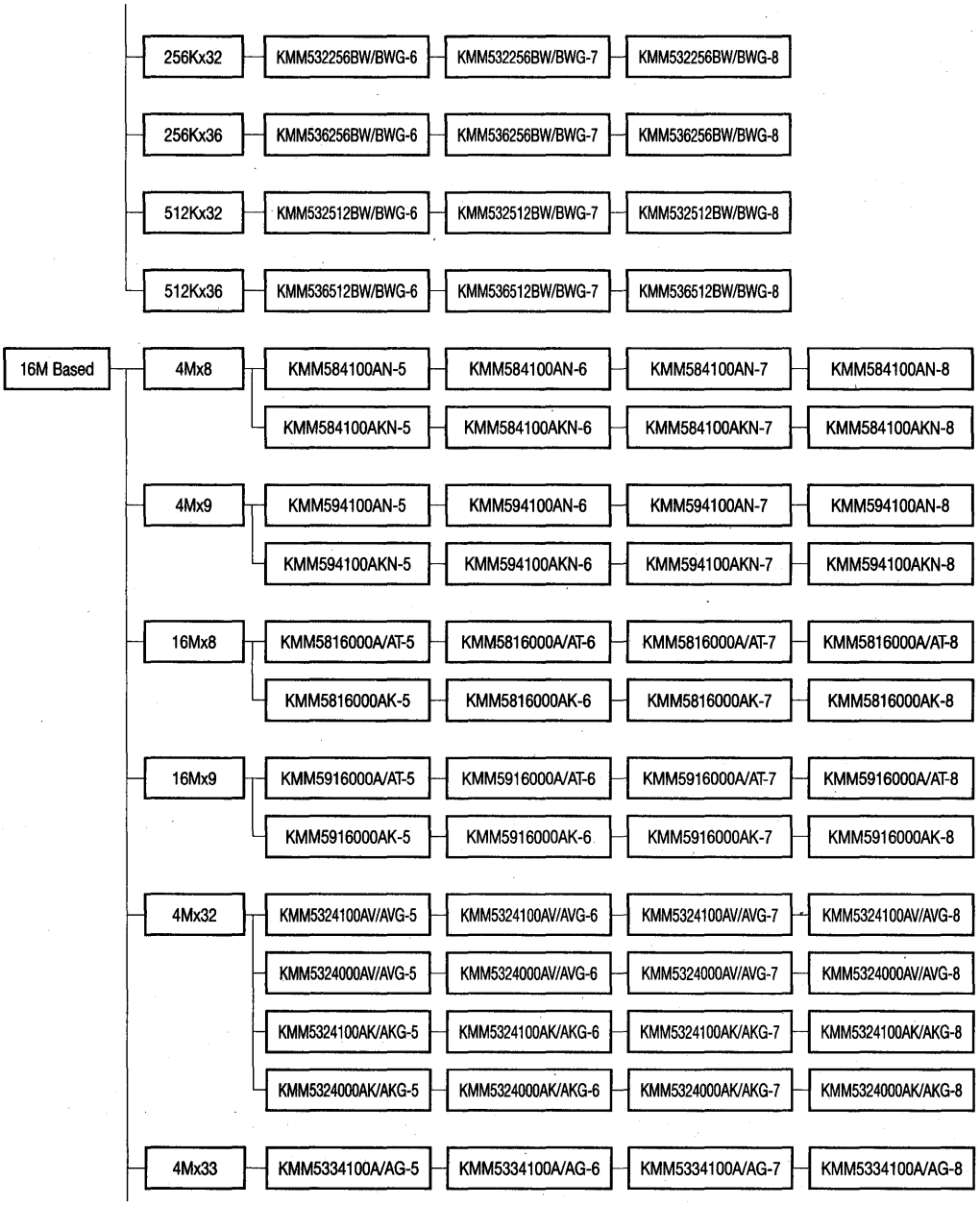
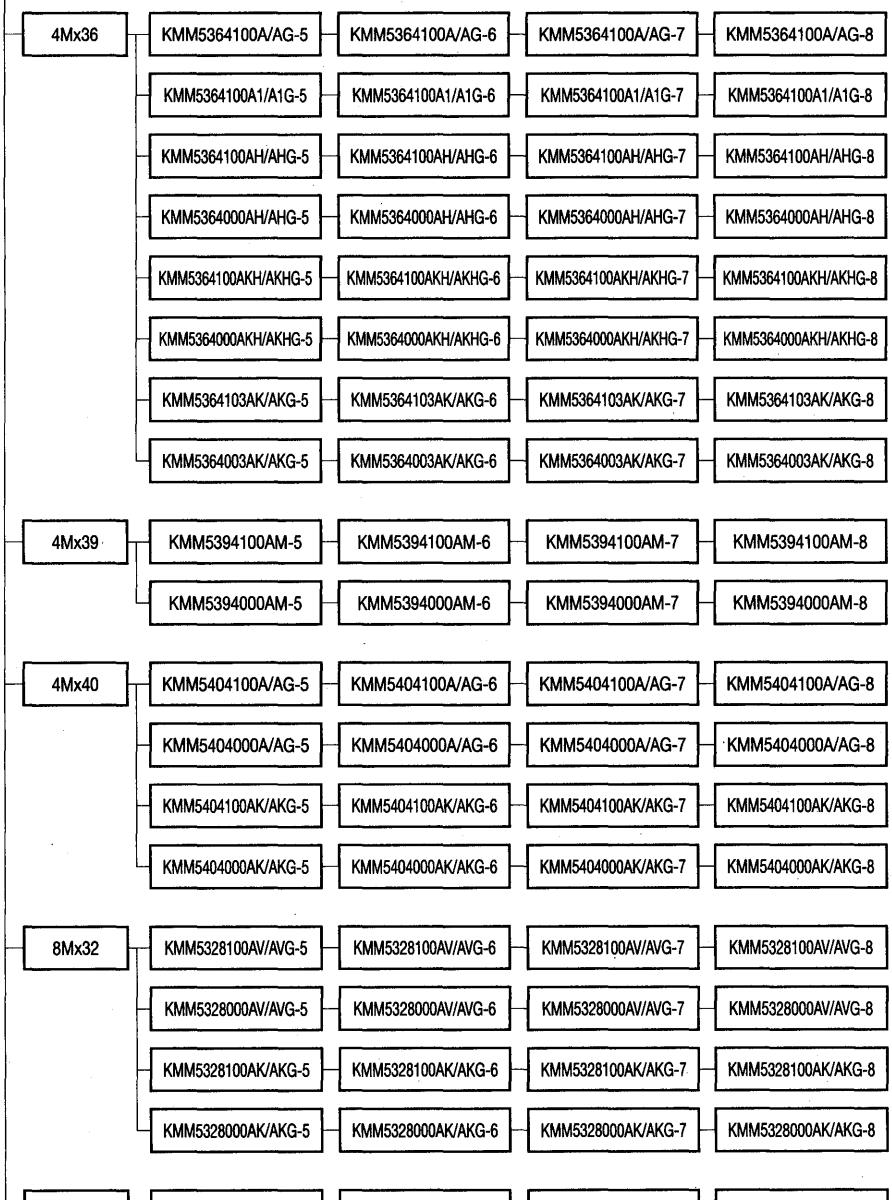
KM416V1204A-L8
KM416V1204A-F6
KM416V1204A-F7
KM416V1204A-F8


64M bit
8Mx8
KM48V8000-5
KM48V8000-5
KM48V8000-7
KM48V8000-L5
KM48V8000-L6
KM48V8000-L7
KM48V8000-F5
KM48V8000-F6
KM48V8000-F7
KM48V8100-5
KM48V8100-6
KM48V8100-7
KM48V8100-L5
KM48V8100-L6
KM48V8100-L7
KM48V8100-F5
KM48V8100-F6
KM48V8100-F7
KM48V8004-5
KM48V8004-6
KM48V8004-7
KM48V8004-L5
KM48V8004-L6
KM48V8004-L7
KM48V8004-F5
KM48V8004-F6
KM48V8004-F7
KM48V8104-5
KM48V8104-6
KM48V8104-7
KM48V8104-L5
KM48V8104-L6
KM48V8104-L7
KM48V8104-F5
KM48V8104-F6
KM48V8104-F7

1.2 Dynamic RAM Module




256Kx32
KMM532256BW/BWG-6
KMM532256BW/BWG-7
KMM532256BW/BWG-8
256Kx36
KMM536256BW/BWG-6
KMM536256BW/BWG-7
KMM536256BW/BWG-8
512Kx32
KMM532512BW/BWG-6
KMM532512BW/BWG-7
KMM532512BW/BWG-8
512Kx36
KMM536512BW/BWG-6
KMM536512BW/BWG-7
KMM536512BW/BWG-8
16M Based
4Mx8
KMM584100AN-5
KMM584100AN-6
KMM584100AN-7
KMM584100AN-8
KMM584100AKN-5
KMM584100AKN-6
KMM584100AKN-7
KMM584100AKN-8
4Mx9
KMM594100AN-5
KMM594100AN-6
KMM594100AN-7
KMM594100AN-8
KMM594100AKN-5
KMM594100AKN-6
KMM594100AKN-7
KMM594100AKN-8
16Mx8
KMM5816000A/AT-5
KMM5816000A/AT-6
KMM5816000A/AT-7
KMM5816000A/AT-8
KMM5816000AK-5
KMM5816000AK-6
KMM5816000AK-7
KMM5816000AK-8
16Mx9
KMM5916000A/AT-5
KMM5916000A/AT-6
KMM5916000A/AT-7
KMM5916000A/AT-8
KMM5916000AK-5
KMM5916000AK-6
KMM5916000AK-7
KMM5916000AK-8
4Mx32
KMM5324100AV/AVG-5
KMM5324100AV/AVG-6
KMM5324100AV/AVG-7
KMM5324100AV/AVG-8
KMM5324000AV/AVG-5
KMM5324000AV/AVG-6
KMM5324000AV/AVG-7
KMM5324000AV/AVG-8
KMM5324100AK/AKG-5
KMM5324100AK/AKG-6
KMM5324100AK/AKG-7
KMM5324100AK/AKG-8
KMM5324000AK/AKG-5
KMM5324000AK/AKG-6
KMM5324000AK/AKG-7
KMM5324000AK/AKG-8
4Mx33
KMM5334100A/AG-5
KMM5334100A/AG-6
KMM5334100A/AG-7
KMM5334100A/AG-8


4Mx36
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KMM5364100A/AG-6
KMM5364100A/AG-7
KMM5364100A/AG-8
KMM5364100A1/A1G-5
KMM5364100A1/A1G-6
KMM5364100A1/A1G-7
KMM5364100A1/A1G-8
KMM5364100AH/AHG-5
KMM5364100AH/AHG-6
KMM5364100AH/AHG-7
KMM5364100AH/AHG-8
KMM5364000AH/AHG-5
KMM5364000AH/AHG-6
KMM5364000AH/AHG-7
KMM5364000AH/AHG-8
KMM5364100AKH/AKHG-5
KMM5364100AKH/AKHG-6
KMM5364100AKH/AKHG-7
KMM5364100AKH/AKHG-8
KMM5364000AKH/AKHG-5
KMM5364000AKH/AKHG-6
KMM5364000AKH/AKHG-7
KMM5364000AKH/AKHG-8
KMM5364103AK/AKG-5
KMM5364103AK/AKG-6
KMM5364103AK/AKG-7
KMM5364103AK/AKG-8
KMM5364003AK/AKG-5
KMM5364003AK/AKG-6
KMM5364003AK/AKG-7
KMM5364003AK/AKG-8
4Mx39
KMM5394100AM-5
KMM5394100AM-6
KMM5394100AM-7
KMM5394100AM-8
KMM5394000AM-5
KMM5394000AM-6
KMM5394000AM-7
KMM5394000AM-8
4Mx40
KMM5404100A/AG-5
KMM5404100A/AG-6
KMM5404100A/AG-7
KMM5404100A/AG-8
KMM5404000A/AG-5
KMM5404000A/AG-6
KMM5404000A/AG-7
KMM5404000A/AG-8
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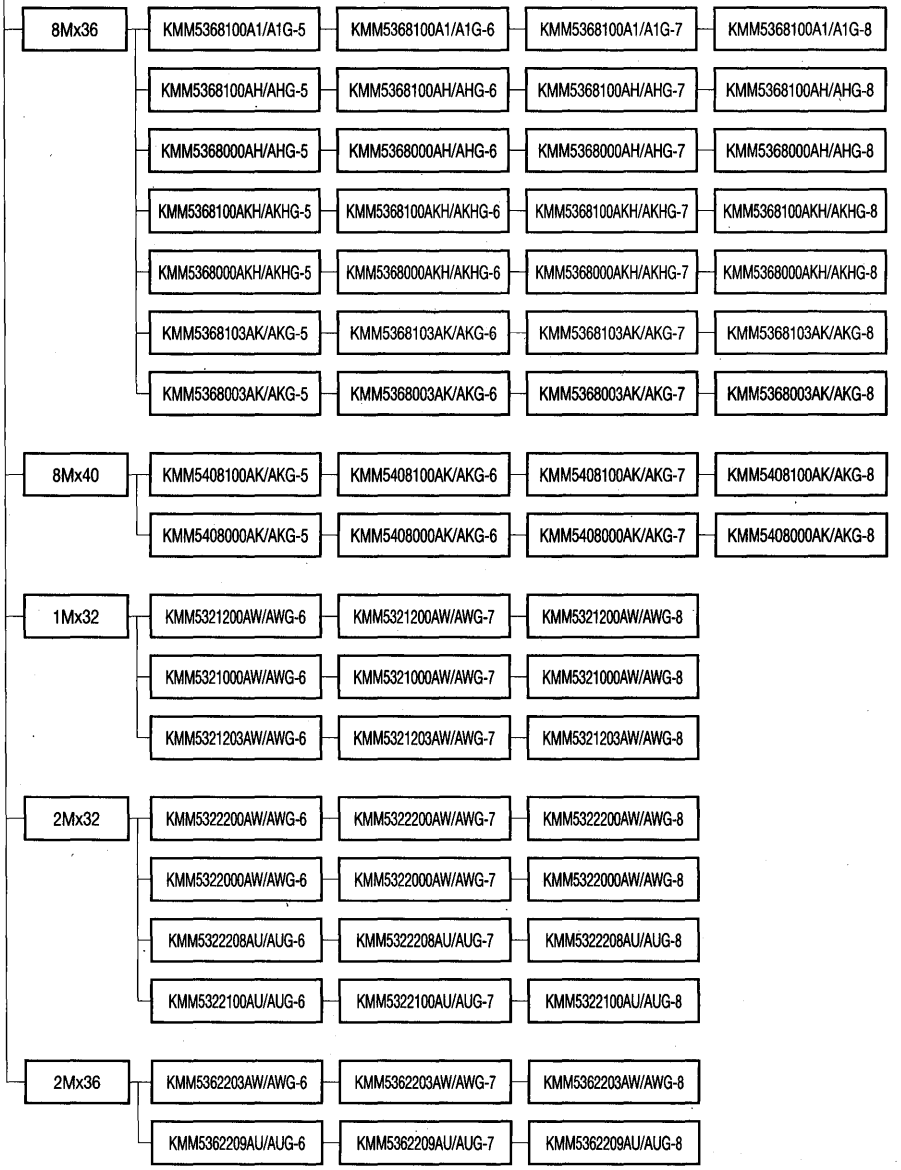
KMM5404100AK/AKG-6
KMM5404100AK/AKG-7
KMM5404100AK/AKG-8
KMM5404000AK/AKG-5
KMM5404000AK/AKG-6
KMM5404000AK/AKG-7
KMM5404000AK/AKG-8
8Mx32
KMM5328100AV/AVG-5
KMM5328100AV/AVG-6
KMM5328100AV/AVG-7
KMM5328100AV/AVG-8
KMM5328000AV/AVG-5
KMM5328000AV/AVG-6
KMM5328000AV/AVG-7
KMM5328000AV/AVG-8
KMM5328100AK/AKG-5
KMM5328100AK/AKG-6
KMM5328100AK/AKG-7
KMM5328100AK/AKG-8
KMM5328000AK/AKG-5
KMM5328000AK/AKG-6
KMM5328000AK/AKG-7
KMM5328000AK/AKG-8
8Mx33
KMM5338100AKV/AKVG-5
KMM5338100AKV/AKVG-6
KMM5338100AKV/AKVG-7
KMM5338100AKV/AKVG-8


8Mx36
KMM5368100A1/A1G-5
KMM5368100A1/A1G-6
KMM5368100A1/A1G-7
KMM5368100A1/A1G-8
KMM5368100AH/AHG-5
KMM5368100AH/AHG-6
KMM5368100AH/AHG-7
KMM5368100AH/AHG-8
KMM5368000AH/AHG-5
KMM5368000AH/AHG-6
KMM5368000AH/AHG-7
KMM5368000AH/AHG-8
KMM5368100AKH/AKHG-5
KMM5368100AKH/AKHG-6
KMM5368100AKH/AKHG-7
KMM5368100AKH/AKHG-8
KMM5368000AKH/AKHG-5
KMM5368000AKH/AKHG-6
KMM5368000AKH/AKHG-7
KMM5368000AKH/AKHG-8
KMM5368103AK/AKG-5
KMM5368103AK/AKG-6
KMM5368103AK/AKG-7
KMM5368103AK/AKG-8
KMM5368003AK/AKG-5
KMM5368003AK/AKG-6
KMM5368003AK/AKG-7
KMM5368003AK/AKG-8
8Mx40
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KMM5408100AK/AKG-6
KMM5408100AK/AKG-7
KMM5408100AK/AKG-8
KMM5408000AK/AKG-5
KMM5408000AK/AKG-6
KMM5408000AK/AKG-7
KMM5408000AK/AKG-8
1Mx32
KMM5321200AW/AWG-6
KMM5321200AW/AWG-7
KMM5321200AW/AWG-8
KMM5321000AW/AWG-6
KMM5321000AW/AWG-7
KMM5321000AW/AWG-8
KMM5321203AW/AWG-6
KMM5321203AW/AWG-7
KMM5321203AW/AWG-8
2Mx32
KMM5322200AW/AWG-6
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KMM5322200AW/AWG-8
KMM5322000AW/AWG-6
KMM5322000AW/AWG-7
KMM5322000AW/AWG-8
KMM5322208AU/AUG-6
KMM5322208AU/AUG-7
KMM5322208AU/AUG-8
KMM5322100AU/AUG-6
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KMM5322100AU/AUG-8
2Mx36
KMM5362203AW/AWG-6
KMM5362203AW/AWG-7
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KMM5362209AU/AUG-6
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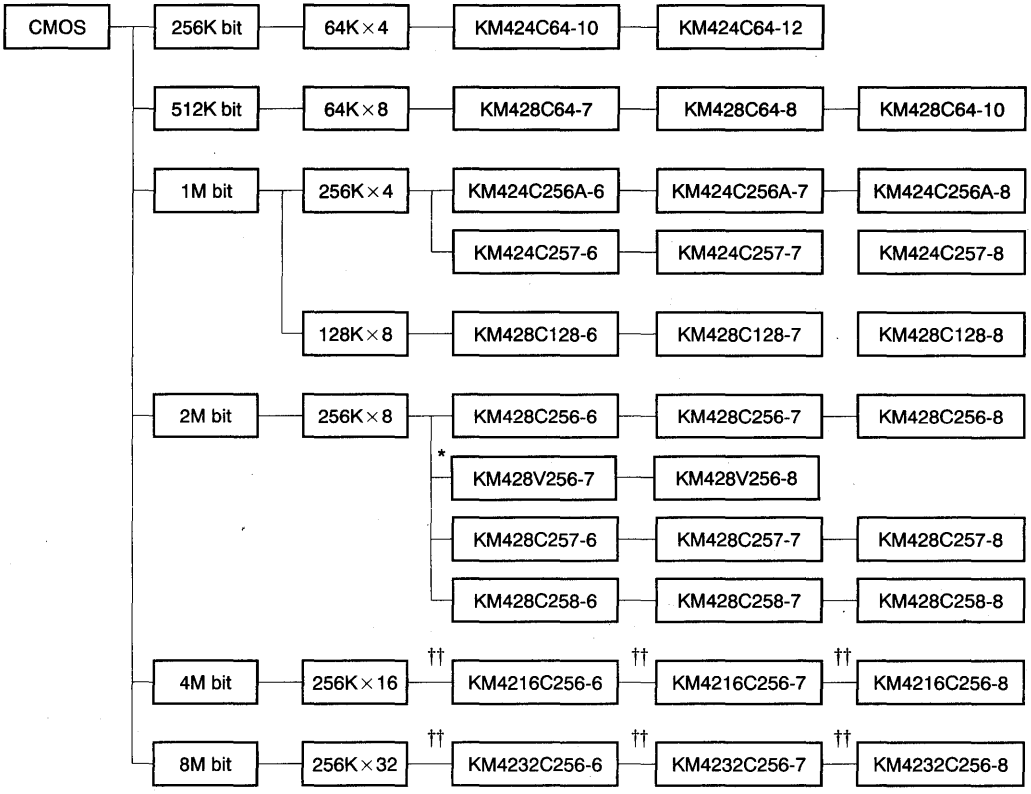
KMM5362209AU/AUG-8

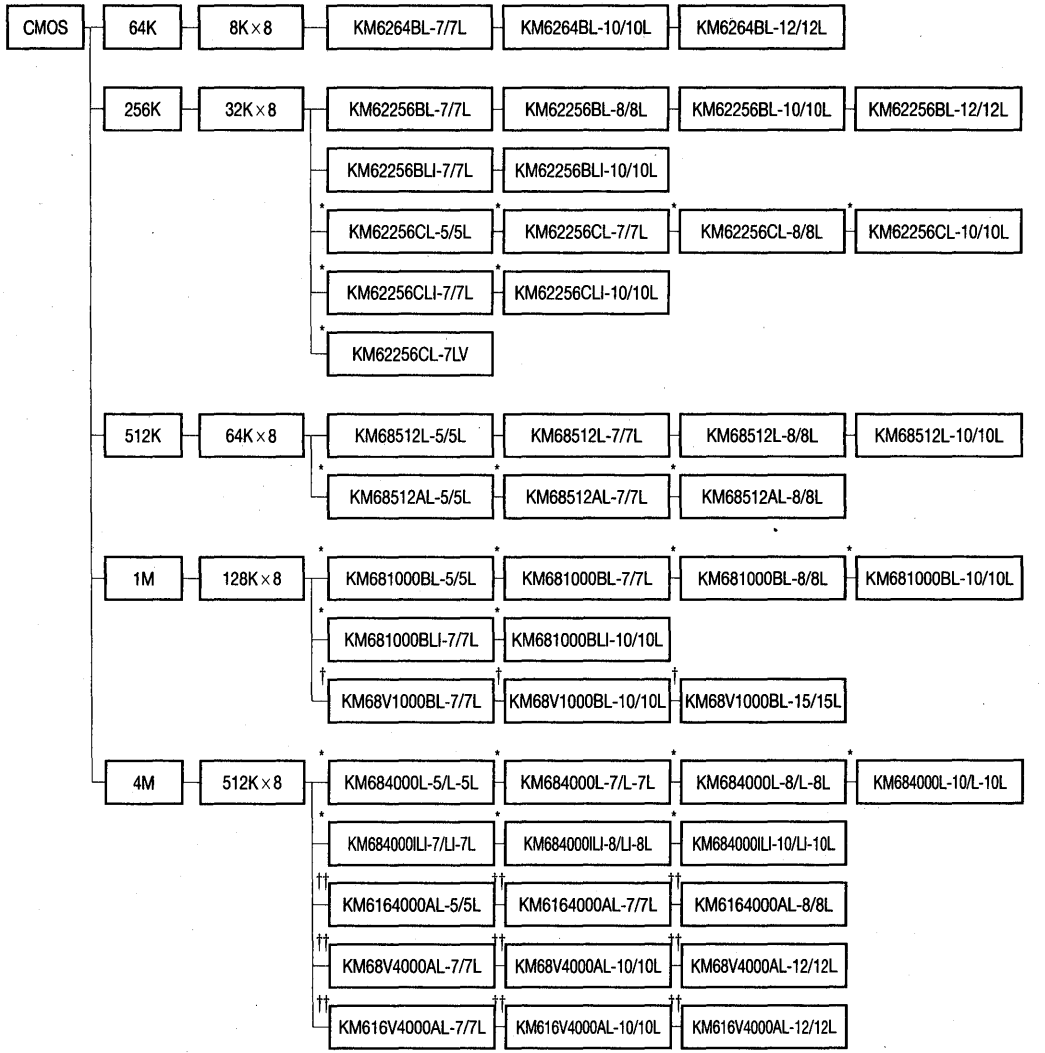
1.3 Video RAM



†† Under Development

1.4 Static RAM

Standard SRAM

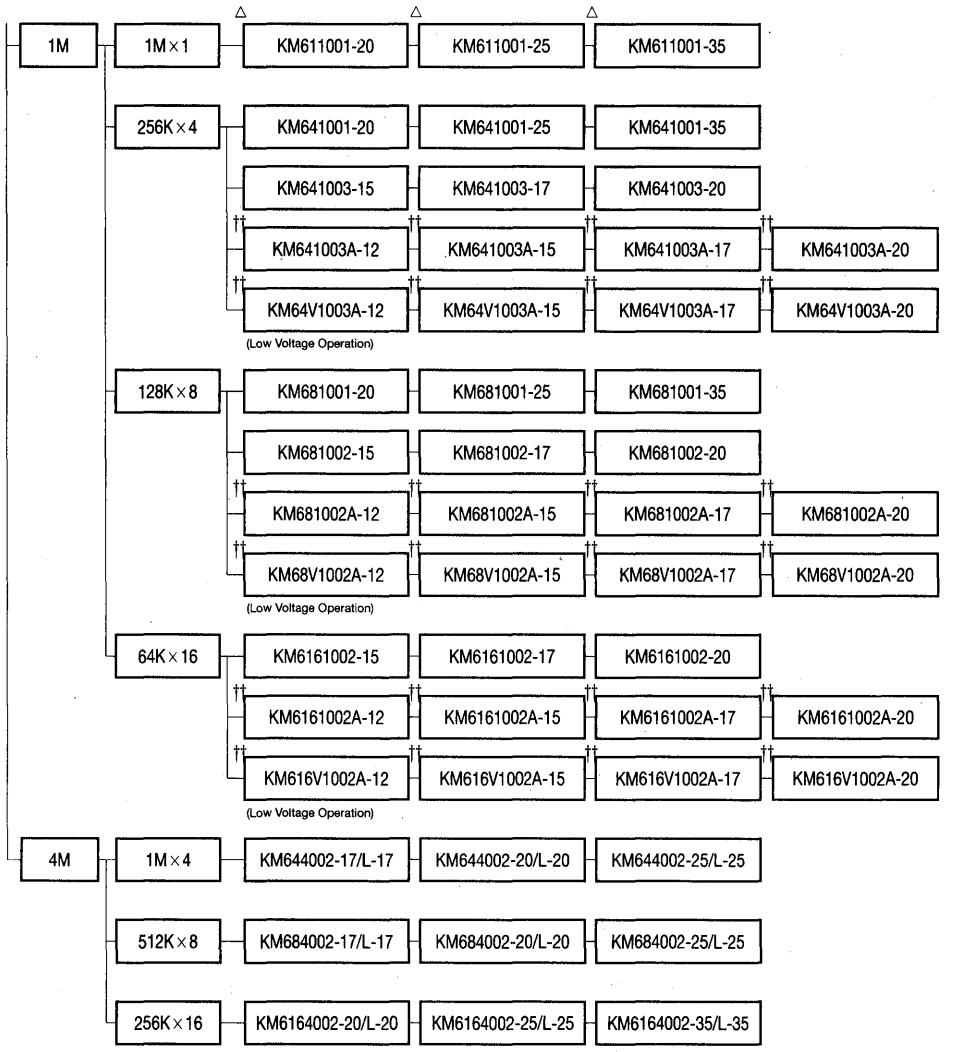


Pseudo SRAM

CMOS	1M	128K×8	KM658128A/L-8/8L	KM658128A/L-10/10L	KM658128A/L-12/12L

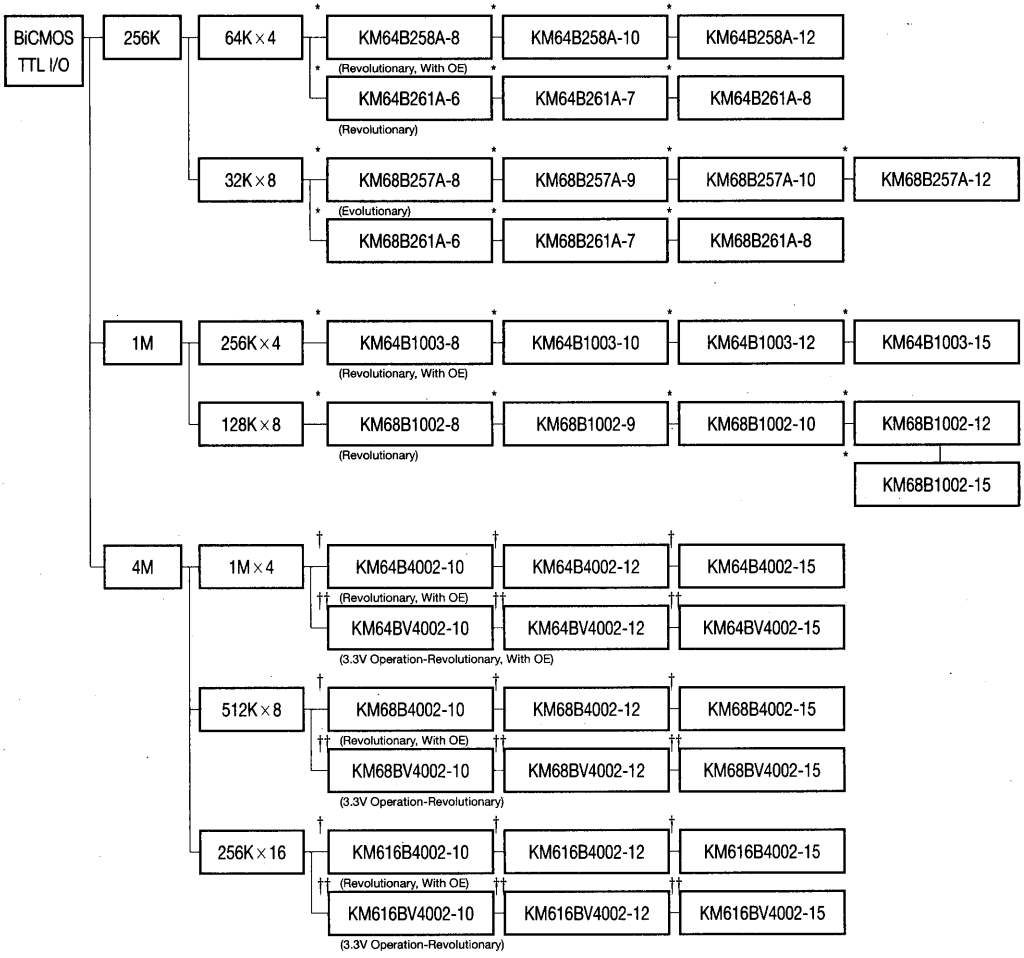
High Speed SRAM

CMOS	64K	16K×4	KM6465B-12	KM6465B-15	KM6465B-20	KM6465B-25
			KM6466B-12 (With OE)	KM6466B-15	KM6466B-20	KM6466B-25
		8K×8	KM6865B-12	KM6865B-15	KM6865B-20	KM6865B-25
	256K	64K×4	△ KM64258B-15 (With OE)	△ KM64258B-20	△ KM64258B-25	
			KM64258C-12 (With OE)	KM64258C-15	KM64258C-20	
			KM64V258C-15 (With OE)	KM64V258C-17	KM64V258C-20	
		32K×8	△ KM68257B-15	△ KM68257B-20	△ KM68257B-25	
			KM68258C-12	KM68258C-15	KM68258C-20	
			△ KM68V257-15 Low Voltage Operation	△ KM68V257-17	△ KM68V257-20	
			KM68V257C-15 (Low Voltage Operation)	KM68V257C-17	KM68V257C-20	
	512K	32K×16	△ KM616513-15	△ KM616513-17	△ KM616513-20	△ KM616513-25
			△ KM616V513-15 Low Voltage Operation	△ KM616V513-17	△ KM616V513-20	

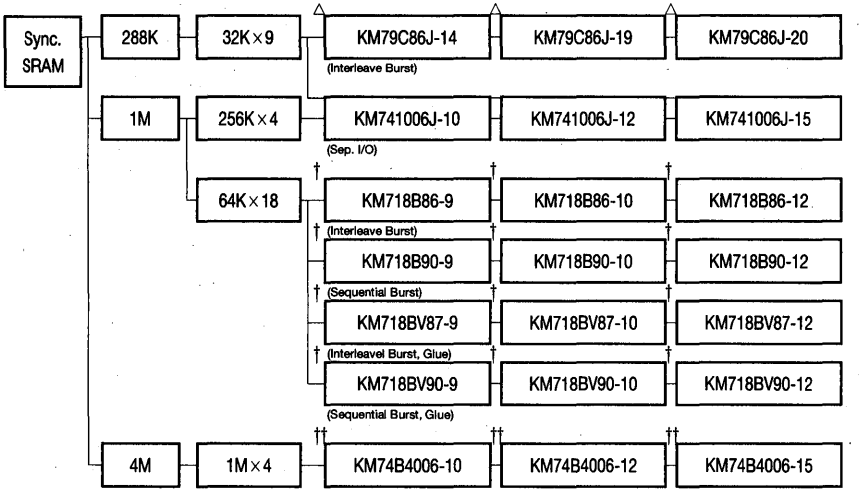


SAMSUNG ELECTRONICS

BiCMOS SRAM


BiCMOS TTL I/O
256K
64K×4
KM64B258A-8
KM64B258A-10
KM64B258A-12
(Revolutionary, With OE)
KM64B261A-6
KM64B261A-7
KM64B261A-8
(Revolutionary)
32K×8
KM68B257A-8
KM68B257A-9
KM68B257A-10
KM68B257A-12
(Evolutionary)
KM68B261A-6
KM68B261A-7
KM68B261A-8
1M
256K×4
KM64B1003-8
KM64B1003-10
KM64B1003-12
KM64B1003-15
(Revolutionary, With OE)
128K×8
KM68B1002-8
KM68B1002-9
KM68B1002-10
KM68B1002-12
KM68B1002-15
(Revolutionary)
4M
1M×4
KM64B4002-10
KM64B4002-12
KM64B4002-15
(Revolutionary, With OE)
KM64BV4002-10
KM64BV4002-12
KM64BV4002-15
(3.3V Operation-Revolutionary, With OE)
512K×8
KM68B4002-10
KM68B4002-12
KM68B4002-15
(Revolutionary, With OE)
KM68BV4002-10
KM68BV4002-12
KM68BV4002-15
(3.3V Operation-Revolutionary)
256K×16
KM616B4002-10
KM616B4002-12
KM616B4002-15
(Revolutionary, With OE)
KM616BV4002-10
KM616BV4002-12
KM616BV4002-15
(3.3V Operation-Revolutionary)

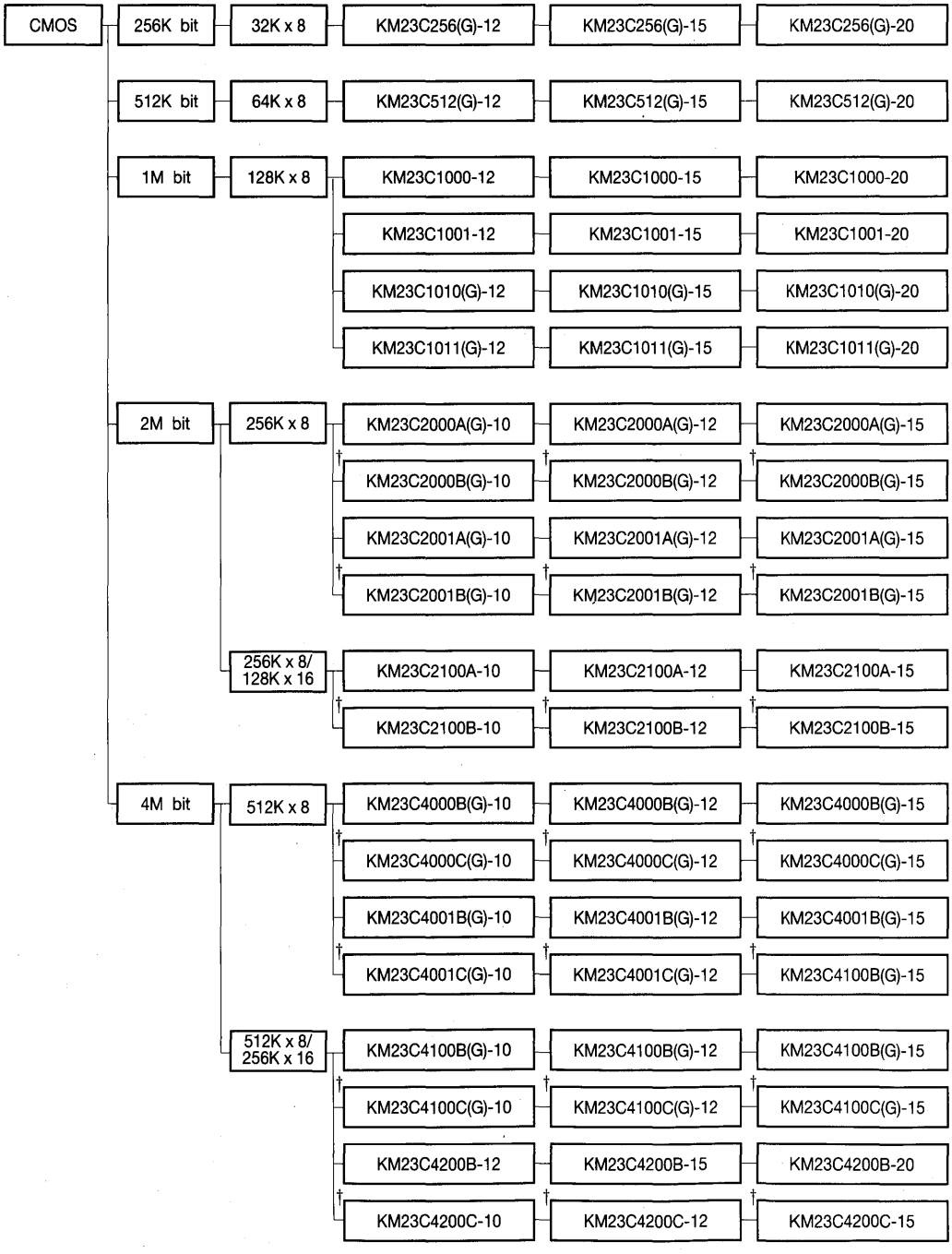
Specialty SRAM

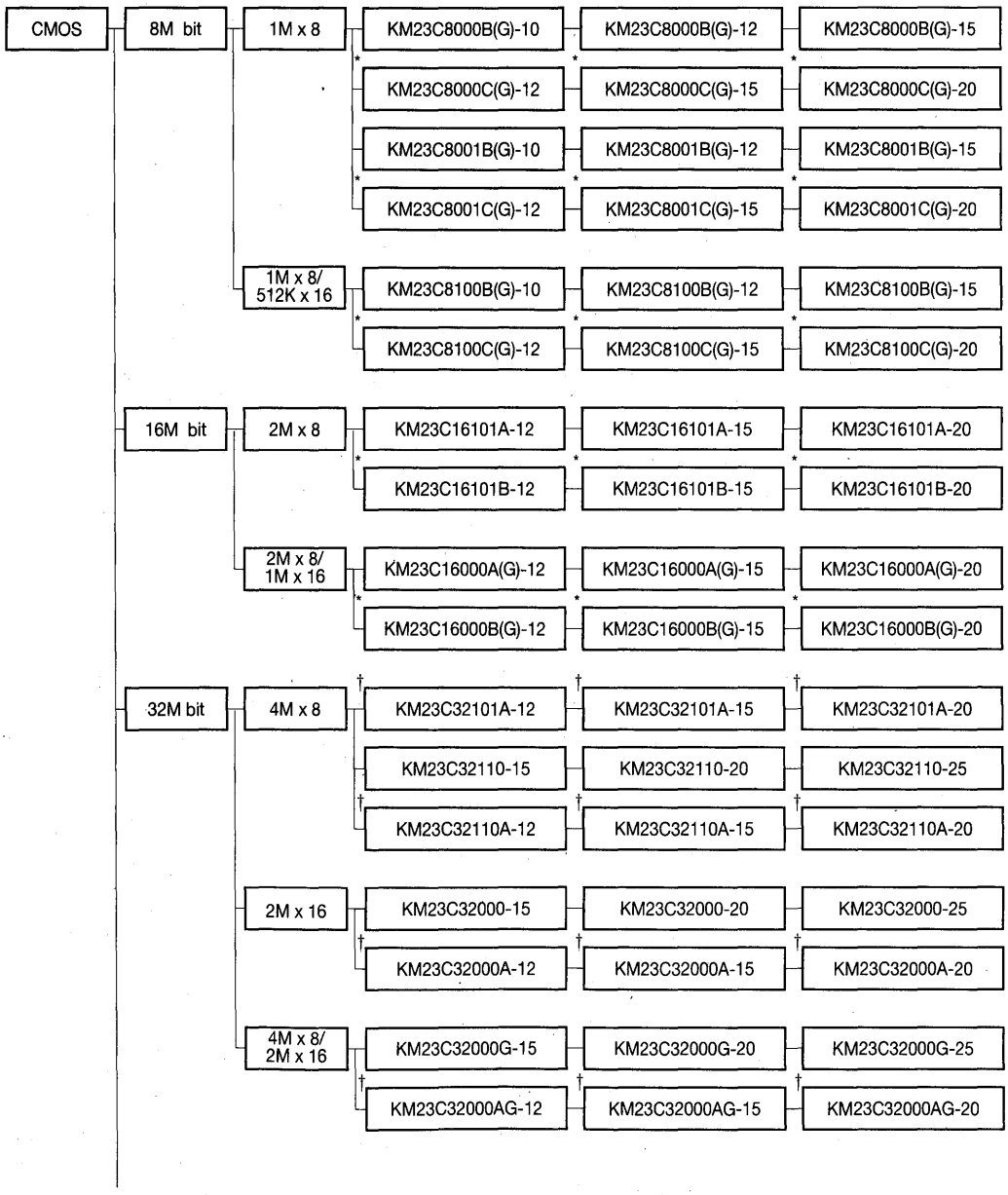


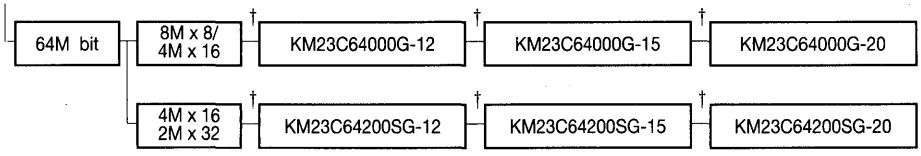
* : New Product † : Preliminary Product †† : Advanced Information △ : Last Time by Product

1.5 MASK ROM

Standard Product

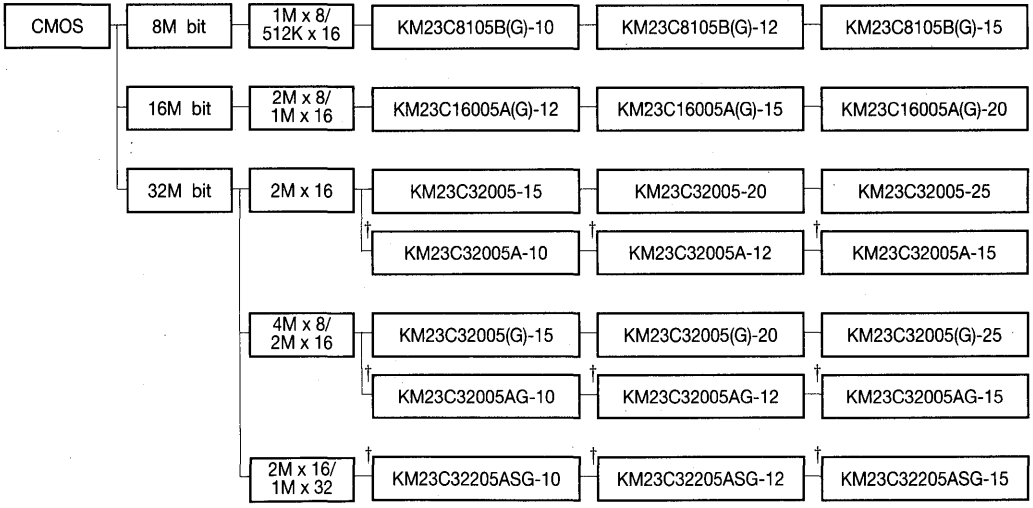



CMOS
8M bit
1M x 8
KM23C8000B(G)-10
KM23C8000B(G)-12
KM23C8000B(G)-15
KM23C8000C(G)-12
KM23C8000C(G)-15
KM23C8000C(G)-20
KM23C8001B(G)-10
KM23C8001B(G)-12
KM23C8001B(G)-15
KM23C8001C(G)-12
KM23C8001C(G)-15
KM23C8001C(G)-20
1M x 8/ 512K x 16
KM23C8100B(G)-10
KM23C8100B(G)-12
KM23C8100B(G)-15
KM23C8100C(G)-12
KM23C8100C(G)-15
KM23C8100C(G)-20
16M bit
2M x 8
KM23C16101A-12
KM23C16101A-15
KM23C16101A-20
KM23C16101B-12
KM23C16101B-15
KM23C16101B-20
2M x 8/ 1M x 16
KM23C16000A(G)-12
KM23C16000A(G)-15
KM23C16000A(G)-20
KM23C16000B(G)-12
KM23C16000B(G)-15
KM23C16000B(G)-20
32M bit
4M x 8
KM23C32101A-12
KM23C32101A-15
KM23C32101A-20
KM23C32110-15
KM23C32110-20
KM23C32110-25
KM23C32110A-12
KM23C32110A-15
KM23C32110A-20
2M x 16
KM23C32000-15
KM23C32000-20
KM23C32000-25
KM23C32000A-12
KM23C32000A-15
KM23C32000A-20
4M x 8/ 2M x 16
KM23C32000G-15
KM23C32000G-20
KM23C32000G-25
KM23C32000AG-12
KM23C32000AG-15
KM23C32000AG-20

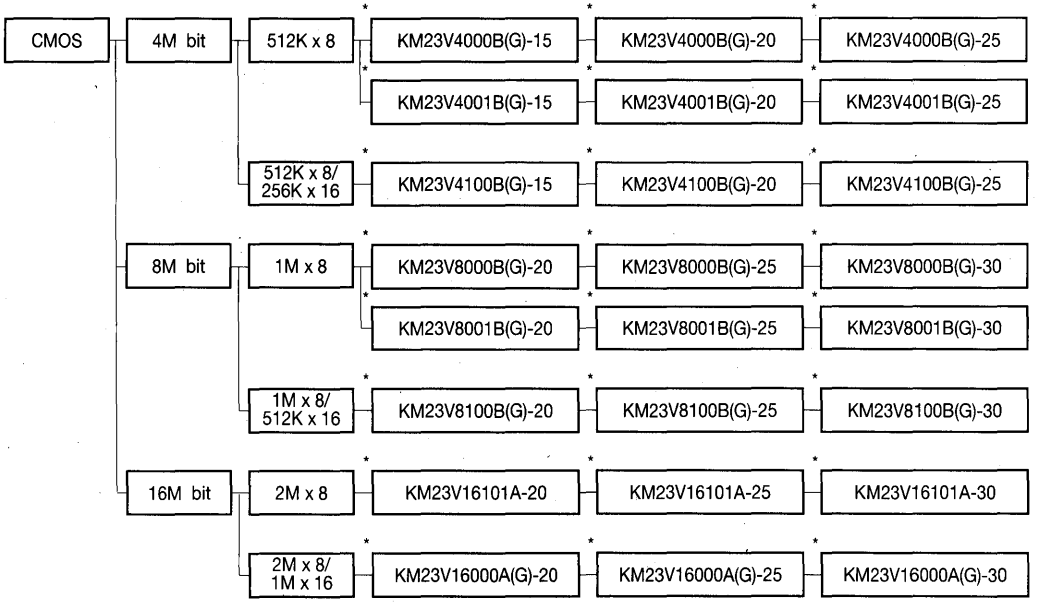


* : New Product
† : Under Development

Page Mode Product



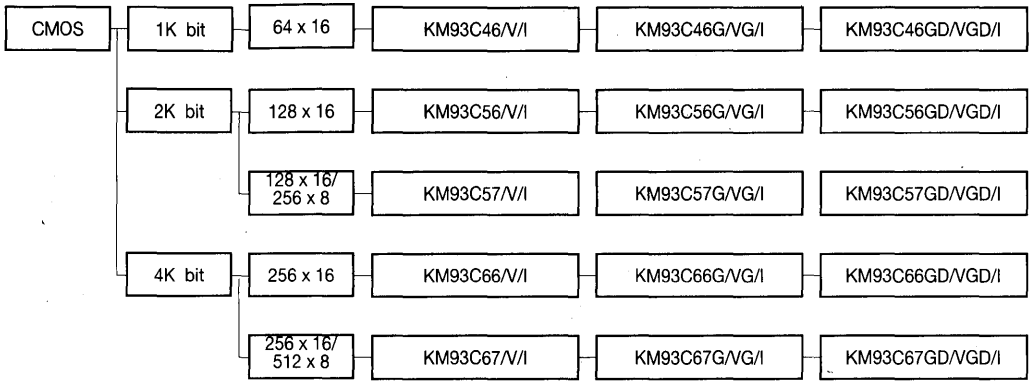
Low Voltage Product



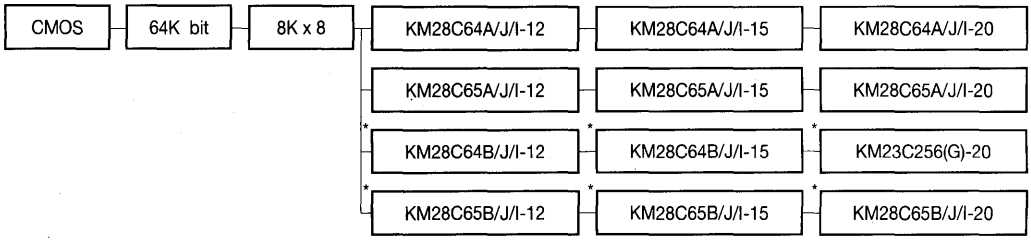
* : New Product
† : Under Development

1.6 EEPROM

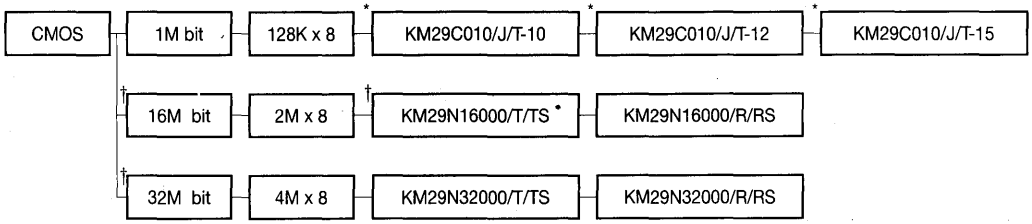
***Serial EEPROM**



***Parallel EEPROM**



1.7 Flash



* : New Product
† : Preliminary Product

2. PRODUCT GUIDE

2.1 Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
1M bit	1Mx1	5V±10%	KM41C1000C# KM41C1000CL# KM41C1000CSL#	60/70/80	Fast Page	P:18 Pin DIP J:20 Pin SOJ Z:20 Pin ZIP V:20 Pin TSOP-I (Forward) VR:20 Pin TSOP-I (Reverse) T:20 Pin TSOP-II (Forward) TR:20 Pin TSOP-II (Reverse
	256Kx4	5V±10%	KM44C256C# KM44C256CL# KM44C256CSL#	60/70/80	Fast Page	
4M bit	4Mx1	5V±10%	KM41C4000C# KM41C4000CL# KM41C4000CSL# KM41C4002C#	50/60/70/80	Fast Page Static Column	P:20 Pin DIP J:20 Pin SOJ Z:20 Pin ZIP V:20 Pin TSOP-I (Forward) VR:20 Pin TSOP-I (Reverse) T:20 Pin TSOP-II (Forward) TR:20 Pin TSOP-II (Reverse
		3.3V±10%	KM41V4000C# KM41V4000CL# KM41V4000CLL#	60/70/80	Fast Page	
	1Mx4	5V±10%	KM44C1000C# KM44C1000CL# KM44C1000CSL# KM44C1010C# KM44C1002C# KM44C1003C# KM44C1003CL# KM44C1003CSL# KM44C1004C# KM44C1004CL# KM44C1004CSL#	50/60/70/80	Fast Page Fast Page with WPB Static Column Quad CAS EDO	
		3.3V±10%	KM44V1000C# KM44V1000CL# KM44V1000CLL# KM44V1004C# KM44V1004CL# KM44V1004CLL#	60/70/80	Fast Page EDO	
4M B/W	512Kx8	5V±10%	KM48C512B# KM48C512BL#	50/60/70/80	Fast Page	

Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
4M B/W	512Kx8	5V±10%	KM48C512BLL# KM48C514B# KM48C514BL# KM48C514BLL#	50/60/70/80	Fast Page EDO	J:28 Pin SOJ Z:28 Pin ZIP T:28 Pin TSOP-II (Forward) TR:28 Pin TSOP-II (Reverse)
		3.3V±10%	KM48V512B# KM48V512BL# KM48V512BLL# KM48V514B# KM48V514BL# KM48V514BLL#	60/70/80	Fast Page EDO	
	512Kx9	5V±10%	KM49C512B# KM49C512BL# KM49C512BLL#	60/70/80	Fast Page	
	256Kx16	5V±10%	KM416C256B# KM416C256BL# KM416C256BLL# KM416C254B# KM416C254BL# KM416C254BLL# KM416C156B# KM416C156BL# KM416C156BLL# KM416C157B# KM416C157BL# KM416C157BLL#	50/60/70/80	Fast Page EDO Fast Page with 2WE	
		3.3V±10%	KM416V256B# KM416V256BL# KM416V256BLL# KM416V254B# KM416V254BL# KM416V254BLL#	60/70/80	Fast Page EDO	
	256Kx18	5V±10%	KM418C256B# KM418C256BL# KM418C256BLL#	60/70/80	Fast Page	
16M bit	16Mx1	5V±10%	KM41C16000A# KM41C16000AL# KM41C16000ALL# KM41C16000ASL#	50/60/70/80	Fast Page(4K)	J:24 Pin SOJ (400mil) T:24 Pin TSOP-II (Forward) (400mil)

Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
16M bit	16Mx1	5V±10%	KM41C16002A#	50/60/70/80	Static Column(4K)	TR:24 Pin TSOP-II (Reverse) (400mil)
		3.3V±10%	KM41V16000A#	60/70/80	Fast Page(4K)	K: 24 Pin SOJ (300mil)
			KM41V16000AL#			S: 24 Pin TSOP-II(Forward) (300mil)
			KM41V16000ALL#			SR: 24 Pin TSOP-II(Reverse) (300mil)
			KM41V16000ASL#			
	4Mx4	5V±10%	KM44C4000A#	50/60/70/80	Fast Page(4K)	
			KM44C4000AL#			
			KM44C4000ALL#			
			KM44C4000ASL#			
			KM44C4100A#		Fast Page(2K)	
			KM44C4100AL#			
			KM44C4100ALL#			
			KM44C4100ASL#			
			KM44C4002A#		Static Column(4K)	
			KM44C4102A#		Static Column(2K)	
			KM44C4003A#		Quad CAS(4K)	
			KM44C4003AL#			
			KM44C4003ALL#			
			KM44C4003ASL#			
			KM44C4103A#		Quad CAS(2K)	
			KM44C4103AL#			
			KM44C4103ALL#			
			KM44C4103ASL#			
			KM44C4004A#		EDO(4K)	
			KM44C4004AL#			
			KM44C4004ALL#			
			KM44C4004ASL#			
			KM44C4104A#		EDO(2K)	
			KM44C4104AL#			
			KM44C4104ALL#			
			KM44C4104ASL#			
			KM44C4010A#		Fast Page with WPB (4K)	
			KM44C4010AL#			
			KM44C4010ALL#			
			KM44C4010ASL#			
			KM44C4110A#		Fast Page with WPB (2K)	
			KM44C4110AL#			
			KM44C4110ALL#			
			KM44C4110ASL#			
			KM44C4005A#			
			KM44C4005AL#		EDO with Quad CAS (4K)	
			KM44C4005ALL#			

Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
16M bit	4Mx4	5V±10%	KM44C4005ASL#	50/60/70/80		J: 24 Pin SOJ (400mil)
			KM44C4105A#		EDO with Quad CAS (2K)	T:24 Pin TSOP-II (Forward) (400mil)
			KM44C4105AL#			TR:24 Pin TSOP-II (Reverse) (400mil)
			KM44C4105ALL#			K: 24 Pin SOJ (300mil)
			KM44C4105ASL#			S:24 Pin TSOP-II (Forward) (300mil)
		3.3V±10%	KM44V4000A#	60/70/80	Fast Page(4K)	SR:24 Pin TSOP-II(Reverse) (300mil)
			KM44V4000AL#			
			KM44V4000ALL#			
			KM44V4000ASL#			
			KM44V4100A#		Fast Page(2K)	
			KM44V4100AL#			
			KM44V4100ALL#			
			KM44V4100ASL#			
			KM44V4004A#		EDO(4K0	
			KM44V4004AL#			
			KM44V4004ALL#			
			KM44V4004ASL#			
			KM44V4104A#		EDO(2K)	
			KM44V4104AL#			
			KM44V4104ALL#			
			KM44V4104ASL#			
16M B/W	2Mx8	5V±10%	KM48C2000A#	50/ 60/70/80	Fast Page(4K)	J:28 Pin SOJ
			KM48C2000AL#			T:28 Pin TSOP-II (Forward)
			KM48C2000ALL#			TR:24 Pin TSOP-II(Reverse)
			KM48C2000ASL#			
			KM48C2100A#		Fast Page(2K)	
			KM48C2100AL#			
			KM48C2100ALL#			
			KM48C2100ASL#			
			KM48C2004A#		EDO(4K)	
			KM48C2004AL#			
			KM48C2004ALL#			
			KM48C2004ASL#			
			KM48C2104A#		EDO(2K)	
			KM48C2104AL#			
			KM48C2104ALL#			
			KM48C2104ASL#			

Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
16M B/W	2Mx8	3.3V±10%	KM48V2000A#	60/70/80	Fast Page(4K)	J:28 Pin SOJ
			KM48V2000AL#			T:28 Pin TSOP-II (Forward)
			KM48V2000ALL#			TR:28 Pin TSOP-II(Reverse)
			KM48V2100A#		Fast Page(2K)	
			KM48V2100AL#			
			KM48V2100ALL#			
			KM48V2004A#		EDO(4K)	
			KM48V2004AL#			
			KM48V2004ALL#			
			KM48V2104A#		EDO(2K)	
			KM48V2104AL#			
			KM48V2104ALL#			
	1Mx16	5V±10%	KM416C1000A#	60/70/80	Fast Page(4K)	J:42 Pin SOJ
			KM416C1000A#-L			T:44 Pin TSOP-II (Forward)
			KM416C1000A#-F			R:44 Pin TSOP-II(Reverse)
			KM416C1200A#		Fast Page(1K)	
			KM416C1200A#-L			
			KM416C1200A#-F			
			KM416C1004A#		EDO(4K)	
			KM416C1004A#-L			
			KM416C1004A#-F			
			KM416C1204A#		EDO(1K)	
			KM416C1204A#-L			
			KM416C1204A#-F			
		3.3V±10%	KM416V1000A#	60/70/80	Fast Page(4K)	
			KM416V1000A#-L			
			KM416V1000A#-F			
			KM416V1200A#		Fast Page(1K)	
			KM416V1200A#-L			
			KM416V1200A#-F			

Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
16M B/W	1Mx16	3.3V±10%	KM416V1004A#	50/60/70	EDO(4K)	J:42 Pin SOJ
			KM416V1004A#-L			T:44 Pin TSOP-II (Forward)
			KM416V1004A#-F			R:44 Pin TSOP-II(Reverse)
			KM416V1204A#		EDO(1K)	
			KM416V1204A#-L			
			KM416V1204A#-F			
64M bit	8Mx8	3.3V±10%	KM48V8000#	50/60/70	Fast Page(8K)	J:34 Pin SOJ
			KM48V8000#-L			T:34 Pin TSOP-II (Forward)
			KM48V8000#-F			R:34 Pin TSOP-II(Reverse)
			KM48V8100#		Fast Page(4K)	
			KM48V8100#-L			
			KM48V8100#-F			
			KM48V8004#		EDO(8K)	
			KM48V8004#-L			
			KM48V8004#-F			
			KM48V8104#		EDO(4K)	
			KM48V8104#-L			
			KM48V8104#-F			

2.2 Dynamic RAM Module

Org.	Part No.	Feature	Speed(ns)	Package	PCB Height	Refresh cycle/ms	C/S
DRAM SIMM Based on 4M DRAM							
1Mx8	KMM581000CN	F/P	60/70/80	S, 30 Pin SIMM	650	1024/16	NOW
1Mx9	KMM591000CN	F/P	60/70/80	S, 30 Pin SIMM	650	1024/16	NOW
4Mx8	KMM584000C	F/P	60/70/80	S, 72 Pin SIMM	805	1024/16	NOW
4Mx9	KMM594000C	F/P	60/70/80	S, 72 Pin SIMM	805	1024/16	NOW
1Mx32	KMM5321000CV/CVG	F/P	50/60/70/80	S, 72 Pin SIMM	855	1024/16	NOW
1Mx33	KMM5331000C/CG	F/P	60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
1Mx36	KMM5361000C2/C2G	F/P, PLCC	60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW
1Mx36	KMM5361000CH	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW
1Mx36	KMM5361003C/CG	F/P, QCAS	50/60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW
1Mx40	KMM5401000C/CG/CM	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW
2Mx32	KMM5322000CV/CVG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx36	KMM5362000C2/C2G	F/P, PLCC	60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx36	KMM5362000CH	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx36	KMM5362003C/CG	F/P, QCAS	50/60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx40	KMM5402000C/CG/CM	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
4Mx32	KMM5324000CV/CVG	Double Nocth	50/60/70/80	D, 72 Pin SIMM	1290	1024/16	NOW
4Mx33	KMM5334000CV/CVG	Double Nocth	50/60/70/80	D, 72 Pin SIMM	1290	1024/16	NOW
4Mx36	KMM5364000C/CG	Double Nocth	50/60/70/80	D, 72 Pin SIMM	1290	1024/16	NOW
DRAM SIMM Based on 4M B/W DRAM							
256Kx32	KMM532256BW/BWG	F/P	60/70/80	S, 72 Pin SIMM	1000	512/8	NOW
256Kx36	KMM536256BW/BWG	F/P	60/70/80	S, 72 Pin SIMM	1000	512/8	NOW
512Kx32	KMM532512BW/BWG	F/P	60/70/80	D, 72 Pin SIMM	1000	512/8	NOW
512Kx36	KMM536512BW/BWG	F/P	60/70/80	D, 72 Pin SIMM	1000	512/8	NOW
DRAM SIMM Based on 16M DRAM							
4Mx8	KMM584100AN	F/P	50/60/70/80	S, 30 Pin SIMM	650	2048/32	NOW
4Mx8	KMM584100AKN	F/P	50/60/70/80	S, 30 Pin SIMM	650	2048/32	'94, 4Q
4Mx9	KMM594100AN	F/P	50/60/70/80	S, 30 Pin SIMM	650	2048/32	NOW
4Mx9	KMM594100AN	F/P	50/60/70/80	S, 30 Pin SIMM	650	2048/32	'94, 4Q
16Mx8	KMM5816000A/AT	F/P	50/60/70/80	D, 30 Pin SIMM	900	4096/64	NOW
16Mx8	KMM5816000AK	F/P	50/60/70/80	D, 30 Pin SIMM	900	4096/64	'94, 4Q
16Mx9	KMM5916000A/AT	F/P	50/60/70/80	D, 30 Pin SIMM	900	4096/64	NOW
16Mx9	KMM5916000AK	F/P	50/60/70/80	D, 30 Pin SIMM	900	4096/64	'94, 4Q
4Mx32	KMM5324100AV/AVG	F/P	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx32	KMM5324000AV/AVG	F/P	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx32	KMM5324100AK/AKG	F/P	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx32	KMM5324000AK/AKG	F/P	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx33	KMM5334100A/AG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW

2.2 Dynamic RAM Module (Continued)

Org.	Part No.	Feature	Speed(ns)	Package	PCB Height	Refresh cycle/ms	C/S
DRAM SIMM Based on 16M DRAM							
4Mx36	KMM5364100A/AG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
4Mx36	KMM5364100A1/A1G	F/P	50/60/70/80	S, 72 Pin SIMM	1250	2048/32	NOW
4Mx36	KMM5364100AH/AHG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx36	KMM5364000AH/AHG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx36	KMM5364100AKH/AKHG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	'94, 4Q
4Mx36	KMM5364000AKH/AKHG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	'94, 4Q
4Mx36	KMM5364103AK/AKG	F/P, QCAS	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx36	KMM5364003AK/AKG	F/P, QCAS	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx39	KMM5394100AM	F/P	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx39	KMM5394000AM	F/P	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx40	KMM5404100A/AG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx40	KMM5404000A/AG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx40	KMM5404100AK/AKG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	'94, 4Q
4Mx40	KMM5404000AK/AKG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	'94, 4Q
8Mx32	KMM5328100AV/AVG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
8Mx32	KMM5328000AV/AVG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	4096/64	NOW
8Mx32	KMM5328100AK/AKG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
8Mx32	KMM5328000AK/AKG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	4096/64	NOW
8Mx33	KMM5338100AKV/AKVG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
8Mx36	KMM5368100A1/A1G	F/P	50/60/70/80	D, 72 Pin SIMM	1375	2048/32	NOW
8Mx36	KMM5368100AH/AHG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1250	2048/32	NOW
8Mx36	KMM5368000AH/AHG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1250	4096/64	NOW
8Mx36	KMM5368100AKH/AKHG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	'94, 4Q
8Mx36	KMM5368000AKH/AKHG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	4096/64	'94, 4Q
8Mx36	KMM5368103AK/AKG	F/P, QCAS	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
8Mx36	KMM5368003AK/AKG	F/P, QCAS	50/60/70/80	D, 72 Pin SIMM	1000	4096/64	NOW
8Mx40	KMM5408100AK/AKG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	'94, 4Q
8Mx40	KMM5408000AK/AKG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	4096/64	'94, 4Q
DRAM SIMM Based on 16M B/W DRAM							
1Mx32	KMM5321200AW/AWG	F/P	60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
1Mx32	KMM5321000AW/AWG	F/P	60/70/80	D, 72 Pin SIMM	1000	4096/64	NOW
1Mx32	KMM5321203AW/AWG	F/P	60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx32	KMM5322200AW/AWG	F/P	60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx32	KMM5322000AW/AWG	F/P	60/70/80	D, 72 Pin SIMM	1000	4096/64	NOW
2Mx32	KMM5322103AU/AUG	F/P, QCAS	60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
2Mx32	KMM5322208AU/AUG	F/P, AND	60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW
2Mx36	KMM5362209AU/AUG	F/P, AND	60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW

2.3 Video RAM

Capacity	Part Number	Orgnization	Speed(ns)	Technology	Features	Package	Remark
256K	KM424C64	64K×4	100/120	CMOS	M/F	24Pin DIP/ZIP	NOW
512K	KM428C64	64K×8	70/80/100	CMOS	M/F	40PIN SOJ	NOW
1M	KM424C256A	256K×4	60/70/80	CMOS	M/F	28Pin ZIP/SOJ	NOW
	KM424C257	256K×4	60/70/80	CMOS	E/F	28Pin ZIP/SOJ	NOW
	KM428C128	128K×8	60/70/80	CMOS	E/F	40Pin SOJ/TSOP-Ⅱ	NOW
2M	KM428C256	256K×8	60/70/80	CMOS	E/F	40Pin SOJ/TSOP-Ⅱ	NOW
	KM428V256	256K×8	70/80	CMOS	E/F(3.3V)	40Pin SOJ/TSOP-Ⅱ	NOW
	KM428C257	256K×8	60/70/80	CMOS	F/F	40Pin SOJ/TSOP-Ⅱ	NOW
	KM428C258	256K×8	60/70/80	CMOS	F/F	40Pin SOJ/TSOP-Ⅱ	NOW
4M	† KM4216C256	256K×16	60/70/80	CMOS	F/F	64Pin SSOP/TSOP-Ⅱ	2Q '94

* : New Product † : Under Development

2.4 Static RAM

Low power SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(μA)	
64K	KM6264BL/BL-L	8K x 8	70/100/120	CMOS	55	100/50	DIP/SDIP/SOP
256K	KM62256BL/BL-L	32K x 8	70/85/100/120	CMOS	70	100/20	DIP/SDIP/SOP/TSOP
	KM62256BLI/BLI-L	32K x 8	70/100	CMOS	70	100/20	DIP/SOP
	* KM62256CL/CL-L	32K x 8	55/70/85/100	CMOS	70	100/20	DIP/SDIP/SOP/TSOP
	* KM62256CLI/CLI-L	32K x 8	70/100	CMOS	70	100/20	SOP/TSOP
512K	KM68512L/L-L	64K x 8	70/85/100	CMOS	70	100/20	SOP/TSOP
	* KM68512AL/AL-L	64K x 8	55/70	CMOS	70	100/20	SOP/TSOP
1M	* KM681000BL/BL-L	128K x 8	55/70/85/100	CMOS	70	100/20	DIP/SOP/TSOP
	* KM681000BLI/BLI-L	128K x 8	70/100	CMOS	70	100/20	SOP/TSOP
4M	* KM684000L/L-L	512K x 8	55/70/85/100	CMOS	70	100/20	DIP/SOP/TSOP
	* KM684000LI/LI-L	512K x 8	70/85/100	CMOS	70	100/50	SOP/TSOP

Low Voltage SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(μA)	
256K	† KM62256CL-LV	32K x 8	70	CMOS	40	20/10	SOP/TSOP
1M	† KM68V1000BL/BL-L	128K x 8	70/100	CMOS	40	50/10	SOP/TSOP
4M	†† KM68V4000AL/AL-L	512K x 8	70/100/120	CMOS	70	50/10	SOP/TSOP
	†† KM616V4000AL/AL-L	256K x 16	70/100	CMOS	70	50/10	SOP/TSOP

Low Voltage SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(μA)	
1M	KM658128A/AL/AL-L	128K x 8	80/100/120	CMOS	70	100/20	DIP/SOP

* : New Product † : Preliminary Product †† : Under Development △ : Last Time by Product

High speed & Ultra High Speed SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(μA)	
64K	KM6465B	16K x 4	12/15/20/25	CMOS	140	1	22 SDIP
	KM6466B	16K x 4	12/15/20/25	CMOS	140	1	24 SDIP/SOJ
	KM6865B	8K x 8	12/15/20/25	CMOS	140	1	28 SDIP/SOJ
256K	△ KM64258B	64K x 4	15/20/25	CMOS	140	2	28 SDIP/SOJ
	KM64258C	64K X 4	12/15/20	CMOS	140	2	28 SOJ
	KM64V258C	64K x 4	15/17/20	CMOS	110	2	28 DIP/SOJ
	* KM64B261A	64K x 4	6/7/8	BiCMOS	160	20	28 SOJ
	* KM64B258A	64K x 4	8/10/12	BiCMOS	185	20	28 SOJ
	△ KM68257B	32K X 8	15/20/25	CMOS	150	2	28 DIP/SOJ
	KM68257C	32K X 8	12/15/20	CMOS	150	2	28 DIP/SOJ
	KM68V257C	32K X 8	15/17/20	CMOS	110	2	28 DIP/SOJ
	* KM68B261A	32K x 8	6/7/8	CMOS	170	20	32 SOJ
	* KM68B257A	32K x 8	8/10/12	CMOS	185	20	28 SOJ
	△ KM68V257	32K x 8	20/25/35	CMOS	90	0.1	28 DIP/SOJ
1M	△ KM611001	1M x 1	20/25/35	CMOS	130	2	28 DIP/SOJ
	KM641001	256K x 4	17/20/25/35	CMOS	150	2	28 SDIP/SOJ
	KM641003	256K x 4	15/17/20	CMOS	170	10	32 SOJ
	†† KM641003A	256K x 4	12/15/17/20	CMOS	185	3/0.2	32 SOJ/TSOP(II)
	†† KM64V1003A	256K x 4	12/15/17/20	CMOS	95	2/0.1	32 SOJ/TSOP(II)
	* KM64B1003	256K x 4	8/10/12/15	BiCMOS	165	10	32 SOJ
	KM681001	128K x 8	20/25/35	CMOS	170	2	32 SDIP/SOJ
	KM681002	128K x 8	15/17/20	CMOS	170	10	32 SOJ/TSOP(II)
	†† KM681002A	128K x 8	12/15/17/20	CMOS	185	3/0.2	32 SOJ/TSOP(II)
	†† KM68V1002A	128K x 8	12/15/17/20	CMOS	95	2/0.1	32 SOJ/TSOP(II)
	* KM68B1002	128K x 8	8/9/10/12/15	BiCMOS	175	10	32 SOJ/TSOP(II)
	KM6161002	64K x 16	15/17/20	CMOS	230	10	44 SOJ/TSOP(II)
	†† KM6161002A	64K x 16	12/15/20	CMOS	250	3/0.2	44 SOJ/TSOP(II)
	†† KM616V1002A	64K x 16	13/15/17/20	CMOS	170	2/0.1	44 SOJ/TSOP(II)
4M	KM644002/L	1M x 4	17/20/25	CMOS	170	10/0.5	32 SOJ
	† KM68B4002	1M x 4	10/12/15	BiCMOS	180	60/30	32 SOJ
	†† KM68BV4002	1M x 4	12/15/20	BiCMOS	170	60/30	32 SOJ
	KM684002/L	512k x 8	17/20/25	CMOS	160	10/0.5	36 SOJ
	† KM68B4002	512K x 8	10/12/15	BiCMOS	200	60/30	36 SOJ
	†† KM68BV4002	512K x 8	12/15/20	BiCMOS	180	60/30	36 SOJ
	KM6164002/L	256K x 16	20/25/35	CMOS	160	10/0.5	44 SOJ
	† KM616B4002	256K x 16	10/12/15	BiCMOS	240	60/30	44 SOJ/54 SOJ
	†† KM616BV4002	256K x 16	12/15/20	BiCMOS	200	60/30	44 SOJ/54 SOJ

* : New Product † : Preliminary Product †† : Under Development △ : Last Time by Product

Specialty SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(μA)	
288K	△ KM79C86	32K x 9	14/19/24	CMOS	190	50	44 PLCC
1M	KM741006	256K x 4	6.5/7/8	CMOS	190	40	46 SOJ
	† KM718B86	64K x 18	9/10/12	BiCMOS	280	80	52 PLCC
	† KM718B91	64K x 18	9/10/12	BiCMOS	280	80	52 PLCC
	† KM718BV87	64K x 18	9/10/12	BiCMOS	280	80	52 PLCC
	† KM718BV91	64K x 18	9/10/12	BiCMOS	280	80	52 PLCC

* : New Product † : Preliminary Product †† : Under Development △ : Last Time by Product

2.5. MASK ROM

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Package	Remark
256K	KM23C256(G)	32K x 8	120/150/200	CMOS	Programmable CE & OE	28DIP(32SOP)	NOW
512K	KM23C512(G)	64K x 8	120/150/200	CMOS	Programmable CE & OE	28DIP(32SOP)	NOW
1M	KM23C1000	128K x 8	120/150/200	CMOS	Programmable CE	28DIP	NOW
	KM23C1001	128K x 8	120/150/200	CMOS	Programmable OE	28DIP	NOW
	KM23C1010(G)	128K x 8	120/150/200	CMOS	Programmable CE & OE	32DIP(32SOP)	NOW
	KM23C1011(G)	128K x 8	120/150/200	CMOS	Programmable OE	32DIP(32SOP)	NOW
2M	KM23C2000A(G)	256K x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	NOW
	KM23C2001A(G)	256K x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	NOW
	KM23C2100A	256K x 8/ 128K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	NOW NOW
	†KM23C2000B(G)	256K x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	4Q.'94
	†KM23C2001B(G)	256K x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	4Q.'94
	†KM23C2100B	256K x 8/ 128K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	4Q.'94
4M	KM23C4000B(G)	512K x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	NOW
	KM23C4001B(G)	512K x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	NOW
	KM23C4100B(G)	512K x 8/ 256K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(40SOP)	NOW
	KM23C4200B	512K x 8/ 256K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	NOW
	†KM23C4000C(G)	512K x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	4Q.'94
	†KM23C4001C(G)	512K x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	4Q.'94
	†KM23C4100C(G)	512K x 8/ 256K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(40SOP)	4Q.'94
	†KM23C4200C	512K x 8/ 256K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	4Q.'94
	* KM23V4000B(G)	512K x 8	150/200/250	CMOS	3.3V Operation	32DIP(32SOP)	NOW
	* KM23V4001B(G)	512K x 8	150/200/250	CMOS	3.3V Operation	32DIP(32SOP)	NOW
	* KM23V4100B(G)	512K x 8/ 256K x 16	150/200/250	CMOS	3.3V Operation	40DIP(40SOP)	NOW
8M	KM23C8000B(G)	1M x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	NOW
	KM23C8001B(G)	1M x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	NOW
	KM23C8100B(G)	1M x 8/ 512K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	42DIP(44SOP)	NOW
	* KM23C8000C(G)	1M x 8	120/150/200	CMOS	Programmable CE & OE	32DIP(32SOP)	NOW
	* KM23C8001C(G)	1M x 8	120/150/200	CMOS	Programmable OE	32DIP(32SOP)	NOW
	* KM23C8100C(G)	1M x 8/ 512K x 16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	42DIP(44SOP)	NOW
	KM23C8105B(G)	1M x 8/ 512K x 16	100/120/150 (tP>50)	CMOS	4Word Page	42DIP(44SOP)	NOW
	* KM23V8000B(G)	1M x 8	200/250/300	CMOS	3.3V Operation	32DIP(32SOP)	NOW
	* KM23V8001B(G)	1M x 8	200/250/300	CMOS	3.3V Operation	32DIP(32SOP)	NOW
	* KM23V8100B(G)	1M x 8/ 512K x 16	200/250/300	CMOS	3.3V Operation	42DIP(44SOP)	NOW

MASK ROM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Package	Remark
16M	KM23C16101A KM23C16000A(G)	2M x 8 2M x 8/ 1M x 16	120/150/200 120/150/200	CMOS CMOS	Programmable OE Programmable CE & OE Word/Byte Mode	36DIP 42DIP(44SOP)	NOW NOW
	* KM23C16101B * KM23C16000B(G)	2M x 8 2M x 8/ 1M x 16	120/150/200 120/150/200	CMOS CMOS	Programmable OE Programmable CE & OE Word/Byte Mode	36DIP 42DIP(44SOP)	NOW NOW
	KM23C16005A(G)	2M x 8/ 1M x 16	120/150/200 (tP > 50)	CMOS	8Word Page	42DIP(44SOP)	NOW
	* KM23V16101A * KM23V16000A(G)	2M x 8 2M x 8/ 1M x 16	200/250/300 200/250/300	CMOS CMOS	3.3V Operation 3.3V Operation	36DIP 42DIP(44SOP)	NOW NOW
32M	KM23C32110 KM23C32000 KM23C32000G	4M x 8 2M x 16 4M x 8/ 2M x 16	150/200/250 150/200/250 150/200/250	CMOS CMOS CMOS	Programmable CE & OE Programmable CE & OE Programmable CE & OE	42DIP 42DIP(44SOP) 42DIP(44SOP)	NOW NOW NOW
	† KM23C32101A † KM23C32110A † KM23C32000A † KM23C32000AG	4M x 8 4M x 8 2M x 16 4M x 8/ 2M x 16	120/150/200 120/150/200 120/150/200 120/150/200	CMOS CMOS CMOS CMOS	Programmable OE Programmable CE & OE Programmable CE & OE Programmable CE & OE Word/Byte Mode	36DIP 42DIP 42DIP 44SOP	4Q.'94 4Q.'94 4Q.'94 4Q.'94
	KM23C32005 KM23C32005G	2M x 16 4M x 8/ 2M x 16	150/200/250 150/200/250	CMOS CMOS	8Word Page 8word Page	42DIP 44SOP	NOW NOW
	† KM23C32005AG	4M x 8/ 2M x 16	100/120/150 (tP > 30)	CMOS	8Word Page	44SOP	1Q.'95
	† KM23C32205ASG	2M x 16 1M x 32	100/120/150 (tP > 30)	CMOS	8word Page	70SSOP	2Q.'95
64M	† KM23C64000G	8M x 8/ 4M x 16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	44SOP	3Q.95
	KM23C64200SG	4M x 16/ 2M x 32	120/150/200	CMOS	Programmable CE & OE	70SSOP	3Q.'95

* : New Product
† : Under Development

2.6 EEPROM/FLASH

Density	Part Number	Organization	Speed(ns)	Technology	Features	Package	Remark
1K bit	KM93C46/G/GD/I	64×16	1MHz	CMOS	Self-timed	8DIP/8SOP	Now
	KM93C46V/VG/VGD/I	64×16	250KHz	CMOS	3.0V-Operation	8DIP/8SOP	Now
2K bit	KM93C56/G/GD/I	128×16	1MHz	CMOS	Auto Erase, Self-timed	8DIP/8SOP	Now
	KM93C57/G/GD/I	128×16/256×8	1MHz	CMOS	Select Organization	8DIP/8SOP	3Q,94
	KM93C56V/VG/VGD/I	128×16	1MHz	CMOS	3.0V Operation	8DIP/8SOP	Now
	KM93C57V/VG/VGD/I	128×16/256×8	1MHz	CMOS	3.0V Operation	8DIP/8SOP	Now
4K bit	KM93C66/G/GD/I	256×16	1MHz	CMOS	Auto Erase, Self-timed	8DIP/8SOP	Now
	KM93C67/G/GD/I	256×16/512×8	1MHz	CMOS	Select Organization	8DIP/8SOP	3Q,94
	KM93C66V/VG/VGD/I	256×16	1MHz	CMOS	3.0V Operation	8DIP/8SOP	Now
	KM93C67V/VG/VGD/I	256×16/512×8	1MHz	CMOS	3.0V Operation	8DIP/8SOP	Now
64K bit	KM28C64A/AJ	8K×8	120/150/200	CMOS	64B Page Mode, D-P, T-B	28DIP/32PLCC	Now
	KM28C64AI/AJI	8K×8	120/150/200	CMOS	Industrial	28DIP/32PLCC	Now
	KM28C65A/AJ	8K×8	120/150/200	CMOS	64B Page Mode, D-P, T-B R-B	28DIP/32PLCC	Now
	KM28C65AI/AJI	8K×8	120/150/200	CMOS	Industrial	28DIP/32PLCC	Now
	KM28C64B/BJ	8K×8	90/120/150	CMOS	64B Page Mode, D-P, T-B	28DIP/32PLCC	3Q,94
	KM28C64BII/BJI	8K×8	90/120/150	CMOS	Industrial	28DIP/32PLCC	3Q,94
	KM28C65B/BJ	8K×8	90/120/150	CMOS	64B Page Mode, D-P, T-B, R-B	28DIP/32PLCC	3Q,94
	KM28C65BI/BJI	8K×8	90/120/150	CMOS	Industrial	28DIP/32PLCC	3Q,94
1M bit	KM29C010/J/T	128K×8	100/120/150	CMOS	128B Page Mode, D-P, T-B	32DIP/32PLCC	Now
16M bit	KM29N16000T/TS	2M×8	t_R = 15 μs	CMOS	256B Page Mode	44(40)TSOP	3Q.94
	KM29N16000R/RS		t_{RC} = 80ns		4K Block Erase		
32M bit	KM29N32000T/TS	4M×8	t_R = 10 μs	CMOS	512B Page Mode	44(40)TSOP	2Q.94
	KM29N32000R/RS		t_{RC} = 50ns		8K Block Erase		

* D-P : Data-Polling, R/B : Ready/Busy, T-B : Toggle Bit

2.7 DRAM Card

Card Style	Vcc	Density	Part No.	Organization	Speed(ns)	PKG	Features
JEIDA/JEDEC	5.0V	2M Byte	KMCJ532512	512Kx32/1Mx16	60/70/80	88 Pin Two Piece	• Fast Page Mode Operation • Low Power Consumption • $\overline{RAS}$ only and Hidden Refresh • $\overline{CAS}$ before $\overline{RAS}$ Refresh
			KMCJ536512	512Kx36/1Mx18	60/70/80	88 Pin Two Piece	
		4M Byte	KMCJ5321000	1Mx32/2Mx16	60/70/80	88 Pin Two Piece	
			KMCJ5361000	1Mx36/2Mx18	60/70/80	88 Pin Two Piece	
		8M Byte	KMCJ5322000	2Mx32/4Mx16	60/70/80	88 Pin Two Piece	
			KMCJ5362000	2Mx36/4Mx18	60/70/80	88 Pin Two Piece	
		16M Byte	KMCJ5324000	4Mx32/8Mx16	60/70/80	88 Pin Two Piece	
			KMCJ5324100	4Mx32/8Mx16	60/70/80	88 Pin Two Piece	
			KMCJ5364100	4Mx36/8Mx18	60/70/80	88 Pin Two Piece	
	3.3V	2M Byte	KMCV532512	512Kx32/1Mx16	60/70/80	88 Pin Two Piece	
		4M Byte	KMCV5321000	1Mx32/2Mx16	60/70/80	88 Pin Two Piece	
		8M Byte	KMCV5322000	2Mx32/4Mx16	60/70/80	88 Pin Two Piece	
		16M Byte	KMCV5324000	4Mx32/8Mx16	60/70/80	88 Pin Two Piece	
			KMCV5324100	4Mx32/8Mx16	60/70/80	88 Pin Two Piece	

SRAM Card

Card Style	Vcc	Capacity	Part No.	Organization	Speed(ns)	PKG	Features
PCMCIA/JEIDA Standard	5.0V	512K Byte	KMCJ616256	256Kx16/512Kx8	150/200/250	68 Pin Two Piece	• 8KByte Attri bute Memory • Replaceable & Rechargeable Battery • High Speed : 150ns
		1M Byte	KMCJ616512	512Kx16/1Mx8	150/200/250	68 Pin Two Piece	
		2M Byte	KMCJ6161000	1Mx16/2Mx8	150/200/250	68 Pin Two Piece	

3. CROSS REFERENCE GUIDE

3.1 Video RAM

Density	Feature	Organization	Samsung	Micron	Toshiba	NEC	Hitachi	Ti
256K	Minimum	64K×4	KM424C64	MT42C4064		μPD41264 μPD42264	HM53461(2)	TMS4461
512K	Minimum	64K×8	KM428C64					
1M	Minimum	256K×4	KM424C256 KM424C256A		TC524256 TC524256A TC524256B TC524257	μPD42273	HM534251 HM534251A HM534252	TMS44C250 SMJ44C250
		128K×8			TC528126A TC528126B		HM538121 HM538121A	TMS48C121
	Extended	256K×4	KM424C257	MT42C4256 MT42C4255	TC524258A TC524258B TC524259B	μPD42274	HM534253A	TMS44C251 SMJ44C251 SMJ44C251A
		128K×8	KM428C128	MT42C8128 MT42C8128	TC528128A TC528128B TC528129B	μPD42275	HM538123A	
2M	Extended	256K×8	KM428C256	MT42C8255				
	Full	256K×8	KM428C257 KM428C258	MT42C8256 MT42C8254	TC528267	μPD482234 μPD482235	HM538253	
4M	Full	256K×32	KM4216C256	MT42C256K16A1				

3.2 Static RAM

Low power SRAM

Den.	Org.	SAMSUNG	HITACHI	SONY	TOSHIBA	MITSUBISHI	NEC
64K	8K x 8	KM6264BL/BL-L	HM6264A/AL/AL-L	CXK5864B-L/B-LL	TC6565AL/AL-L	M5M5165/L	μPD4364L/L-L
256K	32K x 8	KM62256CL/CL-L	HM62256AL/AL-L	CXK58257A-L/A-LL	TC55257BL/BL-L	M5M5255B-L/B-LL	μPD43256B/BL
512K	64K x 8	KM68512AL/AL-L					
1M	128K x 8	KM681000BL/BL-L	HM628128AL/AL-L	CXK581000/L	TC551001AL-AL-L	M5M51008/L	μPD431000AL/ALL
4M	512K x 8	KM628512	HM628512/L/L-L	CXK584000(1)-L	TC554002	M5M54008L/LL	μPD434000/L/LL

Low power SRAM

Den.	Org.	SAMSUNG	HITACHI	TSOHIBA	NEC	OKI	MOTOROLA
1M	128K x 8	KM658128A/AL/AL-L	HM658128A/AL/AL-L	TC518129A/AL/AL-L	μPD428128A/AL/AL-L	MSM548128	MCM518128

High Speed SRAM

Den.	Org.	Samsung	Hitachi	Cypress	Fujitsu	Micron	IDT	Motorola	Toshiba	sony
64K	16K x 4	KM6465B	HM6288	CY7C164A	MB81C74	MT5C6404	IDT7188	MCM6288C	TC55416	CXK5466
	16Kx4(With OE)	KM6466B	HM6289	CY7C166A	MB81C75	MT5C6405	IDT6198		TC55417	CXK5465
	8K X 8	KM6865B		CY7C186A	MB81C78	MT5C6408	IDT7164	MCM6264C	TC5588	CXK5863
256K	64K X 4(5V)	KM64458C	HM67909A	CY7C196	MB81C84A	MT5C2565	IDT61298SA	MCM629C	TC55464A	
	64K X 4(3.3V)	KM64B258C				MT5LC2565				
	32K X 8(5V)	KM68257C	HM62832H	CY7C199		MT5C2568	IDT71256SA	MCM6206D	TC55328A	CXK58258B
	32K x 8(3.3V)	KM68V257C				MT5LC2568	IDT713256	MCM62V06D	TC55V328	
1M	1M x 1(E)	KM11001		CY7C1007		MT5C1001	IDT71281	MCM6227B		
	256K x 4(E)	KM641001	HM624256A	CY7C1006		MT5C1005	IDT71028	MCM6229A		CXK541000
	256K x 4(R)	KM641003	HM674256UH			MT5C256K4A1				
	128K x 8(E)	KM681001	HM6268127H	CY7C1009	MB82008	MT5C1008	IDT71024	MCM6226B		CXK541020
	128K x 8(R)	KM681002				MT5C128K8A1				
	64K x 16(R)	KM6161002		CY7C108		MT5C64K16A1			TC551664	
4M	1M x 4	KM644002	HM624100		MB82201	MT5C1M4B2			TC551402	
	512K x 8	KM684002				MT5C512K8B2				
	256K x 16	KM6164002				MT5C256KX16				

BiCMOS SRAM

Den.	Org.	Samsmung	Hitachi	NEC	Toshiba	Motorola	IDT
256K	64K x 4(With OE)-R	KM64B261A				MCM6709R	
	64K x 4(with-OE)-E	KM64B258A	HM6709SH		TC55B465	MCM6709A	IDT61B298
	32K x 8-R	KM68B261A		μPD46258		MCM6706R	
	32K x 8-E	KM68B257A	HM6783SH		TC55B328	MCM6706A	IDT71256
1M	256K x 4(With OE)-R	KM64B1003			TC55B4257	MCM6729A	
	128K x 8-R	KM68B1002			TC55B8128	MCM6726A	IDT71B024

Specialty SRAM

Den.	Org.	SMAMSUNG	Motorola	Micron	Cypress	ICW
1M	256K x 4	KM741006	MCM67Q804			
	64K x 18	KM718B86	MCM67B618		CY7C1031	ICW73B596
		KM718B90		MT58LC64K18M1		
		KM718BV87	MCM67H618	MT58LC64K18B2		
		KM718BV90		MT58LC64K18M1		

3.3 MASK ROM

DTY	Samsung	NEC	Hitachi	Toshiba	Sharp	Mitsubishi	Fujitsu	Sony
256K	KM23C256		HN623257P HN623258P		LH23255 LH53259	M5M23256P	MB83256	CXK38256
512K	KM23C512			TC53512C	LH53514 LH53515		MB83512	
1M	KM23C1000	uPD23C1000A	HN62321P HN62321BP HN62331P	TC531000C	LH231000B LH531000A	M5M23C100 M5M231000	MB831000 MB831124	CXK381000P
	KM23C1001	uPD23C1010A	HN62321EP HN62331EP			M5M231001		
	KM23C1010	uPD23C1001E	HN62321A	TC531001C	LH231100B			
		uPD23C1000E	HN62331A		LH530800			
	KM23C1011	uPD23C100EA			LH530900			
2M	KM23C2000A	uPD23C2001	HN62302B	TC532000A	LH532300 LH532100B		MB832000 MB832001	CXK382001
	KM23C2001A				LH532200B LH532400			
	KM23C2100A	uPD23C2000	HN62412P		LH532000B			
		uPD23C2000A	HN62422P		LH532500			
4M	KM23C4000B	uPD23C4001E	HN62335 HN62344B	TC534000A	LH534100B	M5M23C401AP	MB834000A	CXK384001
	KM23C4000C		HN62335 HN62344B				MB834000AL	
	KM23V4001B		HN62W335B					
	KM23C4001B				LH534300 LH534400			
	KM23C4001C				LH534300 LH534400			
	KM23C4100B	uPD23C4000	HN62404P	TC534200	LH534000B	M5M23C400AP	MB834100A	
		uPD23C4000A	HN62414P HN62424P HN62444P		LH534500'		MB834200A	
	KM23C4100C	uPD23C4000	HN62404P		LH534000B		MB834100AL	
		uPD23C4000A	HN62414P HN62424P HN62444P		LH534500			
	KM23V4100B KM23C4200B KM23C4200C		HNW15					

3.3 MASK ROM (Continued)

DTY	Samsung	NEC	Hitachi	Toshiba	Sharp	Mitsubishi	Fujitsu	Sony
8M	KM23C8000B	uPD23C8001E	HN62318B	TC538000A	LH538100 LH538200	M5M23801P	MB838000	CXK388000
	KM23C8000C	uPD23C8001E	HN62318B		LH538100 LH538200	M5M23801P	MB838000	
	KM23V8000B		HN62W328B					
	KM23C8001B							
	KM23C8001C							
	KM23V8001B							
	KM23C8100B	uPD23C8000	HN62418P	TC538200A	LH538000	M5M23800P	MB838200	
	KM23C8100C	uPD23C8000	HN62428P	TC538200A	LH538000	M5M23800P		
	KM23C8105B							
	KM23V8100B						MB838200L	
16M	KM23C16101A							
	KM23C16101B							
	KM23V16101A							
	KM23C16000A	uPD23C16000	HN624316P	TC5316200A	LH53160000	M5M23160P	MB831620P	
	KM23C16000B	uPD23C16000	HN624316P	TC5316200A	LH53160000	M5M23160P	MB831620P	
	KM23C16005A					M5M23168P		
	KM23V16000A		HN62W4116					
32M	KM23C32000	uPD23C32000			LH5332000			
	KM23C32000A	uPD23C32000			LH5332000			
	KM23C32005							
	KM23C32005A							
	KM23C32205A							

3.4 EEPROM

***Serial I/O EEPROM**

Density	Samsung	N. S	Exar	Micro Chip	SGSThomson	Catalyat	Rohm	Atmel
1K	KM93C46	NM9346	XRM93C46A	93C46	ST93C46T	CAT93C46A	BR93C46	AT93C46
	KM93C46V	NM93C46L						
2K	KM93C56	NM93C56A	XRM93C56A				BR93C56A	AT93C56
	KM93C57			93C56	ST93C56	CAT36C102		
	KM93C56V	NM93C56L					BR93C56B	
	KM93C57V							
4K	KM93C66	NM93C66	XRM93C66B				BR93C66A	AT93C66
	KM93C67			93C66		CAT35C104		
	KM93C66V	NM93C66L					BR93C66B	
	KM93C67V					CAT33T104		

***Parallel EEPROM**

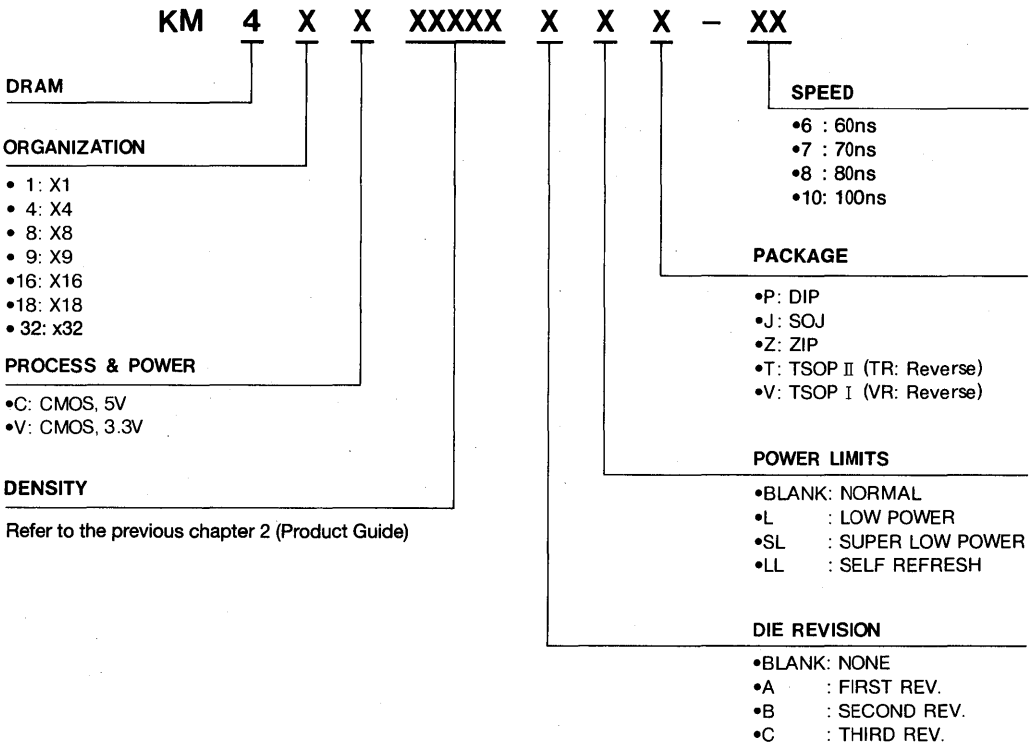
Density	Samsung	Xicor	Seeq	Exel	Atmel	Hitachi	Oki	Catalyat
64K	KM28C64A	X2864A/B X28C64	DQ28C64	XL2864 XL28C64A	AT28C64	HN58064	MSM28C64A	CAT28C65A
	KM28C65A		DQ28C65 DQ2864	XL2865 XL28C65A		HN58C65/66		CAT28C65A
	KM28C64B	X2864A/B X28C64	DQ28C64	XL2864 XL28C64A	AT28C64	HN58064	MSM28C64A	CAT28C65A
	KM28C65B		DQ28C65 DQ2864	XL2865 XL28C65A		HN58C65/66		CAT28C65A

3.5 Flash

Density	Samsung	Toshiba	Seeq	Exel	Atmel	Hitachi	Oki	Catalyat
1M	KM29C010				AT29C010			
16M	KM29N16000	TC5816FT/TR						
32M	KM29N32000	TC5832FT/TR						

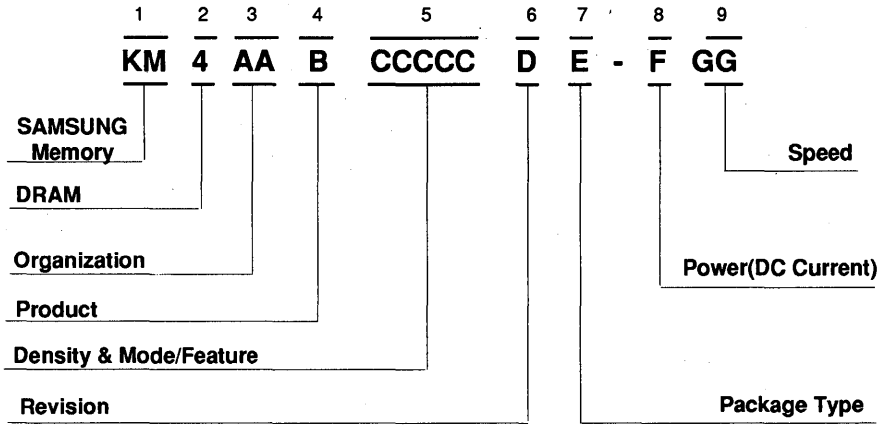
4. ORDERING INFORMATION

4.1 DRAM



* NEW DRAM ORDERING SYSTEM

This new DRAM ordering system will be used for all SAMSUNG's DRAM products in '95.
In '94 DRAM Databook, only used for 16M Byte Word Wide 2nd Gen. and 64M DRAM.



1. SAMSUNG Memory

2. DRAM(4)

3. Organization

1	x 1
4	x 4
8	x 8
9	x 9
16	x 16
18	x 18
32	x 32

4. Product

C	5V
V	3.3V

5. Density & Mode/Feature (Same)

6. Revision

Blank	1st Gen.
A	2nd Gen.
B	3rd Gen.
C	4th Gen.

7. Package Type

J	SOJ
T	TSOP II (Forward)
R	TSOP II (Reverse)
V	TSOP I (Forward)
U	TSOP I (Reverse)
K	SOJ(Shrinked PKG,SOJ)
S	TSOP II (Shrinked PKG,Forward)
W	TSOP II (Shrinked PKG,Reverse)

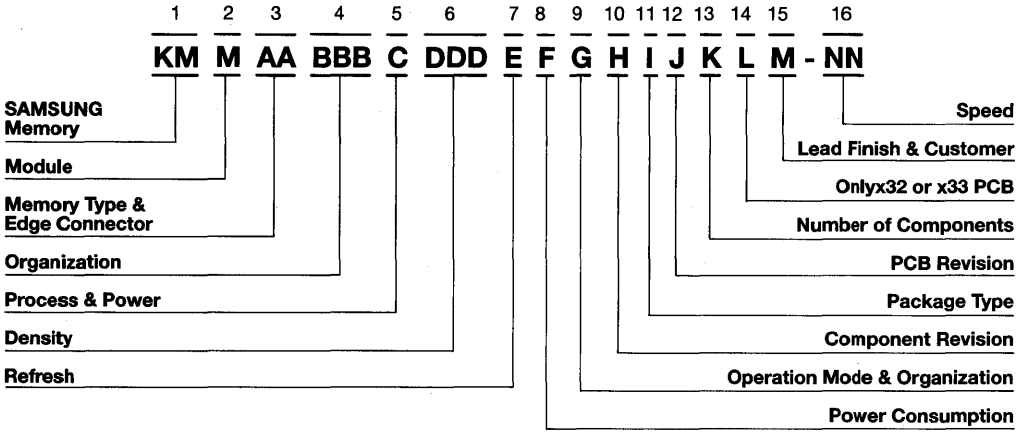
8. Power(DC Current)

Blank	Normal
L	Low power
H	Super Low power
F	Self Refresh with L.P

9 . Speed

-5	50 ns
-6	60 ns
-7	70 ns
-8	80 ns

4.2 DRAM Module



1. SAMSUNG Memory
2. Module
3. Memory Type & Edge Connector
-1 ····· FLASH
-2 ····· Mask ROM
-3 ····· DRAM DIMM
-4 ····· DRAM SIP
-5 ····· DRAM SIMM
-6 ····· SRAM
-7 ····· Pseudo SRAM
-8 ····· ASSP
-9 ····· VRAM

4. Organization
-8/9 ····· x8/x9 bit wide
-18 ····· x18 bit wide
-32/33 ····· x32/x33
-36/40 ····· x36/x39/x40
-64/66 ····· x64/x66
-72/80 ····· x72/x80
-144 ····· x144 bit wide

5. Process & Operation Voltage
-Blank ····· CMOS 5V
-V ····· CMOS 3.3V
-S ····· Sync 3.3V

6. Density
-16 ····· 16M
-8 ····· 8M
-4 ····· 4M
-2 ····· 2M
-1 ····· 2M
-512 ····· 512K
-256 ····· 256K

7. Refresh (16M DRAM Based)
-0 ····· 4K
-1 ····· 2K
-2 ····· 1K

8. Power Consumption
-0 ····· Normal
-2 ····· Low Power
-4 ····· Super Low Power
-6 ····· Self Refresh

9. Operation Mode & Organization
-0 ····· F/P
-1 ····· Nibble
-2 ····· Static Column
-3 ····· Using Quad CAS
-4 ····· Using EDO
-5 ····· Using EDO & Quad CAS
-8 ····· Using Non Memory Logic
-9 ····· Using Non Memory Logic & Quad CAS

10. Component Revision
-Blank ····· None
-A ····· First Rev.
-B ····· Second Rev.
-C ····· Third Rev.

11. Package Type
-Blank ····· SOJ or PLCC
-T ····· TSOP

12. PCB Revision
-Blank ····· None
-1 ····· First Rev.
-2 ····· Second Rev.
-3 ····· Third Rev.

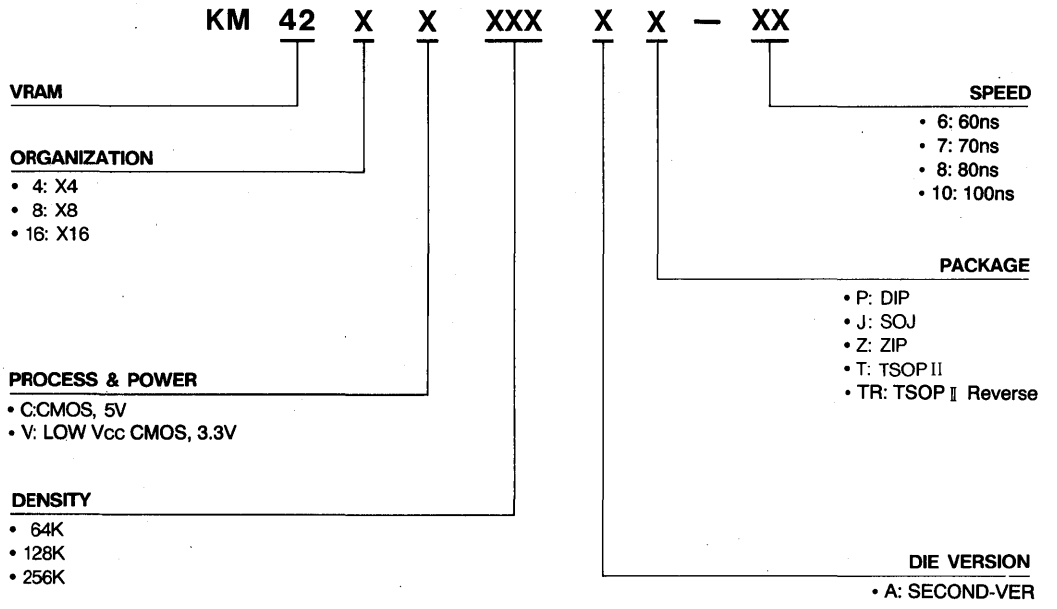
13. Number of Components
-Blank ····· more than 7 chip
-N ····· less than 8 chip
-U ····· Byte Wide Base
-W ····· Word Wide Base

14. Only x32 or x33 PCB
-V ····· x32 or x33 PCB

15. Lead Finish & Customer
-Blank ····· Solder
-G ····· Gold
-D ····· DEC
-H ····· HP
-M ····· IBM
-P ····· Nickel
-Q ····· Compaq
-X ····· Cambex

16. Speed
-5 ····· 50ns
-6 ····· 60ns
-7 ····· 70ns
-8 ····· 80ns

4.3 VRAM


KM 42 X X XXX X X – XX
VRAM
ORGANIZATION
• 4: X4
• 8: X8
• 16: X16
PROCESS & POWER
• C:CMOS, 5V
• V: LOW Vcc CMOS, 3.3V
DENSITY
• 64K
• 128K
• 256K
SPEED
• 6: 60ns
• 7: 70ns
• 8: 80ns
• 10: 100ns
PACKAGE
• P: DIP
• J: SOJ
• Z: ZIP
• T: TSOP II
• TR: TSOP II Reverse
DIE VERSION
• A: SECOND-VER

4.4 Static RAM

KM XX X X X XXXX X X X X-XX X X

MEMORY COMPONENT

DEVICE TYPE

- 6: SRAM(Async.)
- 65: Pseudo SRAM
- 7: SRAM(ASSP)

ORGANIZATION

- 1: ×1bit
- 4: ×4bits
- 2 or 8: ×8bits
- 9: ×9bits
- 16: ×16bits

TECHNOLOGY

- BLANK: CMOS
- B: BiCMOS

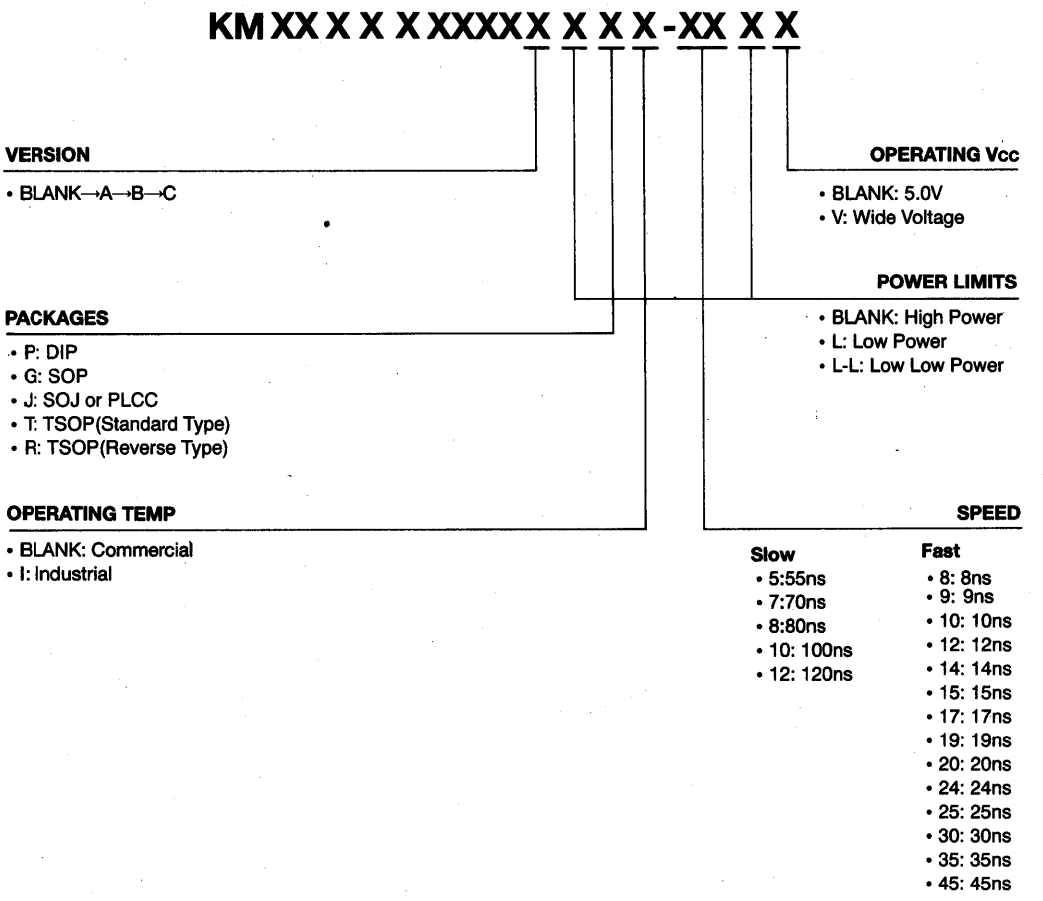
OPERATING Vcc

- BLANK: 5.0V
- V: 3.0 or 3.3V

DENSITY & OPTION

- 64: 64K Slow
- 65: 64K Fast
- 66: 64K Fast(with OE)
- 256: 256K Slow
- 257: 256K Fast
- 258: 256K Fast(with OE)
- 512: 512K Slow
- 513: 512K Fast
- 1000: 1M Slow
- 1001: 1M Fast
- 1002: 1M Fast(Revolutionary)
- 1003: 1M Fast(Revolutionary, with OE)
- 1005: 1M Fast(Sep.I/O)
- 1006: 1M Fast(Sync.,Sep.I/O)
- 86 : 1M Sync. linear Burst, No Glue
- 87 : 1M Sync. linear Burst, Glue
- 90 : 1M Sync. Interleave Burst, No Glue
- 4000: 4M Slow
- 4002: 4M Fast(Revolutionary)
- 8128: 128K×8 Pseudo SRAM
- 8512: 512K×8 Pseudo SRAM

4.4 Static RAM



4.5 MASK ROM

KM 23 X XXX XX X X XX - XX

MEMORY

DEVICE TYPE

- 23 : MASK ROM

PROCESS & POWER

- C : CMOS, 5V
- V : CMOS, 3.3V

DENSITY

- 256 : 256K
- 512 : 512K
- 1 : 1M
- 2 : 2M
- 4 : 4M
- 8 : 8M
- 16 : 16M
- 32 : 32M
- 64 : 64M

ORGANIZATION

- 00 : x 8 bit (1M 28DIP, 2M, 4M, 8M)
  x 16 bit (16M, 32M, 64M)
- 01 : x 8 bit (1M 32Pin)
- 10 : x 8 bit (16M, 32M, 64M)
  x 16 bit (2M, 4M, 8M)
- 11 : x 8 bit (32M 42DIP)
- 20 : x 16 bit & EPROM TYPE PIN OUT (4M)
  x 32 bit (16M, 32M, 64M)

TYPE & MODE

- 0 : COMMERCAL
- 1 : Multi OE
- 5 : PAGE MODE

VERSION

- BLANK→A→B→C

PKG

- BLANK : DIP
- G : SOP
- SG : SSOP

SPEED

- 10 : 100ns
- 12 : 120ns
- 15 : 150ns
- 20 : 200ns

* Internal KF · CODE Inforamtion

KF X X XX X

MASK ROM

DENSITY

- 3 : 256K
- Z : 512K
- 4 : 1M
- Y : 2M
- 5 : 4M
- X : 8M
- 6 : 16M
- W : 32M

PRODUCTION LINE

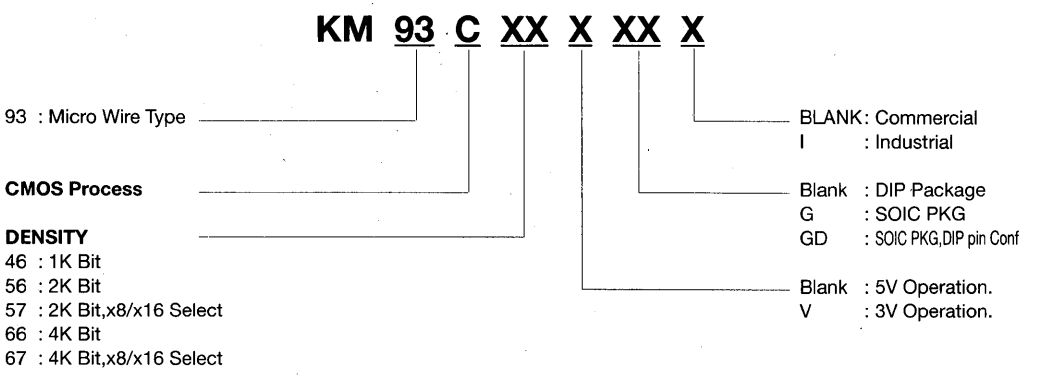
- 1 : LINE 1
- 2 : LINE 2
- 3 : LINE 3

SERIAL NO.

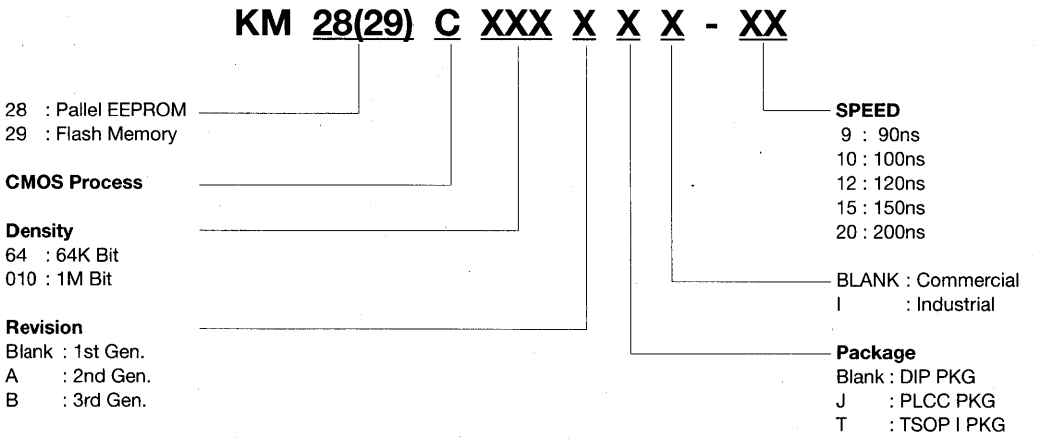
Intermal Ver. NO.

4.6 EEPROM

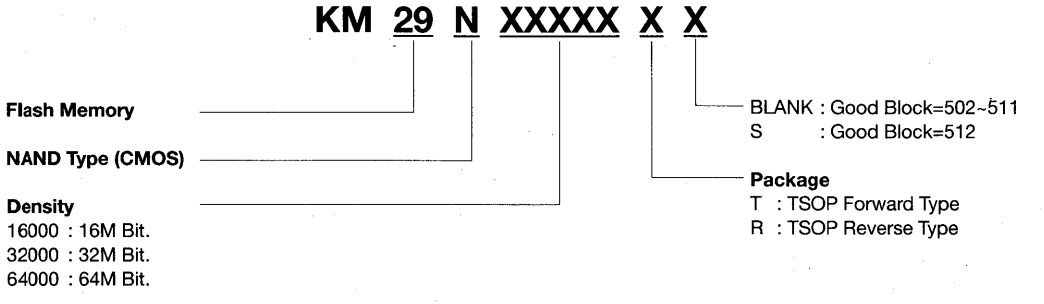
***Serial EEPROM**



***Parallel EEPROM**



4.7 Flash



4.8 Memory Card

KM C W W WW XXXX YYY - ZZ

SAMSUNG MEMORY

CARD

CARD STYLE

- J : PCMCIA/JEIDA/JEDEC STYLE(5.0V)
- V : PCMCIA/JEIDA/JEDEC STYLE(3.3V)

MEMORY TYPE

- 5 : DRAM Card
- 6 : SRAM Card

MEMORY DATA WIDTH

- 8 : 8Bit • 16 :16Bit • 18 :18Bit
- 16 : 16Bit • 32 : 32Bit • 36 : 36Bit

DENSITY & MODE/FEATURE

- DRAM Card
  - 4100 : 4M Bit F. Page, 2K refresh
  - 4000 : 4M Bit F. Page, 4K refresh
  - 2000 : 2M Bit F. Page, 1K refresh
  - 1000 : 1M Bit F. Page, 1K refresh
  - 512 : 512K Bit F. Page, 1K refresh
- SRAM Card
  - 1000 : 1M BIT
  - 512 : 512K BIT
  - 256 : 256K BIT

DIE(COMPONENT) REVISION

- BLANK : NONE
- A : FIRST REV.
- B : SECOND REV.
- C : THIRD REV.

COMPONENT COMPOSITION

- BLANK : ×41×1 BASE
- W : BYTE-WORD WIDE BASE

CUSTOMER CODE

SPEED

- 06 : 60ns • 15 : 150ns
- 07 : 70ns • 20 : 200ns
- 08 : 80ns • 25 : 250ns

NOTES

1M DRAM DATA SHEET 2

1M x 1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM41C1000C/CL/CSL-6	60ns	15ns	110ns
KM41C1000C/CL/CSL-7	70ns	20ns	130ns
KM41C1000C/CL/CSL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible input and output**
- **Single 5V±10% power supply**
- **Refresh Cycle**
  - **512 cycle/8ms refresh (Normal)**
  - **512 cycle/64ms refresh (L-version)**
  - **512 cycle/128ms refresh (SL-version)**
- **Power Dissipation**
  - **Standby : 5.5mW (Normal)**
    1.1mW (L-version)
    0.55mW (SL-version)
  - **Active(60/70/80ms) : 385/358/330mW**
- **256K x 4 fast test mode**
- **JEDEC standard pinout**
- **Available in plastic DIP, SOJ, ZIP, TSOP(I), TSOP(II) and PLCC Packages**

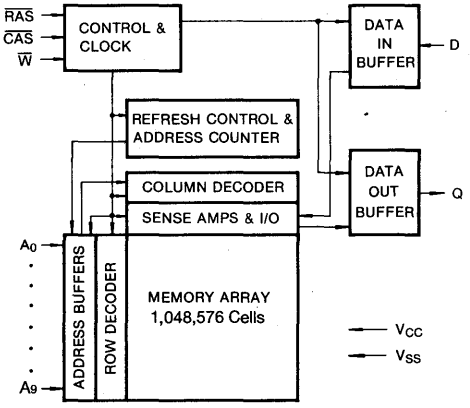
GENERAL DESCRIPTION

The Samsung KM41C1000C/CL/CSL is a CMOS high speed 1,048,576 x 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance microprocessor computers.

The KM41C1000C/CL/CSL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

The KM41C1000C/CL/CSL is fabricated using Samsung's advanced CMOS process.

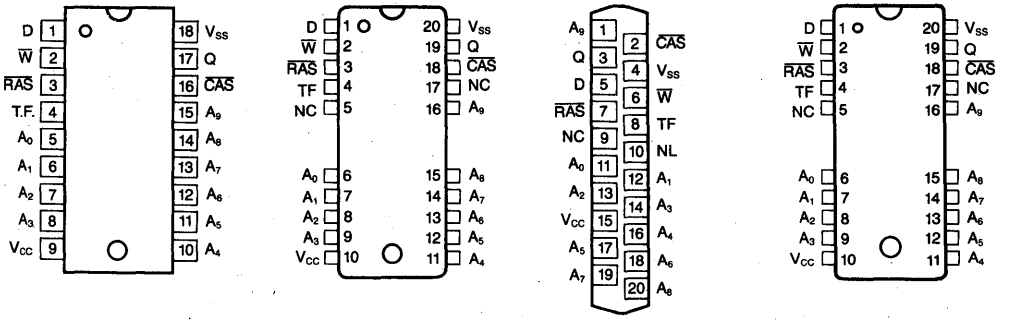
FUNCTIONAL BLOCK DIAGRAM



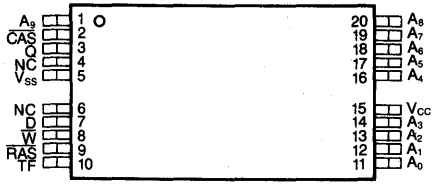
SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top Views)

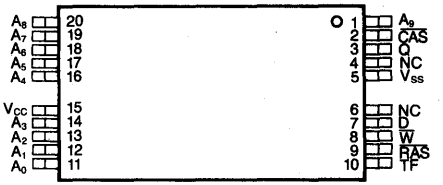
• KM41C1000CP/CLP/CSLP • KM41C1000CJ/CLJ/CSLJ • KM41C1000CZ/CLZ/CSLZ • KM41C1000CT/CLT/CSLT



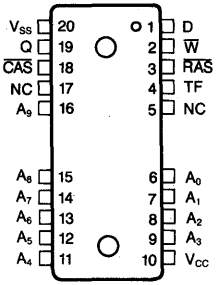
• KM41C1000CV/CLV/CSLV



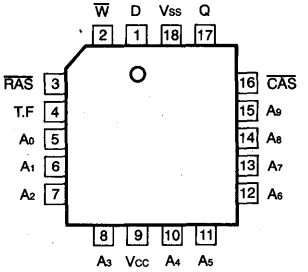
• KM41C1000CVR/CLVR/CSLVR



• KM41C1000CTR/CLTR/CSLTR



• KM41C1000CG/CLG/CSLG



Pin Names	Pin Function
A_0-A_9	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
TF	Test Function
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection
NL	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V_{DD}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	Vcc +1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$, Address Cycling @t_{RC}=min.)	KM41C1000C/CL/CSL-6	I_{CC1}	-	70	mA
	KM41C1000C/CL/CSL-7		-	65	mA
	KM41C1000C/CL/CSL-8		-	60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM41C1000C/CL/CSL-6	I_{CC3}	-	70	mA
	KM41C1000C/CL/CSL-7		-	65	mA
	KM41C1000C/CL/CSL-8		-	60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM41C1000C/CL/CSL-6	I_{CC4}	-	55	mA
	KM41C1000C/CL/CSL-7		-	50	mA
	KM41C1000C/CL/CSL-8		-	45	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)	KM41C1000C	I_{CC5}	-	1	mA
	KM41C1000CL		-	200	μA
	KM41C1000CSL		-	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM41C1000C/CL/CSL-6	I_{CC6}	-	70	mA
	KM41C1000C/CL/CSL-7		-	65	mA
	KM41C1000C/CL/CSL-8		-	60	mA
Battery Back Up Current Average Power Supply Current, Battery back up Mode ($\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V, W=Vcc-0.2V or 0.2V, A0~A9= Vcc-0.2V or 0.2V, D_{IN}=Vcc-0.2V, 0.2V or OPEN : t_{RC}=250μS, t_{RAS}=t_{RAS} min.~1μS)	KM41C1000CL	I_{CC7}	-	200	μA
	KM41C1000CSL			100	μA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤Vcc)		$I_{O(L)}$	-10	10	μA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}, I_{CC4}, Address can be changed maximum once during a Fast Page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	-	5	pF
Input Capacitance (A_0~A_9)	C_{IN2}	-	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	-	7	pF
Output Capacitance (Q)	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	130		150		170		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

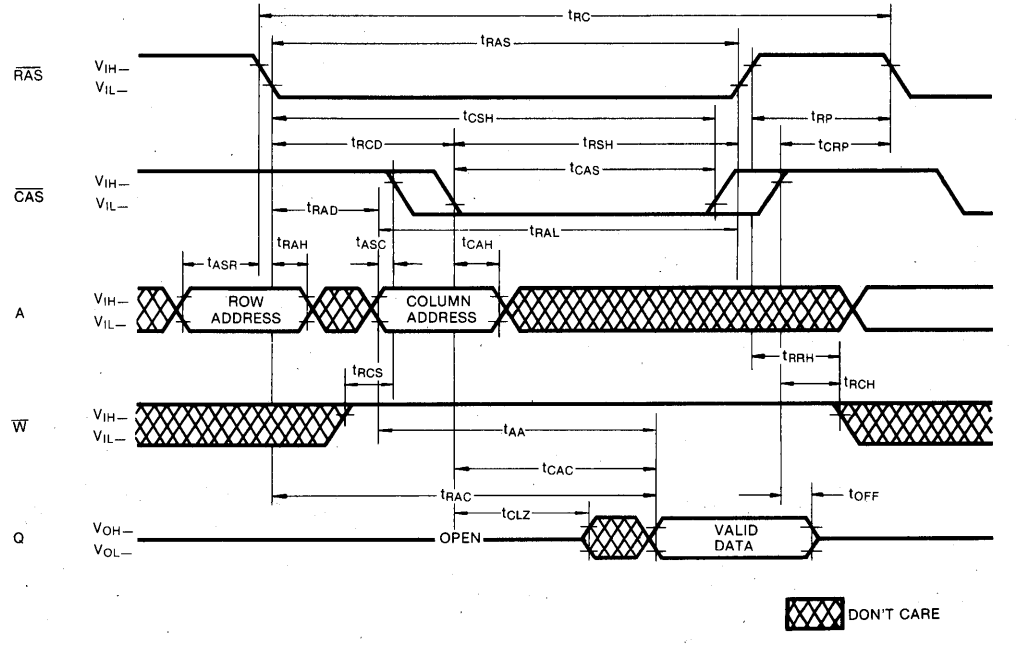
Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		ns	
Data-in set-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	50		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh period (Low power)	tREF		64		64		64	ms	
Refresh period (Super Low power)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	60		70		80		ns	8
Column address to $\overline{W}$ delay time	tAWD	30		35		40		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	15		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		35		40	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	60		60		65		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	tRASP	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page mode)	tCP	10		10		10		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
12. Normal operation requires the "T.F" pin to be connected to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
13. When the "T.F" pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung for specific operational details of the "test function."
14. In a test mode read cycle, the value of t_{RAC}, t_{CAC}, t_{AA} is delayed for 3ns.

TIMING DIAGRAMS

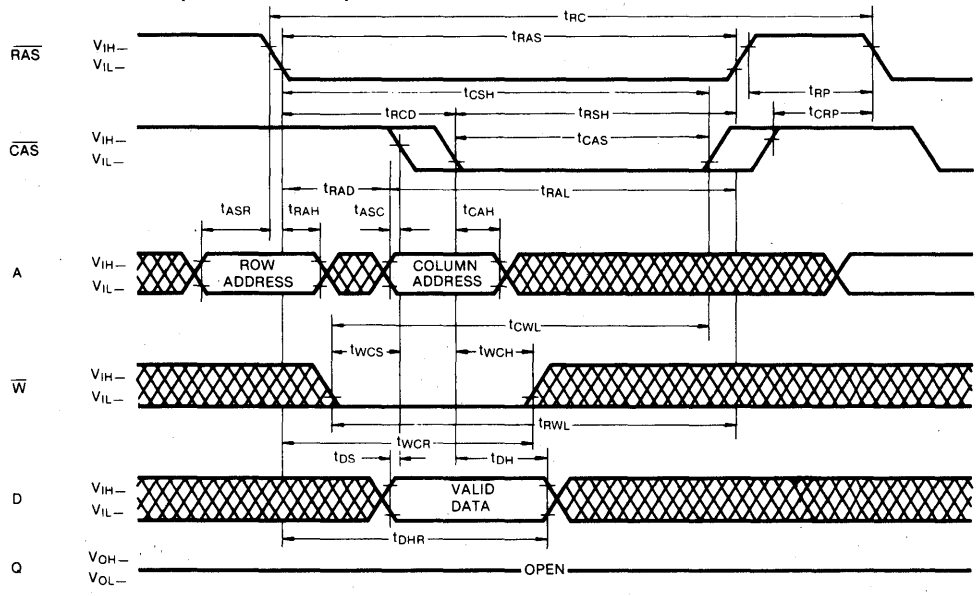
READ CYCLE



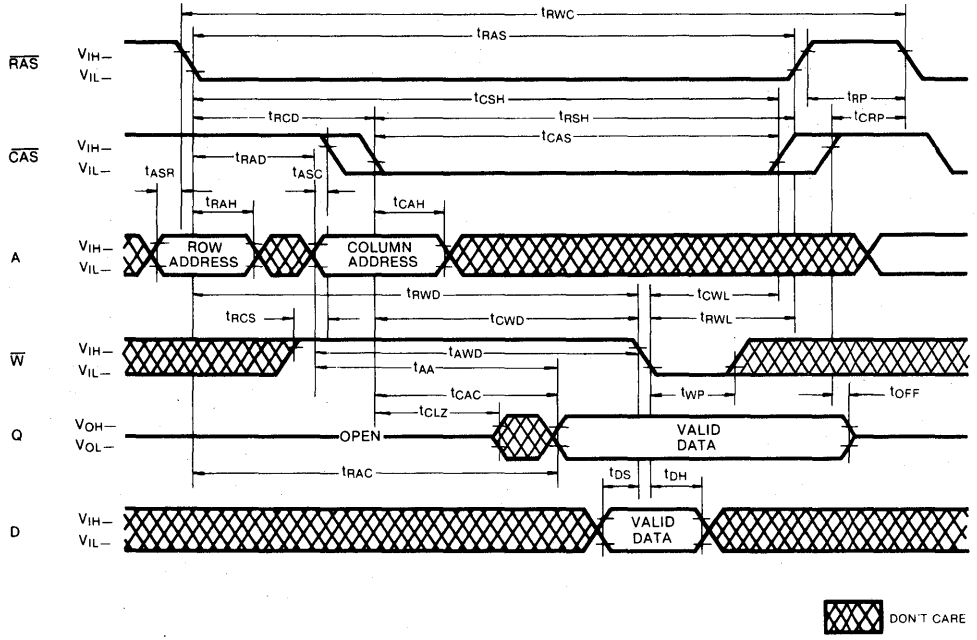
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

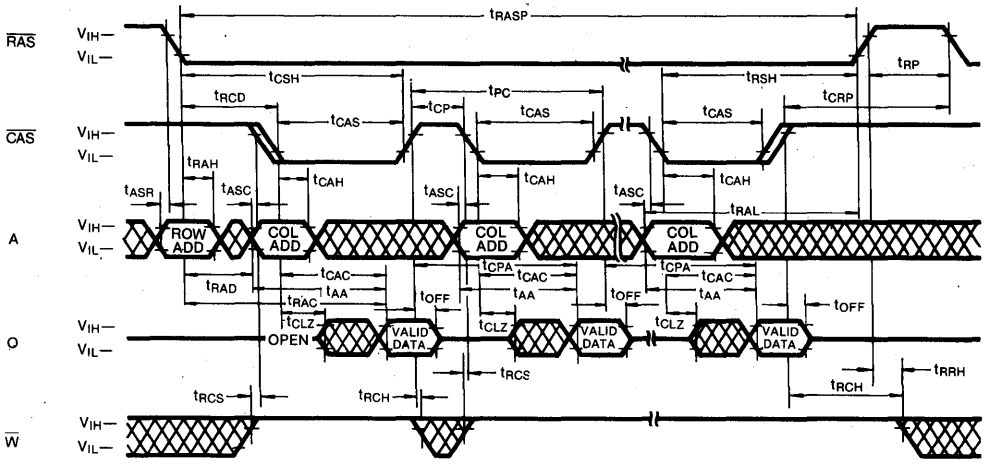


READ-WRITE/READ-MODIFY-WRITE CYCLE

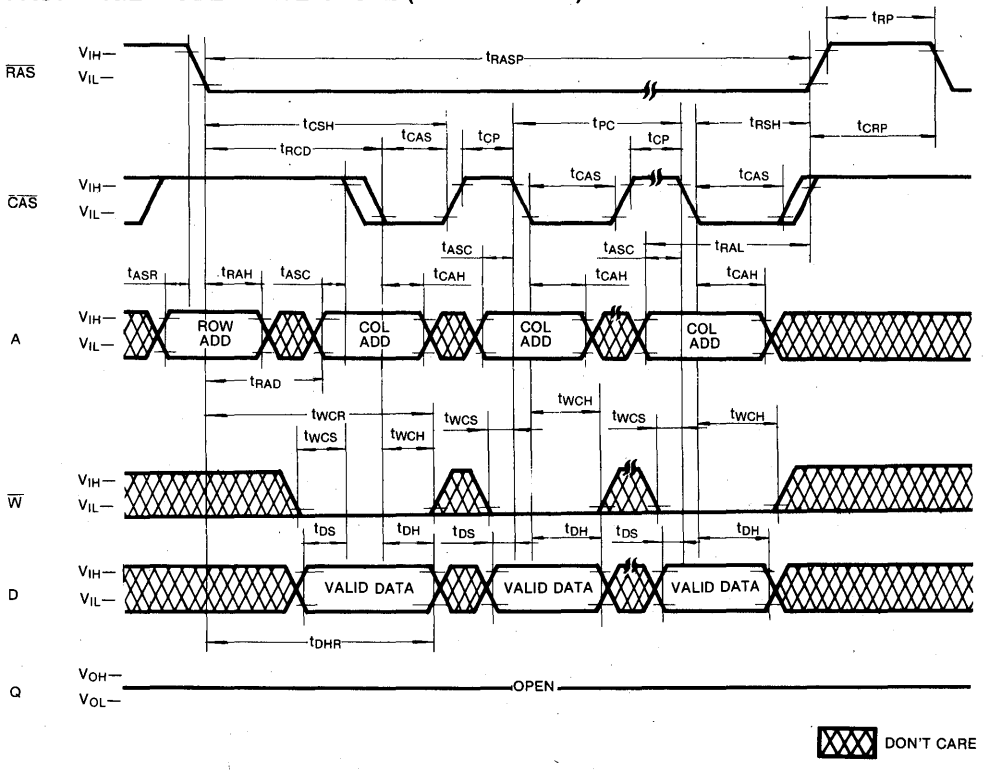


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE

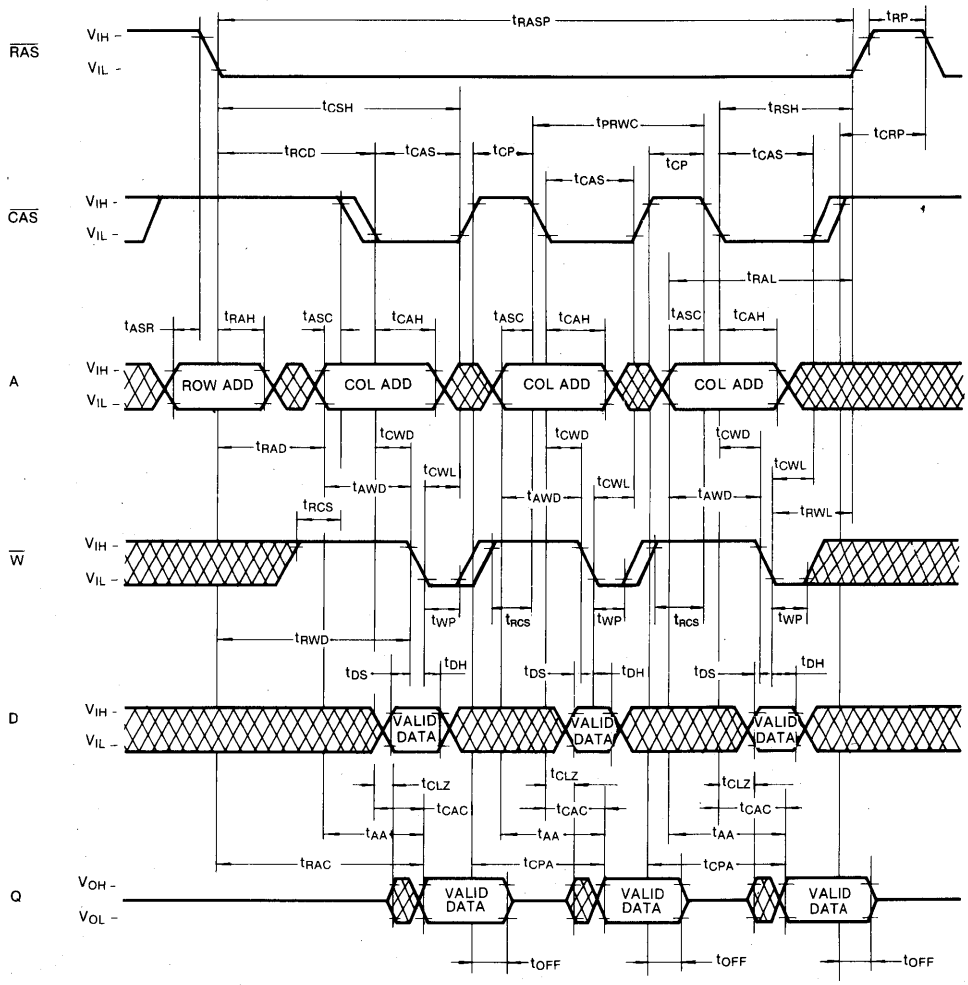


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

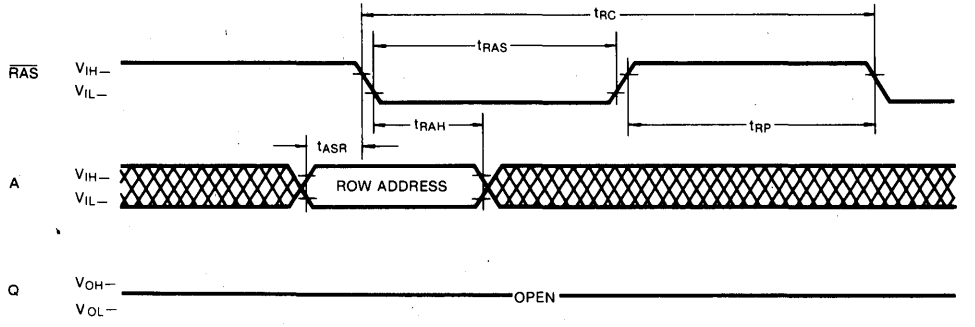
FAST PAGE MODE READ-WRITE CYCLE



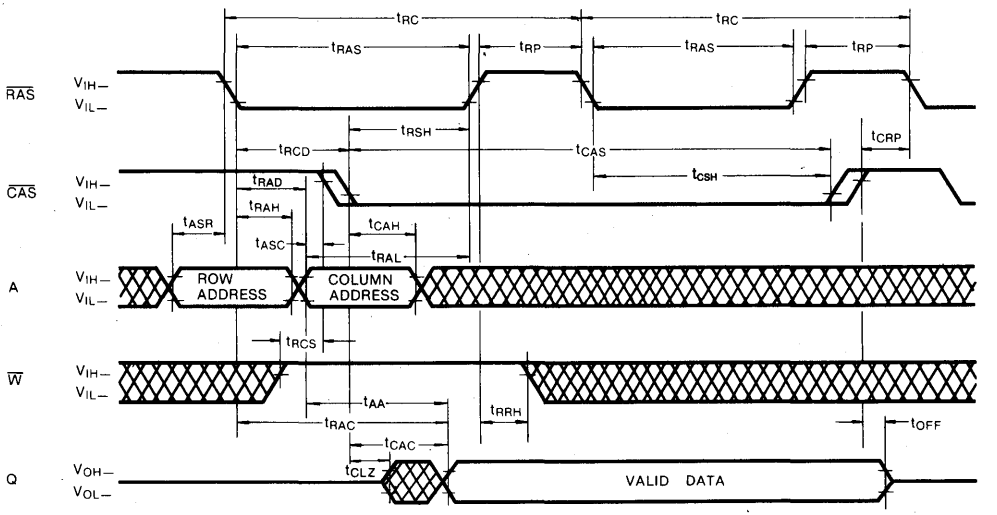
TIMING DIAGRAMS (Continued)

RAS-ONLY REFRESH CYCLE

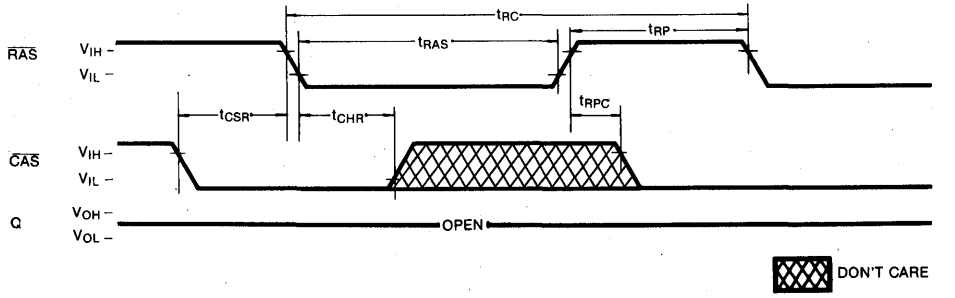
Note: $\overline{CAS} = V_{IH}$, $\overline{W}$,D, A_9 = Don't Care



HIDDEN REFRESH CYCLE

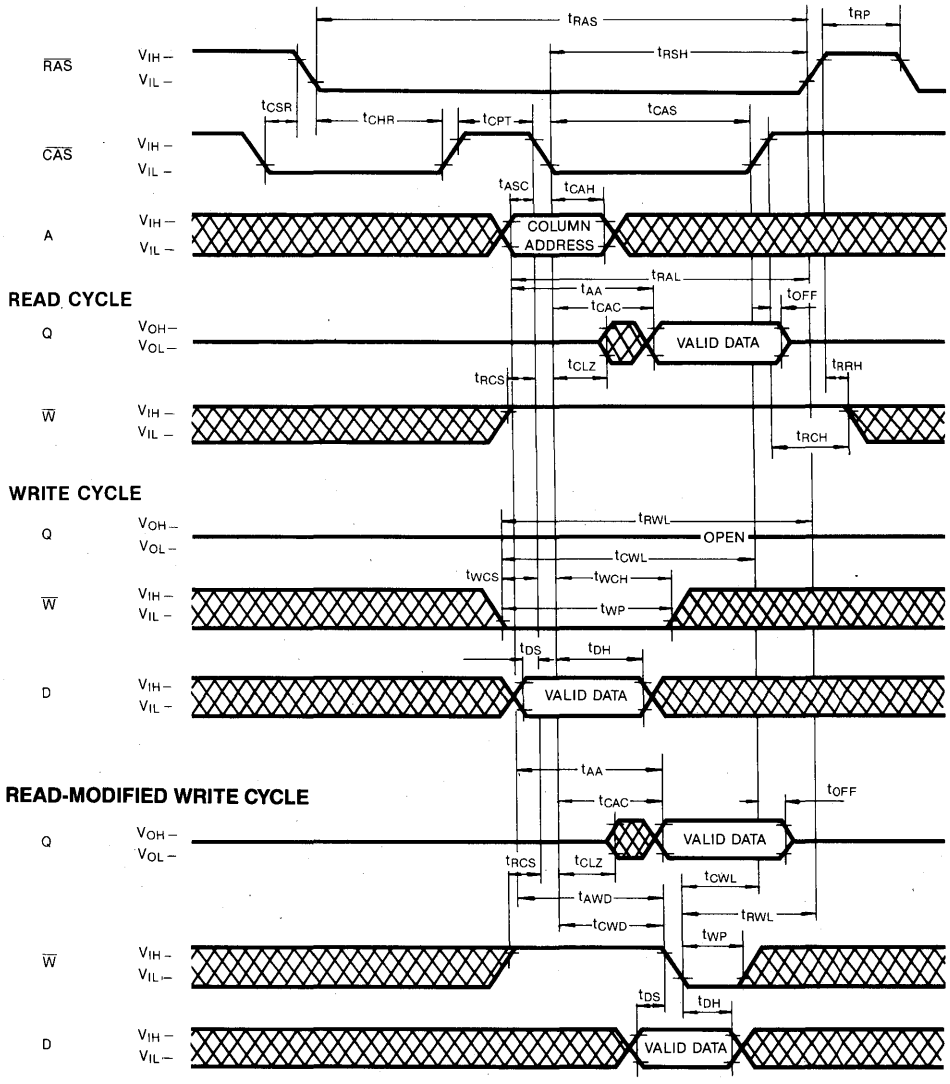


CAS-BEFORE-RAS REFRESH CYCLE



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DON'T CARE

DEVICE OPERATION

The KM41C1000C/CL/CSL contains 1,048,576 memory locations. Twenty address bits are required to address a particular memory location. Since the KM41C1000C/CL/CSL has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column adress strobe($\overline{CAS}$), and the valid row and column address inputs.

Operation of the KM41C1000C/CL/CSL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C1000C/CL/CSL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C1000C/CL/CSL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max), then the access time to valid data is specified by t_{RAC}(min). However if $\overline{CAS}$ goes low after t_{RCD}(max), or if the column address becomes valid after t_{RAD}(max.), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM41C1000C/CL/CSL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur, The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C1000C/CL/CSL has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high(V_{IH}), the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C1000C/CL/CSL operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$ only cycle.

Indeterminate Output State: Delayed Write.

Refresh

The data in the KM41C1000C/CL/CSL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16/64/128 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A_0~A_8). The state of address A_9 is ignored during refresh.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C1000C/CL/CSL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C1000C/CL/CSL hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C1000C/CL/CSL by using read, write or read-modify write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the low address bits A_0 through A_8 are supplied by the on-chip refresh counter. The A_9 bit is set low internally.

Fast Page Mode

The KM41C1000C/CL/CSL has Fast page mode capability which provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time requried to set up and strobe sequential row addresses for the same page

Power-up

If $\overline{RAS}$=V_{SS} during power-up, the KM41C1000C/CL/CSL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current. An initial pause of 200 μ sec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C1000C/CL/CSL inputs act like unteminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used,series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C1000C/CL/CSL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

DEVICE OPERATION (Continued)

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV.

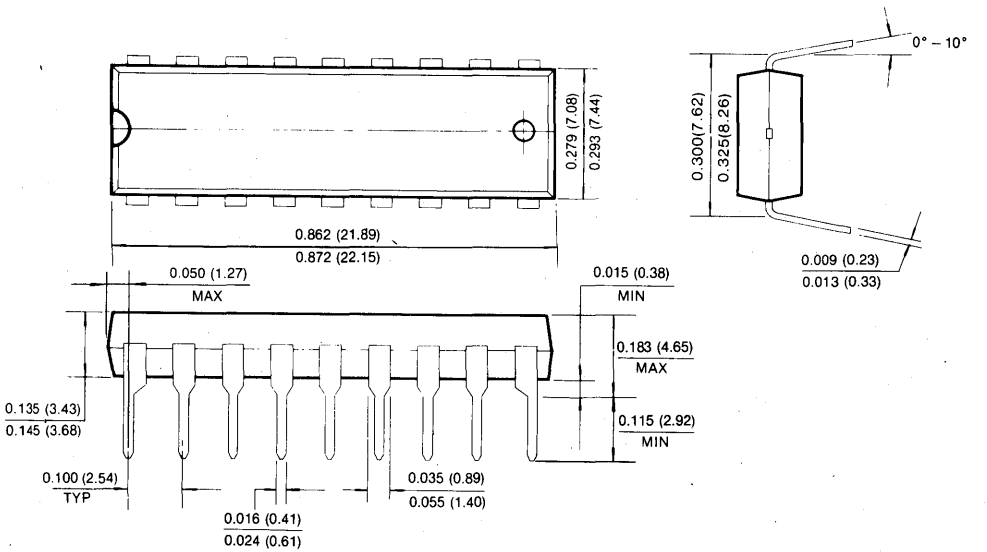
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM41C1000C/CL/CSL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C1000C/CL/CSL and they supply much of the current used by the KM41C1000C/CL/CSL during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (Millimeters)

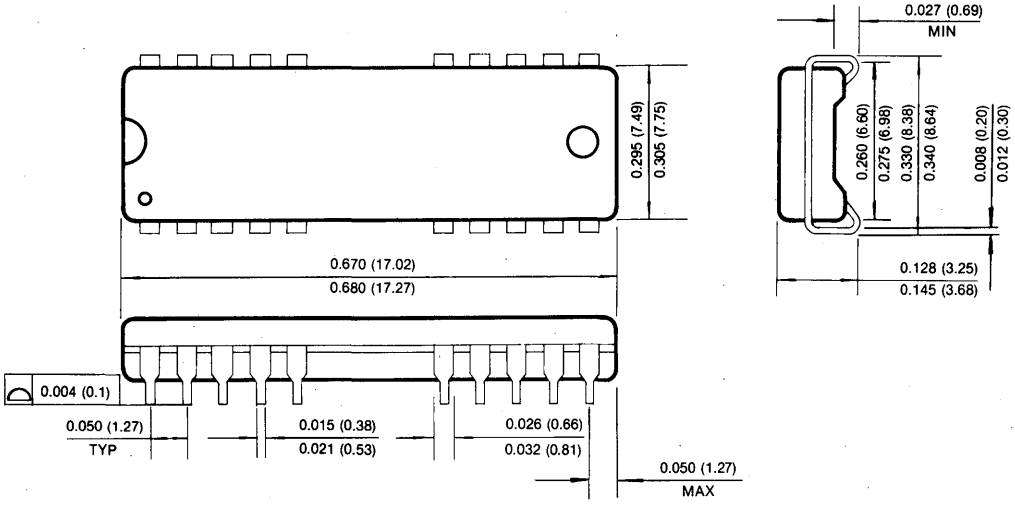


SAMSUNG ELECTRONICS

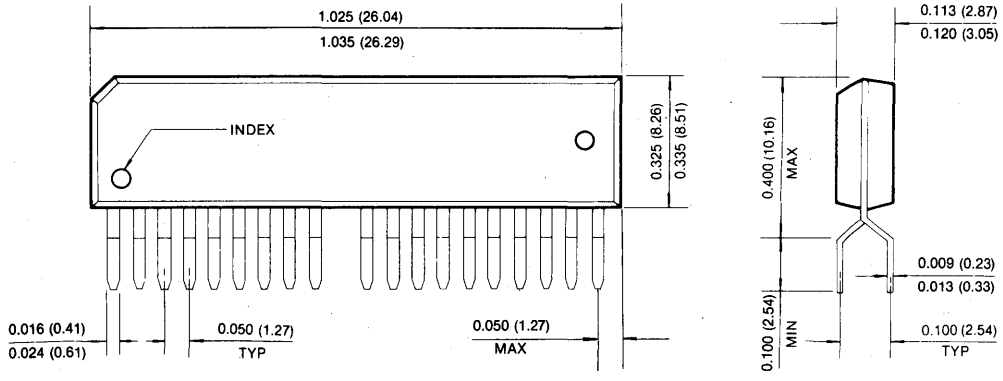
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



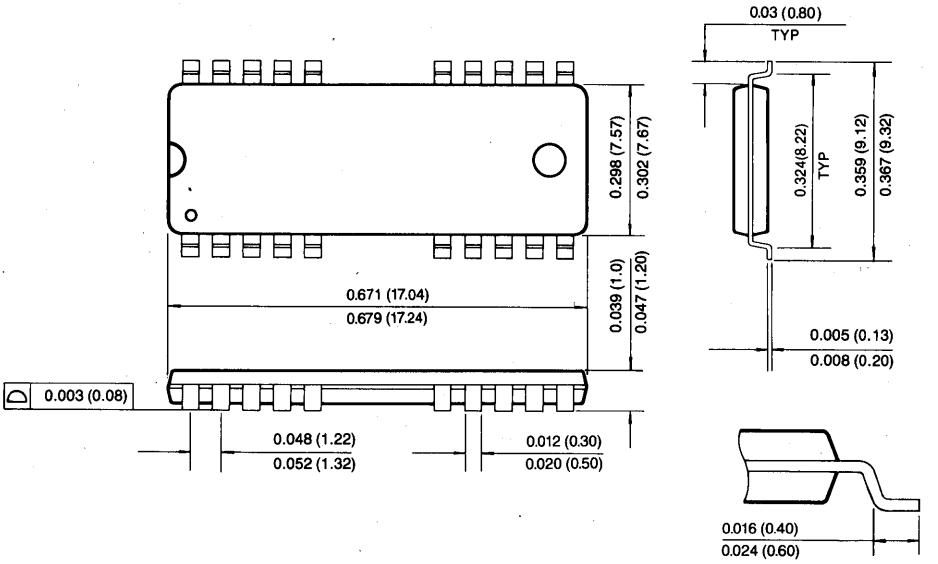
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



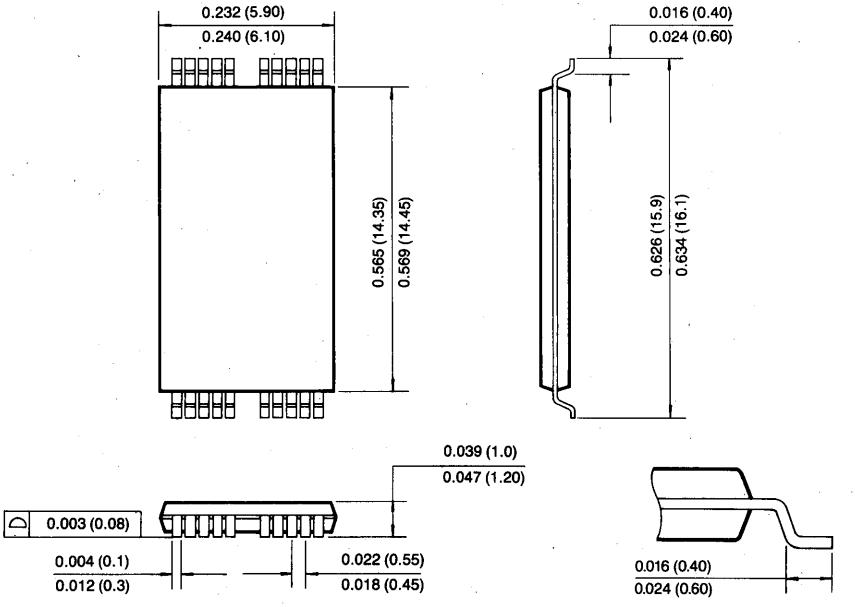
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



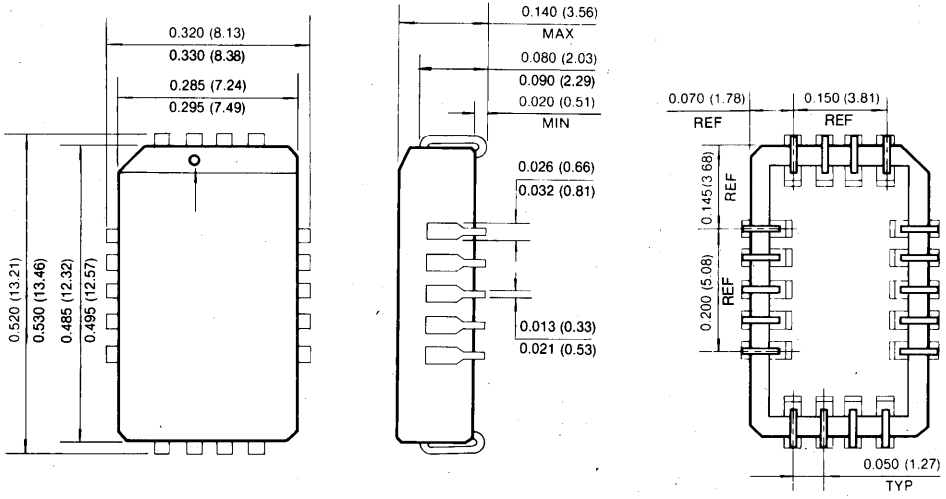
20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)



SAMSUNG ELECTRONICS

PACKAGE DIMENSIONS (Continued)

18- LEAD PLASTIC CHIP CARRIER



256K x 4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM44C256C/CL/CSL-6	60ns	15ns	110ns
KM44C256C/CL/CSL-7	70ns	20ns	130ns
KM44C256C/CL/CSL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or Output Enable Controlled Write**
- **Single 5V±10% power supply**
- **Refresh Cycle**
  - **— 512 cycle/8ms refresh (Normal)**
  - **— 512 cycle/64ms refresh (L-version)**
  - **— 512 cycle/128ms refresh (SL-version)**
- **Power Dissipation**
  - **—Standby : 5.5mW (Normal)**
    1.1mW (L-version)
    0.55mW (SL-version)
  - **— Active(60/70/80ms) : 385/360/330mW**
- **JEDEC standard pinout**
- **Available in plastic DIP, SOJ, ZIP, TSOP(I), and TSOP(II) Packages**

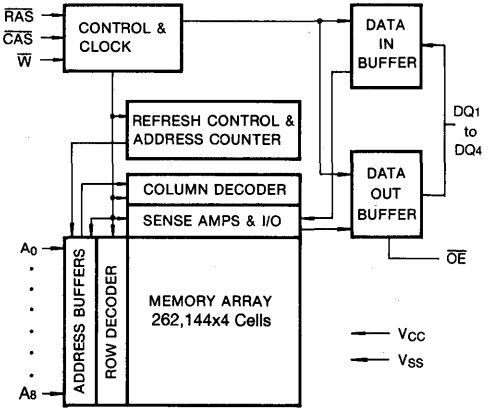
GENERAL DESCRIPTION

The Samsung KM44C256C/CL/CSL is a CMOS high speed 262,144 x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance microprocessor computers.

The KM44C256C/CL/CSL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C256C/CL/CSL is fabricated using Samsung's advanced CMOS process.

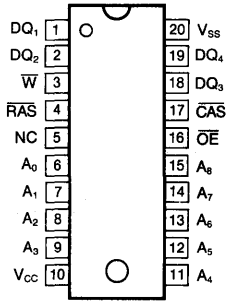
FUNCTIONAL BLOCK DIAGRAM



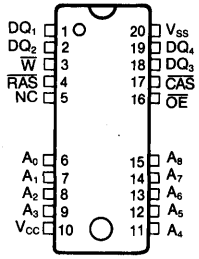
SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top Views)

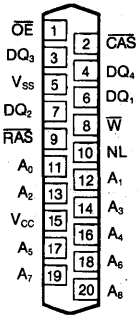
• KM44C256CP/CLP/CSLP



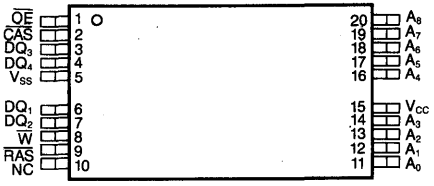
• KM44C256CJ/CLJ/CSLJ



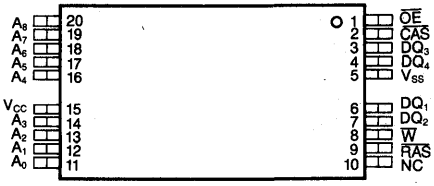
• KM44C256CZ/CLZ/CSLZ



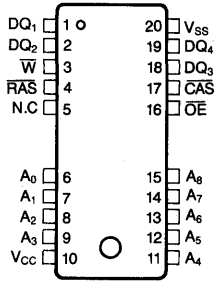
• KM44C256CV/CLV/CSLV



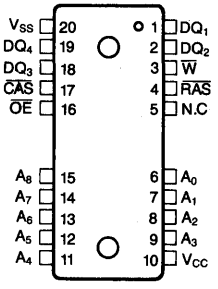
• KM44C256CVR/CLVR/CSLVR



• KM44C256CT/CLT/CSLT



• KM44C256CTR/CLTR/CSLTR



Pin Names	Pin Function
A_0-A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1-DQ_4	Data In/Data Out
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection
NL	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{DD}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$, Address Cycling @t_{RC}=min.)	KM44C256C/CL/CSL-6	I_{CC1}	-	70	mA
	KM44C256C/CL/CSL-7		-	65	mA
	KM44C256C/CL/CSL-8		-	60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM44C256C/CL/CSL-6	I_{CC3}	-	70	mA
	KM44C256C/CL/CSL-7		-	65	mA
	KM44C256C/CL/CSL-8		-	60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44C256C/CL/CSL-6	I_{CC4}	-	55	mA
	KM44C256C/CL/CSL-7		-	50	mA
	KM44C256C/CL/CSL-8		-	45	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM44C256C	I_{CC5}	-	1	mA
	KM44C256CL		-	200	μA
	KM44C256CSL		-	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C256C/CL/CSL-6	I_{CC6}	-	70	mA
	KM44C256C/CL/CSL-7		-	65	mA
	KM44C256C/CL/CSL-8		-	60	mA
Battery Back Up Current Average Power Supply Current, Battery back up Mode ($\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V, $\overline{W}$=V_{CC}-0.2V or o.2V, A_0~A_9= V_{CC}-0.2V or o.2V, D_{IN}=V_{CC}-0.2V, o.2V or OPEN : t_{RC}=250μS, t_{RAS}=t_{RAS} min.~1μS)	KM44C256CL	I_{CC7}	-	200	μA
	KM44C256CSL		-	100	μA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}, I_{CC4}, Address can be changed maximum once during a Fast Page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_8)	C_{IN1}	-	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		175		195		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		55		60		ns	6
Write command pulse width	t_{WP}	15		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (Normal)	t_{REF}		8		8		8	ms	
Refresh period (Low power)	t_{REF}		64		64		64	ms	
Refresh period (Super Low power)	t_{REF}		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		45		45		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		95		105		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	15		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		35		40	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	80		85		90		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20		20	ns	
$\overline{OE}$ command hold time	t_{OEH}	15		20		20		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

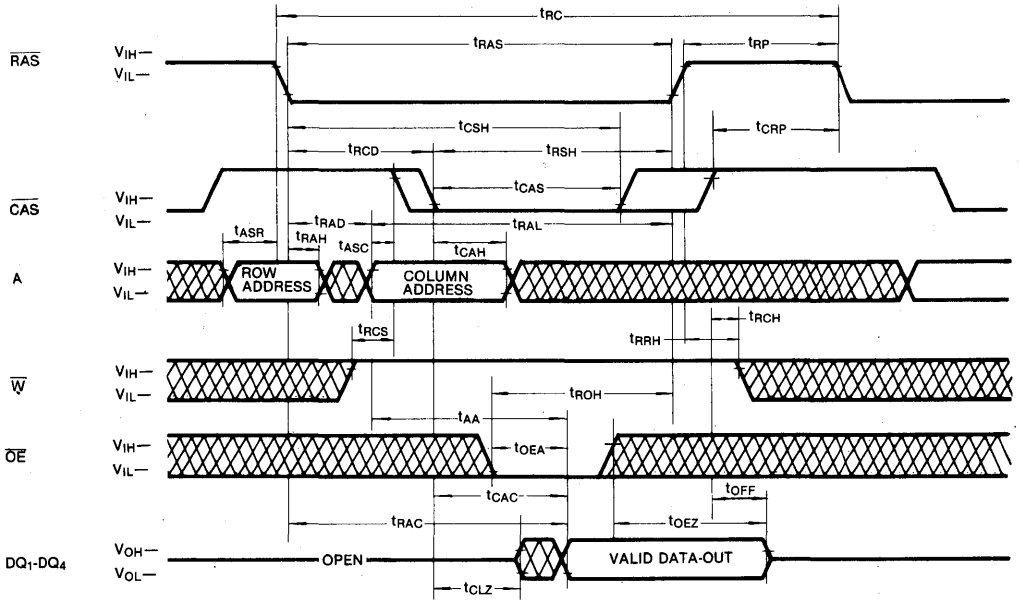
NOTES (Continued)

5. Assumes that $t_{RCD} \geq t_{RCD}(max)$.
6. t_{WCR}, t_{DHR} are referenced to $t_{RAD}(max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}(min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(min)$, $t_{RWD} \geq t_{RWD}(min)$ and $t_{AWD} \geq t_{AWD}(min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RAC}(max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled by t_{AA}.

2

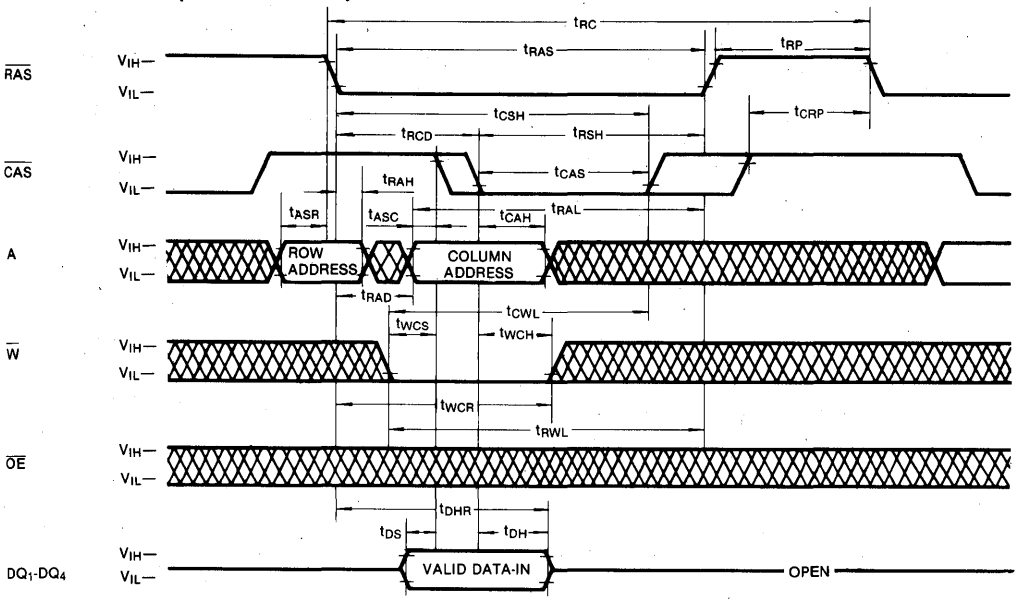
TIMING DIAGRAMS

READ CYCLE

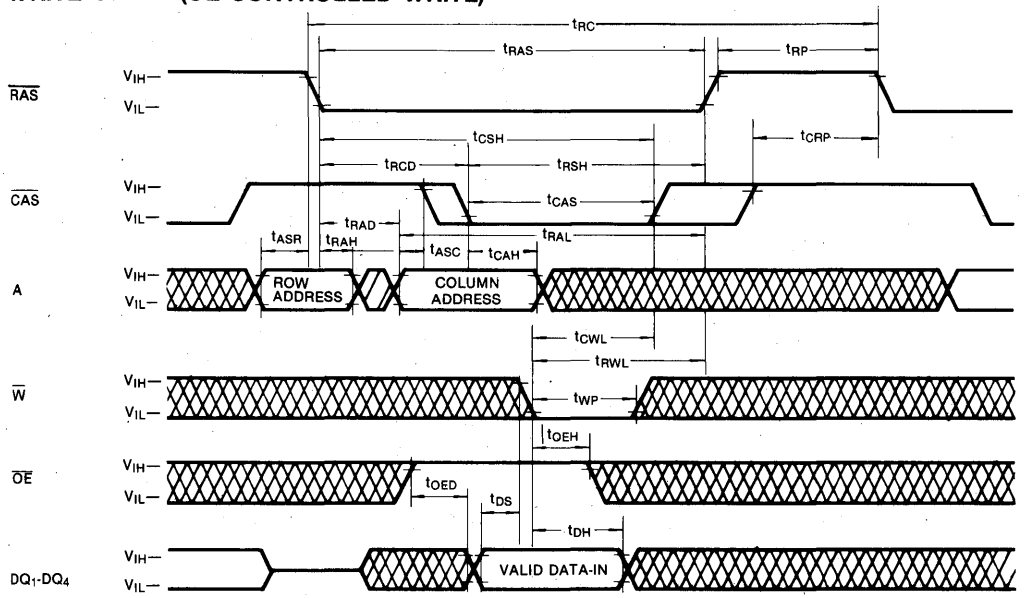


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

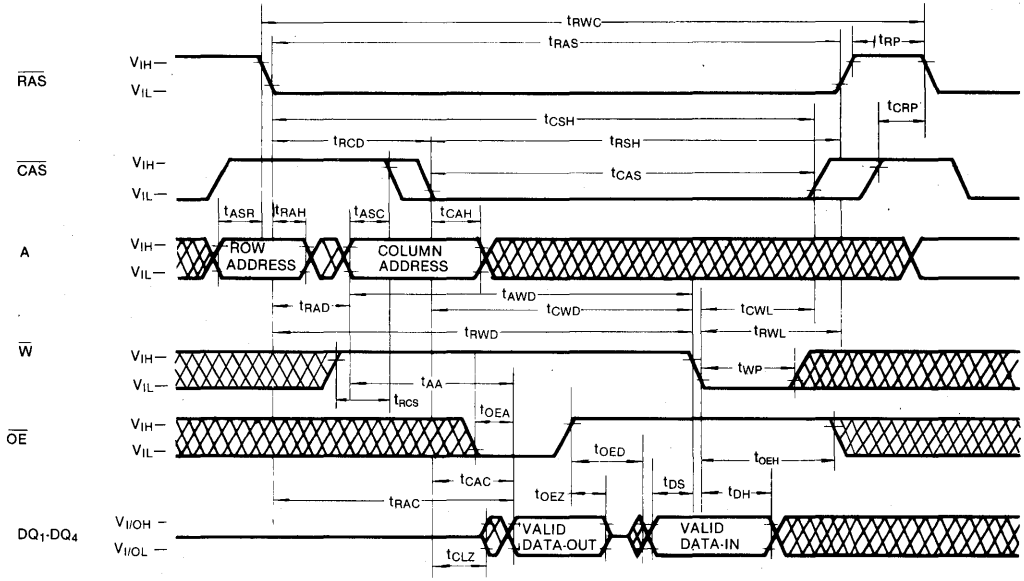


WRITE CYCLE (OE CONTROLLED WRITE)

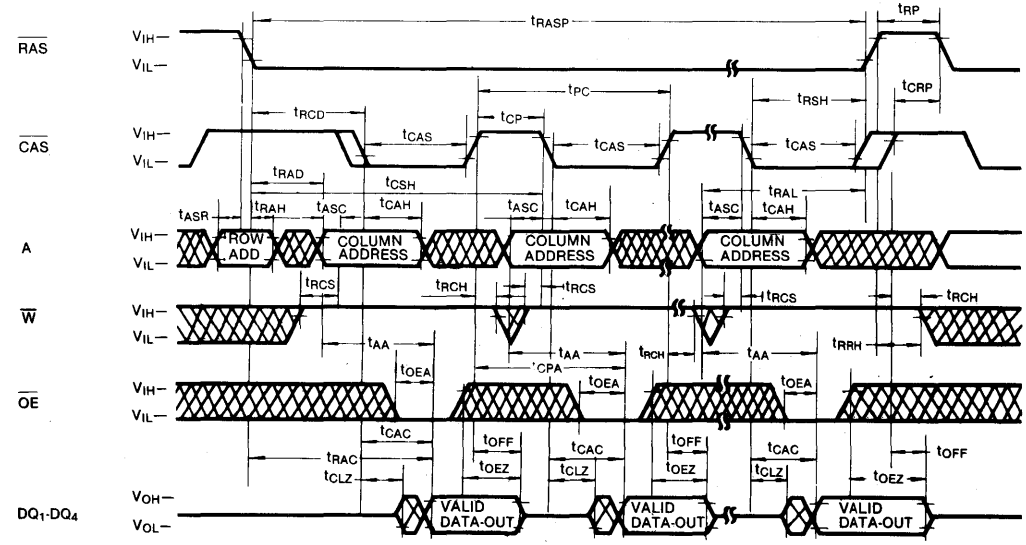


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

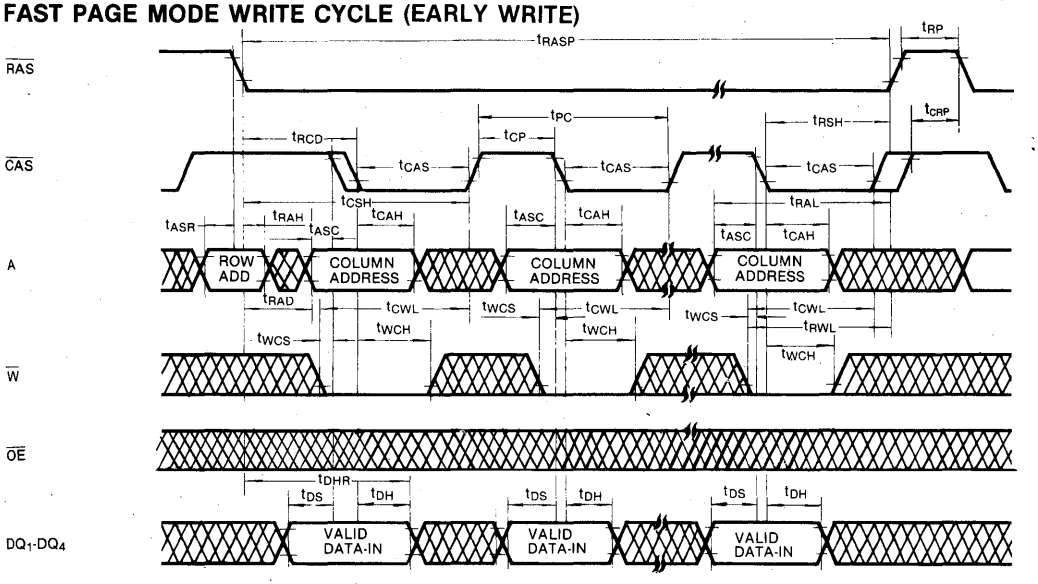


DON'T CARE

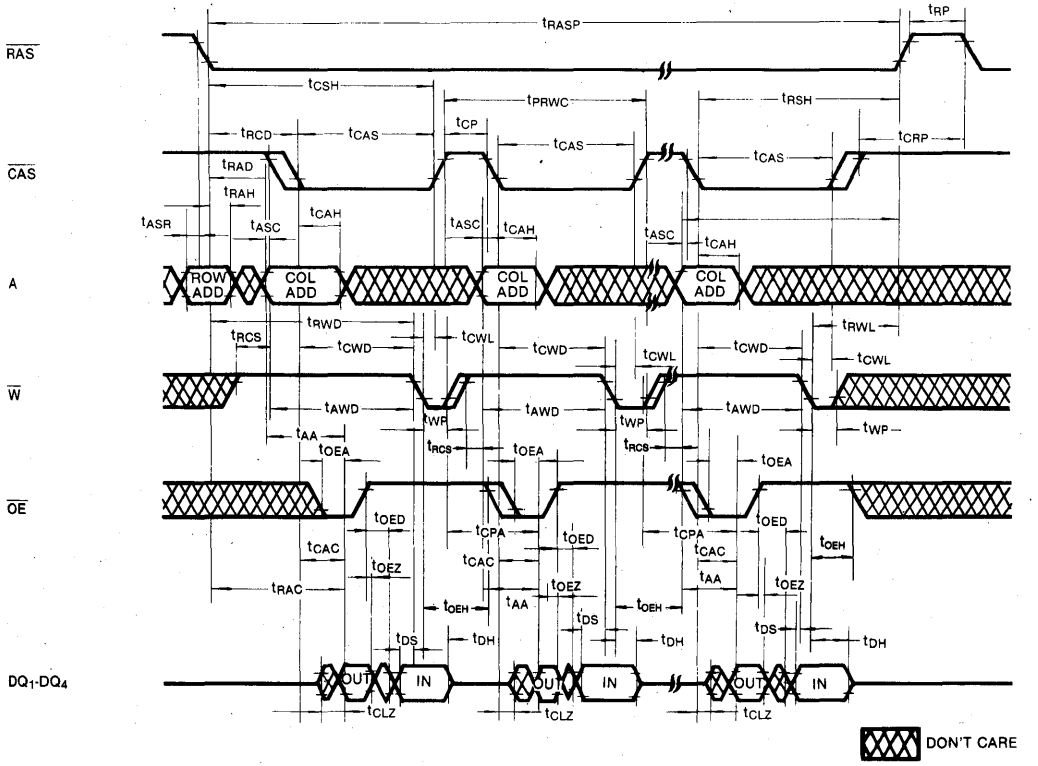
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE

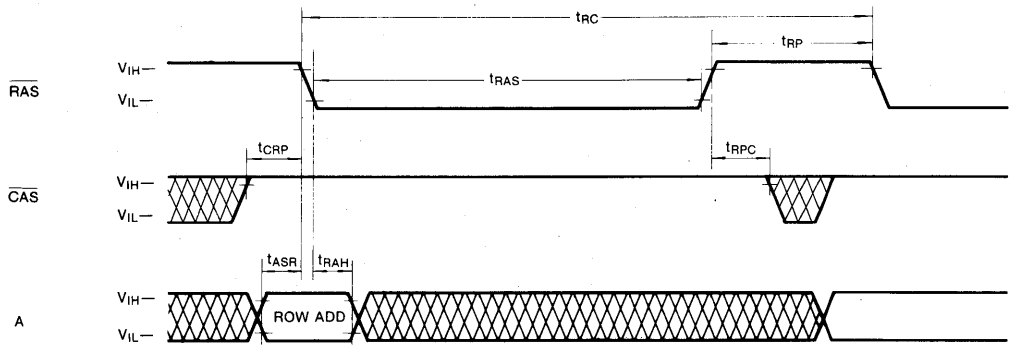


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

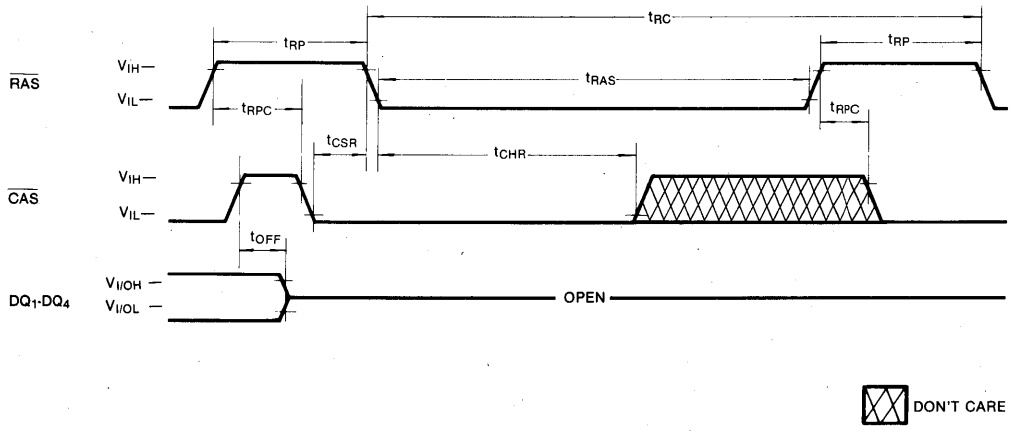
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



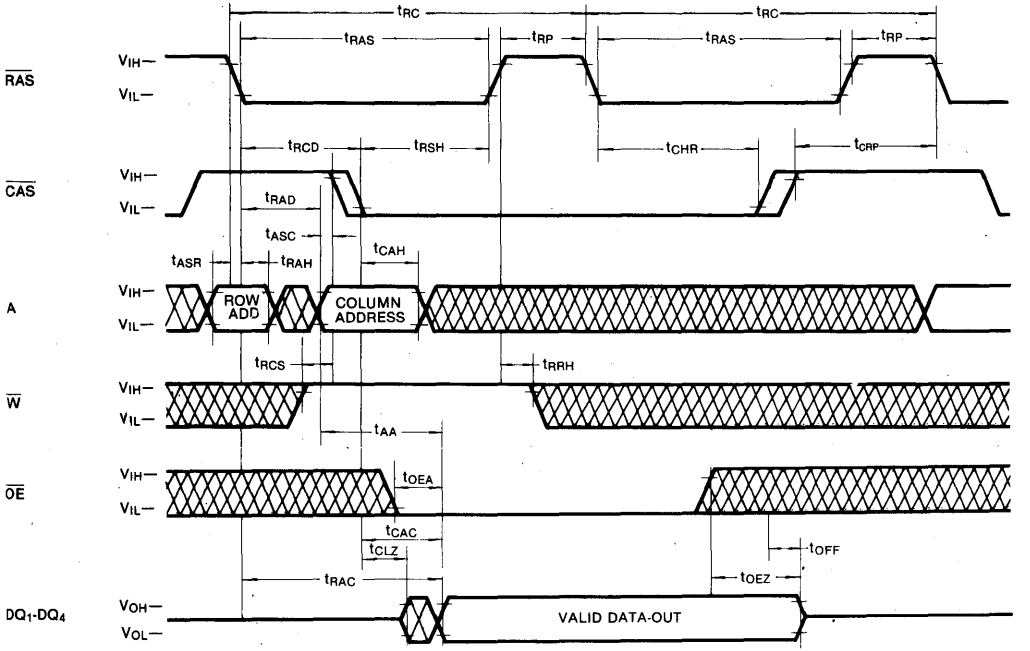
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$, A = Don't care

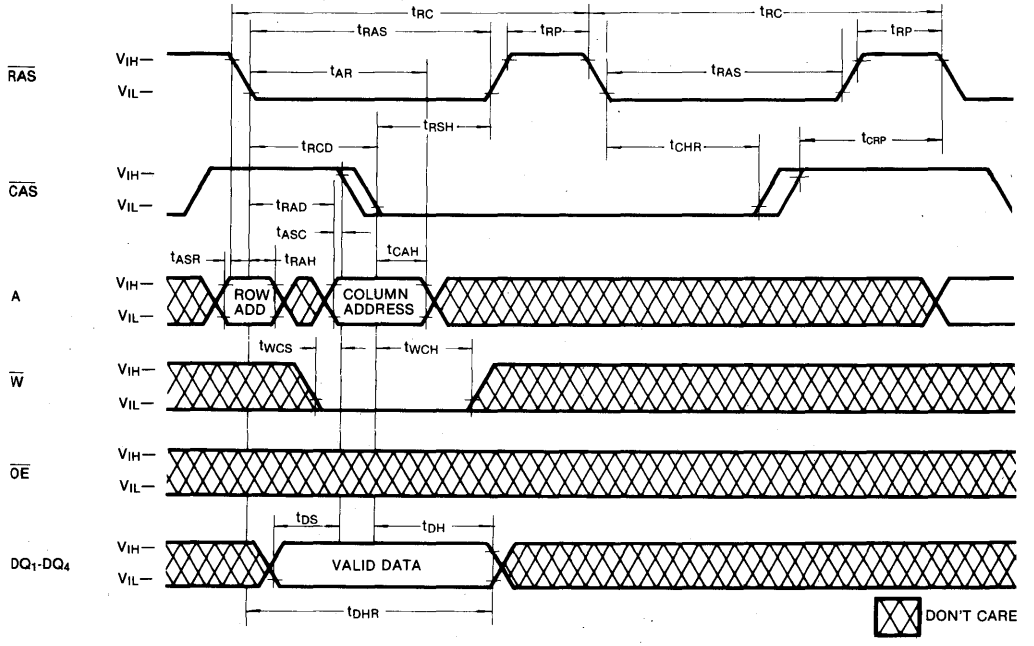


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



SAMSUNG ELECTRONICS

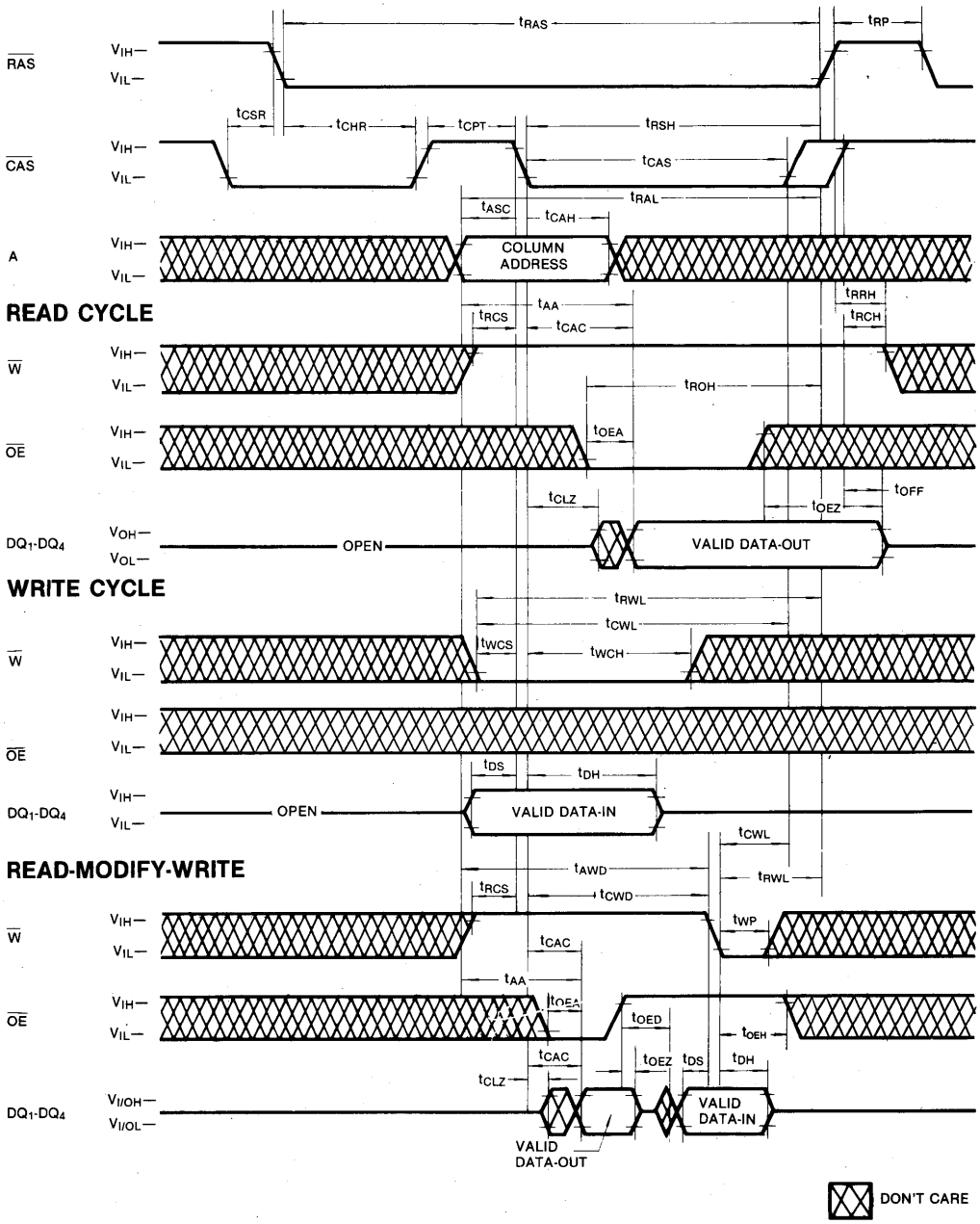
TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

READ CYCLE

WRITE CYCLE

READ-MODIFY-WRITE



DEVICE OPERATION

Device operation

The KM44C256C/CL/CSL contains 1,048,576 memory locations organzed as 262,144 four-bit words. Eighteen address bits are required to address a paricular 4-bit word in the memory array. Since the KM44C256C/CL-/CSL has only 9 address input pins,time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column adress strobe($\overline{CAS}$), and the valid row and column address inputs.

Operation of the KM44C256C/CL/CSL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C256C/CL/CSL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C256C/CL/CSL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max), then the access time to valid data is specified by t_{RAC}(min). However if $\overline{CAS}$ goes low after t_{RCD}(max), or if the column address becomes valid after t_{RAD}(max.), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

The KM44C256C/CL/CSL has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, OE must be low for the period of time defined by to t_{OEA} and t_{OEZ}.

Write

The KM44C256C/CL/CSL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pin is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in he Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. This output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met the output may contiain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C256C/CL/CSL's DQ pins.

Data Output

The KM44C256C/CL/CSL has a three-state output buffer which is controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever $\overline{CAS}$ or $\overline{OE}$ is high(V_{IH}), the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C256C/CL/CSL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode

DEVICE OPERATION (Continued)

Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$ only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM44C256C/CL/CSL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8/64/128 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A_0~A_8).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C256C/CL/CSL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C256C/CL/CSL hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

0ther Refresh Methods: It is also possible to refresh the KM44C256C/CL/CSL by using read, write or read-modify write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the low address bits A_0 through A_8 are supplied by the on-chip refresh counter.

Fast Page Mode

The Fast page mode Provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. Then, while $\overline{RAS}$ is kept low to maintain the row address $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time requried to set up and strobe sequential row addresses for the same page

Power-up

If $\overline{RAS}$=V_{SS} during power-up, the KM44C256C/CL/CSL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current. An initial pause of 200 μ sec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C256C/CL/CSL inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used,series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C256-C/CL/CSL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transisient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS

DEVICE OPERATION (Continued)

run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.
Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Decoupling

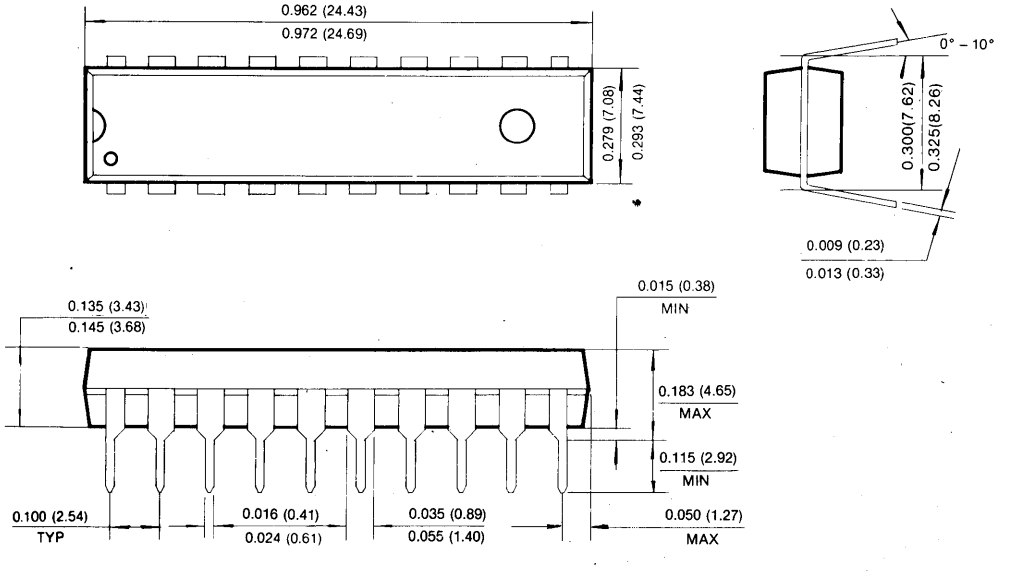
The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.1μF ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM44C256C/CL/CSL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C256C/CL/CSL and they supply much of the current used by the KM44C256-C/CL/CSL during cycling.
In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

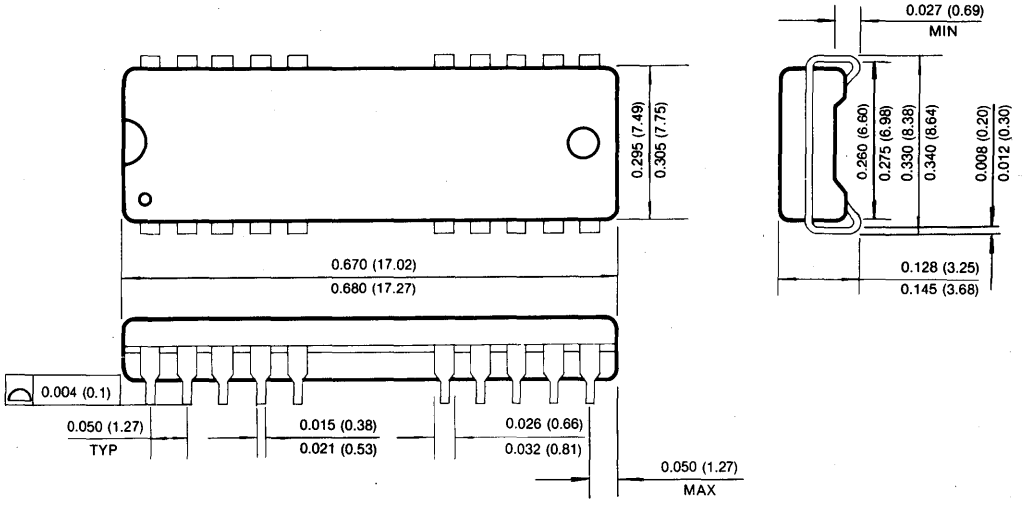
Units: Inches (Millimeters)



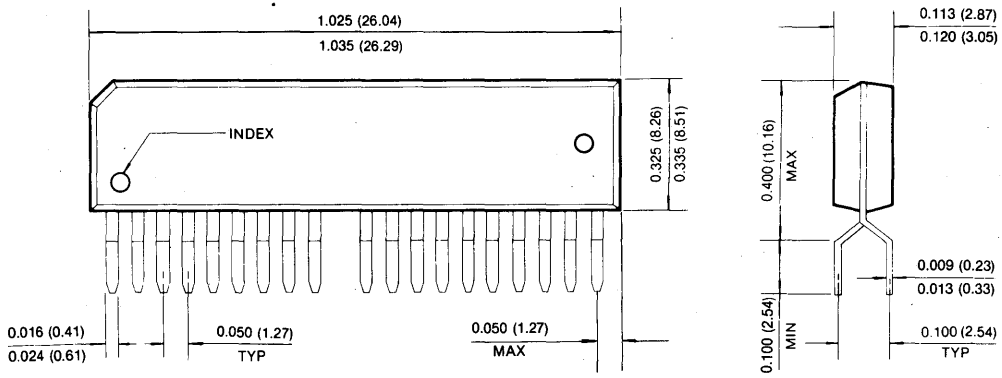
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



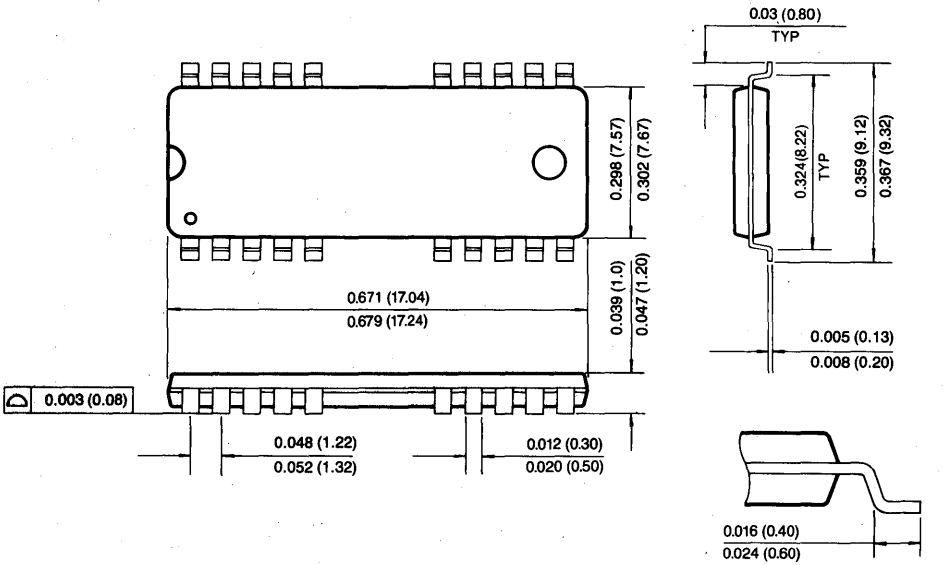
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



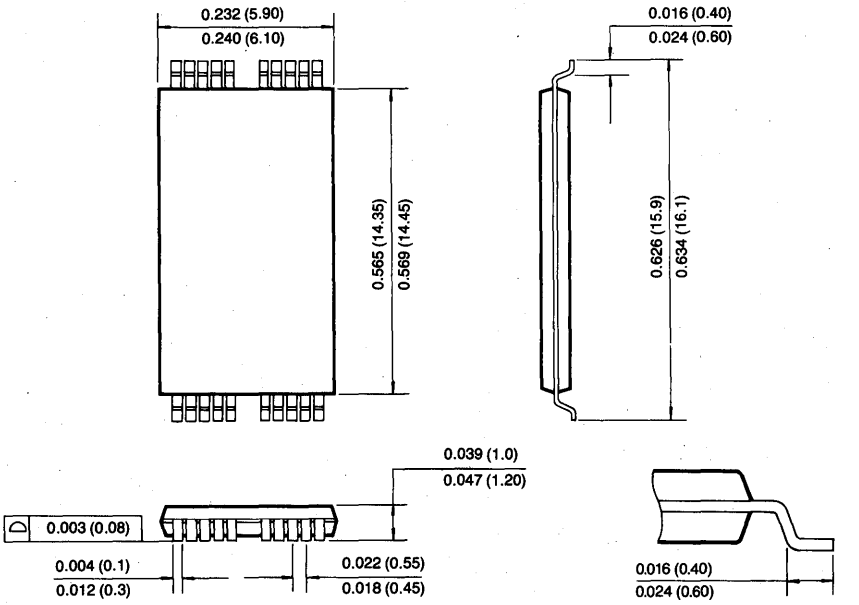
PACKAGE DIMENSIONS (Continued)

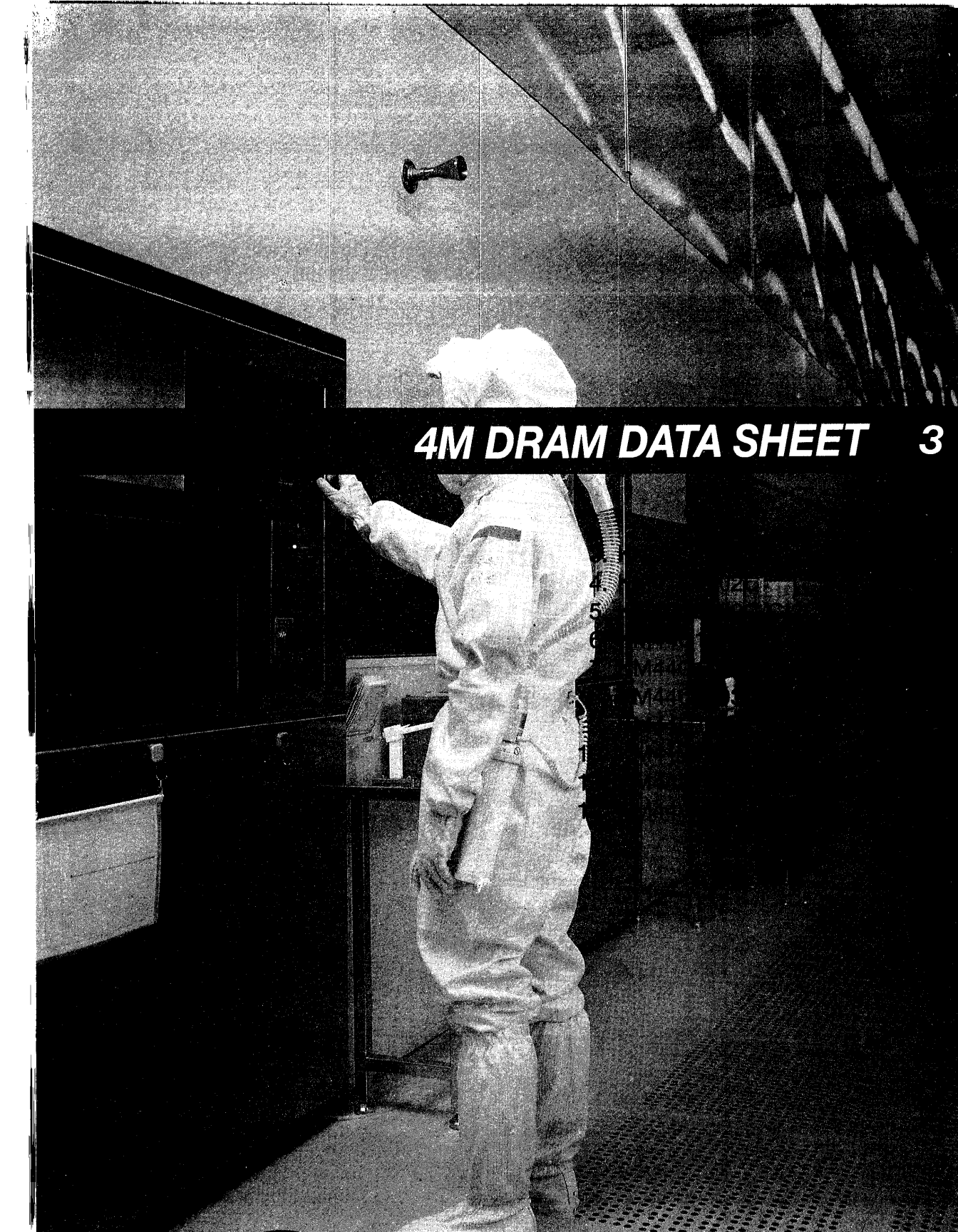
20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)





4M DRAM DATA SHEET 3

4M ×1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM41C4000C/CL/CSL-5	50ns	13ns	90ns
KM41C4000C/CL/CSL-6	60ns	15ns	110ns
KM41C4000C/CL/CSL-7	70ns	20ns	130ns
KM41C4000C/CL/CSL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and hidden refresh capability**
- **Fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Common I/O using early write**
- **Single + 5V ±10% power supply**
- **Refresh Cycle**
  - **1024 cycle/16ms (Normal)**
  - **1024 cycle/128ms (L-version)**
  - **1024 cycle/256ms (SL-version)**
- **Power dissipation**
  - **Standby : 5.5mW(Normal)**
    1.1mW(L-version)
    0.55mW(SL-version)
  - **Active (50/60/70/80): 470/415/360/305mW**
- **JEDEC standard pinout**
- **Available in plastic SOJ, ZIP and TSOP-II packages**

GENERAL DESCRIPTION

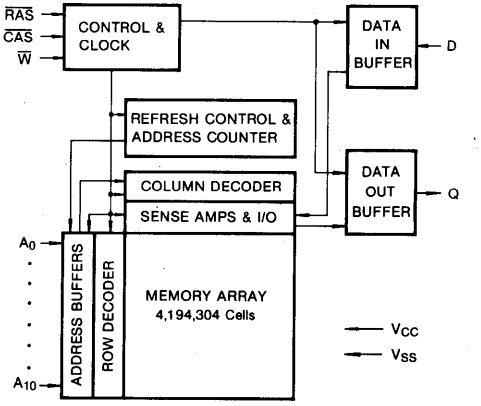
The Samsung KM41C4000C/CL/CSL is a high speed CMOS 4,194,304 × 1 Dynamic Random Access Memory. Its design is optimized for high performancd applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4000C/CL/CSL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capabillity provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

The KM41C4000C/CL/CSL is fabricated using Samsung's advanced CMOS process.

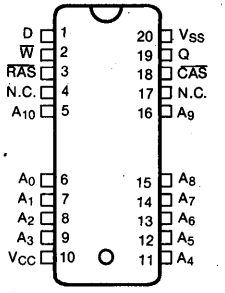
3

FUNCTIONAL BLOCK DIAGRAM

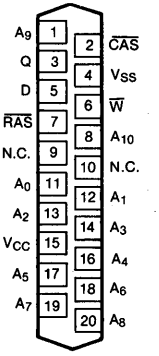


PIN CONFIGURATION (Top Views)

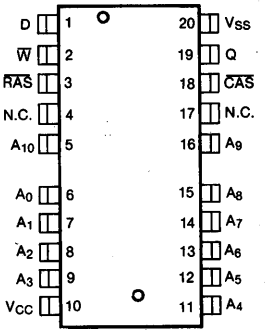
• KM41C4000CJ/CLJ/CSLJ



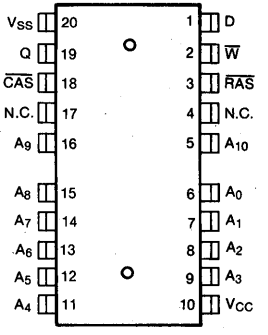
• KM41C4000CZ/CLZ/CSLZ



• KM41C4000CT/CLT/CSLT



• KM41C4000CTR/CLTR/CSLTR



Pin Names	Pin Function
A_0-A_{10}	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	℃
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	–	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	–	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	KM41C4000C/CL/CSL-5	I_{CC1}	-	85	mA
	KM41C4000C/CL/CSL-6		-	75	mA
	KM41C4000C/CL/CSL-7		-	65	mA
	KM41C4000C/CL/CSL-8		-	55	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Cycling @t_{RC}=min.)	KM41C4000C/CL/CSL-5	I_{CC3}	-	85	mA
	KM41C4000C/CL/CSL-6		-	75	mA
	KM41C4000C/CL/CSL-7		-	65	mA
	KM41C4000C/CL/CSL-8		-	55	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM41C4000C/CL/CSL-5	I_{CC4}	-	65	mA
	KM41C4000C/CL/CSL-6		-	55	mA
	KM41C4000C/CL/CSL-7		-	45	mA
	KM41C4000C/CL/CSL-8		-	35	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC} -0.2V)	KM41C4000C	I_{CC5}	-	1	mA
	KM41C4000CL		-	200	μA
	KM41C4000CSL		-	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM41C4000C/CL/CSL-5	I_{CC6}	-	85	mA
	KM41C4000C/CL/CSL-6		-	75	mA
	KM41C4000C/CL/CSL-7		-	65	mA
	KM41C4000C/CL/CSL-8		-	55	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=125(L-ver.)μS T_{RC}=250(SL-ver.)μS T_{RAS}=T_{RAS} min~300ns	KM41C4000CL	I_{CC7}	-	300	μA
	KM41C4000CSL		-	150	μA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $o \leq V_{IN} \leq V_{CC}+0.5V$ all other pins not under test=0 volts.)	$I_{I(L)}$	-10*	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

* Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$= V_{IL}. I_{CC4}, Address can be changed maximum once during a Fast Page Mode Cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	–	5	pF
Input Capacitance (A_0-A_{10})	C_{IN2}	–	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	–	7	pF
Output Capacitance (Q)	C_{OUT}	–	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	108		130		155		175		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	7
Transition time(rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10.000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	35	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	
Data-in-set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		10		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (Low power)	tREF		128		128		128		128	ms	
Refresh period (Super low power)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	13		15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	50		60		70		80		ns	8
Column address to $\overline{W}$ delay time	tAWD	25		30		35		40		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast page mode cycle time	tPC	35		40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	53		60		70		75		ns	
$\overline{RAS}$ pulse width(Fast Page Mode)	tRASP	50	200.000	60	200,000	70	200,000	80	200,000	ns	
$\overline{CAS}$ precharge time(Fast page mode)	tCP	10		10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
Write command set-up time (test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ cycle)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ cycle)	tWRH	10		10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

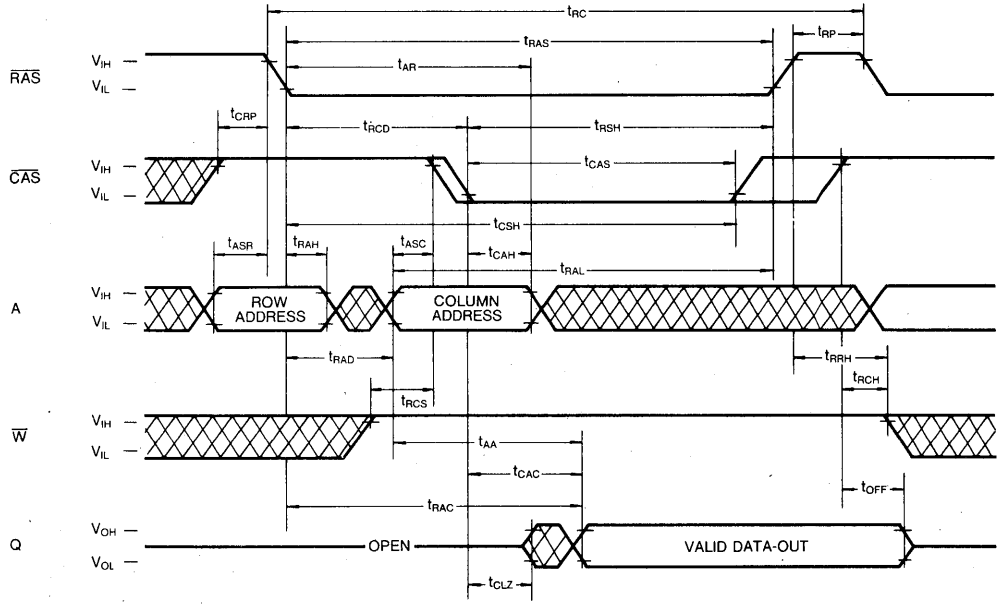
Parameter	Symbol	-5		-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	95		115		135		135		ns	
Read-modify-write cycle time	t_{RWC}	113		135		160		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		18		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		45		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	18		20		25		25		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	55		65		75		85		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	30		35		40		45		ns	8
Fast mode cycle time	t_{PC}	40		45		50		55		ns	
Fast page mode read-modefy-write	t_{PRWC}	58		65		75		80		ns	
$\overline{RAS}$ pulse width(Fast page mode)	t_{RASP}	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45		50	ns	3

NOTES

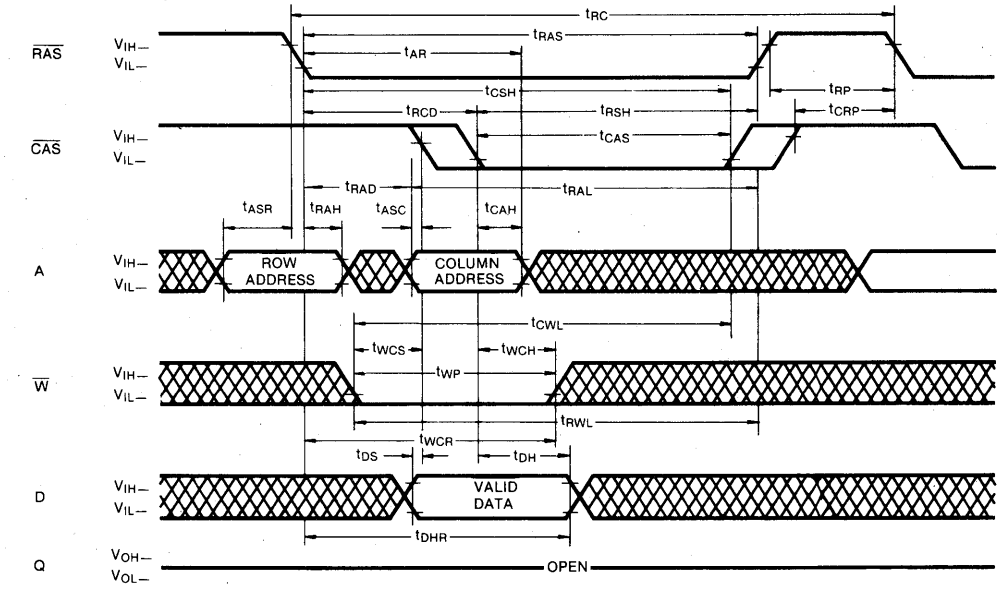
1. An initial pause of 200μs is required after power up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If $t_{RCD(max)}$ is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data our will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE (EARLY WRITE)

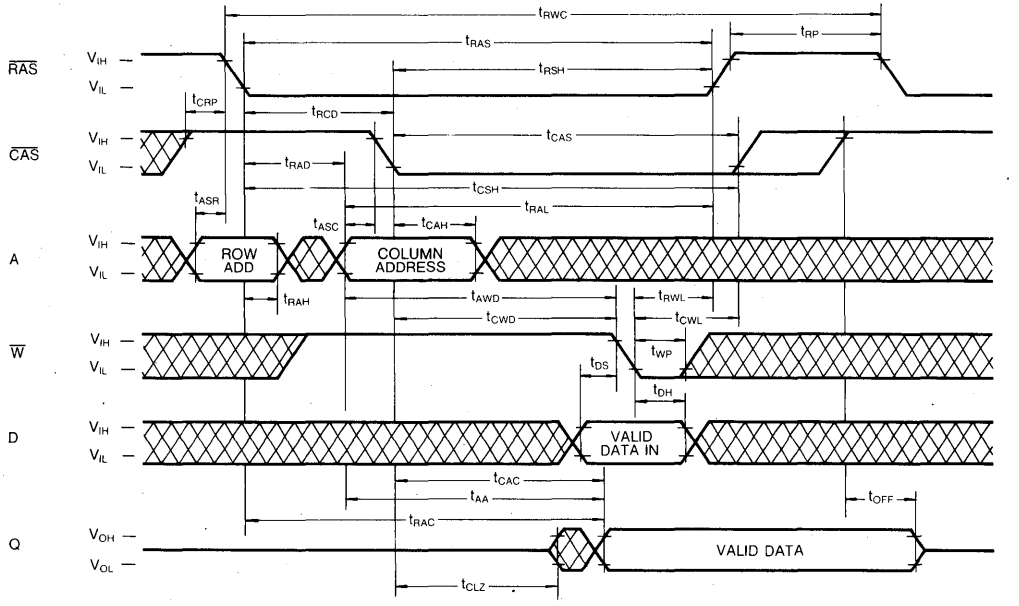


DON'T CARE

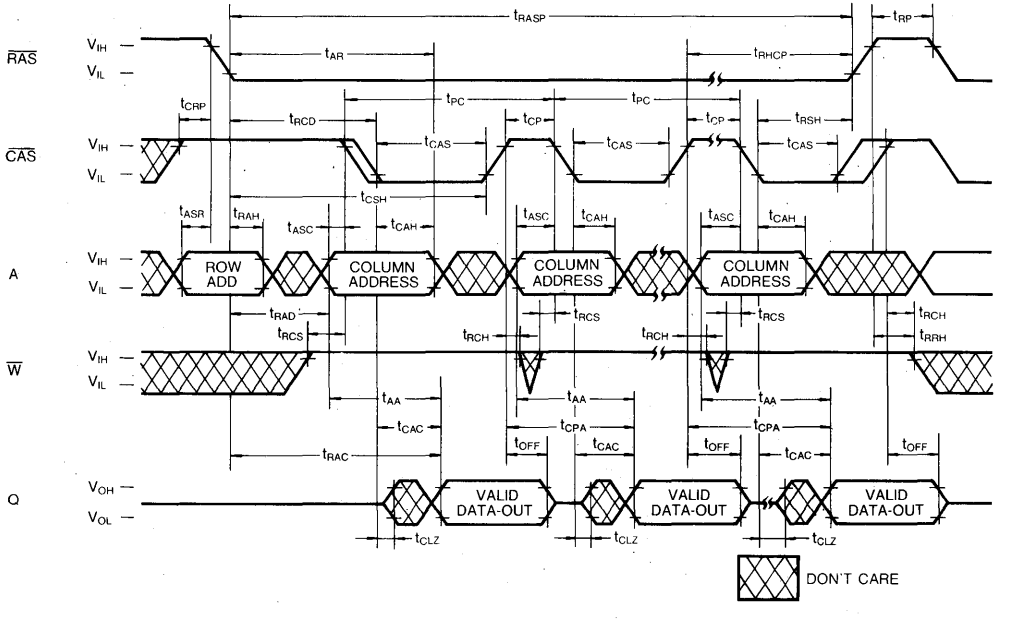
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



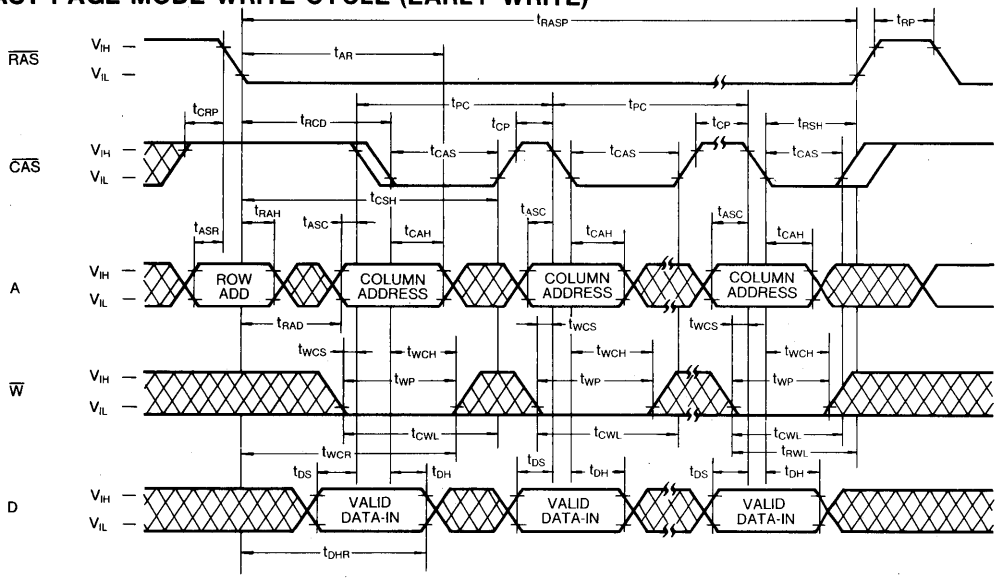
FAST PAGE MODE READ CYCLE



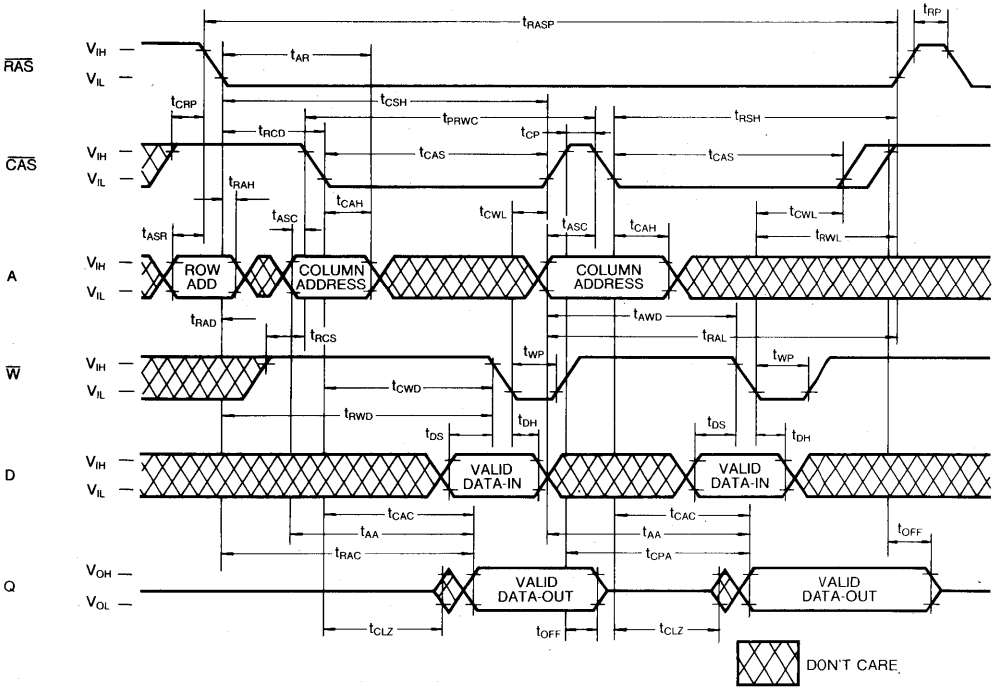
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



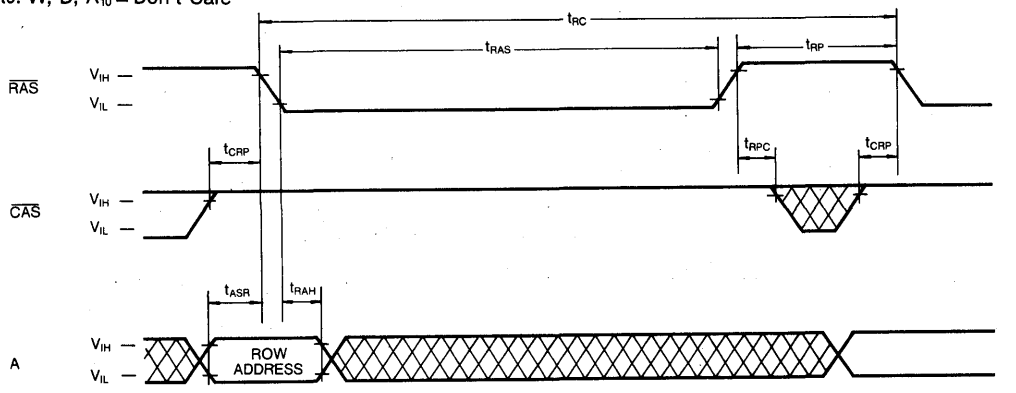
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

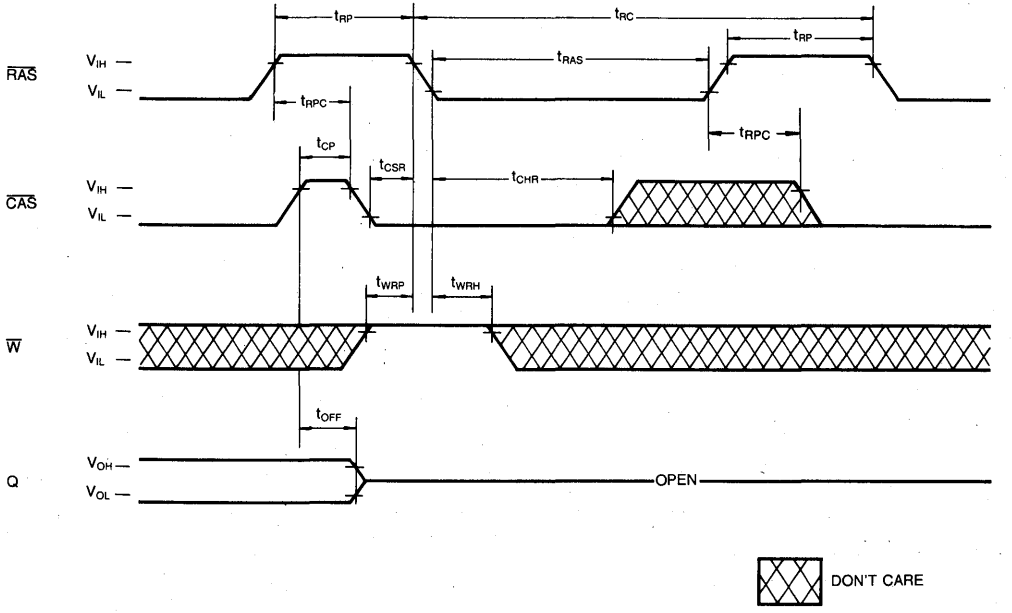
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, D, A_{10} = Don't Care



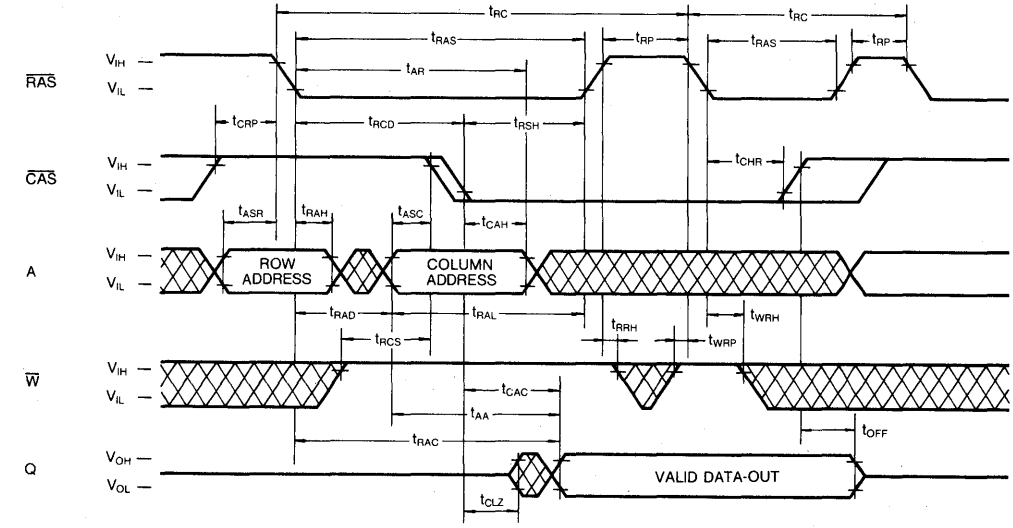
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: Address = Don't Care

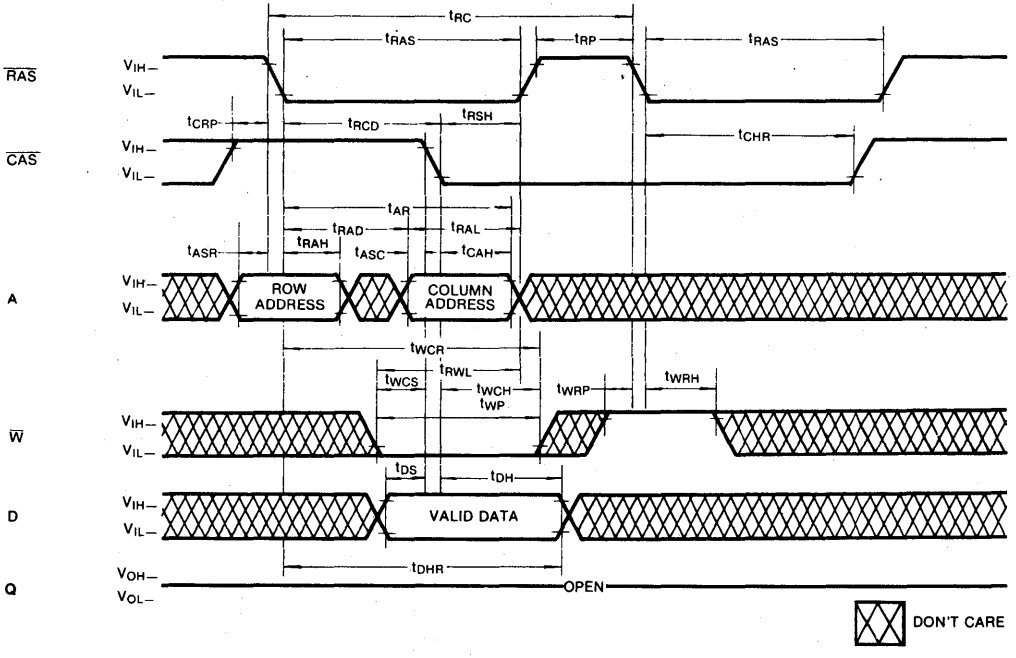


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

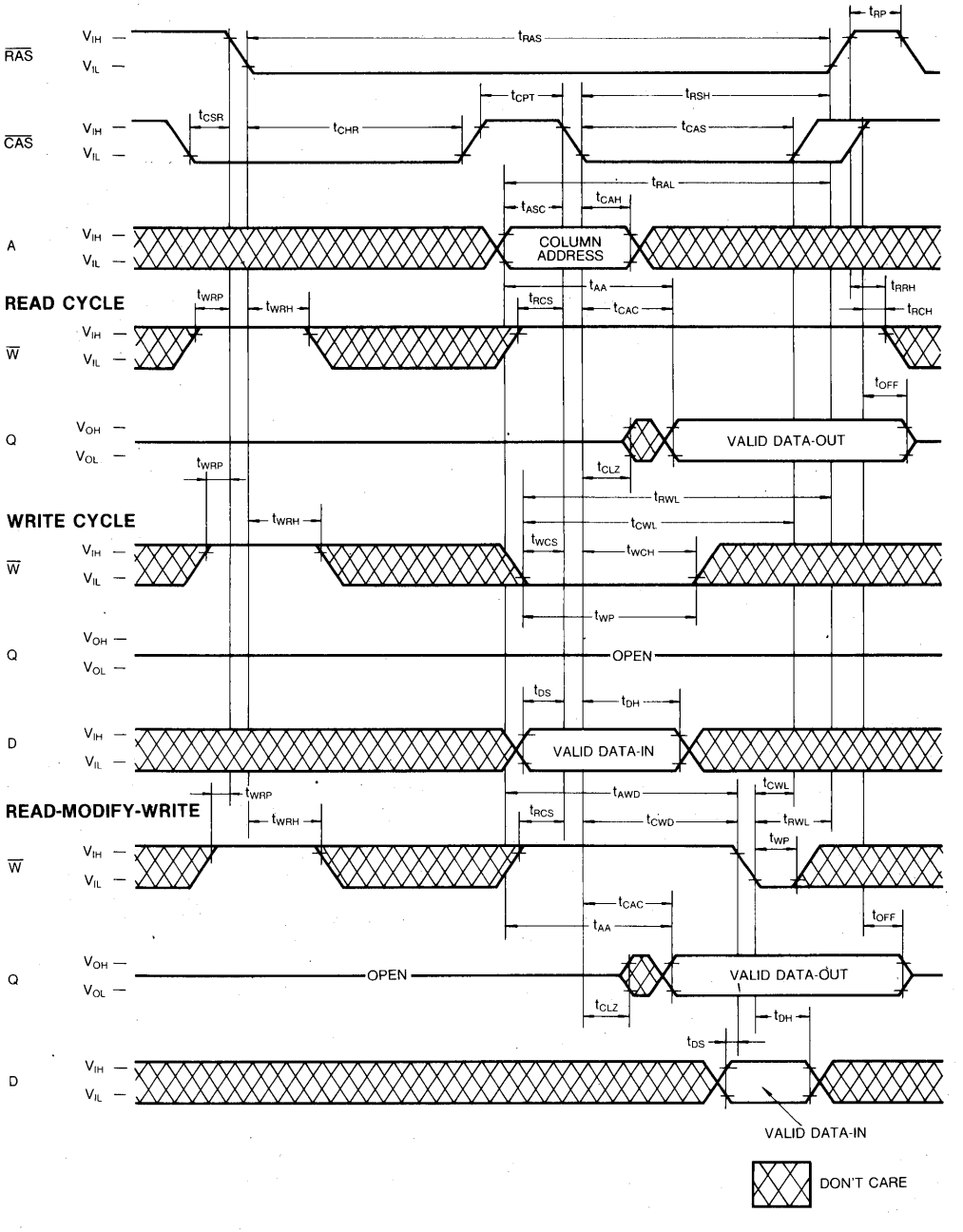


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

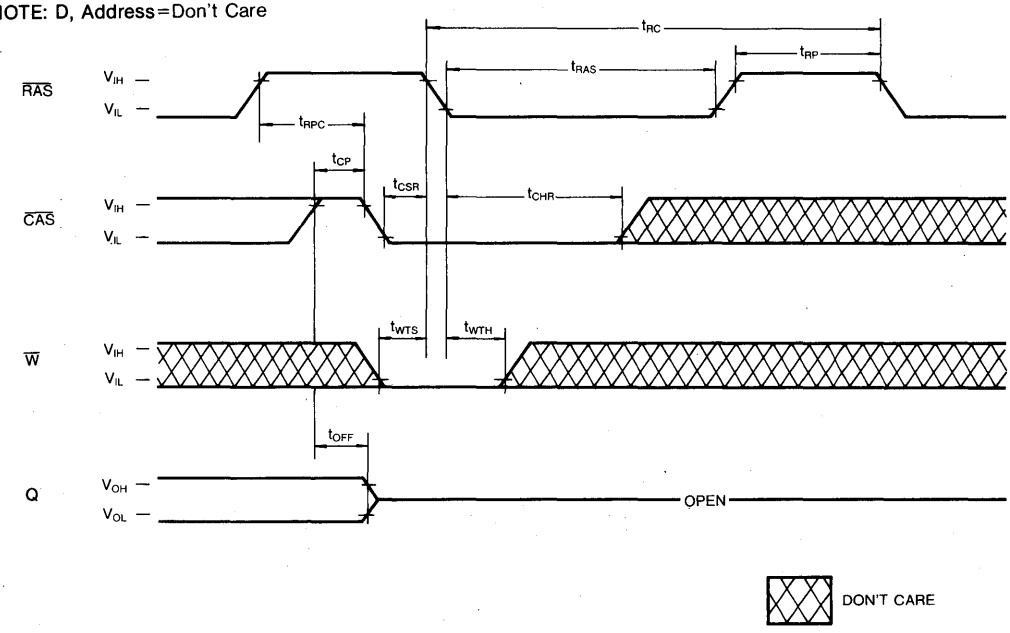
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM41C4000C/CL/CSL is the RAM organized 4, 194,304 words by 1 bit it is internally organized 524, 288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 and A_{10} are not used. If, upon reading, all bits are equal (all "1" or "0"s) the Q pin indicates a "1".
If they were not equal, the Q pin would indicate a "0".

In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode", And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only-Refresh Cycle" puts it back into "Normal Mode". During the test mode operation, a WCBR cycle is used to perform refresh. The "Test Mode" function reduces test time(1/8 in cases of N test pattern.)

DEVICE OPERATION

Device Operation

The KM41C4000C/CL/CSL contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4000C/CL/CSL has only 11 address input pint, time multiplexed addressing is used to input 11 row and 11 column address. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe($\overline{CAS}$), and the valid row and column address inputs.

Operating of the KM41C4000C/CL/CSL begins by strobing in valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C4000C/CL/CSL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time(t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4000C/CL/CSL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max) the access time to valid data is specified by t_{RAC}. if $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minmum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD} (max).

Write

The KM41C4000C/CL/CSL can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. The cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after$\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur, The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeteminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4000C/CL/CSL has three-state output buffer which are controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high(V_{IH}), the outputs is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the putput goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of CAS, Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4000C/CL/CSL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C4000C/CL/CSL is stored on a

DEVICE OPERATION (Continued)

tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16/128/256 ms. There several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C4000C/CL/CSL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation auto-matically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C4000C/CL/CSL hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4000C/CL/CSL by using read, write or read-modify write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM41C4000C/CL/CSL has Fast page mode capability. Fast page mode memory cycles provides faster access and lower power dissipation than normal memory cycles. In Fast page mode, it is possible to perform read, write or read-modify-write cyclels. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A fast page mode cycle beging with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows

Row Address- Bits A_0 through A_9 are supplied by the on-chip refresh counter. This A_{10} bit is set high interally.

Column Address-Bits A_0 through A_{10} are strobed -in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by perfoming 8$\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test patten of "lows"into the memory cells at a single column address and 1024 row address(The row addresses are supplied by the on-chip refresh counter)
3. Using read-modify-write cycles, read the "lows"written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS}$=V_{SS} during power-up, the KM41C4000C/CL/CSL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and ply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize the power-up current. An initial pause of 200 μ sec is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. Eight initialization cycles are also required after any 16(L-version:128, SL-version:256) msec period in which there are no $\overline{RAS}$ cycles. An

DEVICE OPERATION (Continued)

initialization cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C4000C/CL/CSL inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel temination may be used,series temination is generallu recommended since it is simple and draws on additional power. It consists of a resistor in series with the input line placed close to the KM41C4000C/CL/CSL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transinent effects are minized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each inter section or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV

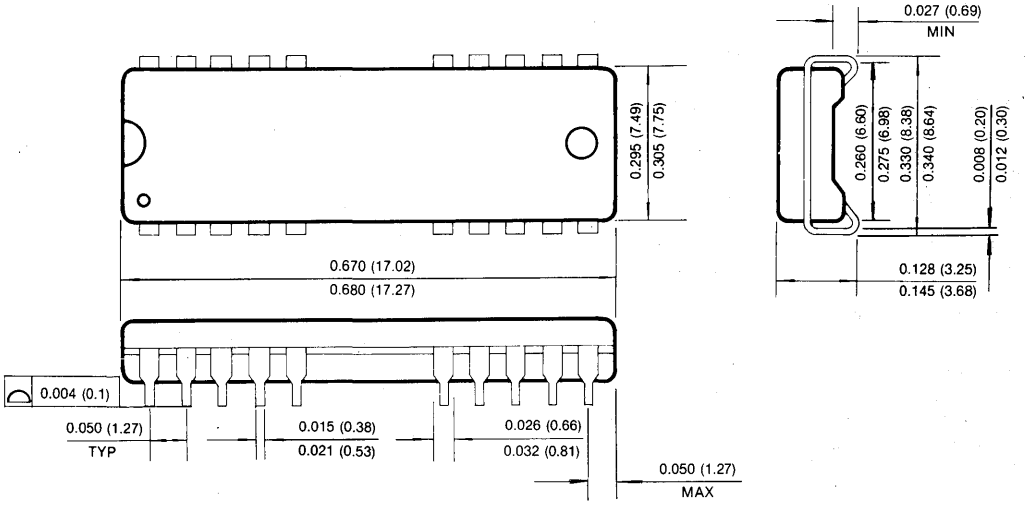
A high frequency 0.1 μF ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM41C4000C/CL/CSL using the shortest possible traces. These capacitors act as a low imped ance shunt for the high frequency switching transients generated by the KM41C4000C/CL/CSL and they supply much of the current used by the KM41C4000C/CL/CSL during cycling.

In anddition, a large tantalum capacitor with a value of 47 μF to 100 μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

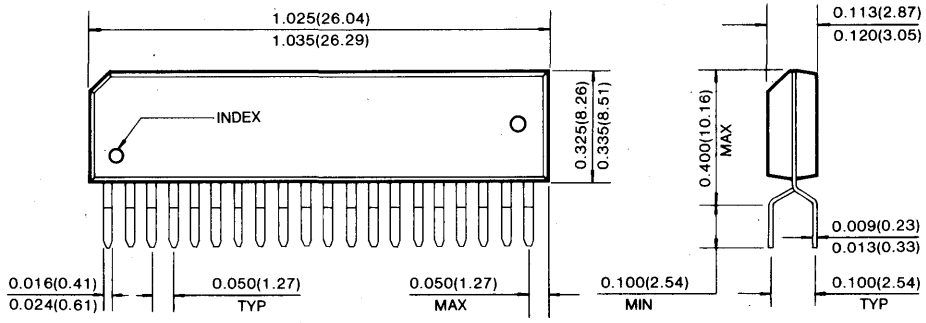
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



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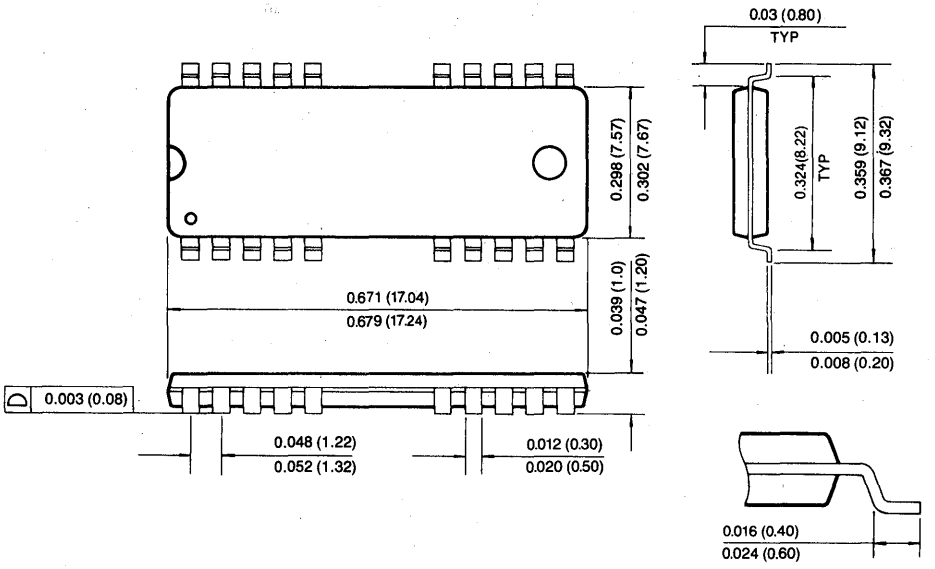
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



4M × 1 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM41C4002C-5	50ns	13ns	90ns
KM41C4002C-6	60ns	15ns	110ns
KM41C4002C-7	70ns	20ns	130ns
KM41C4002C-8	80ns	20ns	150ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Commom I/O using Early Write**
- **Single +5.0V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ, ZIP and TSOP(II) Packages**

GENERAL DESCRIPTION

The Samsung KM41C4002C is a CMOS high speed 4,194,304 × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

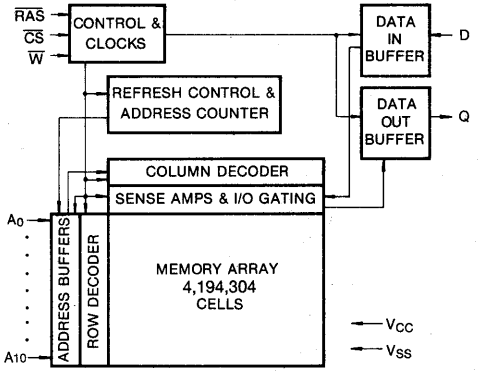
The KM41C4002C features Static Column Mode operation which allows high speed random or Sequential access within a row. Static Column Mode operation offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

The KM41C4002C is fabricated using Samsung's advanced CMOS process.

3

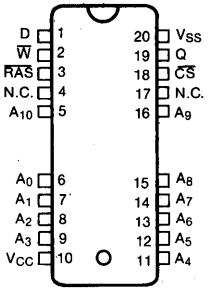
FUNCTIONAL BLOCK DIAGRAM



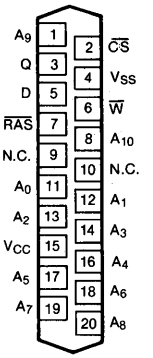
SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top Views)

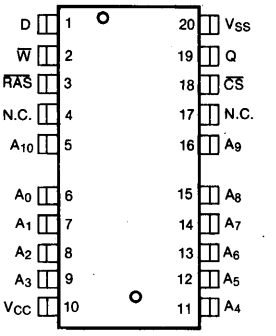
• KM41C4002CJ



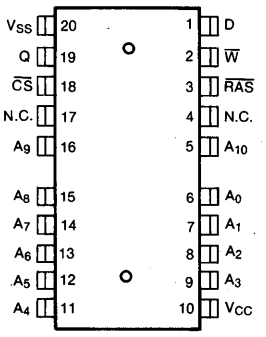
• KM41C4002CZ



• KM41C4002CT



• KM41C4002CTR



Pin Names	Pin Function
A_0-A_{10}	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC}=min.)	KM41C4002C-5	I_{CC1}	-	85	mA
	KM41C4002C-6		-	75	mA
	KM41C4002C-7		-	65	mA
	KM41C4002C-8		-	55	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM41C4002C-5	I_{CC3}	-	85	mA
	KM41C4002C-6		-	75	mA
	KM41C4002C-7		-	65	mA
	KM41C4002C-8		-	55	mA
Static Column Mode Current* ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling @t_{PC}=min.)	KM41C4002C-5	I_{CC4}	-	65	mA
	KM41C4002C-6		-	55	mA
	KM41C4002C-7		-	45	mA
	KM41C4002C-8		-	35	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{CC}-0.2V)		I_{CC5}	-	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC}=min.)	KM41C4002C-5	I_{CC6}	-	85	mA
	KM41C4002C-6		-	75	mA
	KM41C4002C-7		-	65	mA
	KM41C4002C-8		-	55	mA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. I_{CC1}, I_{CC3}, I_{CC6} Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once during a Static Column mode cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance(D)	C_{IN1}	-	5	pF
Input Capacitance (A_0~A_{10})	C_{IN2}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$)	C_{IN3}	-	7	pF
Input Capacitance (Q)	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	108		130		150		170		ns	
Static column mode cycle time	t_{SC}	30		35		40		45		ns	
Static column mode read-write cycle time	t_{SRWC}	53		65		75		85		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
Access time from last write	t_{ALW}		50		55		65		75	ns	3
$\overline{CS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	7
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	2
Output data hold time from column address	t_{AOH}	5		5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		35		40		45		55	ns	
Output data hold time from $\overline{W}$	t_{WOH}	0		0		0		0		ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width(static column mode)	t_{RASC}	50	100,000	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CS}$ pulse width	t_{CS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	13	100,000	15	100,000	20	100,000	20	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold	t_{CAH}	10		10		15		15		ns	
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	40		45		55		60		ns	6

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		70		80		90		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Column address hold time referenced to $\overline{RAS}$ rise.	t_{AH}	5		5		5		5		ns	
Last Write to column address to delay time	t_{LWAD}	20	25	20	30	20	35	20	40	ns	12
Last write to column address gold time	t_{AHLW}	50		55		65		75		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command inactive time	t_{WI}	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		15		15		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	13		15		15		15		ns	
Data-in set-up time	t_{DS}	0		0		0		0		ns	10
Data-in hold time	t_{DH}	10		10		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	13		15		15		15		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	50		60		70		80		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	25		30		35		40		ns	8
$\overline{CS}$ setup time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		10		ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{CS}$-before-$\overline{RAS}$ cycle)	t_{WRP}	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ cycle)	t_{WRH}	10		10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{RPC}	5		5		5		5		ns	
Refresh counter test $\overline{CS}$ precharge time	t_{CPT}	20		20		25		30		ns	

TEST MODE CYCLE

(Note.13)

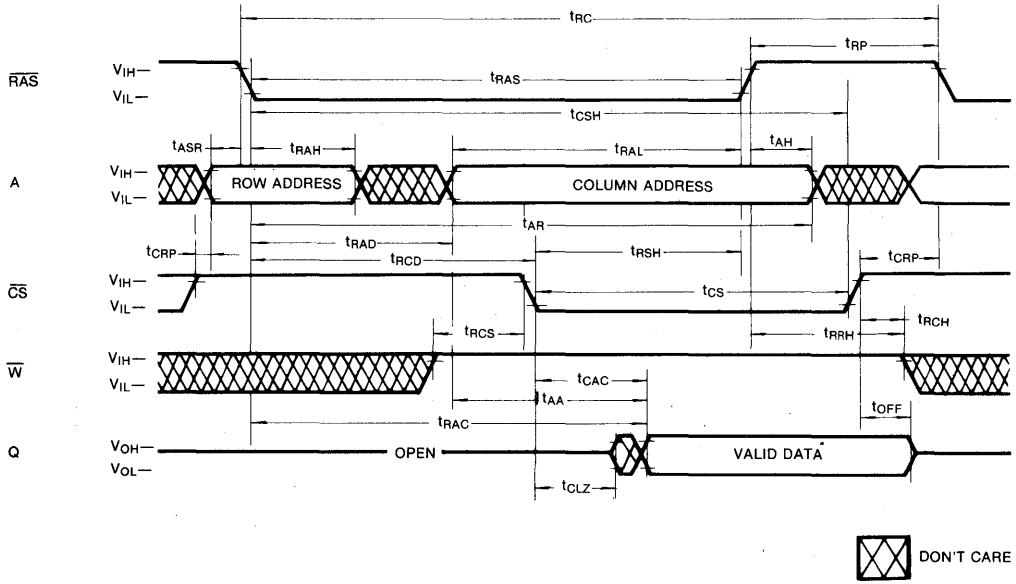
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	95		115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	113		135		155		175		ns	
Access time from $\overline{RAS}$	t_{RAC}		55		65		75		85	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		18		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CS}$ pulse width	t_{CS}	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		25		25		ns	
$\overline{CS}$ hold time	t_{CSH}	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		45		ns	
$\overline{CS}$ to Write enable delay	t_{CWD}	18		20		20		20		ns	8
$\overline{RAS}$ to Write enable delay	t_{RWD}	55		65		75		85		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	30		35		40		45		ns	8
Static column mode cycle time	t_{SC}	35		40		45		50		ns	
Static column mode read-modify-write	t_{SRWC}	58		70		80		90		ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	55	100,000	65	100,000	75	100,000	85	100,000	ns	
Access time from last write	t_{ALW}		55		65		75		85	ns	3,12
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	18	100,000	20	100,000	25	100,000	25	100,000	ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. Operation within the $t_{LWAD(max)}$ limit insures that $t_{ALW(max)}$ can be met. $t_{LWAD(max)}$ is specified as a reference point only. t_{LWAD} is greater than the specified $t_{LWAD(max)}$ limit, then access time is controlled by t_{AA}.
13. These specifications are applied in the test mode.

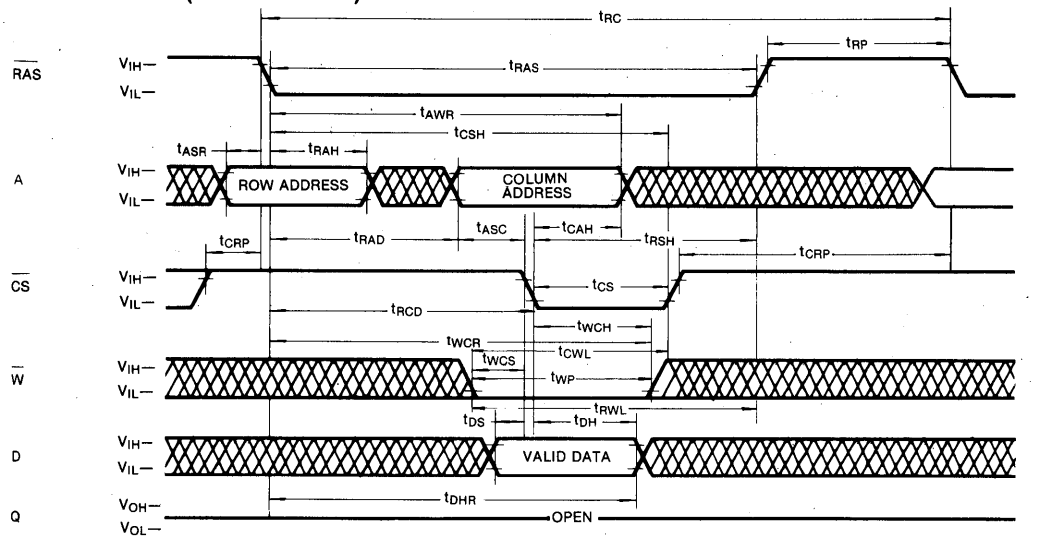
TIMING DIAGRAMS

READ CYCLE

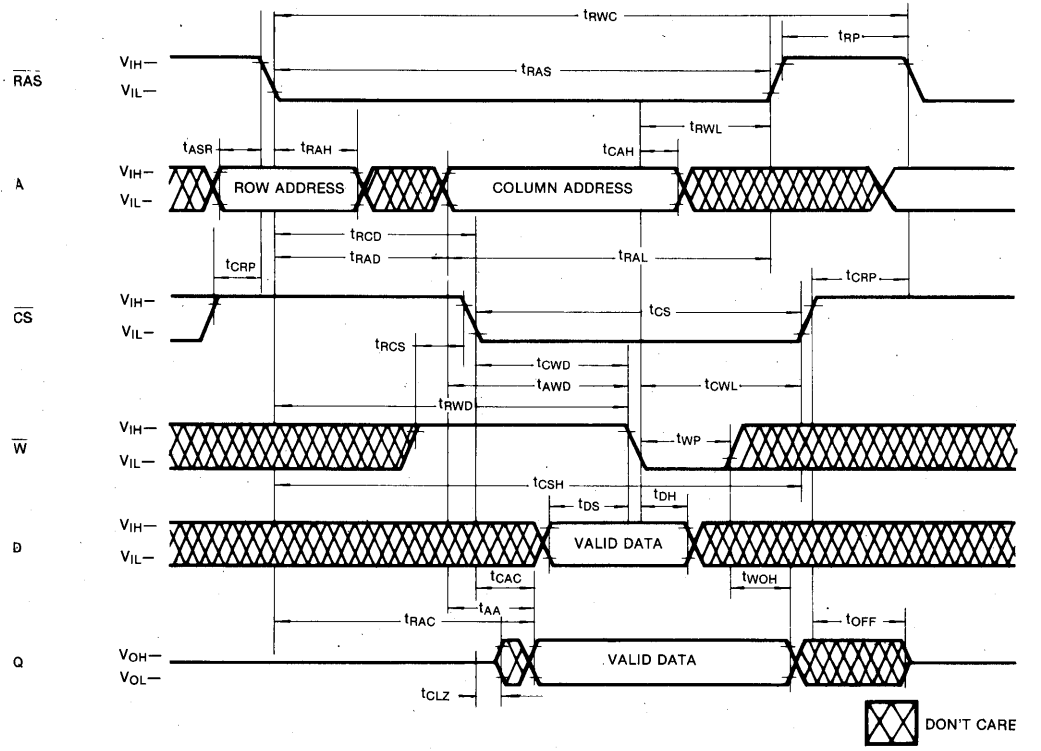


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

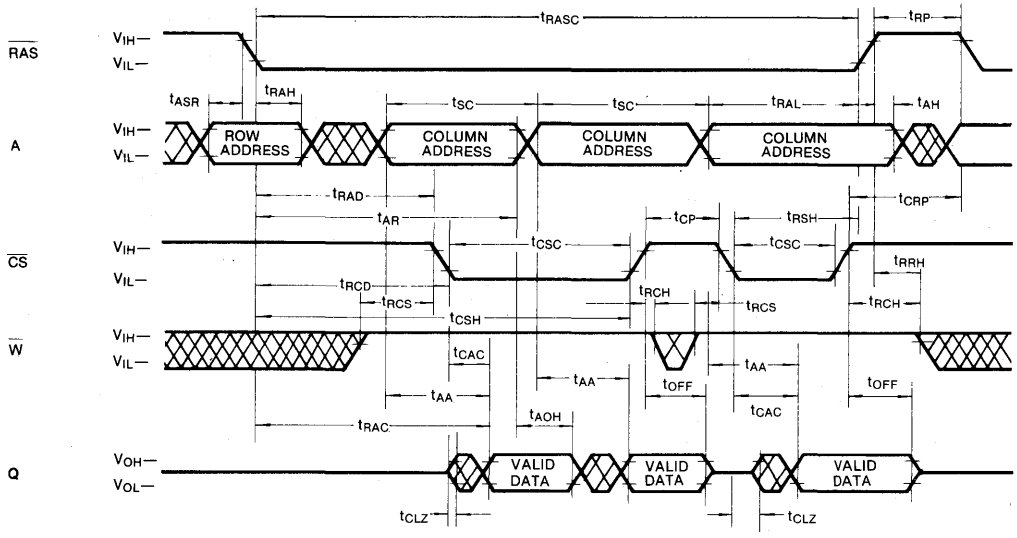


READ-WRITE/READ-MODIFY-WRITE CYCLE

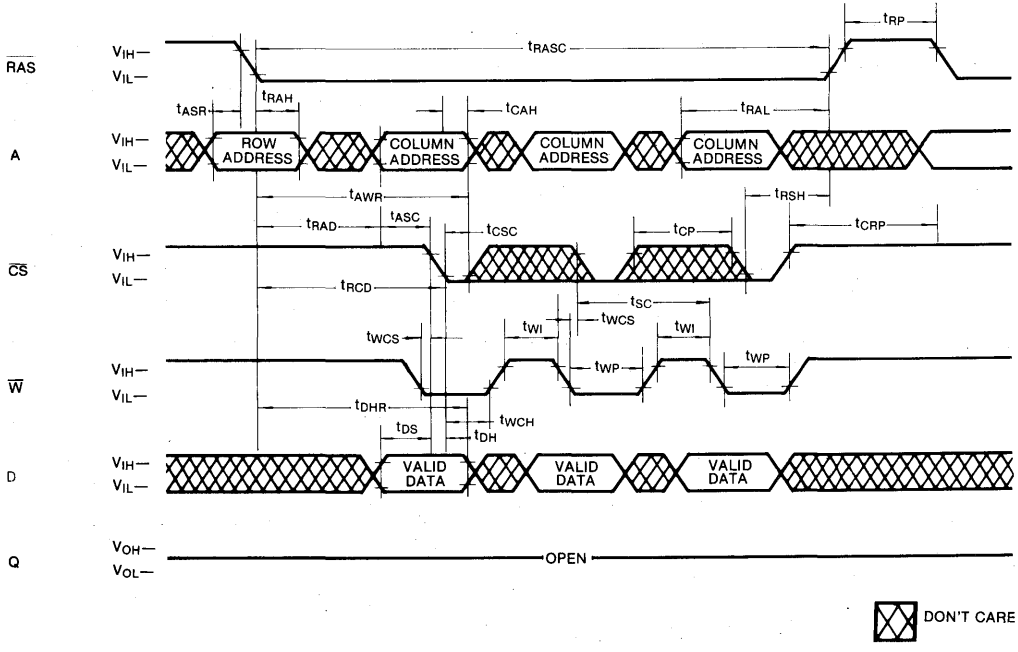


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ CYCLE



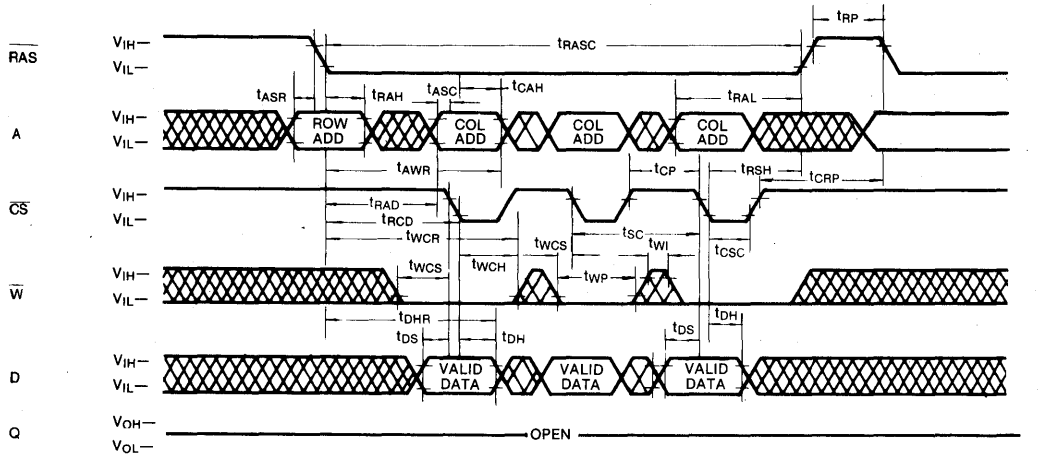
STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ controlled early write)



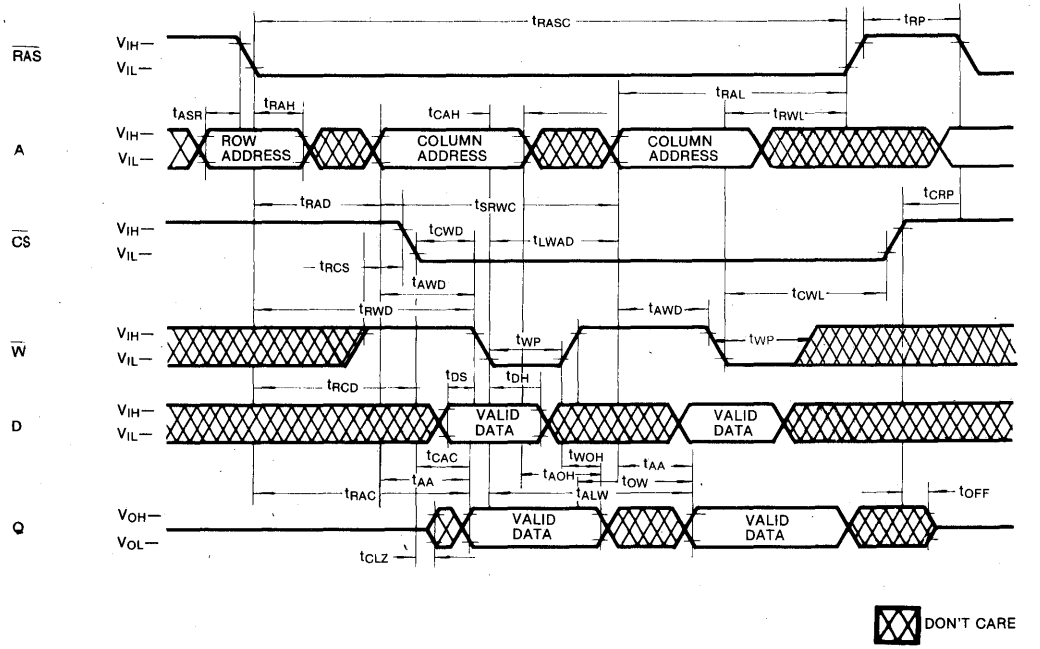
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)

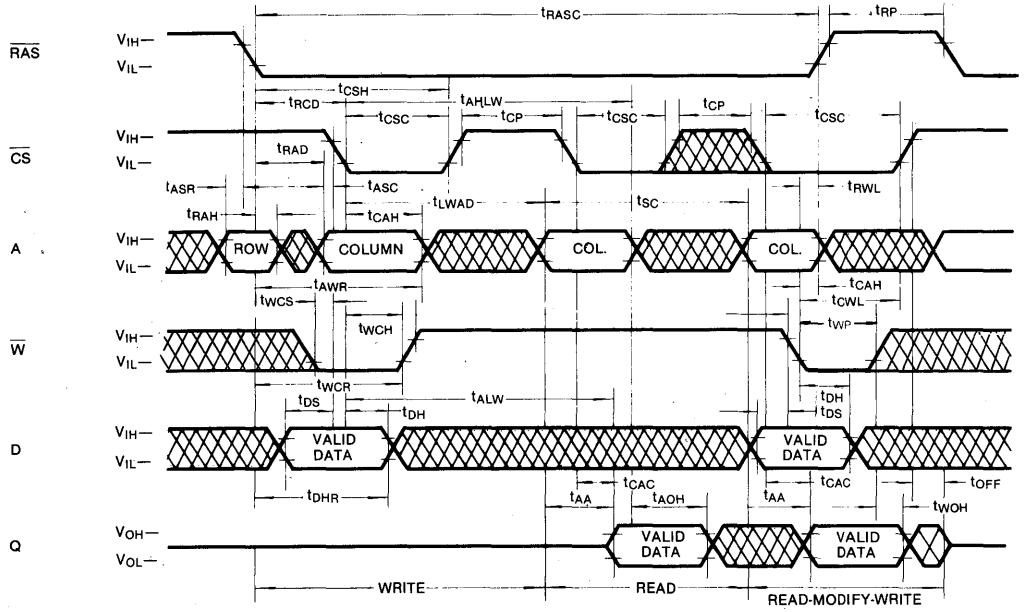


STATIC COLUMN MODE READ-WRITE CYCLE



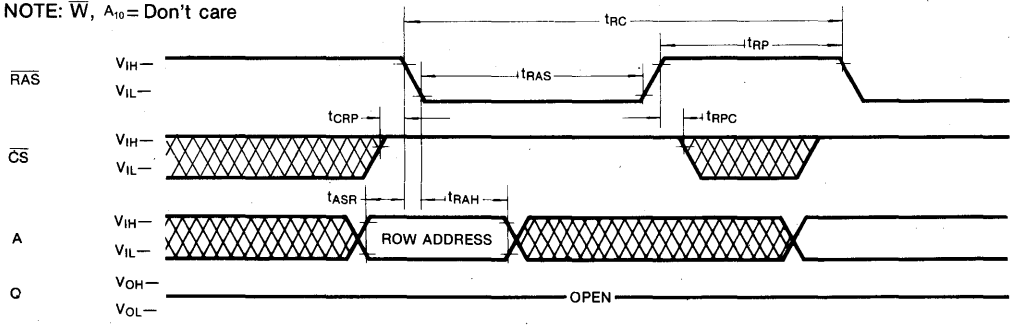
TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE MIXED CYCLE



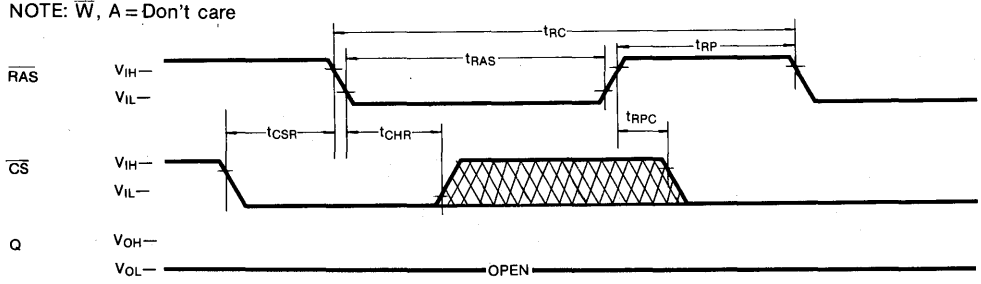
RAS-ONLY REFRESH CYCLE

NOTE: W, A_{10} = Don't care



CS-BEFORE-RAS REFRESH CYCLE

NOTE: W, A = Don't care

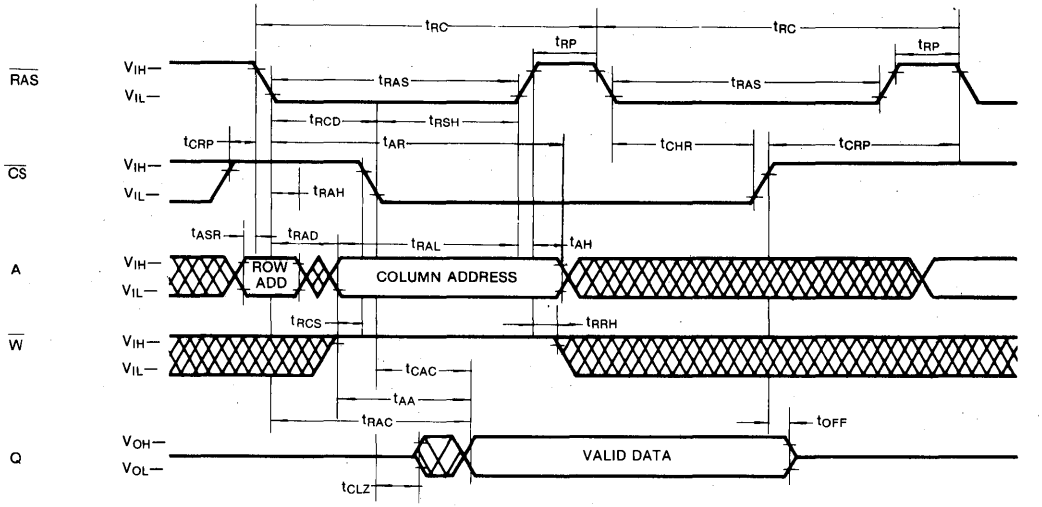


DON'T CARE

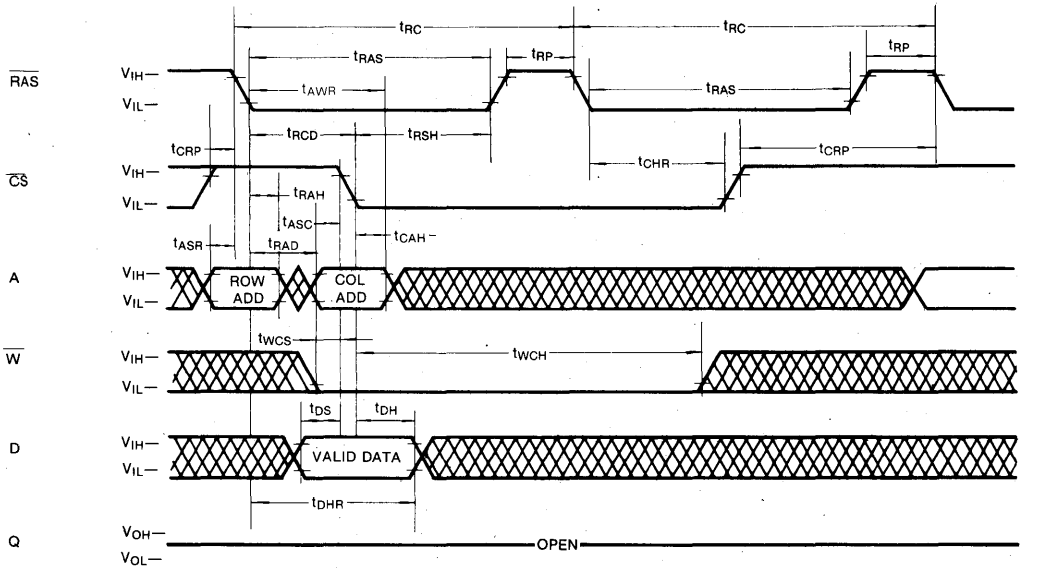
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



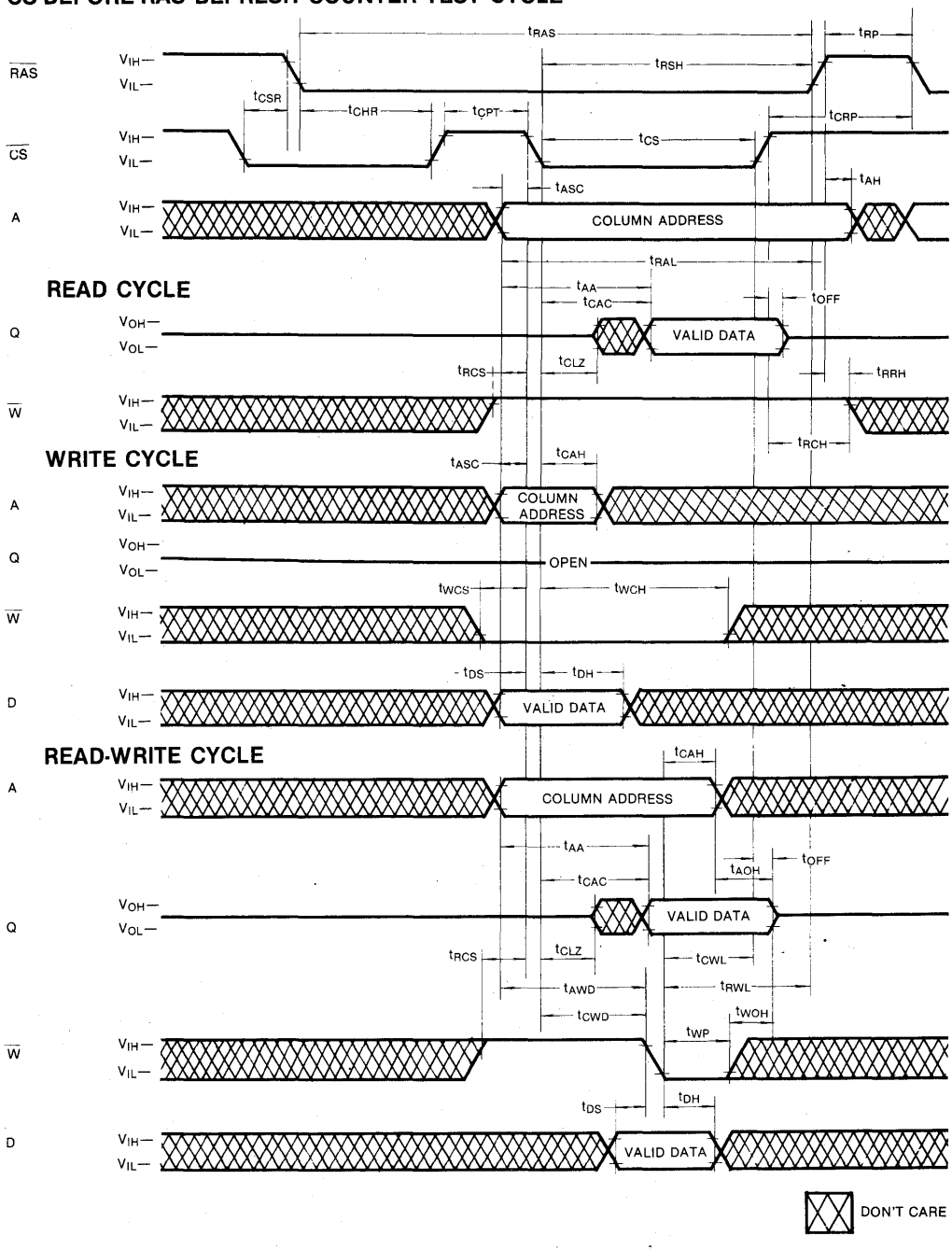
HIDDEN REFRESH CYCLE (WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

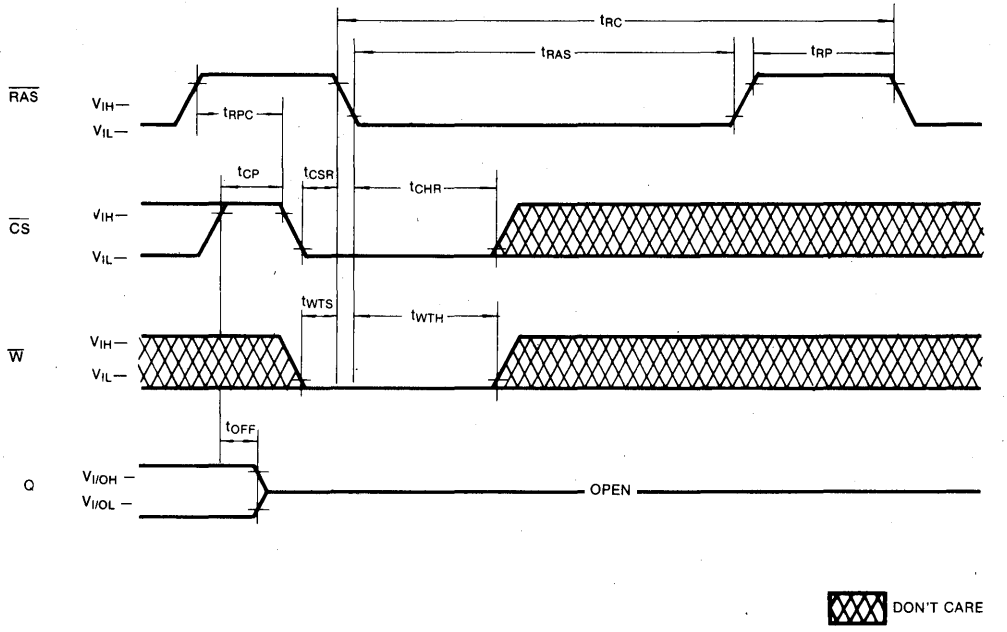
$\overline{CS}$-BEFORE-$\overline{RAS}$ BEFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM41C4002C is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}. A_{10C} and A_{0C} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0" In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM41C4002C contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4002C has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the chip select input($\overline{CS}$) and the valid row and column address inputs.

Operation of the KM41C4002C begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM41C4002C cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high sta5e. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4002C bigin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. If $\overline{CS}$ goes low before t_{RCD}(max), the access time to valid data is specified with respect to the falling edge of $\overline{RAS}$. But the addess time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM41C4002C can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CS}$. The data at the data input pin(D) is wirtten into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the daaressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, tCWD and tAWD are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4002C has a three-state output buffer which is controlled by $\overline{CS}$. Whenever $\overline{CS}$ is high(VIH) the output is in the high impedance(Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing paraneters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4002C operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Static Column Mode Read-Modify-Write.

DEVICE OPERATION (Continued)

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$-before-$\overline{RAS}$ Refresh, $\overline{CS}$-only cycle.
Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C4002C is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16ms. There are several ways to accomplish this.

$\overline{RAS}$-Only-Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each row.

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM41C4002C has $\overline{CS}$-Before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM41C4002C hidden refresh cycle is actually $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4002C by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantateous to perform refresh in this mammer but in gheneral $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

Static Column Mode

Static Column Mode allows high speed read, write or read-modity-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or readmodify-write cycles may be mixed in any order.
A Static Column mode read cycles starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{W}$=V_{IH} and $\overline{RAS}$=V_{IL}.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected ro are written by applying a new column address while $\overline{RAS}$=V_{IL} and toggiling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell trigered by the latter fallin edge of $\overline{W}$ or $\overline{CS}$.

$\overline{CS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-befofore-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CS}$-before-$\overline{RAS}$ refresh operation, is cs goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows.

Row Address — Bits A0 through A9 are supplied by the on-chip refresh counter. The A10 bit is set High internally.

Column Address — Bits A0 through A10 are strobed-in by the falling edge of $\overline{CS}$ as in a normal memory cycle.

Suggested $\overline{CS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. nitialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 512 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 512 times so that highs are written into the 512 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2,3 and 4

Power-up

If $\overline{RAS}$= V_{SS} during power-up, the KM41C4002C could begin an active cycle. This coundition results in higher than necessary current demands from the power supplu during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

DEVICE OPERATION (Continued)

An initial pause of 200μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C4002C inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short sa possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C4002C input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and verticaooy and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft erros). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.1μF ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM41C4002C using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C4002C and they supply much of the current used by the KM41C4002C during cycling.

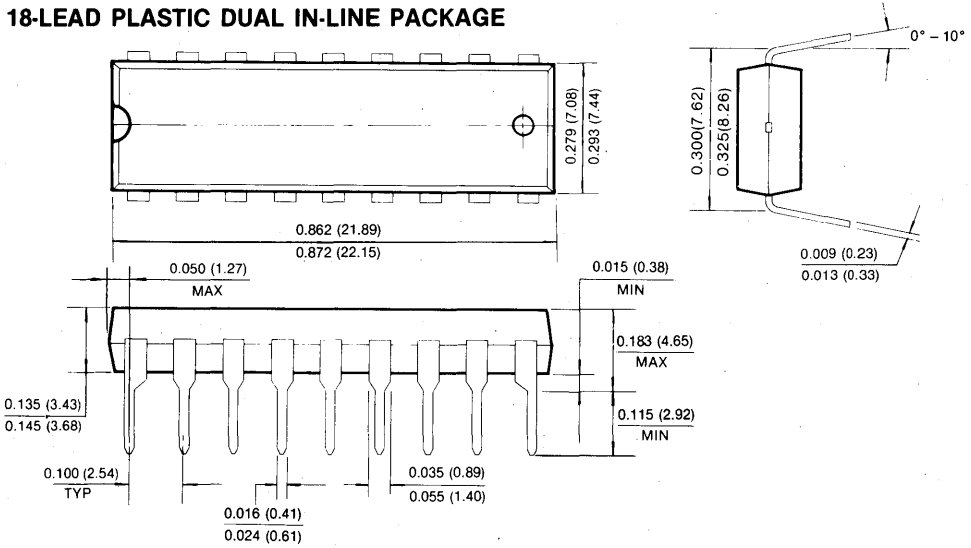
In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

3

PACKAGE DIMENSIONS

Units: Inches (Millimeters)

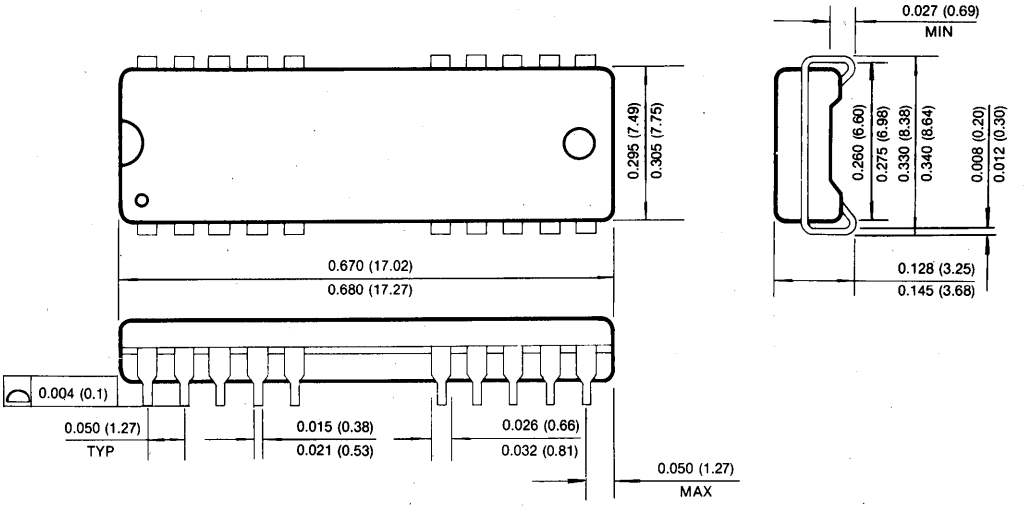
18-LEAD PLASTIC DUAL IN-LINE PACKAGE



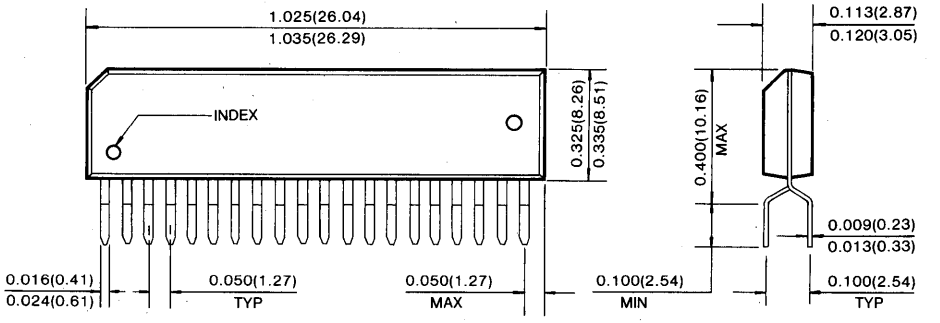
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

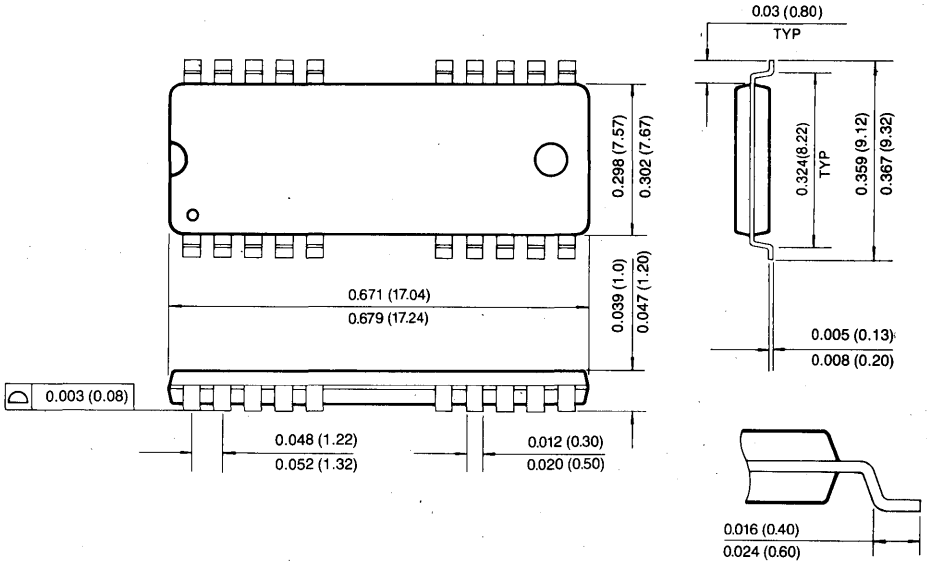


SAMSUNG ELECTRONICS

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



1M ×4Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM44C1000C/CL/CSL-5	50ns	13ns	90ns
KM44C1000C/CL/CSL-6	60ns	15ns	110ns
KM44C1000C/CL/CSL-7	70ns	20ns	130ns
KM44C1000C/CL/CSL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and hidden refresh capability**
- **Fast parallel test mode capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Single + 5V ±10% power supply**
- **Refresh Cycle**
  - **1024 cycle/16ms (Normal)**
  - **1024 cycle/128ms (L-version)**
  - **1024 cycle/256ms (SL-version)**
- **Power Dissipation**
  - **Standby: 5.5mW (Normal)**
    1.1mW (L-Ver.)
    0.55mW (SL-Ver.)
  - **Active (50/60/70/80): 470/415/360/305mW**
- **JEDEC standard pinout**
- **Available in plastic DIP,SOJ, ZIP and TSOP -II packages**

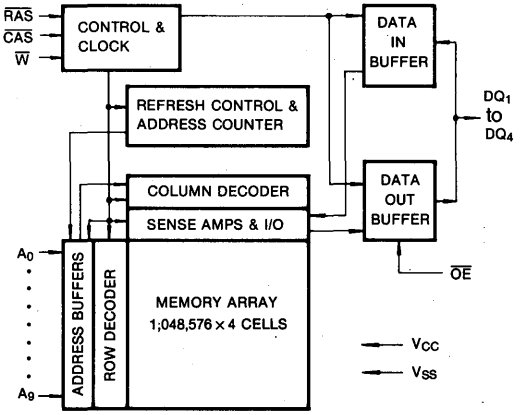
GENERAL DESCRIPTION

The Samsung KM44C1000C/CL/CSL is a high speed CMOS 1,048,576 × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1000C/CL/CSL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alterntive to $\overline{RAS}$-only Refresh. All inputs and outputs are fully TTL compatible.

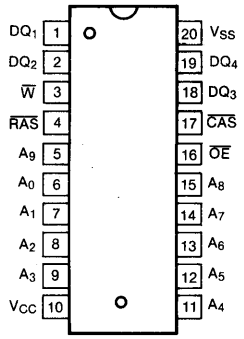
The KM44C1000C/CL/CSL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

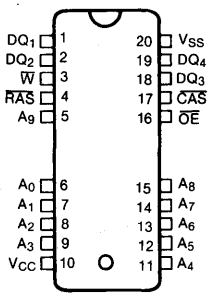


PIN CONFIGURATION (Top Views)

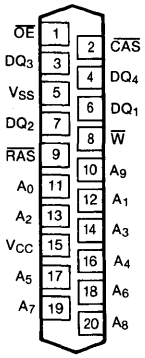
• KM44C1000CP/CLP/CSLP



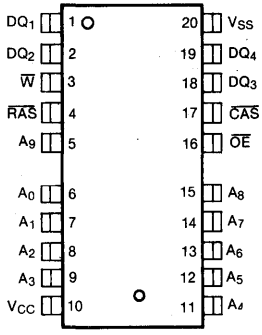
• KM44C1000CJ/CLJ/CSLJ



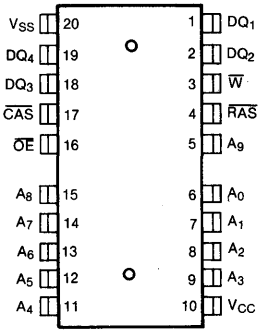
• KM44C1000CZ/CLZ/CSLZ



• KM44C1000CT/CLT/CSLT



• KM44C1000CTR/CLTR/CSLTR



Pin Names	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1~DQ_4	Data In/Data Out
V_{CC}	Power (+5V)
V_{SS}	Ground

3

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	℃
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	–	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	–	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	KM44C1000C/CL/CSL-5	I_{CC1}	-	85	mA
	KM44C1000C/CL/CSL-6		-	75	mA
	KM44C1000C/CL/CSL-7		-	65	mA
	KM44C1000C/CL/CSL-8		-	55	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @tRC=min.)	KM44C1000C/CL/CSL-5	I_{CC3}	-	85	mA
	KM44C1000C/CL/CSL-6		-	75	mA
	KM44C1000C/CL/CSL-7		-	65	mA
	KM44C1000C/CL/CSL-8		-	55	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @tPC=min.)	KM44C1000C/CL/CSL-5	I_{CC4}	-	65	mA
	KM44C1000C/CL/CSL-6		-	55	mA
	KM44C1000C/CL/CSL-7		-	45	mA
	KM44C1000C/CL/CSL-8		-	35	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC} -0.2V)	KM44C1000C	I_{CC5}	-	1	mA
	KM44C1000CL		-	200	μA
	KM44C1000CSL		-	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	KM44C1000C/CL/CSL-5	I_{CC6}	-	85	mA
	KM44C1000C/CL/CSL-6		-	75	mA
	KM44C1000C/CL/CSL-7		-	65	mA
	KM44C1000C/CL/CSL-8		-	55	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ_{1-4}=Don't Care, T_{RC}=125μs(L-Ver.) T_{RC}=250μs(SL-Ver.), T_{RAS}=T_{RAS} min~300ns	KM44C1000CL	I_{CC7}	-	300	μA
	KM44C1000CSL		-	150	μA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}+0.5V$ all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

* Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}=V_{IL}$. I_{CC4}, Address can be changed maximum once during a fast page Mode cycle.

CAPACITANCE (T_A=25° C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	–	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	–	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{DQ}	–	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	7
Transition time(rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10.000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	
Data-in-set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		10		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Refresh period (SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast page mode cycle time	tPC	35		40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	
$\overline{RAS}$ pulse width(Fast Page Mode)	tRASP	50	200,000	60	200,000	70	200,000	80	200,000	ns	
$\overline{CAS}$ precharge time(Fast page mode)	tCP	10		10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command hold time (test mode in)	tWTH	10		10		10		10		ns	
Write command gold time (test mode in)	tWPH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ rcycle)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ rcycle)	tWRH	10		10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

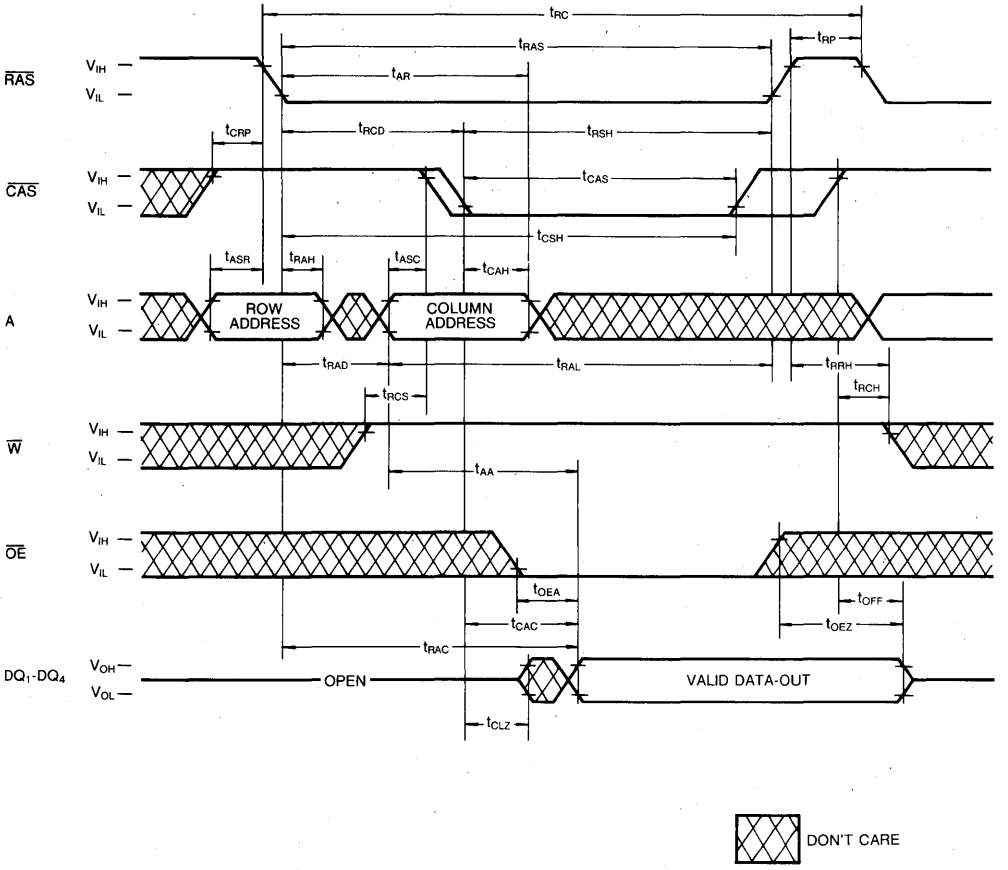
Parameter	Symbol	-5		-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	95		115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	138		160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		18		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		45		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	41		45		55		55		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	53		60		70		75		ns	8
Fast mode cycle time	t_{PC}	40		45		50		55		ns	
Fast page mode read-modefy-write	t_{PRWC}	81		85		100		105		ns	
$\overline{RAS}$ pulse width(Fast page mode)	t_{RASP}	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45		50	ns	3
$\overline{OE}$ access time	t_{OEA}		20		20		25		25	ns	
$\overline{OE}$ to data delay	t_{OED}	18		20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	18		20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If $t_{RCD(max)}$ is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data our will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

TIMING DIAGRAMS

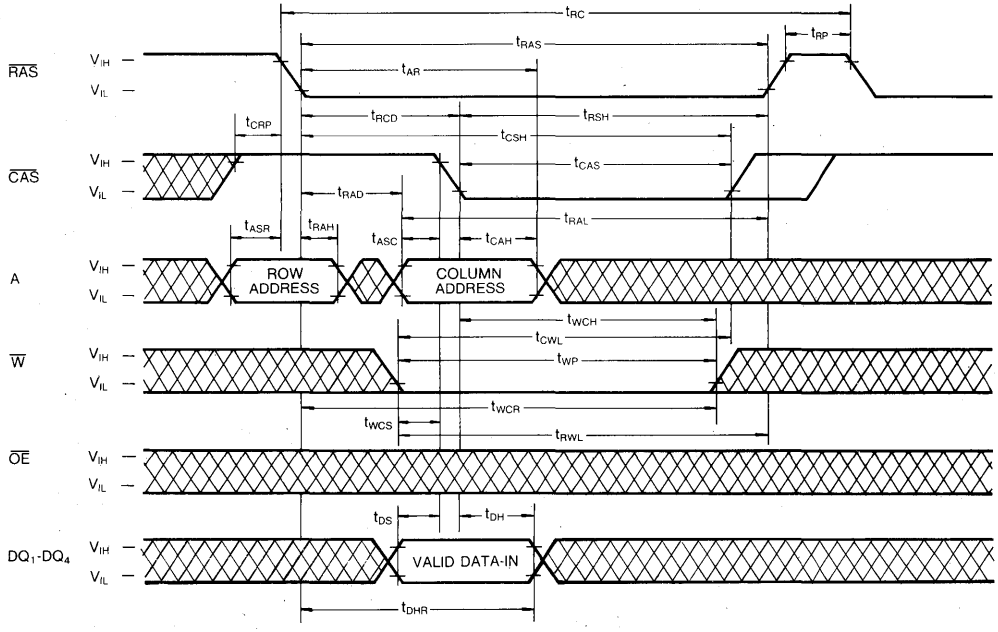
READ CYCLE



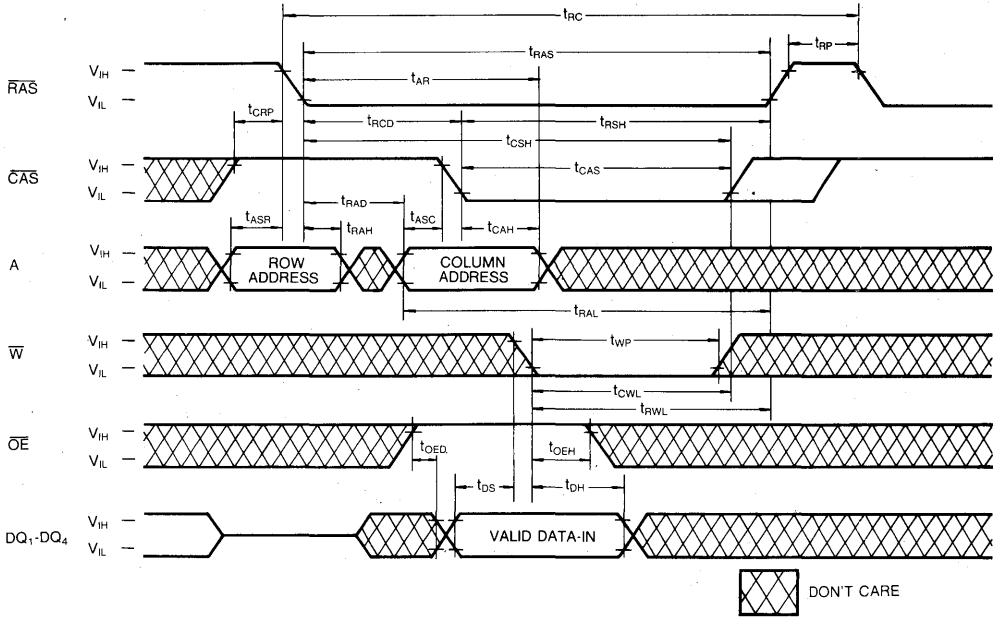
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)

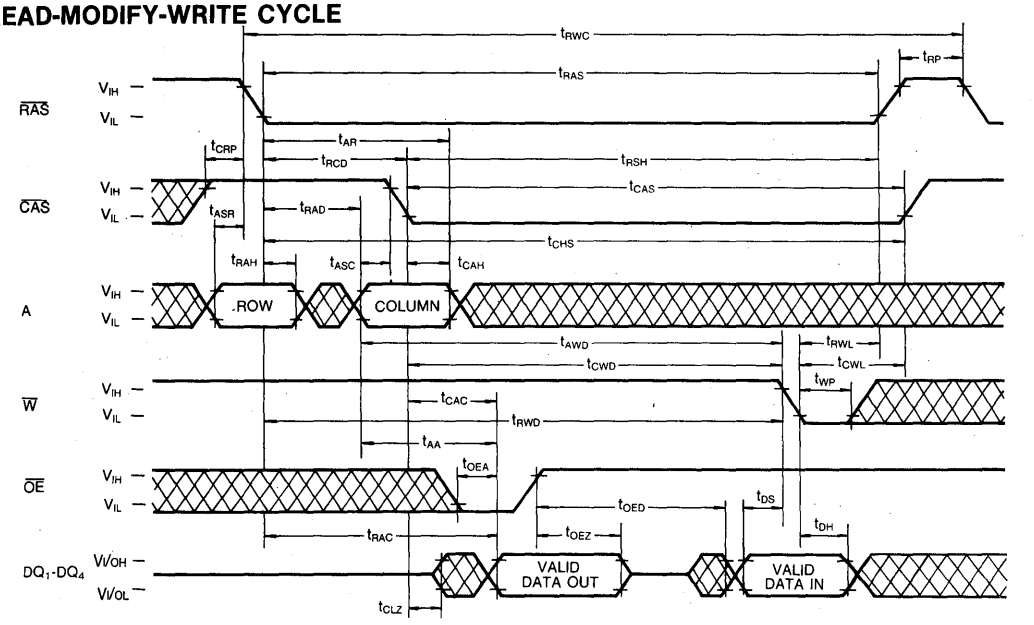


WRITE CYCLE (OE CONTROLLED WRITE)

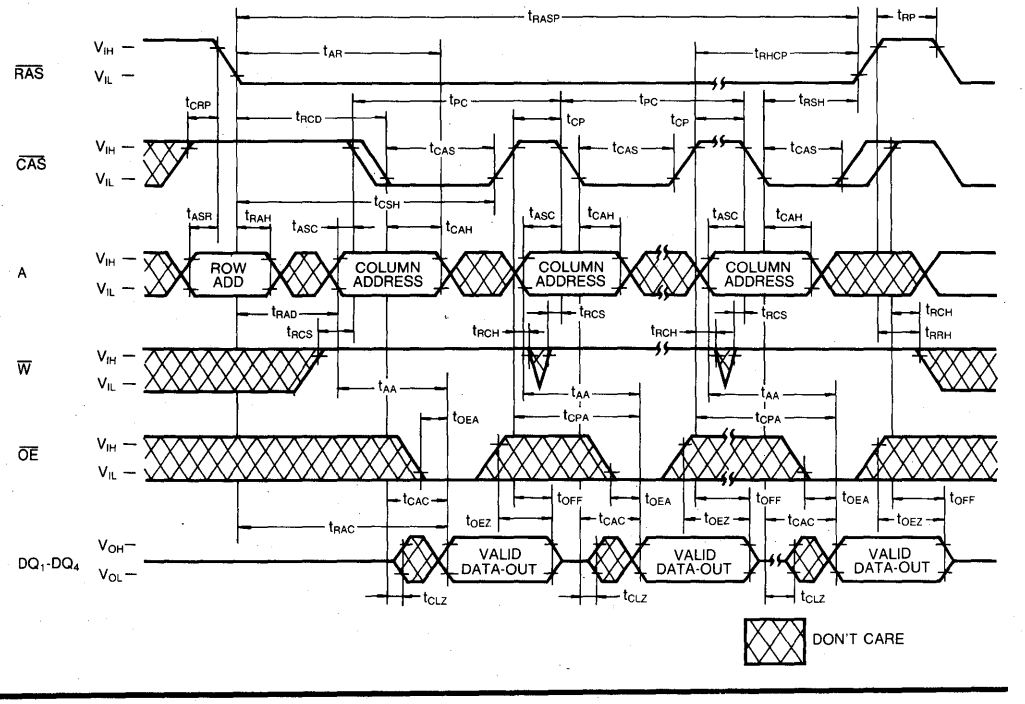


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



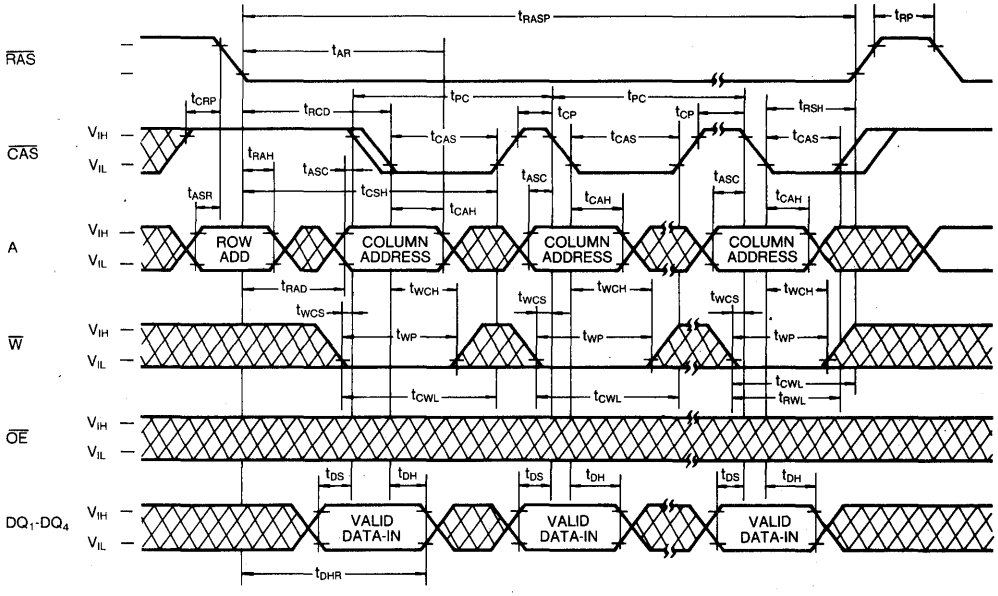
FAST PAGE MODE READ CYCLE



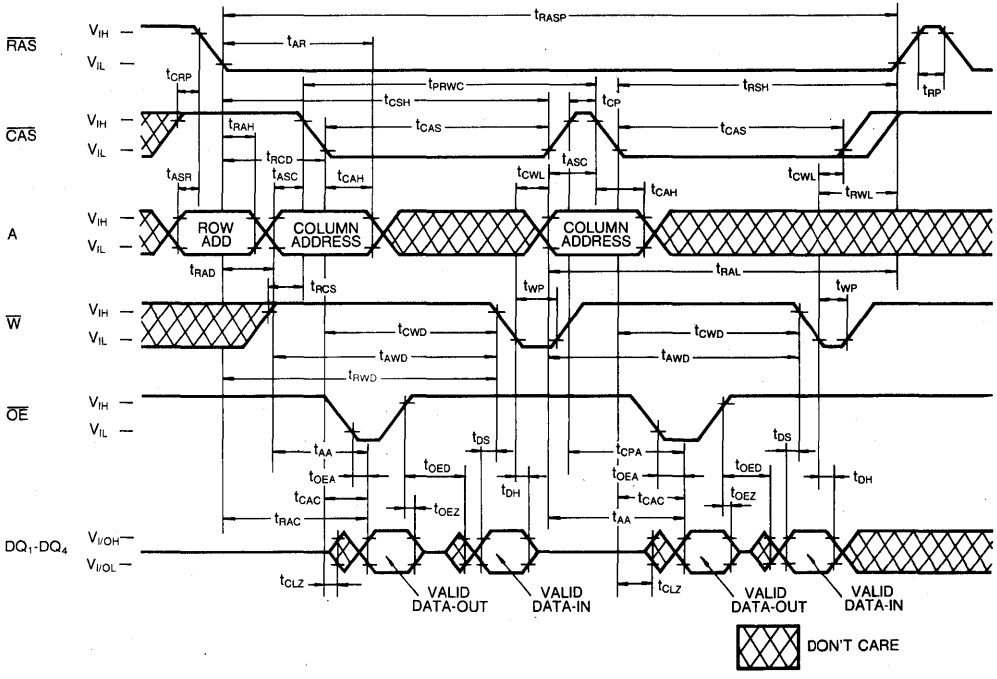
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

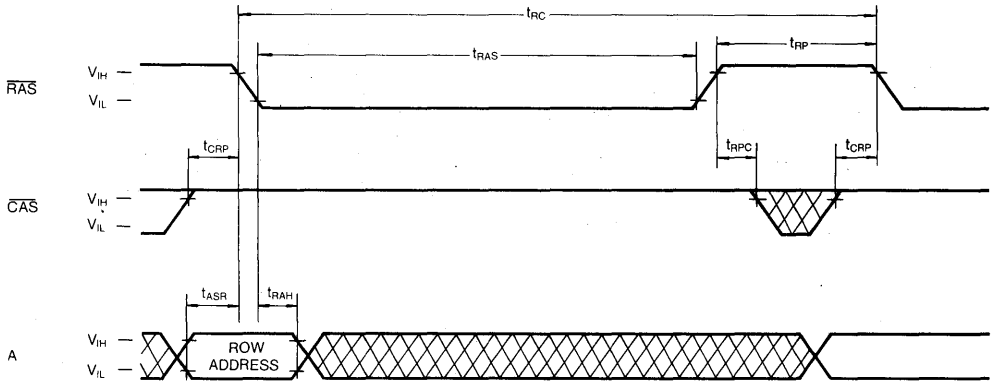


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

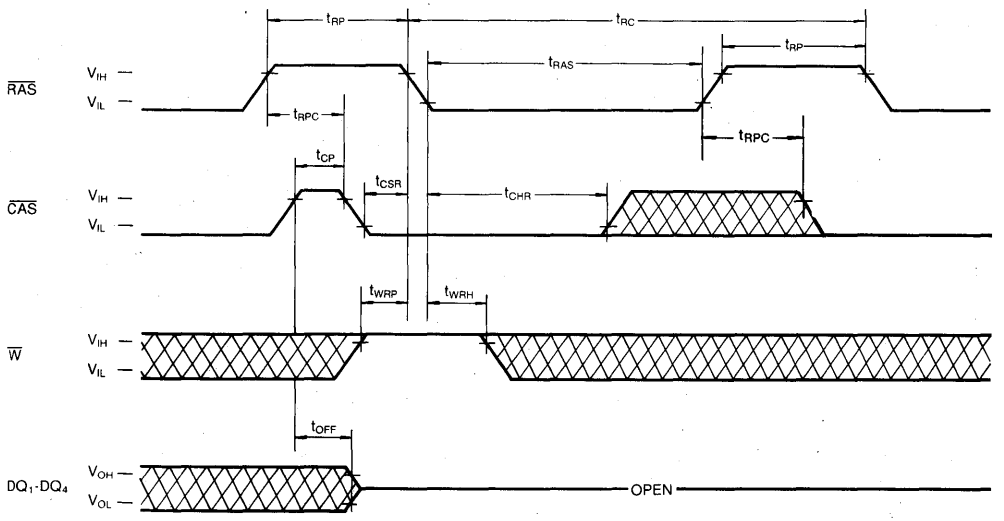
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



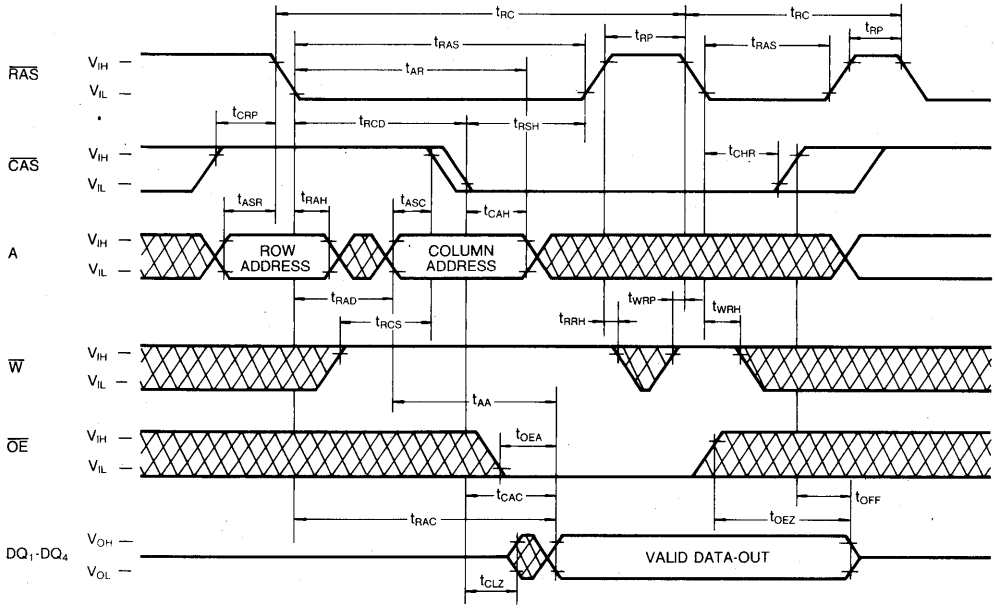
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{OE}$, Address=Don't Care

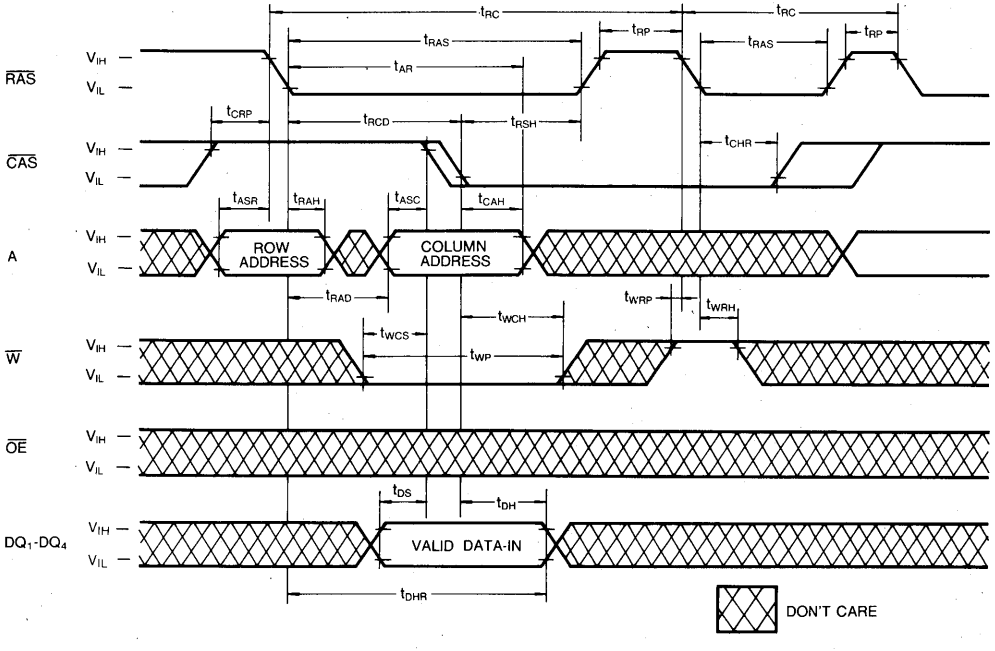


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



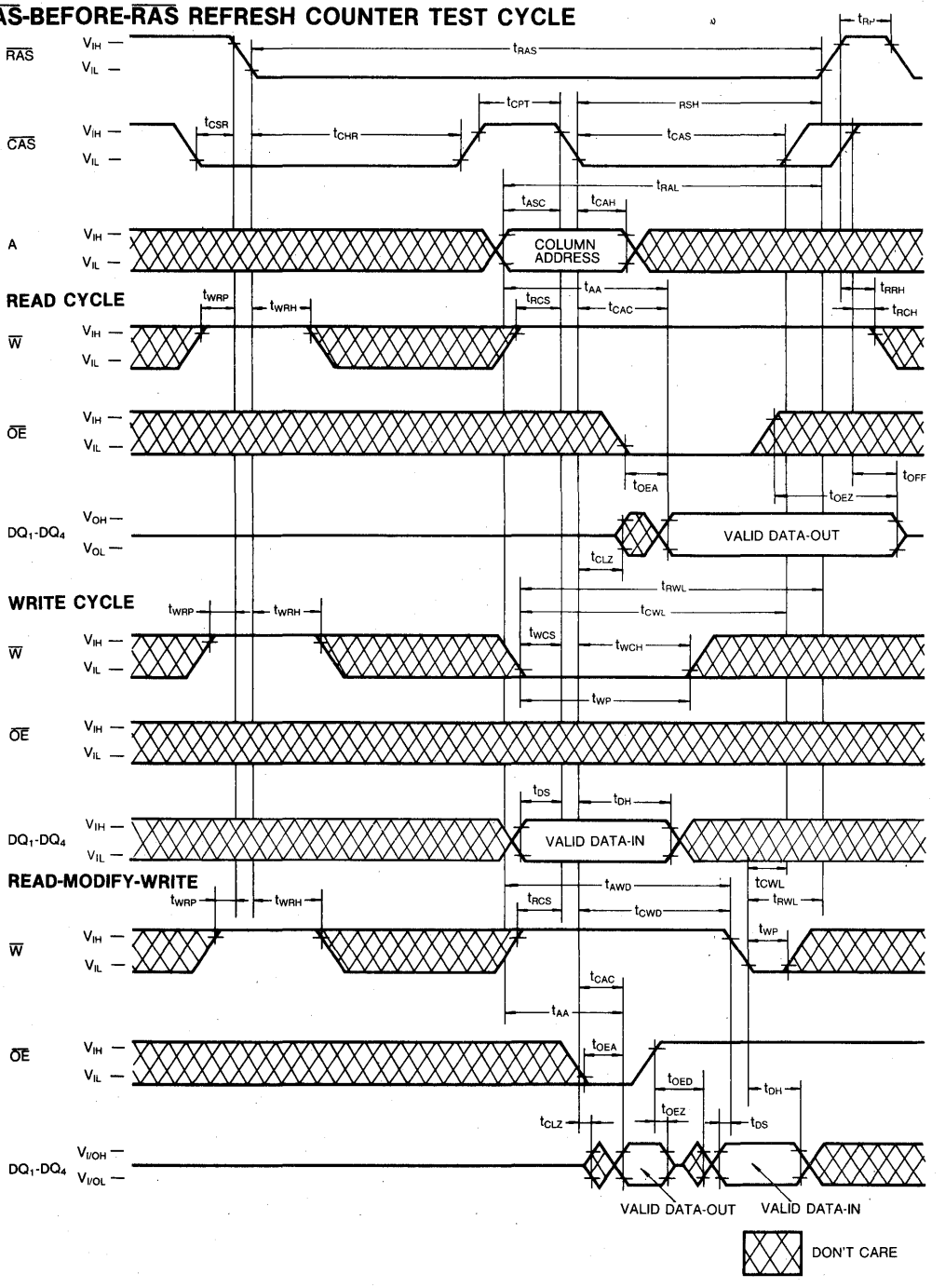
HIDDEN REFRESH CYCLE (WRITE)



SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

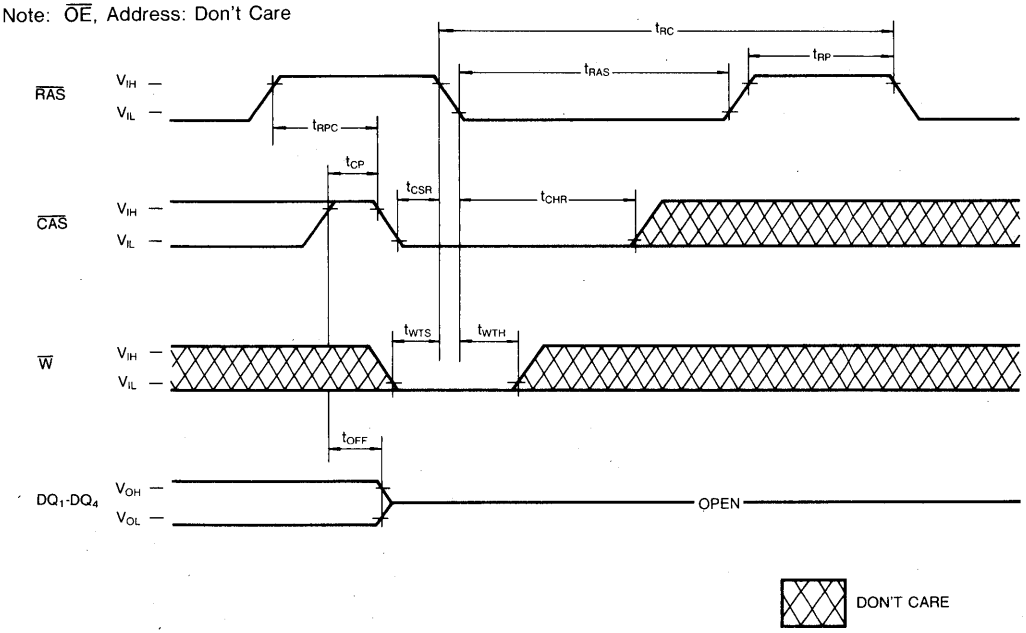


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



TEST MODE DESCRIPTION

The KM44C1000C/CL/CSL is the RAM organized 1,048,576 words by 4 bit internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M x 4 DRAM can be tested as if it were a 512K x 4DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode", And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only-Refresh Cycle" puts it back into "Normal Mode". During the test mode operation, a WCBR cycle is used to perform refresh. The "Test Mode" function reduces test time(1/2 in cases of N test pattern.)

DEVICE OPERATION

The KM44C1000C/CL/CSL contains 4,194,304 memory locations. Twenty address bit are required to address a particular 4-bit word in the memory array. Since the KM44C1000C/CL/CSL has only 10 address input pins, time multiplexed addressing is used to input 10 row (A_0-A_9) and 10 column (A_0-A_9) address. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column adress strobe($\overline{CAS}$), and the valid row and column address inputs.

Operating of the KM44C1000C/CL/CSL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins (A_0-A_9) is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C1000C/CL/CSL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1000C/CL/CSL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid befor t_{RCD}(max), the access time to valid data is specified by t_{RAC}(min). However if $\overline{CAS}$ goes low after t_{RCD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC} (min), it is necessary to meet both t_{RCD}(max) and t_{RAD} (max). The KM44C1000C/CL/CSL has common data I/O pins

The this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the output, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C1000C/CL/CSL can perform eary write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the three state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing W low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur, The late write cycle is very simiar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C1000C/CL/CSL has a three-state output buffer which is controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever $\overline{CAS}$ and $\overline{OE}$ are high(V_{IH}), the outputs are in the high impedance state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output untill $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1000C/CL/CSL operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write(t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM44C1000C/CL/CSL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16/128/256ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C1000C/CL/CSL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is vheld low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C1000C/CL/CSL hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1000C/CL/CSL by using read, write or read-modify write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order.

A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time requried to set up and strobe sequential row addresses for the same page

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CAS}$ goes high and then low again while RAS is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell be addressed with 10 row address bits and 10 column address bits defined as follows

Row Address- Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address-Bits A_0 through A_9 are supplied by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address (The row addresses are supplied by the on-chip refresh counter)
3. Using read-modify-write cycle, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS}$=V_{SS} during power-up, the KM44C1000C/CL/CSL cold possibly begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current. An initial pause of 200 μsec is required after

DEVICE OPERATION (Continued)

power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 16(L-ver:128, SL-ver:256) msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C1000C/CL/CSL inputs act like unteminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terrminate the input lines and to keep them as short as possible. Although eiter series or parallel temination may be used,series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C1000C/CL/CSL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is importnat to lay out the power and ground lines on memory boards in such a way that switching transinent effects are mimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS.

The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV

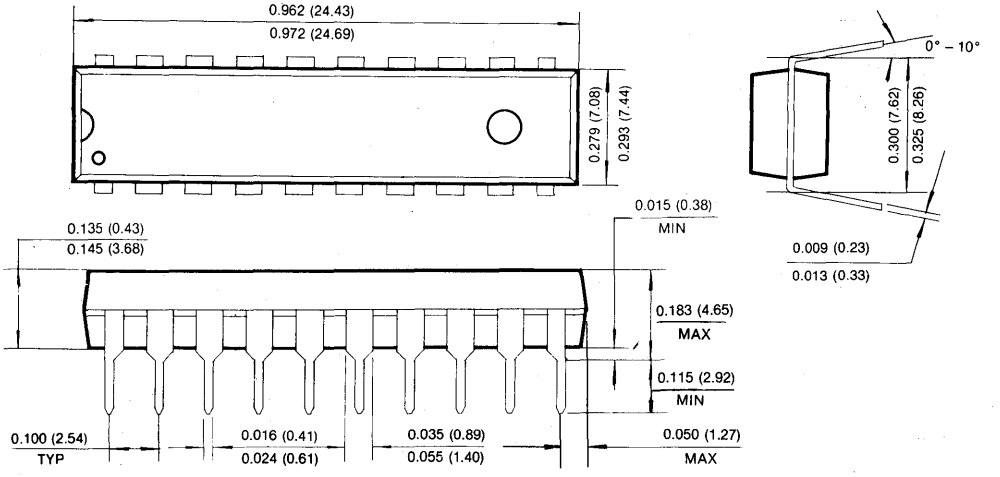
A high frequency 0.1 μF ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM44C1000C/CL/CSL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C1000C/CL/CSL and they supply much of the current used by the KM44C1000C/CL/CSL during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

Units: Inches (Millimeters)

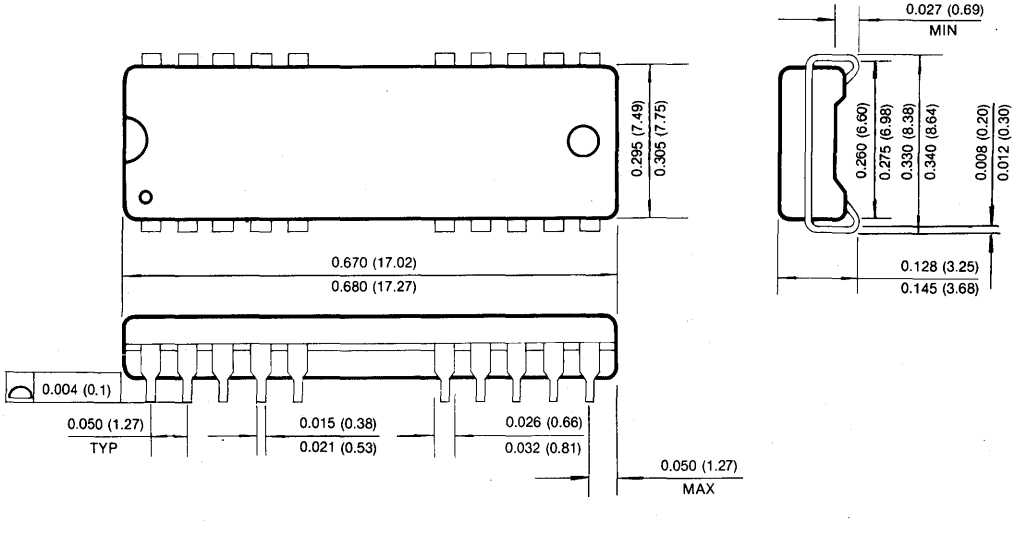
20-LEAD PLASTIC DUAL IN-LINE PACKAGE



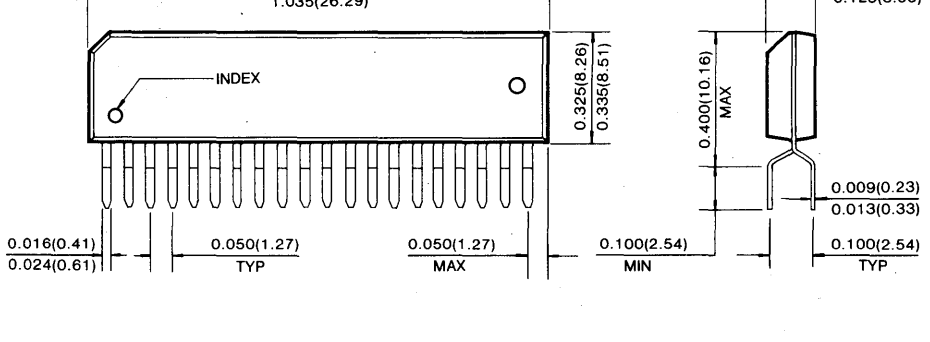
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



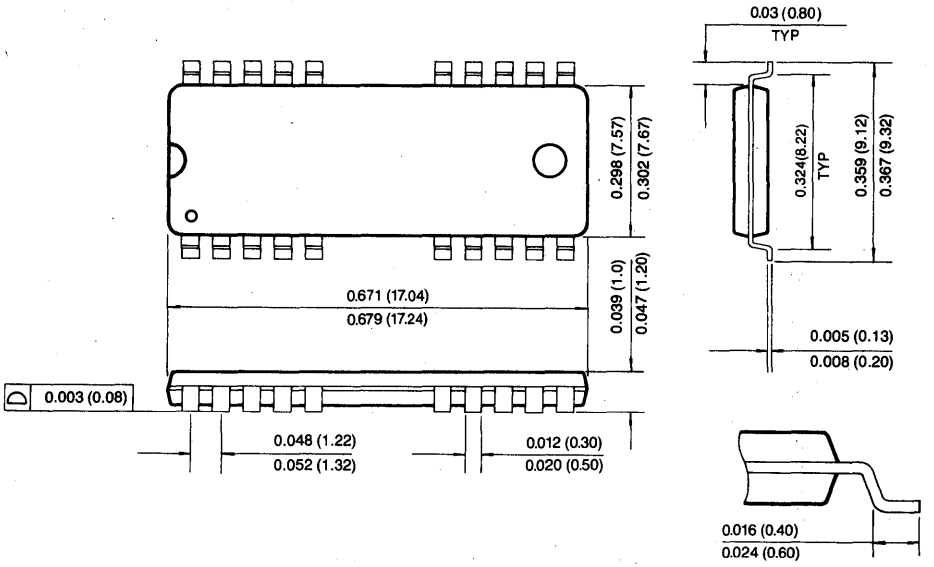
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



1M ×4 Bit CMOS Dynamic RAM with Fast Page Mode (Write Per Bit Mode)

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM44C1010C-5	50ns	13ns	90ns
KM44C1010C-6	60ns	15ns	110ns
KM44C1010C-7	70ns	20ns	130ns
KM44C1010C-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Write Per Bit Mode Capabillity**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early Write or Output Enable Controlled Write**
- **Singple +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in plastic DIP, SOP ZIJ and TSOP(II) Packages**

GENERAL DESCRIPTION

The Samsung KM44C1010C is a high speed CMOS 1,048,576×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

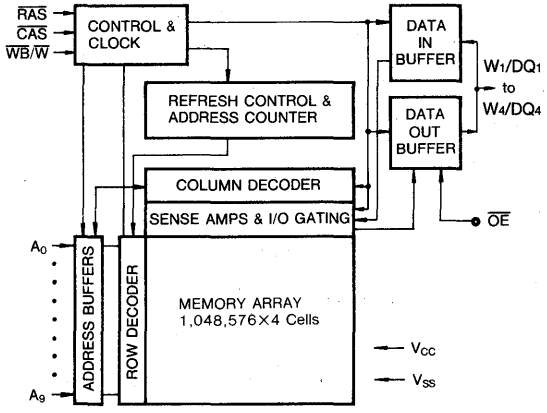
The KM44C1010C features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C1010C is fabricated using Samsung's advanced CMOS process.

3

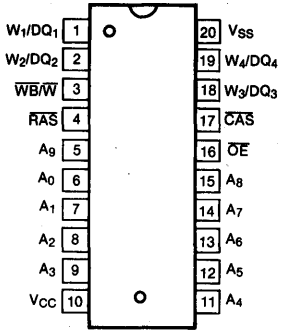
FUNCTIONAL BLOCK DIAGRAM



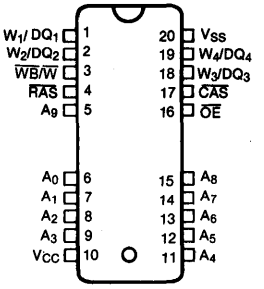
SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top Views)

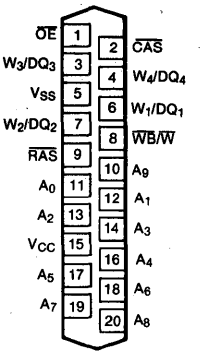
• KM44C1010CP



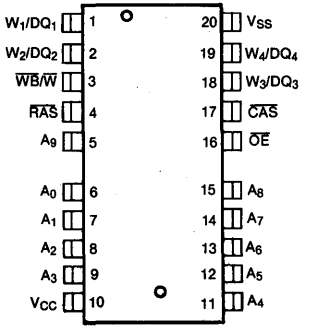
• KM44C1010CJ



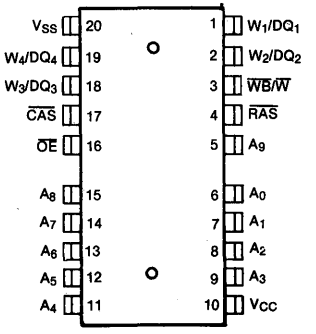
• KM44C1010CZ



• KM44C1010CT



• KM44C1010CTR



Pin Names	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB/W}$	Write per bit/Read/ Write input
$\overline{OE}$	Data Output Enable
W_1/DQ_1 ~ W_4/DQ_4	Write select/ Data In/Out
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C1010C-5	I_{CC1}	-	85	mA
	KM44C1010C-6		-	75	mA
	KM44C1010C-7		-	65	mA
	KM44C1010C-8		-	55	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{WB}$/$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44C1010C-5	I_{CC3}	-	85	mA
	KM44C1010C-6		-	75	mA
	KM44C1010C-7		-	65	mA
	KM44C1010C-8		-	55	mA
Standby Column Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44C1010C-5	I_{CC4}	-	65	mA
	KM44C1010C-6		-	55	mA
	KM44C1010C-7		-	45	mA
	KM44C1010C-8		-	35	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{WB}$/$\overline{W}$=V_{CC}-0.2V)		I_{CC5}	-	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C1010C-5	I_{CC6}	-	85	mA
	KM44C1010C-6		-	75	mA
	KM44C1010C-7		-	65	mA
	KM44C1010C-8		-	55	mA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. I_{CC1}, I_{CC3}, I_{CC6} Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once during a Fast Page mode cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB/W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (W_1/DQ_1~W_4/DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Fast page mode cycle time	t_{PC}	30		40		45		50		ns	
Fast page mode read-write cycle time	t_{PRWC}	76		85		100		105		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width(fast page mode)	t_{RASC}	50	200,000	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold	t_{CAH}	10		10		15		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		15		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command hold time referenced to $\overline{RAS}$	tWCRt	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	
Data-in set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		10		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	6
Refresh period	tREF		16		16		16		16	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	tAWD	40		55		65		70		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	tCPT	20		20		25		30		ns	
Write command set-up time (test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	tWRH	10		10		10		10		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write per bit set-up time	tWBS	0		0		0		0		ns	
Write per bit hold time	tWBH	10		10		10		15		ns	
Write per bit selection set-up time	tWDS	0		0		0		0		ns	
Write per bit selection hold time	tWDH	10		10		10		15		ns	

TEST MODE CYCLE

(Note.12)

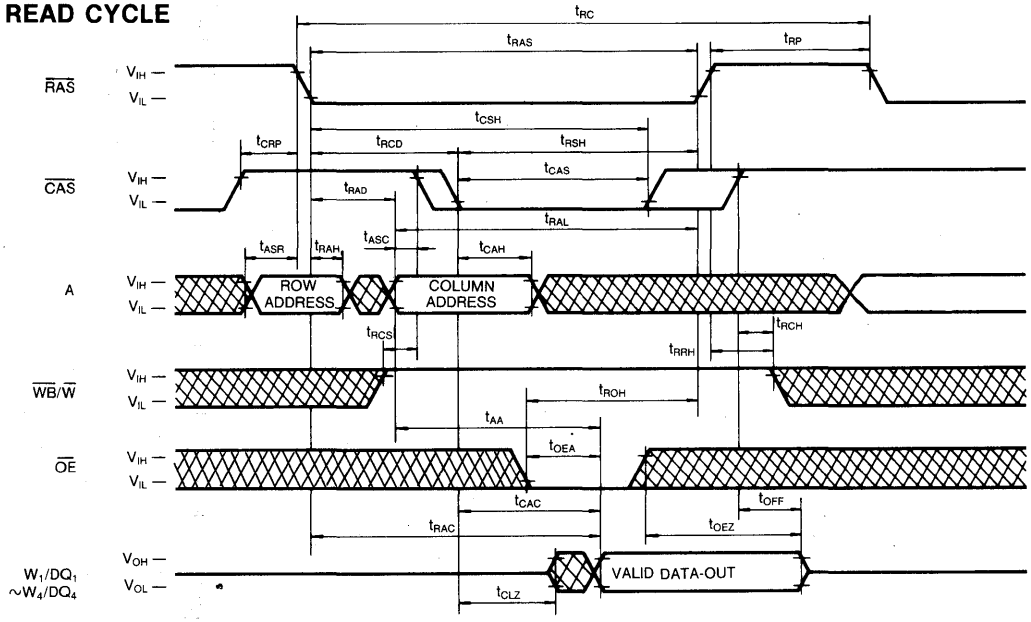
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	95		115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	138		160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		55		65		75		85	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		18		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		45		ns	
$\overline{CAS}$ to Write enable delay	t_{CWD}	41		45		55		55		ns	8
$\overline{RAS}$ to Write enable delay	t_{RWD}	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	53		60		70		75		ns	8
Fast mode cycle time	t_{PC}	40		45		50		55		ns	
Fast page mode read-modiy-write	t_{PRWC}	81		85		100		105		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45		50	ns	3
$\overline{OE}$ access time	t_{OEA}		20		20		25		25	ns	
$\overline{OE}$ to data delay	t_{OED}	18		20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	18		20		25		25		ns	

NOTES

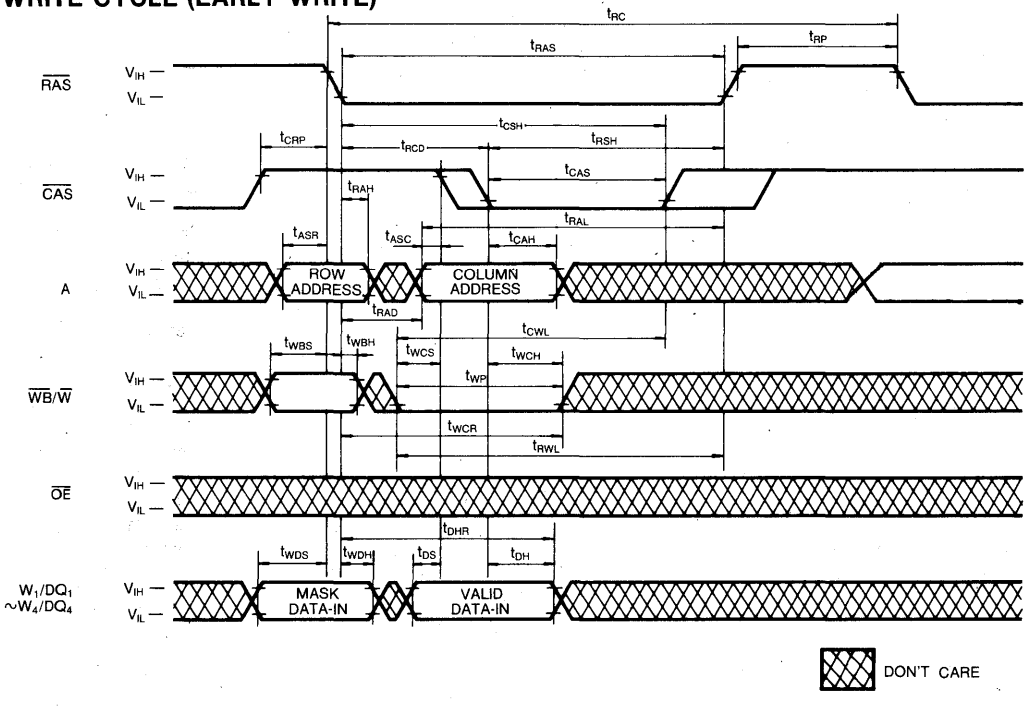
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \leq t_{RCD}$(max).
6. t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC} (max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE



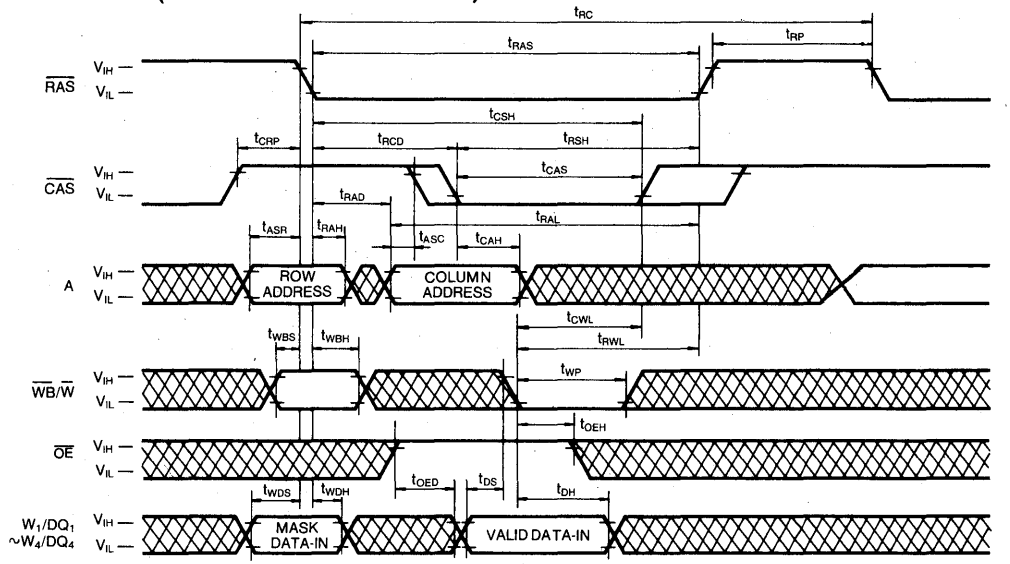
WRITE CYCLE (EARLY WRITE)



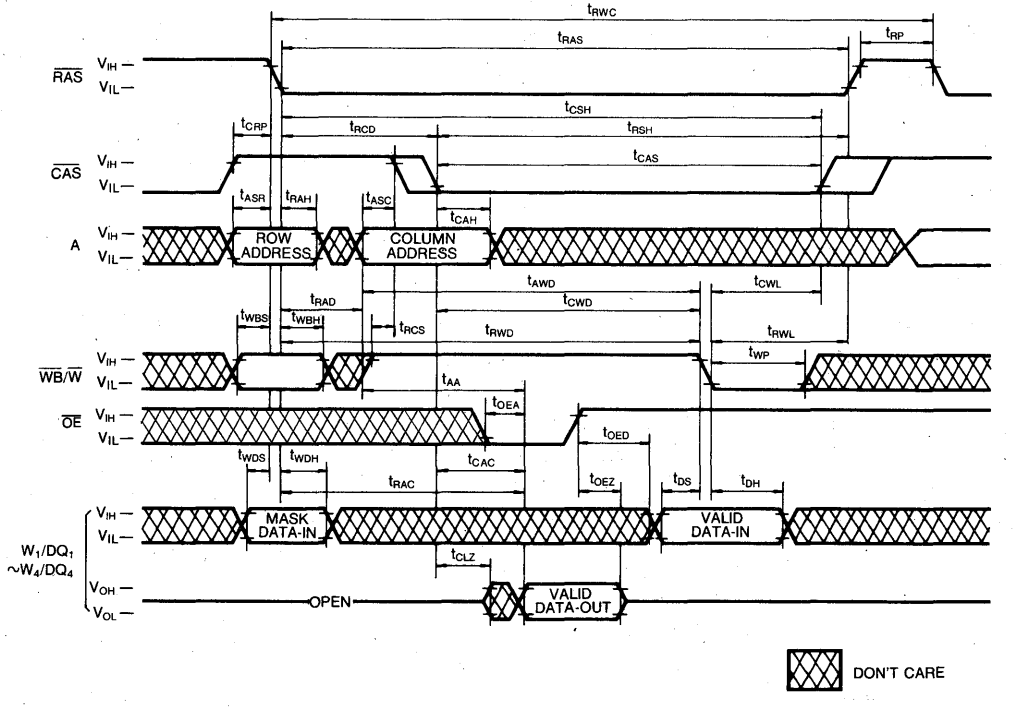
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

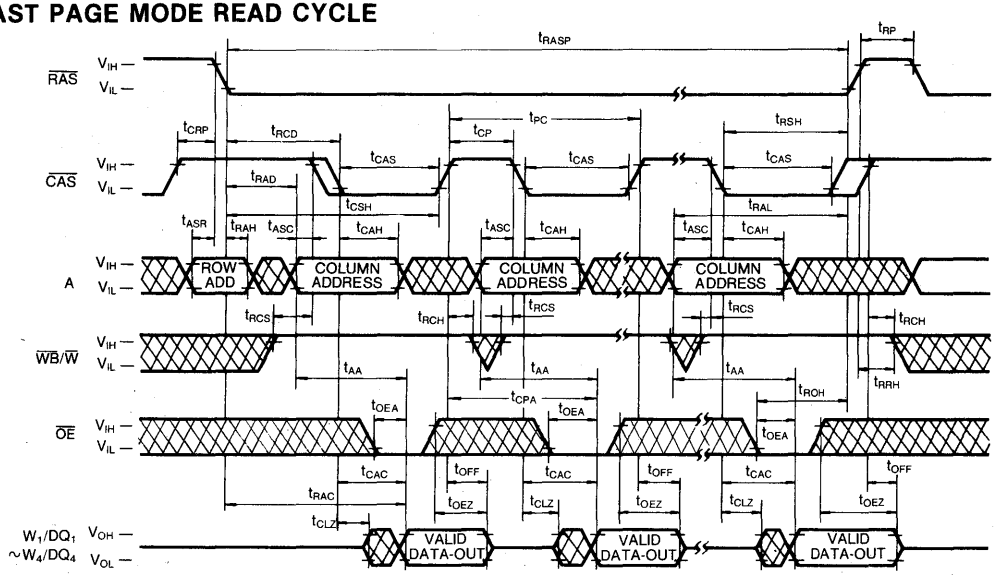


READ-MODIFY-WRITE CYCLE

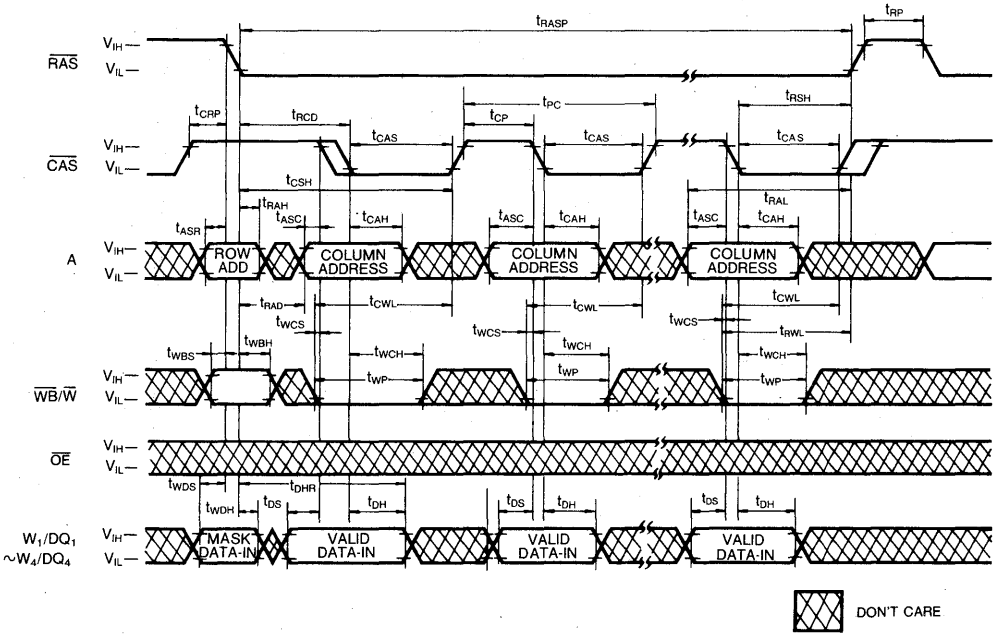


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE

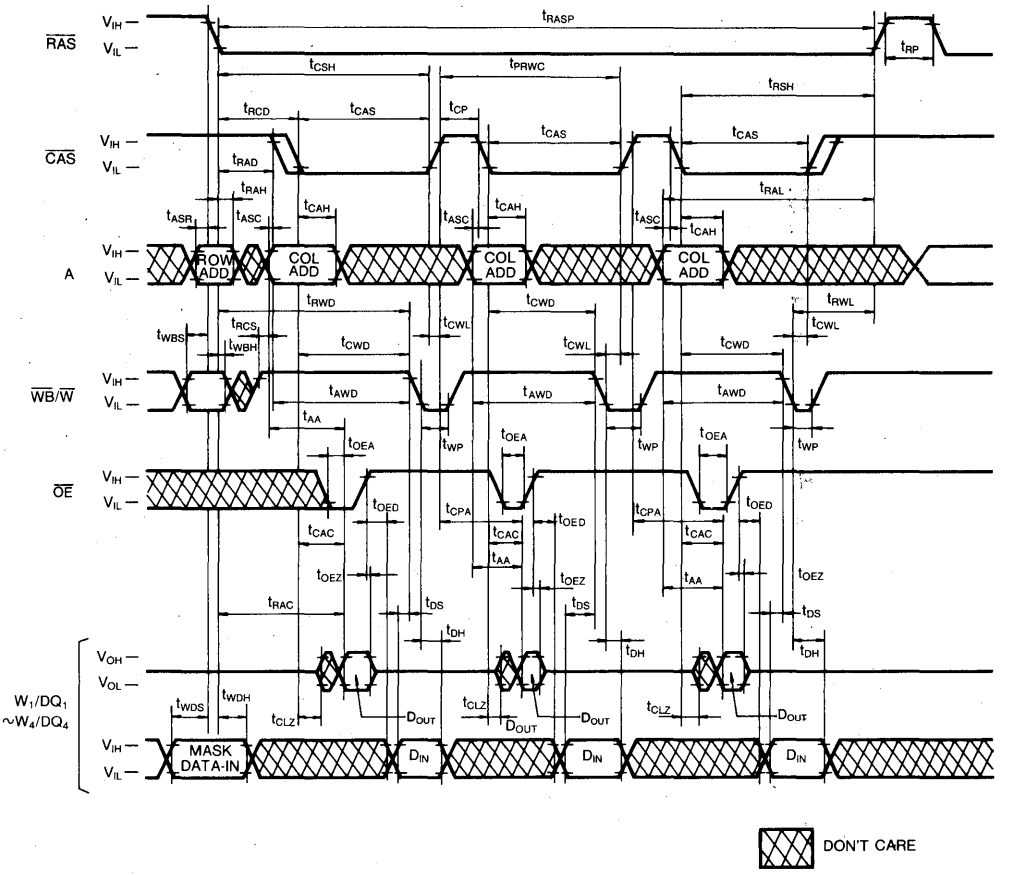


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

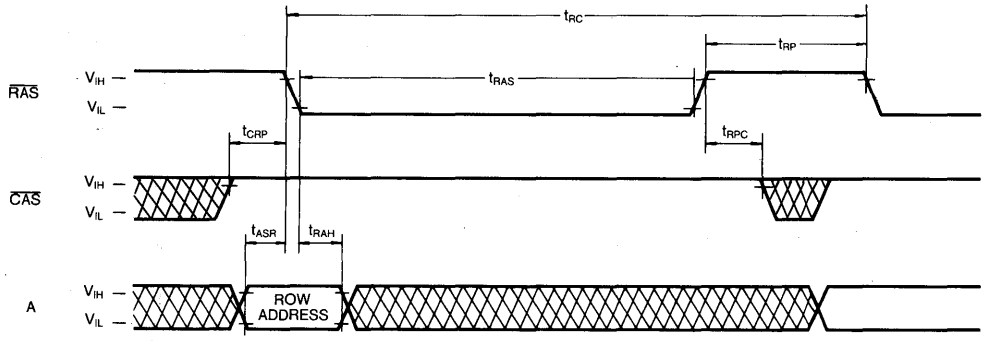
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

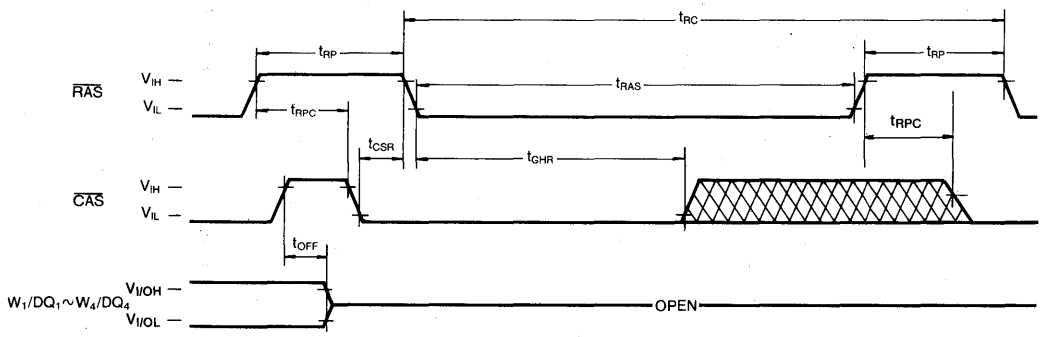
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{WB}/\overline{W}$, $\overline{OE}$=Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

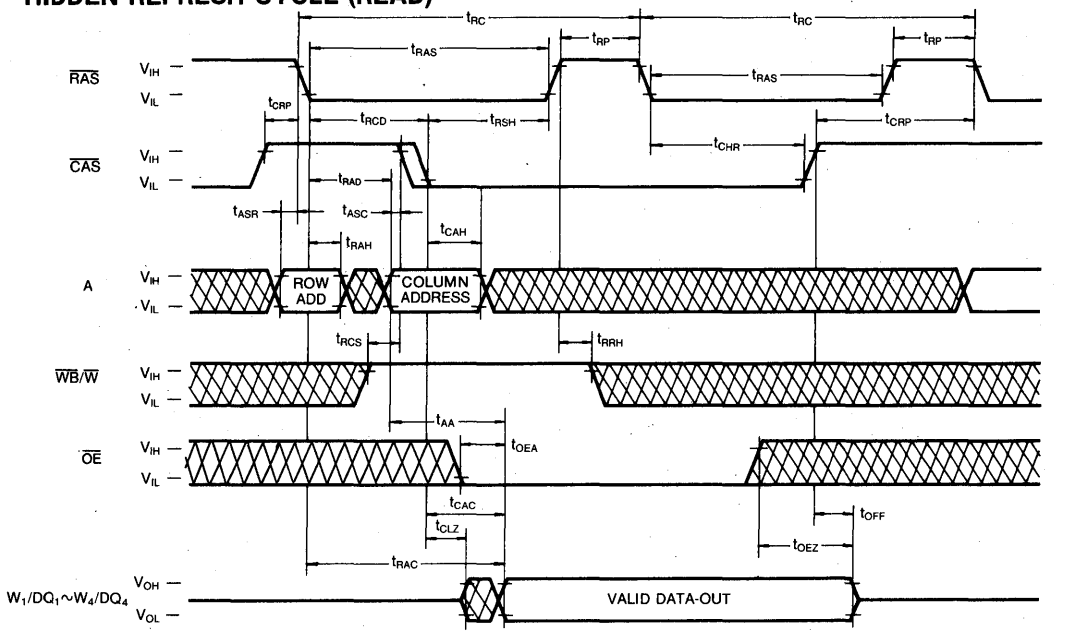
NOTE: $\overline{WB}/\overline{W}$, $\overline{OE}$, A=Don't Care



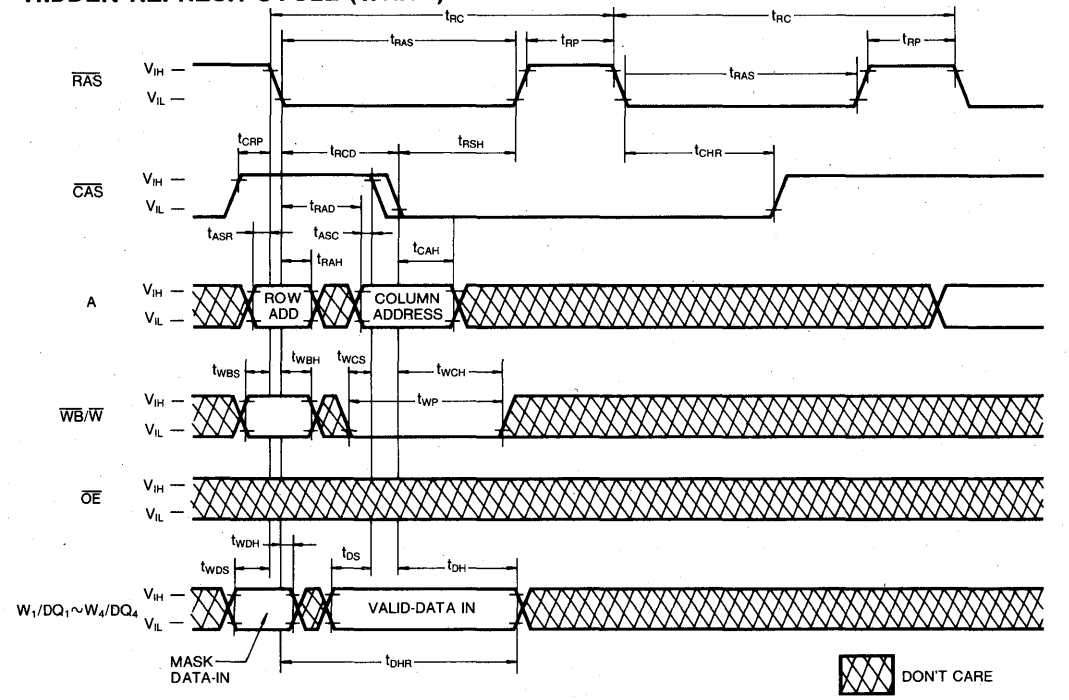

DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

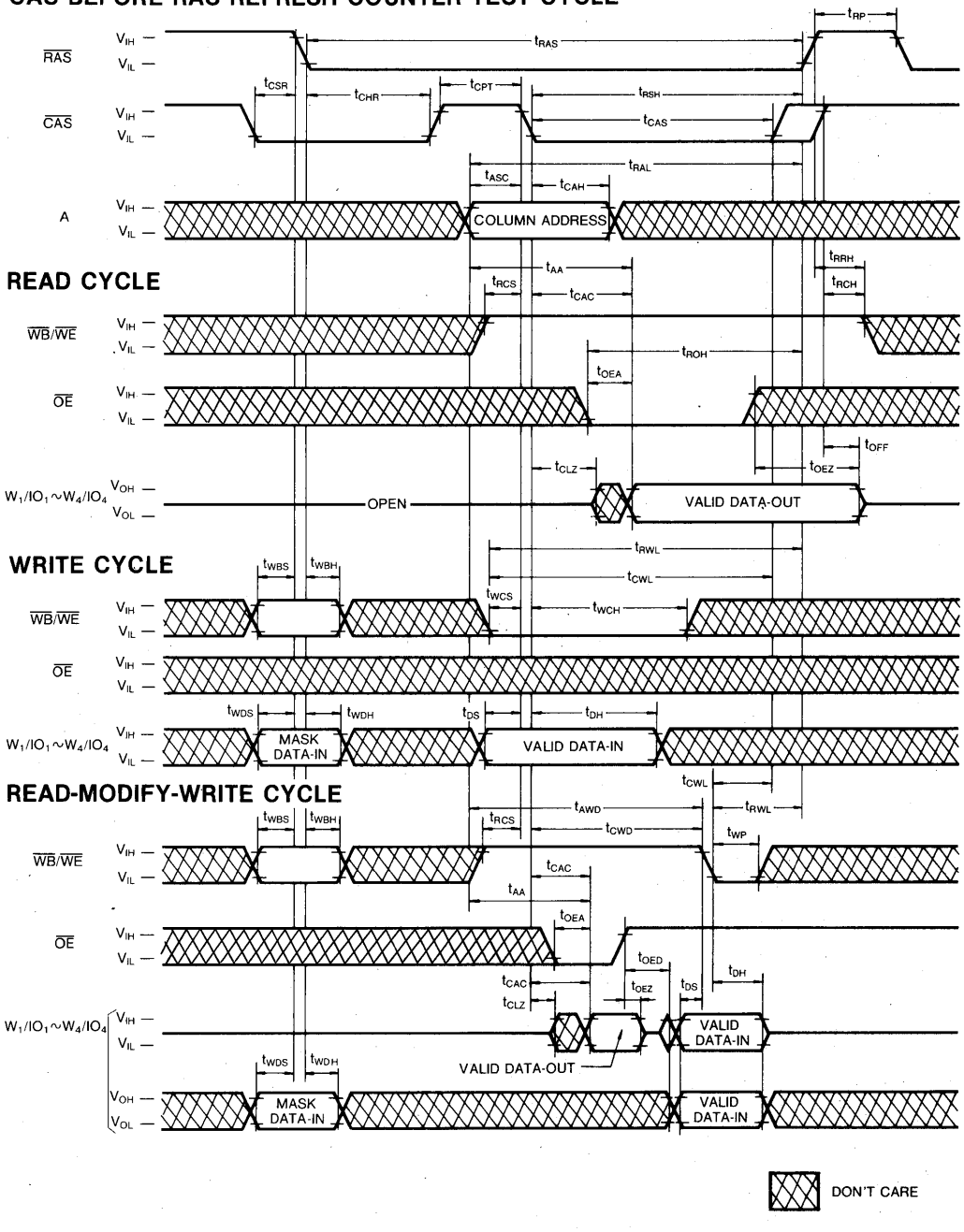


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



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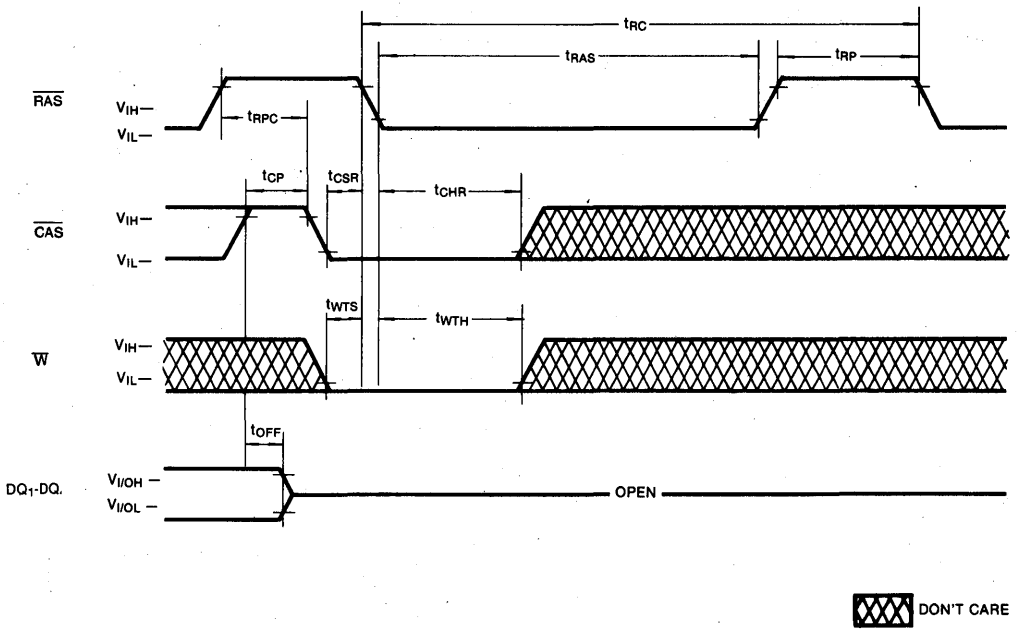
TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: $\overline{OE}$, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1010C is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM. $\overline{W}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM44C1010C contains 4,194,304 memory locations organized as 1,048,576 four-bit words. Twenty address bits are required to address a particular 4-bit word in the memory array. Since the KM44C1010C has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the KM44C1010C begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C1010C cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by $t_{RAS(min)}$ and $t_{CAS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1010C begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before $t_{RCD(max)}$ and if the column address is valid before $t_{RAD(max)}$ then the access time to valid data is specified by $t_{RAC(min)}$. However, if $\overline{CAS}$ goes low after $t_{RAD(max)}$, access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, $t_{RAC(min)}$, it is necessary to meet both $t_{RCD(max)}$ and $t_{RAD(max)}$.

The KM44C1010C has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C1010C can perform early write. $\overline{OE}$ controlled write and read-modify-write cycles. Each of these write cycles is achieved by maintaing the write per bit write enable ($\overline{WB}/\overline{W}$) input high at the falling edge of $\overline{RAS}$. If write-per bit function is performed, $\overline{WB}/\overline{W}$ is kept low at the falling edge of $\overline{RAS}$. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$ IN any type of write cycle, Data-in must be valid at or before the failing edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain the he Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. This output enable input ($\overline{OE}$) must be low during the time defined by $t_{OEA}$and t_{OEZ} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C1010C DQ pins.

Write-Per-Bit

Write-per-bit function is performed in the write cycle, that is early write. $\overline{OE}$ controlled write, read-modify-write. Write-per-bit markes it possible selectively to write one or more of the four I/O pins. To perform write per-bit function at the falling edge of $\overline{RAS}$ the write-per-bit/Write enable ($\overline{WB}/\overline{W}$) is kept low and at the same time Mask data of input pins to write among 4 I/O pins must be in high. If I/O pins that Mask data is kept low, write operation is inhibited.

Data Output

The KM44C1010C has a three state output buffer which are controlled by $\overline{CAS}$ and $\overline{OE}$. When either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}) the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} sepcify

DEVICE OPERATION (Continued)

when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1010C operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM44C1010C is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 1024 row addresses, (A_0-A_9).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C1010C has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C1010C hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1010C by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A_0 through A_9 are supplied by the on-chip refresh counter.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle.

Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS}=V_{SS}$ during power-up, the KM44C1010C could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up courrent.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C1010C inputs act like unterminated transmission lines resulting in significant positive and negative overshoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C1010C input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. the recommended methods are

DEVICE OPERATION (Continued)

gridded power and ground lines orseparate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with may DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C1010C using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C1010C and they supply much of the current used by the KM44C1010C during cycling.

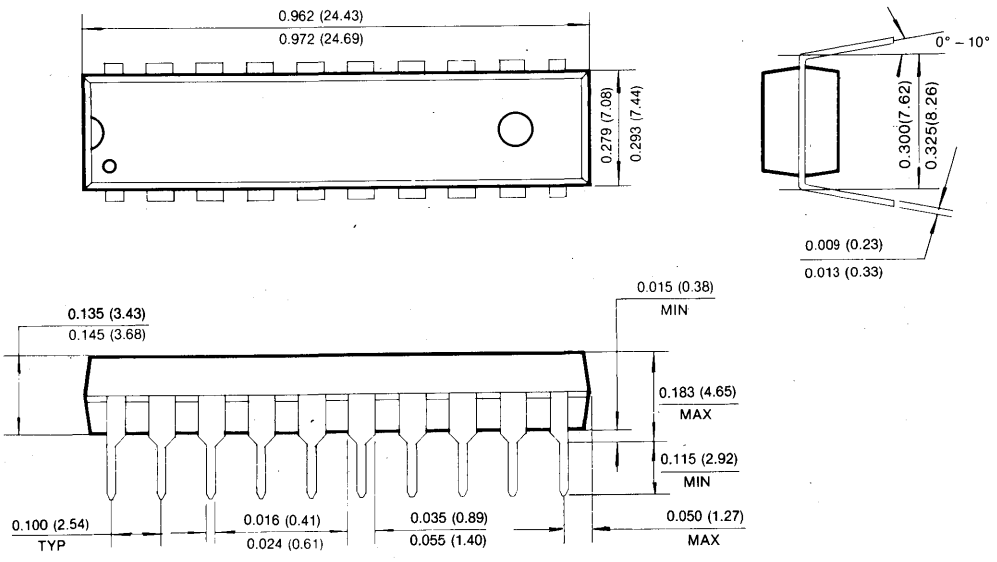
In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

3

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

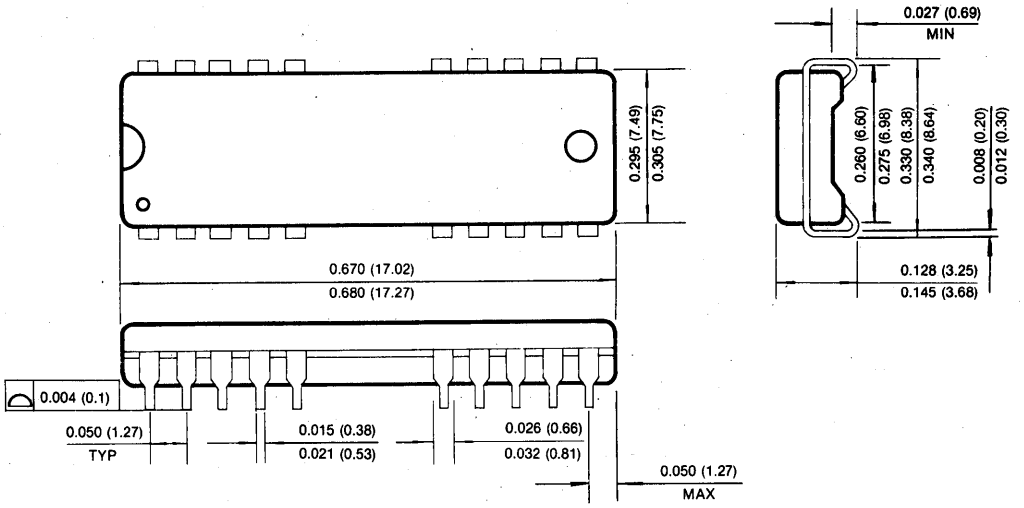
Units: Inches (Millimeters)



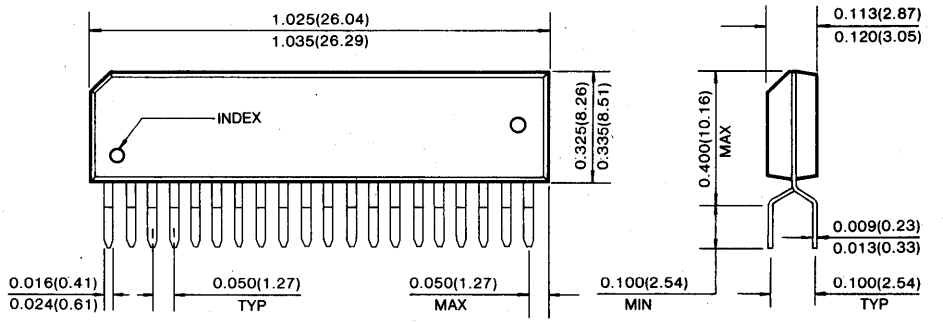
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

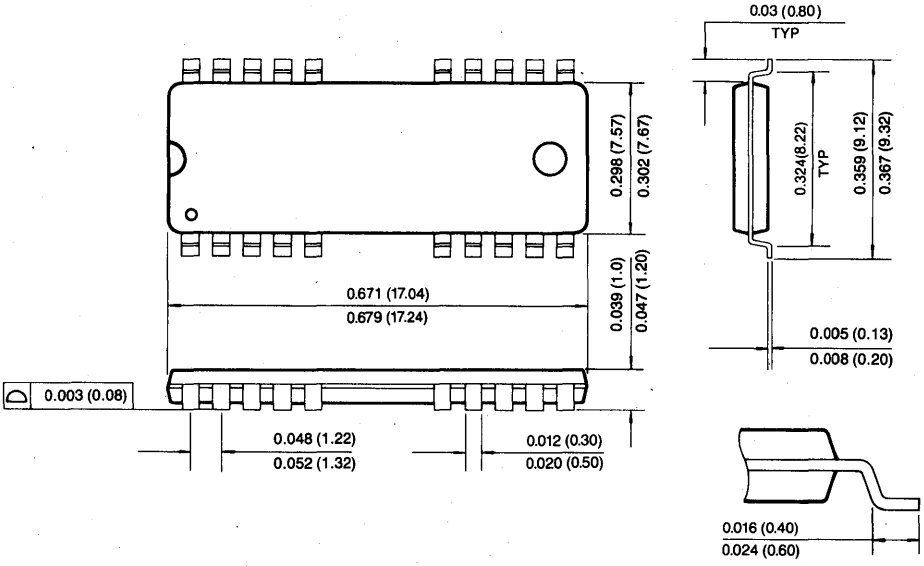


SAMSUNG ELECTRONICS

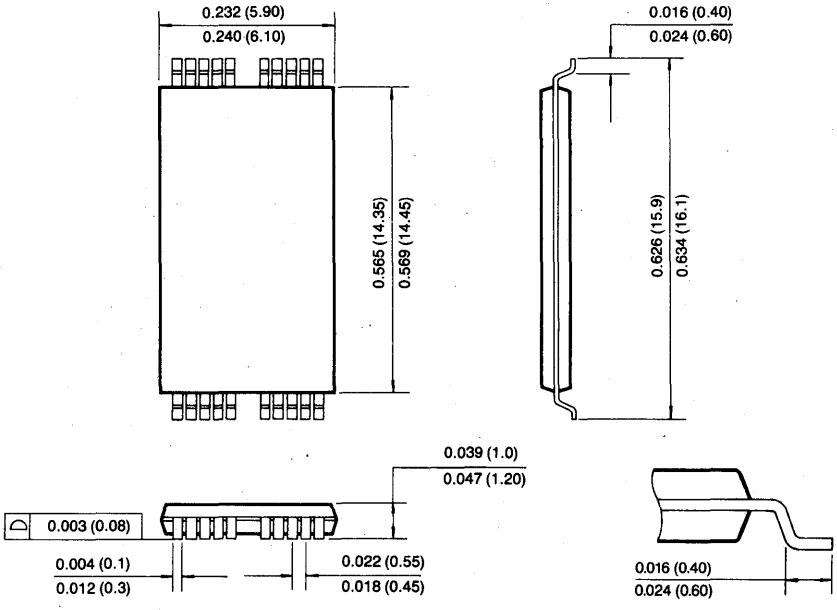
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)



SAMSUNG ELECTRONICS

1M ×4 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM44C1002C-5	50ns	13ns	90ns
KM44C1002C-6	60ns	15ns	110ns
KM44C1002C-7	70ns	20ns	130ns
KM44C1002C-8	80ns	20ns	150ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early Write or Output Enable Controlled Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in plastic DIP, SOJ, ZIP and TSOP(II) Packages**

GENERAL DESCRIPTION

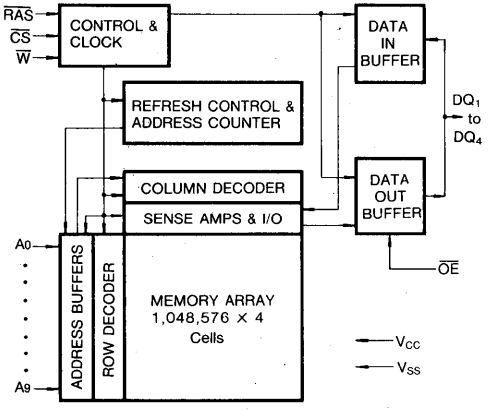
The Samsung KM44C1002C is a CMOS high speed 1,048,576×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

Static Column Mode Operation allows high sepeed random or sequential access within a row. The KM44C1002C offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C1002C is fabricated using Samsung's advanced CMOS process.

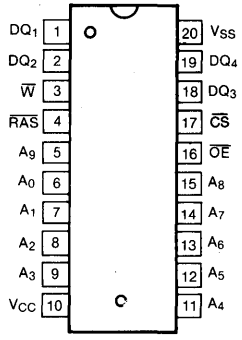
FUNCTIONAL BLOCK DIAGRAM



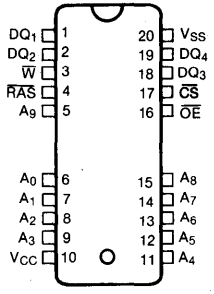
SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top Views)

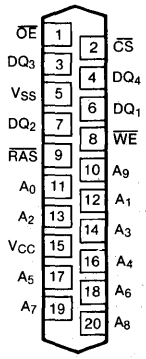
• KM44C1002CP



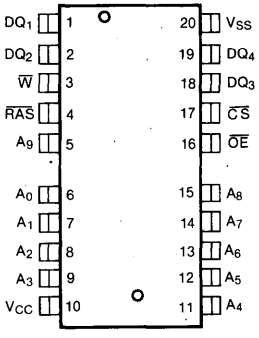
• KM44C1002CJ



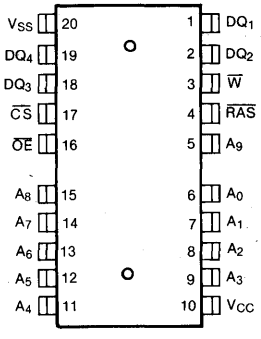
• KM44C1002CZ



• KM44C1002CT



• KM44C1002CTR



Pin Names	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1/DQ_4	Data In/Data Out
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC}=min.)	KM44C1002C-5	I_{CC1}	-	85	mA
	KM44C1002C-6		-	75	mA
	KM44C1002C-7		-	65	mA
	KM44C1002C-8		-	55	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM44C1002C-5	I_{CC3}	-	85	mA
	KM44C1002C-6		-	75	mA
	KM44C1002C-7		-	65	mA
	KM44C1002C-8		-	55	mA
Standby Column Mode Current* ($\overline{RAS}$=$\overline{CS}$=V_{IL} Address Cycling @t_{PC}=min.)	KM44C1002C-5	I_{CC4}	-	65	mA
	KM44C1002C-6		-	55	mA
	KM44C1002C-7		-	45	mA
	KM44C1002C-8		-	35	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{CC}-0.2V)		I_{CC5}	-	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC}=min.)	KM44C1002C-5	I_{CC6}	-	85	mA
	KM44C1002C-6		-	75	mA
	KM44C1002C-7		-	65	mA
	KM44C1002C-8		-	55	mA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. I_{CC1}, I_{CC3}, I_{CC6} Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once during a static column mode cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ1~DQ4)	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, Vcc=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Static column mode cycle time	t_{SC}	30		35		40		45		ns	
Static column mode read-write cycle time	t_{SRWC}	80		85		100		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
Access time from last write	t_{ALW}		50		55		65		75	ns	3
$\overline{CS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	7
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	
Output data hold time from column address	t_{AOH}	5		5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		35		40		45		55	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3		3		ns	
$\overline{RAS}$ precharge time	t_{RP}	30		40		50	50	60	50	ns	2
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70		80		ns	
$\overline{RAS}$ pulse width(static column mode)	t_{RASC}	50	100,000	60	100,000	70	10,000	80	10,000	ns	
$\overline{CS}$ to $\overline{RAS}$ hold time	t_{RSH}	13		15		20	100,000	20	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CS}$ pulse width	t_{CS}	13	10,000	15	10,000	20		20		ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	13	100,000	15	100,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	37	20	45	20	100,000	20	100,000	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	50	15	60	ns	4
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5	35	5	40	ns	11
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold	t_{CAH}	10		10		15		15		ns	
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	40		45		55		60		ns	6
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		70		80		90		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Column address hold time referenced to $\overline{RAS}$ rise	tAH	5		5		5		5		ns	
Last Write to column address to delay time	tLWAD	20	25	20	25	25	35	25	40	ns	12
Last write to column address hold time	tAHLW	50		60		70		80		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		50		55		60		ns	6
Write command pulse width	tWP	10		15		15		15		ns	
Write command inactive time	tWI	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CS}$ lead time	tCWL	13		15		20		20		ns	
Data-in set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	40		50		55		60		ns	6
Refresh period (1024 cycles)	tREF		16		16		16		16	ms	
Write command set-up time	tWCS	0		0		0		0		ms	8
$\overline{CS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ms	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{CS}$ setup time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{RAS}$ to $\overline{CS}$ hold time	tRPC	5		5		5		5		ns	
$\overline{CS}$ precharge time($\overline{CS}$-before-$\overline{RAS}$ counter test cycle)	tCPT	20		20		25		30		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Output buffer trun off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		15		15		ns	

TEST MODE CYCLE

(Note.13)

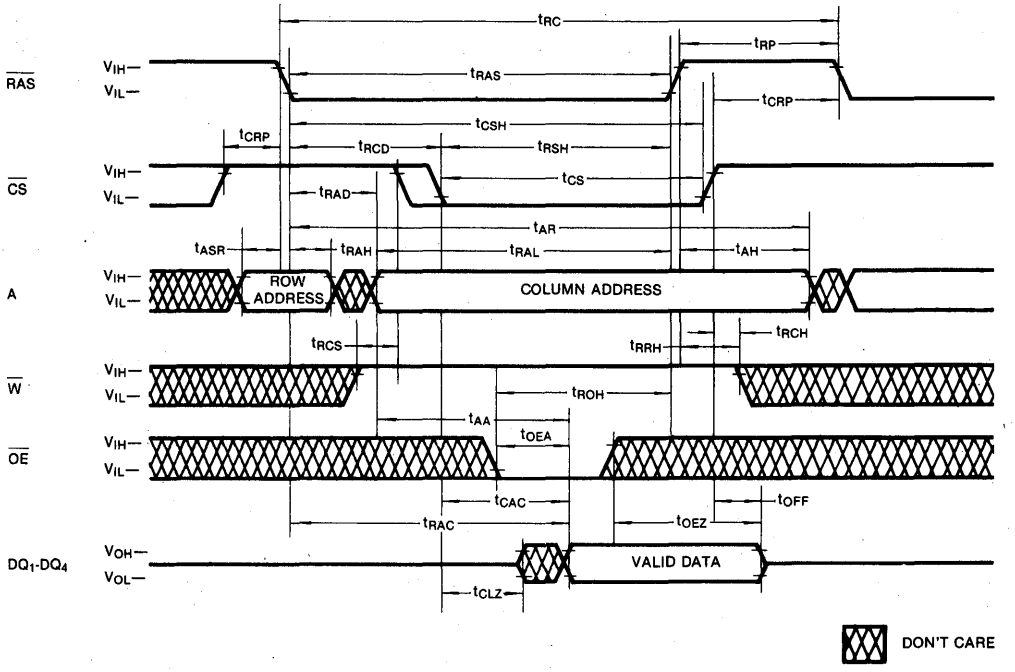
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	95		115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	138		160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		55		65		75		85	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		18		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CS}$ pulse width	t_{CS}	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		25		25		ns	
$\overline{CS}$ hold time	t_{CSH}	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		45		ns	
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	53		60		70		75		ns	8
Static column mode cycle time	t_{SC}	35		40		45		50		ns	
Static column mode read-modefy-write	t_{SRWC}	85		90		105		115		ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	55	100,000	65	100,000	75	100,000	85	100,000	ns	
Access time from last write	t_{ALW}		55		60		70		80	ns	3,12
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	18	100,000	20	100,000	25	100,000	25	100,000	ns	
$\overline{OE}$ access time	t_{OEA}		18		25		25		30		
$\overline{OE}$ to data delay	t_{OED}	18		20		25		25			
$\overline{OE}$ command hold time	t_{OEH}	18		20		25		25			

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. Operation within the $t_{LWAD(max)}$ limit insures that $t_{ALW(max)}$ can be met. $t_{LWAD(max)}$ is specified as a reference point only. t_{LWAD} is greater than the specified $t_{LWAD(max)}$ limit, then access time is controlled by t_{AA}.
13. These specifications are applied in the test mode.

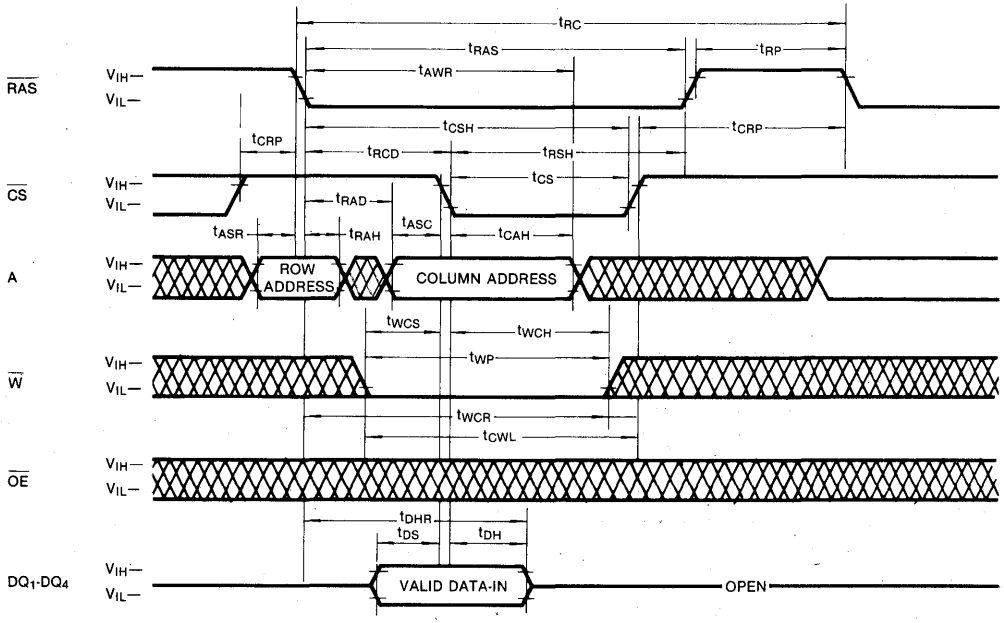
TIMING DIAGRAMS

READ CYCLE

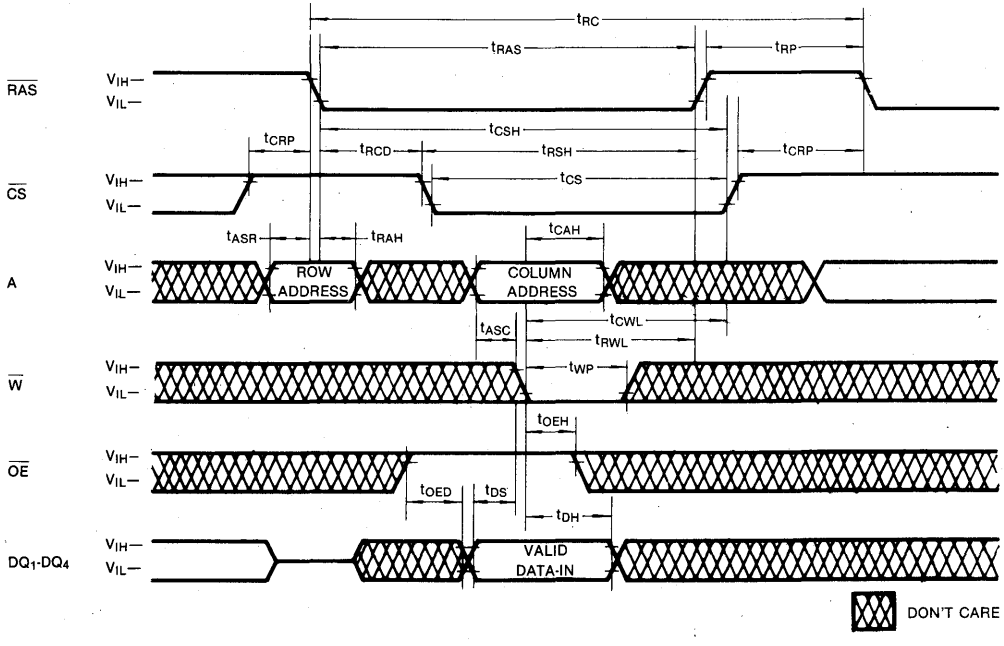


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



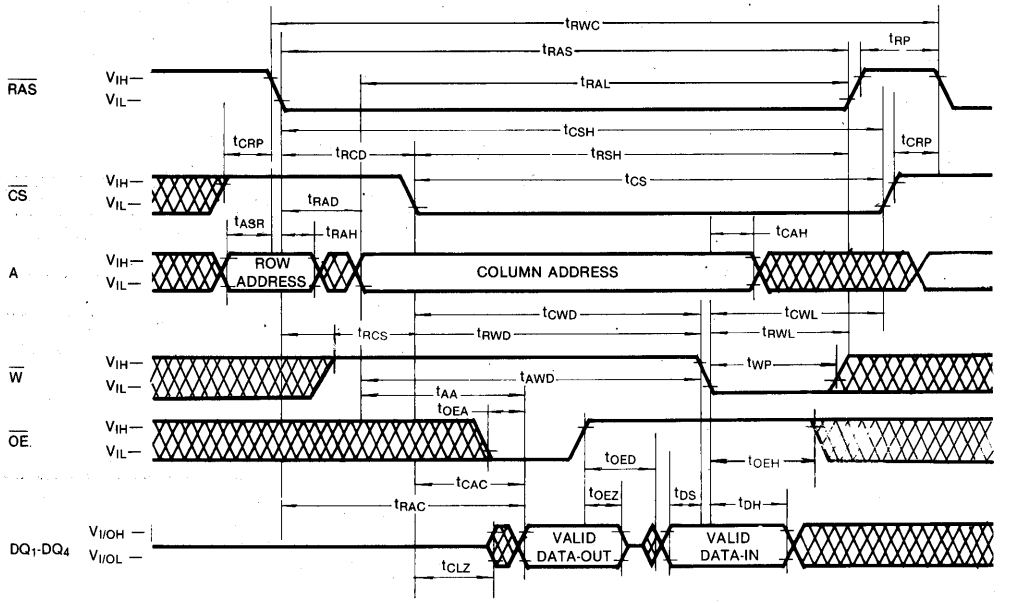
WRITE CYCLE (OE CONTROLLED WRITE)



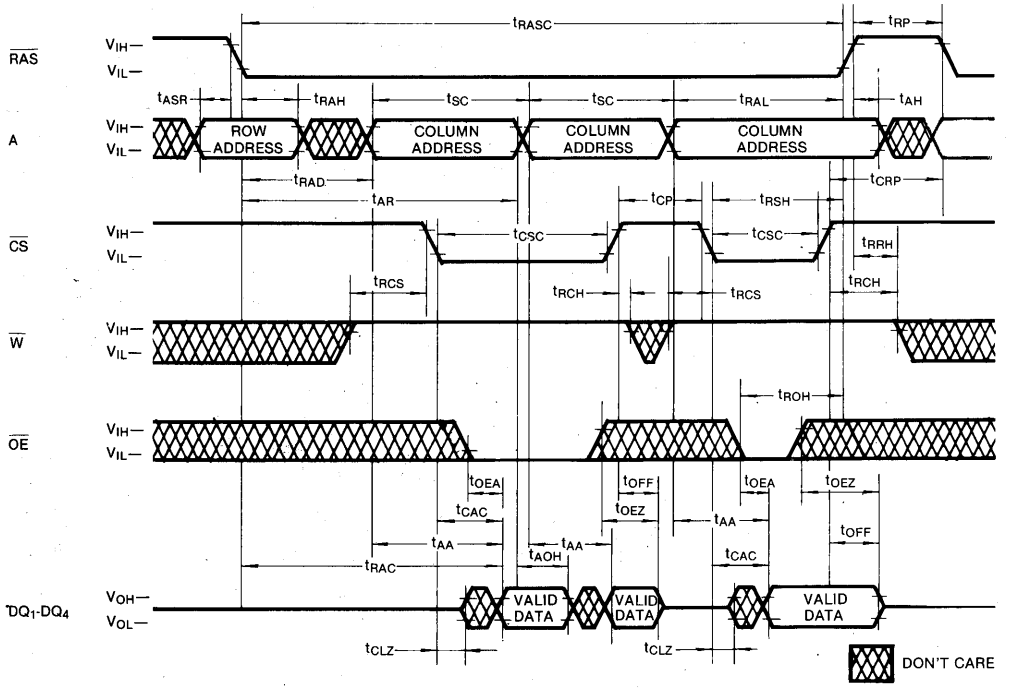
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



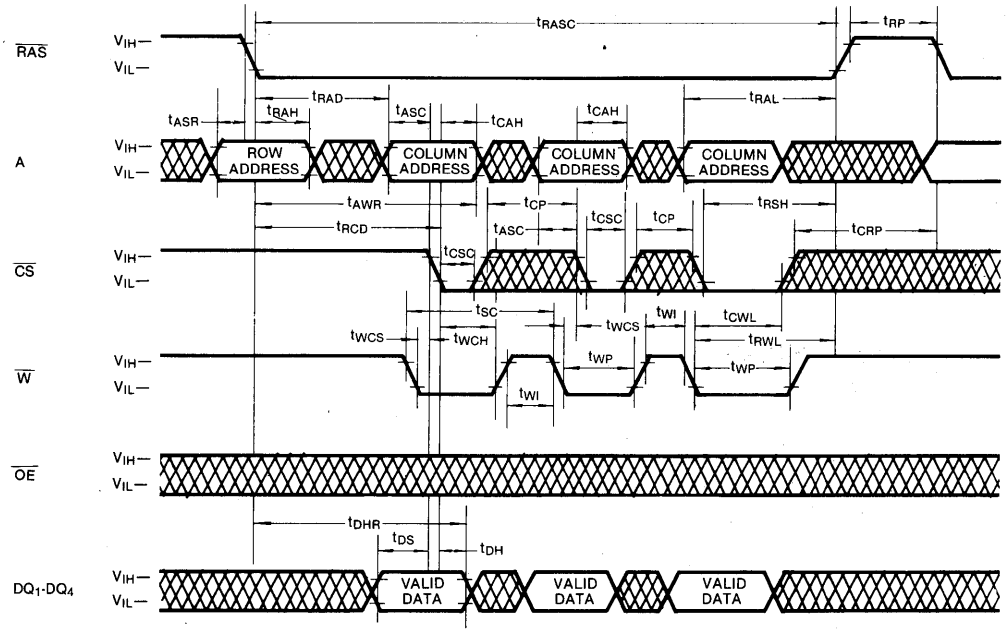
STATIC COLUMN MODE READ CYCLE



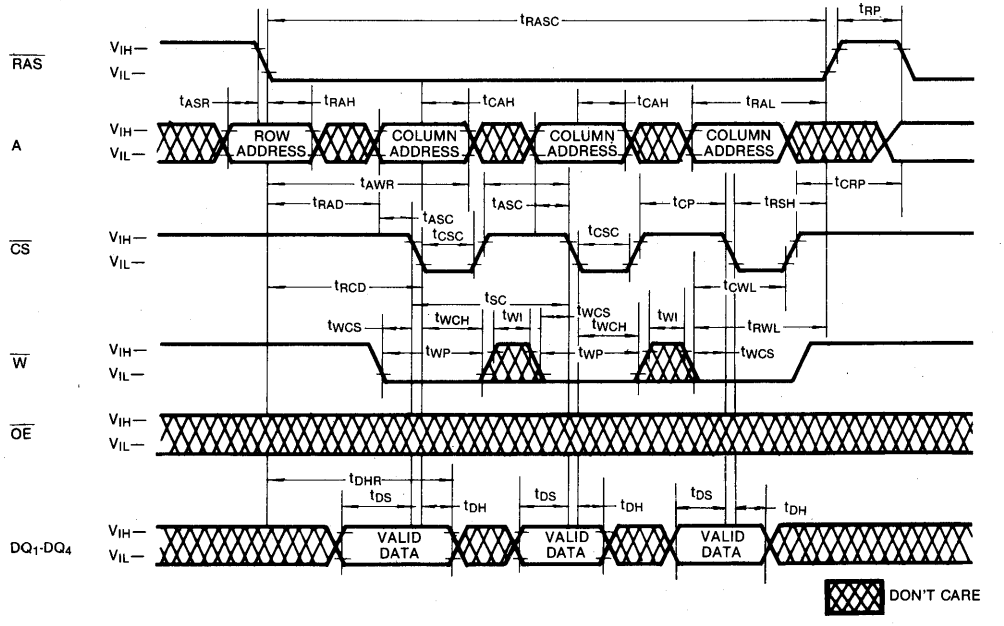
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ controlled early write)

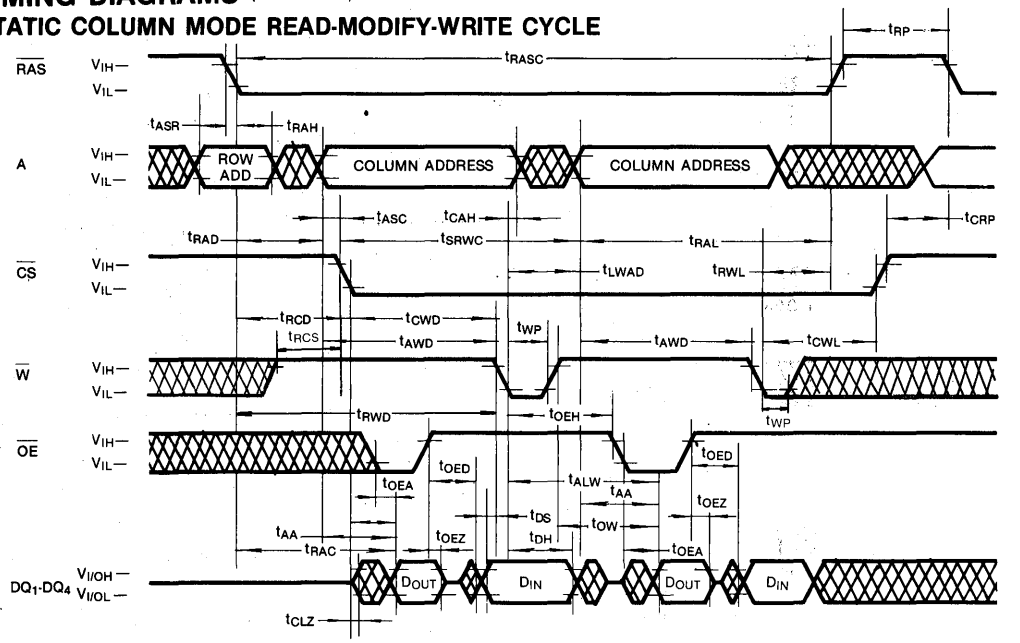


STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)

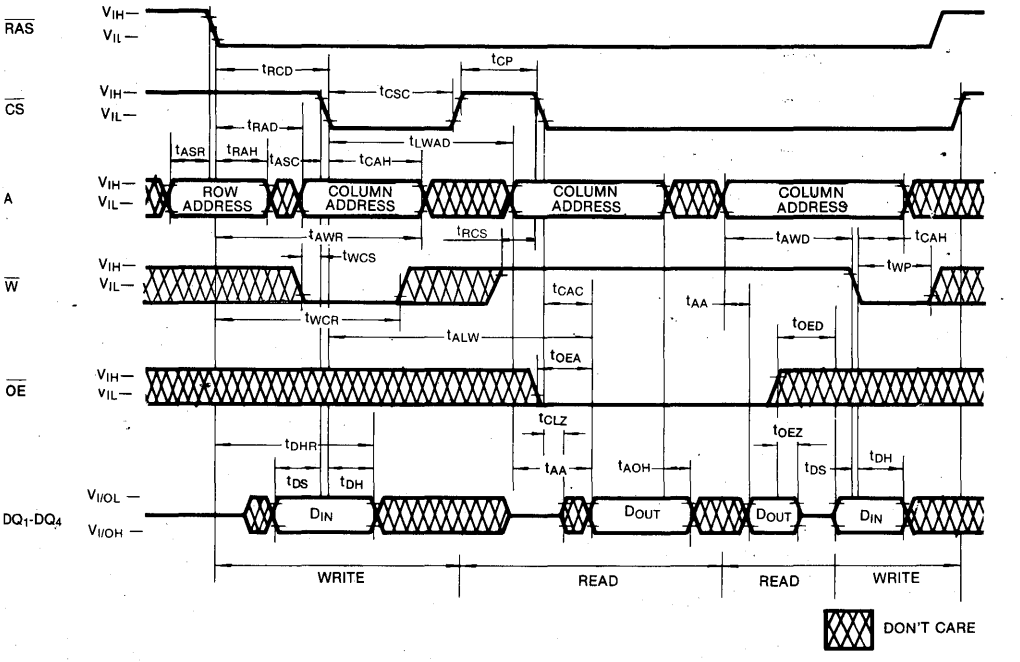


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



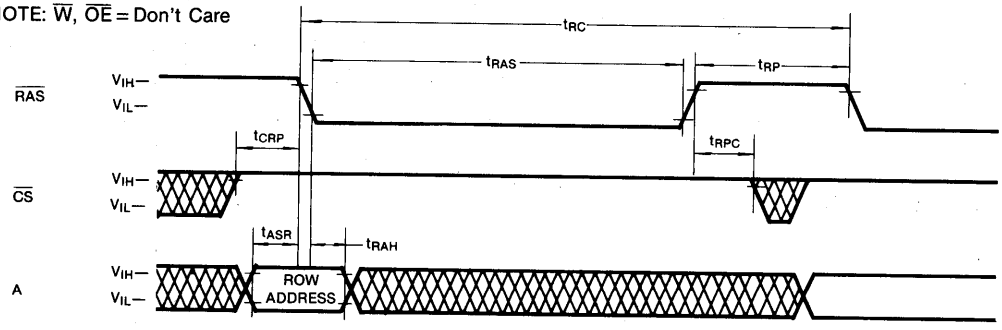
STATIC COLUMN MODE MIXED CYCLE



TIMING DIAGRAMS (Continued)

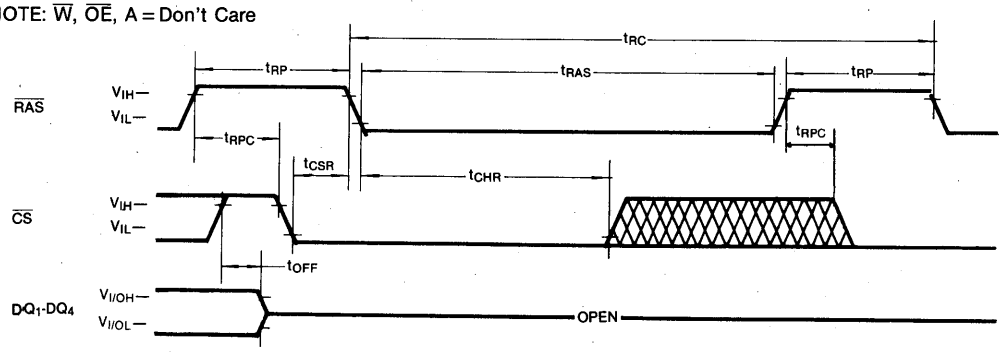
RAS-ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$ = Don't Care



CS-BEFORE-RAS REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care

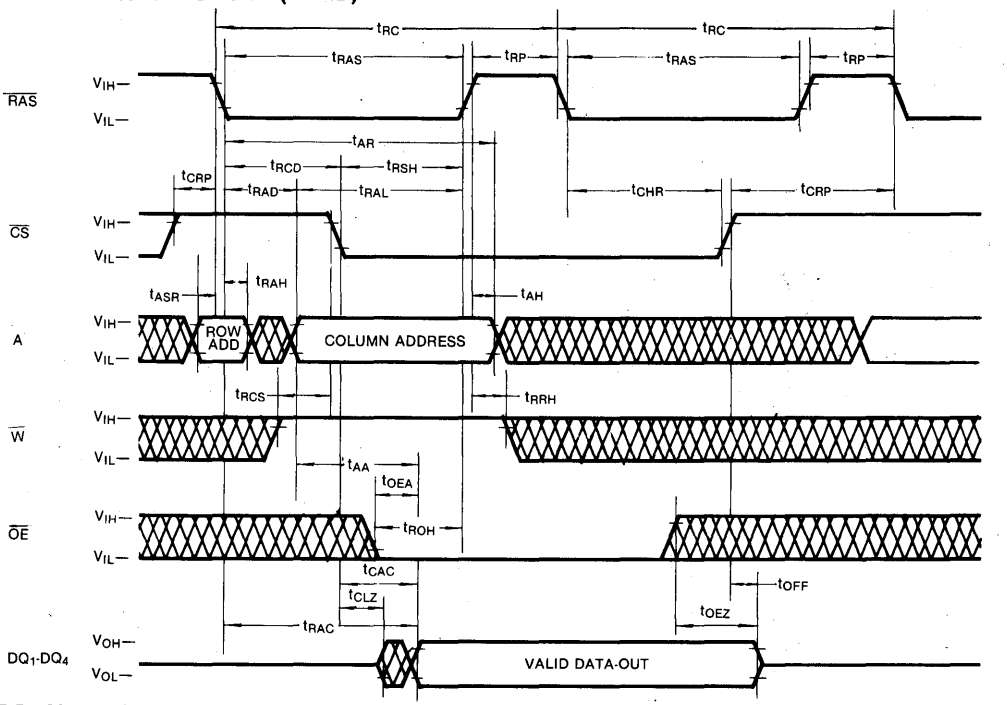


DON'T CARE

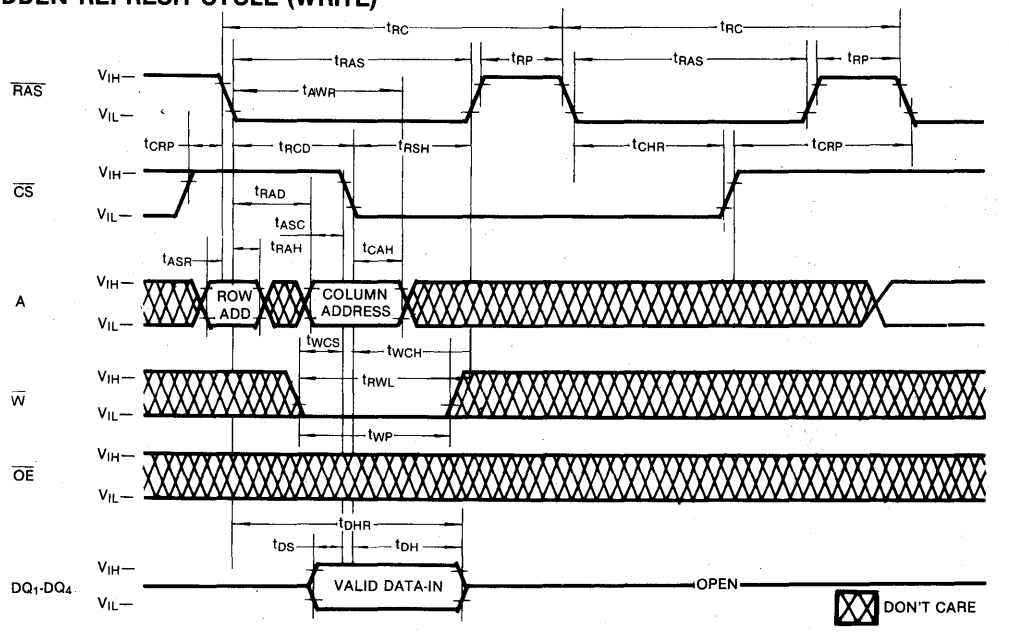
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



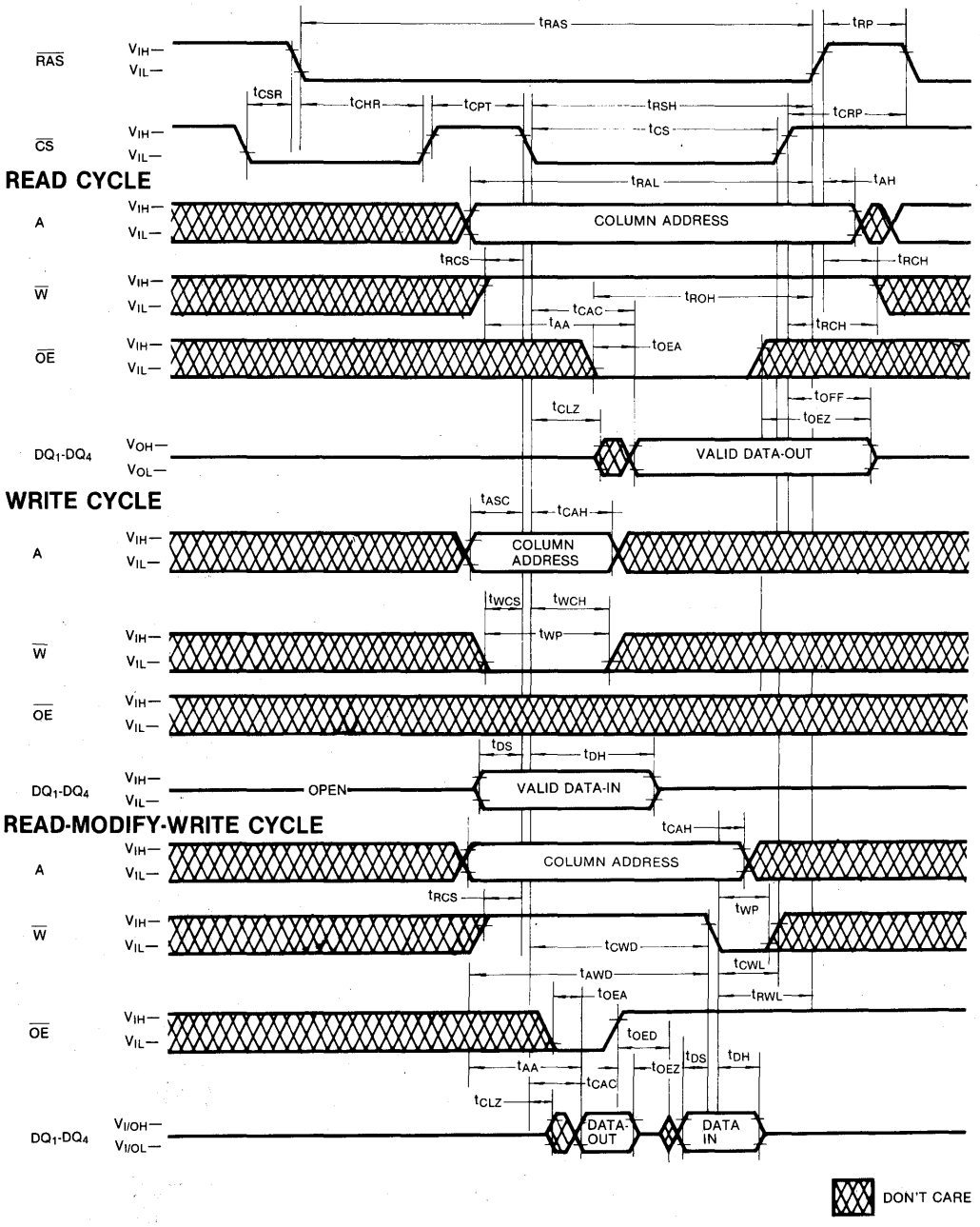
HIDDEN REFRESH CYCLE (WRITE)



SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

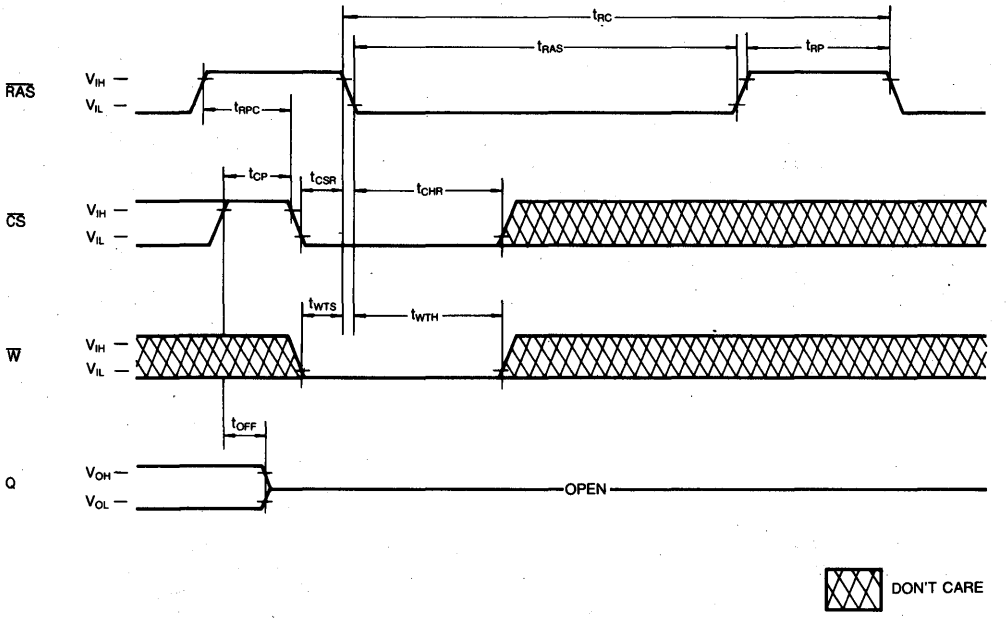


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1002C is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM. $\overline{W}$, $\overline{CS}$ Before $\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM44C1002C contains 4,194,304 memory locations. organized as 1,048,576 four-bit words. TwentytWo address bits are required to address a particular 4-bit word in the memory array. Since the KM44C1002C has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe $\overline{CS}$ and the valid row and column address inputs.

Operation of the KM44C1002C begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM44C1002C cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1002C bigin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the addess time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

The KM44C1002C has common data I/O pins. For this reason and output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs. $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C1002C can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remain in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the daaressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. The output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to apear at the outputs If t_{CWD} and t_{RWD} are not to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C1002C's DQ pins.

Data Output

The KM44C1002C has a three-state output buffer which is controlled by $\overline{CS}$and $\overline{OE}$. Whenever $\overline{CS}$ or $\overline{OE}$ is high(V_{IH}) the output are in the high impedance(Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing paraneters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1002C operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Static Column Mode Read-Modify-Write.

DEVICE OPERATION (Continued)

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$-before-$\overline{RAS}$ Refresh, $\overline{CS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD})

Refresh

The data in the KM44C1002C is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16ms. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only-Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each for each of the 1024 rw address. (A_0~A_9).

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM44C1002C has $\overline{CS}$-Before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM44C1002C hidden refresh cycle is actually $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1002C by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantateous to perform refresh in this mammer but in gheneral $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

Power-up

If $\overline{RAS}$= V_{SS} during power-up, the KM44C1002C might begin an active cycle. This coundition results in higher than necessary current demands from the power supplu during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ rrack with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C1002C inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short sa possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C1002C input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C1002C using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C1002C and they supply much of the current used by the KM44C1002C during cycling.

DEVICE OPERATION (Continued)

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with may DRAMs these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on the memory boards to facilitate the shortest possible address and control lines to all the DRAMs.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

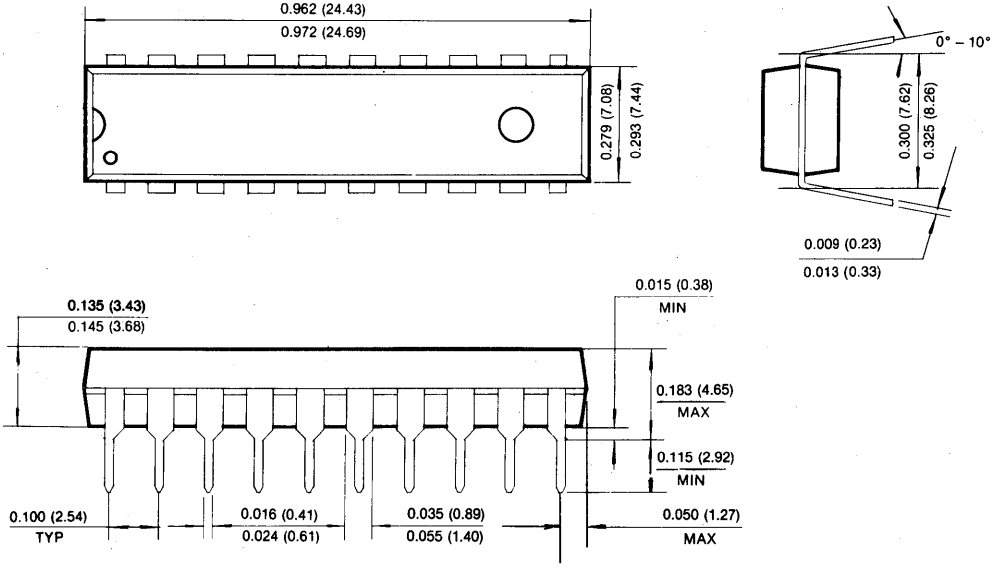
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of eachKM44C1002Busing the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C1002Band they supply much of the current used by theKM44C1002Bduring cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (millimeters)

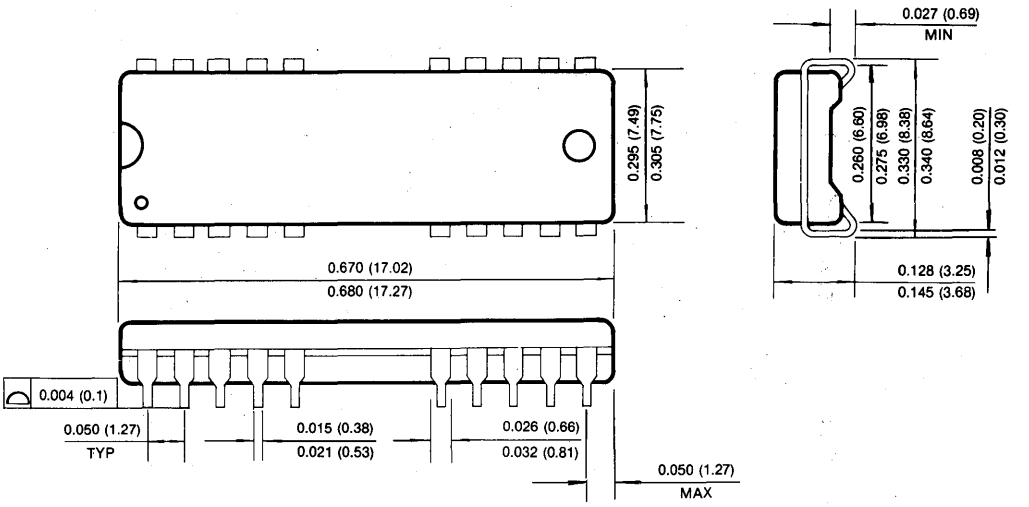


SAMSUNG ELECTRONICS

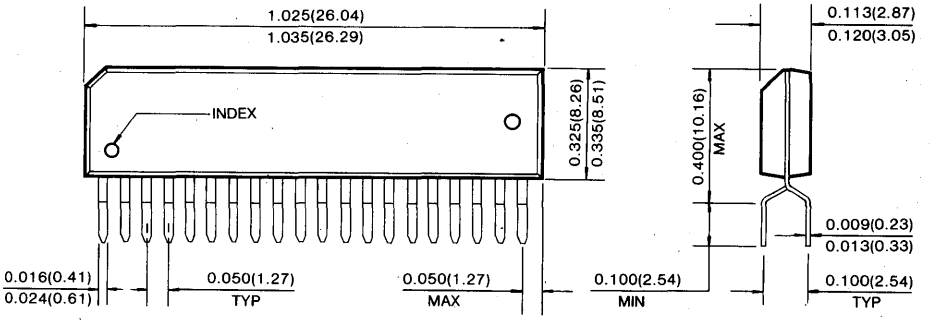
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



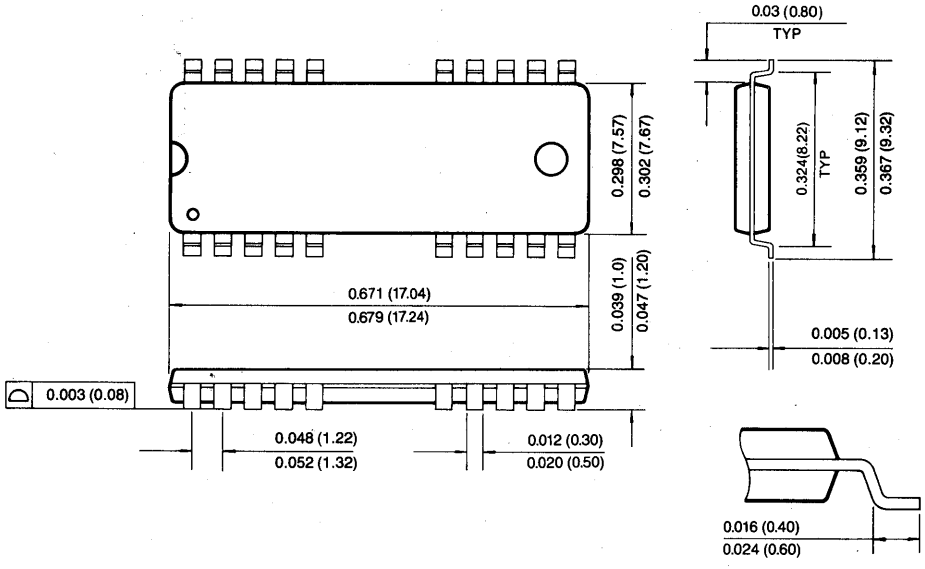
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



1M ×4Bit CMOS Quad CAS RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM44C1003C/CL/CSL-5	50ns	13ns	90ns
KM44C1003C/CL/CSL-6	60ns	15ns	110ns
KM44C1003C/CL/CSL-7	70ns	20ns	130ns
KM44C1003C/CL/CSL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Four separate $\overline{CAS}$ pins provide for separate I/O operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and hidden refresh capability**
- **Fast parallel test mode capability**
- **TTL compatible inputs and outputs**
- **Early wite or output enable controlled write**
- **Single + 5.0V ±10% power supply**
- **Refresh Cycle**
  - **1024 cycle/16ms (Normal)**
  - **1024 cycle/128ms (L-version)**
  - **1024 cycle/256ms (SL-version)**
- **Power Dissipation**
  - **Standby: 5.5mW (Normal)**
    1.1mW (L-version)
    0.55mW (SL-version)
  - **Active (50/60/70/80) : 468/413/358/303mW**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP -II packages**

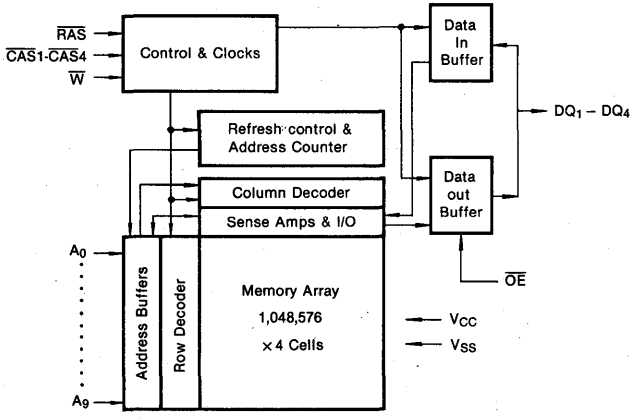
GENERAL DESCRIPTION

The Samsung KM44C1003C/CL/CSL is a CMOS high speed 1,048,576 × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance portable computers.

The KM44C1003C/CL/CSL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides in-chip auto refresh as an alterntive to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible and four separate $\overline{CAS}$ pins provide for separate I/O operation allowing this device to operate in partity mode.

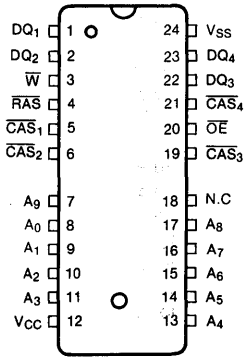
The KM44C1003C/CL/CSL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

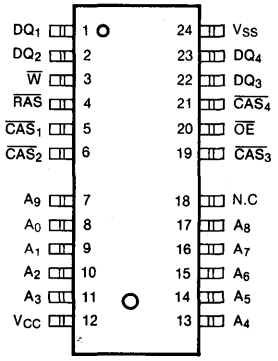


PIN CONFIGURATION (Top Views)

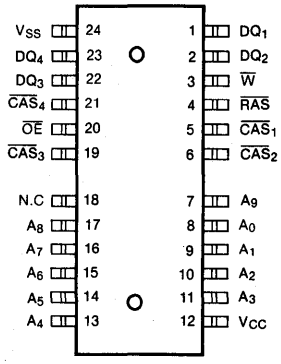
• KM44C1003CJ/CLJ/CSLJ



• KM44C1003CT/CLT/CSLT



• KM44C1003CTR/CLTR/CSLTR



Pin Name	Pin Function
A0-A9	Address Inputs
DQ1-DQ4	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS1}$-$\overline{CAS4}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power(+5.0V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	KM44C1003C/CL/CSL-5	I_{CC1}	-	85	mA
	KM44C1003C/CL/CSL-6		-	75	mA
	KM44C1003C/CL/CSL-7		-	65	mA
	KM44C1003C/CL/CSL-8		-	55	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44C1003C	I_{CC2}	-	2	mA
	KM44C1003CL		-	1	mA
	KM44C1003CSL		-	1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM44C1003C/CL/CSL-5	I_{CC3}	-	85	mA
	KM44C1003C/CL/CSL-6		-	75	mA
	KM44C1003C/CL/CSL-7		-	65	mA
	KM44C1003C/CL/CSL-8		-	55	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44C1003C/CL/CSL-5	I_{CC4}	-	65	mA
	KM44C1003C/CL/CSL-6		-	55	mA
	KM44C1003C/CL/CSL-7		-	45	mA
	KM44C1003C/CL/CSL-8		-	35	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM44C1003C	I_{CC5}	-	1	mA
	KM44C1003CL		-	200	μA
	KM44C1003CSL		-	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C1003C/CL/CSL-5	I_{CC6}	-	85	mA
	KM44C1003C/CL/CSL-6		-	75	mA
	KM44C1003C/CL/CSL-7		-	65	mA
	KM44C1003C/CL/CSL-8		-	55	mA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Max	Units
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ_1-DQ_4=Don't Care T_{RC}=125μS(L-Ver.) 250μS(SL-Ver), T_{RAS}=T_{RAS}min~300ns	KM44C1003CL KM44C1003CSL	I_{CC7}	-	300 150	μA μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once during a fast page mode cycle.

3

CAPACITANCE (T_A=25°C, V_{CC}=5.0V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS_1}$-$\overline{CAS_4}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±0.5V, See notes 1,2)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading C_L=100pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5,19
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3,19
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	7,19
Transition time(rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	17
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	18
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10.000	ns	24
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4,17

AC CHARACTERISTICS (Continued)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading C_L=100pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	18
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	17
Column address hold time	tCAH	10		10		15		15		ns	17
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	17
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	9,18
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	25
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	18
Data set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Refresh period (SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8,17
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	8,17
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	17
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	18
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3,19
Fast page mode cycle time	tPC	35		45		45		50		ns	20
Fast page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	20
$\overline{CAS}$ precharge time	tCP	10		10		10		10		ns	21
$\overline{RAS}$ pulse width(Fast Page Mode)	tRASP	50	200,000	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	22

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	23
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time (test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (test mode in)	tWPH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ rcycle)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ rcycle)	tWRH	10		10		10		10		ns	
Hold time $\overline{CAS}$ low to $\overline{CAS}$ high	tCLCH	5		5		5		5		ns	15,26

TEST MODE CYCLE

(Note.12)

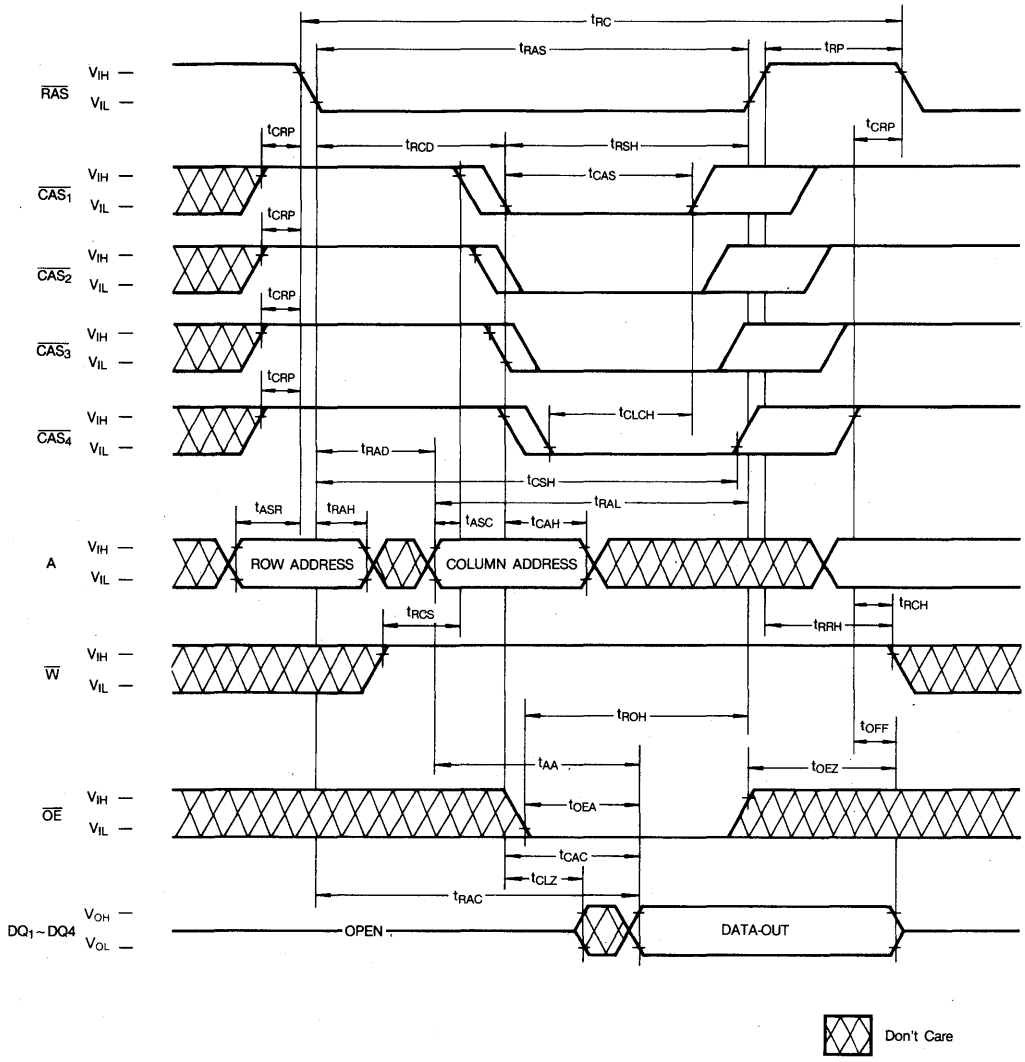
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		60		65		75		85	ns	3,4,11,13
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5,13
Access time from column address	tAA		30		35		40		45	ns	3,11,13
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	81		90		100		105		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	55		65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA	35			40		45		50	ns	3
$\overline{OE}$ access time	tOEA	18			20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. In order to hold the address latched by the first $\overline{CAS}$ $\times$ going low, the parameter t_{CLCH} must be met.
16. If at least one $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the datao-ut buffer, all four $\overline{CAS}$ must be pulsed high for t_{CP}.
17. The first $\overline{CAS}$ $\times$ edge to transition low.
18. The last $\overline{CAS}$ $\times$ edge to transition low.
19. Output parameter is referenced to corresponding $\overline{CAS}$ $\times$ input.
20. Last rising $\overline{CAS}$ $\times$ edge to next cycle's last rising $\overline{CAS}$ $\times$ edge.
21. Last rising $\overline{CAS}$ $\times$ edge to first falling $\overline{CAS}$ $\times$ edge.
22. First DQ $\times$ controlled by the first $\overline{CAS}$ $\times$ to go low.
23. Last DQ $\times$ controlled by the first $\overline{CAS}$ $\times$ to go low.
24. Each $\overline{CAS}$ $\times$ must meet minimum pulse width.
25. Last $\overline{CAS}$ $\times$ to go low.
26. The last falling $\overline{CAS}$ $\times$ edge to the first rising $\overline{CAS}$ $\times$ edge.

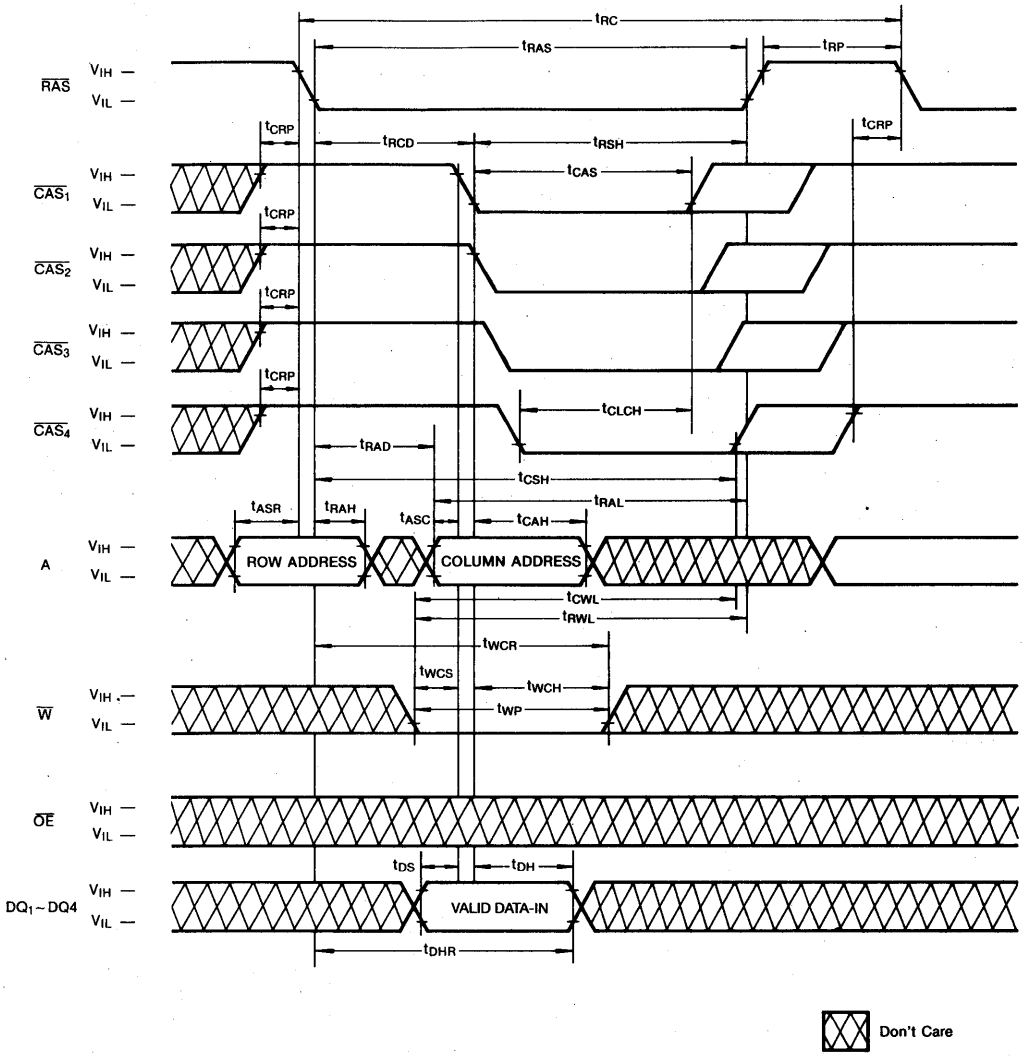
TIMING DIAGRAM

READ CYCLE



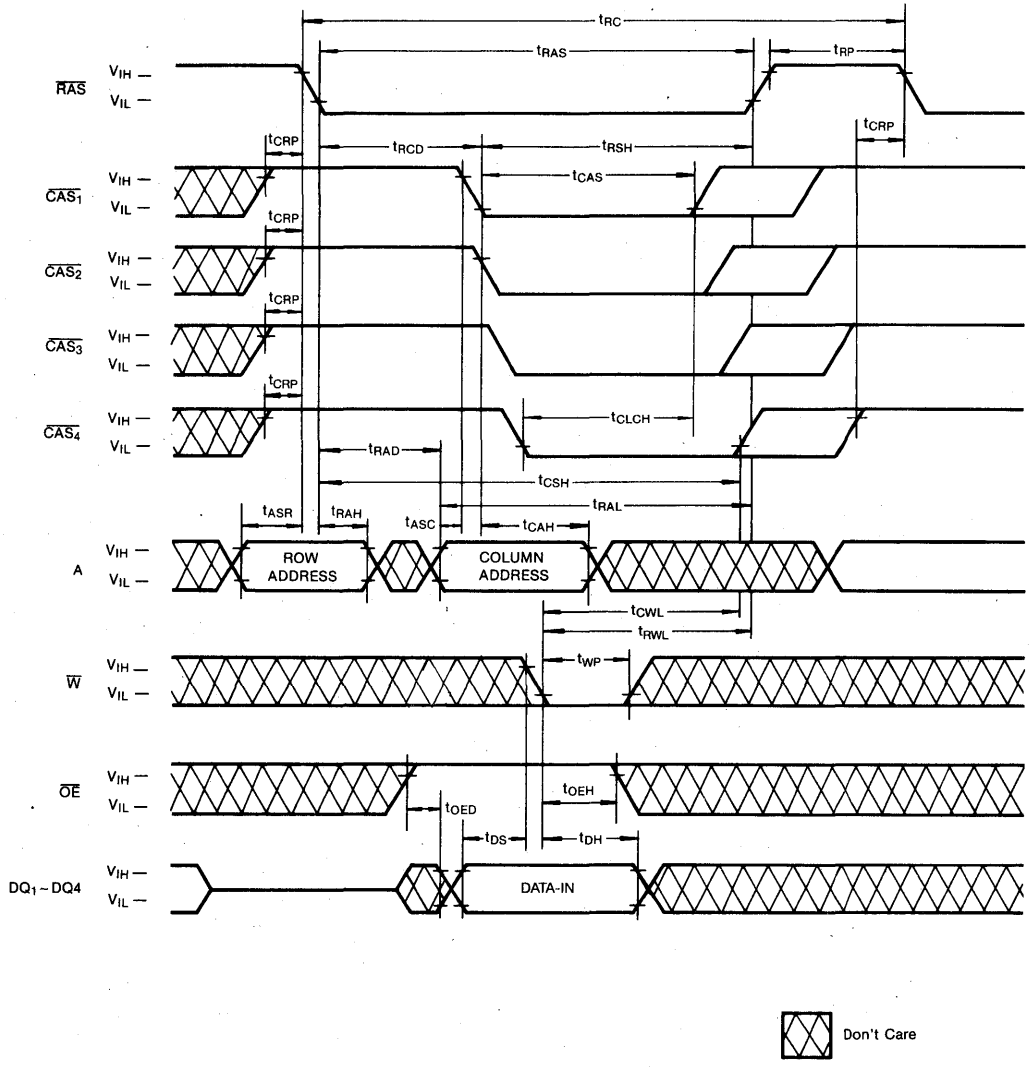
TIMING DIAGRAM (Continued)

WRITE CYCLE (EARLY WRITE)



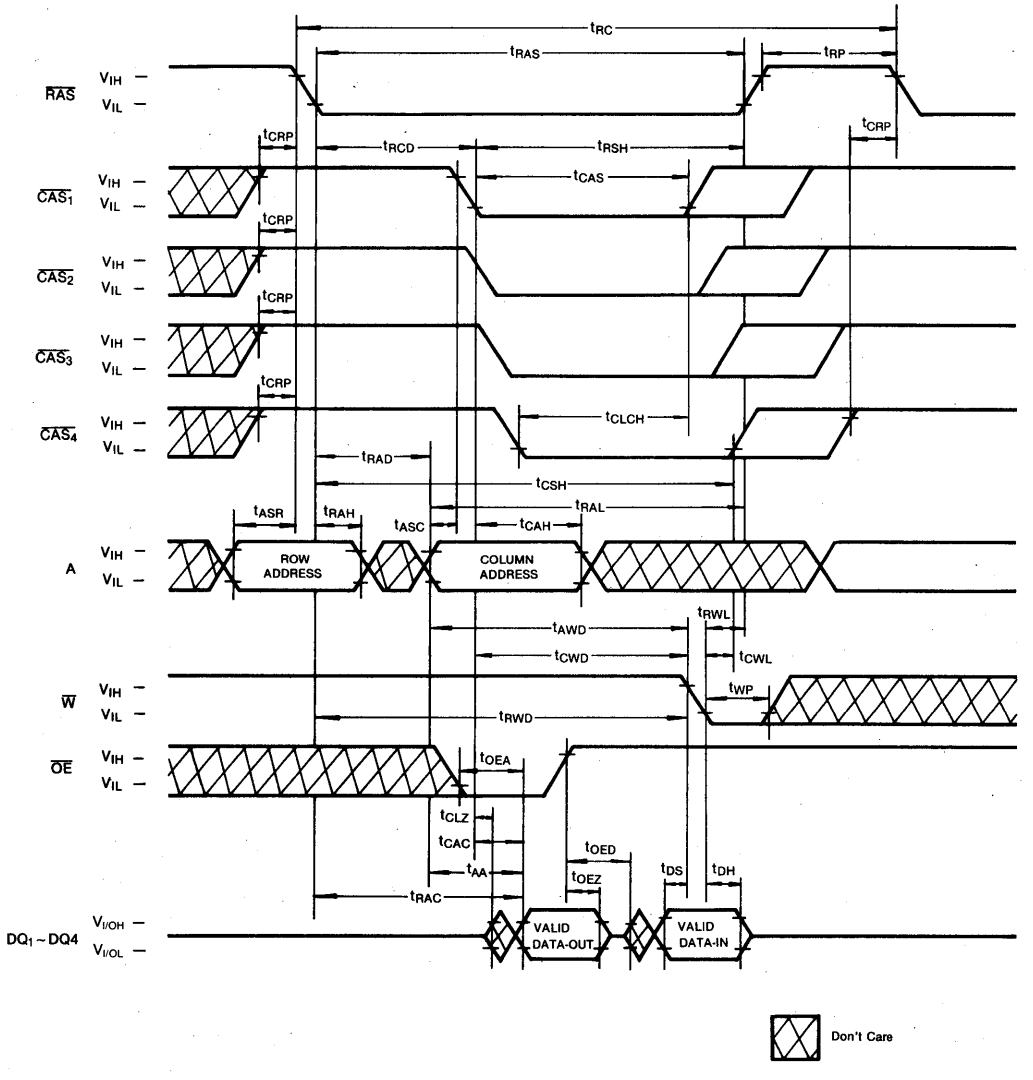
TIMING DIAGRAM (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



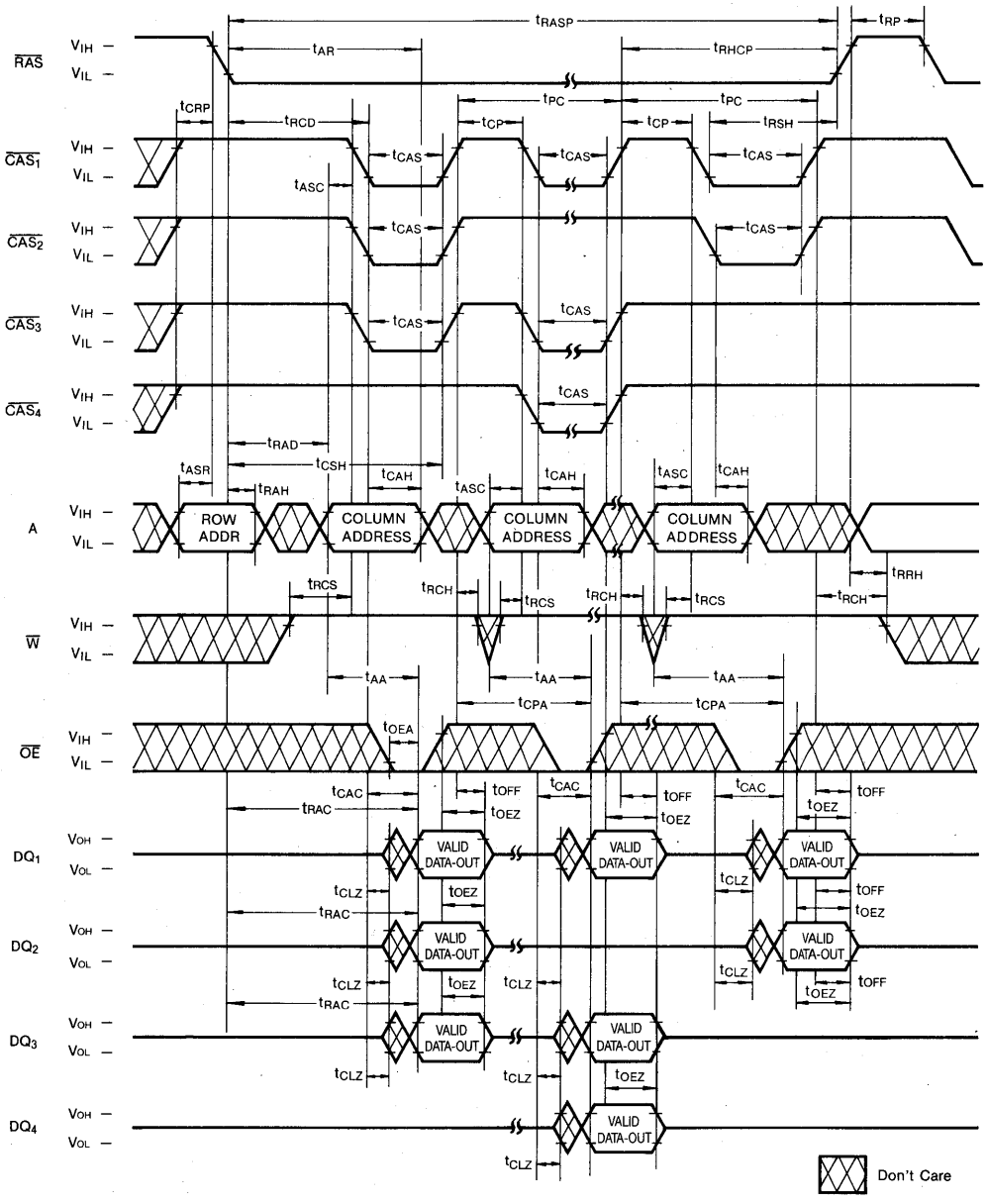
TIMING DIAGRAM (Continued)

READ-MODIFY-WRITE CYCLE



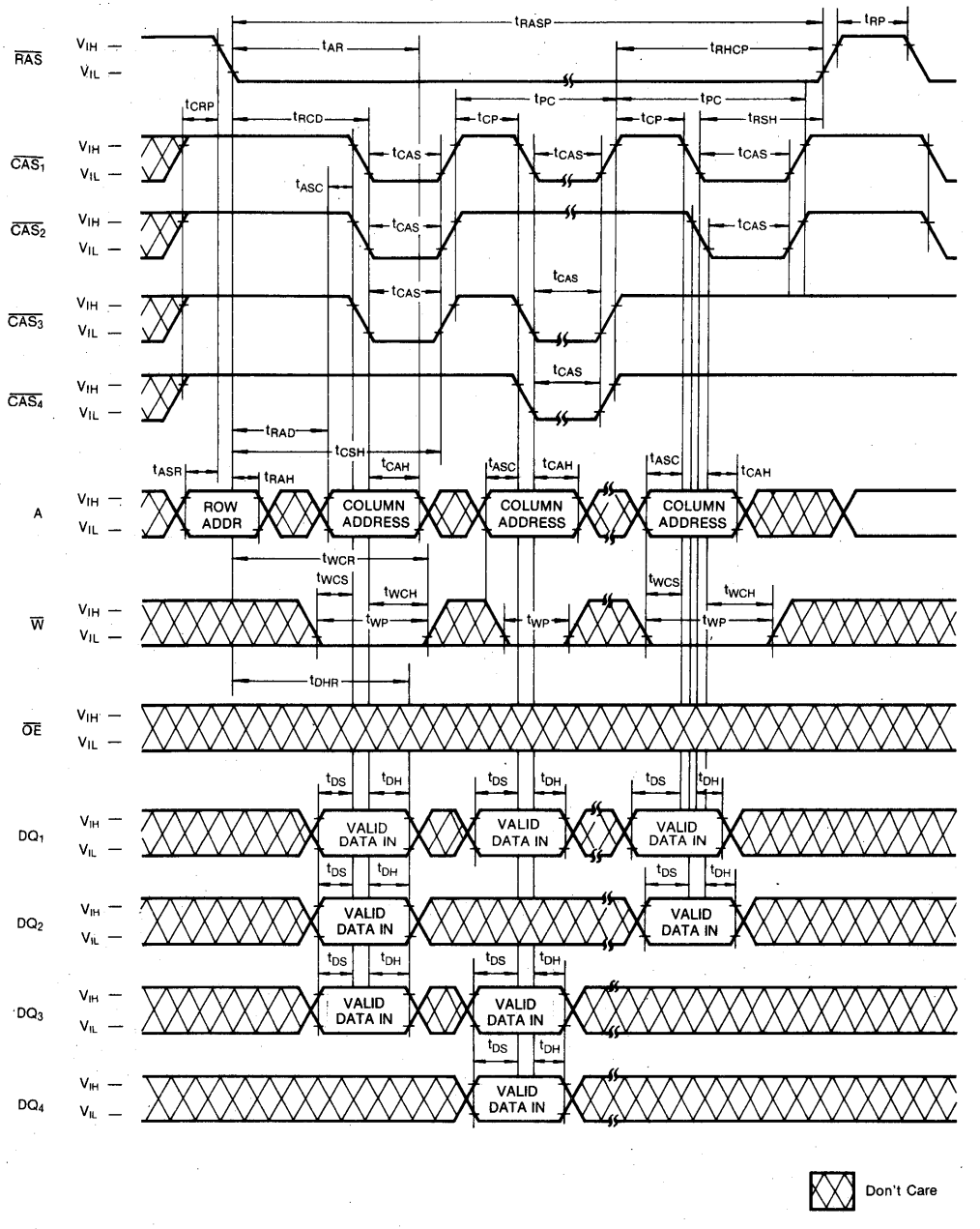
TIMING DIAGRAM (Continued)

FAST PAGE MODE READ CYCLE



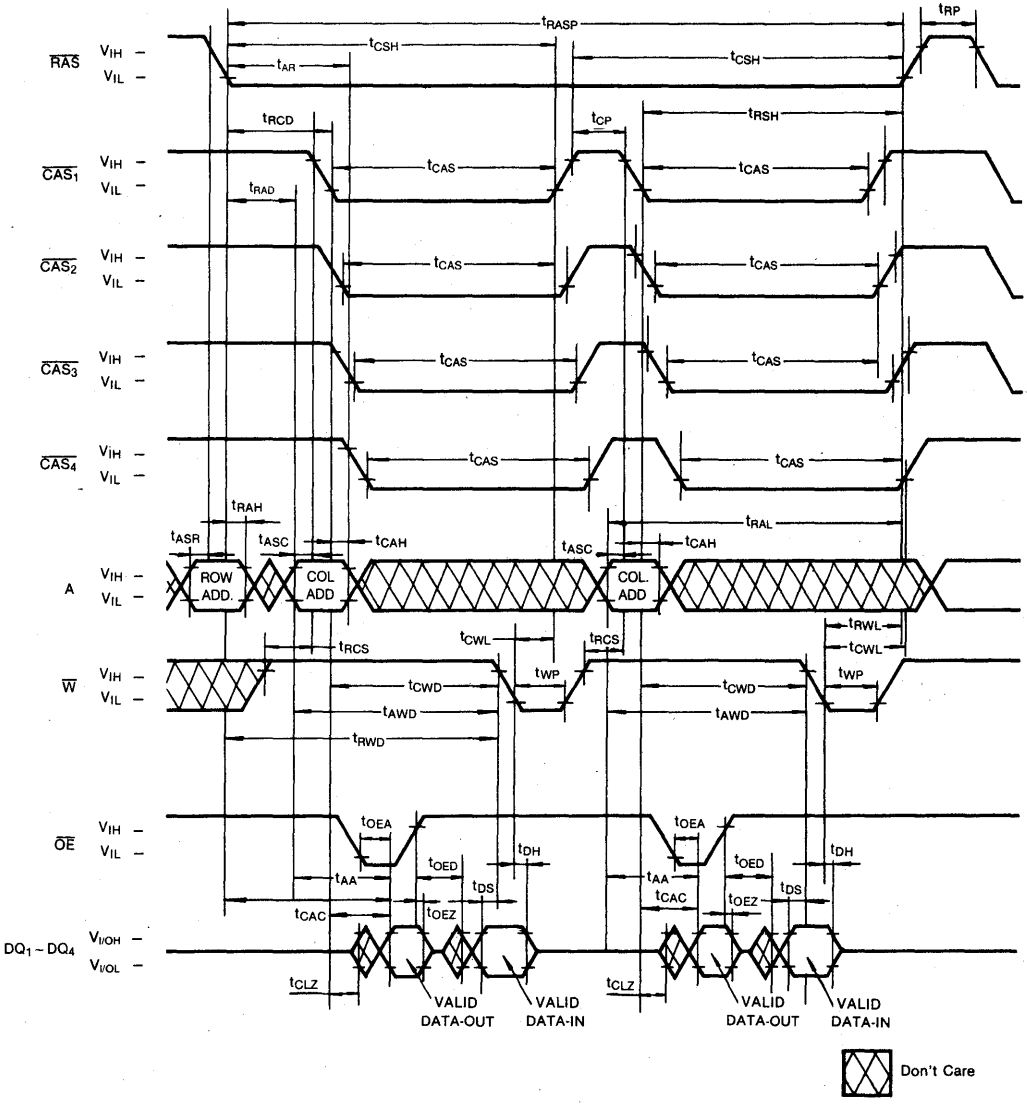
TIMING DIAGRAM (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAM (Continued)

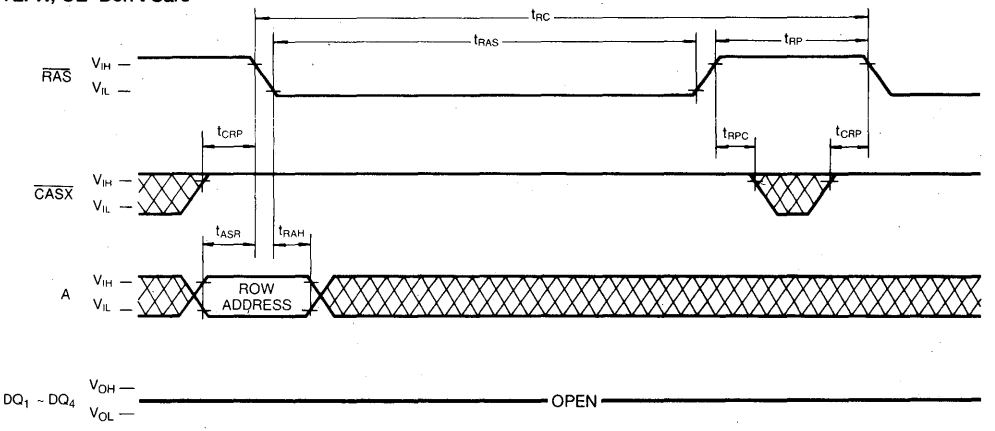
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

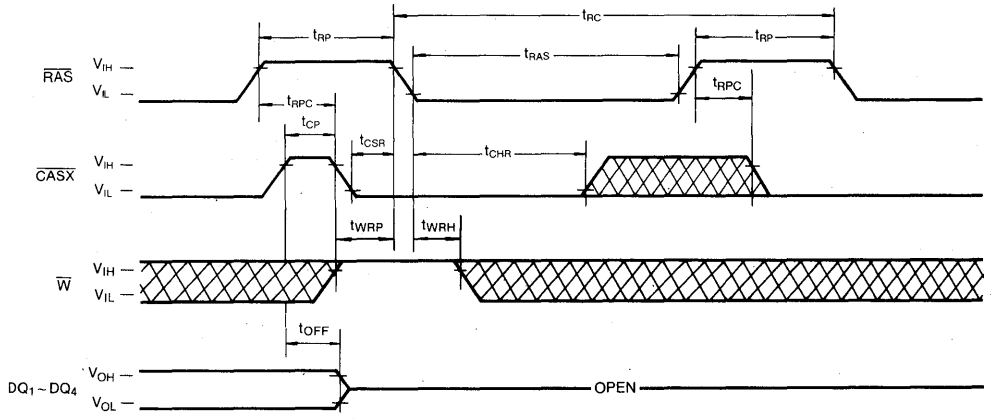
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

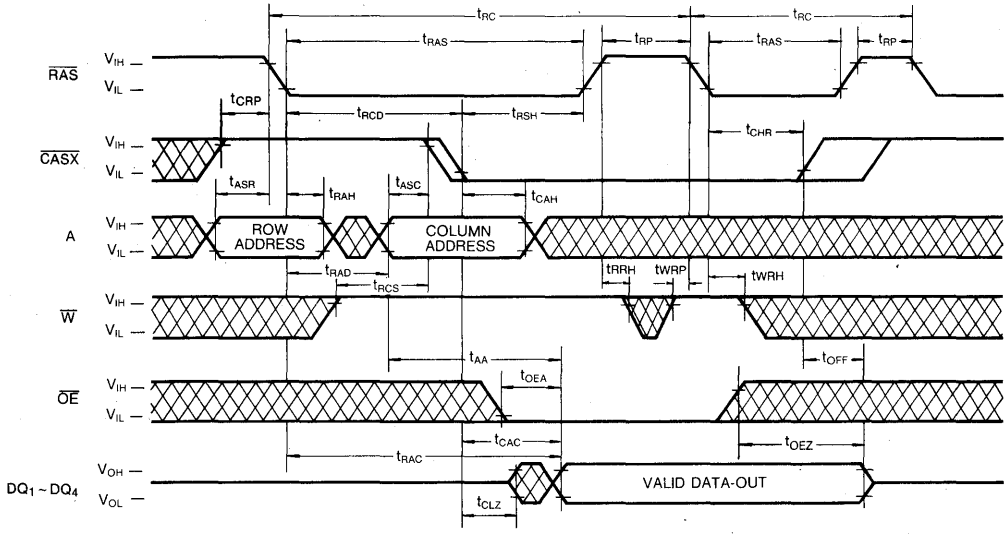
NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care



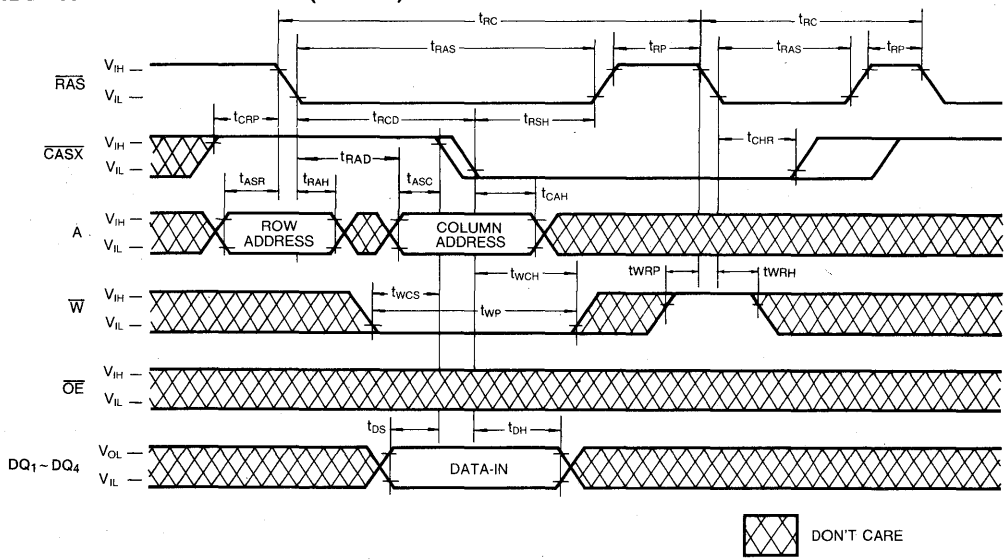
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

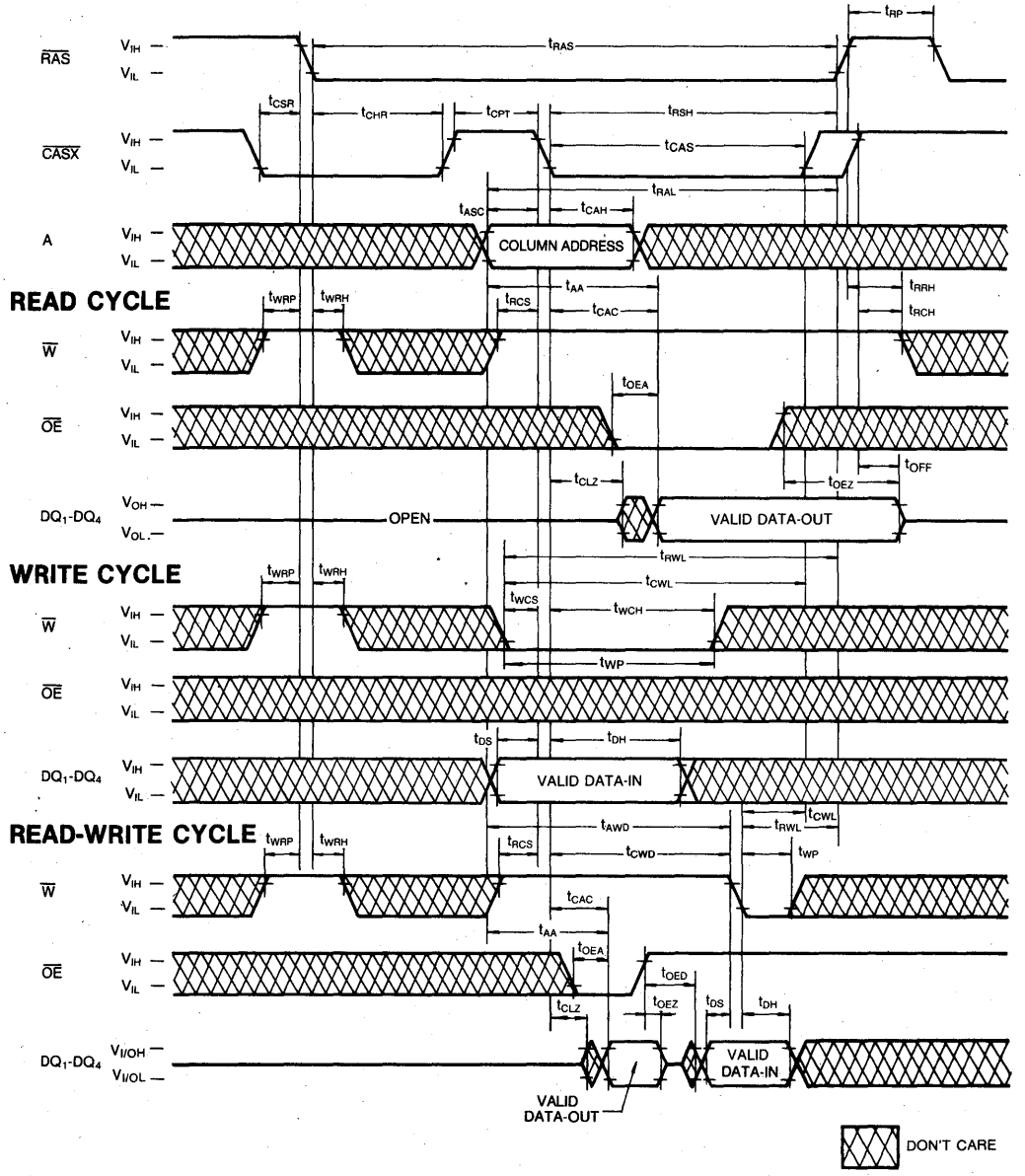


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

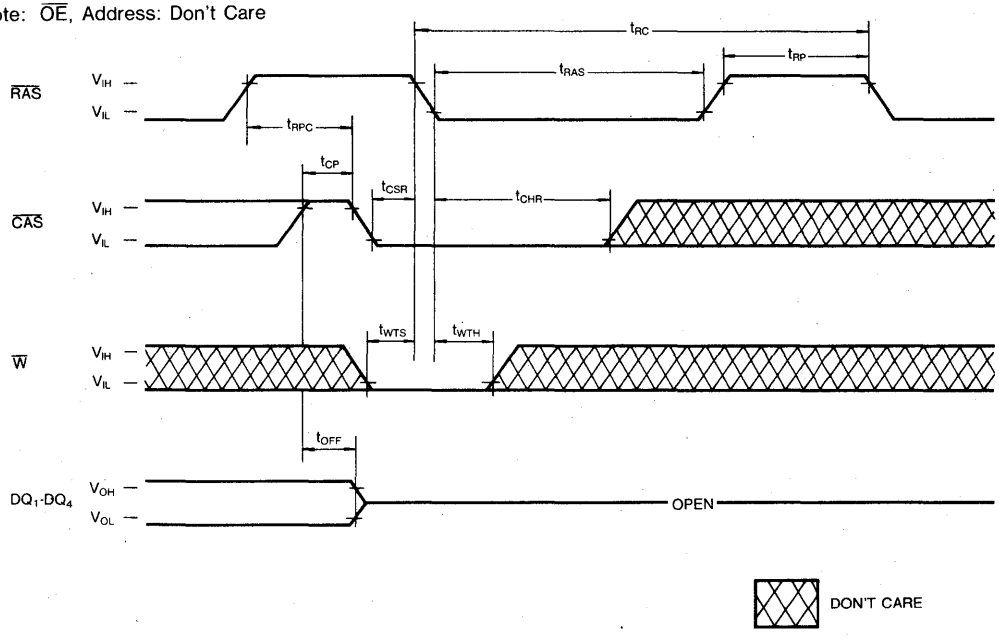


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



TEST MODE DESCRIPTION

The KM44C1003C/CL/CSL is the RAM organized 1, 048,576 words by 4 bit, it is internally organized 524, 288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

The KM44C1003C/CL/CSL contains 4,194,304 memory locations. Twenty address bit are required to address a particular 4-bit word in the memory array. Since the KM44C1003C/CL/CSL has only 10 address input pins, time multiplexed addressing is used to input 10 row (A_0~A_9) and 10 column(A_0~A_9) addresses. The multiplexing is controlled by the timing relationship between the row address strobe($\overline{RAS}$), the column address strobe($\overline{CASx}$) and the valid row and column address inputs.

Operating of the KM44C1003C/CL/CSL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CASx}$ remains high. Then the address on the 10 address input pins(A_0~A_9) is changed from a row address to a column address and is strobed in by $\overline{CASx}$. This is the beginning of any KM44C1003C/CL/CSL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CASx}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time(t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CASx}$ Timing

The minimum $\overline{RAS}$ and $\overline{CASx}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CASx}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1003C/CL/CSL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CASx}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CASx}$ and on the valid column address transition.

If $\overline{CASx}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAC}(max), then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CASx}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max). The KM44C1003C/CL/CSL has common data I/O pins. The this reason an output enable control input($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C1003C/CL/CSL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CASx}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CASx}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CASx}$. The data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the three state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CASx}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CASx}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C1003C/CL/CSL has a three-state output buffers which is controlled by $\overline{CASx}$ and $\overline{OE}$. Whenever $\overline{CASx}$ and $\overline{OE}$ are high (V_{IH}), the outputs are in the high impedance state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CASx}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CASx}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs(as in hidden refresh). Each of the KM44C-1003C/CL/CSL operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CASx}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM44C1003C/CL/CSL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CASx}$ remains high. This cycle must be repeated for each row.

$\overline{CASx}$-before-$\overline{RAS}$ Refresh: The KM44C1003C/CL/ CSL has $\overline{CASx}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CASx}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CASx}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CASx}$ active time and cycling $\overline{RAS}$. The KM44C1003C/CL/CSL hidden refresh cycle is actually a $\overline{CASx}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1003C/CL/CSL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CASx}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the $\overline{CASx}$ is cycled to strobe in additional column address. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CASx}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CASx}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CASx}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CASx}$-before-$\overline{RAS}$ refresh operation, is $\overline{CASx}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CASx}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address — Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address — Bits A_0 through A_9 are supplied by the falling edge of $\overline{CASx}$ as in a normal memory cycle.

Suggested $\overline{CASx}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CASx}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps.

1. Initialize the internal refresh counter by performing 8 $\overline{CASx}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2,3 and 4.

Power-up

If $\overline{RAS}$=V_{SS} during power-up, the KM44C1003C/CL/CSL could possibly begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CASx}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

DEVICE OPERATION (Continued)

An initial pause of 200 μsec is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. Eight initialization cycles are also required after any 64 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C1003C/CL/CSL inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminated the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C1003C/CL/CSL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transienteffects are minimized. the recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity(soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV.

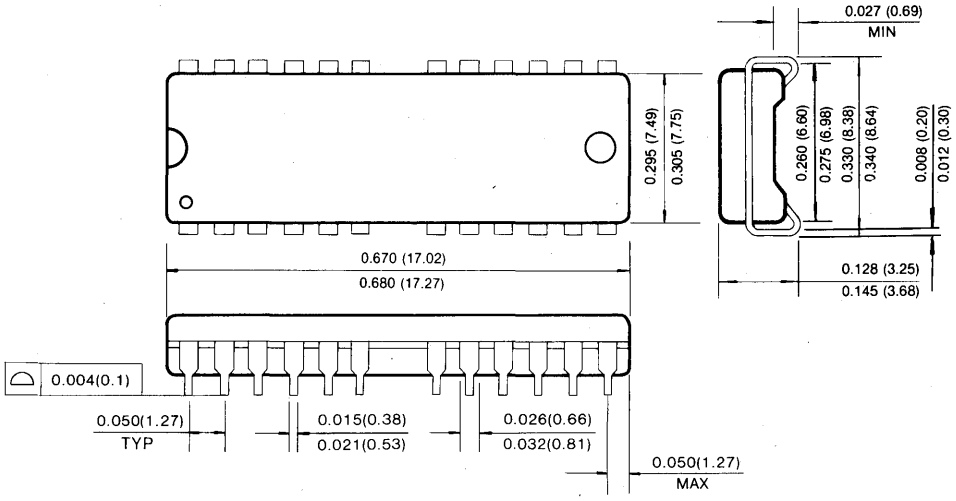
A high frequency 0.1 μF ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM44C1003C/CL/CSL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C1003C/CL/CSL and they supply much of the current used by the KM44C1003C/CL/CSL during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

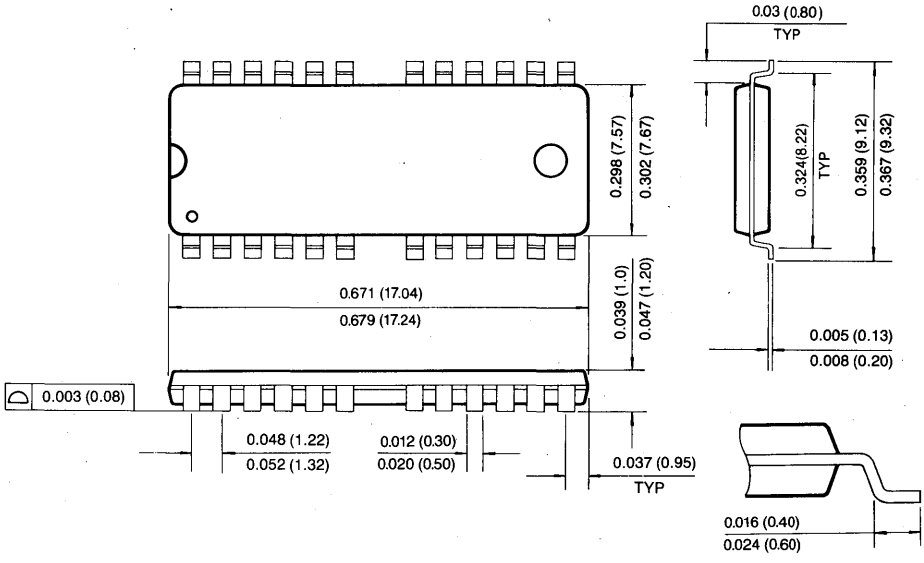
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



SAMSUNG ELECTRONICS

1M ×4Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM44C1004C/CL/CSL-5	50ns	13ns	90ns	20ns
KM44C1004C/CL/CSL-6	60ns	15ns	110ns	24ns
KM44C1004C/CL/CSL-7	70ns	20ns	130ns	29ns
KM44C1004C/CL/CSL-8	80ns	20ns	150ns	34ns

- **Fast Page Mode with Extended data out**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and hidden refresh capability**
- **Fast parallel test mode capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single + 5.0V ±10% power supply**
- **Refresh Cycle**
  - **— 1024 cycle/16ms (Normal)**
  - **— 1024 cycle/128ms (L-version)**
  - **— 1024 cycle/256ms (SL-version)**
- **Power Dissipation**
  - **— Standby: 5.5mW (Normal)**
    1.1mW (L-version)
    0.55mW (SL-version)
  - **— Active (50/60/70/80): 468/413/358/303mW**
- **JEDEC standard pinout**
- **Available in plastic DIP,SOJ,ZIP and TSOP -II packages**

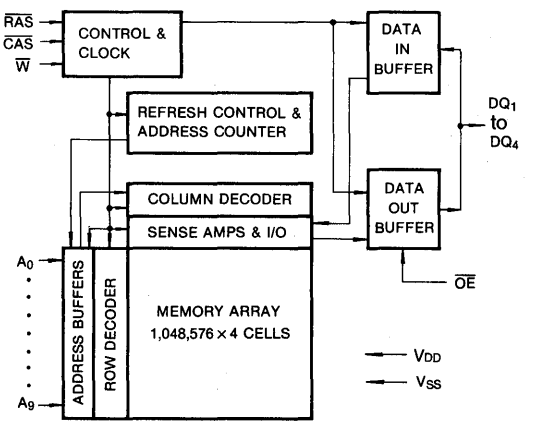
GENERAL DESCRIPTION

The Samsung KM44C1004C/CL/CSL is a high speed CMOS 1,048,576 × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1004C/CL/CSL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alterntive to $\overline{RAS}$-only Refresh. All inputs and outputs are fully TTL compatible.

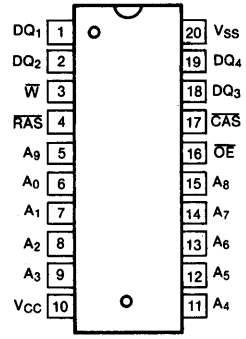
The KM44C1004C/CL/CSL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

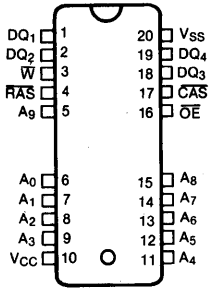


PIN CONFIGURATION (Top Views)

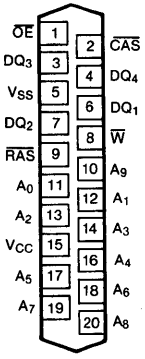
• KM44C1004CP/CLP/CSLP



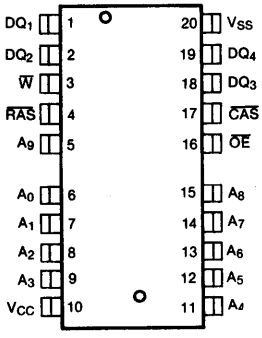
• KM44C1004CJ/CLJ/CSLJ



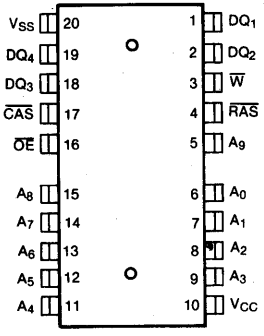
• KM44C1004CZ/CLZ/CSLZ



• KM44C1004CT/CLT/CSLT



• KM44C1004CTR/CLTR/CSLTR



Pin Names	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1~DQ_4	Data In/Data Out
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C1004C/CL/CSL-5	I_{CC1}	-	85	mA
	KM44C1004C/CL/CSL-6			75	mA
	KM44C1004C/CL/CSL-7			65	mA
	KM44C1004C/CL/CSL-8			55	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44C1004C	I_{CC2}	-	2	mA
	KM44C1004CL/CSL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM44C1004C/CL/CSL-5	I_{CC3}	-	85	mA
	KM44C1004C/CL/CSL-6			75	mA
	KM44C1004C/CL/CSL-7			65	mA
	KM44C1004C/CL/CSL-8			55	mA
EDO Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{HPC}=min.)	KM44C1004C/CL/CSL-5	I_{CC4}	-	85	mA
	KM44C1004C/CL/CSL-6			75	mA
	KM44C1004C/CL/CSL-7			65	mA
	KM44C1004C/CL/CSL-8			55	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM44C1004C	I_{CC5}	-	1	mA
	KM44C1004CL			200	μA
	KM44C1004CSL			100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C1004C/CL/CSL-5	I_{CC6}	-	85	mA
	KM44C1004C/CL/CSL-6			75	mA
	KM44C1004C/CL/CSL-7			65	mA
	KM44C1004C/CL/CSL-8			55	mA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Max	Units
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ1-DQ4=Don't Care, T_{RC}=125μS(L-Ver.) T_{RC}=250μS(SL-Ver.), T_{RAS}=T_{RAS} min.~300nS	KM44C1004CL KM44C1004CSL	I_{CC7}	-	300 150	μA μA
Input Leakage Current V_{CC}+0.5V (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once during a Hyper Page cycle.

3

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±0.5V, See notes 1,2)

Test condition: V_{IH}/V_{IL}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading C_L=100 pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	3	20	3	20	ns	7
Transition time(rise and fall)	t_T	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	40		50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10,000	10	10,000	15	10,000	20	10.000	ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		10		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Refresh period (SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		24		29		34		ns	16
Hyper Page read-modify-write cycle time	tHPRWC	62		73		88		98		ns	
$\overline{RAS}$ pulse width (Hyper Page Cycle)	tRASP	50	200,000	60	200,000	70	200,000	80	200,000	ns	
$\overline{CAS}$ precharge time (Hyper Page Cycle)	tCP	8		10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time (test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	7,15
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	7
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	tWPE	5		5		5		5		ns	

TEST MODE CYCLE

(Note.12)

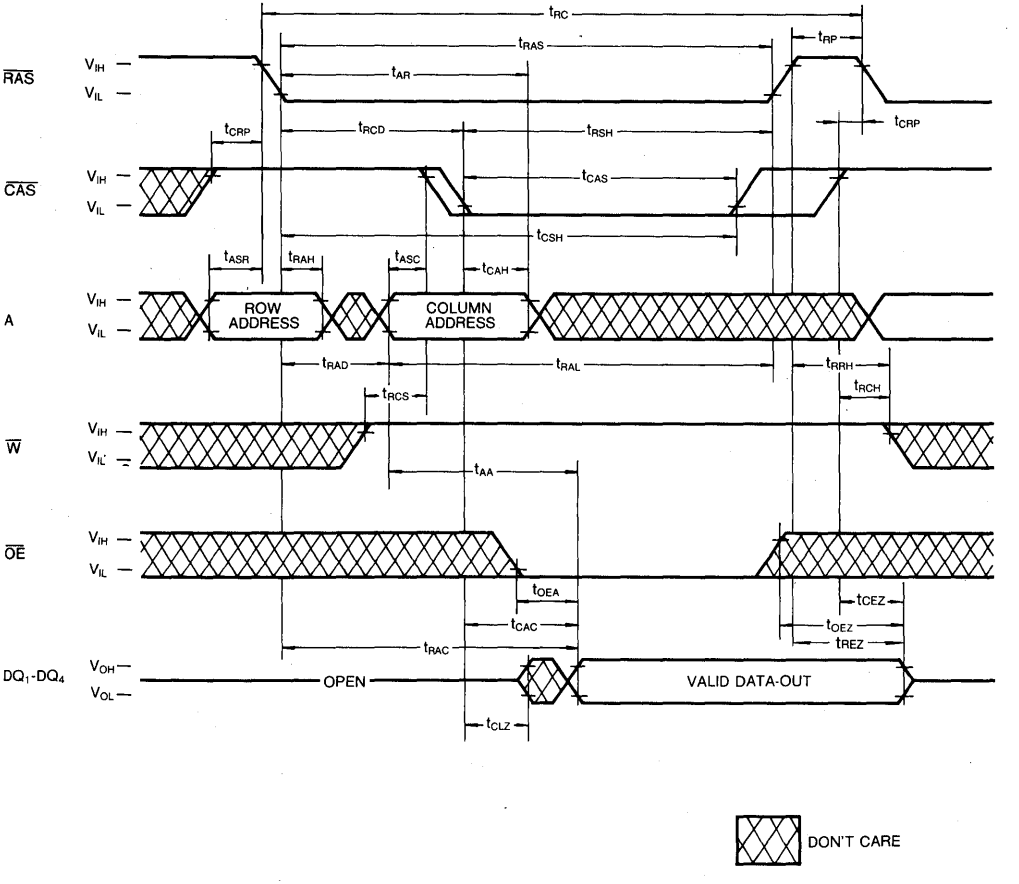
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	95		115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	138		160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		18		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	43		50		55		65		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	53		60		70		75		ns	8
Hyper Page cycle time	t_{HPC}	25		29		34		39		ns	
Hyper Page read-modify-write cycle time	t_{PRWC}	67		78		93		103		ns	
$\overline{RAS}$ pulse width (Hyper Page Cycle)	t_{RASP}	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45		50	ns	3
$\overline{OE}$ access time	t_{OEA}		18		20		25		25	ns	
$\overline{OE}$ to data delay	t_{OED}	18		20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	18		20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs, except t_{HPC} and t_{HPRWC}.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{CEZ}(max), t_{REZ}(max), t_{OEZ}(max) and t_{WEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
16. $t_{ASC} \geq t_{CP\ min}$, Assume t_T=2.0ns.

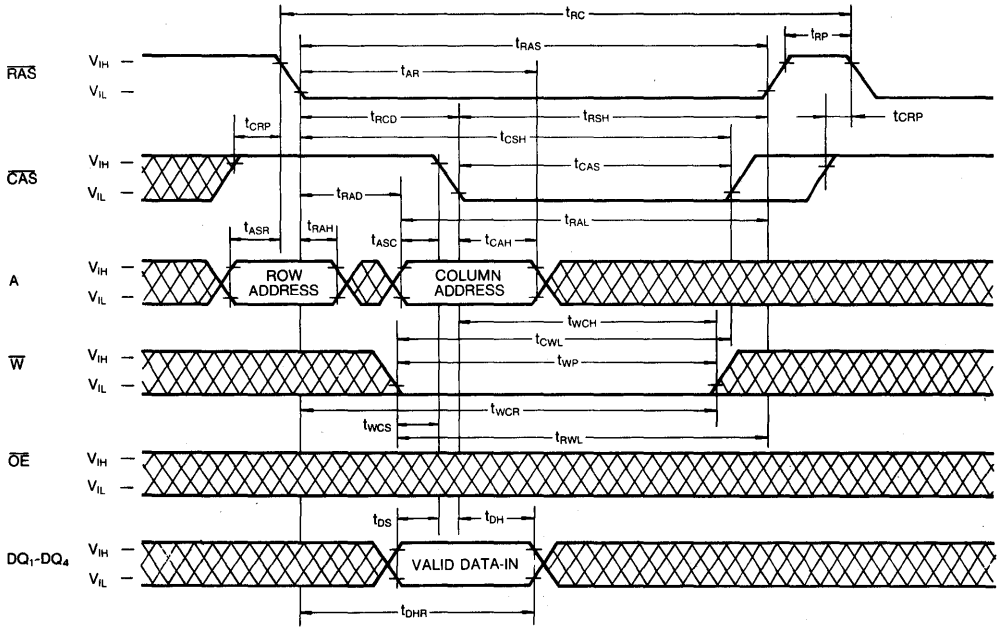
TIMING DIAGRAMS

READ CYCLE

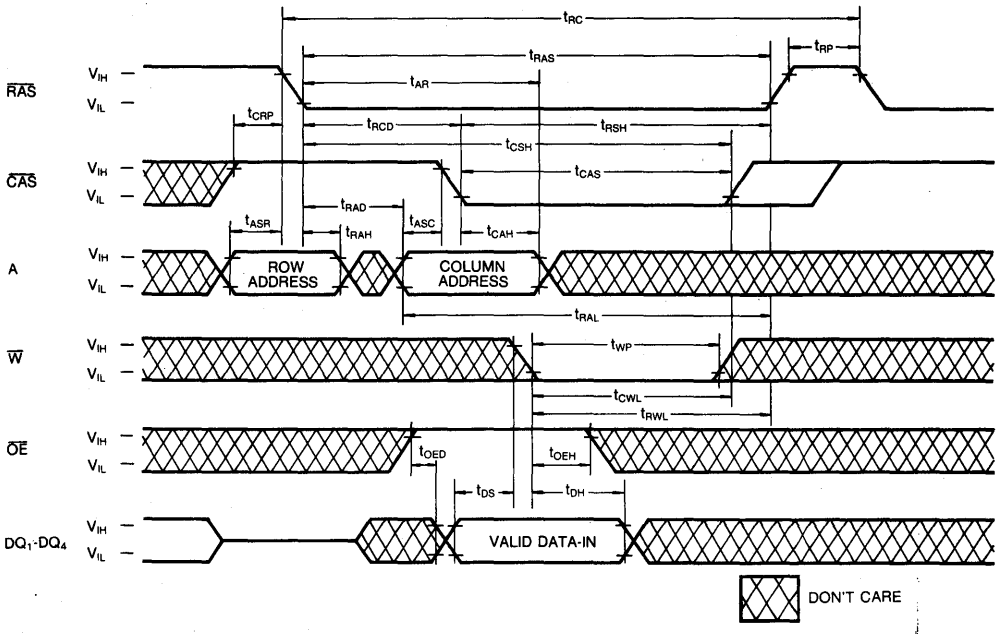


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)

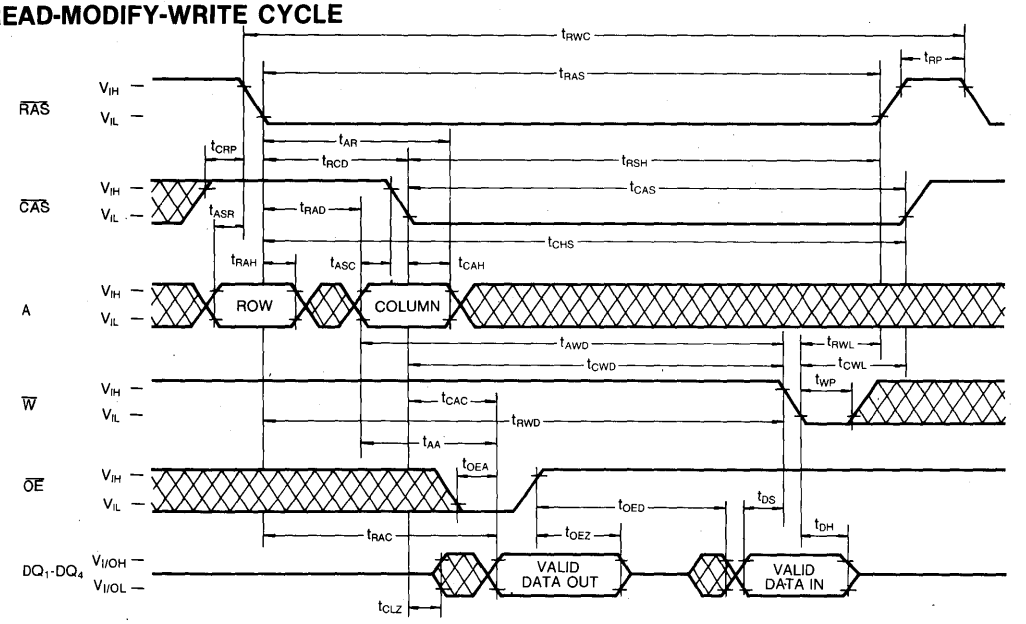


WRITE CYCLE (OE CONTROLLED WRITE)

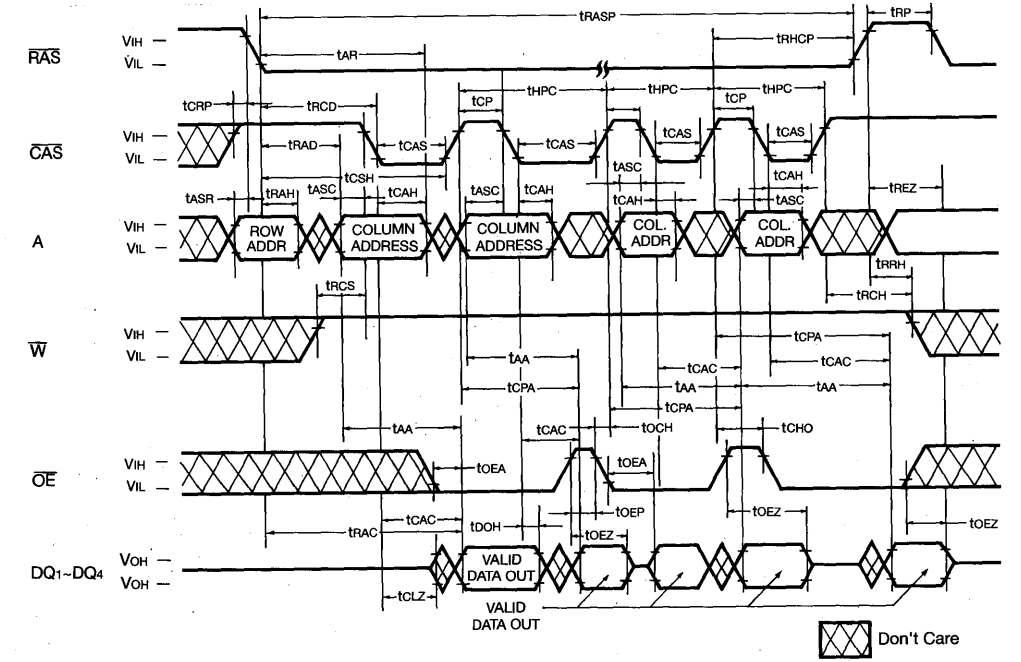


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



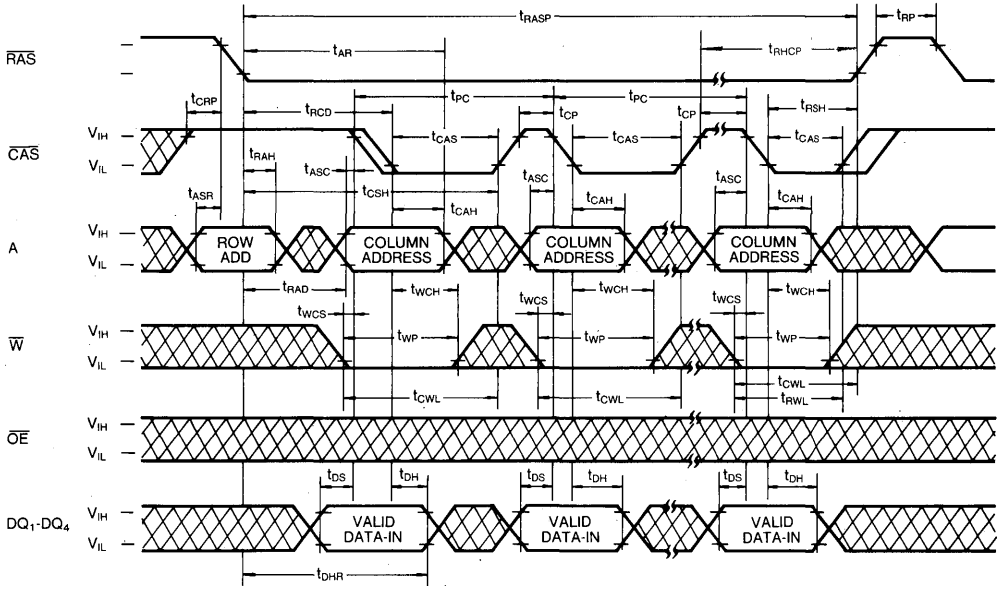
HYPER PAGE READ CYCLE



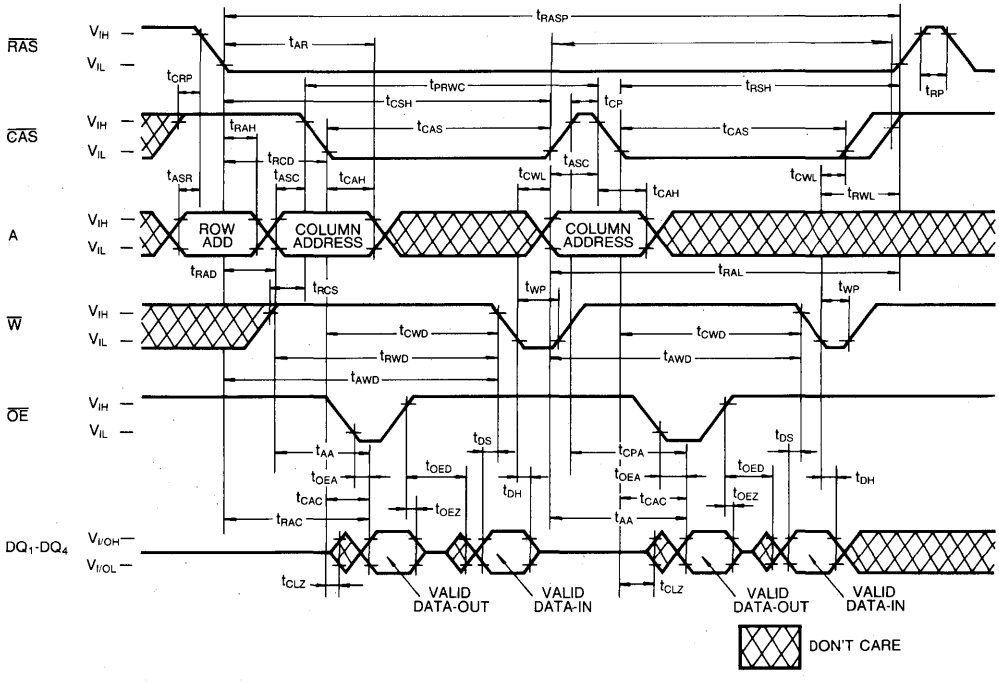
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

HYPER PAGE WRITE CYCLE (EARLY WRITE)

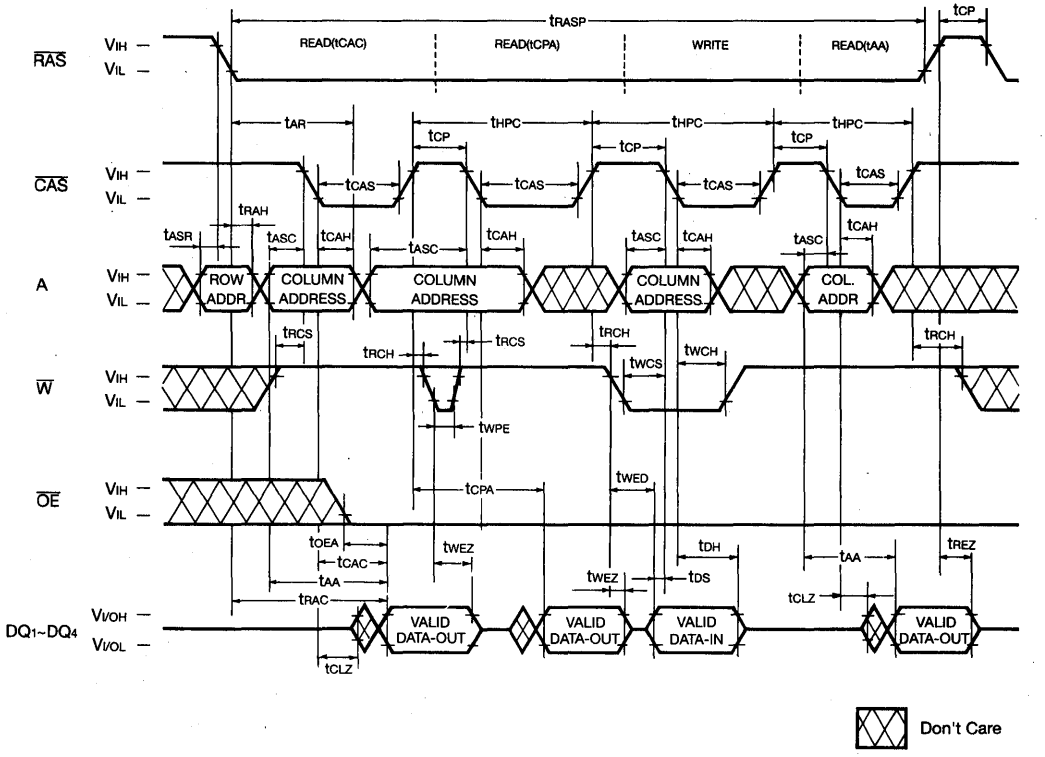


HYPER PAGE READ-MODIFY-WRITE CYCLE



SAMSUNG ELECTRONICS

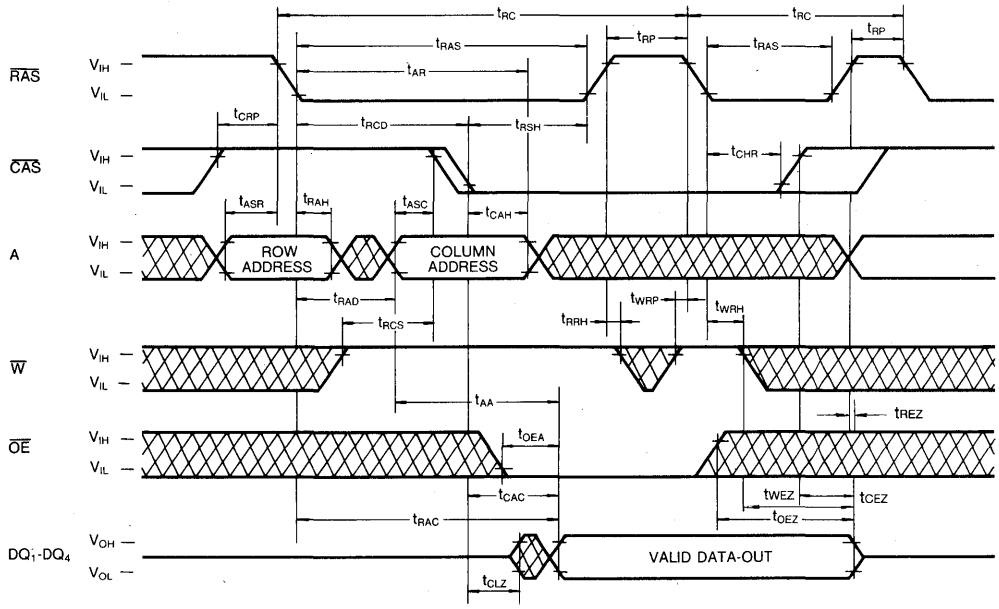
HYPER PAGE READ AND WRITE MIXED CYCLE



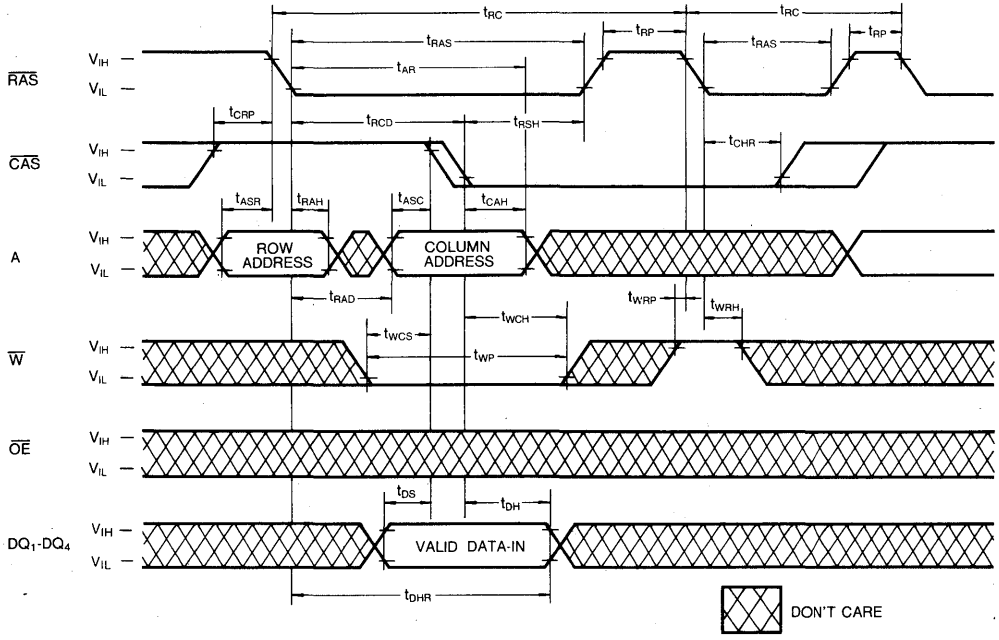
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

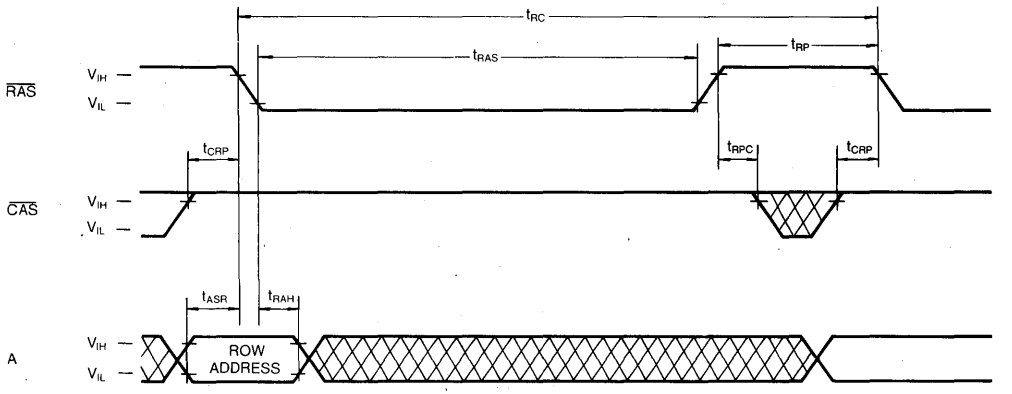


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

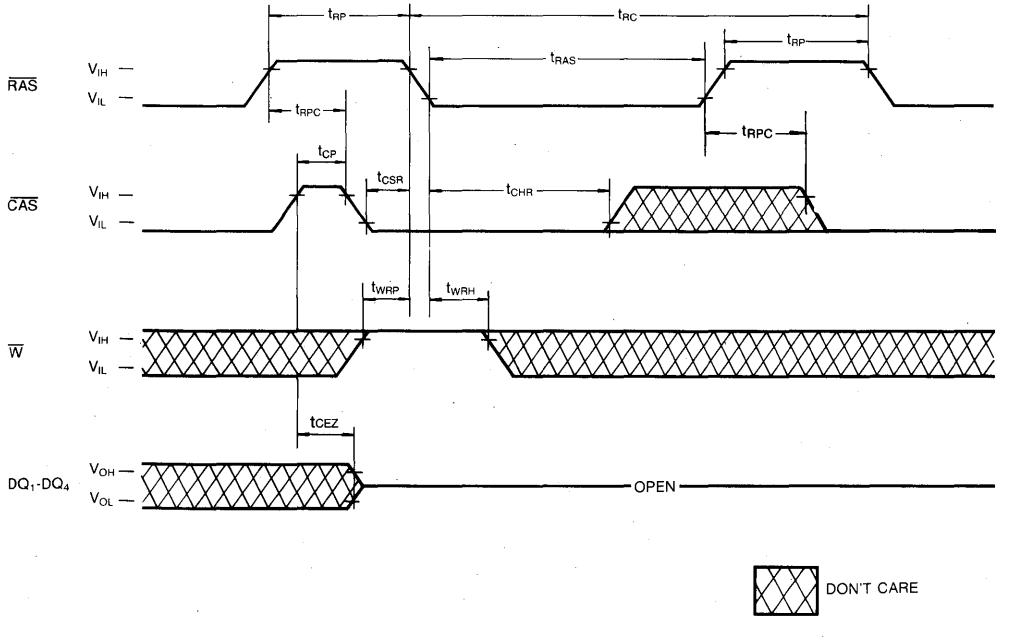
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

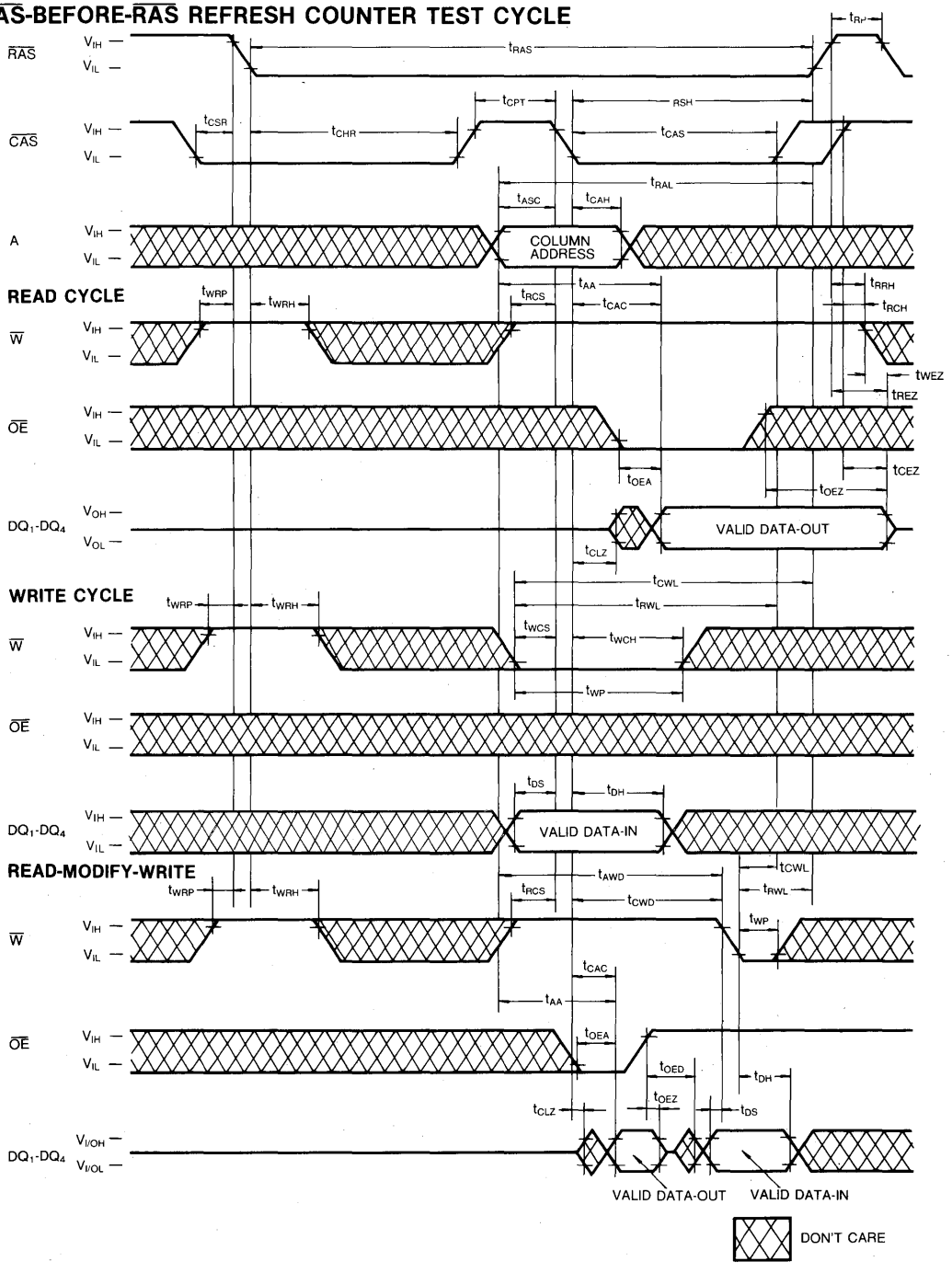
Note: $\overline{OE}$, Address=Don't Care



SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

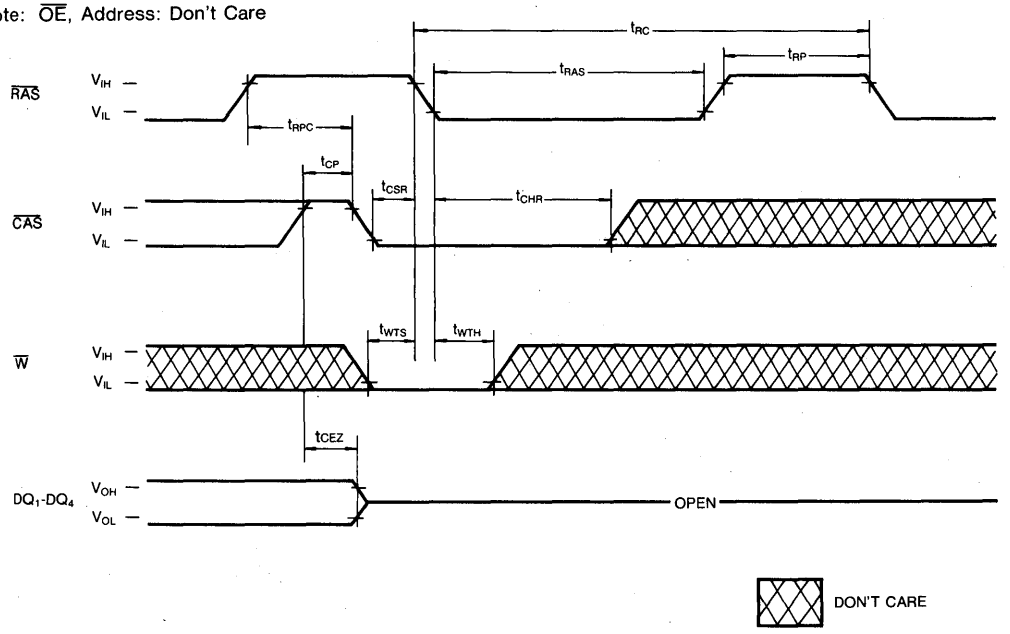
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



TEST MODE DESCRIPTION

The KM44C1004C/CL/CSL is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

The KM44C1004C/CL/CSL contains 4,194,304 memory locations. Twenty address bit are required to address a particular 4-bit word in the memory array. Since the KM44C1004C/CL/CSL has only 10 address input pins, time multiplexed addressing is used to input 10 row (A_0~A_9) and 10 column(A_0~A_9) address. The multiplexing is controlled by the timing relationship between the row address strobe($\overline{RAS}$), the column address strobe($\overline{CAS}$), and the valid row and column address inputs.

Operating of the KM44C1004C/CL/CSL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins(A_0~A_9) is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C1004C/CL/CSL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time(t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1004C/CL/CSL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAC}(max), then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC} (min), it is necessary to meet both t_{RCD}(max) and t_{RAD} (max). The KM44C1004C/CL/CSL has common data I/O pins. The this reason an output enable control input($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C1004C/CL/CSL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CAS}$. The data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the three state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C1004C/CL/CSL has a three-state output buffer which is controlled by $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. When $\overline{RAS}$ and $\overline{CAS}$ go high(V_{IH}) or $\overline{OE}$ goes high (V_{IH}), the outputs are in the high impedance state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data at the output cannot be eliminated by $\overline{CAS}$ rising only and it remains until both $\overline{RAS}$ and $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs(as in hidden refresh). Each of the KM44C1004C/CL/CSL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, EDO Mode Read, EDO Mode Read-Modify-Write.

DEVICE OPERATION (Continued)

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page with EDO Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM44C1004C/CL/CSL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16/128/256ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C1004C/CL/CSL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C1004C/CL/CSL hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1004C/CL/CSL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode with Extended Data Out

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address — Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address — Bits A_0 through A_9 are supplied by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps;

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycle, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2,3 and 4.

Power-up

If $\overline{RAS}$=V_{SS} during power-up, the KM44C1004C/CL/CSL could possibly begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current. An initial pause of 200 μsec is required after power-up followed by any 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 16(L-ver: 128, SL-ver:256) msec period in which there are no $\overline{RAS}$

DEVICE OPERATION (Continued)

cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C1004C/CL/CSL inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C1004C/CL/CSL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. the recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity(soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.1 μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C1004C/CL/CSL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C1004C/CL/CSL and they supply much of the current used by the KM44C1004C/CL/CSL during cycling.

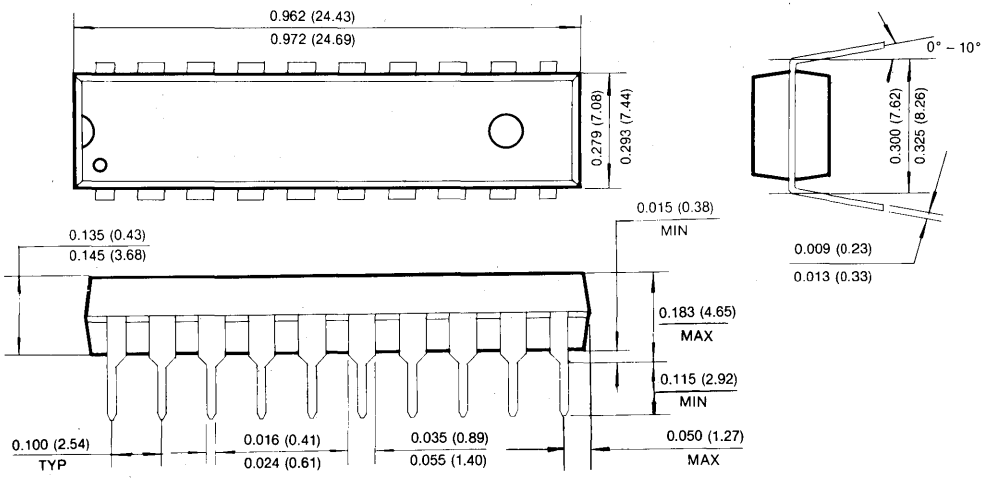
In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

3

PACKAGE DIMENSIONS

Units: Inches (Millimeters)

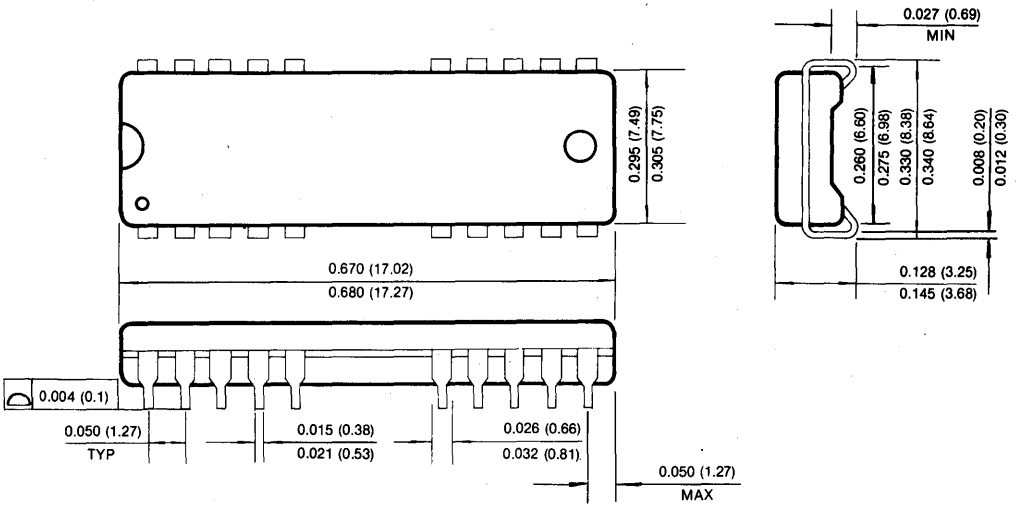
20-LEAD PLASTIC DUAL IN-LINE PACKAGE



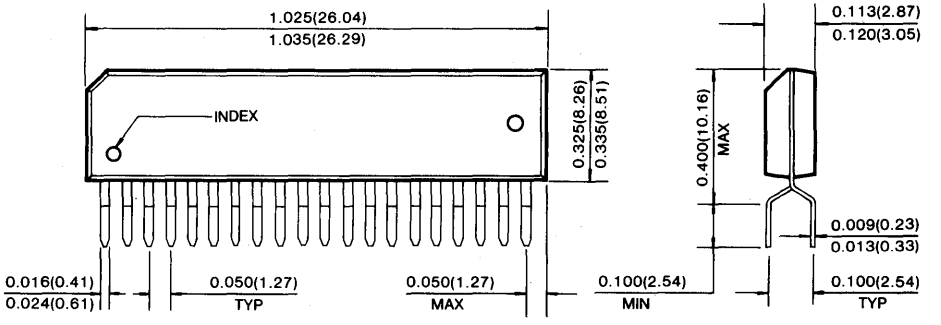
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

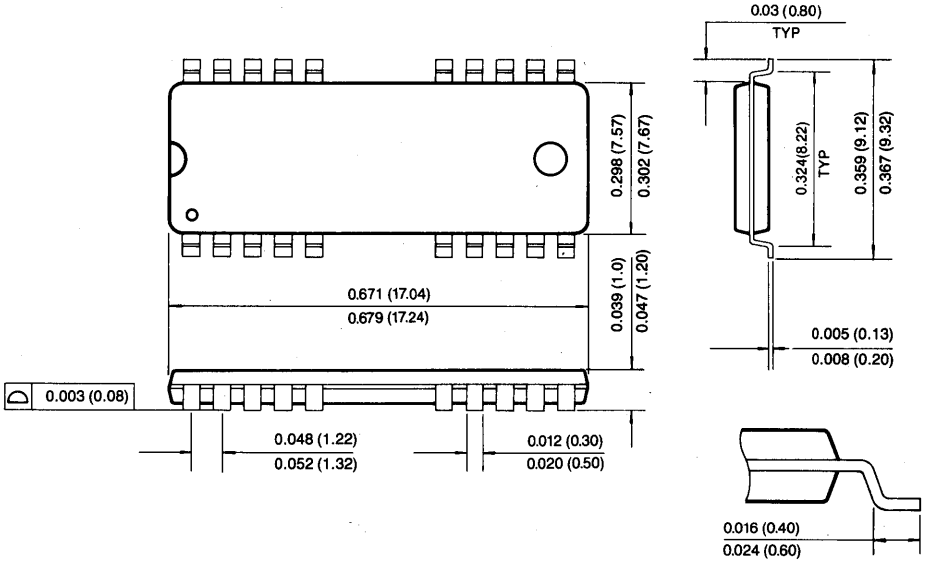


SAMSUNG ELECTRONICS

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



4M × 1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM41V4000C/CL/CLL-6	60ns	15ns	110ns
KM41V4000C/CL/CLL-7	70ns	20ns	130ns
KM41V4000C/CL/CLL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Self Refresh operation (LL-version)**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and hidden refresh capability**
- **Fast parallel test mode capability**
- **TTL compatible inputs and outputs**
- **Common I/O using early write**
- **Single + 3.3V ± 0.3V power supply**
- **Refresh Cycle**
  - **1024 cycle/16ms (Normal)**
  - **1024 cycle/128ms (L-version)**
  - **1024 cycle/128ms (LL-version)**
- **Power Dissipation**
  - **Standby: 3.6mW(Nomal)**
    0.18 mW(L-version)
    0.18mW(LL-version)
  - **Active (60/70/80ns):220/200/180mW**
- **JEDEC standard pinout**
- **Available in plastic SOJ, ZIP and TSOP II packages**

GENERAL DESCRIPTION

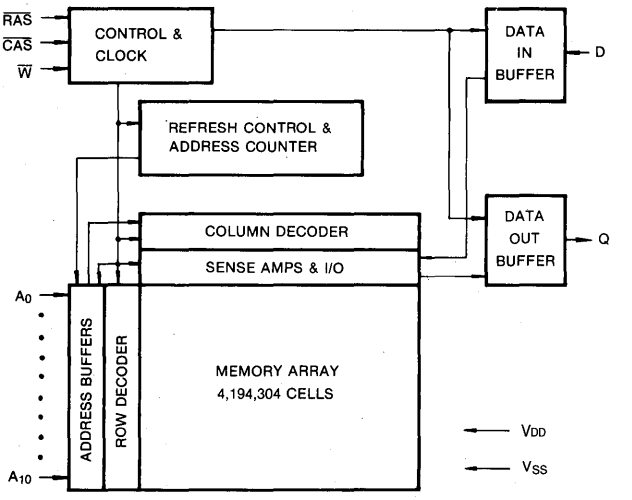
The Samsung KM41V4000C/CL/CLL is a high speed CMOS 4,194,304 bit × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41V4000C/CL/CLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capabillity provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

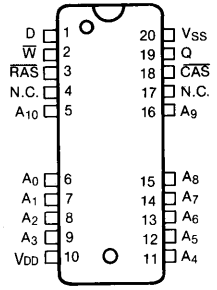
The KM41V4000C/CL/CLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

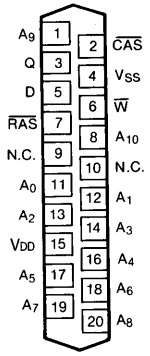


PIN CONFIGURATION (Top Views)

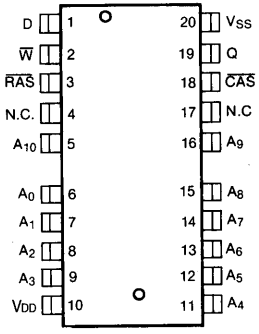
• KM41V4000CJ/CLJ/CLLJ



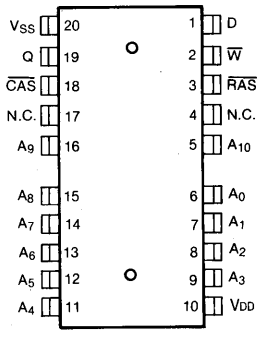
• KM41V4000CZ/CLZ/CLLZ



• KM41V4000CT/CLT/CLLT



• KM41V4000CTR/CLTR/CLLTR



Pin Names	Pin Function
A_0-A_{10}	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{DD}	Power (+3.3V)
V_{SS}	Ground
N.C.	No Connection

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SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5~V_{DD}+0.5	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5~4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, V_{DD} = 3.3V ± 0.3V)

Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Opernting Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	KM41V4000C/CL/CLL-6 KM41V4000C/CL/CLL-7 KM41V4000C/CL/CLL-8	I_{CC1}		60 55 50	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})		I_{CC2}		1	mA
RAS-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM41V4000C/CL/CLL-6 KM41V4000C/CL/CLL-7 KM41V4000C/CL/CLL-8	I_{CC3}		60 55 50	mA mA mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM41V4000C/CL/CLL-6 KM41V4000C/CL/CLL-7 KM41V4000C/CL/CLL-8	I_{CC4}		45 40 35	mA mA mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM41V4000C KM41V4000CL KM41V4000CLL	I_{CC5}		500 100 100	μA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM41V4000C/CL/CLL-6 KM41V4000C/CL/CLL-7 KM41V4000C/CL/CLL-8	I_{CC6}		60 55 50	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=125(L-ver) μS T_{RAS}=T_{RAS} min~300ns	KM41V4000CL	I_{CC7}		200	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=V_{IL} D=$\overline{W}$=A_0~A_{10}=D=V_{DD}-0.2V or 0.2V	KM41V4000CLL	I_{CCS}		150	μA

DC AND OPERATING CHARACTERISTICS(Continued)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0V)	$I_{I(L)}$	-10	10	μA
Output Leakge Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

* Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximun two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be canged maximun once during a Fast Page Mode Cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance(A_0-A_{10},D)	C_{IN1}	—	5	pF
Input Capacitance($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	7	pF
output Capacitance(Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	130		155		175		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time(rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	10		15		15		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Refresh period (L/LL-version)	t_{REF}		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to Write enable delay	t_{CWD}	15		20		20		ns	8
$\overline{RAS}$ to Write enable delay	t_{RWD}	60		70		80		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	30		35		40		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
$\overline{CAS}$ precharge time(fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
Fast page mode read-modify-write	t_{PRWC}	60		70		75		ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{PASS}	100		100		100		μs	13
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	110		130		150		ns	13
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	-50		-50		-50		ns	13

TEST MODE CYCLE

(Note. 12)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	135		160		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		45		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	20		25		25		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	65		75		85		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		45		ns	8
Fast mode cycle time	t_{PC}	45		50		55		ns	
Fast page modered-modify-write	t_{PRWC}	65		80		85		ns	
$\overline{RAS}$ pulse width(fast page mode)	t_{RASP}	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3

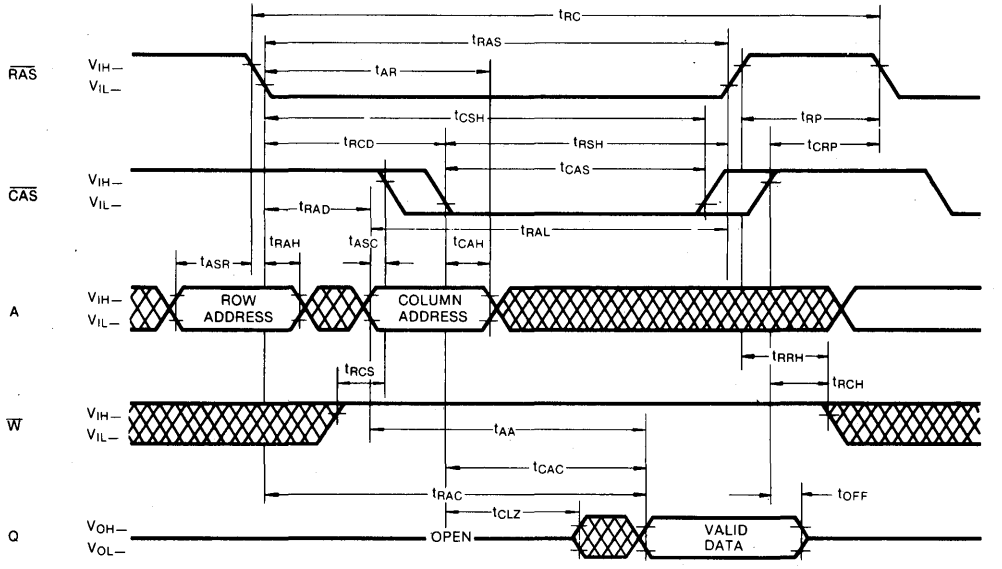
3

NOTES

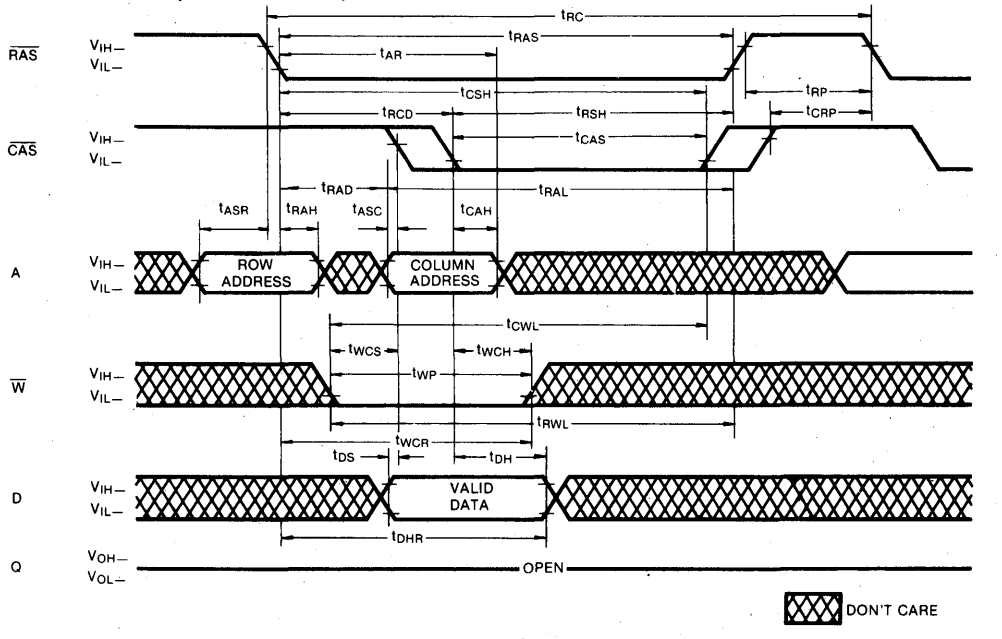
1. An initial pause of 200μs is required after power-up followed by and 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL load and 100pF, and Voh=2.0V, Vol=0.8V
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. 1024 cycle of Burst Refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification

TIMING DIAGRAMS

READ CYCLE

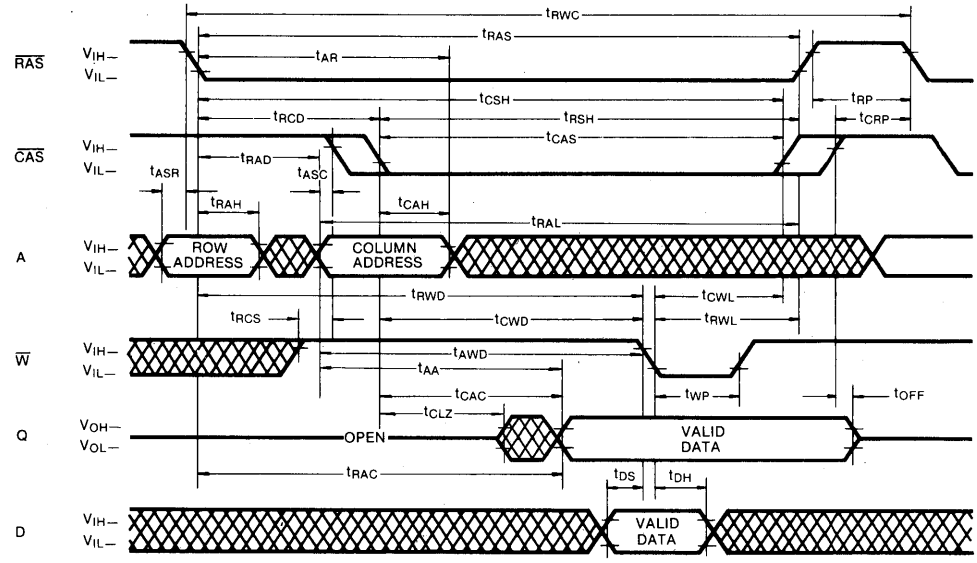


WRITE CYCLE (EARLY WRITE)

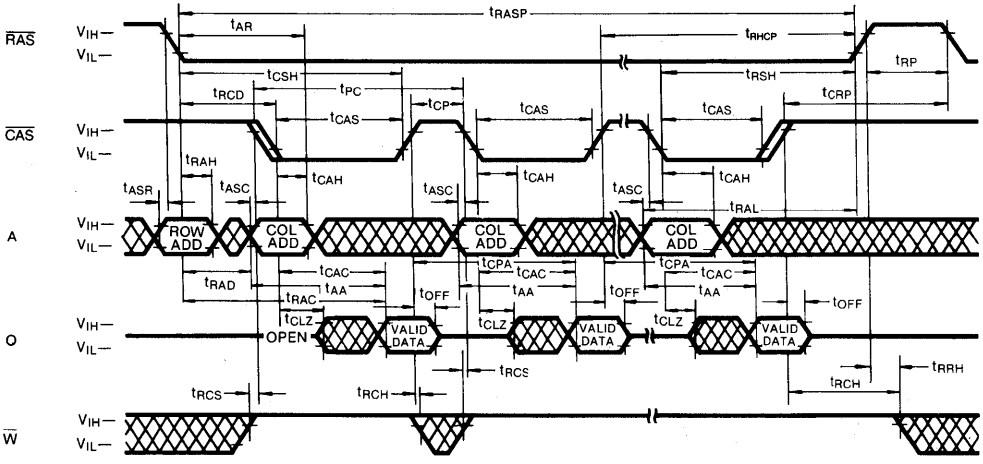


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



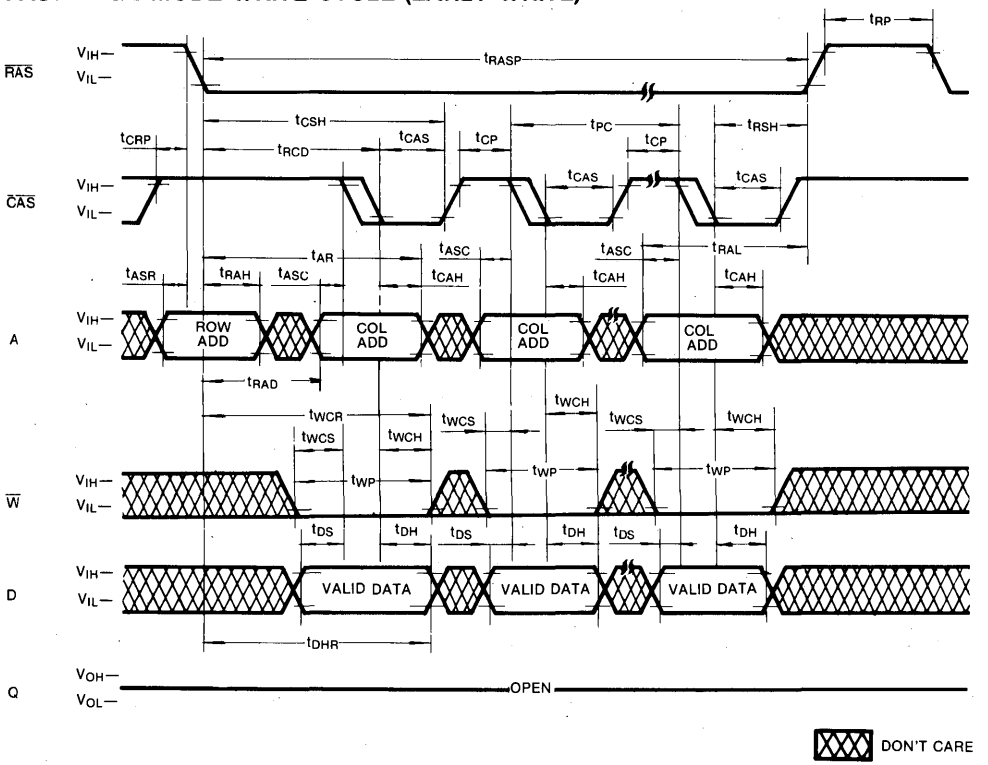
FAST PAGE MODE READ CYCLE



DON'T CARE

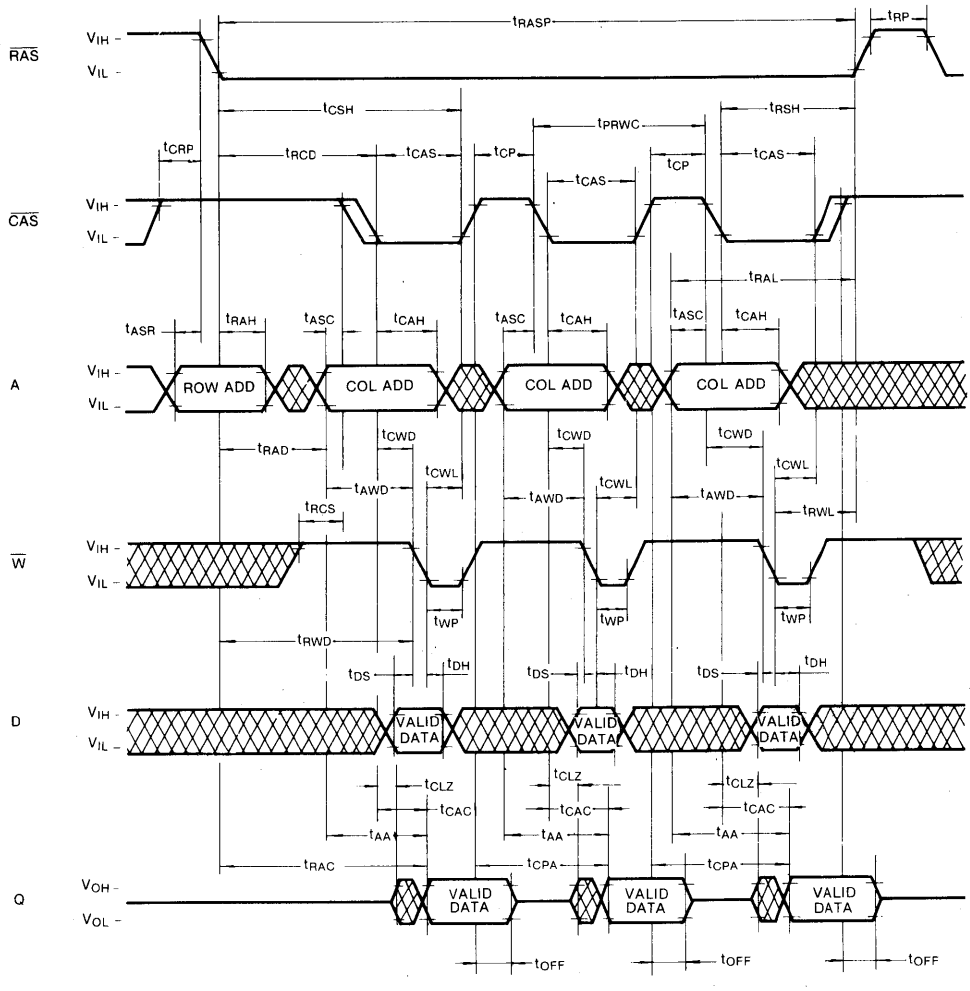
TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

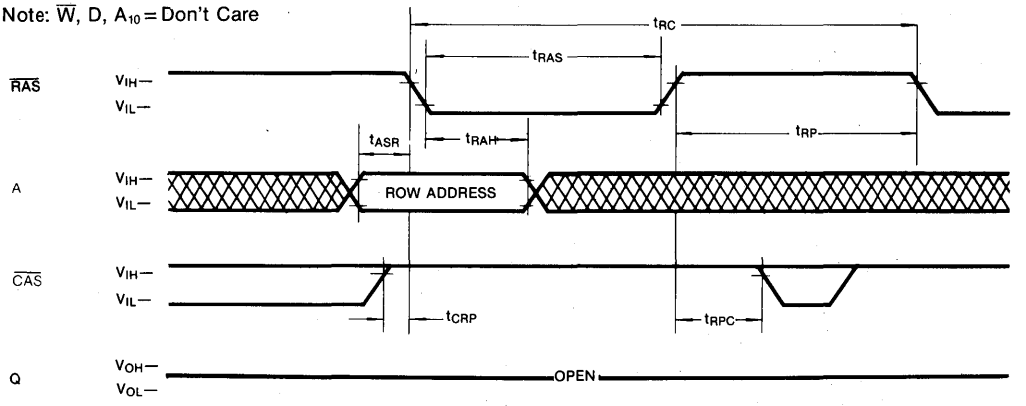
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

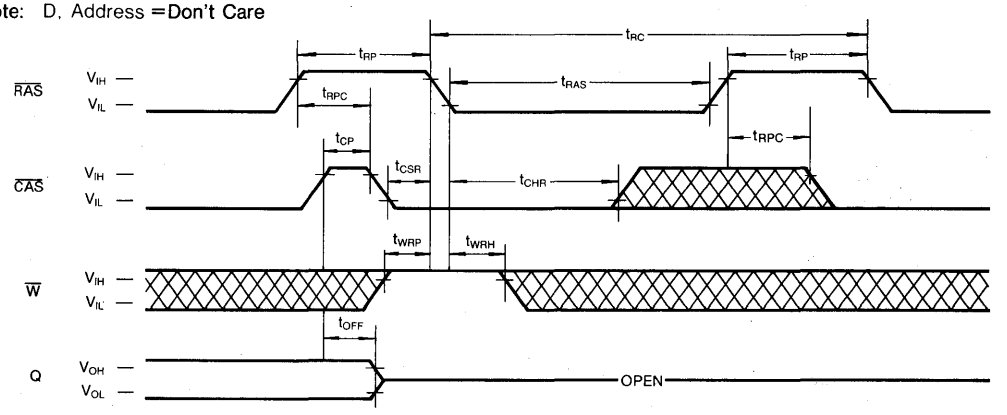
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, D, A_{10} = Don't Care



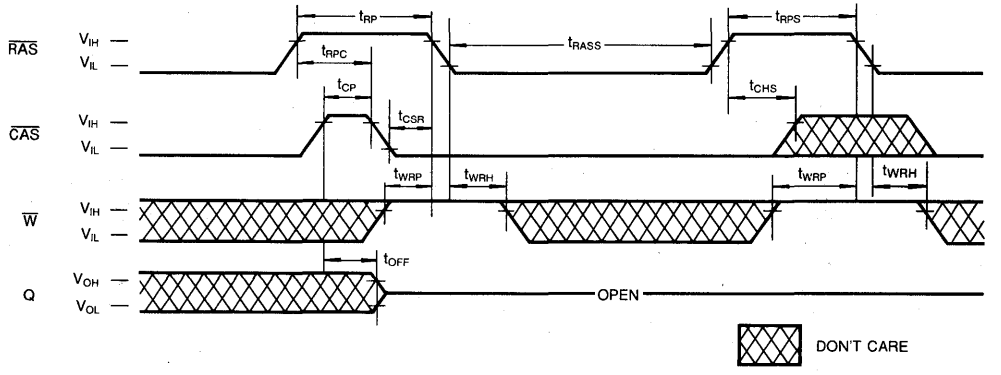
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

Note: D, Address = Don't Care



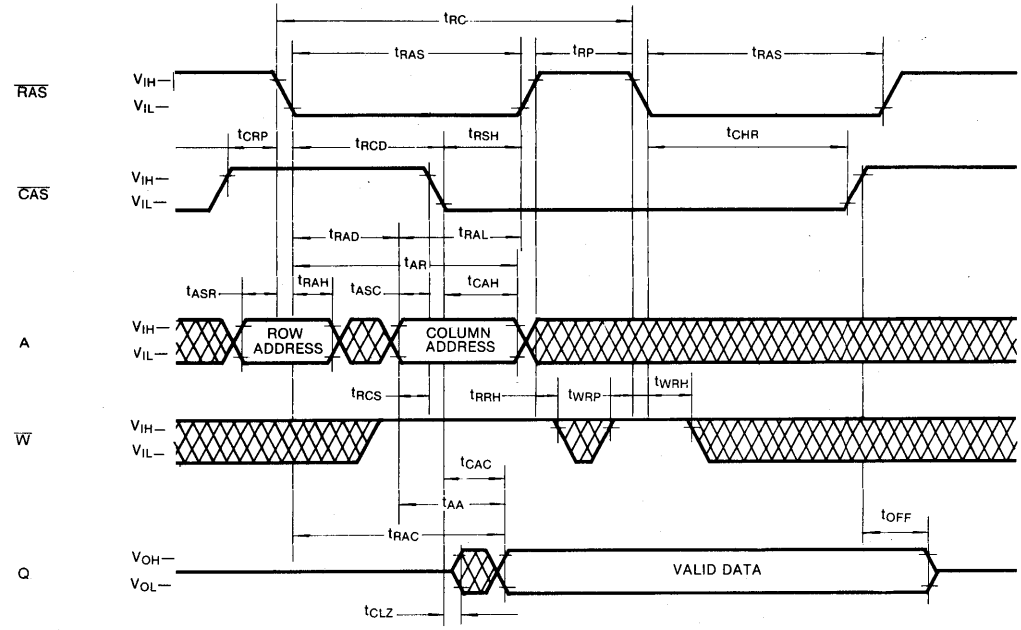
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-ver only)

Note: Address=Don't Care

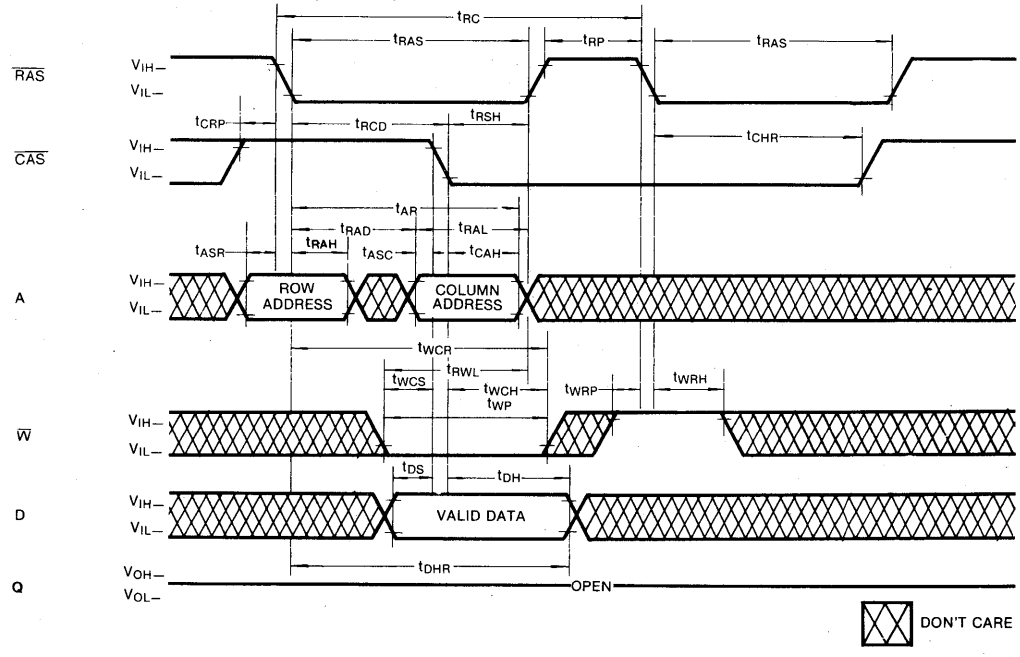


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

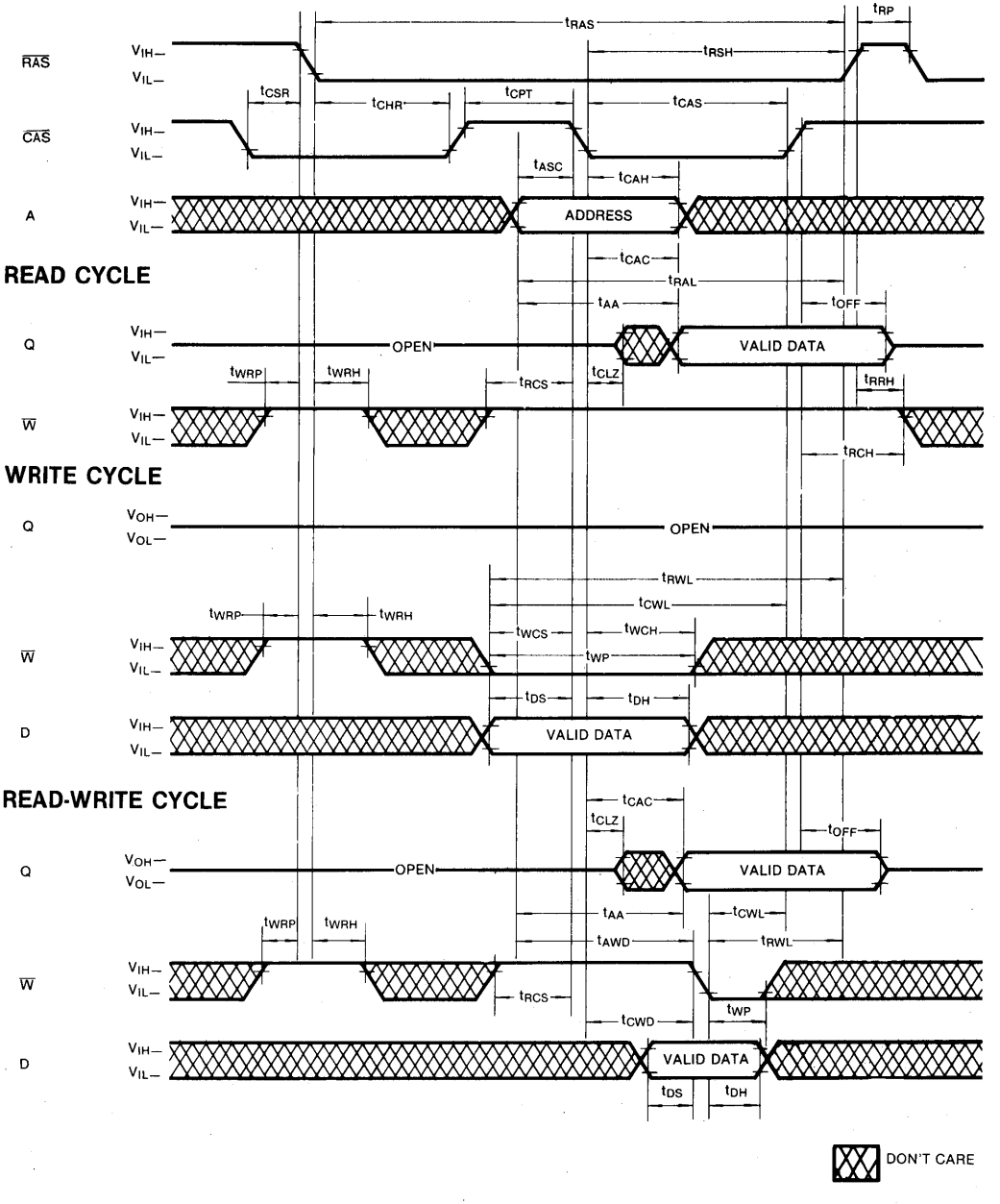


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

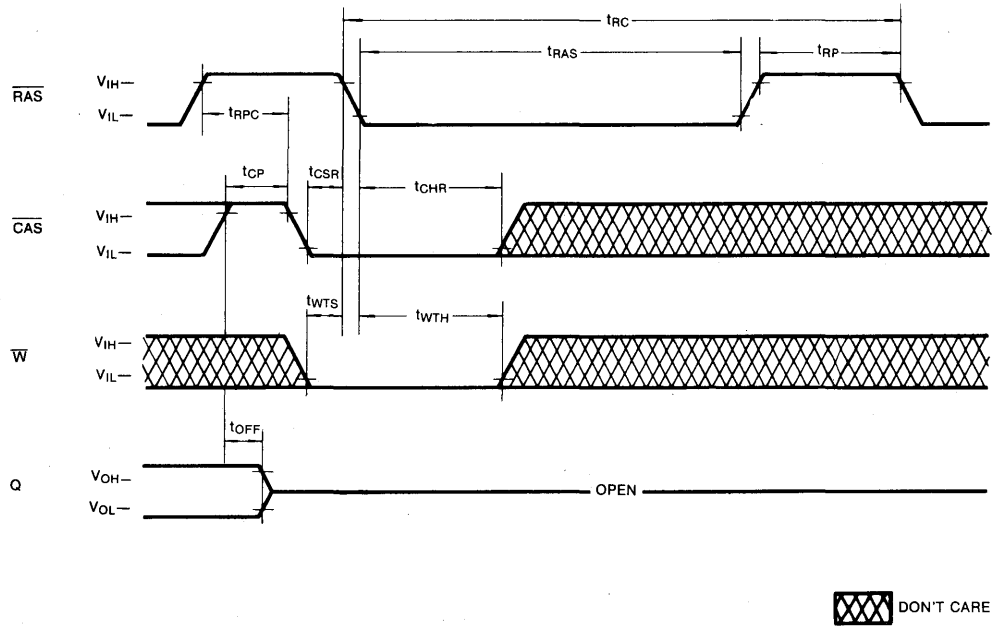
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM41V4000C/CL/CLL is the RAM organized 4, 194,304 words by 1 bit it is internally organized 524, 288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 and A_{10} are not used. If, upon reading, all bits are equal (all "1" or "0"s), the data output pin indicates a "1"If any of the bits differed the data output pin would indicate a "0". In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode", And "$\overline{CAS}$-Before-$\overline{RAS}$ Resfresh Cycle" or "$\overline{RAS}$-only-Refresh Cycle" puts it back into "Normal Mode". During the test mode operation, a WCBR cycle is used to perform refresh. The "Test Mode" function reduces test time(1/8 in cases of N test pattern.)

DEVICE OPERATION

Device Operation

The KM41V4000C/CL/CLL contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41V4000C/CL/CLL has only 11 address input pints, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column adress strobe($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM41V4000C/CL/CLL begins by strobing in valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41V4000C/CL/CLL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time(t_{RP}) requirement.

RAS and CAS Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respecitively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41V4000C/CL/CLL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input(W) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}(min). If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minmum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41V4000C/CL/CLL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. The cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing W low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41V4000C/CL/CLL has three-state output buffer which are controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high(V_{IH}), the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$, Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the putput. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41V4000C/CL/CLL operating cycles is listed below after the corresponding outout state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

DEVICE OPERATION (Continued)

The data in the KM41V4000C/CL/CLL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16(L,LL-ver:128ms). There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41V4000C/CL/CLL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation auto-matically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41V4000C/CL/CLL hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Self Refresh : The self refresh is $\overline{CAS}$-before-$\overline{RAS}$ refresh to be used for long periods of standby, such as al battery back-up. In nomal $\overline{CAS}$-befoerd-$\overline{RAS}$ condtion, when $\overline{RAS}$ is held low above 100 s an internal timer activates an refresh operation of consecutive row addersses in DRAM. The self refresh mode is exited when either $\overline{RAS}$ of $\overline{CAS}$ goes high(V_{IH}).

0ther Refresh Methods: It is also possible to refresh the KM41V4000C/CL/CLL by using read, write or read-modify write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM41V4000C/CL/CLL has Fast page mode capability. Fast page mode memory cycles provides faster access and lower power dissipation than normal memory cycles. In Fast page mode, it is possible to perform read, write or read-modify-write cyclels. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timingy diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address- Bits A_0 through A_9 are supplied by the on-chip refresh counter. This A_{10} bit is set high interally.

Column Address-Bits A_0 through A_{10} are strobed -in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by perfoming 8$\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test patten of "lows"into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS}$=V_{SS} during power-up,the KM41V4000C/CL/CLL could begin an active cycle. This condition results in

DEVICE OPERATION (Continued)

higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current. An initial pause of 200 μsec is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. Eight initialization cycles are also required after any 16 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41V4000C/CL/CLL inputs act like unterninated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel temination may be used,series temination is generally recommended since it is simple and draws on additional power. It consists of a resistor in series with the input line placed close to the KM41V4000C/CL/CLL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching trnsinent effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV.

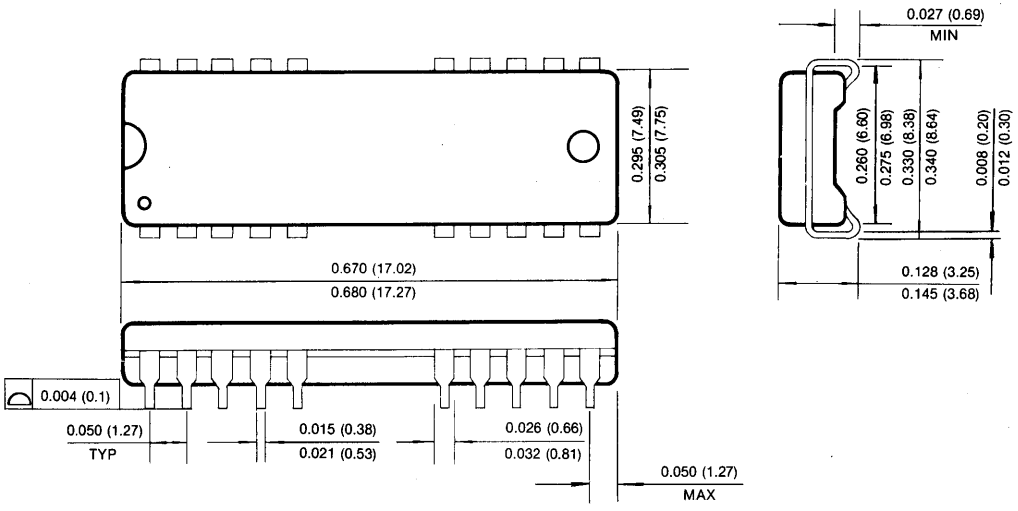
A high frequency 0.1 μF ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM41V4000C/CL/CLL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41V4000C/CL/CLL and they sypply much of the current used by the KM41V4000C/CL/CLL during cycling.

In anddition, a large tantalum capacitor with a value of 47μF to 100μF capacitors between cycles. thereby reducing power ling droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

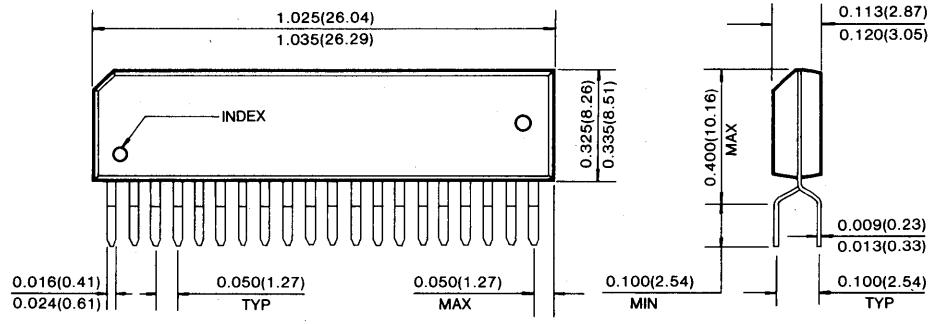
PACKAGE DIMENSIONS

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



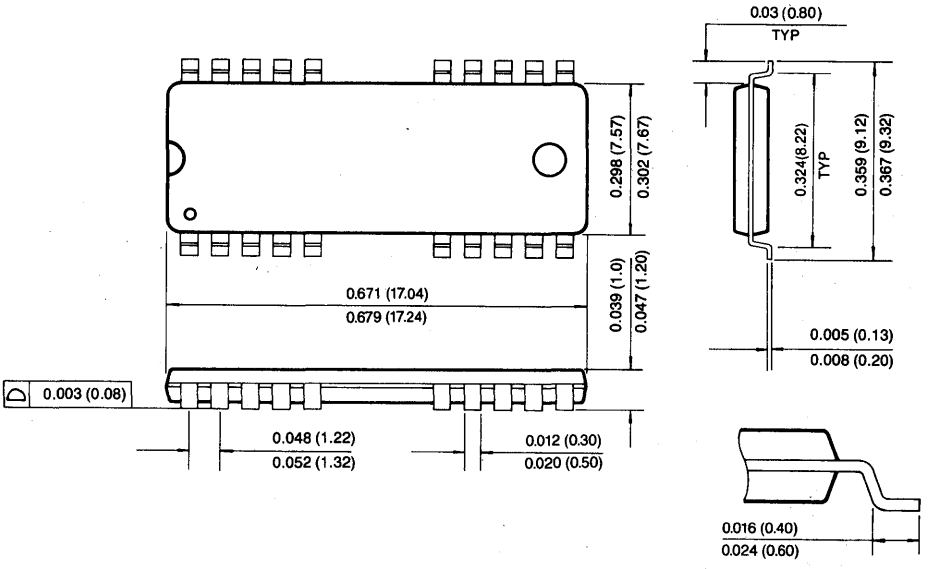
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



1M ×4Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM44V1000C/CL/CLL-6	60ns	15ns	110ns
KM44V1000C/CL/CLL-7	70ns	20ns	130ns
KM44V1000C/CL/CLL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Self Refresh operation (LL-version)**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and hidden refresh capability**
- **Fast parallel test mode capability.**
- **TTL compatible inputs and output**
- **Early write or output enable controlled write**
- **Single + 3.3V ± 0.3V power supply**
- **Refresh Cycle**
  - **1024 cycle/16ms (Normal)**
  - **1024 cycle/128ms (L-version)**
  - **1024 cycle/128ms (LL-version)**
- **Power dissipation**
  - **Standby: 3.6mW (Normal)**
    0.18mW(L-version)
    0.18mW(LL-version)
  - **Active (60/70/80ns):220/200/180mW**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP and TSOP -II packages**

GENERAL DESCRIPTION

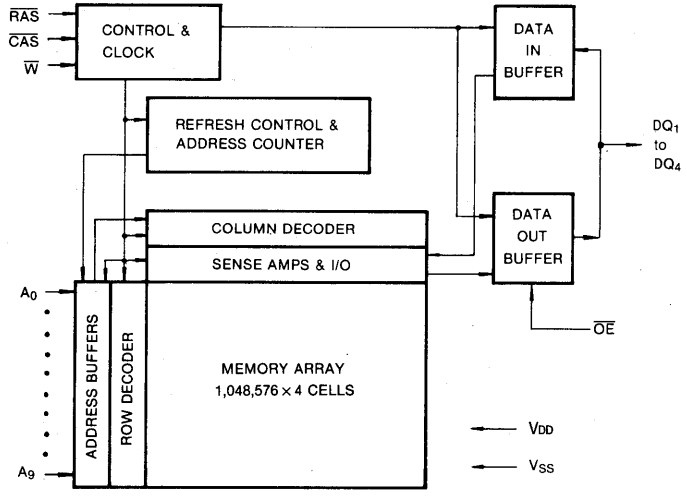
The Samsung KM44V1000C/CL/CLL is a high speed CMOS 1,048,576 bit ×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44V1000C/CL/CLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alter native to $\overline{RAS}$-only Refresh. All inputs and outputs are fully TTL compatible.

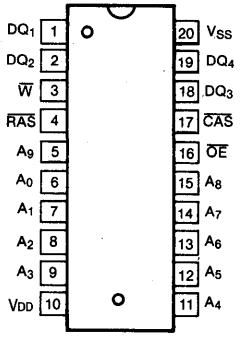
The KM44V1000C/CL/CLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

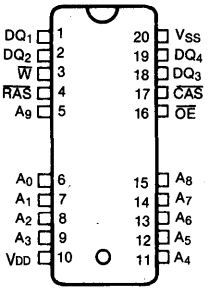


PIN CONFIGURATION (Top Views)

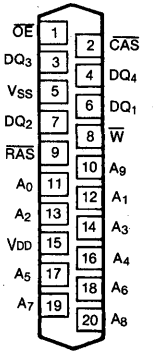
• KM44V1000CP/CLP/CLLP



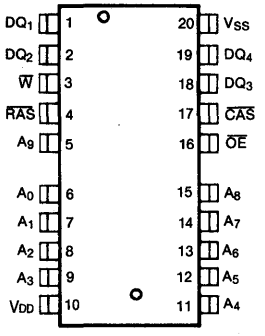
• KM44V1000CJ/CLJ/CLLJ



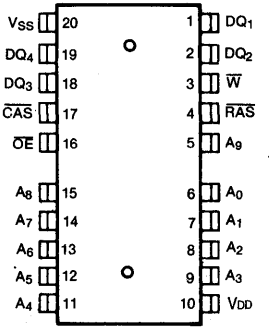
• KM44V1000CZ/CLZ/CLLZ



• KM44V1000CT/CLT/CLLT



• KM44V1000CTR/CLTR/CLLTR



Pin Names	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
$DQ_1 \sim DQ_4$	Data In/Data Out
V_{DD}	Power (+3.3V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	- 0.5~V_{DD} + 0.5	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	−0.5~4.6	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{DD} = 3.3V \pm 0.3V$)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	KM44V1000C/CL/CLL-6 KM44V1000C/CL/CLL-7 KM44V1000C/CL/CLL-8	I_{CC1}	- - -	60 55 50	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM44V1000C/CL/CLL-6 KM44V1000C/CL/CLL-7 KM44V1000C/CL/CLL-8	I_{CC3}	- - -	60 55 50	mA mA mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44V1000C/CL/CLL-6 KM44V1000C/CL/CLL-7 KM44V1000C/CL/CLL-8	I_{CC4}	- - -	45 40 35	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD} -0.2V)	KM44V1000C KM44V1000CL KM44V1000CLL	I_{CC5}	- - -	500 100 100	μA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44V1000C/CL/CLL-6 KM44V1000C/CL/CLL-7 KM44V1000C/CL/CLL-8	I_{CC6}	- - -	60 55 50	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ_1~DQ_4=Don't Care t_{RC}=125(L-ver.)μS t_{RAS}=t_{RAS} min.~300ns	KM44V1000CL	I_{CC7}	-	200	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=V_{IL} $\overline{W}$=$\overline{OE}$=A_0~A_9=V_{DD}-0.2V or 0.2V DQ_1~DQ_4=V_{DD}-0.2V or 0.2V	KM44V1000CLL	I_{CCS}	-	150	μA

DC AND OPERATING CHARACTERISTICS(Continued)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0V)	$I_{I(L)}$	-10	10	μA
Output Leakge Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

* Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximun two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be canged maximun once during a fast page Mode cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance(A_0-A_9)	C_{IN1}	—	5	pF
Input Capacitance($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$,$\overline{OE}$)	C_{IN2}	—	7	pF
output Capacitance(DQ_1-DQ_4)	C_{OUT}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, V_{DD}=3.3V±0.3V, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time(rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command set-up time	tRCS	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		15		15		ns	
Write command hold referenced to $\overline{RAS}$	tWCR	45		55		60		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		20		20		ns	
Data-inset-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	10		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	45		55		60		ns	6
Refresh period (1024 cycles)	tREF		16		16		16	ms	
Refresh period (L-version/LL-version, 1024 cycles)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to write enable delay	tCWD	40		40		50		ns	8
$\overline{RAS}$ to write enable delay	tRWD	85		100		110		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		65		70		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Fast page mode cycle time	tPC	40		45		50		ns	
$\overline{CAS}$ precharge time(Fast page mode)	tCP	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	
Fast page mode read-modify-write	tPRWC	80		95		100		ns	
$\overline{RAS}$ pulse width(Fast Page Mode)	tRASP	60	200,000	70	200,000	80	200,000	ns	
Write command set-up time (test mode in)	tWTS	10		10		10		ns	
Write command hold time (test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	15		20		20		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
$\overline{RAS}$ pulse with($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		μs	13
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	13
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refesh)	tCHS	-50		-50		-50		ns	13

TEST MODE CYCLE

(Note.12)

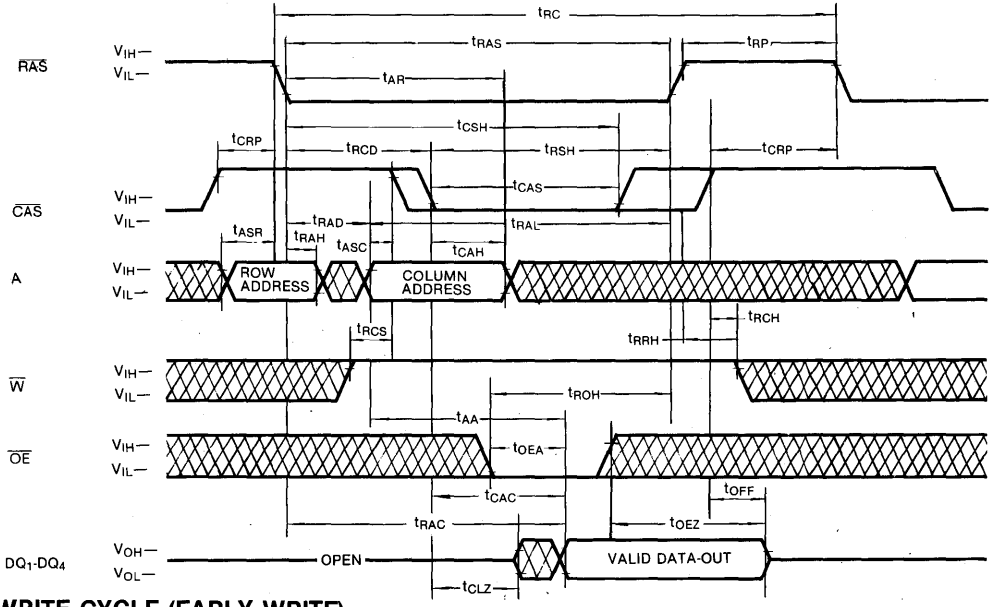
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		45		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	45		45		55		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	90		105		115		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	60		70		75		ns	8
Fast mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modefy-write	t_{PRWC}	85		100		105		ns	
$\overline{RAS}$ pulse width(Fast page mode)	t_{RASP}	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
$\overline{OE}$ access time	t_{OEA}		20		25		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	20		25		25		ns	

NOTES

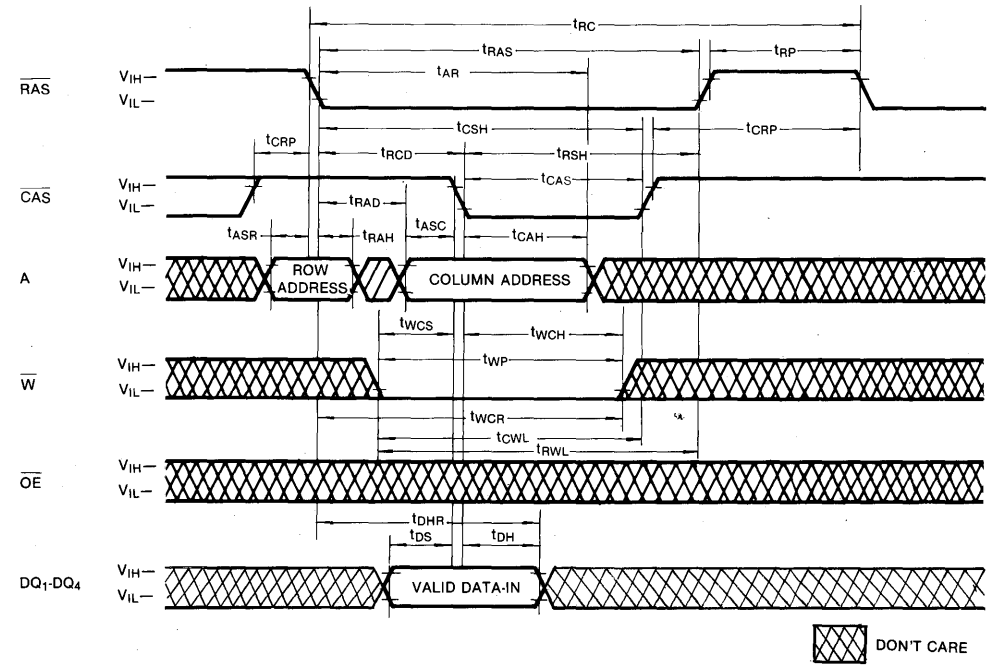
1. An initial pause of 200μs is required after power-up followed by and 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL load and 100pF, and Voh=2.0V, Vol=0.8V
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. 1024 cycle of Burst Refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification

TIMING DIAGRAMS

READ CYCLE

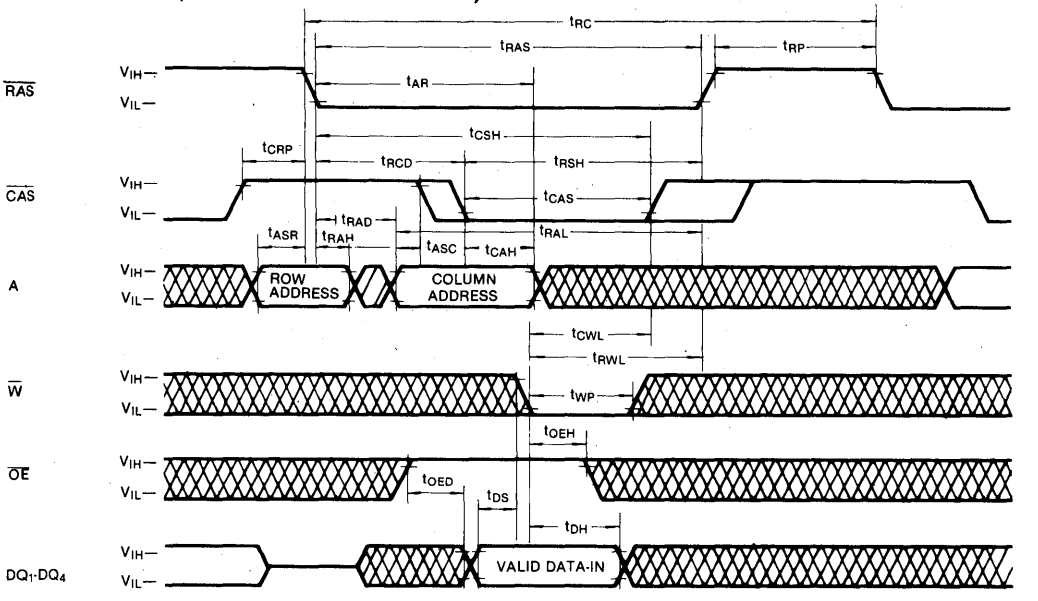


WRITE CYCLE (EARLY WRITE)

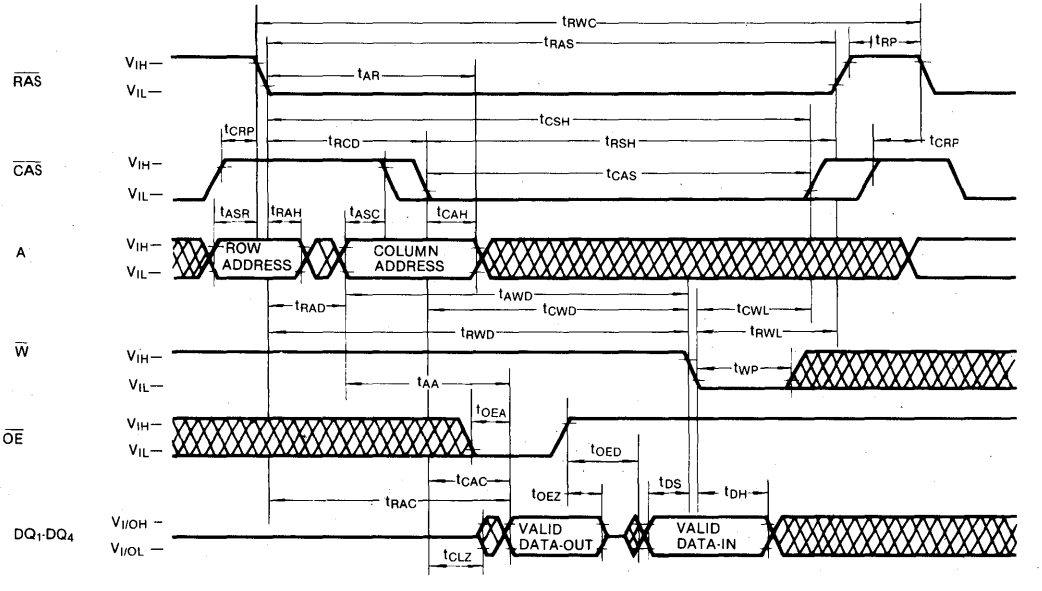


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



READ-MODIFY-WRITE CYCLE

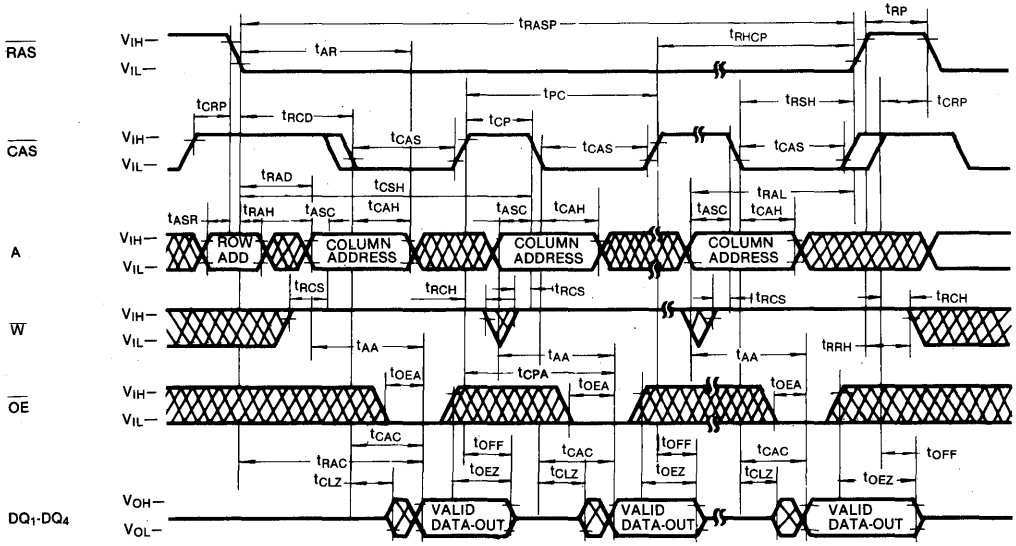


DON'T CARE

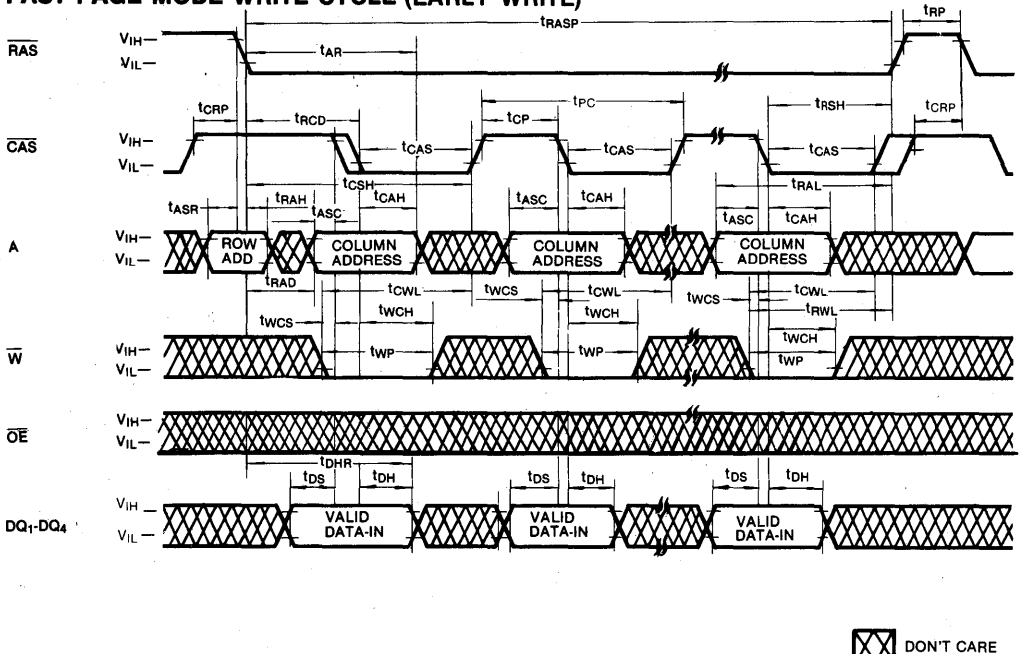
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

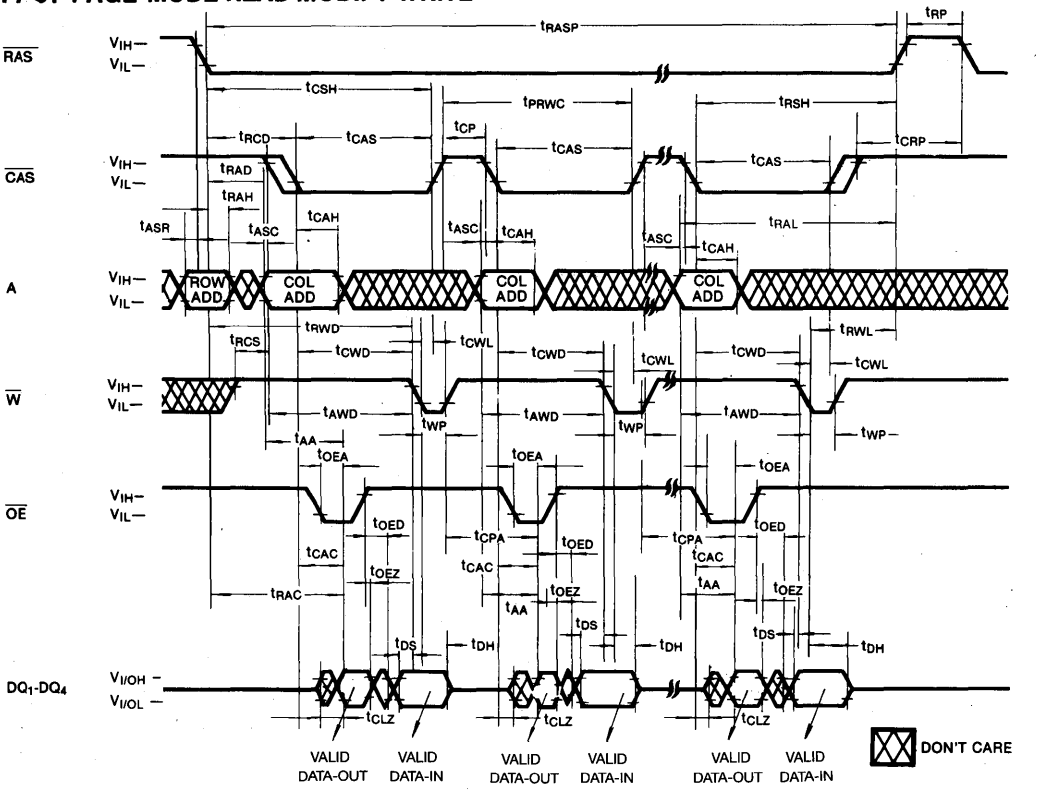


DON'T CARE

SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

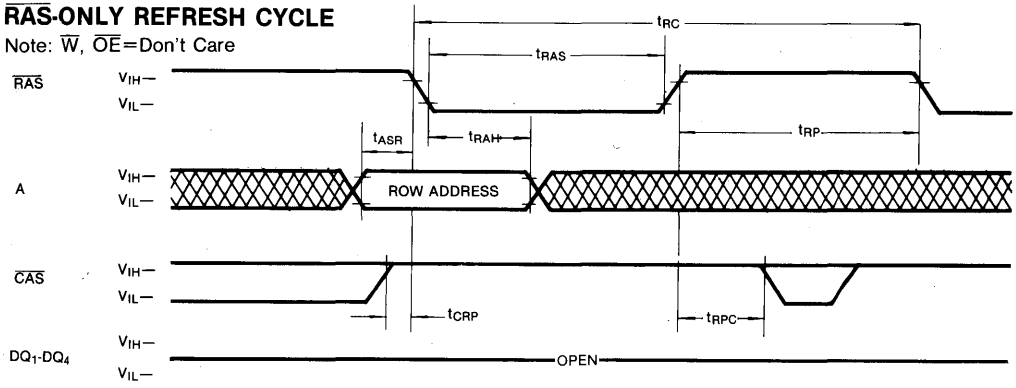
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

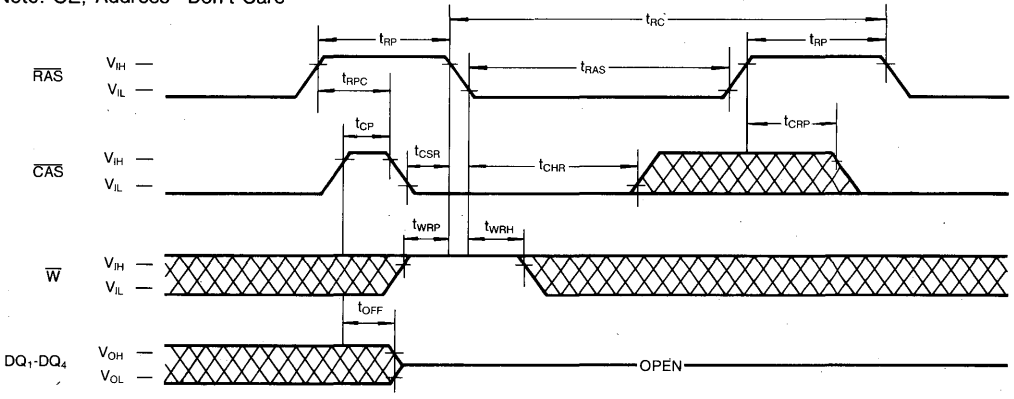
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



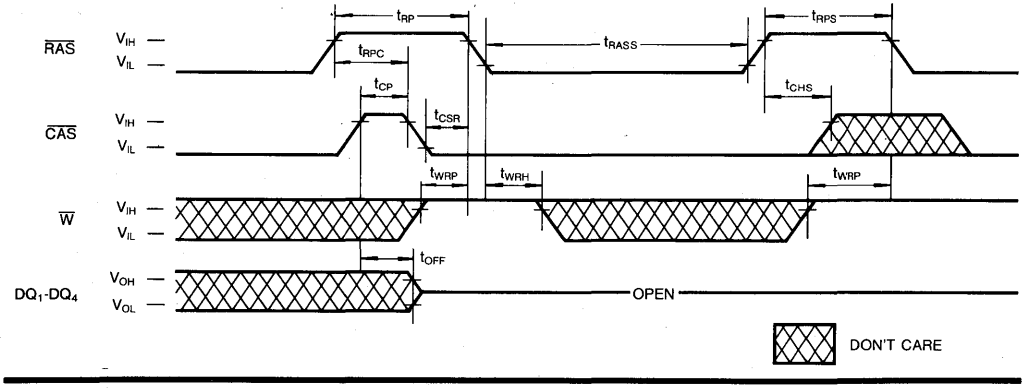
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{OE}$, Address=Don't Care



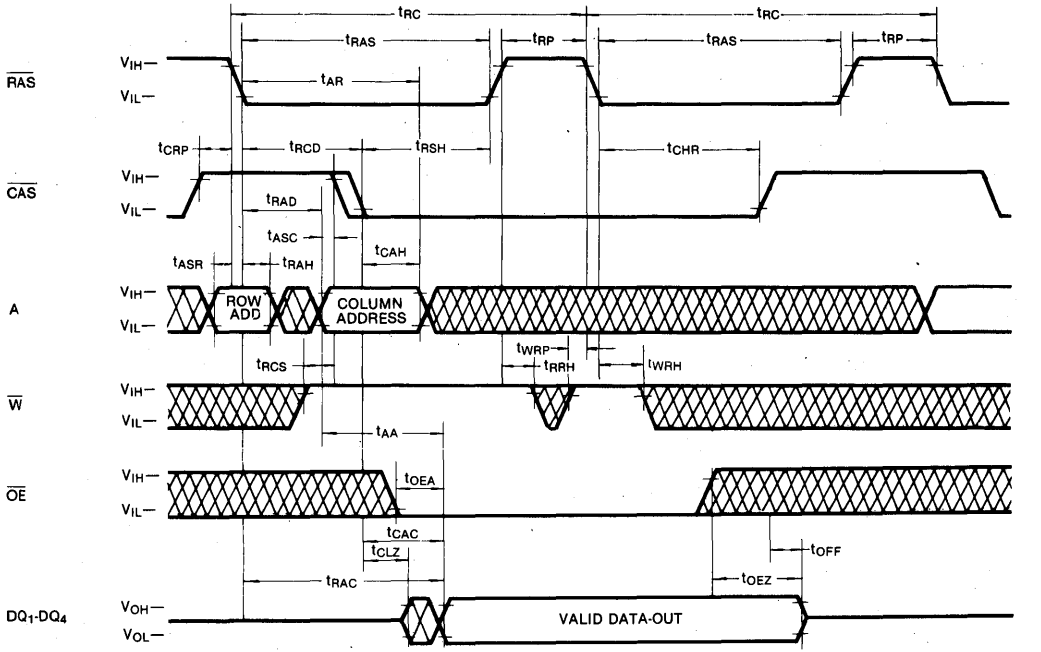
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-ver only)

Note: $\overline{OE}$, Address: Don't Care

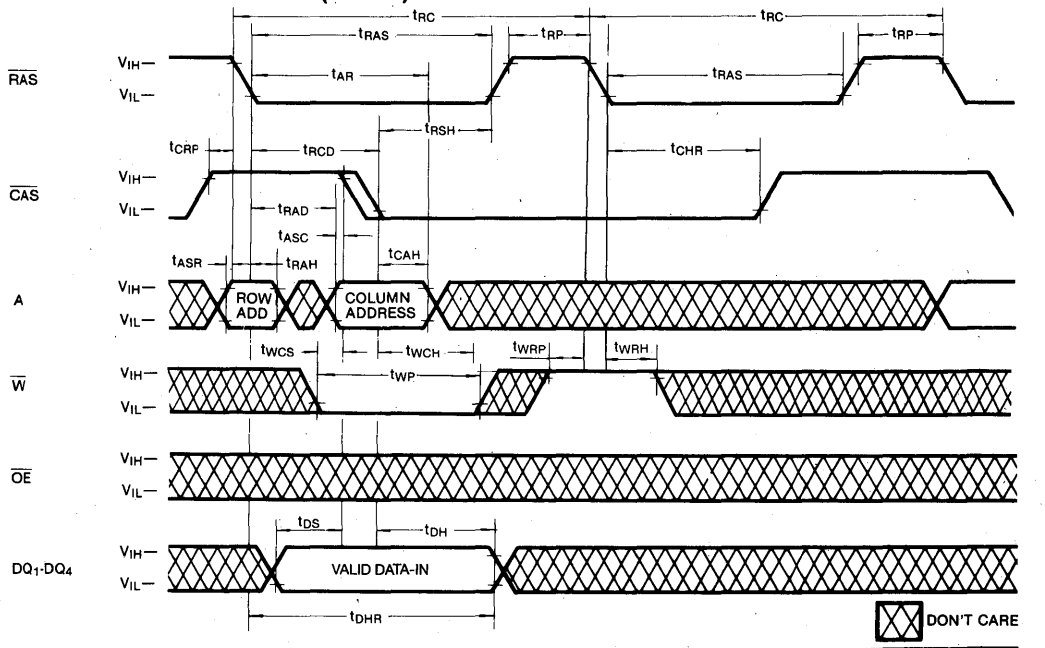


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



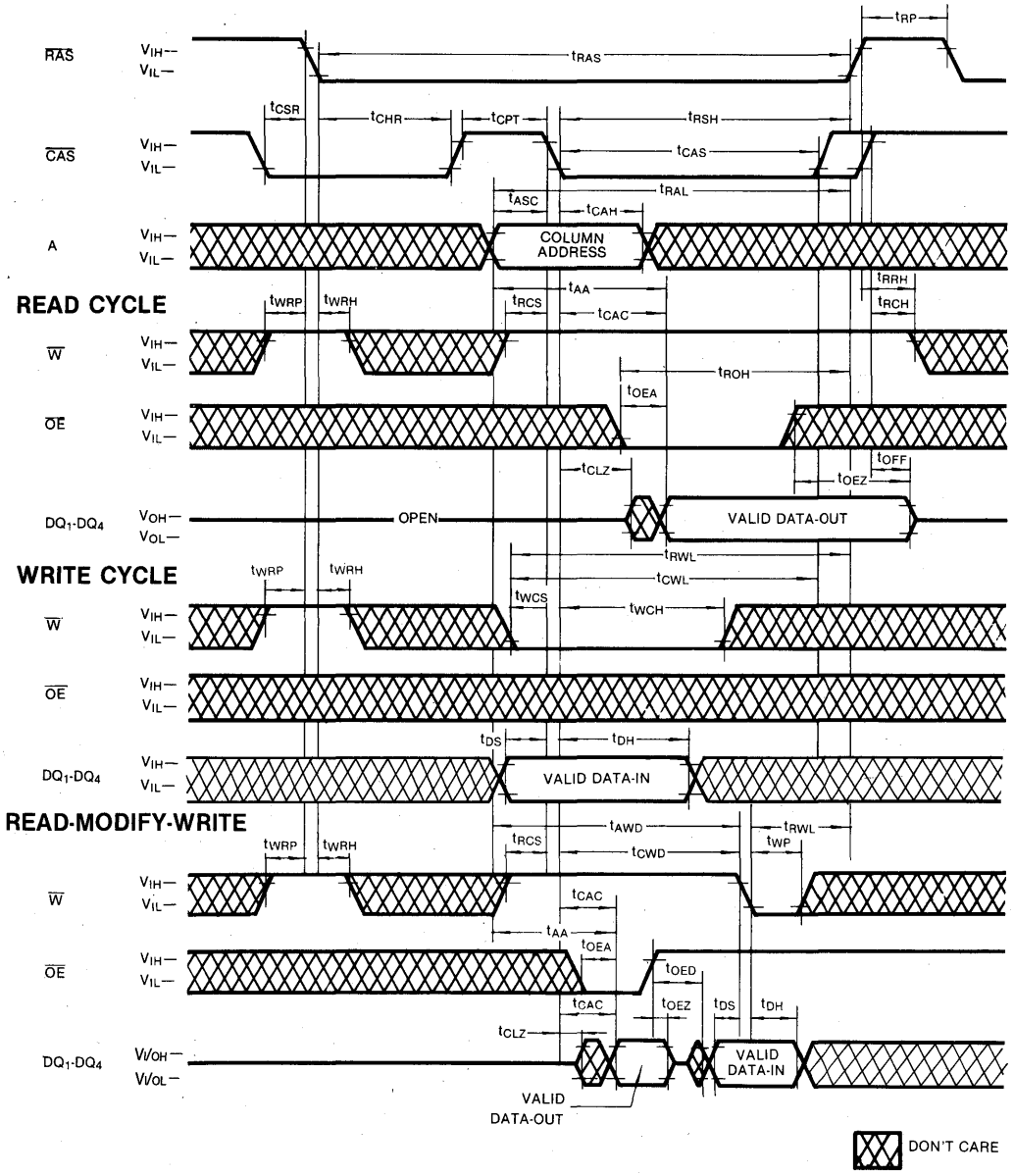
HIDDEN REFRESH CYCLE (WRITE)



SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

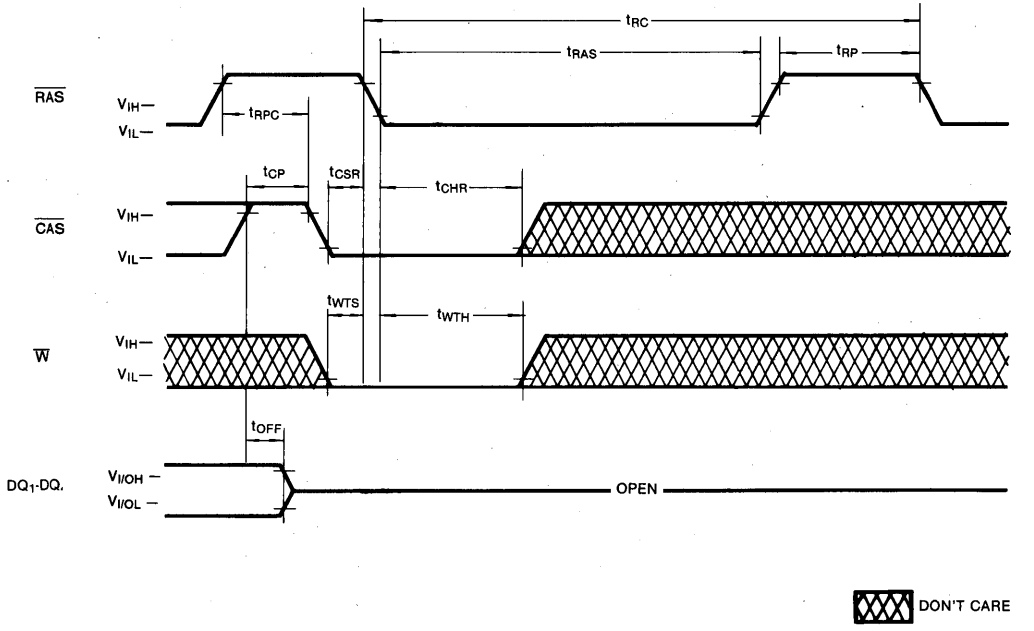
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: $\overline{OE}$, Address=Don't Care



TEST MODE DESCRIPTION

The KM44V1000C/CL/CSL is the RAM organized 1,048,576 words by 4 bit internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M x 4 DRAM can be tested as if it were a 512K x 4 DRAM. $\overline{W}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode", And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$-only-Refresh Cycle" puts it back into "Normal Mode". During the test mode operation, a WCBR cycle is used to perform refresh. The "Test Mode" function reduces test time (1/2 in cases of N test pattern.)

DEVICE OPERATION

DEVICE OPERATION

The KM44V1000C/CL/CLL contains 4,194,304 memory locations. Twenty address bits are required to address a particular 4-bit word in the memory array. Since the KM44V1000C/CL/CLL has only 10 address input pins, time multiplexed addressing is used to input 10 row (A_0-A_9) and 10 column (A_0-A_9) addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column adress strobe($\overline{CAS}$), and the valid row and column address inputs.

Operating of the KM44V1000C/CL/CLL begins by strobing in valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins (A_0-A_9) is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44V1000C/CL/CLL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respecitively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44V1000C/CL/CLL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid befor t_{RAC}(max), then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max), or if the column address bicomes valid after t_{RAD} (max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max). The KM44V1000C/CL/CLL has common data I/O pins

The this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the output, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44V1000C/CL/CLL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CAS}$. The data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early cycle the output buffers remain in the three state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur, The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain datd depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44V1000C/CL/CLL has three-state output buffer which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever $\overline{CAS}$ and $\overline{OE}$ are high(V_{IH}), the outputs is in the high impedance state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$, Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output untill $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44V1000C/CL/CLL operating cycles is listed below after the corresponding output state produced by the

DEVICE OPERATION (Continued)

cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write(t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM44V1000C/CL/CLL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 (L,LL-ver:128ms). There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44V1000C/CL/CLL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44V1000C/CL/CLL hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44V1000C/CL/CLL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time requried to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-RAS refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timingy diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address- Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address-Bits A_0 through A_9 are supplied -in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by perfoming 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, red the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS}$=V_{SS} during power-up, the KM44V1000C/CL/CLL could possibly begin an active cycle. This condition results in higher than necessary current demands from

DEVICE OPERATION (Continued)

the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current.
An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 16 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44V1000C/CL/CLL inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel temination may be used,series temination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44V1000C/CL/CLL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV.

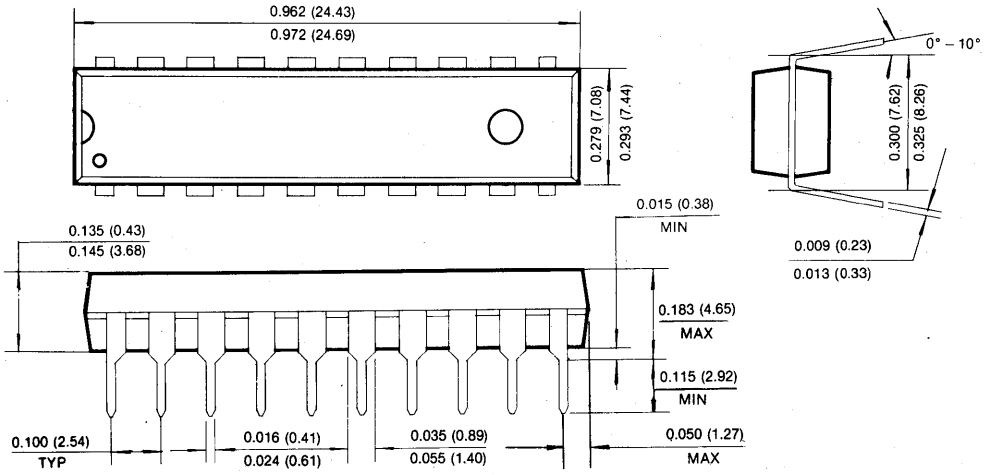
A high frequency 0.1 μF ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM44V1000C/CL/CLL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44V1000C/CL/CLL and they sypply much of the current used by the KM44V1000C/CL/CLL during cycling.

In anddition, a large tantalum capacitor with a value of 47μF to 100μFshould be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

Units: Inches (Millimeters)

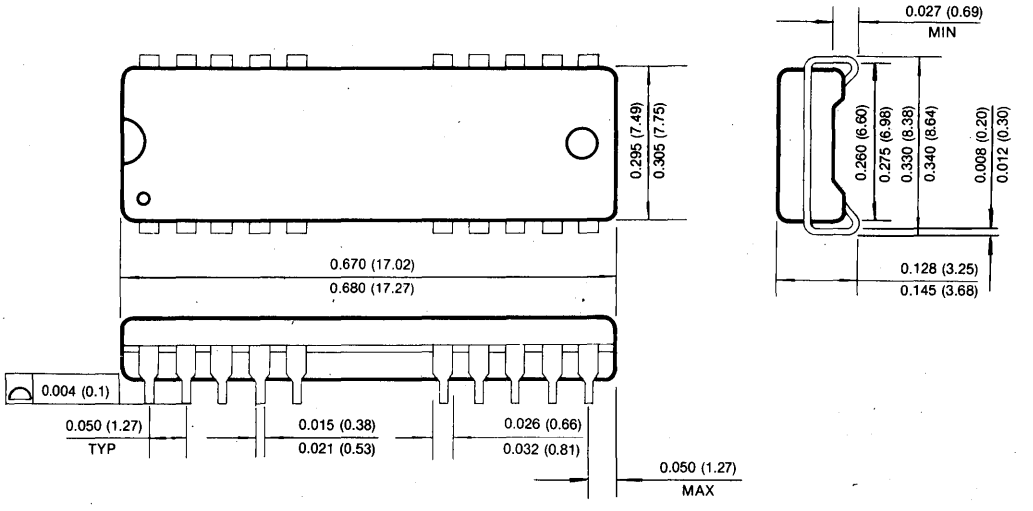
20-LEAD PLASTIC DUAL IN-LINE PACKAGE



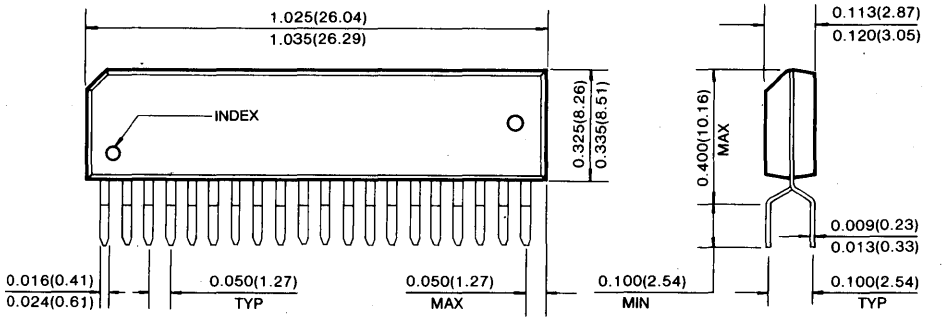
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



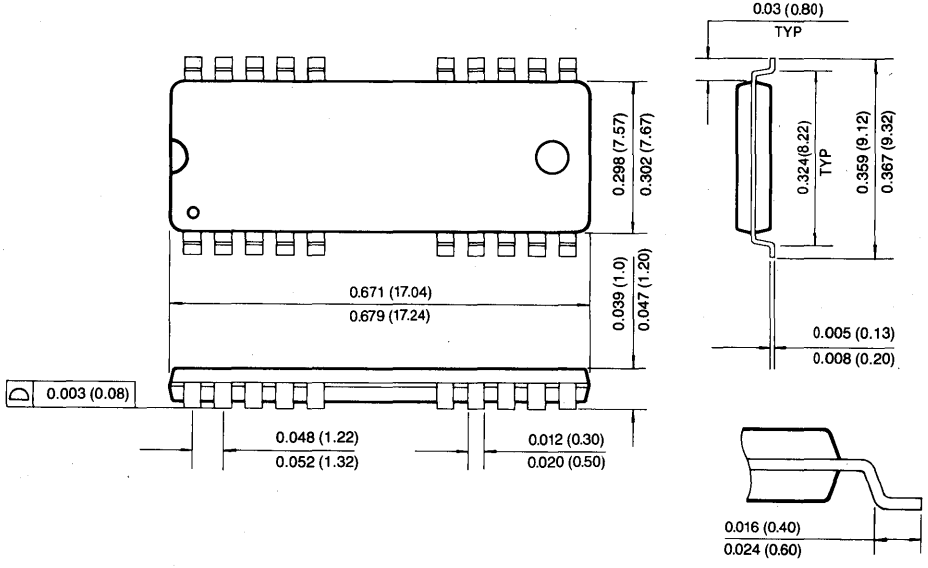
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



1M ×4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM44V1004C/CL/CLL-6	60ns	15ns	110ns	24ns
KM44V1004C/CL/CLL-7	70ns	20ns	130ns	29ns
KM44V1004C/CL/CLL-8	80ns	20ns	150ns	34ns

- **Fast Page Mode with extended data out**
- **Self refresh operation (LL-ver.)**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and hidden refresh capability**
- **Fast parallel test mode capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single +3.3V±0.3V power supply**
- **1024 cycles/16ms refresh (Normal)**
- **1024 cycles/128ms refresh (L/LL-ver)**
- **Power dissipation**
  - **Standby : 3.6mW(Normal)**
    0.36mW(L-ver)
    0.36mW(LL-ver)
  - **Active(60/70/80) : 220/200/180mW**
- **JEDEC standard pinout**
- **Available in plastic DIP, SOJ, ZIP and TSOP(II)**

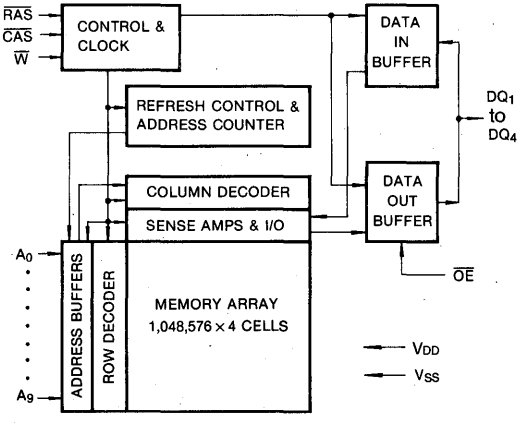
GENERAL DESCRIPTION

The Samsung KM44V1004C/CL/CLL is a CMOS high speed 1,048,576×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM44V1004C/CL/CLL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

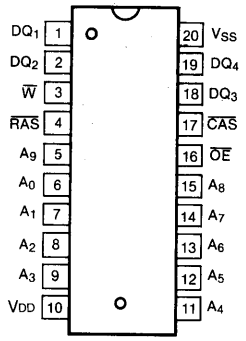
The KM44V1004C/CL/CLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

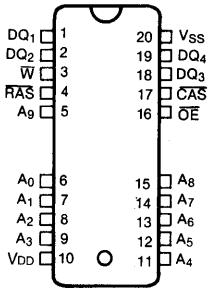


PIN CONFIGURATION (Top Views)

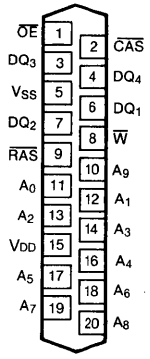
• KM44V1004CP/CLP/CLLP



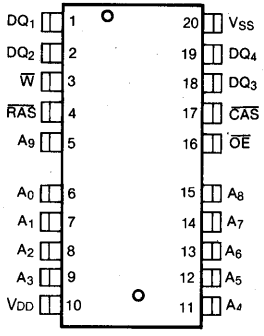
• KM44V1004CJ/CLJ/CLLJ



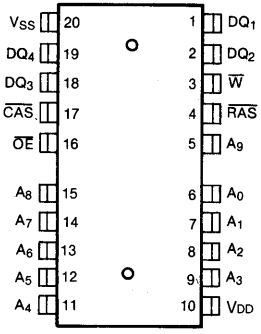
• KM44V1004CZ/CLZ/CLLZ



• KM44V1004CT/CLT/CLLT



• KM44V1004CTR/CLTR/CLLTR



Pin Names	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1~DQ_4	Data In/Data Out
V_{DD}	Power (+3.3V)
V_{SS}	Ground

3

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5~ 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5~ 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44V1004C/CL/CLL-6	I_{CC1}		60	mA
	KM44V1004C/CL/CLL-7			55	mA
	KM44V1004C/CL/CLL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44V1004C	I_{CC2}		500	μA
	KM44V1004CL			500	μA
	KM44V1004CLL			500	μA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44V1004C/CL/CLL-6	I_{CC3}		60	mA
	KM44V1004C/CL/CLL-7			55	mA
	KM44V1004C/CL/CLL-8			50	mA
EDO Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44V1004C/CL/CLL-6	I_{CC4}		60	mA
	KM44V1004C/CL/CLL-7			55	mA
	KM44V1004C/CL/CLL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM44V1004C	I_{CC5}		1	mA
	KM44V1004CL			100	μA
	KM44V1004CLL			100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44V1004C/CL/CLL-6	I_{CC6}		60	mA
	KM44V1004C/CL/CLL-7			55	mA
	KM44V1004C/CL/CLL-8			50	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ1~DQ4=Don't Care t_{RC}=125μs t_{RAS}=t_{RAS} min.~300ns	KM44V1004CL	I_{CC7}		200	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=V_{IL} $\overline{W}$=$\overline{OE}$=A_0-A_9=V_{DD}-0.2V or 0.2V DQ1~DQ4=V_{DD}-0.2V, 0.2V or Open	KM44V1004CLL	I_{CC8}		150	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz))

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, V_{DD}=3.3V±0.3V, See notes 1,2)

Test Condition : V_{IH}/V_{IL}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	15	3	20	3	20	ns	7,14,15
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10K	15	10K	20	10K	ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10		15		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal)	t_{REF}		16		16		16	ms	
Refresh period (L-ver & LL-ver)	t_{REF}		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	60		70		75		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Hyper Page cycle time	t_{HPC}	24		29		34		ns	16
Hyper Page read-modify-write cycle time	t_{HPRWC}	73		88		98		ns	
$\overline{CAS}$ precharge time (Hyper Page cycle)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	t_{RASP}	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	15	3	20	3	20	ns	7,14

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{OE}$ commend hold time	tOEH	15		20		20		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay form $\overline{RAS}$	tREZ	3	15	3	20	3	20	ns	7,14,15
Output buffer turn off delay form $\overline{W}$	tWEZ	3	15	3	20	3	20	ns	7,14
$\overline{W}$ to data delay	tWED	15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		μs	17
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	17
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	17

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		20		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		70		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Hyper Page mode cycle time	tHPC	29		34		39		ns	16
Hyper Page mode read-modify-write cycle time	tHPRWC	78		93		103		ns	
$\overline{RAS}$ pulse width (Hyper Page Mode)	tRASP	65	200,000	75	200,000	85	200,000	ns	

TEST MODE CYCLE(Continued)

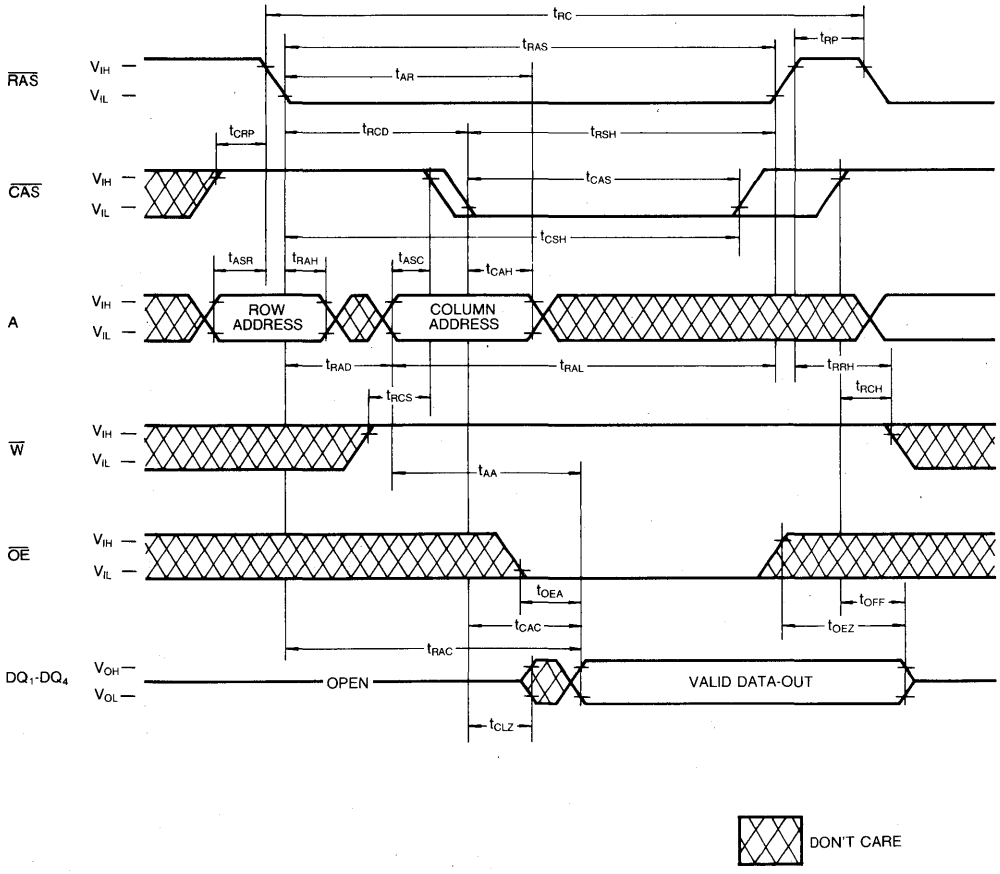
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{CAS}$ precharge	tCPA		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) are assumed to be 5ns for all inputs except tHPC and tHPRWC.
3. Measured with a load equivalent to 1TTL load and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD ≥ tRCD (max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS ≥ tWCS(min) the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD ≥ tCWD(min), tRWD ≥ tRWD(min) and tAWD ≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
16. tASC ≧ tCP min, Assumn tT=2.0ns
17. 1024 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.(LL-ver.)

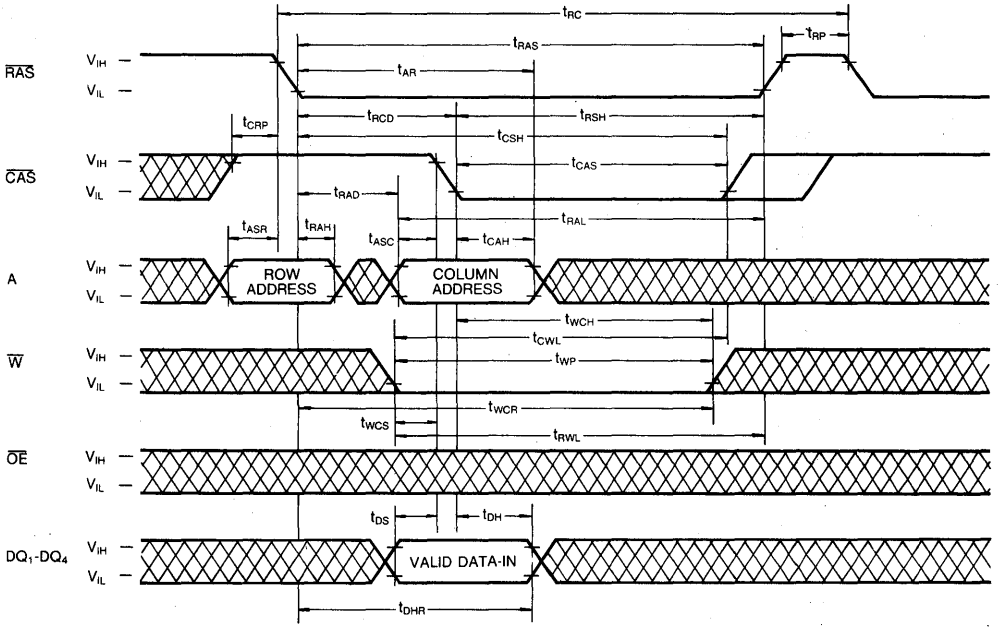
TIMING DIAGRAMS

READ CYCLE

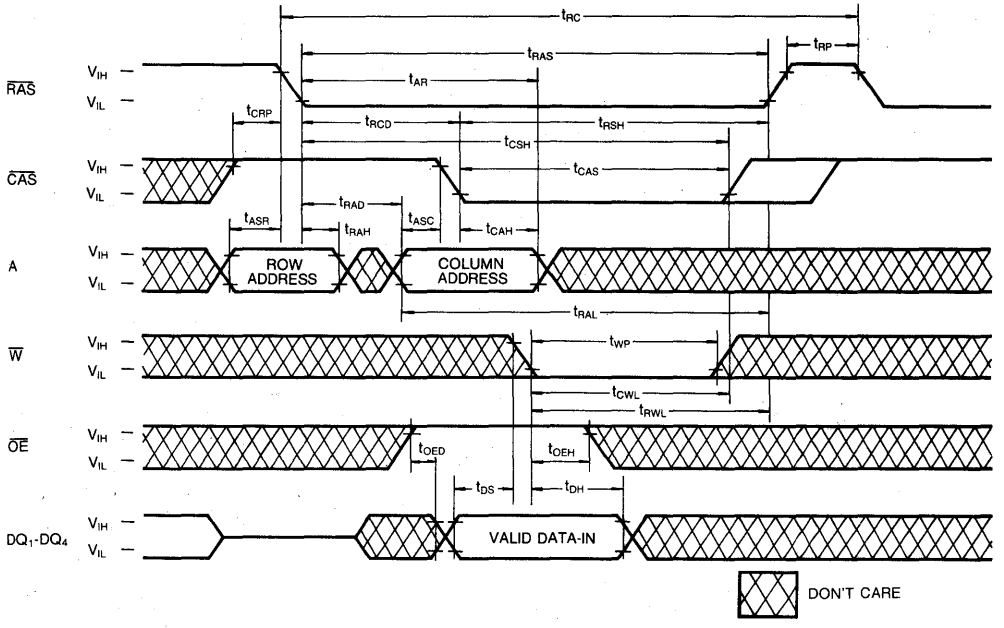


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



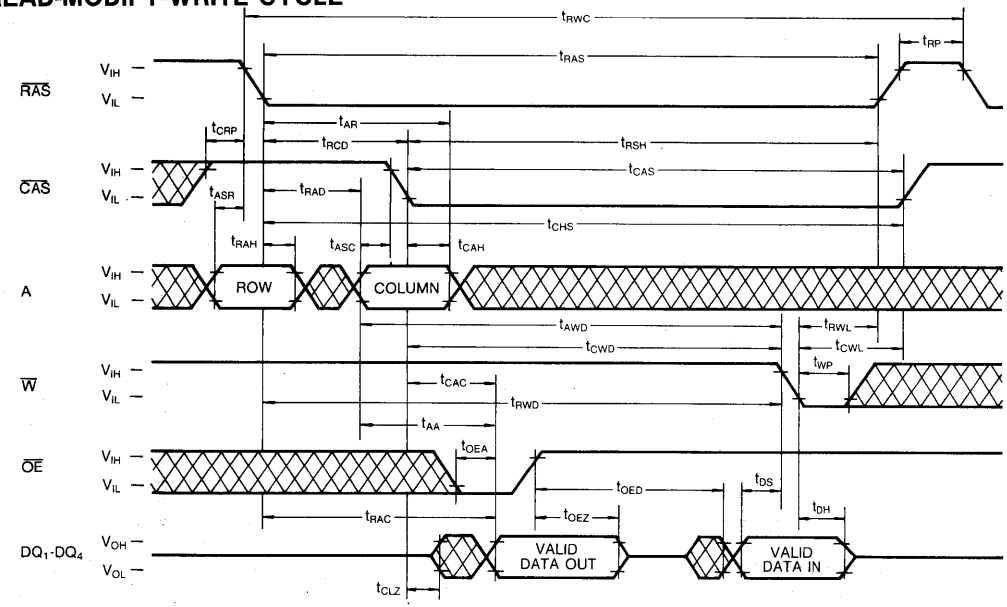
WRITE CYCLE (OE CONTROLLED WRITE)



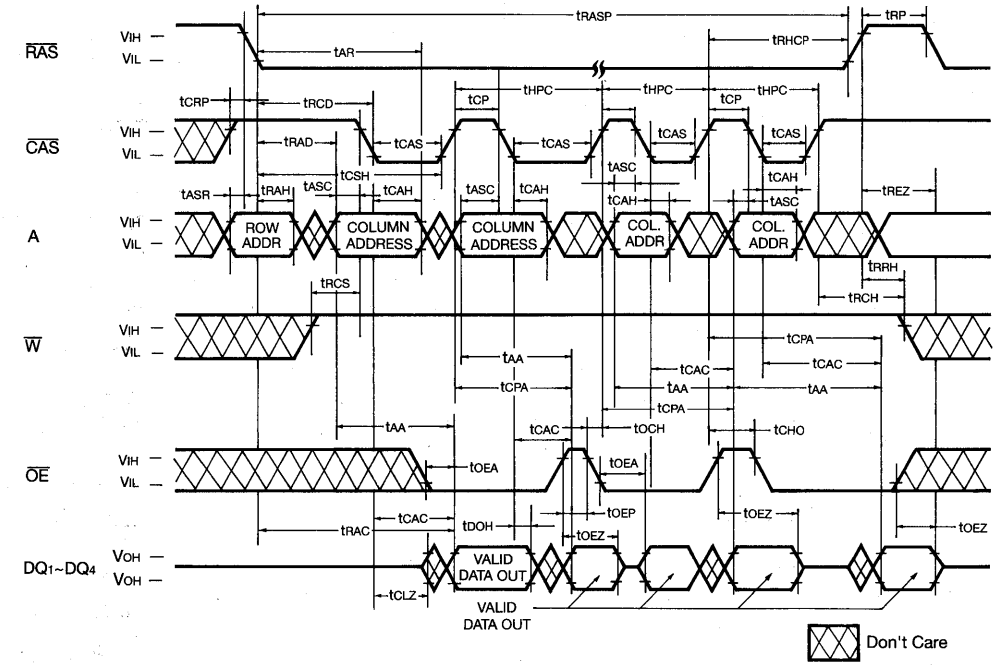
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



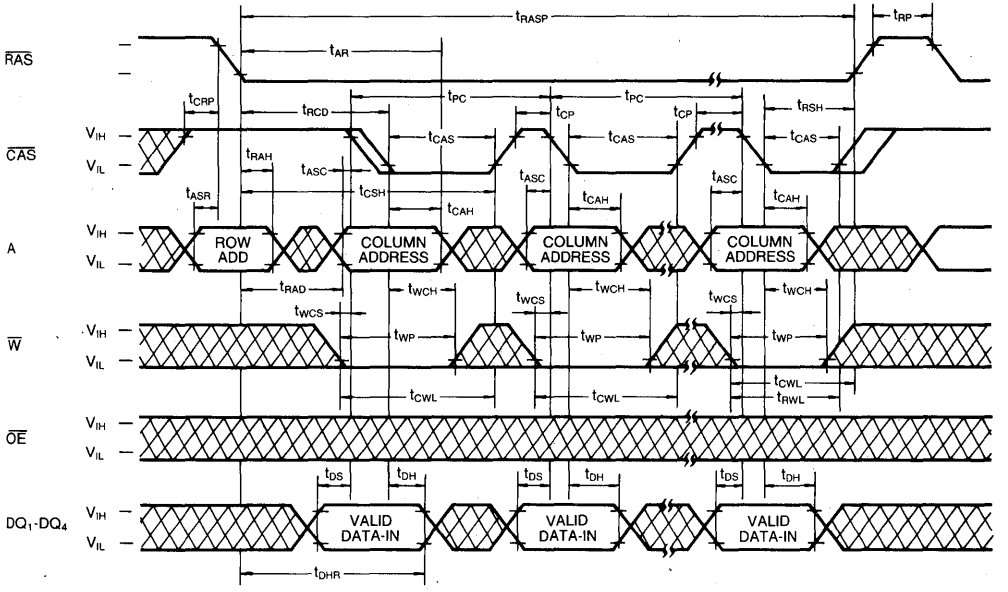
HYPER PAGE READ CYCLE



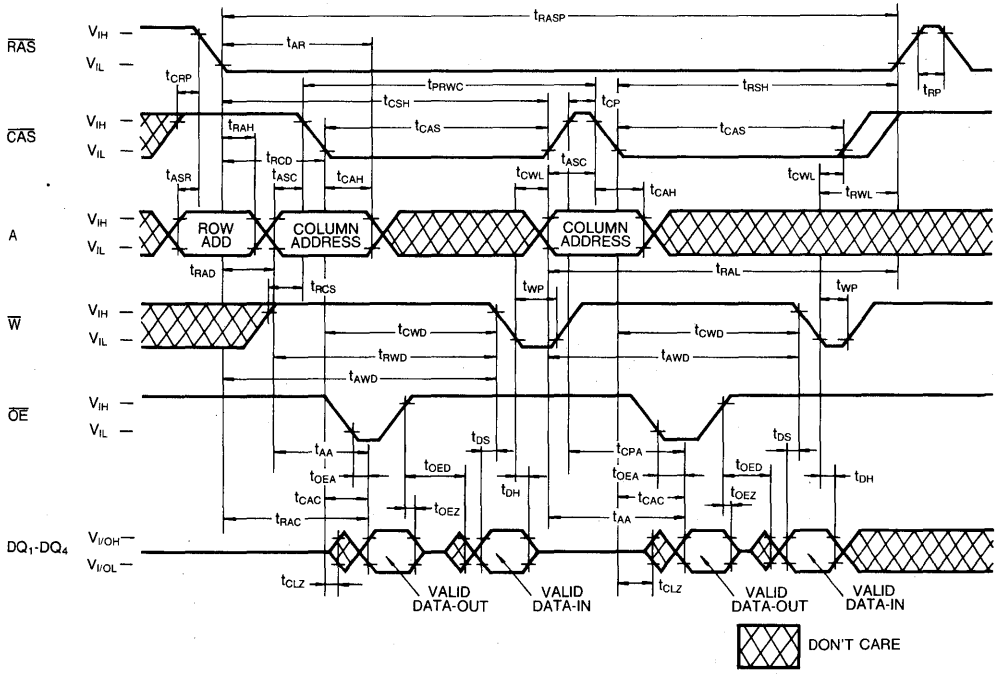
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WITH EDO WRITE CYCLE (EARLY WRITE)

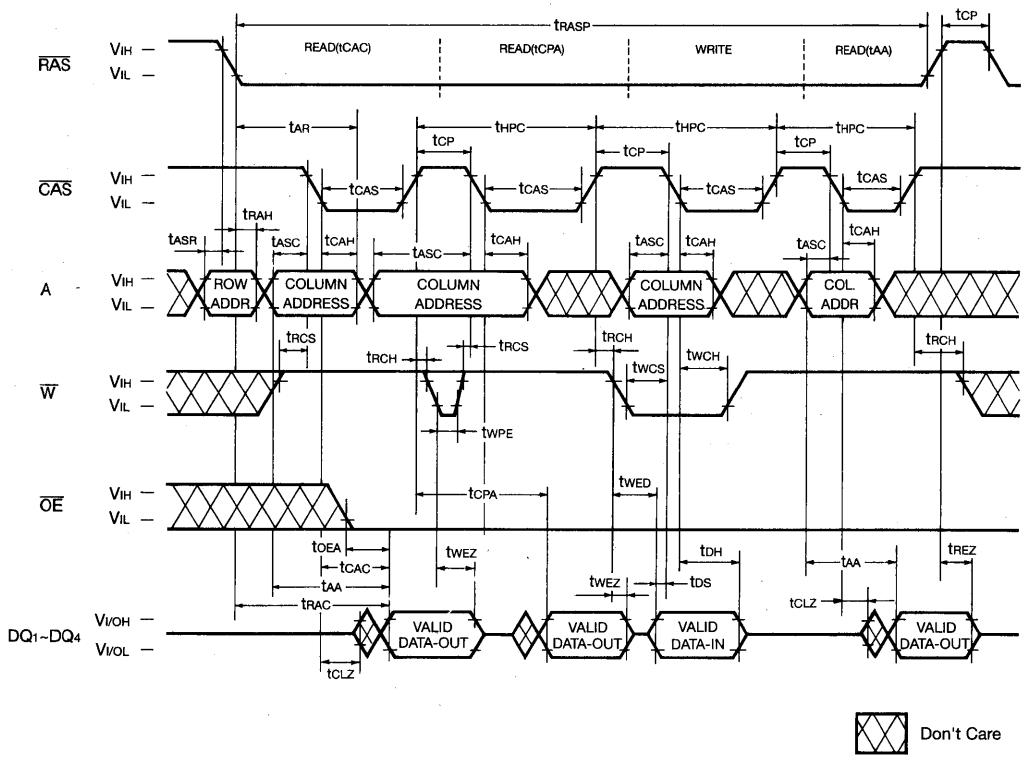


FAST PAGE MODE WITH EDO READ-MODIFY-WRITE CYCLE



SAMSUNG ELECTRONICS

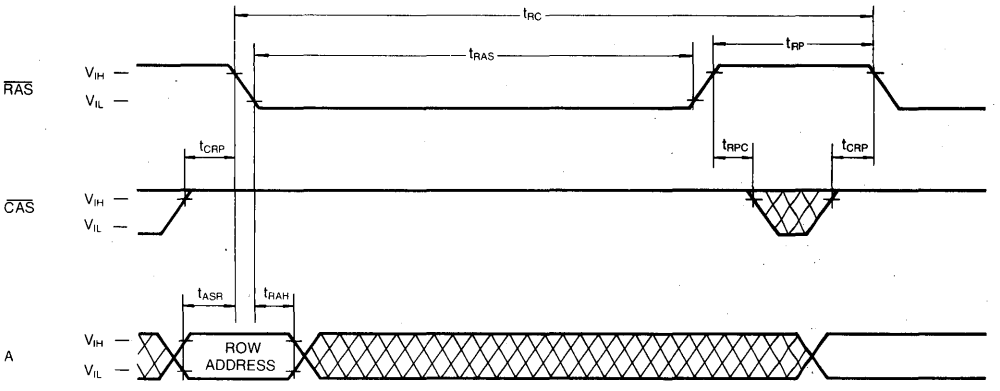
PAGE WITH EDO READ AND WRITE MIXED CYCLE



TIMING DIAGRAMS (Continued)

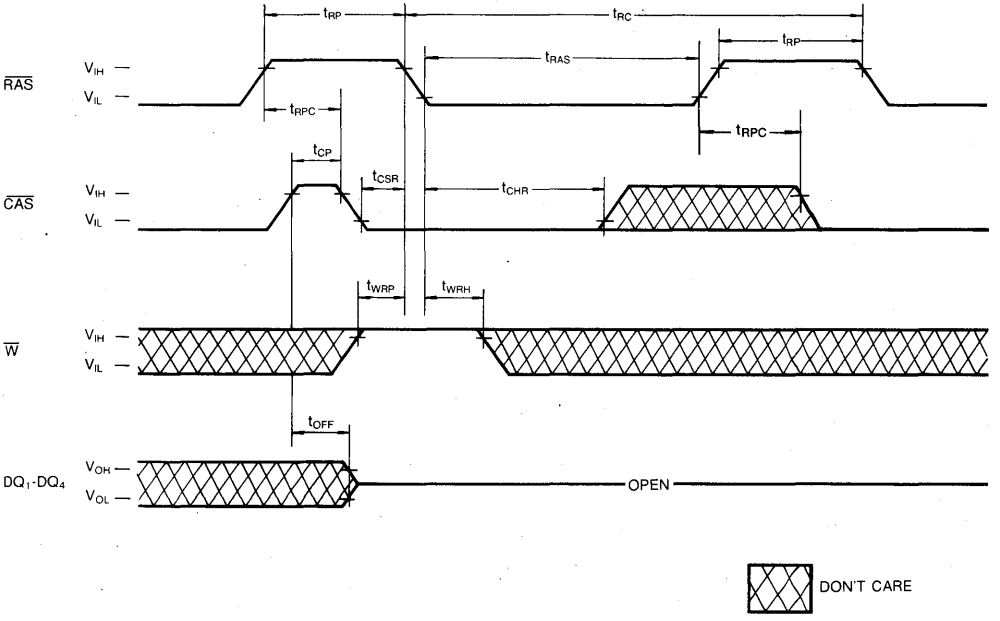
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



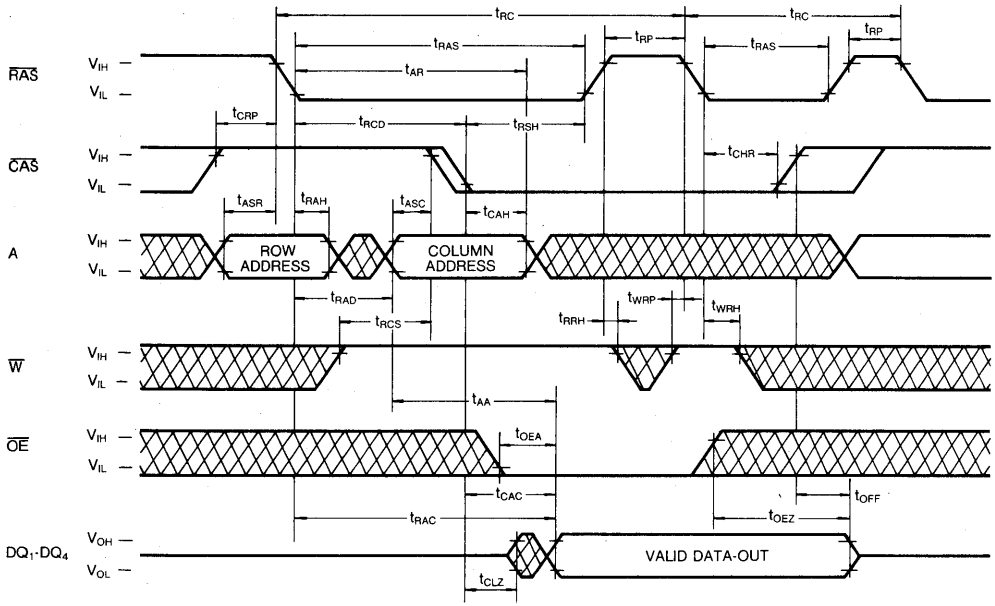
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{OE}$, Address=Don't Care

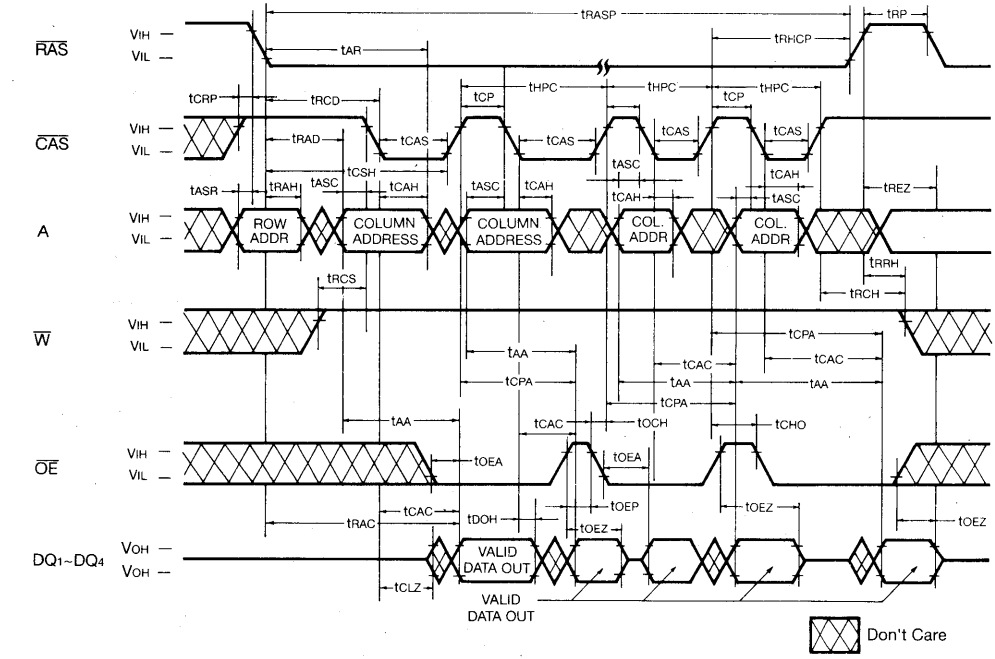


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



HYPER PAGE READ CYCLE



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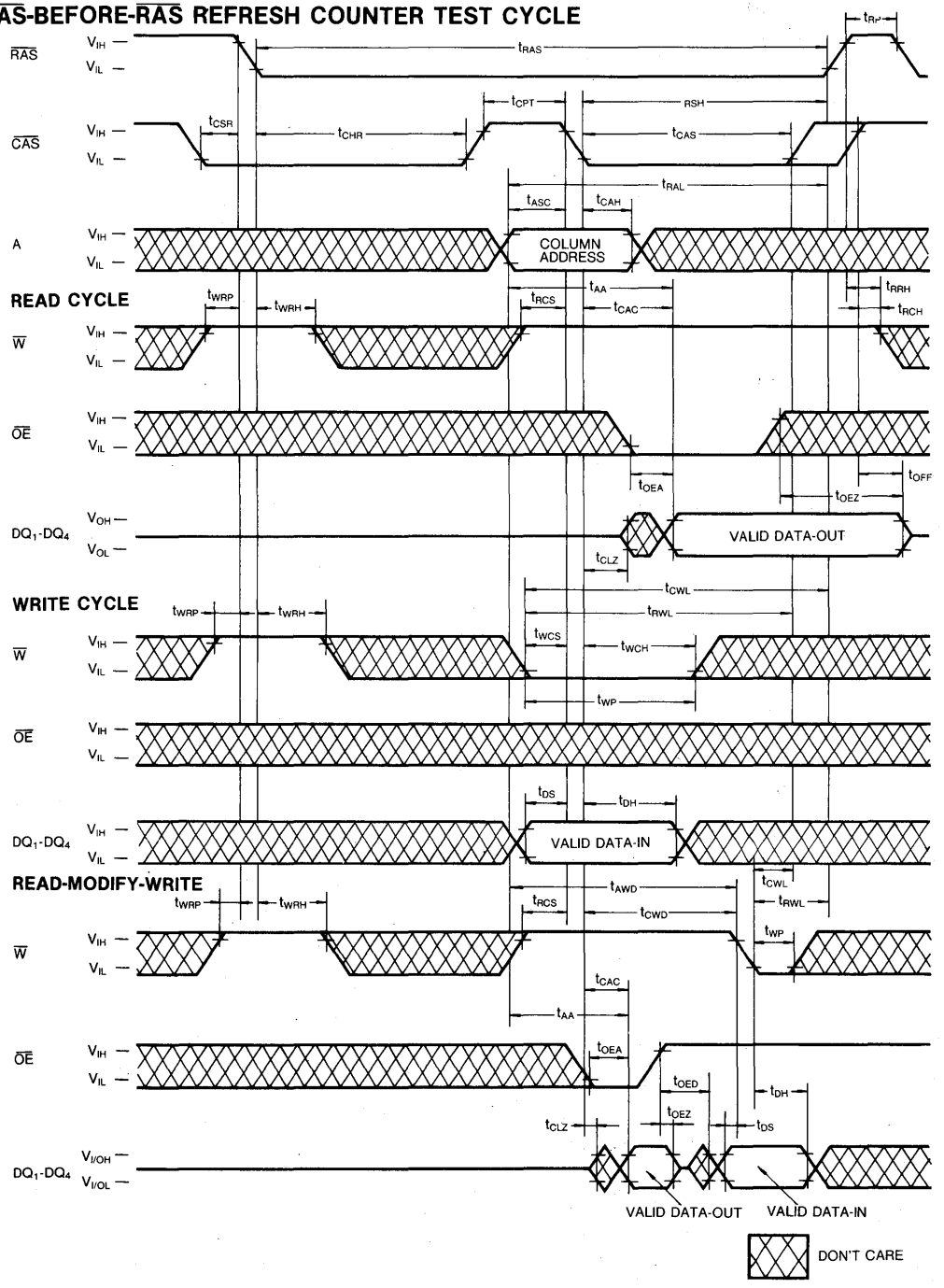
TIMING DIAGRAMS (Continued)

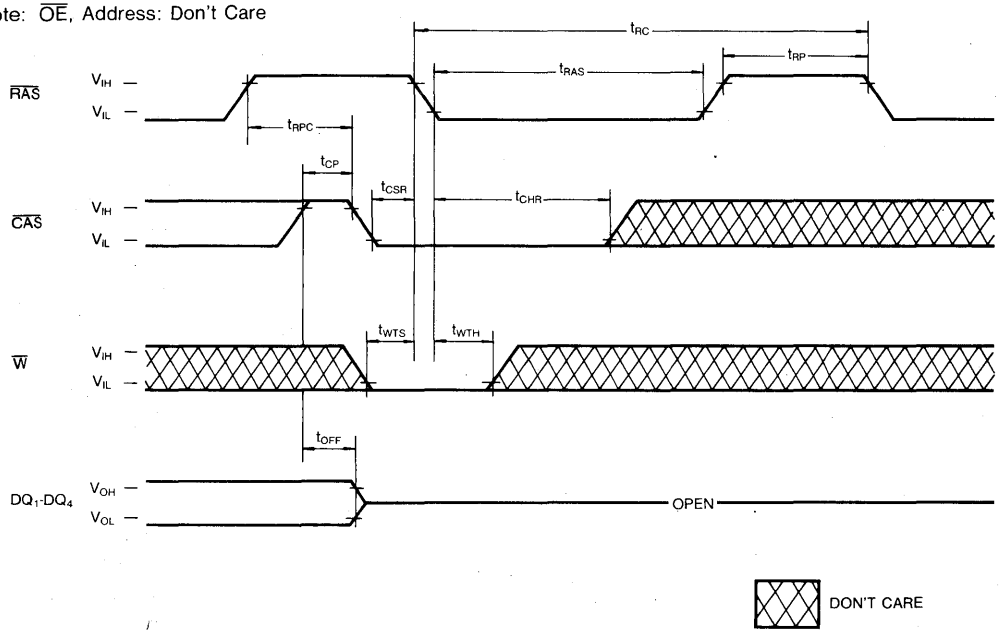
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



TEST MODE DESCRIPTION

The KM44V1004C/CL/CLL is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

The KM44V1004C/CL/CLL contains 4,194,304 memory locations. Twenty address bit are required to address a particular 4-bit word in the memory array. Since the KM44V1004C/CL/CLL has only 10 address input pins, time multiplexed addressing is used to input 10 row (A_0~A_9) and 10 column(A_0~A_9) address. The multiplexing is controlled by the timing relationship between the row address strobe($\overline{RAS}$), the column address strobe($\overline{CAS}$), and the valid row and column address inputs.

Operating of the KM44V1004C/CL/CLL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins(A_0~A_9) is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44V1004C/CL/CLL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time(t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44V1004C/CL/CLL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAC}(max), then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC} (min), it is necessary to meet both t_{RCD}(max) and t_{RAD} (max). The KM44V1004C/CL/CLL has common data I/O pins. The this reason an output enable control input($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44V1004C/CL/CLL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CAS}$. The data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the three state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44V1004C/CL/CLL has a three-state output buffer which is controlled by $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. When $\overline{RAS}$ and $\overline{CAS}$ go high(V_{IH}) or $\overline{OE}$ goes high (V_{IH}), the outputs are in the high impedance state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data at the output cannot be eliminated by $\overline{CAS}$ rising only and it remains until both $\overline{RAS}$ and $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs(as in hidden refresh). Each of the KM44V1004C/CL/CLL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, EDO Mode Read, EDO Mode Read-Modify-Write.

DEVICE OPERATION (Continued)

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page with EDO Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM44V1004C/CL/CLL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16/128/256ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C1004C/CL/ CLL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44V1004C/CL/CLL hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Self Refresh: The self refresh is $\overline{CAS}$-before-$\overline{RAS}$ refresh to be used for long periods of standby, such as al battery back-up. In nomal $\overline{CAS}$-befoerd-$\overline{RAS}$ condition, when $\overline{RAS}$ is held low above 100μs an internal timer activates an refresh operation of consecutive row addersses in DRAM. The self refresh mode is exited when either $\overline{RAS}$ of $\overline{CAS}$ goes high(V_{IH}).

Other Refresh Methods: It is also possible to refresh the KM44V1004C/CL/CLL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode with Extended Data Out

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address — Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address — Bits A_0 through A_9 are supplied by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested CAS-before-RAS Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps;

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycle, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2,3 and 4.

Power-up

If $\overline{RAS}$=Vss during power-up, the KM44C1004C/CL/CLL could possibly begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is

DEVICE OPERATION (Continued)

recommended that $\overline{RAS}$ and $\overline{CAS}$ track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current. An initial pause of 200 μsec is required after power-up followed by any 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 16(L/LL-ver:128, SL-ver:256) msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44V1004C/CL/CLL inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44V1004C/CL/CLL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. the recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity(soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV.

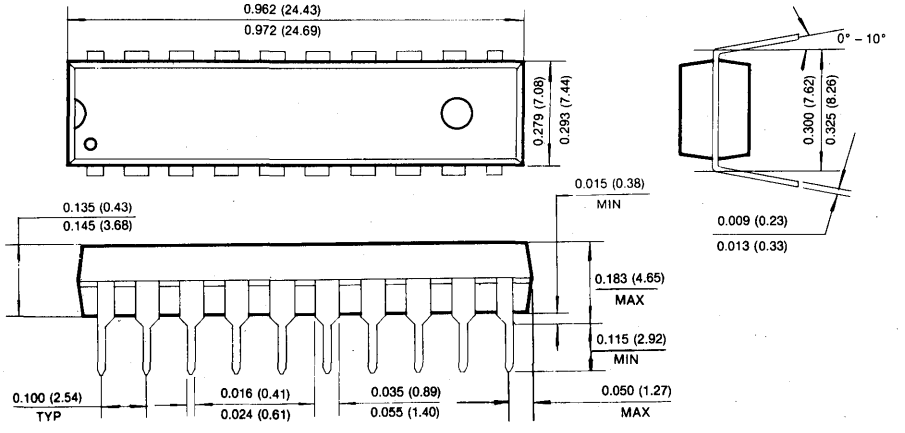
A high frequency 0.1 μF ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM44V1004C/CL/CLL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44V1004C/CL/CLL and they supply much of the current used by the KM44V1004C/CL/CLL during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

Units: Inches (Millimeters)

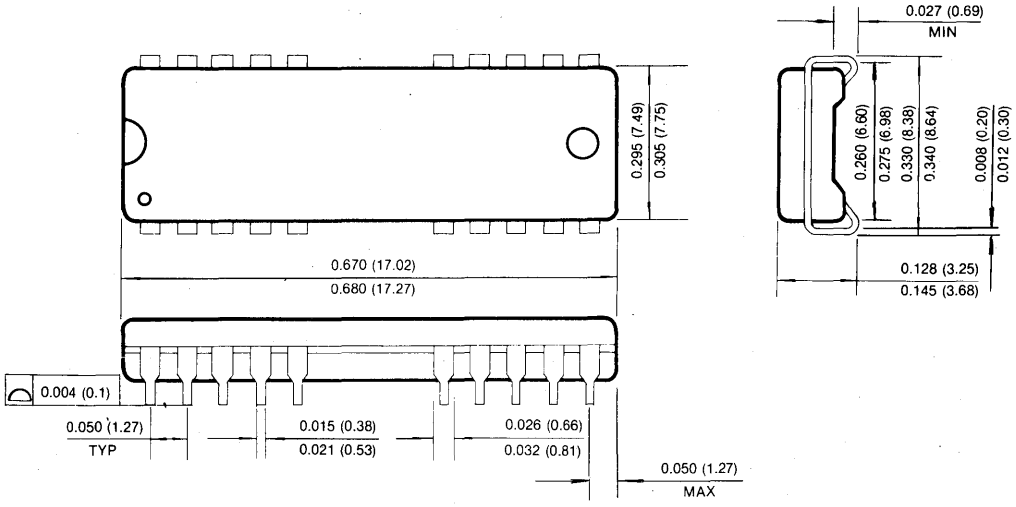
20-LEAD PLASTIC DUAL IN-LINE PACKAGE



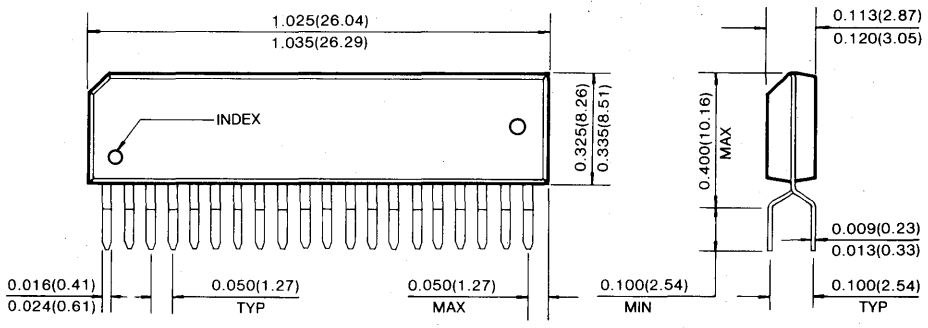
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



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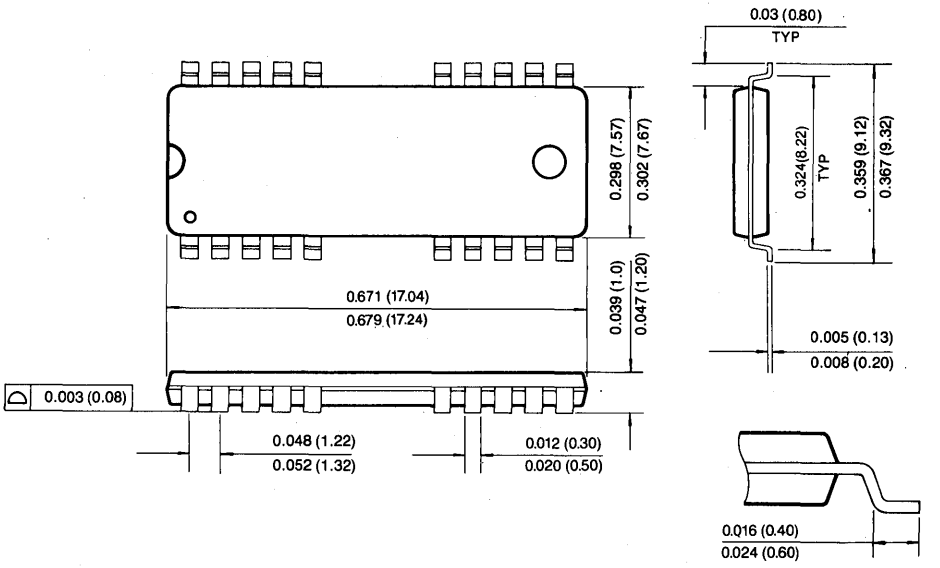
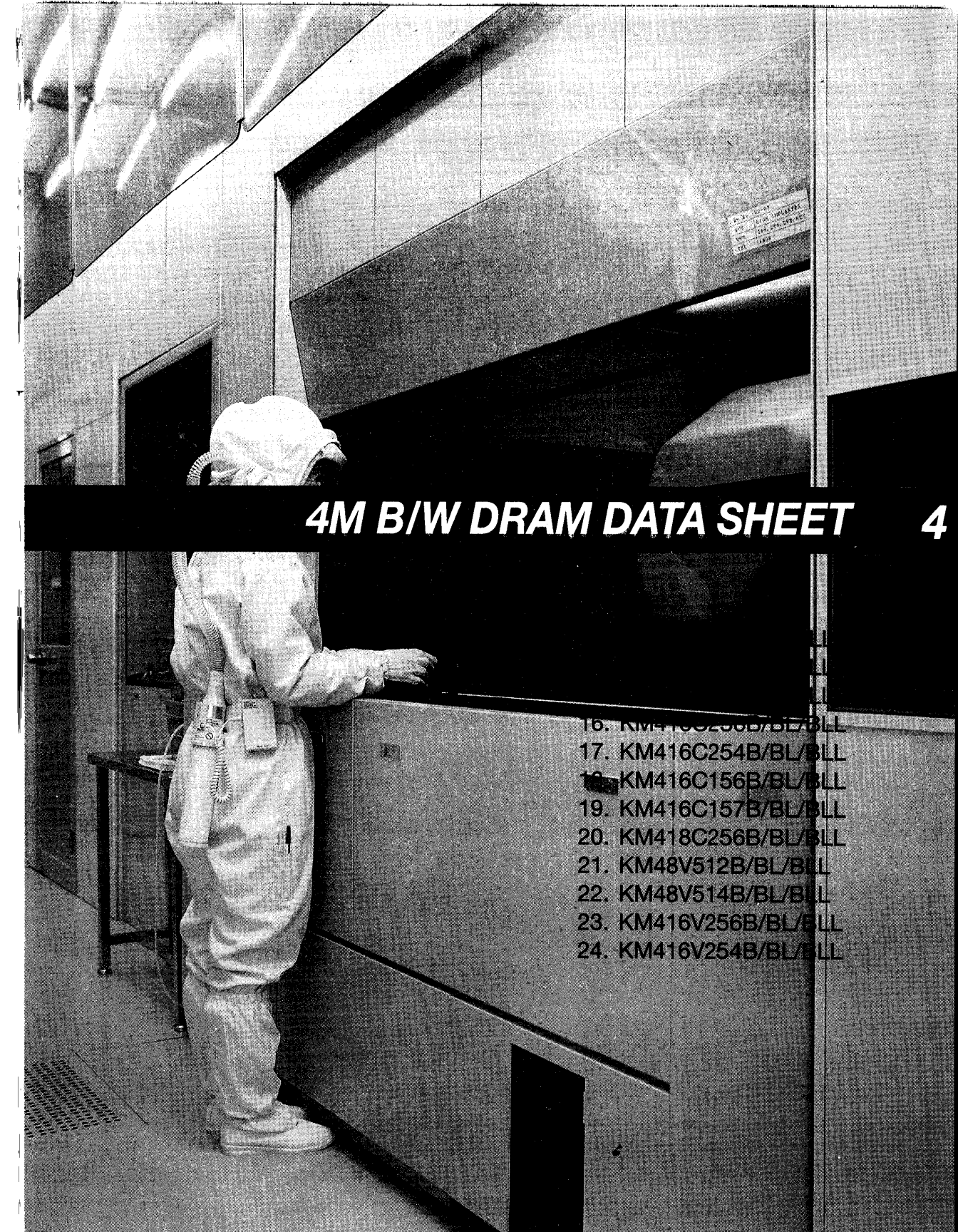
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)





4M B/W DRAM DATA SHEET 4

512K ×8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM48C512B/BL/BLL-5	50ns	15ns	90ns
KM48C512B/BL/BLL-6	60ns	15ns	110ns
KM48C512B/BL/BLL-7	70ns	20ns	130ns
KM48C512B/BL/BLL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Self Refresh operation (LL-version)**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Dual +5.0V±10% power supply**
- **Refresh Cycle**
  - **-1024 cycle/16ms (Normal)**
  - **-1024 cycle/128ms (L-version)**
  - **-1024 cycle/128ms (LL-version)**
- **Power Dissipation**
  - **-Standby: 5.5mW (Normal)**
  - **1.1mW (L-version)**
  - **0.83mW (LL-version)**
  - **-Active (50/60/70/80): 470/385/360/330mW**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP II**

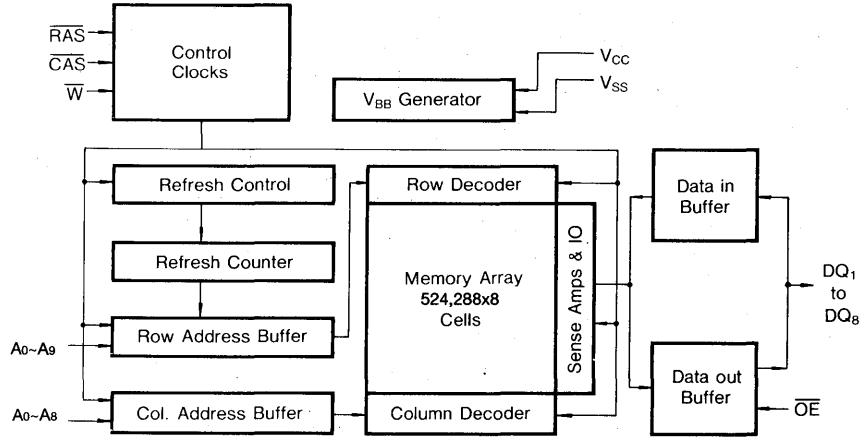
GENERAL DESCRIPTION

The Samsung KM48C512B/BL/BLL is a CMOS high speed 524,288 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM48C512B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

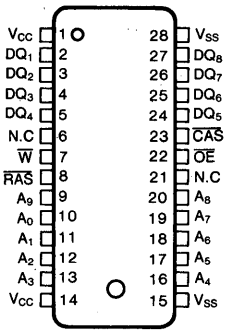
The KM48C512B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



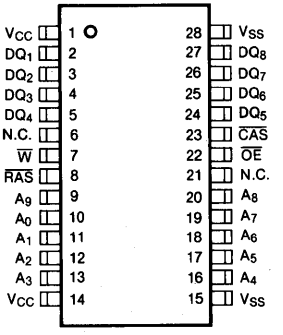
PIN CONFIGURATION (Top Views)

• KM48C512BJ/BLJ/BLLJ



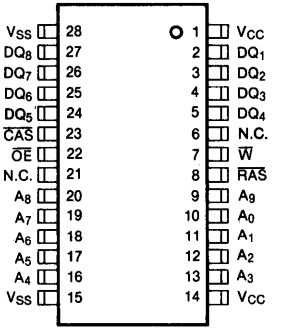
(SOJ)

• KM48C512BT/BLT/BLLT



(TSOP(II)-Forward Type)

• KM48C512BTR/BLTR/BLLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A_0-A_9	Address Input
DQ_{1-8}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe

Pin Name	Pin Function
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

4

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	KM48C512B/BL/BLL-5	I_{CC1}	-	85	mA
	KM48C512B/BL/BLL-6			70	mA
	KM48C512B/BL/BLL-7			65	mA
	KM48C512B/BL/BLL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM48C512B/BL/BLL-5	I_{CC3}	-	85	mA
	KM48C512B/BL/BLL-6			70	mA
	KM48C512B/BL/BLL-7			65	mA
	KM48C512B/BL/BLL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM48C512B/BL/BLL-5	I_{CC4}	-	65	mA
	KM48C512B/BL/BLL-6			55	mA
	KM48C512B/BL/BLL-7			50	mA
	KM48C512B/BL/BLL-8			45	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM48C512B	I_{CC5}	-	1	mA
	KM48C512BL			200	μA
	KM48C512BLL			150	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48C512B/BL/BLL-5	I_{CC6}	-	85	mA
	KM48C512B/BL/BLL-6			70	mA
	KM48C512B/BL/BLL-7			65	mA
	KM48C512B/BL/BLL-8			60	mA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Max	Units
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=0.2V D_{IN}=Don't Care, T_{RC}=125μS T_{RAS}=T_{RAS} min.~300ns	KM48C512BL	I_{CC7}	-	300	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_9=V_{CC}-0.2V or 0.2V DQ_1-DQ_8=V_{CC}-0.2V, 0.2V or Open	KM48C512BLL	I_{CCS}	-	200	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	135		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	15	10,000	20	10,000	20	10.000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	35	20	45	20	50	20	60	ns	4

(*) 50ns Product:V_{CC}=5V ± 5%, Cout=50pF

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		0		ns	8
Write command hold time	tWCH	10		10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		50		55		ns	6
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		20		ns	
Data-in set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		10		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (L-version)	tREF		128		128		128		128	ms	
Refresh period (LL-version)	tREF		128		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	75		85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	50		55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	55		60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast page mode cycle time	tPC	35		40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	80		80		95		100		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	

(*) 50ns Product:V_{CC}=5V ± 5%, Cout=50pF

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ precharge time (Fast Page Mode)	tCP	10		10		10		10		ns	
access time from $\overline{OE}$	tOEA		15		15		20		20	ns	
$\overline{OE}$ to data-in delay time	tOED	15		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	15		15		20		20		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

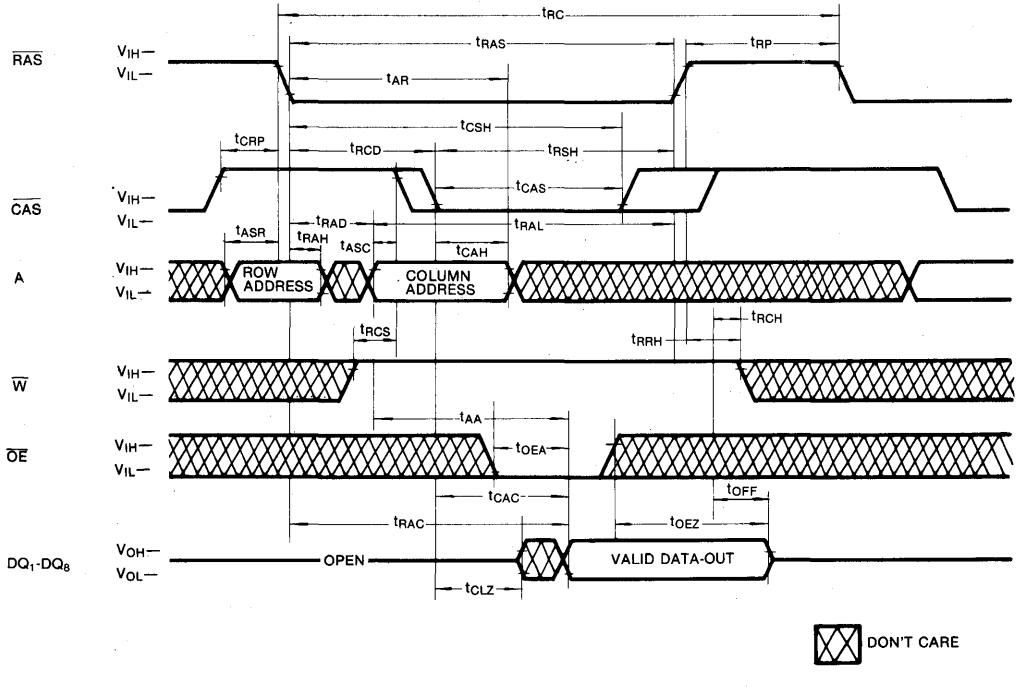
(*) 50ns Product:Vcc=5V ± 5%, Cout=50pF

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} to V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or r_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point ony. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. 1024 cycle of Burst Refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification. (LL-version)

TIMING DIAGRAMS

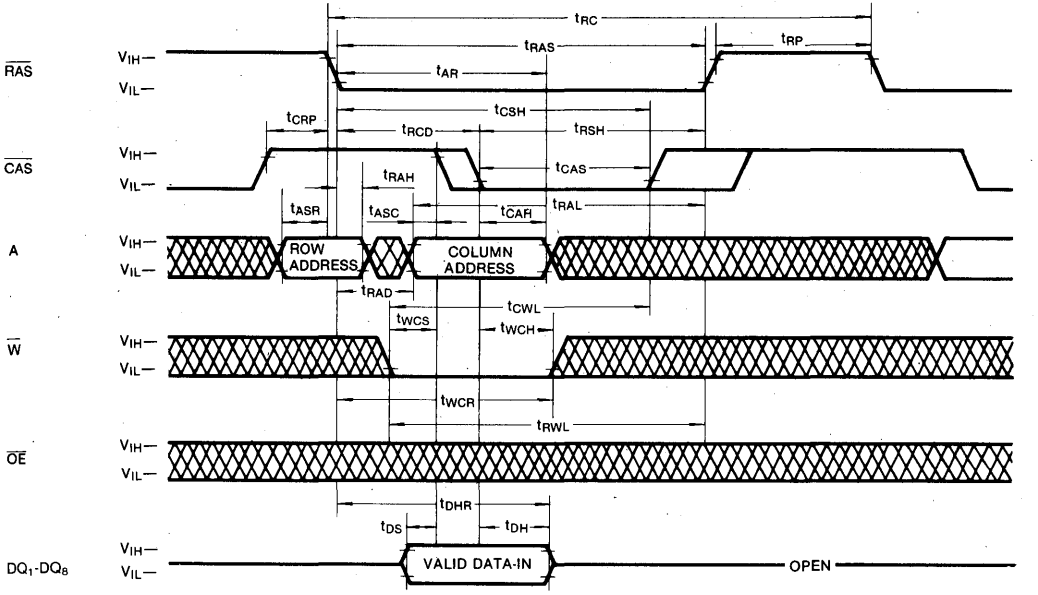
READ CYCLE



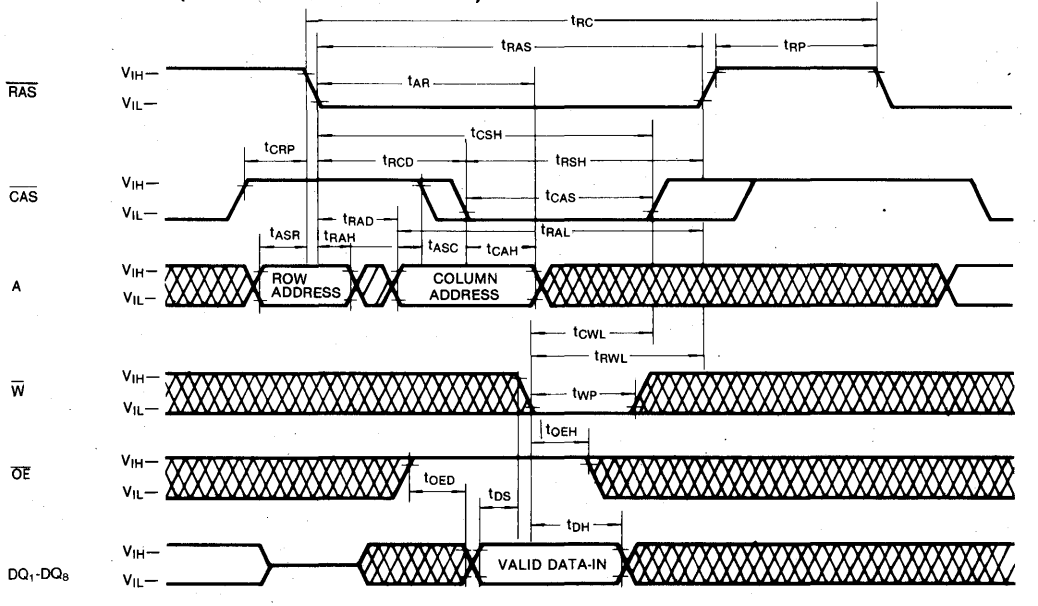
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

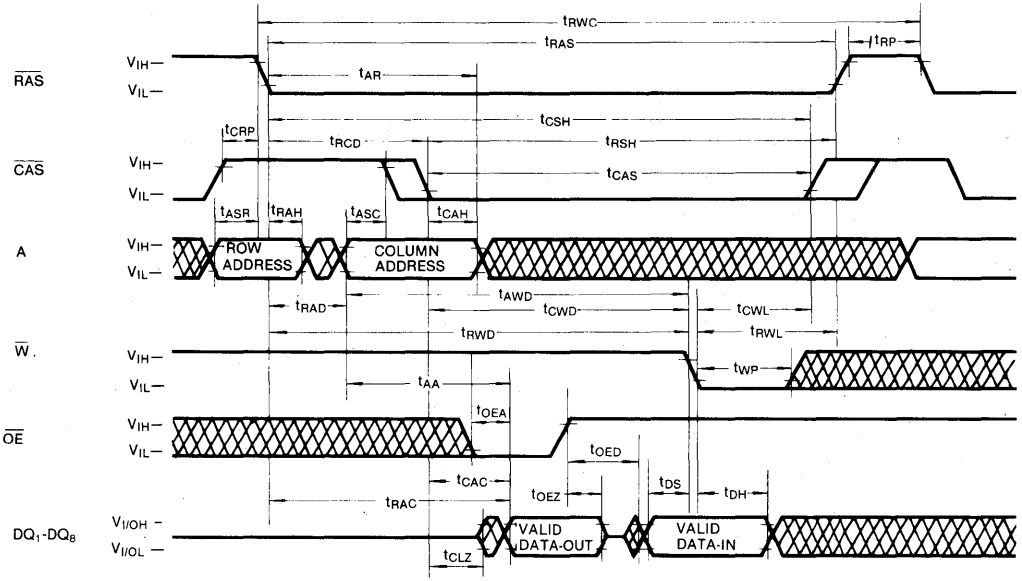


WRITE CYCLE (OE CONTROLLED WRITE)

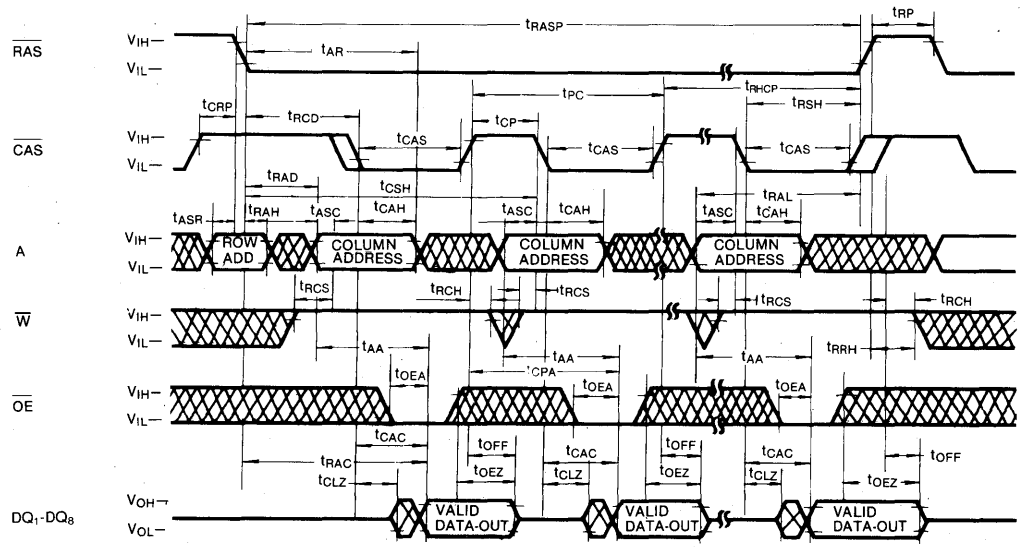


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



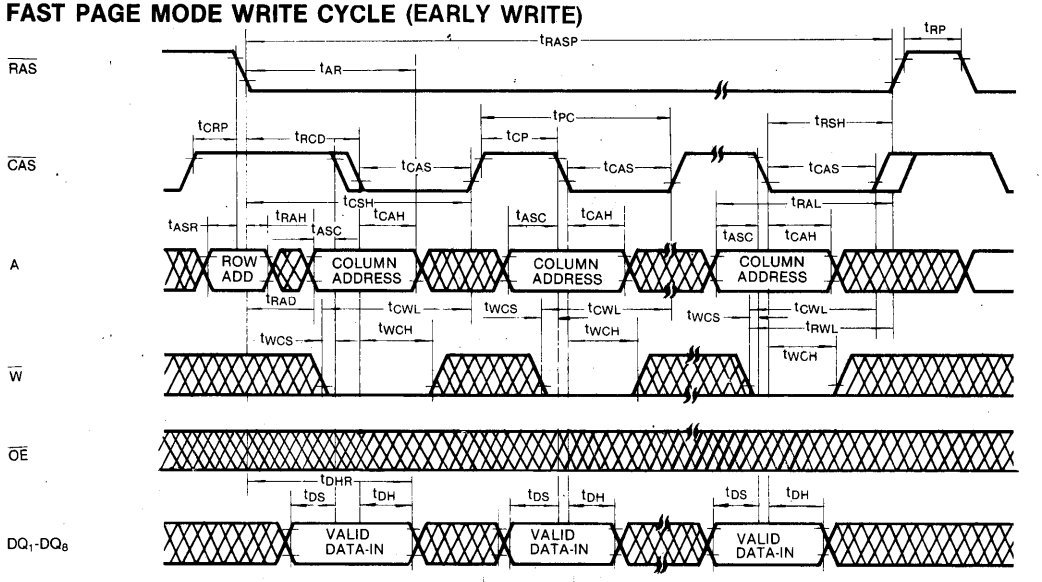
FAST PAGE MODE READ CYCLE



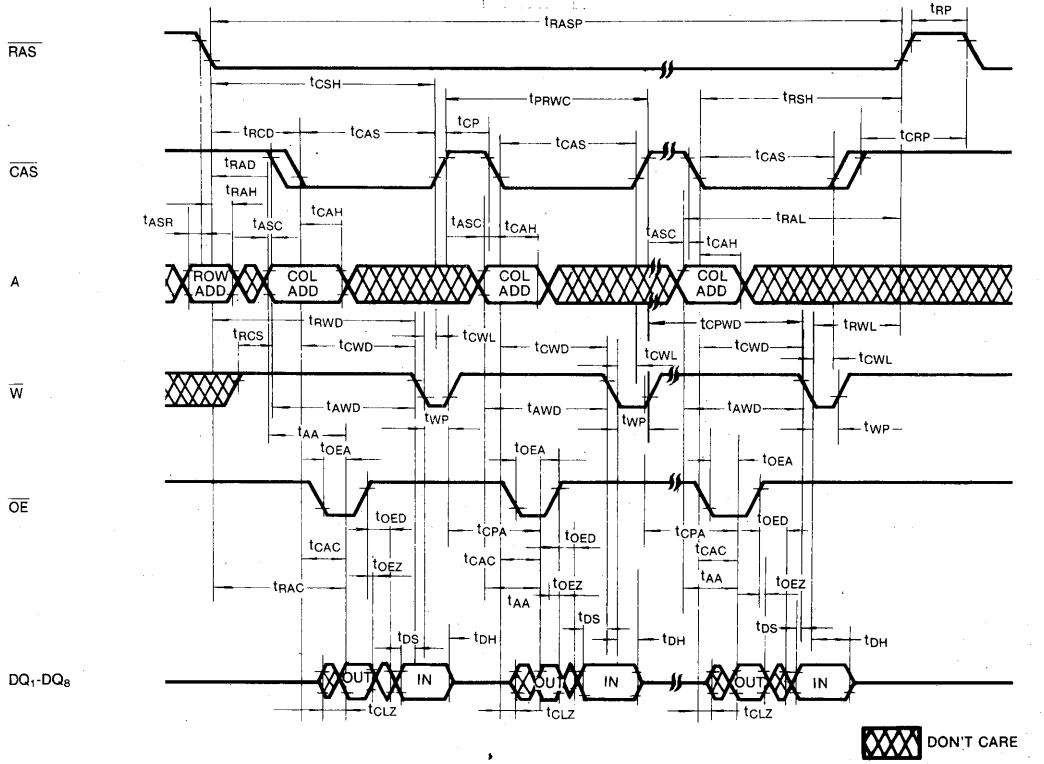
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



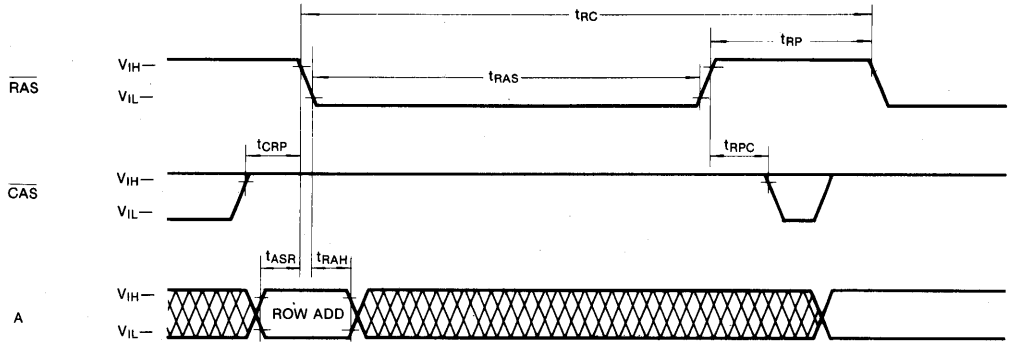
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

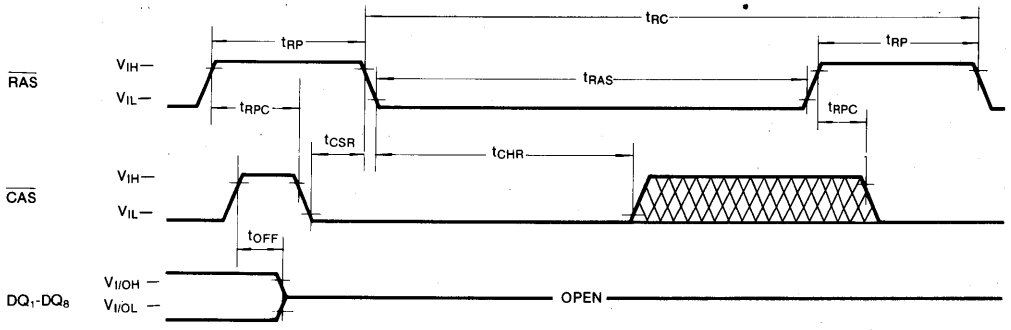
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



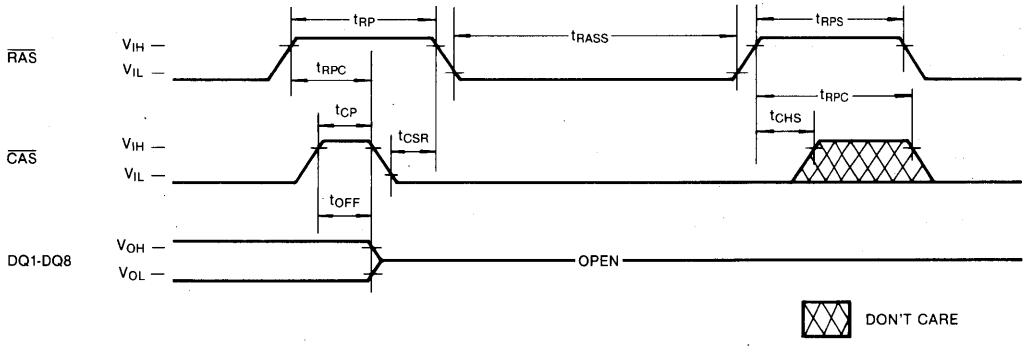
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care



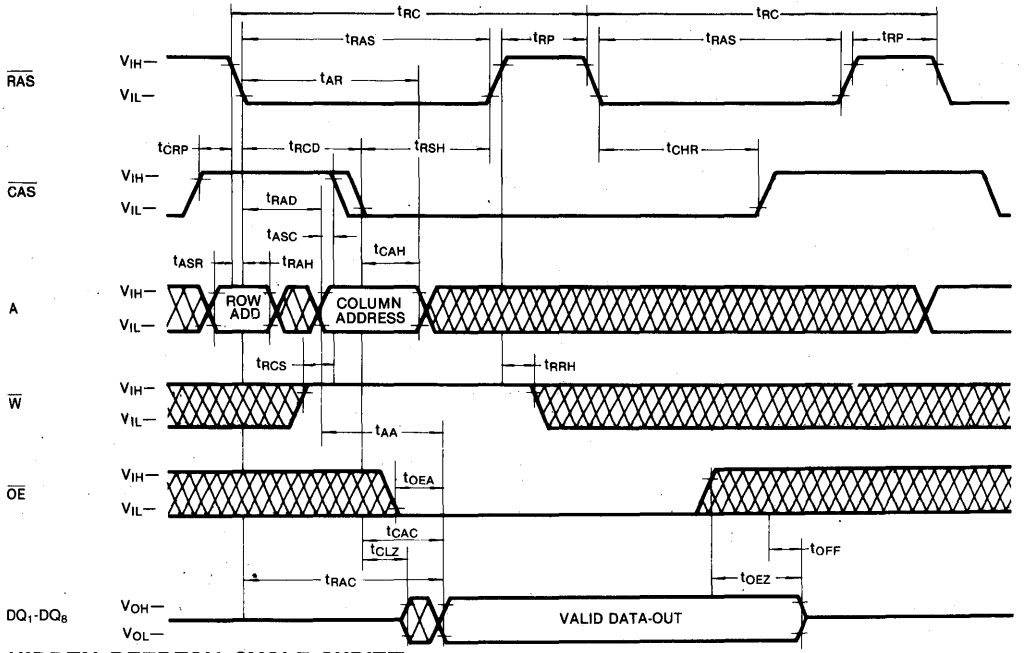
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care

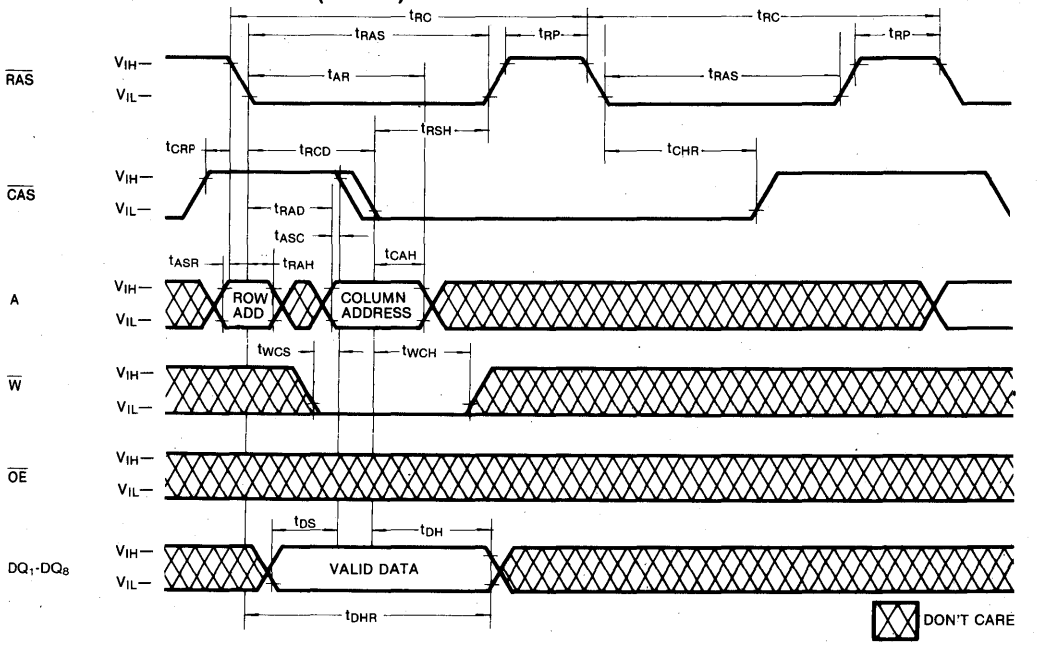


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

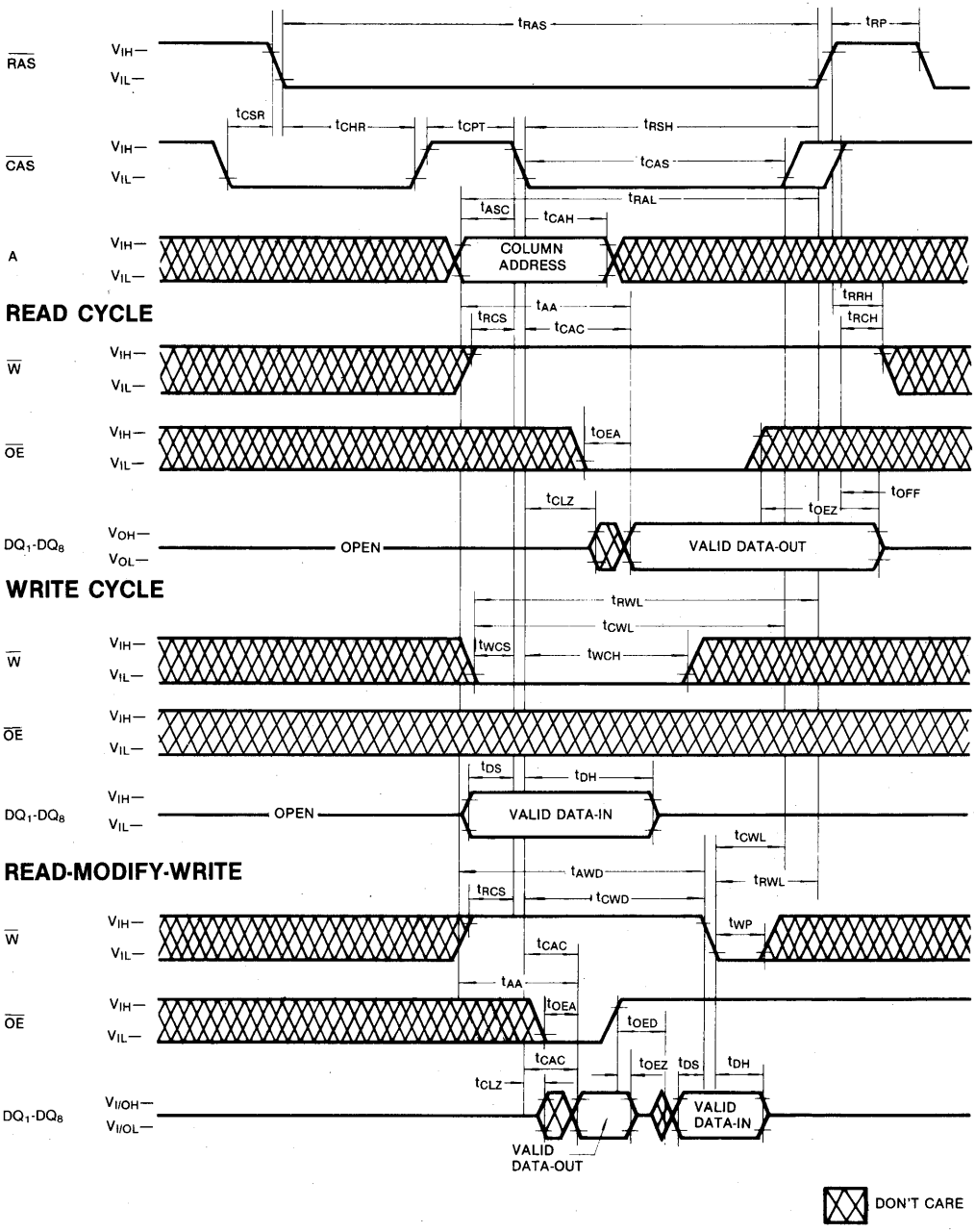


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

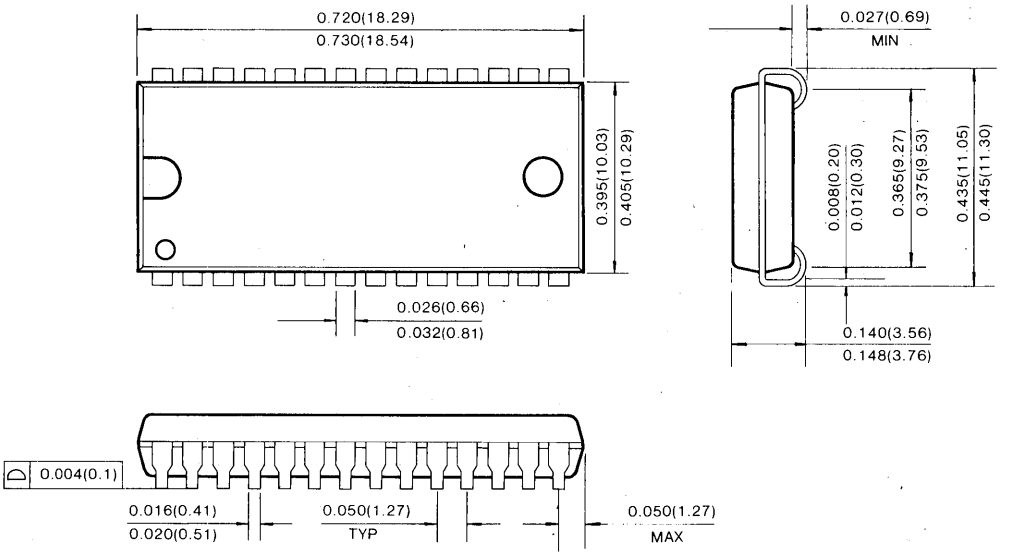
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



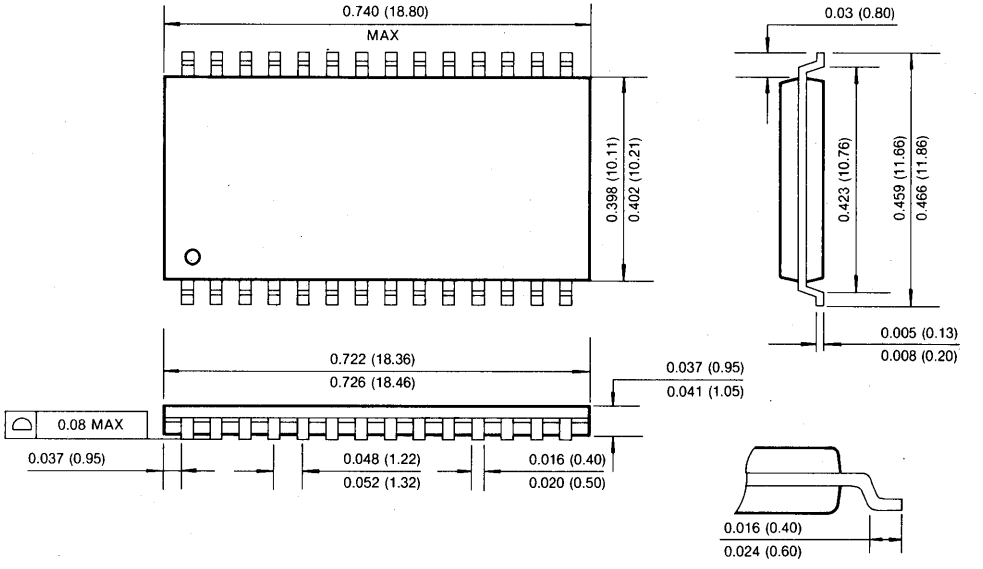
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



512K ×8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM48C514B/BL/BLL-5	50ns	17ns	90ns	20ns
KM48C514B/BL/BLL-6	60ns	17ns	110ns	24ns
KM48C514B/BL/BLL-7	70ns	20ns	130ns	29ns

- **Fast Page Mode with Extended Data Out**
- **Self Rdfresh operation (LL-ver)**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Byte Read/Write Operation**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Dual +5V±10% power supply**
- **Refresh Cycle**
  -1024 cycle/16ms (Normal)
  -1024 cycle/128ms (L/LL-ver)
- **Power Dissipation**
  -Standby: 5.5mW (Normal)
  1.1mW (L-version)
  0.83mW (LL-version)
  -Active (50/60/70): 470/385/360mW
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP II**

GENERAL DESCRIPTION

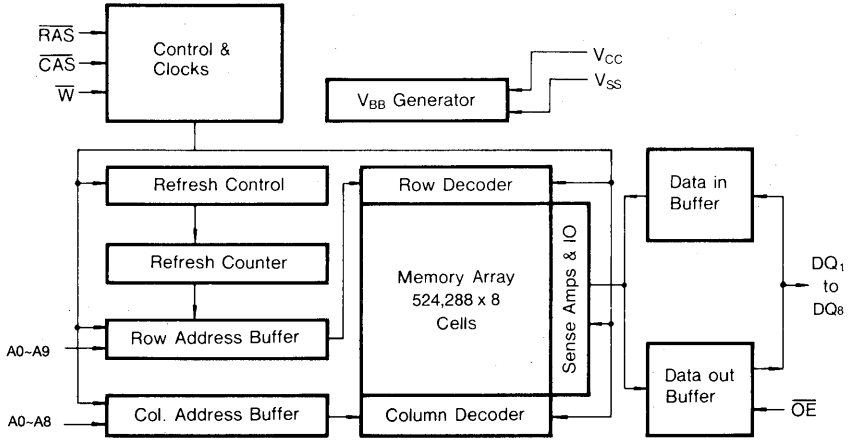
The Samsung KM48C514B/BL/BLL is a CMOS high speed 524,288 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM48C514B/BL/BLL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48C514B/BL/BLL is fabricated using Samsung's advanced CMOS process.

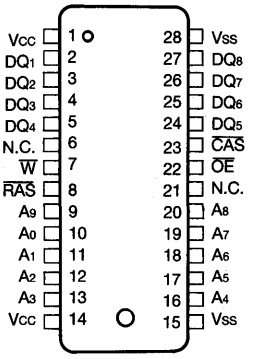
4

FUNCTIONAL BLOCK DIAGRAM



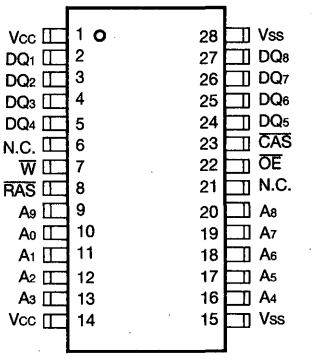
PIN CONFIGURATION (Top Views)

• KM48C514BJ/BLJ/BLLJ



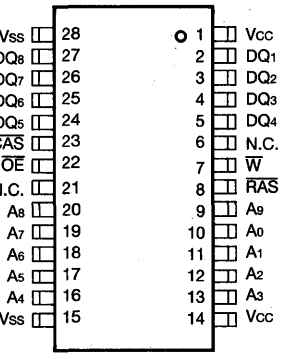
(SOJ)

• KM48C514BT/BLT/BLLT



(TSOP(II)-Forward Type)

• KM48C514BTR/BLTR/BLLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A0-A9	Address Inputs
DQ1~8	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VCC	Power(+5 V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to 7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	W

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	KM48C514B/BL/BLL-5 KM48C514B/BL/BLL-6 KM48C514B/BL/BLL-7	I_{CC1}	-	85 70 65	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM48C514B/BL/BLL-5 KM48C514B/BL/BLL-6 KM48C514B/BL/BLL-7	I_{CC3}	-	85 70 65	mA mA mA
EDO Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM48C514B/BL/BLL-5 KM48C514B/BL/BLL-6 KM48C514B/BL/BLL-7	I_{CC4}	-	65 55 50	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM48C514B KM48C514BL KM48C514BLL	I_{CC5}	-	1 200 150	mA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48C514B/BL/BLL-5 KM48C514B/BL/BLL-6 KM48C514B/BL/BLL-7	I_{CC6}	-	85 70 65	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=0.2V D_{IN}=Don't Care, T_{RC}=125μS T_{RAS}=T_{RAS} min.~300ns	KM48C514BL	I_{CC7}	-	300	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_9=V_{CC}-0.2V or 0.2V DQ_1-DQ_8=V_{CC}-0.2V, 0.2V or Open	KM48C514BLL	I_{CC8}	-	200	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}+0.5V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$,$\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5V±10%, See notes 1,2)

Test condiition:V_{ih}/V_{il}=2.4/0.8V, V_{oh} V_{ol}=2.0/0.8V, Output loading C_L=100pF

Parameter	Symbol	-5(*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		ns	
Read-modify-write cycle time	t_{RWC}	135		155		185		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		17		17		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	3	20	ns	7,14
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	17		17		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	40		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10,000	10	10,000	15	10,000	ns	12
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	

(*) -50ns Product : Output Loading (C_L)=50pF, V_{CC}=5V ± 5%

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	8		10		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		50		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		15		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		10		15		ns	10
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		ns	6
Refresh period (Normal)	tREF		8		8		8	ms	
Refresh period (L-version)	tREF		64		64		64	ms	
Refresh Period(LL-version)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		42		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		95		ns	8
Column address to $\overline{W}$ delay time	tAWD	48		55		60		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		65		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		25		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	3
Hyper Page mode cycle time	tHPC	20		24		29		ns	12
Hyper Page mode read-modity-write cycle time	tHPRWC	62		71		81		ns	12
$\overline{CAS}$ precharge time (Hyper Page mode)	tCP	8		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page mode)	tRASP	50	100K	60	100K	70	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		15		15		20	ns	
$\overline{OE}$ to data dela	tOED	13		15		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	ns	7
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3

(*) -50ns Product : Output Loading (C_L)=50pF, V_{CC}=5V ± 5%

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{OE}$ commend hold time	tOEH	13		15		20		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	ns	7,14
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	ns	7
$\overline{W}$ to data delay	tWED	13		15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width(Hyper page Cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width(LL-ver)	tRASS	100		100		100		μs	13
$\overline{RAS}$ precharge time (LL-ver	tRPS	90		110		130		ns	13
$\overline{CAS}$ hold time (LL-ver)	tCHS	-50		-50		-50		ns	13

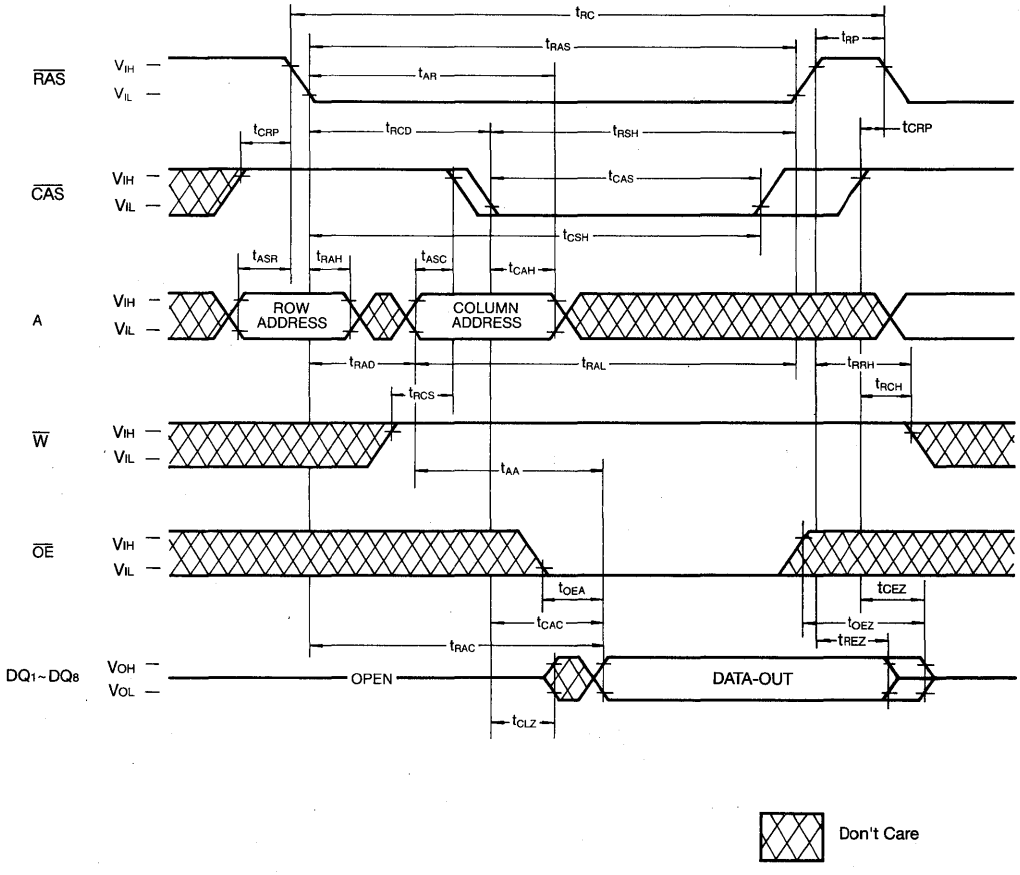
(*) -50ns Product : Output Loading (C_L)=50pF, V_{CC}=5V $\pm$ 5%

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs except tHPC and tHPRWC.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD $\geq$ tRCD (max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS $\geq$ tWCS(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD $\geq$ tCWD(min), tRWD $\geq$ tRWD(min) and tAWD $\geq$ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. tASC $\geq$ tCPmin, Assume tT=2.0 ns
13. 1024 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (LL-ver)
14. If $\overline{RAS}$ goes high befored $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going, If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going

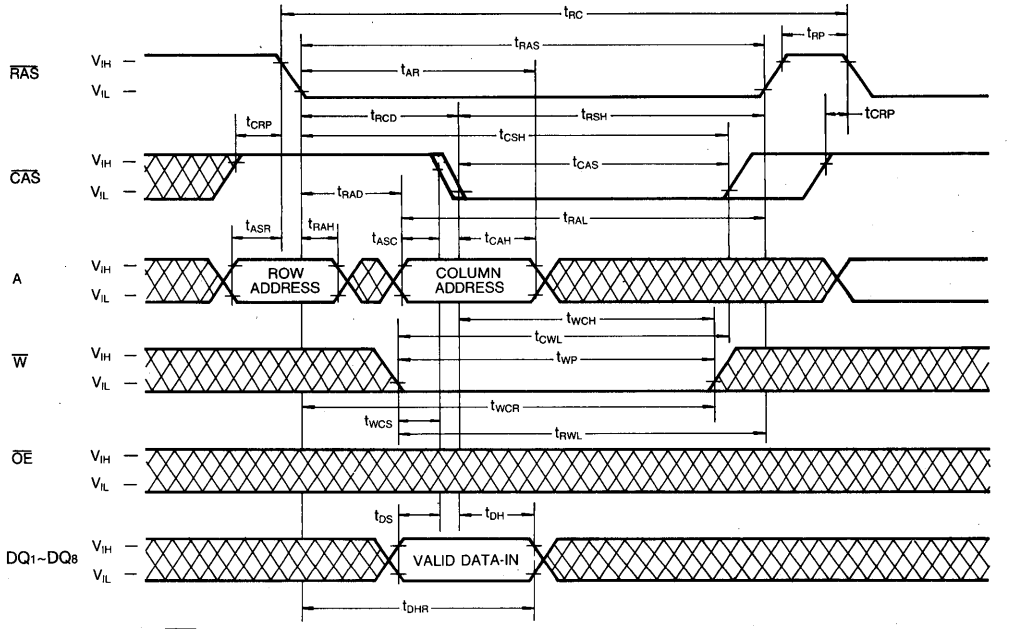
TIMING DIAGRAMS

READ CYCLE



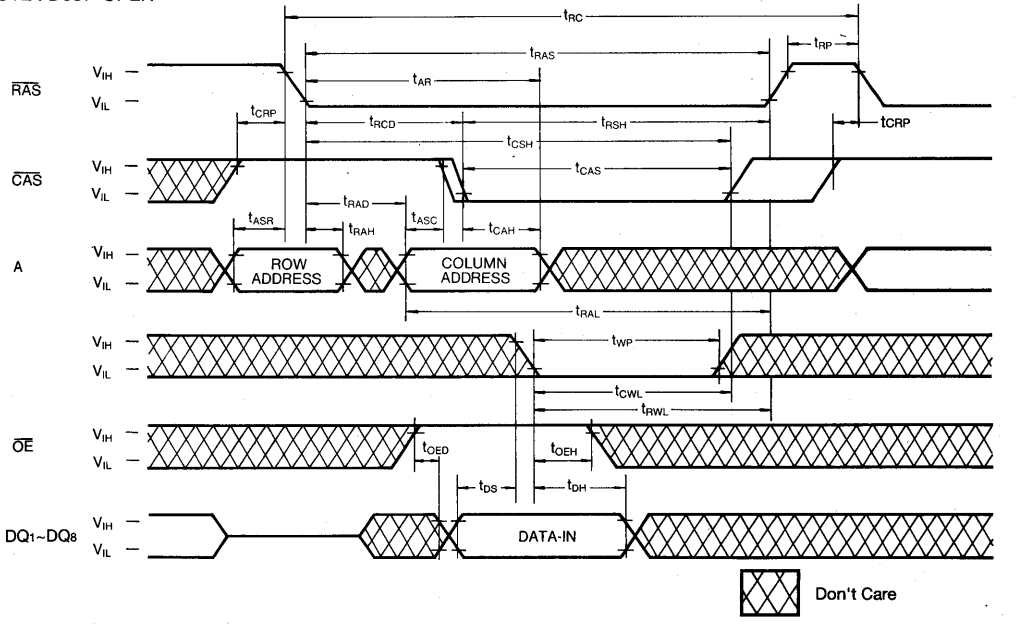
WRITE CYCLE (EARLY CYCLE)

NOTE : DOUT=OPEN



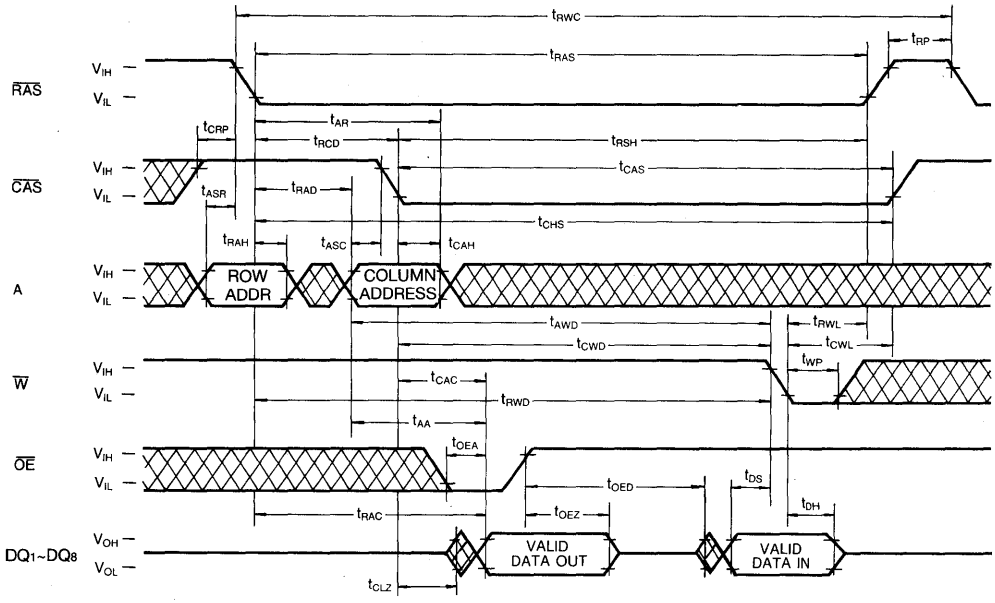
WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : DOUT=OPEN

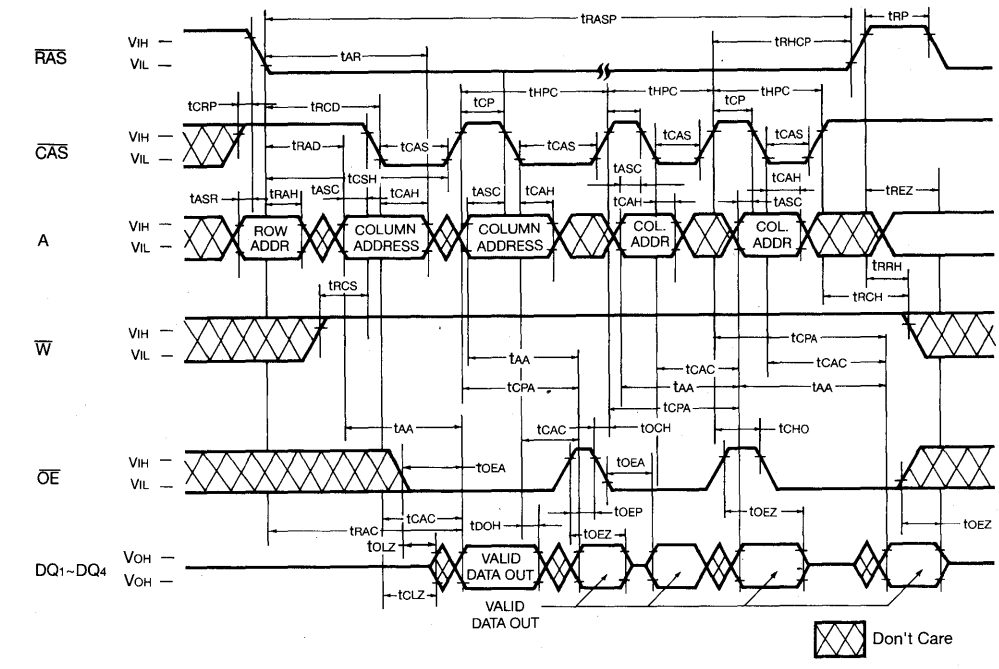


SAMSUNG ELECTRONICS

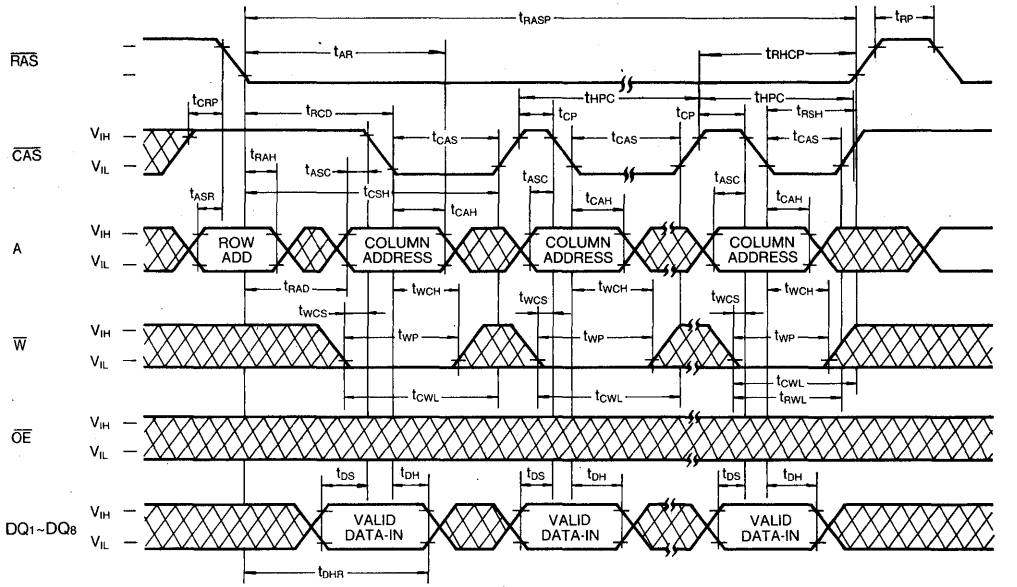
READ-MODIFY-WRITE CYCLE



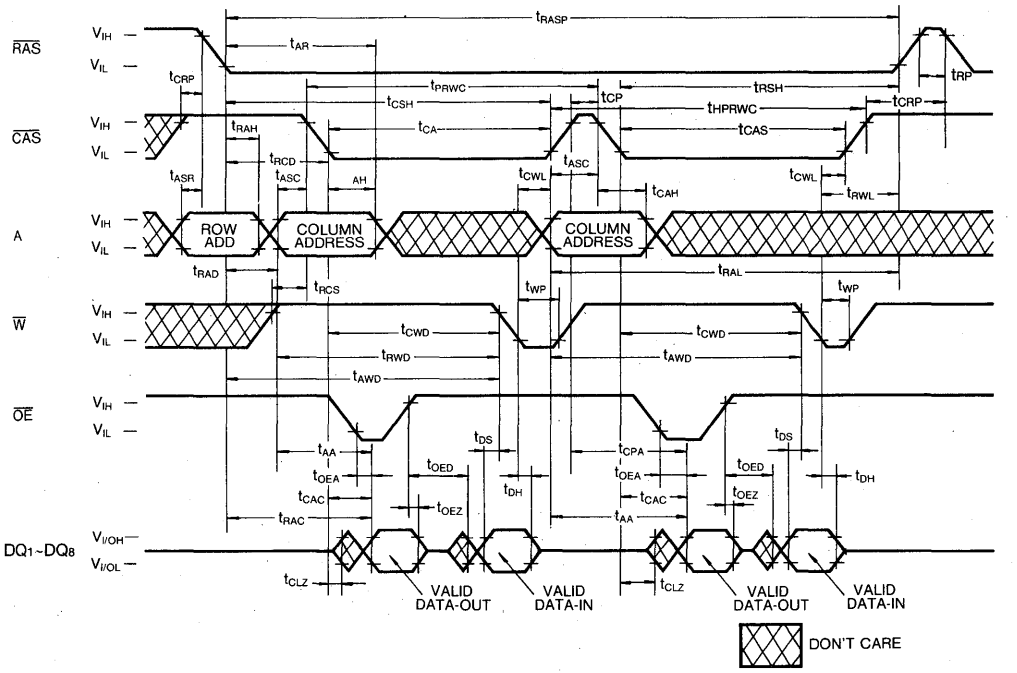
HYPER PAGE READ CYCLE



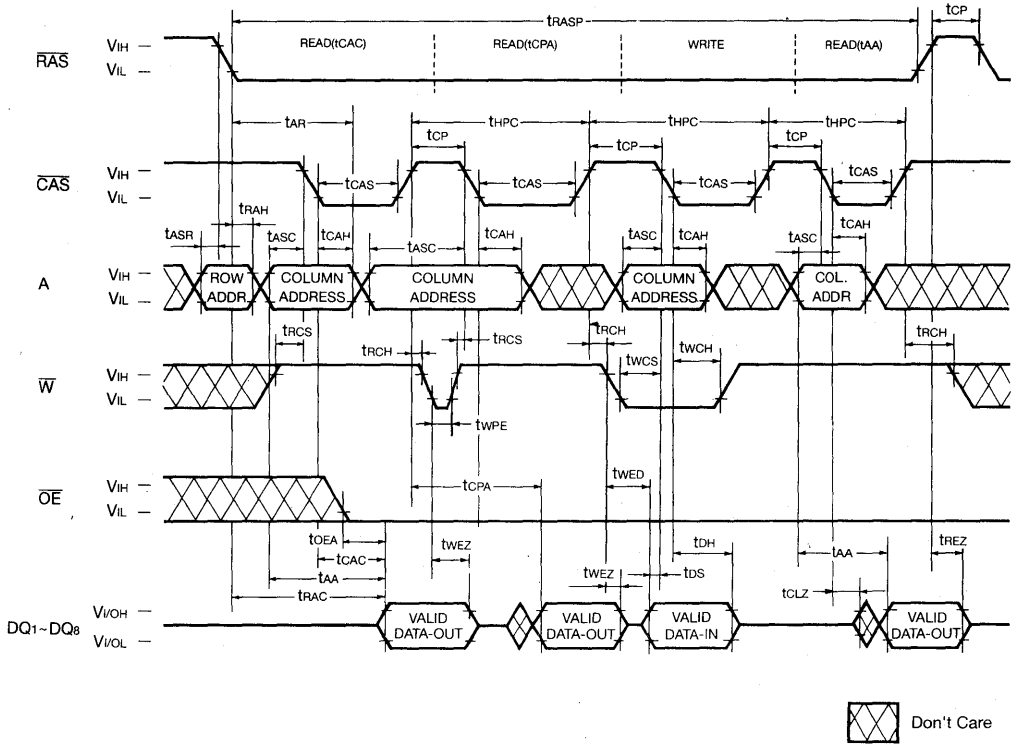
HYPER PAGE WRITE CYCLE (EARLY WRITE)



HYPER PAGE READ-MODIFY-WRITE CYCLE

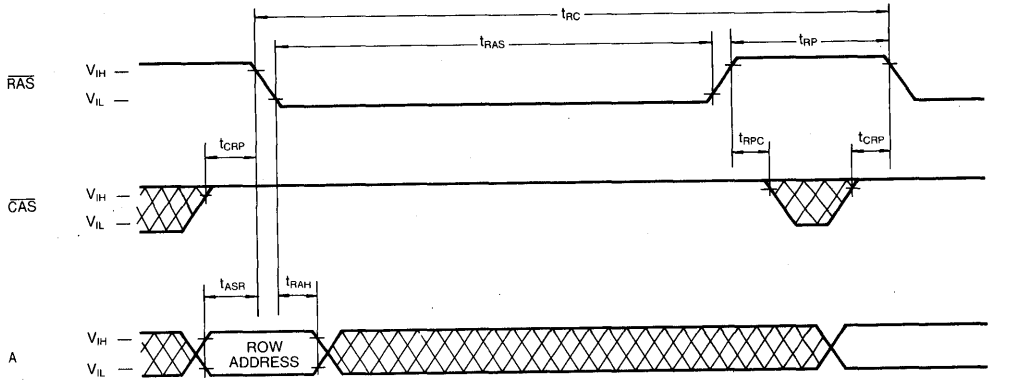


HYPER PAGE READ AND WRITE MIXED CYCLE



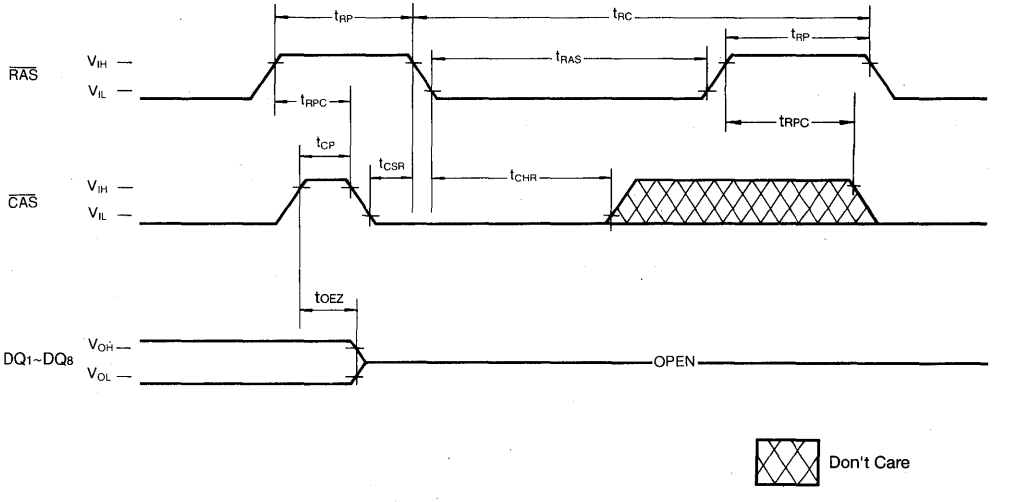
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, DIN=Don't Care
Dout=Open

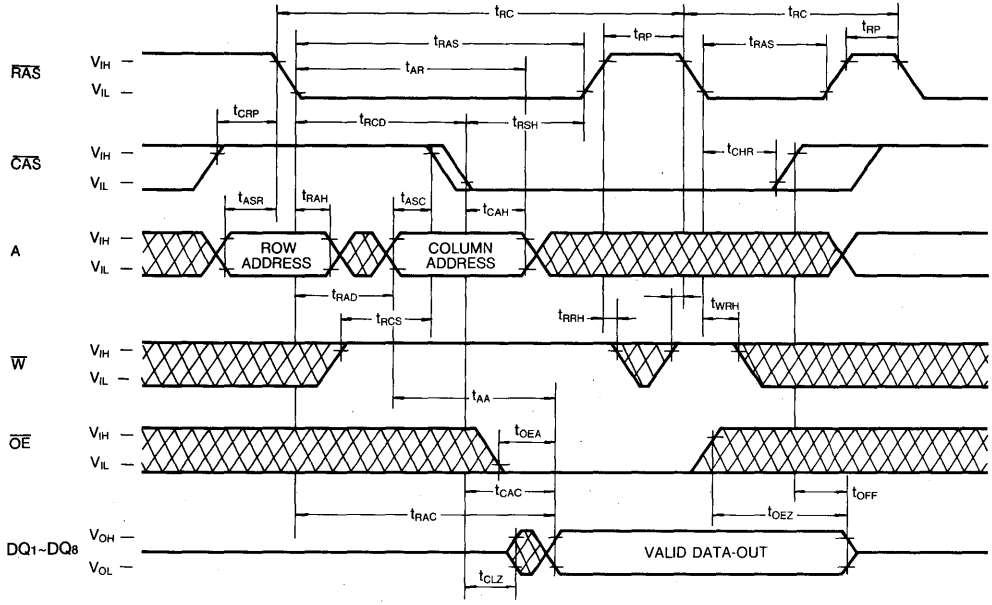


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

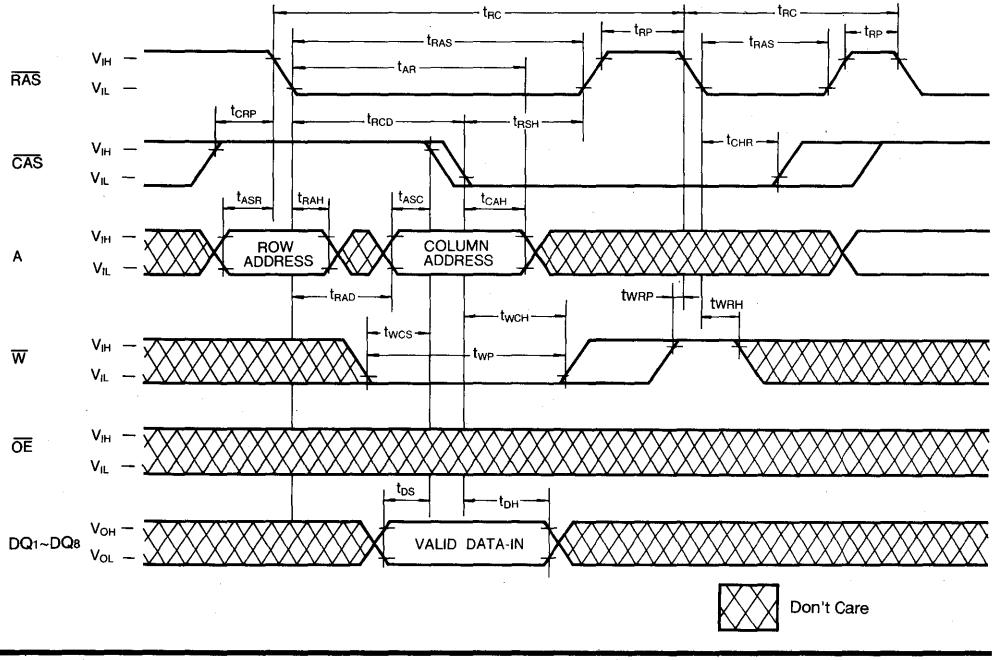
NOTE : $\overline{W}$, $\overline{OE}$, A=Don't Care



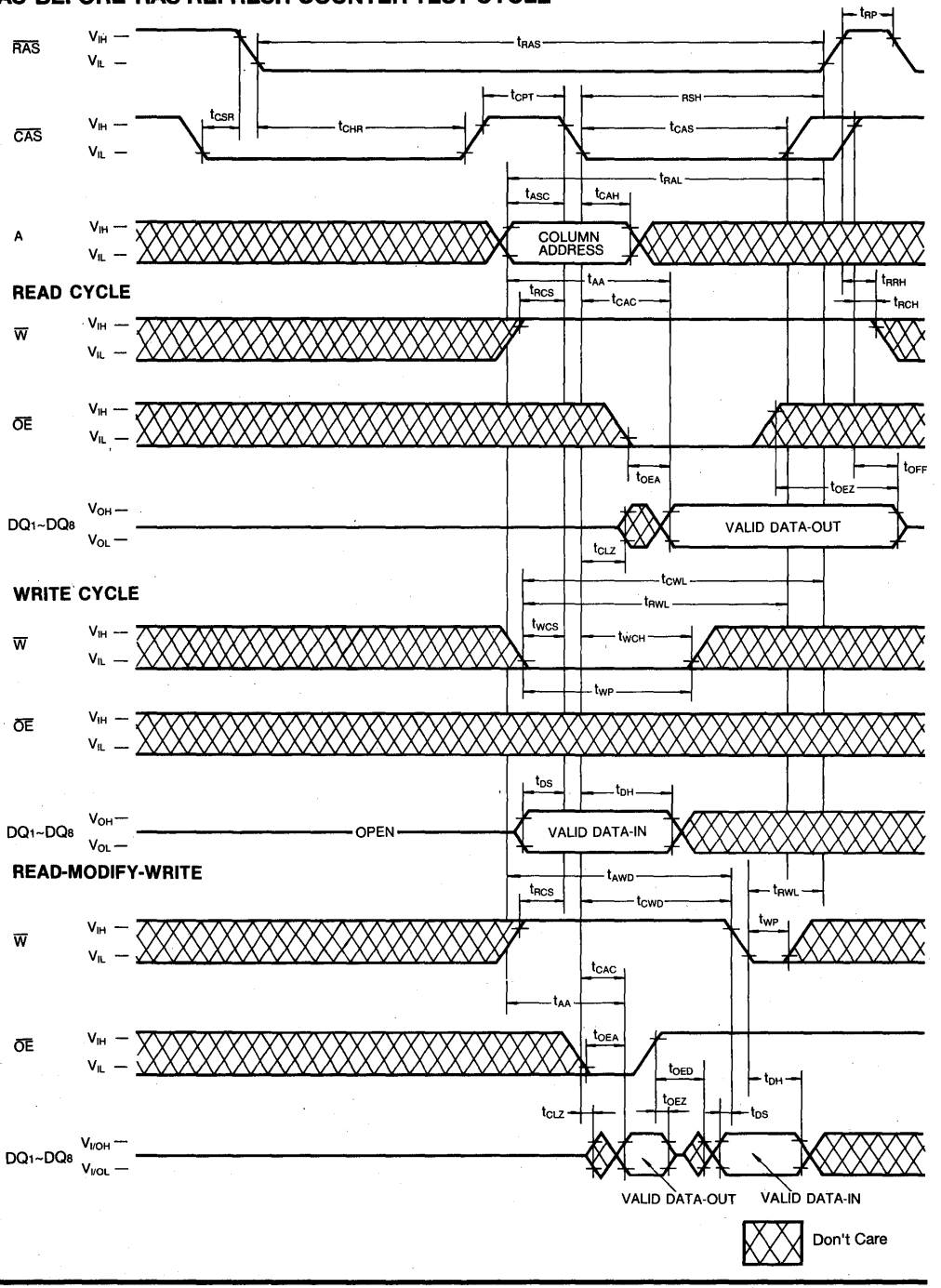
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



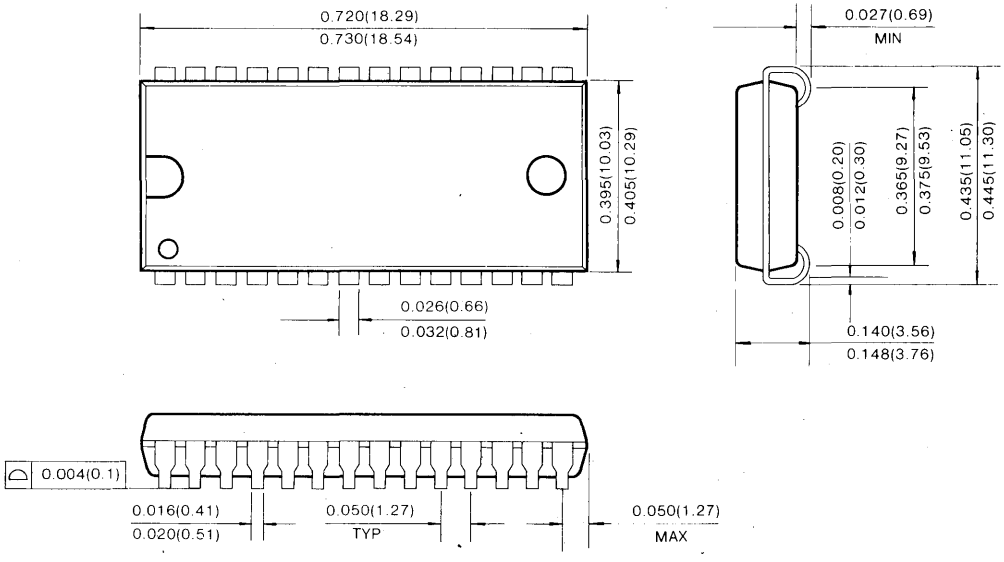
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



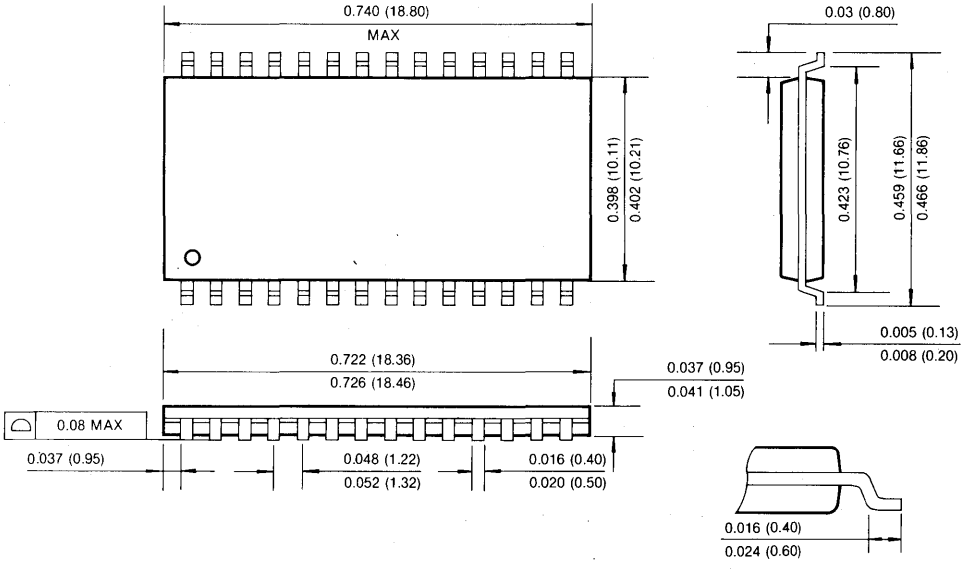
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



512K ×9 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM49C512B/BL/BLL-6	60ns	15ns	110ns
KM49C512B/BL/BLL-7	70ns	20ns	130ns
KM49C512B/BL/BLL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Self Refresh operation (LL-version)**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Dual +5.0V±10% power supply**
- **Refresh Cycle**
  - **-1024 cycle/16ms (Normal)**
  - **-1024 cycle/128ms (L-version)**
  - **-1024 cycle/128ms (LL-version)**
- **Power Dissipation**
  - **-Standby: 5.5mW (Normal)**
  - **1.1mW (L-version)**
  - **0.83mW (LL-version)**
  - **-Active (60/70/80): 415/385/360mW**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP II**

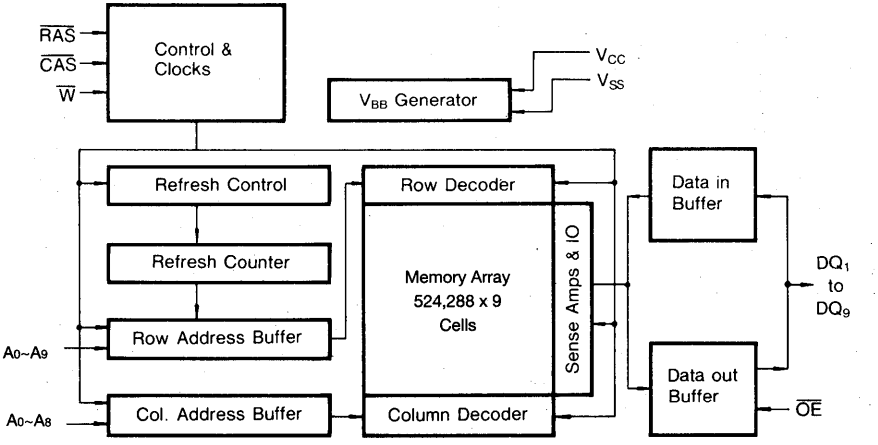
GENERAL DESCRIPTION

The Samsung KM49C512B/BL/BLL is a CMOS high speed 524,288 bit×9 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM49C512B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

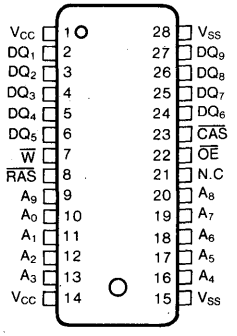
The KM49C512B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



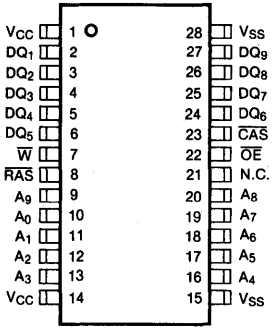
PIN CONFIGURATION (Top Views)

• **KM49C512BJ/BLJ/BLLJ**



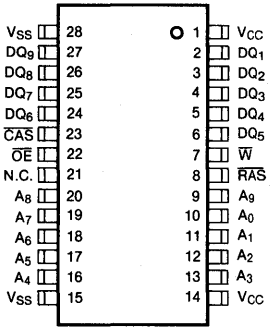
(SOJ)

• **KM49C512BT/BLT/BLLT**



(TSOP(II)-Forward Type)

• **KM49C512BTR/BLTR/BLLTR**



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A_0-A_9	Address Input
DQ_{1-9}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe

Pin Name	Pin Function
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	KM49C512B/BL/BLL-6 KM49C512B/BL/BLL-7 KM49C512B/BL/BLL-8	I_{CC1}	-	75 70 65	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM49C512B/BL/BLL-6 KM49C512B/BL/BLL-7 KM49C512B/BL/BLL-8	I_{CC3}	-	75 70 65	mA mA mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM49C512B/BL/BLL-6 KM49C512B/BL/BLL-7 KM49C512B/BL/BLL-8	I_{CC4}	-	55 50 45	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM49C512B KM49C512BL KM49C512BLL	I_{CC5}	-	1 200 150	mA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM49C512B/BL/BLL-6 KM49C512B/BL/BLL-7 KM49C512B/BL/BLL-8	I_{CC6}	-	75 70 65	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=0.2V D_{IN}=Don't Care, T_{RC}=125μS T_{RAS}=T_{RAS} min.~300ns	KM49C512BL	I_{CC7}	-	300	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_9=V_{CC}-0.2V or 0.2V DQ_1-DQ_8=V_{CC}-0.2V, 0.2V or Open	KM49C512BLL	I_{CC8}	-	200	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}+0.5V$, all other pins not under test=0 V)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_9)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time referenced to $\overline{RAS}$	tAR	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		20		ns	
Data-in set-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	10		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (LL-version)	tREF		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		95		100		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	tRASP	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	tCP	10		10		10		ns	
Access time from $\overline{OE}$	tOEA		15		20		20	ns	
$\overline{OE}$ to data-in delay time	tOED	15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	20	0	20	ns	
$\overline{OE}$ commend hold time	tOEH	15		20		20		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		μs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	12

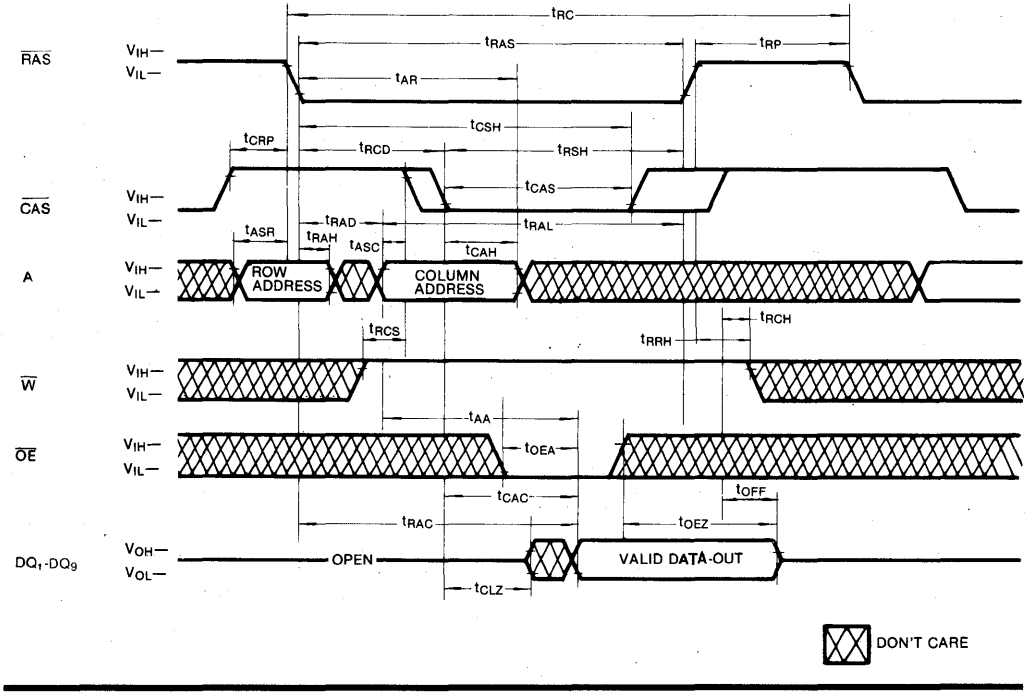
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. t_{OFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} to V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min)and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. 1024 cycle of burst refresh must be executed within 16ms before and after refresh, in order to meet refesh specification(LL-version).

4

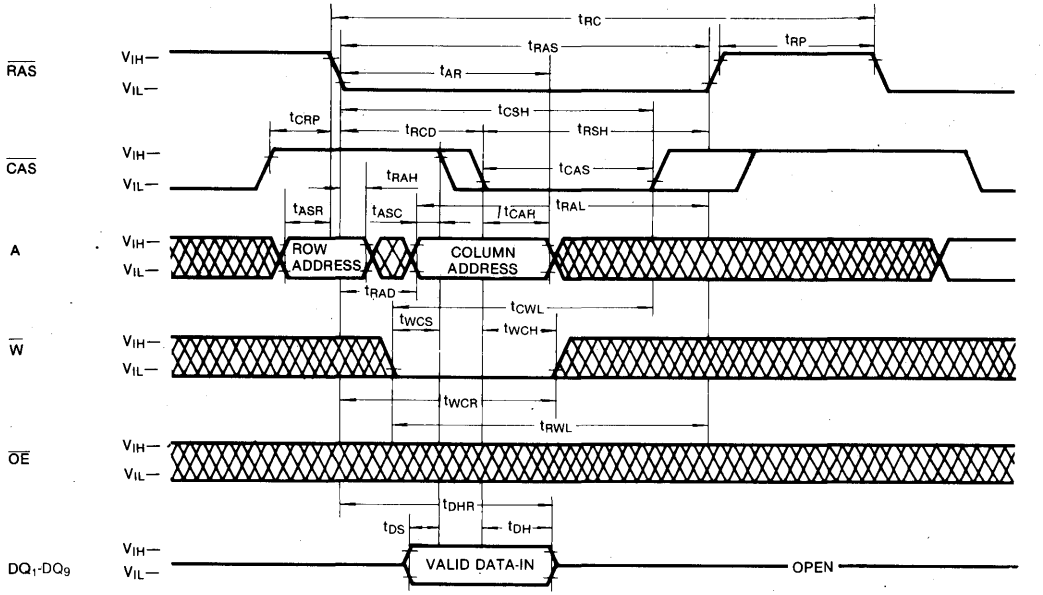
TIMING DIAGRAMS

READ CYCLE

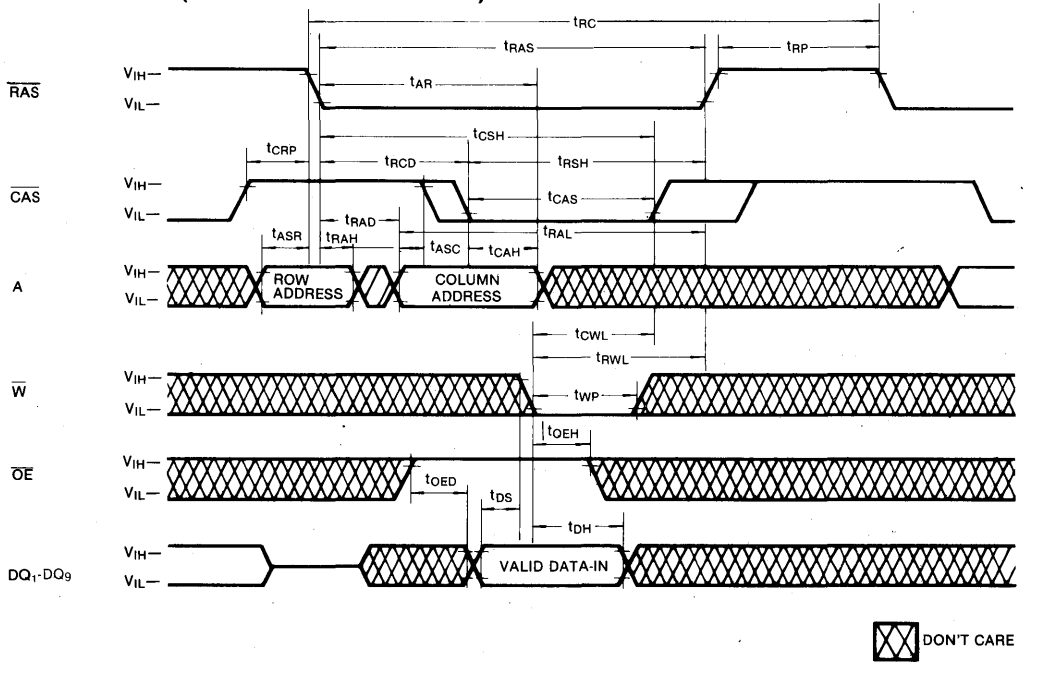


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

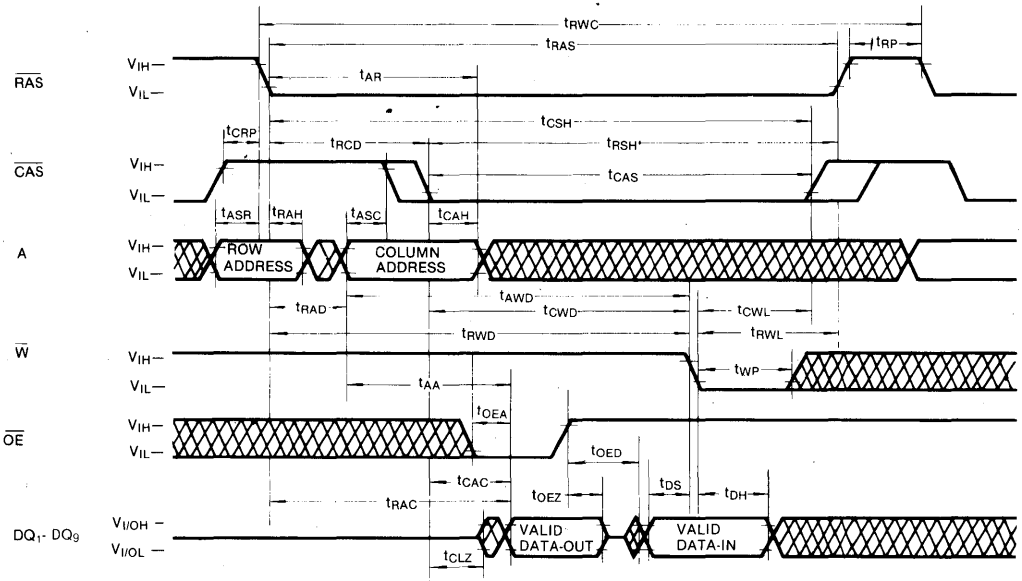


WRITE CYCLE (OE CONTROLLED WRITE)

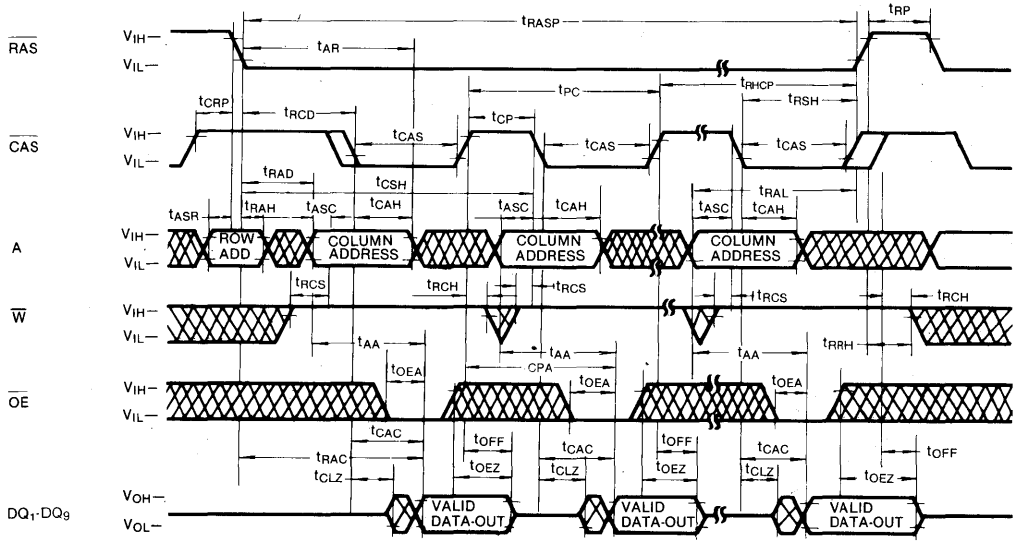


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



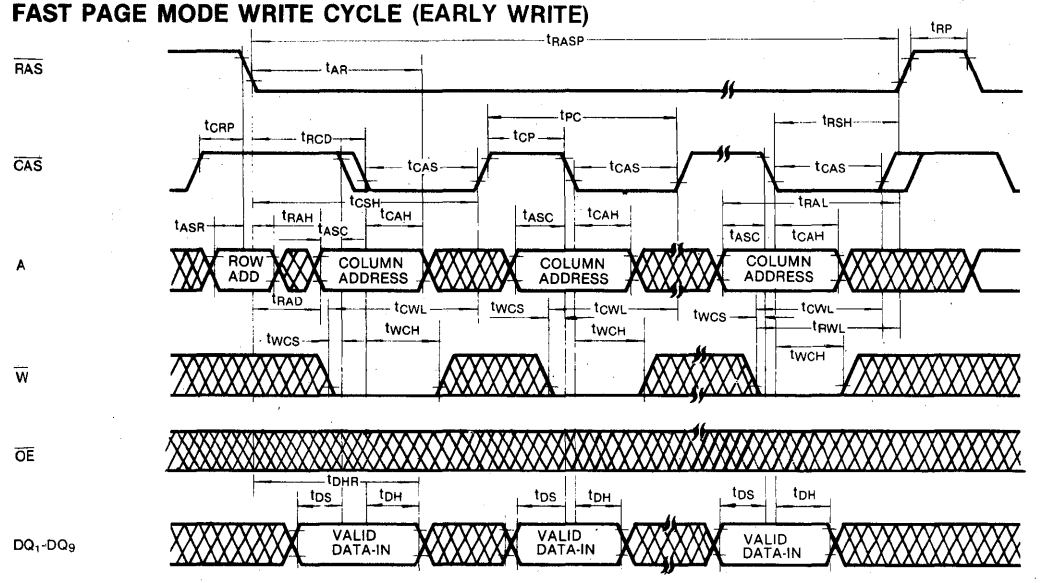
FAST PAGE MODE READ CYCLE



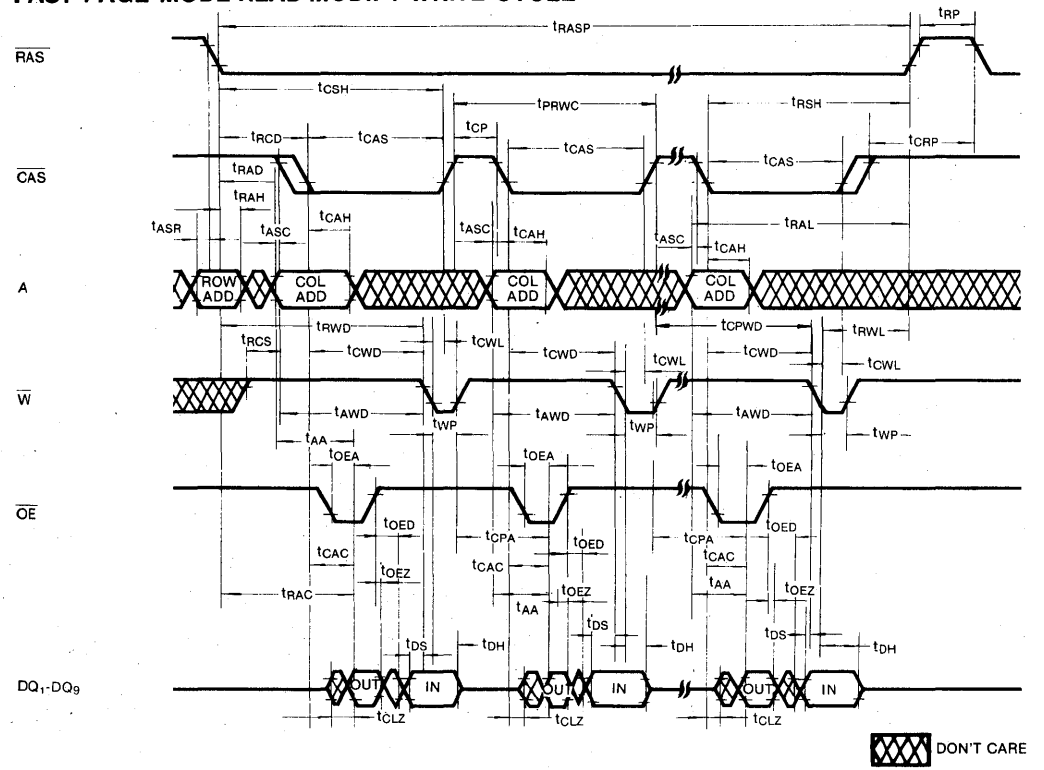
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



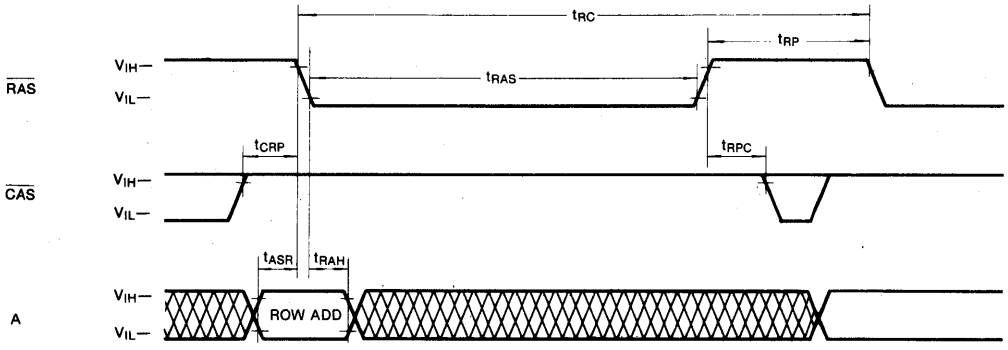
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

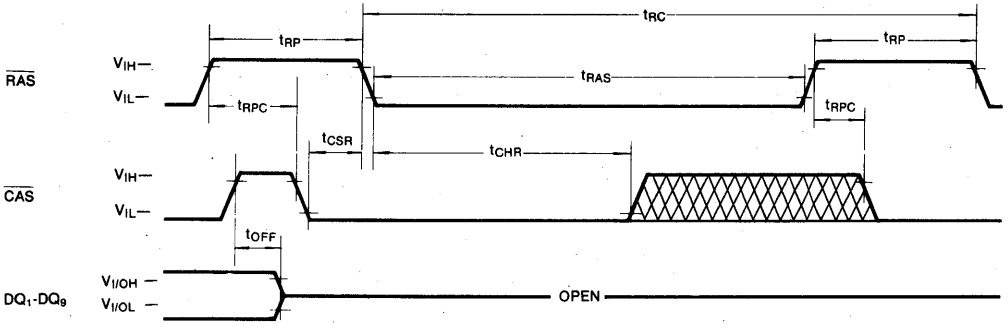
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



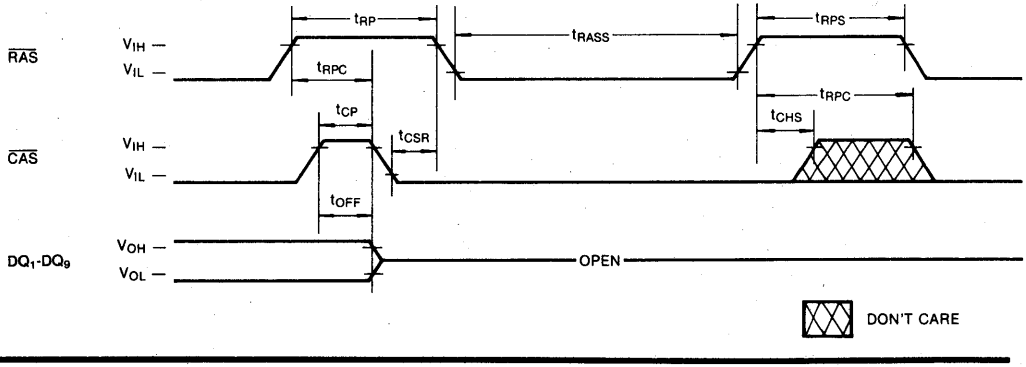
$\overline{CAS}$-before-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care



$\overline{CAS}$-before-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

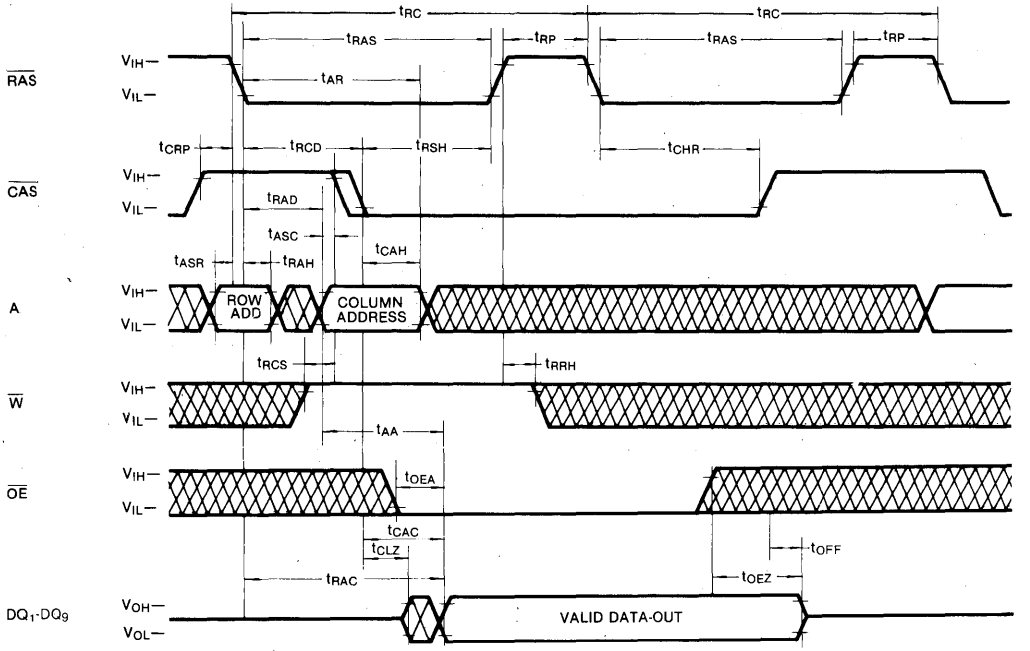
NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care



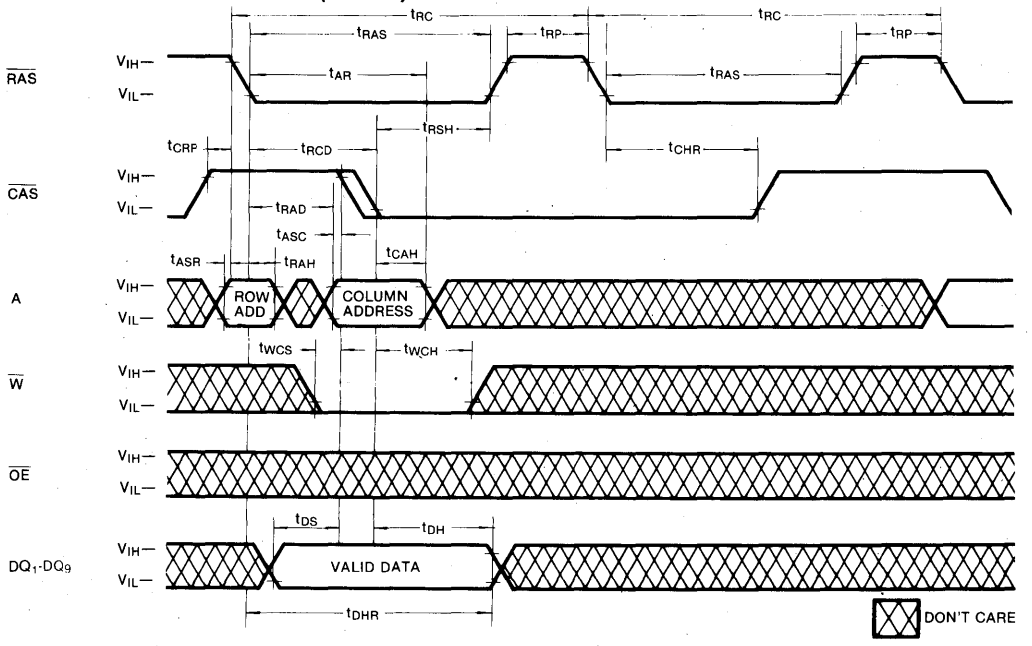
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

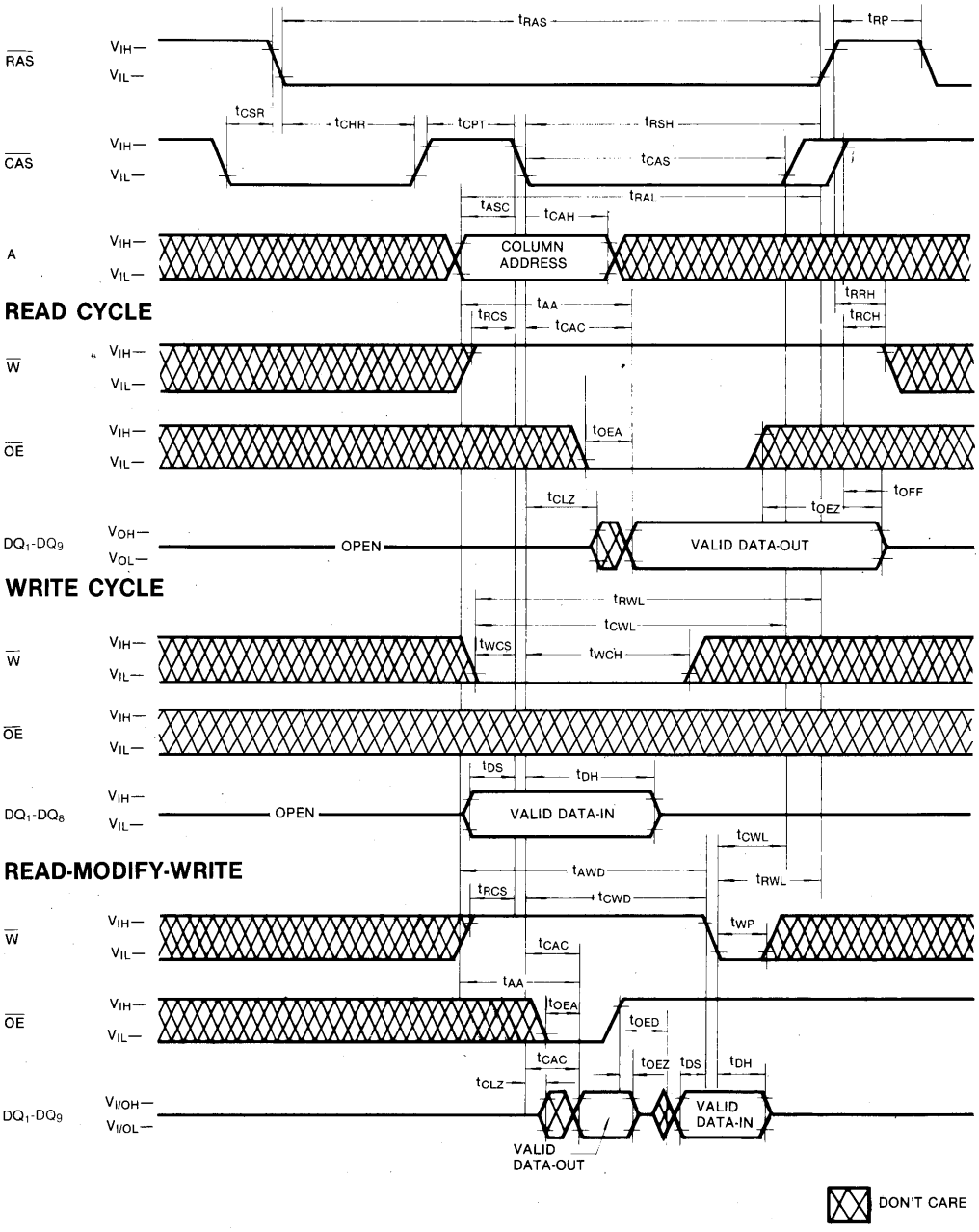


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

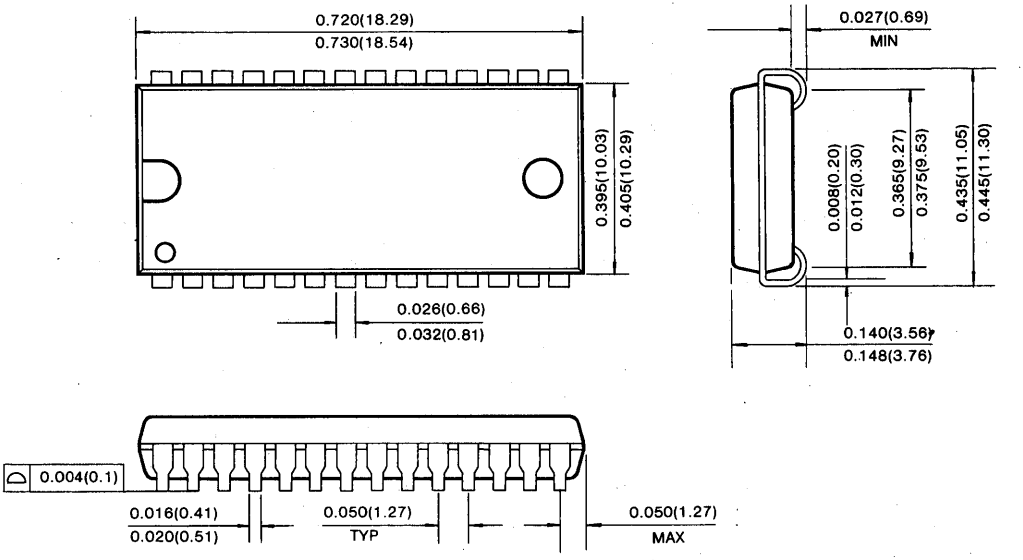
$\overline{CAS}$-before-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



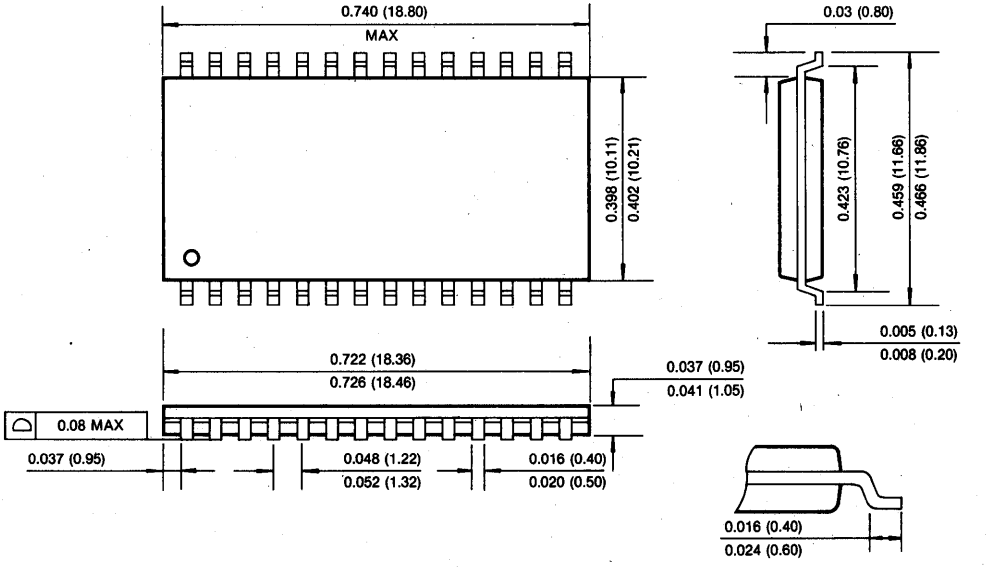
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



256K × 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM416C256B/BL/BLL-5	50ns	15ns	90ns
KM416C256B/BL/BLL-6	60ns	15ns	110ns
KM416C256B/BL/BLL-7	70ns	20ns	130ns
KM416C256B/BL/BLL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Self Refresh operation (LL-version)**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +5.0V±10% power supply**
- **Refresh Cycle**
  - **-512 cycle/8ms (Normal)**
  - **-512 cycle/64ms (L-version)**
  - **-512 cycle/128ms (LL-version)**
- **Power Dissipation**
  - **-Standby: 5.5mW (Normal)**
    1.1mW (L-version)
    0.83mW (LL-version)
  - **-Active (50/60/70/80): 605/495/440/415mW**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP II**

GENERAL DESCRIPTION

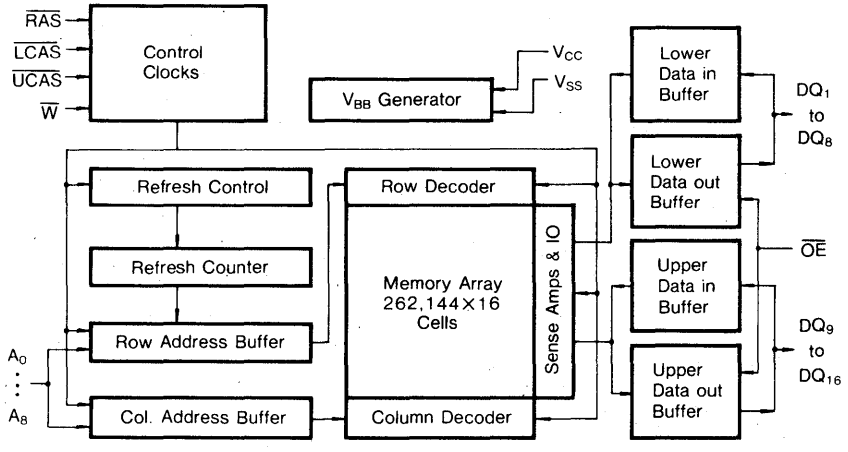
The Samsung KM416C256B/BL/BLL is a CMOS high speed 262,144 bit × 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM416C256B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416C256B/BL/BLL is fabricated using Samsung's advanced CMOS process.

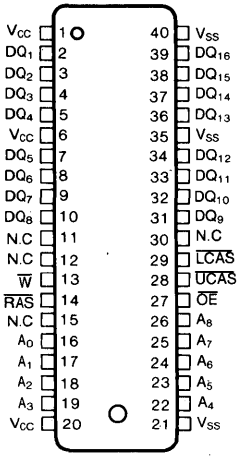
4

FUNCTIONAL BLOCK DIAGRAM



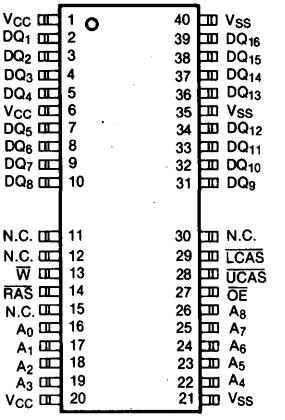
PIN CONFIGURATION (Top Views)

• KM416C256BJ/BLJ/BLLJ



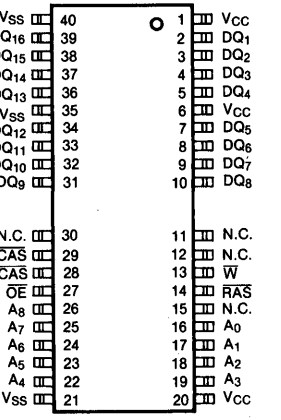
(SOJ)

• KM416C256BT/BLT/BLLT



(TSOP(II)-Forward Type)

• KM416C256BTR/BLTR/BLLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function	Pin Name	Pin Function
A_0-A_8	Address Inputs	$\overline{LCAS}$	Lower Column Address Strobe
$DQ_{1\text{-}16}$	Data In/Out	$\overline{W}$	Read/Write Input
V_{SS}	Ground	$\overline{OE}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
$\overline{UCAS}$	Upper Column Address Strobe	N.C.	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{RC}=min.)	KM416C256B/BL/BLL-5	I_{CC1}	-	110	mA
	KM416C256B/BL/BLL-6			90	mA
	KM416C256B/BL/BLL-7			80	mA
	KM416C256B/BL/BLL-8			75	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM416C256B/BL/BLL-5	I_{CC3}	-	110	mA
	KM416C256B/BL/BLL-6			90	mA
	KM416C256B/BL/BLL-7			80	mA
	KM416C256B/BL/BLL-8			75	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC}=min.)	KM416C256B/BL/BLL-5	I_{CC4}	-	70	mA
	KM416C256B/BL/BLL-6			60	mA
	KM416C256B/BL/BLL-7			55	mA
	KM416C256B/BL/BLL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)	KM416C256B	I_{CC5}	-	1	mA
	KM416C256BL			200	μA
	KM416C256BLL			150	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC}=min.)	KM416C256B/BL/BLL-5	I_{CC6}	-	110	mA
	KM416C256B/BL/BLL-6			90	mA
	KM416C256B/BL/BLL-7			80	mA
	KM416C256B/BL/BLL-8			75	mA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Max	Units
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{UCAS}$=$\overline{LCAS}$=0.2V D_{IN}=Don't Care, T_{RC}=125μS T_{RAS}=T_{RAS} min.~300ns	KM416C256BL	I_{CC7}	-	300	μA
Self Refresh Current $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_8=V_{CC}-0.2V or 0.2V DQ_1-DQ_{16}=V_{CC}-0.2V, 0.2V or Open	KM416C256BLL	I_{CCS}	-	200	μA
Input Leakage Current (Any input 0V$\leq V_{IN} \leq$$V_{CC}$+0.5V, all other pins not under test=0 volts)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V$\leq V_{OUT} \leq V_{CC}$)		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_8)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C$\leq$Ta$\leq$70°C, V_{CC}=5.0V$\pm$10%, See notes 1,2)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	135		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	15	10,000	20	10,000	20	10.000	ns	

(*) 50ns Product:VCC=5V $\pm$ 5%, Cout=50pF

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	35	20	45	20	50	20	60	ns	
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	11
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	6
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		10		10		ns	8
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		50		55		ns	
Write command pulse width	tWP	10		10		10		10		ns	6
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		20		ns	
Data-in set-up time	tDS	0		0		0		0		ns	
Data-in hold time	tDH	10		10		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	10
Refresh period (Normal)	tREF		8		8		8		8	ms	6
Refresh period (L-version)	tREF		64		64		64		64	ms	
Refresh period (LL-version)	tREF		128		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		40		50		50		ns	
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	75		85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	50		55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	55		60		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast page mode cycle time	tPC	35		40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	80		80		95		100		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	

(*) 50ns Product:VCC=5V ± 5%, Cout=50pF

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{CAS}$ precharge time (Fast Page Mode)	tCP	10		10		10		10		ns	
access time from $\overline{OE}$	tOEA		15		15		20		20	ns	
$\overline{OE}$ to data-in delay time	tOED	15		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	15		15		20		20		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

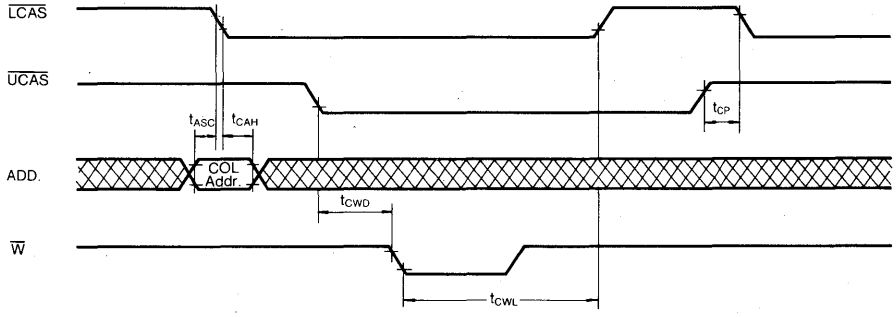
(*) 50ns Product:VCC=5V ± 5%, Cout=50pF

KM416C256B Truth Table

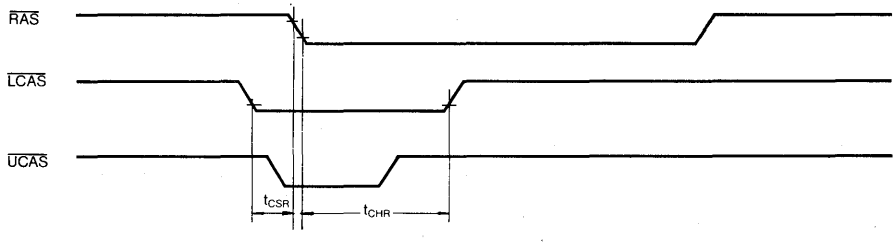
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16	STATE
H	H	H	H	H	HI-Z	HI-Z	Standby
L	H	H	H	H	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

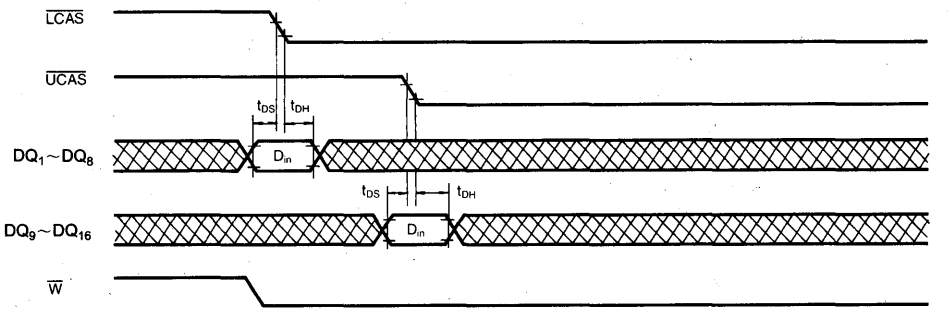
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. 512 cycles of burst refresh must be executed within 8ms before and after self refresh, In order to meet refresh specification.
13. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
14. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
15. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



17. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
18. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

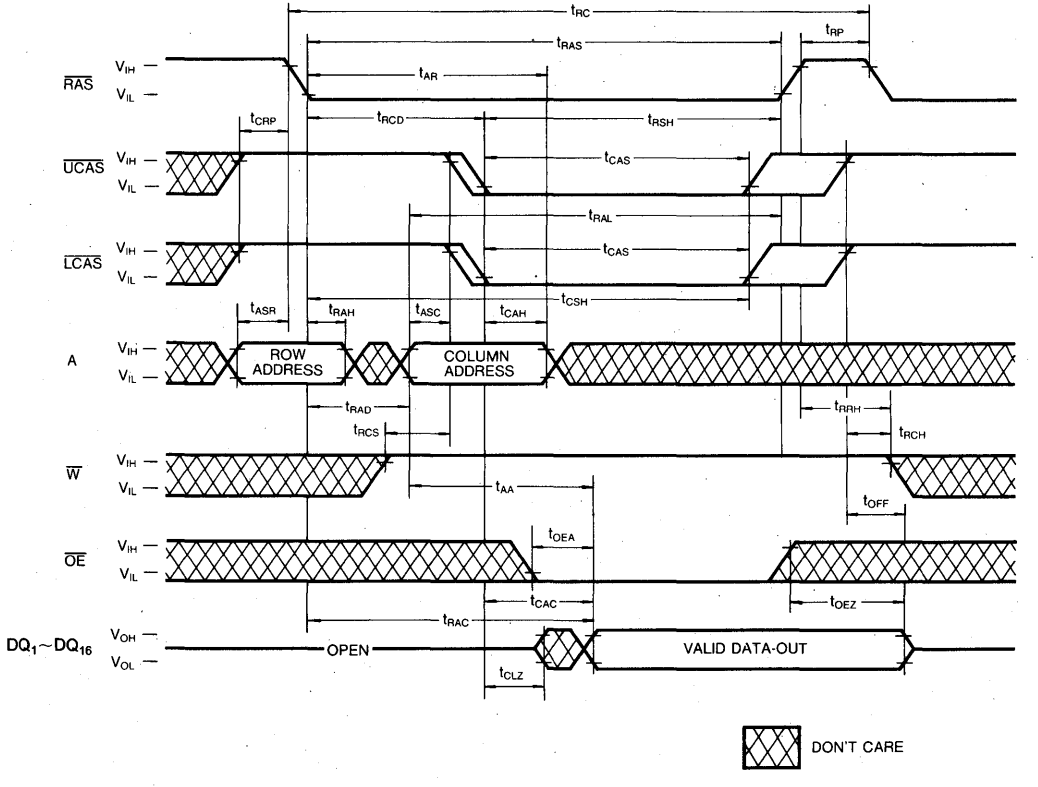


19. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim8)}$, upper byte $D_{in(9\sim16)}$.



TIMING DIAGRAMS

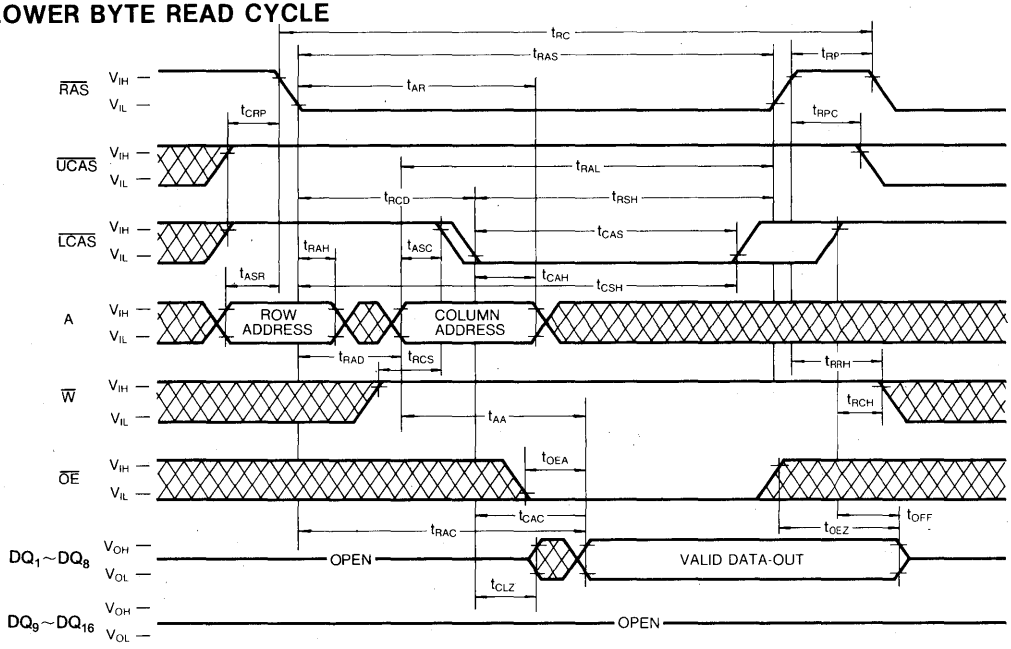
WORD READ CYCLE



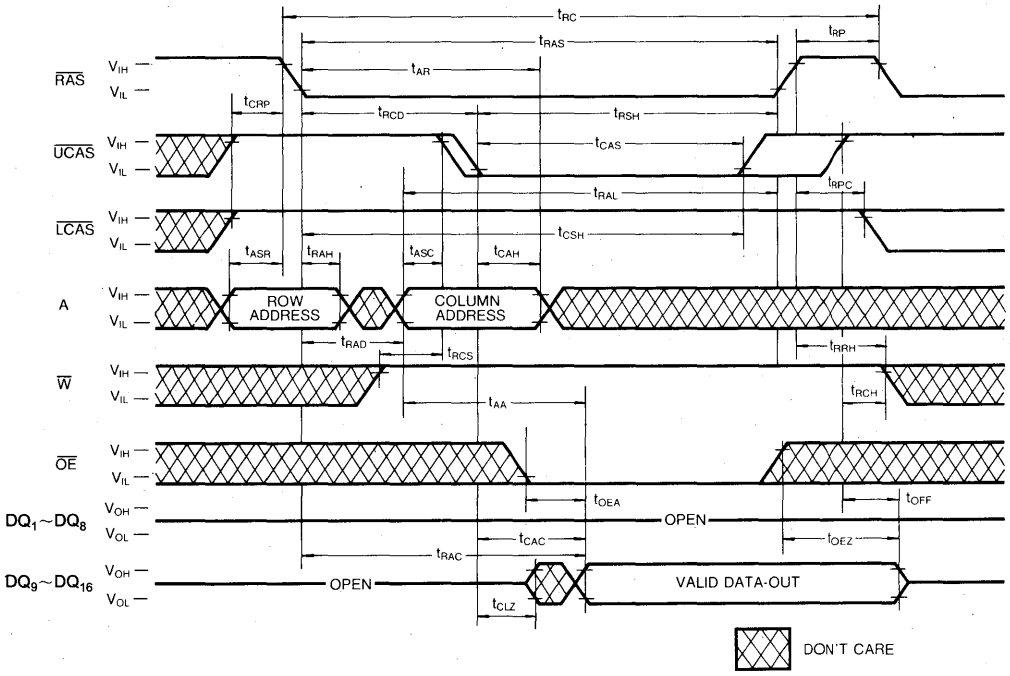
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

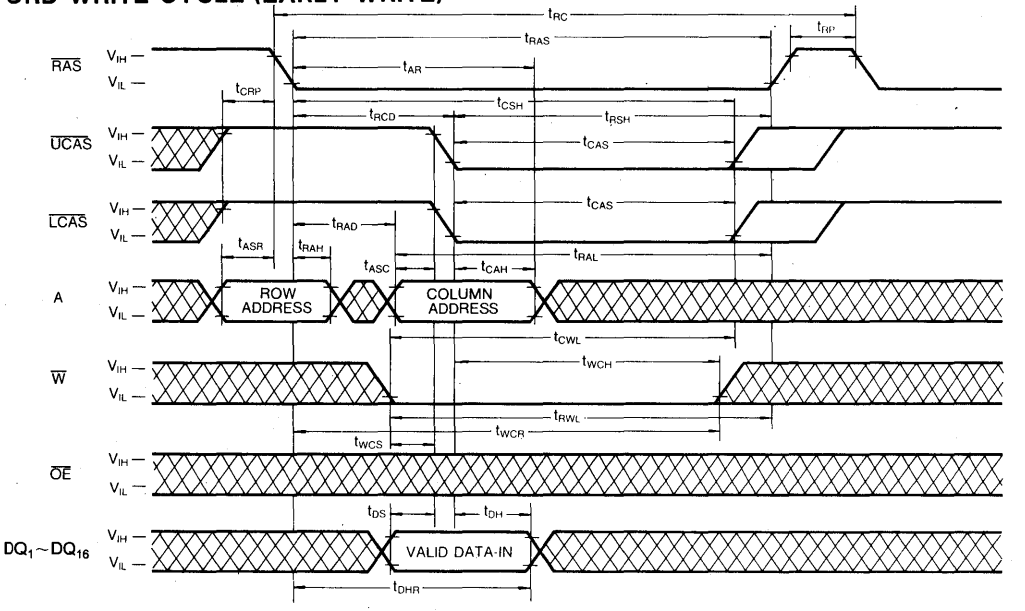


UPPER BYTE READ CYCLE

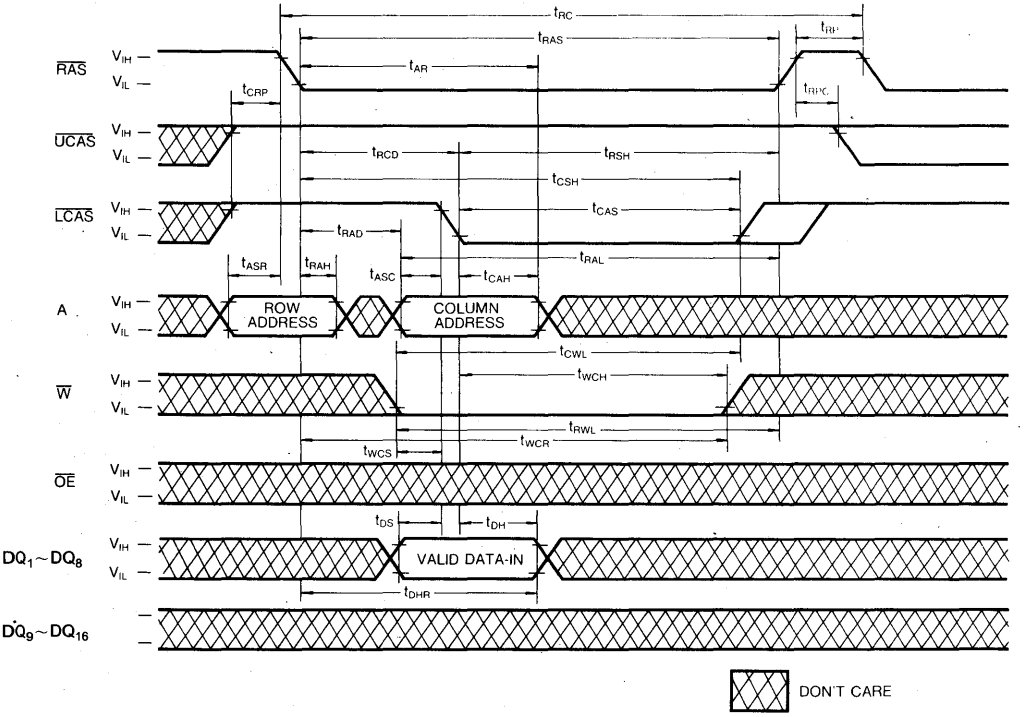


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)

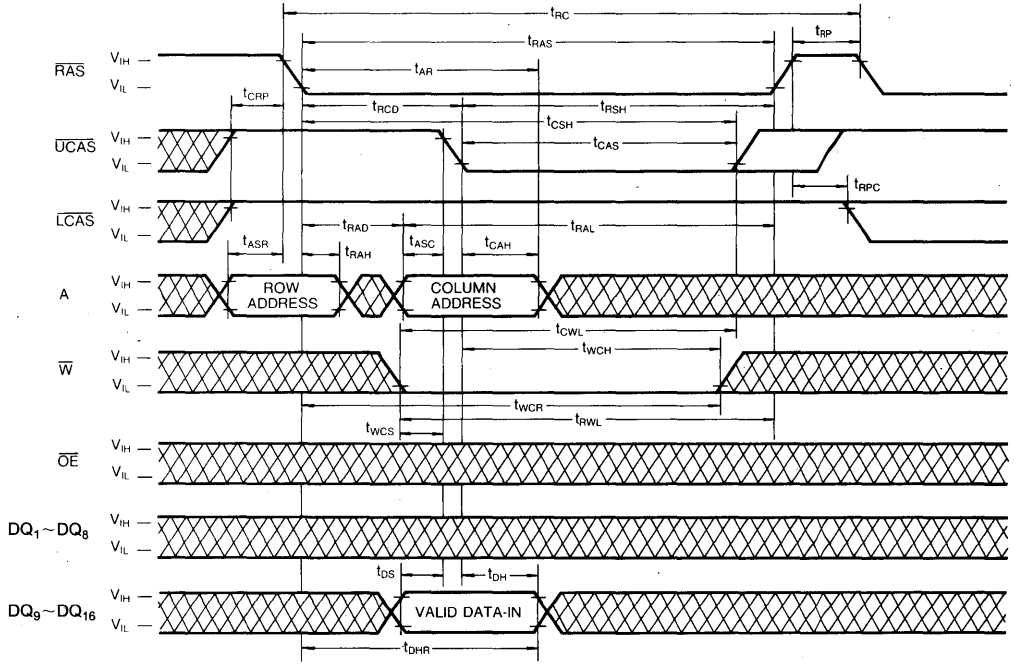


LOWER BYTE WRITE CYCLE (EARLY WRITE)

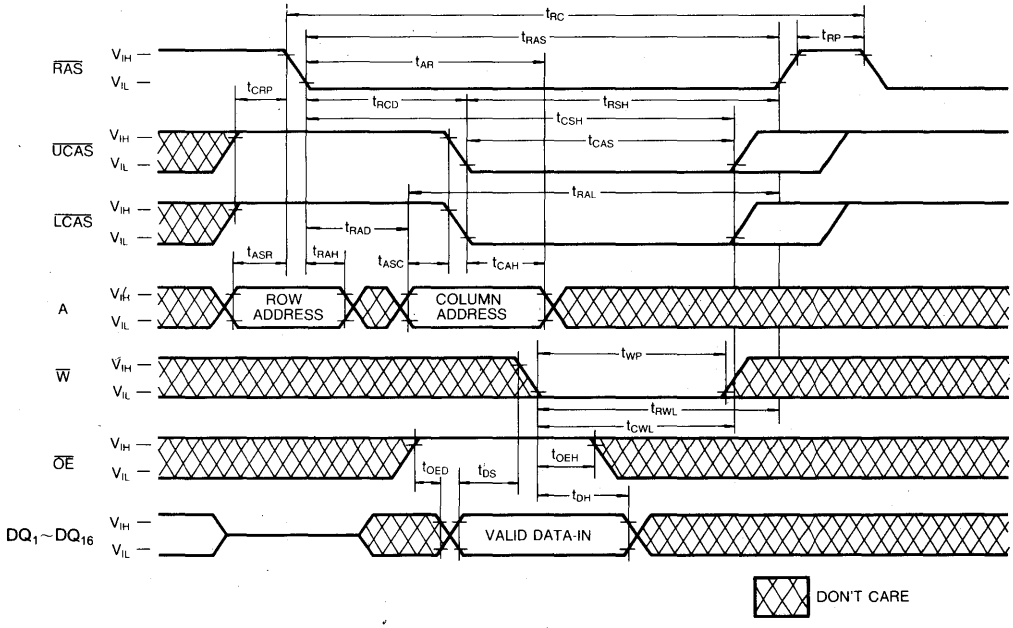


TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

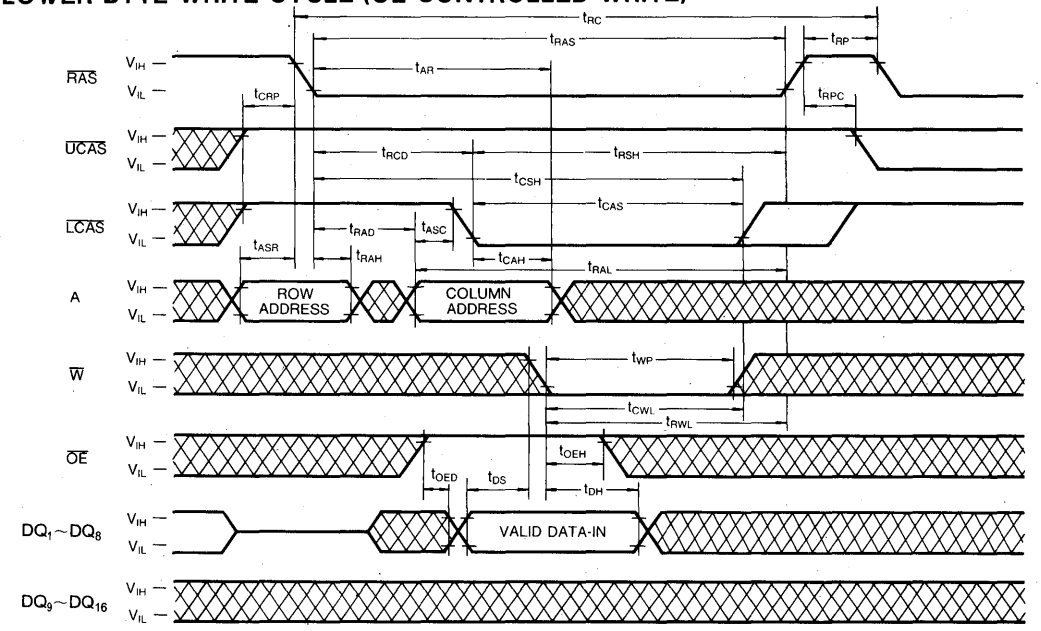


WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

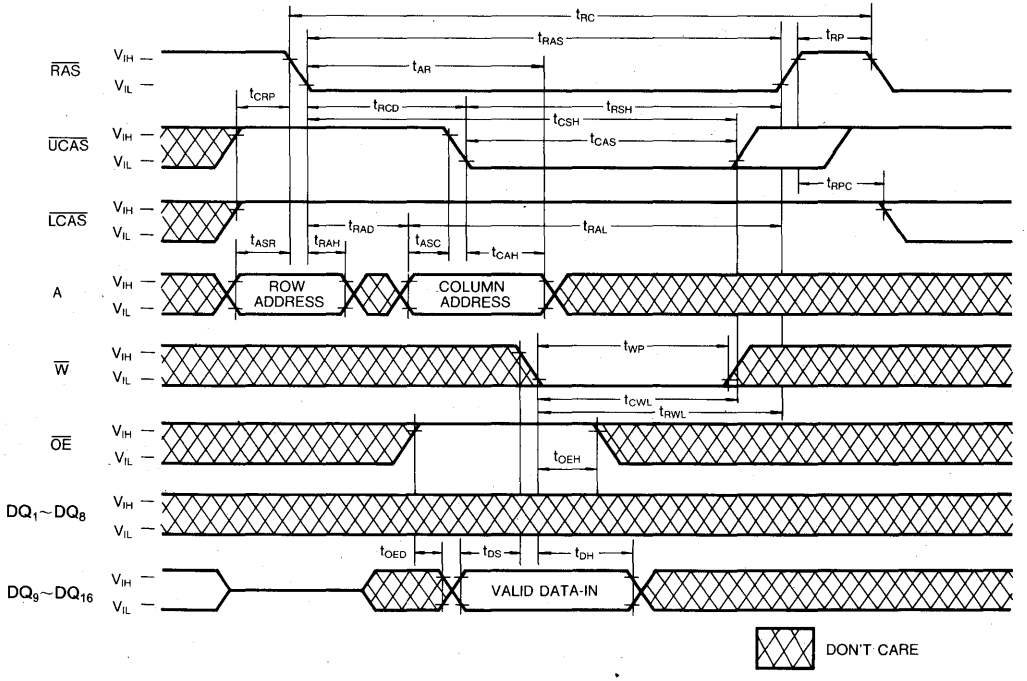


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



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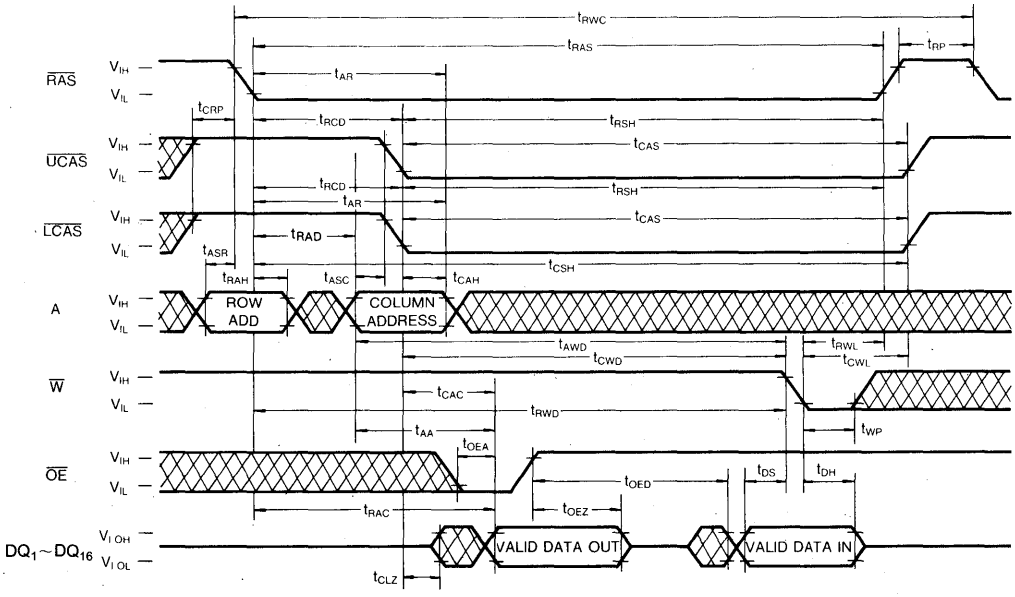
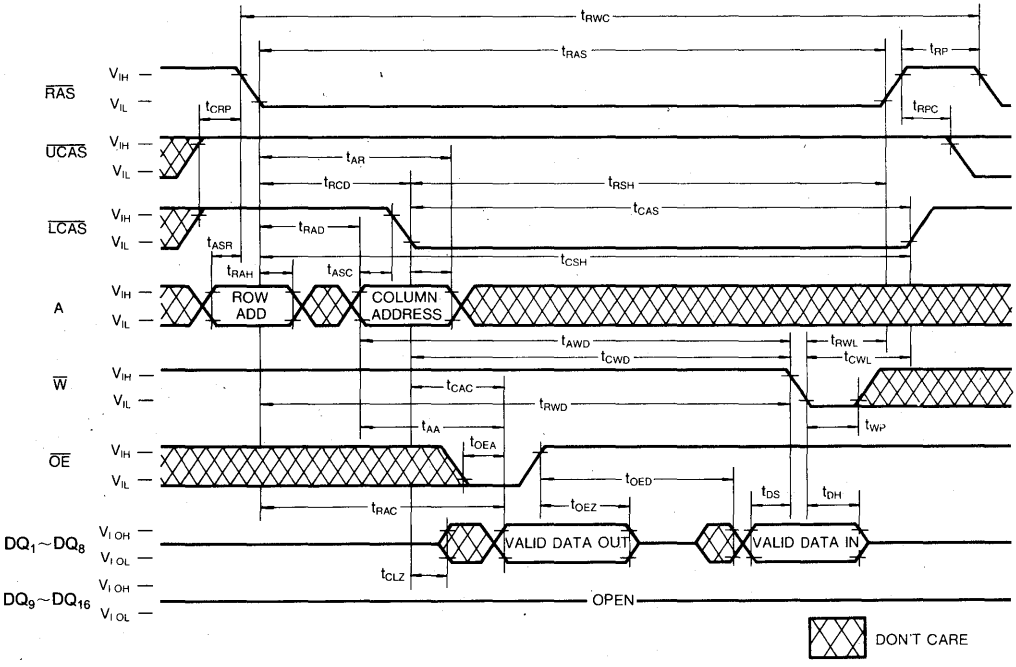
TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

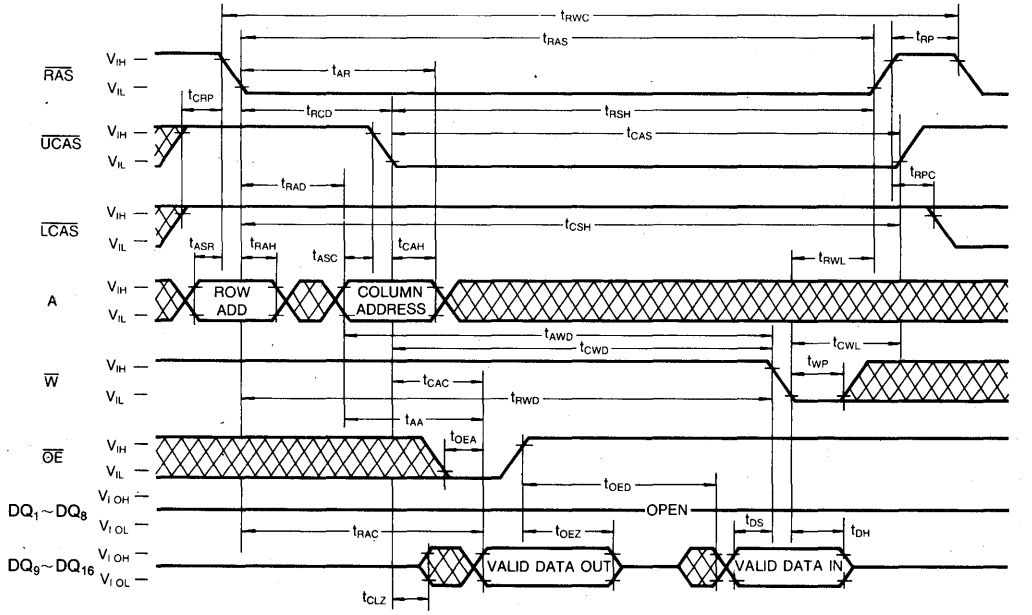


LOWER-BYTE READ-MODIFY-WRITE CYCLE

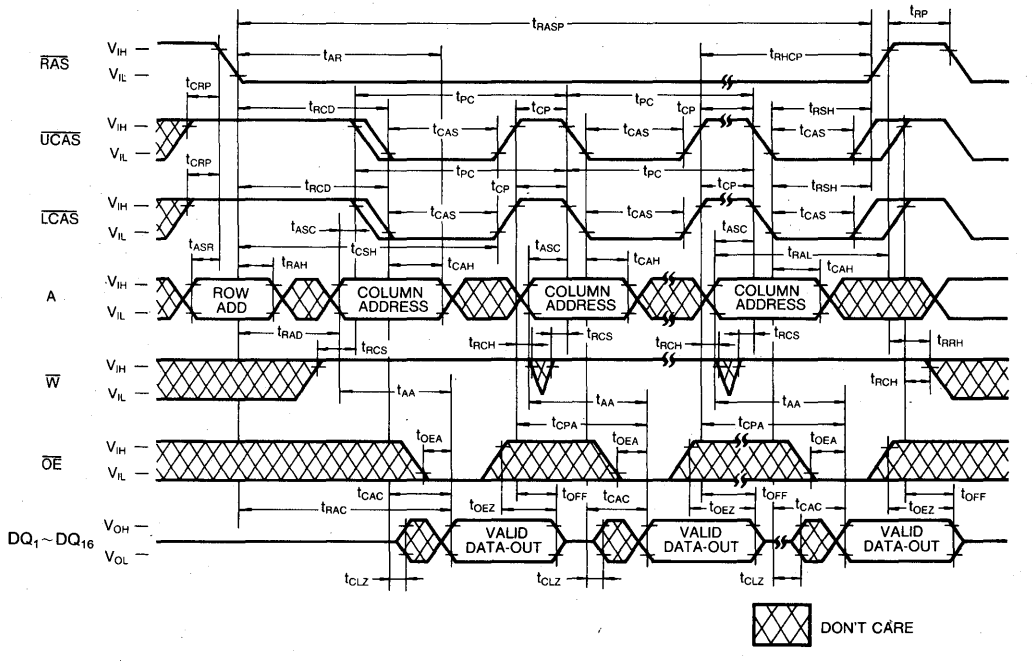


TIMING DIAGRAMS (Continued)

UPPER-BYTE READ-MODIFY-WRITE CYCLE

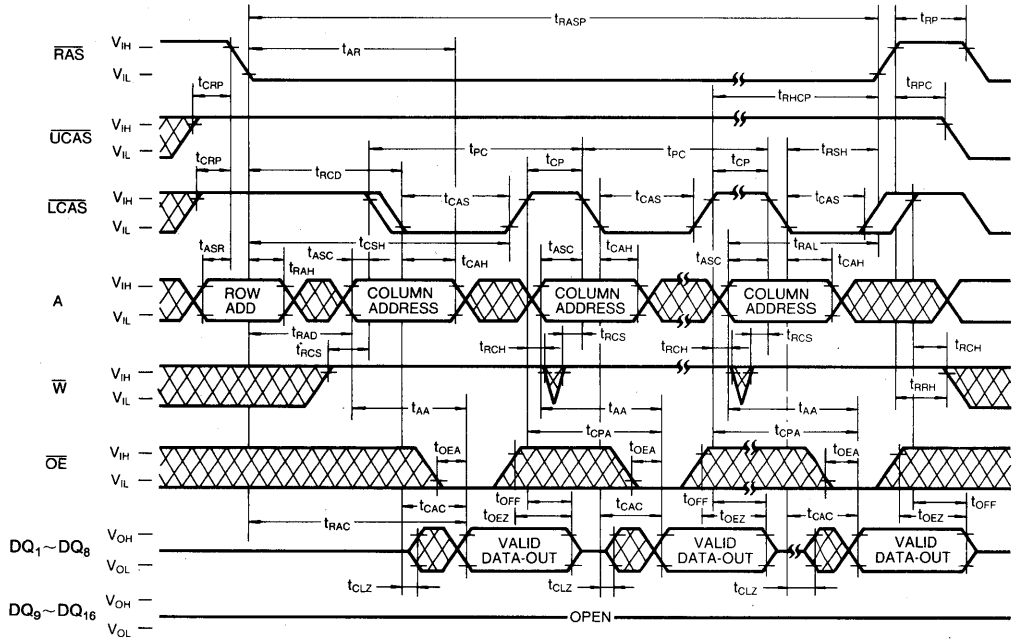


FAST PAGE MODE WORD READ CYCLE

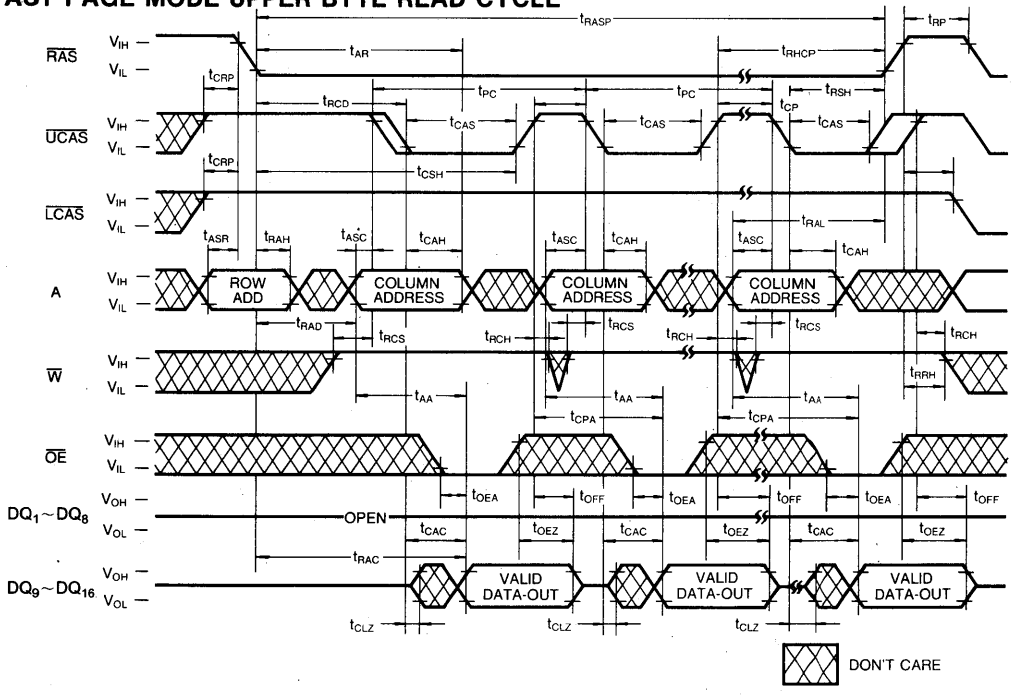


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE

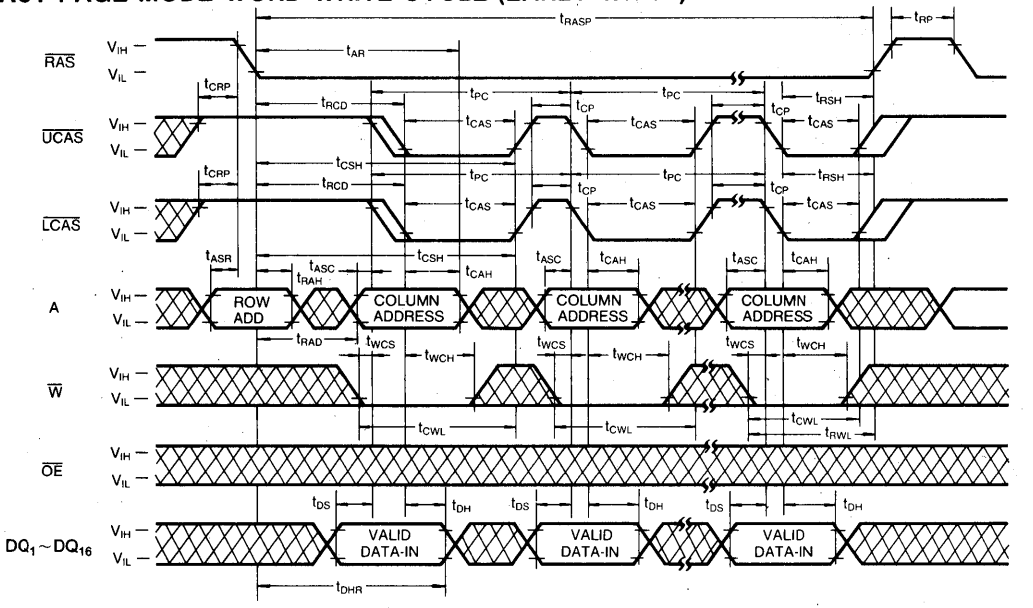


FAST PAGE MODE UPPER BYTE READ CYCLE

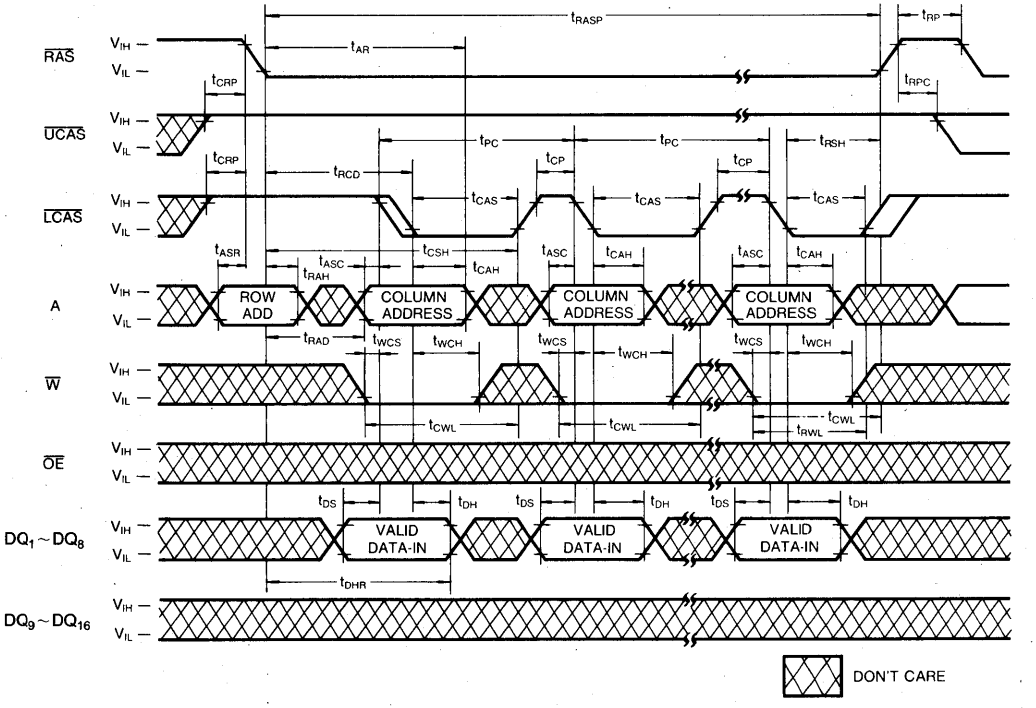


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)



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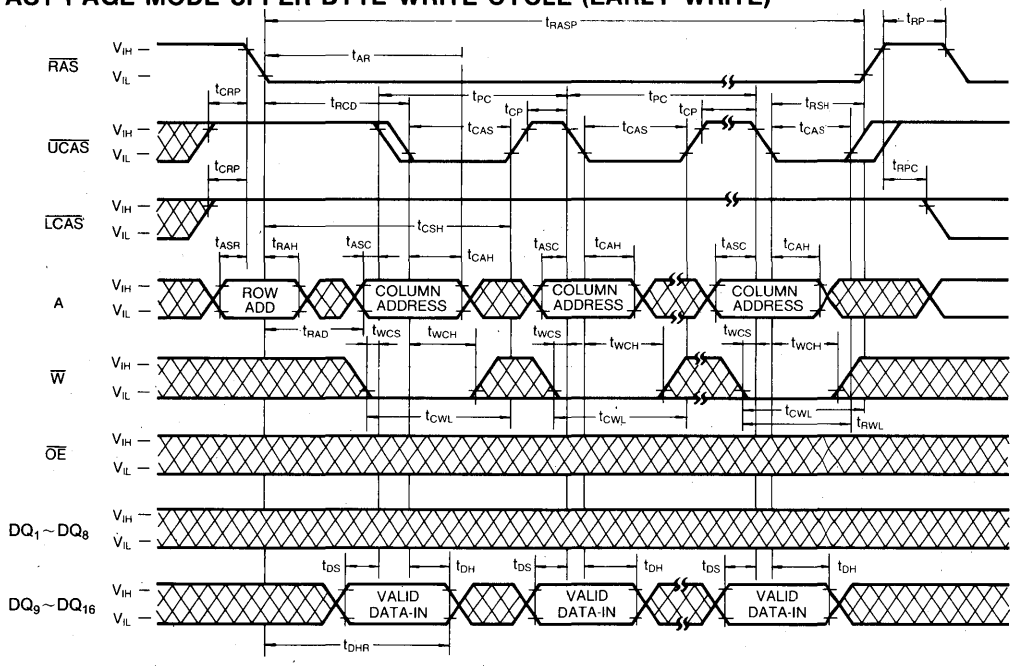
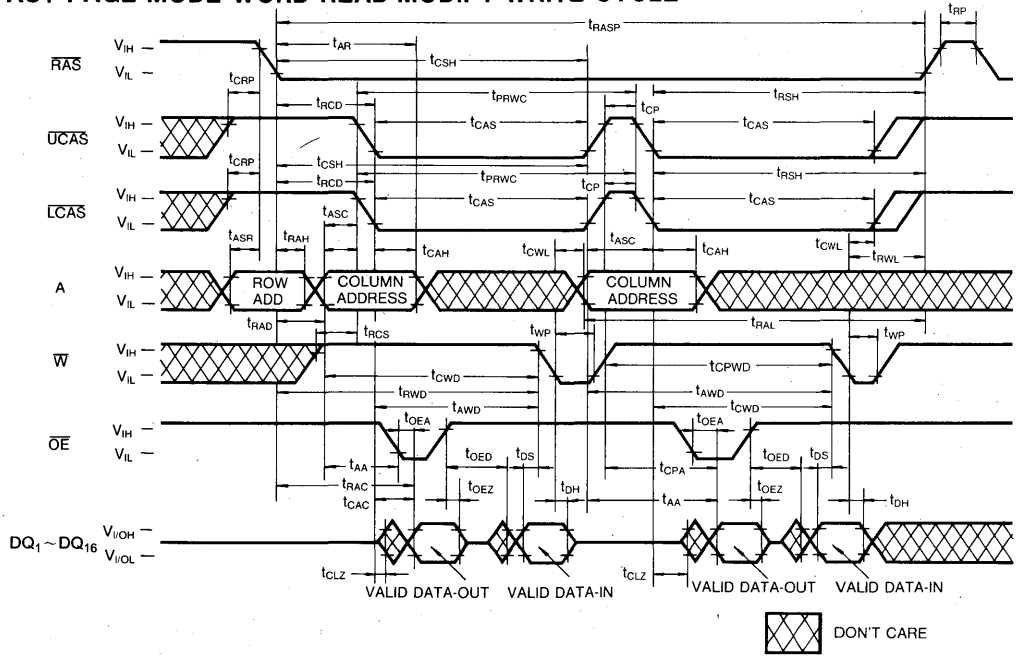
TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)



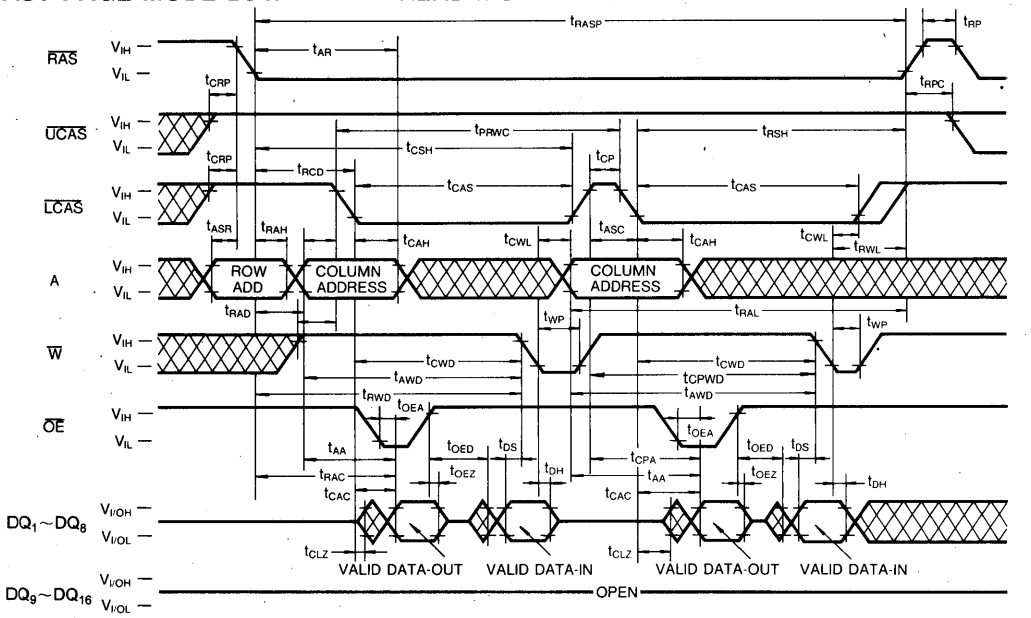
FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE



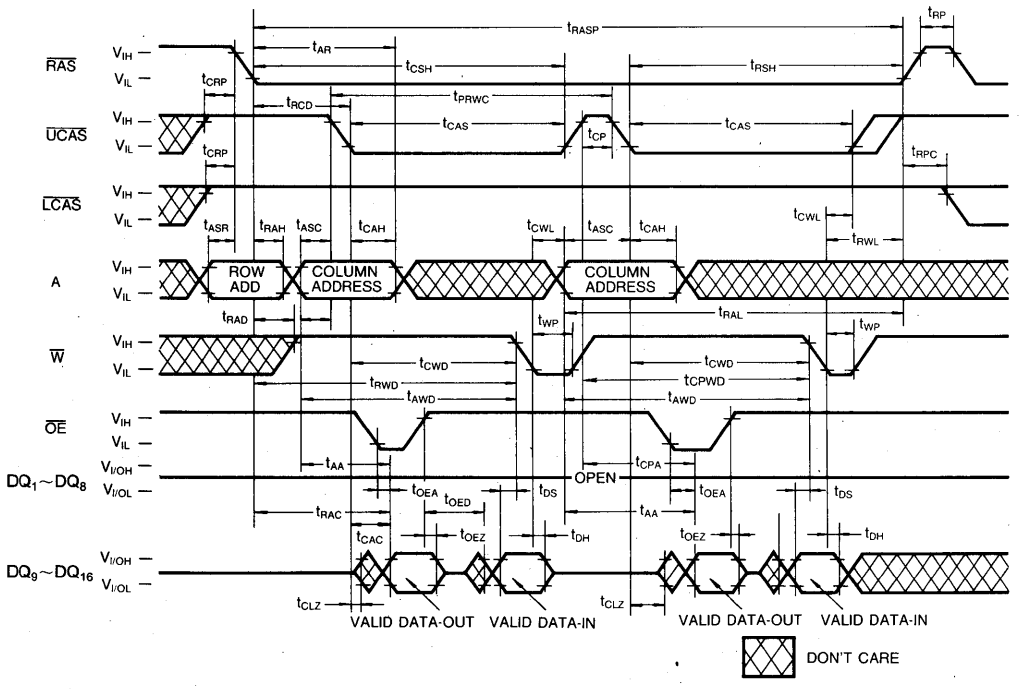
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



FAST PAGE MODE UPPER-BYTE- READ-MODIFY-WRITE CYCLE

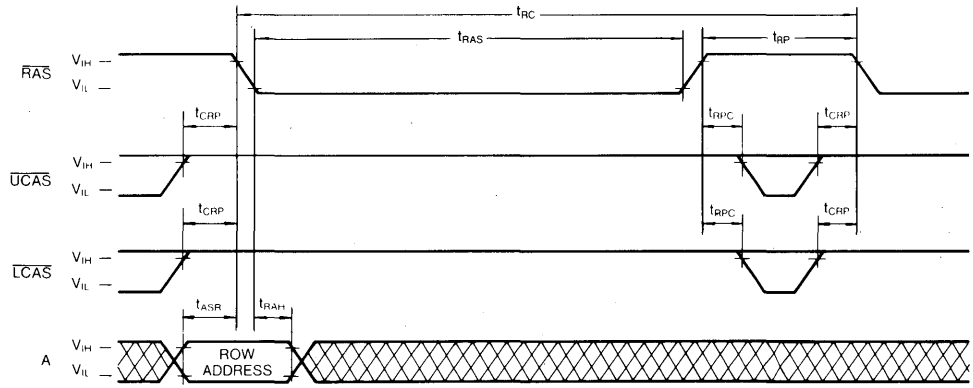


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

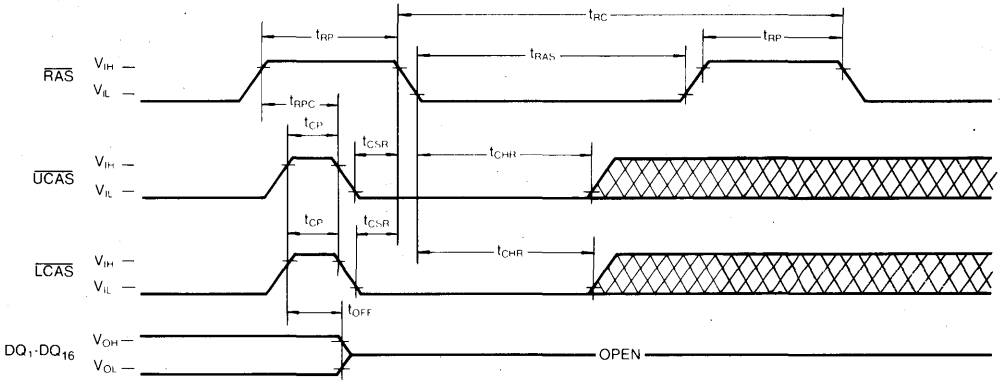
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



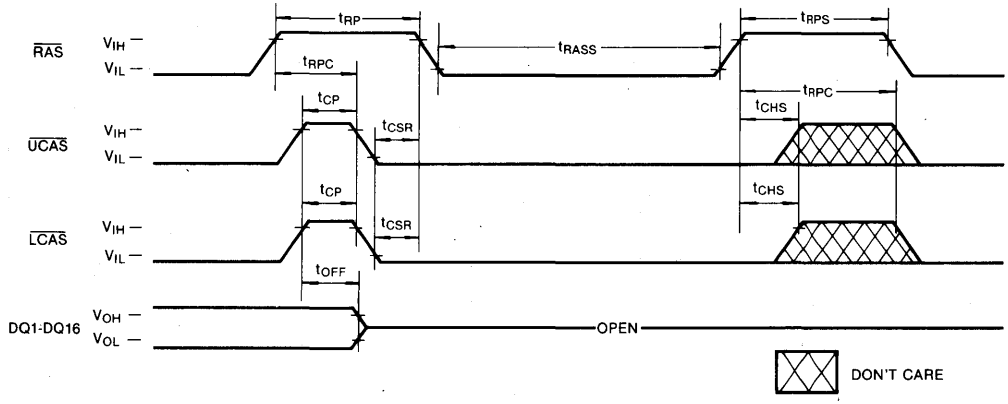
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

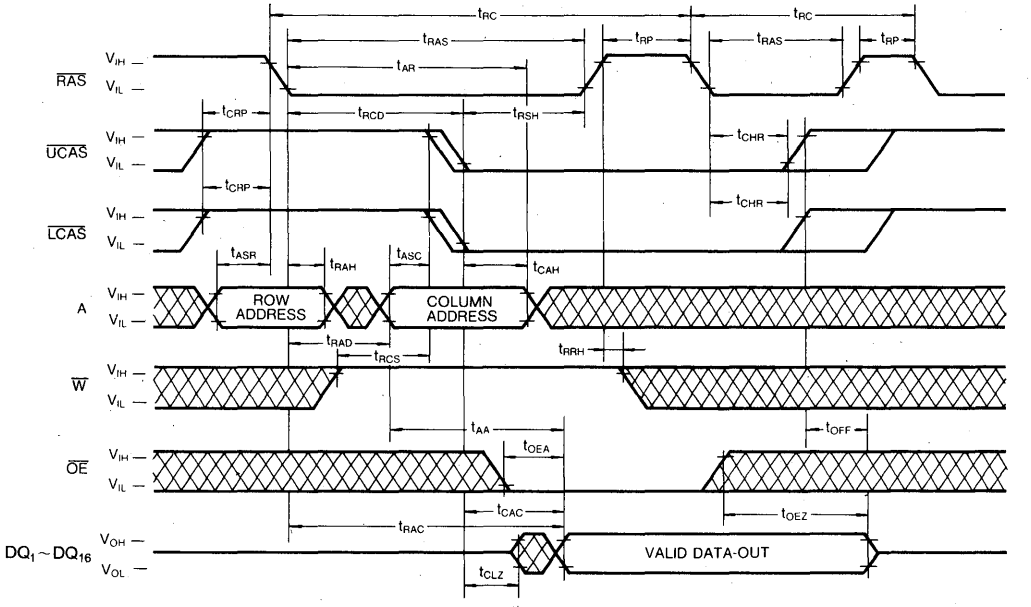
NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care



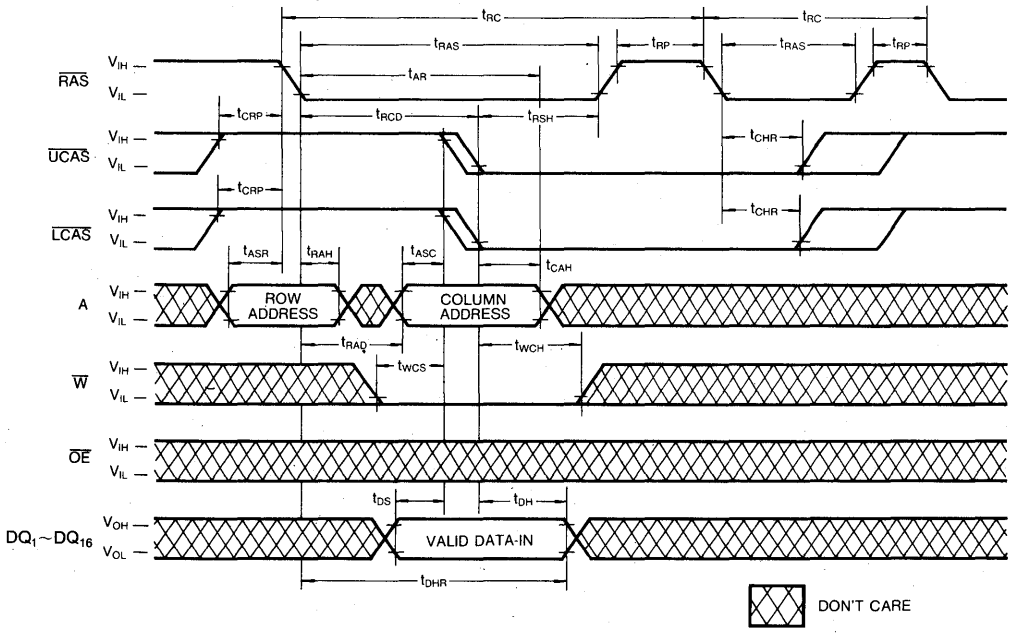
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

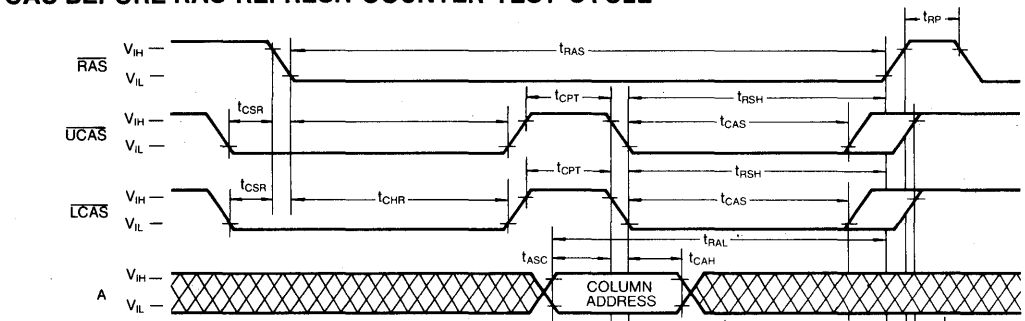


HIDDEN REFRESH CYCLE (WRITE)

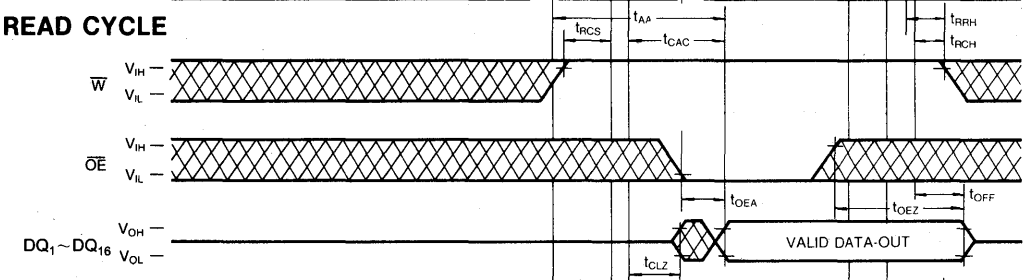


TIMING DIAGRAMS (Continued)

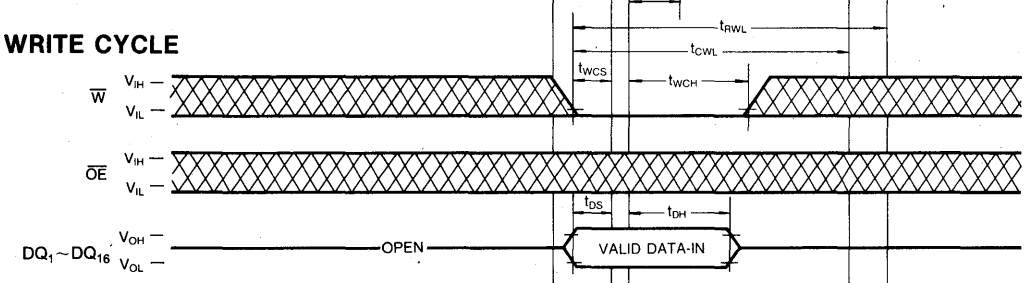
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



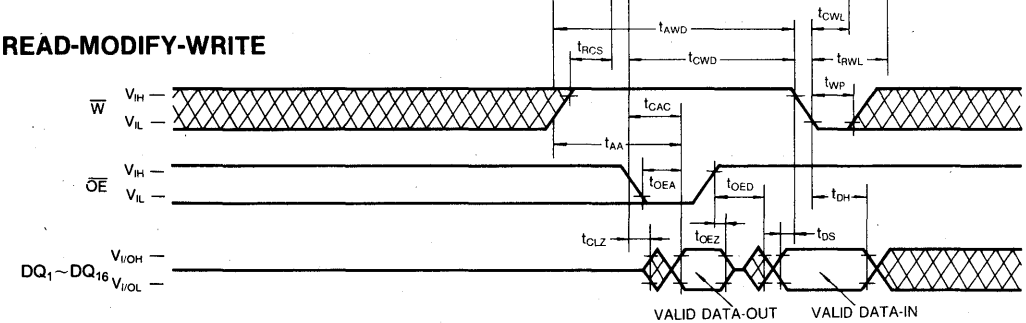
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE

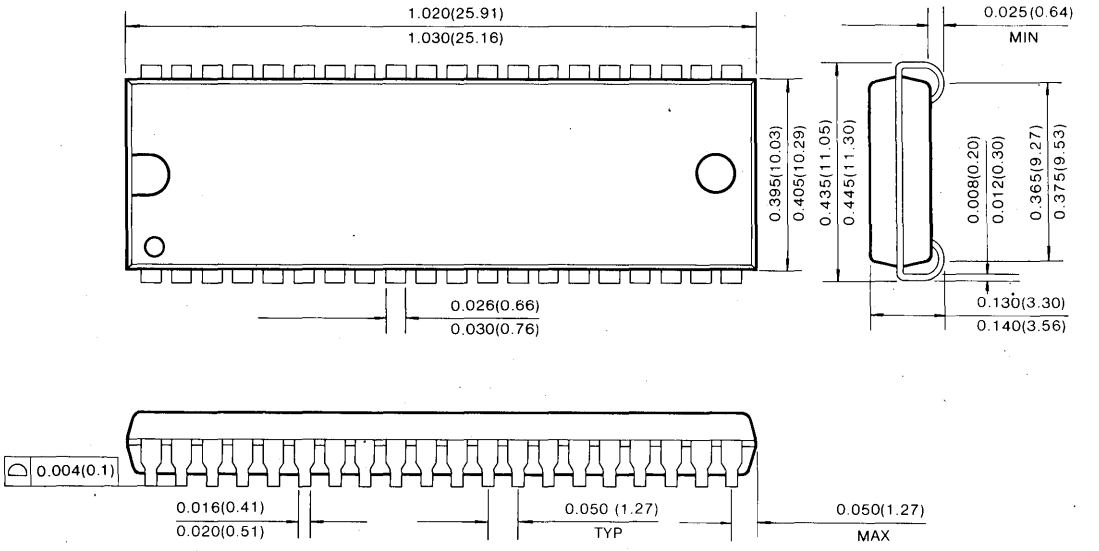


DON'T CARE

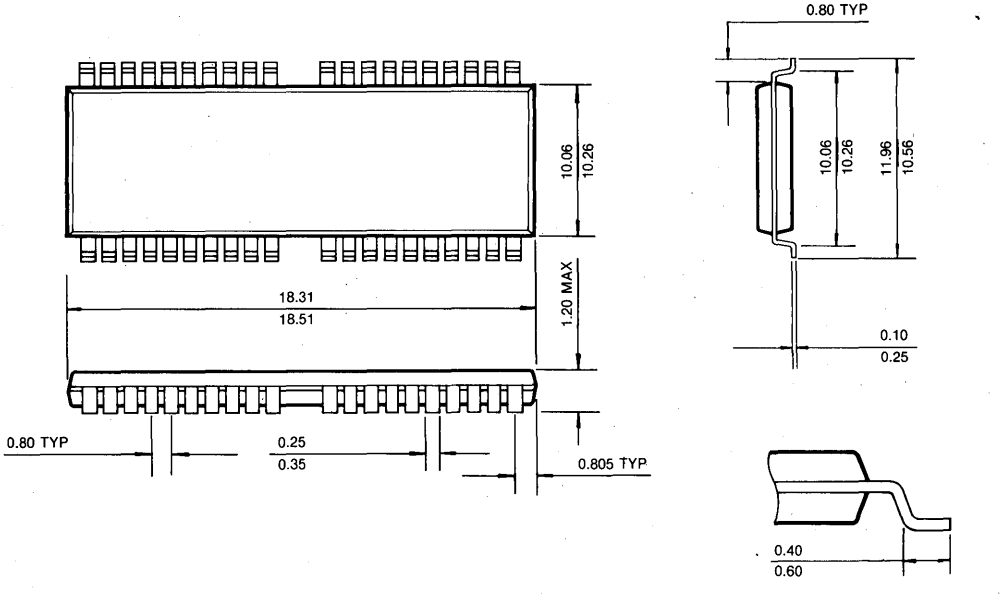
PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)



256K ×16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM416C254B/BL/BLL-5	50ns	17ns	90ns	20ns
KM416C254B/BL/BLL-6	60ns	17ns	110ns	24ns
KM416C254B/BL/BLL-7	70ns	20ns	130ns	29ns

- **Fast Page Mode with Extended Data Out**
- **Byte word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Self Refresh operation (LL-ver)**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +5V±10% power supply**
- **Refresh Cycle**
  -512 cycle/8ms (Normal)
  -512 cycle/64ms (L-version)
  -512 cycle/128ms (LL-version)
- **Power Dissipation**
  -Standby : 5.5mW(Normal)
  1.1mW(L-version)
  0.83mW(LL-version)
  -Active (50/60/70): 605/495/440 mW
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP II**

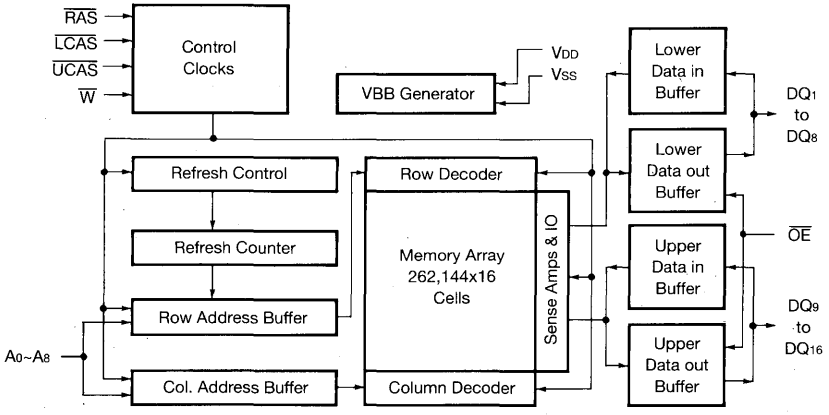
GENERAL DESCRIPTION

The Samsung KM416C254B/BL/BLL is a CMOS high speed 262,144 bit × 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM416C254B/BL/BLL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

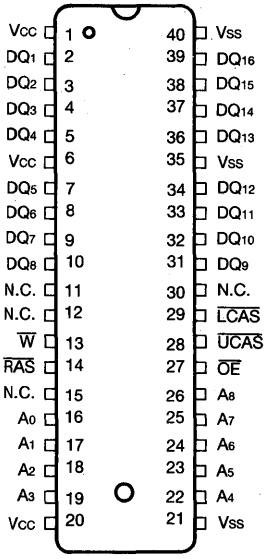
The KM416C254B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

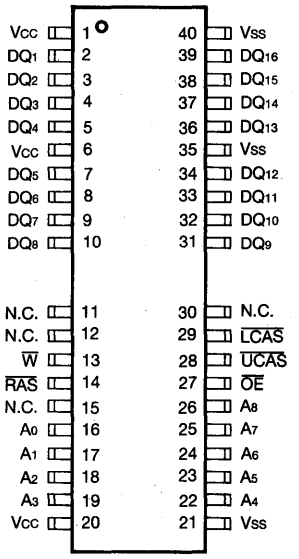


PIN CONFIGURATION (Top Views)

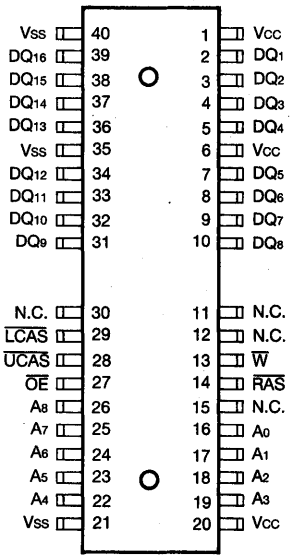
• KM416C254BJ/BLJ/BLLJ



• KM416C254BT/BLT/BLLT



• KM416C254BTR/BLTR/BLLTR



Pin Name	Pin Function
A0-A8	Address Inputs
DQ1~16	Data In/Out
VSS	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VCC	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1~+7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1~+7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	KM416C254B/BL/BLL-5 KM416C254B/BL/BLL-6 KM416C254B/BL/BLL-7	I_{CC1}	-	110 90 80	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM416C254B/BL/BLL-5 KM416C254B/BL/BLL-6 KM416C254B/BL/BLL-7	I_{CC3}	-	110 90 80	mA mA mA
Hyper page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$=$\overline{LCAS}$, Address Cycling @t_{PC}=min.)	KM416C254B/BL/BLL-5 KM416C254B/BL/BLL-6 KM416C254B/BL/BLL-7	I_{CC4}	-	70 60 55	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)	KM416C254B KM416C254BL KM416C254BLL	I_{CC5}	-	1 200 150	mA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{UCAS}$=$\overline{LCAS}$ Cycling @t_{RC}=min.)	KM416C254B/BL/BLL-5 KM416C254B/BL/BLL-6 KM416C254B/BL/BLL-7	I_{CC6}	-	110 90 80	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{UCAS}$=$\overline{LCAS}$= 0.2V D_{IN}=Don't Care, T_{RC}=125μS T_{RAS}=T_{RAS} min.~300ns	KM416C254BL	I_{CC7}	-	300	μA
Self Refresh Current $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_8=V_{CC}-0.2V or 0.2V DQ_1-DQ_{16}=V_{CC}-0.2V, 0.2V or Open	KM416C254BLL	I_{CC8}	-	200	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}+0.5V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_8)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5V±10%, See notes 1,2)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, Output loading C_L=100pF

Parameter	Symbol	-5(*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		ns	
Read-modify-write cycle time	t_{RWC}	135		155		185		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		17		17		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	3	20	ns	7,14
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	17		17		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	40		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10,000	10	10,000	15	10,000	ns	12
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	

(*) -50ns Product : Output Loading (C_L)=50pF, V_{CC}=5V ± 5%

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	8		10		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		50		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		10		15		ns	10
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		ns	6
Refresh period (Normal)	tREF		8		8		8	ms	
Refresh period (L-version)	tREF		64		64		64	ms	
Refresh Period(LL-version)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		42		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		95		ns	8
Column address to $\overline{W}$ delay time	tAWD	48		55		60		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		65		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		25		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	3
Hyper Page mode cycle time	tHPC	20		24		29		ns	12
Hyper Page mode read-modity-write cycle time	tHPRWC	62		71		81		ns	12
$\overline{CAS}$ precharge time (Hyper Page mode)	tCP	8		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page mode)	tRASP	50	100K	60	100K	70	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		15		15		20	ns	
$\overline{OE}$ to Output in Low-z	tOLZ	3		3		3		ns	
$\overline{OE}$ to data delay	tOED	13		15		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	ns	7

(*) -50ns Product : Output Loading (C_L)=50pF, V_{CC}=5V ± 5%

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{OE}$ commend hold time	tOEH	13		15		20		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	ns	7,14
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	ns	7
$\overline{W}$ to data delay	tWED	13		15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width(LL-ver)	tRASS	100		100		100		μs	13
$\overline{RAS}$ precharge time (LL-ver)	tRPS	90		110		130		ns	13
$\overline{CAS}$ hold time (LL-ver)	tCHS	-50		-50		-50		ns	13

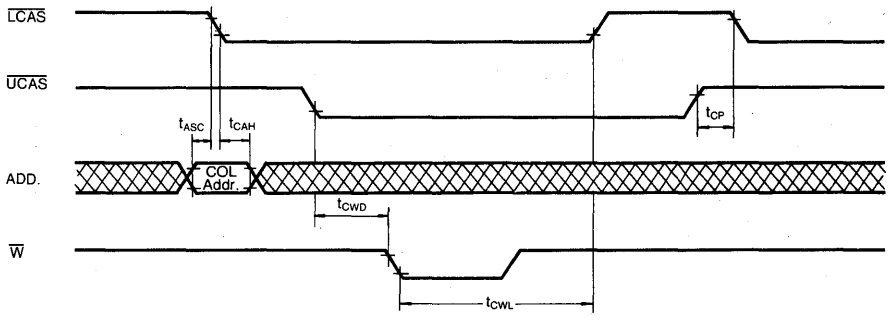
(*) -50ns Product : Output Loading (C_L)=50pF, V_{CC}=5V $\pm$ 5%

KM416C254B/BL/BLL Truth Table

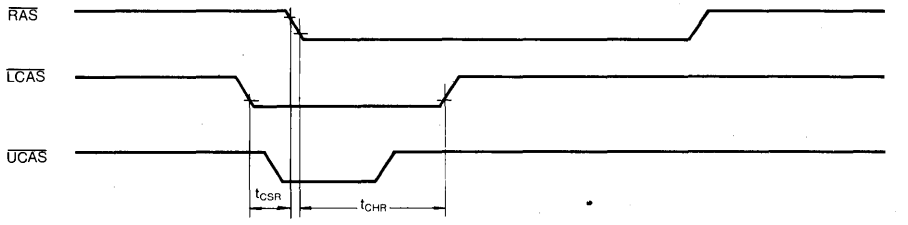
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ_1~DQ_8	DQ_9~DQ_{16}	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

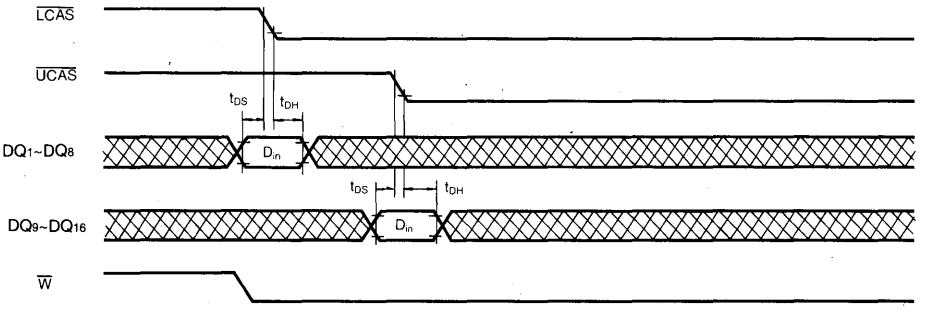
1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs except t_{HPC} and t_{HPRWC}.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. $t_{ASC} \geq t_{CP}$ min, Assume tT=2.0 ns
13. 512 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (LL-Ver)
14. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
16. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
17. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
18. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



19. t_{CSR} is refernced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
20. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low



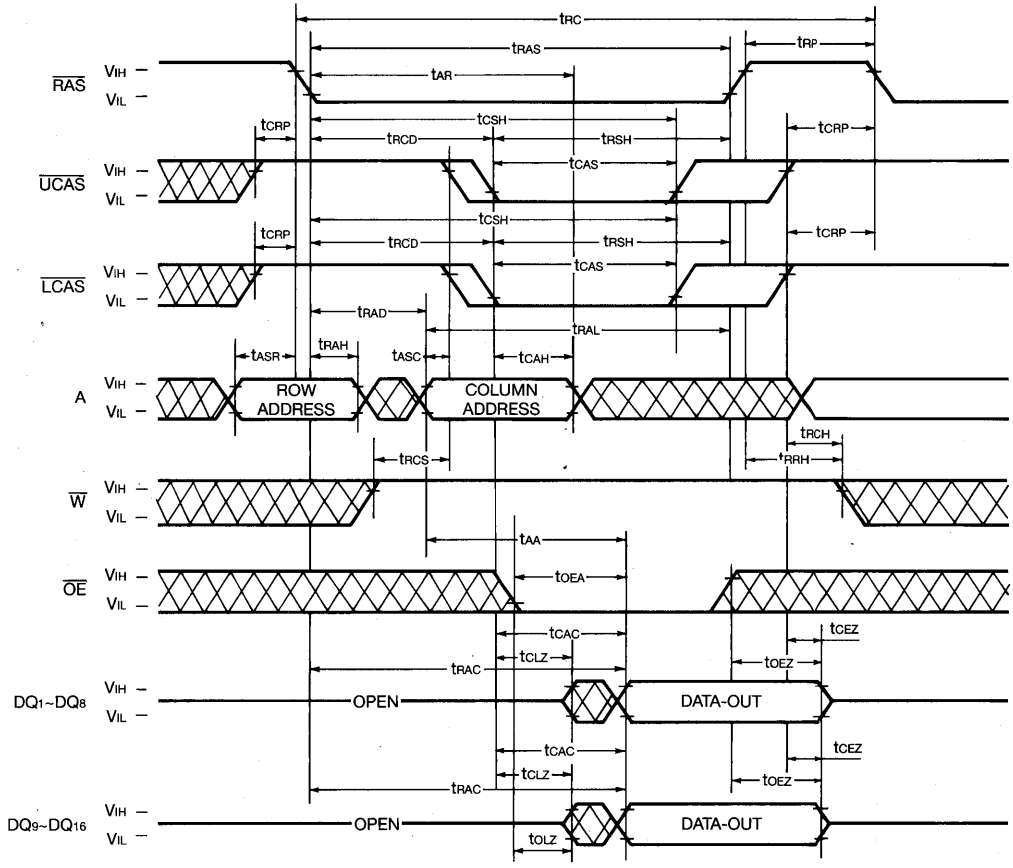
21. t_{DS}, t_{DH}, is independently specified for lower byte $D_{IN(1-8)}$, upper byte $D_{in(9\sim16)}$.



TIMING DIAGRAM

WORD READ CYCLE

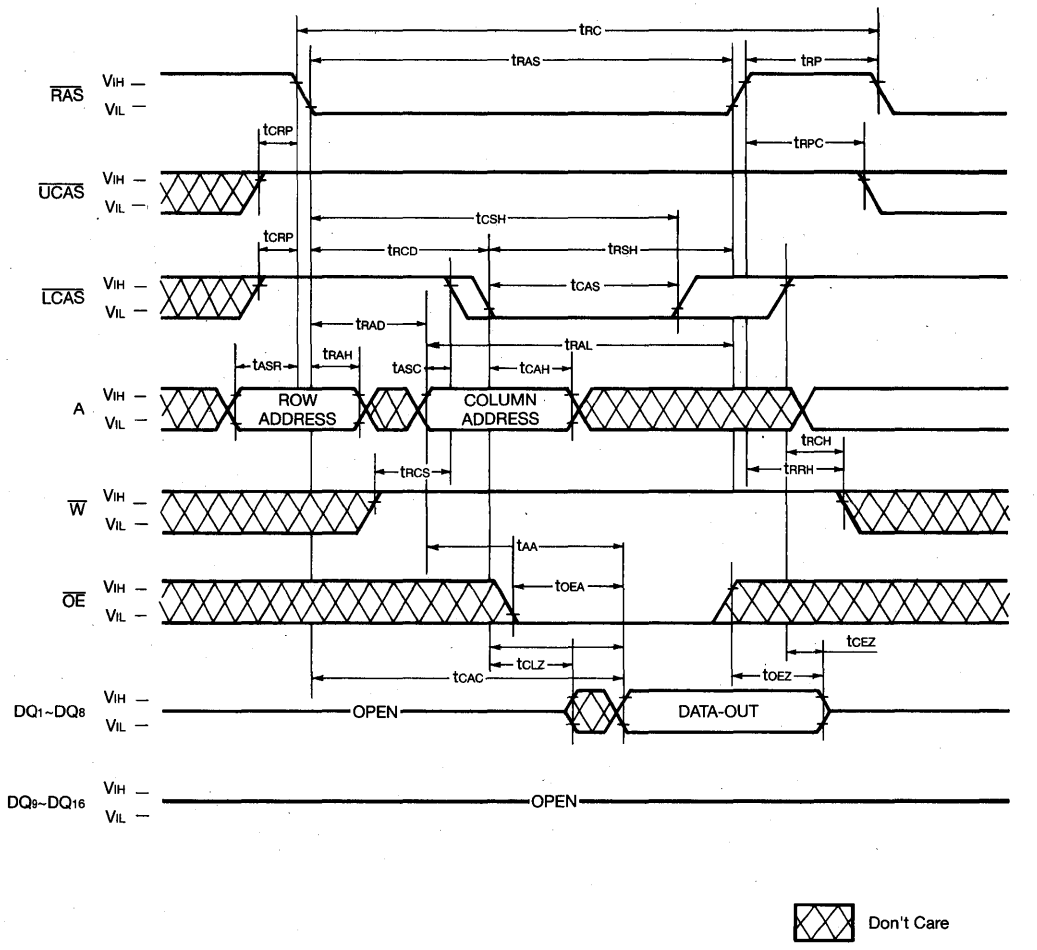
NOTE : DIN=OPEN



TIMING DIAGRAM

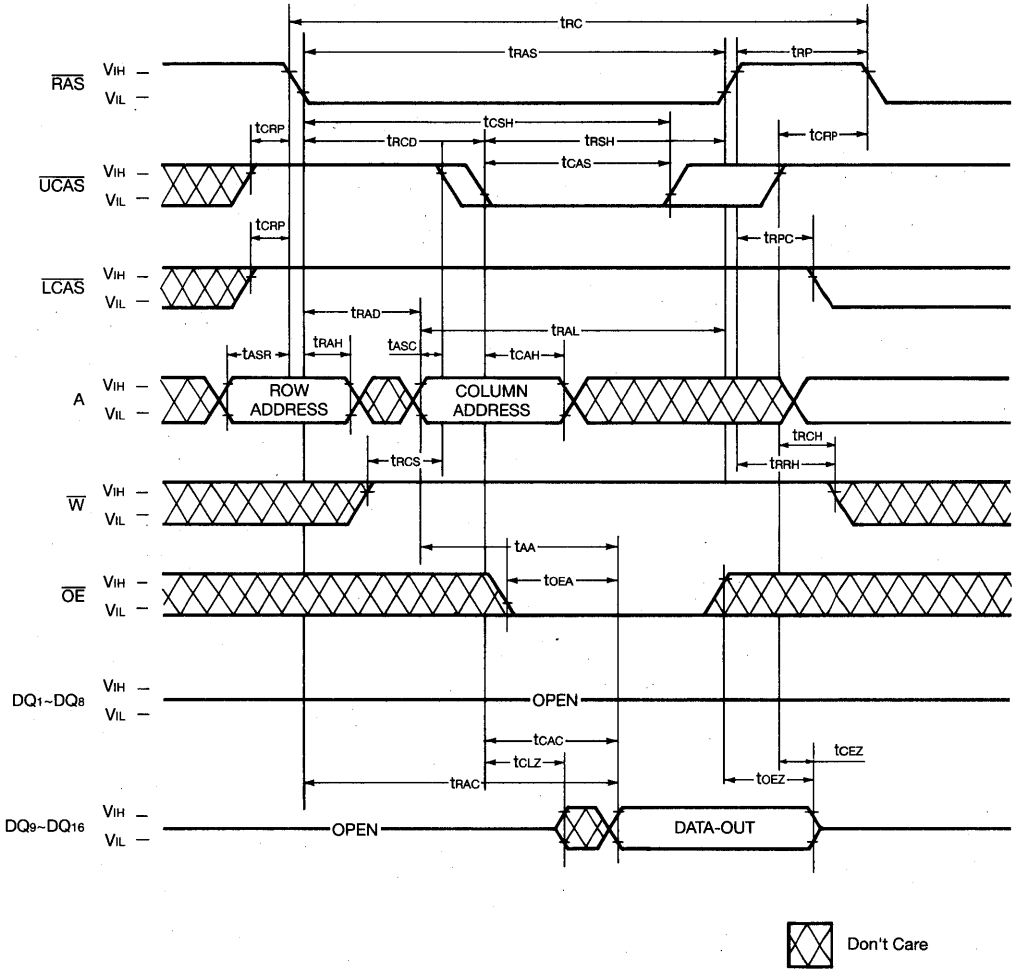
LOWER BYTE READ CYCLE

NOTE : D_{IN}=OPEN



UPPER BYTE READ CYCLE

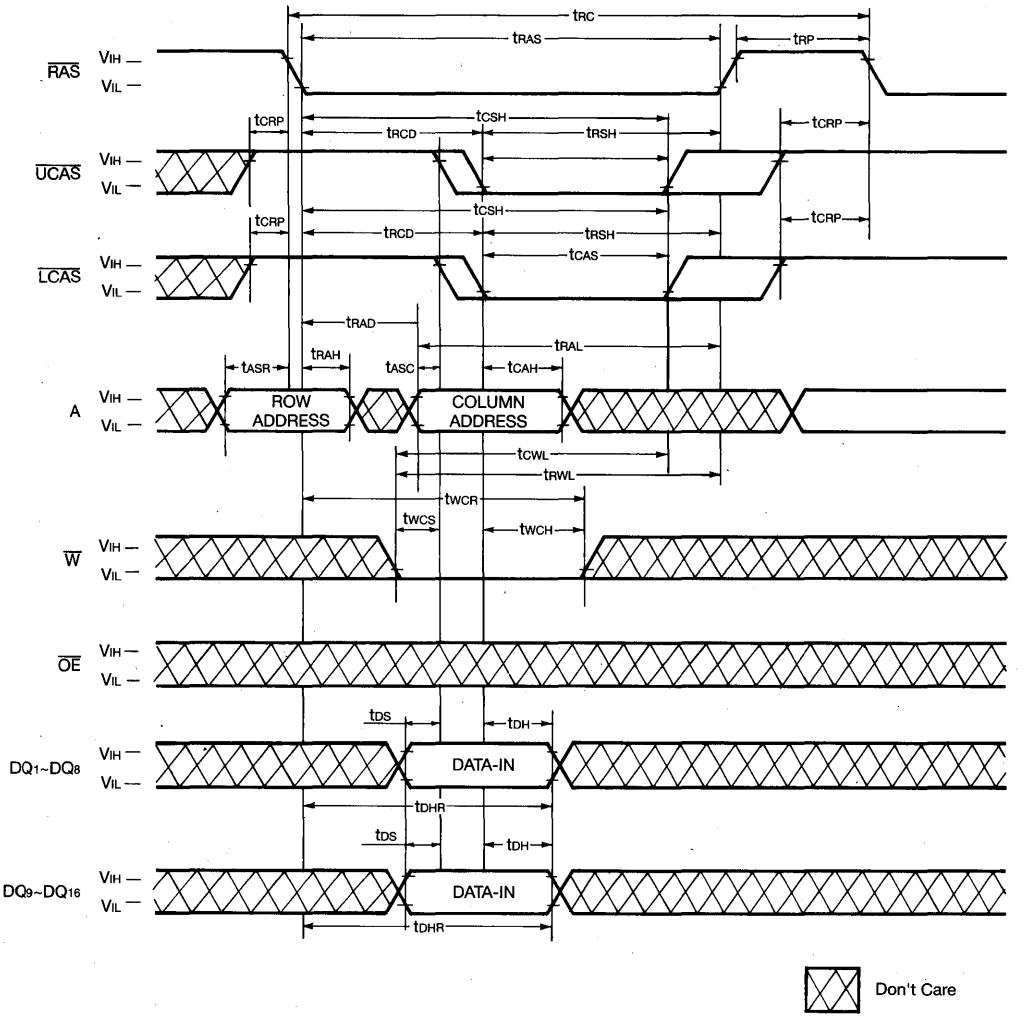
NOTE : D_{IN}=OPEN



SAMSUNG ELECTRONICS

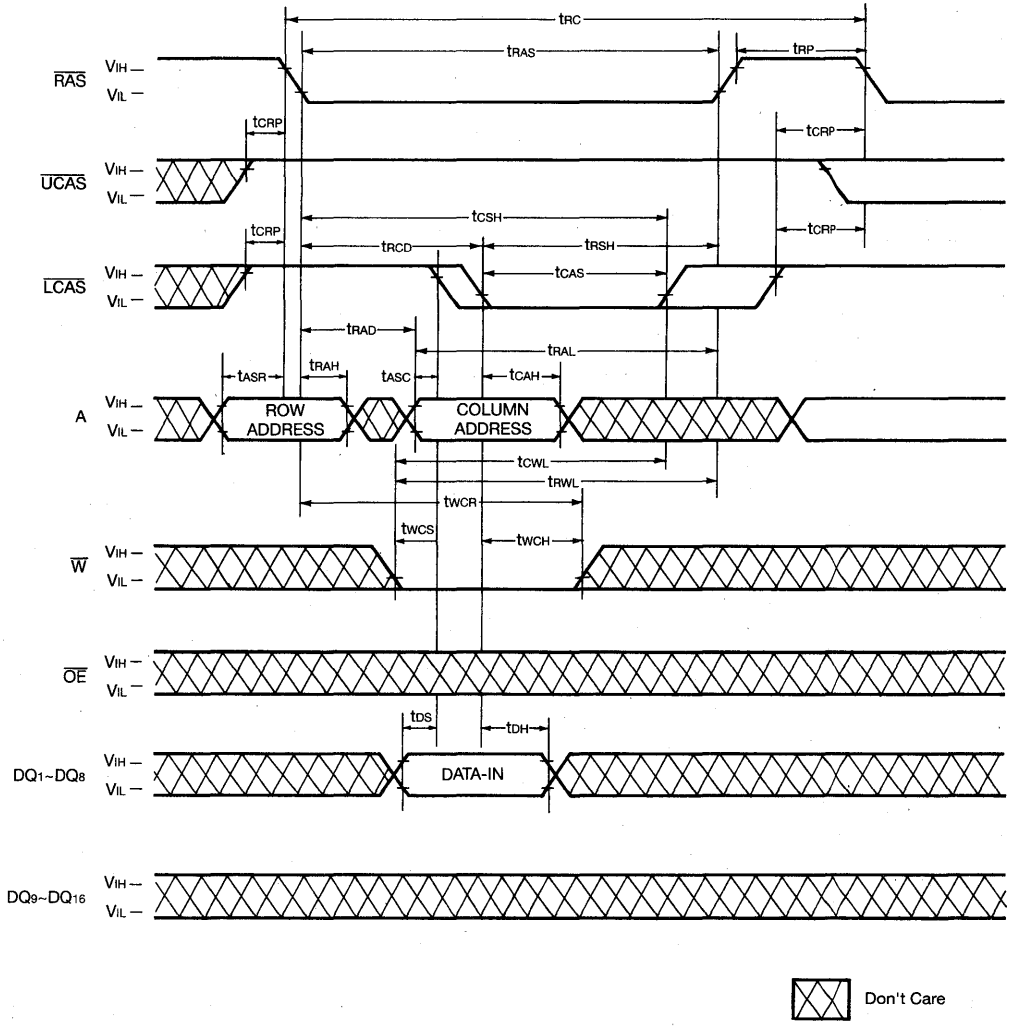
WORD WRITE CYCLE (EARLY WRITE)

NOTE : DOUT=OPEN



LOWER BYTE WRITE CYCLE (EARLY WRITE)

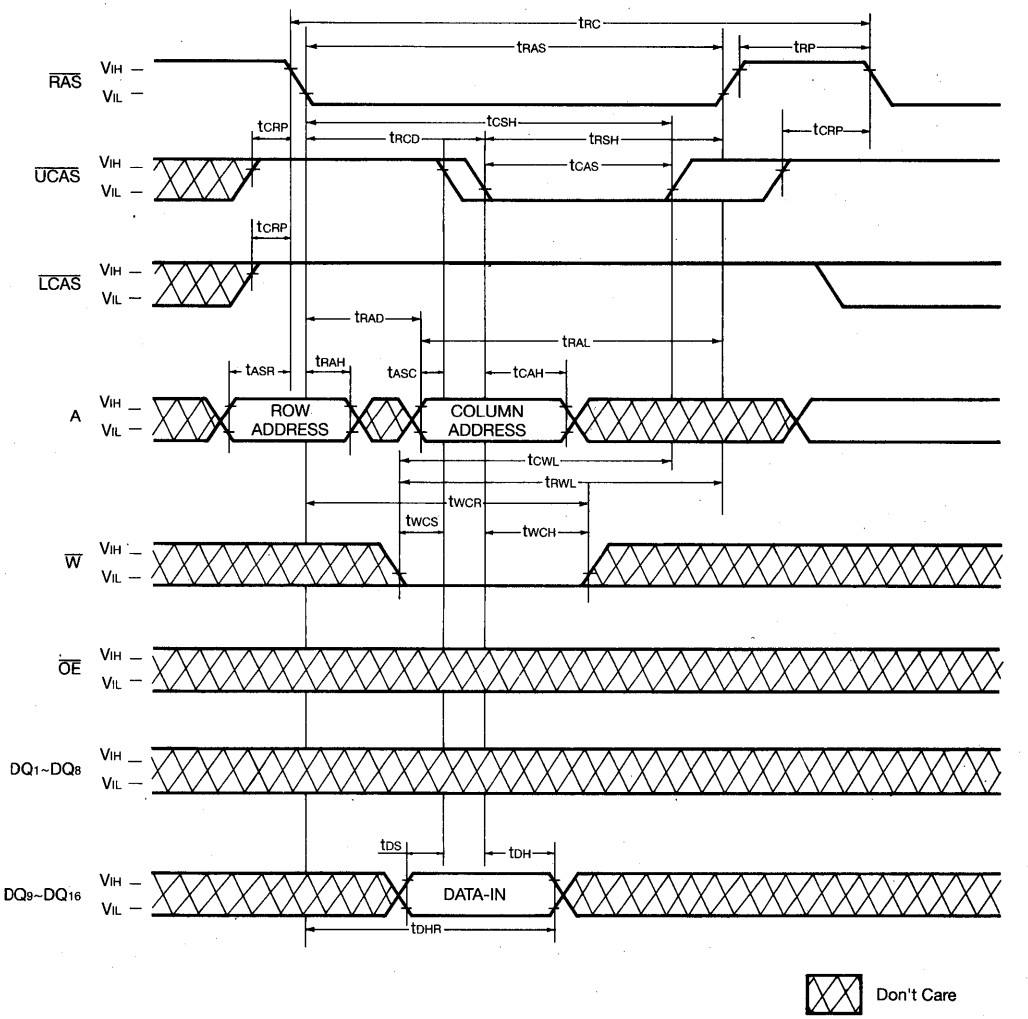
NOTE : DOUT=OPEN



SAMSUNG ELECTRONICS

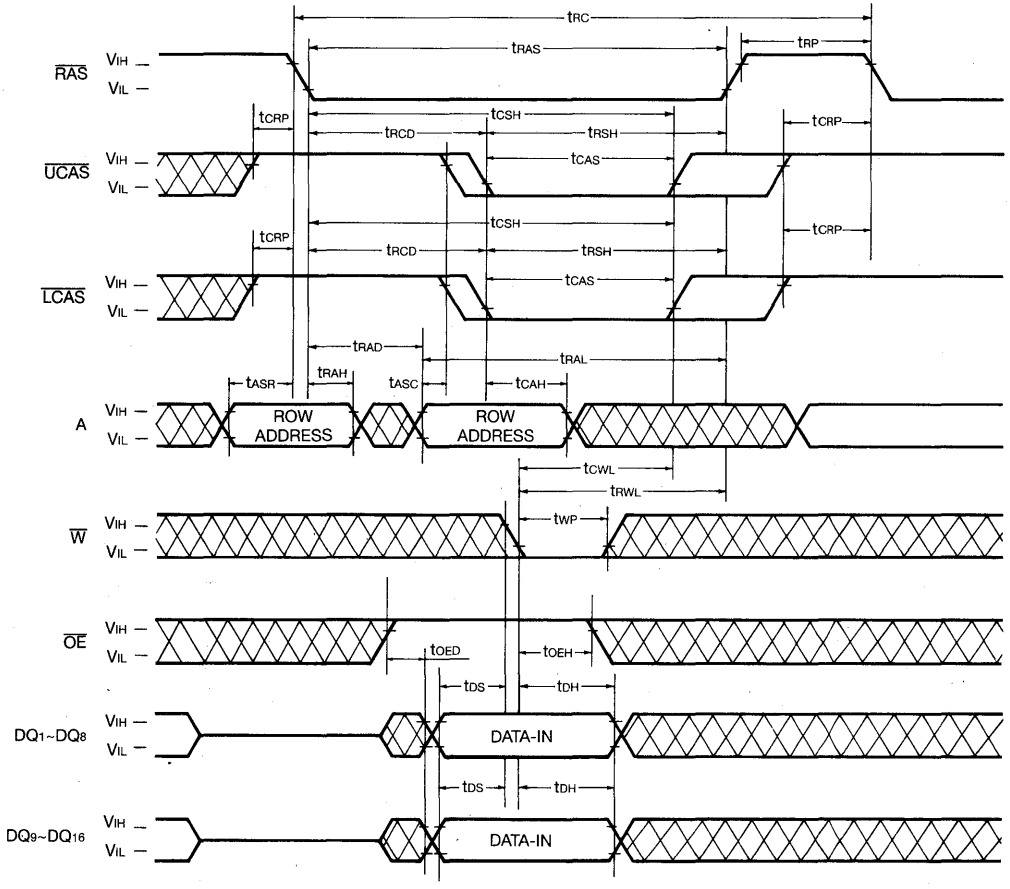
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT=OPEN



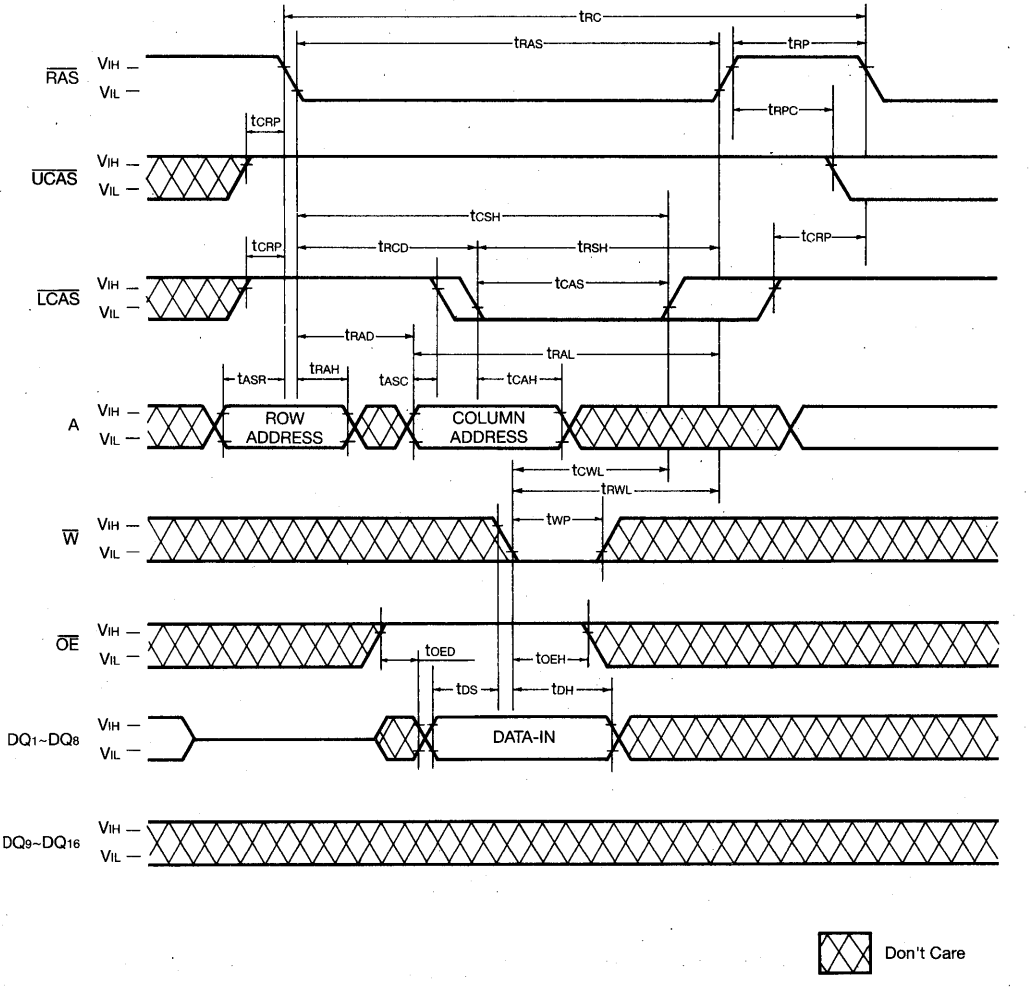
WORD WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : DOUT=OPEN



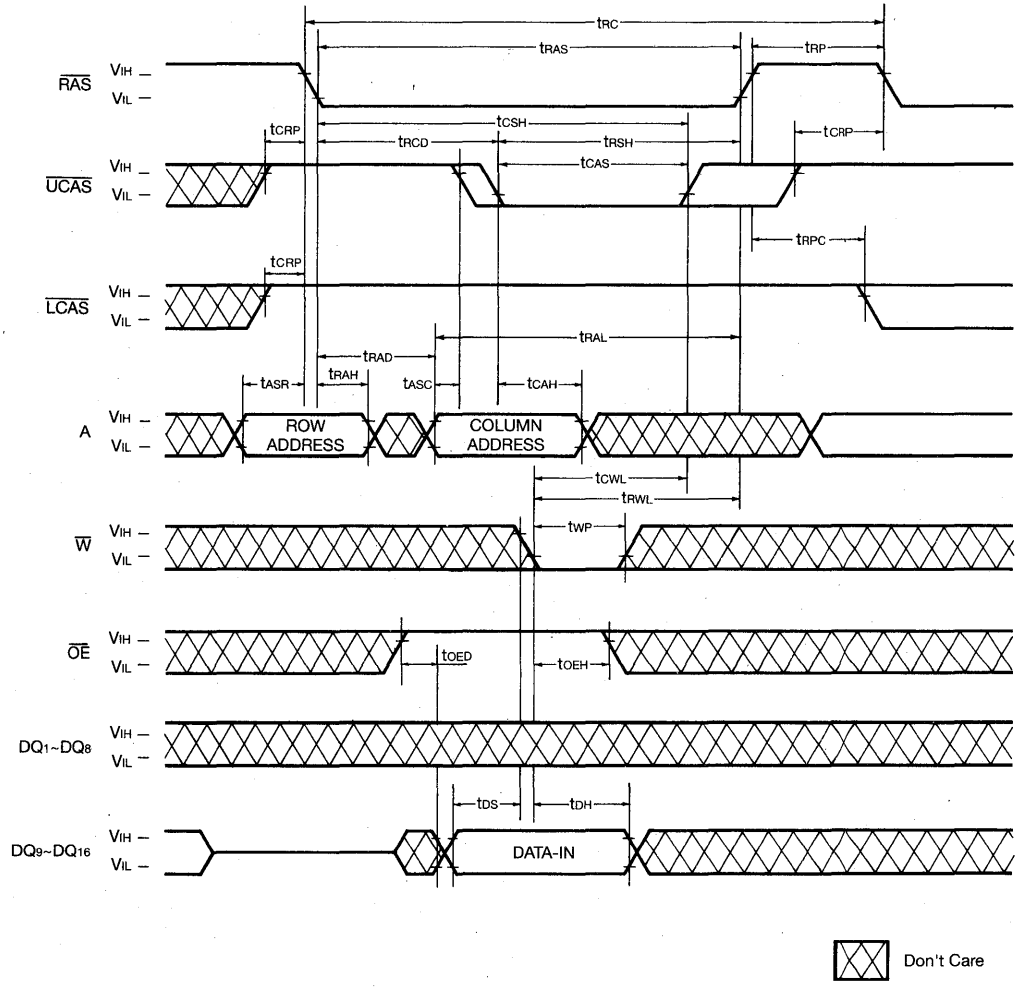
LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : DOUT=OPEN



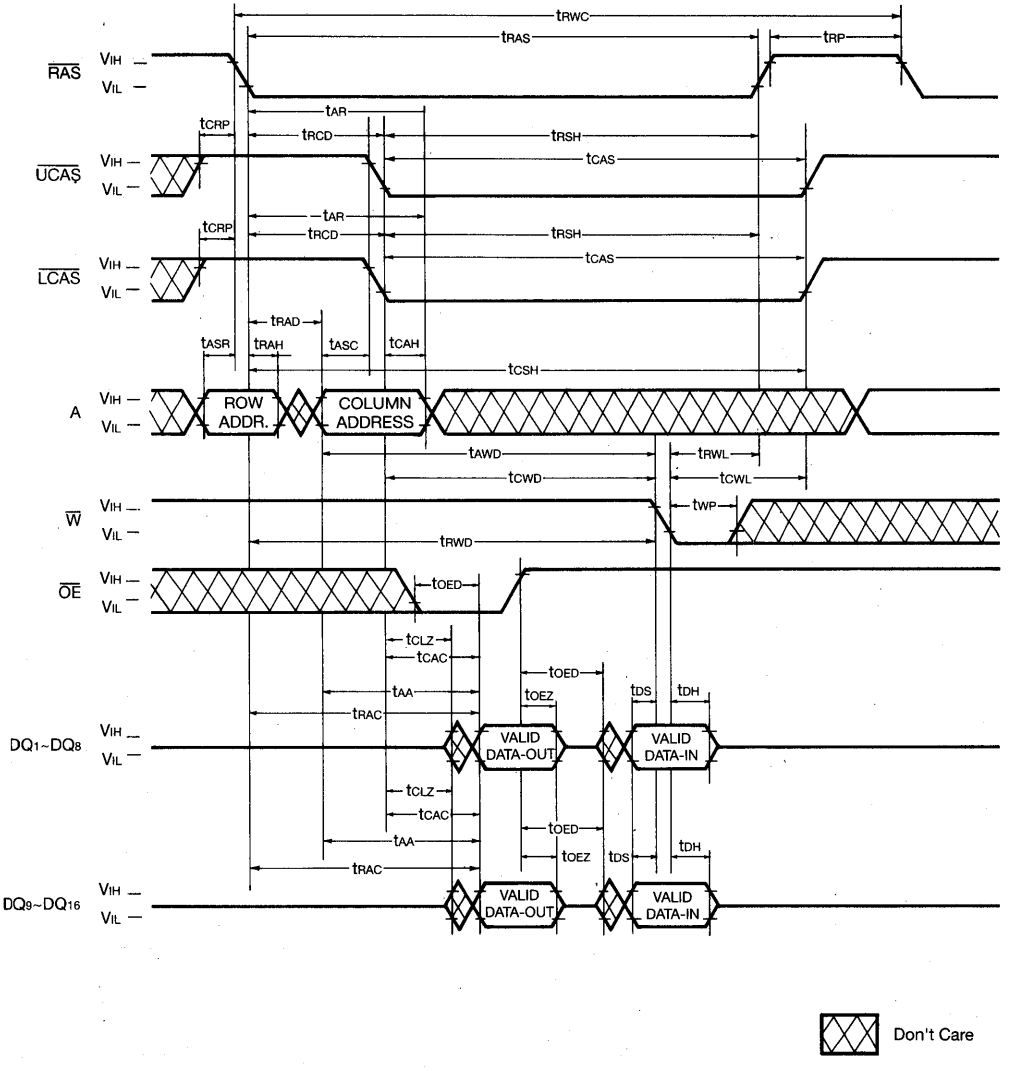
UPPER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : DOUT=OPEN

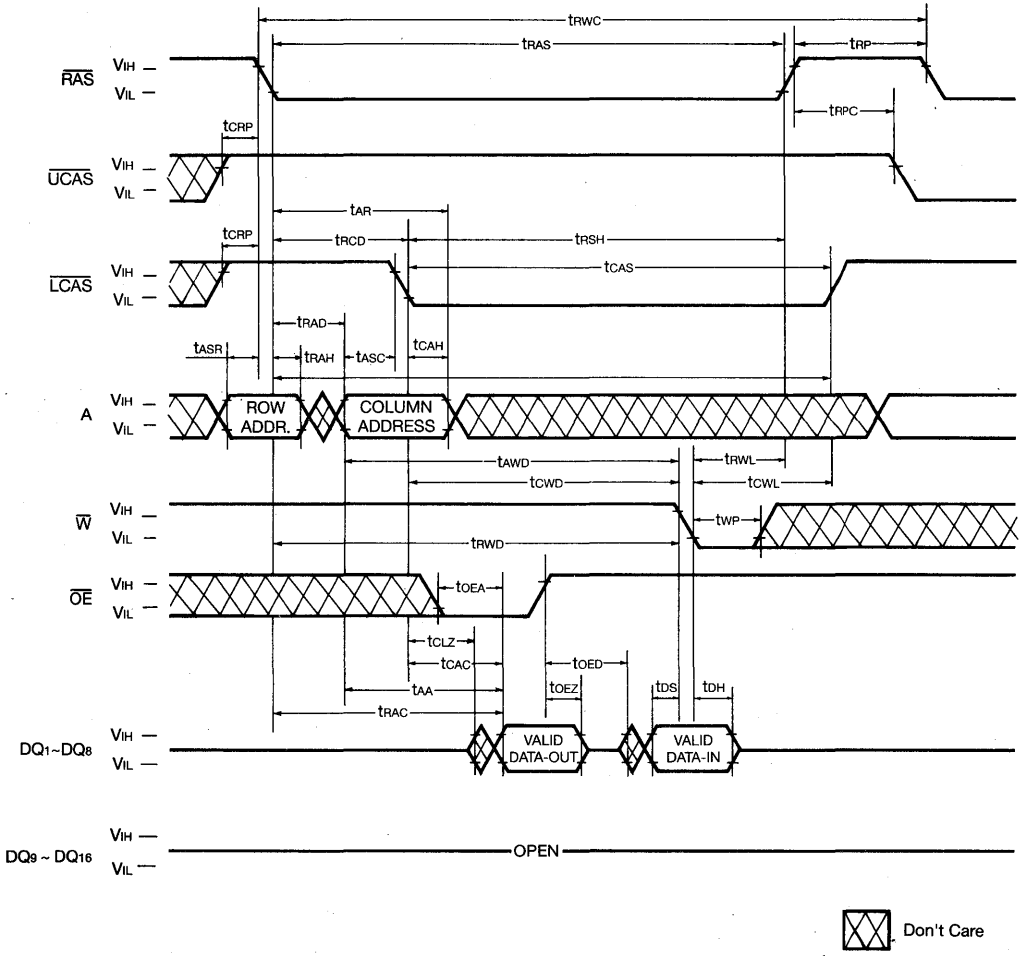


SAMSUNG ELECTRONICS

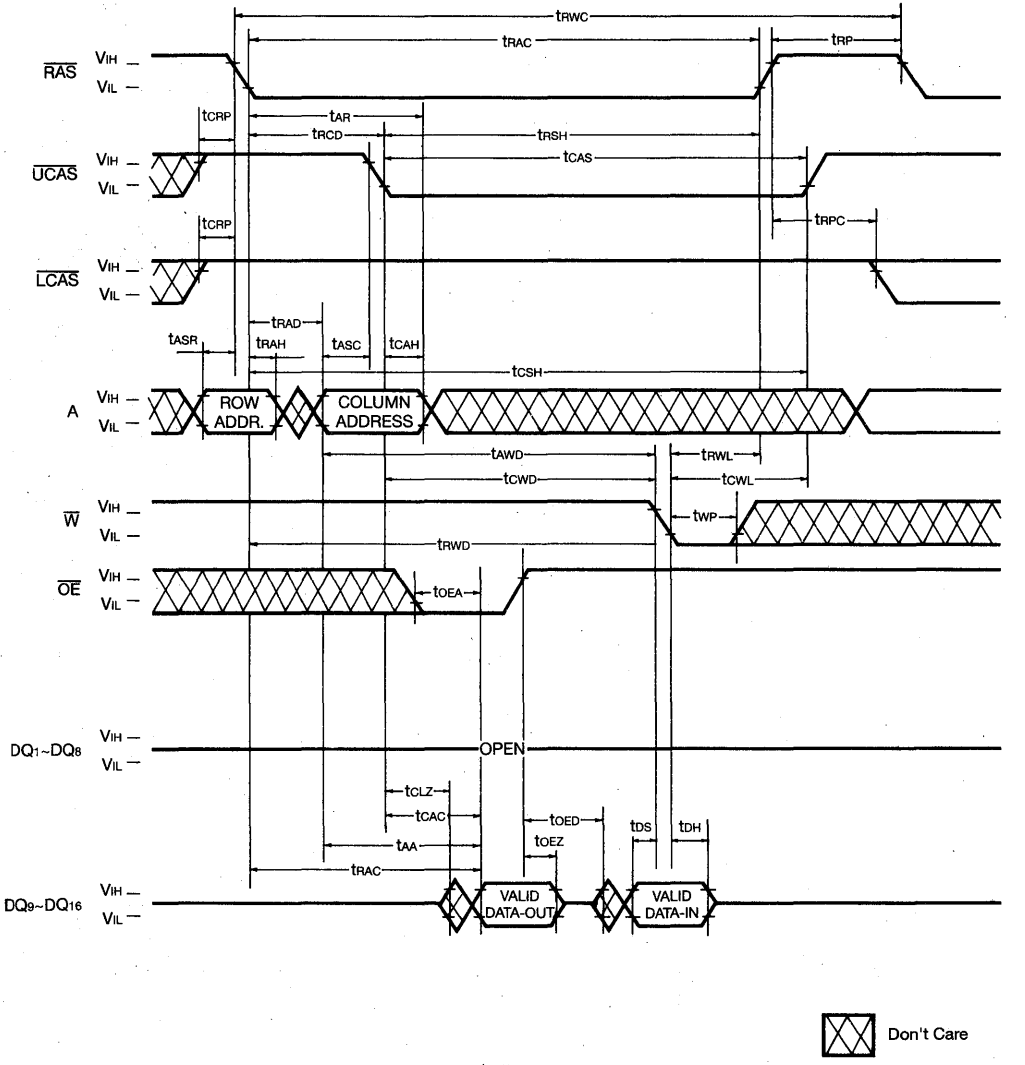
WORD READ-MODIFY-WRITE CYCLE



LOWER-BYTE READ-MODIFY-WRITE CYCLE

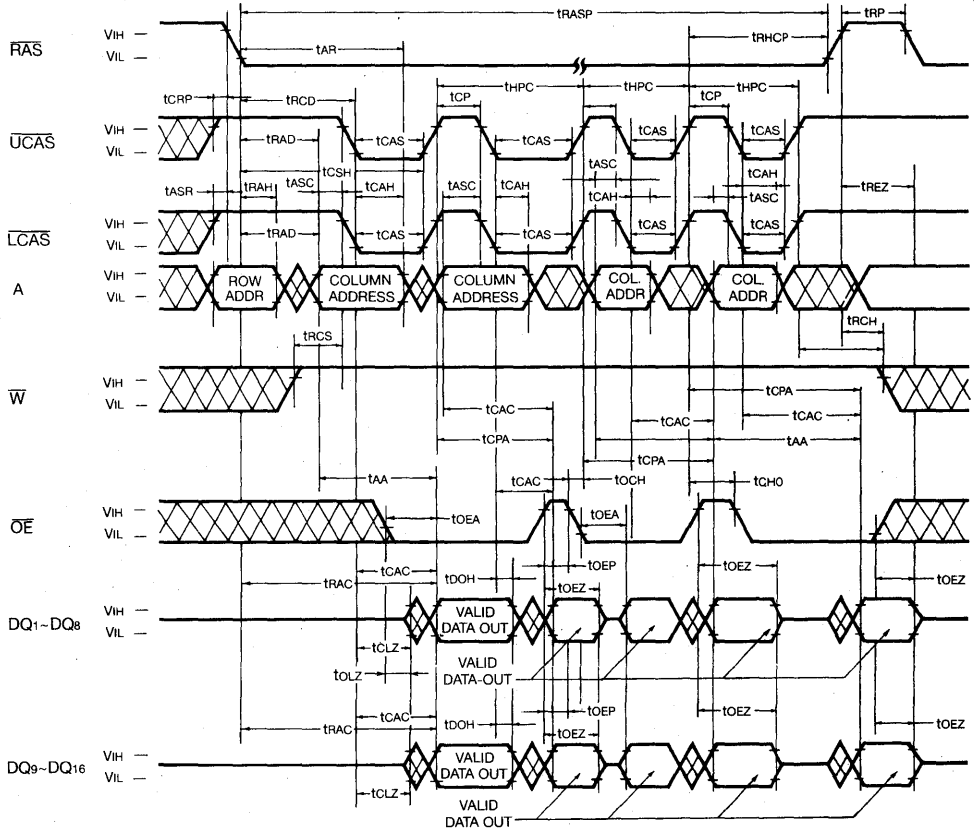


UPPER-BYTE READ-MODIFY-WRITE CYCLE

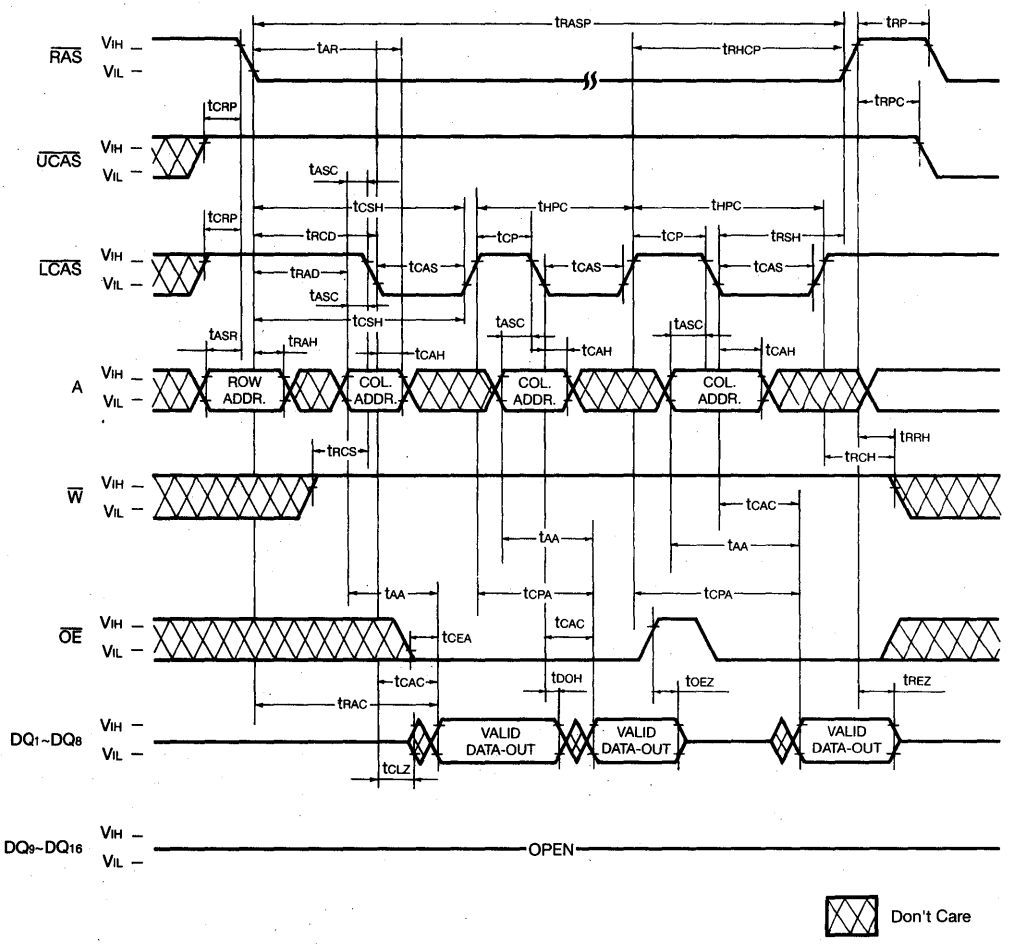


SAMSUNG ELECTRONICS

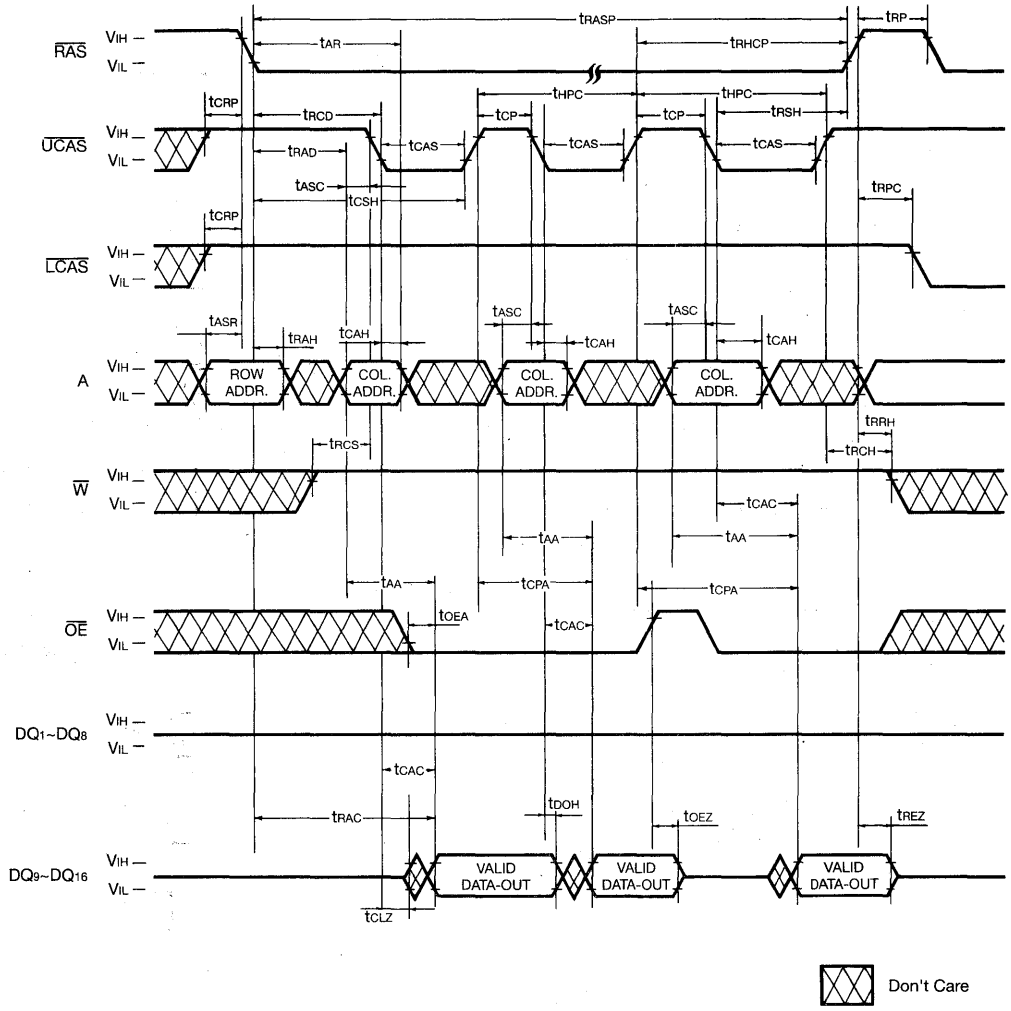
HYPER PAGE MODE WORD READ CYCLE



HYPER PAGE MODE LOWER BYTE READ CYCLE



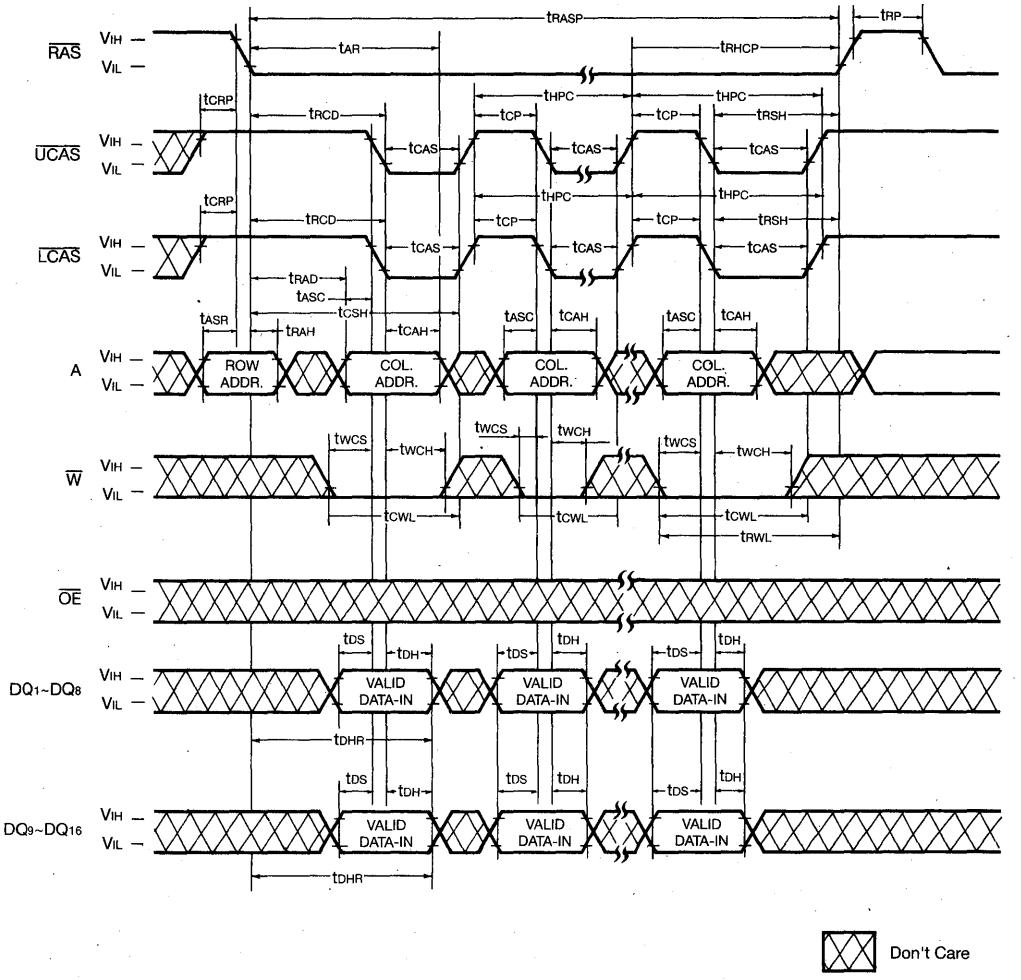
HYPER PAGE MODE UPPER BYTE READ CYCLE



SAMSUNG ELECTRONICS

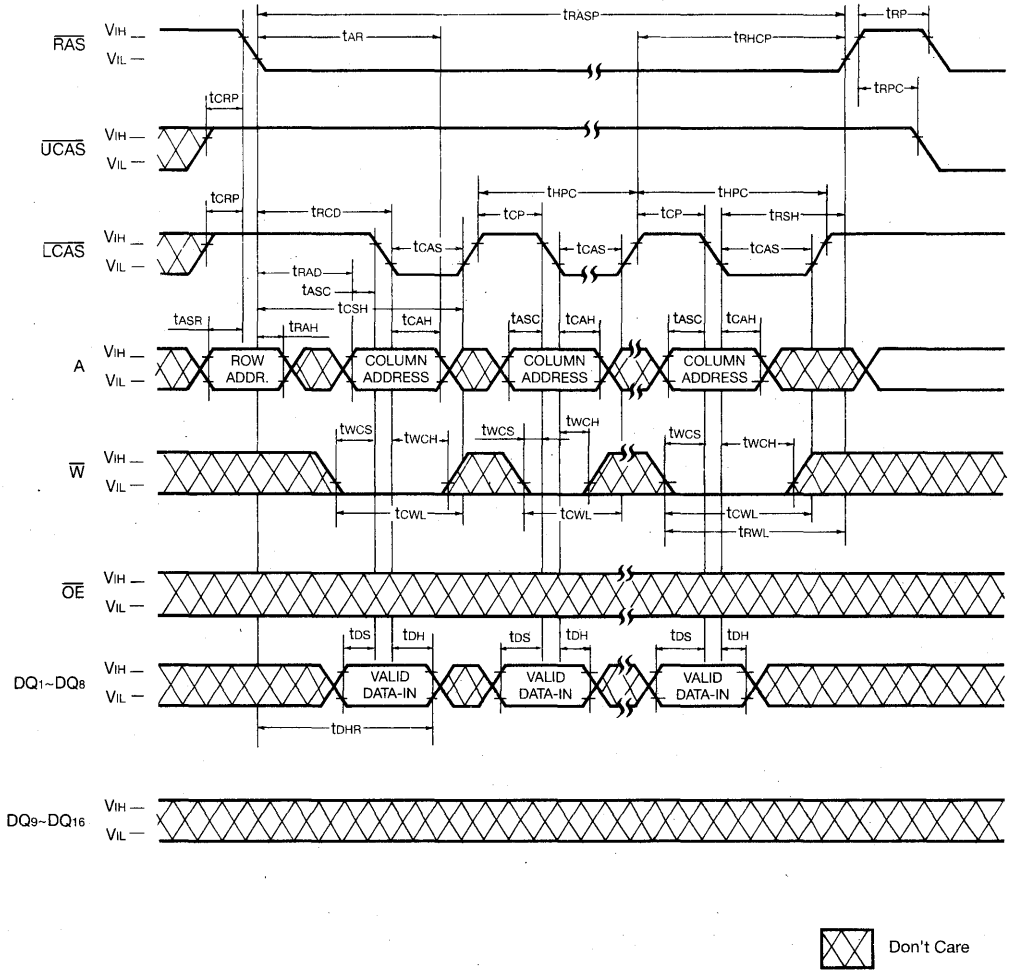
HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : DOUT=OPEN



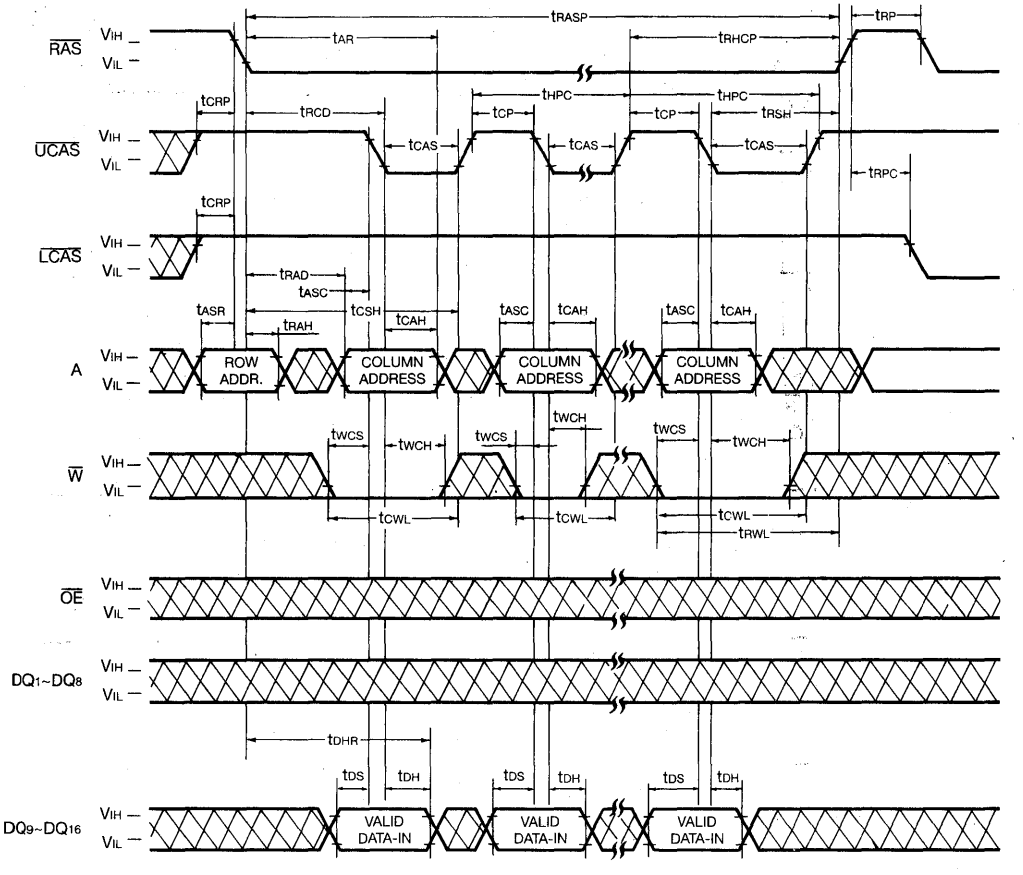
HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT}=OPEN

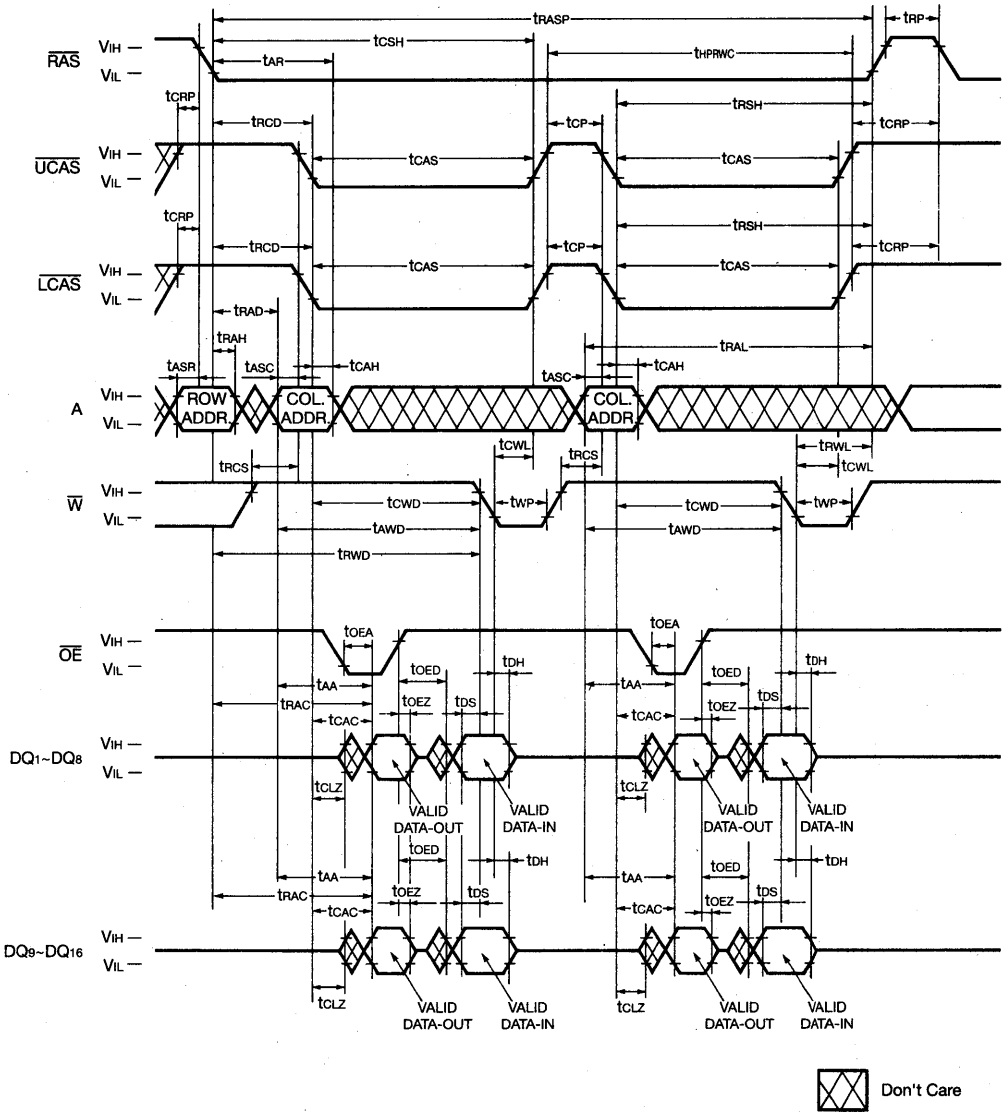


HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT=OPEN

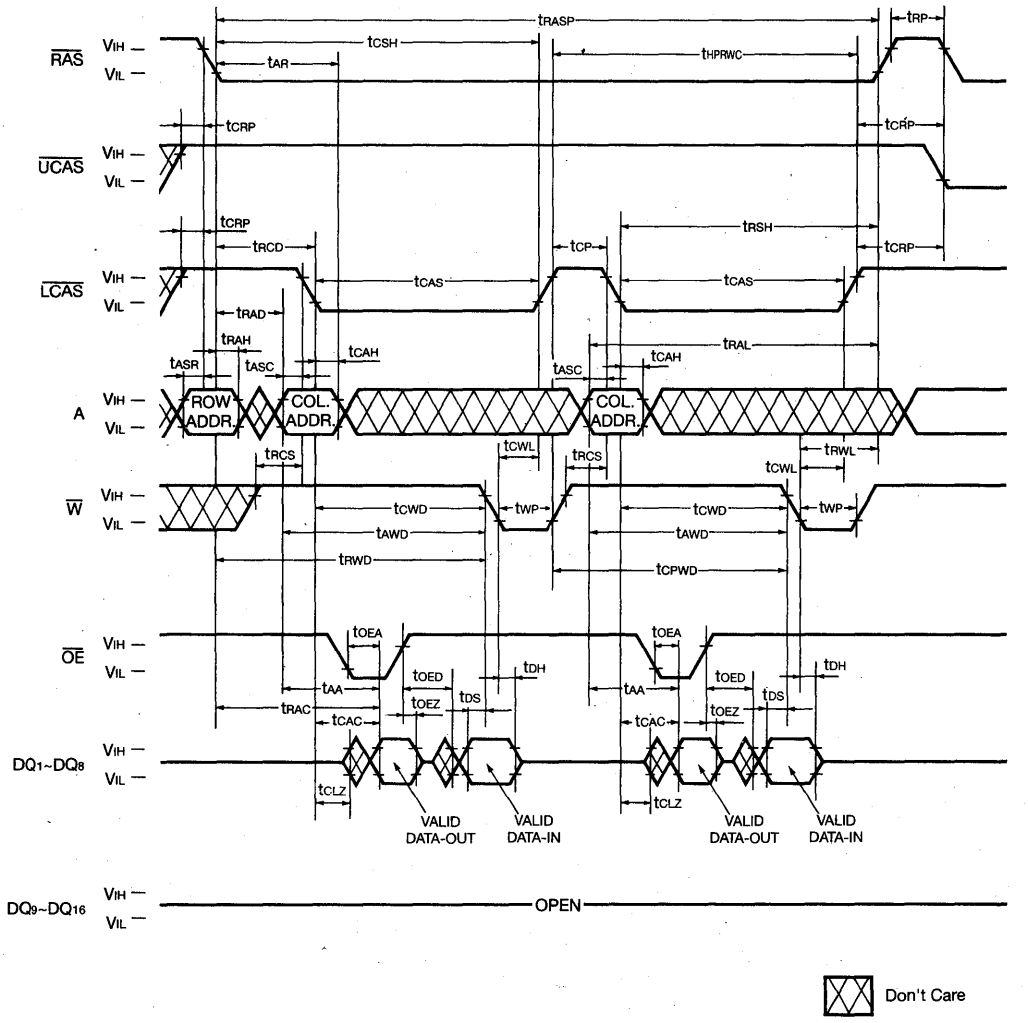


HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE

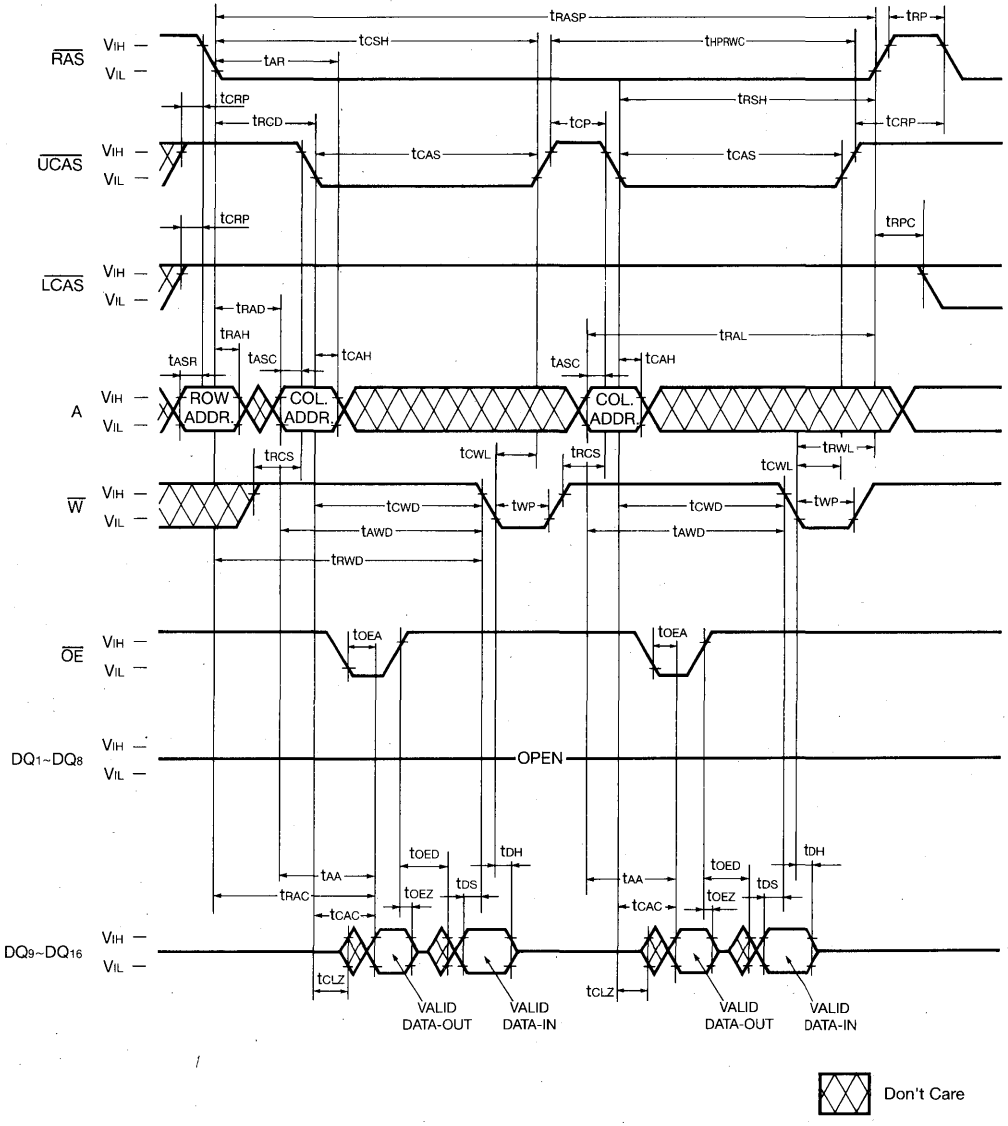


SAMSUNG ELECTRONICS

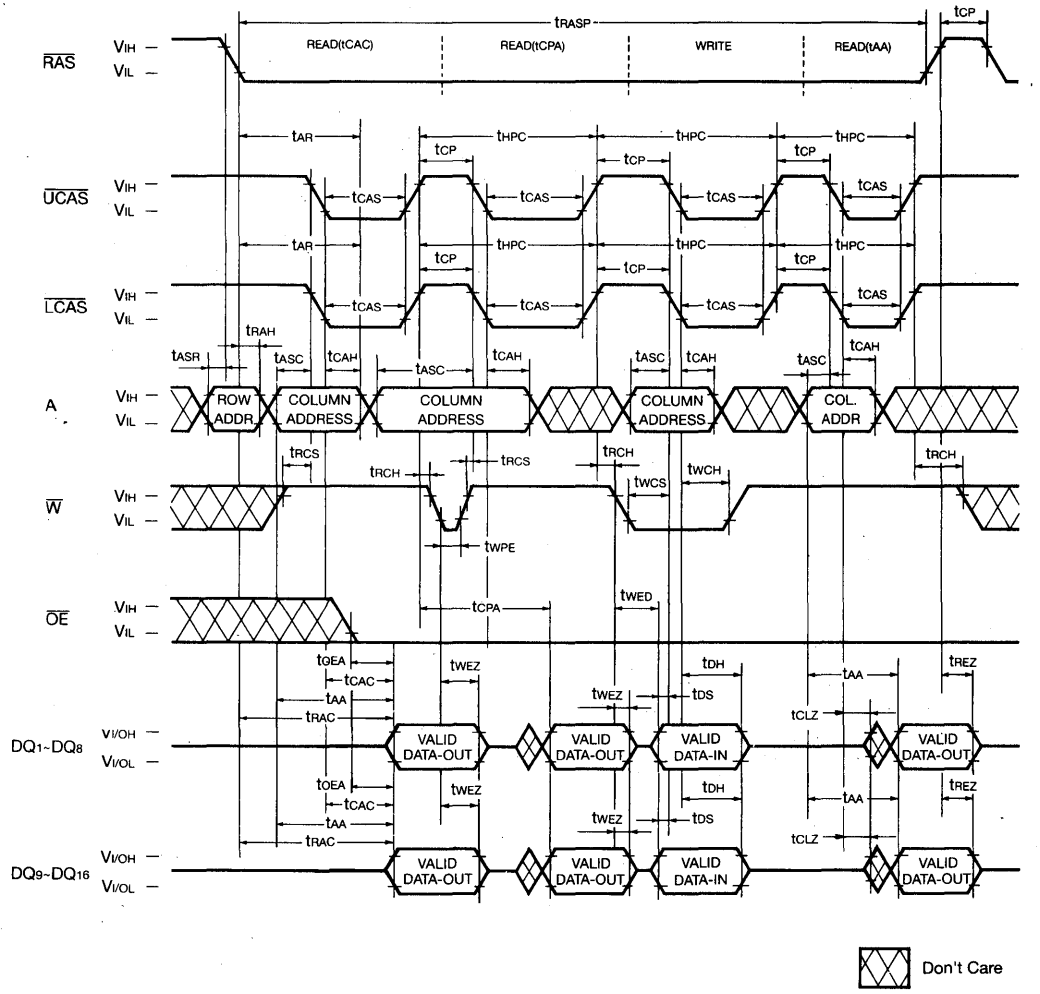
HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE

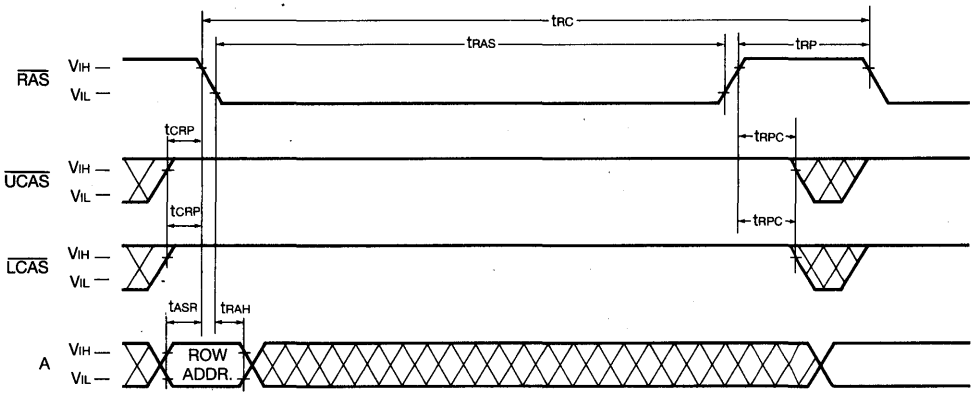


HYPER PAGE READ AND WRITE MIXED CYCLE



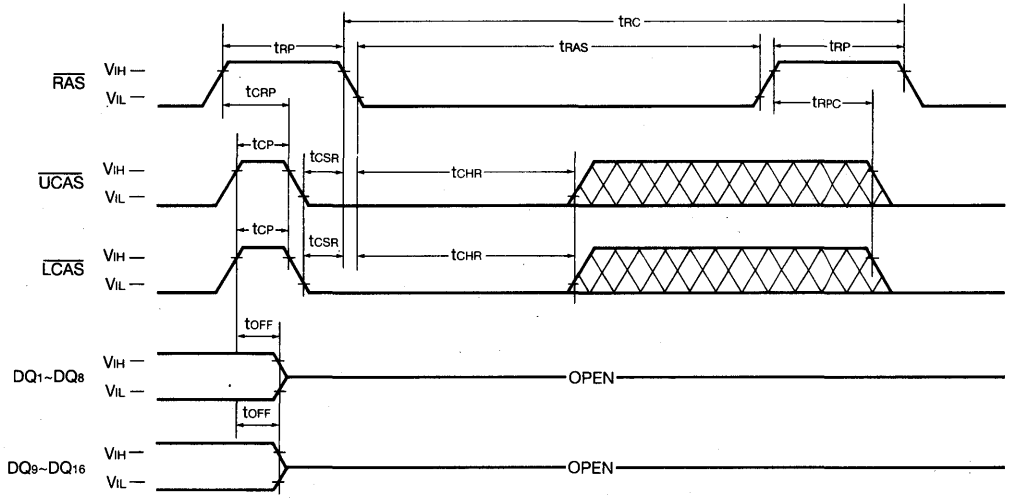
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN}=Don't Care
D_{OUT}=OPEN



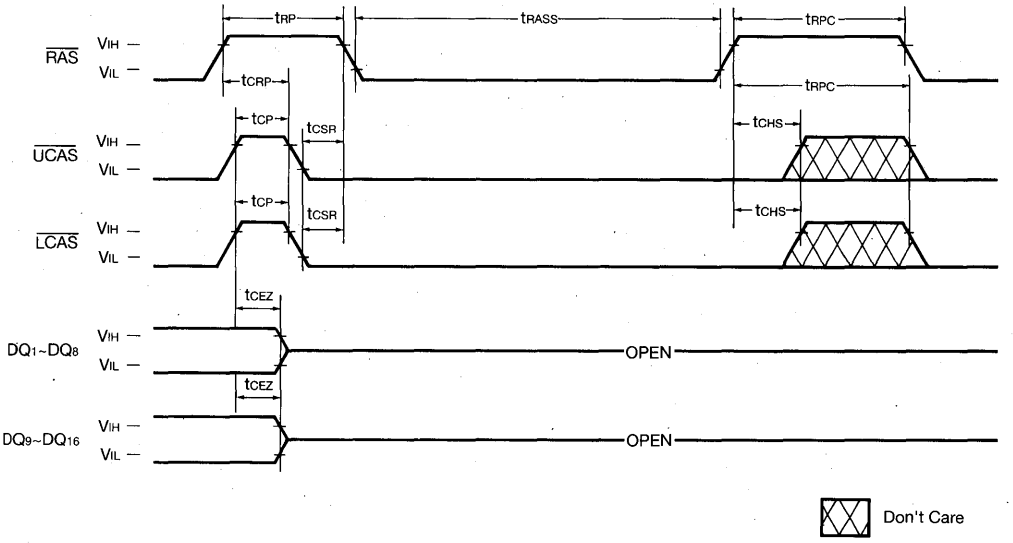
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A=Don't Care

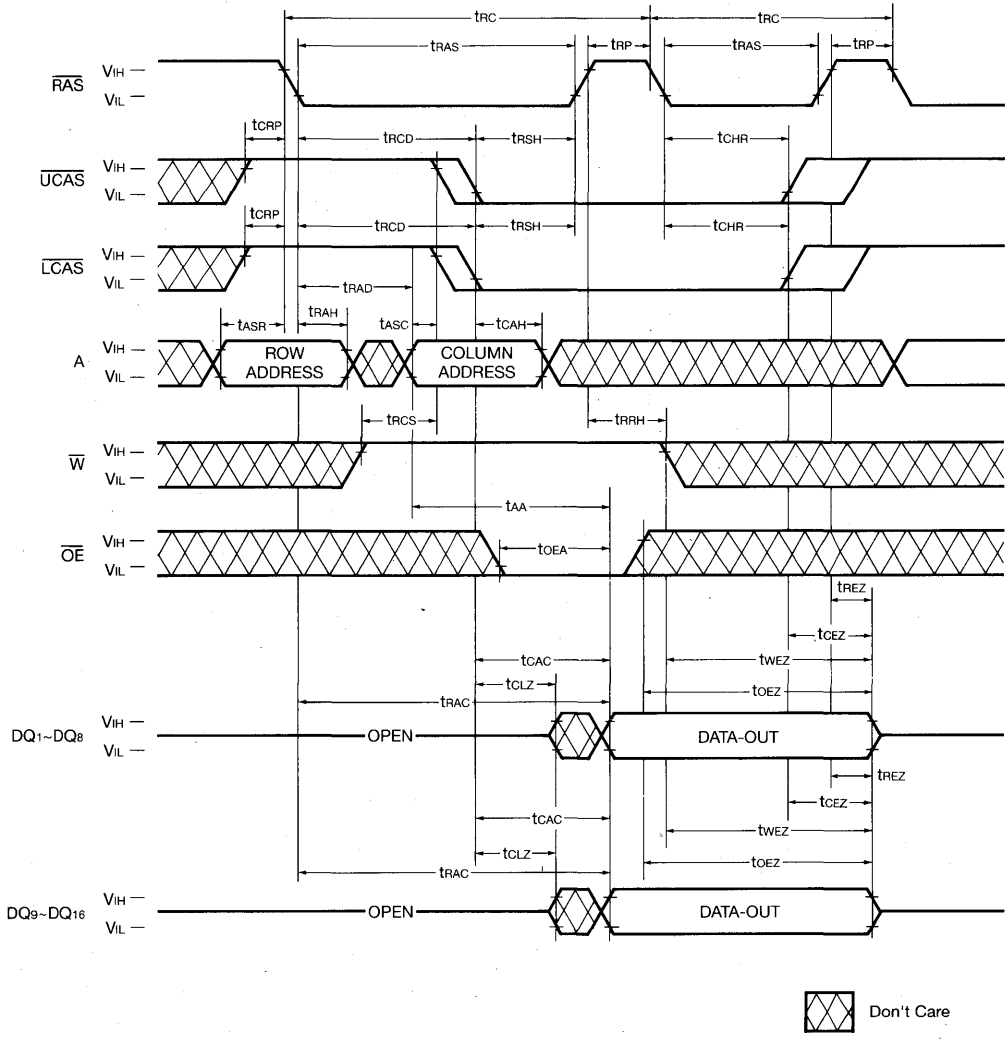


$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-Version)

NOTE : $\overline{W}$, $\overline{OE}$, A=Don't Care

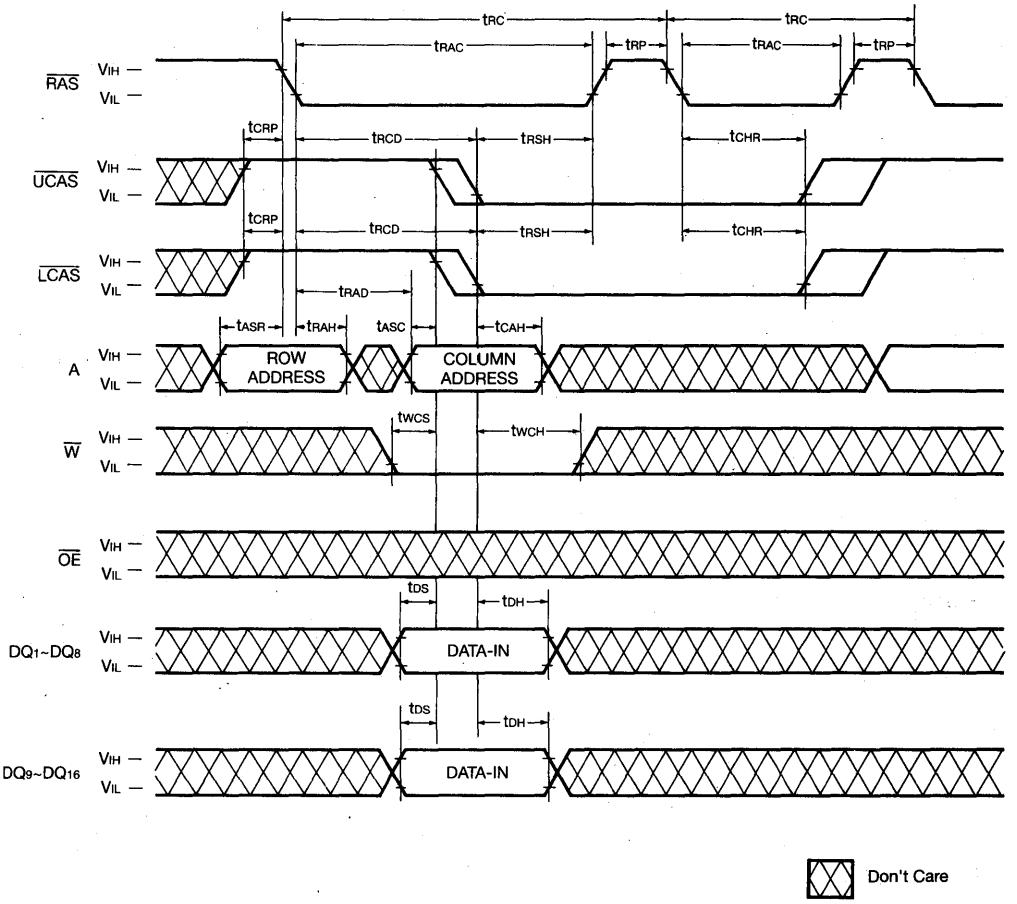


HIDDEN REFRESH CYCLE (READ)

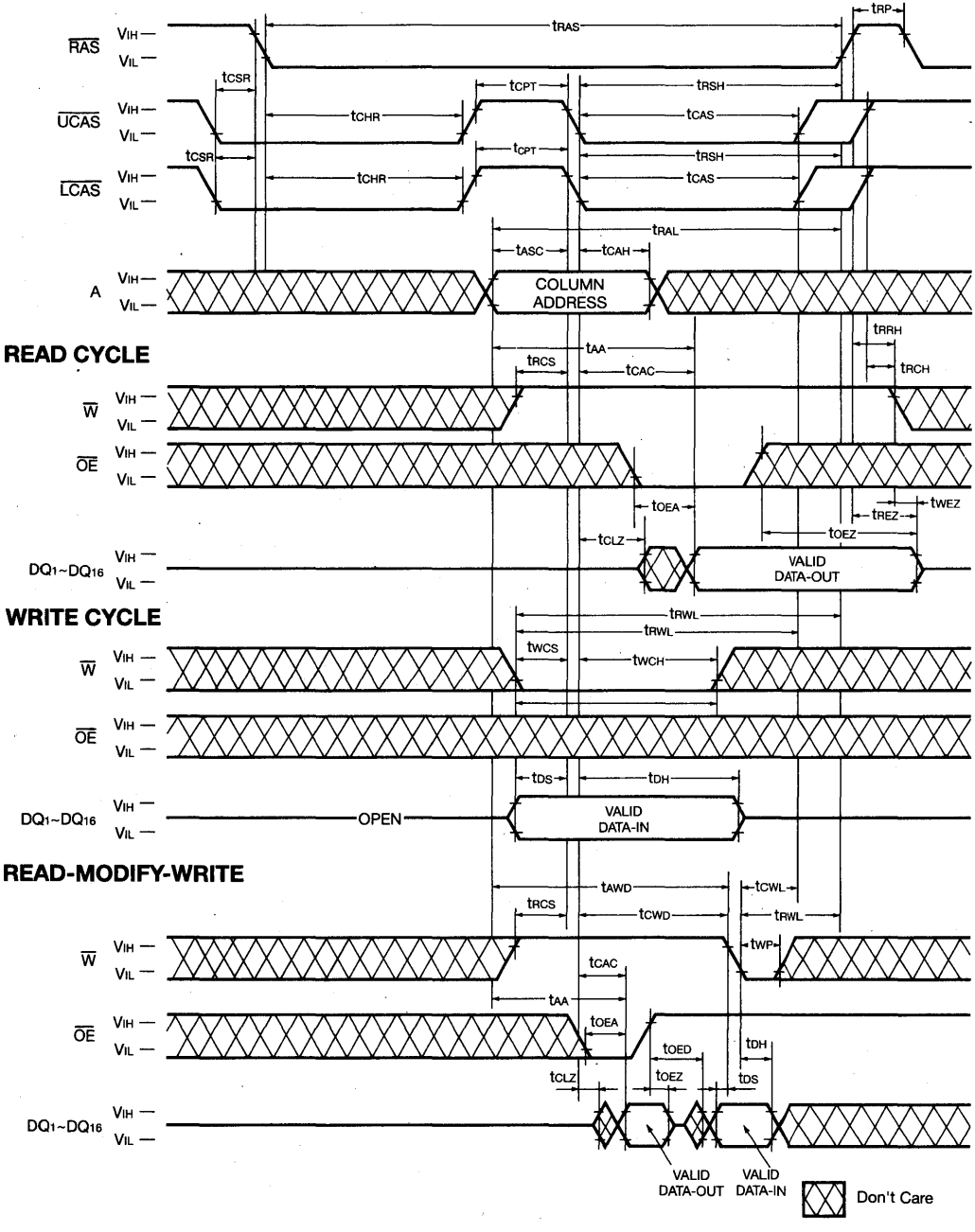


HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT=OPEN



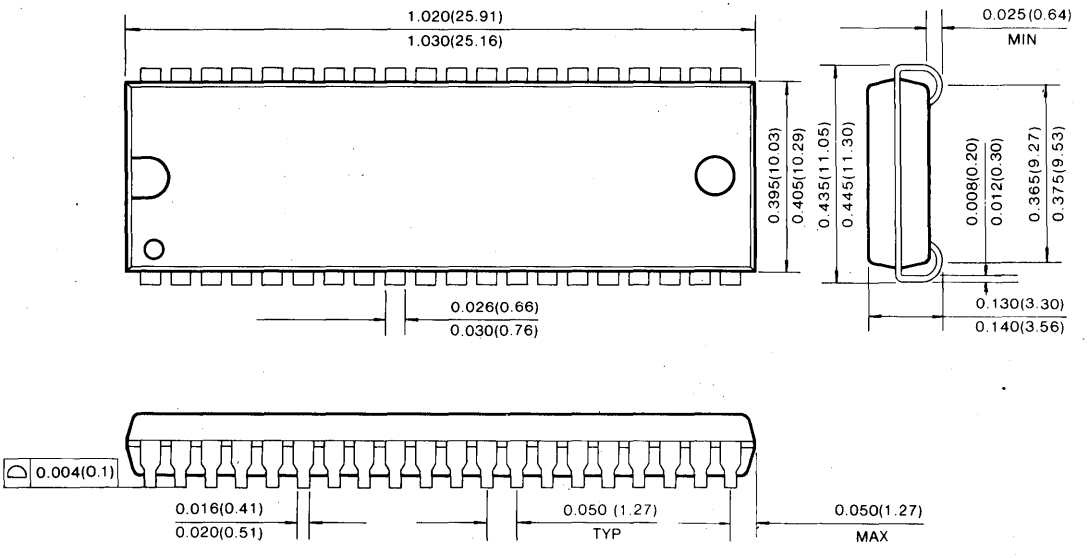
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



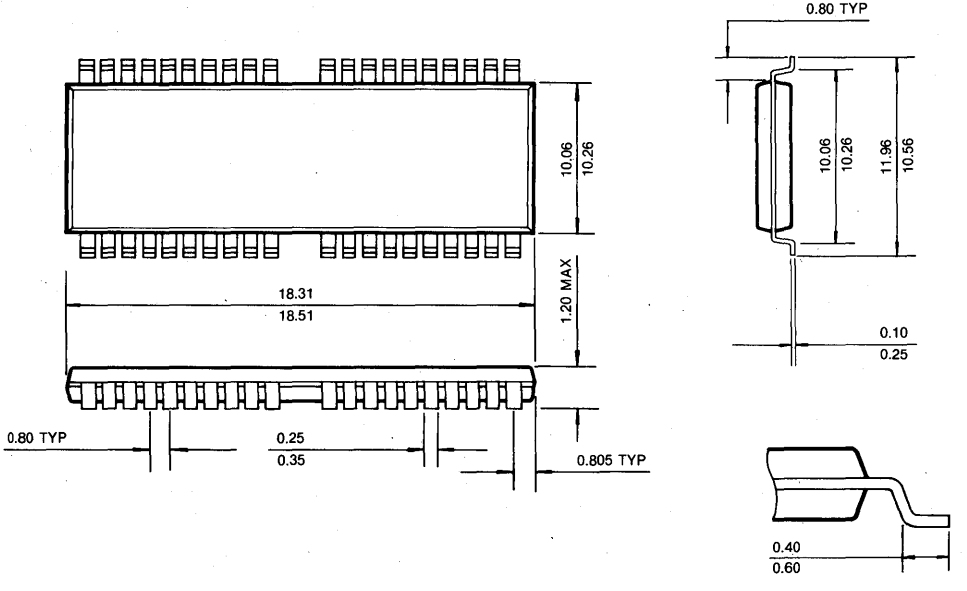
PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)



256K × 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM416C156B/BL/BLL-5	50ns	15ns	90ns
KM416C156B/BL/BLL-6	60ns	15ns	110ns
KM416C156B/BL/BLL-7	70ns	20ns	130ns
KM416C156B/BL/BLL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Byte Write operation (2$\overline{W}$)**
- **Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Self Refresh Operation (LL-version)**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +5V±10% power supply**
- **Refresh Cycle**
  - **-512 cycle/8ms refresh**
  - **-512 cycle/64ms (L-Version)**
  - **-512 cycle/128ms (LL-Version)**
- **Power Dissipation**
  - **-Standby: 5.5mW (Normal)**
  - **1.1mW (L-version)**
  - **0.83mW (LL-version)**
  - **-Active (50/60/70/80): 605/495/440/415mW**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP (II)**

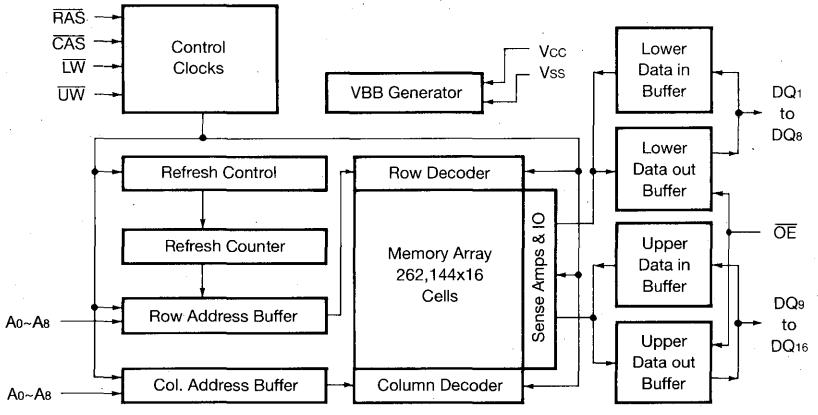
GENERAL DESCRIPTION

The Samsung KM416C156B/BL/BLL is a CMOS high speed 262,144 bit × 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance portable computers.

The KM416C156B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

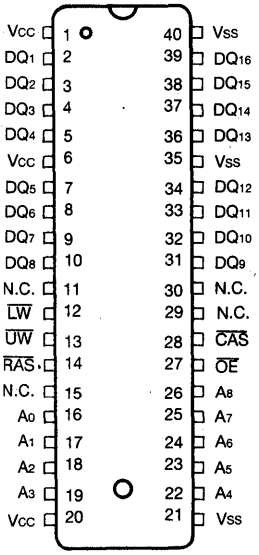
The KM416C156B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

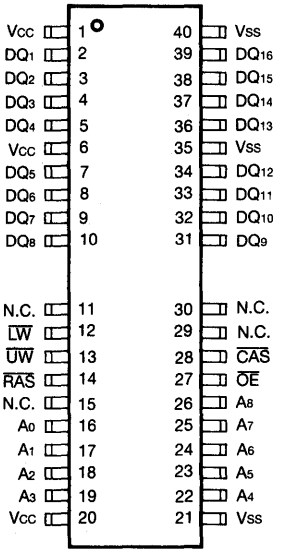


PIN CONFIGURATION (Top Views)

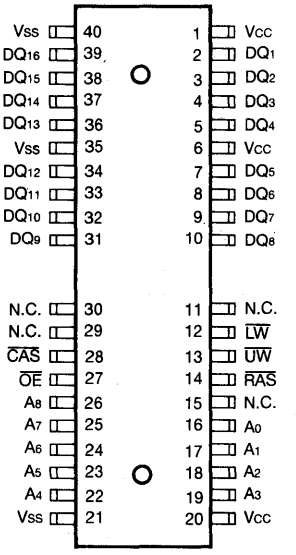
• KM416C156BJ/BLJ/BLLJ



• KM416C156BT/BLT/BLLT



• KM416C156BTR/BLTR/BLLTR



Pin Name	Pin Function
A0-A8	Address Inputs
DQ1~16	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{UW}$	Read Upper Byte Write Input
$\overline{LW}$	Read Lower Byte Write Input
$\overline{OE}$	Data Output Enable
VCC	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} +1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM416C156B/BL/BLL-5	I_{CC1}	-	110	mA
	KM416C156B/BL/BLL-6			90	mA
	KM416C156B/BL/BLL-7			80	mA
	KM416C156B/BL/BLL-8			75	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{UW}$=$\overline{LW}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM416C156B/BL/BLL-5	I_{CC3}	-	110	mA
	KM416C156B/BL/BLL-6			90	mA
	KM416C156B/BL/BLL-7			80	mA
	KM416C156B/BL/BLL-8			75	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM416C156B/BL/BLL-5	I_{CC4}	-	70	mA
	KM416C156B/BL/BLL-6			60	mA
	KM416C156B/BL/BLL-7			55	mA
	KM416C156B/BL/BLL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{UW}$=$\overline{LW}$=V_{CC}-0.2V)	KM416C156B	I_{CC5}	-	1	mA
	KM416C156BL			200	mA
	KM416C156BLL			150	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM416C156B/BL/BLL-5	I_{CC6}	-	110	mA
	KM416C156B/BL/BLL-6			90	mA
	KM416C156B/BL/BLL-7			80	mA
	KM416C156B/BL/BLL-8			75	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=0.2V D_{IN}=Don't Care, T_{RC}=125μS(L-ver.), T_{RAS}=T_{RAS} min.~300ns	KM416C156BL	I_{CC7}	-	300	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{xW}$=$\overline{OE}$=A_0-A_8=V_{CC}-0.2V or 0.2V	KM416C156BLL	I_{CCS}		200	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level ($I_{O(H)}$=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level ($I_{O(L)}$=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_8)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{LW}$, $\overline{UW}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5V±10%, See notes 1,2)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	135		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	35	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	

(*) 50ns Product:V_{CC}=5V ± 5%, Cout=50pF

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		50		55		ns	6
Write command pulse width	t_{WP}	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		8		8		8		8	ms	
Refresh period (L-Version)	t_{REF}		64		64		64		64	ms	
Refresh period (LL-Version)	t_{REF}		128		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{LW}$, $\overline{UW}$ delay time	t_{CWD}	40		40		50		50		ns	8
$\overline{RAS}$ to $\overline{LW}$, $\overline{UW}$ delay time	t_{RWD}	75		85		95		105		ns	8
Column address to $\overline{LW}$, $\overline{UW}$ delay time	t_{AWD}	50		55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	55		60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	80		80		95		100		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	20	ns	7

(*) 50ns Product:Vcc=5V ± 5%, Cout=50pF

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{OE}$ commend hold time	tOEH	15		15		20		20		ns	
Masked write set-up time	tMCS	0		0		0		0		ns	
Masked write hold time referenced to $\overline{RAS}$	tMRH	0		0		0		0		ns	
Masked write hold time referenced to $\overline{CAS}$	tMCH	0		0		0		0		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

(*) 50ns Product:V_{CC}=5V ± 5%, Cout=50pF

KM416C156B Truth Table

$\overline{RAS}$	$\overline{CAS}$	$\overline{UW}$	$\overline{LW}$	$\overline{OE}$	DQ_1~DQ_8	DQ_9~DQ_{16}	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	X	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	L	L	X	DQ-IN	DQ-IN	Word Write
L	L	H	L	X	DQ-IN	-	Byte Write
L	L	L	H	X	-	DQ-IN	Byte Write

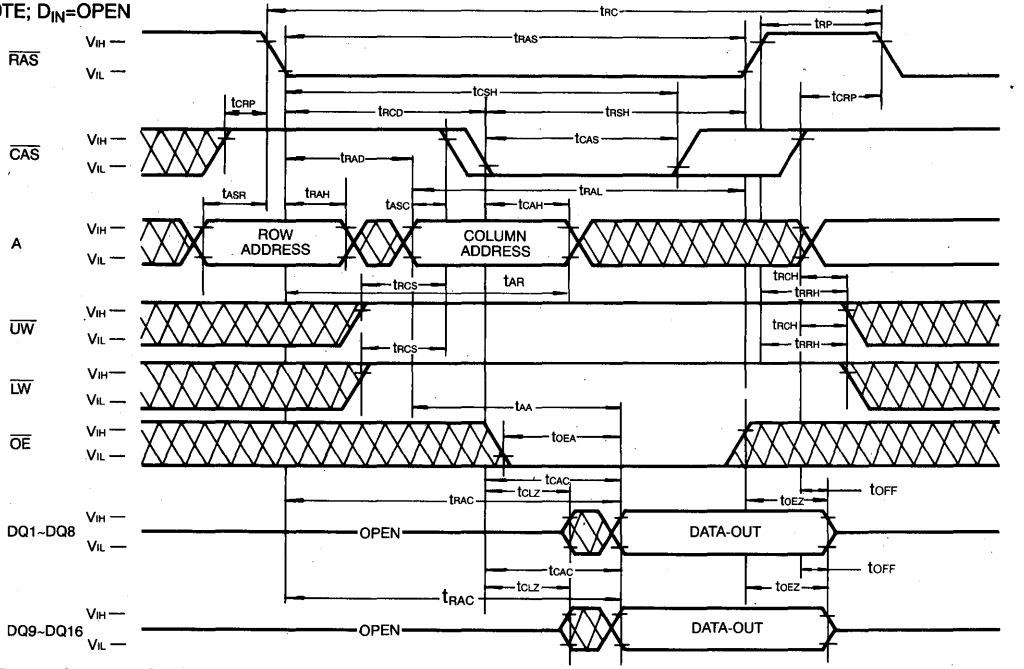
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. 512 cycles of burst refresh must be executed within 8ms before and after self refresh, In order to meet refresh specification.
13. t_{RCS}, t_{MCS} are referenced to the later $\overline{W}$ rising edge at early write cycle.
14. t_{WCS} is referenced to the later $\overline{W}$ falling edge at early write cycle.
15. t_{CWL}, t_{RWL} are referenced to the later $\overline{W}$ falling edge at early write cycle.
16. t_{WCH}, t_{WP} are referenced to the earler $\overline{W}$ falling edge at early write cycle.
17. t_{RWD}, t_{AWD}, t_{CWD} are referenced to the earler $\overline{W}$ falling edge at Read-Modify-write cycle.

TIMING DIAGRAM

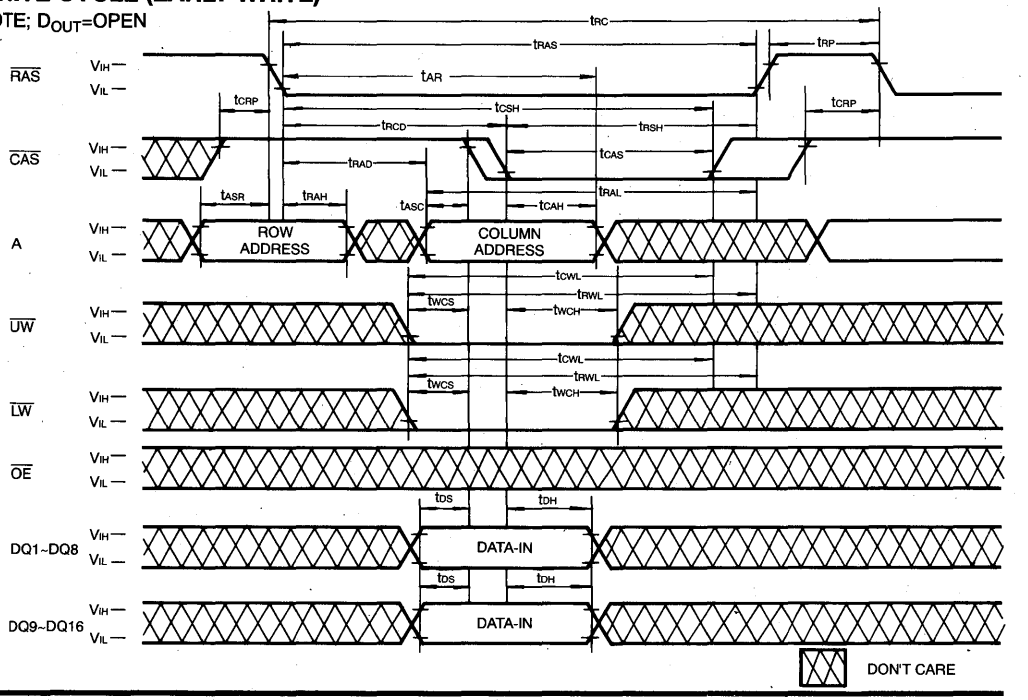
READ CYCLE

NOTE; D_{IN}=OPEN



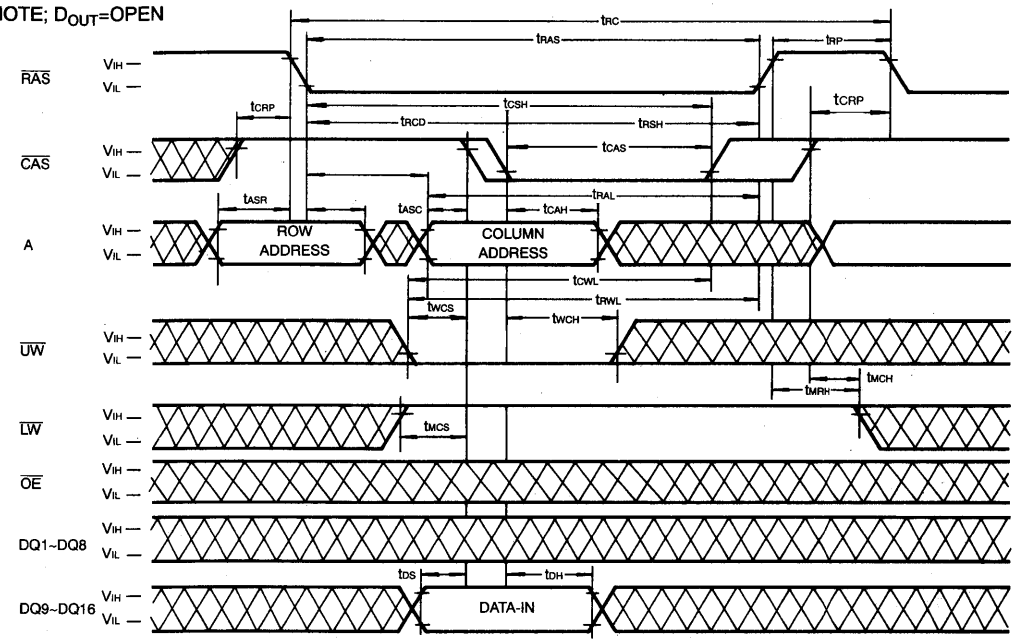
WRITE CYCLE (EARLY WRITE)

NOTE; D_{OUT}=OPEN



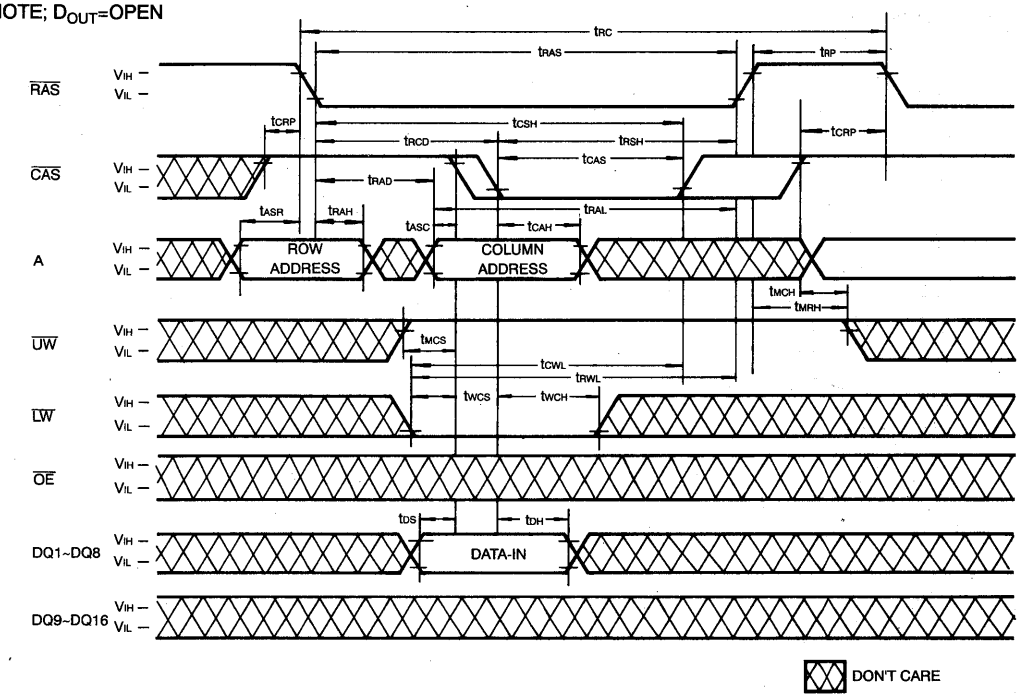
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE; D_{OUT}=OPEN



LOWER BYTE WRITE CYCLE (EARLY WRITE)

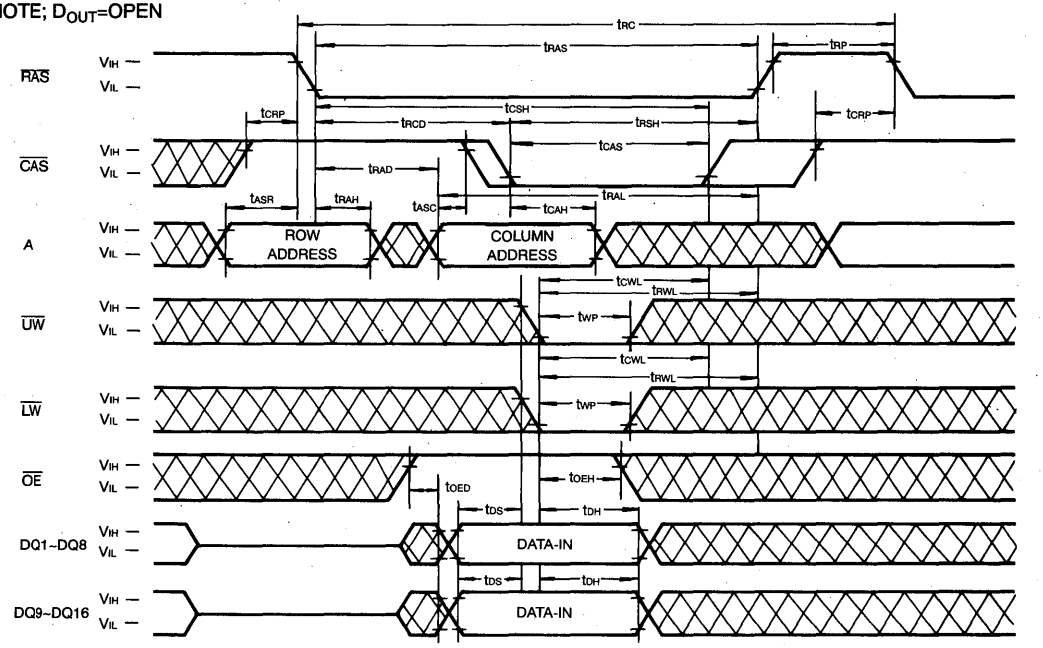
NOTE; D_{OUT}=OPEN



SAMSUNG ELECTRONICS

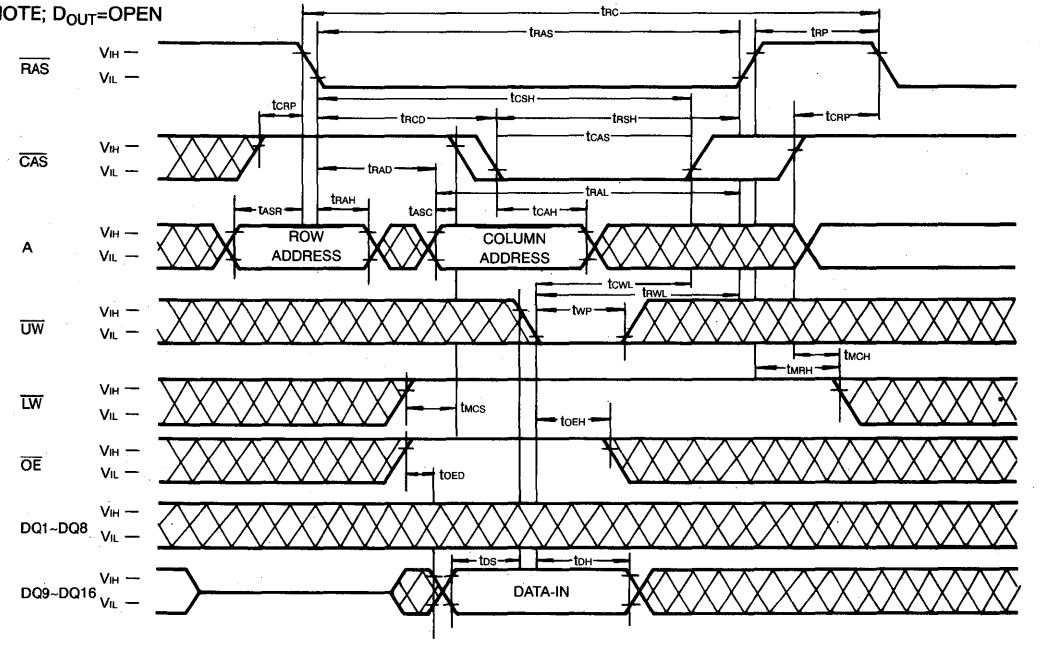
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE; D_{OUT}=OPEN



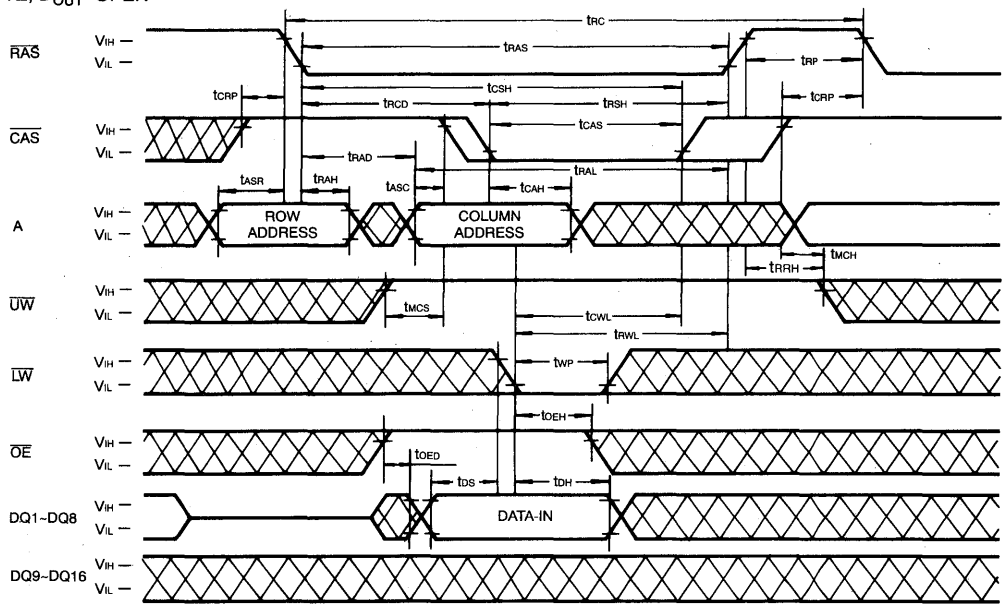
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE; D_{OUT}=OPEN

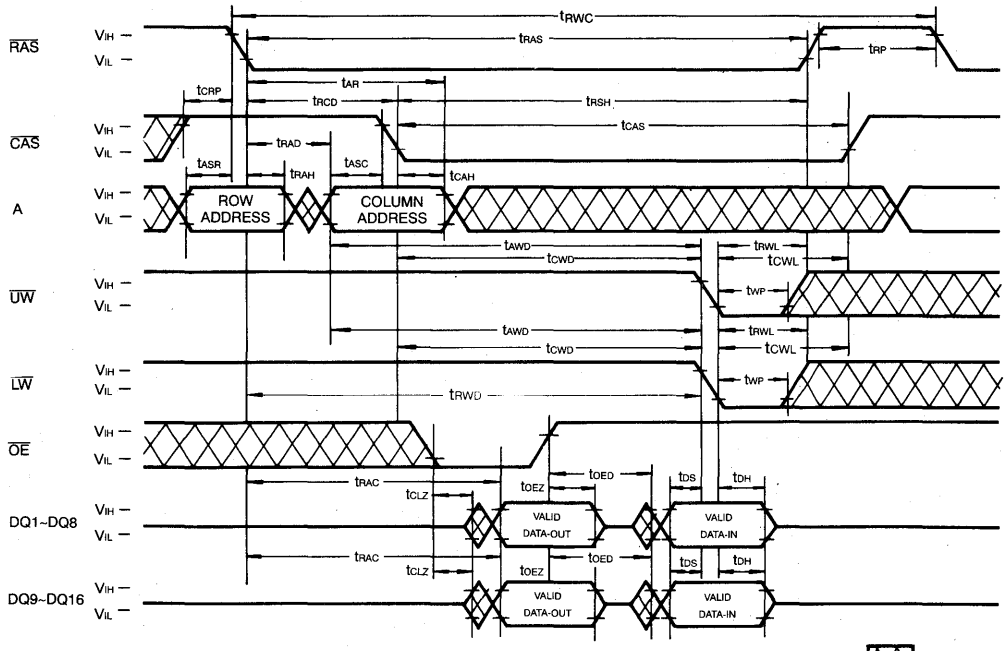


LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

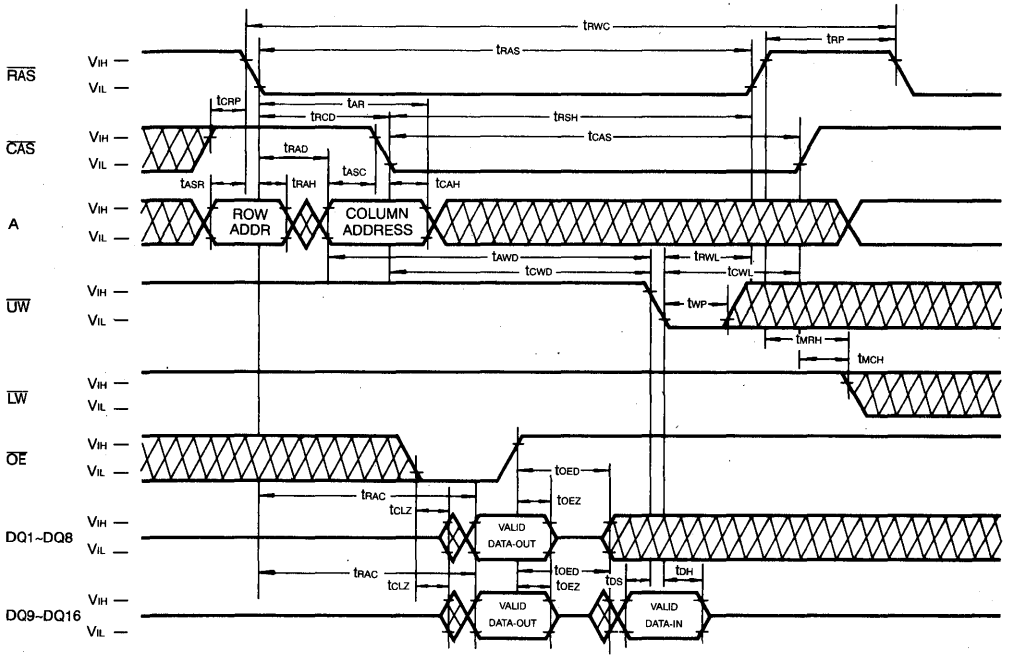
NOTE; D_{OUT}=OPEN



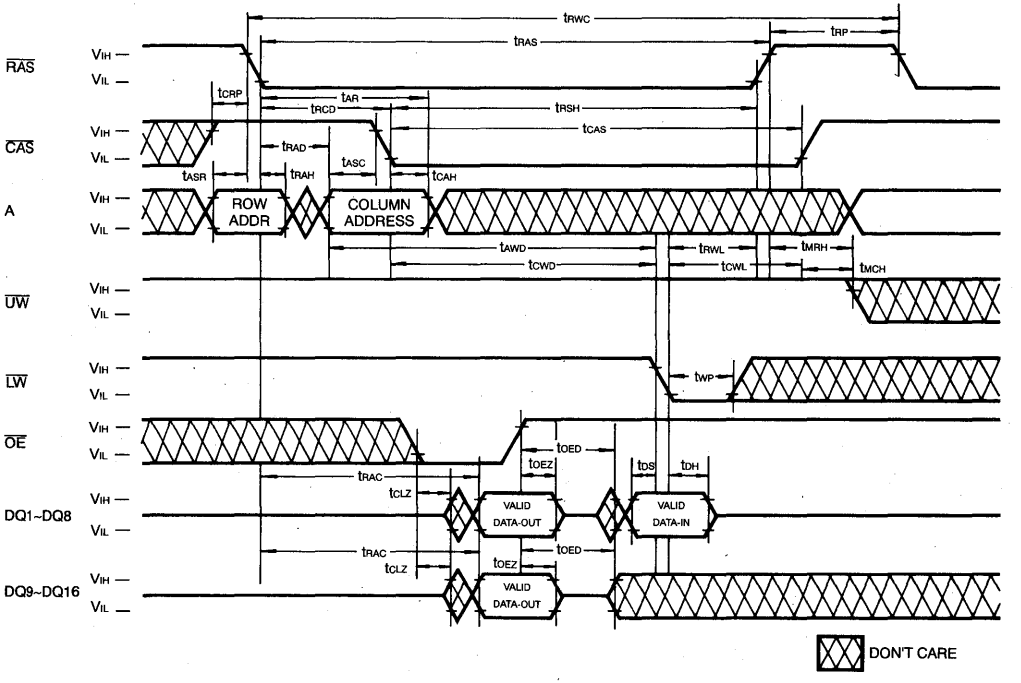
READ-MODIFY-WRITE CYCLE



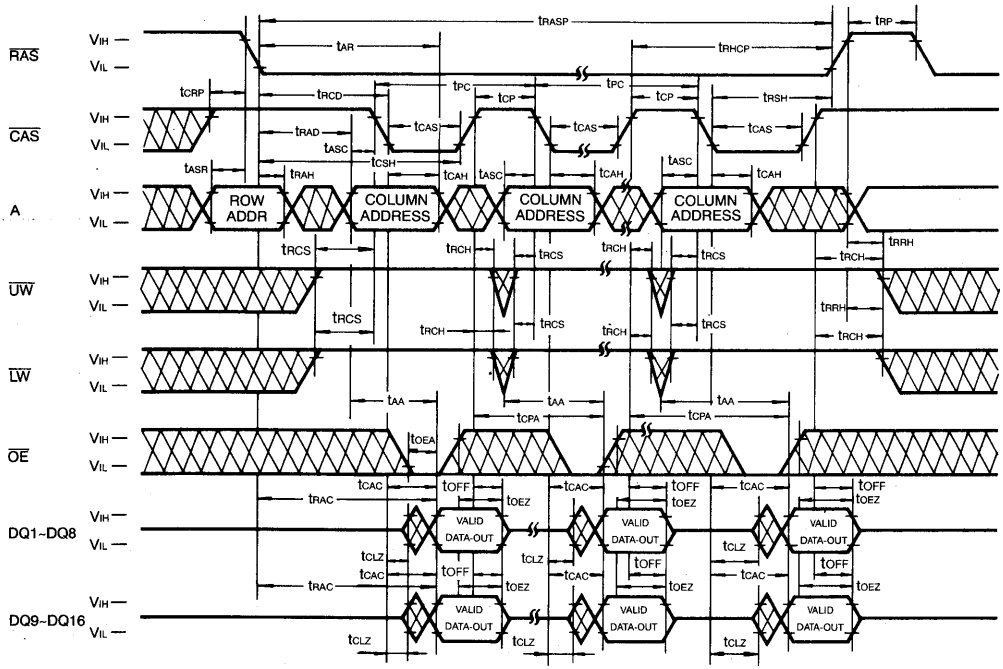
READ-MODIFY-UPPER-BYTE-WRITE CYCLE



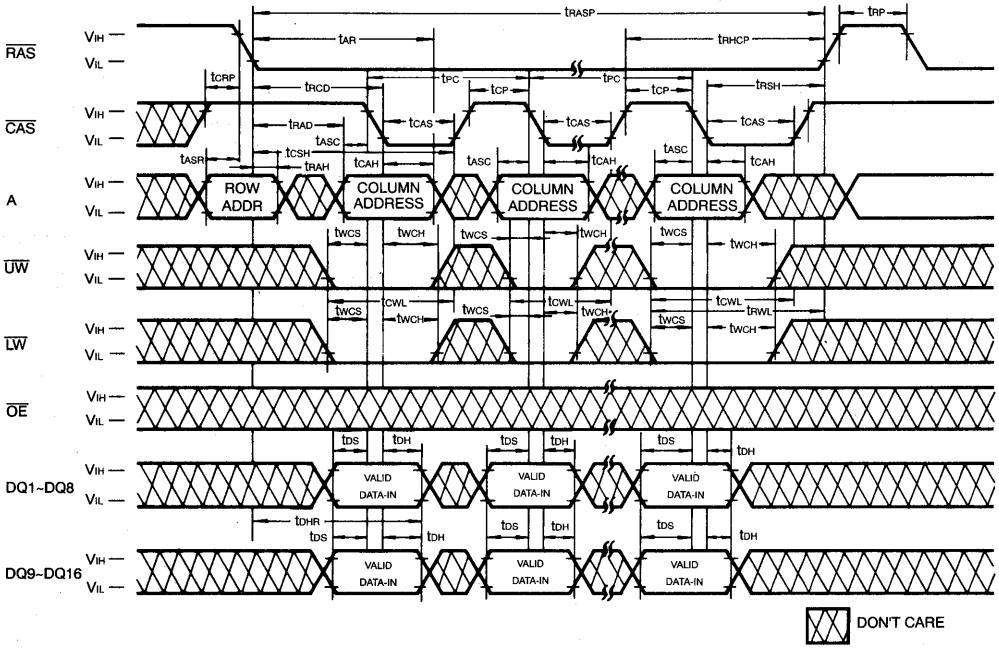
READ-MODIFY-LOWER-BYTE-WRITE CYCLE



FAST PAGE MODE WORD READ CYCLE



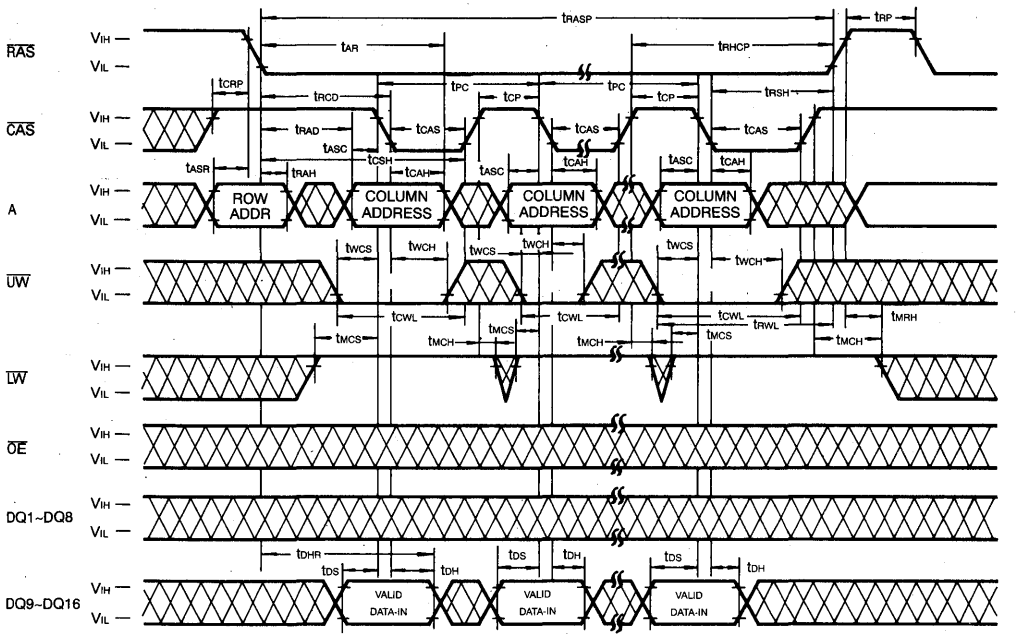
FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)



SAMSUNG ELECTRONICS

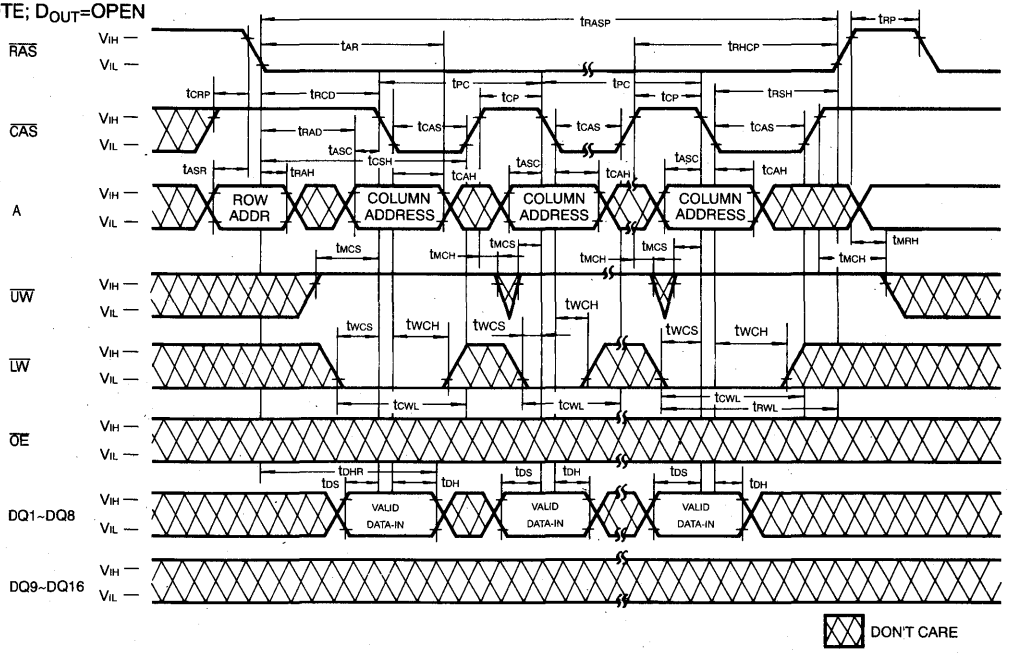
FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE; D_{OUT}=OPEN

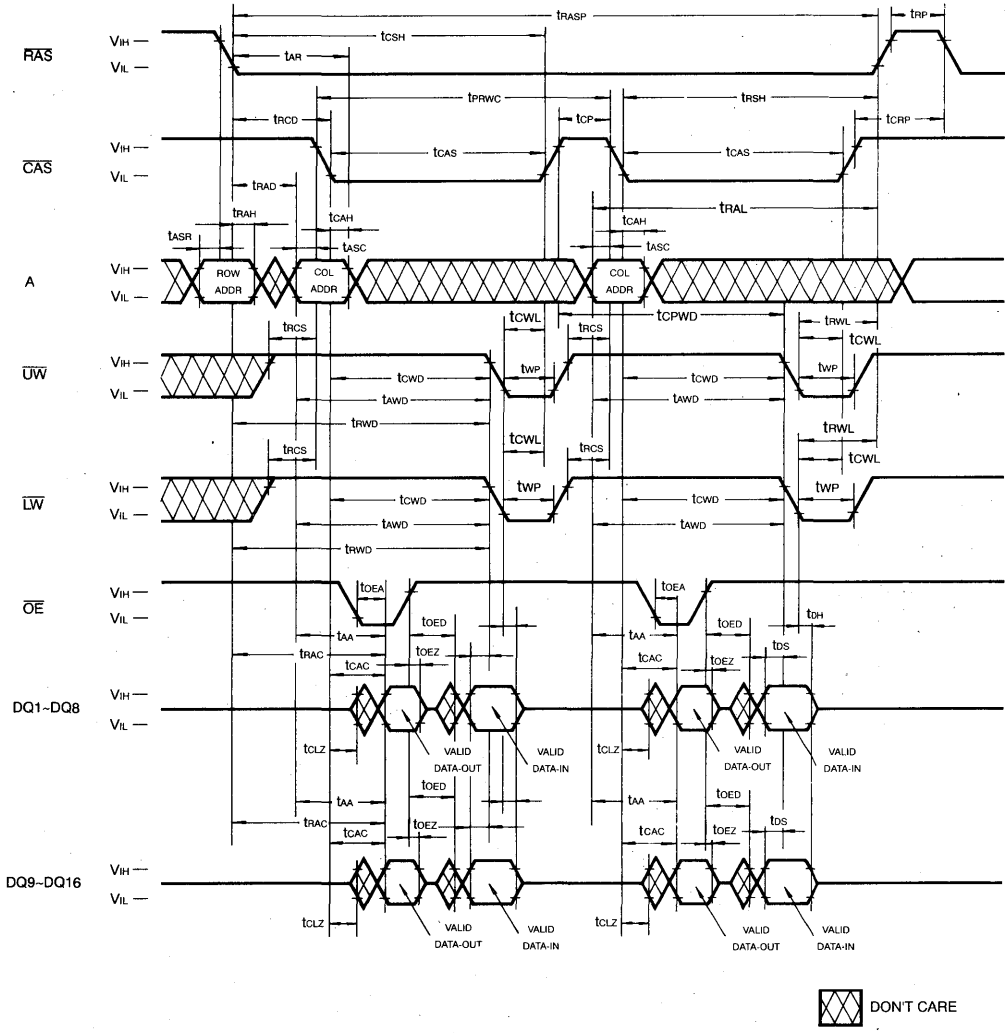


FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE; D_{OUT}=OPEN

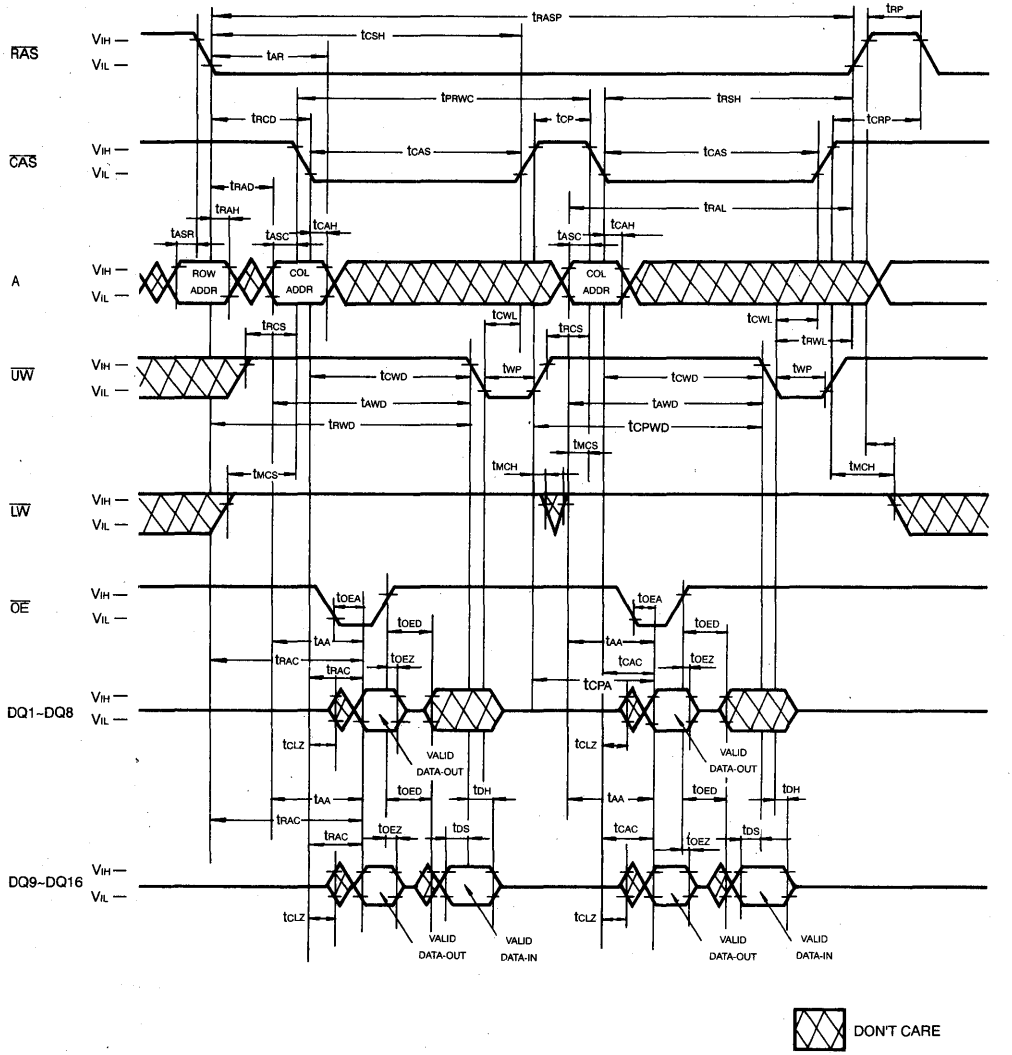


FAST PAGE MODE READ-MODIFY- WRITE CYCLE

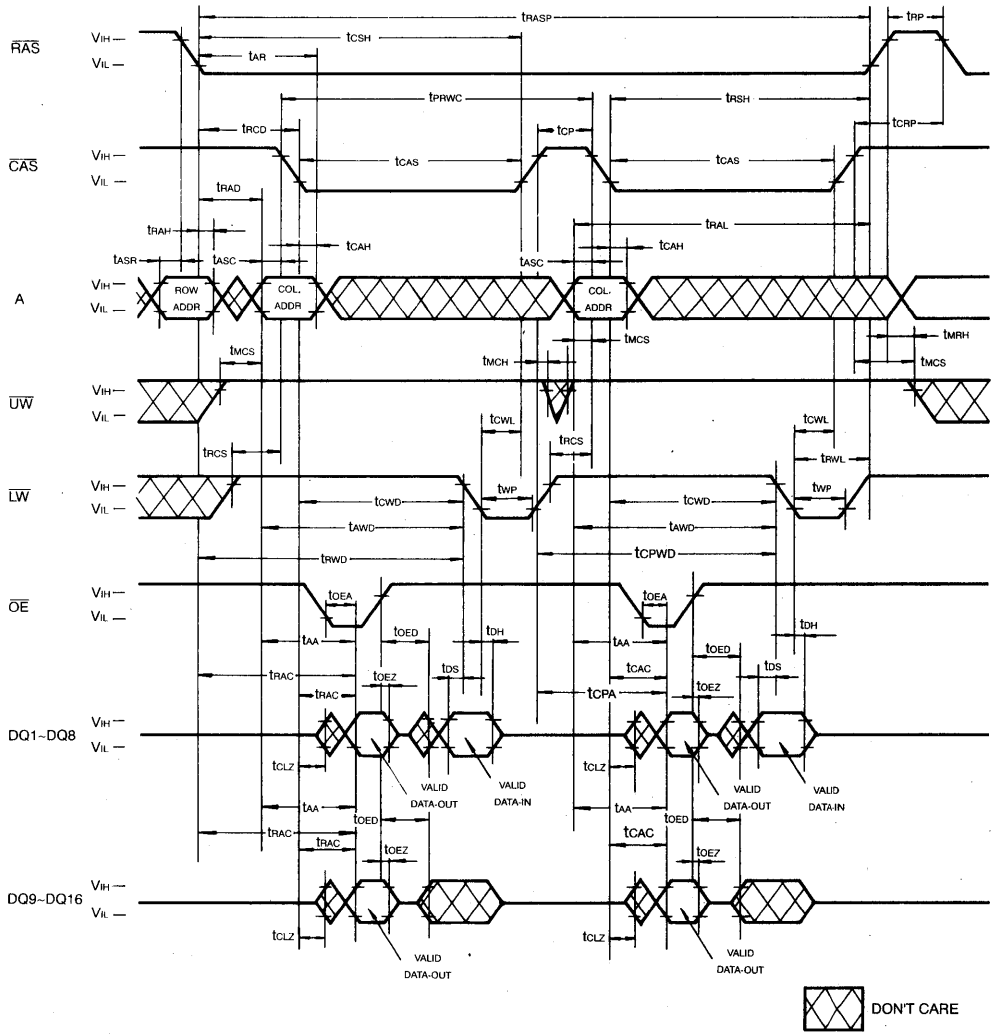


SAMSUNG ELECTRONICS

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE

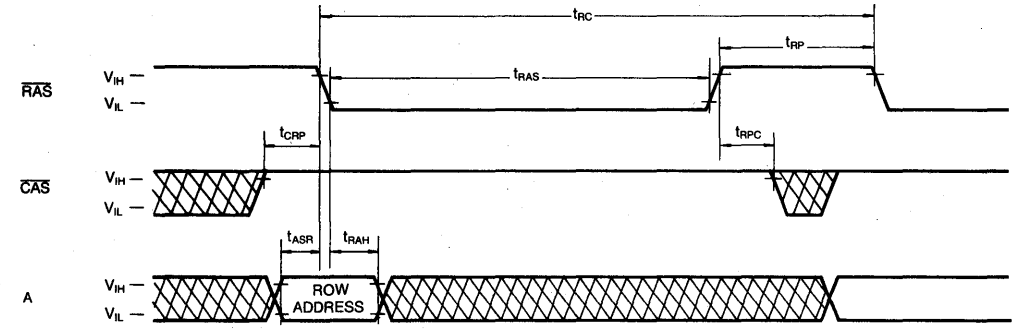


FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



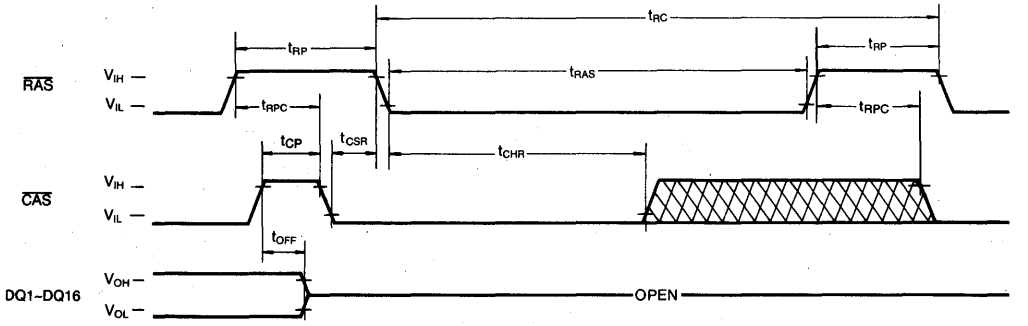
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE; $\overline{UW}$, $\overline{LW}$, $\overline{OE}$, D_{IN}=Don't Care D_{OUT}=OPEN



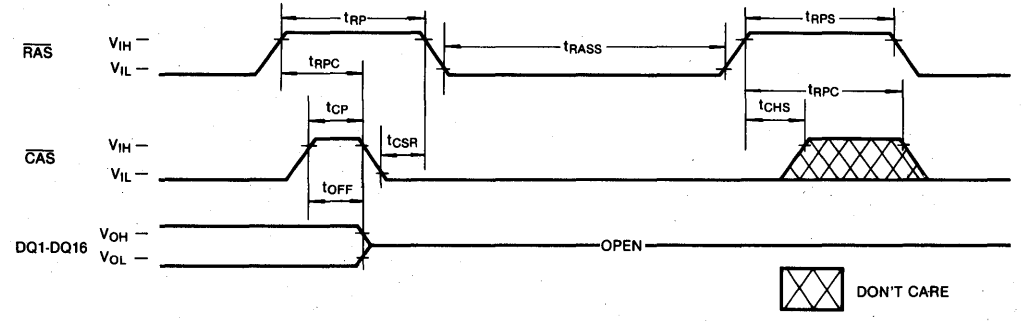
$\overline{CAS}$-before-$\overline{RAS}$ REFRESH CYCLE

NOTE; $\overline{UW}$, $\overline{LW}$, $\overline{OE}$, A=Don't Care

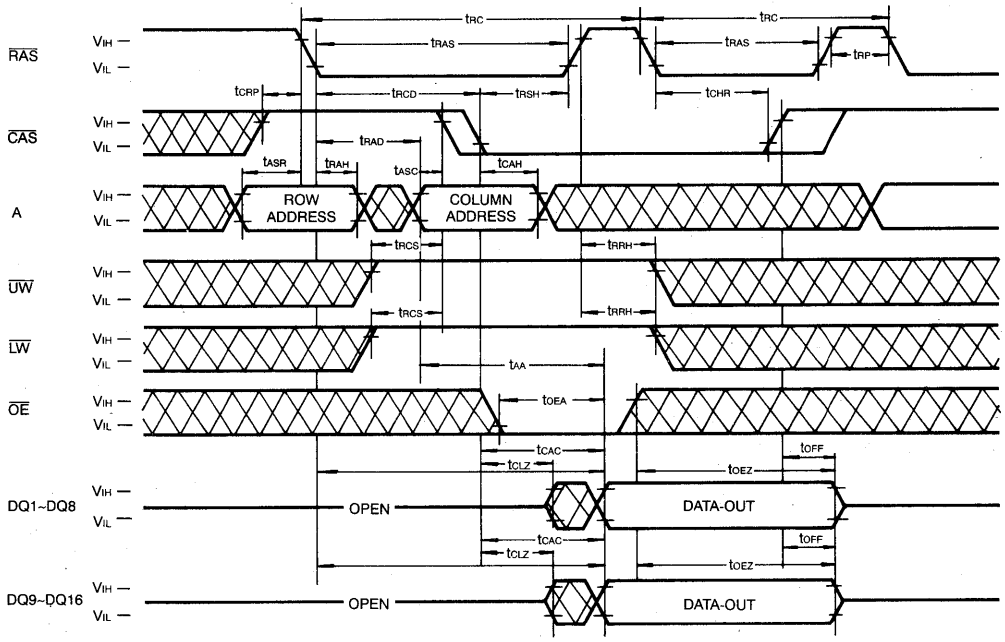


$\overline{CAS}$-before-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

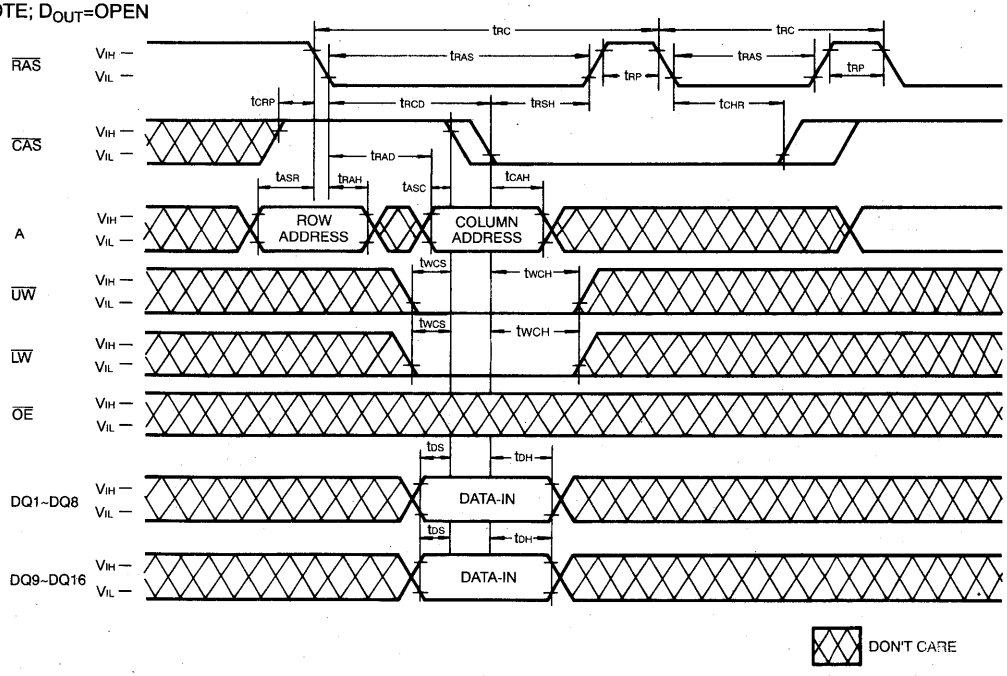


HIDDEN REFRESH CYCLE (READ)



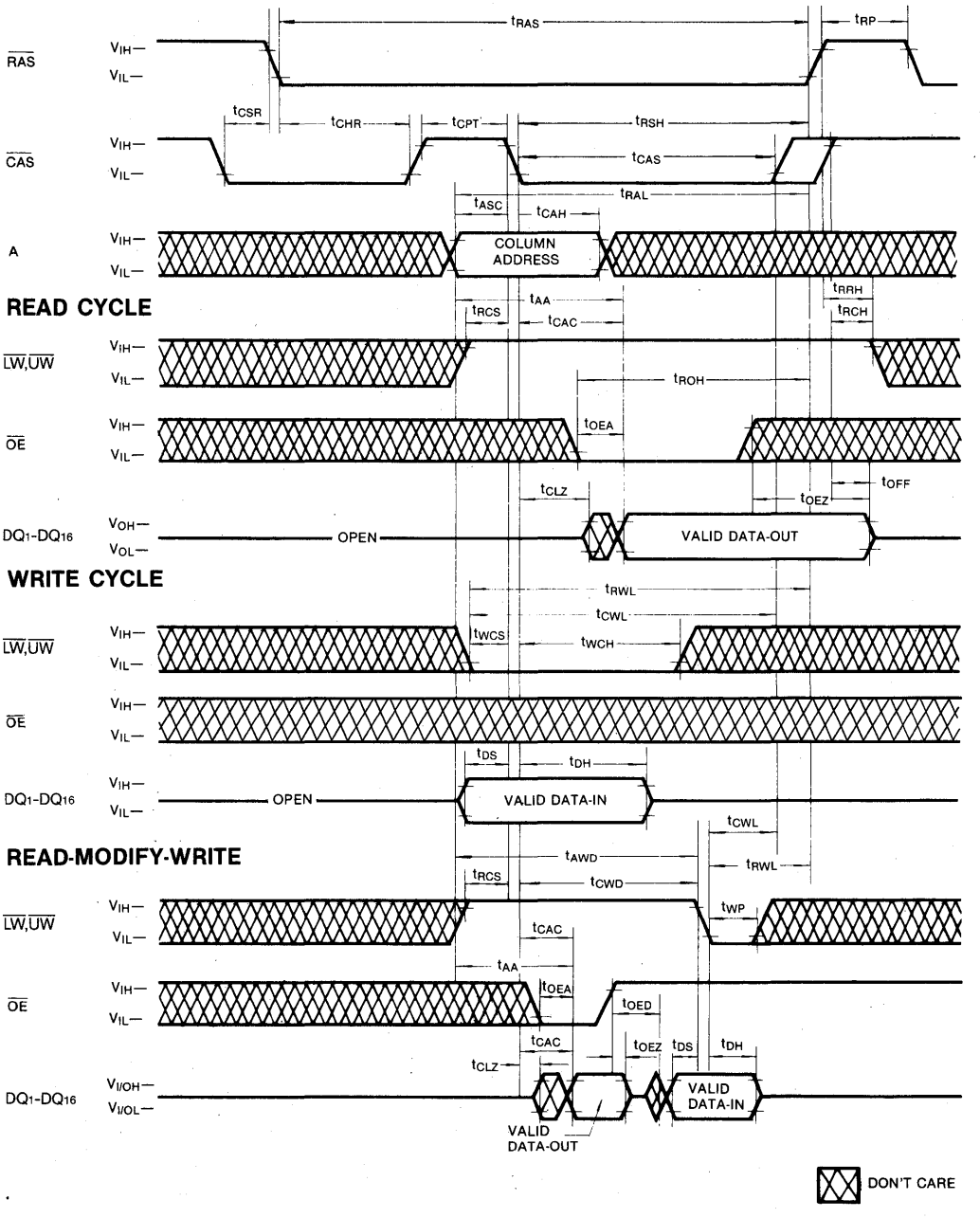
HIDDEN REFRESH CYCLE (WRITE)

NOTE; D_{OUT}=OPEN



TIMING DIAGRAMS (Continued)

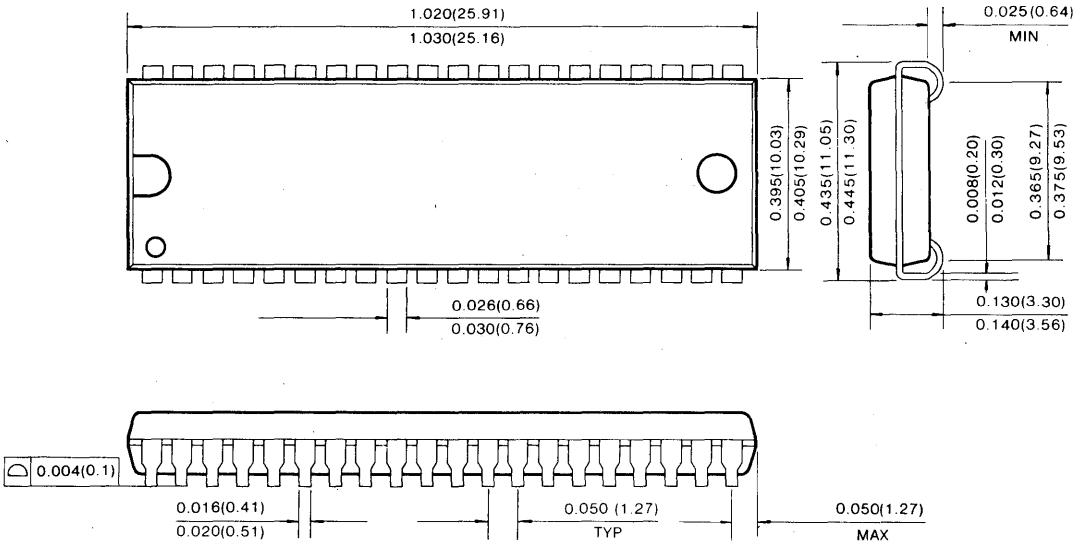
CAS-before-RAS REFRESH COUNTER TEST CYCLE



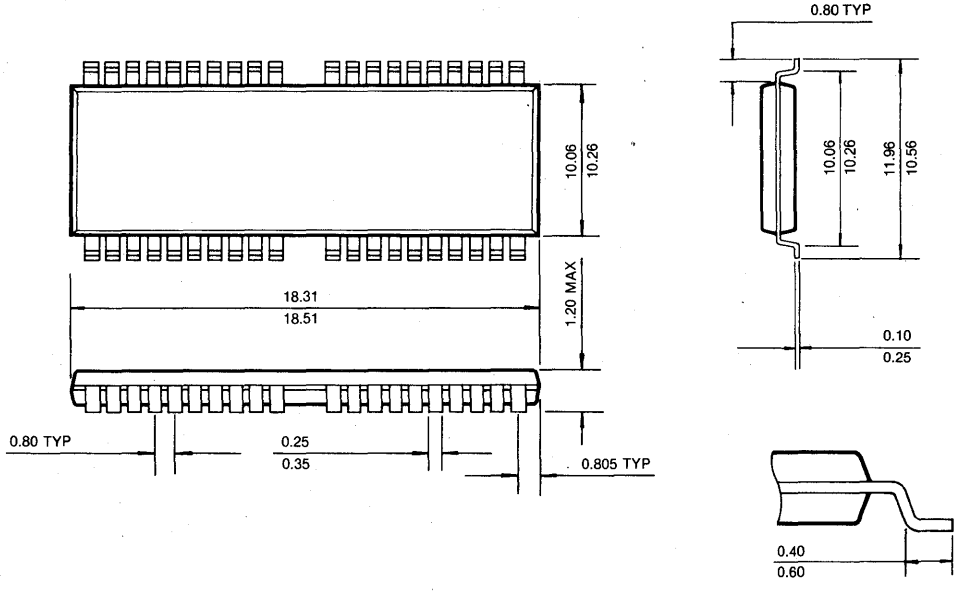
PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)



256K × 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM416C157B/BL/BLL-5	50ns	15ns	90ns
KM416C157B/BL/BLL-6	60ns	15ns	110ns
KM416C157B/BL/BLL-7	70ns	20ns	130ns
KM416C157B/BL/BLL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Byte Write operation(2W)**
- **Word Read/Write operation**
- **CAS-before-RAS refresh capability**
- **RAS-only and Hidden Refresh capability**
- **RAS-only and Hidden Refresh capability**
- **Self Refresh operation (LL-version)**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +5V±10% power supply**
- **Refresh cycle**
  - **-1024 cycle/16ms (Normal)**
  - **-1024 cycle/128ms (L & LL-Ver)**
- **Power Dissipation**
  - **-Standby: 5.5mW (Normal)**
  - **1.1mW (L-version)**
  - **0.83mW (LL-version)**
  - **-Active (50/60/70/80): 470/385/360/330mW**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP (II)**

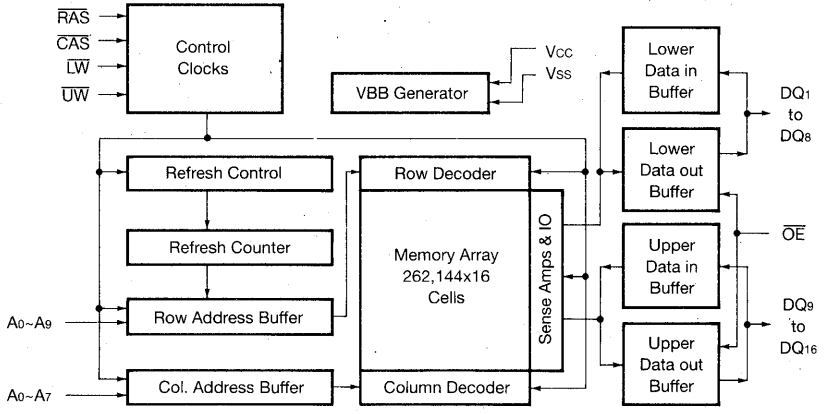
GENERAL DESCRIPTION

The Samsung KM416C157B/BL/BLL is a CMOS high speed 262,144 bit × 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance portable computers.

The KM416C157B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

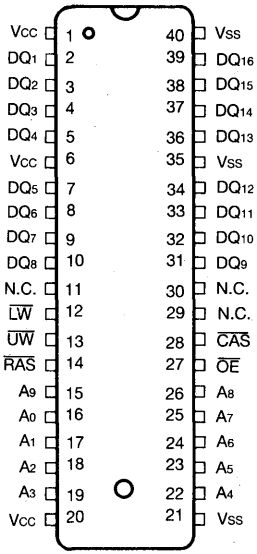
The KM416C157B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

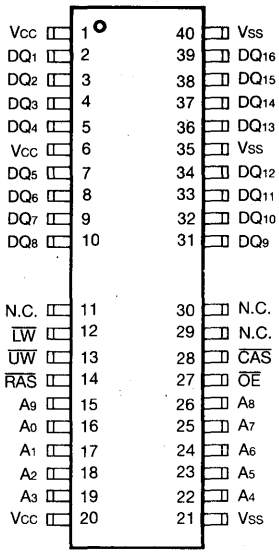


PIN CONFIGURATION (Top Views)

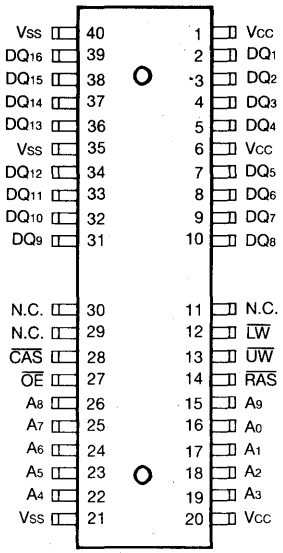
• KM416C157BJ/BLJ/BLLJ



• KM416C157BT/BLT/BLLT



• KM416C157BTR/BLTR/BLLTR



Pin Name	Pin Function
A0-A9	Address Inputs
DQ1~16	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{UW}$	Read/Upper Byte Write Input
$\overline{LW}$	Read/Lower Byte Write Input
$\overline{OE}$	Data Output Enable
VCC	Power(+5V)
N.C.	No Connection

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} +1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM416C157B/BL/BLL-5	I_{CC1}	-	85	mA
	KM416C157B/BL/BLL-6			70	mA
	KM416C157B/BL/BLL-7			65	mA
	KM416C157B/BL/BLL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{UW}$=$\overline{LW}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM416C157B/BL/BLL-5	I_{CC3}	-	85	mA
	KM416C157B/BL/BLL-6			70	mA
	KM416C157B/BL/BLL-7			65	mA
	KM416C157B/BL/BLL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM416C157B/BL/BLL-5	I_{CC4}	-	65	mA
	KM416C157B/BL/BLL-6			55	mA
	KM416C157B/BL/BLL-7			50	mA
	KM416C157B/BL/BLL-8			45	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{UW}$=$\overline{LW}$=V_{CC}-0.2V)	KM416C157B	I_{CC5}	-	1	mA
	KM416C157BL			200	μA
	KM416C157BLL			150	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM416C157B/BL/BLL-5	I_{CC6}	-	85	mA
	KM416C157B/BL/BLL-6			70	mA
	KM416C157B/BL/BLL-7			65	mA
	KM416C157B/BL/BLL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=0.2V D_{IN}=Don't Care, T_{RC}=125μS(L-ver.), T_{RAS}=T_{RAS} min.~300ns	KM416C157BL	I_{CC7}	-	300	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{xW}$=$\overline{OE}$=A_0-A_9=V_{CC}-0.2V or 0.2V	KM416C157BLL	I_{CCS}		200	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{LW}$, $\overline{UW}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5V±10%, See notes 1,2)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	135		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	35	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	

* 50ns Product : V_{CC}=5V±5%, Cout=50pF

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		50		55		ns	6
Write command pulse width	t_{WP}	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		16		16		16		16	ms	
Refresh period (L,LL-Version)	t_{REF}		128		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{LW}$, $\overline{UW}$ delay time	t_{CWD}	40		40		50		50		ns	8
$\overline{RAS}$ to $\overline{LW}$, $\overline{UW}$ delay time	t_{RWD}	75		85		95		105		ns	8
Column address to $\overline{LW}$, $\overline{UW}$ delay time	t_{AWD}	50		55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	55		60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	80		80		95		100		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	20	ns	7
$\overline{OE}$ commend hold time	t_{OEH}	15		15		20		20		ns	

*50ns Product : V_{CC}=5V±5%, Cout=50pF

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Masked write set-up time	t_{MCS}	0		0		0		0		ns	
Masked write hold time referenced to $\overline{RAS}$	t_{MRH}	0		0		0		0		ns	
Masked write hold time referenced to $\overline{CAS}$	t_{MCH}	0		0		0		0		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		100		100		100		μs	
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	-50		-50		-50		-50		ns	12

* 50ns Product : V_{CC}=5V$\pm$5%, Cout=50pF

KM416C157B Truth Table

$\overline{RAS}$	$\overline{CAS}$	$\overline{UW}$	$\overline{LW}$	$\overline{OE}$	DQ_1~DQ_8	DQ_9~DQ_{16}	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	X	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	L	L	X	DQ-IN	DQ-IN	Word Write
L	L	H	L	X	DQ-IN	-	Byte Write
L	L	L	H	X	-	DQ-IN	Byte Write

4

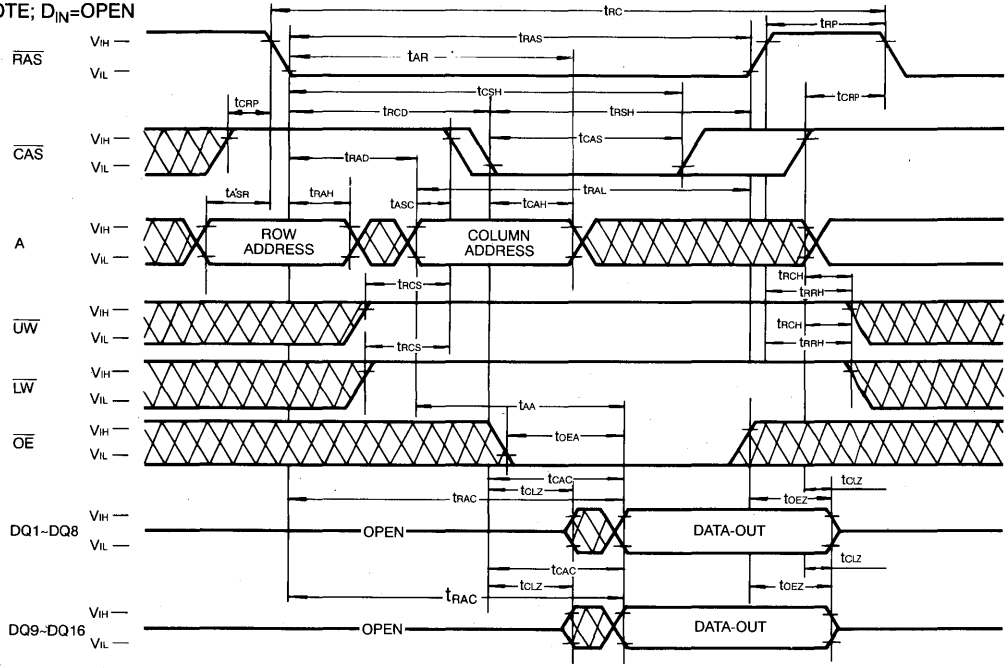
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. 1024 cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification
13. t_{RCS}, t_{MCS} are referenced to the later $\overline{W}$ rising edge at early write cycle.
14. t_{WCS} is referenced to the later $\overline{W}$ falling edge at early write cycle.
15. t_{CWL}, t_{RWL} are referenced to the later $\overline{W}$ falling edge at early write cycle.
16. t_{WCH}, t_{WP} are referenced to the earler $\overline{W}$ falling edge at early write cycle.
17. t_{RWD}, t_{AWD}, t_{CWD} are referenced to the earler $\overline{W}$ falling edge at Read-Modify-write cycle.

TIMING DIAGRAM

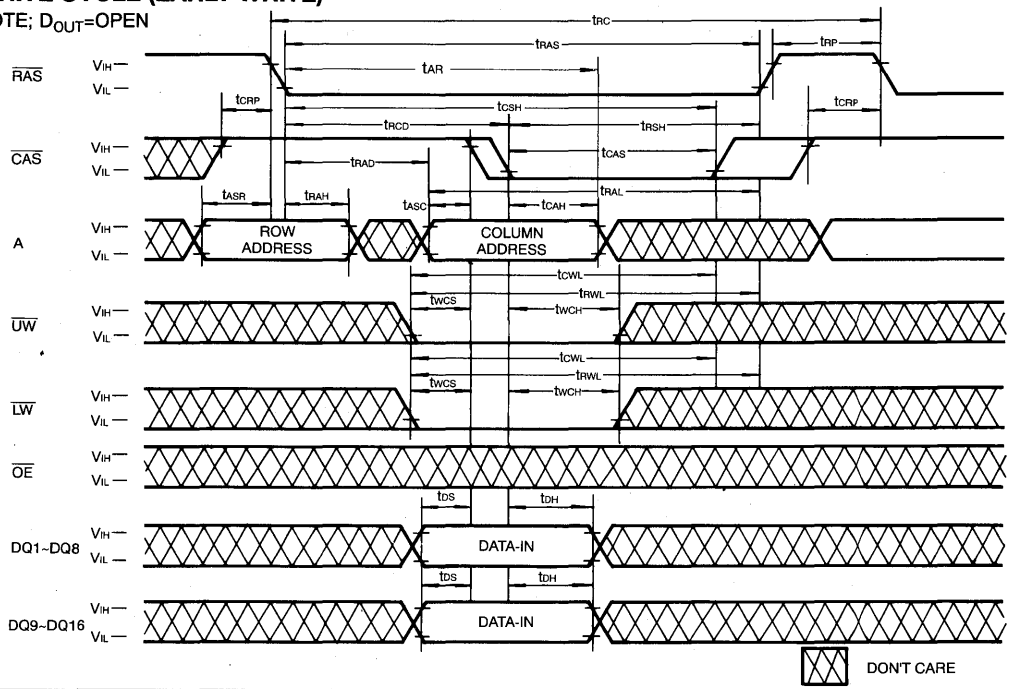
READ CYCLE

NOTE; D_{IN}=OPEN



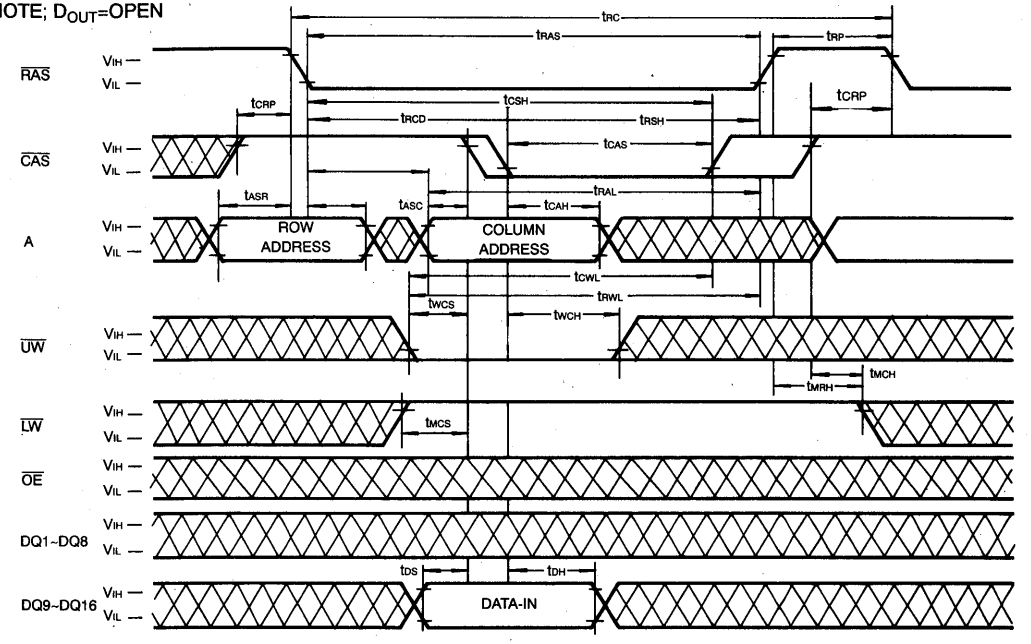
WRITE CYCLE (EARLY WRITE)

NOTE; D_{OUT}=OPEN



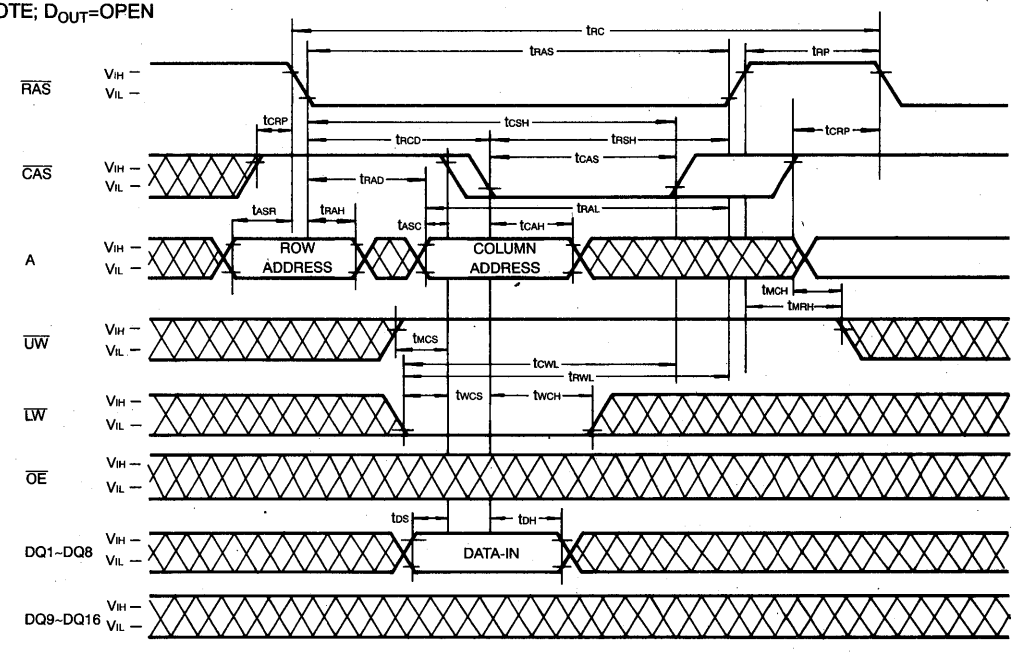
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE; D_{OUT}=OPEN



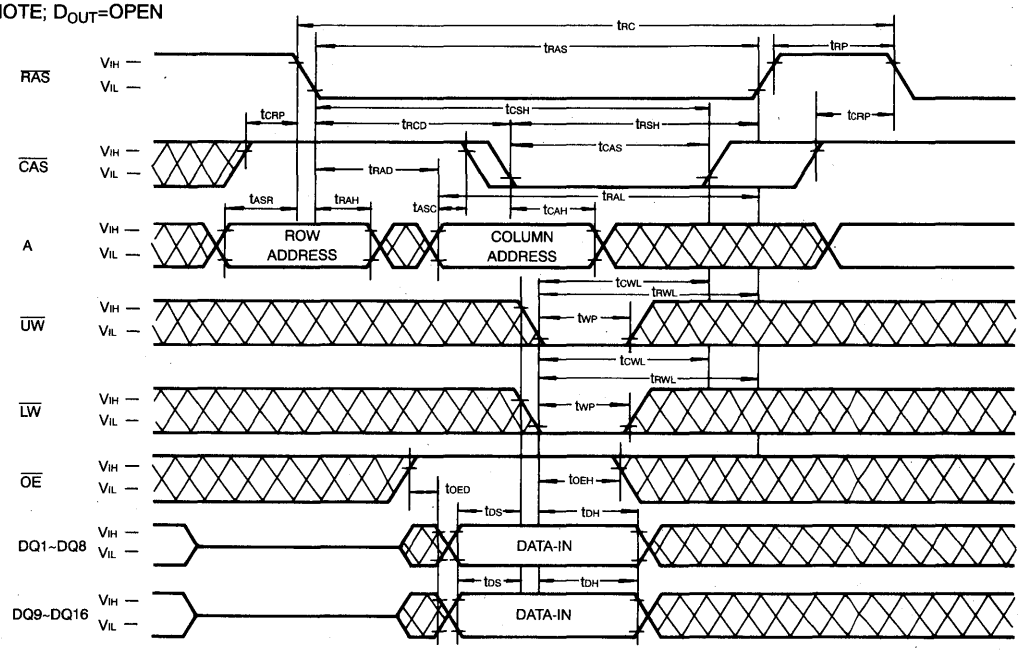
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE; D_{OUT}=OPEN



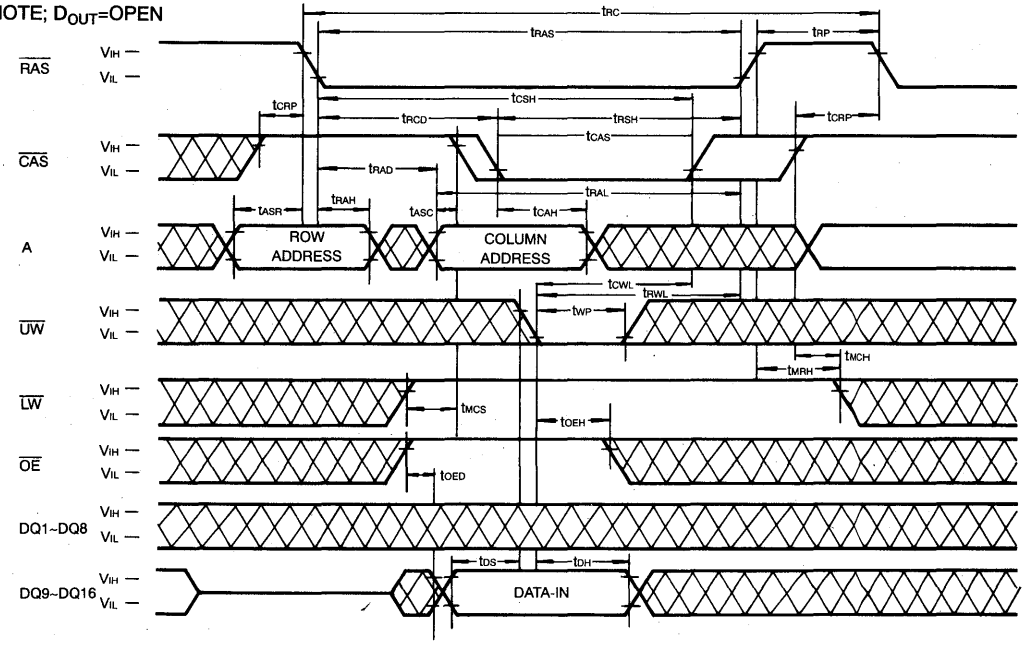
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE; D_{OUT}=OPEN



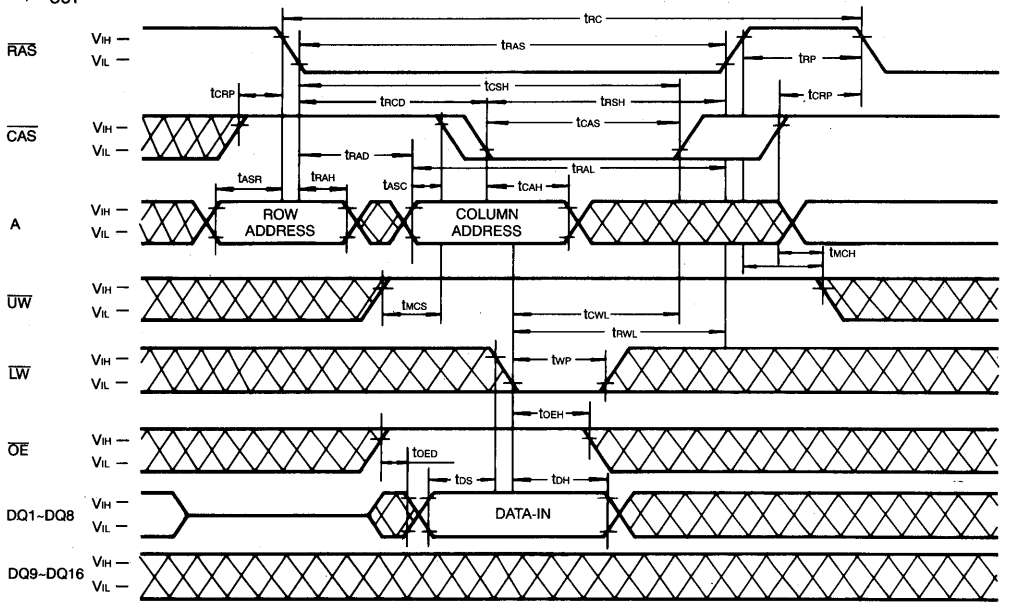
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE; D_{OUT}=OPEN

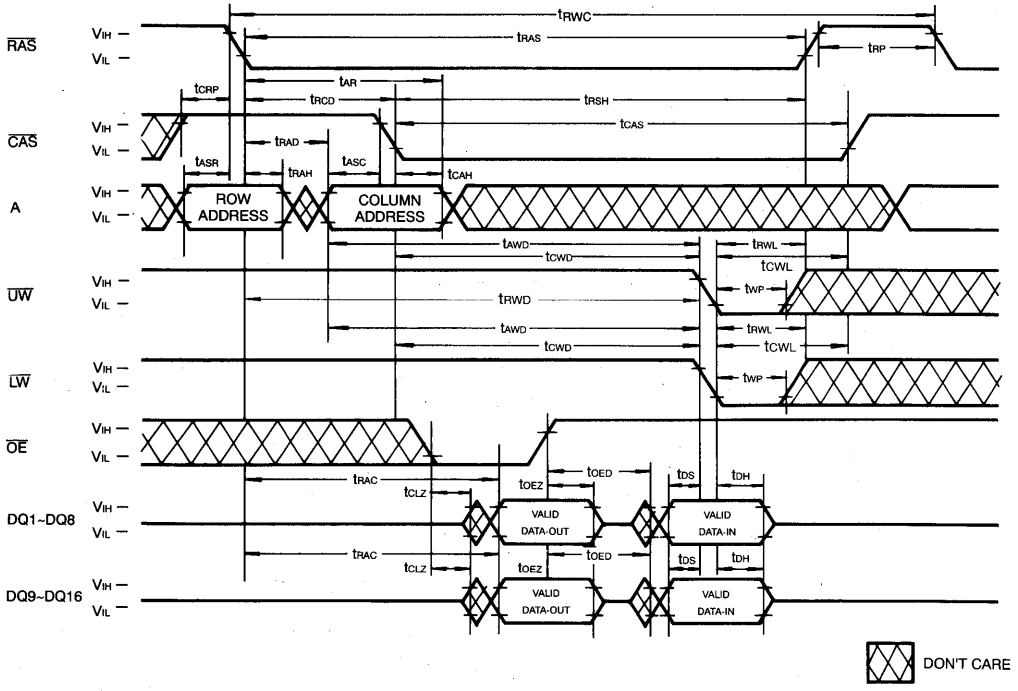


LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE; D_{OUT}=OPEN

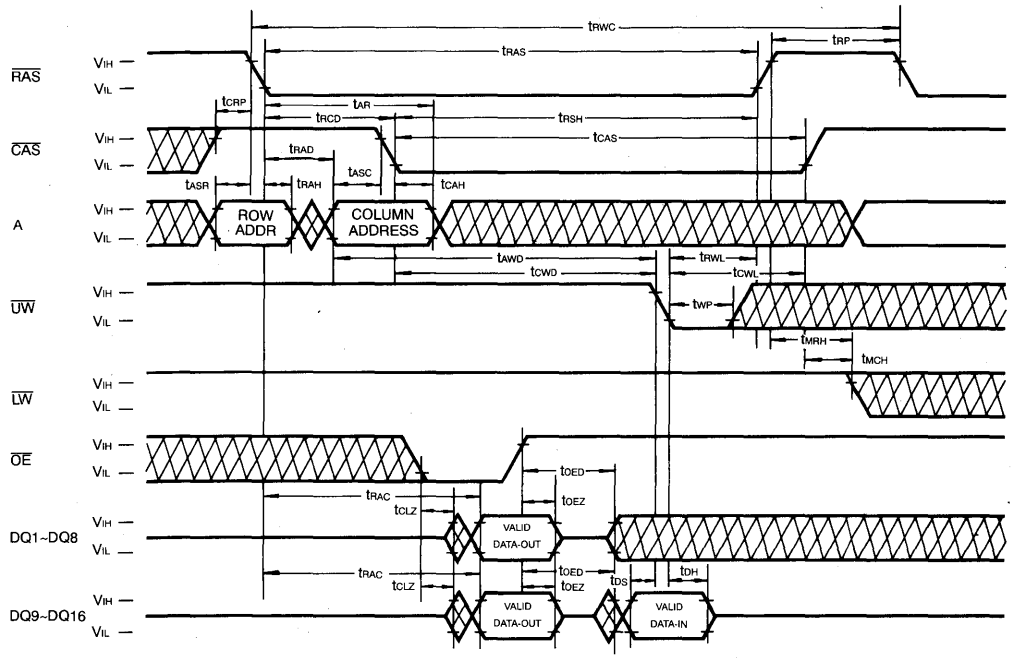


READ-MODIFY-WRITE CYCLE

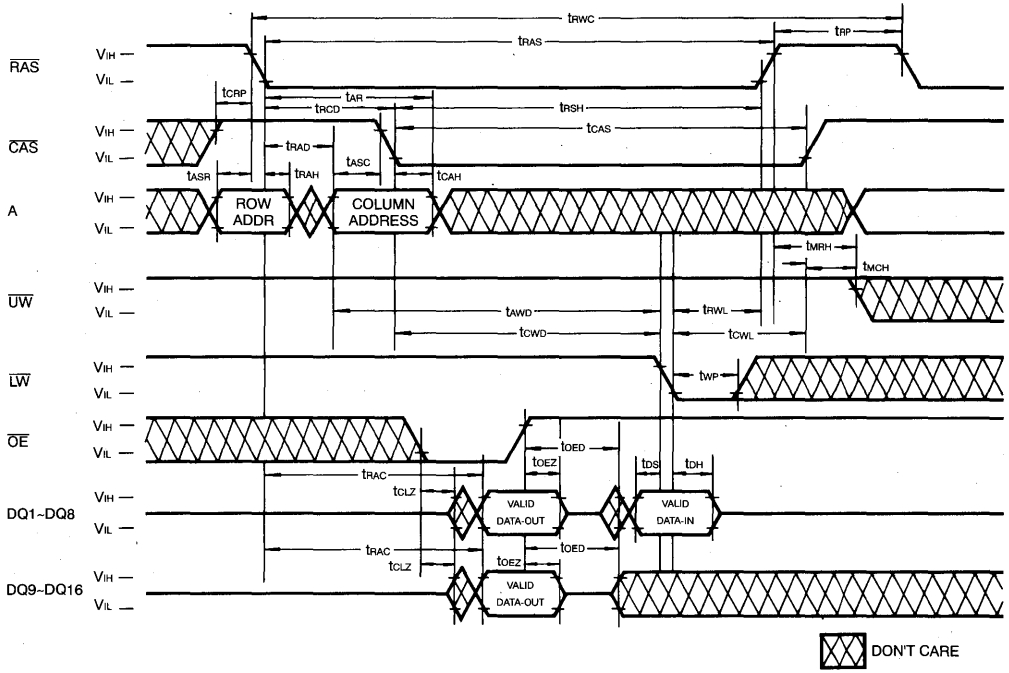


SAMSUNG ELECTRONICS

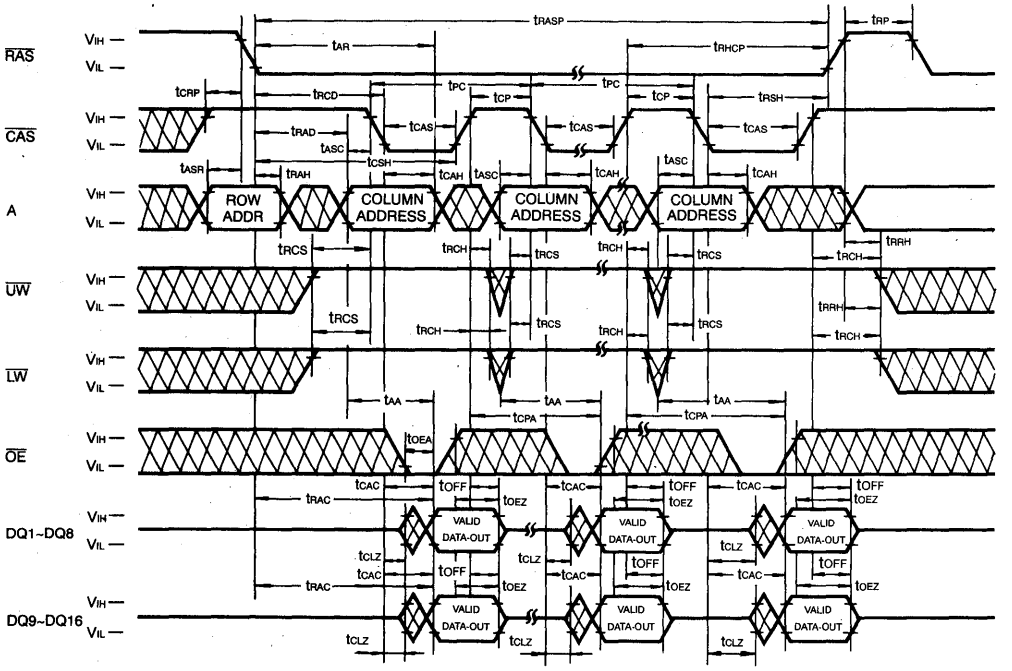
READ-MODIFY-UPPER-BYTE-WRITE CYCLE



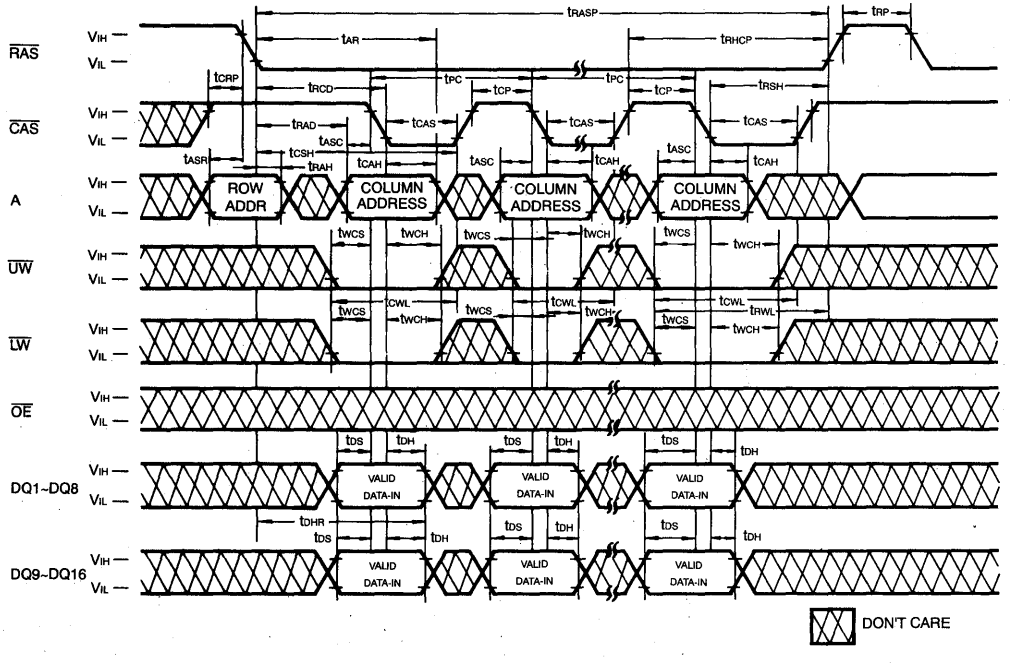
READ-MODIFY-LOWER-BYTE-WRITE CYCLE



FAST PAGE MODE WORD READ CYCLE

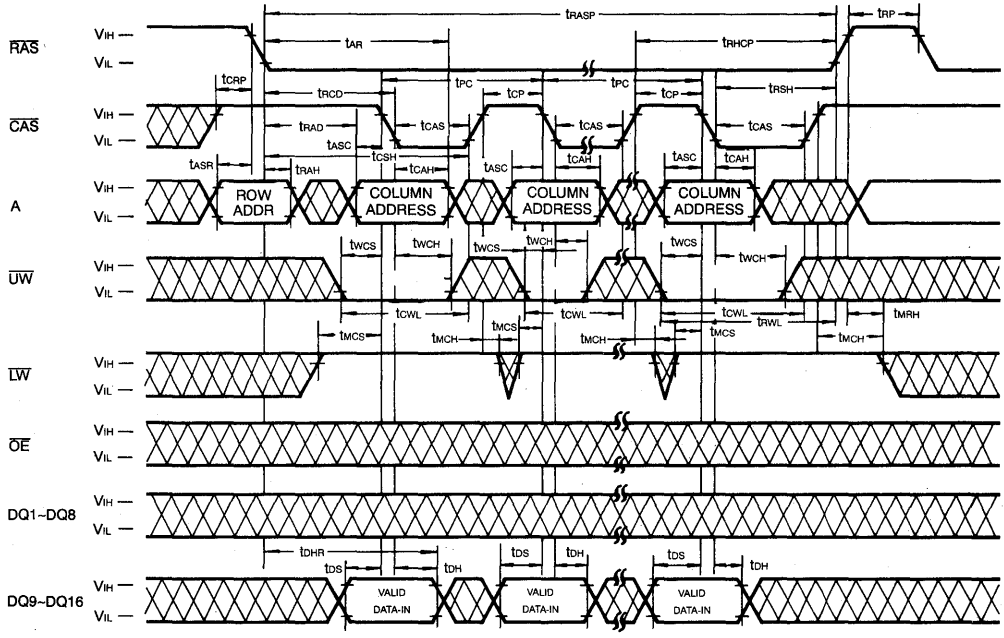


FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)



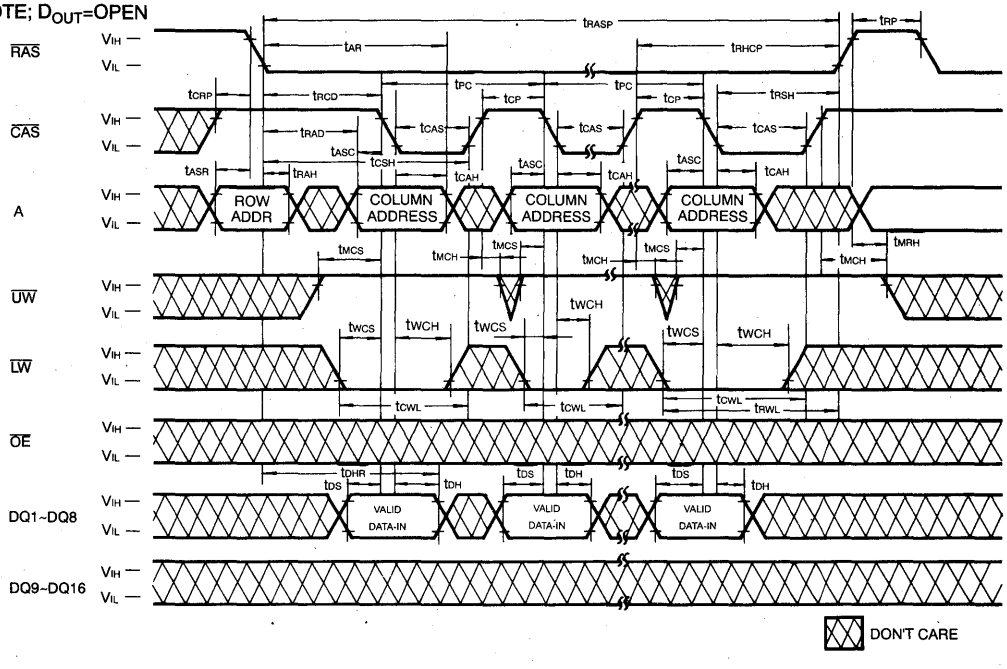
FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE; D_{OUT}=OPEN

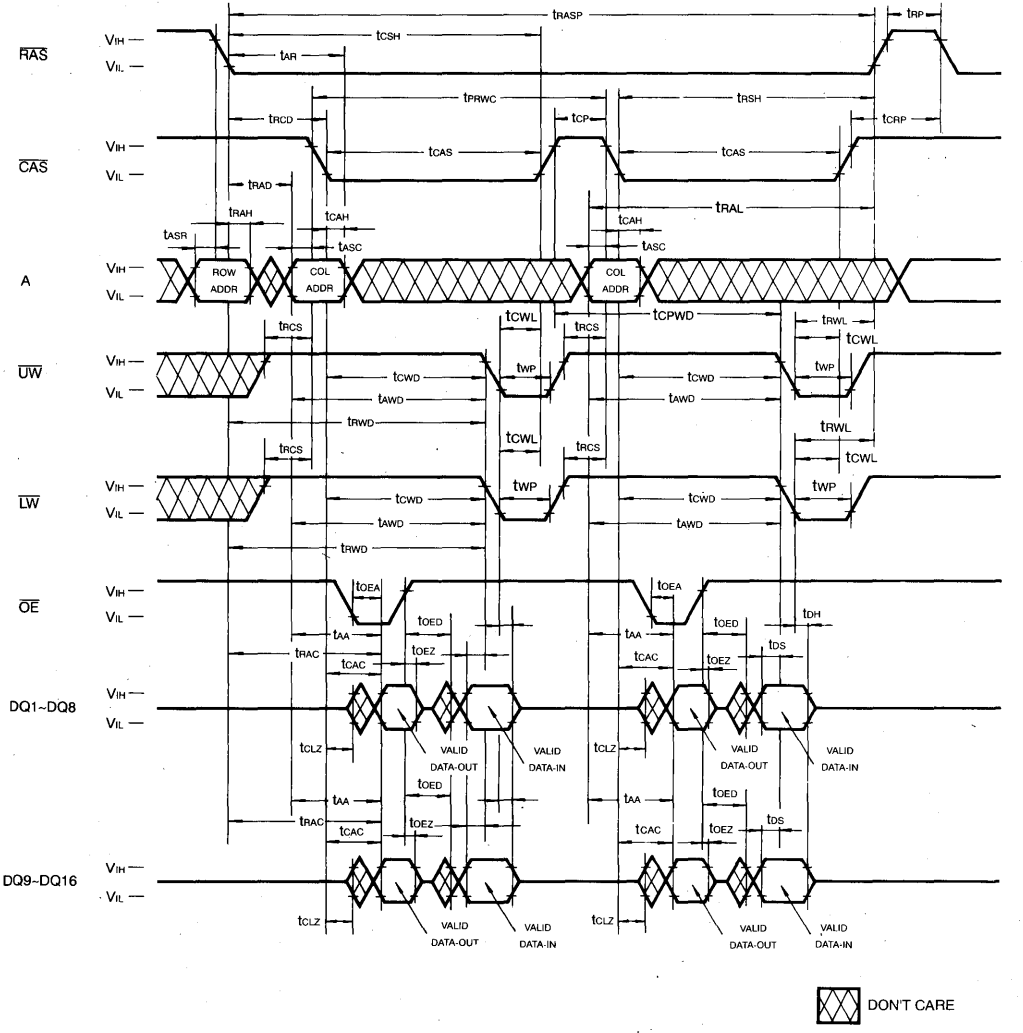


FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

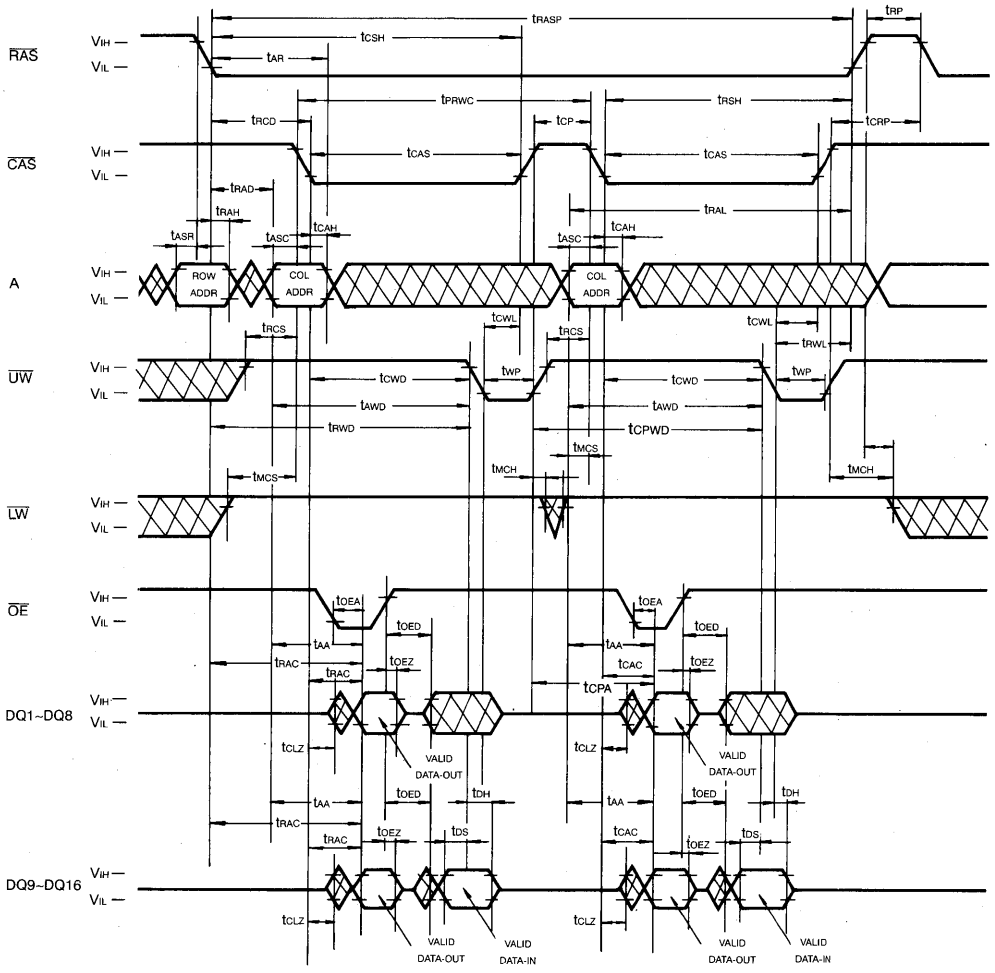
NOTE; D_{OUT}=OPEN



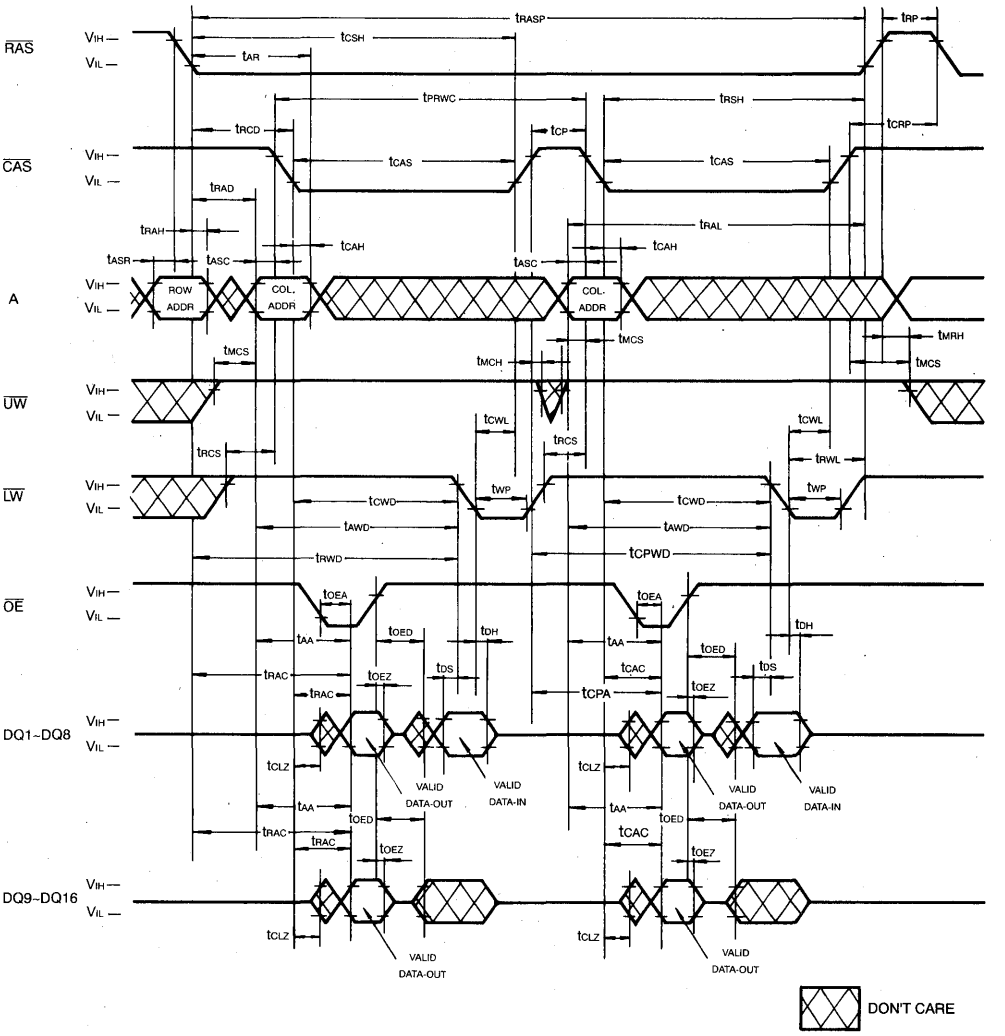
FAST PAGE MODE READ-MODIFY- WRITE CYCLE



FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE

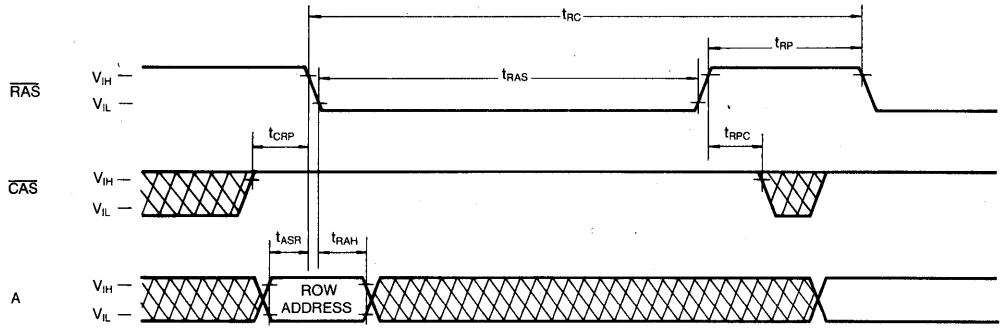


FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



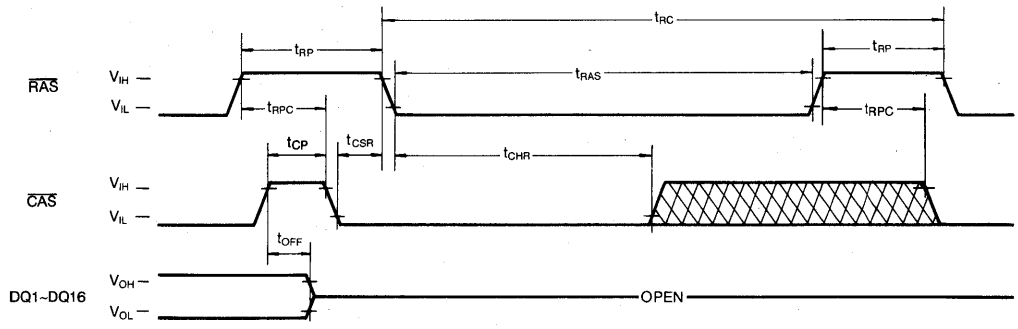
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE; $\overline{UW}$, $\overline{LW}$, $\overline{OE}$, D_{IN}=Don't Care D_{OUT}=OPEN



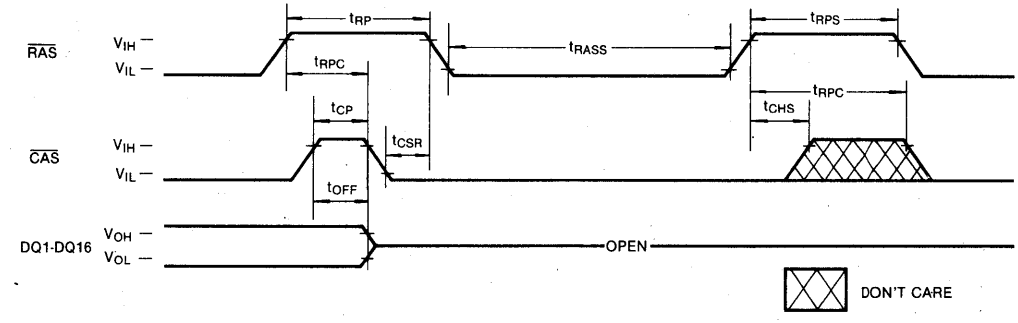
$\overline{CAS}$-before-$\overline{RAS}$ REFRESH CYCLE

NOTE; $\overline{UW}$, $\overline{LW}$, $\overline{OE}$, A=Don't Care

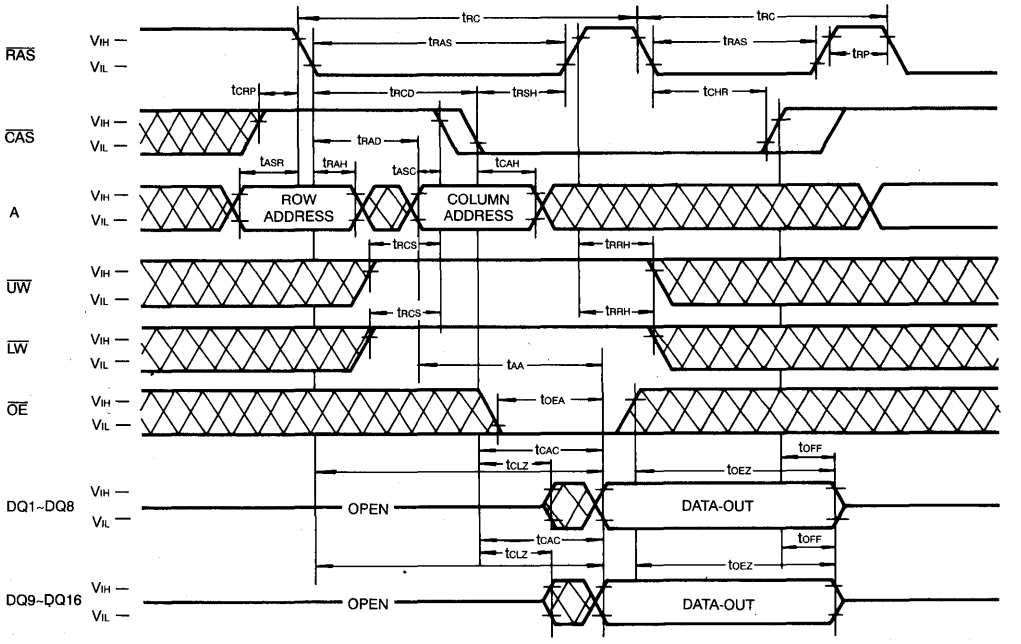


$\overline{CAS}$-before-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

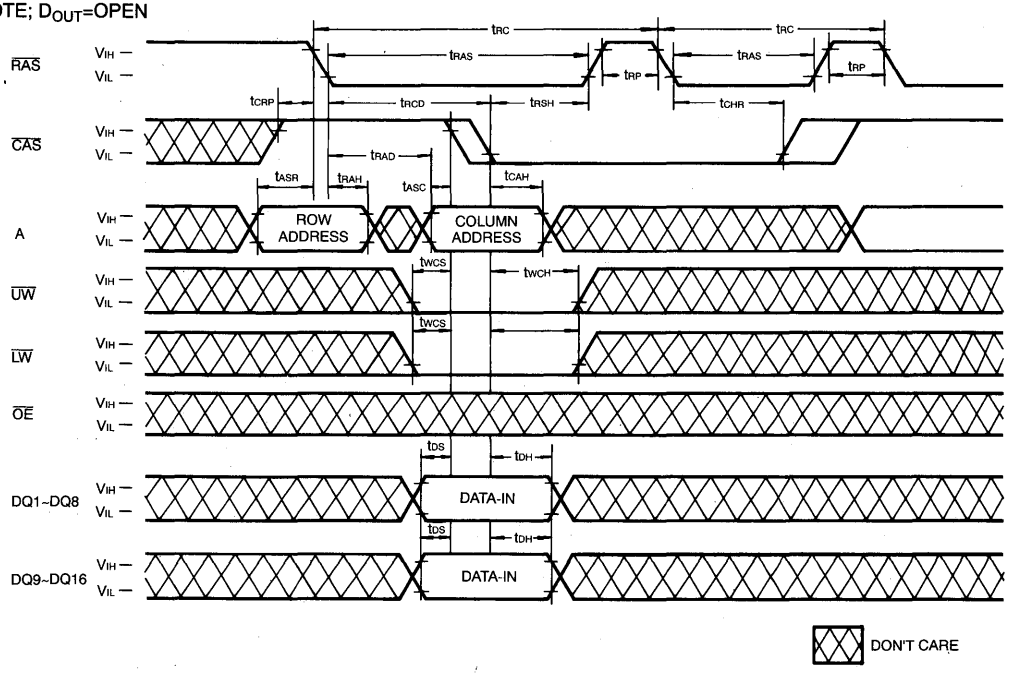


HIDDEN REFRESH CYCLE (READ)



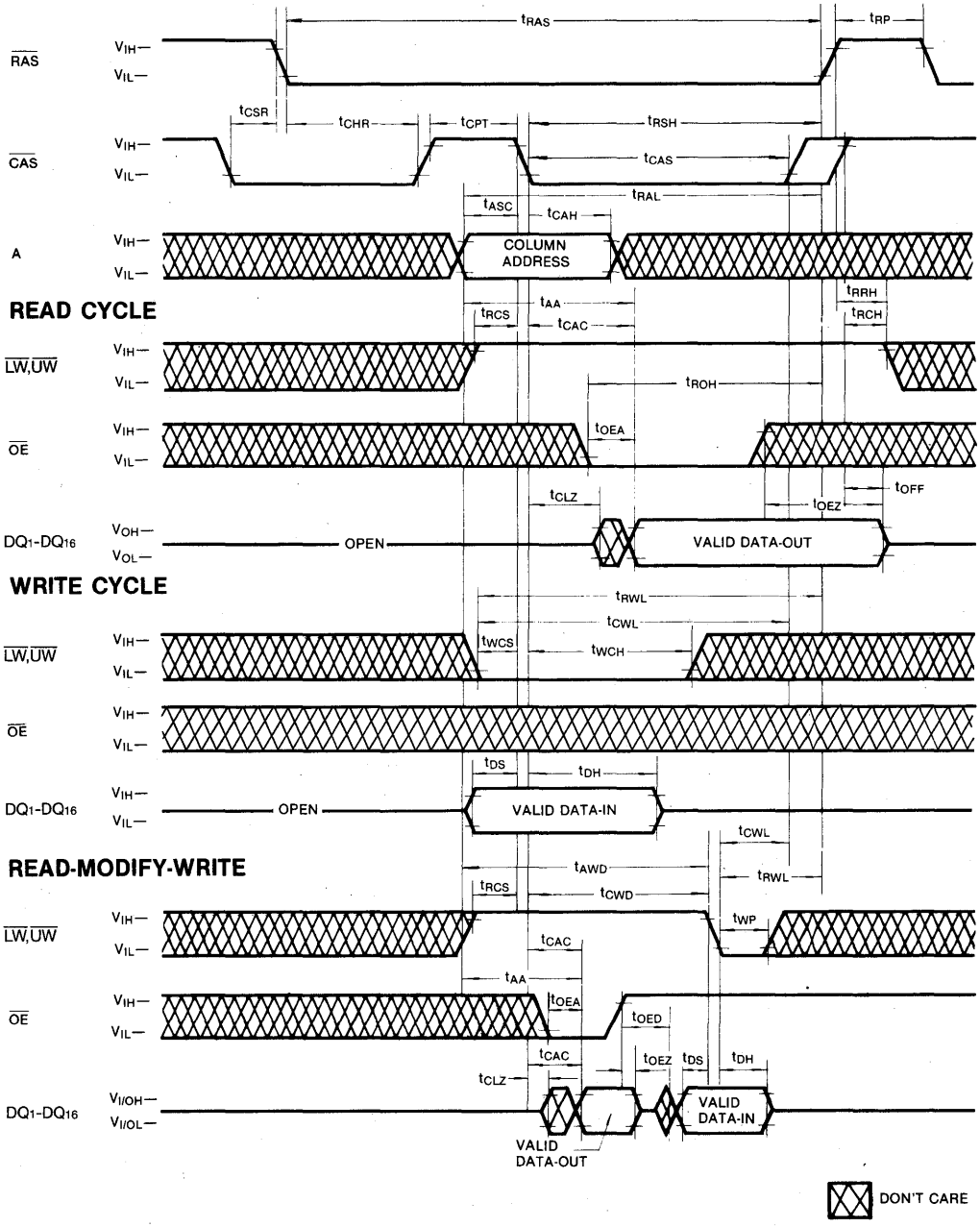
HIDDEN REFRESH CYCLE (WRITE)

NOTE; D_{OUT}=OPEN



TIMING DIAGRAMS (Continued)

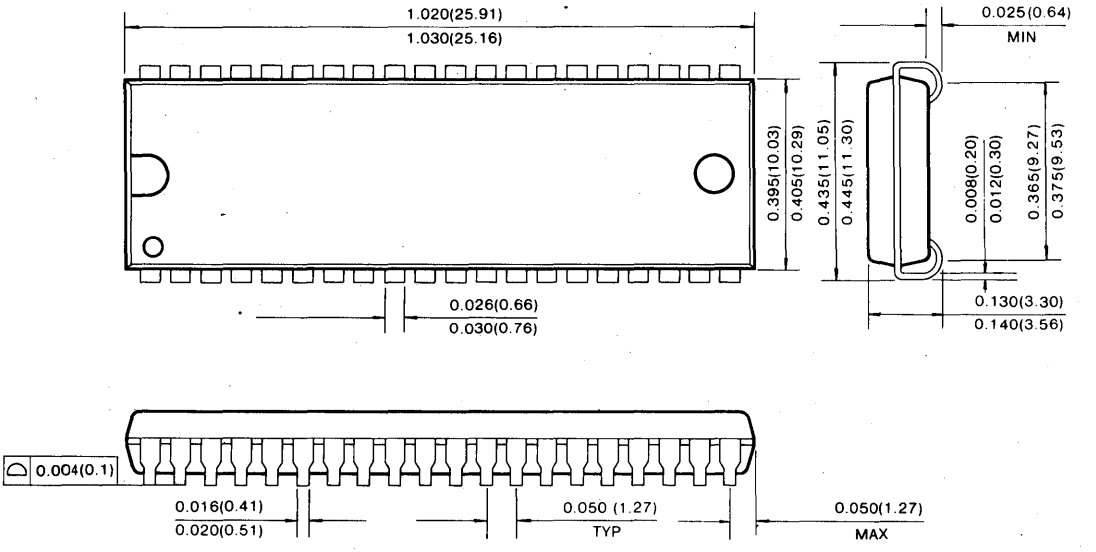
$\overline{CAS}$-before-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



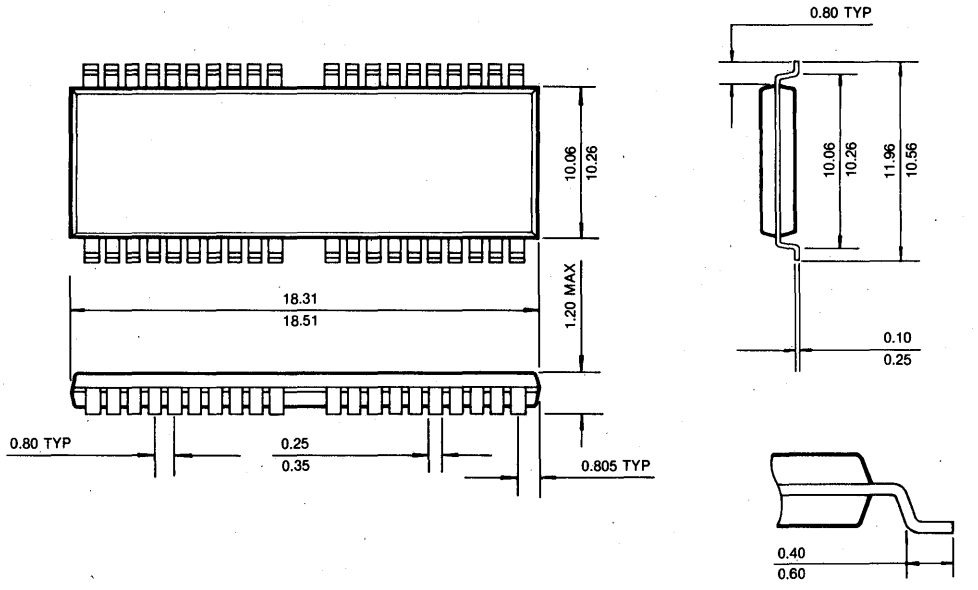
PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)



256K × 18 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM418C256B/BL/BLL-6	60ns	15ns	110ns
KM418C256B/BL/BLL-7	70ns	20ns	130ns
KM418C256B/BL/BLL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Self Refresh operation (LL-version)**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +5.0V±10% power supply**
- **Refresh Cycle**
  - **-512 cycle/8ms (Normal)**
  - **-512 cycle/64ms (L-version)**
  - **-512 cycle/128ms (LL-version)**
- **Power Dissipation**
  - **-Standby: 5.5mW (Normal)**
  - **1.1mW (L-version)**
  - **0.83mW (LL-version)**
  - **-Active (60/70/80): 525/470/440mW**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP II**

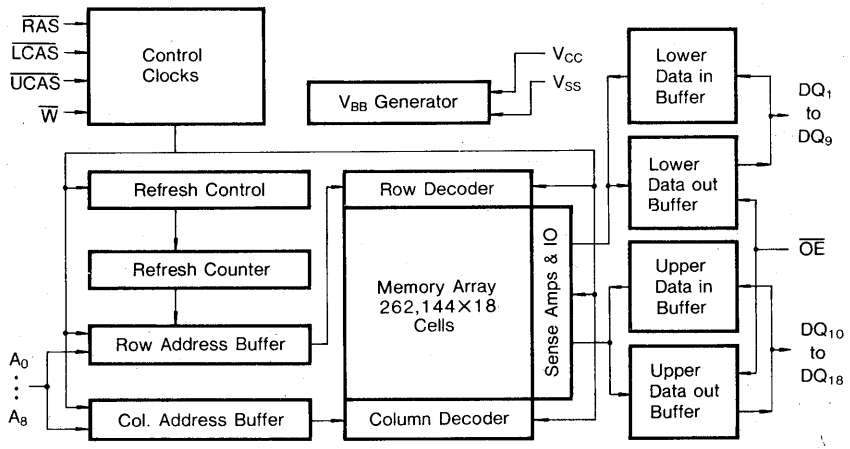
GENERAL DESCRIPTION

The Samsung KM418C256B/BL/BLL is a CMOS high speed 262,144 bit × 18 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM418C256B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

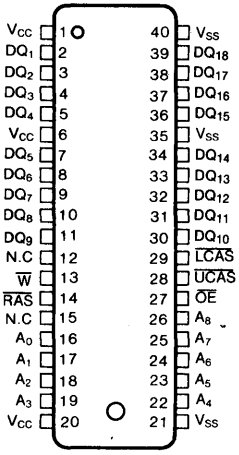
The KM418C256B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



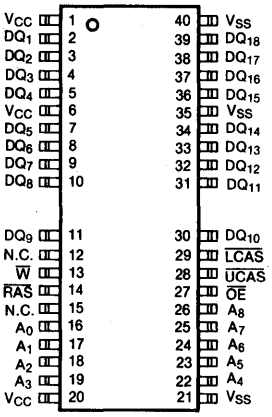
PIN CONFIGURATION (Top Views)

• **KM418C256BJ/BLJ/BLLJ**



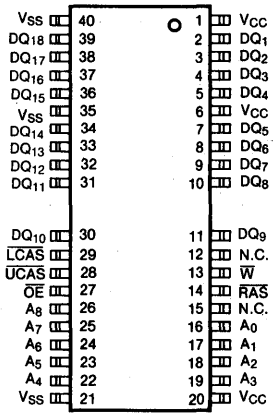
(SOJ)

• **KM418C256BT/BLT/BLLT**



(TSOP(II)-Forward Type)

• **KM418C256BTR/BLTR/BLLTR**



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A_0-A_8	Address Inputs
DQ_{1-18}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe

Pin Name	Pin Function
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power (+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{RC}=min.)	KM418C256B/BL/BLL-6 KM418C256B/BL/BLL-7 KM418C256B/BL/BLL-8	I_{CC1}	-	95 85 80	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH},$\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM418C256B/BL/BLL-6 KM418C256B/BL/BLL-7 KM418C256B/BL/BLL-8	I_{CC3}	-	95 85 80	mA mA mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC}=min.)	KM418C256B/BL/BLL-6 KM418C256B/BL/BLL-7 KM418C256B/BL/BLL-8	I_{CC4}	-	60 55 50	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)	KM418C256B KM418C256BL KM418C256BLL	I_{CC5}	-	1 200 150	mA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC}=min.)	KM418C256B/BL/BLL-6 KM418C256B/BL/BLL-7 KM418C256B/BL/BLL-8	I_{CC6}	-	95 85 80	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V, xCAS=0.2V D_{IN}=Don't Care, T_{RC}=125μS T_{RAS}=T_{RAS} min.~300ns	KM418C256BL	I_{CC7}	-	300	μA
Self Refresh Current $\overline{RAS}$=x$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_8=V_{CC}-0.2V or 0.2V DQ_1-DQ_{16}=V_{CC}-0.2V, 0.2V or Open	KM418C256BLL	I_{CC5}	-	200	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_8)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_{18})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command set-up time	t_{WCS}	0		0		0		ns	8
Write command hold time	t_{WCH}	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		50		55		ns	6
Write command pulse width	t_{WP}	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		ns	

AC CHARACTERISTICS (Continued)

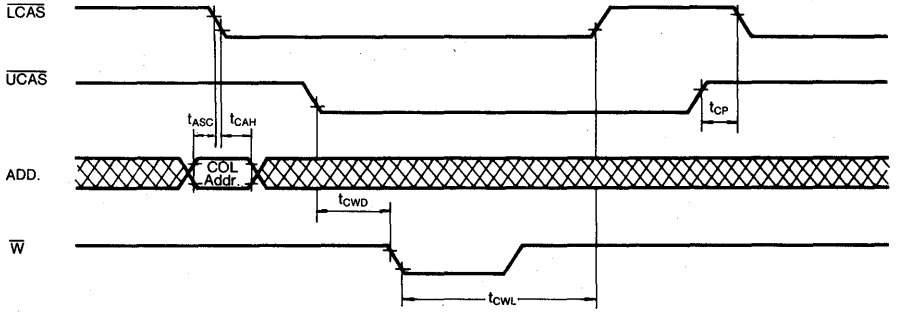
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal)	t_{REF}		8		8		8	ms	
Refresh period (L-version)	t_{REF}		64		64		64	ms	
Refresh period (LL-version)	t_{REF}		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		95		105		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	85		95		100		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		ns	
Access time from $\overline{OE}$	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data-in delay time	t_{OED}	15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ commend hold time	t_{OEH}	15		20		20		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		100		100		μs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	-50		-50		-50		ns	12

KM418C256B Truth Table

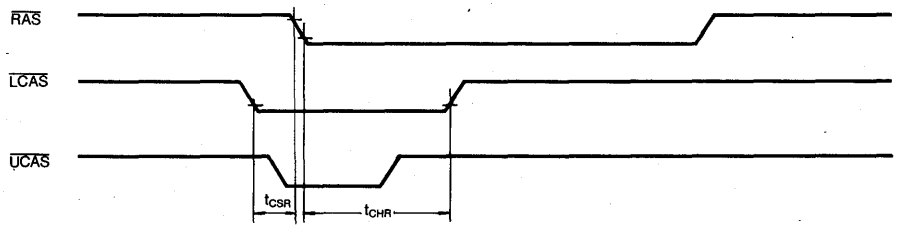
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	$DQ_{1\sim9}$	$DQ_{10\sim18}$	State
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Lower Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-In	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	—

NOTES

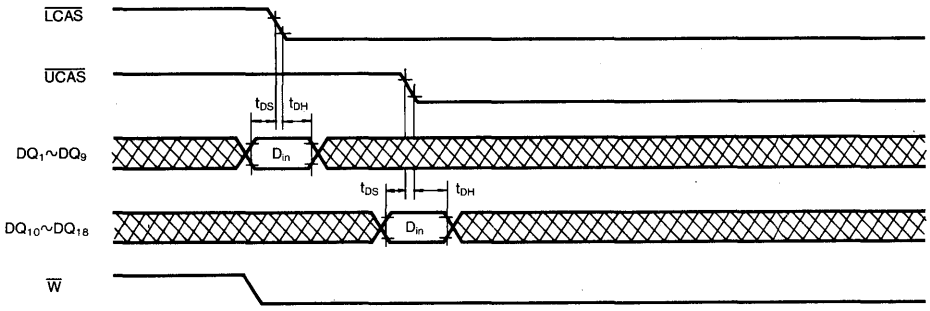
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating aprameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. 512 cycles of burst refresh must be executed within 8ms before and after self refresh, In order to meet refresh specification.
13. t_{ASC}, t_{CAH} are referenced to the earler $\overline{CAS}$ falling edge.
14. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
15. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



17. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
18. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

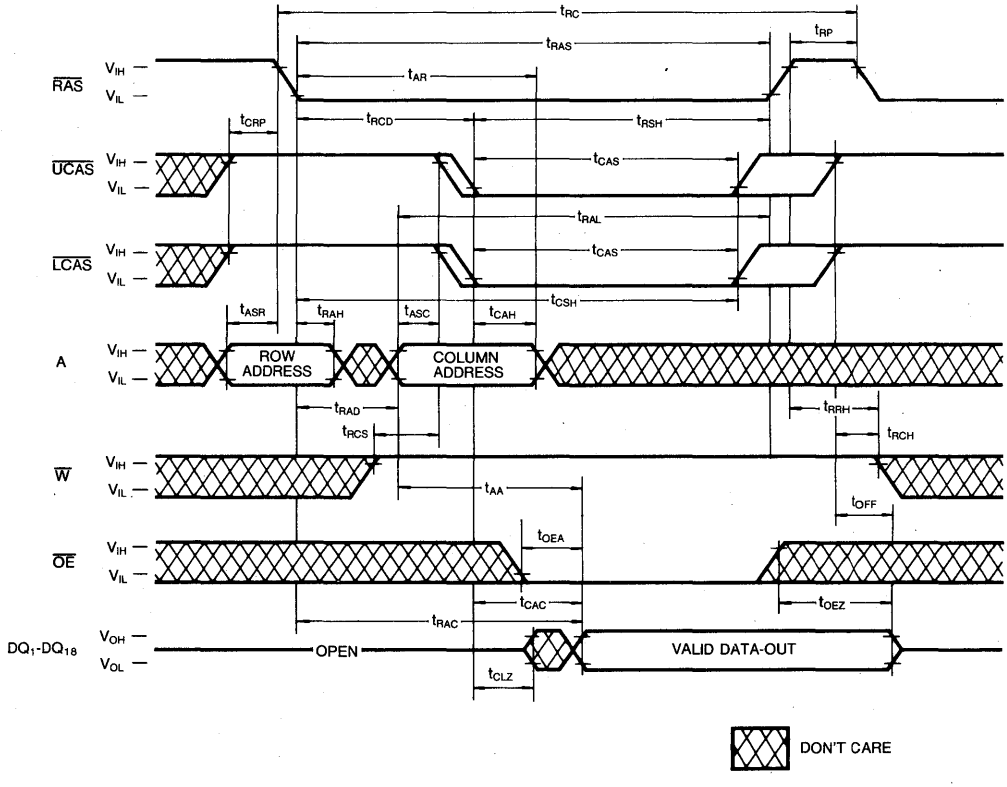


19. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim9)}$, upper byte $D_{in(10\sim18)}$.



TIMING DIAGRAMS

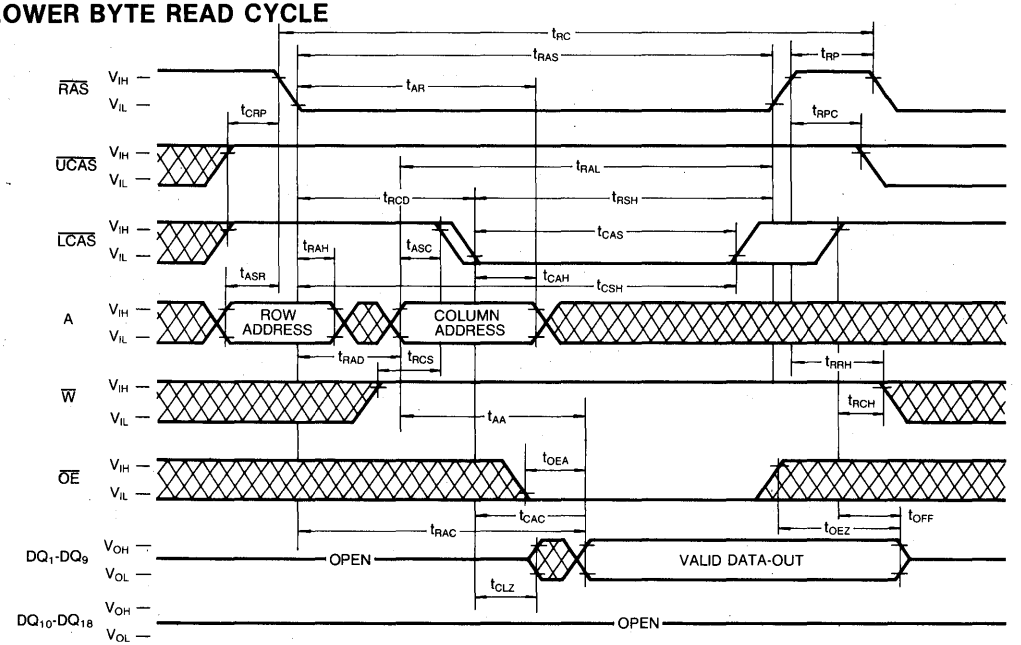
WORD READ CYCLE



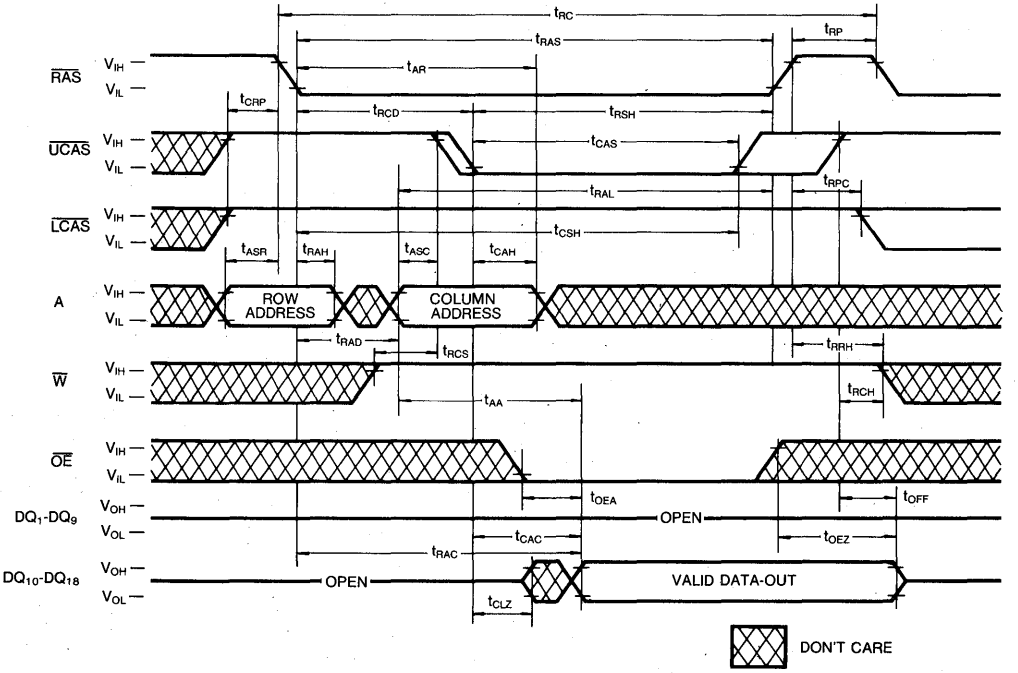
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

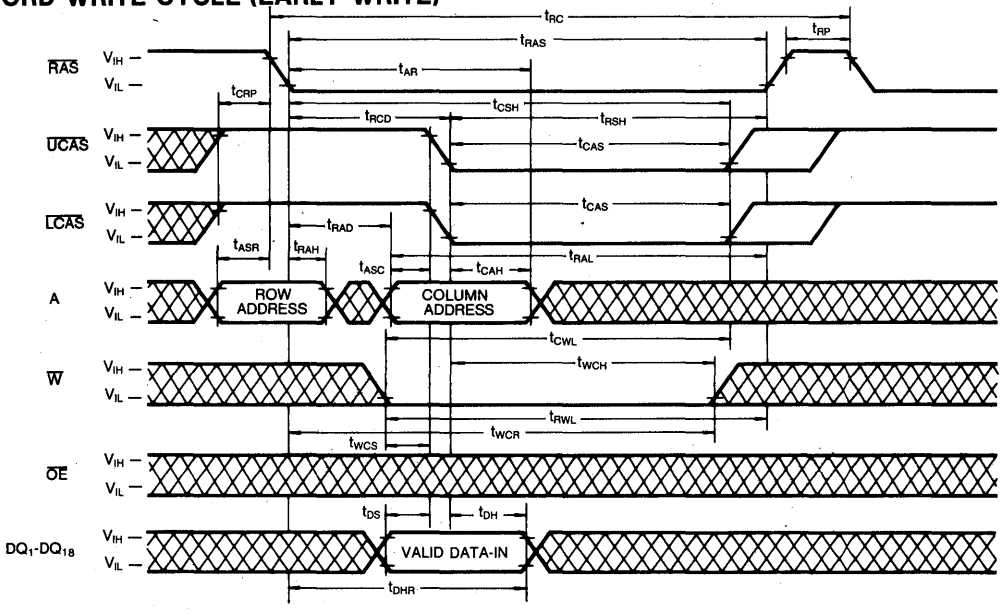


UPPER BYTE READ CYCLE

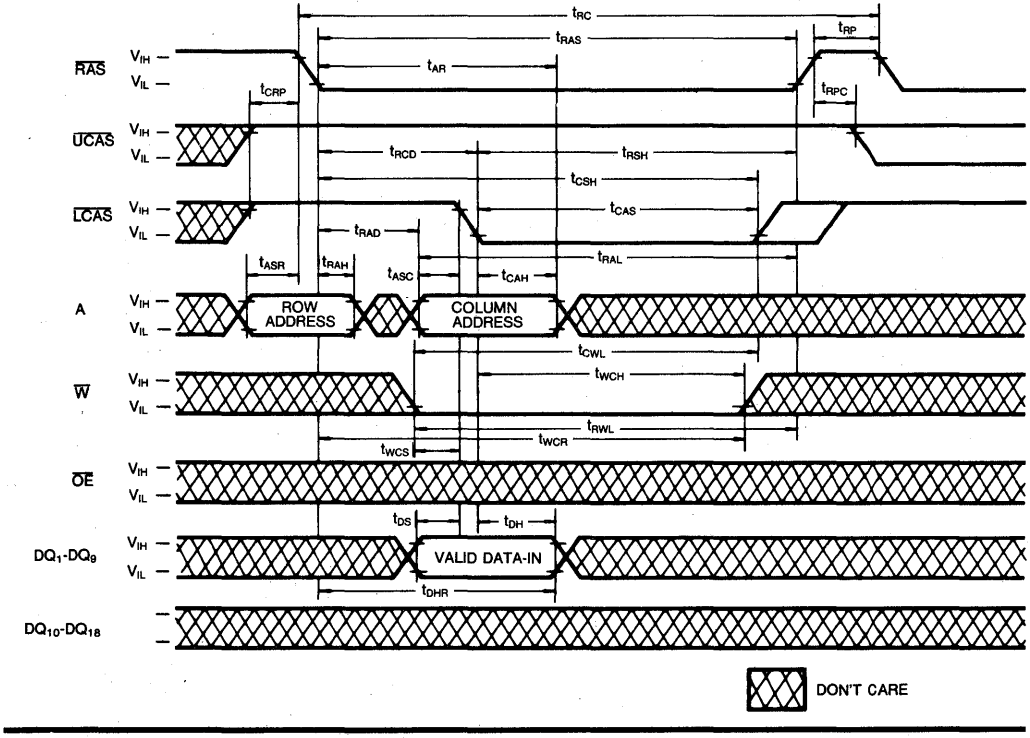


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)

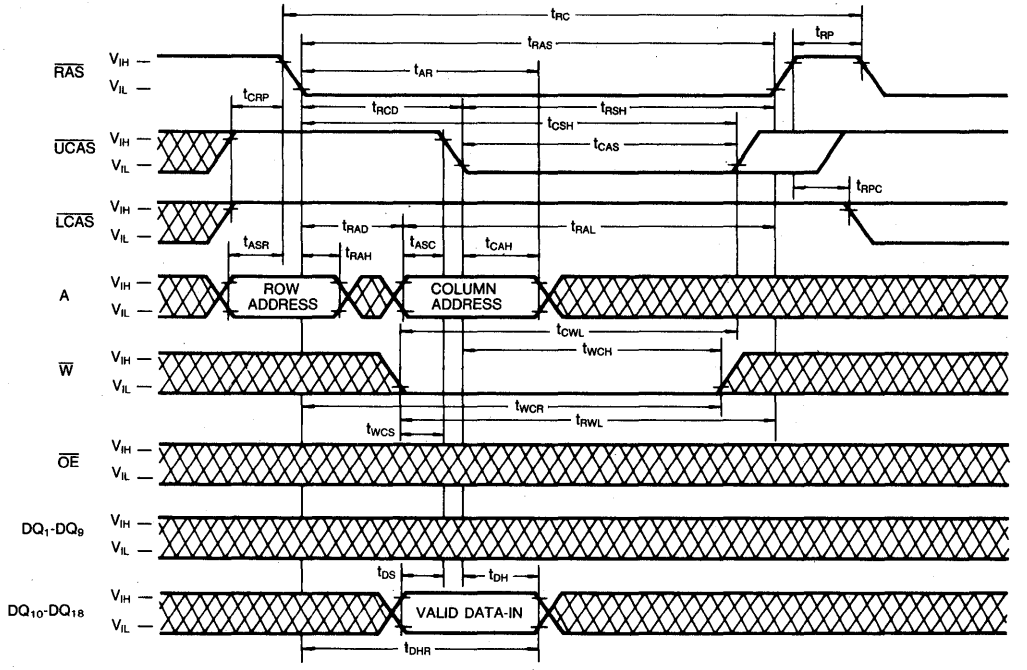


LOWER BYTE WRITE CYCLE (EARLY WRITE)

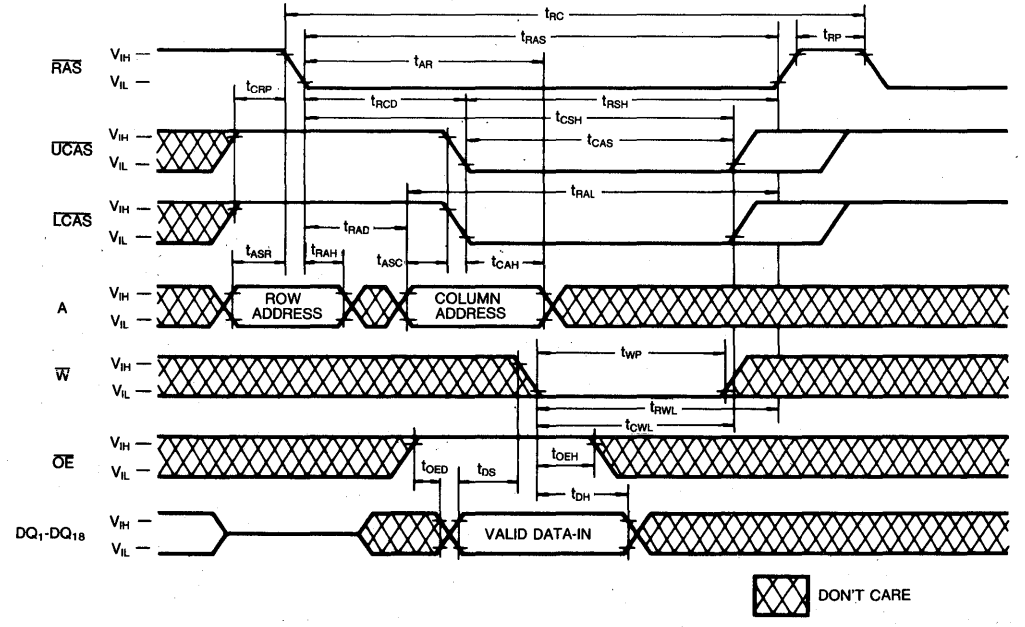


TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

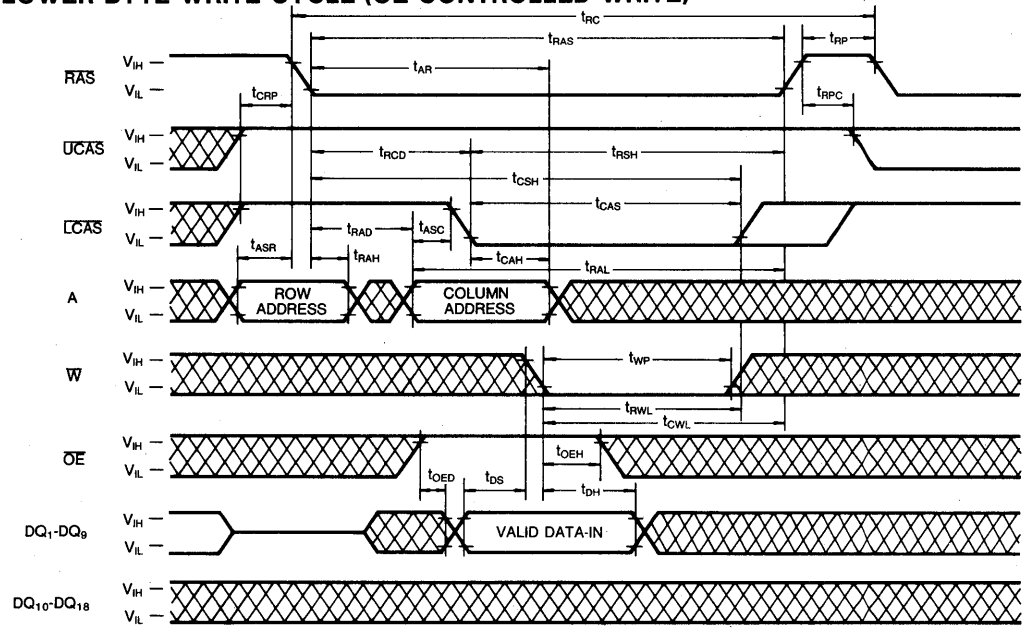


WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

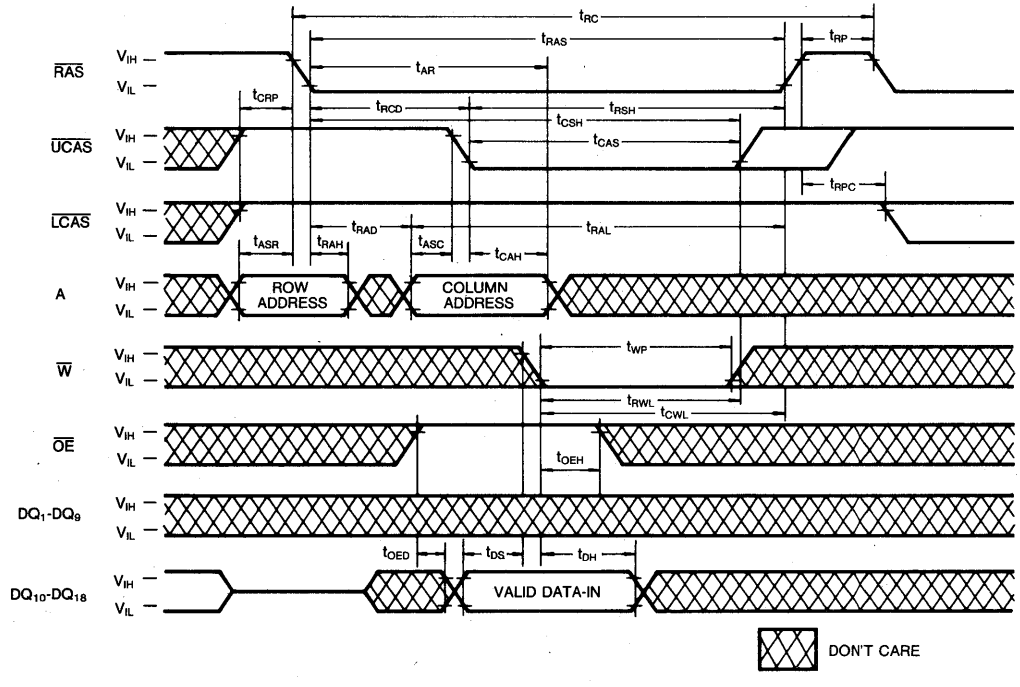


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

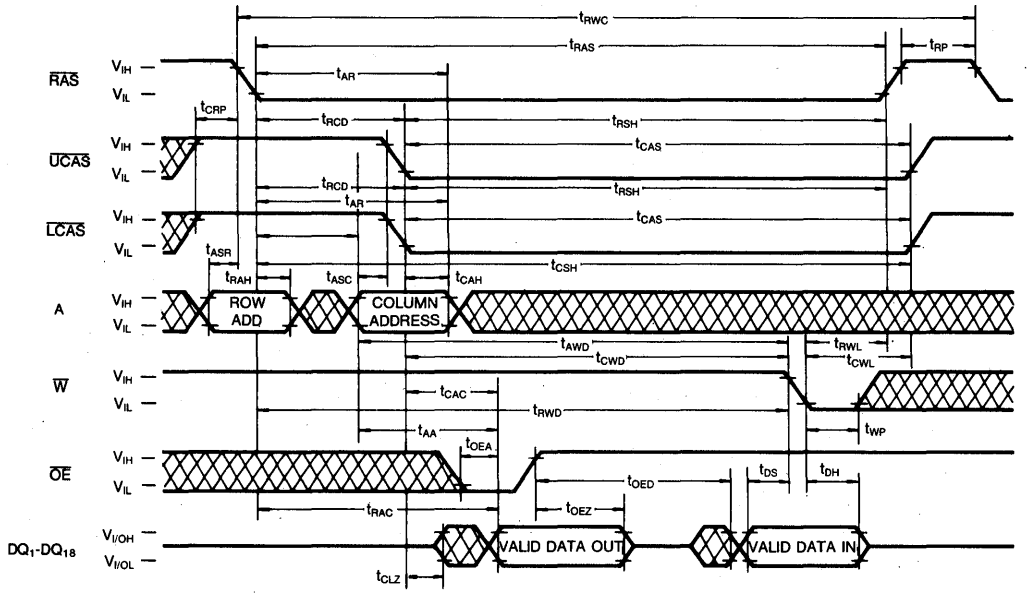


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

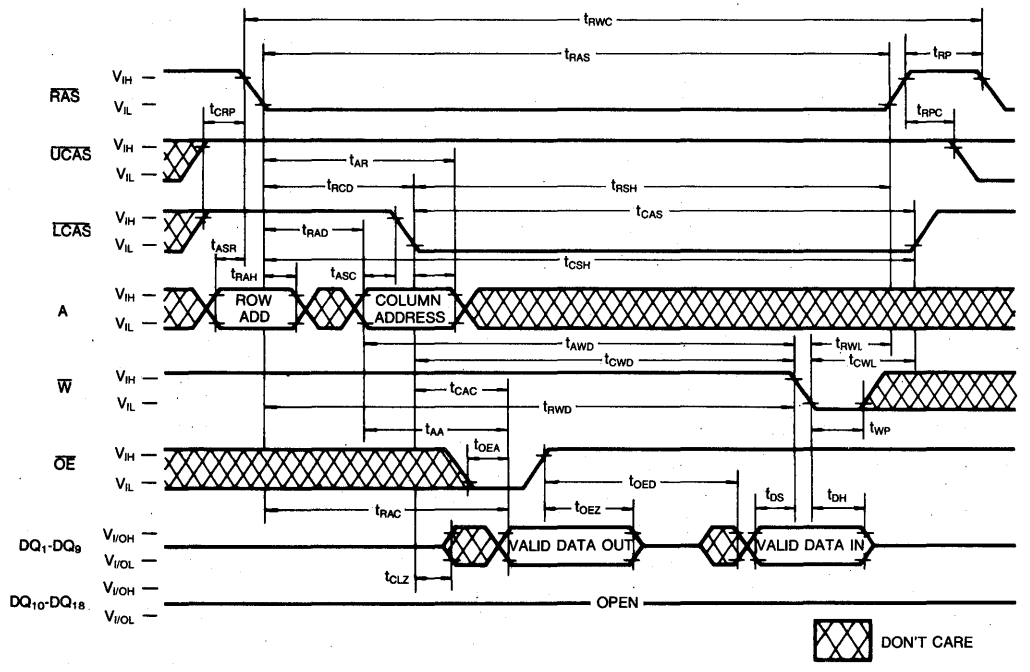


TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

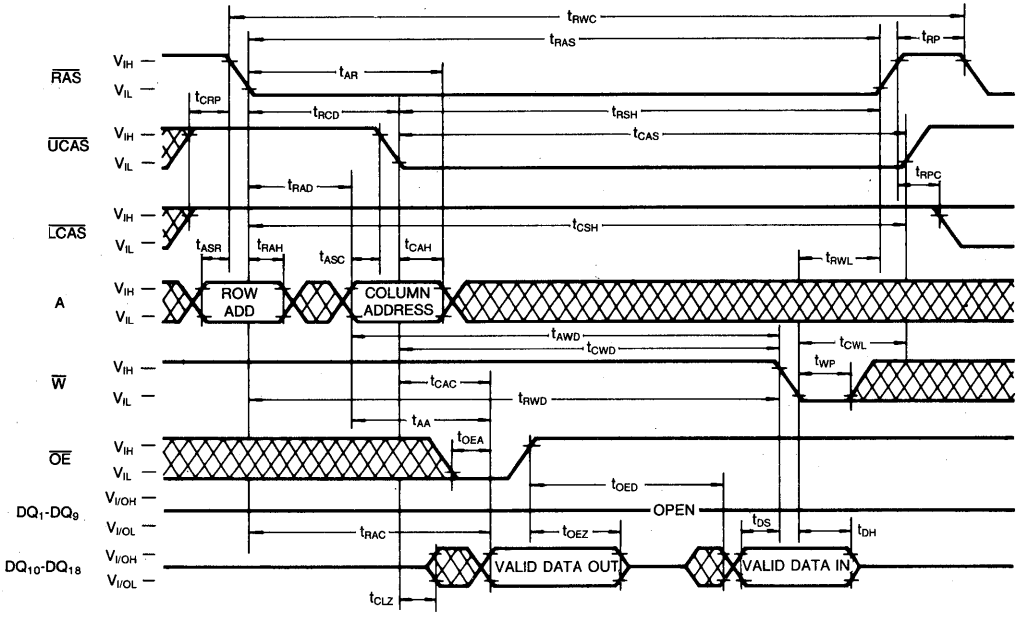


LOWER-BYTE READ-MODIFY-WRITE CYCLE

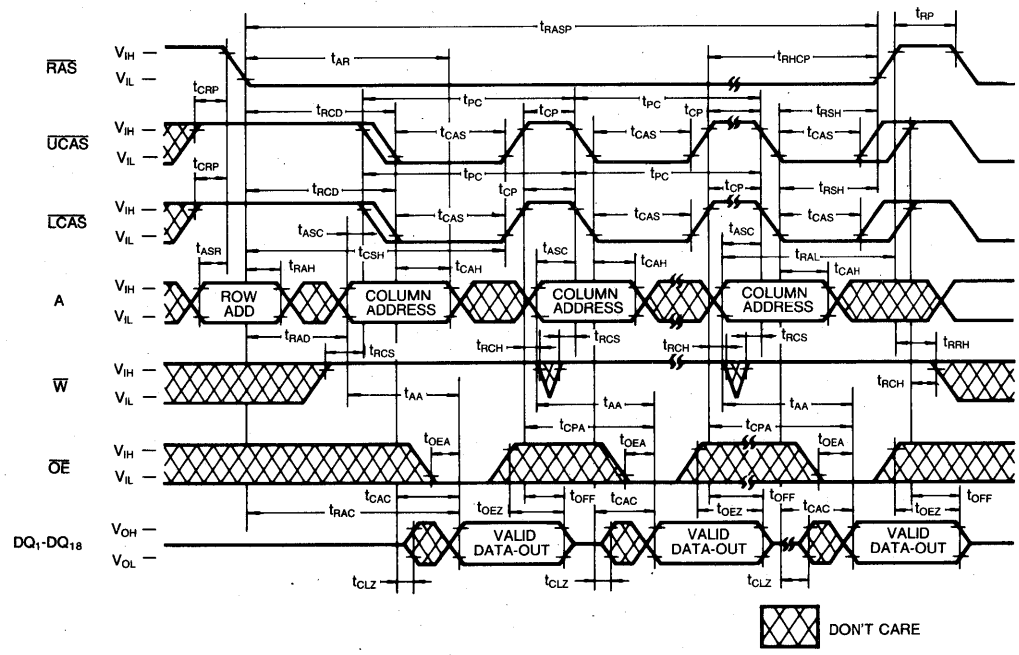


TIMING DIAGRAMS (Continued)

UPPER-BYTE READ-MODIFY-WRITE CYCLE

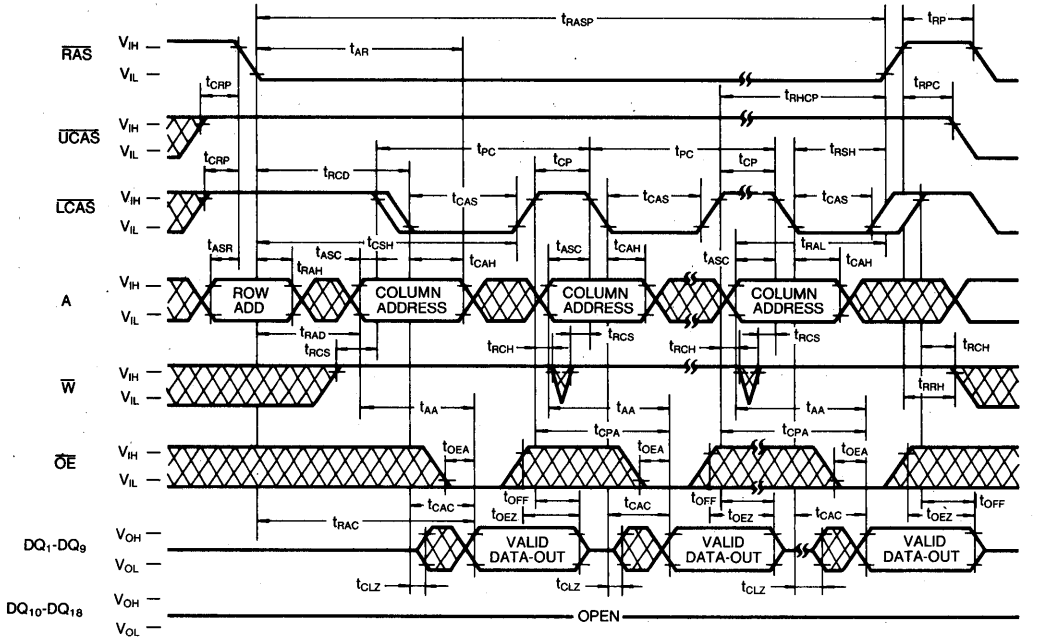


FAST PAGE MODE WORD READ CYCLE

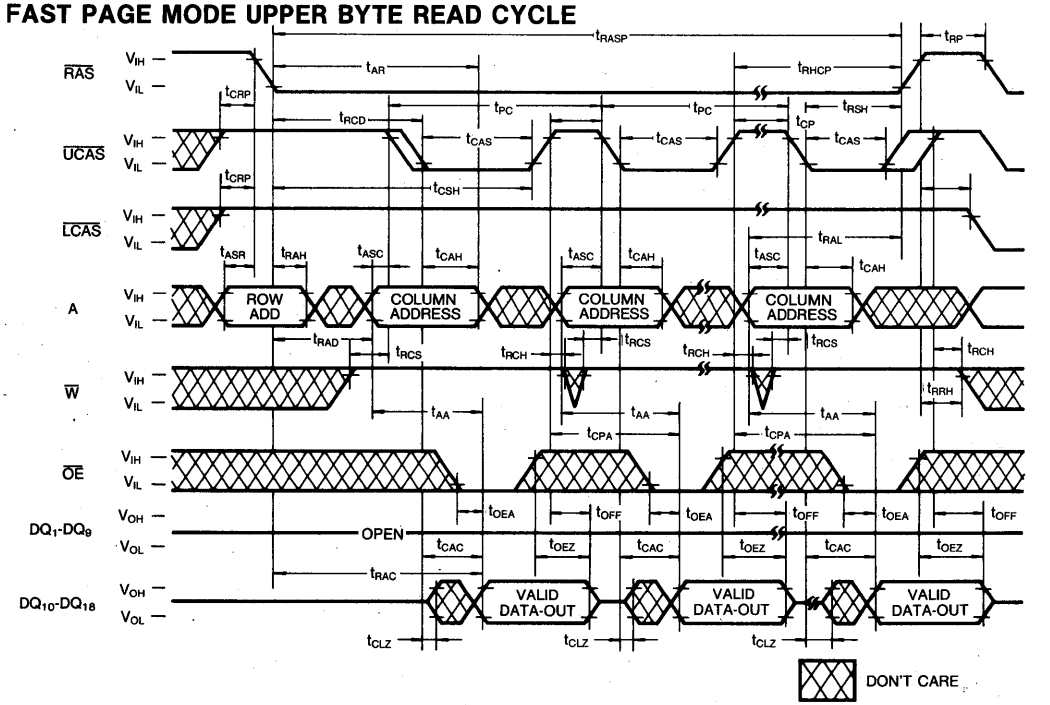


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE

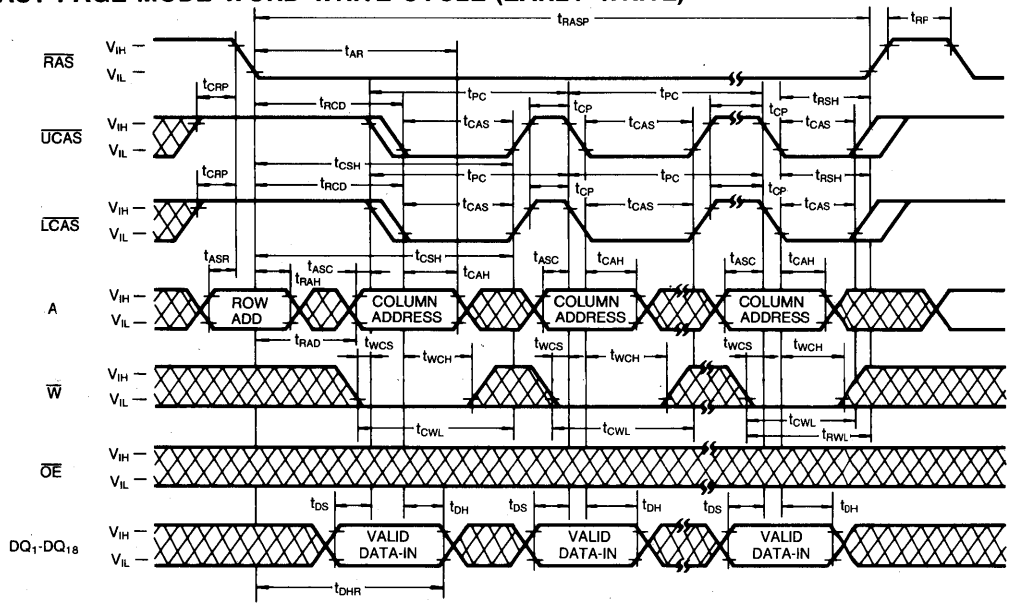


FAST PAGE MODE UPPER BYTE READ CYCLE

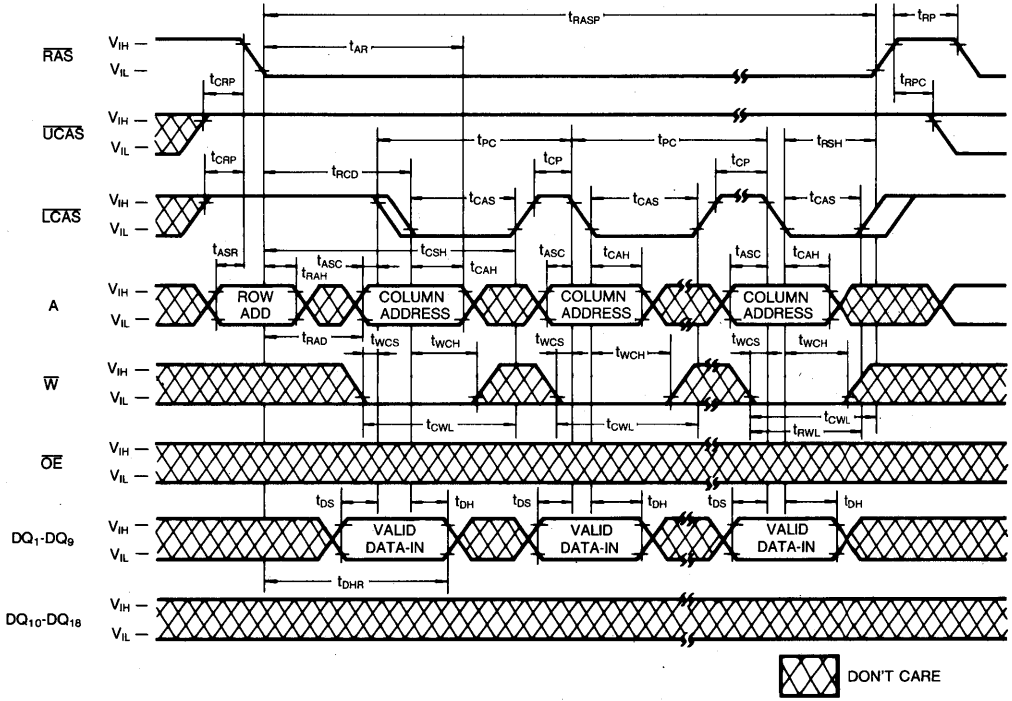


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

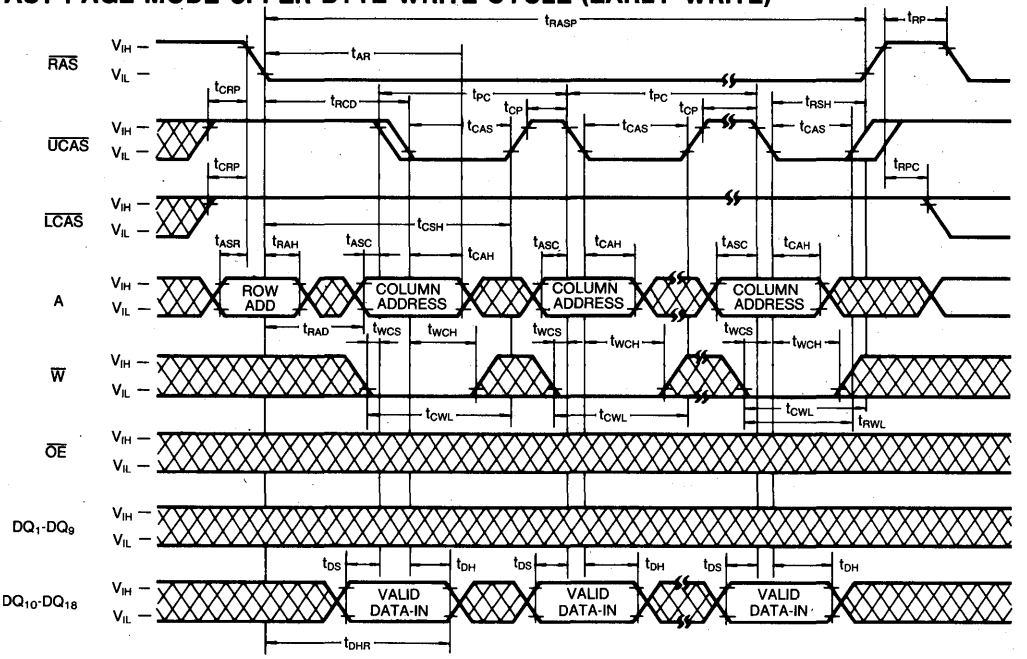


FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)

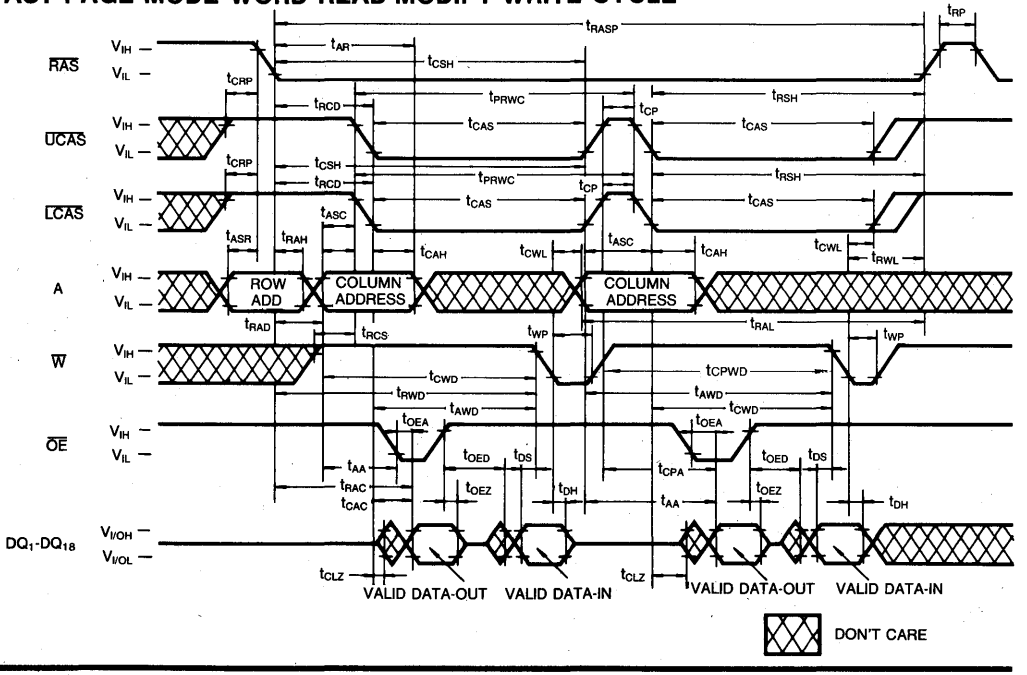


TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

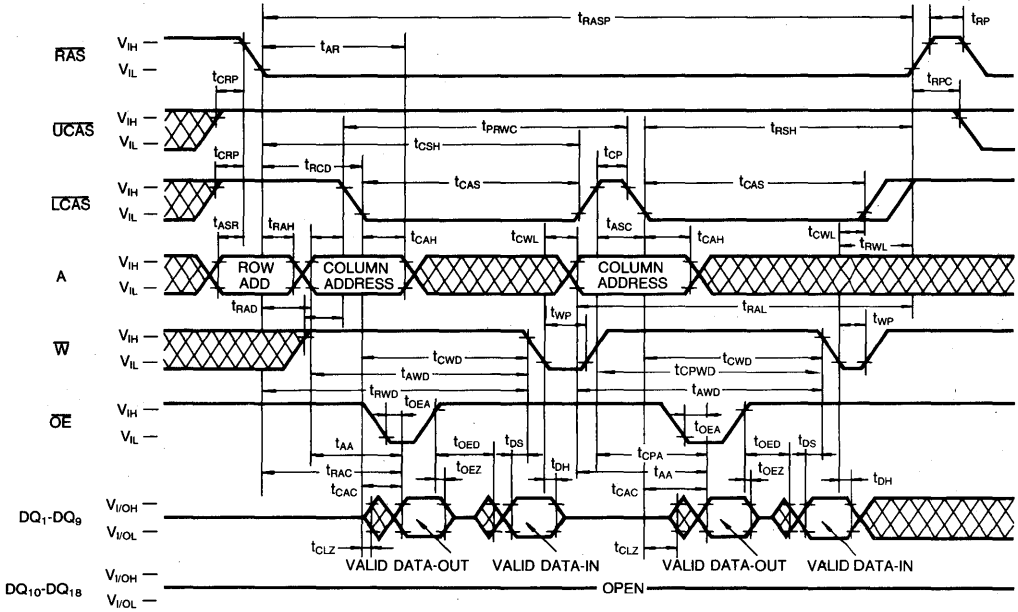


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

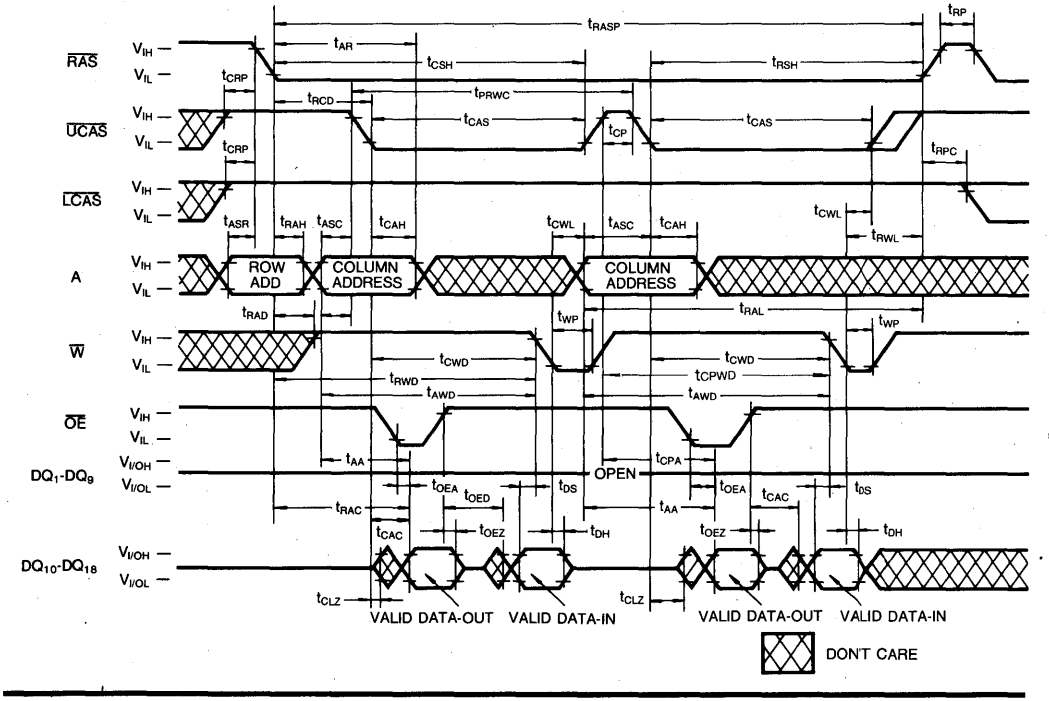


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ-MODIFY-WRITE CYCLE

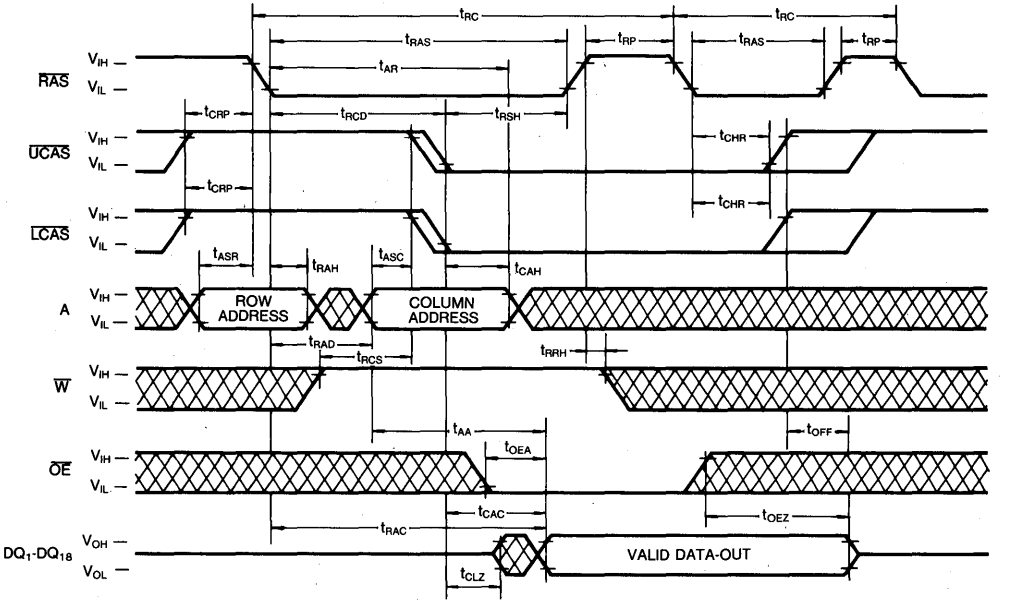


FAST PAGE MODE UPPER BYTE READ-MODIFY-WRITE CYCLE

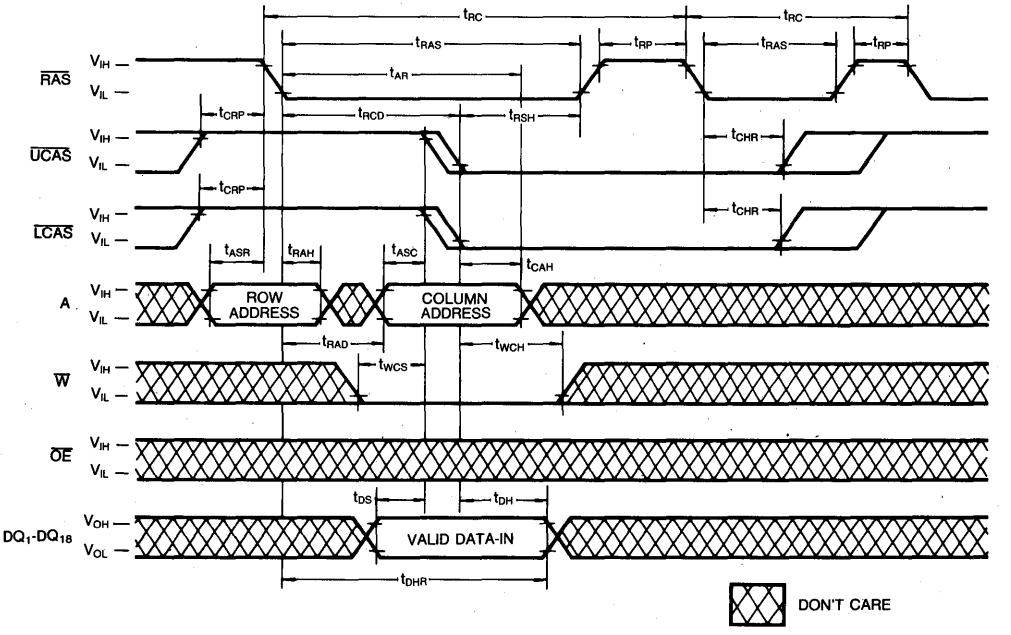


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

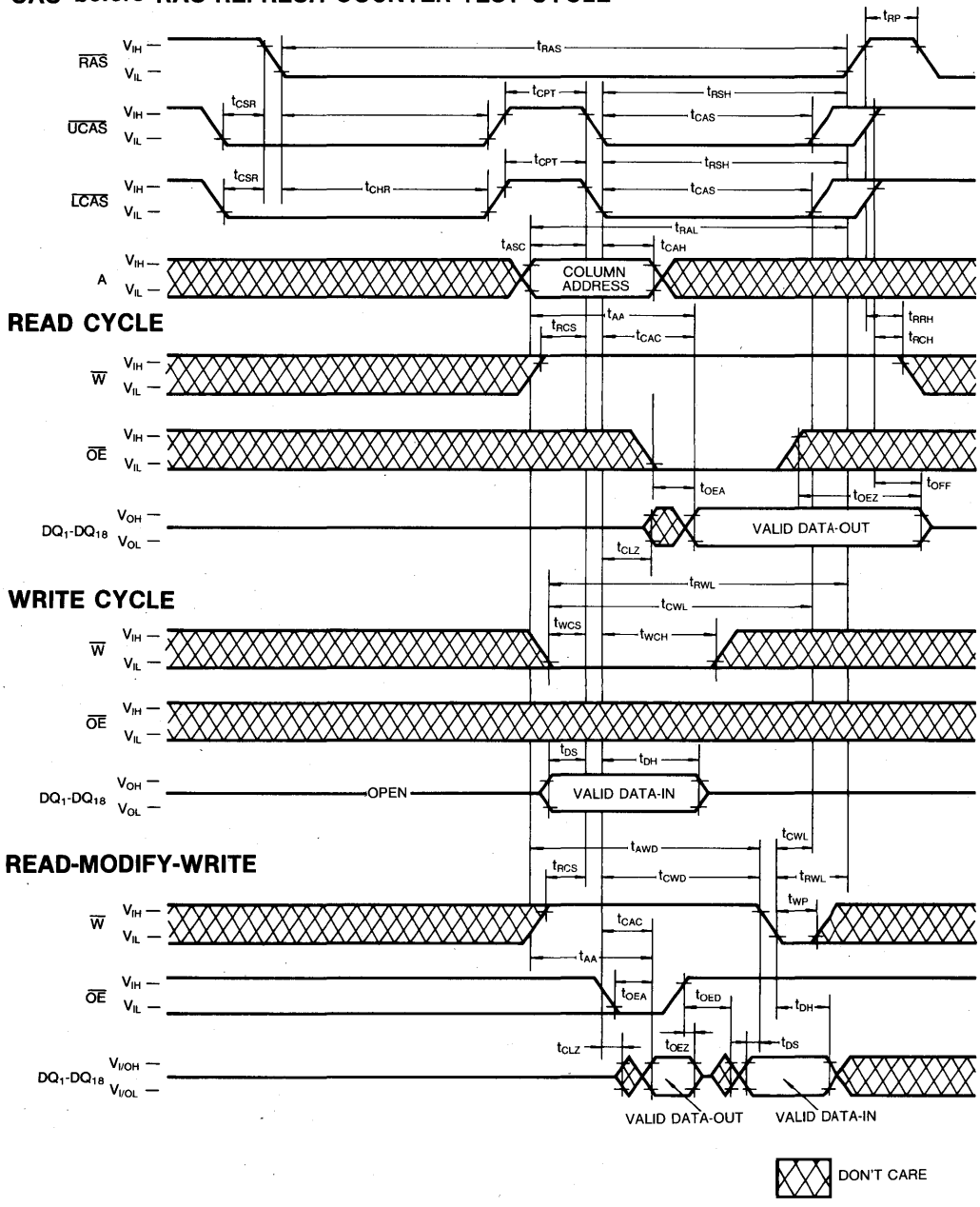


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

$\overline{CAS}$- before-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

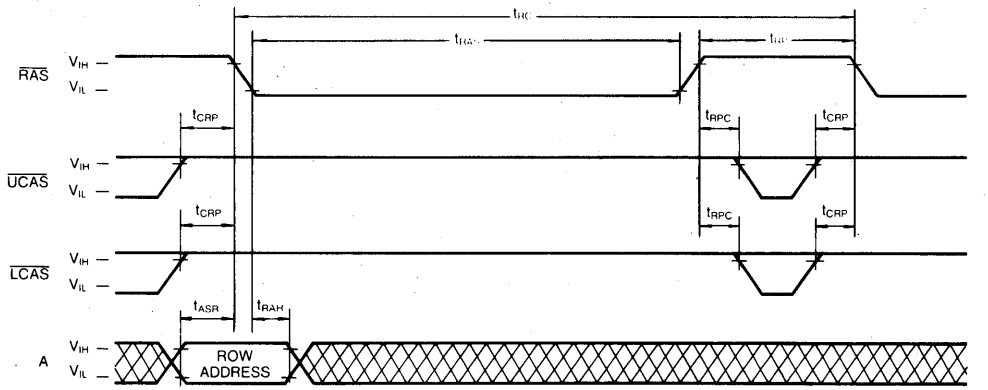


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

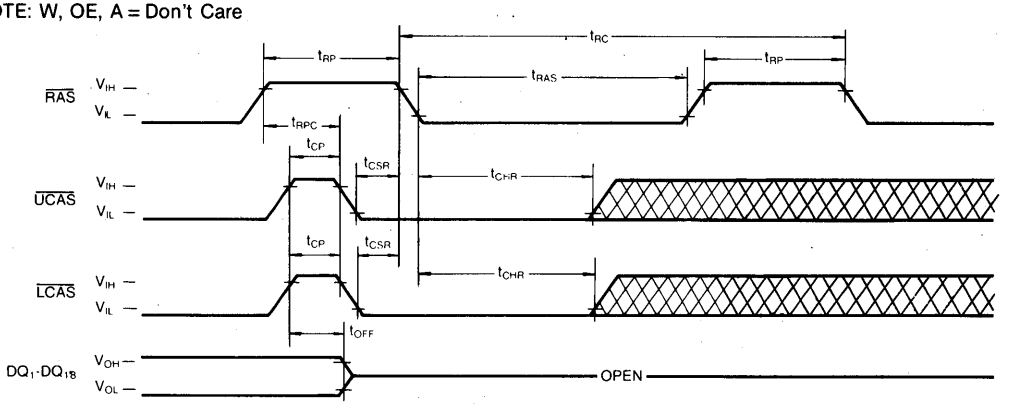
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



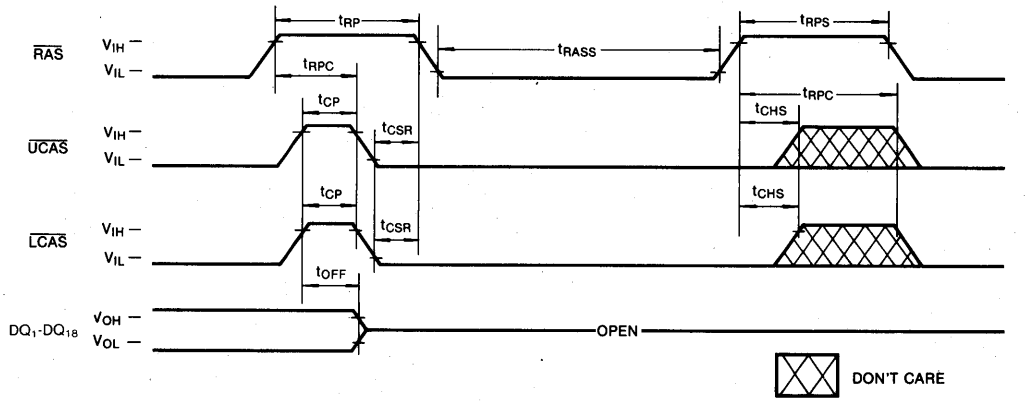
$\overline{CAS}$-before-$\overline{RAS}$ REFRESH CYCLE

NOTE: W, OE, A = Don't Care



$\overline{CAS}$-before-$\overline{RAS}$ SELF REFRESH CYCLE (Self refresh only)

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care

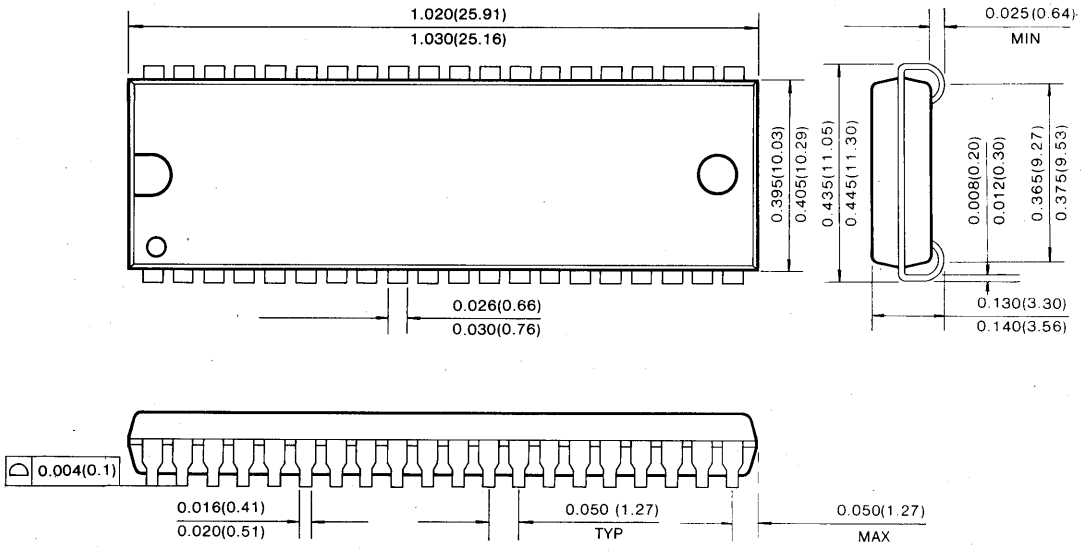


SAMSUNG ELECTRONICS

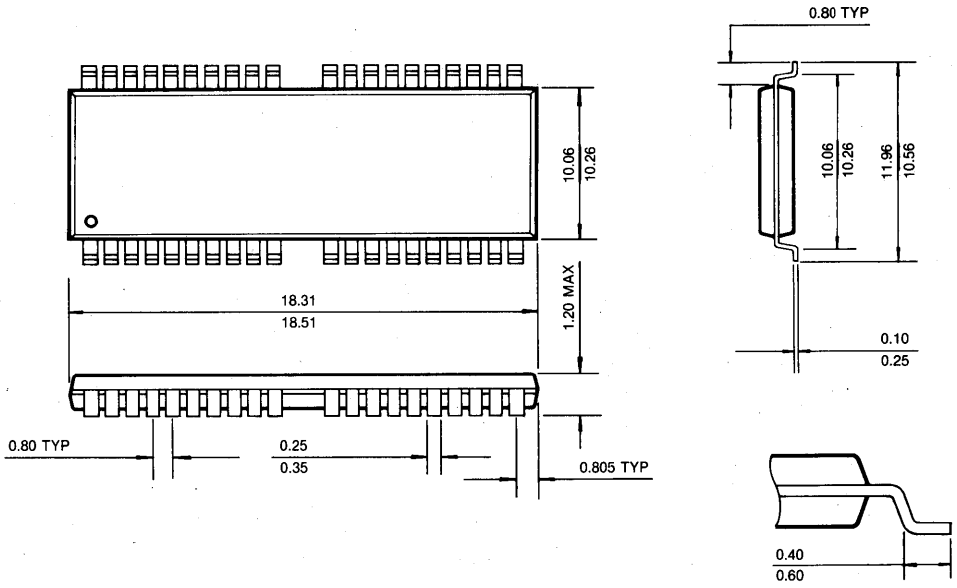
PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)



SAMSUNG ELECTRONICS

512K ×8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM48V512B/BL/BLL-6	60ns	15ns	110ns
KM48V512B/BL/BLL-7	70ns	20ns	130ns
KM48V512B/BL/BLL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Self Refresh operation (LL-version)**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Dual +3.3V±0.3V power supply**
- **Refresh Cycle**
  - **-1024 cycle/16ms (Normal)**
  - **-1024 cycle/128ms (L-version)**
  - **-1024 cycle/128ms (LL-version)**
- **Power Dissipation**
  - **-Standby: 1.8mW (Normal)**
  - **0.36mW (L-version)**
  - **0.36mW (LL-version)**
  - **-Active (60/70/80): 255/235/220mW**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP II**

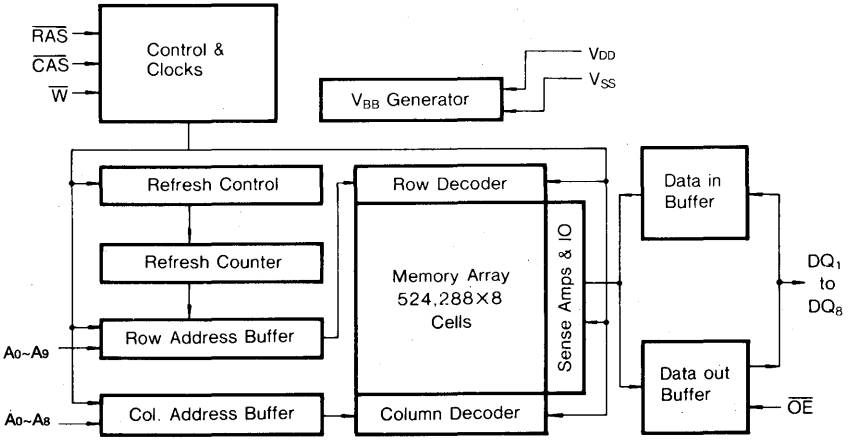
GENERAL DESCRIPTION

The Samsung KM48V512B/BL/BLL is a CMOS high speed 524,288 bit×8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM48V512B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

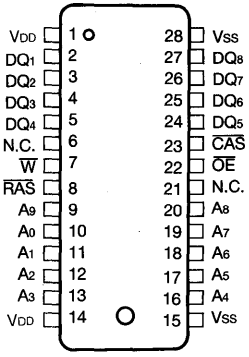
The KM48V512B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



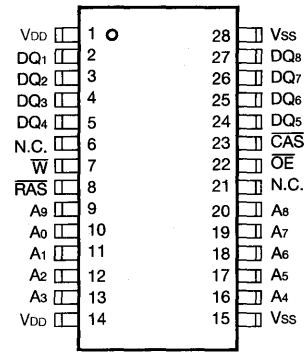
PIN CONFIGURATION (Top Views)

• KM48V512BJ/BLJ/BLLJ



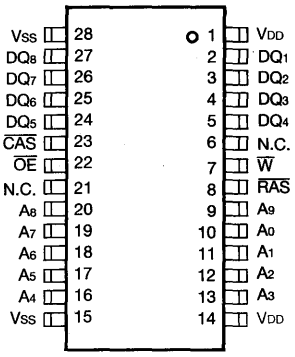
(SOJ)

• KM48V512BT/BLT/BLLT



(TSOP(II)-Forward Type)

• KM48V512BTR/BLTR/BLLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A0-A9	Address Inputs
DQ1~8	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VDD	Power(+3.3V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5 to 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.1	—	V_{DD} +0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	KM48V512B/BL/BLL-6 KM48V512B/BL/BLL-7 KM48V512B/BL/BLL-8	I_{CC1}	-	70 65 60	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM48V512B/BL/BLL-6 KM48V512B/BL/BLL-7 KM48V512B/BL/BLL-8	I_{CC3}	-	70 65 60	mA mA mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM48V512B/BL/BLL-6 KM48V512B/BL/BLL-7 KM48V512B/BL/BLL-8	I_{CC4}	-	55 50 45	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM48V512B KM48V512BL KM48V512BLL	I_{CC5}	-	500 100 100	μA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48V512B/BL/BLL-6 KM48V512B/BL/BLL-7 KM48V512B/BL/BLL-8	I_{CC6}	-	70 65 60	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{DD}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=0.2V D_{IN}=Don't Care, T_{RC}=125μS T_{RAS}=T_{RAS} min.~300ns	KM48V512BL	I_{CC7}	-	200	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_9=V_{DD}-0.2V or 0.2V DQ_1-DQ_8=V_{DD}-0.2V, 0.2V or Open	KM48V512BLL	I_{CC8}	-	100	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 V)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	

AC CHARACTERISTICS (Continued)

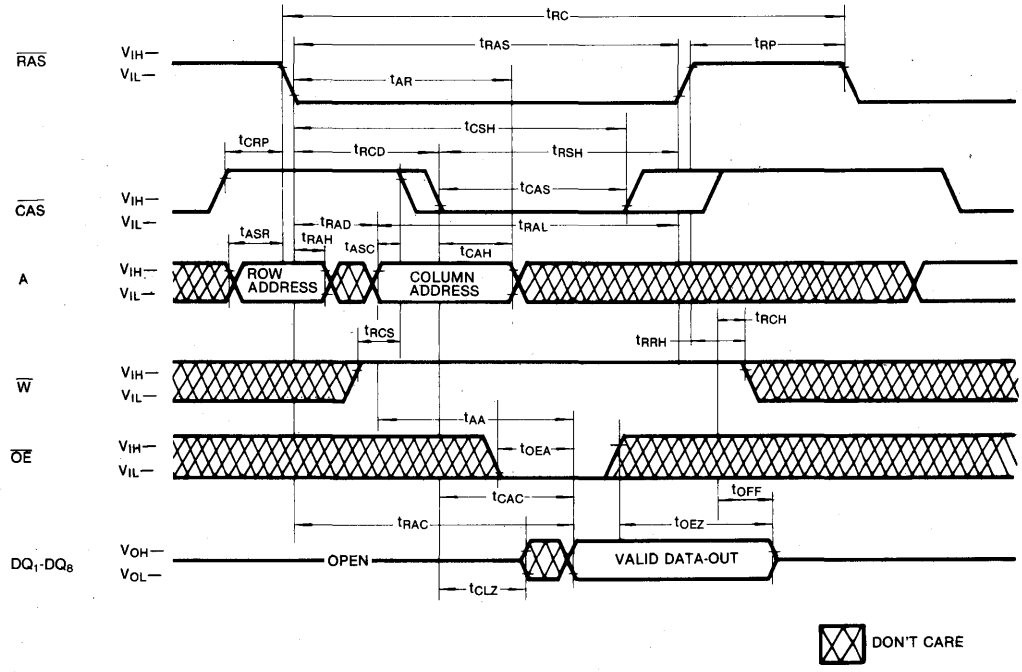
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command set-up time	t_{WCS}	0		0		0		ns	8
Write command hold time	t_{WCH}	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		50		55		ns	6
Write command pulse width	t_{WP}	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	15		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (Normal)	t_{REF}		16		16		16	ms	
Refresh period (L-version)	t_{REF}		128		128		128	ms	
Refresh period (LL-version)	t_{REF}		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		95		105		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	80		95		100		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		ns	
Access time from $\overline{OE}$	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data-in delay time	t_{OED}	15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ commend hold time	t_{OEH}	15		20		20		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		100		100		μs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	-50		-50		-50		ns	12

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF, Voh=2.0V and Vol=0.8V
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} to V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or r_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point ony. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. 1024 cycle of Burst Refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification. (LL-version)

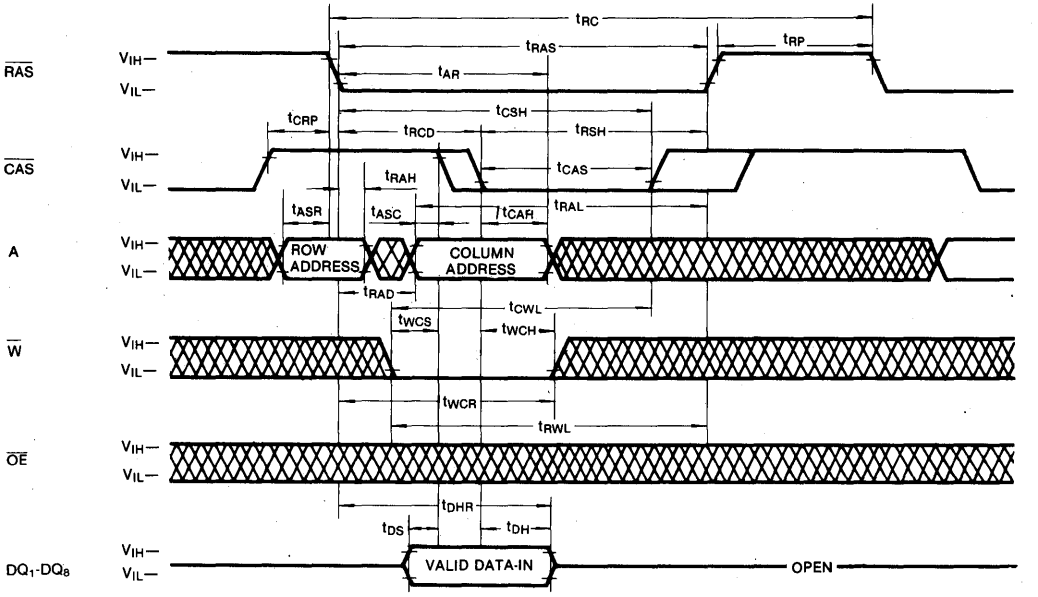
TIMING DIAGRAMS

READ CYCLE

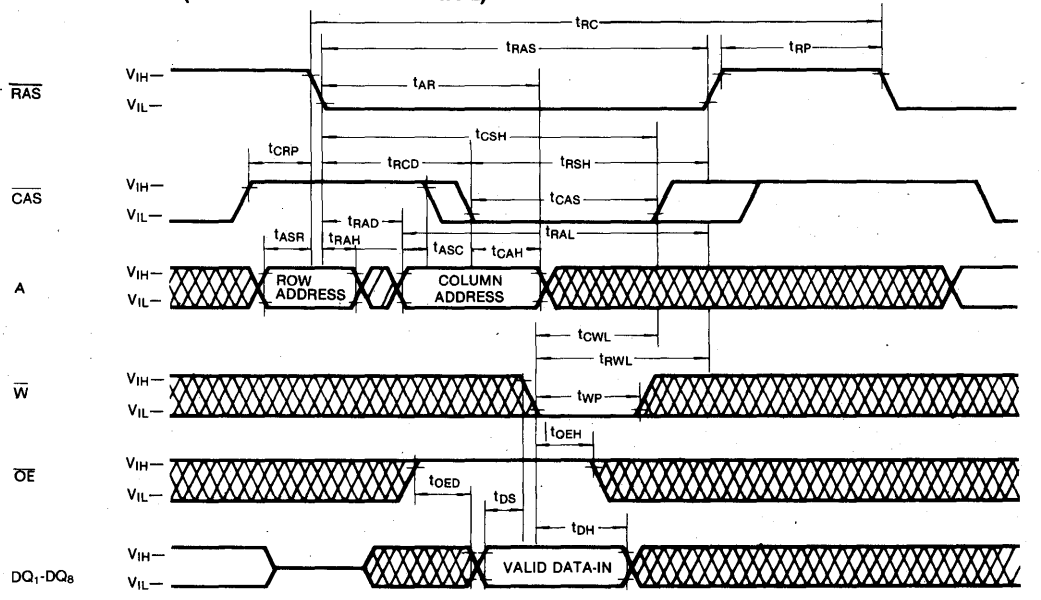


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



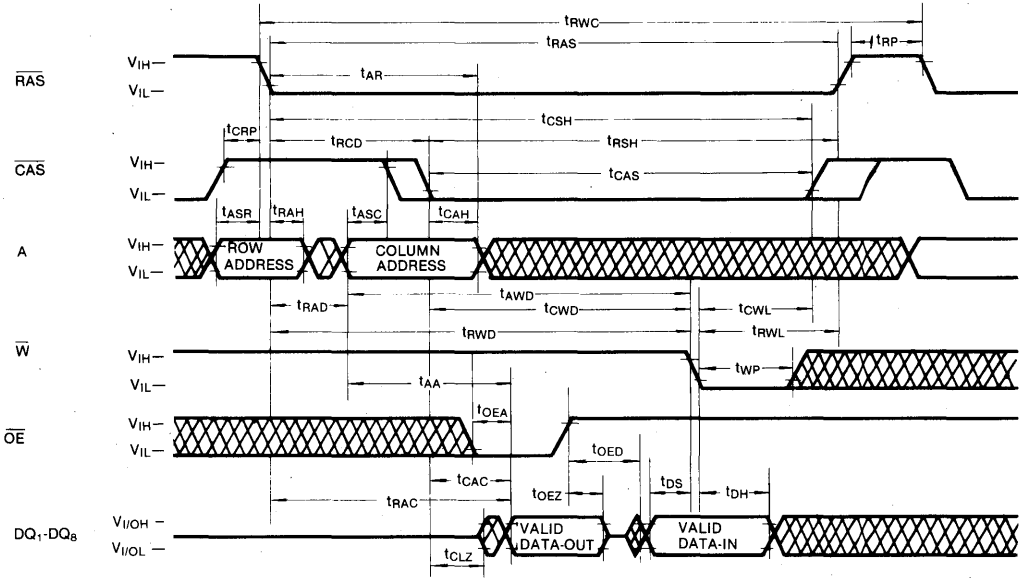
WRITE CYCLE (OE CONTROLLED WRITE)



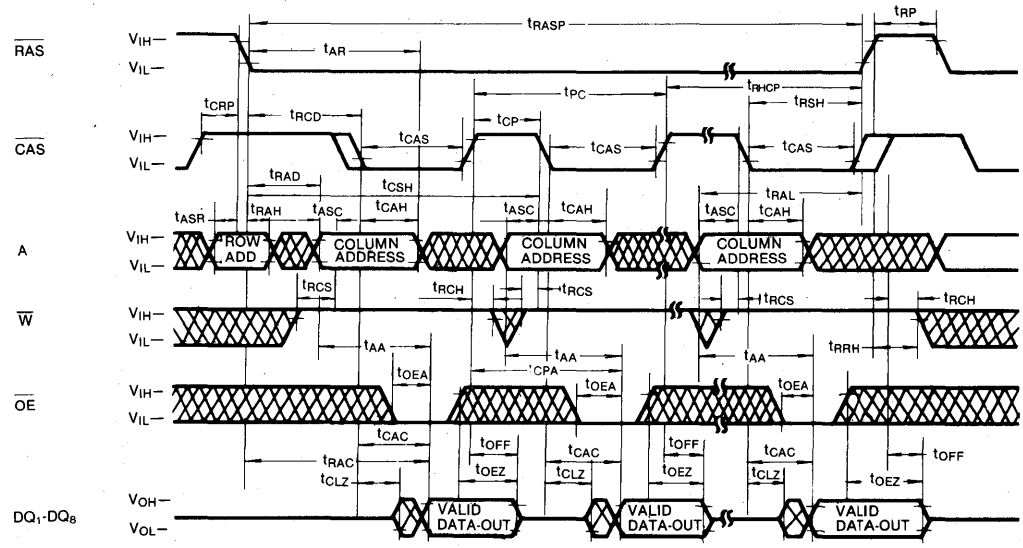
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

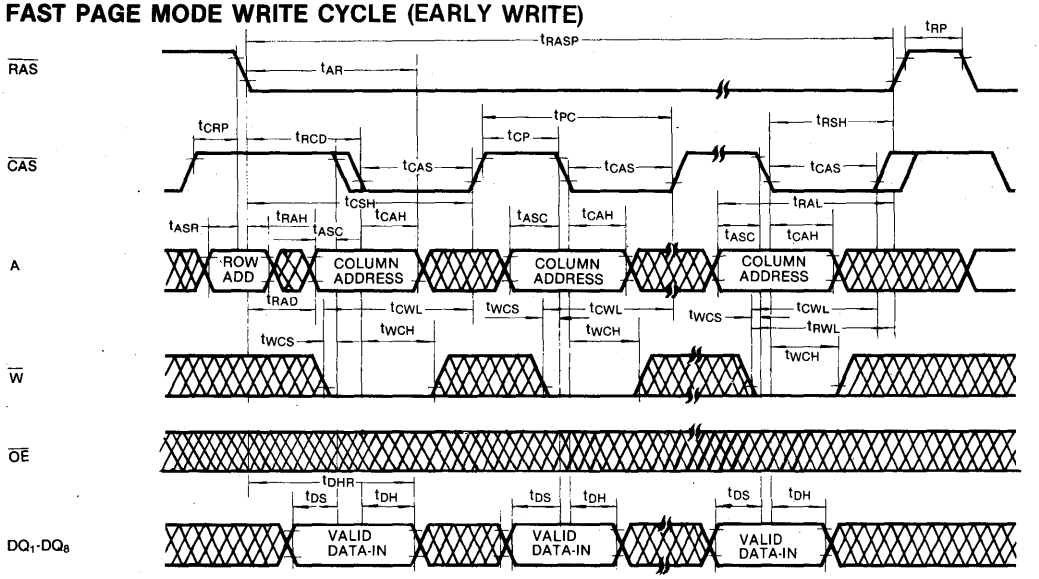


DON'T CARE

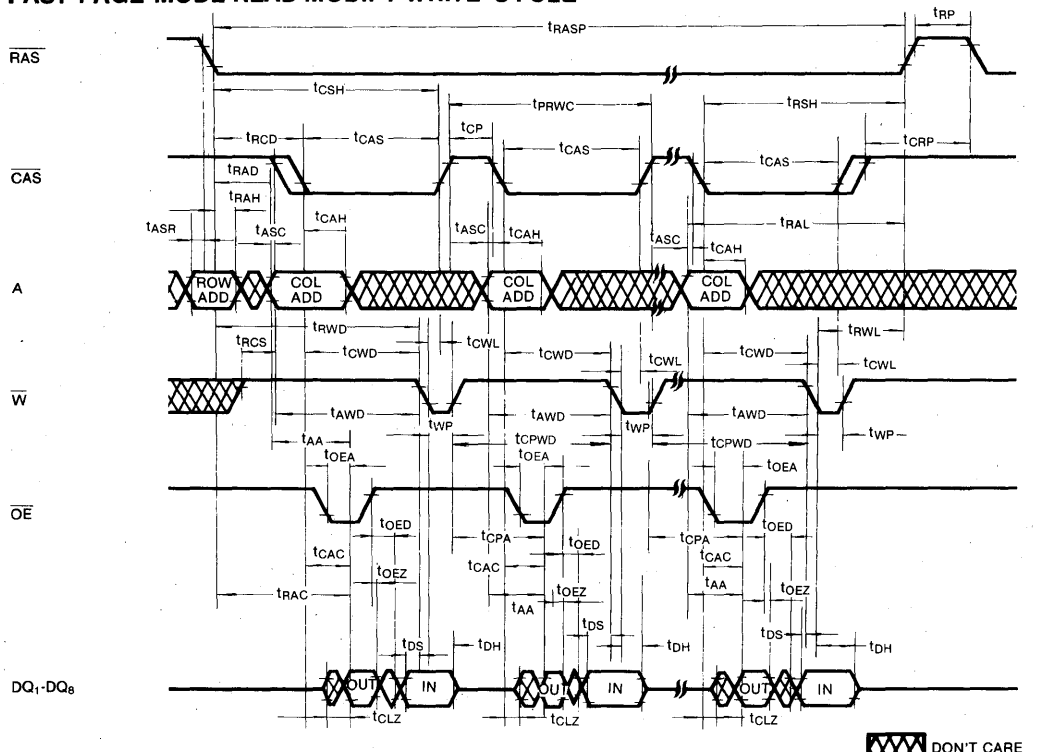
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

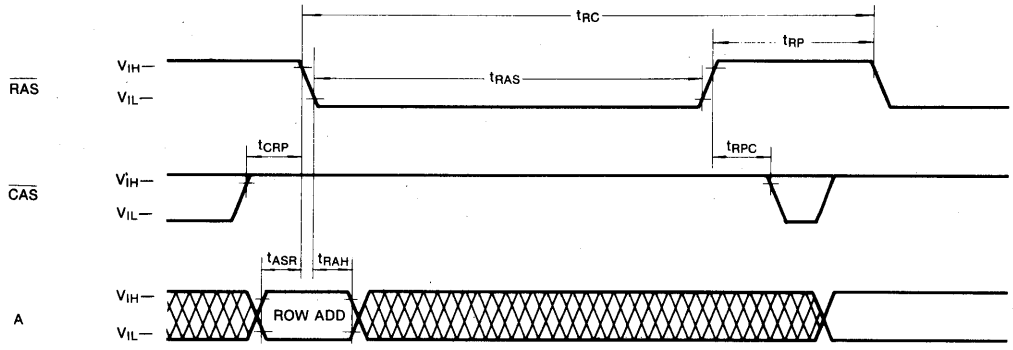


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

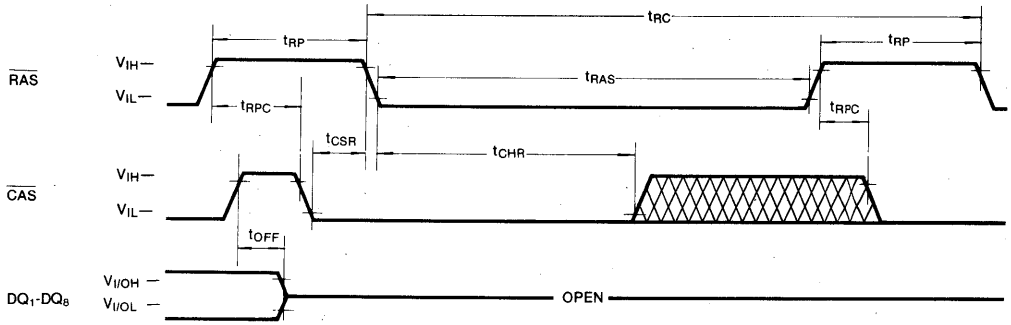
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



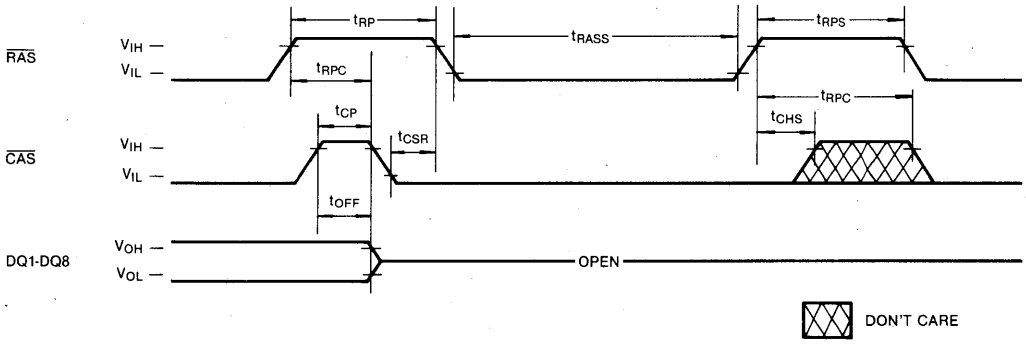
$\overline{CAS}$-before-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care



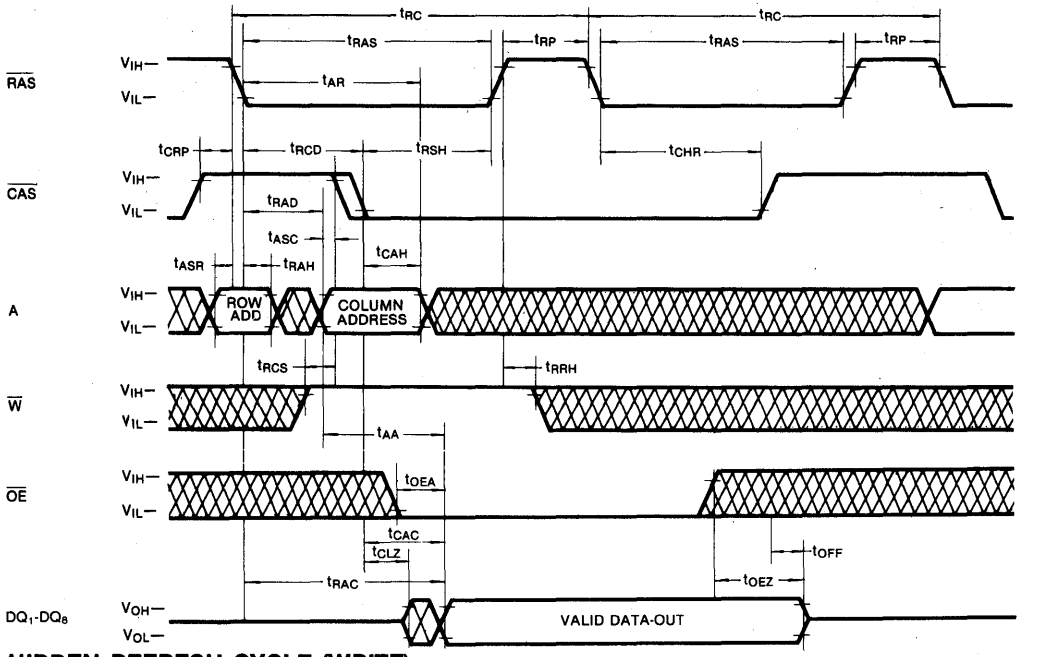
$\overline{CAS}$-before-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care

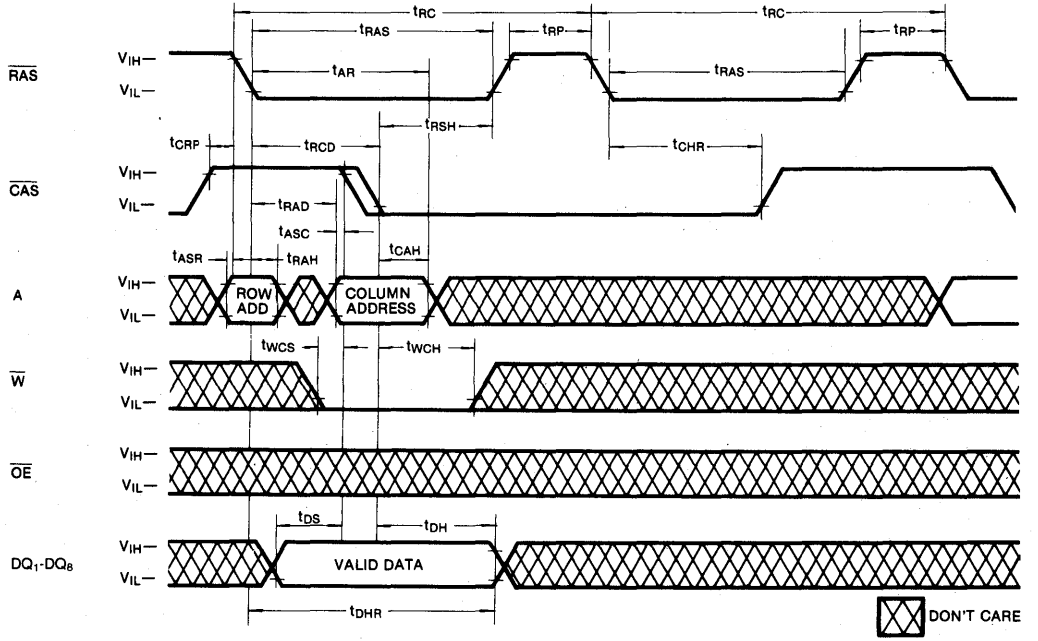


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

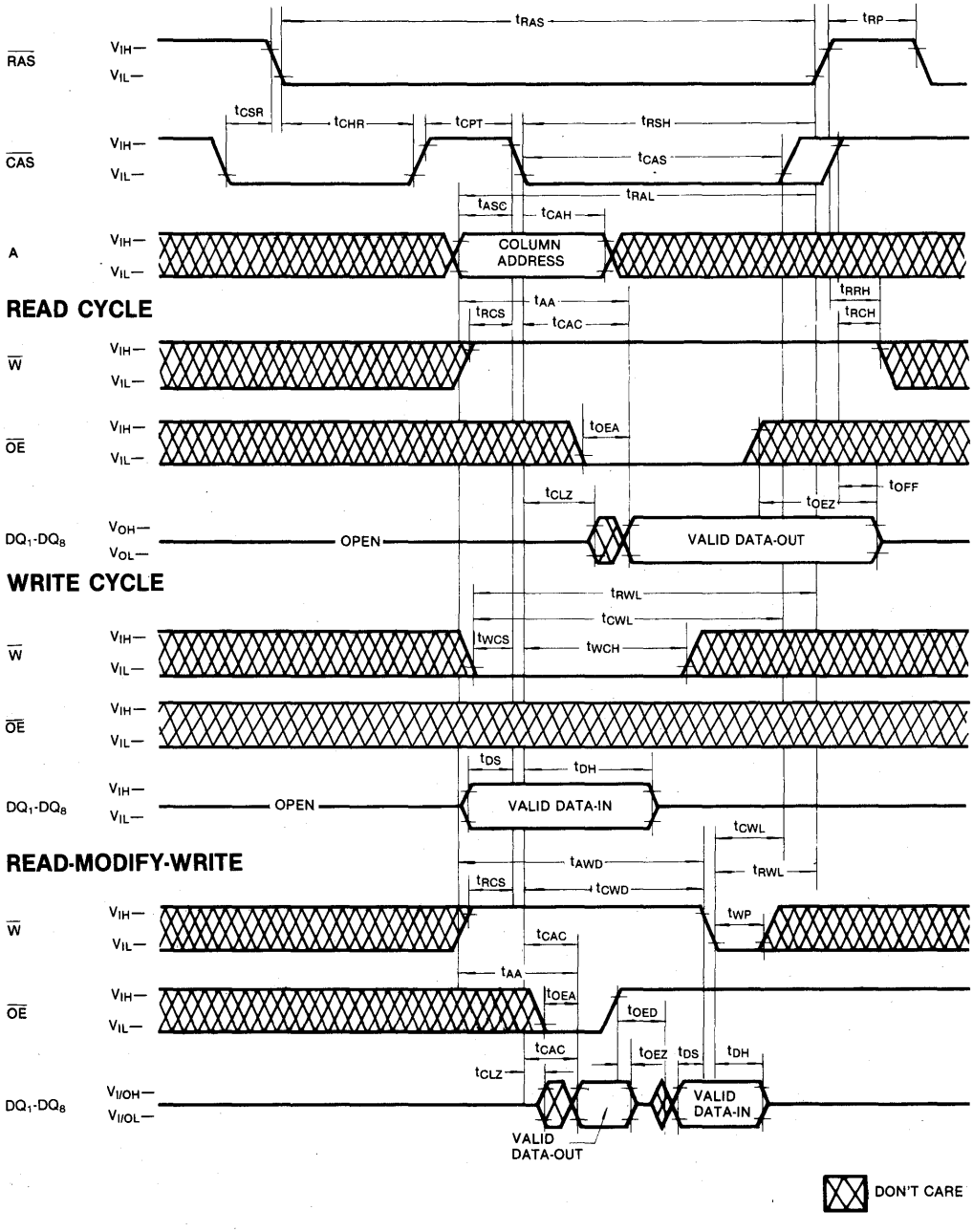


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

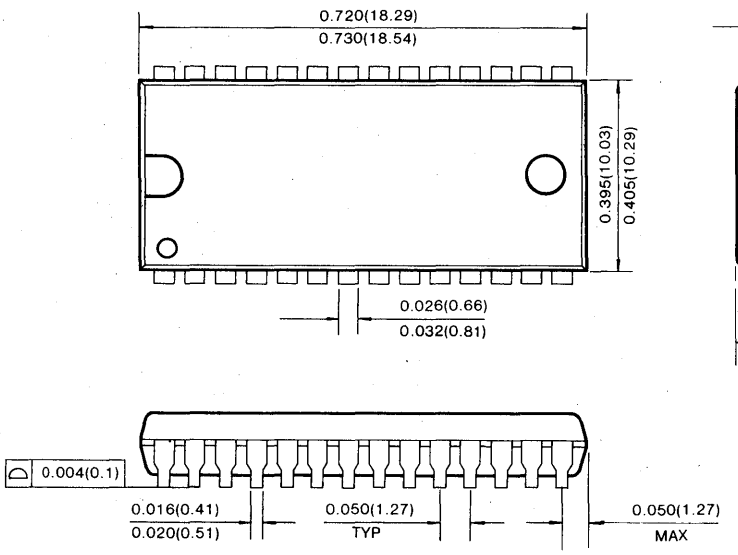
CAS-before-RAS REFRESH COUNTER TEST CYCLE



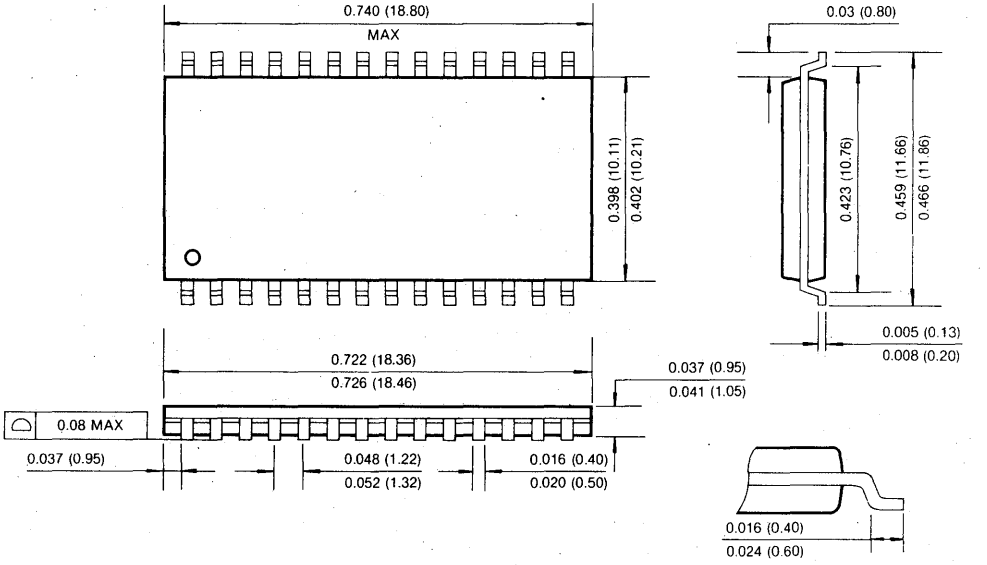
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



512K ×8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM48V514B/BL/BLL-6	60ns	17ns	110ns	24ns
KM48V514B/BL/BLL-7	70ns	20ns	130ns	29ns
KM48V514B/BL/BLL-8	80ns	20ns	150ns	34ns

- **Fast Page Mode with Extended Data Out**
- **Self Refresh operation (LL-version)**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Byte Read/write operation**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Dual +3.3V±0.3V power supply**
- **Refresh Cycle**
  -1024 cycle/16ms (Normal)
  -1024 cycle/128ms (L/LL-ver)
- **Power Dissipation**
  -Standby : 1.8mW (Normal)
  0.36mW (L-Version)
  0.36mW (LL-version)
- **Active (60/70/80) : 255/235/220mW**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP II**

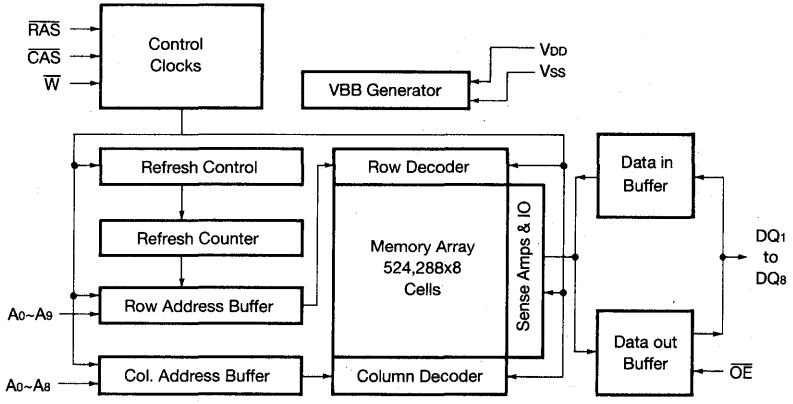
GENERAL DESCRIPTION

The Samsung KM48V514B/BL/BLL is a CMOS high speed 524,288×8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM48V514B/BL/BLL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

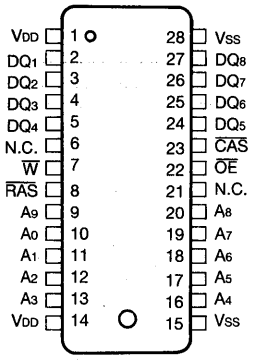
The KM48V514B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



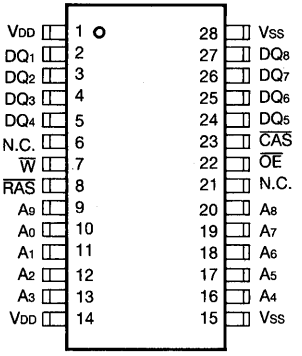
PIN CONFIGURATION (Top Views)

• KM48V514BJ/BLJ/BLLJ



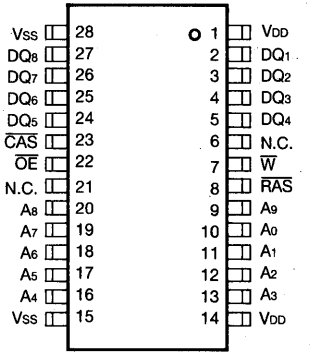
(SOJ)

• KM48V514BT/BLT/BLLT



(TSOP(II)-Forward Type)

• KM48V514BTR/BLTR/BLLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A0-A9	Address Inputs
DQ1~8	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VDD	Power(+3.3V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5~4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5~4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.1	—	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	KM48V514B/BL/BLL-6	I_{CC1}	-	70	mA
	KM48V514B/BL/BLL-7			65	mA
	KM48V514B/BL/BLL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM48V514B/BL/BLL-6	I_{CC3}	-	70	mA
	KM48V514B/BL/BLL-7			65	mA
	KM48V514B/BL/BLL-8			60	mA
EDO Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM48V514B/BL/BLL-6	I_{CC4}	-	55	mA
	KM48V514B/BL/BLL-7			50	mA
	KM48V514B/BL/BLL-8			45	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM48V514B	I_{CC5}	-	500	μA
	KM48V514BL			100	μA
	KM48V514BLL			100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48V514B/BL/BLL-6	I_{CC6}	-	70	mA
	KM48V514B/BL/BLL-7			65	mA
	KM48V514B/BL/BLL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{DD}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=0.2V D_{IN}=Don't Care, T_{RC}=125μS T_{RAS}=T_{RAS} min.~300ns	KM48V514BL	I_{CC7}	-	200	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_9=V_{DD}-0.2V or 0.2V DQ_1-DQ_8=V_{DD}-0.2V, 0.2V or Open	KM48V514BLL	I_{CC8}	-	100	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		17		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Turn-off delay from $\overline{CAS}$	t_{CEZ}	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	17		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	15	10,000	20	10,000	ns	12
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		50		55		ns	6
Write command pulse width	t_{WP}	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	15		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (Normal)	t_{REF}		16		16		16	ms	
Refresh Period(L & LL-ver)	t_{REF}		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	42		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		95		105		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Hyper Page mode cycle time	t_{HPC}	24		29		34		ns	12
Hyper Page mode read-modity-write cycle time	t_{HPRWC}	76		81		91		ns	12
$\overline{CAS}$ precharge time (Hyper Page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	15	3	20	3	20	ns	7
$\overline{OE}$ commend hold time	t_{OEH}	15		20		20		ns	
$\overline{OE}$ to output in Low-z	t_{OLZ}	3		3		3		ns	3
Output data hold time	t_{DOH}	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	0	15	0	20	0	20	ns	7

AC CHARACTERISTICS (Continued)

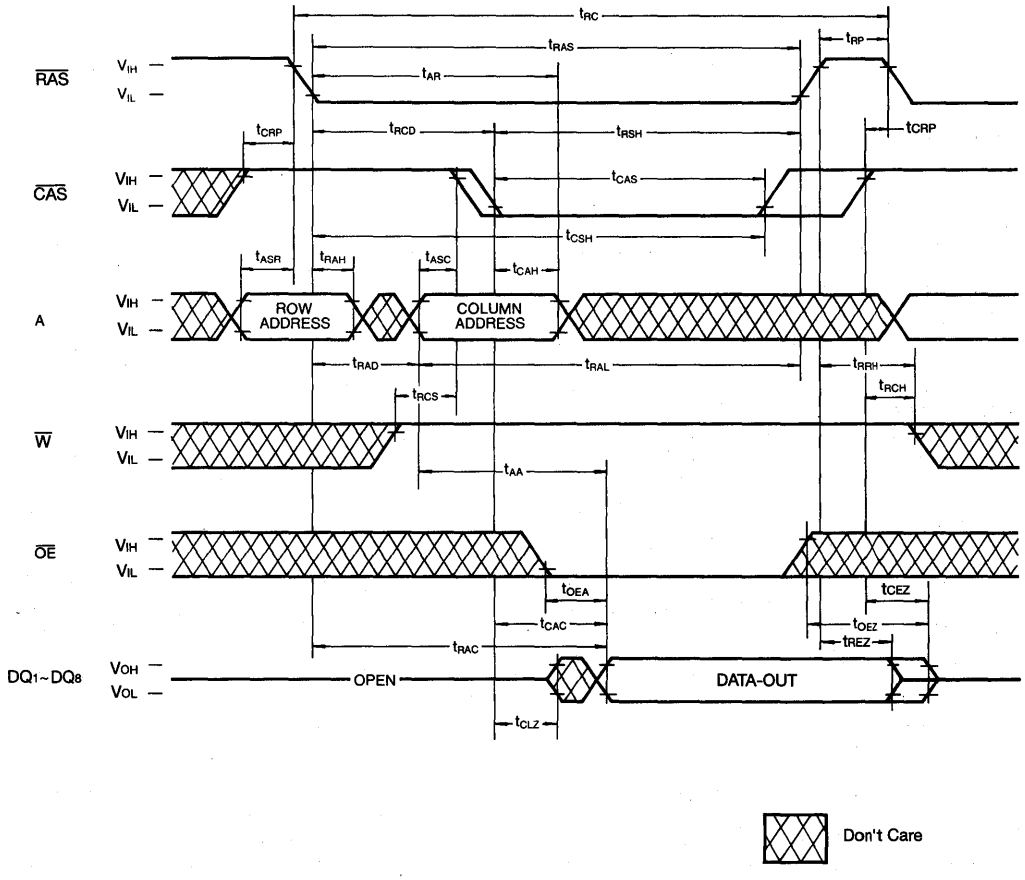
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{W}$ to data delay	tWED	15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ Pulse width (Hyper Page Cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh	tRASS	100		100		100		μs	13
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	13
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	13

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs except tHPC and tHPRWC.
3. Measured with a load equivalent to 1 TTL loads and 100pF, V_{oh}/V_{ol}=2.0/0.8V.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD $\geq$ tRCD (max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS $\geq$ tWCS(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD $\geq$ tCWD(min), tRWD $\geq$ tRWD(min) and tAWD $\geq$ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. tASC $\geq$ tCPmin, Assume tT=2.0 ns
13. 1024 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (LL-ver)
14. If $\overline{RAS}$ goes high befored $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going, If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going

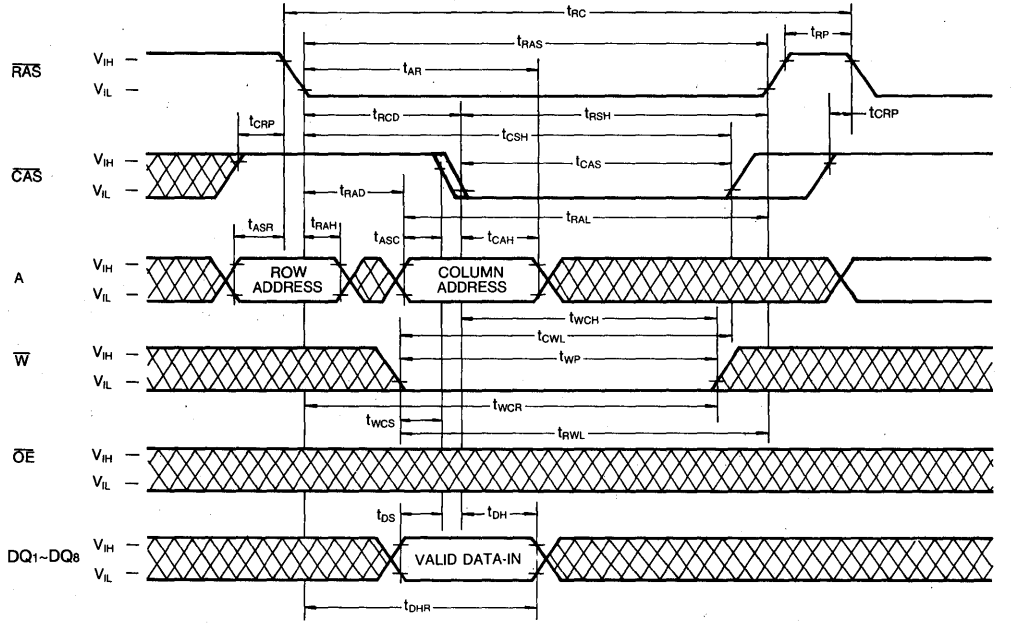
TIMING DIAGRAMS

READ CYCLE



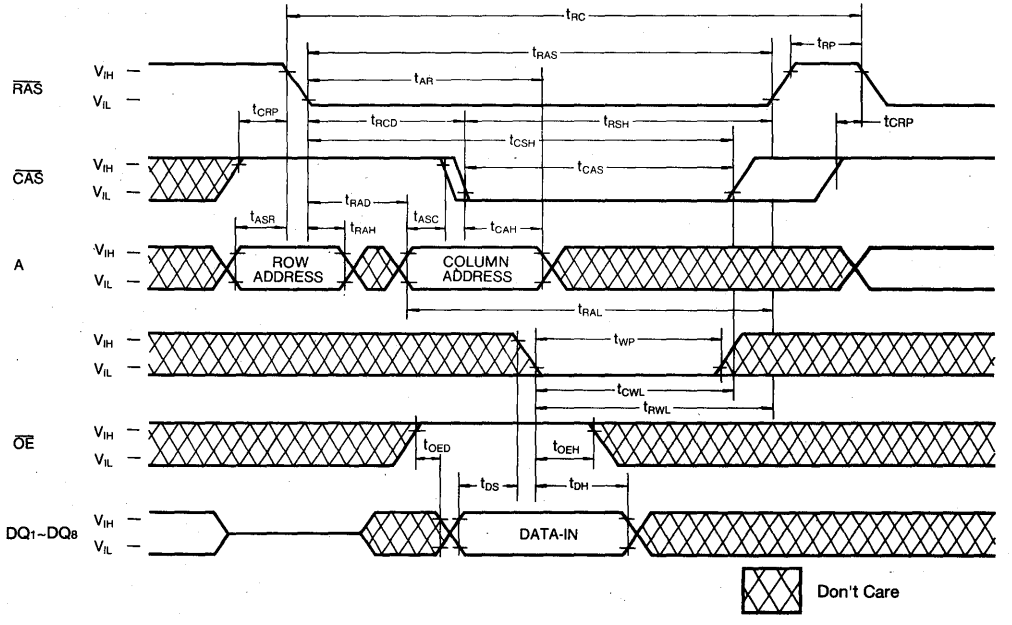
WRITE CYCLE (EARLY CYCLE)

NOTE : DOUT=OPEN

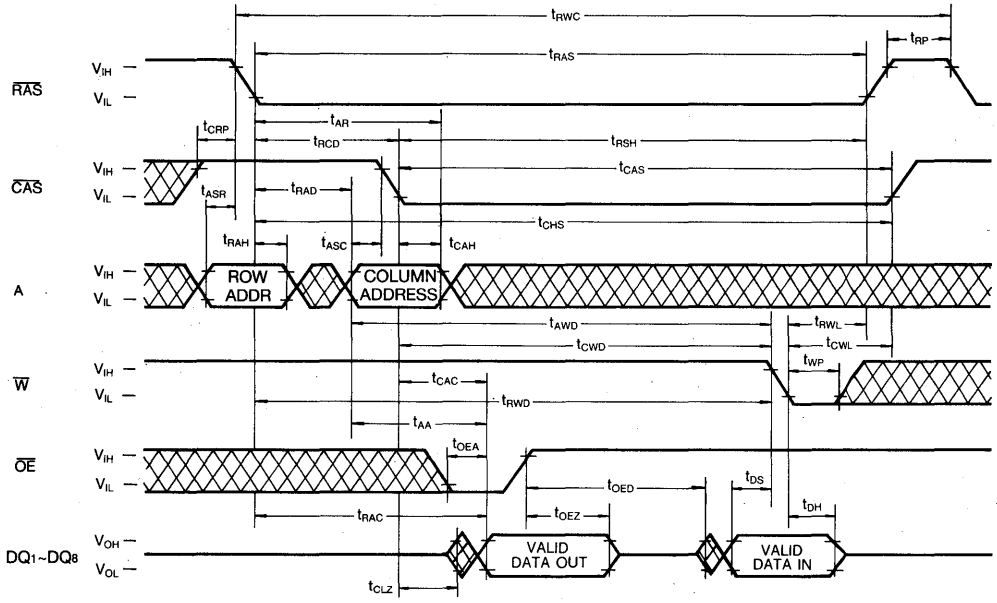


WRITE CYCLE (OE CONTROLLED WRITE)

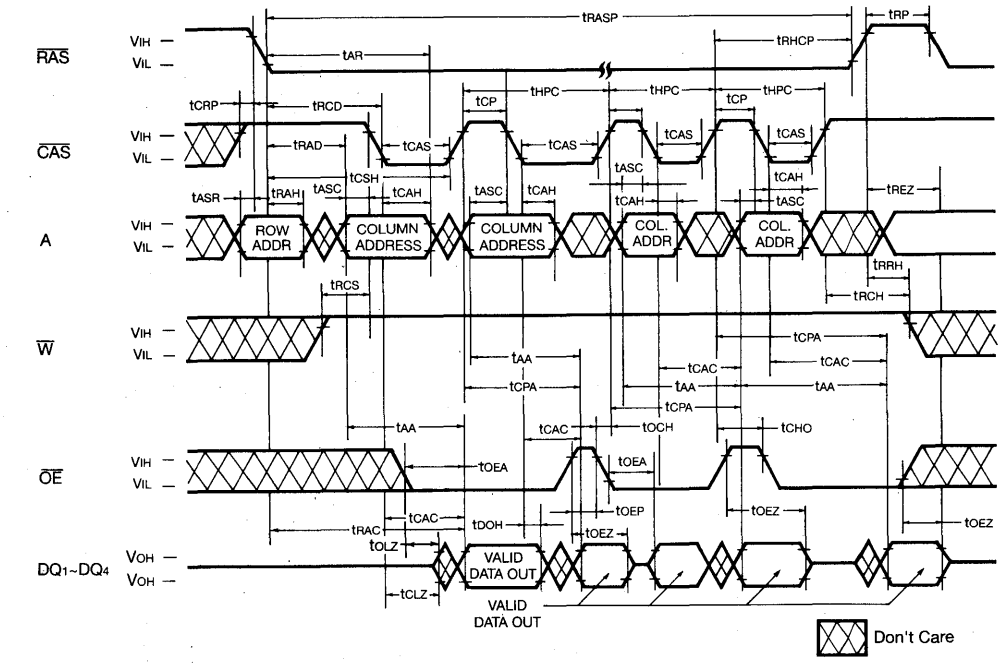
NOTE : DOUT=OPEN



READ-MODIFY-WRITE CYCLE

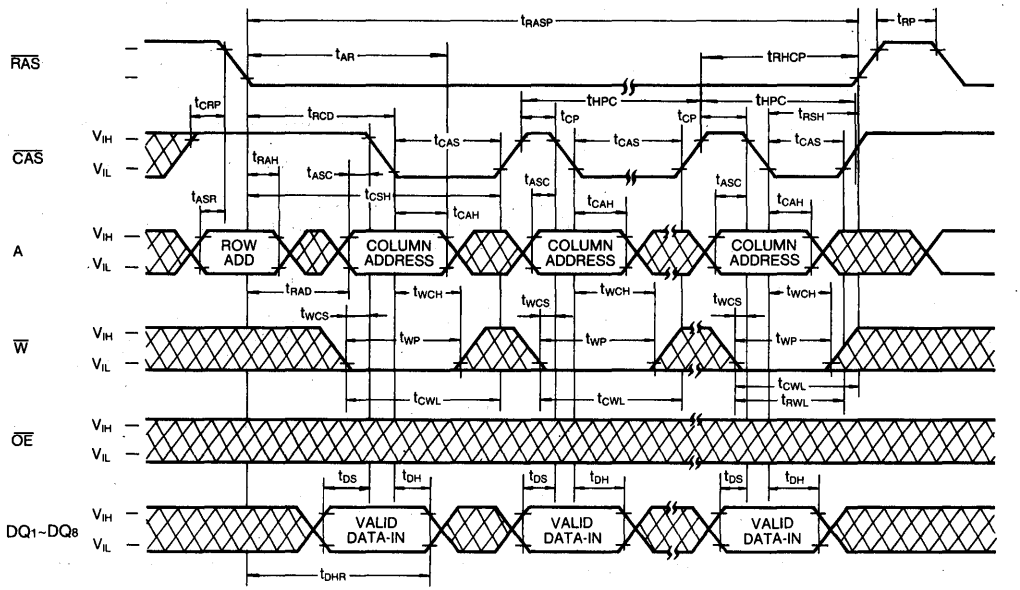


HYPER PAGE READ CYCLE

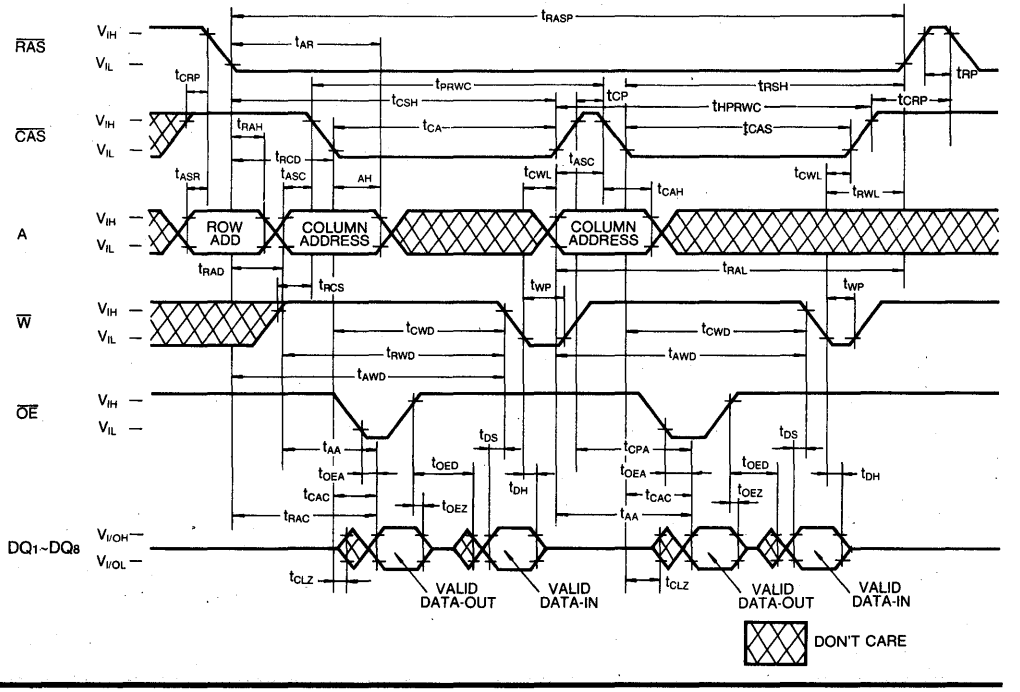


SAMSUNG ELECTRONICS

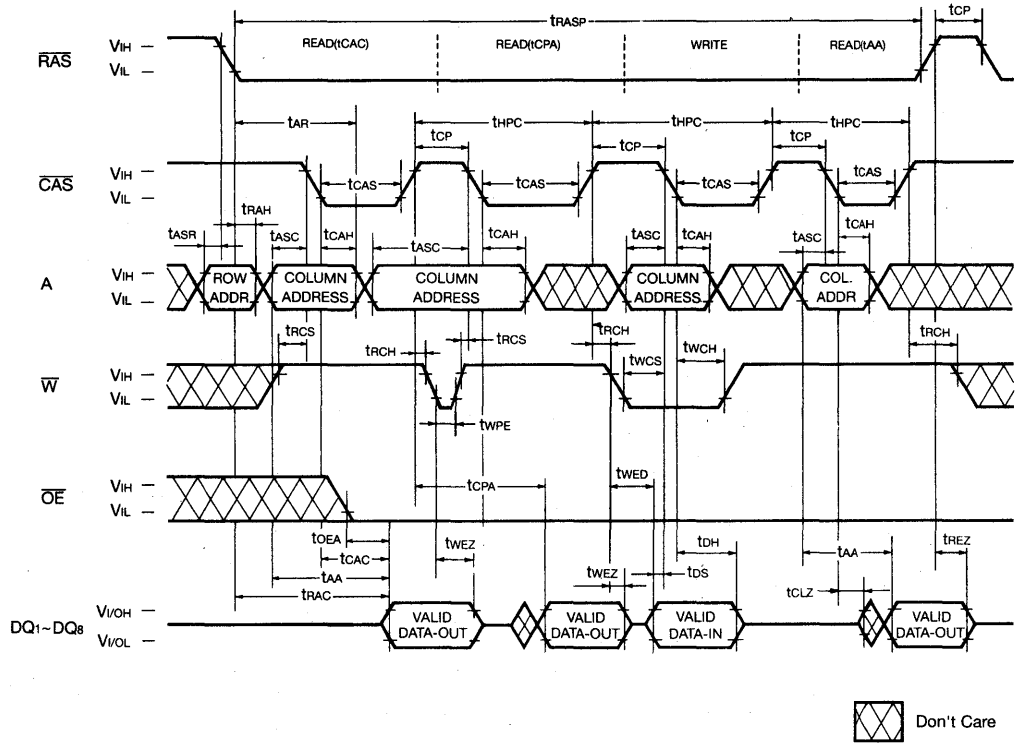
HYPER PAGE WRITE CYCLE (EARLY WRITE)



HYPER PAGE READ-MODIFY-WRITE CYCLE

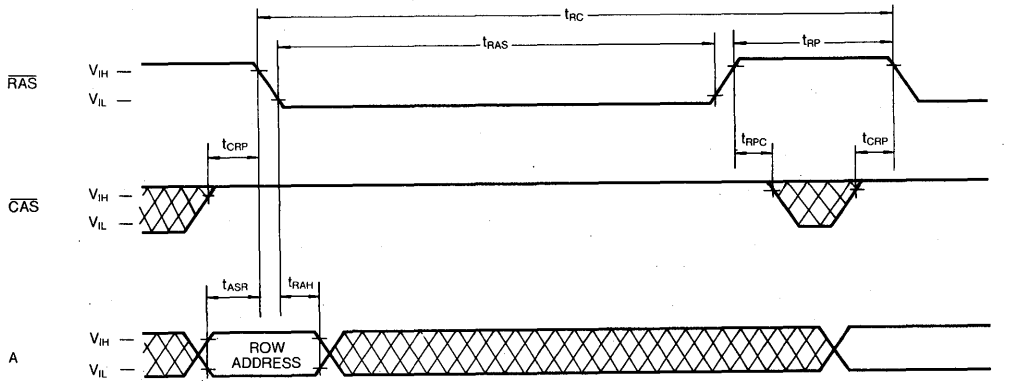


HYPER PAGE READ AND WRITE MIXED CYCLE



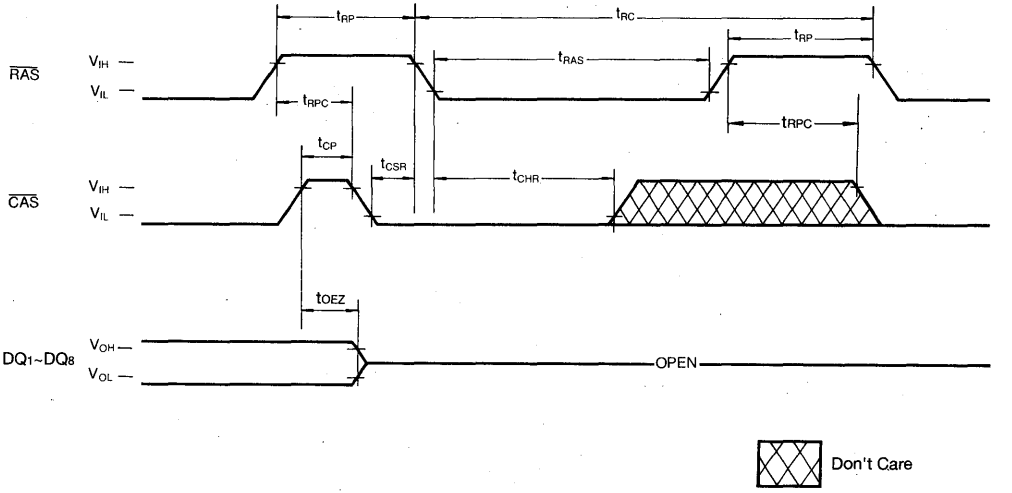
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, DIN=Don't Care
Dout=Open

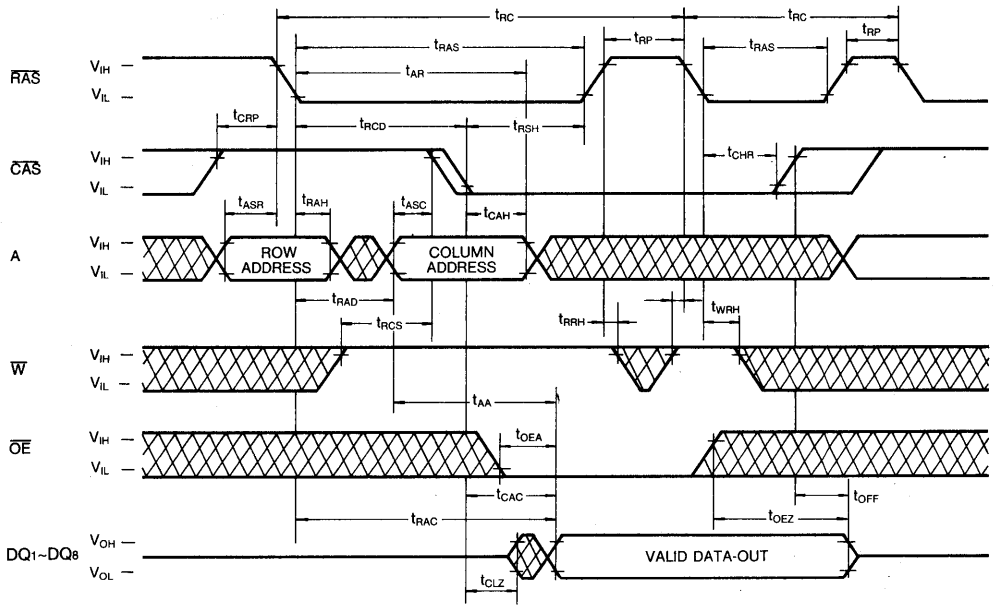


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

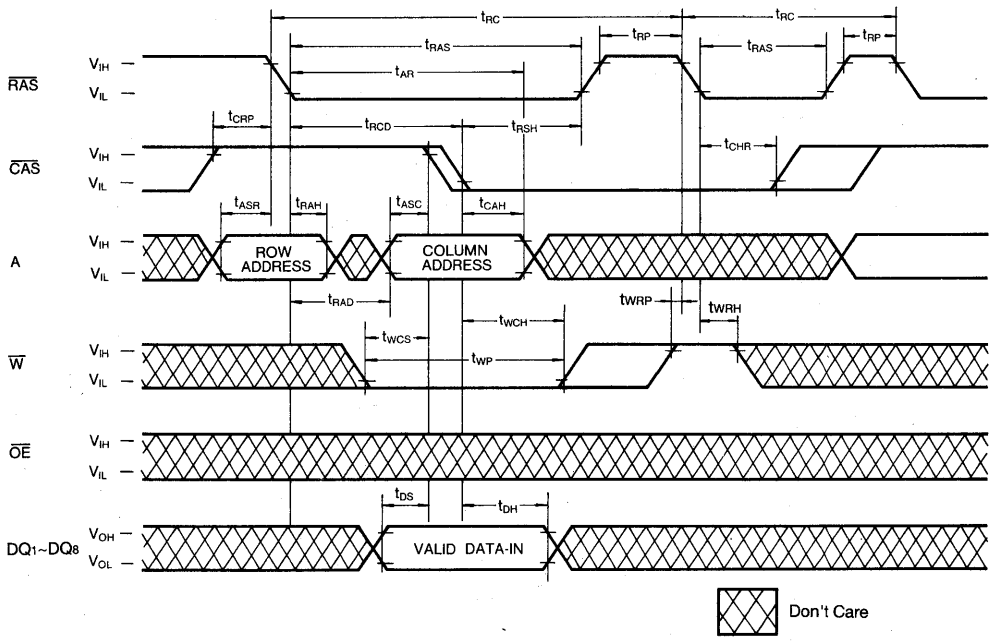
NOTE : $\overline{W}$, $\overline{OE}$, A=Don't Care



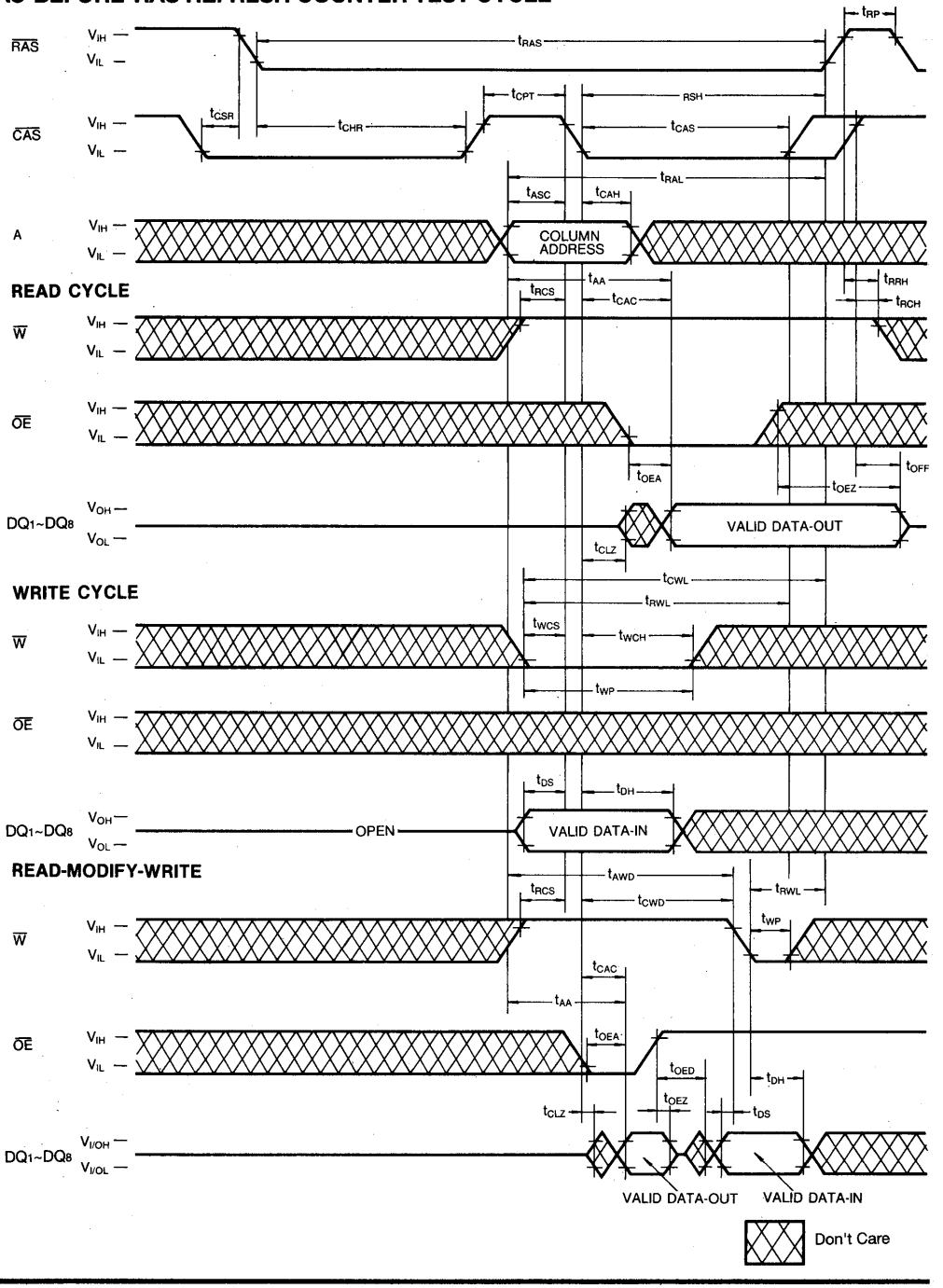
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



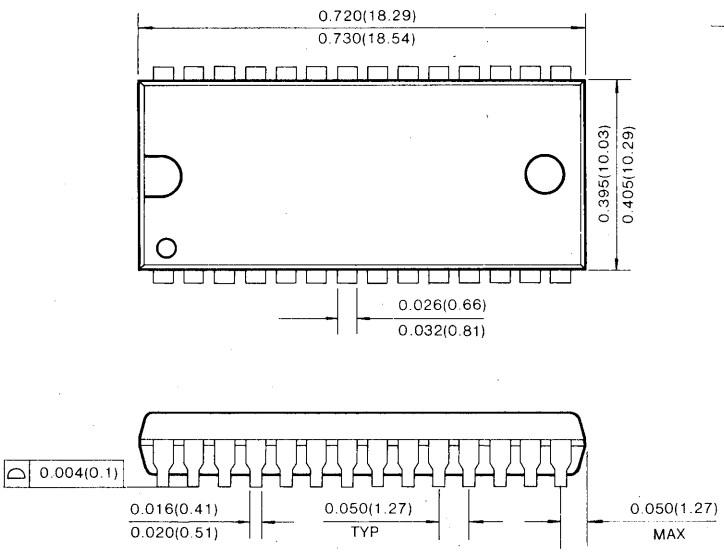
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



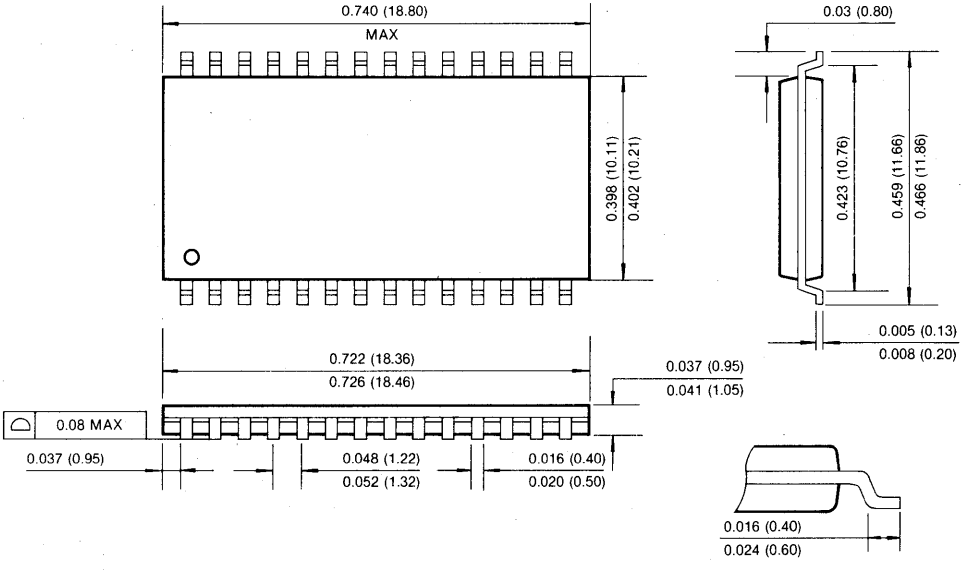
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



256K × 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM416V256B/BL/BLL-6	60ns	15ns	110ns
KM416V256B/BL/BLL-7	70ns	20ns	130ns
KM416V256B/BL/BLL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Self Refresh operation (LL-version)**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +3.3V±0.3V power supply**
- **Refresh Cycle**
  - **-512 cycle/8ms (Normal)**
  - **-512 cycle/64ms (L-version)**
  - **-512 cycle/128ms (LL-version)**
- **Power Dissipation**
  - **-Standby: 1.8mW (Normal)**
  - **0.36mW (L-version)**
  - **0.36mW (LL-version)**
  - **-Active (60/70/80): 325/290/270mW**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP II**

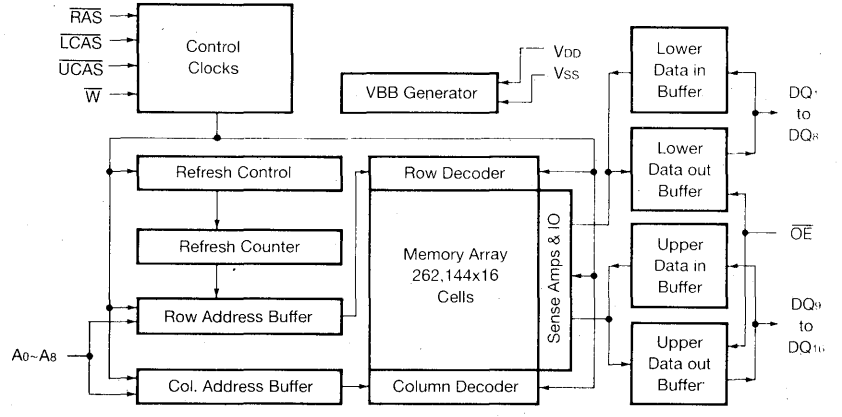
GENERAL DESCRIPTION

The Samsung KM416V256B/BL/BLL is a CMOS high speed 262,144 bit × 16 Dynamic Random Access Memory. Its design is optimized for low power applications such as portable computer and hand-held system.

The KM416V256B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

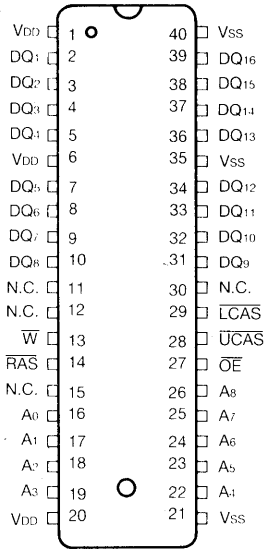
The KM416V256B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

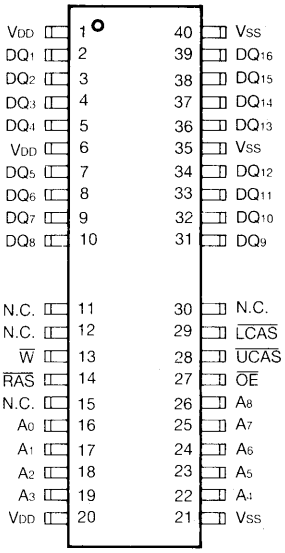


PIN CONFIGURATION (Top Views)

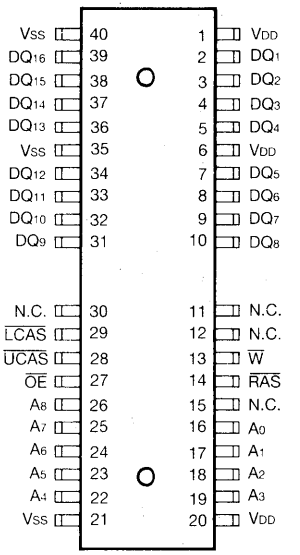
• KM416V256BJ/BLJ/BLLJ



• KM416V256BT/BLT/BLLT



• KM416V256BTR/BLTR/BLLTR



Pin Name	Pin Function
A0-A8	Address Inputs
DQ1-16	Data In/Out
VSS	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe

Pin Name	Pin Function
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VDD	Power(+3.3V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to VSS	VIN, VOUT	-0.5~4.6	V
Voltage on VDD supply relative to VSS	VDD	-0.5~4.6	V
Storage Temperature	Tstg	-55 to + 150	C
Power Dissipation	PD	1	W
Short Circuit Output Current	IOS	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.1	—	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{RC}=min.)	KM416V256B/BL/BLL-6 KM416V256B/BL/BLL-7 KM416V256B/BL/BLL-8	I_{CC1}	-	90 80 75	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM416V256B/BL/BLL-6 KM416V256B/BL/BLL-7 KM416V256B/BL/BLL-8	I_{CC3}	-	90 80 75	mA mA mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC}=min.)	KM416V256B/BL/BLL-6 KM416V256B/BL/BLL-7 KM416V256B/BL/BLL-8	I_{CC4}	-	60 55 50	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{DD}-0.2V)	KM416V256B KM416V256BL KM416V256BLL	I_{CC5}	-	500 100 100	μA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC}=min.)	KM416V256B/BL/BLL-6 KM416V256B/BL/BLL-7 KM416V256B/BL/BLL-8	I_{CC6}	-	90 80 75	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{DD}-0.2V Input Low Voltage(V_{IL})=0.2V xCAS=V_{IL} D_{IN}=Don't Care, T_{RC}=125μS T_{RAS}=T_{RAS} min.~300ns	KM416V256BL	I_{CC7}	-	200	μA
Self Refresh Current $\overline{RAS}$=x$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_8=V_{DD}-0.2V or 0.2V DQ_1-DQ_{16}=V_{DD}-0.2V, 0.2V or Open	KM416V256BLL	I_{CC8}	-	100	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{DD}+0.3V, all other pins not under test=0 V)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{DD})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_8)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command set-up time	t_{WCS}	0		0		0		ns	8
Write command hold time	t_{WCH}	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		50		55		ns	6
Write command pulse width	t_{WP}	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		ns	

AC CHARACTERISTICS (Continued)

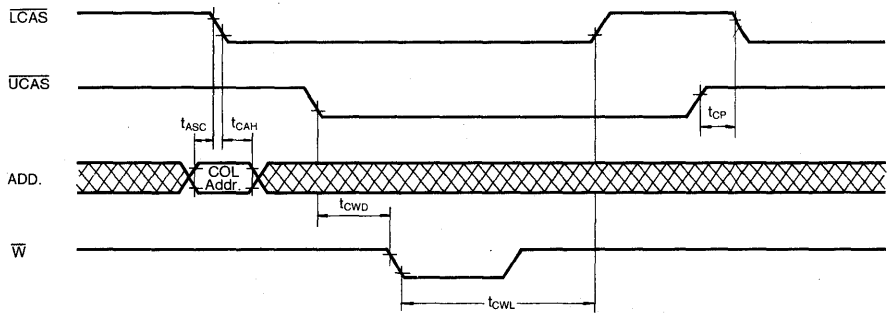
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	15		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (Normal)	t_{REF}		8		8		8	ms	
Refresh period (L-version)	t_{REF}		64		64		64	ms	
Refresh period (LL-version)	t_{REF}		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		95		105		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	80		95		100		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		ns	
Access time from $\overline{OE}$	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data-in delay time	t_{OED}	15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ commend hold time	t_{OEH}	15		20		20		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		100		100		μs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	-50		-50		-50		ns	12

KM416V256B/BL/BLL Truth Table

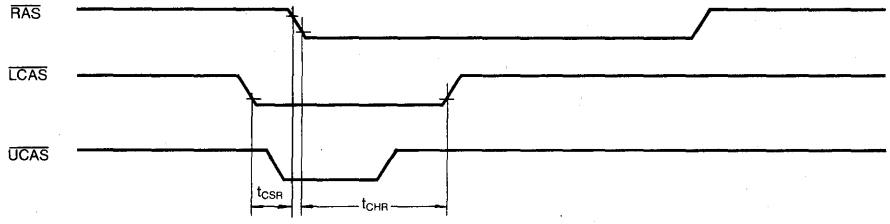
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ_1~DQ_8	DQ_9~DQ_{16}	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

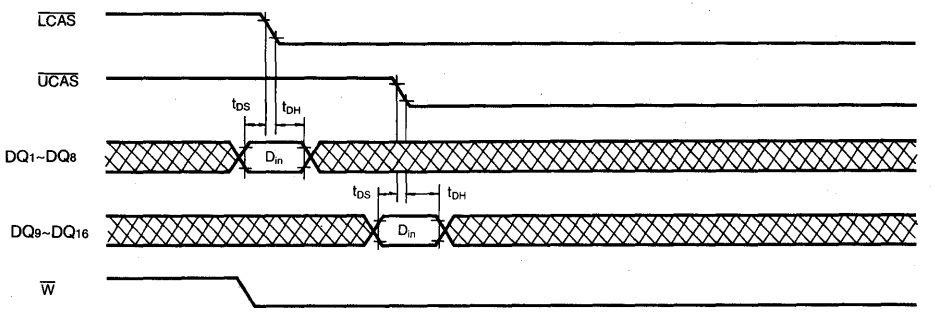
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF, V_{oh}=2.0V and V_{ol}=0.8V
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. t_{OFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. 512 cycles of burst refresh must be executed within 8ms before and after self refresh, In order to meet refresh specification.
13. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
14. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
15. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



17. t_{CSR} is referenced to darlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
18. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

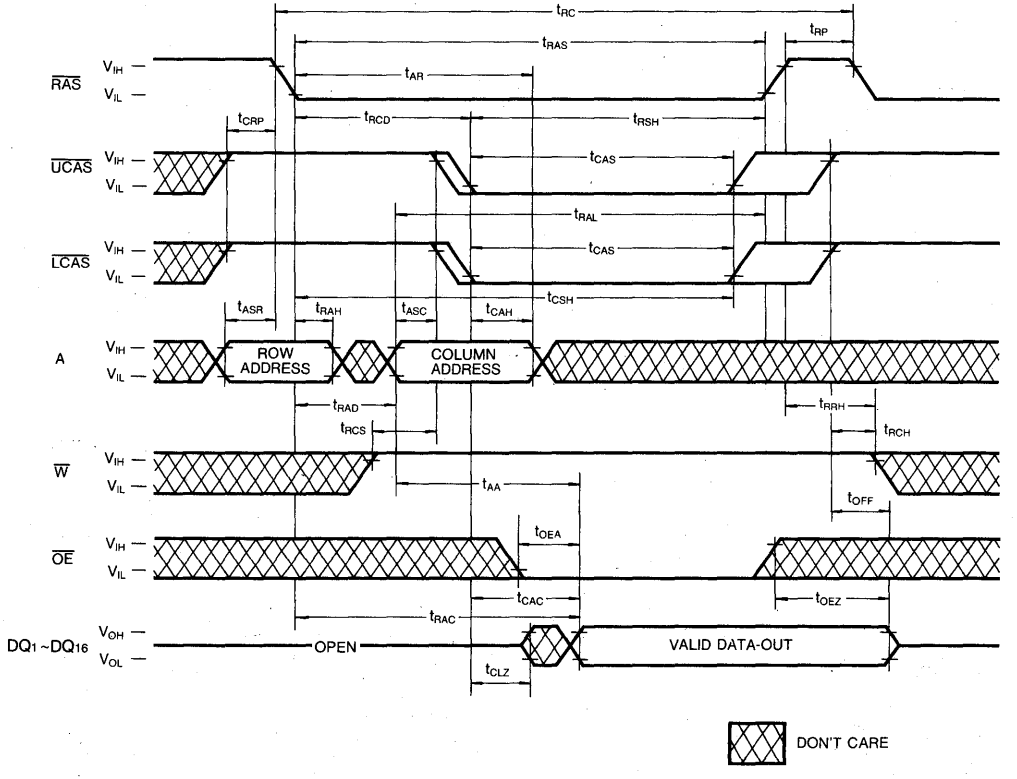


19. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim8)}$, upper byte $D_{in(9\sim16)}$.



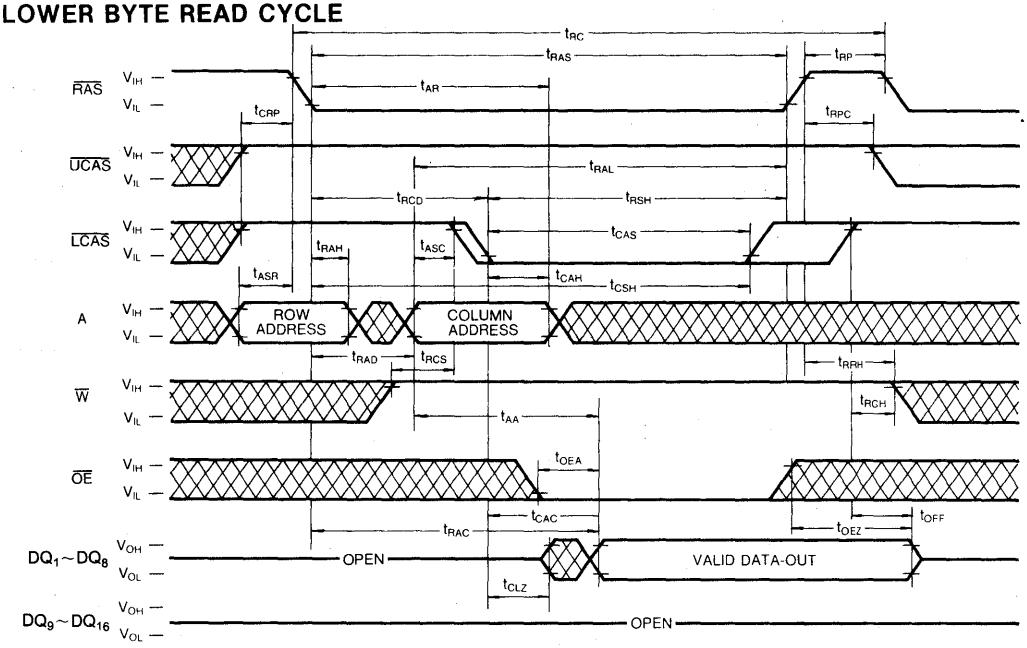
TIMING DIAGRAMS

WORD READ CYCLE

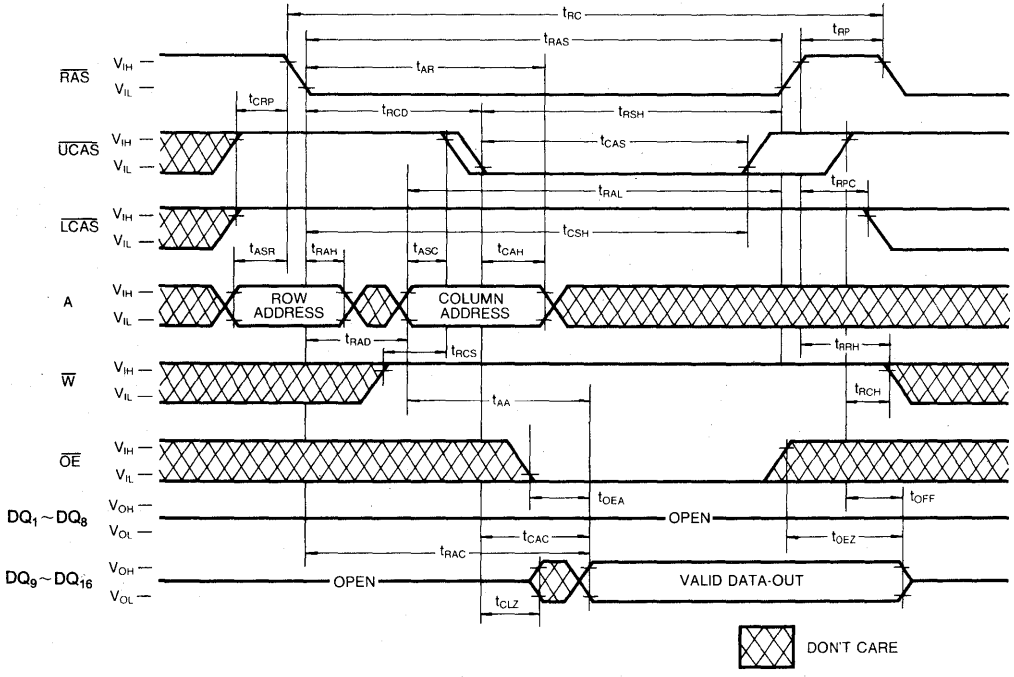


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

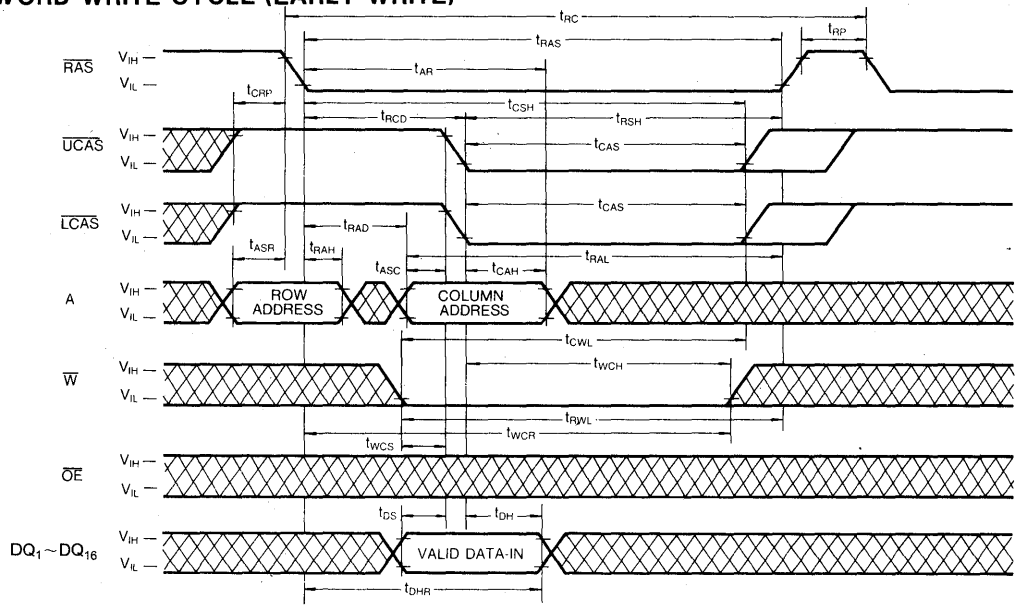


UPPER BYTE READ CYCLE

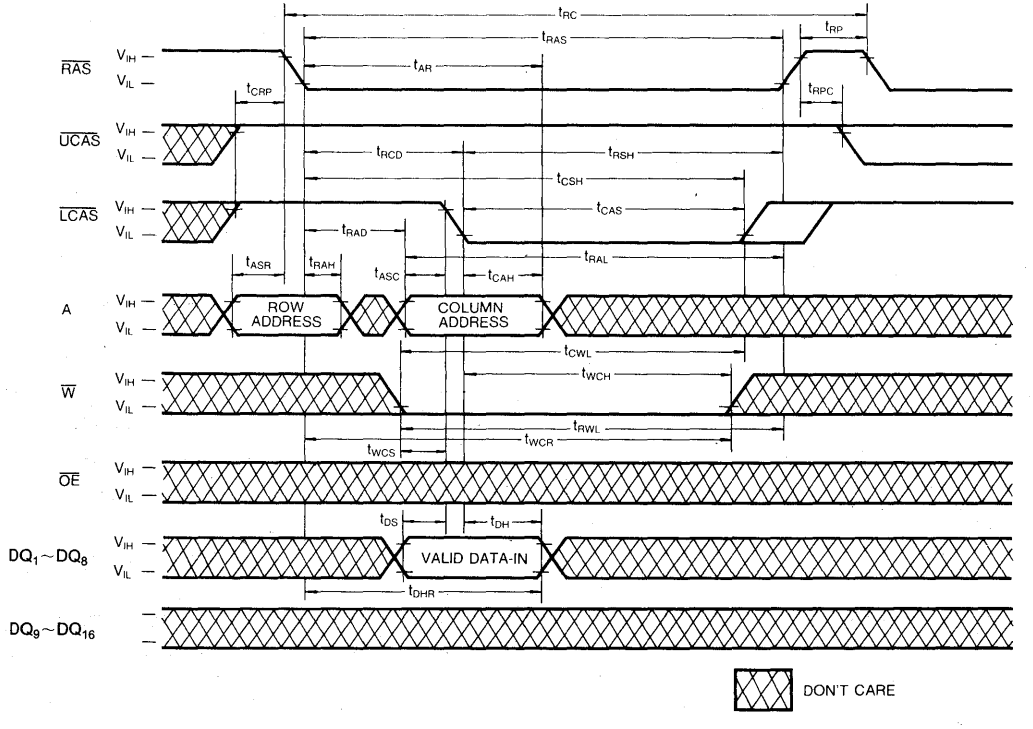


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)

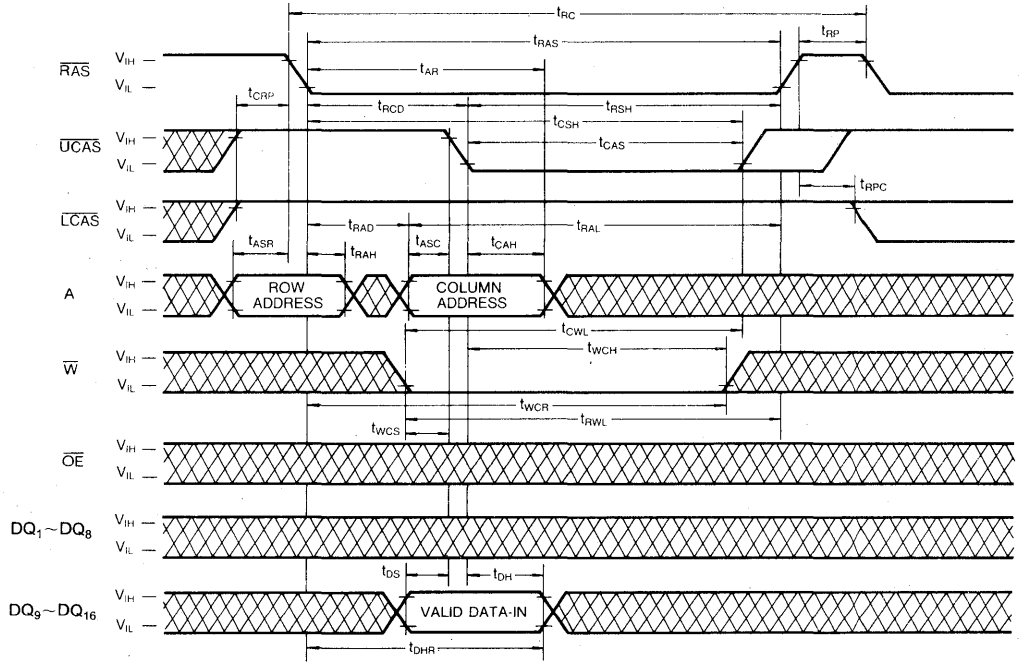


LOWER BYTE WRITE CYCLE (EARLY WRITE)

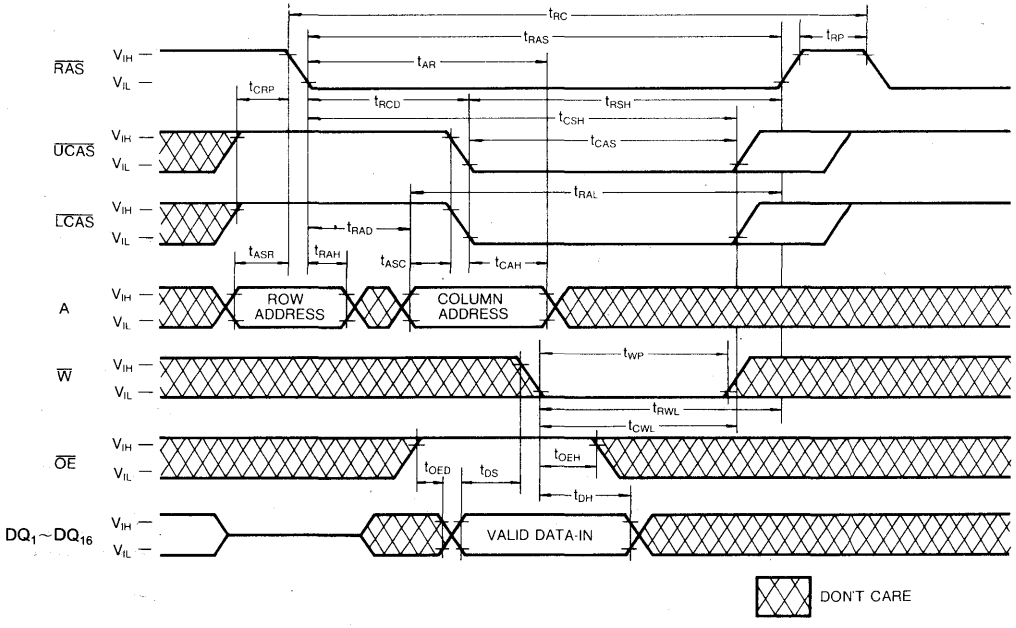


TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

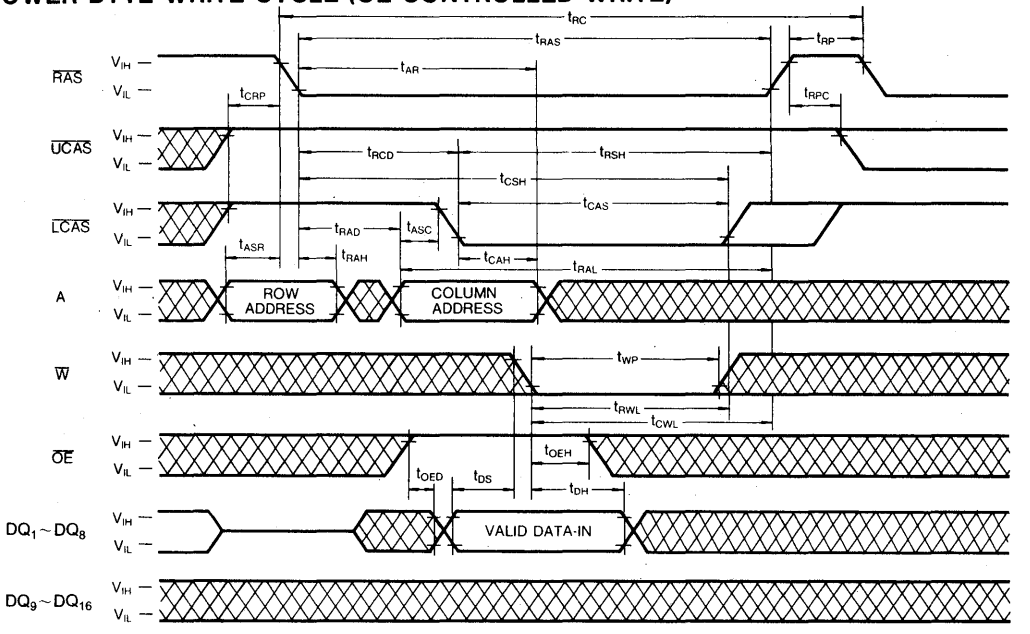


WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

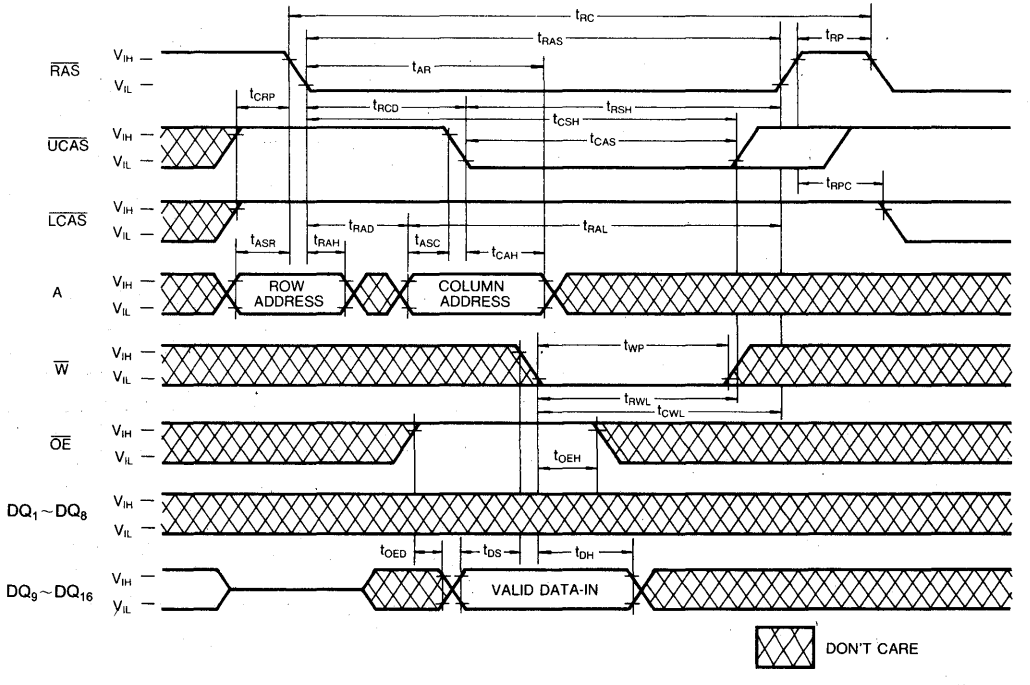


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

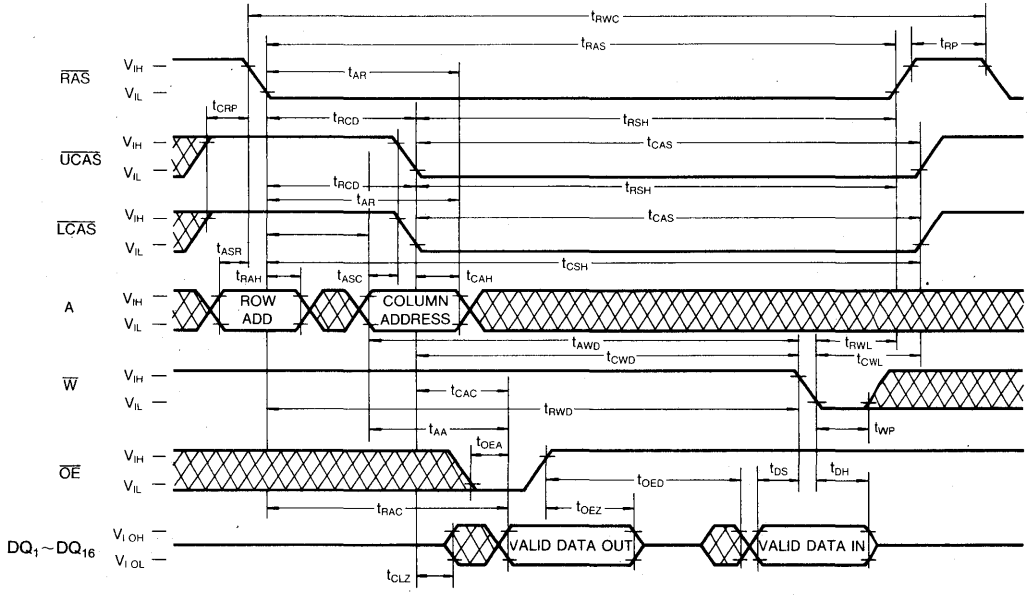


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

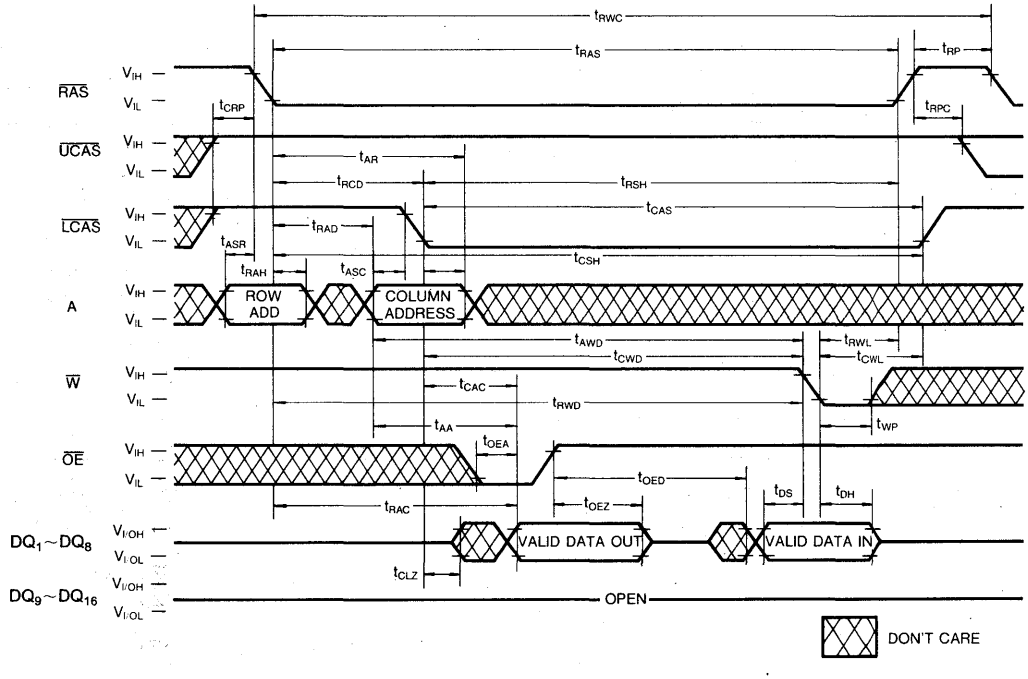


TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

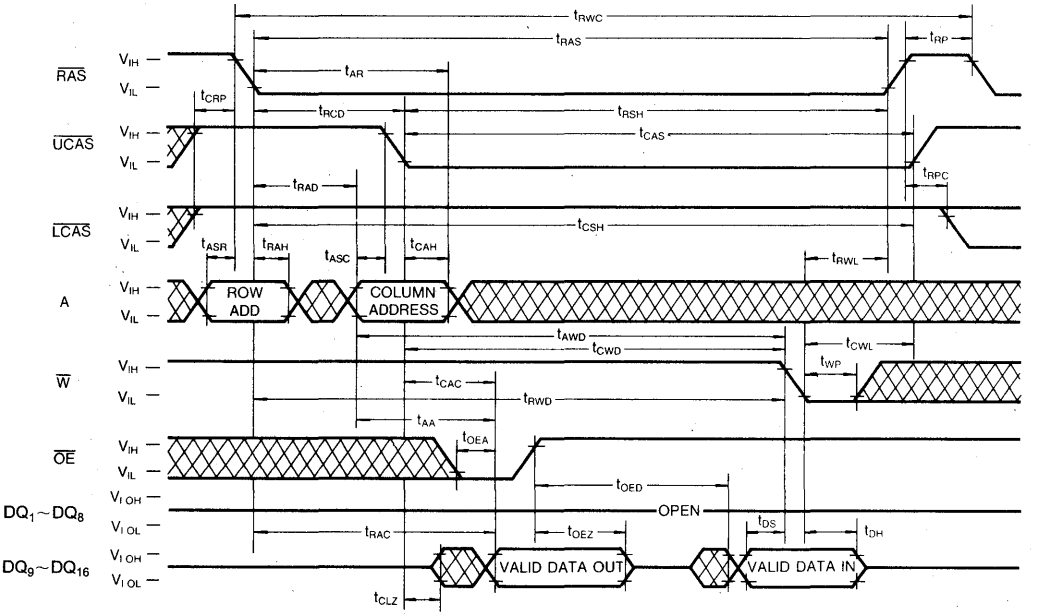


LOWER-BYTE READ-MODIFY-WRITE CYCLE

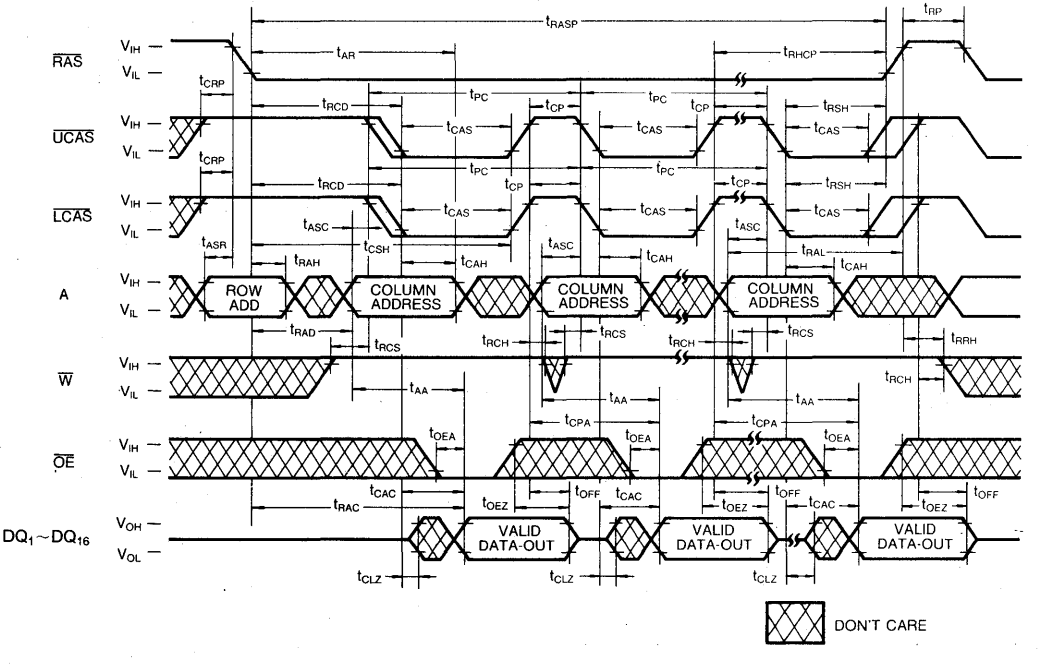


TIMING DIAGRAMS (Continued)

UPPER-BYTE READ-MODIFY-WRITE CYCLE

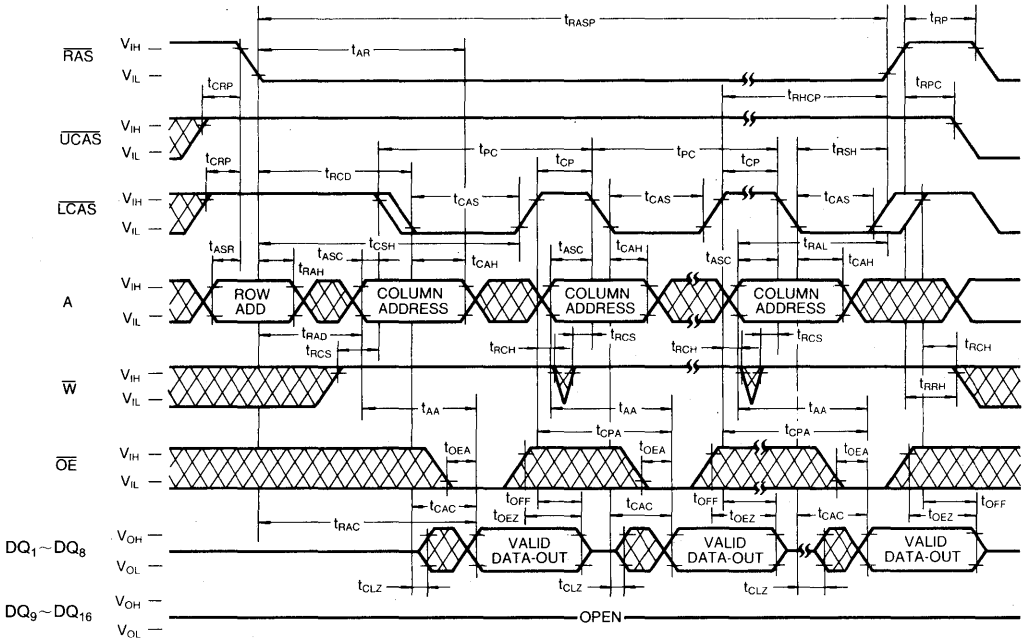


FAST PAGE MODE WORD READ CYCLE

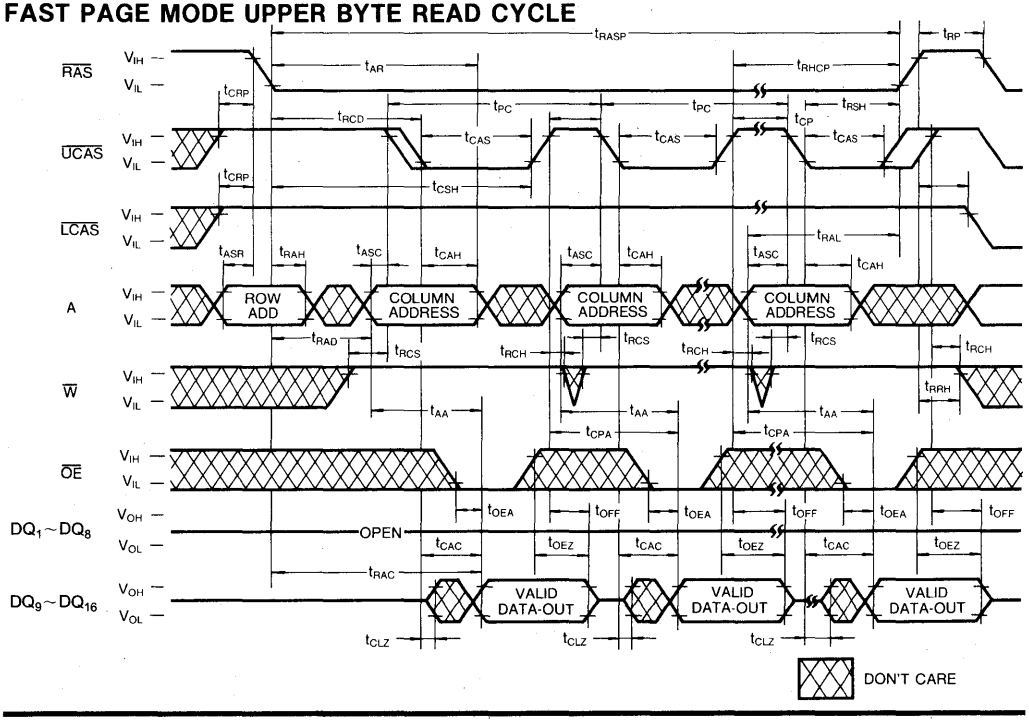


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE

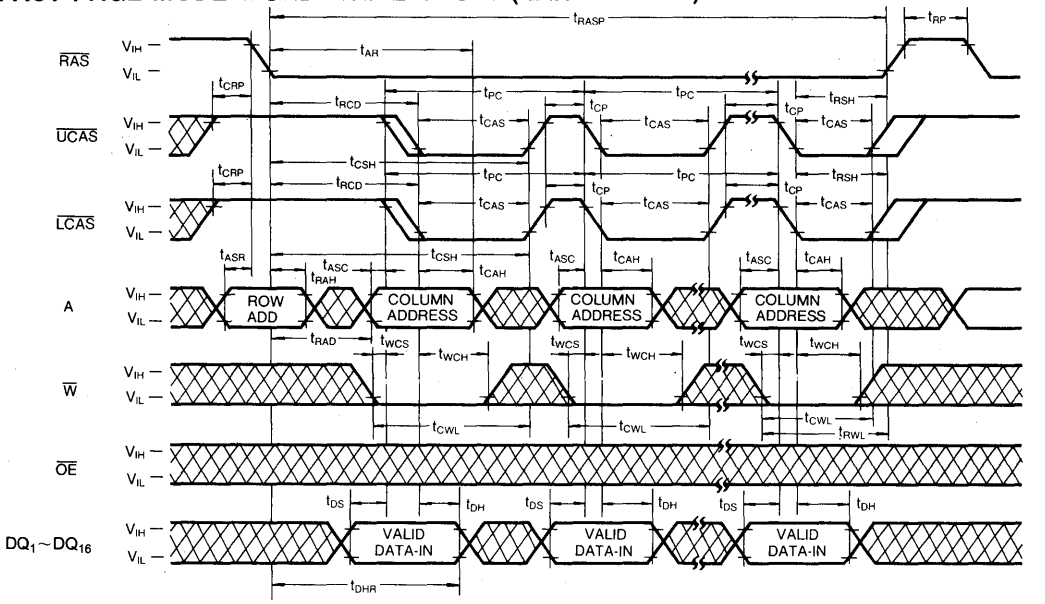


FAST PAGE MODE UPPER BYTE READ CYCLE

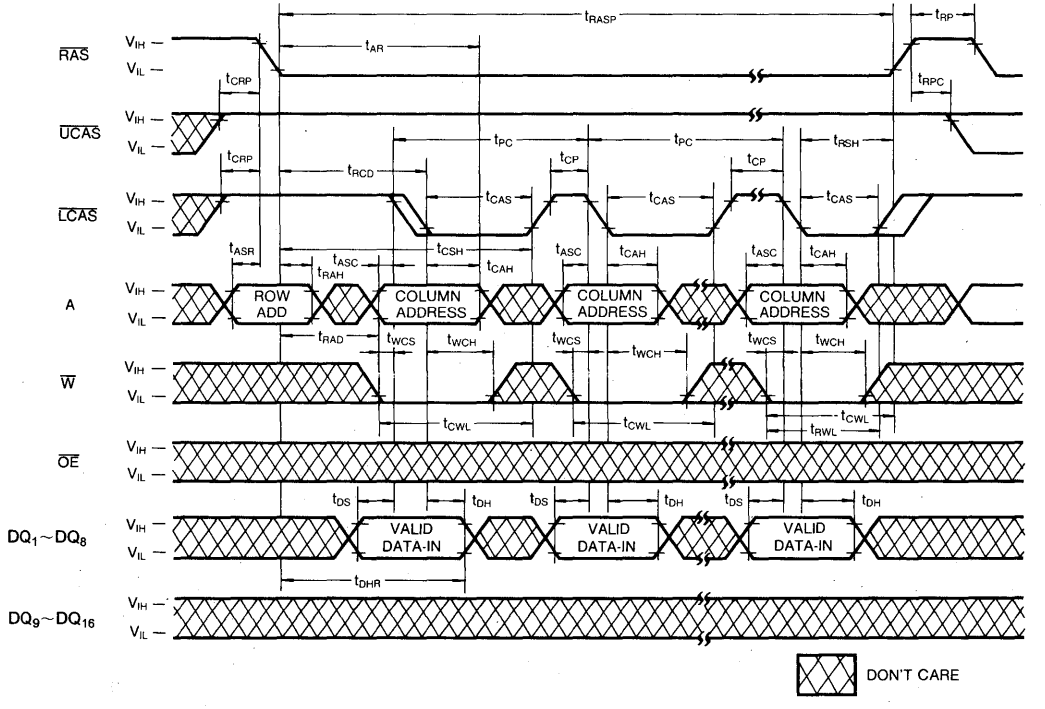


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

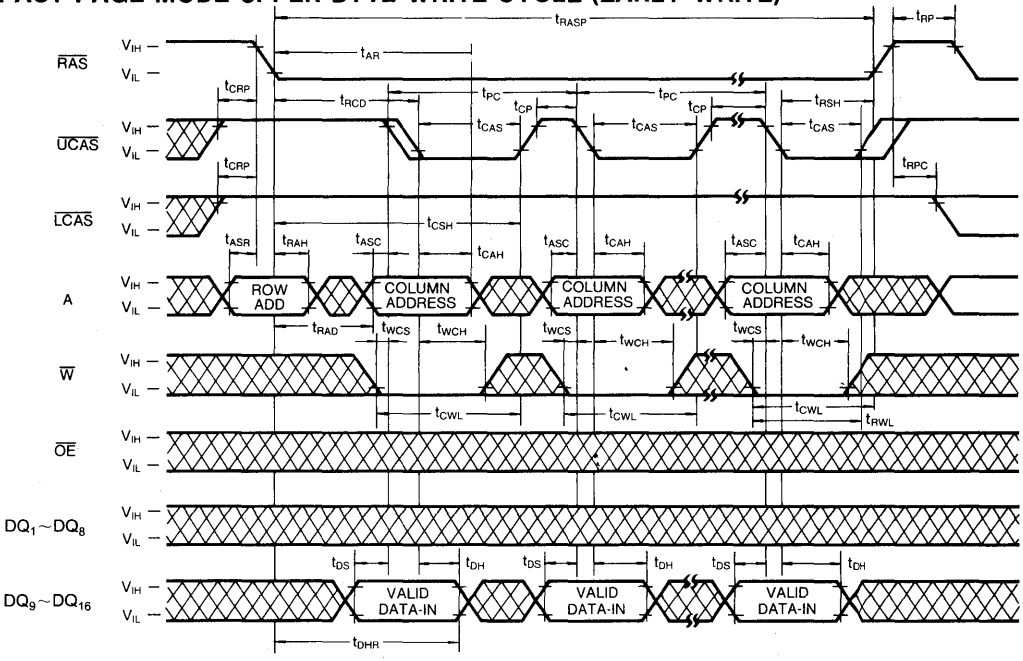


FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)

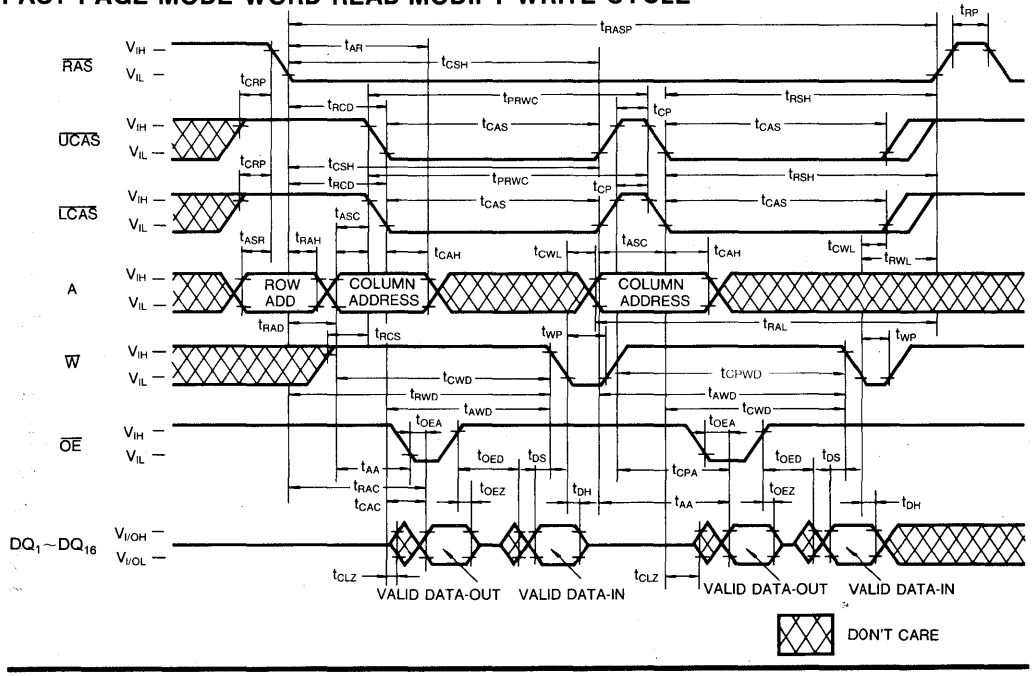


TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)



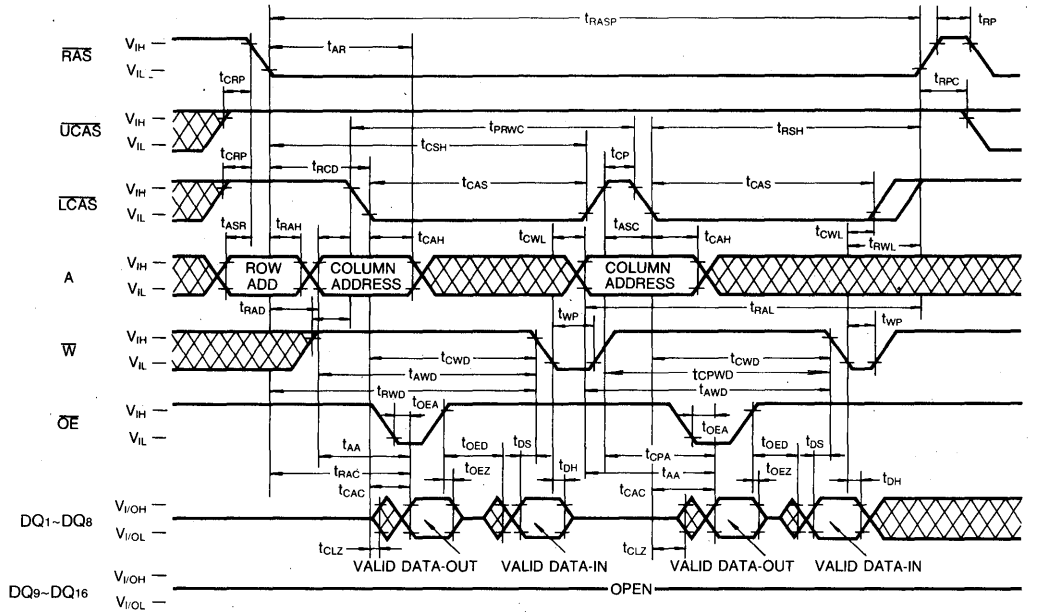
FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE



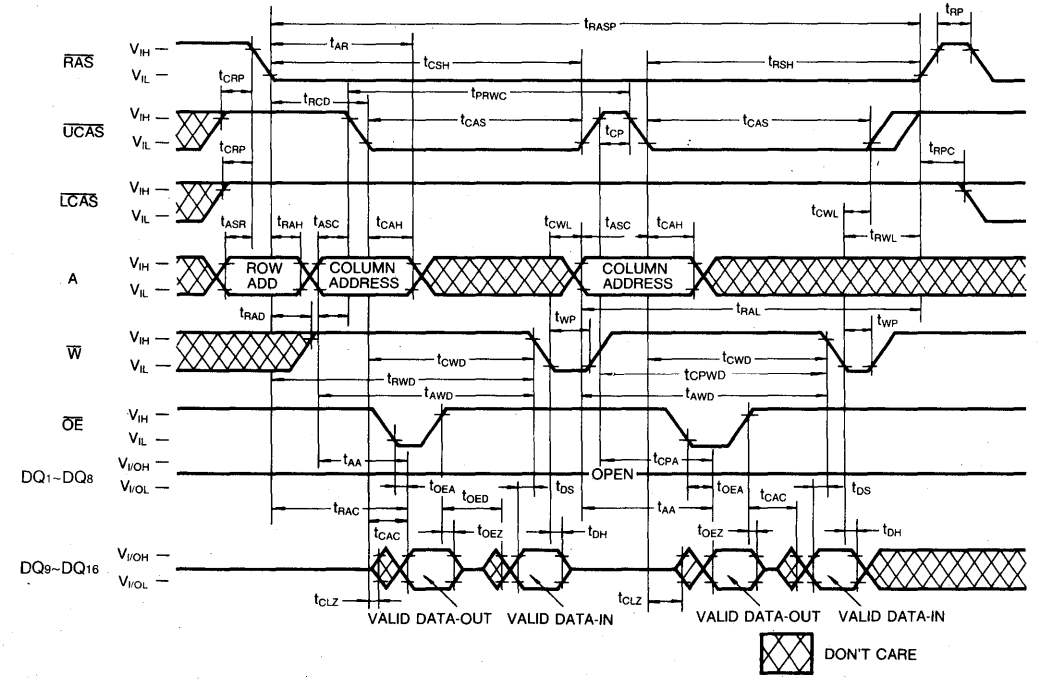
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER-BYTE READ-MODIFY-WRITE CYCLE



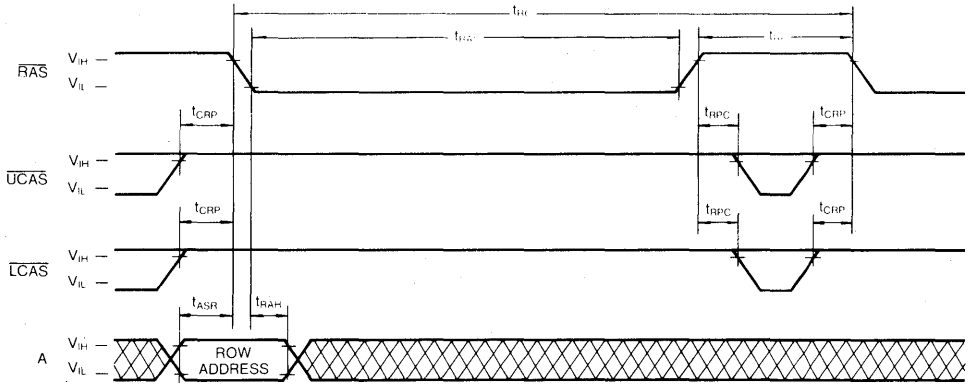
FAST PAGE MODE UPPER-BYTE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

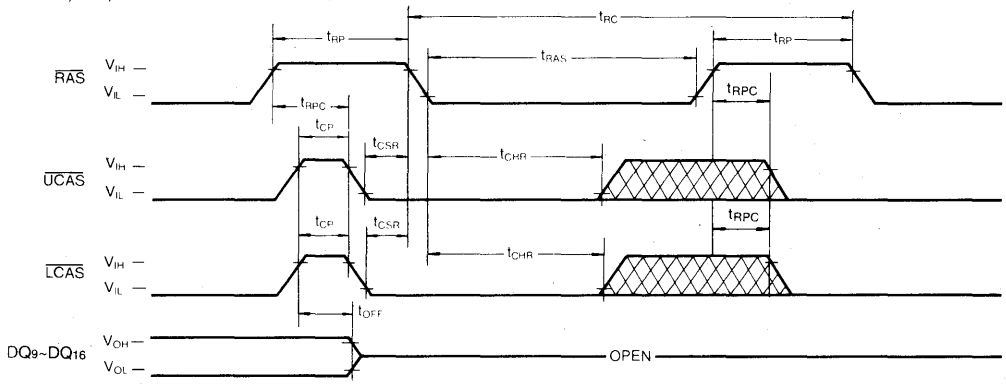
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



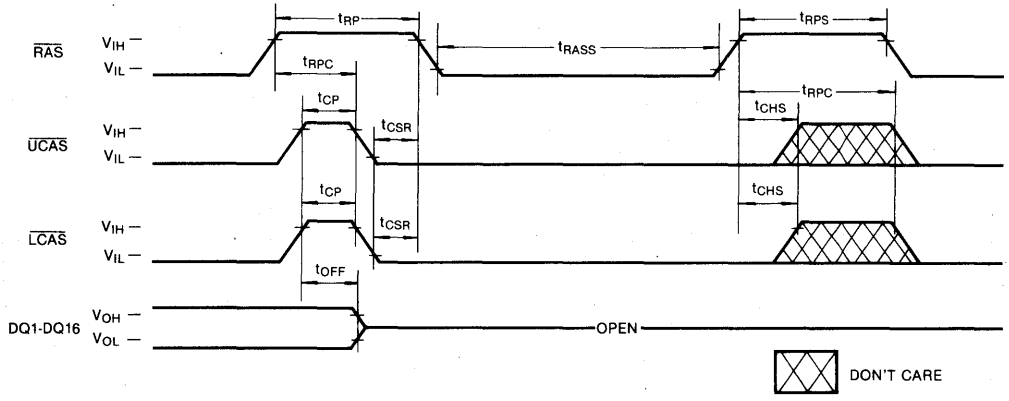
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: W, OE, A = Don't Care



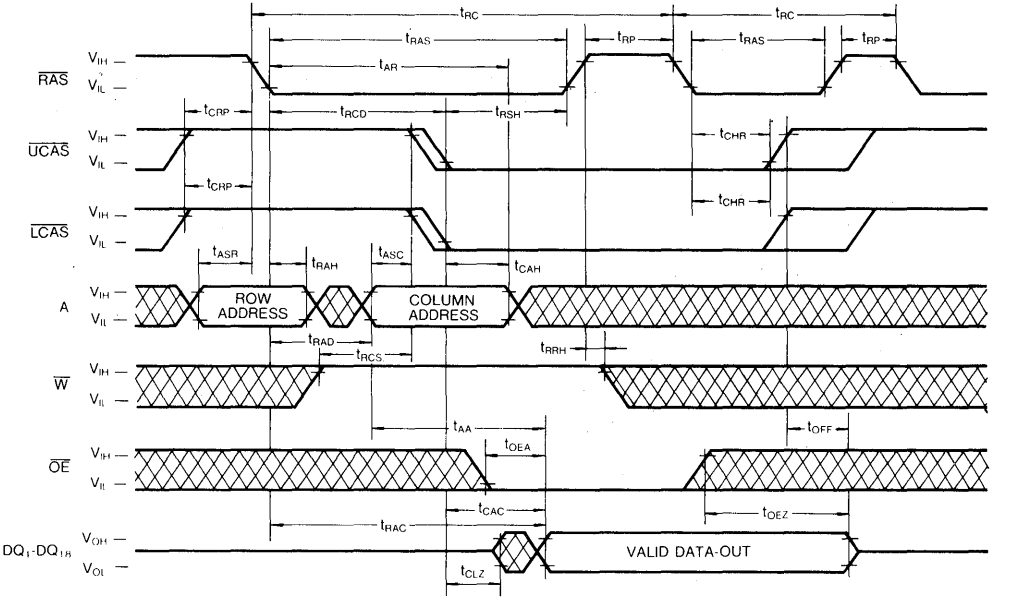
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care

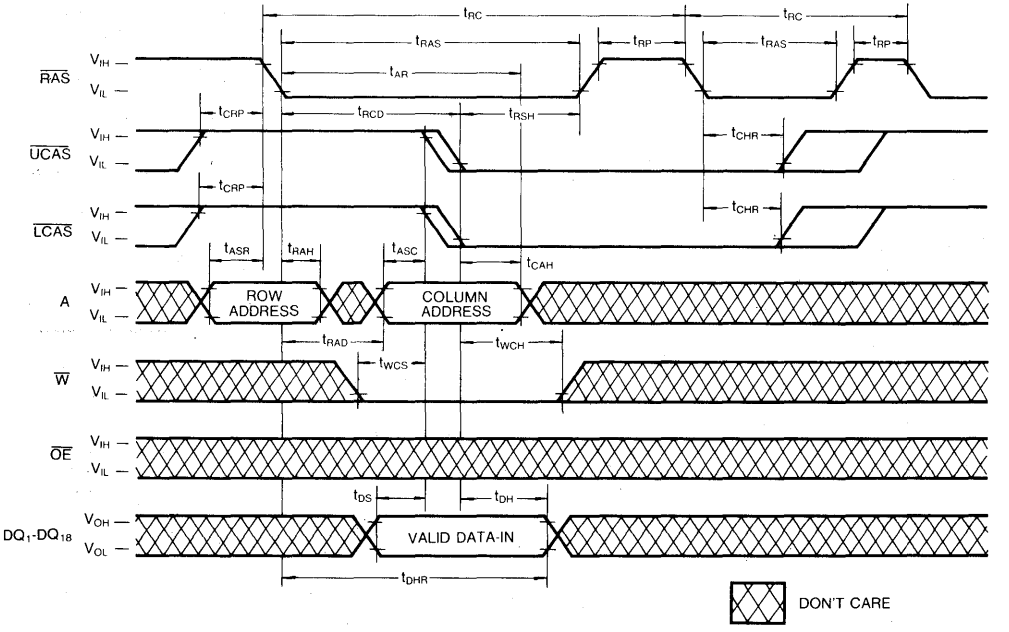


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

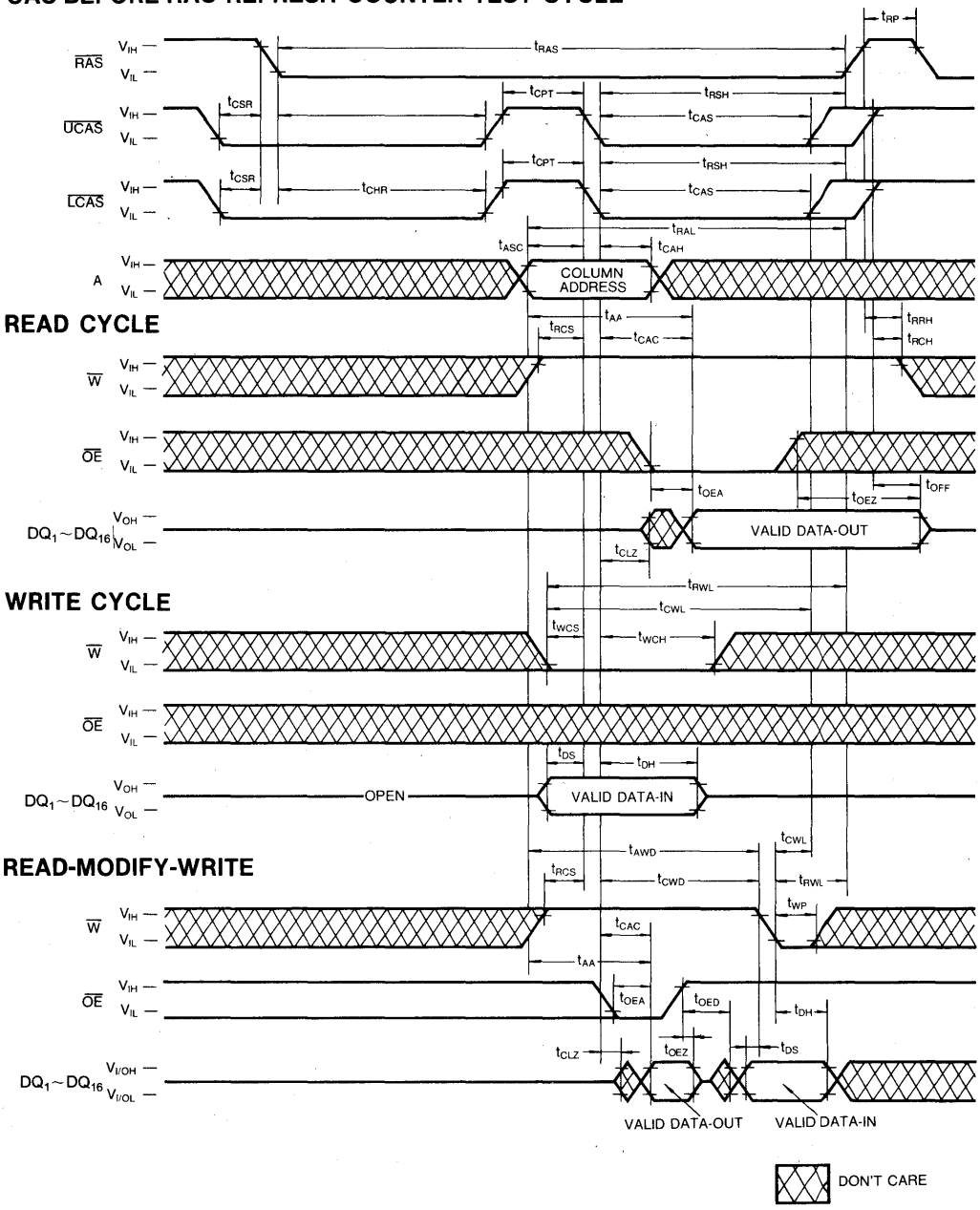


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

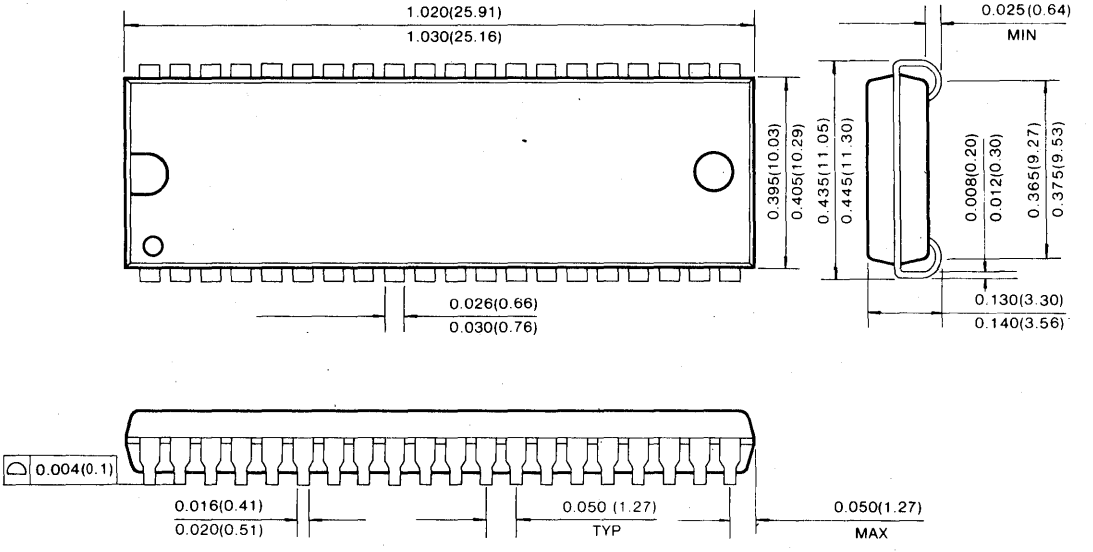
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



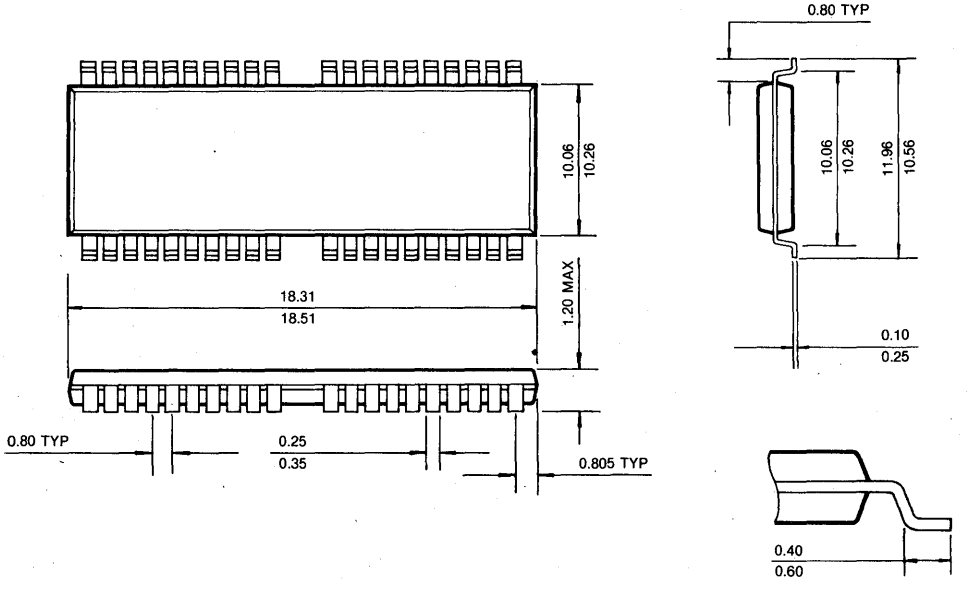
PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)



SAMSUNG ELECTRONICS

256K × 16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM416V254B/BL/BLL-6	60ns	17ns	110ns	24ns
KM416V254B/BL/BLL-7	70ns	20ns	130ns	29ns
KM416V254B/BL/BLL-8	80ns	20ns	150ns	34ns

- **Fast Page Mode with Extended Data out**
- **Byte word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Self Refresh operation (LL-version)**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple 3.3V±0.3V power supply**
- **Refresh Cycle**
  - **-512 cycle/8ms (Normal)**
  - **-512 cycle/64ms (L-version)**
  - **-512 cycle/128ms (LL-version)**
- **Power Dissipation**
  - **-Standby : 1.8mW(Normal)**
  - **0.36mW(L-version)**
  - **0.36mW(LL-version)**
  - **-Active (60/70/80): 255/235/220mW**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP II**

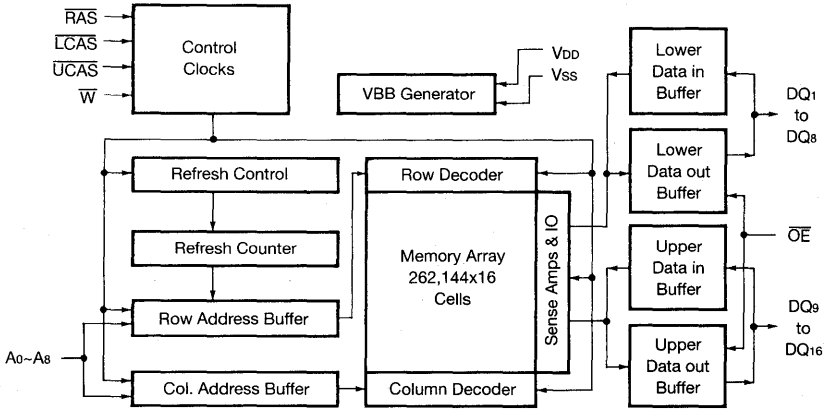
GENERAL DESCRIPTION

The Samsung KM416V254B/BL/BLL is a CMOS high speed 262,144 bit × 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM416V254B/BL/BLL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

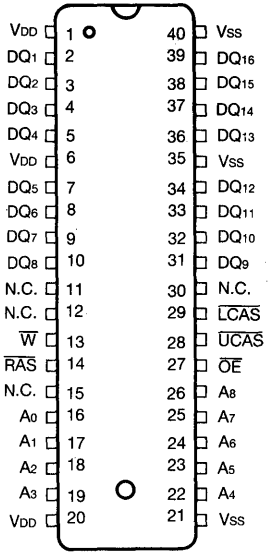
The KM416V254B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

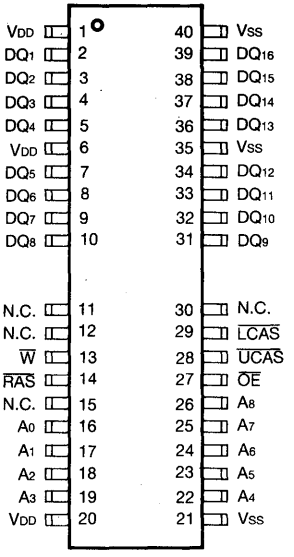


PIN CONFIGURATION (Top Views)

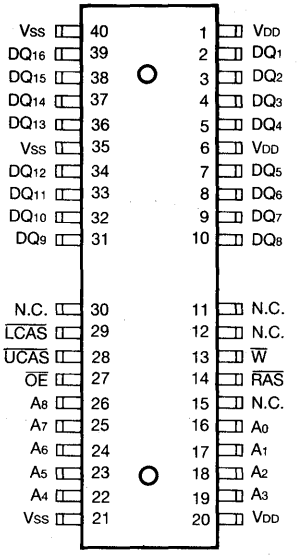
• KM416V254BJ/BLJ/BLLJ



• KM416V254BT/BLT/BLLT



• KM416V254BTR/BLTR/BLLTR



Pin Name	Pin Function
A0-A8	Address Inputs
DQ1~16	Data In/Out
VSS	Ground
RAS	Row Address Strobe
UCAS	Upeer Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VDD	Power(+3.3V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5~4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5~4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.1	—	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$=$\overline{LCAS}$, Address Cycling @t_{RC}=min.)	KM416V254B/BL/BLL-6 KM416V254B/BL/BLL-7 KM416V254B/BL/BLL-8	I_{CC1}	-	70 65 60	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM416V254B/BL/BLL-6 KM416V254B/BL/BLL-7 KM416V254B/BL/BLL-8	I_{CC3}	-	70 65 60	mA mA mA
Hyper page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$=$\overline{LCAS}$, Address Cycling @t_{PC}=min.)	KM416V254B/BL/BLL-6 KM416V254B/BL/BLL-7 KM416V254B/BL/BLL-8	I_{CC4}	-	60 55 50	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{DD}-0.2V)	KM416V254B KM416V254BL KM416V254BLL	I_{CC5}	-	500 100 100	μA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{UCAS}$=$\overline{LCAS}$ Cycling @t_{RC}=min.)	KM416V254B/BL/BLL-6 KM416V254B/BL/BLL-7 KM416V254B/BL/BLL-8	I_{CC6}	-	70 65 60	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{DD}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{UCAS}$=$\overline{LCAS}$=0.2V D_{IN}=Don't Care, T_{RC}=125μS T_{RAS}=T_{RAS} min.~300ns	KM416V254BL	I_{CC7}	-	200	μA
Self Refresh Current $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_8=V_{DD}-0.2V or 0.2V DQ_1-DQ_{16}=V_{DD}-0.2V, 0.2V or Open	KM416V254BLL	I_{CC8}	-	100	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_8)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		17		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Turn-off delay from $\overline{CAS}$	t_{CEZ}	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	17		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	15	10,000	20	10,000	ns	12
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time referenced to $\overline{RAS}$	tAR	50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		20		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	15		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	tDHR	50		55		60		ns	6
Refresh Period (Normal)	tREF		8		8		8	ms	
Refresh Period (L-ver)	tREF		64		64		64	ms	
Refresh Period (LL-ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	42		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Hyper Page mode cycle time	tHPC	24		29		34		ns	12
Hyper Page mode read-modity-write cycle time	tHPRWC	76		81		91		ns	12
$\overline{CAS}$ precharge time (Hyper Page mode)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page mode)	tRASP	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	7
$\overline{OE}$ commend hold time	tOEH	15		20		20		ns	
$\overline{OE}$ to Output in Low-Z	tOLZ	3		3		3		ns	3
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	20	3	20	ns	7,14

AC CHARACTERISTICS (Continued)

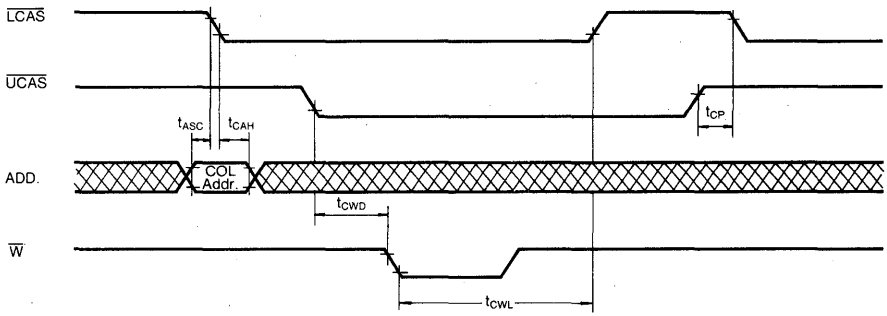
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Output buffer turn off delay from $\overline{W}$	tWEZ	3	15	3	20	3	20	ns	7
$\overline{W}$ to data delay	tWED	15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh	tRASS	100		100		100		μs	13
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	13
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	13

KM416V254B/BL/BLL Truth Table

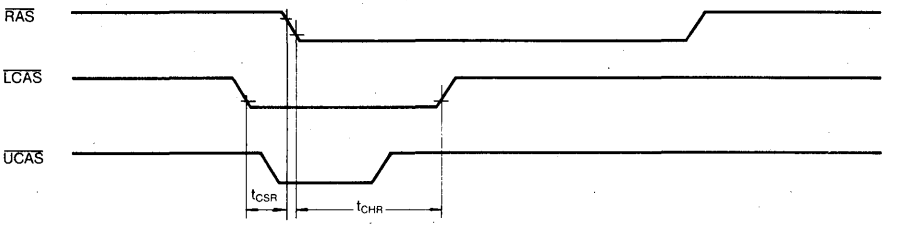
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

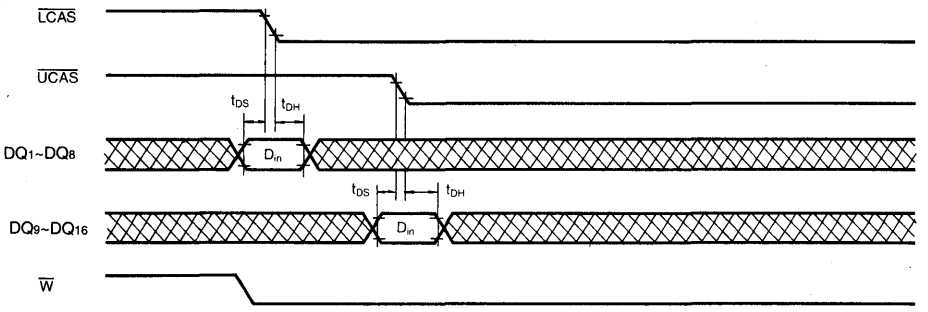
1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs except t_{HPC} and t_{HPRWC}.
3. Measured with a load equivalent to 1 TTL loads and 100pF, V_{oh}=2.0V and V_{ol}=0.8V
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. $t_{ASC} \geq t_{CP}$ min, Assume tT=2.0 ns
13. 512 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (LL-Ver)
14. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
16. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
17. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
18. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



19. t_{CSR} is refernced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
20. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low



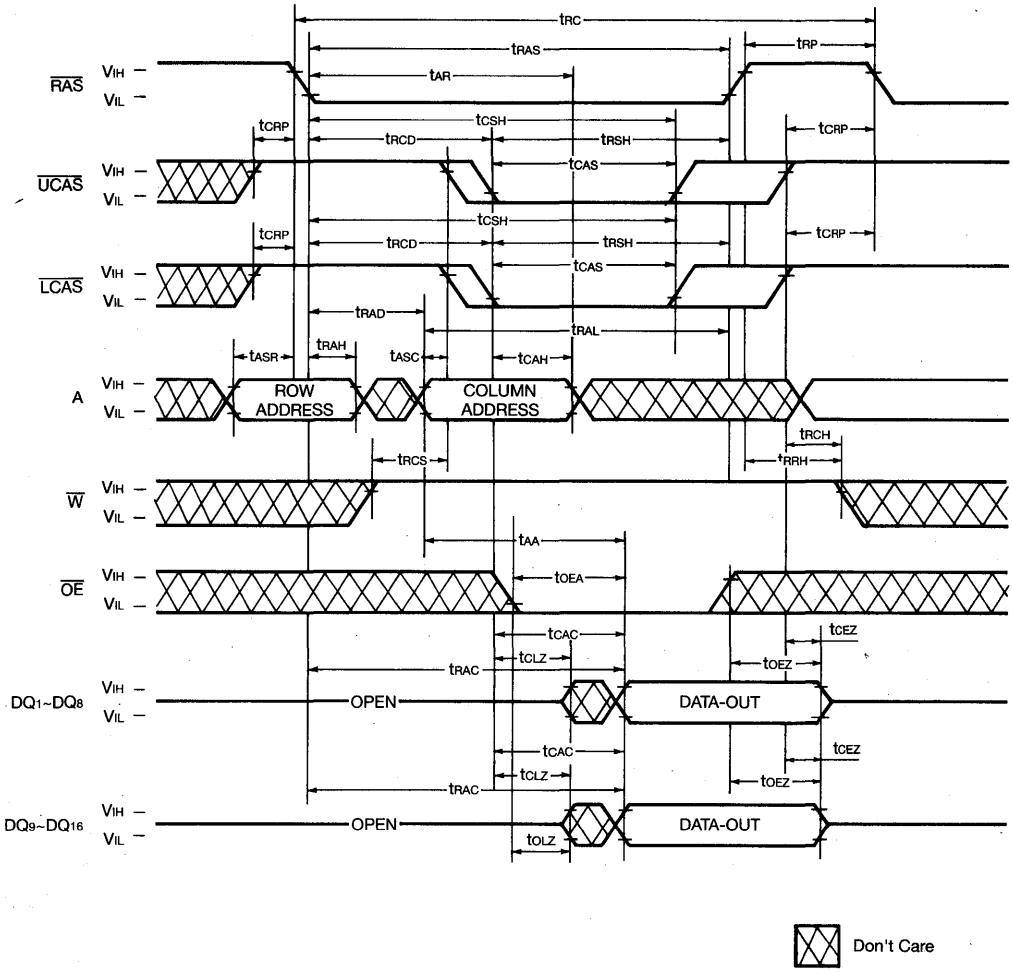
21. t_{DS}, t_{DH}, is independently specified for lower byte $D_{IN(1-8)}$, upper byte $D_{in(9\sim16)}$.



TIMING DIAGRAM

WORD READ CYCLE

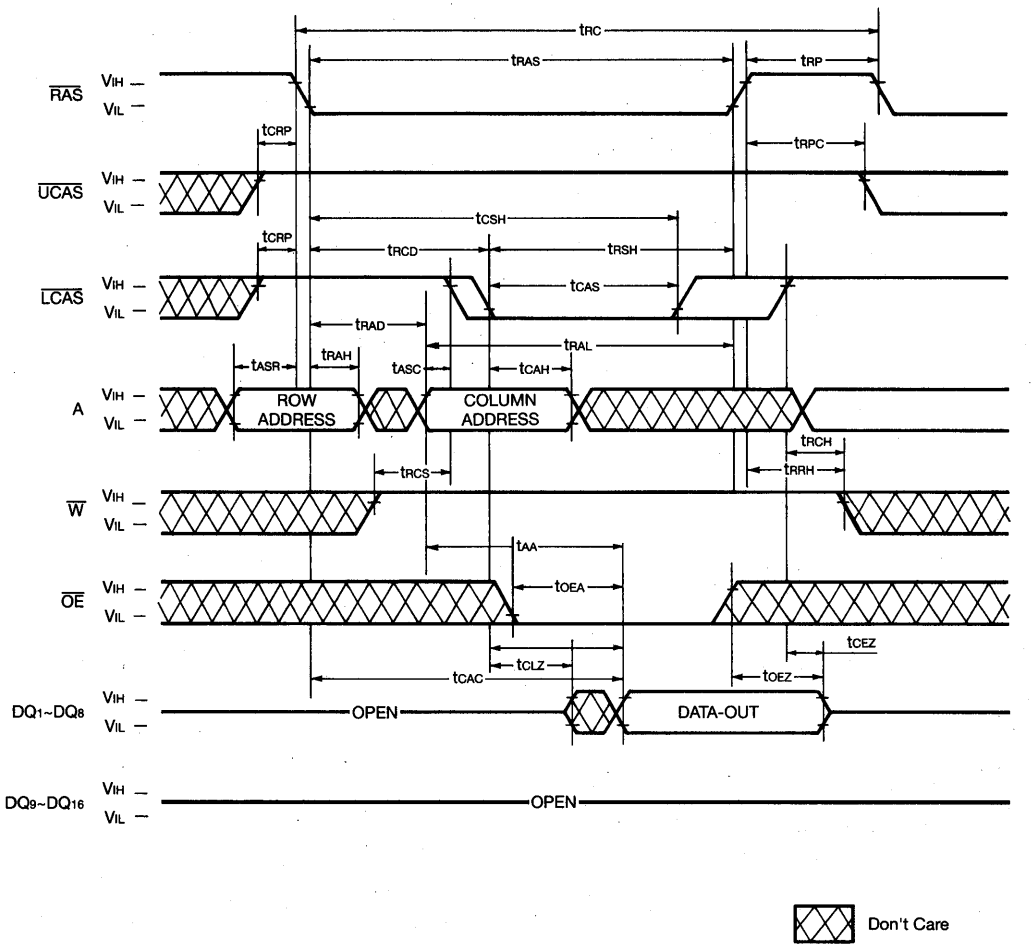
NOTE : DIN=OPEN



TIMING DIAGRAM

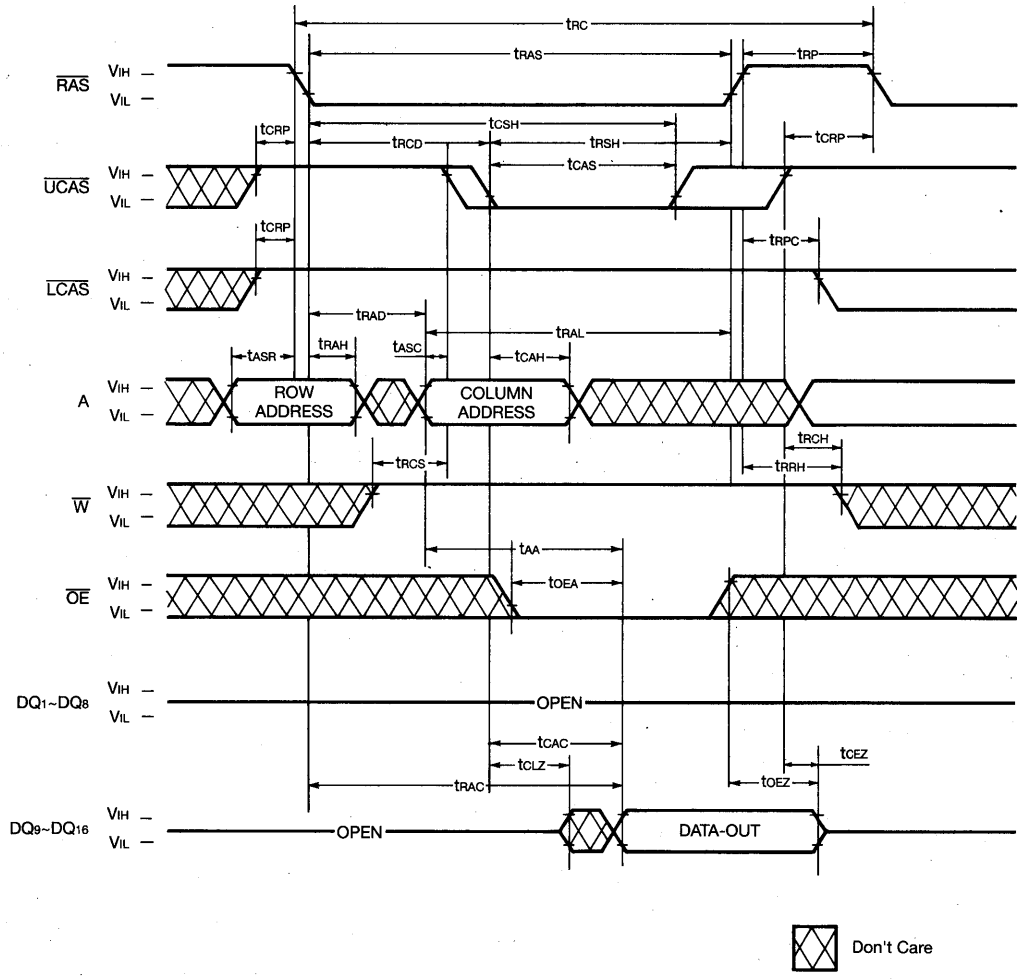
LOWER BYTE READ CYCLE

NOTE : DIN=OPEN



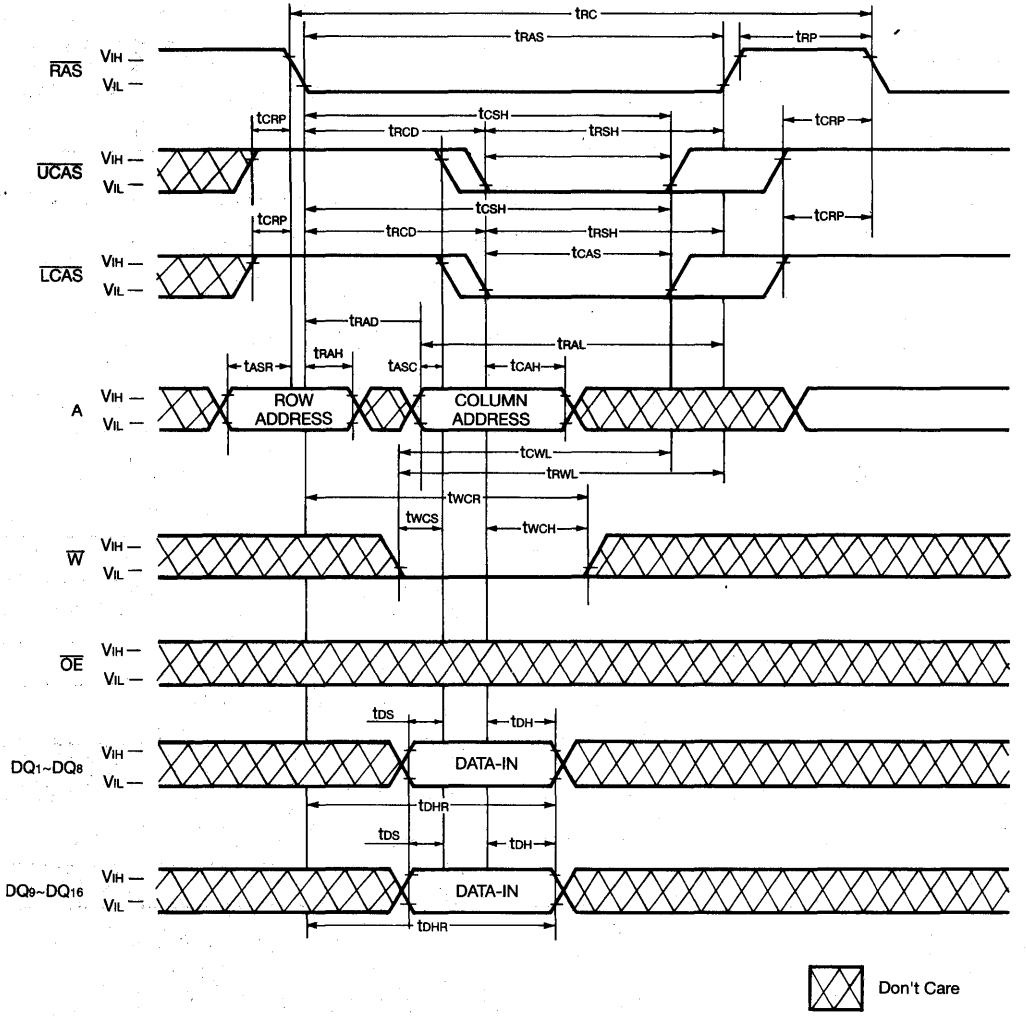
UPPER BYTE READ CYCLE

NOTE : DIN=OPEN



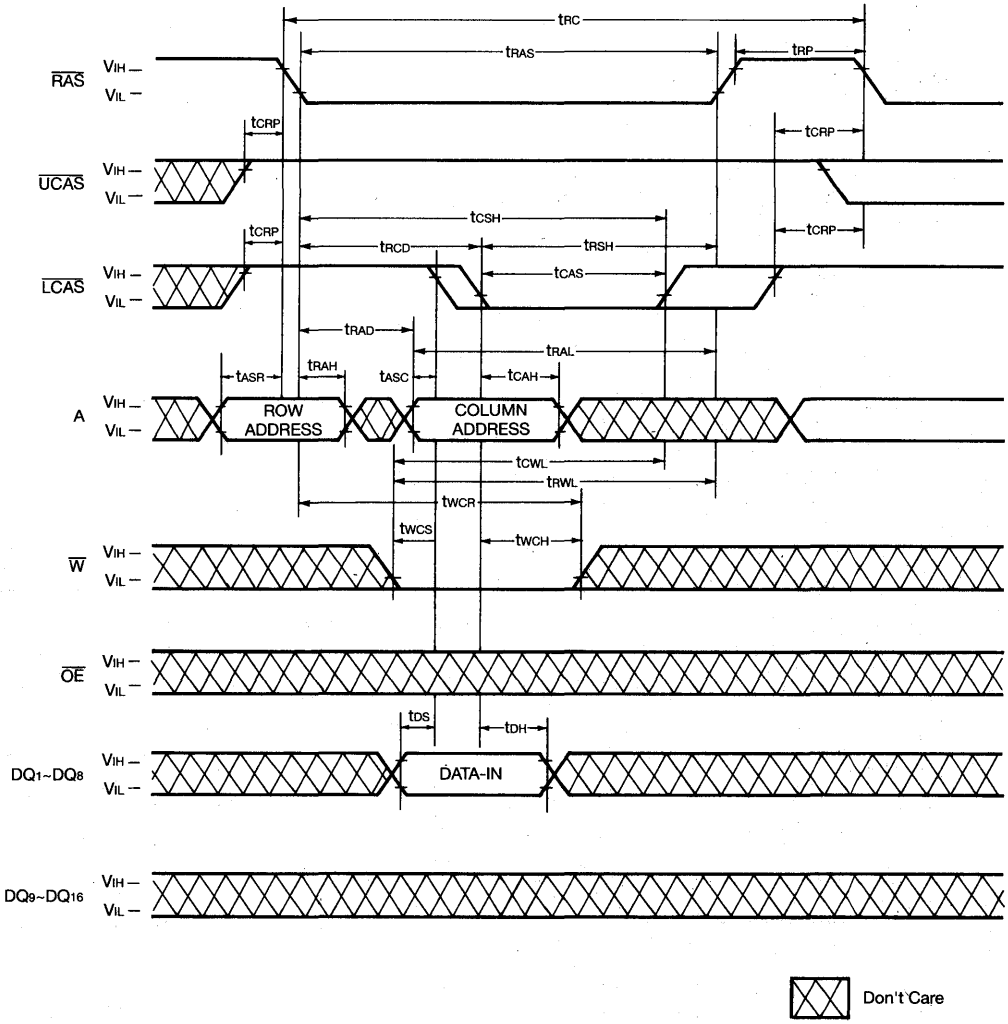
WORD WRITE CYCLE (EARLY WRITE)

NOTE : DOUT=OPEN



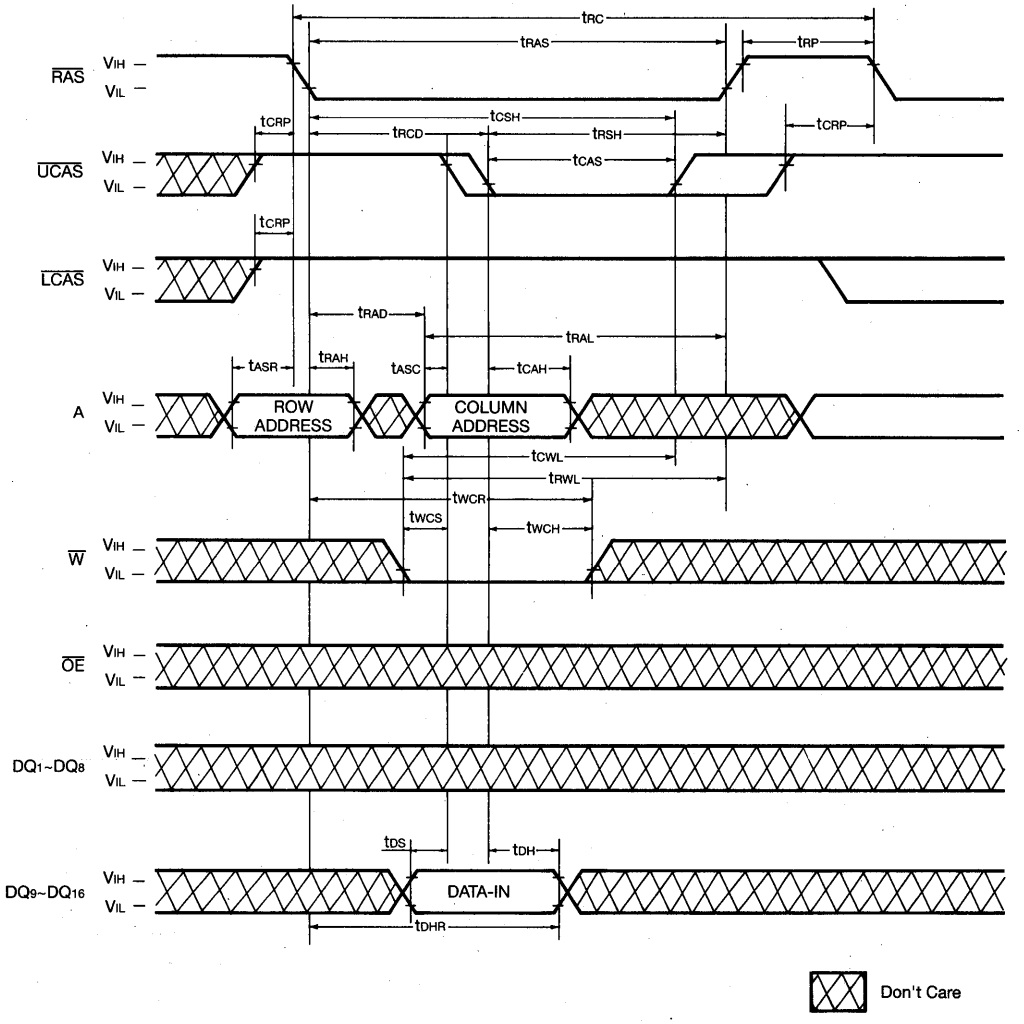
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT=OPEN



UPPER BYTE WRITE CYCLE (EARLY WRITE)

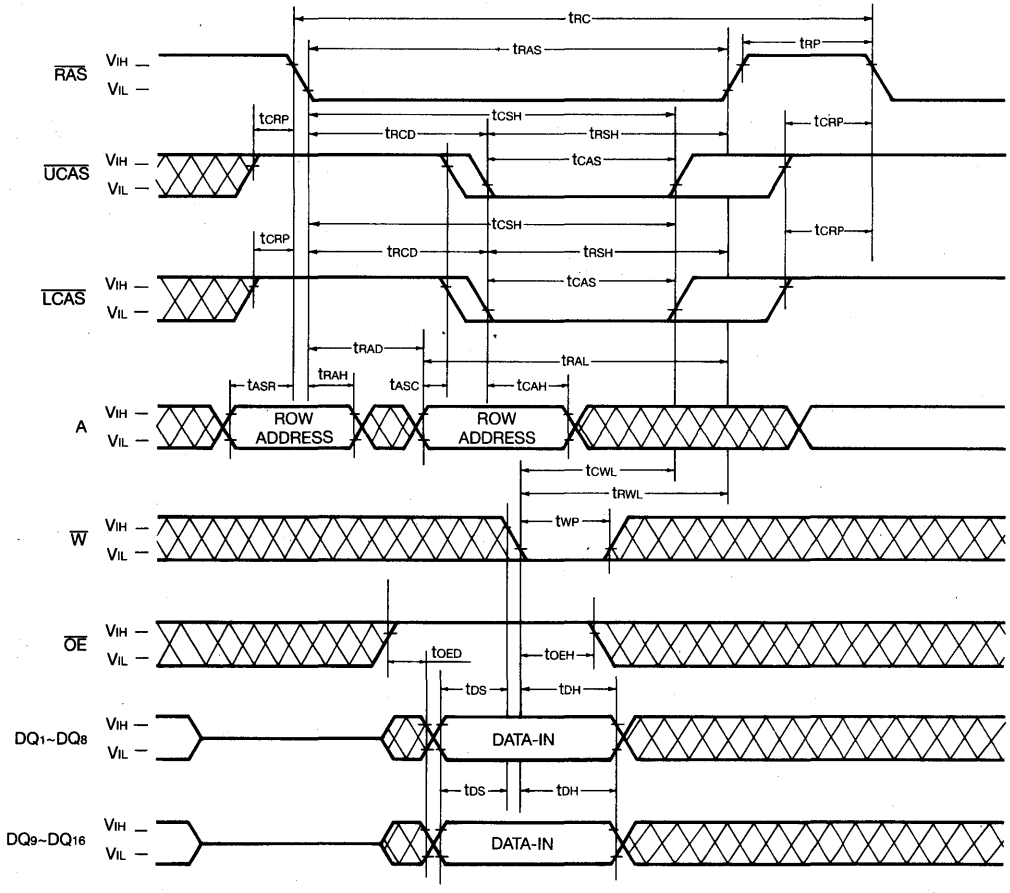
NOTE : DOUT=OPEN



SAMSUNG ELECTRONICS

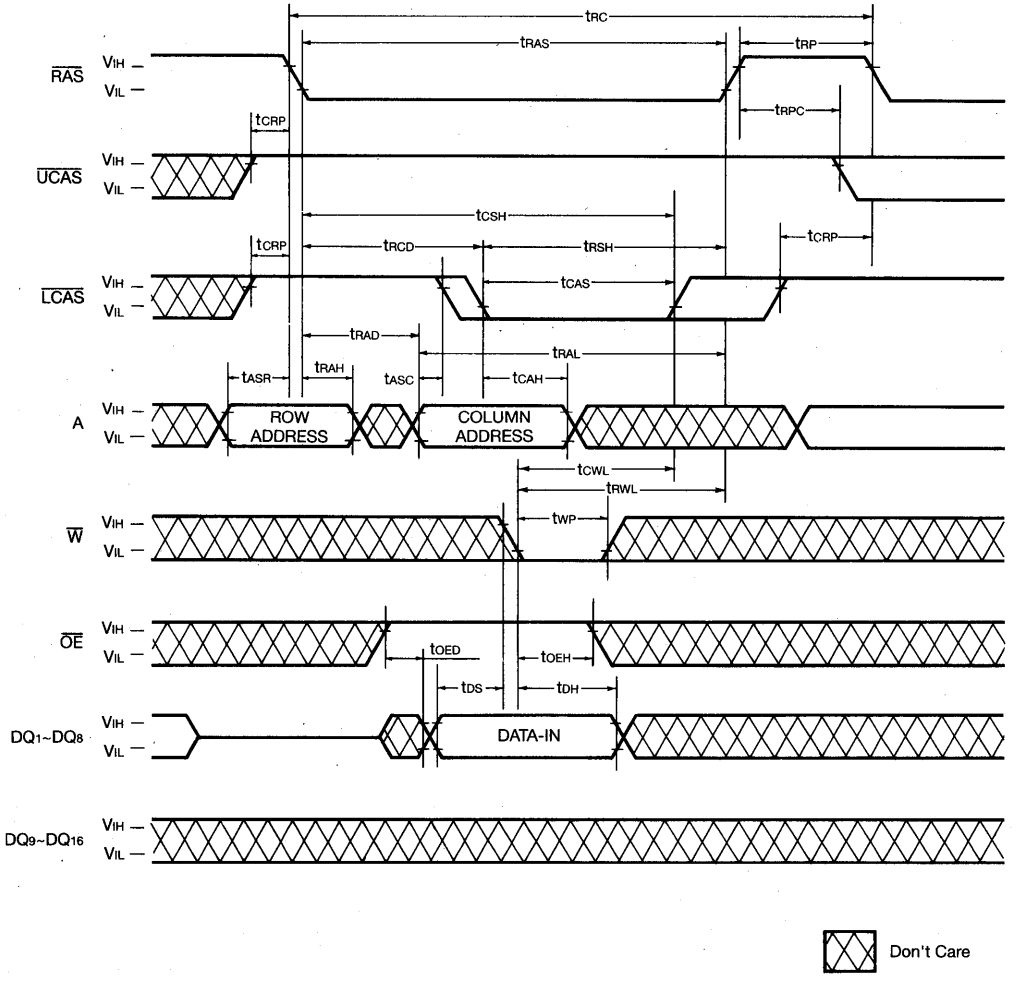
WORD WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : DOUT=OPEN



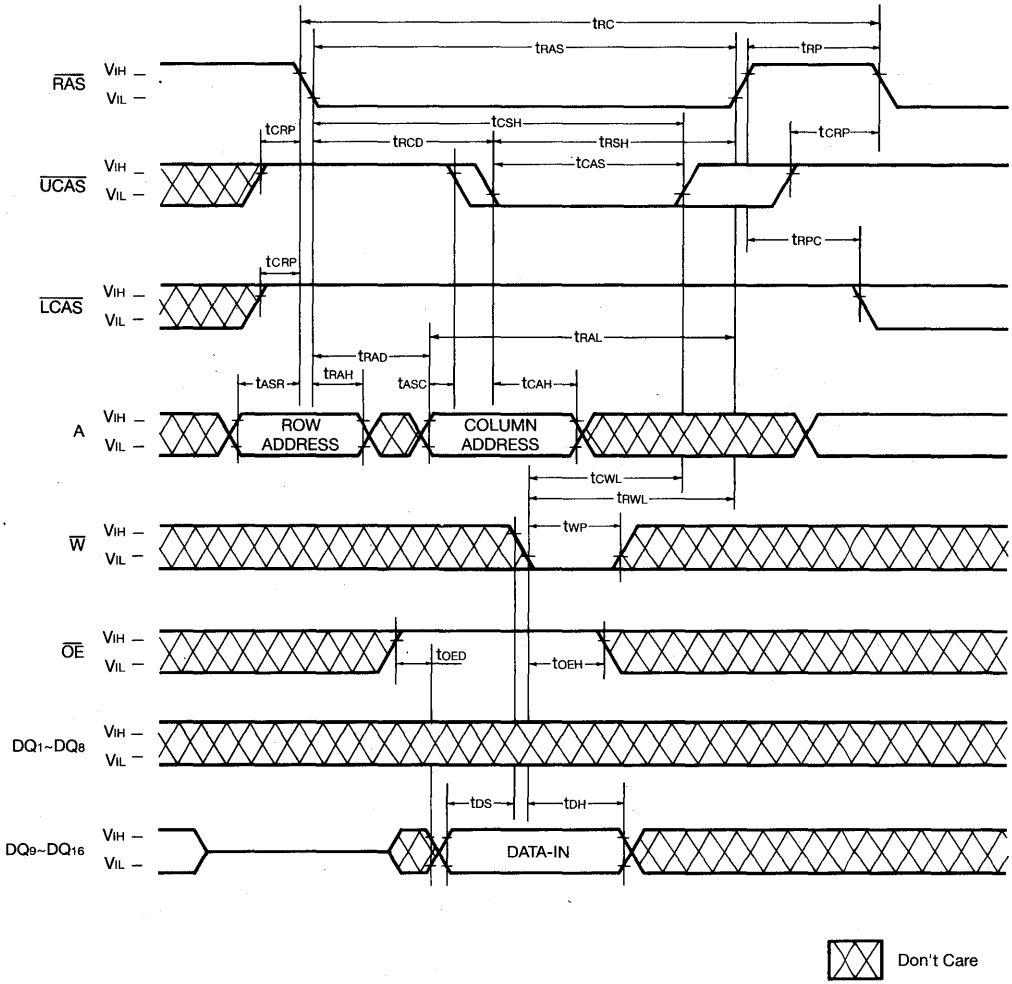
LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : DOUT=OPEN



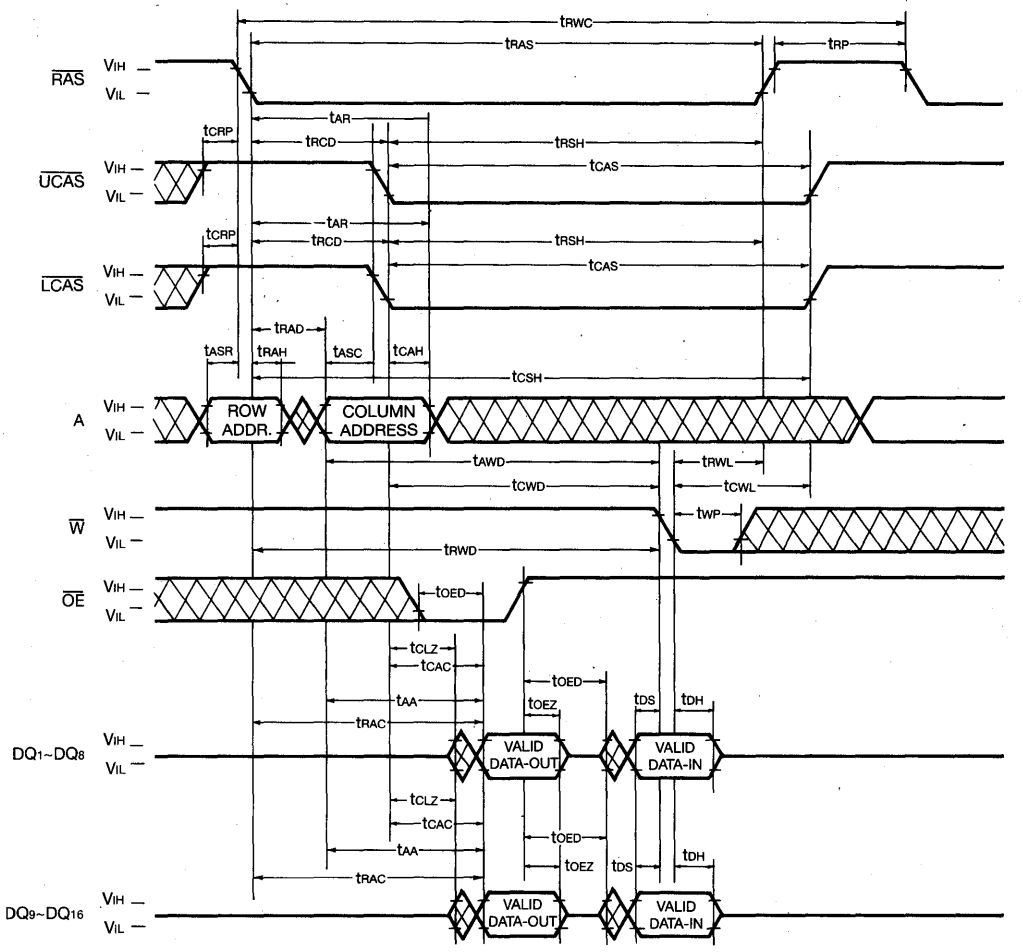
UPPER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : DOUT=OPEN

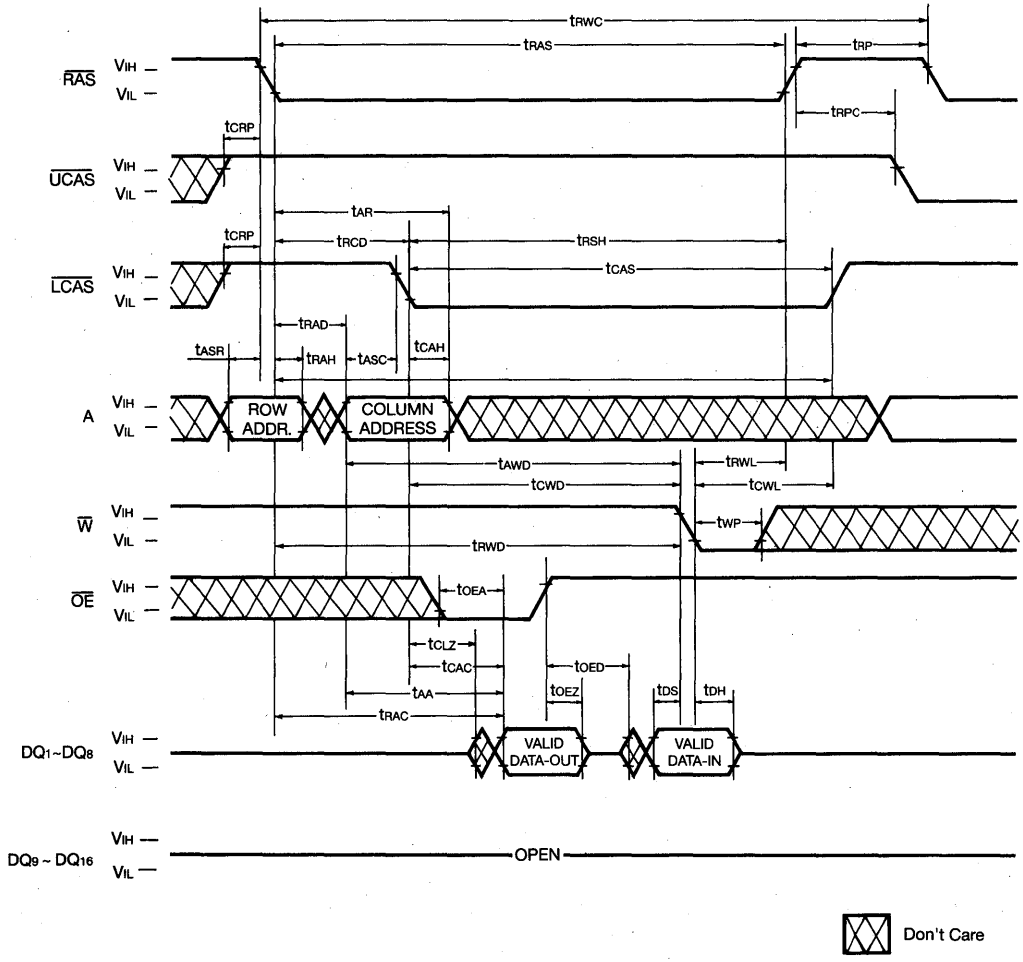


SAMSUNG ELECTRONICS

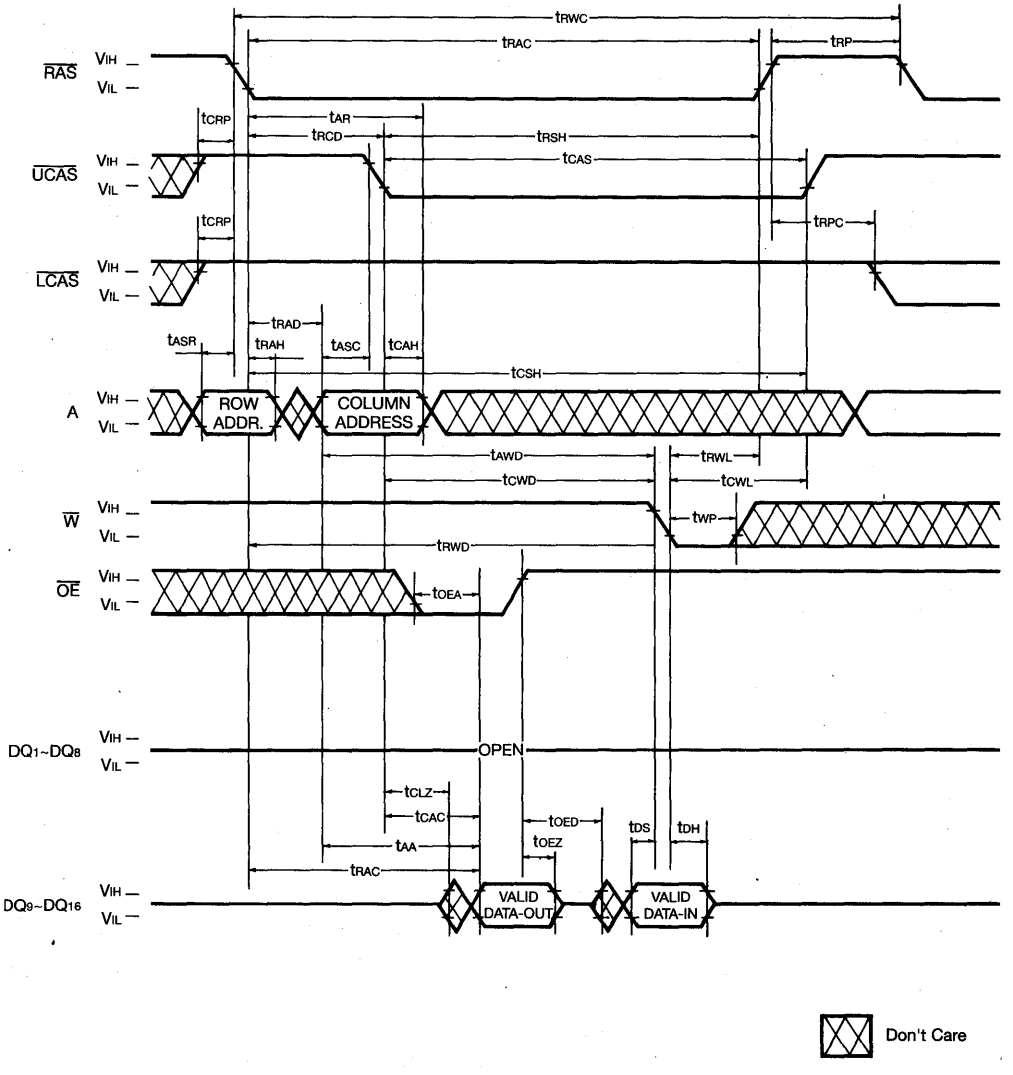
WORD READ-MODIFY-WRITE CYCLE



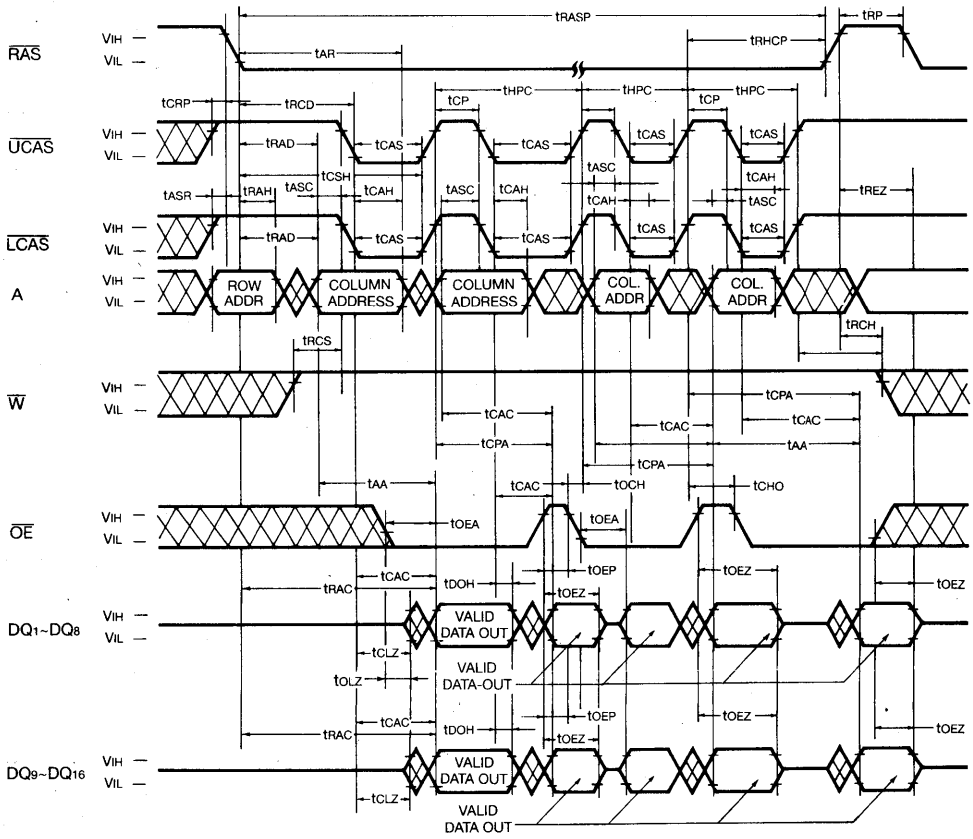
LOWER-BYTE READ-MODIFY-WRITE CYCLE



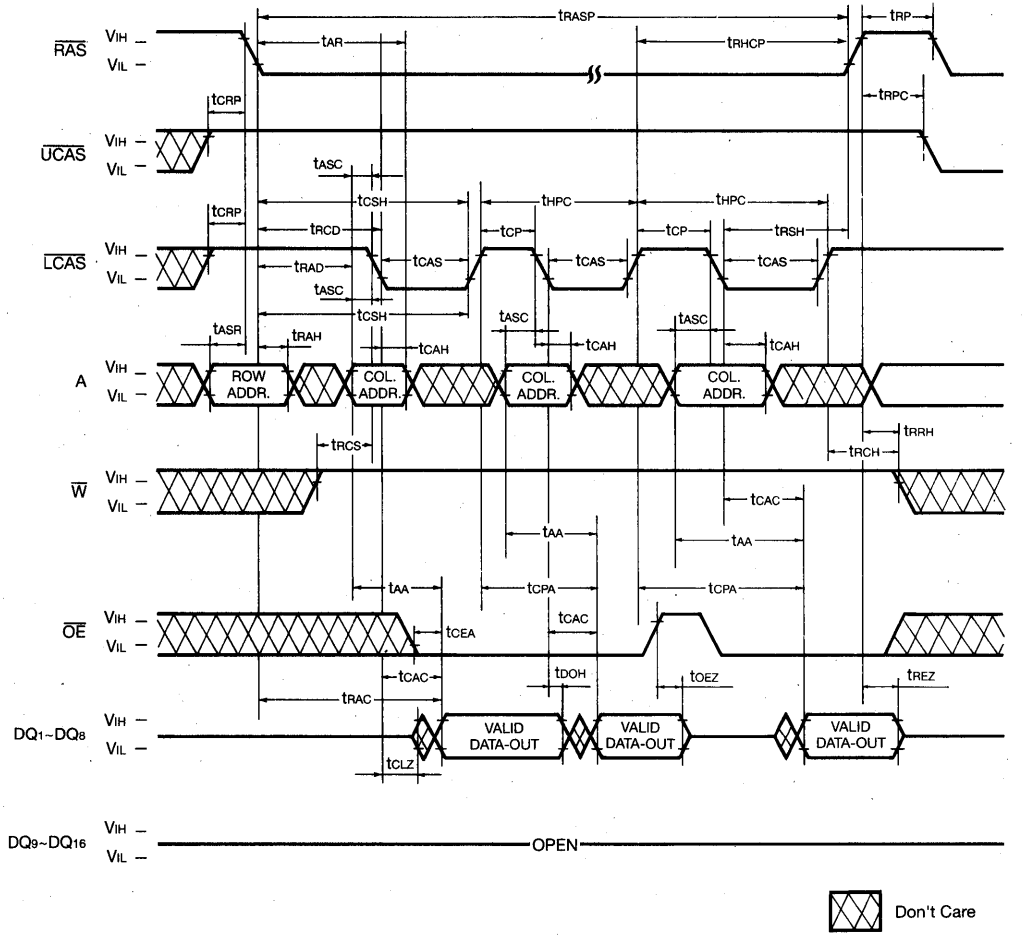
UPPER-BYTE READ-MODIFY-WRITE CYCLE



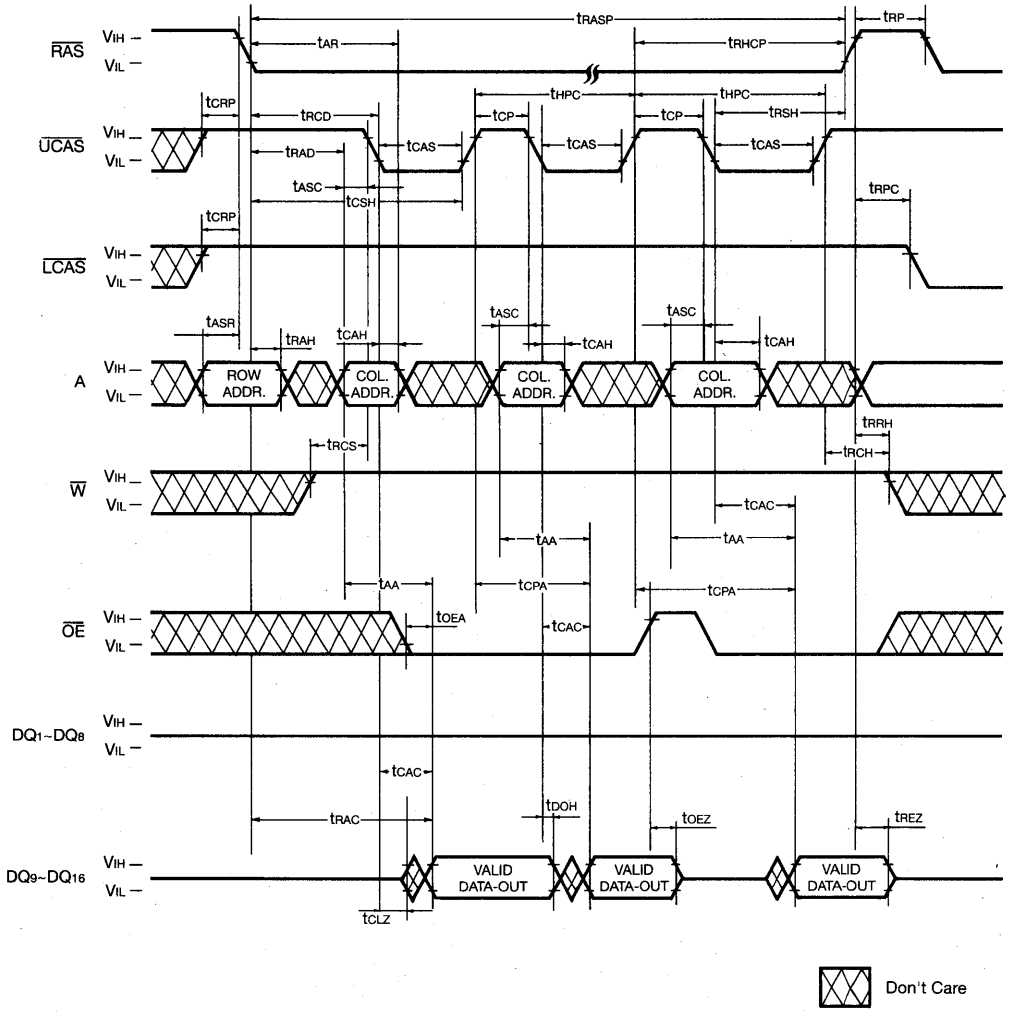
HYPER PAGE MODE WORD READ CYCLE



HYPER PAGE MODE LOWER BYTE READ CYCLE

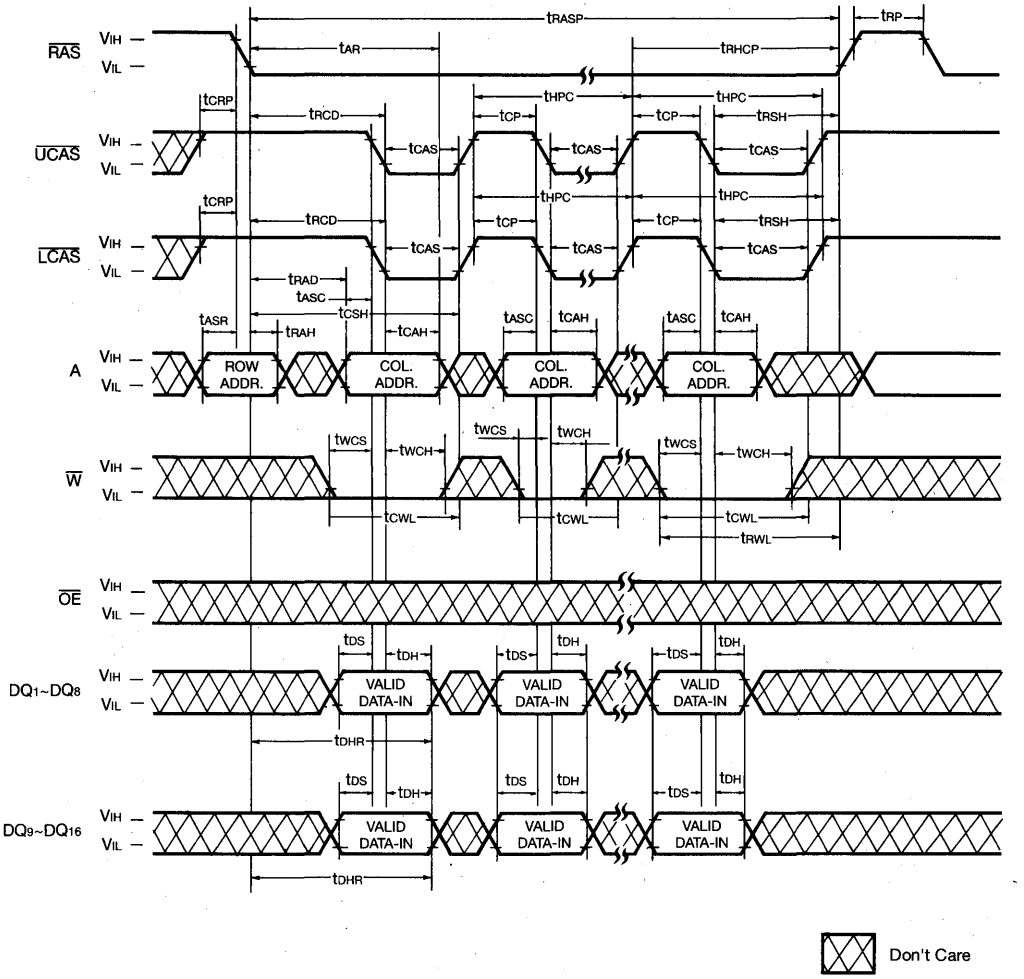


HYPER PAGE MODE UPPER BYTE READ CYCLE



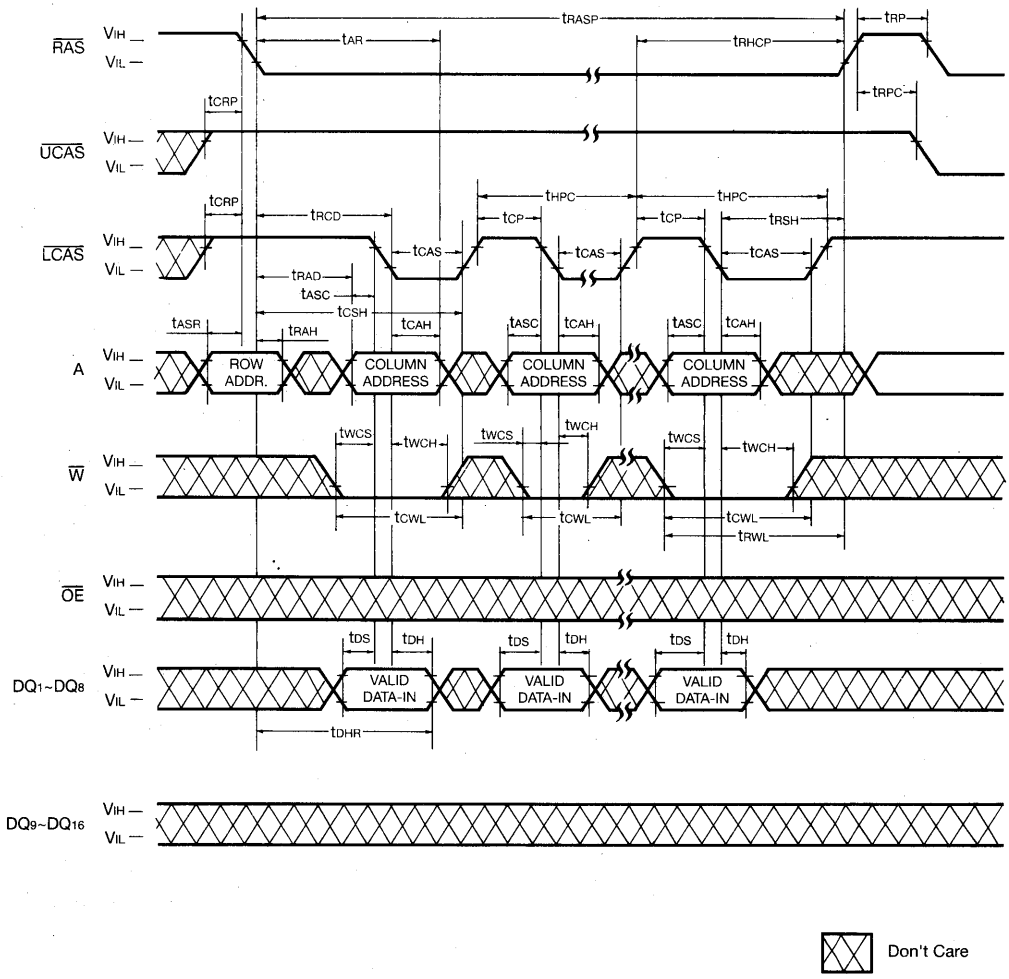
HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : DOUT=OPEN



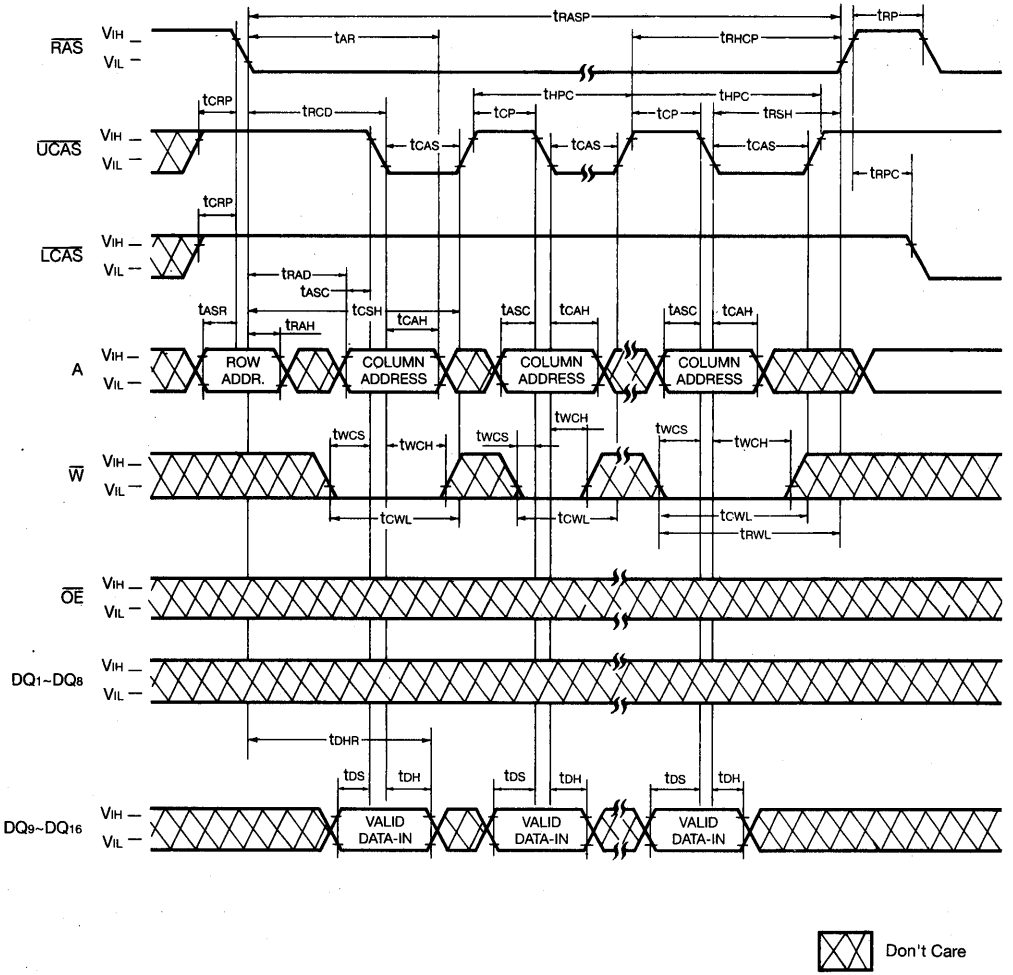
HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT=OPEN

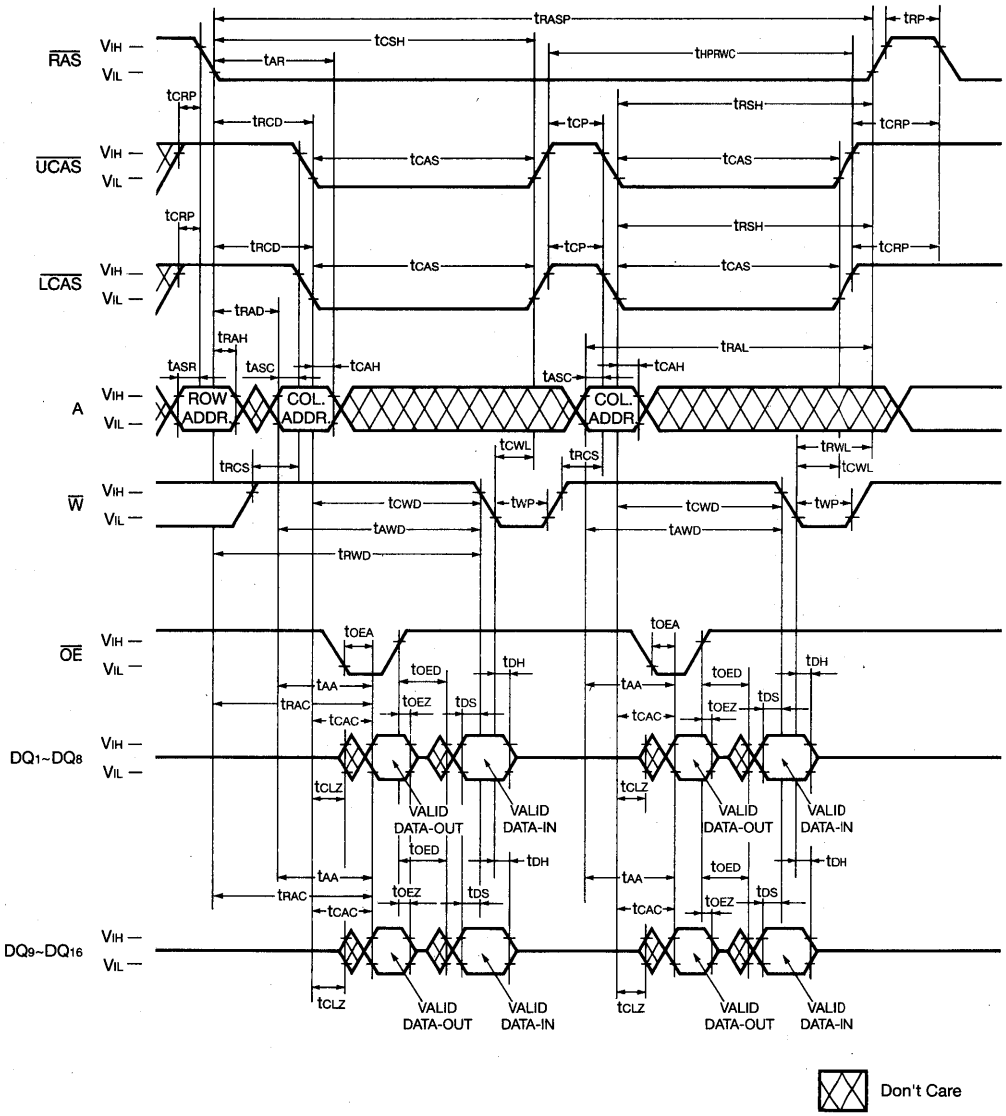


HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

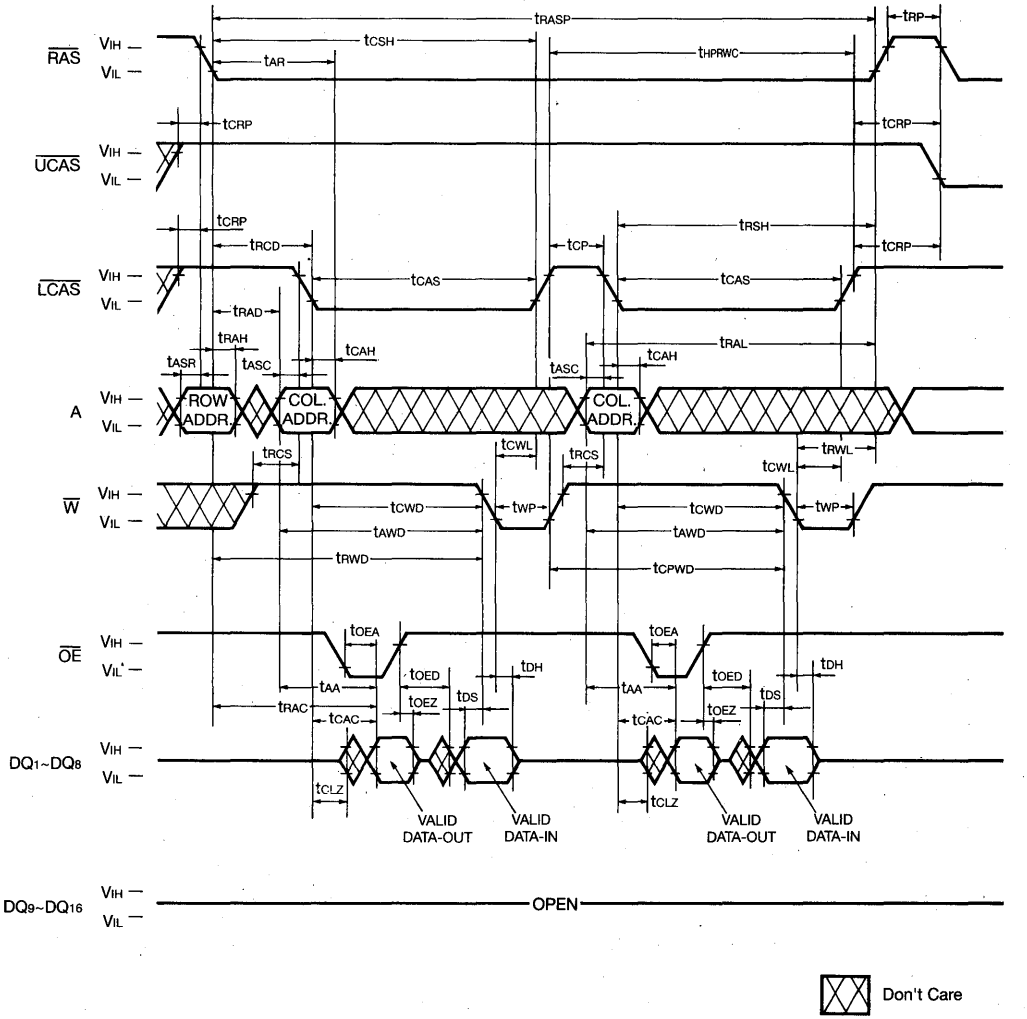
NOTE : DOUT=OPEN



HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE

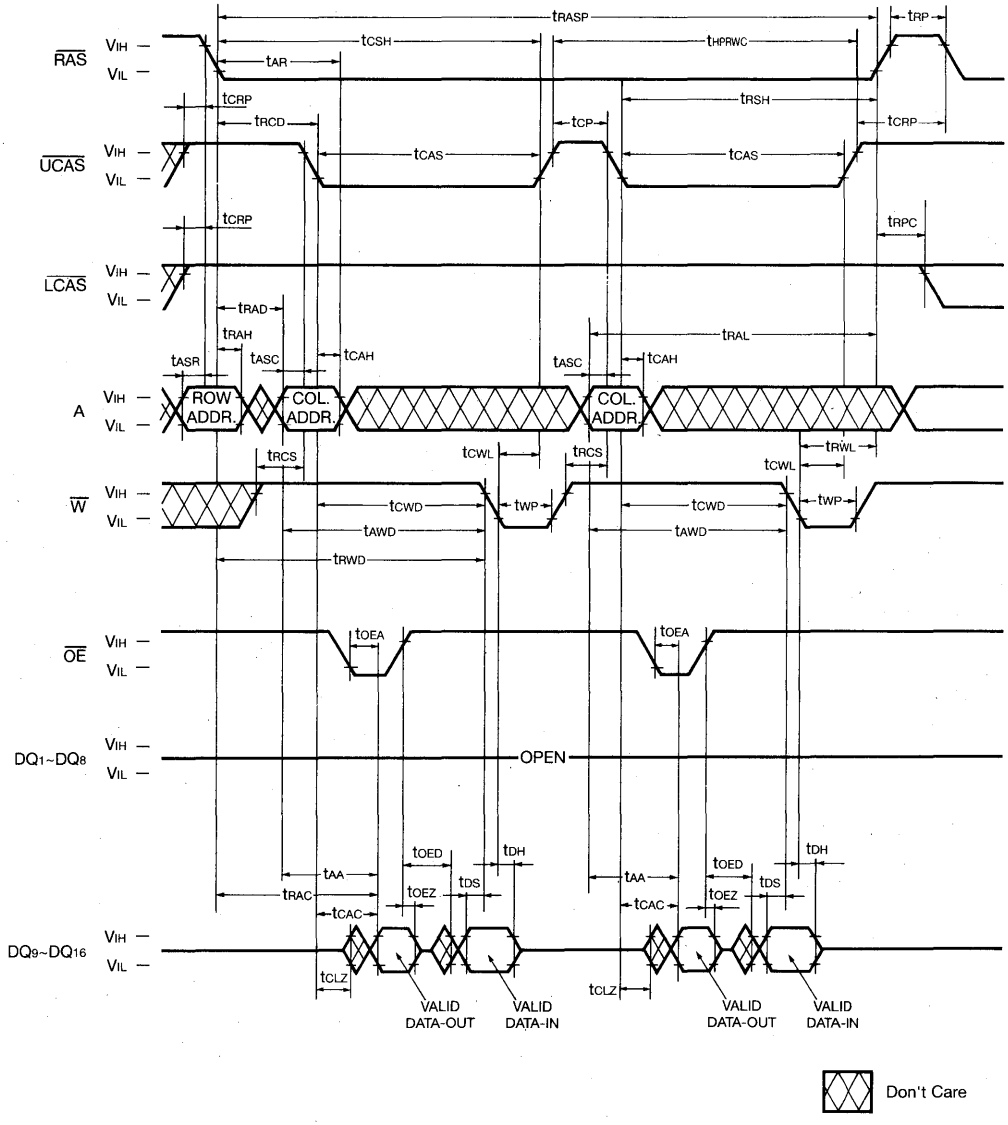


HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



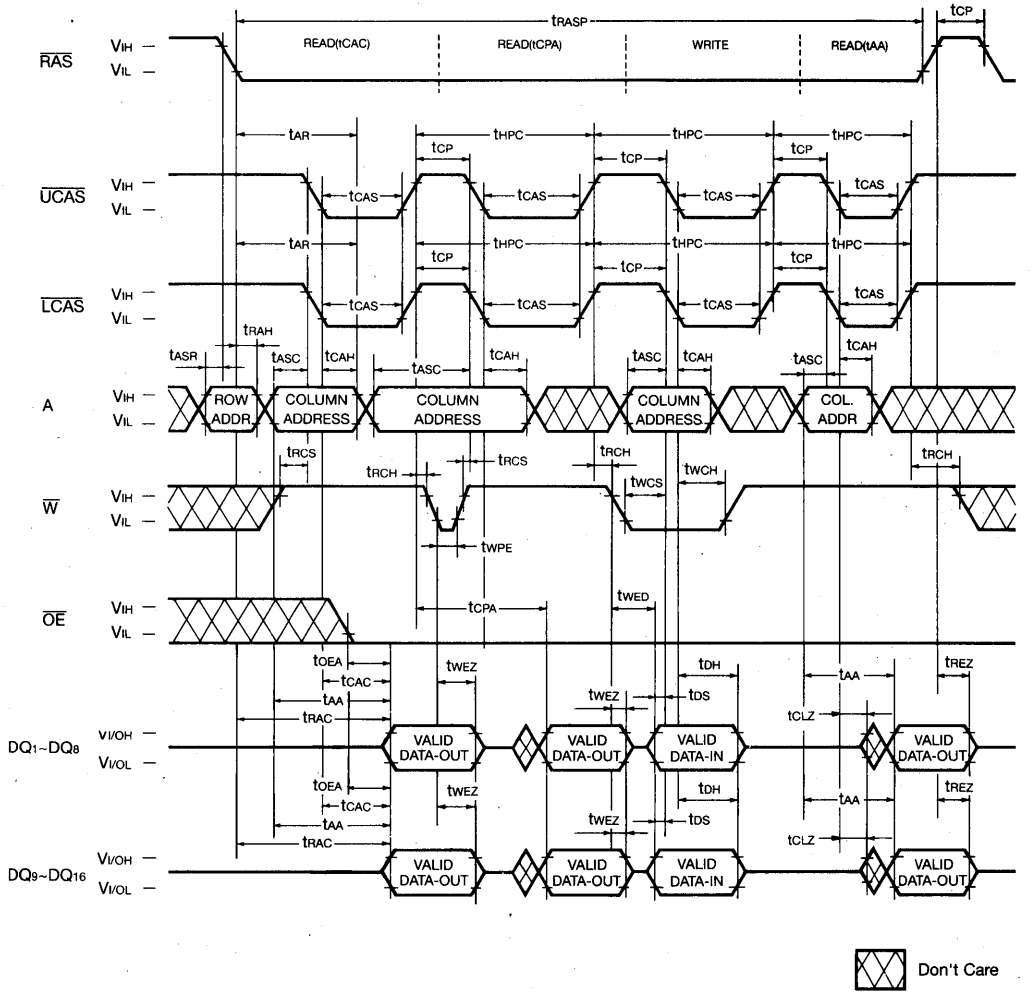
SAMSUNG ELECTRONICS

HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



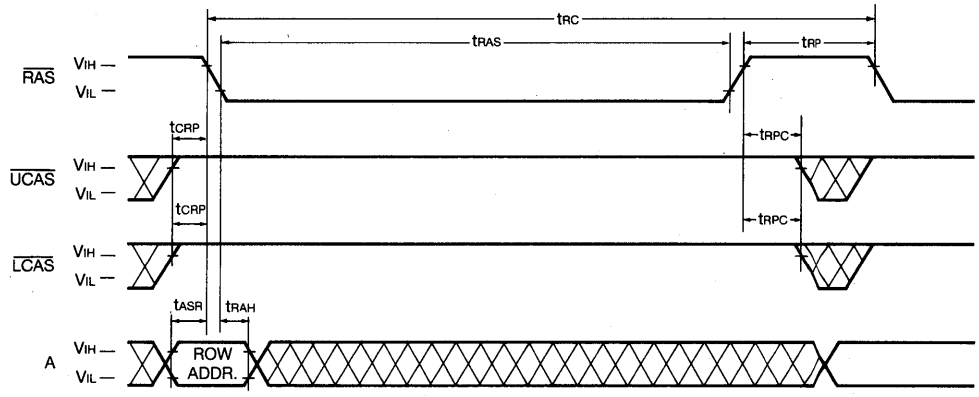
SAMSUNG ELECTRONICS

HYPER PAGE READ AND WRITE MIXED CYCLE



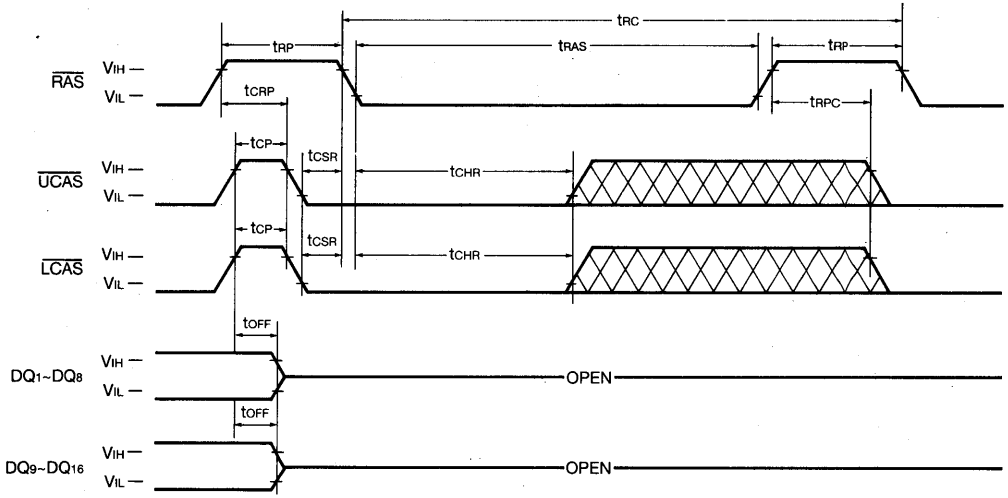
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN}=Don't Care
D_{OUT}=OPEN



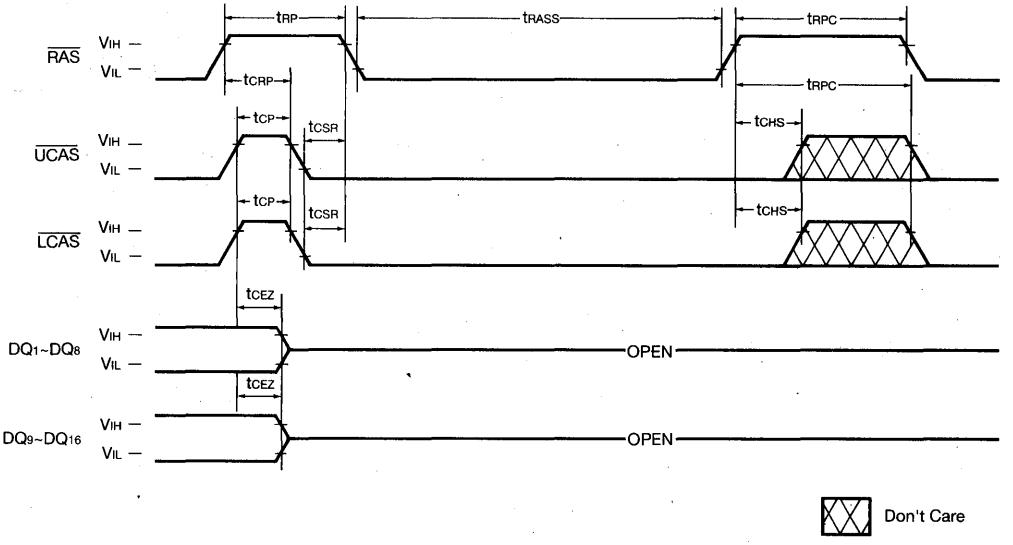
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A=Don't Care

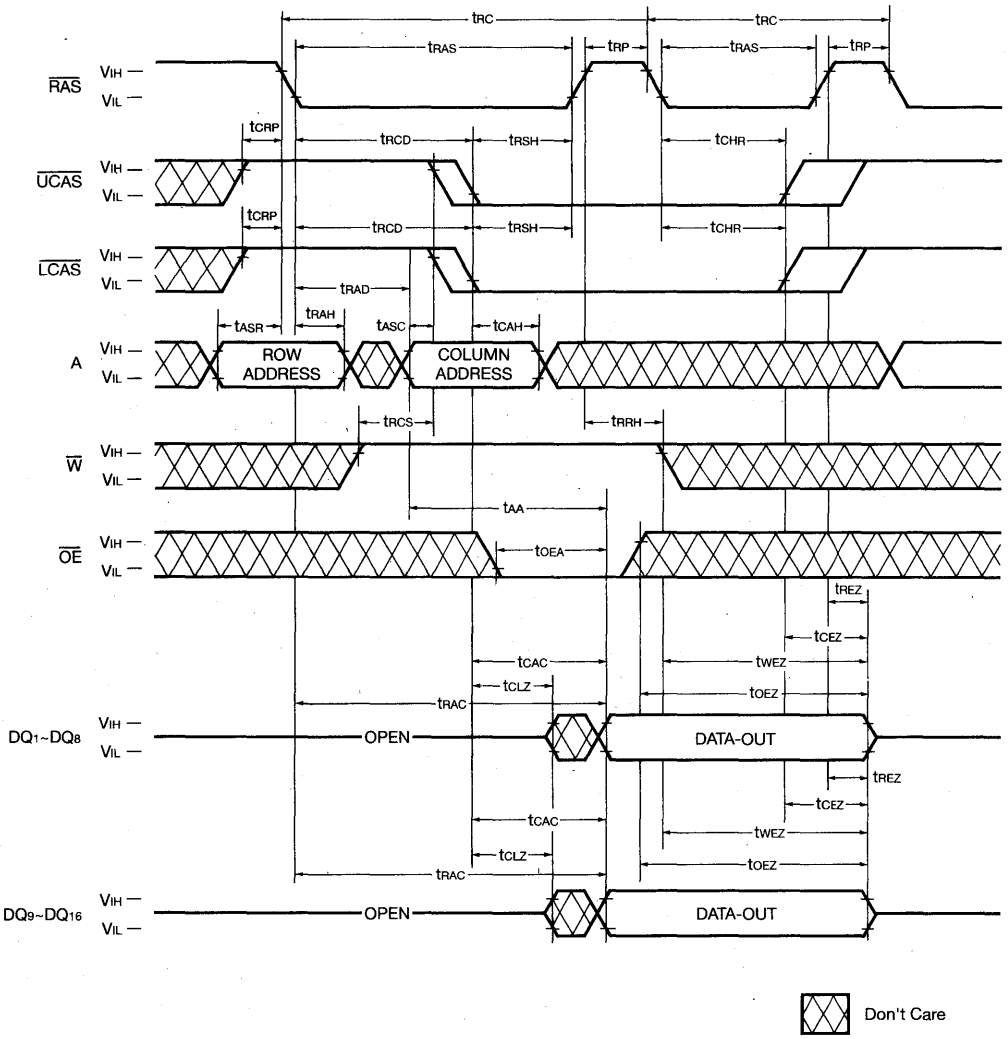


$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-Version)

NOTE : $\overline{W}$, $\overline{OE}$, A=Don't Care

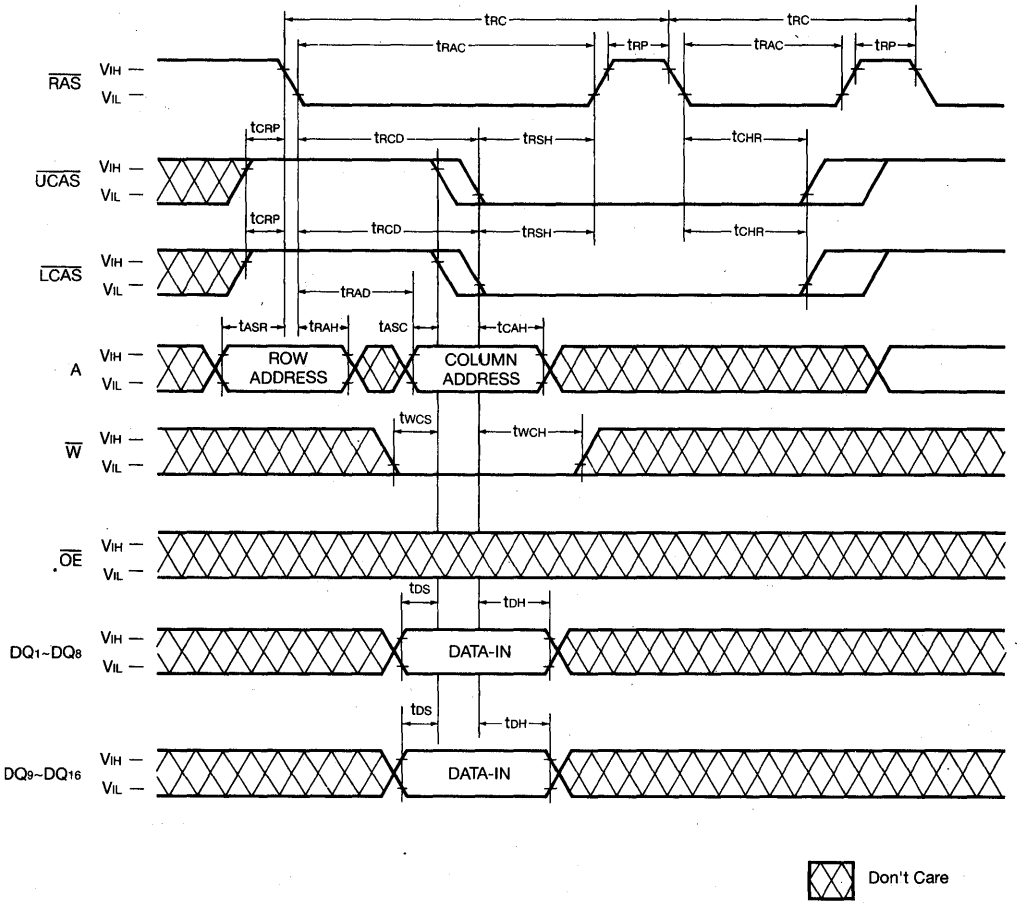


HIDDEN REFRESH CYCLE (READ)

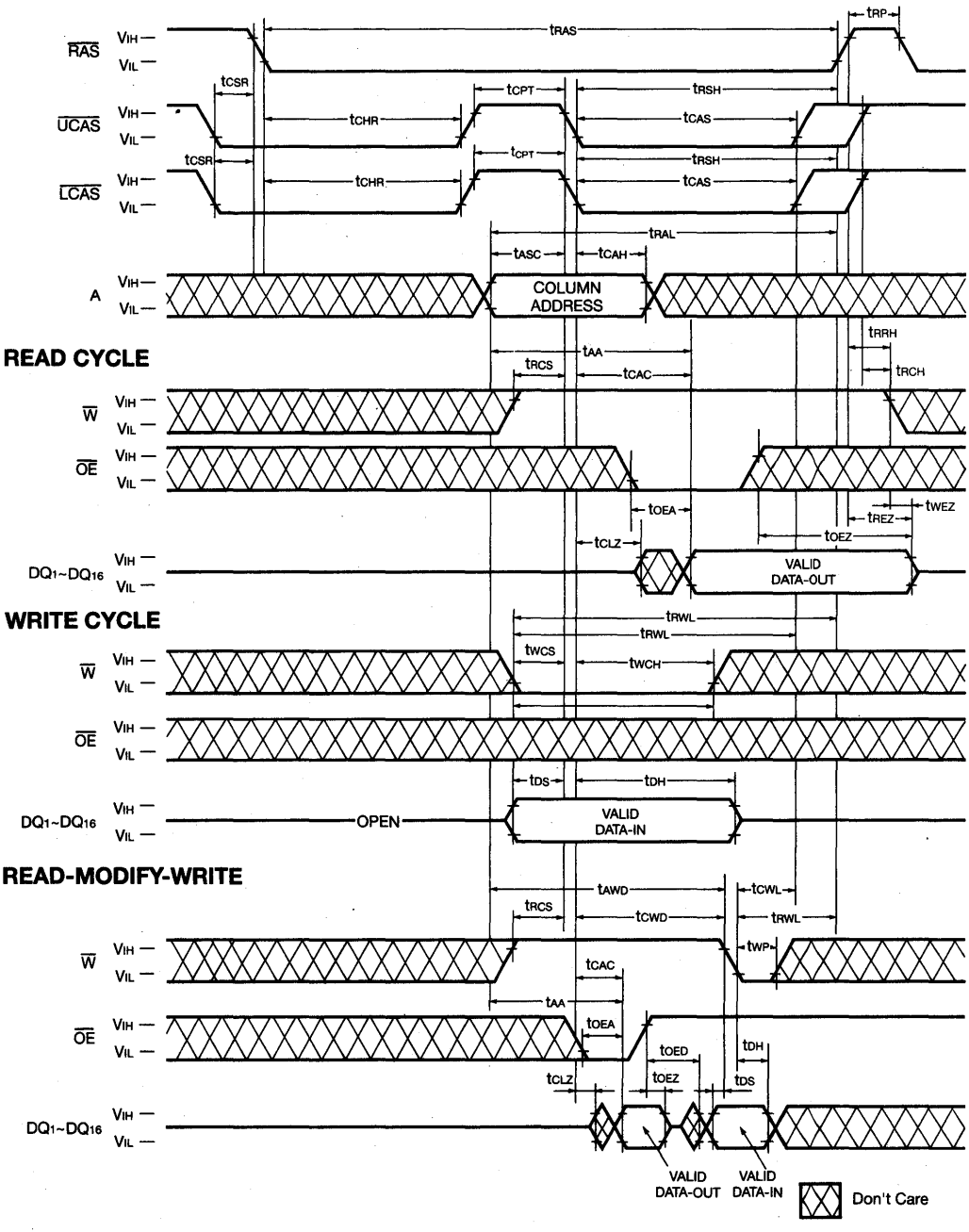


HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT=OPEN



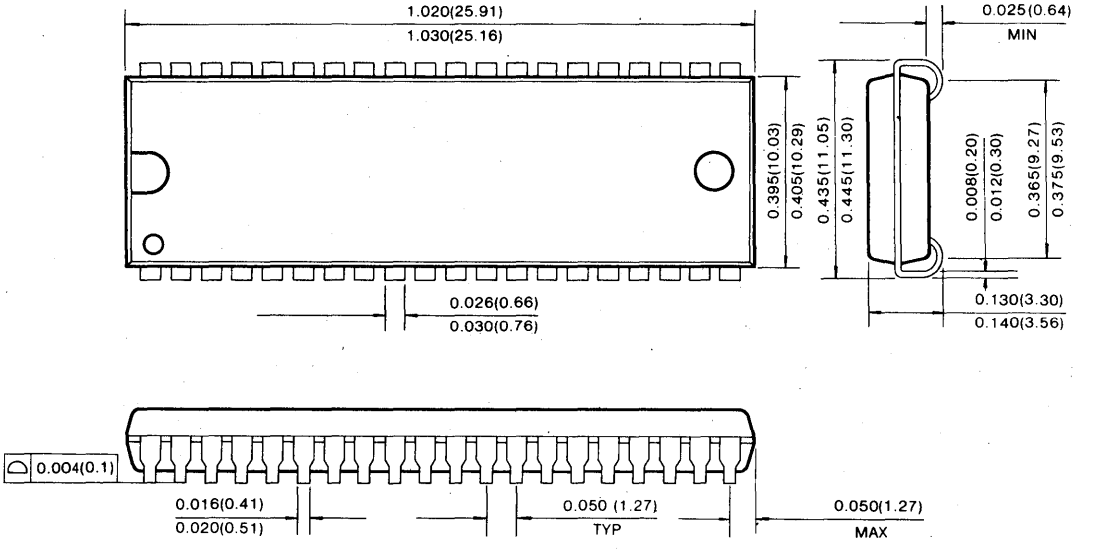
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



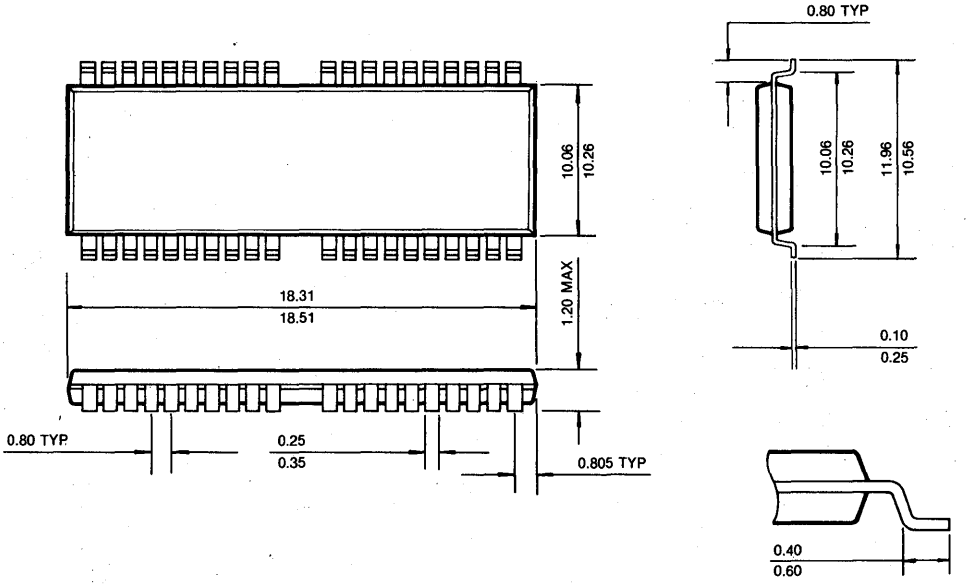
PACKAGE DIMENSION

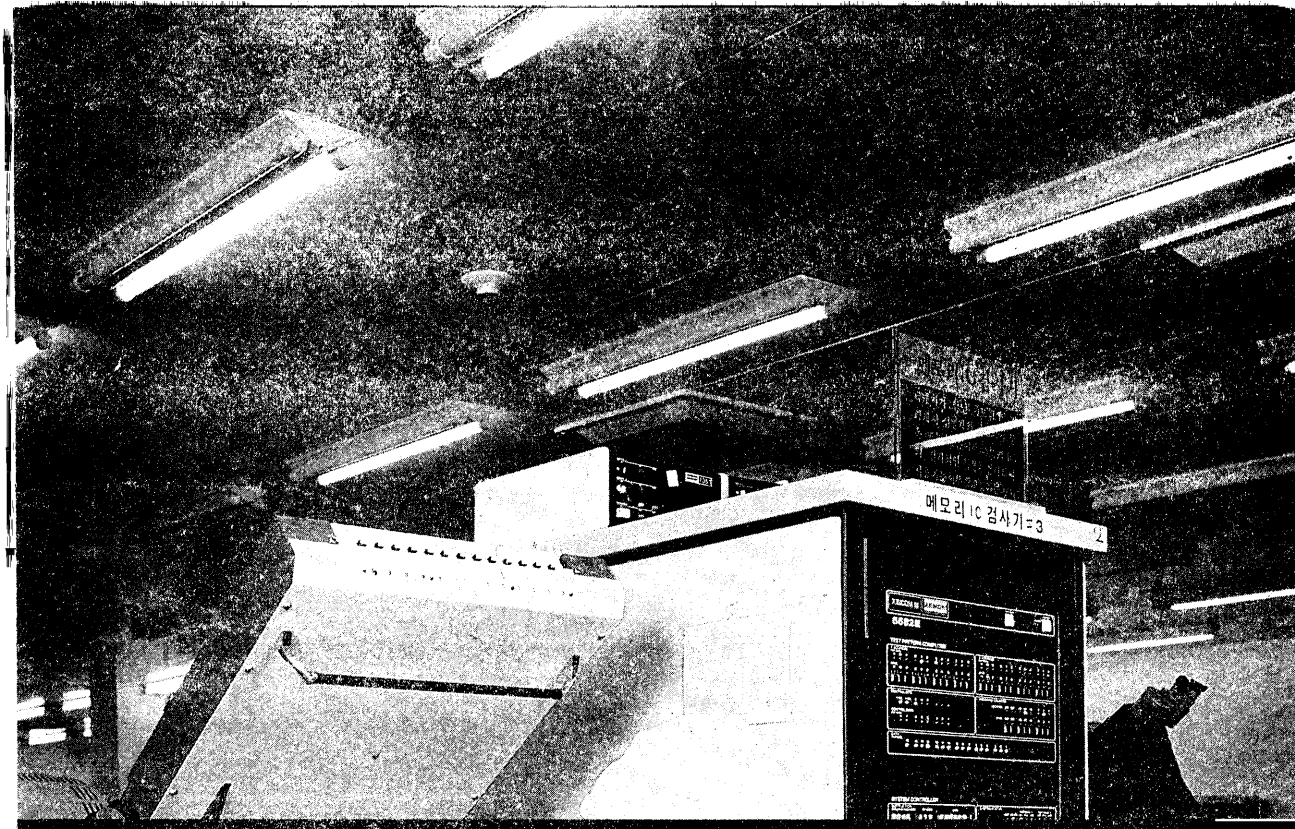
40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)





16M DRAM DATA SHEET 5

16M × 1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM41C16000A/AL/ALL/ASL-5	50ns	13ns	90ns
KM41C16000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM41C16000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM41C16000A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Common I/O using Early Write**
- **Single+5.0V±10% power supply**
- **4096 cycles/64ms refresh**
- **4096 cycles/128ms (Low Power & Self Ref.)**
- **4096 cycles/256ms (Super Low Power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

The Samsung KM41C16000A/AL/ALL/ASL is a high speed CMOS 16,777,216 bit × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

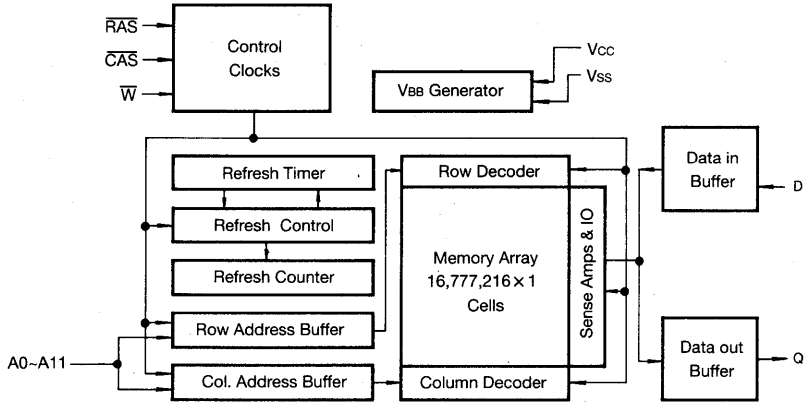
The KM41C16000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

The KM41C16000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

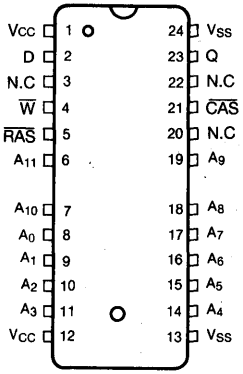
5

FUNCTIONAL BLOCK DIAGRAM



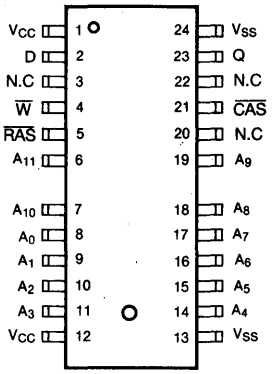
PIN CONFIGURATION (Top Views)

• **KM41C16000 AJ/ALJ/ALLJ/ASLJ**
AK/ALK/ALLK/ASLK



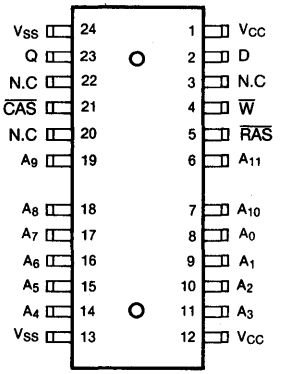
J : 400MIL
K : 300MIL

• **KM41C16000 AT/ALT/ALLT/ASLT**
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S: 300MIL(Forward)

• **KM41C16000 ATR/ALTR/ALLTR/ASLTR**
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
D	Data In
Q	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
VCC	Power(+5.0V)
VSS	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM41C16000A/AL/ALL/ASL-5	I_{CC1}	-	90	mA
	KM41C16000A/AL/ALL/ASL-6			80	mA
	KM41C16000A/AL/ALL/ASL-7			70	mA
	KM41C16000A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM41C16000A	I_{CC2}	-	2	mA
	KM41C16000AL			1	mA
	KM41C16000ALL			1	mA
	KM41C16000ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM41C16000A/AL/ALL/ASL-5	I_{CC3}	-	90	mA
	KM41C16000A/AL/ALL/ASL-6			80	mA
	KM41C16000A/AL/ALL/ASL-7			70	mA
	KM41C16000A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM41C16000A/AL/ALL/ASL-5	I_{CC4}	-	80	mA
	KM41C16000A/AL/ALL/ASL-6			70	mA
	KM41C16000A/AL/ALL/ASL-7			60	mA
	KM41C16000A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM41C16000A	I_{CC5}	-	1	mA
	KM41C16000AL			300	μA
	KM41C16000ALL			200	μA
	KM41C16000ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM41C16000A/AL/ALL/ASL-5	I_{CC6}	-	90	mA
	KM41C16000A/AL/ALL/ASL-6			80	mA
	KM41C16000A/AL/ALL/ASL-7			70	mA
	KM41C16000A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=31.5μS(L-Ver.) 62.5μS(SL-Ver.), T_{RAS}≦min~300ns	KM41C16000AL	I_{CC7}	-	450	μA
	KM41C16000ASL			350	μA

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SAMSUNG ELECTRONICS

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=A0-A11=Vcc-0.2V or 0.2V D,Q=Vcc-0.2V, 0.2V or Open	KM41C16000ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN} ≤Vcc+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	-	7	pF
Input Capacitance (A0-A11)	C_{IN2}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	-	7	pF
Input Capacitance (Q)	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, Vcc=5.0V±0.5V, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64		64	ms	
Refresh period (Low Power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low Power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	13		15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	50		60		70		80		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	25		30		35		40		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	53		60		70		75		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		10		ns	

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AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ refresh)	tRASS	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tRPS	90		110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note 12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	18		20		25		25		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	55		65		75		85		ns	8
Column address to $\overline{W}$ delay time	tAWD	30		35		40		45		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	58		65		75		80		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

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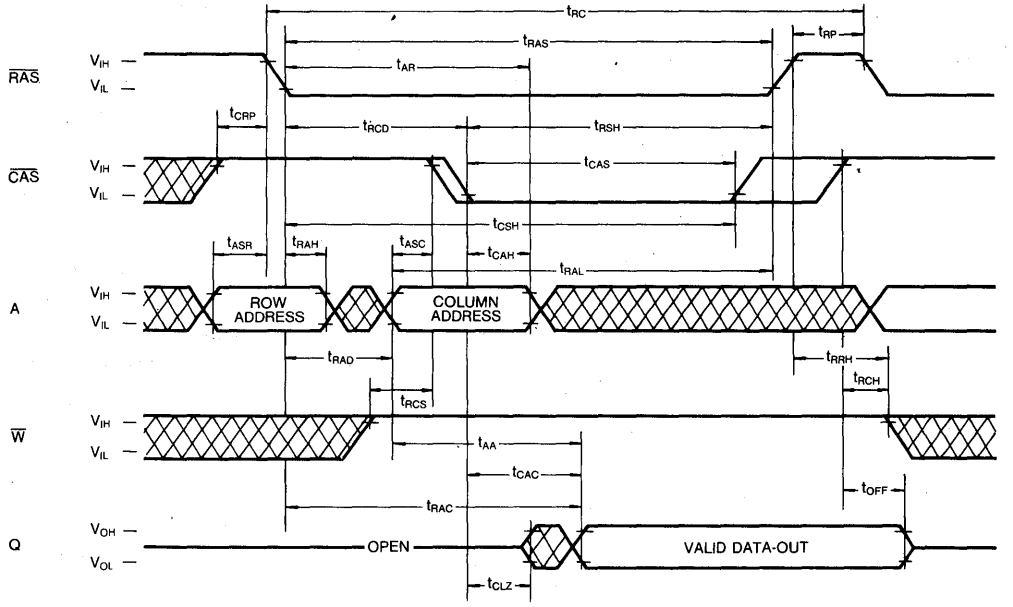
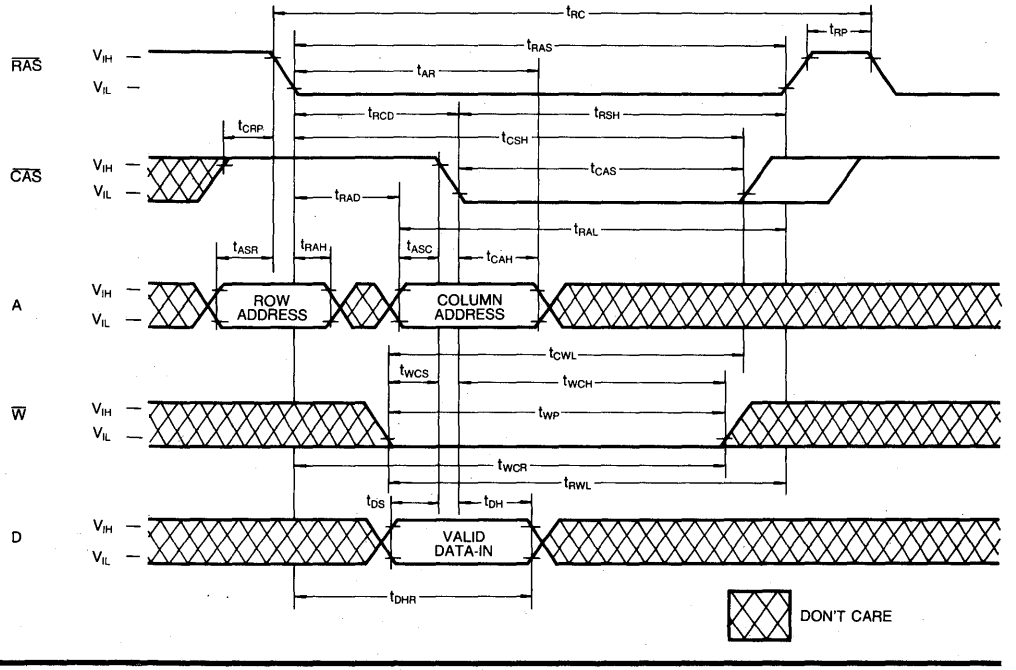
TIMING DIAGRAMS

READ CYCLE

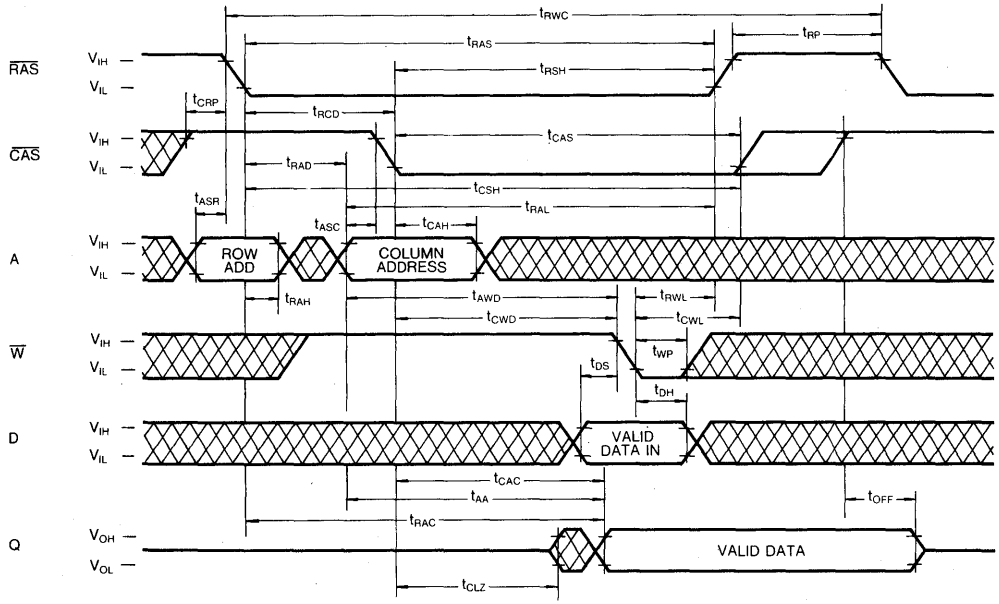


WRITE CYCLE (EARLY WRITE)

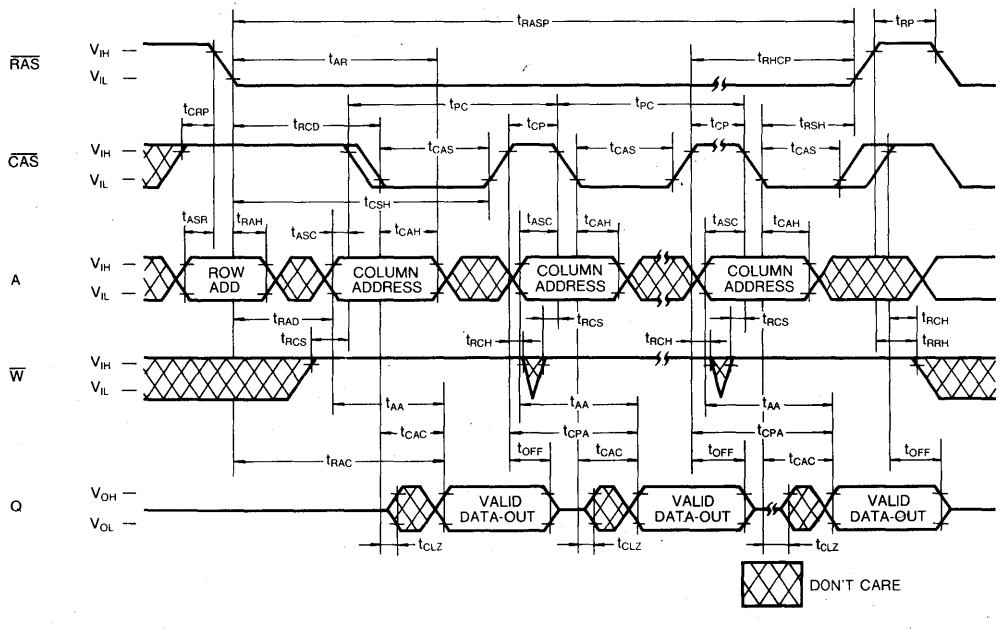


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE



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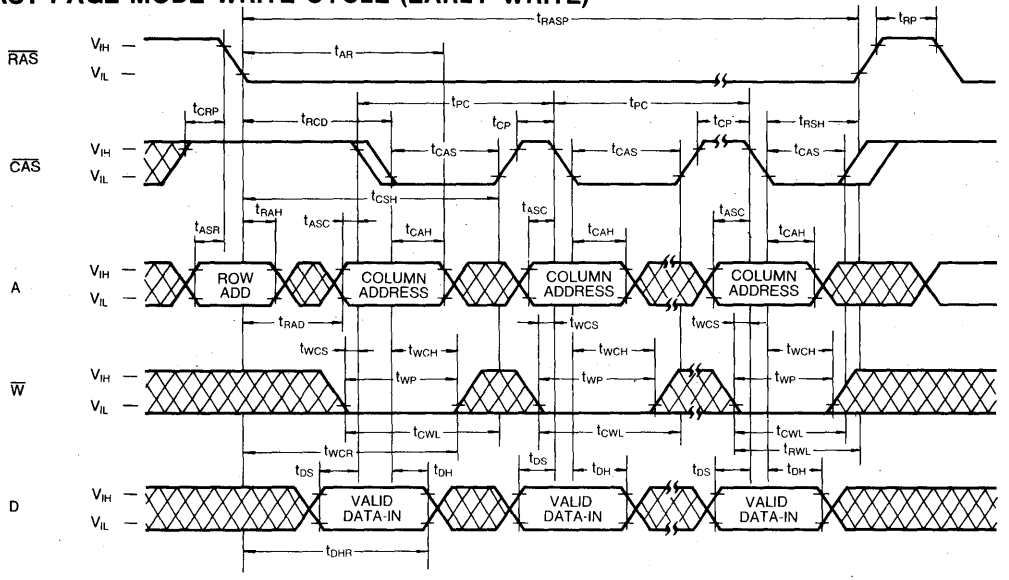
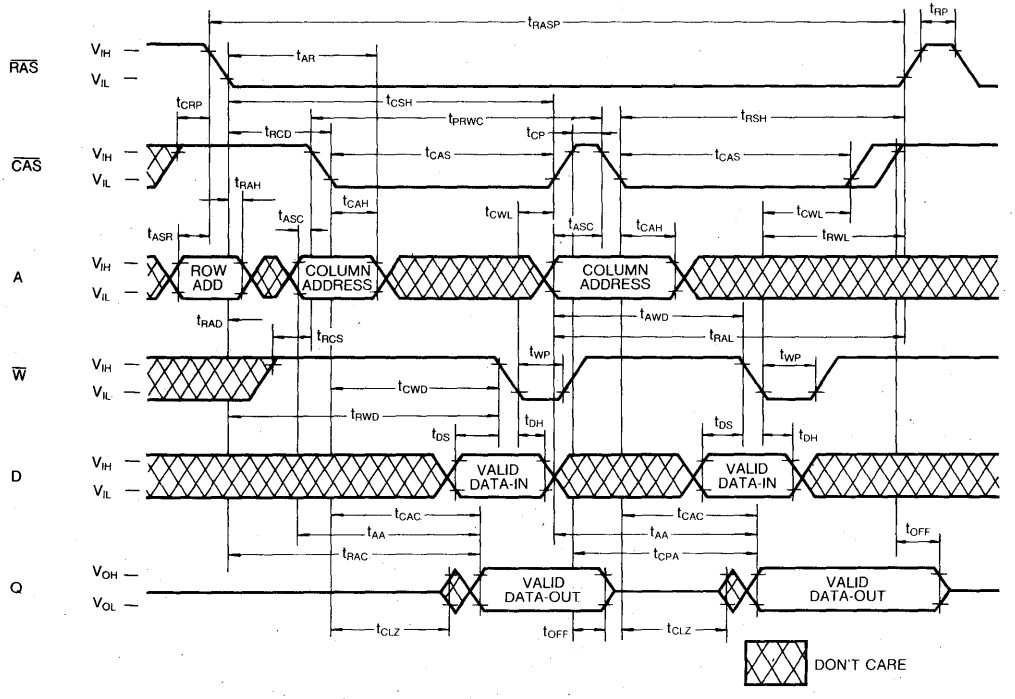
TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



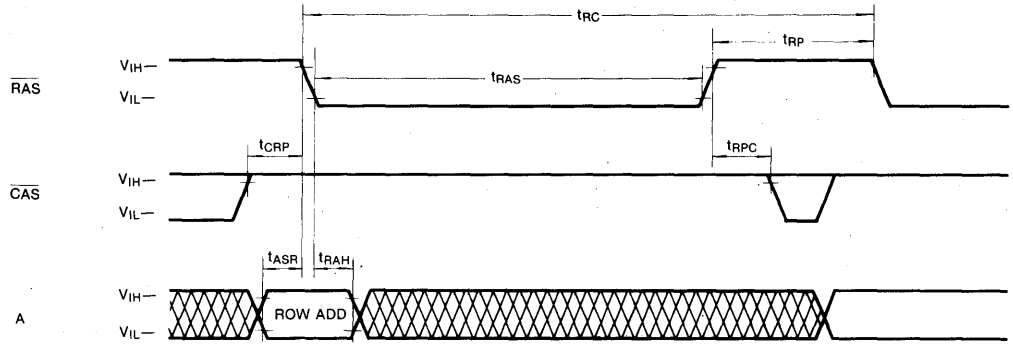
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

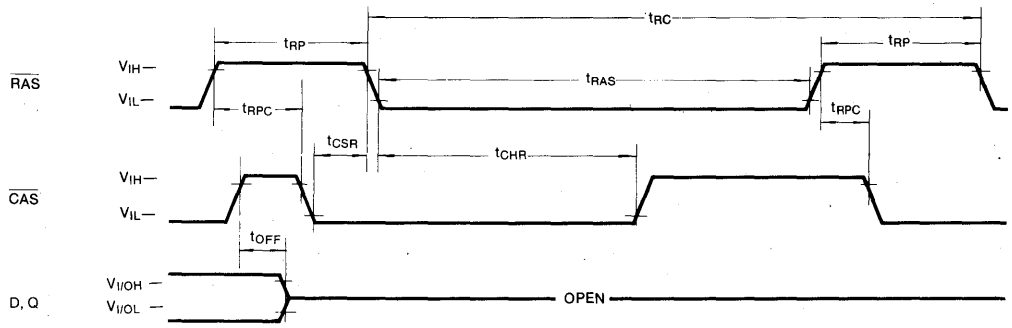
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, = Don't care



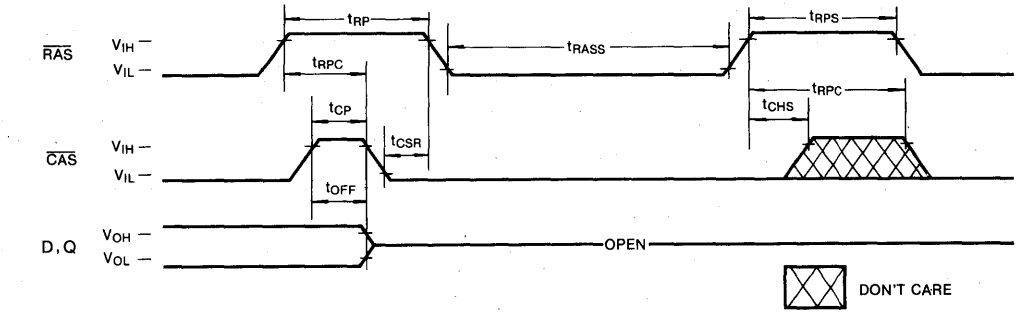
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, A=Don't Care



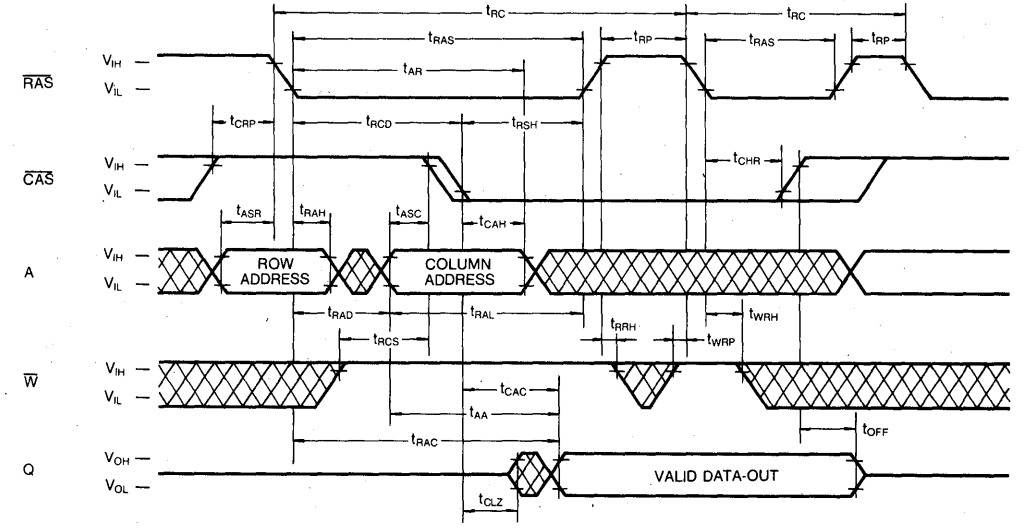
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, A=Don't Care

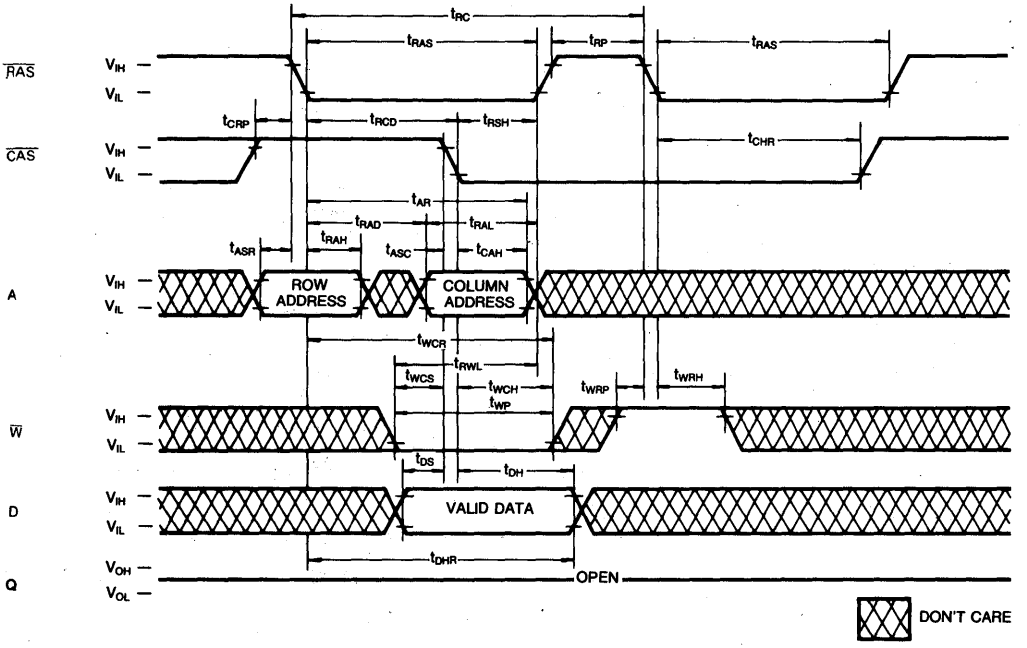


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

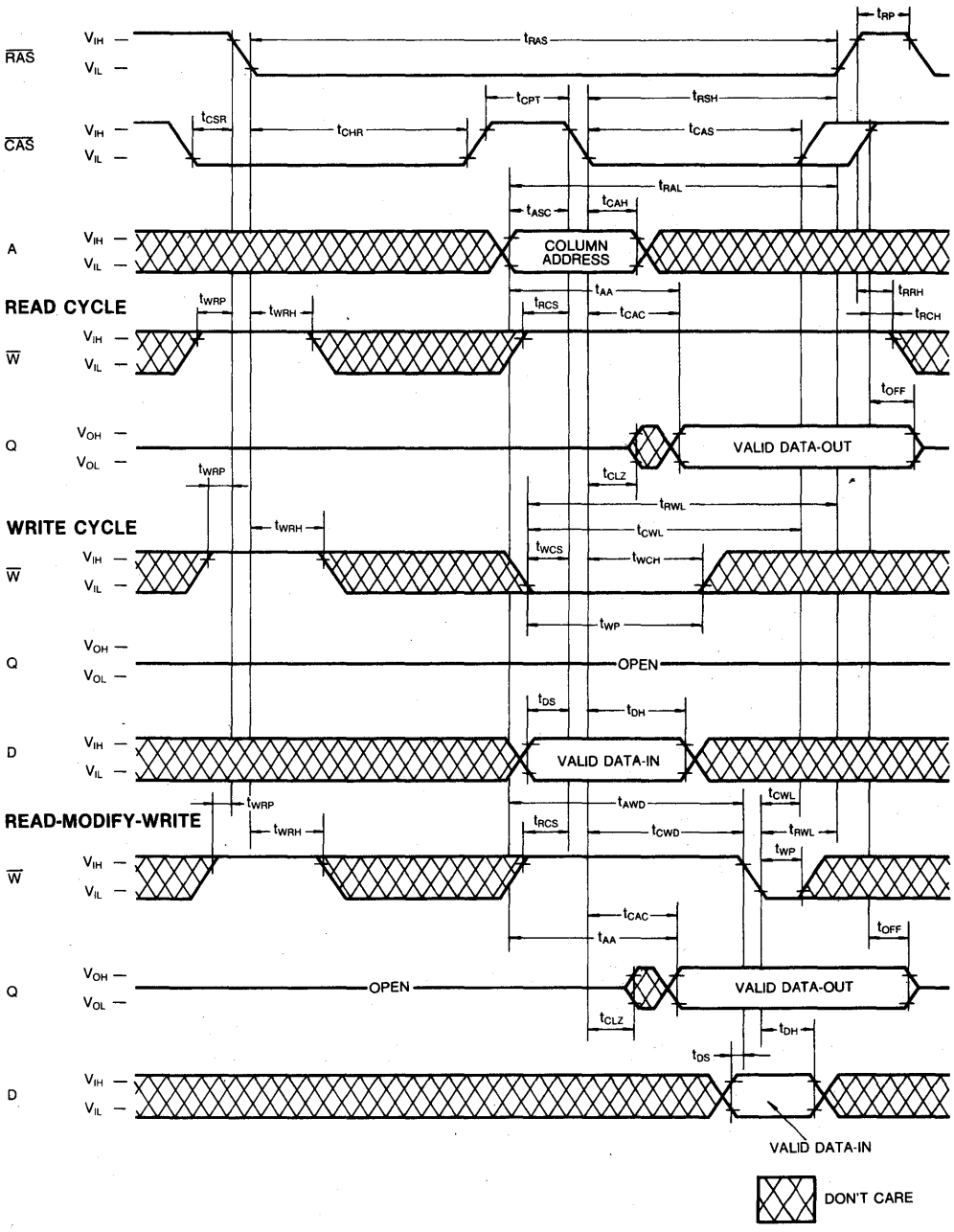


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

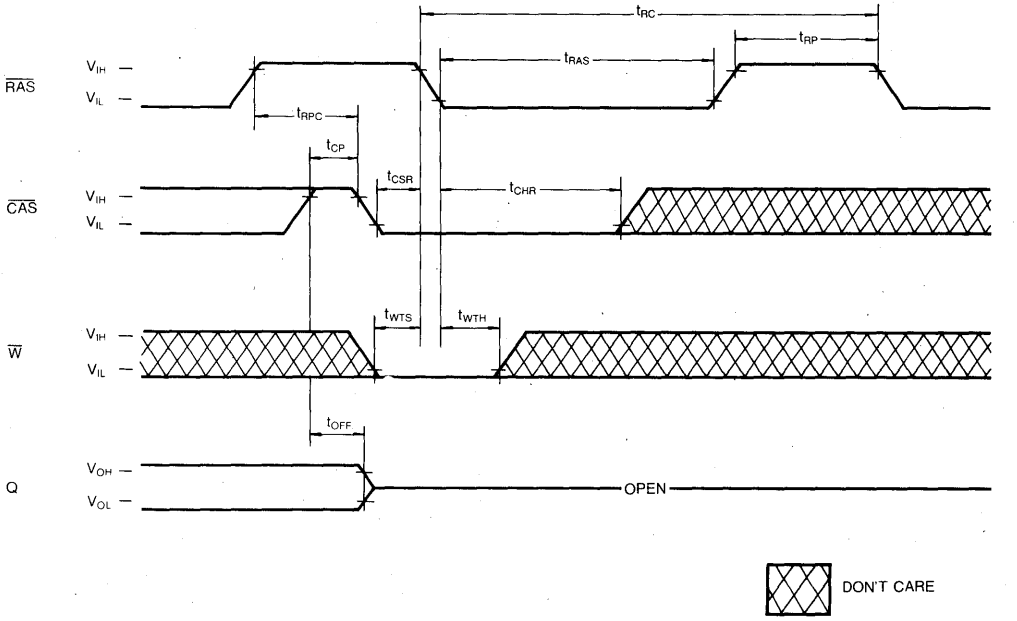
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: D, Address: Don't Care



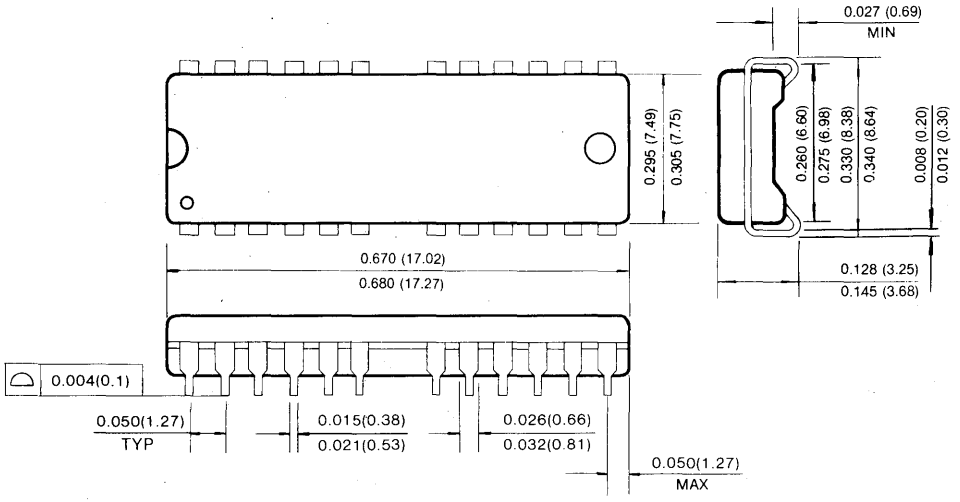
TEST MODE DESCRIPTION

The KM41C16000A/AL/ALL/ASL is the RAM organized 16,777,216 words by 1 bit, it is internally organized 1, 048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0, A_1, A_{10} and A_{11} are not used. If, upon reading, 16 bits are equal (all "1"s or "0"s) the Q pin indicates a "1".
If they were not equal, the Q pin would indicate a "0". In "Test Mode", the 16M DRAM can be tested as if it were a 1M × 1 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/16 in cases of N test pattern).

PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



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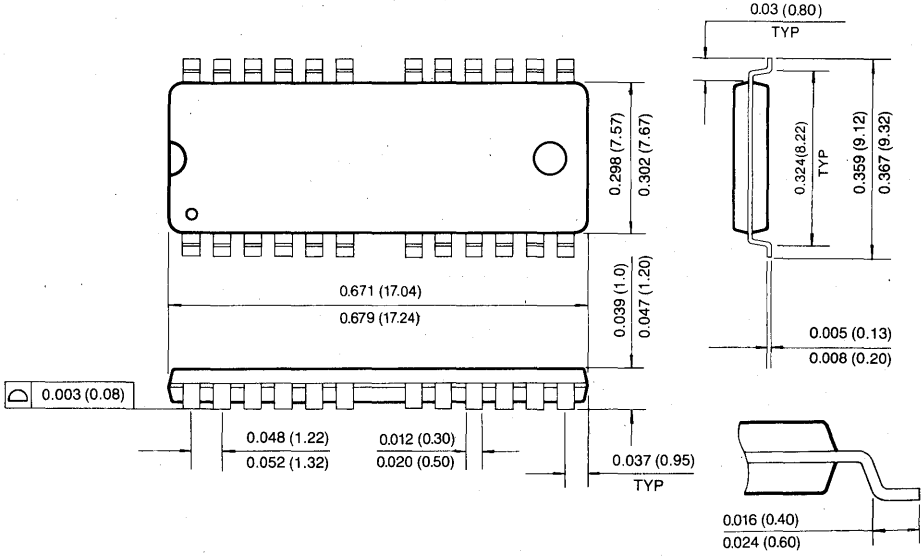
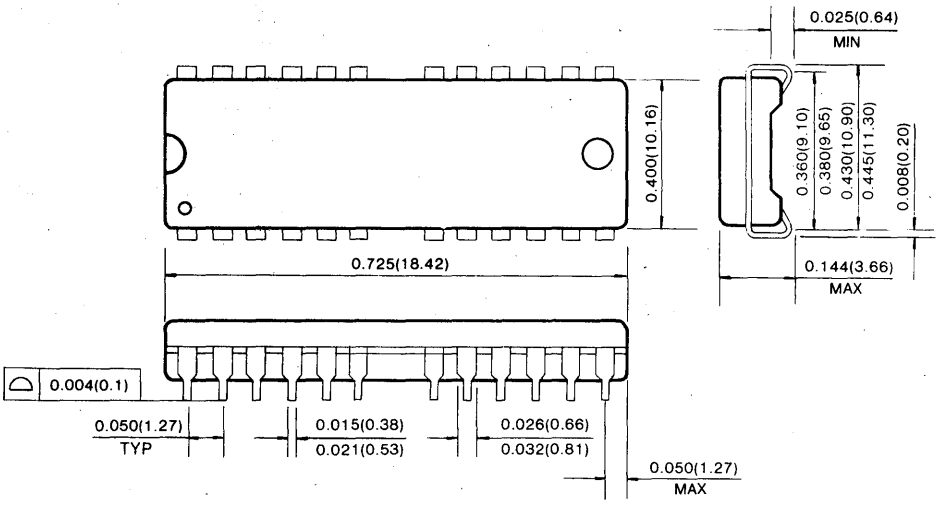
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



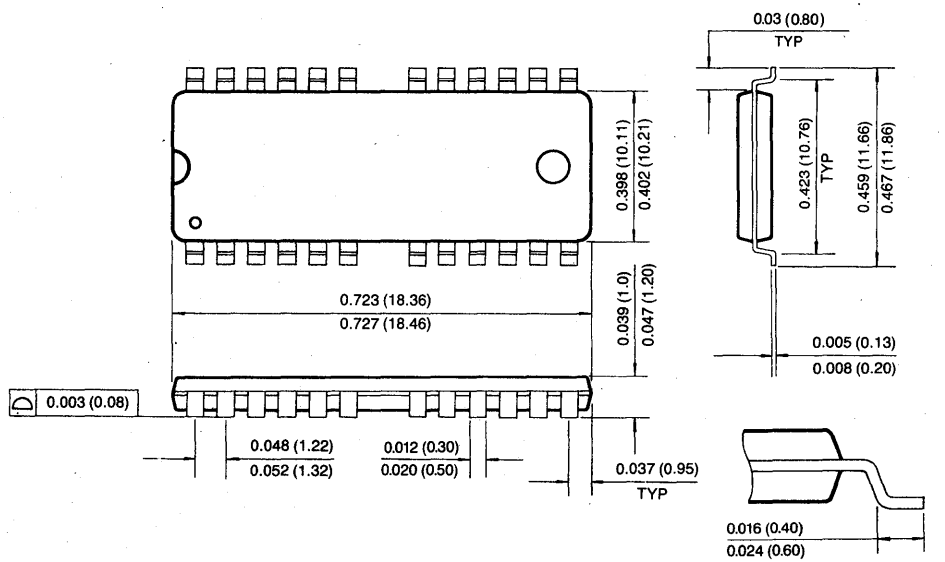
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



16M ×1 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM41C16002A/AL/ALL/ASL-5	50ns	13ns	90ns
KM41C16002A/AL/ALL/ASL-6	60ns	15ns	110ns
KM41C16002A/AL/ALL/ASL-7	70ns	20ns	130ns
KM41C16002A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Static Column Mode operation**
- **Self Refresh Operation (LL-ver, only)**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V±10% power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

The Samsung KM41C16002A/AL/ALL/ASL is a high speed CMOS 16,777,216 bit × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM41C16002A/AL/ALL/ASL features Static Column Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

The KM41C16002A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

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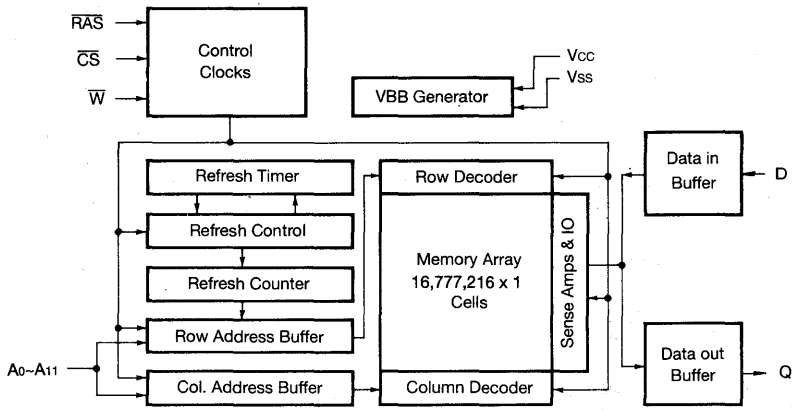
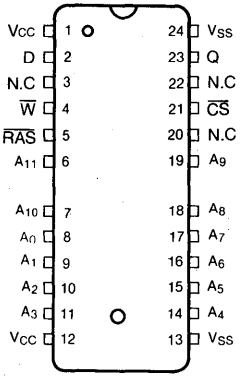
FUNCTIONAL BLOCK DIAGRAM



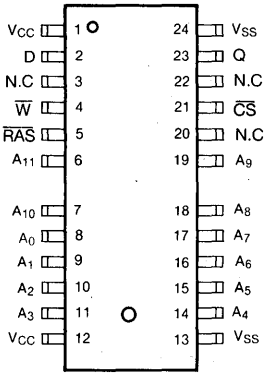
PIN CONFIGURATION (Top Views)

• **KM41C16002 AJ/ALJ/ALLJ/ASLJ**
AK/ALK/ALLK/ASLK



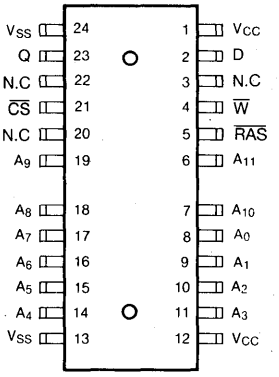
J : 400MIL
K : 300MIL

• **KM41C16002 AT/ALT/ALLT/ASLT**
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S: 300MIL(Forward)

• **KM41C16002 ATR/ALTR/ALLTR/ASLTR**
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
D	Data In
Q	Data out
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select input
$\overline{W}$	Read/Write Input
VCC	Power(+5.0V)
VSS	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC}=min.)	KM41C16002A/AL/ALL/ASL-5	I_{CC1}	-	90	mA
	KM41C16002A/AL/ALL/ASL-6			80	mA
	KM41C16002A/AL/ALL/ASL-7			70	mA
	KM41C16002A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{IH})	KM41C16002A	I_{CC2}	-	2	mA
	KM41C16002AL			1	mA
	KM41C16002ALL			1	mA
	KM41C16002ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM41C16002A/AL/ALL/ASL-5	I_{CC3}	-	90	mA
	KM41C16002A/AL/ALL/ASL-6			80	mA
	KM41C16002A/AL/ALL/ASL-7			70	mA
	KM41C16002A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CS}$, Address Cycling @t_{PC}=min.)	KM41C16002A/AL/ALL/ASL-5	I_{CC4}	-	80	mA
	KM41C16002A/AL/ALL/ASL-6			70	mA
	KM41C16002A/AL/ALL/ASL-7			60	mA
	KM41C16002A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{CC}-0.2V)	KM41C16002A	I_{CC5}	-	1	mA
	KM41C16002AL			300	μA
	KM41C16002ALL			200	μA
	KM41C16002ASL			200	μA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC}=min.)	KM41C16002A/AL/ALL/ASL-5	I_{CC6}	-	90	mA
	KM41C16002A/AL/ALL/ASL-6			80	mA
	KM41C16002A/AL/ALL/ASL-7			70	mA
	KM41C16002A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CS}$=$\overline{CS}$-Before-$\overline{RAS}$ Cycling or 0.2V D=Don't Care t_{RC}=31.25μs(L-Ver.) 62.5μs(SL-Ver.), t_{RAS} =t_{RAS} min~300ns	KM41C16002AL	I_{CC7}	-	450	μA
	KM41C16002ASL			350	μA

SAMSUNG ELECTRONICS

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CS}$=0.2V $\overline{W}$=A0-A11=Vcc-0.2V or 0.2V Vcc-0.2V, 0.2V or Open	KM41C16002ALL	Iccs	-	300	μA
Input Leakage Current (Any input 0≤VIN ≤Vcc+0.5V, all other pins not under test=0 volts.)		IIL	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤VOUT≤Vcc)		IOL	-10	10	μA
Output High Voltage Level (IOH=-5mA)		VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)		VOL	-	0.4	V

*NOTE: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, Address can be changed maximum two times while $\overline{RAS}$=VIL. In ICC4, Address can be changed maximum once within one Static Column cycle.

CAPACITANCE (TA=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	CIN1	-	7	pF
Input Capacitance (A0~A11)	CIN2	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$)	CIN3	-	7	pF
Input Capacitance (Q)	COUT	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, Vcc=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	115		135		155		175		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,11
Access time from $\overline{CS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
$\overline{CS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CS}$ pulse width	tCS	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		50		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64		64	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	15		15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	50		60		70		80		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	25		30		35		40		ns	8
$\overline{CS}$ set-up time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Static column mode cycle time	t_{SC}	30		35		40		45		ns	3
Static column mode read-write cycle time	t_{SRWC}	50		60		70		80		ns	
Access time from last write	t_{ALW}		50		55		65		75	ns	3, 12
Output data hold time from column address	t_{AOH}	5		5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		35		40		45		55	ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{CS}$ pulse width (Static column mode)	t_{CSC}	13	200000	15	200000	20	200000	20	200000	ns	
$\overline{CS}$ precharge time (Static column mode)	t_{CP}	10		10		10		10		ns	
Column address hold time referenced to $\overline{RAS}$ rising	t_{AH}	5		5		5		5		ns	
Last write to column address delay time	t_{LWAD}	20	25	20	25	25	30	25	35	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Last write to column address hold time	t_{AHLW}	50		55		65		75		ns	
Write command inactive time	t_{WI}	10		10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	13		15		20		20		ns	
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	40		45		55		60		ns	6
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	90		110		130		150		ns	15
$\overline{CS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	95		115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	140		160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		55		65		75		85	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		18		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CS}$ pulse width	t_{CS}	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		25		ns	
$\overline{CS}$ hold time	t_{CSH}	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		45		ns	
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	45		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	80		90		105		115		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		60		70		75		ns	8
Static column mode cycle time	t_{SC}	35		40		45		50		ns	
Static column mode read-write cycle time	t_{SRWC}	85		90		105		110		ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from last write	t_{ALW}		50		60		70		80	ns	3,12

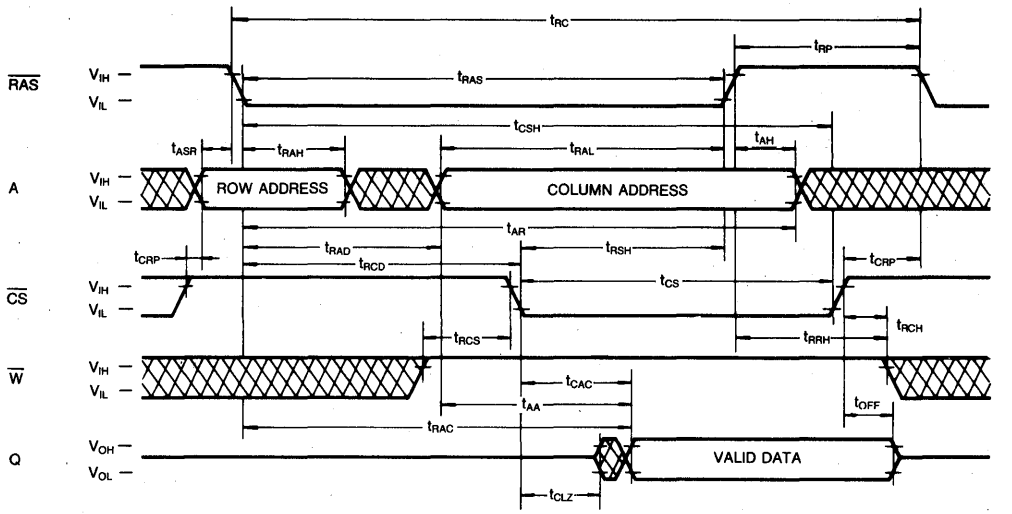
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data output is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

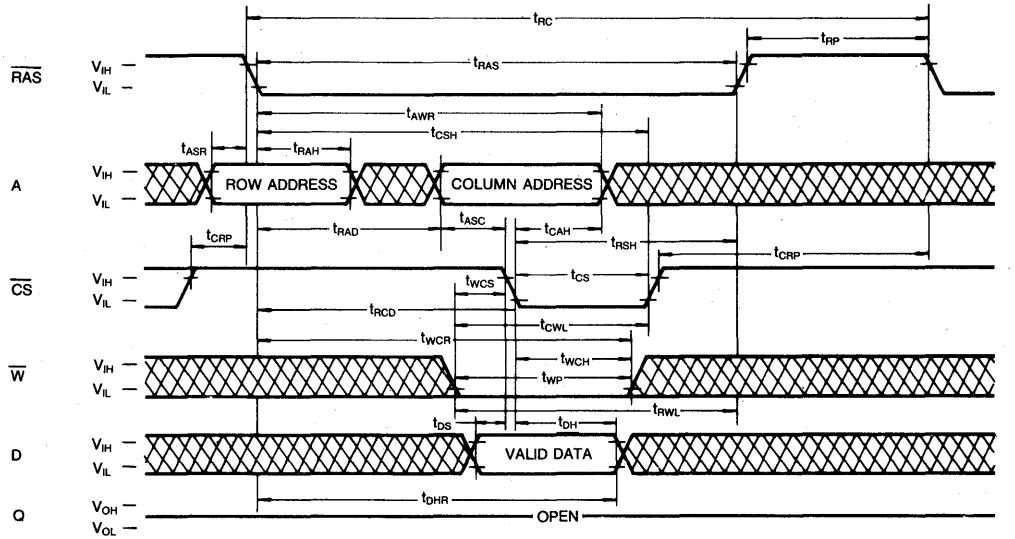
5

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE (EARLY WRITE)

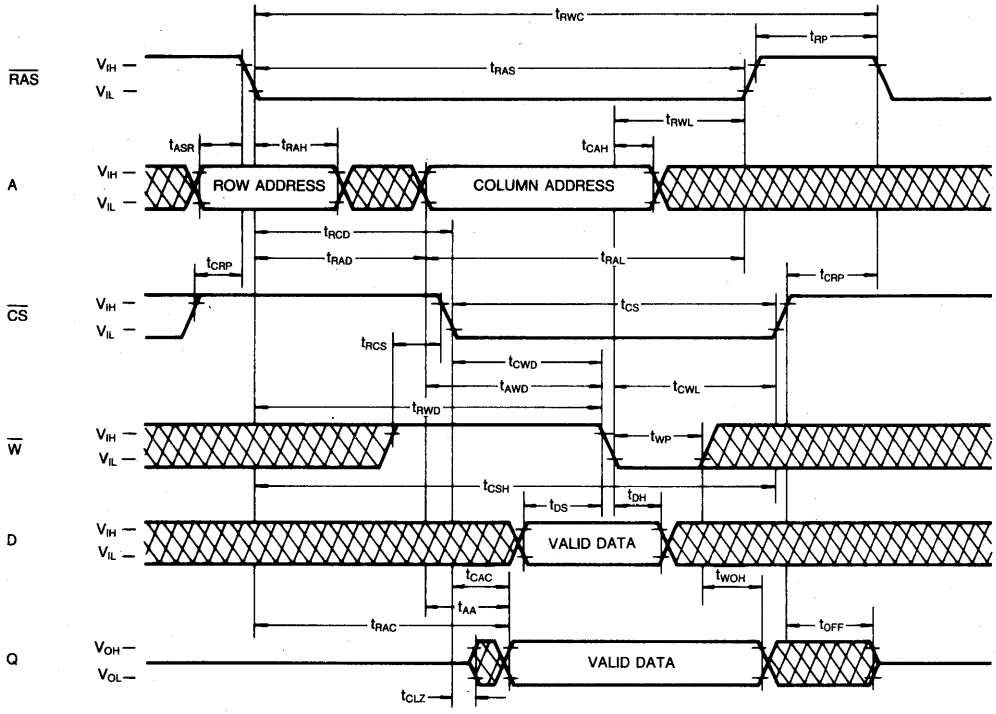


DON'T CARE

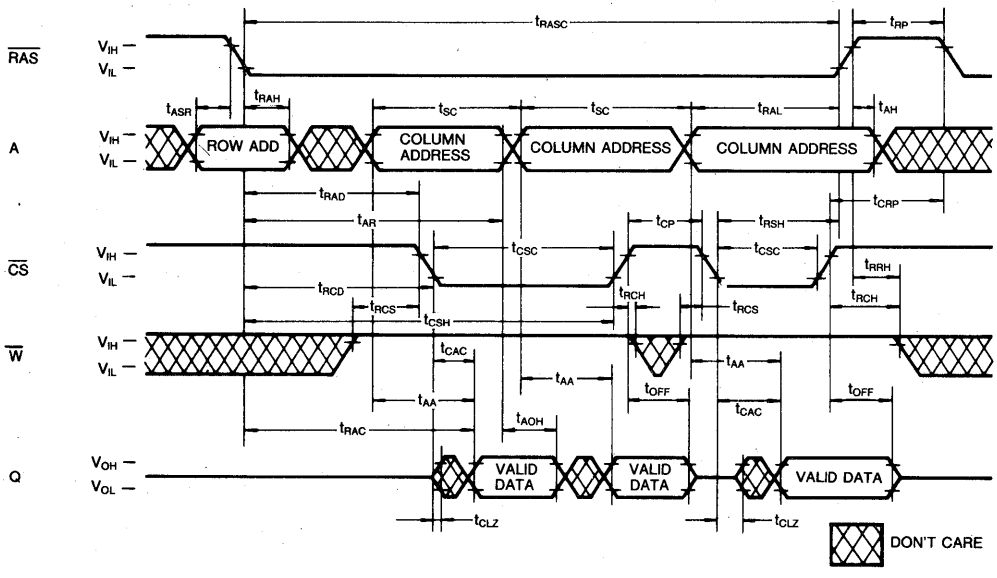
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



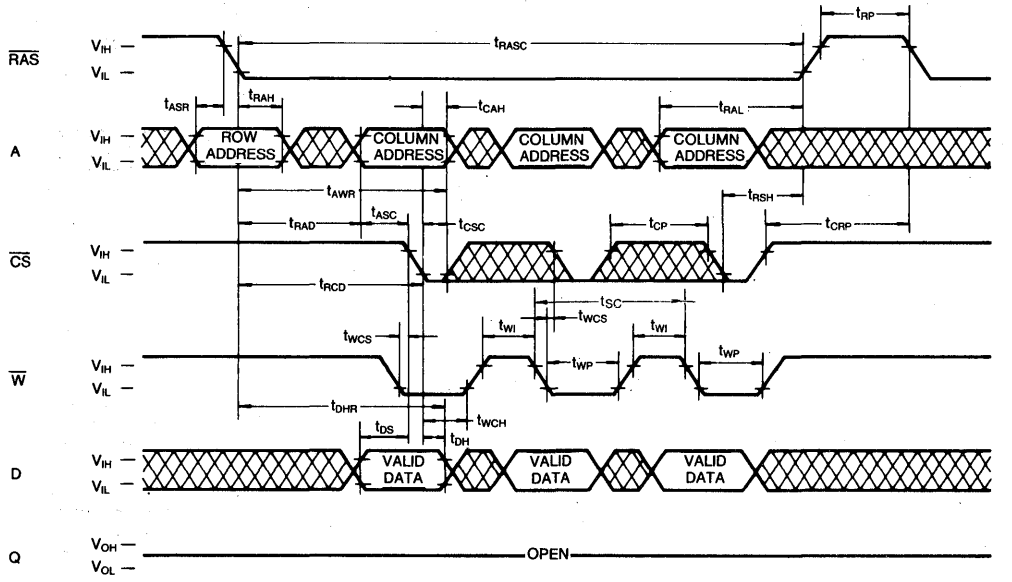
STATIC COLUMN MODE READ CYCLE



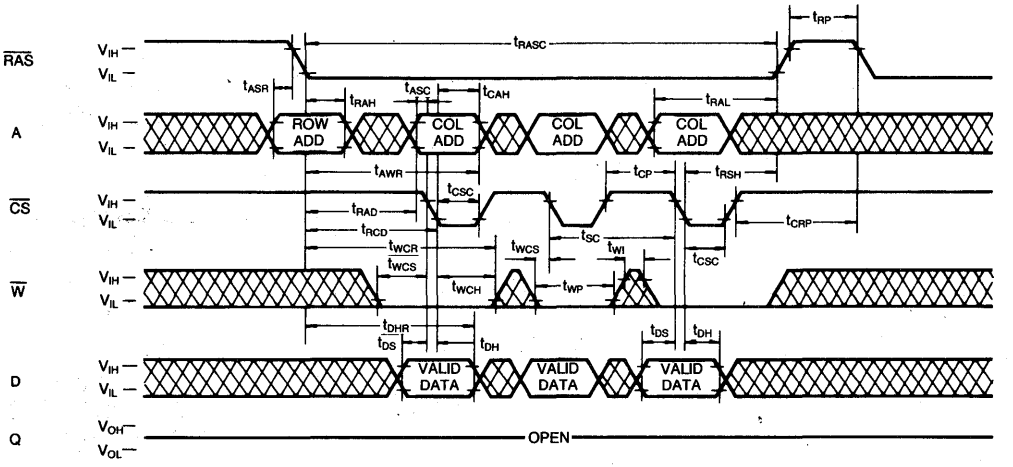
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ CONTROLLED EARLY WRITE)



STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ CONTROLLED EARLY WRITE)

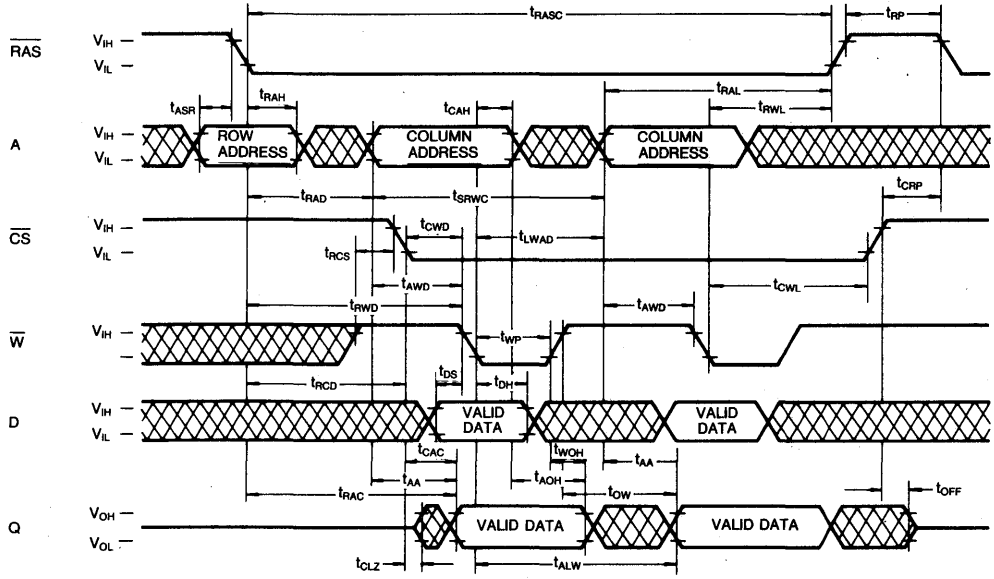


DON'T CARE

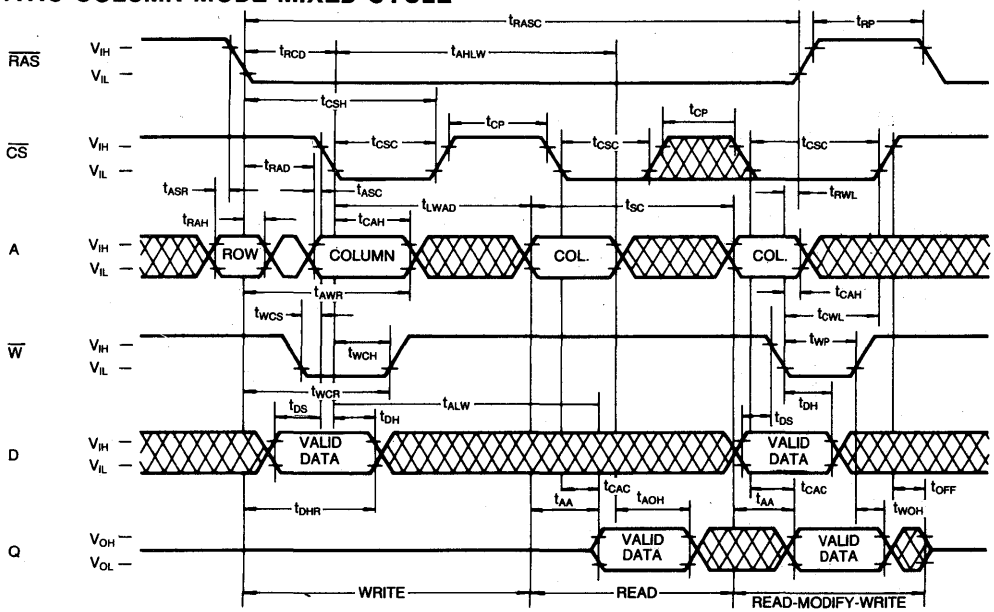
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-WRITE CYCLE



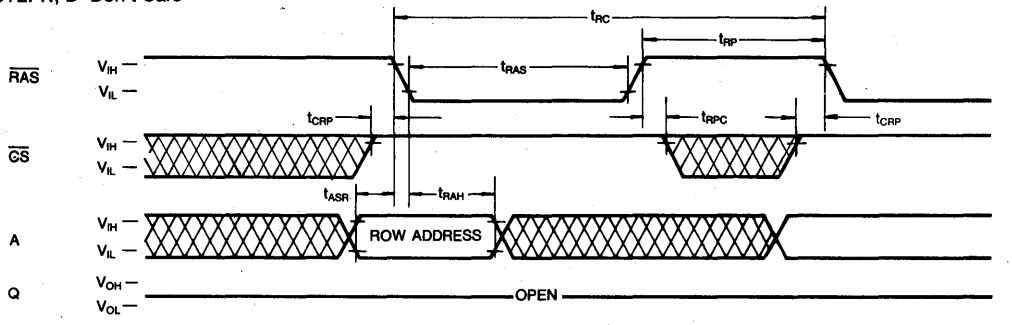
STATIC COLUMN MODE MIXED CYCLE



TIMING DIAGRAMS (Continued)

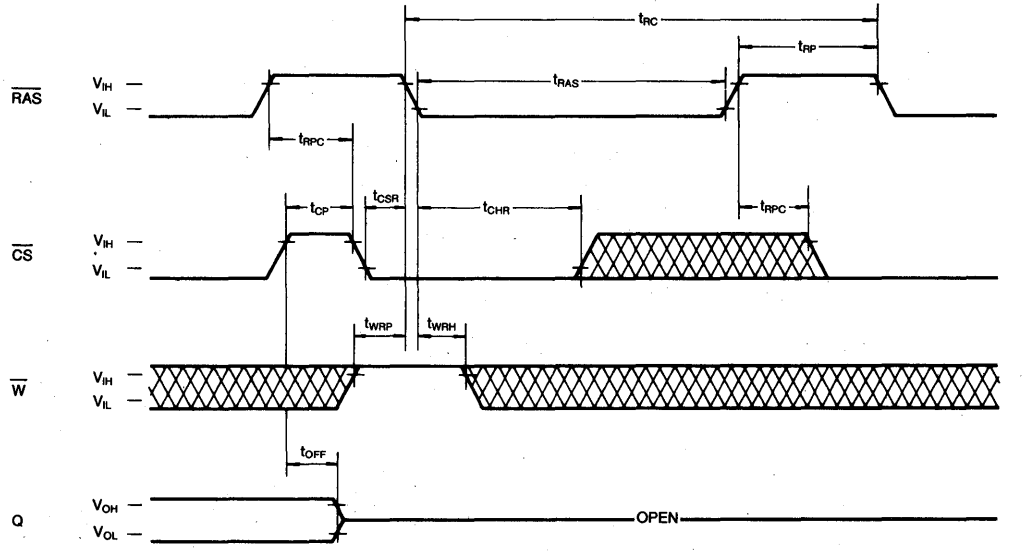
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{W}$, D=Don't Care



$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address=Don't Care

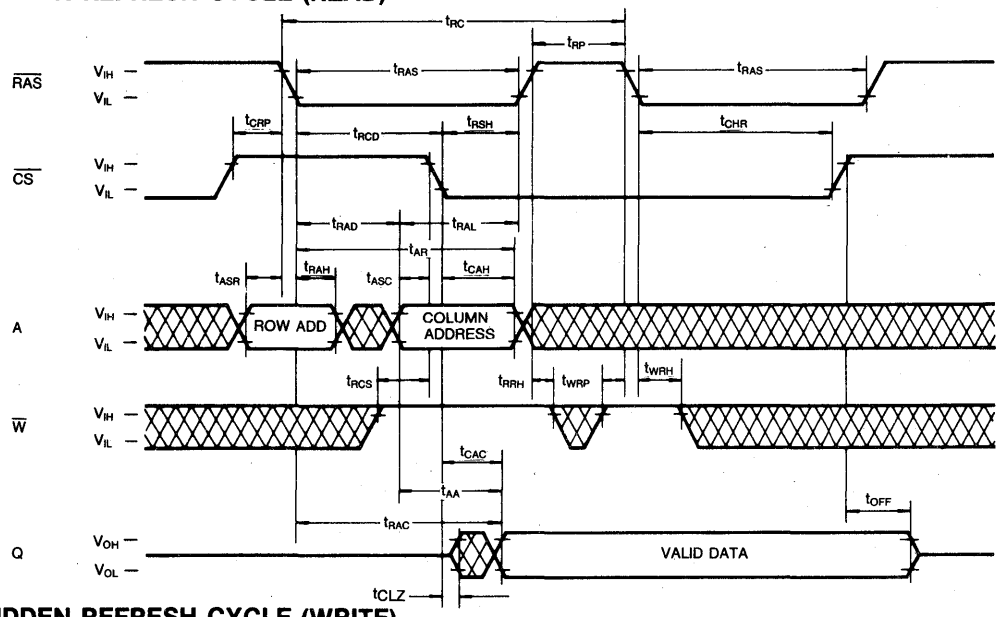


DON'T CARE

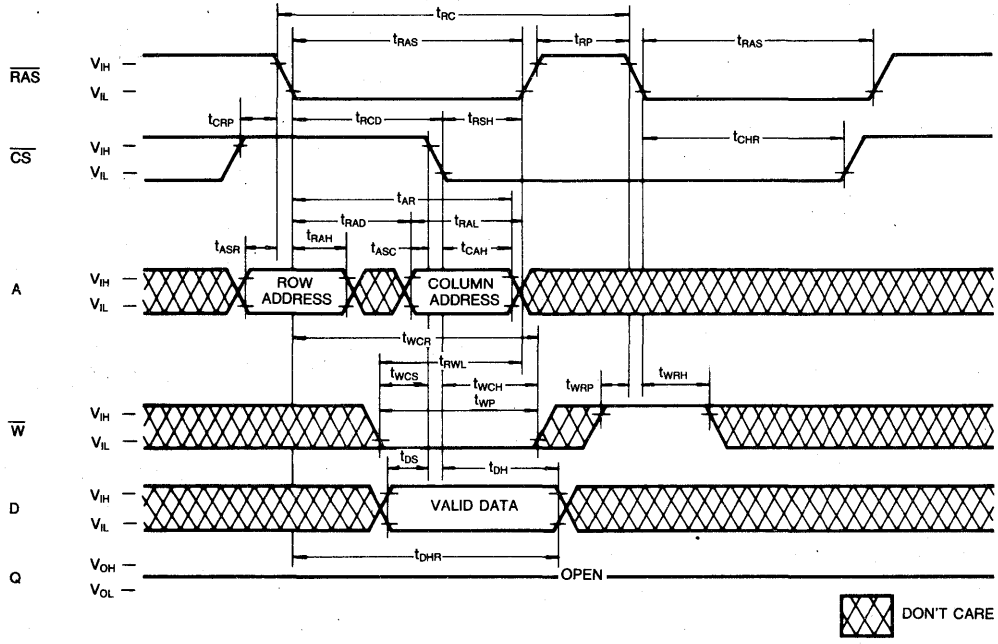
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

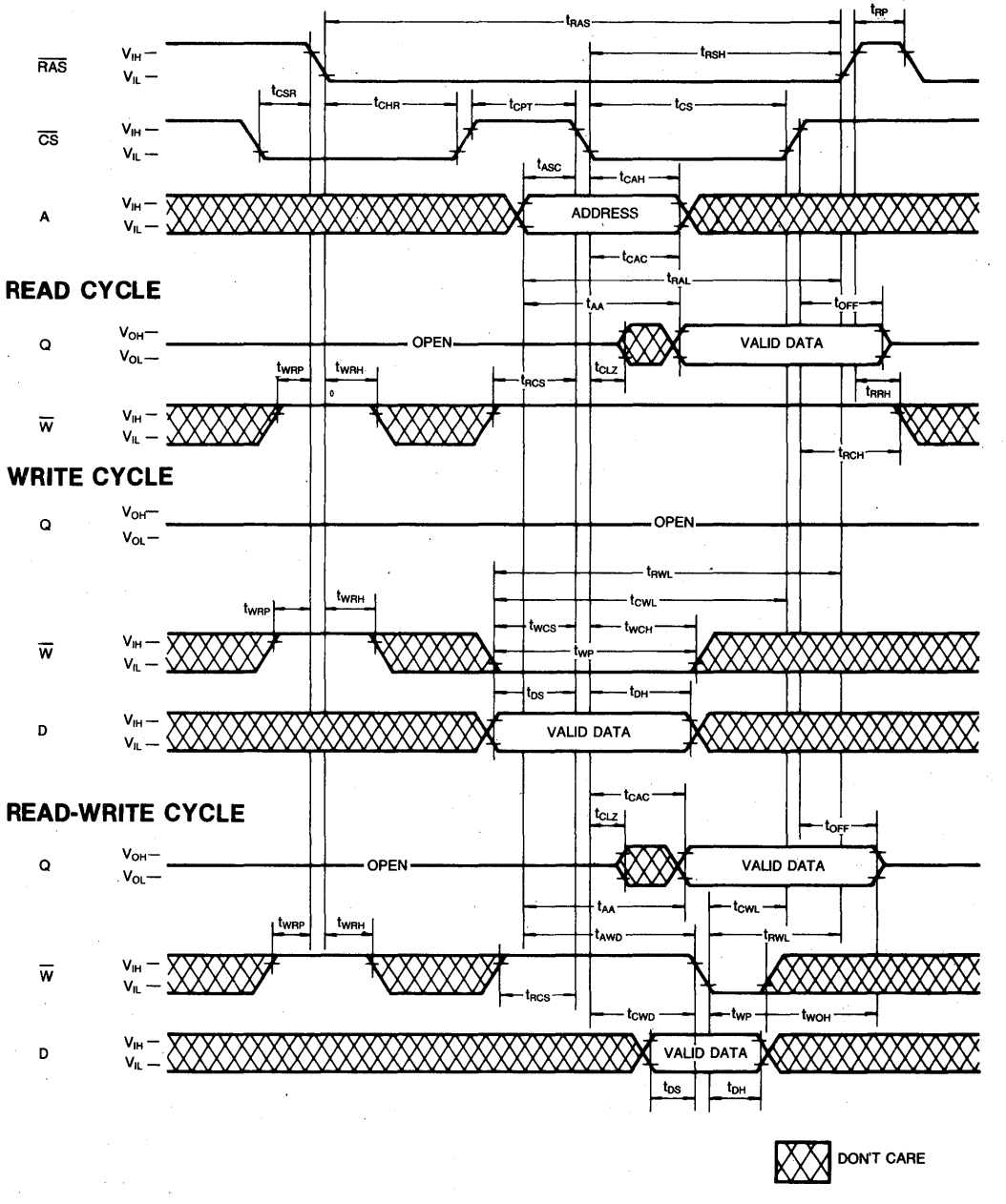


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

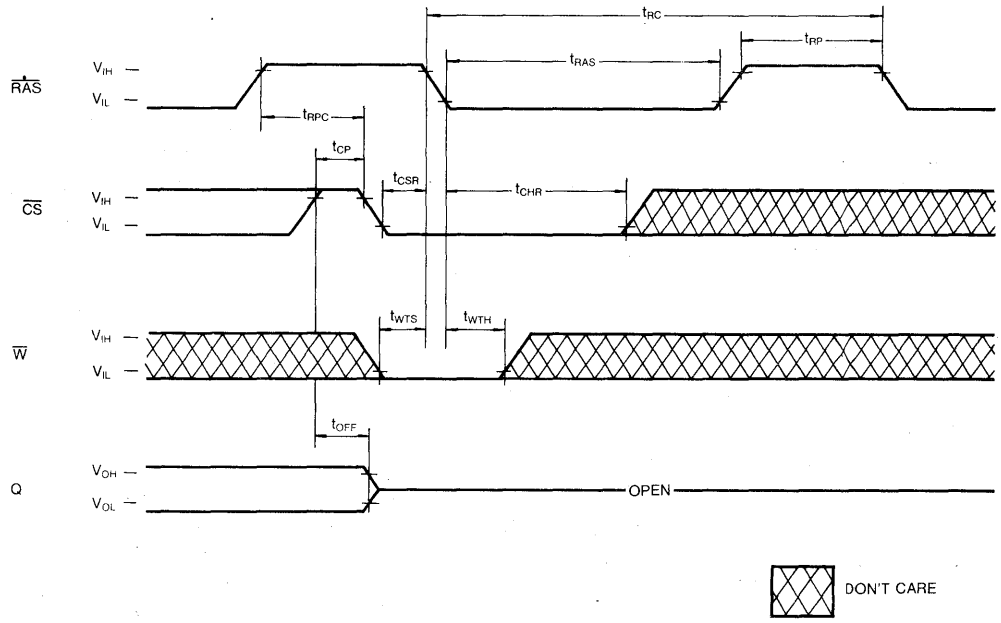


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: D, Address: Don't Care



TEST MODE DESCRIPTION

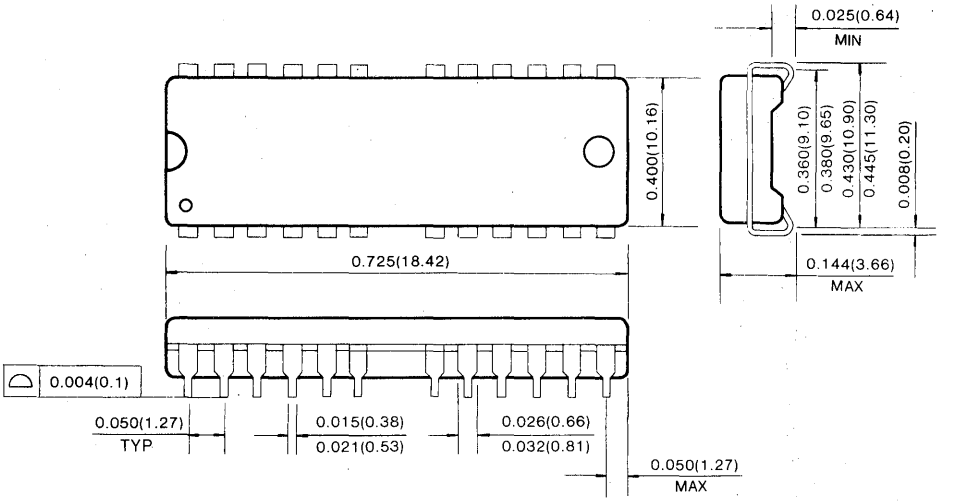
The KM41C16002 is the RAM organized 16,777,216 words by 1 bit, it is internally organized 1,048,576 words by 16 bits. In "Test mode," data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0, A_1, A_{10} and A_{11} are not used. If, upon reading, 16 bits are equal (all "1" or "0"s) the Q pin indicates a "1."

If they were not equal, the Q pin would indicate a "0." In "Test Mode," the 16M DRAM can be tested as if it were a 1M × 1 DRAM. $\overline{W}$, $\overline{CS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode." And "$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode." The "Test Mode" function reduces test time (1/16 in cases of N test pattern).

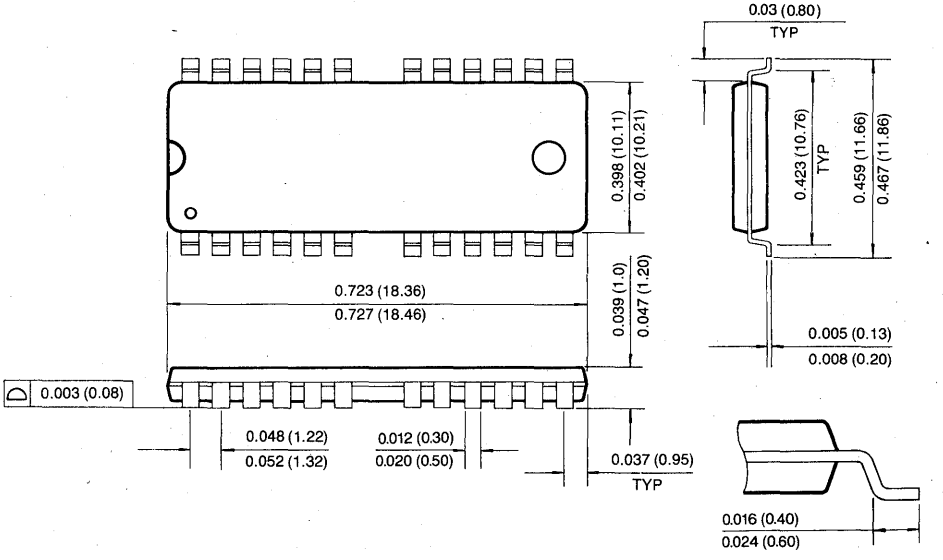
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)



4M ×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM44C4000A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4000A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V±10% power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

The Samsung KM44C4000A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C4000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

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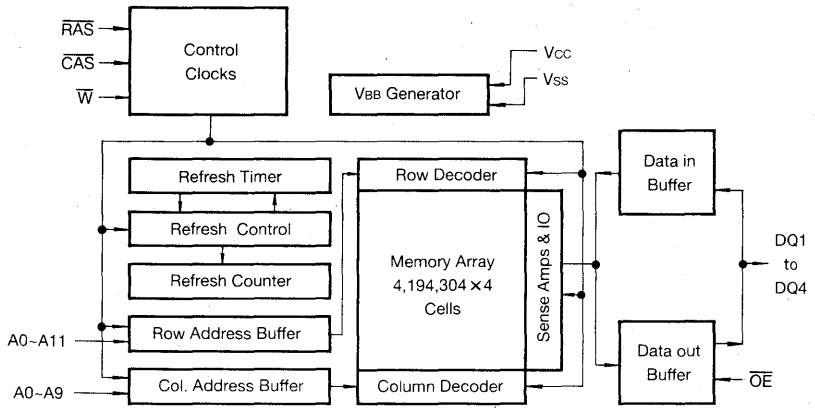
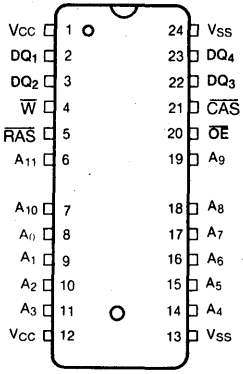
FUNCTIONAL BLOCK DIAGRAM



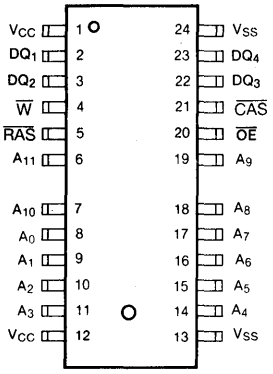
PIN CONFIGURATION (Top Views)

• KM44C4000 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



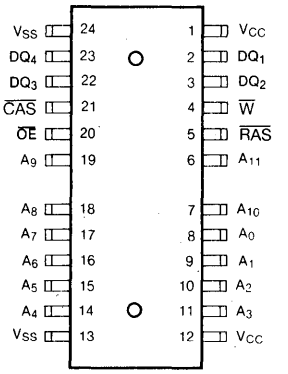
J : 400MIL
K : 300MIL

• KM44C4000 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44C4000 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1~4	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power(+5.0V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4000A/AL/ALL/ASL-5	I_{CC1}	-	90	mA
	KM44C4000A/AL/ALL/ASL-6			80	mA
	KM44C4000A/AL/ALL/ASL-7			70	mA
	KM44C4000A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44C4000A	I_{CC2}	-	2	mA
	KM44C4000AL			1	mA
	KM44C4000ALL			1	mA
	KM44C4000ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44C4000A/AL/ALL/ASL-5	I_{CC3}	-	90	mA
	KM44C4000A/AL/ALL/ASL-6			80	mA
	KM44C4000A/AL/ALL/ASL-7			70	mA
	KM44C4000A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44C4000A/AL/ALL/ASL-5	I_{CC4}	-	80	mA
	KM44C4000A/AL/ALL/ASL-6			70	mA
	KM44C4000A/AL/ALL/ASL-7			60	mA
	KM44C4000A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM44C4000A	I_{CC5}	-	1	mA
	KM44C4000AL			300	μA
	KM44C4000ALL			200	μA
	KM44C4000ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4000A/AL/ALL/ASL-5	I_{CC6}	-	90	mA
	KM44C4000A/AL/ALL/ASL-6			80	mA
	KM44C4000A/AL/ALL/ASL-7			70	mA
	KM44C4000A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=31.25μS(L-Ver.) 62.5μS(SL-Ver.), T_{RAS}≦min~300ns	KM44C4000AL	I_{CC7}	-	450	μA
	KM44C4000ASL			350	μA

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DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A0-A11=VCC-0.2V or 0.2V DQ1-DQ4=VCC-0.2V, 0.2V or Open	KM44C4000ALL	ICCS	-	300	μA
Input Leakage Current (Any input 0≤VIN ≤VCC+0.5V, all other pins not under test=0 volts.)		II(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤VOUT≤VCC)		IO(L)	-10	10	μA
Output High Voltage Level (IOH=-5mA)		VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)		VOL	-	0.4	V

*NOTE: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, Address can be changed maximum two times while $\overline{RAS}$=VIL. In ICC4, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (TA=25°C, VCC=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0~A11)	CIN1	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	CIN2	-	7	pF
Input Capacitance (DQ1~DQ4)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, VCC=5.0V±0.5V, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64		64	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	76		85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ pulse width(Fast Page mode)	t_{RASP}	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		13		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	13		15		20		20		ns	

5

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

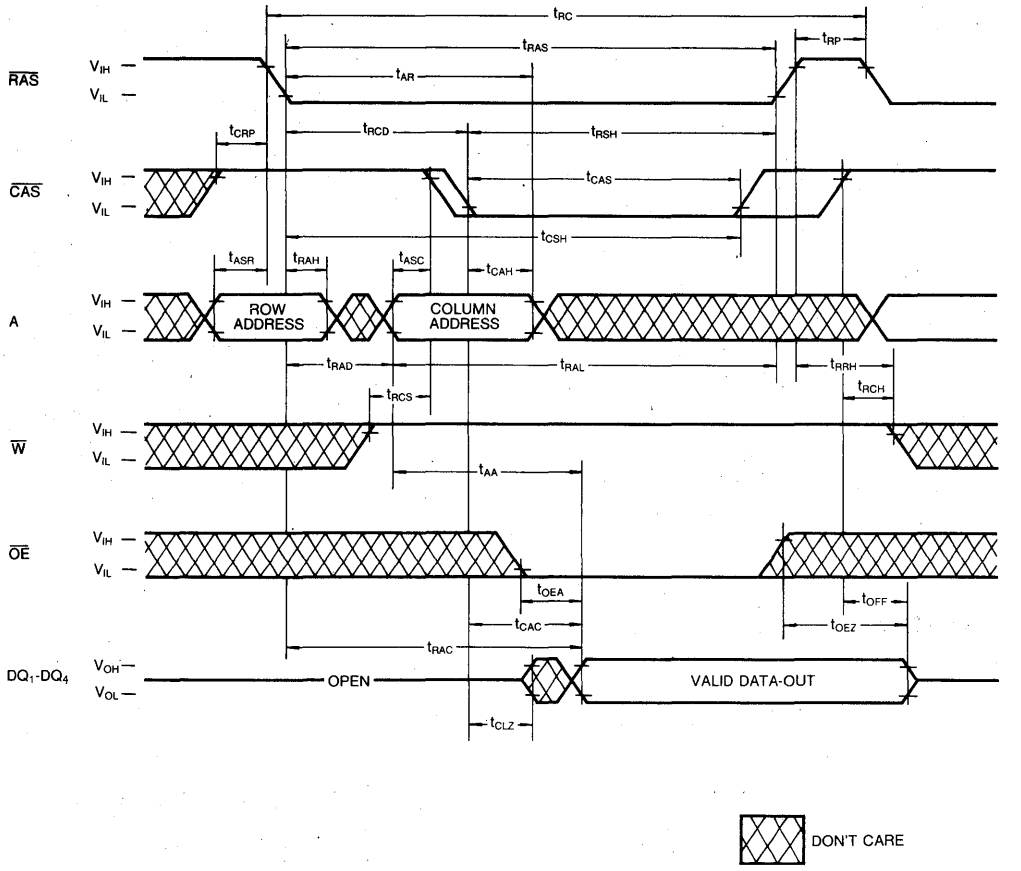
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

5

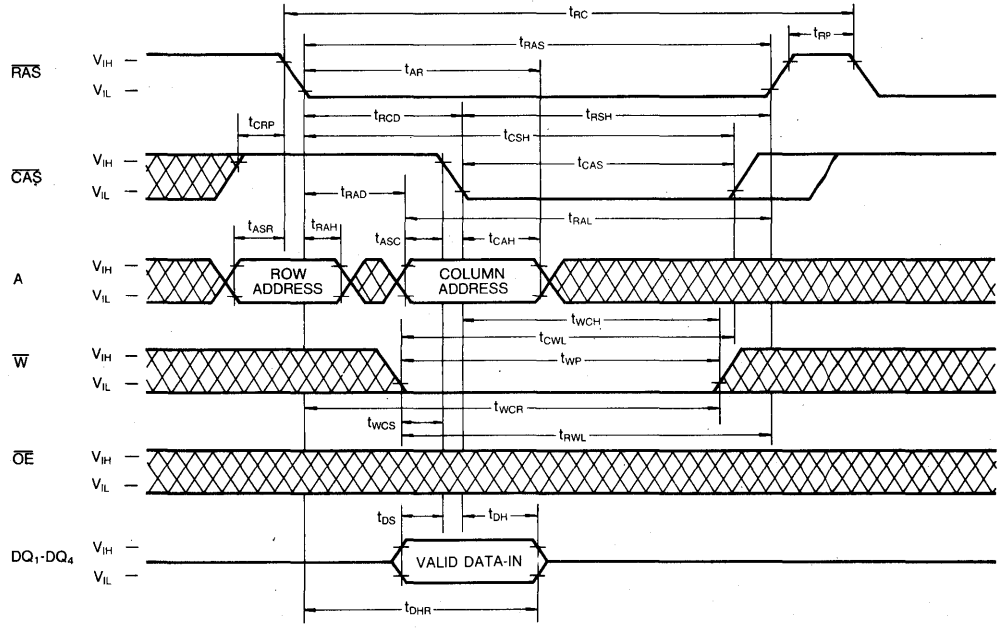
TIMING DIAGRAMS

READ CYCLE

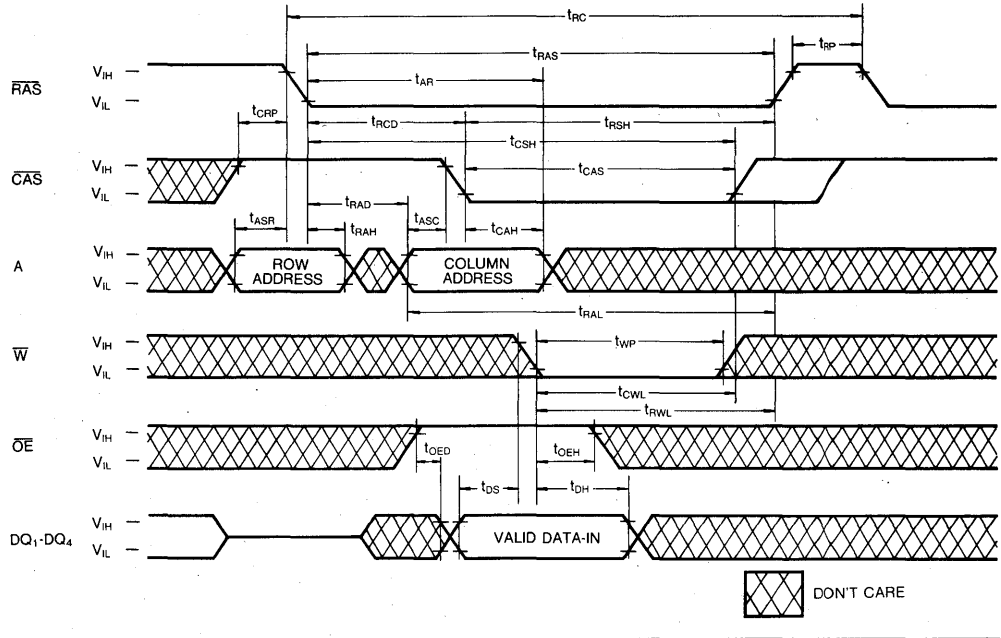


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



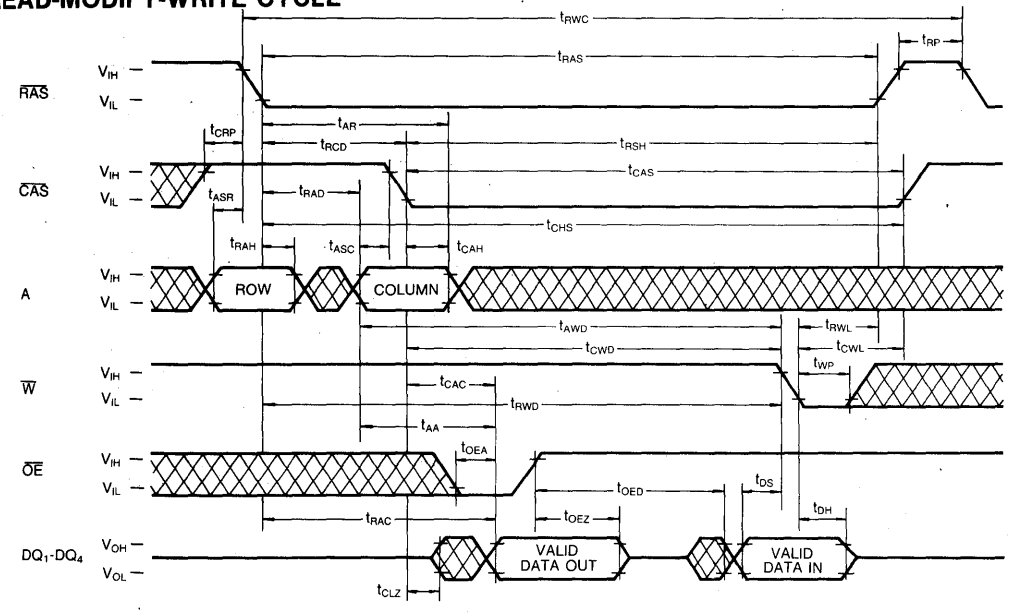
WRITE CYCLE (OE CONTROLLED WRITE)



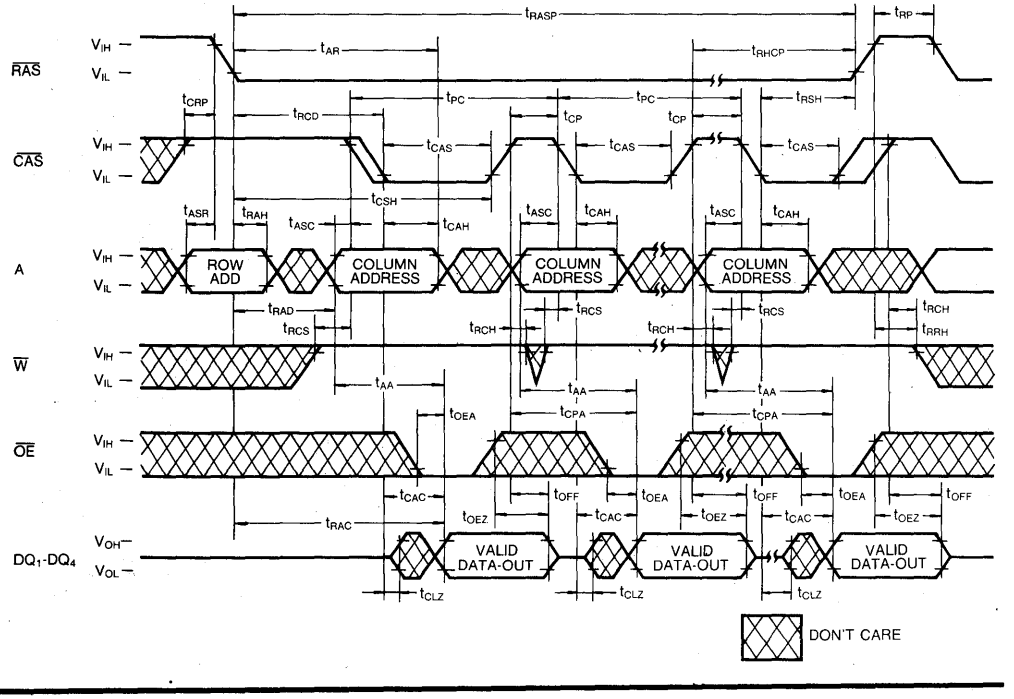
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



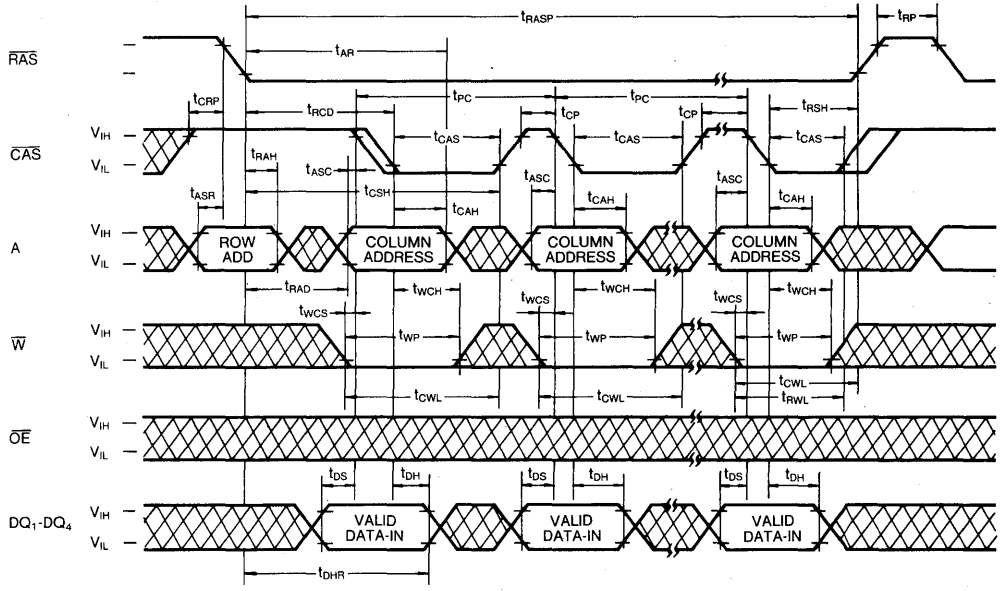
FAST PAGE MODE READ CYCLE



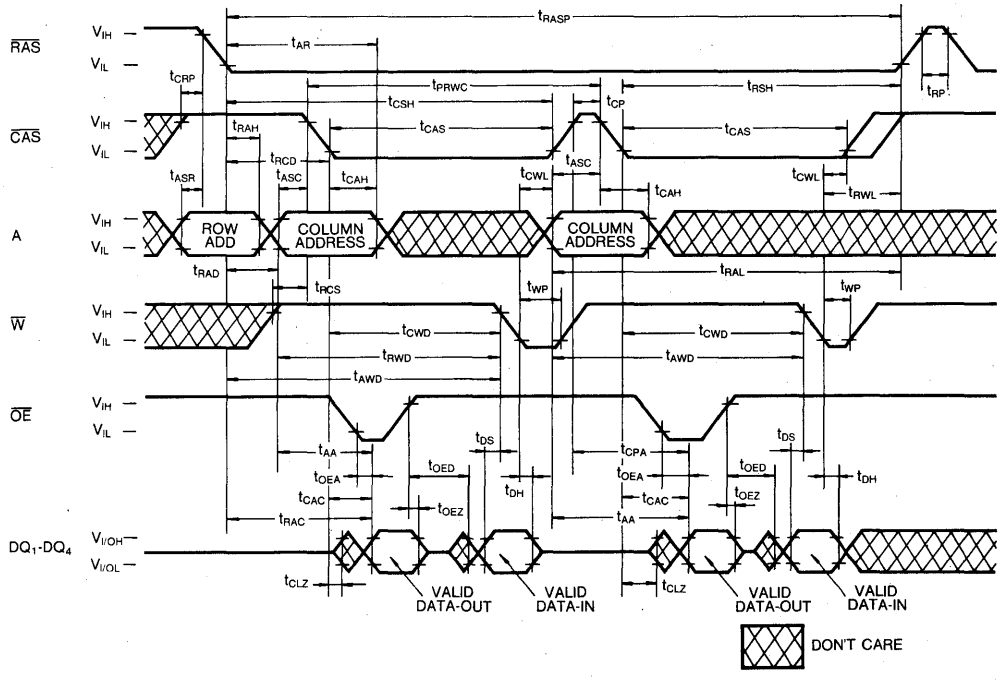
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



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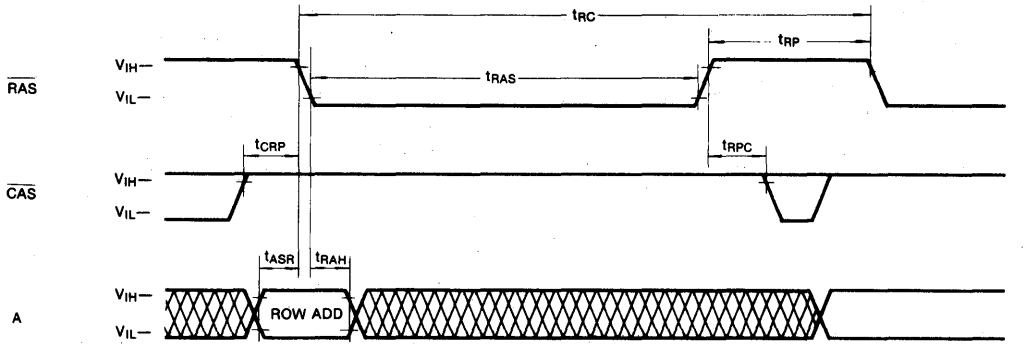
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

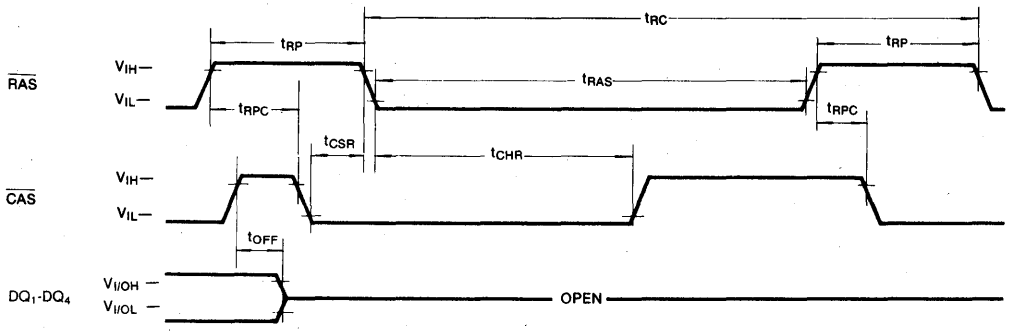
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



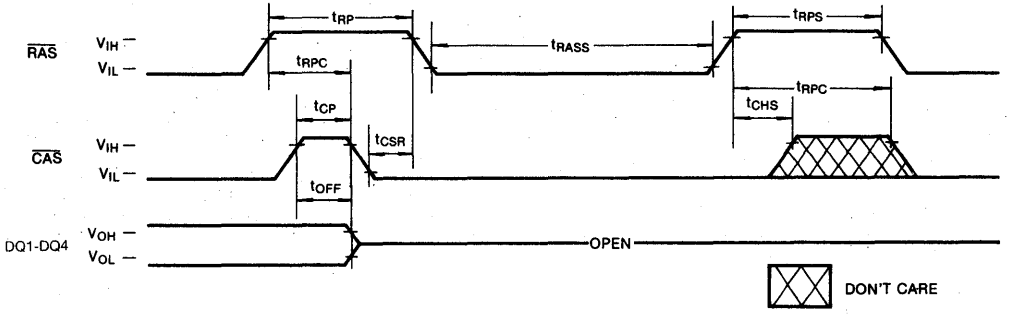
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



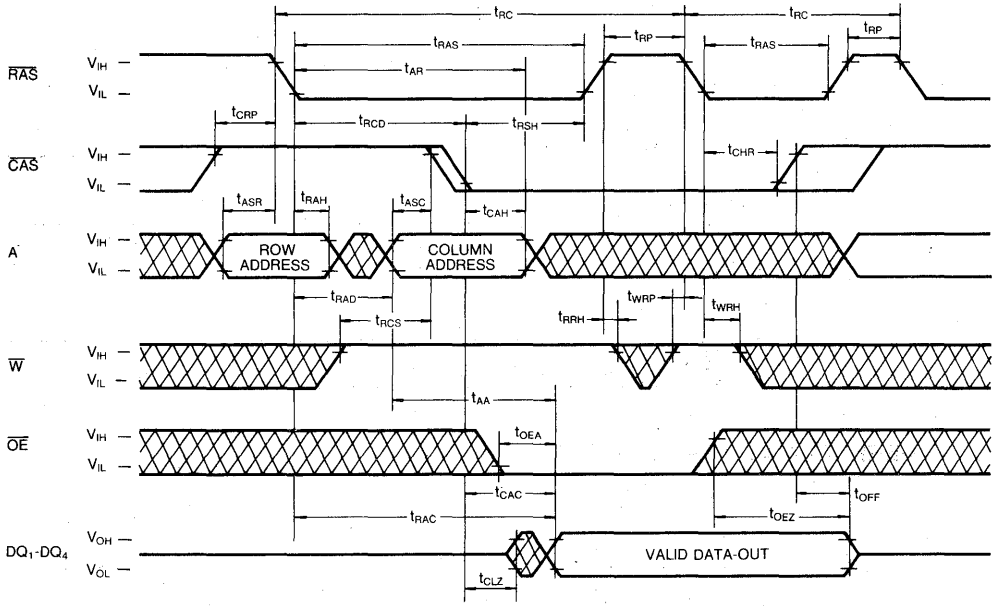
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

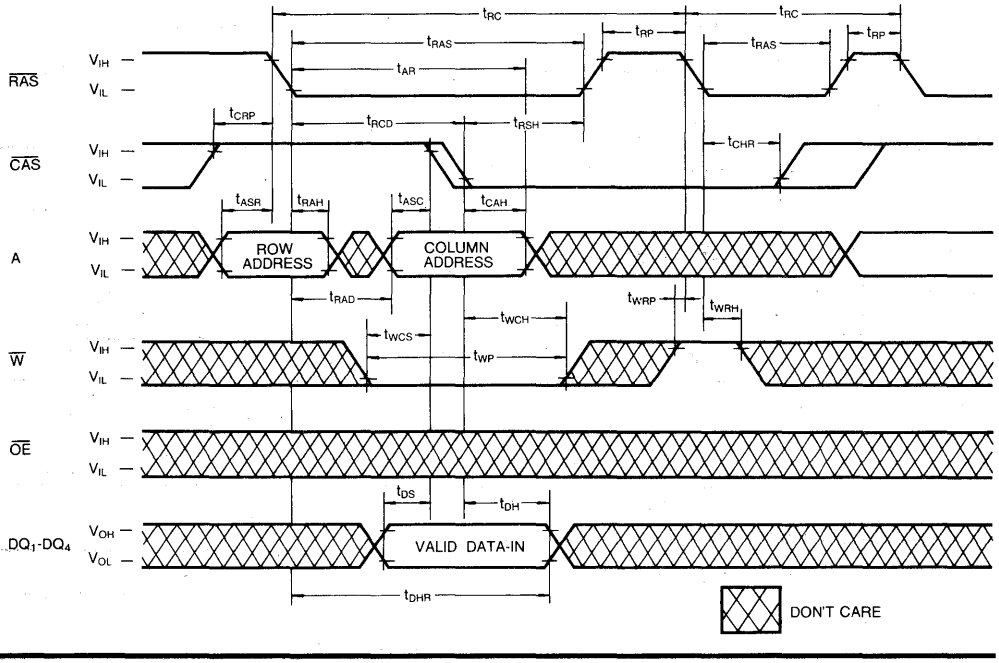


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

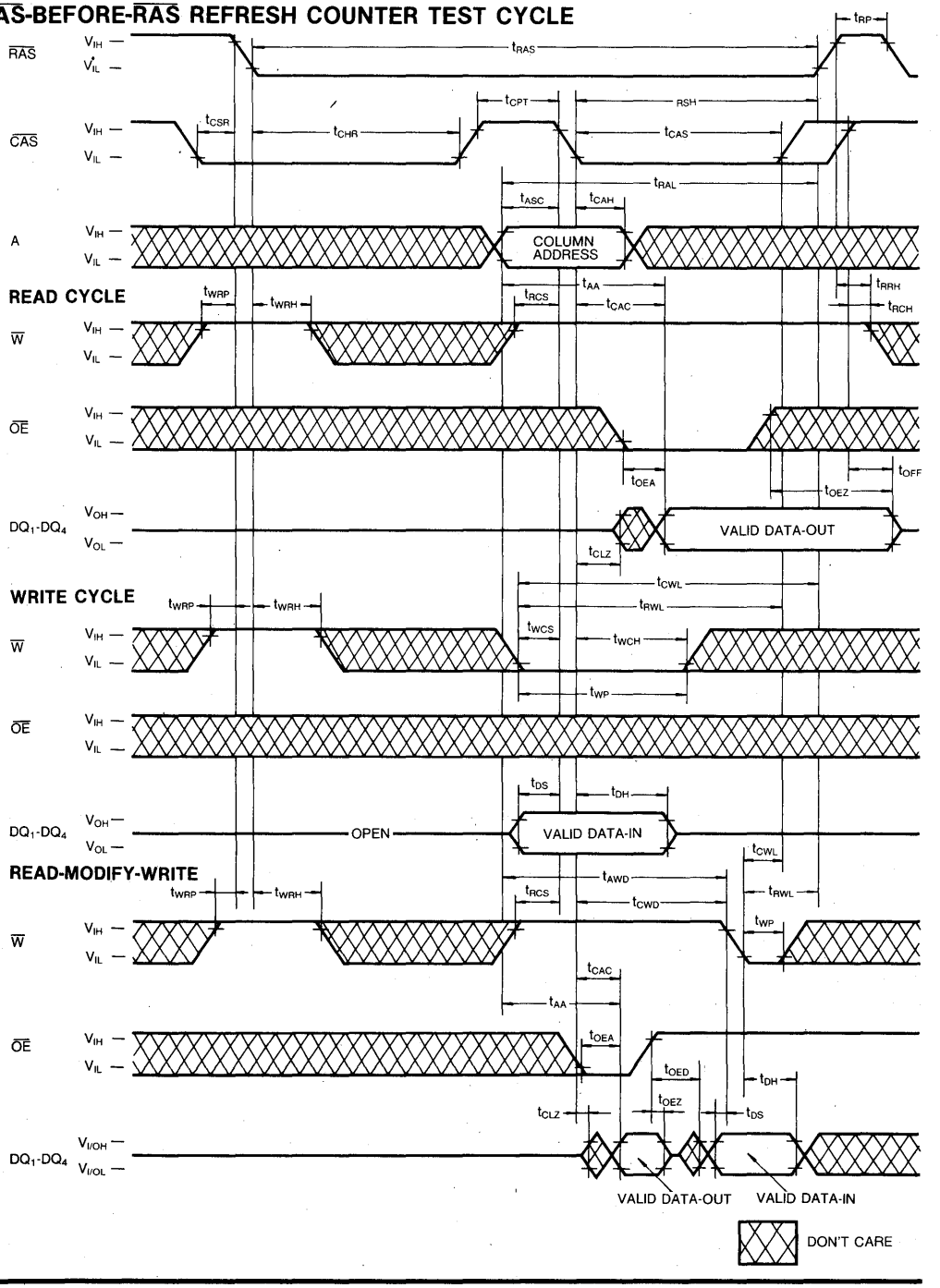


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

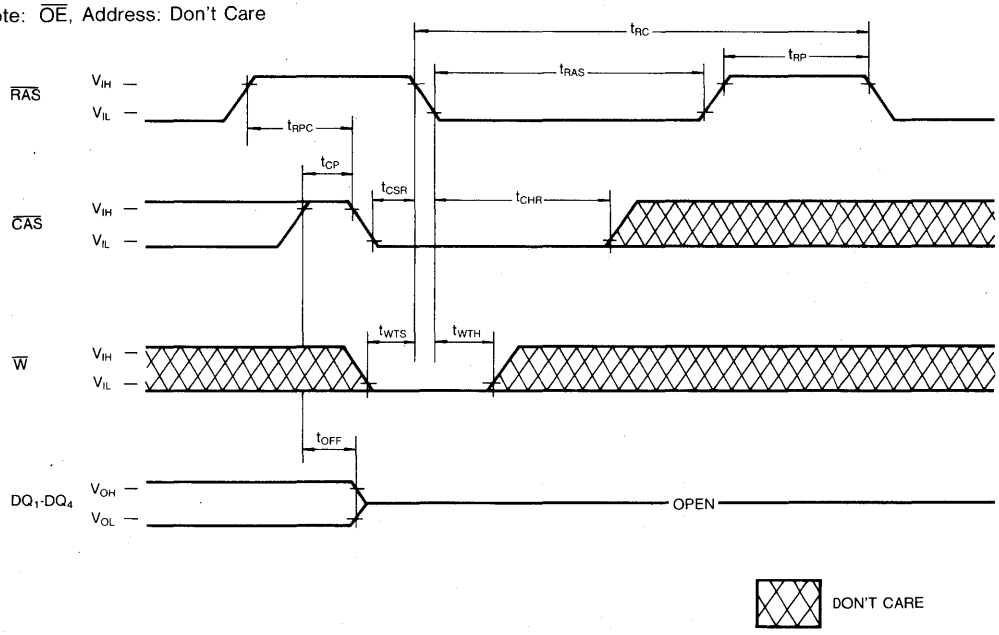
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



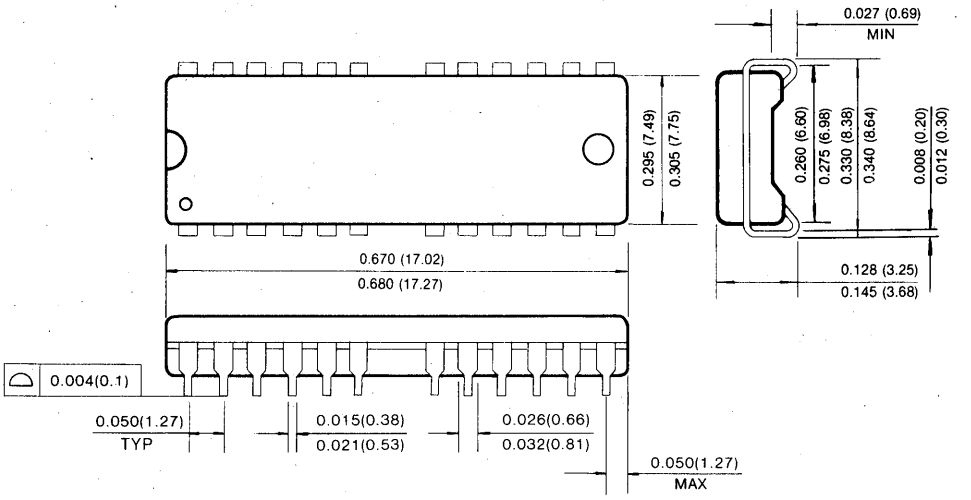
TEST MODE DESCRIPTION

The KM44C4000A/AL/ALL/ASL is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1, 048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 and A_1 are not used. If, upon reading, four bits on one D/Q pin are equal (all "1"s or "0"s) the D/Q pin indicates a "1". If they were not equal, the D/Q pin would indicate a "0". In "Test Mode", the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

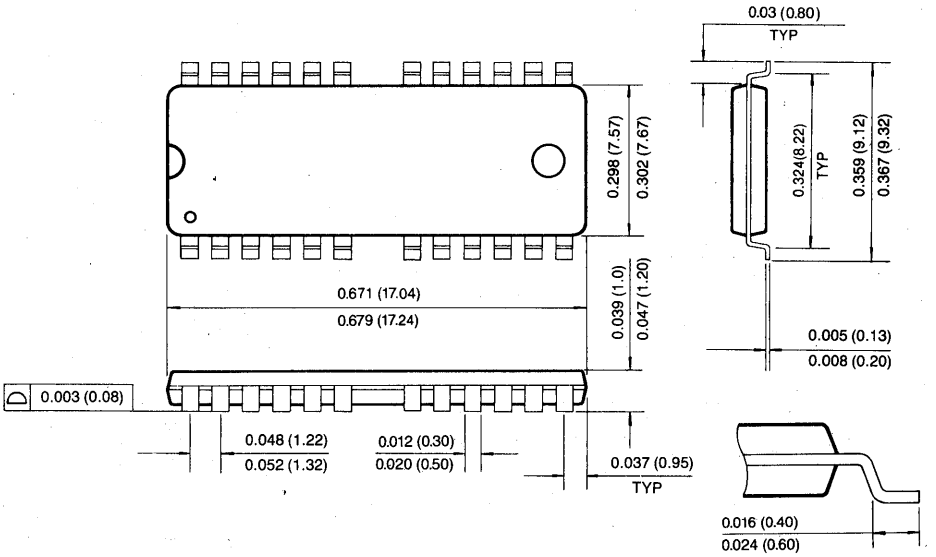
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



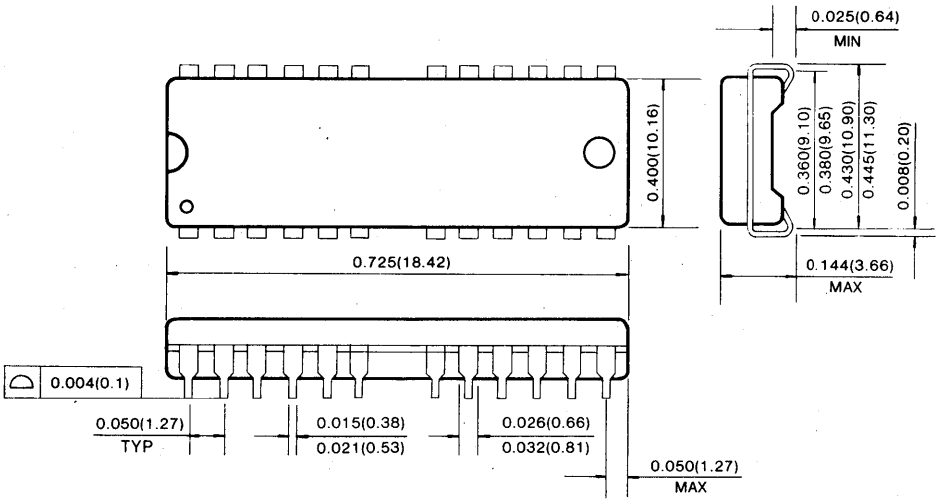
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



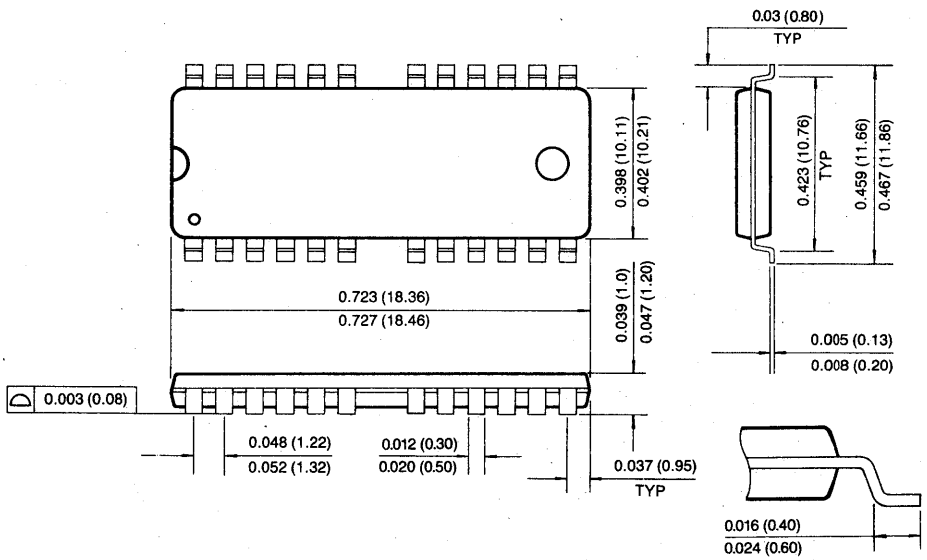
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



5

4M ×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM44C4100A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4100A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4100A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4100A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V±10% power supply**
- **2048 cycles/32ms refresh (Normal)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

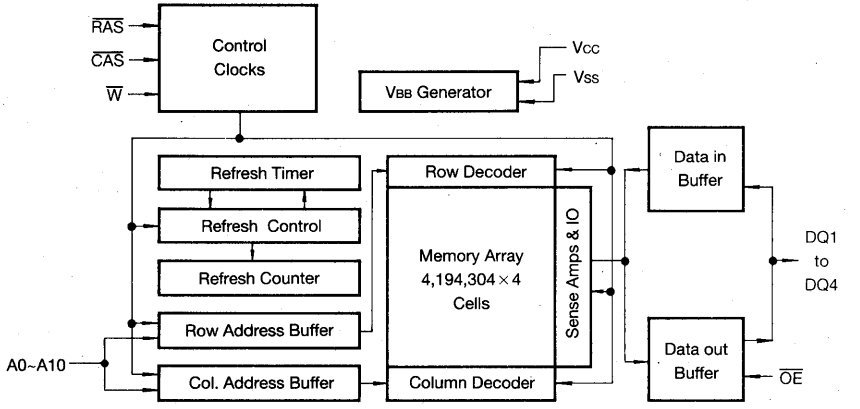
The Samsung KM44C4100A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4100A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

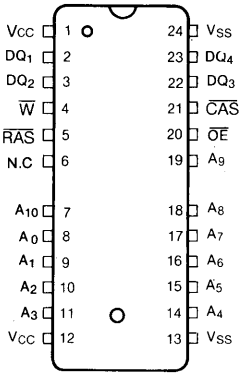
The KM44C4100A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



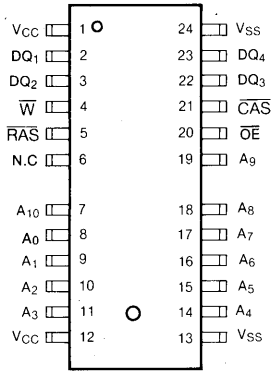
PIN CONFIGURATION (Top Views)

• **KM44C4100 AJ/ALJ/ALLJ/ASLJ**
AK/ALK/ALLK/ASLK



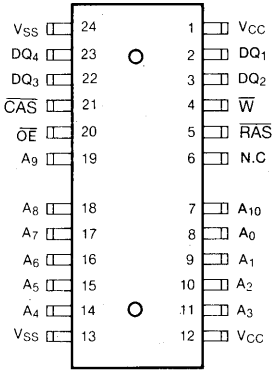
J : 400MIL
K : 300MIL

• **KM44C4100 AT/ALT/ALLT/ASLT**
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• **KM44C4100 ATR/ALTR/ALLTR/ASLTR**
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ1~4	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4100A/AL/ALL/ASL-5	I_{CC1}	-	110	mA
	KM44C4100A/AL/ALL/ASL-6			100	mA
	KM44C4100A/AL/ALL/ASL-7			90	mA
	KM44C4100A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44C4100A	I_{CC2}	-	2	mA
	KM44C4100AL			1	mA
	KM44C4100ALL			1	mA
	KM44C4100ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44C4100A/AL/ALL/ASL-5	I_{CC3}	-	110	mA
	KM44C4100A/AL/ALL/ASL-6			100	mA
	KM44C4100A/AL/ALL/ASL-7			90	mA
	KM44C4100A/AL/ALL/ASL-8			80	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44C4100A/AL/ALL/ASL-5	I_{CC4}	-	90	mA
	KM44C4100A/AL/ALL/ASL-6			80	mA
	KM44C4100A/AL/ALL/ASL-7			70	mA
	KM44C4100A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM44C4100A	I_{CC5}	-	1	mA
	KM44C4100AL			300	μA
	KM44C4100ALL			200	μA
	KM44C4100ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4100A/AL/ALL/ASL-5	I_{CC6}	-	110	mA
	KM44C4100A/AL/ALL/ASL-6			100	mA
	KM44C4100A/AL/ALL/ASL-7			90	mA
	KM44C4100A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=62.5μS(L-Ver.) 125μS(SL-Ver.), T_{RAS}≤min~300ns	KM44C4100AL	I_{CC7}	-	400	μA
	KM44C4100ASL			300	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{10}=V_{CC}-0.2V or 0.2V DQ_1-DQ_4=V_{CC}-0.2V, 0.2V or Open	KM44C4100ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25 C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{10})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		32		32		32		32	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	76		85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ pulse width(Fast Page mode)	t_{RASP}	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		13		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	13		15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

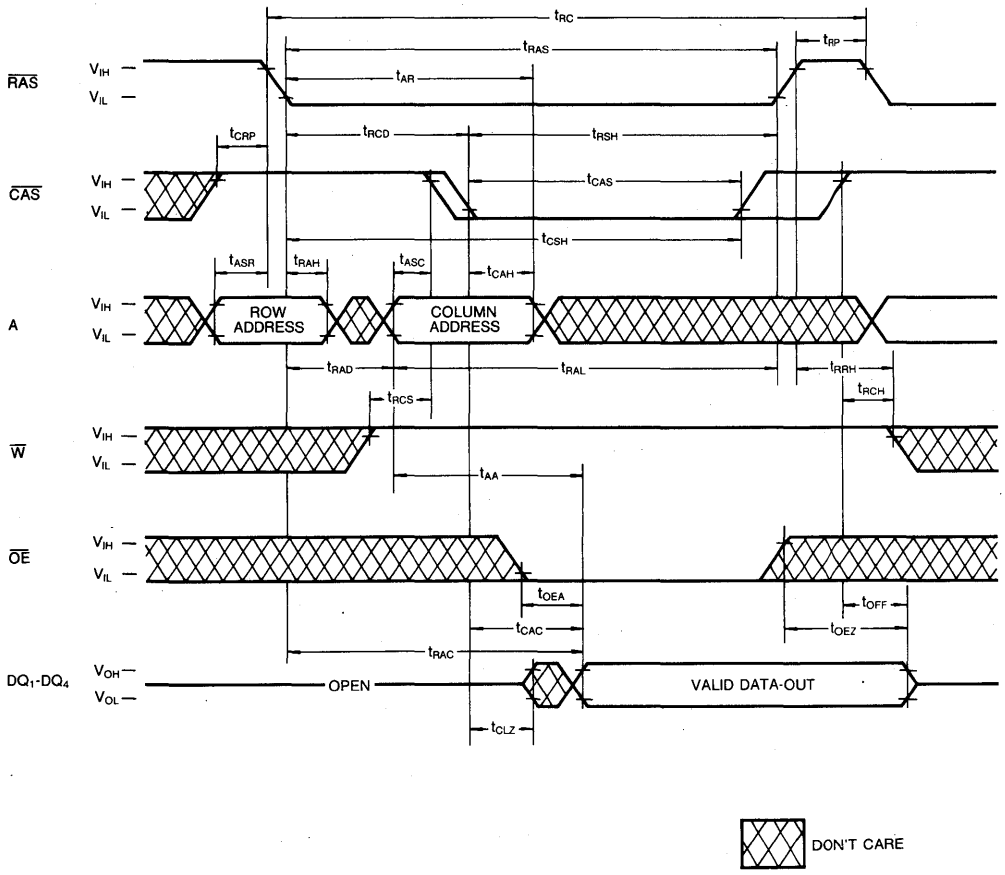
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

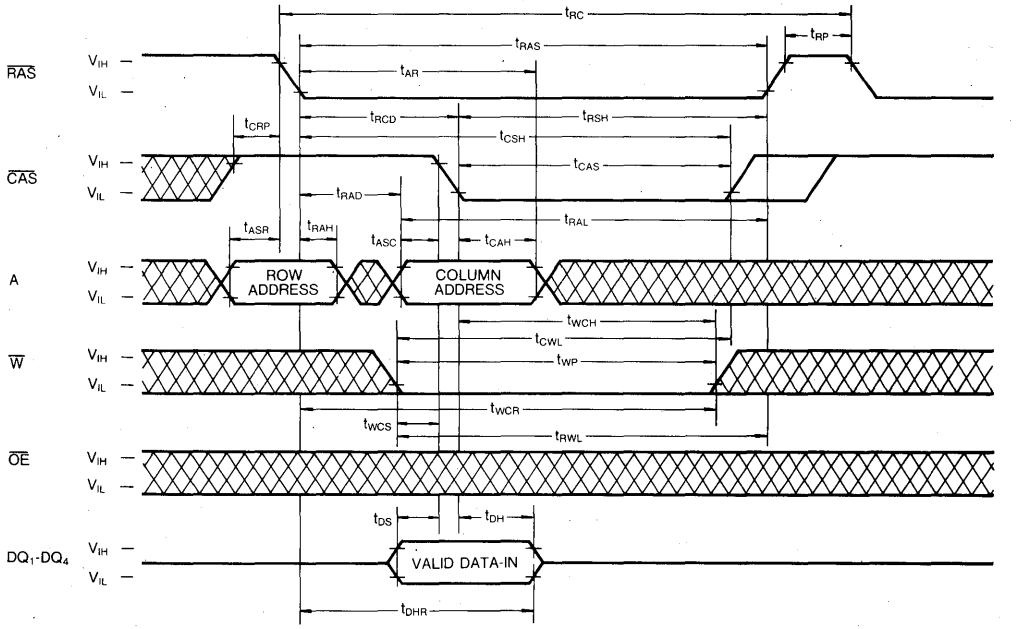
TIMING DIAGRAMS

READ CYCLE

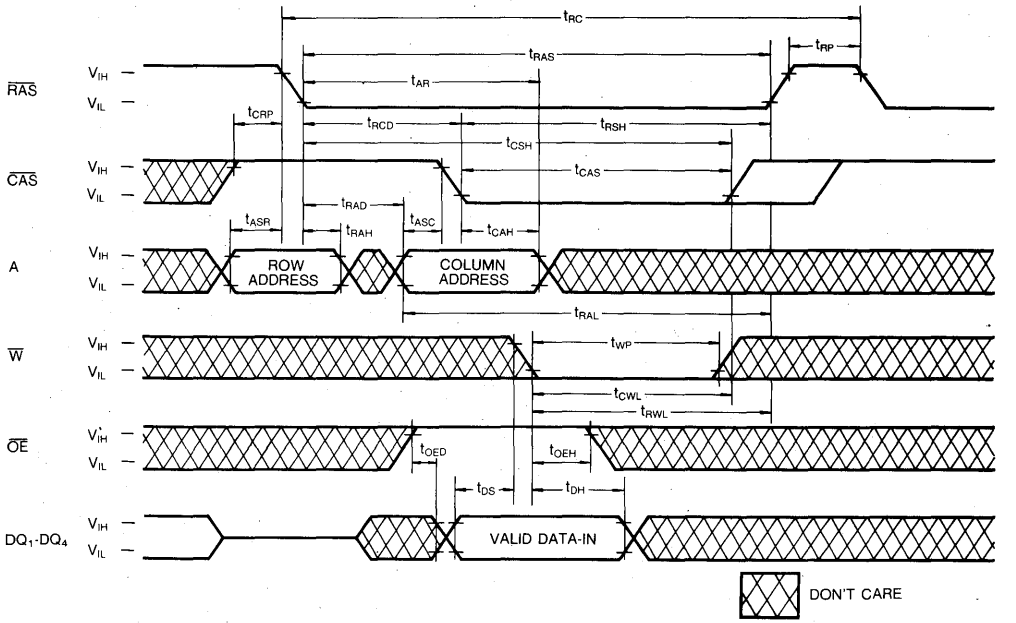


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)

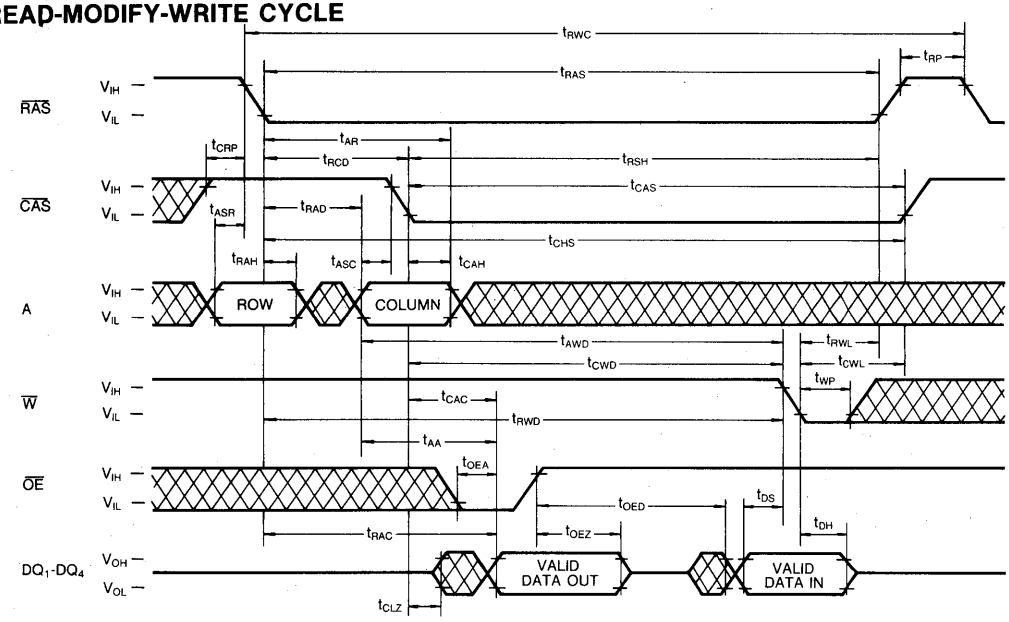


WRITE CYCLE (OE CONTROLLED WRITE)

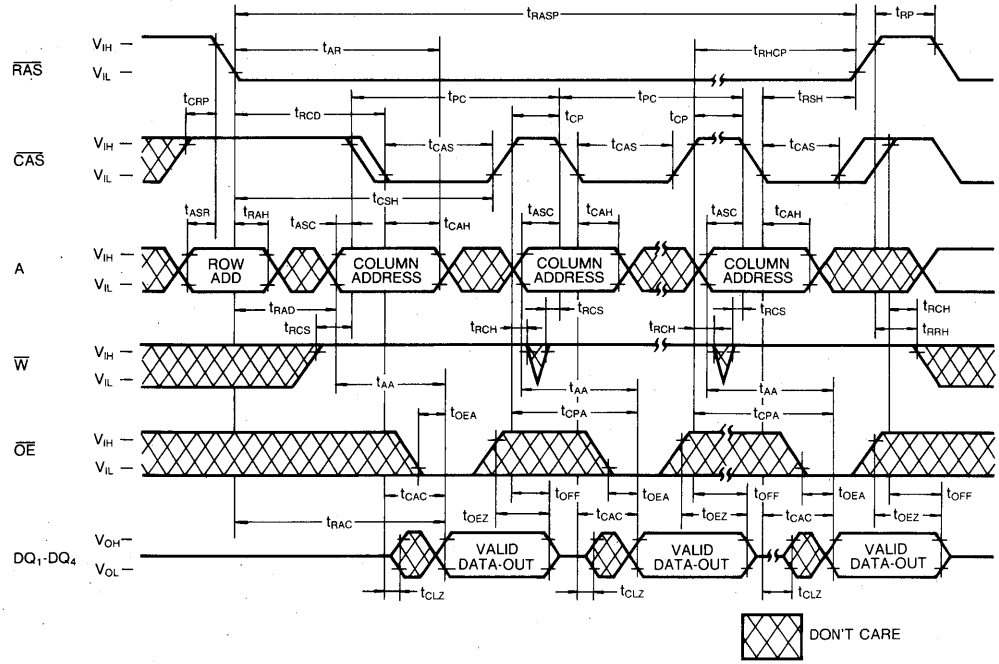


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



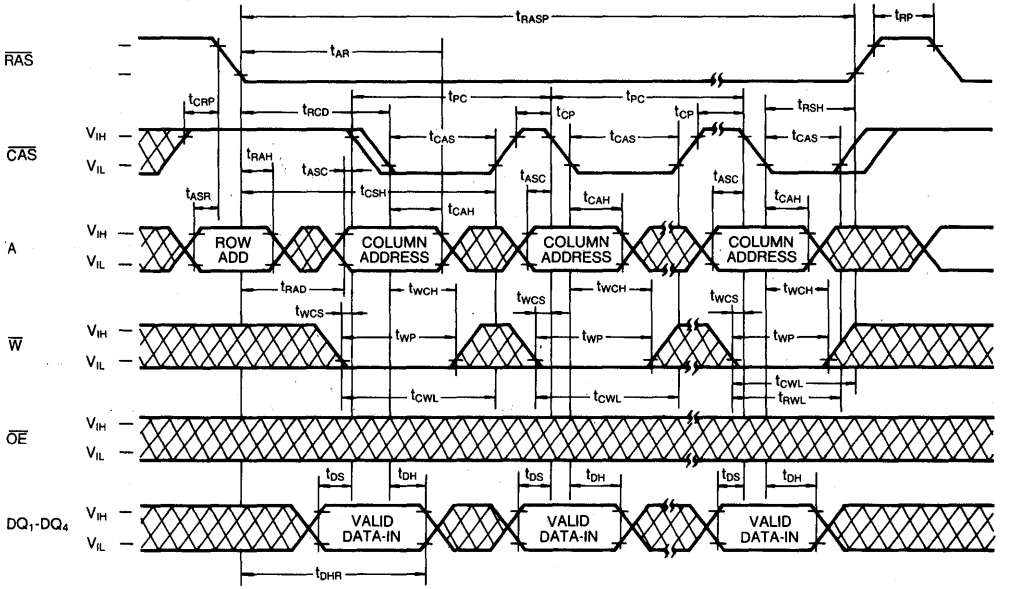
FAST PAGE MODE READ CYCLE



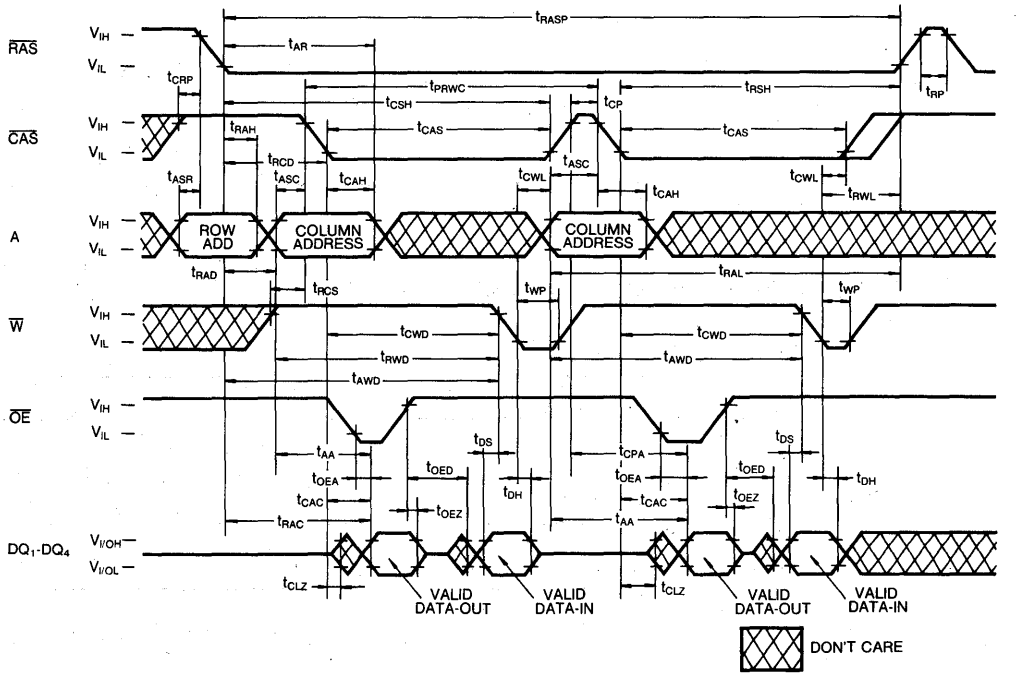
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



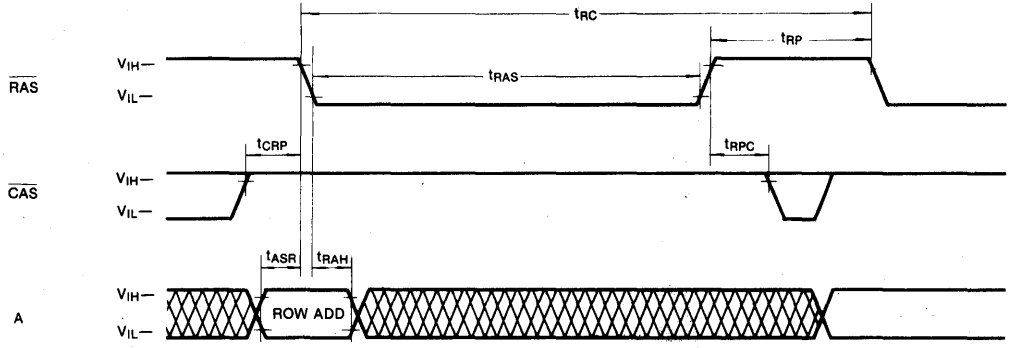
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

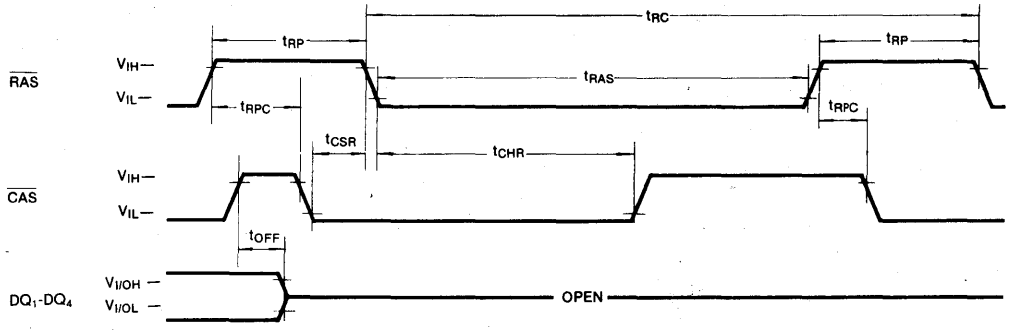
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



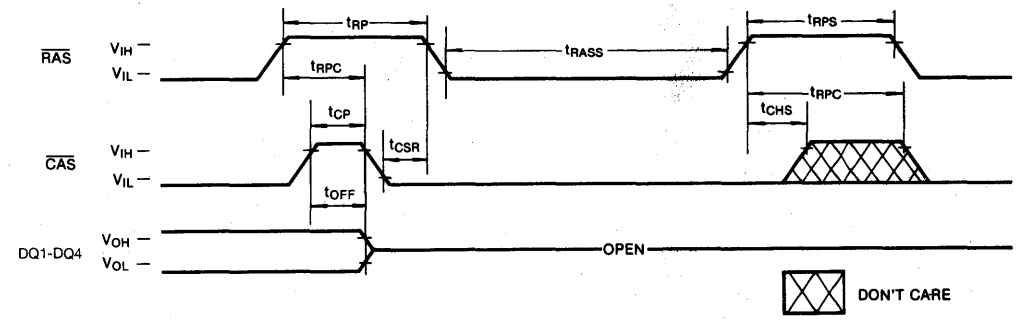
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



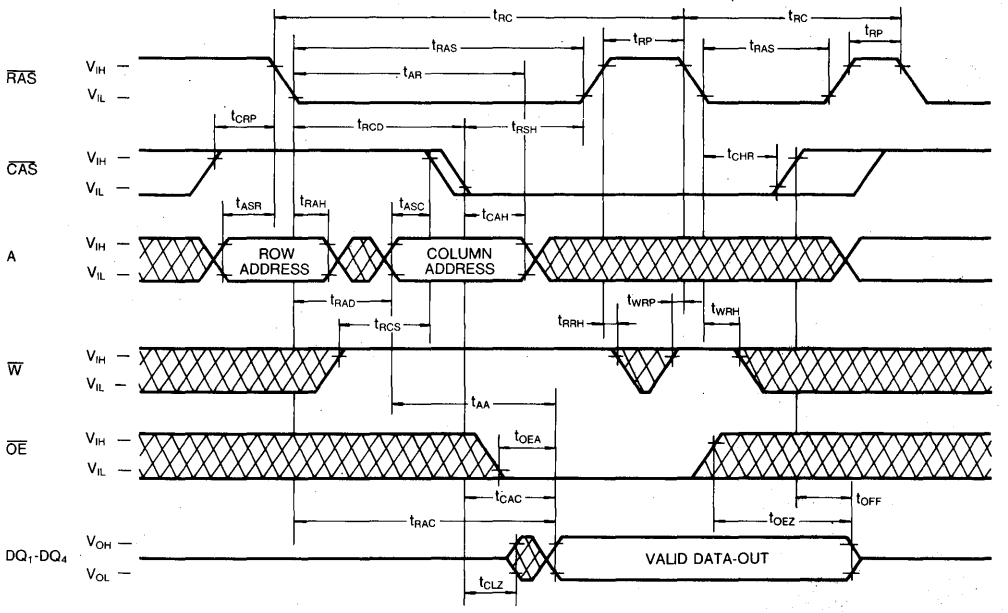
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

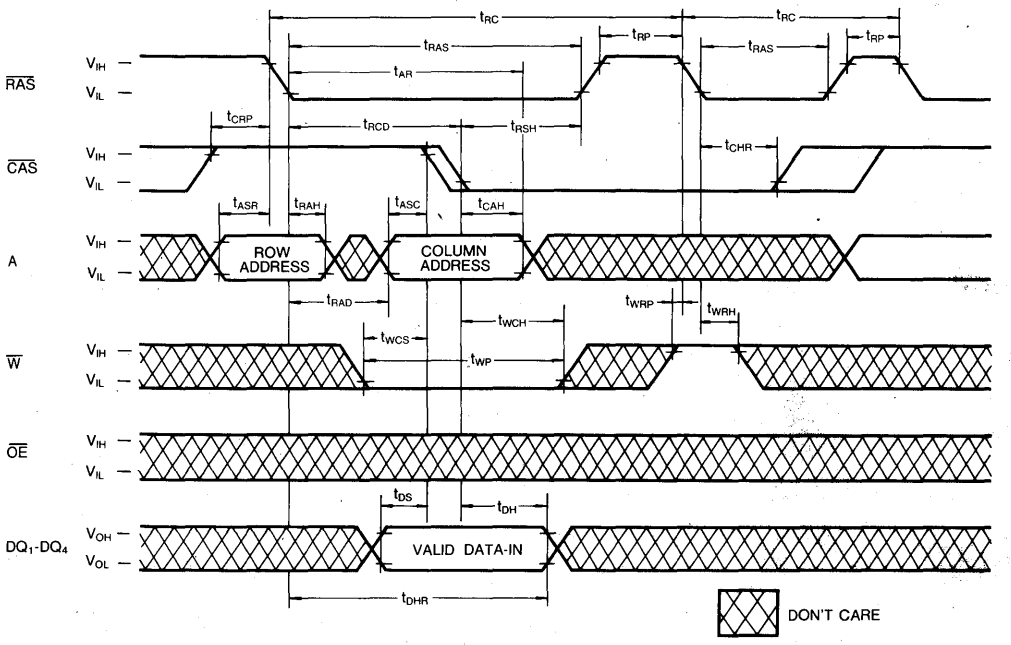


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



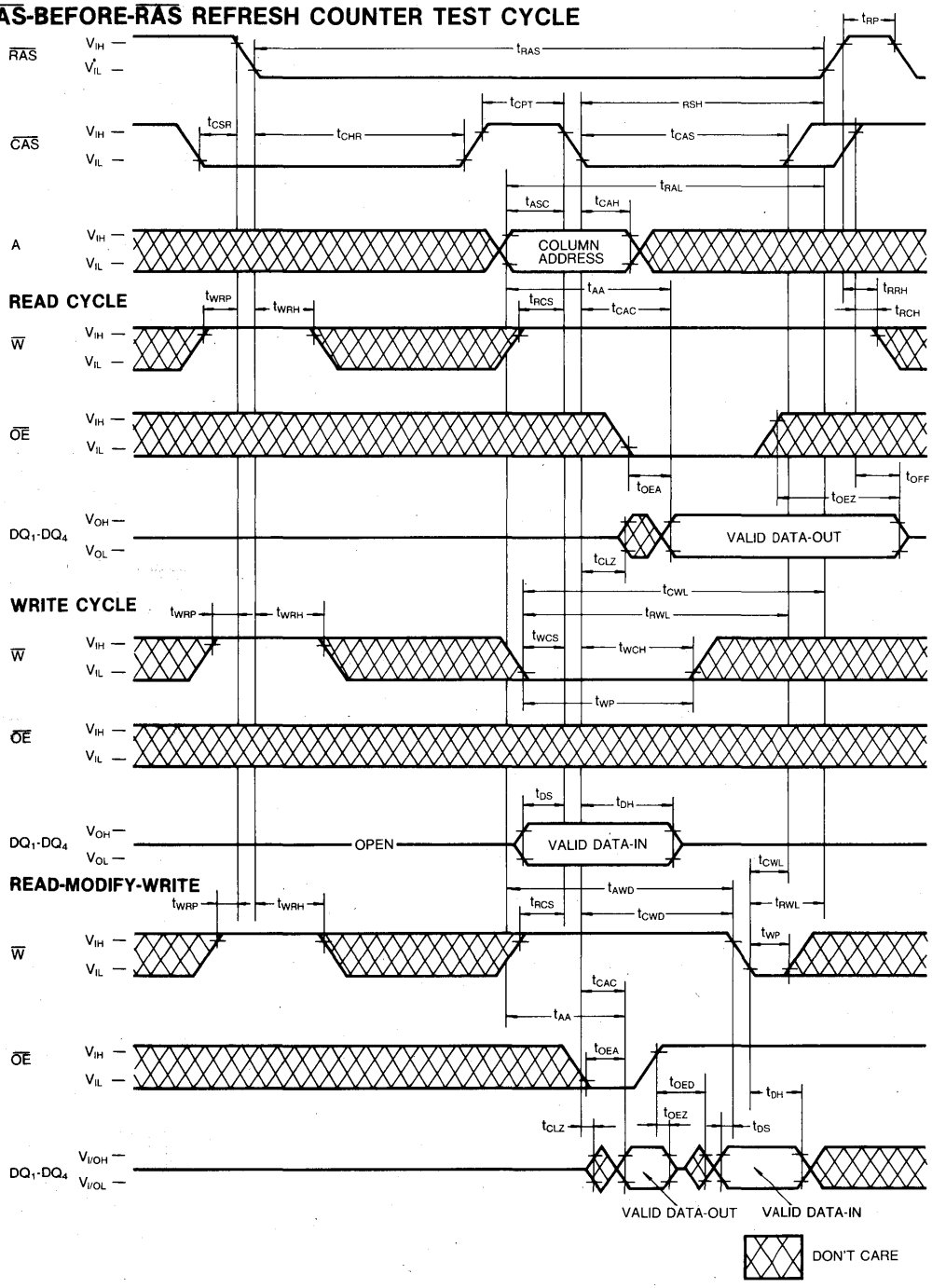
HIDDEN REFRESH CYCLE (WRITE)



SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



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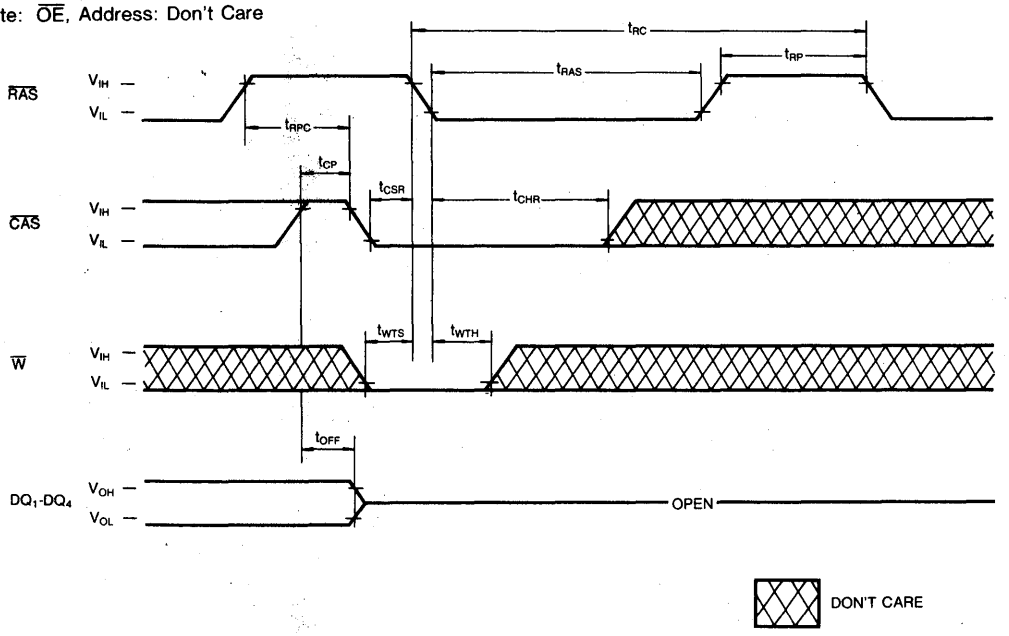
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



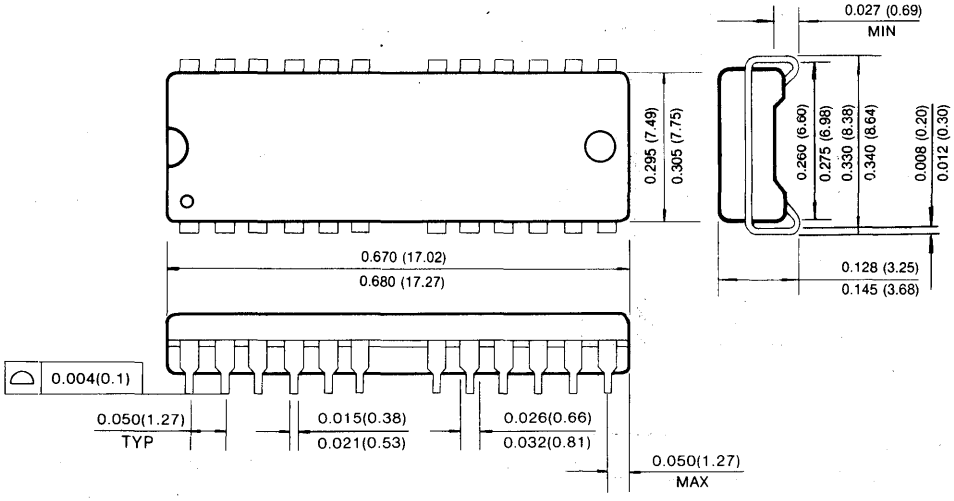
TEST MODE DESCRIPTION

The KM44C4100A/AL/ALL/ASL is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1, 048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 and A_1 are not used. If, upon reading, four bits on one D/Q pin are equal (all "1"s or "0"s) the D/Q pin indicates a "1". If they were not equal, the D/Q pin would indicate a "0". In "Test Mode", the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

PACKAGE DIMENSIONS

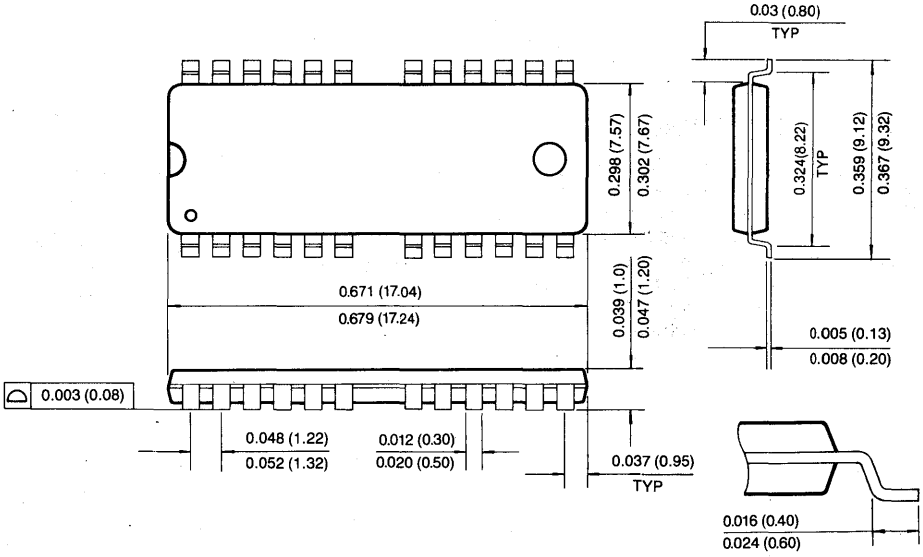
24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



5

24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

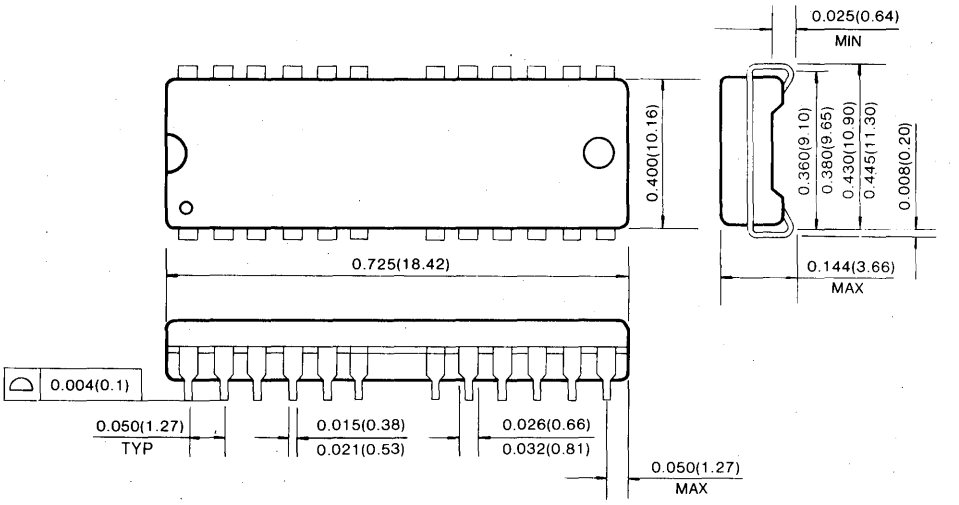


SAMSUNG ELECTRONICS

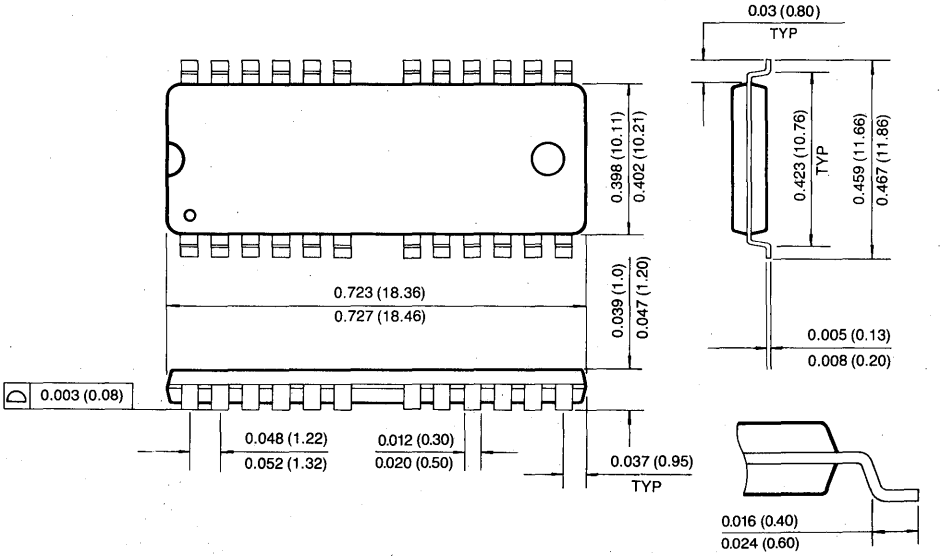
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M ×4 Bit CMOS Dynamic RAM with Fast Page Mode (Write Per Bit Mode)

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM44C4010A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4010A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4010A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4010A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Self Refresh Operation (LL-ver. only)**
- **Write Per bit Mode capability**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V±10% power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

The Samsung KM44C4010A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

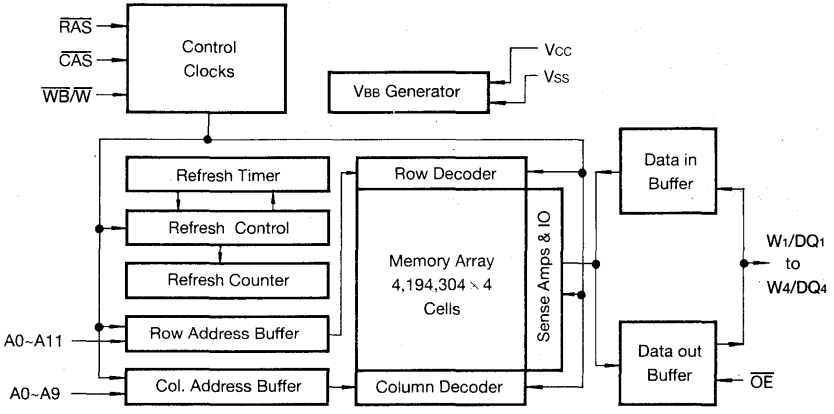
The KM44C4010A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C4010A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

5

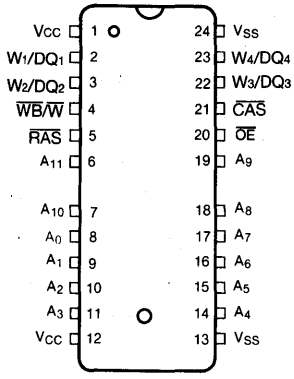
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

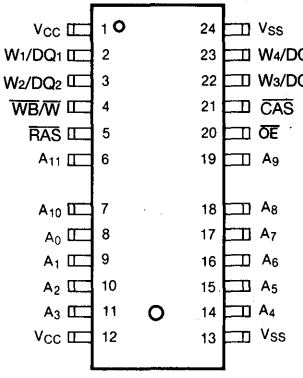
PIN CONFIGURATION (Top Views)

• **KM44C4010 AJ/ALJ/ALLJ/ASLJ**
AK/ALK/ALLK/ASLK



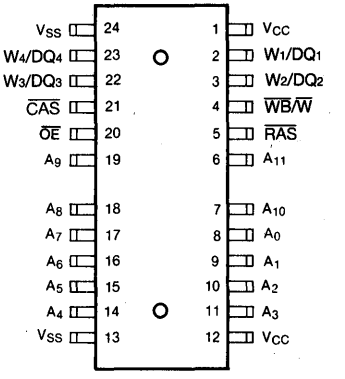
J : 400MIL
K : 300MIL

• **KM44C4010 AT/ALT/ALLT/ASLT**
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S: 300MIL(Forward)

• **KM44C4010 ATR/ALTR/ALLTR/ASLTR**
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
W1/DQ1~W4/DQ4	Write Select/Data in, out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB/W}$	Write Per Bit/Read/Write input
$\overline{OE}$	Data Output Enable
VCC	Power(+5.0V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4010A/AL/ALL/ASL-5	I_{CC1}	-	90	mA
	KM44C4010A/AL/ALL/ASL-6			80	mA
	KM44C4010A/AL/ALL/ASL-7			70	mA
	KM44C4010A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{WB}$/$\overline{W}$=V_{IH})	KM44C4010A	I_{CC2}	-	2	mA
	KM44C4010AL			1	mA
	KM44C4010ALL			1	mA
	KM44C4010ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44C4010A/AL/ALL/ASL-5	I_{CC3}	-	90	mA
	KM44C4010A/AL/ALL/ASL-6			80	mA
	KM44C4010A/AL/ALL/ASL-7			70	mA
	KM44C4010A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44C4010A/AL/ALL/ASL-5	I_{CC4}	-	80	mA
	KM44C4010A/AL/ALL/ASL-6			70	mA
	KM44C4010A/AL/ALL/ASL-7			60	mA
	KM44C4010A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{WB}$/$\overline{W}$=V_{CC}-0.2V)	KM44C4010A	I_{CC5}	-	1	mA
	KM44C4010AL			300	μA
	KM44C4010ALL			200	μA
	KM44C4010ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4010A/AL/ALL/ASL-5	I_{CC6}	-	90	mA
	KM44C4010A/AL/ALL/ASL-6			80	mA
	KM44C4010A/AL/ALL/ASL-7			70	mA
	KM44C4010A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V W_1/DQ_1~W_4/DQ_4=Don't Care t_{RC}=31.25μs(L-Ver.) 62.5μs(SL-Ver.), t_{RAS}=t_{RAS} min~300ns	KM44C4010AL	I_{CC7}	-	450	μA
	KM44C4010ASL			350	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{WB}$/$\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{CC}-0.2V or 0.2V W_1/DQ_1-W_4/DQ_4=V_{CC}-0.2V, 0.2V or Open	KM44C4010ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		I_{OL}	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}$/$\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (W_1/DQ_1~W_4/DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64		64	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	76		85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ pulse width(Fast Page mode)	t_{RASP}	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		13		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	13		15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	15
Write per bit set-up time	tWBS	0		0		0		0		ns	
Write per bit hold time	tWBH	10		10		10		10		ns	
Write selection set-up time	tWDS	0		0		0		0		ns	
Write per bit selection hold time	tWDH	10		10		10		10		ns	

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

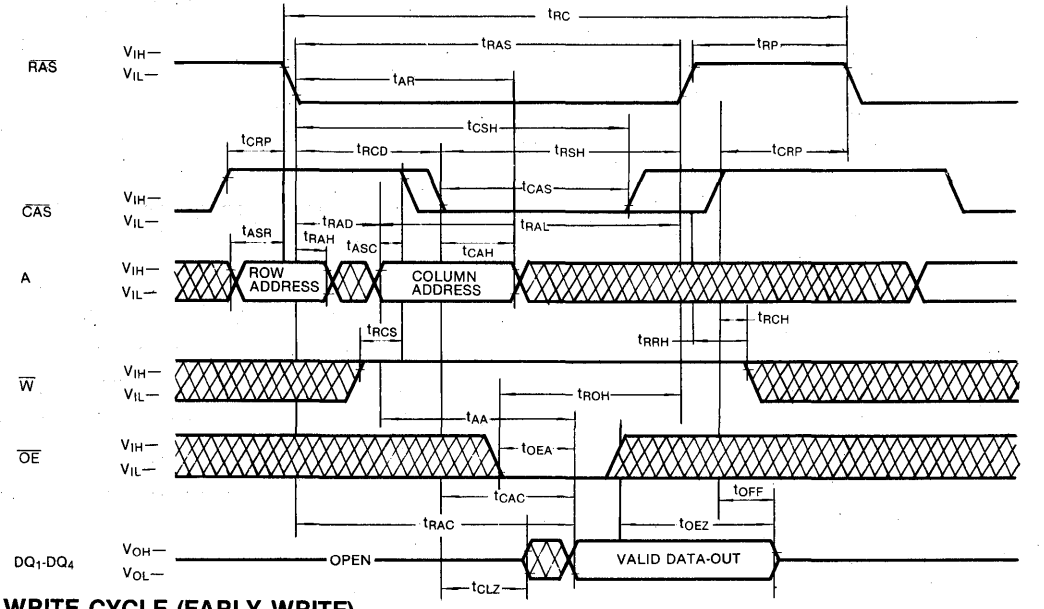
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data output is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

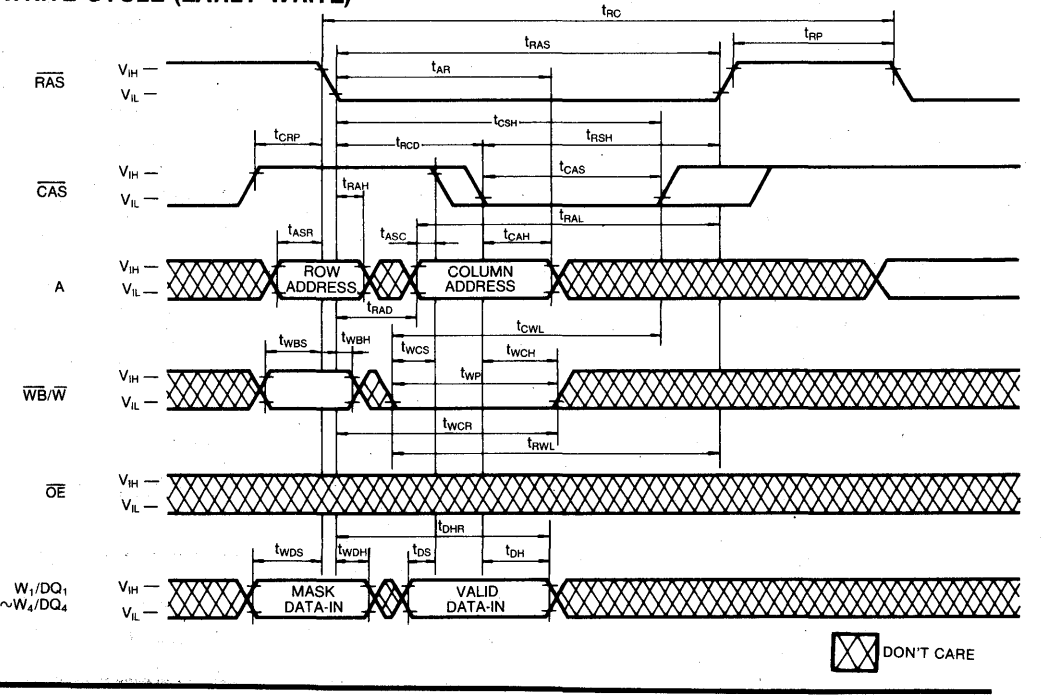
5

TIMING DIAGRAMS

READ CYCLE

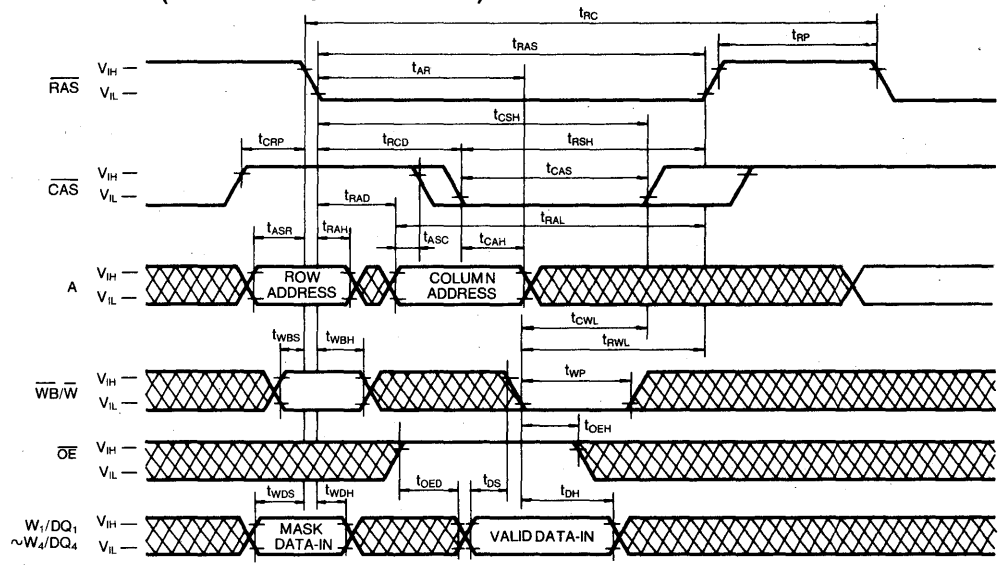


WRITE CYCLE (EARLY WRITE)

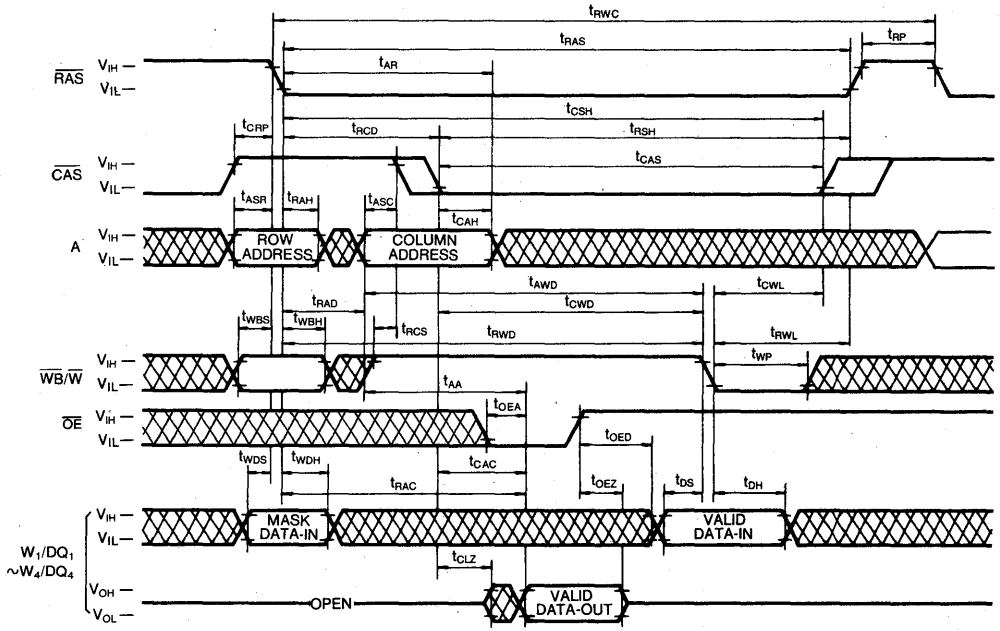


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

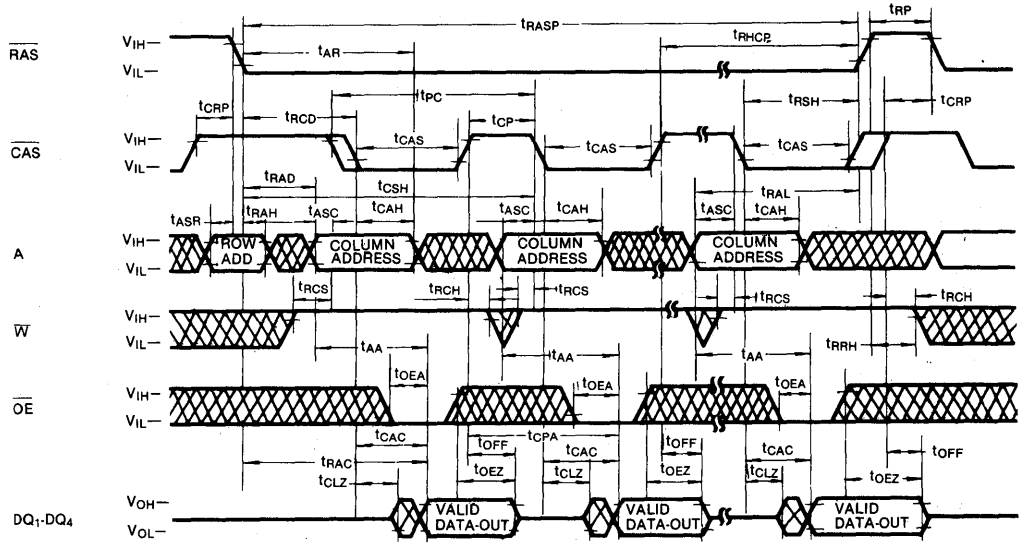


READ-MODIFY-WRITE CYCLE

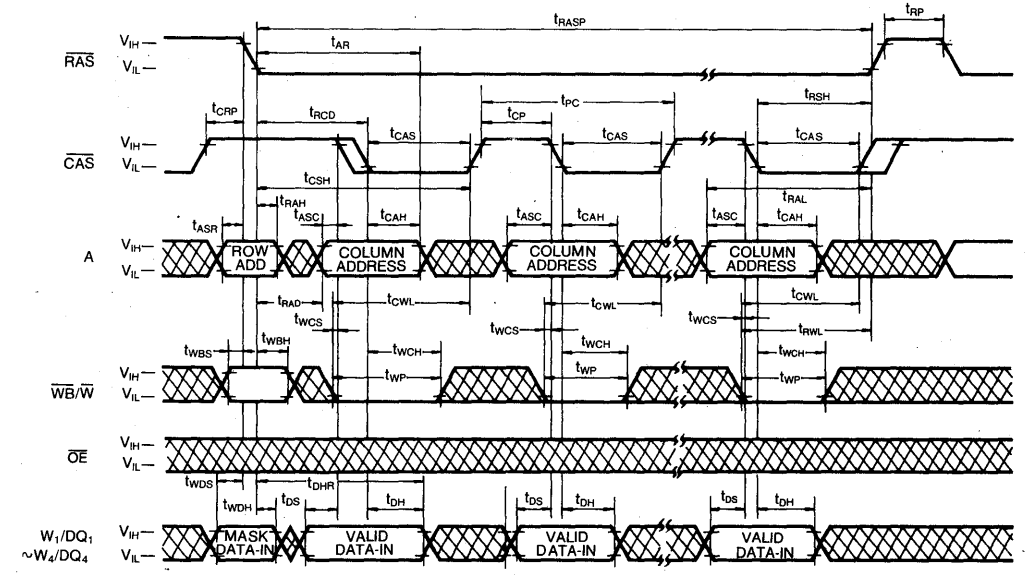


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

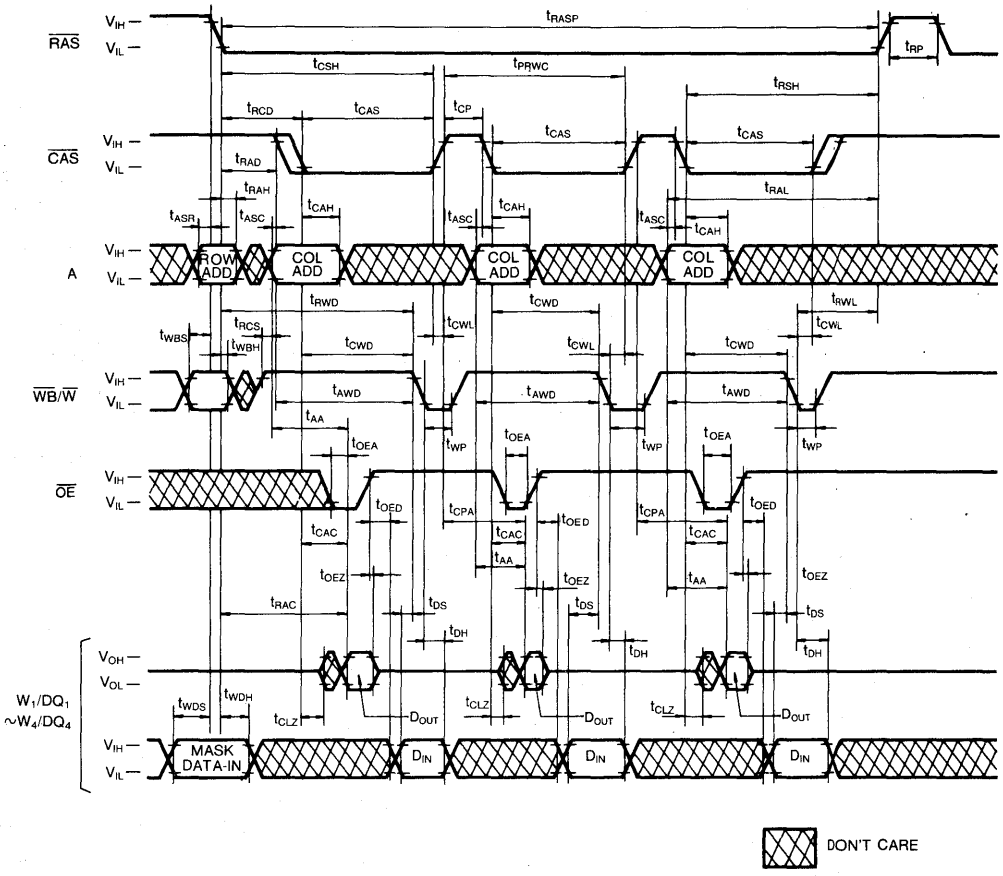


DON'T CARE

SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

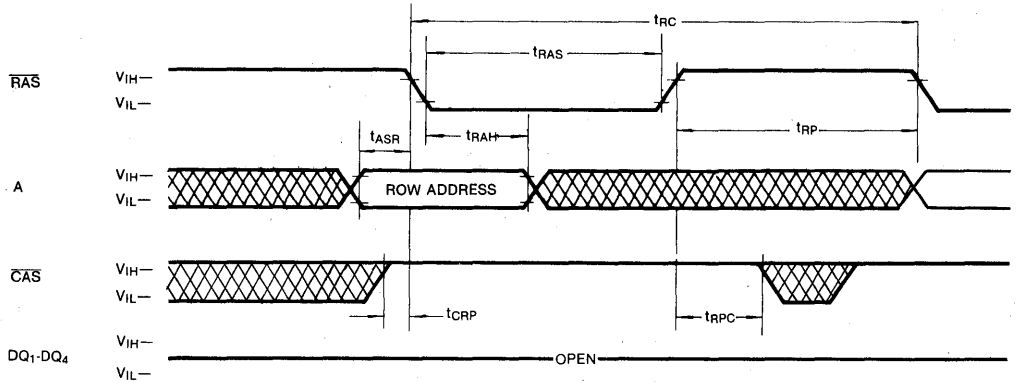


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

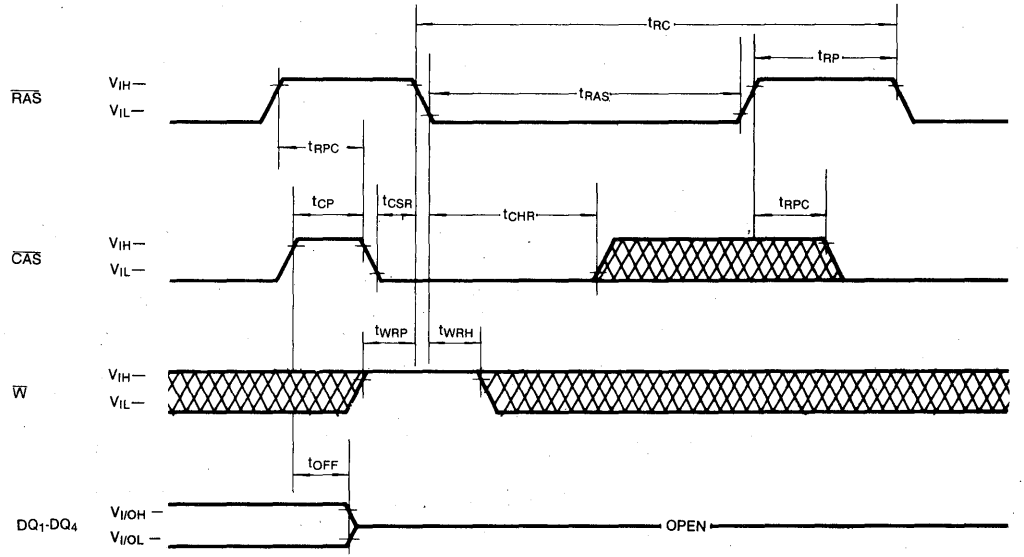
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



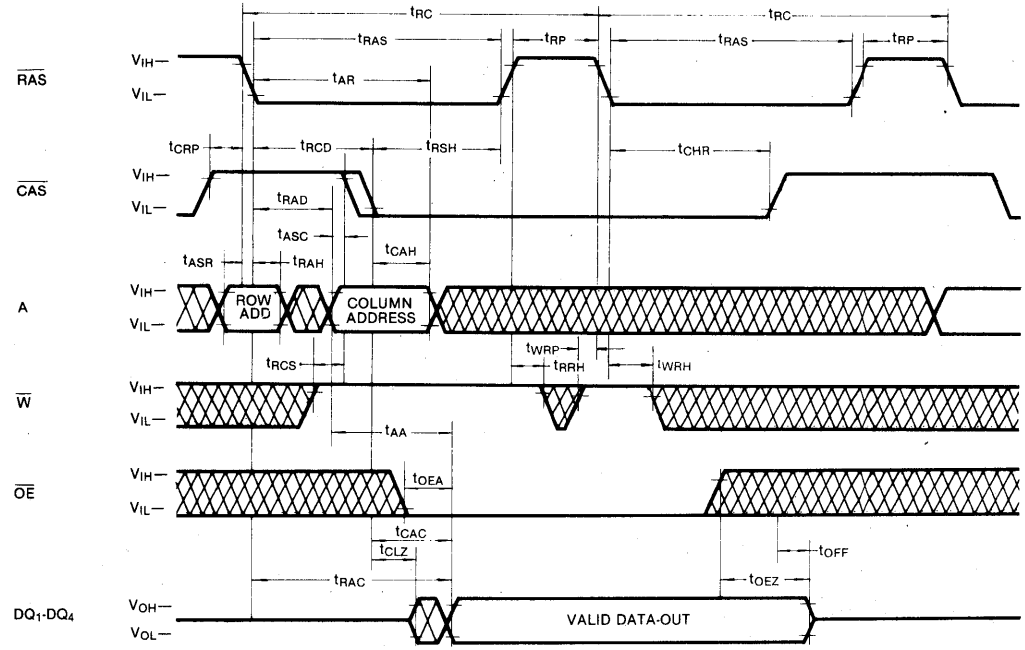
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{OE}$, Address = Don't Care

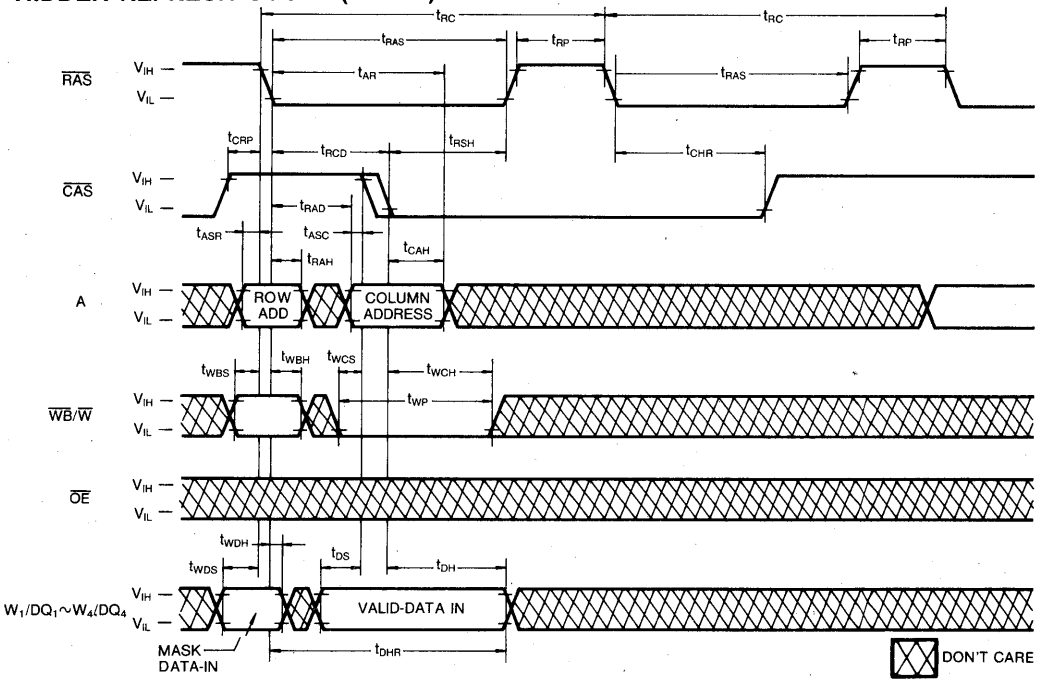


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



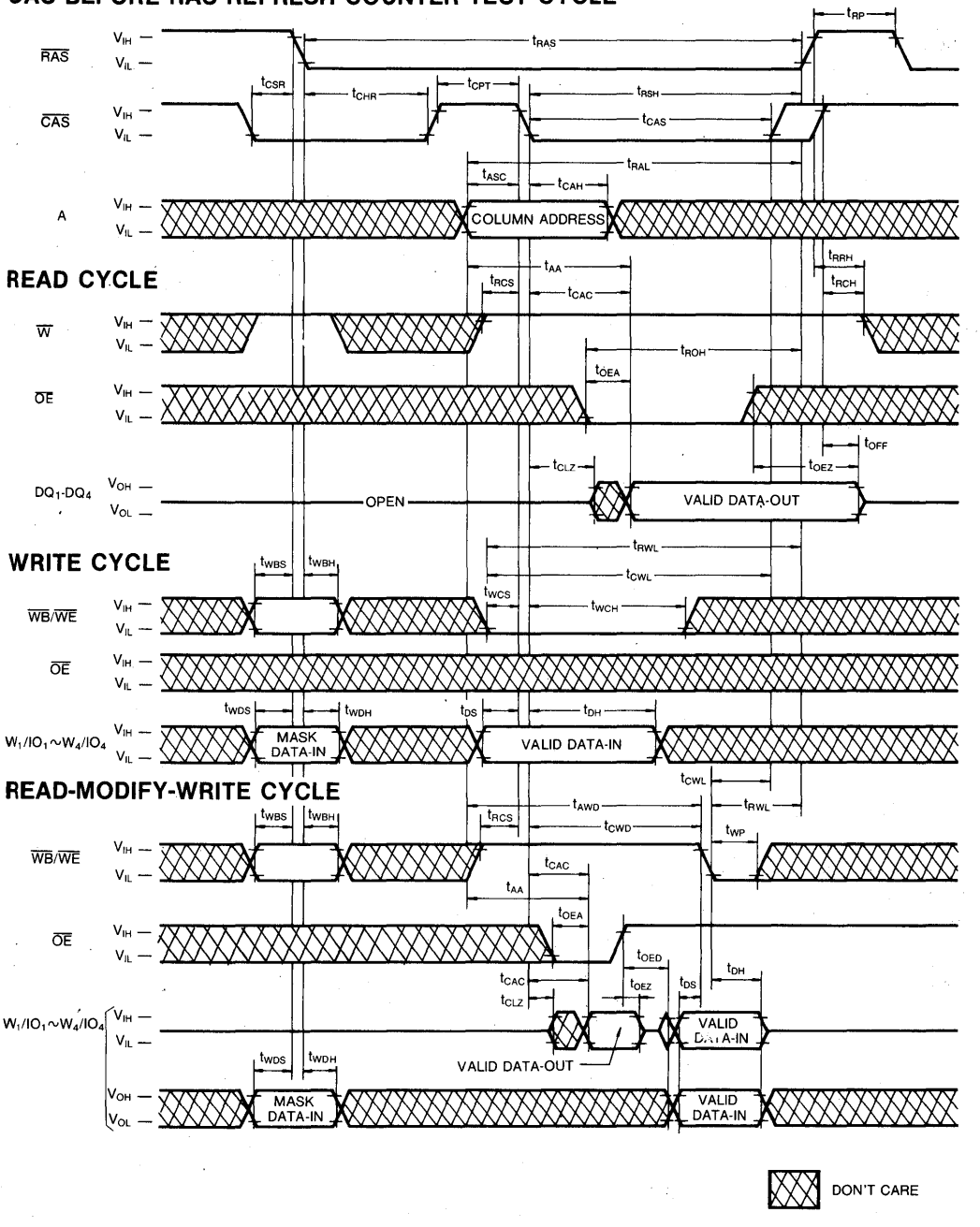
HIDDEN REFRESH CYCLE (WRITE)



SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

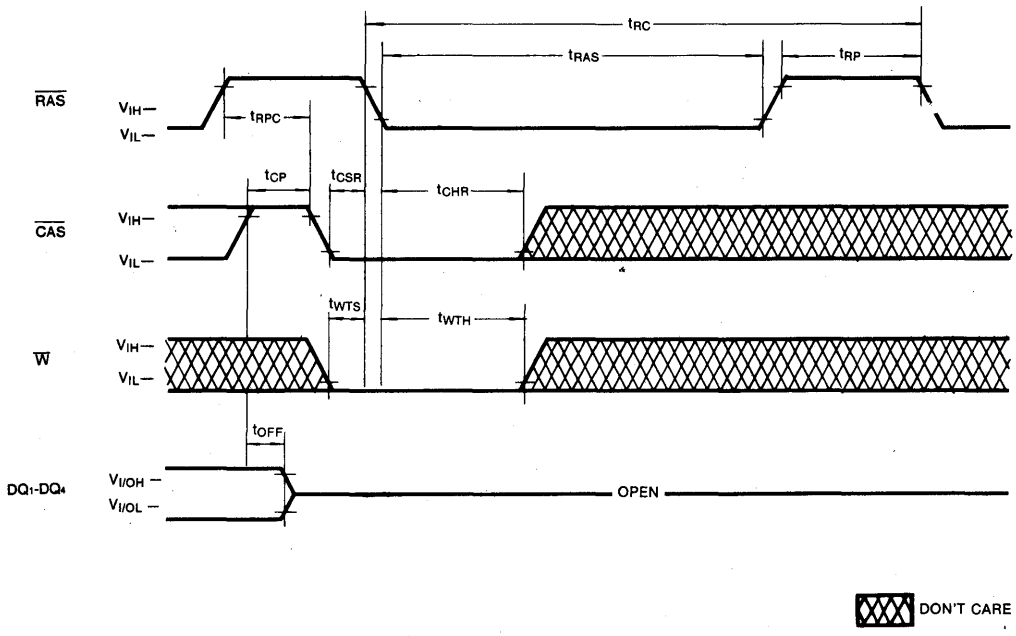
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: $\overline{OE}$, Address=Don't Care



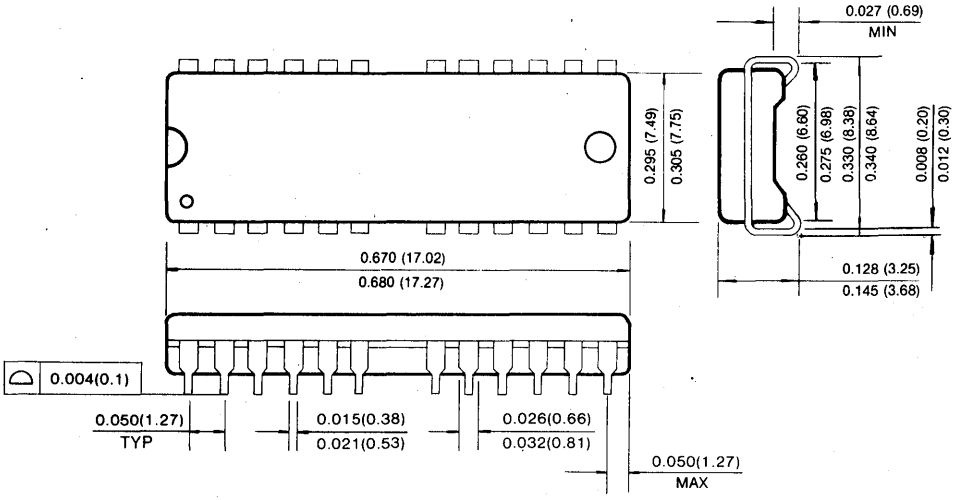
TEST MODE DESCRIPTION

The KM44C4010 is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 and A_1 are not used. If, upon reading, four bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 4M x 4 DRAM can be tested as if it were a 1M x 4 DRAM. $\overline{W}$, $\overline{CAS}$-Before-Ras Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

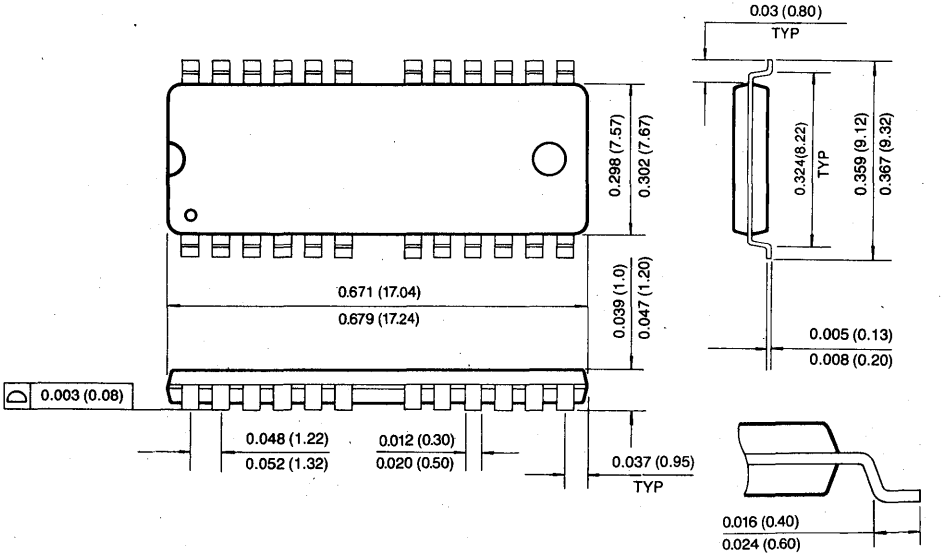
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



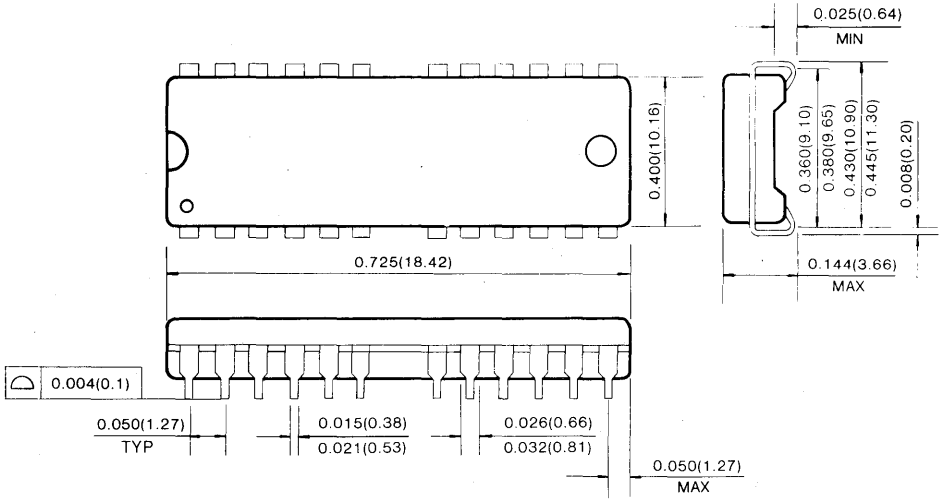
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



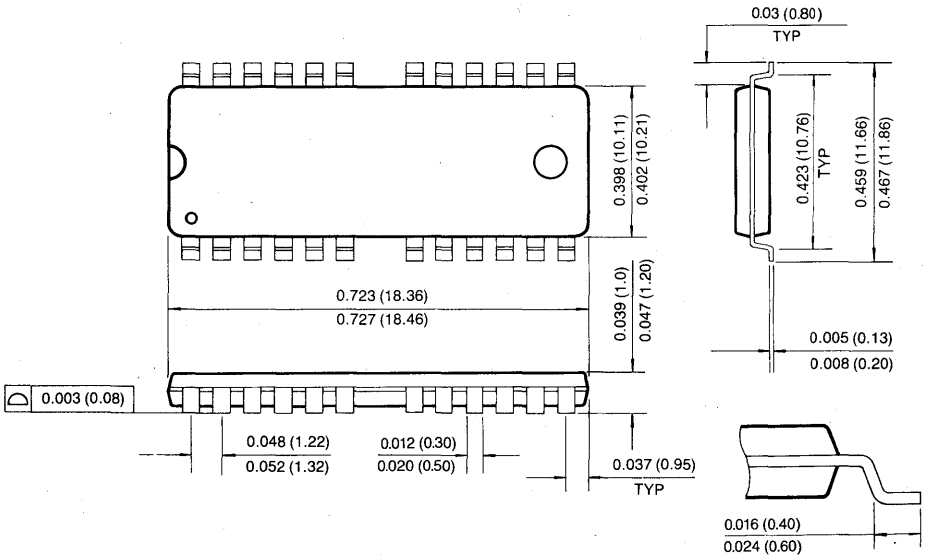
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



5

4M ×4 Bit CMOS Dynamic RAM with Fast Page Mode (Write Per Bit Mode)

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM44C4110A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4110A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4110A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4110A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Self Refrdsh Operation (LL-ver. only)**
- **Write Per Bit Mode capability**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V±10% power supply**
- **2048 cycles/32ms refresh (Normal)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

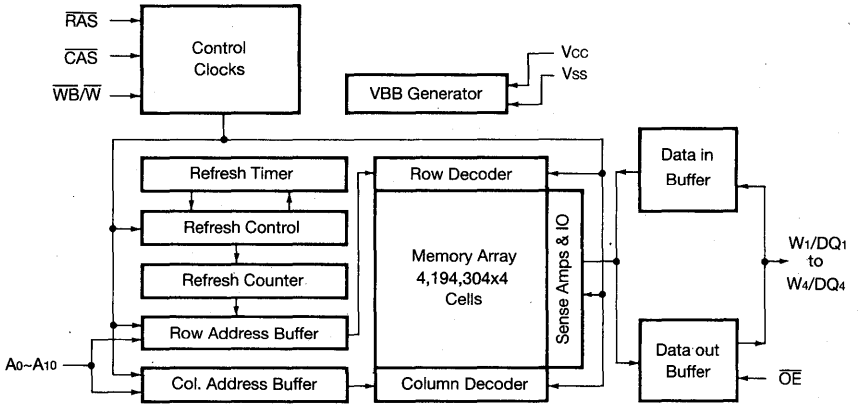
The Samsung KM44C4110A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4110A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C4110A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

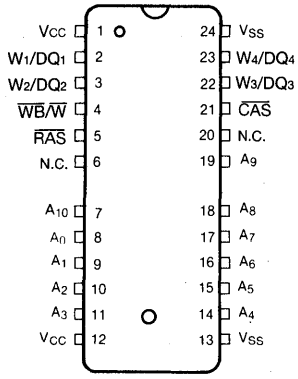
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

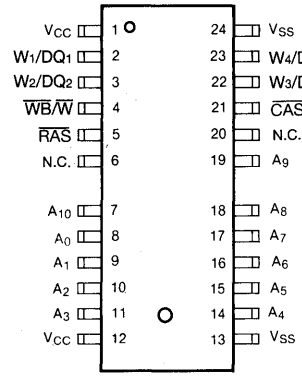
PIN CONFIGURATION (Top Views)

• **KM44C4110 AJ/ALJ/ALLJ/ASLJ**
AK/ALK/ALLK/ASLK



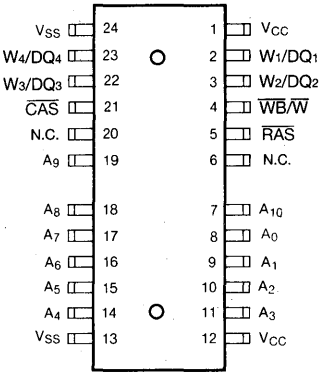
J : 400MIL
K : 300MIL

• **KM44C4110 AT/ALT/ALLT/ASLT**
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S: 300MIL(Forward)

• **KM44C4110 ATR/ALTR/ALLTR/ASLTR**
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
W_1/DQ_1~W_4/DQ_4	Write Select/Data in, out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB/W}$	Write Per Bit/Read, Write input
$\overline{OE}$	Data Output Enable
V_{CC}	Power(+5.0V)
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4110A/AL/ALL/ASL-5	I_{CC1}	-	110	mA
	KM44C4110A/AL/ALL/ASL-6			100	mA
	KM44C4110A/AL/ALL/ASL-7			90	mA
	KM44C4110A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{WB/W}$=V_{IH})	KM44C4110A	I_{CC2}	-	2	mA
	KM44C4110AL			1	mA
	KM44C4110ALL			1	mA
	KM44C4110ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44C4110A/AL/ALL/ASL-5	I_{CC3}	-	110	mA
	KM44C4110A/AL/ALL/ASL-6			100	mA
	KM44C4110A/AL/ALL/ASL-7			90	mA
	KM44C4110A/AL/ALL/ASL-8			80	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44C4110A/AL/ALL/ASL-5	I_{CC4}	-	90	mA
	KM44C4110A/AL/ALL/ASL-6			80	mA
	KM44C4110A/AL/ALL/ASL-7			70	mA
	KM44C4110A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{WB/W}$=V_{CC}-0.2V)	KM44C4110A	I_{CC5}	-	1	mA
	KM44C4110AL			300	μA
	KM44C4110ALL			200	μA
	KM44C4110ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4110A/AL/ALL/ASL-5	I_{CC6}	-	110	mA
	KM44C4110A/AL/ALL/ASL-6			100	mA
	KM44C4110A/AL/ALL/ASL-7			90	mA
	KM44C4110A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ_1~DQ_4=Don't Care t_{RC}=62.5μs(L-Ver.) 125μs(SL-Ver.), t_{RAS}=t_{RAS} min~300ns	KM44C4110AL	I_{CC7}	-	400	μA
	KM44C4110ASL			300	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{WB}$/$\overline{W}$=$\overline{OE}$=A_0-A_{10}=V_{CC}-0.2V or 0.2V W_1/DQ_1-W_4/DQ_4=V_{CC}-0.2V, 0.2V or Open	KM44C4110ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		I_{OL}	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{10})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}$/$\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (W_1/DQ_1~W_4/DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		50		55		60		ns	6
Refresh period (Normal)	t_{REF}		32		32		32		32	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	80		85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ pulse width(Fast Page mode)	t_{RASP}	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		13		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	13		15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	15
Write per bit set-up time	tWBS	0		0		0		0		ns	
Write per bit hold time	tWBH	10		10		10		10		ns	
Write selection set-up time	tWDS	0		0		0		0		ns	
Write per bit selection hold time	tWDH	10		10		10		10		ns	

TEST MODE CYCLE

(Note.12)

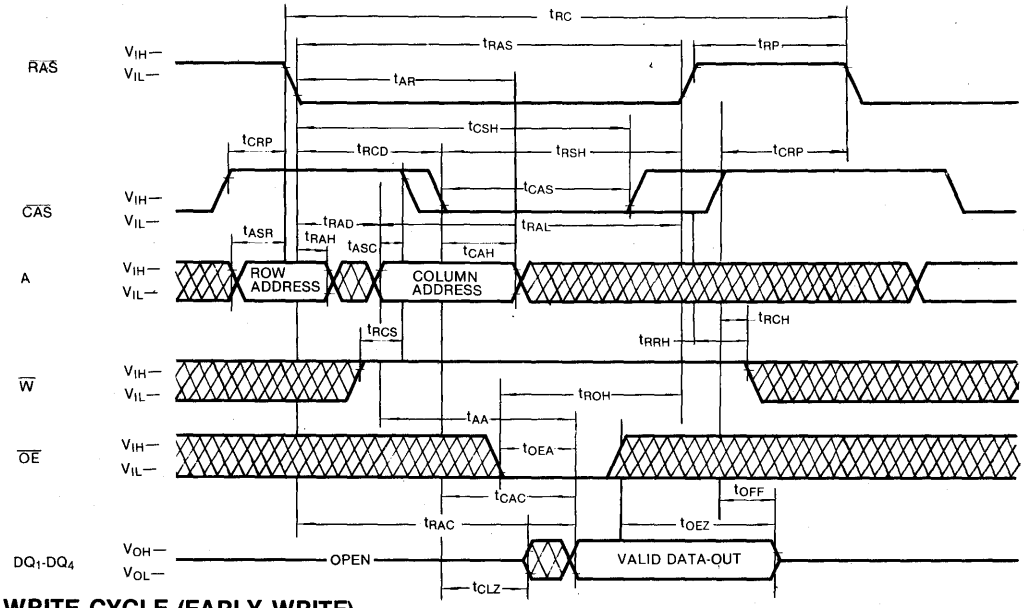
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

NOTES

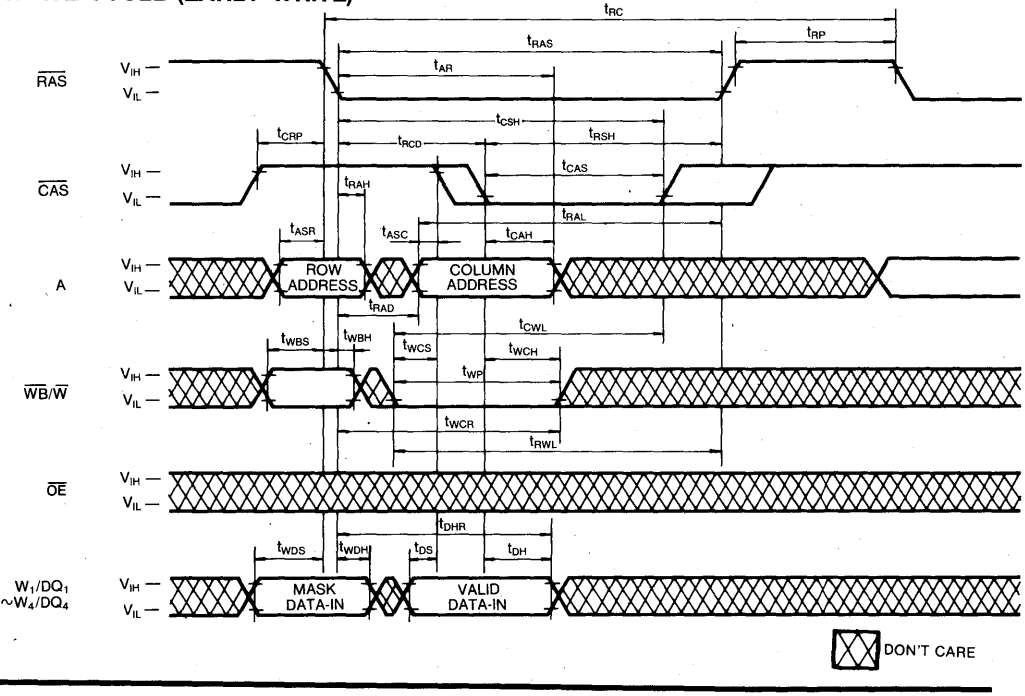
1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data output is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 32ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS

READ CYCLE

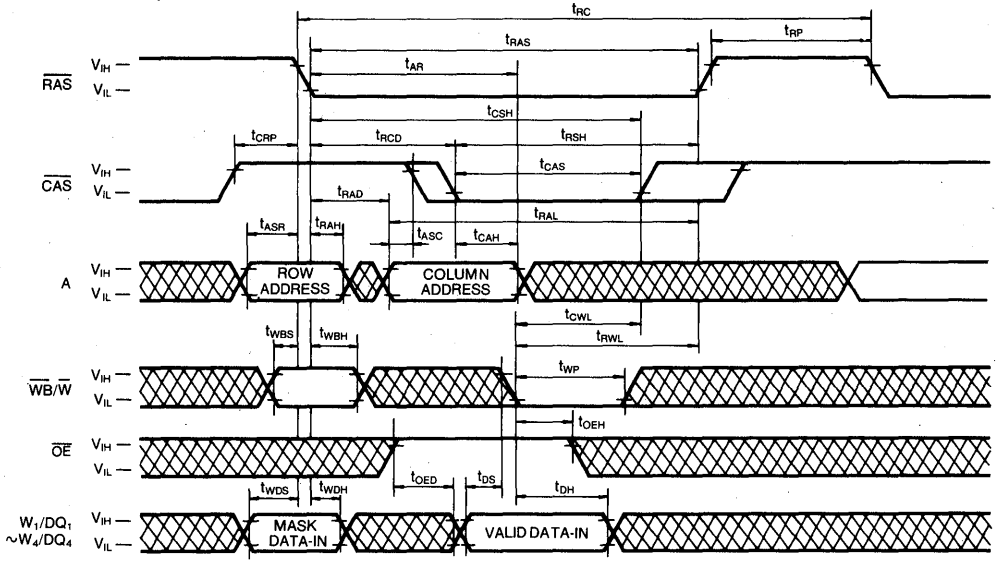


WRITE CYCLE (EARLY WRITE)

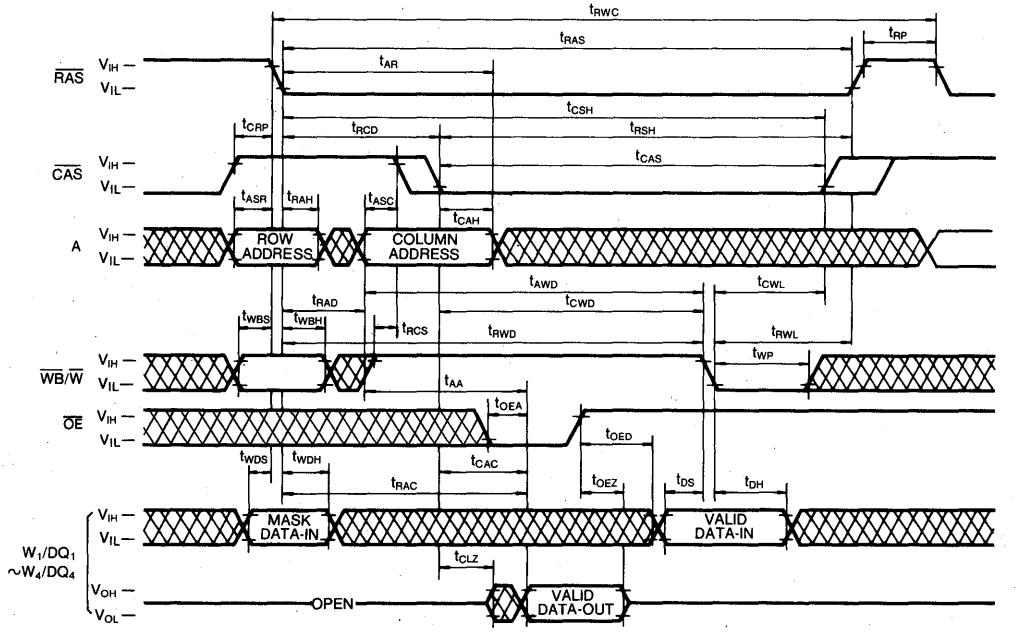


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



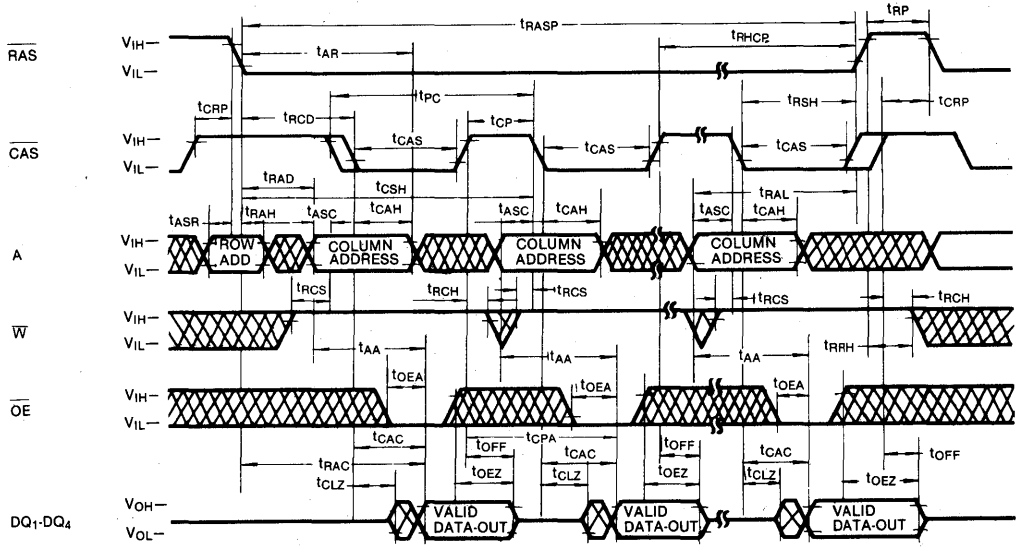
READ-MODIFY-WRITE CYCLE



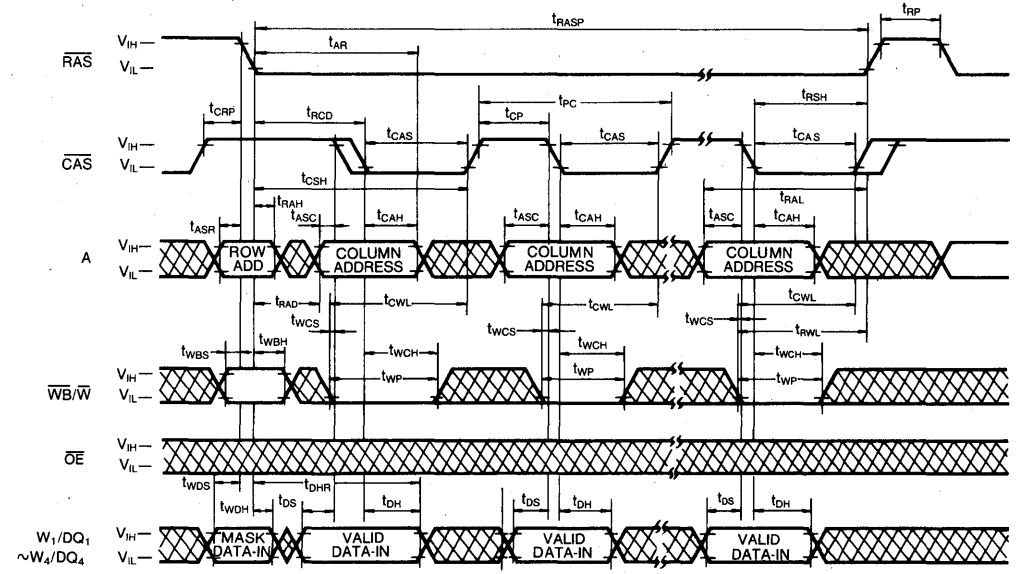
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



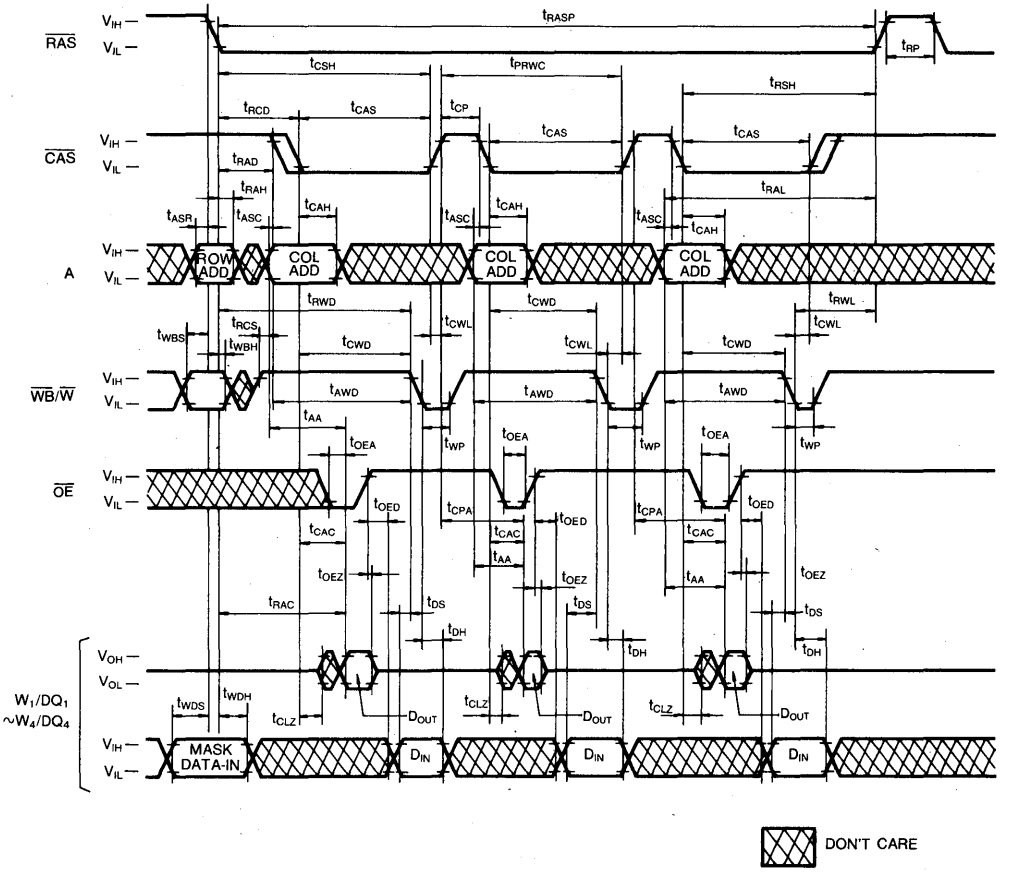
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

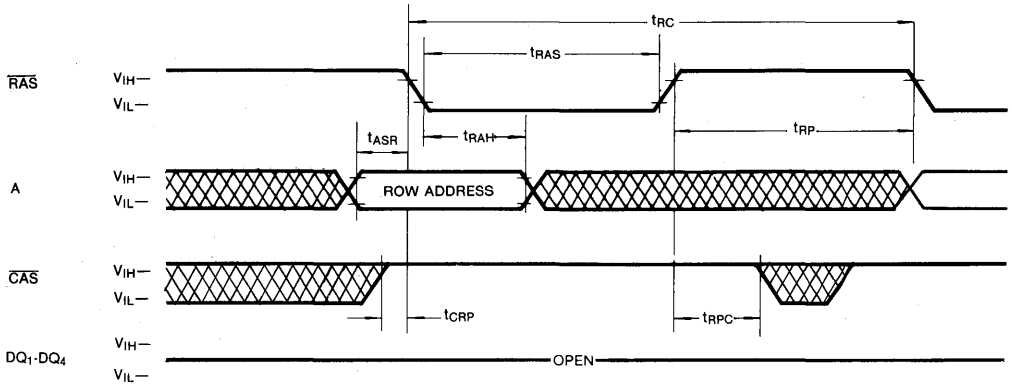


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

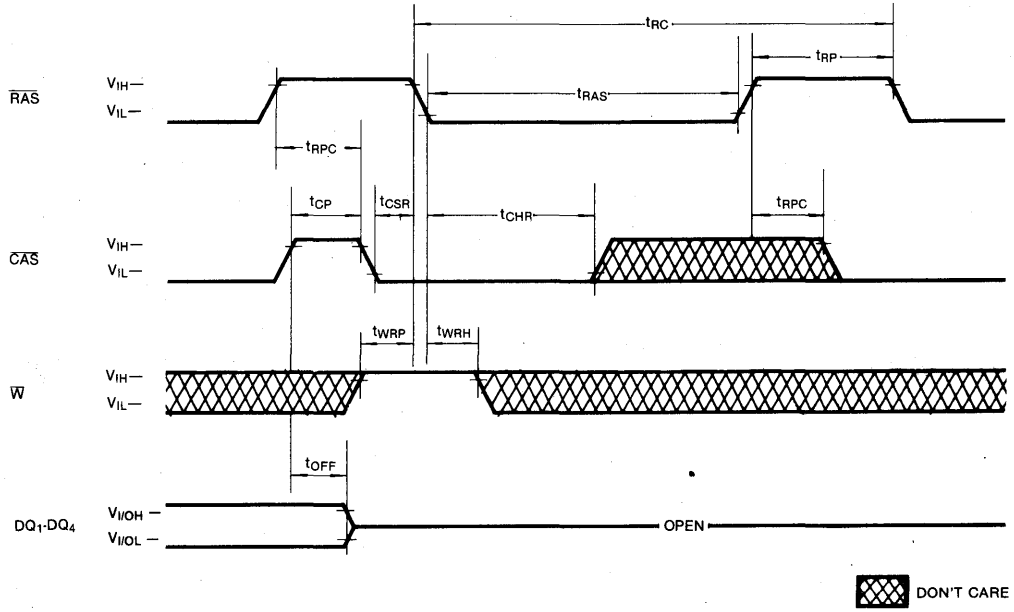
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

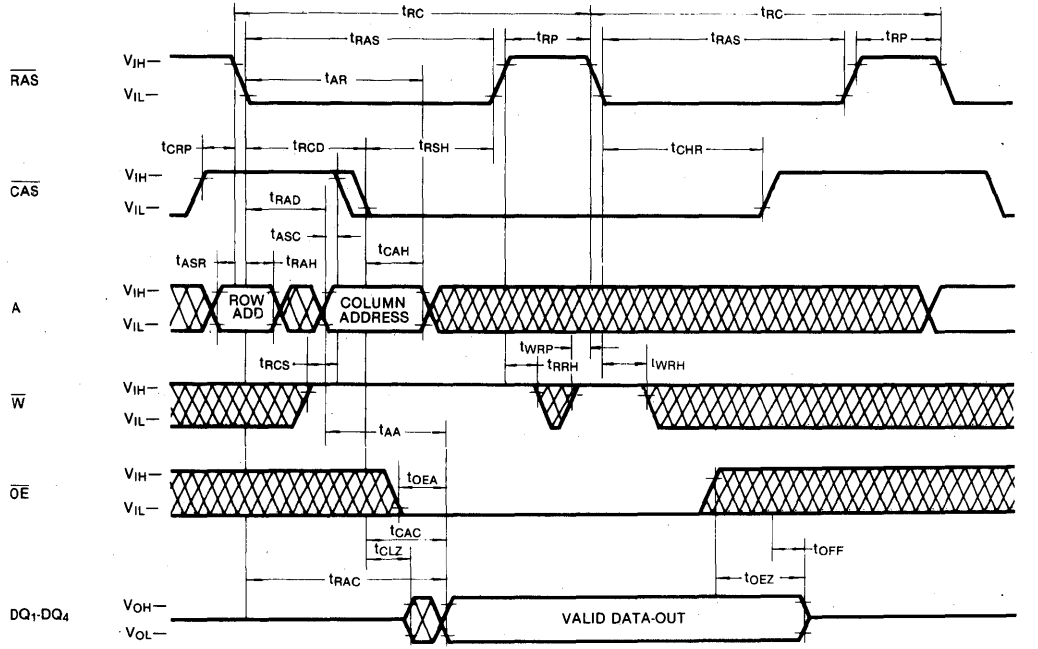
NOTE: $\overline{OE}$, Address = Don't Care



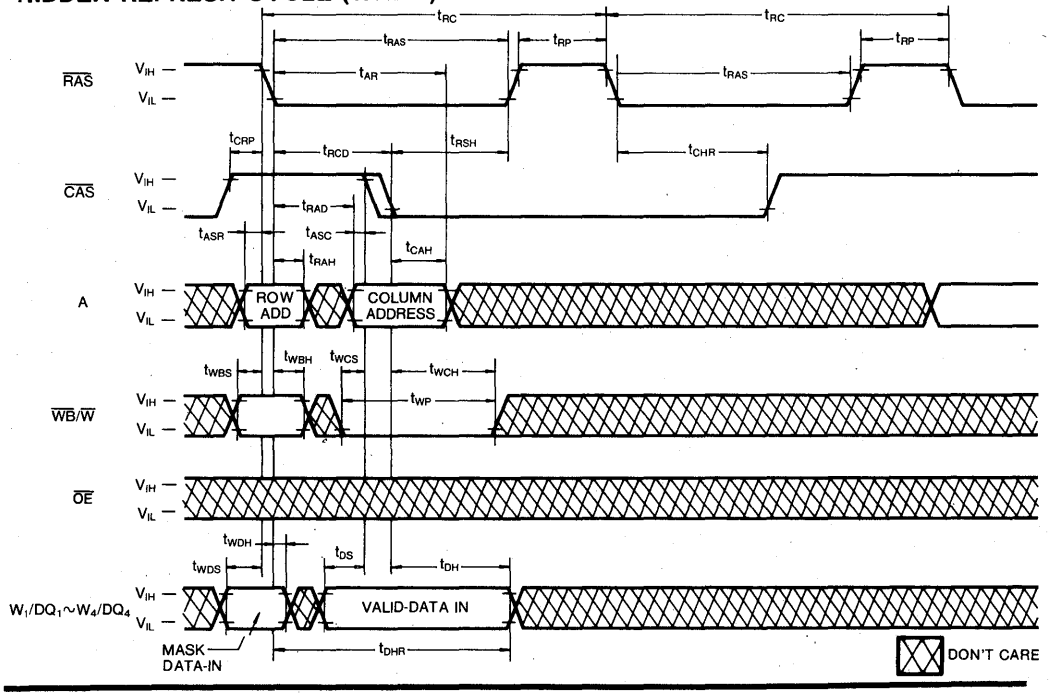
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



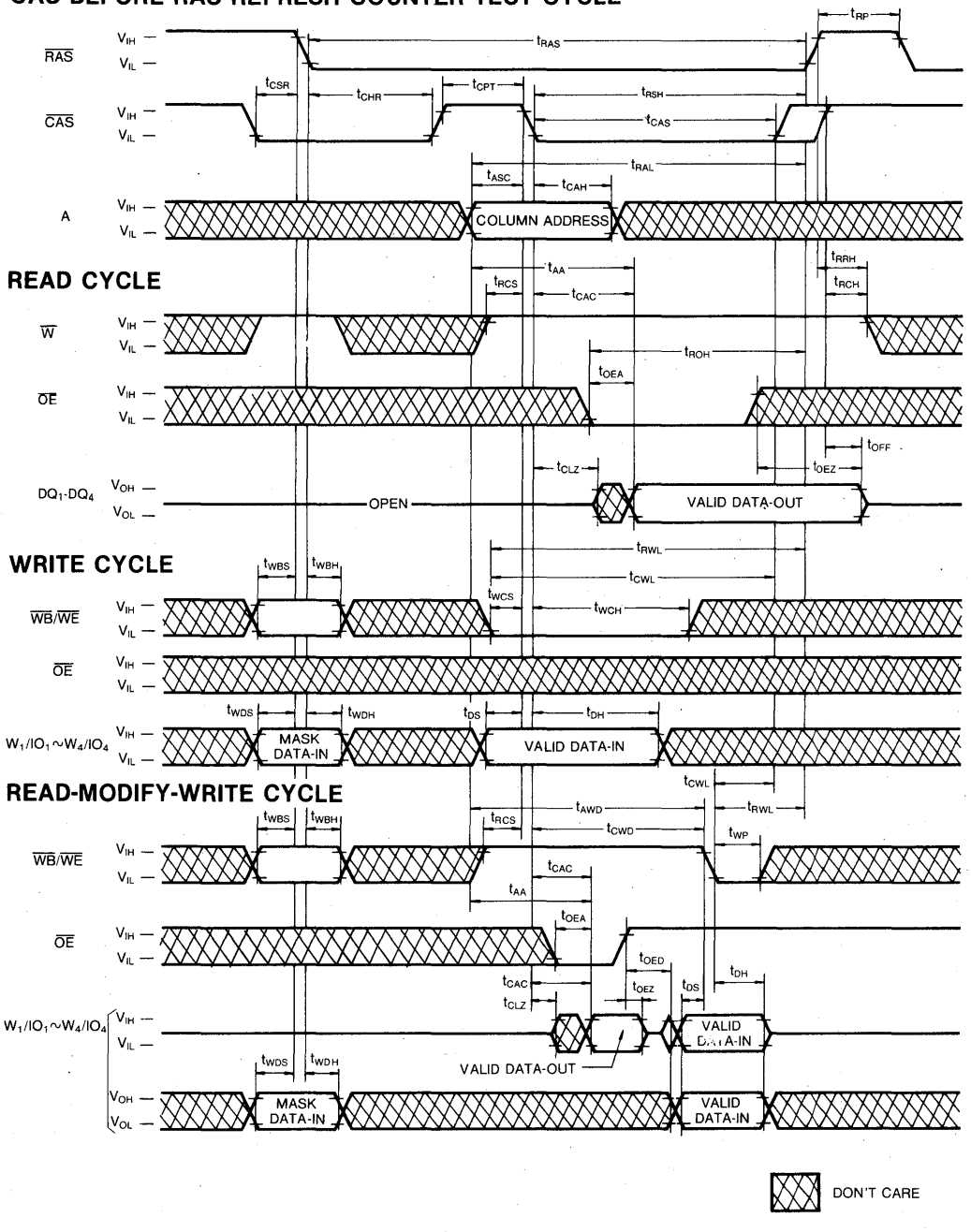
HIDDEN REFRESH CYCLE (WRITE)



SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

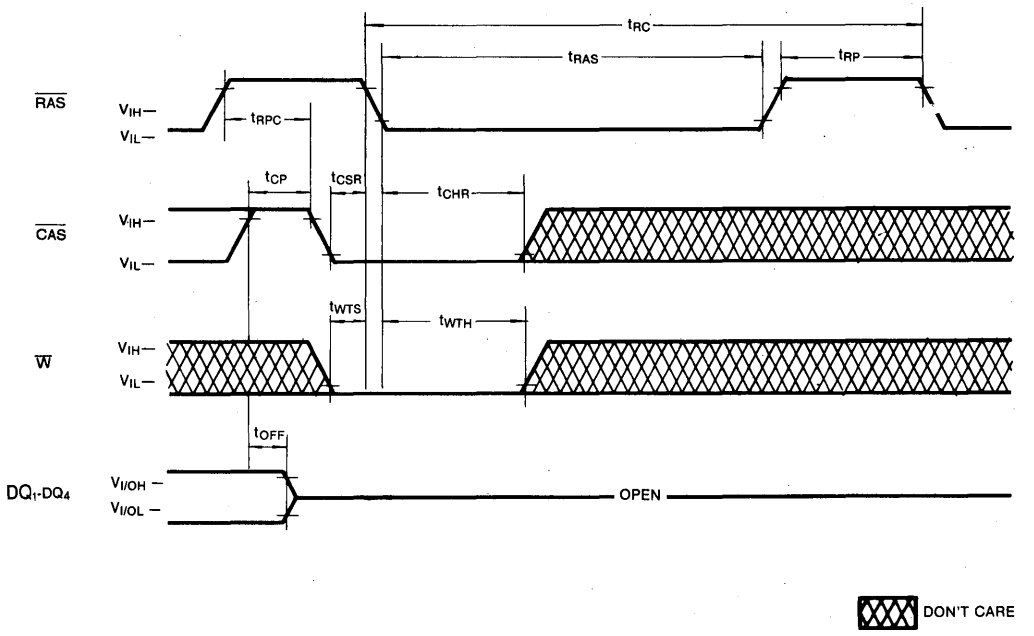


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: $\overline{OE}$, Address=Don't Care



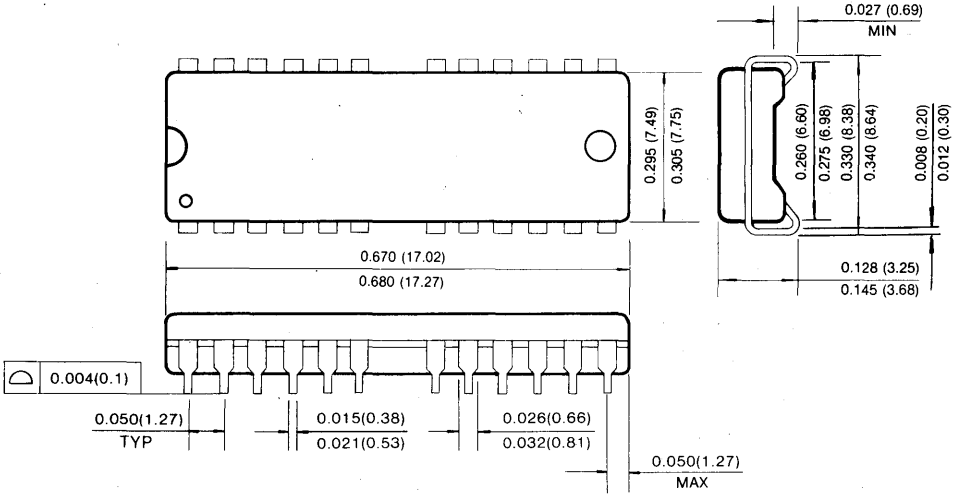
TEST MODE DESCRIPTION

The KM44C4110 is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 and A1 are not used. If, upon reading, four bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode" the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. $\overline{W}$, $\overline{CAS}$-Before-RAS Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "RAS only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



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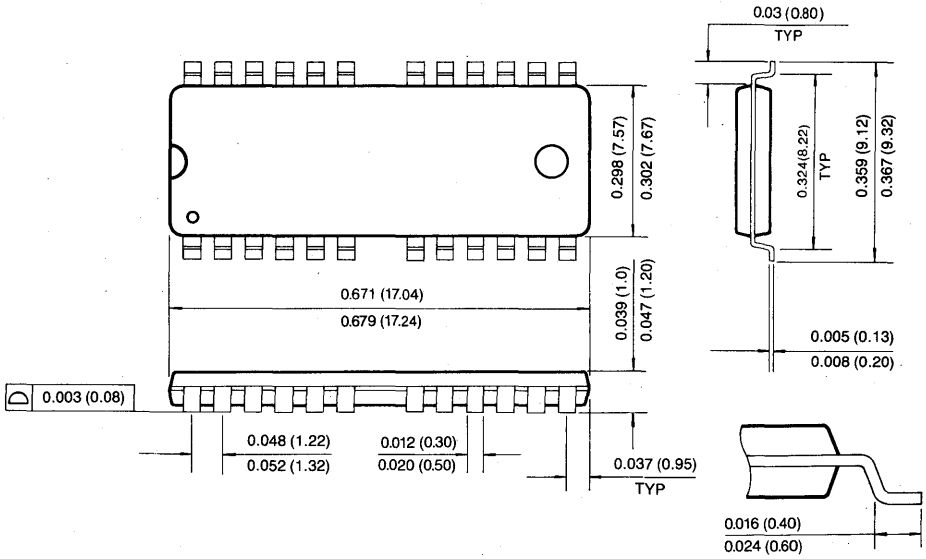
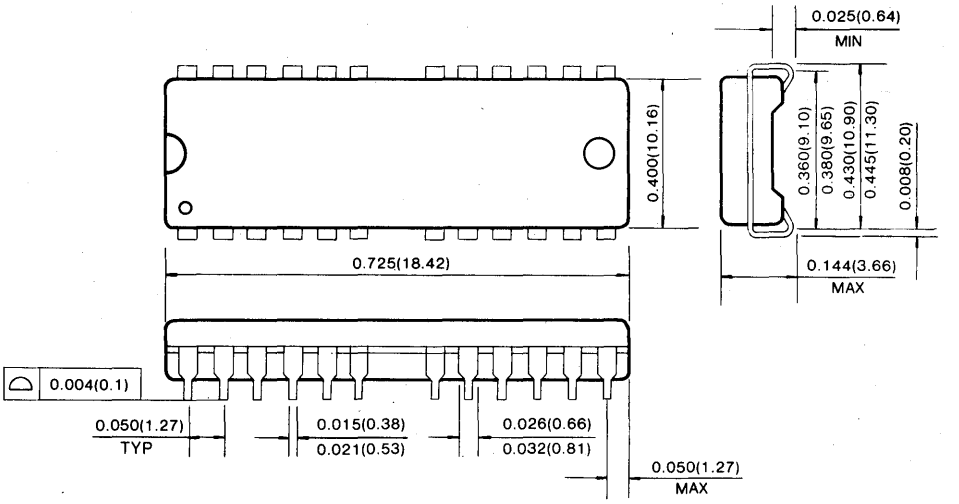
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



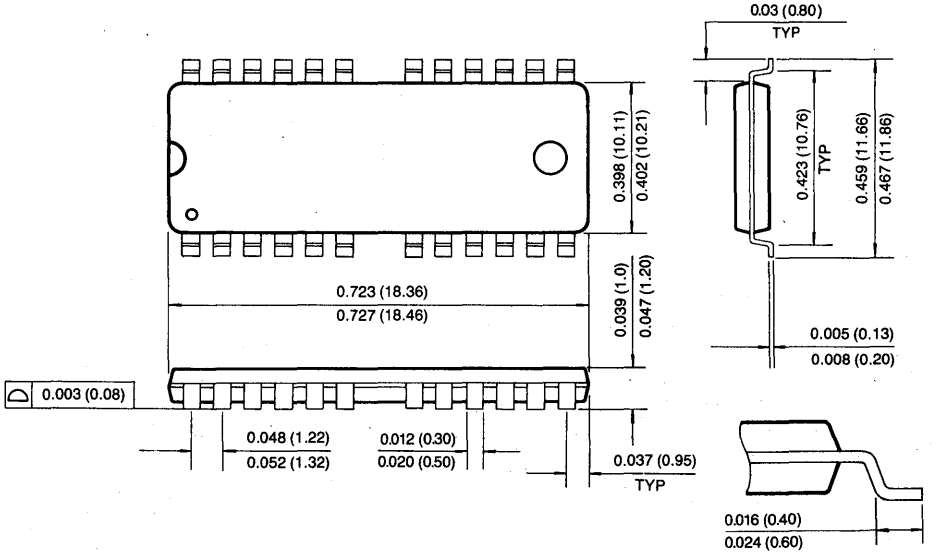
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M ×4 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM44C4002A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4002A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4002A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4002A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Static Column Mode operation**
- **Self Refresh Operation (LL-ver, only)**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V±10% power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

The Samsung KM44C4002A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4002A/AL/ALL/ASL features Static Column Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C4002A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

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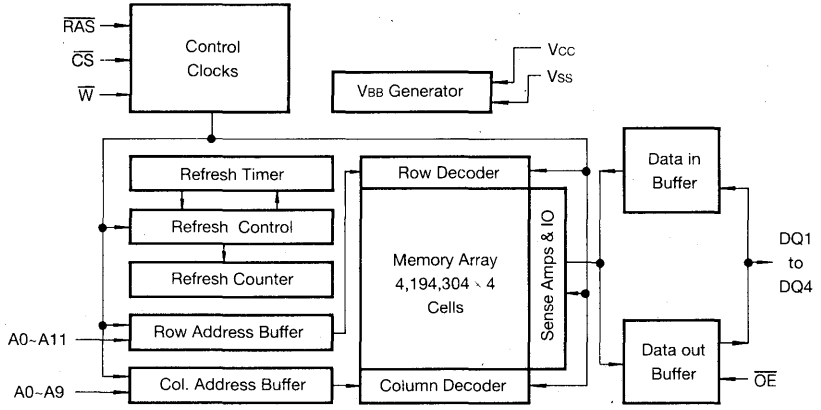
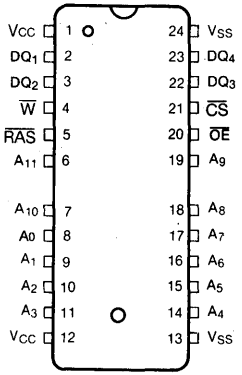
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

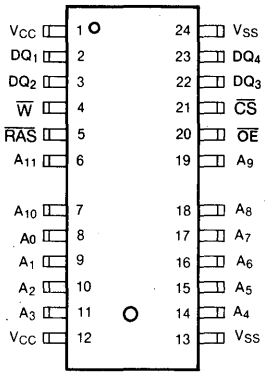
PIN CONFIGURATION (Top Views)

• KM44C4002 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



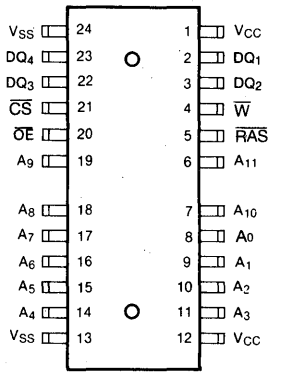
J : 400MIL
K : 300MIL

• KM44C4002 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44C4002 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A_0-A_{11}	Address Inputs
$DQ_{1\sim4}$	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select input
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power(+5.0V)
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC}=min.)	KM44C4002A/AL/ALL/ASL-5	I_{CC1}	-	90	mA
	KM44C4002A/AL/ALL/ASL-6			80	mA
	KM44C4002A/AL/ALL/ASL-7			70	mA
	KM44C4002A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{IH})	KM44C4002A	I_{CC2}	-	2	mA
	KM44C4002AL			1	mA
	KM44C4002ALL			1	mA
	KM44C4002ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44C4002A/AL/ALL/ASL-5	I_{CC3}	-	90	mA
	KM44C4002A/AL/ALL/ASL-6			80	mA
	KM44C4002A/AL/ALL/ASL-7			70	mA
	KM44C4002A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CS}$, Address Cycling @t_{PC}=min.)	KM44C4002A/AL/ALL/ASL-5	I_{CC4}	-	80	mA
	KM44C4002A/AL/ALL/ASL-6			70	mA
	KM44C4002A/AL/ALL/ASL-7			60	mA
	KM44C4002A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{CC}-0.2V)	KM44C4002A	I_{CC5}	-	1	mA
	KM44C4002AL			300	μA
	KM44C40 02ALL			200	μA
	KM44C4002ASL			200	μA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC}=min.)	KM44C4002A/AL/ALL/ASL-5	I_{CC6}	-	90	mA
	KM44C4002A/AL/ALL/ASL-6			80	mA
	KM44C4002A/AL/ALL/ASL-7			70	mA
	KM44C4002A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CS}$=$\overline{CS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ_1~DQ_4=Don't Care t_{RC}=31.25μs(L-Ver.) 62.5μs(SL-Ver.), t_{RAS} =t_{RAS} min~300ns	KM44C4002AL	I_{CC7}	-	450	μA
	KM44C4002ASL			350	μA

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DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{CC}-0.2V or 0.2V DQ_1-DQ_4=V_{CC}-0.2V, 0.2V or Open	KM44C4002ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		I_{OL}	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one Static Column cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CS}$ pulse width	t_{CS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		50		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64		64	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CS}$ set-up time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Static column mode cycle time	t_{SC}	30		35		40		45		ns	3
Static column mode read-write cycle time	t_{SRWC}	80		85		100		110		ns	
Access time from last write	t_{ALW}		50		55		65		75	ns	3, 12
Output data hold time from column address	t_{AOH}	5		5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		35		40		45		55	ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{CS}$ pulse width (Static column mode)	t_{CSC}	13	200000	15	200000	20	200000	20	200000	ns	
$\overline{CS}$ precharge time (Static column mode)	t_{CP}	10		10		10		10		ns	
Column address hold time referenced to $\overline{RAS}$ rising	t_{AH}	5		5		5		5		ns	
Last write to column address delay time	t_{LWAD}	20	25	20	25	25	30	25	35	ns	
Last write to column address hold time	t_{AHLW}	50		55		65		75		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command inactive time	tWI	10		10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	13		15		20		20		ns	
Write address hold time referenced to $\overline{RAS}$	tAWR	40		45		55		60		ns	6
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	15
$\overline{CS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	140		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CS}$ pulse width	tCS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		20		25		25		ns	
$\overline{CS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CS}$ to $\overline{W}$ delay time	tCWD	45		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	80		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		60		70		75		ns	8
Static column mode cycle time	tSC	35		40		45		50		ns	
Static column mode read-write cycle time	tSRWC	85		90		105		110		ns	
$\overline{RAS}$ pulse width (Static column mode)	tRASC	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from last write	tALW		55		60		70		80	ns	3,12
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

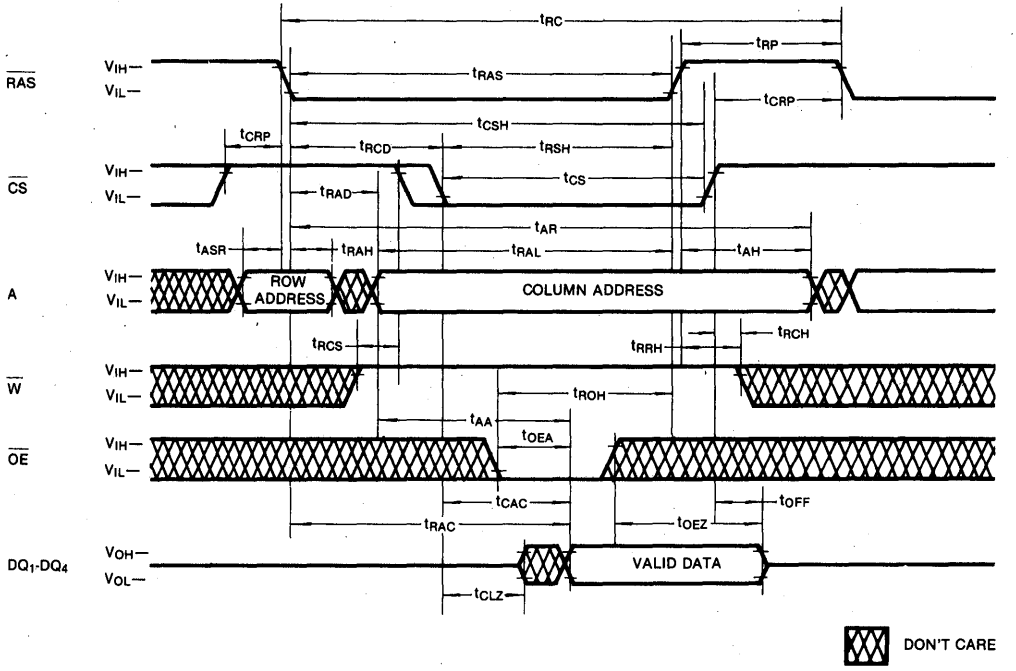
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data output is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

5

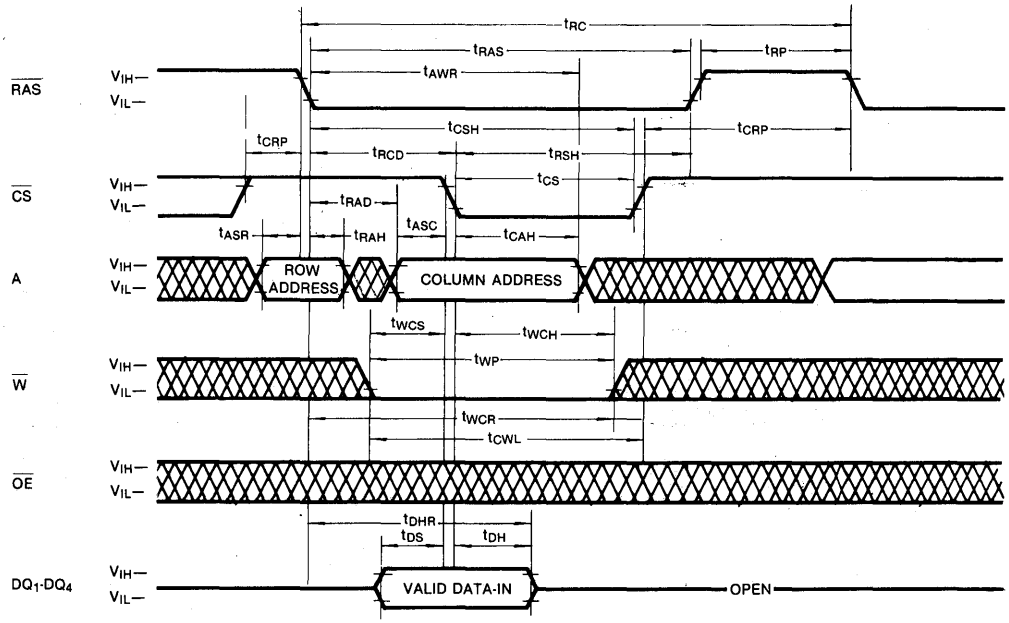
TIMING DIAGRAMS

READ CYCLE

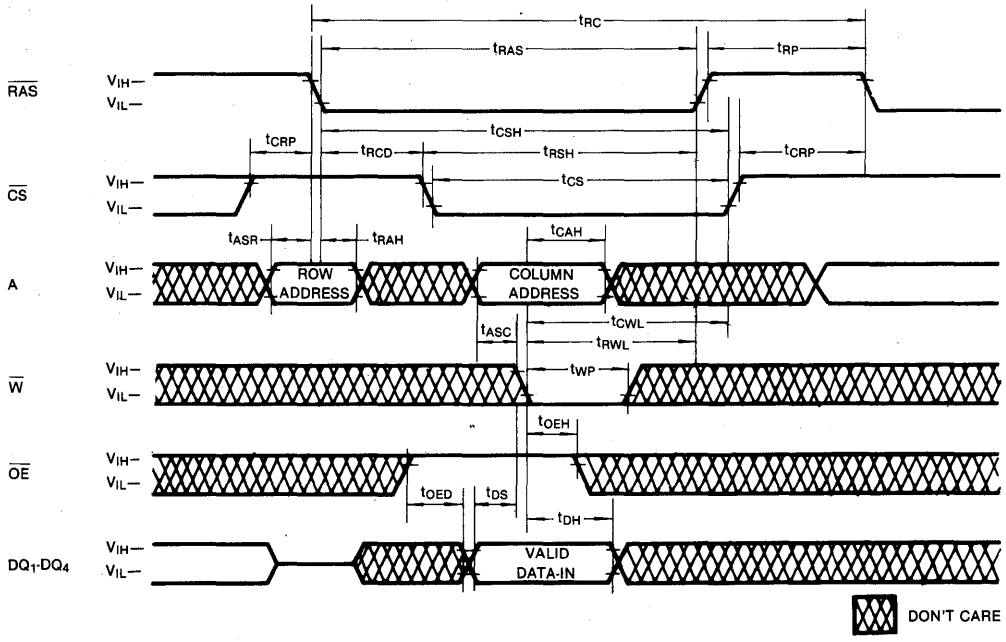


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



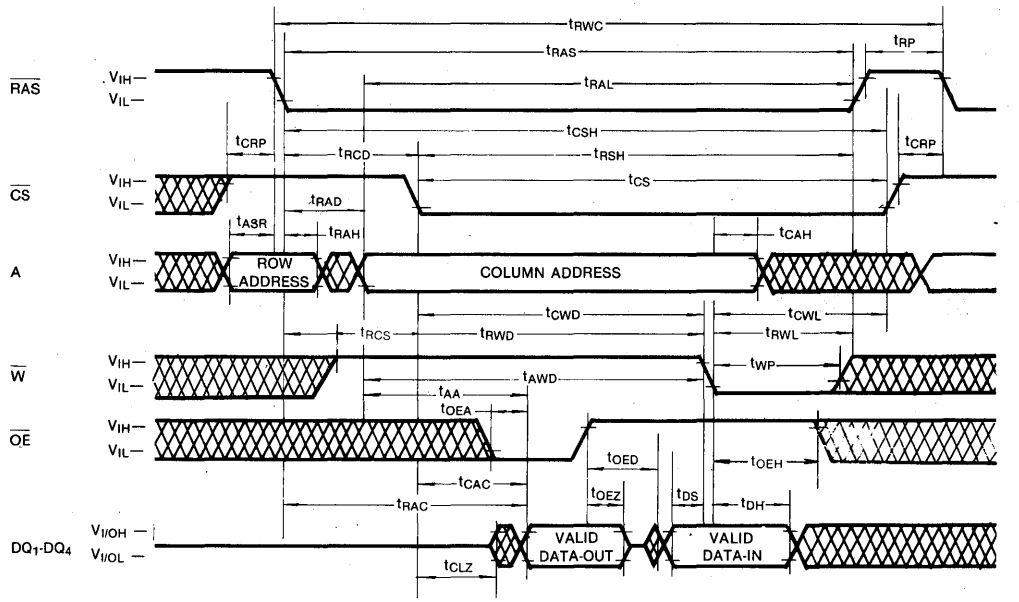
WRITE CYCLE (OE CONTROLLED WRITE)



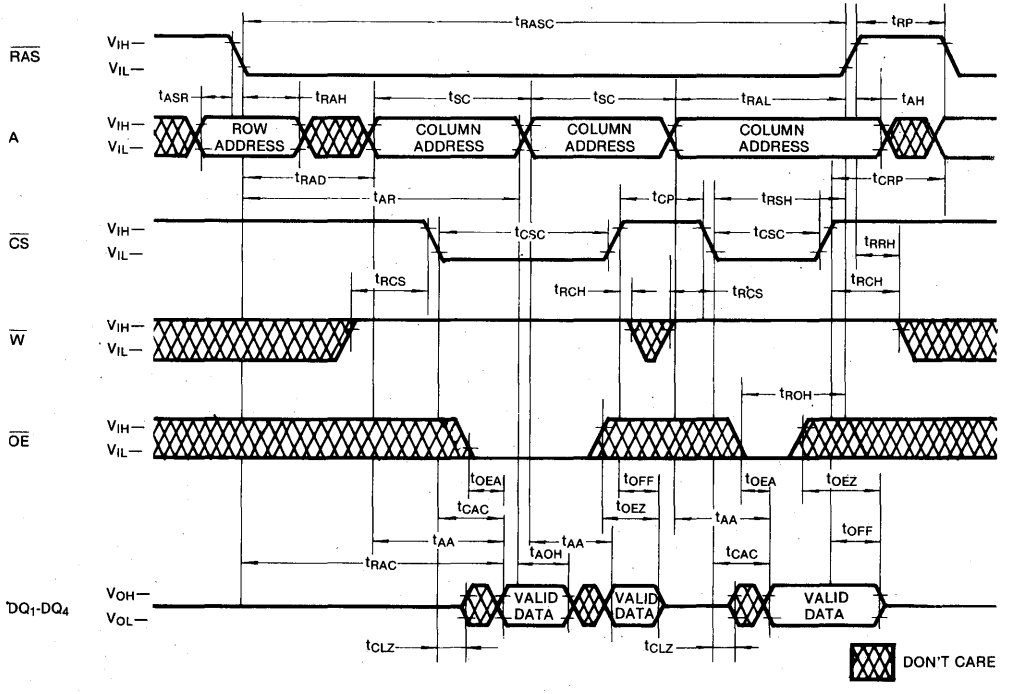
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

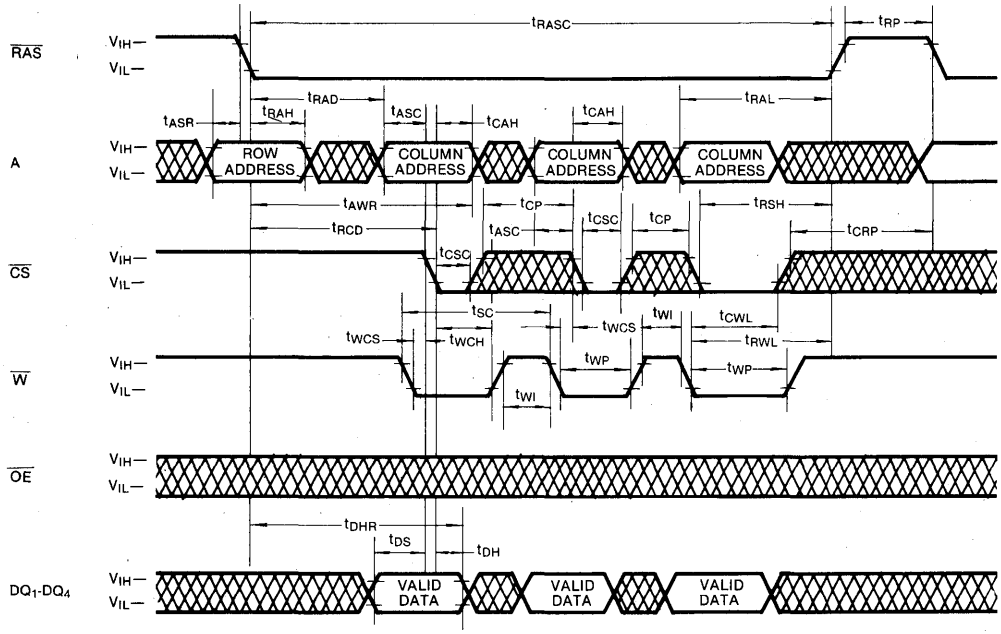


STATIC COLUMN MODE READ CYCLE

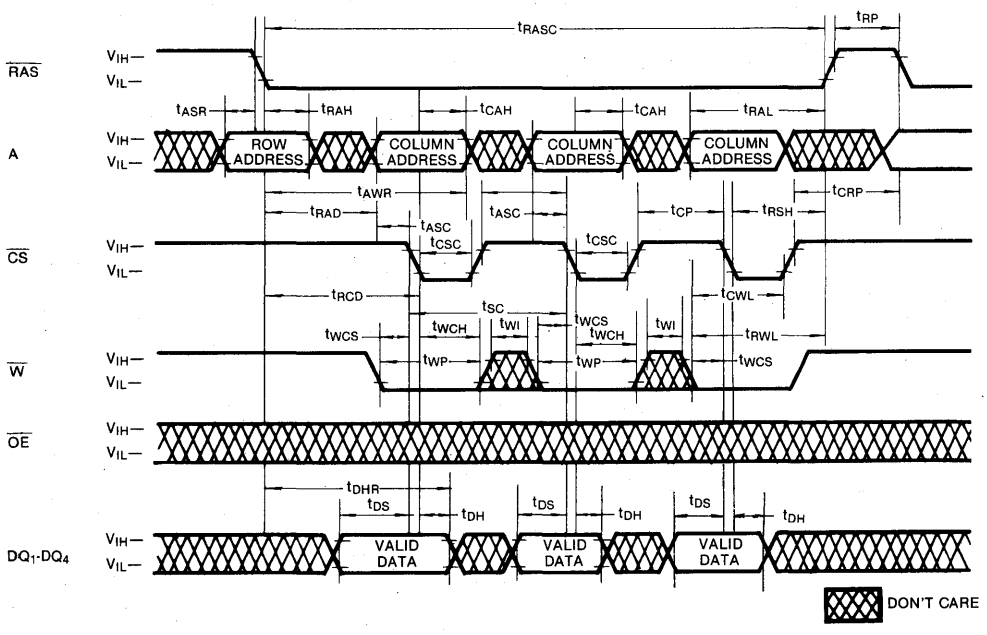


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ controlled early write)



STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)



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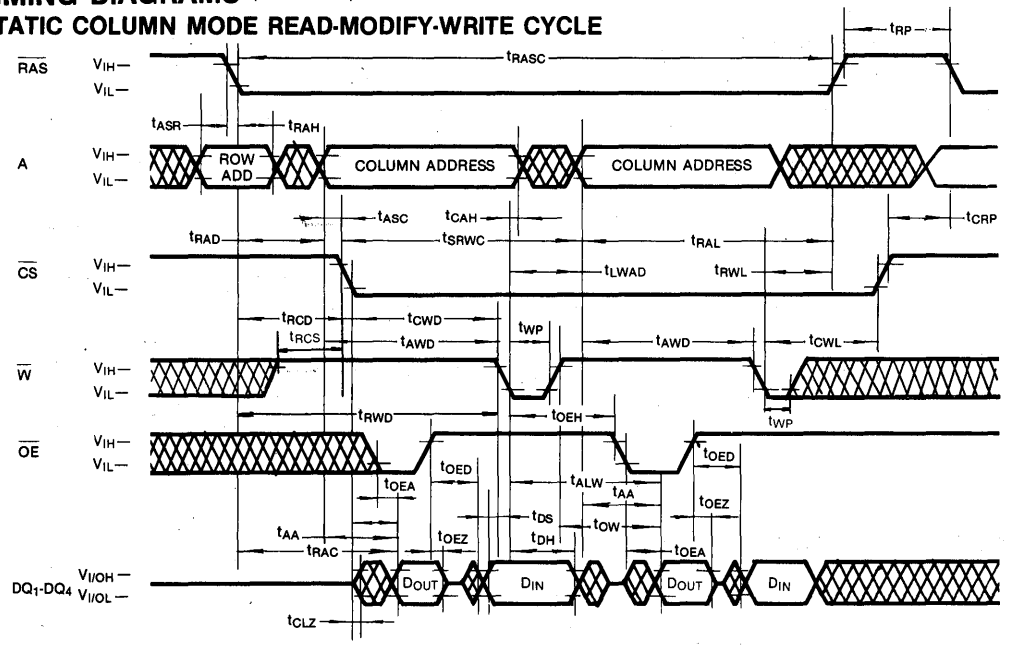
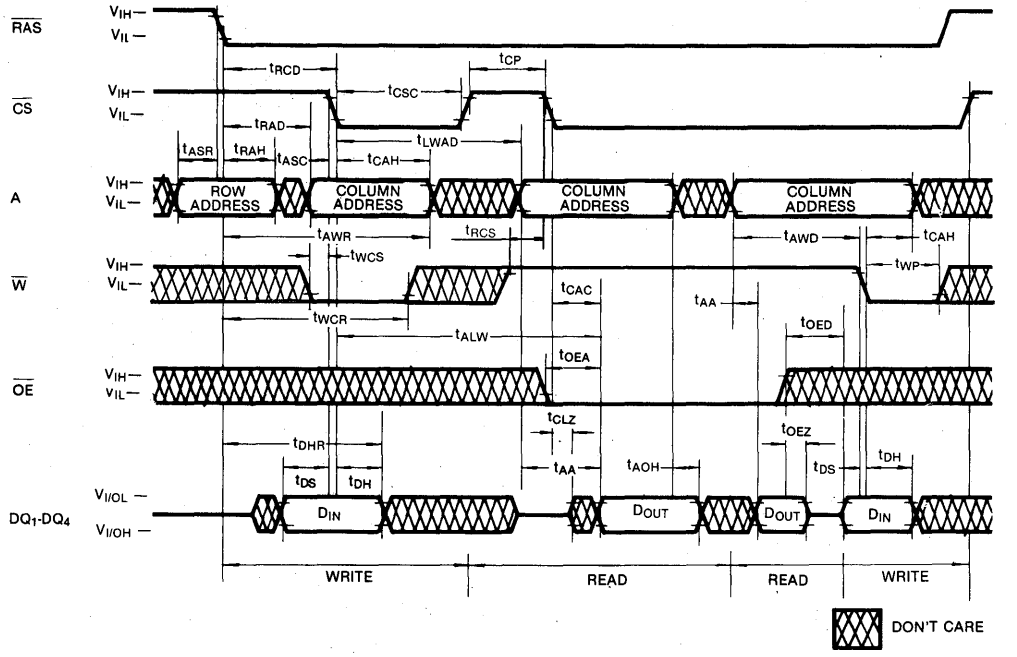
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE MIXED CYCLE

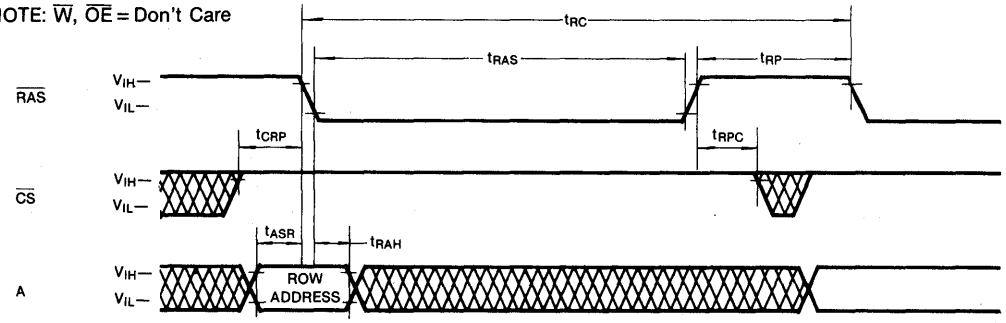


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

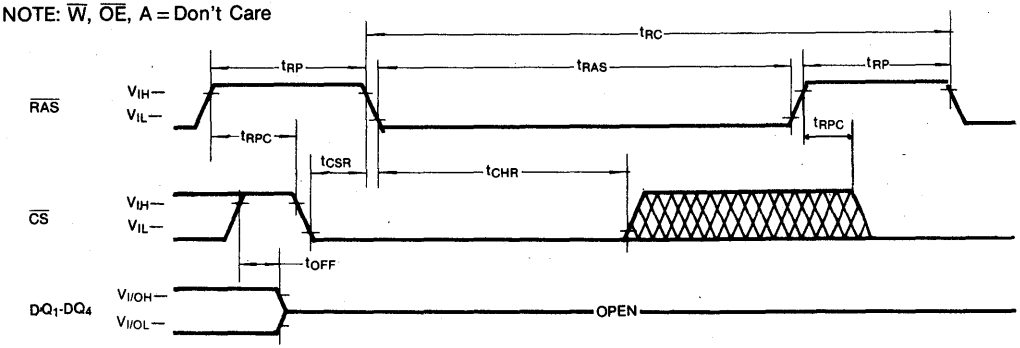
RAS-ONLY REFRESH CYCLE

NOTE: W, OE = Don't Care



CS-BEFORE-RAS REFRESH CYCLE

NOTE: W, OE, A = Don't Care

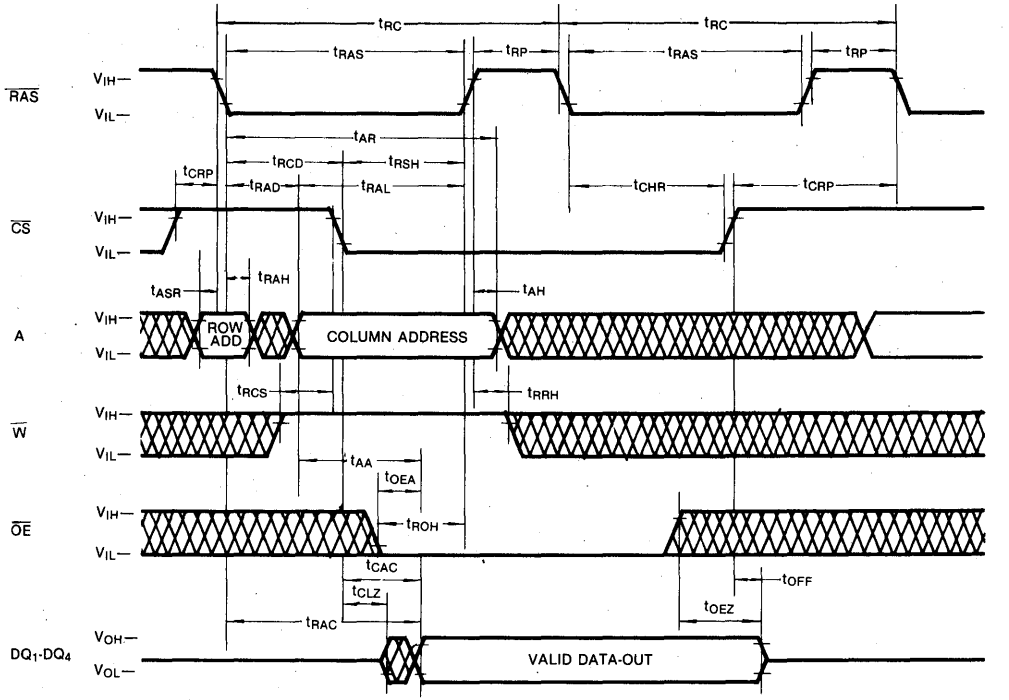


DON'T CARE

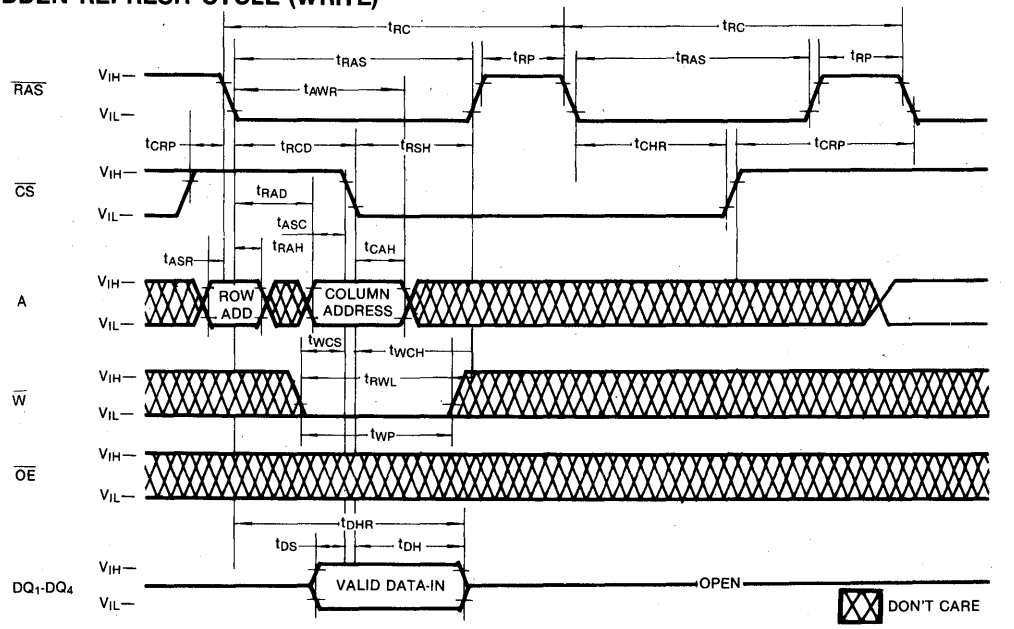
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



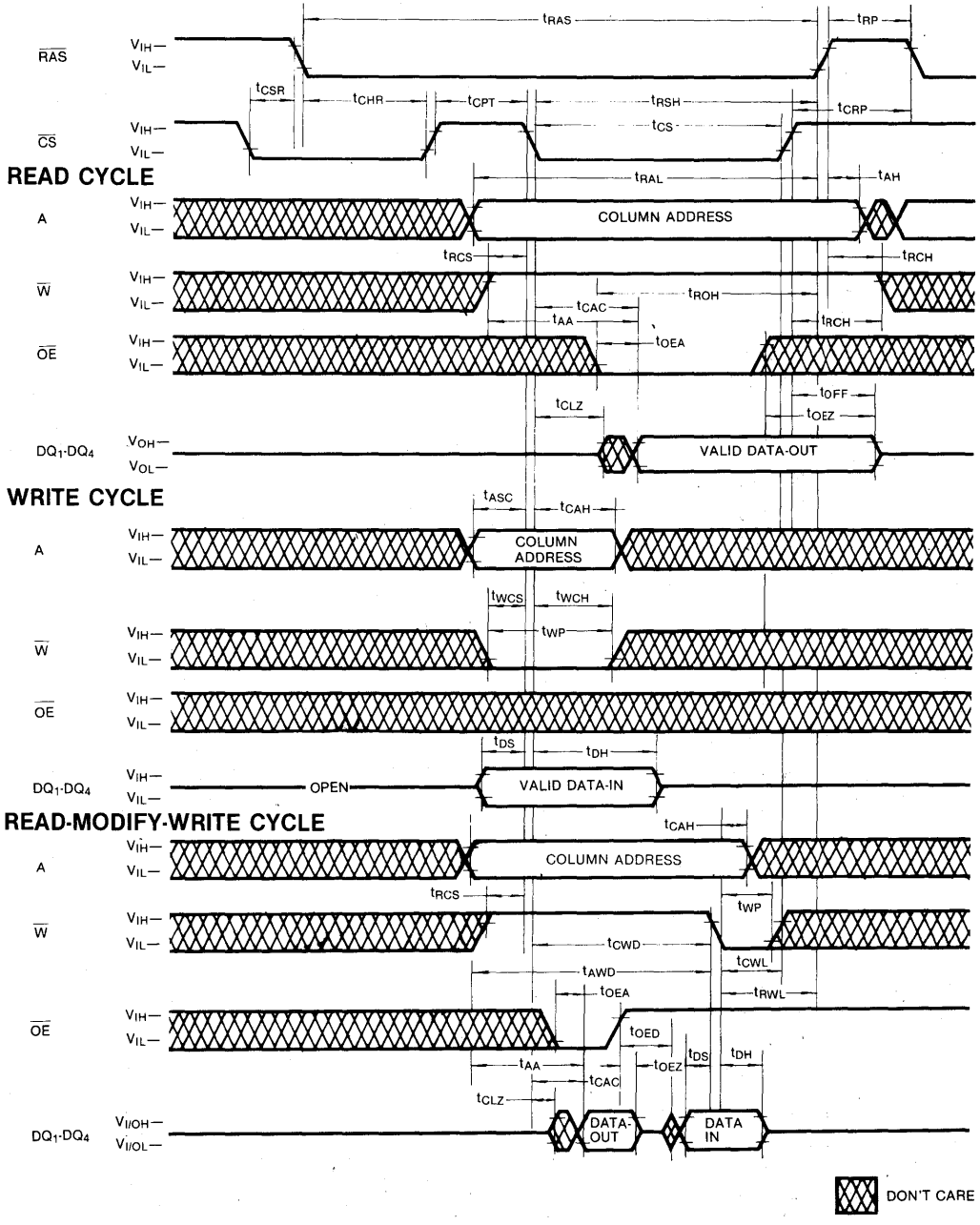
HIDDEN REFRESH CYCLE (WRITE)



SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

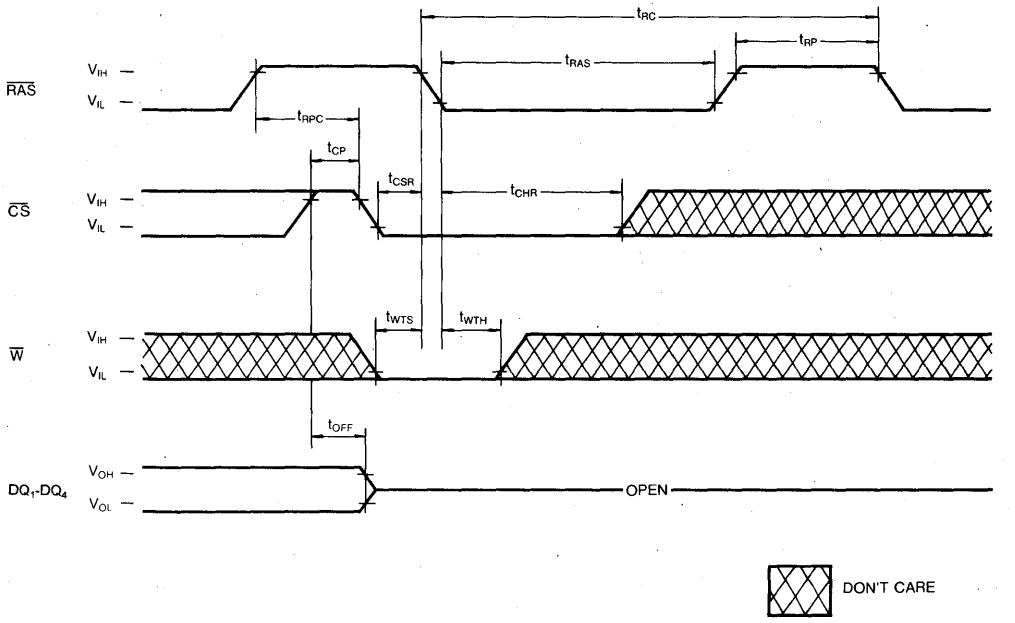
CS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



TEST MODE DESCRIPTION

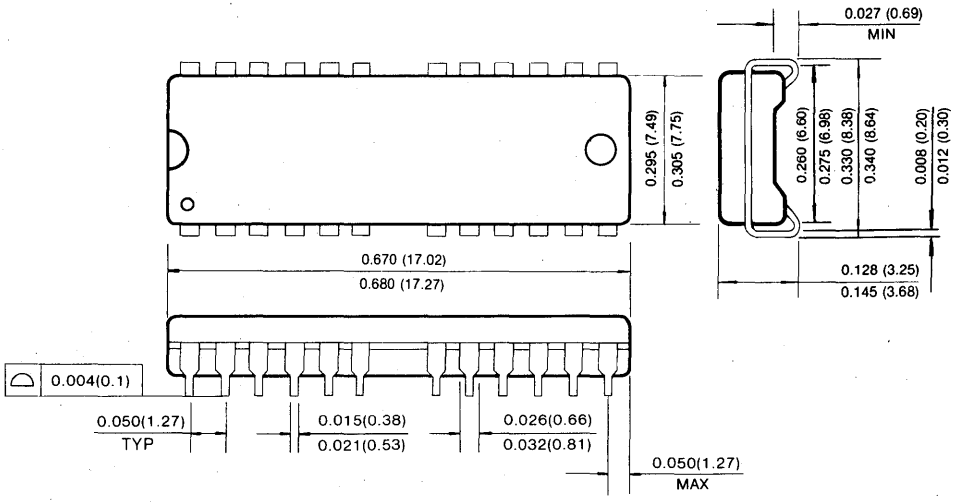
The KM44C4002 is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0, A_1, are not used. If, upon reading, 16 bits are equal (all "1" or "O"s) the Q pin indicates a "1".
If they were not equal, the Q pin would indicate a "0".

In "Test Mode", the 16M DRAM can be tested as if it were a 1M × 4 DRAM. $\overline{W}$, $\overline{CS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And $\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE "or" $\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



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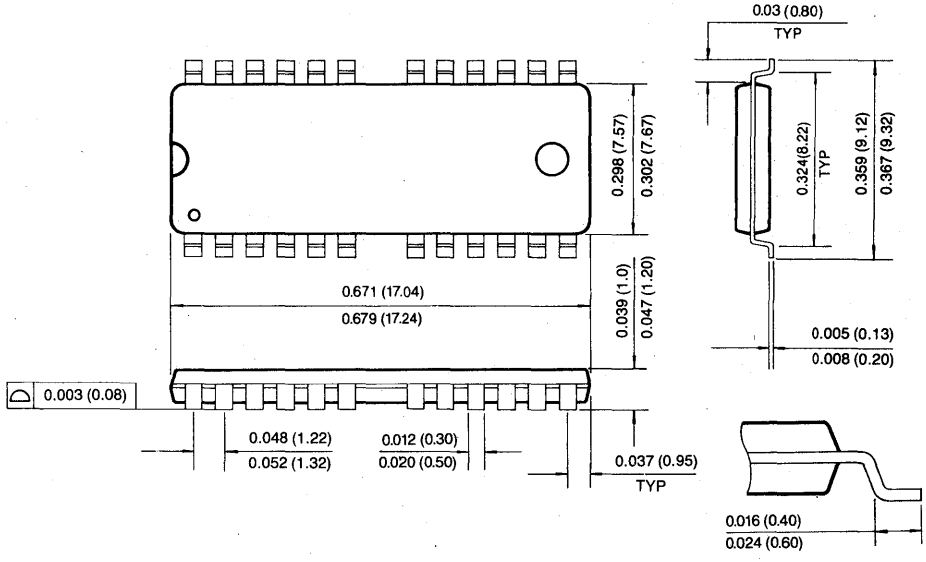
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

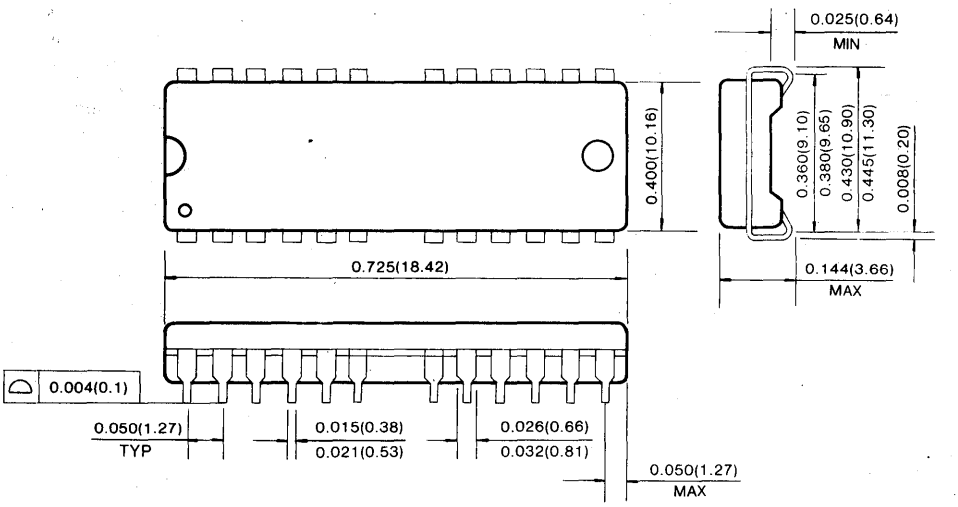


SAMSUNG ELECTRONICS

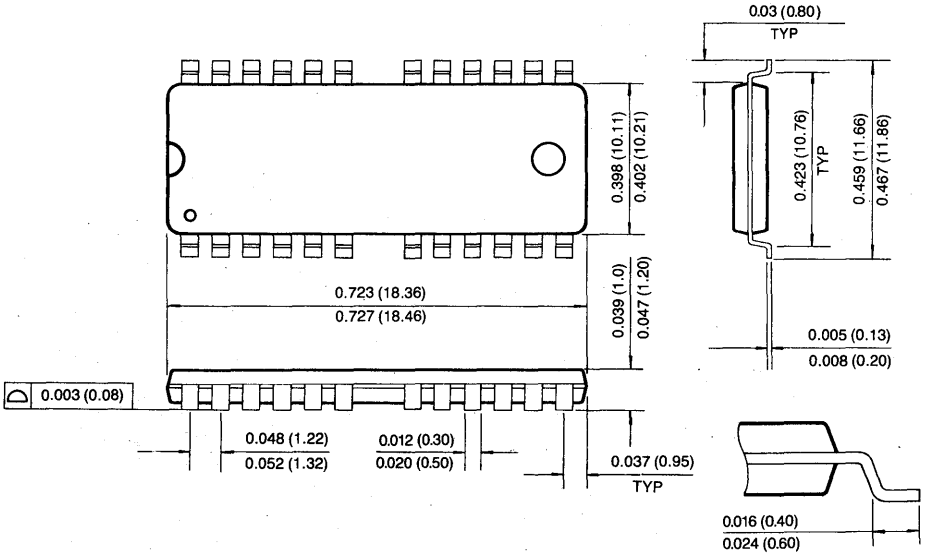
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M ×4 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM44C4102A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4102A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4102A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4102A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Self Refresh Operation (LL-ver. only)**
- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V±10% power supply**
- **2048 cycles/32ms refresh (Normal)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

The Samsung KM44C4102A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4102A/AL/ALL/ASL features Static Column Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C4102A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

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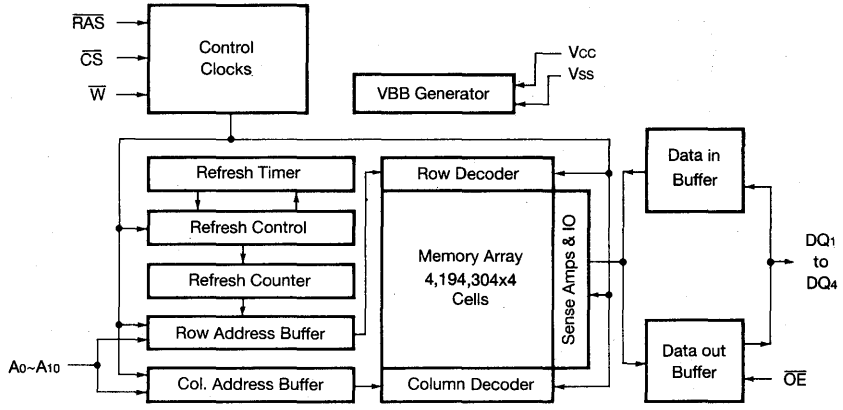
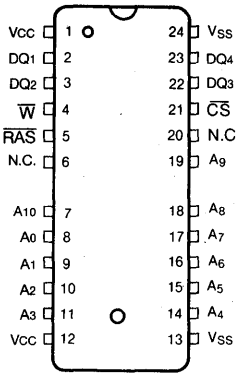
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

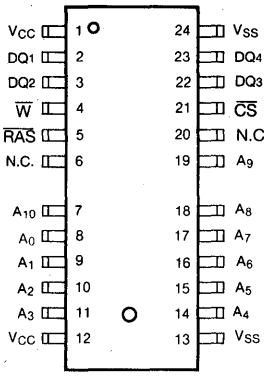
PIN CONFIGURATION (Top Views)

• **KM44C4102 AJ/ALJ/ALLJ/ASLJ**
AK/ALK/ALLK/ASLK



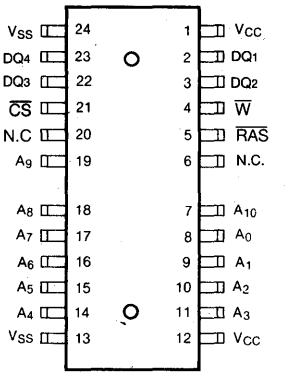
J : 400MIL
K : 300MIL

• **KM44C4102 AT/ALT/ALLT/ASLT**
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S: 300MIL(Forward)

• **KM44C4102 ATR/ALTR/ALLTR/ASLTR**
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
$DQ_{1\sim4}$	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select input
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC}=min.)	KM44C4102A/AL/ALL/ASL-5	I_{CC1}	-	110	mA
	KM44C4102A/AL/ALL/ASL-6			100	mA
	KM44C4102A/AL/ALL/ASL-7			90	mA
	KM44C4102A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{IH})	KM44C4102A	I_{CC2}	-	2	mA
	KM44C4102AL			1	mA
	KM44C4102ALL			1	mA
	KM44C4102ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44C4102A/AL/ALL/ASL-5	I_{CC3}	-	110	mA
	KM44C4102A/AL/ALL/ASL-6			100	mA
	KM44C4102A/AL/ALL/ASL-7			90	mA
	KM44C4102A/AL/ALL/ASL-8			80	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CS}$, Address Cycling @t_{PC}=min.)	KM44C4102A/AL/ALL/ASL-5	I_{CC4}	-	90	mA
	KM44C4102A/AL/ALL/ASL-6			80	mA
	KM44C4102A/AL/ALL/ASL-7			70	mA
	KM44C4102A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{CC}-0.2V)	KM44C4102A	I_{CC5}	-	1	mA
	KM44C4102AL			300	μA
	KM44C4102ALL			200	μA
	KM44C4102ASL			200	μA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC}=min.)	KM44C4102A/AL/ALL/ASL-5	I_{CC6}	-	110	mA
	KM44C4102A/AL/ALL/ASL-6			100	mA
	KM44C4102A/AL/ALL/ASL-7			90	mA
	KM44C4102A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CS}$=$\overline{CS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ1~DQ4=Don't Care t_{RC}=62.5μs(L-Ver.) 125μs(SL-Ver.), t_{RAS}=t_{RAS} min~300ns	KM44C4102AL	I_{CC7}	-	400	μA
	KM44C4102ASL			300	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{10}=V_{CC}-0.2V or 0.2V DQ_1-DQ_4=V_{CC}-0.2V, 0.2V or Open	KM44C4102ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤5.5V)		I_{OL}	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one Static Column cycle.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{10})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CS}$ pulse width	t_{CS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		50		55		60		ns	6
Refresh period (Normal)	t_{REF}		32		32		32		32	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CS}$ set-up time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Static column mode cycle time	t_{SC}	30		35		40		45		ns	3
Static column mode read-write cycle time	t_{SRWC}	80		85		100		110		ns	
Access time from last write	t_{ALW}		50		55		65		75	ns	3, 12
Output data hold time from column address	t_{AOH}	5		5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		35		40		45		55	ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{CS}$ pulse width (Static column mode)	t_{CSC}	13	200000	15	200000	20	200000	20	200000	ns	
$\overline{CS}$ precharge time (Static column mode)	t_{CP}	10		10		10		10		ns	
Column address hold time referenced to $\overline{RAS}$ rising	t_{AH}	5		5		5		5		ns	
Last write to column address delay time	t_{LWAD}	20	25	20	25	25	30	25	35	ns	
Last write to column address hold time	t_{AHLW}	50		55		65		75		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command inactive time	t_{WI}	10		10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	13		15		20		20		ns	
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	40		45		55		60		ns	6
$\overline{OE}$ access time	t_{OEA}		13		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	13		15		20		20		ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	90		110		130		150		ns	15
$\overline{CS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	95		115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	140		160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		55		65		75		85	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		18		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CS}$ pulse width	t_{CS}	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		25		ns	
$\overline{CS}$ hold time	t_{CSH}	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		45		ns	
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	45		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	80		90		105		115		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		60		70		75		ns	8
Static column mode cycle time	t_{SC}	35		40		45		50		ns	
Static column mode read-write cycle time	t_{SRWC}	85		90		105		110		ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from last write	t_{ALW}		55		60		70		80	ns	3,12
$\overline{OE}$ access time	t_{OEA}		18		20		25		25	ns	
$\overline{OE}$ to data delay	t_{OED}	18		20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	18		20		25		25		ns	

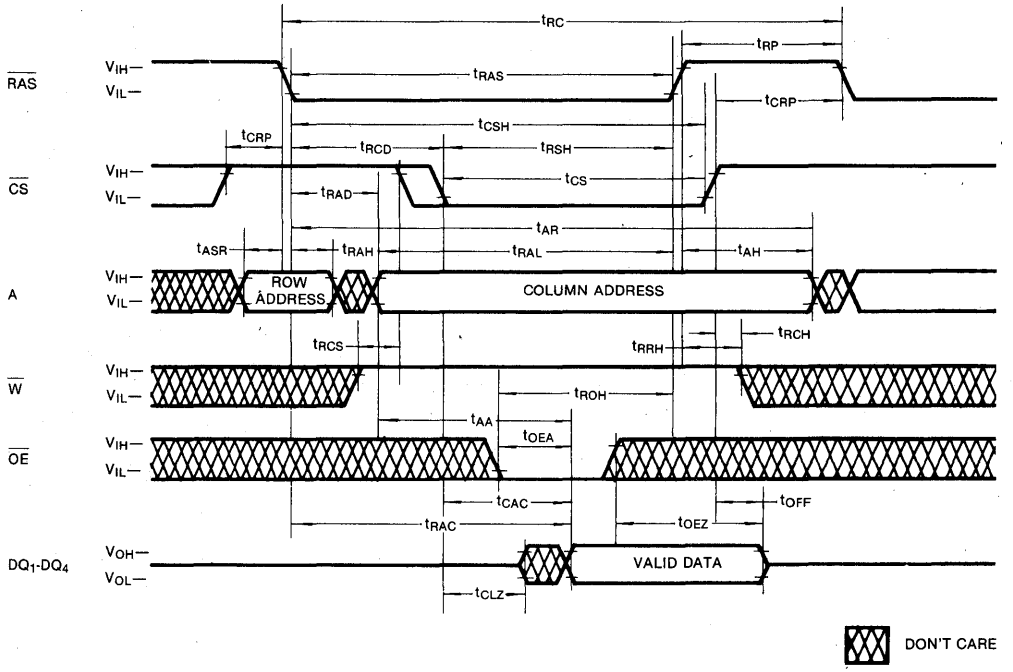
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data output is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

5

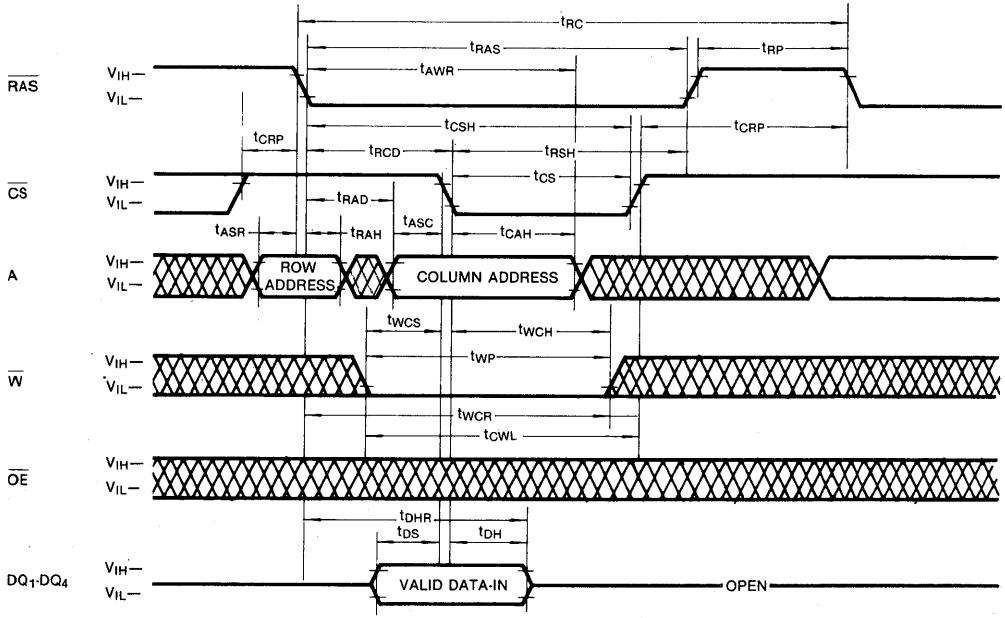
TIMING DIAGRAMS

READ CYCLE

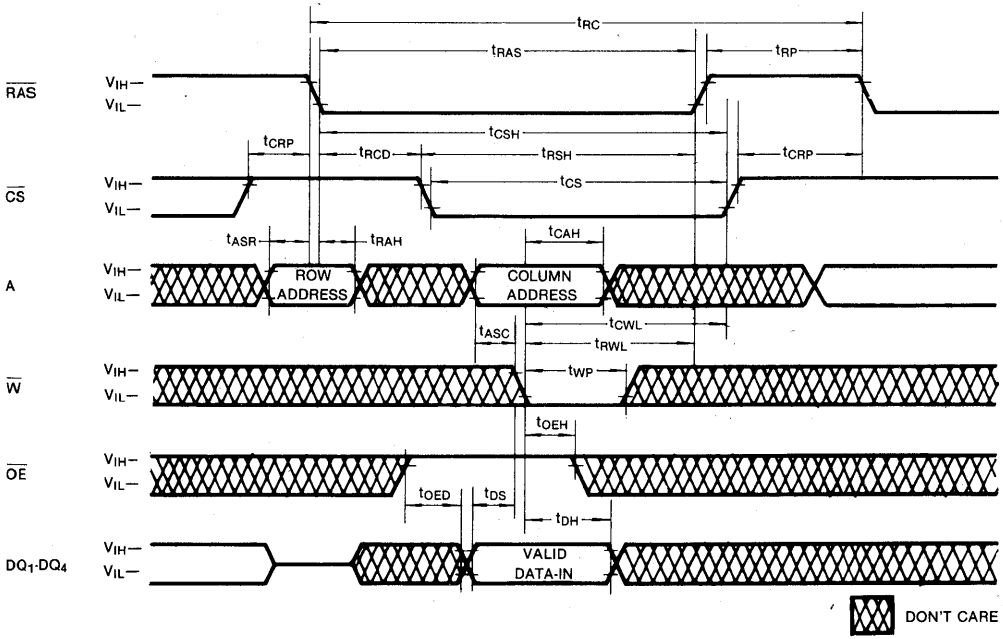


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

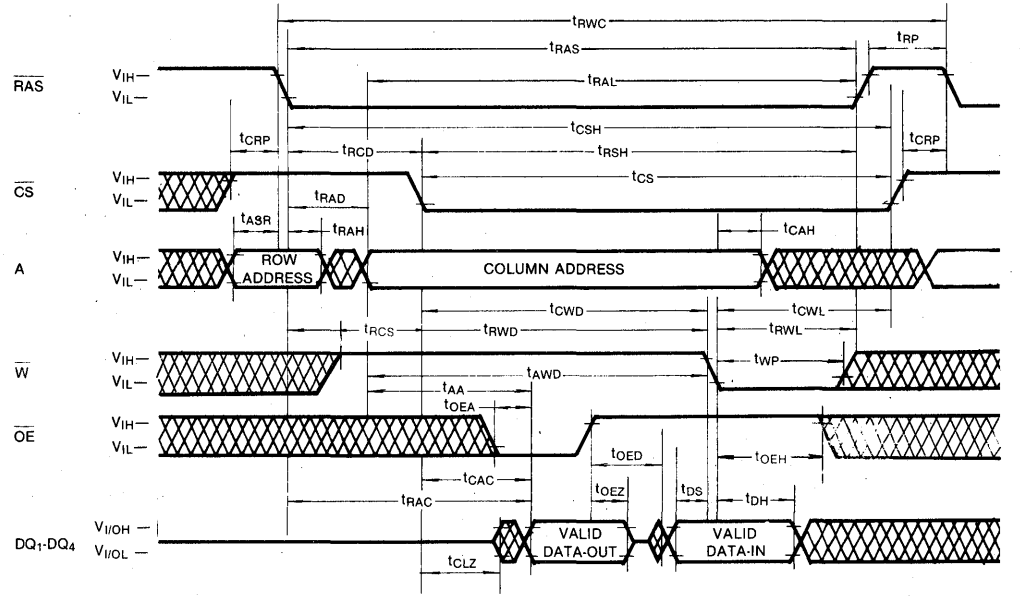


WRITE CYCLE (OE CONTROLLED WRITE)

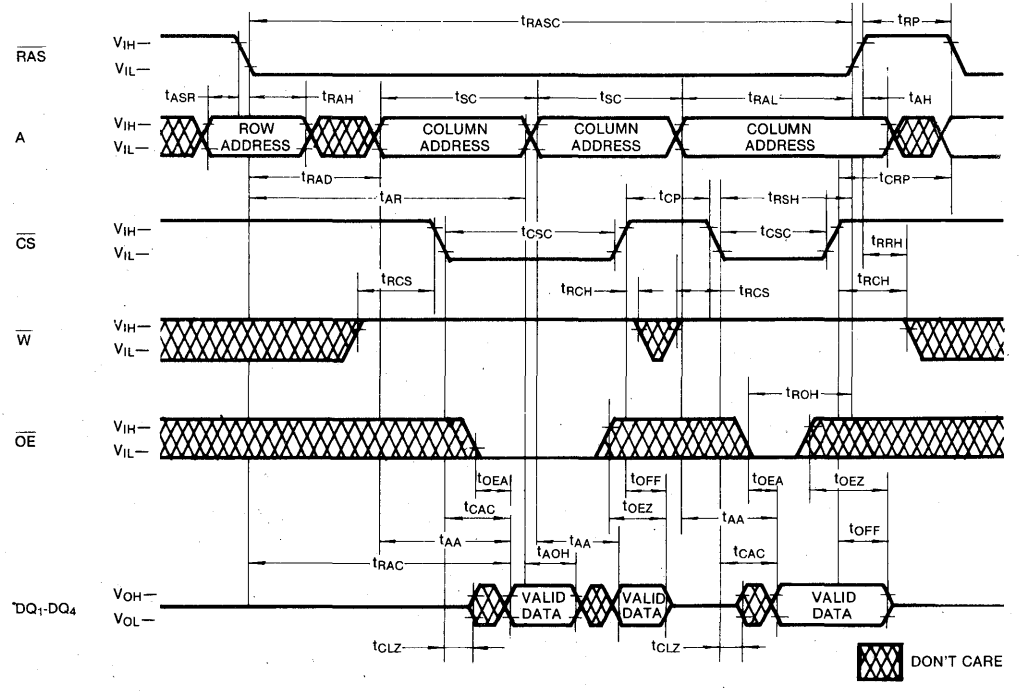


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

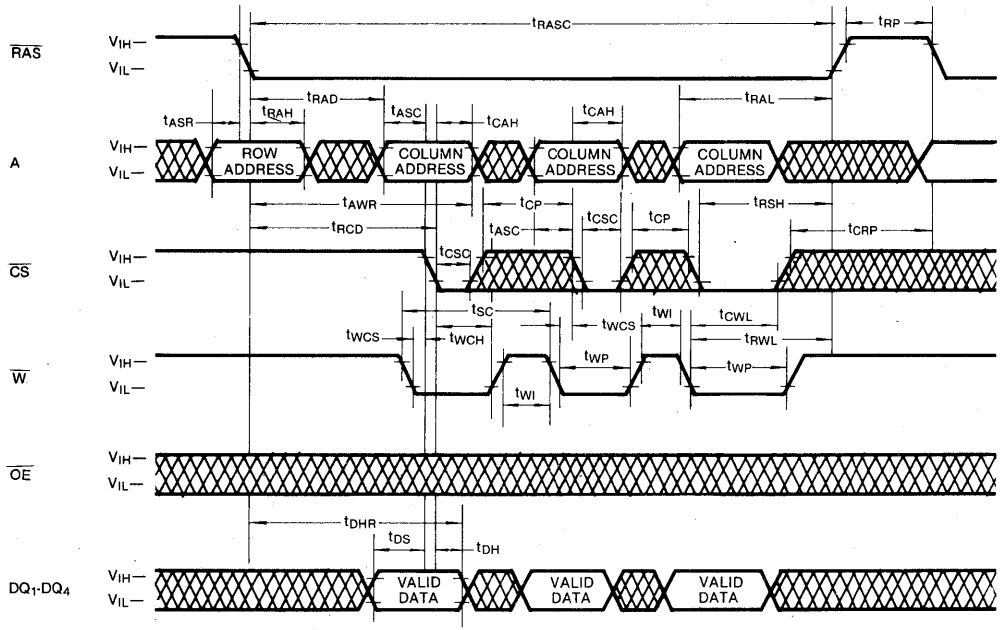


STATIC COLUMN MODE READ CYCLE

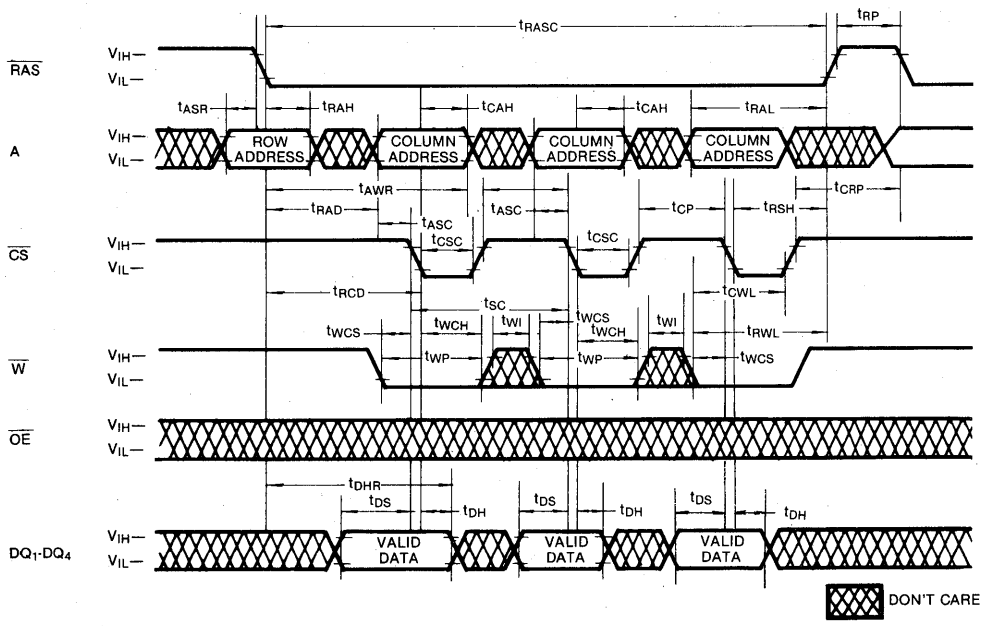


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ controlled early write)



STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)



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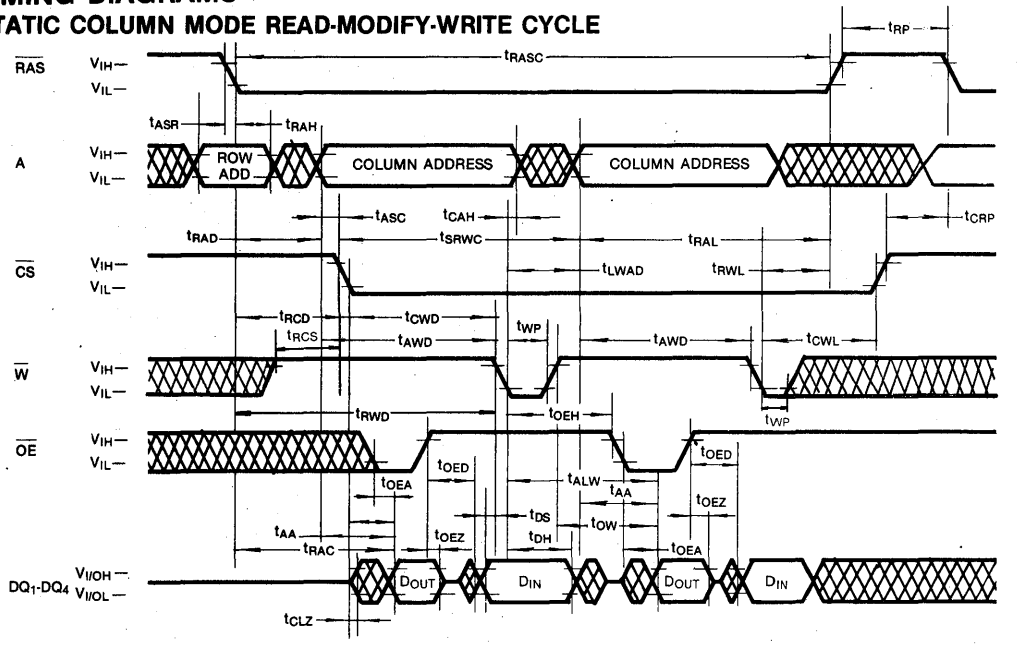
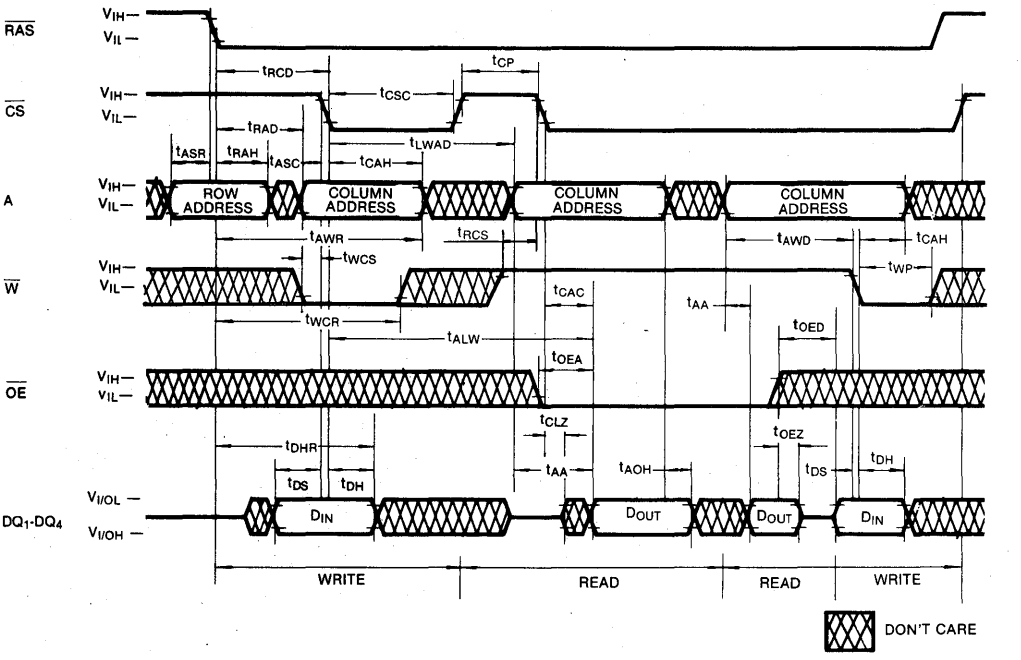
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE MIXED CYCLE

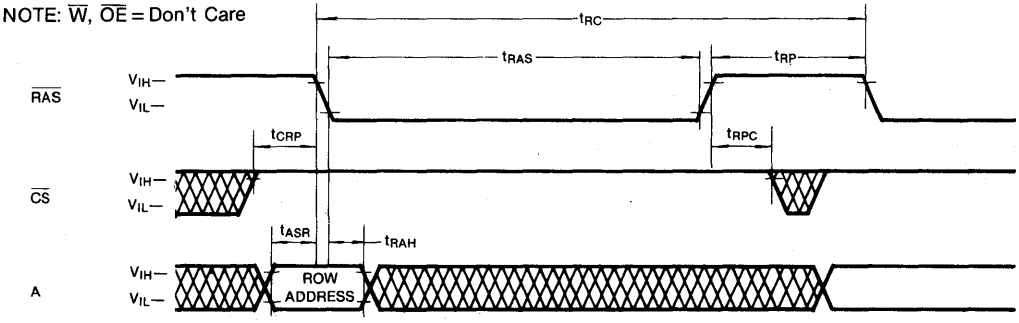


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

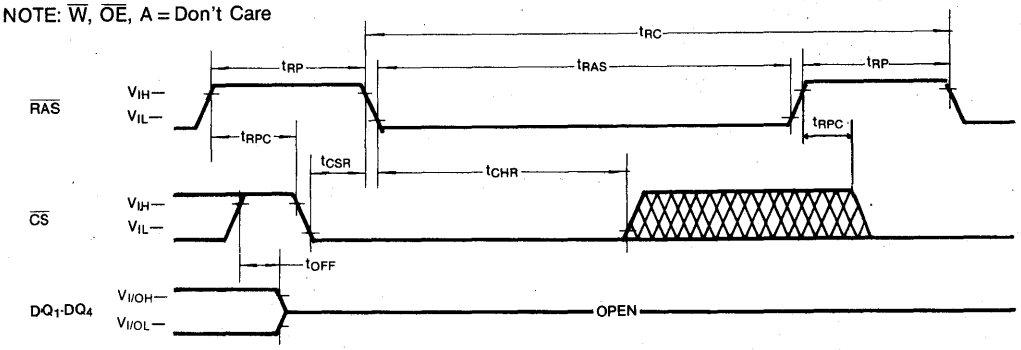
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$ = Don't Care



$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care



DON'T CARE

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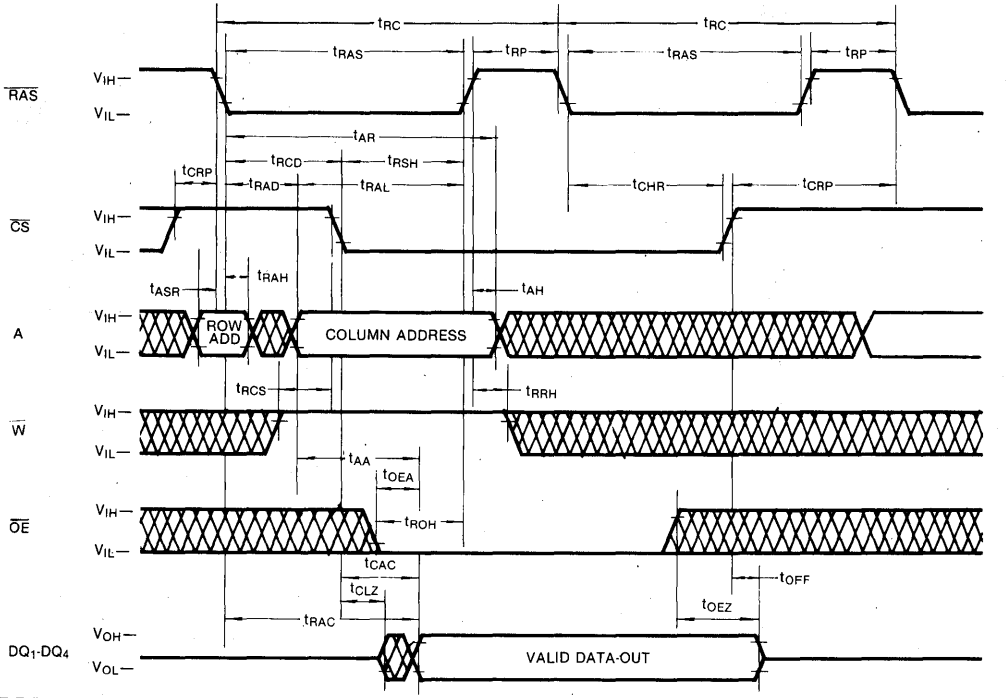
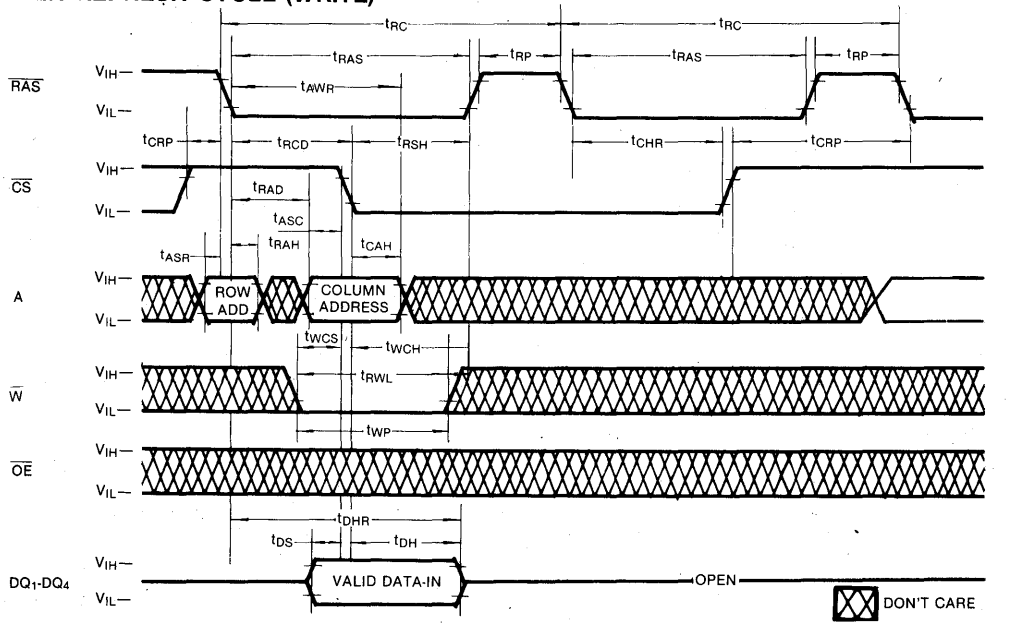
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



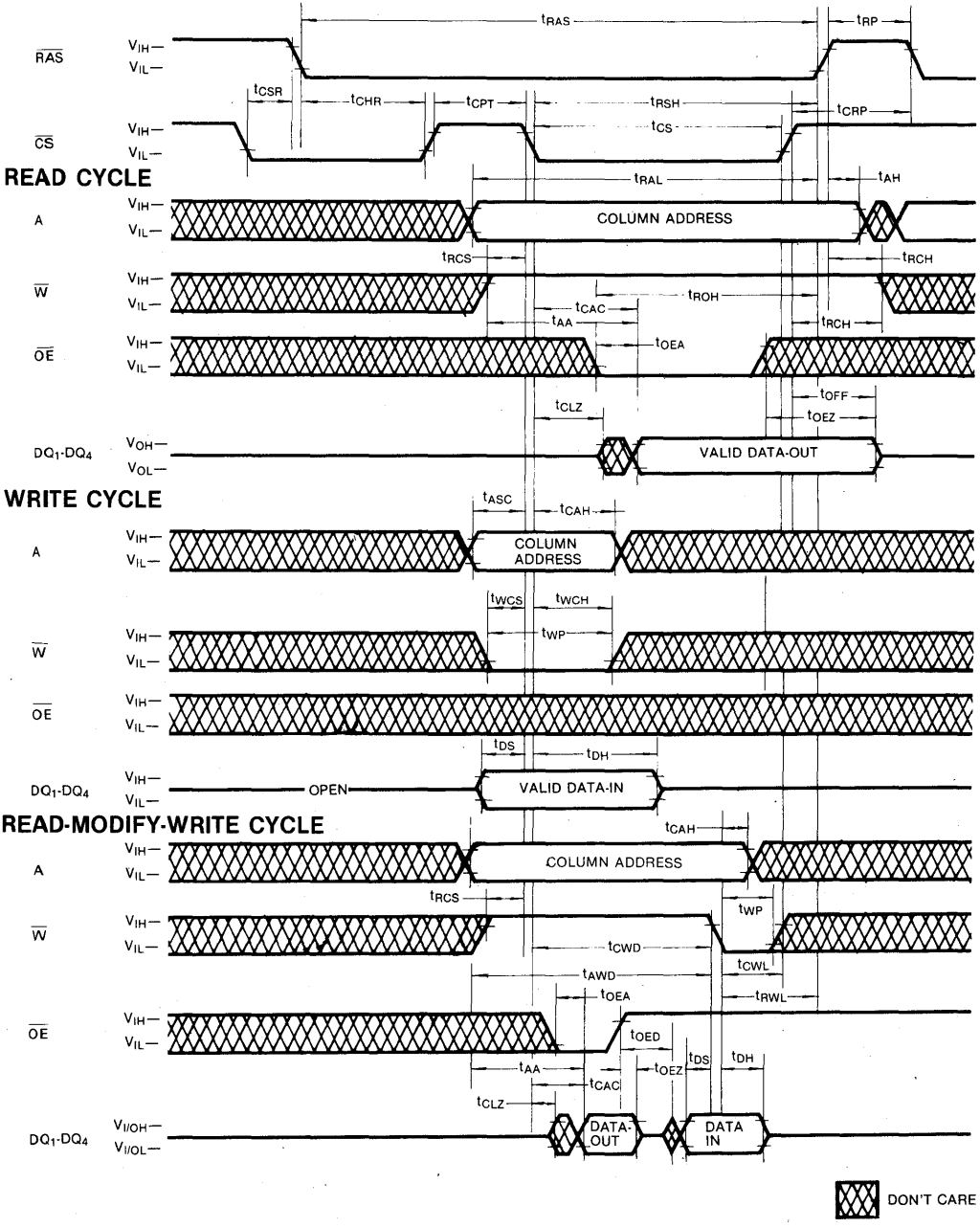
HIDDEN REFRESH CYCLE (WRITE)



SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

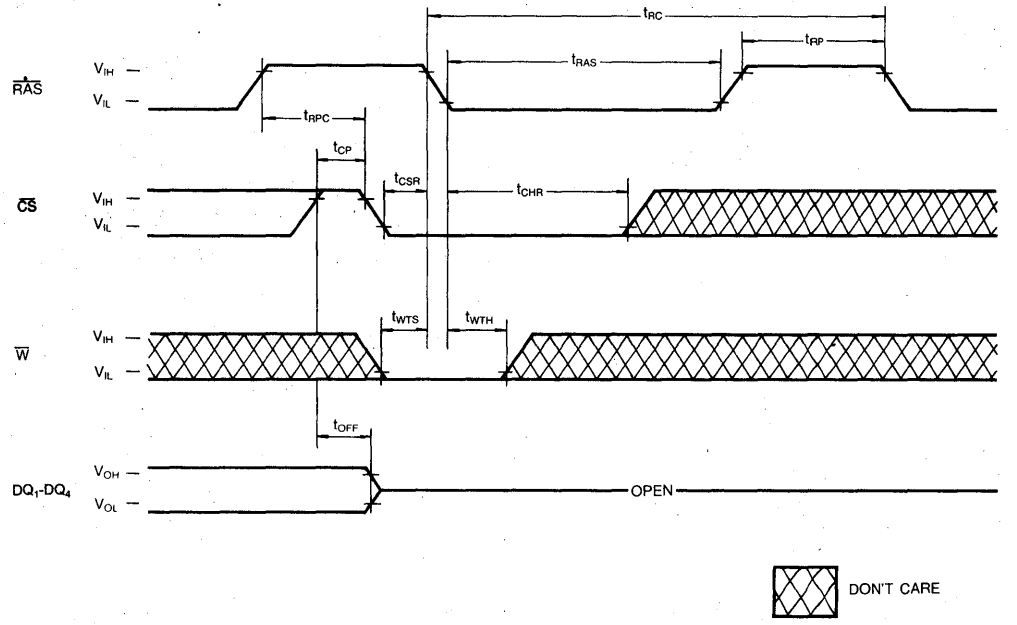
CS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



TEST MODE DESCRIPTION

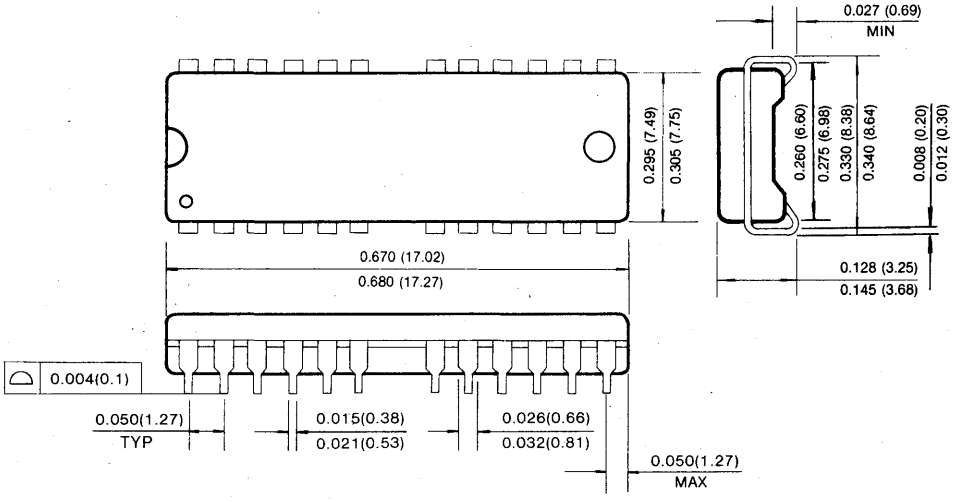
The KM44C4102 is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0, A_1, are not used. If, upon reading, 16 bits are equal (all "1" or "O"s) the Q pin indicates a "1".
If they were not equal, the Q pin would indicate a "0".

In "Test Mode", the 16M DRAM can be tested as if it were a 1M × 4 DRAM. $\overline{W}$, $\overline{CS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And $\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE "or" $\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



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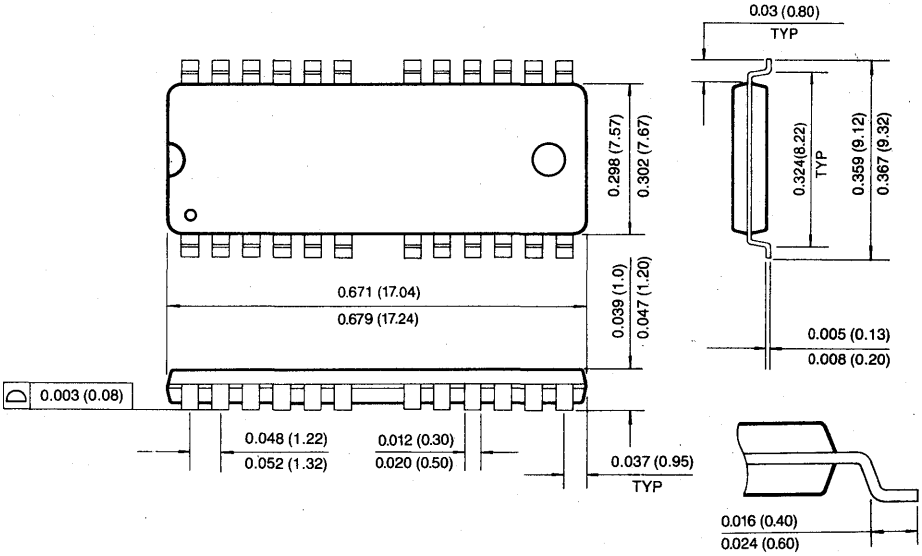
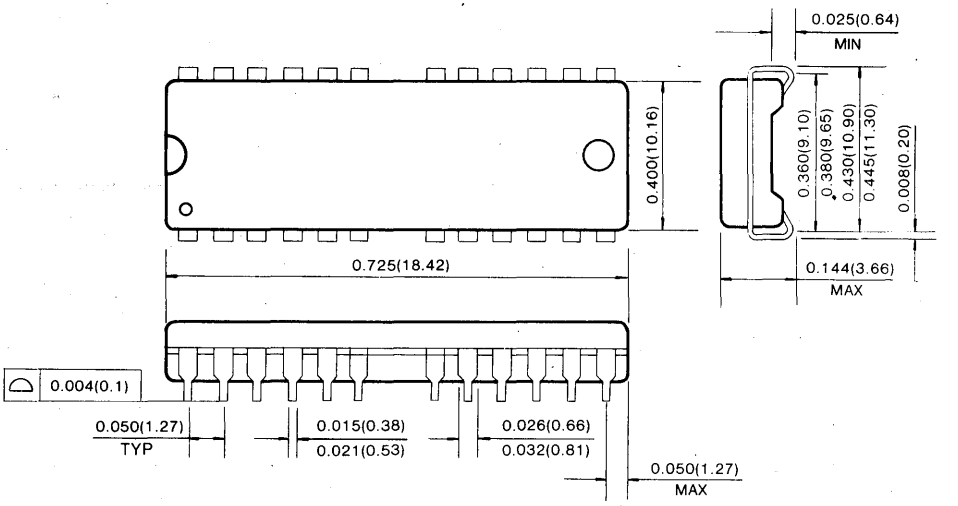
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



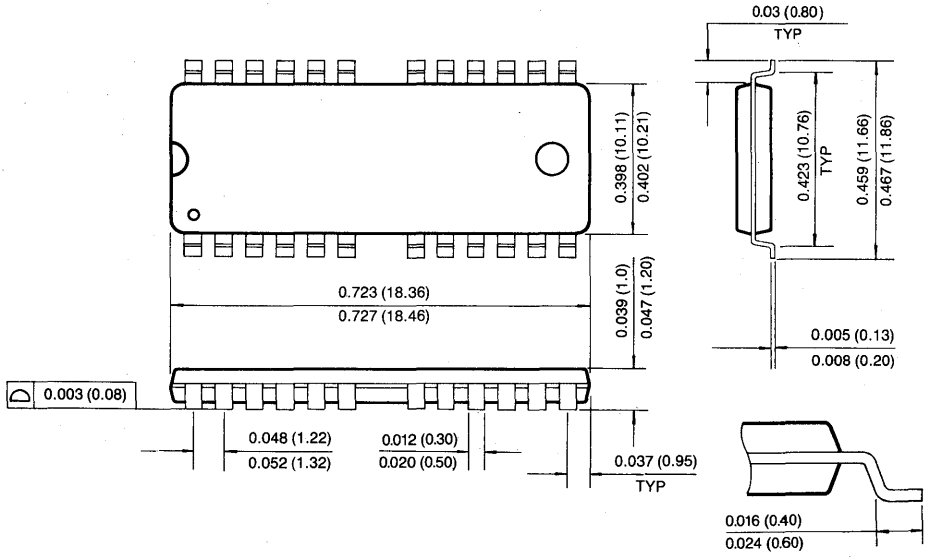
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M ×4 Bit CMOS Quad CAS DRAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM44C4003A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4003A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4003A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4003A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Self Refresh Operation (LL-ver. only)**
- **Four separate $\overline{CAS}$ pins provide for separate I/O operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V±10% power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

The Samsung KM44C4003A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4003A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible and four separate $\overline{CAS}$ pins provide for separate I/O operation allowing this device to operate in parity mode.

The KM44C4003A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

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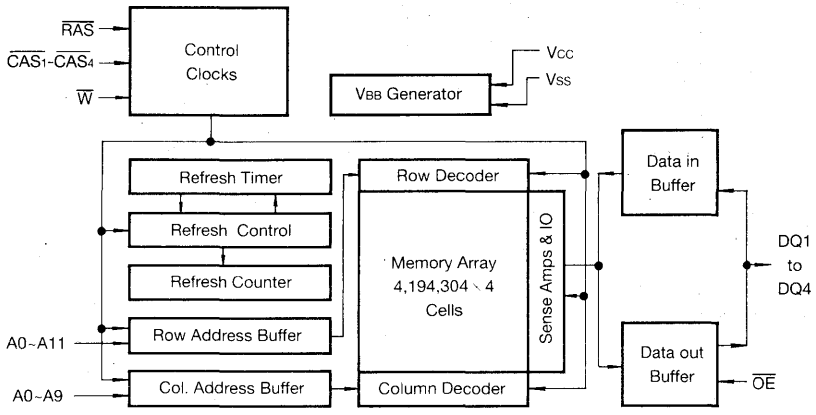
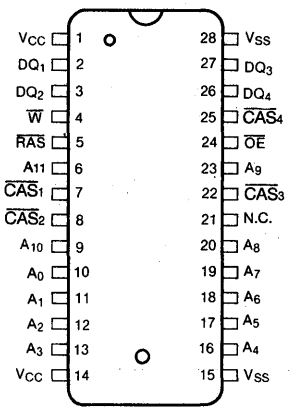
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

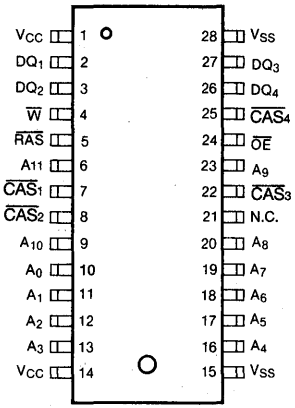
PIN CONFIGURATION (Top Views)

• KM44C4003 AJ/ALJ/ALLJ/ASLJ



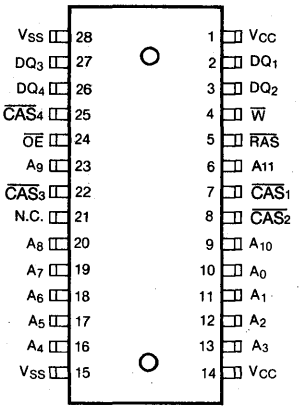
J : 400MIL

• KM44C4003 AT/ALT/ALLT/ASLT



T : 400MIL(Forward)

• KM44C4003 ATR/ALTR/ALLTR/ASLTR



TR : 400MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1~4	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}_1$~$\overline{CAS}_4$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VCC	Power(+5.0V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4003A/AL/ALL/ASL-5	I_{CC1}	-	90	mA
	KM44C4003A/AL/ALL/ASL-6			80	mA
	KM44C4003A/AL/ALL/ASL-7			70	mA
	KM44C4003A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44C4003A	I_{CC2}	-	2	mA
	KM44C4003AL			1	mA
	KM44C4003ALL			1	mA
	KM44C4003ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44C4003A/AL/ALL/ASL-5	I_{CC3}	-	90	mA
	KM44C4003A/AL/ALL/ASL-6			80	mA
	KM44C4003A/AL/ALL/ASL-7			70	mA
	KM44C4003A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44C4003A/AL/ALL/ASL-5	I_{CC4}	-	80	mA
	KM44C4003A/AL/ALL/ASL-6			70	mA
	KM44C4003A/AL/ALL/ASL-7			60	mA
	KM44C4003A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM44C4003A	I_{CC5}	-	1	mA
	KM44C4003AL			300	μA
	KM44C4003ALL			200	μA
	KM44C4003ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4003A/AL/ALL/ASL-5	I_{CC6}	-	90	mA
	KM44C4003A/AL/ALL/ASL-6			80	mA
	KM44C4003A/AL/ALL/ASL-7			70	mA
	KM44C4003A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ_1~DQ_4=Don't Care t_{RC}=31.25μs(L-Ver.) 62.5μs(SL-Ver.), t_{RAS}=t_{RAS}≦min~300ns	KM44C4003AL	I_{CC7}	-	450	μA
	KM44C4003ASL			350	μA

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DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{CC}-0.2V or 0.2V DQ_1-DQ_4=V_{CC}-0.2V, 0.2V or Open	KM44C4003ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}$+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±0.5V, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5,19
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3,19
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	0	20	ns	7,19
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	17
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	18
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	24
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4,17
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	18
Row address set-up time	t_{ASR}	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	17
Column address hold time	tCAH	10		10		15		15		ns	17
Column address hold time referenced to $\overline{RAS}$	tAR	40		50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	17
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	9,18
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	25
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	18
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64		64	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8,17
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	8,17
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	18
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3,19
Fast Page mode cycle time	tPC	35		40		45		50		ns	20
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	20
$\overline{CAS}$ precharge time (Fast Page mode)	tCP	10		10		10		10		ns	21
$\overline{RAS}$ pulse width(Fast Page mode)	tRASP	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	22
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	23
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	

5

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	15
Hold time $\overline{CAS}$ low to $\overline{CAS}$ high	tCLCH	5		5		5		5		ns	16

TEST MODE CYCLE

(Note.12)

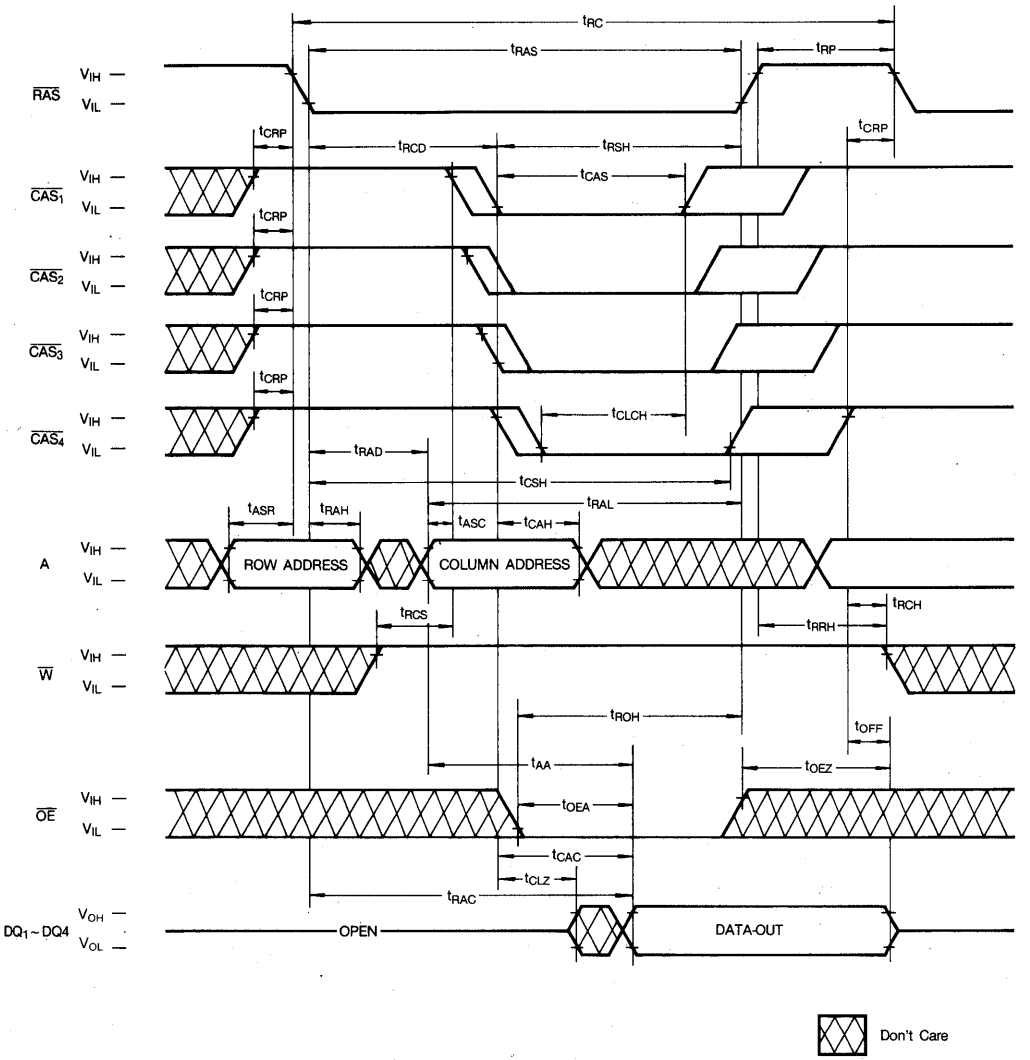
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11,13
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5,13
Access time from column address	tAA		30		35		40		45	ns	3,11,13
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. In order to hold the address latched by the first $\overline{CAS}$ going low. the parameter t_{CLCH} must be met.
17. The first $\overline{CASx}$ edge to transition low.
18. The last $\overline{CASx}$ edge to transition high.
19. Output parameter is referenced to corresponding $\overline{CASx}$ input.
20. Last rising $\overline{CASx}$ edge to next cycle's last rising $\overline{CASx}$ edge.
21. Last rising $\overline{CASx}$ edge to first falling $\overline{CAS}$ edge.
22. First DQx controlled by the first $\overline{CASx}$ to go low.
23. Last DQx controlled by the last $\overline{CASx}$ to go high.
24. Each $\overline{CASx}$ must meet minimum pulse width.
25. Last $\overline{CASx}$ to go low.

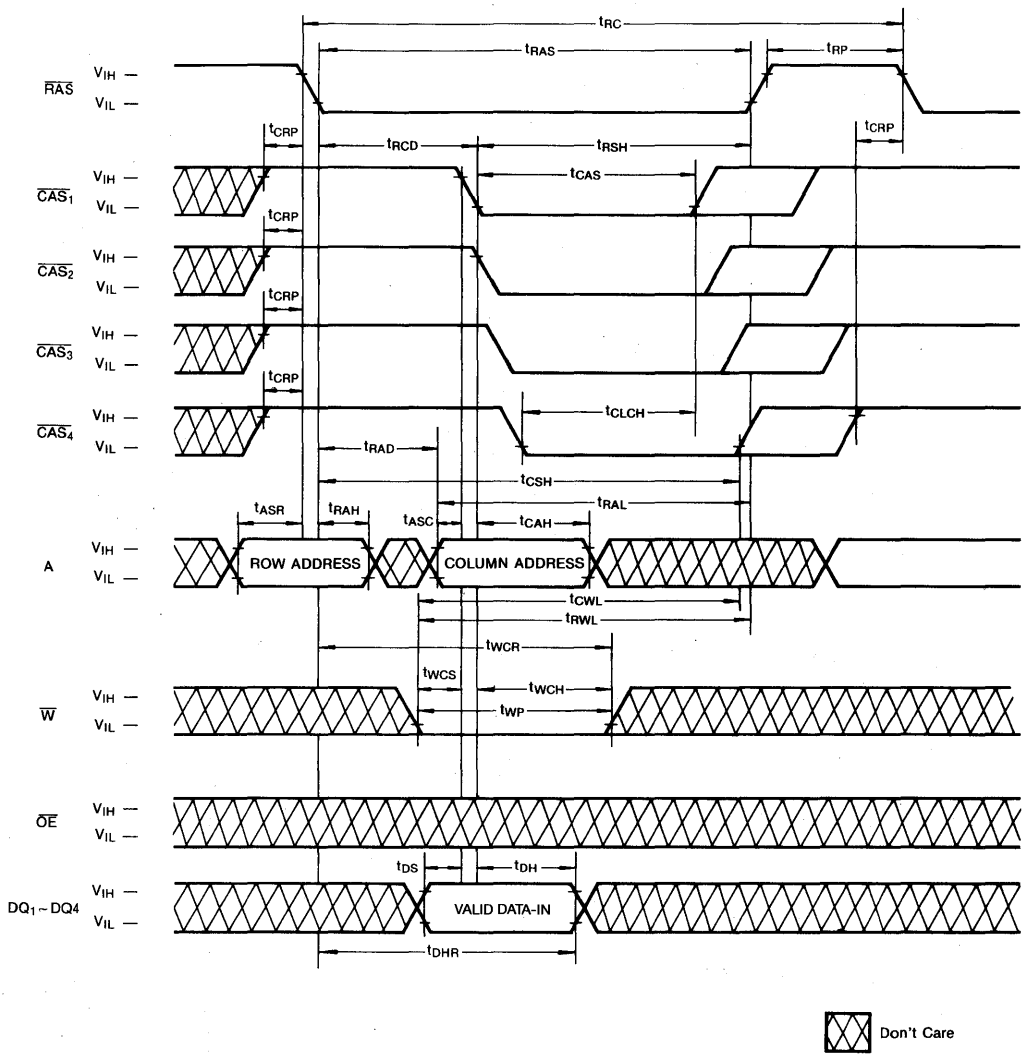
TIMING DIAGRAM

READ CYCLE



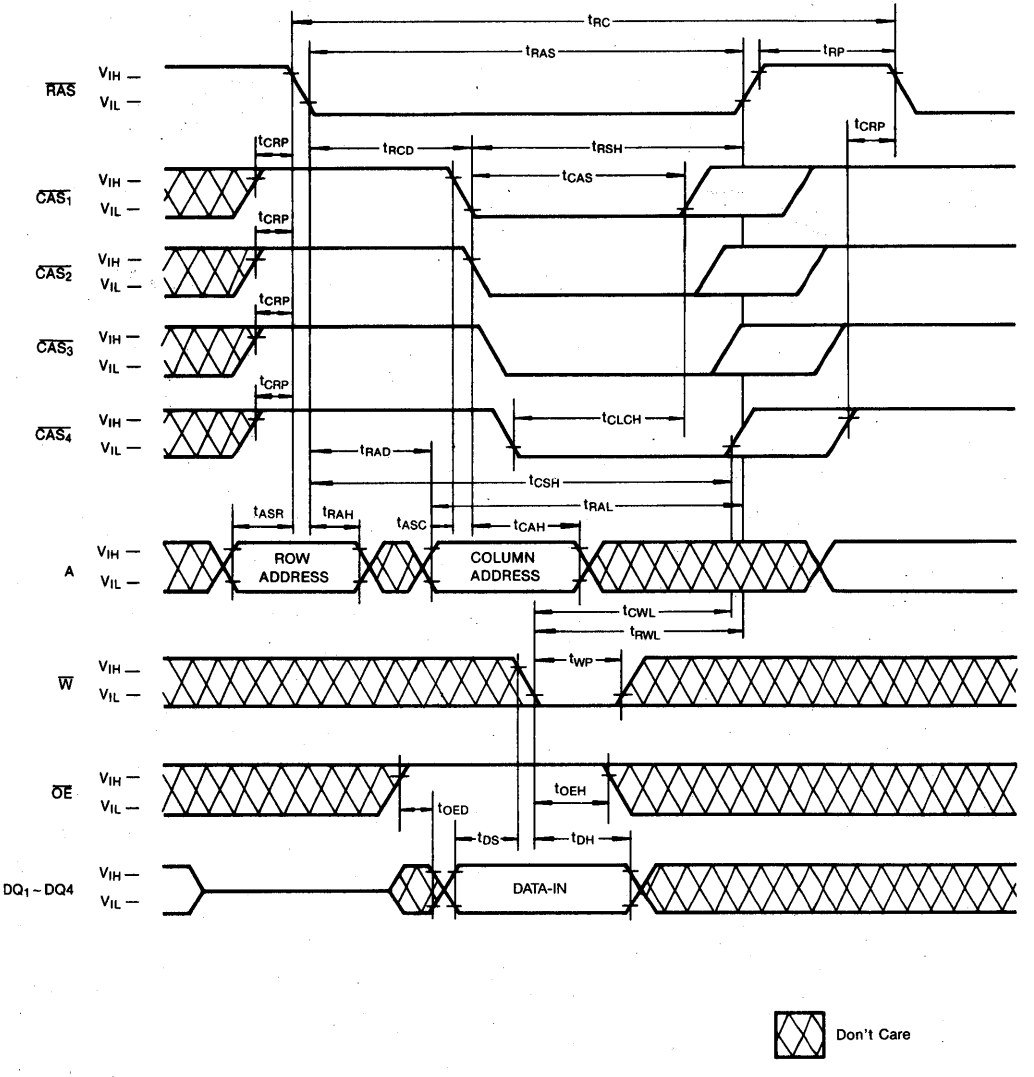
TIMING DIAGRAM (Continued)

WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAM (Continued)

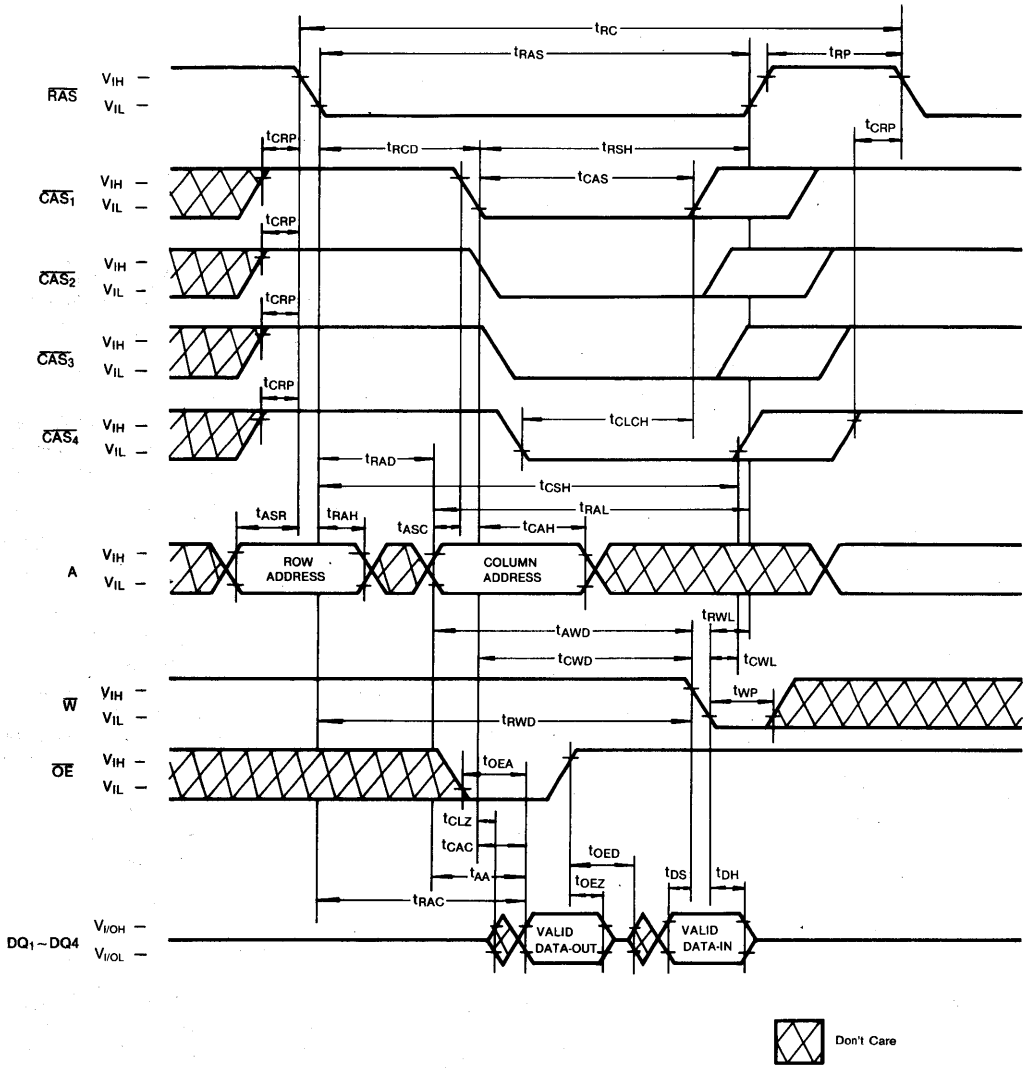
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



SAMSUNG ELECTRONICS

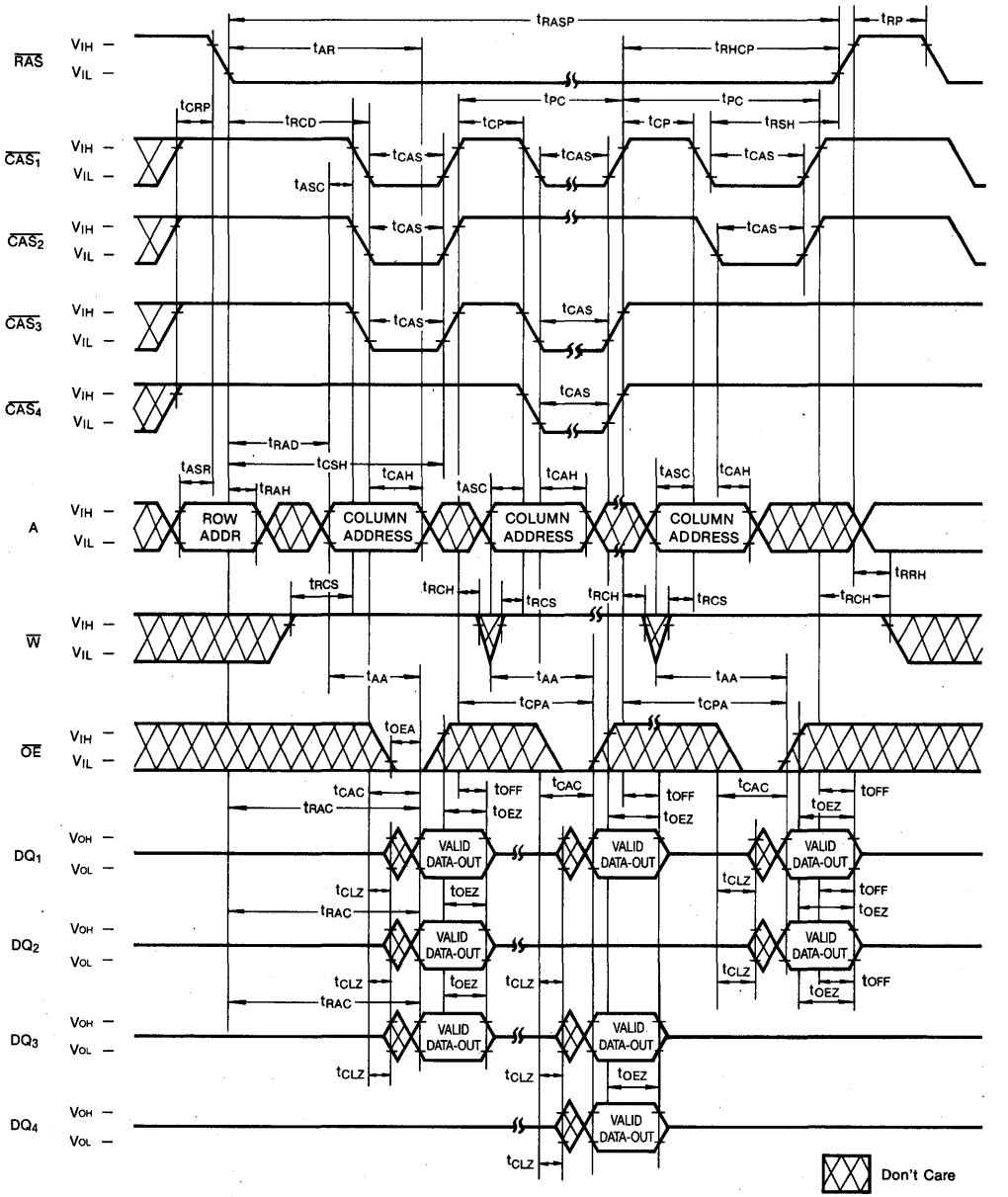
TIMING DIAGRAM (Continued)

READ-MODIFY-WRITE CYCLE



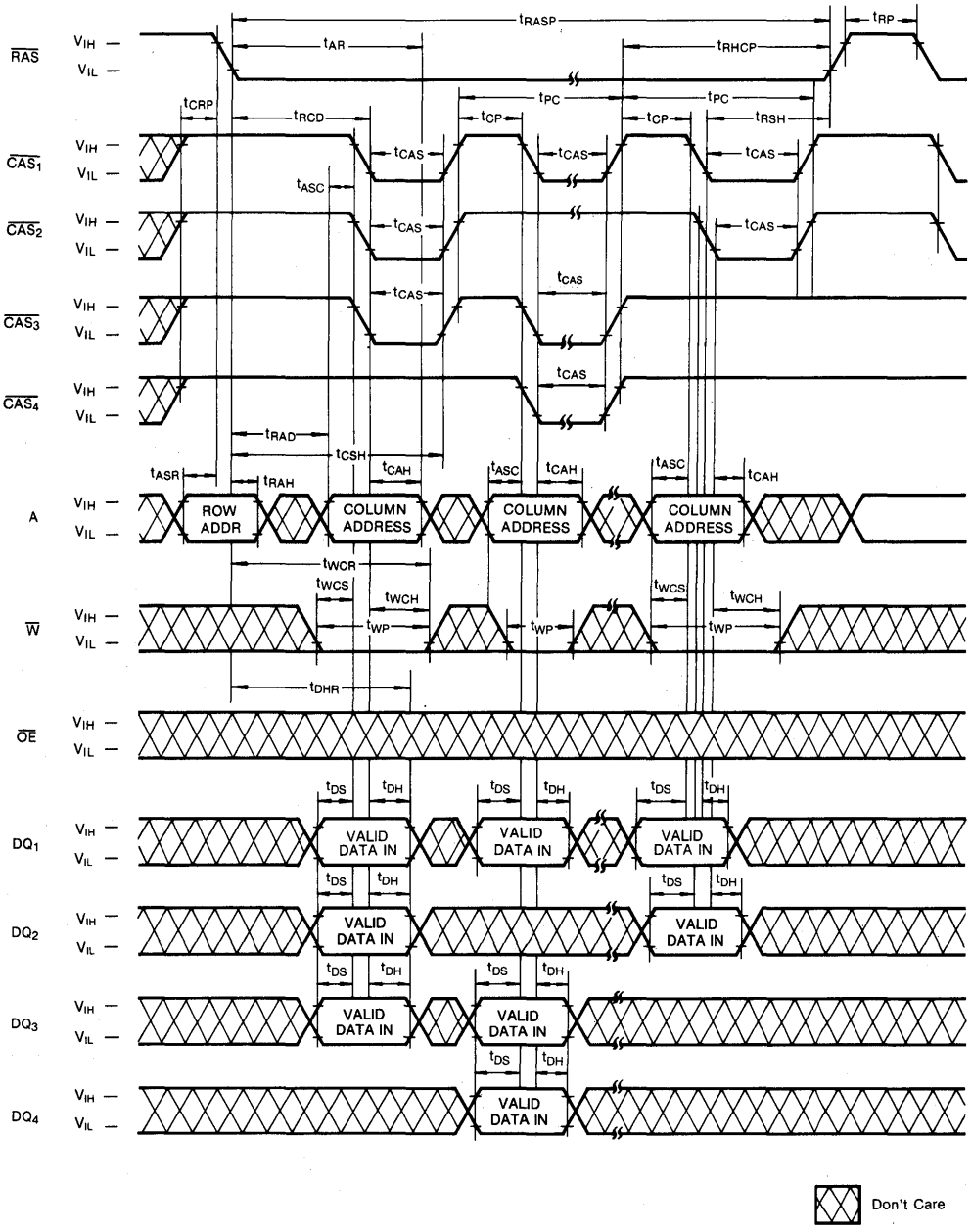
TIMING DIAGRAM (Continued)

FAST PAGE MODE READ CYCLE



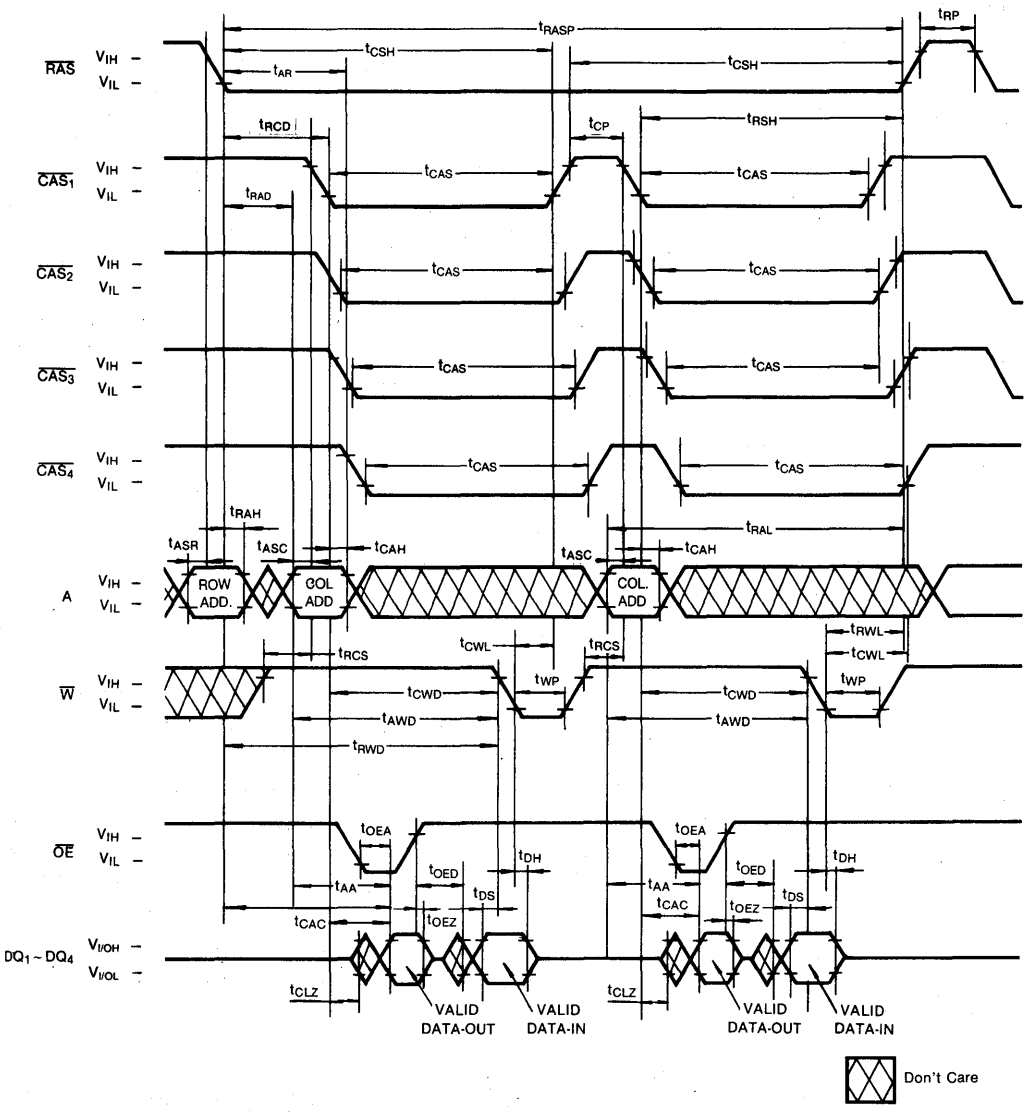
TIMING DIAGRAM (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAM (Continued)

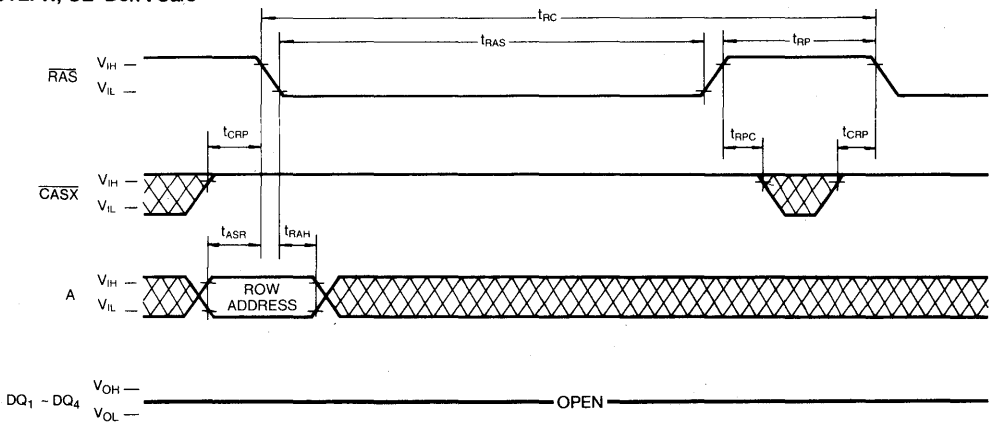
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

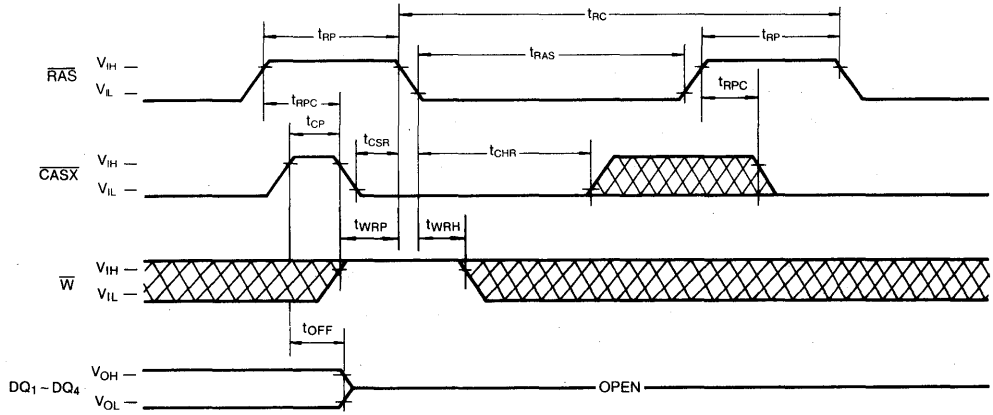
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

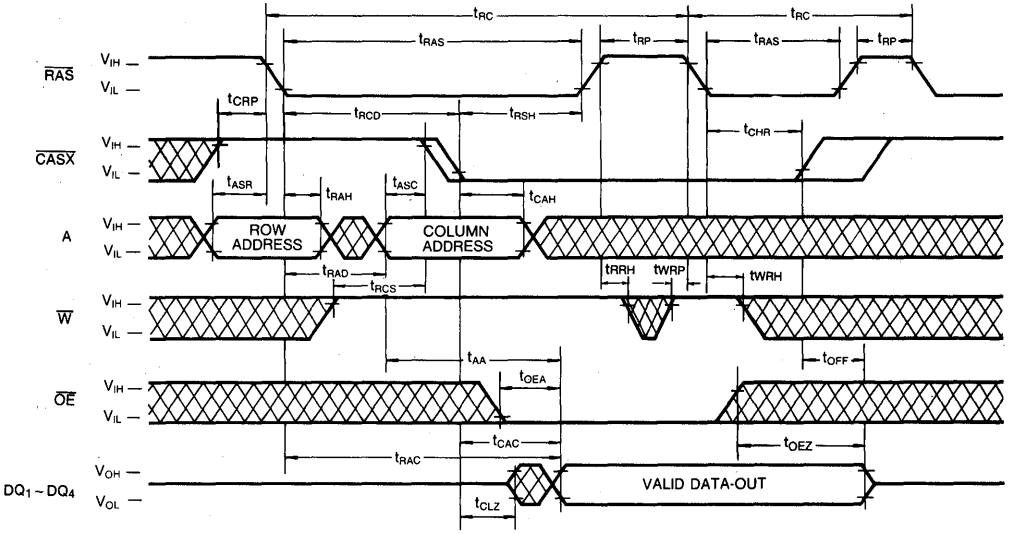
NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care



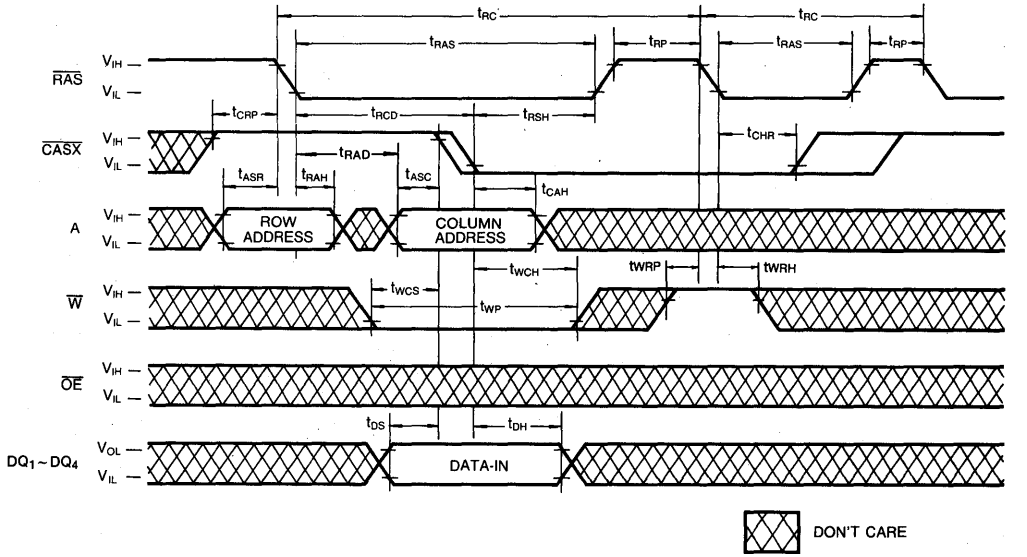
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

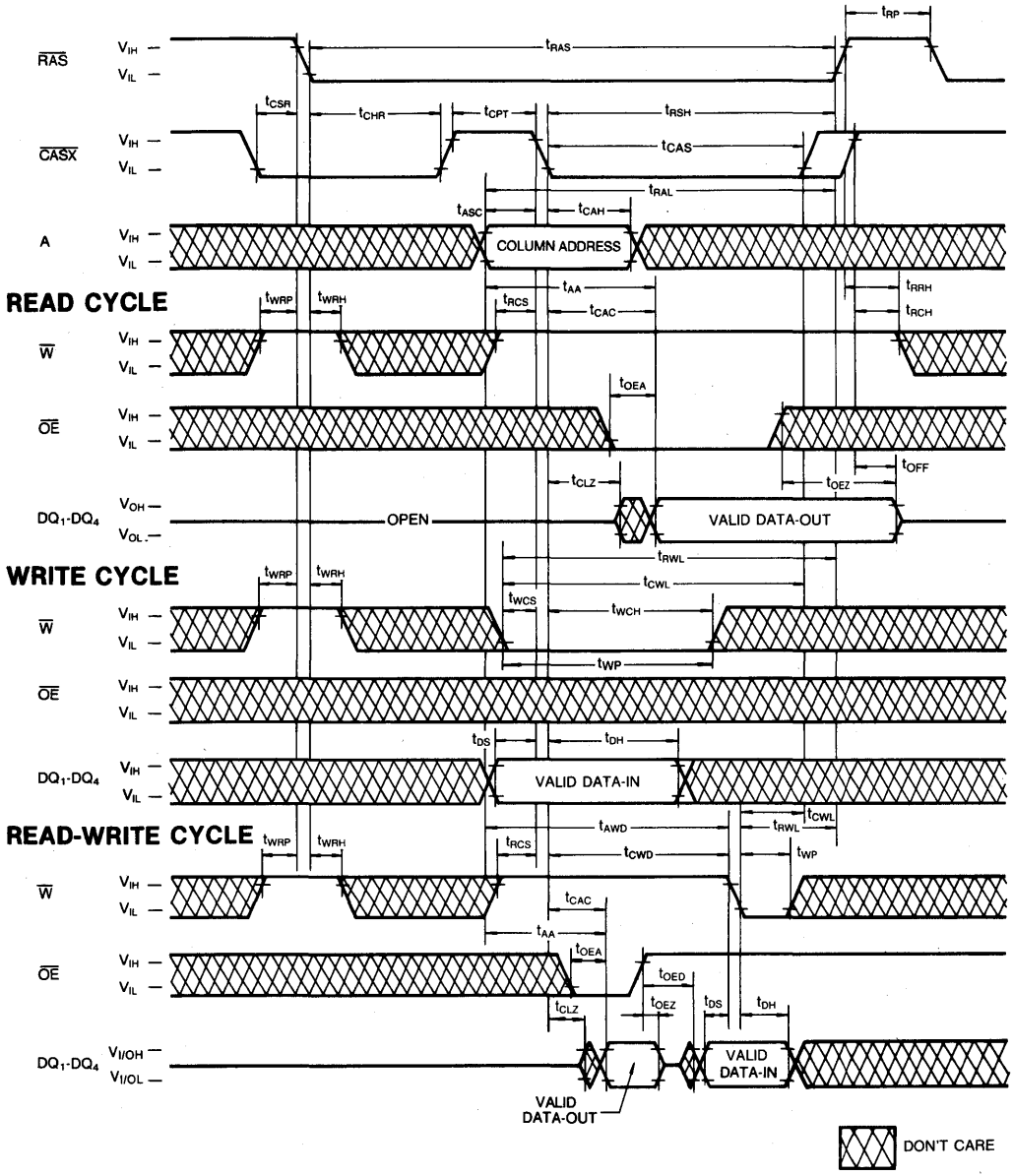


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

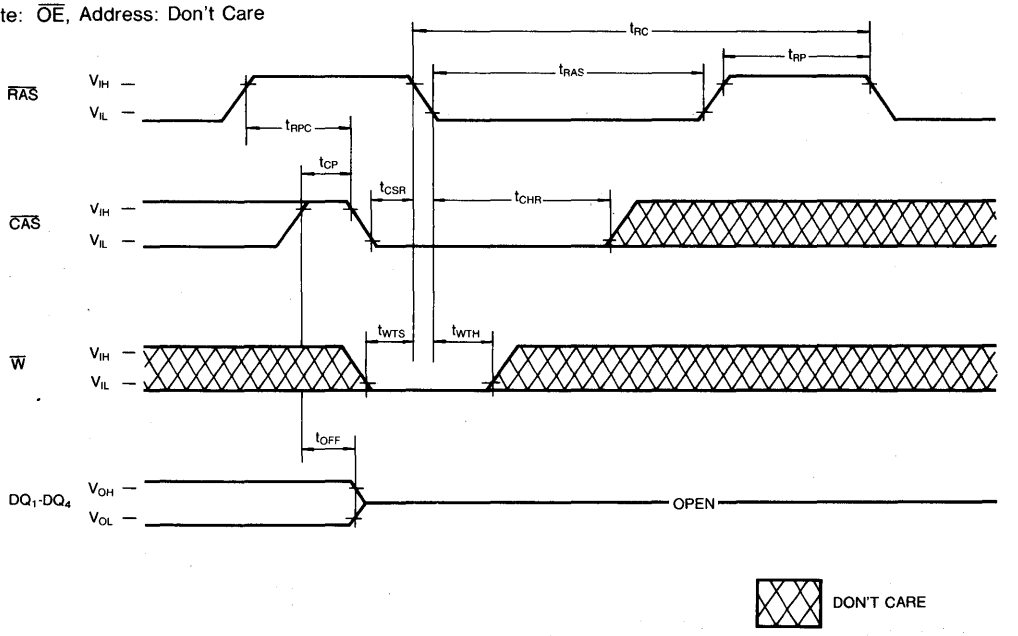
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

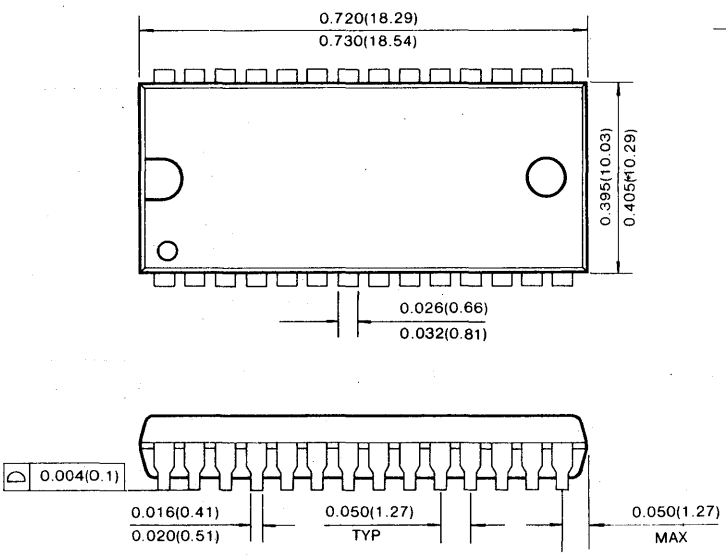
Note: $\overline{OE}$, Address: Don't Care



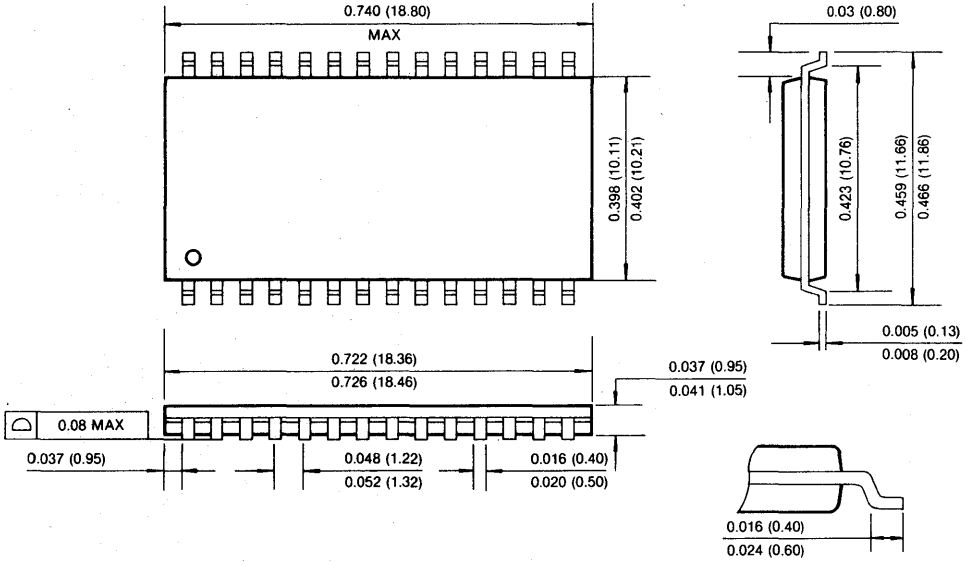
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



4M ×4 Bit CMOS Quad CAS DRAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM44C4103A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4103A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4103A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4103A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Self Refresh Operation (LL-ver, only)**
- **Four separate $\overline{CAS}$ pins provide for separate I/O operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V±10% power supply**
- **2048 cycles/32ms refresh (Normal)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

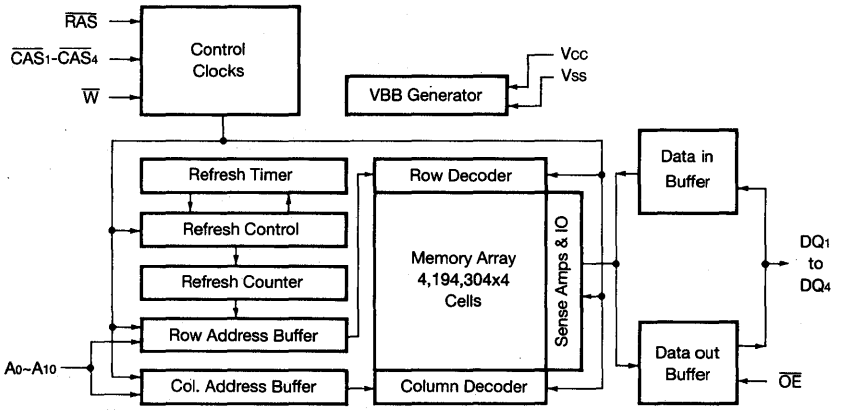
The Samsung KM44C4103A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4103A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.and four separate $\overline{CAS}$ pins provide for separate I/O operation allowing this device to operate in parity mode.

The KM44C4103A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

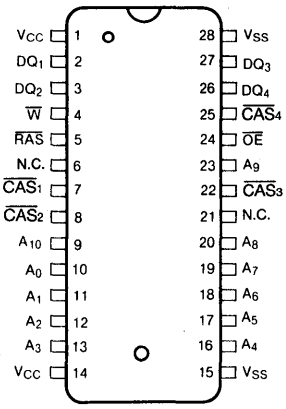
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

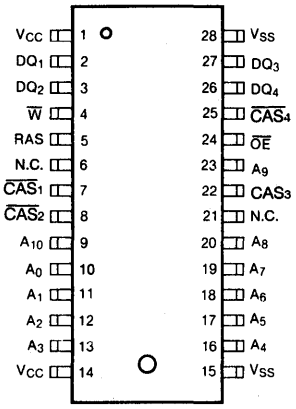
PIN CONFIGURATION (Top Views)

• KM44C4103 AJ/ALJ/ALLJ/ASLJ



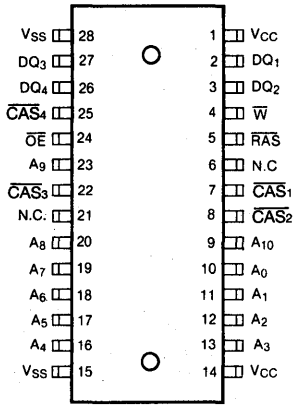
J : 400MIL

• KM44C4103 AT/ALT/ALLT/ASLT



T : 400MIL(Forward)

• KM44C4103 ATR/ALTR/ALLTR/ASLTR



TR : 400MIL(Reverse)

Pin Name	Pin Function
A0-A10	Address Inputs
DQ1~4	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS1}$~$\overline{CAS4}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VCC	Power(+5.0V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4103A/AL/ALL/ASL-5	I_{CC1}	-	110	mA
	KM44C4103A/AL/ALL/ASL-6			100	mA
	KM44C4103A/AL/ALL/ASL-7			90	mA
	KM44C4103A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44C4103A	I_{CC2}	-	2	mA
	KM44C4103AL			1	mA
	KM44C4103ALL			1	mA
	KM44C4103ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44C4103A/AL/ALL/ASL-5	I_{CC3}	-	110	mA
	KM44C4103A/AL/ALL/ASL-6			100	mA
	KM44C4103A/AL/ALL/ASL-7			90	mA
	KM44C4103A/AL/ALL/ASL-8			80	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44C4103A/AL/ALL/ASL-5	I_{CC4}	-	90	mA
	KM44C4103A/AL/ALL/ASL-6			80	mA
	KM44C4103A/AL/ALL/ASL-7			70	mA
	KM44C4103A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM44C4103A	I_{CC5}	-	1	mA
	KM44C4103AL			300	μA
	KM44C4103ALL			200	μA
	KM44C4103ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4103A/AL/ALL/ASL-5	I_{CC6}	-	110	mA
	KM44C4103A/AL/ALL/ASL-6			100	mA
	KM44C4103A/AL/ALL/ASL-7			90	mA
	KM44C4103A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ1~DQ4=Don't Care t_{RC}=62.5μs(L-Ver.) 125μs(SL-Ver.), t_{RAS}=t_{RAS}≤min~300ns	KM44C4103AL	I_{CC7}	-	400	μA
	KM44C4103ASL			300	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{10}=V_{CC}-0.2V or 0.2V DQ_1-DQ_4=V_{CC}-0.2V, 0.2V or Open	KM44C4103ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{10})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±0.5V, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5,19
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3,19
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	0	20	ns	7,19
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	17
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	18
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	24
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4,17
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	18
Row address set-up time	t_{ASR}	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	17
Column address hold time	t_{CAH}	10		10		15		15		ns	17
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	17
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9,18
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		15		15		ns	25
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		20		20		ns	18
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		32		32		32		64	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8,17
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ns	8,17
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	18
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3,19
Fast Page mode cycle time	t_{PC}	35		40		45		50		ns	20
Fast Page mode read-modify-write cycle time	t_{PRWC}	76		85		100		105		ns	20
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		10		ns	21
$\overline{RAS}$ pulse width(Fast Page mode)	t_{RASP}	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		13		15		20		20	ns	22
$\overline{OE}$ to data delay	t_{OED}	13		15		20		20		ns	23
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	13		15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	90		110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	-50		-50		-50		-50		ns	15
Hold time $\overline{CAS}$ low to $\overline{CAS}$ high	t_{CLCH}	5		5		5		5		ns	16

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	95		115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	138		160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		55		65		75		85	ns	3,4,11,13
Access time from $\overline{CAS}$	t_{CAC}		18		20		25		25	ns	3,4,5,13
Access time from column address	t_{AA}		30		35		40		45	ns	3,11,13
$\overline{RAS}$ pulse width	t_{RAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	53		60		70		75		ns	8
Fast Page mode cycle time	t_{PC}	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45		50	ns	3
$\overline{OE}$ access time	t_{OEA}		18		20		25		25	ns	
$\overline{OE}$ to data delay	t_{OED}	18		20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	18		20		25		25		ns	

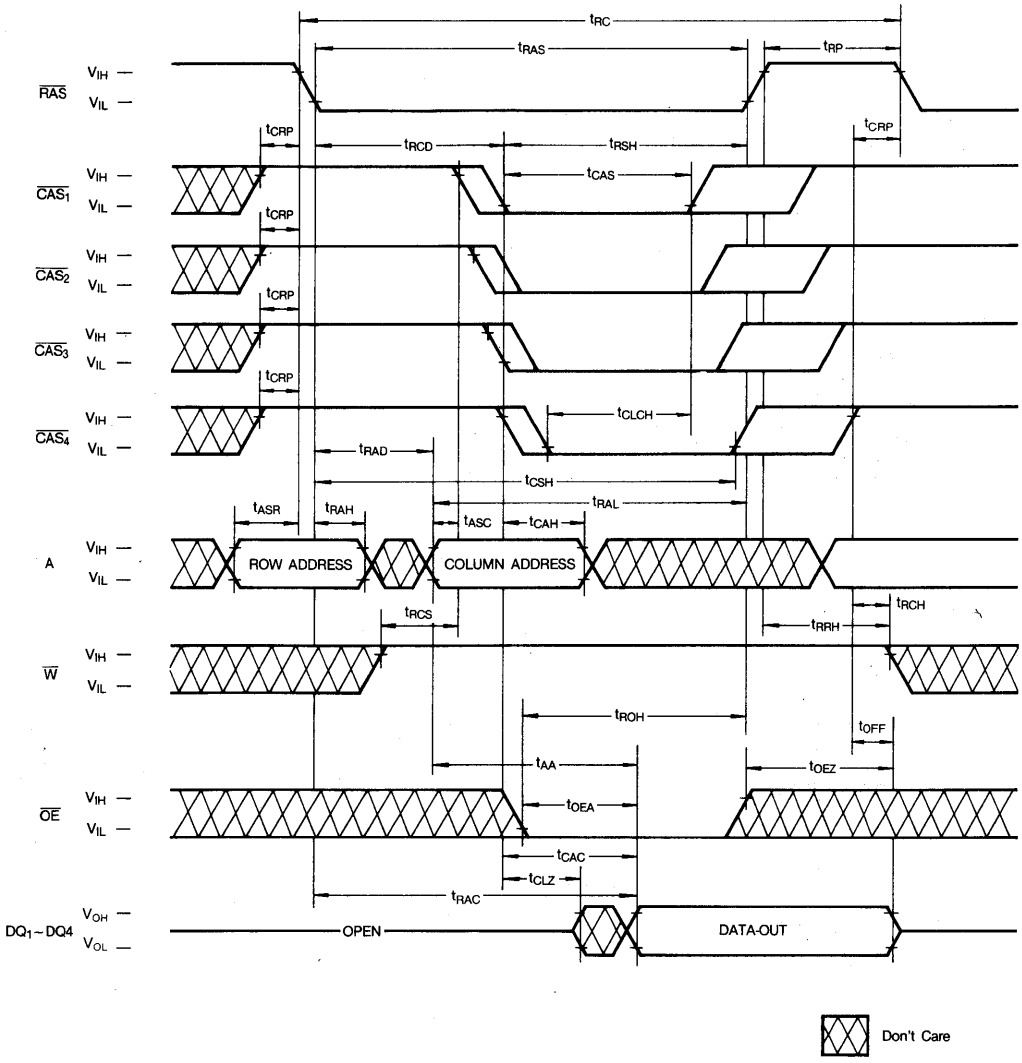
5

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 32ms before and after self refresh, in order to meet refresh specification.
16. In order to hold the address latched by the first $\overline{CASx}$ going low. The parameter t_{CLCH} must be met.
17. The first $\overline{CASx}$ edge to transition low.
18. The last $\overline{CASx}$ edge to transition high.
19. Output parameter is referenced to corresponding $\overline{CASx}$ input.
20. Last rising $\overline{CASx}$ edge to next cycle's last rising $\overline{CASx}$ edge.
21. Last rising $\overline{CASx}$ edge to first falling $\overline{CASx}$ edge.
22. First DQx controlled by the first $\overline{CASx}$ to go low.
23. Last DQx controlled by the last $\overline{CASx}$ to go high.
24. Each $\overline{CASx}$ must meet minimum pulse width.
25. Last $\overline{CASx}$ to go low.

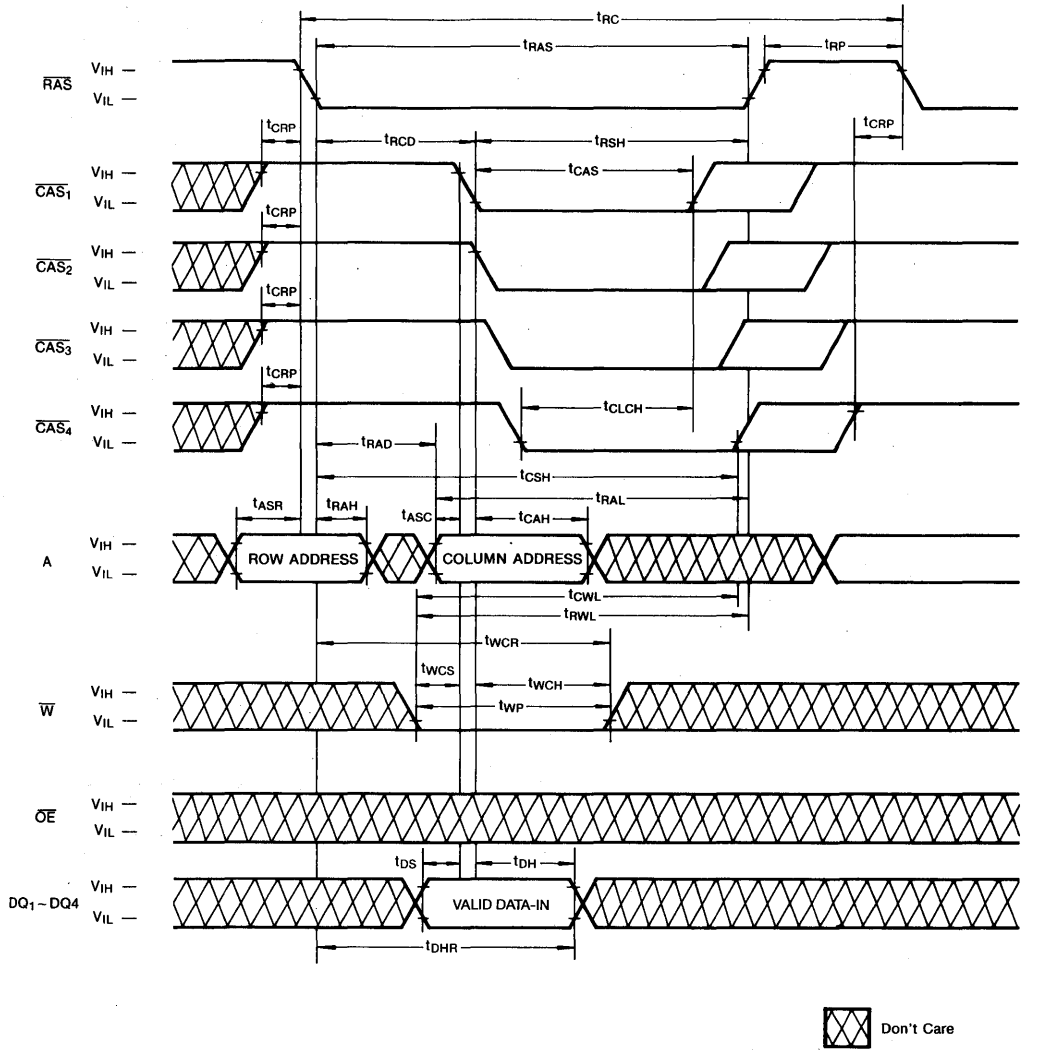
TIMING DIAGRAM

READ CYCLE



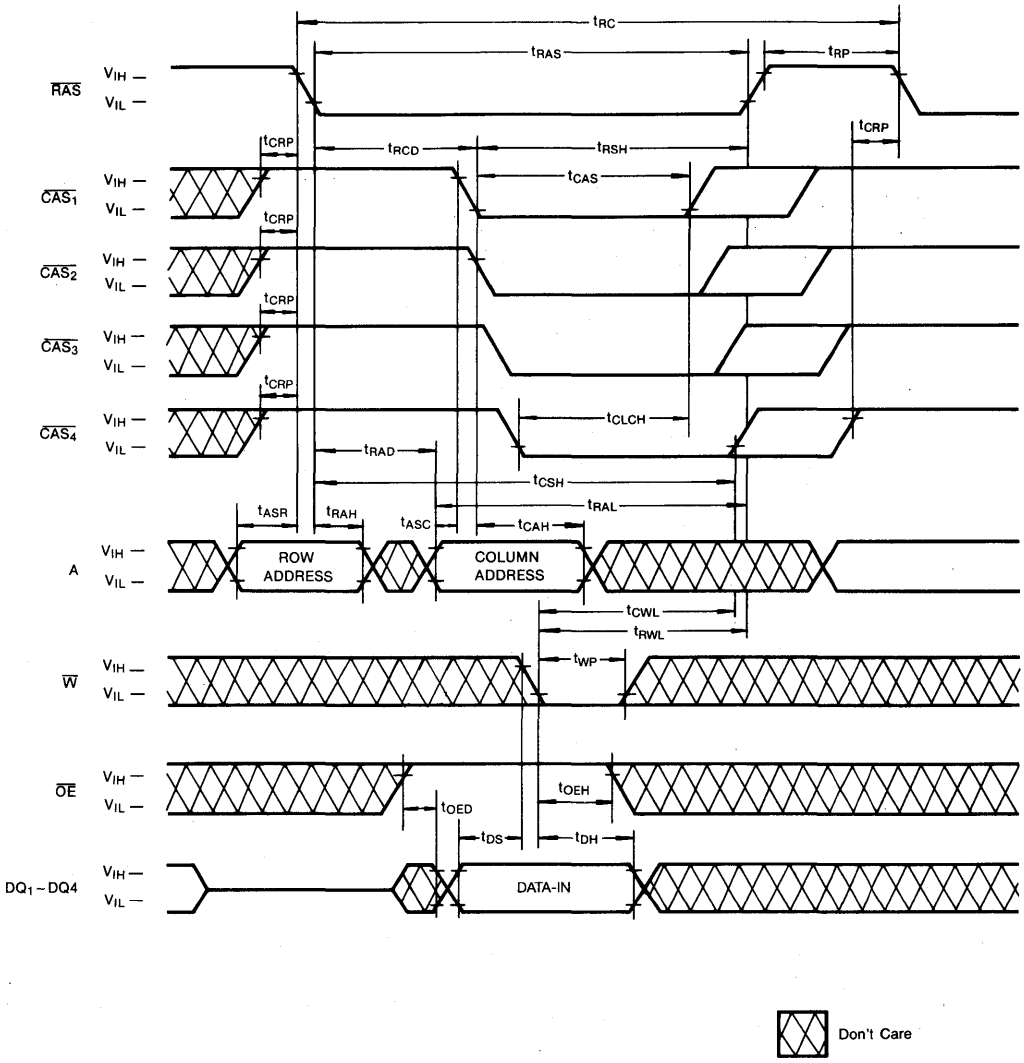
TIMING DIAGRAM (Continued)

WRITE CYCLE (EARLY WRITE)



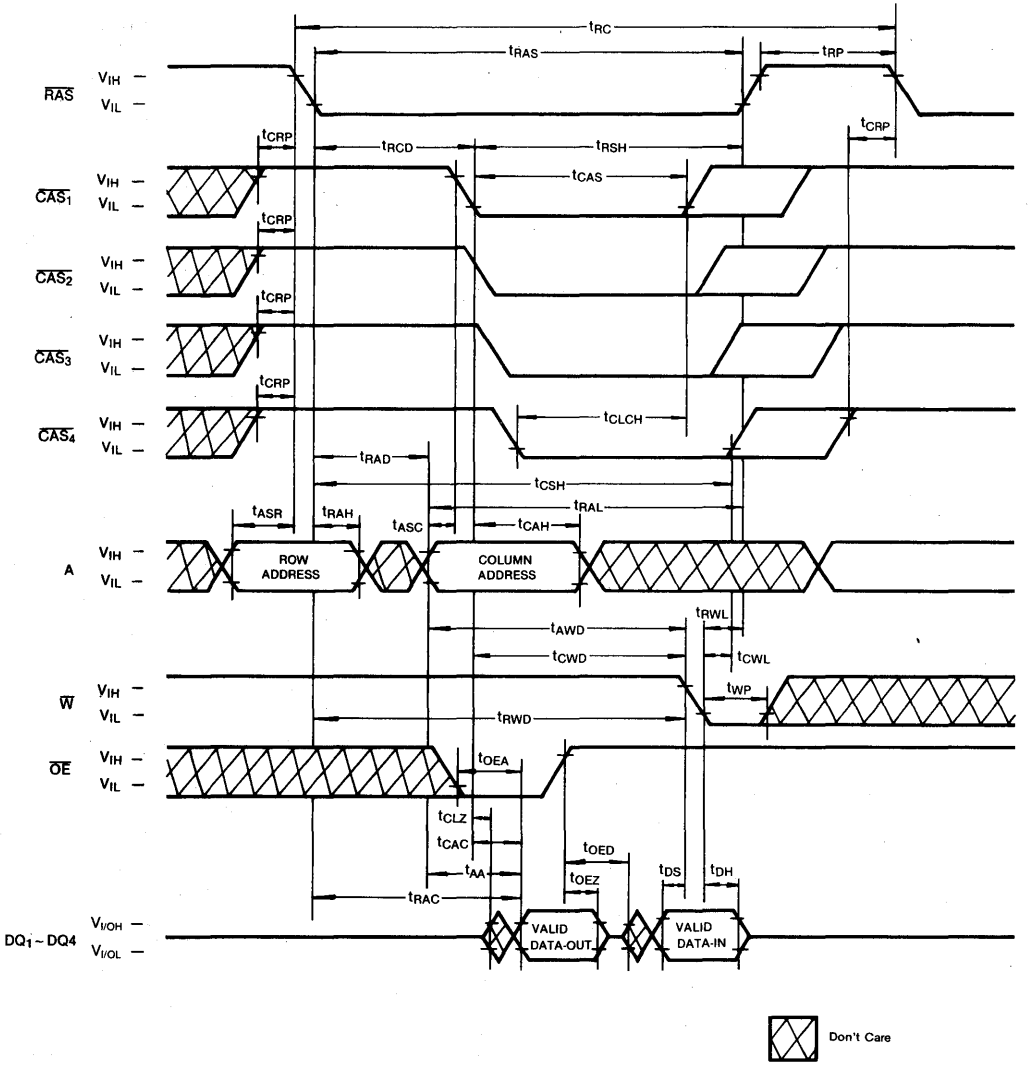
TIMING DIAGRAM (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



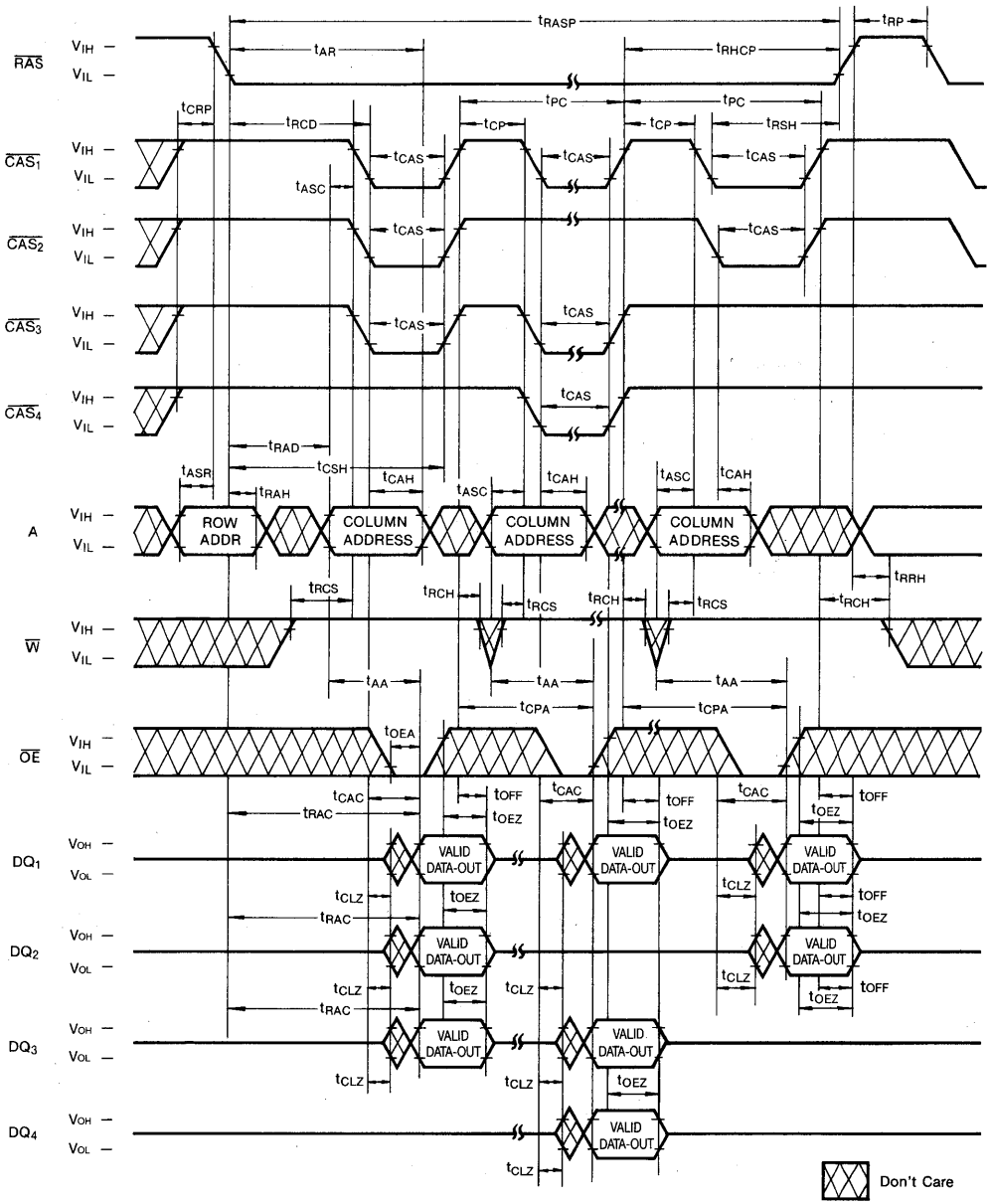
TIMING DIAGRAM (Continued)

READ-MODIFY-WRITE CYCLE



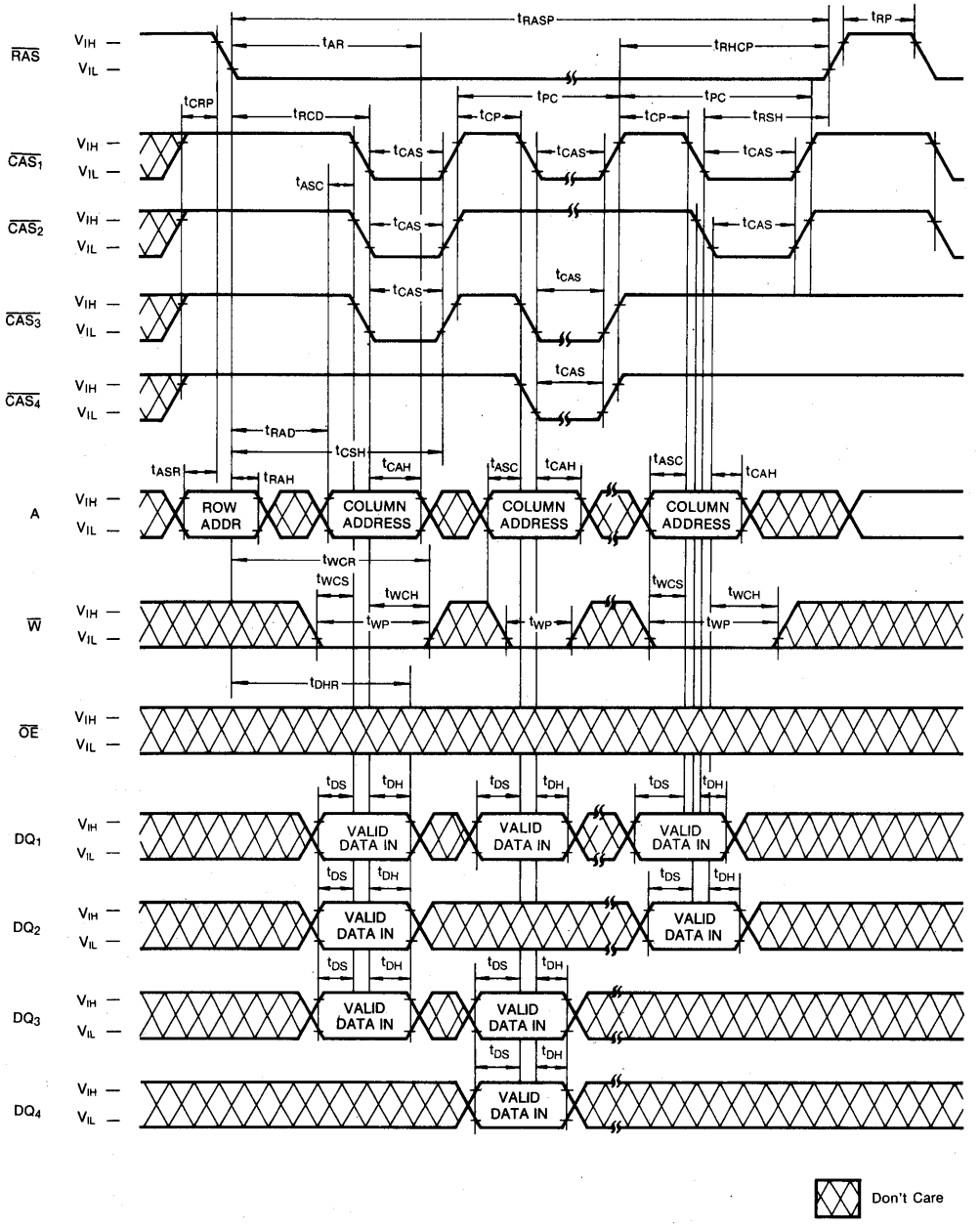
TIMING DIAGRAM (Continued)

FAST PAGE MODE READ CYCLE



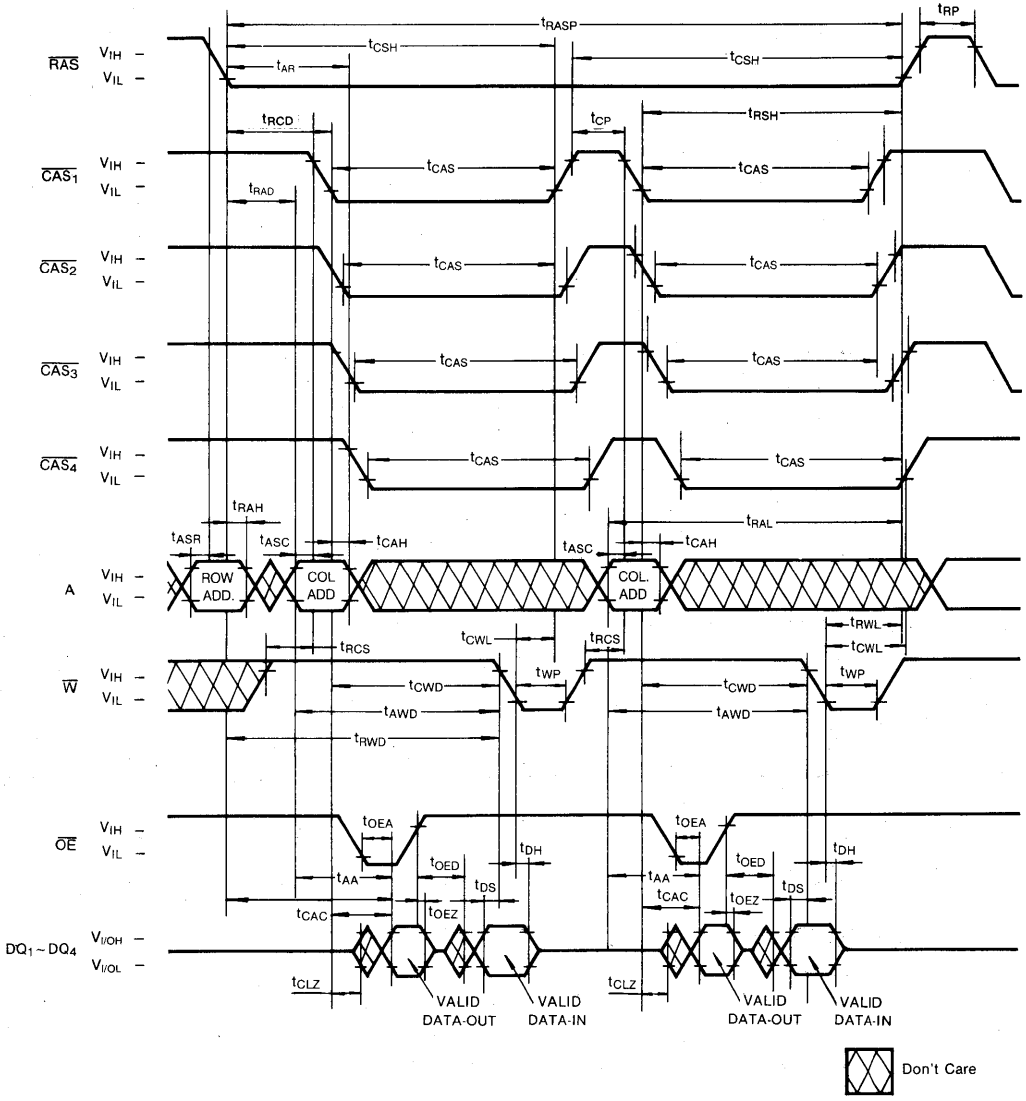
TIMING DIAGRAM (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAM (Continued)

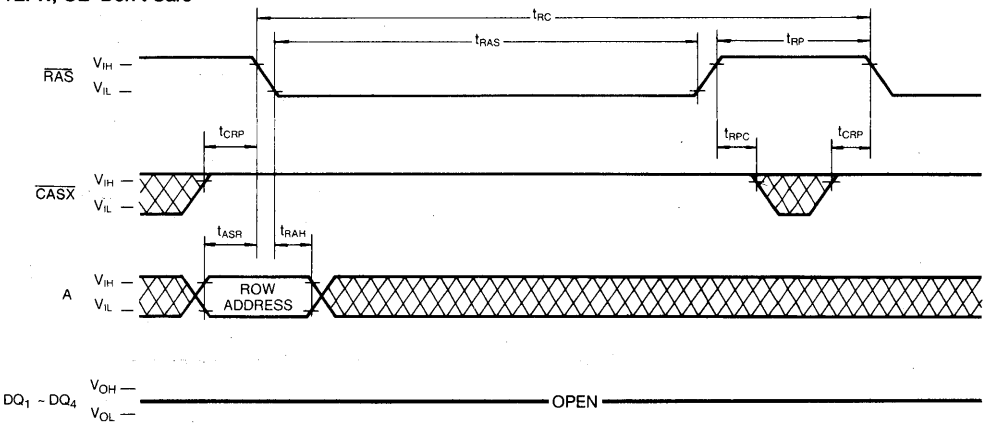
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

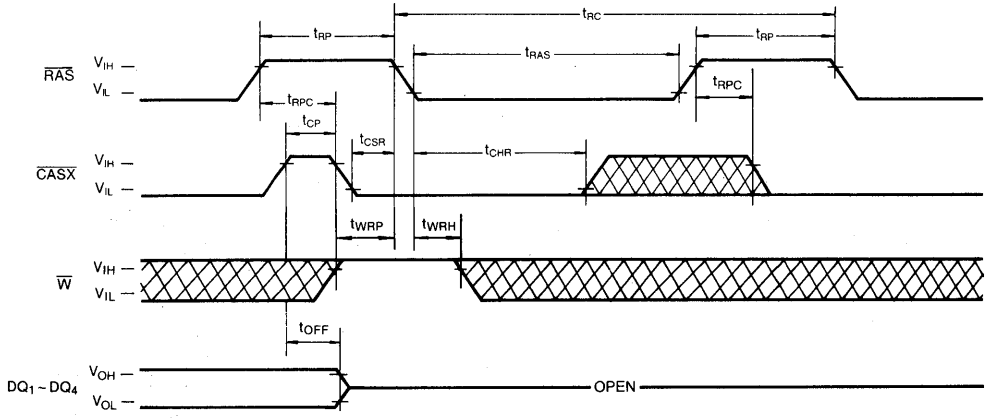
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

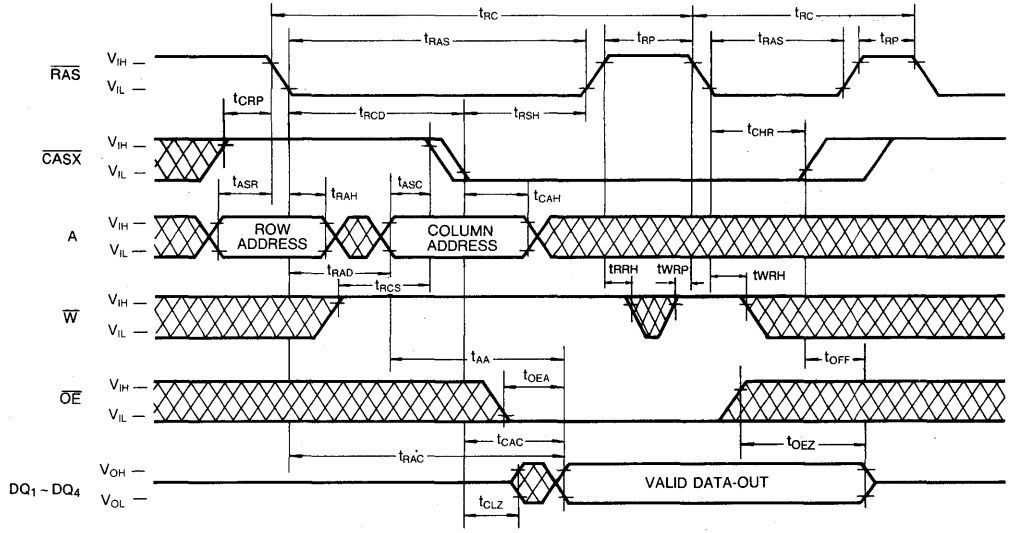
NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care



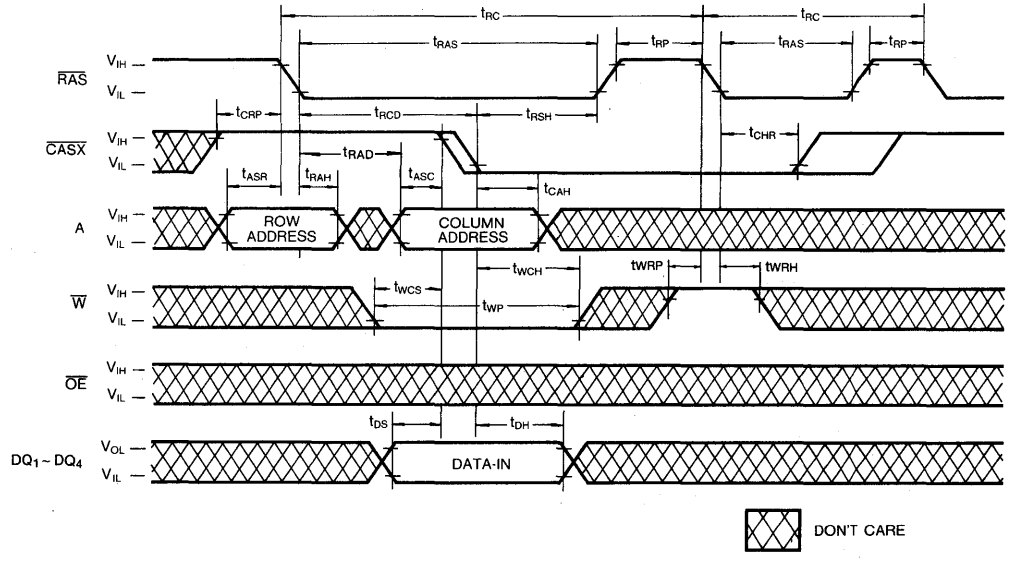
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

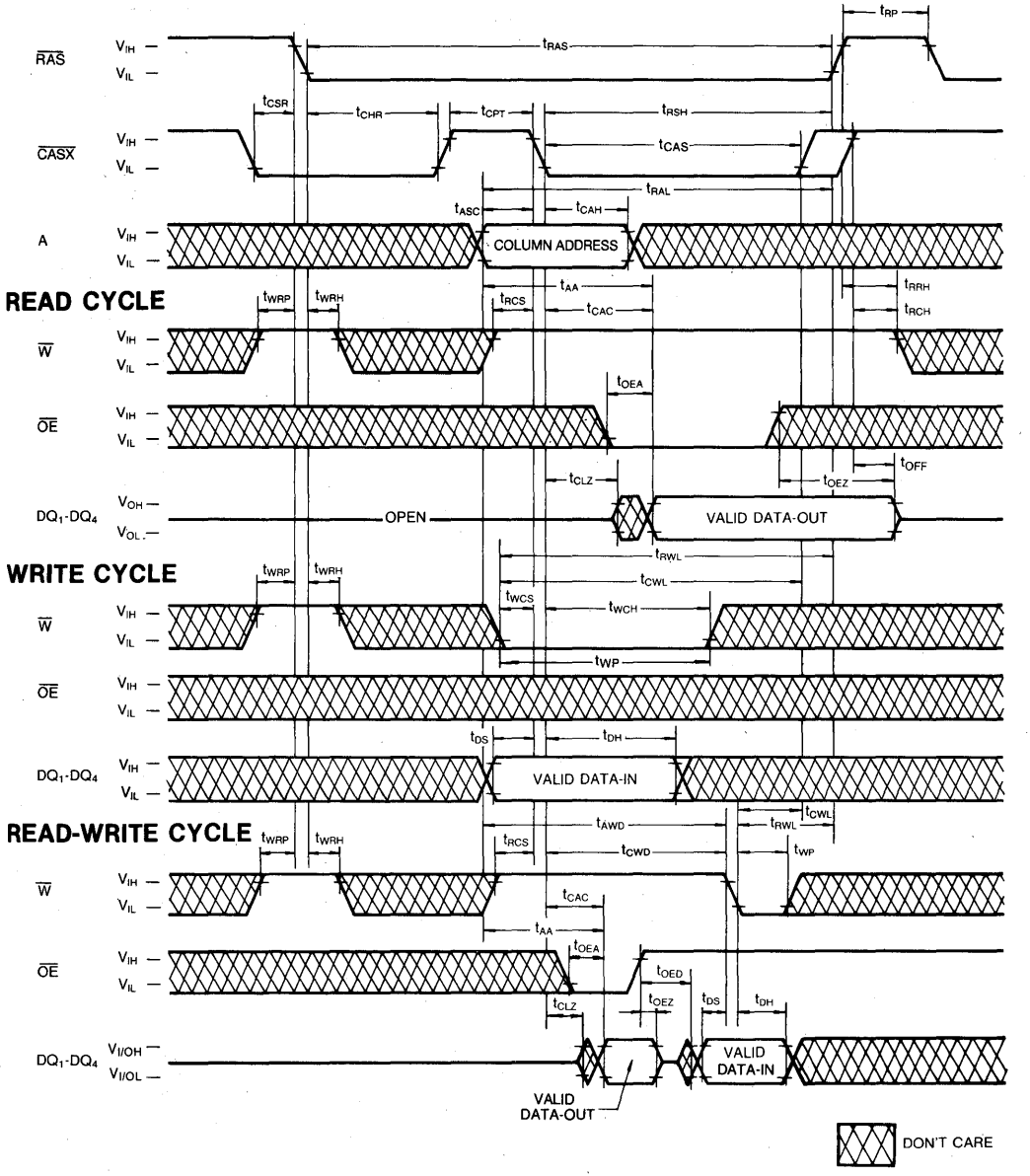


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

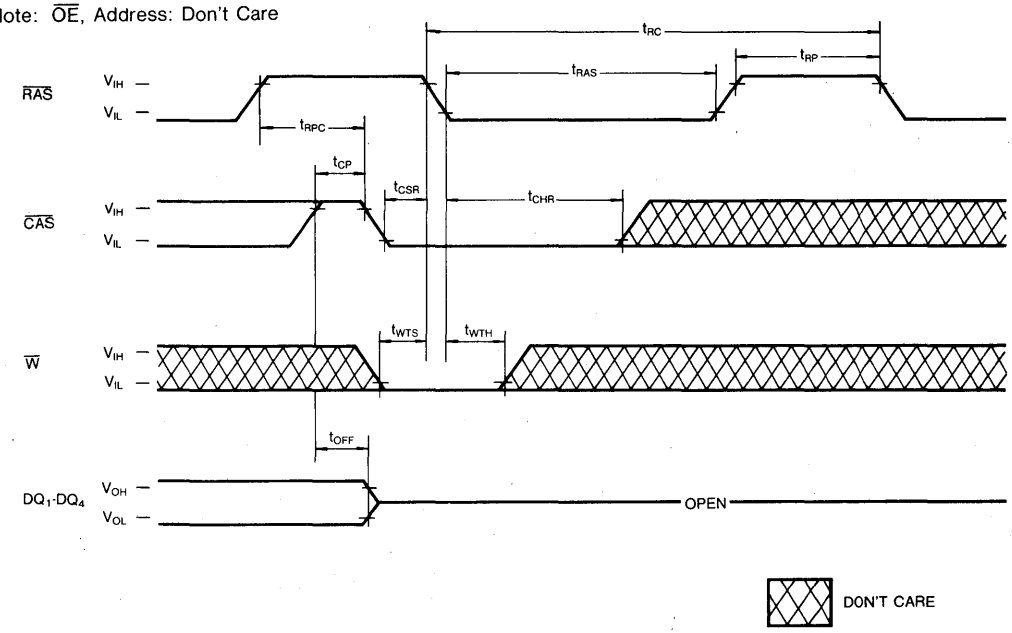


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



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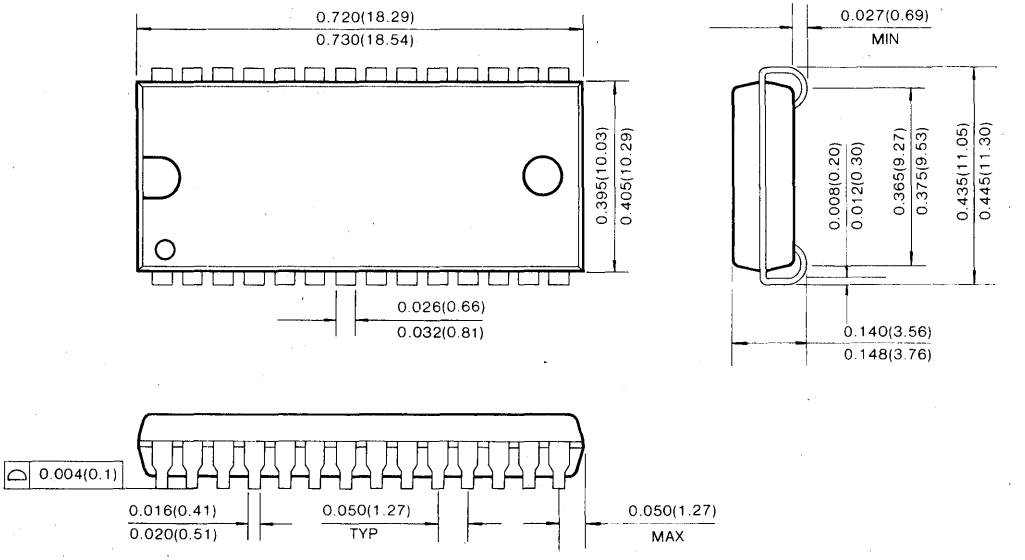
SAMSUNG ELECTRONICS

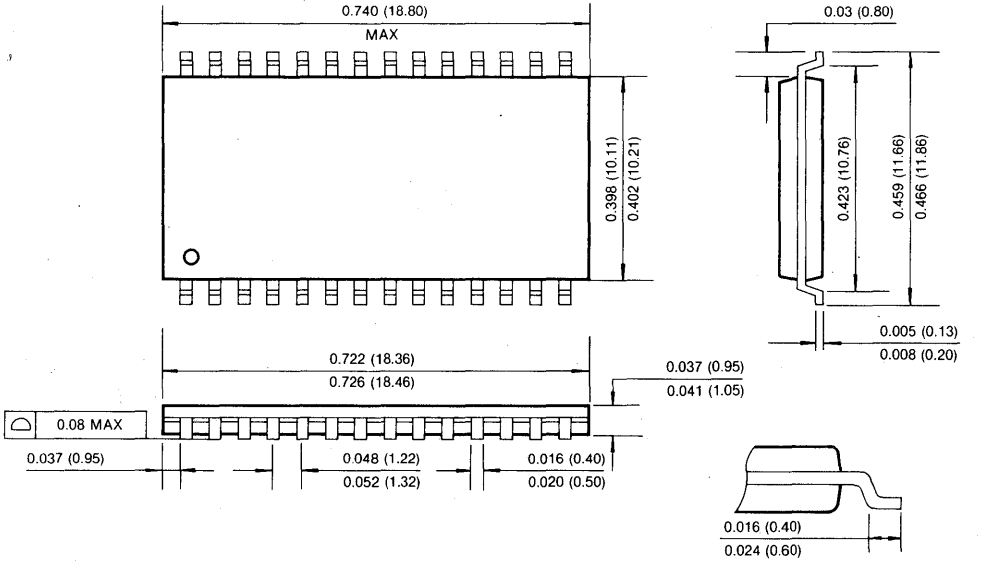
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



4M ×4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM44C4004A/AL/ALL/ASL-5	50ns	13ns	90ns	20ns
KM44C4004A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM44C4004A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM44C4004A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- **Fast Page Mode with Extended data out**
- **Self Refresh operation (LL-ver. only)**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V±10% power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

The Samsung KM44C4004A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4004A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C4004A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

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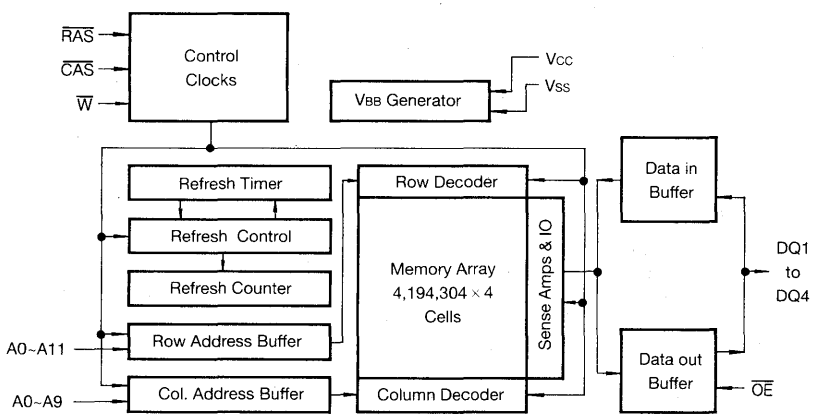
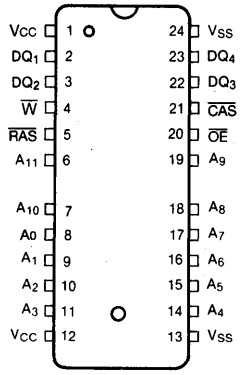
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

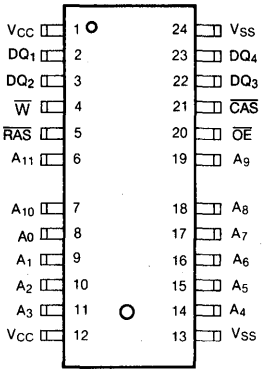
PIN CONFIGURATION (Top Views)

• KM44C4004 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



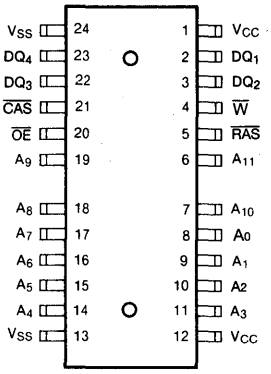
J : 400MIL
K : 300MIL

• KM44C4004 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44C4004 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1~4	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power(+5.0V)

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4004A/AL/ALL/ASL-5	I_{CC1}	-	90	mA
	KM44C4004A/AL/ALL/ASL-6			80	mA
	KM44C4004A/AL/ALL/ASL-7			70	mA
	KM44C4004A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44C4004A	I_{CC2}	-	2	mA
	KM44C4004AL			1	mA
	KM44C4004ALL			1	mA
	KM44C4004ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44C4004A/AL/ALL/ASL-5	I_{CC3}	-	90	mA
	KM44C4004A/AL/ALL/ASL-6			80	mA
	KM44C4004A/AL/ALL/ASL-7			70	mA
	KM44C4004A/AL/ALL/ASL-8			60	mA
Hyper Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44C4004A/AL/ALL/ASL-5	I_{CC4}	-	100	mA
	KM44C4004A/AL/ALL/ASL-6			90	mA
	KM44C4004A/AL/ALL/ASL-7			80	mA
	KM44C4004A/AL/ALL/ASL-8			70	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM44C4004A	I_{CC5}	-	1	mA
	KM44C4004AL			300	μA
	KM44C4004ALL			200	μA
	KM44C4004ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4004A/AL/ALL/ASL-5	I_{CC6}	-	90	mA
	KM44C4004A/AL/ALL/ASL-6			80	mA
	KM44C4004A/AL/ALL/ASL-7			70	mA
	KM44C4004A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ_1~DQ_4=Don't Care t_{RC}=31.25μs(L-Ver.) 62.5μs(SL-Ver.), t_{RAS}=t_{RAS}≦min~300ns	KM44C4004AL	I_{CC7}	-	450	μA
	KM44C4004ASL			350	μA

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DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{CC}-0.2V or 0.2V DQ_1-DQ_4=V_{CC}-0.2V, 0.2V or Open	KM44C4004ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one Hyper page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±0.5V, See notes 1,2)

Test condition: V_{ih}/V_{il}=2.4V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		2		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	3	20	3	20	ns	7,15
Transition time (rise and fall)	t_T	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		50		60		ns	16
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	15	10K	20	10K	ns	4
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	11
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	8		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		15		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64		64	ms	
Refresh period (L-ver)	t_{REF}		128		128		128		128	ms	
Refresh period (SL-ver)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CAS}$ oprecharge to $\overline{W}$ delay time	t_{CPWD}	53		60		70		75		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Hyper Page cycle time	t_{HPC}	20		24		29		34		ns	17
Hyper Page read-modify-write cycle time	t_{HPRWC}	62		71		86		96		ns	17
$\overline{CAS}$ precharge time (Hyper Page Cycle)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page Cycle)	t_{RASP}	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		13		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	13		15		20		20		ns	

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AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	7
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	12
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	12
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	7,16
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	7
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width (LL-ver)	tRASS	100		100		100		100		μs	15
$\overline{RAS}$ precharge time (LL-ver)	tRPS	90		110		130		150		ns	15
$\overline{CAS}$ hold time (LL-ver)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	13	10,000	15	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	43		20		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Hyper Page cycle time	tHPC	25		29		34		39		ns	
Hyper Page read-modify-write cycle time	tHPRWC	67		76		91		101		ns	

TEST MODE CYCLE (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ pulse width (Hyper Page Cycle)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

TEST MODE DESCRIPTION

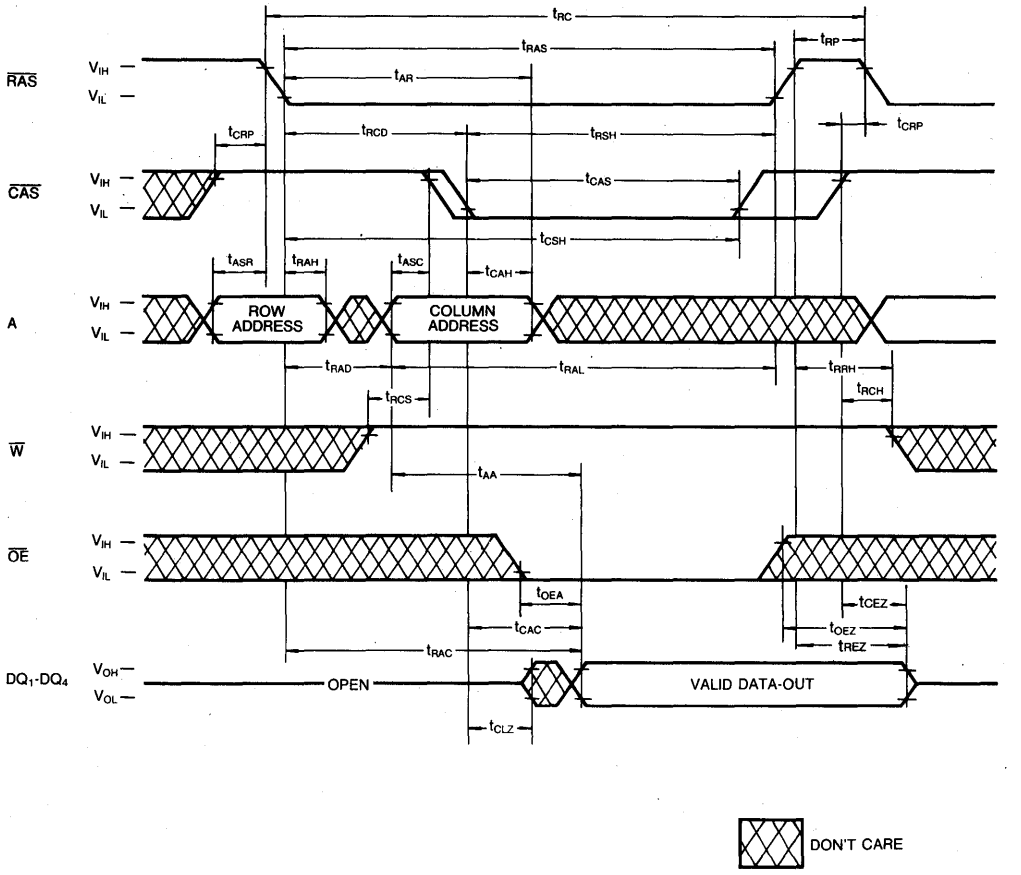
The KM44C4004A/AL/ALL/ASL is the CMOS DRAM organizied 4,194,304 words by 4 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s)the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode". the 4Mx4 DRAM can be tested as if it were a 1Mx4 DRAM. $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", and "$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" peforms the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time(1/4 in cases of N test pattern)

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) are assumed to be 5ns for all inputs, without tHPC and tHPRWC.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD ≥ tRCD (max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS ≥ tWCS(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD ≥ tCWD(min), tRWD ≥ tRWD(min) and tAWD ≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. tREZ(max),tCEZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going
17. tASC ≧ tCP (min), Assumn tT=2.0ns

TIMING DIAGRAMS

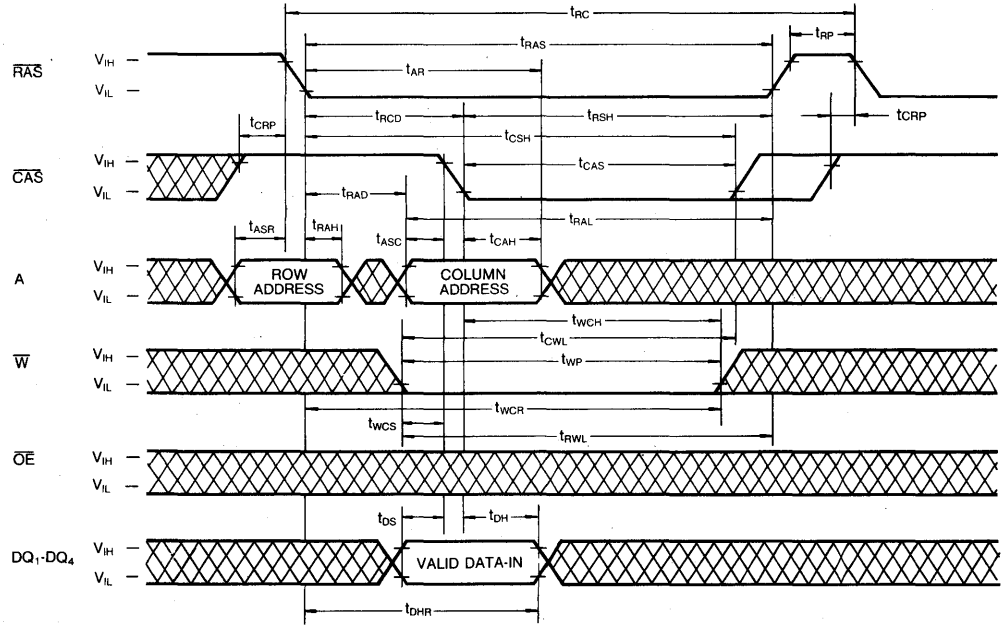
READ CYCLE



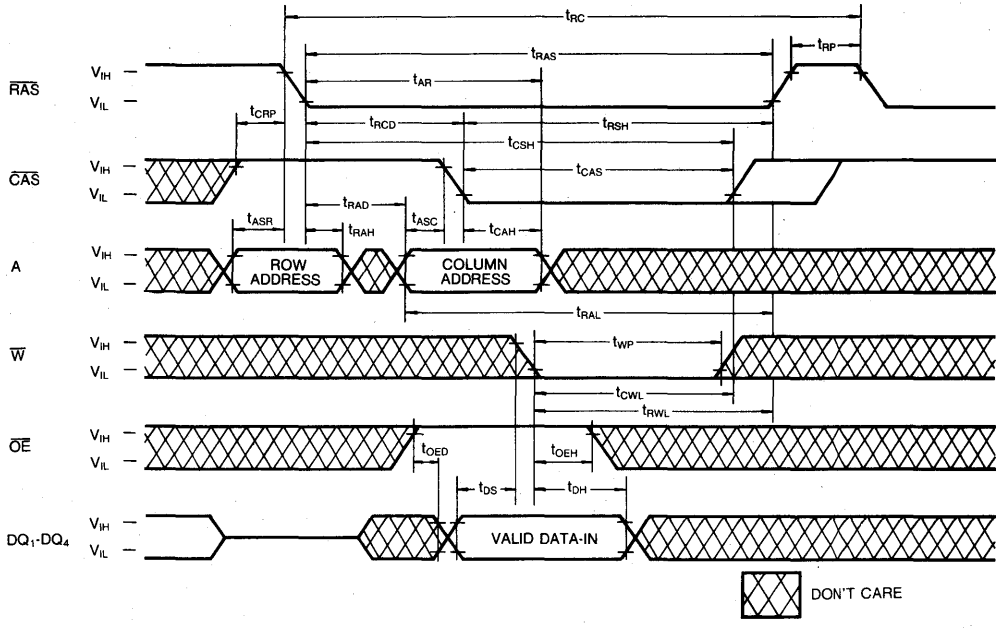
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



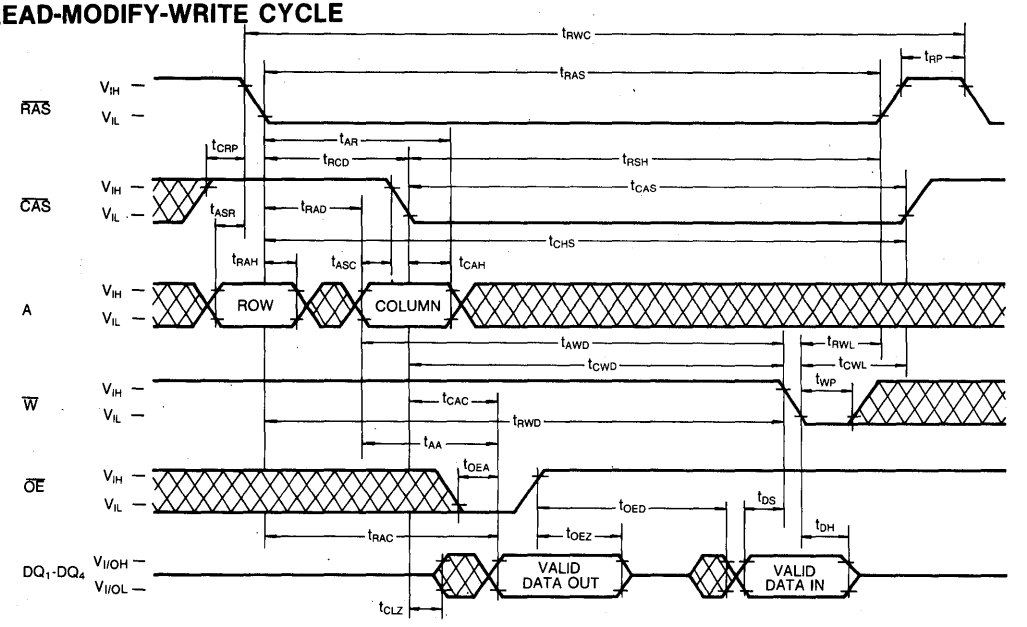
WRITE CYCLE (OE CONTROLLED WRITE)



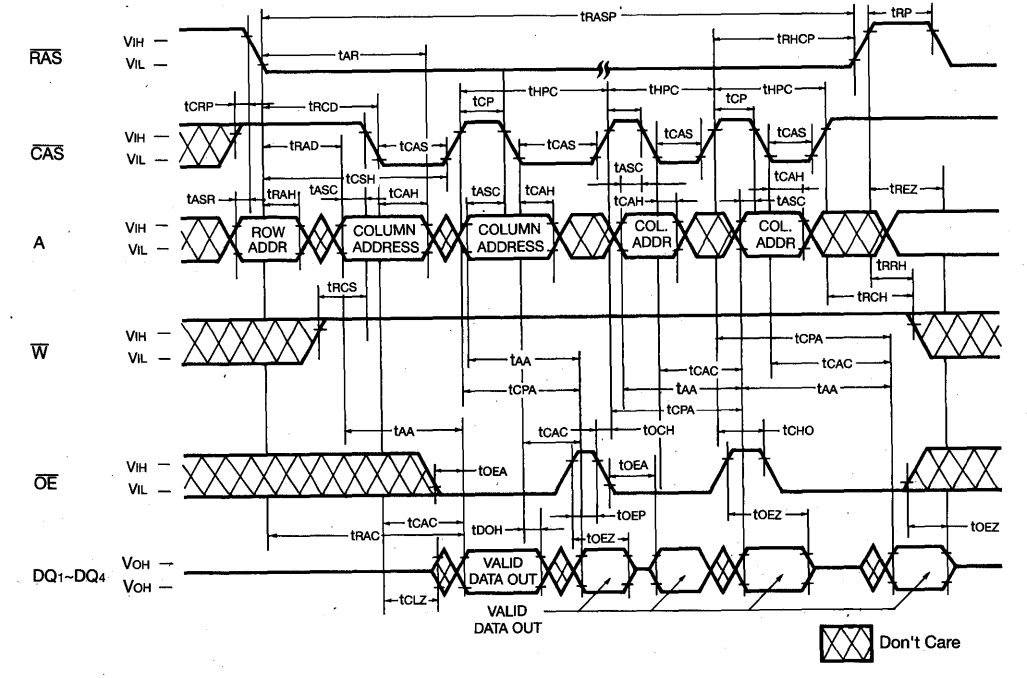
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



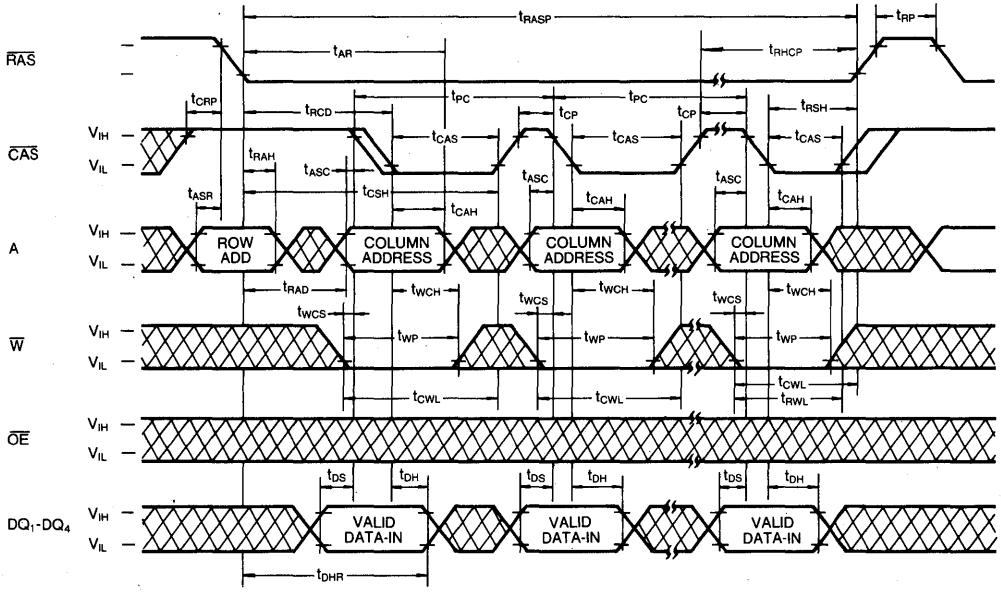
HYPER PAGE READ CYCLE



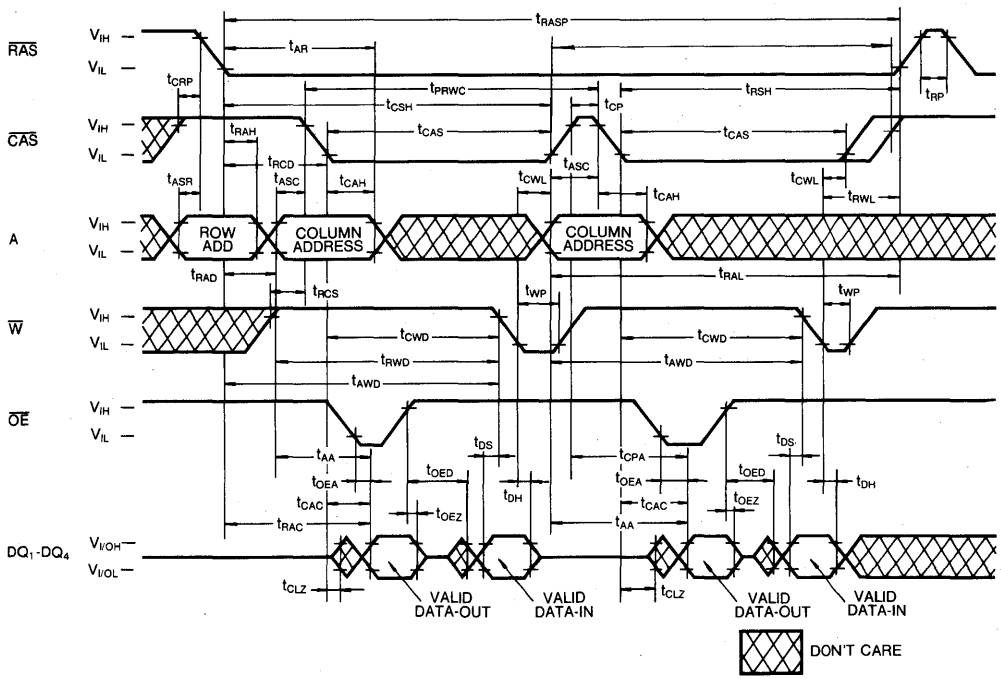
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

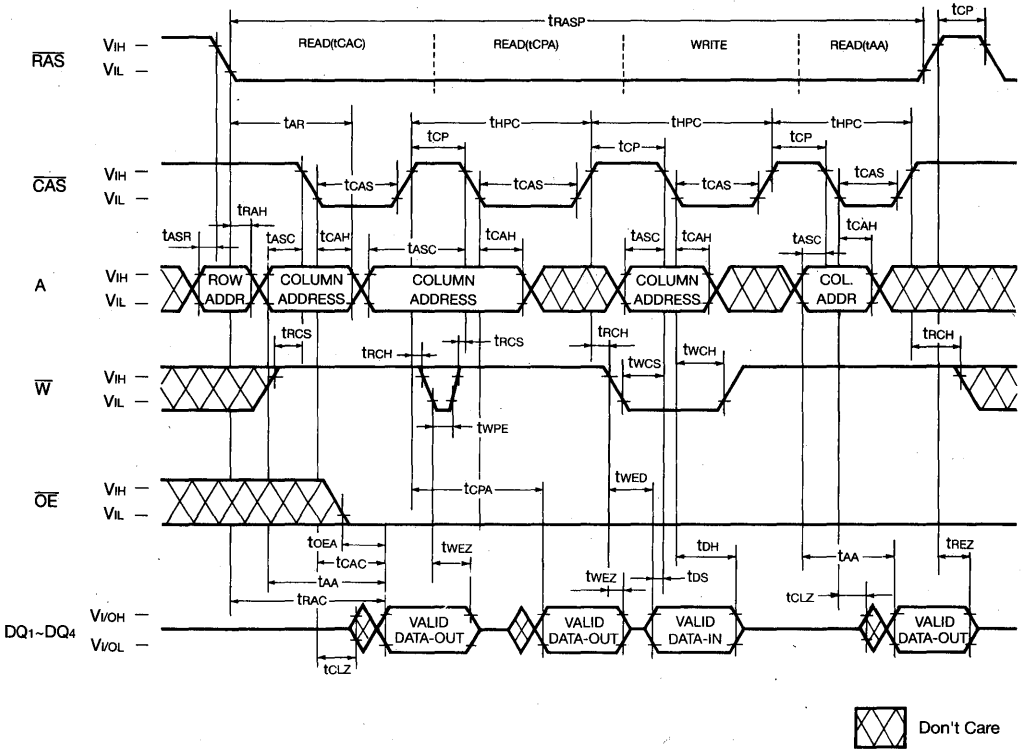
HYPER PAGE WRITE CYCLE (EARLY WRITE)



HYPER PAGE READ-MODIFY-WRITE CYCLE

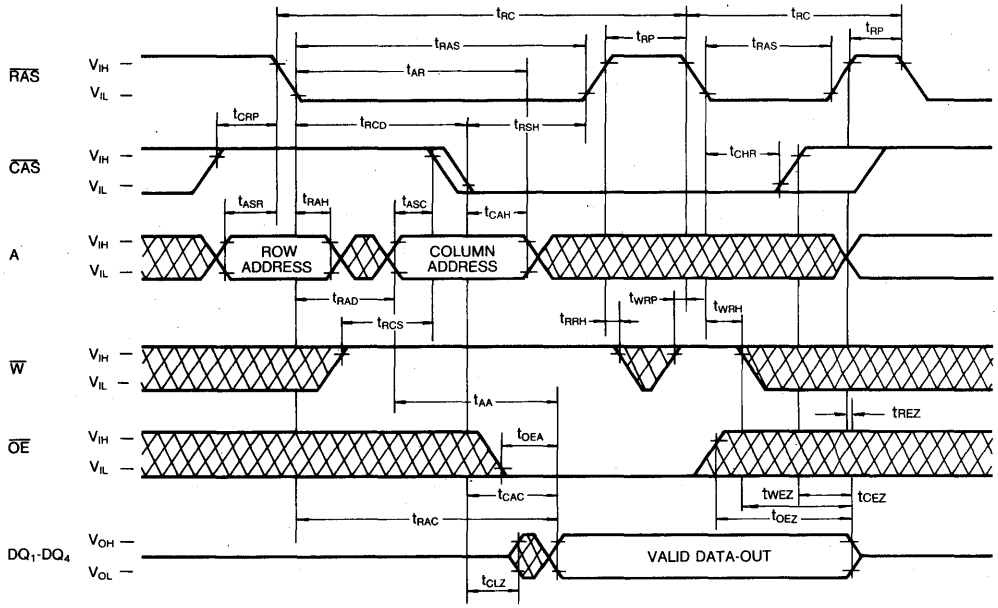


HYPER PAGE READ AND WRITE MIXED CYCLE

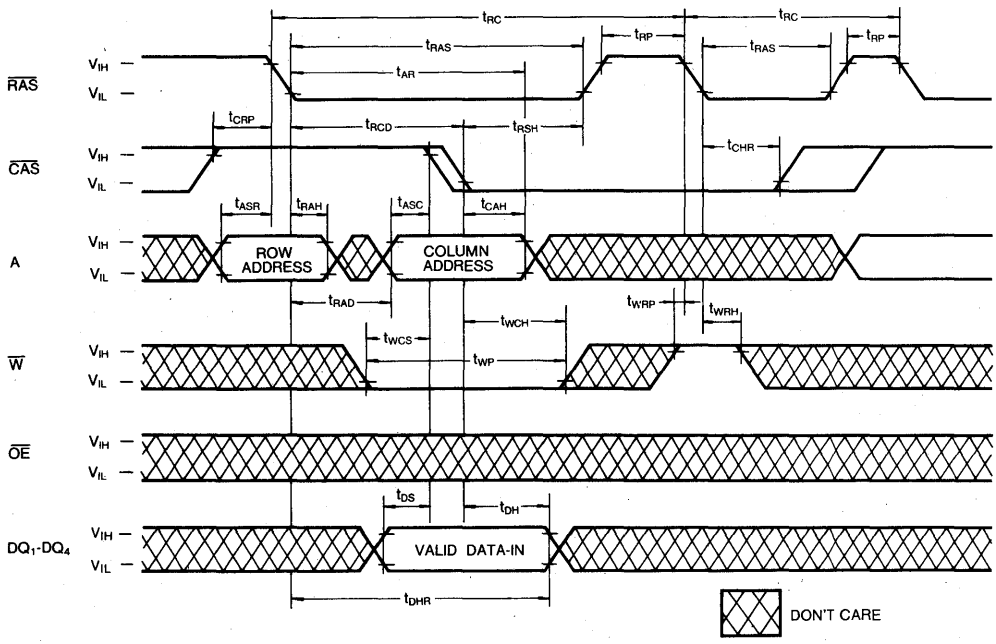


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



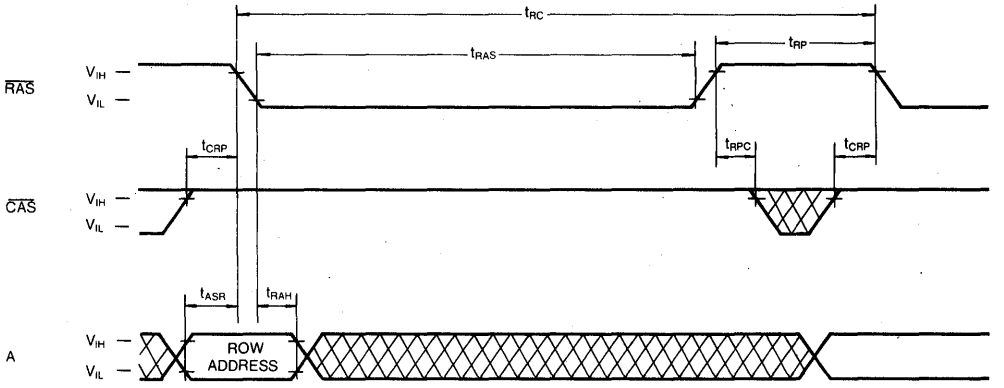
HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

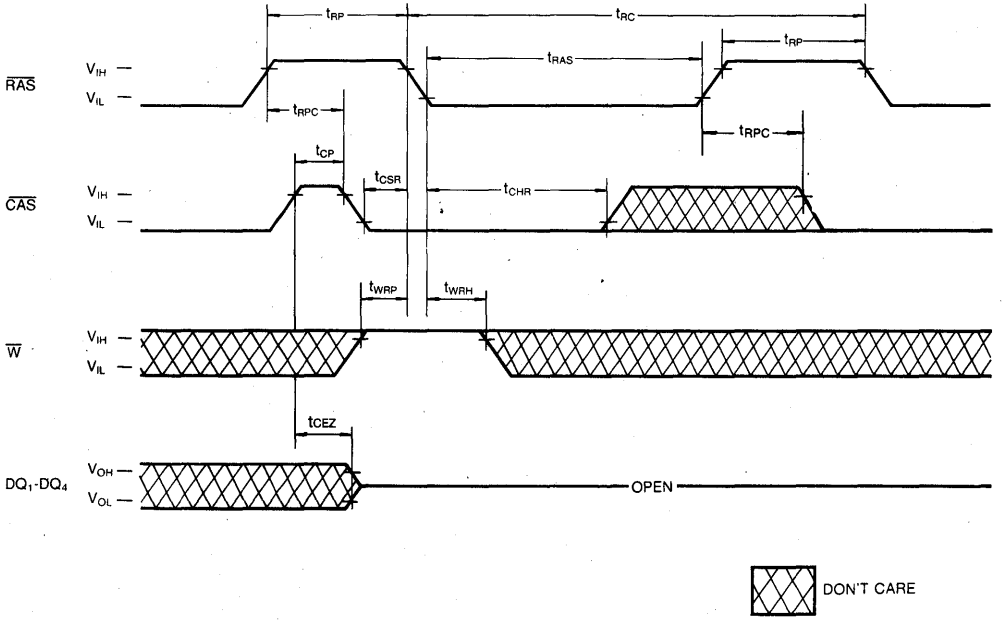
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



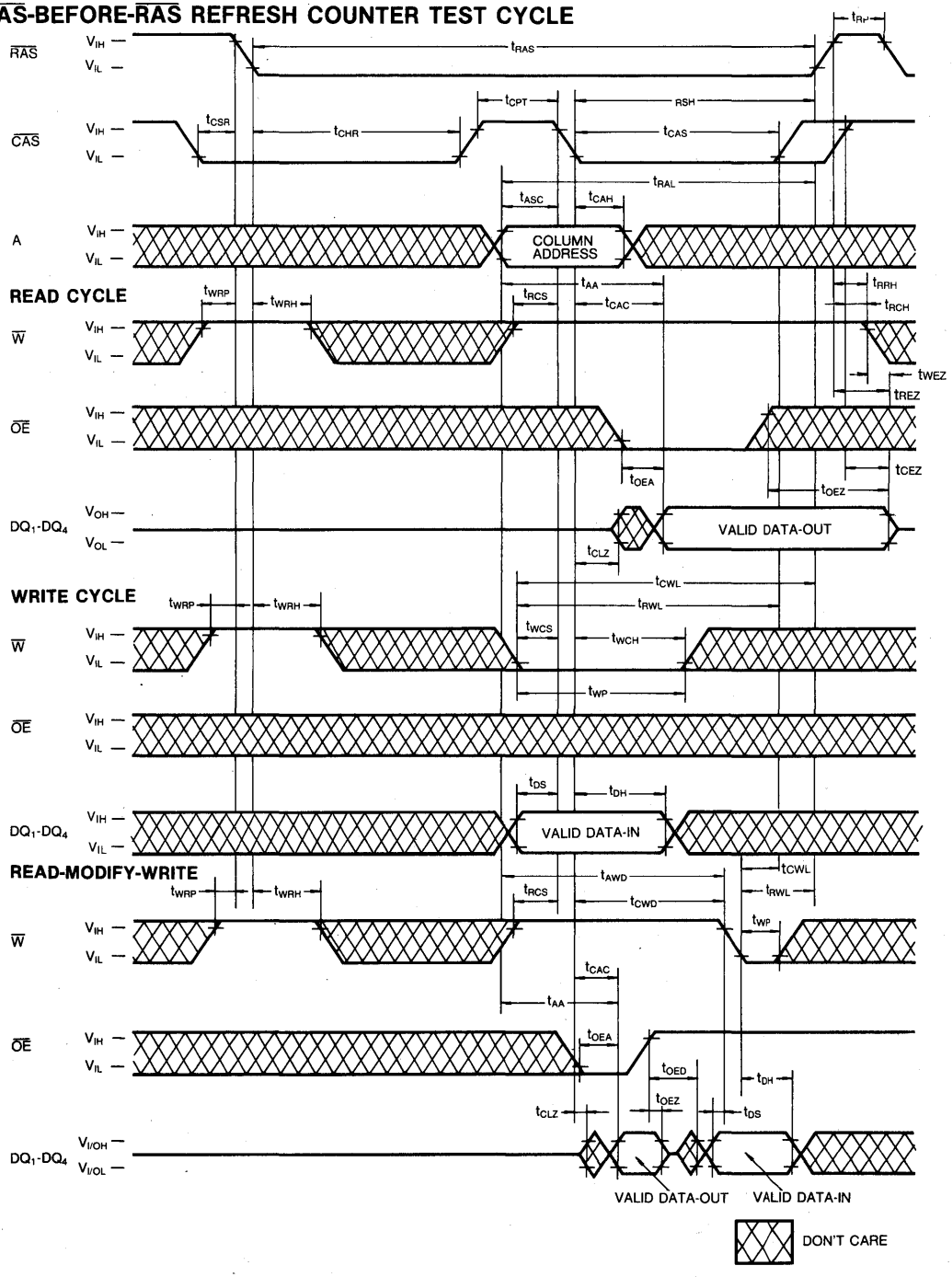
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{OE}$, Address=Don't Care



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



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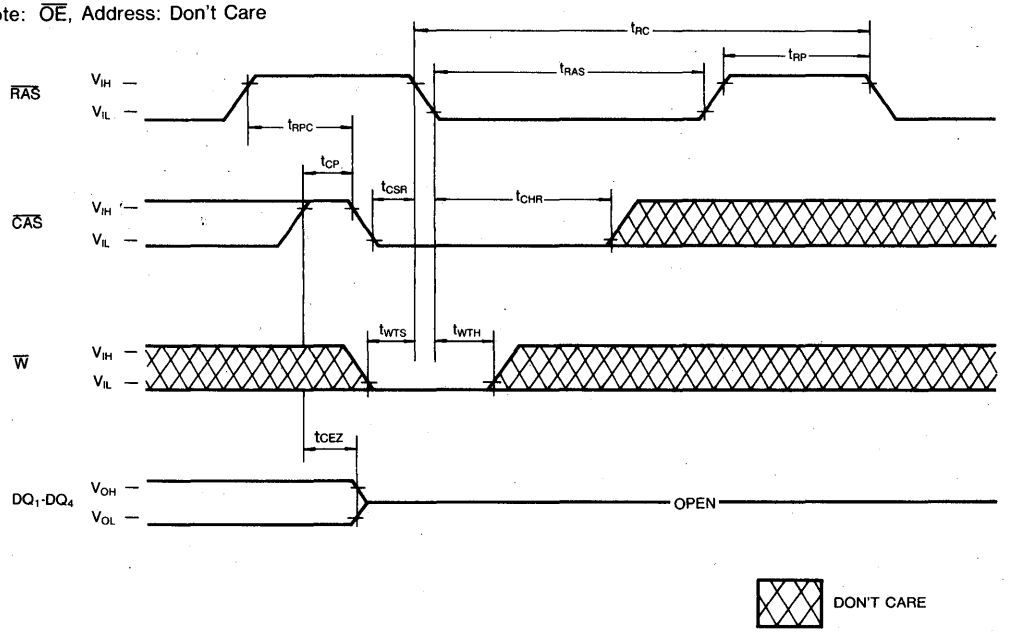
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

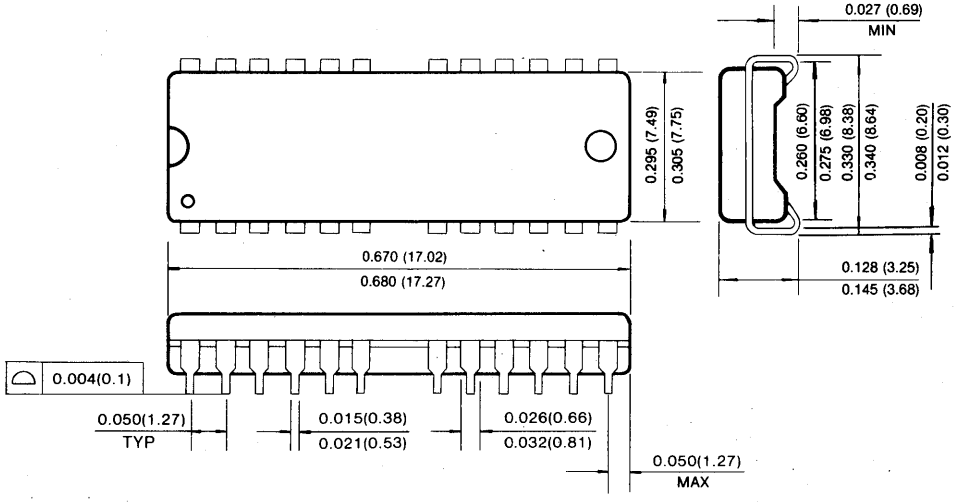
Note: $\overline{OE}$, Address: Don't Care



PACKAGE DIMENSIONS

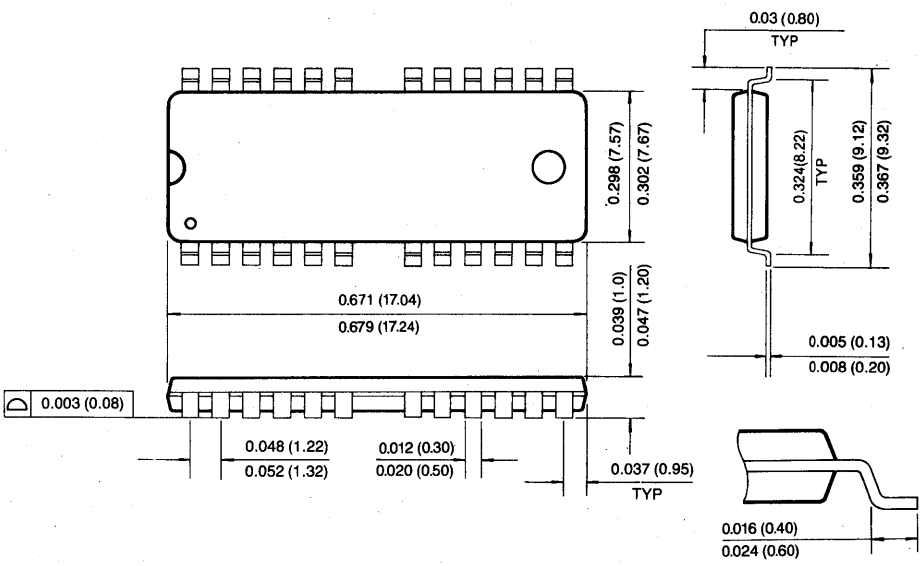
24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



5

24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

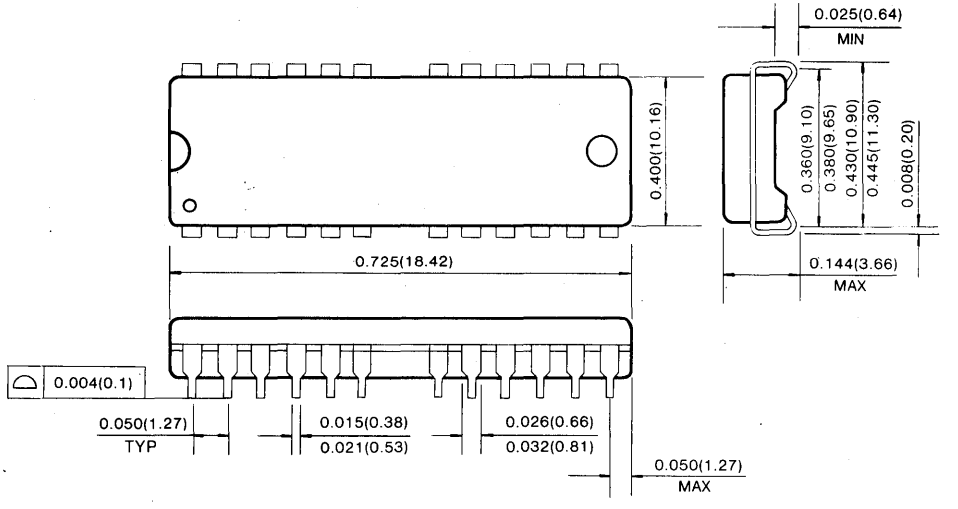


SAMSUNG ELECTRONICS

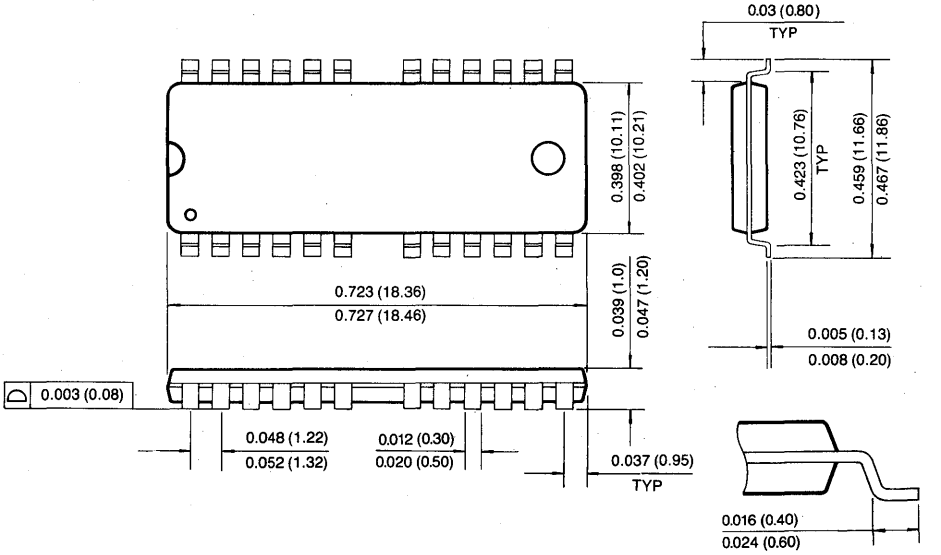
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M ×4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
KM44C4104A/AL/ALL/ASL-5	50ns	13ns	90ns	20ns
KM44C4104A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM44C4104A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM44C4104A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- **Fast Page Mode with Extended data out**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V±10% power supply**
- **2048 cycles/32ms refresh (Normal)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

The Samsung KM44C4104A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4104A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C4104A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

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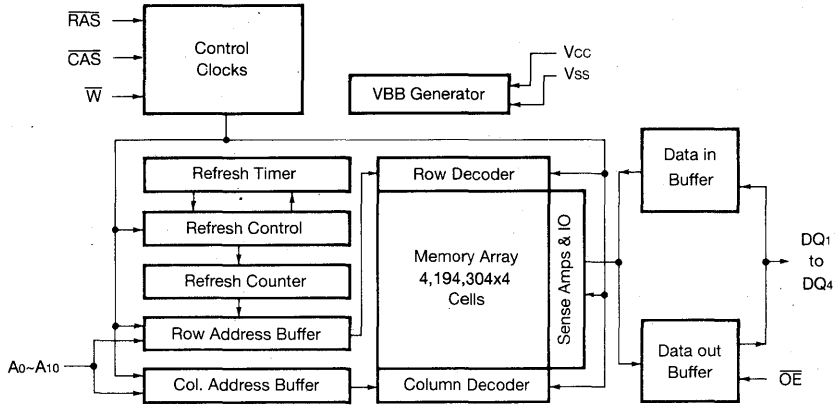
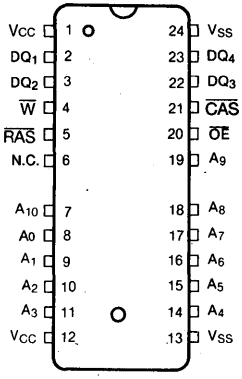
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

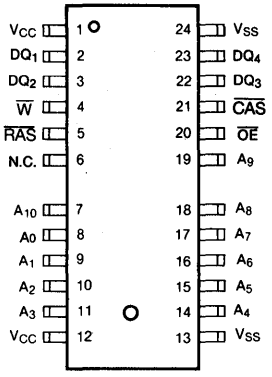
PIN CONFIGURATION (Top Views)

• KM44C4104 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



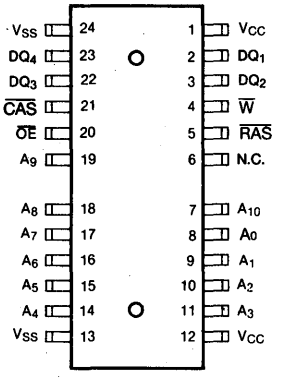
J : 400MIL
K : 300MIL

• KM44C4104 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44C4104 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ_{1-4}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power(+5.0V)
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4104A/AL/ALL/ASL-5	I_{CC1}	-	110	mA
	KM44C4104A/AL/ALL/ASL-6			100	mA
	KM44C4104A/AL/ALL/ASL-7			90	mA
	KM44C4104A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44C4104A	I_{CC2}	-	2	mA
	KM44C4104AL			1	mA
	KM44C4104ALL			1	mA
	KM44C4104ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44C4104A/AL/ALL/ASL-5	I_{CC3}	-	110	mA
	KM44C4104A/AL/ALL/ASL-6			100	mA
	KM44C4104A/AL/ALL/ASL-7			90	mA
	KM44C4104A/AL/ALL/ASL-8			80	mA
Hyper Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44C4104A/AL/ALL/ASL-5	I_{CC4}	-	110	mA
	KM44C4104A/AL/ALL/ASL-6			100	mA
	KM44C4104A/AL/ALL/ASL-7			90	mA
	KM44C4104A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM44C4104A	I_{CC5}	-	1	mA
	KM44C4104AL			300	μA
	KM44C4104ALL			200	μA
	KM44C4104ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4104A/AL/ALL/ASL-5	I_{CC6}	-	110	mA
	KM44C4104A/AL/ALL/ASL-6			100	mA
	KM44C4104A/AL/ALL/ASL-7			90	mA
	KM44C4104A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ_1~DQ_4=Don't Care t_{RC}=62.5μs(L-Ver.) 125μs(SL-Ver.), t_{RAS}=t_{RAS}≦min~300ns	KM44C4104AL	I_{CC7}	-	400	μA
	KM44C4104ASL			300	μA

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SAMSUNG ELECTRONICS

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{10}=V_{CC}-0.2V or 0.2V DQ_1-DQ_4=V_{CC}-0.2V, 0.2V or Open	KM44C4104ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one Hyper page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{10})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±0.5V, See notes 1,2)

Test condition: V_{ih}/V_{il}=2.4V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		2		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	3	20	3	20	ns	7,15
Transition time (rise and fall)	t_T	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		50		60		ns	16
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	15	10K	20	10K	ns	4
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	11
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		32		32		32		32	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Refresh period (SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{CAS}$ oprecharge to $\overline{W}$ delay time	tCPWD	53		60		70		75		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		24		29		34		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	62		71		86		96		ns	17
$\overline{CAS}$ precharge time (Hyper Page Cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page Cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	

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AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	7
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	12
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	12
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	7,15
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	7
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width (LL-ver)	tRASS	100		100		100		100		μs	16
$\overline{RAS}$ precharge time (LL-ver)	tRPS	90		110		130		150		ns	16
$\overline{CAS}$ hold time (LL-ver)	tCHS	-50		-50		-50		-50		ns	16

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	13	10,000	15	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	43		20		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Hyper Page cycle time	tHPC	25		29		34		39		ns	
Hyper Page read-modify-write cycle time	tHPRWC	67		76		91		101		ns	

TEST MODE CYCLE (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ pulse width (Hyper Page Cycle)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

TEST MODE DESCRIPTION

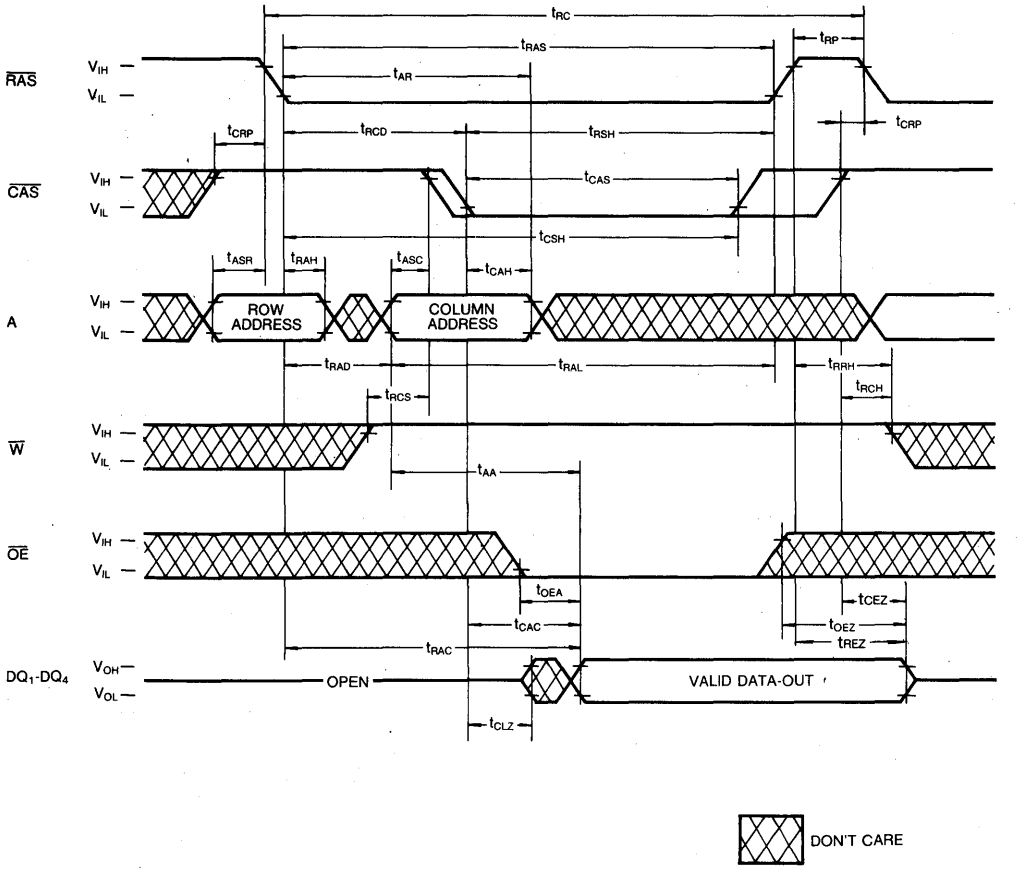
The KM44C4104A/AL/ALL/ASL is the CMOS DRAM organizied 4,194,304 words by 4 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s)the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode". the 4Mx4 DRAM can be tested as if it were a 1Mx4 DRAM. $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", and "$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" peforms the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time(1/4 in cases of N test pattern)

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) are assumed to be 5ns for all inputs, without tHPC and tHPRWC.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD ≥ tRCD (max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS ≥ tWCS(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD ≥ tCWD(min), tRWD ≥ tRWD(min) and tAWD ≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. tREZ(max), tCEZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before RAS high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going
17. tASC ≧ tCP (min), Assumn tT=2.0ns

TIMING DIAGRAMS

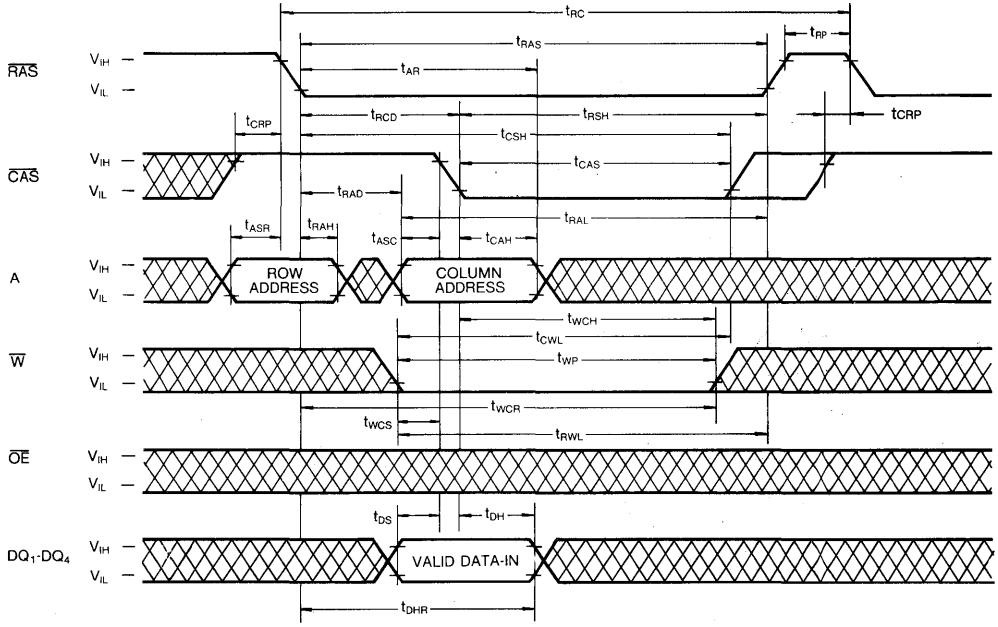
READ CYCLE



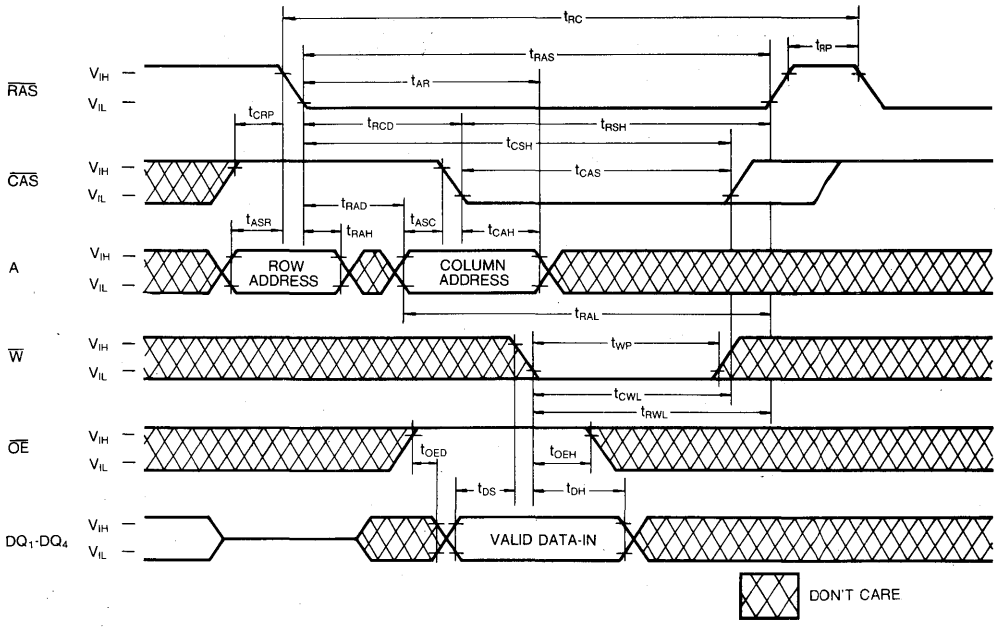
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



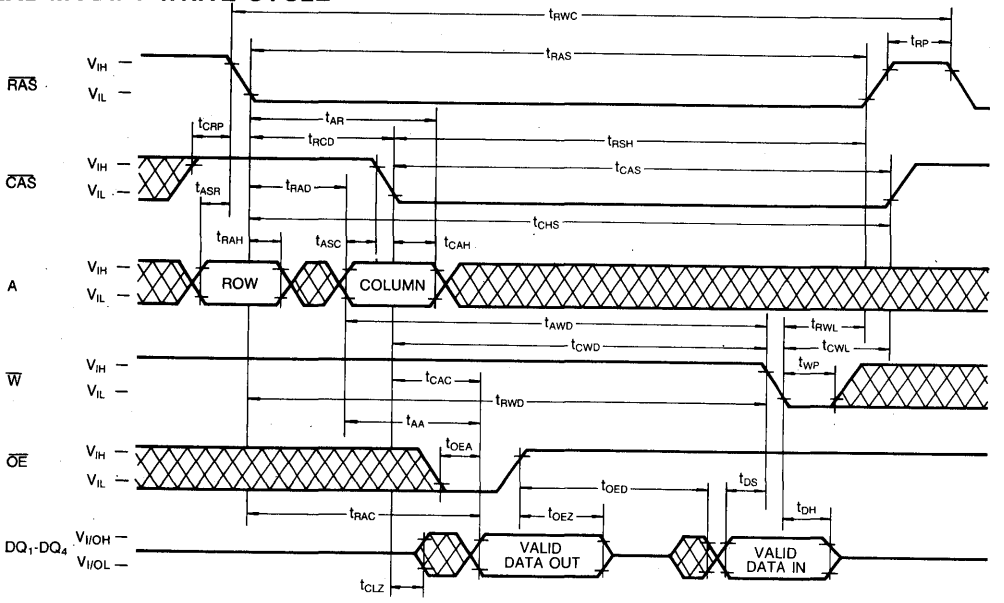
WRITE CYCLE (OE CONTROLLED WRITE)



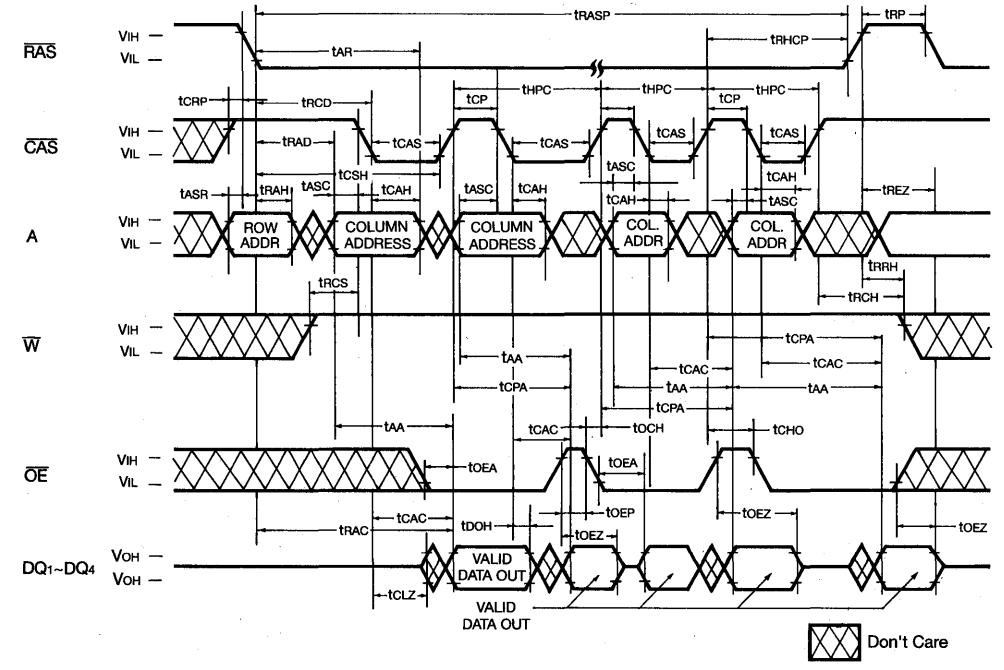
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE

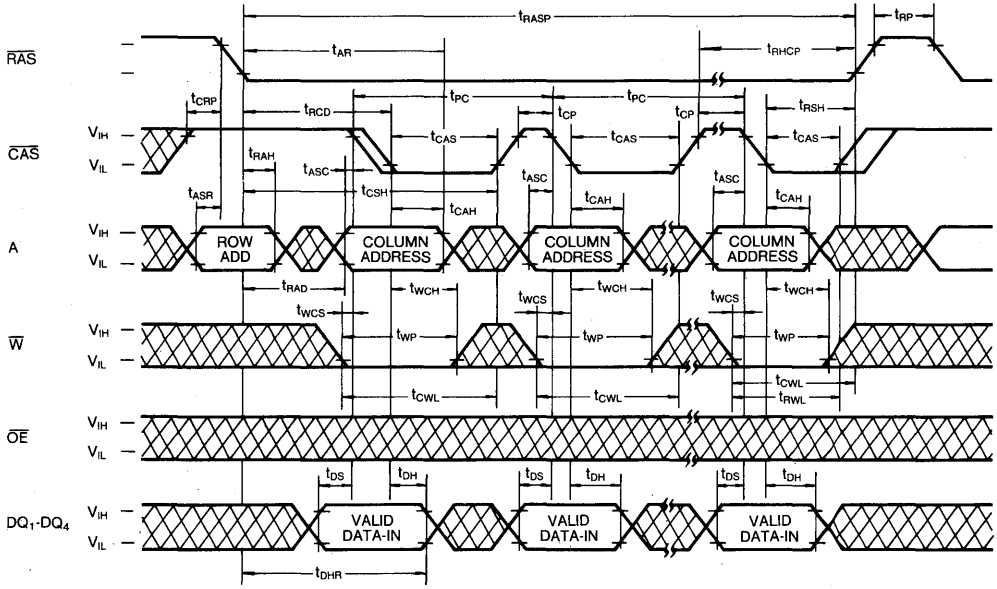


HYPER PAGE READ CYCLE

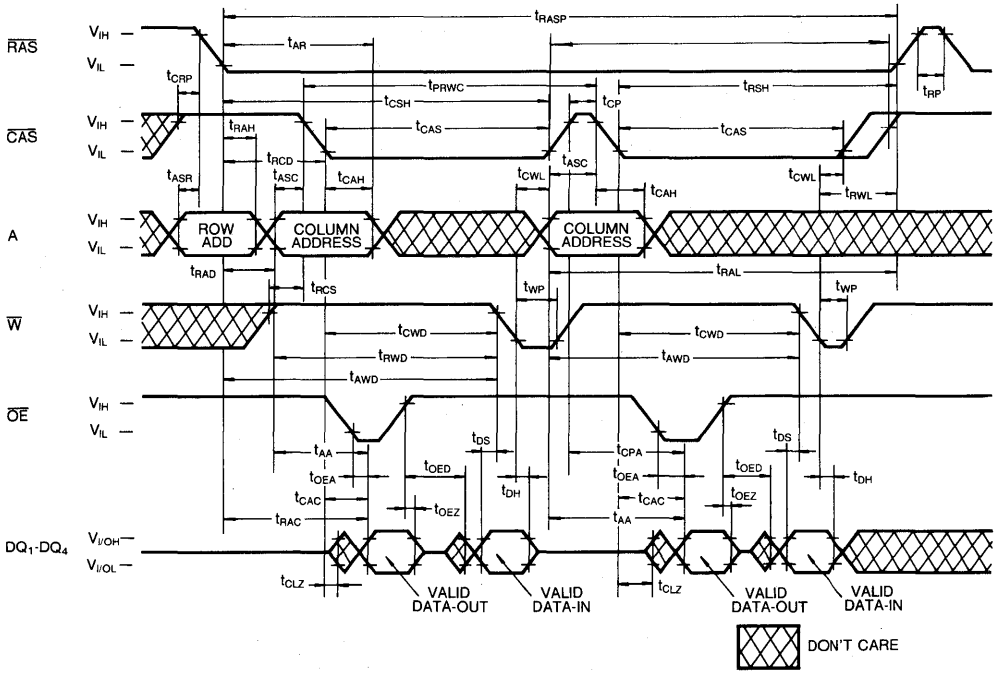


TIMING DIAGRAMS (Continued)

HYPER PAGE WRITE CYCLE (EARLY WRITE)

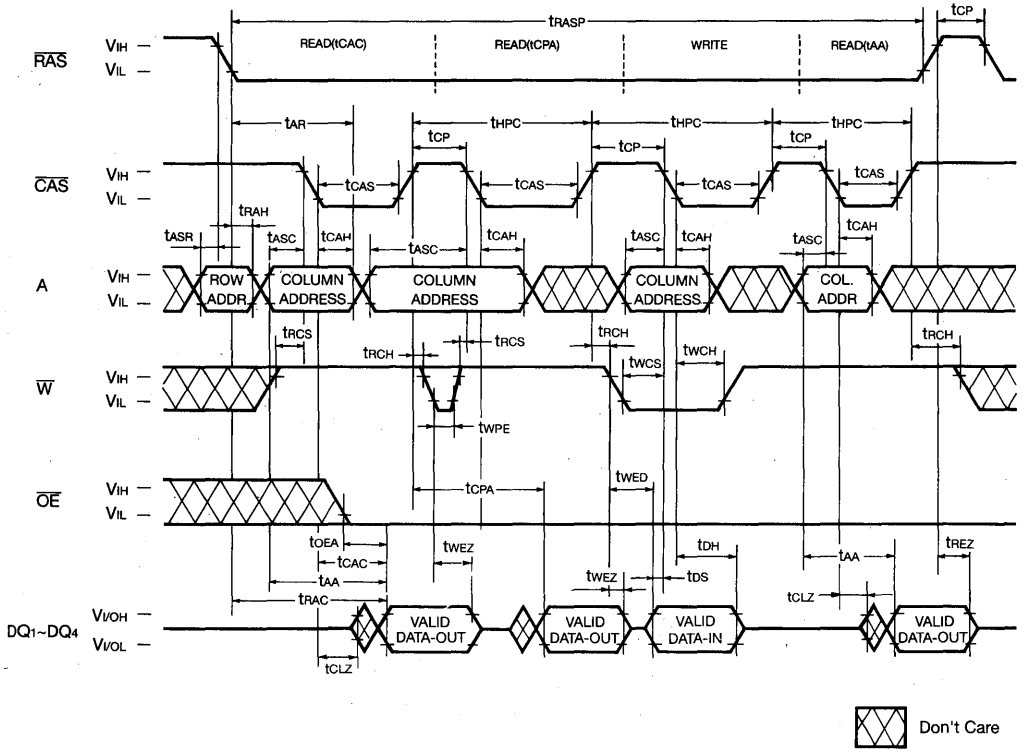


HYPER PAGE READ-MODIFY-WRITE CYCLE



SAMSUNG ELECTRONICS

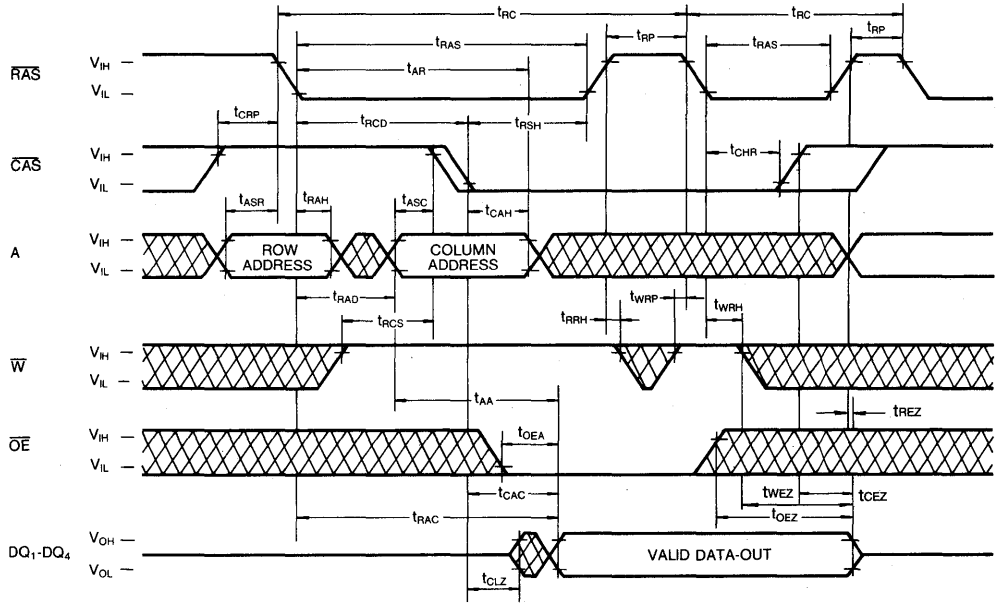
HYPER PAGE READ AND WRITE MIXED CYCLE



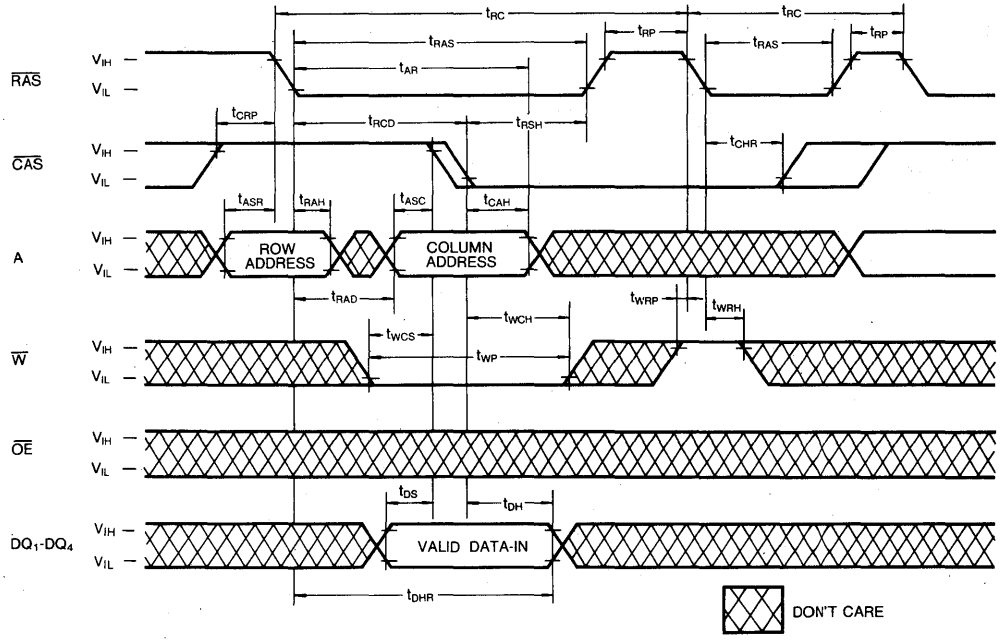
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



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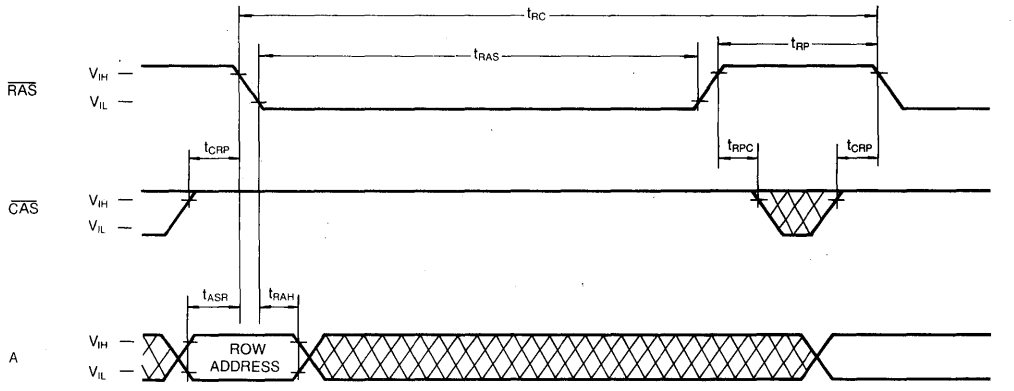
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

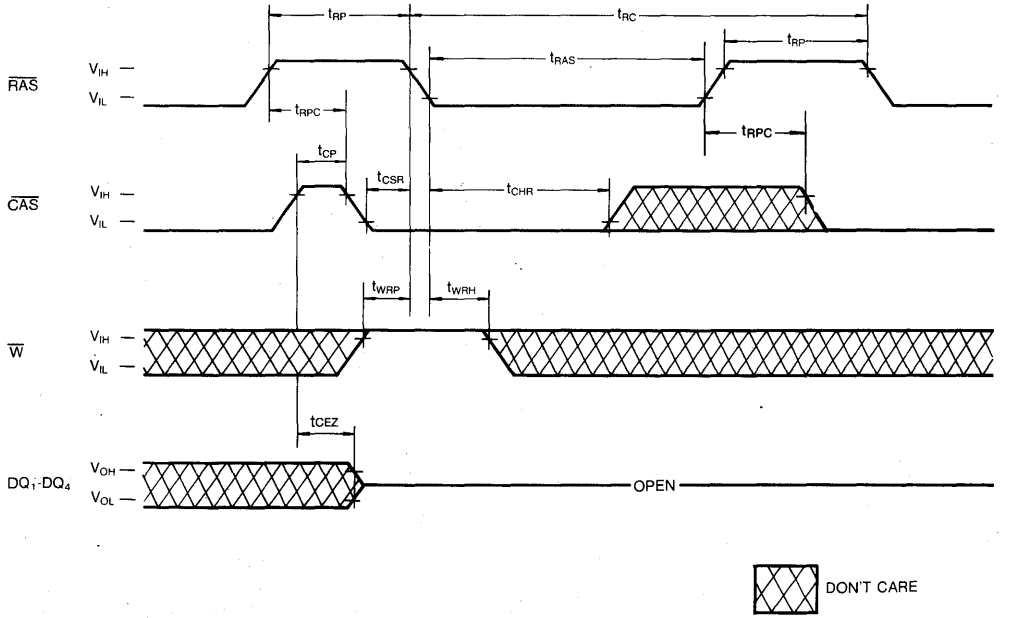
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



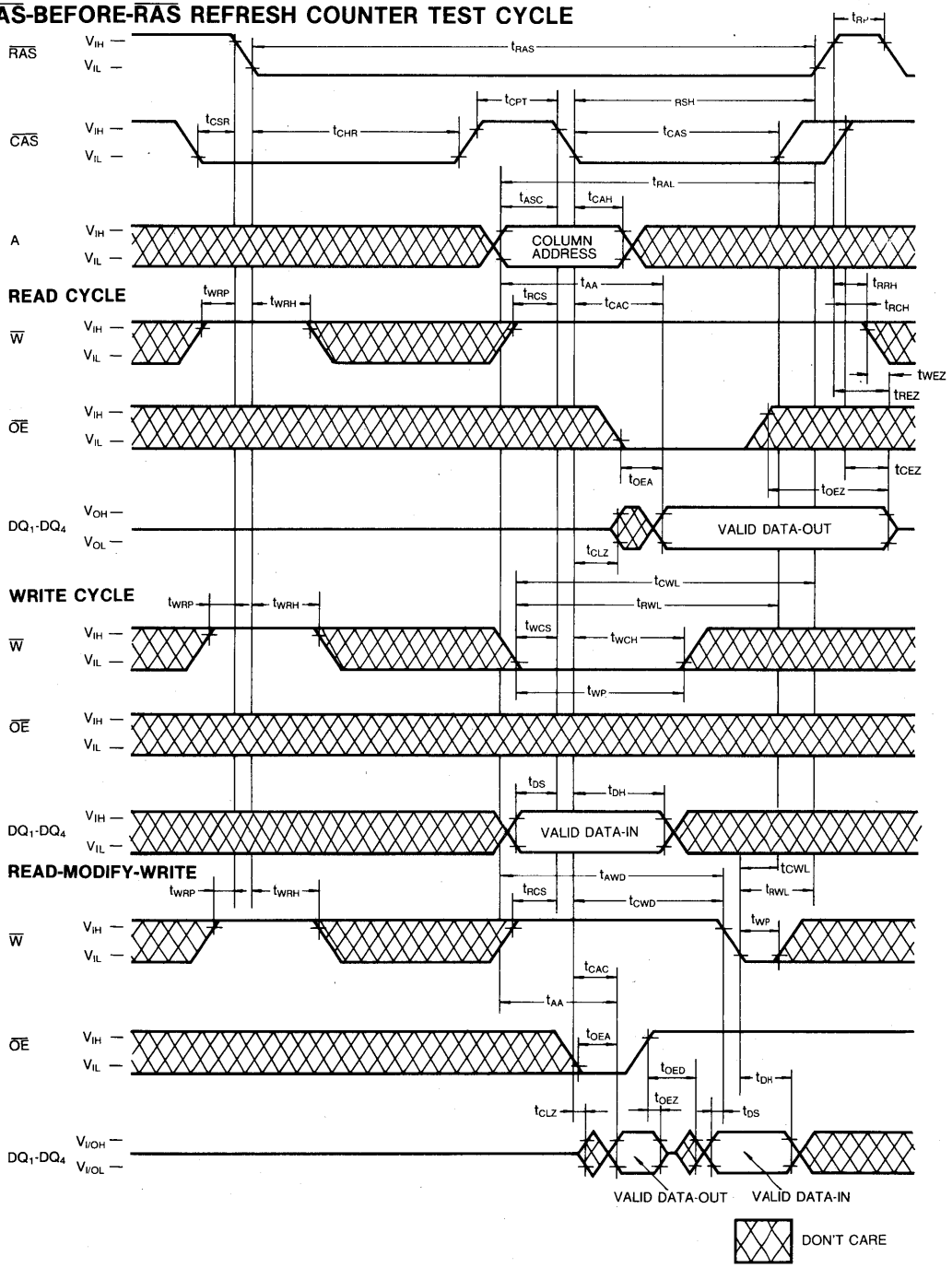
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{OE}$, Address=Don't Care



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

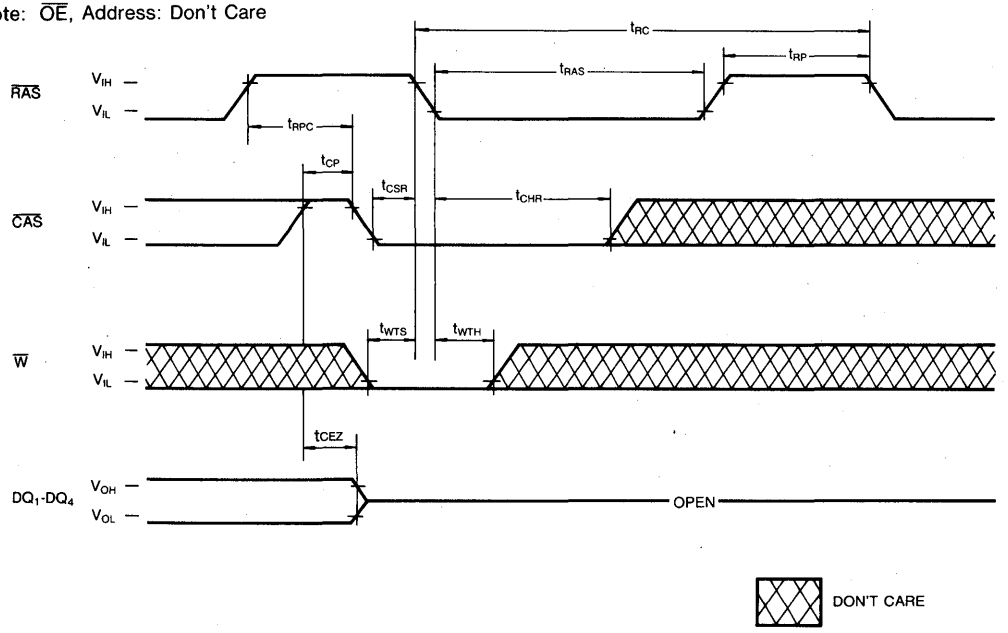


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

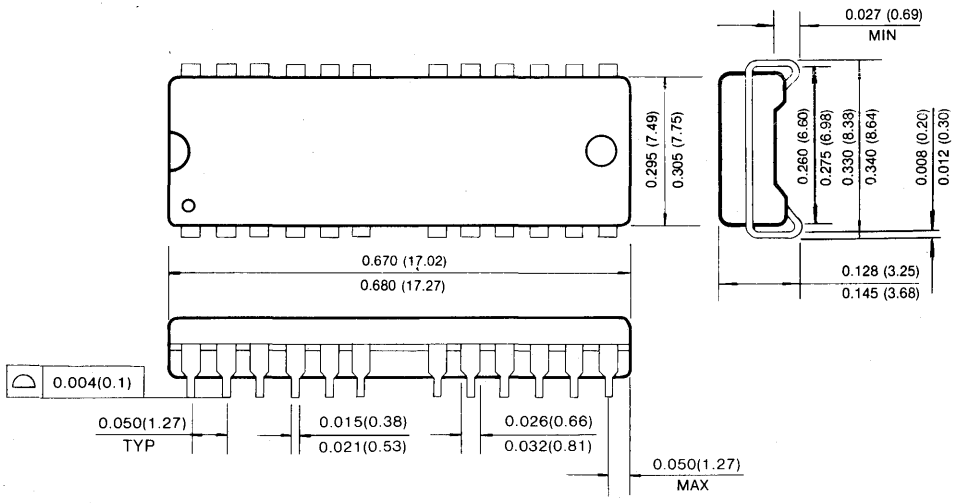
Note: $\overline{OE}$, Address: Don't Care



PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



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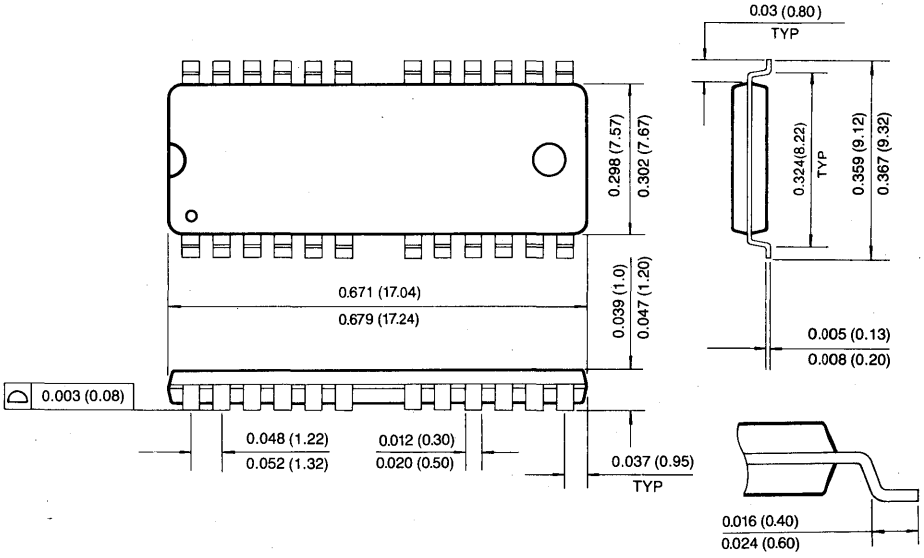
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

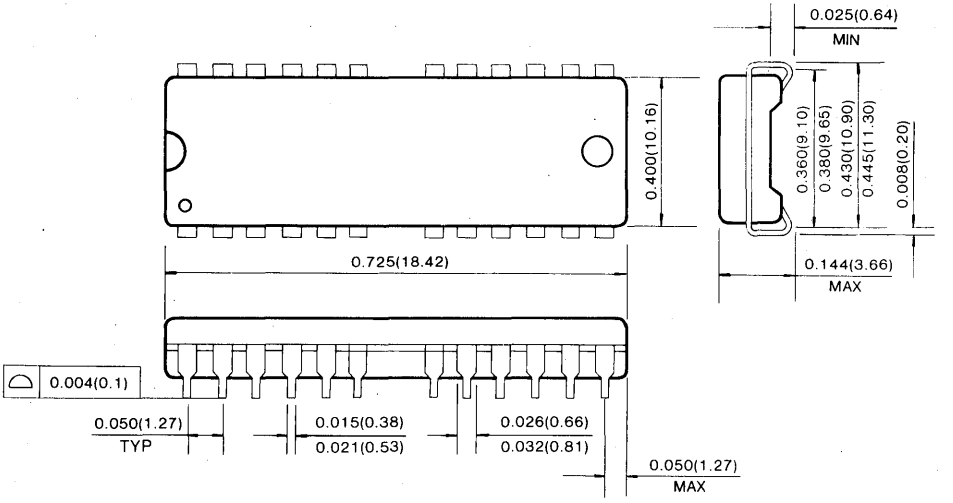


SAMSUNG ELECTRONICS

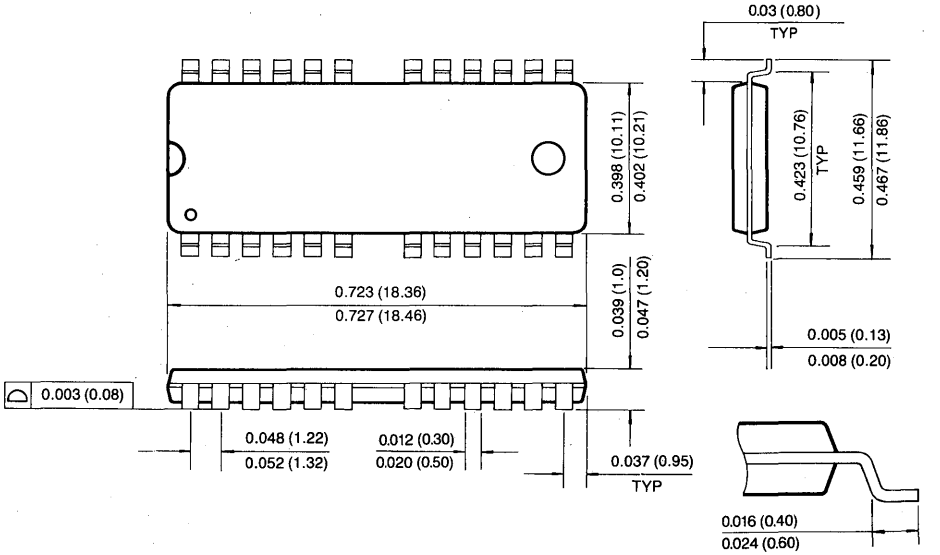
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



16M × 1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM41V16000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM41V16000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM41V16000A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Common I/O using Early Write**
- **Single+3.3V±0.3V power supply**
- **4096 cycles/64ms refresh(Normal)**
- **4096 cycles/128ms refresh(Low power & Self Ref.)**
- **4096 cycles/256ms refresh(Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

GENERAL DESCRIPTION

The Samsung KM41V16000A/AL/ALL/ASL is a high speed CMOS 16,777,216 bit × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM41V16000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM41V16000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

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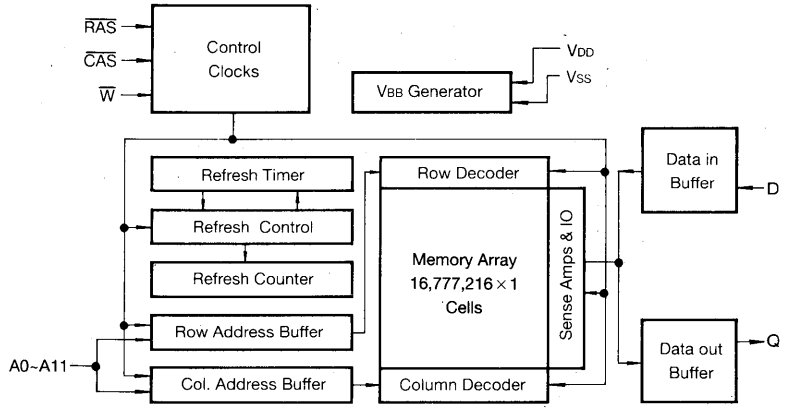
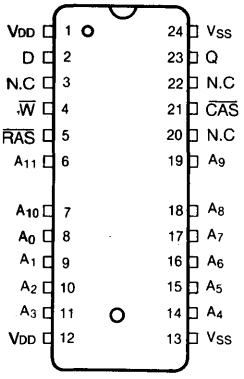
FUNCTIONAL BLOCK DIAGRAM



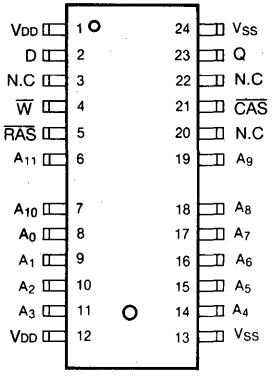
PIN CONFIGURATION (Top Views)

• **KM41V16000 AJ/ALJ/ALLJ/ASLJ /AK/ALK/ALLK/ASLK**



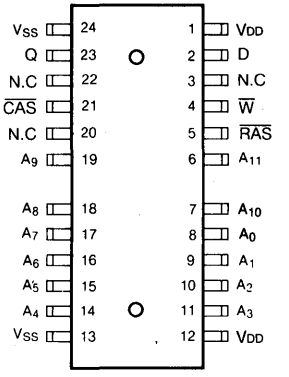
J : 400MIL
K : 300MIL

• **KM41V16000 AT/ALT/ALLT/ASLT /AS/ALS/ALLS/ASLS**



T : 400MIL(Forward)
S : 300MIL(Forward)

• **KM41V16000 ATR/ALTR/ALLTR/ASLTR /ASR/ALSR/ALLSR/ASLSR**



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
D	Data In
Q	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
VCC	Power(+3.3V)
VDD	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 ~ 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM41V16000A/AL/ALL/ASL-6	I_{CC1}	-	80	mA
	KM41V16000A/AL/ALL/ASL-7			70	mA
	KM41V16000A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM41V16000A	I_{CC2}	-	2	mA
	KM41V16000AL			1	mA
	KM41V16000ALL			1	mA
	KM41V16000ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM41V16000A/AL/ALL/ASL-6	I_{CC3}	-	80	mA
	KM41V16000A/AL/ALL/ASL-7			70	mA
	KM41V16000A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM41V16000A/AL/ALL/ASL-6	I_{CC4}	-	70	mA
	KM41V16000A/AL/ALL/ASL-7			60	mA
	KM41V16000A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM41V16000A	I_{CC5}	-	1	mA
	KM41V16000AL			300	μA
	KM41V16000ALL			200	μA
	KM41V16000ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM41V16000A/AL/ALL/ASL-6	I_{CC6}	-	80	mA
	KM41V16000A/AL/ALL/ASL-7			70	mA
	KM41V16000A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=31.25μS(L-Ver.) 62.5μS(SL-Ver.), T_{RAS}=T_{RAS} min.~300ns	KM41V16000AL	I_{CC7}	-	450	μA
	KM41V16000ASL			350	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$= A_0-A_{11}=V_{DD}-0.2V or 0.2V D, Q=V_{DD}-0.2V, 0.2V or Open	KM41V16000ALL	I_{CC8}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	-	7	pF
Input Capacitance (A_0-A_{11})	C_{IN2}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	-	7	pF
Input Capacitance (Q)	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Test Condition : V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64	ms	
Refresh period (Low power & self Ref.)	t_{REF}		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	60		70		80		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	30		35		40		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	60		70		75		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ refresh)	t_{RASS}	100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{RPS}	110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHS}	-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

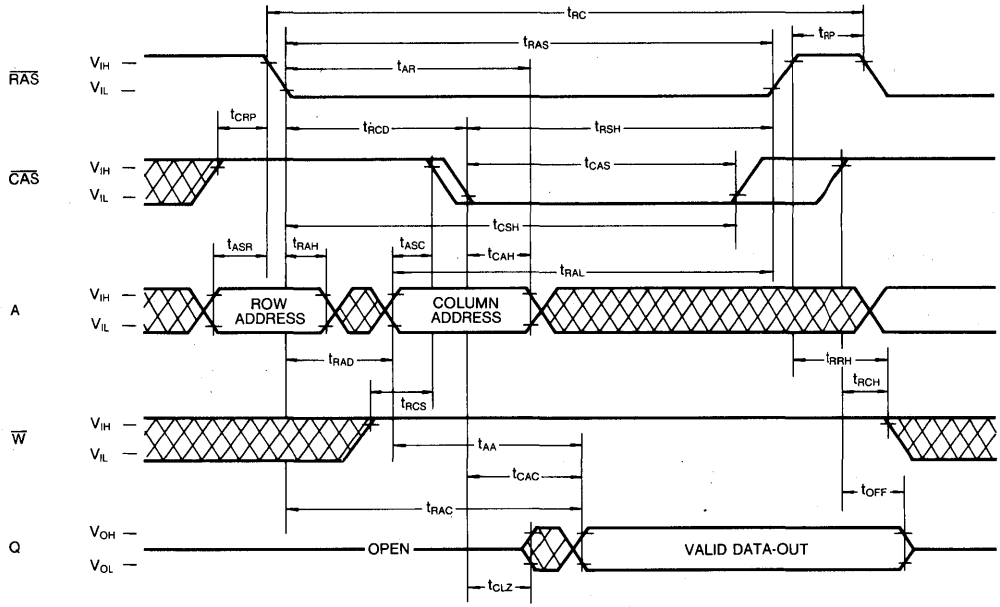
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	20		25		25		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	65		75		85		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		45		ns	8
Fast Page mode cycle time	t_{PC}	45		50		55		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	65		75		80		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3

NOTES

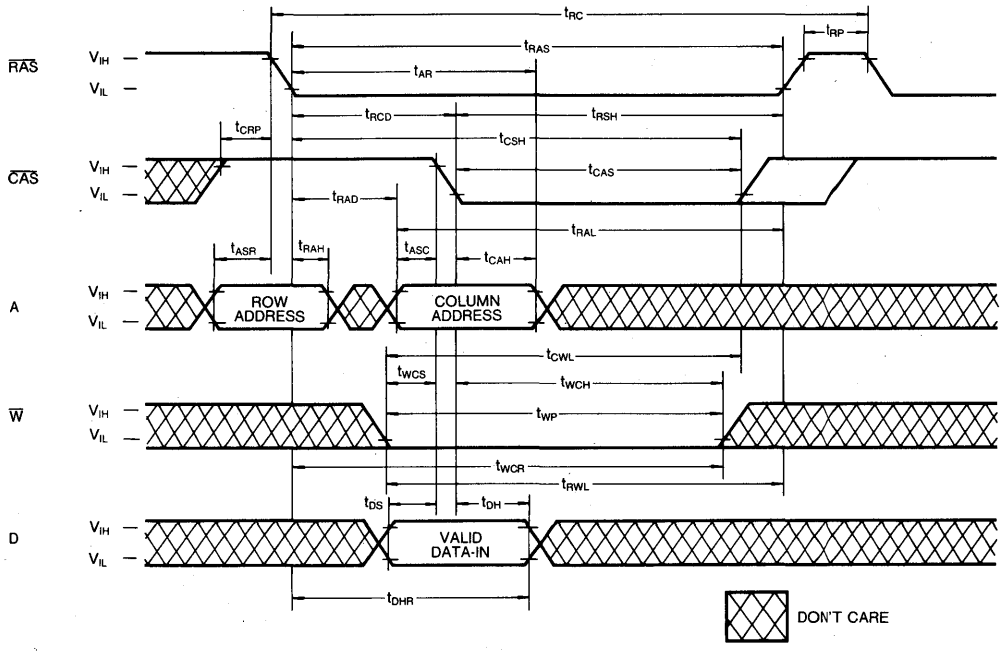
1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 100pF and V_{oh}=2.0V(I_{OUT}=2mA), V_{ol}=0.8V(I_{OUT}=2mA)
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within **16ms** before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS

READ CYCLE

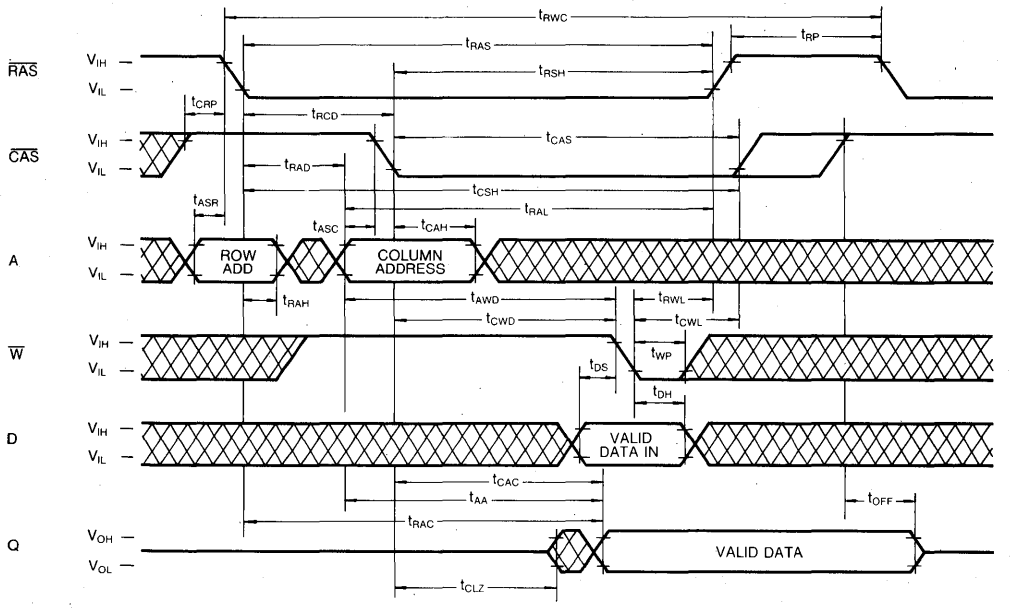


WRITE CYCLE (EARLY WRITE)

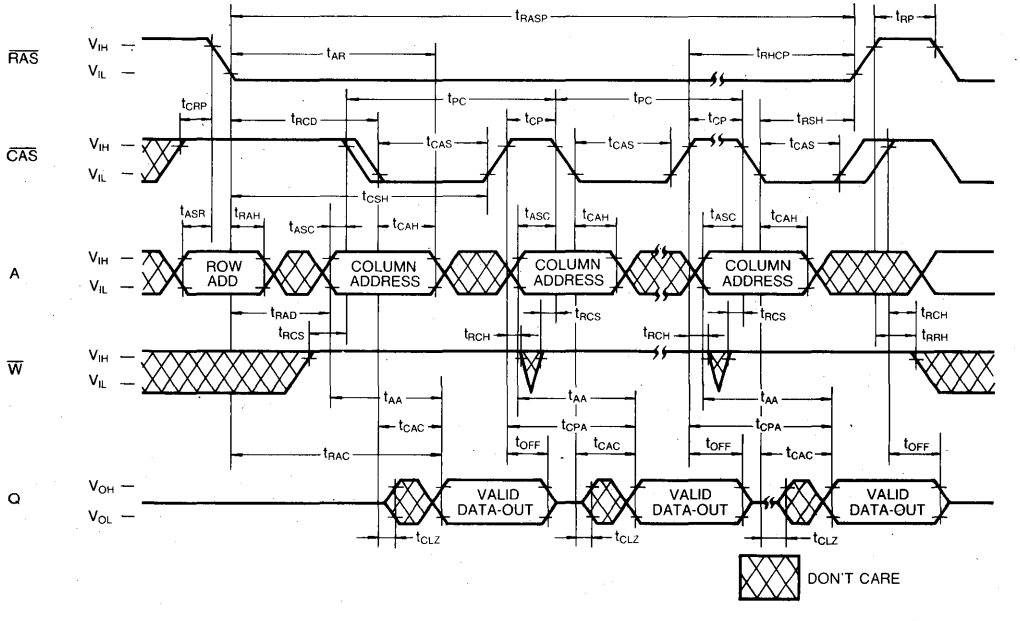


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

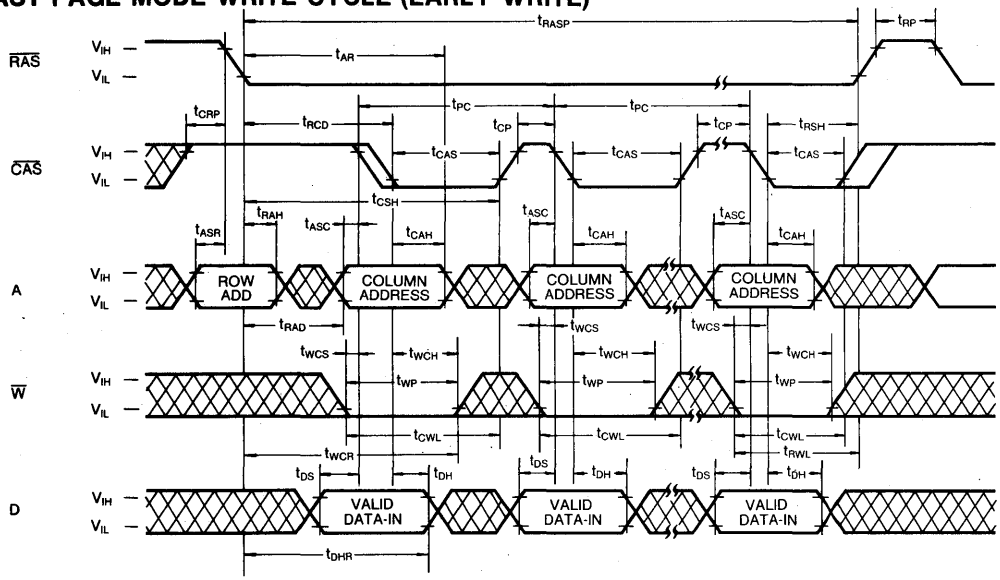


FAST PAGE MODE READ CYCLE

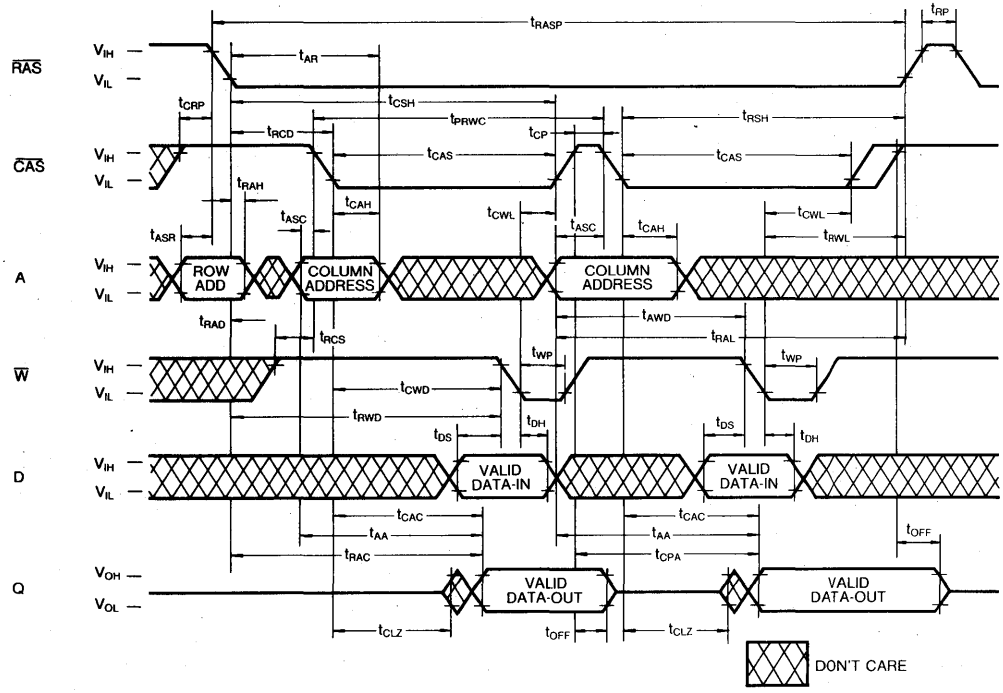


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



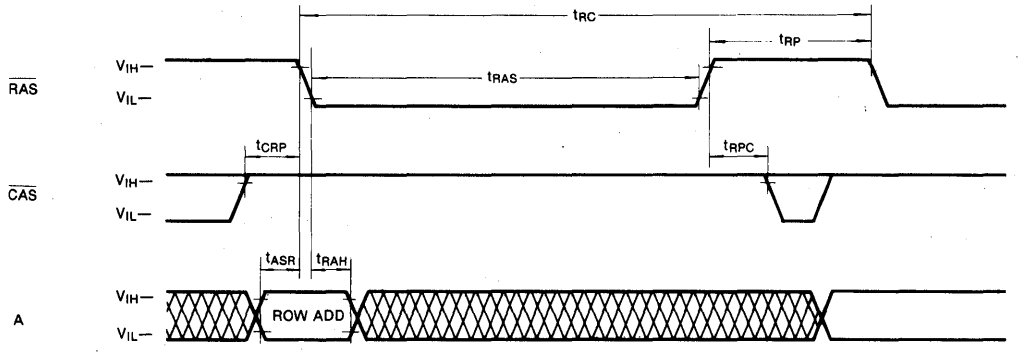
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

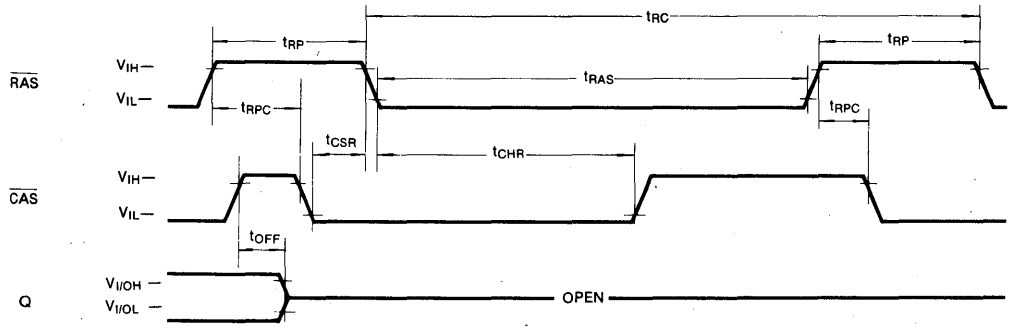
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$ = Don't care



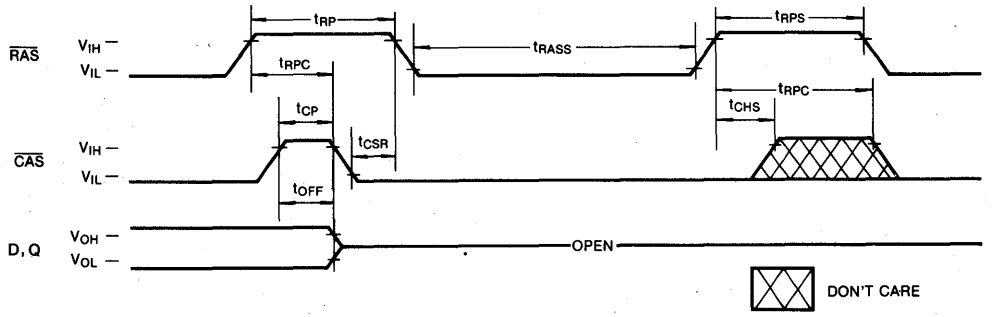
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, A=Don't Care



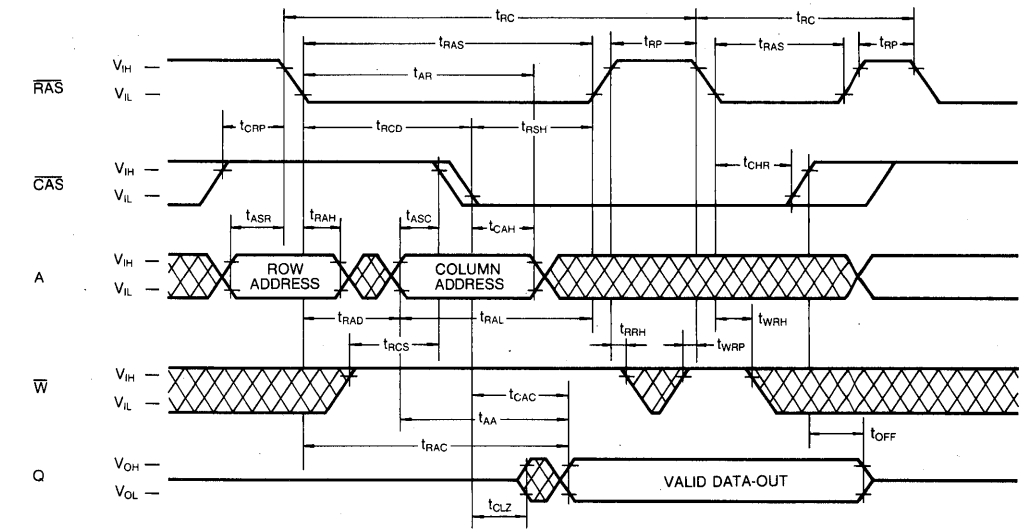
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, A=Don't Care

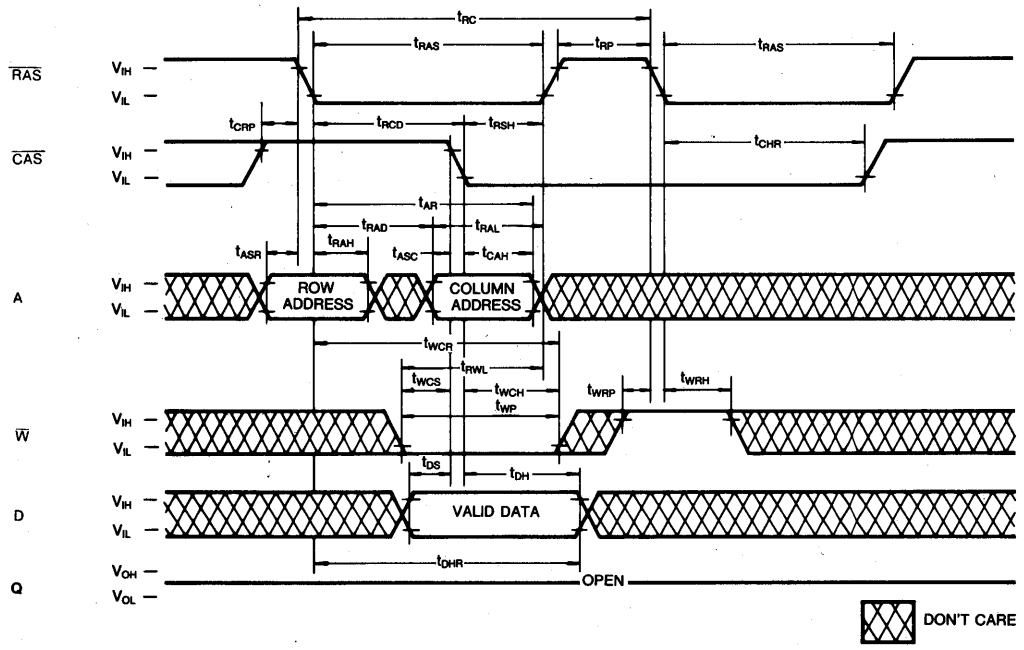


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



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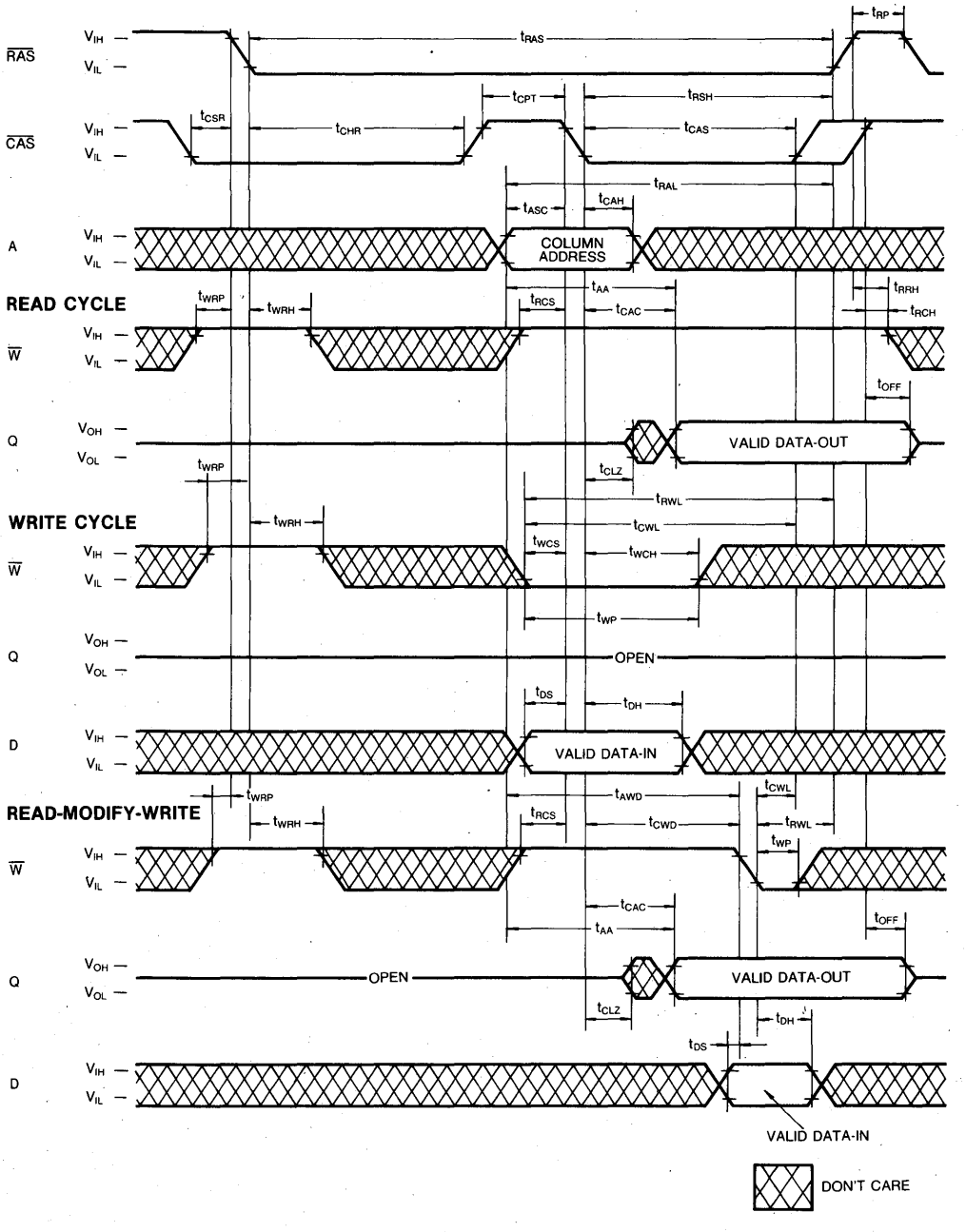
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

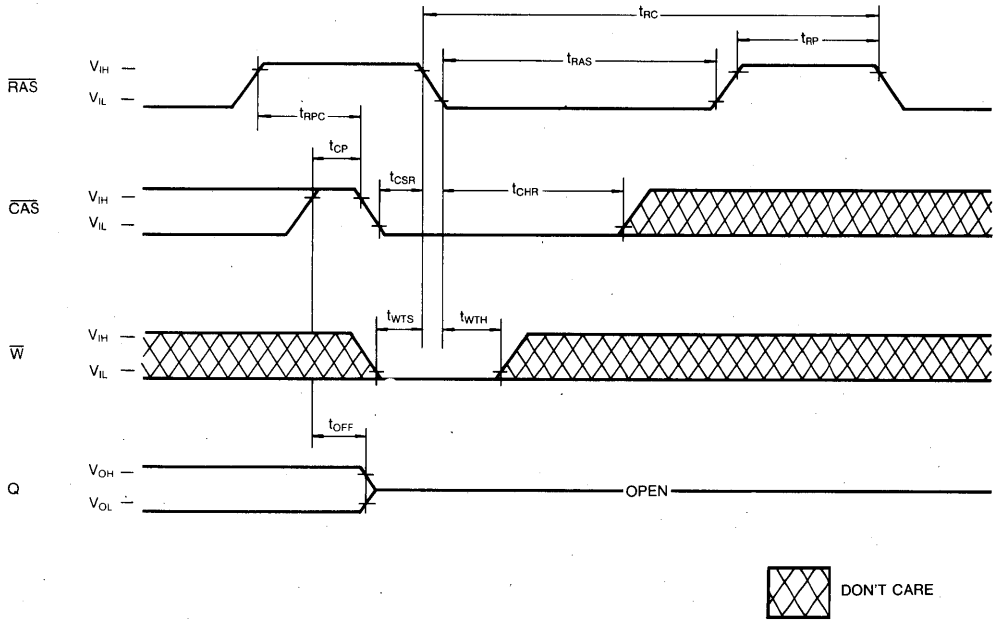


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: D, Address: Don't Care



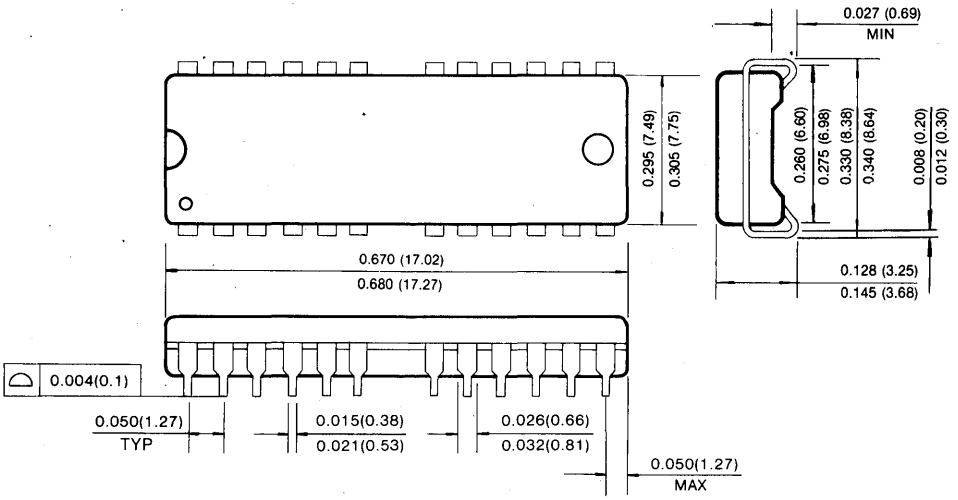
TEST MODE DESCRIPTION

The KM41V16000A/AL/ALL/ASL is the RAM organized 16,777,216 words by 1 bit, it is internally organized 1, 048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0, A_1, A_{10} and A_{11} are not used. If, upon reading, 16 bits are equal (all "1"s or "0"s) the Q pin indicates a "1".
If they were not equal, the Q pin would indicate a "0". In "Test Mode", the 16M DRAM can be tested as if it were a 1M×1 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/16 in cases of N test pattern).

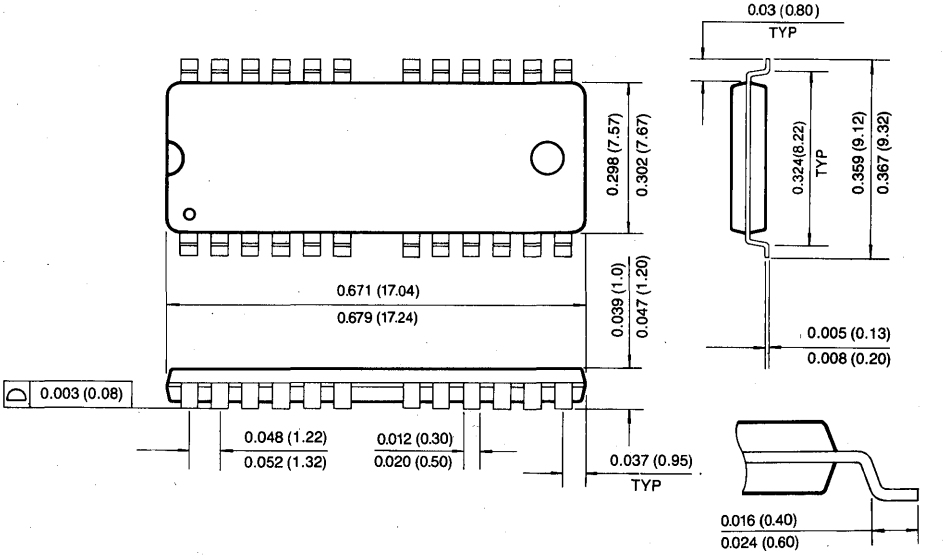
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

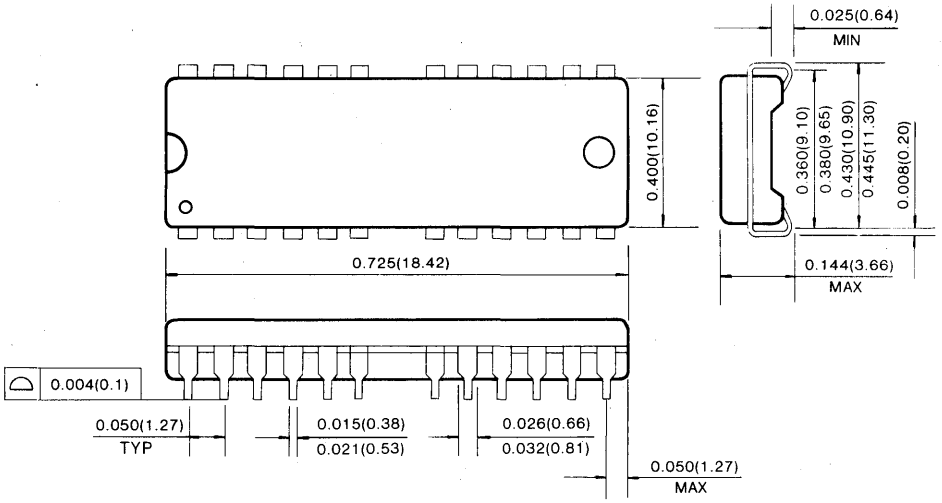


SAMSUNG ELECTRONICS

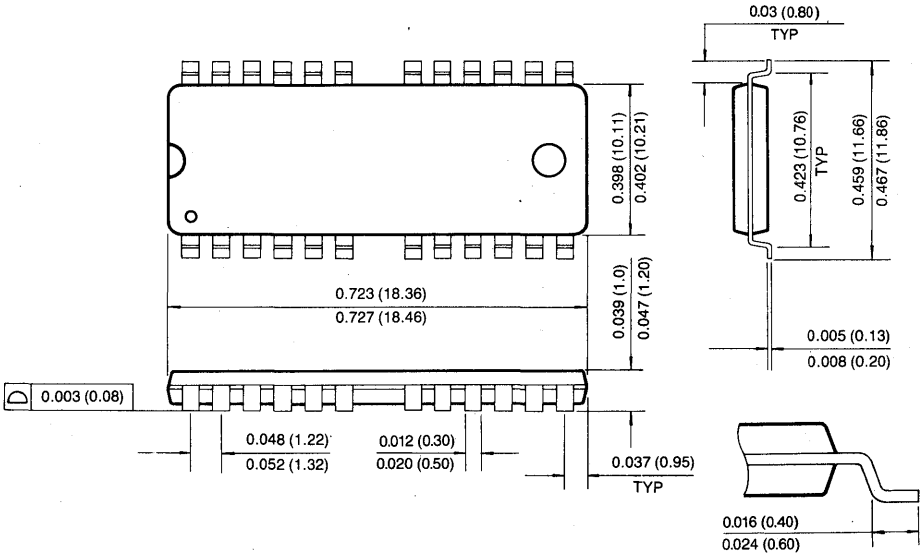
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M ×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM44V4000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44V4000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44V4000A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Single+3.3V±0.3V power supply**
- **4096 cycles/64ms refresh (Normal DRAM)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

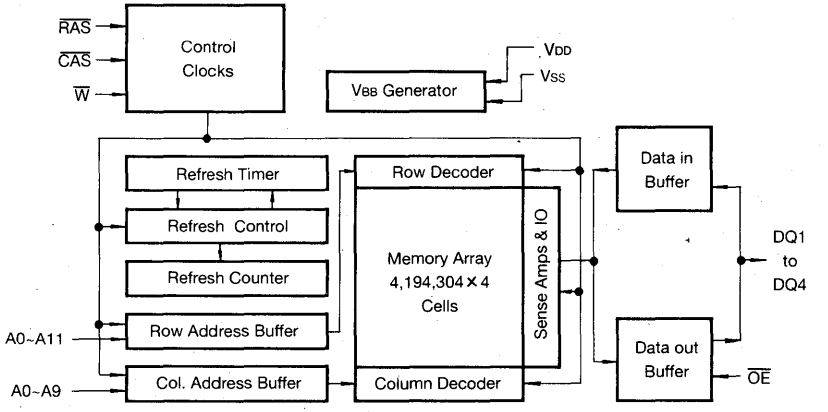
The Samsung KM44V4000A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44V4000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

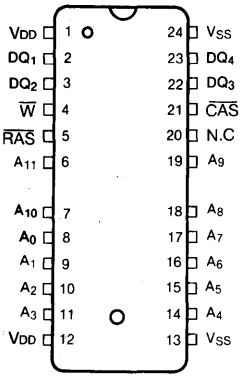
The KM44V4000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



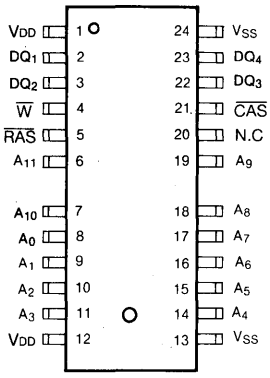
PIN CONFIGURATION (Top Views)

• **KM44V4000 AJ/ALJ/ALLJ/ASLJ /AK/ALK/ALLK/ASLK**



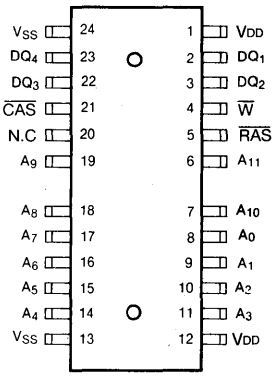
J : 400MIL
K : 300MIL

• **KM44V4000 AT/ALT/ALLT/ASLT /AS/ALS/ALLS/ASLS**



T : 400MIL(Forward)
S : 300MIL(Forward)

• **KM44V4000 ATR/ALTR/ALLTR/ASLTR /ASR/ALSR/ALLSR/ASLSR**



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1~4	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VDD	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 ~ 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44V4000A/AL/ALL/ASL-6	I_{CC1}	-	80	mA
	KM44V4000A/AL/ALL/ASL-7			70	mA
	KM44V4000A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44V4000A	I_{CC2}	-	2	mA
	KM44V4000AL			1	mA
	KM44V4000ALL			1	mA
	KM44V4000ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44V4000A/AL/ALL/ASL-6	I_{CC3}	-	80	mA
	KM44V4000A/AL/ALL/ASL-7			70	mA
	KM44V4000A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44V4000A/AL/ALL/ASL-6	I_{CC4}	-	70	mA
	KM44V4000A/AL/ALL/ASL-7			60	mA
	KM44V4000A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM44V4000A	I_{CC5}	-	1	mA
	KM44V4000AL			300	μA
	KM44V4000ALL			200	μA
	KM44V4000ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44V4000A/AL/ALL/ASL-6	I_{CC6}	-	80	mA
	KM44V4000A/AL/ALL/ASL-7			70	mA
	KM44V4000A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=31.25μS(L-Ver.) 62.5μS(SL-Ver.), T_{RAS}=T_{RAS} min.~300ns	KM44V4000AL	I_{CC7}	-	450	μA
	KM44V4000ASL			350	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{DD}-0.2V or 0.2V DQ_1~DQ_4=V_{DD}-0.2V, 0.2V or Open	KM44V4000ALL	I_{CC8}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Test Condition : V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal DRAM only)	t_{REF}		64		64		64	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ commend hold time	t_{OEH}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Fast Page mode cycle time	tPC	45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	20		25		25		ns	

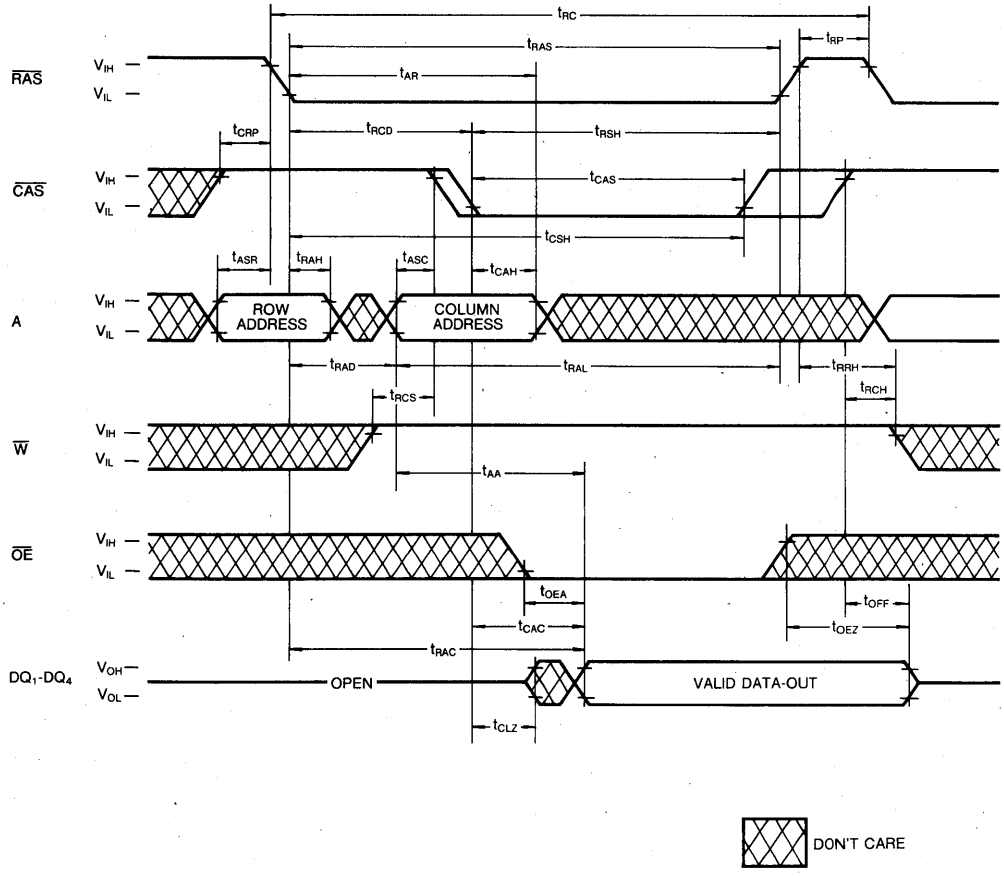
5

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 100pF and V_{oh}=2.0V(I_{OUT}=2mA), V_{ol}=0.8V(I_{OUT}=2mA)
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS

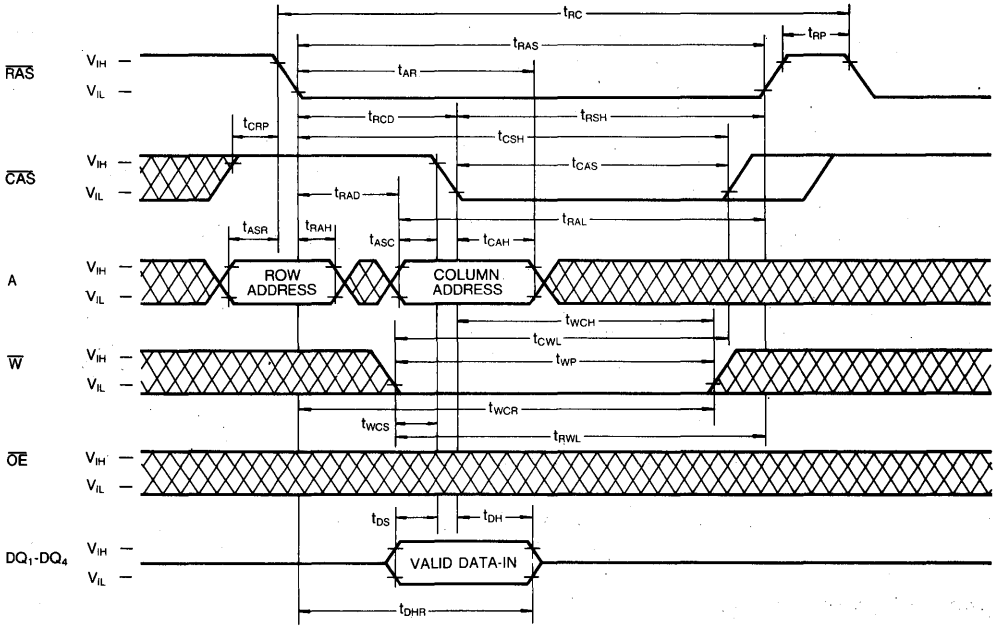
READ CYCLE



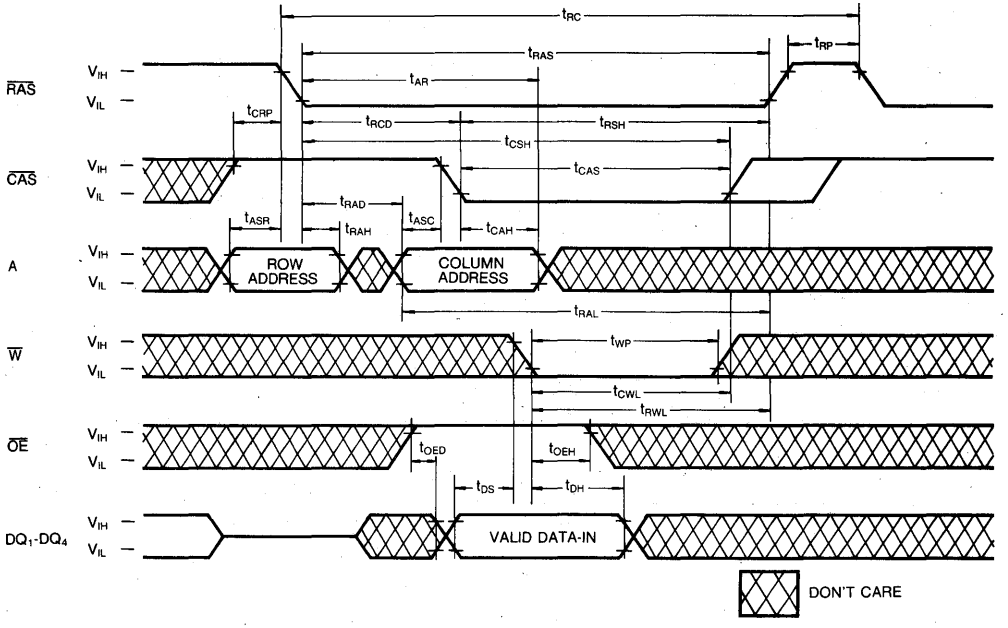
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



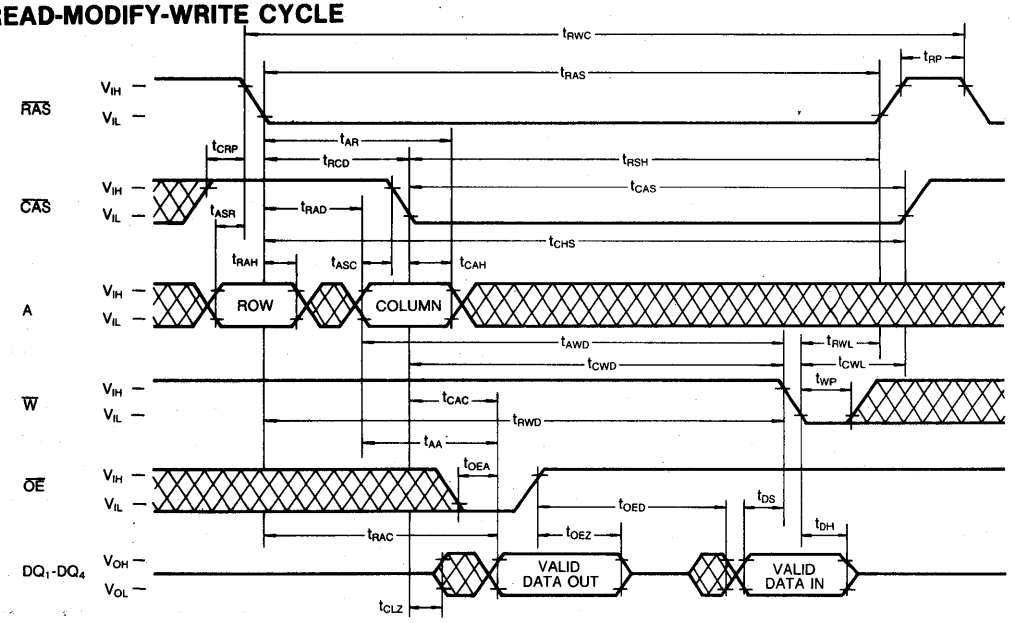
WRITE CYCLE (OE CONTROLLED WRITE)



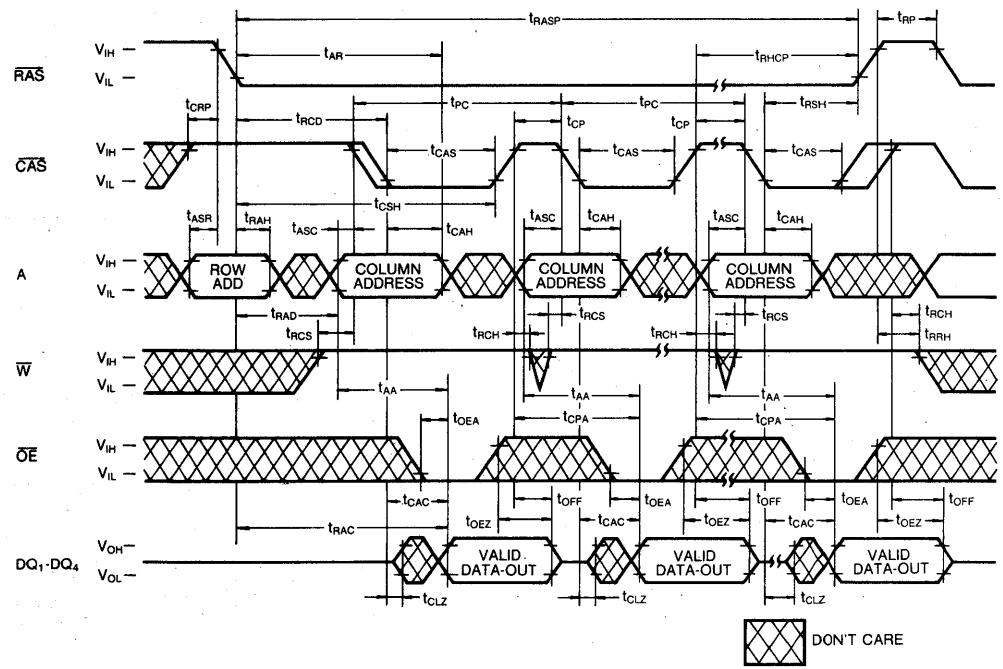
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



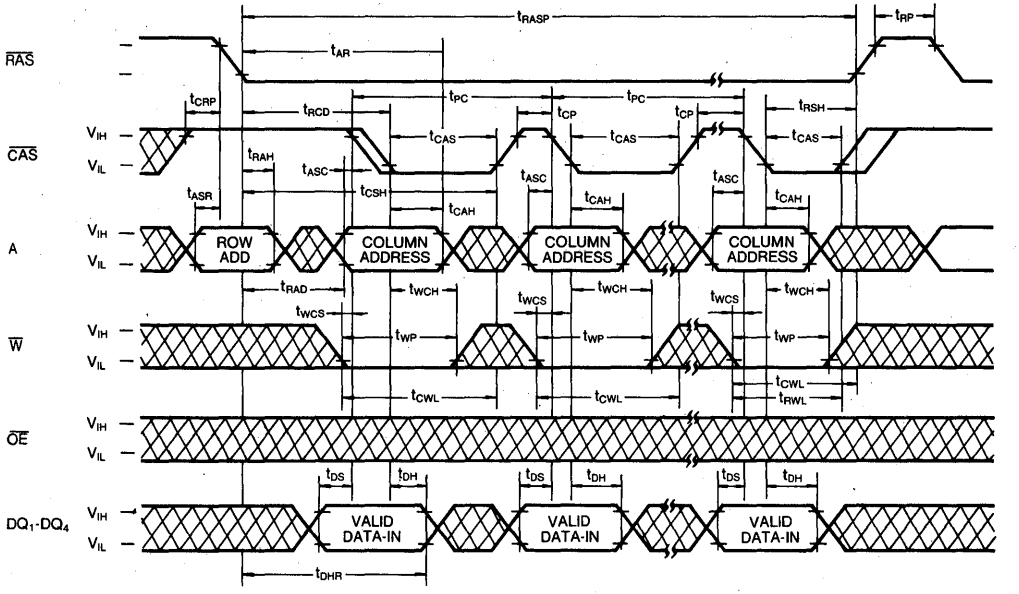
FAST PAGE MODE READ CYCLE



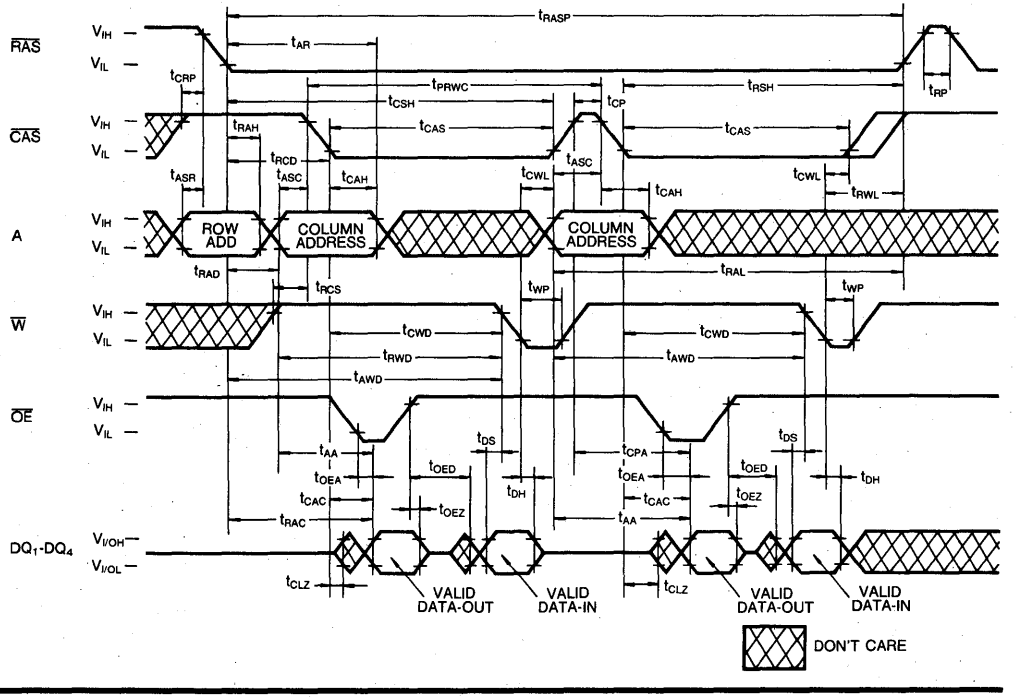
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

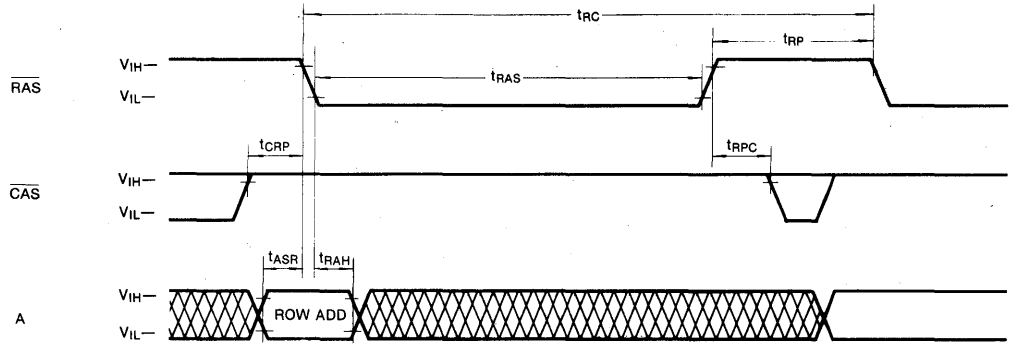


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

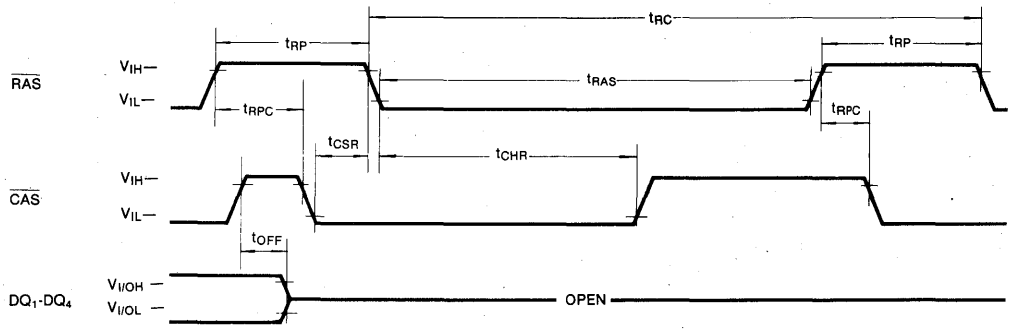
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



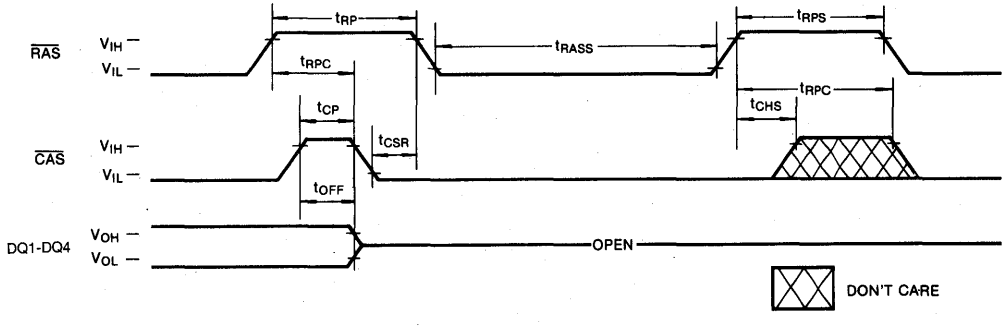
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



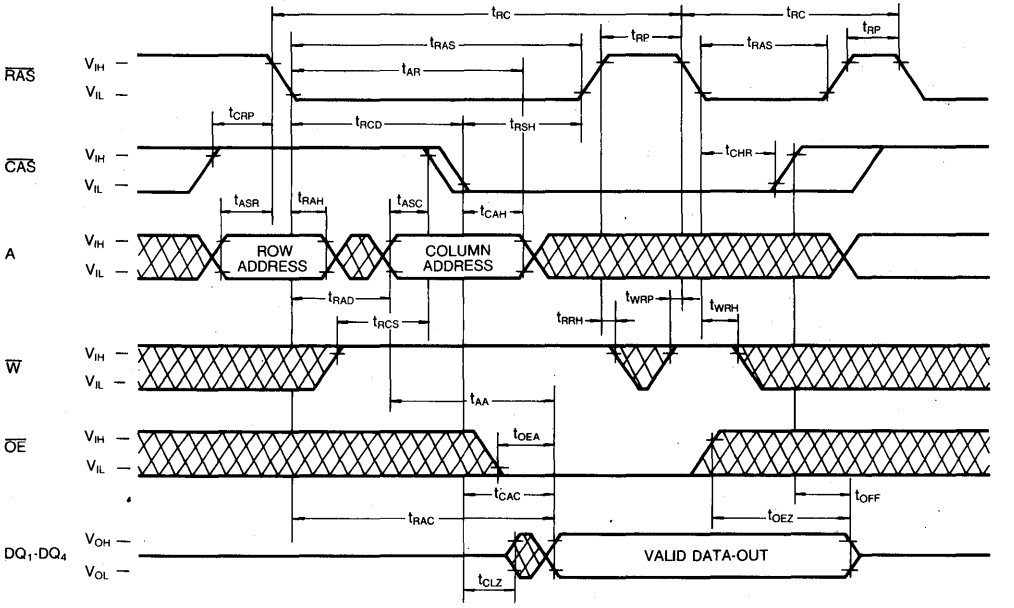
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

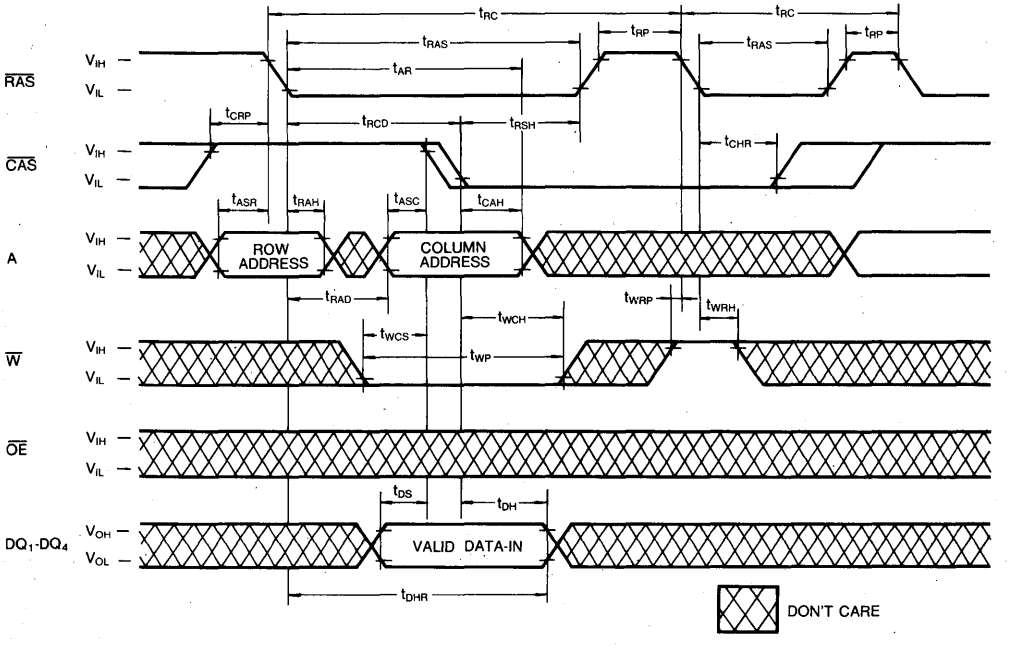


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

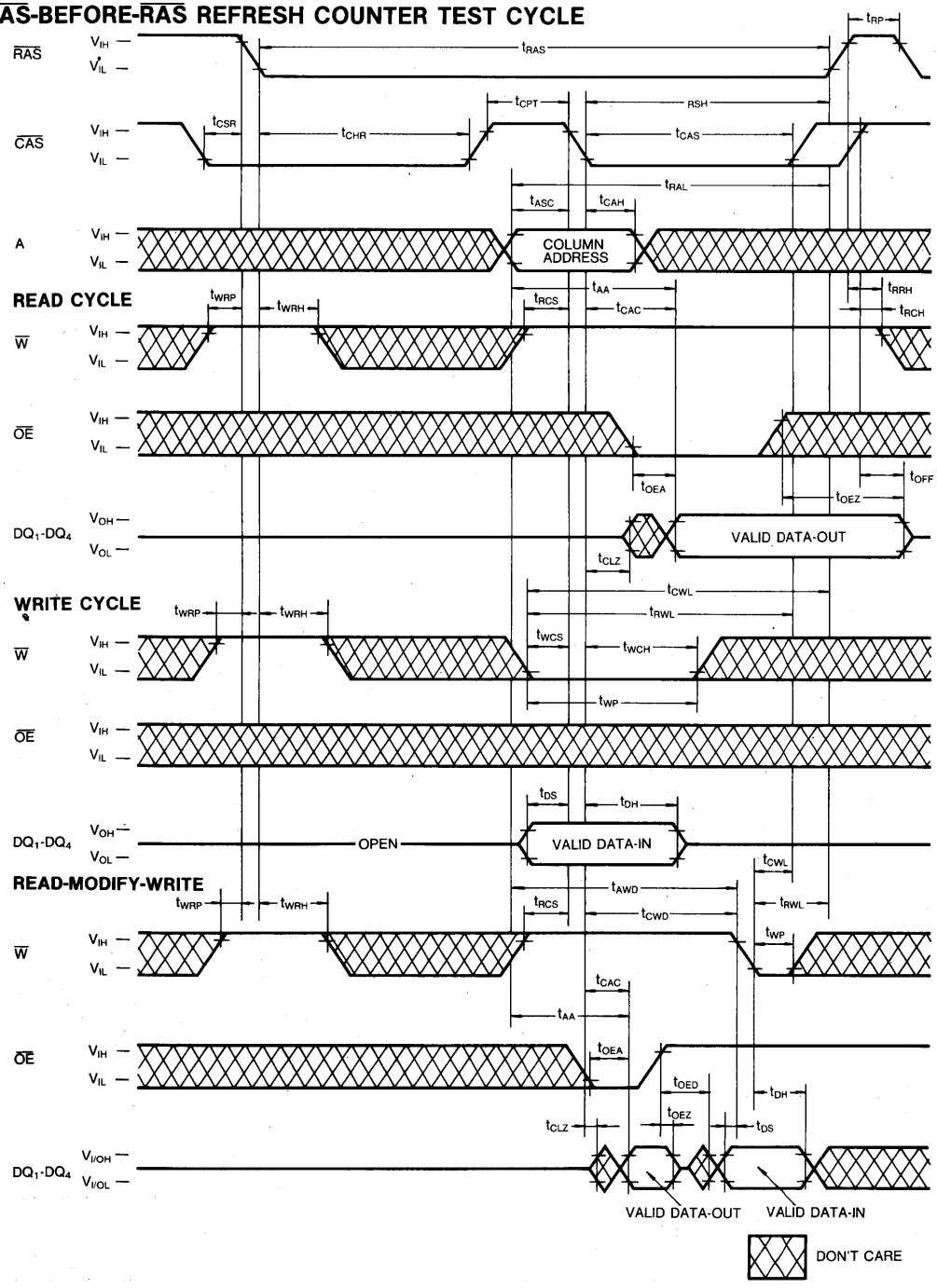


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



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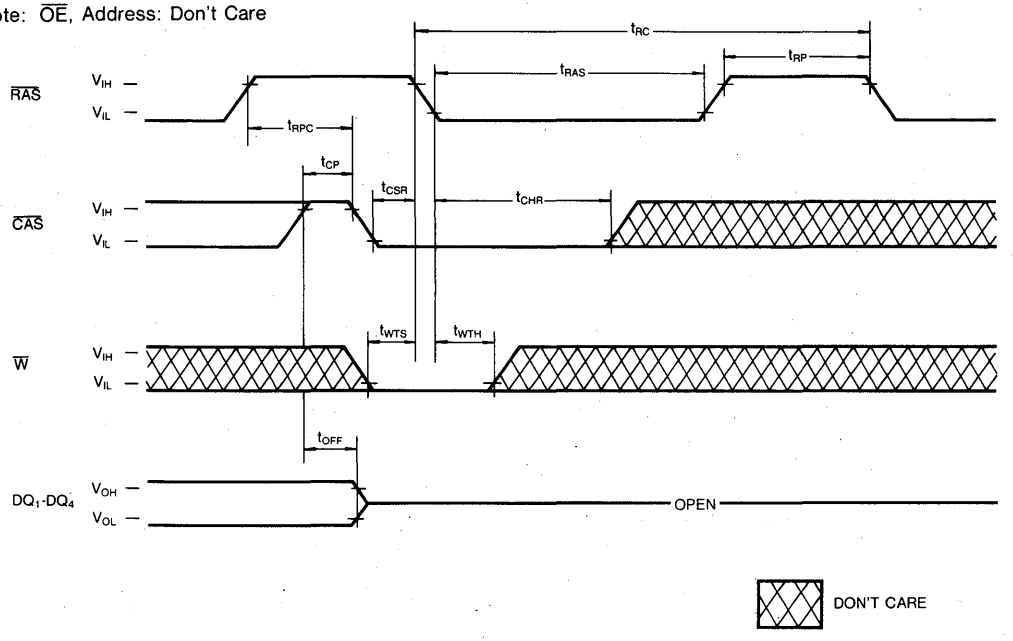
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



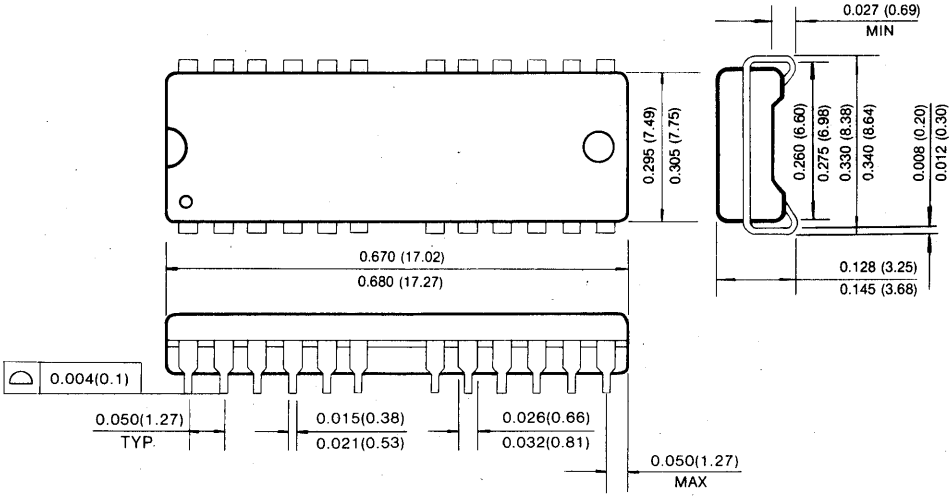
TEST MODE DESCRIPTION

The KM44V4000A/AL/ALL/ASL is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1, 048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 and A_1 are not used. If, upon reading, four bits on one D/Q pin are equal (all "1"s or "0"s) the D/Q pin indicates a "1". If they were not equal, the D/Q pin would indicate a "0". In "Test Mode", the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



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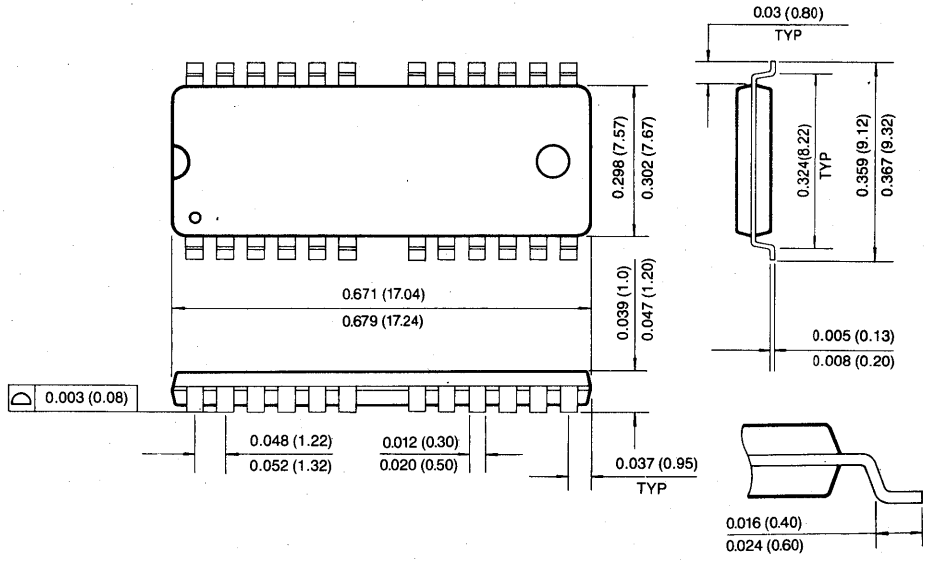
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

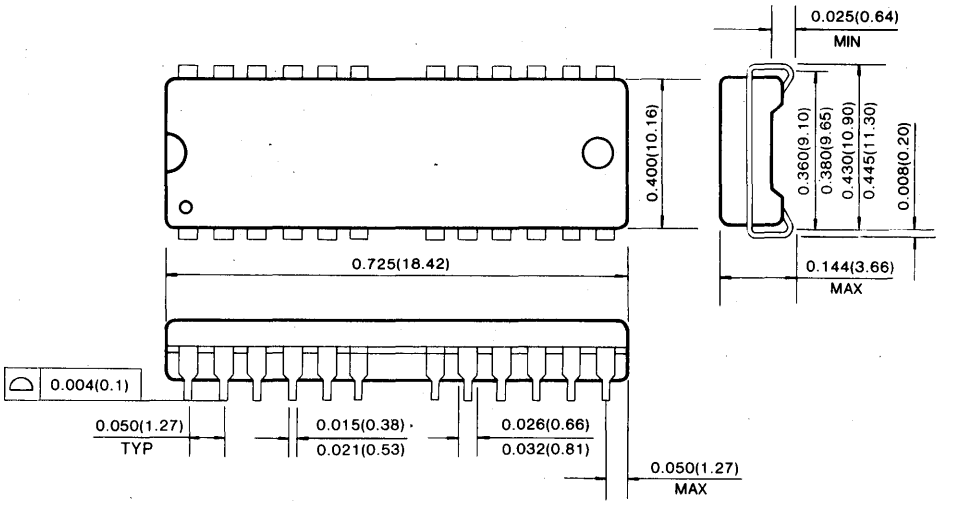


SAMSUNG ELECTRONICS

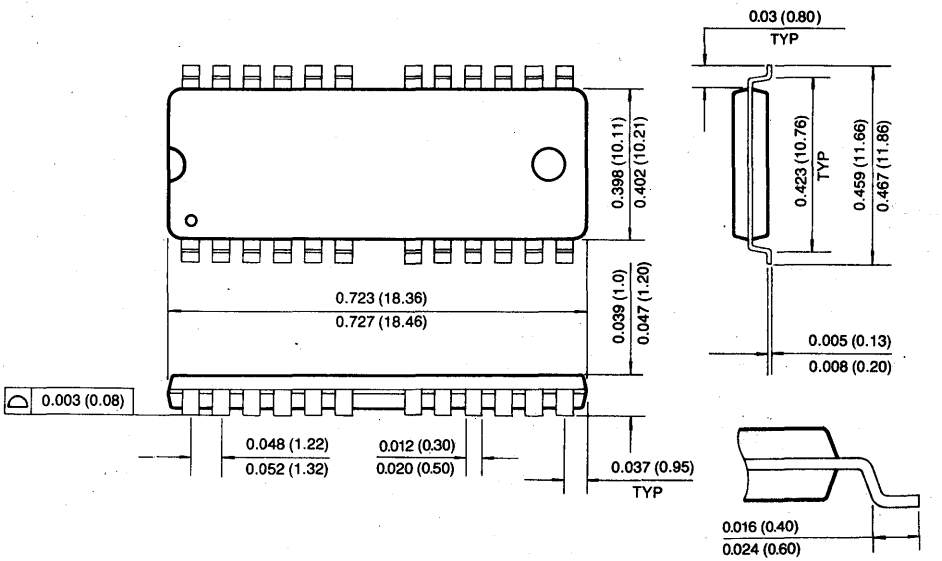
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M ×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM44V4100A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44V4100A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44V4100A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Single+3.3V±0.3V power supply**
- **2048 cycles/32ms refresh (Normal DRAM)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

The Samsung KM44V4100A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44V4100A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44V4100A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

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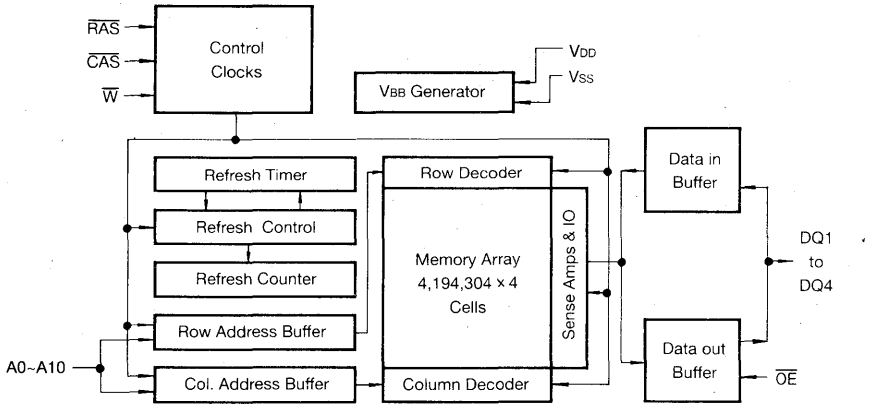
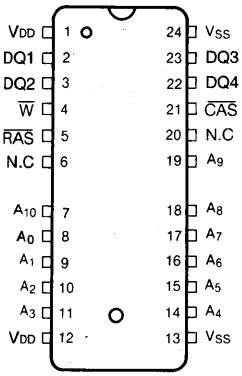
FUNCTIONAL BLOCK DIAGRAM



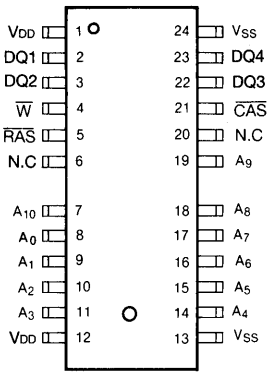
PIN CONFIGURATION (Top Views)

• KM44V4100 AJ/ALJ/ALLJ/ASLJ /AK/ALK/ALLK/ASLK



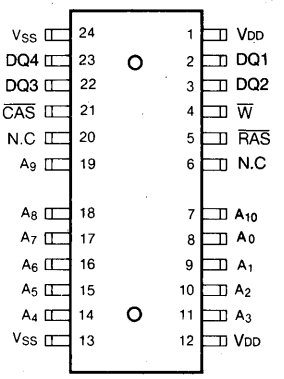
J : 400MIL
K : 300MIL

• KM44V4100 AT/ALT/ALLT/ASLT /AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44V4100 ATR/ALTR/ALLTR/ASLTR /ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ_{1-4}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{DD}	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 ~ 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44V4100A/AL/ALL/ASL-6	I_{CC1}	-	100	mA
	KM44V4100A/AL/ALL/ASL-7			90	mA
	KM44V4100A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44V4100A	I_{CC2}	-	2	mA
	KM44V4100AL			1	mA
	KM44V4100ALL			1	mA
	KM44V4100ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44V4100A/AL/ALL/ASL-6	I_{CC3}	-	100	mA
	KM44V4100A/AL/ALL/ASL-7			90	mA
	KM44V4100A/AL/ALL/ASL-8			80	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44V4100A/AL/ALL/ASL-6	I_{CC4}	-	80	mA
	KM44V4100A/AL/ALL/ASL-7			70	mA
	KM44V4100A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM44V4100A	I_{CC5}	-	1	mA
	KM44V4100AL			300	μA
	KM44V4100ALL			200	μA
	KM44V4100ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44V4100A/AL/ALL/ASL-6	I_{CC6}	-	100	mA
	KM44V4100A/AL/ALL/ASL-7			90	mA
	KM44V4100A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=62.5μS(L-Ver.) 125μS(SL-Ver.), T_{RAS}=T_{RAS} min.~300ns	KM44V4100AL	I_{CC7}	-	400	μA
	KM44V4100ASL			300	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$= A_0-A_{10} =V_{DD}-0.2V or 0.2V DQ_1~DQ_4=V_{DD}-0.2V, 0.2V or Open	KM44V4100ALL	I_{CC8}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{10})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Test Condition : V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal DRAM only)	t_{REF}		32		32		32	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ commend hold time	t_{OEH}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Fast Page mode cycle time	tPC	45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	20		25		25		ns	

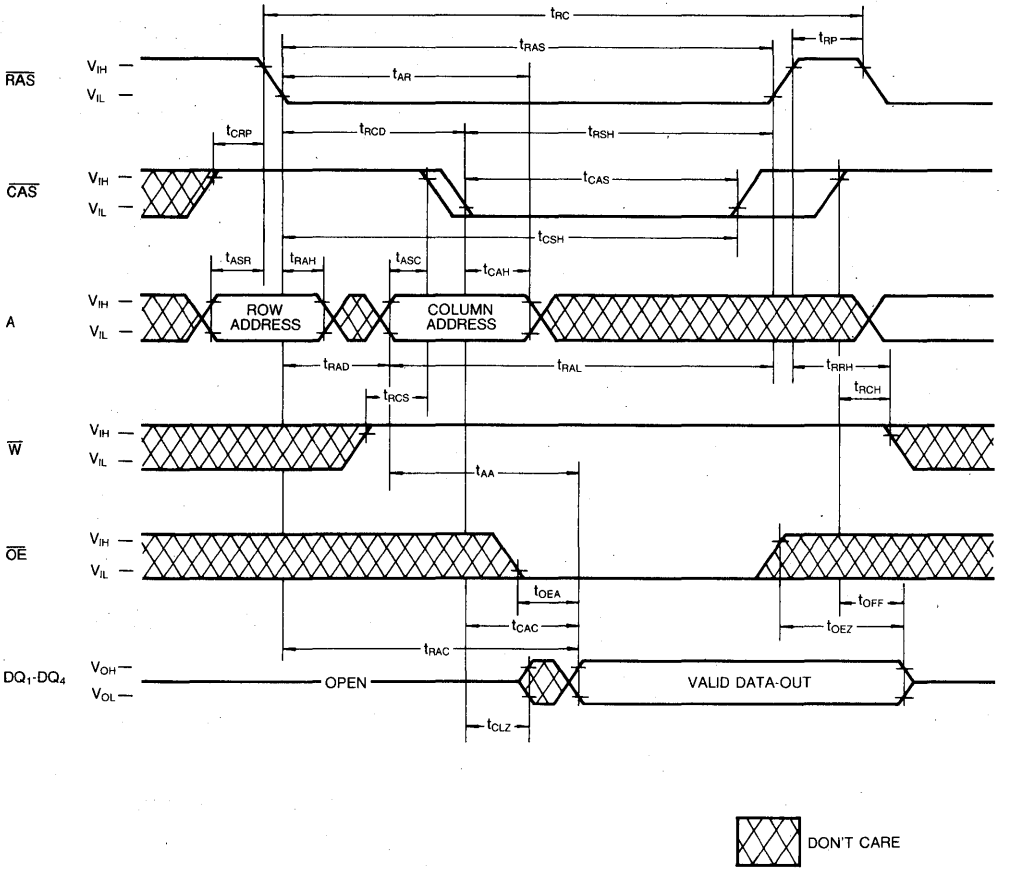
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 100pF and V_{oh}=2.0V(I_{OUT}=2mA), V_{ol}=0.8V(I_{OUT}=2mA)
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

5

TIMING DIAGRAMS

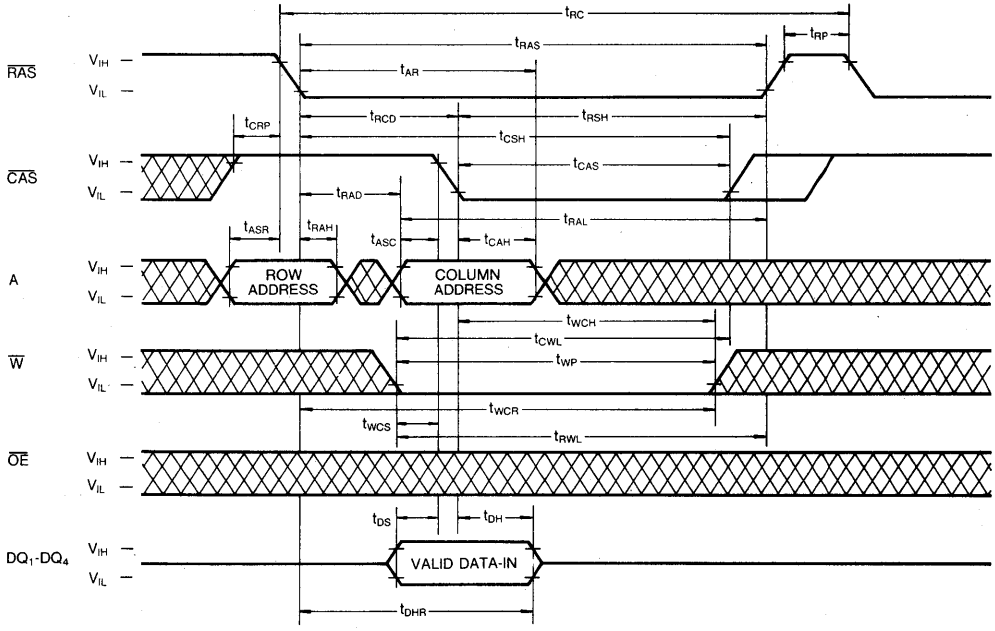
READ CYCLE



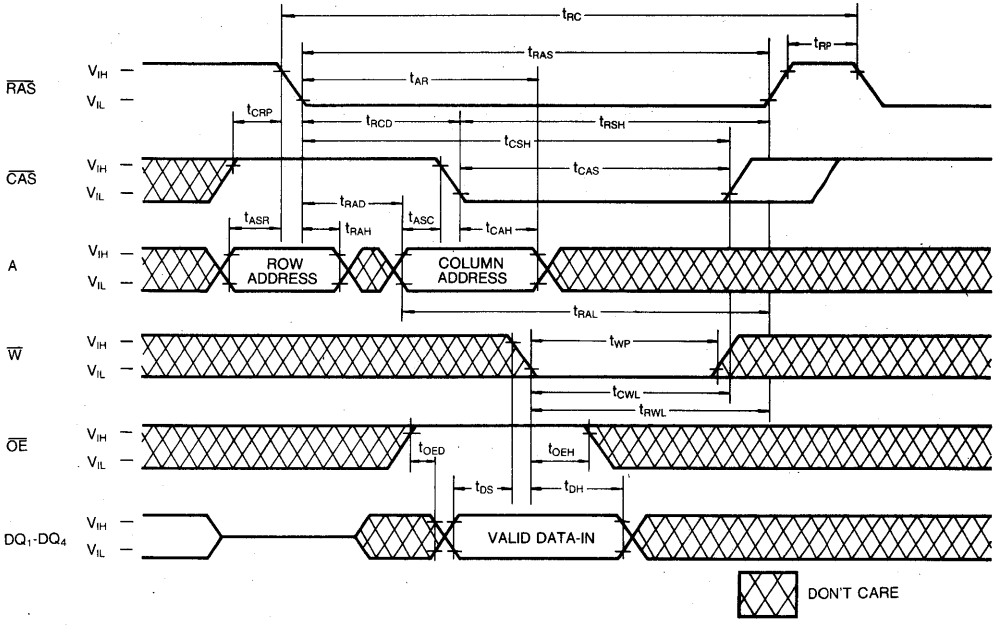
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



WRITE CYCLE (OE CONTROLLED WRITE)



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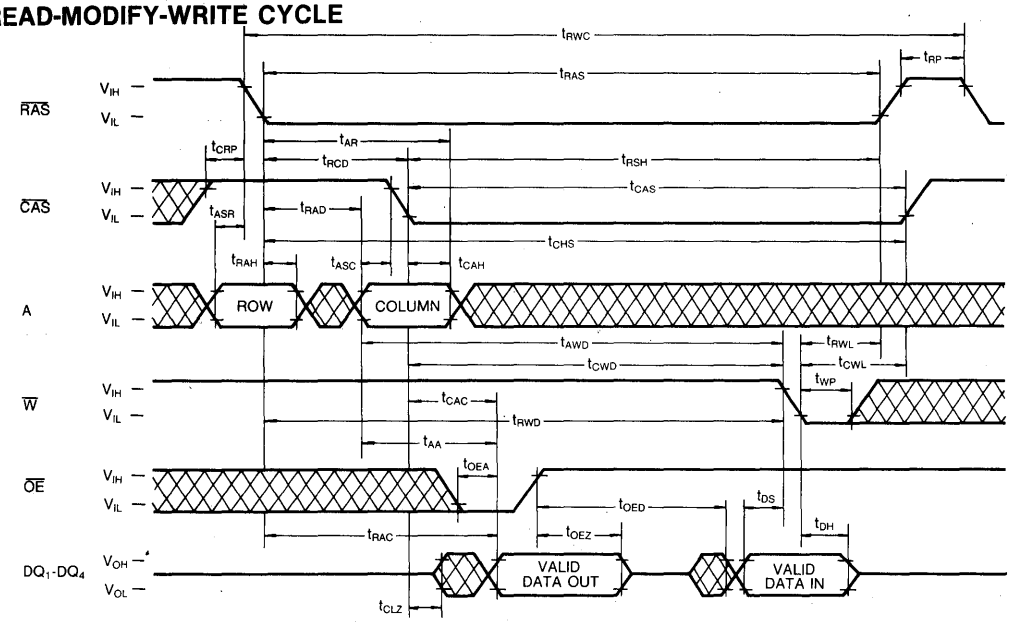
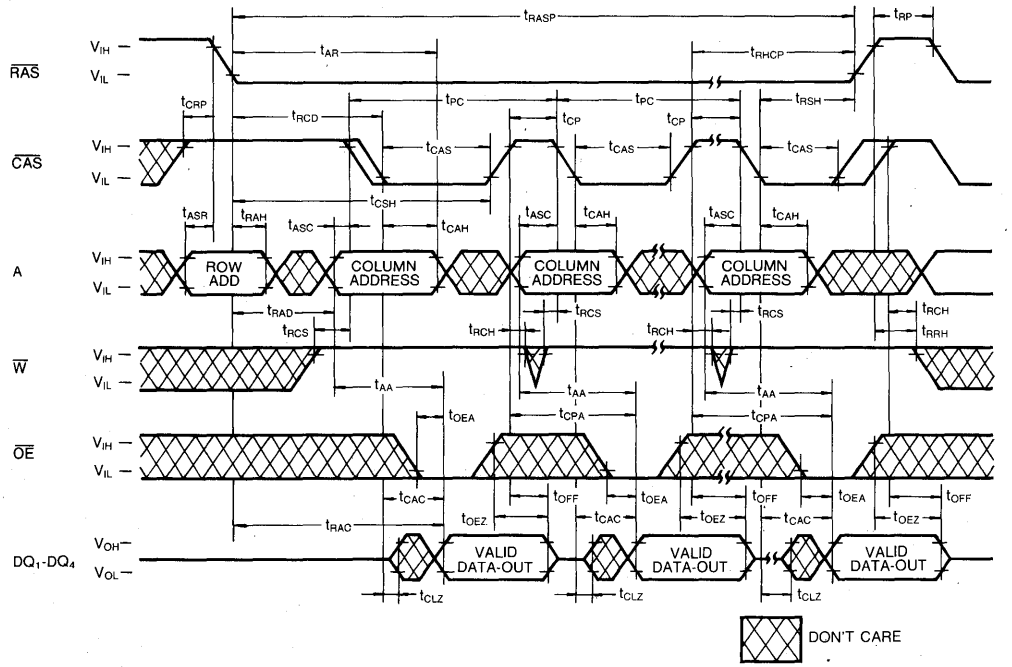
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



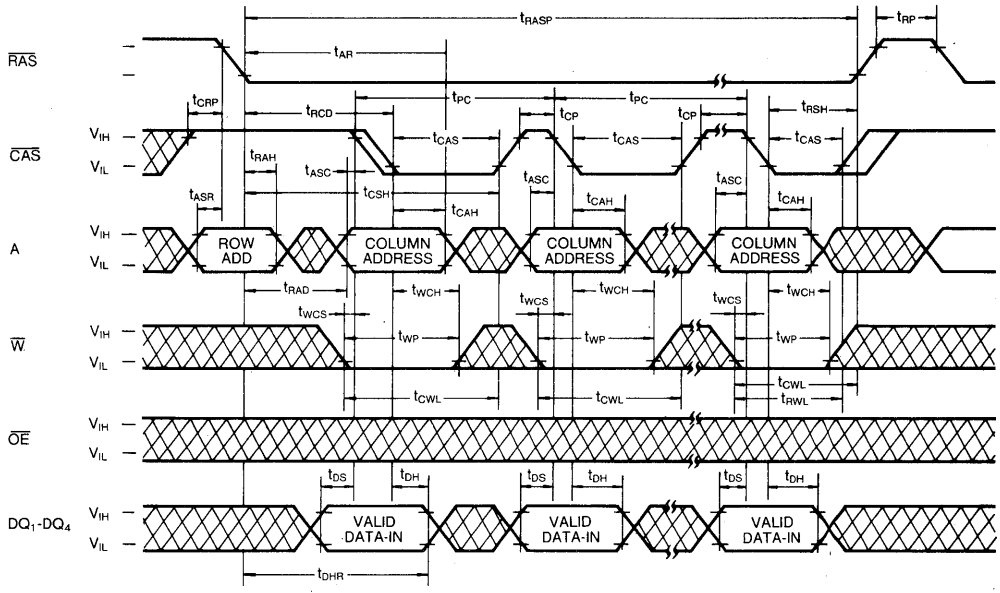
FAST PAGE MODE READ CYCLE



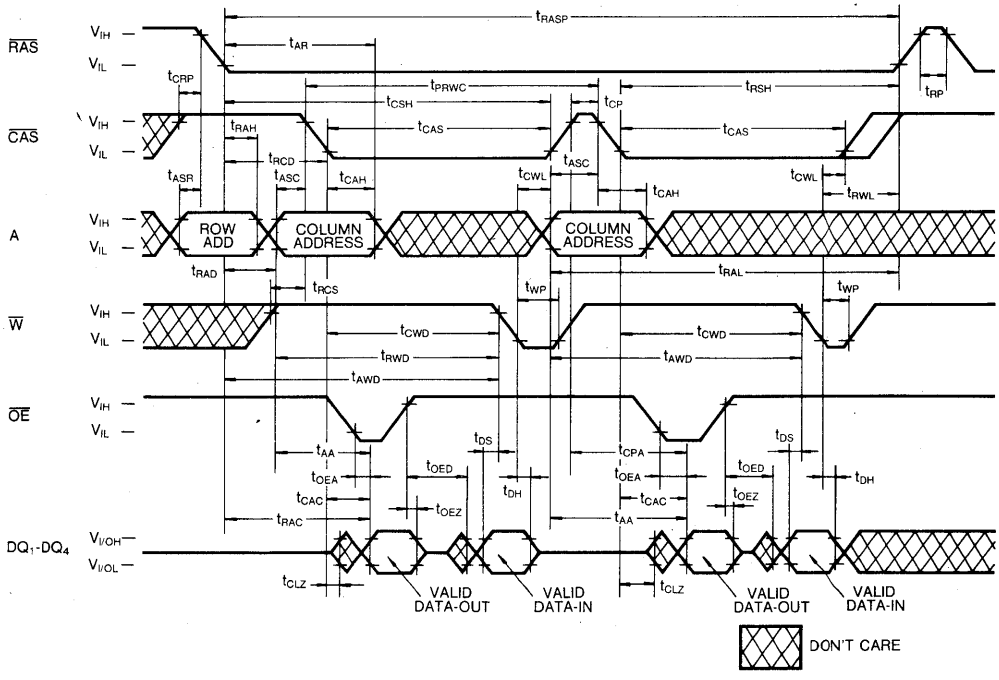
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



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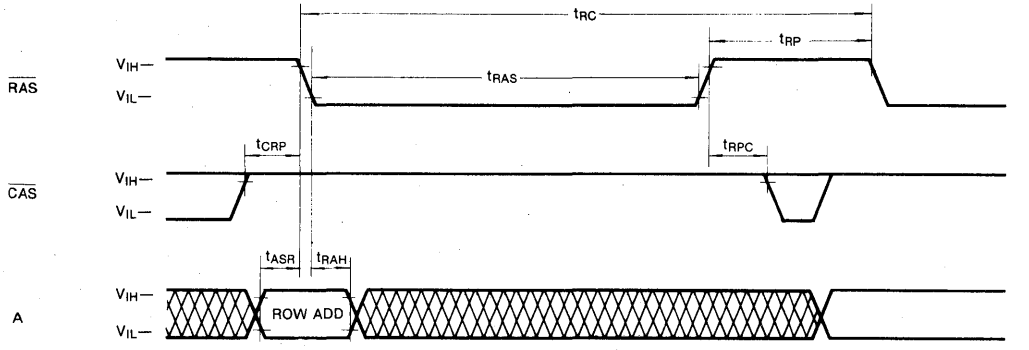
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

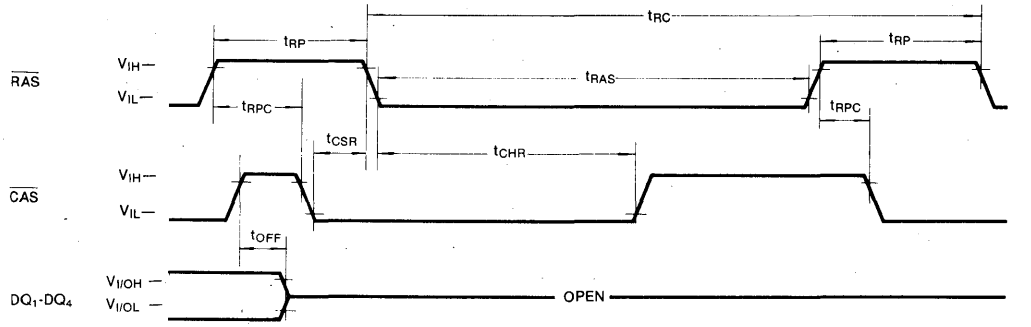
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



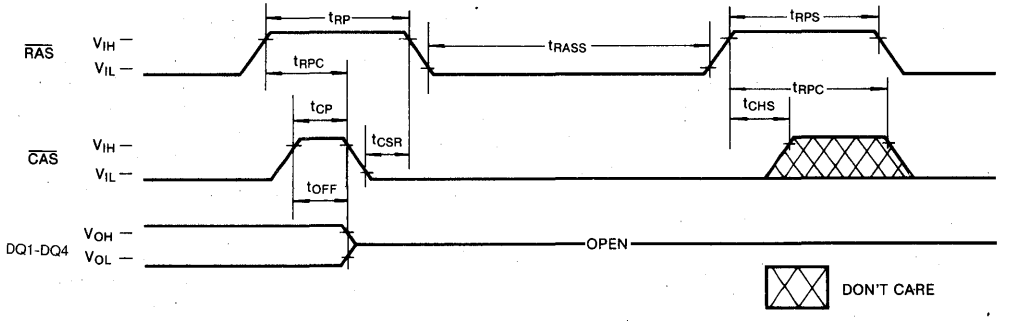
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



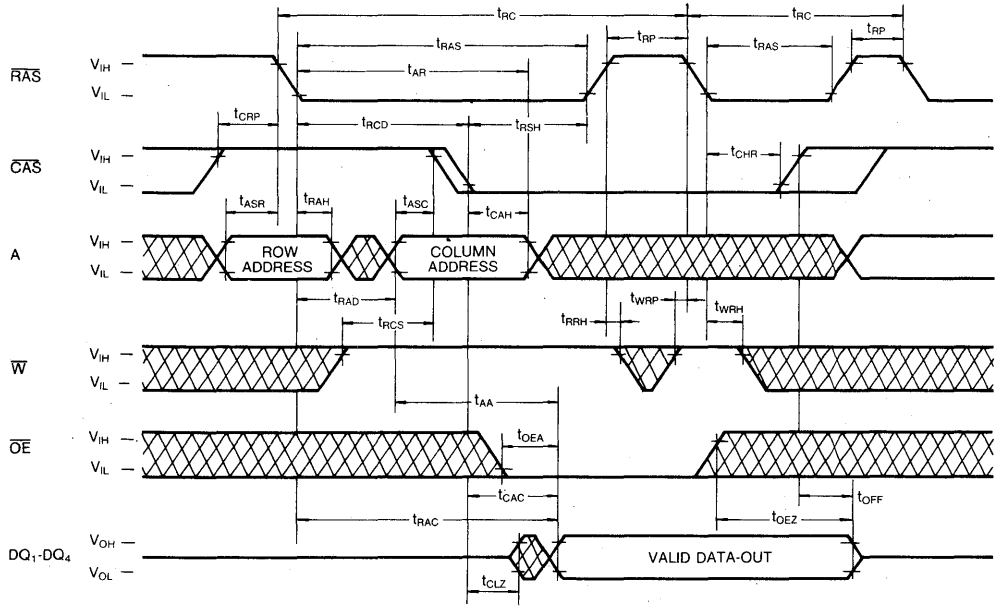
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

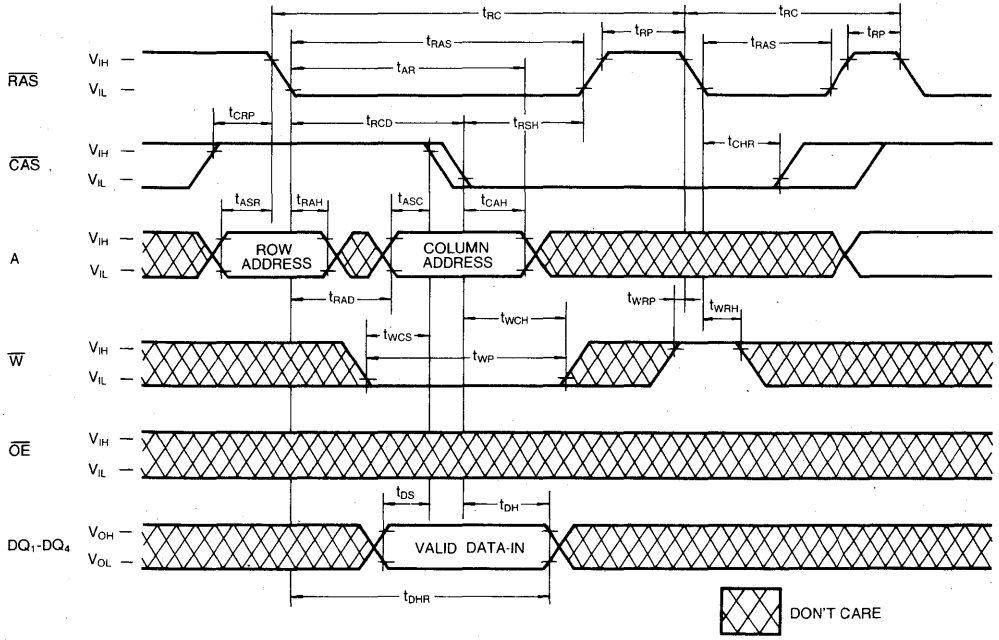


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



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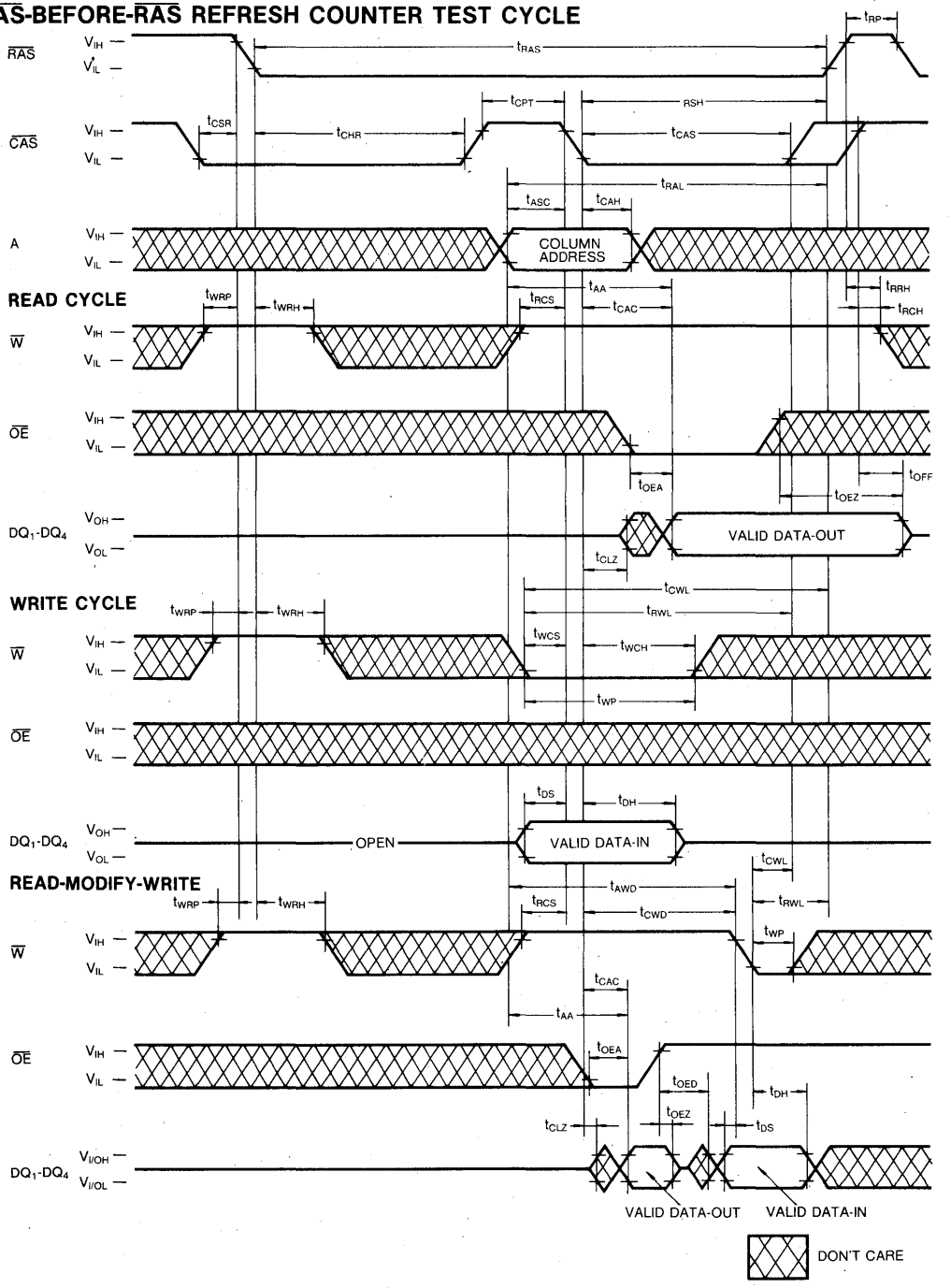
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

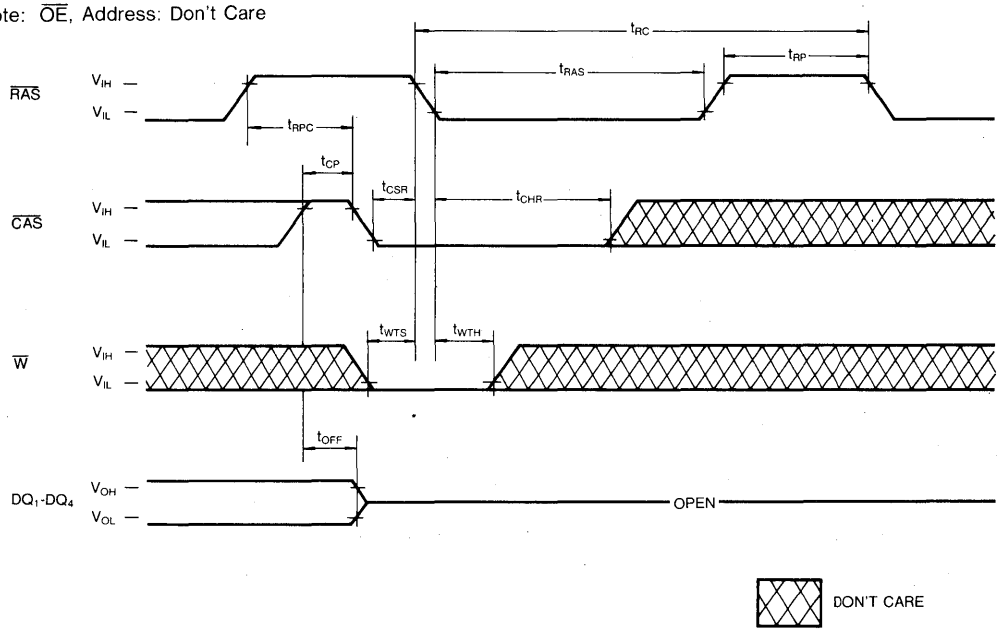


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



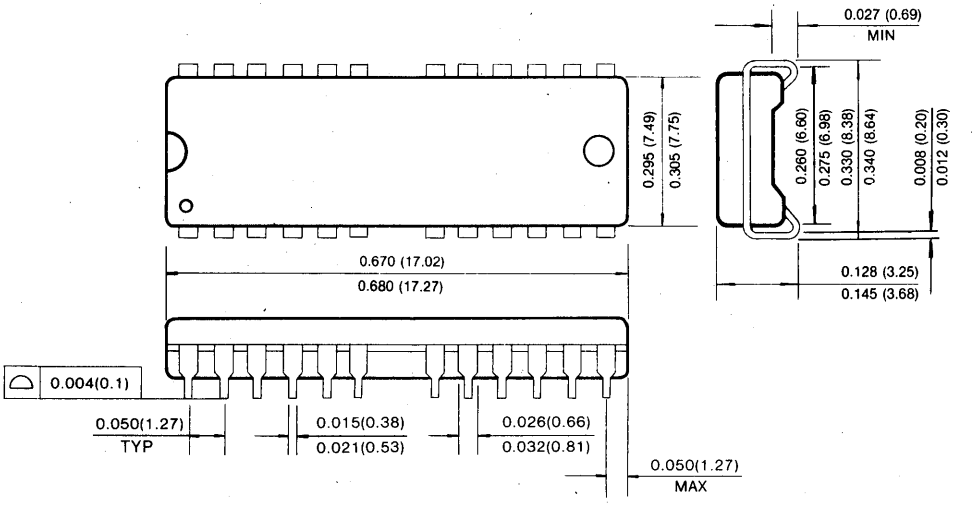
TEST MODE DESCRIPTION

The KM44V4100A/AL/ALL/ASL is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1, 048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 and A_1 are not used. If, upon reading, four bits on one D/Q pin are equal (all "1"s or "0"s) the D/Q pin indicates a "1". If they were not equal, the D/Q pin would indicate a "0". In "Test Mode", the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

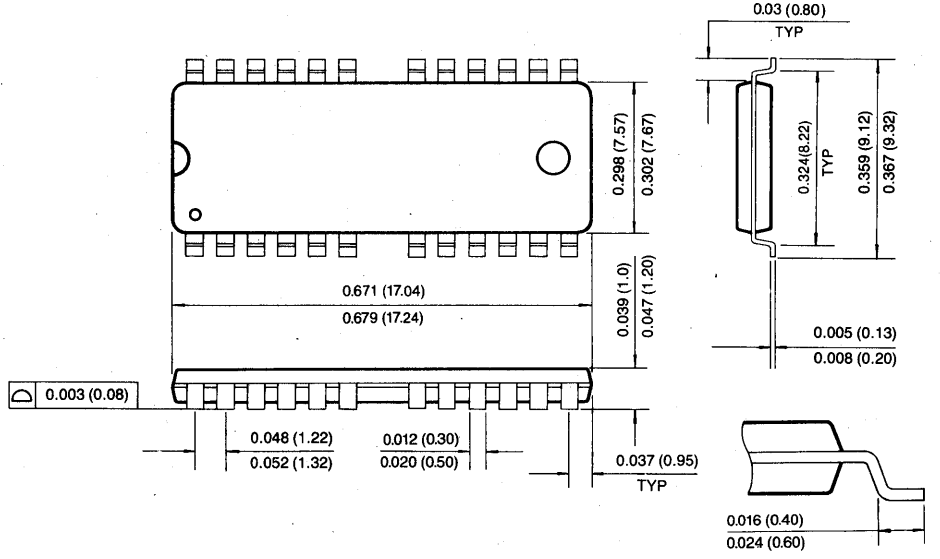
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

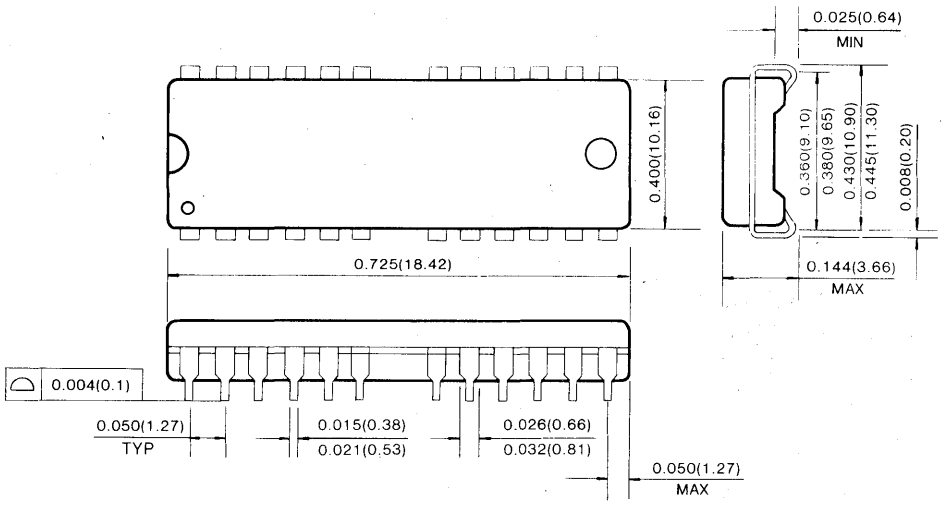


SAMSUNG ELECTRONICS

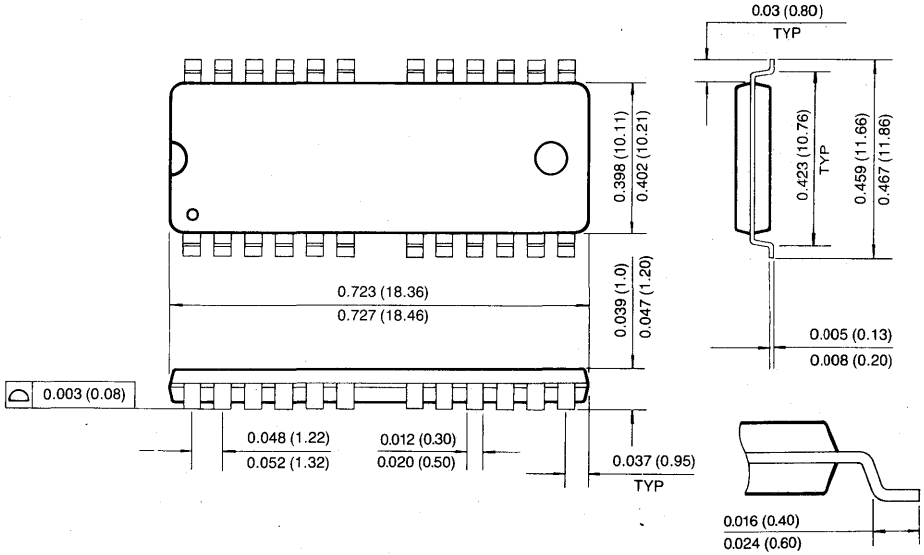
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



5

4M ×4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
KM44V4004A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM44V4004A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM44V4004A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- **Fast Page Mode with Extended data out**
- **Self Refresh Operation (LL-ver. only)**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **LVTTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+3.3V±0.3V power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

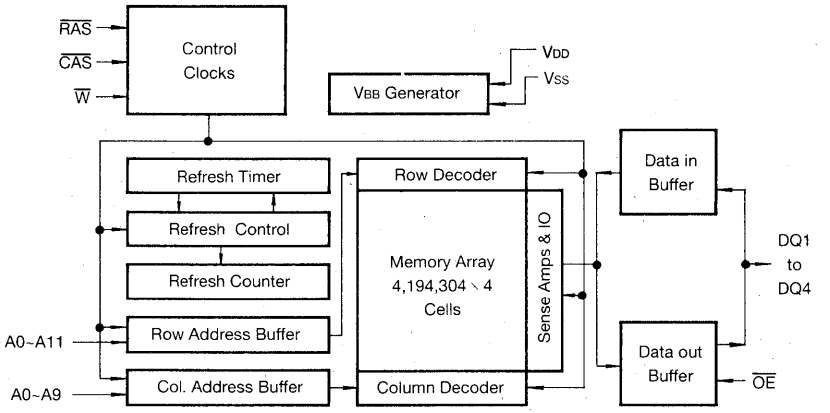
The Samsung KM44V4004A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44V4004A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

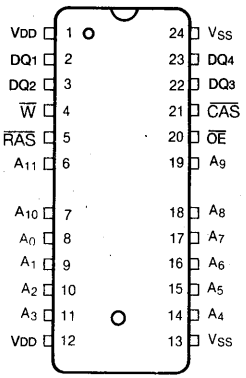
The KM44V4004A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



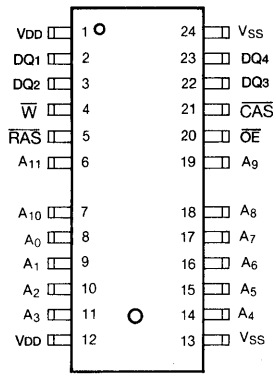
PIN CONFIGURATION (Top Views)

• **KM44V4004 AJ/ALJ/ALLJ/ASLJ**
AK/ALK/ALLK/ASLK



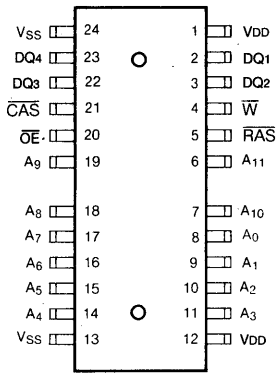
J : 400MIL
K : 300MIL

• **KM44V4004 AT/ALT/ALLT/ASLT**
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S: 300MIL(Forward)

• **KM44V4004 ATR/ALTR/ALLTR/ASLTR**
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A_0-A_{11}	Address Inputs
DQ_1~DQ_4	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{DD}	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5~ 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5~ 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44V4004A/AL/ALL/ASL-6	I_{CC1}	-	80	mA
	KM44V4004A/AL/ALL/ASL-7			70	mA
	KM44V4004A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44V4004A	I_{CC2}	-	2	mA
	KM44V4004AL			1	mA
	KM44V4004ALL			1	mA
	KM44V4004ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44V4004A/AL/ALL/ASL-6	I_{CC3}	-	80	mA
	KM44V4004A/AL/ALL/ASL-7			70	mA
	KM44V4004A/AL/ALL/ASL-8			60	mA
Hyper Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44V4004A/AL/ALL/ASL-6	I_{CC4}	-	90	mA
	KM44V4004A/AL/ALL/ASL-7			80	mA
	KM44V4004A/AL/ALL/ASL-8			70	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM44V4004A	I_{CC5}	-	1	mA
	KM44V4004AL			300	μA
	KM44V4004ALL			200	μA
	KM44V4004ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44V4004A/AL/ALL/ASL-6	I_{CC6}	-	80	mA
	KM44V4004A/AL/ALL/ASL-7			70	mA
	KM44V4004A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ1~DQ4=Don't Care t_{RC}=31.25μs(L-Ver.) 62.5μs(SL-Ver.), t_{RAS}=t_{RAS} min.~300ns	KM44V4004AL	I_{CC7}	-	450	μA
	KM44V4004ASL			350	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{DD}-0.2V or 0.2V DQ1~DQ4=V_{DD}-0.2V, 0.2V or Open	KM44V4004ALL	I_{CC8}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	I_{OL}	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz))

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Test condition: V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		3		ns	3
Output buffer turn-off delayfrom $\overline{CAS}$	t_{CEZ}	3	15	3	20	3	20	ns	7,14,16
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	45		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	15	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10		15		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	60		70		75		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Hyper Page cycle time	t_{HPC}	24		29		34		ns	17
Hyper Page read-modify-write cycle time	t_{HPRWC}	71		86		96		ns	17
$\overline{CAS}$ precharge time (Hyper Page cycle)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	7,14
$\overline{OE}$ commend hold time	tOEH	15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	7,16
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width(Hyper Page cycle)	tWPE	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	20	3	20	ns	7,14,16
Output buffer turn off delay from $\overline{W}$	tWEZ	3	15	3	20	3	20	ns	7,14
$\overline{W}$ to data delay	tWED	15		20		20		ns	
$\overline{RAS}$ pulse width (LL-Ver)	tRASS	100		100		100		μs	15
$\overline{RAS}$ precharge time (LL-Ver)	tRPS	110		130		150		ns	15
$\overline{CAS}$ hold time (LL-Ver)	tCHS	-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		20		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	15	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	20		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Hyper Page mode cycle time	tHPC	29		34		39		ns	
Hyper Page mode read-modify-write cycle time	tHPRWC	76		91		101		ns	
$\overline{RAS}$ pulse width (Hyper Page Mode)	tRASP	65	200,000	75	200,000	85	200,000	ns	

TEST MODE CYCLE(Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	
$\overline{OE}$ access time	t_{OEA}		20		25		25	ns	3
$\overline{OE}$ to data delay	t_{OED}	20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	20		25		25		ns	

TEST MODE DESCRIPTION

The KM44V4004A/AL/ALL/ASL is the CMOS DRAM organized 4,194,304 words by 4 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 4Mx4 DRAM can be tested as if it were a 1Mx4 DRAM.

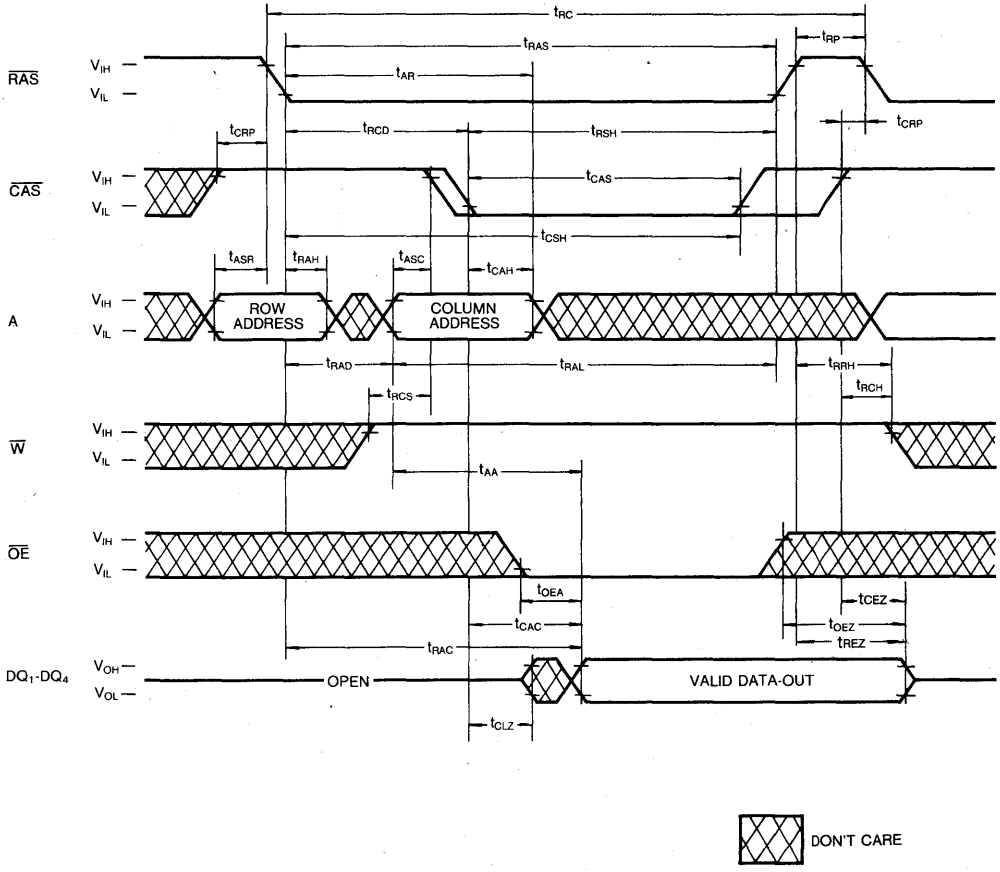
$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", And "$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" or $\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{W}$ and $\overline{RAS}$ Refresh Cycle" peforms the refresh operation with internal CBR refresh address counter. The "Test Mode" funcition reduces test time (1/4 in cases of N test pattern)

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs, without t_{HPC} and t_{HPRWC}.
3. Measured with a load equivalent to 100pF and V_{oh}=2.0V(I_{OUT}=2mA), V_{ol}=0.8V(I_{OUT}=2mA)
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{RWZ}(max), t_{CEZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going
17. $t_{ASC} \geq t_{CP}$(min), Assumn t_T=2.0ns

TIMING DIAGRAMS

READ CYCLE



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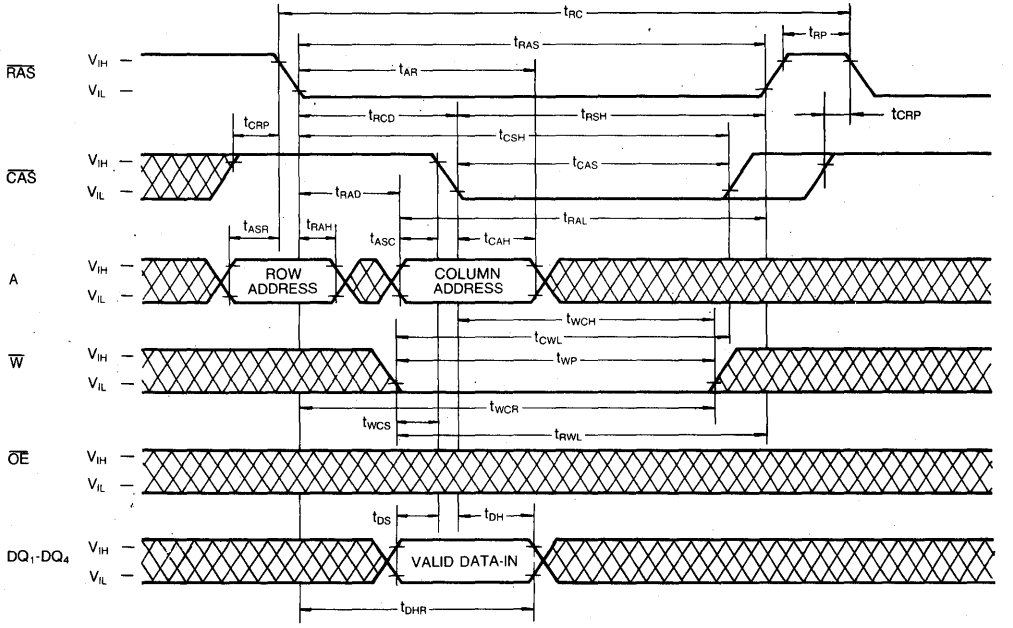
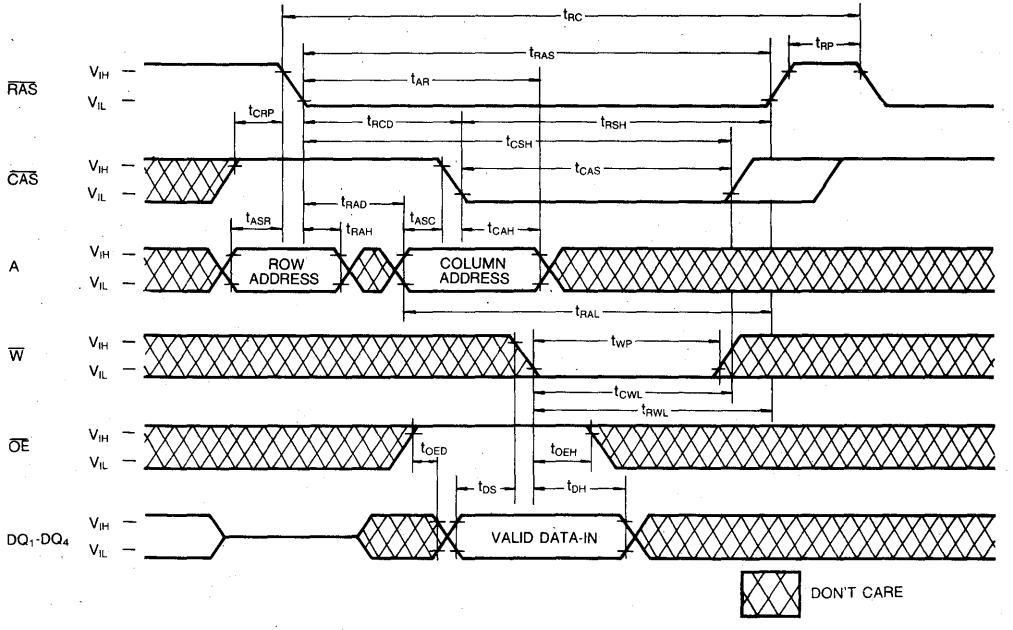
TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



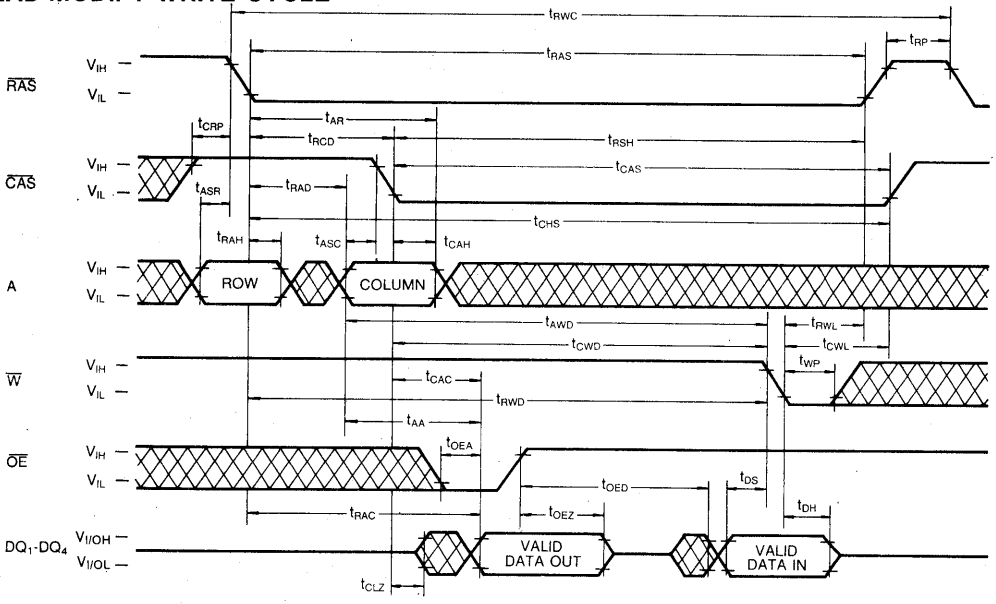
WRITE CYCLE (OE CONTROLLED WRITE)



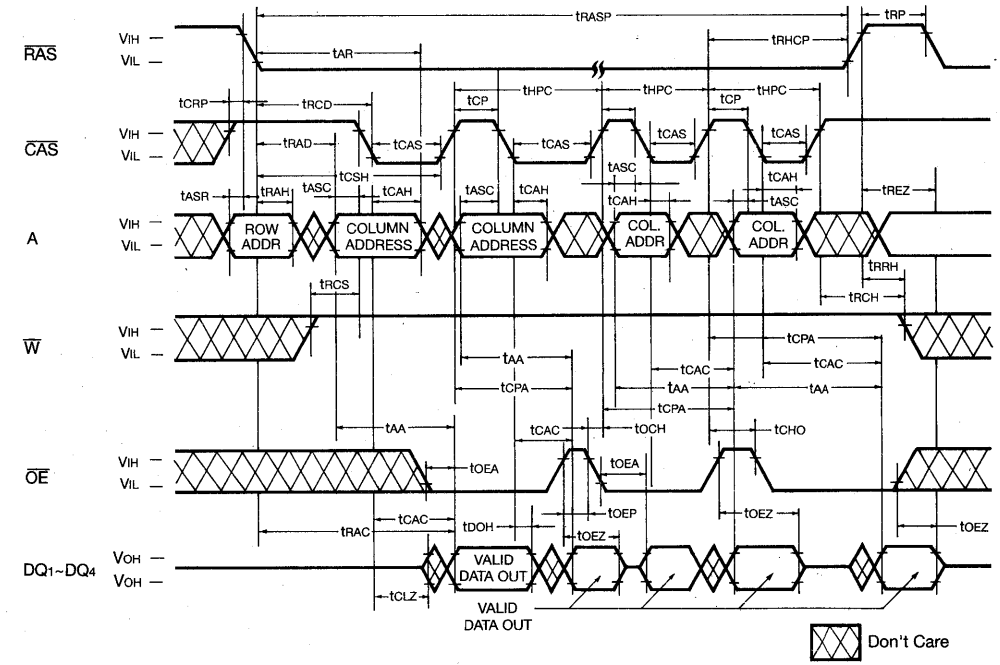
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



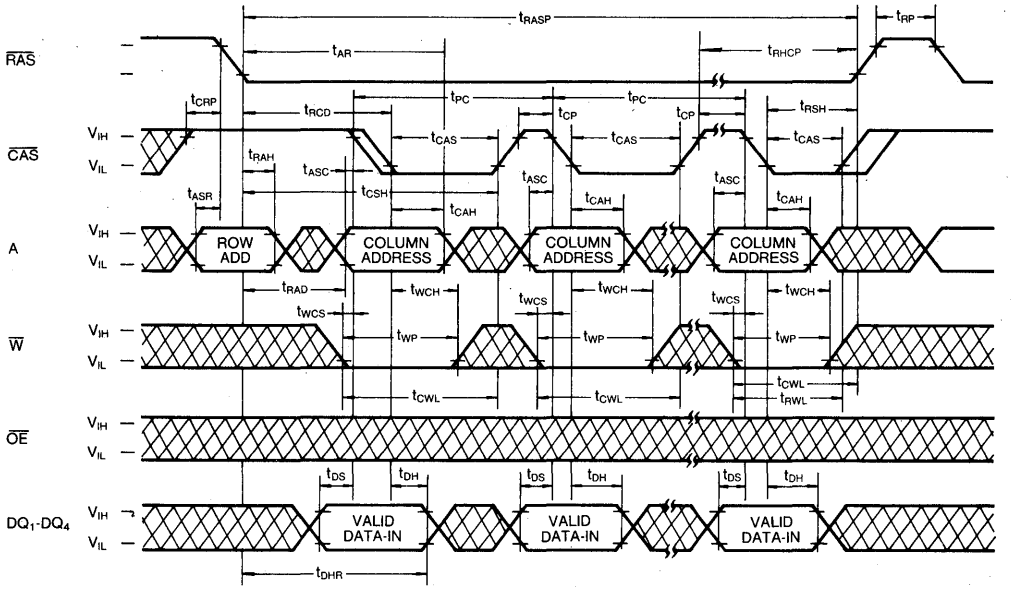
HYPER PAGE READ CYCLE



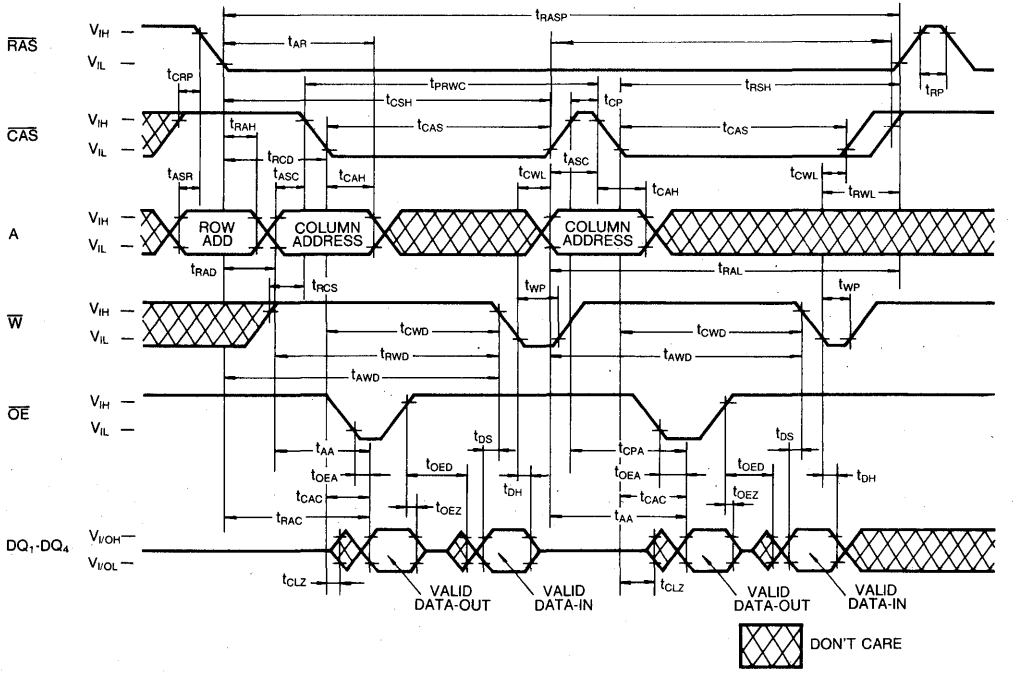
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

HYPER PAGE WRITE CYCLE (EARLY WRITE)

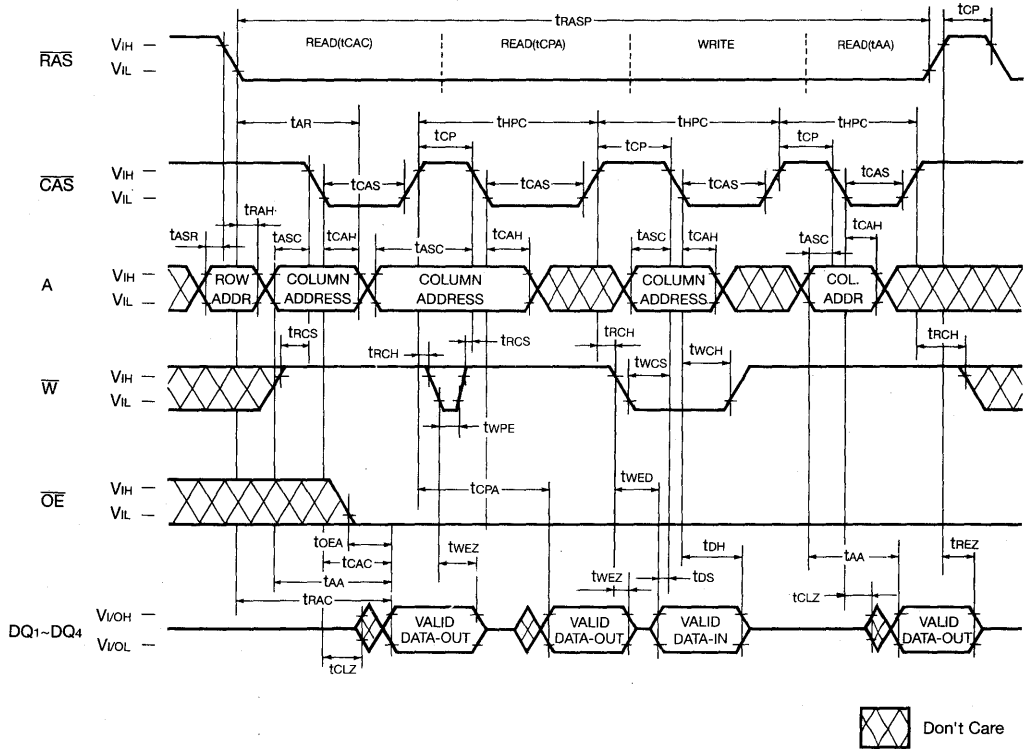


HYPER PAGE READ-MODIFY-WRITE CYCLE



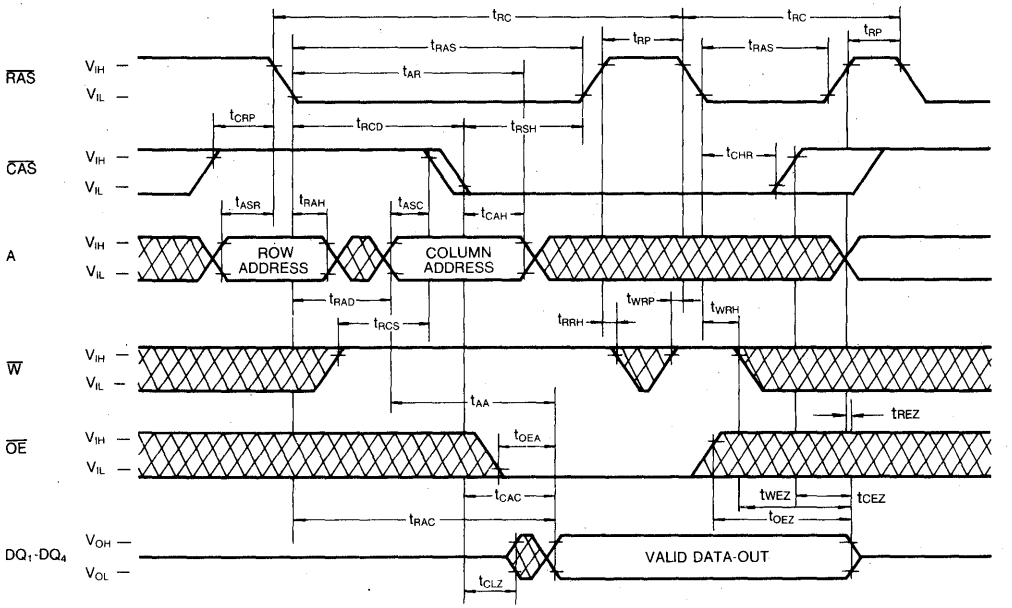
SAMSUNG ELECTRONICS

HYPER PAGE READ AND WRITE MIXED CYCLE

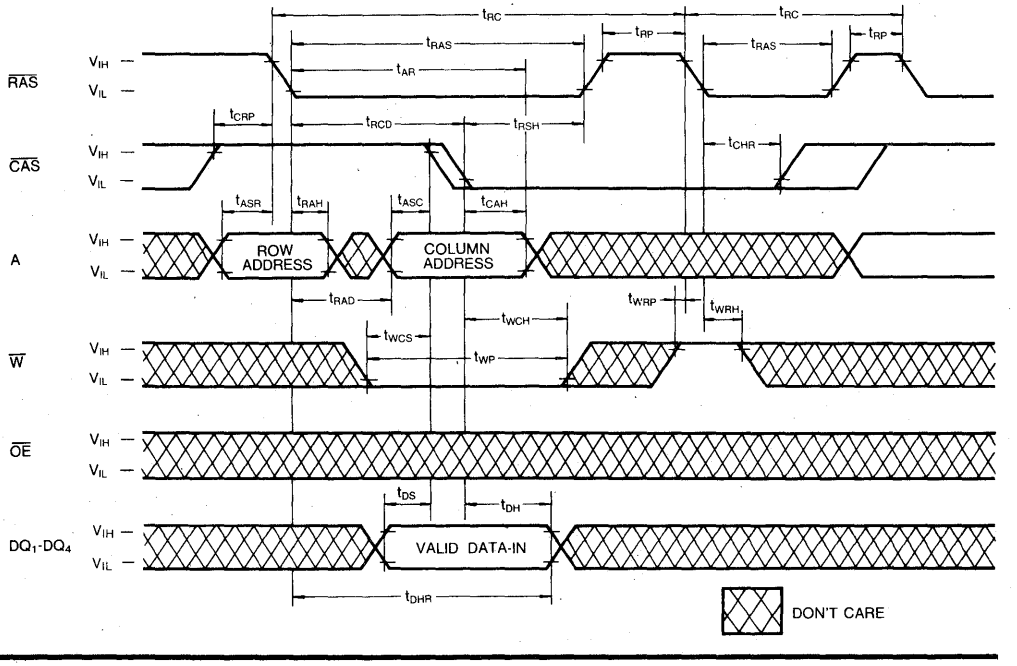


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



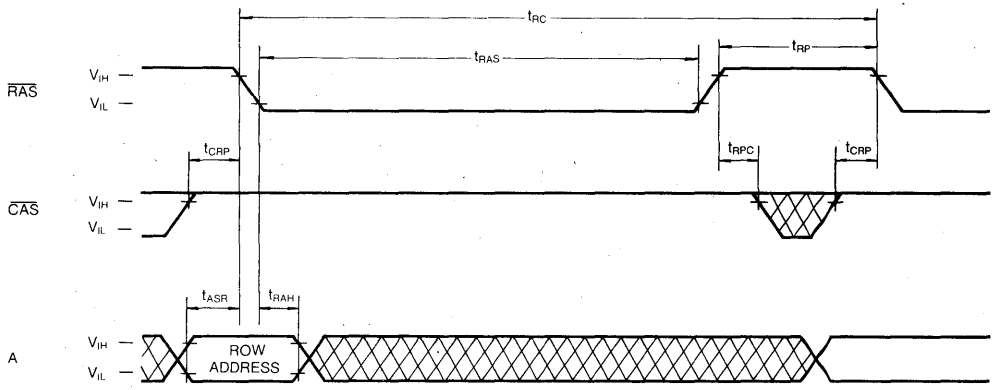
HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

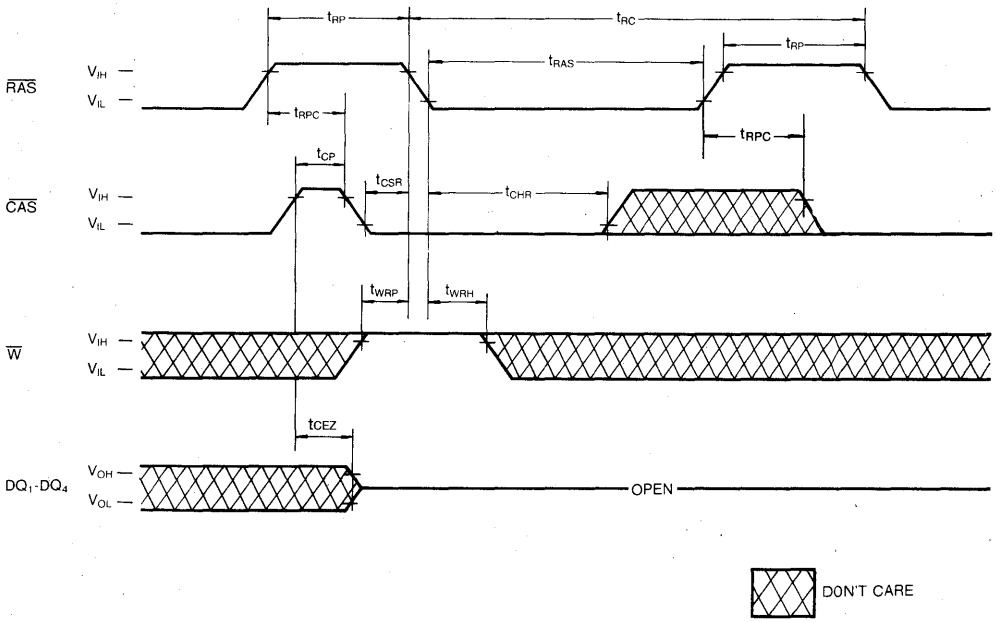
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



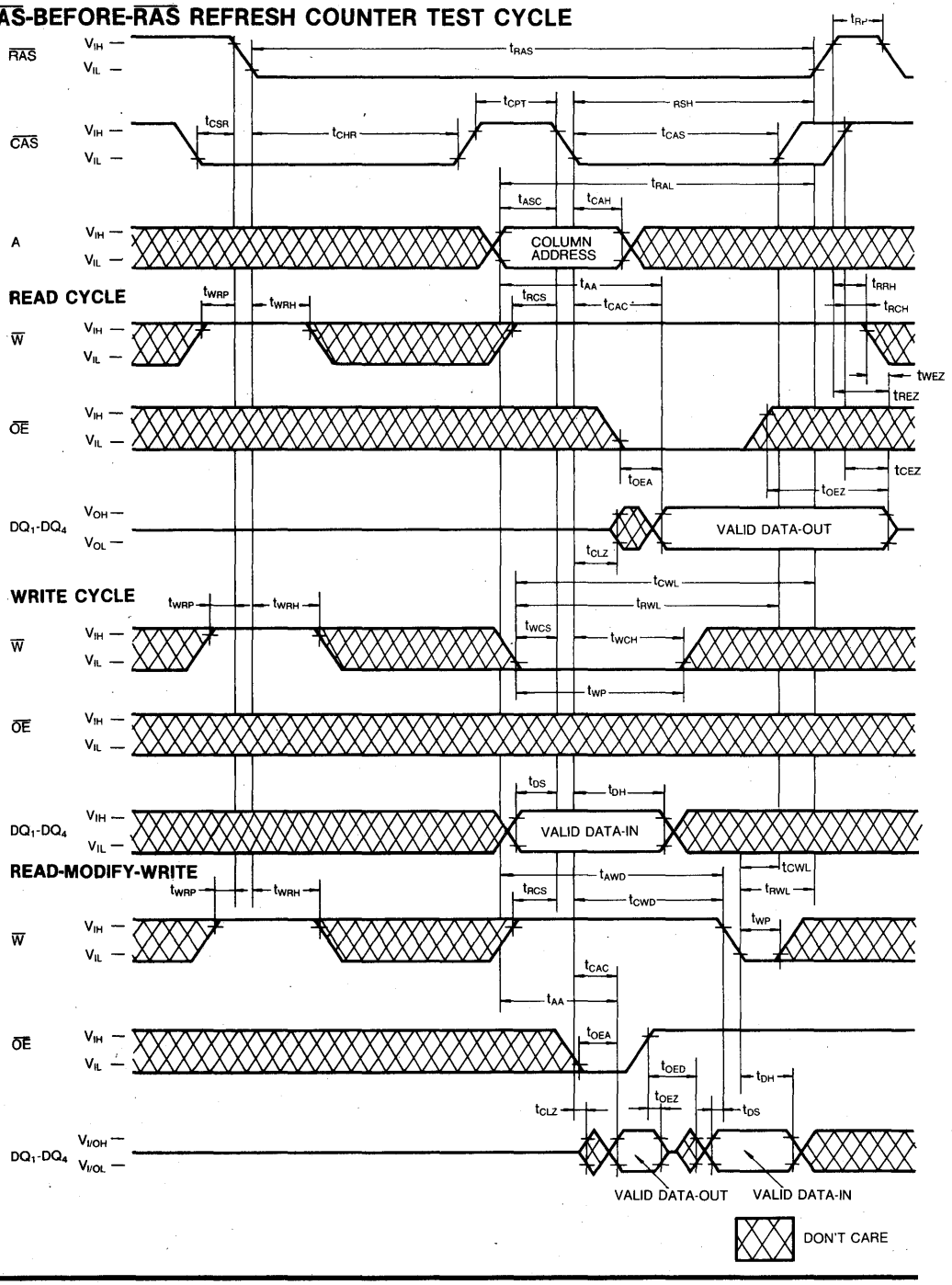
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{OE}$, Address=Don't Care



TIMING DIAGRAMS (Continued)

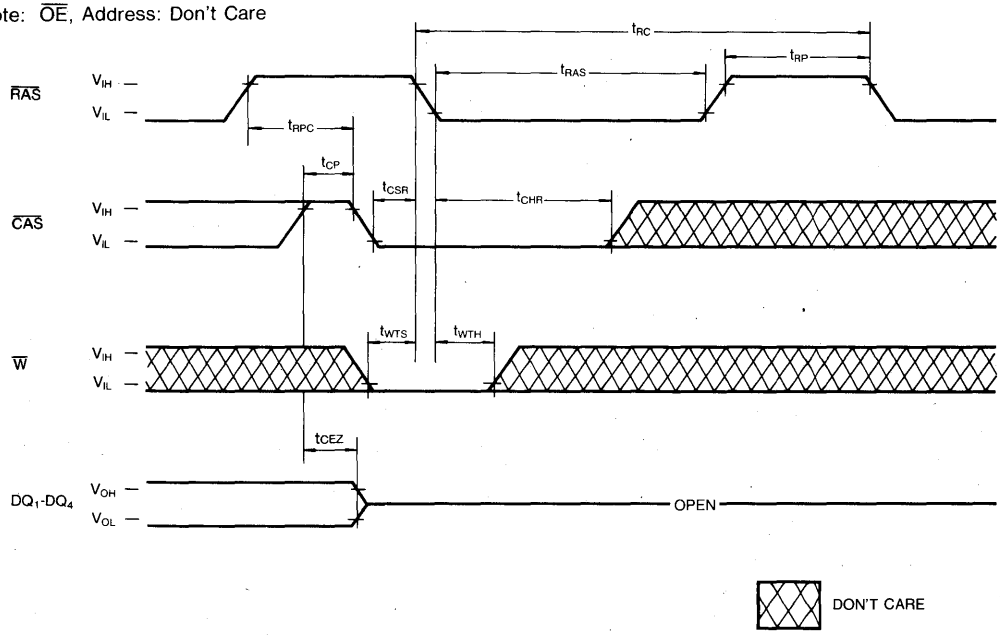
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



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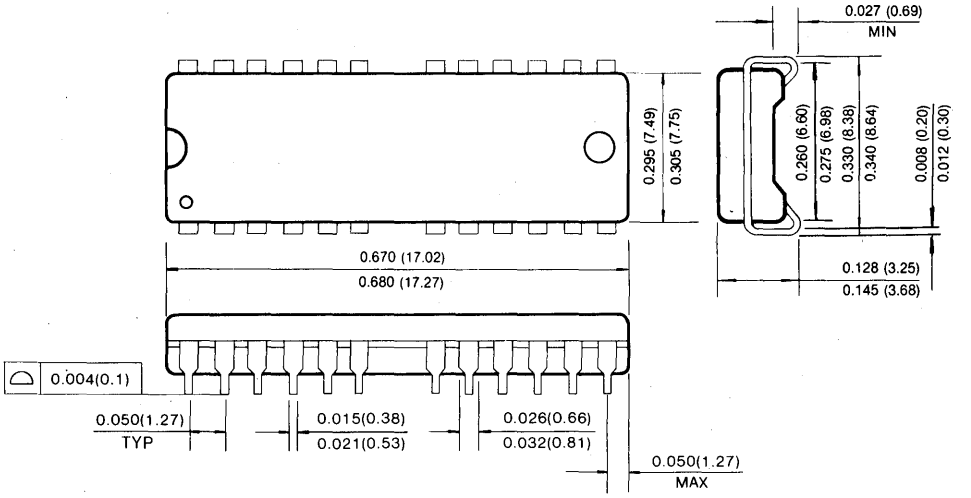
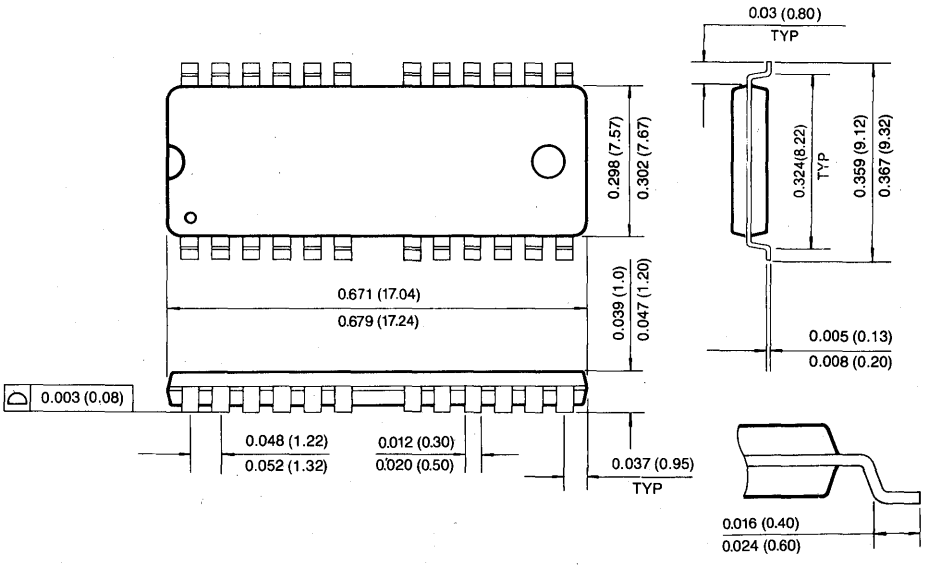
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

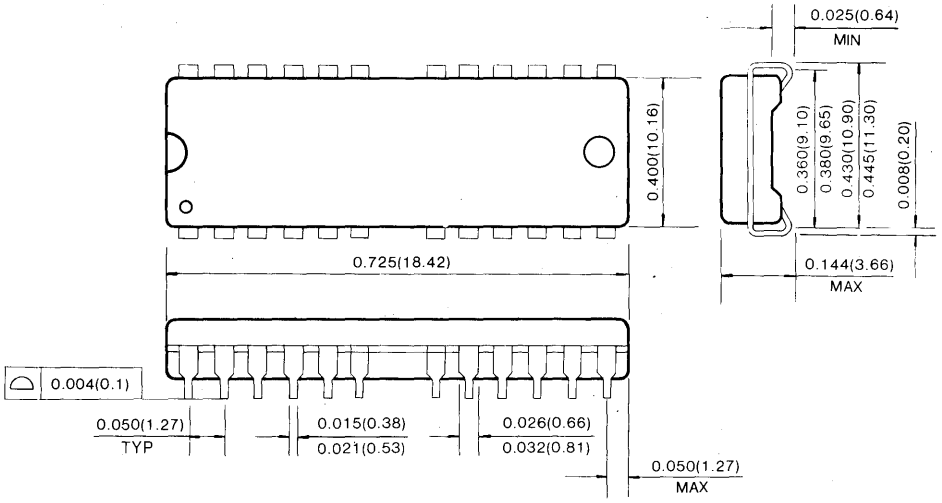


SAMSUNG ELECTRONICS

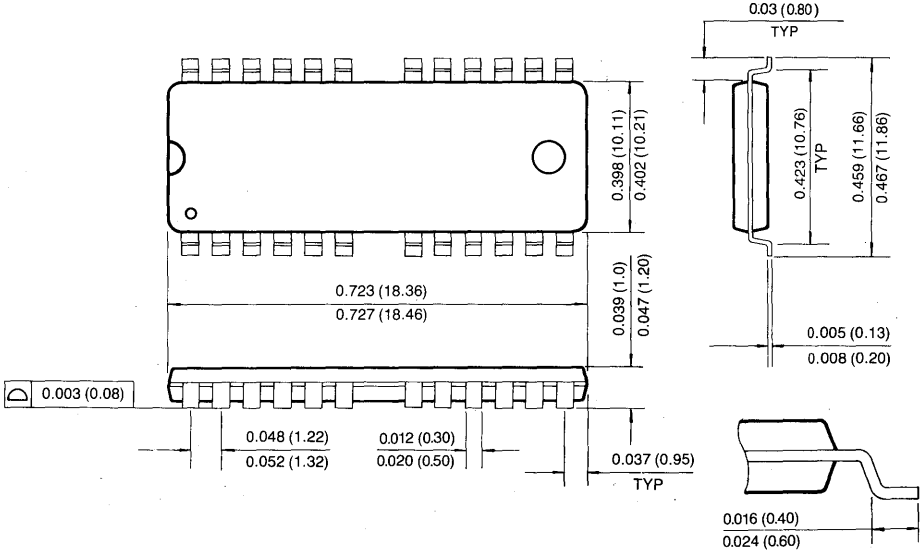
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



5

4M ×4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM44V4104A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM44V4104A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM44V4104A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- **Fast Page Mode with Extended data out**
- **Self Refresh Operation (LL-ver. only)**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **LVTTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+3.3V±0.3V power supply**
- **2048 cycles/32ms refresh (Normal)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

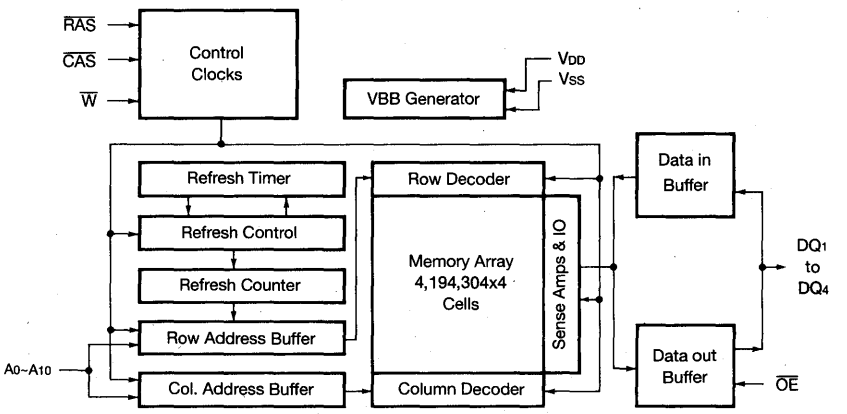
The Samsung KM44V4104A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44V4104A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44V4104A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

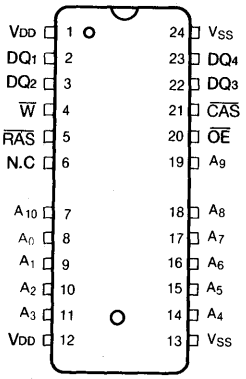
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

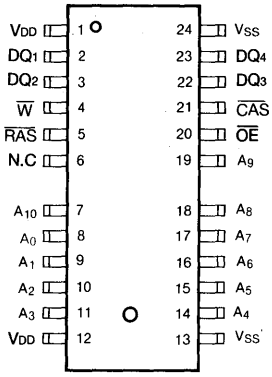
PIN CONFIGURATION (Top Views)

• **KM44V4104 AJ/ALJ/ALLJ/ASLJ**
AK/ALK/ALLK/ASLK



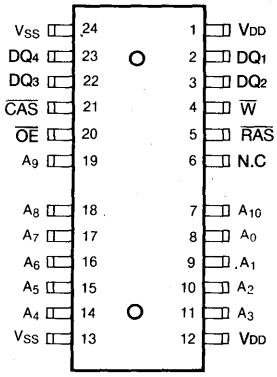
J : 400MIL
K : 300MIL

• **KM44V4104 AT/ALT/ALLT/ASLT**
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S: 300MIL(Forward)

• **KM44V4104 ATR/ALTR/ALLTR/ASLTR**
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A10	Address Inputs
DQ1-4	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VDD	Power(+3.3V)
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5~ 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5~ 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44V4104A/AL/ALL/ASL-6	I_{CC1}	-	100	mA
	KM44V4104A/AL/ALL/ASL-7			90	mA
	KM44V4104A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44V4104A	I_{CC2}	-	2	mA
	KM44V4104AL			1	mA
	KM44V4104ALL			1	mA
	KM44V4104ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44V4104A/AL/ALL/ASL-6	I_{CC3}	-	100	mA
	KM44V4104A/AL/ALL/ASL-7			90	mA
	KM44V4104A/AL/ALL/ASL-8			80	mA
Hyper Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44V4104A/AL/ALL/ASL-6	I_{CC4}	-	100	mA
	KM44V4104A/AL/ALL/ASL-7			90	mA
	KM44V4104A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM44V4104A	I_{CC5}	-	1	mA
	KM44V4104AL			300	μA
	KM44V4104ALL			200	μA
	KM44V4104ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44V4104A/AL/ALL/ASL-6	I_{CC6}	-	100	mA
	KM44V4104A/AL/ALL/ASL-7			90	mA
	KM44V4104A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V, DQ_1~DQ_4=Don't Care t_{RC}=62.5μs(L-Ver.) 125μs(SL-Ver.), t_{RAS}=t_{RAS} min.~300ns	KM44V4104AL	I_{CC7}	-	400	μA
	KM44V4104ASL			300	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=2.0V $\overline{W}$=$\overline{OE}$=A_0-A_{10}=V_{DD}-0.2V or 0.2V DQ_1~DQ_4=V_{DD}-0.2V, 0.2V or Open	KM44V4104ALL	I_{CCS}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	I_{OL}	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz))

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{10})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Test condition: V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{OFF}	3	15	3	50	3	20	ns	7,14,16
Transition time (rise and fall)	t_T	2	50	2	20	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	45		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	15	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10		15		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal)	t_{REF}		32		32		32	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	60		70		75		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Hyper Page cycle time	t_{HPC}	24		29		34		ns	17
Hyper Page read-modify-write cycle time	t_{HPRWC}	71		86		96		ns	17
$\overline{CAS}$ precharge time (Hyper Page cycle)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	7,14
$\overline{OE}$ commend hold time	tOEH	15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	7,16
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width(Hyper Page cycle)	tWPE	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	20	3	20	ns	7,14,16
Output buffer turn off delay from $\overline{W}$	tWEZ	3	15	3	20	3	20	ns	7,14
$\overline{W}$ to data delay	tWED	15		20		20		ns	
$\overline{RAS}$ pulse width (LL-Ver)	tRASS	100		100		100		μs	15
$\overline{RAS}$ precharge time (LL-Ver)	tRPS	110		130		150		ns	15
$\overline{CAS}$ hold time (LL-Ver)	tCHS	-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		20		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	15	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	20		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Hyper Page mode cycle time	tHPC	29		34		39		ns	
Hyper Page mode read-modify-write cycle time	tHPRWC	76		91		101		ns	
$\overline{RAS}$ pulse width (Hyper Page Mode)	tRASP	65	200,000	75	200,000	85	200,000	ns	

TEST MODE CYCLE(Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	
$\overline{OE}$ access time	t_{OEA}		20		25		25	ns	3
$\overline{OE}$ to data delay	t_{OED}	20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	20		25		25		ns	

TEST MODE DESCRIPTION

The KM44V4104A/AL/ALL/ASL is the CMOS DRAM organized 4,194,304 words by 4 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 4Mx4 DRAM can be tested as if it were a 1Mx4 DRAM.

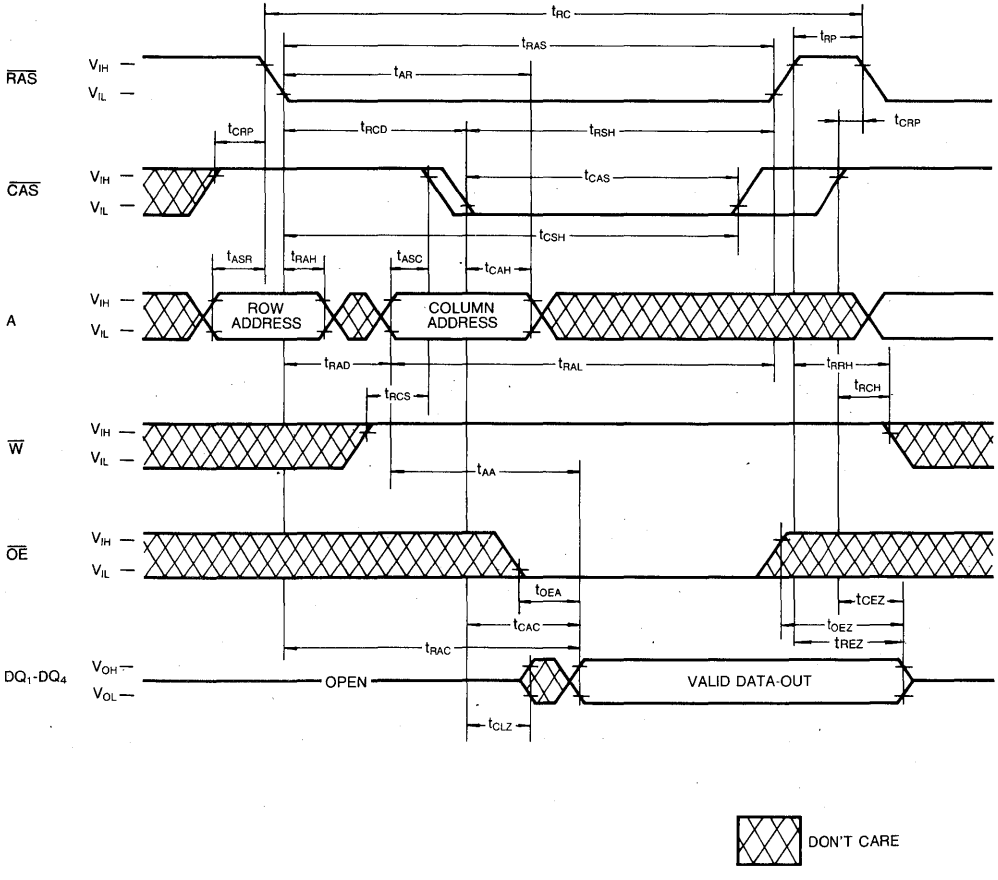
$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", And "$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" or $\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{W}$ and $\overline{RAS}$ Refresh Cycle" peforms the refresh operation with internal CBR refresh address counter. The "Test Mode" funcition reduces test time (1/4 in cases of N test pattern)

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs, without t_{HPC} and t_{HPRWC}.
3. Measured with a load equivalent to 100pF and V_{OH}=2.0V(I_{OUT}=2mA), V_{OL}=0.8V(I_{OUT}=2mA)
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{REZ}(max), t_{CEZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going
17. $t_{ASC} \geq t_{CP}$(min), Assumn t_T=2.0ns

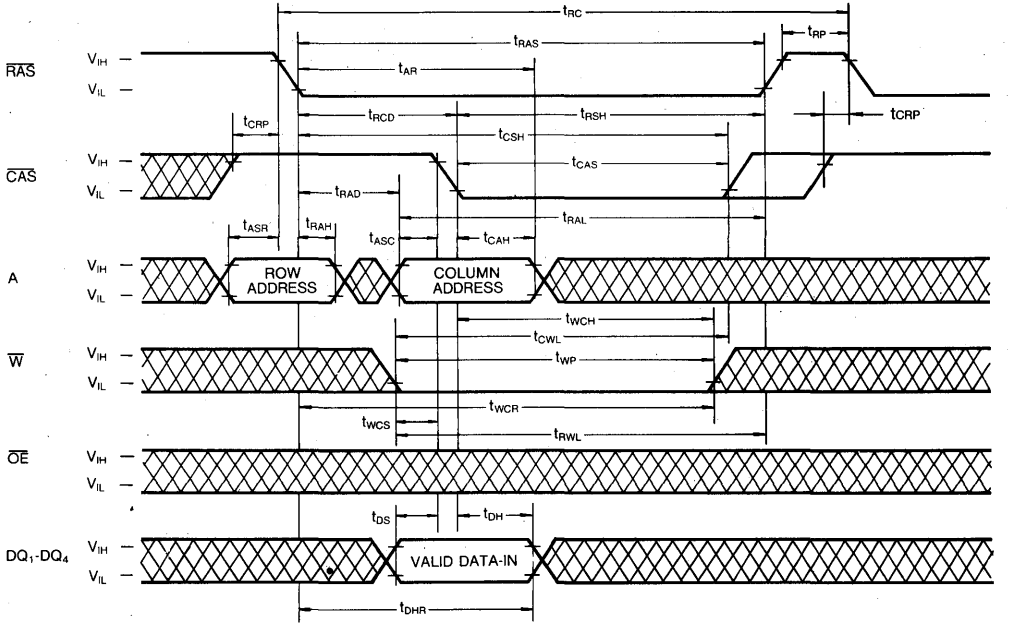
TIMING DIAGRAMS

READ CYCLE

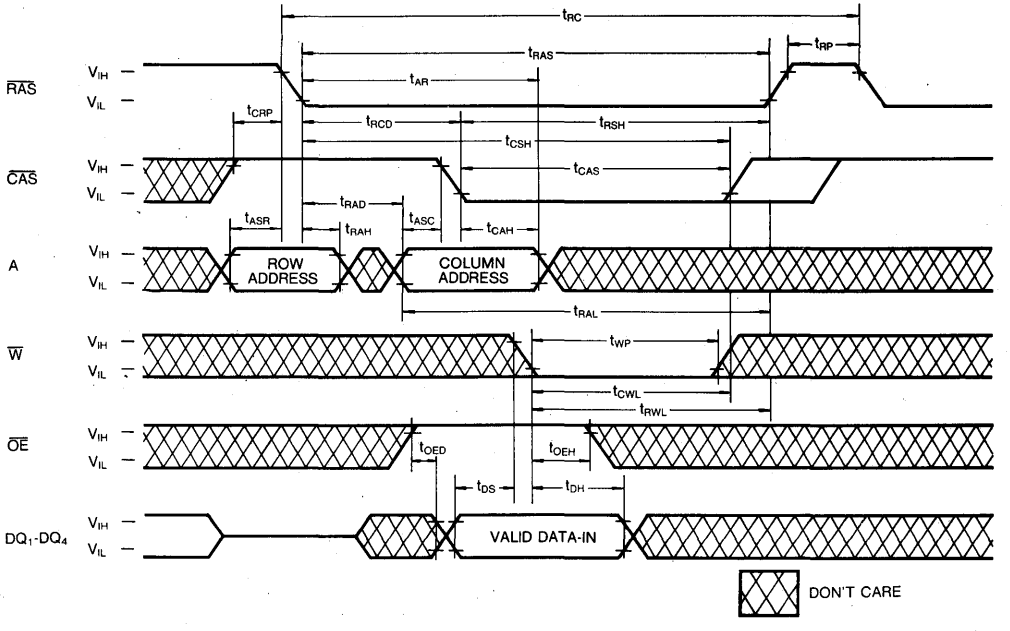


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)

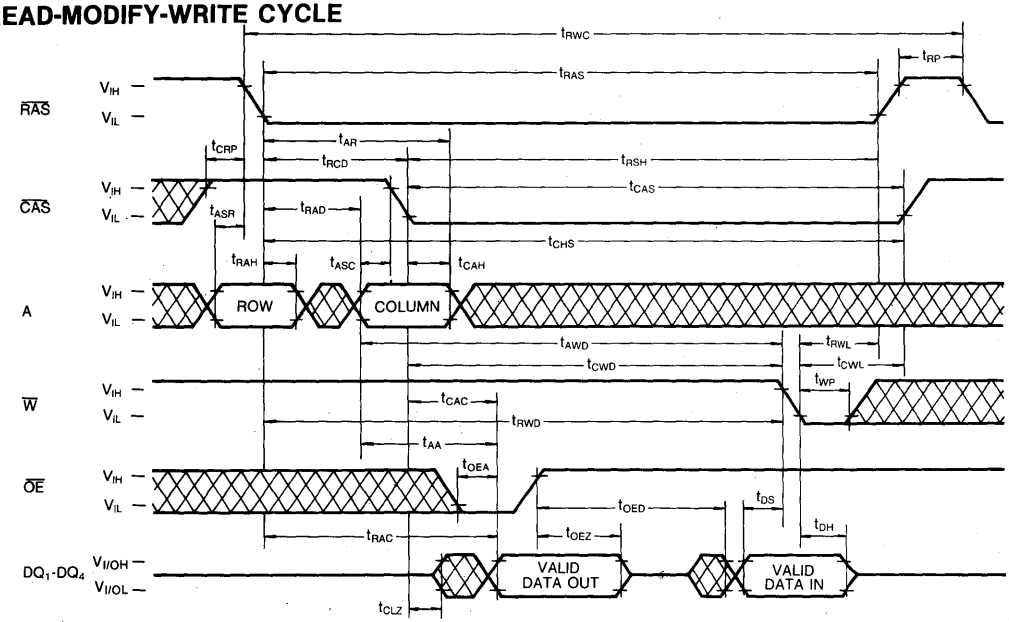


WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

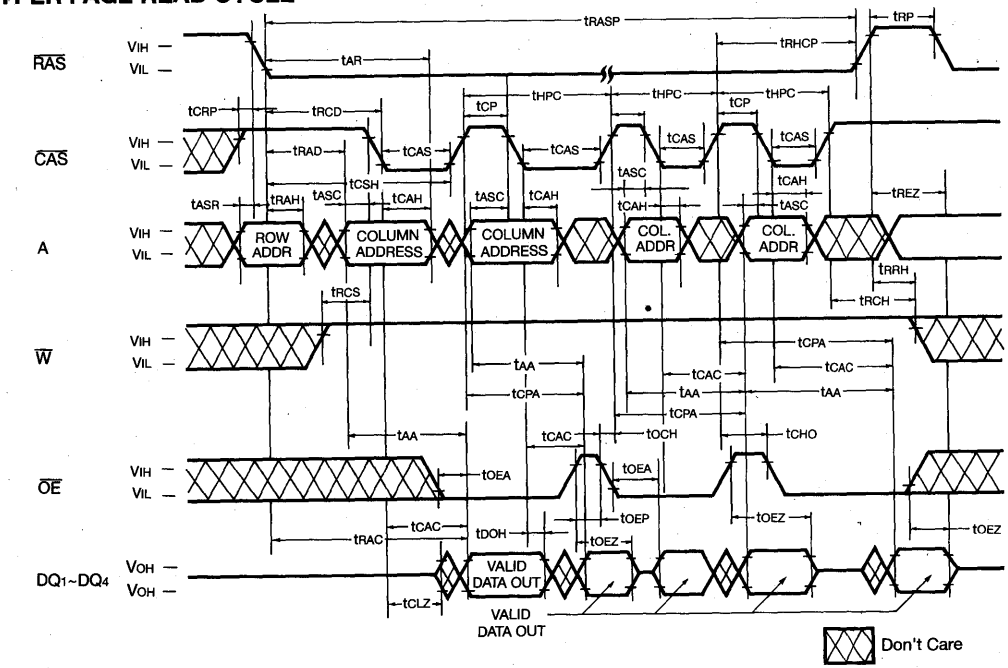


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



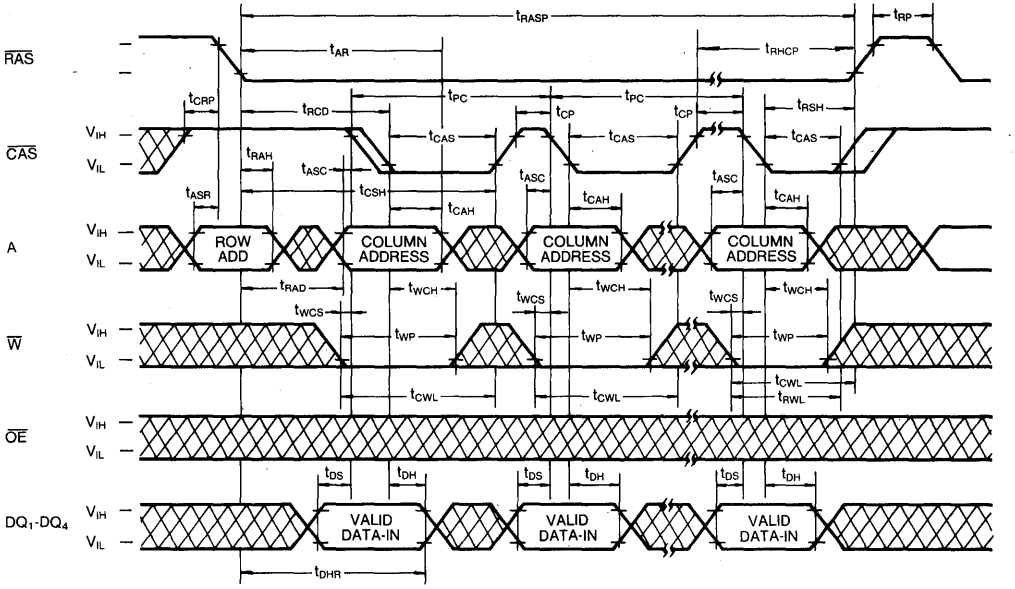
HYPER PAGE READ CYCLE



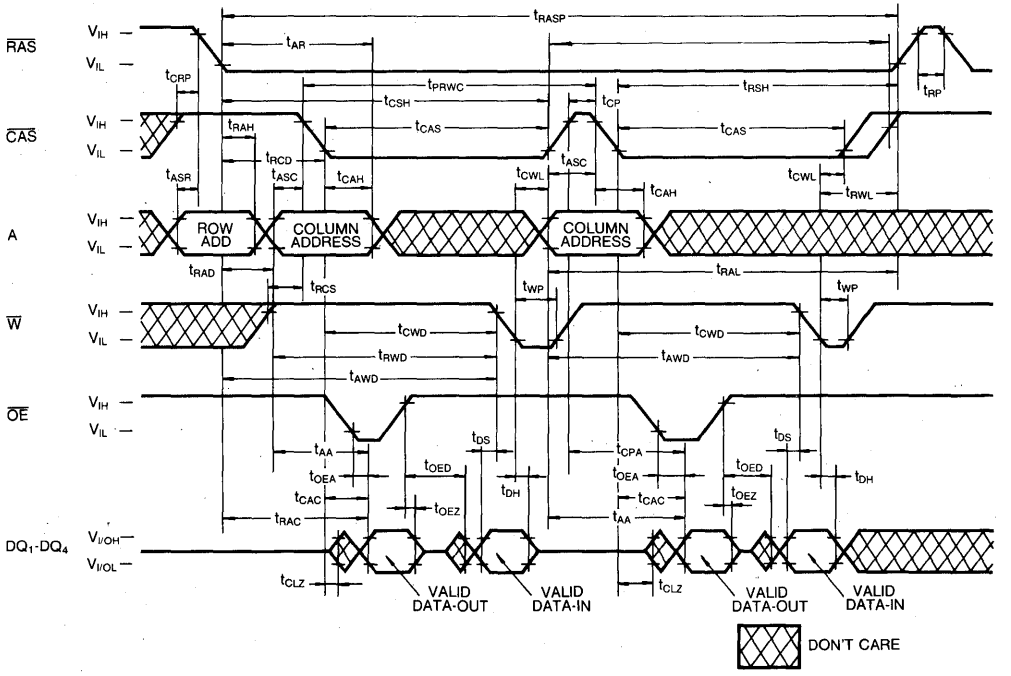
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

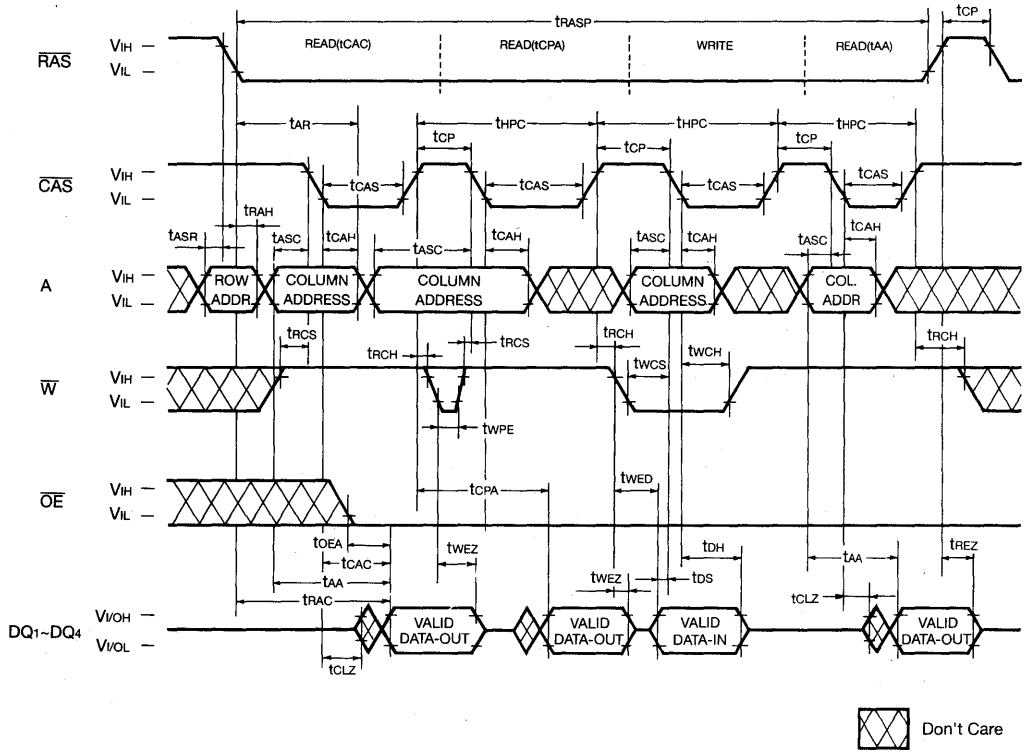
HYPER PAGE WRITE CYCLE (EARLY WRITE)



HYPER PAGE READ-MODIFY-WRITE CYCLE

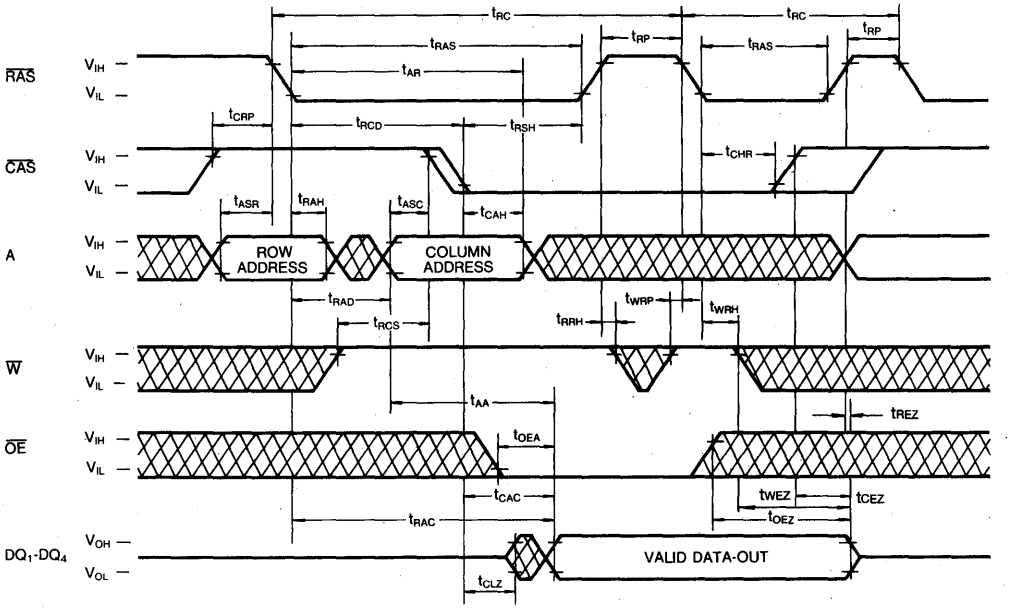


HYPER PAGE READ AND WRITE MIXED CYCLE

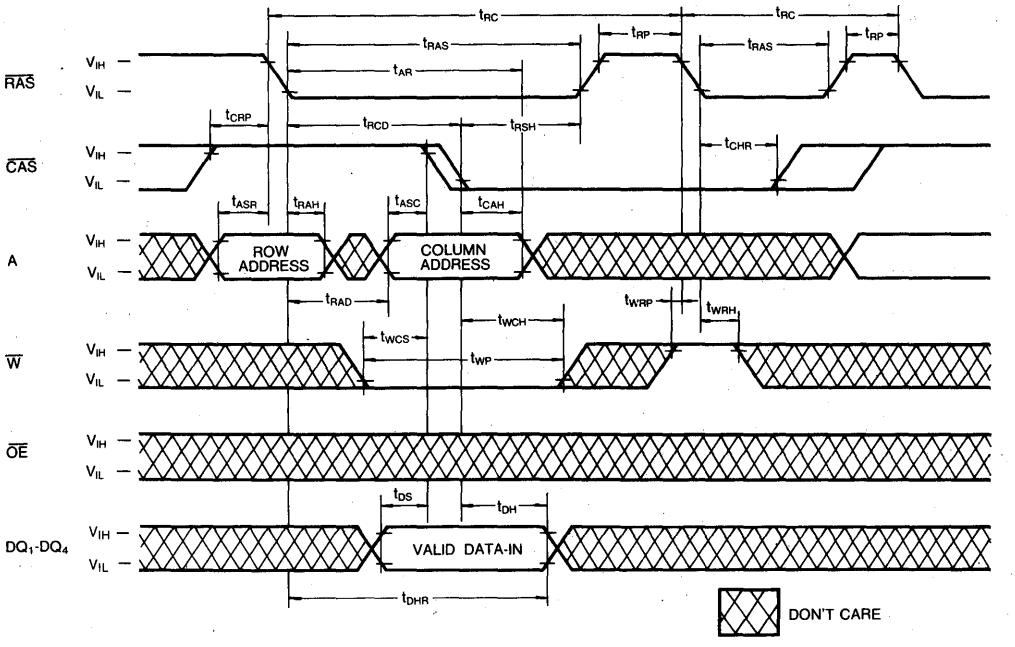


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

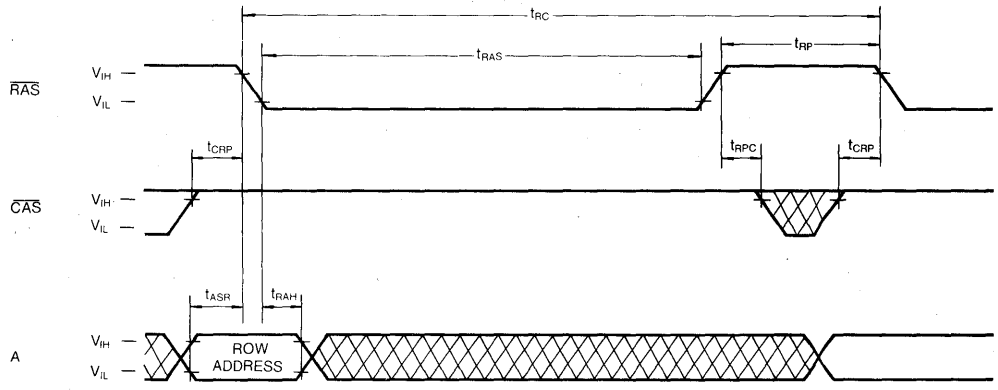


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

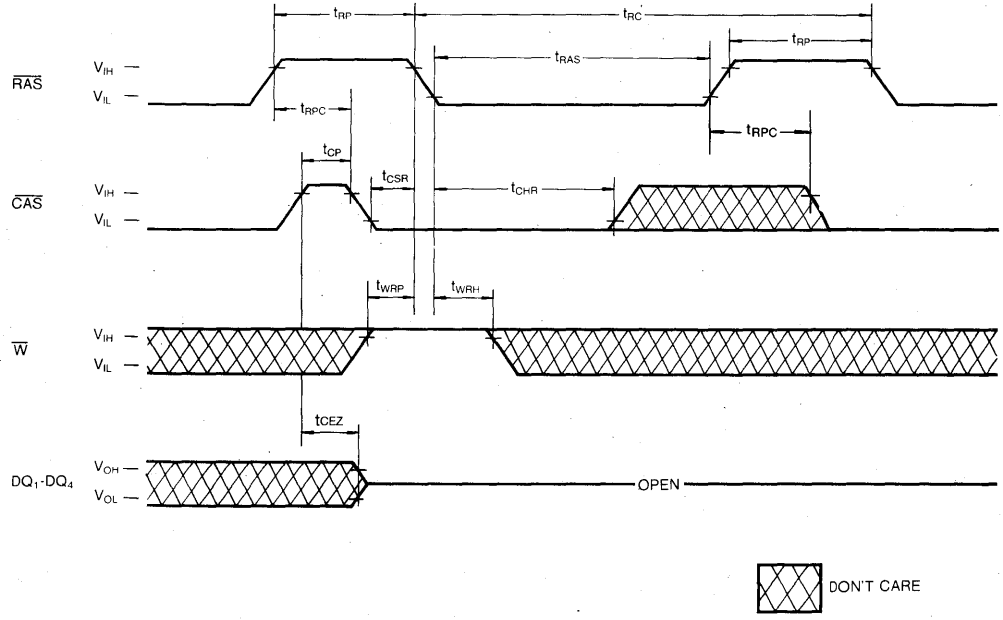
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

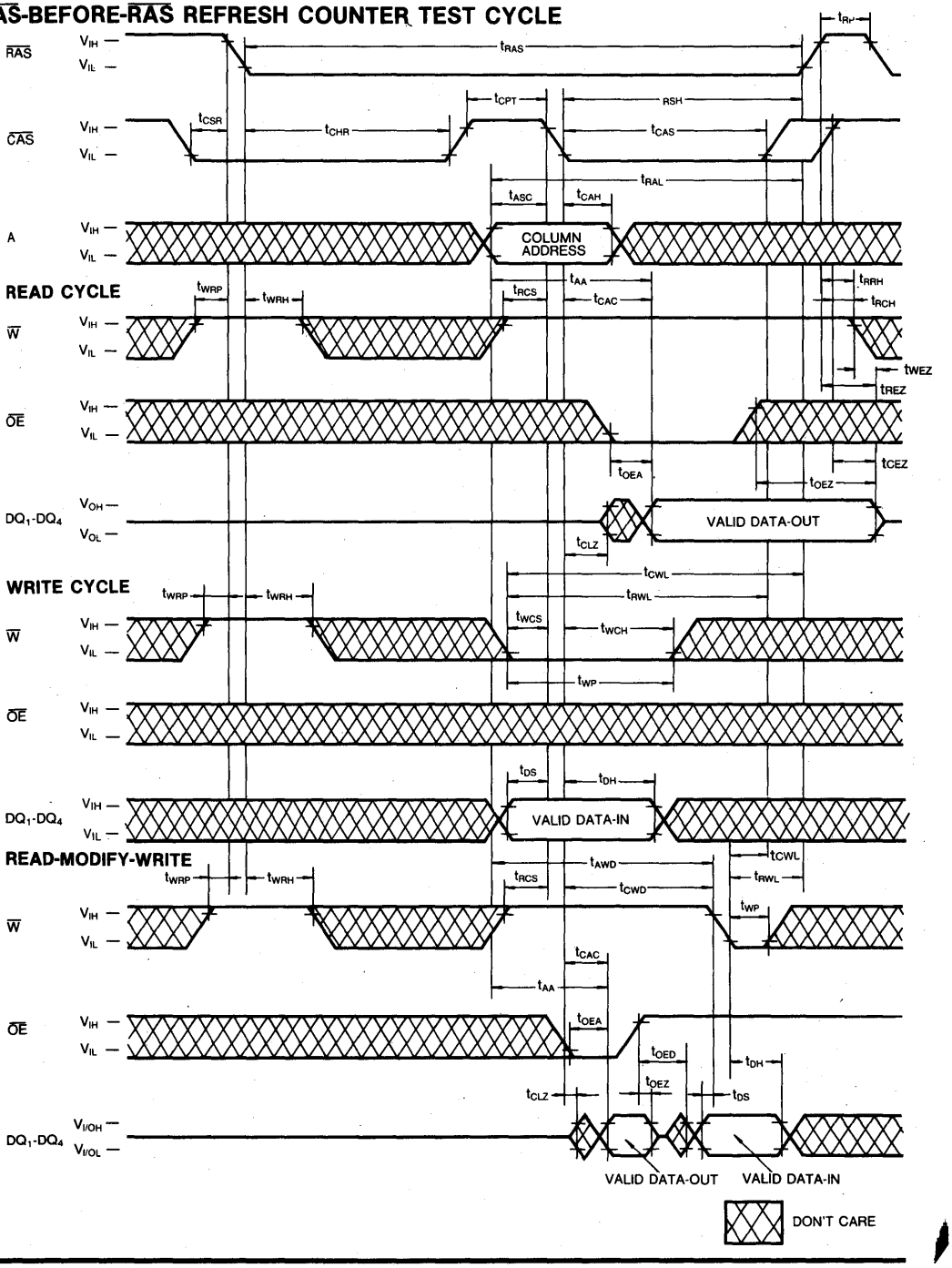
Note: $\overline{OE}$, Address=Don't Care



SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

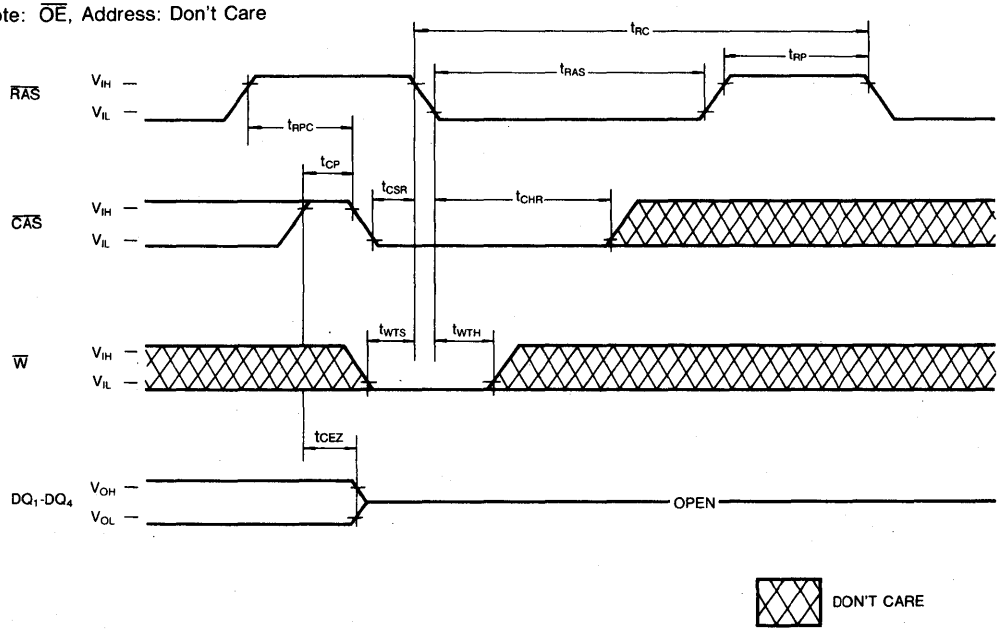
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



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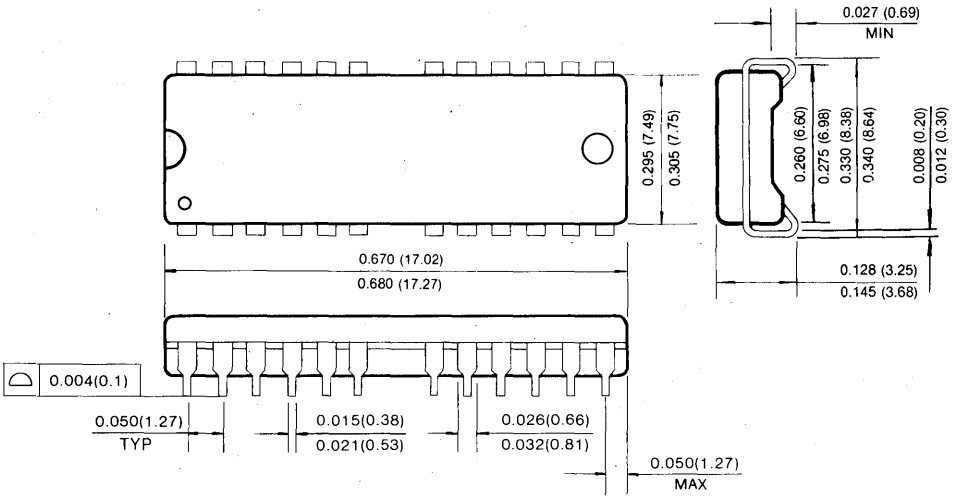
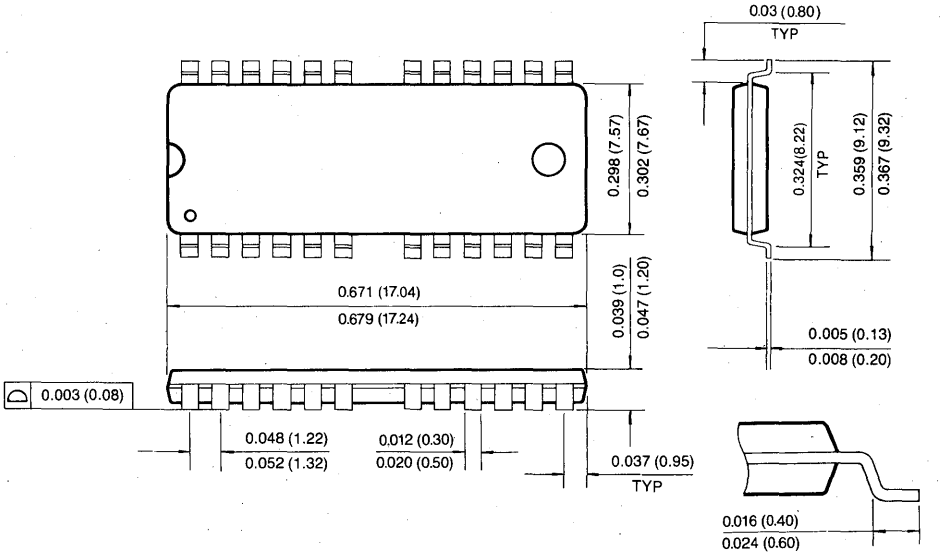
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

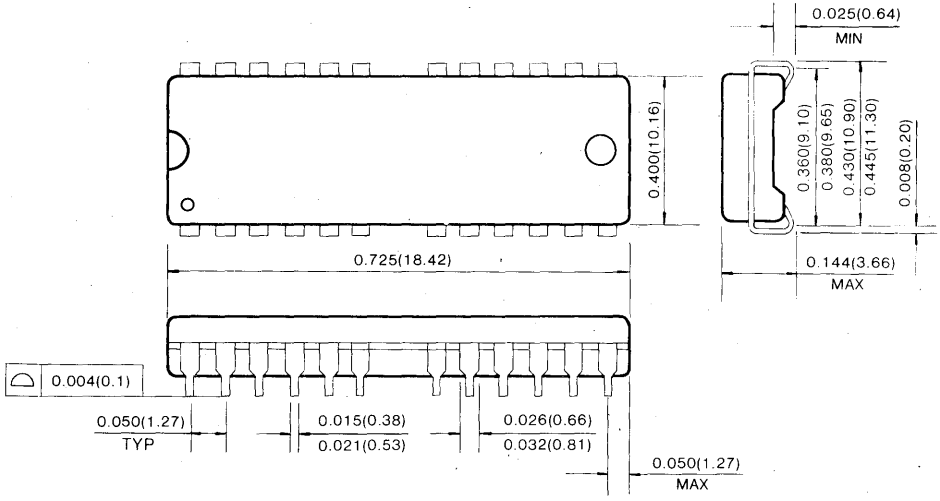


SAMSUNG ELECTRONICS

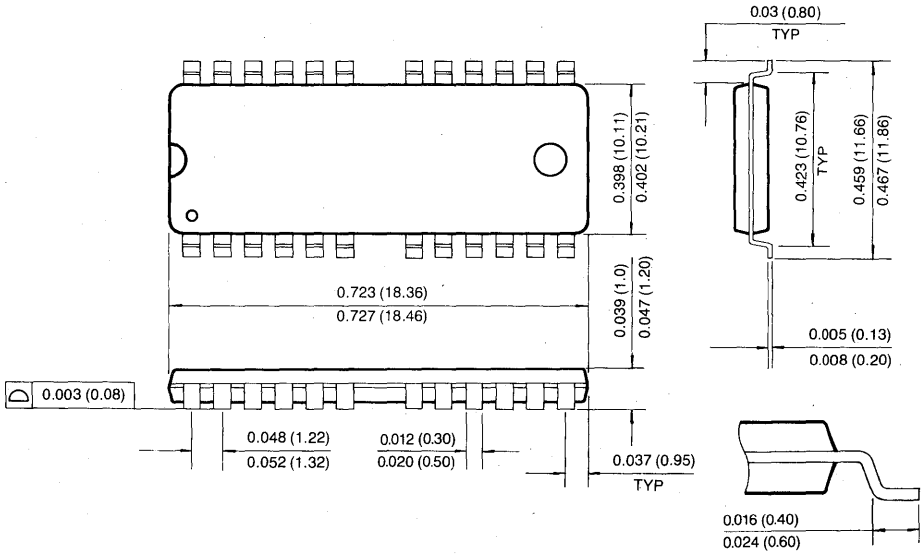
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



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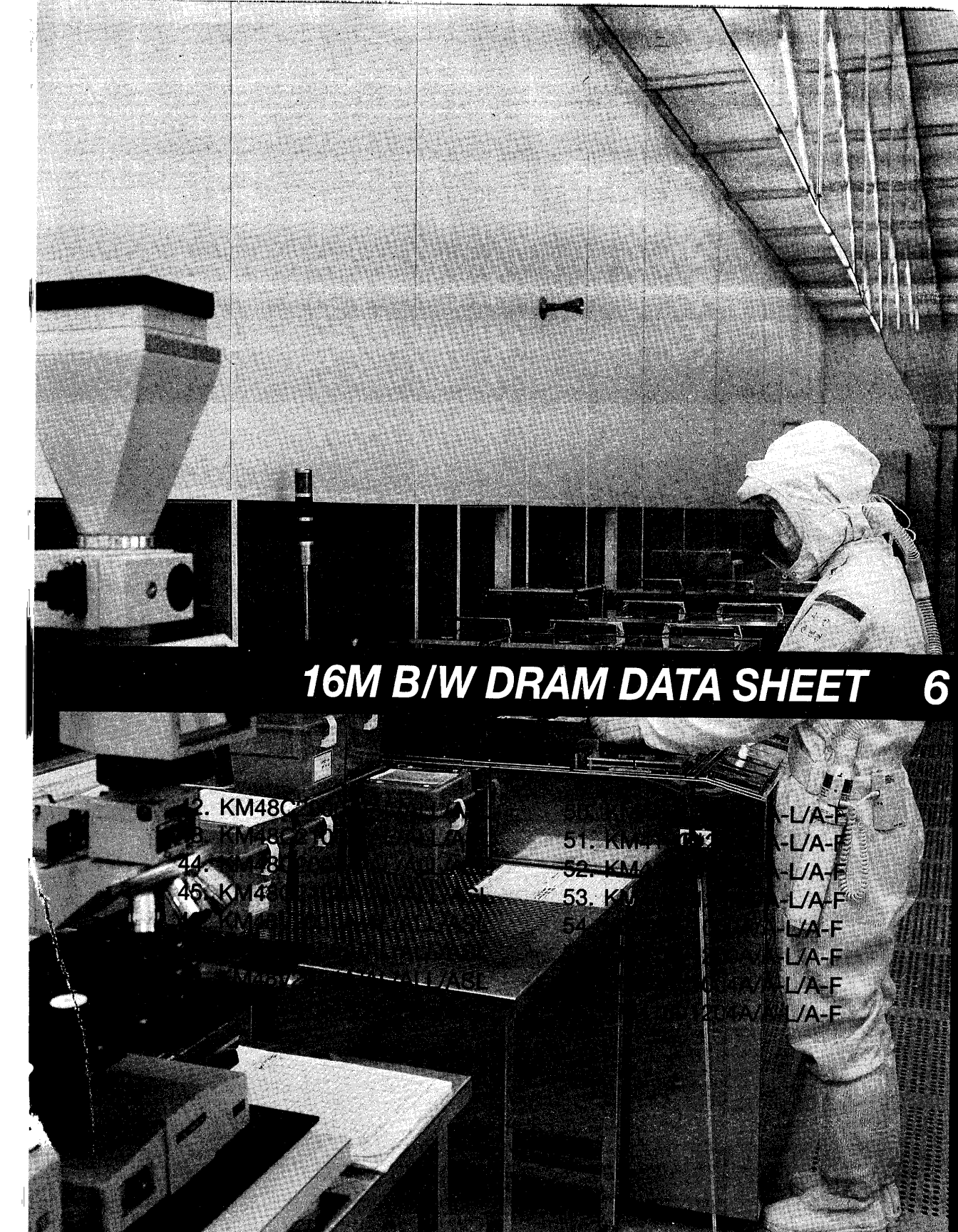
NOTES



16M B/W DRAM DATA SHEET 6

2M ×8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM48C2000A/AL/ALL/ASL-5	50ns	13ns	90ns
KM48C2000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM48C2000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM48C2000A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **CAS-before-RAS refresh capability**
- **RAS-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V±10% power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

GENERAL DESCRIPTION

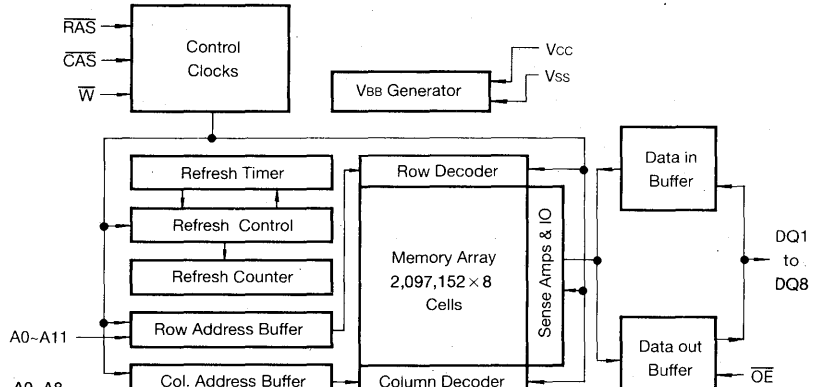
The Samsung KM48C2000A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48C2000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

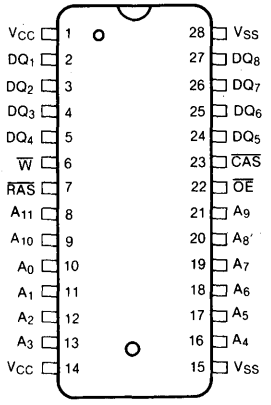
The KM48C2000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

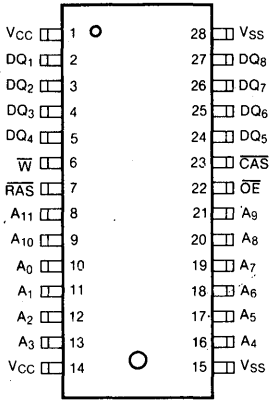


PIN CONFIGURATION (Top Views)

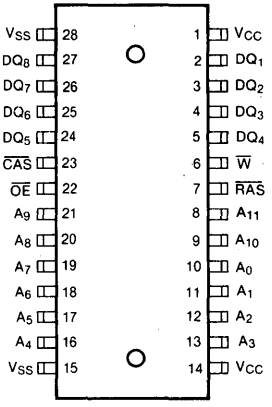
• KM48C2000 AJ/ALJ/ALLJ/ASLJ



• KM48C2000 AT/ALT/ALLT/ASLT



• KM48C2000 ATR/ALTR/ALLTR/ASLTR



Pin Name	Pin Function
A0-A11	Address Inputs
DQ1~8	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VCC	Power(+5.0V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48C2000A/AL/ALL/ASL-5	I_{CC1}	-	90	mA
	KM48C2000A/AL/ALL/ASL-6			80	mA
	KM48C2000A/AL/ALL/ASL-7			70	mA
	KM48C2000A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48C2000A	I_{CC2}	-	2	mA
	KM48C2000AL			1	mA
	KM48C2000ALL			1	mA
	KM48C2000ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM48C2000A/AL/ALL/ASL-5	I_{CC3}	-	90	mA
	KM48C2000A/AL/ALL/ASL-6			80	mA
	KM48C2000A/AL/ALL/ASL-7			70	mA
	KM48C2000A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM48C2000A/AL/ALL/ASL-5	I_{CC4}	-	80	mA
	KM48C2000A/AL/ALL/ASL-6			70	mA
	KM48C2000A/AL/ALL/ASL-7			60	mA
	KM48C2000A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM48C2000A	I_{CC5}	-	1	mA
	KM48C2000AL			300	μA
	KM48C2000ALL			200	μA
	KM48C2000ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48C2000A/AL/ALL/ASL-5	I_{CC6}	-	90	mA
	KM48C2000A/AL/ALL/ASL-6			80	mA
	KM48C2000A/AL/ALL/ASL-7			70	mA
	KM48C2000A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=31.25μS(L-Ver.) 62.5μS(SL-Ver.), T_{RAS}≦300ns	KM48C2000AL	I_{CC7}	-	450	μA
	KM48C2000ASL			350	μA

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SAMSUNG ELECTRONICS

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{CC}-0.2V or 0.2V DQ_1-DQ_8=V_{CC}-0.2V, 0.2V or Open	KM48C2000ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±0.5V, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64		64	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to W delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	76		85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ pulse width(Fast Page mode)	t_{RASP}	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		13		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	13		15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

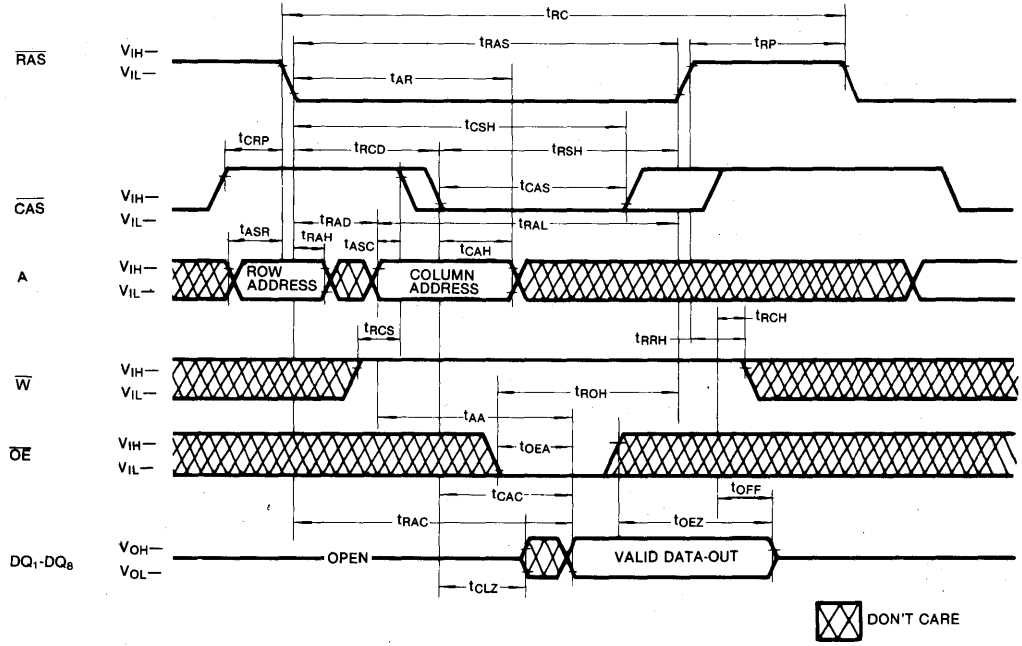
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS

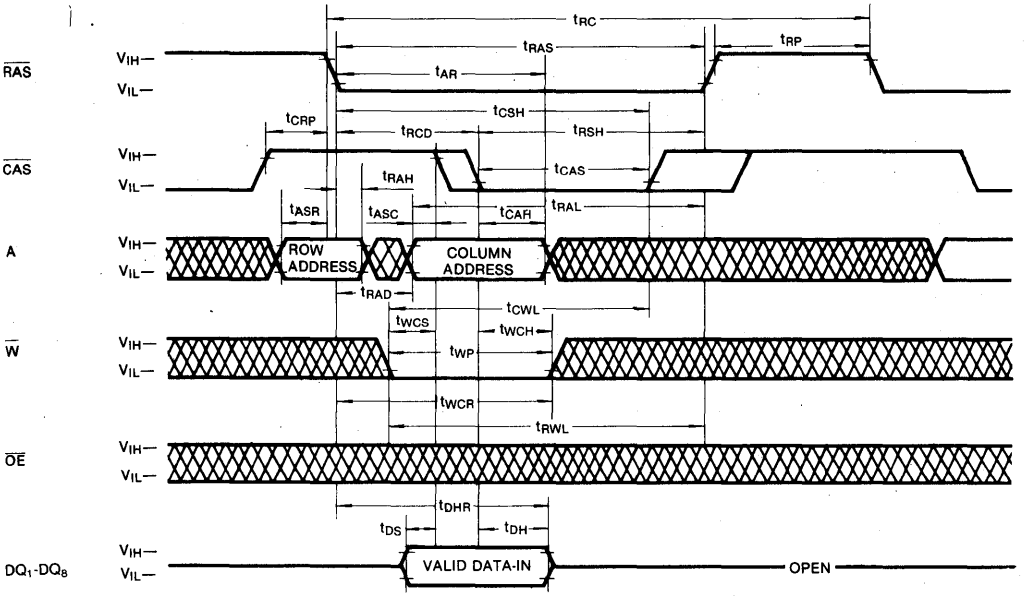
READ CYCLE



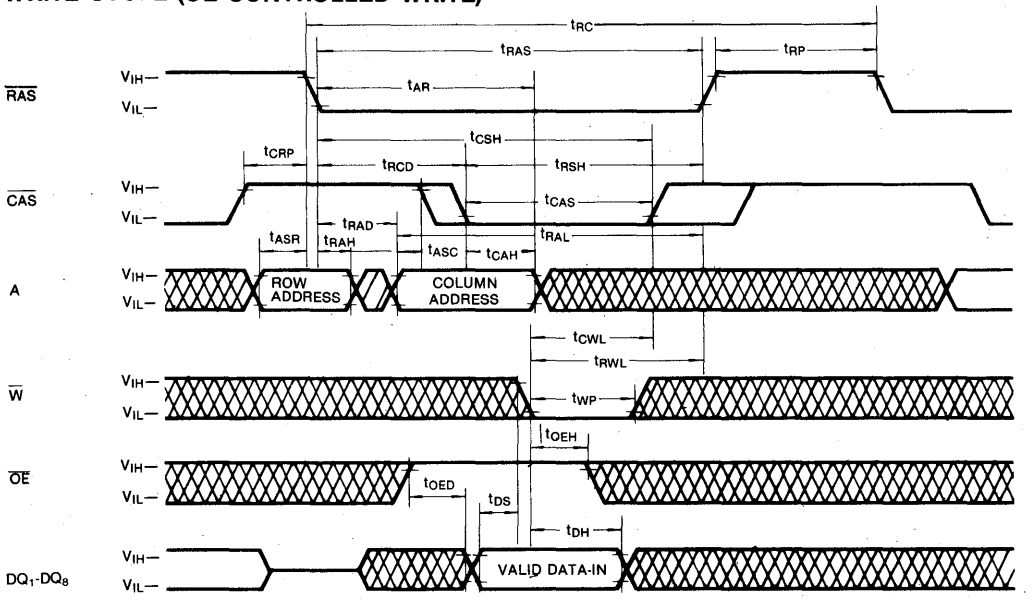
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

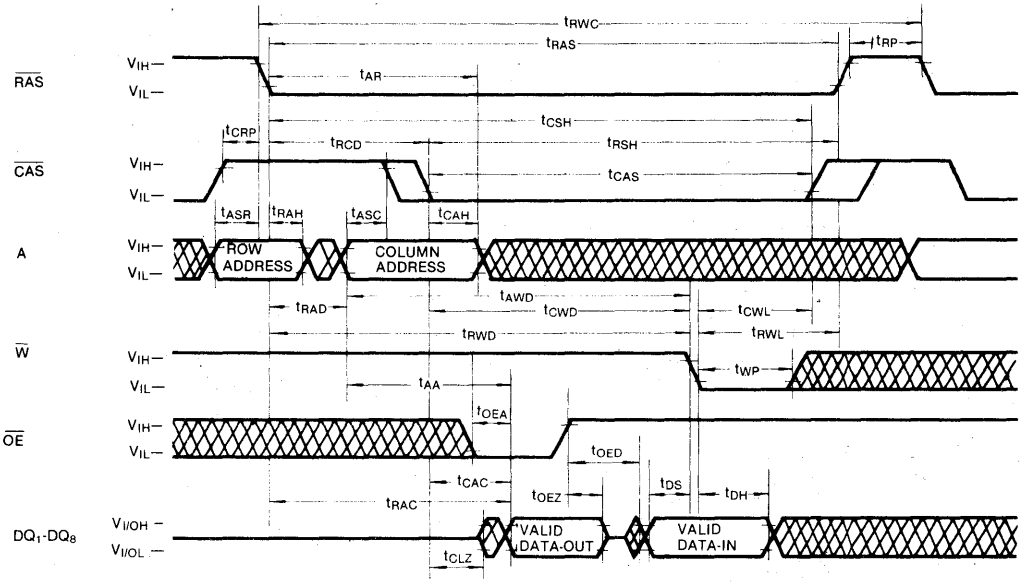


WRITE CYCLE (OE CONTROLLED WRITE)

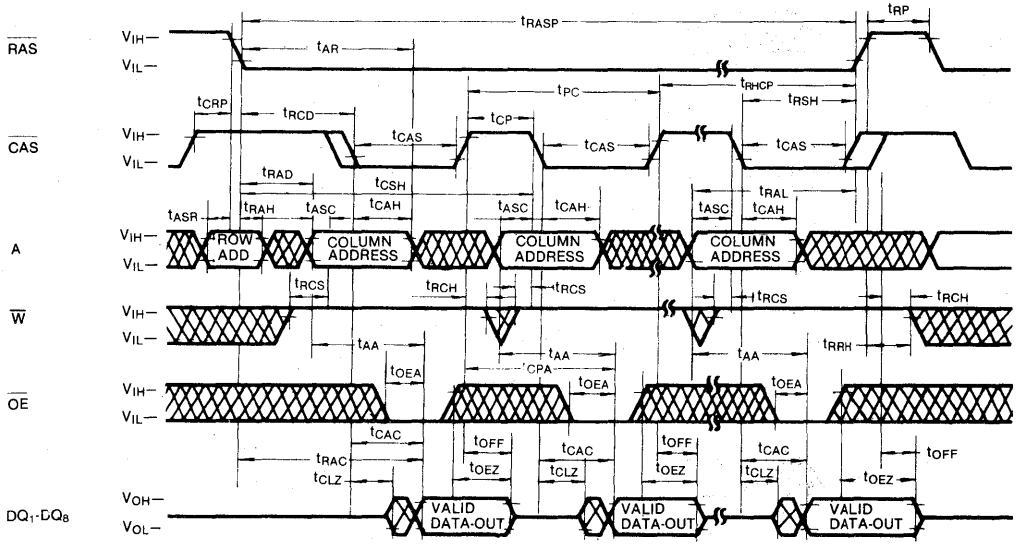


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



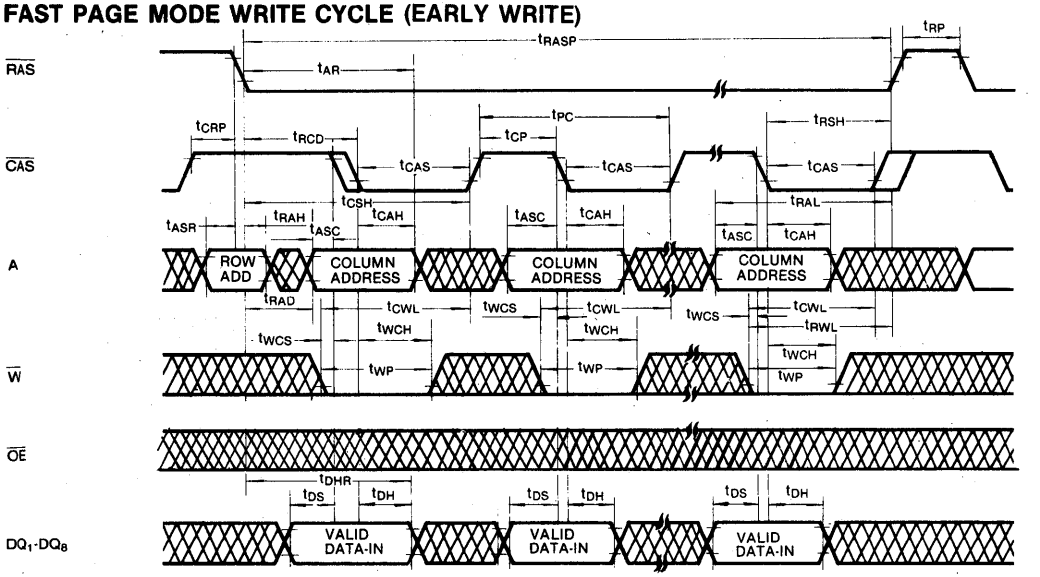
FAST PAGE MODE READ CYCLE



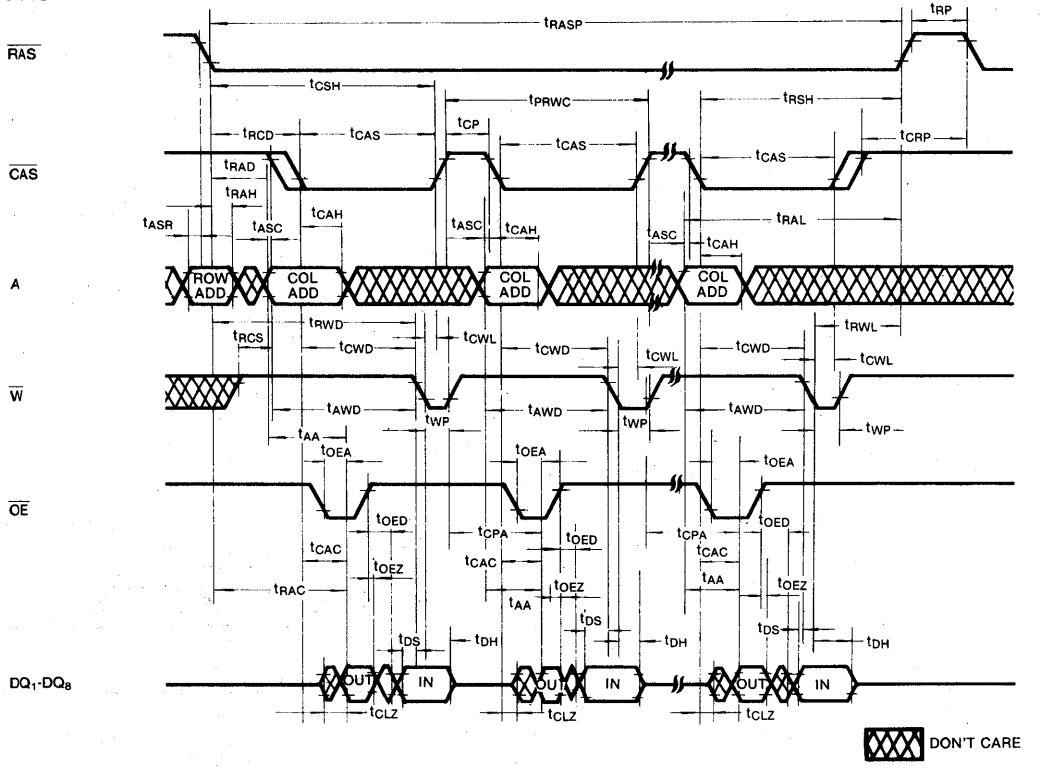
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



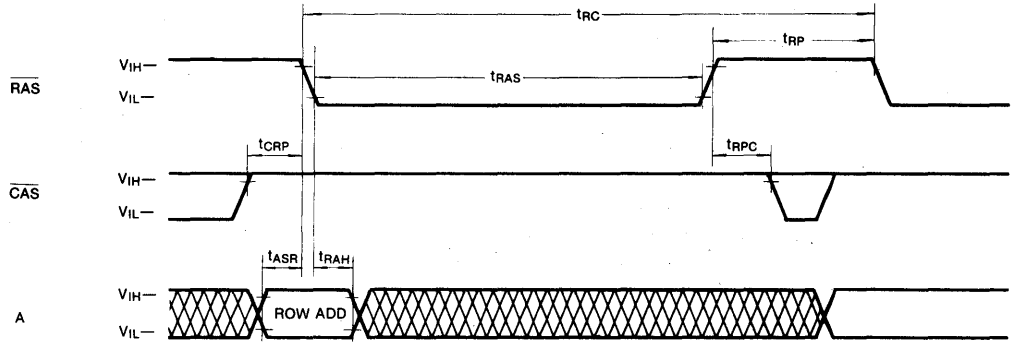
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

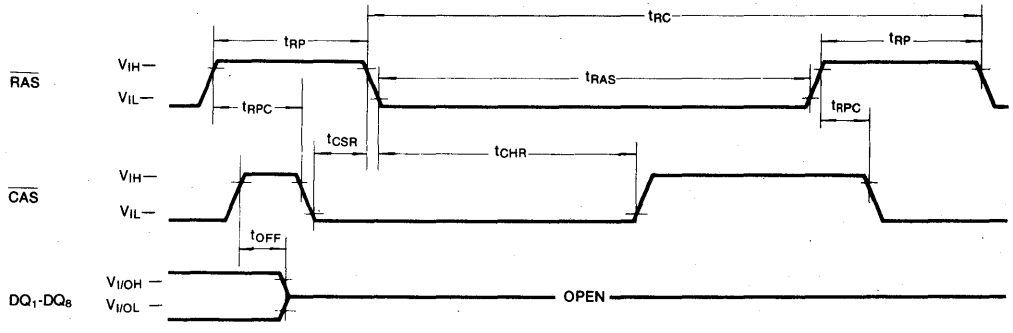
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



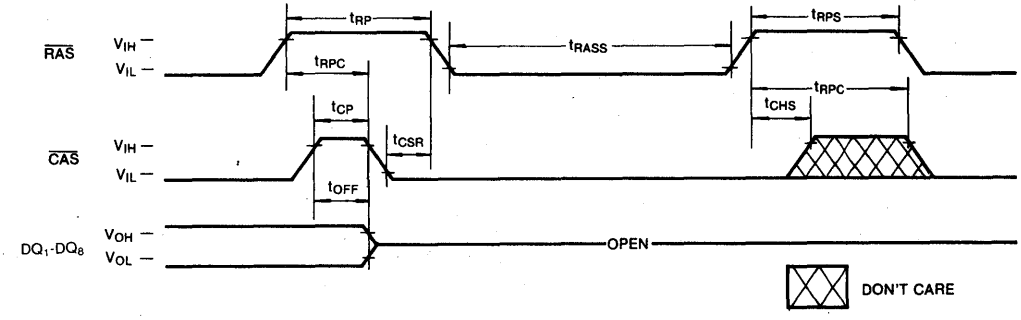
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



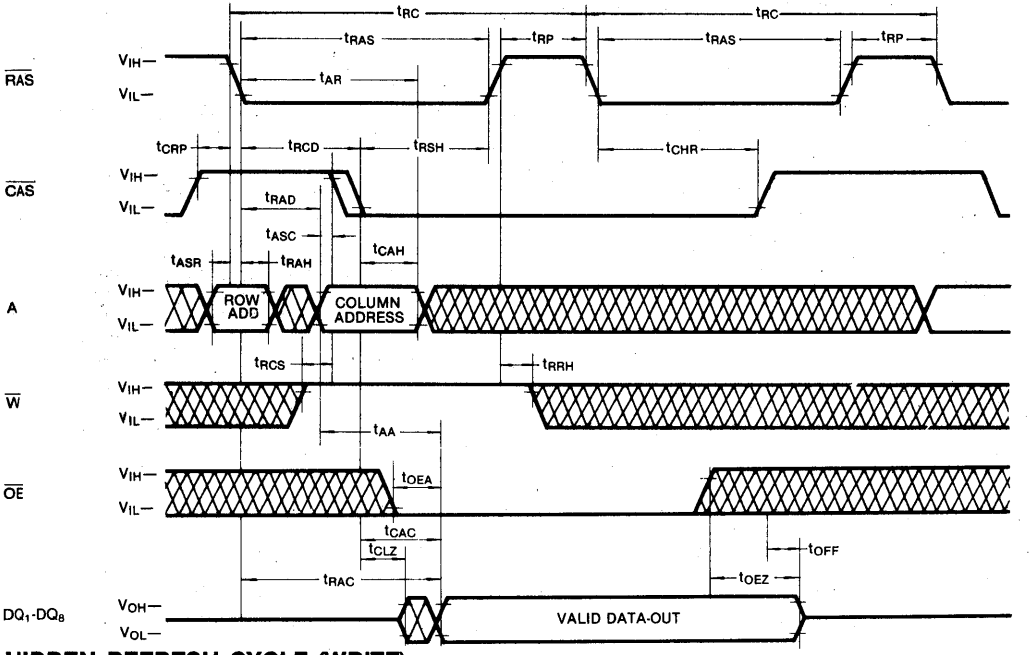
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

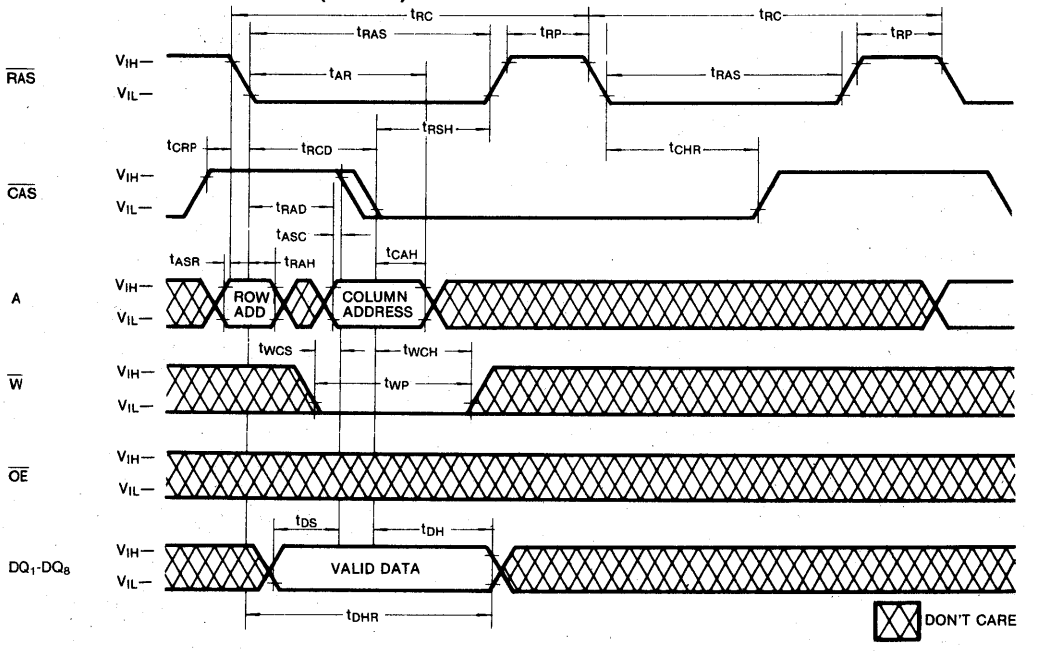


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

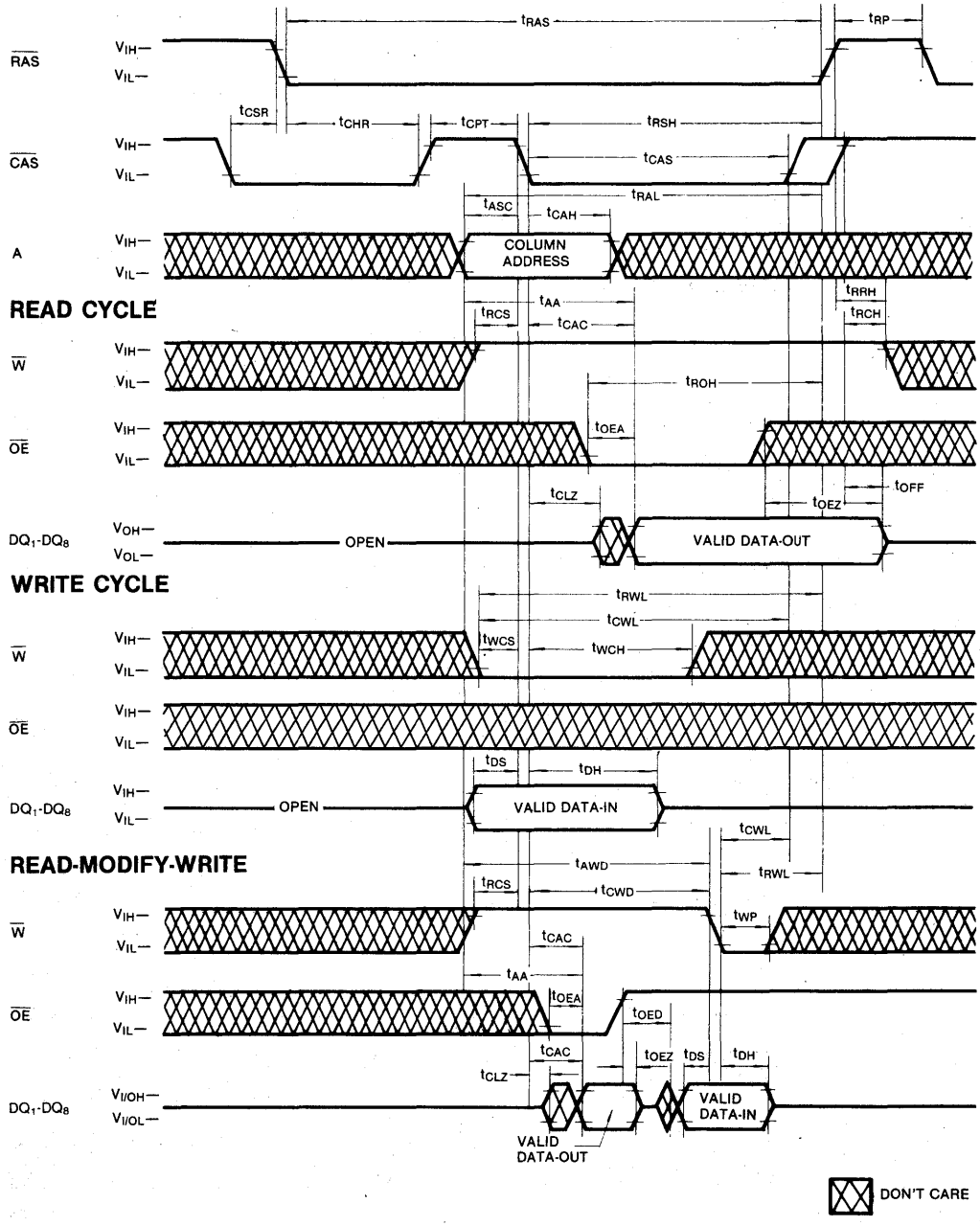


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

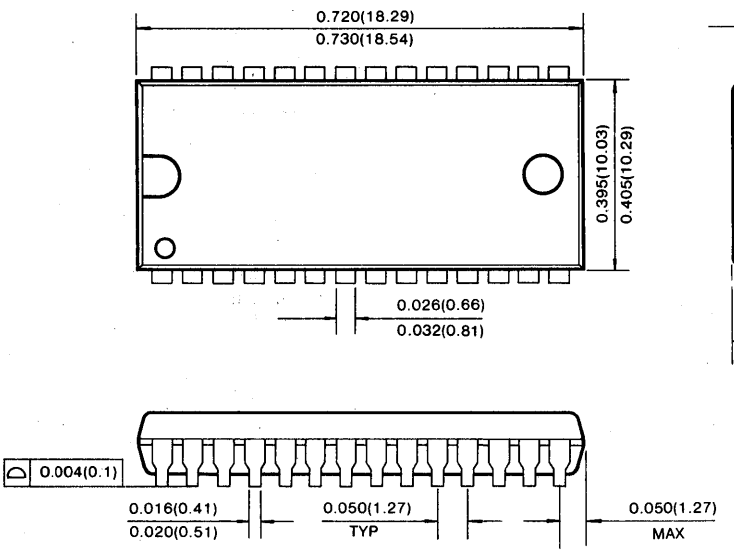
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE DIMENSION

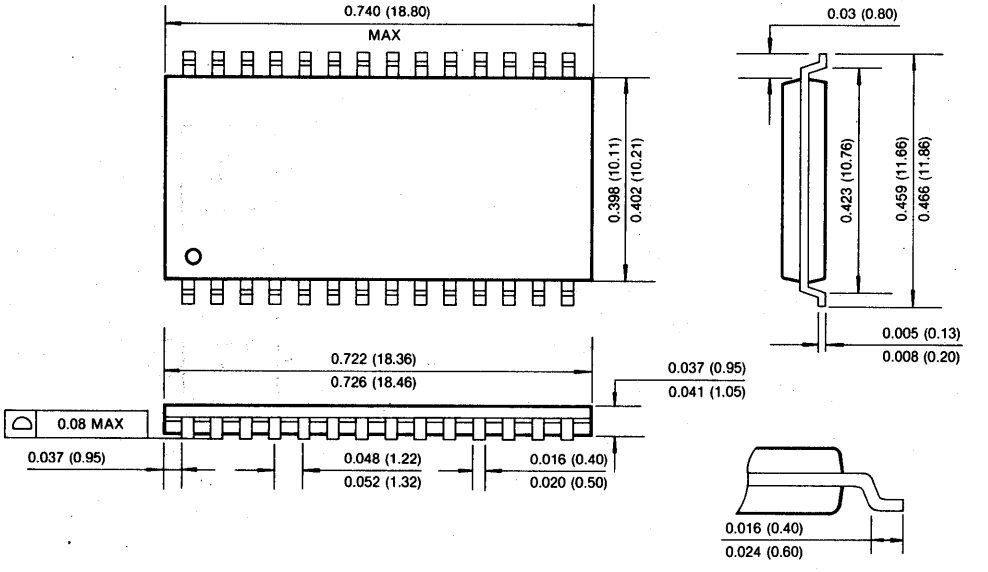
28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)



2M ×8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM48C2100A/AL/ALL/ASL-5	50ns	13ns	90ns
KM48C2100A/AL/ALL/ASL-6	60ns	15ns	110ns
KM48C2100A/AL/ALL/ASL-7	70ns	20ns	130ns
KM48C2100A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V ± 10% power supply**
- **2048 cycles/32ms refresh (Normal)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

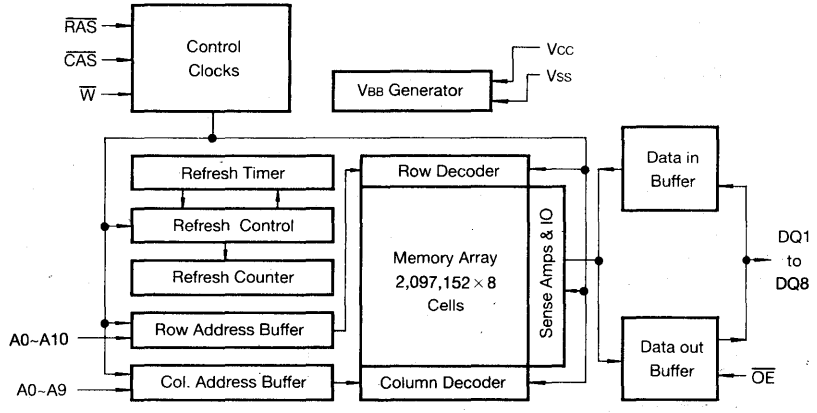
The Samsung KM48C2100A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48C2100A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48C2100A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

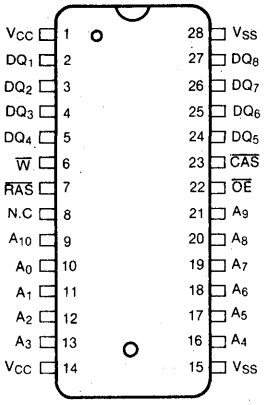
FUNCTIONAL BLOCK DIAGRAM



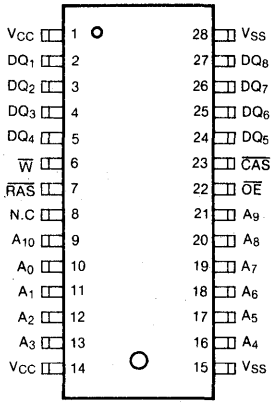
6

PIN CONFIGURATION (Top Views)

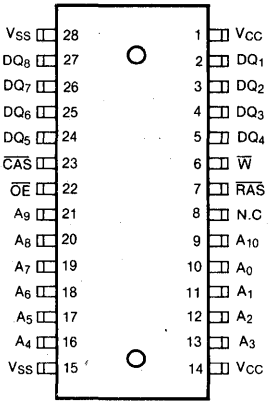
• KM48C2100 AJ/ALJ/ALLJ/ASLJ



• KM48C2100 AT/ALT/ALLT/ASLT



• KM48C2100 ATR/ALTR/ALLTR/ASLTR



Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ1~8	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power(+5V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48C2100A/AL/ALL/ASL-5	I_{CC1}	-	110	mA
	KM48C2100A/AL/ALL/ASL-6			100	mA
	KM48C2100A/AL/ALL/ASL-7			90	mA
	KM48C2100A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48C2100A	I_{CC2}	-	2	mA
	KM48C2100AL			1	mA
	KM48C2100ALL			1	mA
	KM48C2100ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM48C2100A/AL/ALL/ASL-5	I_{CC3}	-	110	mA
	KM48C2100A/AL/ALL/ASL-6			100	mA
	KM48C2100A/AL/ALL/ASL-7			90	mA
	KM48C2100A/AL/ALL/ASL-8			80	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM48C2100A/AL/ALL/ASL-5	I_{CC4}	-	90	mA
	KM48C2100A/AL/ALL/ASL-6			80	mA
	KM48C2100A/AL/ALL/ASL-7			70	mA
	KM48C2100A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM48C2100A	I_{CC5}	-	1	mA
	KM48C2100AL			300	μA
	KM48C2100ALL			200	μA
	KM48C2100ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48C2100A/AL/ALL/ASL-5	I_{CC6}	-	110	mA
	KM48C2100A/AL/ALL/ASL-6			100	mA
	KM48C2100A/AL/ALL/ASL-7			90	mA
	KM48C2100A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=62.5μS(L-Ver.) 125μS(SL-Ver.), T_{RAS}≦300ns	KM48C2100AL	I_{CC7}	-	400	μA
	KM48C2100ASL			300	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{10}=V_{CC}-0.2V or 0.2V DQ_1-DQ_8=V_{CC}-0.2V, 0.2V or Open	KM48C2100ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{10})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1-DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		32		32		32		32	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	76		85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ pulse width(Fast Page mode)	t_{RASP}	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		13		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	13		15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note 12)

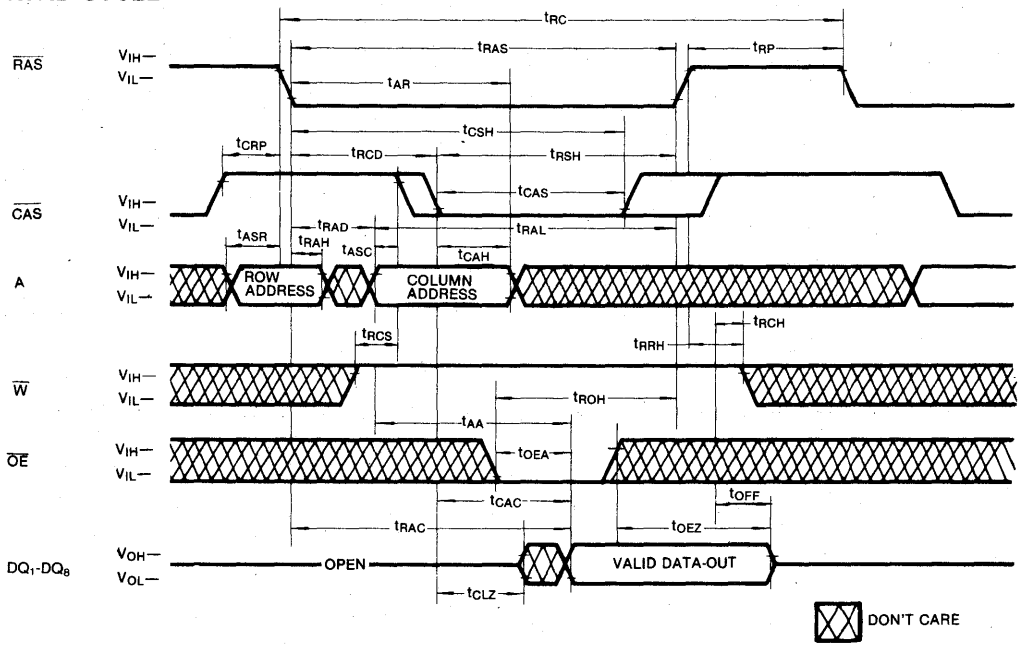
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

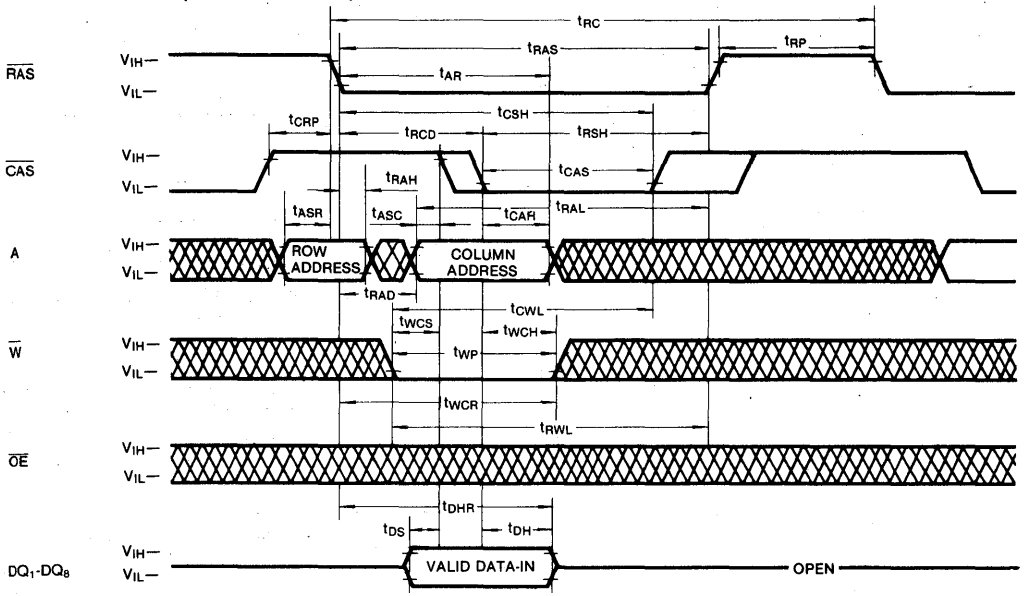
TIMING DIAGRAMS

READ CYCLE

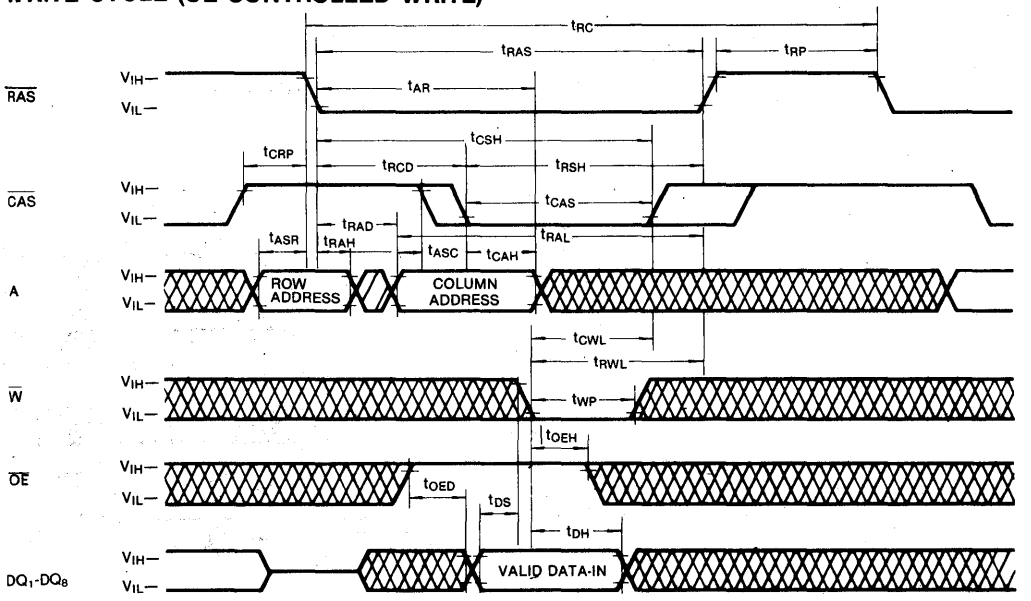


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



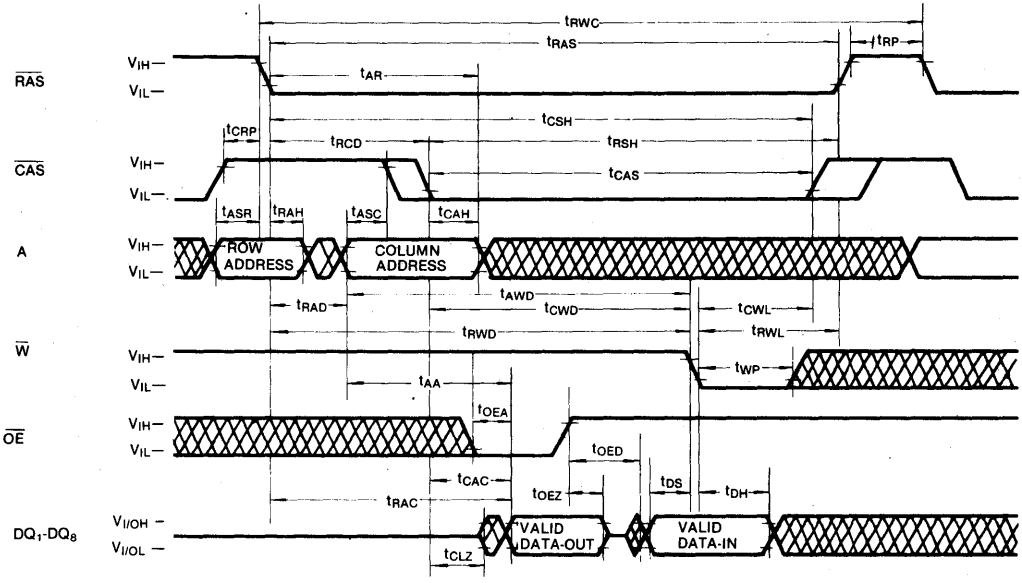
WRITE CYCLE (OE CONTROLLED WRITE)



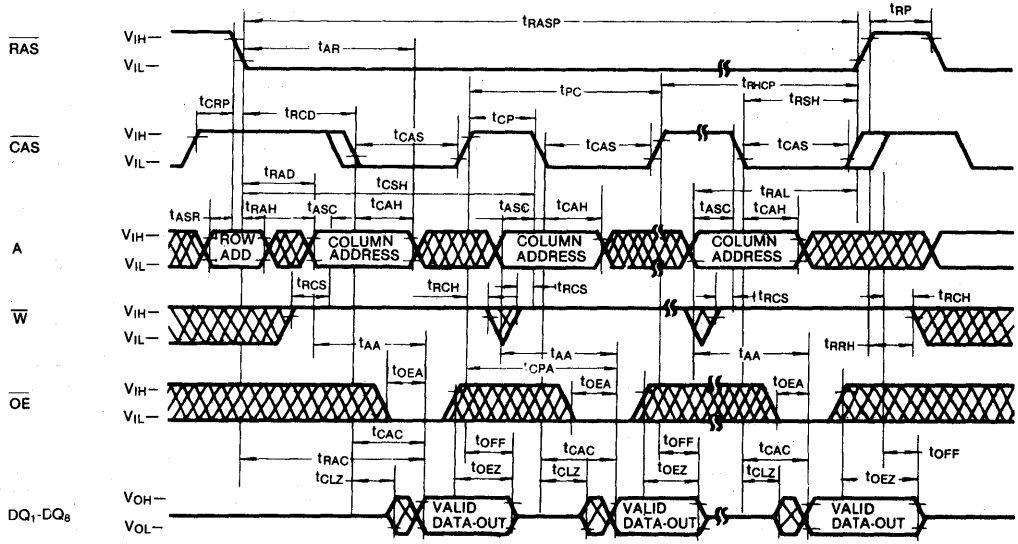
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

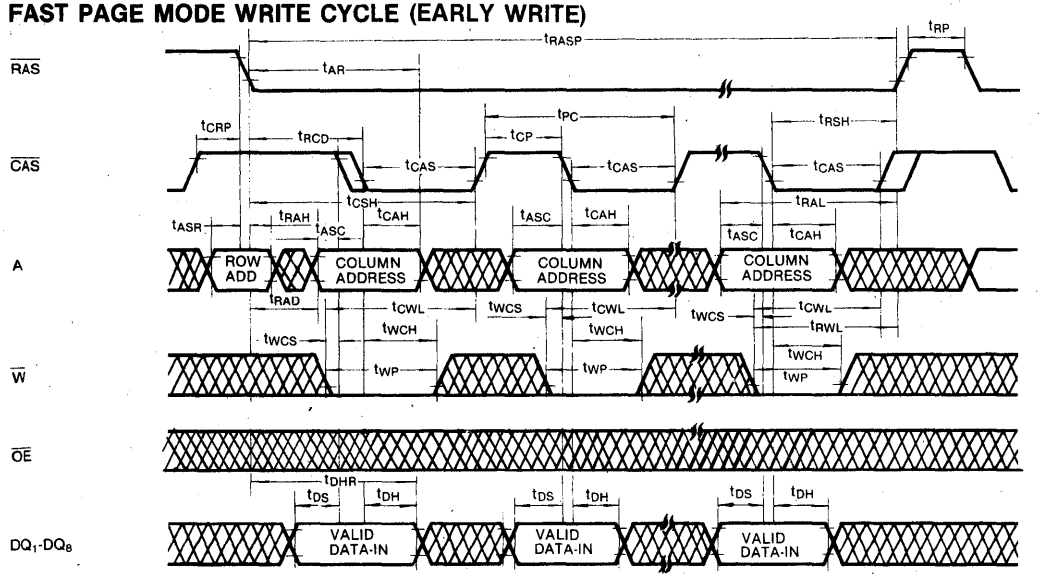


DON'T CARE

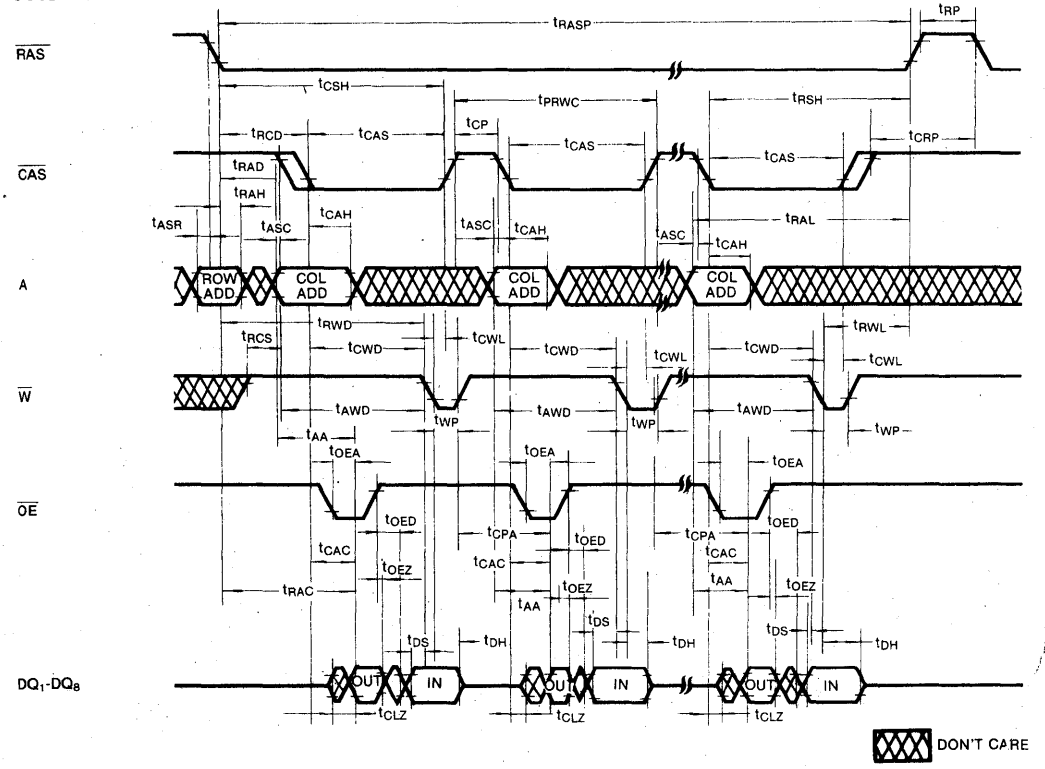
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

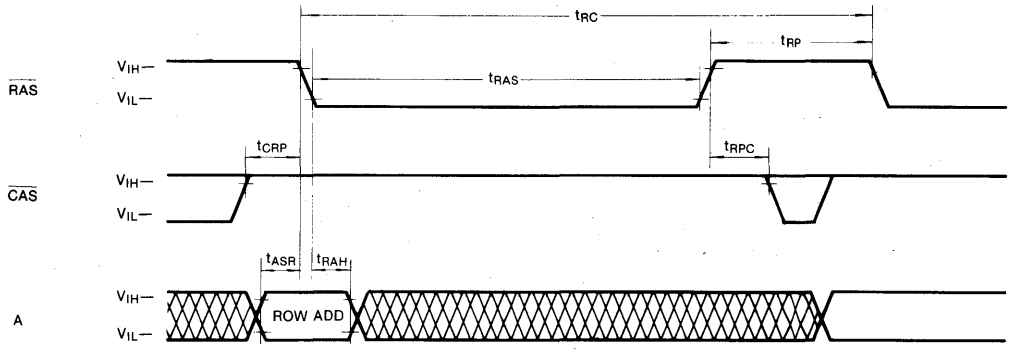


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

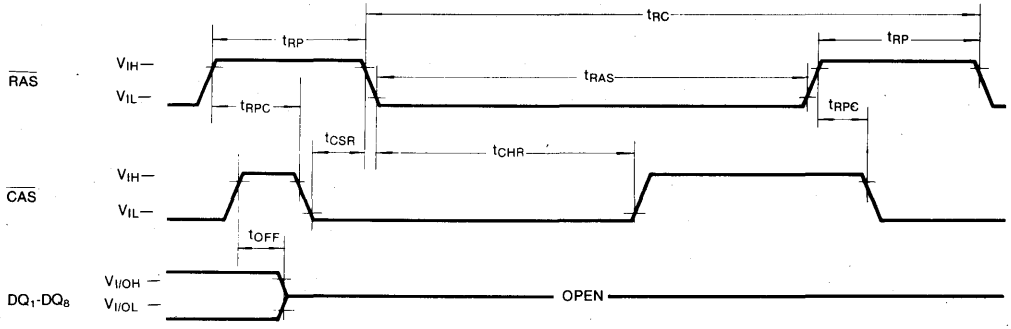
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



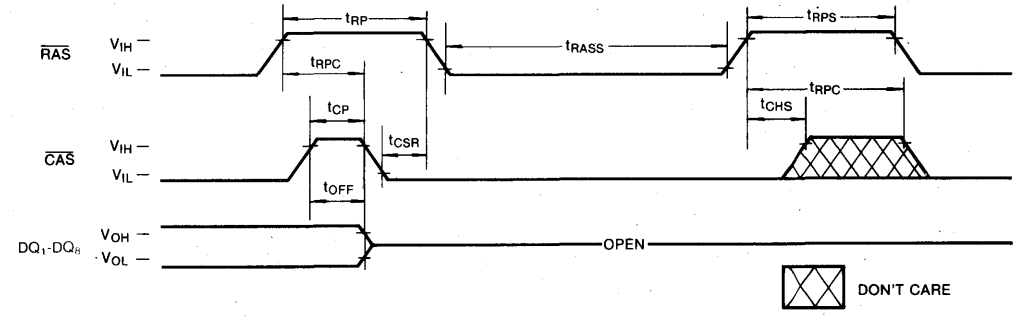
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



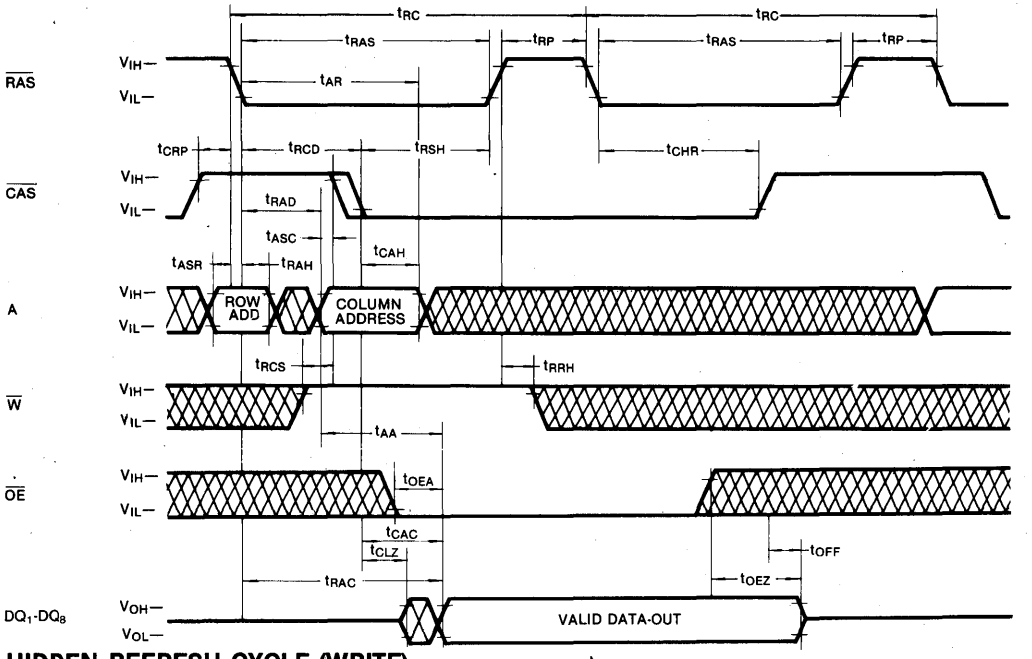
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

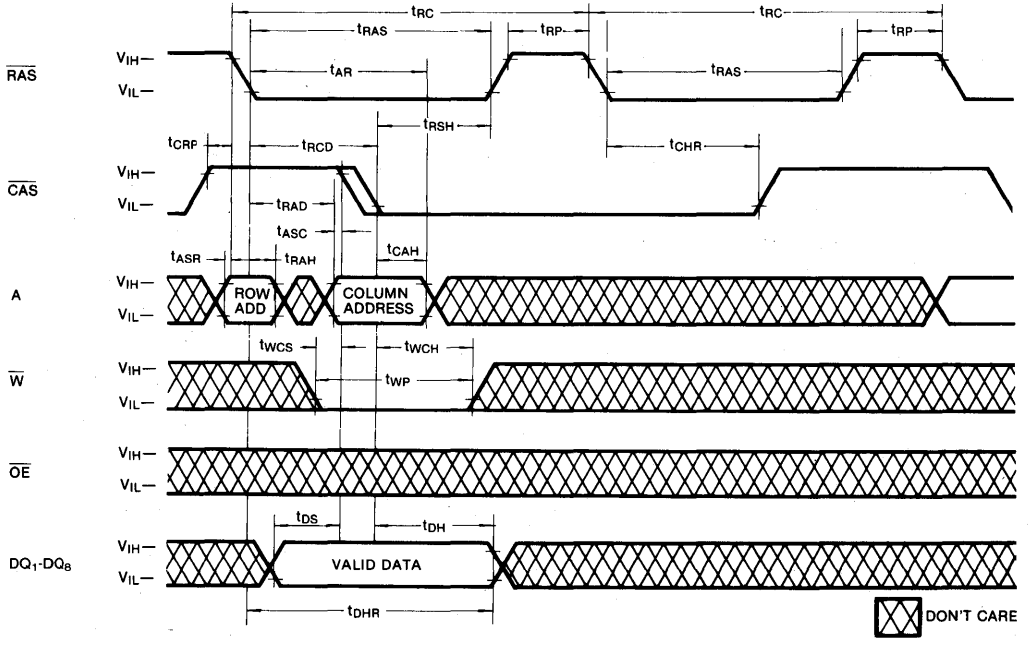


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

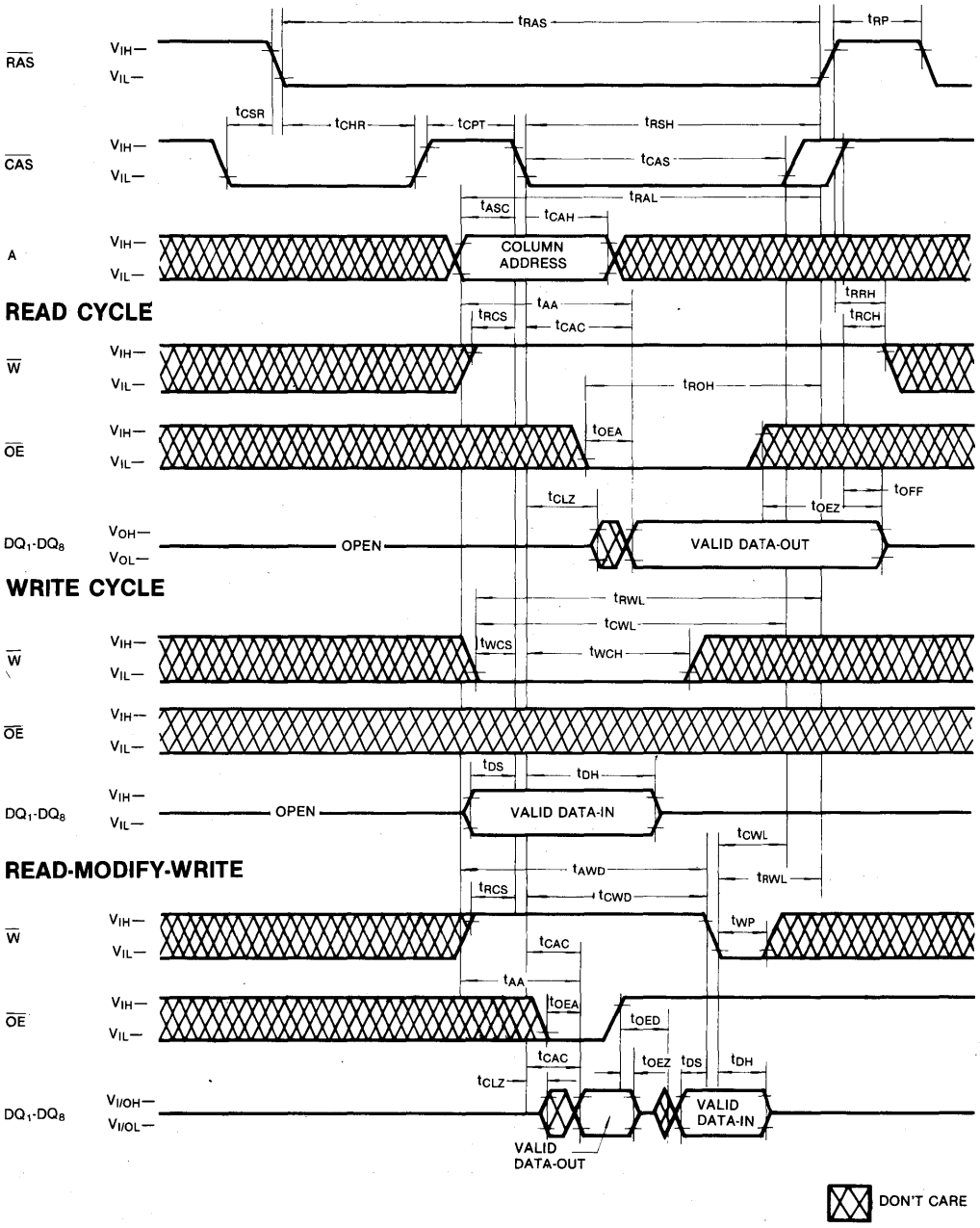


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

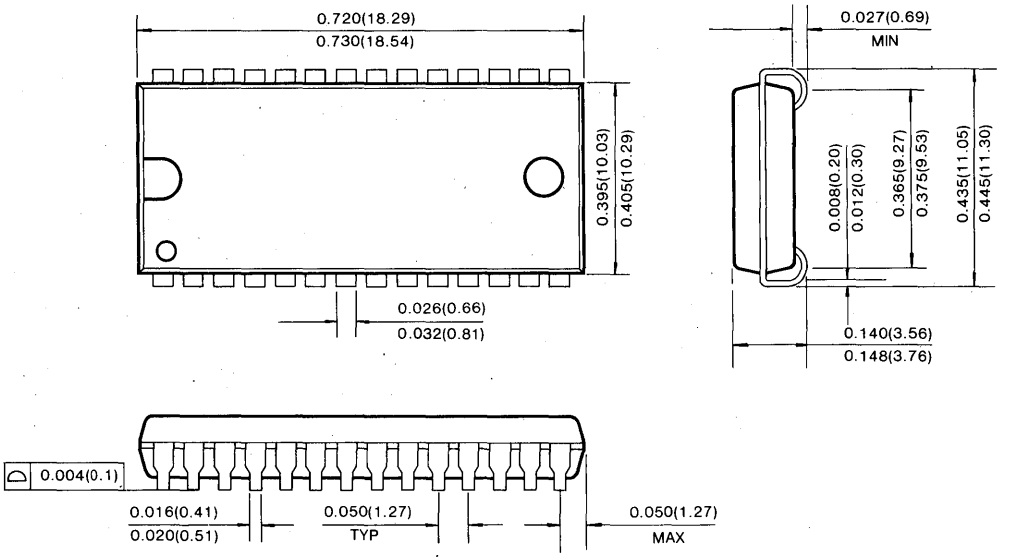
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE DIMENSION

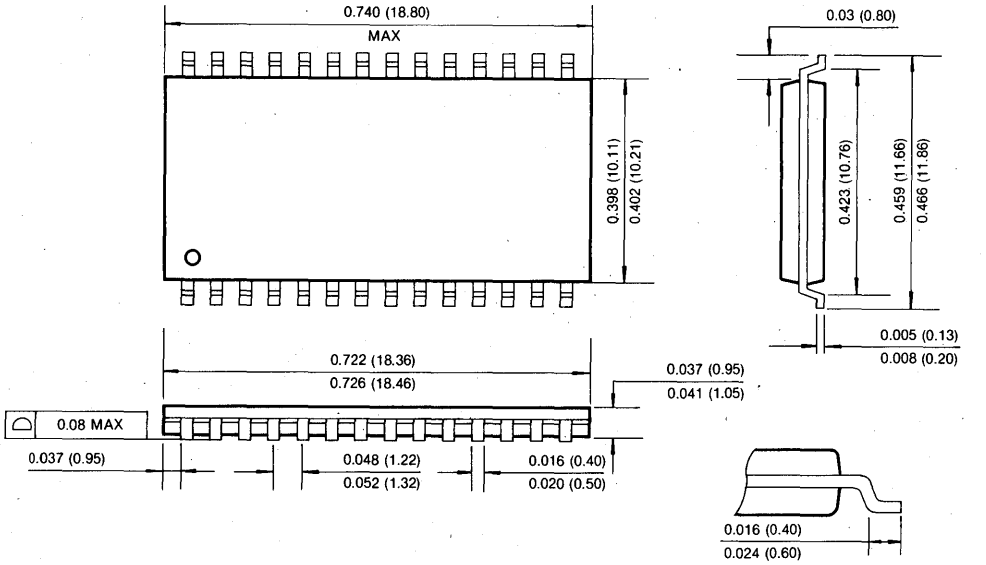
28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)



2M ×8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM48C2004A/AL/ALL/ASL-5	50ns	13ns	90ns	20ns
KM48C2004A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM48C2004A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM48C2004A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- **Fast Page Mode with Extended data out**
- **Self Refresh Operation (LL-ver. only)**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single +5.0V±10% power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

GENERAL DESCRIPTION

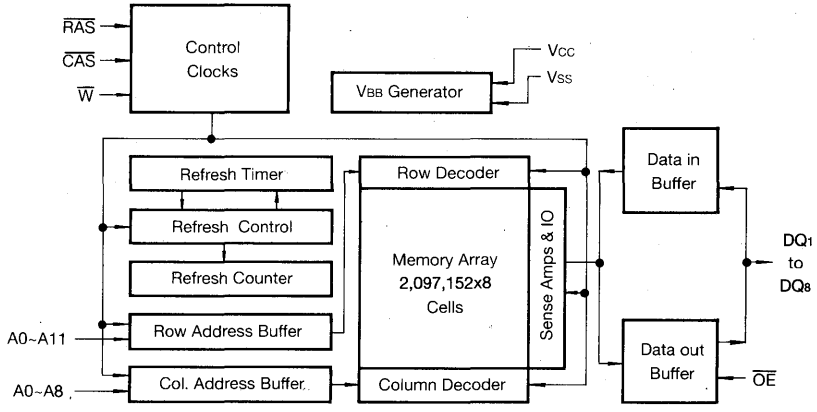
The Samsung KM48C2004A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit×8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48C2004A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48C2004A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

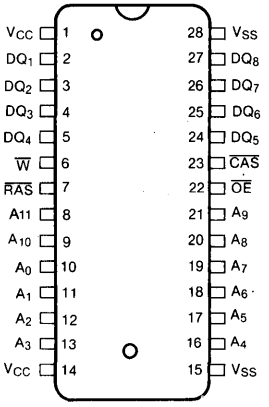


6

SAMSUNG ELECTRONICS

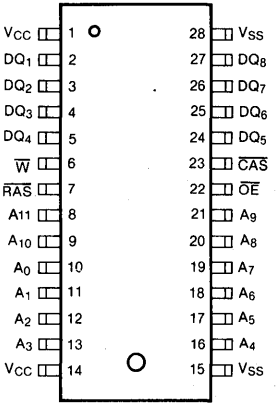
PIN CONFIGURATION (Top Views)

• KM48C2004 AJ/ALJ/ALLJ/ASLJ



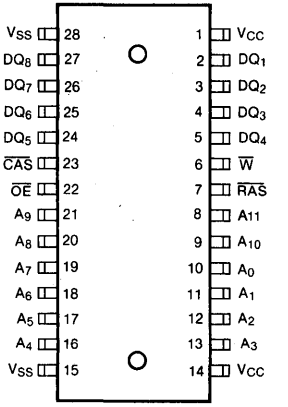
J : 400MIL

• KM48C2004 AT/ALT/ALLT/ASLT



T : 400MIL (Forword)

• KM48C2004 ATR/ALTR/ALLTR/ASLTR



TR : 400MIL (Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-8	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power(+5.0V)

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48C2004A/AL/ALL/ASL-5	I_{CC1}	-	90	mA
	KM48C2004A/AL/ALL/ASL-6			80	mA
	KM48C2004A/AL/ALL/ASL-7			70	mA
	KM48C2004A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48C2004A	I_{CC2}	-	2	mA
	KM48C2004AL			1	mA
	KM48C2004ALL			1	mA
	KM48C2004ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM48C2004A/AL/ALL/ASL-5	I_{CC3}	-	90	mA
	KM48C2004A/AL/ALL/ASL-6			80	mA
	KM48C2004A/AL/ALL/ASL-7			70	mA
	KM48C2004A/AL/ALL/ASL-8			60	mA
Hyper Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM48C2004A/AL/ALL/ASL-5	I_{CC4}	-	100	mA
	KM48C2004A/AL/ALL/ASL-6			90	mA
	KM48C2004A/AL/ALL/ASL-7			80	mA
	KM48C2004A/AL/ALL/ASL-8			70	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM48C2004A	I_{CC5}	-	1	mA
	KM48C2004AL			300	μA
	KM48C2004ALL			200	μA
	KM48C2004ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48C2004A/AL/ALL/ASL-5	I_{CC6}	-	90	mA
	KM48C2004A/AL/ALL/ASL-6			80	mA
	KM48C2004A/AL/ALL/ASL-7			70	mA
	KM48C2004A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=Vcc-0.2V Input Low Voltage(V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V, DQ_1~DQ_8=Don't Care, t_{RC}=31.25μs(L-Ver.) 62.5μs(SL-Ver.), t_{RAS}=t_{RAS}min~300ns	KM48C2004AL	I_{CC7}	-	450	μA
	KM48C2004ASL			350	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{CC}-0.2V or 0.2V DQ_1-DQ_8=V_{CC}-0.2V, 0.2V or Open	KM48C2004ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, V_{CC}=5.0V±0.5V, See notes 1,2)

Test condition: V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	3	20	3	20	ns	7,14,15
Transition time (rise and fall)	t_T	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	15	10K	20	10K	ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	8		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		15		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64		64	ms	
Refresh period (L-ver)	t_{REF}		128		128		128		128	ms	
Refresh period (SL-ver)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CAS}$ address to $\overline{W}$ delay time	t_{CPWD}	53		60		70		75		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Hyper Page cycle time	t_{HPC}	20		24		29		34		ns	17
Hyper Page read-modify-write cycle time	t_{HPRWC}	62		71		86		96		ns	17
$\overline{CAS}$ precharge time (Hyper Page Cycle)	t_{CP}	8		10		10		10		ns	
$\overline{RAS}$ pulse width(Hyper Page Cycle)	t_{RASP}	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		13		15		20		20	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	7,14
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	12
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	12
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	7,14,15
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	7,14
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width (LL-ver)	tRASS	100		100		100		100		μs	16
$\overline{RAS}$ precharge time (LL-ver)	tRPS	90		110		130		150		ns	16
$\overline{CAS}$ hold time (LL-ver)	tCHS	-50		-50		-50		-50		ns	16

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11,13
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5,13
Access time from column address	tAA		30		35		40		45	ns	3,11,13
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	13	10,000	15	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	43		50		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Hyper Page cycle time	tHPC	25		29		34		39		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	67		76		91		101		ns	17

TEST MODE CYCLE (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ pulse width (Hyper Page Cycle)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

TEST MODE DESCRIPTION

The KM48C2004A/AL/ALL/ASL is the CMOS DRAM organized 2,097,152 words by 8 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 2Mx8 DRAM can be tested as if it were a 1Mx8 DRAM.

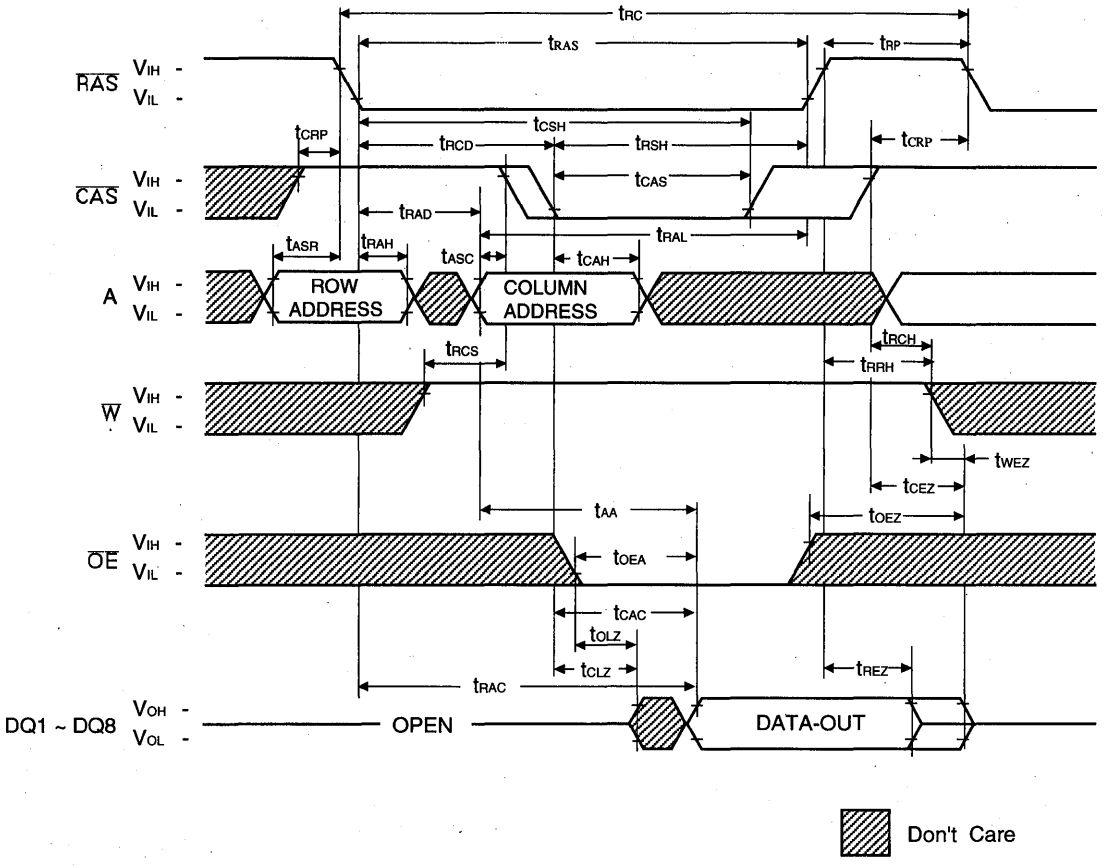
$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", and "$\overline{CAS}$ before $\overline{RAS}$ refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" peforms the refresh operation with internal CBR refresh address counter. The "test Mode" function reduces test time (1/2 in cases of N test pattern).

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) are assumed to be 5ns for all inputs, except tHPC and tHPRWC.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD ≥ tRCD (max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS ≥ tWCS(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD ≥ tCWD(min), tRWD ≥ tRWD(min) and tAWD ≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. tCEZ(max), tOEZ(max) tREZ(max) and tWEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going
17. tASC ≧ tCP(min), Assumn tT=2.0ns

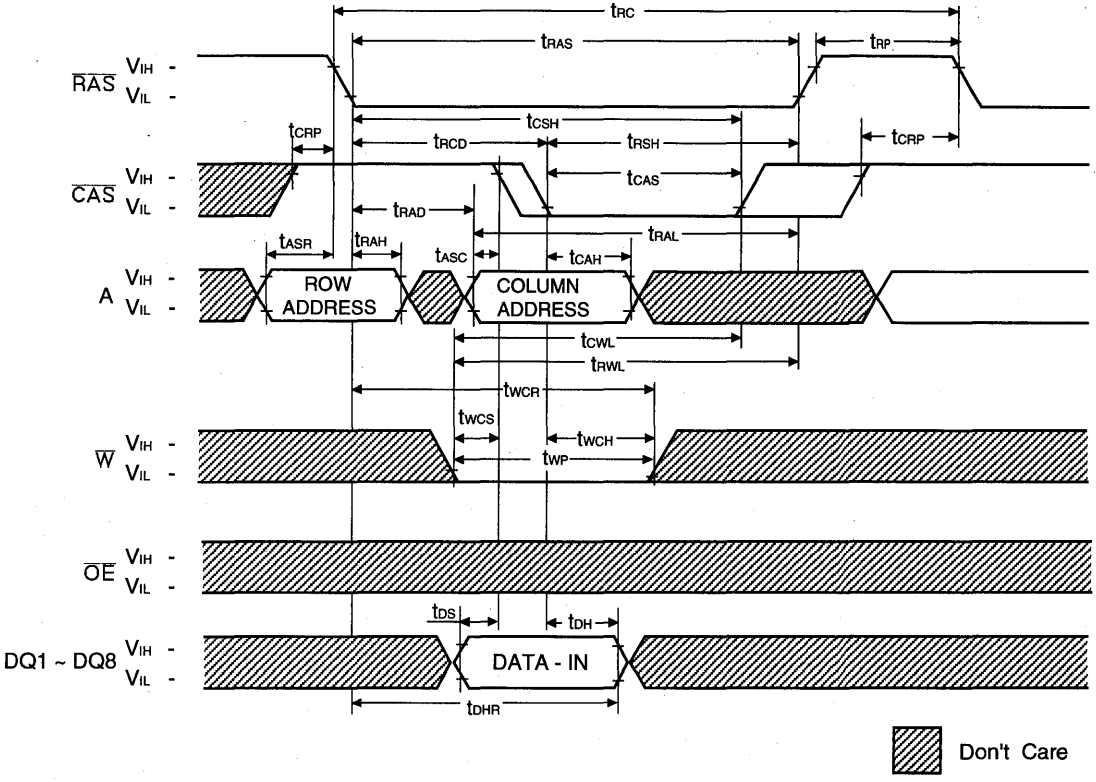
TIMING DIAGRAM

READ CYCLE



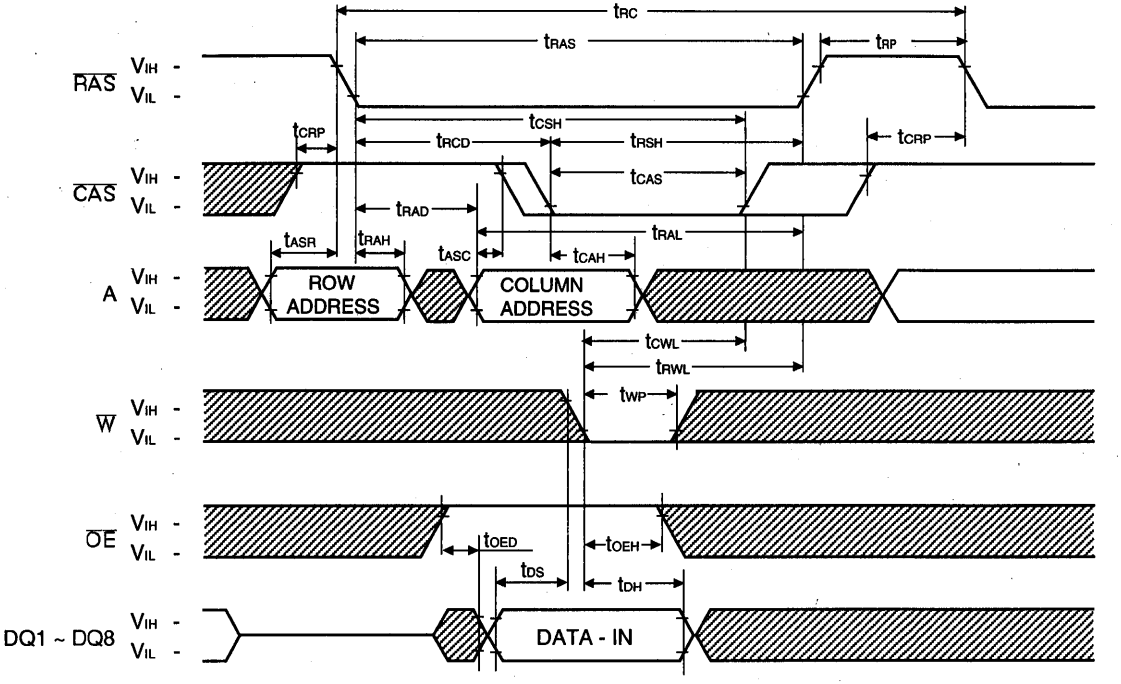
WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



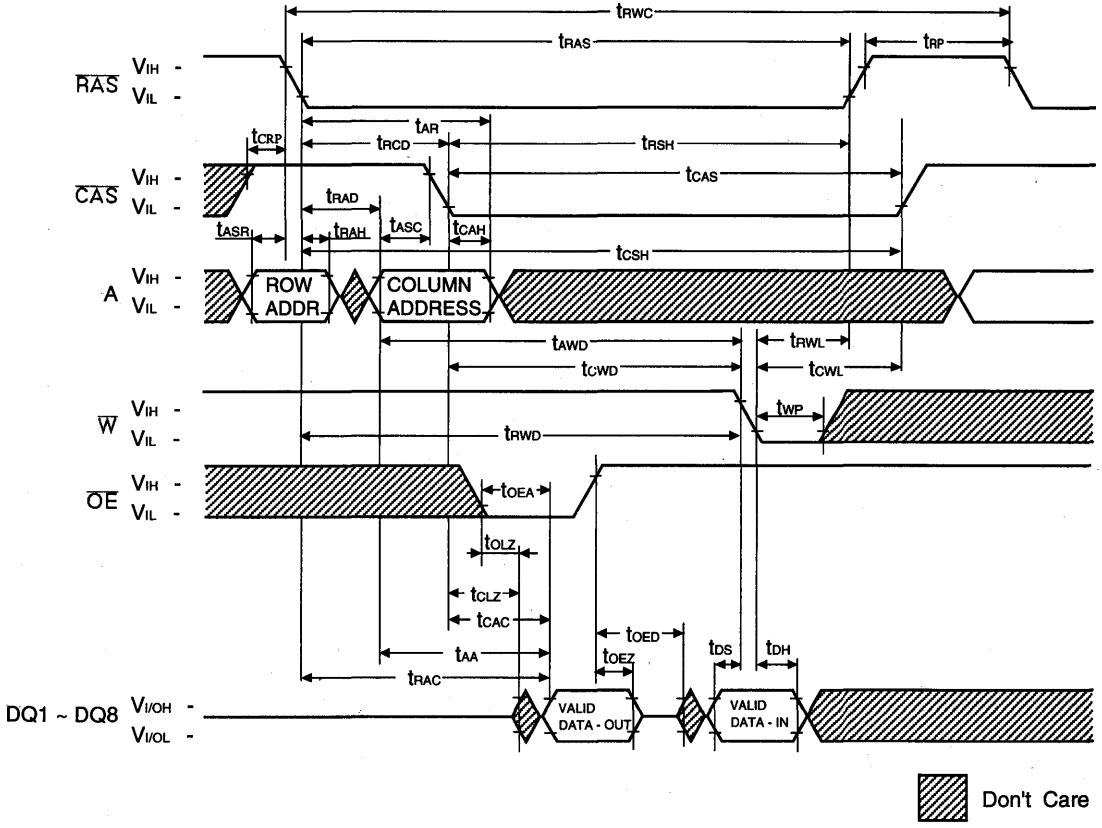
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



Don't Care

READ - MODIFY - WRITE CYCLE



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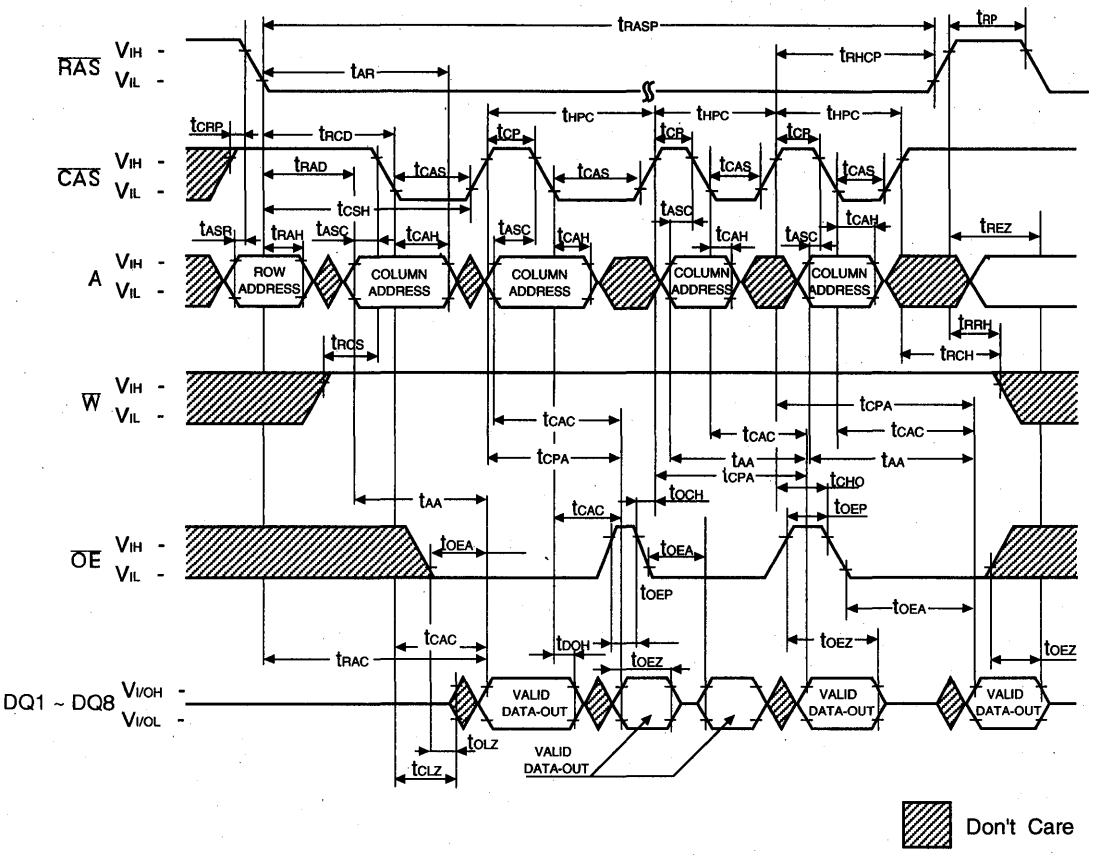
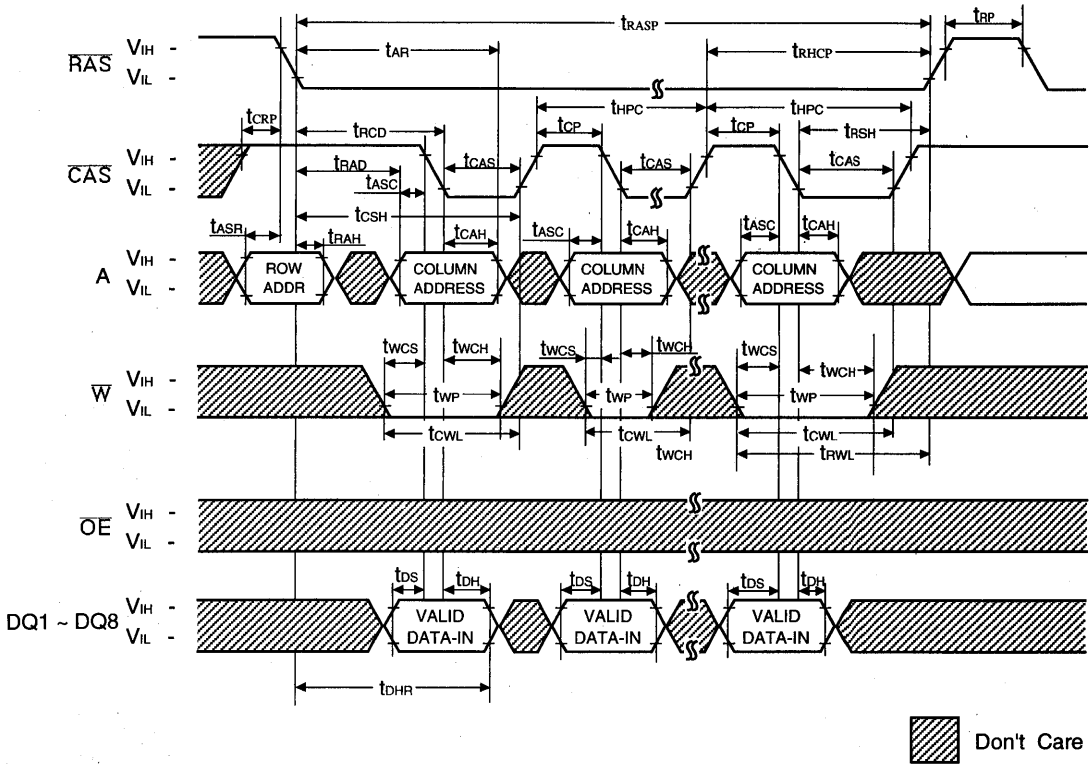
HYPER PAGE READ CYCLE



HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



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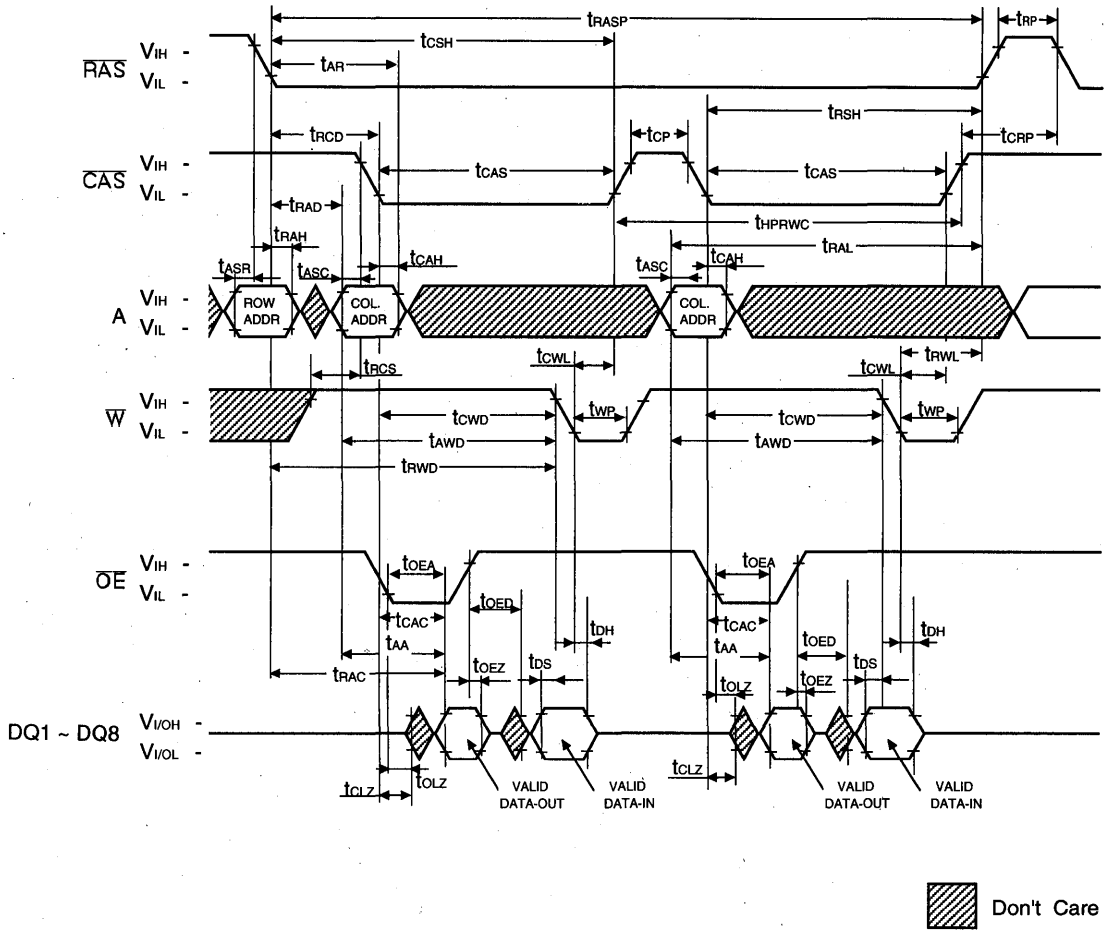
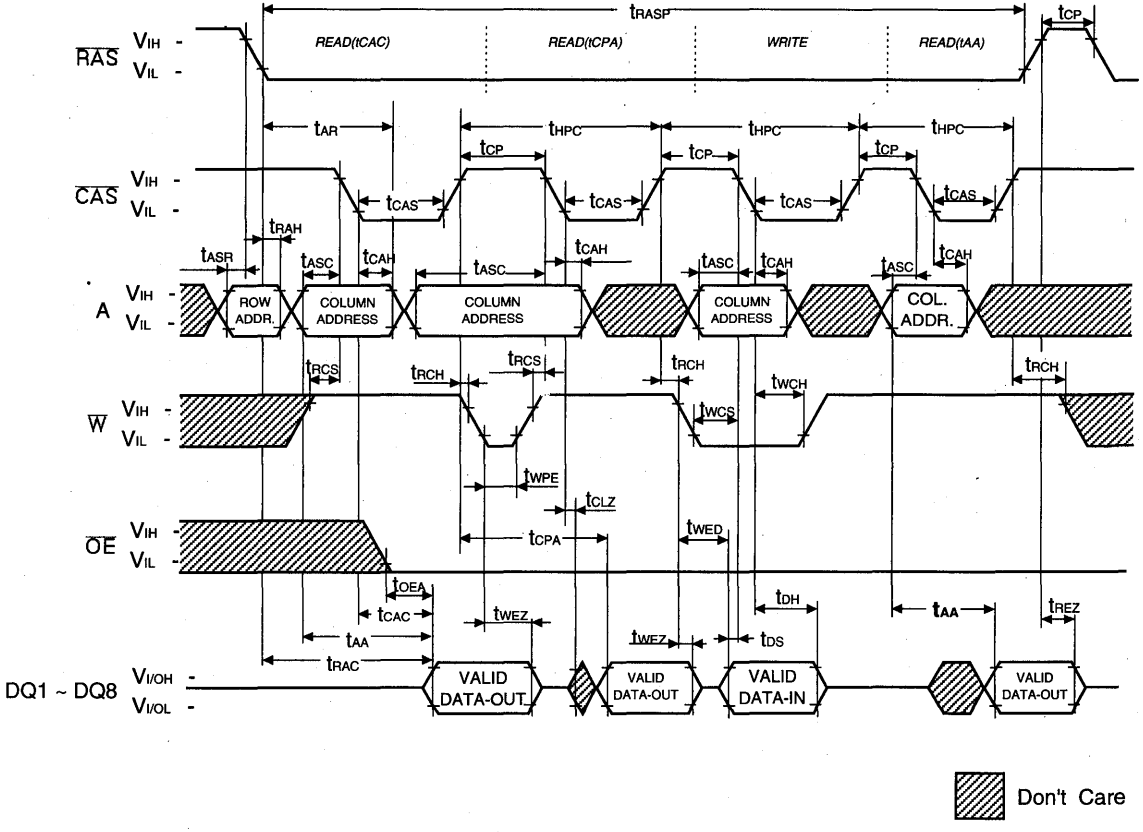
SAMSUNG ELECTRONICS

HYPER PAGE READ-MODIFY-WRITE CYCLE

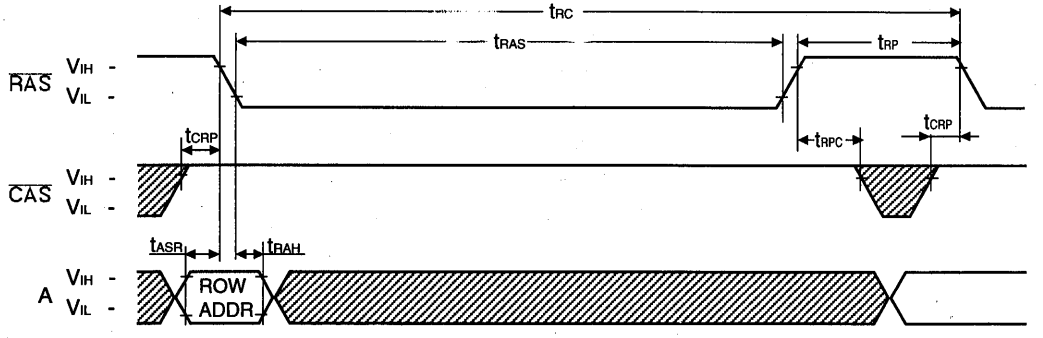


HYPER PAGE READ AND WRITE MIXED CYCLE



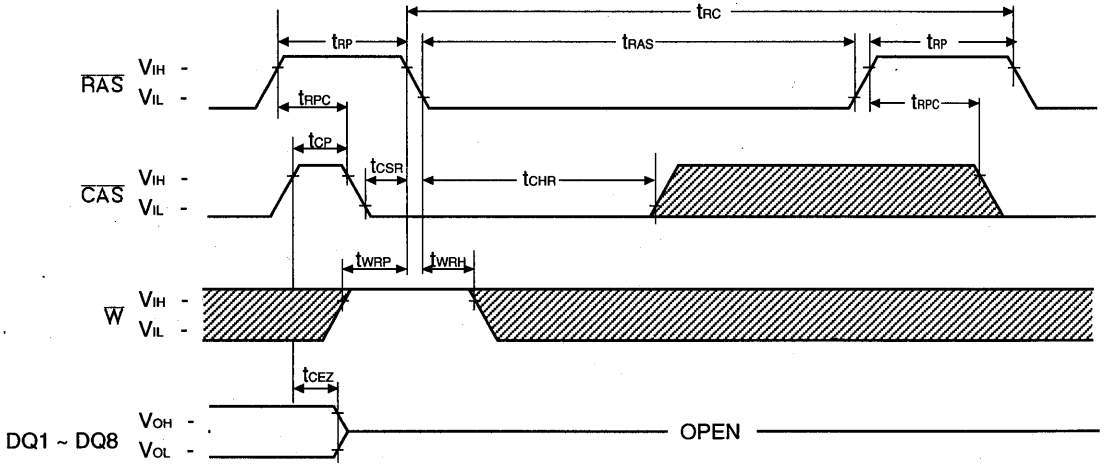
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



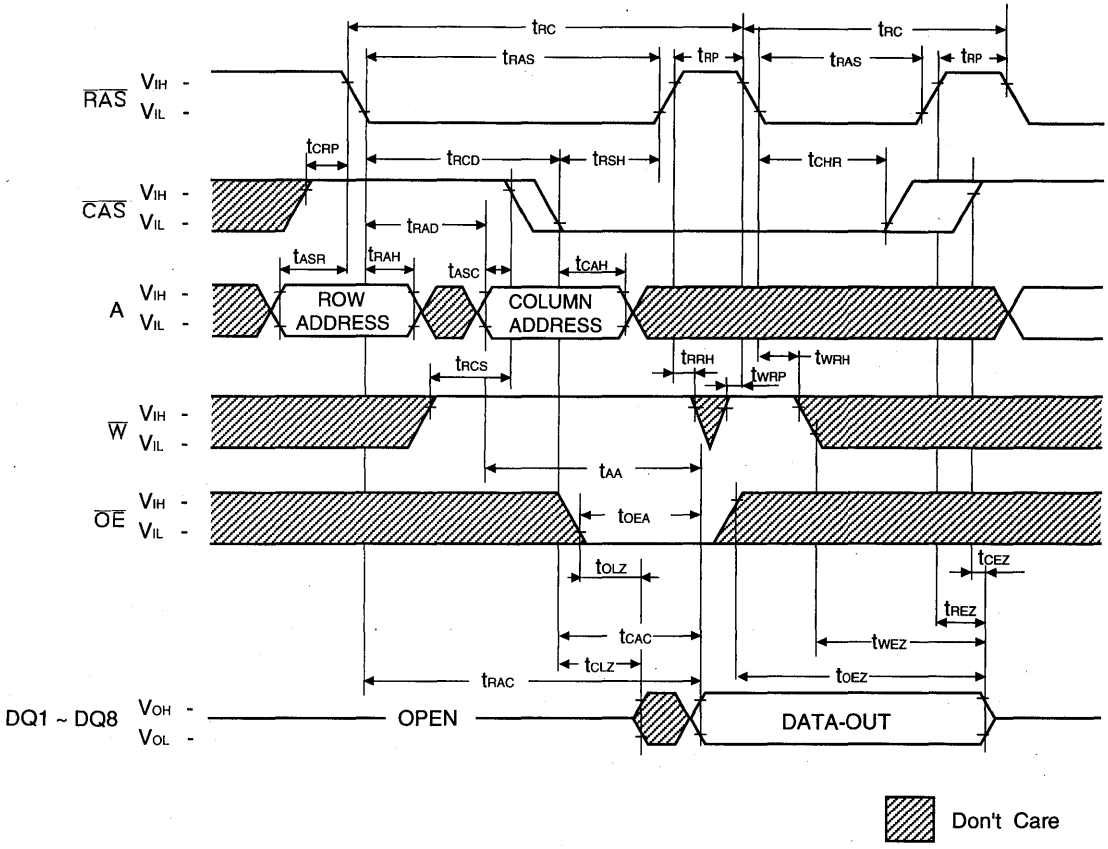
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



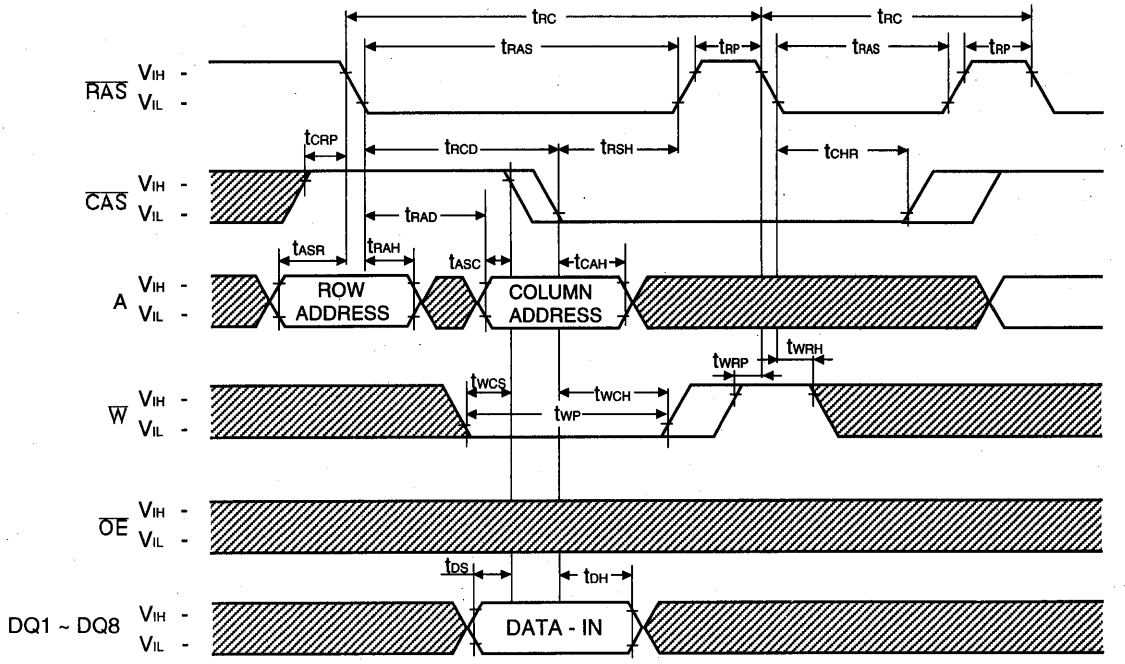
Don't Care

HIDDEN REFRESH CYCLE (READ)



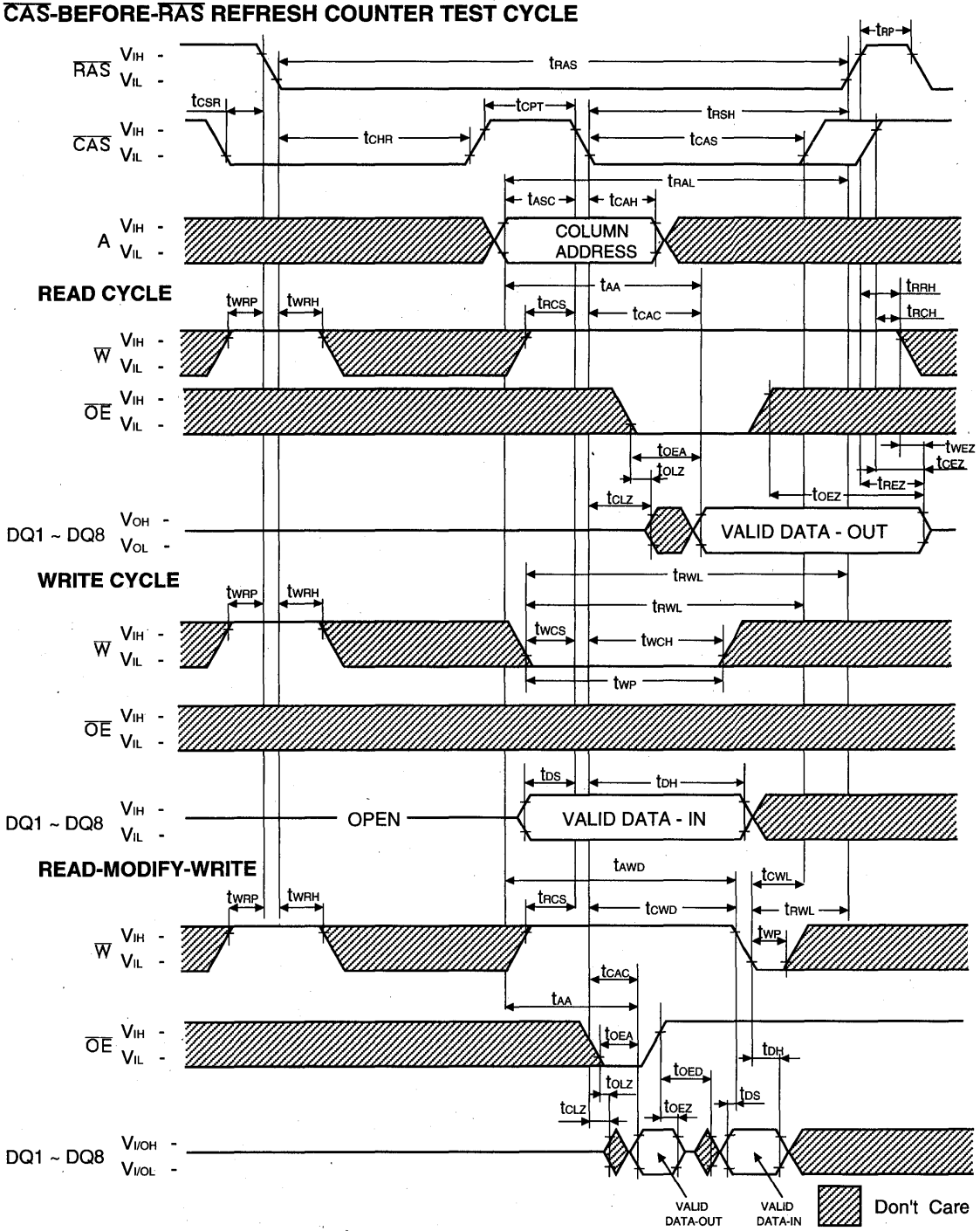
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



Don't Care

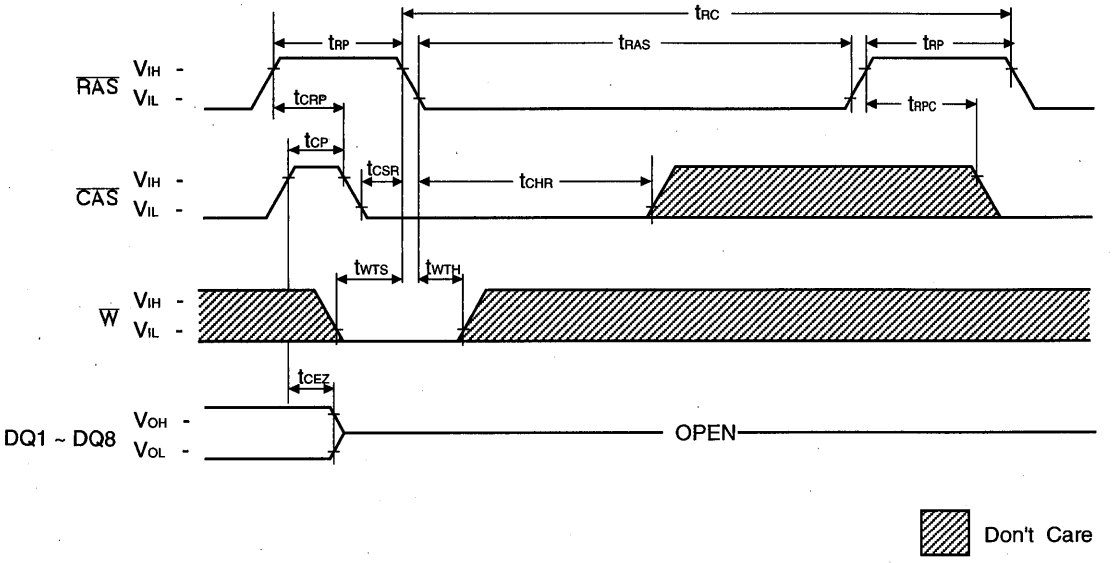
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



SAMSUNG ELECTRONICS

TEST MODE IN CYCLE

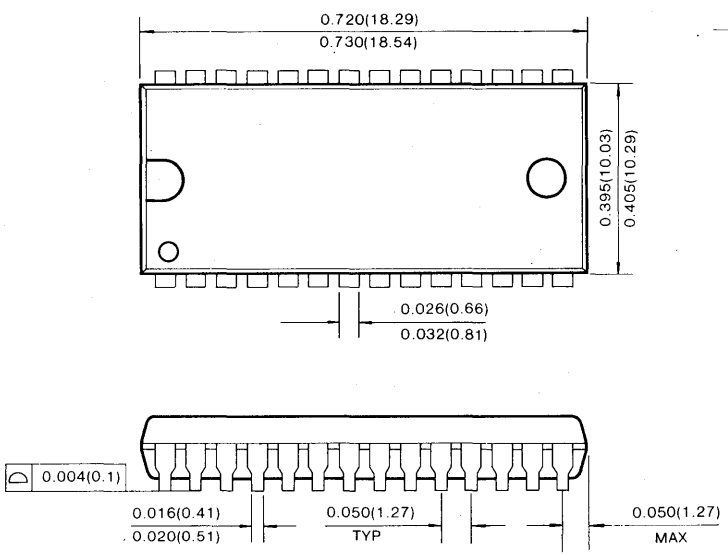
NOTE : $\overline{OE}$, A = Don't Care



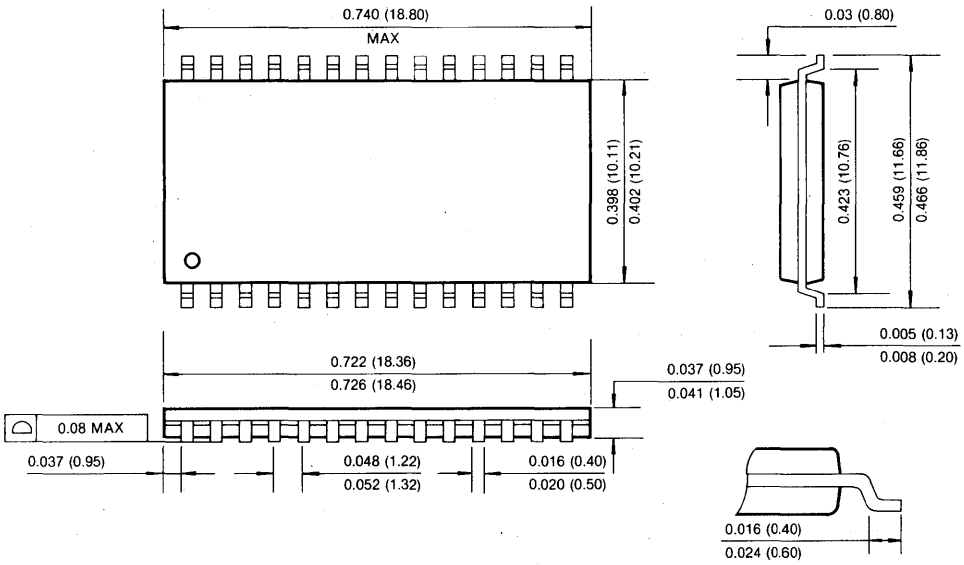
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



2M×8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
KM48C2104A/AL/ALL/ASL-5	50ns	13ns	90ns	20ns
KM48C2104A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM48C2104A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM48C2104A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- **Fast Page Mode with Extended data out**
- **Self Refresh Operation (LL-ver. only)**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single +5.0V±10% power supply**
- **2048 cycles/32ms refresh (Normal)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

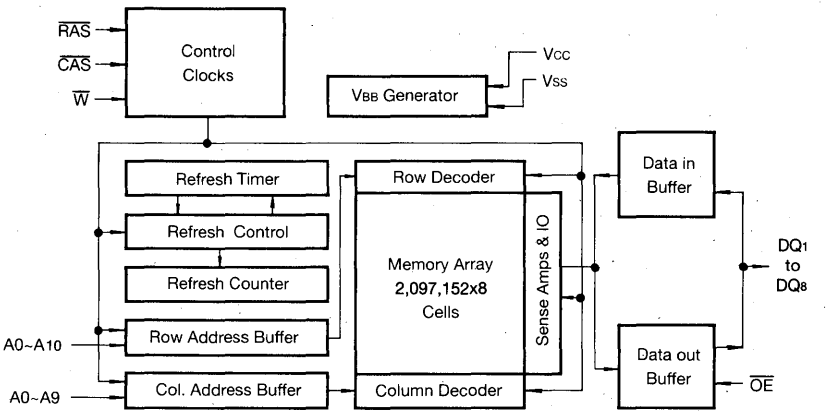
The Samsung KM48C2104A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit×8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48C2104A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48C2104A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

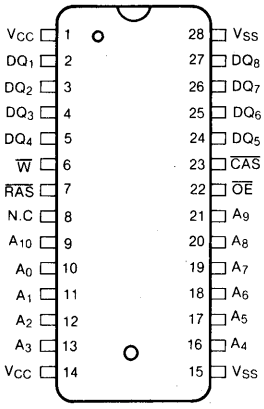
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

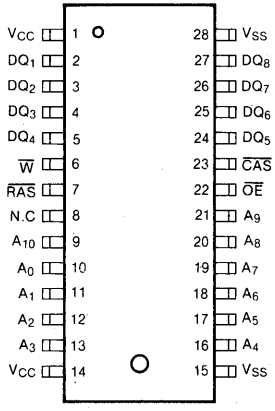
PIN CONFIGURATION (Top Views)

• KM48C2104 AJ/ALJ/ALLJ/ASLJ



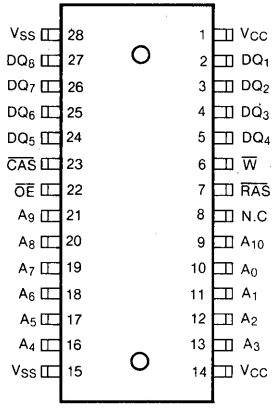
J : 400MIL

• KM48C2104 AT/ALT/ALLT/ASLT



T : 400MIL(Forward)

• KM48C2104 ATR/ALTR/ALLTR/ASLTR



TR : 400MIL(Reverse)

Pin Name	Pin Function
A0-A10	Address Inputs
DQ1~8	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{OE}$	Data Output Enable
Vcc	Power(+5.0V)
N.C	No Connection

6

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48C2104A/AL/ALL/ASL-5	I_{CC1}	-	110	mA
	KM48C2104A/AL/ALL/ASL-6			100	mA
	KM48C2104A/AL/ALL/ASL-7			90	mA
	KM48C2104A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48C2104A	I_{CC2}	-	2	mA
	KM48C2104AL			1	mA
	KM48C2104ALL			1	mA
	KM48C2104ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM48C2104A/AL/ALL/ASL-5	I_{CC3}	-	110	mA
	KM48C2104A/AL/ALL/ASL-6			100	mA
	KM48C2104A/AL/ALL/ASL-7			90	mA
	KM48C2104A/AL/ALL/ASL-8			80	mA
Hyper Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM48C2104A/AL/ALL/ASL-5	I_{CC4}	-	110	mA
	KM48C2104A/AL/ALL/ASL-6			100	mA
	KM48C2104A/AL/ALL/ASL-7			90	mA
	KM48C2104A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM48C2104A	I_{CC5}	-	1	mA
	KM48C2104AL			300	μA
	KM48C2104ALL			200	μA
	KM48C2104ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48C2104A/AL/ALL/ASL-5	I_{CC6}	-	110	mA
	KM48C2104A/AL/ALL/ASL-6			100	mA
	KM48C2104A/AL/ALL/ASL-7			90	mA
	KM48C2104A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V, DQ1~DQ8=Don't Care t_{RC}=62.5μs(L-Ver.) 125μs(SL-Ver.), t_{RAS}=t_{RAS} min~300ns	KM48C2104AL	I_{CC7}	-	400	μA
	KM48C2104ASL			300	μA

SAMSUNG ELECTRONICS

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{10}=V_{CC}-0.2V or 0.2V DQ_1-DQ_8=V_{CC}-0.2V, 0.2V or Open	KM48C2104ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{10})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, V_{CC}=5.0V±0.5V, See notes 1,2)

Test condition: V_{ih}/V_{il}=2.4V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		3		3		ns	3
Output buffer turn-off delay	t_{CEZ}	3	13	3	15	3	20	3	20	ns	7,14,15
Transition time (rise and fall)	t_T	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	15	10K	20	10K	ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		32		32		32		32	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Refresh period (SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{CAS}$ address to $\overline{W}$ delay time	tCPWD	53		60		70		75		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		24		29		34		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	62		71		86		96		ns	17
$\overline{CAS}$ precharge time (Hyper Page Cycle)	tCP	8		10		10		10		ns	
$\overline{RAS}$ pulse width(Hyper Page Cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	7,14
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	12
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	12
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAs}$	tREZ	3	13	3	15	3	20	3	20	ns	7,14,15
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	7,14
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width (LL-ver)	tRASS	100		100		100		100		μs	16
$\overline{RAS}$ precharge time (LL-ver)	tRPS	90		110		130		150		ns	16
$\overline{CAS}$ hold time (LL-ver)	tCHS	-50		-50		-50		-50		ns	16

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11,13
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5,13
Access time from column address	tAA		30		35		40		45	ns	3,11,13
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	13	10,000	15	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	43		50		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Hyper Page cycle time	tHPC	25		29		34		39		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	67		76		91		101		ns	17

TEST MODE CYCLE (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ pulse width (Hyper Page Cycle)	t_{RASP}	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45		50	ns	3
$\overline{OE}$ access time	t_{OEA}		18		20		25		25	ns	
$\overline{OE}$ to data delay	t_{OED}	18		20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	18		20		25		25		ns	

TEST MODE DESCRIPTION

The KM48C2104A/AL/ALL/ASL is the CMOS DRAM organized 2,097,152 words by 8 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 2Mx8 DRAM can be tested as if it were a 1Mx8 DRAM.

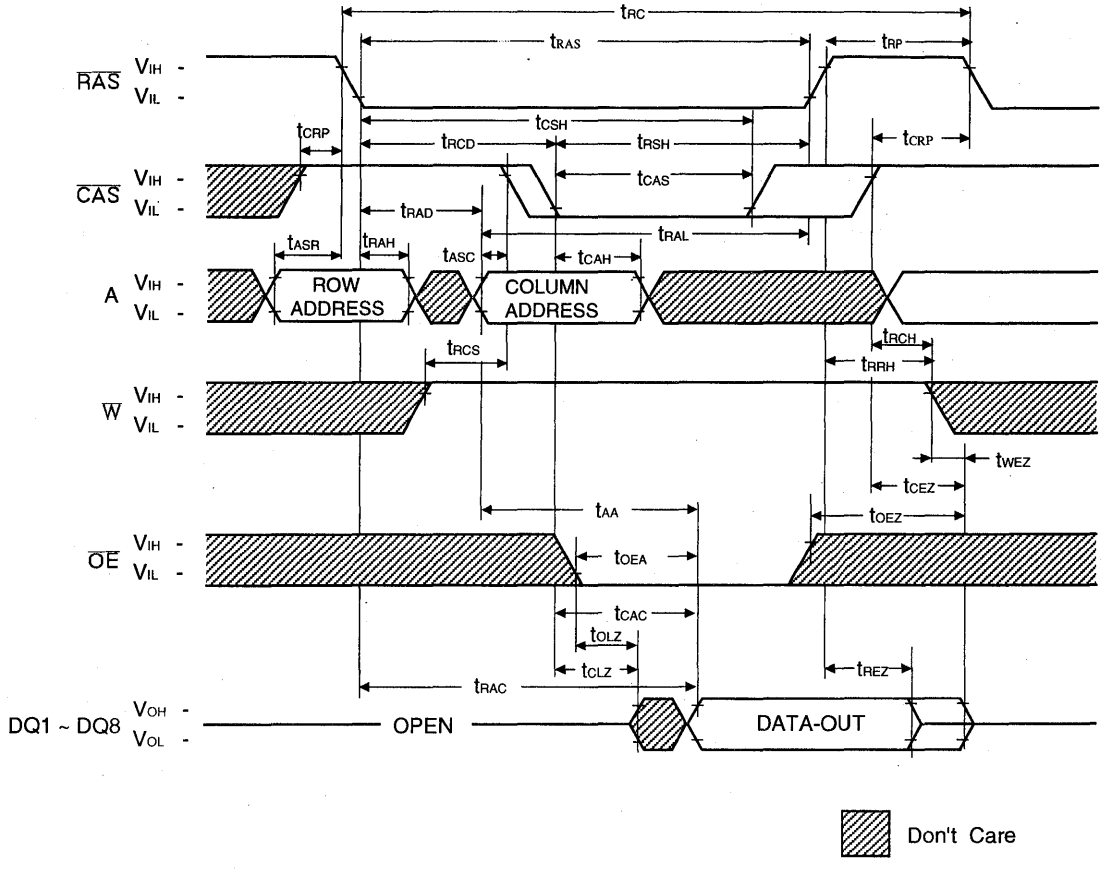
$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", And "$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" peforms the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs, without t_{HPC} and t_{HPRWC}.
3. Measured with a load equivalent to 2TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{REZ}(max), t_{CEZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. If RAS goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going
17. $t_{ASC} \geq t_{CP}$min, Assumn t_T=2.0ns

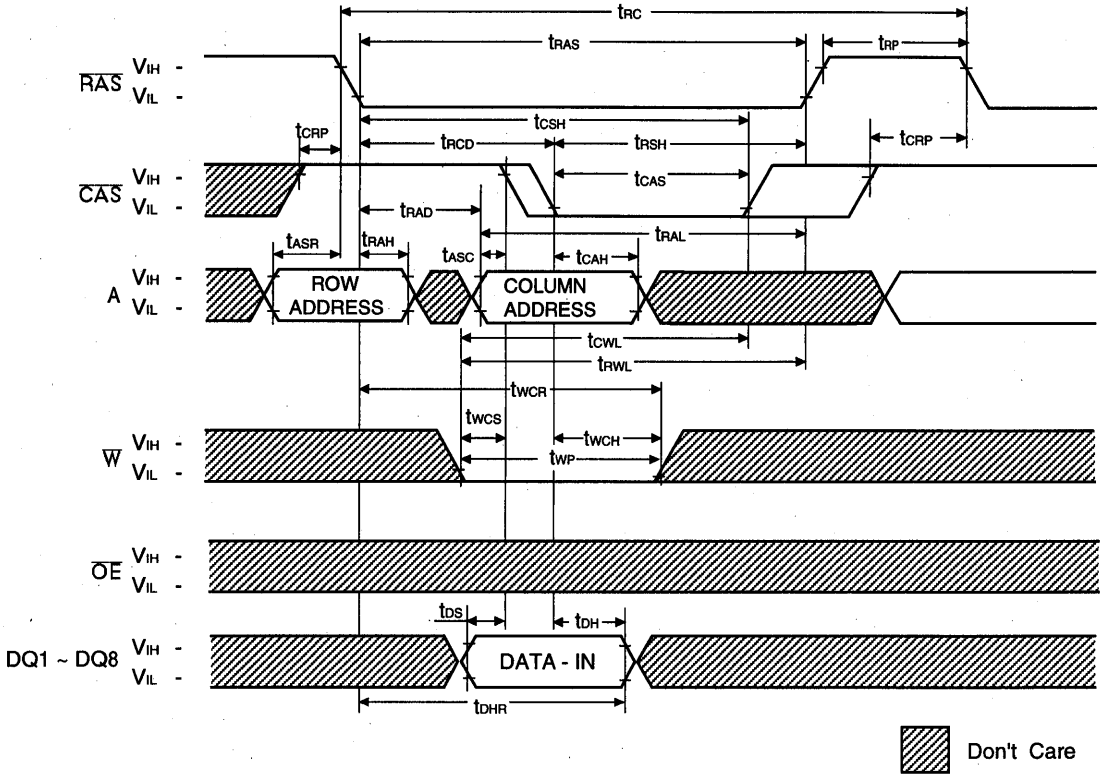
TIMING DIAGRAM

READ CYCLE



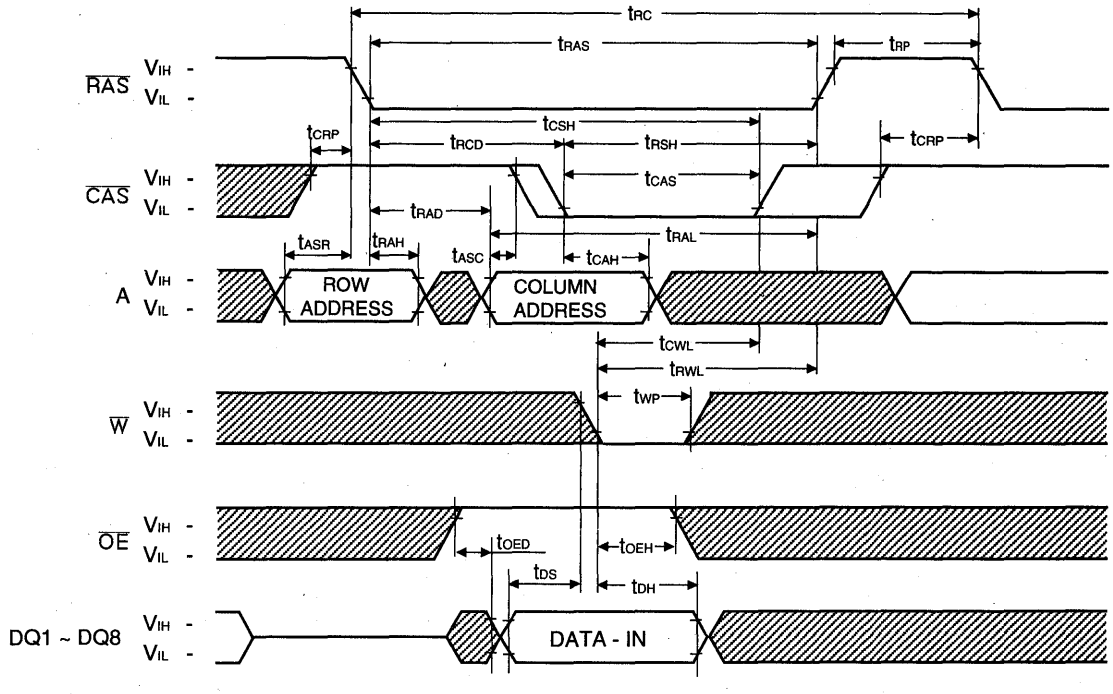
WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



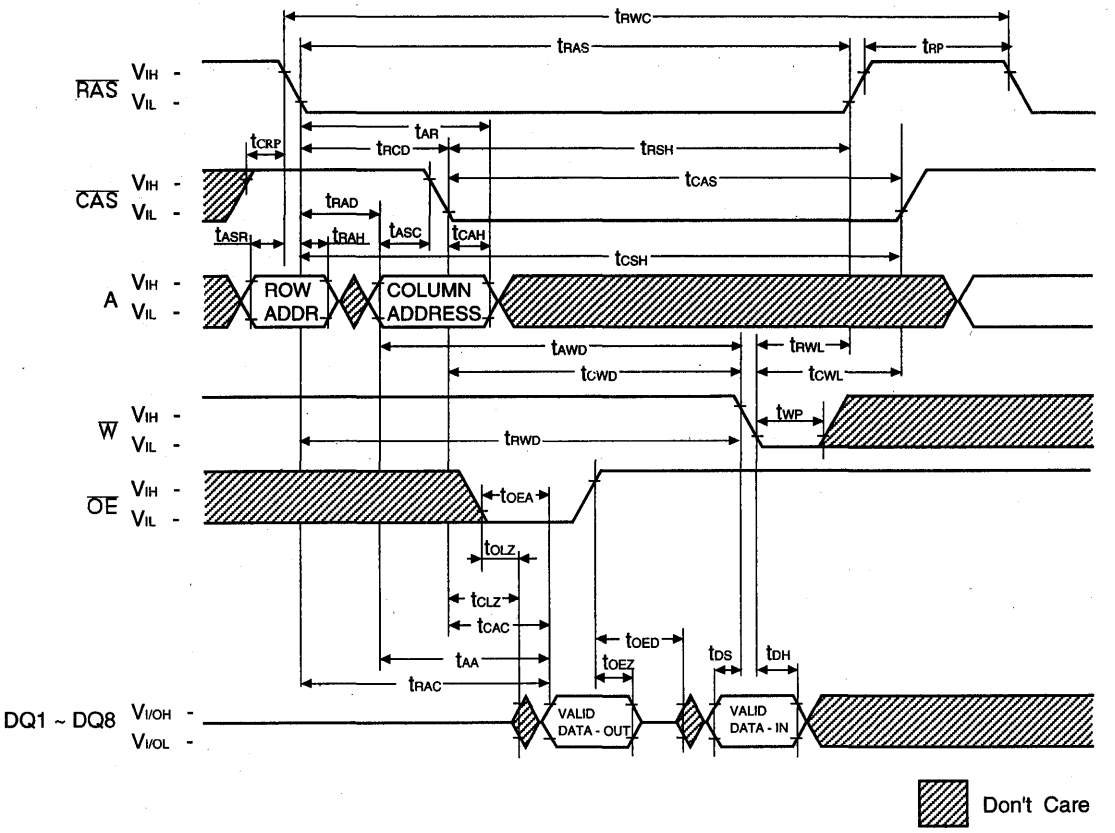
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

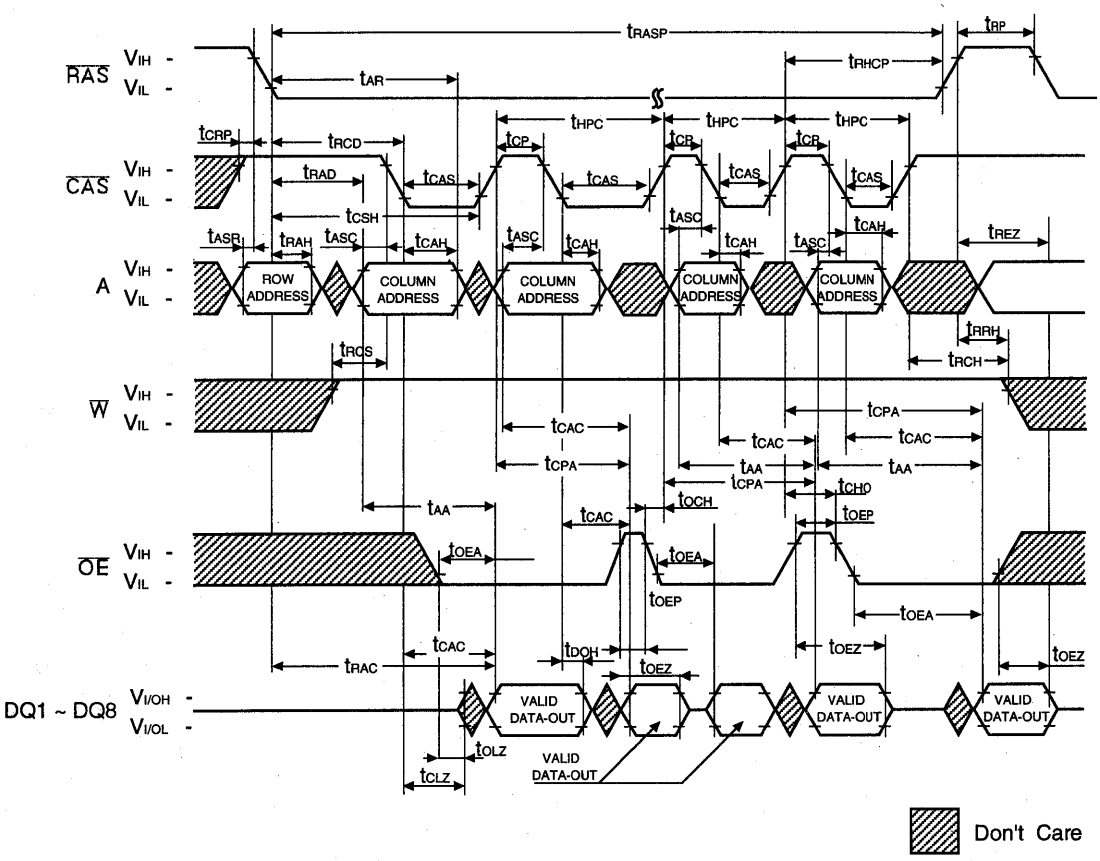


Don't Care

READ - MODIFY - WRITE CYCLE

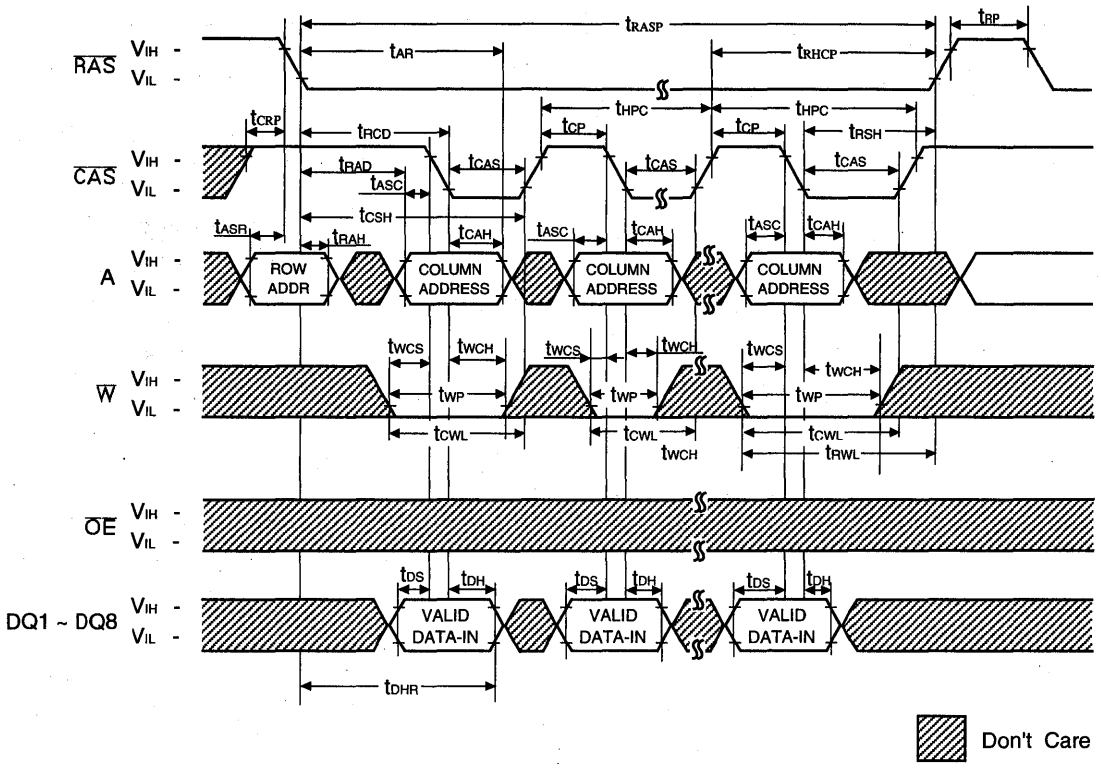


HYPER PAGE READ CYCLE

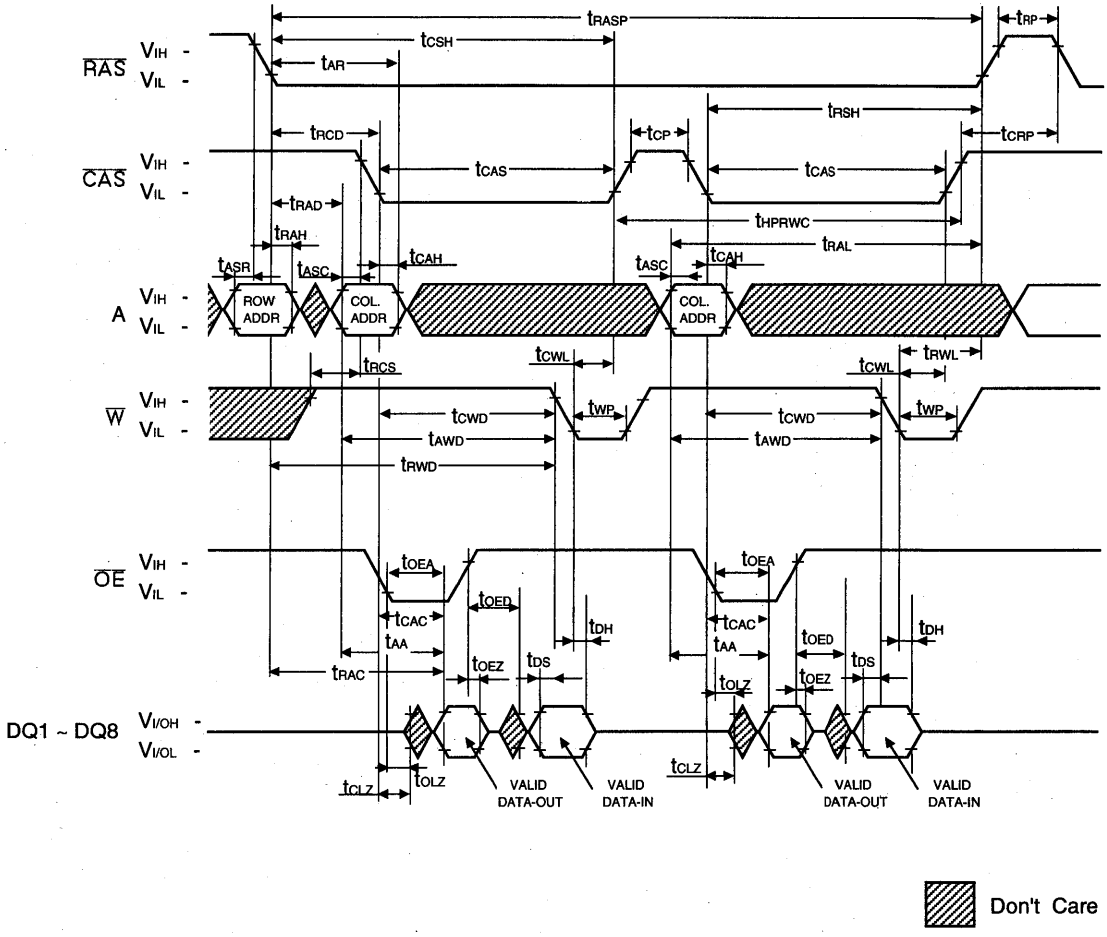


HYPER PAGE WRITE CYCLE (EARLY WRITE)

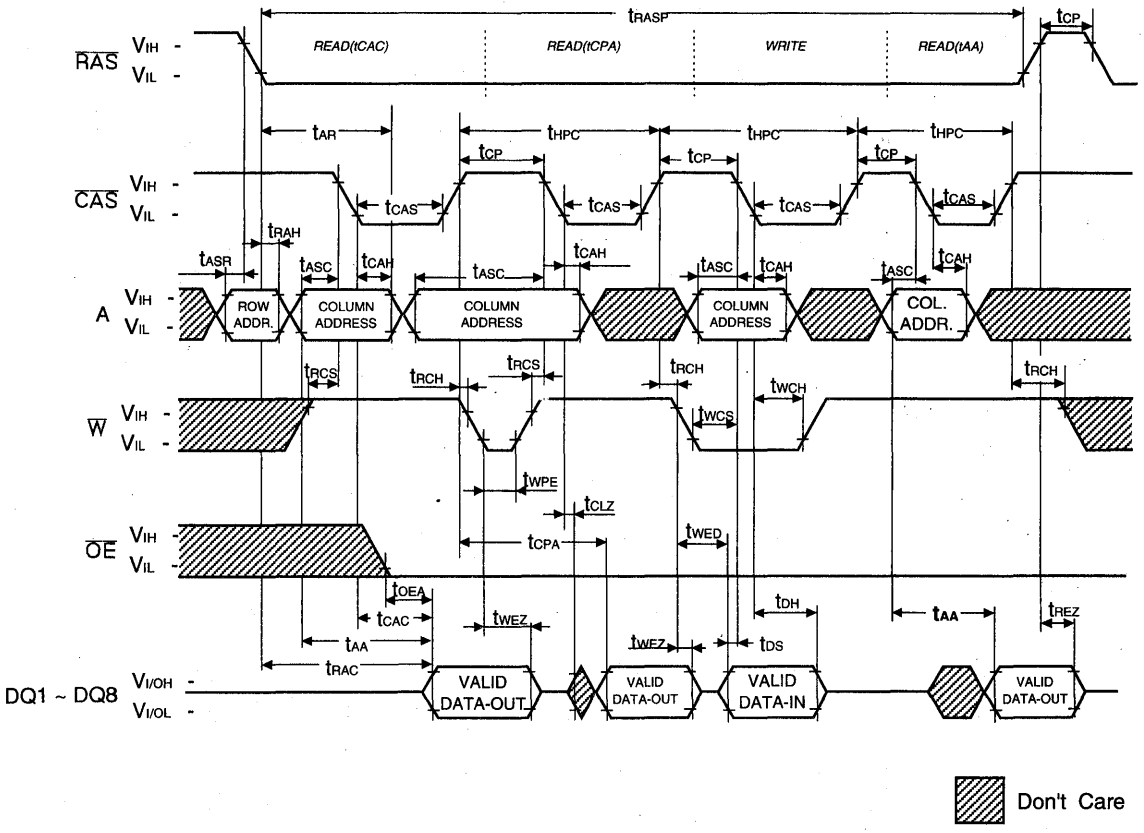
NOTE : D_{OUT} = Open



HYPER PAGE READ-MODIFY-WRITE CYCLE

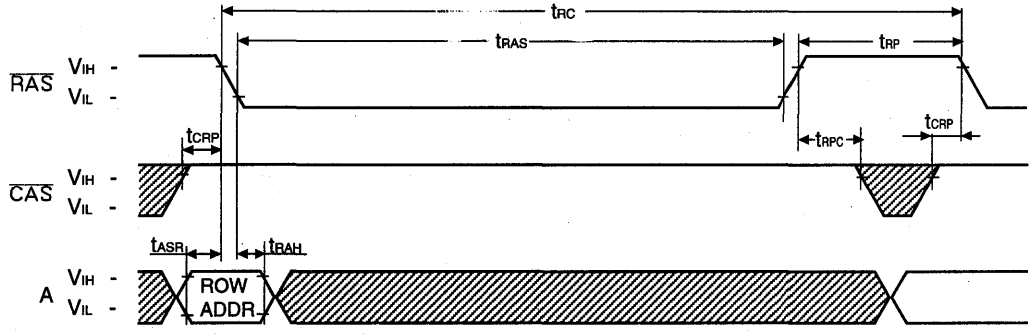


HYPER PAGE READ AND WRITE MIXED CYCLE



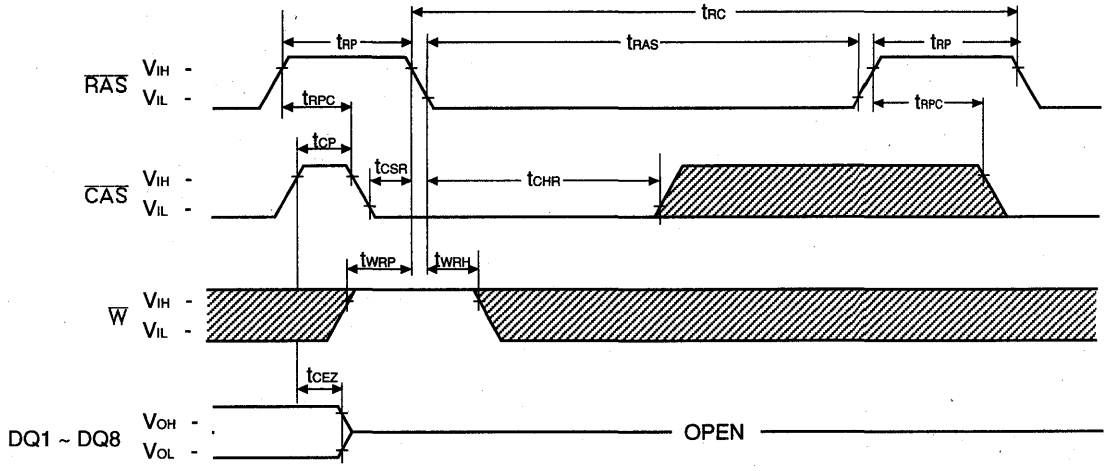
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

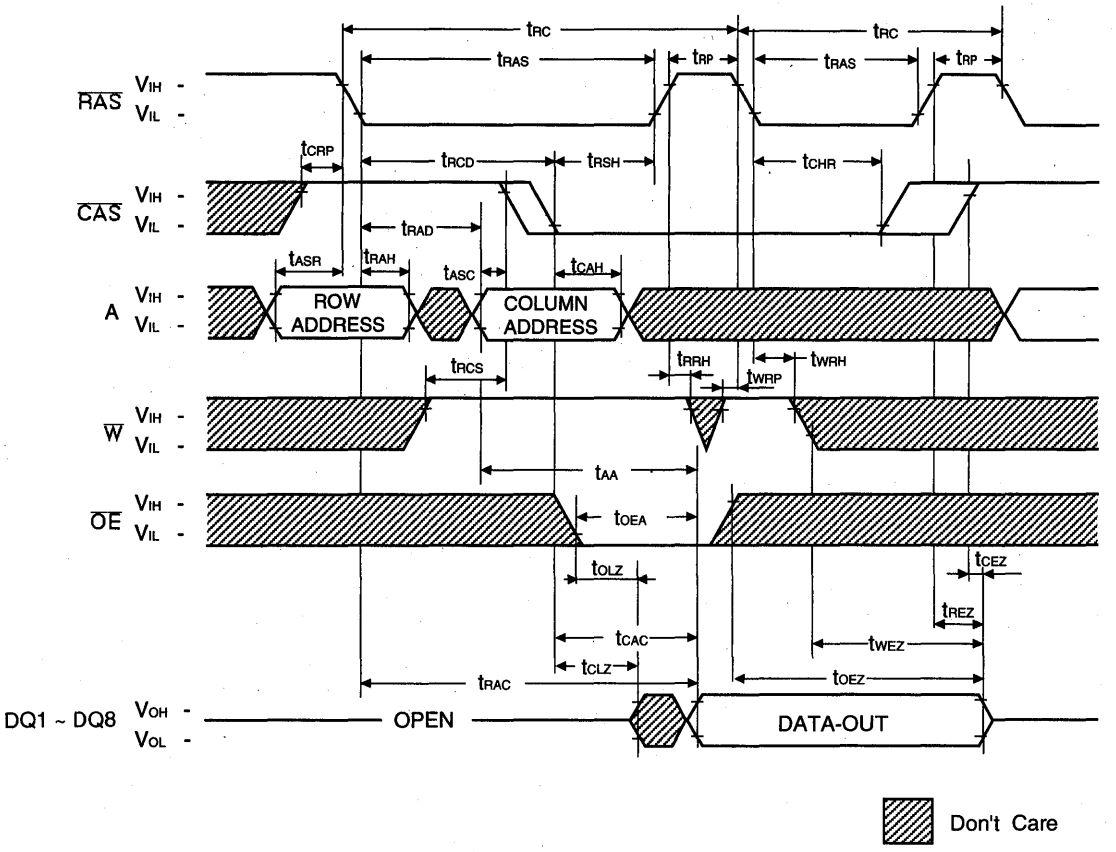
NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



Don't Care

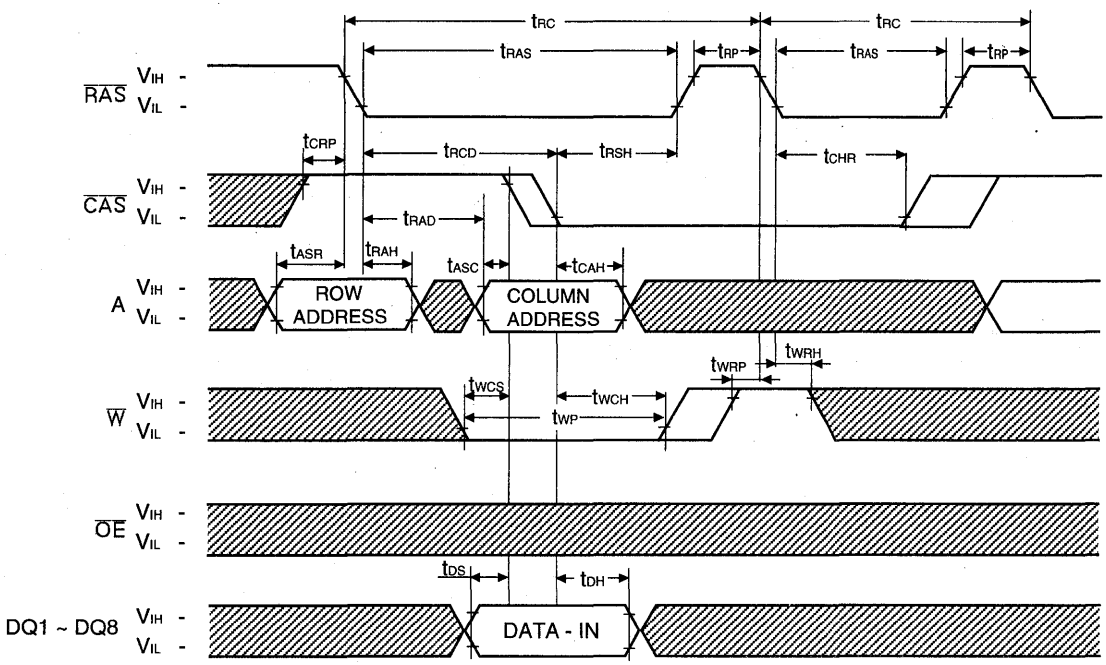
6

HIDDEN REFRESH CYCLE (READ)

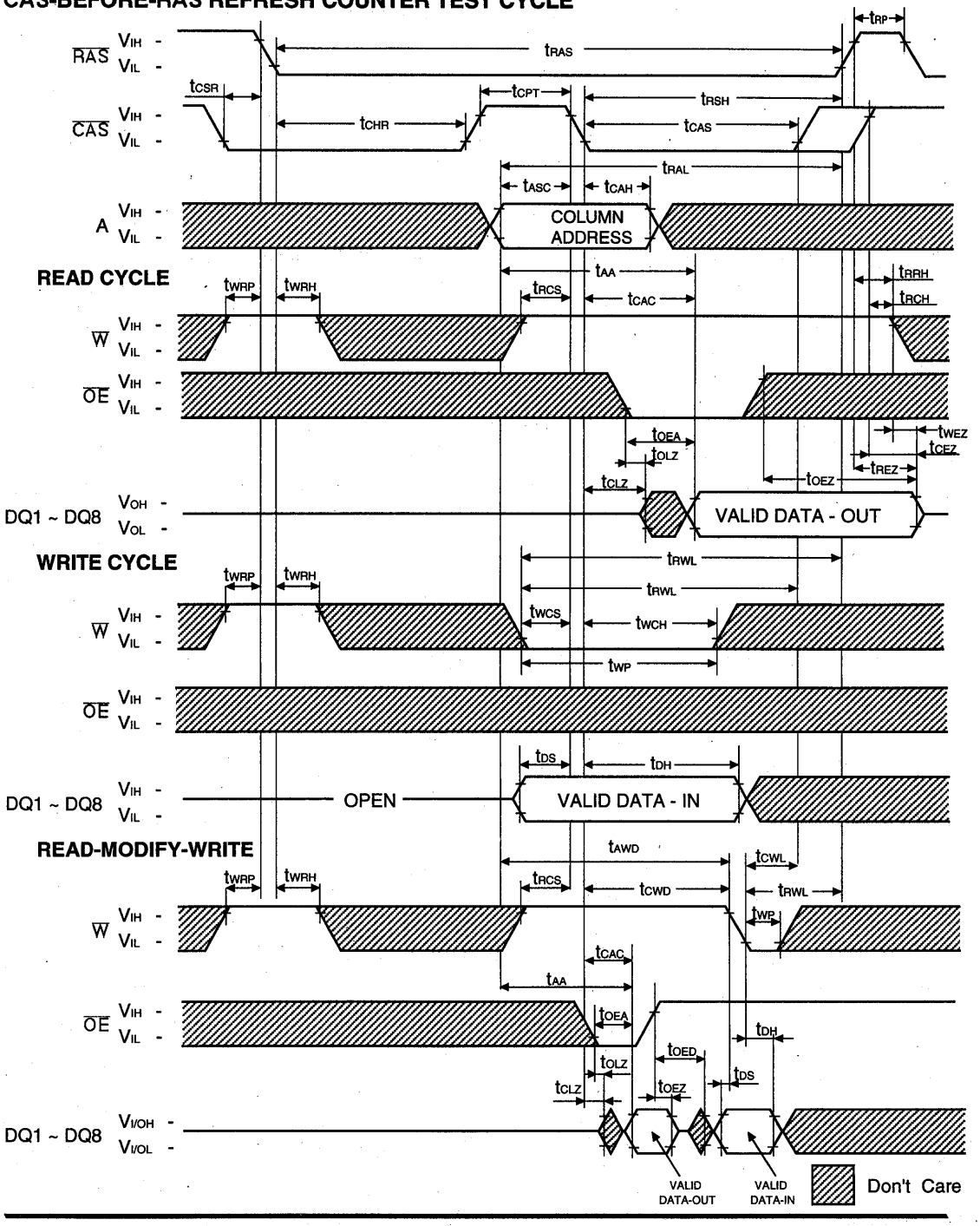


HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN

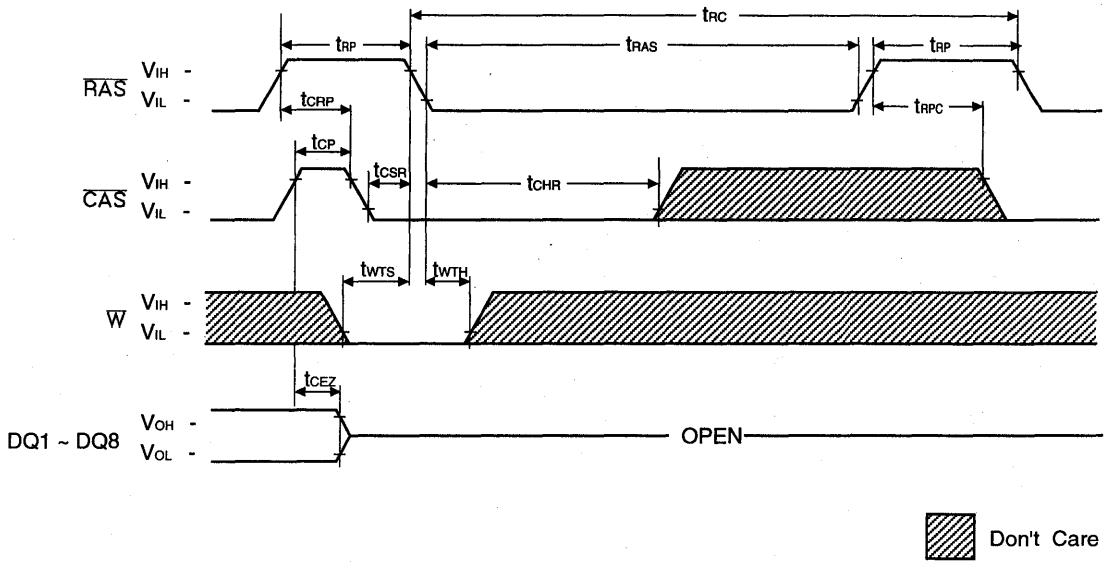


CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TEST MODE IN CYCLE

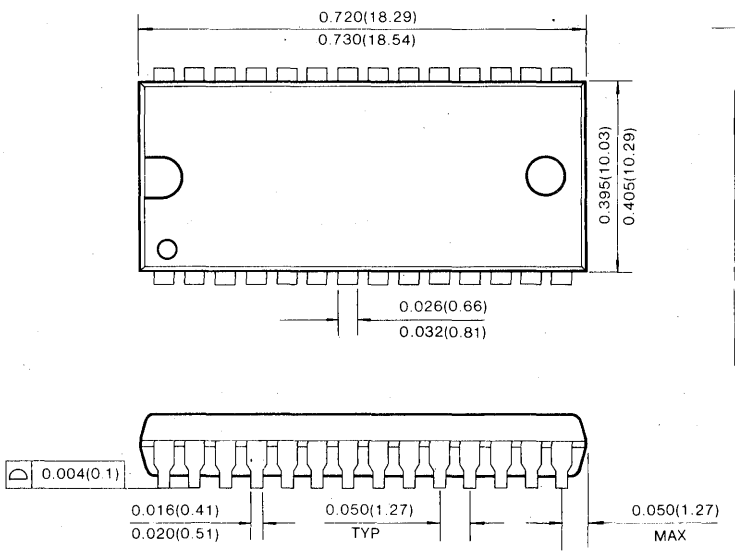
NOTE : $\overline{OE}$, A = Don't Care



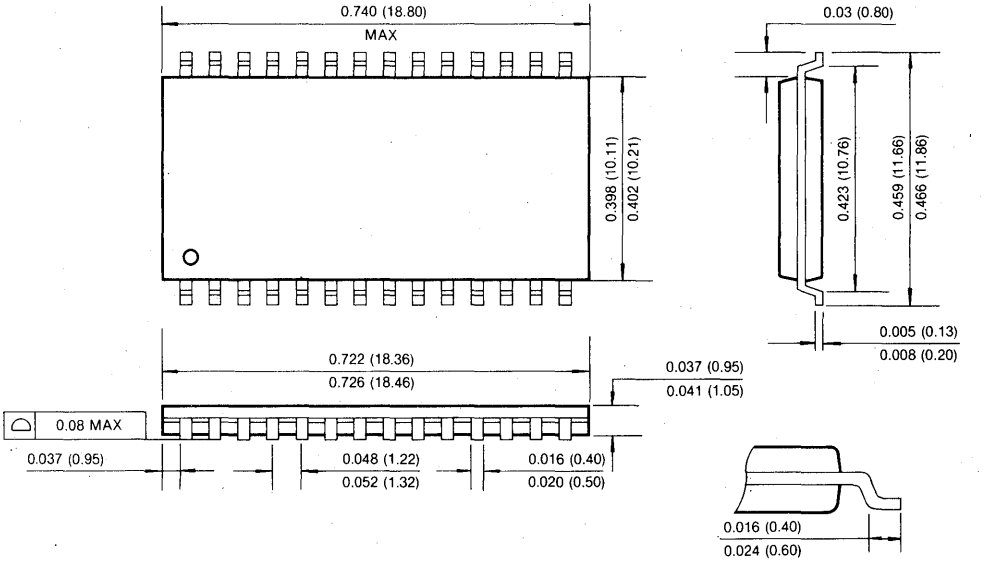
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



2M ×8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM48V2000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM48V2000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM48V2000A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Single+3.3V±0.3V power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

GENERAL DESCRIPTION

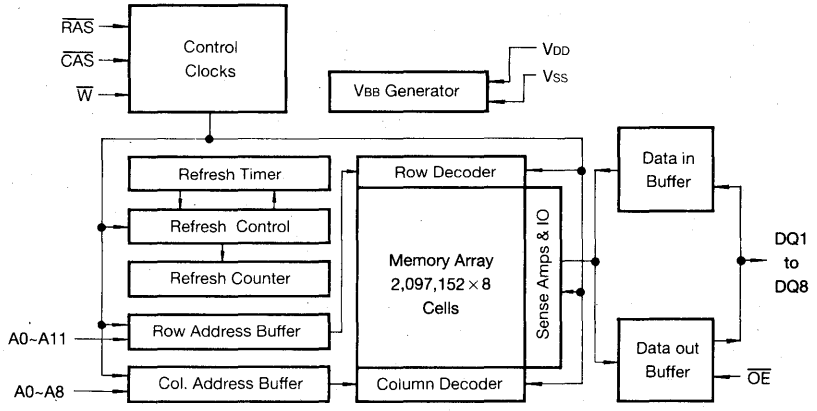
The Samsung KM48V2000A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48V2000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48V2000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

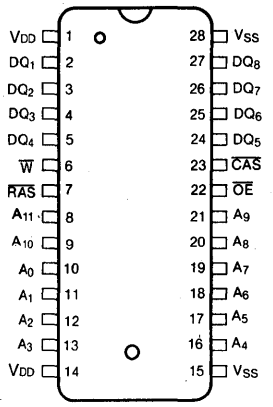
FUNCTIONAL BLOCK DIAGRAM



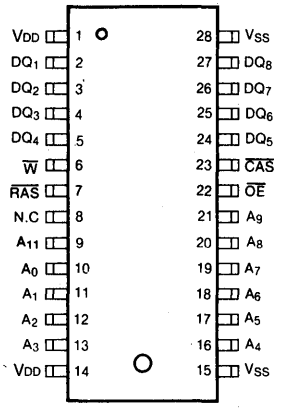
6

PIN CONFIGURATION (Top Views)

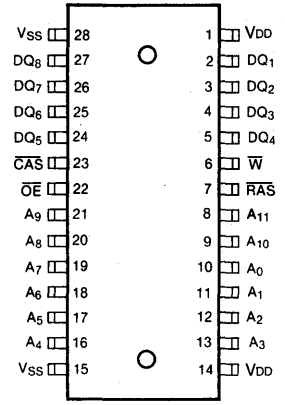
• KM48V2000 AJ/ALJ/ALLJ/ASLJ



• KM48V2000 AT/ALT/ALLT/ASLT



• KM48V2000 ATR/ALTR/ALLTR/ASLTR



Pin Name	Pin Function
A0-A11	Address Inputs
DQ1~8	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VDD	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 ~ 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48V2000A/AL/ALL/ASL-6 KM48V2000A/AL/ALL/ASL-7 KM48V2000A/AL/ALL/ASL-8	I_{CC1}	-	80 70 60	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48V2000A KM48V2000AL KM48V2000ALL KM48V2000ASL	I_{CC2}	-	2 1 1 1	mA mA mA mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM48V2000A/AL/ALL/ASL-6 KM48V2000A/AL/ALL/ASL-7 KM48V2000A/AL/ALL/ASL-8	I_{CC3}	-	80 70 60	mA mA mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM48V2000A/AL/ALL/ASL-6 KM48V2000A/AL/ALL/ASL-7 KM48V2000A/AL/ALL/ASL-8	I_{CC4}	-	70 60 50	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM48V2000A KM48V2000AL KM48V2000ALL KM48V2000ASL	I_{CC5}	-	1 300 200 200	mA μA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48V2000A/AL/ALL/ASL-6 KM48V2000A/AL/ALL/ASL-7 KM48V2000A/AL/ALL/ASL-8	I_{CC6}	-	80 70 60	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=31.25μS(L-Ver.) 62.5μS(SL-Ver.), T_{RAS}=T_{RAS} min.~300ms	KM48V2000AL KM48V2000ASL	I_{CC7}	-	450 350	μA μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{DD}-0.2V or 0.2V DQ_1~DQ_8=V_{DD}-0.2V, 0.2V or Open	KM48V2000ALL	I_{CC8}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Test Condition : V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ commend hold time	t_{OEH}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

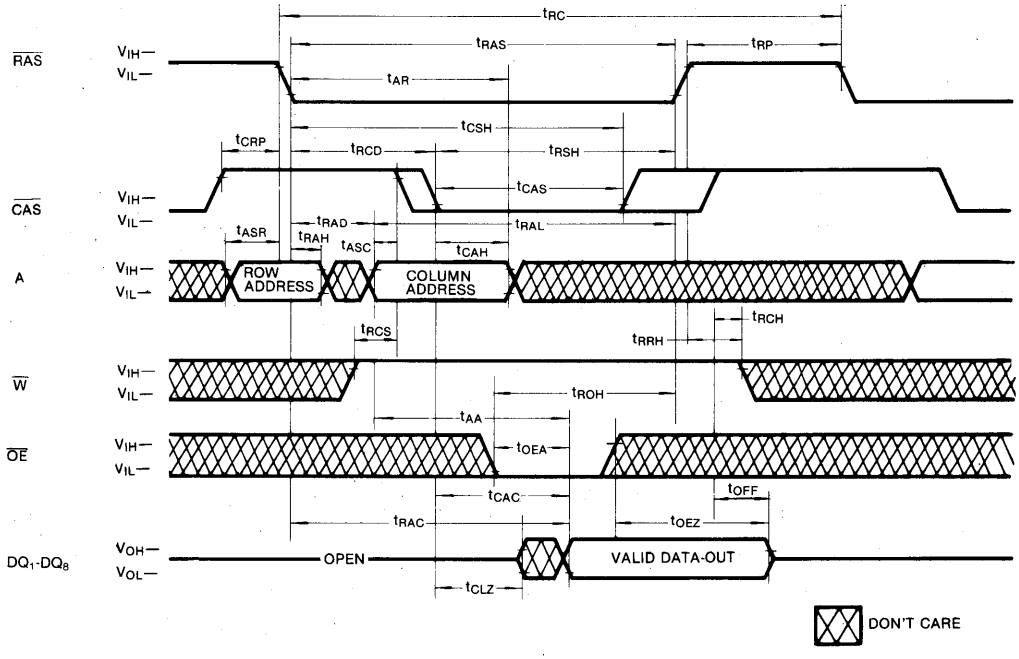
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Fast Page mode cycle time	tPC	45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 100pF and V_{oh}=2.0V(I_{OUT}=2mA), V_{ol}=0.8V(I_{OUT}=2mA)
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

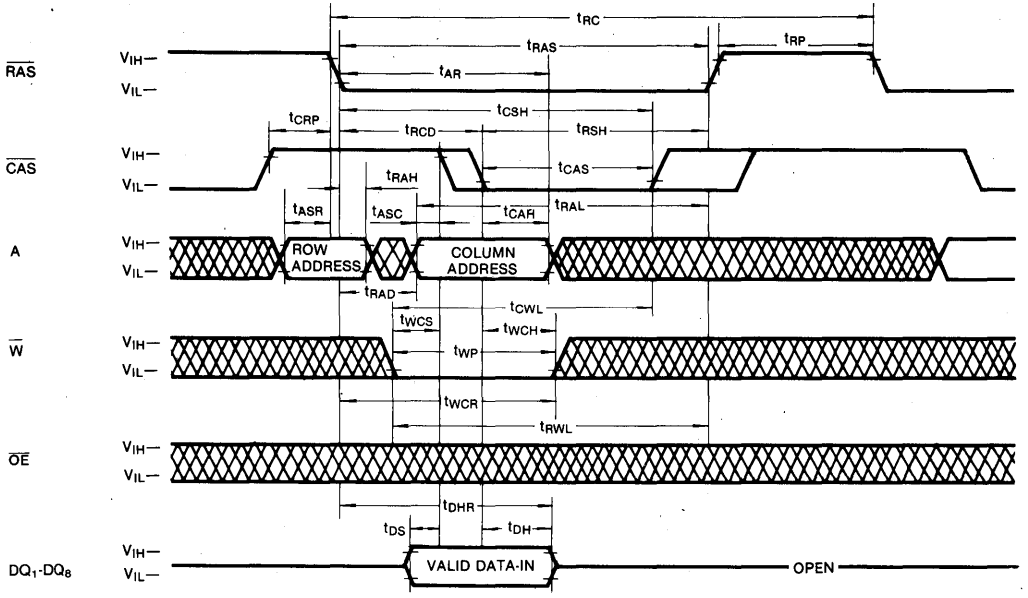
TIMING DIAGRAMS

READ CYCLE

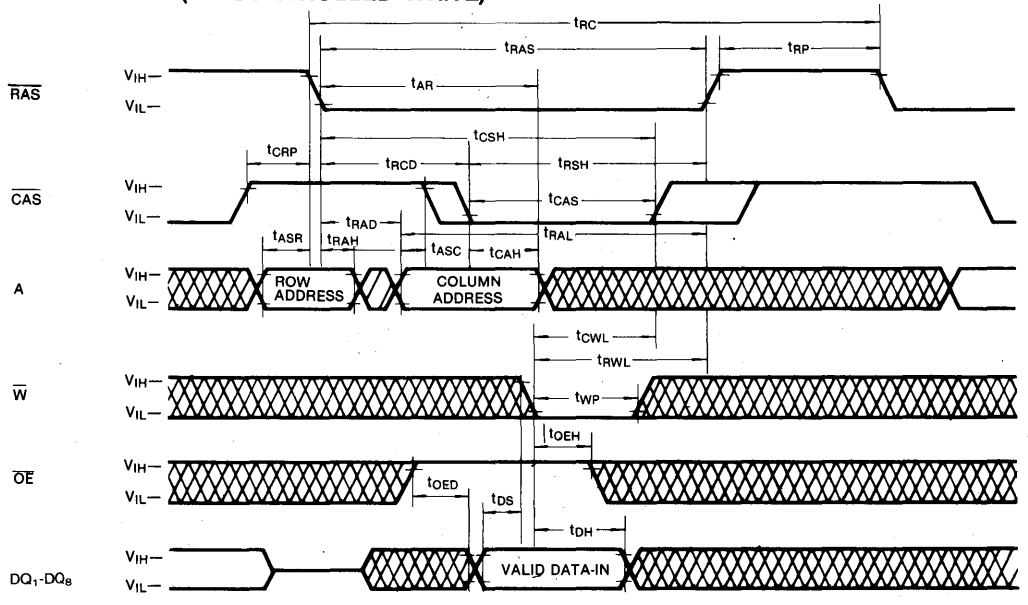


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



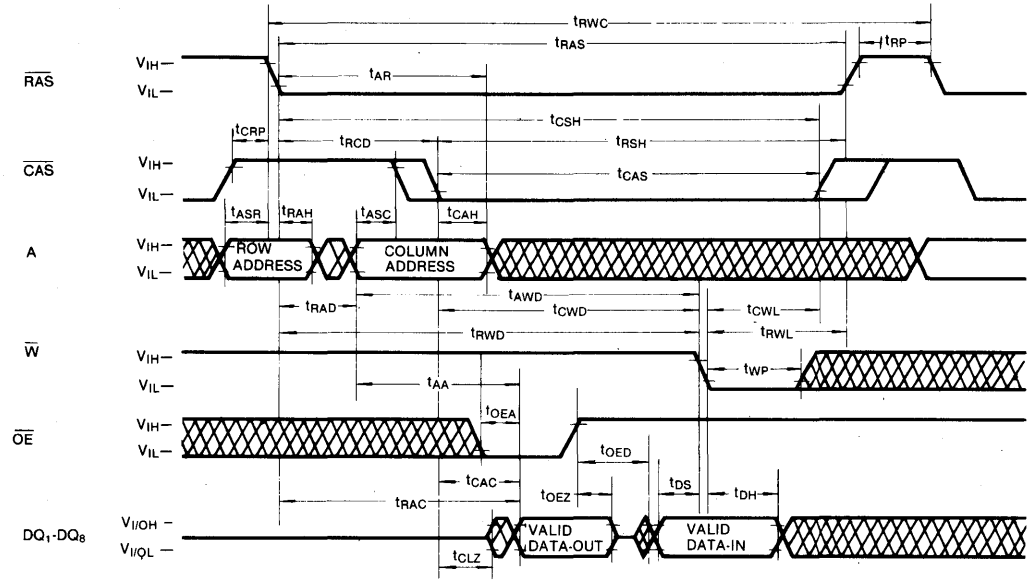
WRITE CYCLE (OE CONTROLLED WRITE)



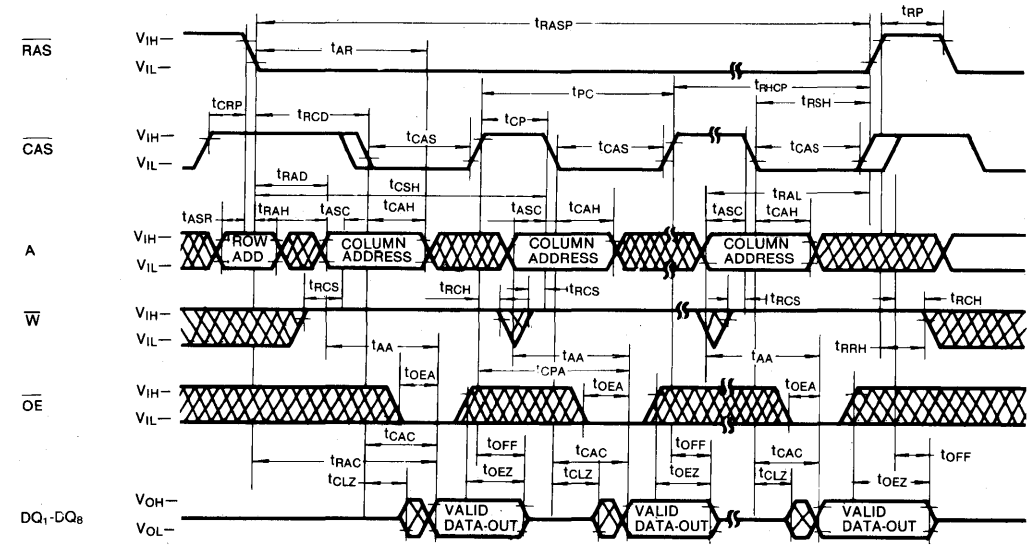
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



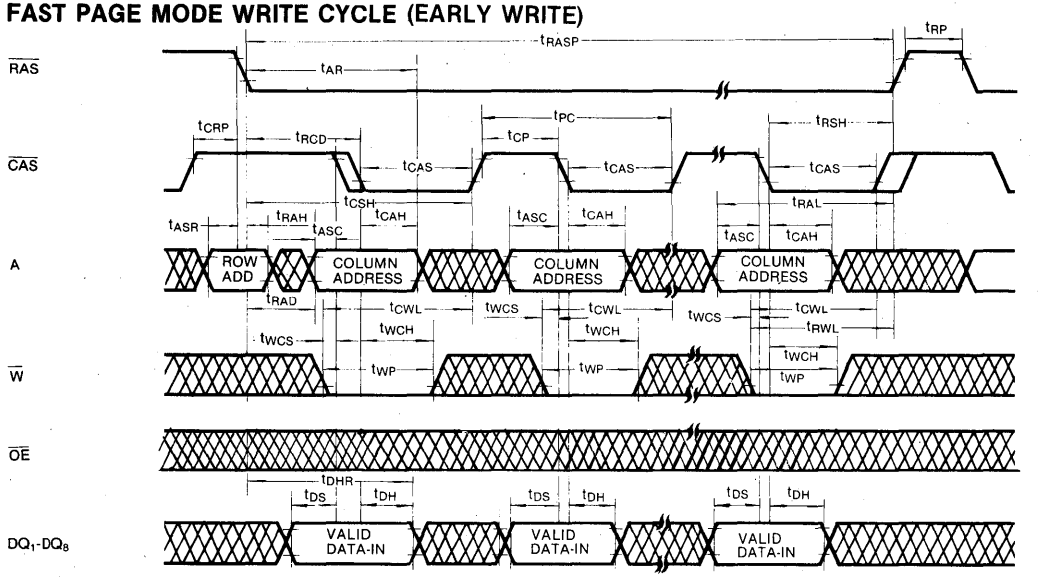
FAST PAGE MODE READ CYCLE



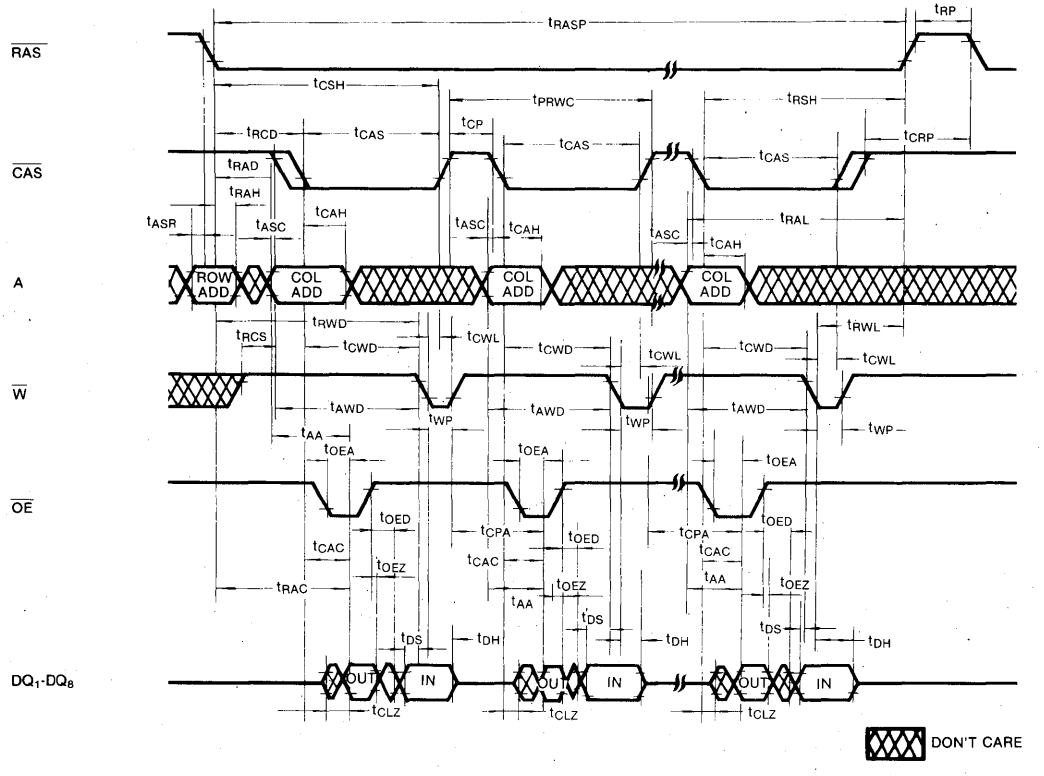
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



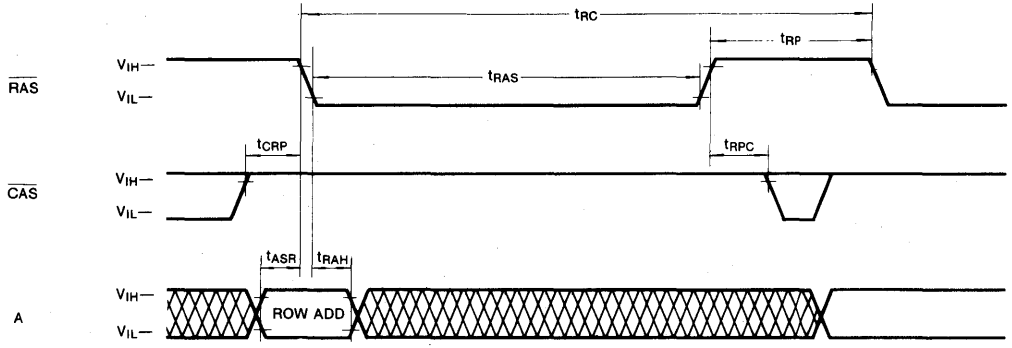
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

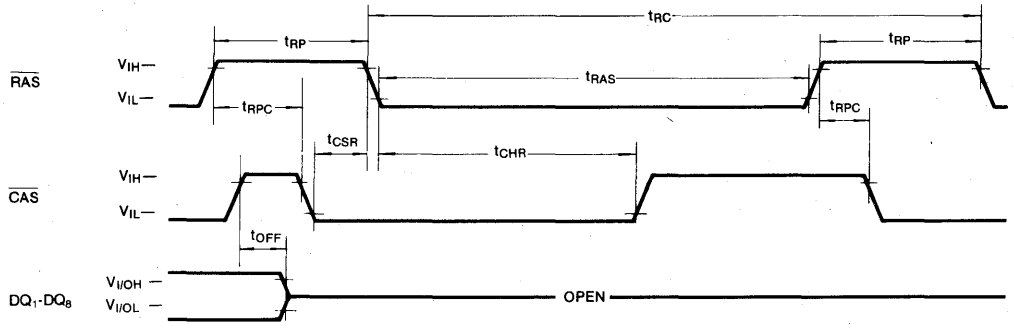
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



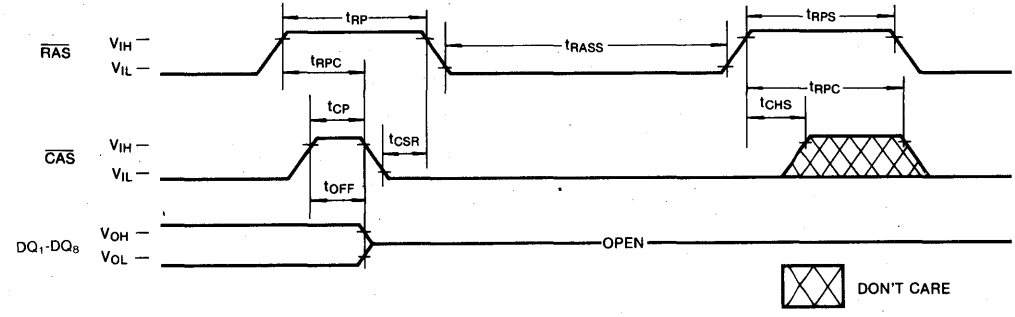
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



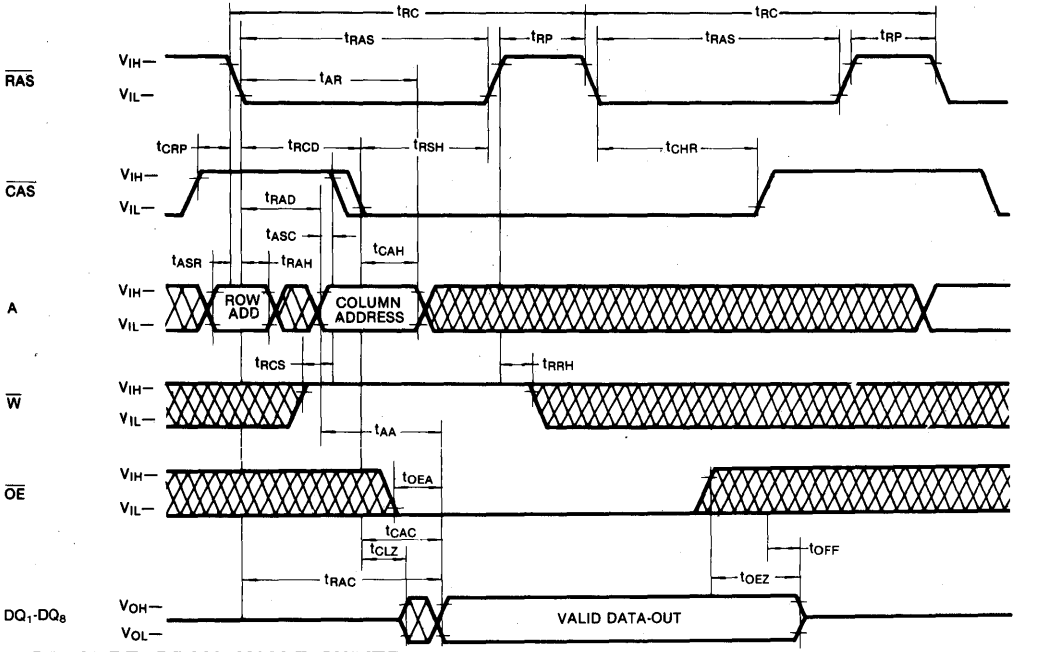
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

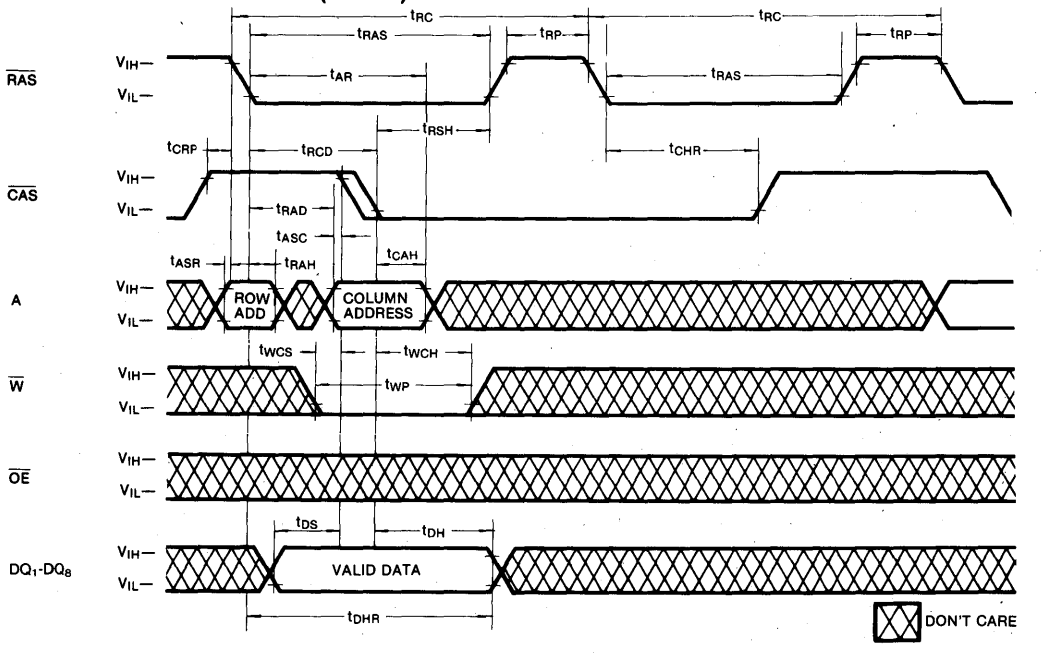


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



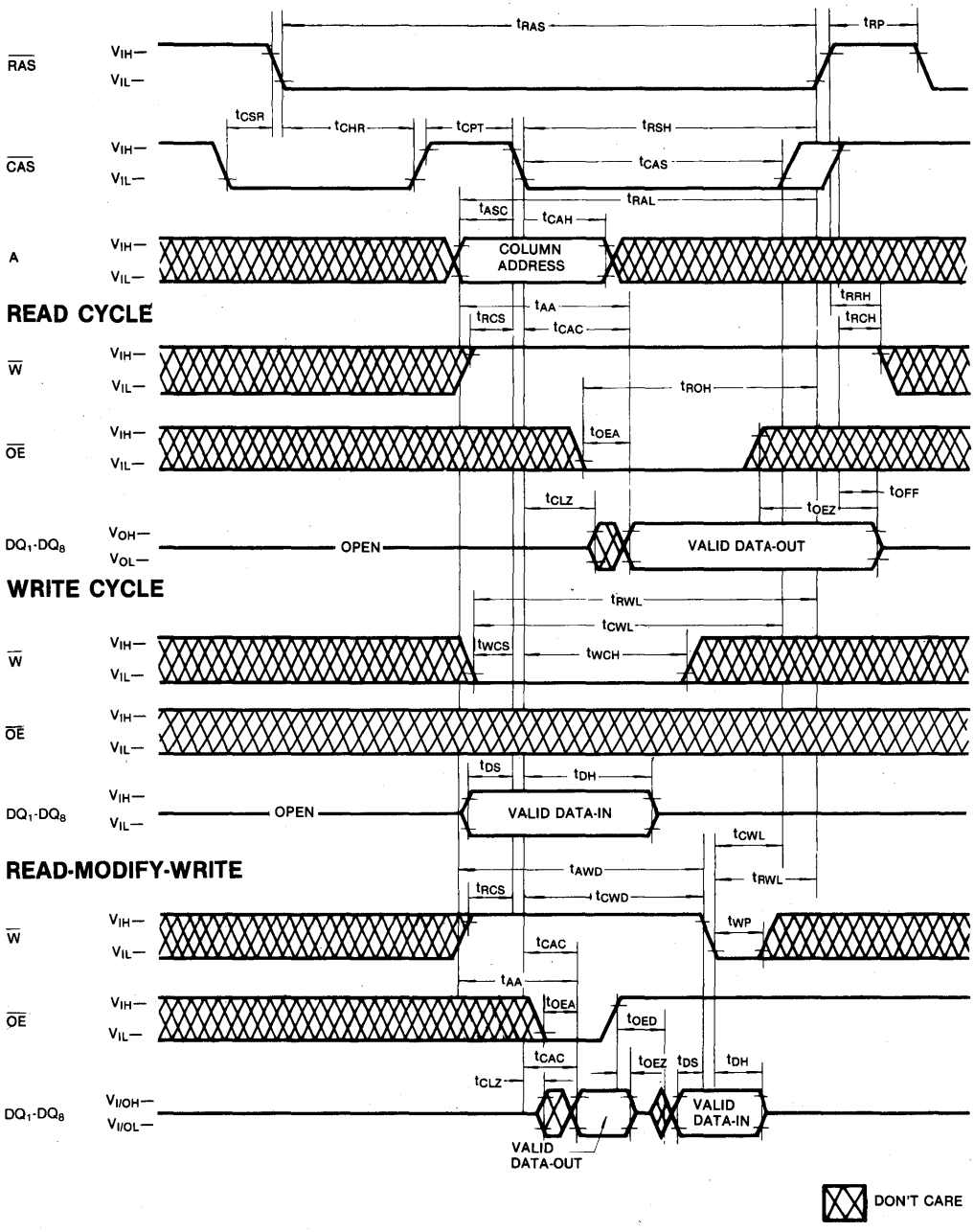
HIDDEN REFRESH CYCLE (WRITE)



SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

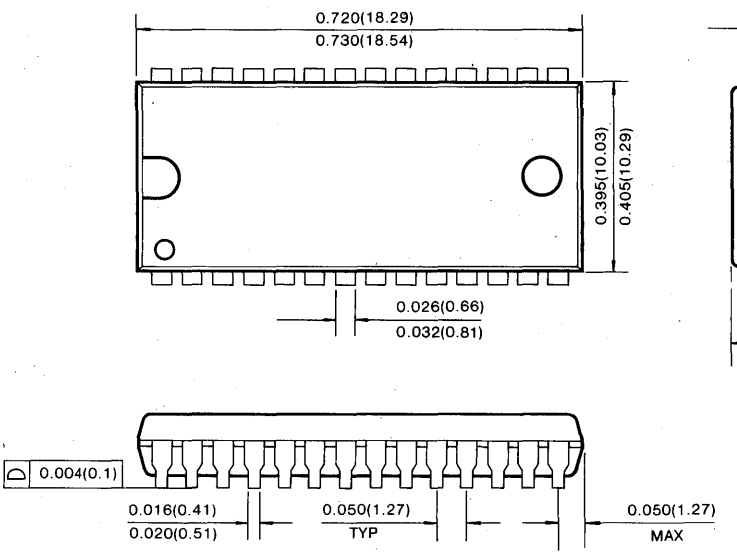
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE DIMENSION

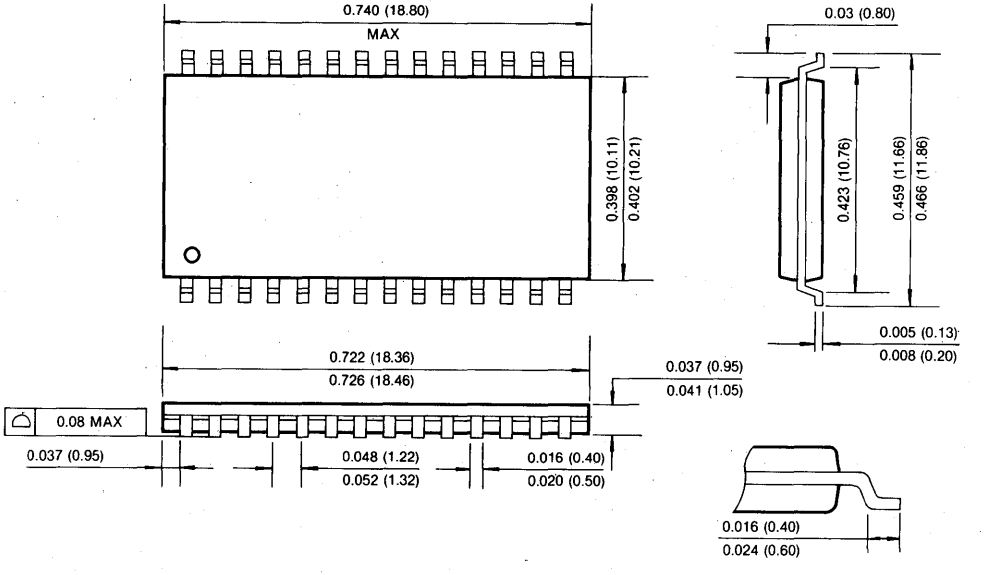
28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)



2M ×8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM48V2100A/AL/ALL/ASL-6	60ns	15ns	110ns
KM48V2100A/AL/ALL/ASL-7	70ns	20ns	130ns
KM48V2100A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Single+3.3V±0.3V power supply**
- **2048 cycles/32ms refresh (Normal)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

GENERAL DESCRIPTION

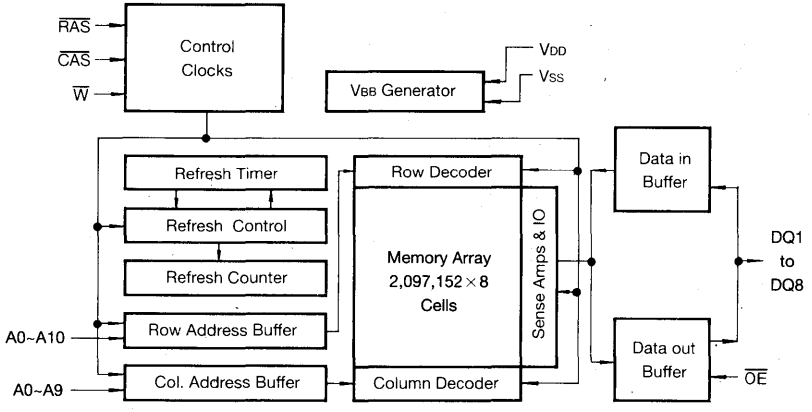
The Samsung KM48V2100A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48V2100A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48V2100A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

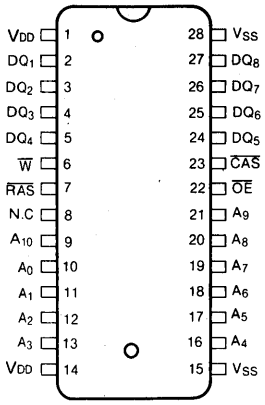
FUNCTIONAL BLOCK DIAGRAM



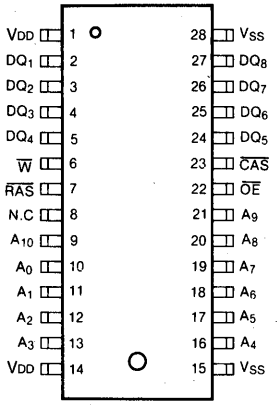
6

PIN CONFIGURATION (Top Views)

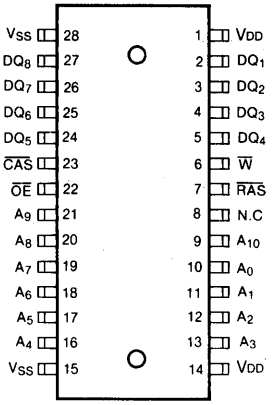
• KM48V2100 AJ/ALJ/ALLJ/ASLJ



• KM48V2100 AT/ALT/ALLT/ASLT



• KM48V2100 ATR/ALTR/ALLTR/ASLTR



Pin Name	Pin Function
A0-A10	Address Inputs
DQ1~8	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VDD	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 ~ 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48V2100A/AL/ALL/ASL-6 KM48V2100A/AL/ALL/ASL-7 KM48V2100A/AL/ALL/ASL-8	I_{CC1}	-	100 90 80	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48V2100A KM48V2100AL KM48V2100ALL KM48V2100ASL	I_{CC2}	-	2 1 1 1	mA mA mA mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM48V2100A/AL/ALL/ASL-6 KM48V2100A/AL/ALL/ASL-7 KM48V2100A/AL/ALL/ASL-8	I_{CC3}	-	100 90 80	mA mA mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM48V2100A/AL/ALL/ASL-6 KM48V2100A/AL/ALL/ASL-7 KM48V2100A/AL/ALL/ASL-8	I_{CC4}	-	80 70 60	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM48V2100A KM48V2100AL KM48V2100ALL KM48V2100ASL	I_{CC5}	-	1 300 200 200	mA μA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48V2100A/AL/ALL/ASL-6 KM48V2100A/AL/ALL/ASL-7 KM48V2100A/AL/ALL/ASL-8	I_{CC6}	-	100 90 80	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=62.5μS(L-Ver.) 125μS(SL-Ver.), T_{RAS}=T_{RAS} min.~300ns	KM48V2100AL KM48V2100ASL	I_{CC7}	-	400 300	μA μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{10}=V_{DD}-0.2V or 0.2V DQ_1~DQ_8=V_{DD}-0.2V, 0.2V or Open	KM48V2100ALL	I_{CC8}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Test Condition : V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal)	t_{REF}		32		32		32	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ commend hold time	t_{OEH}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

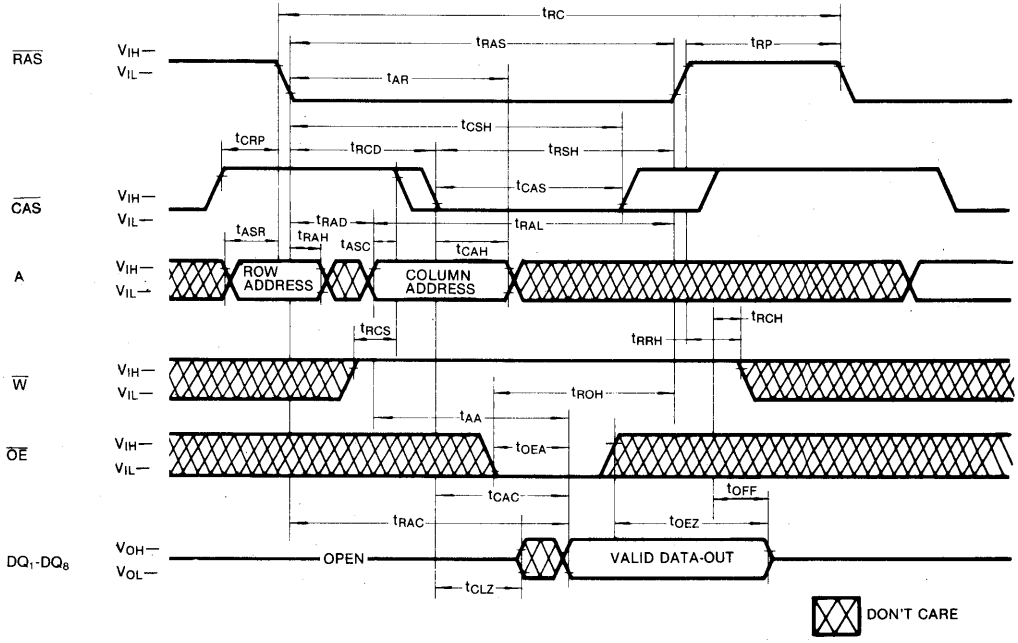
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Fast Page mode cycle time	tPC	45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 100pF and V_{oh}=2.0V(I_{OUT}=2mA), V_{ol}=0.8V(I_{OUT}=2mA)
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

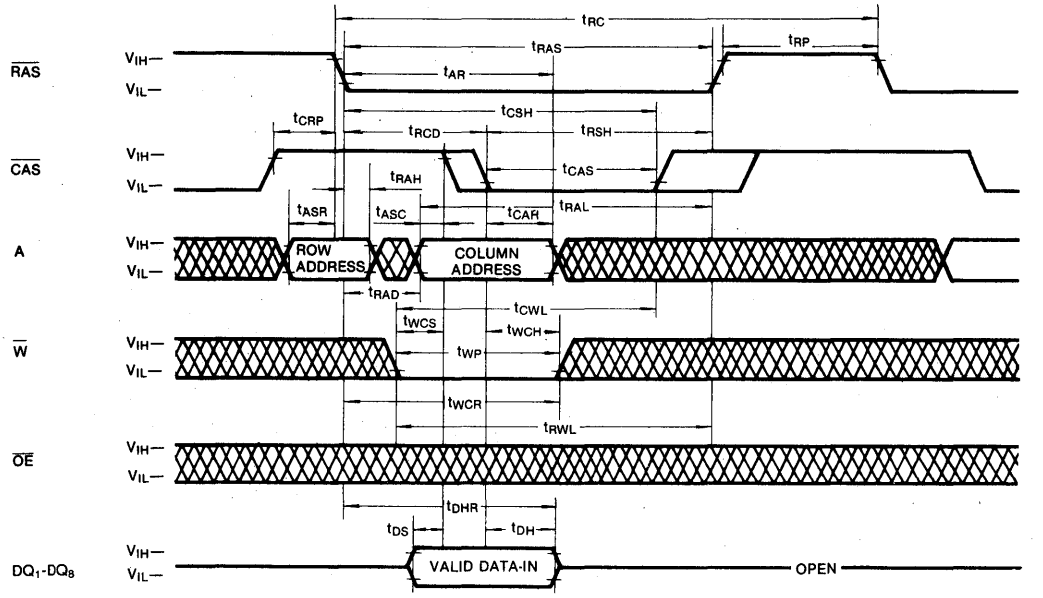
TIMING DIAGRAMS

READ CYCLE

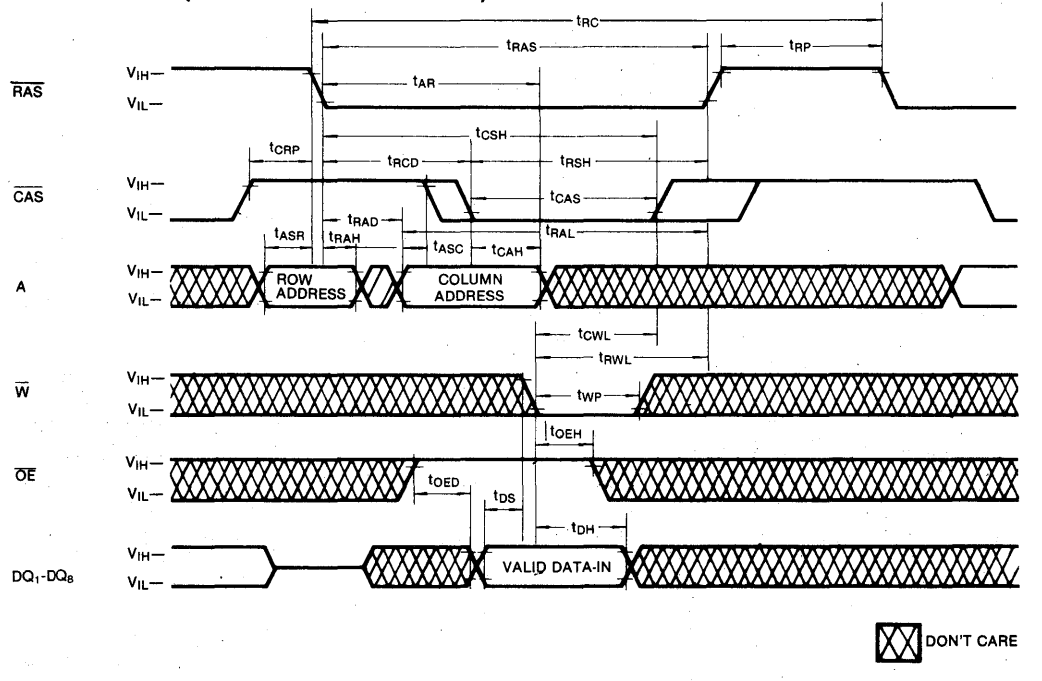


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

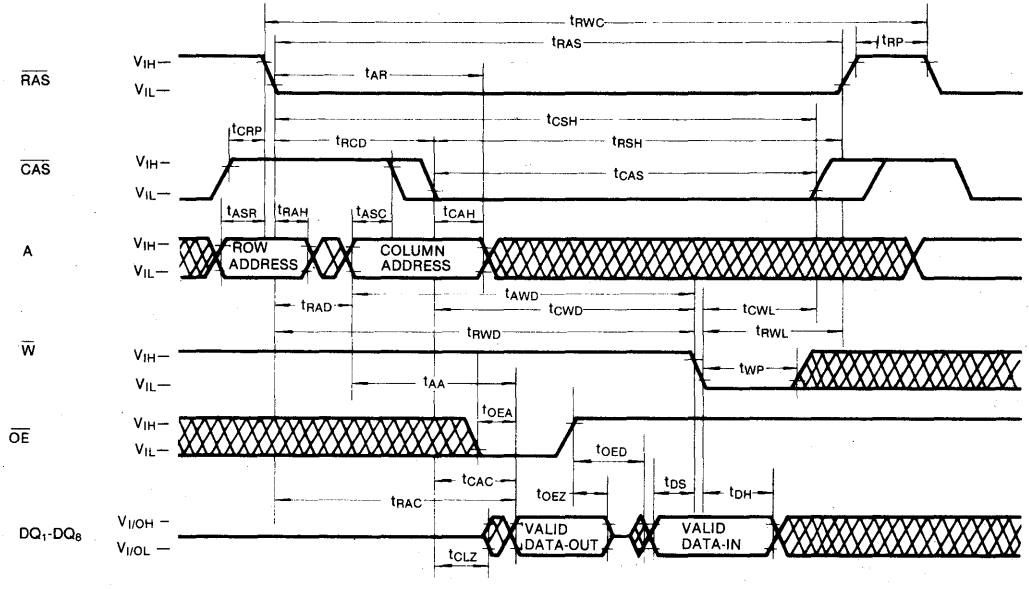


WRITE CYCLE (OE CONTROLLED WRITE)

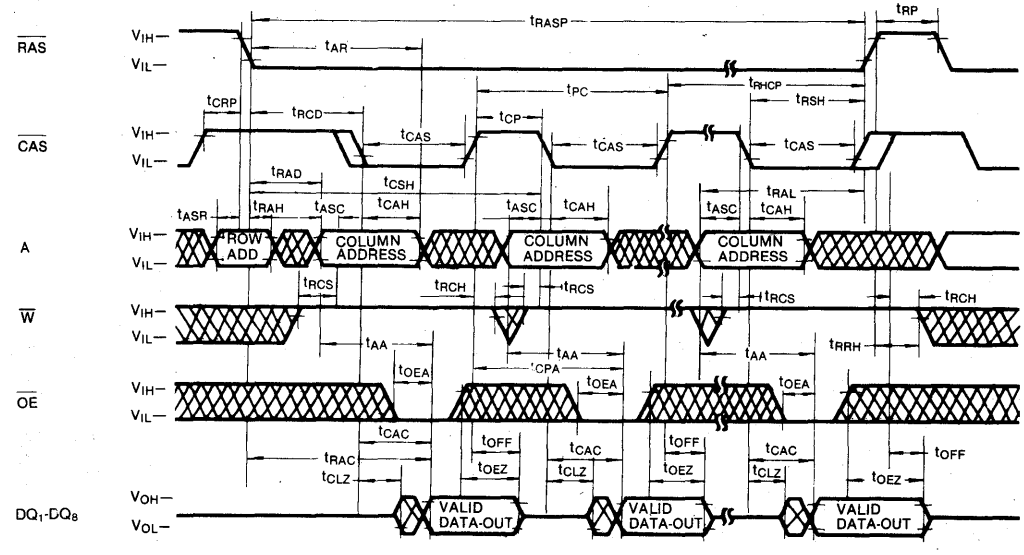


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



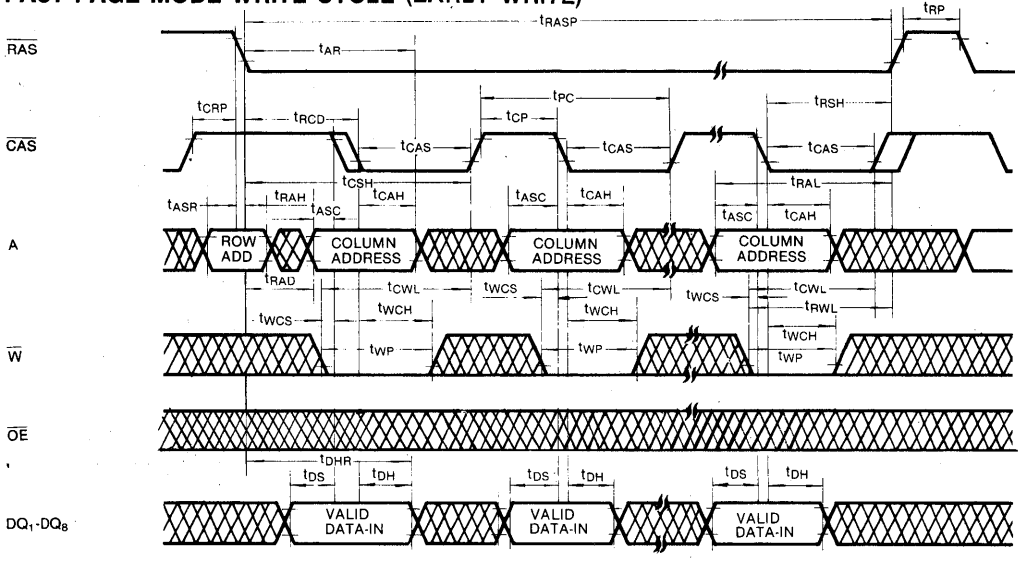
FAST PAGE MODE READ CYCLE



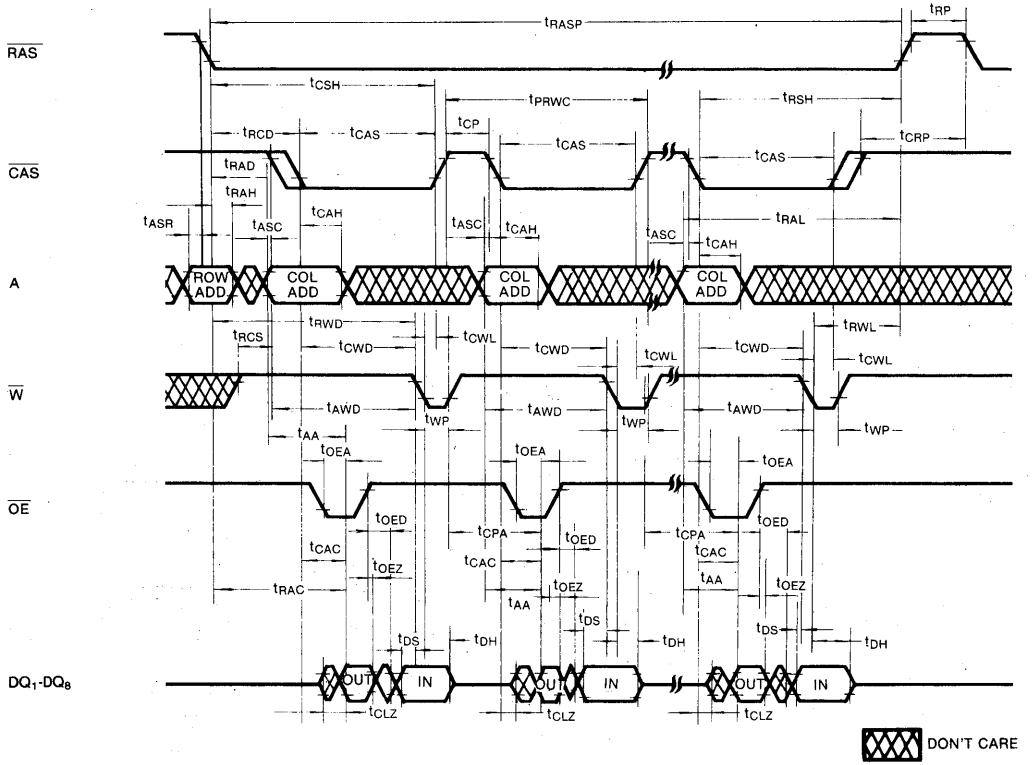
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



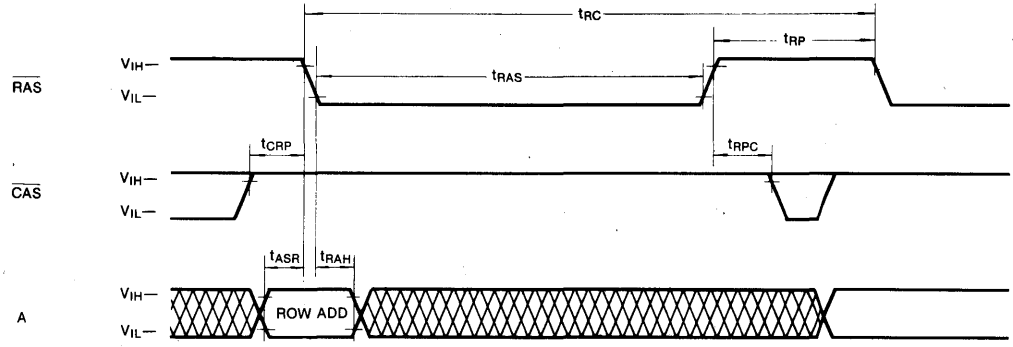
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

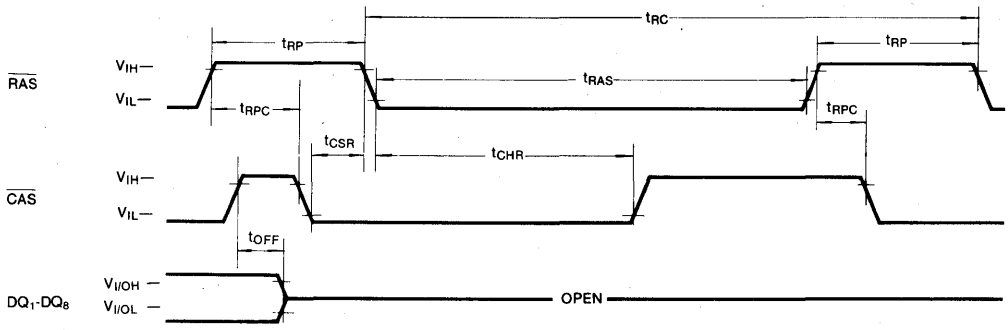
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



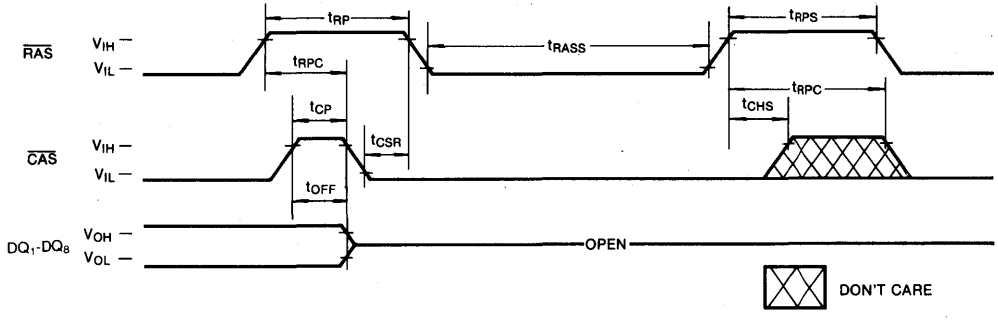
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



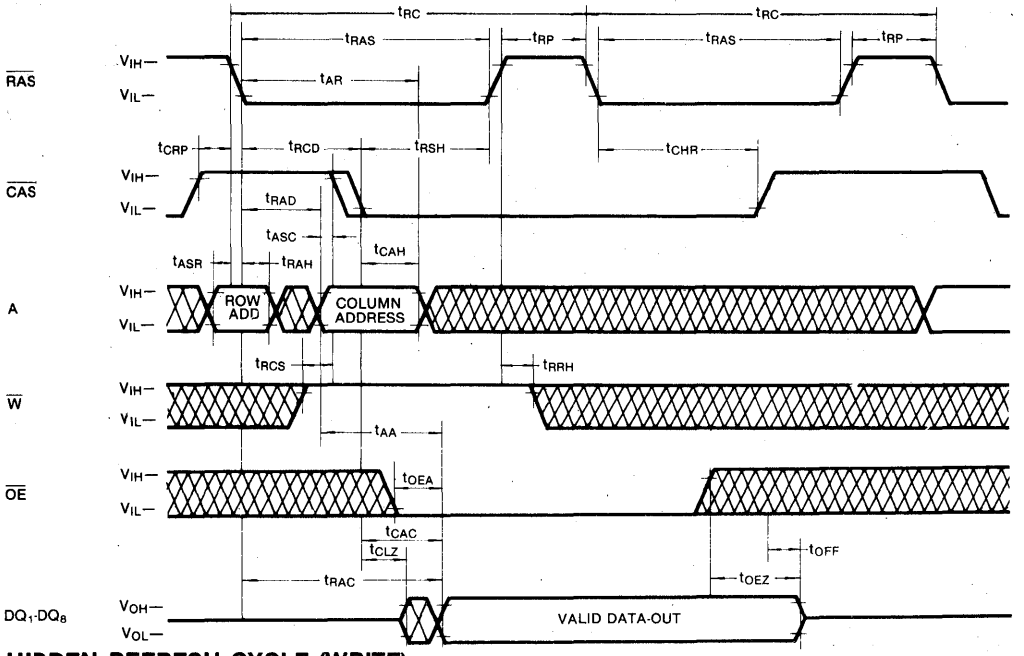
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

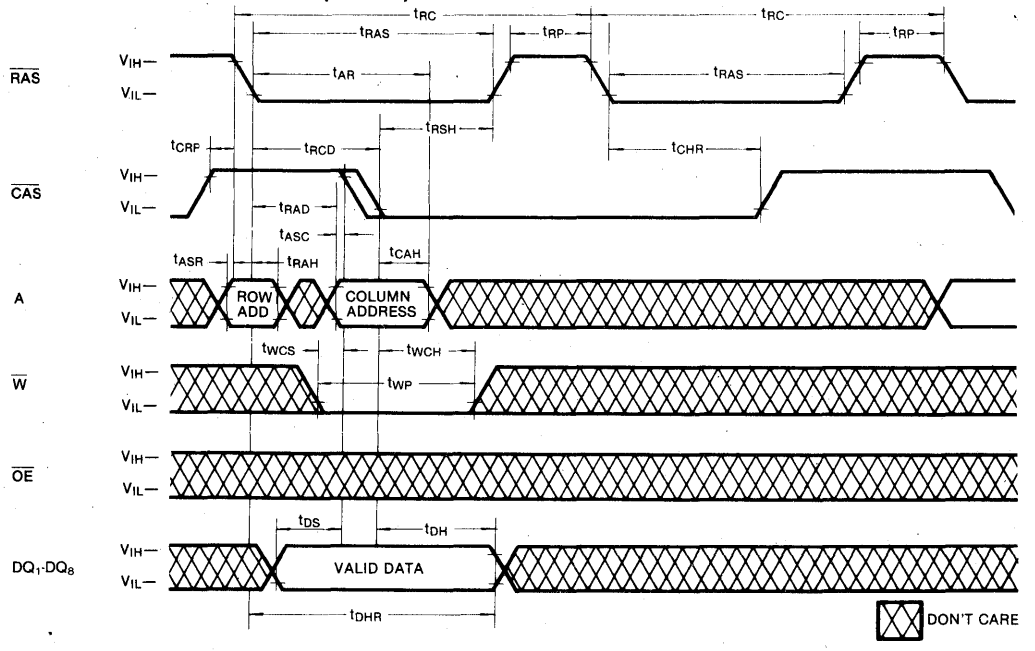


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

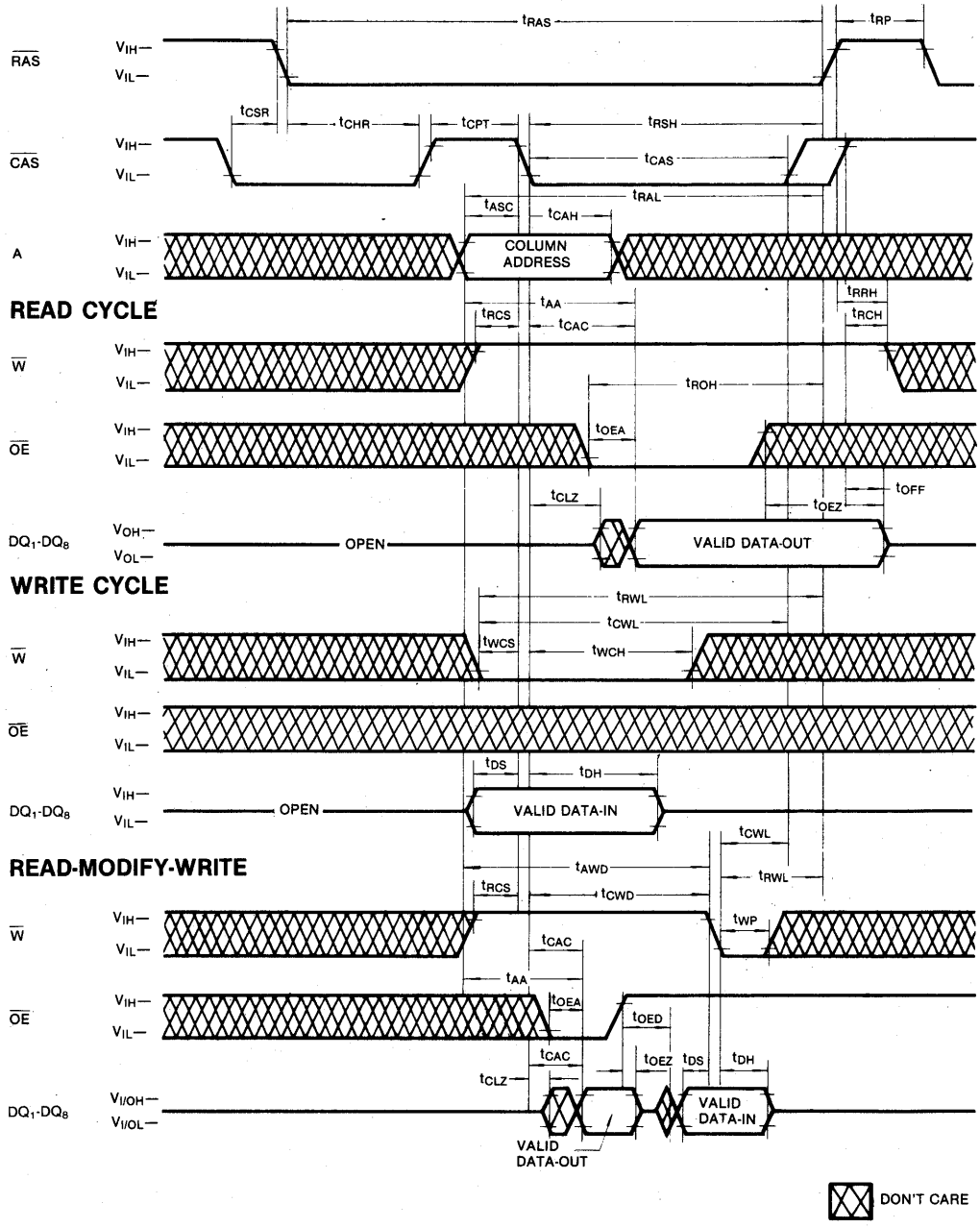


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

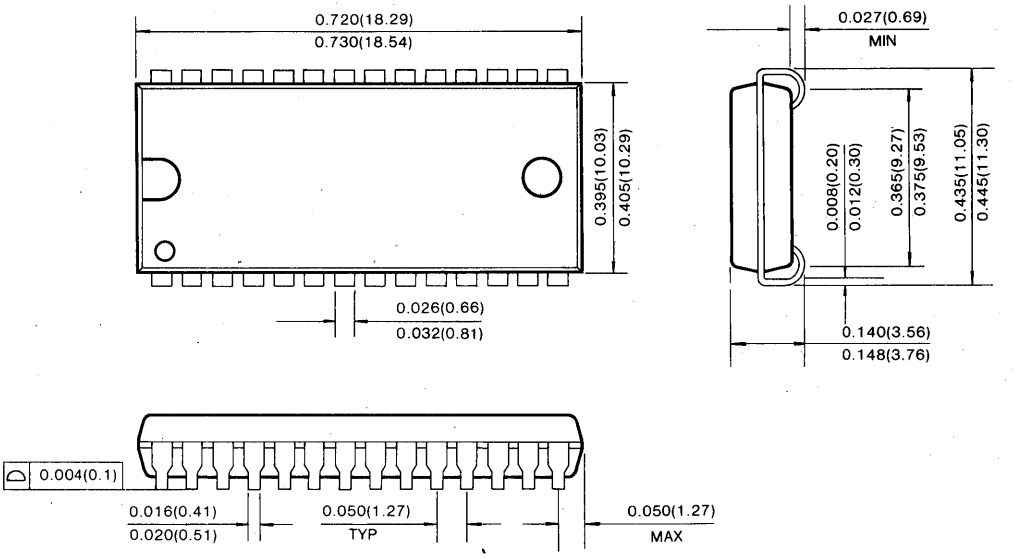
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE DIMENSION

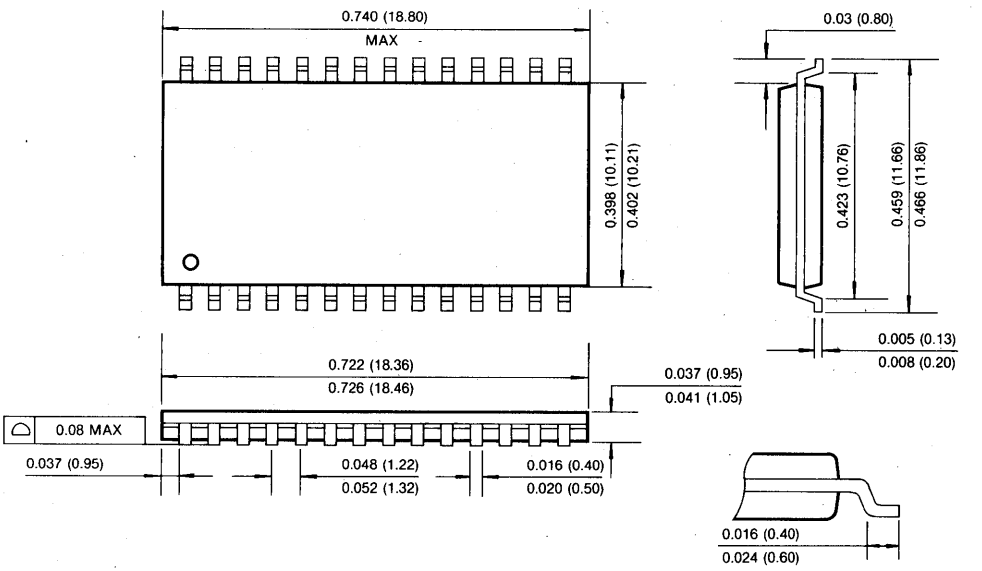
28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)



SAMSUNG ELECTRONICS

2M ×8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
KM48V2004A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM48V2004A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM48V2004A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- **Fast Page Mode with Extended data out**
- **Self Refresh Operation (LL-ver. only)**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **LVTTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+3.3V±0.3V power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

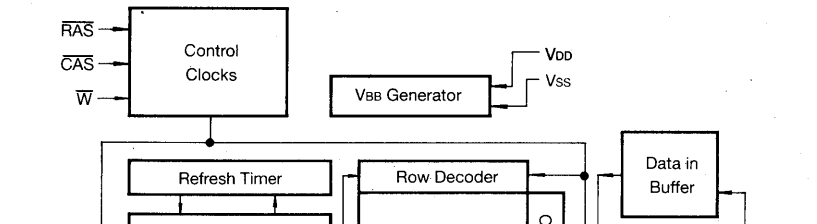
The Samsung KM48V2004A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit×8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48V2004A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48V2004A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



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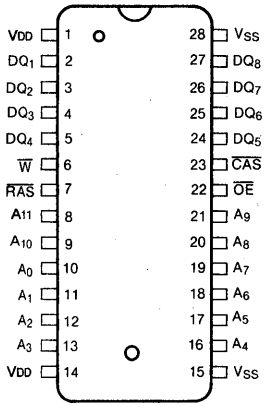
SAMSUNG ELECTRONICS

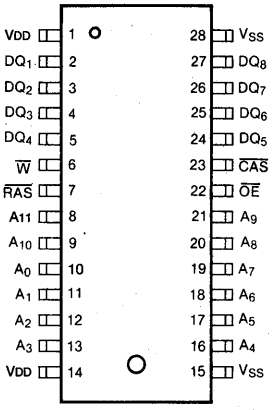
PIN CONFIGURATION (Top Views)

• KM48V2004 AJ/ALJ/ALLJ/ASLJ



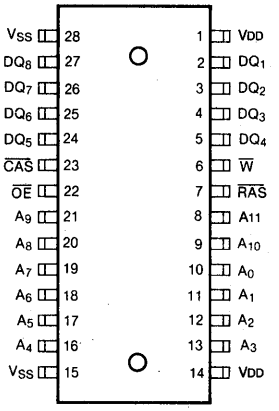
J : 400MIL

• KM48V2004 AT/ALT/ALLT/ASLT



T : 400MIL (Forword)

• KM48V2004 ATR/ALTR/ALLTR/ASLTR



TR : 400MIL (Reverse)

Pin Name	Pin Function
A_0-A_{11}	Address Inputs
$DQ_{1\sim8}$	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{DD}	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5~ 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5~ 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48V2004A/AL/ALL/ASL-6 KM48V2004A/AL/ALL/ASL-7 KM48V2004A/AL/ALL/ASL-8	I_{CC1}	-	80 70 60	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48V2004A KM48V2004AL KM48V2004ALL KM48V2004ASL	I_{CC2}	-	2 1 1 1	mA mA mA mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM48V2004A/AL/ALL/ASL-6 KM48V2004A/AL/ALL/ASL-7 KM48V2004A/AL/ALL/ASL-8	I_{CC3}	-	80 70 60	mA mA mA
Hyper Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM48V2004A/AL/ALL/ASL-6 KM48V2004A/AL/ALL/ASL-7 KM48V2004A/AL/ALL/ASL-8	I_{CC4}	-	90 80 70	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM48V2004A KM48V2004AL KM48V2004ALL KM48V2004ASL	I_{CC5}	-	1 300 200 200	mA μA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48V2004A/AL/ALL/ASL-6 KM48V2004A/AL/ALL/ASL-7 KM48V2004A/AL/ALL/ASL-8	I_{CC6}	-	80 70 60	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ_1~DQ_8=Don't Care t_{RC}=31.25μs(L-Ver.) 62.5μs(SL-Ver.), t_{RAS}=t_{RAS} min.~300ns	KM48V2004AL KM48V2004ASL	I_{CC7}	-	450 350	μA μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{DD}-0.2V or 0.2V DQ_1~DQ_8=V_{DD}-0.2V, 0.2V or Open	KM48V2004ALL	I_{CC8}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz))

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Test condition: V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	45		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	15	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	6
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	9
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	
Write command pulse width	t_{WP}	10		15		15		ns	6
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10		15		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	60		70		75		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Hyper Page cycle time	t_{HPC}	24		29		34		ns	17
Hyper Page read-modify-write cycle time	t_{HPRWC}	71		86		96		ns	17
$\overline{CAS}$ precharge time (Hyper Page cycle)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	7,14
$\overline{OE}$ commend hold time	tOEH	15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	7,15
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	tWPE	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from $\overline{W}$	tWEZ	3	15	3	20	3	20	ns	7,14
$\overline{W}$ to data delay	tWED	15		20		20		ns	
$\overline{RAS}$ pulse width (LL-ver)	tRASS	100		100		100		μs	16
$\overline{RAS}$ precharge time (LL-ver)	tRPS	110		130		150		ns	16
$\overline{CAS}$ hold time (LL-ver)	tCHS	-50		-50		-50		ns	16

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	15	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	50		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Hyper Page cycle time	tHPC	29		34		39		ns	
Hyper Page read-modify-write cycle time	tHPRWC	76		91		101		ns	
$\overline{RAS}$ pulse width (Hyper Page Cycle)	tRASP	65	200,000	75	200,000	85	200,000	ns	

TEST MODE CYCLE (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
$\overline{OE}$ access time	t_{OEA}		20		25		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	20		25		25		ns	

TEST MODE DESCRIPTION

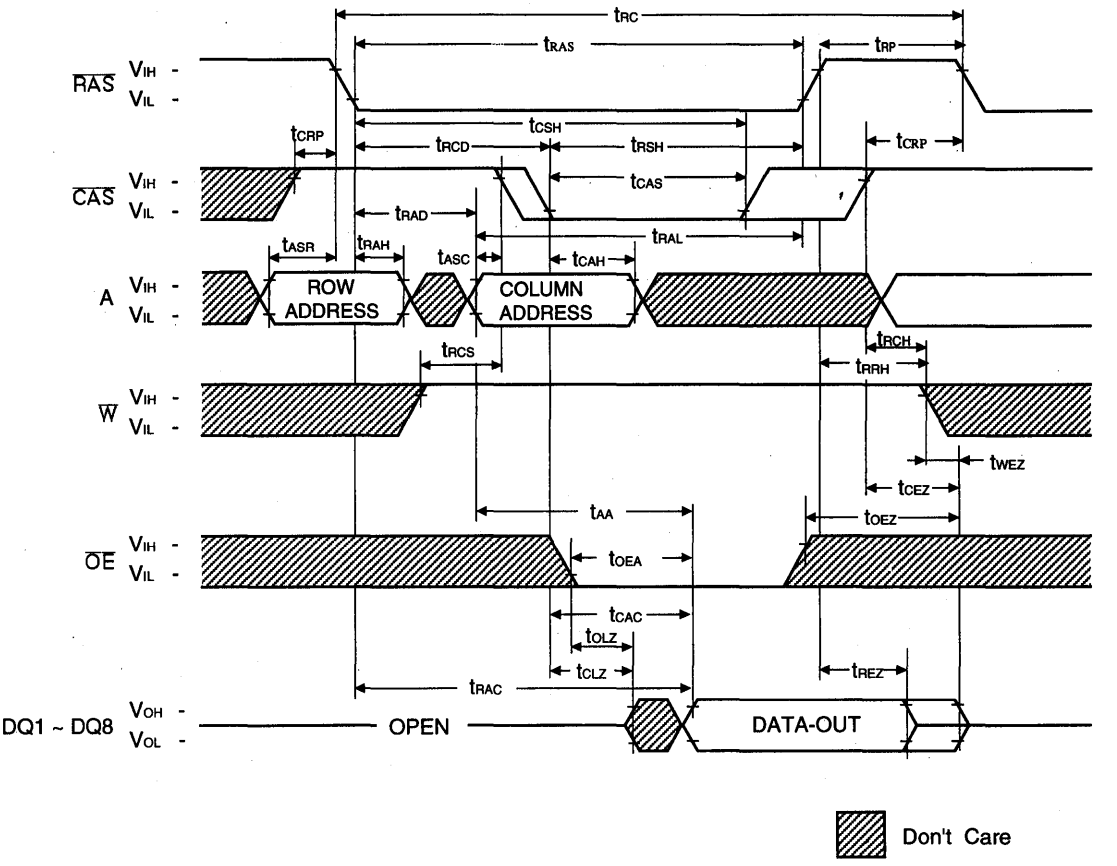
The KM48V2004A/AL/ALL/ASL is the CMOS DRAM organized 2,097,152 words by 8 bit internally organized 1,048,576 words by 16 bits. In " Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In Test Mode", the 2Mx8 DRAM can be tested as if it were a 1Mx8 DRAM. $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", And "$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" peforms the refresh operation with internal CBR refresh address counter. "Test Mode" function reduces test time (1/2 in cases of N test pattern).

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs, without t_{HPC} and t_{HPRWC}.
3. Measured with a load equivalent to 1TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{REZ}(max), t_{CEZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.
16. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going
17. $t_{ASC} \geq t_{CP}$(min), Assumn t_T=2.0ns

TIMING DIAGRAM

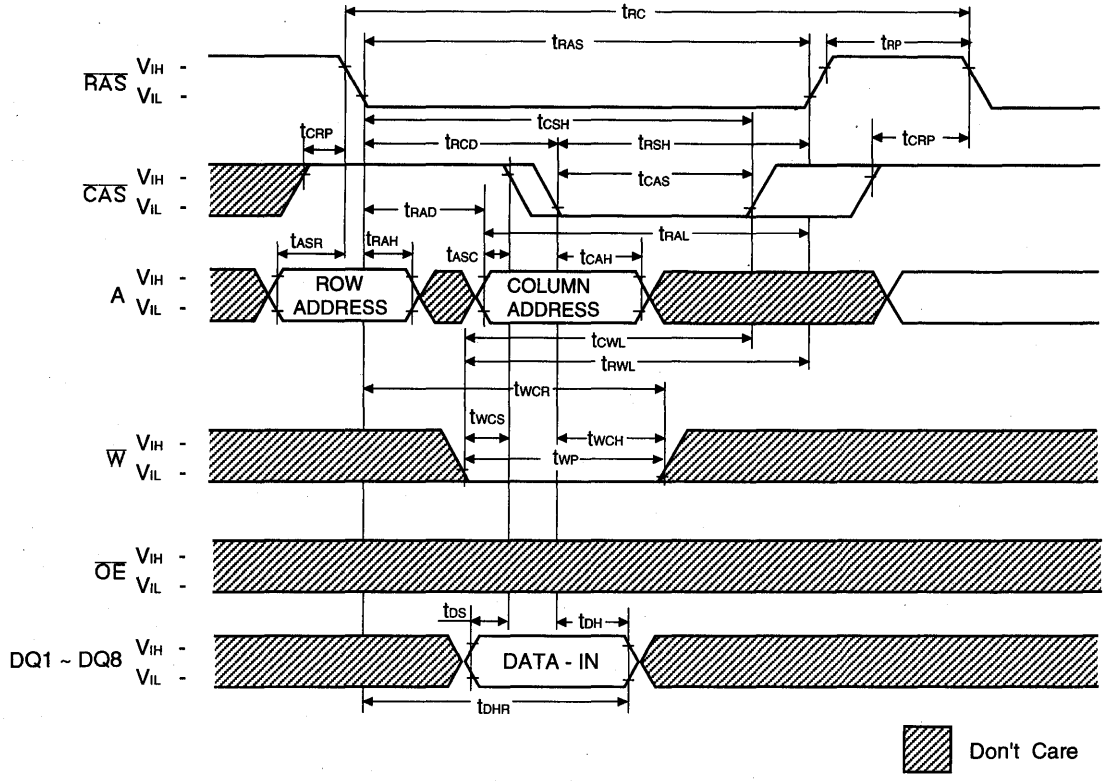
READ CYCLE



SAMSUNG ELECTRONICS

WRITE CYCLE (EARLY WRITE)

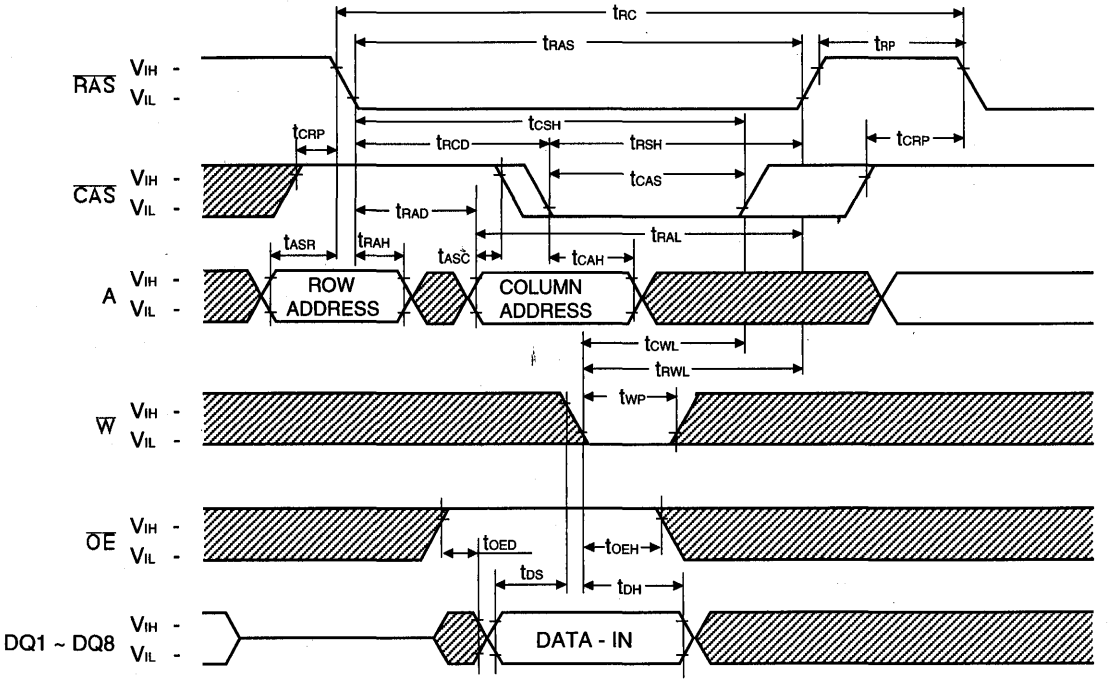
NOTE : D_{OUT} = OPEN



SAMSUNG ELECTRONICS

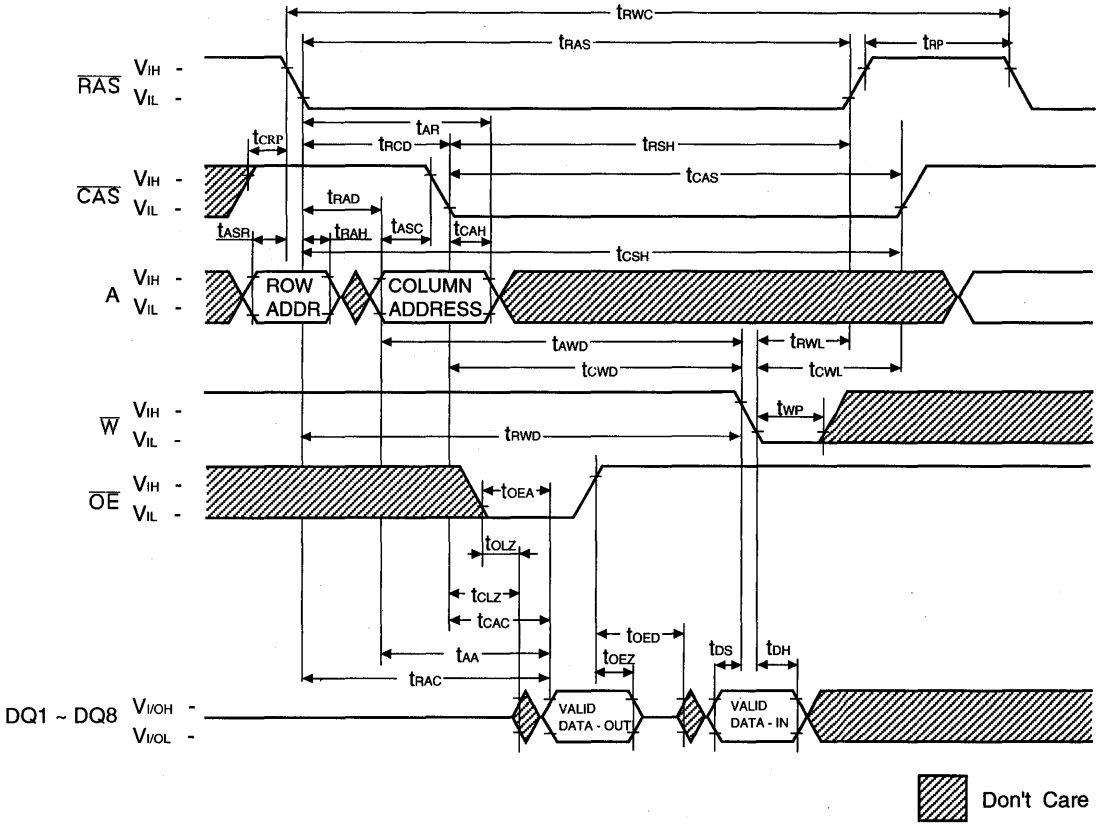
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

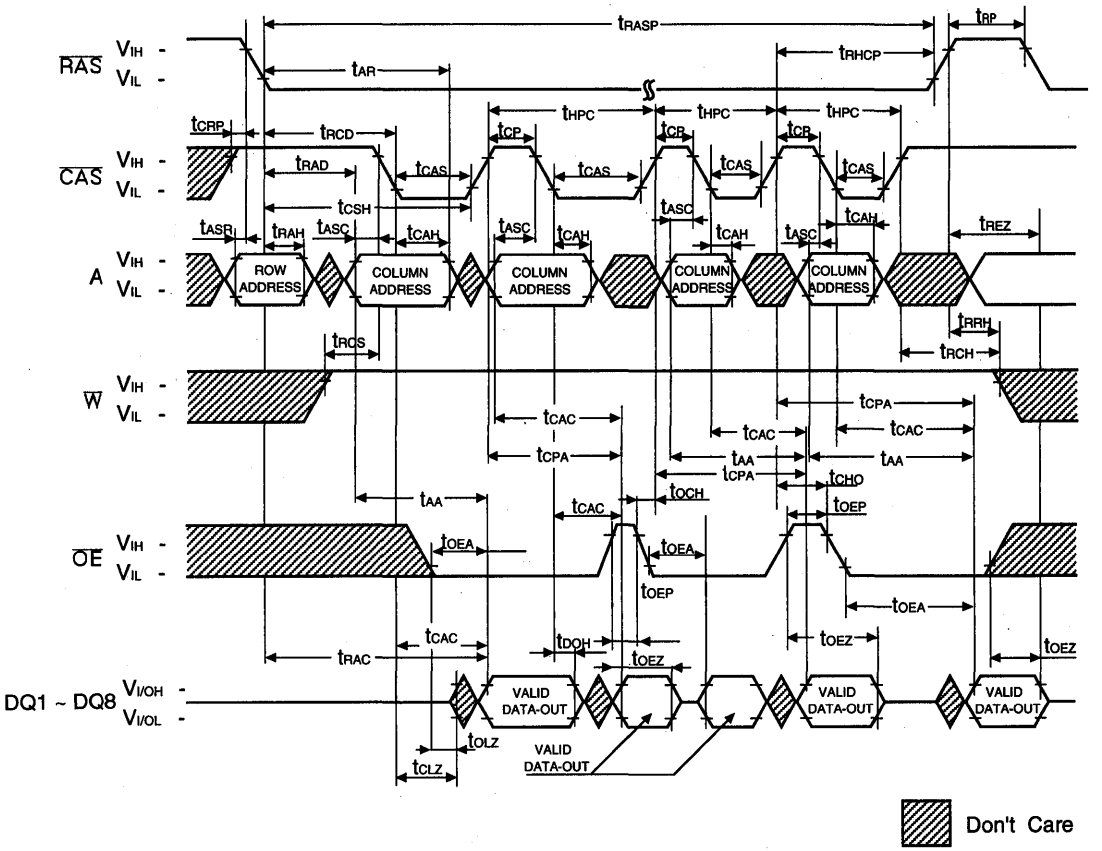


Don't Care

READ - MODIFY - WRITE CYCLE

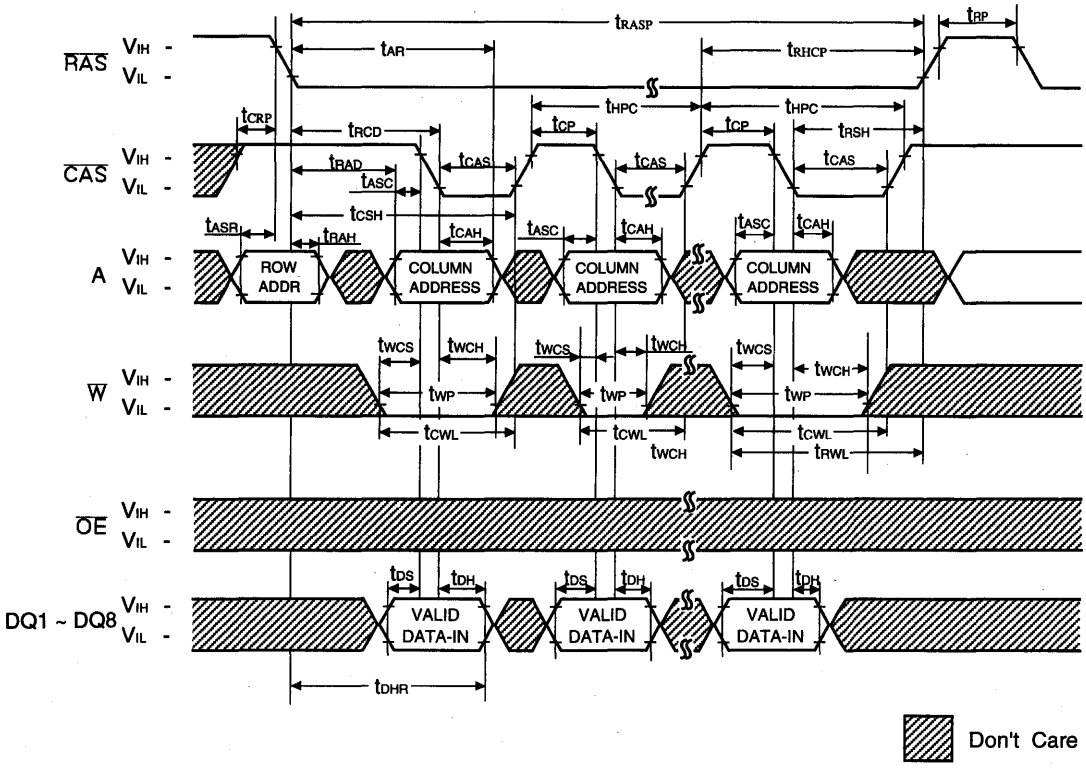


HYPER PAGE READ CYCLE



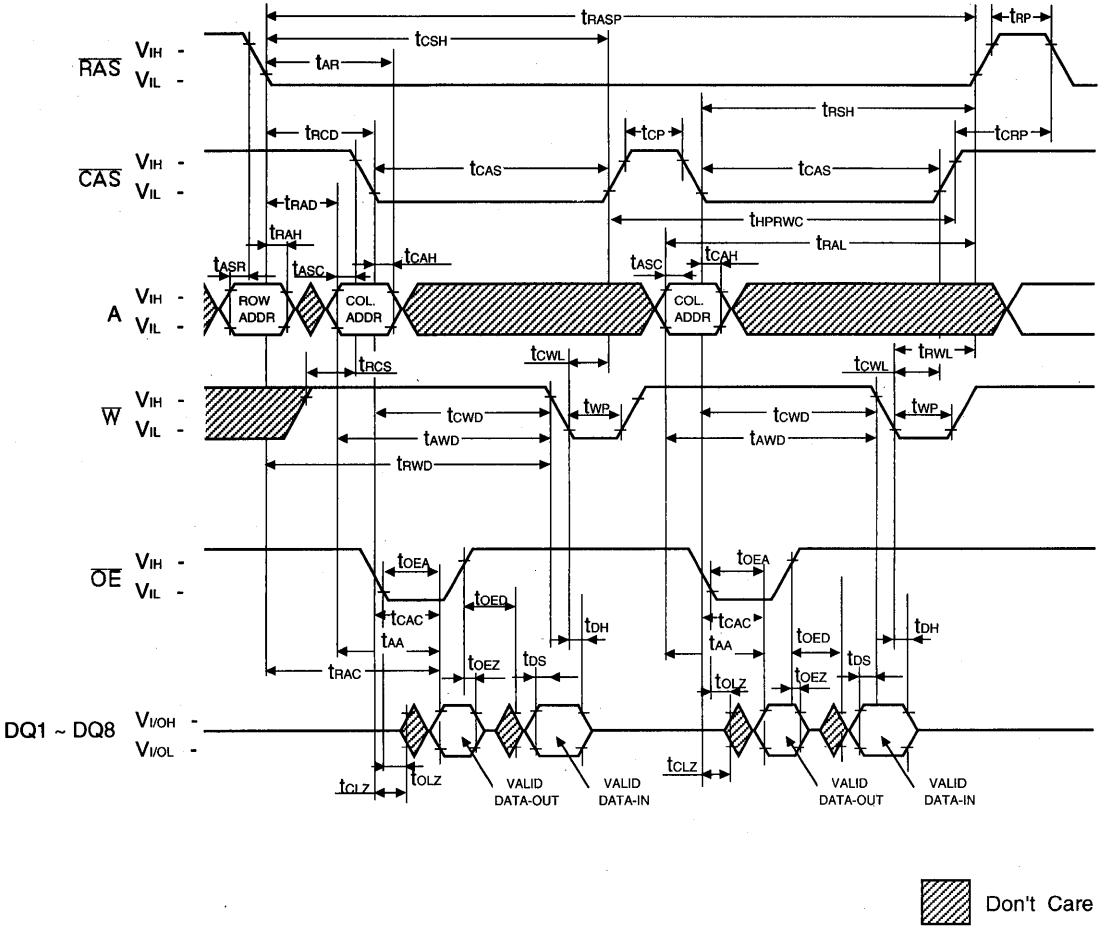
HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open

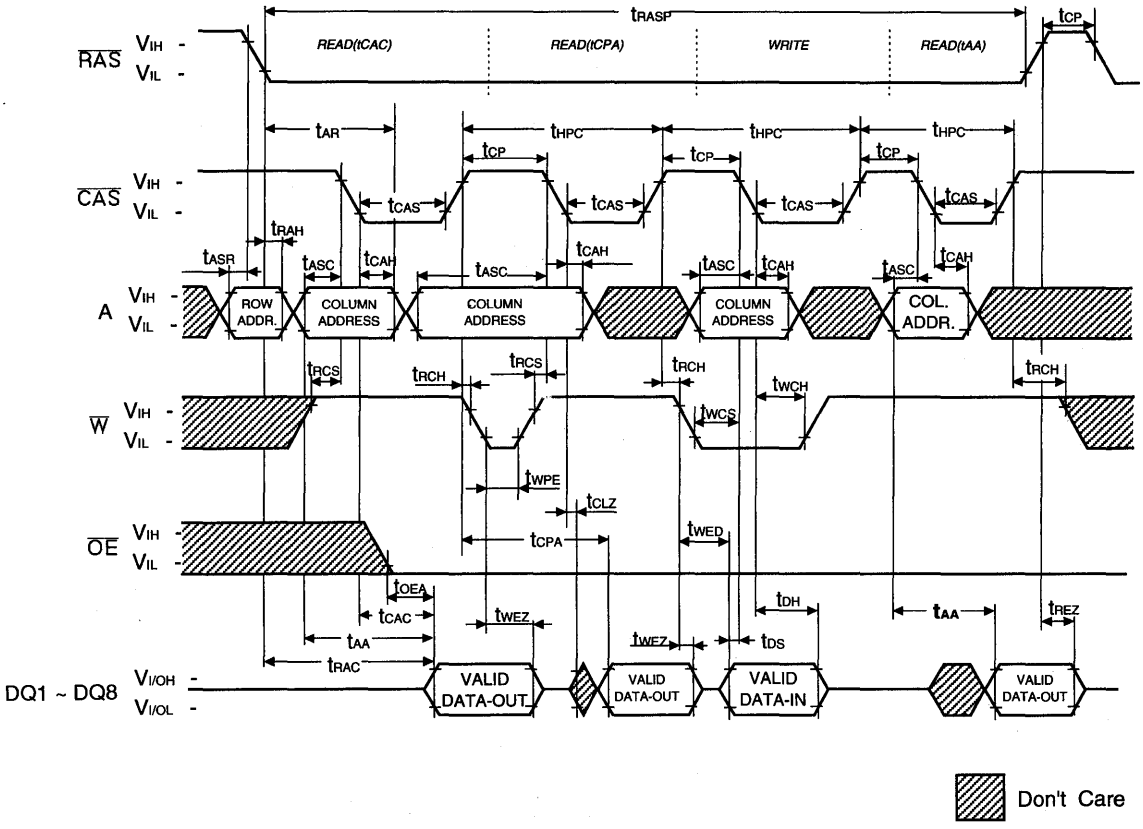


SAMSUNG ELECTRONICS

HYPER PAGE READ-MODIFY-WRITE CYCLE

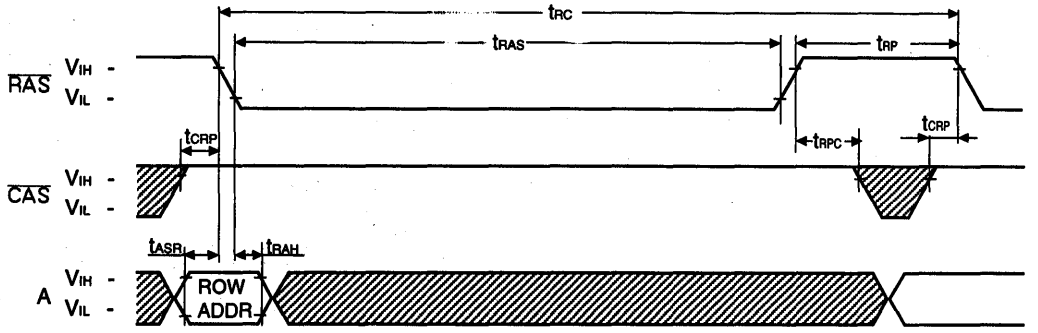


HYPER PAGE READ AND WRITE MIXED CYCLE



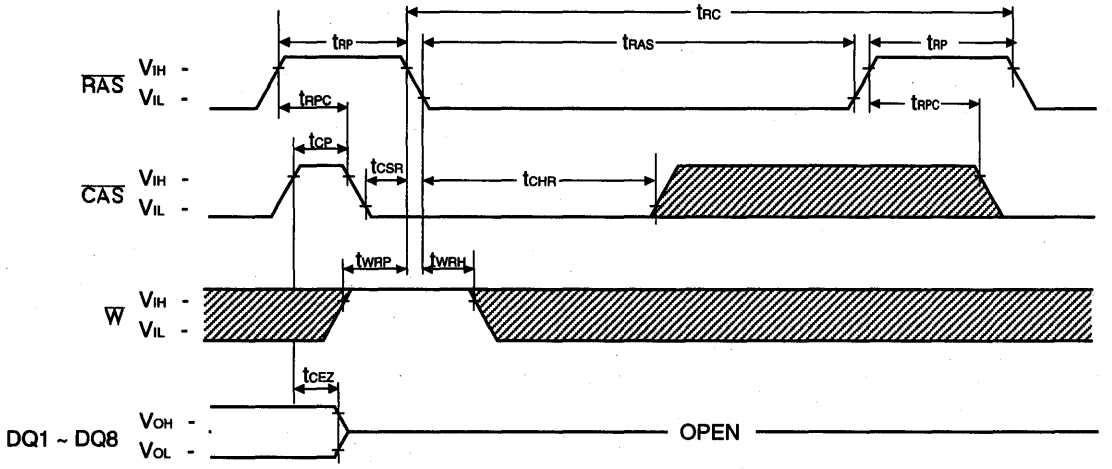
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



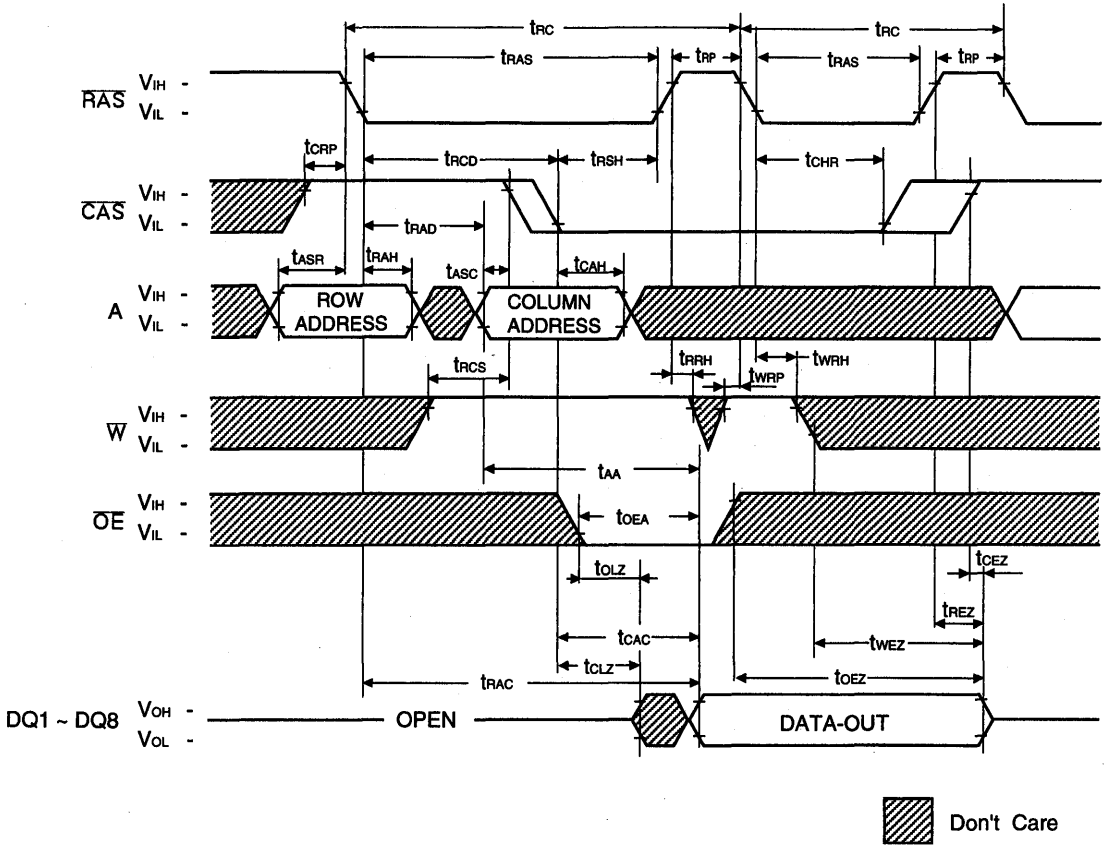
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



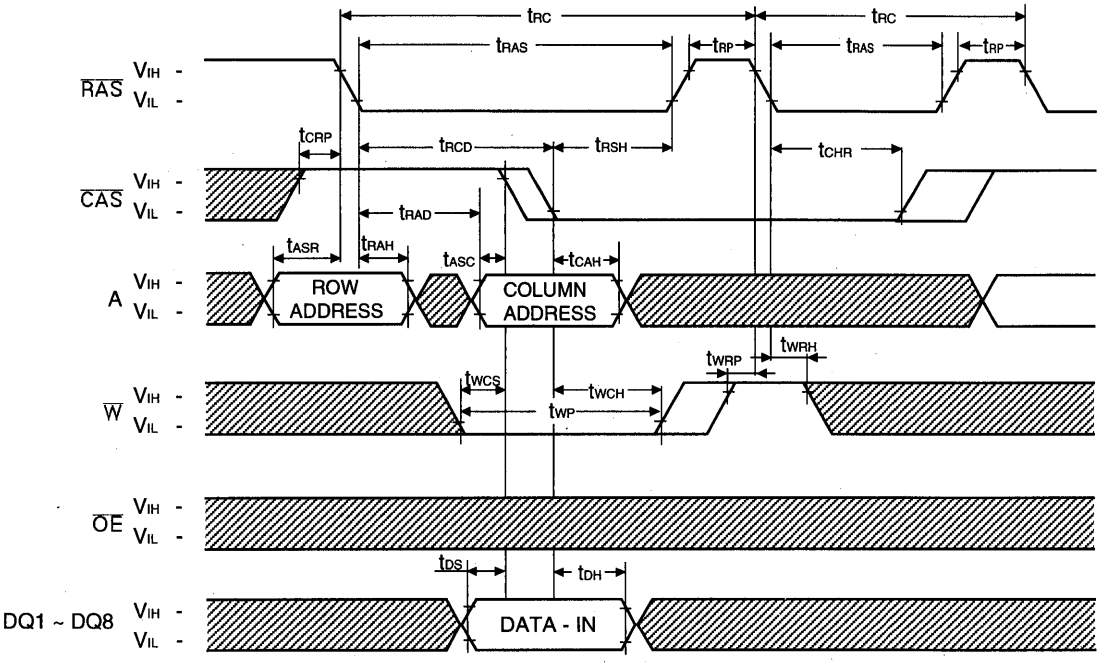
Don't Care

HIDDEN REFRESH CYCLE (READ)



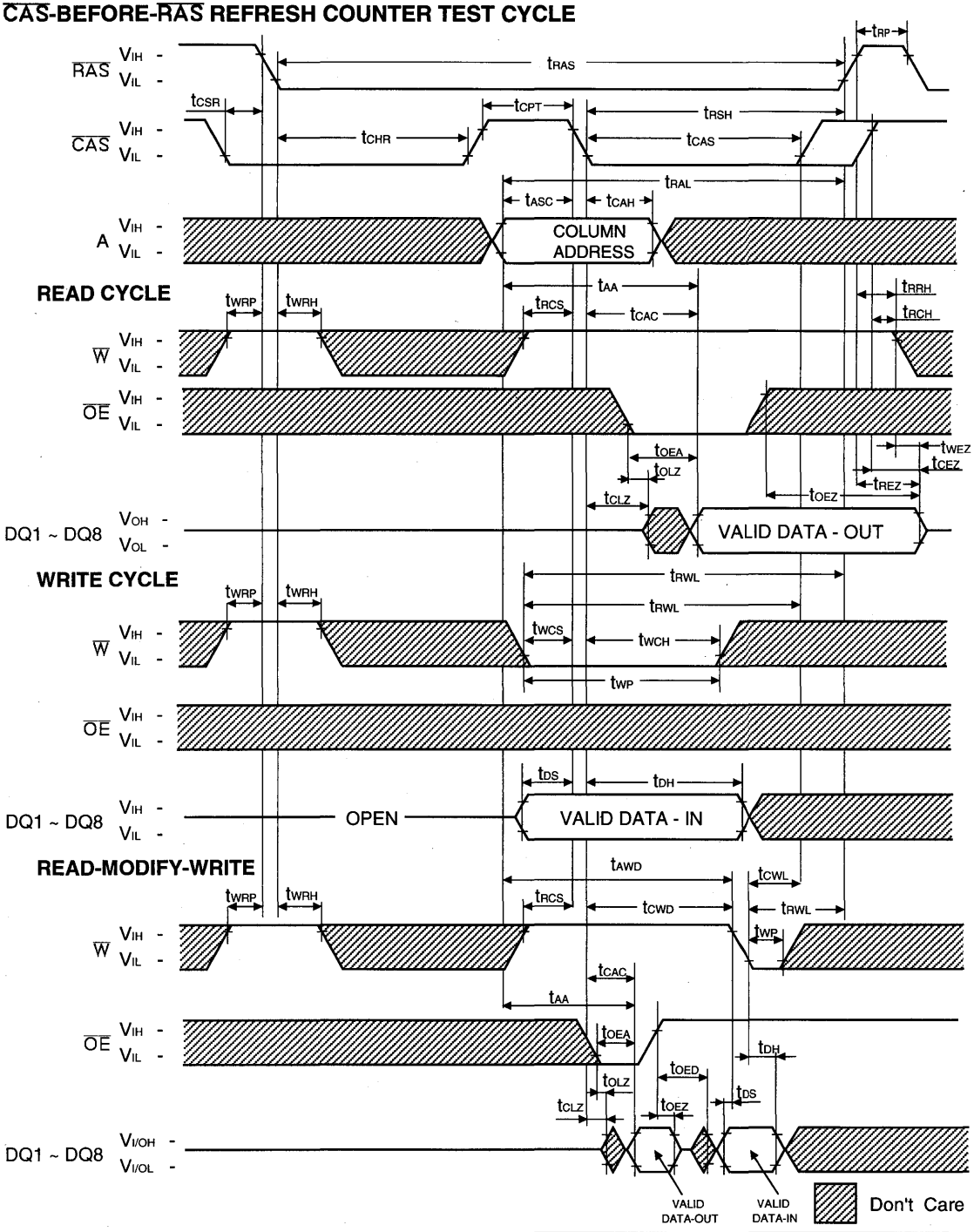
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



Don't Care

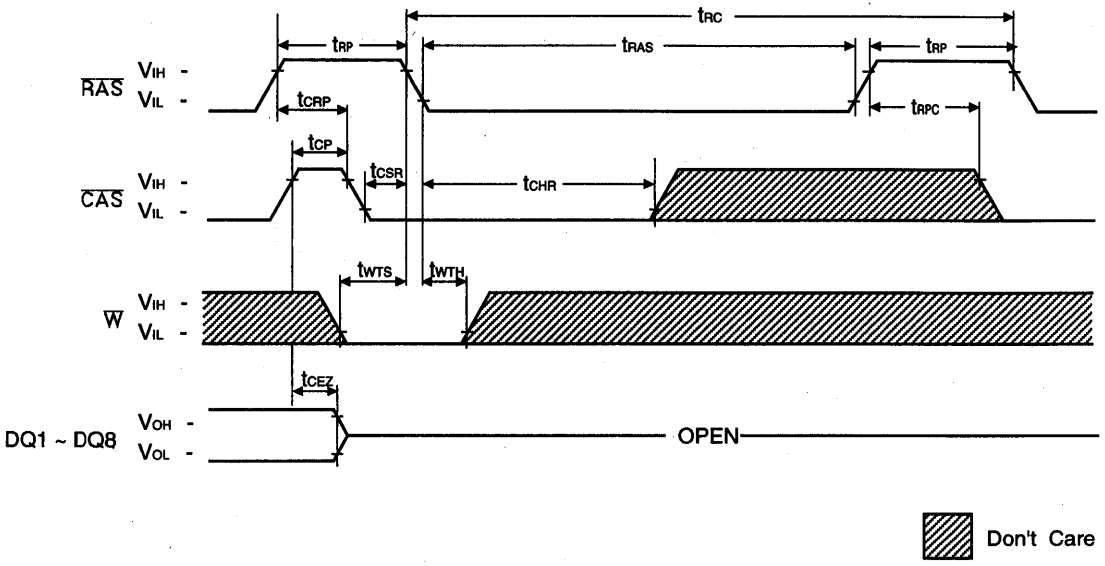
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



SAMSUNG ELECTRONICS

TEST MODE IN CYCLE

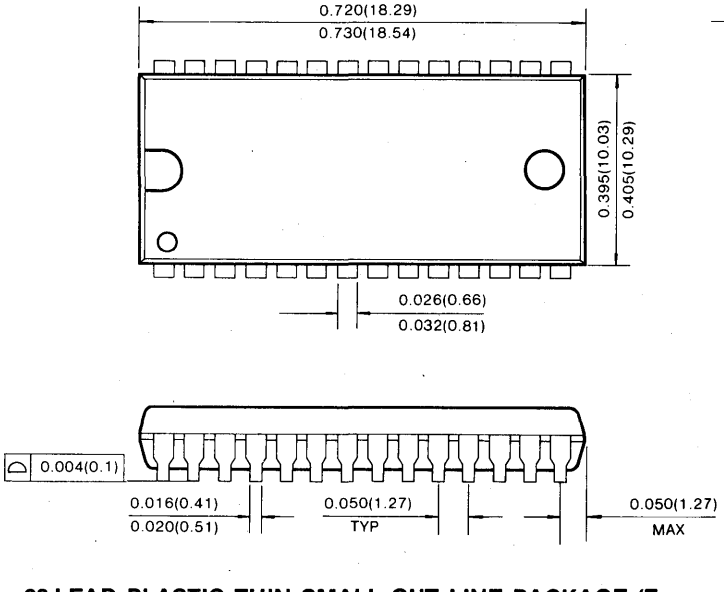
NOTE : $\overline{OE}$, A = Don't Care



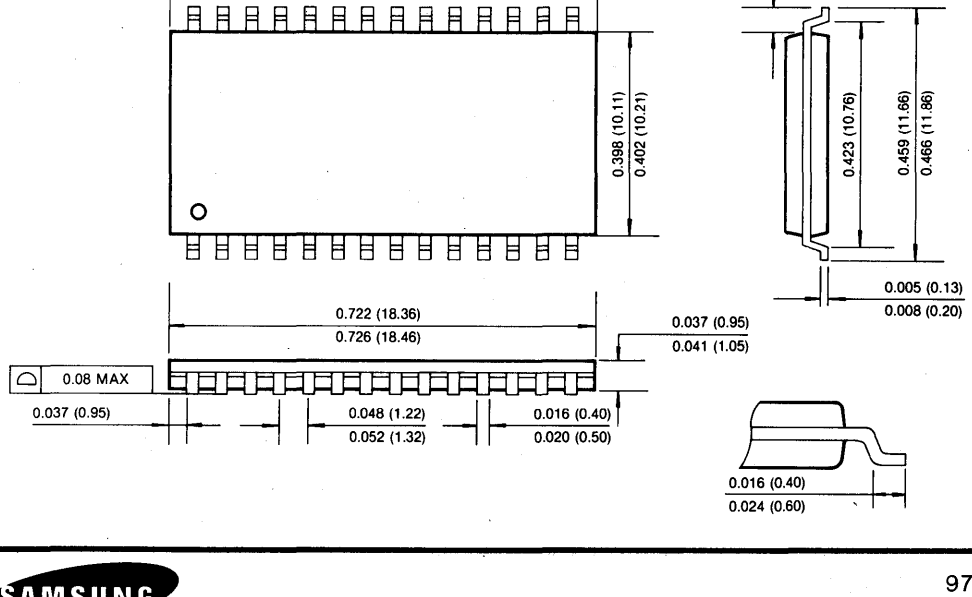
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



2M×8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
KM48V2104A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM48V2104A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM48V2104A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- **Fast Page Mode with Extended data out**
- **Self Refresh operation (LL-ver. only)**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **LVTTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+3.3V±0.3V power supply**
- **2048 cycles/32ms refresh (Normal)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

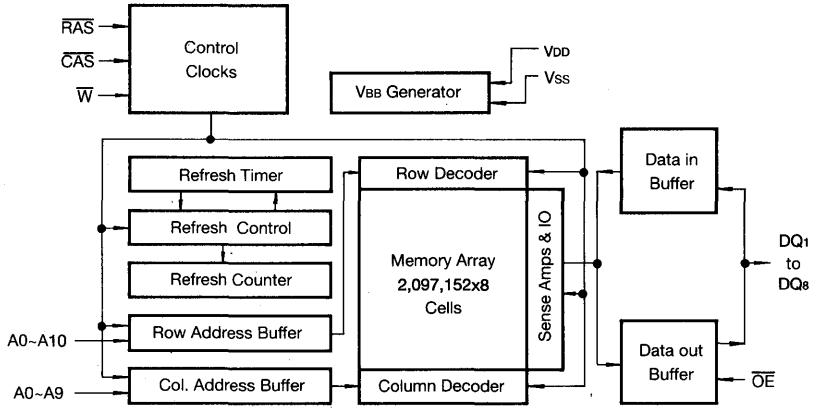
The Samsung KM48V2104A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit×8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48V2104A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48V2104A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

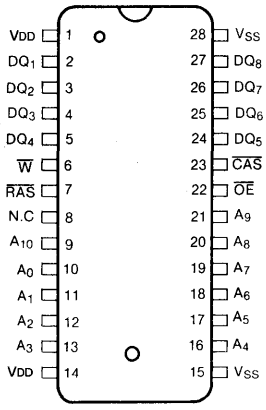
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

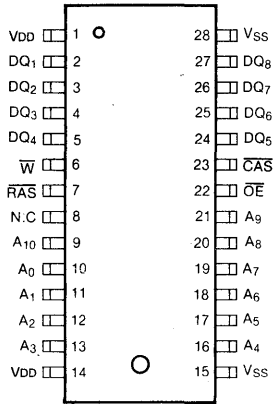
PIN CONFIGURATION (Top Views)

• KM48V2104 AJ/ALJ/ALLJ/ASLJ



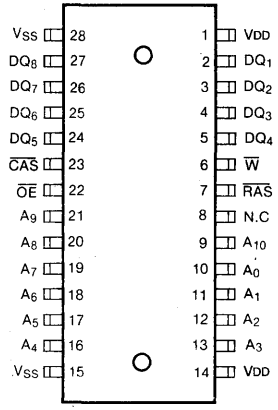
J : 400MIL

• KM48V2104 AT/ALT/ALLT/ASLT



T : 400MIL(Forward)

• KM48V2104 ATR/ALTR/ALLTR/ASLTR



TR : 400MIL(Reverse)

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ_{1-8}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{DD}	Power(+3.3V)
N.C	No Connection

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SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5~ 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5~ 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	Ios	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48V2104A/AL/ALL/ASL-6	I_{CC1}	-	100	mA
	KM48V2104A/AL/ALL/ASL-7			90	mA
	KM48V2104A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48V2104A	I_{CC2}	-	2	mA
	KM48V2104AL			1	mA
	KM48V2104ALL			1	mA
	KM48V2104ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM48V2104A/AL/ALL/ASL-6	I_{CC3}	-	100	mA
	KM48V2104A/AL/ALL/ASL-7			90	mA
	KM48V2104A/AL/ALL/ASL-8			80	mA
Hyper Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM48V2104A/AL/ALL/ASL-6	I_{CC4}	-	100	mA
	KM48V2104A/AL/ALL/ASL-7			90	mA
	KM48V2104A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM48V2104A	I_{CC5}	-	1	mA
	KM48V2104AL			300	μA
	KM48V2104ALL			200	μA
	KM48V2104ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48V2104A/AL/ALL/ASL-6	I_{CC6}	-	100	mA
	KM48V2104A/AL/ALL/ASL-7			90	mA
	KM48V2104A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{DD}-0.2V, Input Low Voltage (V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V, DQ_1~DQ_8=Don't Care, t_{RC}=62.5μs(L-Ver.) 125μs(SL-Ver.), t_{RAS}=t_{RAS} min.~300ns	KM48V2104AL	I_{CC7}	-	400	μA
	KM48V2104ASL			300	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{10}=V_{DD}-0.2V or 0.2V DQ_1~DQ_8=V_{DD}-0.2V, 0.2V or Open	KM48V2104ALL	I_{CCS}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz))

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{10})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Test Condition : V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{OEZ}	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	45		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	15	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	6
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	9
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	
Write command pulse width	t_{WP}	10		15		15		ns	6
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10		15		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal)	t_{REF}		32		32		32	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	60		70		75		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Hyper Page cycle time	t_{HPC}	24		29		34		ns	17
Hyper Page read-modify-write cycle time	t_{HPRWC}	71		86		96		ns	17
$\overline{CAS}$ precharge time (Hyper Page cycle)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	7,14
$\overline{OE}$ commend hold time	tOEH	15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	7,15
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	tWPE	5		5		5		ns	
Output buffer turn off delay from $\overline{RAs}$	tREZ	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from $\overline{W}$	tWEZ	3	15	3	20	3	20	ns	7,14
$\overline{W}$ to data delay	tWED	15		20		20		ns	
$\overline{RAS}$ pulse width (LL-ver)	tRASS	100		100		100		μs	16
$\overline{RAS}$ precharge time (LL-ver)	tRPS	110		130		150		ns	16
$\overline{CAS}$ hold time (LL-ver)	tCHS	-50		-50		-50		ns	16

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	15	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	50		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Hyper Page cycle time	tHPC	29		34		39		ns	
Hyper Page read-modify-write cycle time	tHPRWC	76		91		101		ns	
$\overline{RAS}$ pulse width (Hyper Page Cycle)	tRASP	65	200,000	75	200,000	85	200,000	ns	

TEST MODE CYCLE (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
$\overline{OE}$ access time	t_{OEA}		20		25		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	20		25		25		ns	

TEST MODE DESCRIPTION

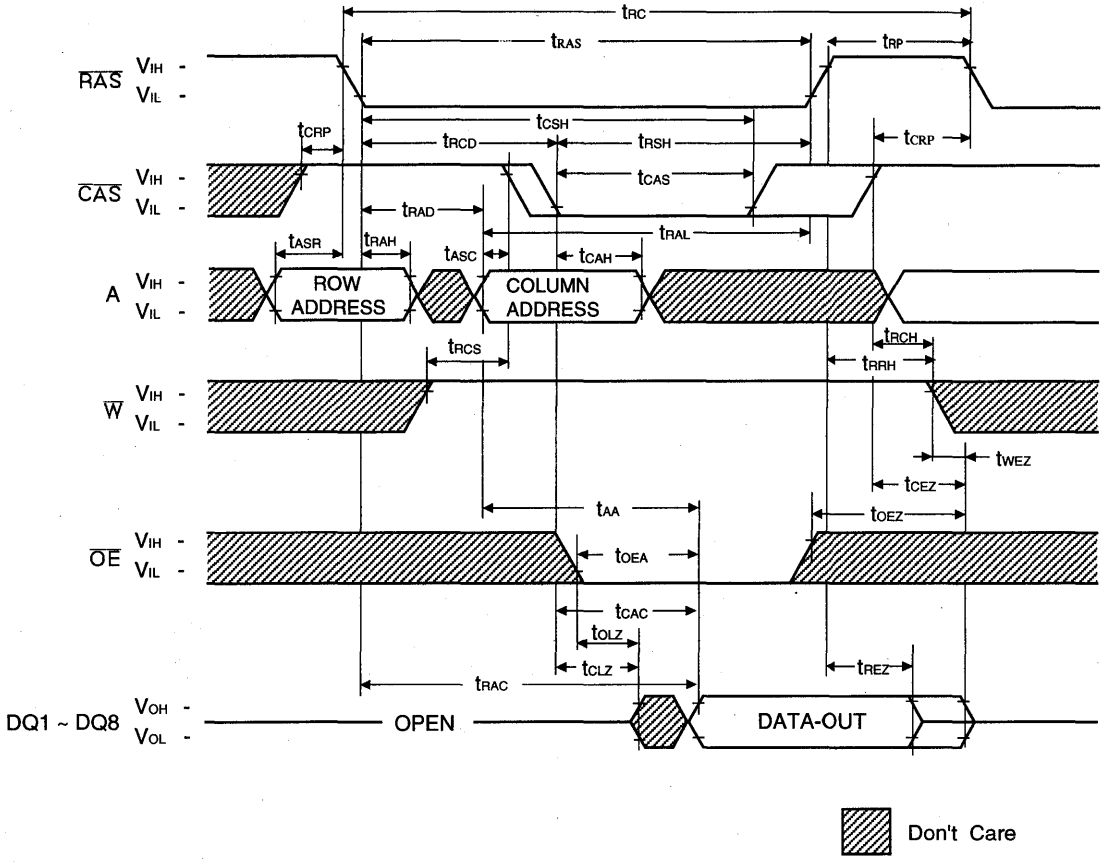
The KM48V2104A/AL/ALL/ASL is the CMOS DRAM organized 2,097,152 words by 8 bit internally organized 1,048,576 words by 16 bits. In " Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In Test Mode", the 2Mx8 DRAM can be tested as if it were a 1Mx8 DRAM. $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", And "$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" or "RAS Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" peforms the refresh operation with internal CBR refresh address counter. "Test Mode" function reduces test time (1/2 in cases of N test pattern).

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs, without t_{HPC} and t_{HPRWC}.
3. Measured with a load equivalent to 1TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{REZ}(max), t_{CEZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going
17. $t_{ASC} \geq t_{CP}$min, Assumn t_T=2.0ns

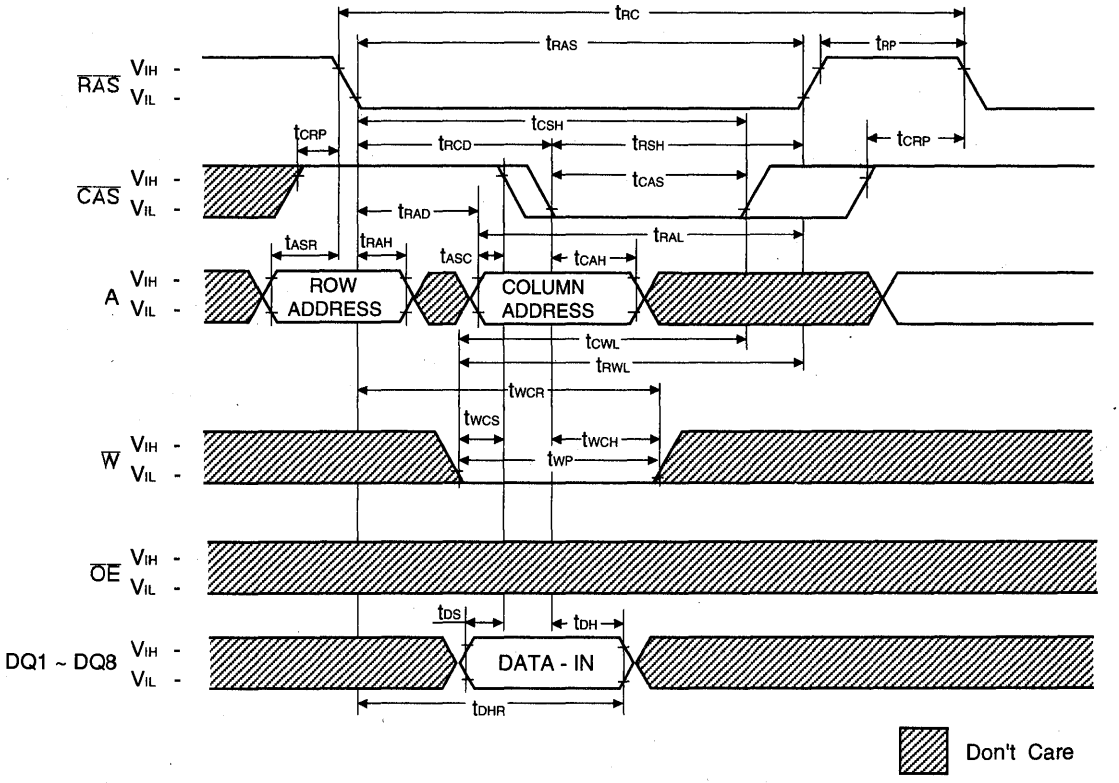
TIMING DIAGRAM

READ CYCLE



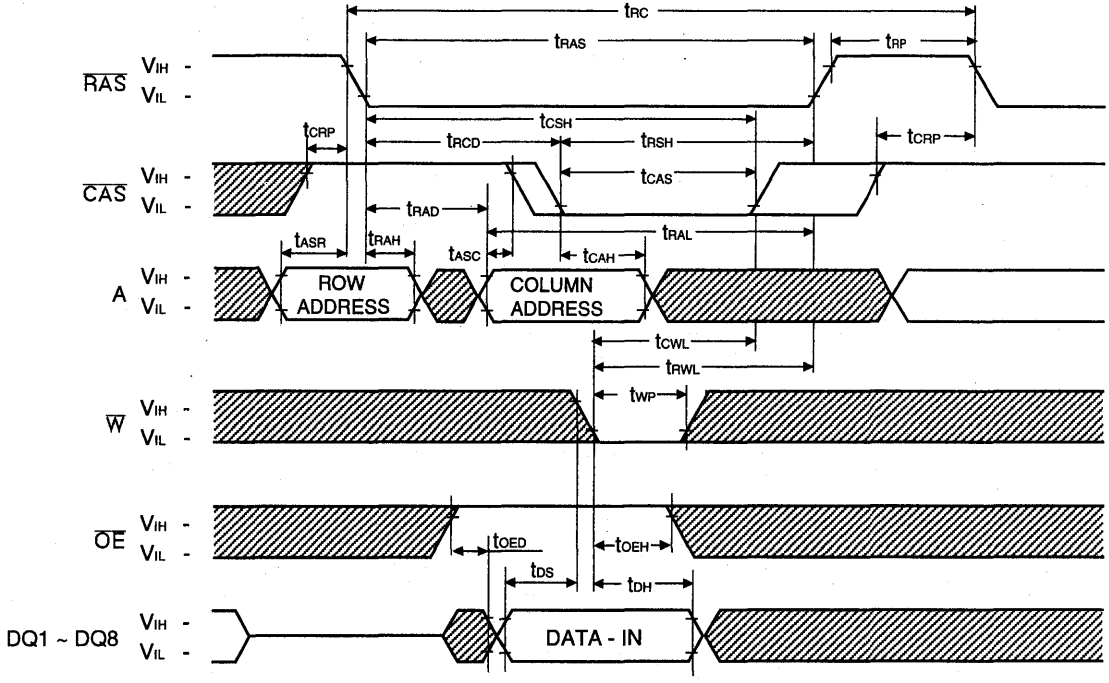
WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



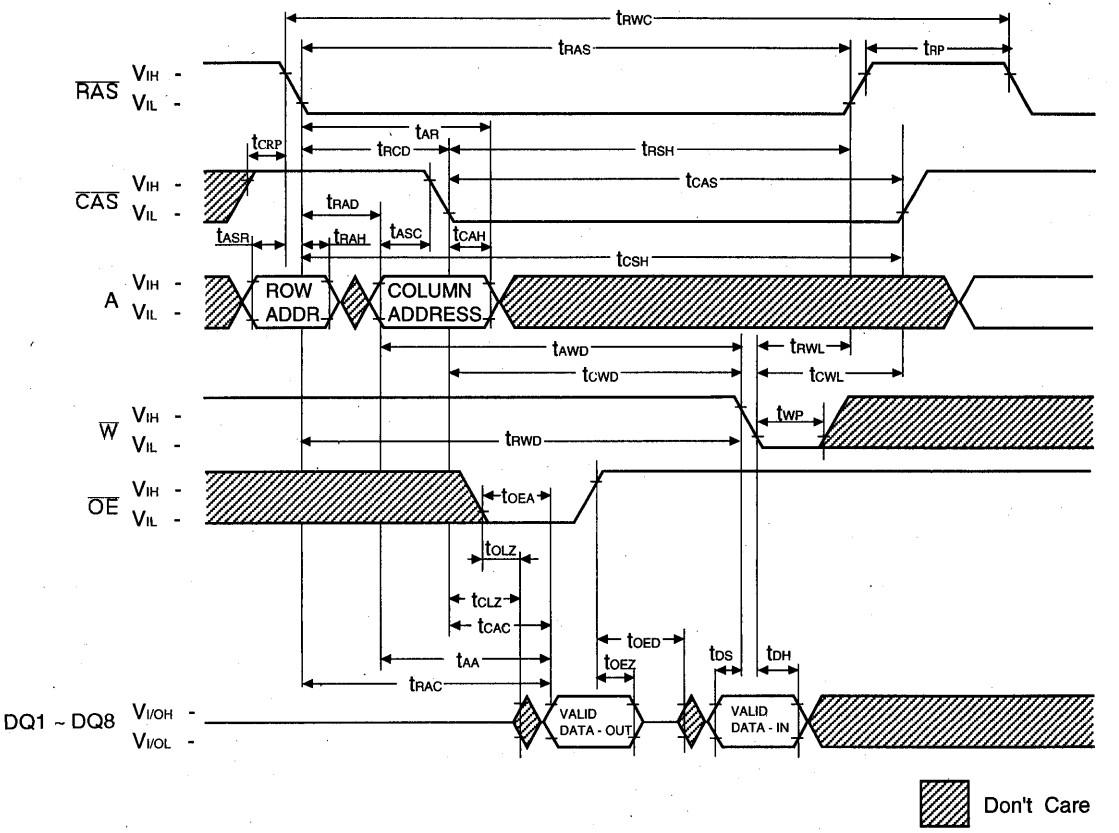
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

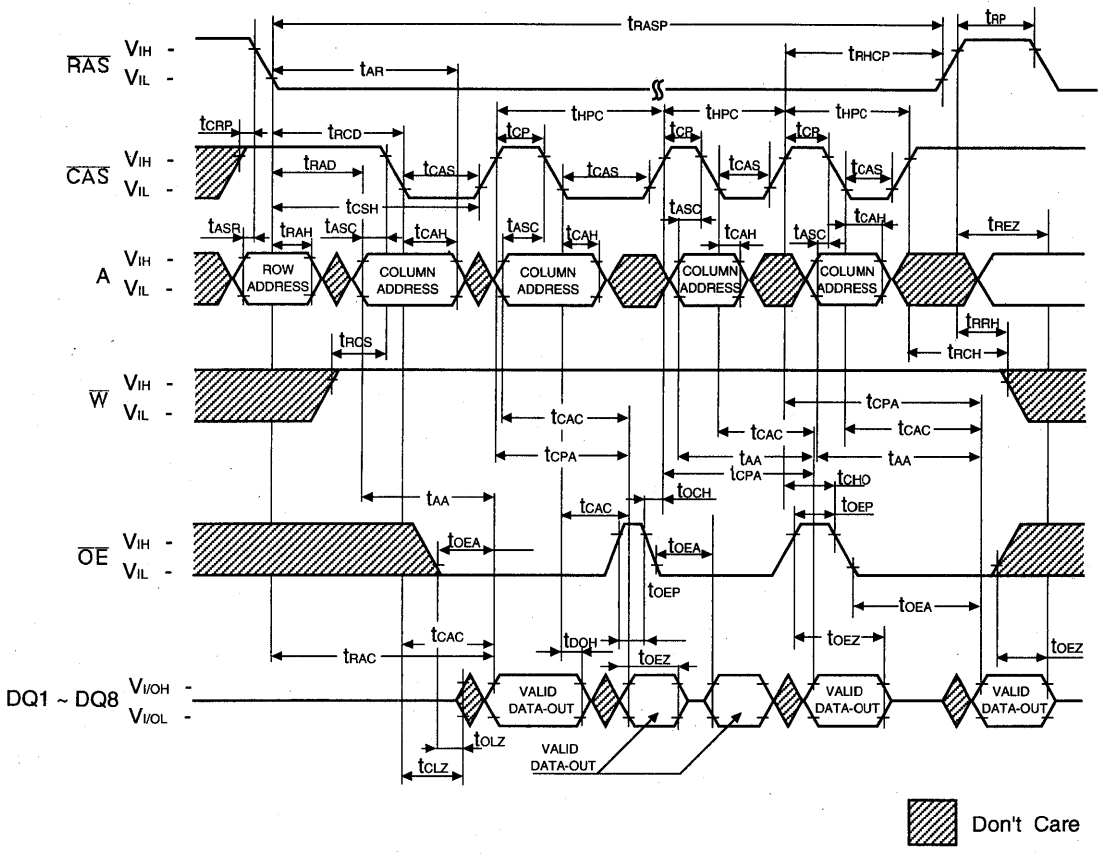


Don't Care

READ - MODIFY - WRITE CYCLE

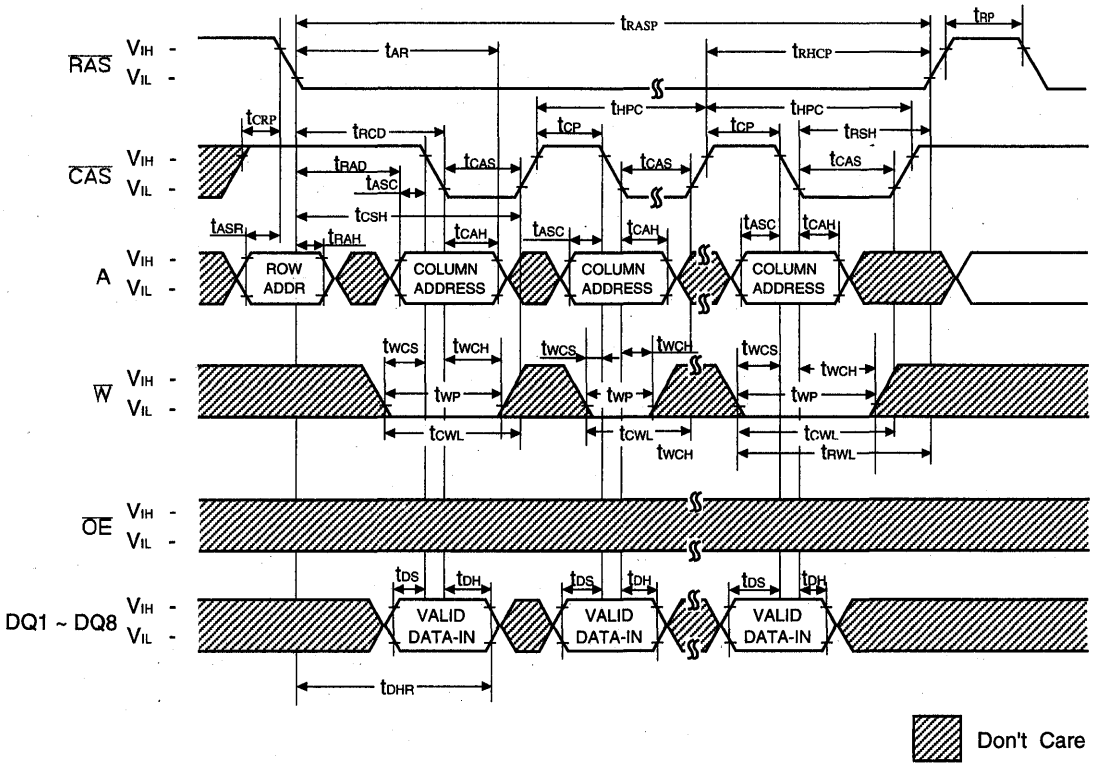


HYPER PAGE READ CYCLE

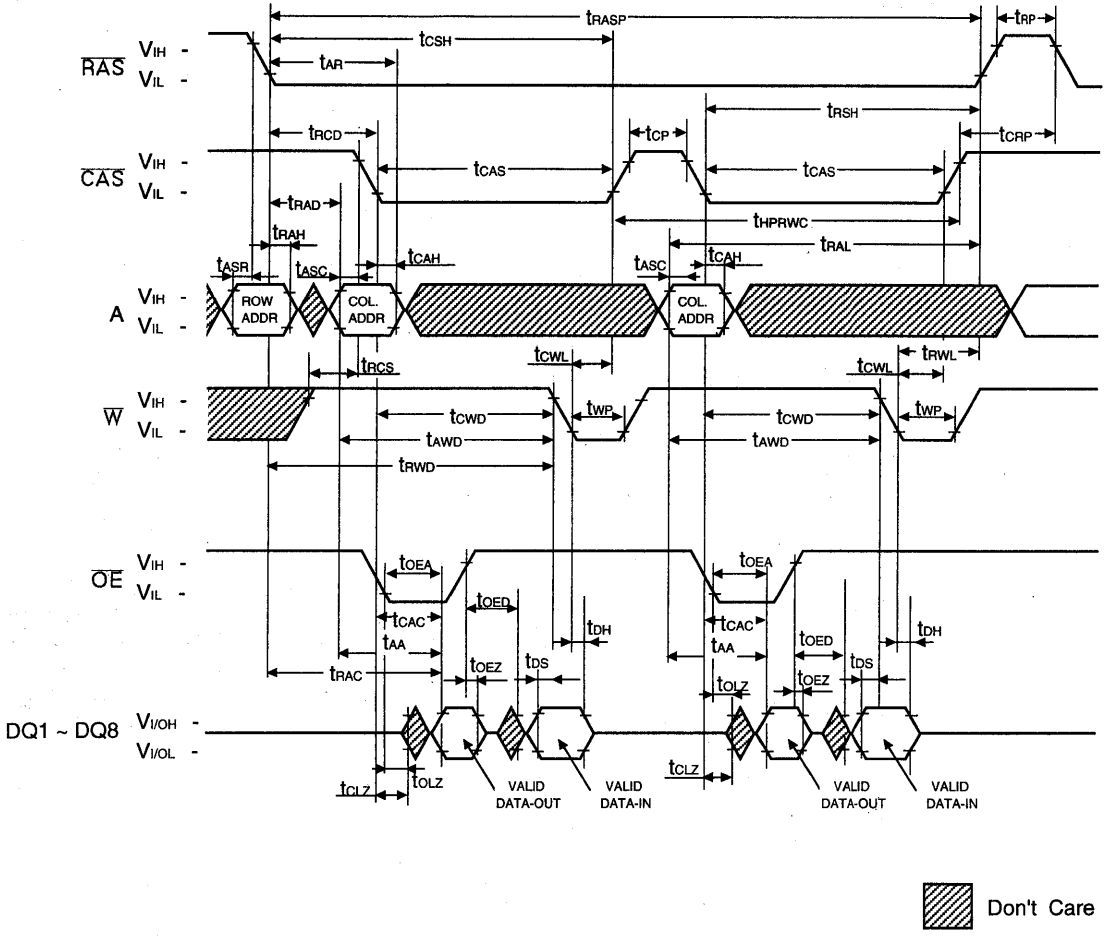


HYPER PAGE WRITE CYCLE (EARLY WRITE)

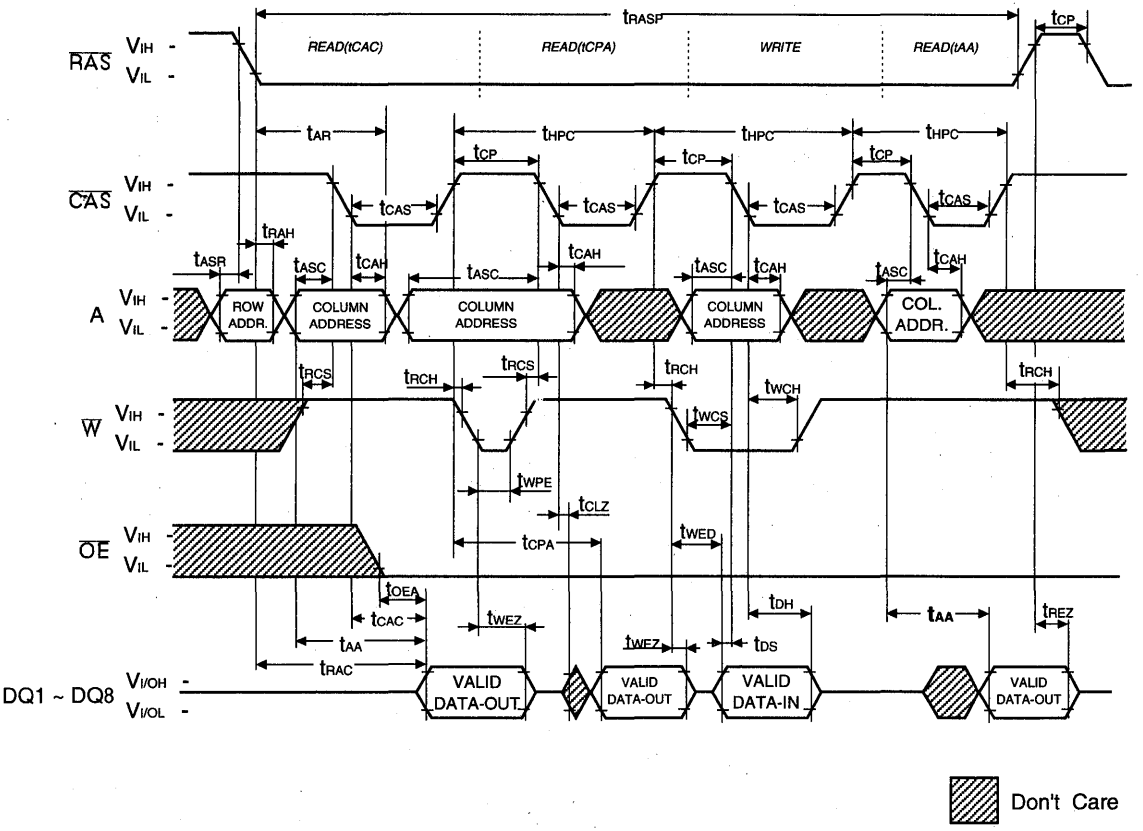
NOTE : D_{OUT} = Open



HYPER PAGE READ-MODIFY-WRITE CYCLE



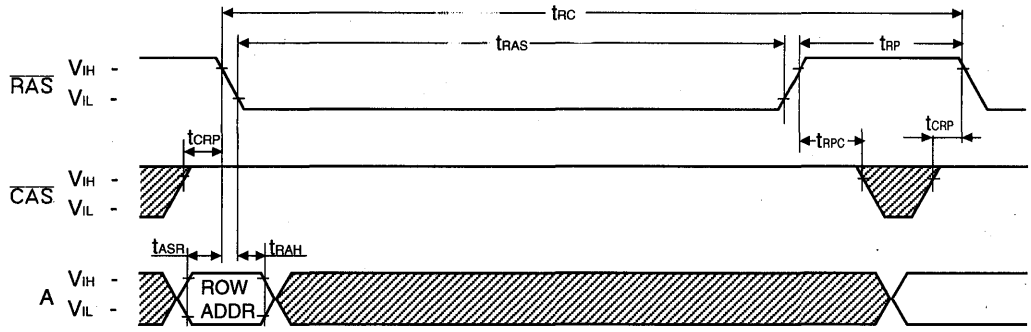
HYPER PAGE READ AND WRITE MIXED CYCLE



SAMSUNG ELECTRONICS

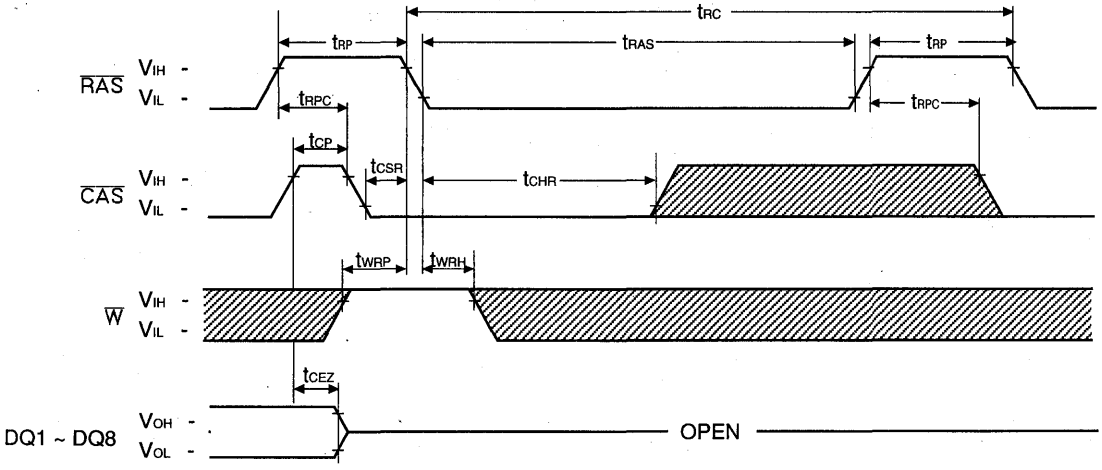
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open

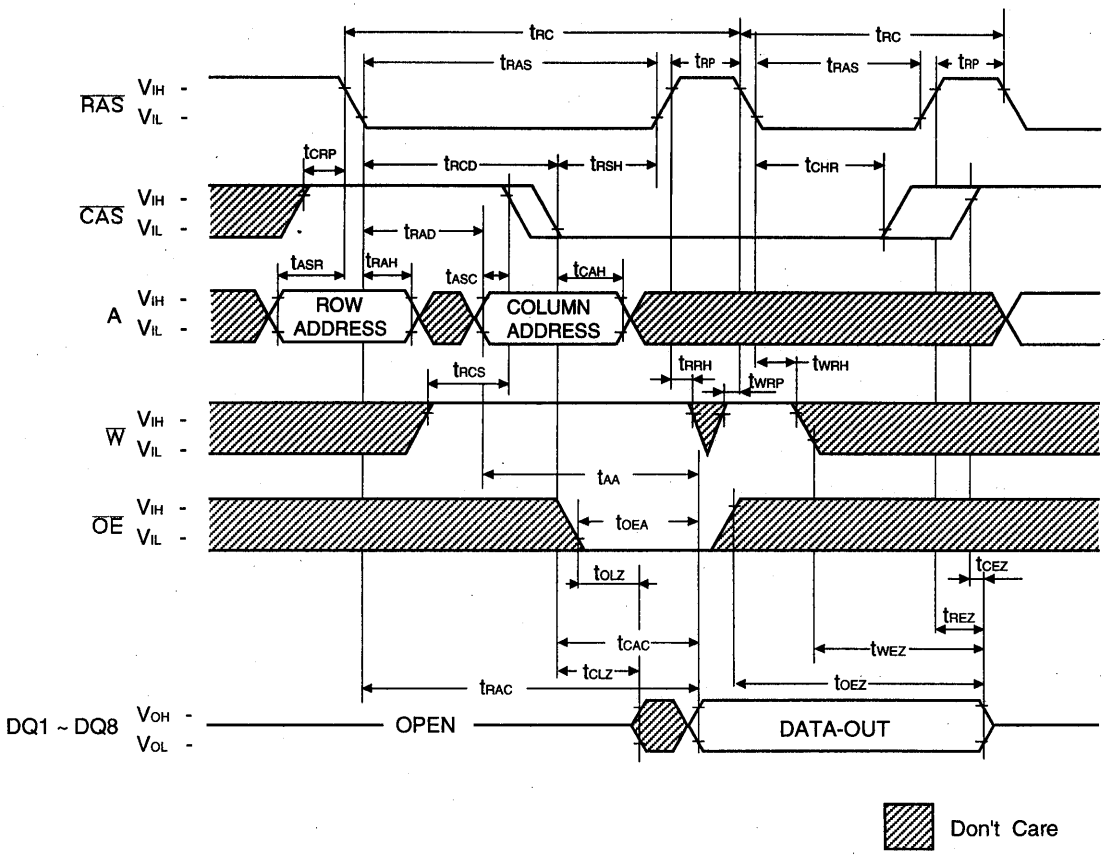


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

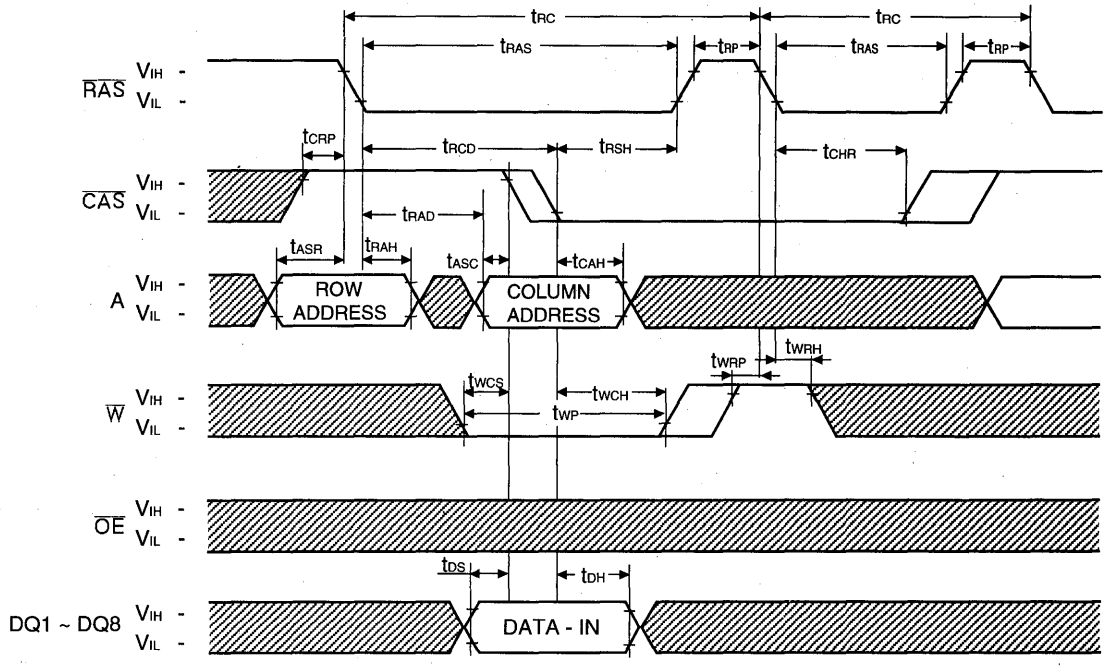


HIDDEN REFRESH CYCLE (READ)



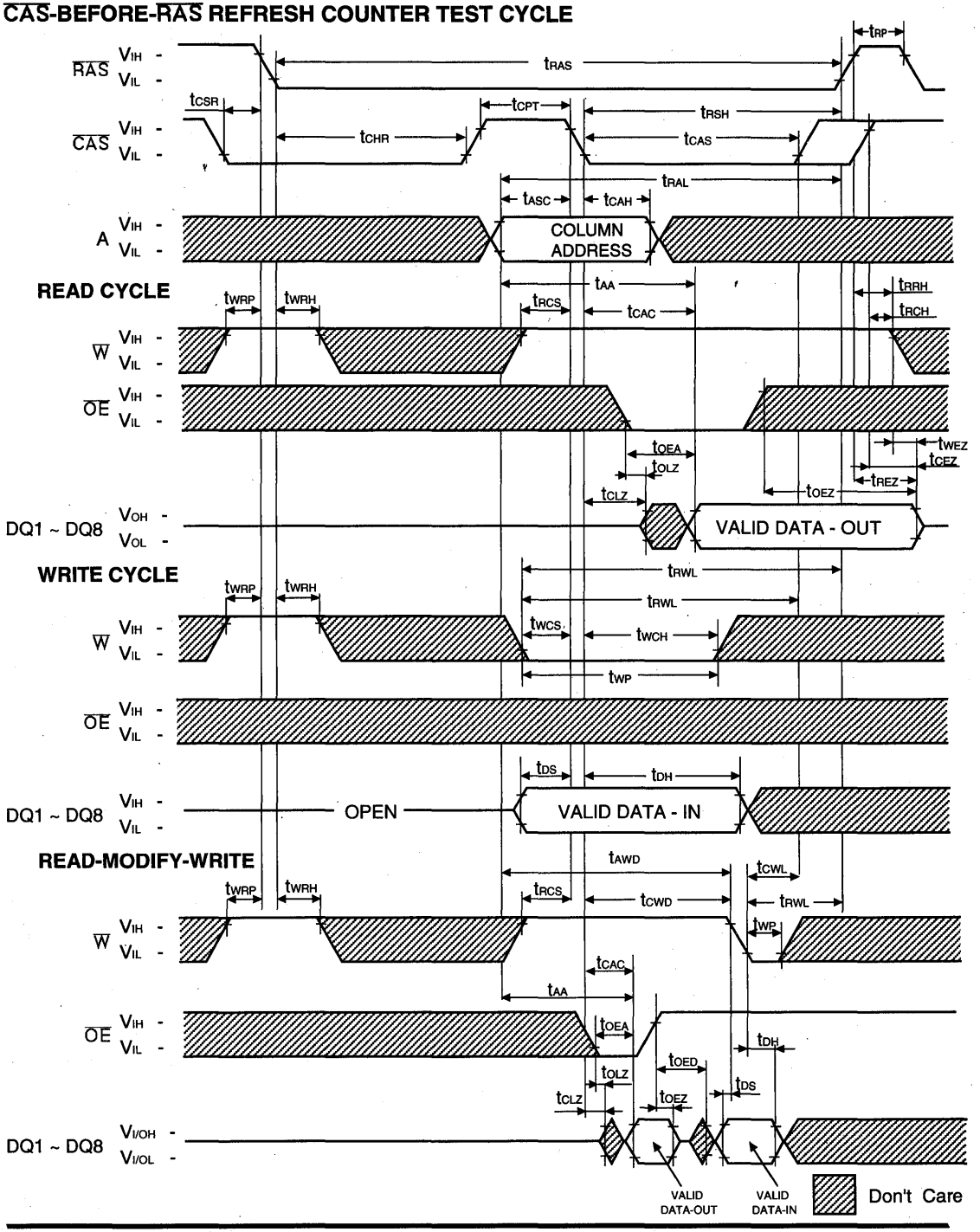
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



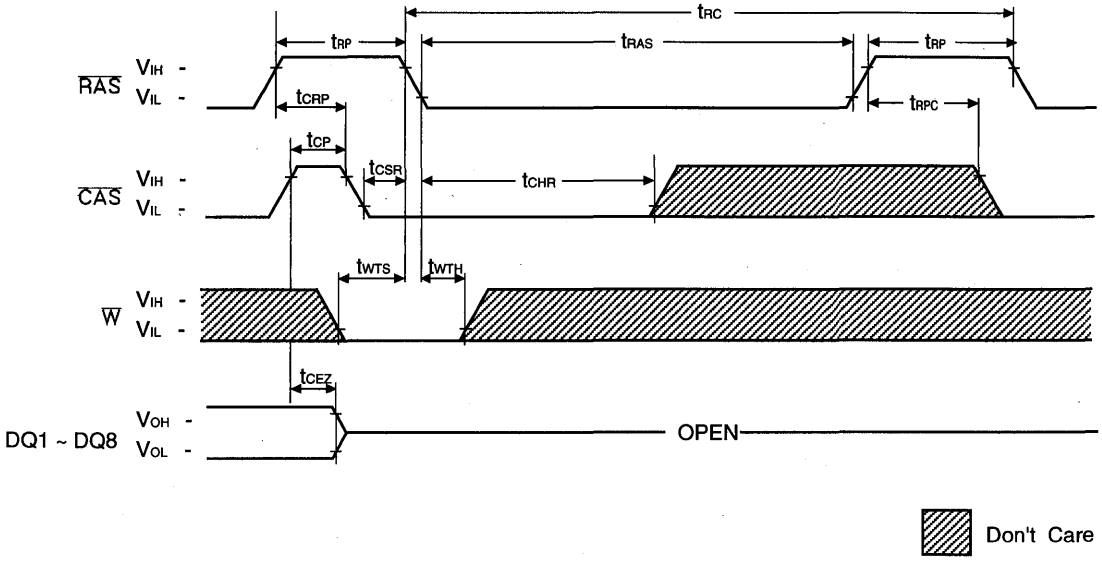
Don't Care

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't Care

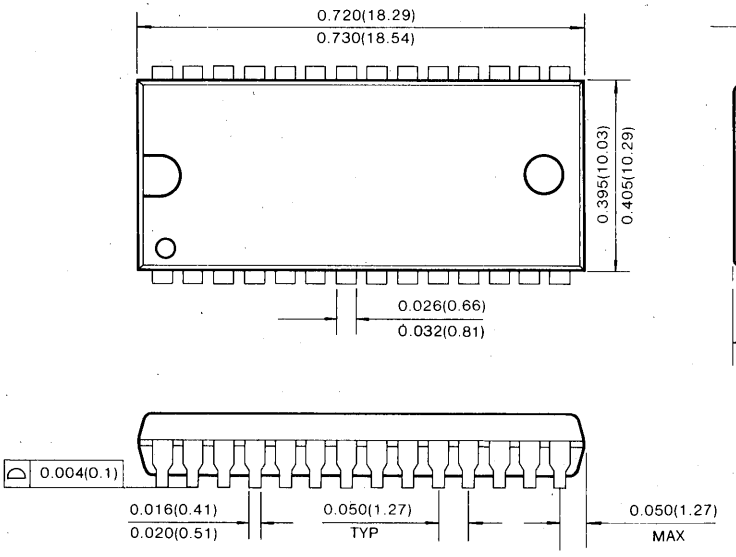


6

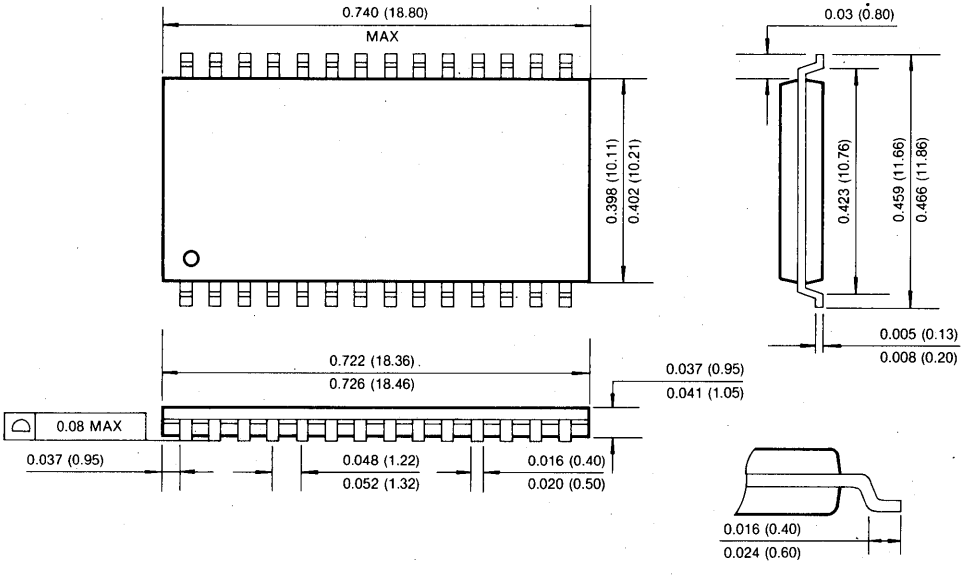
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



1M x 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM416C1000A-6/A-L6/A-F6	60ns	15ns	110ns
KM416C1000A-7/A-L7/A-F7	70ns	20ns	130ns
KM416C1000A-8/A-L8/A-F8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **RAS-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +5V±10% power supply**
- **Refresh Cycle**
  - **4096 cycle/64ms (Normal)**
  - **4096 cycle/128ms (L-version)**
  - **4096 cycle/128ms (F-version)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP II packages**

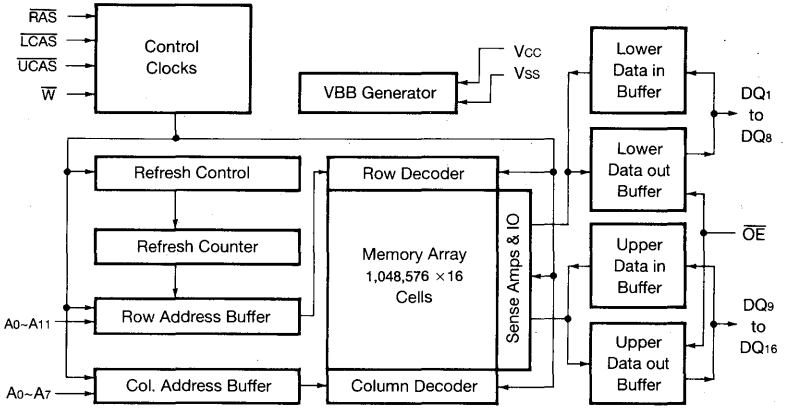
GENERAL DESCRIPTION

The Samsung KM416C1000A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

The KM416C1000A/A-L/A-F features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416C1000A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

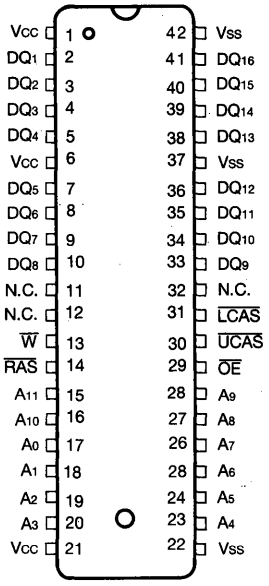
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

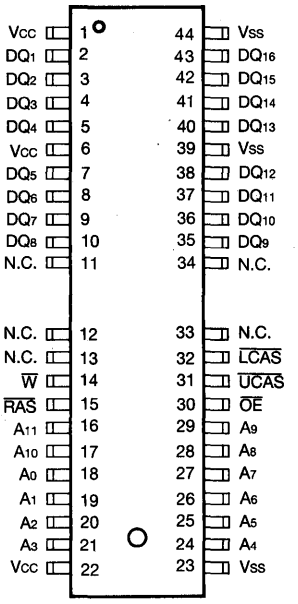
PIN CONFIGURATION (Top Views)

• KM416C1000AJ



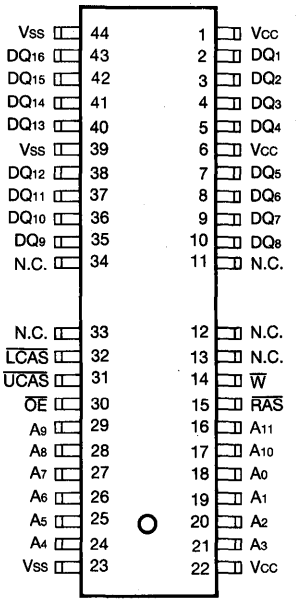
(SOJ)

• KM416C1000AT



(TSOP(II)-Forword)

• KM416C1000AR



(TSOP(II)-Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-16	Data In/Out
Vss	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
Vcc	Power(+5V)
N.C.	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 ~ + 7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 ~ + 7	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{RC}=min.)	KM416C1000A-6/A-L6/A-F6 KM416C1000A-7/A-L7/A-F7 KM416C1000A-8/A-L8/A-F8	I_{CC1}	-	100 90 80	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})	KM416C1000A KM416C1000A-L KM416C1000A-F	I_{CC2}	-	2 1 1	mA mA mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM416C1000A-6/A-L6/A-F6 KM416C1000A-7/A-L7/A-F7 KM416C1000A-8/A-L8/A-F8	I_{CC3}	-	100 90 80	mA mA mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC}=min.)	KM416C1000A-6/A-L6/A-F6 KM416C1000A-7/A-L7/A-F7 KM416C1000A-8/A-L8/A-F8	I_{CC4}	-	100 90 80	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)	KM416C1000A KM416C1000A-L KM416C1000A-F	I_{CC5}	-	1 300 200	mA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC}=min.)	KM416C1000A-6/A-L6/A-F6 KM416C1000A-7/A-L7/A-F7 KM416C1000A-8/A-L8/A-F8	I_{CC6}	-	100 90 80	mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V, Input Low Voltage(V_{IL})=0.2V $\overline{UCAS}$, $\overline{LCAS}$=0.2V D_{IN}=Don't Care, t_{RC}=31.25μs (L-Version) t_{RAS}=t_{RAS} min~300ns	KM416C1000A-L	I_{CC7}	-	450	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL} $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{CC}-0.2V or 0.2V DQ_1-DQ_{16}=V_{CC}-0.2V or 0.2V or Open	KM416C1000A-F	I_{CCS}	-	250	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 V)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once while page mode cycle time t_{PC}.

CAPACITANCE (T_A=25°C, V_{CC}=5V. f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~11)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

(Test condition : V_{IH}/V_{IL}=2.4V/0.8V, V_{OH}/V_{OL}=2.4V/0.4V, Output Loading C_L=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command set-up time	t_{WCS}	0		0		0		ns	8
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		50		55		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	10		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64	ms	
Refresh period (L-version)	t_{REF}		128		128		128	ms	
Refresh period (F-version)	t_{REF}		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		95		105		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	80		95		100		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

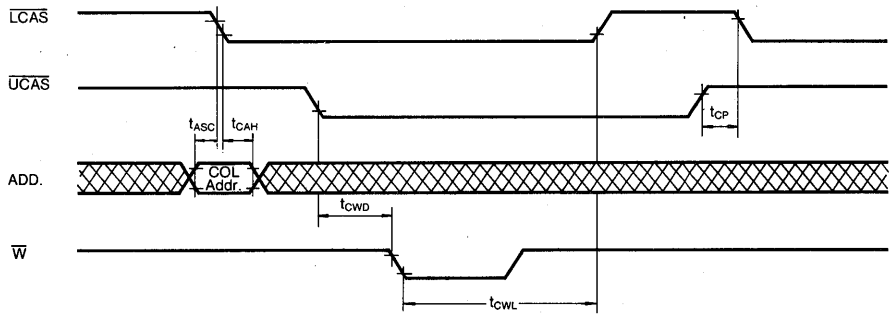
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
$\overline{RAS}$ pulse width (F-ver)	tRASS	100		100		100		μs	19
$\overline{RAS}$ precharge time (F-ver)	tRPS	110		130		150		ns	19
$\overline{CAS}$ hlod time (F-ver)	tCHS	-50		-50		-50		ns	19

KM416C1000A/A-L/A-F Truth Table

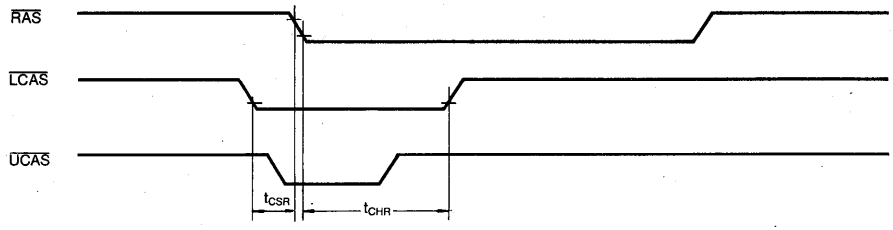
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

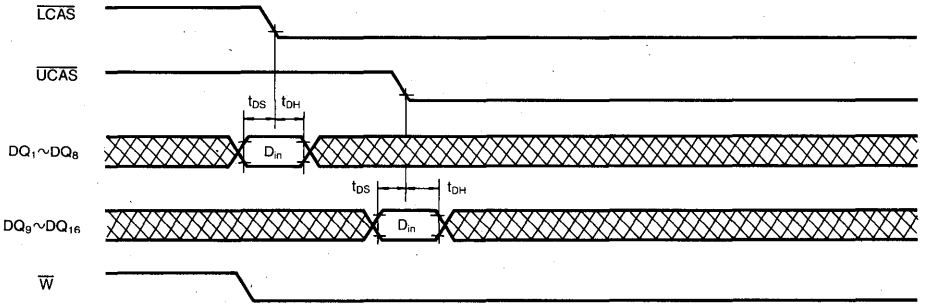
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
17. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



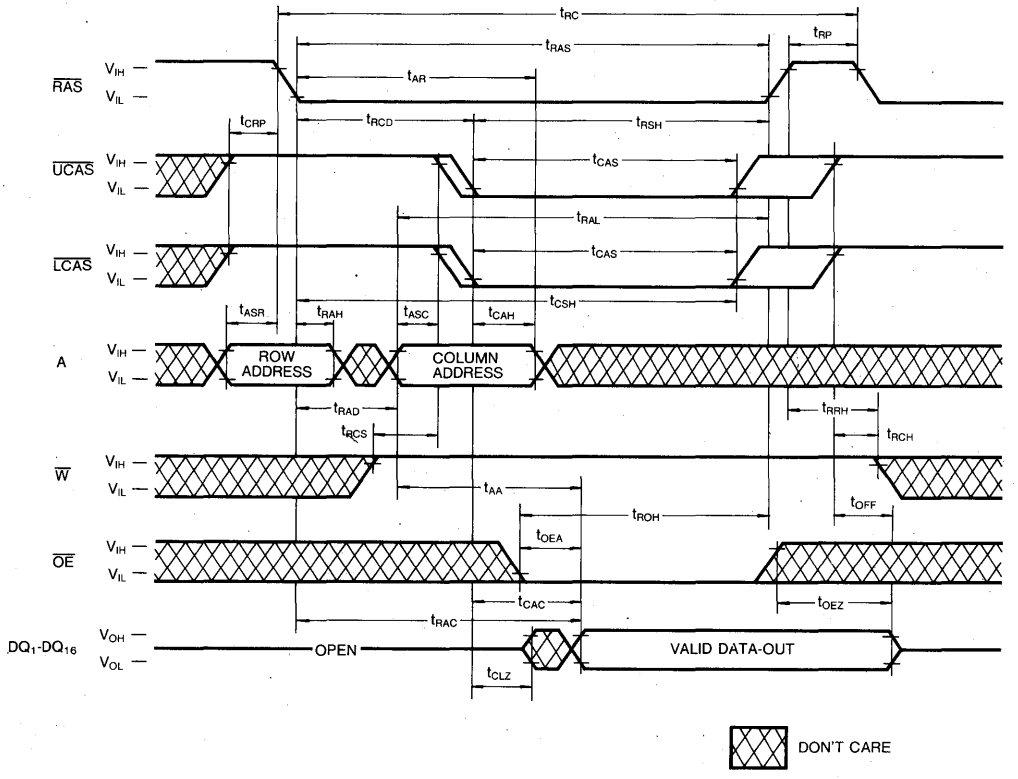
18. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim8)}$, upper byte $D_{in(9\sim16)}$



19. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh speciffication (F-version)

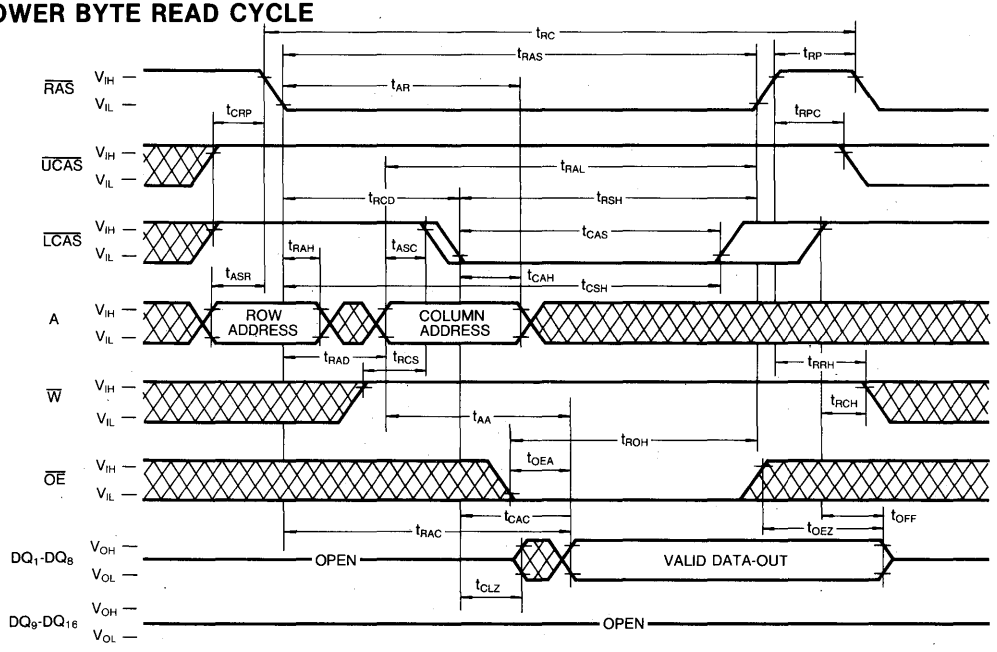
TIMING DIAGRAMS

WORD READ CYCLE

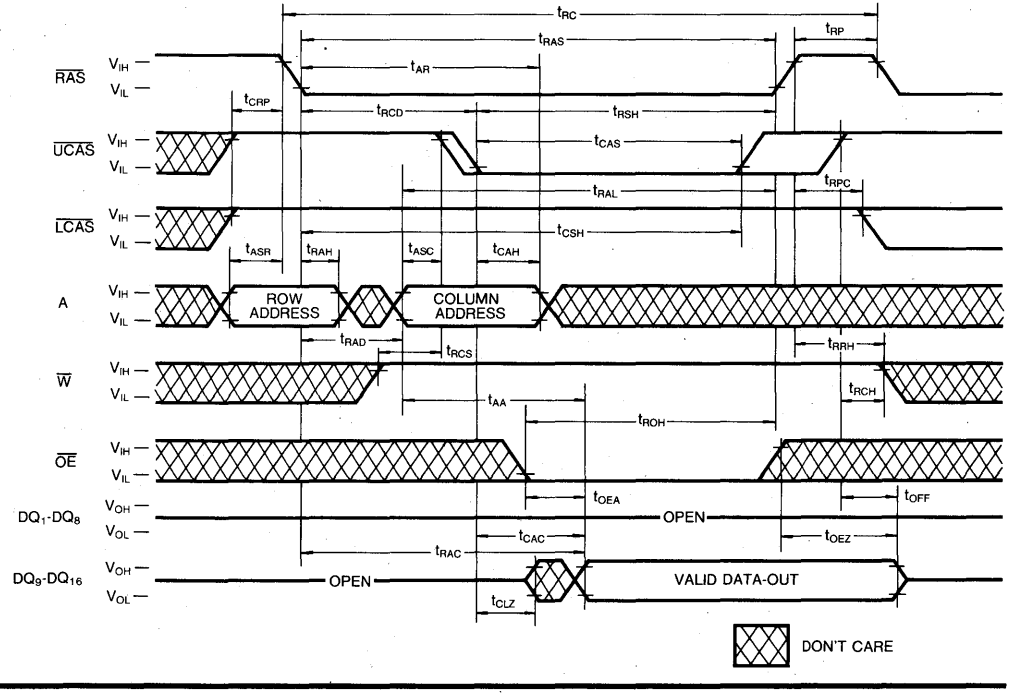


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE



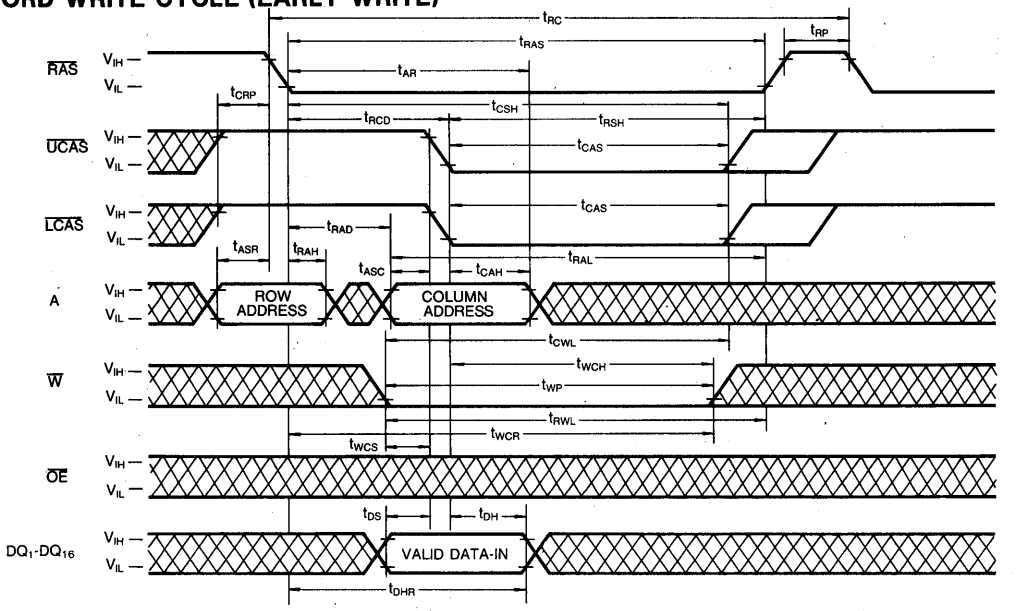
UPPER BYTE READ CYCLE



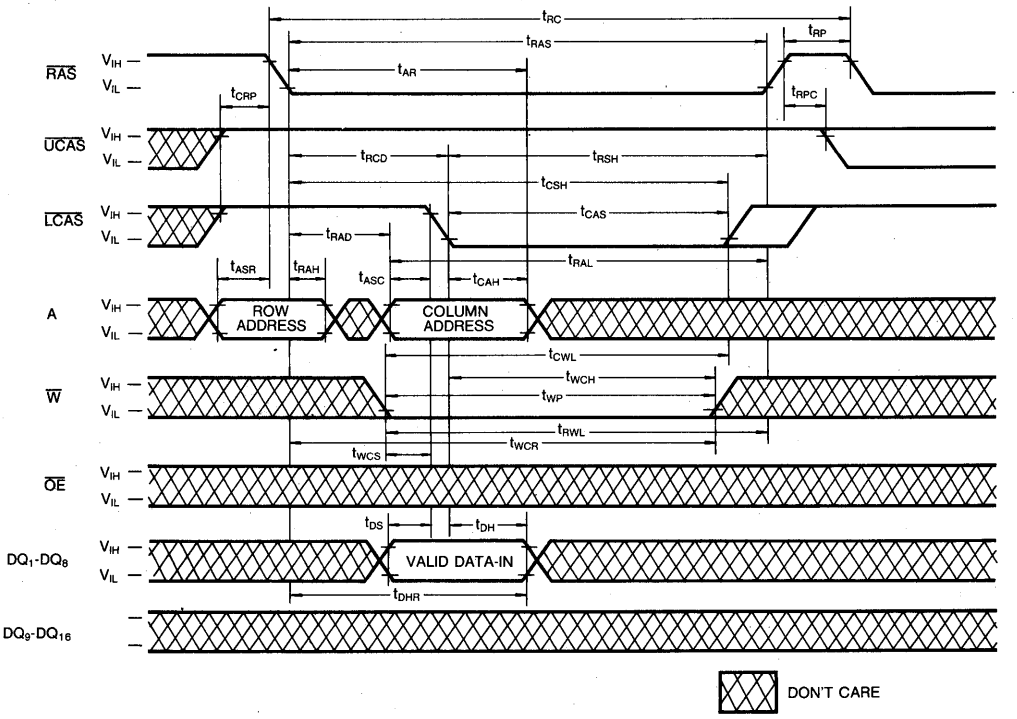
6

TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)



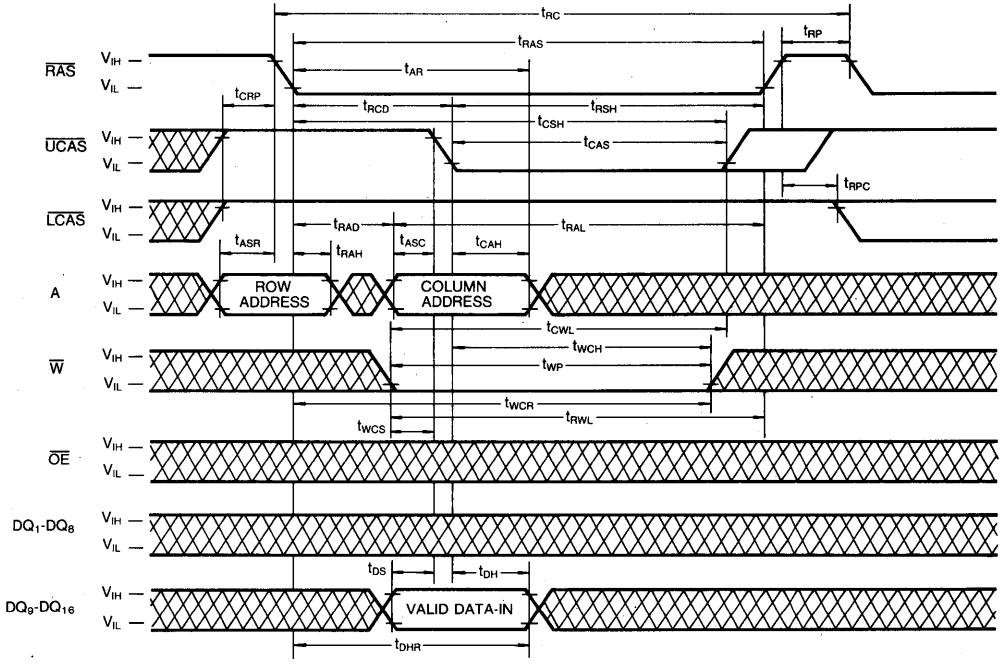
LOWER BYTE WRITE CYCLE (EARLY WRITE)



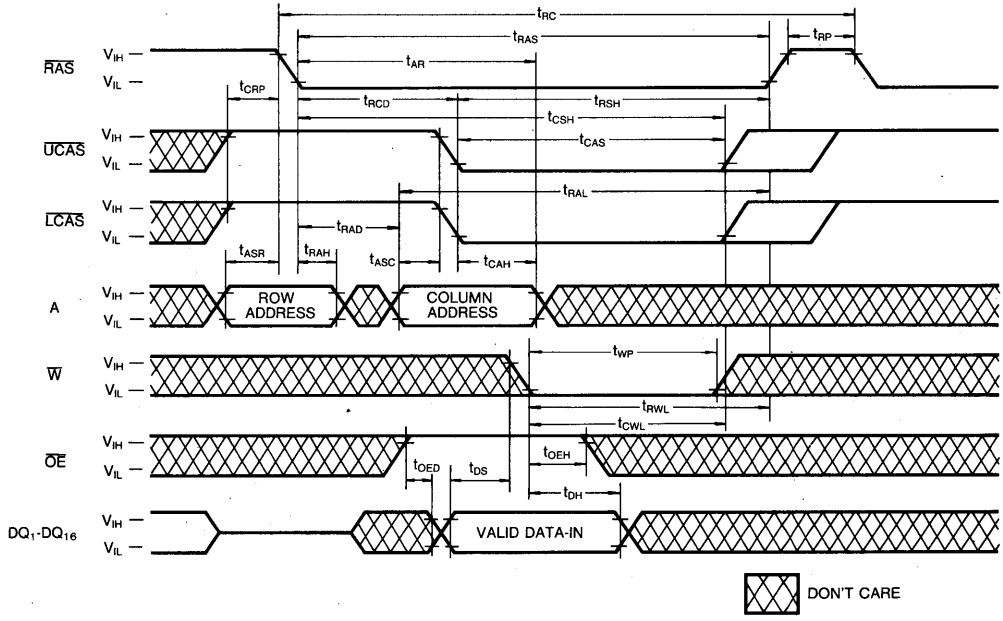
DON'T CARE

TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)



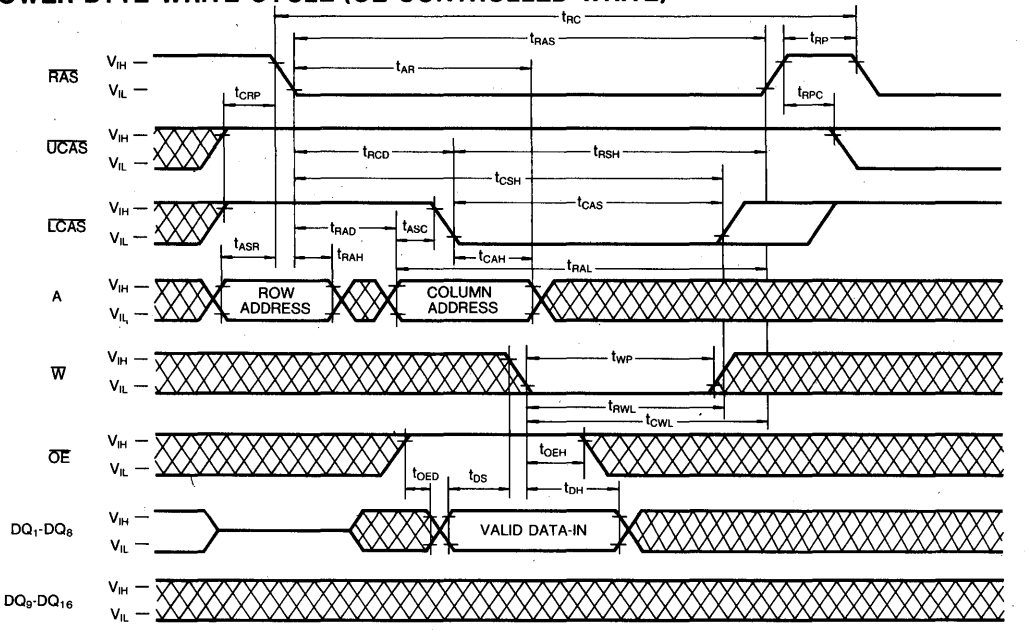
WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



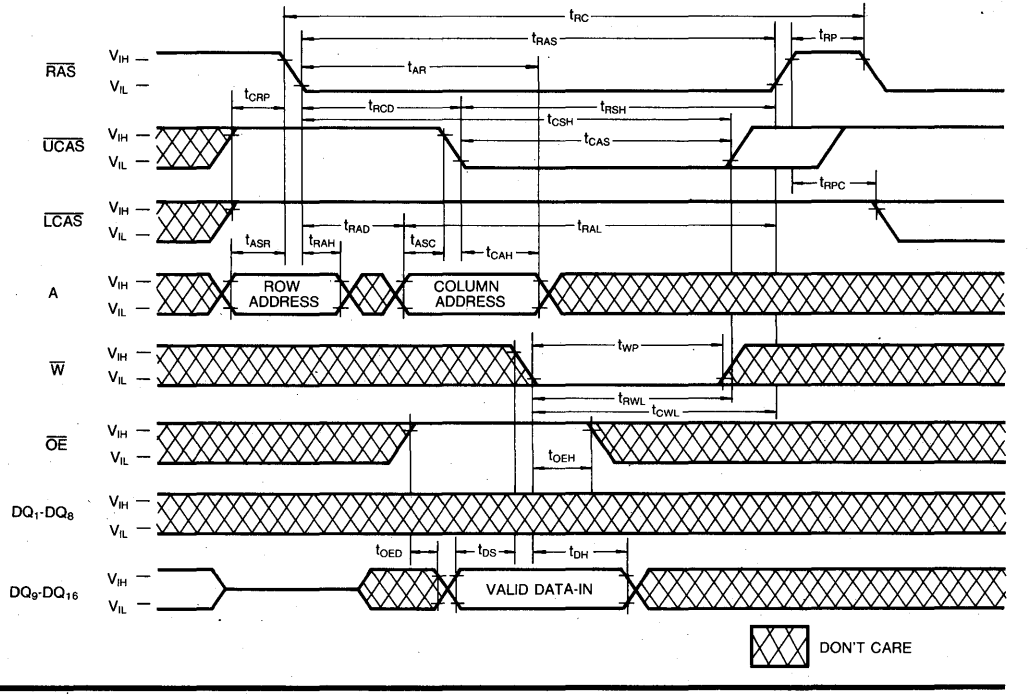
6

TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

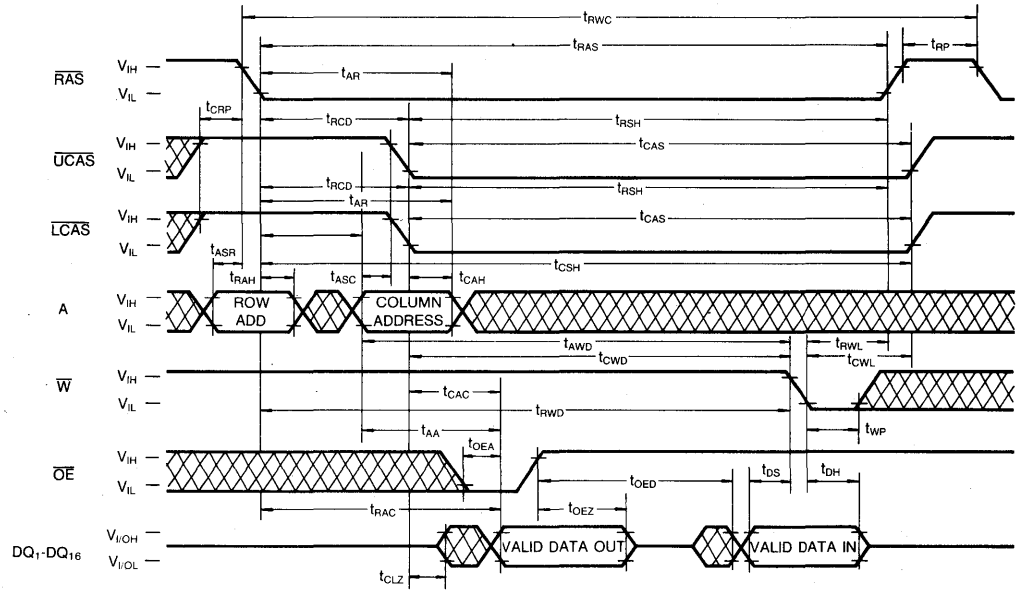


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

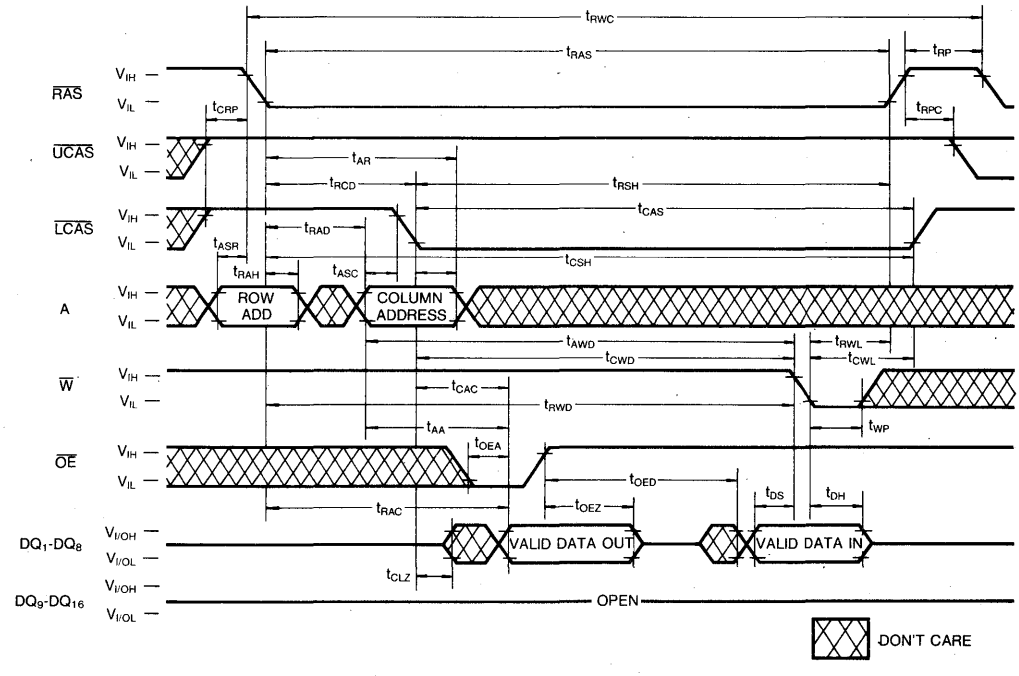


TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

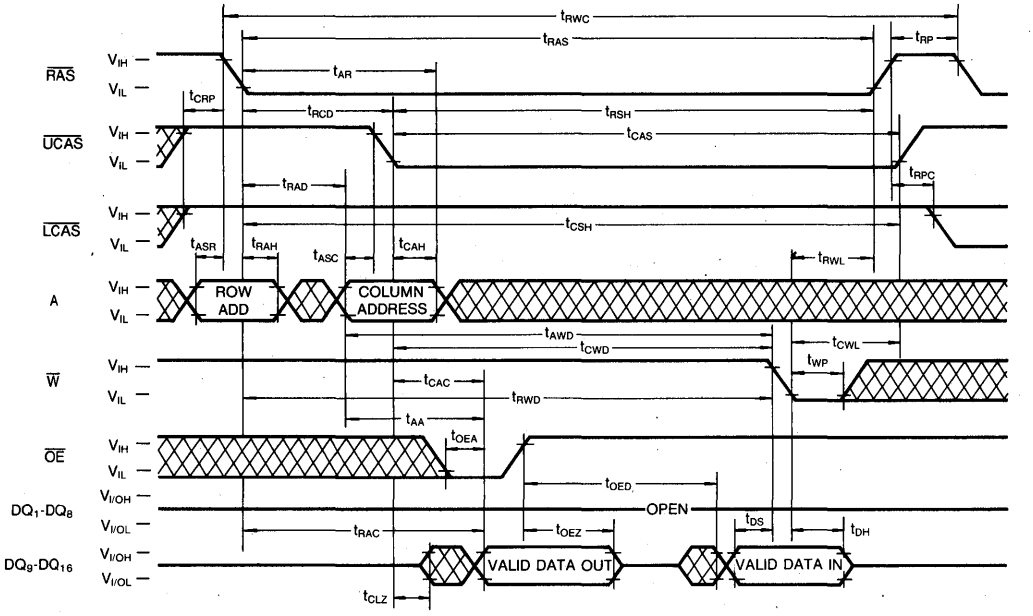


READ-MODIFY-LOWER-BYTE-WRITE CYCLE

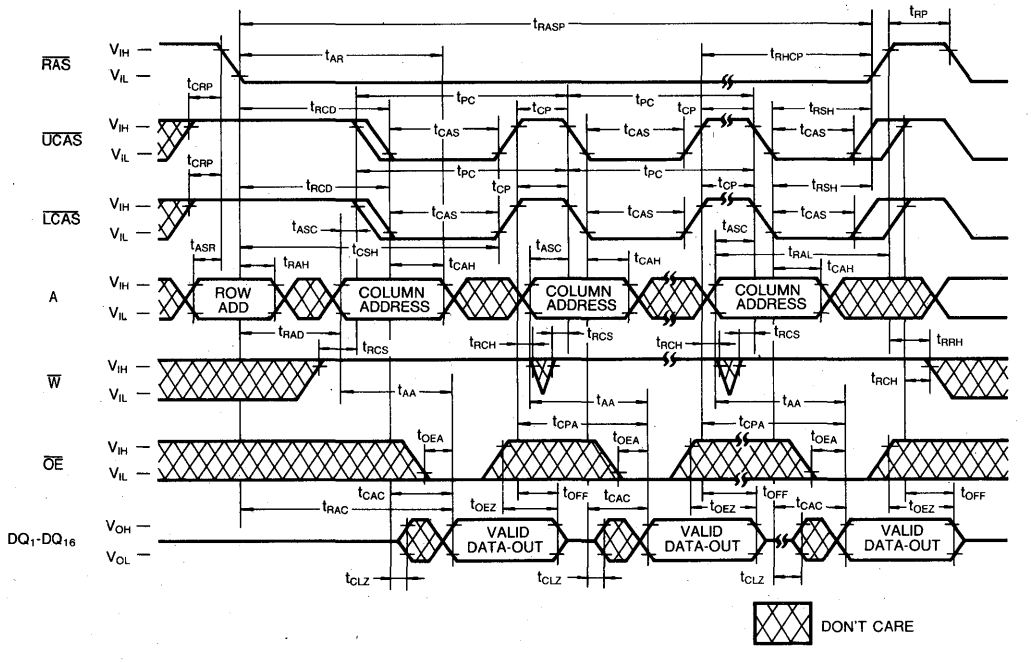


TIMING DIAGRAMS (Continued)

READ-MODIFY-UPPER-BYTE-WRITE CYCLE

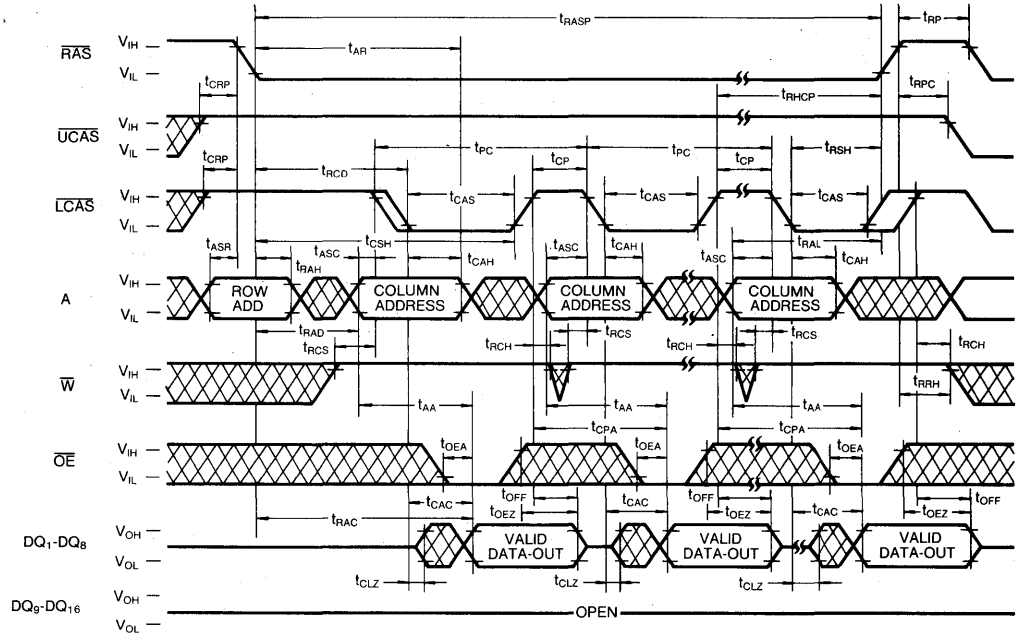


FAST PAGE MODE WORD READ CYCLE

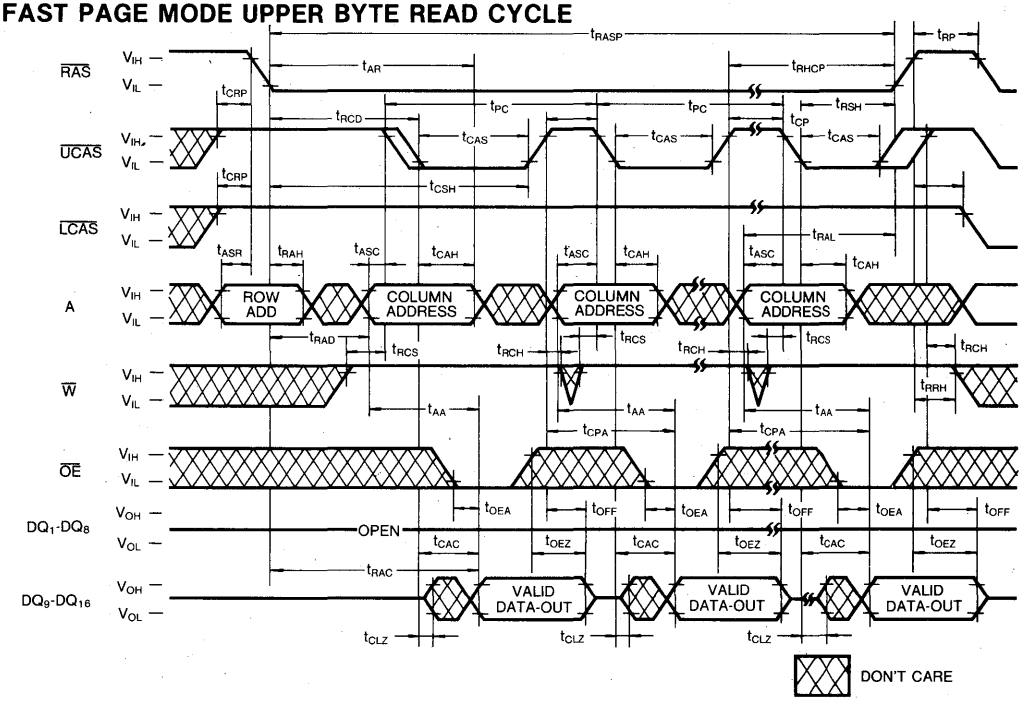


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE



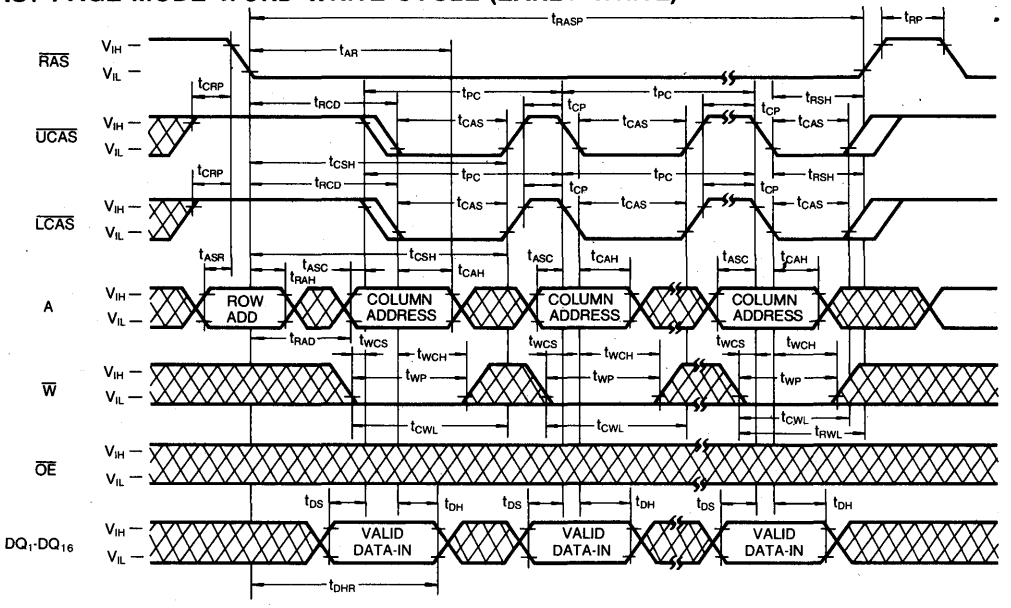
FAST PAGE MODE UPPER BYTE READ CYCLE



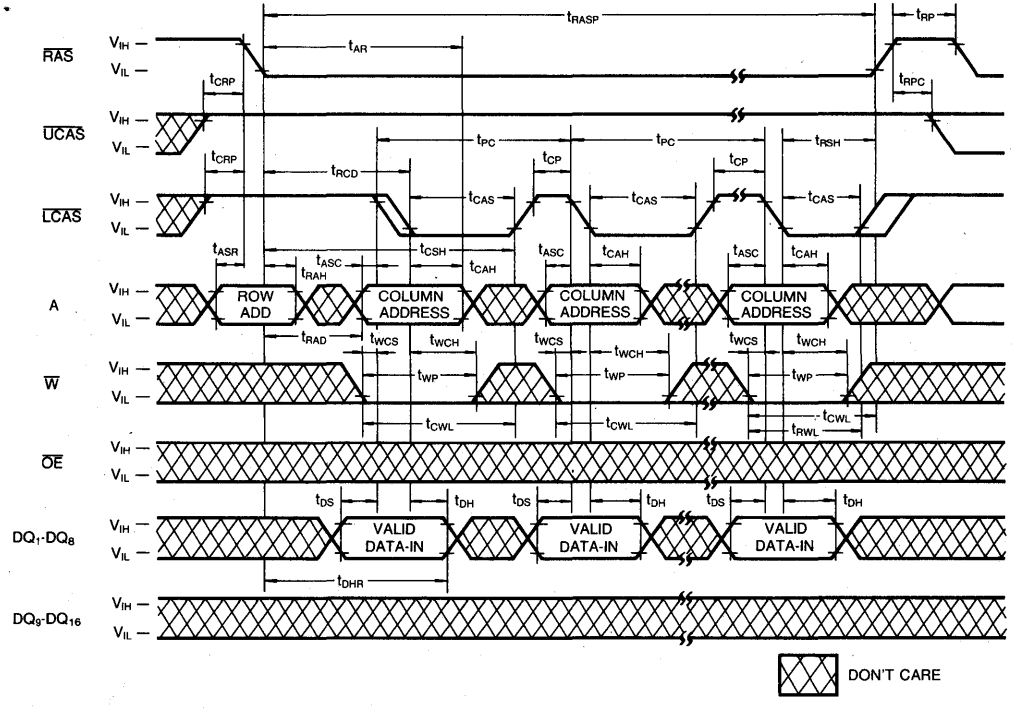
6

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

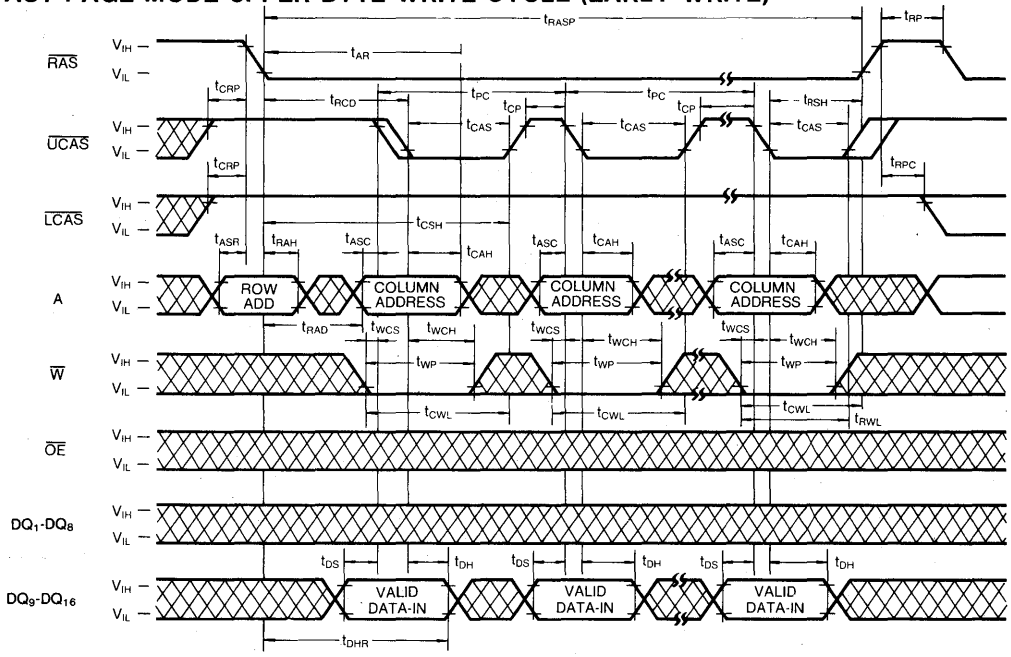


FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)

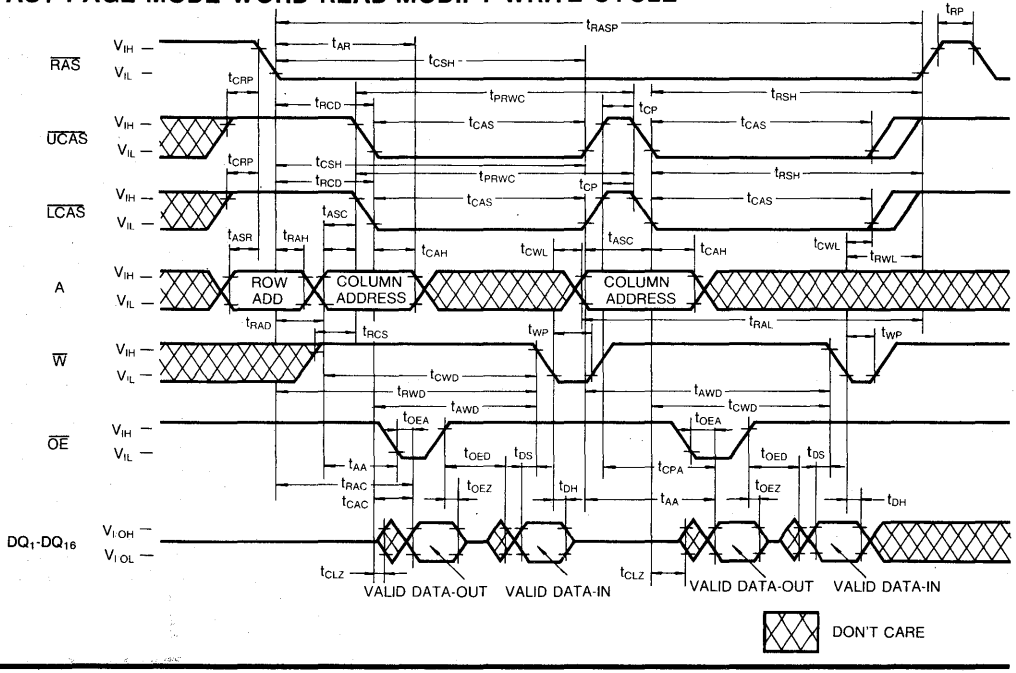


TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)



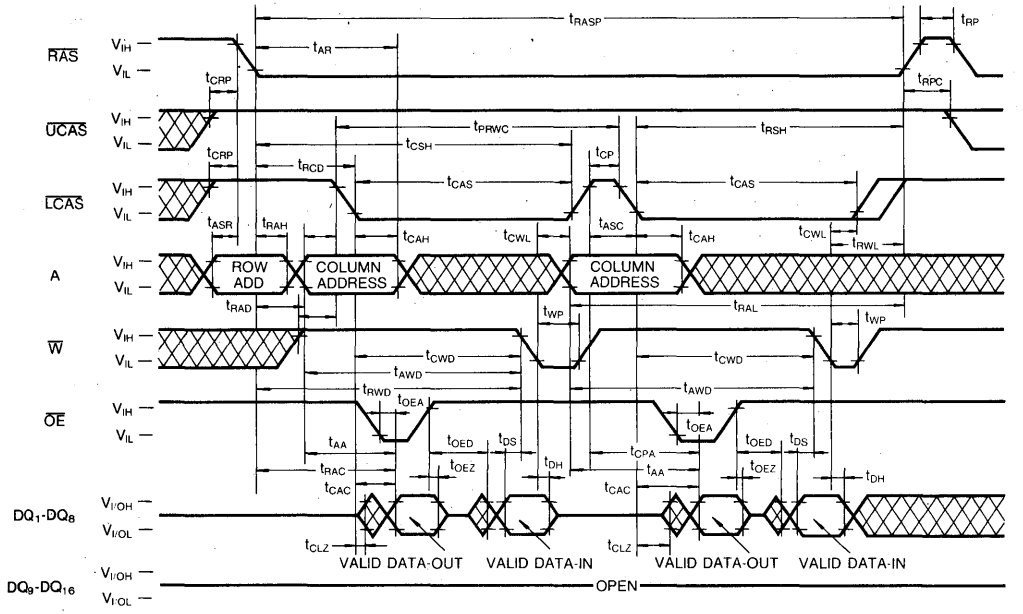
FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE



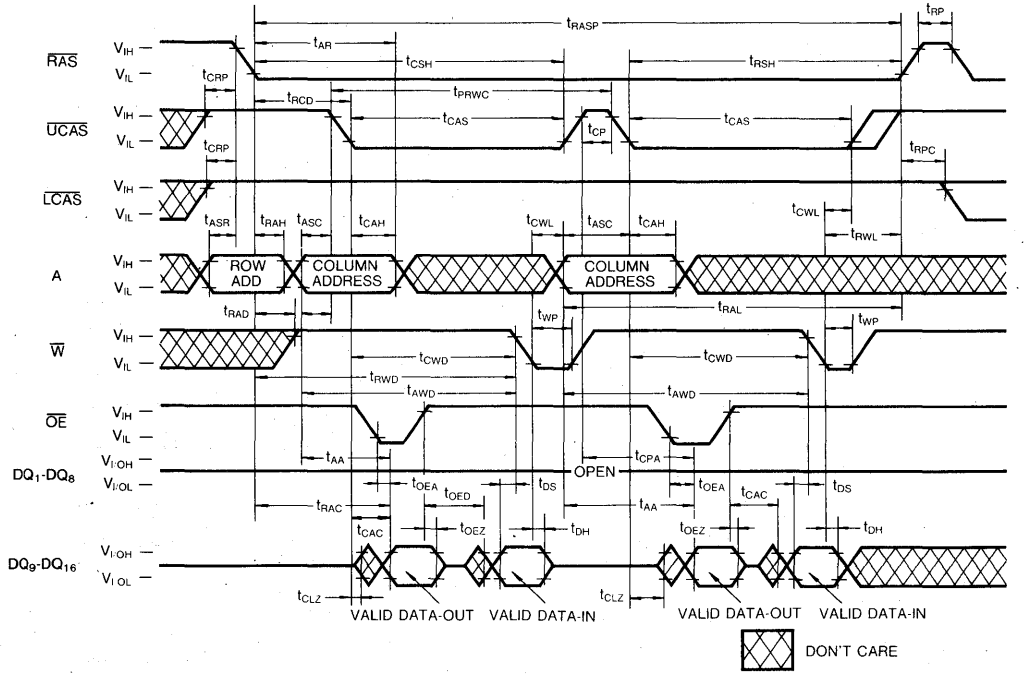
6

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



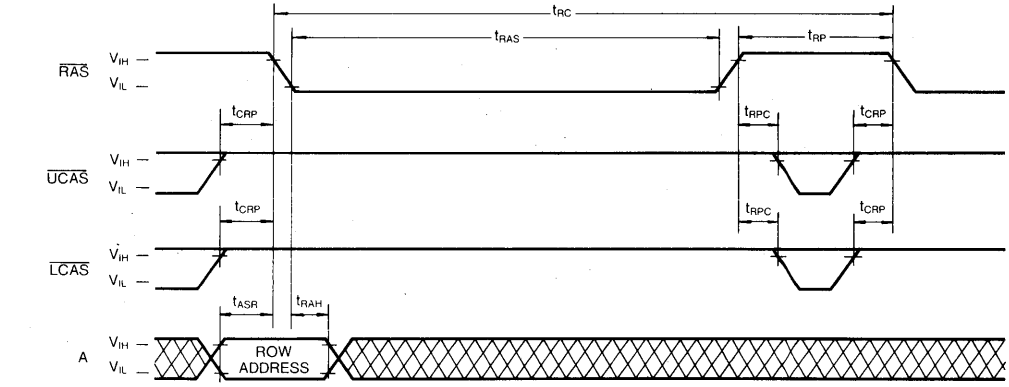
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



TIMING DIAGRAMS (Continued)

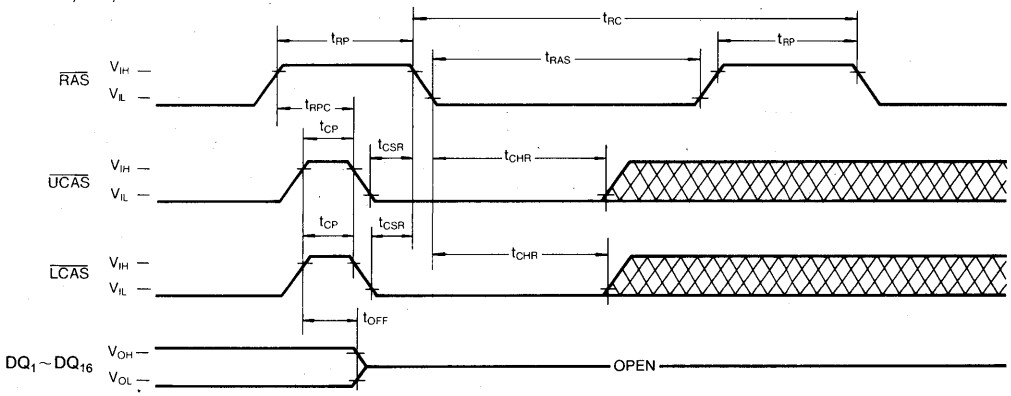
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



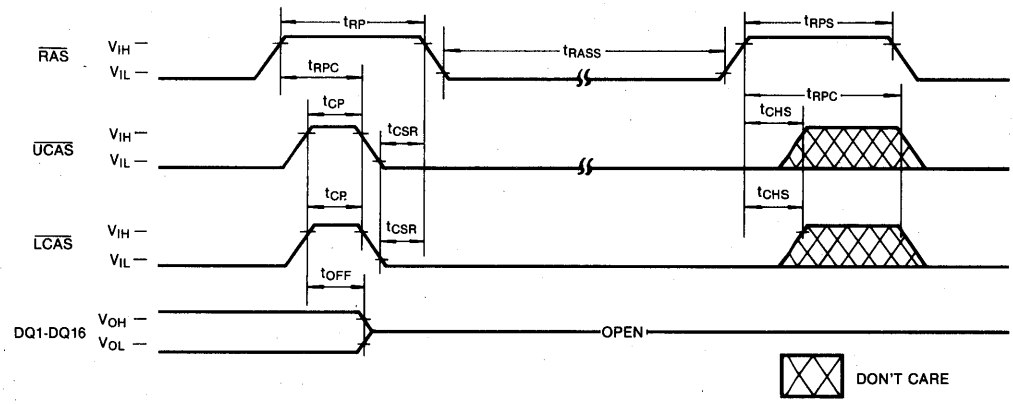
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care



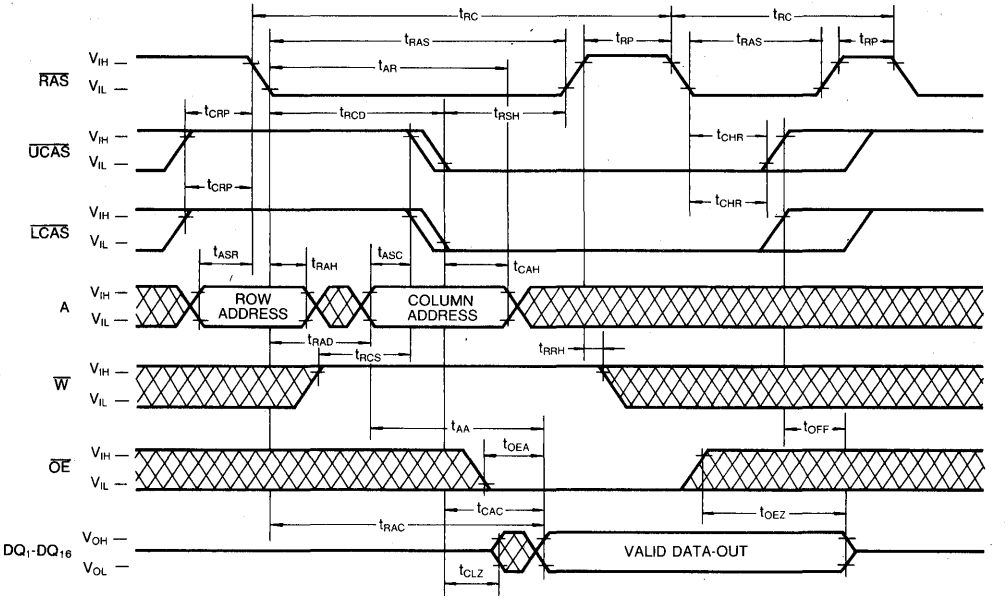
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care

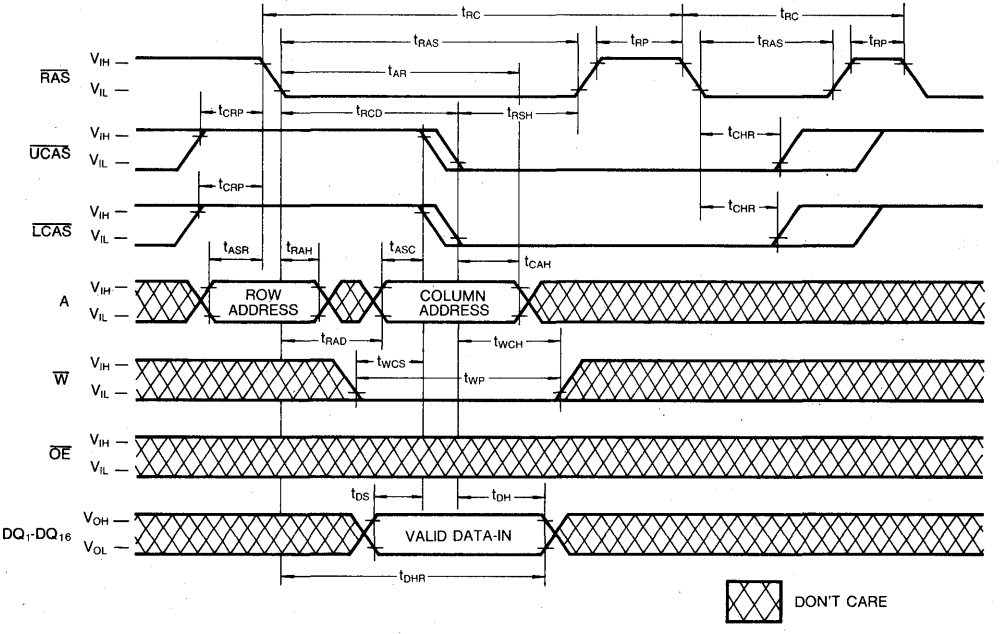


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

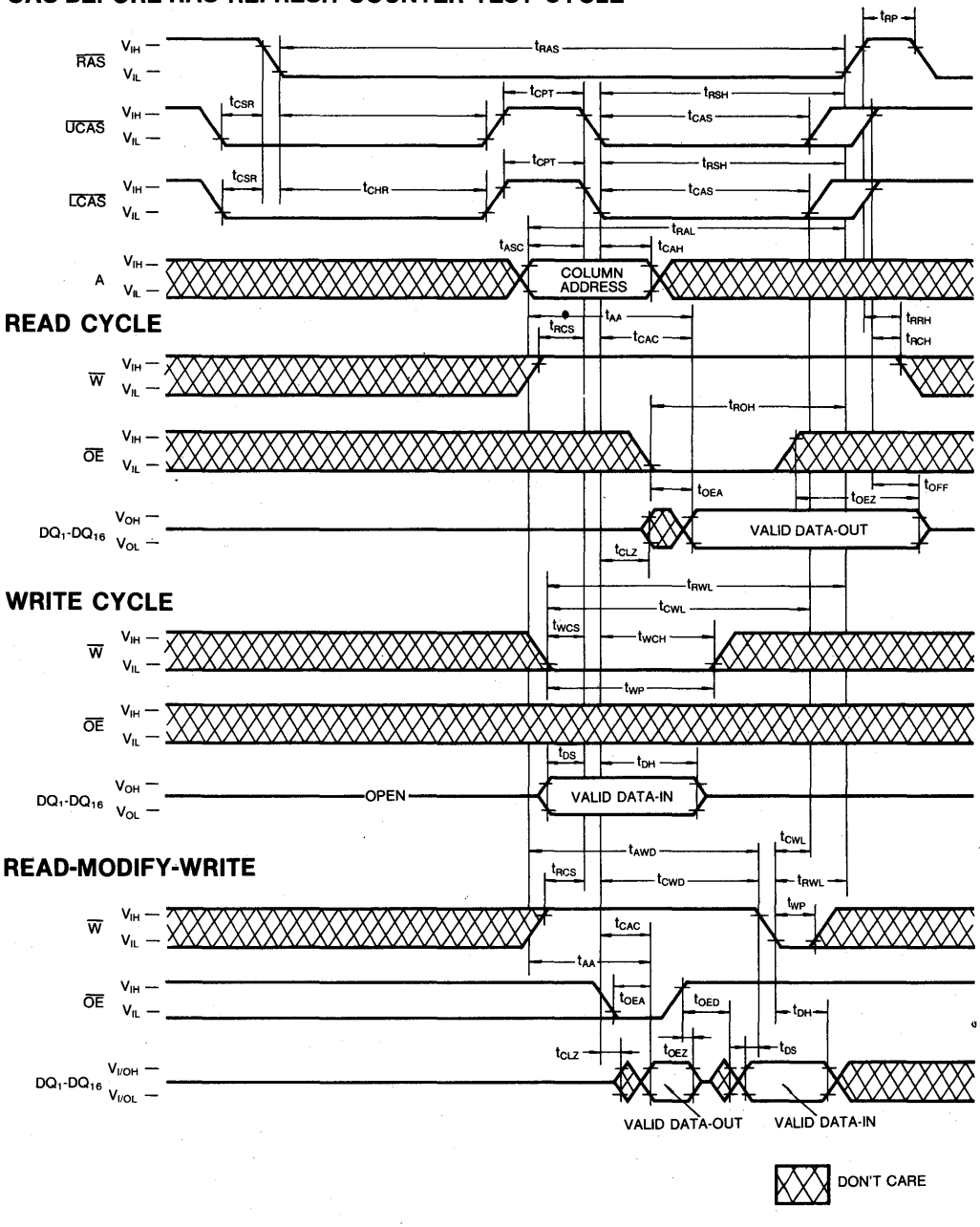


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

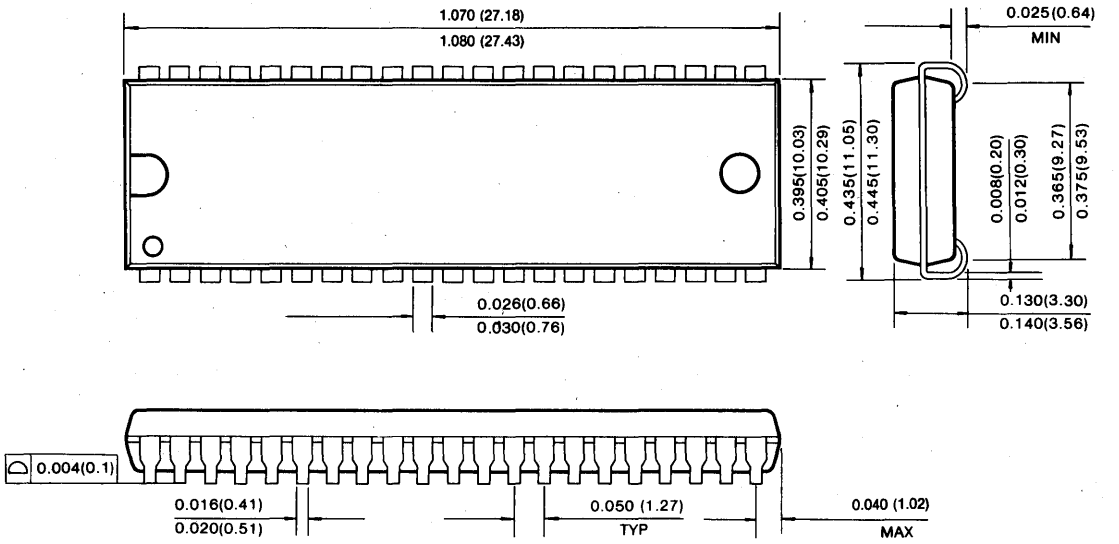
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



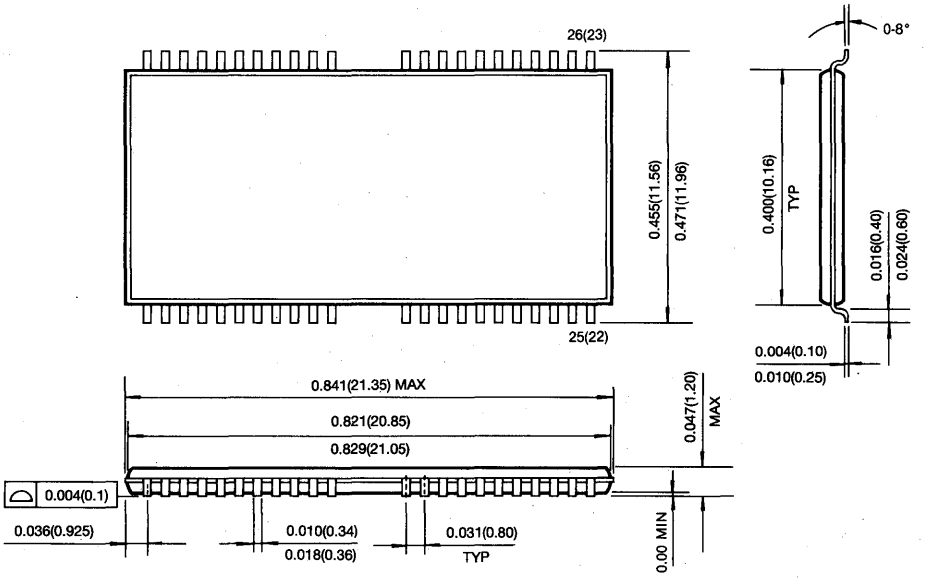
PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



1M x 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM416C1200A-6/A-L6/A-F6	60ns	15ns	110ns
KM416C1200A-7/A-L7/A-F7	70ns	20ns	130ns
KM416C1200A-8/A-L8/A-F8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +5V$\pm$10% power supply**
- **Refresh Cycle**
  - **1024 cycles/16ms (Normal)**
  - **1024 cycles/128ms (L-version)**
  - **1024 cycles/128ms (F-version)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

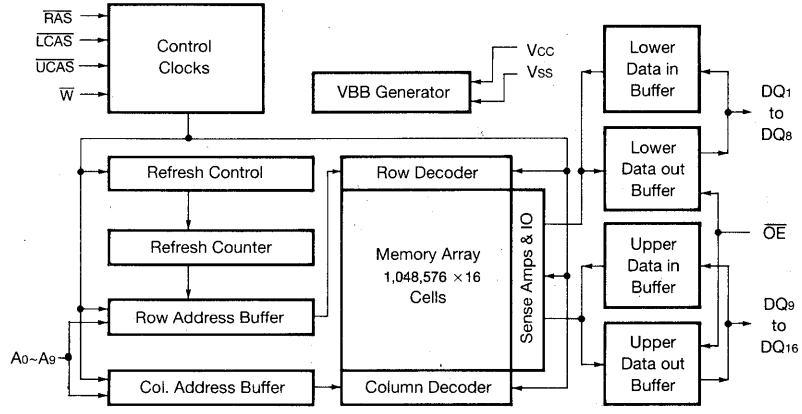
GENERAL DESCRIPTION

The Samsung KM416C1200A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

The KM416C1200A/A-L/A-F features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416C1200A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

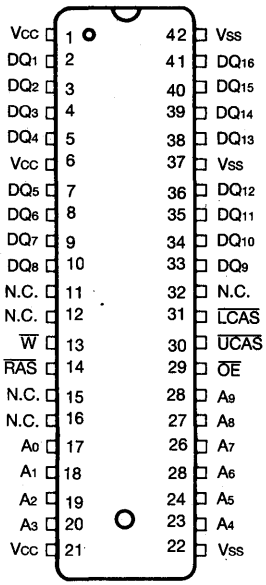
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

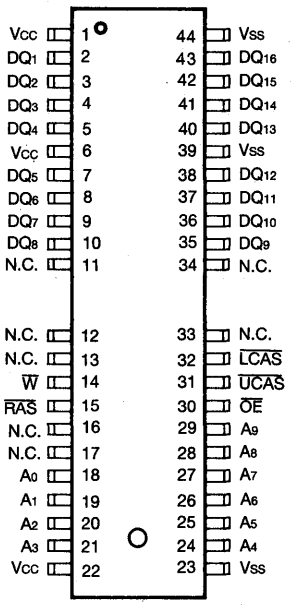
PIN CONFIGURATION (Top Views)

• KM416C1200AJ



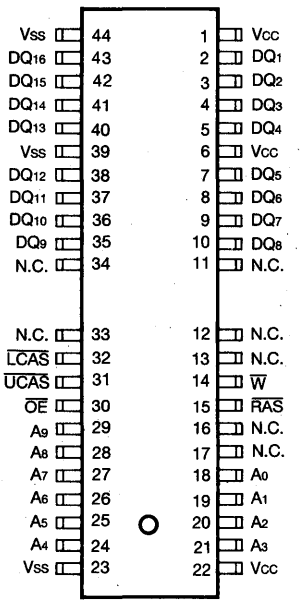
(SOJ)

• KM416C1200AT



(TSOP(II)-Forword)

• KM416C1200AR



(TSOP(II)-Reverse)

Pin Name	Pin Function
A0-A9	Address Inputs
DQ1-16	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VCC	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1~ + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1~ + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{RC}=min.)	KM416C1200A-6/A-L6/A-F6 KM416C1200A-7/A-L7/A-F7 KM416C1200A-8/A-L8/A-F8	I_{CC1}	-	160 150 140	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})	KM416C1200A KM416C1200A-L KM416C1200A-F	I_{CC2}	-	2 1 1	mA mA mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM416C1200A-6/A-L6/A-F6 KM416C1200A-7/A-L7/A-F7 KM416C1200A-8/A-L8/A-F8	I_{CC3}	-	160 150 140	mA mA mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC}=min.)	KM416C1200A-6/A-L6/A-F6 KM416C1200A-7/A-L7/A-F7 KM416C1200A-8/A-L8/A-F8	I_{CC4}	-	110 100 90	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)	KM416C1200A KM416C1200A-L KM416C1200A-F	I_{CC5}	-	1 300 200	mA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC}=min.)	KM416C1200A-6/A-L6/A-F6 KM416C1200A-7/A-L7/A-F7 KM416C1200A-8/A-L8/A-F8	I_{CC6}	-	160 150 140	mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V, Input Low Voltage(V_{IL})=0.2V $\overline{UCAS}$, $\overline{LCAS}$= 0.2V D_{IN}=Don't Care, t_{RC}=125μs (L-Version) t_{RAS}=t_{RAS} min~300ns	KM416C1200A-L	I_{CC7}	-	350	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_9=V_{CC}-0.2V or 0.2V DQ_1-DQ_{16}=V_{CC}-0.2V, 0.2V or Open	KM416C1200A-F	I_{CCS}	-	250	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 V)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once while page mode cycle time t_{PC}.

CAPACITANCE (T_A=25°C, V_{CC}=5V. f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

(Test condition : V_{IH}/V_{IL}=2.4V/0.8V, V_{OH}/V_{OL}=2.4V/0.4V, Output Loading C_L=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		20		ns	
Data-in set-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	10		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		95		100		ns	
$\overline{RAS}$ pulse width (Fast page mode)	tRASP	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	
$\overline{CAS}$ precharge time (Fast page mode)	tCP	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	15		20		20		ns	

AC CHARACTERISTICS (Continued)

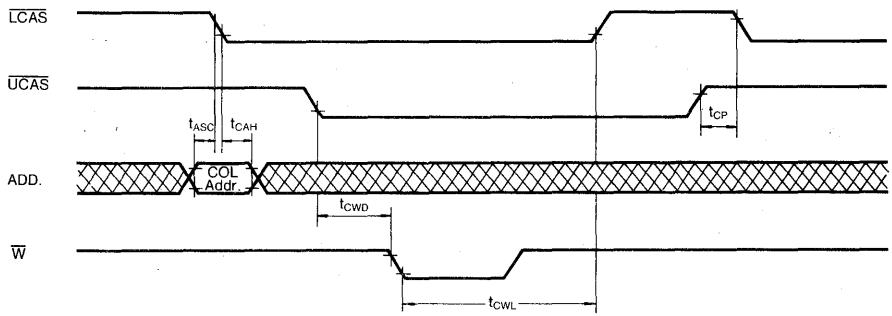
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
$\overline{RAS}$ pulse width (F-ver)	tRASS	100		100		100		μs	19
$\overline{RAS}$ precharge time (F-ver)	tRPS	110		130		150		ns	19
$\overline{CAS}$ hlod time (F-ver)	tCHS	-50		-50		-50		ns	19

KM416C1200A/A-L/A-F Truth Table

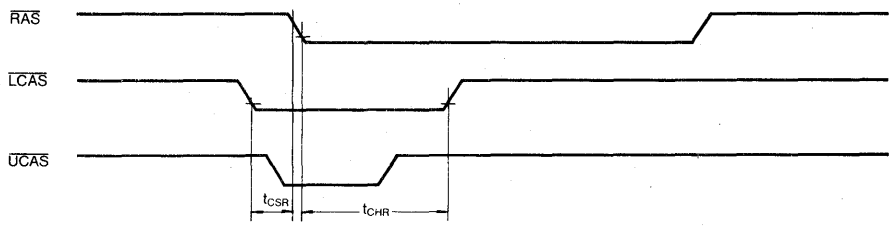
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ_1~DQ_8	DQ_9~DQ_{16}	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

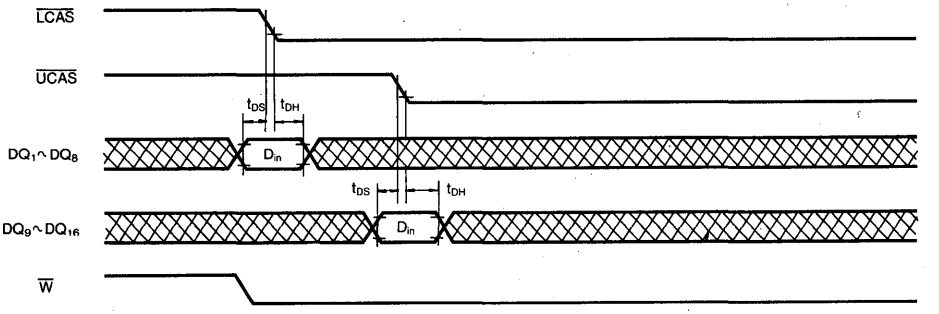
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating aprameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle: If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
17. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

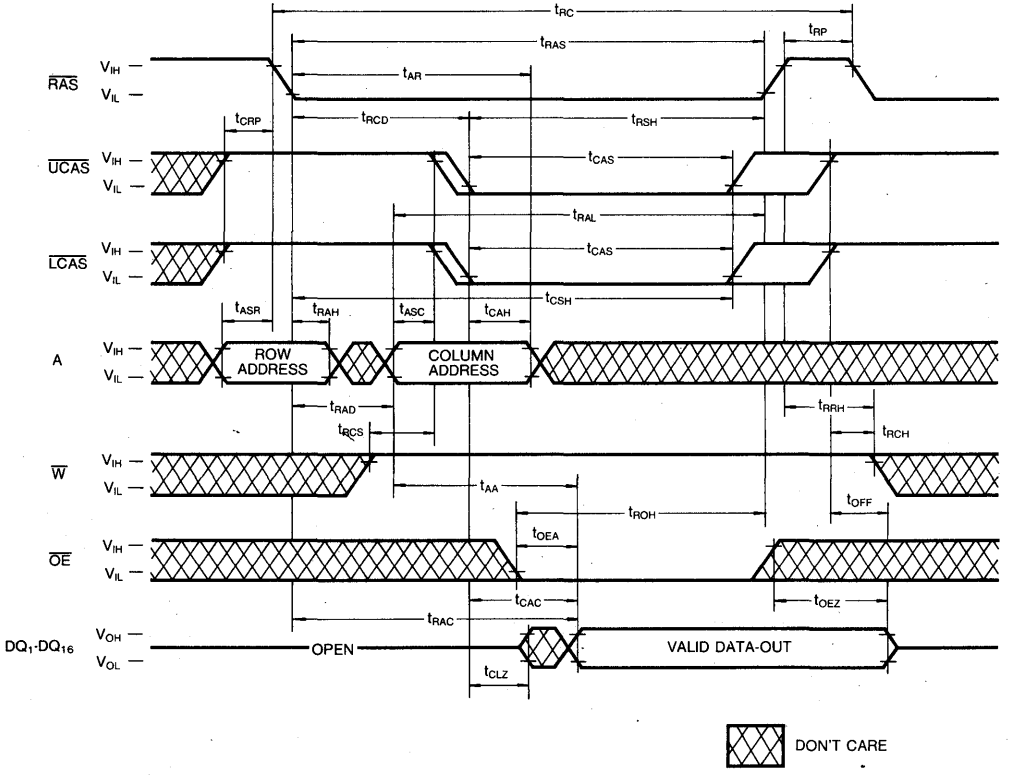


18. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim8)}$, upper byte $D_{in(9\sim16)}$



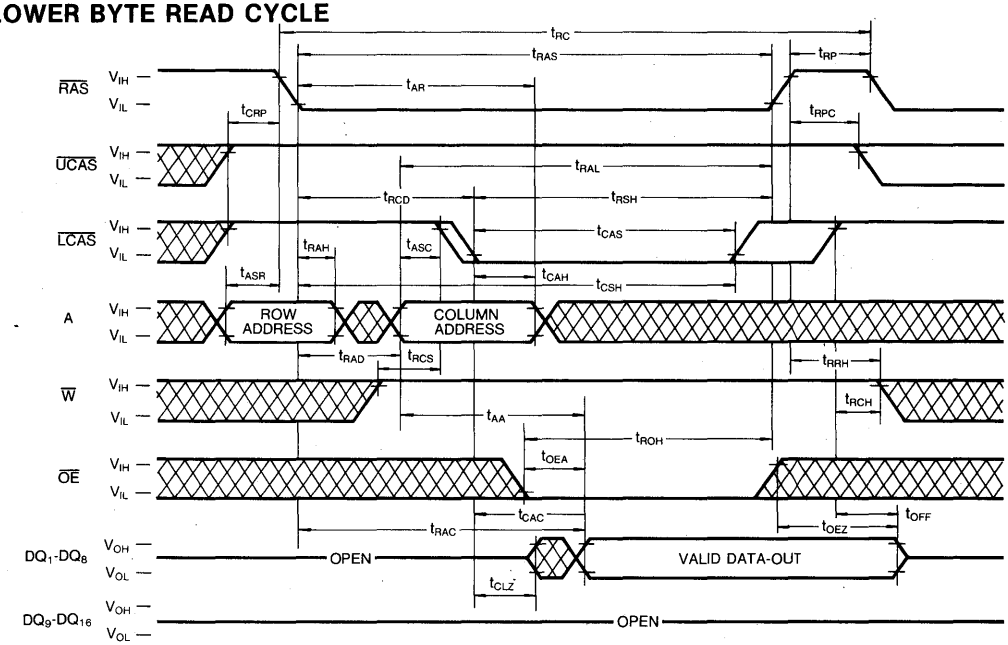
TIMING DIAGRAMS

WORD READ CYCLE

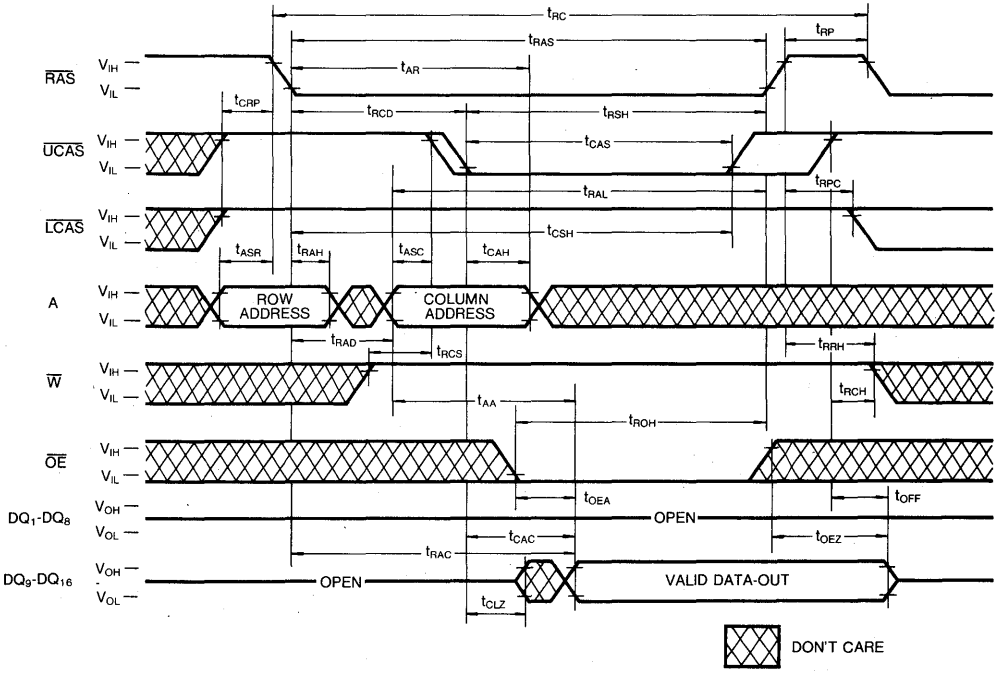


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

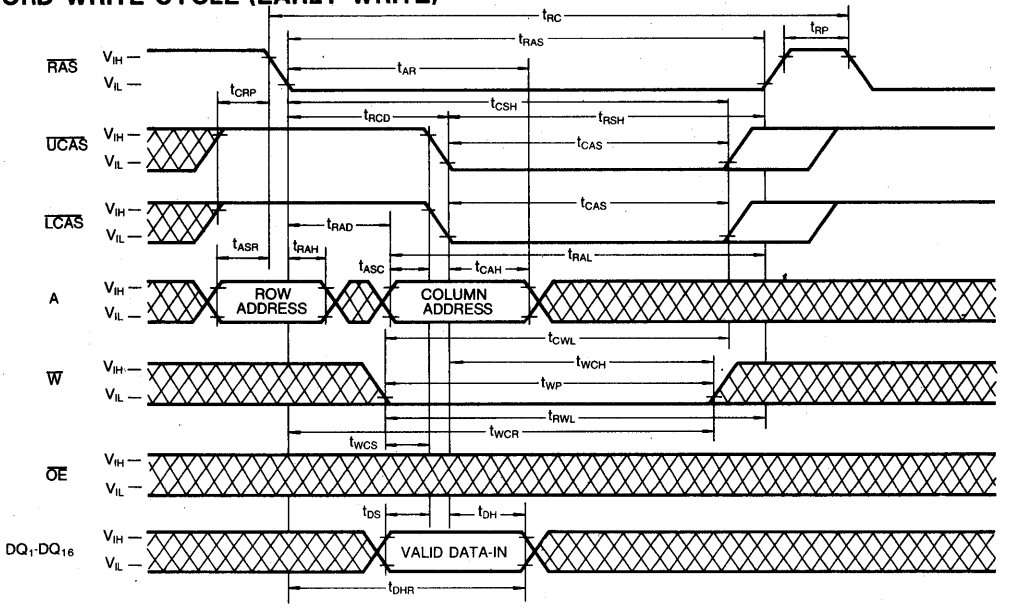


UPPER BYTE READ CYCLE

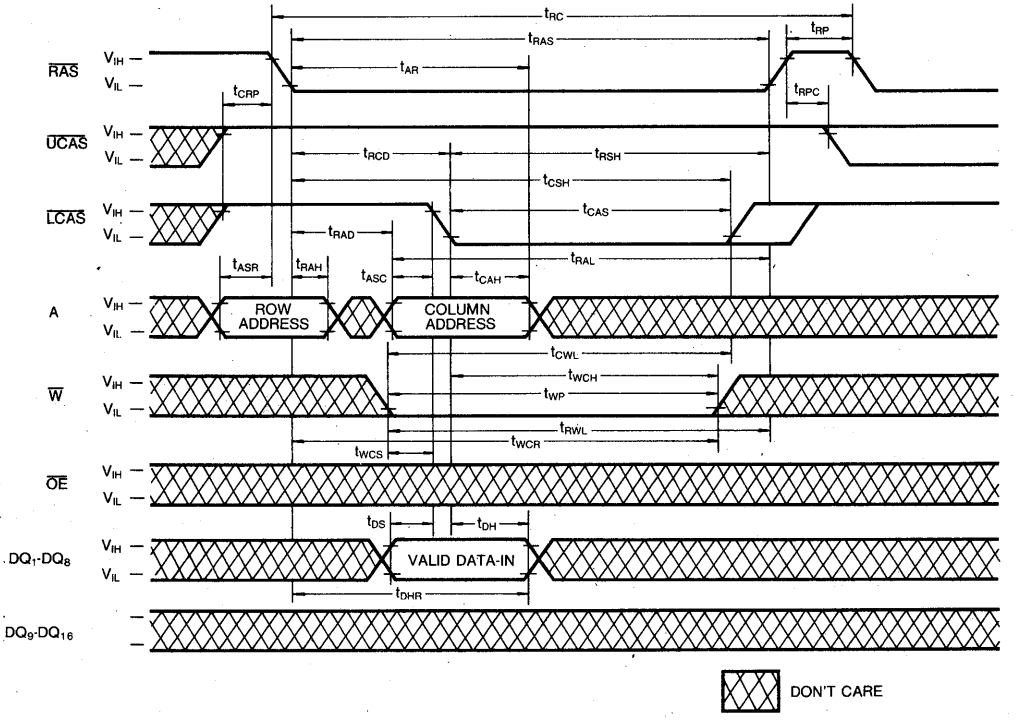


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)

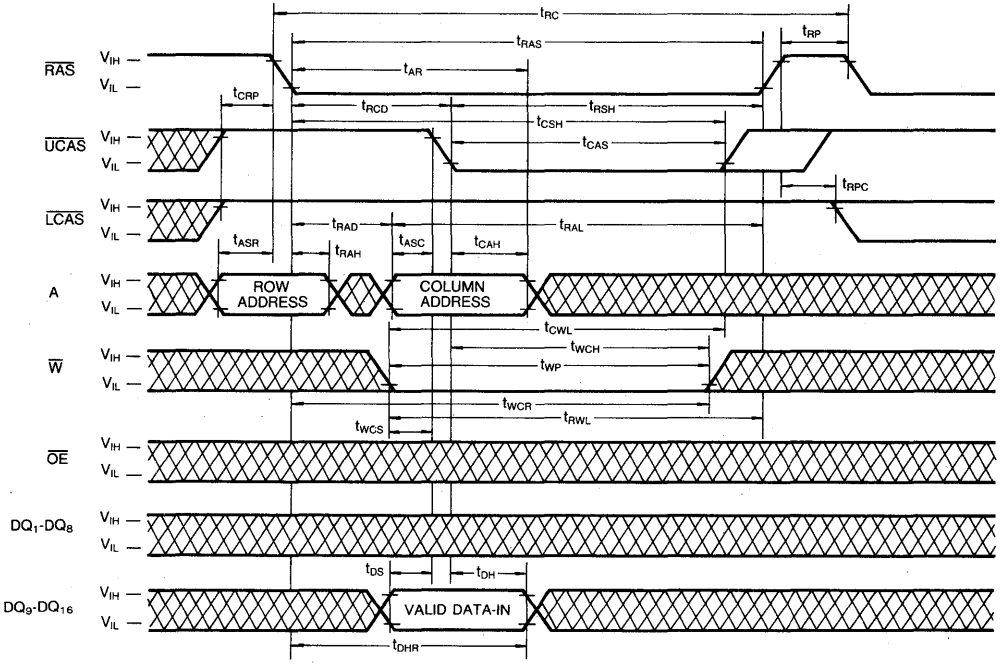


LOWER BYTE WRITE CYCLE (EARLY WRITE)

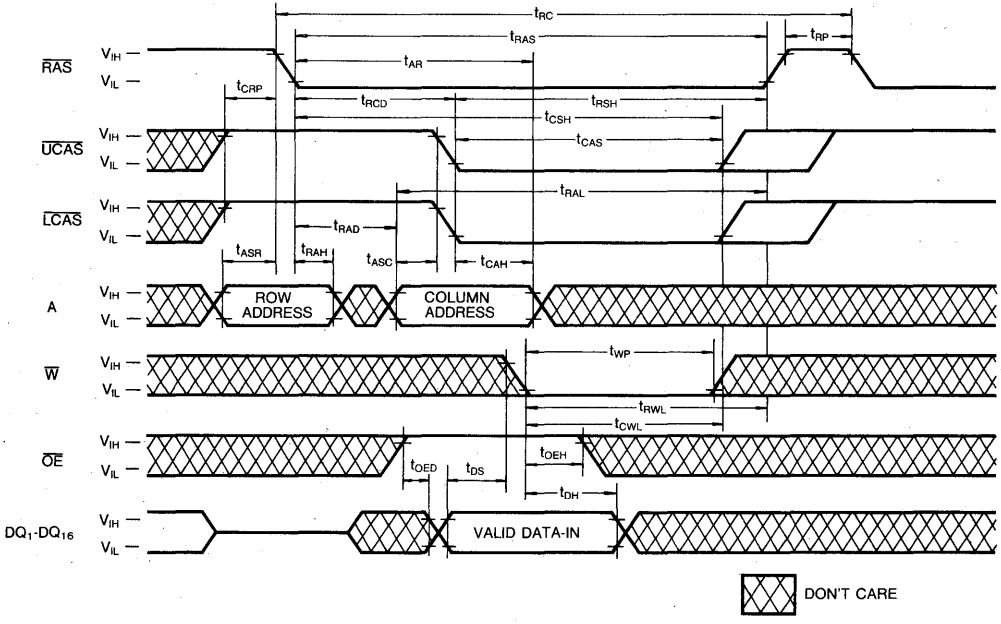


TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

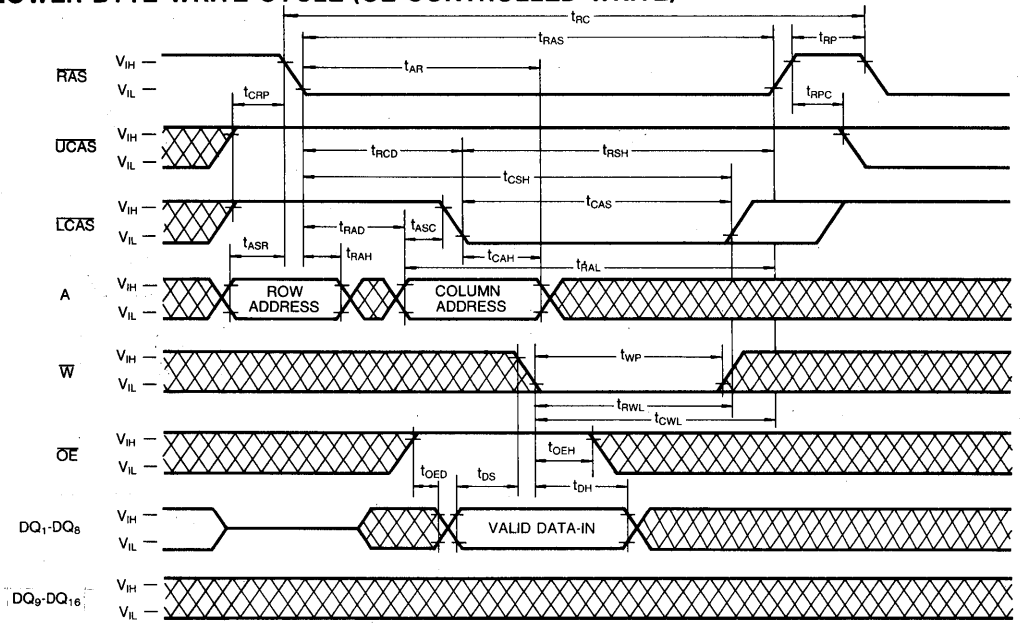


WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

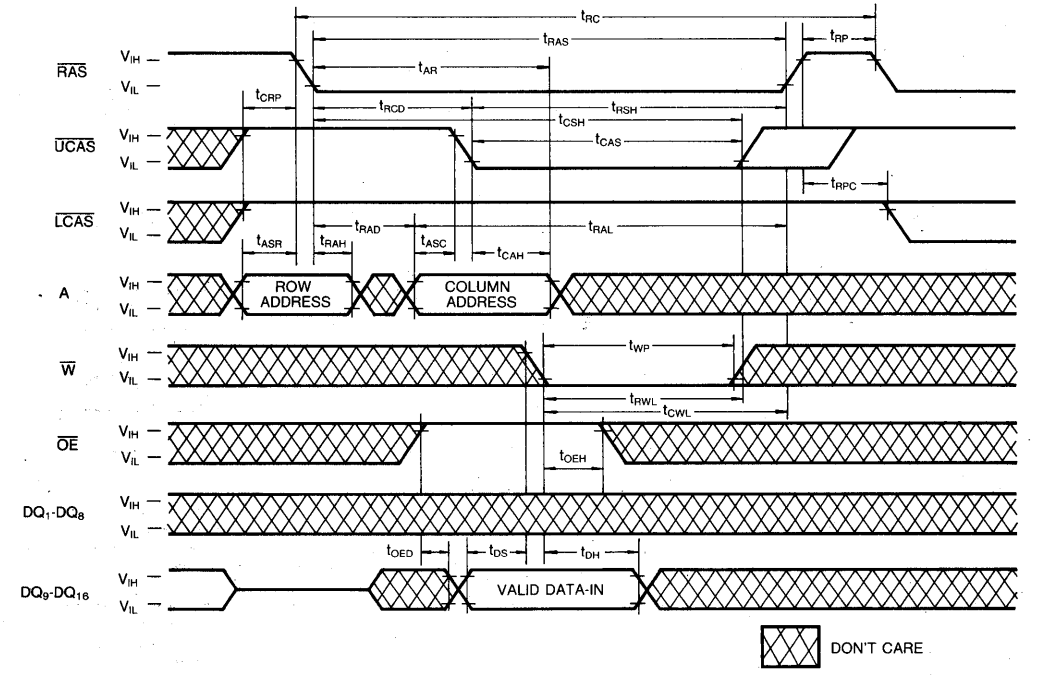


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

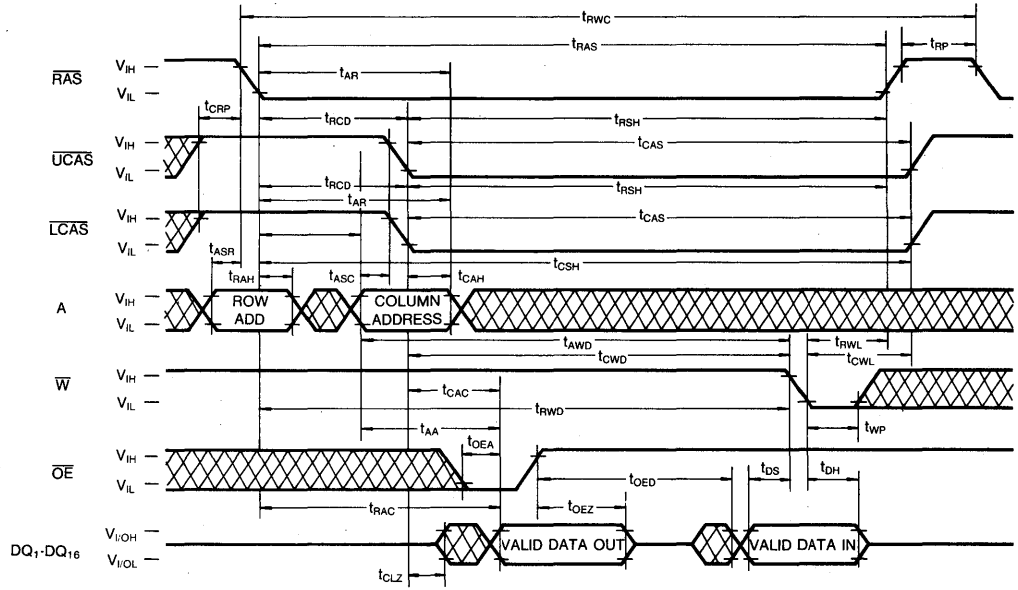


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

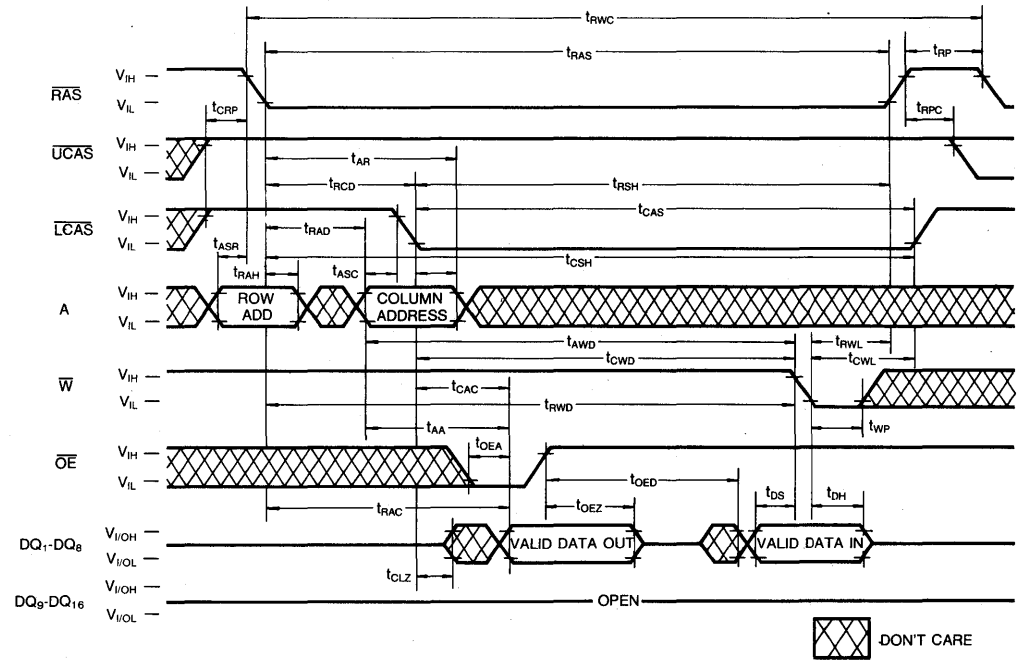


TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

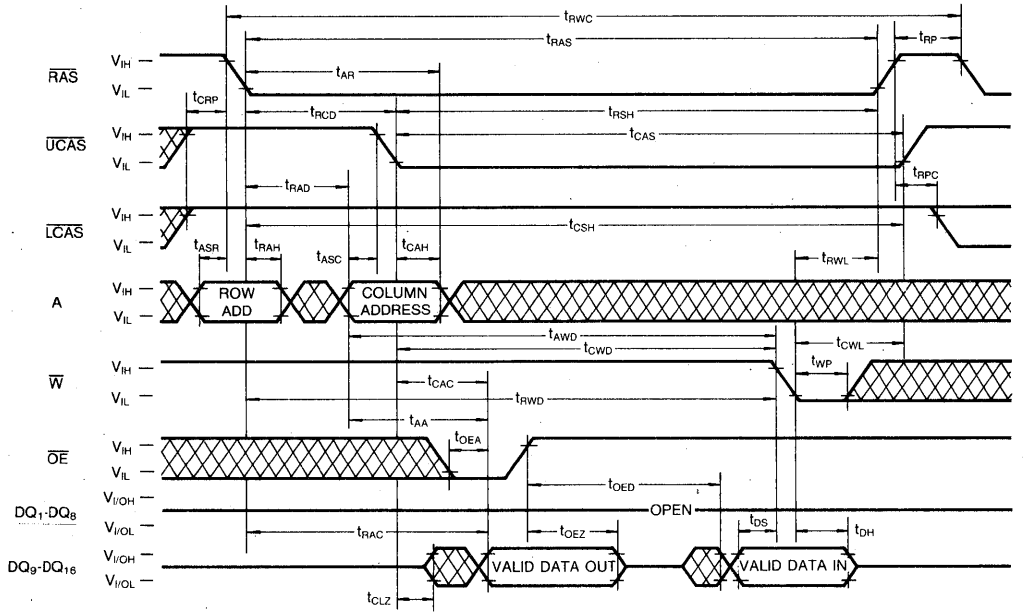


READ-MODIFY-LOWER-BYTE-WRITE CYCLE

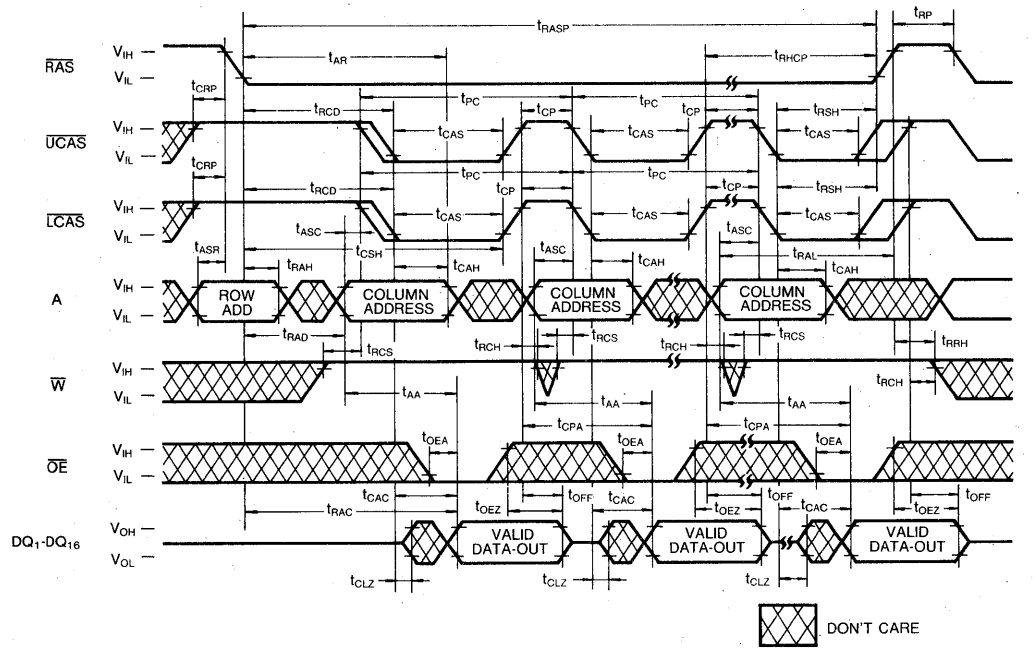


TIMING DIAGRAMS (Continued)

READ-MODIFY-UPPER-BYTE-WRITE CYCLE

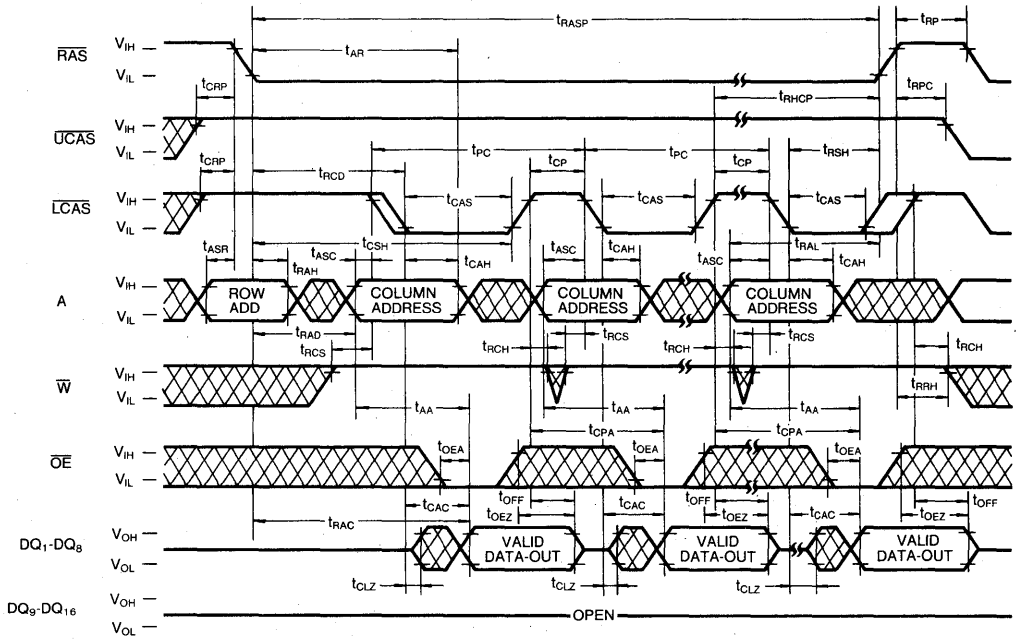


FAST PAGE MODE WORD READ CYCLE

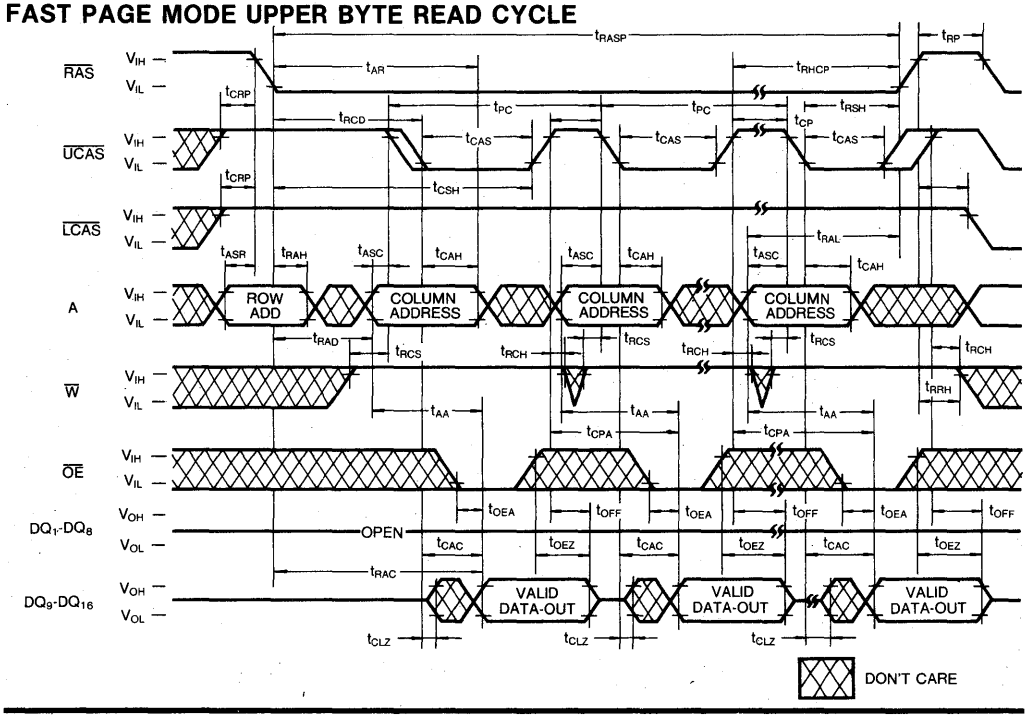


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE

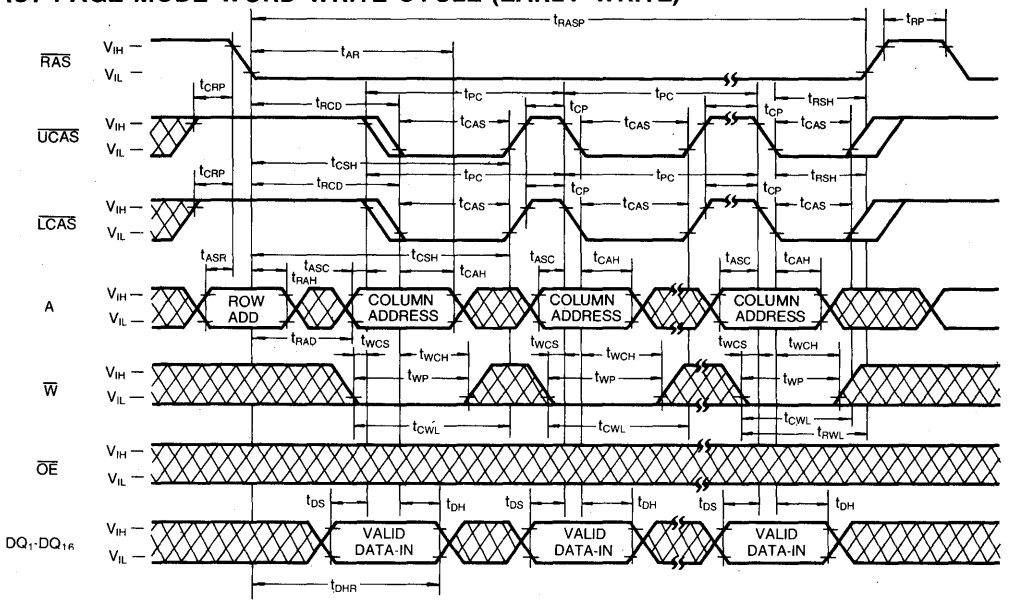


FAST PAGE MODE UPPER BYTE READ CYCLE

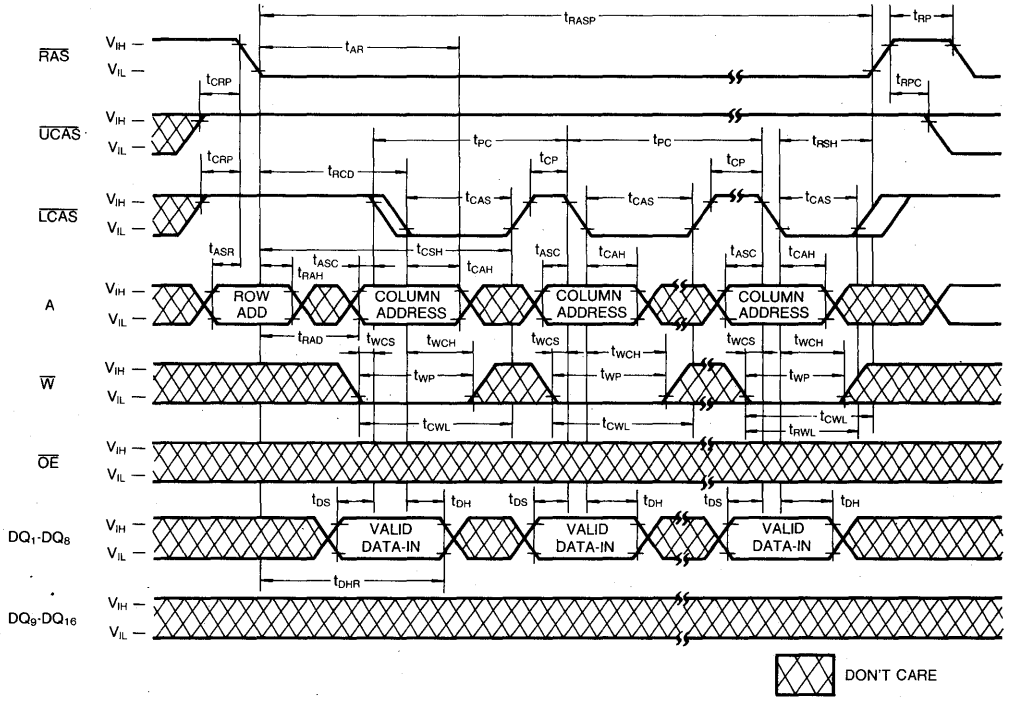


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

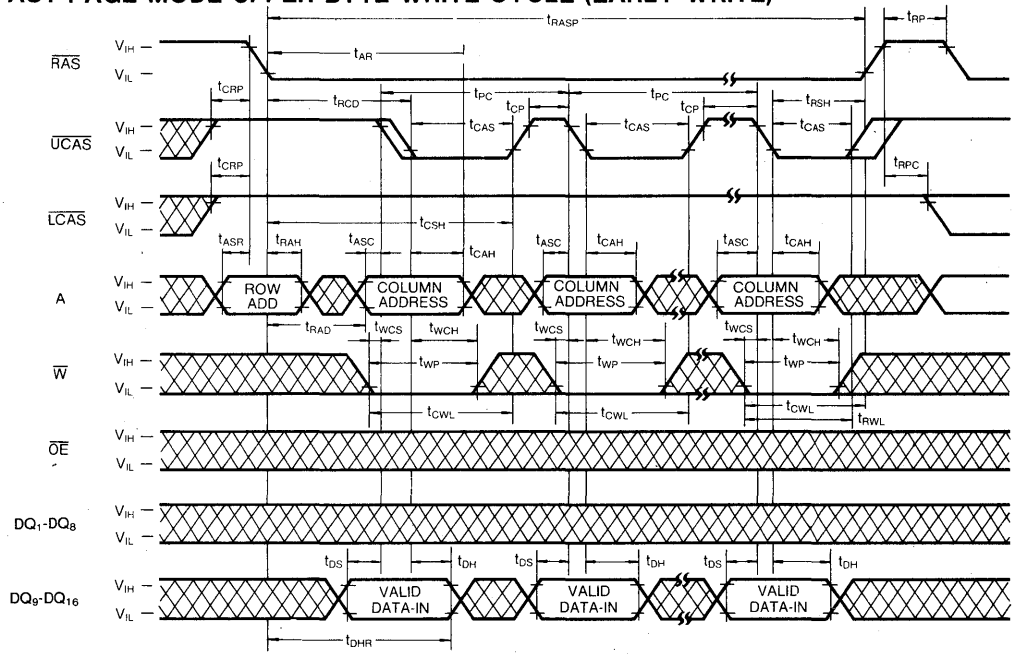


FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)

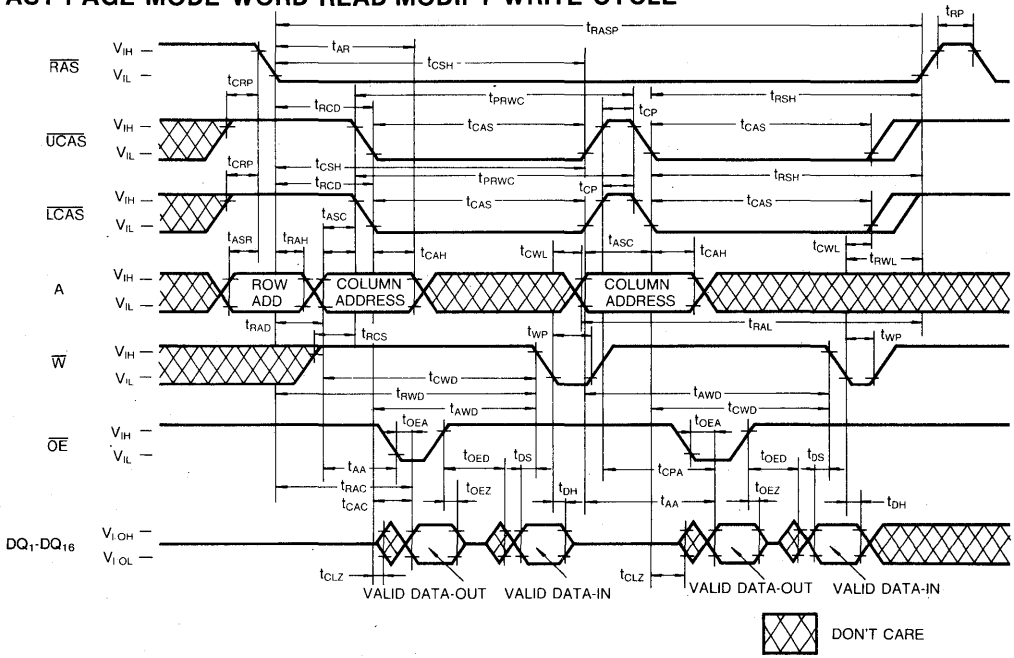


TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

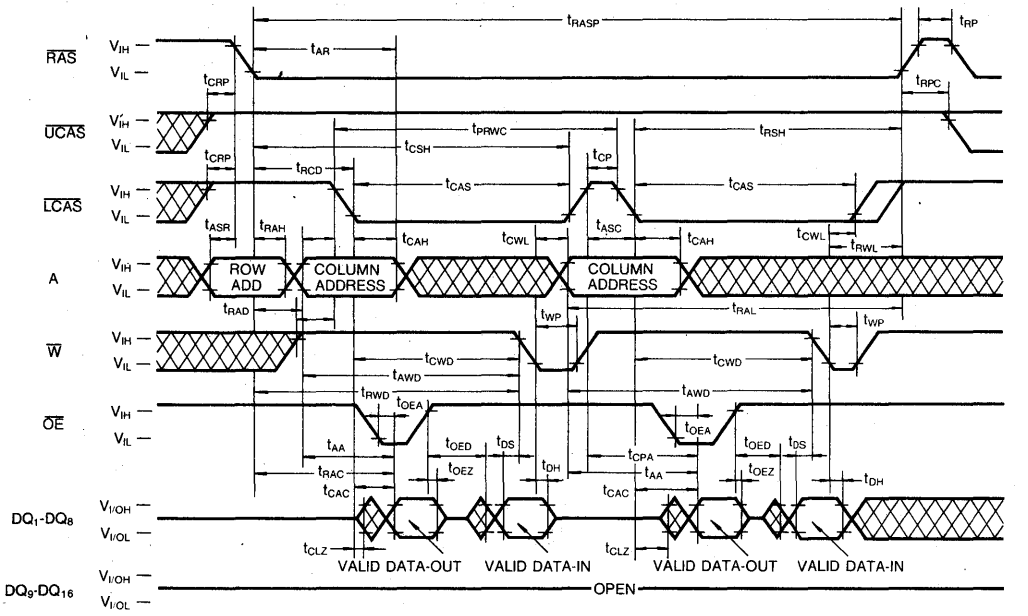


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

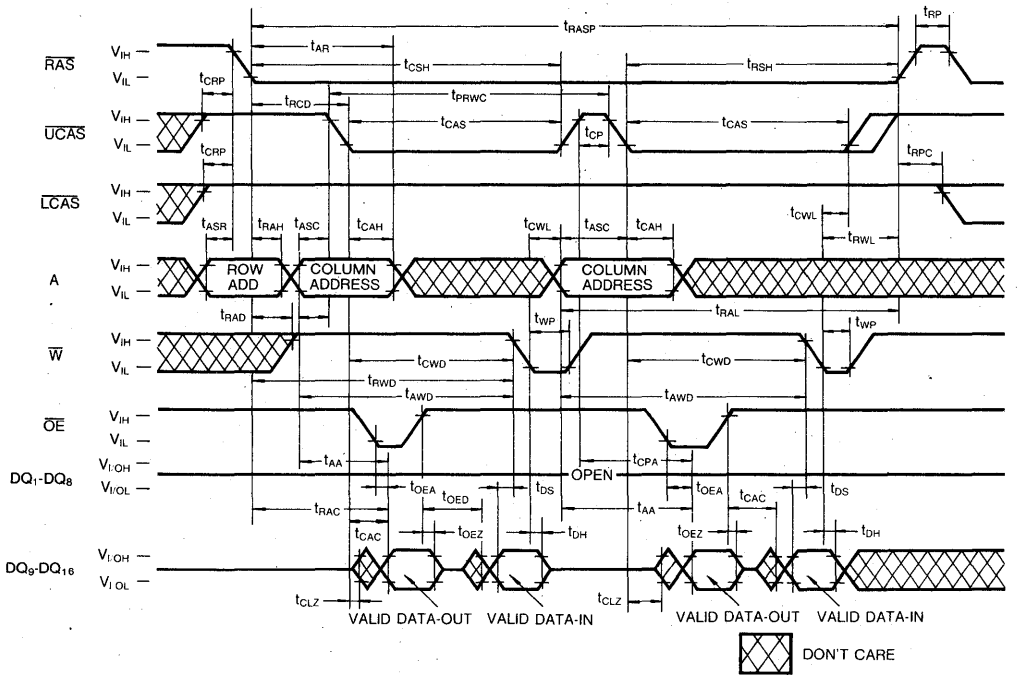


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



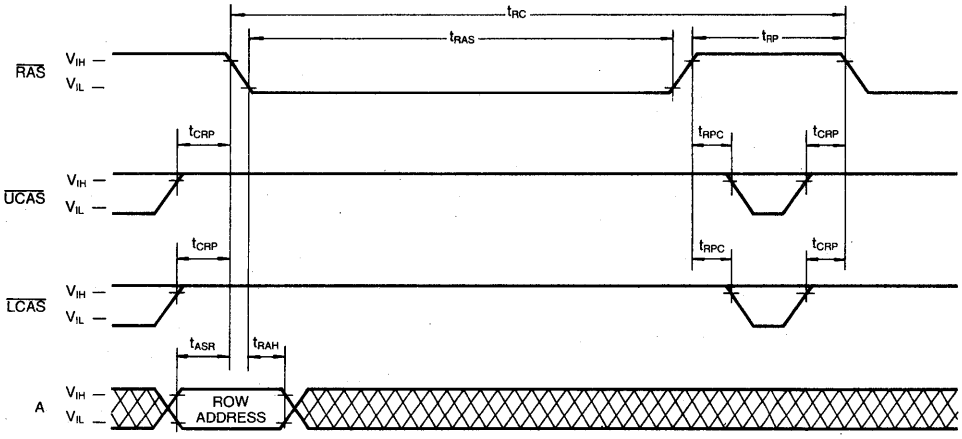
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



TIMING DIAGRAMS (Continued)

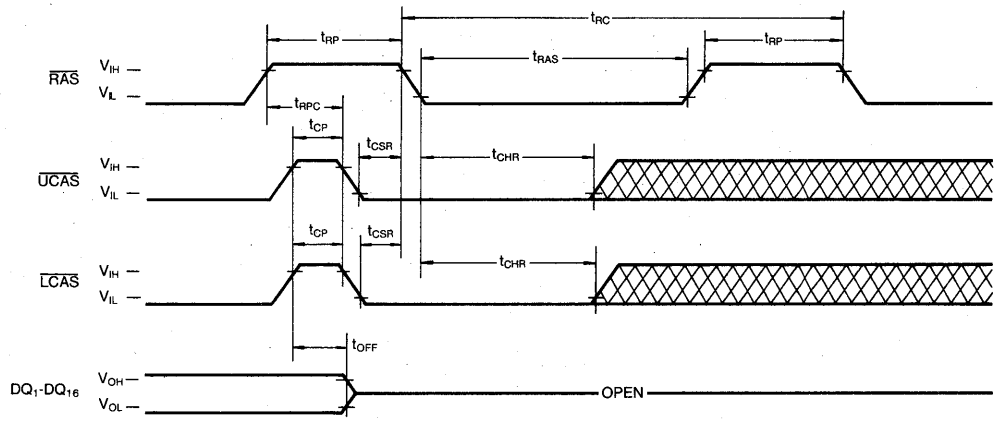
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

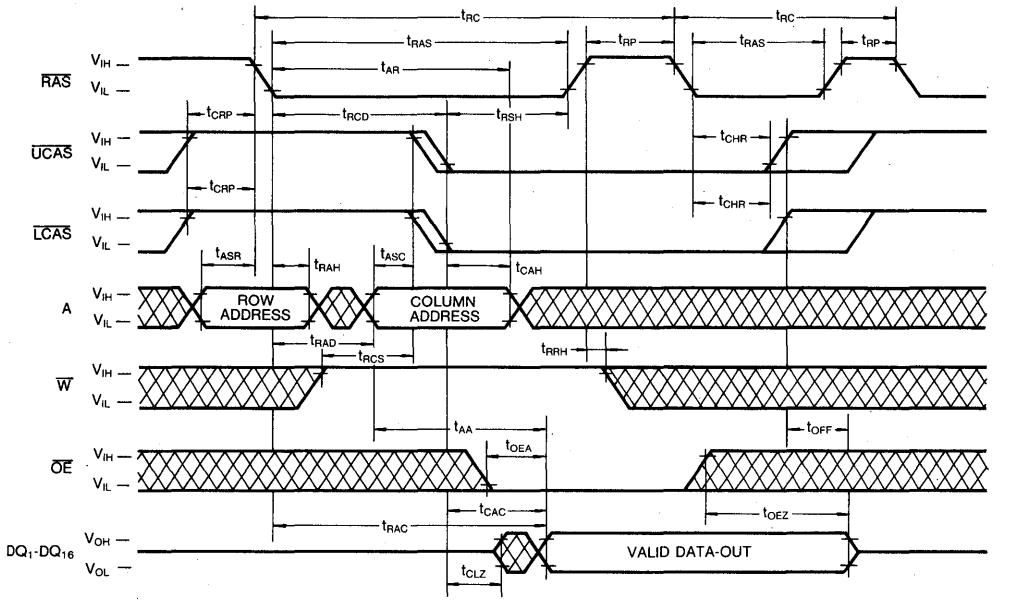
NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



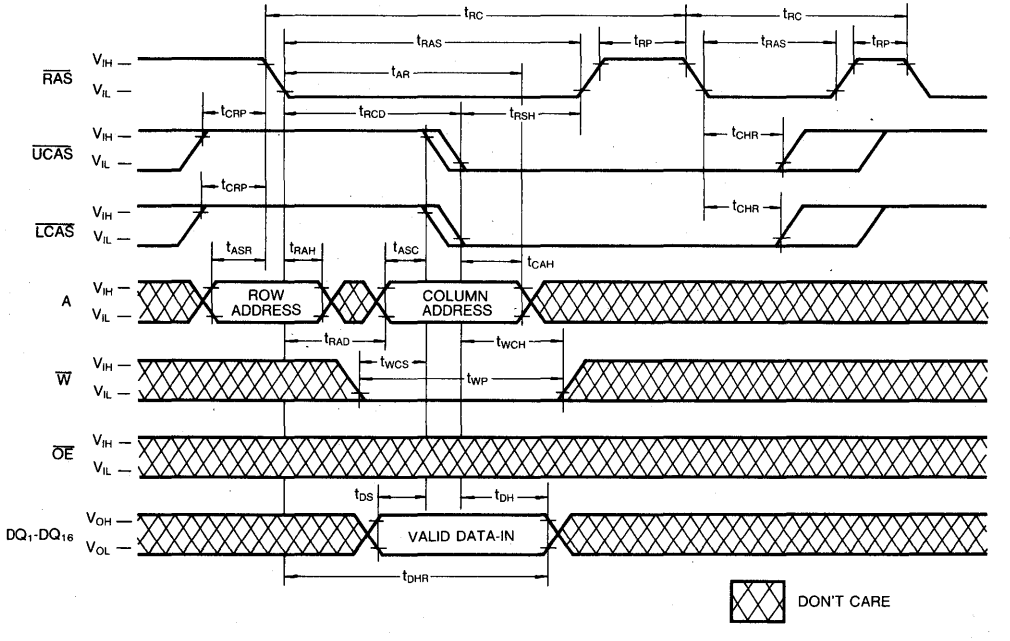
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

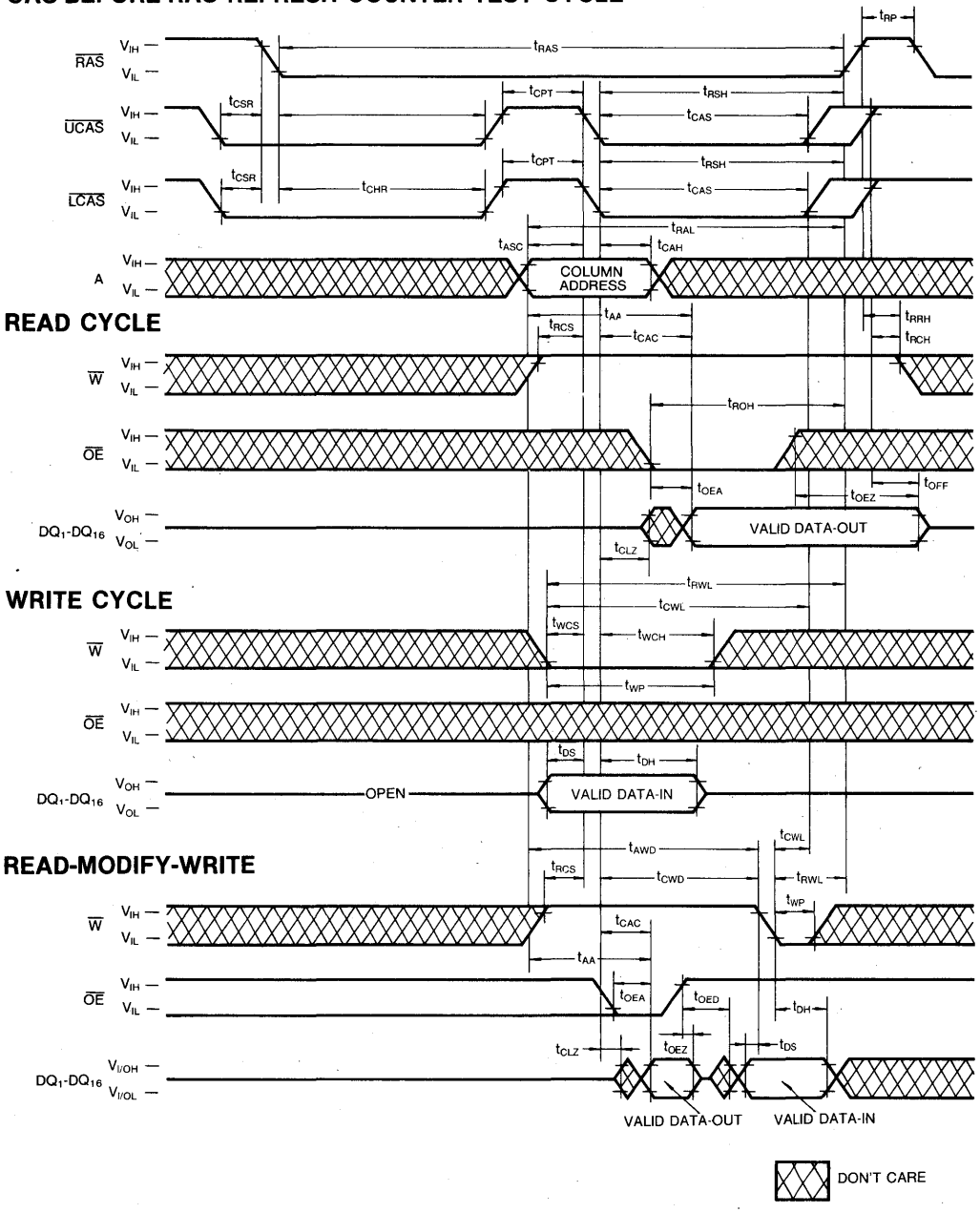


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

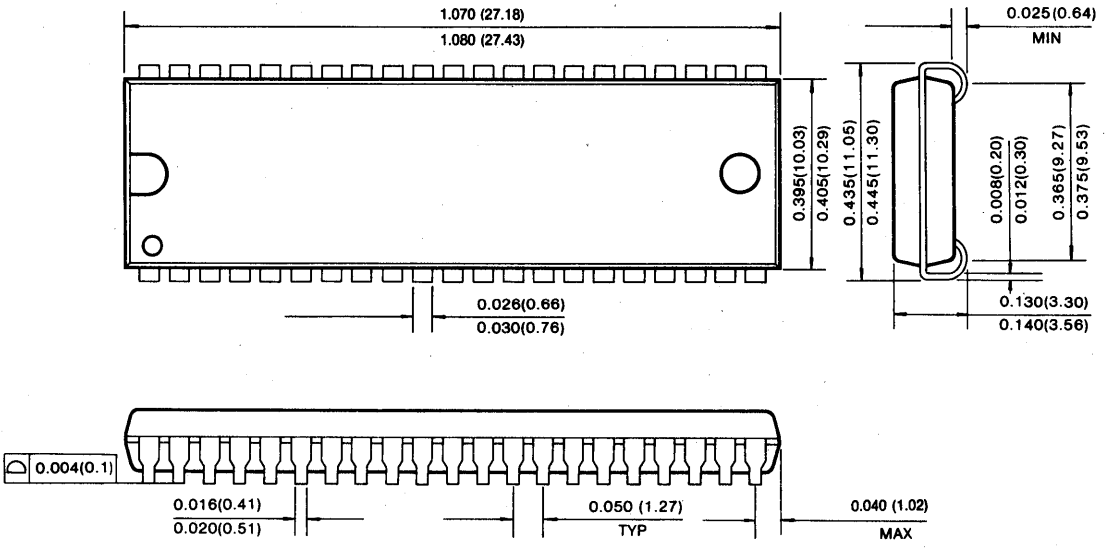
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



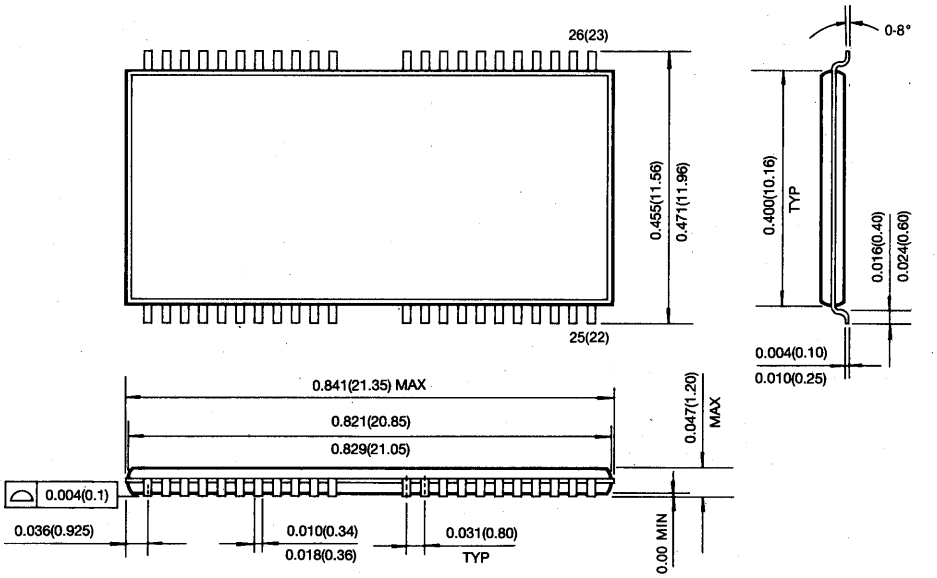
PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



1M x 16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM416C1004A-6/A-L6/A-F6	60ns	17ns	110ns	24ns
KM416C1004A-7/A-L7/A-F7	70ns	20ns	130ns	29ns
KM416C1004A-8/A-L8/A-F8	80ns	20ns	150ns	34ns

- **Extended Data Out Mode**
  (Fast Page Mode with Extended Data Out)
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +5V±10% power supply**
- **Refresh Cycle**
  -4096 cycle/64ms (Normal)
  -4096 cycle/128ms (L-version)
  -4096 cycle/128ms (F-version)
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

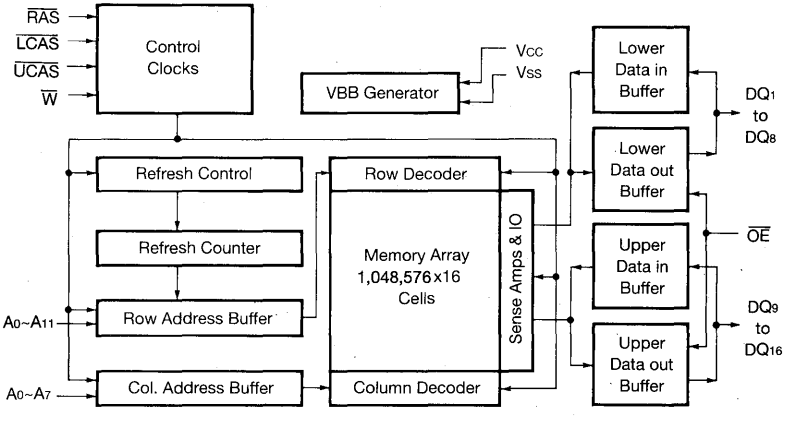
GENERAL DESCRIPTION

The Samsung KM416C1004A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

The KM416C1004A/A-L/A-F features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

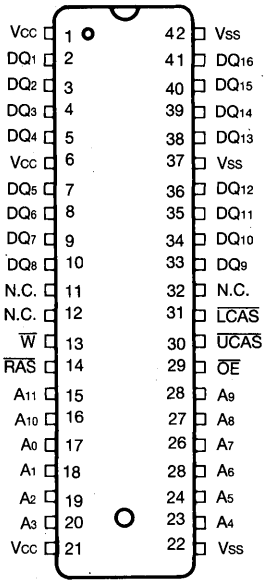
The KM416C1004A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



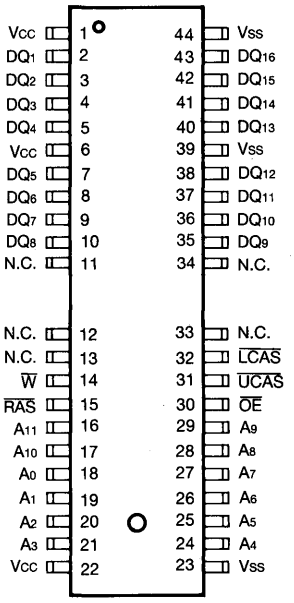
PIN CONFIGURATION (Top Views)

• KM416C1004AJ



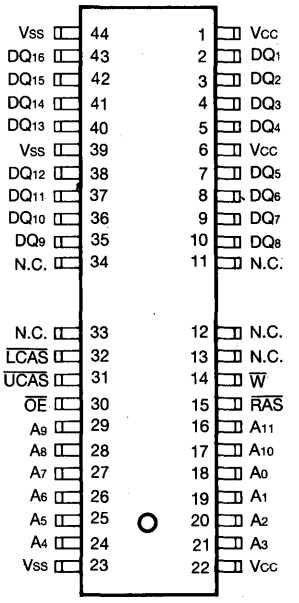
(SOJ)

• KM416C1004AT



(TSOP(II)-Forword)

• KM416C1004AR



(TSOP(II)-Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-16	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VCC	Power(+5V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 t0 + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{RC}=min.)	KM416C1004A-6/A-L6/A-F6 KM416C1004A-7/A-L7/A-F7 KM416C1004A-8/A-L8/A-F8	I_{CC1}	-	100 90 80	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})	KM416C1004A KM416C1004A-L KM416C1004A-F	I_{CC2}	-	2 1 1	mA mA mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM416C1004A-6/A-L6/A-F6 KM416C1004A-7/A-L7/A-F7 KM416C1004A-8/A-L8/A-F8	I_{CC3}	-	100 90 80	mA mA mA
EDO Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC}=min.)	KM416C1004A-6/A-L6/A-F6 KM416C1004A-7/A-L7/A-F7 KM416C1004A-8/A-L8/A-F8	I_{CC4}	-	120 110 100	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)	KM416C1004A KM416C1004A-L KM416C1004A-F	I_{CC5}	-	1 300 200	mA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC}=min.)	KM416C1004A-6/A-L6/A-F6 KM416C1004A-7/A-L7/A-F7 KM416C1004A-8/A-L8/A-F8	I_{CC6}	-	100 90 80	mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V, Input Low Voltage(V_{IL})=0.2V $\overline{UCAS}$, $\overline{LCAS}$= 0.2V D_{IN}=Don't Care, t_{RC}=31.25μs (L-Ver) t_{RAS}=t_{RAS} min~300ns	KM416C1004A-L	I_{CC7}	-	450	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{CC}-0.2V or 0.2V DQ_1-DQ_{16}=V_{CC}-0.2V or 0.2V or Open	KM416C1004A-F	I_{CCS}	-	250	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 V)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once while one Hyper page mode cycle time t_{HPC}.

CAPACITANCE (T_A=25°C, V_{CC}=5V. f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5V±10%, See notes 1,2)

(Test condition : V_{IH}/V_{IL}=2.4V/0.8V, V_{OH}/V_{OL}=2.0V/0.8V, Output Loading C_L=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		17		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	17		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	15	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	15
Column address hold time	tCAH	10		15		15		ns	15
Column address hold time referenced to $\overline{RAS}$	tAR	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	10		15		20		ns	18
Data-in set-up time	tDS	0		0		0		ns	10,21
Data-in hold time	tDH	10		15		15		ns	10,21
Data-in hold time referenced to $\overline{RAS}$	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		50		50		ns	8,17
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	20
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		25		30		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	15		20		20		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	7
$\overline{OE}$ commend hold time	tOEH	15		20		20		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Hyper Page mode cycle time	t_{HPC}	24		29		34		ns	12
Hyper Page mode read-modify-write cycle time	t_{HPRWC}	76		81		91		ns	12
$\overline{CAS}$ orcgarge time (Hyper page mode)	t_{CP}	10		10		10		ns	16
$\overline{RAS}$ pulse width (Hyper page mode)	t_{RASP}	60	200.000	70	200.000	80	200.000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
Output data hold time	t_{DOH}	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	15	3	20	3	20	ns	7
$\overline{W}$ to data delay	t_{WED}	15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		5		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		5		ns	
$\overline{RAS}$ pulse width (F-ver)	t_{RASS}	100		100		100		μs	13
$\overline{RAS}$ precharge time (F-ver)	t_{RPS}	110		130		150		ns	13
$\overline{CAS}$ hlod time (F-ver)	t_{CHS}	-50		-50		-50		ns	13

KM416C1004A/A-L/A-F Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ_1~DQ_8	DQ_9~DQ_{16}	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

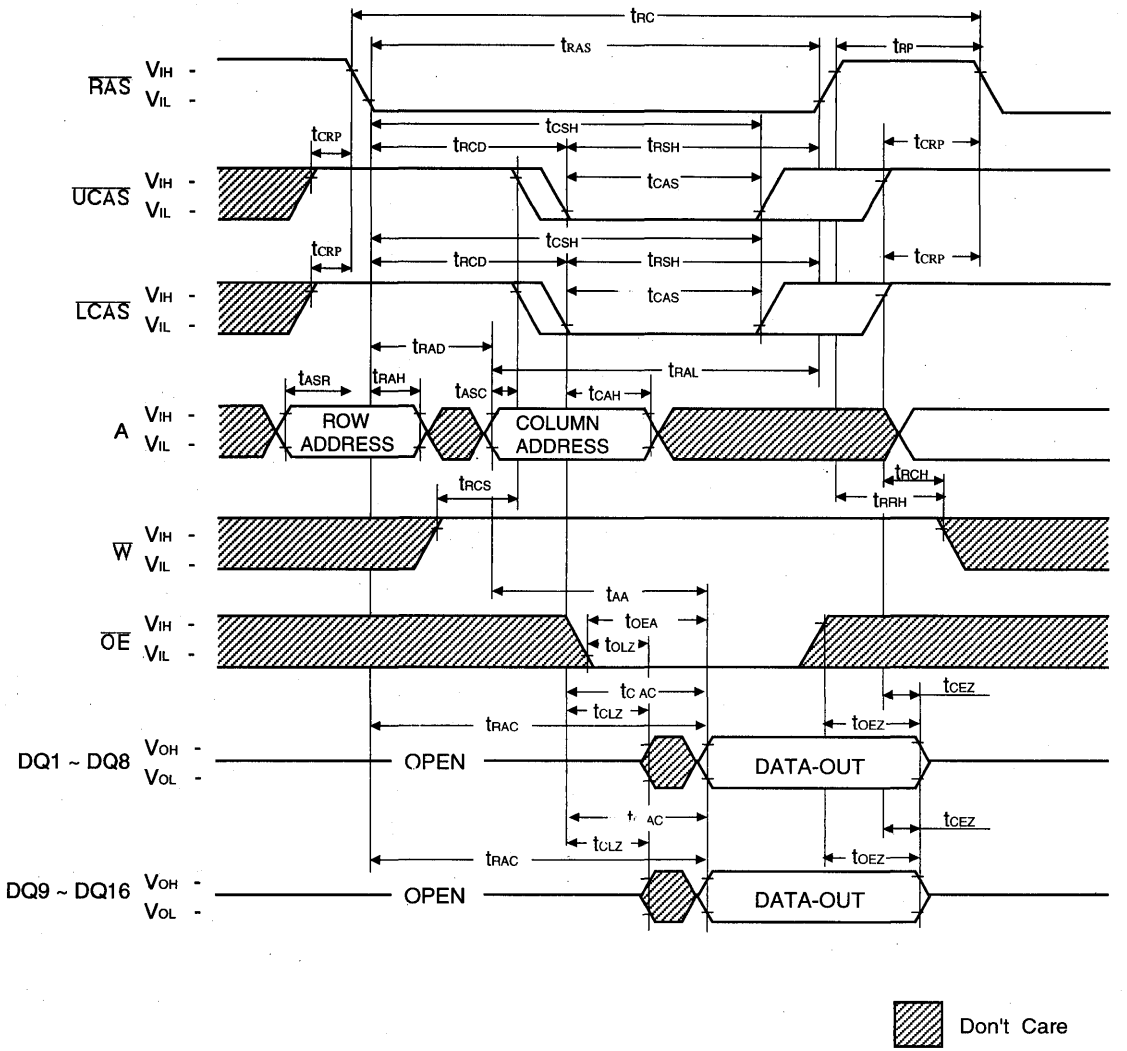
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2TTL Loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. $t_{ASC} \geq t_{CP}$ min, Assume t_T=2.0ns.
13. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (F-version)
14. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
16. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
17. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
18. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
19. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
20. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.
21. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim8)}$, upper byte $D_{in(9\sim16)}$

TIMING DIAGRAM

WORD READ CYCLE

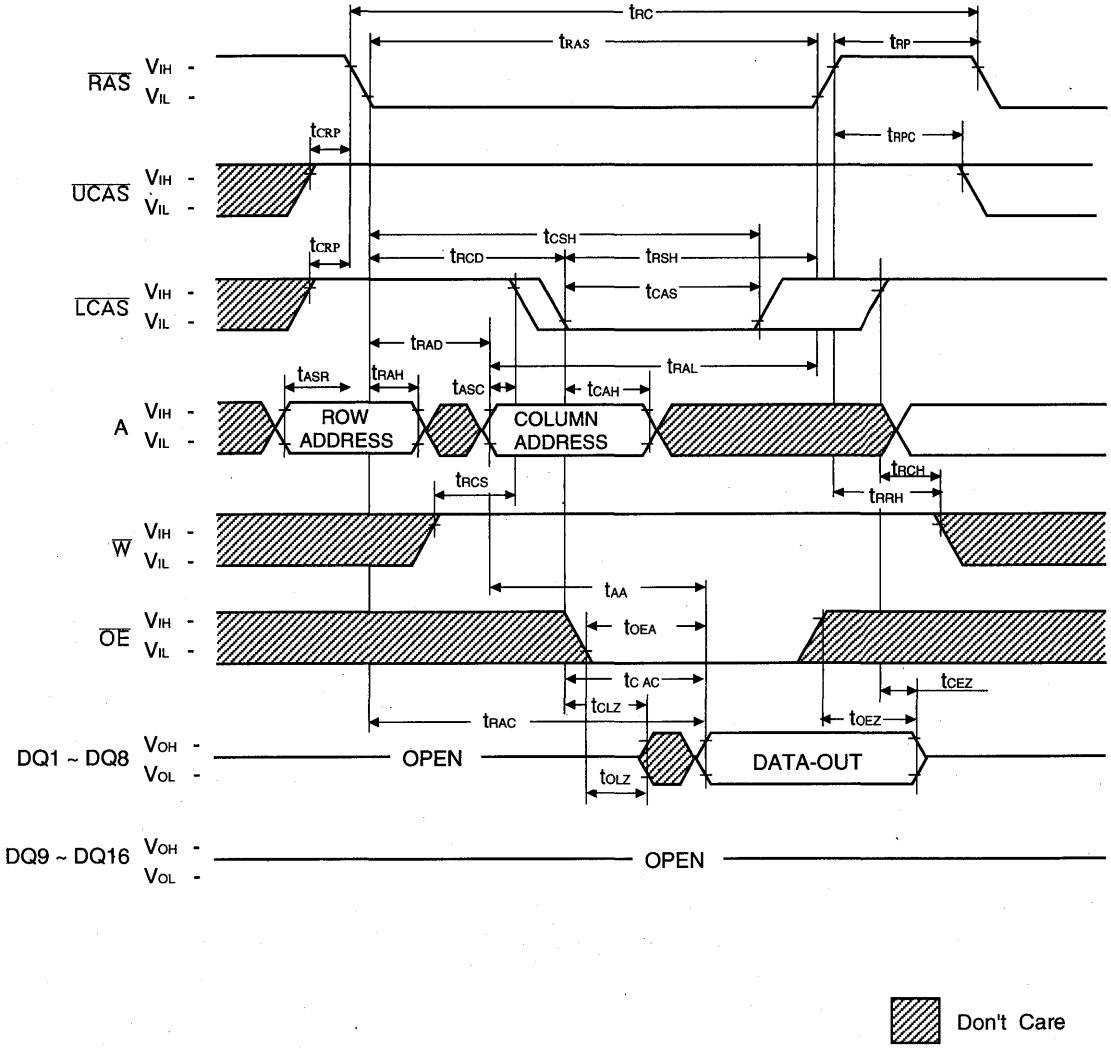
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

LOWER BYTE READ CYCLE

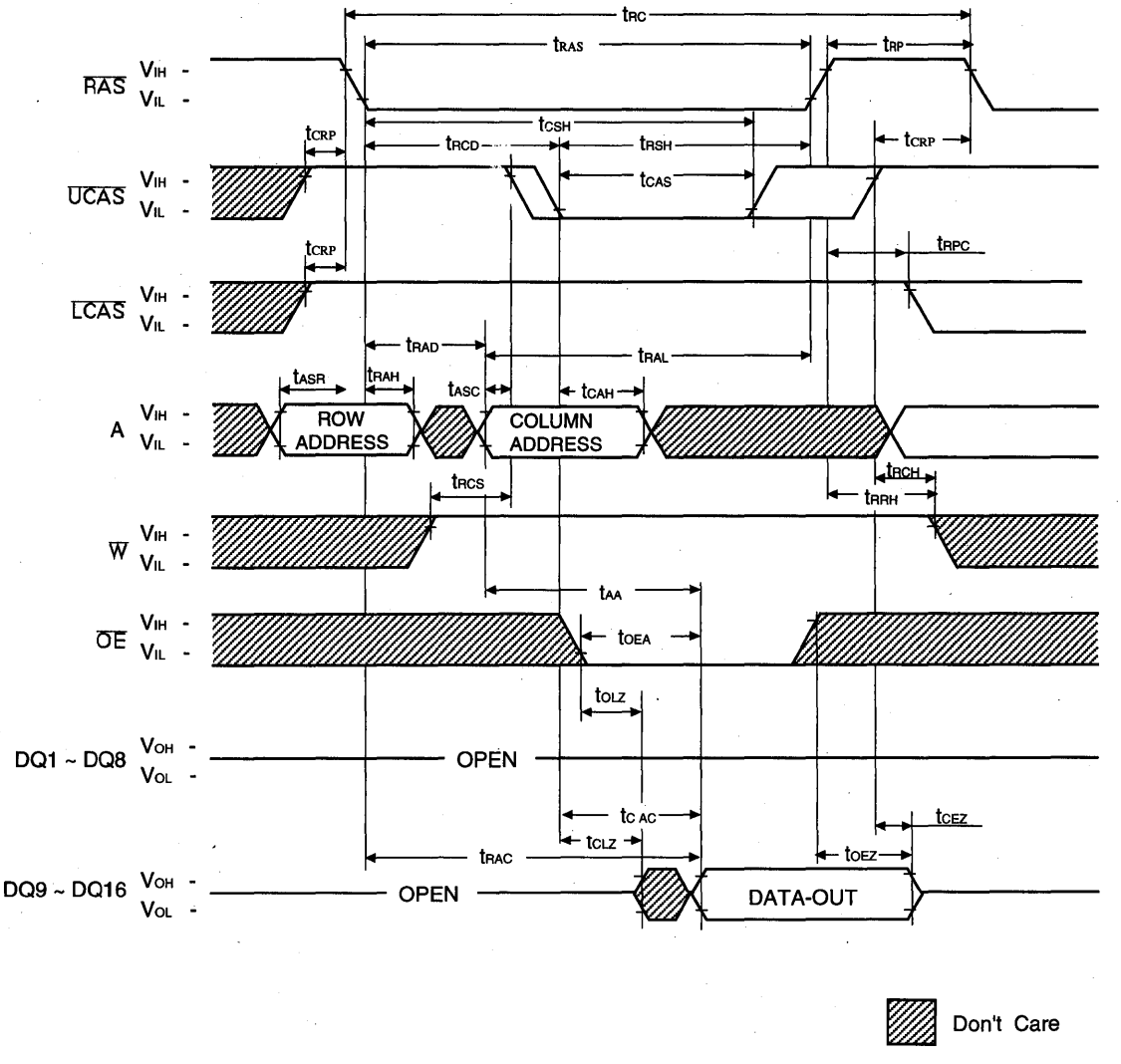
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

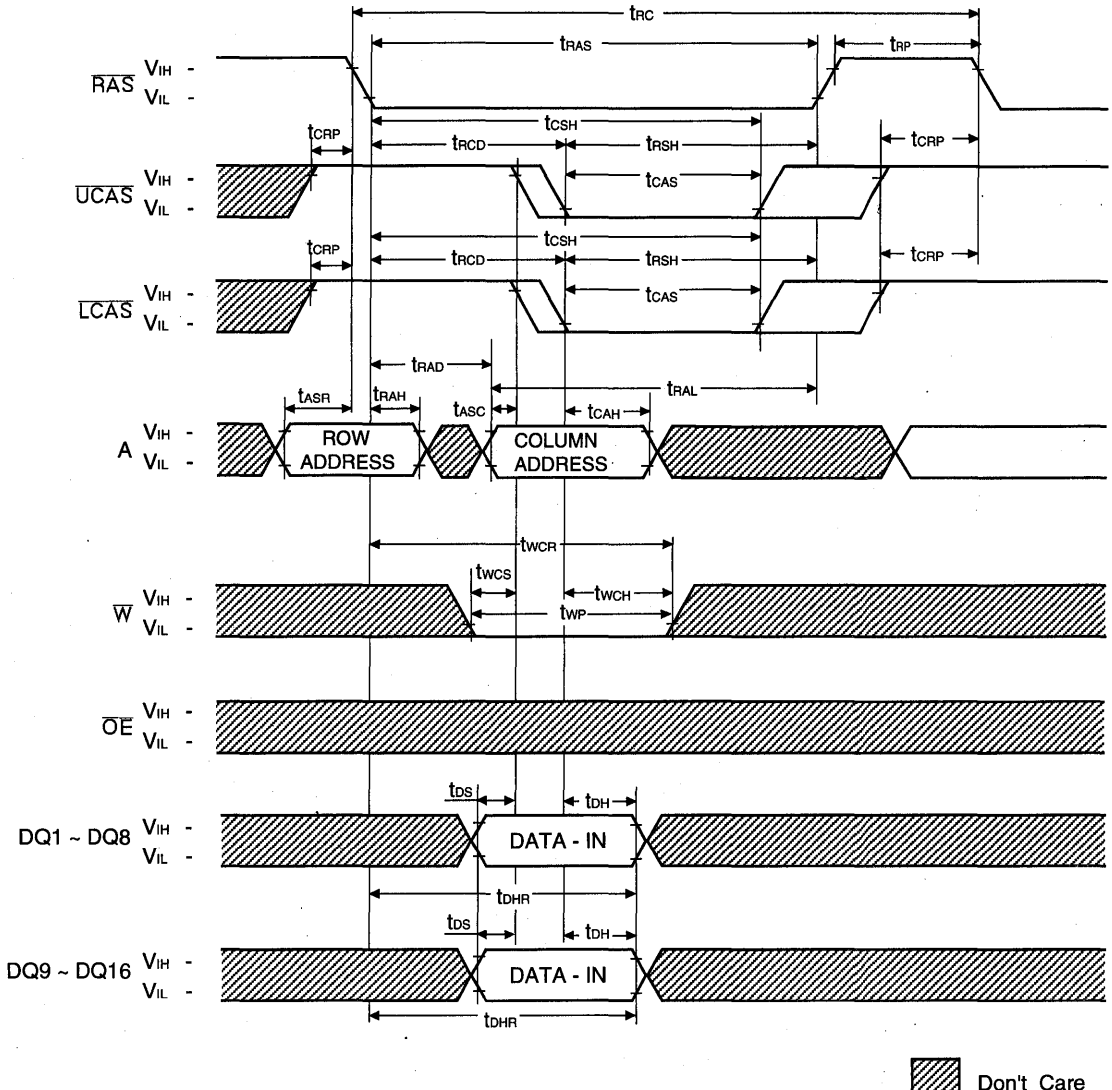
UPPER BYTE READ CYCLE

NOTE : D_{IN} = OPEN



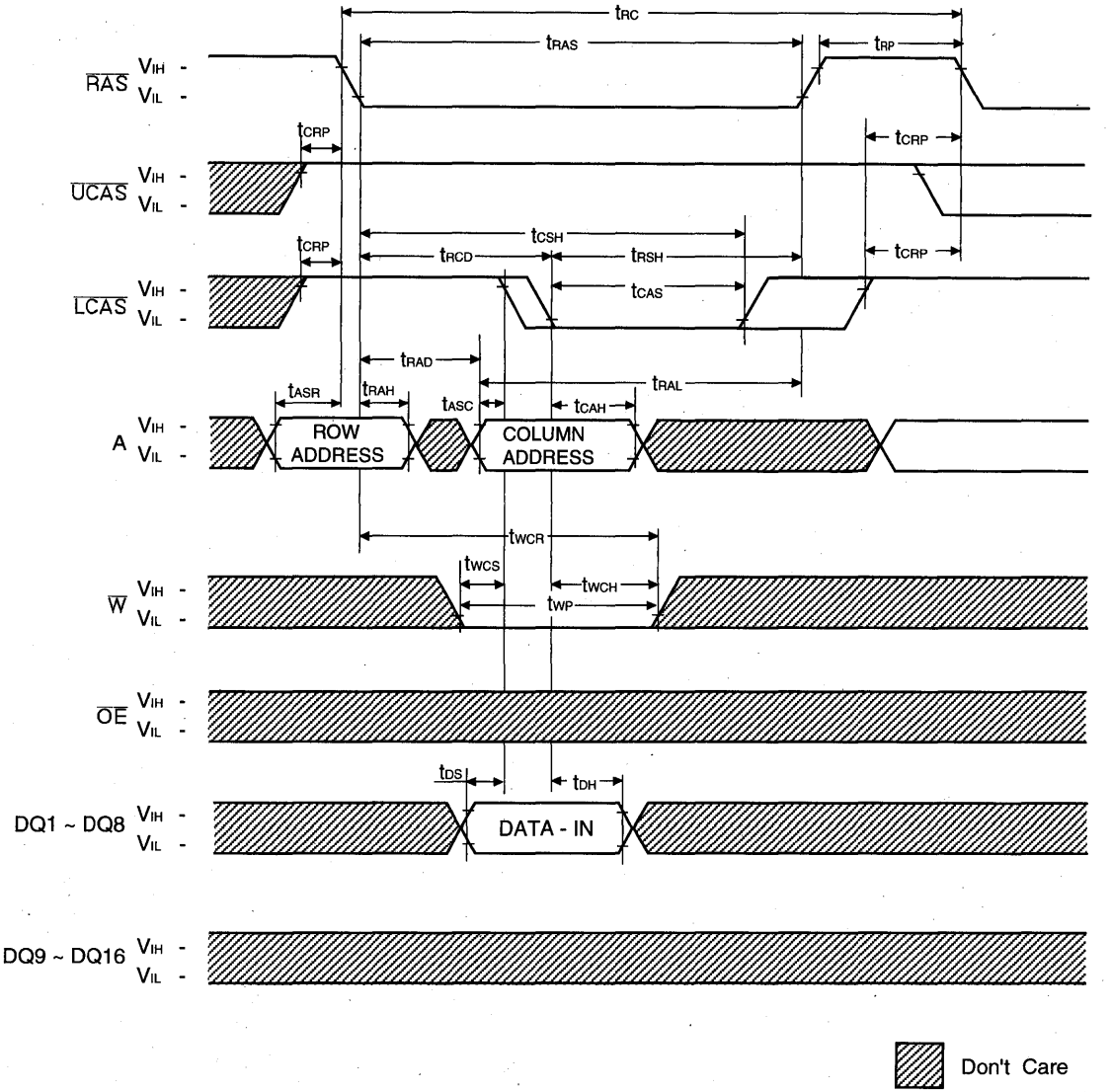
WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



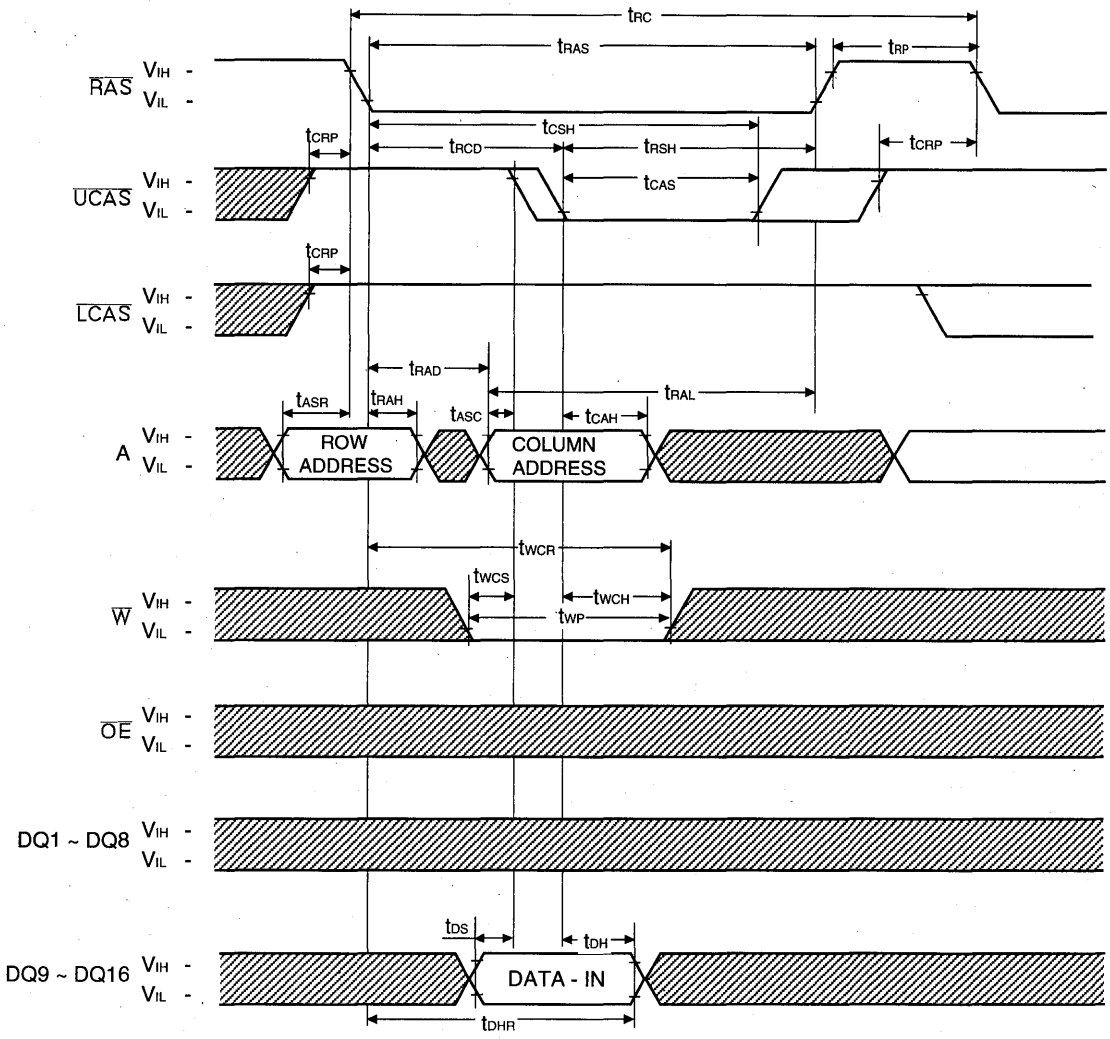
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



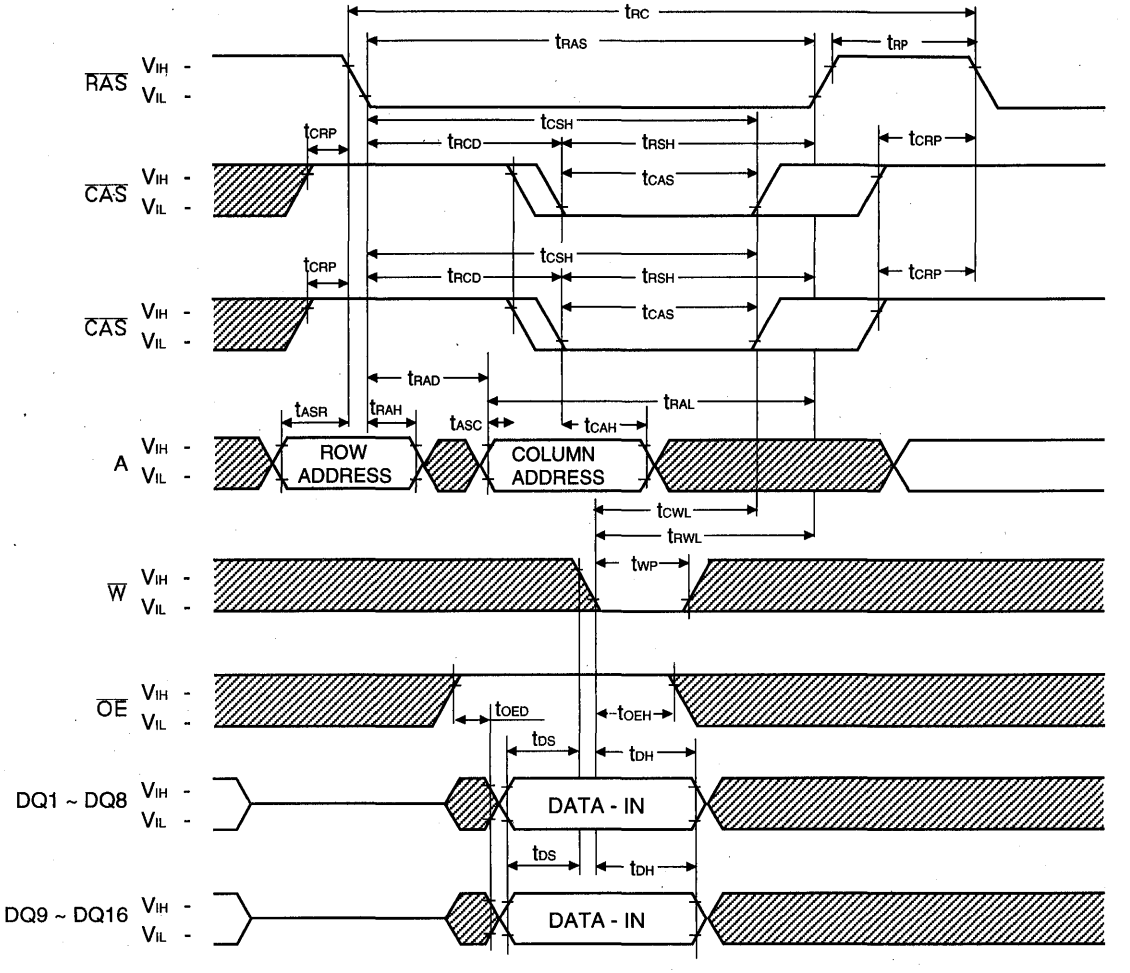
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



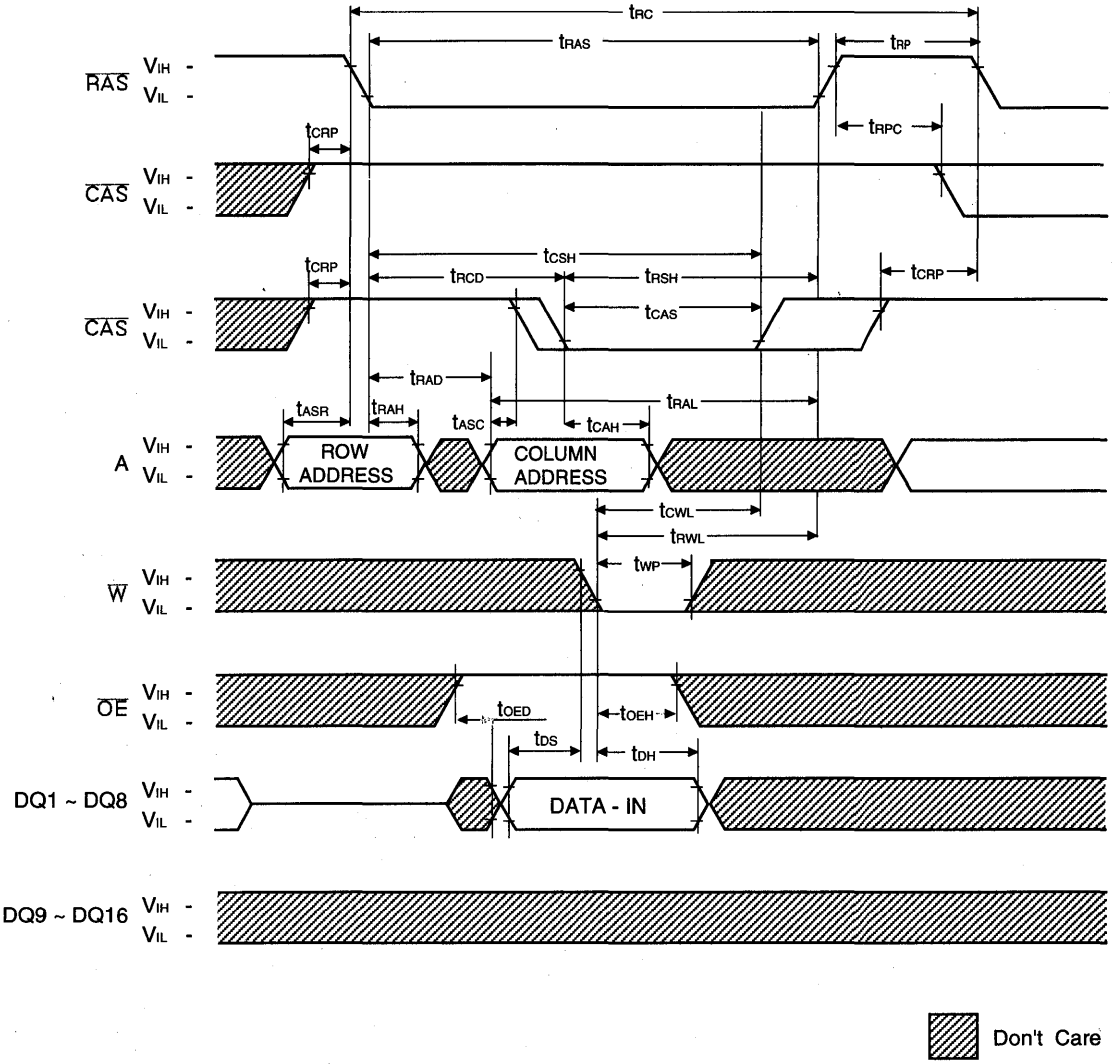
WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



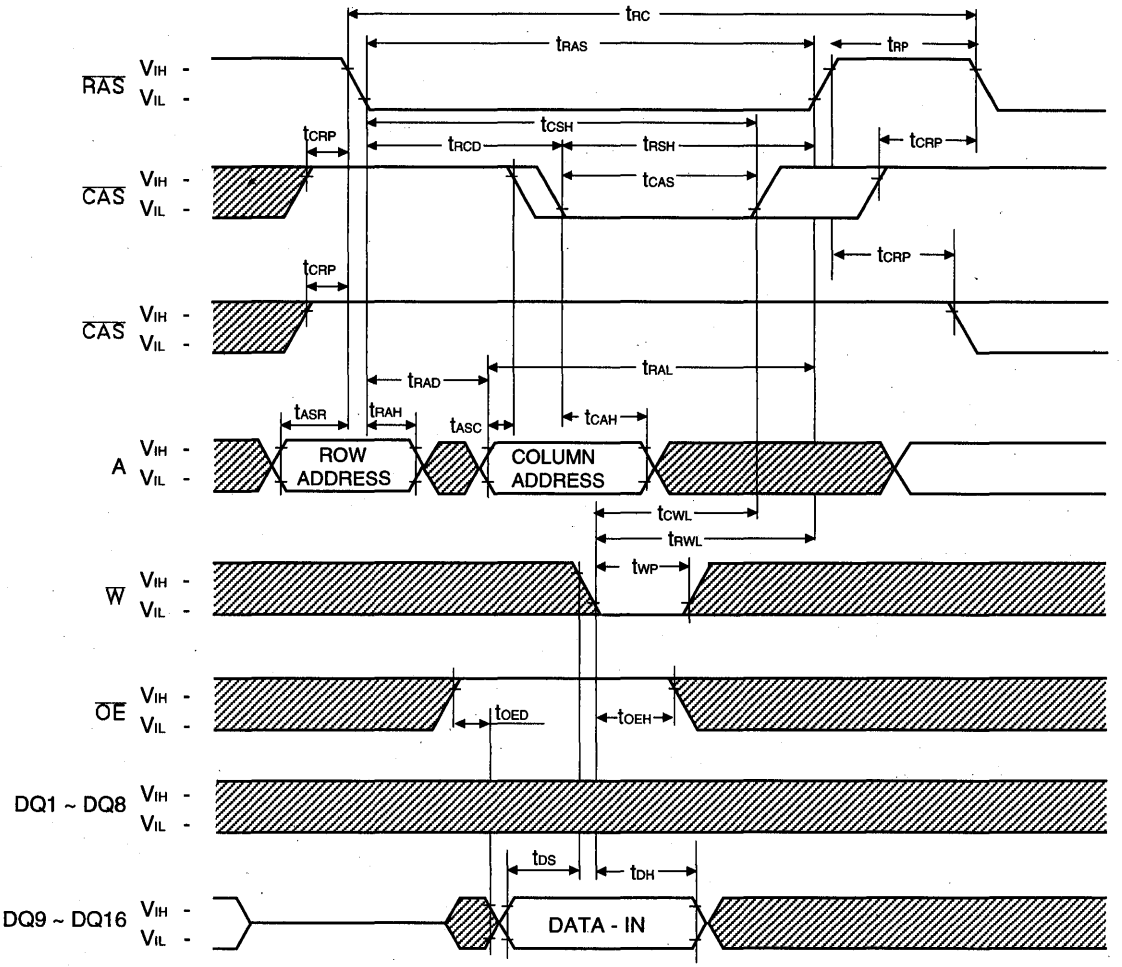
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

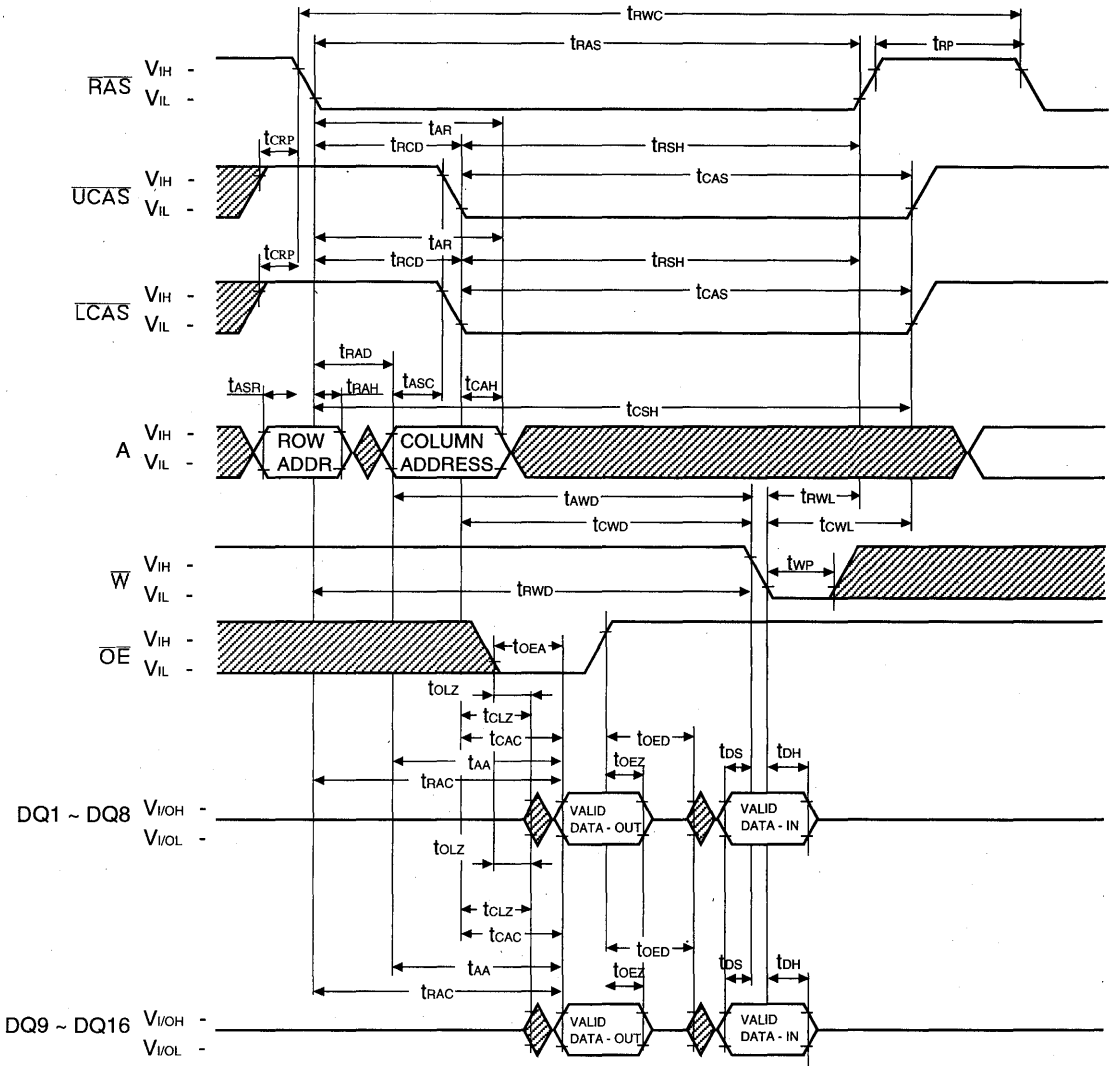


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

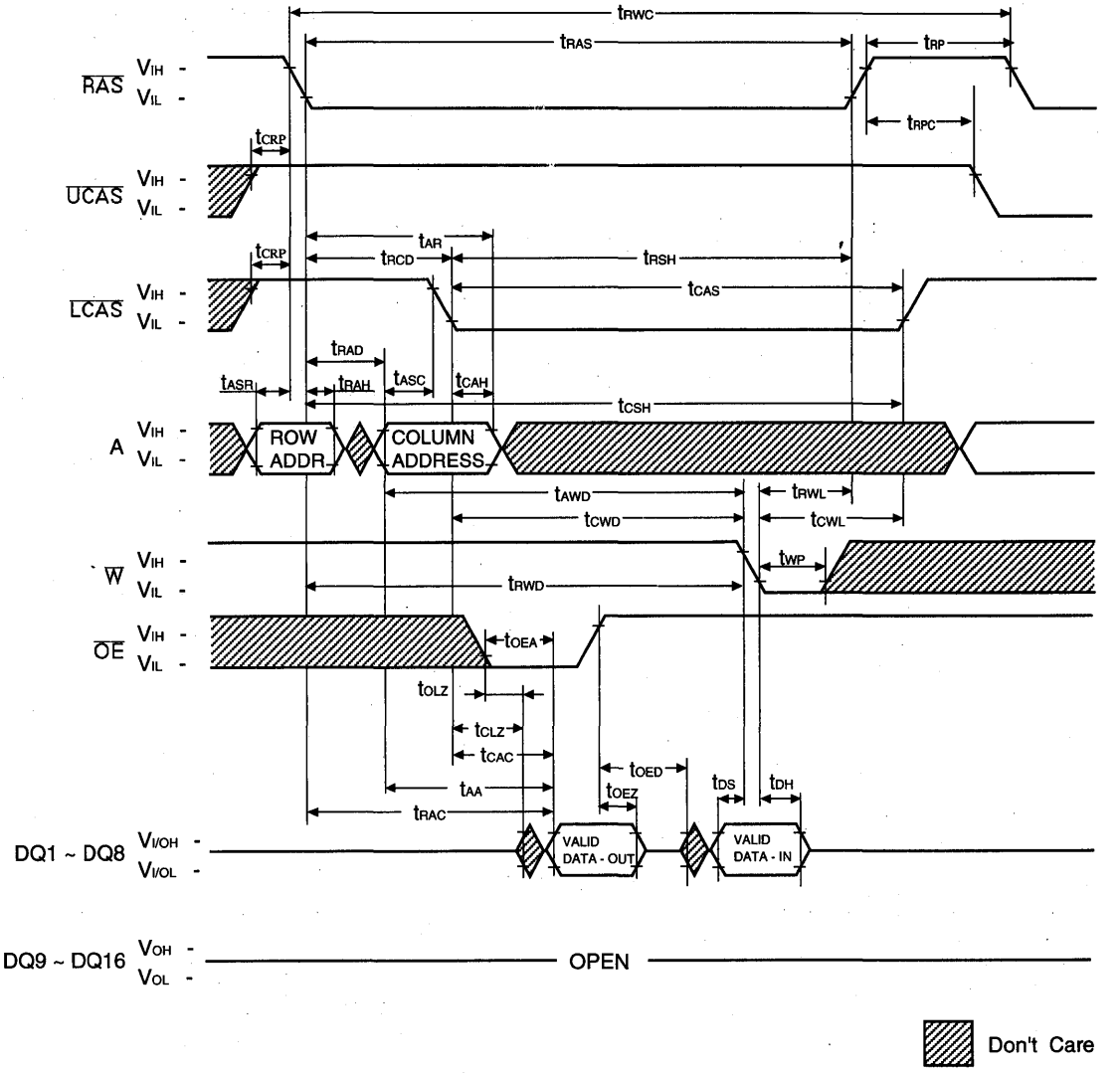
NOTE : D_{OUT} = OPEN



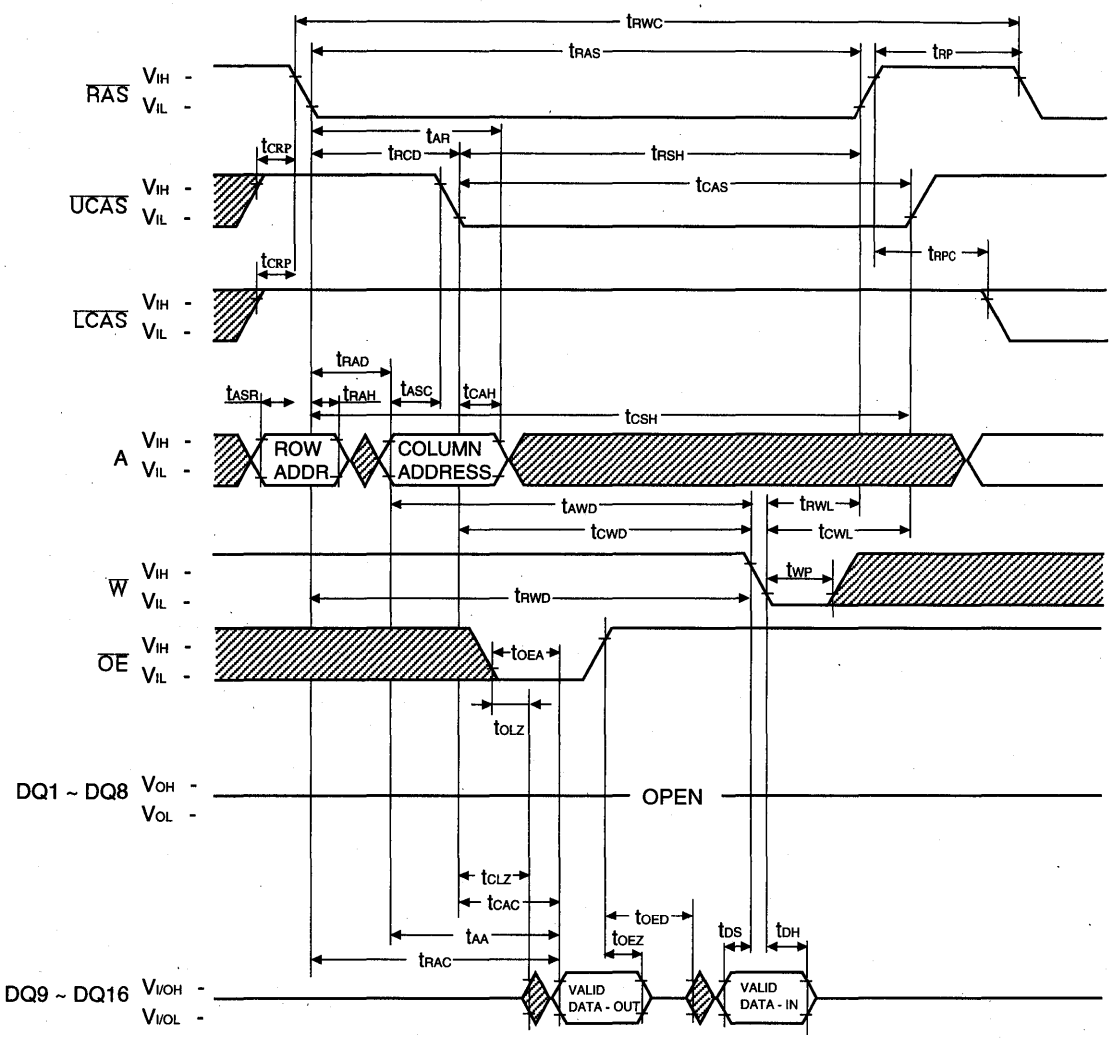
WORD READ - MODIFY - WRITE CYCLE



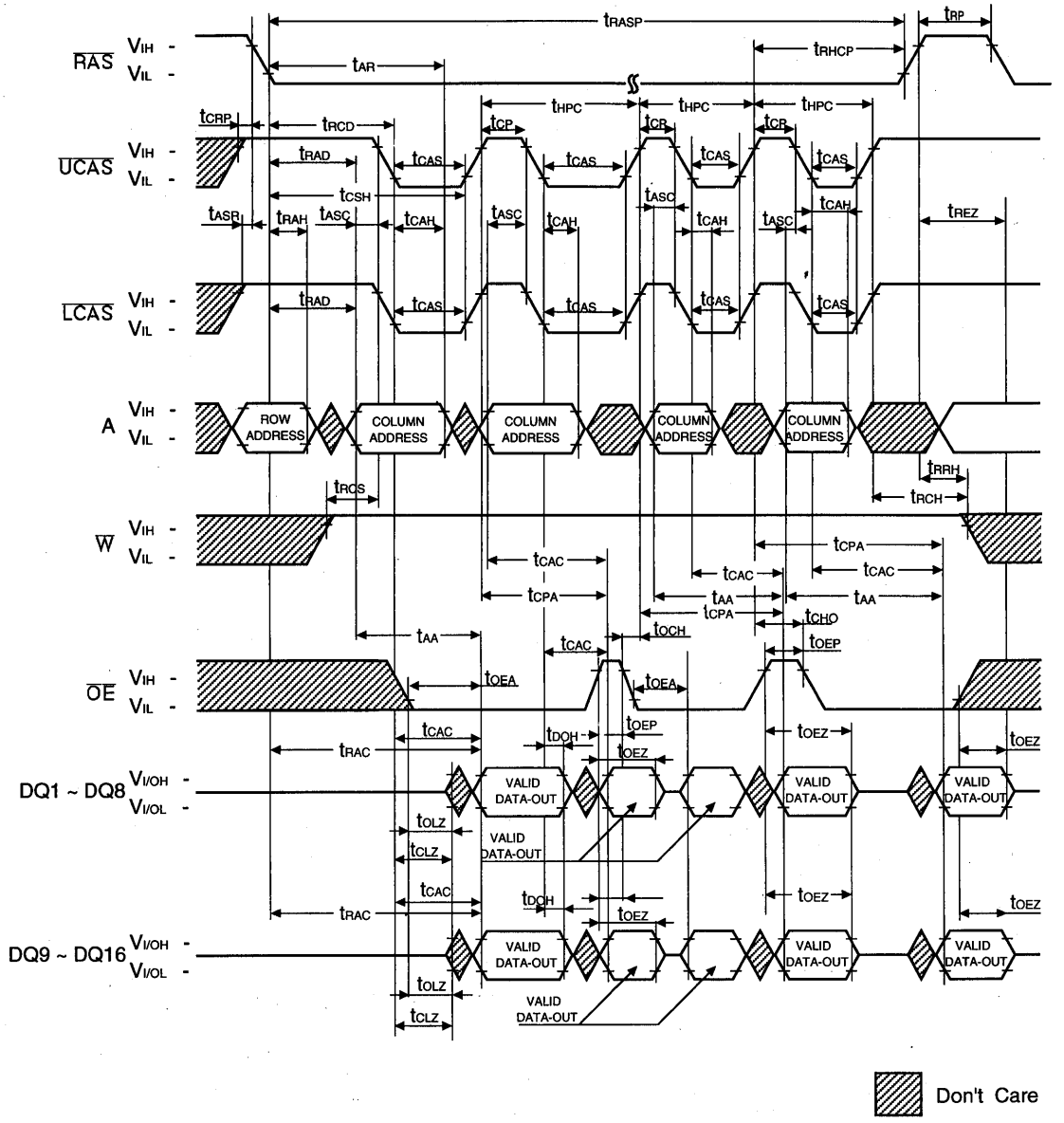
LOWER-BYTE READ - MODIFY - WRITE CYCLE



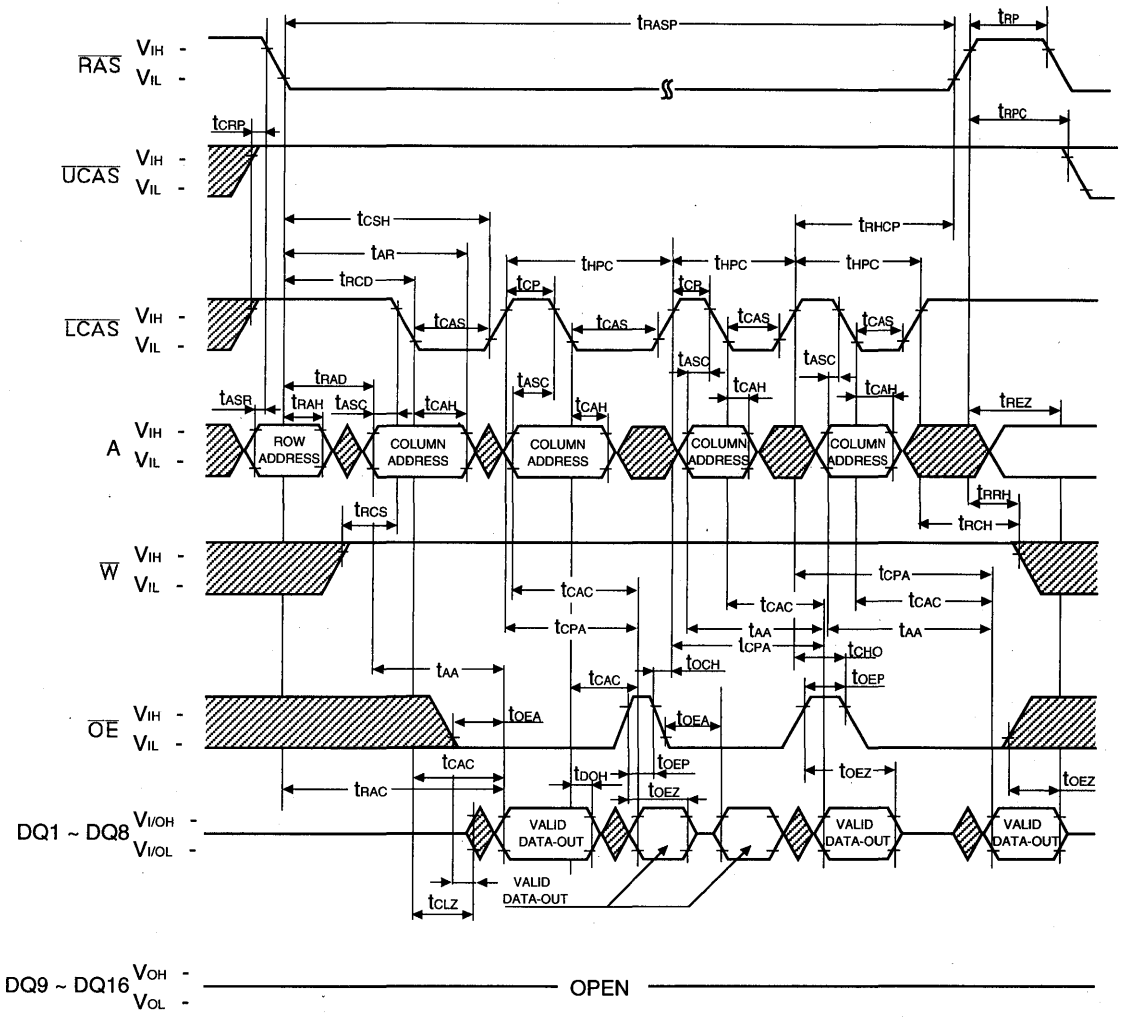
UPPER-BYTE READ - MODIFY - WRITE CYCLE



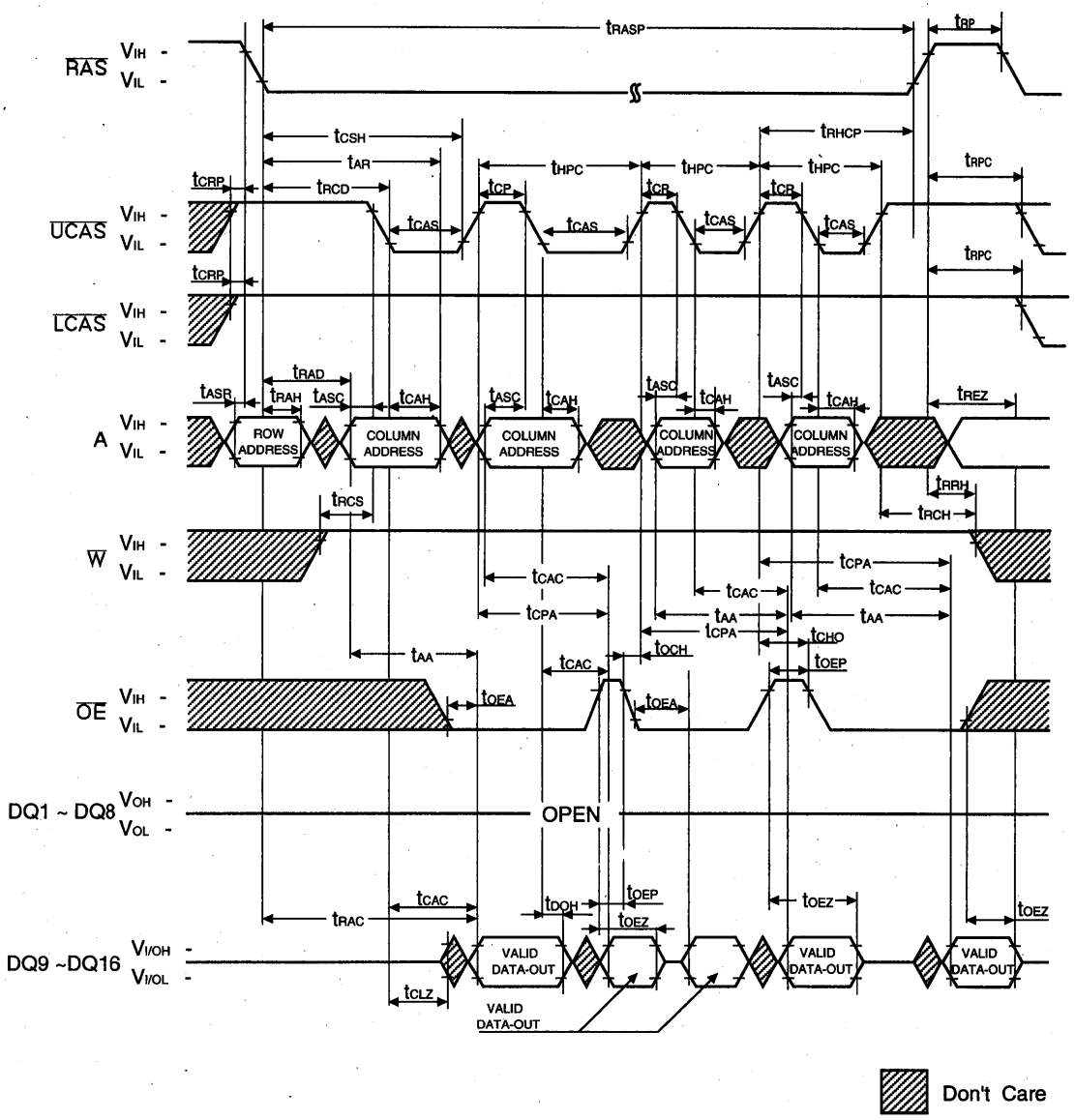
HYPER PAGE MODE WORD READ CYCLE



HYPER PAGE MODE LOWER BYTE READ CYCLE

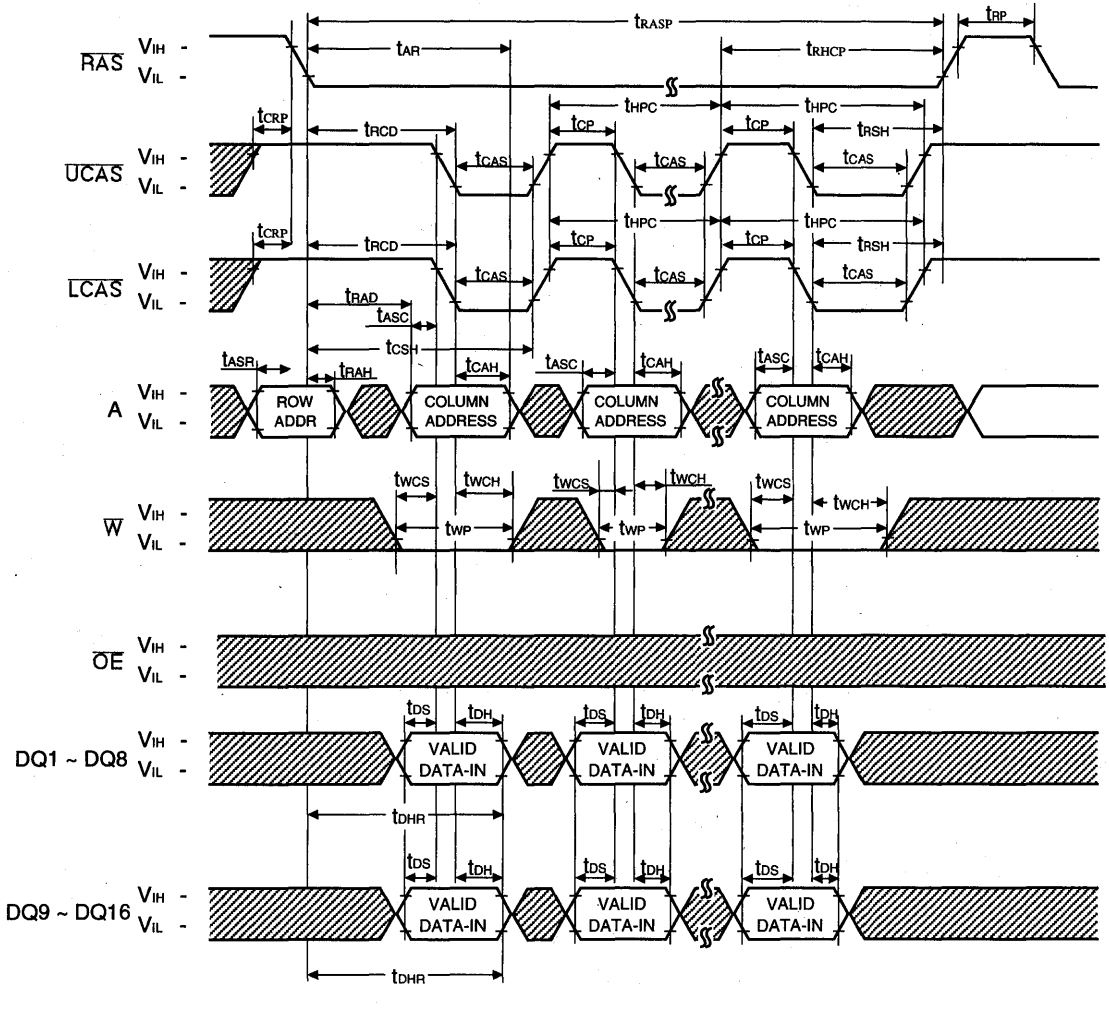


HYPER PAGE MODE UPPER BYTE READ CYCLE



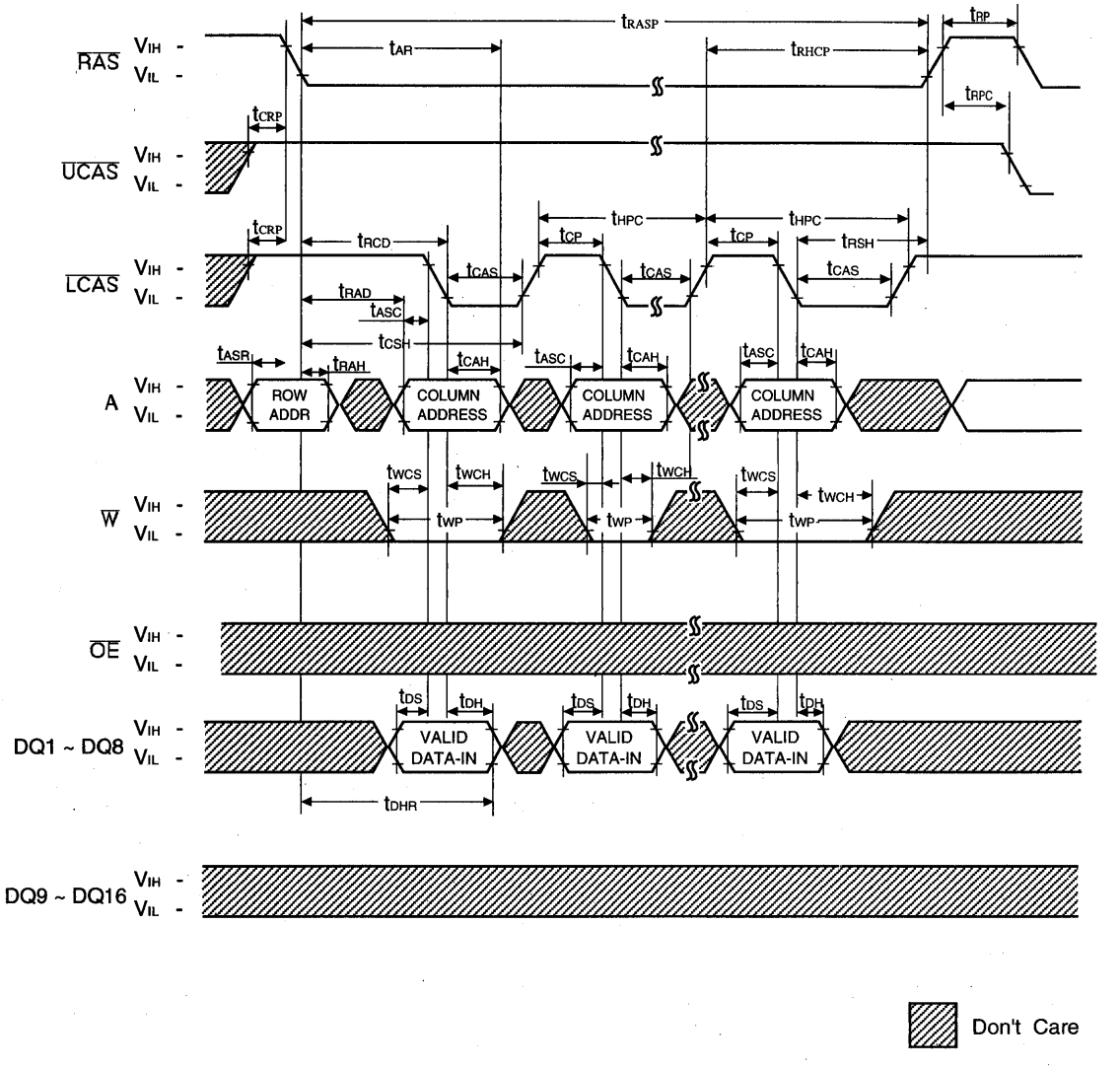
HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



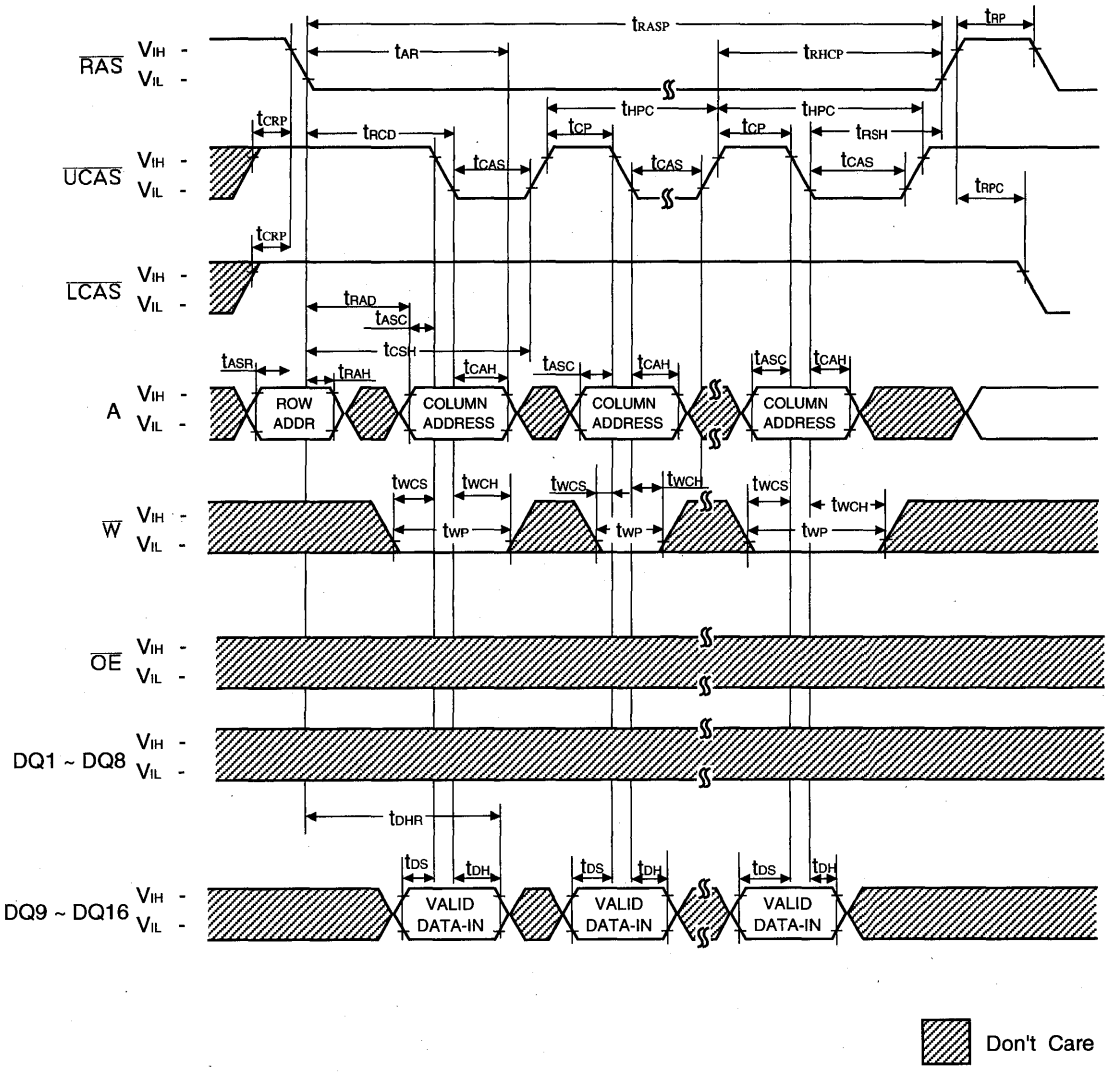
HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open

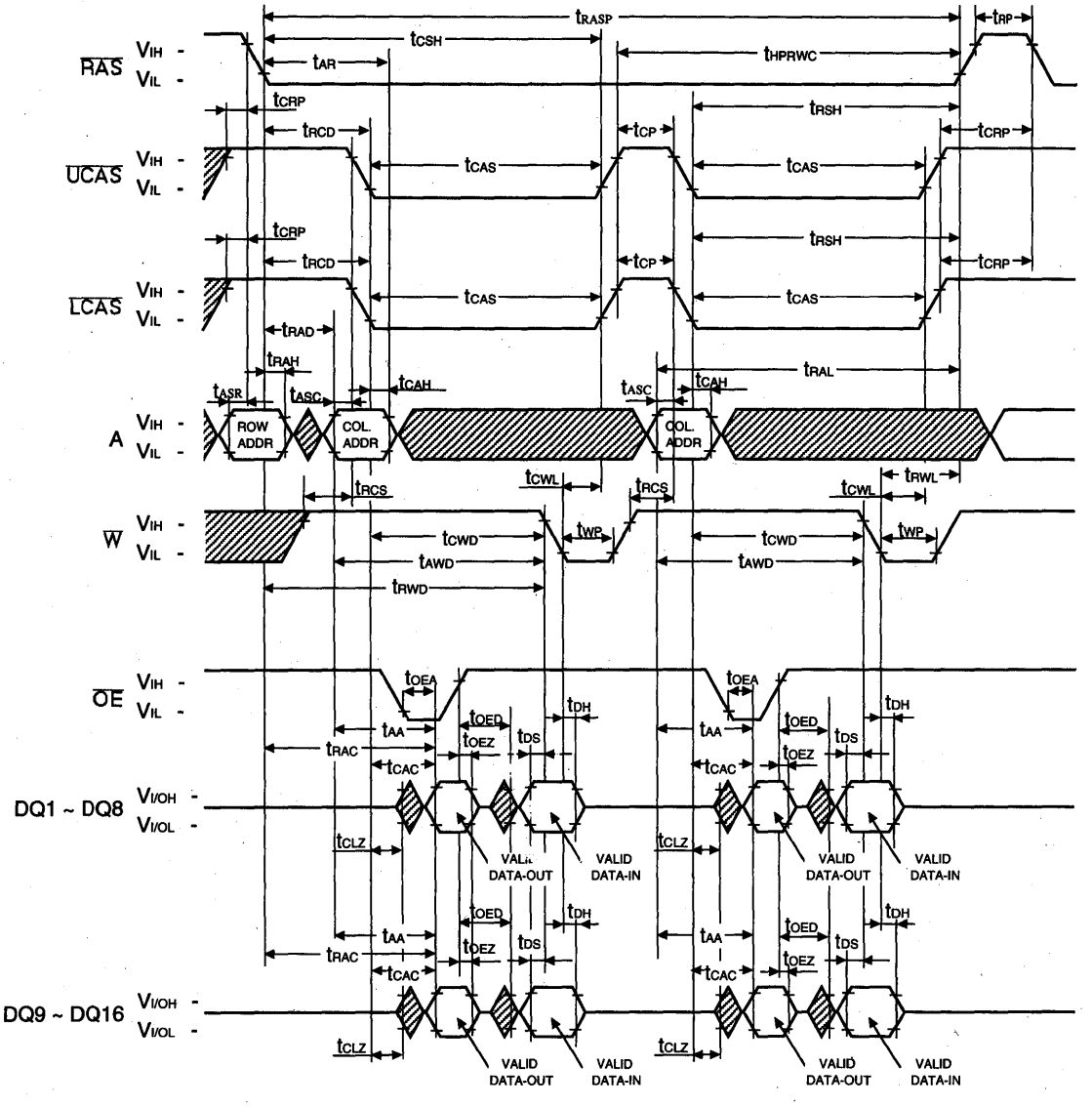


HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

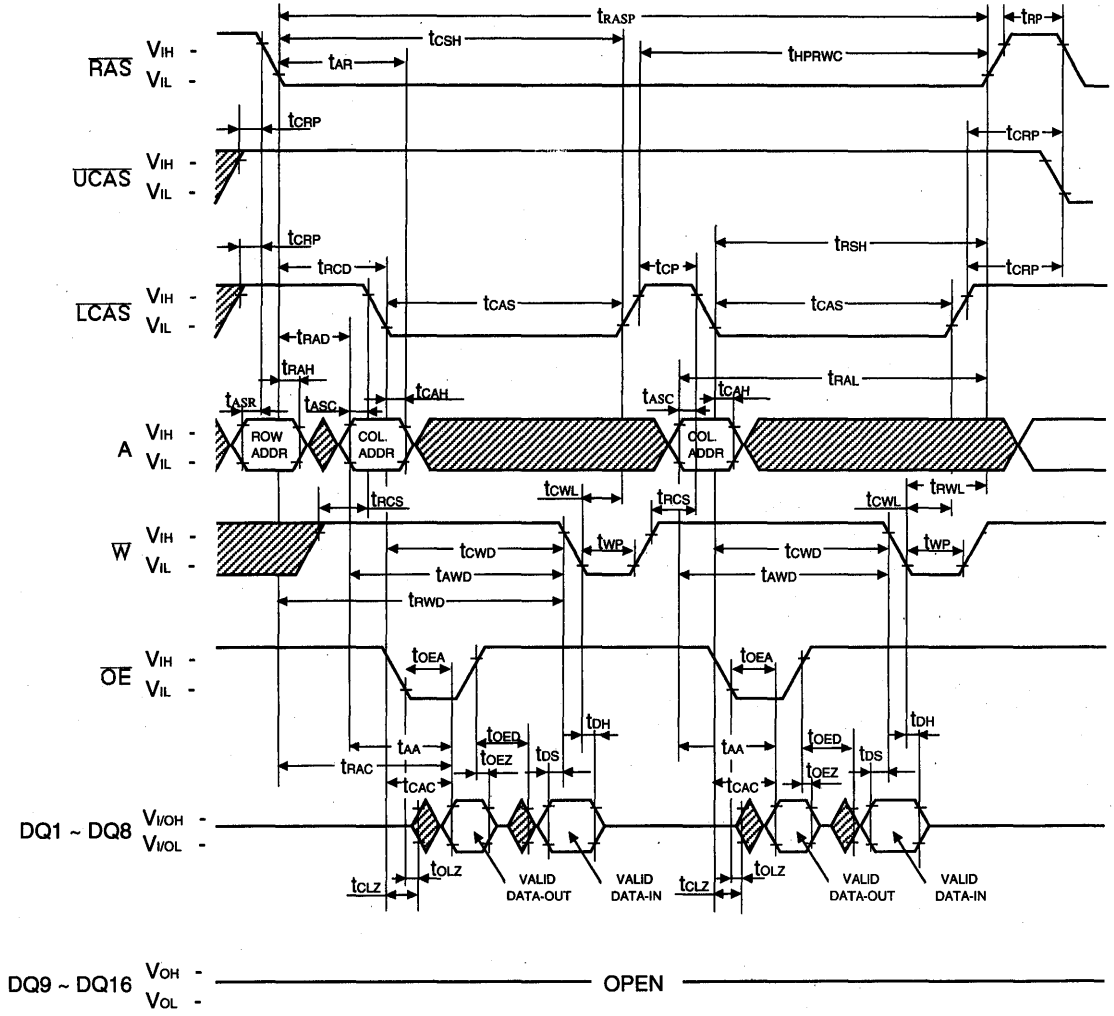
NOTE : D_{OUT} = Open



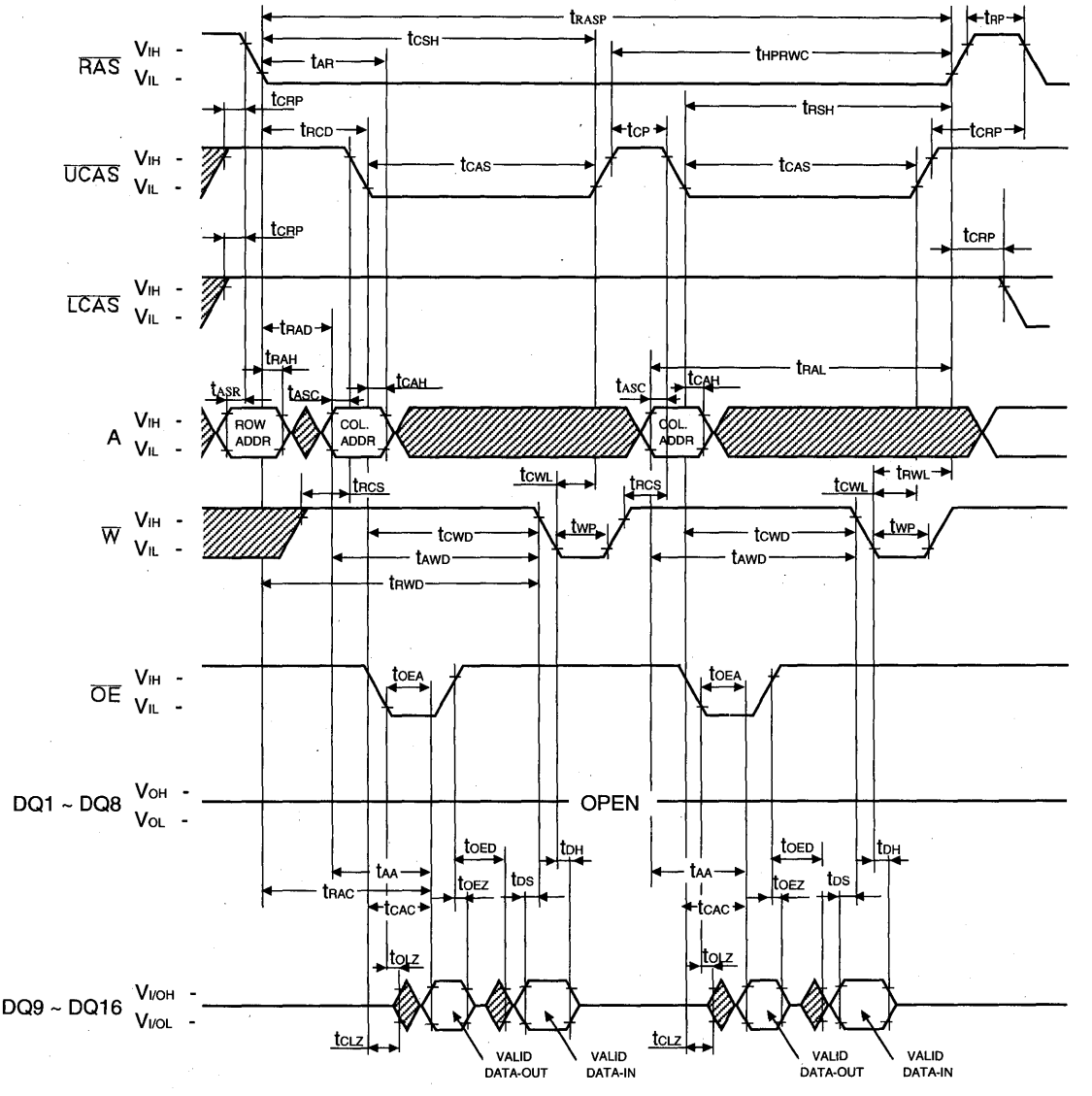
HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE



HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE

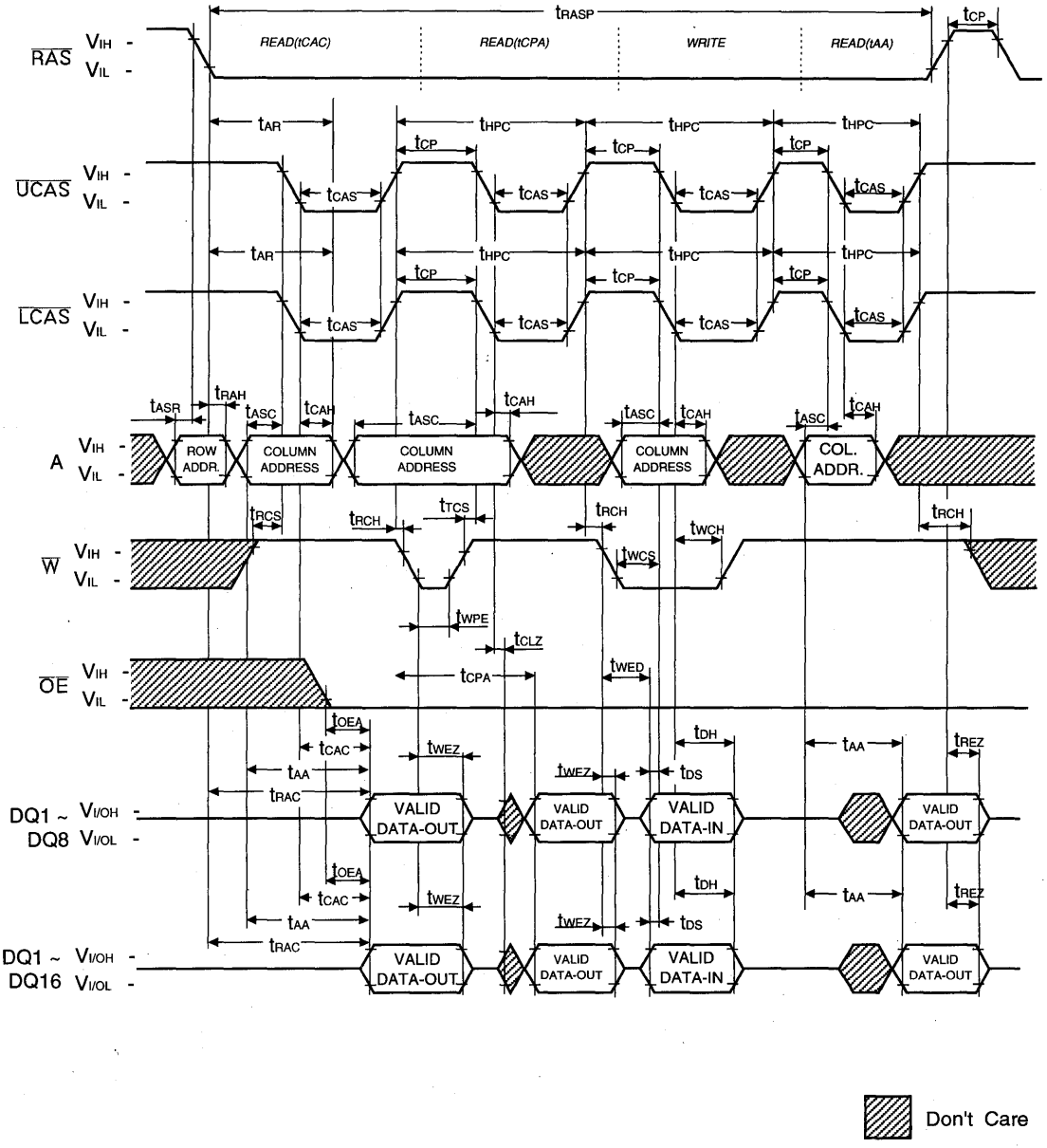


HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



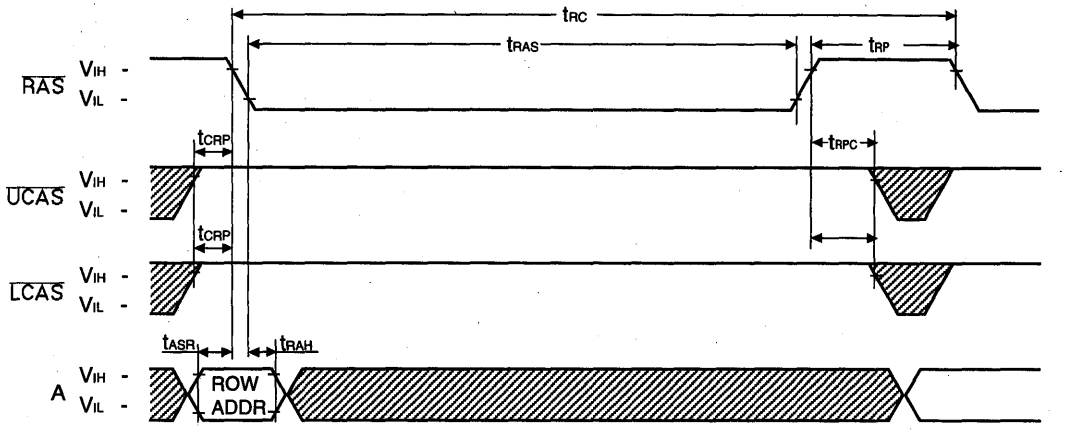
SAMSUNG ELECTRONICS

HYPER PAGE READ AND WRITE MIXED CYCLE



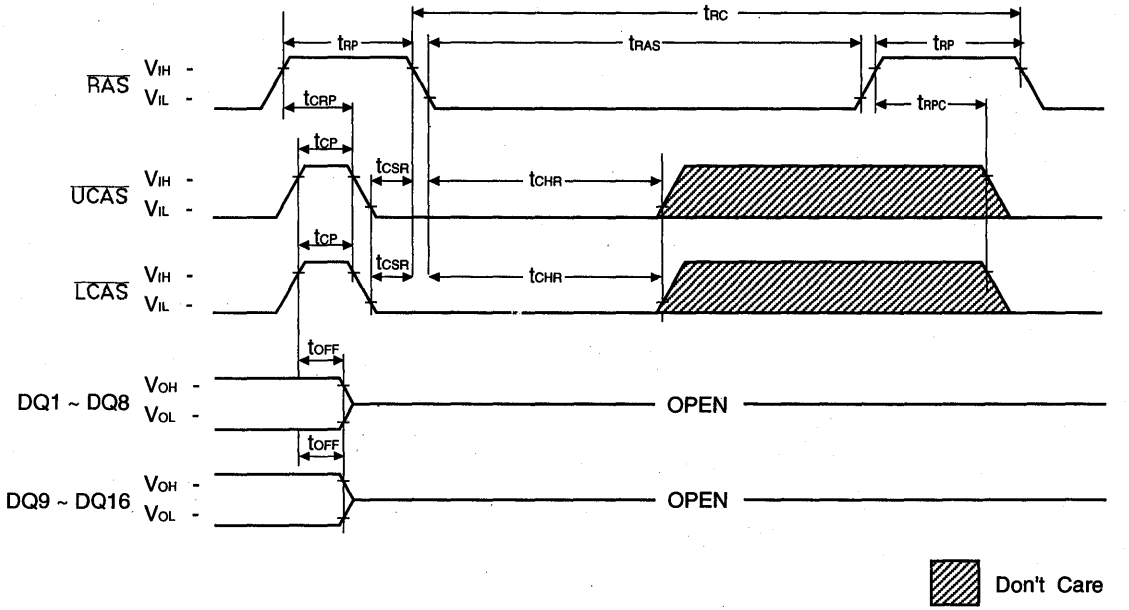
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



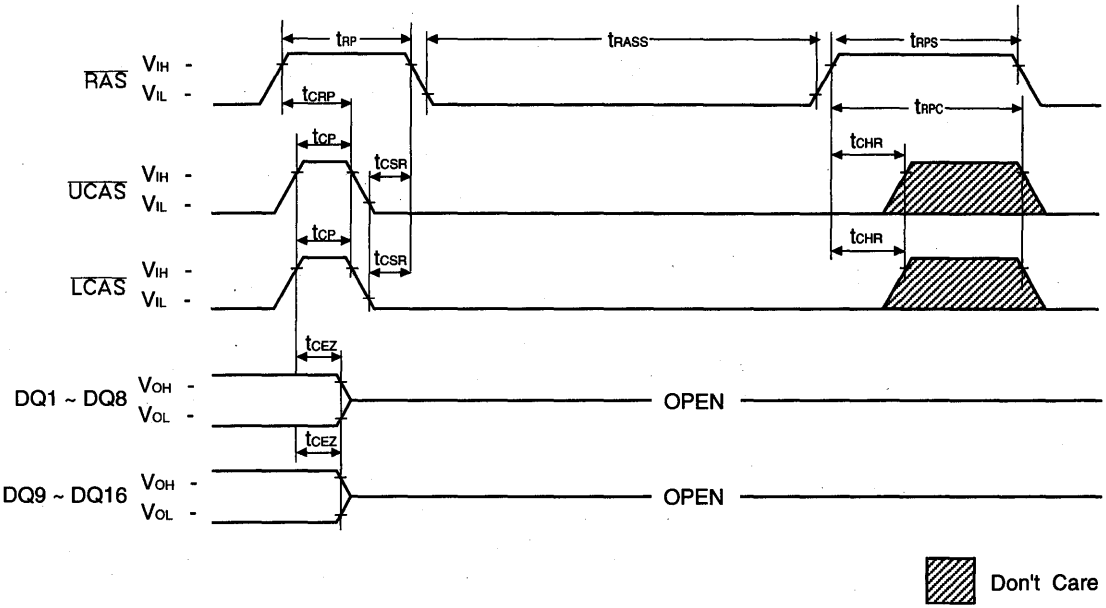
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



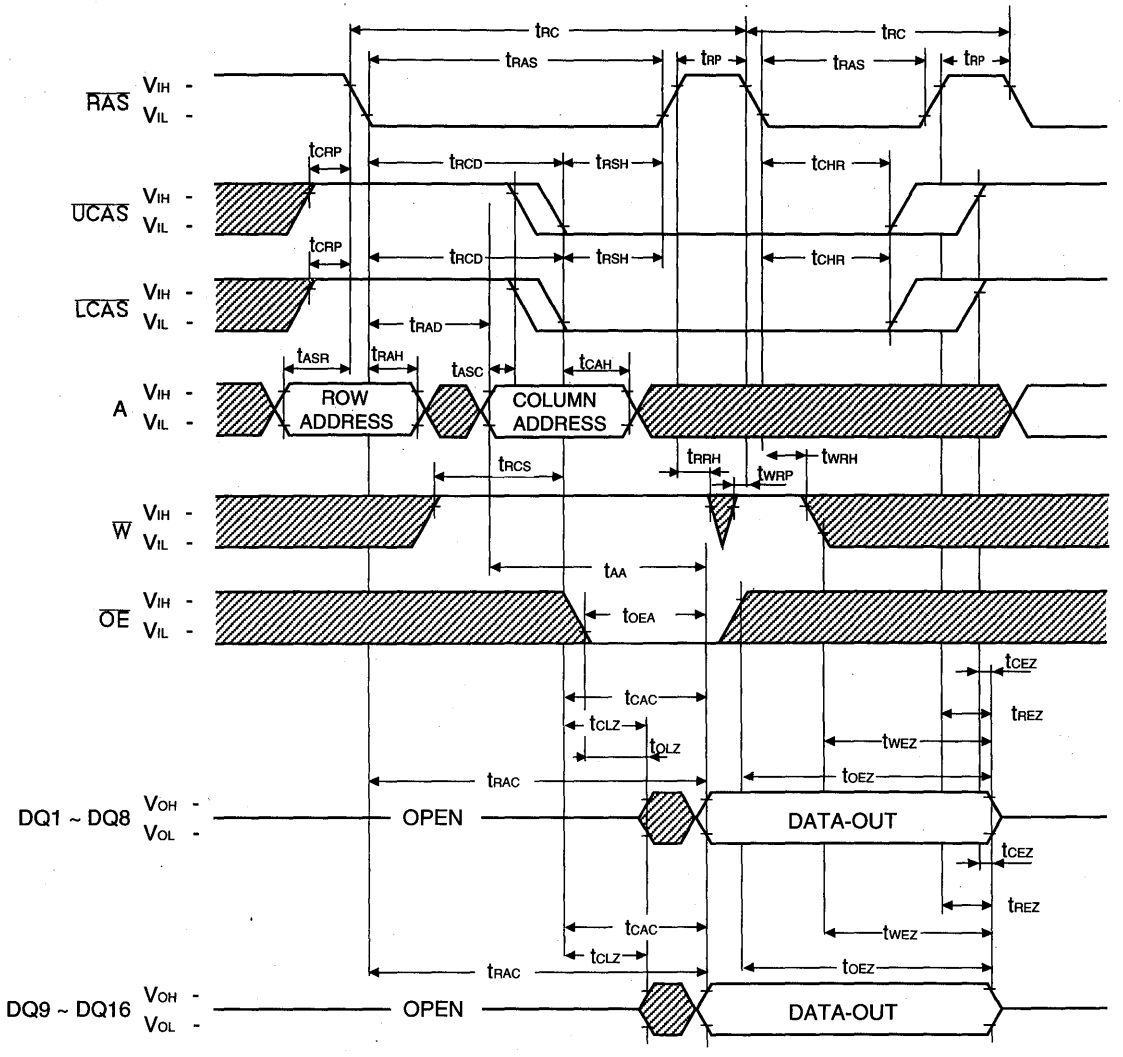
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE(LL-version)

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



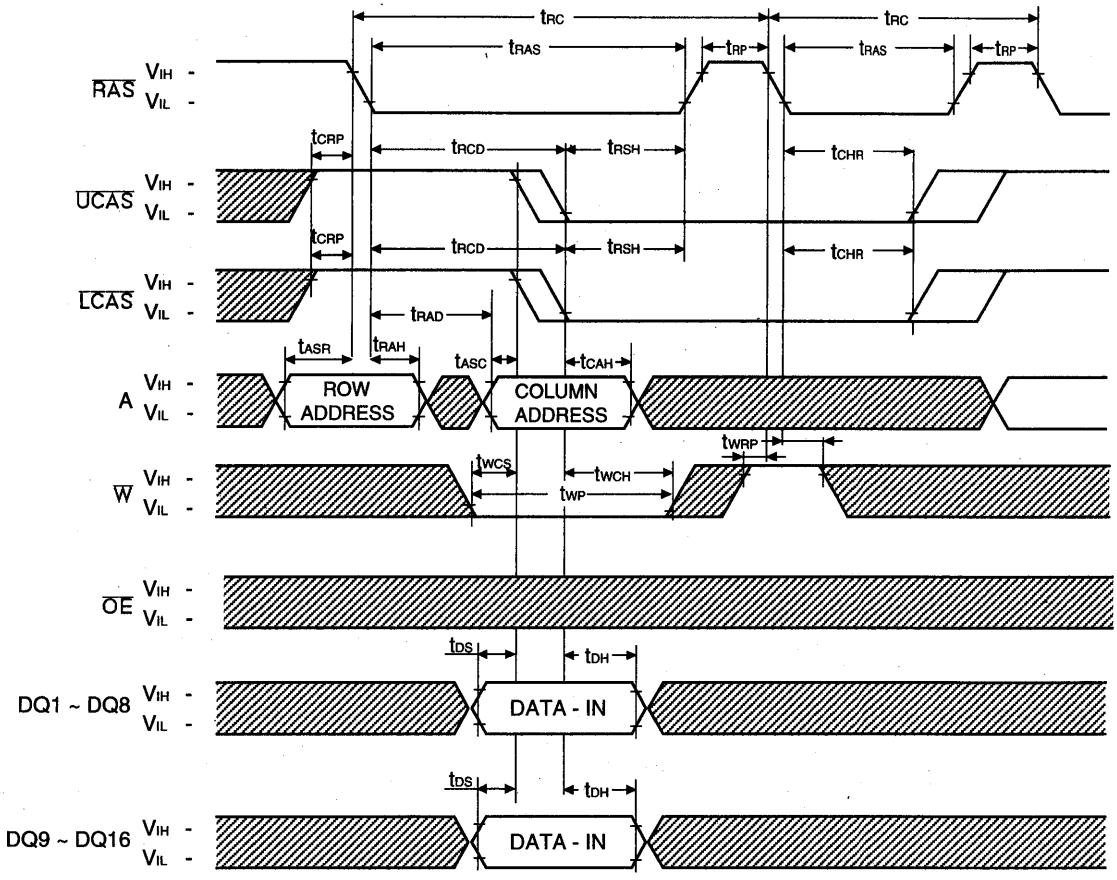
6

HIDDEN REFRESH CYCLE (READ)



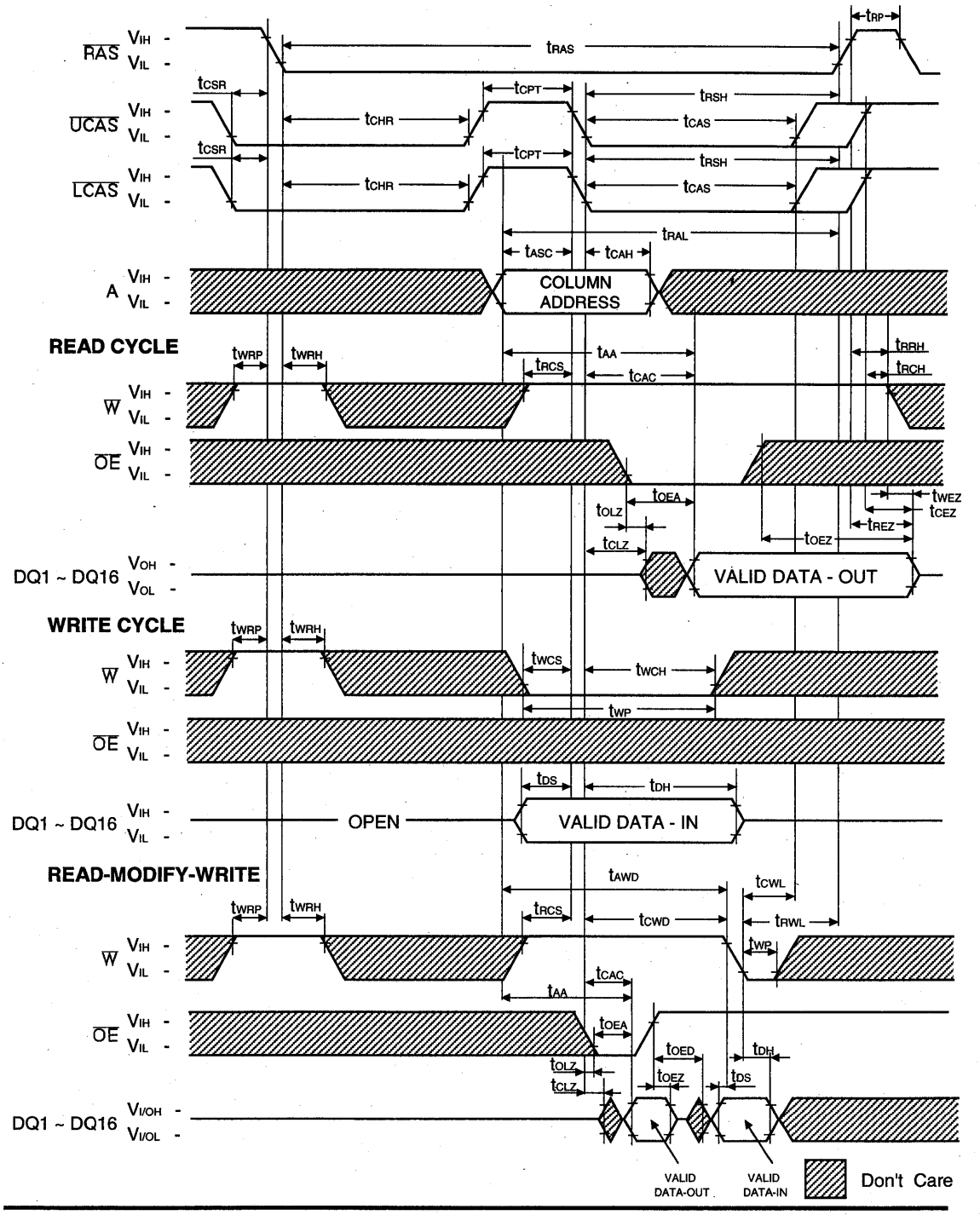
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



Don't Care

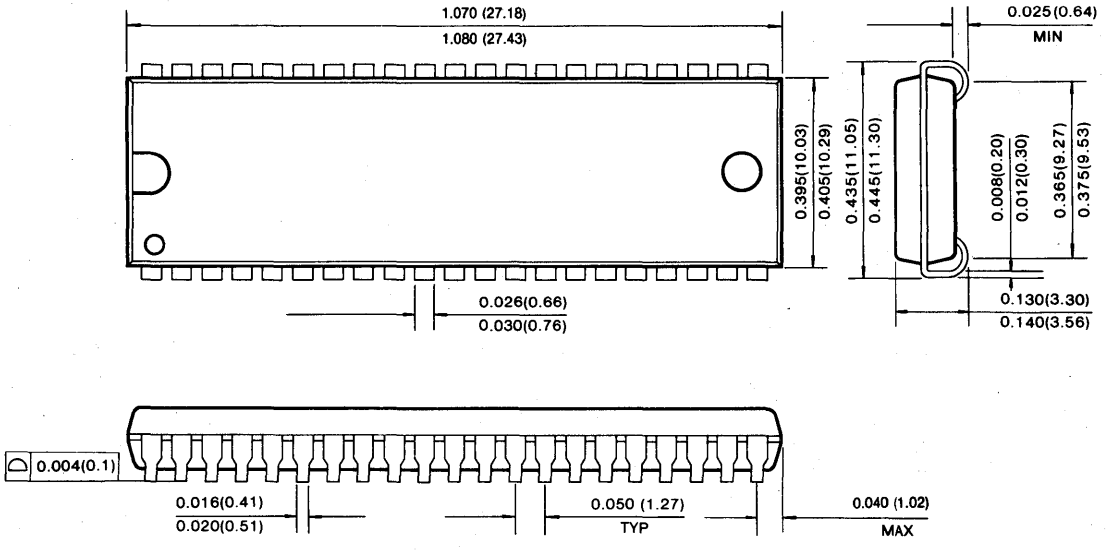
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



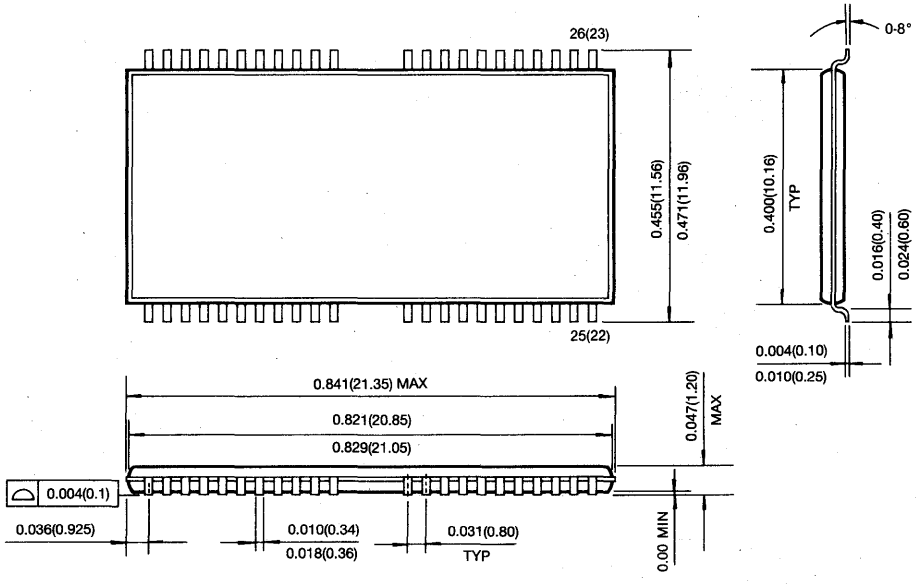
PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



1M x 16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM416C1204A-6/A-L6/A-F6	60ns	17ns	110ns	24ns
KM416C1204A-7/A-L7/A-F7	70ns	20ns	130ns	29ns
KM416C1204A-8/A-L8/A-F8	80ns	20ns	150ns	34ns

- **Extended Data Out Mode (Fast Page Mode with Extended Data Out)**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +5V±10% power supply**
- **Refresh Cycle**
  - **-1024 cycle/16ms (Normal)**
  - **-1024 cycle/128ms (L-version)**
  - **-1024 cycle/128ms (F-version)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

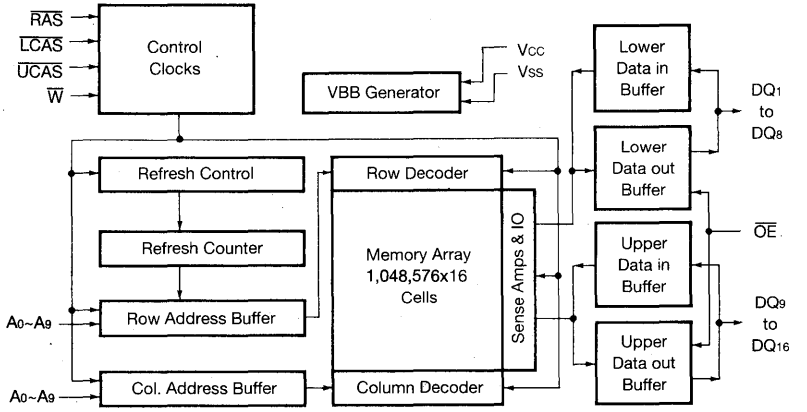
GENERAL DESCRIPTION

The Samsung KM416C1204A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

The KM416C1204A/A-L/A-F features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416C1204A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

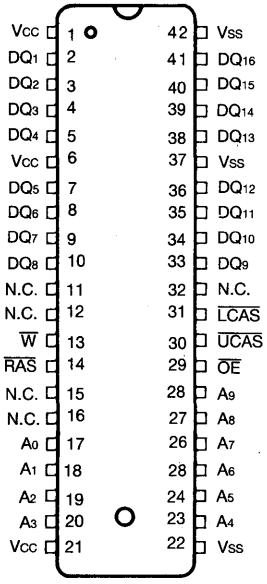
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

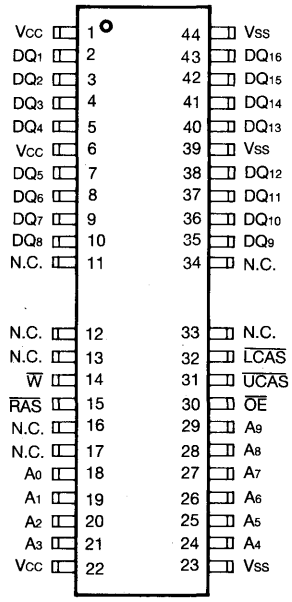
PIN CONFIGURATION (Top Views)

• KM416C1204AJ



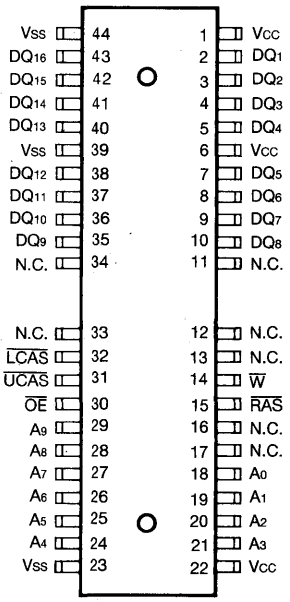
(SOJ)

• KM416C1204AT



(TSOP(II)-Forword)

• KM416C1204AR



(TSOP(II)-Reverse)

Pin Name	Pin Function
A0-A9	Address Inputs
DQ1-16	Data In/Out
VSS	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VCC	Power(+5V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 t0 + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{RC}=min.)	KM416C1204A-6/A-L6/A-F6 KM416C1204A-7/A-L7/A-F7 KM416C1204A-8/A-L8/A-F8	I_{CC1}	-	160 150 140	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})	KM416C1204A KM416C1204A-L KM416C1204A-F	I_{CC2}	-	2 1 1	mA mA mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM416C1204A-6/A-L6/A-F6 KM416C1204A-7/A-L7/A-F7 KM416C1204A-8/A-L8/A-F8	I_{CC3}	-	160 150 140	mA mA mA
EDO Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC}=min.)	KM416C1204A-6/A-L6/A-F6 KM416C1204A-7/A-L7/A-F7 KM416C1204A-8/A-L8/A-F8	I_{CC4}	-	130 120 110	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)	KM416C1204A KM416C1204A-L KM416C1204A-F	I_{CC5}	-	1 300 200	mA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC}=min.)	KM416C1204A-6/A-L6/A-F6 KM416C1204A-7/A-L7/A-F7 KM416C1204A-8/A-L8/A-F8	I_{CC6}	-	160 150 140	mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V, Input Low Voltage(V_{IL})=0.2V $\overline{UCAS}$, $\overline{LCAS}$= 0.2V D_{IN}=Don't Care, t_{RC}=125μs (L-Ver) t_{RAS}=t_{RAS} min~300ns	KM416C1204A-L	I_{CC7}	-	350	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_9=V_{CC}-0.2V or 0.2V DQ_1-DQ_{16}=V_{CC}-0.2V or 0.2V or Open	KM416C1204A-F	I_{CCS}	-	250	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 V)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once while one Hyper page mode cycle time t_{HPC}.

CAPACITANCE (T_A=25°C, V_{CC}=5V. f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5V±10%, See notes 1,2)

(Test condition : V_{IH}/V_{IL}=2.4V/0.8V, V_{OH}/V_{OL}=2.0V/0.8V, Output Loading C_L=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		17		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	17		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	15	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	15
Column address hold time	tCAH	10		15		15		ns	15
Column address hold time referenced to $\overline{RAS}$	tAR	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	10		15		20		ns	18
Data-in set-up time	tDS	0		0		0		ns	10,21
Data-in hold time	tDH	10		15		15		ns	10,21
Data-in hold time referenced to $\overline{RAS}$	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		50		50		ns	8,17
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	20
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		25		30		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	15		20		20		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	7
$\overline{OE}$ commend hold time	tOEH	15		20		20		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Hyper Page mode cycle time	t_{HPC}	24		29		34		ns	12
Hyper Page mode read-modify-write cycle time	t_{HPRWC}	76		81		91		ns	12
$\overline{CAS}$ orcgarge time (Hyper page mode)	t_{CP}	10		10		10		ns	16
$\overline{RAS}$ pulse width (Hyper page mode)	t_{RASP}	60	200.000	70	200.000	80	200.000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
Output data hold time	t_{DOH}	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	15	3	20	3	20	ns	7
$\overline{W}$ to data delay	t_{WED}	15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		5		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		5		ns	
$\overline{RAS}$ pulse width (F-ver)	t_{RASS}	100		100		100		μs	13
$\overline{RAS}$ precharge time (F-ver)	t_{RPS}	110		130		150		ns	13
$\overline{CAS}$ hlod time (F-ver)	t_{CHS}	-50		-50		-50		ns	13

KM416C1204A/A-L/A-F Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ_1~DQ_8	DQ_9~DQ_{16}	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	x	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

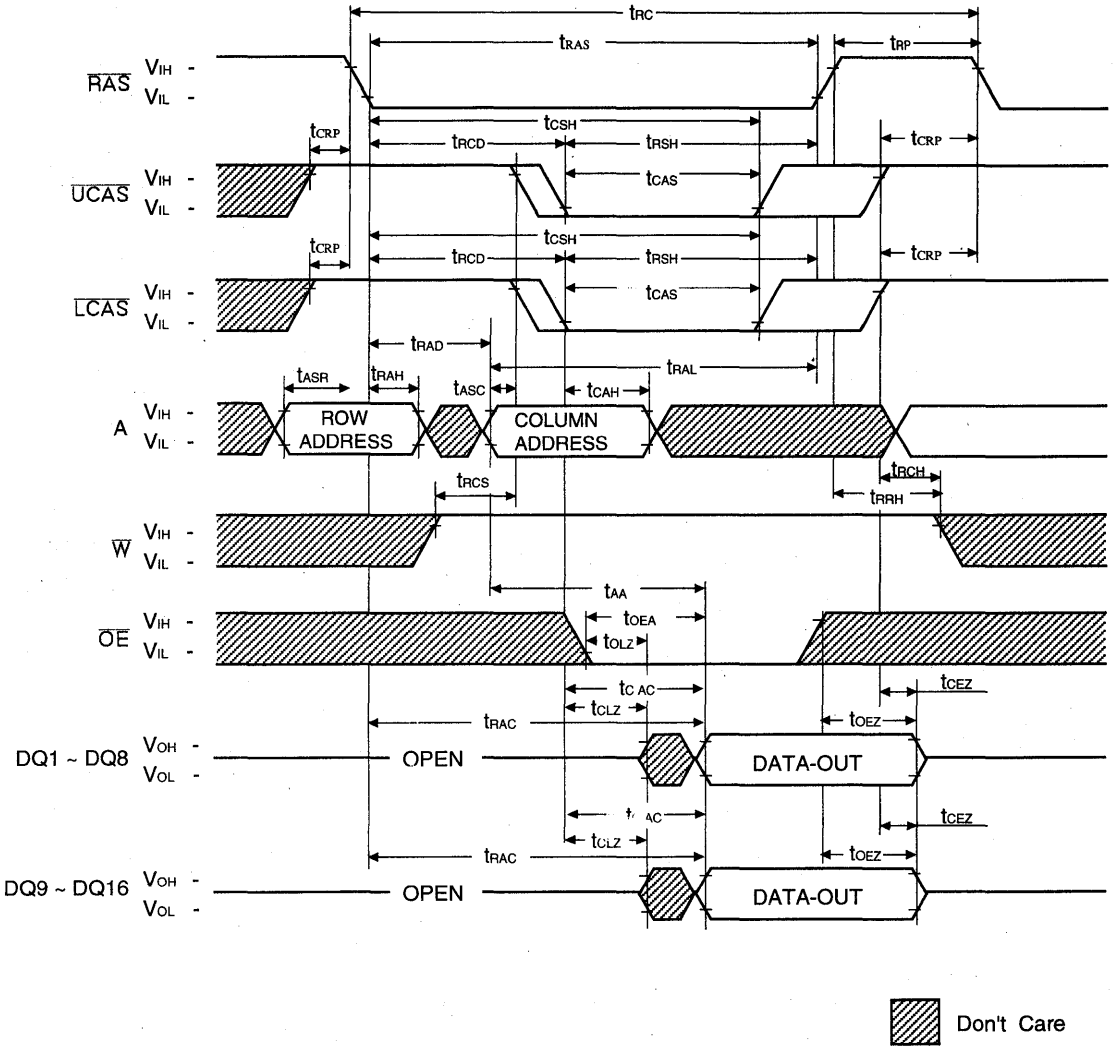
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2TTL Loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. $t_{ASC} \geq t_{CP}$ min, Assume t_T=2.0ns.
13. 1024 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (F-version)
14. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
16. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
17. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
18. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
19. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
20. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.
21. t_{DS}, t_{DH} is independetly specified for lower byte D_{in} ($_{1\sim8}$), upper byte $D_{in(9\sim16)}$

TIMING DIAGRAM

WORD READ CYCLE

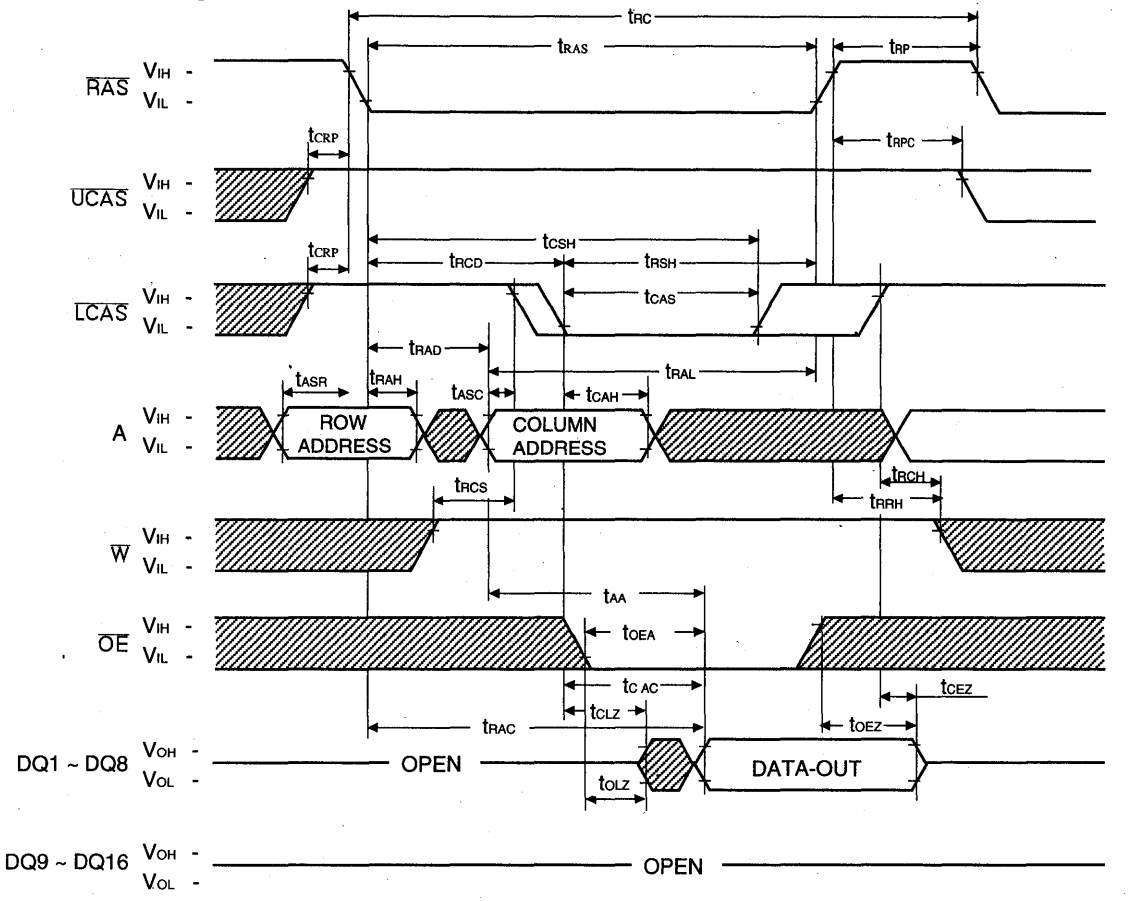
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

LOWER BYTE READ CYCLE

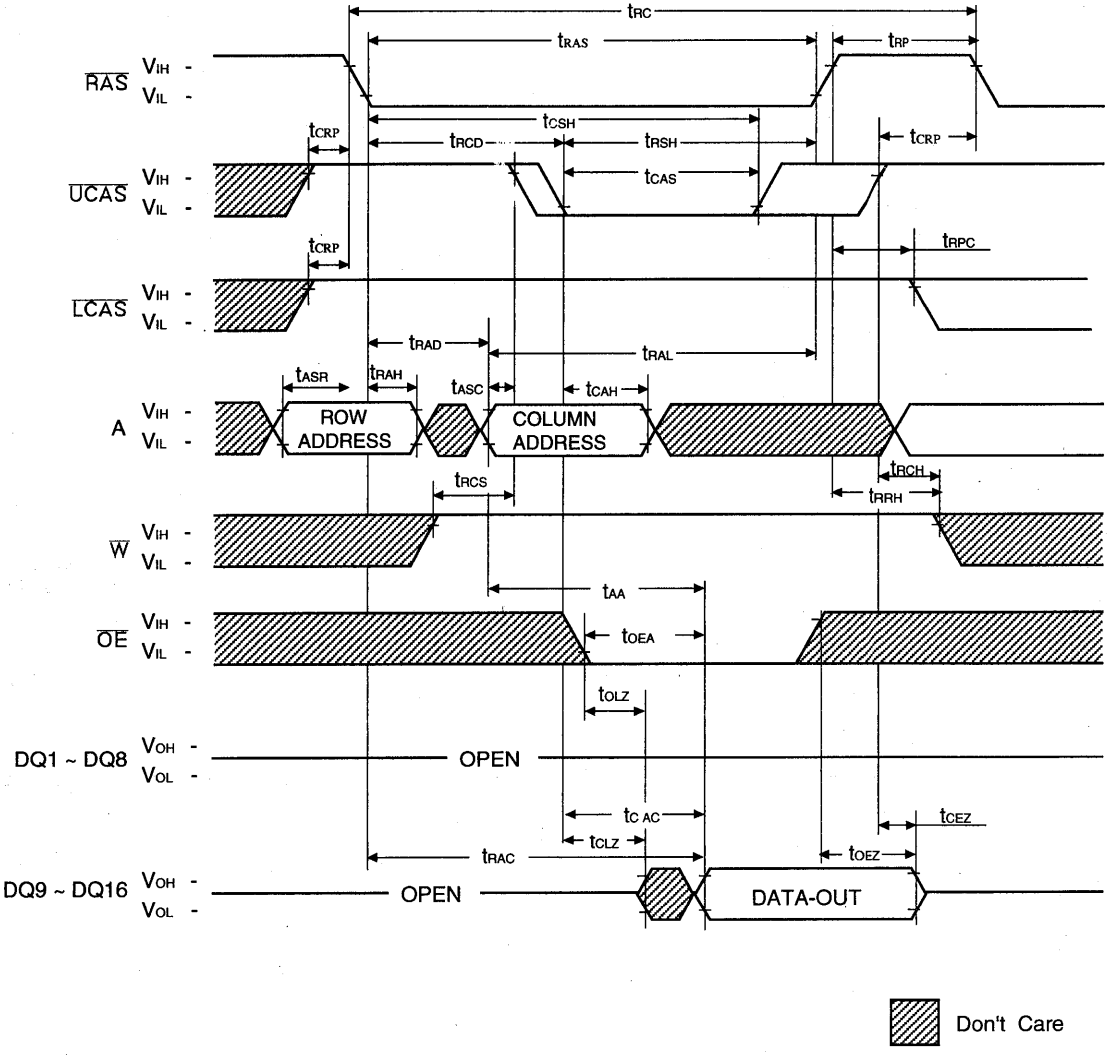
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

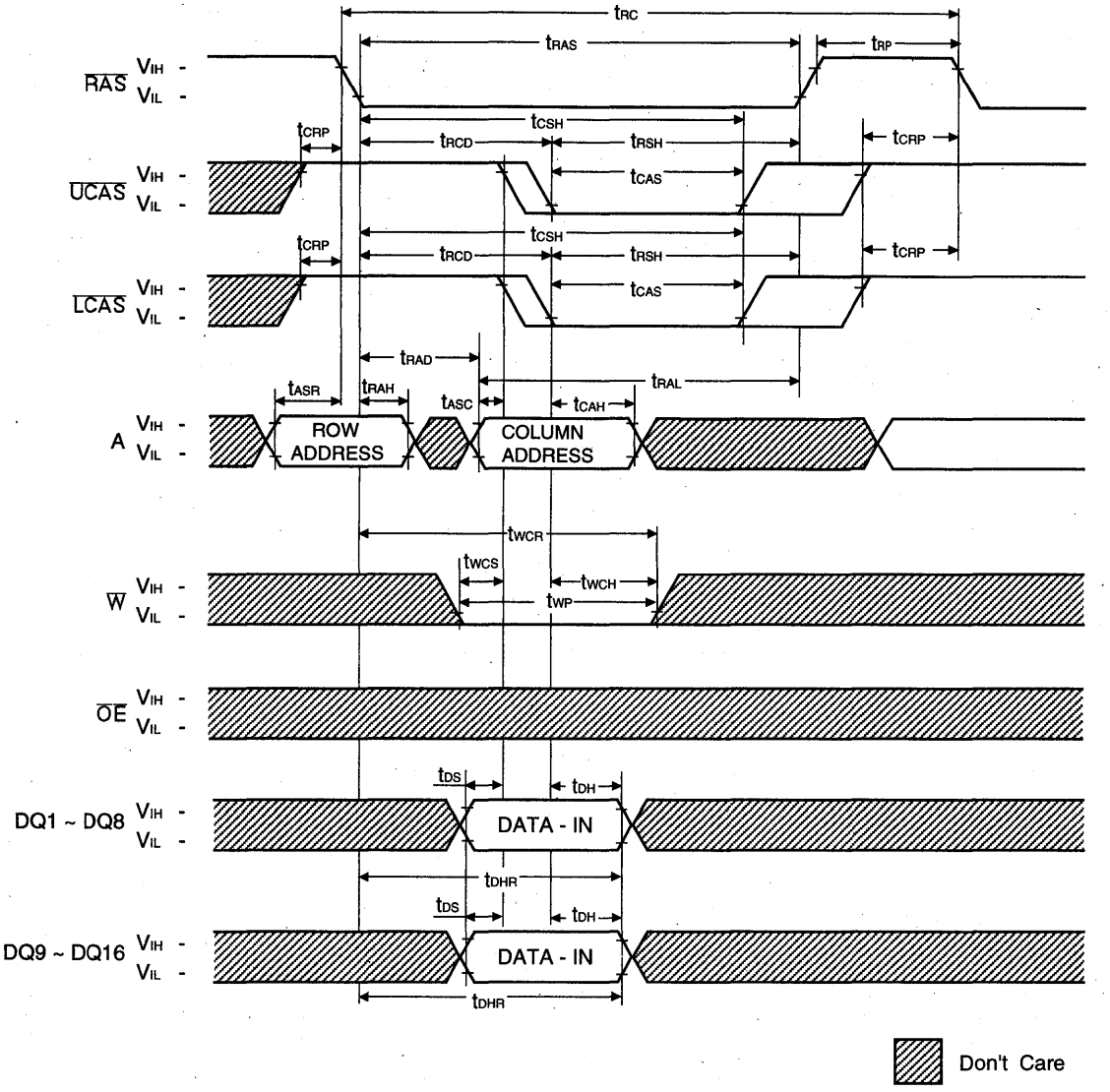
UPPER BYTE READ CYCLE

NOTE : D_{IN} = OPEN



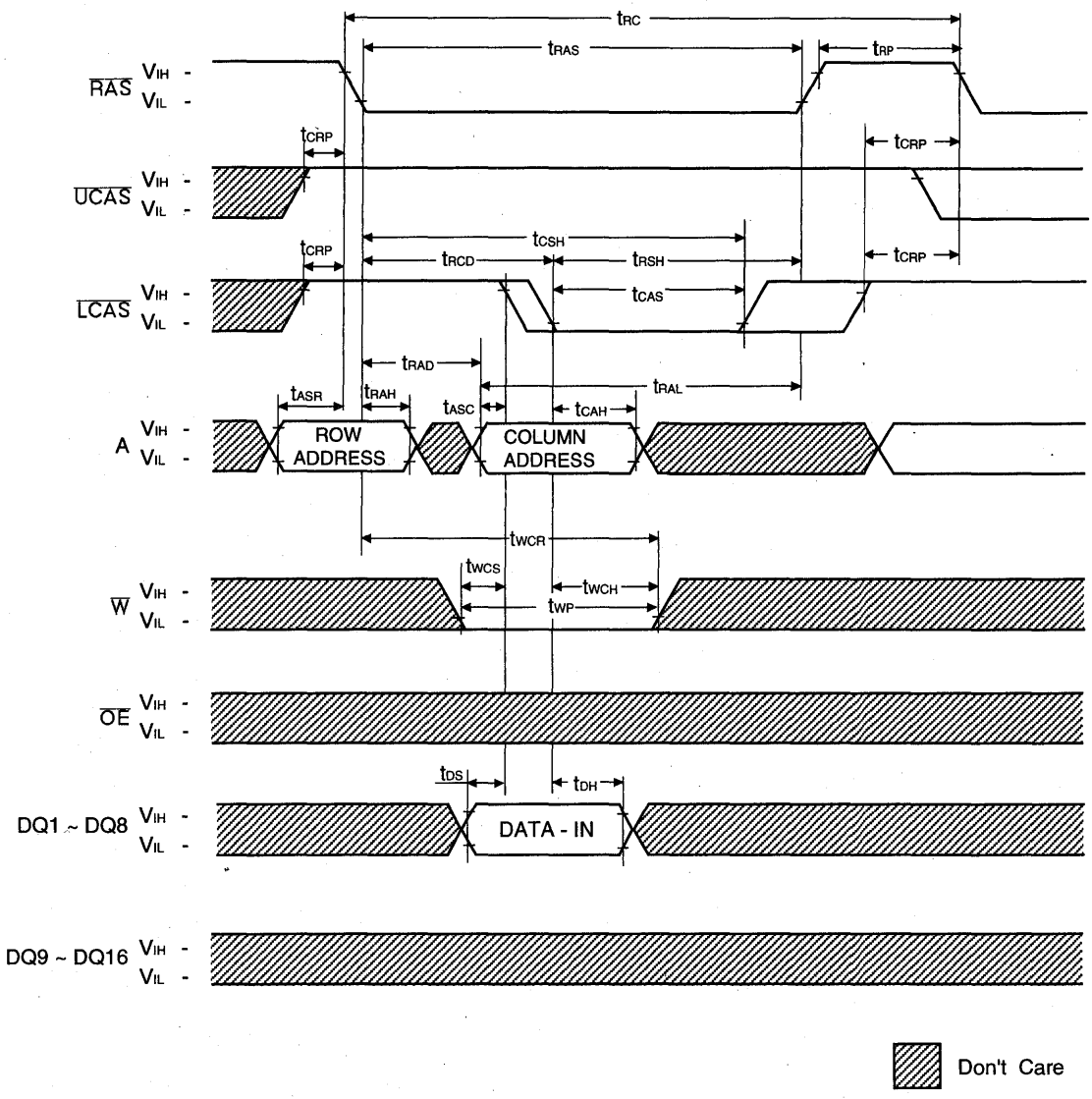
WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



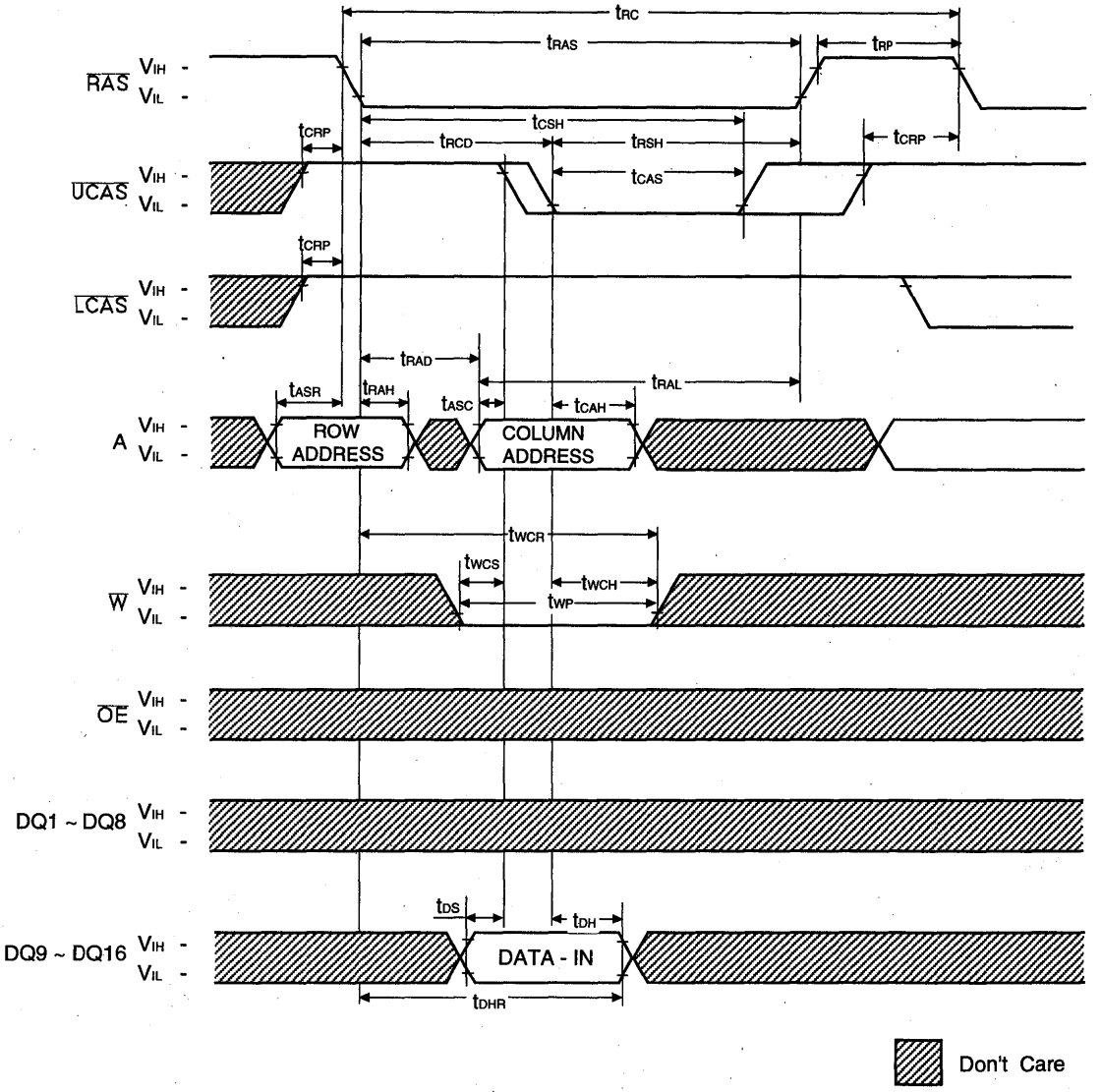
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



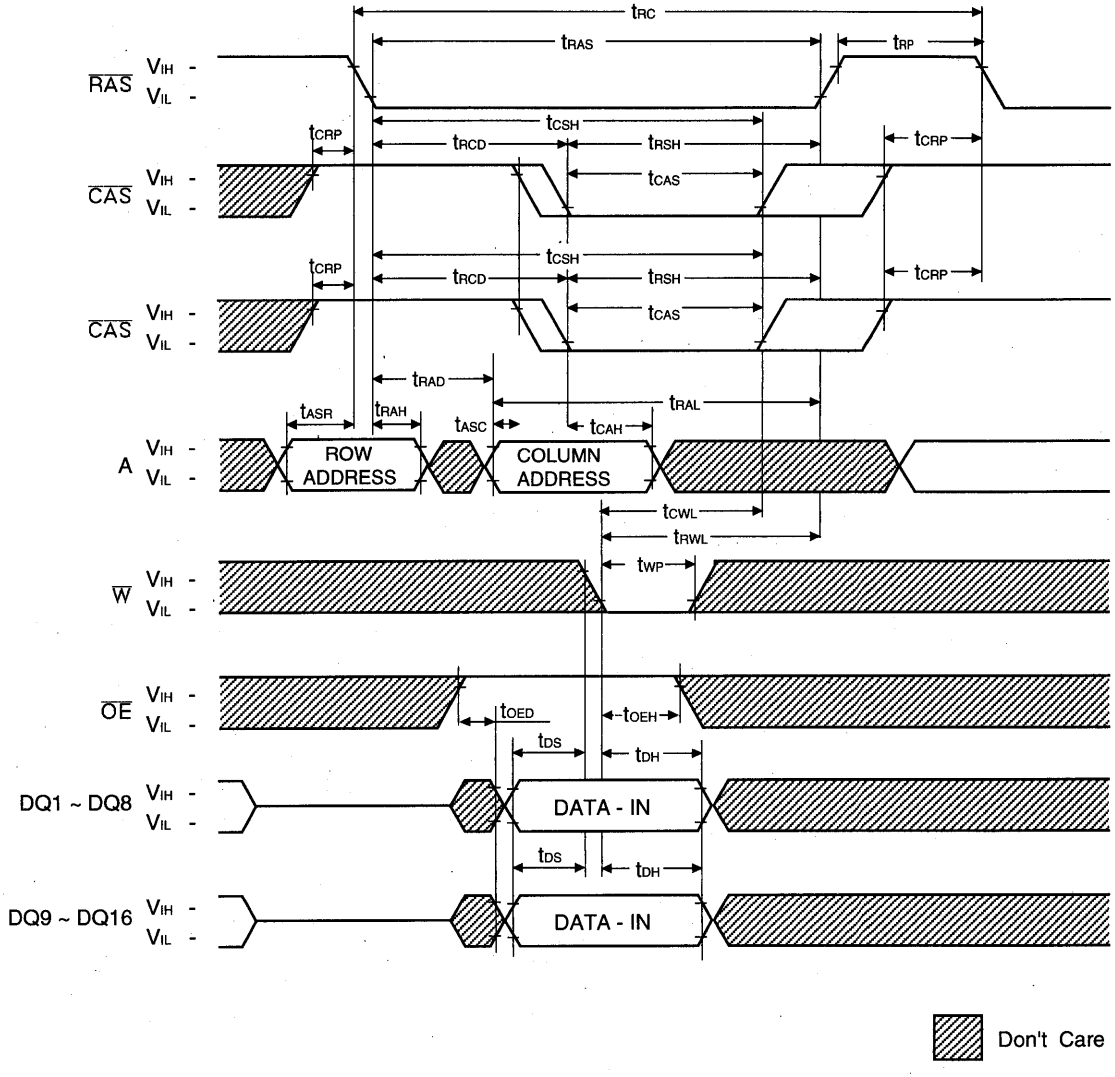
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



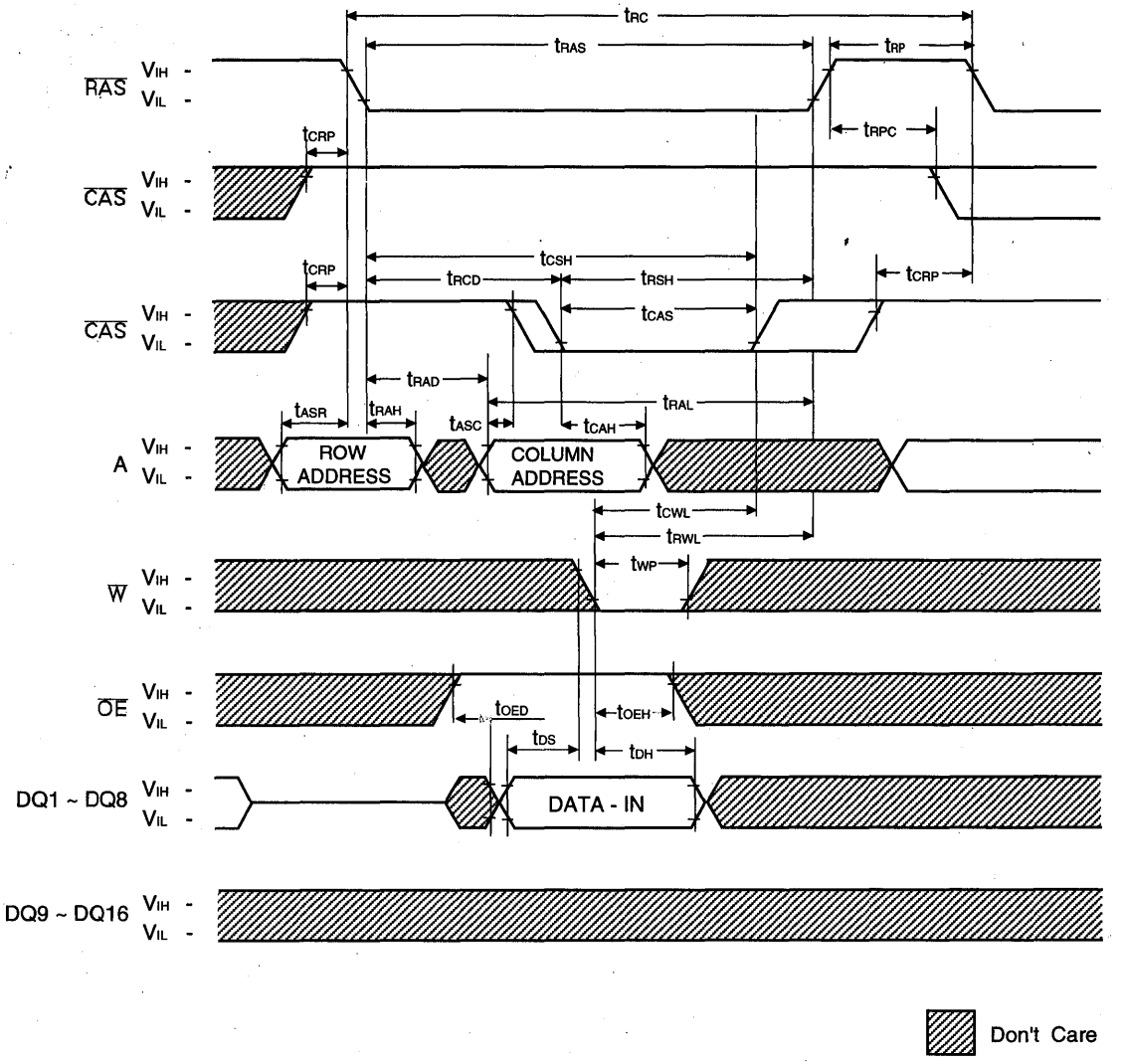
WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



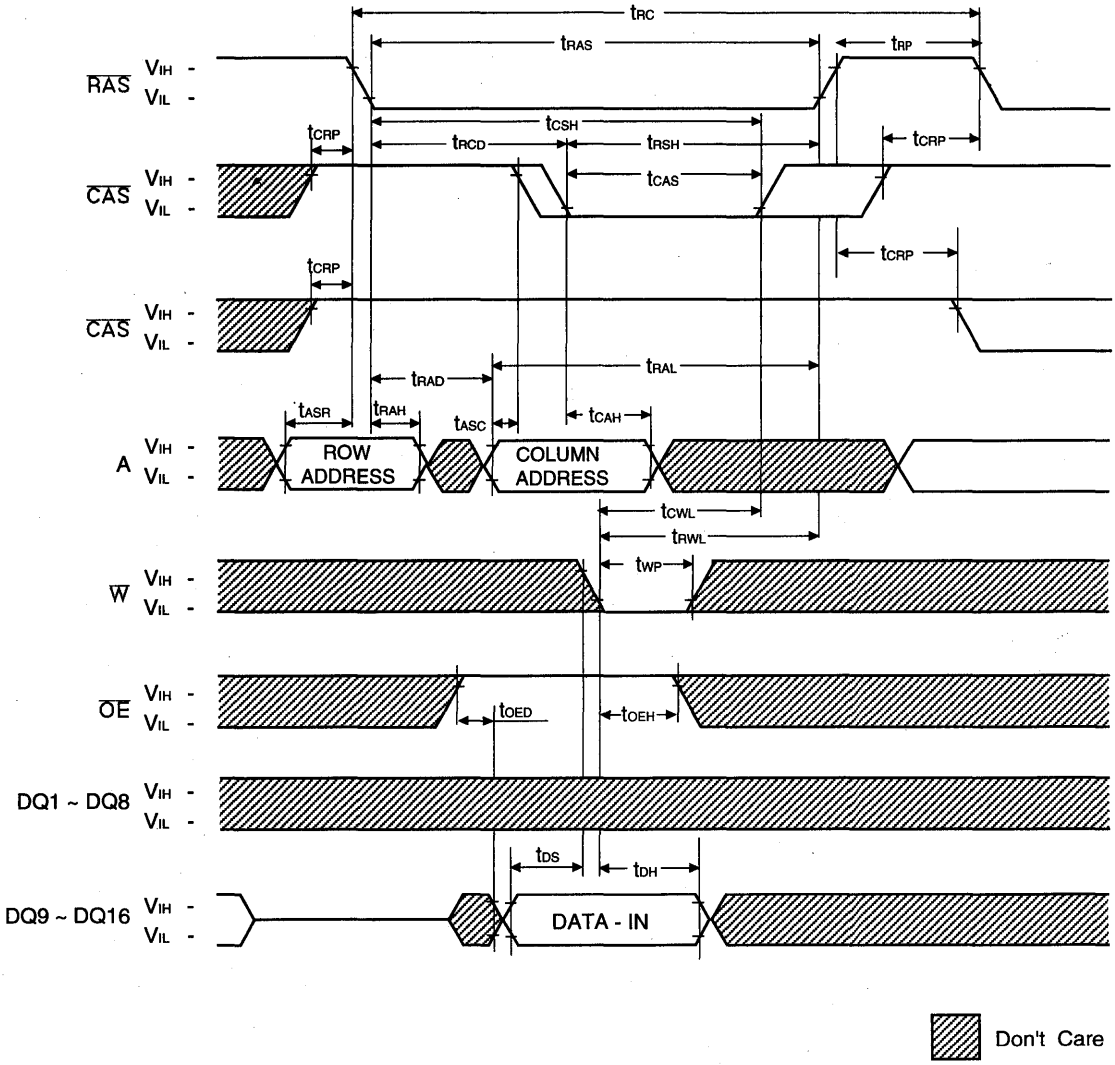
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

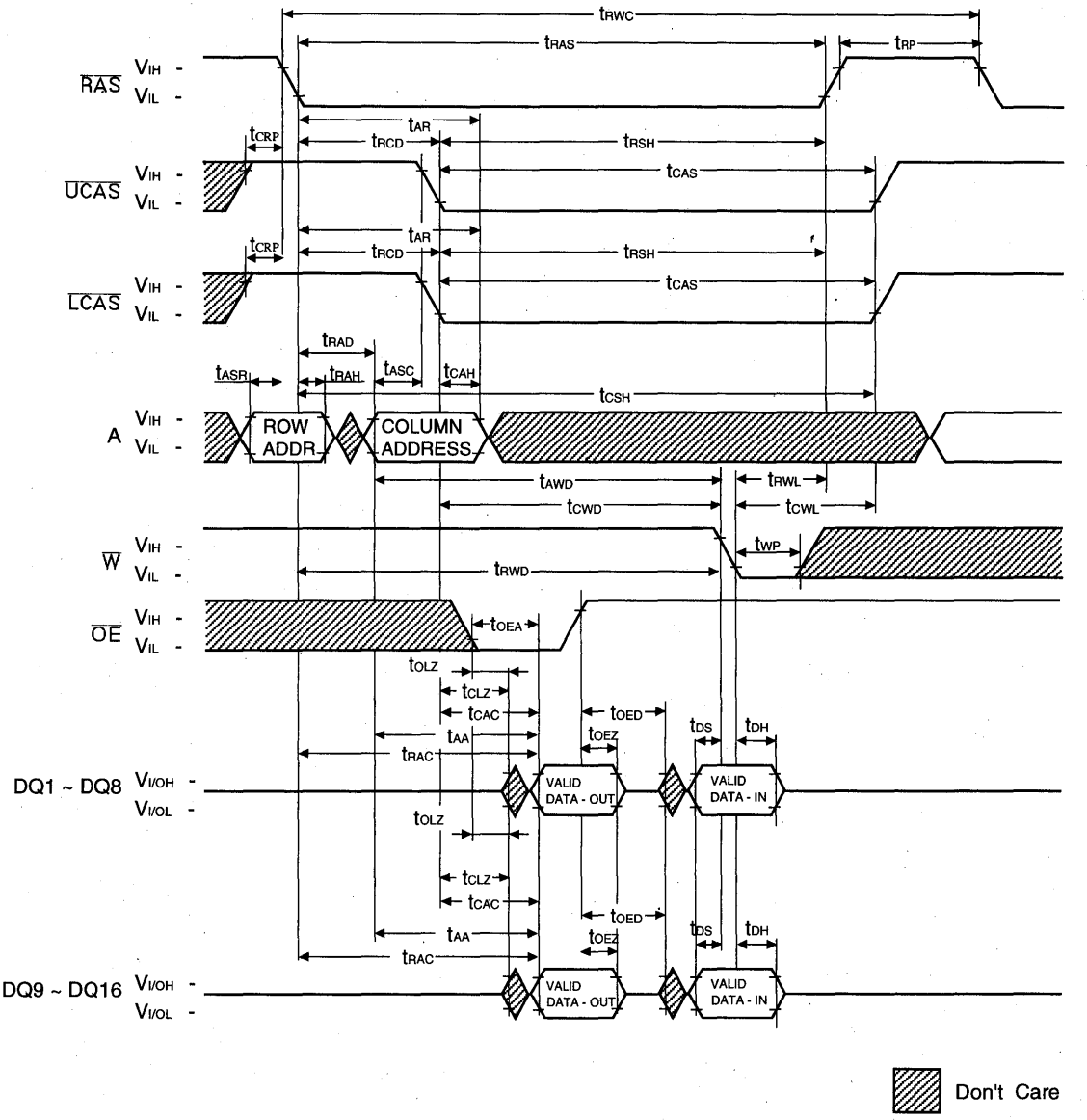


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

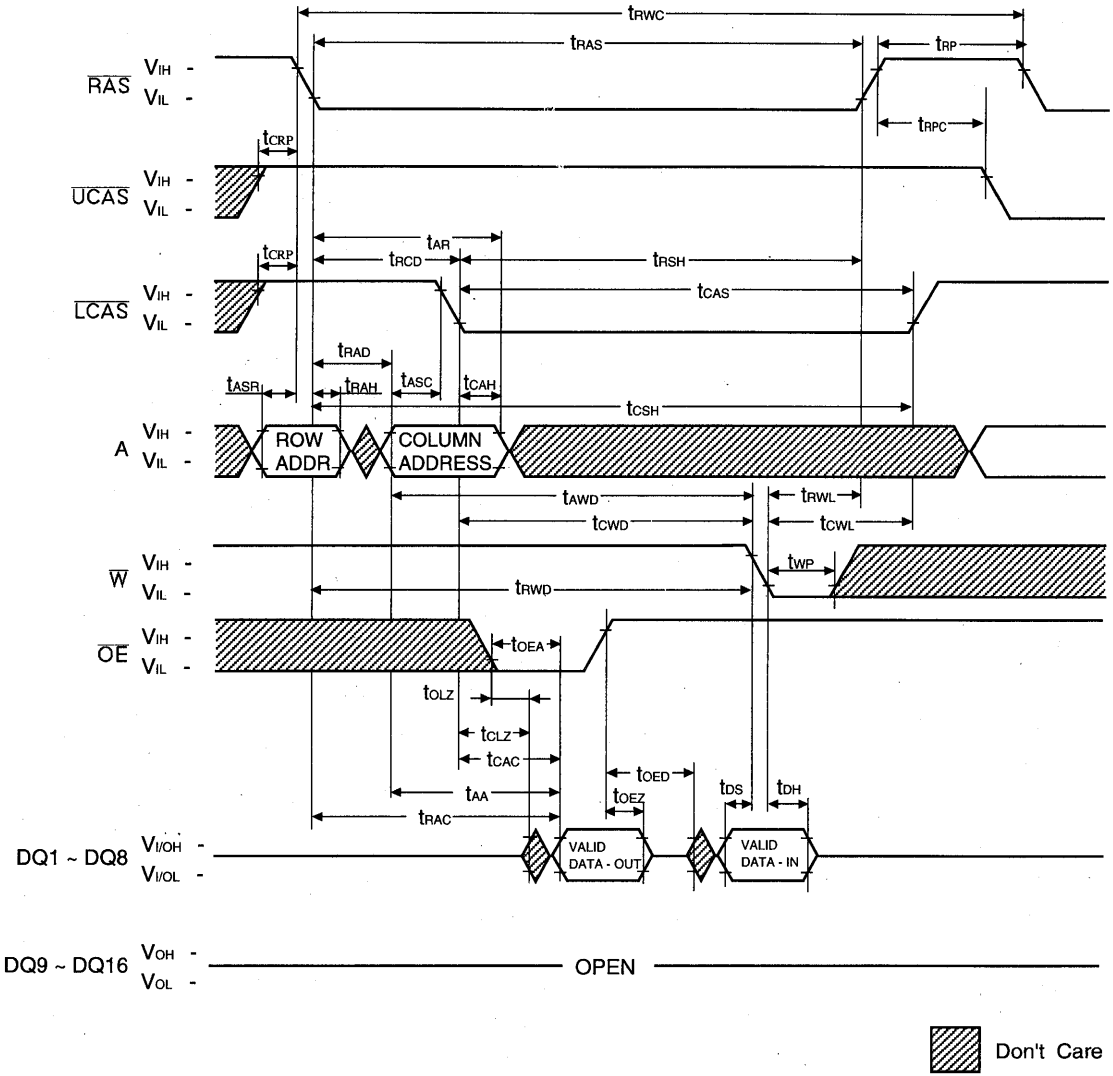
NOTE : D_{OUT} = OPEN



WORD READ - MODIFY - WRITE CYCLE

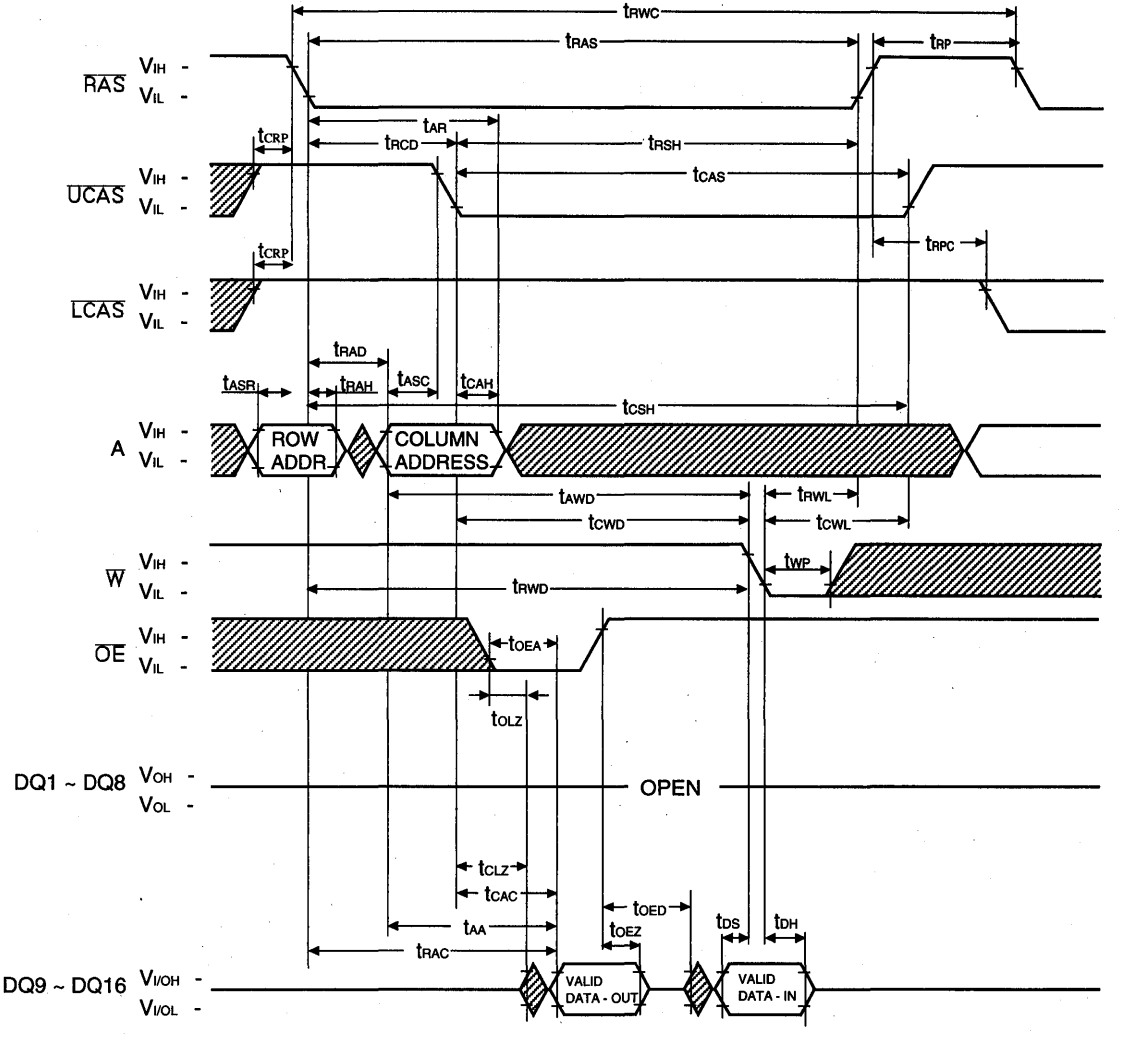


LOWER-BYTE READ - MODIFY - WRITE CYCLE

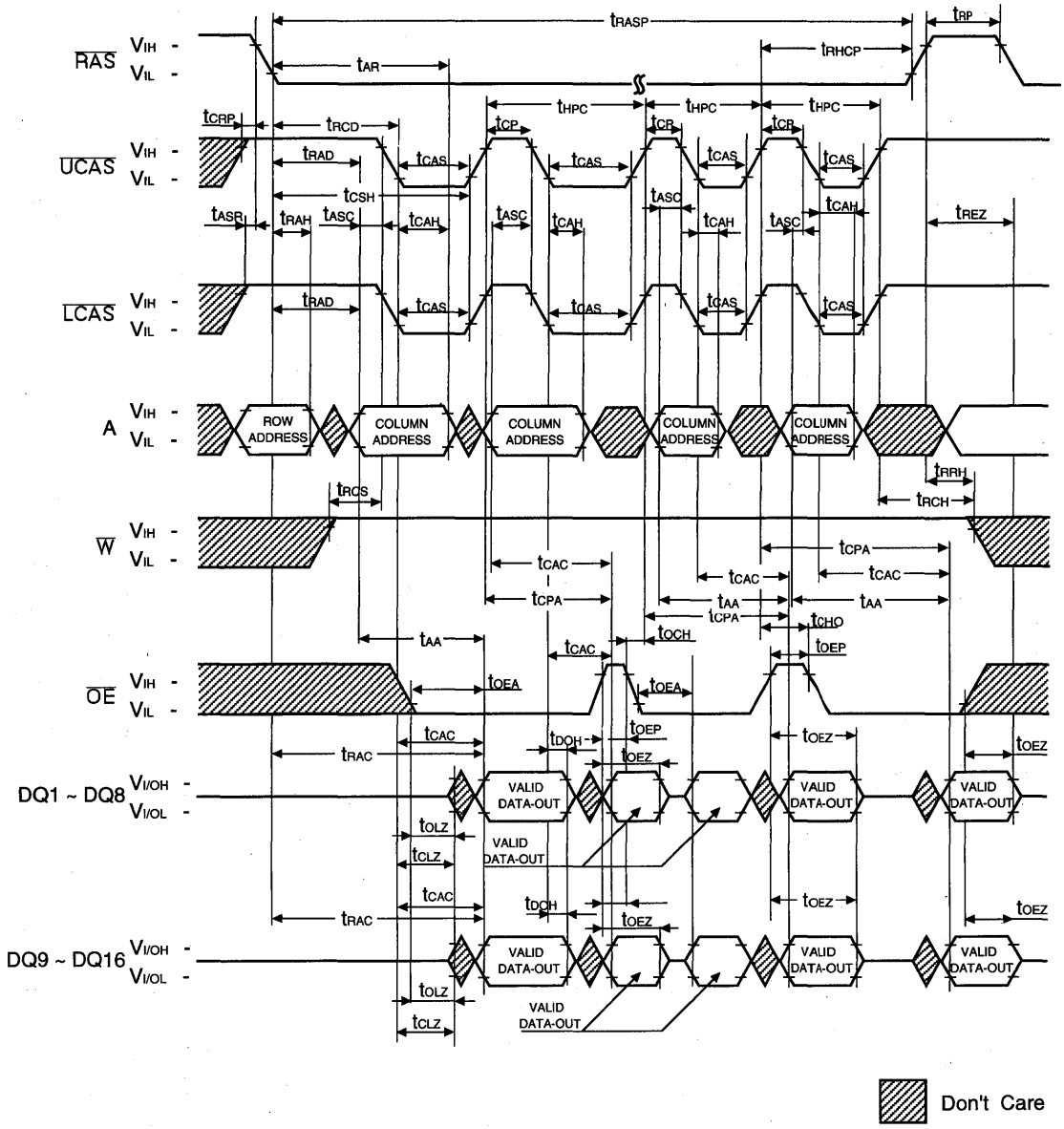


6

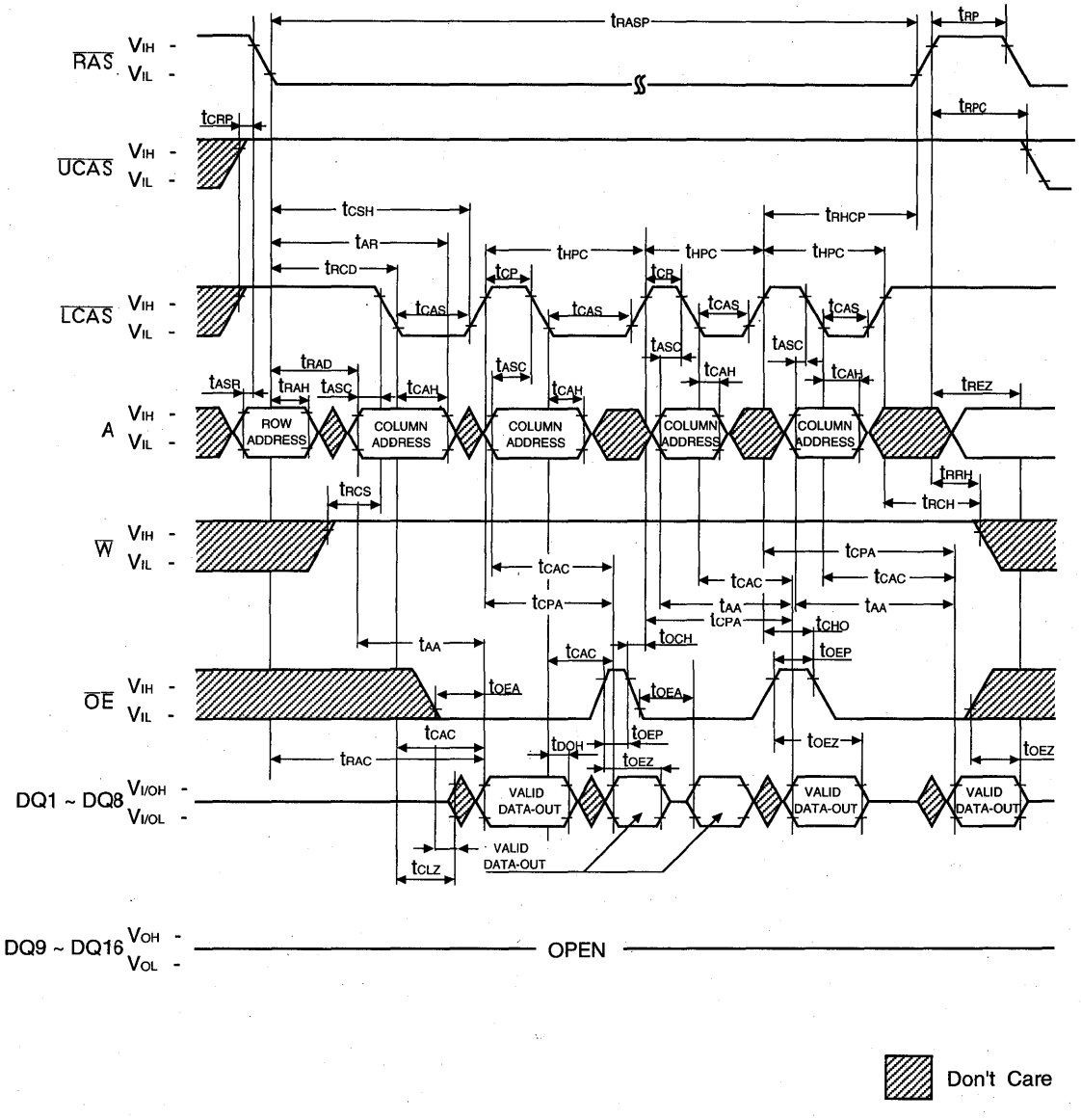
UPPER-BYTE READ - MODIFY - WRITE CYCLE



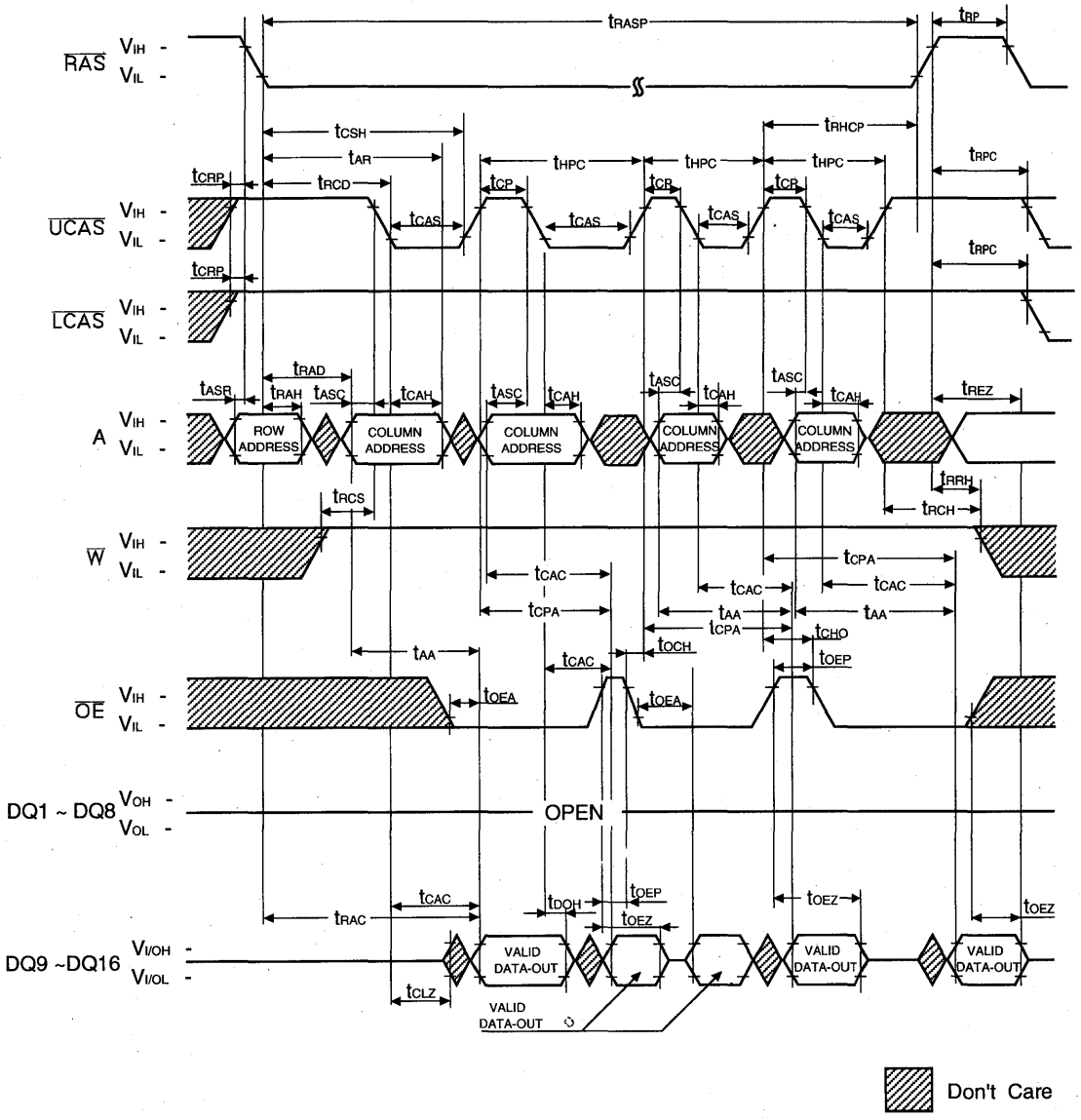
HYPER PAGE MODE WORD READ CYCLE



HYPER PAGE MODE LOWER BYTE READ CYCLE

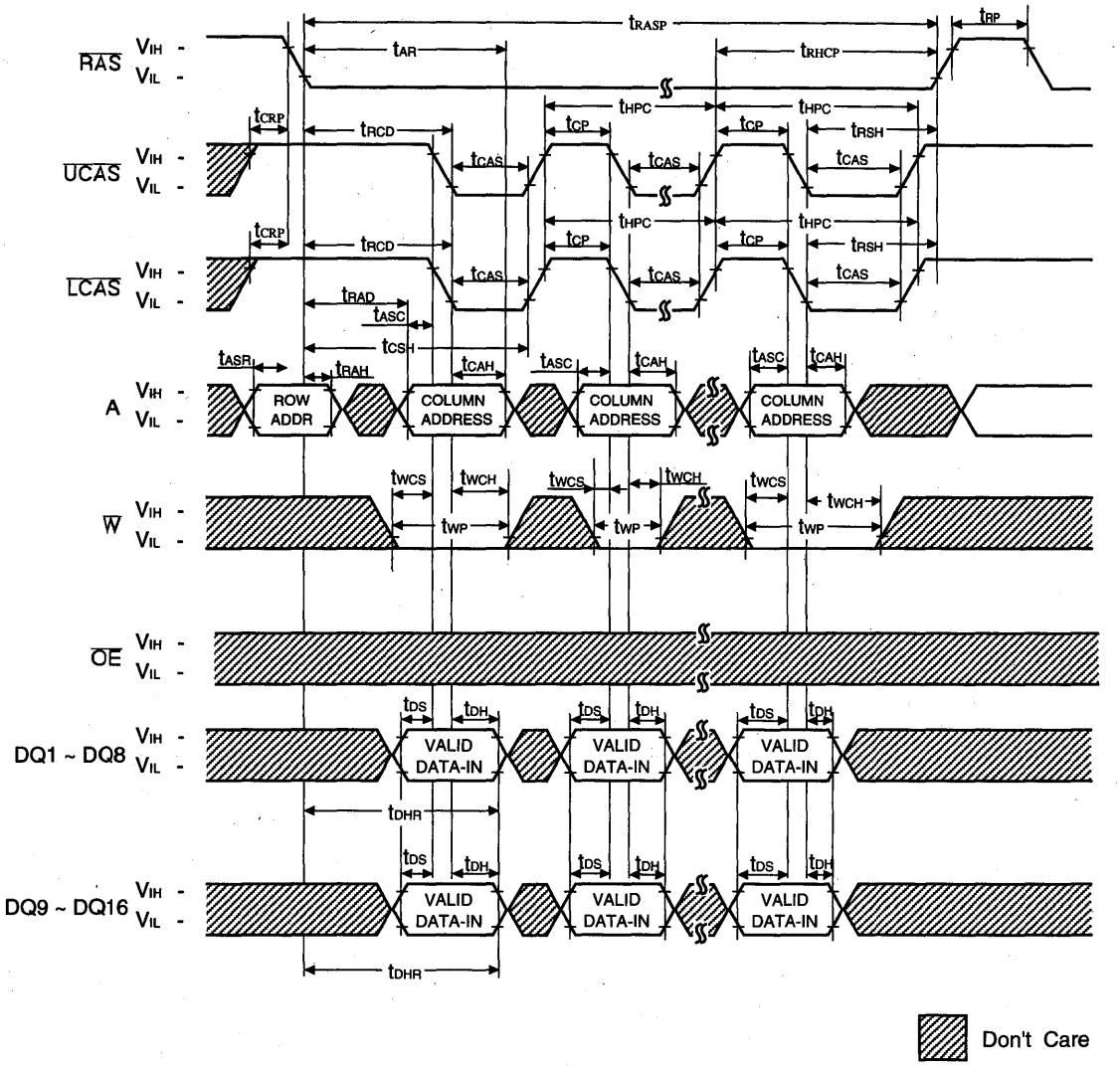


HYPER PAGE MODE UPPER BYTE READ CYCLE



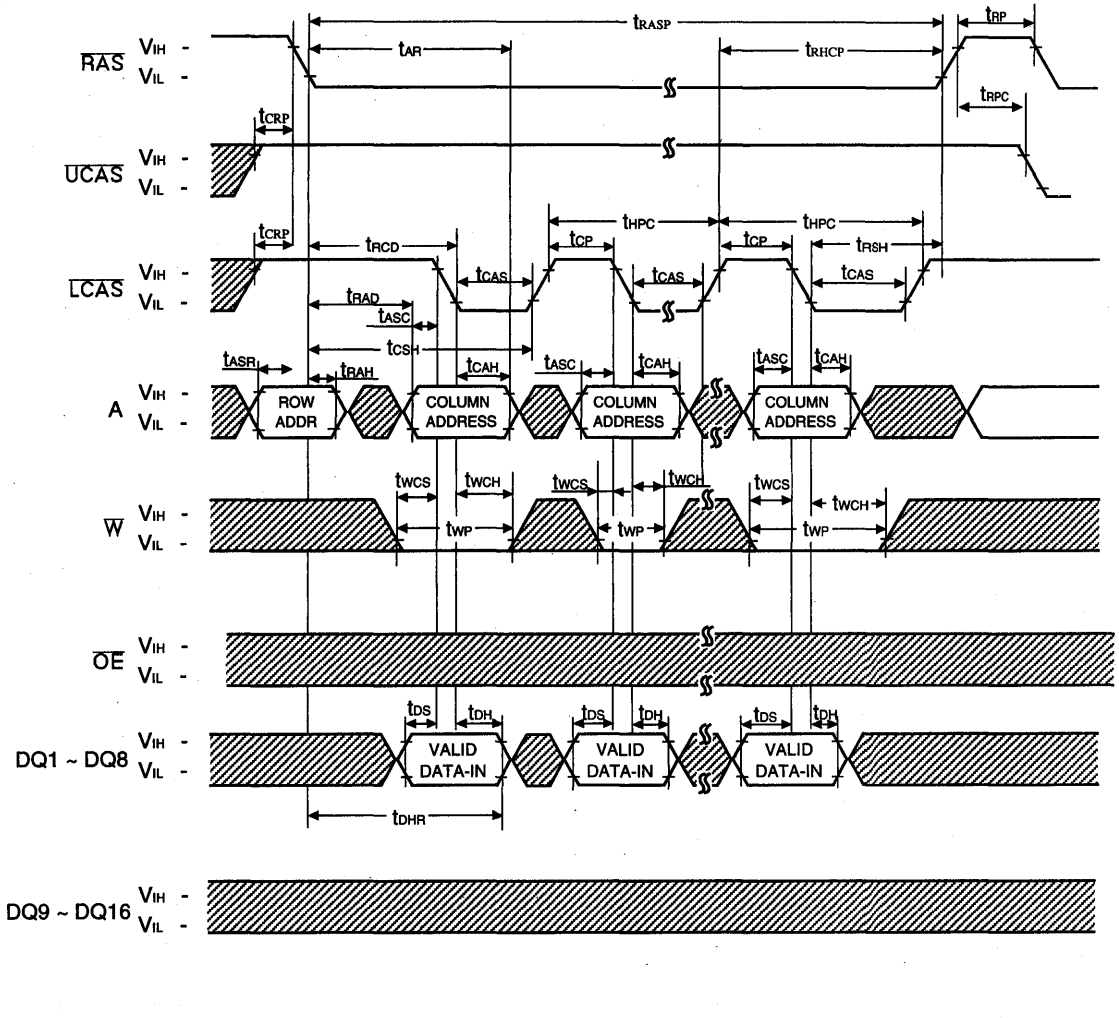
HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



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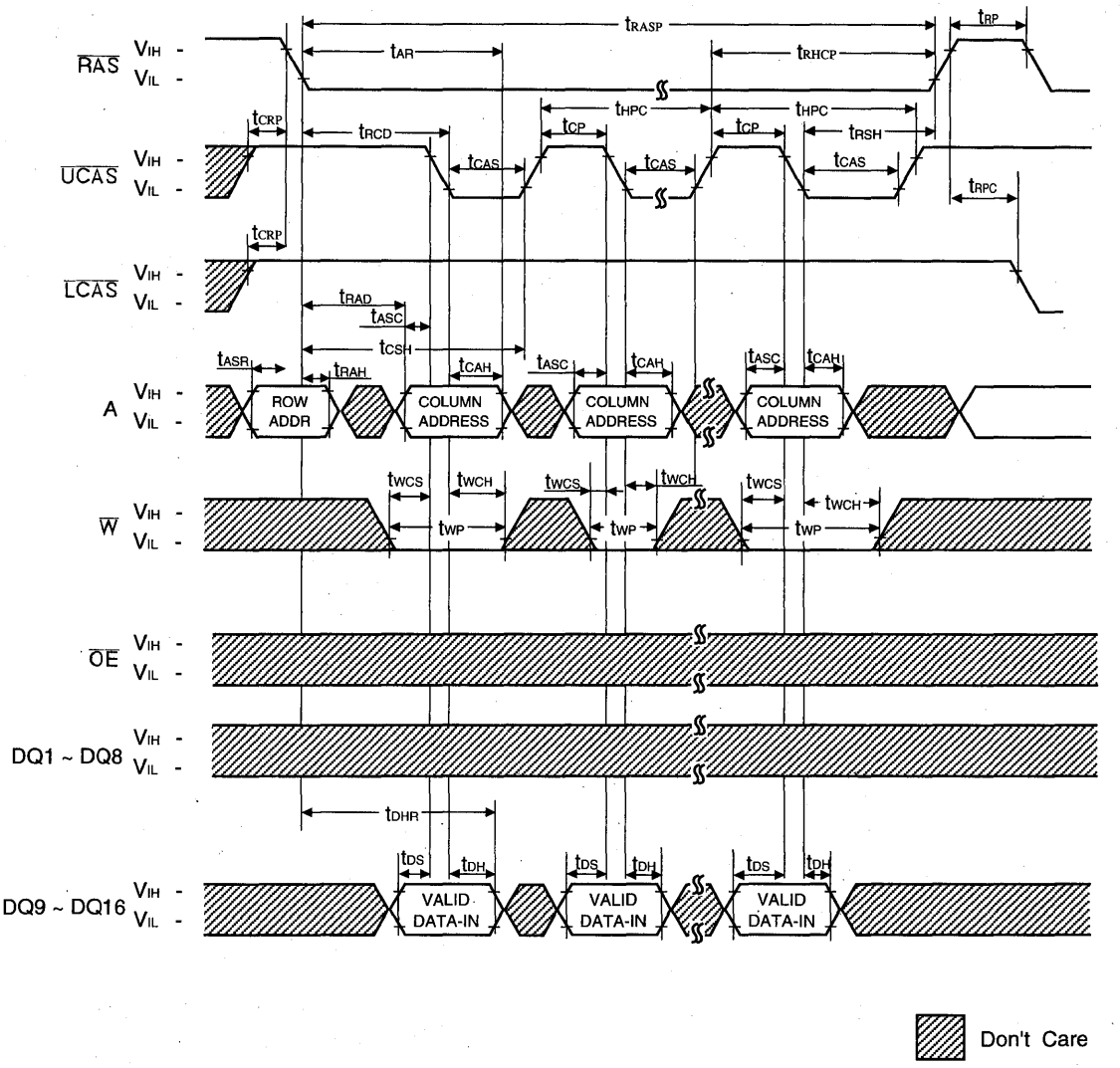
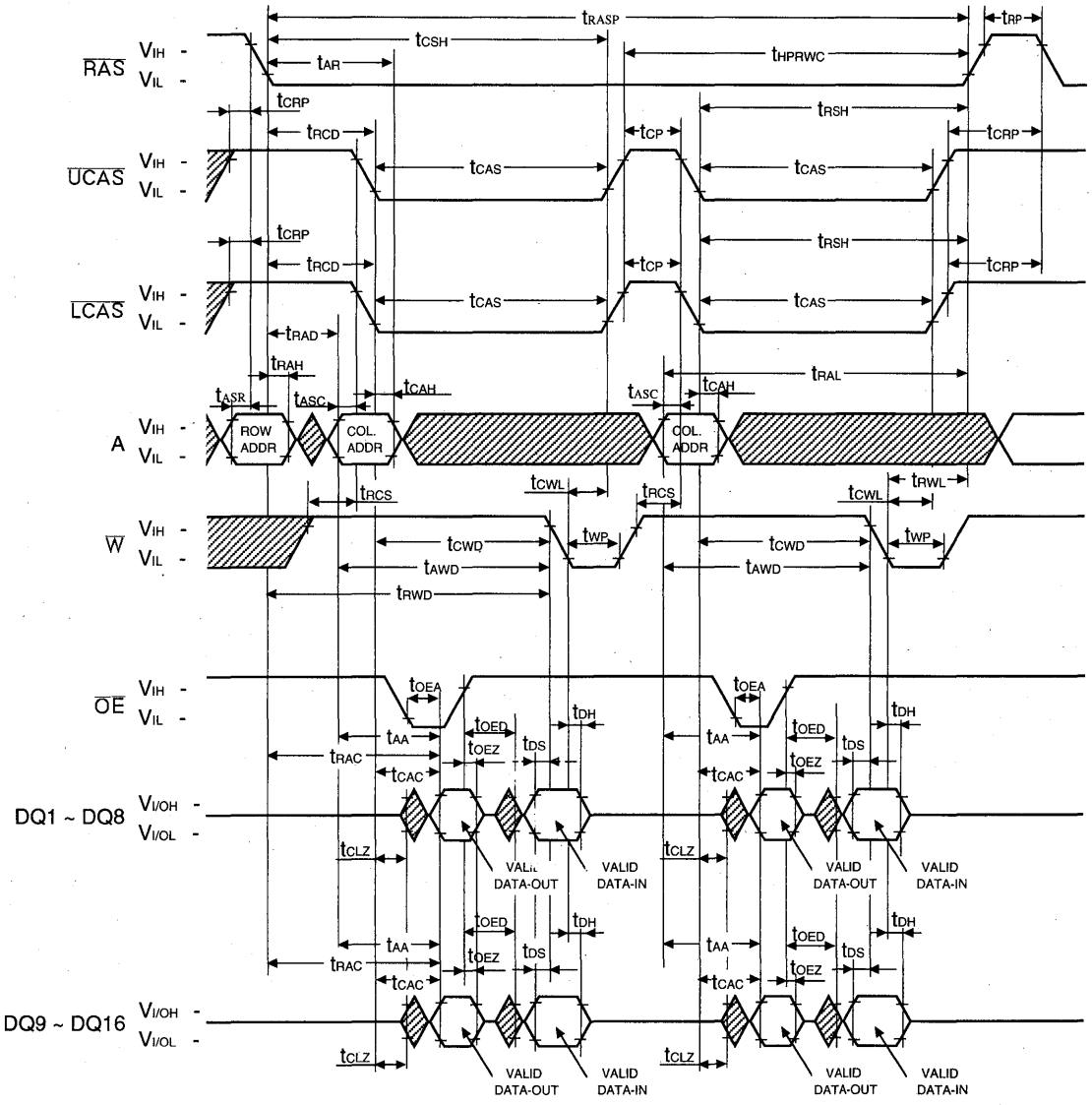
HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

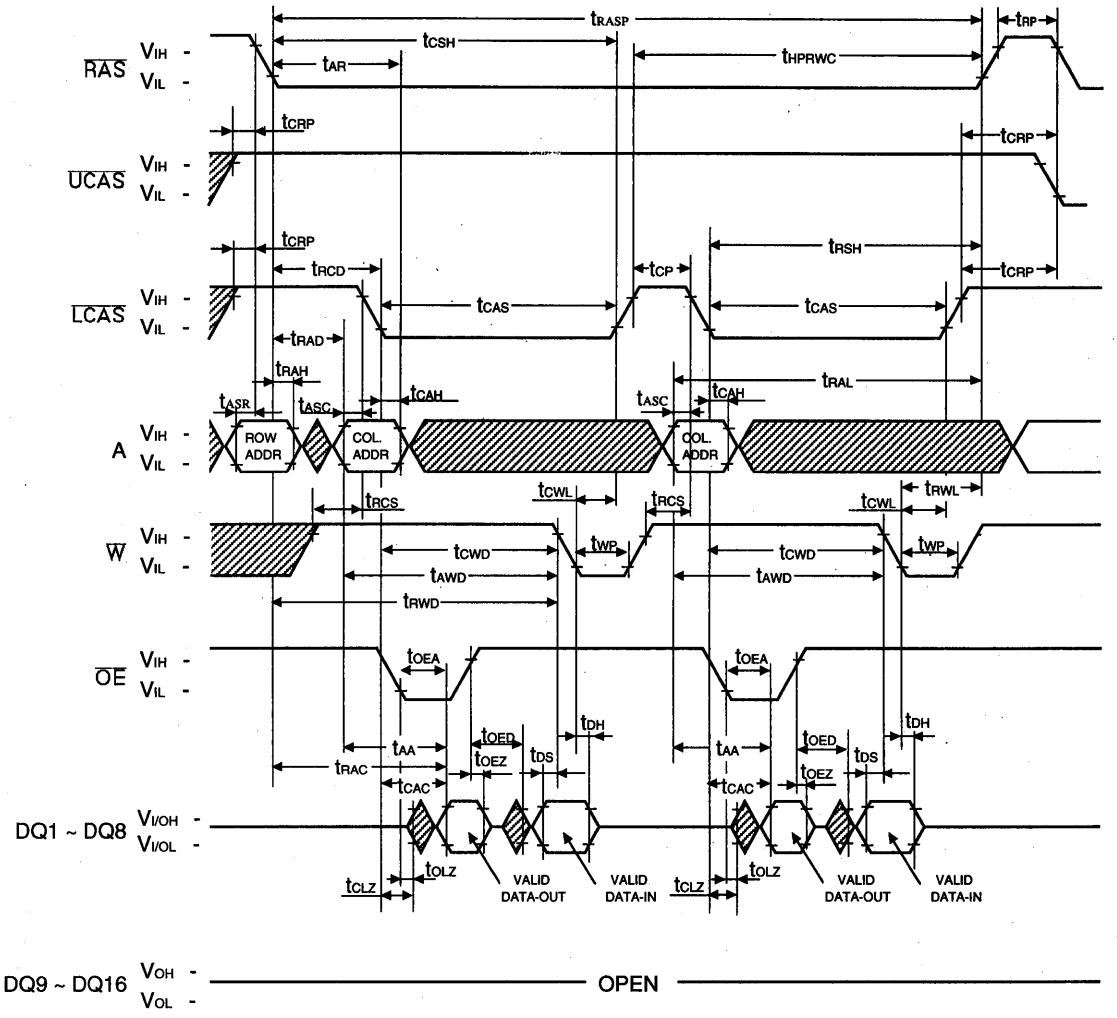
NOTE : D_{OUT} = Open



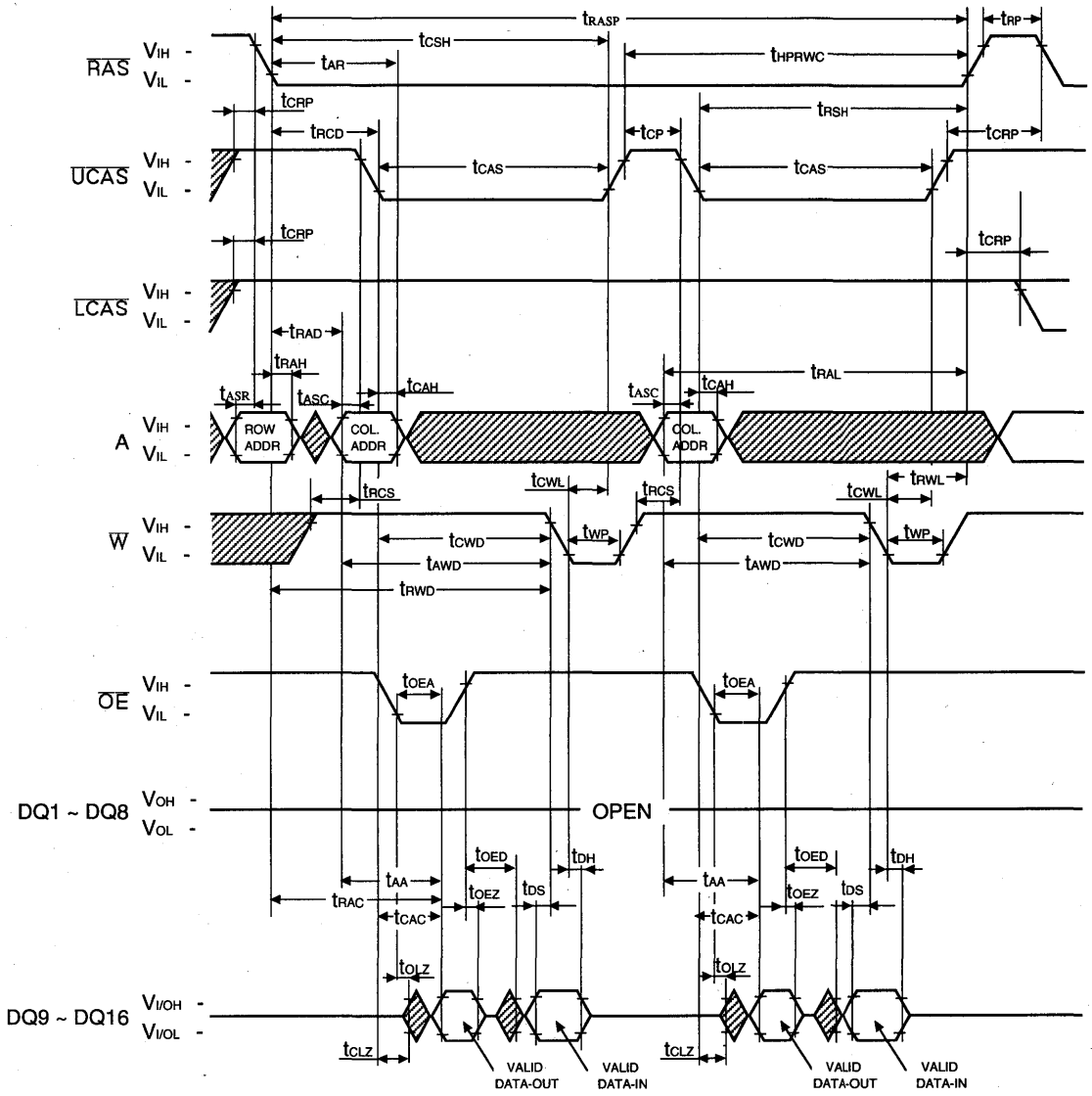
HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE



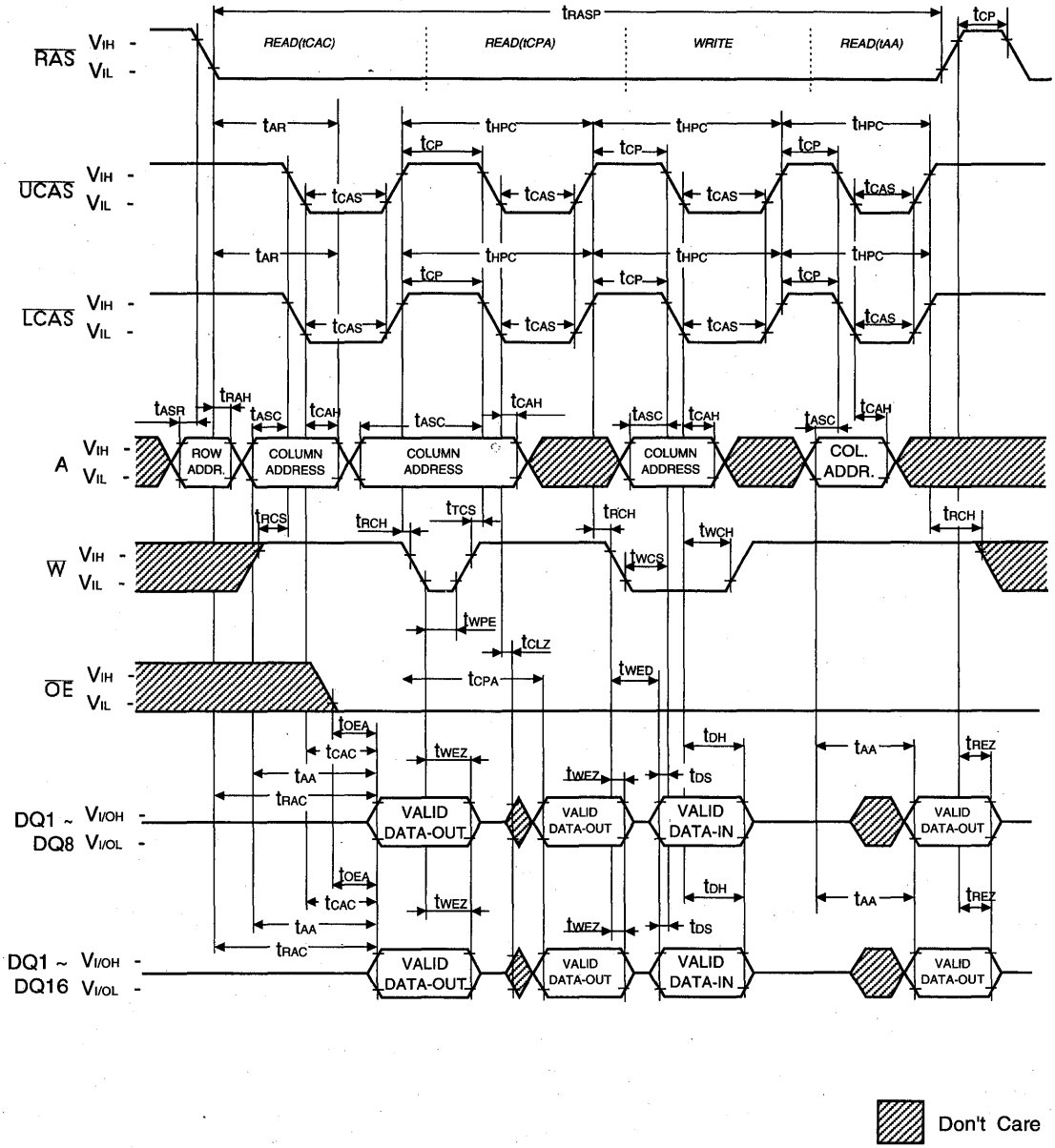
HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE

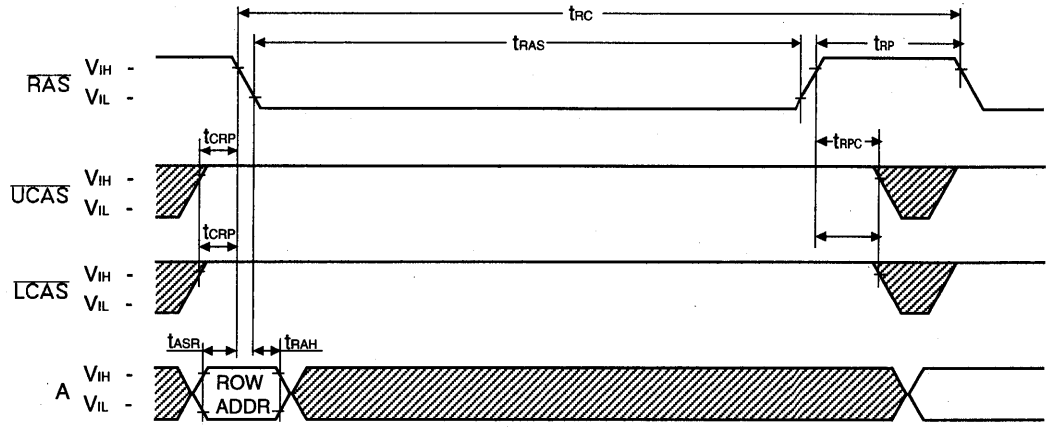


HYPER PAGE READ AND WRITE MIXED CYCLE



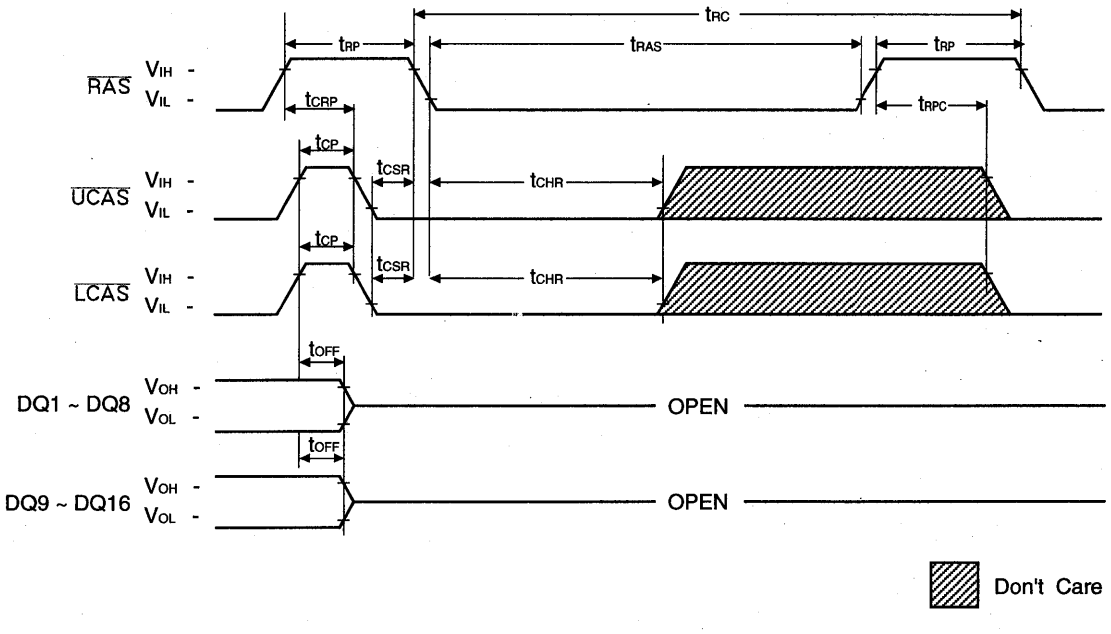
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



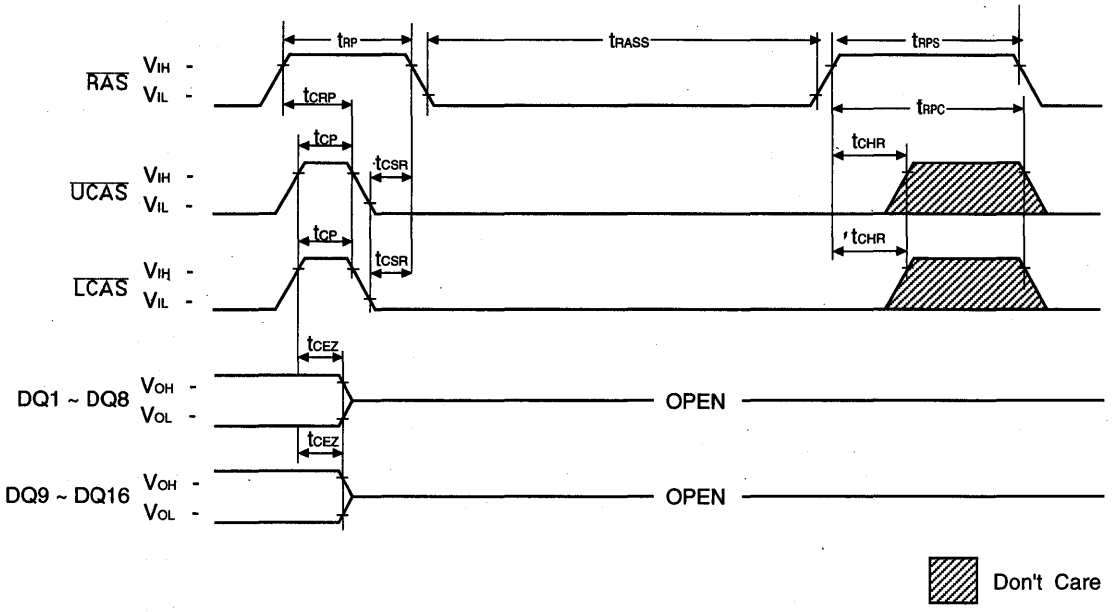
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

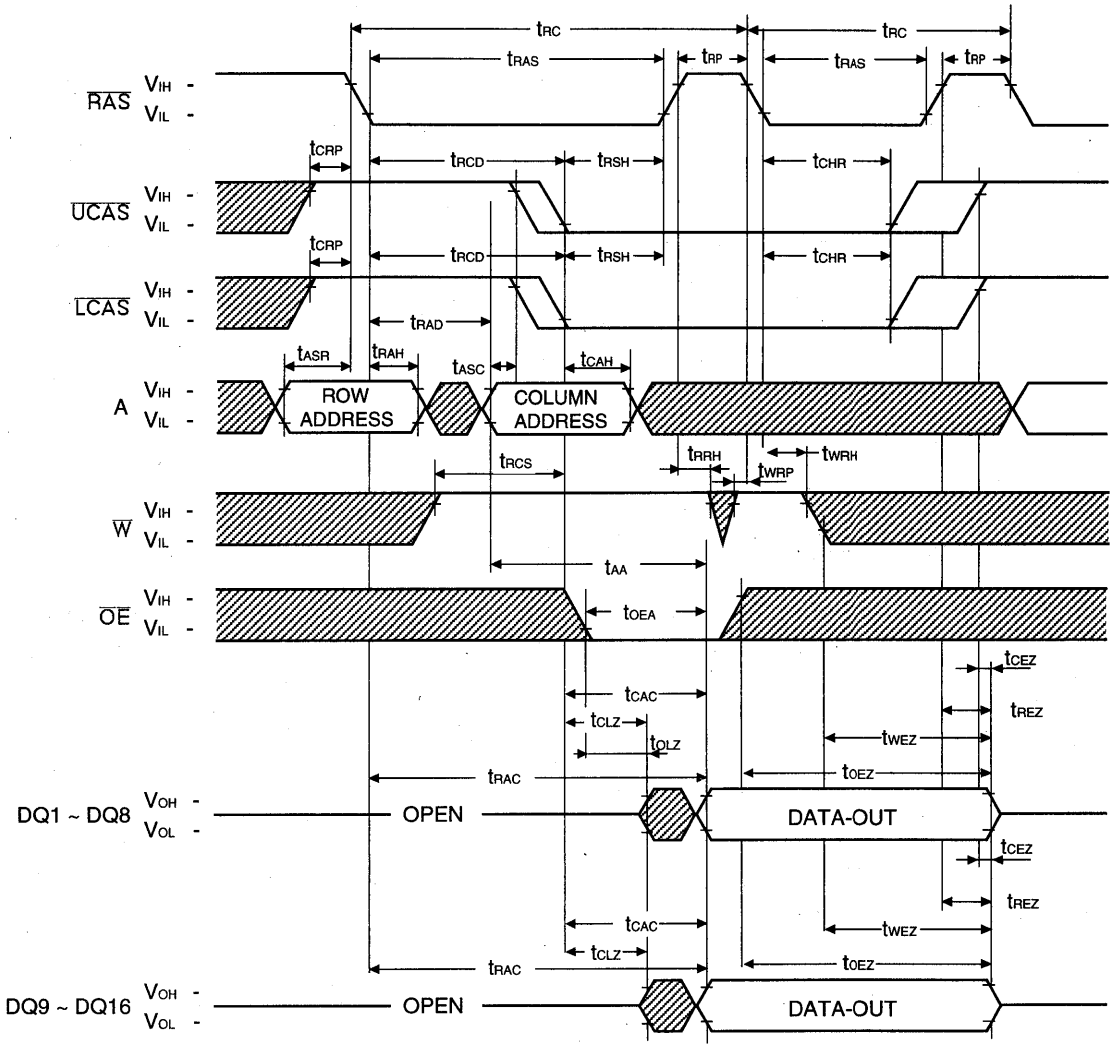


$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE(LL-version)

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



HIDDEN REFRESH CYCLE (READ)

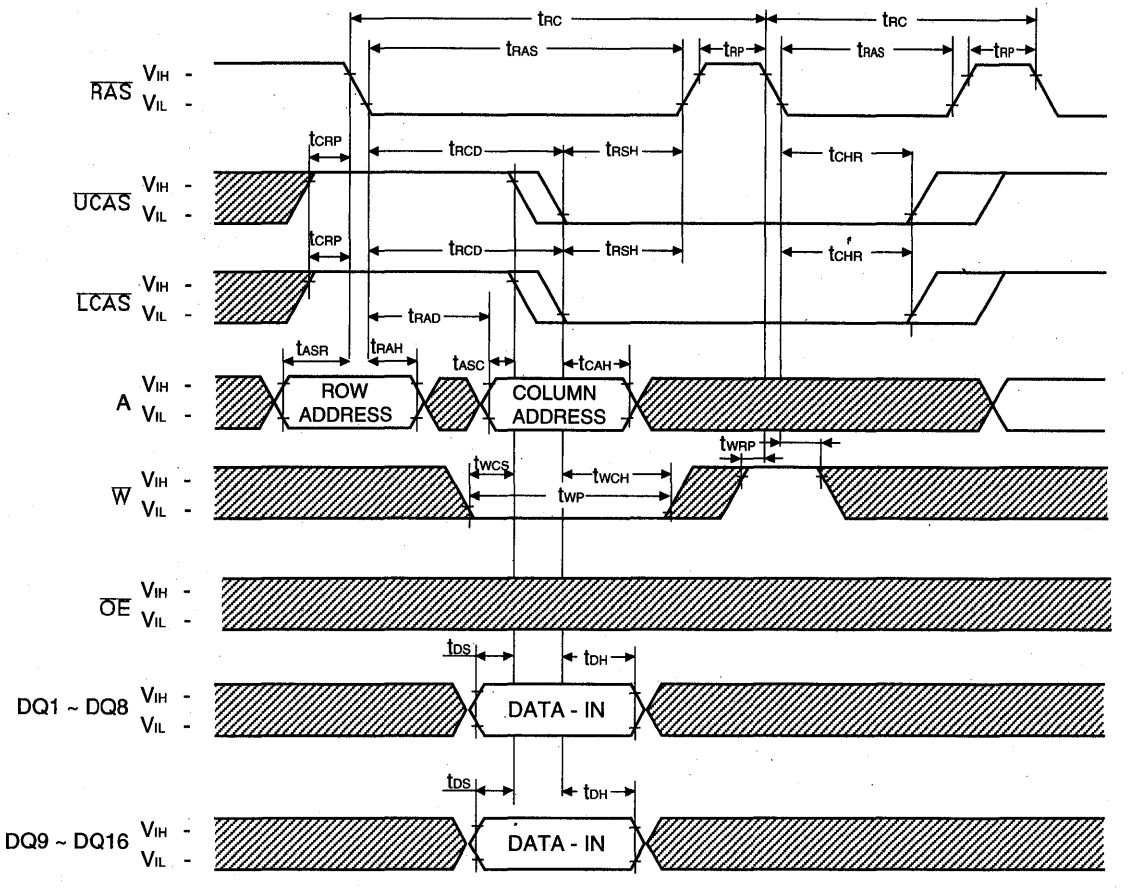


Don't Care

SAMSUNG ELECTRONICS

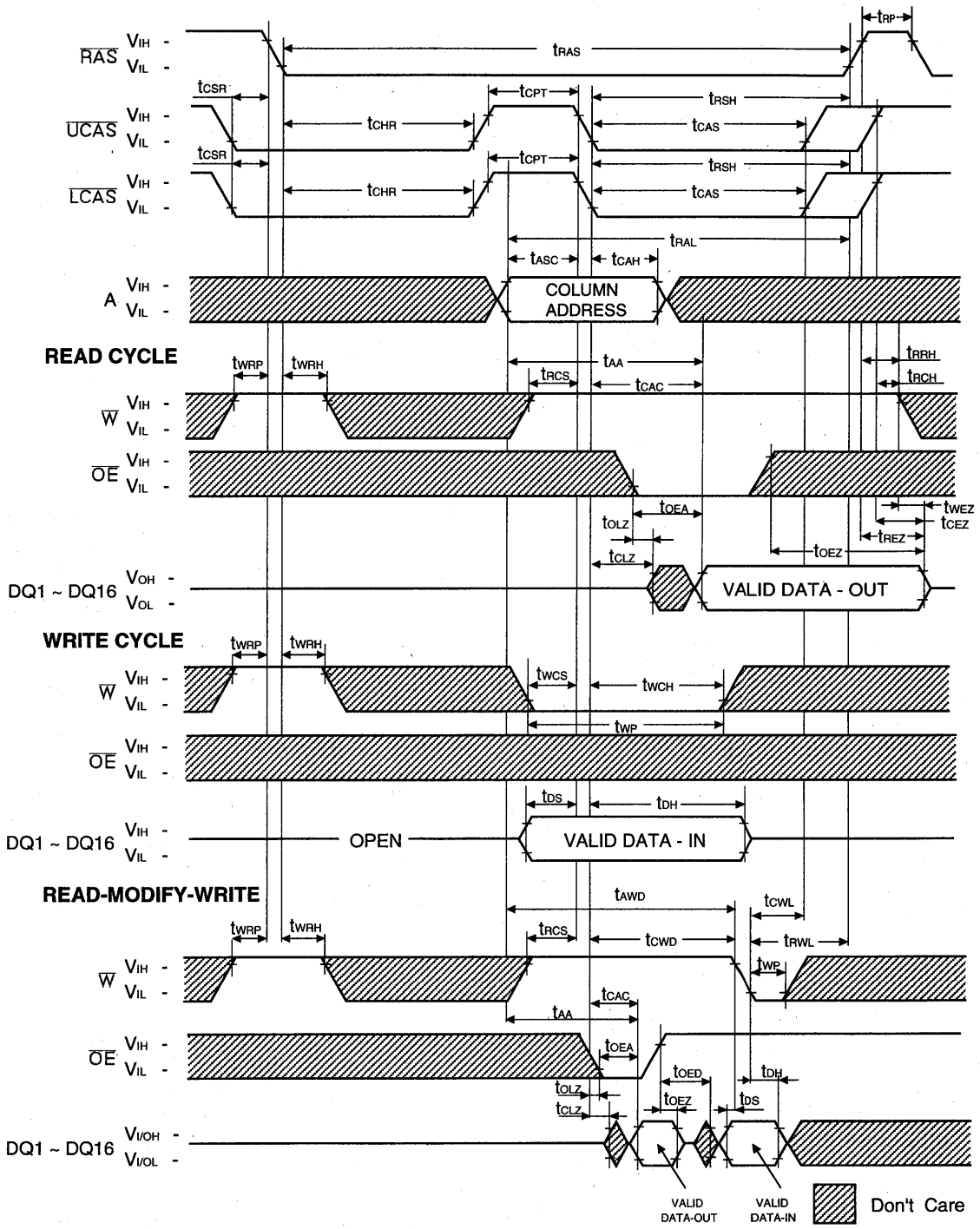
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



Don't Care

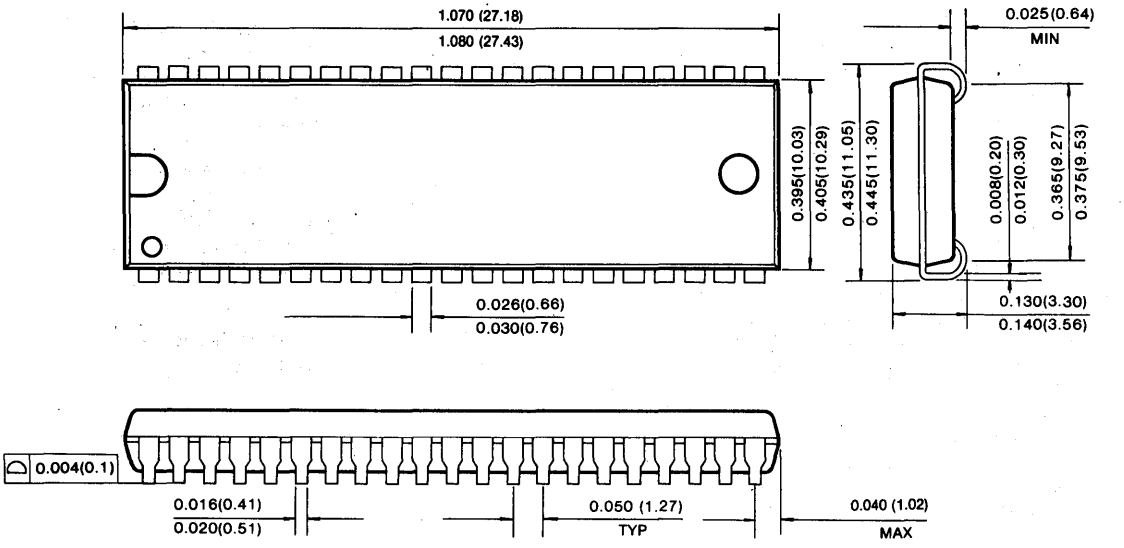
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



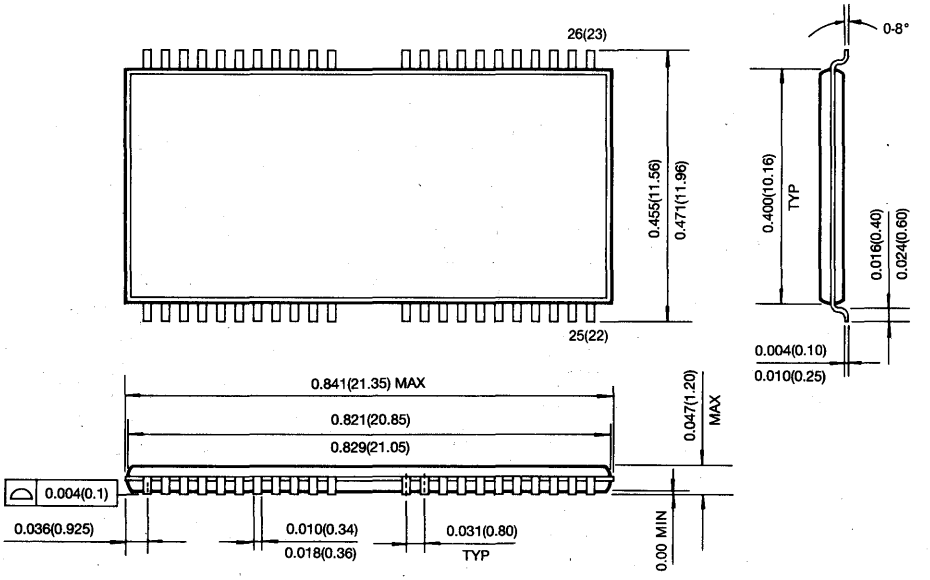
PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



1M x 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM416V1000A-6/A-L6/A-F6	60ns	15ns	110ns
KM416V1000A-7/A-L7/A-F7	70ns	20ns	130ns
KM416V1000A-8/A-L8/A-F8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +3.3V±0.3V power supply**
- **Refresh Cycle**
  - **4096 cycle/64ms (Normal)**
  - **4096 cycle/128ms (L-version)**
  - **4096 cycle/128ms (F-version)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

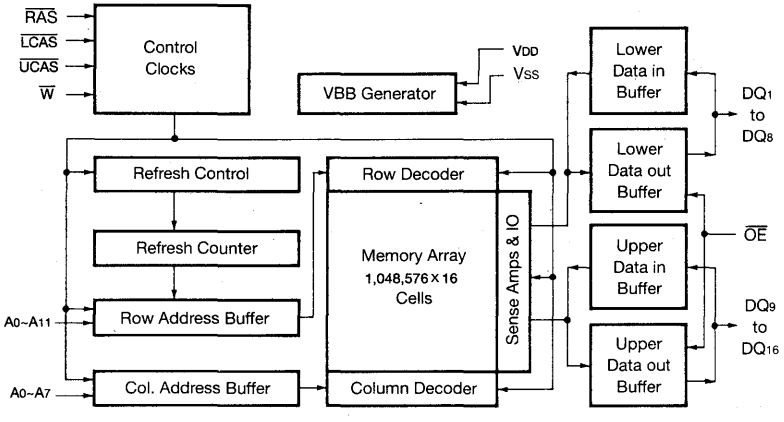
GENERAL DESCRIPTION

The Samsung KM416V1000A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

The KM416V1000A/A-L/A-F features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416V1000A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



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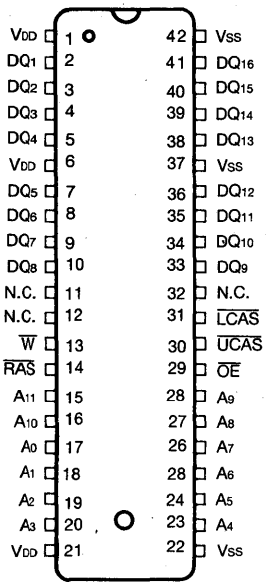
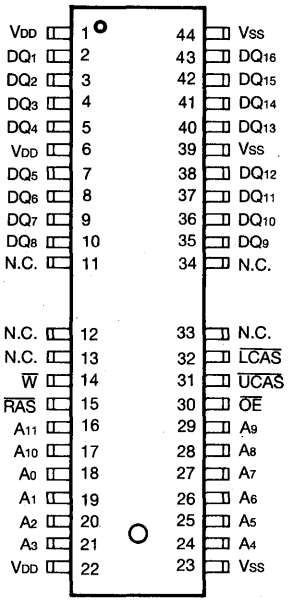
PIN CONFIGURATION (Top Views)

• KM416V1000AJ



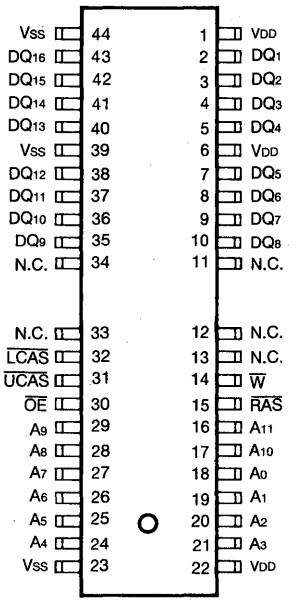
(SOJ)

• KM416V1000AT



(TSOP(II)-Forword)

• KM416V1000AR



(TSOP(II)-Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-16	Data In/Out
VSS	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VDD	Power(+3.3V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 to 4.6	V
Storage Temperature	T_{stg}	-55 to+150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.1	—	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{RC}=min.)	KM416V1000A-6/A-L6/A-F6	I_{CC1}	-	90	mA
	KM416V1000A-7/A-L7/A-F7			80	mA
	KM416V1000A-8/A-L8/A-F8			70	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})	KM416V1000A	I_{CC2}	-	2	mA
	KM416V1000A-L			1	mA
	KM416V1000A-F			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM416V1000A-6/A-L6/A-F6	I_{CC3}	-	90	mA
	KM416V1000A-7/A-L7/A-F7			80	mA
	KM416V1000A-8/A-L8/A-F8			70	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC}=min.)	KM416V1000A-6/A-L6/A-F6	I_{CC4}	-	90	mA
	KM416V1000A-7/A-L7/A-F7			80	mA
	KM416V1000A-8/A-L8/A-F8			70	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{DD}-0.2V)	KM416V1000A	I_{CC5}	-	1	mA
	KM416V1000A-L			300	μA
	KM416V1000A-F			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC}=min.)	KM416V1000A-6/A-L6/A-F6	I_{CC6}	-	90	mA
	KM416V1000A-7/A-L7/A-F7			80	mA
	KM416V1000A-8/A-L8/A-F8			70	mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V_{IH})=V_{DD}-0.2V, Input Low Voltage(V_{IL})=0.2V $\overline{UCAS}$, $\overline{LCAS}$= 0.2V D_{IN}=Don't Care, t_{RC}=31.25μs (L-Version) t_{RAS}=t_{RAS} min~300ns	KM416V1000A-L	I_{CC7}	-	450	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL} $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{DD}-0.2V or 0.2V DQ_1-DQ_{16}=V_{DD}-0.2V or 0.2V or Open	KM416V1000A-F	I_{CCS}	-	250	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{DD}+0.3V, all other pins not under test=0 V)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{DD})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once while page mode cycle time t_{PC}.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V. f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

(Test condition : V_{IH}/V_{IL}=2.1V/0.8V, V_{OH}/V_{OL}=2.0V/0.8V, Output Loading C_L=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		20		ns	
Data-in set-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	10		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		95		100		ns	
$\overline{RAS}$ pulse eidth (Fast page mode)	tRASP	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	
$\overline{CAS}$ precharge time (Fast page mode)	tCP	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	15		20		20		ns	

AC CHARACTERISTICS (Continued)

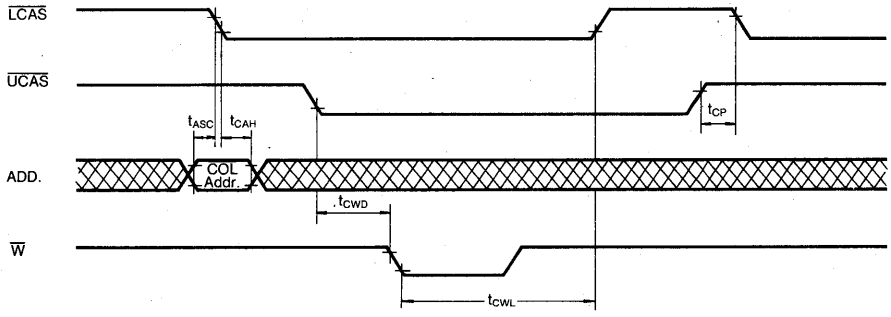
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
$\overline{RAS}$ pulse width (F-ver)	tRASS	100		100		100		μs	19
$\overline{RAS}$ precharge time (F-ver)	tRPS	110		130		150		ns	19
$\overline{CAS}$ hlod time (F-ver)	tCHS	-50		-50		-50		ns	19

KM416V1000A/A-L/A-F Truth Table

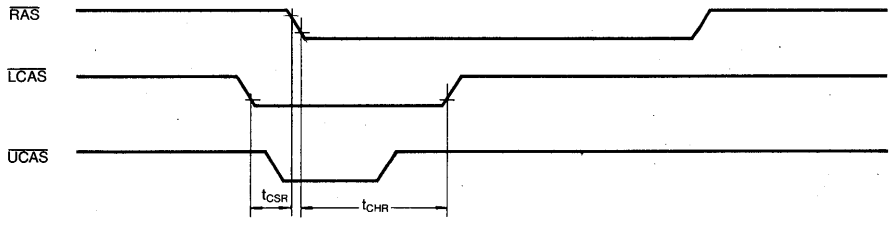
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ_1~DQ_8	DQ_9~DQ_{16}	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

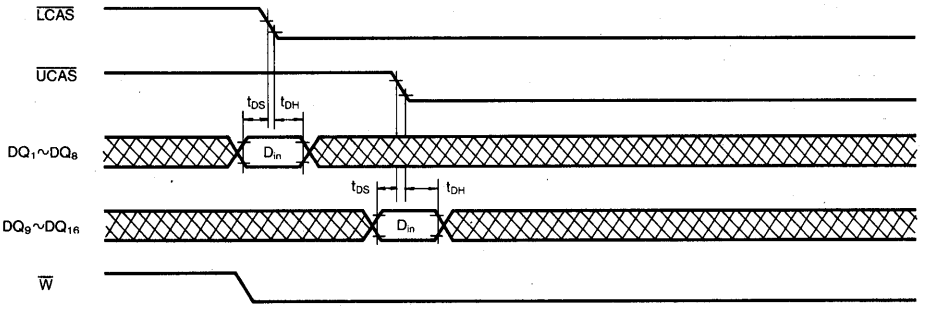
1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL Loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. t_{OFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
17. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



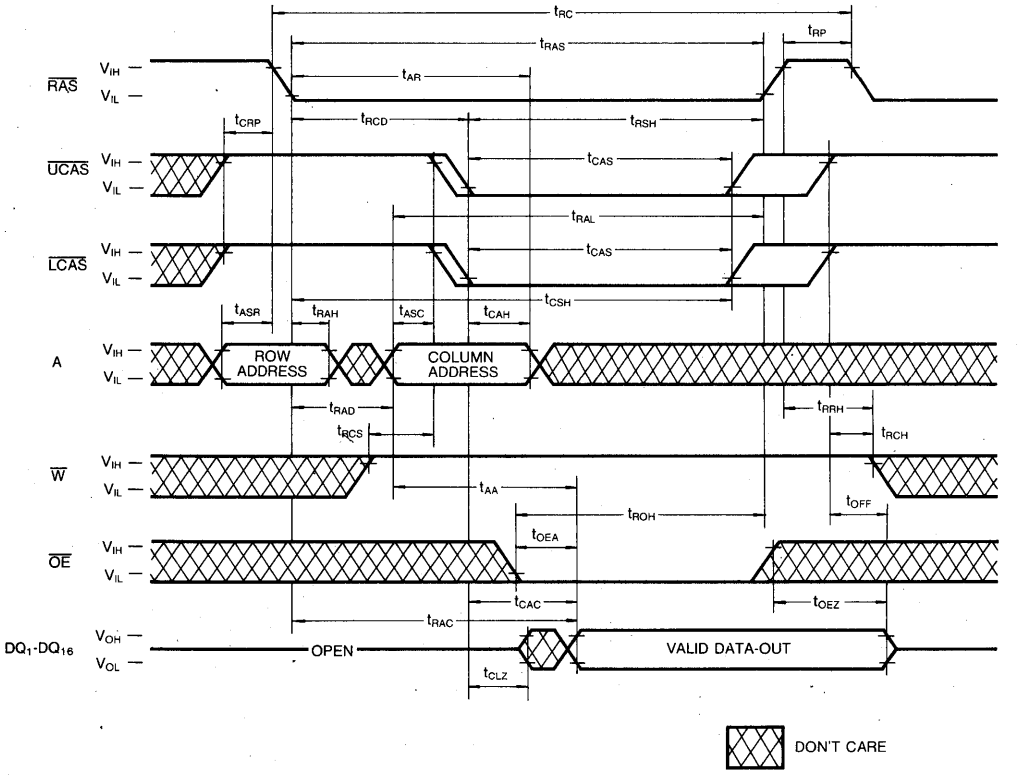
18. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim8)}$, upper byte $D_{in(9\sim16)}$



19. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (F-version).

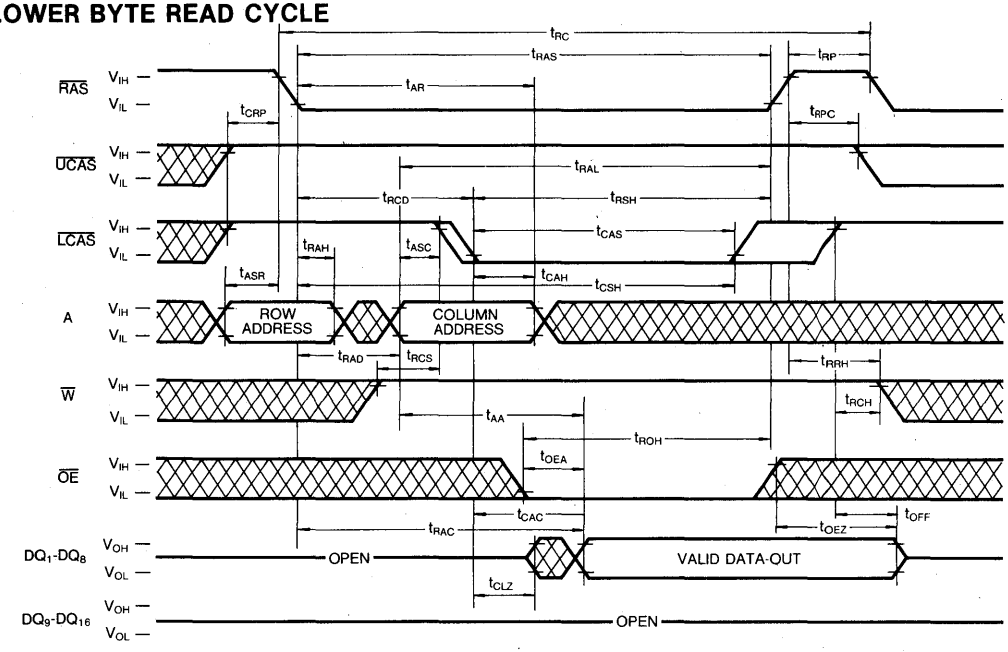
TIMING DIAGRAMS

WORD READ CYCLE

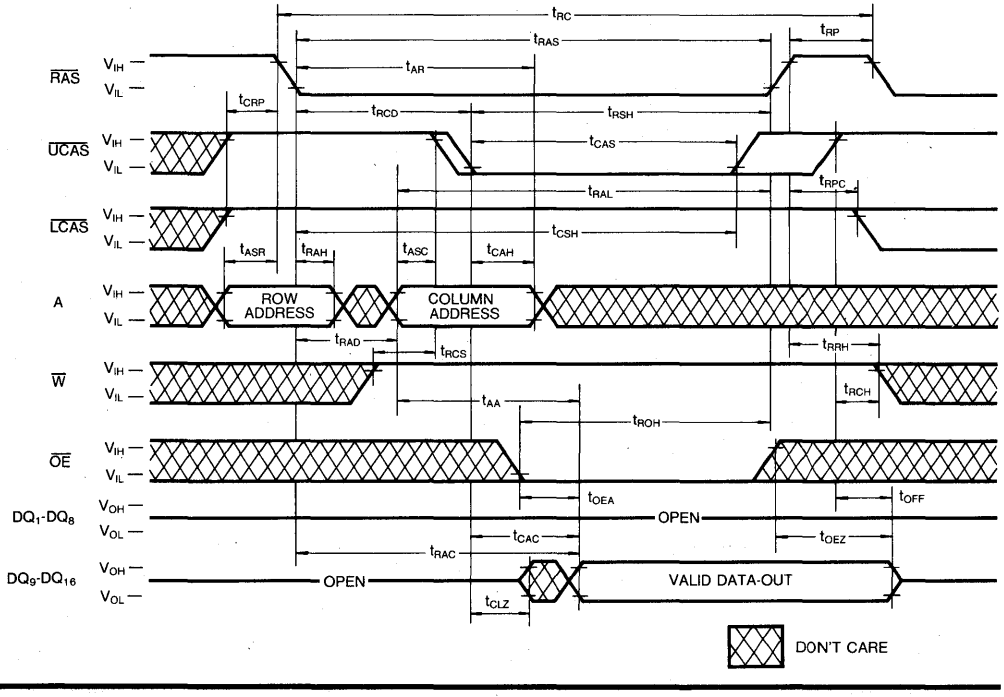


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

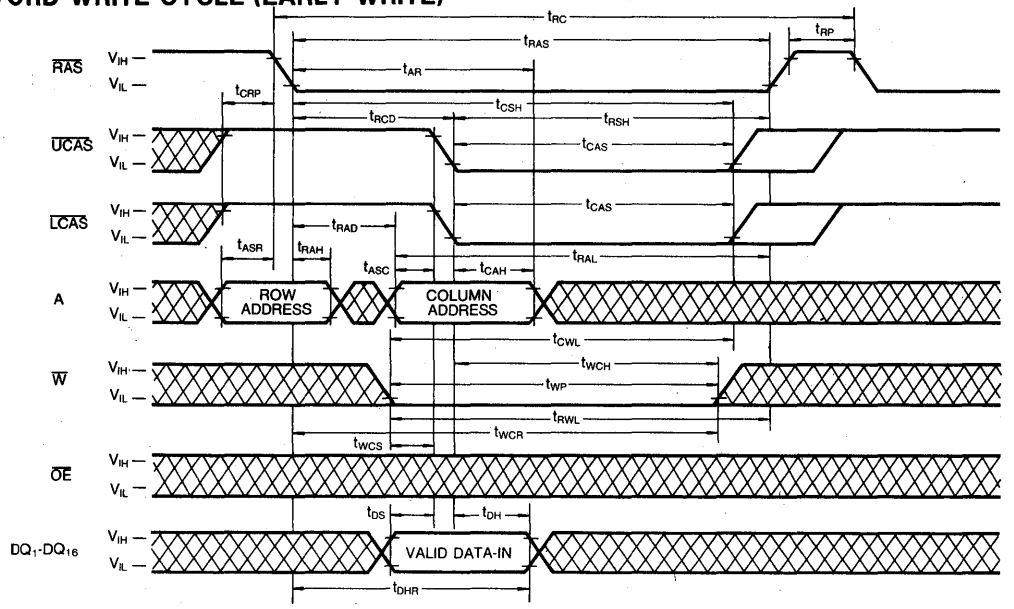


UPPER BYTE READ CYCLE

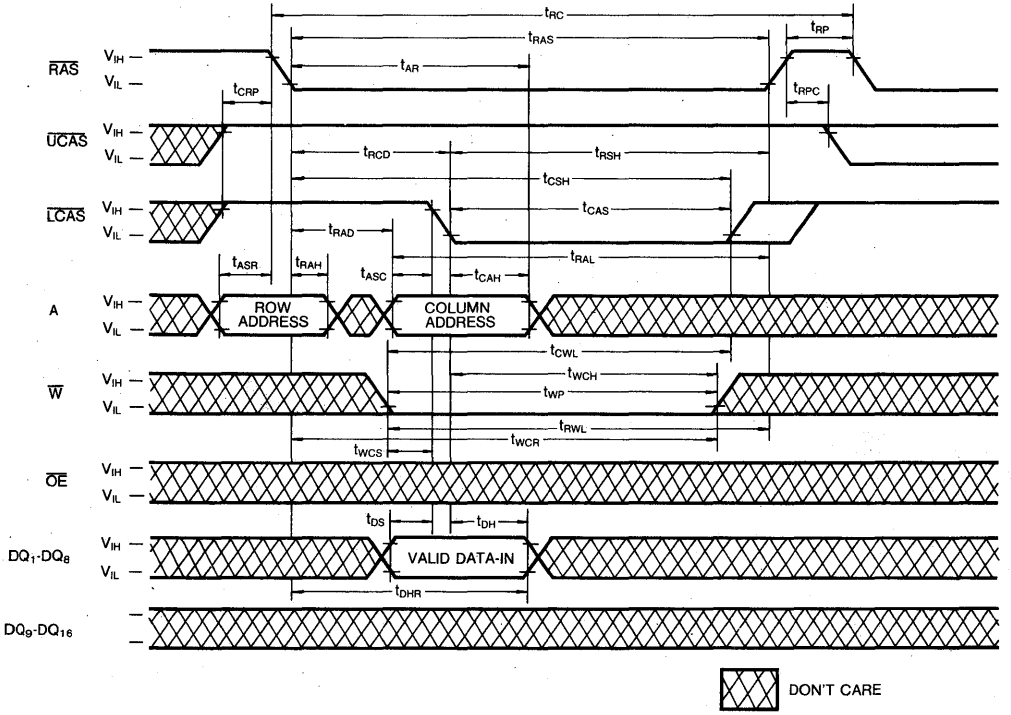


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)

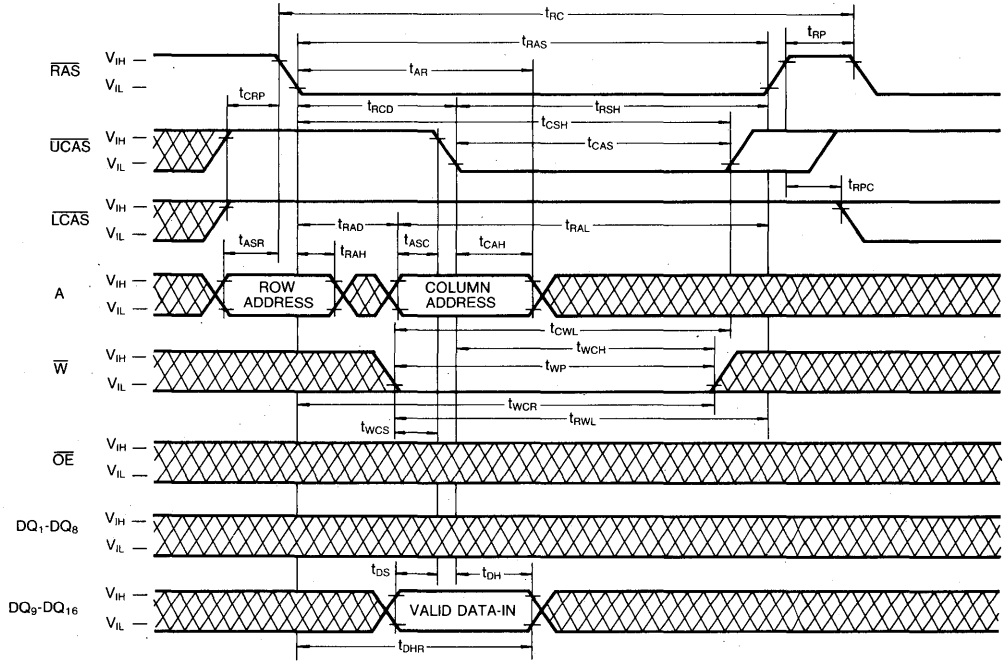


LOWER BYTE WRITE CYCLE (EARLY WRITE)

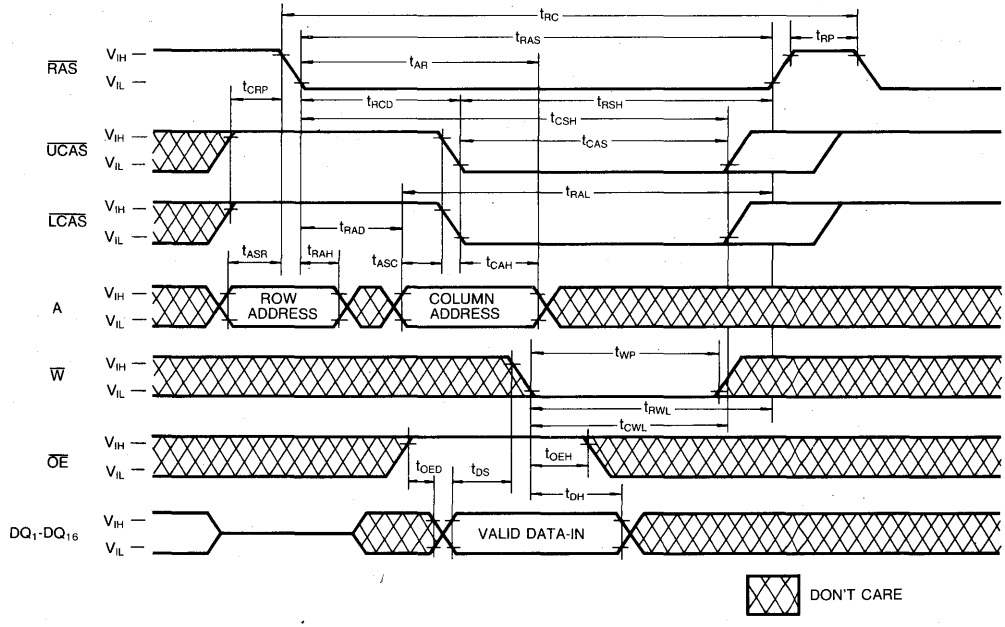


TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

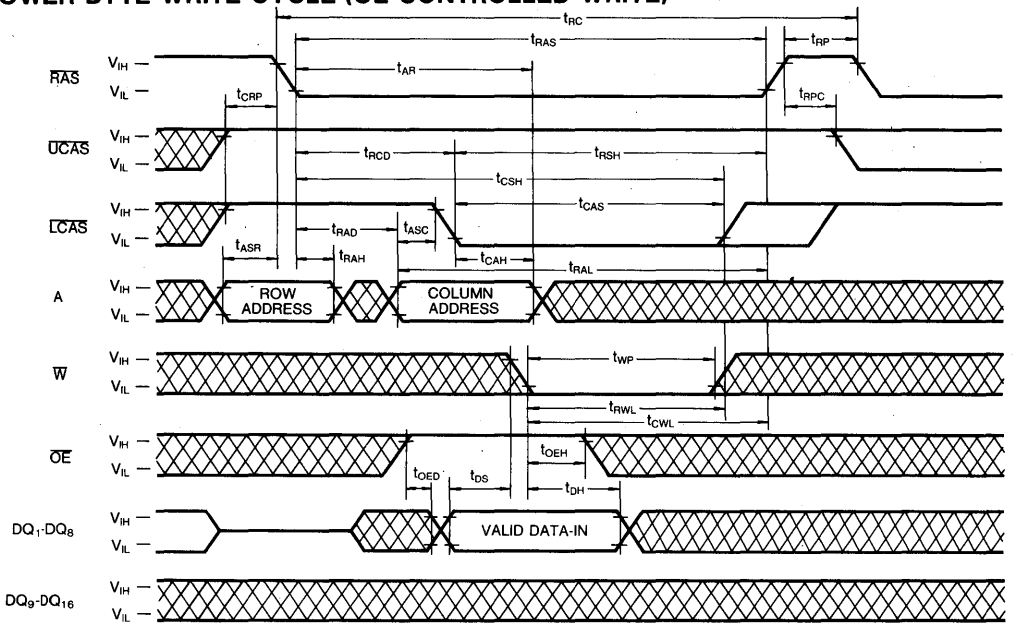


WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

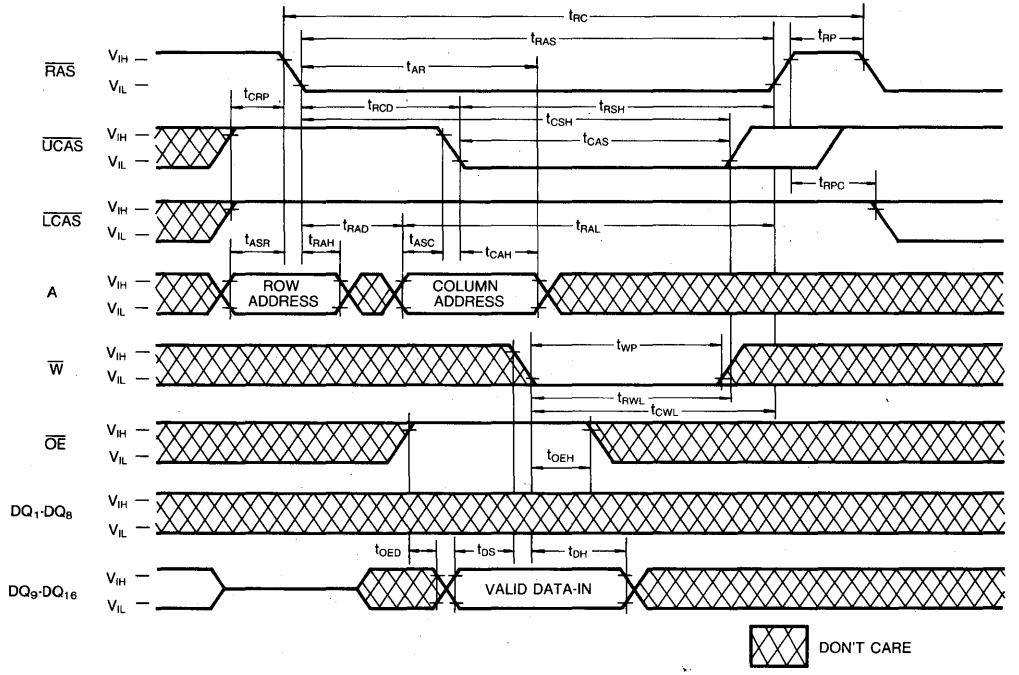


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

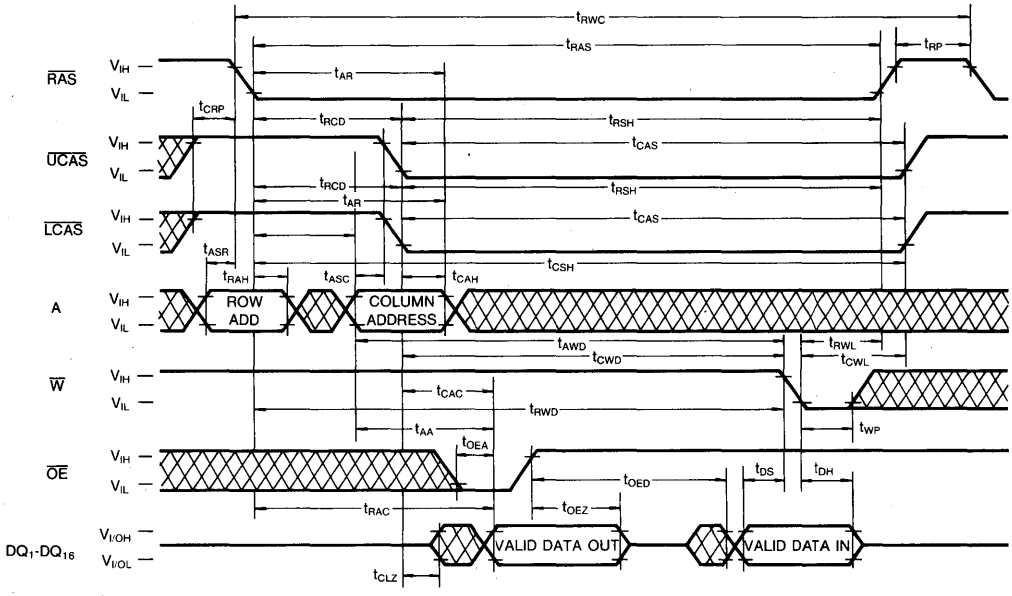


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

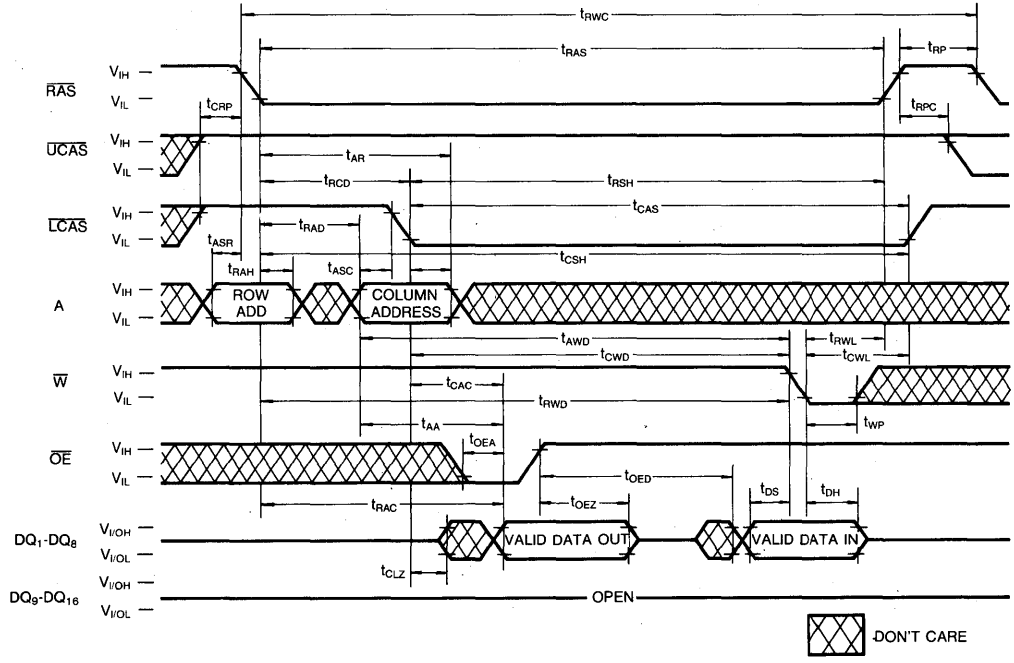


TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

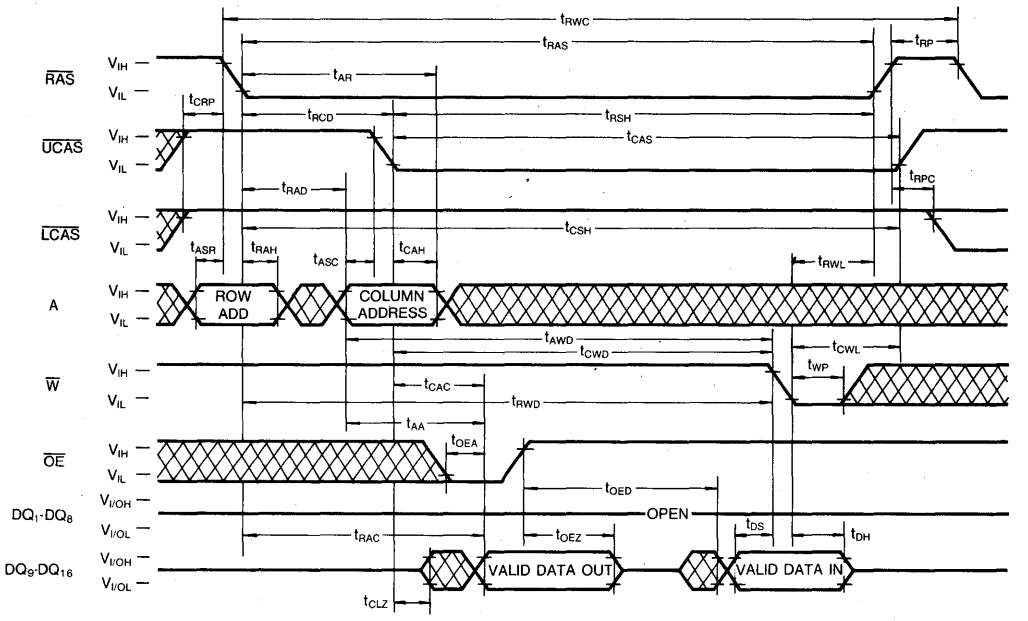


READ-MODIFY-LOWER-BYTE-WRITE CYCLE

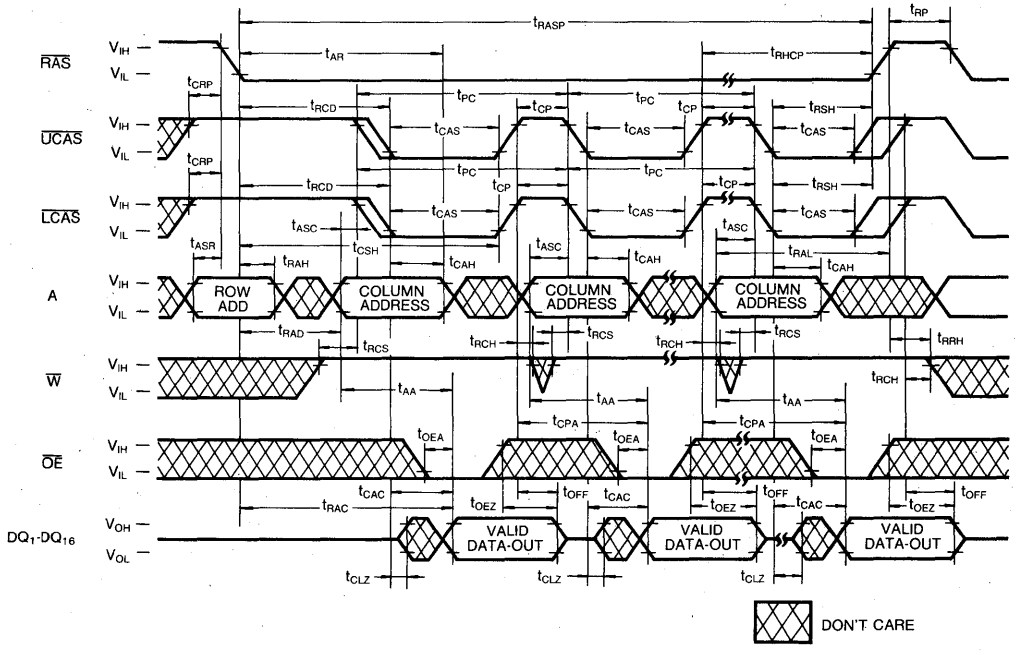


TIMING DIAGRAMS (Continued)

READ-MODIFY-UPPER-BYTE-WRITE CYCLE

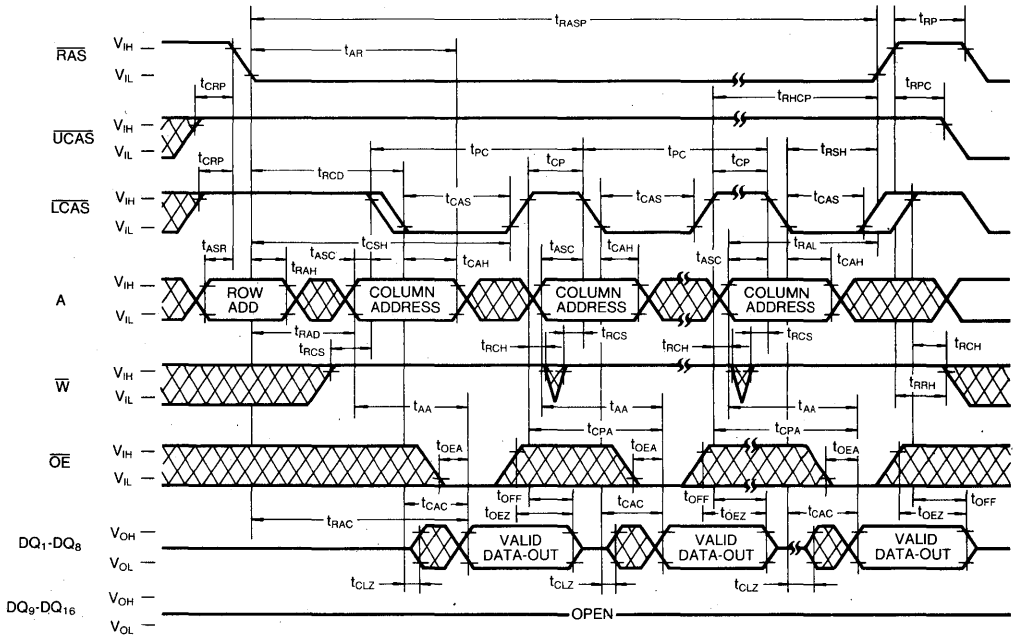


FAST PAGE MODE WORD READ CYCLE

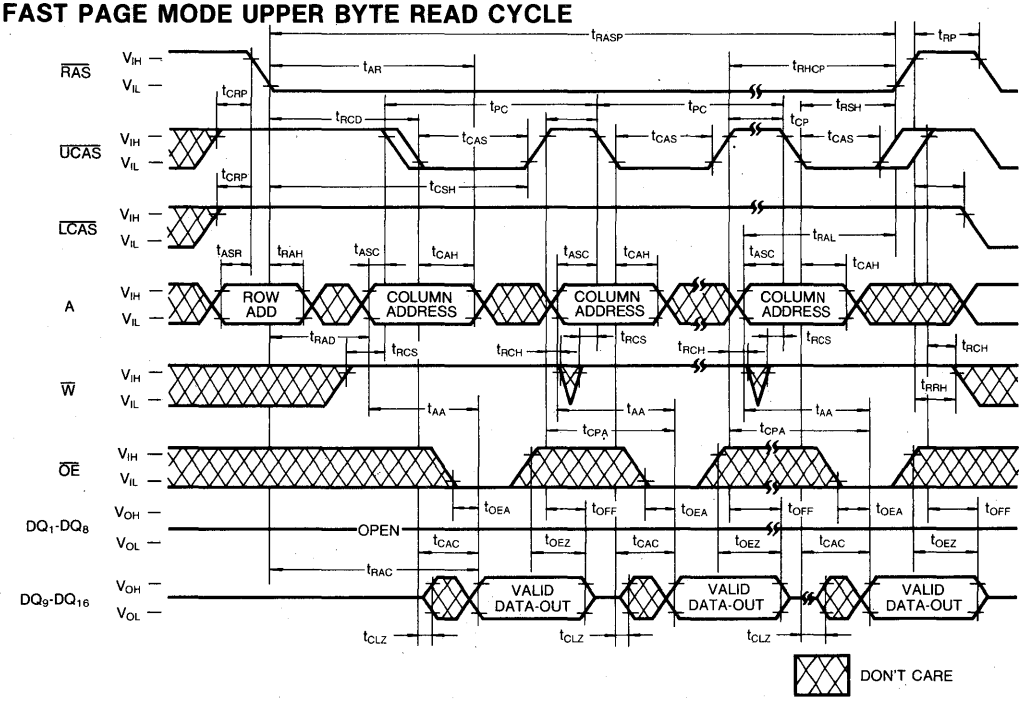


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE



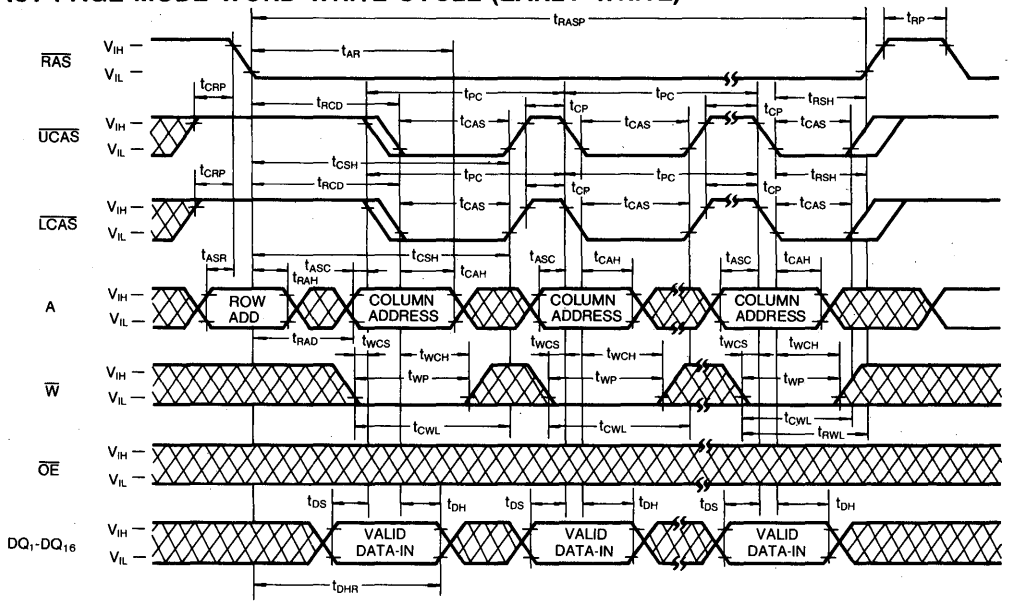
FAST PAGE MODE UPPER BYTE READ CYCLE



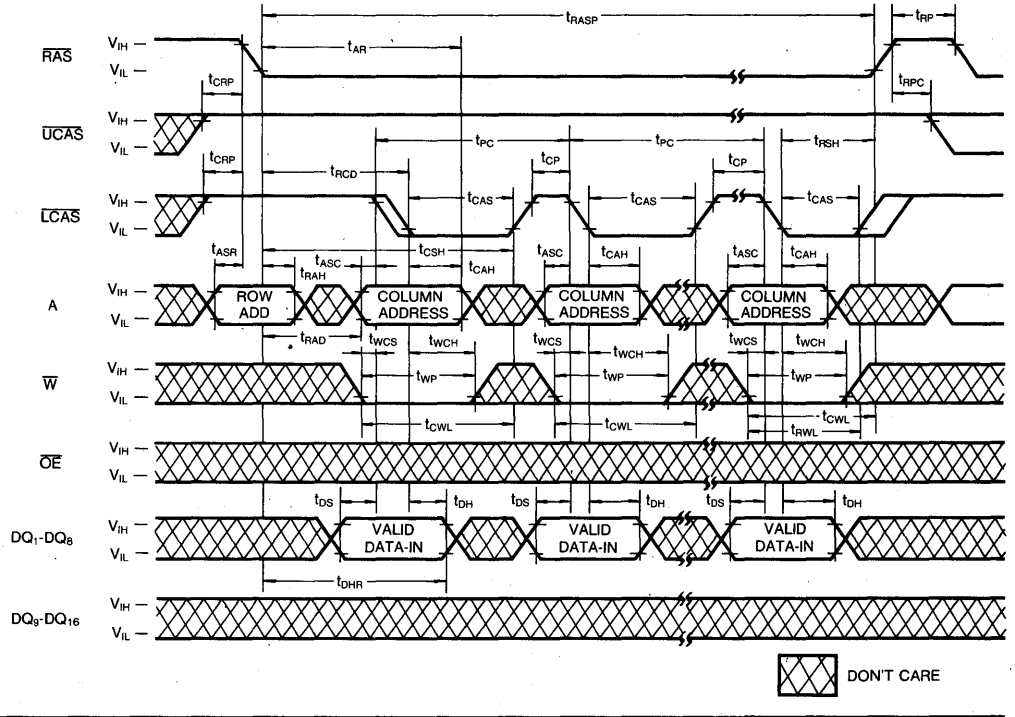
6

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

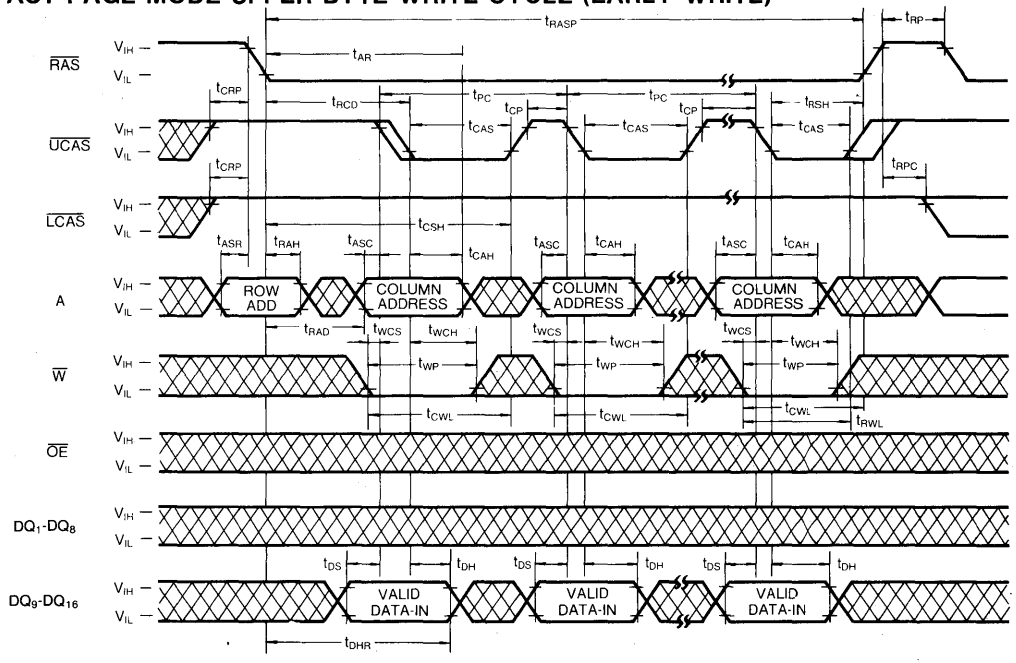


FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)

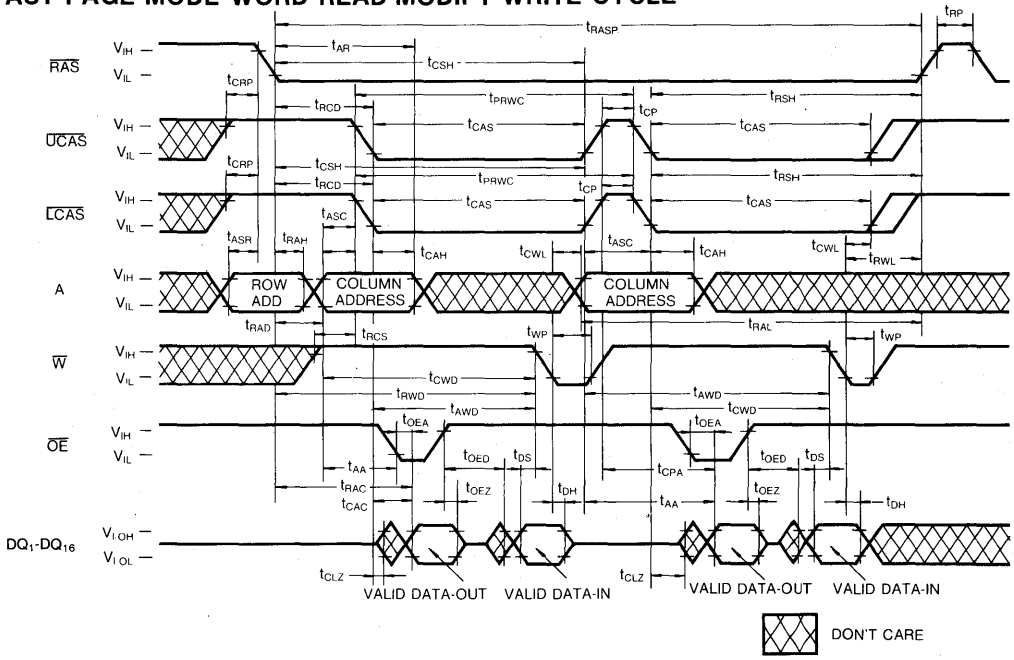


TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

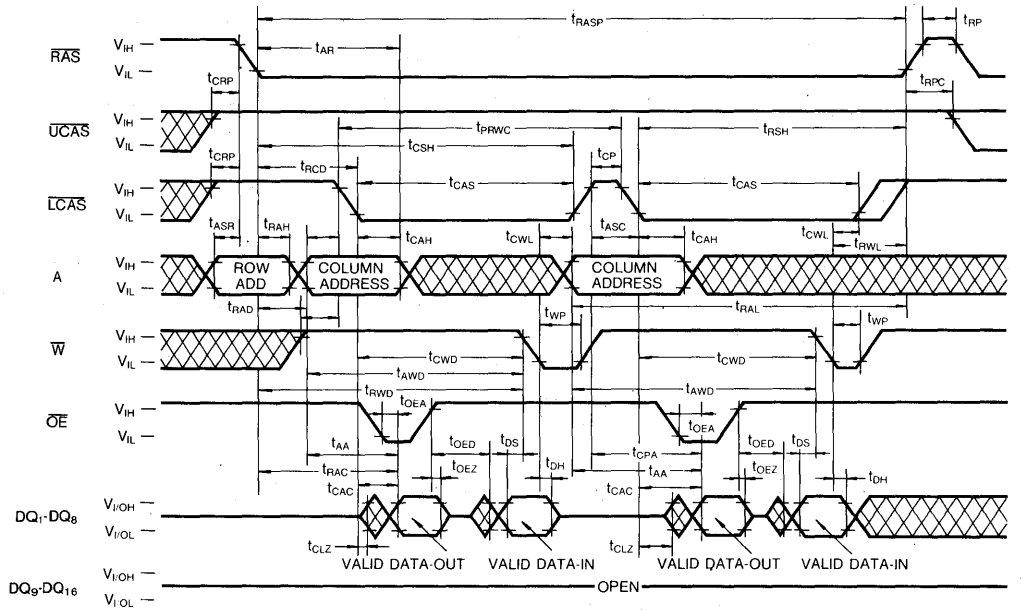


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

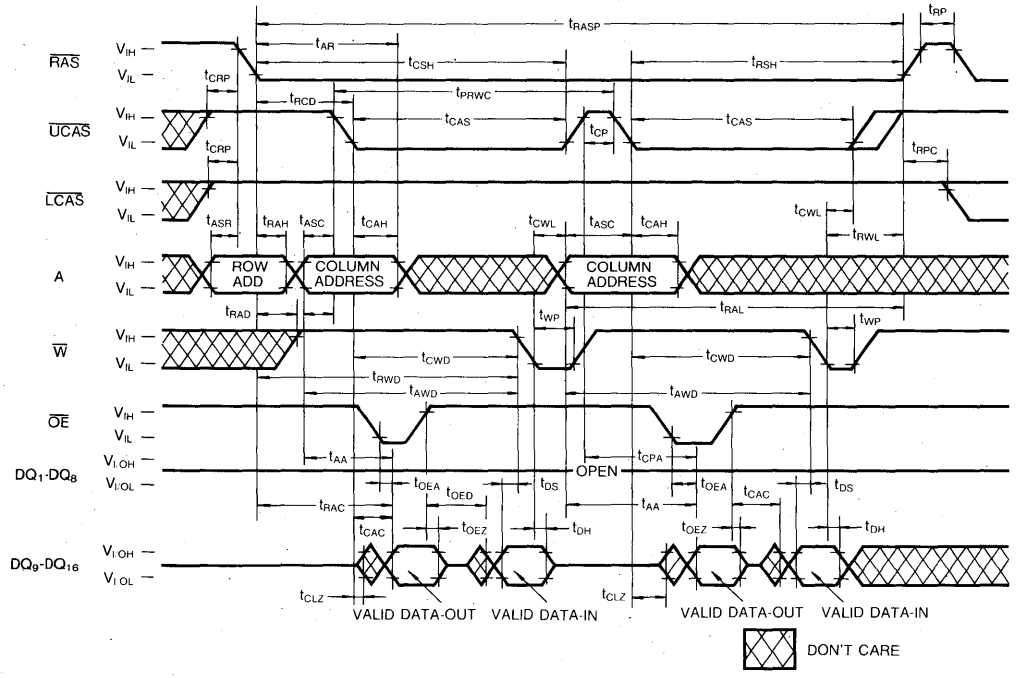


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



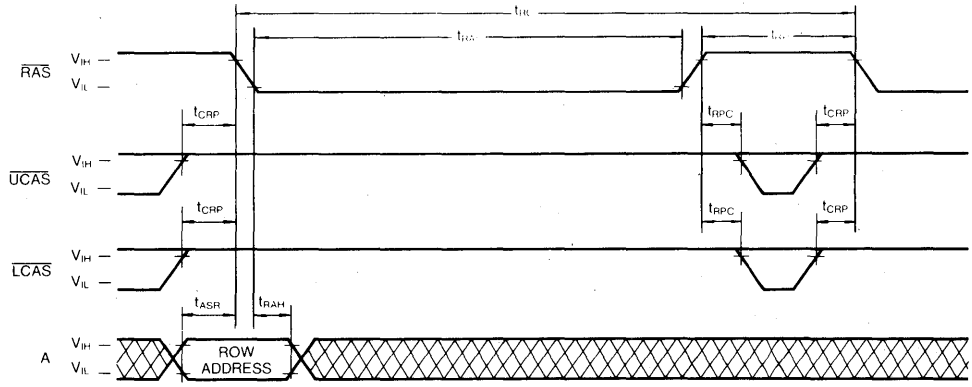
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



TIMING DIAGRAMS (Continued)

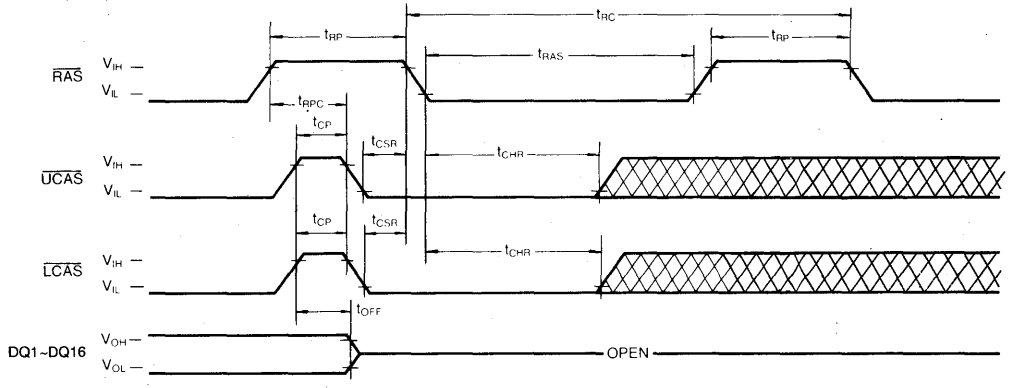
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



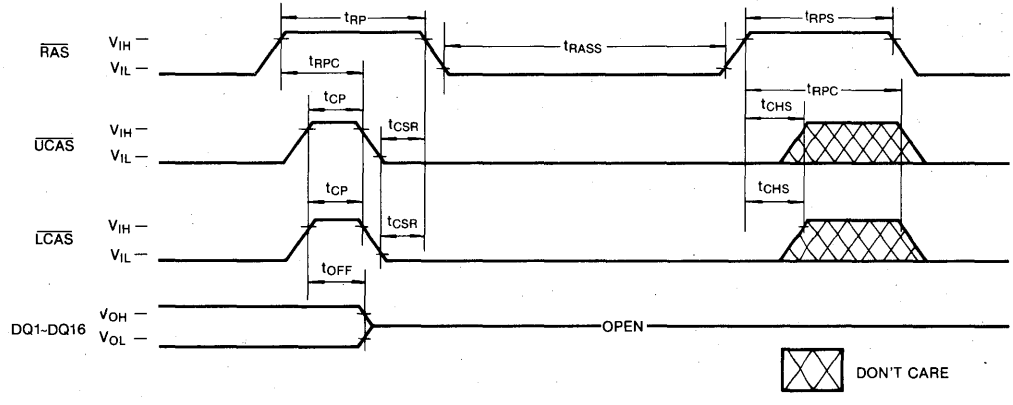
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: W, OE, A = Don't Care



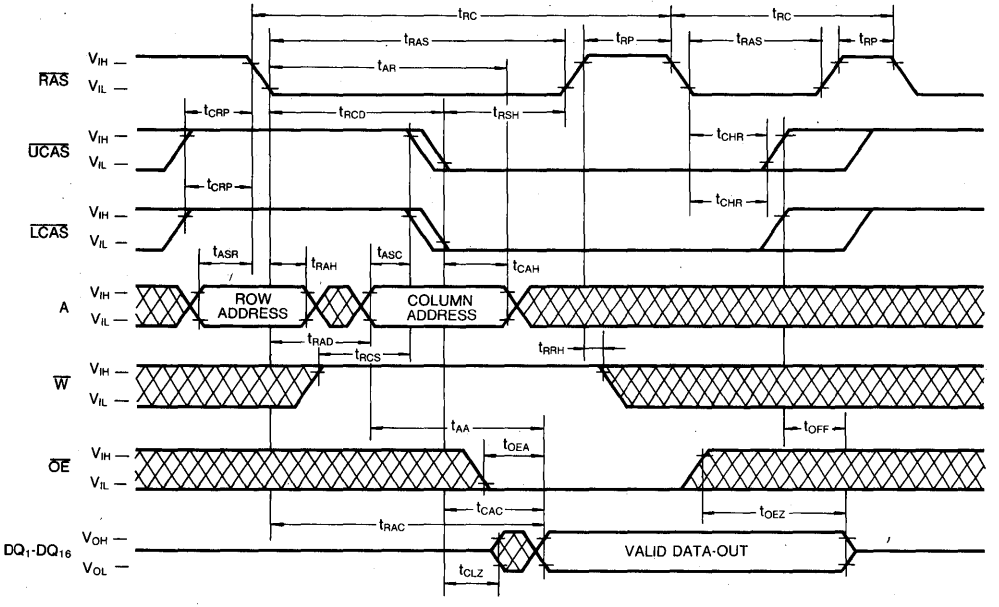
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (Self restresh only)

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care

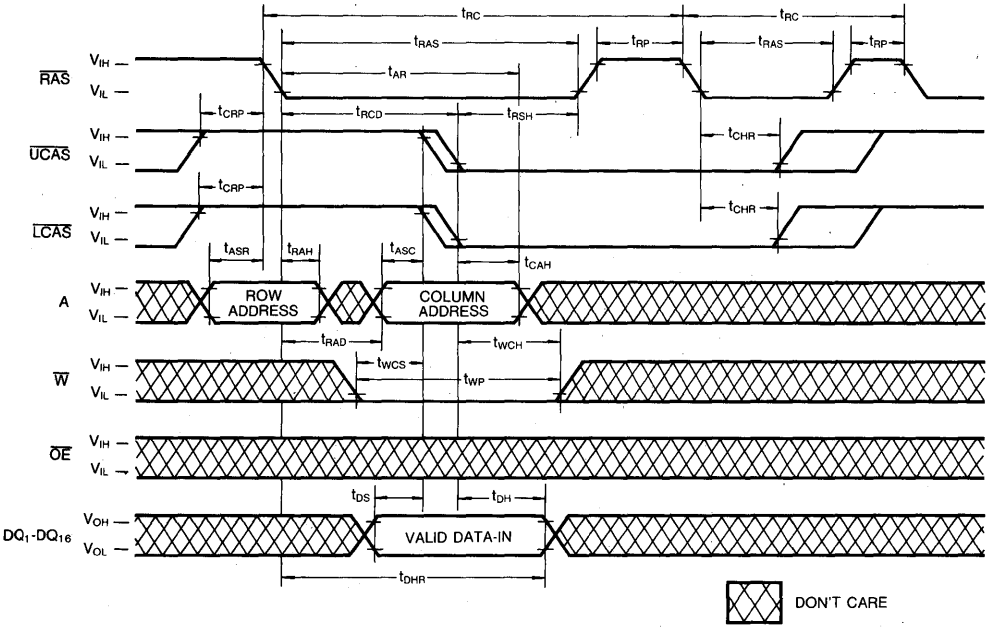


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

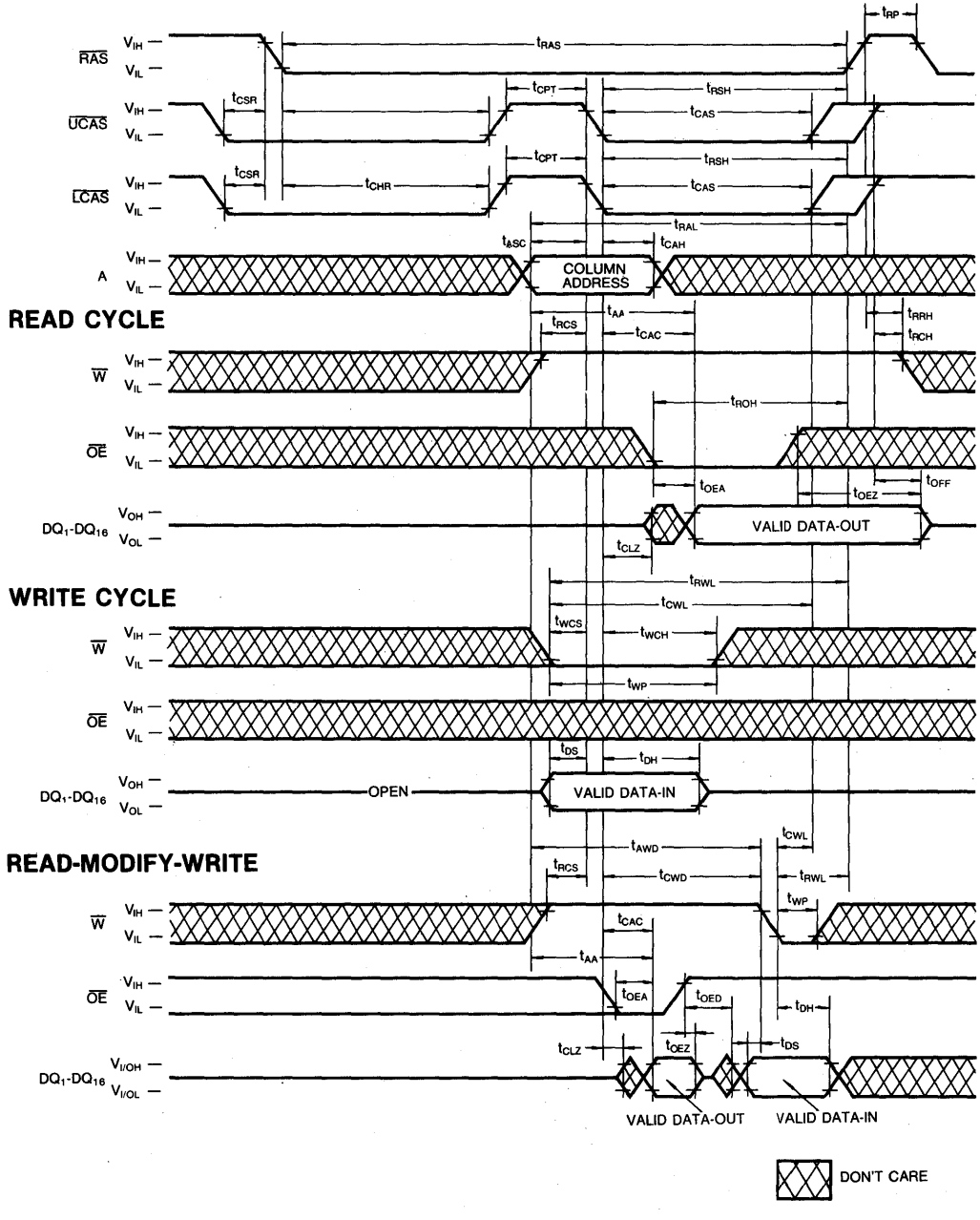


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



READ CYCLE

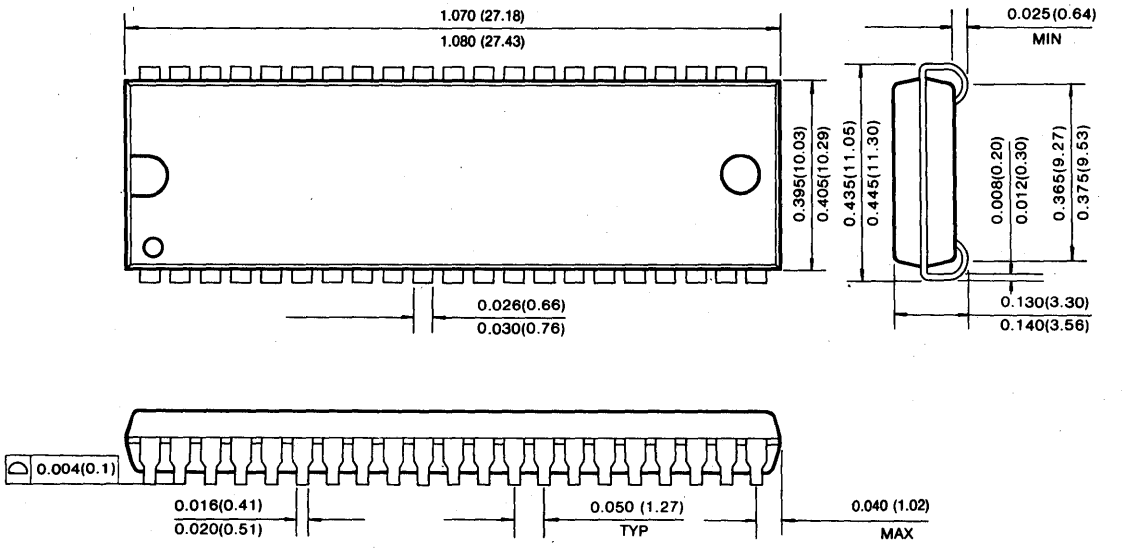
WRITE CYCLE

READ-MODIFY-WRITE

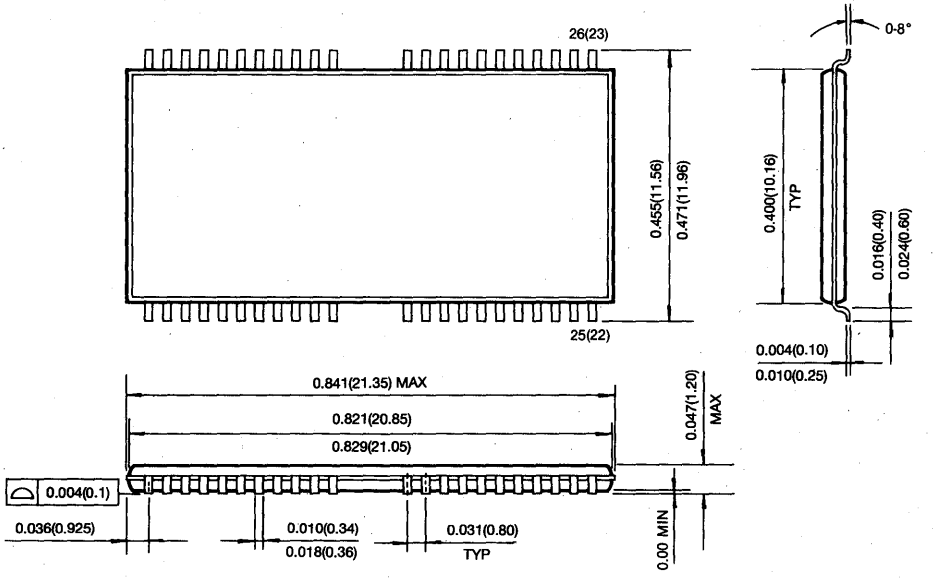
PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



1M x 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM416V1200A-6/A-L6/A-F6	60ns	15ns	110ns
KM416V1200A-7/A-L7/A-F7	70ns	20ns	130ns
KM416V1200A-8/A-L8/A-F8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +3.3V±0.3V power supply**
- **Refresh Cycle**
  - **1024 cycle/16ms (Normal)**
  - **1024 cycle/128ms (L-version)**
  - **1024 cycle/128ms (F-version)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

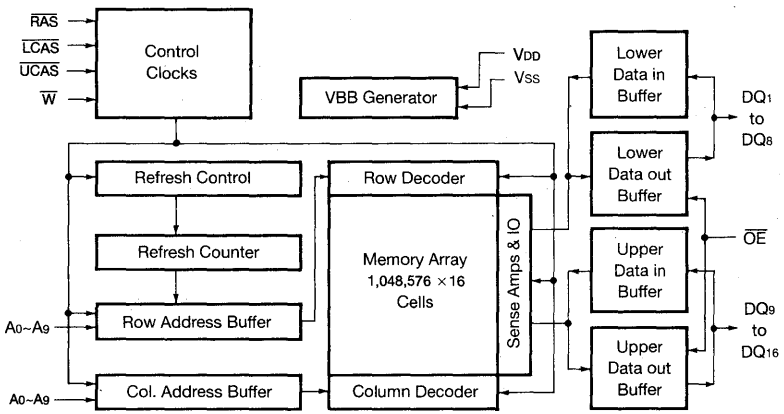
GENERAL DESCRIPTION

The Samsung KM416V1200A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

The KM416V1200A/A-L/A-F features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416V1200A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

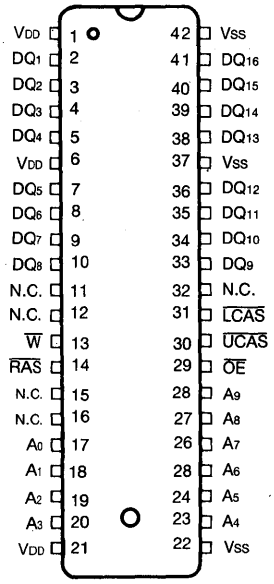
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

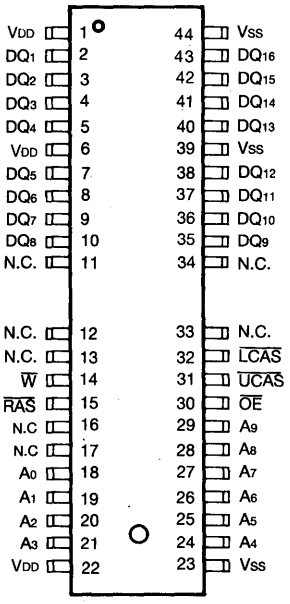
PIN CONFIGURATION (Top Views)

• KM416V1200AJ



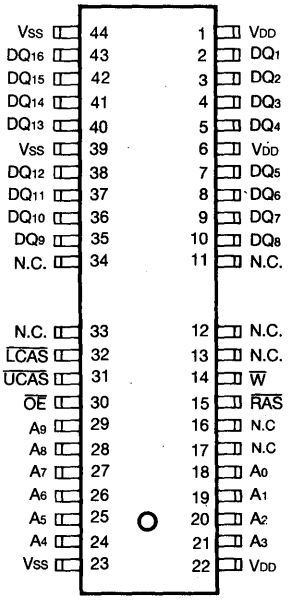
(SOJ)

• KM416V1200AT



(TSOP(II)-Forword)

• KM416V1200AR



(TSOP(II)-Reverse)

Pin Name	Pin Function
A0-A9	Address Inputs
DQ1-16	Data In/Out
VSS	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VDD	Power(+3.3V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 to 4.6	V
Storage Temperature	T_{stg}	-55 to+150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.1	—	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{RC}=min.)	KM416V1200A-6/A-L6/A-F6	I_{CC1}	-	150	mA
	KM416V1200A-7/A-L7/A-F7			140	mA
	KM416V1200A-8/A-L8/A-F8			130	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})	KM416V1200A	I_{CC2}	-	2	mA
	KM416V1200A-L			1	mA
	KM416V1200A-F			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM416V1200A-6/A-L6/A-F6	I_{CC3}	-	150	mA
	KM416V1200A-7/A-L7/A-F7			140	mA
	KM416V1200A-8/A-L8/A-F8			130	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC}=min.)	KM416V1200A-6/A-L6/A-F6	I_{CC4}	-	100	mA
	KM416V1200A-7/A-L7/A-F7			90	mA
	KM416V1200A-8/A-L8/A-F8			80	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{DD}-0.2V)	KM416V1200A	I_{CC5}	-	1	mA
	KM416V1200A-L			300	μA
	KM416V1200A-F			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC}=min.)	KM416V1200A-6/A-L6/A-F6	I_{CC6}	-	150	mA
	KM416V1200A-7/A-L7/A-F7			140	mA
	KM416V1200A-8/A-L8/A-F8			130	mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V_{IH})=V_{DD}-0.2V, Input Low Voltage(V_{IL})=0.2V $\overline{UCAS}$, $\overline{LCAS}$= 0.2V D_{IN}=Don't Care, t_{RC}=125μs (L-Version) t_{RAS}=t_{RAS} min~300ns	KM416V1200A-L	I_{CC7}	-	350	μA

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DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_9=V_{DD}-0.2V or 0.2V DQ_1-DQ_{16}=V_{DD}-0.2V or 0.2V or Open	KM416V1200A-F	I_{CCS}	-	250	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{DD}+0.3V, all other pins not under test=0 V)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{DD})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once while page mode cycle time t_{PC}.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V. f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

(Test condition : V_{IH}/V_{IL}=2.1V/0.8V, V_{OH}/V_{OL}=2.0V/0.8V, Output Loading C_L=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		20		ns	
Data-in set-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	10		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		95		100		ns	
$\overline{RAS}$ pulse eidth (Fast page mode)	tRASP	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	
$\overline{CAS}$ precharge time (Fast page mode)	tCP	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	15		20		20		ns	

AC CHARACTERISTICS (Continued)

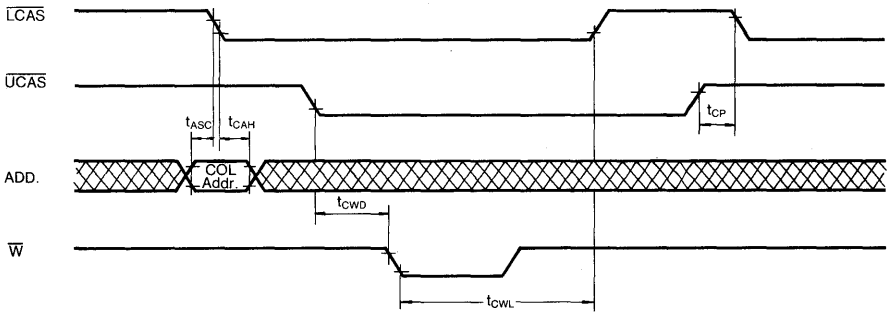
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
$\overline{RAS}$ pulse width (F-ver)	tRASS	100		100		100		μs	19
$\overline{RAS}$ precharge time (F-ver)	tRPS	110		130		150		ns	19
$\overline{CAS}$ hlod time (F-ver)	tCHS	-50		-50		-50		ns	19

KM416V1200A/A-L/A-F Truth Table

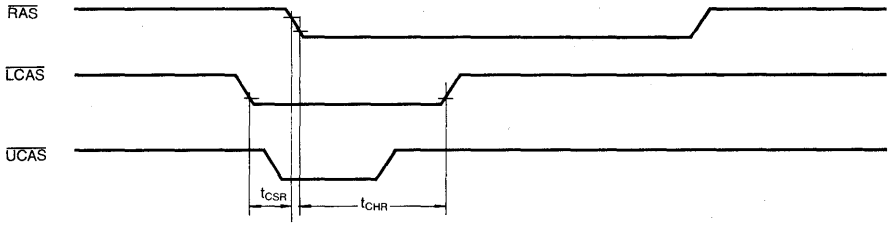
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

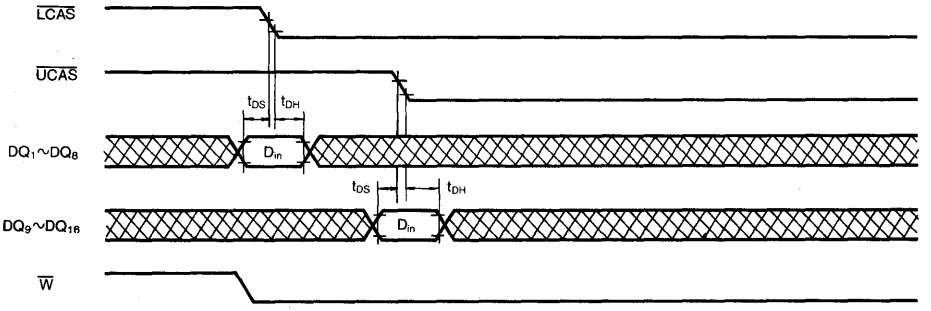
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating aprameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
17. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

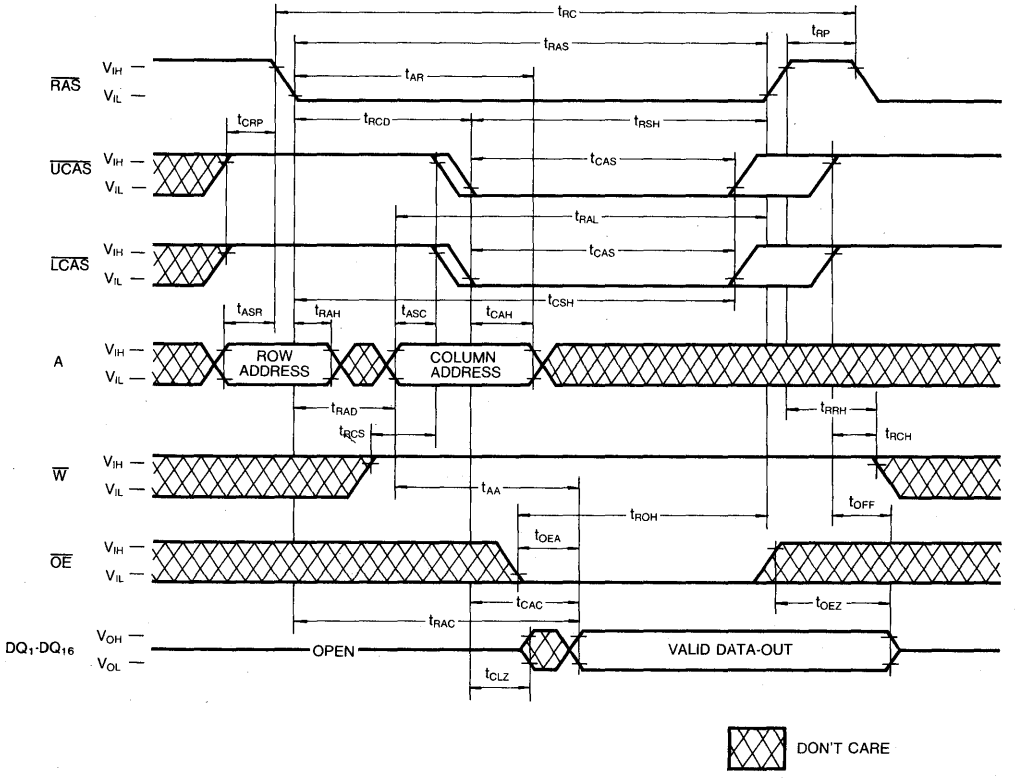


18. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim8)}$, upper byte $D_{in(9\sim16)}$



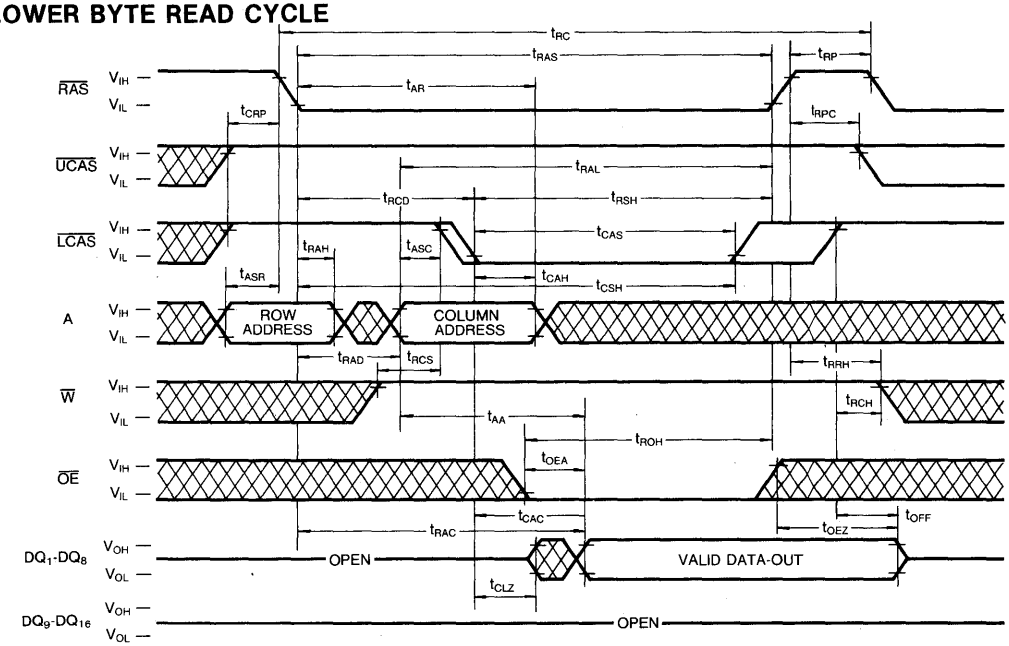
TIMING DIAGRAMS

WORD READ CYCLE

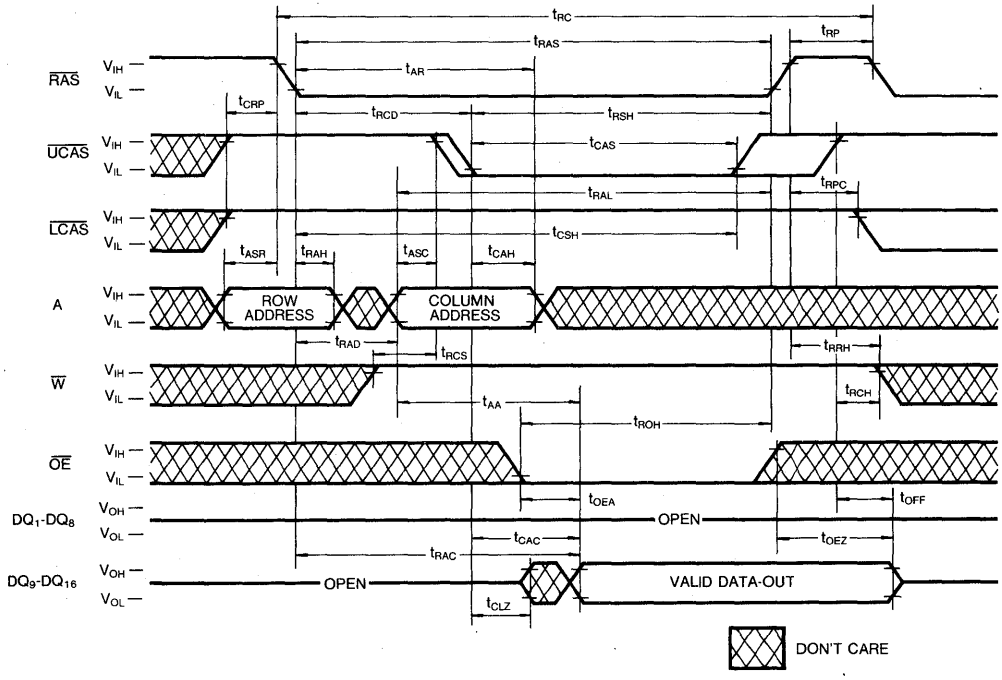


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE



UPPER BYTE READ CYCLE



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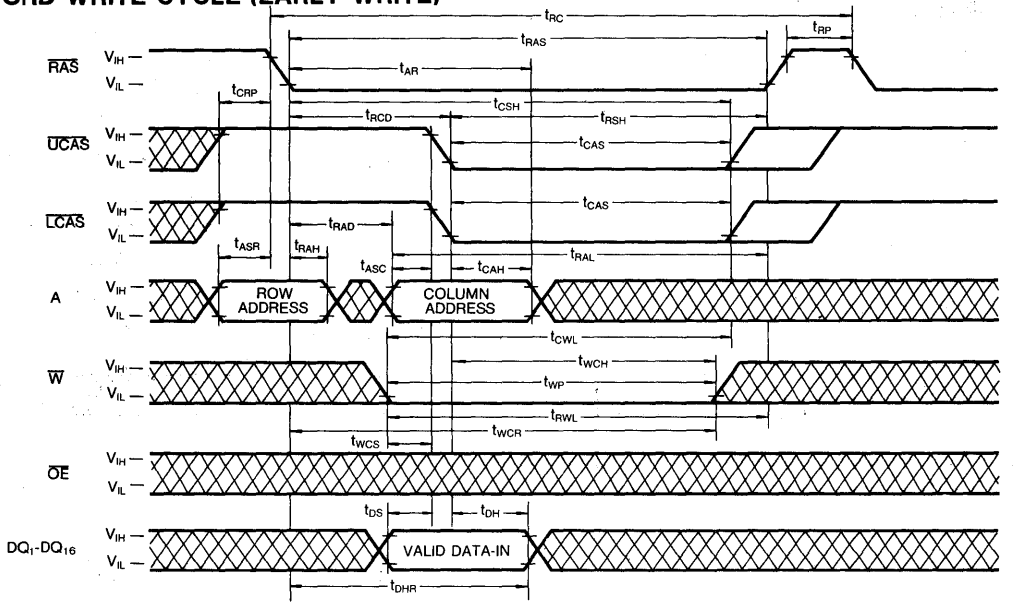
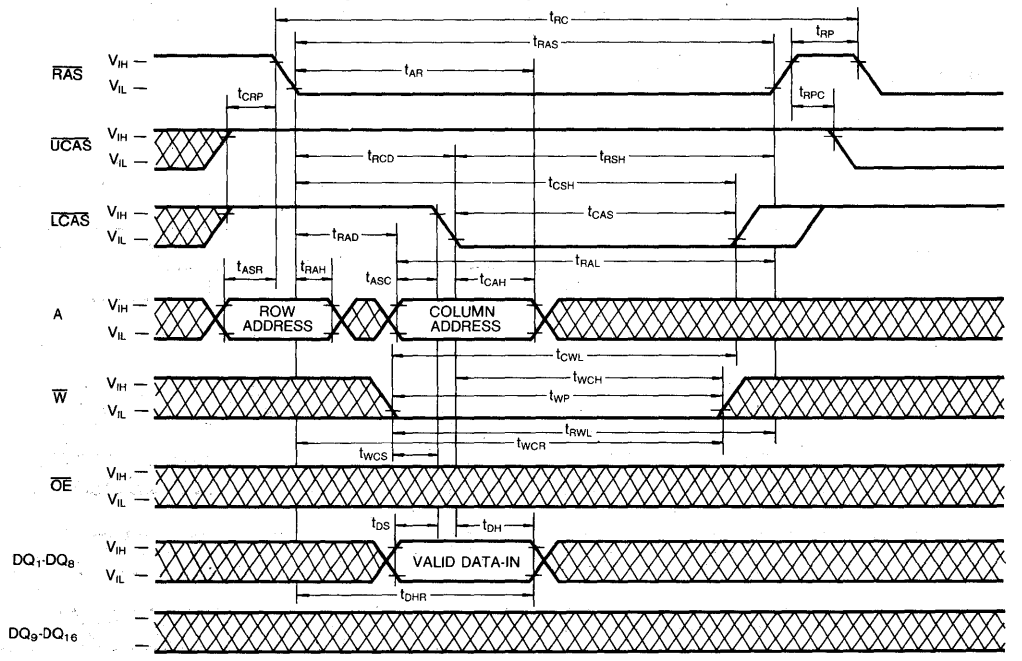
TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)

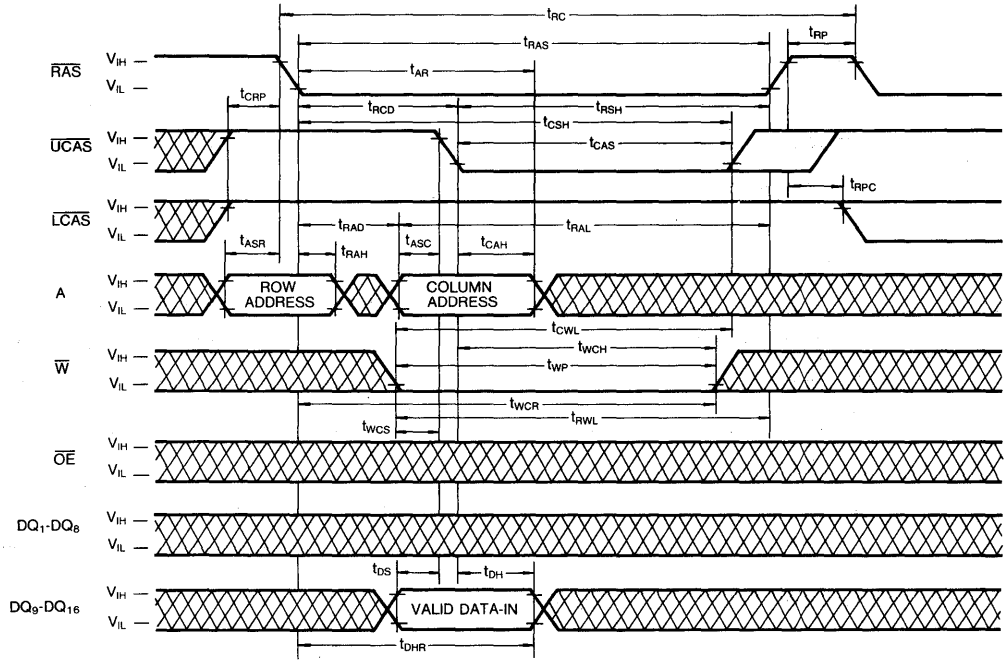


LOWER BYTE WRITE CYCLE (EARLY WRITE)

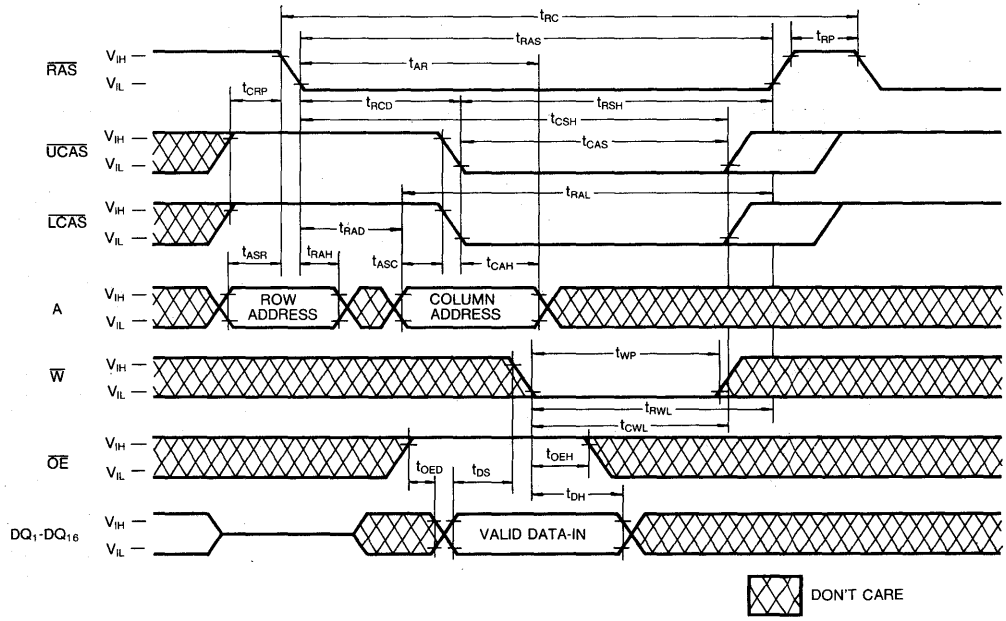


TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

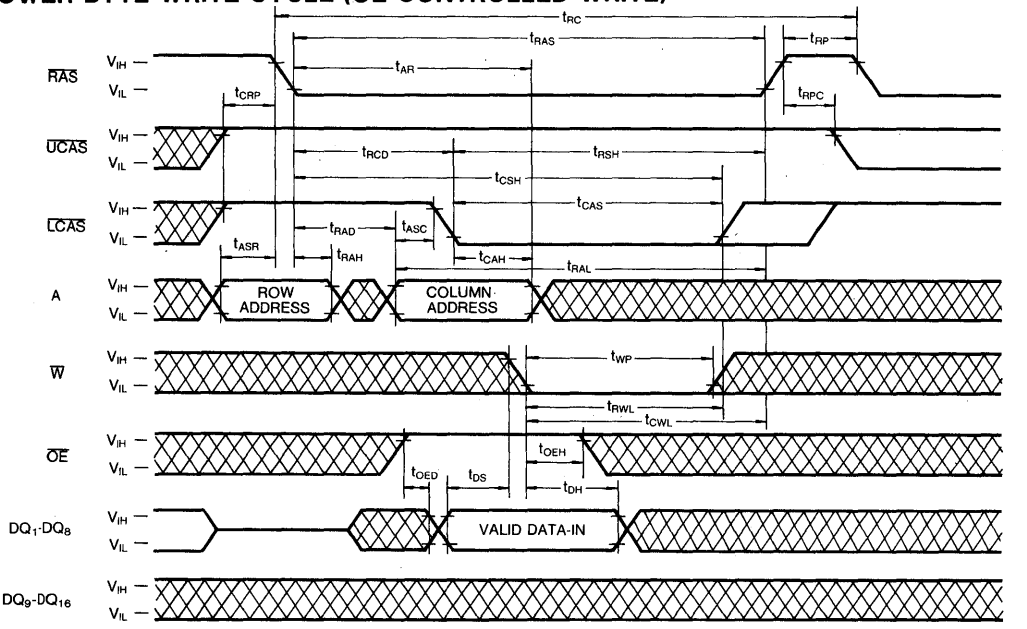


WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

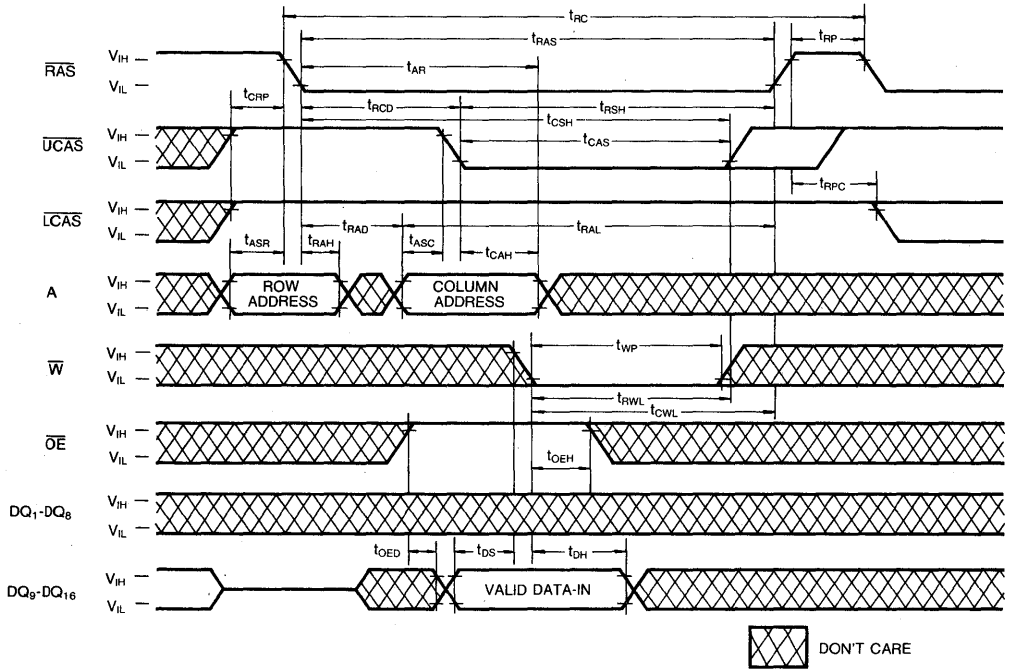


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

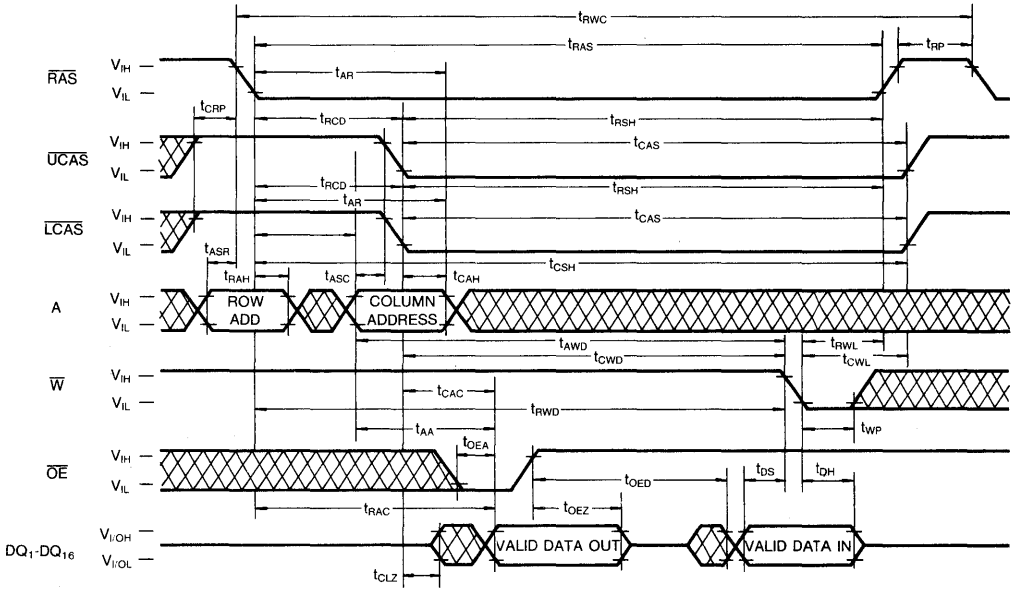


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

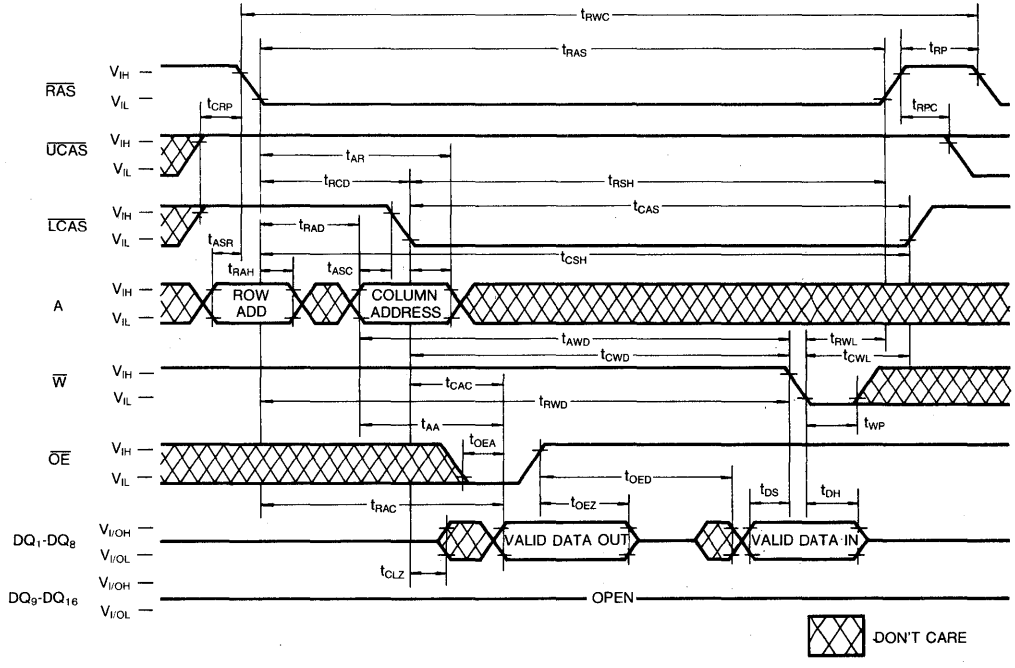


TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

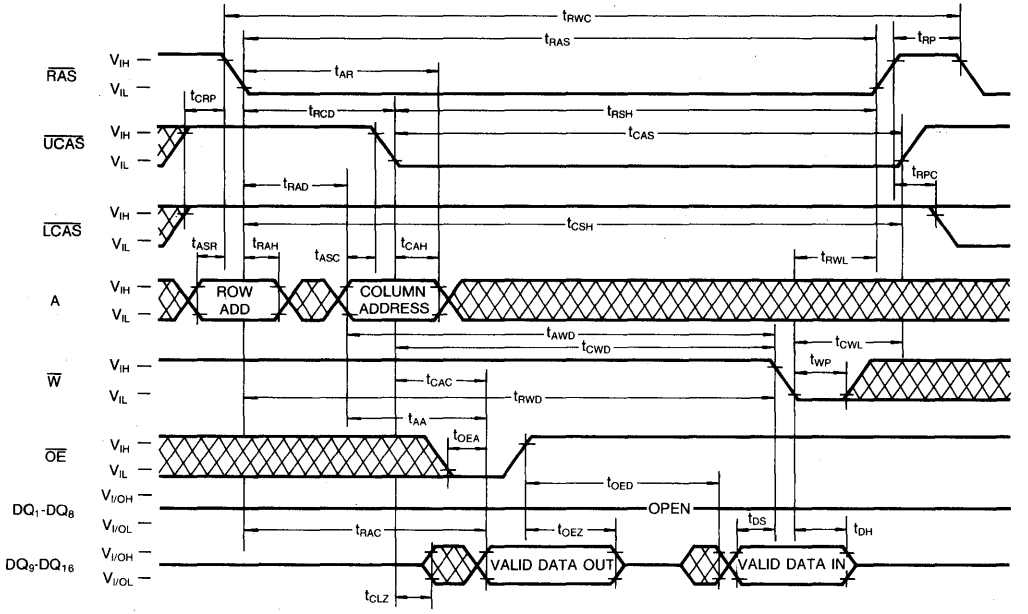


READ-MODIFY-LOWER-BYTE-WRITE CYCLE

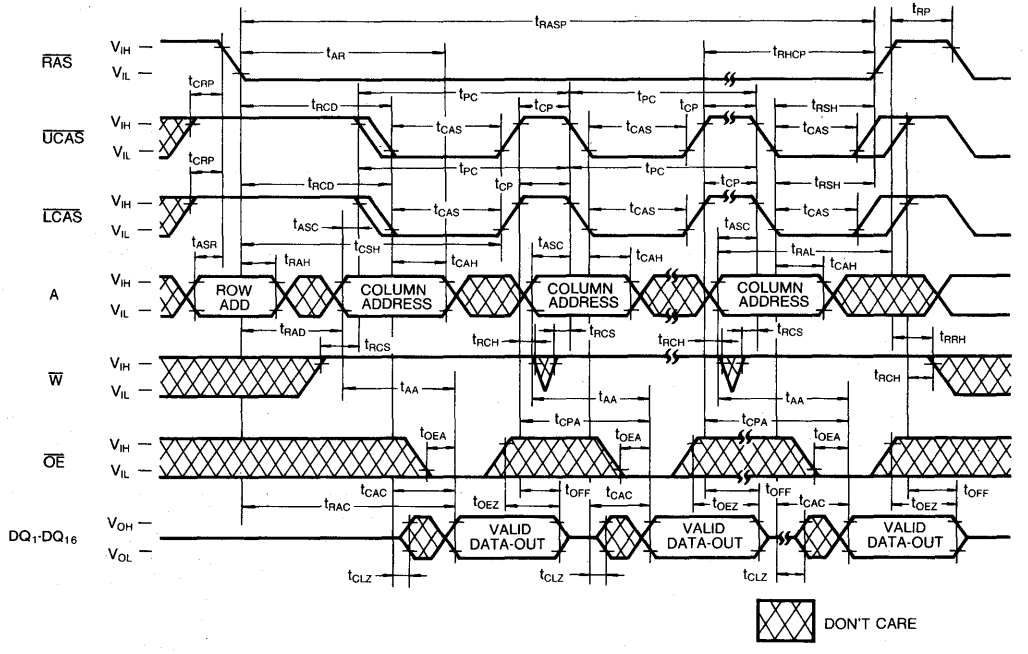


TIMING DIAGRAMS (Continued)

READ-MODIFY-UPPER-BYTE-WRITE CYCLE

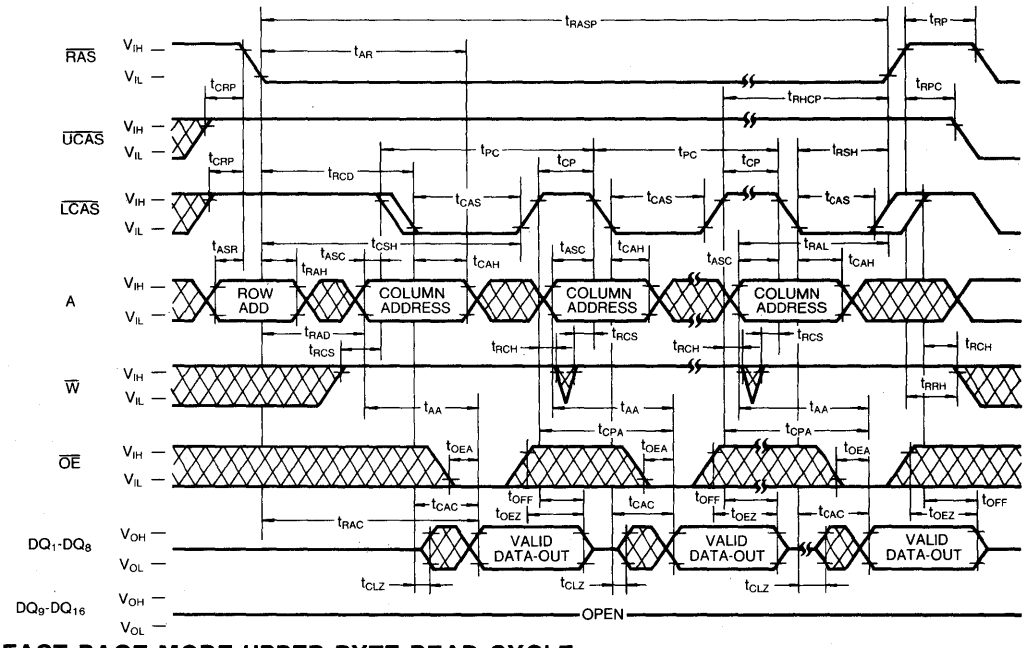


FAST PAGE MODE WORD READ CYCLE

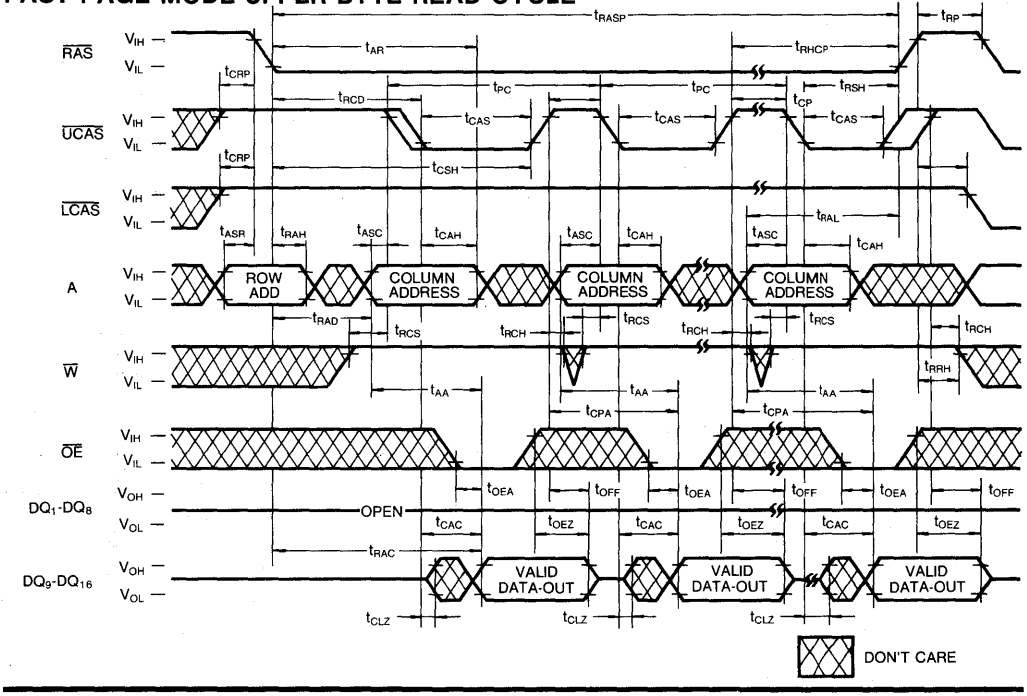


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE



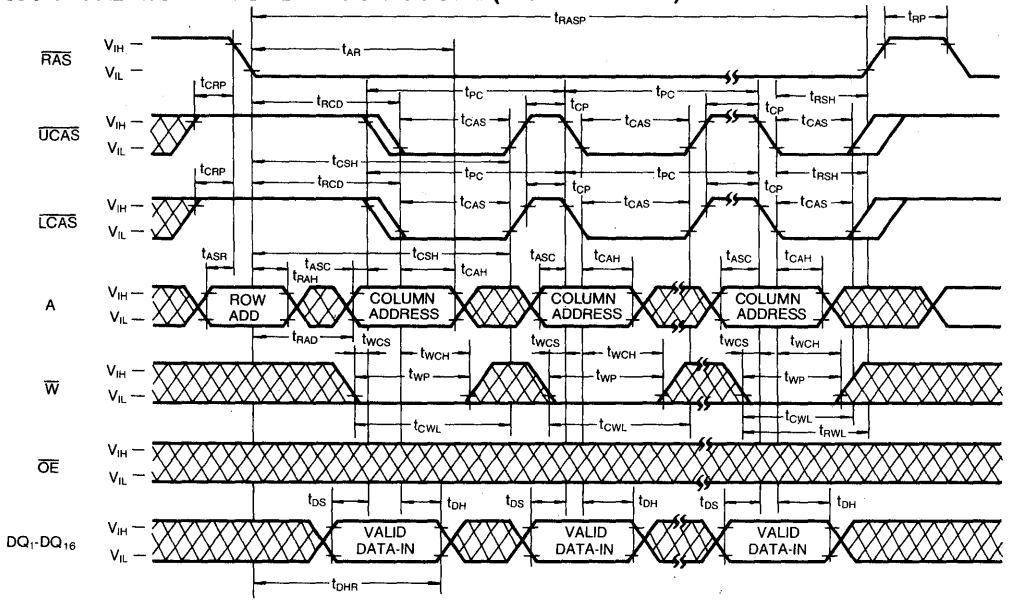
FAST PAGE MODE UPPER BYTE READ CYCLE



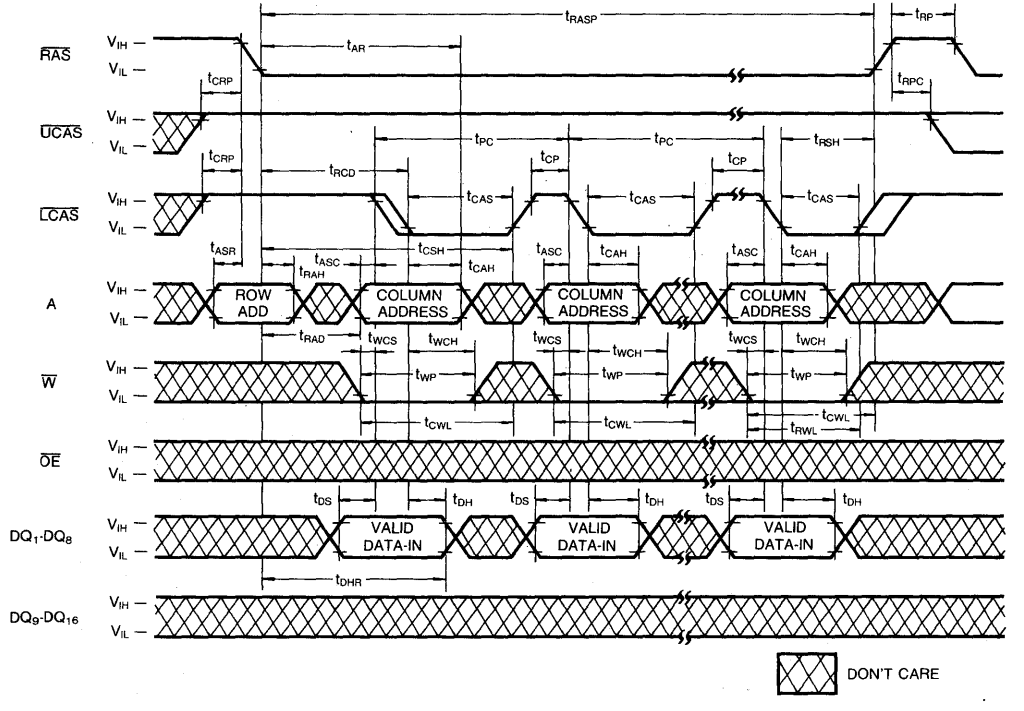
6

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

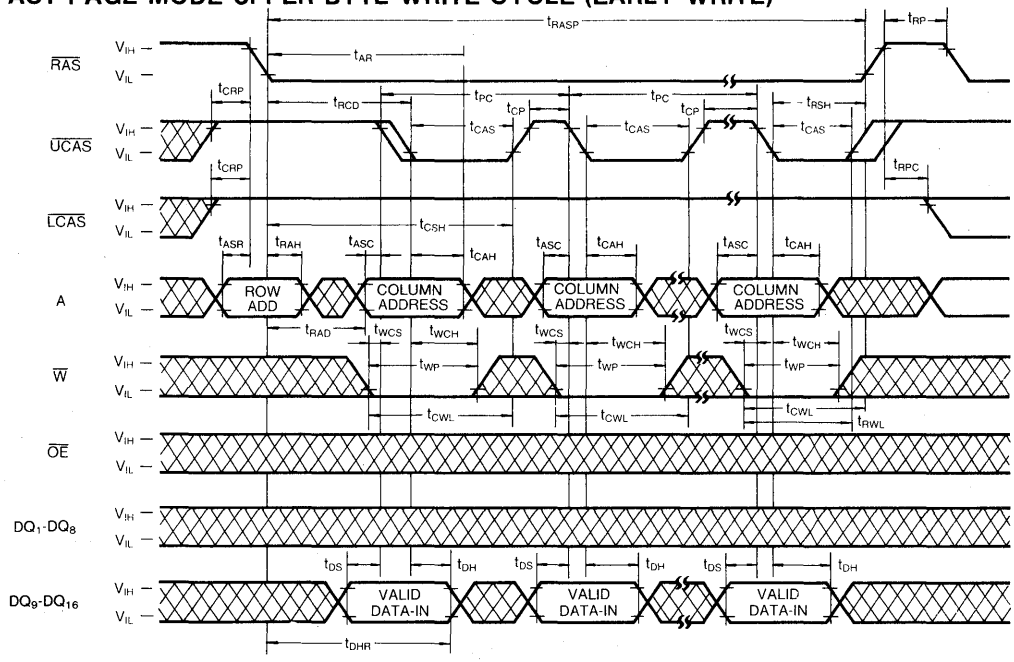


FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)

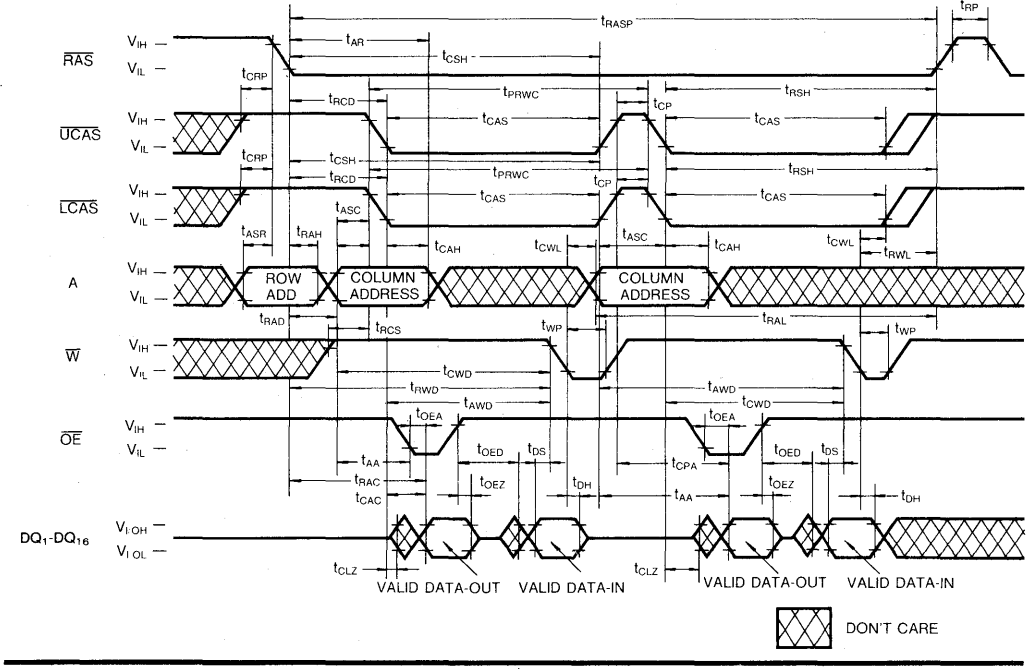


TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

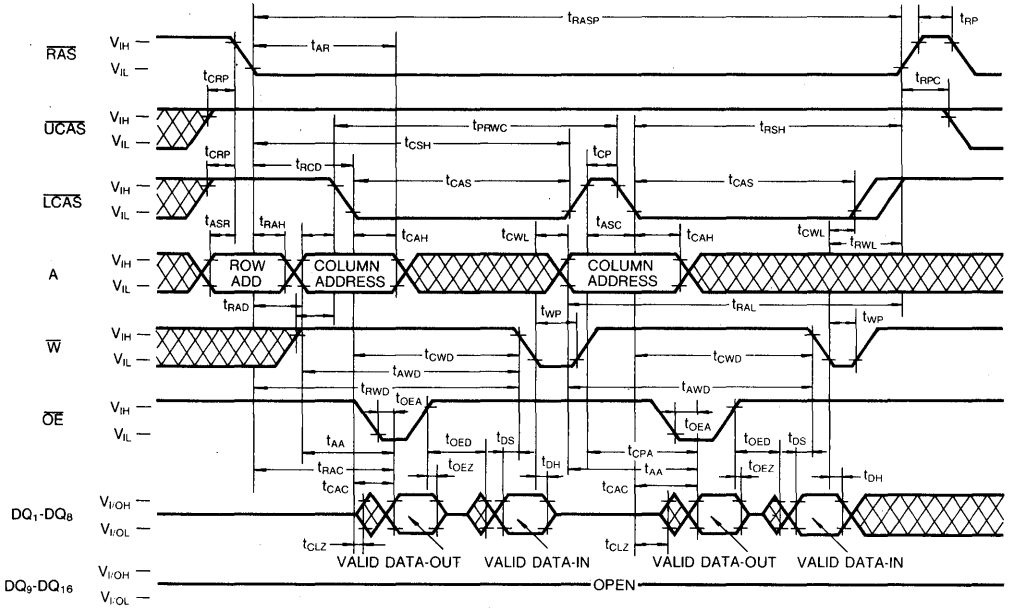


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

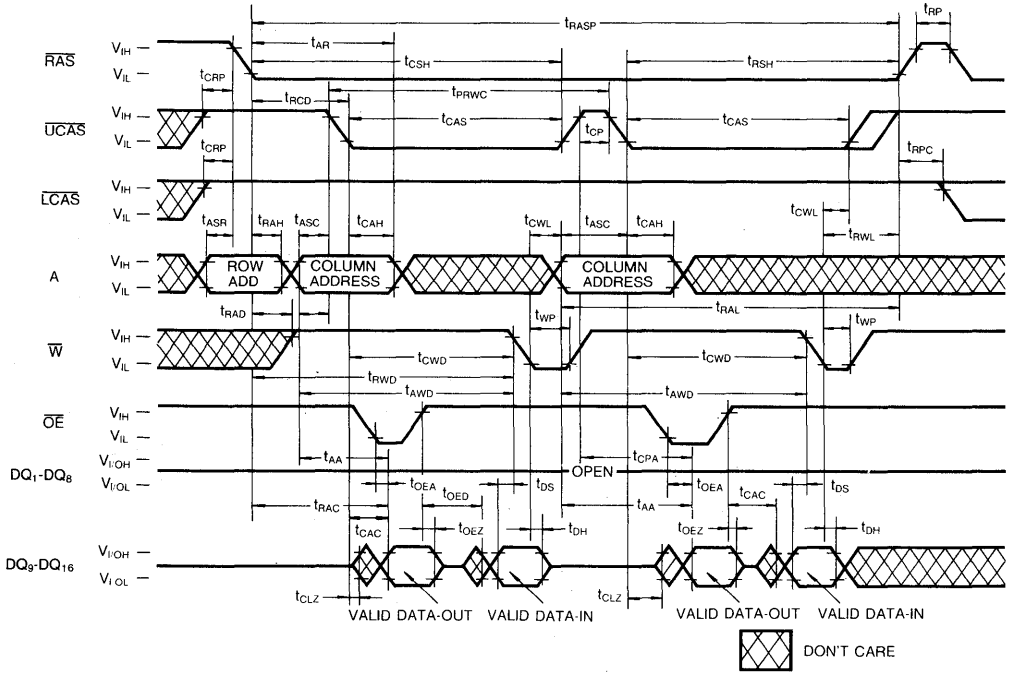


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



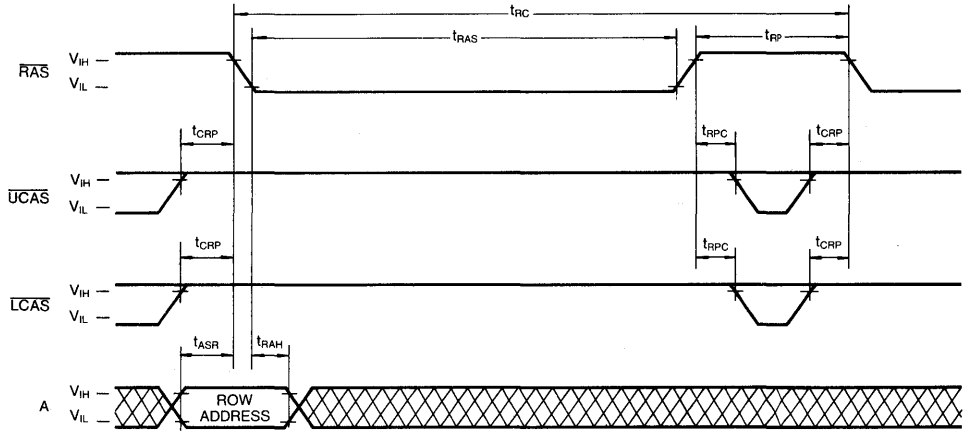
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



TIMING DIAGRAMS (Continued)

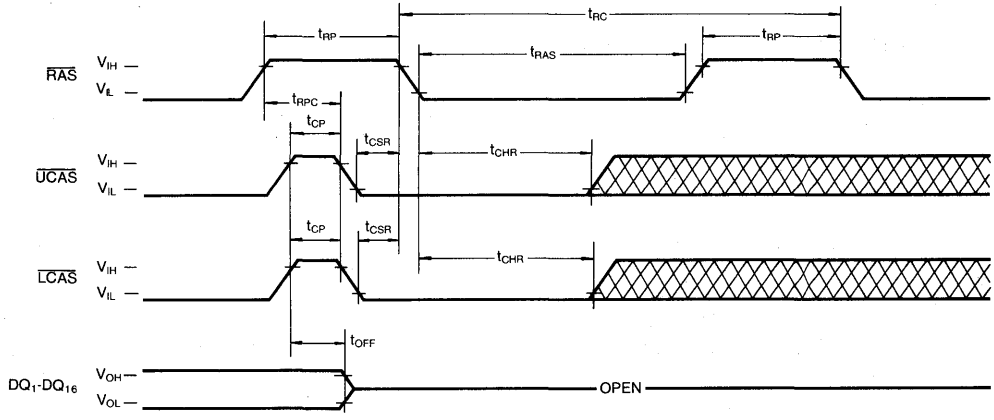
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care

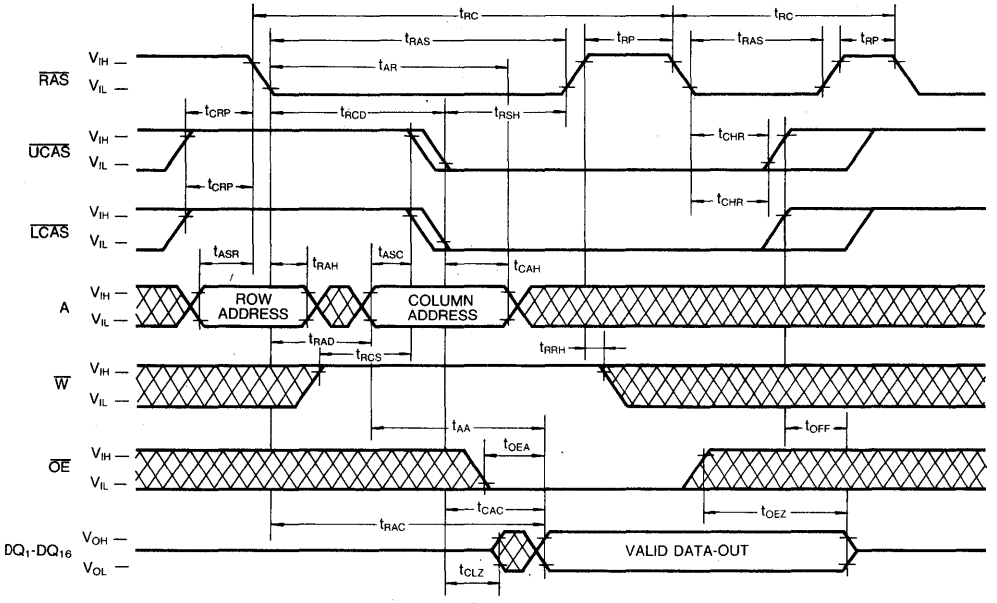


DON'T CARE

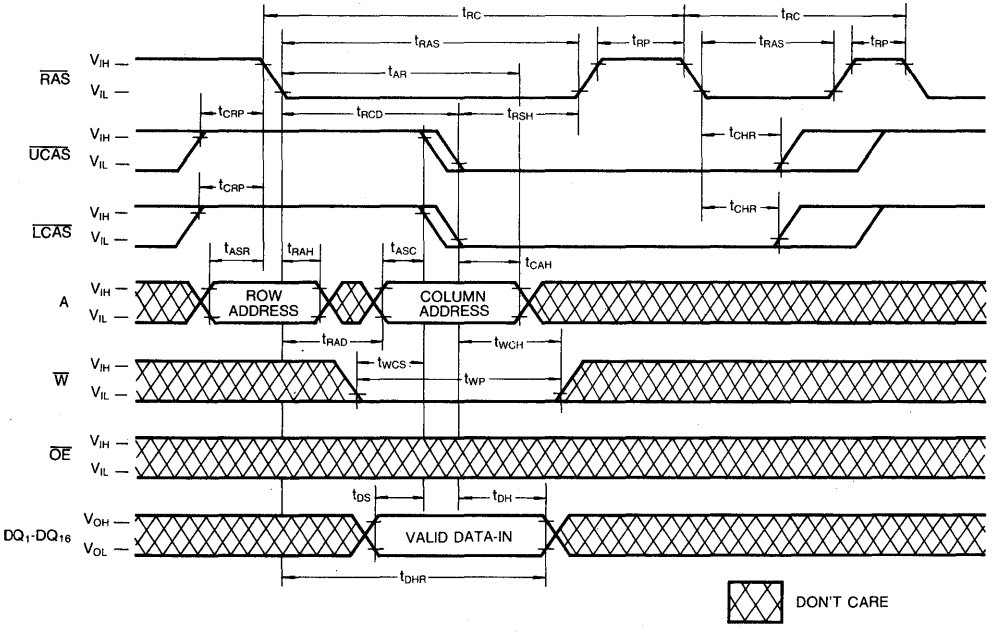
6

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

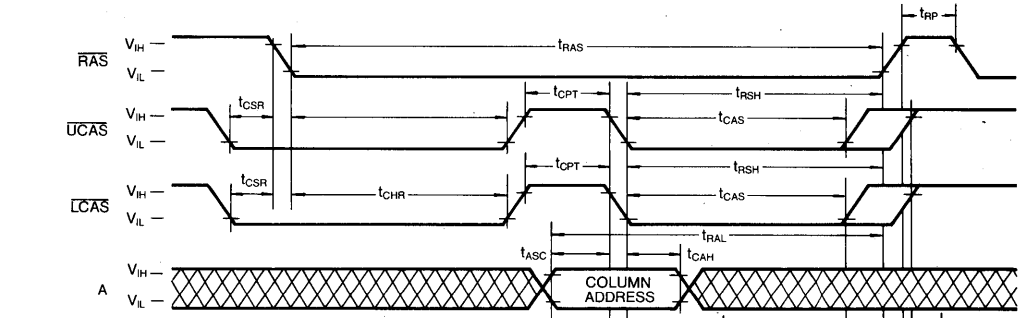


HIDDEN REFRESH CYCLE (WRITE)

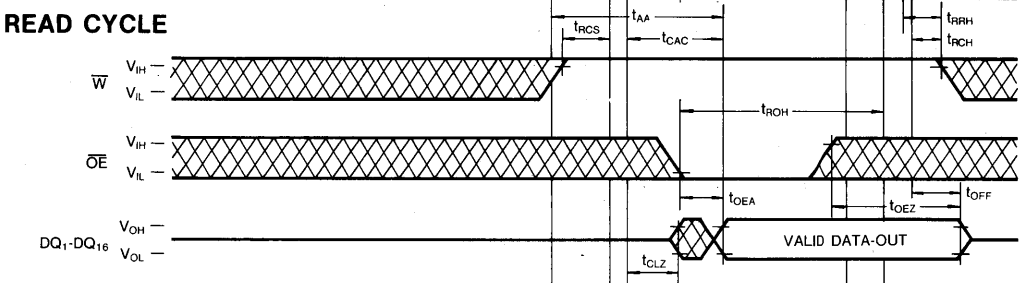


TIMING DIAGRAMS (Continued)

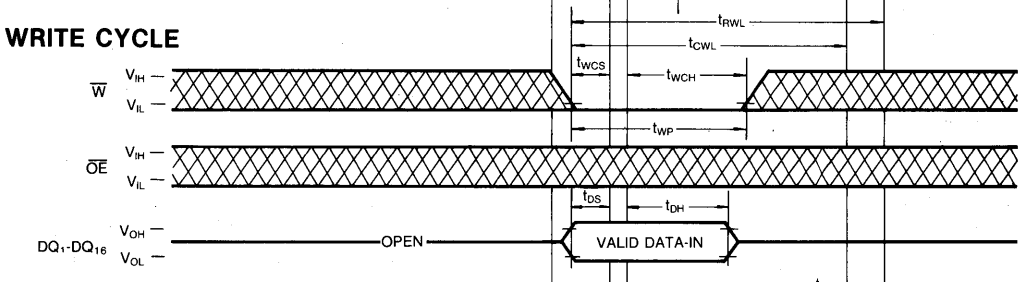
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



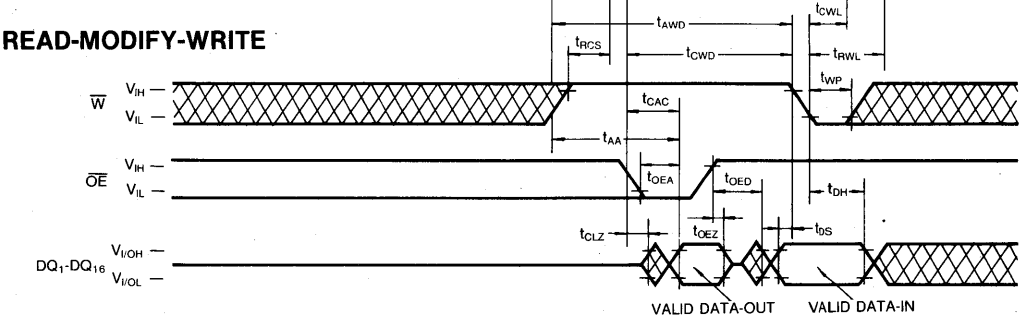
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE



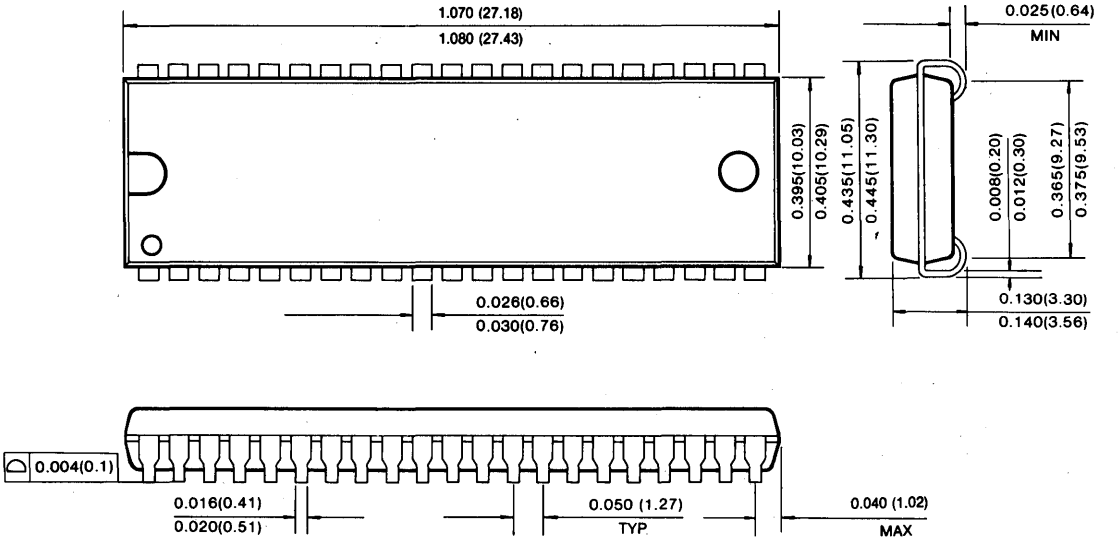
DON'T CARE

6

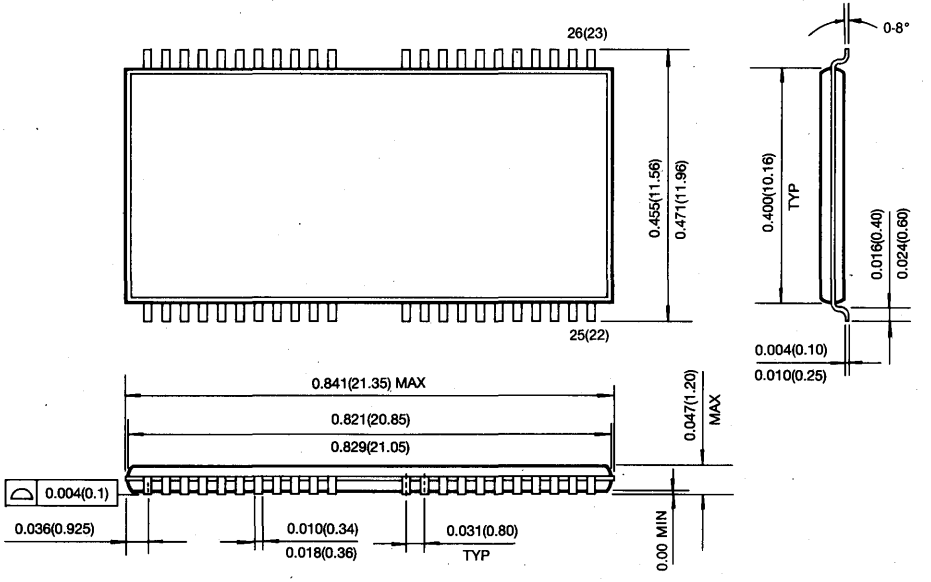
PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



1M x 16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM416V1004A-6/A-L6/A-F6	60ns	17ns	110ns	24ns
KM416V1004A-7/A-L7/A-F7	70ns	20ns	130ns	29ns
KM416V1004A-8/A-L8/A-F8	80ns	20ns	150ns	34ns

- **Extended Data Out Mode (Fast Page Mode with Extended Data Out)**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +3.3V±0.3V power supply**
- **Refresh Cycle**
  - **4096 cycle/64ms (Normal)**
  - **4096 cycle/128ms (L-version)**
  - **4096 cycle/128ms (F-version)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

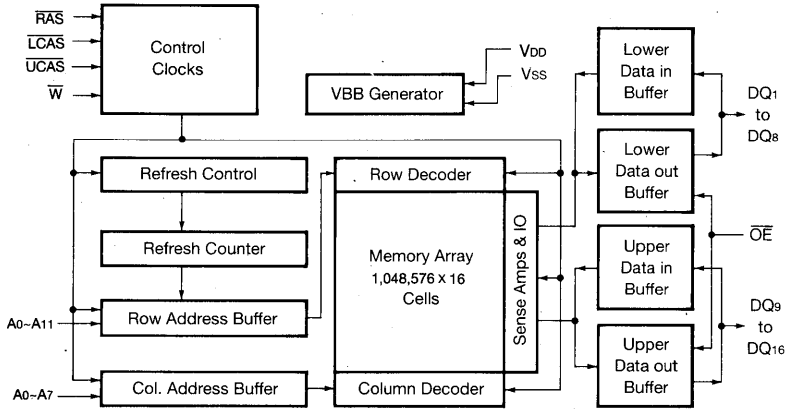
GENERAL DESCRIPTION

The Samsung KM416V1004A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

The KM416V1004A/A-L/A-F features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416V1004A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

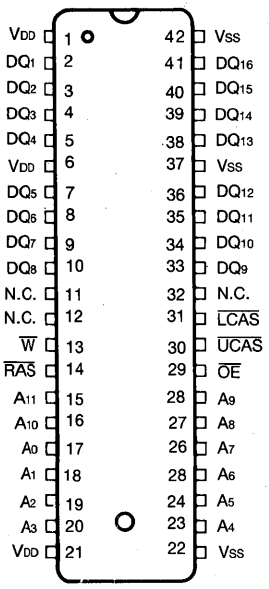
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

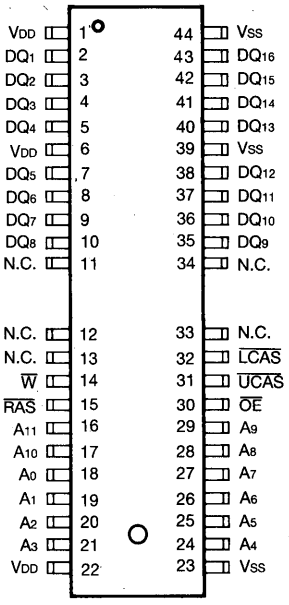
PIN CONFIGURATION (Top Views)

• KM416V1004AJ



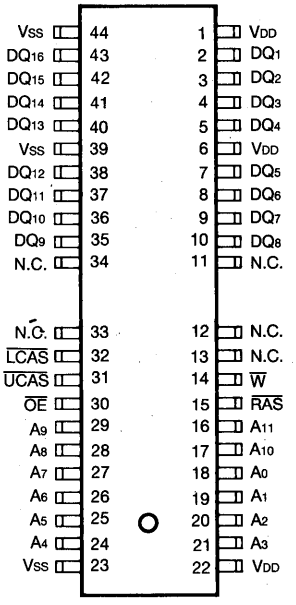
(SOJ)

• KM416V1004AT



(TSOP(II)-Forword)

• KM416V1004AR



(TSOP(II)-Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-16	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VDD	Power(+3.3V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 to 4.6	V
Storage Temperature	T_{stg}	-55 to+150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.1	—	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{RC}=min.)	KM416V1004A-6/A-L6/A-F6 KM416V1004A-7/A-L7/A-F7 KM416V1004A-8/A-L8/A-F8	I_{CC1}	-	90 80 70	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})	KM416V1004A KM416V1004AL KM416V1004ALL	I_{CC2}	-	2 1 1	mA mA mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM416V1004A-6/A-L6/A-F6 KM416V1004A-7/A-L7/A-F7 KM416V1004A-8/A-L8/A-F8	I_{CC3}	-	90 80 70	mA mA mA
EDO Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC}=min.)	KM416V1004A-6/A-L6/A-F6 KM416V1004A-7/A-L7/A-F7 KM416V1004A-8/A-L8/A-F8	I_{CC4}	-	110 100 90	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{DD}-0.2V)	KM416V1004A KM416V1004AL KM416V1004ALL	I_{CC5}	-	1 300 200	mA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC}=min.)	KM416V1004A-6/A-L6/A-F6 KM416V1004A-7/A-L7/A-F7 KM416V1004A-8/A-L8/A-F8	I_{CC6}	-	90 80 70	mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V_{IH})=V_{DD}-0.2V, Input Low Voltage(V_{IL})=0.2V $\overline{UCAS}$, $\overline{LCAS}$=0.2V D_{IN}=Don't Care, t_{RC}=31.25μs (L-Version) t_{RAS}=t_{RAS} min~300ns	KM416V1004A-L	I_{CC7}	-	450	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{DD}-0.2V or 0.2V DQ_1-DQ_{16}=V_{DD}-0.2V or 0.2V or Open	KM416V1004A-F	I_{CCS}	-	250	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{DD}+0.3V, all other pins not under test=0 V)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{DD})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once while one Hyper page mode cycle time t_{HPC}.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V. f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~$_{11}$)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

(Test condition : V_{IH}/V_{IL}=2.1V/0.8V, V_{OH}/V_{OL}=2.0V/0.8V, Output Loading C_L=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		17		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	17		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	15	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	15
Column address hold time	tCAH	10		15		15		ns	15
Column address hold time referenced to $\overline{RAS}$	tAR	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	10		15		20		ns	18
Data-in set-up time	tDS	0		0		0		ns	10,21
Data-in hold time	tDH	10		15		15		ns	10,21
Data-in hold time referenced to $\overline{RAS}$	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		50		50		ns	8,17
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	20
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		25		30		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	15		20		20		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	7
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Hyper Page mode cycle time	t_{HPC}	24		29		34		ns	12
Hyper Page mode read-modify-write cycle time	t_{HPRWC}	76		81		91		ns	12
$\overline{CAS}$ precharge time (Hyper page mode)	t_{CP}	10		10		10		ns	16
$\overline{RAS}$ pulse width (Hyper Page mode)	t_{RASP}	60		70		80		ns	
$\overline{RAS}$ hold time from CAS precharge	t_{RHCP}	35		40		45		ns	
Output data hold time	t_{DOH}	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	15	3	20	3	20	ns	7
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		5		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		5		ns	
$\overline{W}$ to data delay	t_{WED}	15		20		20		ns	
$\overline{RAS}$ pulse width (F-ver)	t_{RASS}	100		100		100		μs	13
$\overline{RAS}$ precharge time (F-ver)	t_{RPS}	110		130		150		ns	13
$\overline{CAS}$ hlod time (F-ver)	t_{CHS}	-50		-50		-50		ns	13

KM416V1004A/A-L/A-F Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ_1~DQ_8	DQ_9~DQ_{16}	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

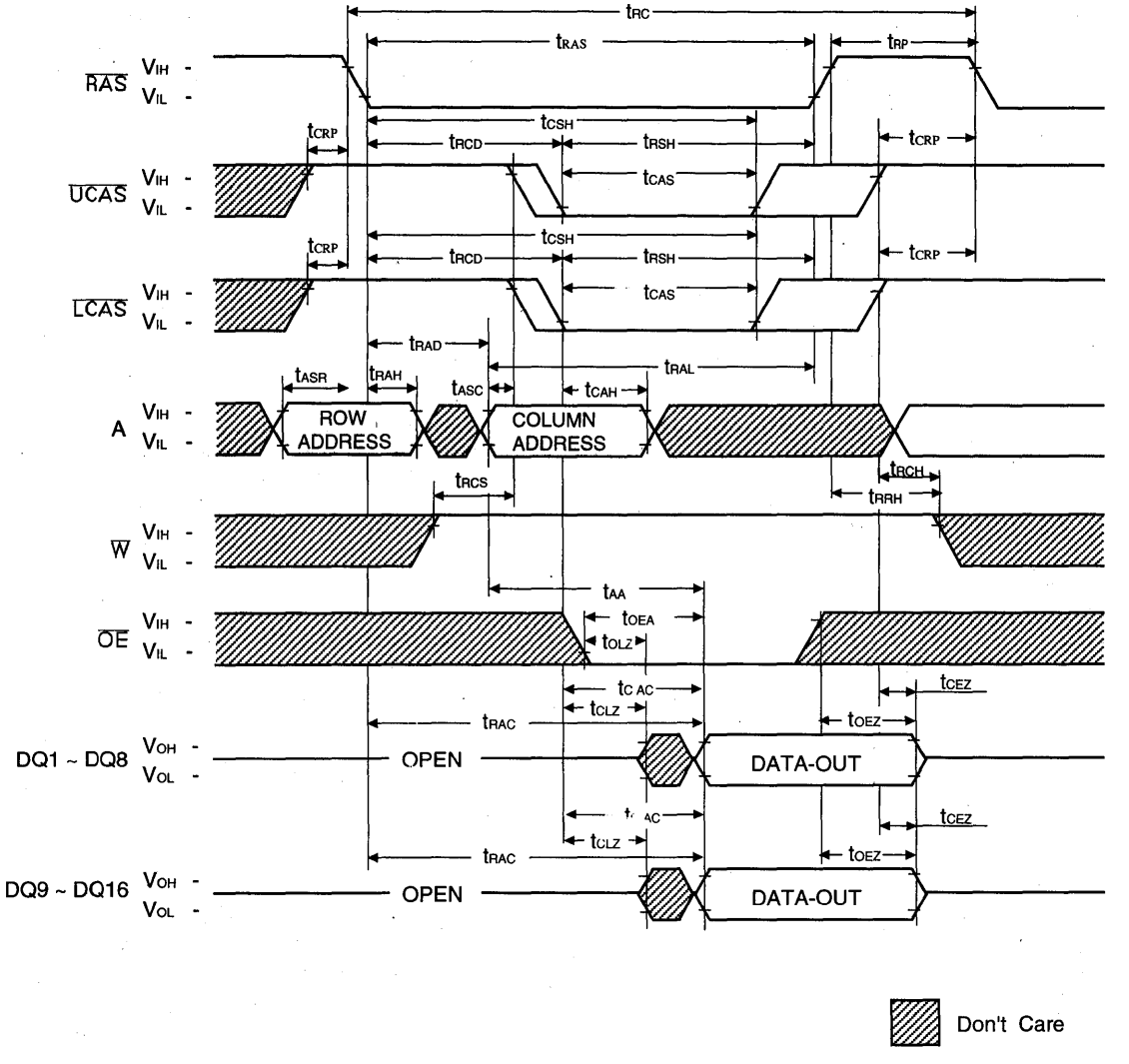
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL Loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. $t_{ASC} \geq t_{CP}$ min, Assume t_T=2.0ns.
13. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (F-version)
14. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
16. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
17. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
18. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
19. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
20. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.
21. t_{DS}, t_{DH} is independetly specified for lower byte D_{in} ($_{1\sim8}$), upper byte D_{in}($_{9\sim16}$)

TIMING DIAGRAM

WORD READ CYCLE

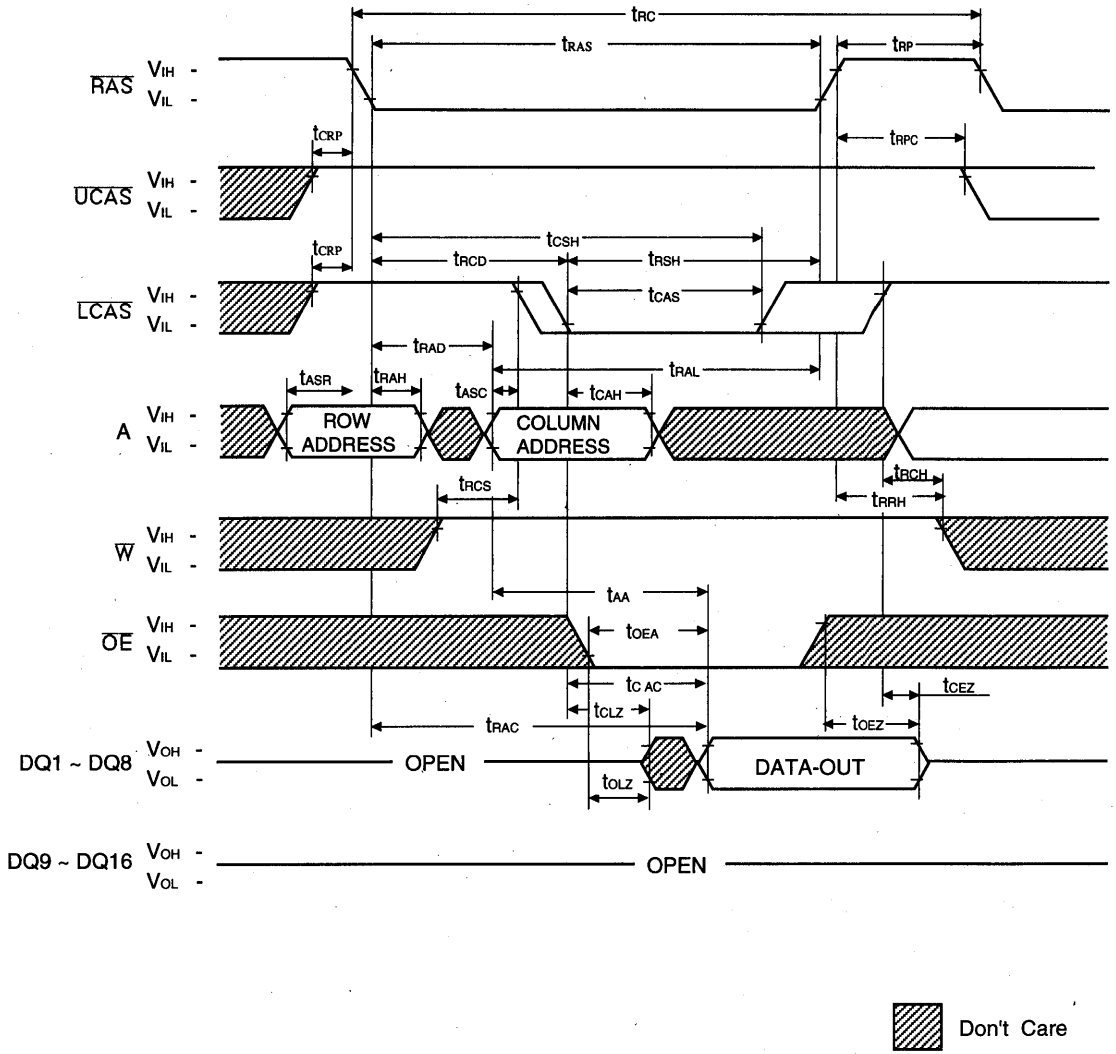
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

LOWER BYTE READ CYCLE

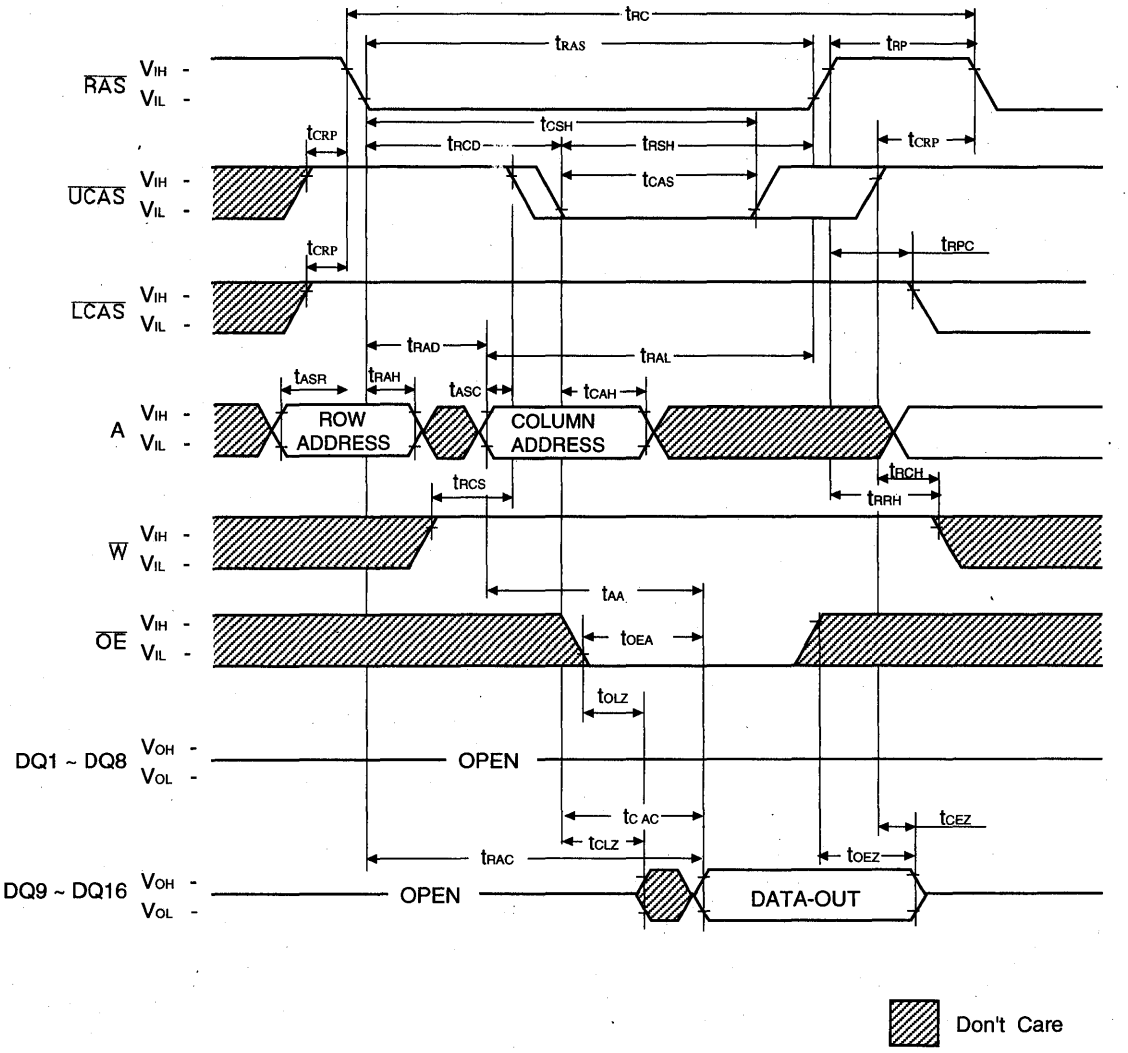
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

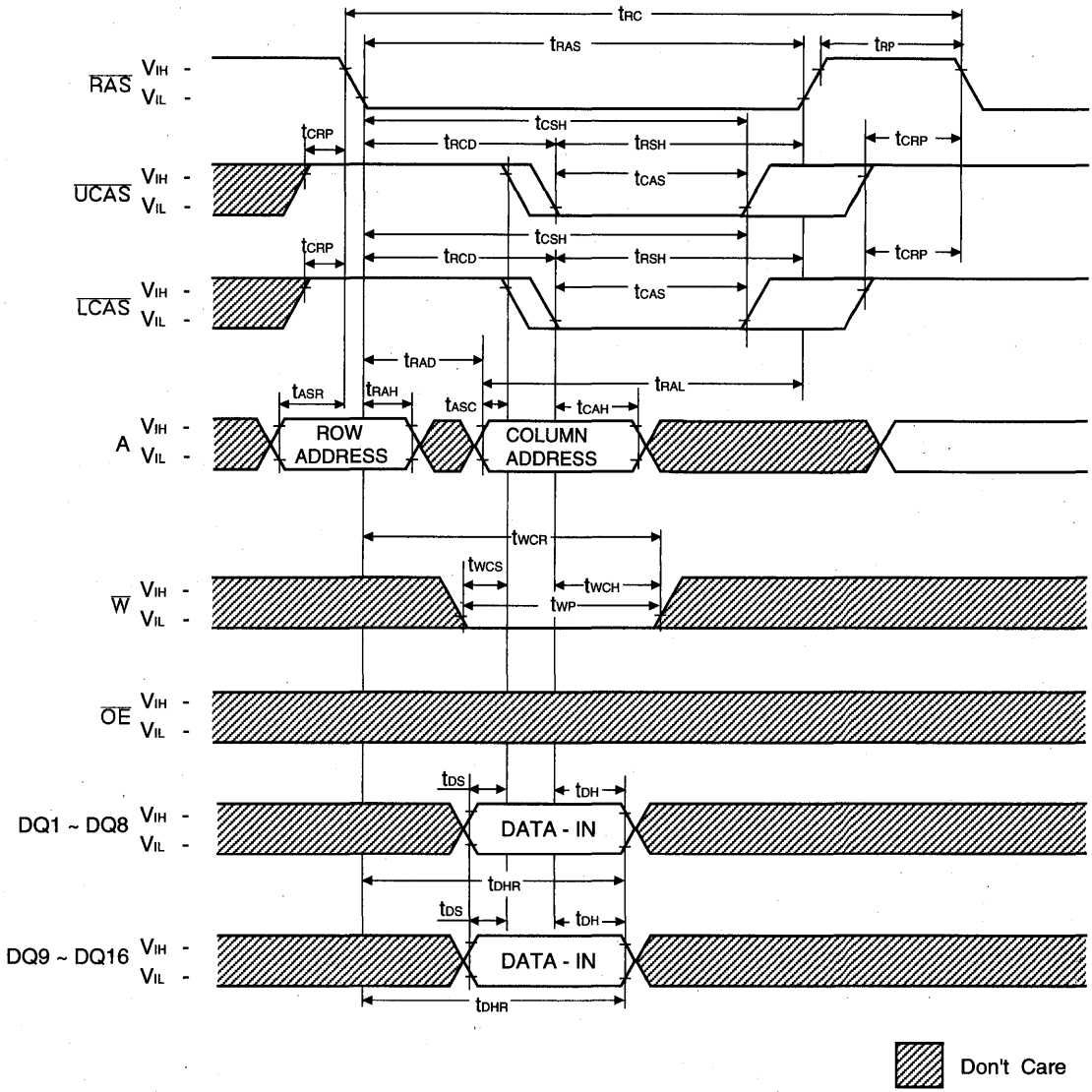
UPPER BYTE READ CYCLE

NOTE : D_{IN} = OPEN



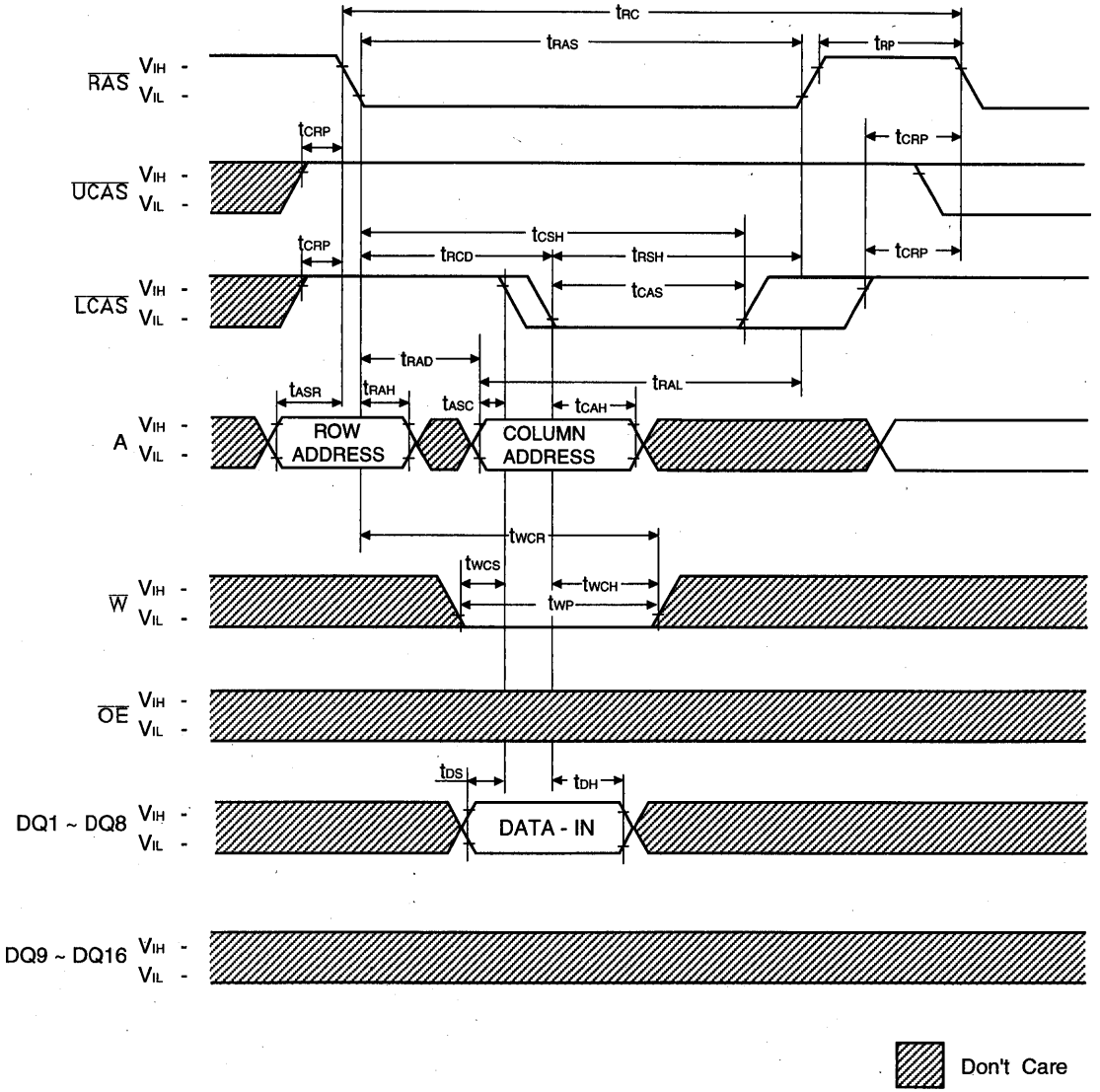
WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



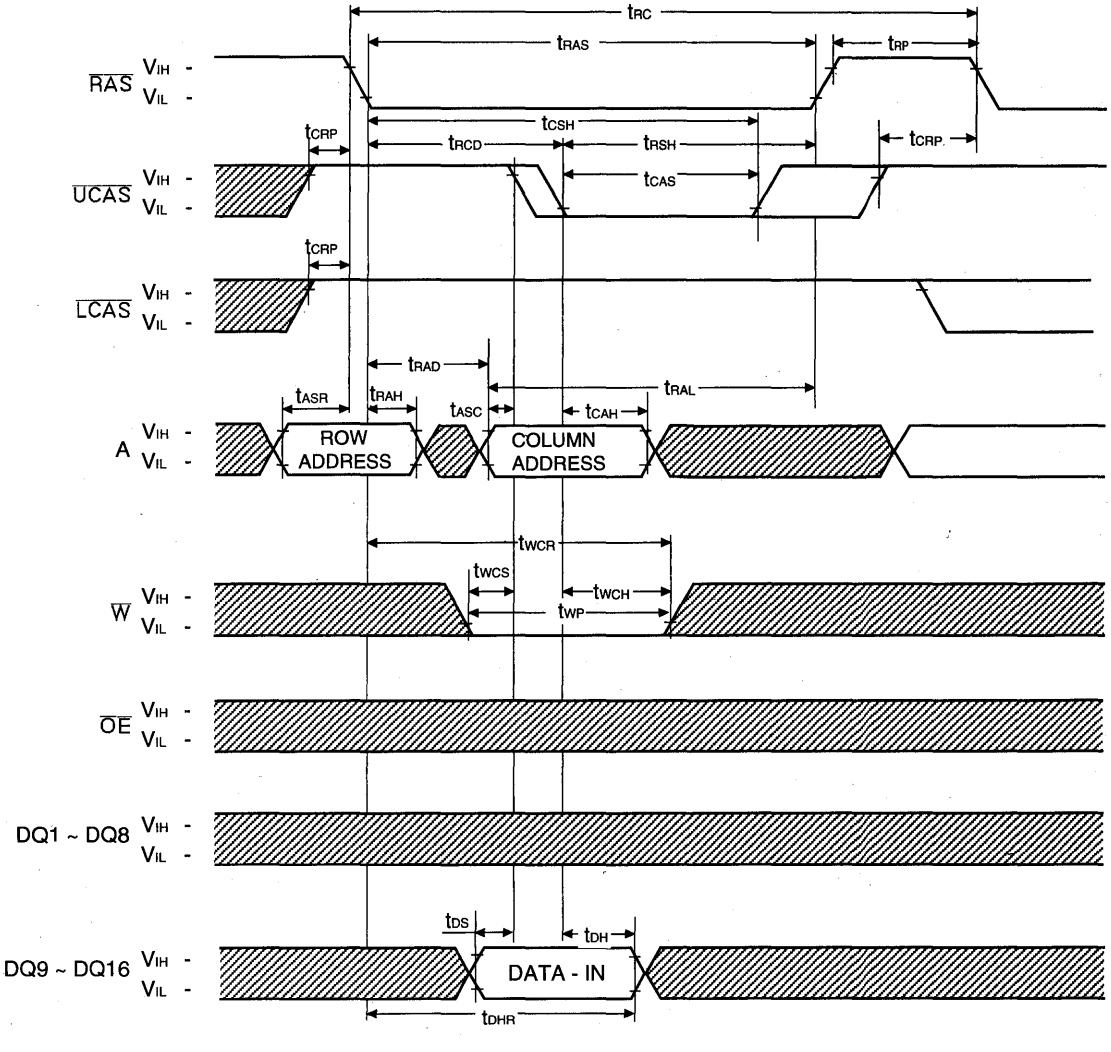
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



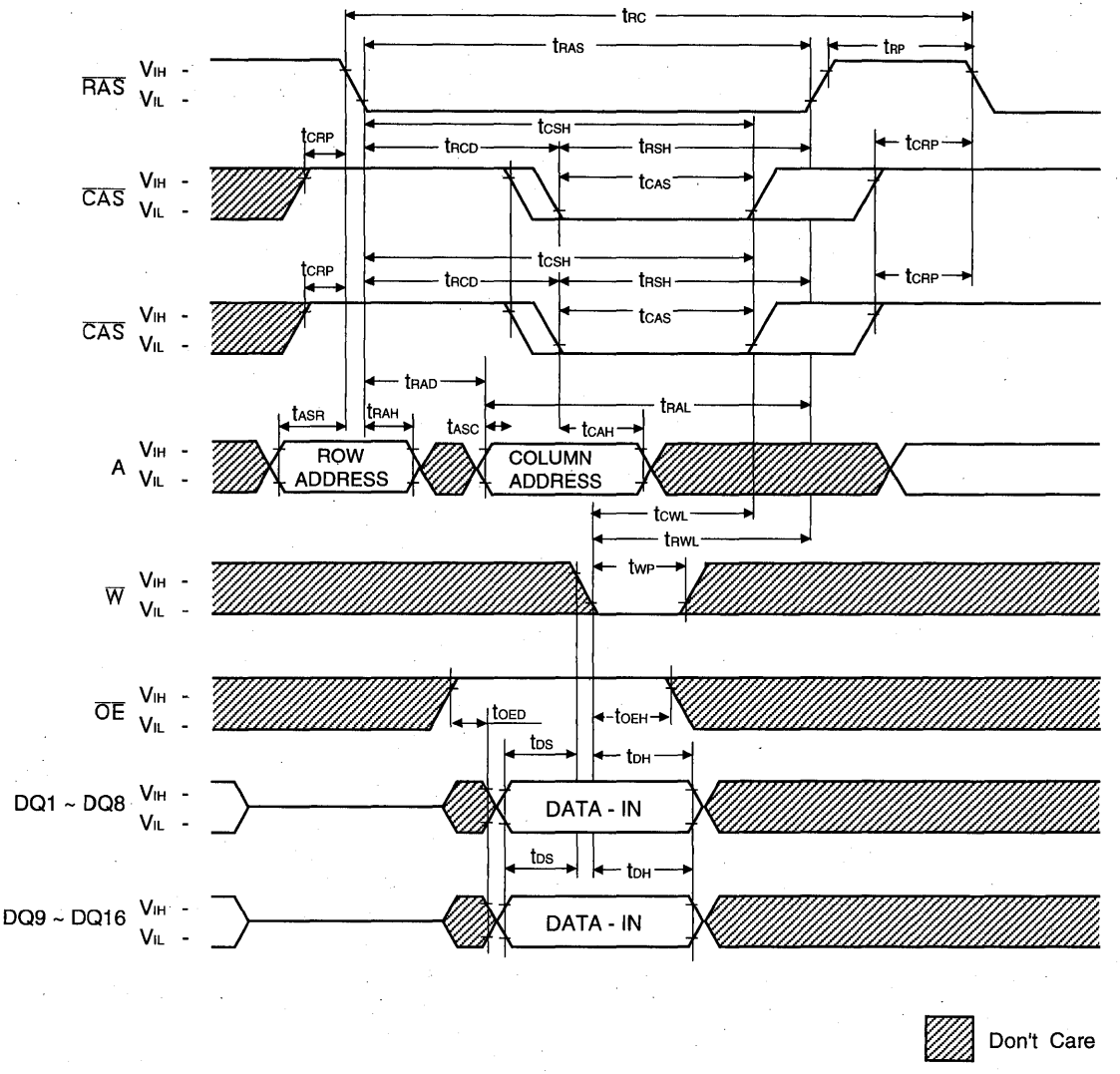
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



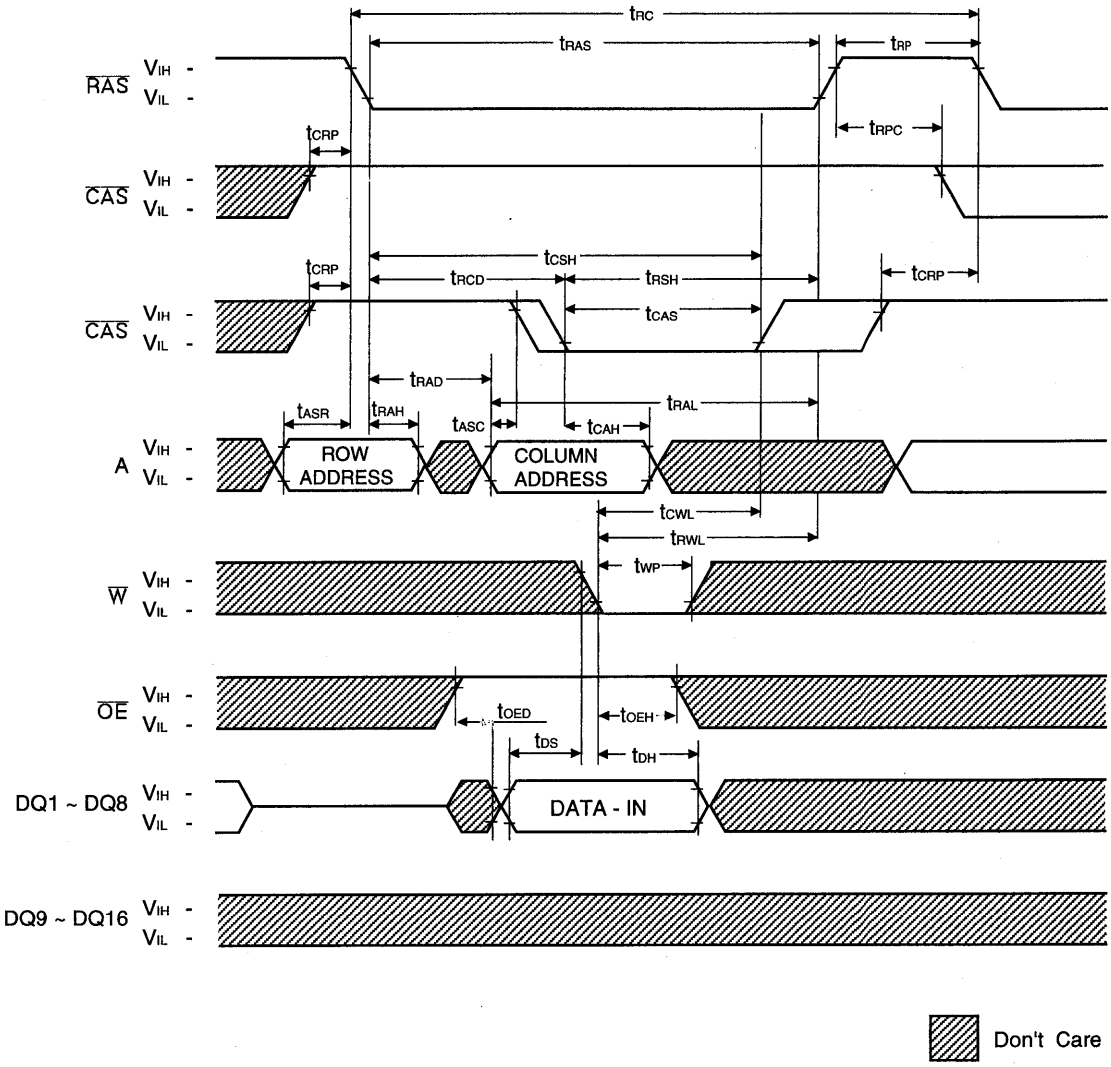
WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



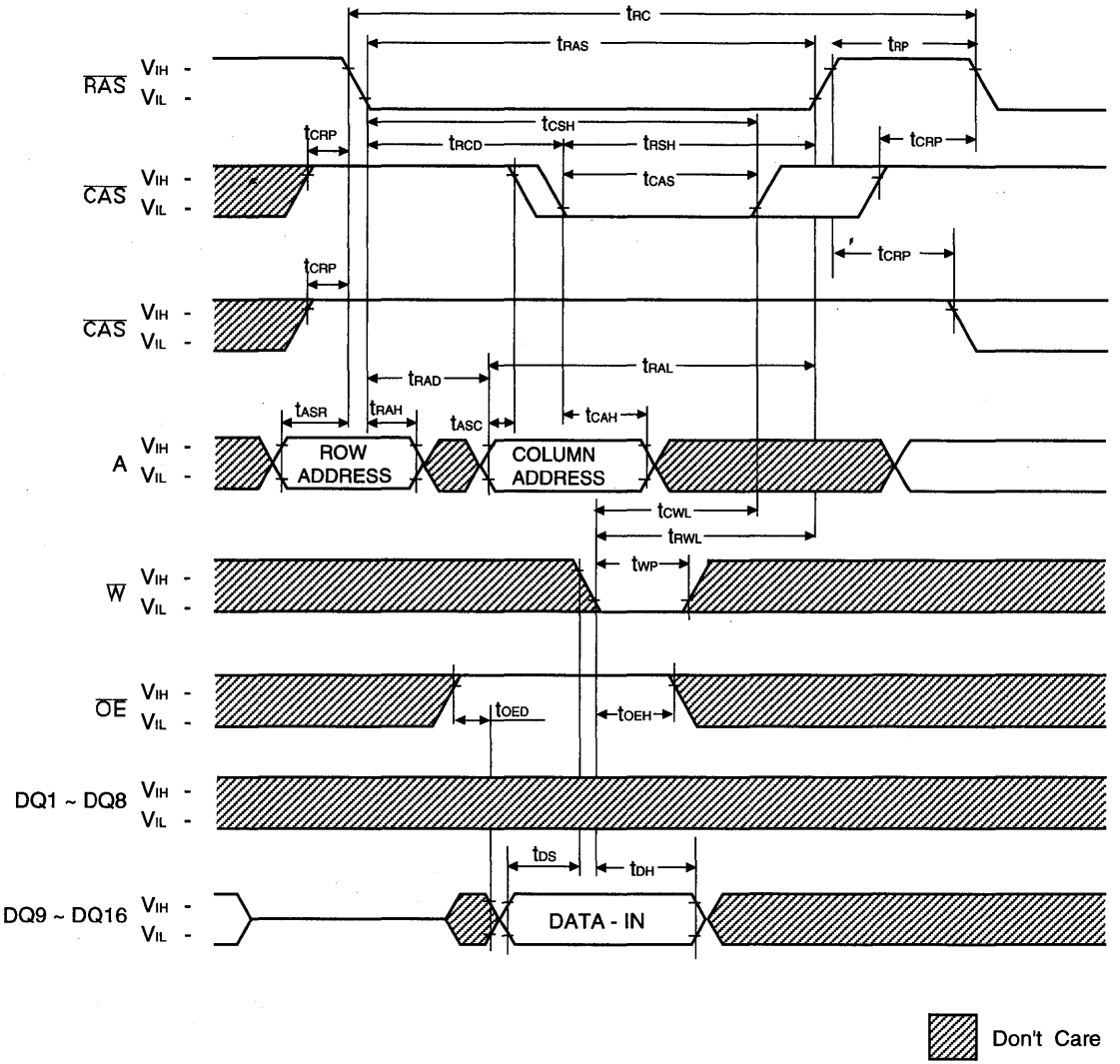
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

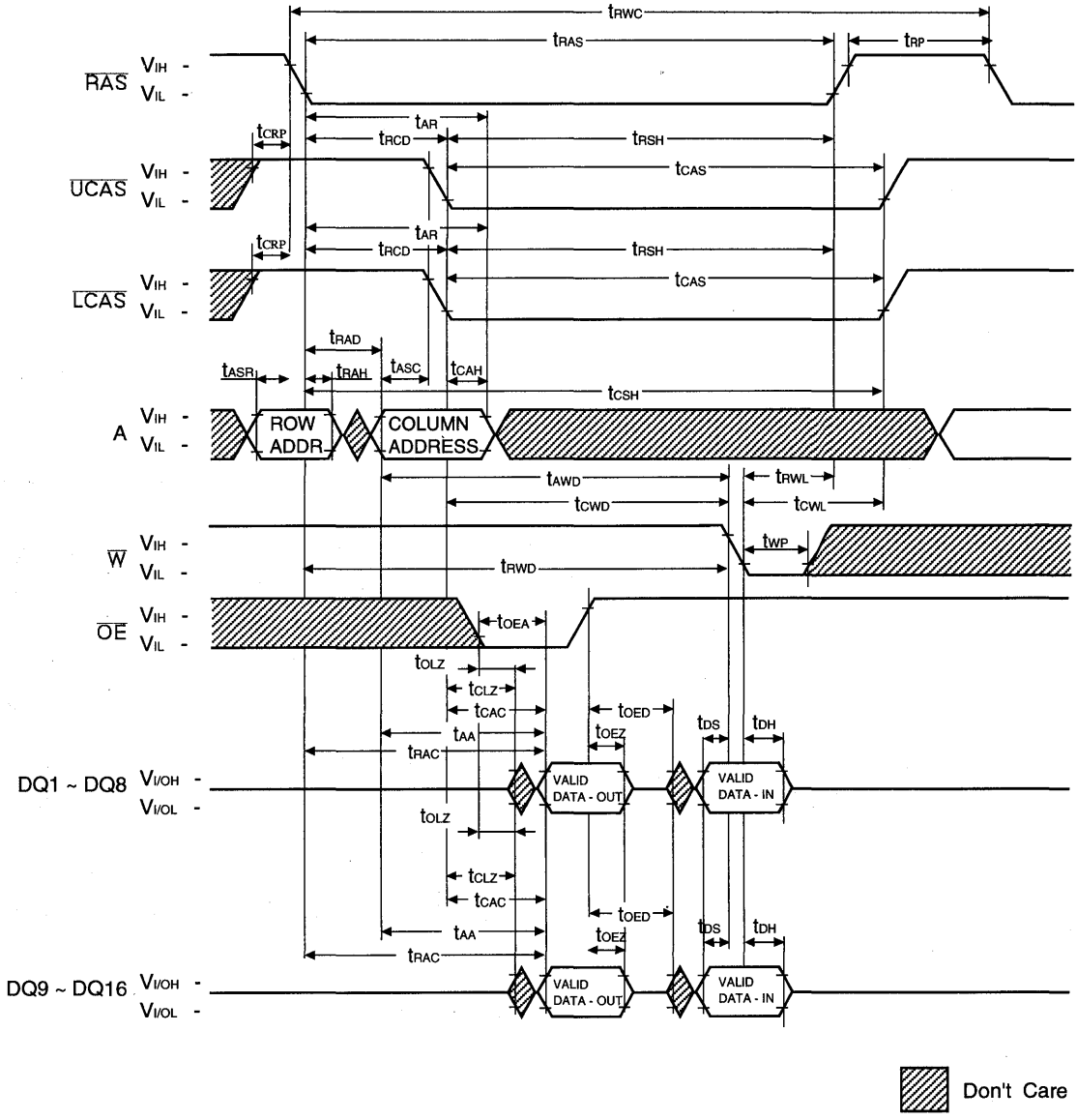


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

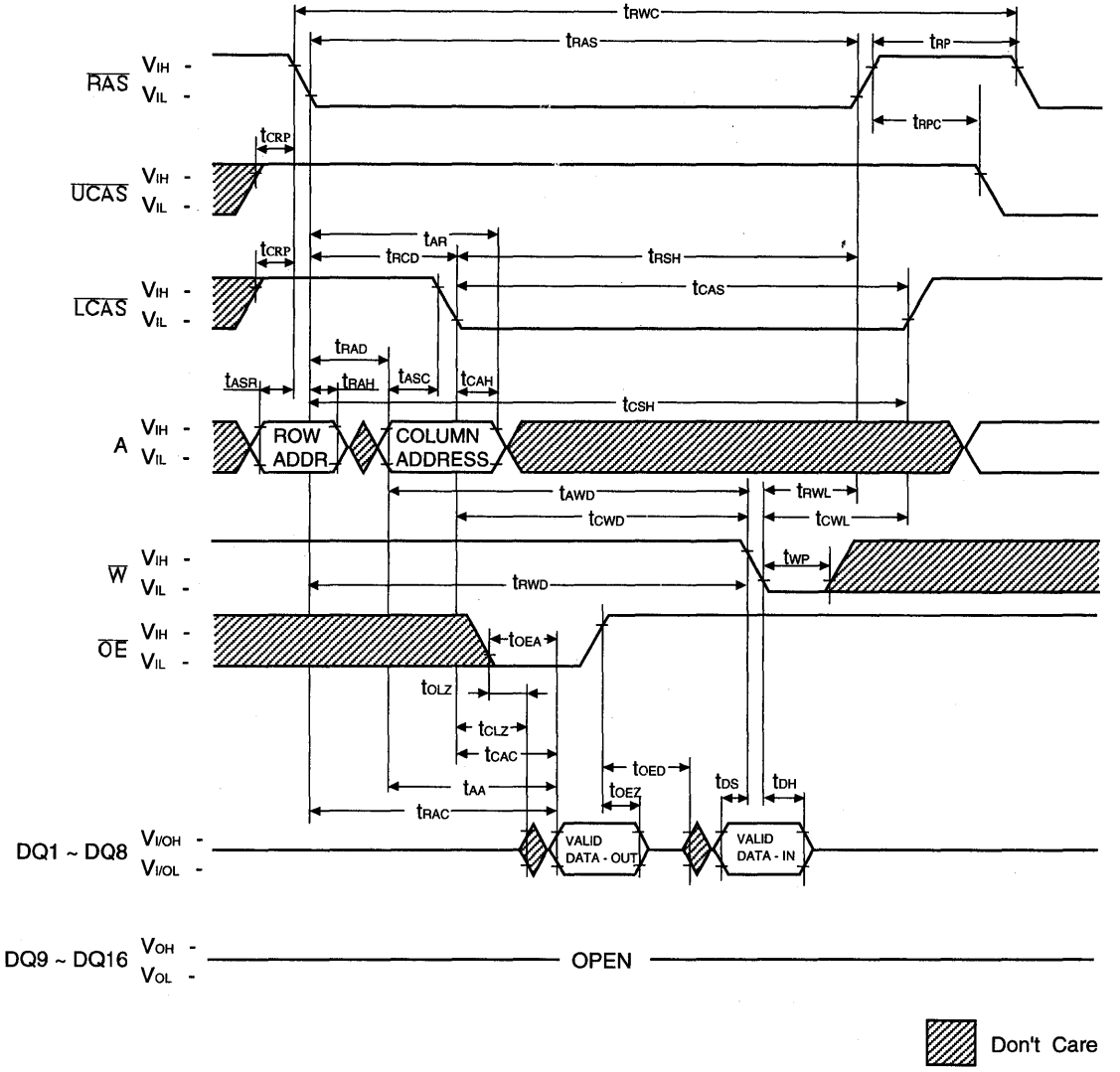
NOTE : D_{OUT} = OPEN



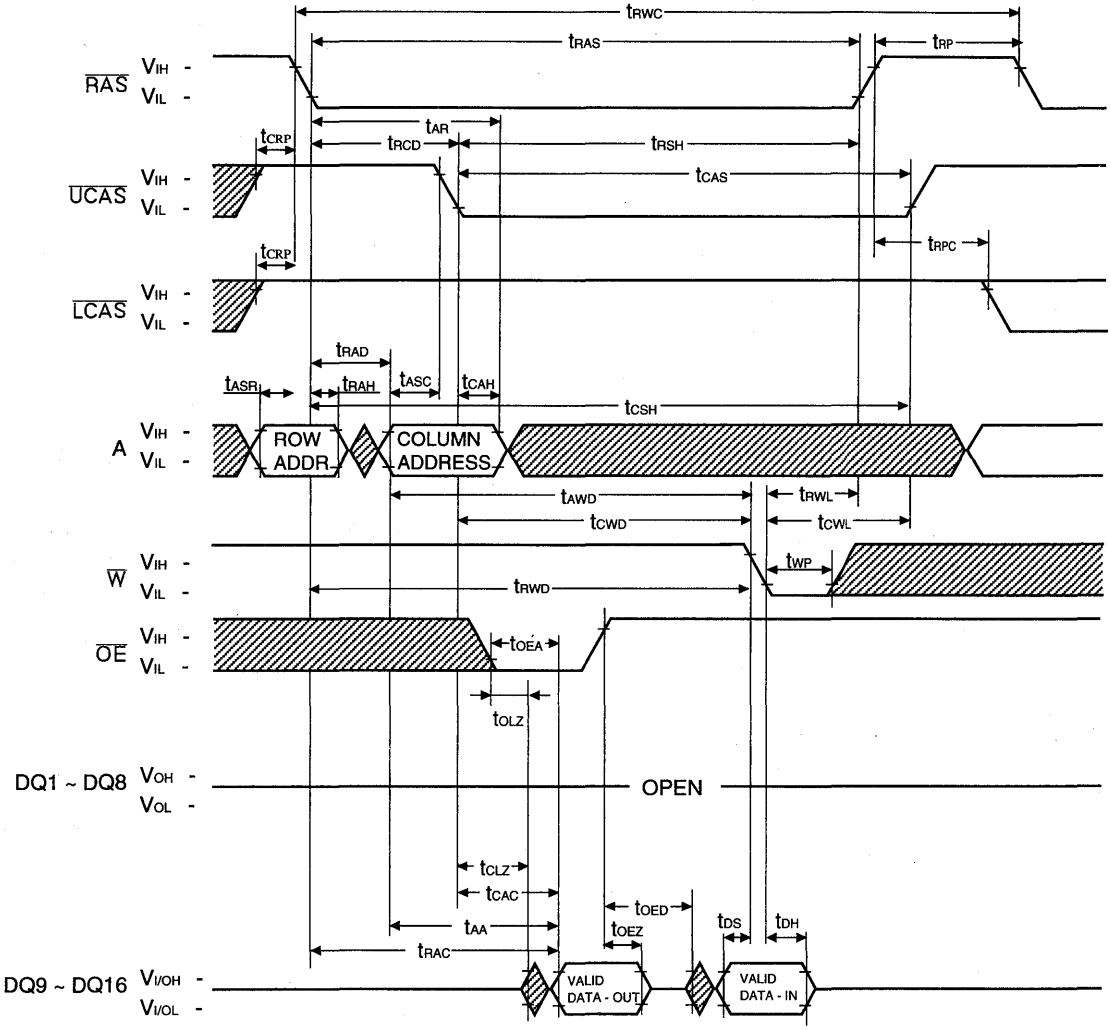
WORD READ - MODIFY - WRITE CYCLE



LOWER-BYTE READ - MODIFY - WRITE CYCLE

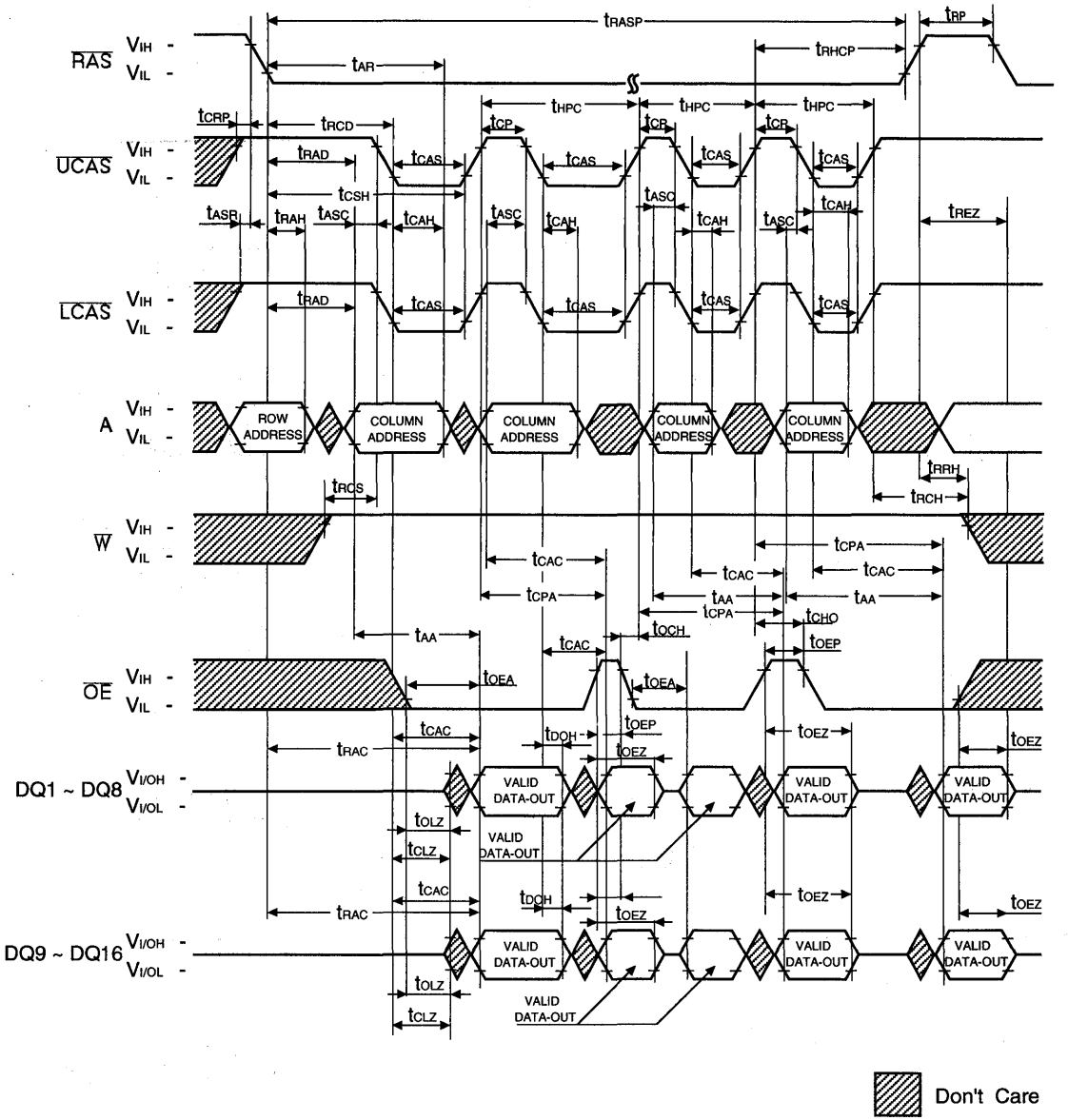


UPPER-BYTE READ - MODIFY - WRITE CYCLE

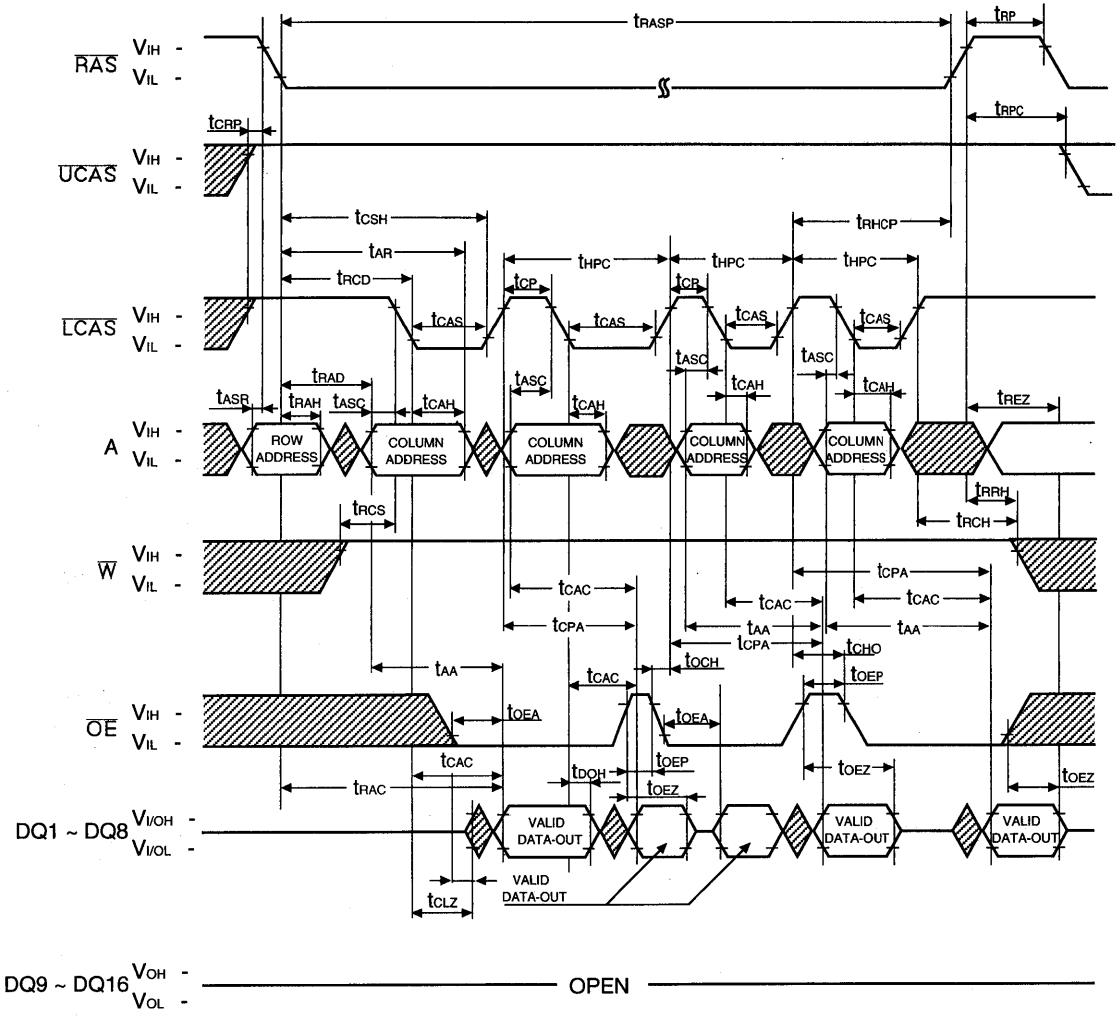


SAMSUNG ELECTRONICS

HYPER PAGE MODE WORD READ CYCLE

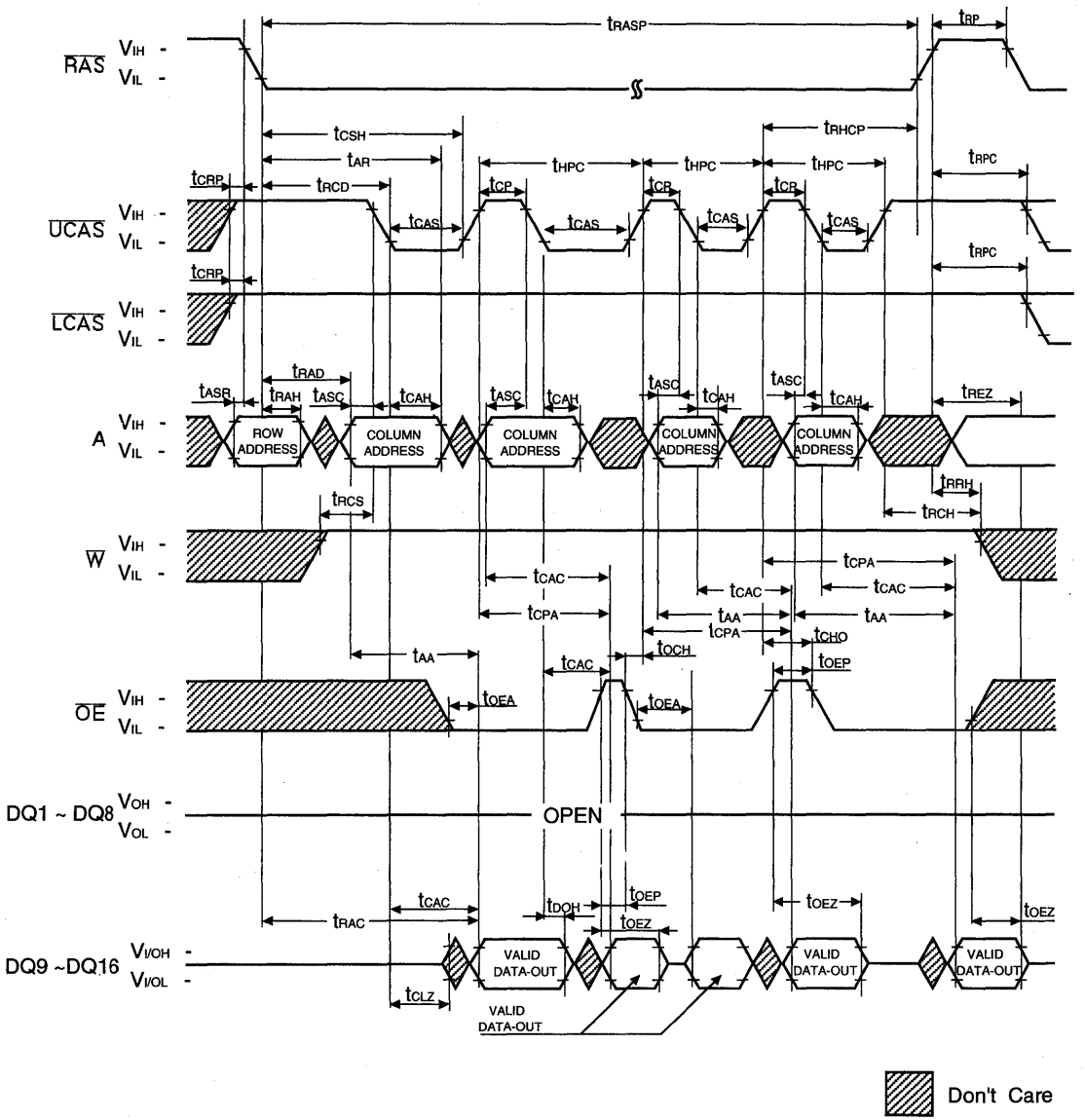


HYPER PAGE MODE LOWER BYTE READ CYCLE



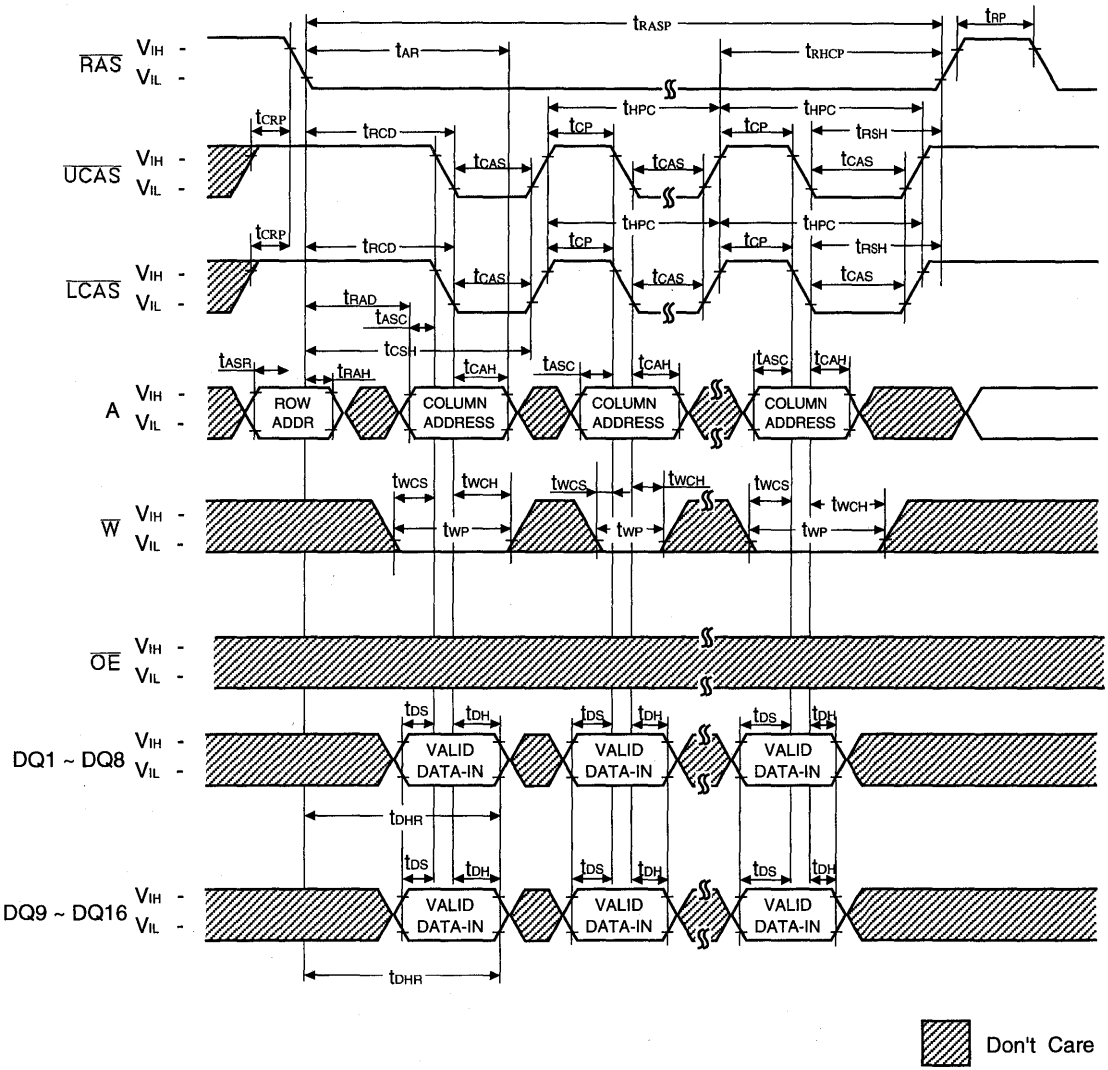
SAMSUNG ELECTRONICS

HYPER PAGE MODE UPPER BYTE READ CYCLE



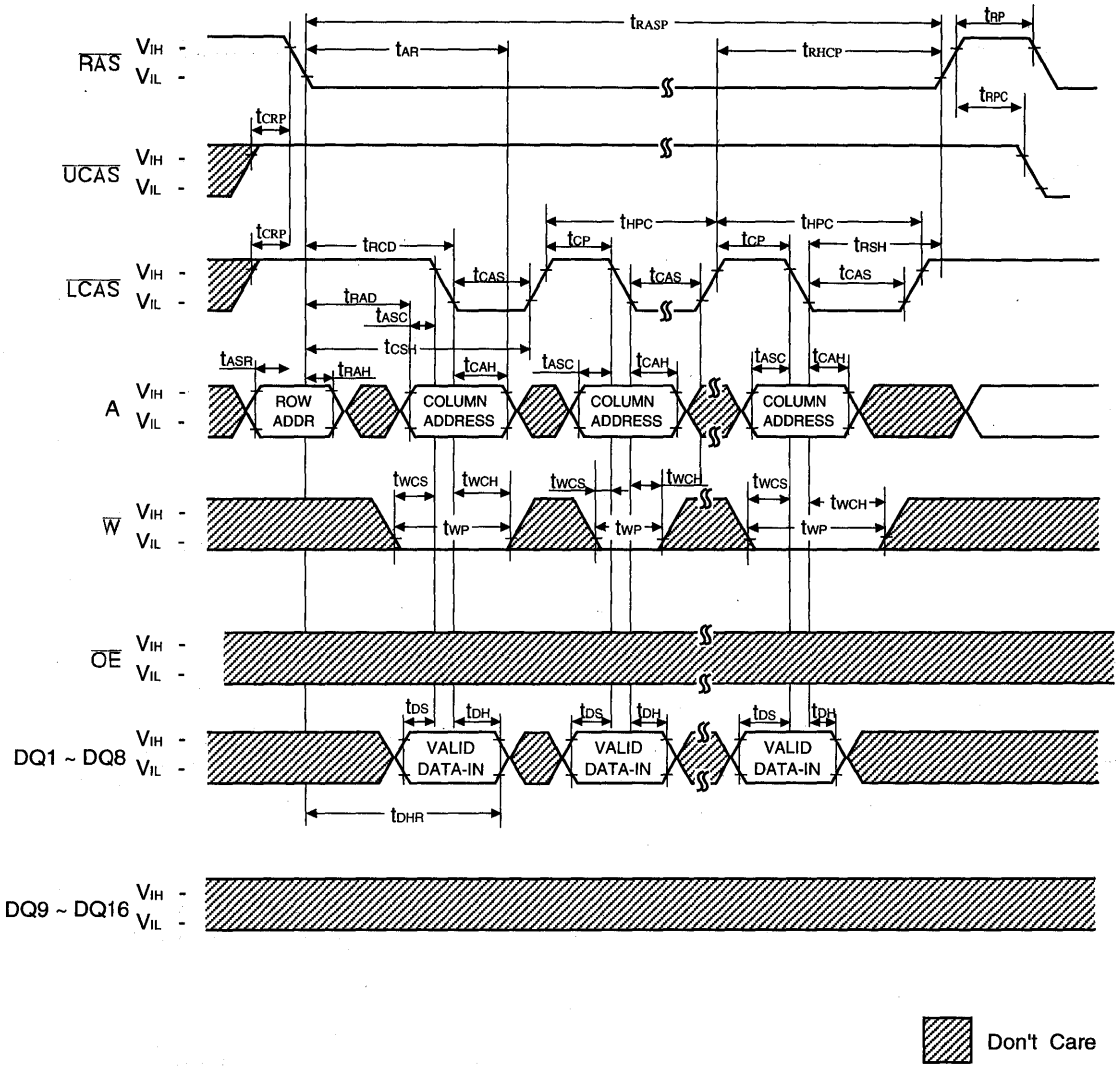
HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



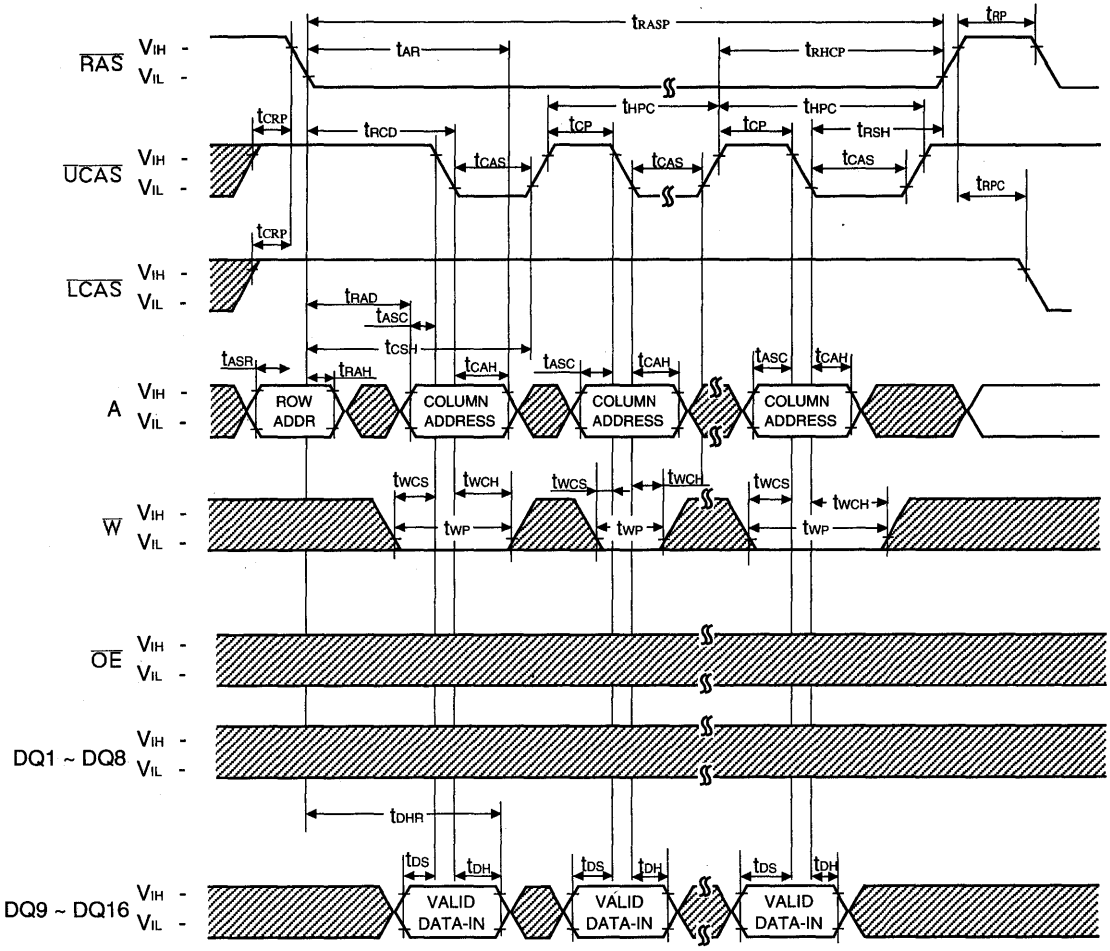
HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open

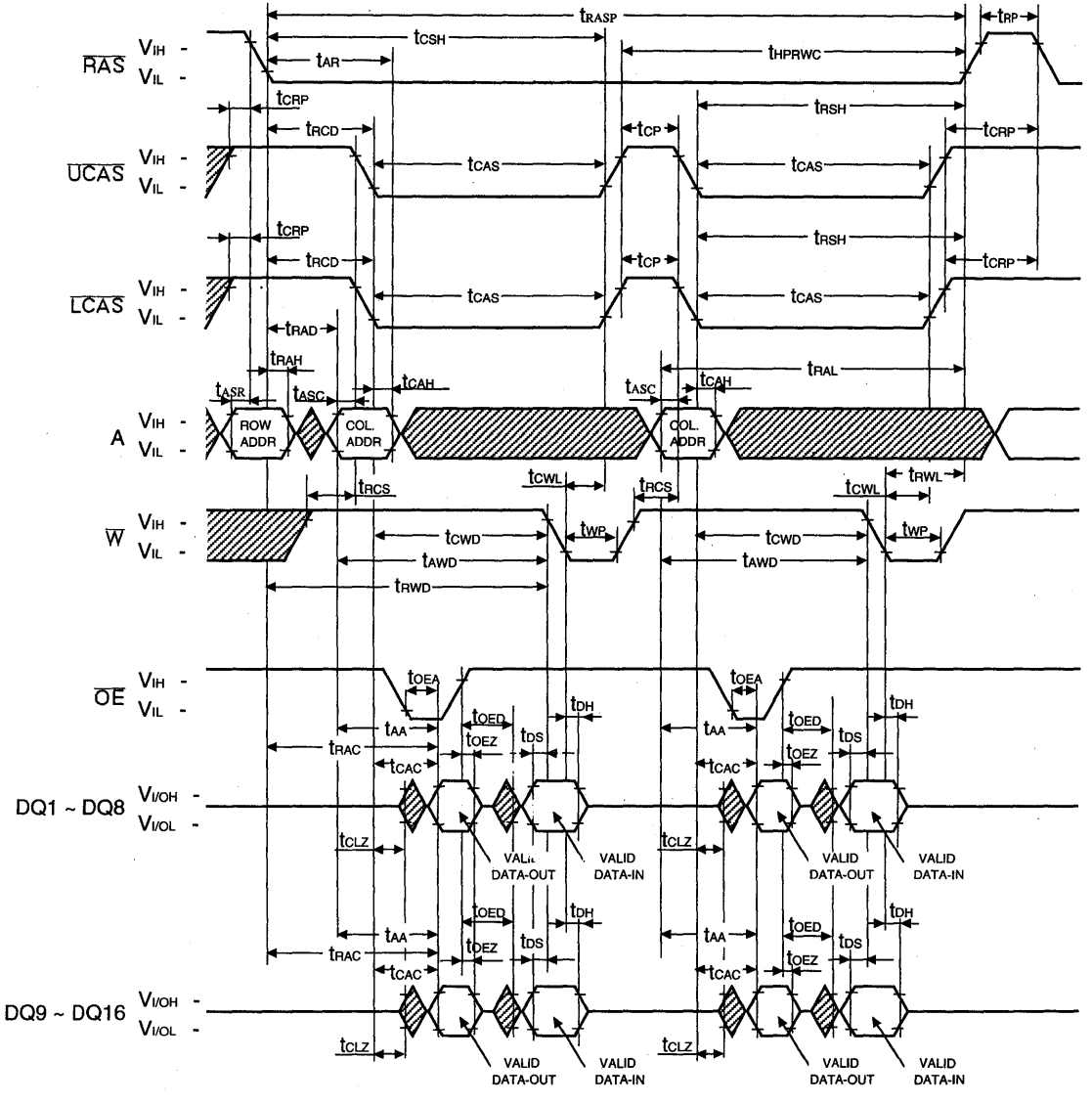


HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

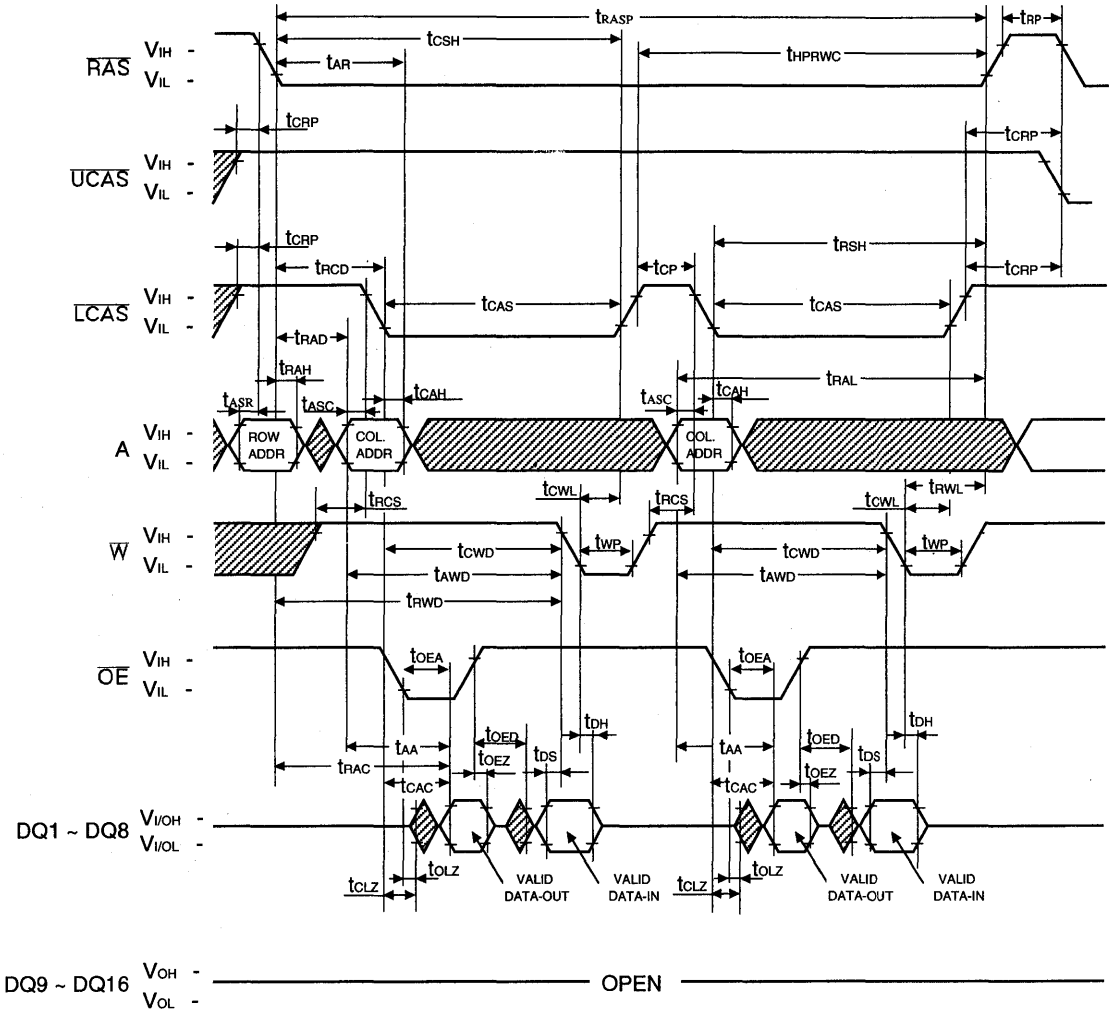
NOTE : D_{OUT} = Open



HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE

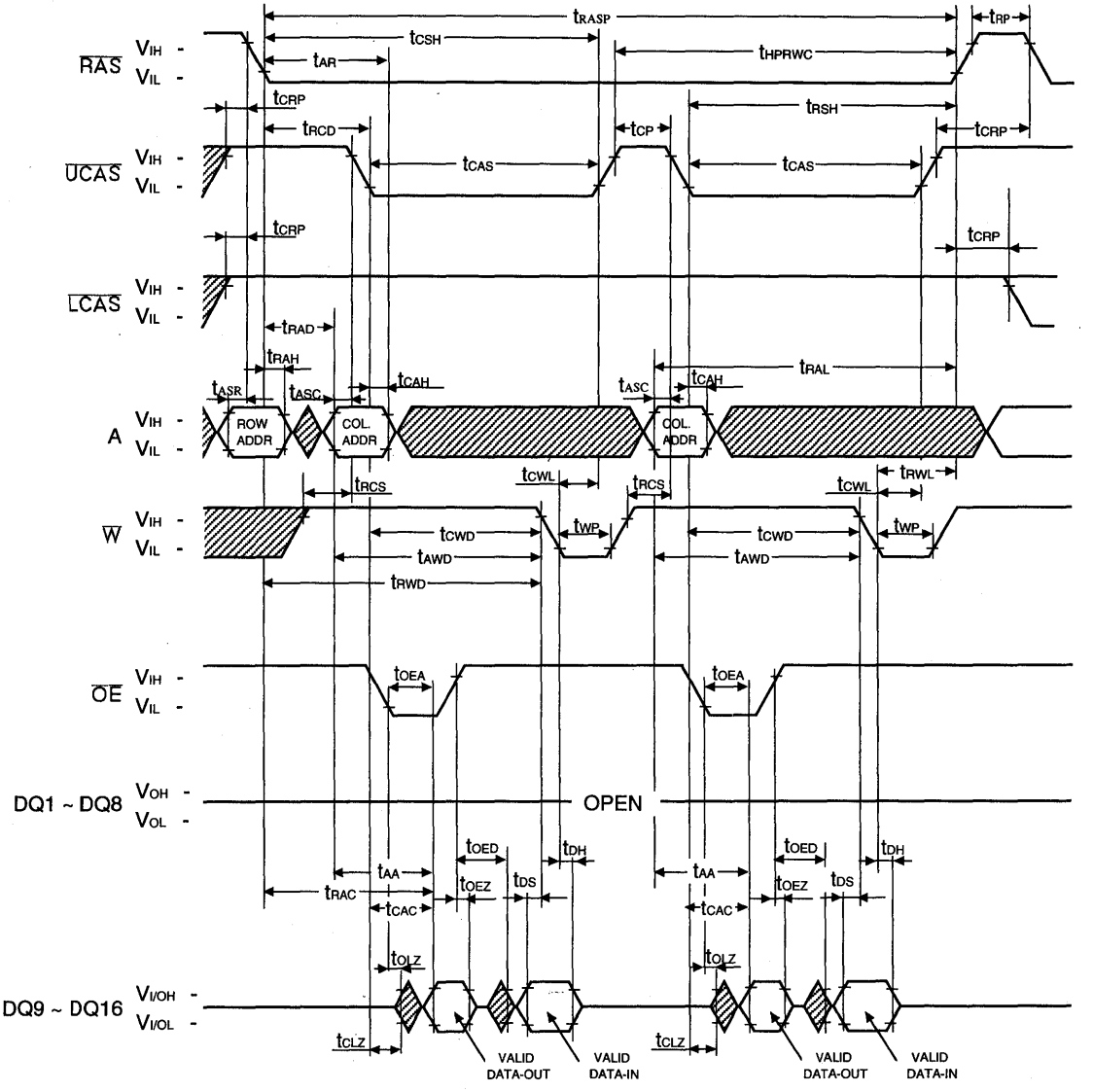


HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



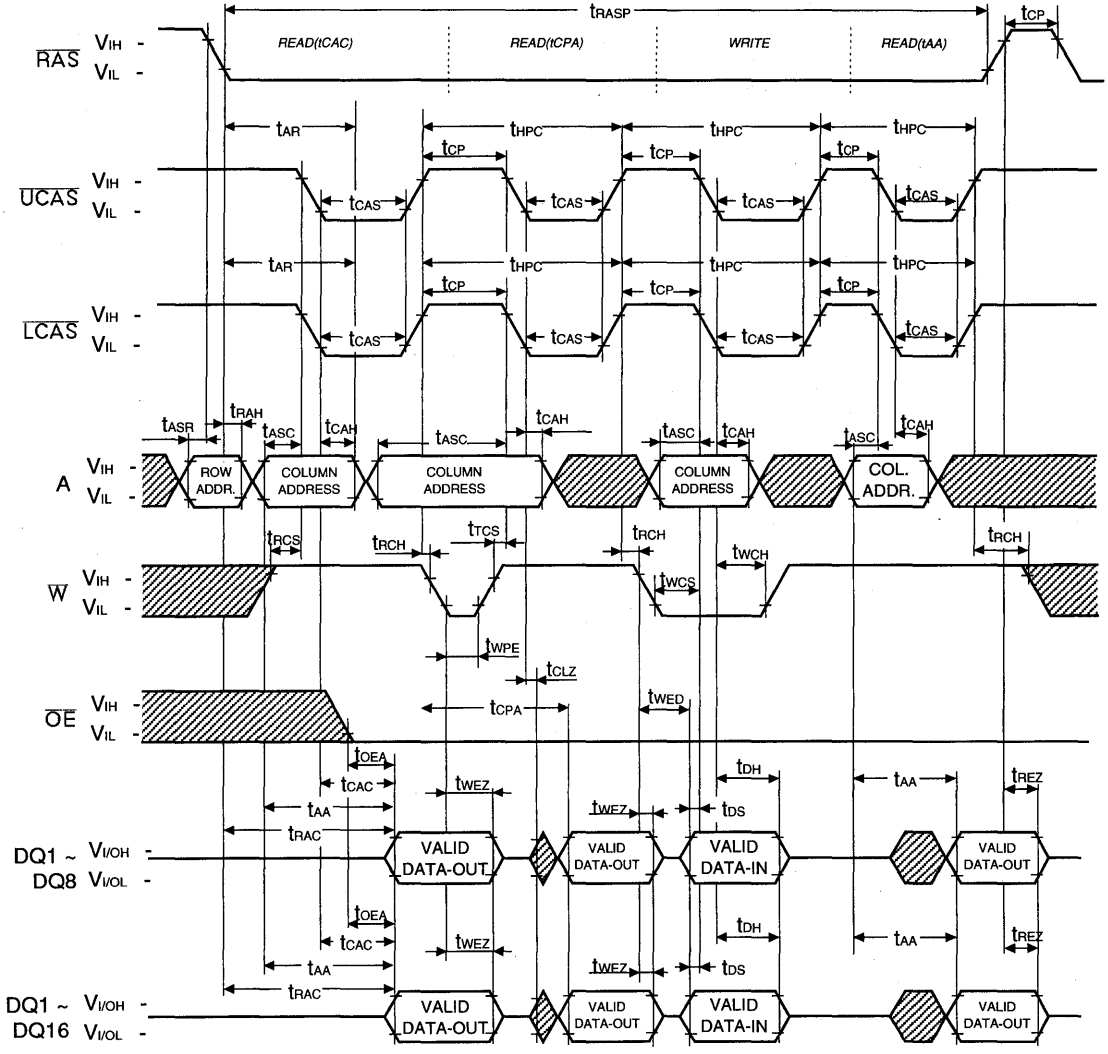
Don't Care

HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



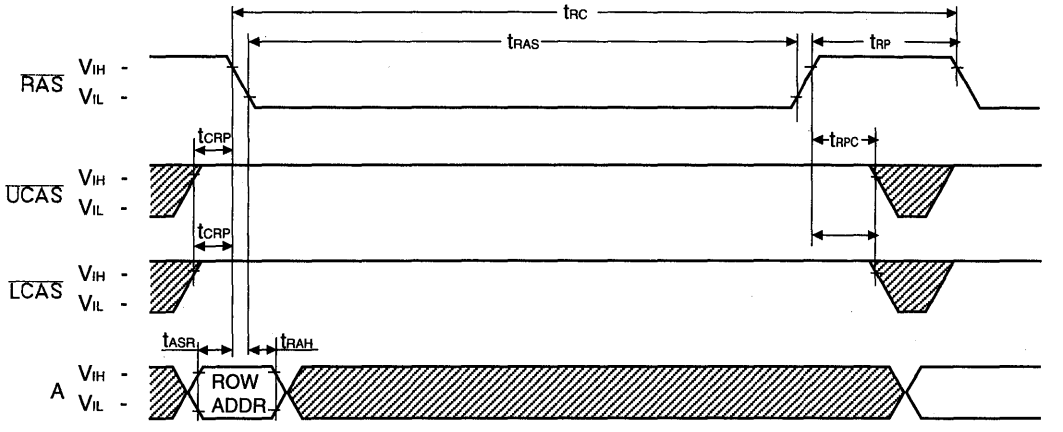
Don't Care

HYPER PAGE READ AND WRITE MIXED CYCLE



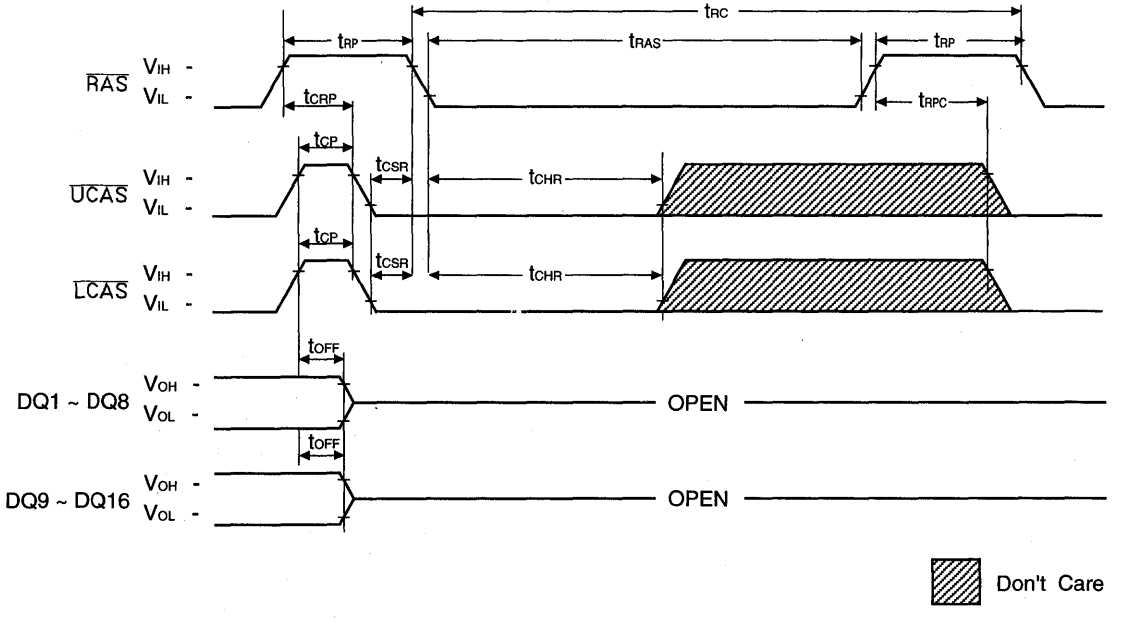
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



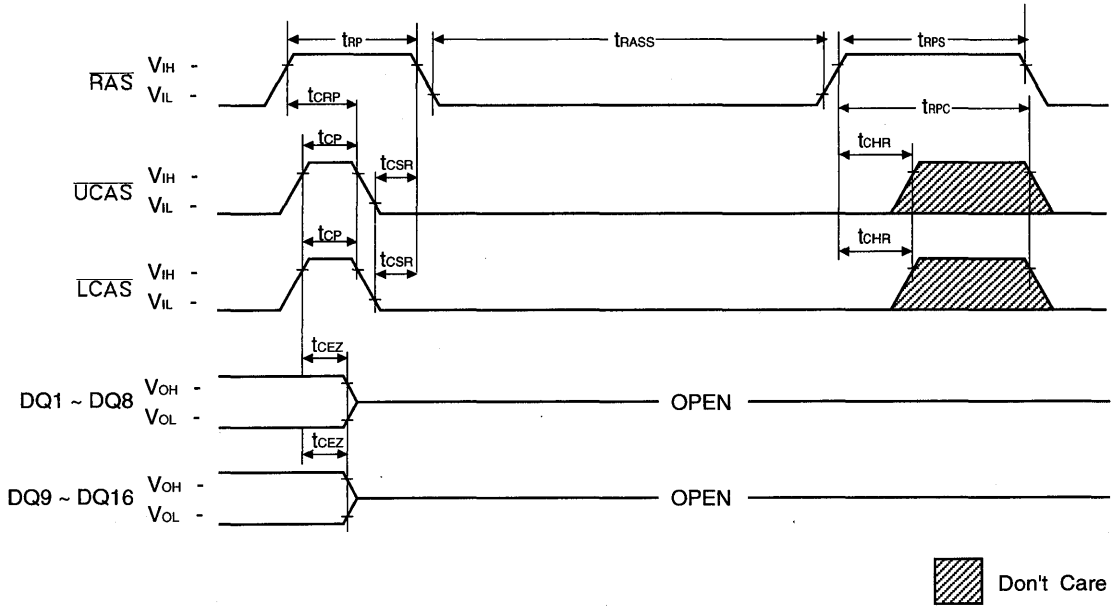
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE(LL-version)

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



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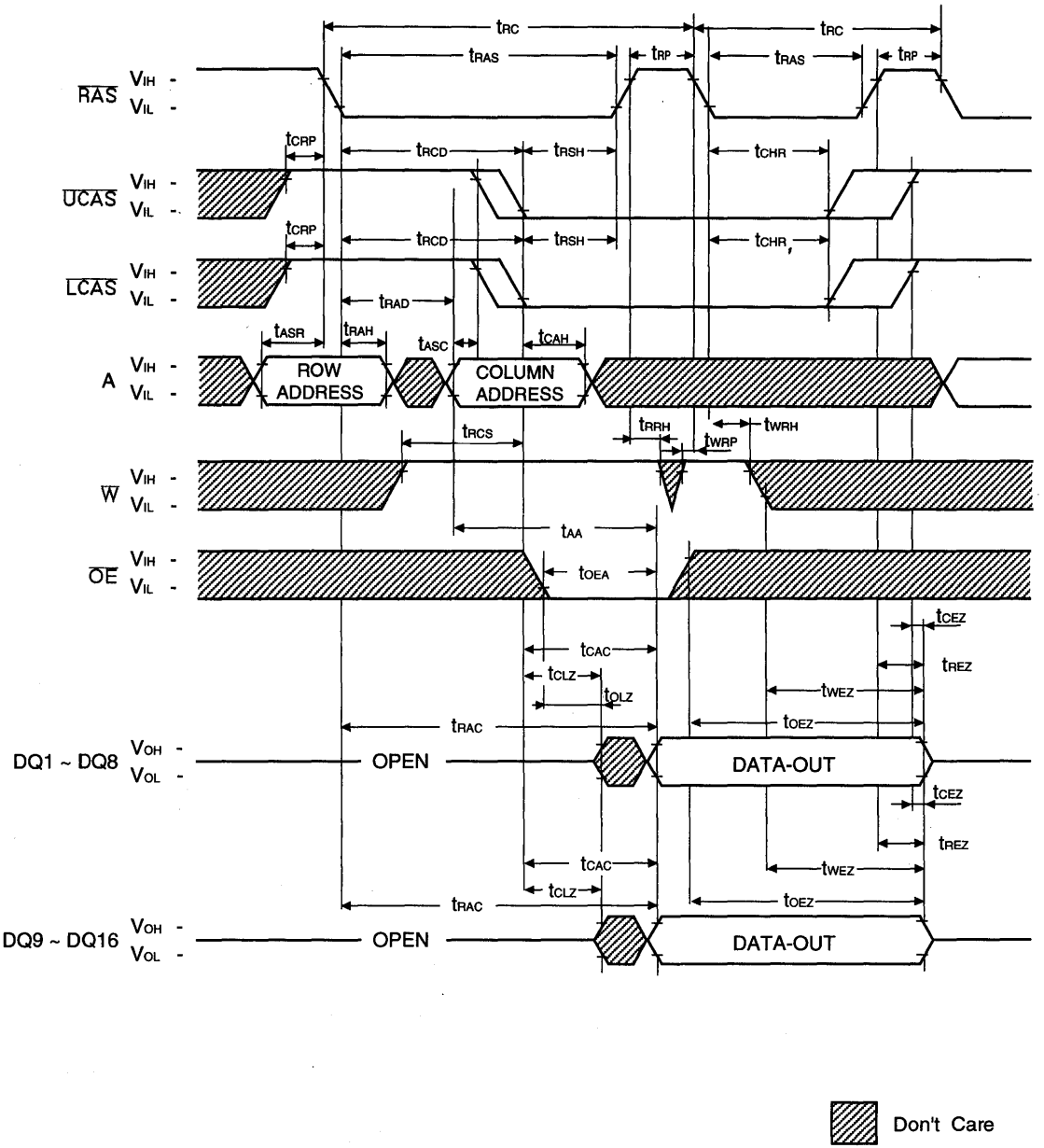
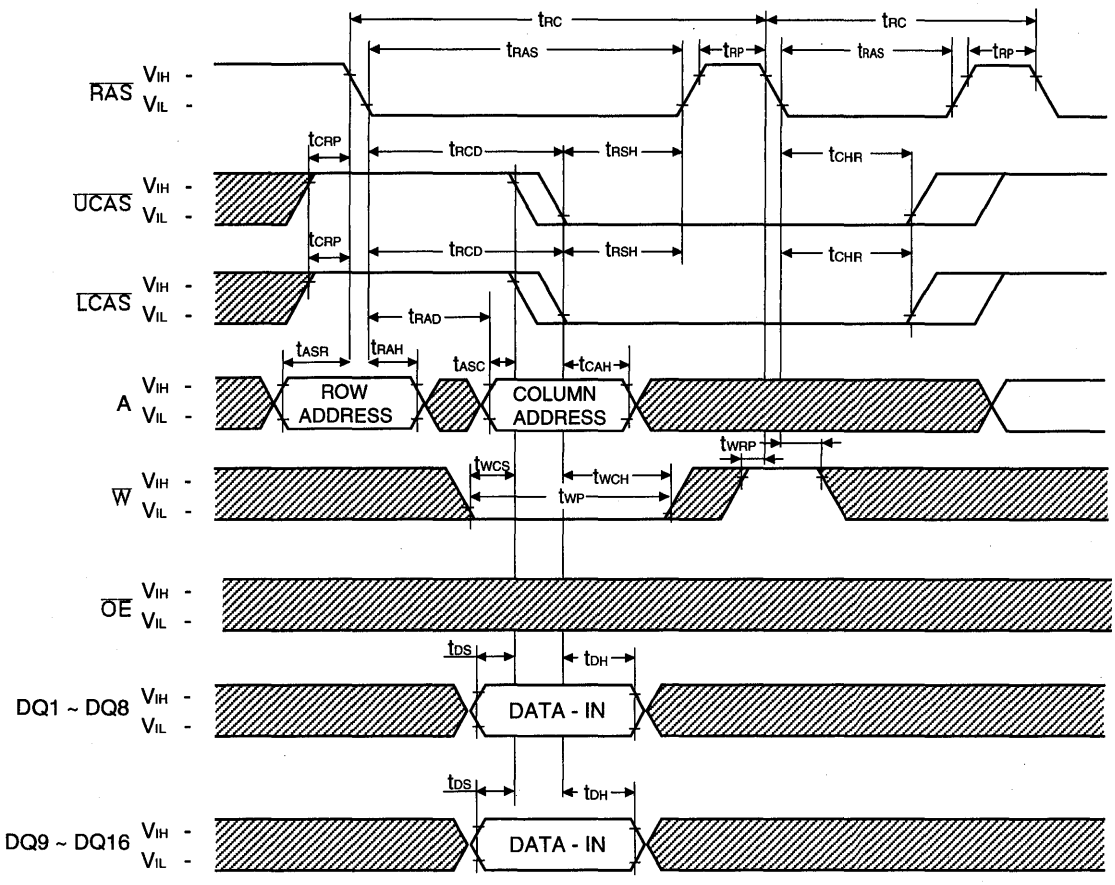
SAMSUNG ELECTRONICS

HIDDEN REFRESH CYCLE (READ)



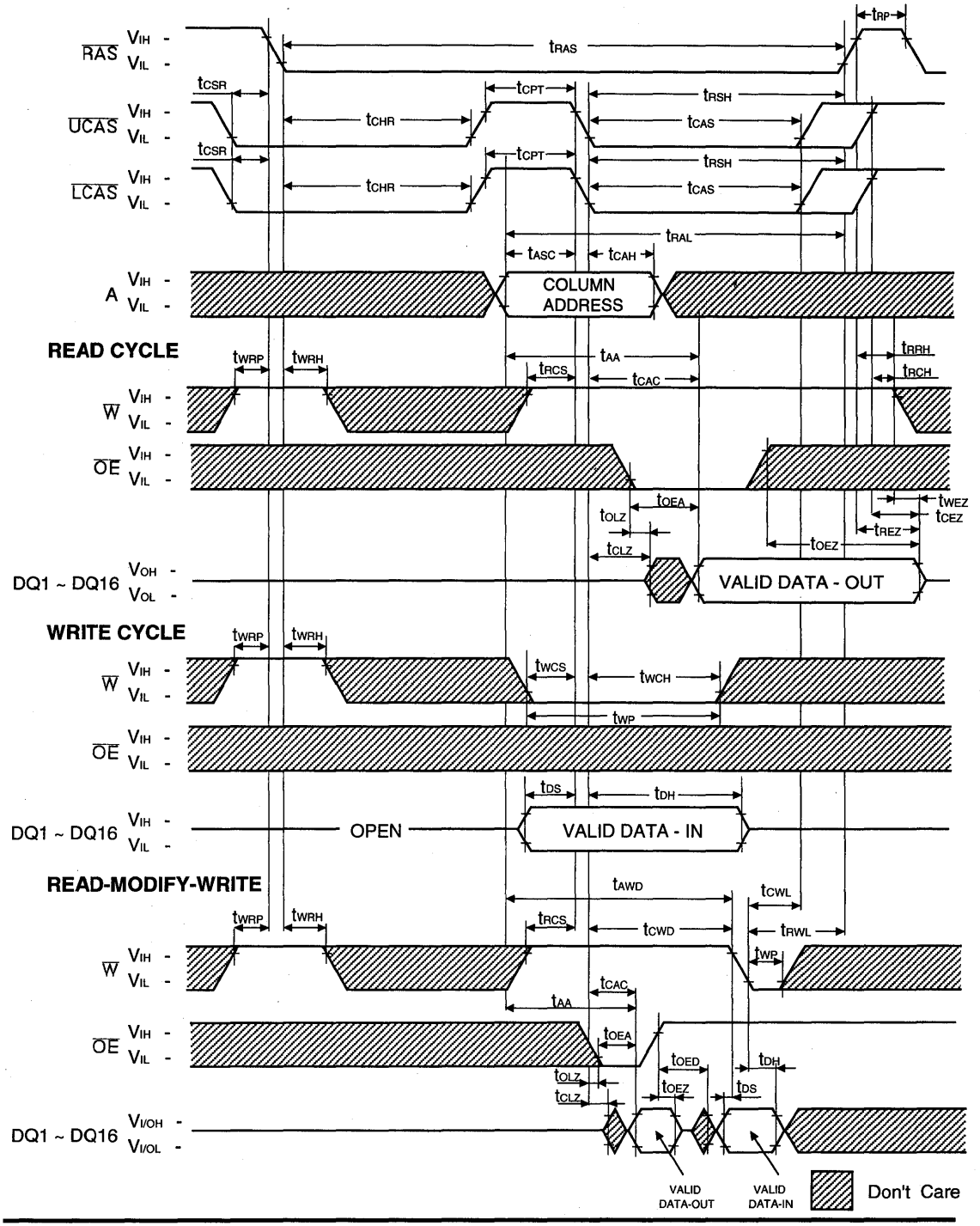
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



Don't Care

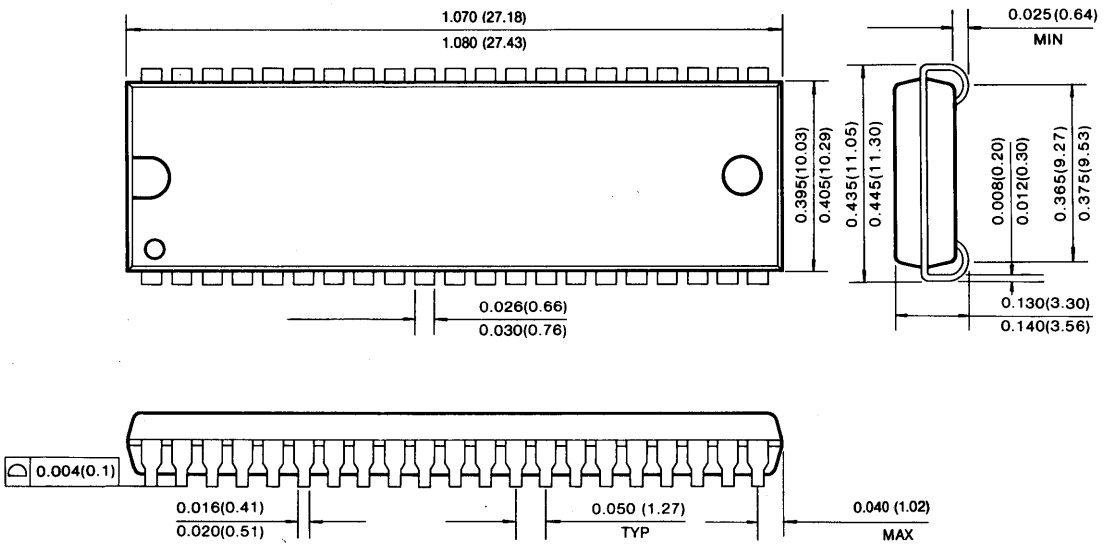
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



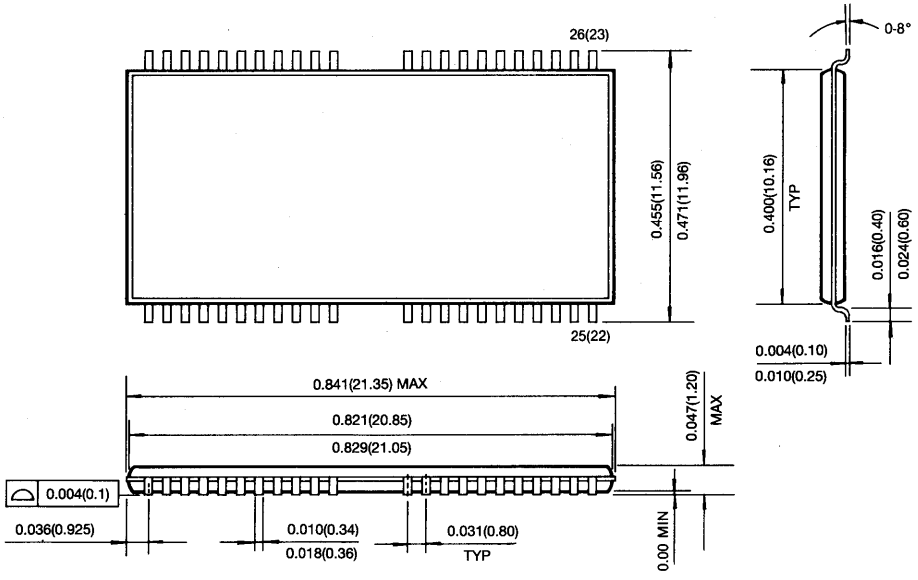
PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



1M x 16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM416V1204A-6/A-L6/A-F6	60ns	17ns	110ns	24ns
KM416V1204A-7/A-L7/A-F7	70ns	20ns	130ns	29ns
KM416V1204A-8/A-L8/A-F8	80ns	20ns	150ns	34ns

- **Extended Data Out Mode (Fast page Mode with Extended Data Out)**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +3.3V±0.3V power supply**
- **Refresh Cycle**
  - **1024 cycle/16ms (Normal)**
  - **1024 cycle/128ms (L-version)**
  - **1024 cycle/128ms (F-version)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

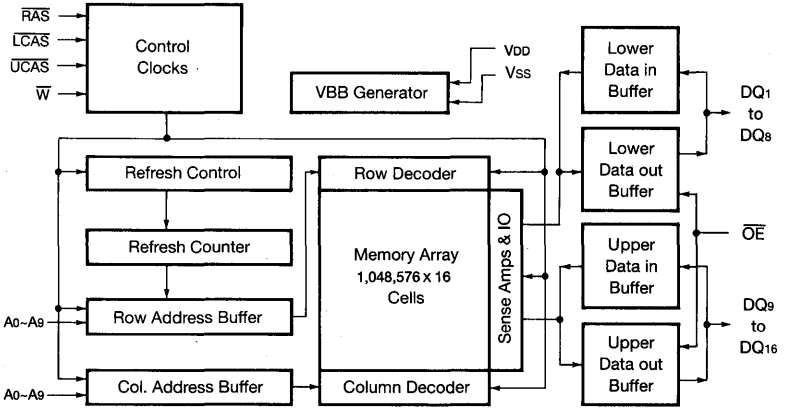
GENERAL DESCRIPTION

The Samsung KM416V1204A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

The KM416V1204A/A-L/A-F features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416V1204A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

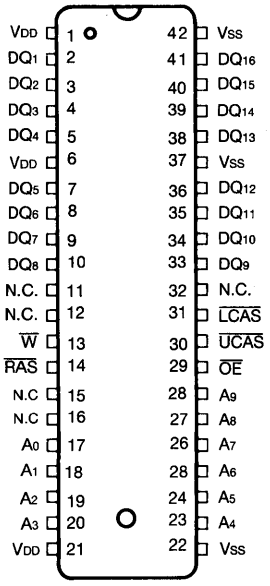
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

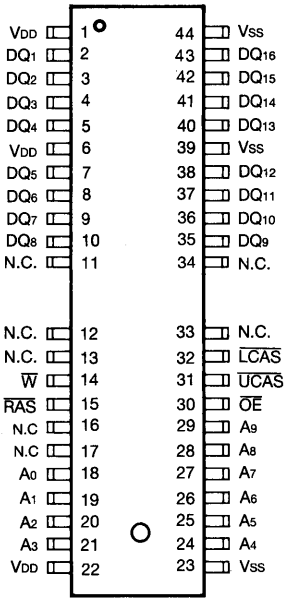
PIN CONFIGURATION (Top Views)

• KM416V1204AJ



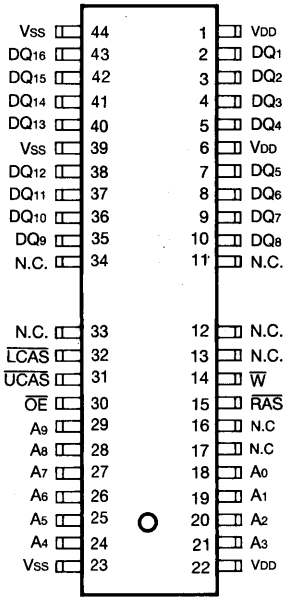
(SOJ)

• KM416V1204AT



(TSOP(II)-Forword)

• KM416V1204AR



(TSOP(II)-Reverse)

Pin Name	Pin Function
A0-A9	Address Inputs
DQ1-16	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VDD	Power(+3.3V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 to 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.1	—	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{RC}=min.)	KM416V1204A-6/A-L6/A-F6 KM416V1204A-7/A-L7/A-F7 KM416V1204A-8/A-L8/A-F8	I_{CC1}	-	150 140 130	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})	KM416V1204A KM416V1204A-L KM416V1204A-F	I_{CC2}	-	2 1 1	mA mA mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM416V1204A-6/A-L6/A-F6 KM416V1204A-7/A-L7/A-F7 KM416V1204A-8/A-L8/A-F8	I_{CC3}	-	150 140 130	mA mA mA
EDO Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC}=min.)	KM416V1204A-6/A-L6/A-F6 KM416V1204A-7/A-L7/A-F7 KM416V1204A-8/A-L8/A-F8	I_{CC4}	-	120 110 100	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{DD}-0.2V)	KM416V1204A KM416V1204A-L KM416V1204A-F	I_{CC5}	-	1 300 200	mA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC}=min.)	KM416V1204A-6/A-L6/A-F6 KM416V1204A-7/A-L7/A-F7 KM416V1204A-8/A-L8/A-F8	I_{CC6}	-	150 140 130	mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V_{IH})=V_{DD}-0.2V, Input Low Voltage(V_{IL})=0.2V $\overline{UCAS}$, $\overline{LCAS}$= 0.2V D_{IN}=Don't Care, t_{RC}=125μs (L-Ver) t_{RAS}=t_{RAS} min~300ns	KM416V1204A-L	I_{CC7}	-	350	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_9=V_{DD}-0.2V or 0.2V DQ_1-DQ_{16}=V_{DD}-0.2V or 0.2V or Open	KM416V1204A-F	I_{CCS}	-	250	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{DD}+0.3V, all other pins not under test=0 V)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{DD})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once while one Hyper page mode cycle time t_{HPC}.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V. f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

(Test condition : V_{IH}/V_{IL}=2.1V/0.8V, V_{OH}/V_{OL}=2.0V/0.8V, Output Loading C_L=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		17		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CLZ}	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	17		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	15	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	15
Column address hold time	t_{CAH}	10		15		15		ns	15
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command set-up time	t_{WCS}	0		0		0		ns	8
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		50		55		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10		15		20		ns	18
Data-in set-up time	t_{DS}	0		0		0		ns	10,21
Data-in hold time	t_{DH}	10		15		15		ns	10,21
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal)	t_{REF}		16		16		16	ms	
Refresh period (L-version)	t_{REF}		128		128		128	ms	
Refresh period (F-version)	t_{REF}		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8,17
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		95		105		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	20
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25\		30		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	15	3	20	3	20	ns	7
$\overline{OE}$ commend hold time	t_{OEH}	15		20		20		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Hyper Page mode cycle time	t_{HPC}	24		29		34		ns	12
Hyper Page mode read-modify-write cycle time	t_{HPRWC}	76		81		91		ns	12
$\overline{CAS}$ orcgarge time (Hyper page mode)	t_{CP}	10		10		10		ns	16
$\overline{RAS}$ pulse width (Hyper page mode)	t_{RASP}	60	200.000	70	200.000	80	200.000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
Output data hold time	t_{DOH}	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	15	3	20	3	20	ns	7
$\overline{W}$ to data delay	t_{WED}	15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		5		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		5		ns	
$\overline{RAS}$ pulse width (F-ver)	t_{RASS}	100		100		100		μs	13
$\overline{RAS}$ precharge time (F-ver)	t_{RPS}	110		130		150		ns	13
$\overline{CAS}$ hlod time (F-ver)	t_{CHS}	-50		-50		-50		ns	13

KM416V1204A/A-L/A-F Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ_1~DQ_8	DQ_9~DQ_{16}	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	x	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

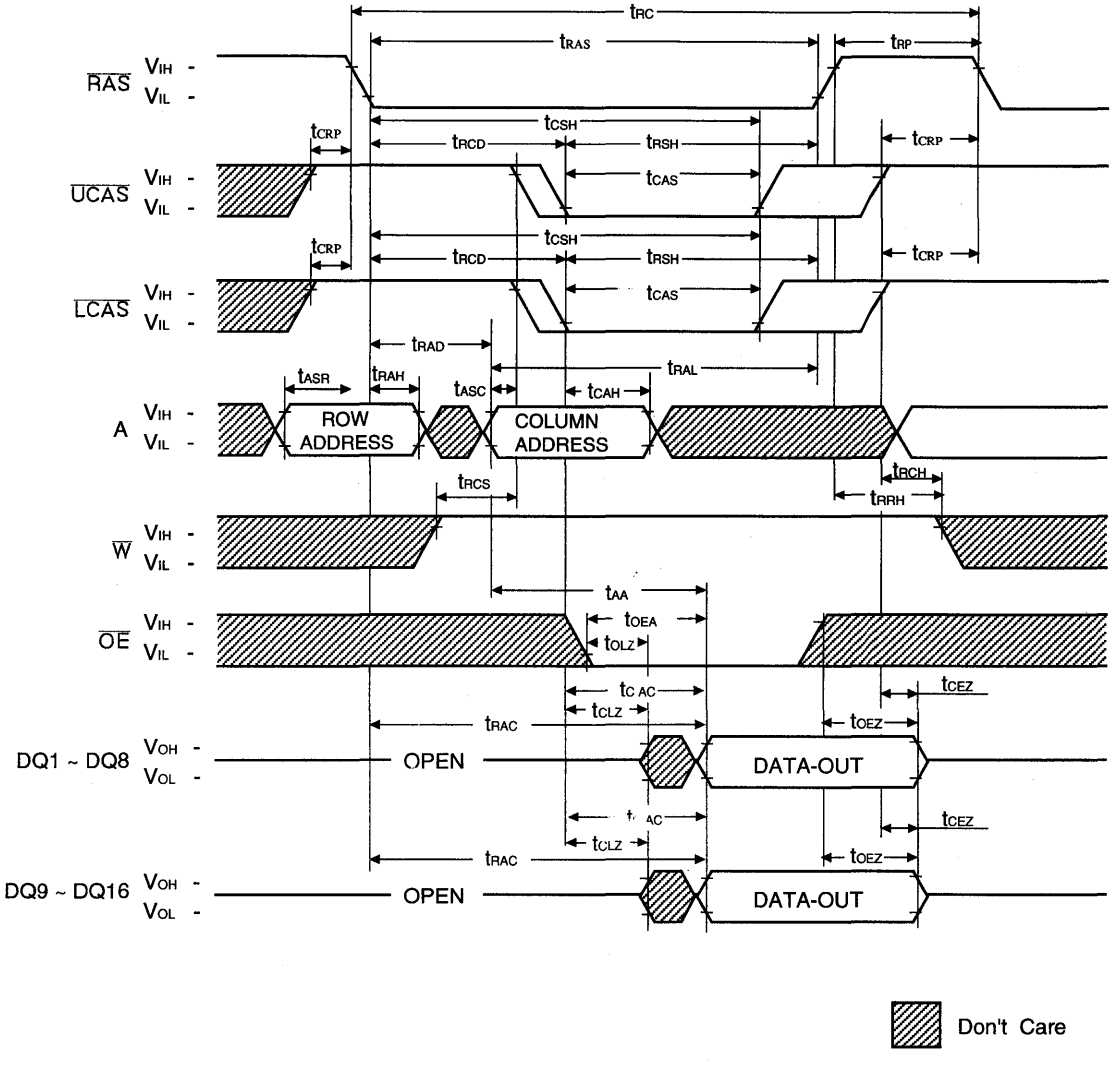
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL Loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. $t_{ASC} \geq t_{CP}$ min, Assume t_T=2.0ns.
13. 1024 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (F-version)
14. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
16. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
17. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
18. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
19. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
20. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.
21. t_{DS}, t_{DH} is independetly specified for lower byte D_{in} (1~8), upper byte $D_{in(9\sim16)}$

TIMING DIAGRAM

WORD READ CYCLE

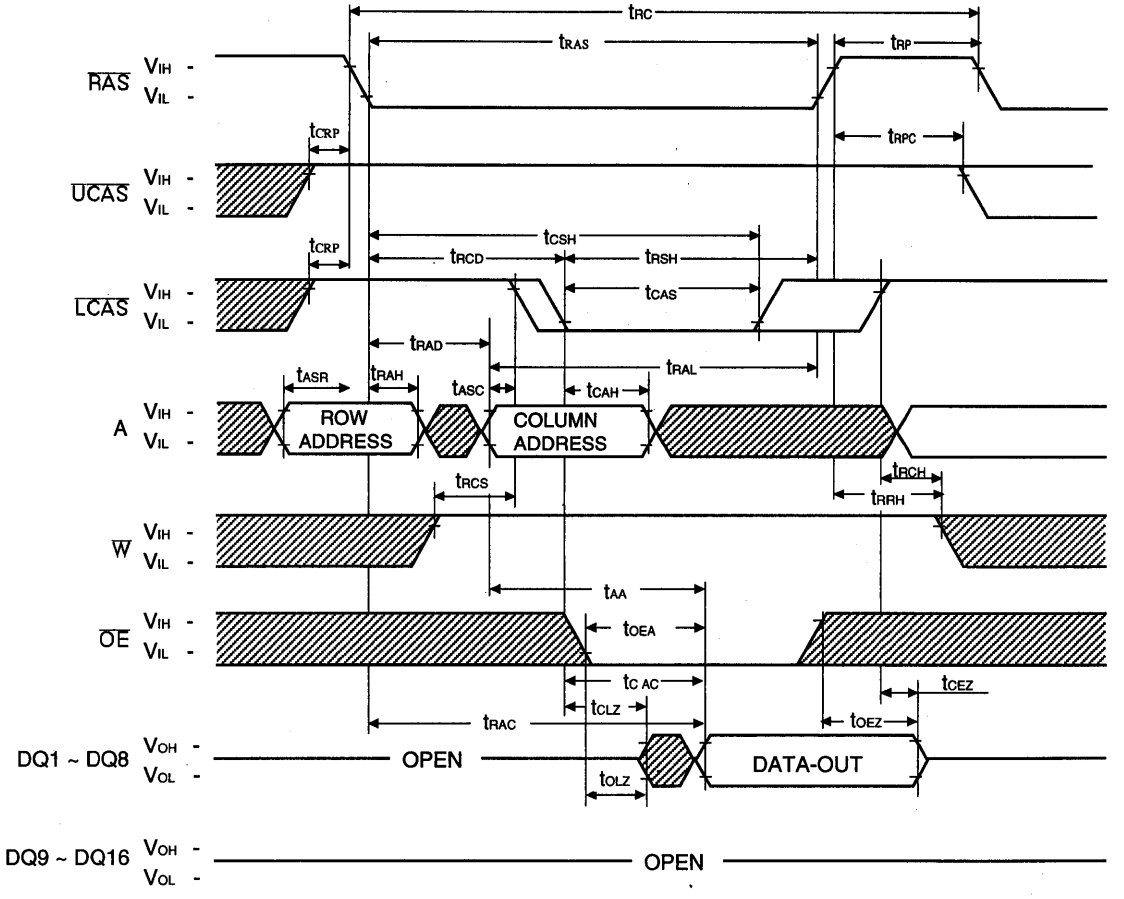
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

LOWER BYTE READ CYCLE

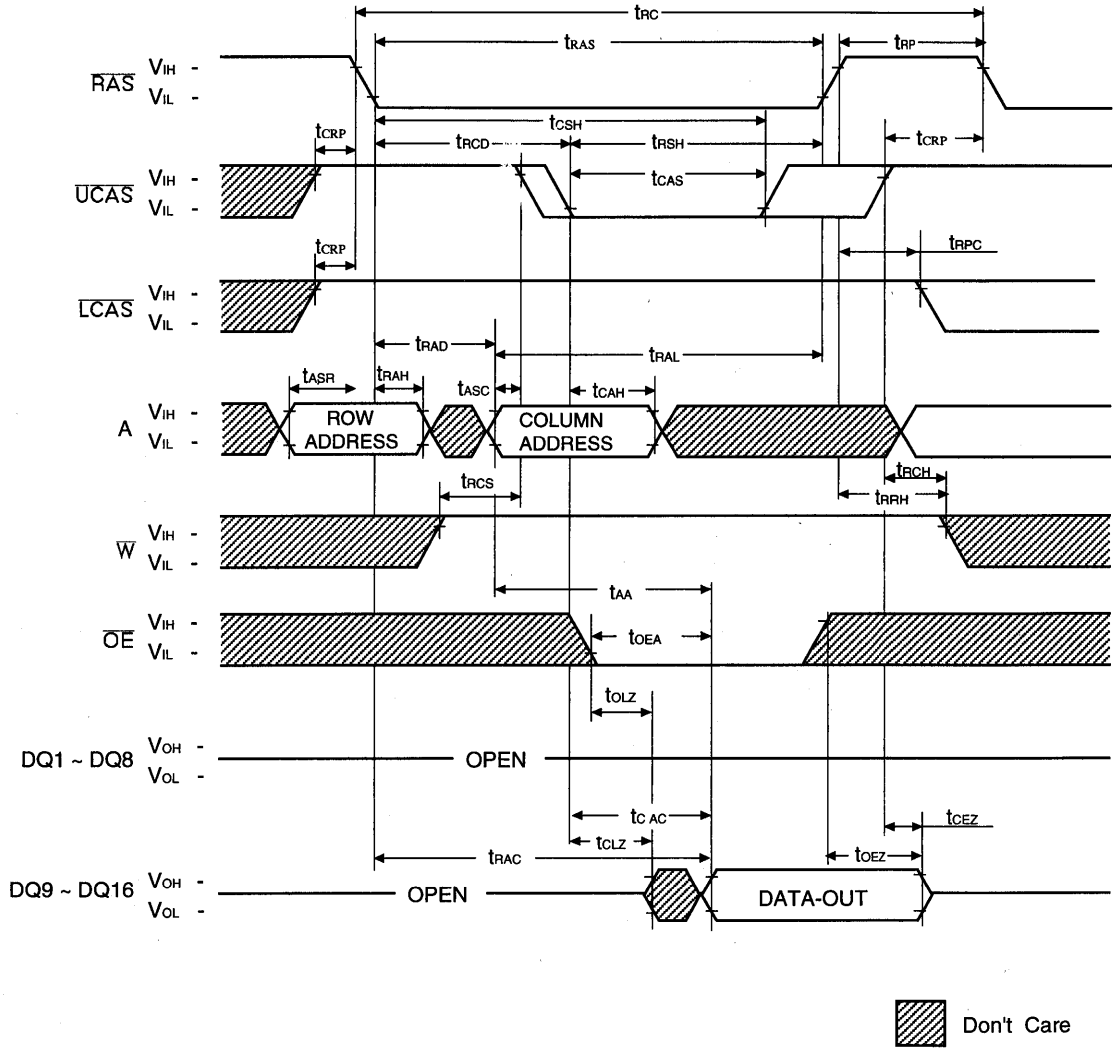
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

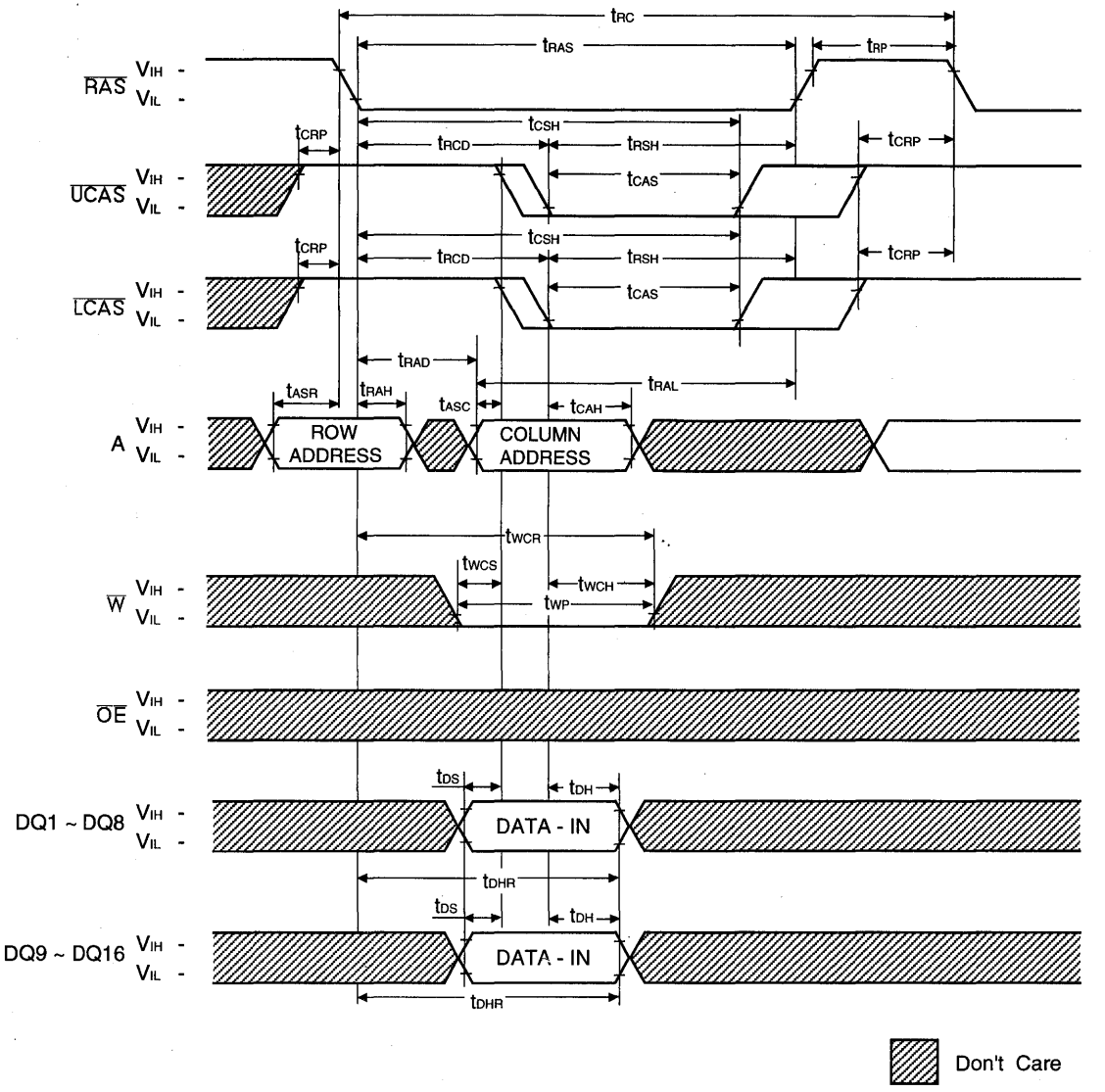
UPPER BYTE READ CYCLE

NOTE : D_{IN} = OPEN



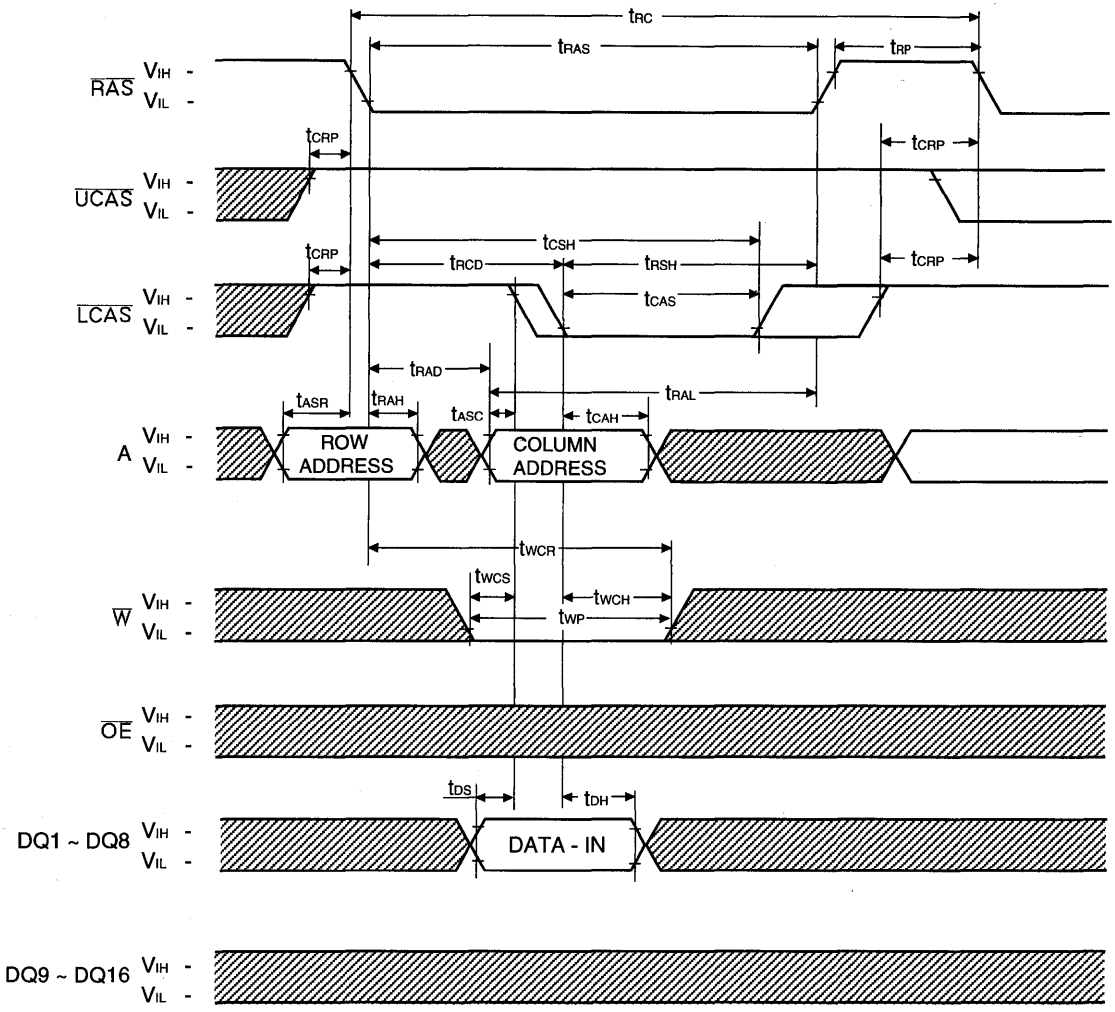
WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



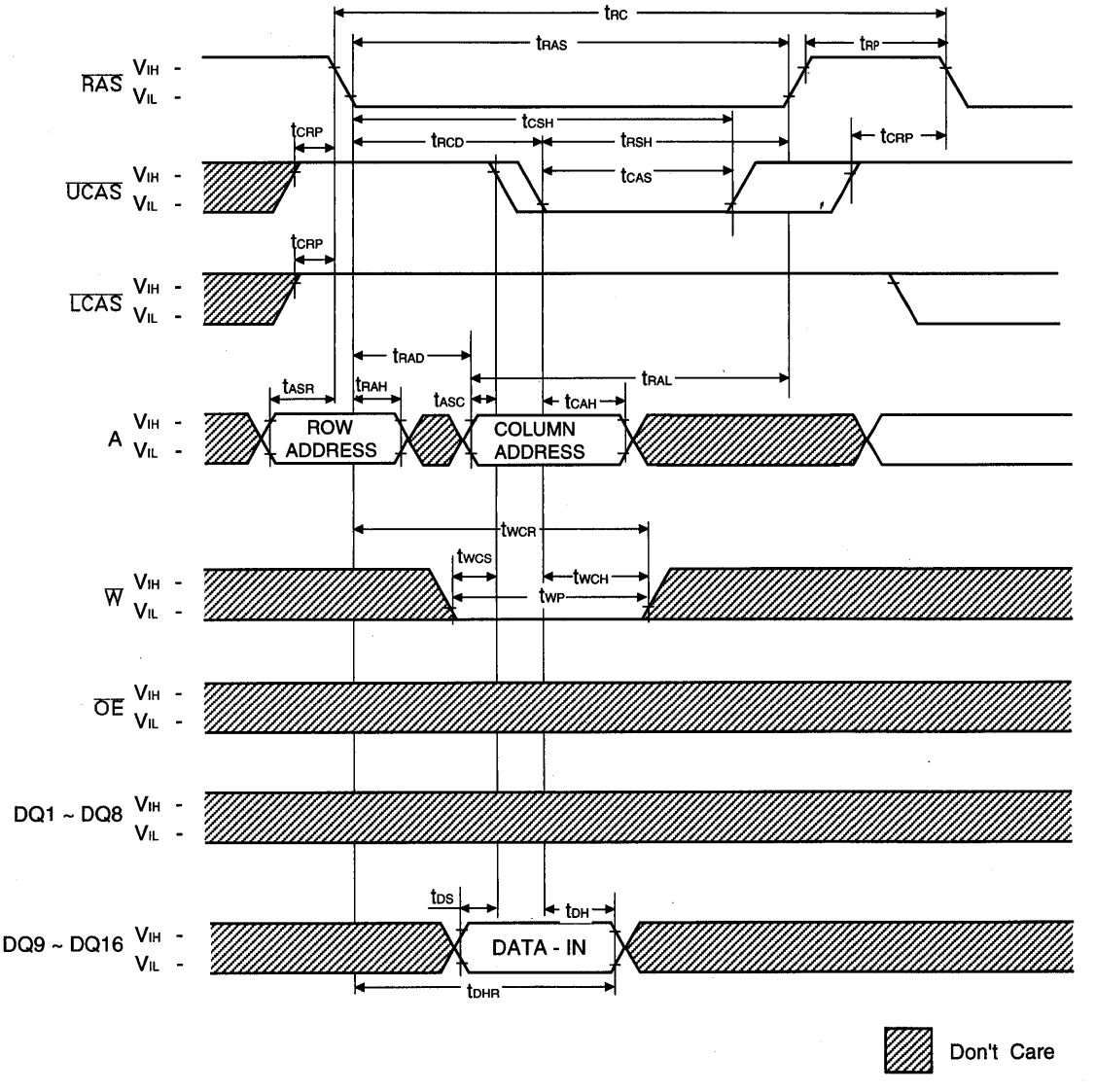
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



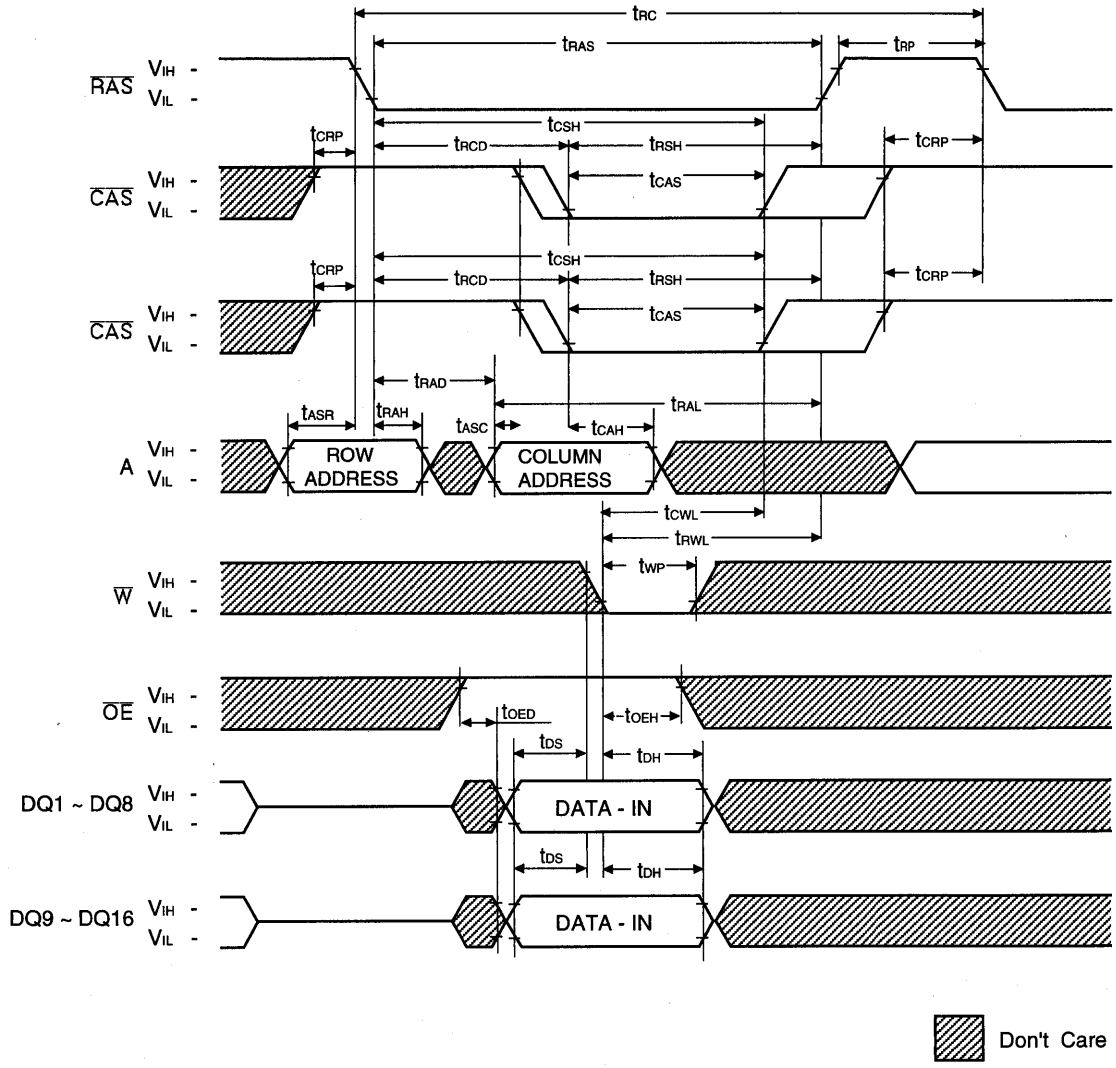
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



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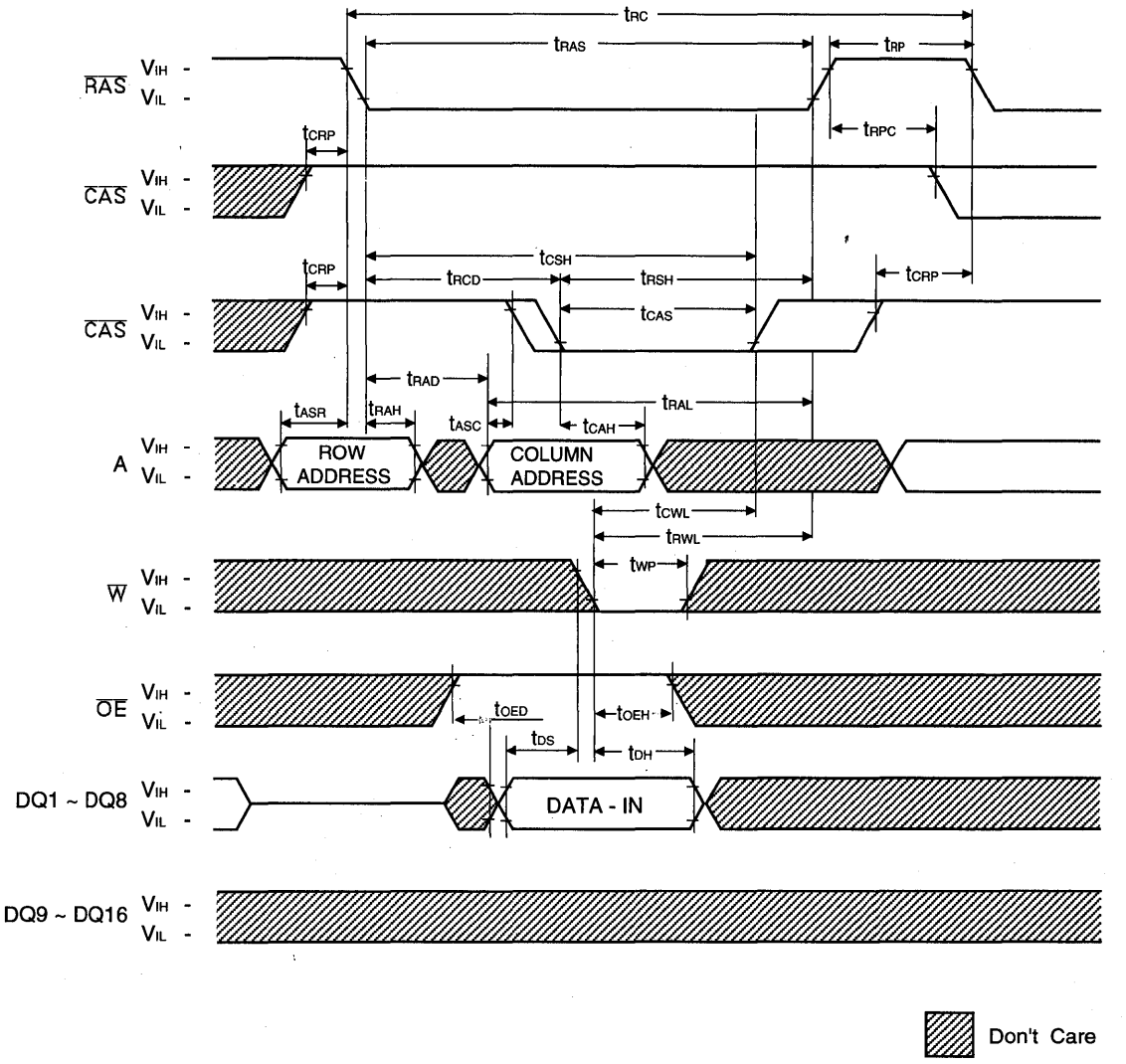
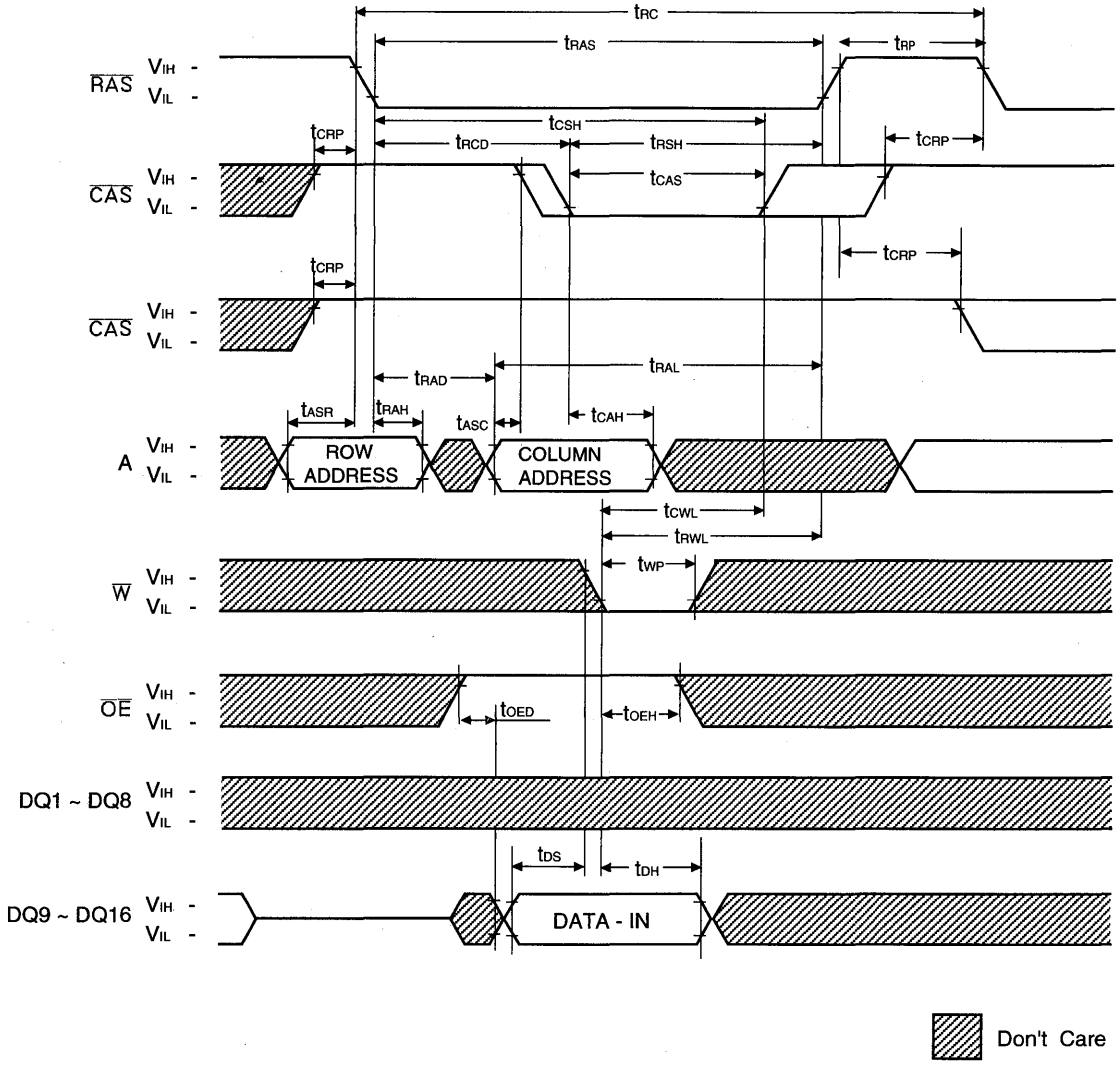
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



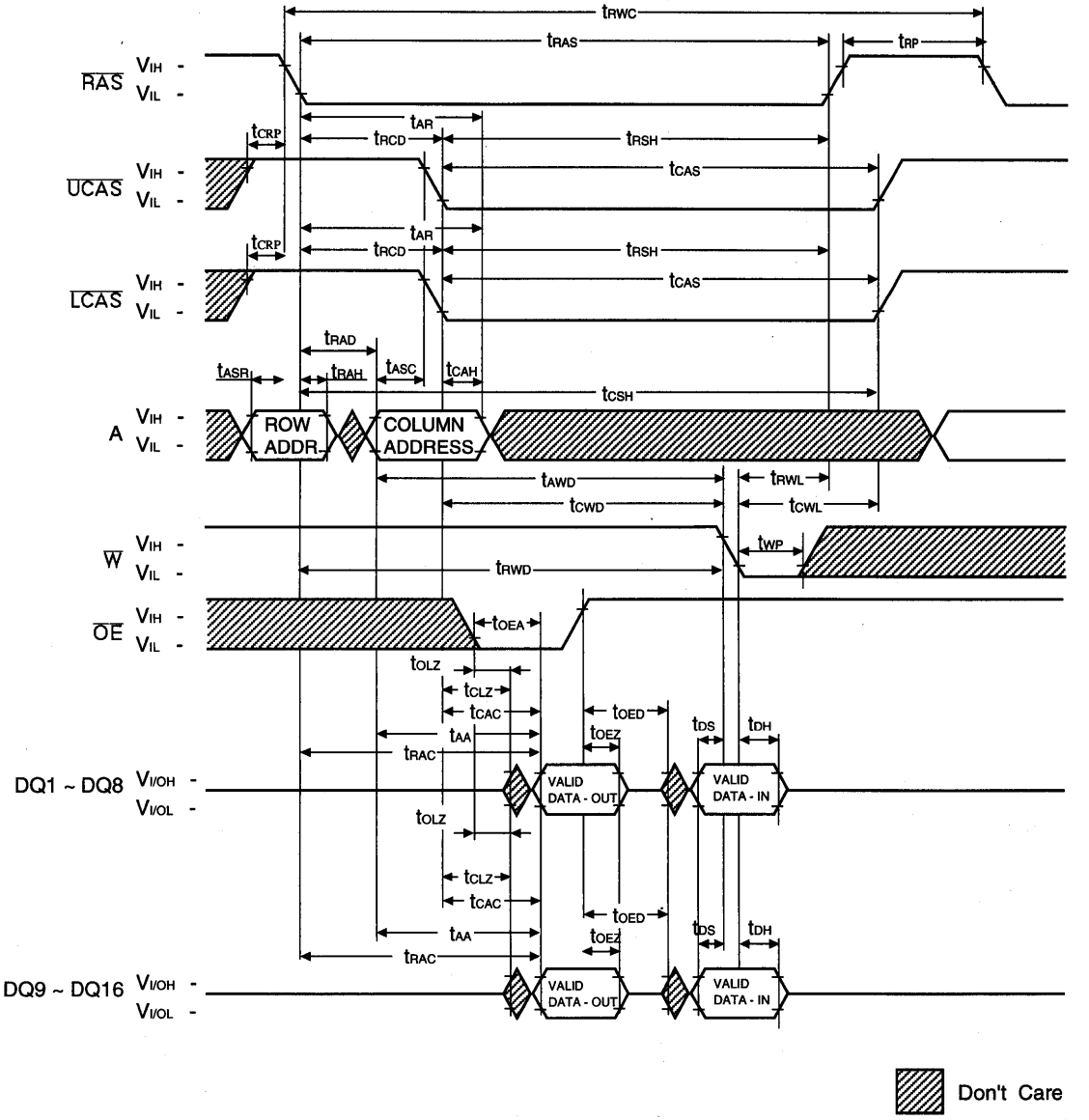
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

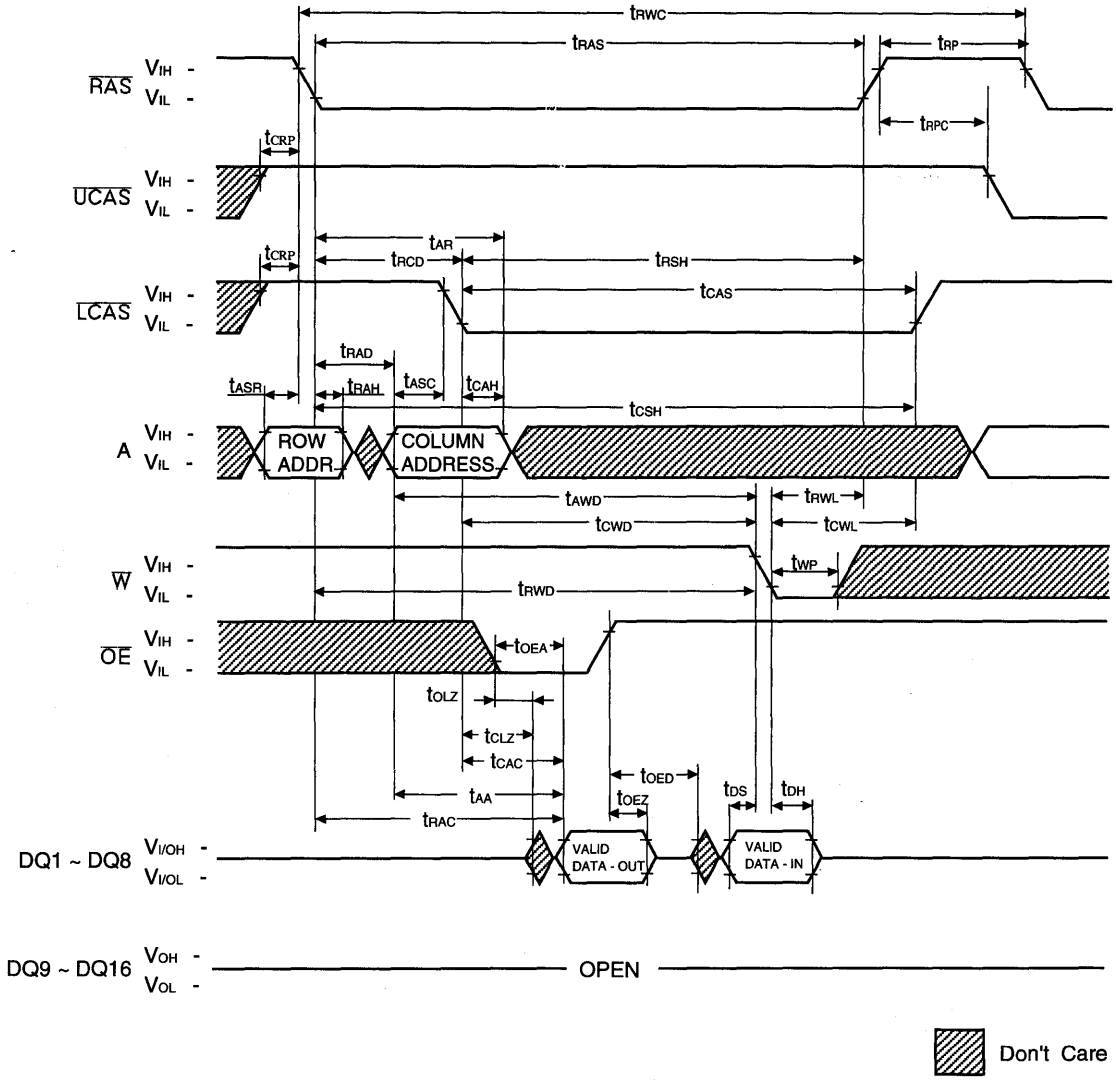


Don't Care

WORD READ - MODIFY - WRITE CYCLE

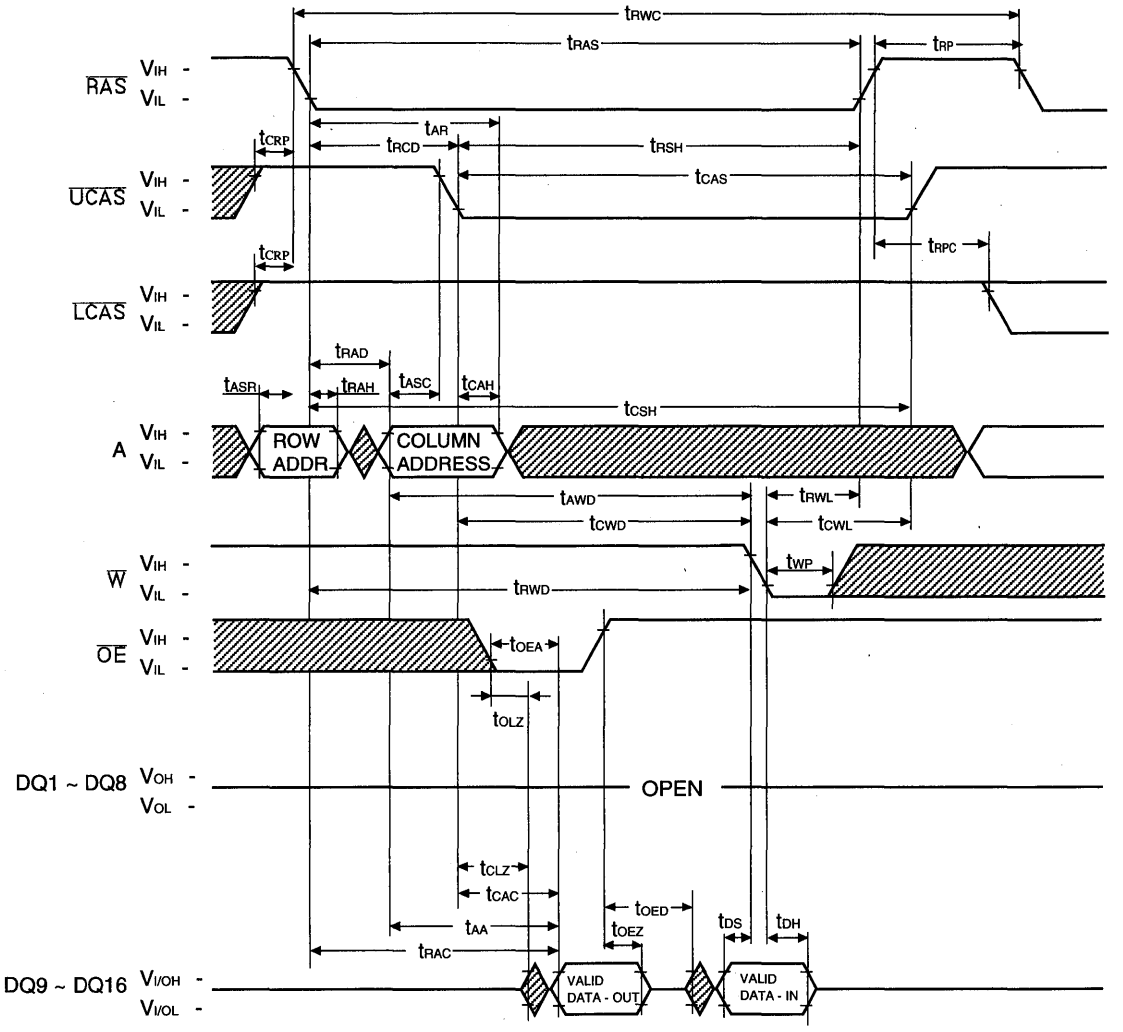


LOWER-BYTE READ - MODIFY - WRITE CYCLE

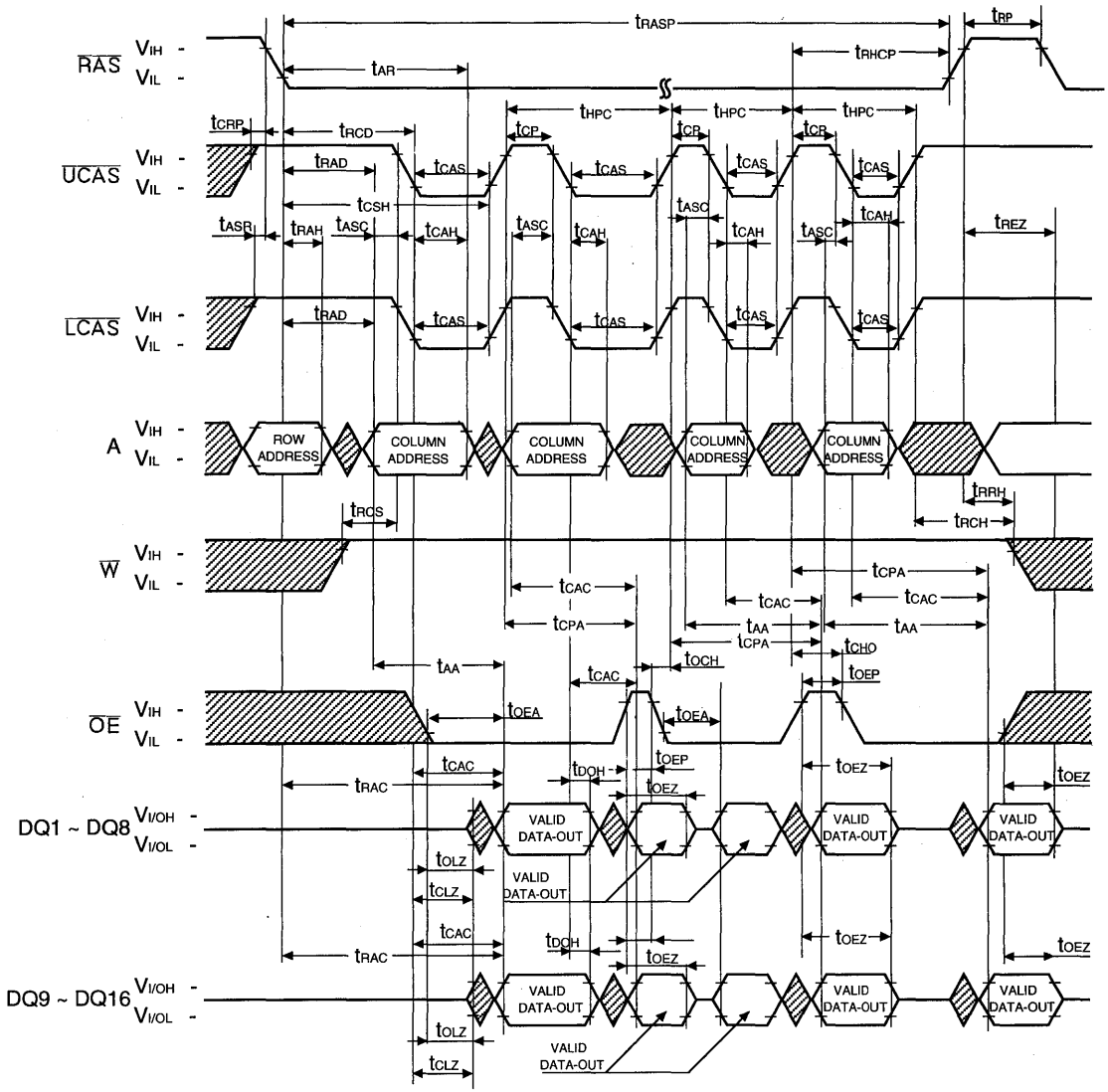


6

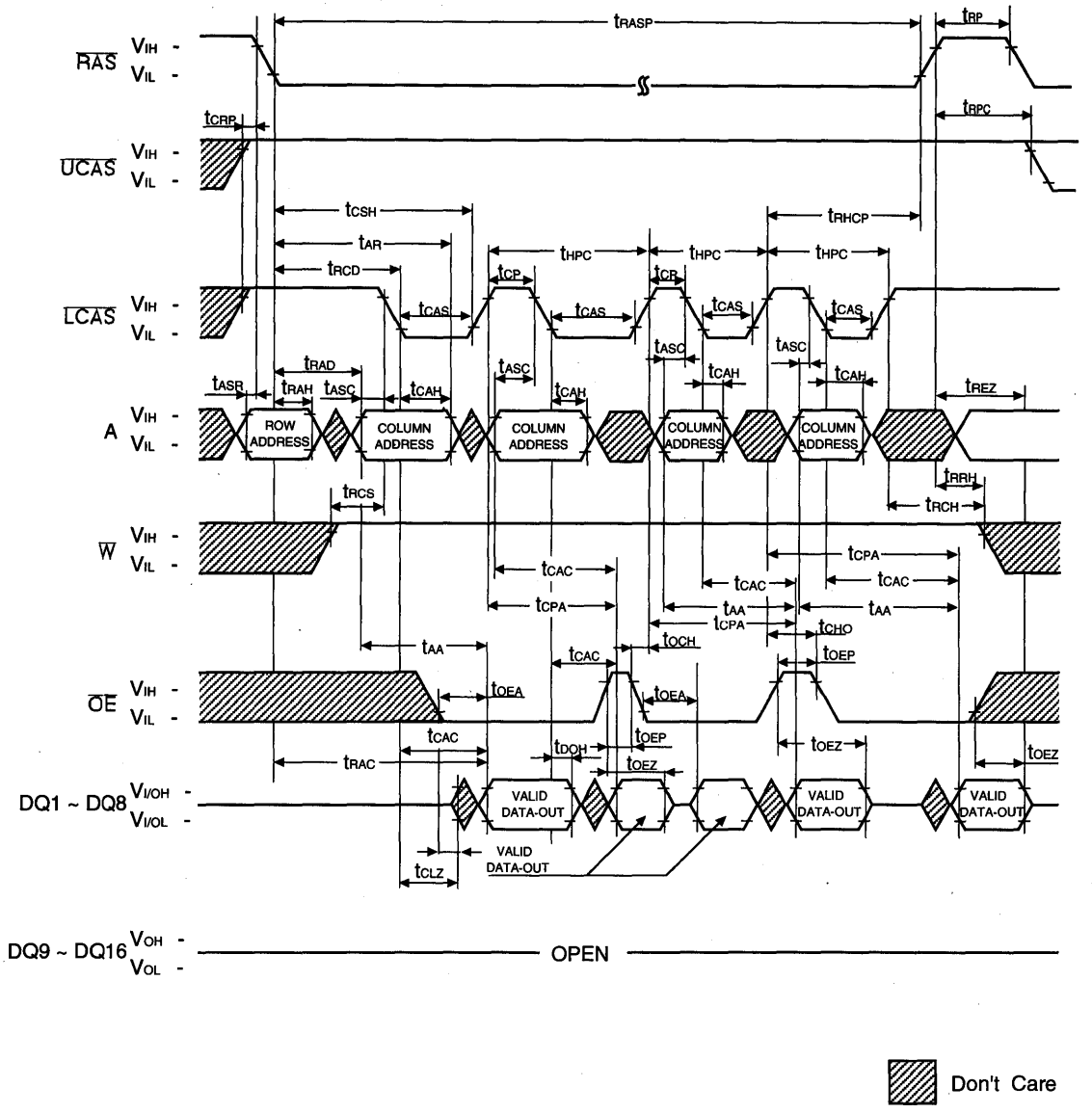
UPPER-BYTE READ - MODIFY - WRITE CYCLE



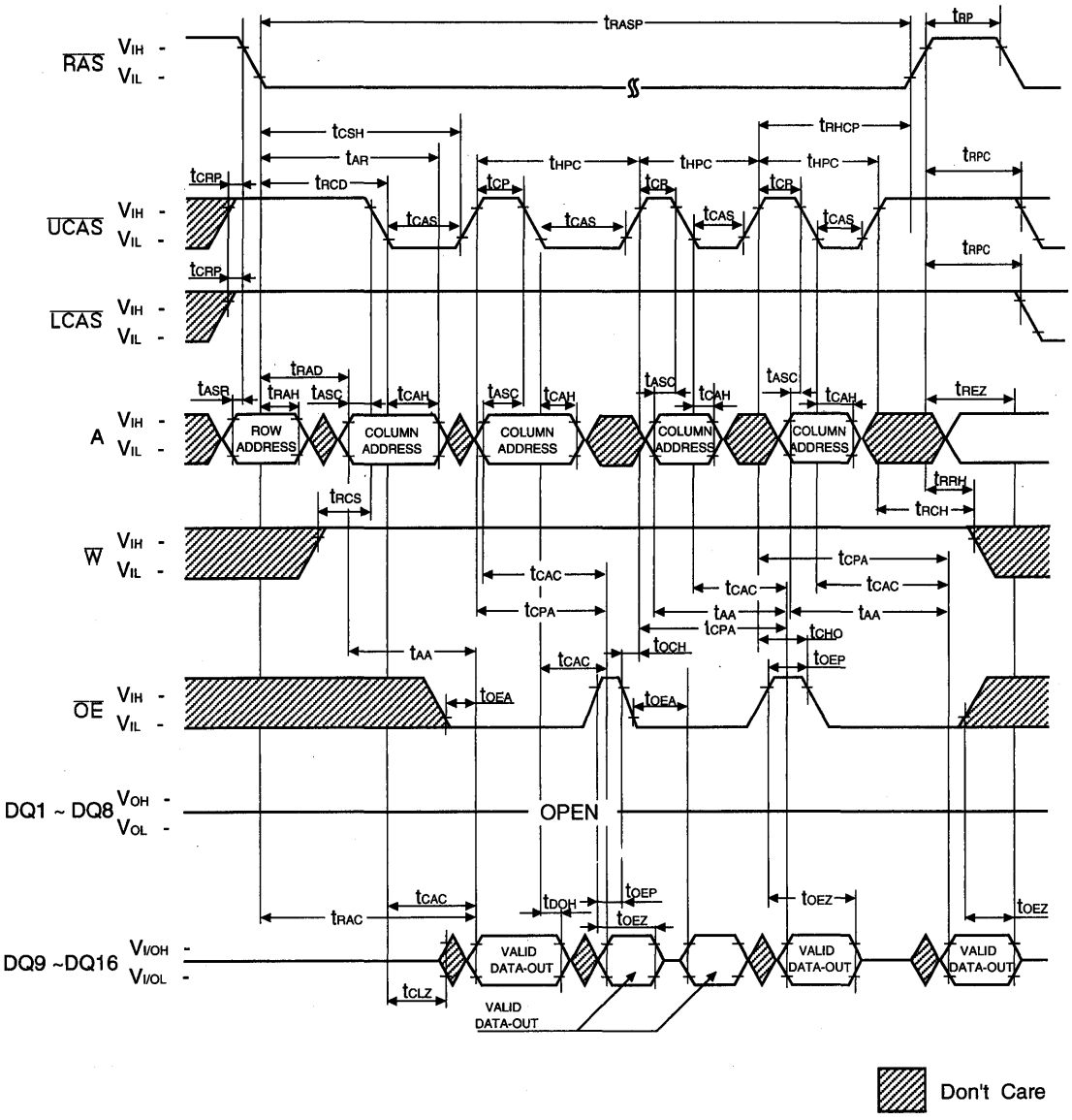
HYPER PAGE MODE WORD READ CYCLE



HYPER PAGE MODE LOWER BYTE READ CYCLE

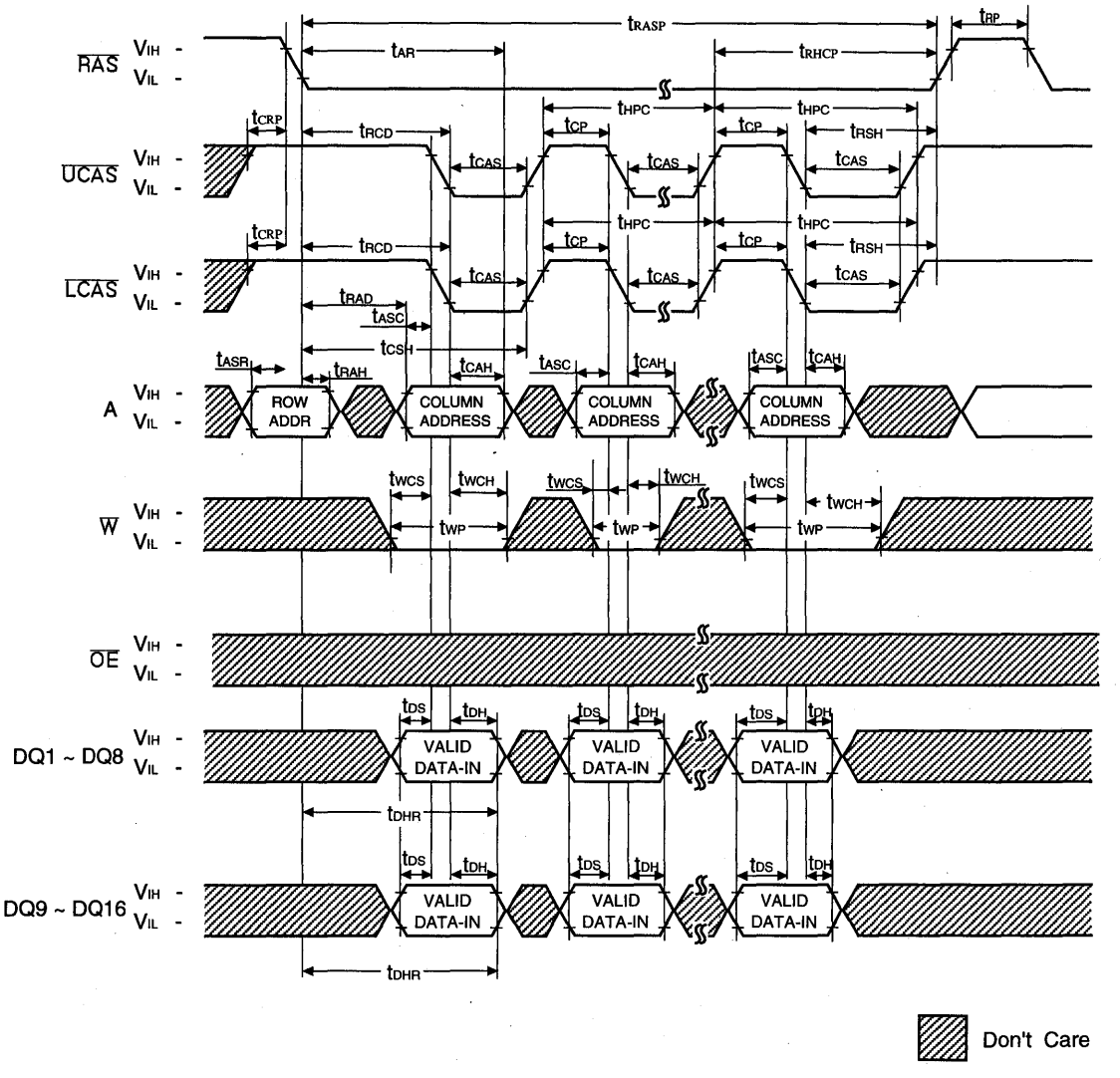


HYPER PAGE MODE UPPER BYTE READ CYCLE



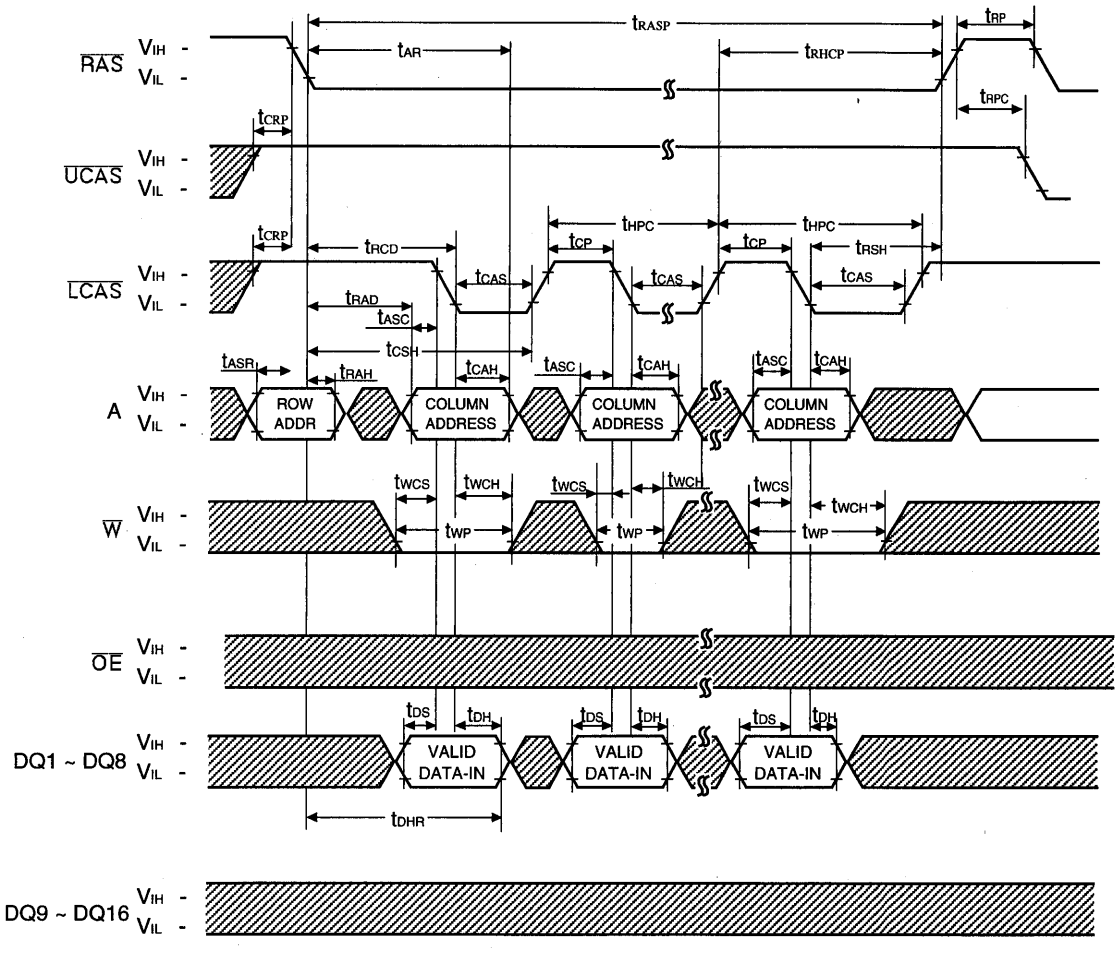
HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



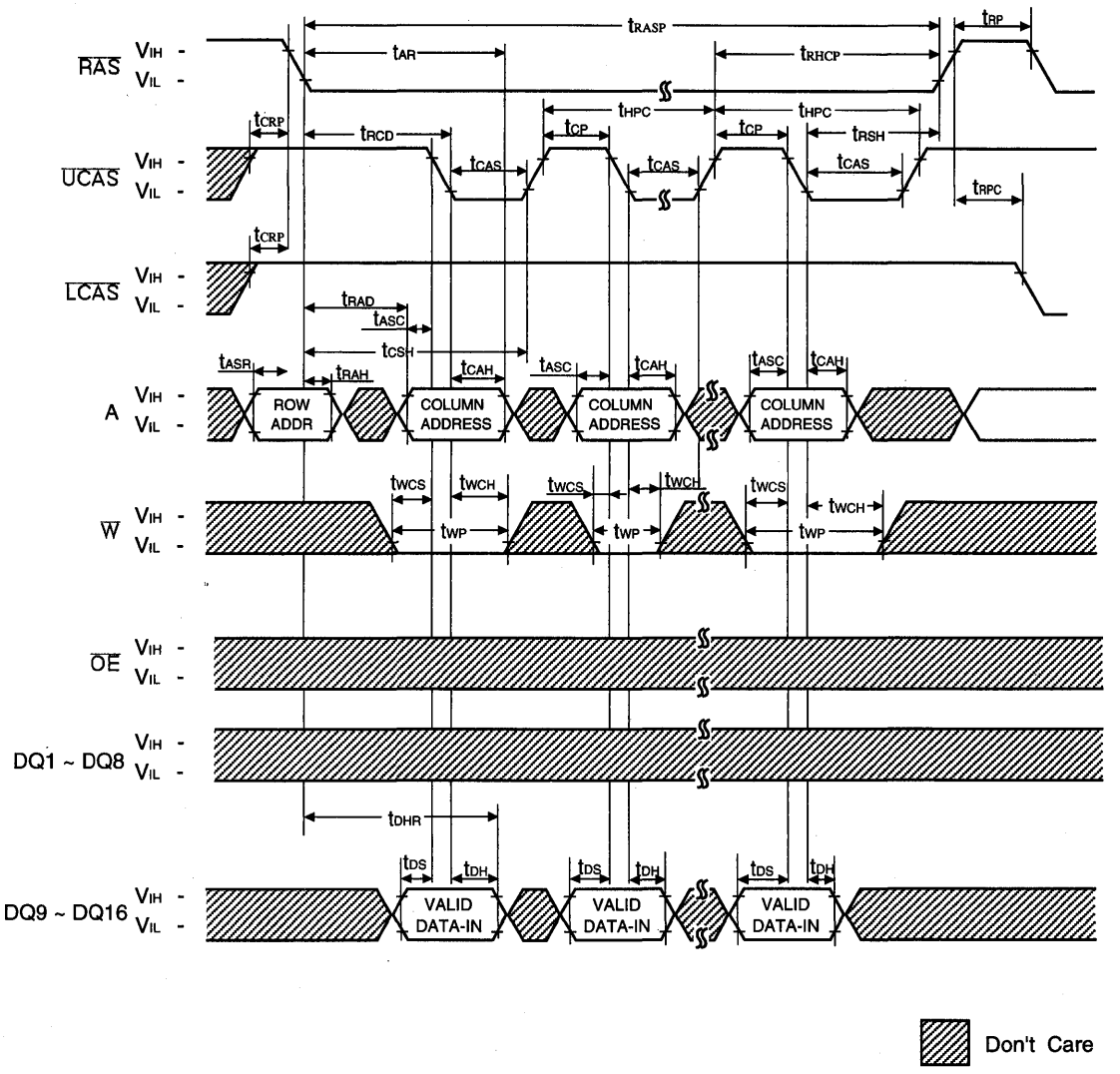
HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open

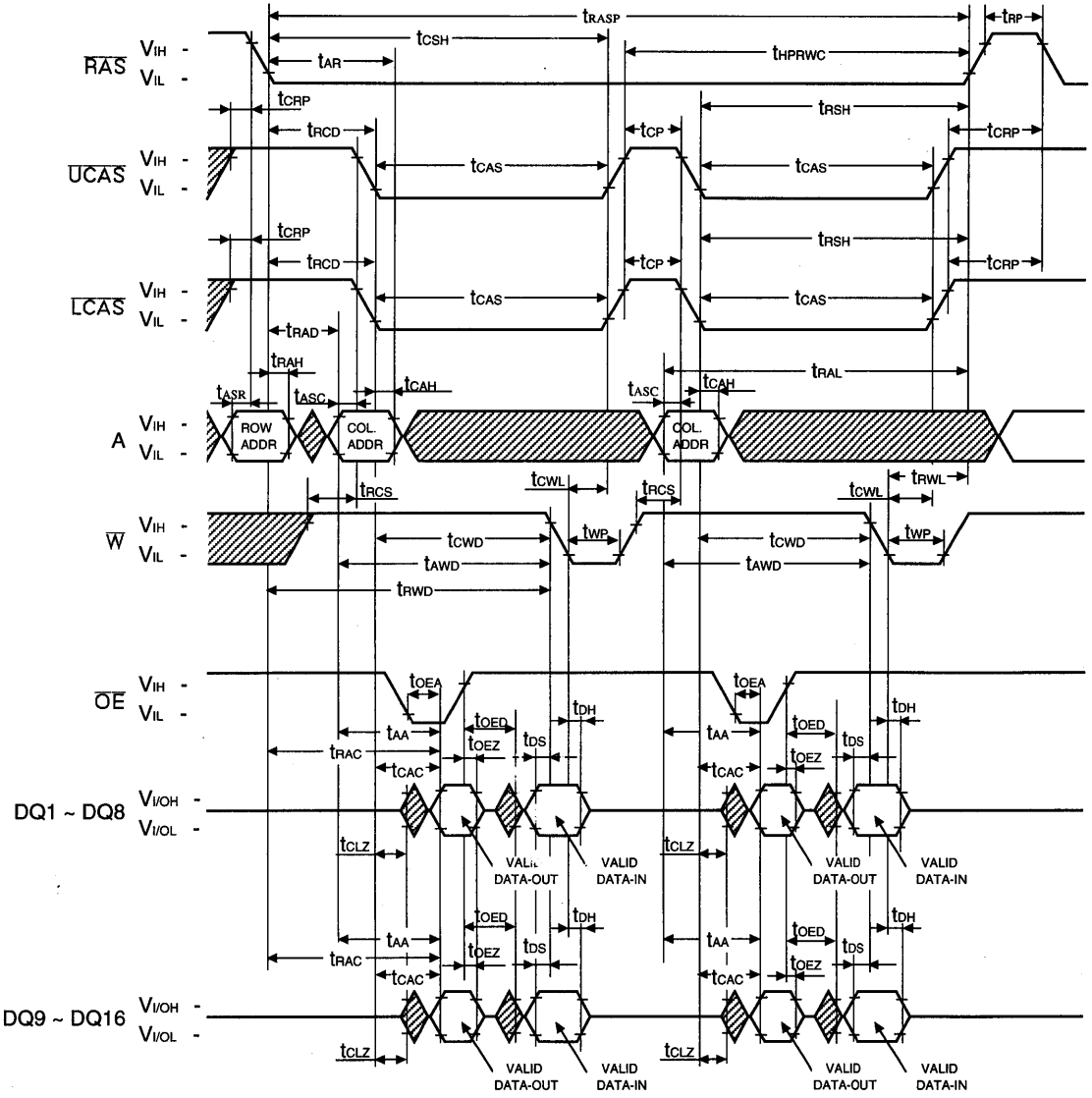


HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

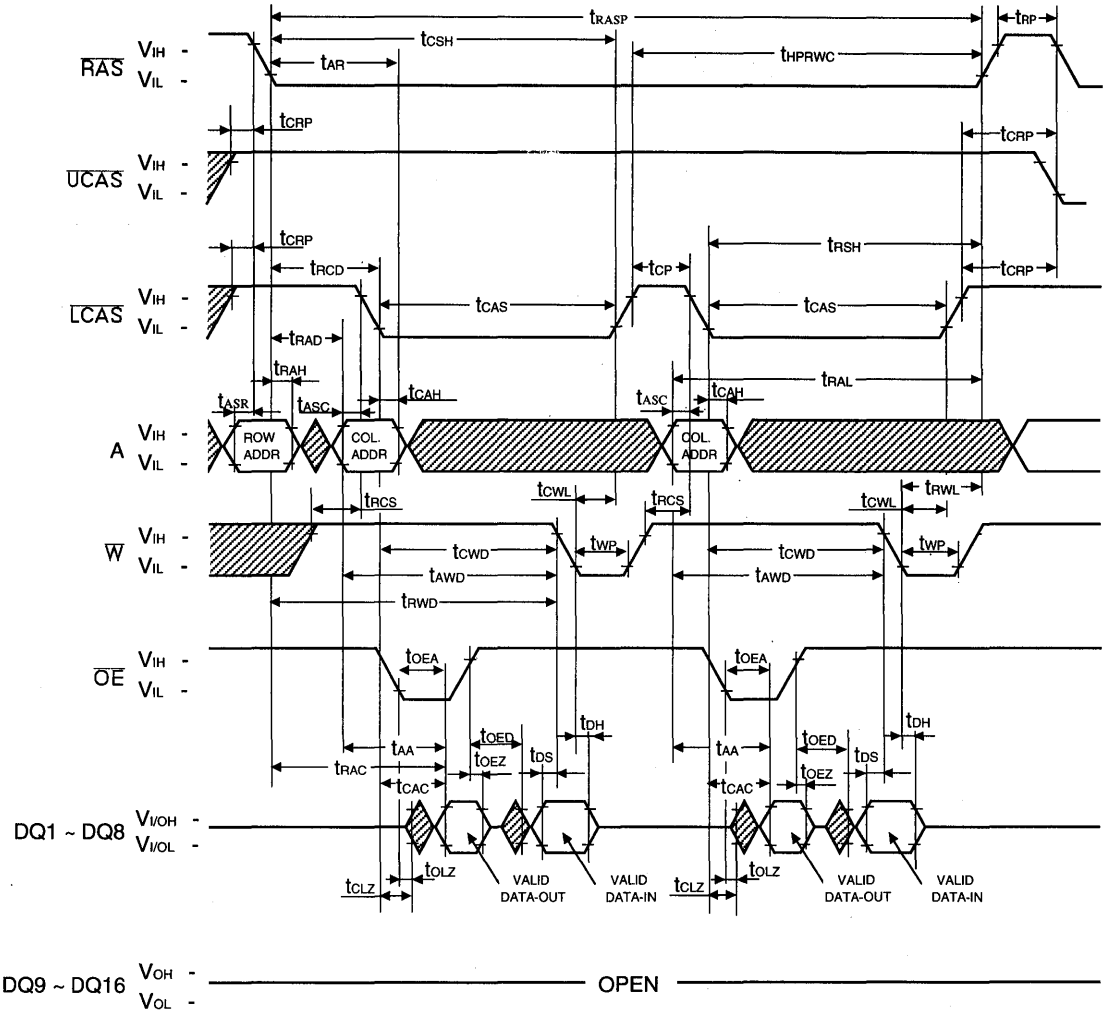
NOTE : D_{OUT} = Open



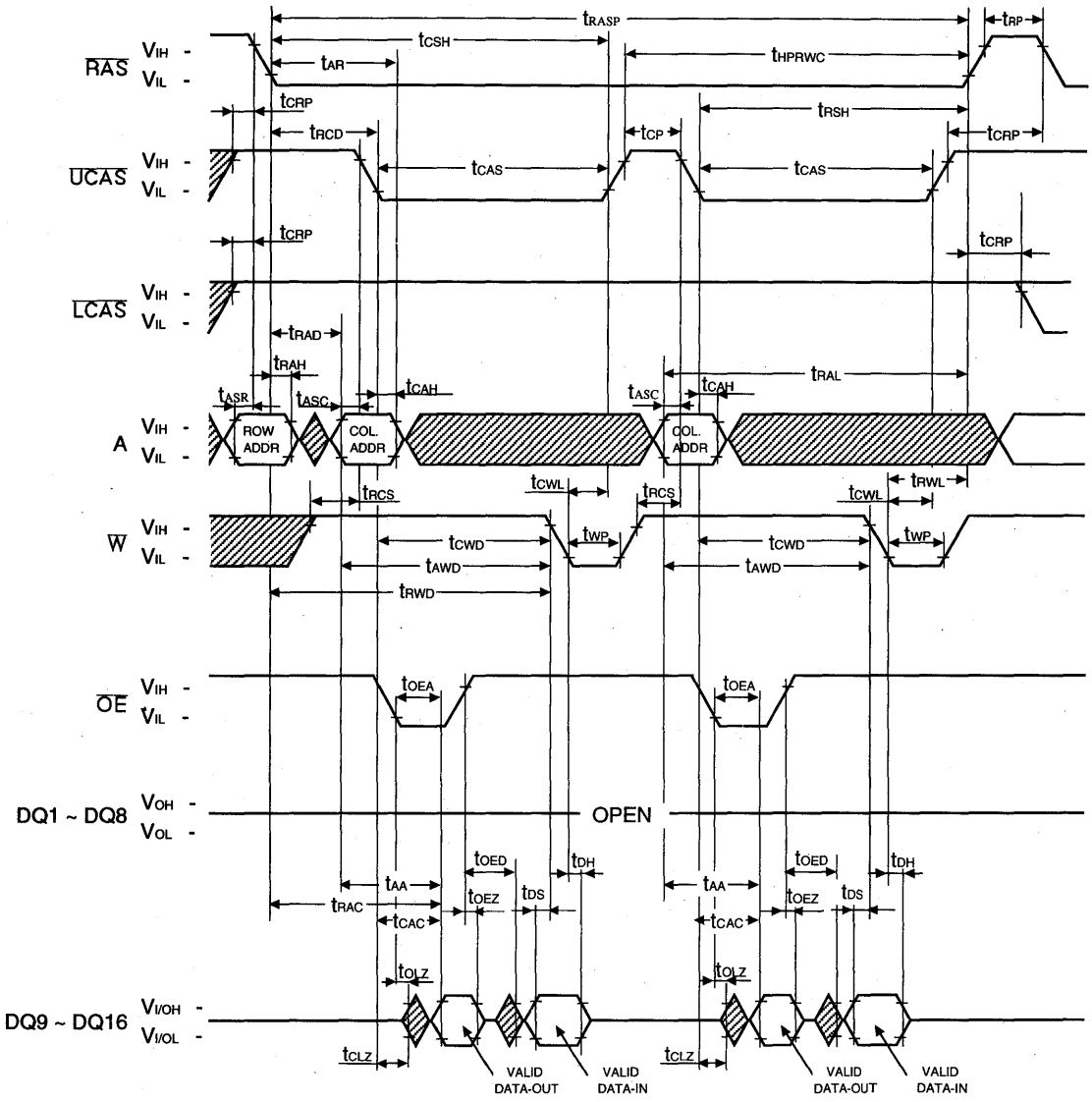
HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE



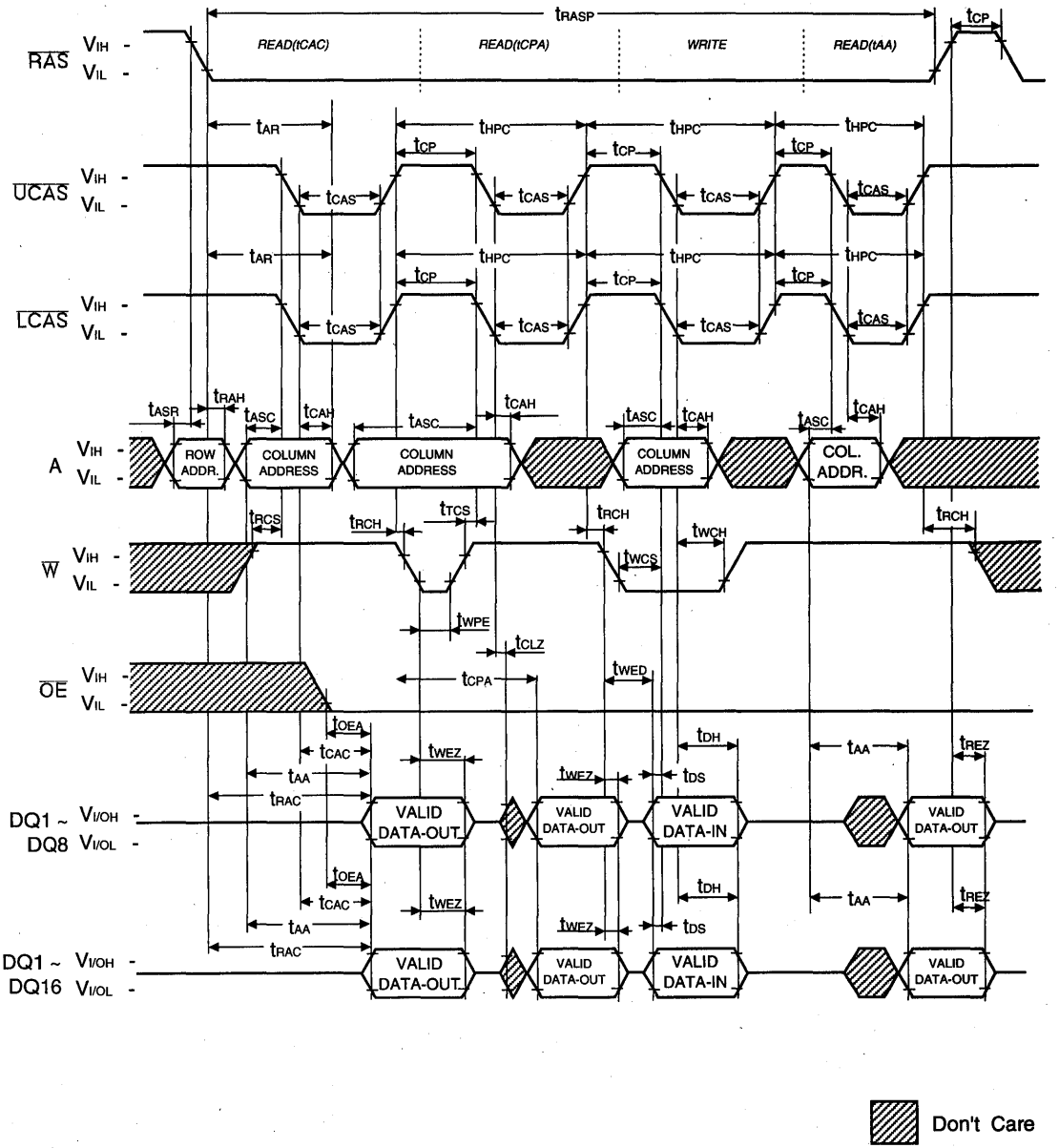
HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE

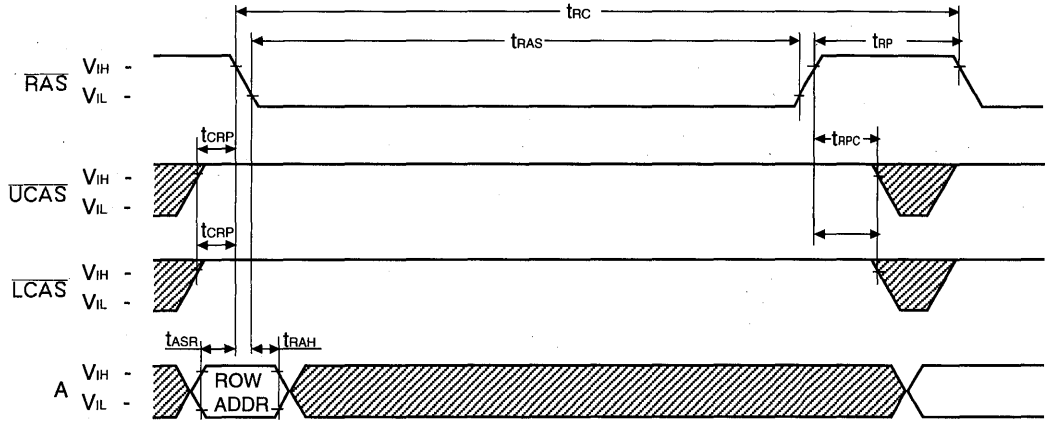


HYPER PAGE READ AND WRITE MIXED CYCLE



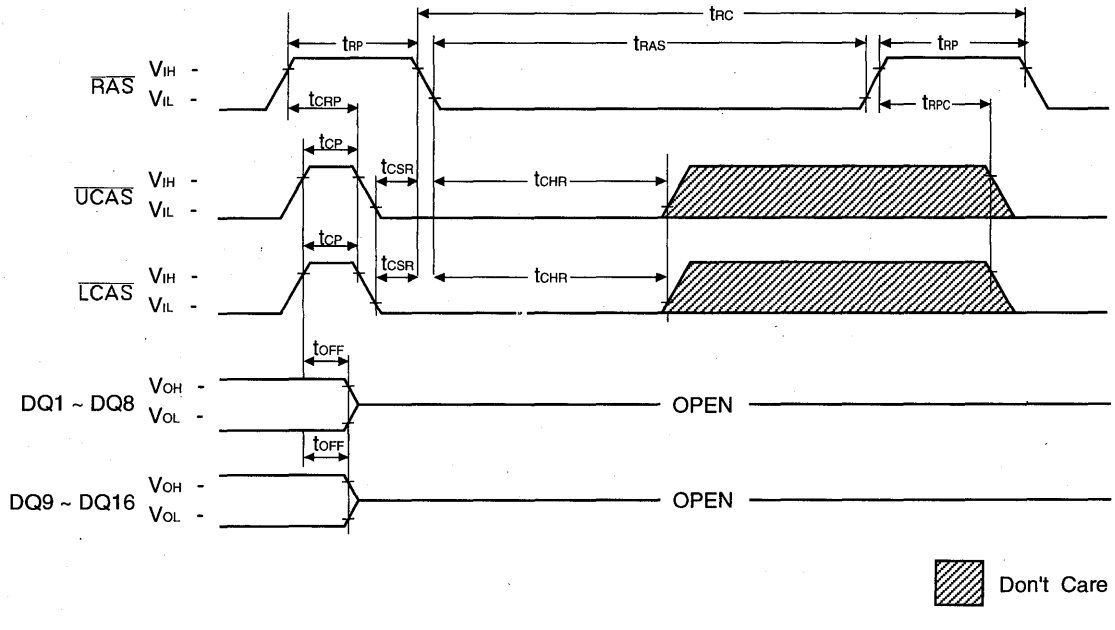
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



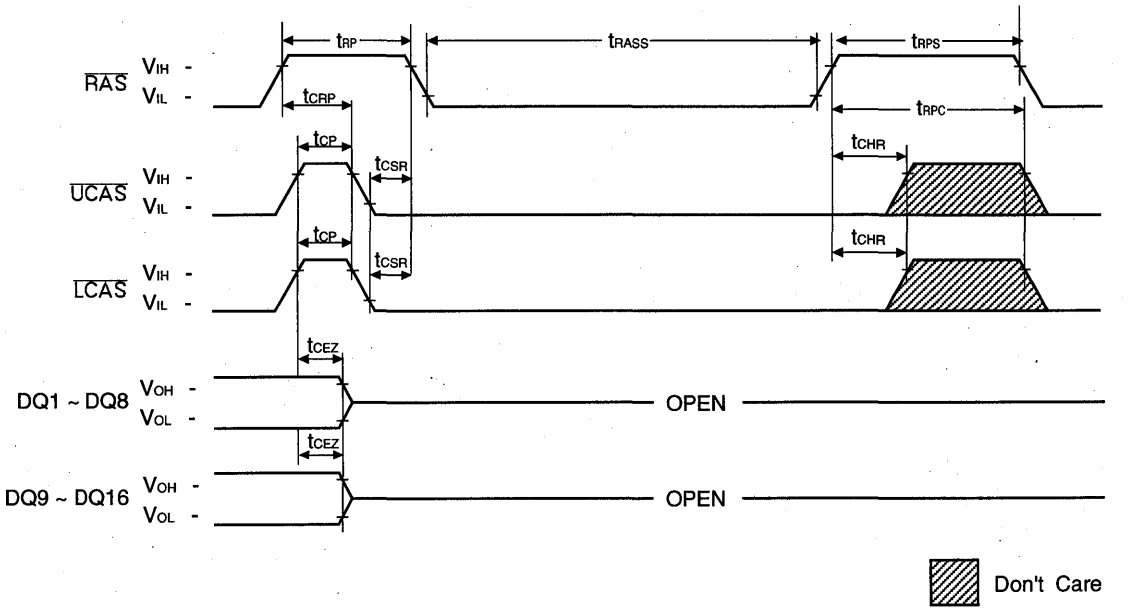
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

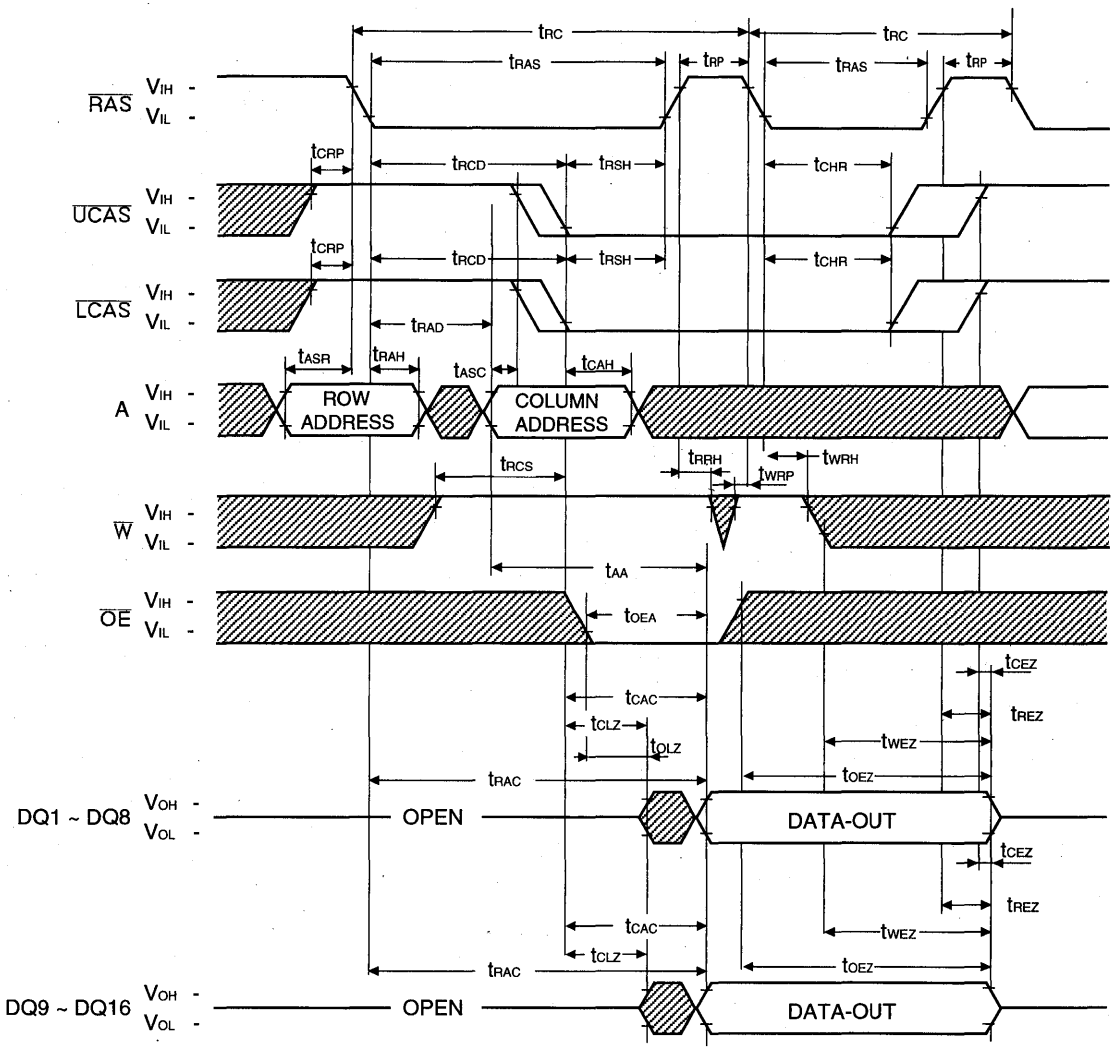


$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE(LL-version)

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

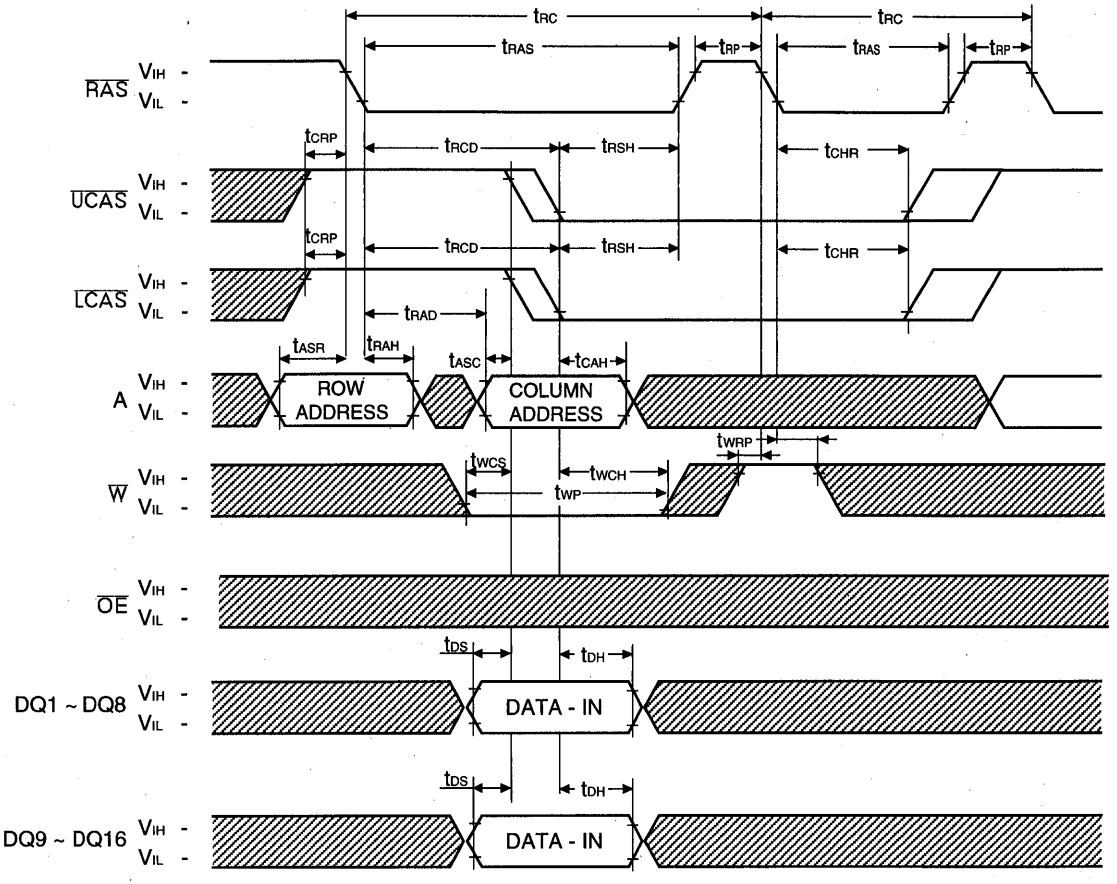


HIDDEN REFRESH CYCLE (READ)



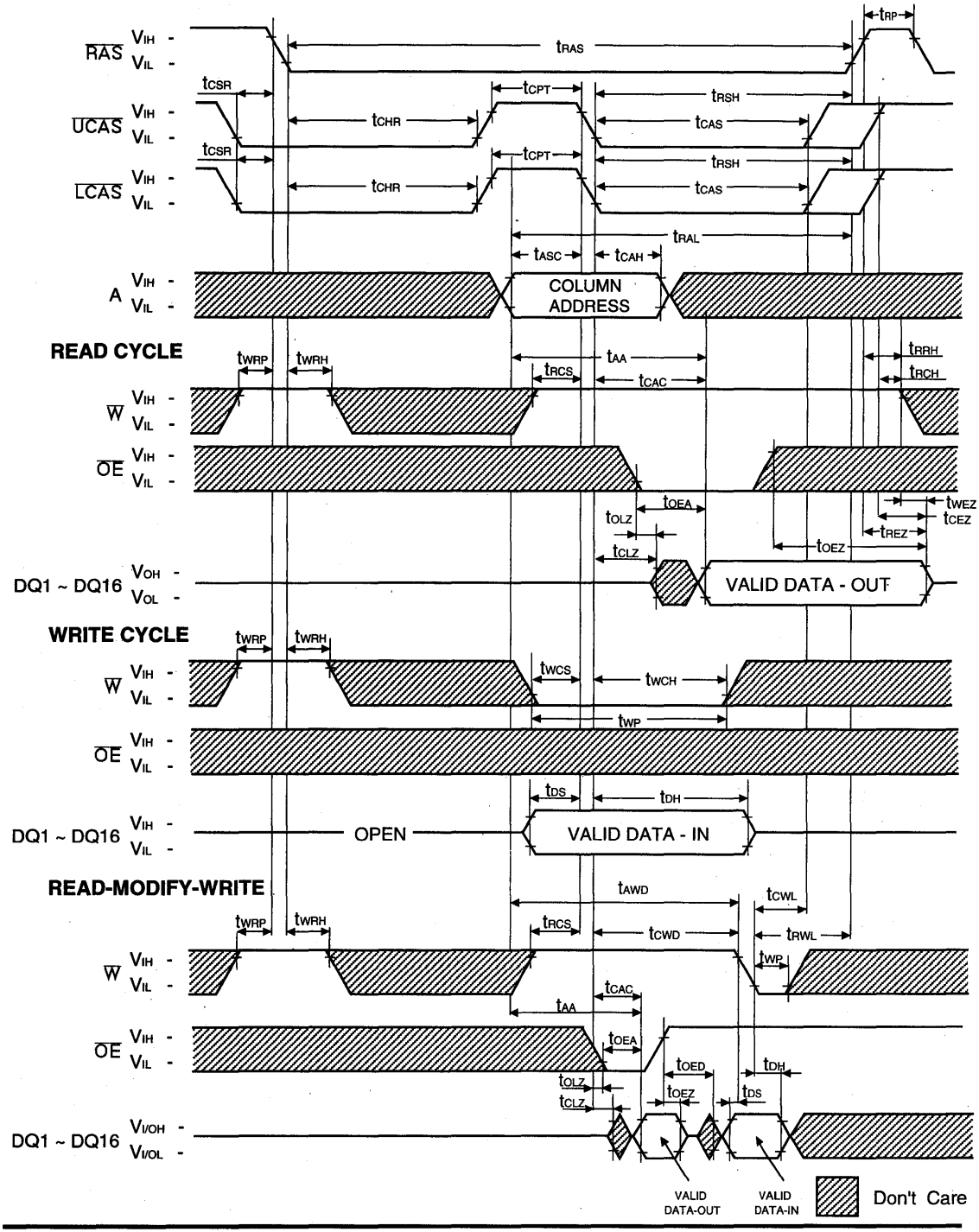
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



Don't Care

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

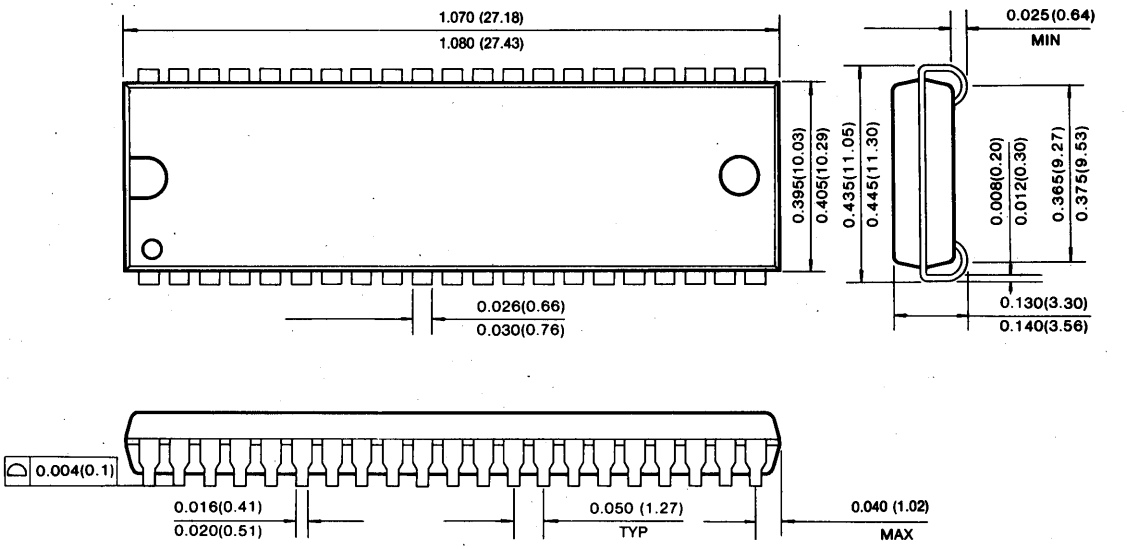


SAMSUNG ELECTRONICS

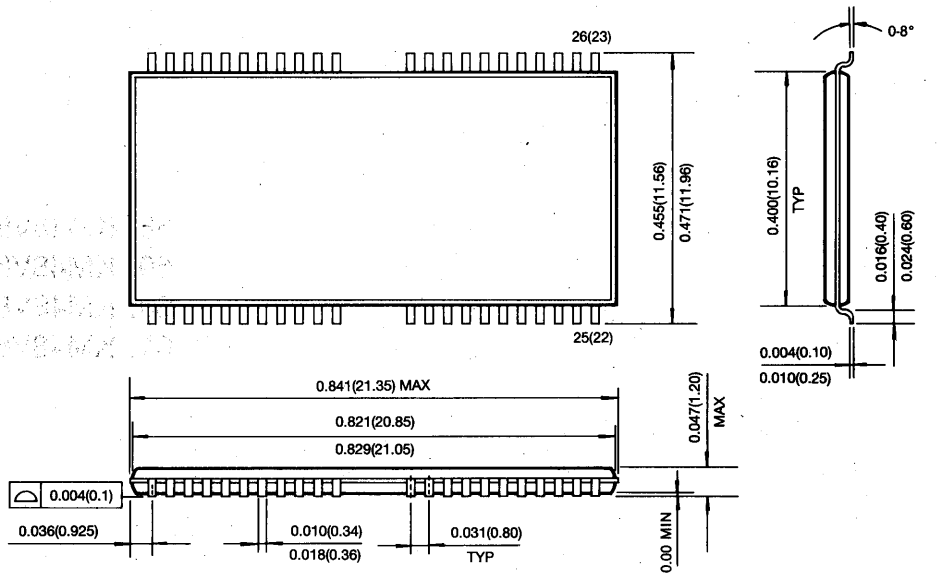
PACKAGE DIMENSION

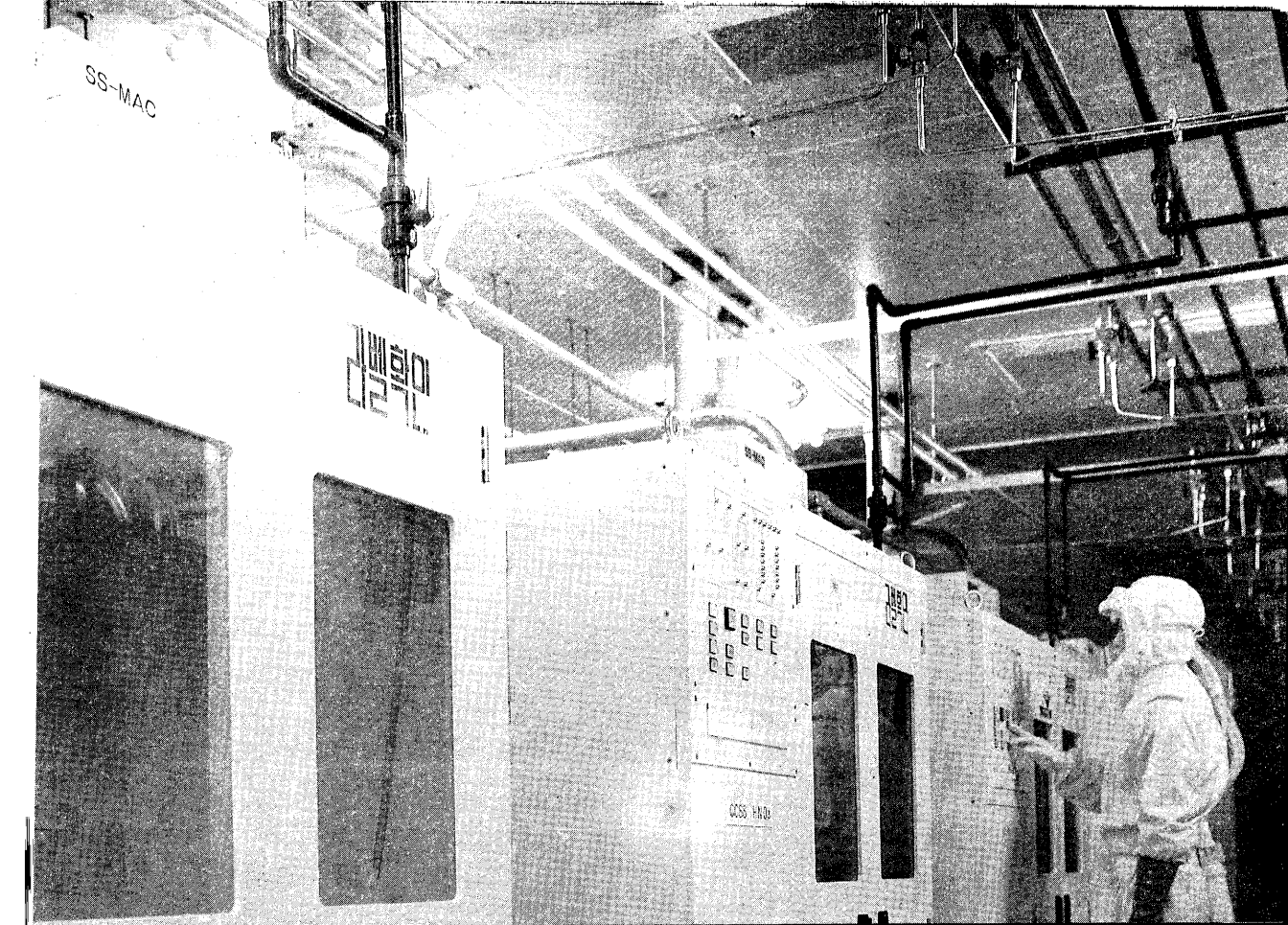
42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)





64M DRAM DATA SHEET 7

58. KM48V8000
59. KM4[illegible]
60. KM[illegible]
61. KM[illegible]

8M x 8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM48V8000-5	50ns	13ns	90ns
KM48V8000-6	60ns	15ns	110ns
KM48V8000-7	70ns	20ns	130ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **3.3V±0.3V power supply**
- **8192 cycles/128ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages.**

GENERAL DESCRIPTION

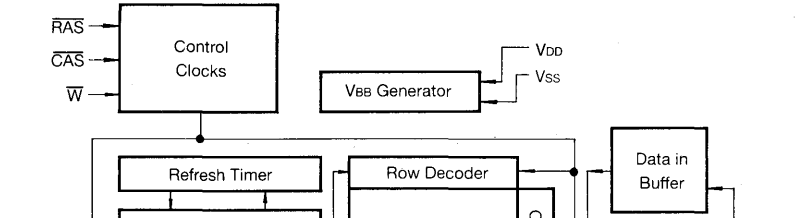
The Samsung KM48V8000 is a high speed CMOS 8,388,608 bit x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48V8000 features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48V8000 is fabricated using Samsung's advanced CMOS process

FUNCTIONAL BLOCK DIAGRAM



7

8M x 8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM48V8004-5	50ns	13ns	90ns	20ns
KM48V8004-6	60ns	15ns	110ns	24ns
KM48V8004-7	70ns	20ns	130ns	29ns

- **Fast Page Mode operation with Extended data out**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **3.3V$\pm$0.3V power supply**
- **8192 cycles/128ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages.**

GENERAL DESCRIPTION

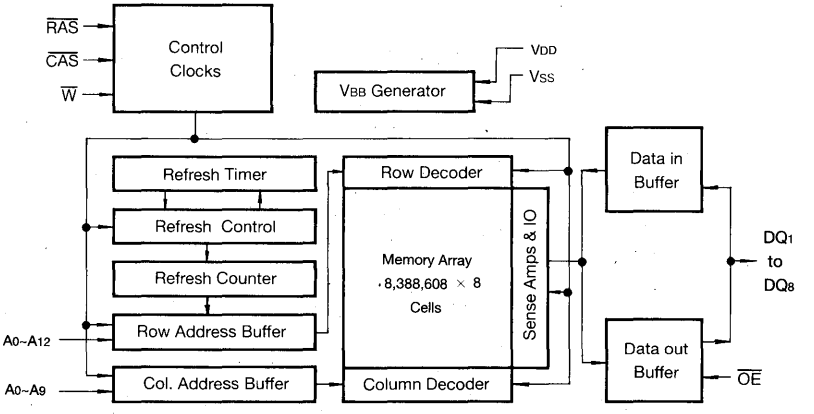
The Samsung KM48V8004 is a high speed CMOS 8,388,608 bit x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, minicomputers, graphics and high performance portable computers.

The KM48V8004 features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48V8004 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



8M x 8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM48V8100-5	50ns	13ns	90ns
KM48V8100-6	60ns	15ns	110ns
KM48V8100-7	70ns	20ns	130ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **3.3V±0.3V power supply**
- **4096 cycles/64ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages.**

GENERAL DESCRIPTION

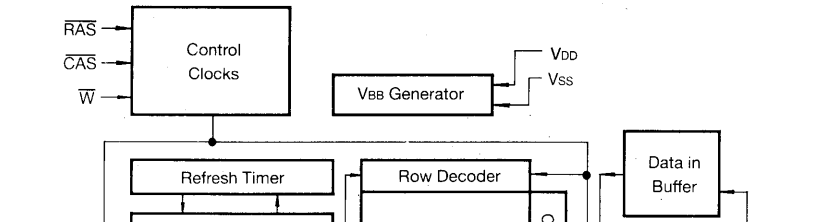
The Samsung KM48V8100 is a high speed CMOS 8,388,608 bit x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainfremes, minicomputers, graphics and high performance portable computers.

The KM48V8100 features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48V8100 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



8M x 8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM48V8104-5	50ns	13ns	90ns	20ns
KM48V8104-6	60ns	15ns	110ns	24ns
KM48V8104-7	70ns	20ns	130ns	29ns

- **Fast Page Mode operation with Extended data out**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$ only and Hidden Refresh capability**
- **Fast parallel test mode capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **3.3V±0.3V power supply**
- **4096 cycles/64ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages.**

GENERAL DESCRIPTION

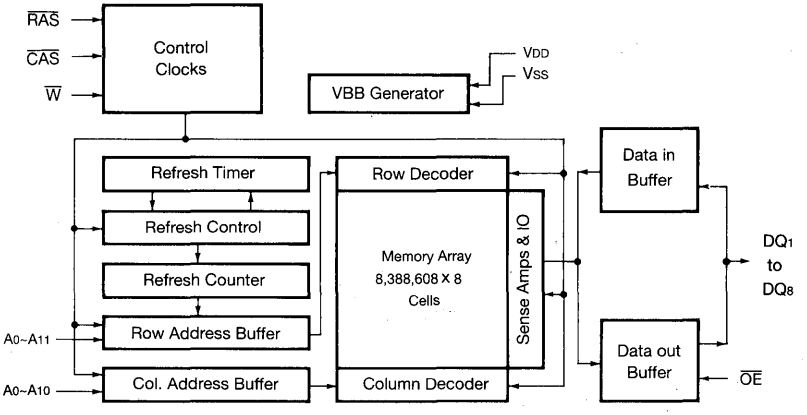
The Samsung KM48V8104 is a high speed CMOS 8,388,608 bit x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, minicomputers, graphics and high performance portable computers.

The KM48V8104 features EDO Mode operation which allows high speed random access of memory cells within the same row.

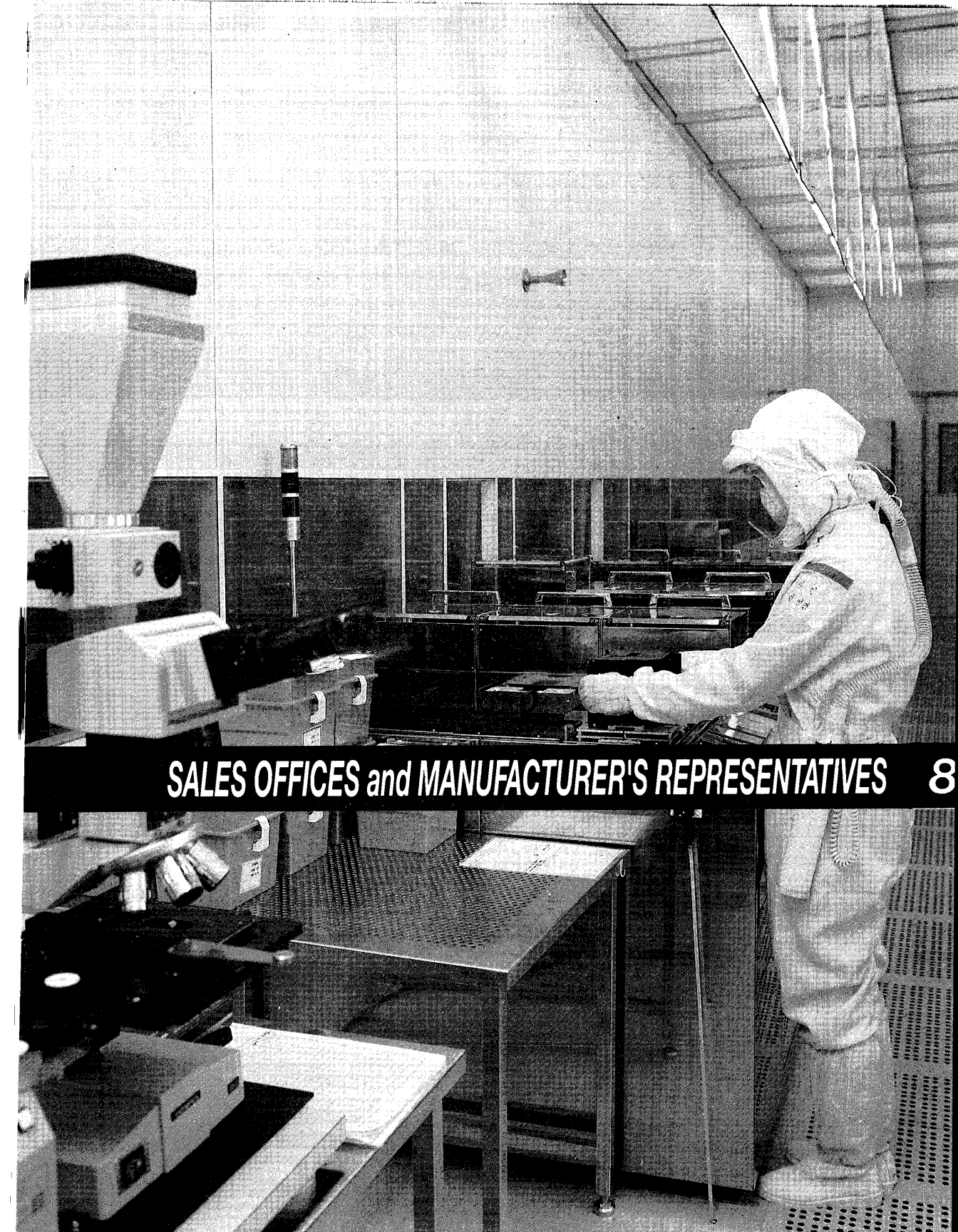
$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48V8104 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS



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Suite 130
Ft. Wayne, IN 46804

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Lenexa, KS 66215 — FAX: (913) 888-4848

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