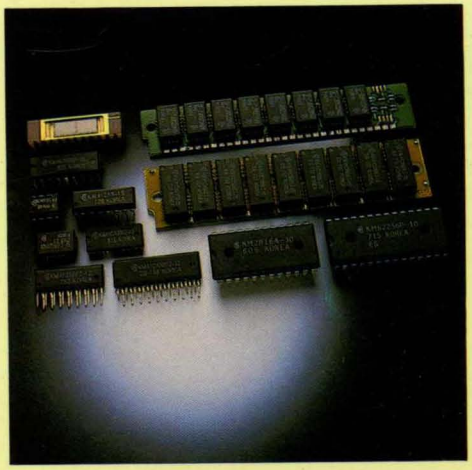
SAMSUNG

MOS Memory Data Book



1988

SAMSUNG SEMICONDUCTOR DATA BOOK LIST

I. Semiconductor Product Guide

II. Transistor Data Book

- Vol. 1: Small Signal TR
- Vol. 2: Bipolar Power TR
- Vol. 3: TR Pellet

III. Linear IC Data Book

- Vol. 1: Audio/Video
- Vol. 2: Telecom/Industrial/Data Converter IC

IV. MOS Product Data Book

V. High Performance CMOS Logic Data Book

VI. MOS Memory Data Book

VII. SFET Data Book

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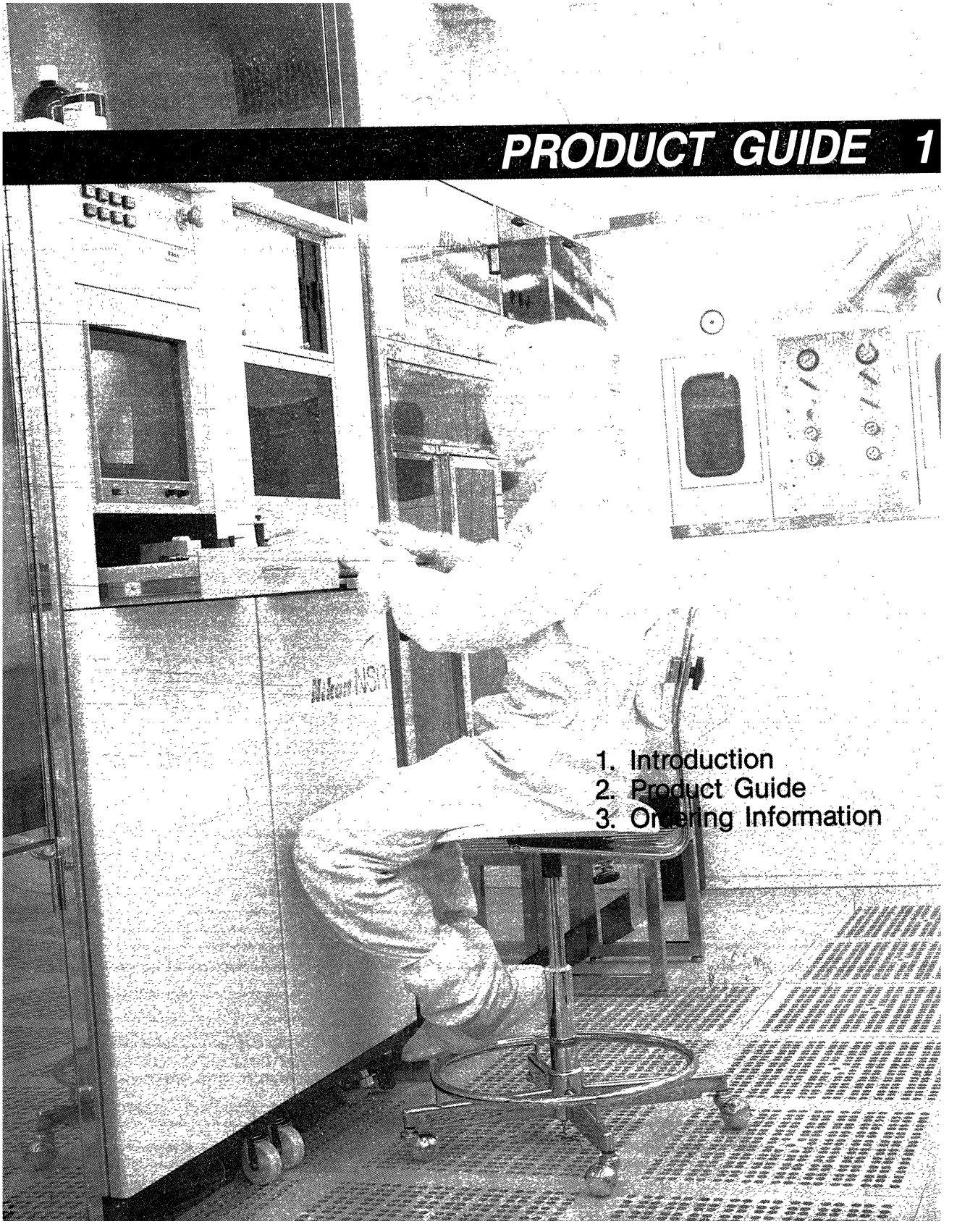
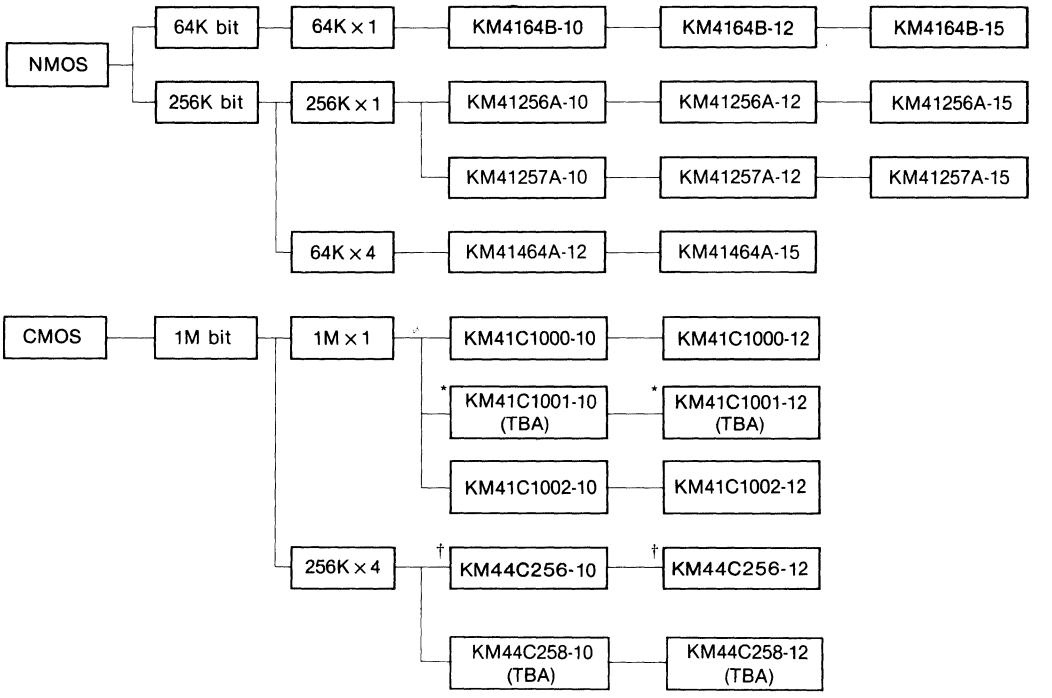
PRODUCT GUIDE 1



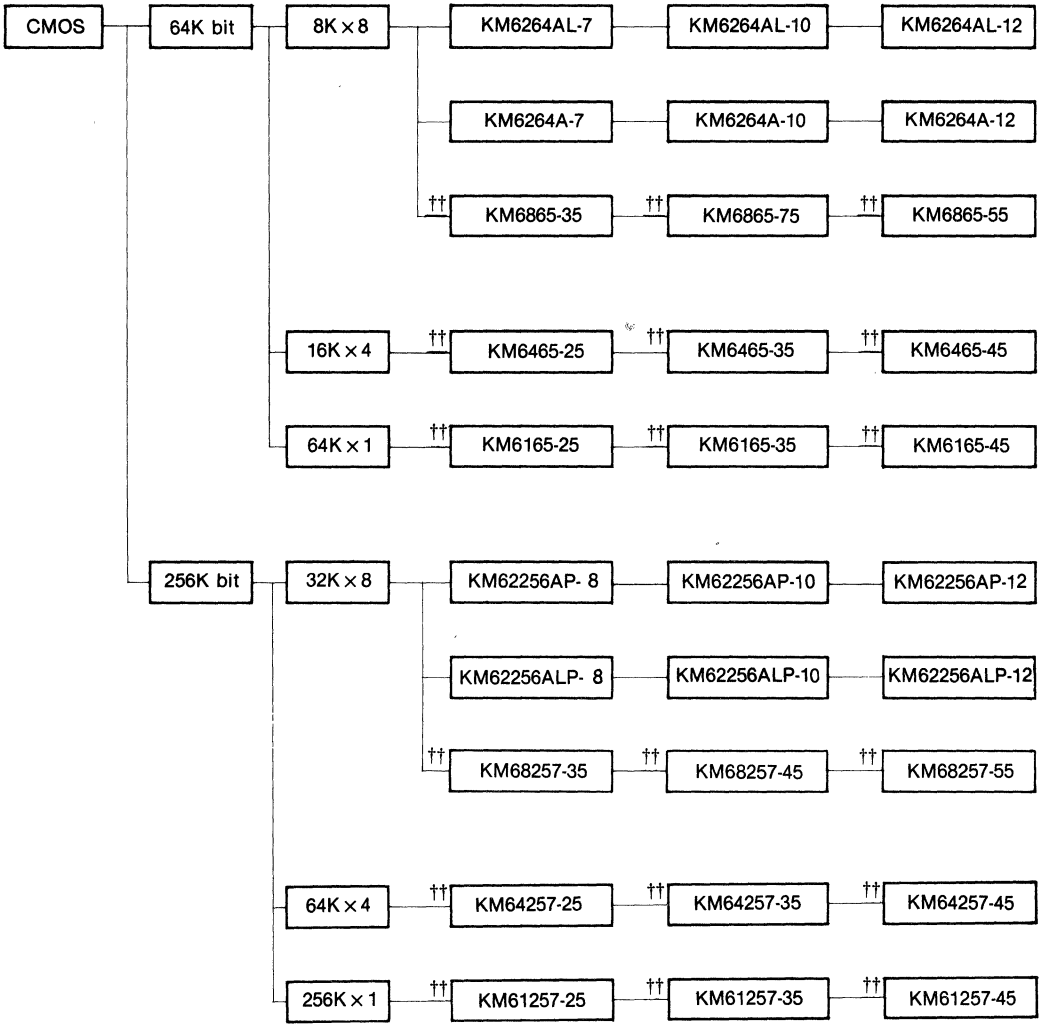
1. INTRODUCTION

1.1 Dynamic RAM



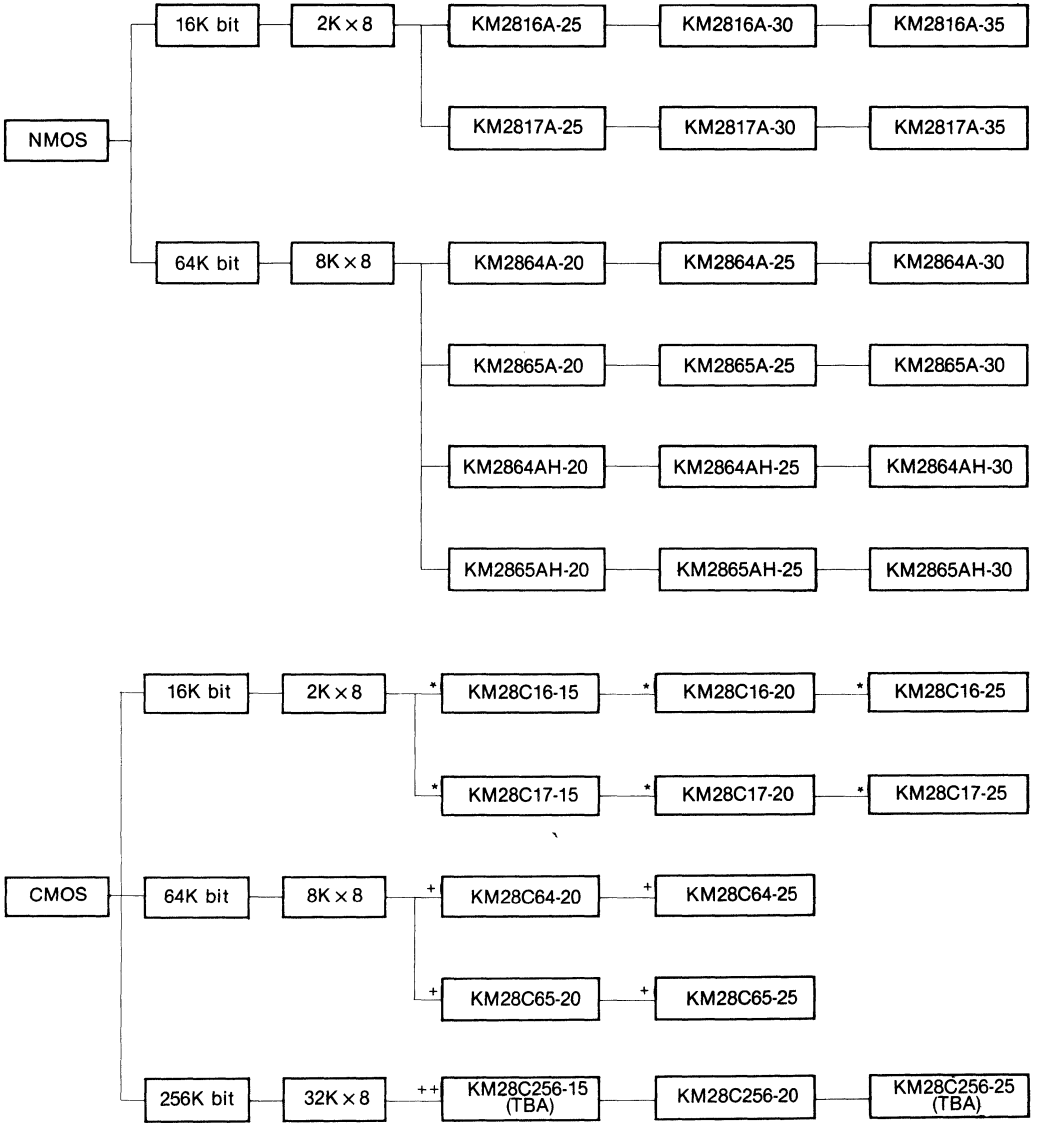
† New Product
* Preliminary Product
†† Under Development
(TBA): To Be Announced

1.2 Static RAM



† New Product
* Preliminary Product
††Under Development
(TBA): To Be Announced

1.3 EEPROM



† New Product
* Preliminary Product
††Under Development
(TBA): To Be Announced

2. PRODUCT GUIDE

2.1 Dynamic RAM

Capacity	Part Number	Organization	Speed (ns)	Technology	Features	Packages	Remark
64K bit	KM4164B-12	64K × 1	120	NMOS	Page Mode	16-Pin DIP	Now
	KM4164B-15	64K × 1	150	NMOS	Page Mode	16-Pin DIP	Now
256K bit	KM41256AP-12	256K × 1	120	NMOS	Page Mode	16-Pin DIP	Now
	KM41256AP-15	256K × 1	150	NMOS	Page Mode	16-Pin DIP	Now
	KM41256AJ-12	256K × 1	120	NMOS	Page Mode	18-Pin PLCC	Now
	KM41256AJ-15	256K × 1	150	NMOS	Page Mode	18-Pin PLCC	Now
	KM41256AZ-12	256K × 1	120	NMOS	Page Mode	16-Pin ZIP	Now
	KM41256AZ-15	256K × 1	150	NMOS	Page Mode	16-Pin ZIP	Now
	KM41257AP-12	256K × 1	120	NMOS	Nibble Mode	16-Pin DIP	Now
	KM41257AP-15	256K × 1	150	NMOS	Nibble Mode	16-Pin DIP	Now
	KM41257AJ-12	256K × 1	120	NMOS	Nibble Mode	18-Pin PLCC	Now
	KM41257AJ-15	256K × 1	150	NMOS	Nibble Mode	18-Pin PLCC	Now
	KM41257AZ-12	256K × 1	120	NMOS	Nibble Mode	16-Pin ZIP	Now
	KM41257AZ-15	256K × 1	150	NMOS	Nibble Mode	16-Pin ZIP	Now
	KM41464AP-12	64K × 4	120	NMOS	Page Mode	18-Pin DIP	Now
	KM41464AP-15	64K × 4	150	NMOS	Page Mode	18-Pin DIP	Now
	KM41464AJ-12	64K × 4	120	NMOS	Page Mode	18-Pin PLCC	Now
	KM41464AJ-15	64K × 4	150	NMOS	Page Mode	18-Pin PLCC	Now
	KM41464AZ-12	64K × 4	120	NMOS	Page Mode	20-Pin ZIP	Now
	KM41464AZ-15	64K × 4	150	NMOS	Page Mode	20-Pin ZIP	Now
1M bit	KM41C1000P-10	1M × 1	100	CMOS	Fast Page Mode	18-Pin DIP	Now
	KM41C1000P-12	1M × 1	120	CMOS	Fast Page Mode	18-Pin DIP	Now
	KM41C1000J-10	1M × 1	100	CMOS	Fast Page Mode	20-Pin SOJ	Now
	KM41C1000J-12	1M × 1	120	CMOS	Fast Page Mode	20-Pin SOJ	Now
	KM41C1000Z-10	1M × 1	100	CMOS	Fast Page Mode	20-Pin ZIP	Now
	KM41C1000Z-12	1M × 1	120	CMOS	Fast Page Mode	20-Pin ZIP	Now
	KM41C1002P-10	1M × 1	100	CMOS	S. Column Mode	18-Pin DIP	Now
	KM41C1002P-12	1M × 1	120	CMOS	S. Column Mode	18-Pin DIP	Now
	†KM44C256J-10	256K × 4	100	CMOS	Fast Page Mode	20-Pin SOJ	Now
	†KM44C256J-12	256K × 4	120	CMOS	Fast Page Mode	20-Pin SOJ	Now

* KM41C1001 (Nibble Mode) and KM44C258 (Static Column Mode) are available in Q4,'88.

2.2 Dynamic RAM MODULE

Part Number	Organization	Speed (ns)	Technology	Features	Packages	Remark
KMM48256-12	256K × 8	120	NMOS	Page Mode	30-Pin SIP	Call Factory
KMM48256-15	256K × 8	150	NMOS	Page Mode	30-Pin SIP	Call Factory
KMM58256-12	256K × 8	120	NMOS	Page Mode	30-Pin SIMM (Edge Connector)	Call Factory
KMM58256-15	256K × 8	150	NMOS	Page Mode	30-Pin SIMM (Edge Connector)	Call Factory
KMM49256-12	256K × 9	120	NMOS	Page Mode	30-Pin SIP	Call Factory
KMM49256-15	256K × 9	150	NMOS	Page Mode	30-Pin SIP	Call Factory
KMM59256-12	256K × 9	120	NMOS	Page Mode	30-Pin SIMM (Edge Connector)	Call Factory
KMM59256-15	256K × 9	150	NMOS	Page Mode	30-Pin SIMM (Edge Connector)	Call Factory

† New Product

2.2 Dynamic RAM MODULE (Continued)

Part Number	Organization	Speed (ns)	Technology	Features	Packages	Remark
KMM481000-10	1M × 8	100	CMOS	Fast Page Mode	30-Pin SIP	Call Factory
KMM481000-12	1M × 8	120	CMOS	Fast Page Mode	30-Pin SIP	Call Factory
KMM581000-10	1M × 8	100	CMOS	Fast Page Mode	30-Pin SIMM (Edge Connector)	Call Factory
KMM581000-12	1M × 8	120	CMOS	Fast Page Mode	30-Pin SIMM (Edge Connector)	Call Factory
KMM491000-10	1M × 9	100	CMOS	Fast Page Mode	30-Pin SIP	Call Factory
KMM491000-12	1M × 9	120	CMOS	Fast Page Mode	30-Pin SIP	Call Factory
KMM591000-10	1M × 9	100	CMOS	Fast Page Mode	30-Pin SIMM (Edge Connector)	Call Factory
KMM591000-12	1M × 9	120	CMOS	Fast Page Mode	30-Pin SIMM (Edge Connector)	Call Factory

2.3 Static RAM

Capacity	Part Number	Organization	Speed (ns)	Technology	Current		Packages	Remark
					Active, mA Typ (max)	Standby, μA Typ (max)		
64K bit	†KM6264A-7	8K × 8	70	CMOS	35 (70)	(1mA)	28-Pin DIP	Now
	KM6264A-10	8K × 8	100	CMOS	35 (70)	(1mA)	28-Pin DIP	Now
	KM6264A-12	8K × 8	120	CMOS	35 (70)	(1mA)	28-Pin DIP	Now
	†KM6264AL-7	8K × 8	70	CMOS	35 (70)	(1mA)	28-Pin DIP	Now
	KM6264AL-10	8K × 8	100	CMOS	35 (70)	2 (0.1mA)	28-Pin DIP	Now
	KM6264AL-12	8K × 8	120	CMOS	35 (70)	2 (0.1mA)	28-Pin DIP	Now
64K bit	††KM6165-25	64K × 1	25	CMOS	(100)	(100)	22-Pin SDIP	under development
	KM6165-35	64K × 1	35	CMOS	(100)	(100)	22-Pin SDIP	under development
	KM6165-45	64K × 1	45	CMOS	(100)	(100)	22-Pin SDIP	under development
	KM6465-25	16K × 4	25	CMOS	(100)	(100)	22-Pin SDIP	under development
	KM6465-35	16K × 4	35	CMOS	(100)	(100)	22-Pin SDIP	under development
	KM6465-45	16K × 4	45	CMOS	(100)	(100)	22-Pin SDIP	under development
	KM6865-35	8K × 8	35	CMOS	(100)	(100)	28-Pin SDIP	under development
	KM6865-45	8K × 8	45	CMOS	(100)	(100)	28-Pin SDIP	under development
	KM6865-55	8K × 8	55	CMOS	(100)	(100)	28-Pin SDIP	under development
256K bit	KM62256P-10	32K × 8	100	CMOS	35 (60)	(1mA)	28-Pin DIP	Now
	KM62256P-12	32K × 8	120	CMOS	35 (60)	(1mA)	28-Pin DIP	Now
	KM62256P-15	32K × 8	150	CMOS	35 (60)	(1mA)	28-Pin DIP	Now
	KM62256LP-10	32K × 8	100	CMOS	35 (60)	(0.1mA)	28-Pin DIP	Now
	KM62256LP-12	32K × 8	120	CMOS	35 (60)	(0.1mA)	28-Pin DIP	Now
	KM62256LP-15	32K × 8	150	CMOS	35 (60)	(0.1mA)	28-Pin DIP	Now
	††KM61257-25	256K × 1	25	CMOS	(100)	(100)	24-Pin SDIP	under development
	KM61257-35	256K × 1	35	CMOS	(100)	(100)	24-Pin SDIP	under development
	KM61257-45	256K × 1	45	CMOS	(100)	(100)	24-Pin SDIP	under development
	KM64257-25	64K × 4	25	CMOS	(100)	(100)	24-Pin SDIP	under development
	KM64257-35	64K × 4	35	CMOS	(100)	(100)	24-Pin SDIP	under development
	KM64257-45	64K × 4	45	CMOS	(100)	(100)	24-Pin SDIP	under development
	KM68257-35	32K × 8	35	CMOS	(100)	(100)	28-Pin DIP	under development
	KM68257-45	32K × 8	45	CMOS	(100)	(100)	28-Pin DIP	under development
	KM68257-55	32K × 8	55	CMOS	(100)	(100)	28-Pin DIP	under development

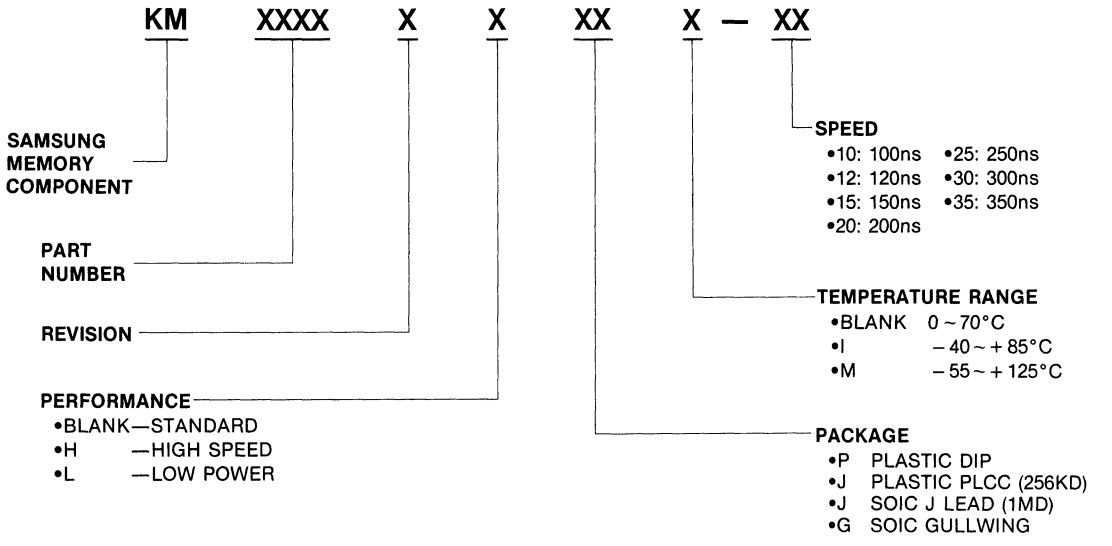
† New Product
†† Under Development

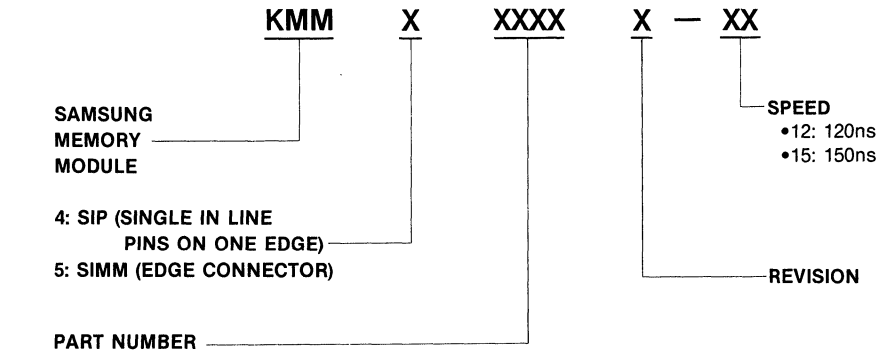
2.4 EEPROM

Capacity	Part Number	Organization	Speed (ns)	Technology	Write Cycle Time (min) (ms)	Features	Packages	Remark
16K bit	KM2816A-25	2K × 8	250	NMOS	10	—	24-Pin DIP	Now
	KM2816A-30	2K × 8	300	NMOS	10	—	24-Pin DIP	Now
	KM2816A-35	2K × 8	350	NMOS	10	—	24-Pin DIP	Now
	KM2817A-25	2K × 8	250	NMOS	10	Ready/Busy	28-Pin DIP	Now
	KM2817A-30	2K × 8	300	NMOS	10	Ready/Busy	28-Pin DIP	Now
	KM2817A-35	2K × 8	350	NMOS	10	Ready/Busy	28-Pin DIP	Now
	†KM28C16-15	2K × 8	150	CMOS	2	Ready/Busy	24-Pin DIP	under development
	†KM28C16-20	2K × 8	200	CMOS	2	Ready/Busy	24-Pin DIP	under development
	†KM28C16-25	2K × 8	250	CMOS	2	Ready/Busy	24-Pin DIP	under development
	†KM28C17-15	2K × 8	150	CMOS	2	Ready/Busy	28-Pin DIP	under development
	†KM28C17-20	2K × 8	200	CMOS	2	Ready/Busy	28-Pin DIP	under development
	†KM28C17-25	2K × 8	250	CMOS	2	Ready/Busy	28-Pin DIP	under development
64K bit	KM2864A-20	8K × 8	200	NMOS	10	Data Polling	28-Pin DIP	Now
	KM2864A-25	8K × 8	250	NMOS	10	Data Polling	28-Pin DIP	Now
	KM2864A-30	8K × 8	300	NMOS	10	Data Polling	28-Pin DIP	Now
	KM2865A-20	8K × 8	200	NMOS	10	Data Polling, Ready/Busy	28-Pin DIP	Now
	KM2865A-25	8K × 8	250	NMOS	10	Data Polling, Ready/Busy	28-Pin DIP	Now
	KM2865A-30	8K × 8	300	NMOS	10	Data Polling, Ready/Busy	28-Pin DIP	Now
	KM2864AH-20	8K × 8	200	NMOS	2	Data Polling	28-Pin DIP	Now
	KM2864AH-25	8K × 8	250	NMOS	2	Data Polling	28-Pin DIP	Now
	KM2864AH-30	8K × 8	300	NMOS	2	Data Polling	28-Pin DIP	Now
	KM2865AH-20	8K × 8	200	NMOS	2	Data Polling, Ready/Busy	28-Pin DIP	Now
	KM2865AH-25	8K × 8	250	NMOS	2	Data Polling, Ready/Busy	28-Pin DIP	Now
	KM2865AH-30	8K × 8	300	NMOS	2	Data Polling, Ready/Busy	28-Pin DIP	Now
	KM28C64-20	8K × 8	200	CMOS	5	Data Polling, Page Mode	28-Pin DIP	Now
	KM28C64-25	8K × 8	250	CMOS	5	Data Polling, Page Mode	28-Pin DIP	Now
	KM28C65-20	8K × 8	200	CMOS	5	Ready/Busy, Page Mode	28-Pin DIP	Now
	KM28C65-25	8K × 8	250	CMOS	5	Ready/Busy, Page Mode	28-Pin DIP	Now
256K	††KM28C256-15	32K × 8	130	CMOS	5	Data Polling, Toggle bit	28-Pin DIP	under development
	††KM28C256-20	32K × 8	200	CMOS	5	Data Polling, Toggle bit	28-Pin DIP	under development
	††KM28C256-25	32K × 8	250	CMOS	5	Data Polling, Toggle bit	28-Pin DIP	under development

† New Product
††Under Development

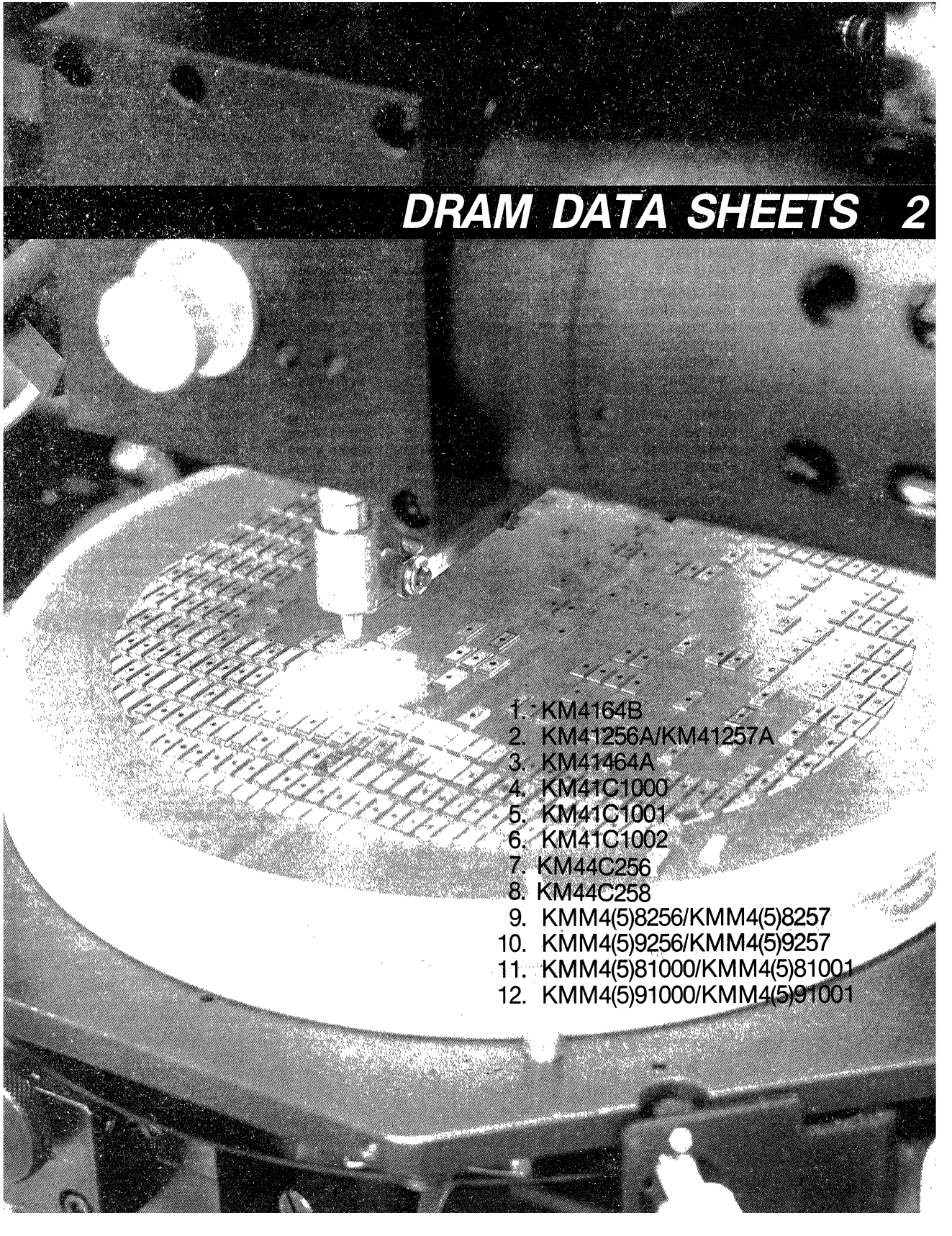
3. ORDERING INFORMATION





NOTES

DRAM DATA SHEETS 2



1. KM4164B
2. KM41256A/KM41257A
3. KM41464A
4. KM41C1000
5. KM41C1001
6. KM41C1002
7. KM44C256
8. KM44C258
9. KMM4(5)8256/KMM4(5)8257
10. KMM4(5)9256/KMM4(5)9257
11. KMM4(5)81000/KMM4(5)81001
12. KMM4(5)91000/KMM4(5)91001

Dynamic RAM

Capacity	Part Number	Organization	Speed (ns)	Technology	Features	Packages	Remark
64K bit	KM4164B-12	64K × 1	120	NMOS	Page Mode	16-Pin DIP	Now
	KM4164B-15	64K × 1	150	NMOS	Page Mode	16-Pin DIP	Now
256K bit	KM41256AP-12	256K × 1	120	NMOS	Page Mode	16-Pin DIP	Now
	KM41256AP-15	256K × 1	150	NMOS	Page Mode	16-Pin DIP	Now
	KM41256AJ-12	256K × 1	120	NMOS	Page Mode	18-Pin PLCC	Now
	KM41256AJ-15	256K × 1	150	NMOS	Page Mode	18-Pin PLCC	Now
	KM41256AZ-12	256K × 1	120	NMOS	Page Mode	16-Pin ZIP	Now
	KM41256AZ-15	256K × 1	150	NMOS	Page Mode	16-Pin ZIP	Now
	KM41257AP-12	256K × 1	120	NMOS	Nibble Mode	16-Pin DIP	Now
	KM41257AP-15	256K × 1	150	NMOS	Nibble Mode	16-Pin DIP	Now
	KM41257AJ-12	256K × 1	120	NMOS	Nibble Mode	18-Pin PLCC	Now
	KM41257AJ-15	256K × 1	150	NMOS	Nibble Mode	18-Pin PLCC	Now
	KM41257AZ-12	256K × 1	120	NMOS	Nibble Mode	16-Pin ZIP	Now
	KM41257AZ-15	256K × 1	150	NMOS	Nibble Mode	16-Pin ZIP	Now
	KM41464AP-12	64K × 4	120	NMOS	Page Mode	18-Pin DIP	Now
	KM41464AP-15	64K × 4	150	NMOS	Page Mode	18-Pin DIP	Now
	KM41464AJ-12	64K × 4	120	NMOS	Page Mode	18-Pin PLCC	Now
	KM41464AJ-15	64K × 4	150	NMOS	Page Mode	18-Pin PLCC	Now
	KM41464AZ-12	64K × 4	120	NMOS	Page Mode	20-Pin ZIP	Now
	KM41464AZ-15	64K × 4	150	NMOS	Page Mode	20-Pin ZIP	Now
1M bit	KM41C1000P-10	1M × 1	100	CMOS	Fast Page Mode	18-Pin DIP	Now
	KM41C1000P-12	1M × 1	120	CMOS	Fast Page Mode	18-Pin DIP	Now
	KM41C1000J-10	1M × 1	100	CMOS	Fast Page Mode	20-Pin SOJ	Now
	KM41C1000J-12	1M × 1	120	CMOS	Fast Page Mode	20-Pin SOJ	Now
	KM41C1000Z-10	1M × 1	100	CMOS	Fast Page Mode	20-Pin ZIP	Now
	KM41C1000Z-12	1M × 1	120	CMOS	Fast Page Mode	20-Pin ZIP	Now
	KM41C1002P-10	1M × 1	100	CMOS	S. Column Mode	18-Pin DIP	Now
	KM41C1002P-12	1M × 1	120	CMOS	S. Column Mode	18-Pin DIP	Now
	†KM44C256J-10	256K × 4	100	CMOS	Fast Page Mode	20-Pin SOJ	Now
	†KM44C256J-12	256K × 4	120	CMOS	Fast Page Mode	20-Pin SOJ	Now

* KM41C1001 (Nibble Mode) and KM44C258 (Static Column Mode) are available in Q4,'88.

64K x 1 Bit Dynamic RAM with Page Mode

FEATURES

- **Performance range**

	t_{RAC}	t_{CAC}	t_{RC}
KM4164B-10	100ns	55ns	190ns
KM4164B-12	120ns	60ns	220ns
KM4164B-15	150ns	75ns	260ns

- **Page Mode capability**
- **Single +5V ±10% power supply**
- **Common I/O using early write**
- **TTL compatible inputs and output**
- **Schmitt Triggers on all input control lines**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **128 cycle/2ms refresh**
- **Jedec standard pinout in 16-pin DIP**

GENERAL DESCRIPTION

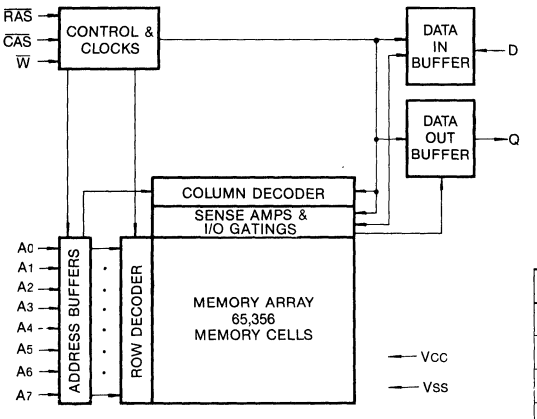
The KM4164B is a fully decoded NMOS Dynamic Random Access Memory organized as 65,536 one-bit words. The design is optimized for high speed, high performance applications such as computer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The KM4164B features page mode which allows high speed random access of up to 256-bits within the same row. Multiplexed row and column address inputs permit the KM4164B to be housed in a standard 16-pin DIP.

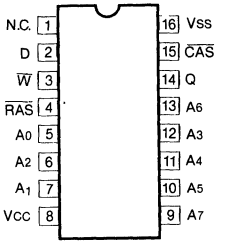
The KM4164B is fabricated using Samsung's advanced silicon gate NMOS process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_7	Address inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−2.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7.5	V
Storage Temperature	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OS}	50	mA

*Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	$V_{CC}+1$	V
Input Low Voltage	V_{IL}	−2.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ cycling; @t_{RC} = min.)	KM4164B-10	I_{CC1}	—	60	mA
	KM4164B-12		—	50	mA
	KM4164B-15		—	45	mA
Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles min.)		I_{CC2}	—	4	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; @t_{RC} = min.)	KM4164B-10	I_{CC3}	—	50	mA
	KM4164B-12		—	40	mA
	KM4164B-15		—	35	mA
Page Mode Current* ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; @t_{PC} = min.)	KM4164B-10	I_{CC4}	—	45	mA
	KM4164B-12		—	35	mA
	KM4164B-15		—	30	
Input Leakage Current (Any input $0 \le V_{IN} \le 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \le V_{OUT} \le 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$)		I_{OL}	−10	10	μA
Output High Voltage Level ($I_{OH} = -5mA$)		V_{OH}	2.4	—	V
Output Low Voltage Level ($I_{OL} = 4.2mA$)		V_{OL}	—	0.4	V

*Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0-A_7, D)	C_{IN1}	—	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	6	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	KM4164B-10		KM4164B-12		KM4164B-15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	190		220		260		ns	
Read-modify-write cycle time	t_{RWC}	215		255		300		ns	
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	3, 4
Access time from $\overline{CAS}$	t_{CAC}		55		60		75	ns	3, 5
Output buffer turn-off delay time	t_{OFF}	0	25	0	30	0	35	ns	6
Transition time (rise and fall)	t_T	3	100	3	100	3	100	ns	
$\overline{RAS}$ precharge time	t_{RP}	80		90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	55		60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	55	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	15	45	20	60	25	75	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	0		0		0		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	15		18		20		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	25		30		35		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	70		90		110		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	
Write command set-up time	t_{WCS}	0		0		0		ns	7
Write command hold time	t_{WCH}	30		35		45		ns	
Write command pulse width	t_{WP}	30		35		45		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		35		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25		35		45		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	
Data-in hold time	t_{DH}	30		35		40		ns	
$\overline{CAS}$ to write enable delay time	t_{CWD}	50		55		65		ns	7

AC CHARACTERISTICS (Continued)

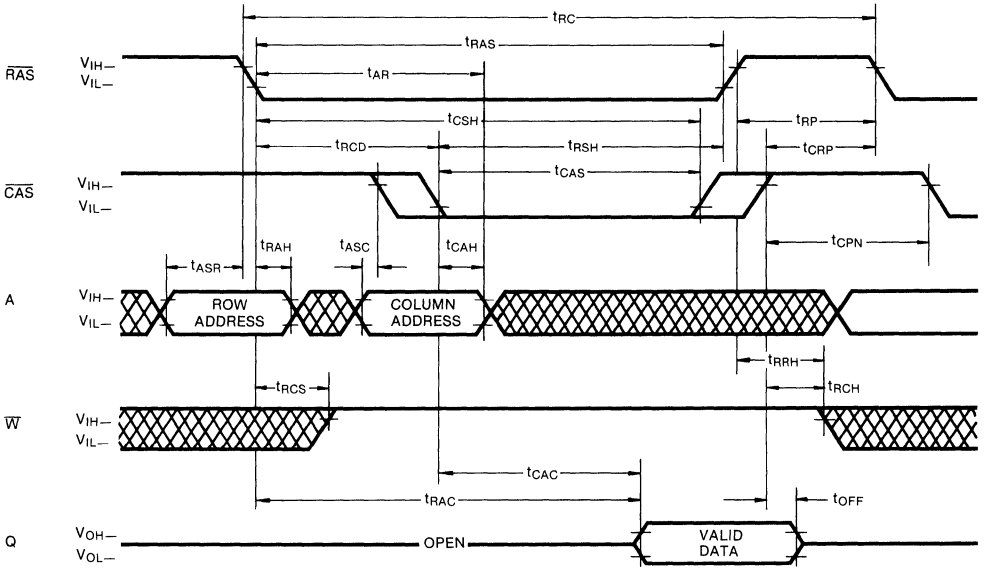
Parameter	Symbol	KM4164B-10		KM4164B-12		KM4164B-15		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to write enable delay time	t_{RWD}	95		115		140		ns	7
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	75		95		120		ns	
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	75		95		115		ns	
Page mode cycle time	t_{PC}	105		120		145		ns	
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	40		45		60		ns	
$\overline{CAS}$ precharge time (all cycles except page mode)	t_{CPN}	25		25		30		ns	
Refresh period	t_{REF}		2		2		2	ms	

NOTES

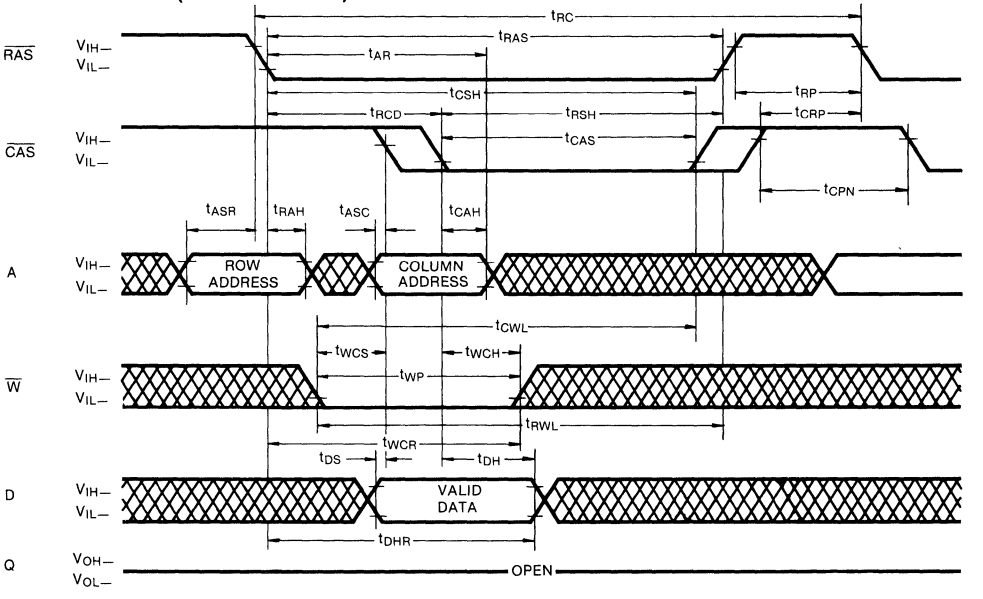
1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(mas) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the T_{RCD}(max) limit insures that T_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by T_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{CWD} and t_{RWD} are restrictive operating parameters for the read-modify-write cycle only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} > t_{RWD}$(min), the cycle is a late write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

TIMING DIAGRAMS

READ CYCLE

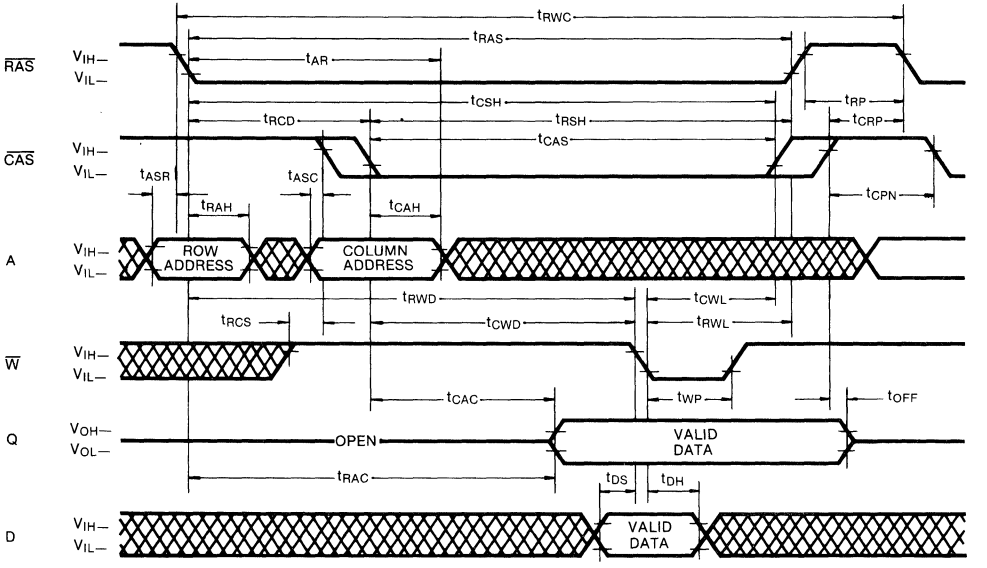


WRITE CYCLE (EARLY WRITE)

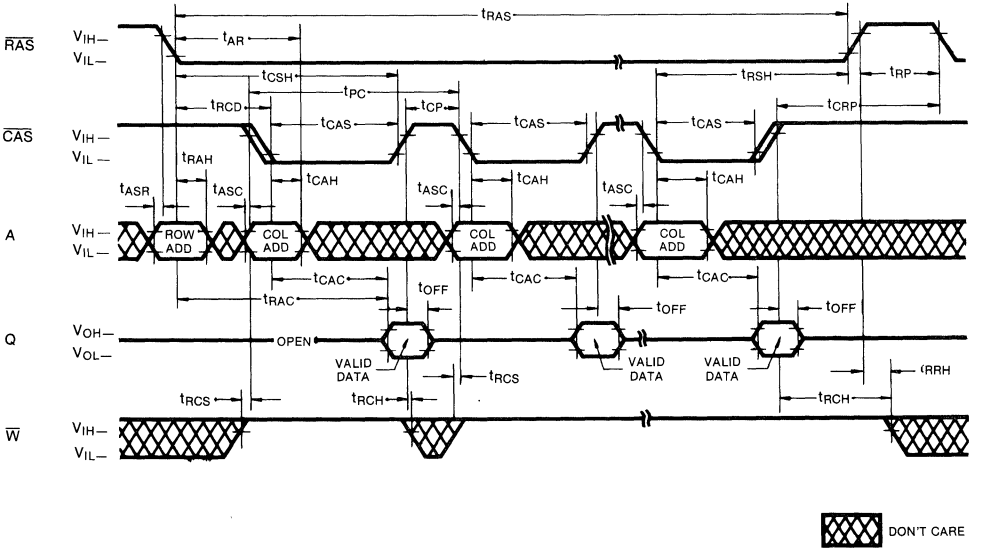


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

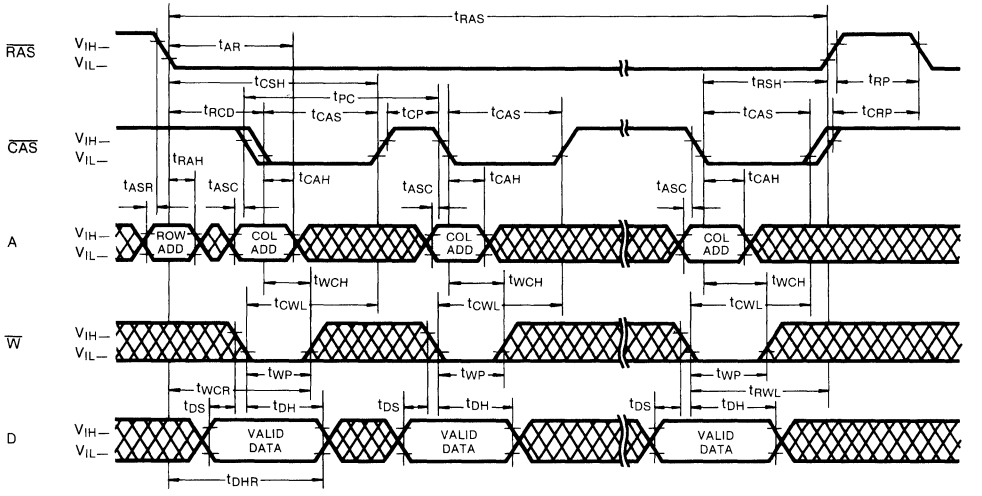


PAGE MODE READ CYCLE



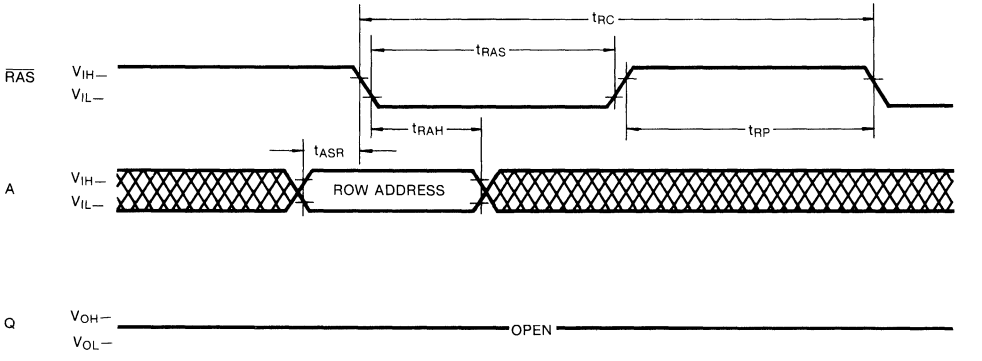
TIMING DIAGRAMS (Continued)

PAGE MODE WRITE CYCLE



RAS-ONLY REFRESH CYCLE

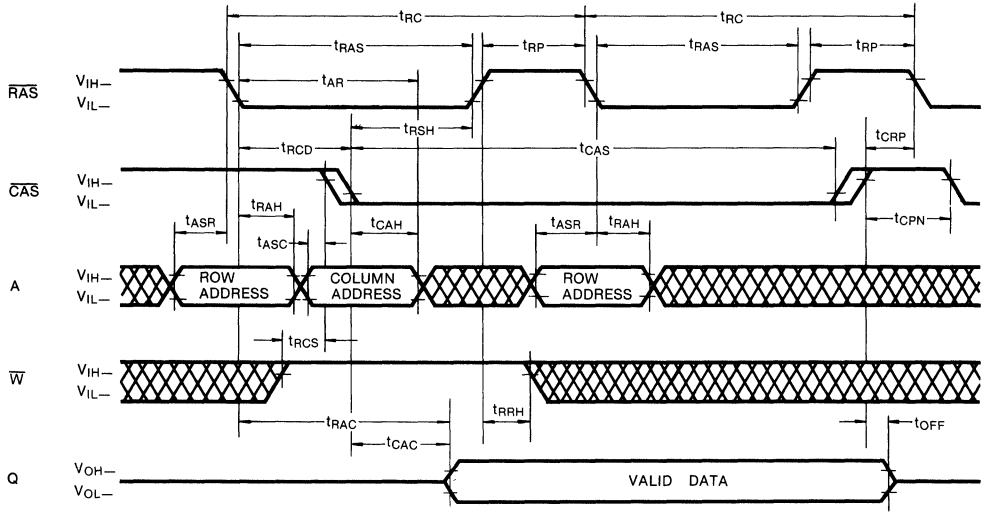
Note: CAS = V_{IH} W,D = Don't care



DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE



KM4164B OPERATION

Device Operation

The KM4164B contains 65,536 memory locations. Sixteen address bits are required to address a particular memory location. Since the KM4164B has only 8 address input pins, time multiplexed addressing is used to input 8 row and 8 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the KM4164B begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 8 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM4164B cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse width are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM4164B begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The output of the KM4164B remains in the Hi-Z state until valid data appears at the output. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured

DEVICE OPERATION (Continued)

from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM4164B can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} and t_{CWD}, are not necessarily met. The state of data-out is indeterminate since the output could be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM4164B has a tri-state output buffer which is controlled by $\overline{CAS}$ (and $\overline{W}$ for early write).
Whenever $\overline{CAS}$ is high (V_{IH}), the output is in the high impedance (Hi-Z) state, In any cycle in which valid data appears at the output, the output first remains in the Hi-Z state until the data is valid and then the valid data appears at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM4164B operating cycles are listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Page Mode Read, Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Page Mode write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM4164B is stored on a tiny capacitor within each memory cell. Due to leakage, the data will leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 2 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and strobing in a refresh row address with $\overline{RAS}$.

Other Refresh Methods: It is also possible to refresh the KM4164B by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only refresh is the preferred method.

Page Mode

Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up the KM4164B might begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 100μsec is required after power-up followed by 8 initialized cycles before proper device

DEVICE OPERATION (Continued)

operation is assured. Eight initialization cycles are also required after any 2 ms period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM4164B inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM4164B input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Decoupling

The importance of proper decoupling cannot be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). The total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

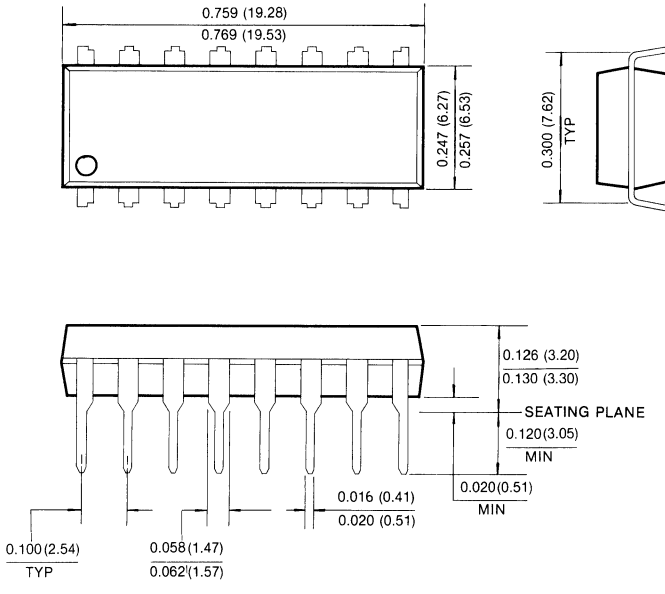
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM4164B using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM4164B and they supply much of the current used by the KM4164B during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor throughout the memory array.

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (millimeters)



256K x 1 Bit Dynamic RAM with Page/Nibble Mode

FEATURES

- **Performance range**

	t_{RAC}	t_{CAC}	t_{RC}
KM41256/7A-10	100ns	50ns	200ns
KM41256/7A-12	120ns	60ns	230ns
KM41256/7A-15	150ns	75ns	260ns

- **Page Mode capability-KM41256A**
- **Nibble Mode capability-KM41257A**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and output**
- **Common I/O using early write**
- **Single +5V±10% power supply**
- **256 cycle/4ms refresh**
- **Jedec standard pinout in 16-pin plastic DIP, 18 lead PLCC and 16-pin plastic ZIP.**

DESCRIPTION

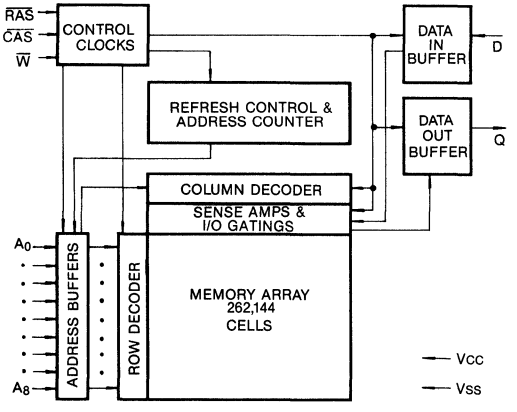
The KM41256/7A is a fully decoded NMOS Dynamic Random Access Memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as computer memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The KM41256A features page mode which allows high speed random access of memory cells within the same row. The KM41257A features nibble mode which allows high speed serial access of up to 4 bits of data. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. Multiplexed row and column address inputs permit the KM41256/7A to be housed in a JEDEC standard 16-pin DIP.

The KM41256/7A is fabricated using Samsung's advanced silicon gate NMOS process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size.

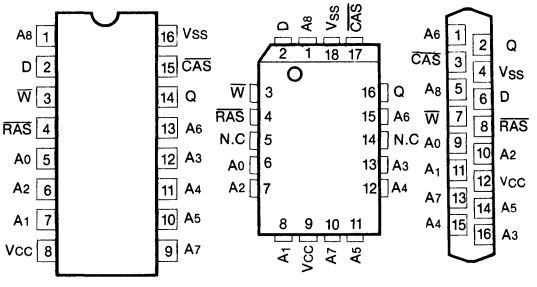
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

- **KM41256/7AP** **•KM41256/7AJ** **•KM41256/7AZ**



Pin Name	Pin Function
A_0-A_8	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OS}	50	mA

*Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ cycling; @t_{RC} = min.)	KM41256/7A-10	I_{CC1}	—	85	mA
	KM41256/7A-12		—	75	mA
	KM41256/7A-15		—	65	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	4.5	mA
RAS-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; @t_{RC} = min.)	KM41256/7A-10	I_{CC3}	—	70	mA
	KM41256/7A-12		—	65	mA
	KM41256/7A-15		—	60	mA
Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; @t_{PC} = min.)	KM41256A-10	I_{CC4}	—	65	mA
	KM41256A-12		—	55	mA
	KM41256A-15		—	45	mA
Nibble Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; @t_{NC} = min.)	KM41257A-10	I_{CC5}	—	65	mA
	KM41257A-12		—	55	mA
	KM41257A-15		—	45	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ cycling @t_{RC} = min.)	KM41256/7A-10	I_{CC6}	—	70	mA
	KM41256/7A-12		—	65	mA
	KM41256/7A-15		—	60	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 5.5V$, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$)	I_{OL}	−10	10	μA
Output High Voltage Level ($I_{OH} = -5mA$)	V_{OH}	2.4	—	V
Output Low Voltage Level ($I_{OL} = 4.2mA$)	V_{OL}	—	0.4	V

*Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8, D)	C_{IN1}	—	7	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	10	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1,2)

KM41256/7A STANDARD OPERATION

Parameter	Symbol	KM41256A-10 KM41257A-10		KM41256A-12 KM41257A-12		KM41256A-15 KM41257A-15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	200		230		260		ns	
Read-modify-write cycle time	t_{RWC}	245		265		310		ns	
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	3.4
Access time from $\overline{CAS}$	t_{CAC}		50		60		75	ns	3.5
Output buffer turn-off delay time	t_{OFF}	0	25	0	30	0	40	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	90		100		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50		60		75		ns	
$\overline{CAS}$ precharge time (all cycles except page mode)	t_{CPN}	45		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	110		120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	15		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	

KM41256/7A STANDARD OPERATION (Continued)

Parameter	Symbol	KM41256A-10 KM41257A-10		KM41256A-12 KM41257A-12		KM41256A-15 KM41257A-15		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time referenced to $\overline{RAS}$	t_{AR}	65		80		100		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		20		ns	
Write command set-up time	t_{WCS}	0		0		0		ns	7
Write command hold time	t_{WCH}	35		40		45		ns	
Write command pulse width	t_{WP}	35		40		45		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		40		45		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	
Data-in hold time	t_{DH}	35		40		45		ns	
$\overline{CAS}$ to write enable delay time	t_{CWD}	50		60		75		ns	7
$\overline{RAS}$ to write enable delay time	t_{RWD}	100		120		150		ns	7
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		100		120		ns	
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	85		100		120		ns	
Refresh period (256 cycles)	t_{REF}		4		4		4	ms	

KM41256/7A $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	20		25		30		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	50		55		60		ns	
Refresh counter test cycle time	t_{RTC}	330		375		430		ns	
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	50		60		70		ns	
Refresh counter test $\overline{RAS}$ pulse width	t_{TRAS}	230		265		320		ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ hold time	t_{RPC}	20		20		20		ns	

KM41257A NIBBLE MODE

Nibble mode read/write cycle time	t_{NC}	50		60		75		ns	
Nibble mode read-write cycle time	t_{NRWC}	75		90		105		ns	
Nibble mode access time	t_{NCAC}		20		30		40	ns	
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	20		30		40		ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	20		25		30		ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	30		40		50		ns	
Nibble mode $\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{RNH}	20		20		20		ns	
Nibble mode $\overline{CAS}$ to $\overline{W}$ delay time	t_{NCWD}	30		30		35		ns	
Nibble mode $\overline{W}$ to $\overline{CAS}$ lead time	t_{NCWL}	25		25		30		ns	

KM41256A PAGE MODE (Continued)

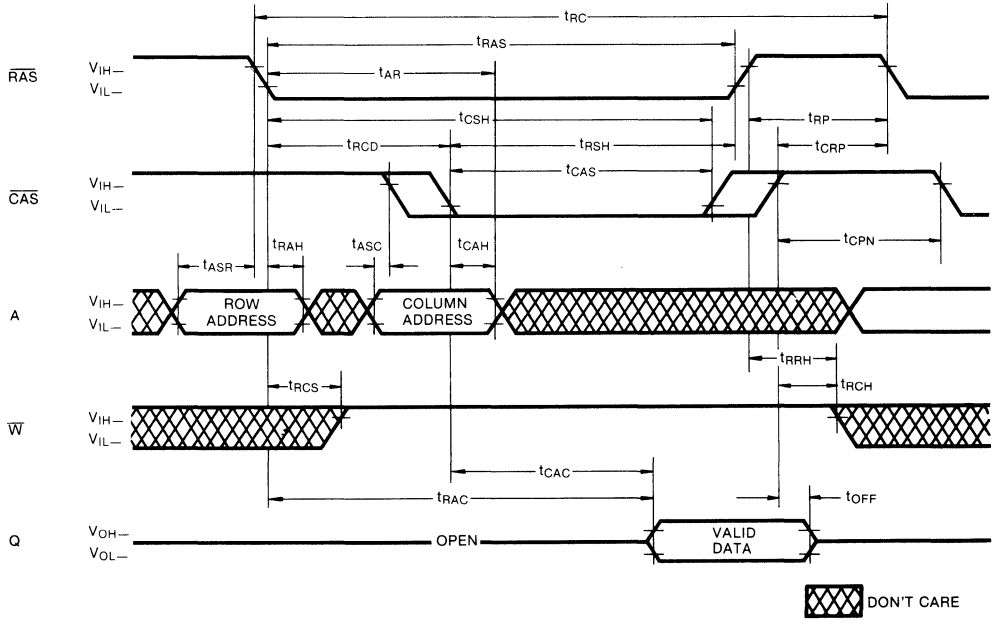
Parameter	Symbol	KM41256A-10		KM41256A-12		KM41256A-15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Page mode cycle time	t_{PC}	100		120		145		ns	
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	45		50		60		ns	

NOTES

1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{CWD} and t_{RWD} are restrictive operating parameters for the read-modify-write cycle only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} > t_{RWD}$(min), the cycle is a late write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

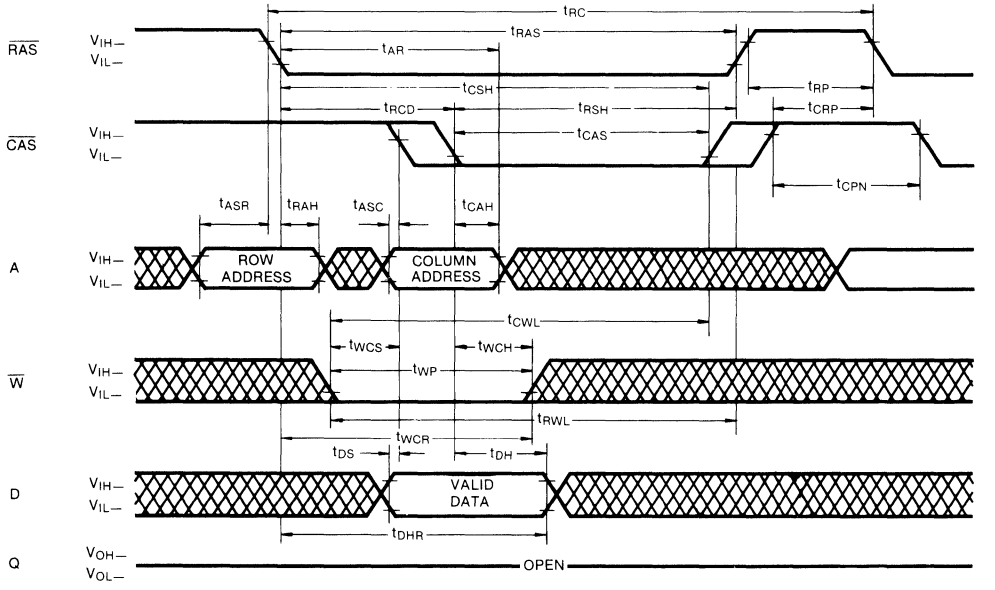
TIMING DIAGRAMS

READ CYCLE

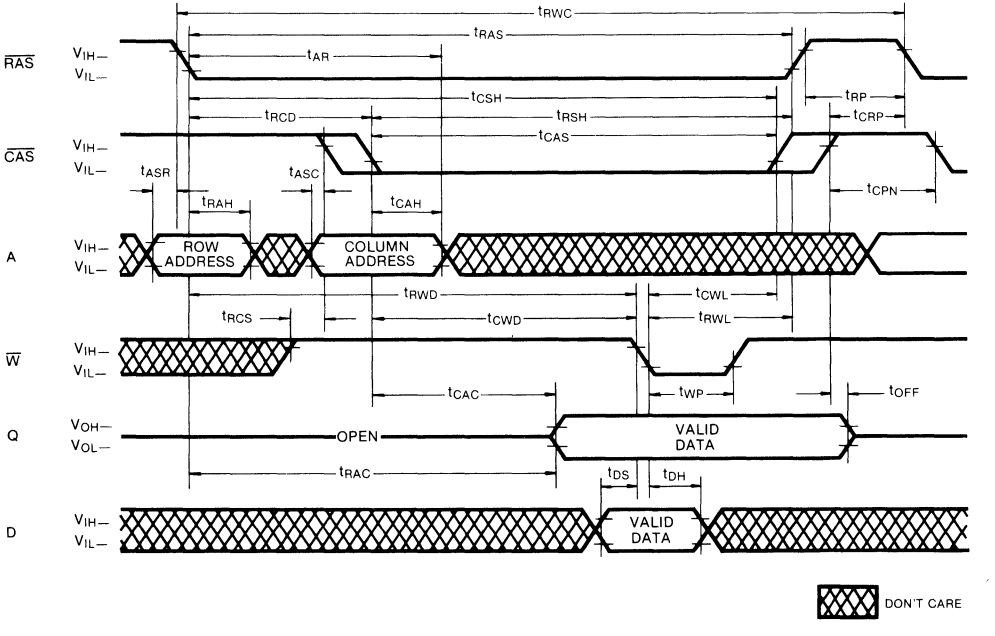


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

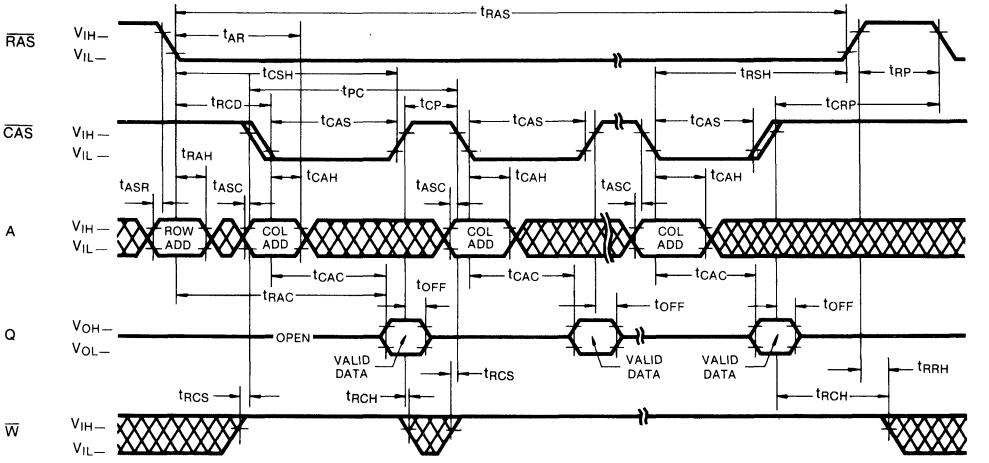


READ-WRITE/READ-MODIFY-WRITE CYCLE

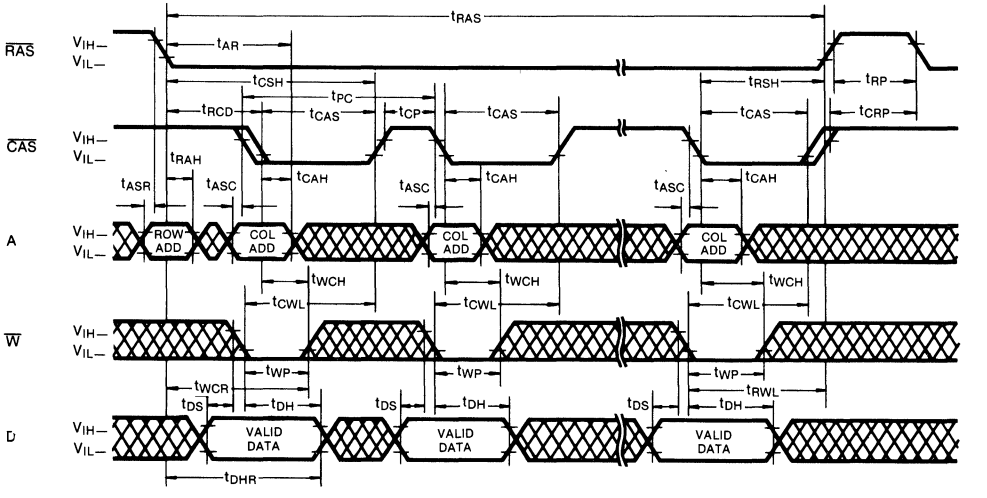


TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE (KM41256A)



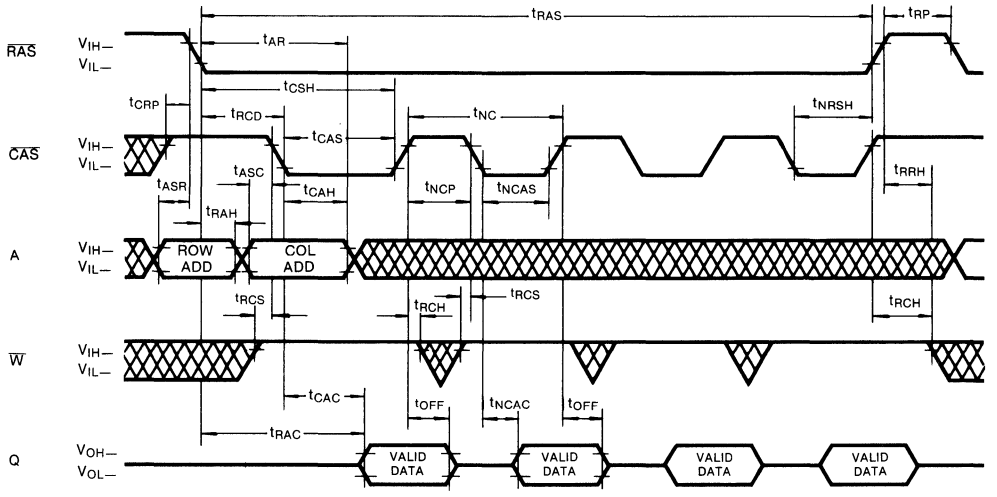
PAGE MODE WRITE CYCLE (KM41256A)



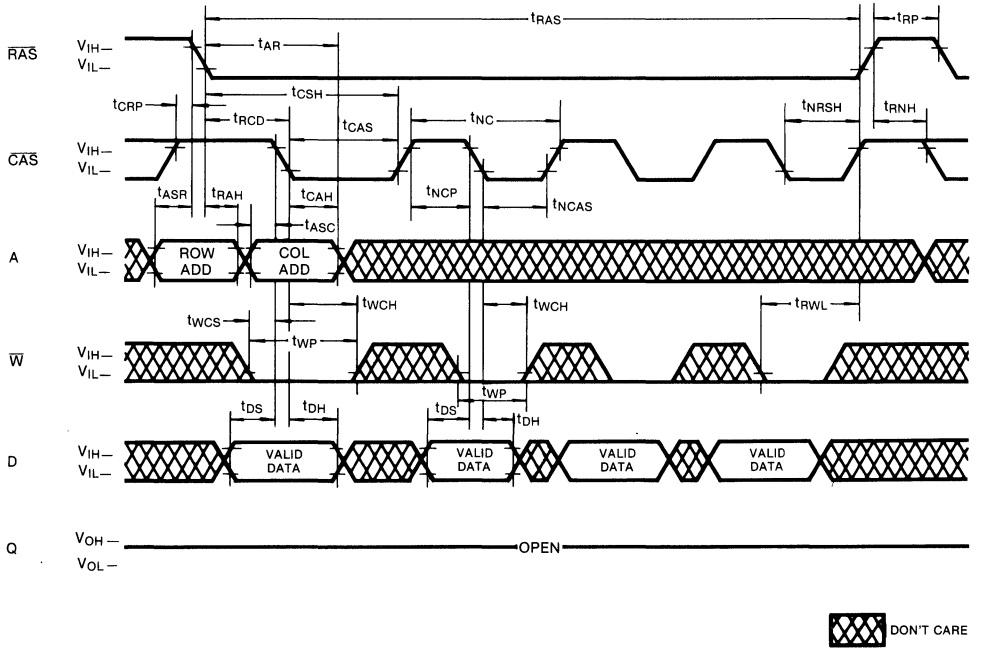
DON'T CARE

TIMING DIAGRAMS (Continued)

NIBBLE MODE READ CYCLE (KM41257A)

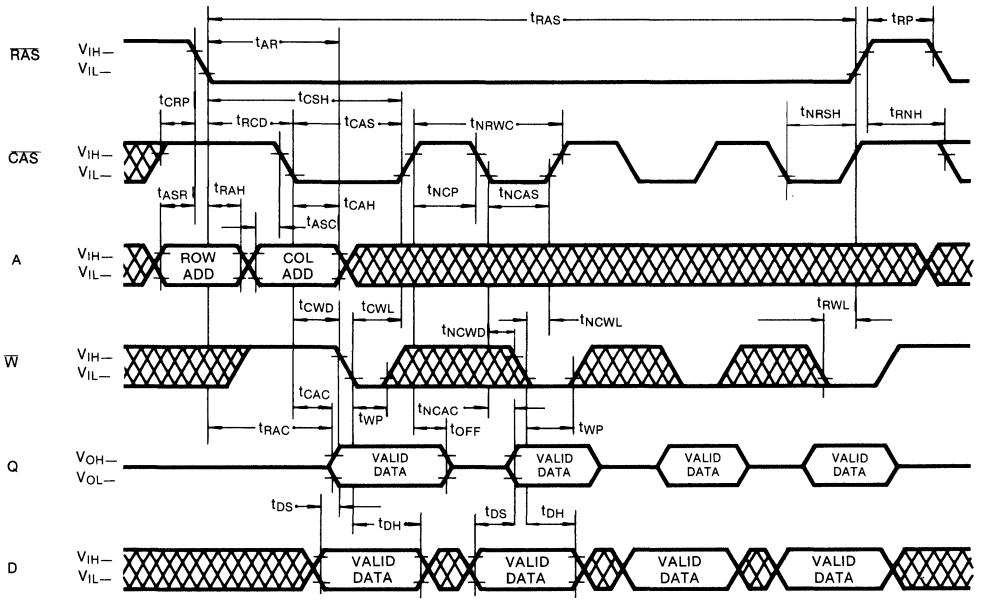


NIBBLE MODE WRITE CYCLE (KM41257A)



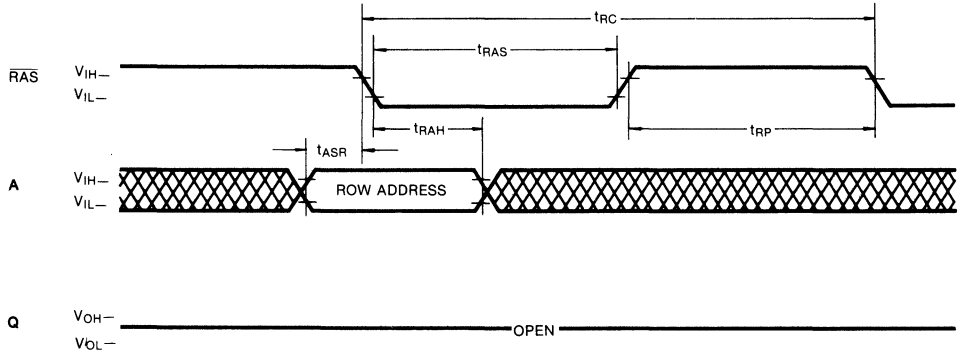
TIMING DIAGRAMS (Continued)

NIBBLE MODE READ-WRITE CYCLE (KM41257A)



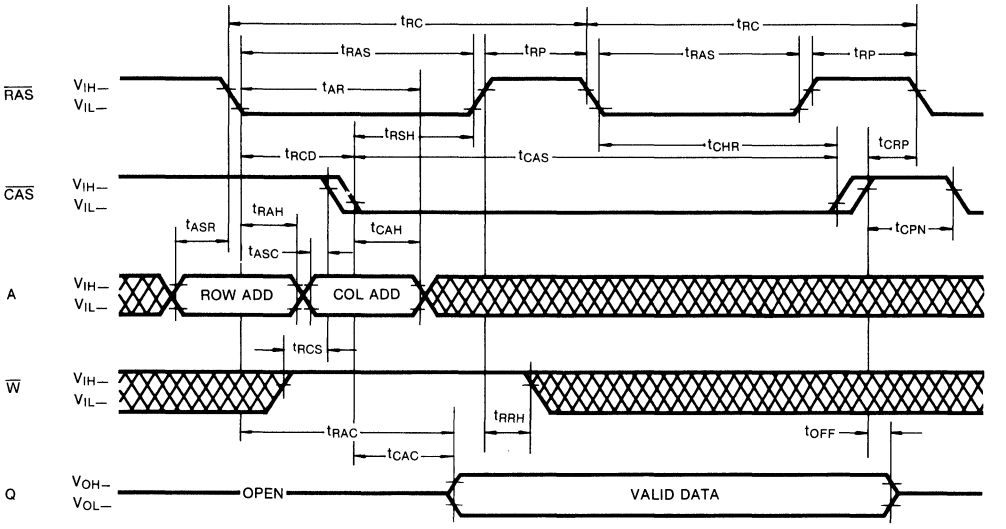
RAS-ONLY REFRESH CYCLE

NOTE: $\overline{CAS}$ = V_{IH}, $\overline{W}$, D = Don't Care



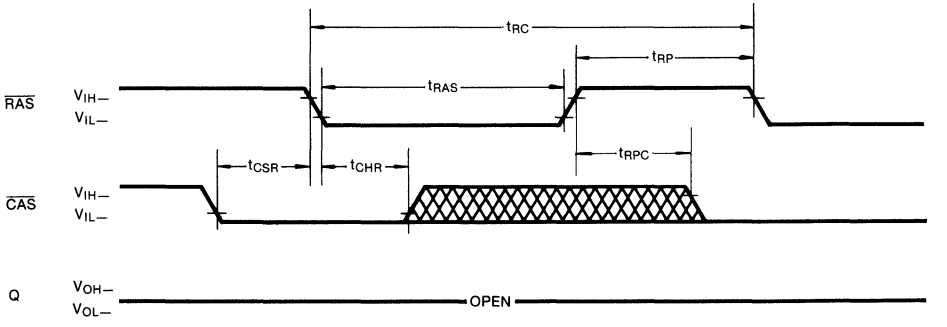
TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH CYCLE

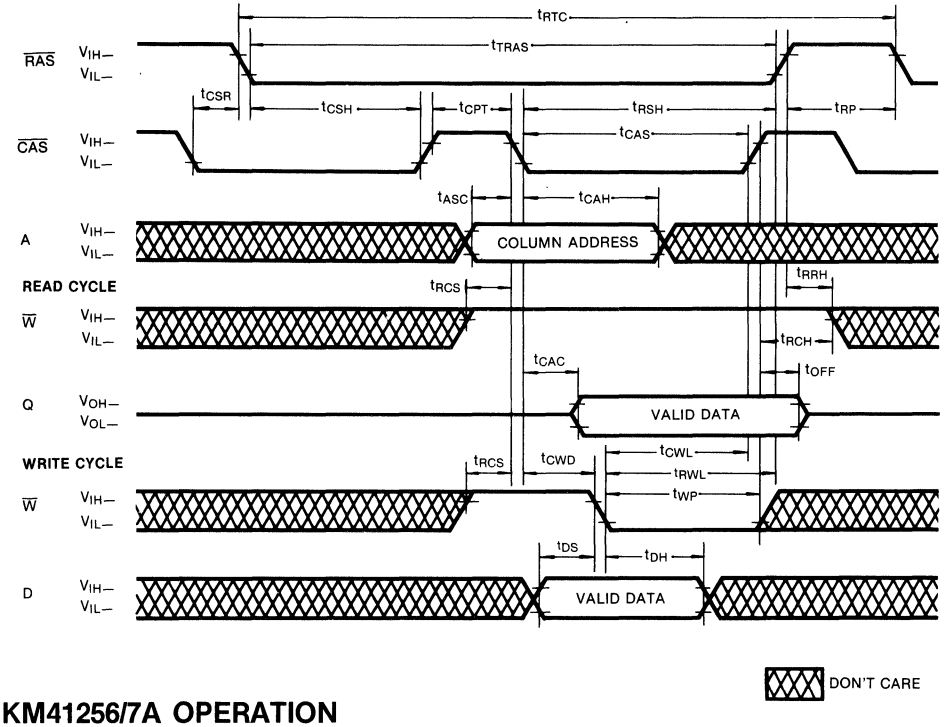
NOTE: Address, W, D = Don't Care



DON'T CARE

TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



KM41256/7A OPERATION

Device Operation

The KM41256/7A contains 262,144 memory locations. Eighteen address bits are required to address a particular memory location. Since the KM41256/7A has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the KM41256/7A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41256/7A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse width are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41256/7A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

DEVICE OPERATION (Continued)

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The output of the KM41256/7A remains in the Hi-Z state until valid data appears at the output. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41256/7A can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} and t_{CWD}, are not necessarily met. The state of data-out is indeterminate since the output could be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41256/7A has a tri-state output buffer which is controlled by $\overline{CAS}$ (and $\overline{W}$ for early write).
Whenever $\overline{CAS}$ is high (V_{IH}), the output is in the high impedance (Hi-Z) state, In any cycle in which valid data appears at the output, the output first remains in the Hi-Z state until the data is valid and then the valid data appears at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41256/7A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Page Mode Read, Page Mode Read-Modify-Write. Nibble Mode Read, Nibble Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Page Mode Write, Nibble Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41256/7A is stored on a tiny capacitor within each memory cell. Due to leakage, the data will leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 4 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41256/7A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addressed. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs and the on-chip refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and strobing in a refresh row address with $\overline{RAS}$. The KM41256/7A hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required in hidden refresh cycles by DRAMS that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Other Refresh Methods: It is also possible to refresh the KM41256/7A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only refresh is the preferred method.

DEVICE OPERATION (Continued)

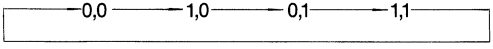
Page Mode (KM41256A)

The KM41257A has page mode capability. Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Nibble Mode (KM41257A)

The KM41257A has nibble mode capability. Nibble mode operation allows high speed serial read, write or read-modify-write access of 4 consecutive bits. The first of 4 bits is accessed in the usual manner. The remaining nibble bits are accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low.

The 4 bits of data that may be accessed during nibble mode are determined by the lower 8 row address bits (RA_0-RA_7) and 8 column address bits (CA_0-CA_7). The two address bits, $RA_8$and CA_8, are used to select 1 of the 4 nibble bits for initial access. The remaining nibble bits are accessed by toggling $\overline{CAS}$ with $\overline{RAS}$ held low. Each high-low $\overline{CAS}$ transition will internally increment the nibble address (RA_8, CA_8) as shown in the following diagram.



If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on a subsequent access, the new data will be written into the selected cell location.

A nibble cycle can be a read, write, or read-modify-write cycle. Any combinations of reads and writes or read-modify-writes are allowed.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter test cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

Row Address—Bits A0 through A7 are supplied by the on-chip refresh counter. The A8 bit is set high internally.

Column Address—Bits A0 through A8 are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedures

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 256 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 256 times so that highs are written into the 256 memory cells.
4. Read the "highs" written during step 3.
5. Compliment the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS}$=V_{SS} during power-up the KM41256/7A might begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 100μsec is required after power-up followed by 8 initialized cycles before proper device operation is assured. Eight initialization cycles are also required after any 4 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41256/7A inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be us-

DEVICE OPERATION (Continued)

ed, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41256/7A input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Decoupling

The importance of proper decoupling cannot be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). The total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

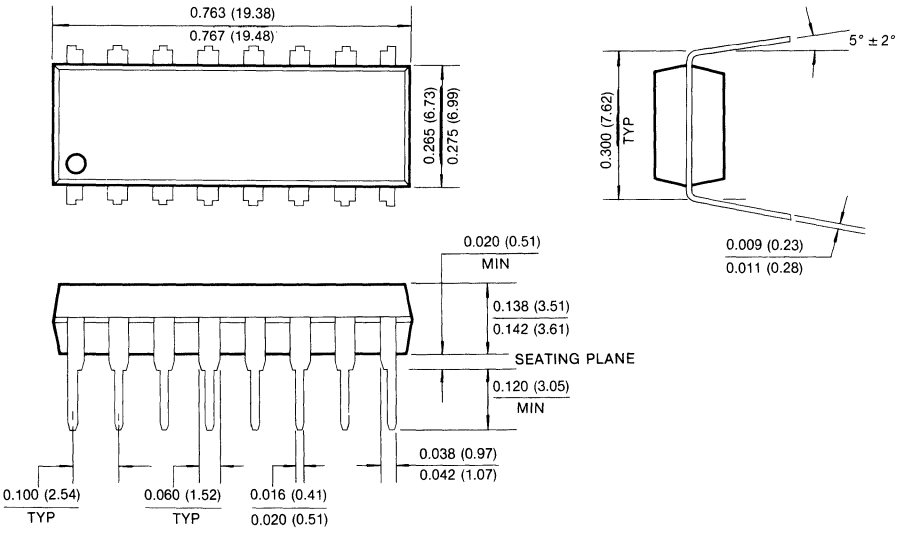
A high frequency 0.3μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41256/7A using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41256/7A and they supply much of the current used by the KM41256/7A during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.3μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor throughout the memory array.

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE

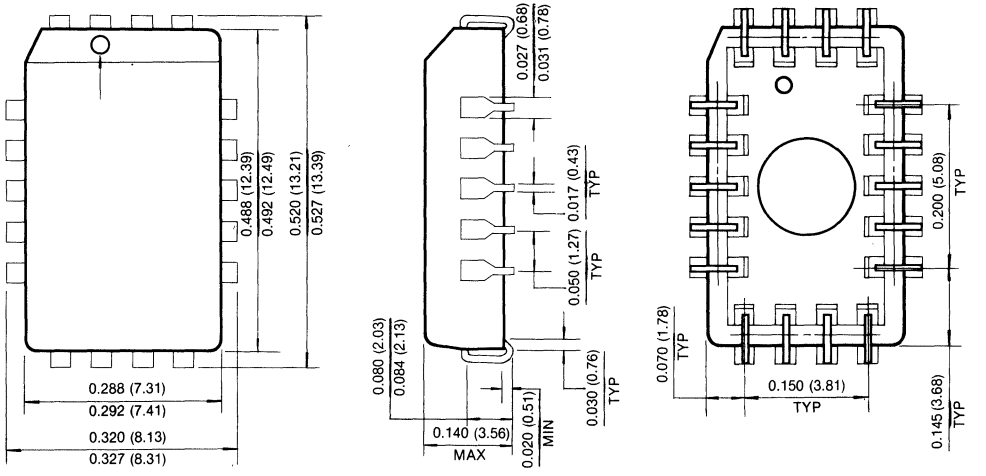
Units: Inches (millimeters)



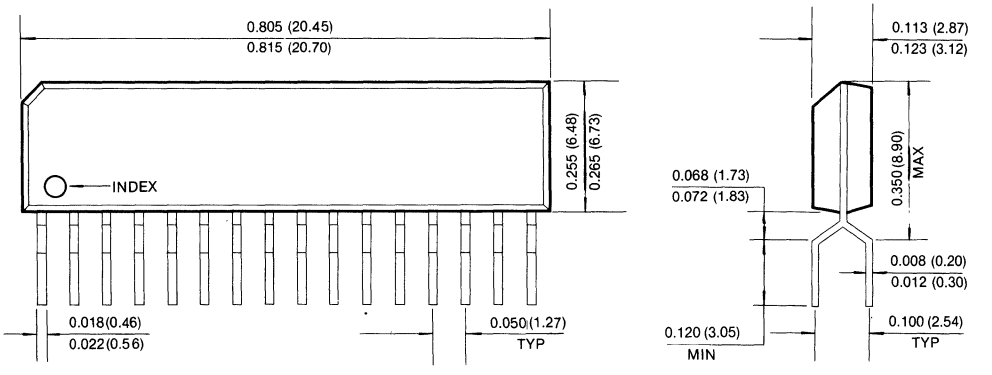
PACKAGE DIMENSIONS (Continued)

18- LEAD PLASTIC CHIP CARRIER

Units: Inches (millimeters)



16-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE



64K x 4 Bit Dynamic RAM with Page Mode

FEATURES

- **Performance range**

	t_{RAC}	t_{CAC}	t_{RC}
KM41464A-12	120ns	60ns	220ns
KM41464A-15	150ns	75ns	260ns

- **Page Mode capability**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or Output Enable Controlled Write**
- **Single +5V±10% power supply**
- **256 cycle/4ms refresh**
- **JEDEC standard pinout in 18-pin DIP, 18-lead PLCC and 20-pin ZIP.**

GENERAL DESCRIPTION

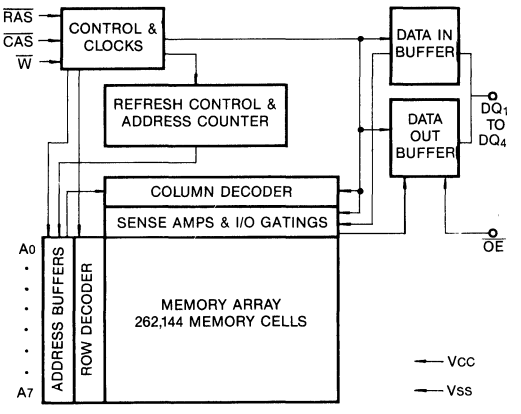
The KM41464A is a fully decoded 65,536 x 4 NMOS Dynamic Random Access Memory. The design is optimized for high speed, high performance applications such as computer memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The KM41464A features page mode which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. Multiplexed row and column address inputs permit the KM41464A to be housed in standard packages.

The KM41464A is fabricated using Samsung's advanced silicon gate NMOS process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size.

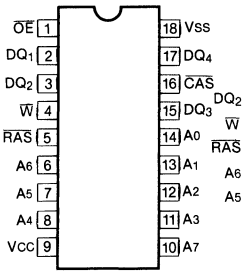
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and outputs are TTL complible.

FUNCTIONAL BLOCK DIAGRAM

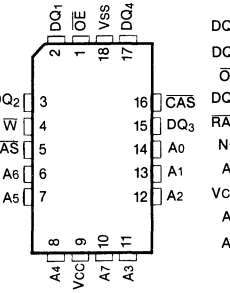


PIN CONFIGURATION

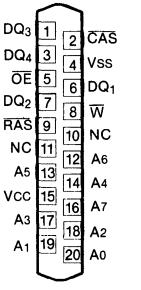
- **KM41464AP**



- **KM41464AJ**



- **KM41464AZ**



Pin Name	Pin Function
A_0-A_7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Output Enable
DQ_1-DQ_4	Data In/Out
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling; @t_{RC} = min.)	KM41464A-12 KM41464A-15	I_{CC1}	— —	75 65	mA mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)		I_{CC2}	—	4.5	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; @t_{RC} = min.)	KM41464A-12 KM41464A-15	I_{CC3}	— —	65 60	mA mA
PAGE MODE CURRENT* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; @t_{PC} = min.)	KM41464A-12 KM41464A-15	I_{CC4}	— —	55 45	mA mA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT ($\overline{RAS}$ cycling; @t_{RC} = min.)	KM41464A-12 KM41464A-15	I_{CC5}	— —	65 60	mA mA
INPUT LEAKAGE CURRENT (Any input 0 ≤ V_{IN} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V		I_{DQL}	−10	10	μA
OUTPUT HIGH VOLTAGE LEVEL (I_{OH} = −5mA)		V_{OH}	2.4	—	V
OUTPUT LOW VOLTAGE LEVEL (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_7)	C_{IN1}	—	7	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	10	pF
Output Capacitance (DQ_1-DQ_4)	C_{DQ}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1,2)

KM41464A STANDARD OPERATION

Parameter	Symbol	KM41464A-12		KM41464A-15		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	220		260		ns	
Read-modify-write cycle time	t_{RWC}	305		355		ns	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	3, 4
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	3, 5
Output buffer turn-off delay time	t_{OFF}	0	30	0	40	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		65		ns	
$\overline{CAS}$ precharge time (all cycles except page mode)	t_{CPN}	30		35		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	40		45		ns	
Write command pulse width	t_{WP}	40		45		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	

KM41464A STANDARD OPERATION (Continued)

Parameter	Symbol	KM41464A-12		KM41464A-15		Units	Notes
		Min	Max	Min	Max		
Data-in set-up time	t_{DS}	0		0		ns	
Data-in hold time	t_{DH}	40		45		ns	
$\overline{CAS}$ to write enable delay time	t_{CWD}	100		120		ns	7
$\overline{RAS}$ to write enable delay time	t_{RWD}	160		195		ns	7
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	100		120		ns	
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	100		120		ns	
Access time from $\overline{OE}$	t_{OEA}		30		40	ns	
$\overline{OE}$ to Data in delay time	t_{OED}	30		40		ns	
Output Buffer turn off delay from $\overline{OE}$	t_{OEZ}	0	30	0	40	ns	
$\overline{OE}$ hold time referenced to $\overline{W}$	t_{OEH}	25		25		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		ns	
Din to $\overline{CAS}$ delay time	t_{DZC}	0		0		ns	8
Din to $\overline{OE}$ delay time	t_{DZO}	0		0		ns	8
Refresh period (256 cycles)	t_{REF}		4		4	ms	

KM41464A $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh)	t_{CSR}	25		30		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh)	t_{CHR}	55		60		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{PRC}	20		20		ns	

KM41464A PAGE MODE

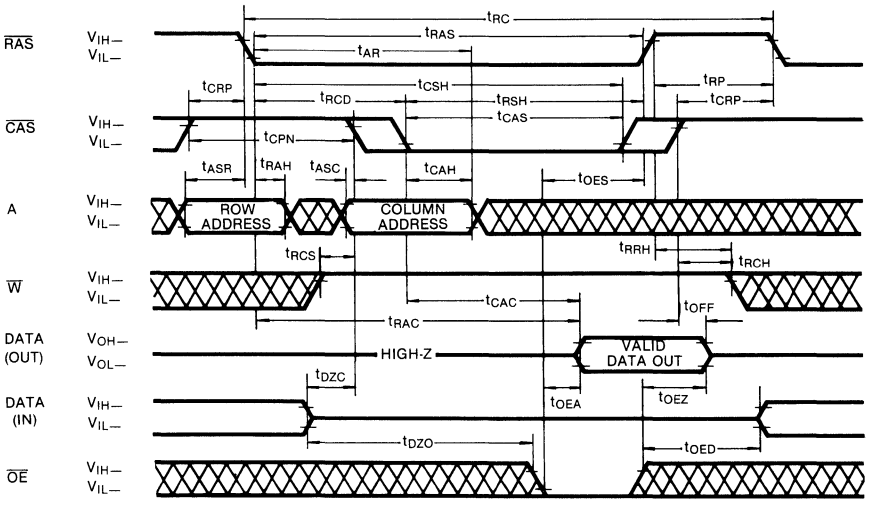
Page mode cycle time	t_{PC}	120		145		ns	
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	50		60		ns	

NOTES

1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{CWD} and t_{RWD} are restrictive operating parameters for the read-modify-write cycle only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} > t_{RWD}$(min), the cycle is a late write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
8. Either t_{DZC} or t_{DZO} must be satisfied for all cycles.

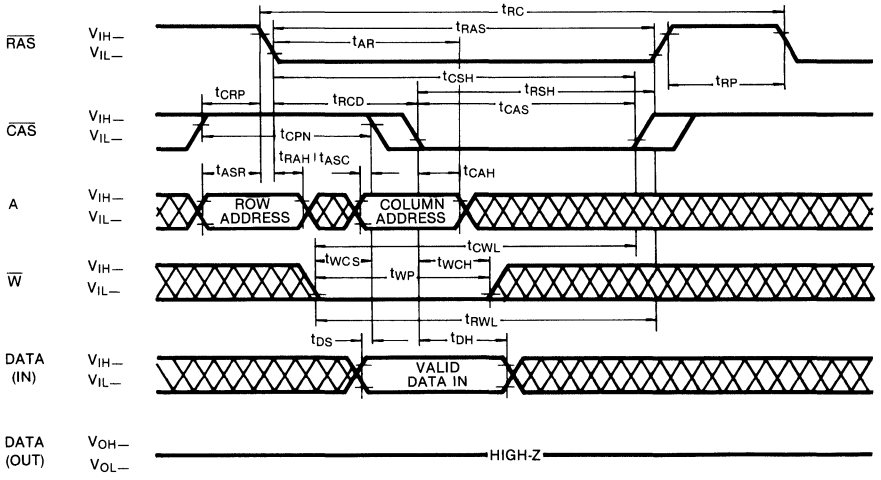
TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE (EARLY WRITE)

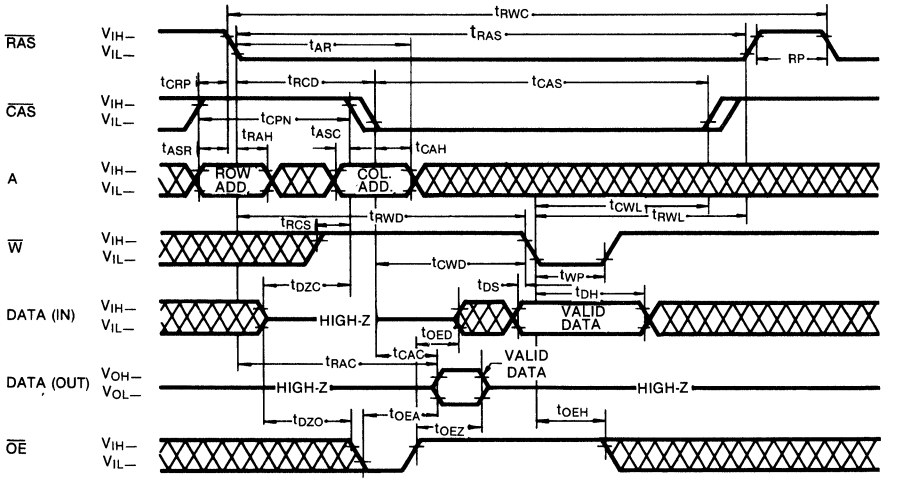
$\overline{OE}$ = Don't Care



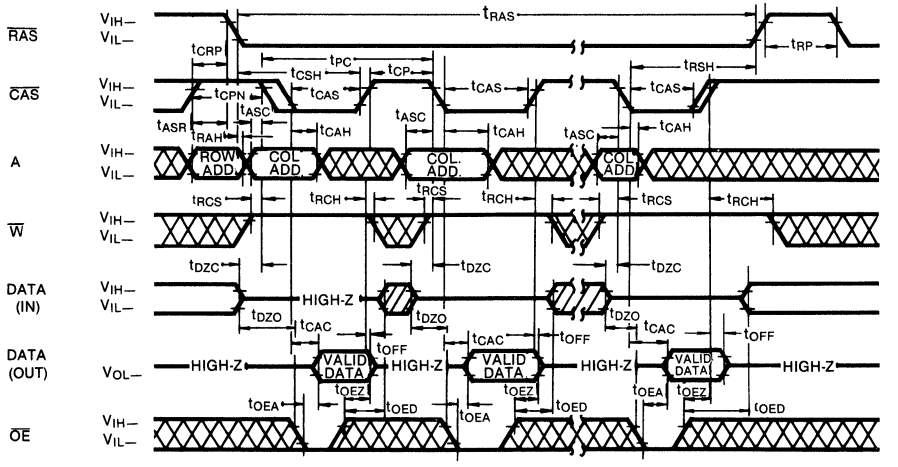
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



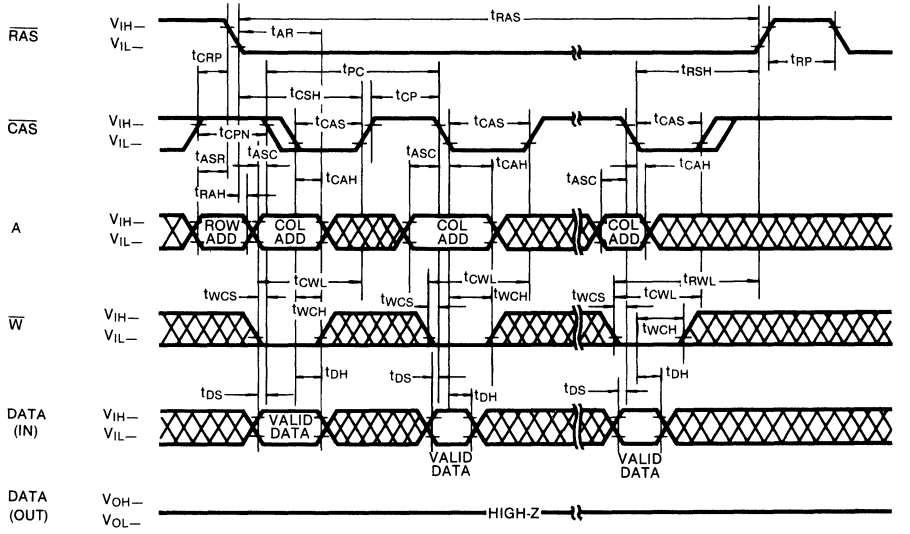
PAGE MODE READ CYCLE



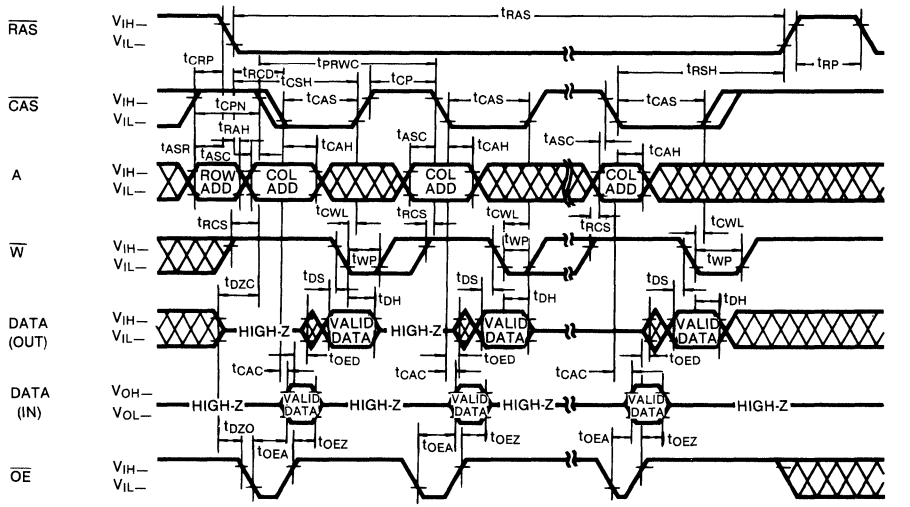
TIMING DIAGRAMS (Continued)

PAGE MODE WRITE CYCLE

$\overline{OE}$ = Don't Care



PAGE MODE READ-MODIFY-WRITE CYCLE

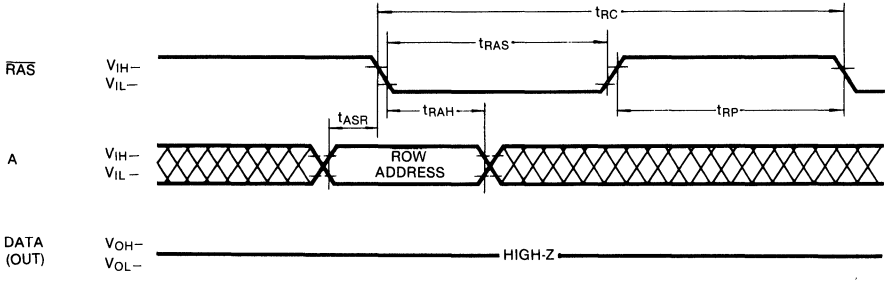


DON'T CARE

TIMING DIAGRAMS (Continued)

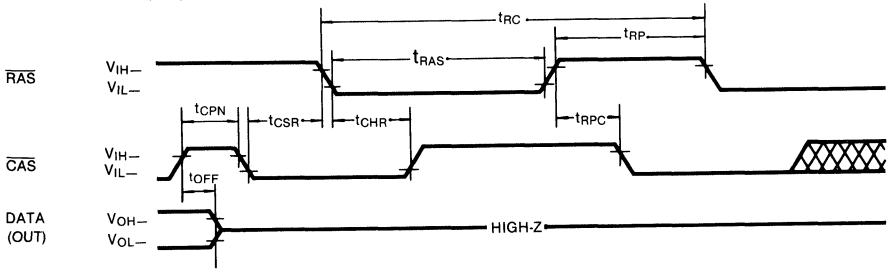
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{CAS}$ = V_{IH}; $\overline{W}$, $\overline{OE}$, D = Don't Care

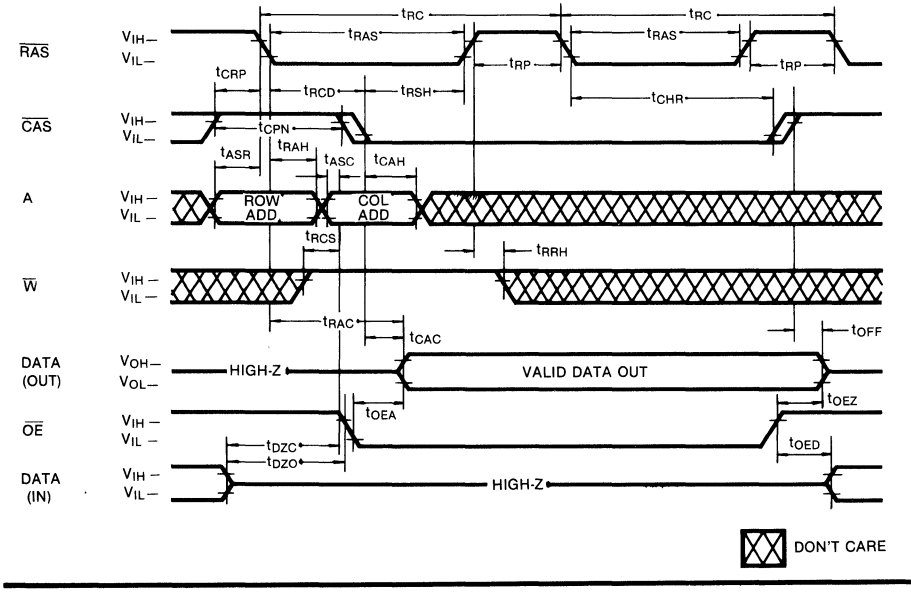


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address, $\overline{W}$, $\overline{OE}$, D = Don't Care



HIDDEN REFRESH CYCLE



KM41464A OPERATION

Device Operation

The KM41464A contains 262,144 memory locations organized as 65,536 x 4-bit words. Sixteen address bits are required to address a particular 4-bit word in the memory array. Since the KM41464A has only 8 address input pins, time multiplexed addressing is used to input 8 row and 8 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the KM41464A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 8 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41464A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse width are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41464A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The four outputs of the KM41464A remains in the Hi-Z state until valid data appears at the output. The KM41464A has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41464A can perform early write, and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the outputs remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the outputs before and during the time that data is being written into the same cell locations. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM41464's DQ pins.

Data Output

The KM41464A has tri-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. When either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs first remains in the Hi-Z state until the data is valid and then the valid data appears at the outputs. The valid data remains at the outputs until $\overline{CAS}$ or $\overline{OE}$ returns high. This is true even if a new RAS cycle occurs (as in hidden refresh). Each of the KM41464A operating cycles are listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Page Mode Read, Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Page Mode write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM41464A is stored on a tiny capacitor within each memory cell. Due to leakage, the data will leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 4 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method

KM41464A OPERATION (Continued)

for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This must be performed on each of the 256 row addresses (A_0-A_7) every 4ms.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh: The KM41464A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs and the on-chip refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41464A hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required in hidden refresh cycles by DRAMS that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Other Refresh Methods: It is also possible to refresh the KM41464A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh are the preferred methods.

Page Mode

Page mode memory cycles provide faster access and lower power dissipaton than normal memory cycles. In page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS}$=V_{SS} during power-up the KM41464A might begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 100μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 4 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41464A inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41464A input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMs.

Decoupling

The importance of proper decoupling cannot be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). The total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.3μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41464A using the shortest possible traces.

KM41464A OPERATION (Continued)

These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41464A and they supply much of the current used by the KM41464A during cycling.

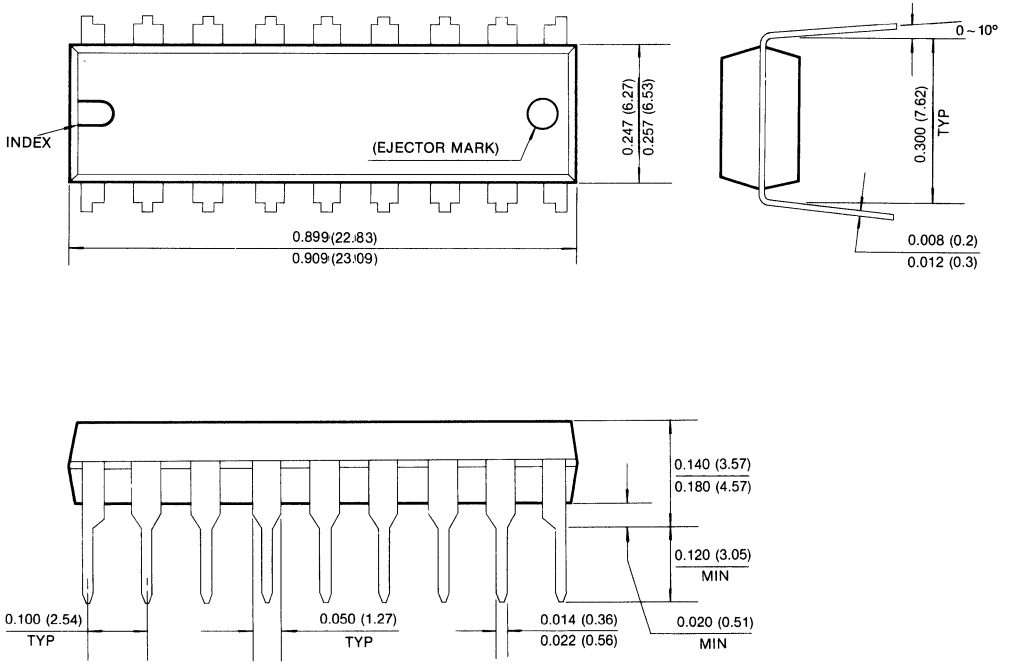
In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.3μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

2

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

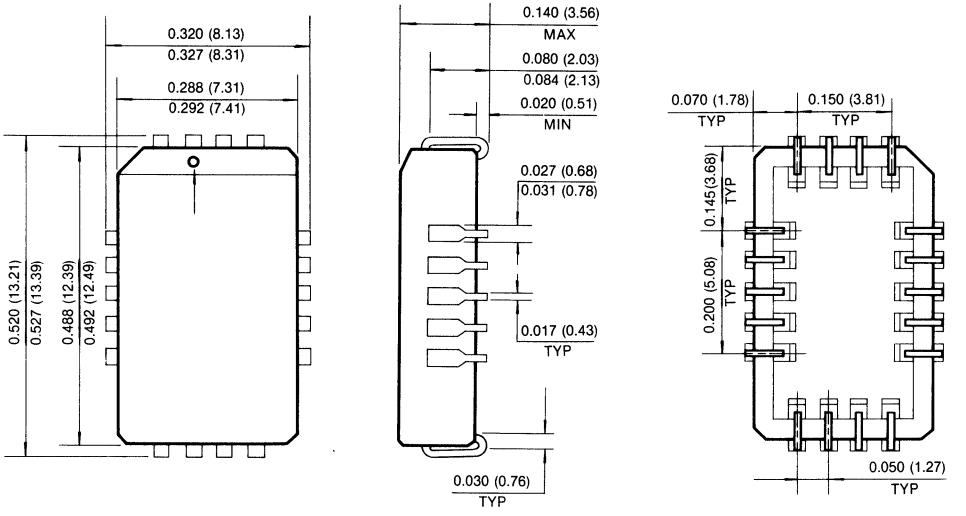
Units: Inches (millimeters)



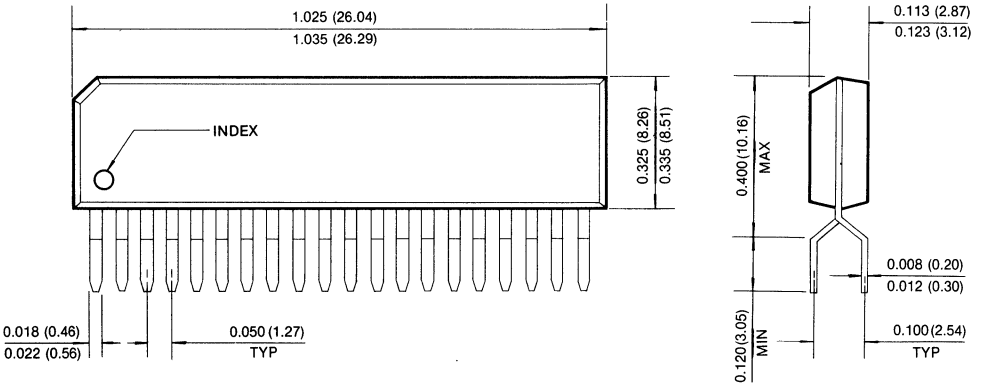
PACKAGE DIMENSIONS (Continued)

18-PIN PLASTIC LEADED CHIP CARRIER

Units: Inches (millimeters)



20-PIN PLASTIC ZIGZAG-IN-LINE PACKAGE



1M x 1 Bit Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C1000-10	100ns	25ns	190ns
KM41C1000-12	120ns	30ns	220ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh**
- **$\overline{RAS}$-only and Hidden Refresh**
- **TTL compatible inputs and output**
- **Common I/O using early write**
- **Single +5V ± 10% power supply**
- **512 cycle/8ms refresh**
- **256K x 4 fast test mode**
- **JEDEC standard pinout available in Plastic DIP, SOJ, ZIP packages.**

GENERAL DESCRIPTION

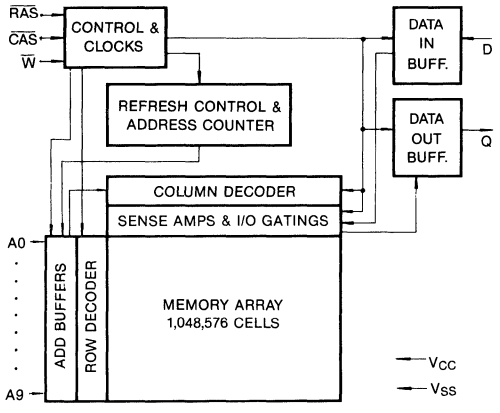
The Samsung KM41C1000 is a CMOS high speed 1,048,576 x 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C1000 features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

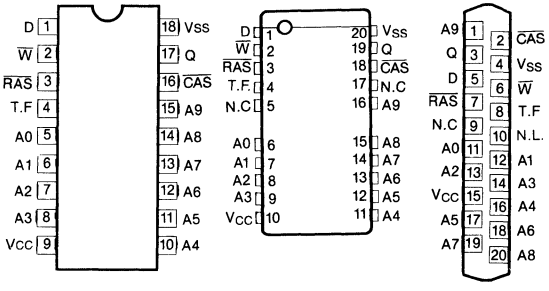
The KM41C1000 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

- **KM41C1000P** - **KM41C1000J** - **KM41C1000Z**



Pin Name	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D	Data In
Q	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
T.F.	Test Function
N.C.	No Connection
N.L.	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	0.6	W
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling; @t_{RC} = min.)	KM41C1000-10	I_{CC1}	—	60	mA
	KM41C1000-12		—	50	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; @t_{RC} = min.)	KM41C1000-10	I_{CC3}	—	60	mA
	KM41C1000-12		—	50	mA
FAST PAGE MODE CURRENT* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; @t_{PC} = min.)	KM41C1000-10	I_{CC4}	—	40	mA
	KM41C1000-12		—	30	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC} = min.)	KM41C1000-10	I_{CC6}	—	60	mA
	KM41C1000-12		—	50	mA
INPUT LEAKAGE CURRENT (Any input, 0≤V_{IN}≤6.5V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤5.5V, Vcc = 5.5V, Vss = 0V,)		I_{OL}	−10	10	μA
OUTPUT HIGH VOLTAGE LEVEL (I_{OH} = −5mA)		V_{OH}	2.4	—	V
OUTPUT LOW VOLTAGE LEVEL (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance ($A_0 - A_9$)	C_{IN2}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1,2)

STANDARD OPERATION

Parameter	Symbol	KM41C1000-10		KM41C1000-12		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	190		220		ns	
Read-modify-write cycle time	t_{RWC}	220		255		ns	
Access time from $\overline{RAS}$	t_{RAC}		100		120	ns	3, 4, 10
Access time from $\overline{CAS}$	t_{CAC}		25		30	ns	3, 4, 5
Access time from column address	t_{AA}		50		60	ns	3, 10
Access time from $\overline{CAS}$ precharge	t_{CPA}		55		65	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3
Output buffer turn-off delay time	t_{OFF}	0	30	0	35	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		ns	
$\overline{CAS}$ precharge time (except fast page mode cycle)	t_{CPN}	15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	75	25	90	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	95		115		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	50		60		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	20	50	20	60	ns	10
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8

STANDARD OPERATION (Continued)

Parameter	Symbol	KM41C1000-10		KM41C1000-12		Unit	Notes
		Min	Max	Min	Max		
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	20		25		ns	
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		30		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25		30		ns	
Data-in set-up time	t_{DS}	0		0		ns	9
Data-in hold time	t_{DH}	20		25		ns	9
$\overline{CAS}$ to write enable delay time	t_{CWD}	25		30		ns	7
$\overline{RAS}$ to write enable delay time	t_{RWD}	100		120		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	50		60		ns	7
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	95		115		ns	
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	95		115		ns	
Refresh period (512 cycles)	t_{REF}		8		8	ms	

FAST PAGE MODE

Page mode cycle time	t_{PC}	60		70		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		15		ns	
Fast page mode read-modify-write	t_{PRWC}	90		105		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	100	100,000	120	100,000	ns	

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

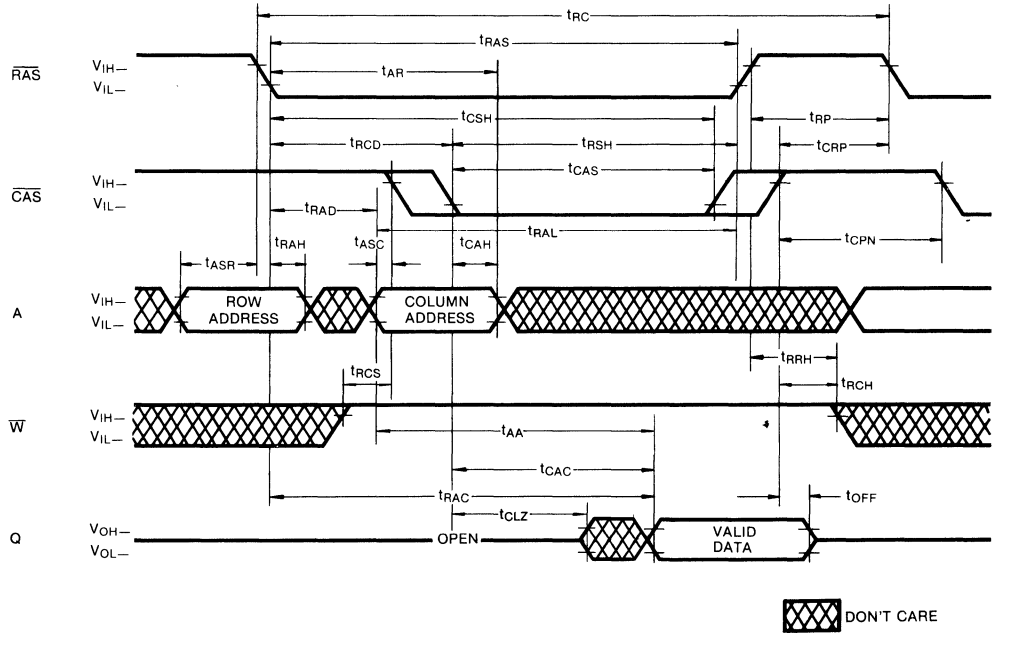
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		ns	
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	50		60		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
11. Normal operation requires the "T.F" pin to be connected to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
12. When the "T.F" pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung Semiconductor for specific operational details of the "test function".

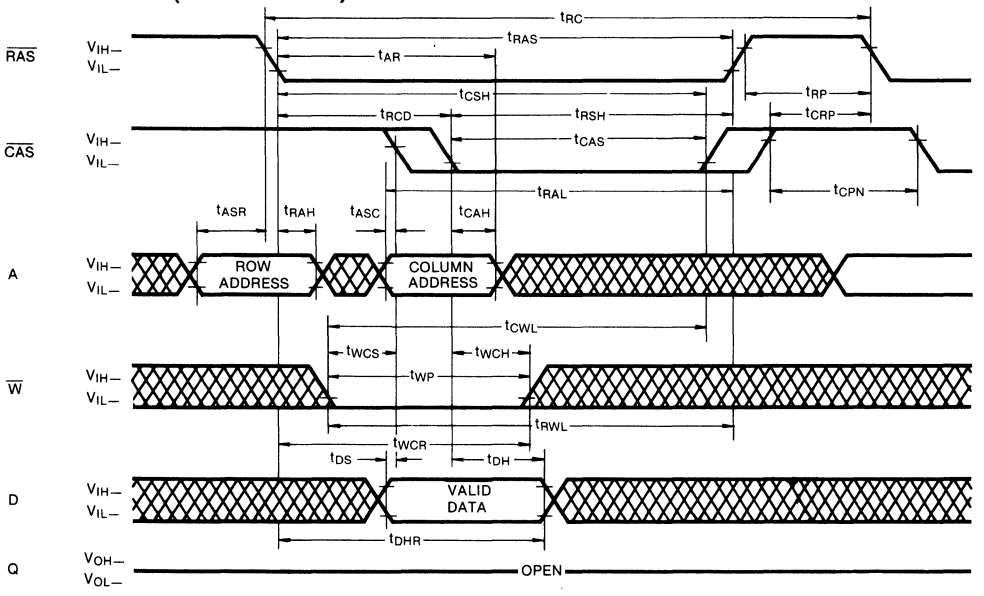
TIMING DIAGRAMS

READ CYCLE

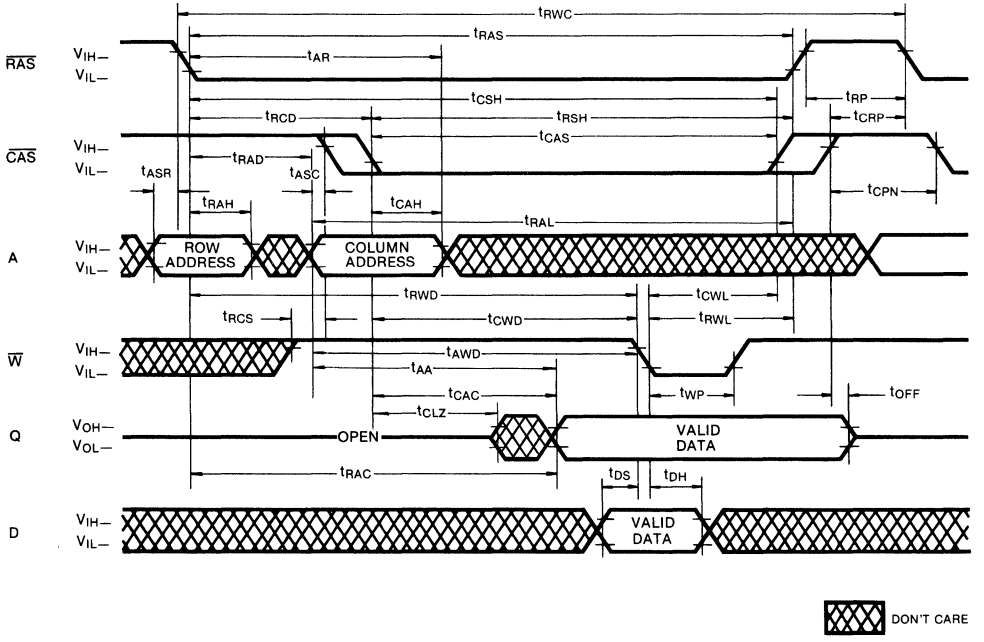


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

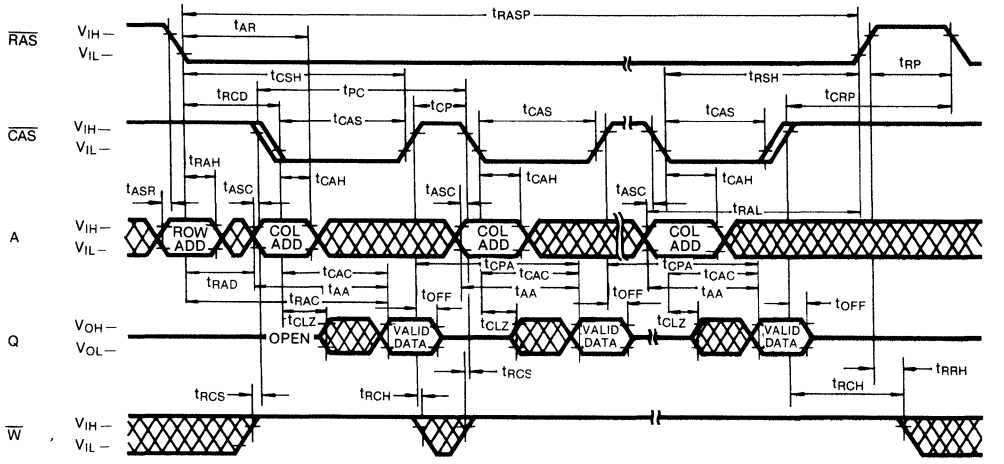


READ-WRITE/READ-MODIFY-WRITE CYCLE

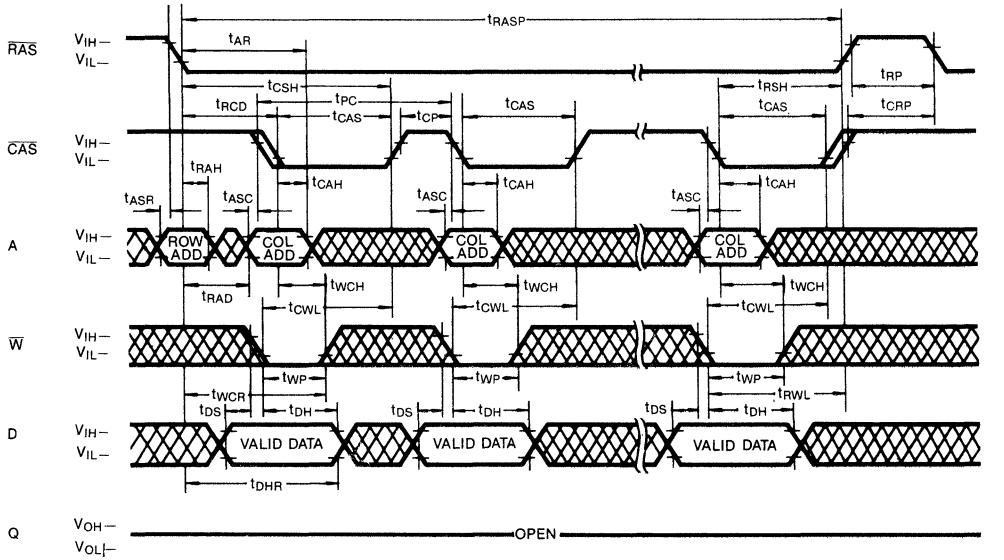


TIMING DIAGRAMS

FAST PAGE MODE READ CYCLE



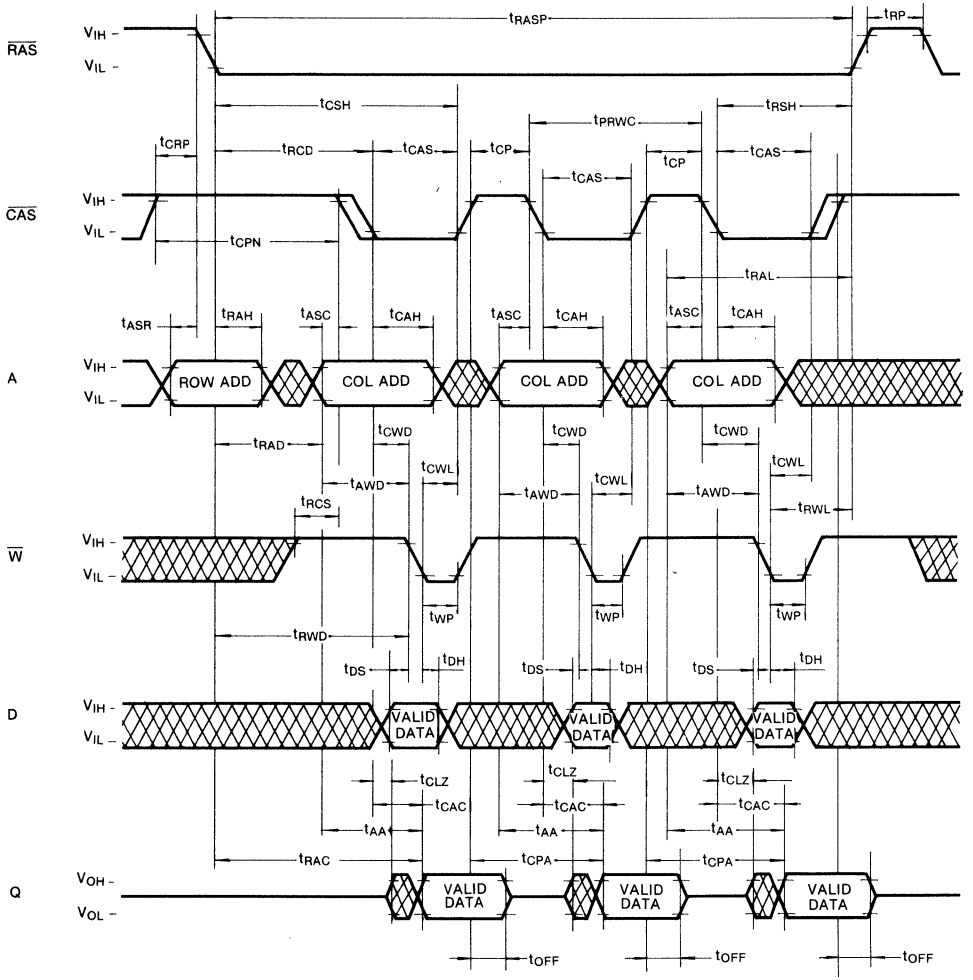
FAST PAGE MODE WRITE CYCLE



DON'T CARE

TIMING DIAGRAMS (Continued)

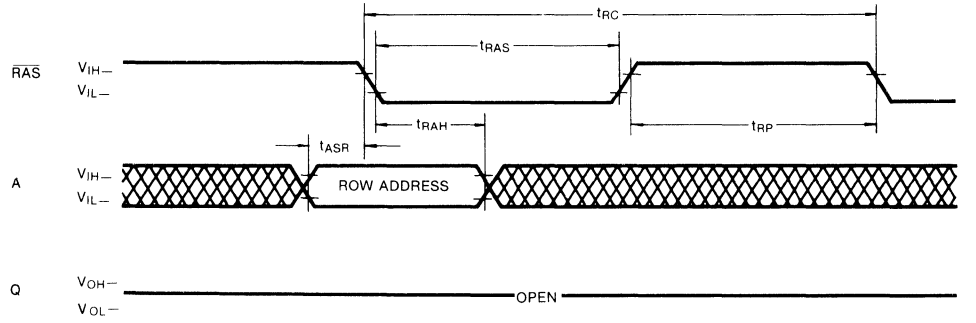
FAST PAGE MODE READ-WRITE CYCLE



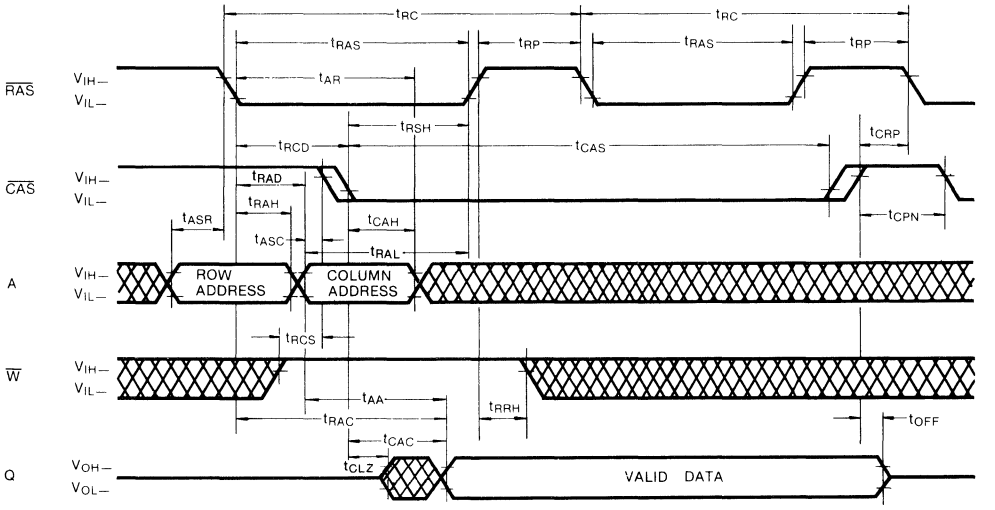
TIMING DIAGRAMS (Continued)

$\overline{RAS}$-ONLY REFRESH CYCLE

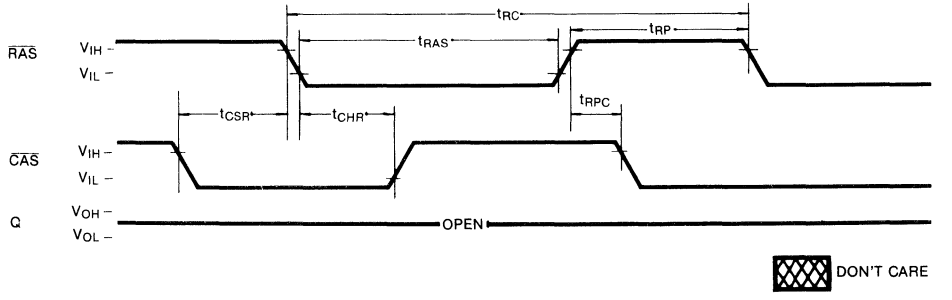
Note: $\overline{CAS}$ = V_{IH}, $\overline{W}$,D, A_9 = Don't Care



HIDDEN REFRESH CYCLE

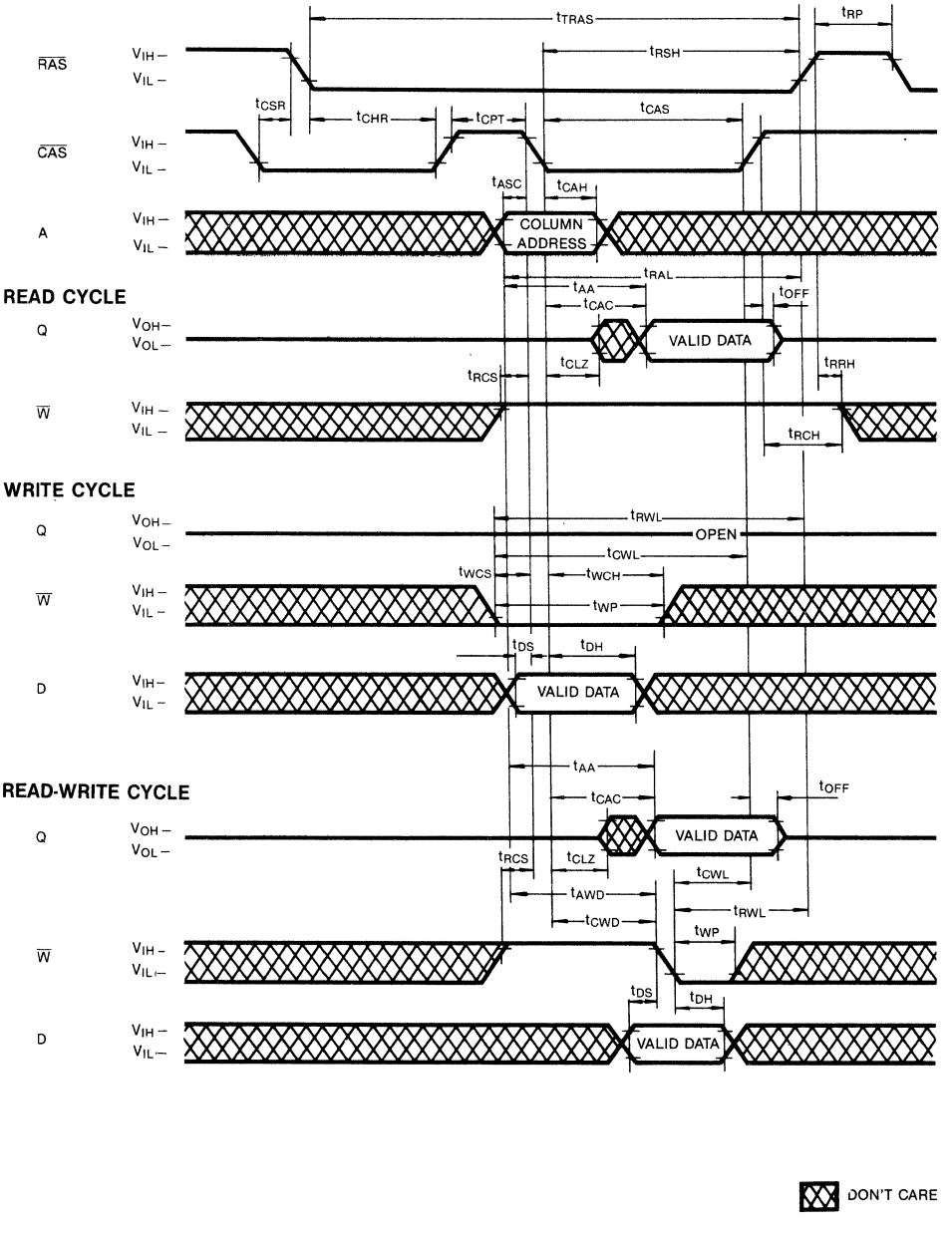


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



KM41C1000 OPERATION

Device Operation

The KM41C1000 contains 1,048,576 memory locations. Twenty address bits are required to address a particular memory location. Since the KM41C1000 has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM41C1000 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C1000 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (tRP) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by tRAS(min) and tCAS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C1000 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before tRCD(max) and if the column address is valid before tRAD(max) then the access time to valid data is specified by tRAC(min). However, if $\overline{CAS}$ goes low after tRCD(max) or if the column address becomes valid after tRAD(max), the access time is specified by tCAC or tAA. In order to achieve the minimum access time, tRAC(min), it is necessary to meet both tRCD(max) and tRAD(max).

Write

The KM41C1000 can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, tRWD, tCWD and tAWD, are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C1000 has a tri-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (VIH) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by tCLZ after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after tCLZ and before the valid data appears at the output. The timing parameters tCAC, tRAC and tAA specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C1000 operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C1000 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A0-A8). The state of address A9 is ignored during refresh.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C1000 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (tCSR) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C1000 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C1000 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter. The A9 bit is set high internally.

Fast Page Mode

The KM41C1000 has Fast Page mode capability which provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM41C1000 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C1000 inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C1000 input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

DEVICE OPERATION (Continued)

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the VCC to VSS voltage (measured at the device pins) should not exceed 500mV.

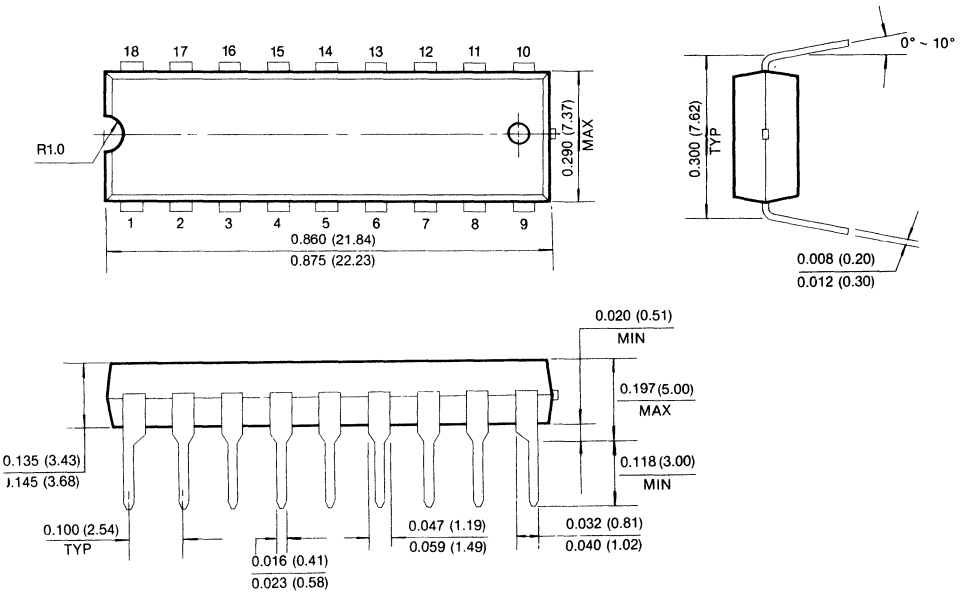
A high frequency 0.3μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41C1000 using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C1000 and they supply much of the current used by the KM41C1000 during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.3μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

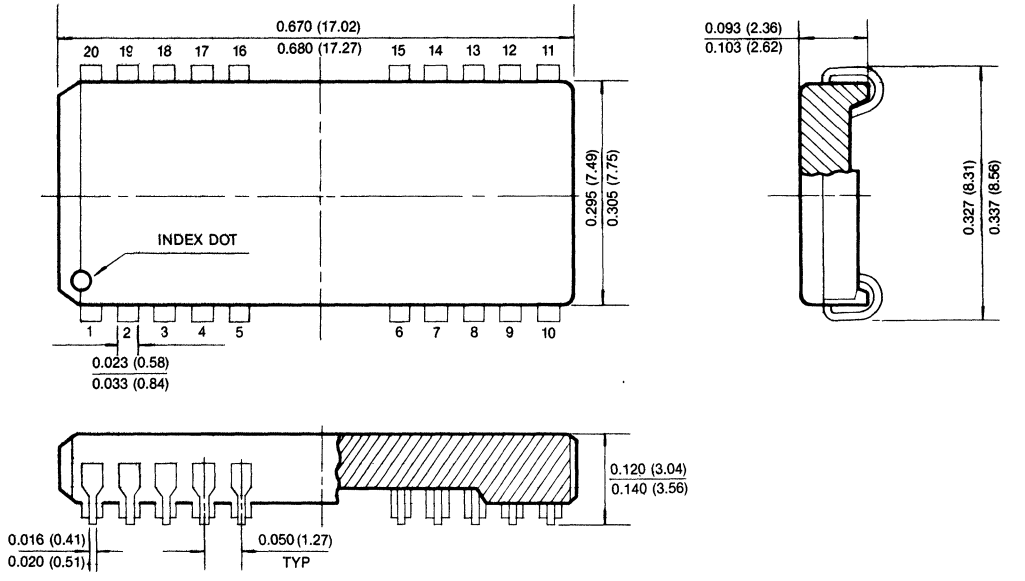
Units: Inches (millimeters)



PACKAGE DIMENSIONS

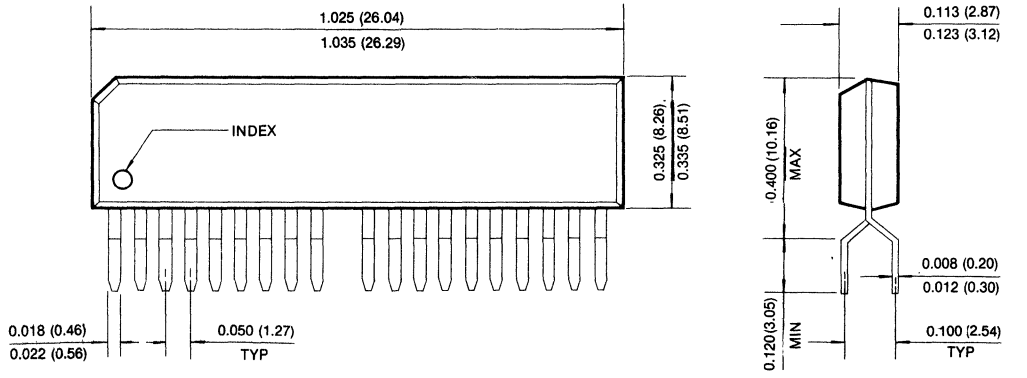
20/26-PIN PLASTIC SMALL OUT-LINE J-LEAD

Unit: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



2

1M x 1 Bit Dynamic RAM with Nibble Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C1001-10	100ns	25ns	190ns
KM41C1001-12	120ns	30ns	220ns

- **Nibble Mode Operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh**
- **$\overline{RAS}$-only and Hidden Refresh**
- **TTL compatible inputs and output**
- **Common I/O using early write**
- **Single +5V ± 10% power supply**
- **512 cycle/8ms refresh**
- **256K x 4 fast test mode**
- **JEDEC standard pinout available in Plastic DIP, SOJ, ZIP packages.**

GENERAL DESCRIPTION

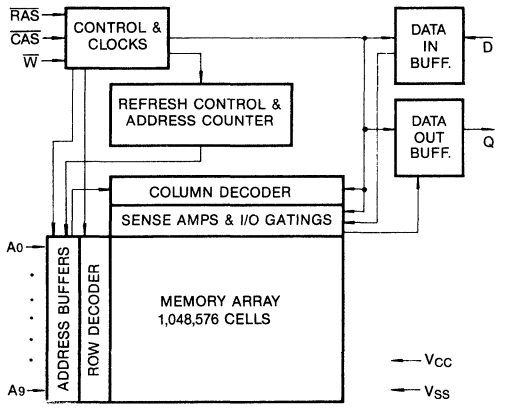
The Samsung KM41C1001 is a CMOS high speed 1,048,576 x 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C1001 features Nibble Mode operation which allows high speed random access of up to 4-bits of data.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

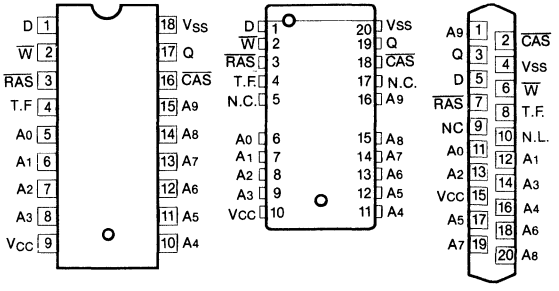
The KM41C1001 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

- **KM41C1001P** • **KM41C1001J** • **KM41C1001Z**



Pin Name	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D	Data In
Q	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
T.F.	Test Function
N.C.	No Connection
N.L.	No Lead

1M x 1 Bit Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C1002-10	100ns	25ns	190ns
KM41C1002-12	120ns	30ns	220ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and output**
- **Common I/O using 'Early Write'**
- **Single +5V ± 10% power supply**
- **512 cycles/8ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic DIP, SOJ and ZIP**

GENERAL DESCRIPTION

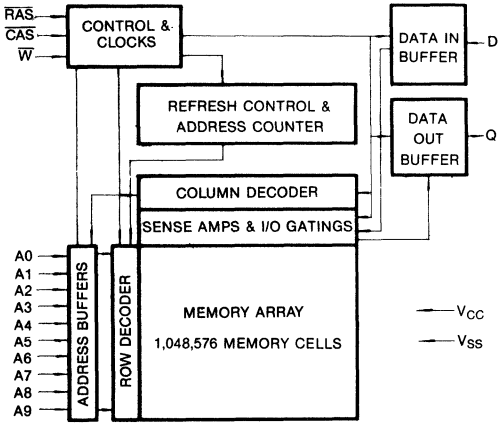
The Samsung KM41C1002 is a CMOS high speed 1,048,576 x 1 dynamic Random Access Memory. Its design is optimized for high performance applications such as cache based mainframes and mini computers, graphics, digital signal processing and high performance microprocessor systems.

Static Column Mode Operation allows high speed random or Sequential access within a row. The KM41C1002 offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

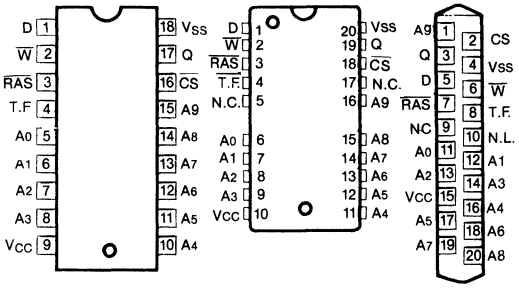
The KM41C1002 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

- **KM41C1002P** - **KM41C1002J** - **KM41C1002Z**



Pin Name	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
$\overline{W}$	Read/Write Input
D	Data In
Q	Data Out
T.F.	Test Function
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection
N.L.	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC} = min)	KM41C1002-10 KM41C1002-12	I_{CC1}	— —	60 50	mA mA
Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CS}$ = V_{IH}, $\overline{RAS}$ Cycling @t_{RC} = min)	KM41C1002-10 KM41C1002-12	I_{CC3}	— —	60 50	mA mA
Static Column Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CS}$ = V_{IL} @t_{SC} = min)	KM41C1002-10 KM41C1002-12	I_{CC4}	— —	40 30	mA mA
Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{SC} = min)	KM41C1002-10 KM41C1002-12	I_{CC6}	— —	60 50	mA mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test = 0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq 5.5V$		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance (A_0-A_9)	C_{IN2}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1.2)

STANDARD OPERATION

Parameter	Symbol	KM41C1002-10		KM41C1002-12		Units	Notes
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	190		220		ns	
Read-modify-write Cycle Time	t_{RWC}	220		255		ns	
Static Column Mode Cycle Time	t_{SC}	55		65		ns	
Static Column Mode Read-write Cycle Time	t_{SRWC}	100		120		ns	
Access Time from $\overline{RAS}$	t_{RAC}		100		120	ns	3, 4, 10
Access Time from $\overline{CS}$	t_{CAC}		25		30	ns	3, 4, 5
Access Time from Column Address	t_{AA}		50		60	ns	3, 10
Access Time from Last Write	t_{ALW}		95		115	ns	3, 11
$\overline{CS}$ to Output in Low-Z	t_{CLZ}	5		5		ns	3
Output Buffer Turn-off Delay Time	t_{OFF}	0	30	0	35	ns	6
Output Data Hold Time from Column Address	t_{AOH}	5		5		ns	
Output Data Enable Time from $\overline{W}$	t_{OW}		70		85	ns	
Output Data Hold Time from $\overline{W}$	t_{WOH}	0		0		ns	
Transition Time (rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ Precharge Time	t_{RP}	80		90		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10,000	120	10,000	ns	
$\overline{RAS}$ Pulse Width (static column mode)	t_{RASC}	100	100,000	120	100,000	ns	
$\overline{CS}$ to $\overline{RAS}$ Hold Time	t_{RSH}	25		30		ns	
$\overline{RAS}$ to $\overline{CS}$ Hold Time	t_{CSH}	100		120		ns	
$\overline{CS}$ Pulse Width	t_{CS}	25		30		ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RCD}	25	75	25	90	ns	4
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	50	20	60	ns	10
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		ns	
$\overline{CS}$ Precharge Time (static column mode)	t_{CP}	10		15		ns	
Row Address Set-up Time	t_{ASR}	0		0		ns	
Row Address Hold Time	t_{RAH}	15		15		ns	
Column Address Set-up Time	t_{ASC}	0		0		ns	
Column Address Hold Time	t_{CAH}	20		25		ns	
Write Address Hold Time Referenced to $\overline{RAS}$	t_{AWR}	95		115		ns	

STANDARD OPERATION (Continued)

Parameter	Symbol	KM41C1002-10		KM41C1002-12		Units	Notes
		Min	Max	Min	Max		
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	115		140		ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	50		60		ns	
Column Address Hold Time Referenced to $\overline{RAS}$ Rise	t_{AH}	10		15		ns	
Write Command to $\overline{CS}$ Lead Time	t_{CWL}	25		30		ns	
Last Write to Column Address Delay Time	t_{LWAD}	25	45	30	55	ns	
Last Write to Column Address Hold Time	t_{AHLW}	95		115		ns	
Read Command Set-up Time Referenced to $\overline{RAS}$	t_{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{CS}$	t_{RCH}	0		0		ns	8
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write Command Hold Time	t_{WCH}	20		25		ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	95		115		ns	
Write Command Pulse Width	t_{WP}	20		25		ns	
Write Command Inactive Time	t_{WI}	10		15		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25		30		ns	
Data-in Set-up Time	t_{DS}	0		0		ns	9
Data-in Hold Time	t_{DH}	20		25		ns	9
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	95		115		ns	
Refresh Period (512 cycles)	t_{REF}		8		8	ms	
Write Command Set-up Time	t_{WCS}	0		0		ns	7
$\overline{CS}$ to Write Enable Delay Time (read-write cycle)	t_{CWD}	25		30		ns	7
$\overline{RAS}$ to Write Enable Delay Time (read-write cycle)	t_{RWD}	100		120		ns	7
Column Address to $\overline{W}$ Delay Time	t_{AWD}	50		60		ns	7
$\overline{CS}$ Setup Time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	
$\overline{CS}$ Hold Time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	30		30		ns	
$\overline{RAS}$ Precharge to $\overline{CS}$ Hold Time	t_{RPC}	10		10		ns	
$\overline{CS}$ Precharge Time (refresh counter test)	t_{CPT}	50		60		ns	
$\overline{CS}$ Precharge Time	t_{CPN}	15		20		ns	

NOTES

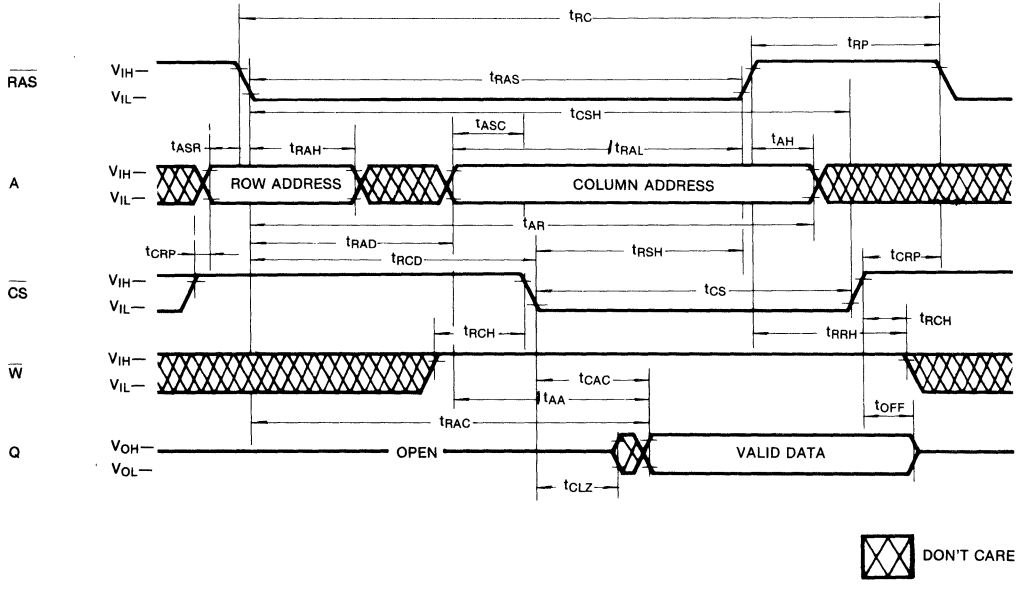
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

NOTES (Continued)

5. Assumes that $t_{RCD} \geq t_{RCD}(max)$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}(min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(min)$, $t_{RWD} \geq t_{RWD}(min)$ and $t_{AWD} \geq t_{AWD}(min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RAD}(max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled by t_{AA}.
11. Operation within the $t_{LWAD}(max)$ limit insures that $t_{ALW}(max)$ can be met. $t_{LWAD}(max)$ is specified as a reference point only. If t_{LWAD} is greater than the specified $t_{LWAD}(max)$ limit, then access time is controlled by t_{AA}.
12. Normal operation requires the "T.F." pin to be connected to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
13. When the "T.F." pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung Semiconductor for specific operational details of the "test function".

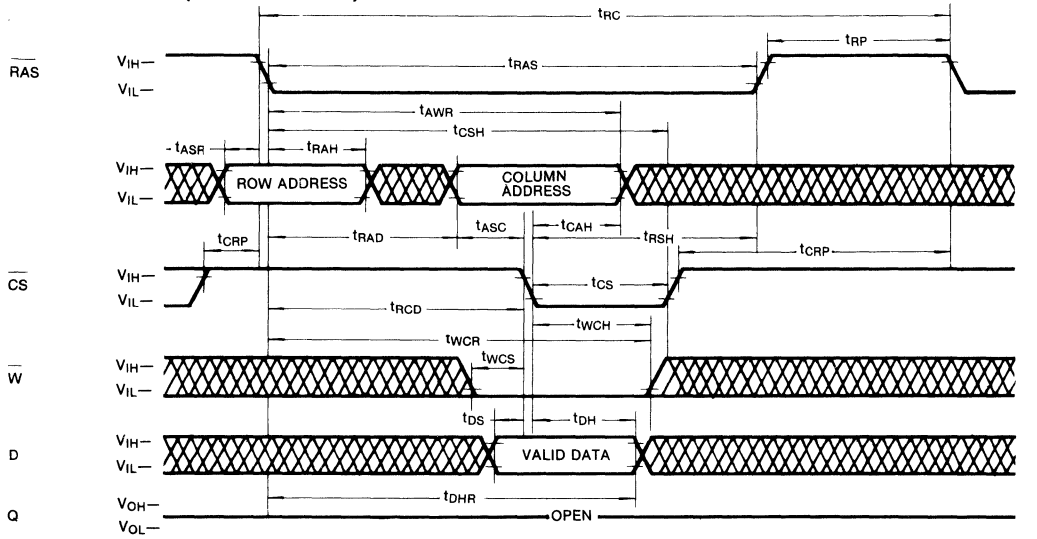
TIMING DIAGRAMS

READ CYCLE

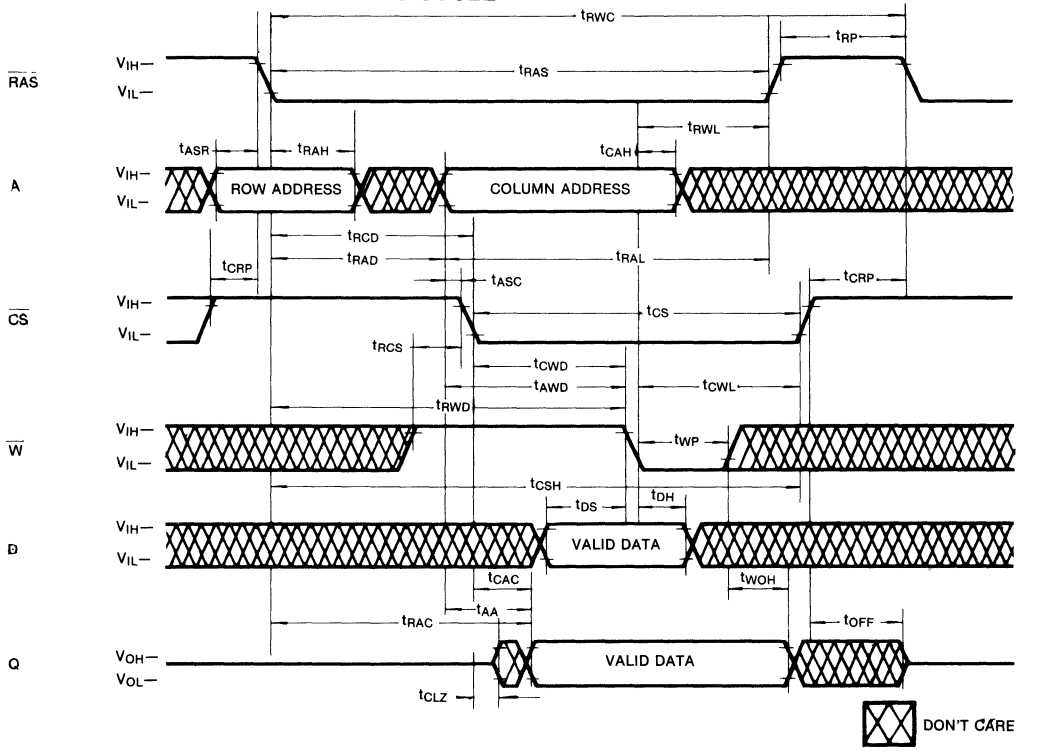


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

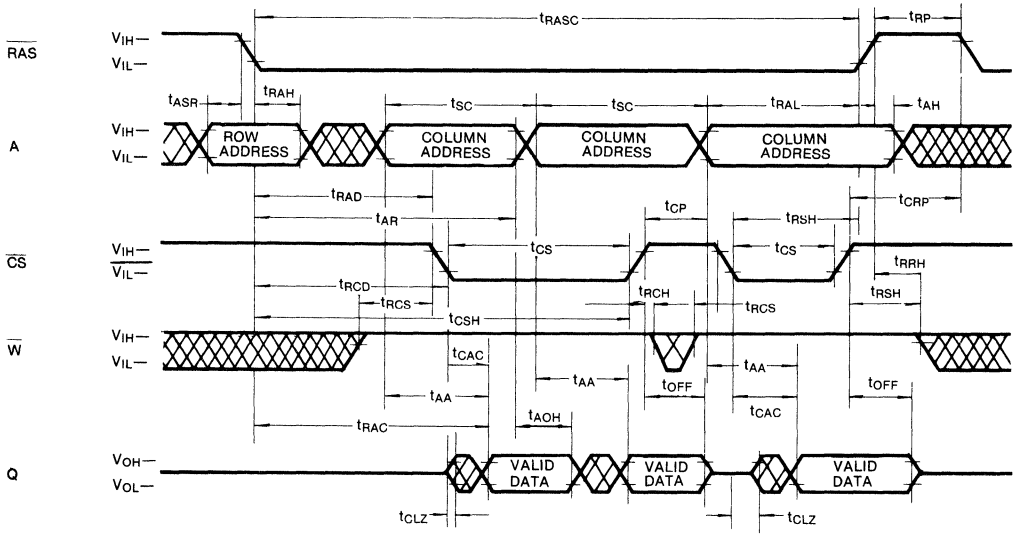


READ-WRITE/READ-MODIFY-WRITE CYCLE

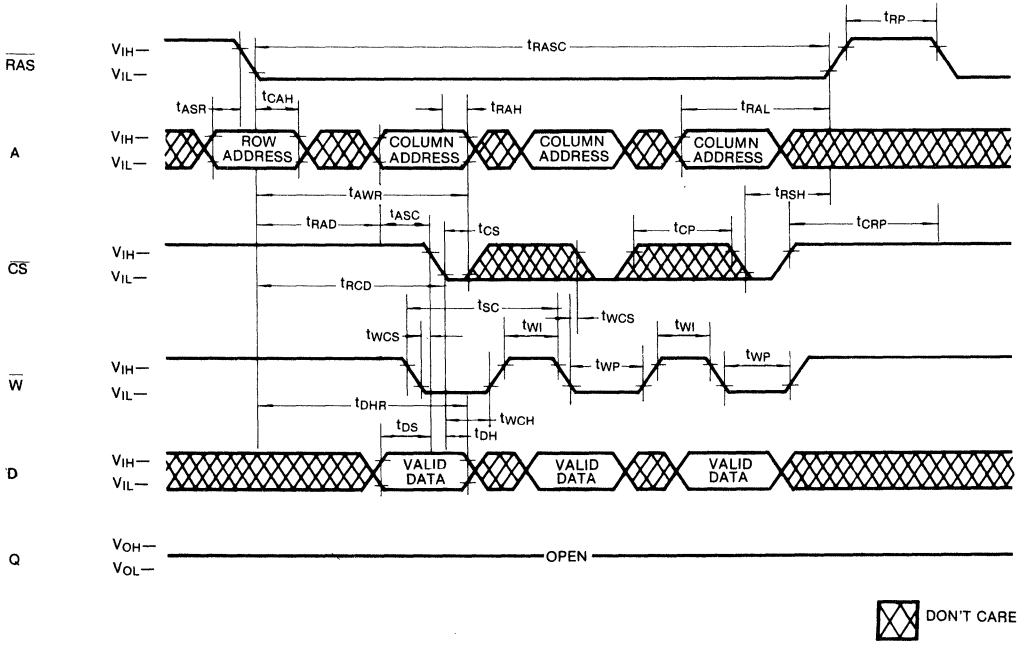


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ CYCLE

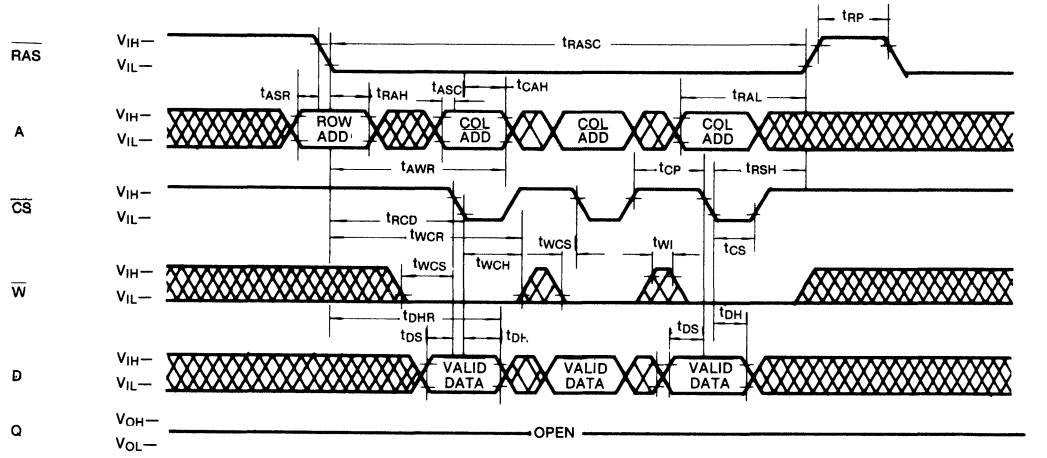


STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ controlled early write)

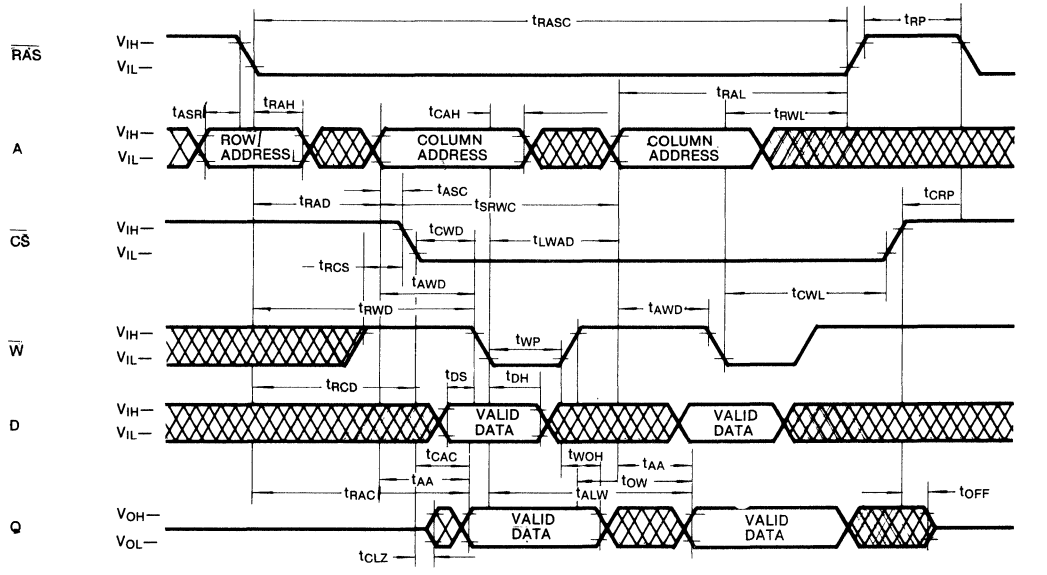


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)

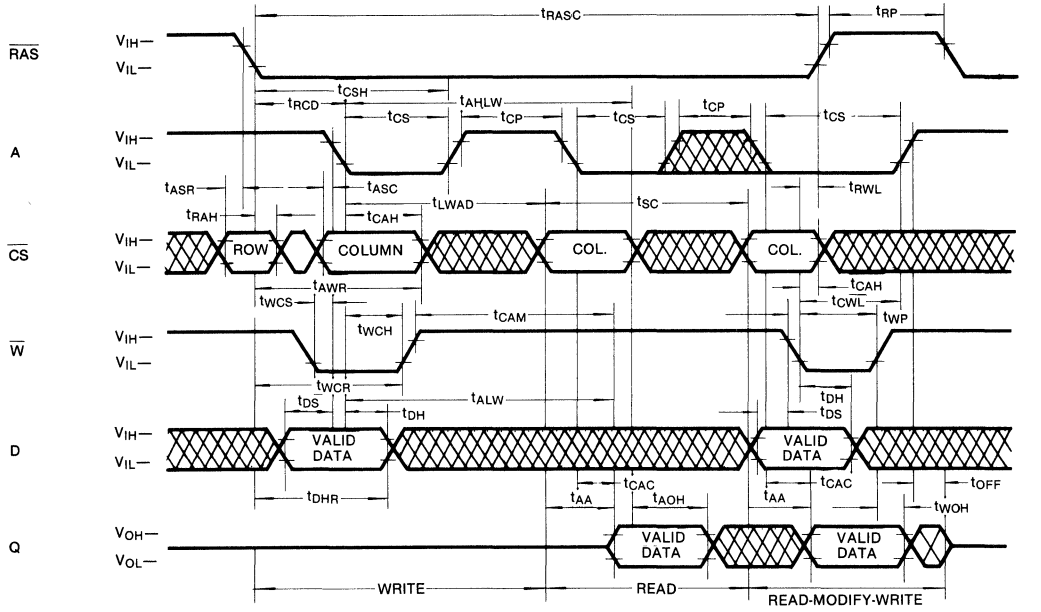


STATIC COLUMN MODE READ-WRITE CYCLE



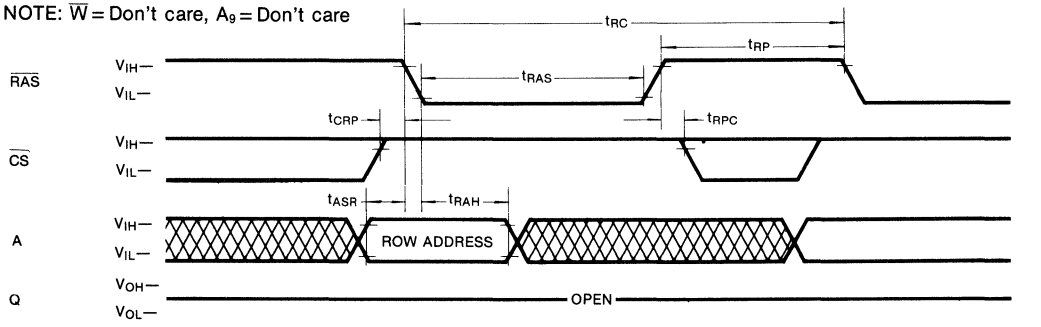
TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE MIXED CYCLE

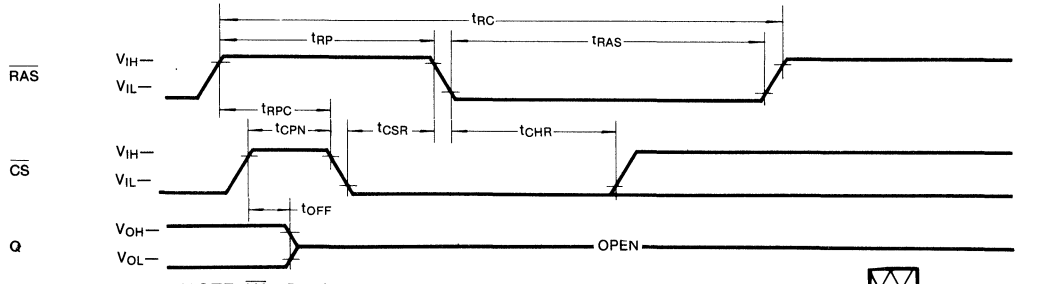


RAS-ONLY REFRESH CYCLE

NOTE: $\overline{W}$ = Don't care, A_9 = Don't care



CS-BEFORE-RAS REFRESH CYCLE

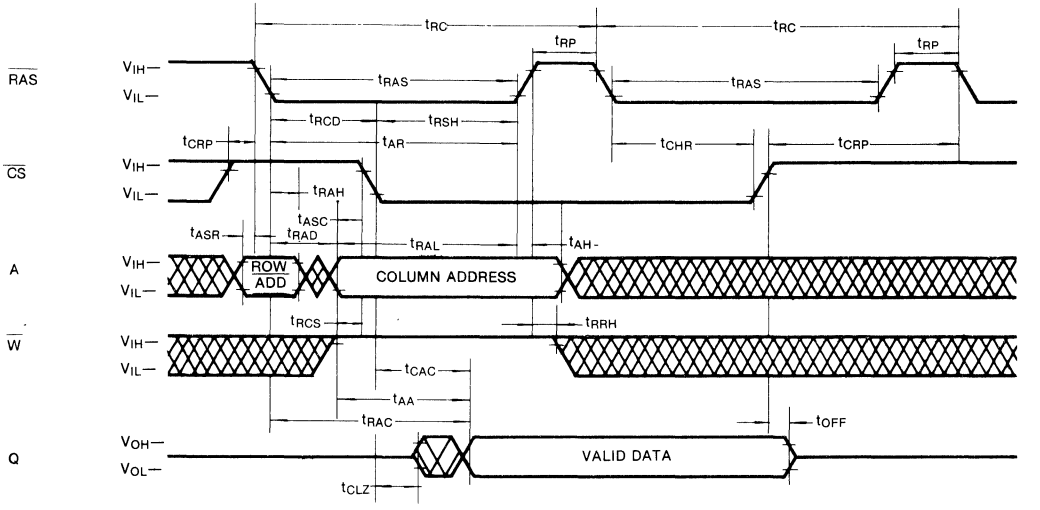


NOTE: $\overline{W}$ = Don't care, A_0-A_9 = Don't care

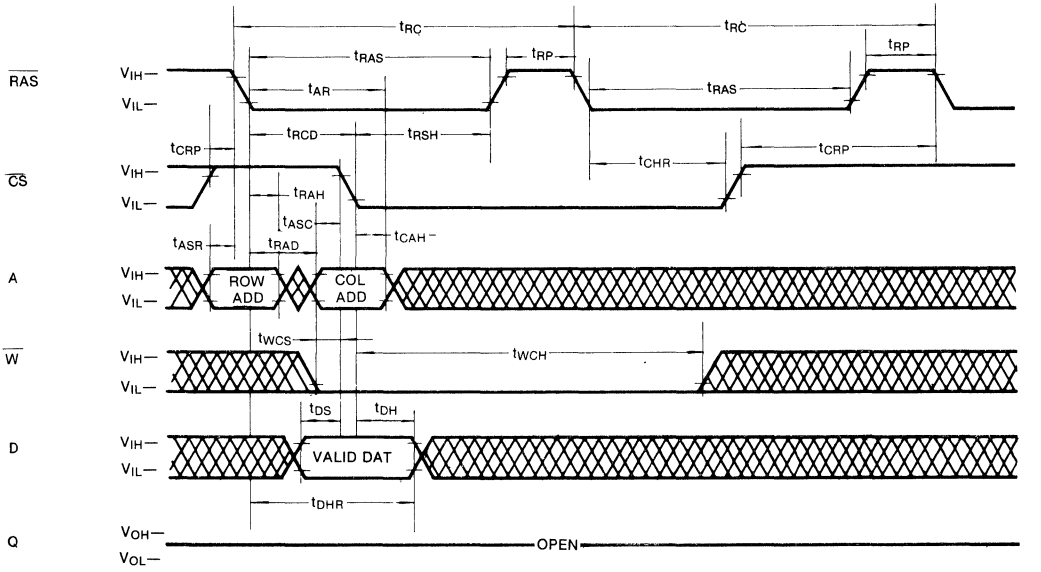
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



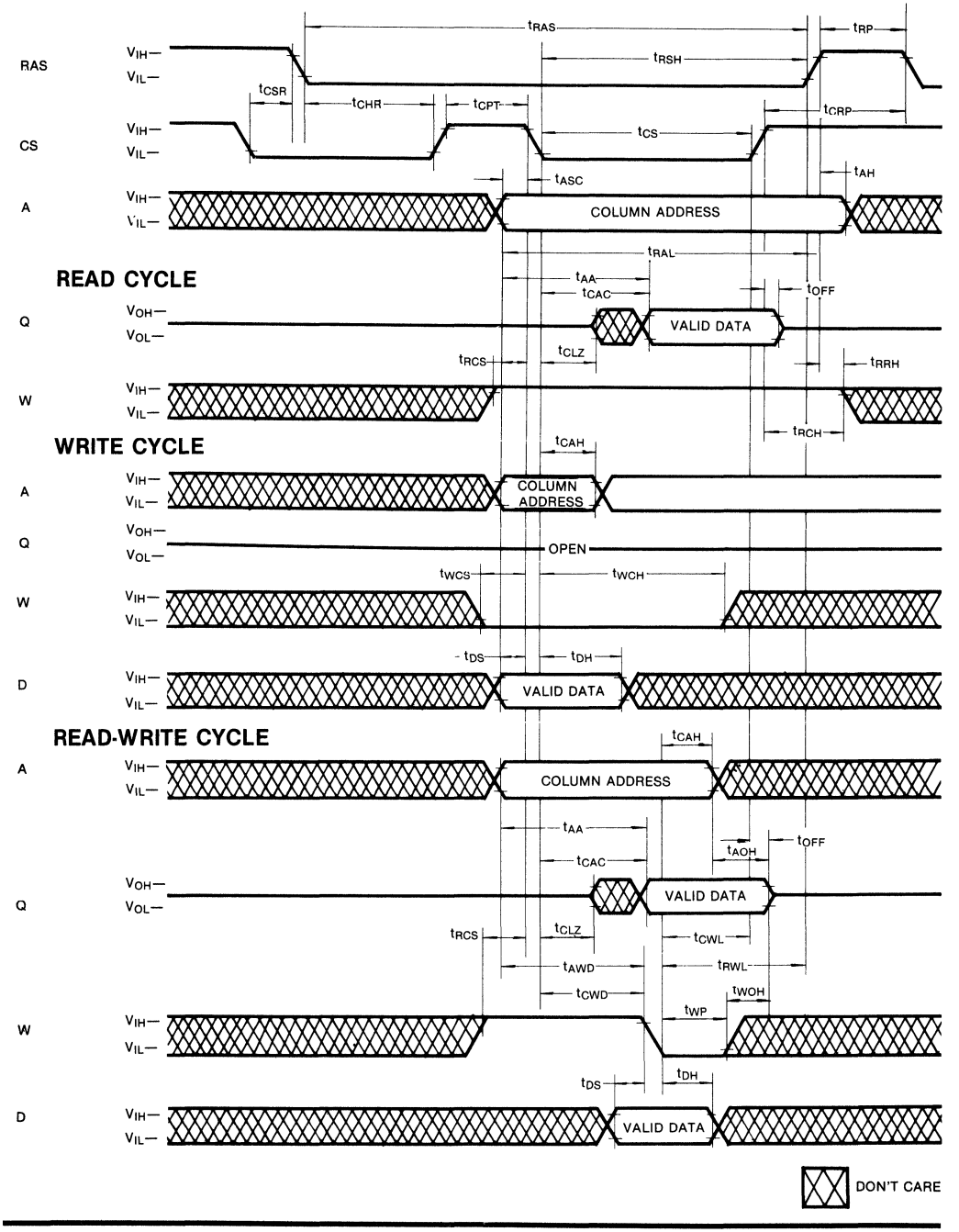
HIDDEN REFRESH CYCLE (WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

CS-BEFORE-RAS BEFRESH COUNTER TEST CYCLE



KM41C1002 OPERATION

Device Operation

The KM41C1002 contains 1,048,576 memory locations. Twenty address bits are required to address a particular memory location. Since the KM41C1002 has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CS}$) and the valid row and column address inputs.

Operation of the KM41C1002 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM41C1002 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the RAS precharge time (tRP) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by tRAS(min) and tCAS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C1002 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before tRCD(max) and if the column address is valid before tRAD(max) then the access time to valid data is specified by tRAC(min). However, if $\overline{CS}$ goes low after tRCD(max) or if the column address becomes valid after tRAD(max), access is specified by tCAC or tAA. In order to achieve the minimum access time, tRAC(min), it is necessary to meet both tRCD(max) and tRAD(max).

Write

The KM41C1002 can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between W and $\overline{CS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of W or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, tRWD, tCWD and tAWD, are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C1002 has a tri-state output buffer which is controlled by $\overline{CS}$. Whenever $\overline{CS}$ is high (VIH) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by tCLZ after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after tCLZ and before the valid data appears at the output. The timing parameters tCAC, tRAC and tAA specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C1002 operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write, Nibble Mode Read, Nibble Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, Nibble Mode Write, $\overline{CS}$-before-RAS Refresh, $\overline{CS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C1002 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A0-A8). The state of address A9 is ignored during refresh.

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM41C1002 has $\overline{CS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If CS is held low for the specified set up time (tCSR) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM41C1002 hidden refresh cycle is actually a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C1002 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter. The A9 bit is set high internally.

Static Column Mode

Static column mode allows high speed read, write or read-modify-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or read-modify-write cycles may be mixed in any order.

A static column mode read cycle starts as a normal cycle. Additional cells within the selected row are read by applying a new column address while $\overline{W}$ = VIH and $\overline{RAS}$ = VIL.

A static column mode write cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{RAS}$ = VIL and toggling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell triggered by the latter falling edge of W or $\overline{CS}$.

A static column mode read-modify-write cycle starts as a normal cycle. Additional cells within the selected row are accessed by applying a new column address while $\overline{RAS}$ = VIL and toggling $\overline{W}$. The data and column address are strobbed and latched by the latter falling edge of $\overline{W}$.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM41C1002 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after powerp up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C1002 inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel ter-

DEVICE OPERATION (Continued)

mination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C1002 input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines tb the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the VCC to VSS voltage (measured at the device pins) should not exceed 500mV.

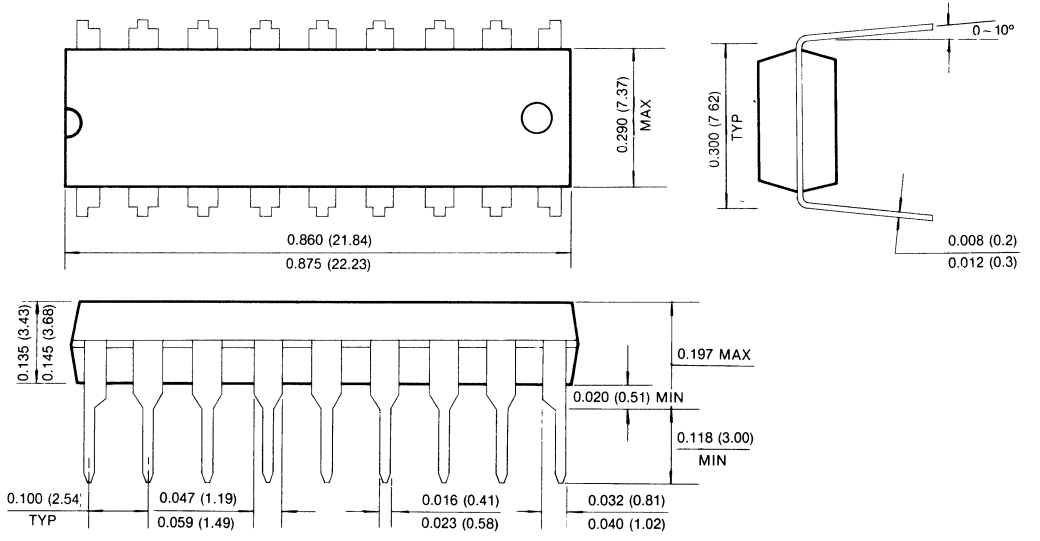
A high frequency 0.3μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41C1002 using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C1002 and they supply much of the current used by the KM41C1002 during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.3μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

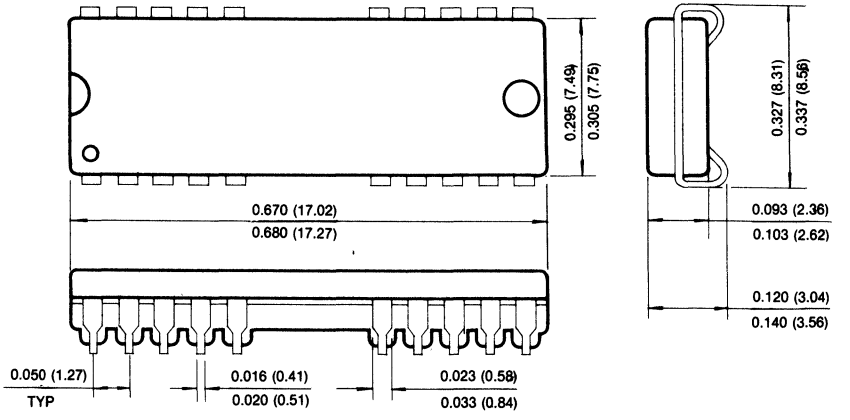
Units: Inches (millimeters)



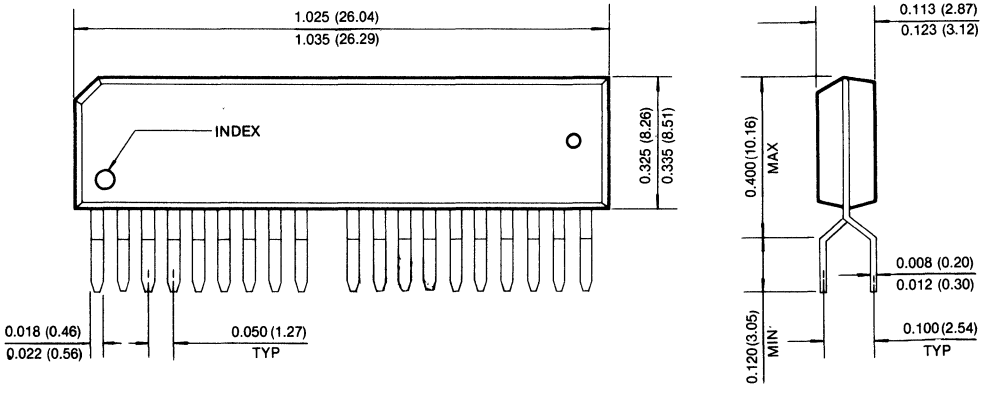
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

units: inches (millimeters)



20-PIN PLASTIC ZIGZAG-IN-LINE PACKAGE



2

256K x 4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C256-10	100ns	25ns	190ns
KM44C256-12	120ns	30ns	220ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and output**
- **Early Write or output Enable Controlled Write**
- **Single +5V ± 10% power supply**
- **512 cycles/8ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic DIP, SOJ and ZIP**

GENERAL DESCRIPTION

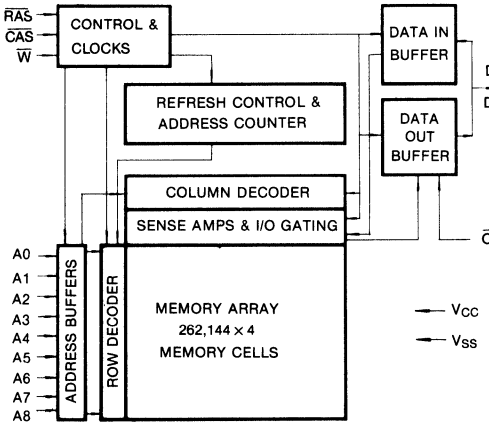
The Samsung KM44C256 is a CMOS high speed 262,144 x 4 dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C256 features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

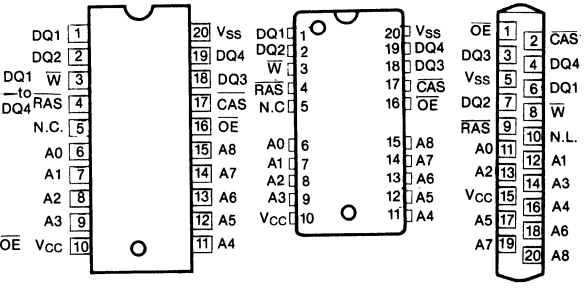
The KM44C256 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

- **KM44C256P** - **KM44C256J** - **KM44C256Z**



Pin Name	Pin Function
A_0-A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1-DQ_4	Data In/Data Out
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection
N.L.	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min)	KM44C256-10 KM44C256-12	I_{CC1}	— —	70 60	mA mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @t_{RC} = min)	KM44C256-10 KM44C256-12	I_{CC3}	— —	70 60	mA mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling @t_{PC} = min)	KM44C256-10 KM44C256-12	I_{CC4}	— —	50 40	mA mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min)	KM44C256-10 KM44C256-12	I_{CC6}	— —	70 60	mA mA
Input Leakage Current (Any input $0 \le V_{IN} \le 6.5V$, all other pins not under test = 0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \le V_{OUT} \le 5.5V$		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	$C_{IN/OUT}$	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1, 2)

Parameter	Symbol	KM44C256-10		KM44C256-12		Units	Notes
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	190		220		ns	
Read-modify-write Cycle Time	t_{RWC}	255		295		ns	
Fast Page Mode Cycle Time	t_{PC}	60		70		ns	
Fast Page Mode Read-modify-write Cycle Time	t_{PRWC}	110		130		ns	
Access Time from $\overline{RAS}$	t_{RAC}		100		120	ns	3, 4, 10
Access Time from $\overline{CAS}$	t_{CAC}		25		30	ns	3, 4, 5
Access Time from Column Address	t_{AA}		50		60	ns	3, 10
Access Time from $\overline{CAS}$ Precharge	t_{CPA}		55		65	ns	3
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	5		5		ns	3
Output Buffer Turn-off Delay	t_{OFF}	0	30	0	35	ns	6
Transition Time (rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ Precharge Time	t_{RP}	80		90		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10,000	120	10,000	ns	
$\overline{RAS}$ Pulse Width (fast page mode)	t_{RASP}	100	100,000	120	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	25		30		ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100		120		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10,000	30	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	75	25	90	ns	4
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	50	20	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		ns	
$\overline{CAS}$ Precharge time	t_{CPN}	15		20			
$\overline{CAS}$ Precharge Time (fast page mode)	t_{CP}	10		15		ns	
Row Address Set-up Time	t_{ASR}	0		0		ns	
Row Address Hold Time	t_{RAH}	15		15		ns	
Column Address Set-up Time	t_{ASC}	0		0		ns	
Column Address Hold Time	t_{CAH}	20		25		ns	
Column Address Hold Time Reference to $\overline{RAS}$	t_{AR}	95		115		ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	50		60		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM44C256-10		KM44C256-12		Units	Notes
		Min	Max	Min	Max		
Read Command Set-up Time	t_{RCS}	0		0		ns	
Read Command Hold Time	t_{RCH}	0		0		ns	8
Read Command Hold Time Reference to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write Command Hold Time	t_{WCH}	20		25		ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	95		115		ns	
Write Command Pulse Width	t_{WP}	20		25		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25		30		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25		30		ns	
Data Set-up Time	t_{DS}	0		0		ns	9
Data Hold Time	t_{DH}	20		25		ns	9
Data Hold Time Referenced to $\overline{RAS}$	t_{DHR}	95		115		ns	
Refresh Period	t_{REF}		8		8	ms	
Write Command Set-up Time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ Delay Time	t_{CWD}	60		70		ns	7
$\overline{RAS}$ to $\overline{W}$ Delay Time	t_{RWD}	135		160		ns	7
Column Address to $\overline{W}$ Delay Time	t_{AWD}	85		100		ns	7
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	t_{CSR}	10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	t_{CHR}	30		30		ns	
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	t_{RPC}	10		10		ns	
$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ counter test cycle)	t_{CPT}	50		60		ns	
$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	t_{ROH}	20		20		ns	
$\overline{OE}$ Access Time	t_{OEA}		25		30	ns	
$\overline{OE}$ to Data Delay	t_{OED}	25		30		ns	
Output Buffer Turn Off Delay Time from $\overline{OE}$	t_{OEZ}	0	25	0	30	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	25		30		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

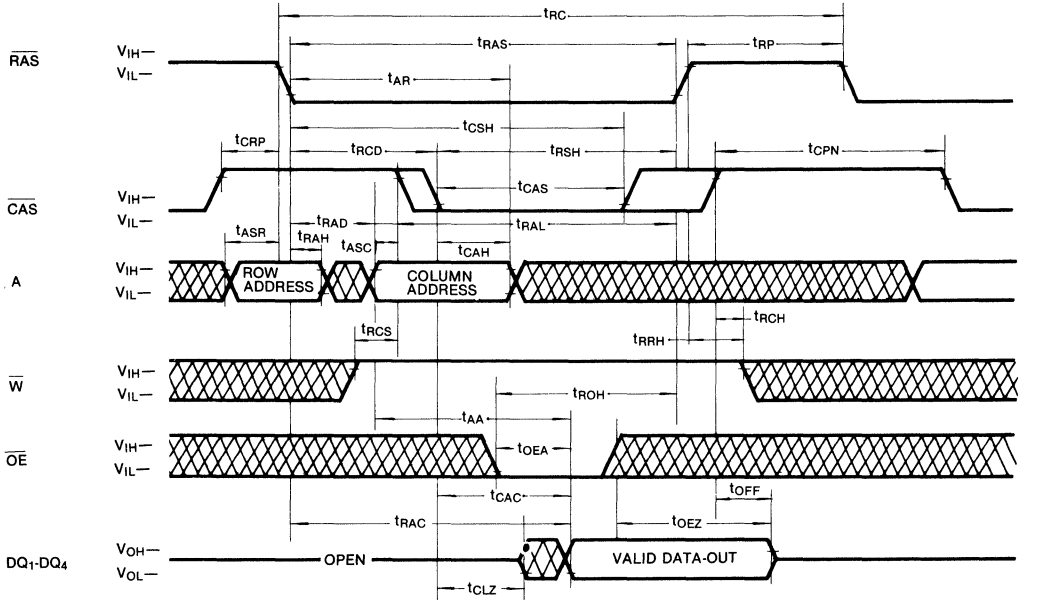
NOTES (Continued)

5. Assumes that $t_{RCD} \geq t_{RCD}(max)$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}(min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(min)$, $t_{RWD} \geq t_{RWD}(min)$ and $t_{AWD} \geq t_{AWD}(min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the $t_{RAD}(max)$ limit insures that $t_{RCD}(max)$ can be met. $t_{RAD}(max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled by t_{AA}.

2

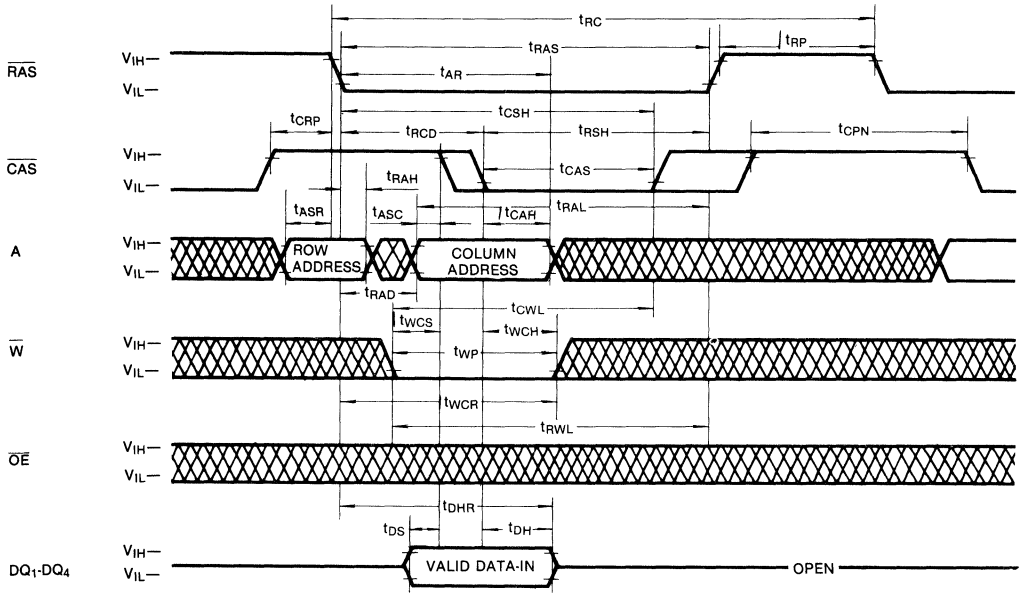
TIMING DIAGRAMS

READ CYCLE

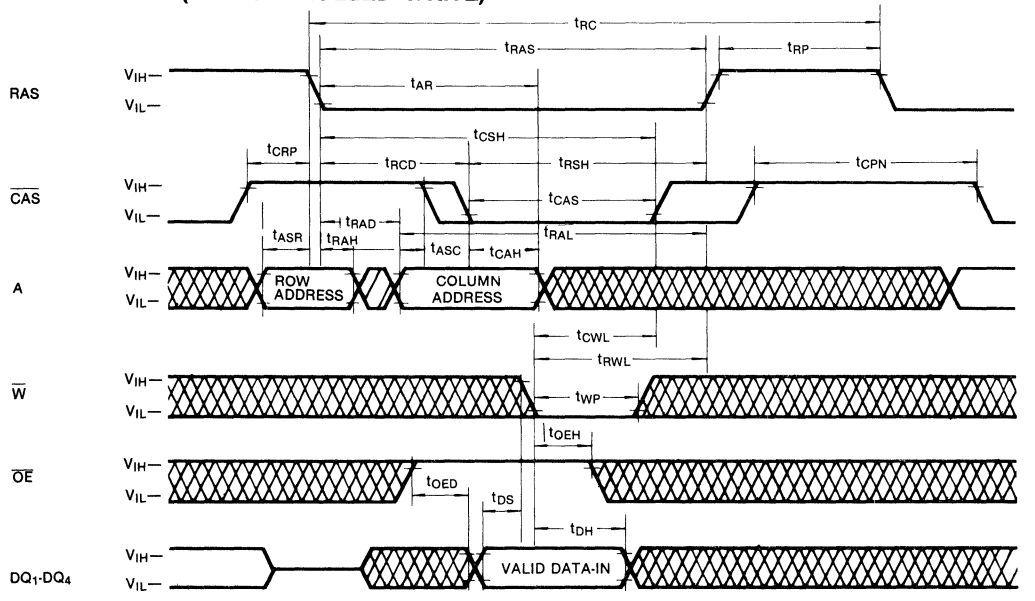


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



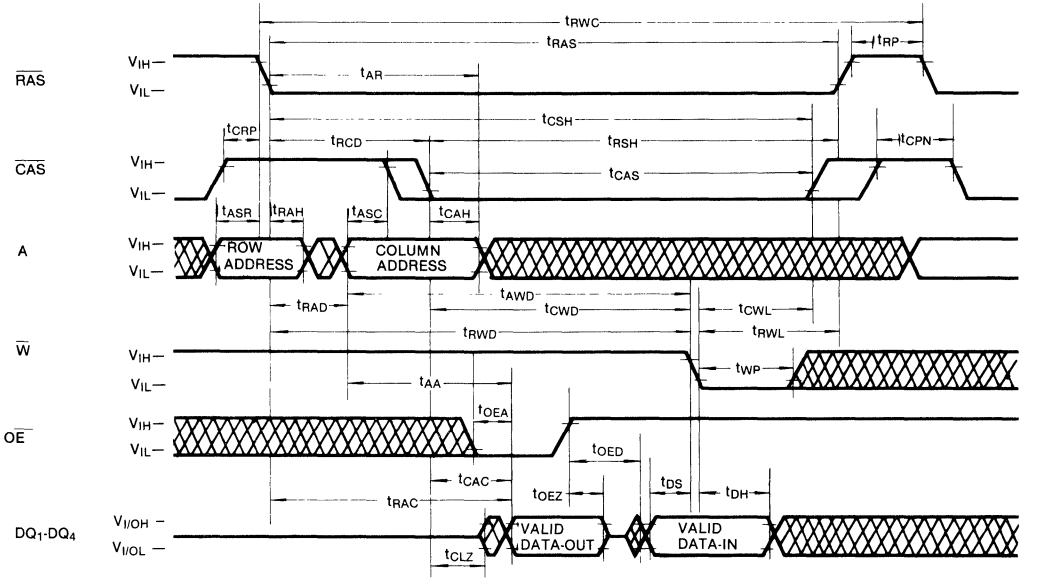
WRITE CYCLE (OE CONTROLLED WRITE)



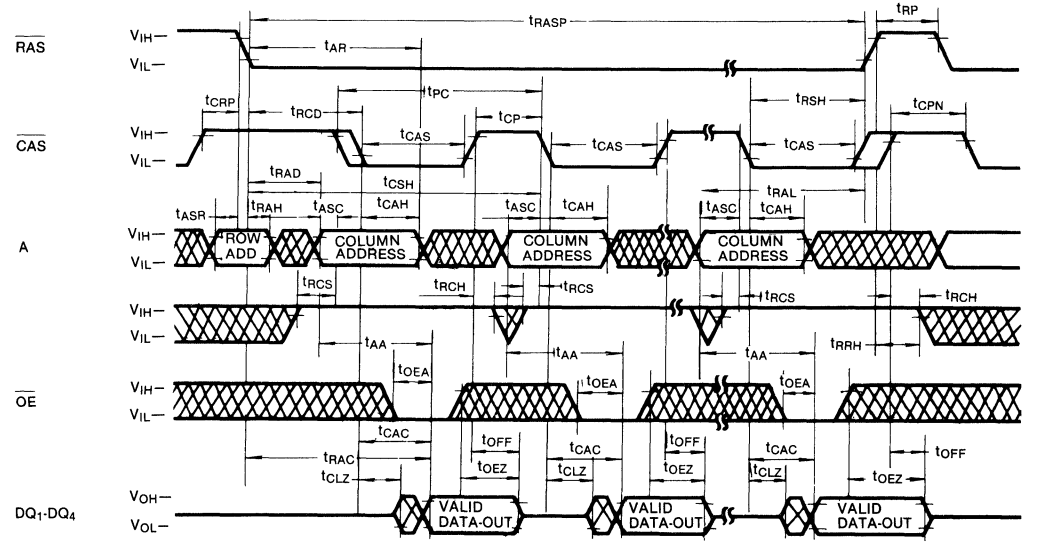
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE



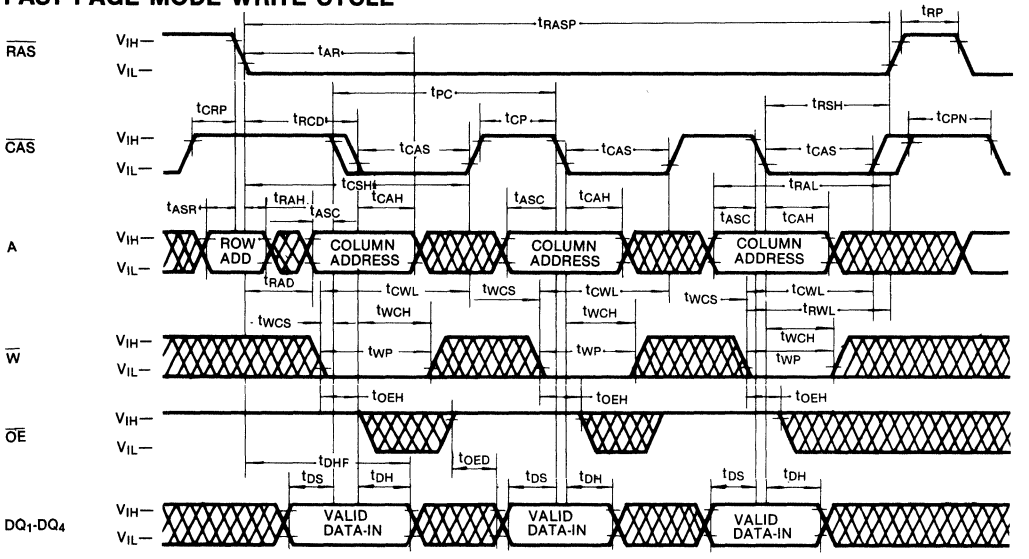
FAST PAGE MODE READ CYCLE



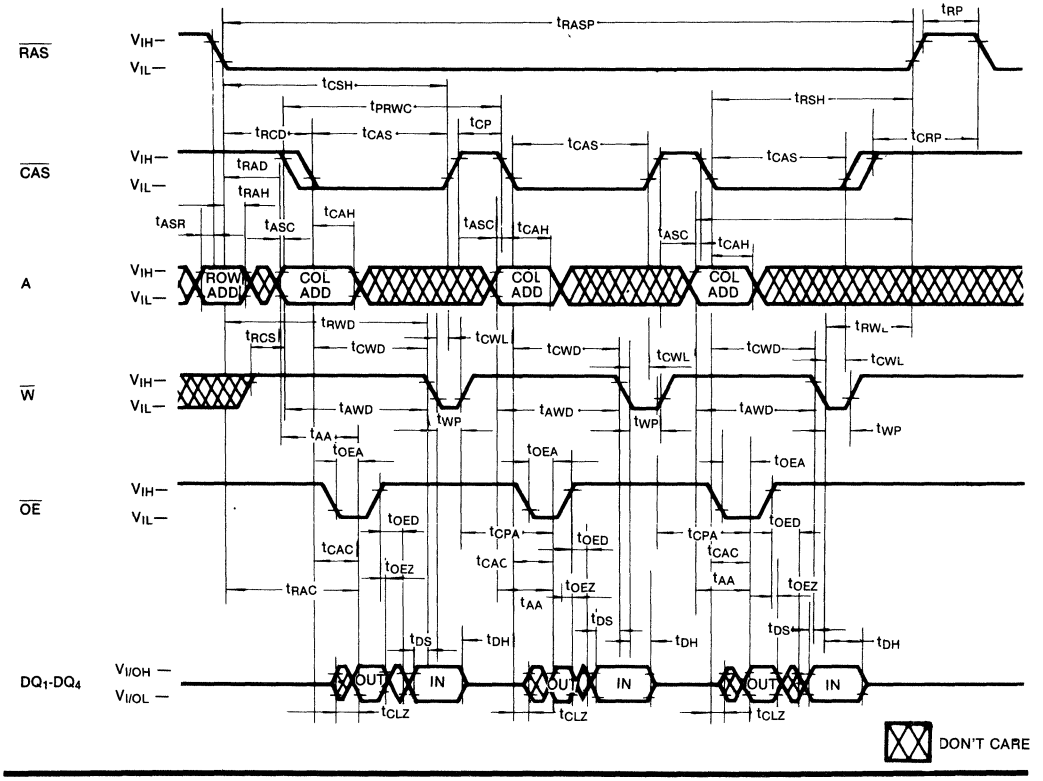
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE



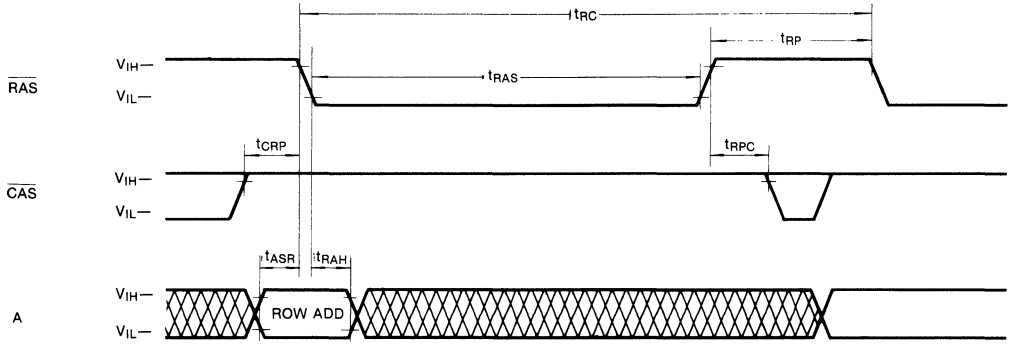
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

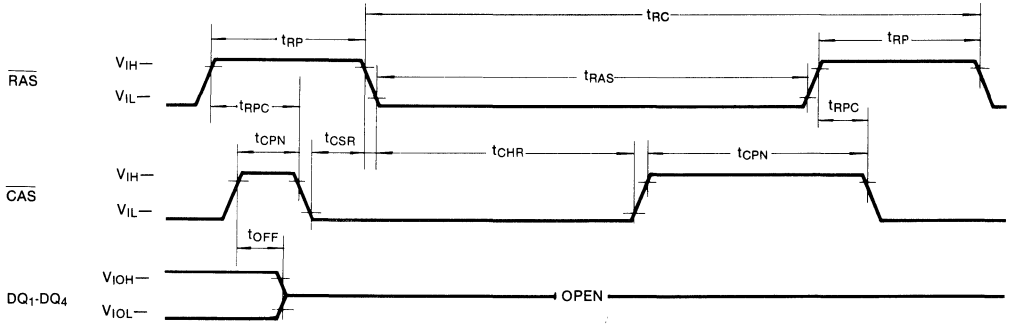
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

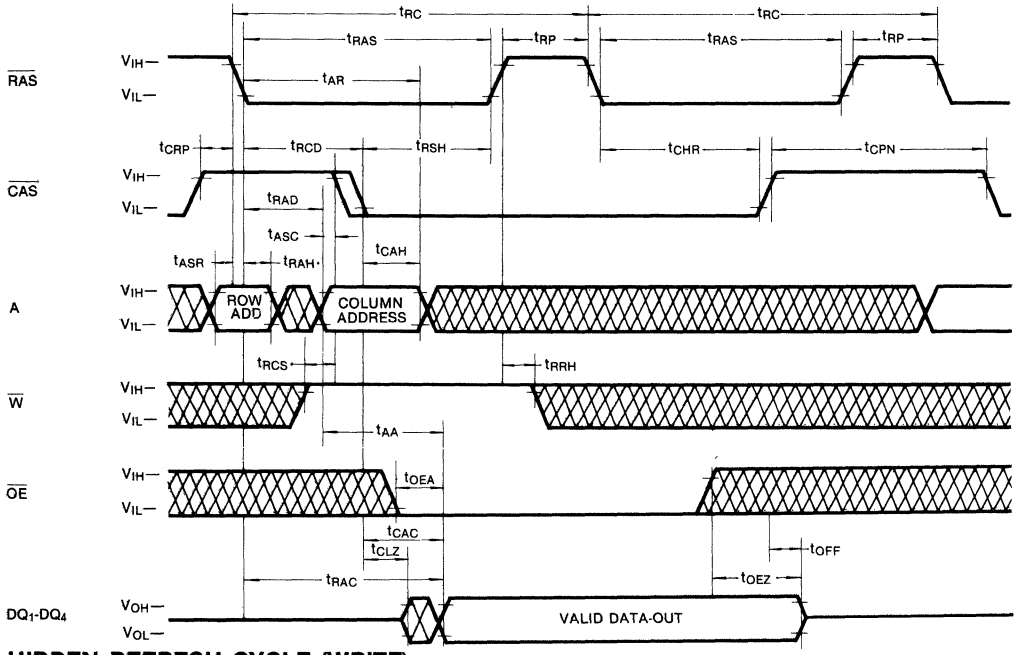
Note: $\overline{W}$, $\overline{OE}$, A = Don't care



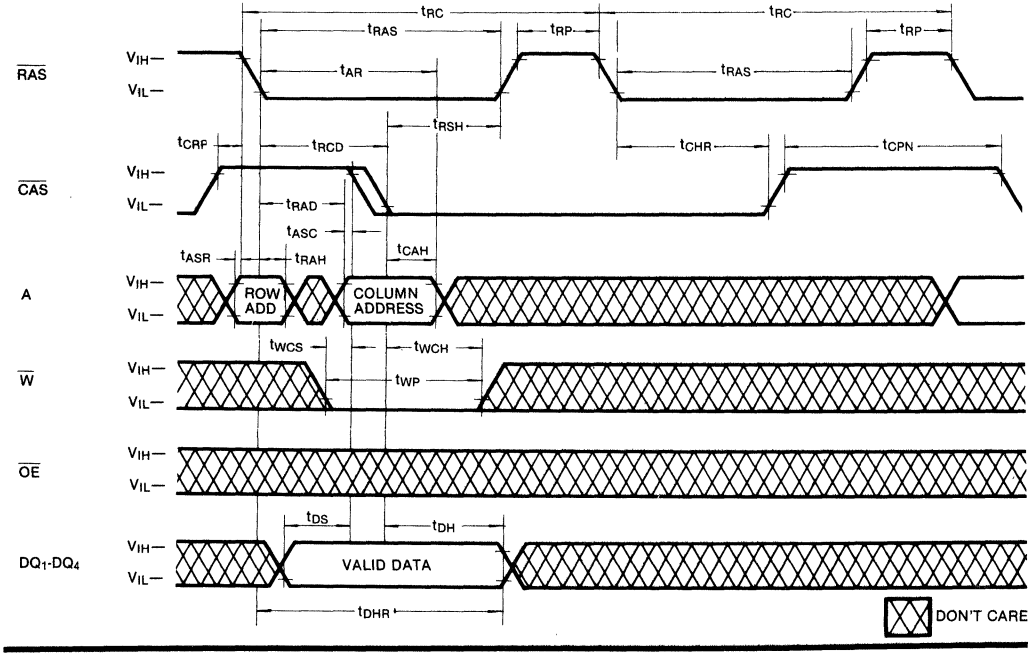
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

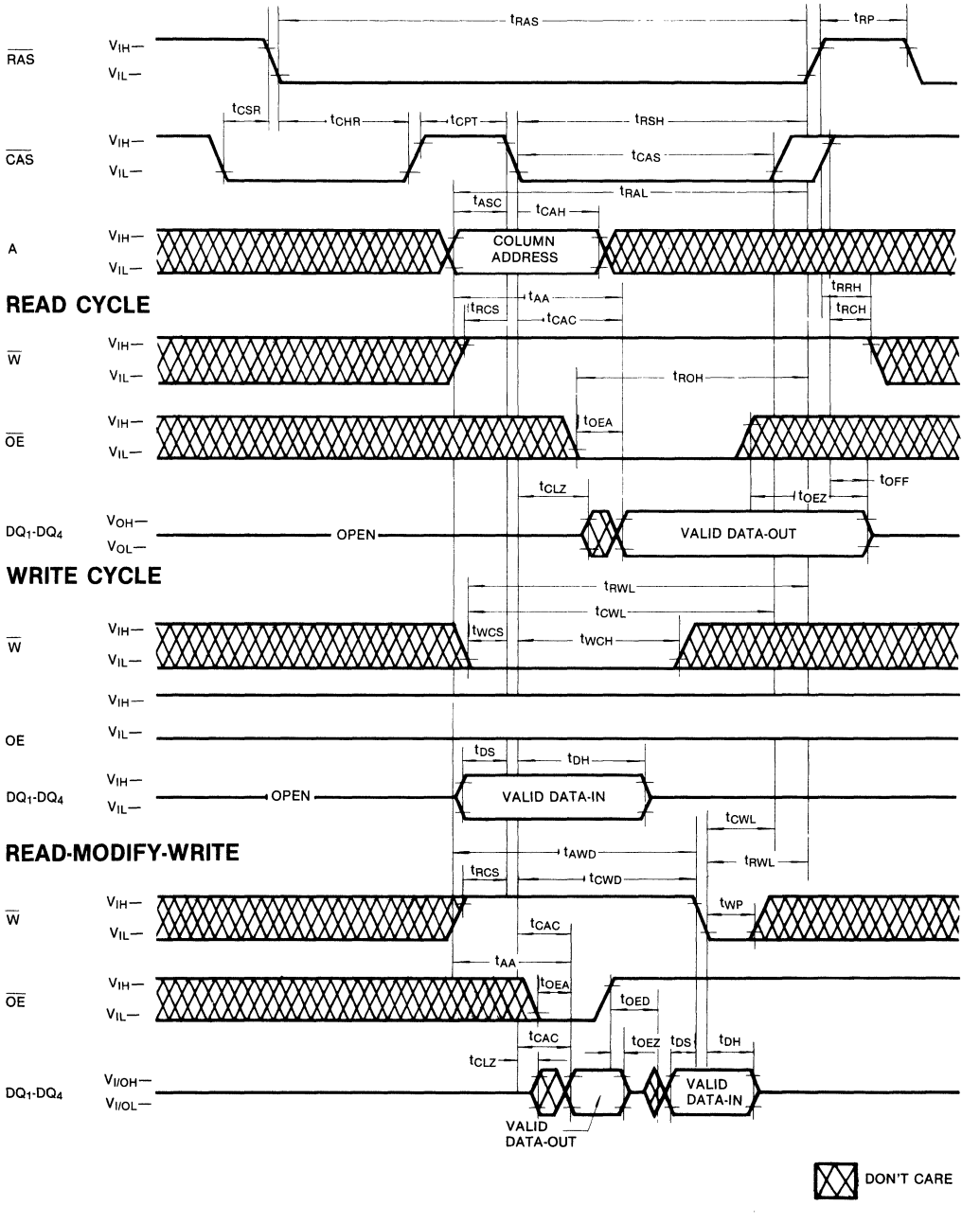


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



KM44C256 OPERATION

Device Operation

The KM44C256 contains 1,048,576 memory locations organized as 262,144 four-bit words. Eighteen address bits are required to address a particular 4-bit word in the memory array. Since the KM44C256 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the KM44C256 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C256 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (tRP) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by tRAS(min) and tCAS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C256 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before tRCD(max) and if the column address is valid before tRAD(max) then the access time to valid data is specified by tRAC(min). However, if $\overline{CAS}$ goes low after tRCD(max) or if the column address becomes valid after tRAD(max), access is specified by tCAC or tAA. In order to achieve the minimum access time, tRAC(min), it is necessary to meet both tRCD(max) and tRAD(max).

The KM44C256 has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by tOEA and tOEZ.

Write

The KM44C256 can perform early write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between W, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the outputs remain in the Hi-Z state. In the early write cycle the output buffers remain in he Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the outputs before and during the time that data is being written into the same cell locations. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. This output enable input ($\overline{OE}$) must be low during the time defined by tOEA and tOEZ for data to appear at the outputs. If tCWD and tRWD are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C256's DQ pins.

Data Output

The KM44C256 has a tri-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. When either $\overline{CAS}$ or $\overline{OE}$ is high (VIH) the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by tCLZ after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after tCLZ and before the valid data appears at the output. The timing parameters tCAC, tRAC and tAA specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C256 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (tCWD or tRWD are not met)

DEVICE OPERATION (Continued)

Refresh

The data in the KM44C256 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This

cycle must be repeated for each of the 512 row addresses, (A0-A8).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C256 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (tCSR) before RAS goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C256 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C256 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-RAS refresh is the preferred method.

CAS-before-RAS Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM44C256 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C256 inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C256 input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

DEVICE OPERATION (Continued)

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the VCC to VSS voltage (measured at the device pins) should not exceed 500mV.

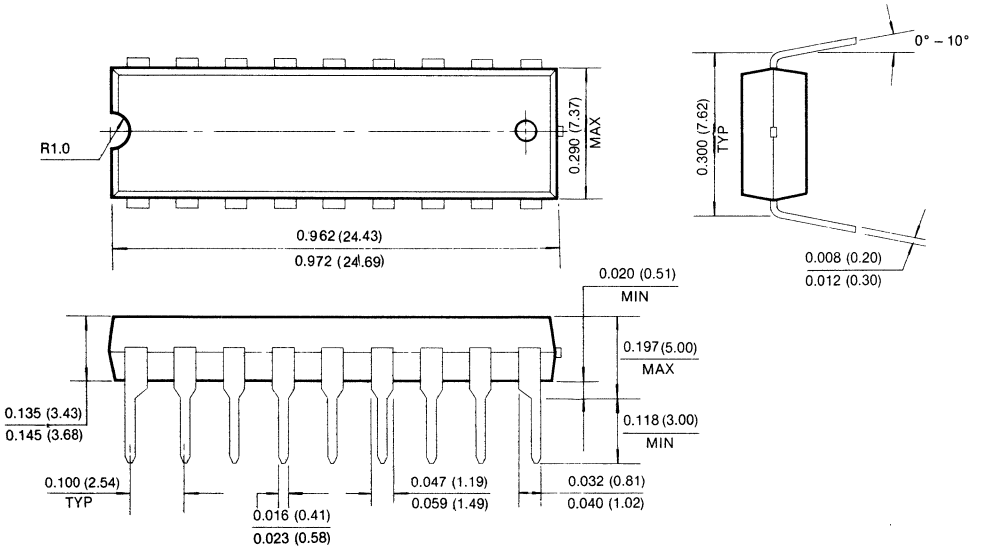
A high frequency 0.3μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C256 using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C256 and they supply much of the current used by the KM44C256 during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.3μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

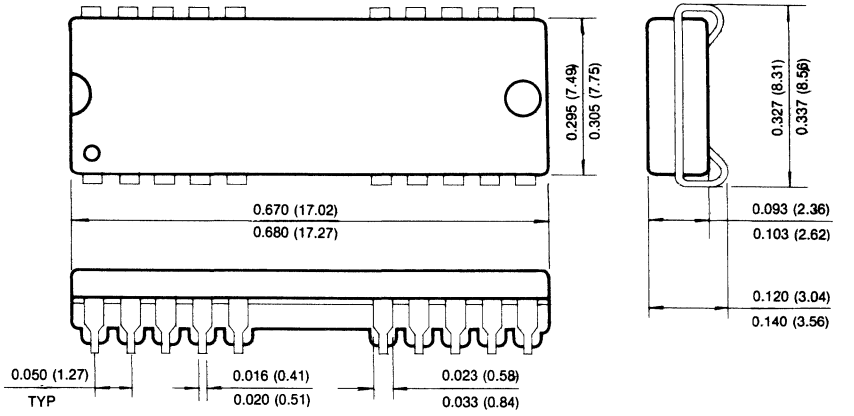
Units: Inches (millimeters)



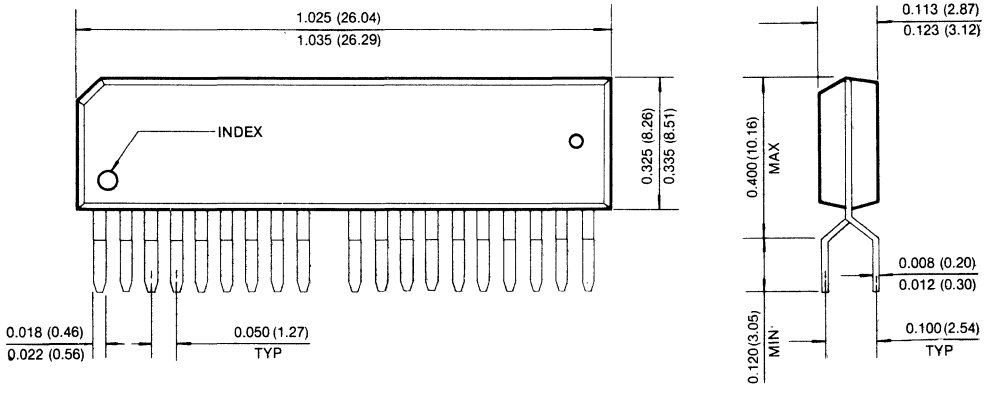
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

units: inches (millimeters)



20-PIN PLASTIC ZIGZAG-IN-LINE PACKAGE



256K x 4 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C258-10	100ns	25ns	190ns
KM44C258-12	120ns	35ns	220ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh**
- **$\overline{RAS}$-only and Hidden refresh**
- **TTL compatible inputs and output**
- **Early Write or Output Enable Controlled Write**
- **Single +5V ± 10% power supply**
- **512 cycles/8ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic 20-pin DIP, SOJ and ZIP**

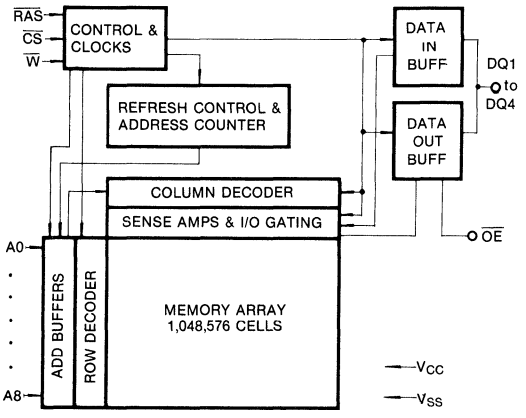
GENERAL DESCRIPTION

The Samsung KM44C258 is a CMOS high speed 262,144 x 4 bit Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C258 features Static Column Mode which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and outputs are fully TTL compatible.

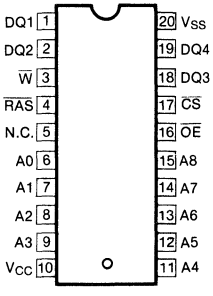
The KM44C258 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

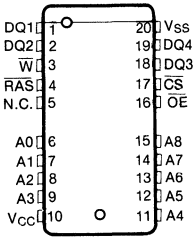


PIN CONFIGURATIONS

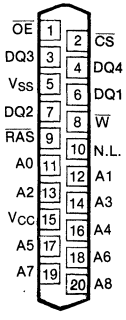
- **KM44C258P**



- **KM44C258J**



- **KM44C258Z**



Pin Name	Pin Function
A_0-A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Column Address Strobe
DQ_1-DQ_4	Data In/Data Out
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection
N.L.	No Lead

256K x 8 Bit DRAM Memory Modules SIP/SIMM

FEATURES

- **262,144 x 8-bit Organization**
- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM48256/7-12	120ns	60ns	230ns
KMM58256/7-12	120ns	60ns	230ns
KMM48256/7-15	150ns	75ns	260ns
KMM58256/7-15	150ns	75ns	260ns

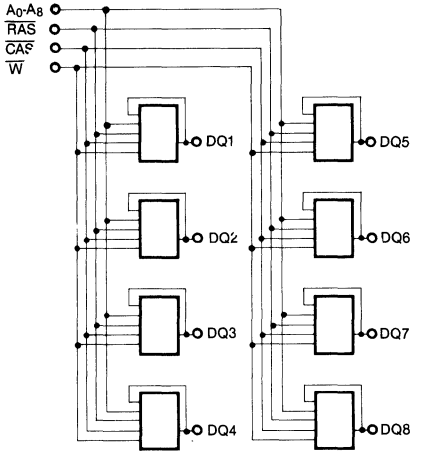
- **Page Mode capability: KMM48256 and KMM58256**
- **Nibble Mode capability: KMM48257 and KMM58257**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V ±10% power supply**
- **256 cycle/4ms refresh**

GENERAL DESCRIPTION

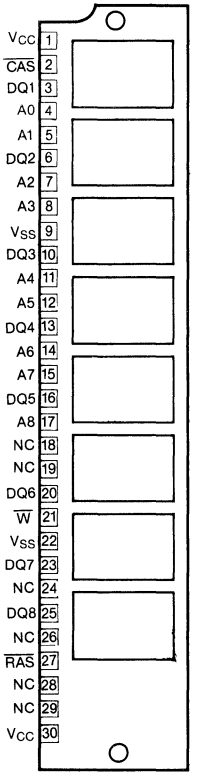
The Samsung KMM48256, KMM48257, KMM58256 and KMM58257 are 256K x 8 dynamic RAM high density memory modules. Samsung's 256K x 8 memory modules consists of eight KM41256/7 DRAMs in 18-pin PLCC packages mounted on a 30 pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each DRAM.

The 256K x 8 DRAM modules are available in two package styles. The KMM48256 and KMM48257 are SIPs with leads suitable for through hole mounting or for mounting in a socket. The KMM58256 and KMM58257 are SIMMs with edge connections and are intended for mounting into 30 pin edge connector sockets.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_8	Address Inputs
DQ	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PART NUMBERS

KMM48256-12	120ns	SIP	Page Mode
KMM48256-15	150ns	SIP	Page Mode
KMM58256-12	120ns	SIMM	Page Mode
KMM58256-15	150ns	SIMM	Page Mode
KMM48257-12	120ns	SIP	Nibble Mode
KMM48257-15	150ns	SIP	Nibble Mode
KMM58257-12	120ns	SIMM	Nibble Mode
KMM58257-15	150ns	SIMM	Nibble Mode

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	$V_{CC}+1$	V
Input Low Voltage	V_{IL}	−1	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling; @t_{RC} = min)	KMM48256/7-12, KMM58256/7-12	I_{CC1}	—	600	mA
	KMM48256/7-15, KMM58256/7-15		—	520	mA
STANDBY CURRENT ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles min)		I_{CC2}	—	36	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; @t_{RC} = min)	KMM48256/7-12, KMM58256/7-12	I_{CC3}	—	520	mA
	KMM48256/7-15, KMM58256/7-15		—	480	mA
PAGE MODE CURRENT* ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; @t_{PC} = min)	KMM48256-12, KMM58256-12	I_{CC4}	—	440	mA
	KMM48256-15, KMM58256-15		—	360	mA
NIBBLE MODE CURRENT* ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; @t_{NC} = min)	KMM48257-12, KMM58257-12	I_{CC5}	—	440	mA
	KMM48257-15, KMM58257-15		—	360	mA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ cycling; @t_{RC} = min)	KMM48256/7-12, KMM58256/7-12	I_{CC6}	—	520	mA
	KMM48256/7-15, KMM58256/7-15		—	480	mA
INPUT LEAKAGE CURRENT (Any input, $0 \le V_{IN} \le 5.5V$, Vcc = 5.5V, V_{SS} = 0V, all other pins not under test = 0 volts.)		I_{IL}	−80	80	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \le V_{OUT} \le 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$)		I_{OL}	−10	10	μA
OUTPUT HIGH VOLTAGE LEVEL ($I_{OH} = -5mA$)		V_{OH}	2.4	—	V
OUTPUT LOW VOLTAGE LEVEL ($I_{OL} = 4.2mA$)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input capacitance ($A_0 - A_9$)	C_A	—	56	pF
Input capacitance ($\overline{RAS}$)	C_{RAS}	—	64	pF
Input capacitance ($\overline{CAS}$)	C_{CAS}	—	64	pF
Input capacitance ($\overline{W}$)	C_W	—	64	pF
Input capacitance ($DQ_1 - DQ_8$)	C_{DQ}	—	17	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1,2.)
STANDARD OPERATION

Parameter	Symbol	KMM48256/7-12 KMM58256/7-12		KMM48256/7-15 KMM58256/7-15		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	230		260		ns	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	3,5
Output buffer turn-off delay time	t_{OFF}	0	30	0	40	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	100		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ precharge time (all cycles except page mode)	t_{CPN}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	
Write command set-up time	t_{WCS}	0		0		ns	
Write command hold time	t_{WCH}	40		45		ns	
Write command pulse width	t_{WP}	40		45		ns	

STANDARD OPERATION (Continued)

Parameter	Symbol	KMM48256/7-12 KMM58256/7-12		KMM48256/7-15 KMM58256/7-15		Units	Notes
		Min	Max	Min	Max		
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in set-up time	t_{DS}	0		0		ns	
Data-in hold time	t_{DH}	40		45		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	100		120		ns	
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	100		120		ns	
Refresh period (256 cycles)	t_{REF}		4		4	ms	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	25		30		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	55		60		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	20		20		ns	

PAGE MODE (KMM48256/KMM58256)

Page mode cycle time	t_{PC}	120		145		ns	
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	50		60		ns	

NIBBLE MODE (KMM48257/KMM58257)

Nibble mode read or write cycle time	t_{NC}	60		75		ns	
Nibble mode access time	t_{NCAC}		30		40	ns	
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	30		40		ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	25		30		ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	40		50		ns	
Nibble mode $\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{RNH}	20		20		ns	
Nibble Mode $\overline{CAS}$ to $\overline{W}$ delay	t_{NCWD}	30		35		ns	
Nibble Mode $\overline{W}$ to $\overline{CAS}$ lead time	t_{NCWL}	25		30		ns	

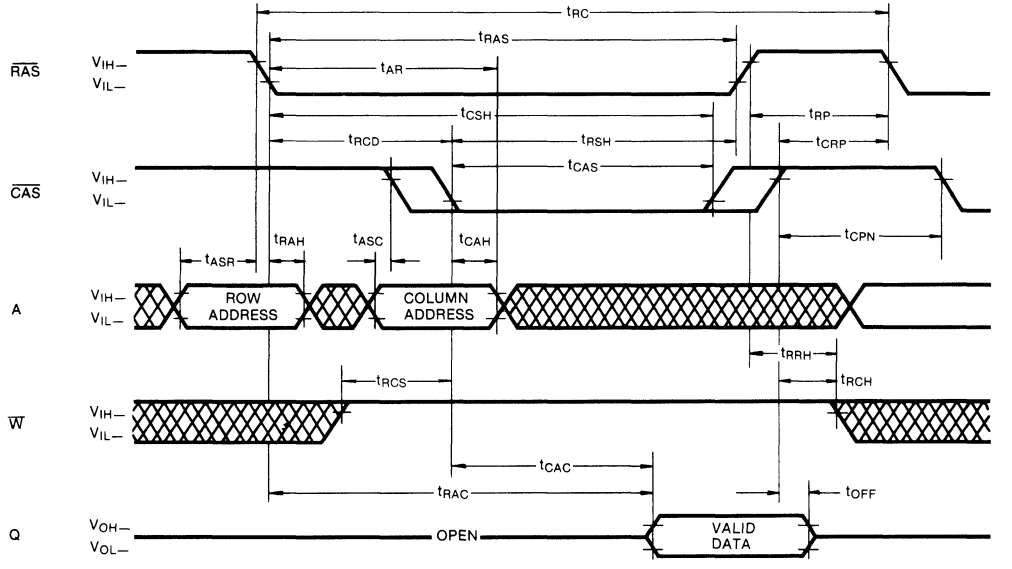
NOTES

1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. Before using the internal refresh counter, 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh initialization cycles are required (instead of 8 $\overline{RAS}$ cycles).
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

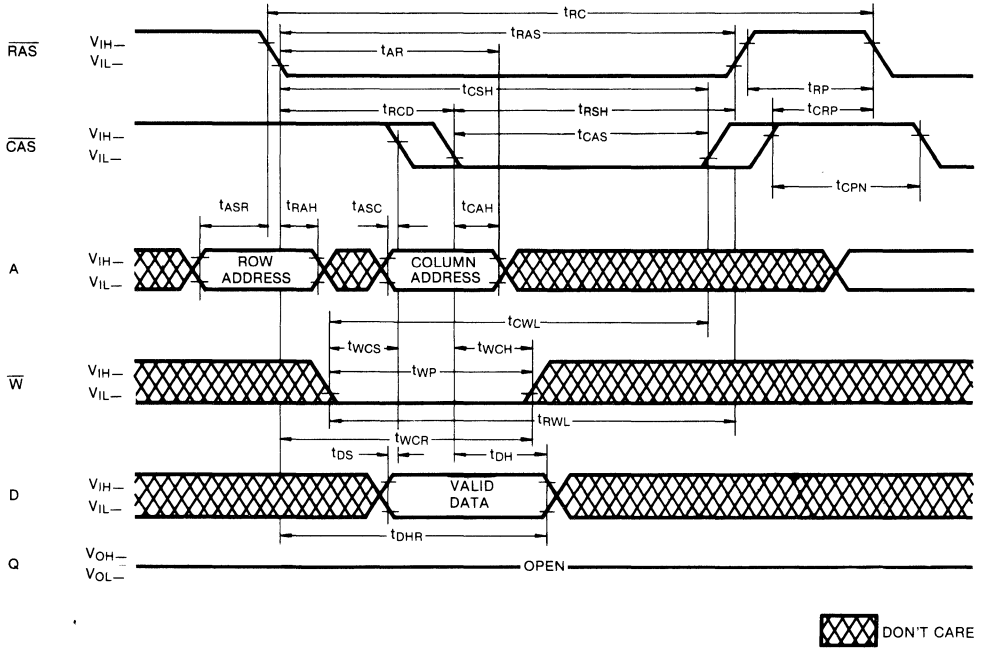
2

TIMING DIAGRAMS

READ CYCLE

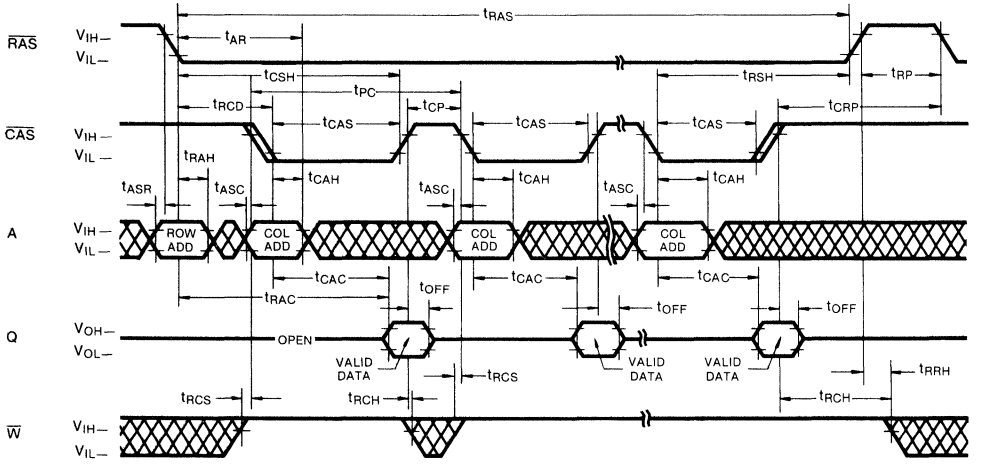


WRITE CYCLE (EARLY WRITE)

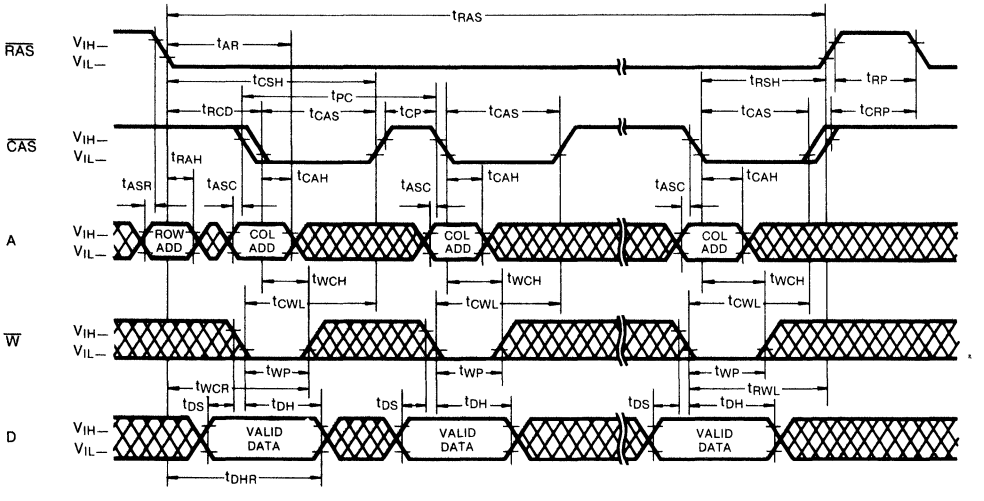


TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE

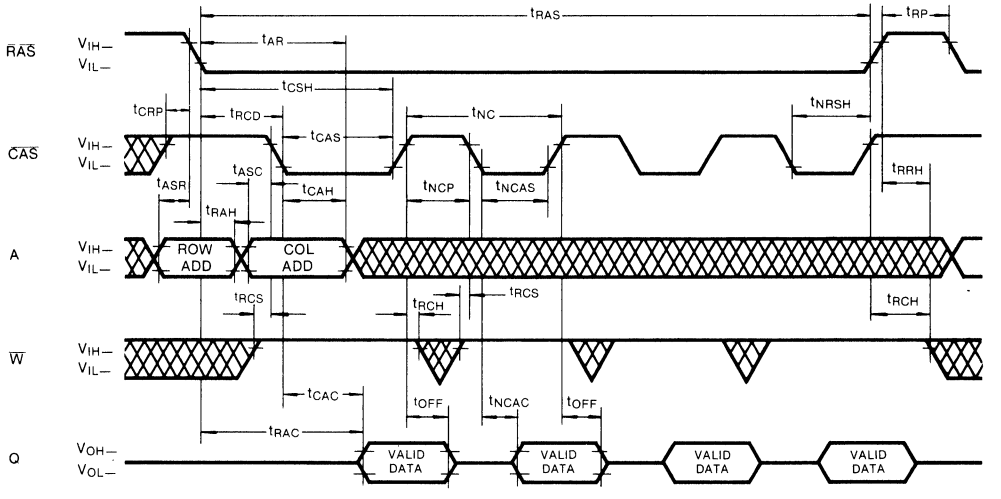


DON'T CARE

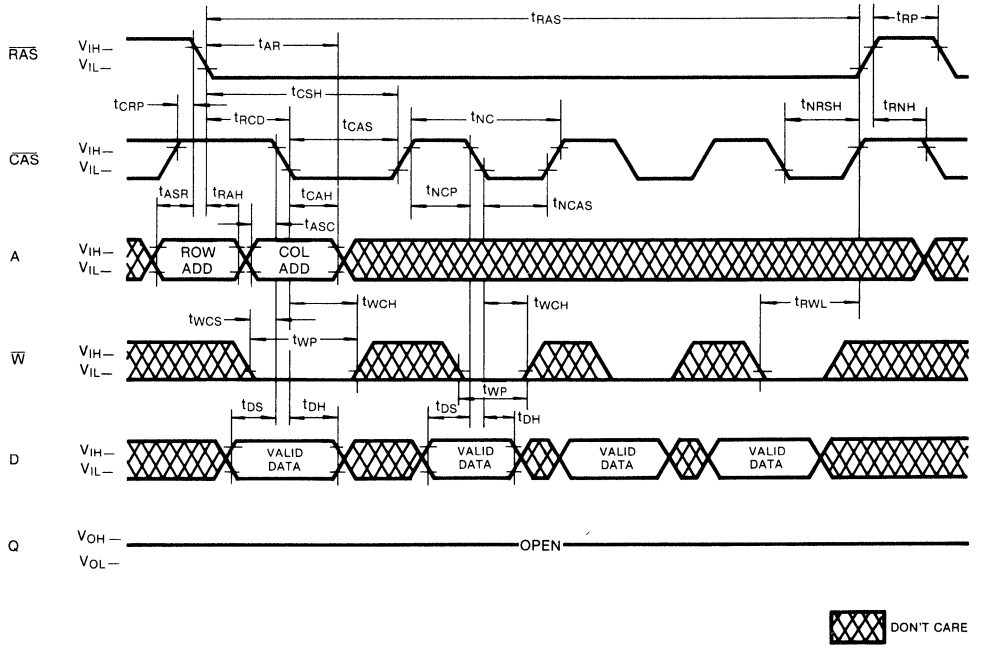
2

TIMING DIAGRAMS (Continued)

NIBBLE MODE READ CYCLE



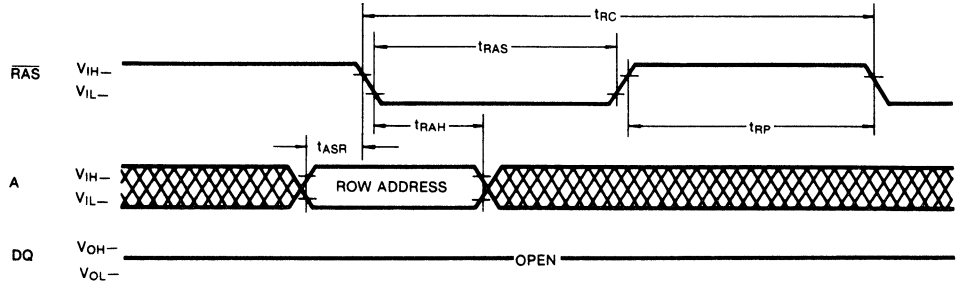
NIBBLE MODE WRITE CYCLE



TIMING DIAGRAMS (Continued)

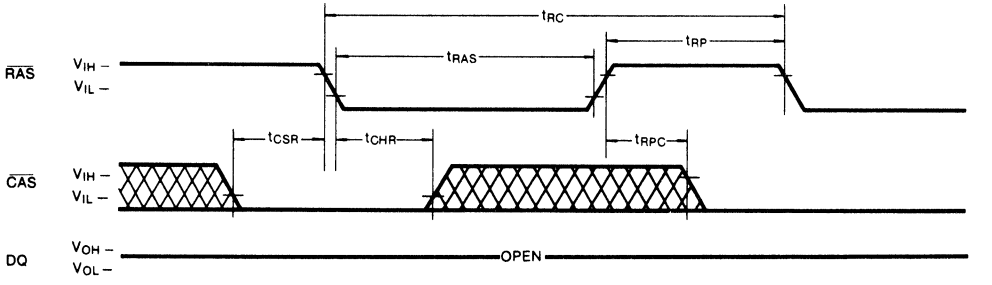
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{W}$ = DON'T CARE, $A_8 = V_{IL}$ or V_{IH}, $\overline{CAS} = V_{IH}$

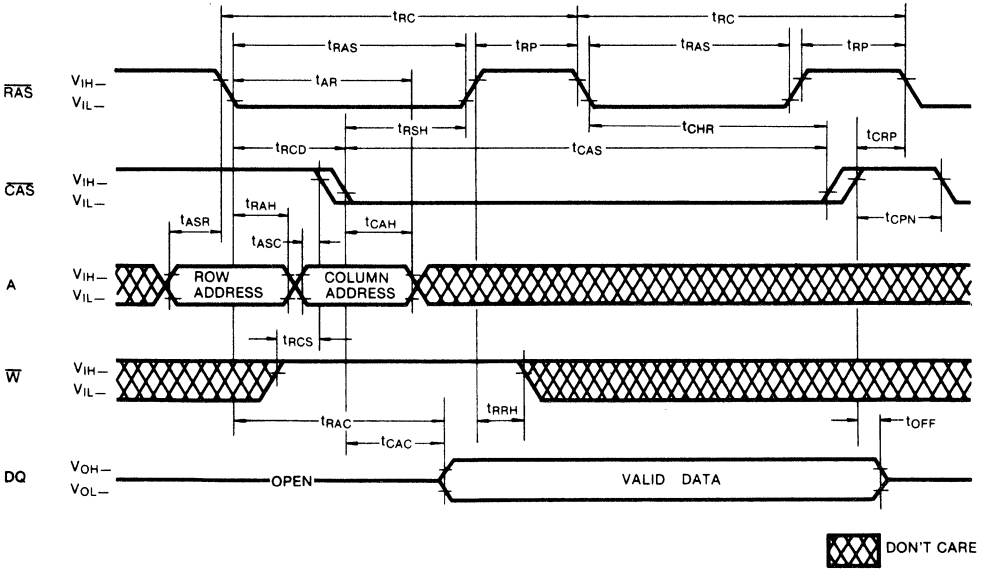


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: ADDRESS, $\overline{W}$ = DON'T CARE



HIDDEN REFRESH CYCLE

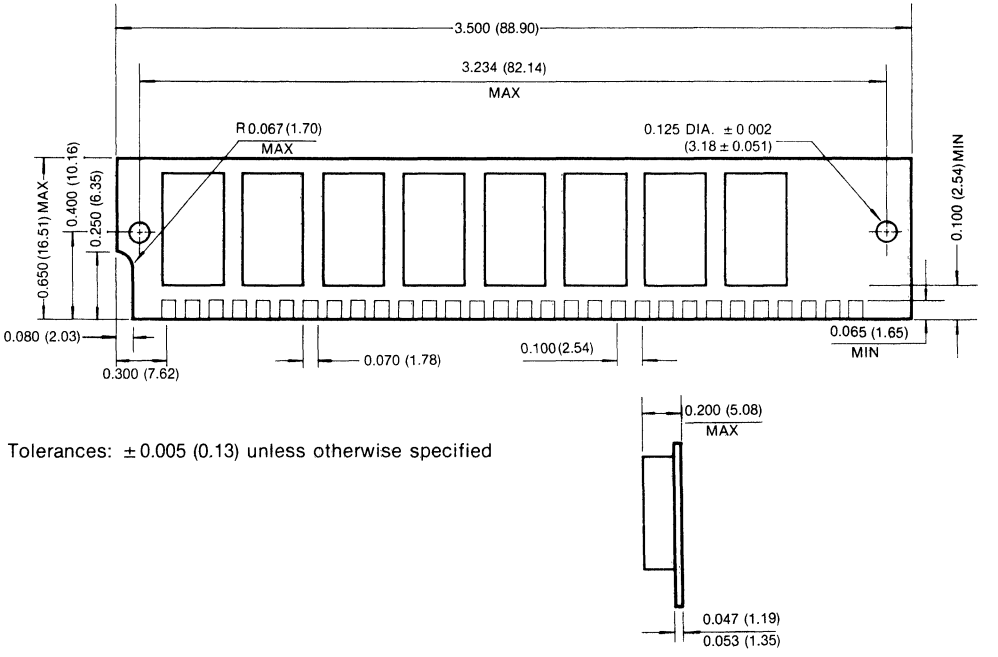


2

PACKAGE DIMENSIONS

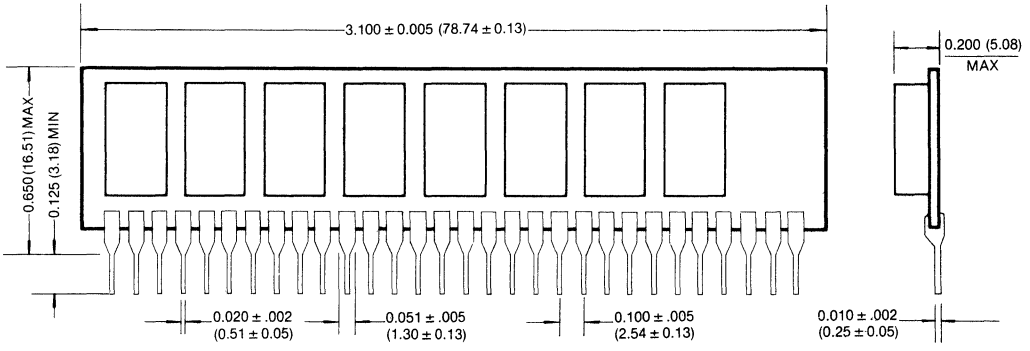
KMM58256 and KMM58257 (256K x 8 SIMM)

Units: Inches (millimeters)



Tolerances: ± 0.005 (0.13) unless otherwise specified

KMM48256 and KMM48257 (256K x 8 SIP)



256K x 9 Bit DRAM Memory Modules SIP/SIMM

FEATURES

- **262,144 x 9-bit Organization**
- **Ninth device has separate D,Q and $\overline{CAS}$ for Parity applications.**
- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM49256/7-12	120ns	60ns	230ns
KMM59256/7-12	120ns	60ns	230ns
KMM49256/7-15	150ns	75ns	260ns
KMM59256/7-15	150ns	75ns	260ns

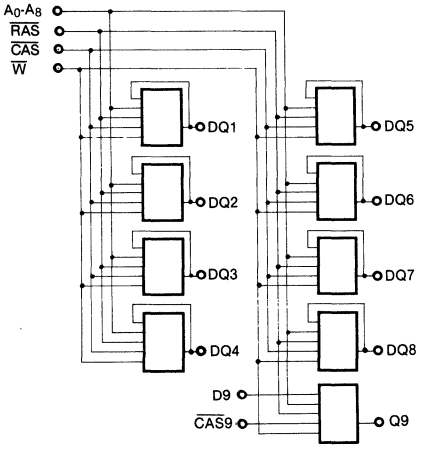
- **Page Mode capability: KMM49256 and KMM59256**
- **Nibble Mode capability: KMM49257 and KMM59257**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V ±10% power supply**
- **256 cycle/4ms refresh**

GENERAL DESCRIPTION

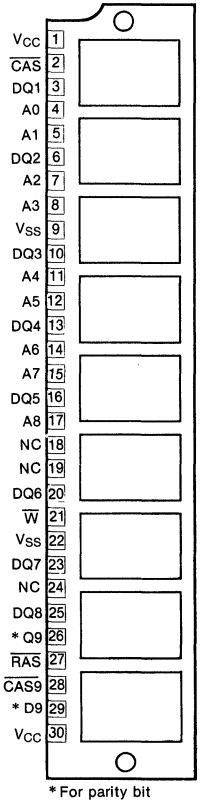
The Samsung KMM49256, KMM49257, KMM59256 and KMM59257 are 256K x 9 dynamic RAM high density memory modules. The ninth bit is generally used for parity and is controlled by $\overline{CAS}_9$. Samsung's 256K x 9 memory modules consists of nine KM41256/7 DRAMs in 18-pin PLCC packages mounted on a 30 pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each DRAM.

The 256K x 9 DRAM modules are available in two package styles. The KMM49256 and KMM49257 are SIPs with leads suitable for through hole mounting or for mounting in a socket. The KMM59256 and KMM59257 are SIMMs with edge connections and are intended for mounting into 30 pin edge connector sockets.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



*For parity bit

Pin Name	Pin Function
A_0-A_8	Address Inputs
D_9	Data In
Q_9	Data Out
DQ	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{CAS}_9$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PART NUMBERS

KMM49256-12	120ns	SIP	Page Mode
KMM49256-15	150ns	SIP	Page Mode
KMM59256-12	120ns	SIMM	Page Mode
KMM59256-15	150ns	SIMM	Page Mode
KMM49257-12	120ns	SIP	Nibble Mode
KMM49257-15	150ns	SIP	Nibble Mode
KMM59257-12	120ns	SIMM	Nibble Mode
KMM59257-15	150ns	SIMM	Nibble Mode

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	9	W
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	−1	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling; @t_{RC} = min)	KMM49256/7-12, KMM59256/7-12	I_{CC1}	—	675	mA
	KMM49256/7-15, KMM59256/7-15		—	585	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min)		I_{CC2}	—	41	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; @t_{RC} = min)	KMM49256/7-12, KMM59256/7-12	I_{CC3}	—	585	mA
	KMM49256/7-15, KMM59256/7-15		—	540	mA
PAGE MODE CURRENT* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; @t_{PC} = min)	KMM49256-12, KMM59256-12	I_{CC4}	—	495	mA
	KMM49256-15, KMM59256-15		—	405	mA
NIBBLE MODE CURRENT* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; @t_{NC} = min)	KMM49257-12, KMM59257-12	I_{CC5}	—	495	mA
	KMM49257-15, KMM59257-15		—	405	mA
$\overline{CAS}$-BEFORE $\overline{RAS}$-REFRESH CURRENT* ($\overline{RAS}$ cycling; @t_{RC} = min)	KMM49256/7-12, KMM59256/7-12	I_{CC6}	—	585	mA
	KMM49256/7-15, KMM59256/7-15		—	540	mA
INPUT LEAKAGE CURRENT (D_9, $\overline{CAS_9}$ input, 0≤V_{IN}≤5.5V, Vcc = 5.5V, Vss = 0V, all other pins not under test = 0 volts.)		I_{IL1}	−10	10	μA
INPUT LEAKAGE CURRENT (A, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$ inputs, 0≤V_{IN}≤5.5V, Vcc = 5.5V, Vss = 0V, all other pins not under test = 0 volts.)		I_{IL2}	−90	90	μA
OUTPUT LEAKAGE CURRENT (DQ, Q_9, Data out is disabled, 0V≤V_{OUT}≤5.5V, Vcc = 5.5V, Vss = 0V,)		I_{OL}	−10	10	μA
OUTPUT HIGH VOLTAGE LEVEL (I_{OH} = −5mA)		V_{OH}	2.4	—	V
OUTPUT LOW VOLTAGE LEVEL (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input capacitance ($A_0 - A_8$)	C_A	—	63	pF
Input capacitance ($\overline{RAS}$)	C_{RAS}	—	72	pF
Input capacitance ($\overline{CAS}$)	C_{CAS}	—	64	pF
Input capacitance ($\overline{W}$)	C_W	—	72	pF
Input capacitance ($\overline{CAS_9}$)	C_{CAS9}	—	10	pF
Input capacitance (D_9)	C_{D9}	—	7	pF
Input capacitance (DQ_1-DQ_8)	C_{DQ}	—	17	pF
Output capacitance (Q_9)	C_{Q9}	—	10	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1,2.)
STANDARD OPERATION

Parameter	Symbol	KMM49256/7-12 KMM59256/7-12		KMM49256/7-15 KMM59256/7-15		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	230		260		ns	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	3,5
Output buffer turn-off delay time	t_{OFF}	0	30	0	40	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	100		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ precharge time (all cycles except page mode)	t_{CPN}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	

STANDARD OPERATION (Continued)

Parameter	Symbol	KMM49256/7-12 KMM59256/7-12		KMM49256/7-15 KMM59256/7-15		Units	Notes
		Min	Max	Min	Max		
Write command set-up time	t_{WCS}	0		0		ns	
Write command hold time	t_{WCH}	40		45		ns	
Write command pulse width	t_{WP}	40		45		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in set-up time	t_{DS}	0		0		ns	
Data-in hold time	t_{DH}	40		45		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	100		120		ns	
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	100		120		ns	
Refresh period (256 cycles)	t_{REF}		4		4	ms	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	25		30		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	55		60		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	20		20		ns	

PAGE MODE (KMM49256/KMM59256)

Page mode cycle time	t_{PC}	120		145		ns	
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	50		60		ns	

NIBBLE MODE (KMM49257/KMM59257)

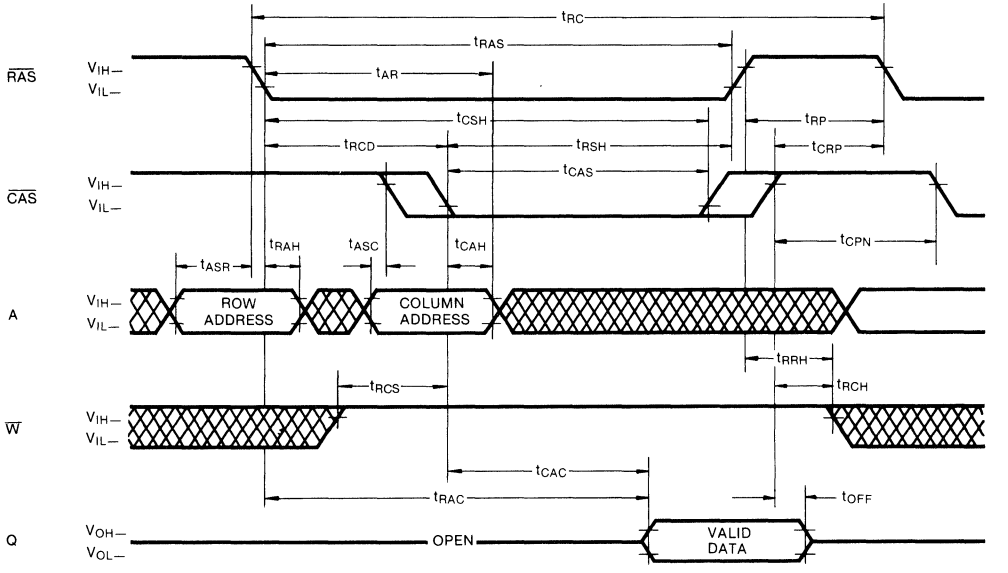
Nibble mode read or write cycle time	t_{NC}	60		75		ns	
Nibble mode access time	t_{NCAC}		30		40	ns	
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	30		40		ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	25		30		ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	40		50		ns	
Nibble mode $\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{RNH}	20		20		ns	
Nibble mode $\overline{CAS}$ to $\overline{W}$ delay time	t_{NCWD}	30		35		ns	
Nibble mode $\overline{W}$ to $\overline{CAS}$ lead time	t_{NCWL}	25		30		ns	

NOTES

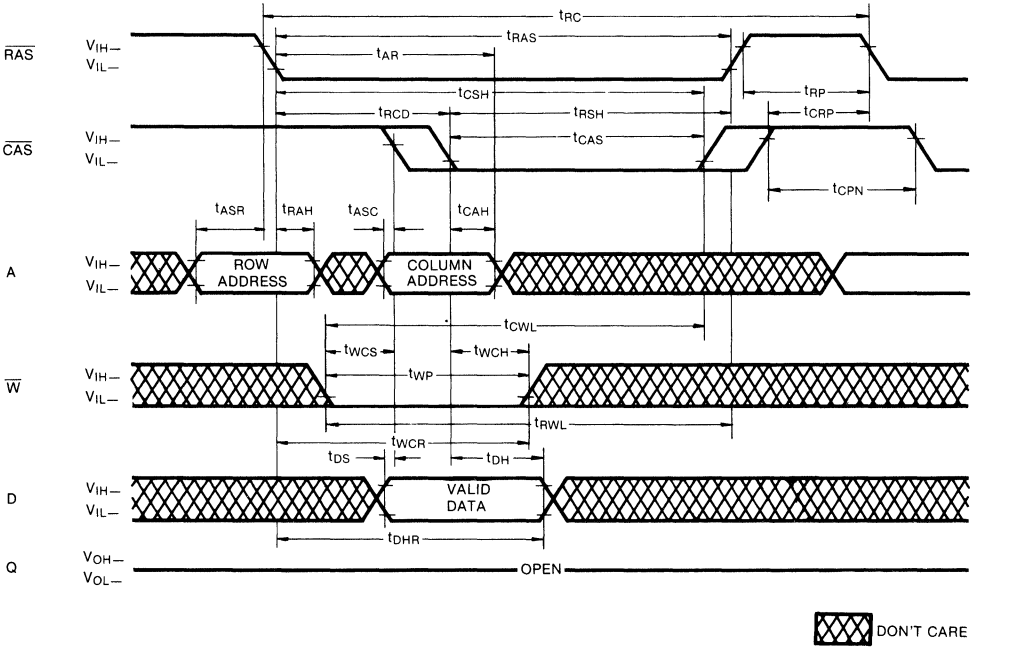
1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. Before using the internal refresh counter, 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh initialization cycles are required (instead of 8 $\overline{RAS}$ cycles).
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

TIMING DIAGRAMS

READ CYCLE

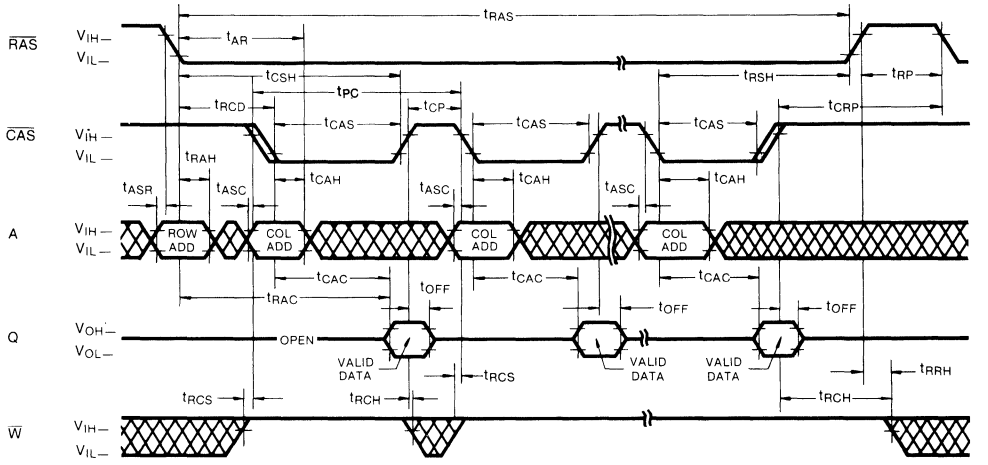


WRITE CYCLE (EARLY WRITE)

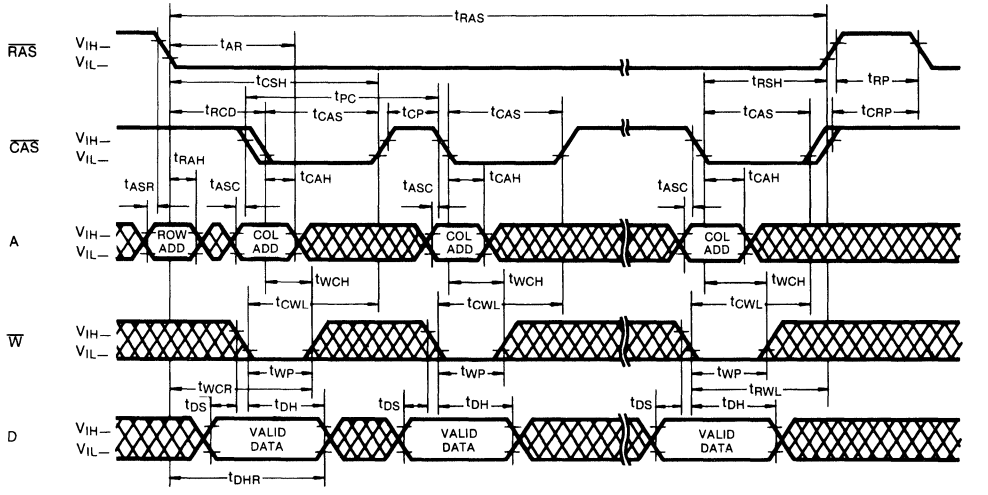


TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE



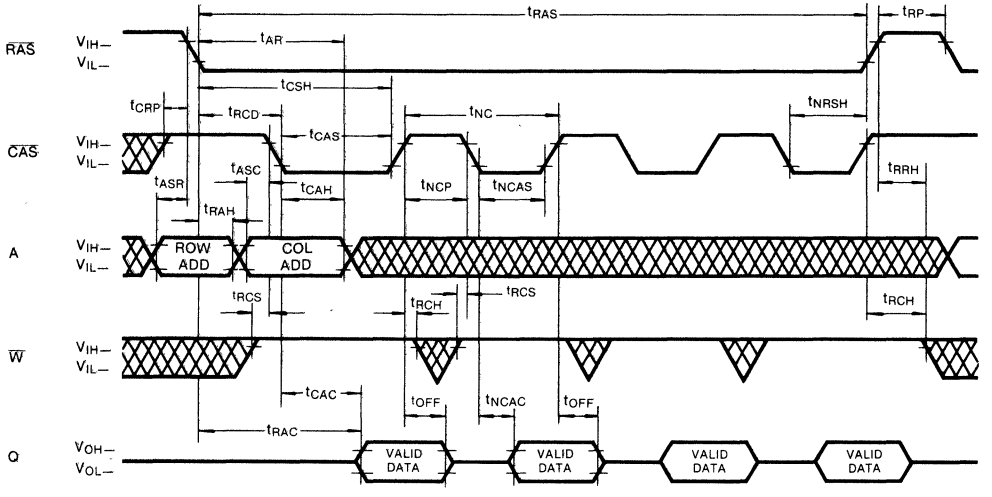
PAGE MODE WRITE CYCLE



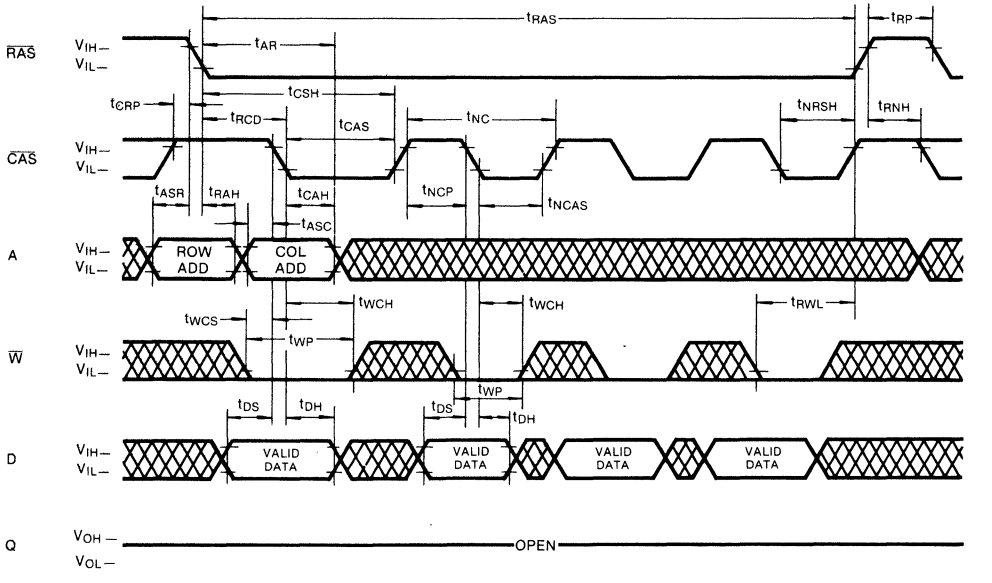
DON'T CARE

TIMING DIAGRAMS (Continued)

NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE



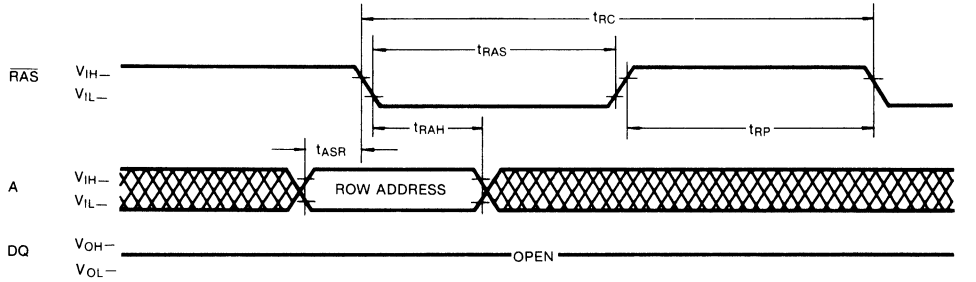
DON'T CARE

2

TIMING DIAGRAMS (Continued)

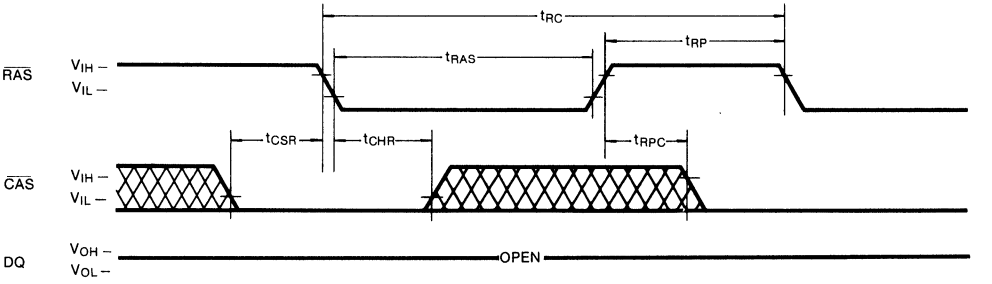
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{W}$ = DON'T CARE, $A_8 = V_{IL}$ or V_{IH}, $\overline{CAS} = V_{IH}$

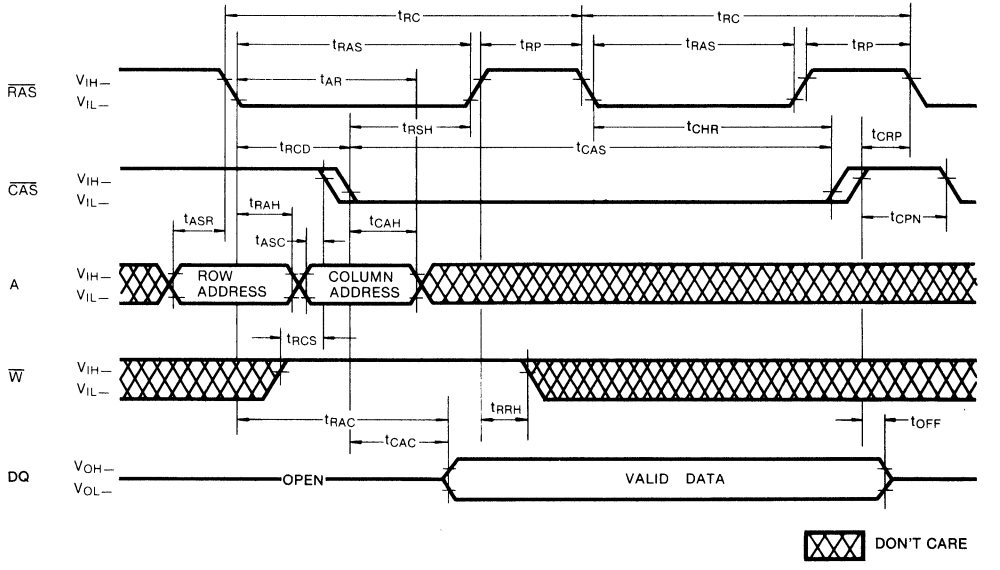


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: ADDRESS, $\overline{W}$ = DON'T CARE



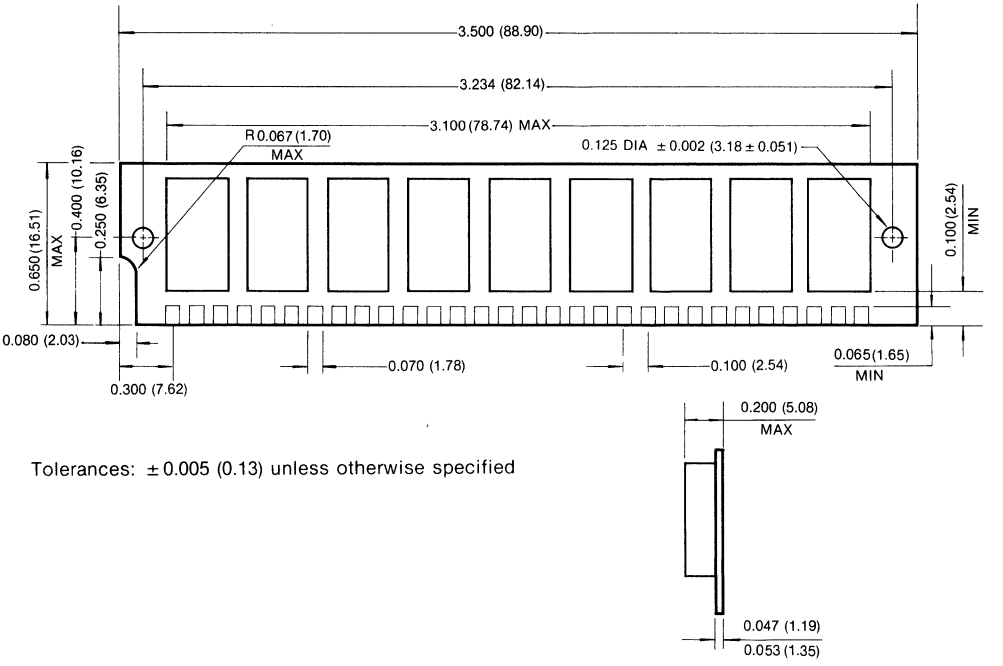
HIDDEN REFRESH CYCLE



PACKAGE DIMENSIONS

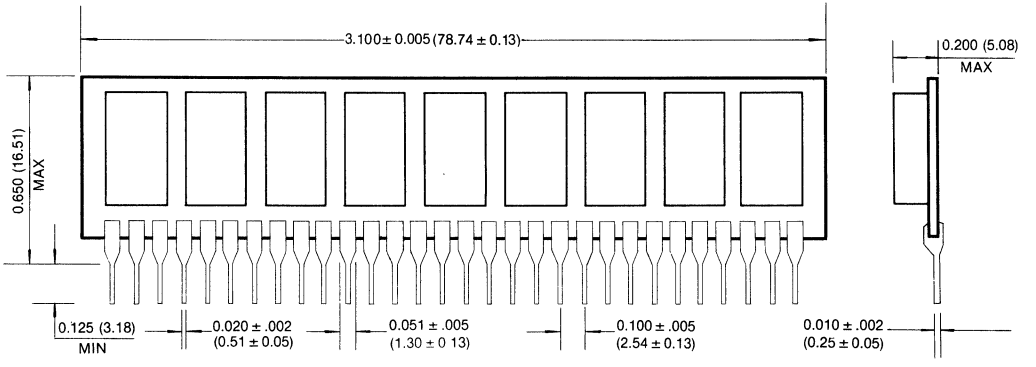
KMM59256 and KMM59257 (256K x 9 SIMM)

Units: Inches (millimeters)



Tolerances: ± 0.005 (0.13) unless otherwise specified

KMM49256 and KMM49257 (256K x 9 SIP)



1M x 8 DRAM SIP and SIMM Memory Modules

FEATURES

- **1,048,576 x 8-bit Organization**
- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM481000-10	100ns	25ns	190ns
KMM581000-10	100ns	25ns	190ns
KMM481000-12	120ns	30ns	220ns
KMM581000-12	120ns	30ns	220ns

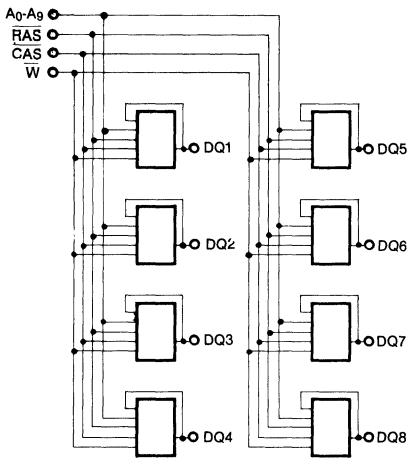
- **Fast Page Mode capability**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V ± 10% power supply**
- **512 cycles/8ms refresh**
- **JEDEC standard pinout**

GENERAL DESCRIPTION

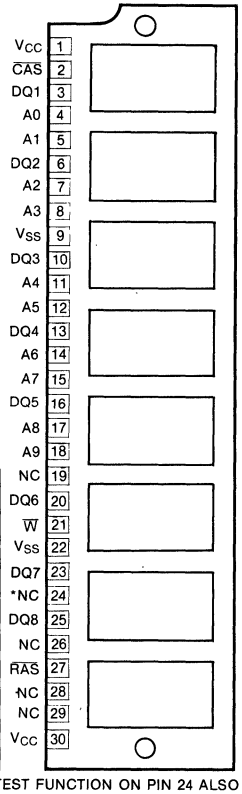
The Samsung KMM481000 and KMM581000 are 1M x 8 dynamic RAM high density memory modules. Samsung 1M x 8 memory modules consist of eight KM41C1000 DRAMS in 20-pin SOJ packages mounted on a 30 pin glass-epoxy substrate. A 0.22μF decouping capacitor is mounted under each DRAM.

The 1M x 8 DRAM modules are available in two package styles. The KMM481000 is SIP with leads suitable for through hole mounting or for mounting in a socket. The KMM581000 is SIMM with edge connections and is intended for mounting into 30 pin edge connector socket.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



*TEST FUNCTION ON PIN 24 ALSO WILL BE AVAILABLE BY OPTION

Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PART NUMBERS

KMM481000-10	100ns	SIP	Page Mode
KMM481000-12	120ns	SIP	Page Mode
KMM581000-10	100ns	SIMM	Page Mode
KMM581000-12	120ns	SIMM	Page Mode

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	4.8	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min)	KMM481000-10, KMM581000-10 KMM481000-12, KMM581000-12	I_{CC1}	— —	480 400	mA mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	16	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @t_{RC} = min)	KMM481000-10, KMM581000-10 KMM481000-12, KMM581000-12	I_{CC3}	— —	480 400	mA mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling @t_{PC} = min)	KMM481000-10, KMM581000-10 KMM481000-12, KMM581000-12	I_{CC4}	— —	320 240	mA mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	8	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min)	KMM481000-10, KMM581000-10 KMM481000-12, KMM581000-12	I_{CC6}	— —	480 400	mA mA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0 volts)		I_{IL}	−80	80	μA
Output Leakage Current (Data out is disabled, 0 ≤ V_{OUT} ≤ 5.5V		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	50	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	60	pF
Output Capacitance (DQ_1-DQ_8)	C_{DQ}	—	15	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1, 2)

Parameter	Symbol	KMM4(5)81000-10		KMM4(5)81000-12		Units	Notes
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	190		220		ns	
Access Time from $\overline{RAS}$	t_{RAC}		100		120	ns	3, 4, 10
Access Time from $\overline{CAS}$	t_{CAC}		25		30	ns	3, 4, 5
Access Time from Column Address	t_{AA}		50		60	ns	3, 10
Access Time from CAS Precharge	t_{CPA}		55		65	ns	3
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	5		5		ns	3
Output Buffer Turn-off Delay Time	t_{OFF}	0	30	0	35	ns	6
Transition Time (rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ Precharge Time	t_{RP}	80		90		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10,000	120	10,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	25		30		ns	
$\overline{CAS}$ Precharge time (except fast page)	t_{CPN}	15		20		ns	
CAS Hold Time	t_{CSH}	100		120		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10,000	30	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	75	25	90	ns	4
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	50	20	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		ns	
Row Address Set-up Time	t_{ASR}	0		0		ns	
Row Address Hold Time	t_{RAH}	15		15		ns	
Column Address Set-up Time	t_{ASC}	0		0		ns	
Column Address Hold Time	t_{CAH}	20		25		ns	
Column Address Hold Time Reference to $\overline{RAS}$	t_{AR}	95		115		ns	
Column Address to RAS Lead Time	t_{RAL}	50		60		ns	
Read Command Set-up Time	t_{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read Command Hold Time Reference to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write Command Hold Time	t_{WCH}	20		25		ns	

AC CHARACTERISTICS (Continued)

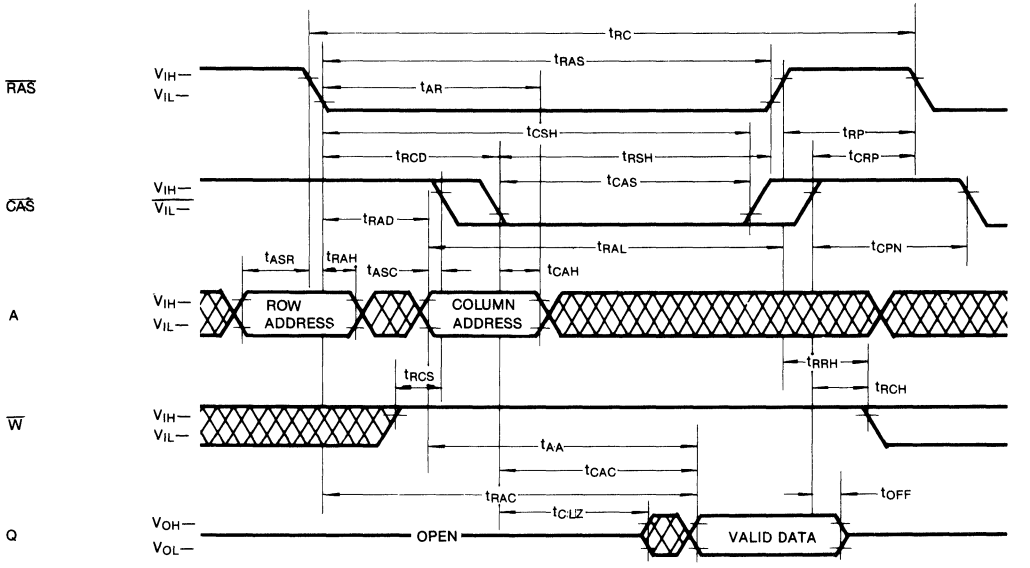
Parameter	Symbol	KMM4(5)81000-10		KMM4(5)81000-12		Units	Notes
		Min	Max	Min	Max		
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	95		115		ns	
Write Command Pulse Width	t_{WP}	20		25		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25		30		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25		30		ns	
Data-in Set-up Time	t_{DS}	0		0		ns	9
Data-in Hold Time	t_{DH}	20		25		ns	9
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	95		115		ns	
Refresh Period (512 cycles)	t_{REF}		8		8	ms	
Write Command Set-up Time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	30		30		ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10		10		ns	
Fast Page Mode Cycle Time	t_{PC}	60		70		ns	
$\overline{CAS}$ Precharge Time (fast page mode)	t_{CP}	10		15		ns	
$\overline{RAS}$ Pulse Width (fast page mode)	t_{RASP}	100	100,000	120	100,000	ns	

NOTES

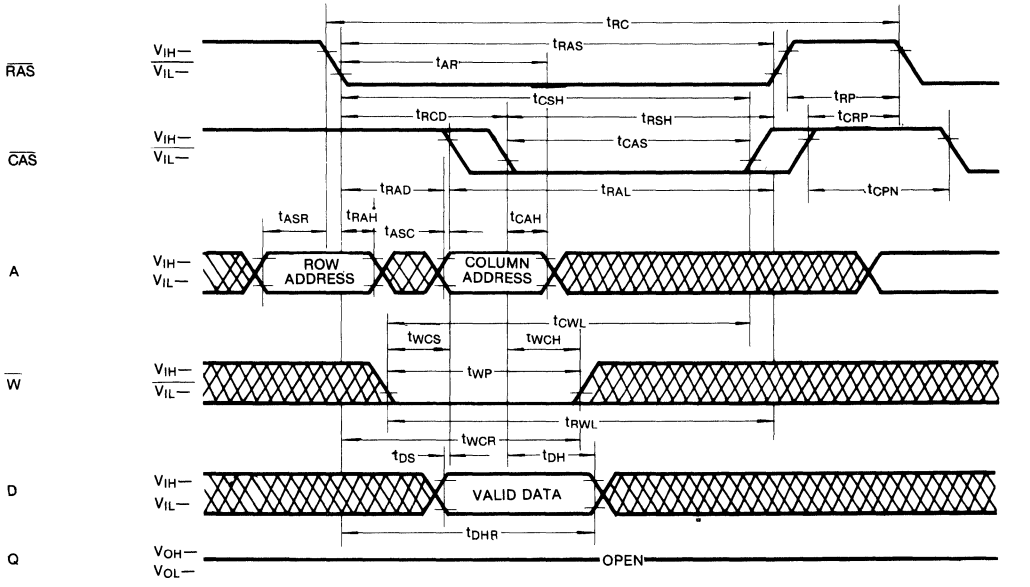
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non restrictive operating parameters. It is included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$(min) the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RCD}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. Normal operation requires the "T.F." pin to be connected to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
12. When the "T.F." pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung Semiconductor for specific operational details of the "test function".

TIMING DIAGRAMS

READ CYCLE

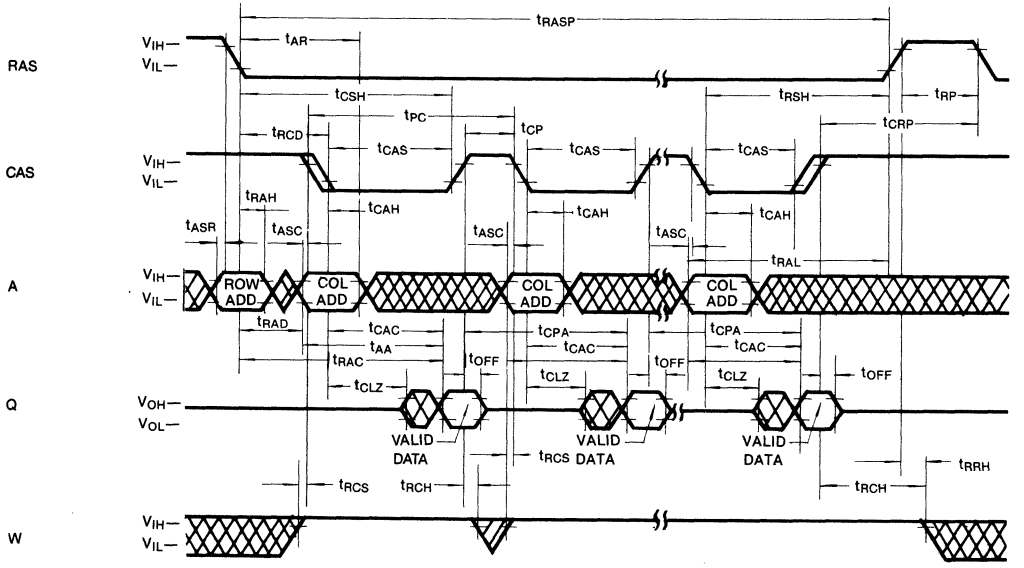


WRITE CYCLE (EARLY WRITE)

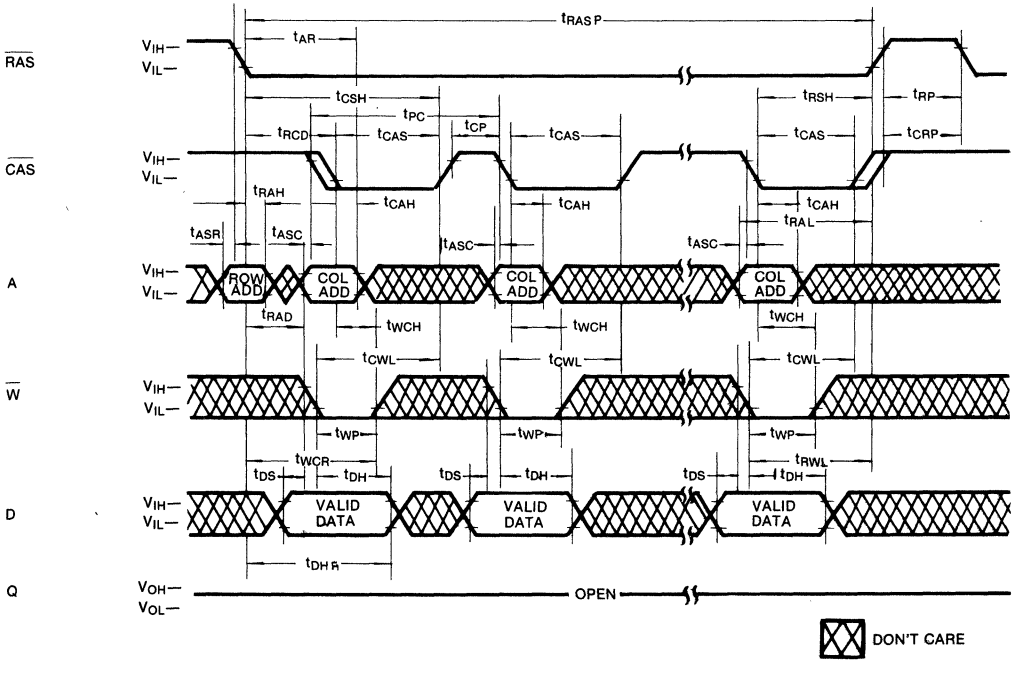


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



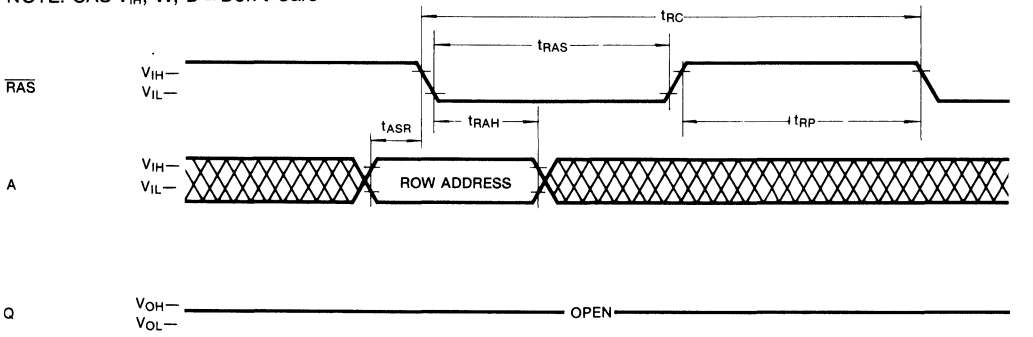
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



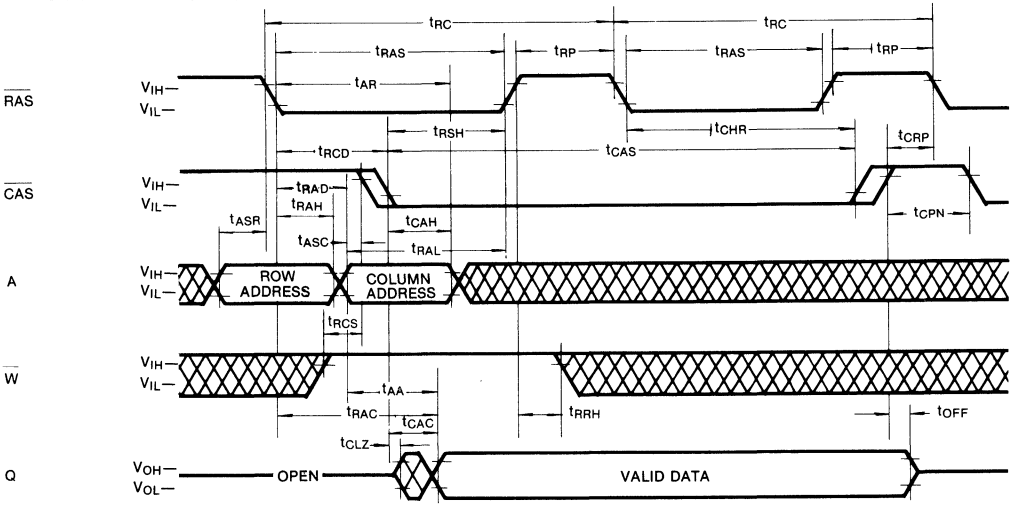
TIMING DIAGRAMS (Continued)

RAS-ONLY REFRESH CYCLE

NOTE: CAS-V_{IH}, W, D = Don't Care

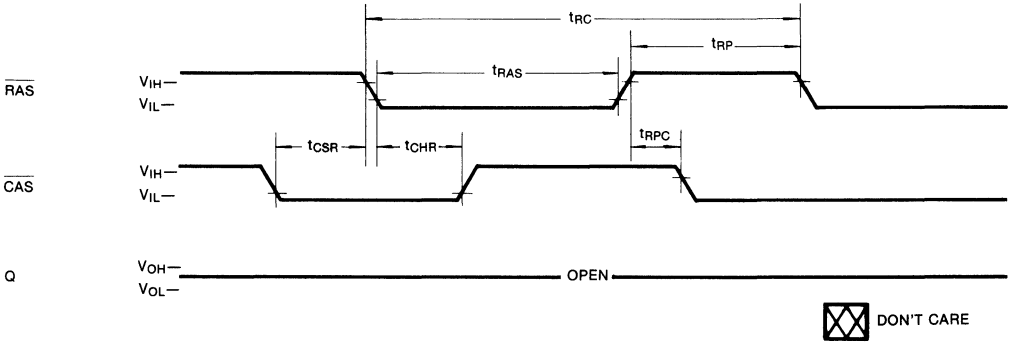


HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH CYCLE

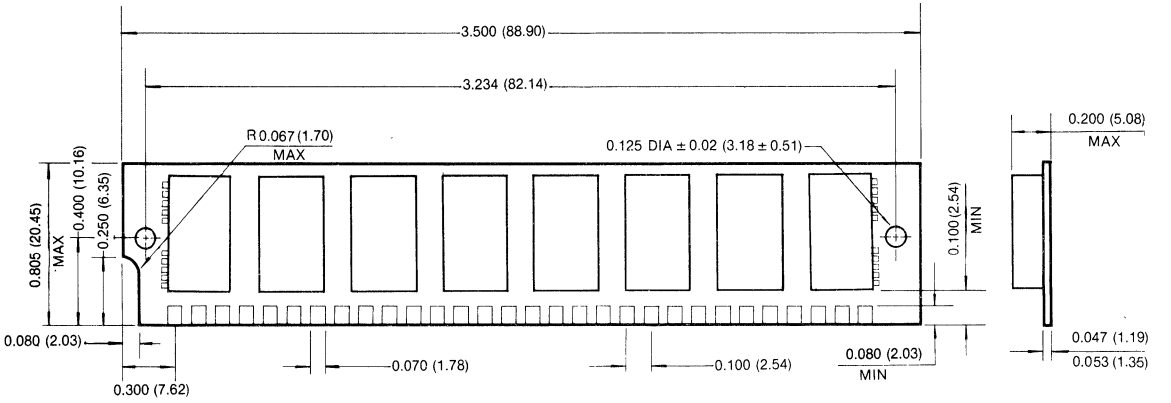
NOTE: Address, W, D = Don't Care



PACKAGE DIMENSIONS

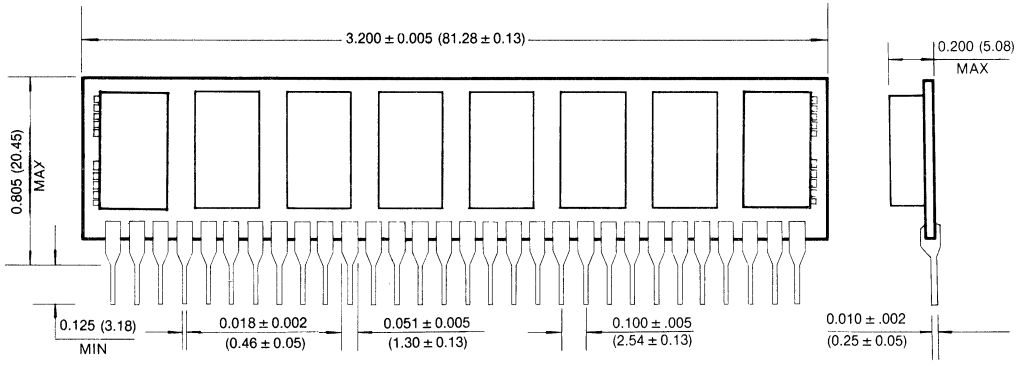
KMM581000 (1M x 8 SIMM)

Units: Inches (millimeters)



TOLERANCES: ± 0.005 (0.13) UNLESS OTHERWISE SPECIFIED

KMM481000 (1M x 8 SIP)



1M x 9 DRAM SIP and SIMM Memory Modules

FEATURES

- **1,048,576 x 9-bit Organization**
- **Ninth device has separate D, Q and $\overline{CAS}$ for Parity applications.**
- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM491000-10	100ns	25ns	190ns
KMM591000-10	100ns	25ns	190ns
KMM491000-12	120ns	30ns	220ns
KMM591000-12	120ns	30ns	220ns

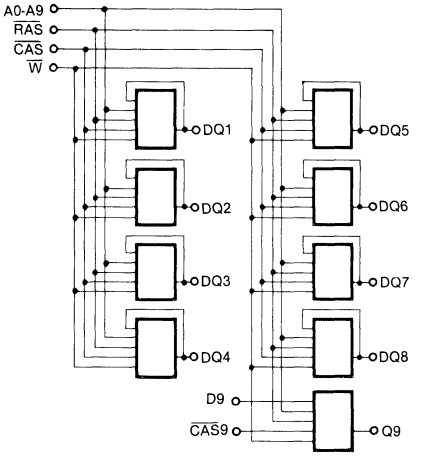
- **Fast Page Mode capability**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V ± 10% power supply**
- **512 cycles/8ms refresh**
- **JEDEC standard pinout**

GENERAL DESCRIPTION

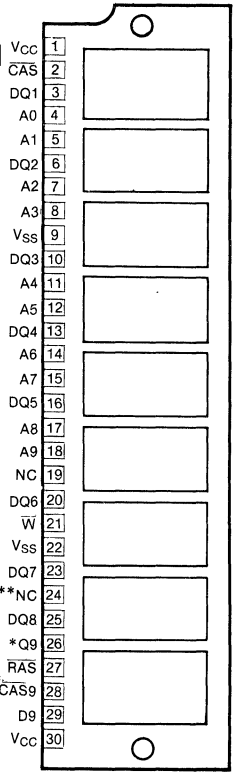
The Samsung KMM491000 and KMM591000 are 1M x 9 dynamic RAM high density memory modules. The ninth bit is generally used for parity and is controlled by $\overline{CAS9}$. Samsung 1M x 9 memory modules consist of nine KM41C1000 DRAMS in 20-pin SOJ packages mounted on a 30 pin glass-epoxy substrate. A 0.22μF decouping capacitor is mounted under each DRAM.

The 1M x 9 DRAM modules are available in two package styles. The KMM491000 is SIP with leads suitable for through hole mounting or for mounting in a socket. The KMM591000 is SIMM with edge connections and is intended for mounting into 30 pin edge connector socket.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



* FOR PARITY BIT
** TEST FUNCTION ON PIN 24 ALSO WILL BE AVAILABLE BY OPTION

PIN NAMES

Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ	Data In/Out
D_9	Data In
Q_9	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{CAS_9}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN NAMES

KMM491000-10	100ns	SIP	Page Mode
KMM491000-12	120ns	SIP	Page Mode
KMM591000-10	100ns	SIMM	Page Mode
KMM591000-12	120ns	SIMM	Page Mode

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	5.4	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min)	KMM491000-10, KMM591000-10 KMM491000-12, KMM591000-12	I_{CC1}	— —	540 450	mA mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	18	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @t_{RC} = min)	KMM491000-10, KMM591000-10 KMM491000-12, KMM591000-12	I_{CC3}	— —	540 450	mA mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling @t_{PC} = min)	KMM491000-10, KMM591000-10 KMM491000-12, KMM591000-12	I_{CC4}	— —	360 270	mA mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	9	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min)	KMM491000-10, KMM591000-10 KMM491000-12, KMM591000-12	I_{CC6}	— —	540 450	mA mA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0 volts)		I_{IL}	−90	90	μA
Output Leakage Current (Data out is disabled, 0 ≤ V_{OUT} ≤ 5.5V		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	C_{IN1}	—	60	pF
Input Capacitance (D_9, $\overline{CAS_9}$)	C_{IN2}	—	7	pF
Input Capacitance (DQ_1-DQ_8)	C_{DQ}	—	15	pF
Output Capacitance (D_9)	C_{Q9}	—	10	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1, 2)

Parameter	Symbol	KMM4(5)91000-10		KMM4(5)91000-12		Units	Notes
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	190		220		ns	
Access Time from $\overline{RAS}$	t_{RAC}		100		120	ns	3, 4, 10
Access Time from $\overline{CAS}$	t_{CAC}		25		30	ns	3, 4, 5
Access Time from Column Address	t_{AA}		50		60	ns	3, 10
Access Time from $\overline{CAS}$ Precharge	t_{CPA}		55		65	ns	3
CAS to Output in Low-Z	t_{CLZ}	5		5		ns	3
Output Buffer Turn-off Delay Time	t_{OFF}	0	30	0	35	ns	6
Transition Time (rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ Precharge Time	t_{RP}	80		90		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10,000	120	10,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	25		30		ns	
$\overline{CAS}$ Precharge time (except fast page)	t_{CPN}	15		20		ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100		120		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10,000	30	10,000	ns	
$\overline{RAS}$ to CAS Delay Time	t_{RCD}	25	75	25	90	ns	4
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	50	20	60	ns	10
$\overline{CAS}$ to RAS Precharge Time	t_{CRP}	10		10		ns	
Row Address Set-up Time	t_{ASR}	0		0		ns	
Row Address Hold Time	t_{RAH}	15		15		ns	
Column Address Set-up Time	t_{ASC}	0		0		ns	
Column Address Hold Time	t_{CAH}	20		25		ns	
Column Address Hold Time Reference to $\overline{RAS}$	t_{AR}	95		115		ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	50		60		ns	
Read Command Set-up Time	t_{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read Command Hold Time Reference to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write Command Hold Time	t_{WCH}	20		25		ns	

AC CHARACTERISTICS (Continued)

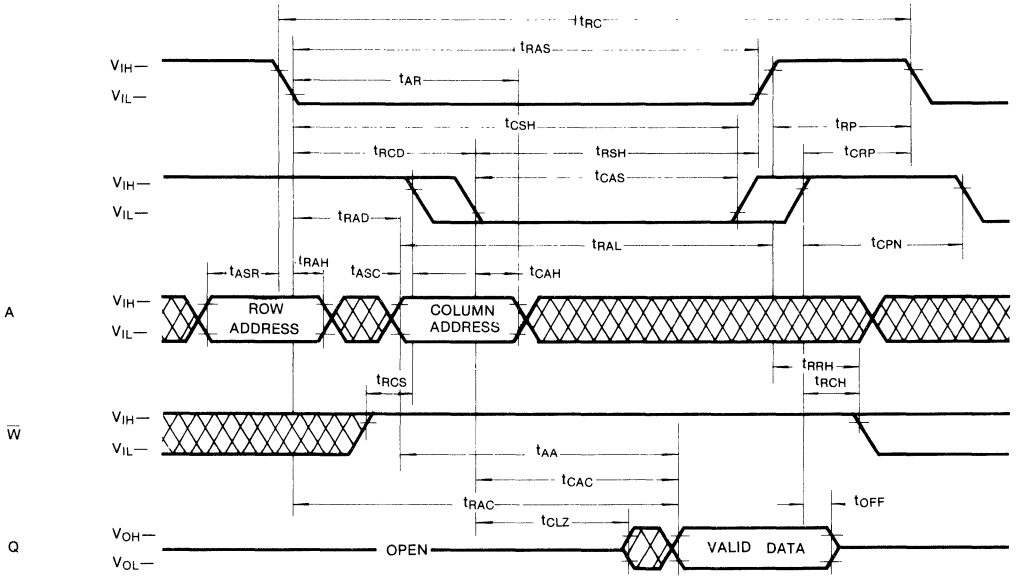
Parameter	Symbol	KMM4(5)91000-10		KMM4(5)91000-12		Units	Notes
		Min	Max	Min	Max		
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	95		115		ns	
Write Command Pulse Width	t_{WP}	20		25		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25		30		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25		30		ns	
Data-in Set-up Time	t_{DS}	0		0		ns	9
Data-in Hold Time	t_{DH}	20		25		ns	9
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	95		115		ns	
Refresh Period (512 cycles)	t_{REF}		8		8	ms	
Write Command Set-up Time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	30		30		ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10		10		ns	
Fast Page Mode Cycle Time	t_{PC}	60		70		ns	
$\overline{CAS}$ Precharge Time (fast page mode)	t_{CP}	10		15		ns	
$\overline{RAS}$ Pulse Width (fast page mode)	t_{RASP}	100	100,000	120	100,000	ns	

NOTES

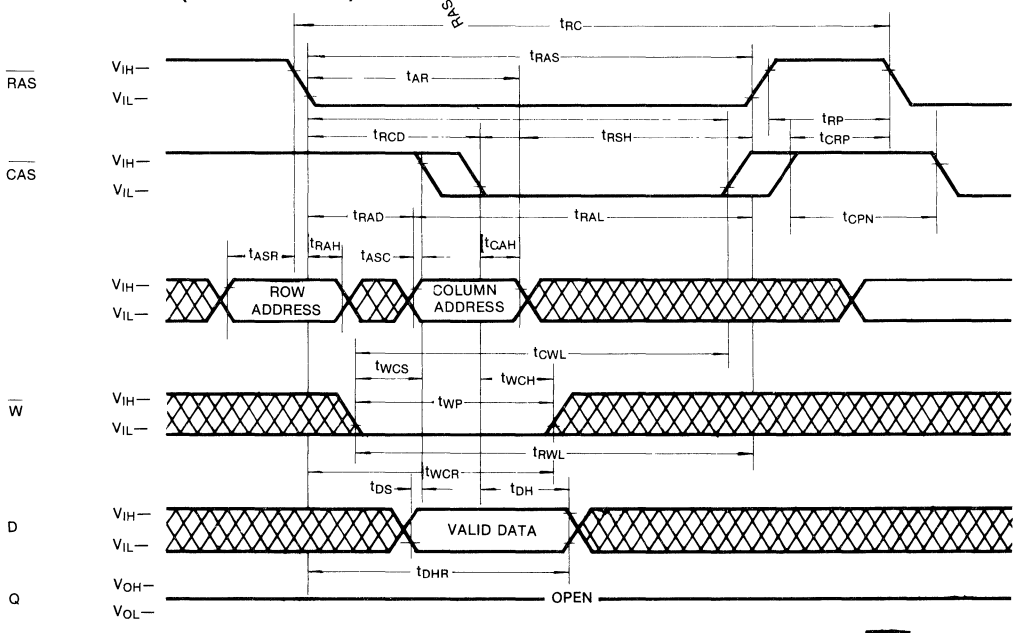
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non restrictive operating parameters. It is included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$(min) the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RCD}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. Normal operation requires the "T.F." pin to be connected to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
12. When the "T.F." pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung Semiconductor for specific operational details of the "test function".

TIMING DIAGRAMS

READ CYCLE

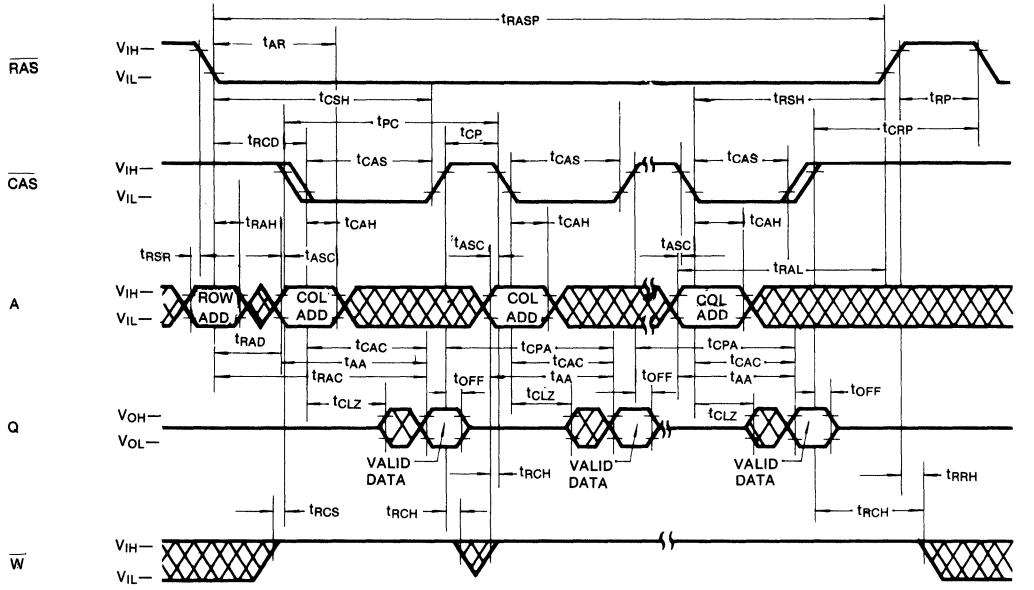


WRITE CYCLE (EARLY WRITE)

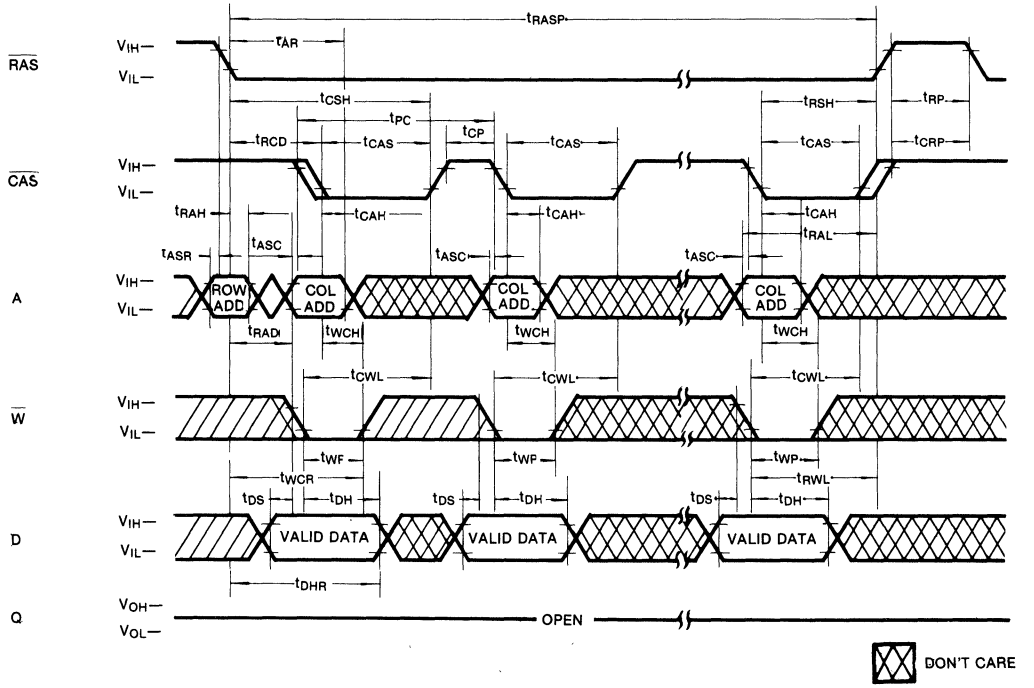


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



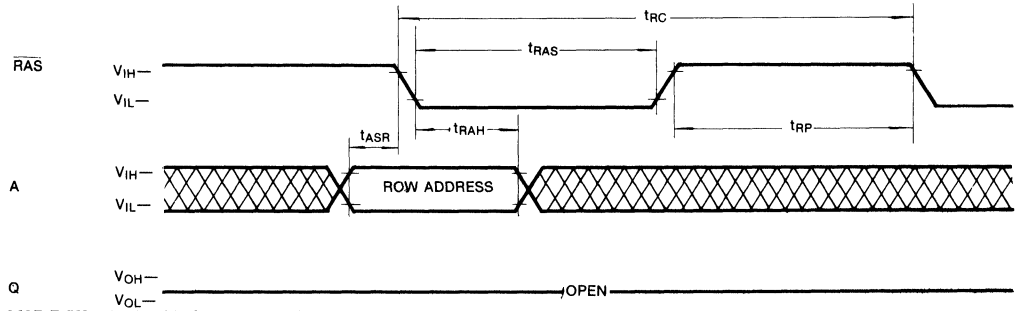
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



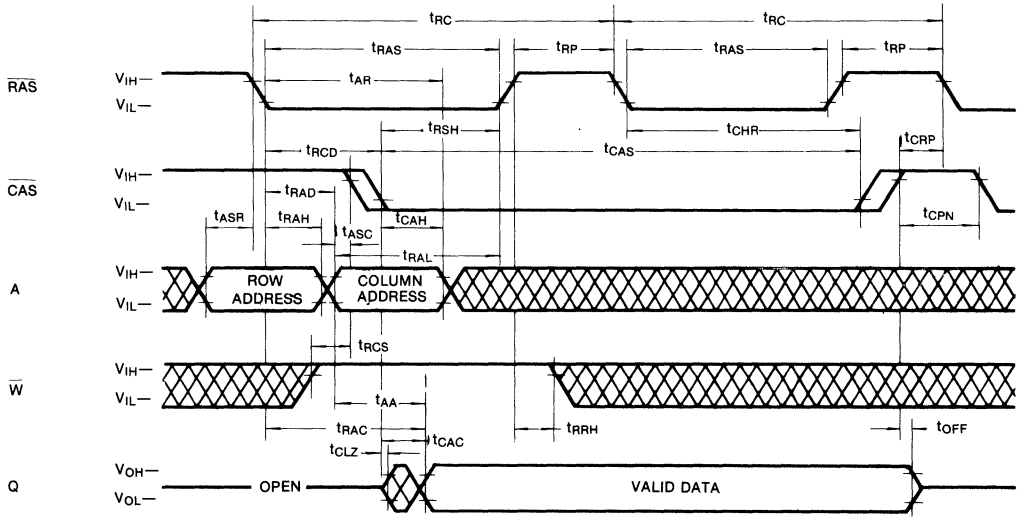
TIMING DIAGRAMS (Continued)

$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{CAS} = V_{IH}$, $\overline{W}$, A_9 = Don't Care

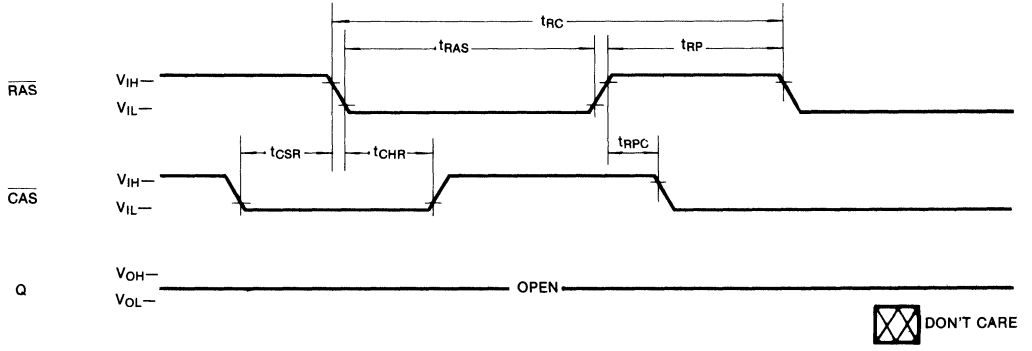


HIDDEN REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

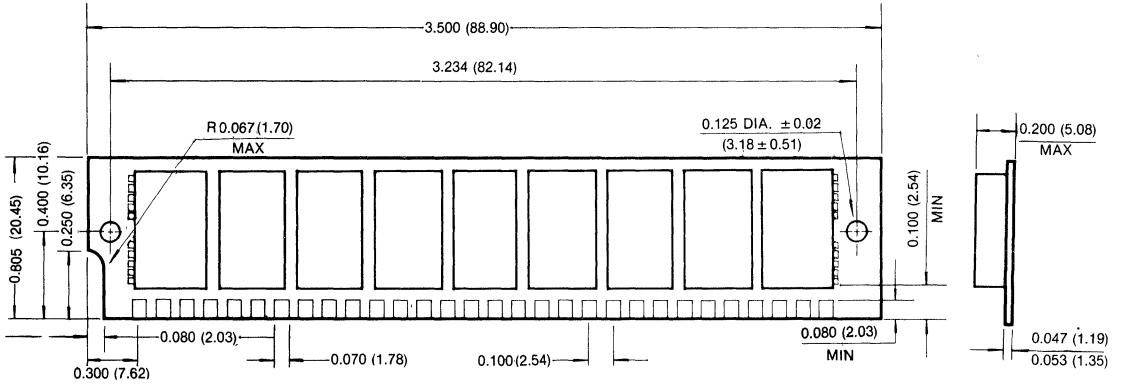
NOTE: Address, $\overline{W}$, D = Don't Care



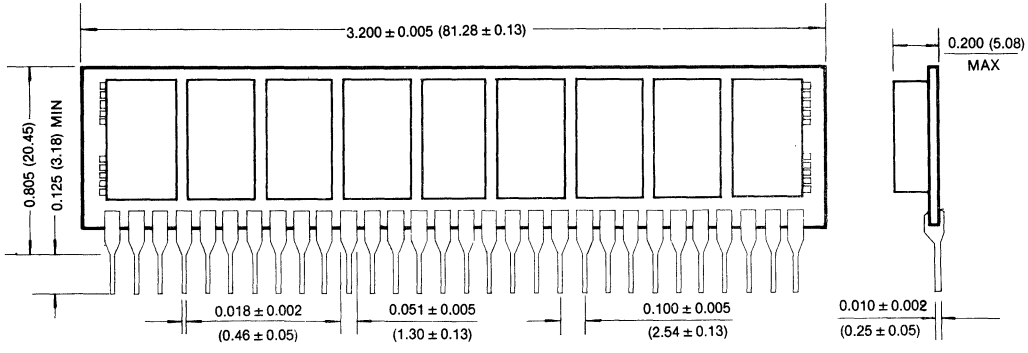
PACKAGE DIMENSIONS

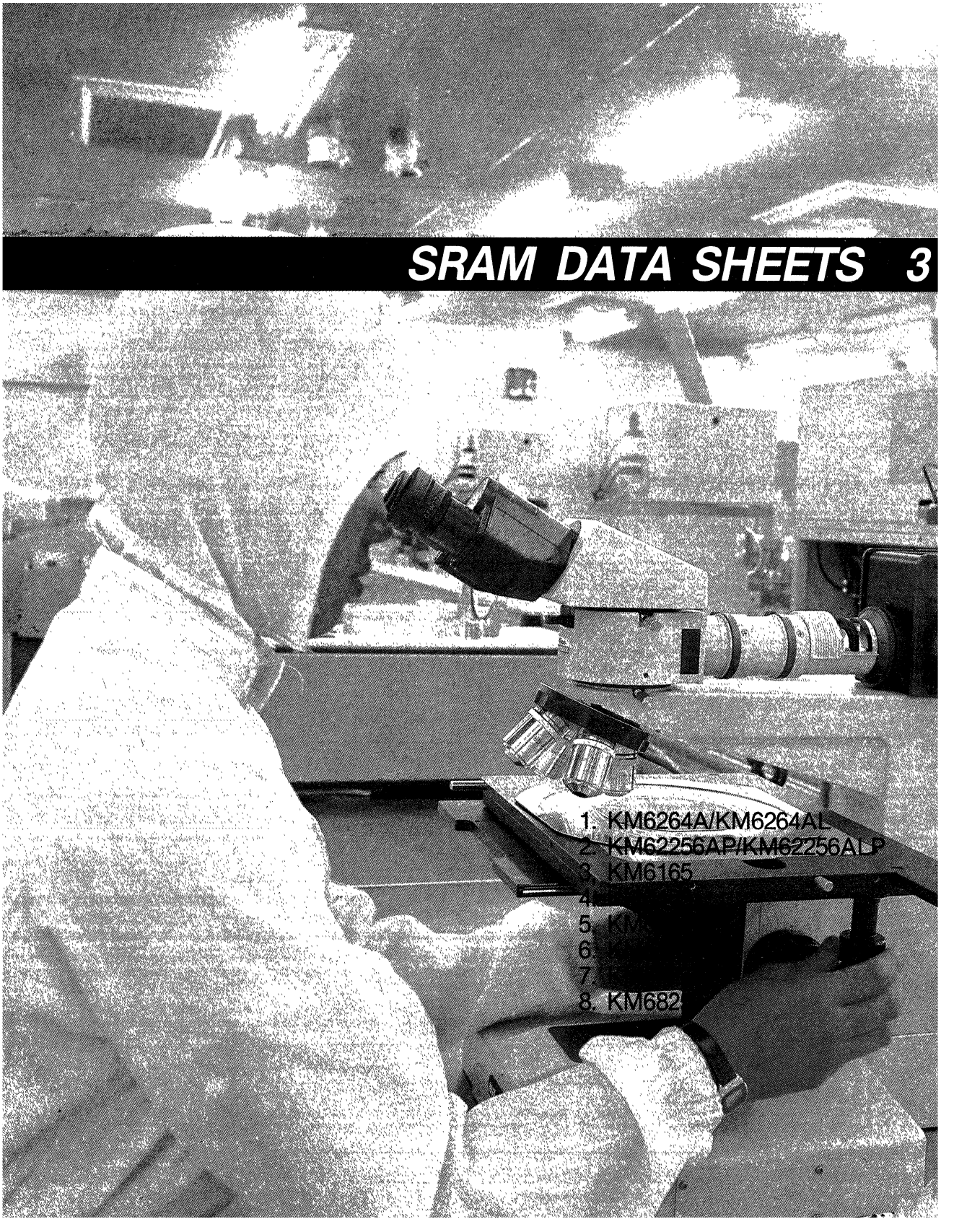
KMM591000 (1M x 9 SIMM)

Units: Inches (millimeters)



KMM491000 (1M x 9 SIP)





SRAM DATA SHEETS 3

1. KM6264A/KM6264AL
2. KM62256AP/KM62256ALP
3. KM6165
4.
5. KM
6.
7.
8. KM682

Static RAM

Capacity	Part Number	Organization	Speed (ns)	Technology	Current		Packages	Remark
					Active, mA Typ (max)	Standby, μA Typ (max)		
64K bit	†KM6264A-7	8K × 8	70	CMOS	35 (70)	(1mA)	28-Pin DIP	Now
	KM6264A-10	8K × 8	100	CMOS	35 (70)	(1mA)	28-Pin DIP	Now
	KM6264A-12	8K × 8	120	CMOS	35 (70)	(1mA)	28-Pin DIP	Now
	†KM6264AL-7	8K × 8	70	CMOS	35 (70)	(1mA)	28-Pin DIP	Now
	KM6264AL-10	8K × 8	100	CMOS	35 (70)	2 (0.1mA)	28-Pin DIP	Now
	KM6264AL-12	8K × 8	120	CMOS	35 (70)	2 (0.1mA)	28-Pin DIP	Now
64K bit	††KM6165-25	64K × 1	25	CMOS	(100)	(100)	22-Pin SDIP	under development
	KM6165-35	64K × 1	35	CMOS	(100)	(100)	22-Pin SDIP	under development
	KM6165-45	64K × 1	45	CMOS	(100)	(100)	22-Pin SDIP	under development
	KM6465-25	16K × 4	25	CMOS	(100)	(100)	22-Pin SDIP	under development
	KM6465-35	16K × 4	35	CMOS	(100)	(100)	22-Pin SDIP	under development
	KM6465-45	16K × 4	45	CMOS	(100)	(100)	22-Pin SDIP	under development
	KM6865-35	8K × 8	35	CMOS	(100)	(100)	28-Pin SDIP	under development
	KM6865-45	8K × 8	45	CMOS	(100)	(100)	28-Pin SDIP	under development
	KM6865-55	8K × 8	55	CMOS	(100)	(100)	28-Pin SDIP	under development
256K bit	KM62256P-10	32K × 8	100	CMOS	35 (60)	(1mA)	28-Pin DIP	Now
	KM62256P-12	32K × 8	120	CMOS	35 (60)	(1mA)	28-Pin DIP	Now
	KM62256P-15	32K × 8	150	CMOS	35 (60)	(1mA)	28-Pin DIP	Now
	KM62256LP-10	32K × 8	100	CMOS	35 (60)	(0.1mA)	28-Pin DIP	Now
	KM62256LP-12	32K × 8	120	CMOS	35 (60)	(0.1mA)	28-Pin DIP	Now
	KM62256LP-15	32K × 8	150	CMOS	35 (60)	(0.1mA)	28-Pin DIP	Now
	††KM61257-25	256K × 1	25	CMOS	(100)	(100)	24-Pin SDIP	under development
	KM61257-35	256K × 1	35	CMOS	(100)	(100)	24-Pin SDIP	under development
	KM61257-45	256K × 1	45	CMOS	(100)	(100)	24-Pin SDIP	under development
	KM64257-25	64K × 4	25	CMOS	(100)	(100)	24-Pin SDIP	under development
	KM64257-35	64K × 4	35	CMOS	(100)	(100)	24-Pin SDIP	under development
	KM64257-45	64K × 4	45	CMOS	(100)	(100)	24-Pin SDIP	under development
	KM68257-35	32K × 8	35	CMOS	(100)	(100)	28-Pin DIP	under development
	KM68257-45	32K × 8	45	CMOS	(100)	(100)	28-Pin DIP	under development
	KM68257-55	32K × 8	55	CMOS	(100)	(100)	28-Pin DIP	under development

† New Product
†† Under Development

8K x 8 Bit Static RAM

FEATURES

- **Fast Access Time 70, 100, 120ns (max.)**
- **Low Standby Current: 100μA (max.)**
- **Low Data Retention Current: 50μA (max.)**
- **Capability of Battery Back-up Operation**
- **Data Retention Voltage: 2.0V (min.)**
- **Single 5V ± 10% supply**
- **TTL compatible inputs and outputs**
- **Pin compatible with 64K EPROMS**
- **Fully Static Operation**
- **Standard 28 pin DIP**
- **Common I/O, Tristate Output**

GENERAL DESCRIPTION

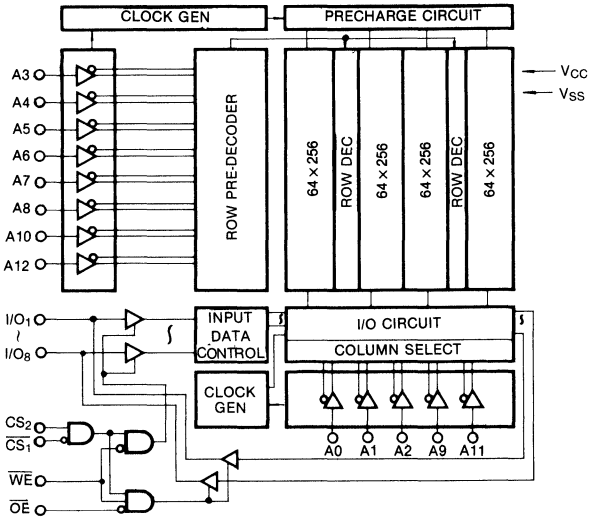
The KM6264A/AL is a 65,538-bit high speed Static Random Access Memory organized as 8,192 words by 8 bits. This device is fabricated using Samsung's advanced CMOS process.

The KM6264A/AL has an output enable input for precise control of the data outputs. It also has chip enable inputs for the minimum current power down mode. The KM6264A/AL has been designed for high speed and low power applications. It is particularly well suited for battery backup non-volatile memory applications.

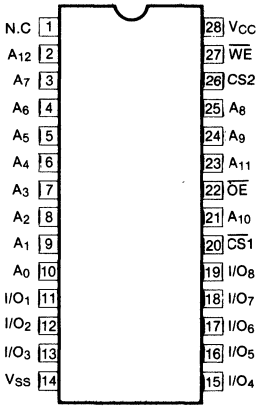
Two versions are available; the KM6264A and KM6264AL. The L-version is specified with lower standby and data retention currents than the standard version. Otherwise the two versions are identical.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{12}	Address Inputs
WE	Write Enable
CS_1, CS_2	Chip Select
OE	Output Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS* (See Note)

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−0.3 to V_{CC}+0.5	V
Voltage on V_{CC} supply relative V_{SS}	V_{CC}	−0.5 to +7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−55 to +125	°C
Operating Temperature	T_A	0 to +70	°C

*Note: Stresses greater than listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*Note: V_{IL} (min) = −3.0V for ≤50ns pulse.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Device	Min	Typ	Max	Units
Input Leakage Current	I_{LI}	$V_{IN}=V_{SS}$ to V_{CC}				2	μA
Output Leakage Current	I_{LO}	$\overline{CS1}=V_{IH}$ or CS2=V_{IL} or $\overline{OE}=V_{IH}$, $V_{SS}\leq V_{I/O}\leq V_{CC}$				2	μA
Operating Power Supply Current	I_{CC1}	$\overline{CS1}=V_{IL}$, CS2=V_{IH}, I_{OUT}=0mA				40	mA
Average Operating Current	I_{CC2}	Min Cycle, 100% Duty $\overline{CS1}=V_{IL}$, CS2=V_{IH}			35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}=V_{IH}$ or CS2=V_{IL}				3	mA
	I_{SB1}	$\overline{CS1}\geq V_{CC}-0.2V$	KM6264A			1	mA
		$-0.3V\leq CS2\leq 0.2V$	KM6264AL		2	100	μA
Output High Voltage	V_{OH}	I_{OH}=−1.0mA		2.4			V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA				0.4	V

CAPACITANCE (f=1MHz, T_A=25°C)*

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	8	pF

*Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

(Ta = 0°C to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.8 to 2.4V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Level	1.5V
Output Load	1 TTL Load and C_L* 100pF (including scope and jig capacitance)

*C_L = 30pF for KM6264A-7, KM6264AL-7

READ CYCLE

Parameter	Symbol	KM6264A-7 KM6264AL-7		KM6264A-10 KM6264AL-10		KM6264A-12 KM6264AL-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		100		120		ns
Address Cycle Time	t_{AA}		70		100		120	ns
Chip Select to Output	t_{CO1}, t_{CO2}		70		100		120	ns
Output Enable to Valid Output	t_{OE}		35		50		60	ns
Chip Enable to Low-Z Output	t_{LZ1}, t_{LZ2}	5		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	30	0	35	0	40	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	35	0	40	ns
Output Hold from Address Change	t_{OH}	10		10		15		ns

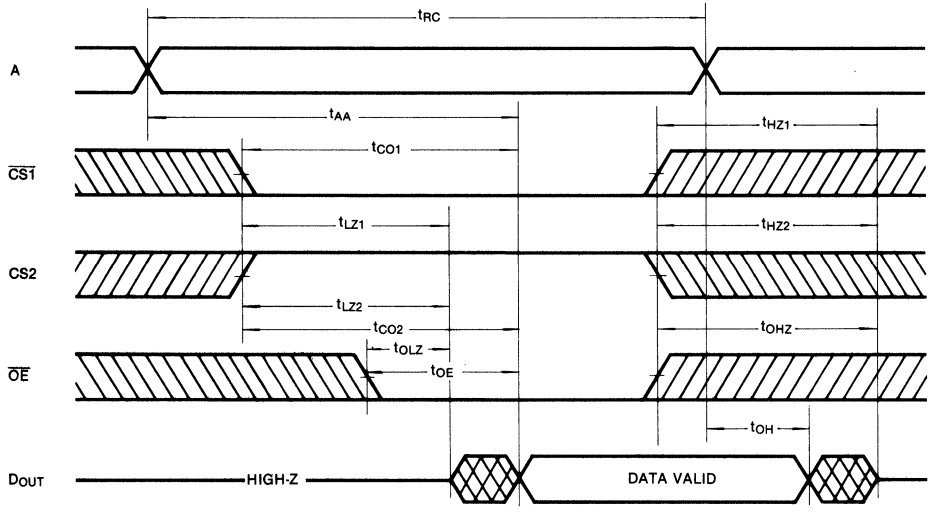
WRITE CYCLE

Parameter	Symbol	KM6264A-7 KM6264AL-7		KM6264A-10 KM6264AL-10		KM6264A-12 KM6264AL-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		100		120		ns
Chip Select to End of Write	t_{CW}	60		80		85		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	60		80		85		ns
Write Pulse Width	t_{WP}	40		60		70		ns
Write Recovery from $\overline{CS1}$ or $\overline{WE}$	t_{WR1}, t_{WR}	0		5		5		ns
Write Recovery from CS2	t_{WR2}	10		15		15		ns
Write to Output High-Z	t_{WHZ}	0	30	0	35	0	40	ns
Data to Write Time Overlap	t_{DW}	30		40		50		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End of Write to Output Low-Z	t_{OW}	5		5		10		ns

NOTES:
1. t_{HZ} AND t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to the V_{OH} or V_{OL} levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
3. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
4. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
5. t_{AS} is measured from the address valid to the beginning of write.
6. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends at $\overline{CS1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS2 going low.
7. If $\overline{OE}$, CS2 and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase to the outputs must not be applied because bus contention can occur.
8. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
9. D_{OUT} is the read data of the new address.
10. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the output must not be applied to them.
11. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
12. When $\overline{CS1}$ is low and CS2 is high, the address input must not be in the high impedance state.

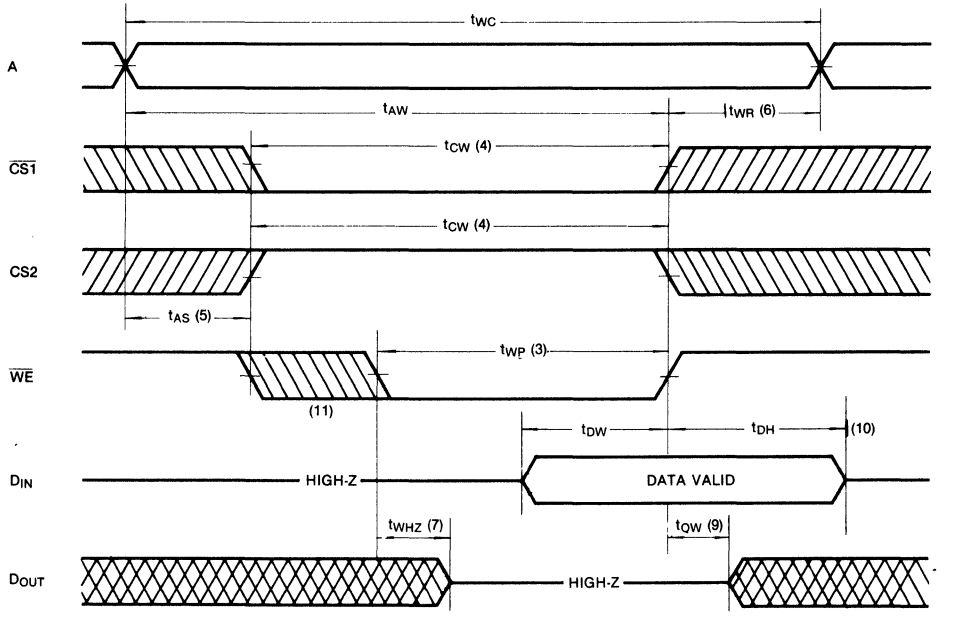
TIMING DIAGRAMS

READ CYCLE ($\overline{WE} = V_{IH}$)

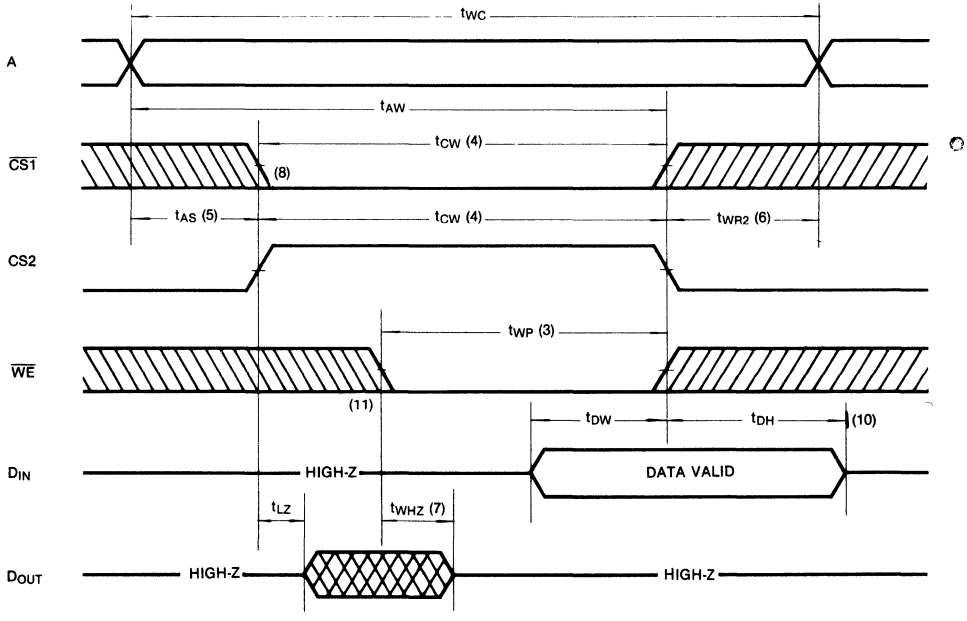


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{WE}$ CONTROLLED)

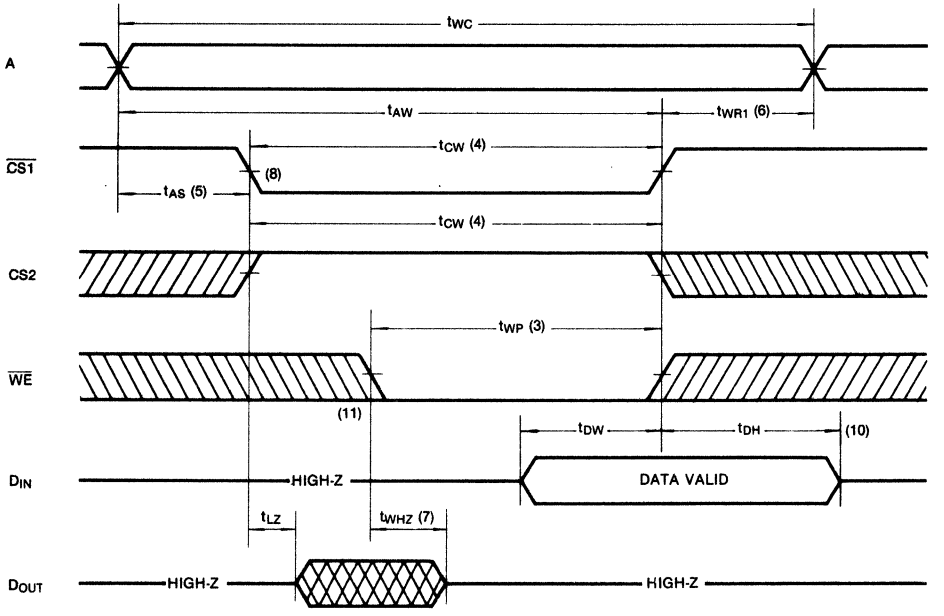


WRITE CYCLE ($\overline{CS1}$ CONTROLLED)



TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{CS2}$ CONTROLLED)

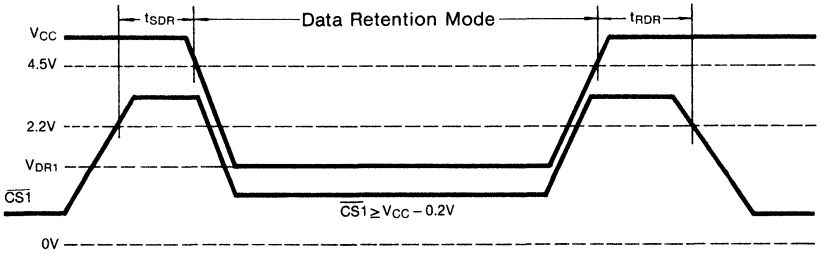


DATA RETENTION CHARACTERISTICS (T_A = 0°C to +70°C)

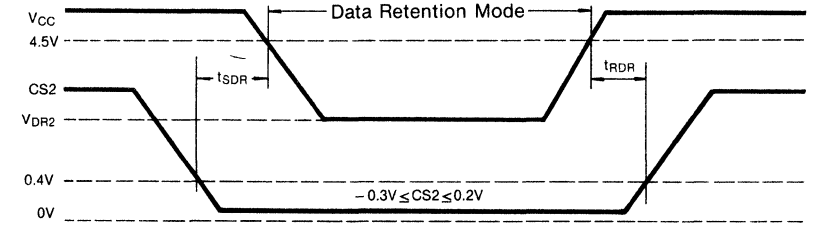
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
V_{CC} for Data Retention	V_{DR1}	$\overline{CS1} \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	2.0	—	5.5	V
	V_{DR2}	$CS2 \leq 0.2V$	2.0	—	5.5	V
Data Retention	I_{DR1}	V_{CC} 3.0V, $\overline{CS1} \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	—	1	50*	μA
	I_{DR2}	$V_{CC} = 3.0V$, $CS2 \leq 0.2V$	—	1	50*	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Wave forms (below)	0			ns
Recovery Time	t_{RDR}		t_{RC}**			ns

* 20μA max at T_A = 0 40°C, KM6264A: 1.0mA (MAX)
** t_{RC} = Read Cycle Time

DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM (2) (CS2 Controlled)



NOTE: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, V_{IN} for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

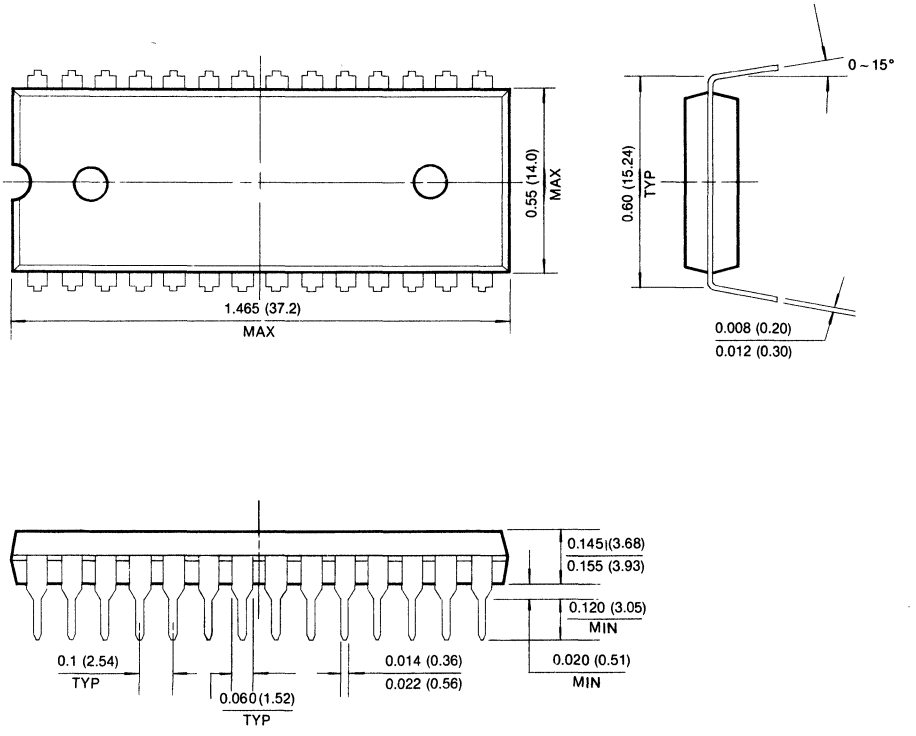
FUNCTION TABLE

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
X	H	X	X	Power Down	High-Z	I_{SB}
X	X	L	X	Power Down	High-Z	I_{SB}
H	L	H	H	Output Disabled	High-Z	I_{CC}
H	L	H	L	Read	D_{OUT}	I_{CC}
L	L	H	X	Write	D_{IN}	I_{CC}

PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



32K x 8 Bit Static RAM

FEATURES

- **Fast Access Time 80, 100, 120ns (max.)**
- **Low Power Dissipation**
  - **Standby: 0.55mW (max.)**
  - **Operating: 248mW (max.)**
- **Low Data Retention Current: 50μA (max.)**
- **Capability of Battery Back-up Operation**
- **Data Retention Voltage: 2.0V (min.)**
- **Single 5V ± 10% supply**
- **TTL compatible inputs and outputs**
- **Pin compatible with 256K EPROMS**
- **Full Static Operation**
  - **— No clock or refresh required**
- **Standard 28 pin DIP**
- **Common I/O, Tristate Output**

GENERAL DESCRIPTION

The KM62256AP/ALP is a 262,144 bit high speed Static Random Access Memory organized as 32,768 words by 8 bits.

This device is fabricated using Samsung's advanced CMOS technology with polysilicon resistors.

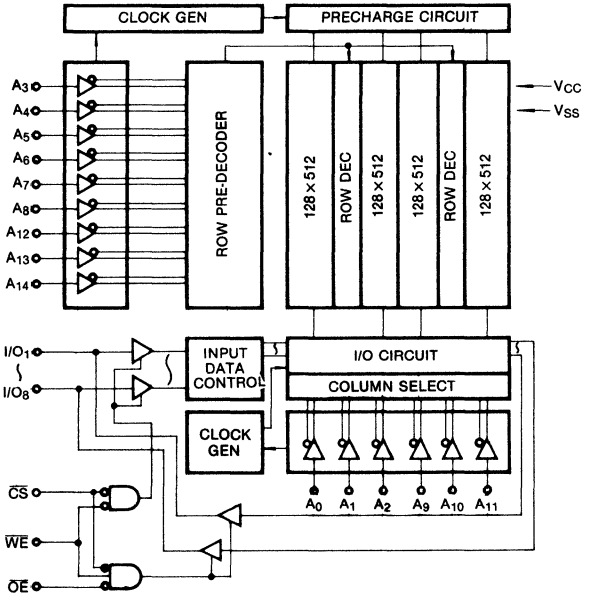
The KM62256AP/ALP has an output enable for precise control of the data output.

It also has a chip enable for the minimum current power down mode. The KM62256AP/ALP has been designed for high speed and low power applications. It is particularly well suited for battery backup non-volatile memory applications.

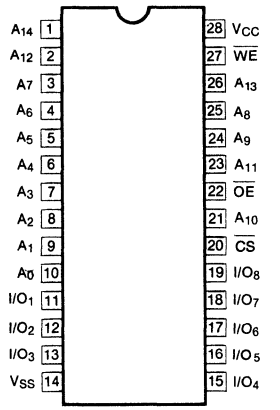
Two versions are available the KM62256ALP and KM62256ALP. The L-version is specified with lower standby and data retention currents than the standard version.

Otherwise the two versions are identical.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0—A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1—I/O_8	Data Inputs/Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (See Note)*

Rating	Symbol	Value	Units
Voltage on any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.3 to $V_{CC}+0.5$	V
Voltage on V_{CC} Supply Relative V_{CC}	V_{CC}	-0.5 to $+7.0$	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-55 to $+125$	°C
Operating Temperature	T_A	0 to $+70$	°C

*Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	$V_{CC}+0.5$	V
Input Low Voltage	V_{IL}	-0.3*	—	0.8	V

Note: V_{IL}(min) = -3.0V for $\leq$50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Device	Min	Typ	Max	Units
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}				1	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ $V_{I/O} = V_{SS}$ to V_{CC}				1	μA
Operating Power Supply Current	I_{CC1}	$\overline{CS} = V_{IL}$, I_{OUT} = 0mA				45	mA
Average Operating Current	I_{CC2}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, I_{OUT} = 0mA			35	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$				2	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$	KM62256AP			1	mA
			KM62256ALP		2	100	μA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA				0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -1.0$mA		2.4			V

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, $f = 1.0$ MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF

Note: Capacitance is periodically sampled and not 100% tested.

AC CHARACTERISTICS

($T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.8 to 2.4V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL Load and $C_L = 100$ pF (including scope and jig capacitance)

READ CYCLE

Parameter	Symbol	KM62256AP-8 KM6264ALP-8		KM62256AP-10 KM6264ALP-10		KM62256AP-12 KM6264ALP-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	80		100		120		ns
Address Access Time	t_{AA}		80		100		120	ns
Chip Select to Output	t_{ACS}		80		100		120	ns
Output Enable to Valid Output	t_{OE}		40		50		60	ns
Chip Enable to Low-Z Output	t_{CLZ}	5		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{CHZ}	0	30	0	35	0	40	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	35	0	40	ns
Output Hold from Address Change	t_{OH}	5		10		15		ns

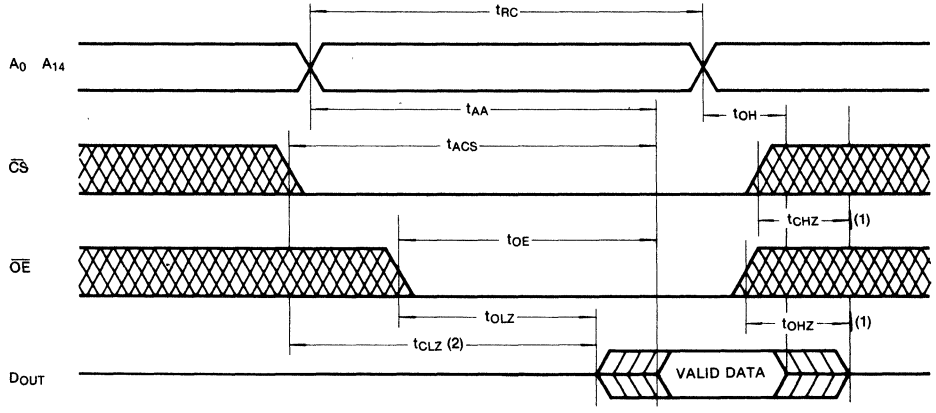
WRITE CYCLE

Parameter	Symbol	KM62256AP-8 KM62256ALP-8		KM62256AP-10 KM62256ALP-10		KM62256AP-12 KM62256ALP-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	80		100		120		ns
Chip Select to End of Write	t_{CW}	70		80		85		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	70		80		85		ns
Write Pulse Width	t_{WP}	55		60		70		ns
Write Recovery Time	t_{WR}	0		5		5		ns
Write to Output High-Z	t_{WHZ}	0	30	0	35	0	40	ns
Data to Write Time Overlap	t_{DW}	30		40		50		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End of Write to Output Low-Z	t_{OW}	5		10		10		ns

NOTES:
1. t_{CHZ} and t_{OHZ} are definded as the time at which the outputs achieve the open circuit condition and are not referenced to the V_{OH} or V_{OL} level.
2. At any given temperature and voltage condition, t_{CHZ} max is less then t_{CLZ} min both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.
5. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
6. During this period, I/O pins are in the output state. The input signals out of phase must not applied.
7. $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
8. If $\overline{OE}$ is high, I/O pins remain in a high-impedance state.
9. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
10. When Chip Select ($\overline{CS}$) is low, the address input must not be in the high impedance state.

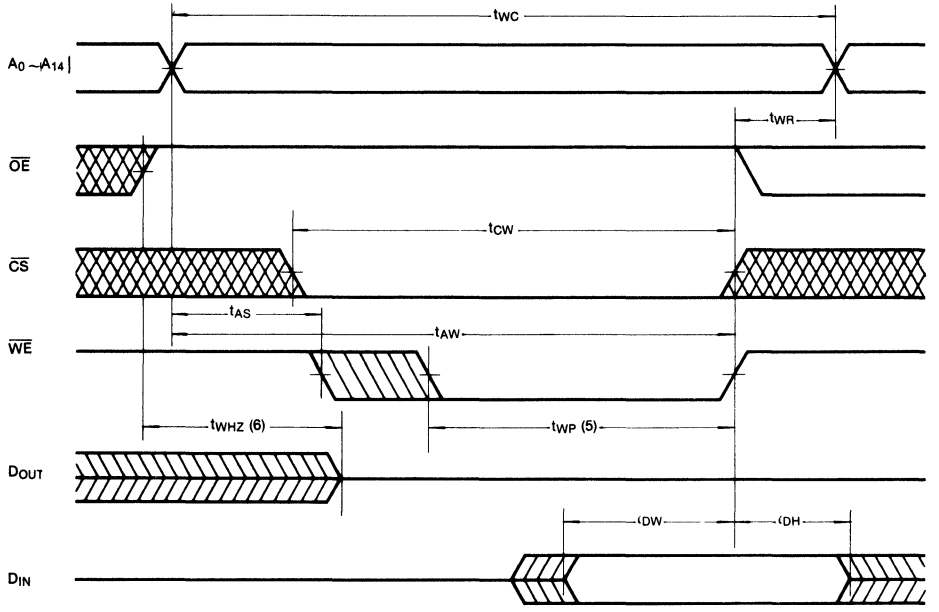
TIMING DIAGRAMS

READ CYCLE (NOTE 1,2,3,4)

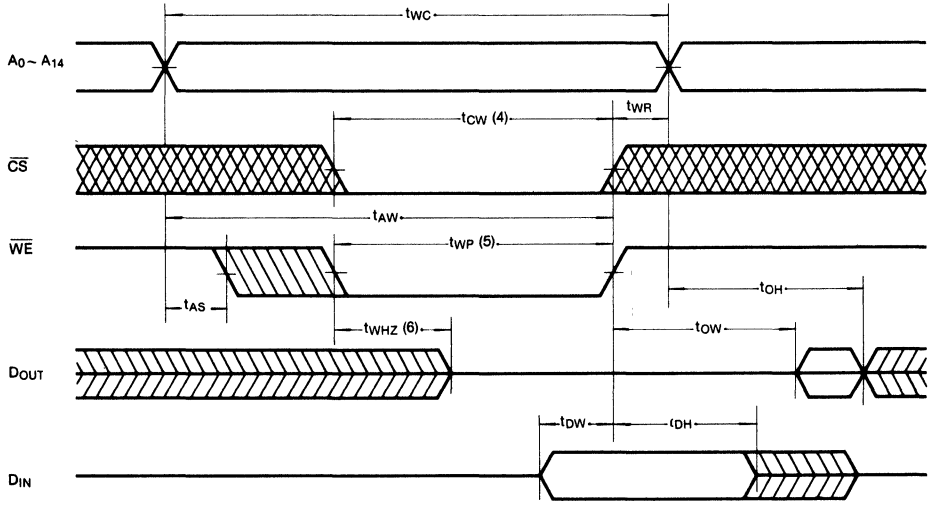


TIMING DIAGRAMS (Continued)

WRITE CYCLE 1 ($\overline{WE}$ CONTROLLED) (NOTE 5,6,7,8)



WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED) (NOTE 5,6,7,8,9)

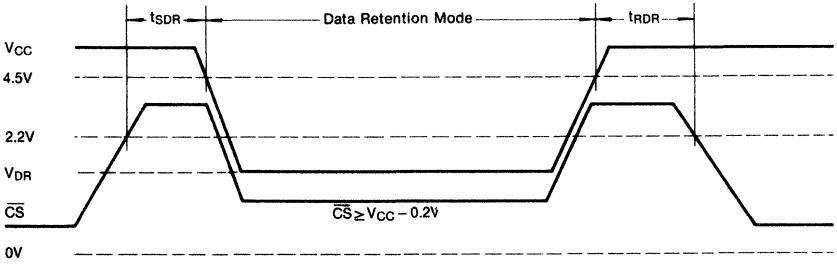


DATA RETENTION CHARACTERISTICS (T_A = 0°C to +70°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I_{DR}	$V_{CC} = 3.0V$ $\overline{CS} \geq V_{CC} - 0.2V$		1	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Wave forms (below)	0			ns
Recovery Time	t_{RDR}		t_{RC}*			ns

* t_{RC} = Read Cycle Time

DATA RETENTION WAVEFORM

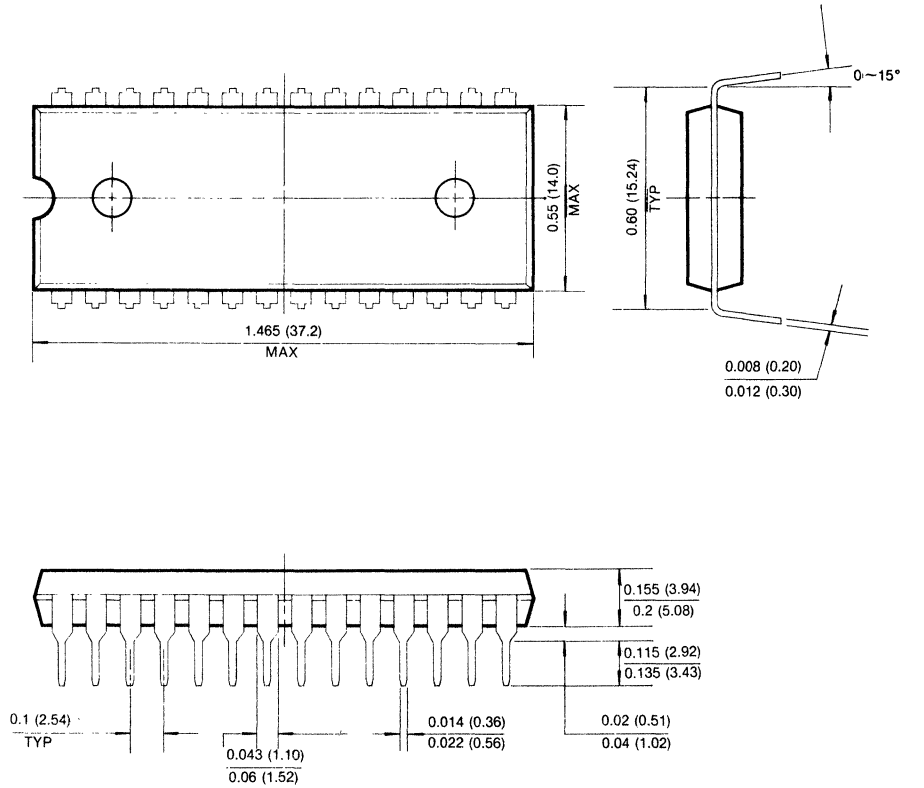


Note: The Other inputs (Address, $\overline{OE}$, $\overline{WE}$, I/O) can be in a high impedance state

PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



64K x 1 Bit Static RAM

FEATURES

- **Fast Access Time 25, 35, 45ns (max.)**
- **Low Power Dissipation**
  Standby (TTL): 2mA (max.)
  (CMOS): 100μA (max.)
  Operating : 100mA (max.)
- **Single 5V ± 10% supply**
- **TTL compatible inputs and outputs**
- **Full Static Operation**
  —No clock or refresh required
- **Tristate Output**
- **Low Data Retention Current: 50μA (max.)**
- **Battery Back-up Operation**
  —2V (min.) Data Retention
- **Standard 24-pin DIP (300 mil)**

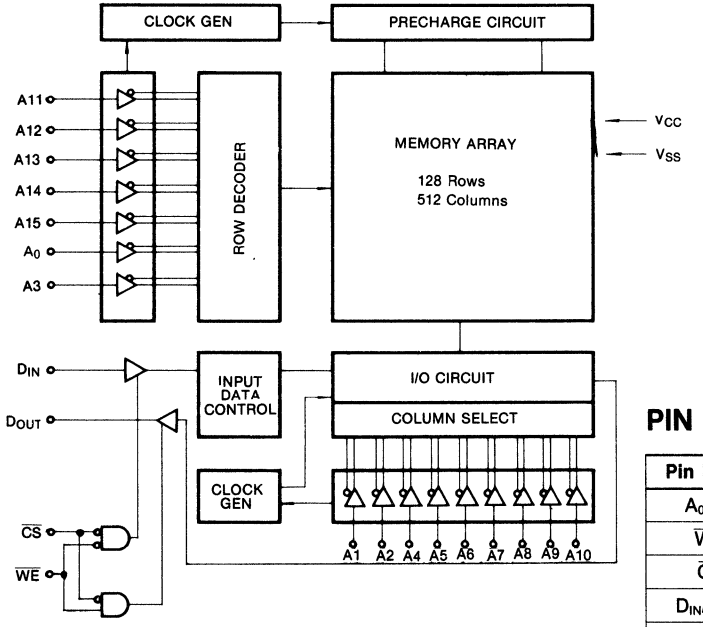
GENERAL DESCRIPTION

The KM6165 is a 65,538-bit high speed Static Random Access Memory organized as 65,538 words by 1 bit. The device is fabricated using Samsung's advanced CMOS process.

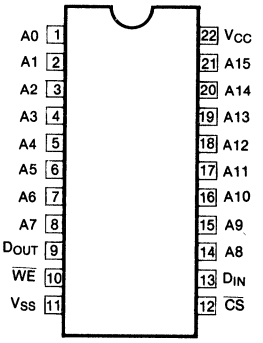
The KM6165 has a chip enable input for the minimum current power down mode.

The KM6165 has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back up for nonvolatility is required.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin Name	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
D_{IN}/D_{OUT}	Data Input /Output
V_{CC}	+5V Power Supply
V_{SS}	Ground

16K x 4 Bit Static RAM

FEATURES

- **Fast Access Time 25, 35, 45ns (max.)**
- **Low Power Dissipation**
  Standby (TTL): 2mA (max.)
  (CMOS): 100μA (max.)
  Operating : 100mA (max.)
- **Single 5V ± 10% supply**
- **TTL compatible inputs and outputs**
- **Full Static Operation**
  —No clock or refresh required
- **Common I/O, Tristate Output**
- **Low Data Retention Current: 50μA (max.)**
- **Battery Back-up Operation**
  —2V (min.) Data Retention
- **Standard 22-pin DIP (300 mil)**

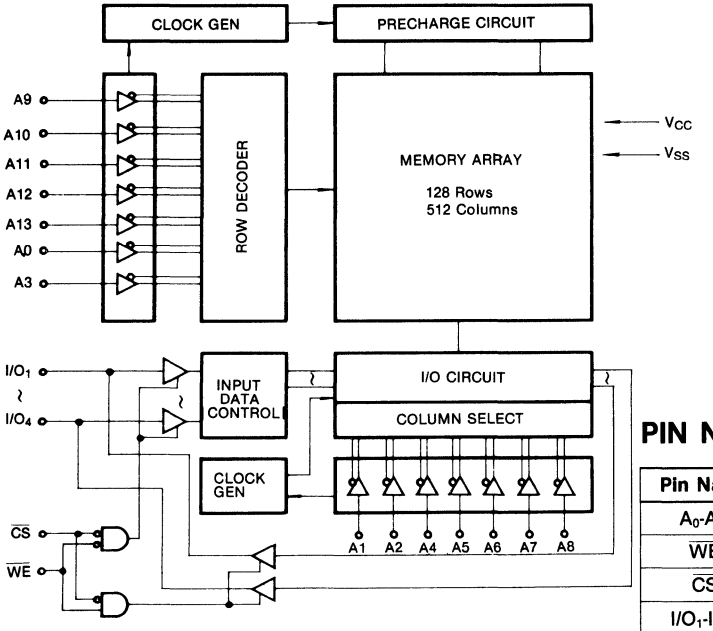
GENERAL DESCRIPTION

The KM6465 is a 65,538-bit high speed Static Random Access Memory organized as 16,384 words by 4 bits. The device is fabricated using Samsung's advanced CMOS process.

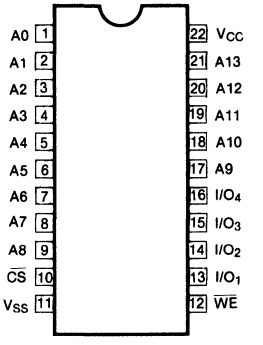
The KM6465 has a chip enable input for the minimum current power down mode.

The KM6465 has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back up for nonvolatility is required.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin Name	Pin Function
A_0-A_{13}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground

8K x 8 Bit Static RAM

FEATURES

- **Fast Access Time 35, 45, 55ns (max.)**
- **Low Power Dissipation**
  Standby (TTL): 2mA (max.)
  (CMOS): 100μA (max.)
  Operating : 100mA (max.)
- **Single 5V ± 10% supply**
- **TTL compatible inputs and outputs**
- **Full Static Operation**
  —No clock or refresh required
- **Common I/O, Tristate Output**
- **Low Data Retention Current: 50μA (max.)**
- **Battery Back-up Operation**
  —2V (min.) Data Retention
- **Standard 28-pin DIP (300 mil)**

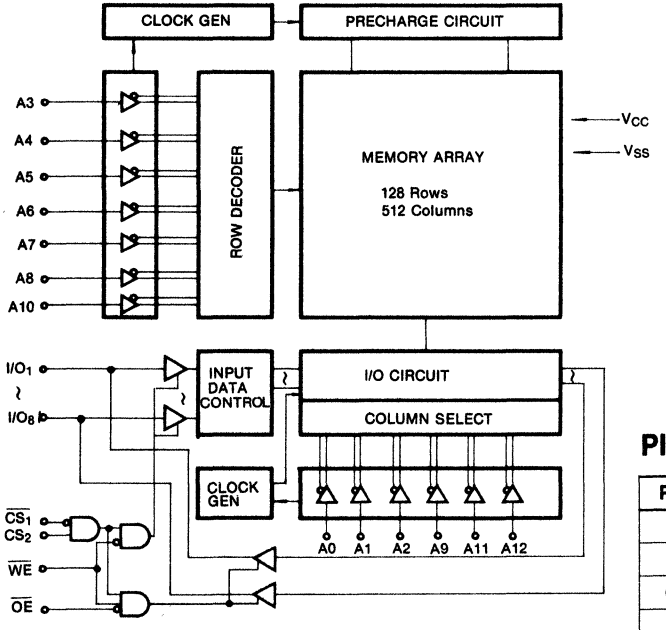
GENERAL DESCRIPTION

The KM6865 is a 65,538-bit high speed Static Random Access Memory organized as 8,192 words by 8 bits. The device is fabricated using Samsung's advanced CMOS process.

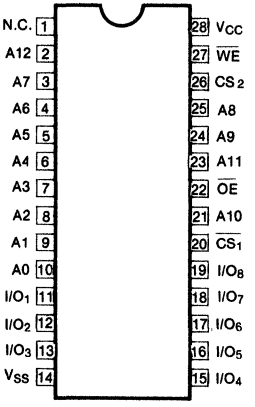
The KM6865 has an output enable input for precise control of the data outputs. It also has chip enable inputs for the minimum current power down mode.

The KM6865 has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back up for nonvolatility is required.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin Name	Pin Function
A_0-A_{12}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS_1}$, CS_2	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground
N.C.	No Connection

256K x 1 Bit Static RAM

FEATURES

- **Fast Access Time 25, 35, 45ns (max.)**
- **Low Power Dissipation**
  Standby (TTL): 2mA (max.)
  (CMOS): 100μA (max.)
  Operating : 100mA (max.)
- **Single 5V ± 10% supply**
- **TTL compatible inputs and output**
- **Full Static Operation**
  —No clock or refresh required
- **Tristate Output**
- **Low Data Retention Current: 50μA (max.)**
- **Battery Back-up Operation**
  —2V (min.) Data Retention
- **Standard 24-pin DIP (300 mil)**

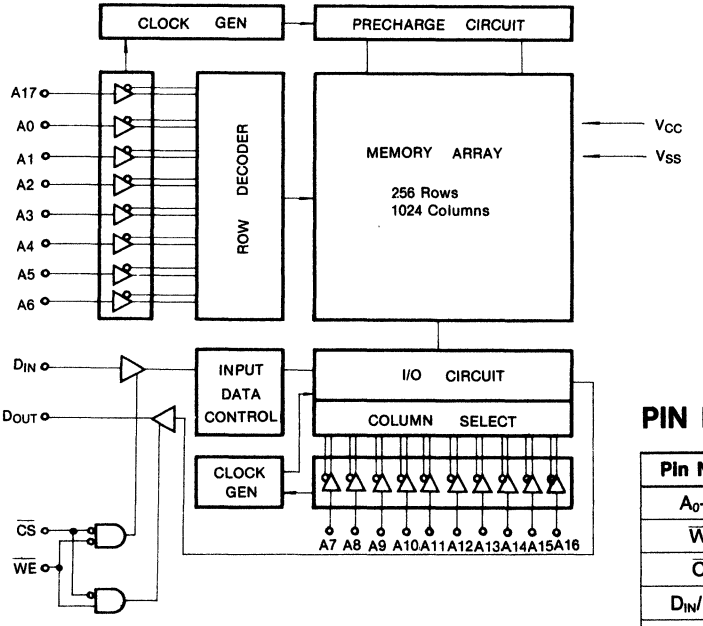
GENERAL DESCRIPTION

The KM61257 is a 262,144-bit high speed Static Random Access Memory organized as 262,144 words by 1 bit. The device is fabricated using Samsung's advanced CMOS process.

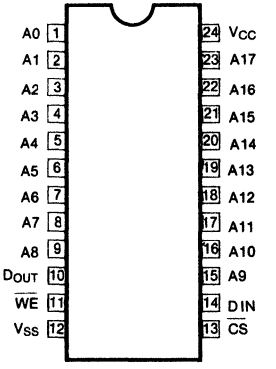
The KM61257 has a chip enable input for the minimum current power down mode.

The KM61257 has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back up for nonvolatility is required.

FUNCTION BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin Name	Pin Function
A_0-A_{17}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
D_{IN}/D_{OUT}	Data Inputs/Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground

64K × 4 Bit Static RAM

FEATURES

- **Fast Access Time 25, 35, 45ns (max.)**
- **Low Power Dissipation**
  Standby (TTL) : 2mA (max.)
  (CMOS): 100μA (max.)
  Operating : 100mA (max.)
- **Single 5V ± 10% supply**
- **TTL compatible inputs and outputs**
- **Full Static Operation**
  —No clock or refresh required
- **Common I/O, Tristate Output**
- **Low Data Retention Current: 50μA (max.)**
- **Battery Back-up Operation**
  —2V (min.) Data Retention
- **Standard 24-pin DIP (300 mil)**

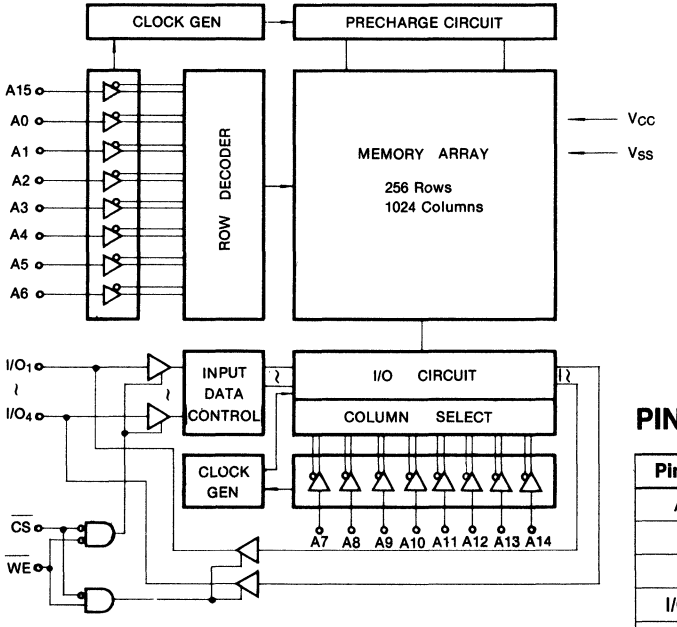
GENERAL DESCRIPTION

The KM64257 is a 262,144-bit high speed Static Random Access Memory organized as 65,538 words by 4 bits. The device is fabricated using Samsung's advanced CMOS process.

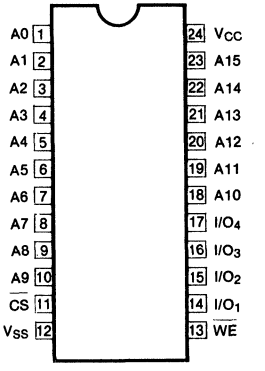
The KM64257 has a chip enable input for the minimum current power down mode.

The KM64257 has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back up for nonvolatility is required.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin Name	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground

32K x 8 Bit Static RAM

FEATURES

- **Fast Access Time 35, 45, 55ns (max.)**
- **Low Power Dissipation**
  Standby (TTL) : 2mA (max.)
  (CMOS): 100μA (max.)
  Operating : 100mA (max.)
- **Single 5V ± 10% supply**
- **TTL compatible inputs and outputs**
- **Full Static Operation**
  —No clock or refresh required
- **Common I/O, Tristate Output**
- **Low Data Retention Current: 50μA (max.)**
- **Battery Back-up Operation**
  —2V (min.) Data Retention
- **Standard 28-pin DIP (600 mil)**

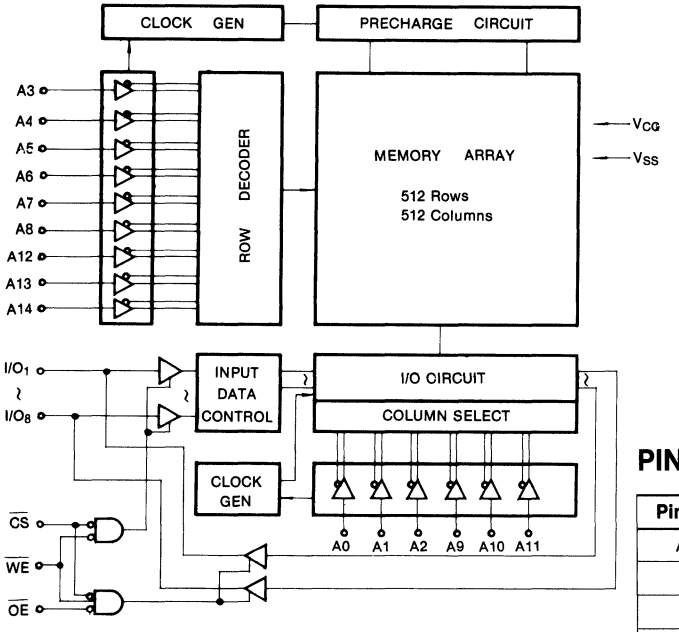
GENERAL DESCRIPTION

The KM68257 is a 262,144-bit high speed Static Random Access Memory organized as 32,767 words by 8 bits. The device is fabricated using Samsung's advanced CMOS process.

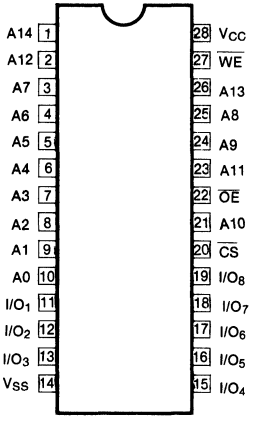
The KM68257 has an output enable input for precise control of the data outputs. It also has a chip enable input for the minimum current power down mode.

The KM68257 has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back up for nonvolatility is required.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

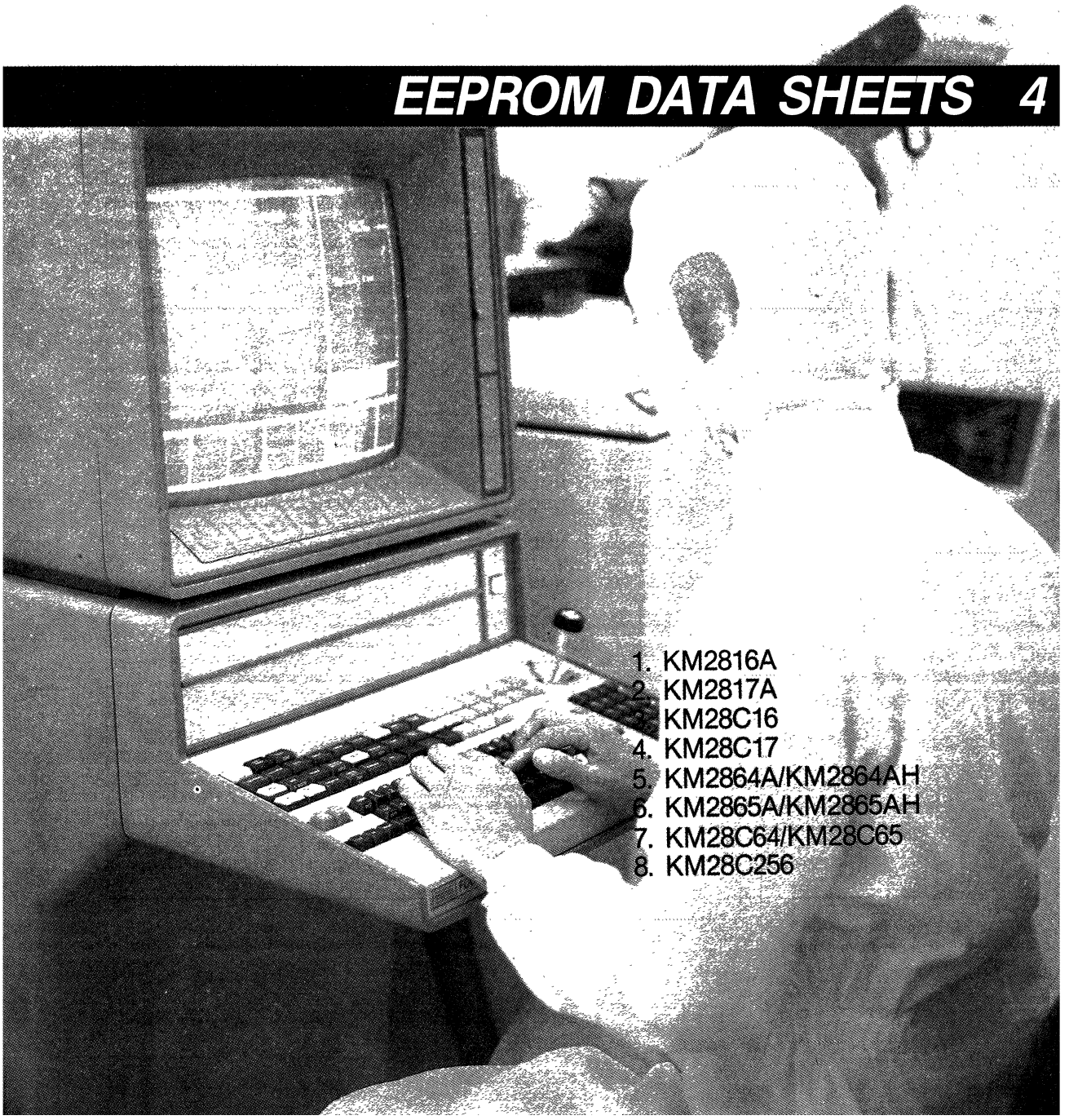


PIN NAMES

Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground

NOTES

EEPROM DATA SHEETS 4



1. KM2816A
2. KM2817A
3. KM28C16
4. KM28C17
5. KM2864A/KM2864AH
6. KM2865A/KM2865AH
7. KM28C64/KM28C65
8. KM28C256

EEPROM

Capacity	Part Number	Organization	Speed (ns)	Technology	Write Cycle Time (min) (ms)	Features	Packages	Remark
16K bit	KM2816A-25	2K × 8	250	NMOS	10	—	24-Pin DIP	Now
	KM2816A-30	2K × 8	300	NMOS	10	—	24-Pin DIP	Now
	KM2816A-35	2K × 8	350	NMOS	10	—	24-Pin DIP	Now
	KM2817A-25	2K × 8	250	NMOS	10	Ready/$\overline{\text{Busy}}$	28-Pin DIP	Now
	KM2817A-30	2K × 8	300	NMOS	10	Ready/$\overline{\text{Busy}}$	28-Pin DIP	Now
	KM2817A-35	2K × 8	350	NMOS	10	Ready/$\overline{\text{Busy}}$	28-Pin DIP	Now
	†KM28C16-15	2K × 8	150	CMOS	2	Ready/$\overline{\text{Busy}}$	24-Pin DIP	under development
	†KM28C16-20	2K × 8	200	CMOS	2	Ready/$\overline{\text{Busy}}$	24-Pin DIP	under development
	†KM28C16-25	2K × 8	250	CMOS	2	Ready/$\overline{\text{Busy}}$	24-Pin DIP	under development
	†KM28C17-15	2K × 8	150	CMOS	2	Ready/$\overline{\text{Busy}}$	28-Pin DIP	under development
	†KM28C17-20	2K × 8	200	CMOS	2	Ready/$\overline{\text{Busy}}$	28-Pin DIP	under development
	†KM28C17-25	2K × 8	250	CMOS	2	Ready/$\overline{\text{Busy}}$	28-Pin DIP	under development
64K bit	KM2864A-20	8K × 8	200	NMOS	10	$\overline{\text{Data}}$ Polling	28-Pin DIP	Now
	KM2864A-25	8K × 8	250	NMOS	10	$\overline{\text{Data}}$ Polling	28-Pin DIP	Now
	KM2864A-30	8K × 8	300	NMOS	10	$\overline{\text{Data}}$ Polling	28-Pin DIP	Now
	KM2865A-20	8K × 8	200	NMOS	10	$\overline{\text{Data}}$ Polling, Ready/$\overline{\text{Busy}}$	28-Pin DIP	Now
	KM2865A-25	8K × 8	250	NMOS	10	$\overline{\text{Data}}$ Polling, Ready/$\overline{\text{Busy}}$	28-Pin DIP	Now
	KM2865A-30	8K × 8	300	NMOS	10	$\overline{\text{Data}}$ Polling, Ready/$\overline{\text{Busy}}$	28-Pin DIP	Now
	KM2864AH-20	8K × 8	200	NMOS	2	$\overline{\text{Data}}$ Polling	28-Pin DIP	Now
	KM2864AH-25	8K × 8	250	NMOS	2	$\overline{\text{Data}}$ Polling	28-Pin DIP	Now
	KM2864AH-30	8K × 8	300	NMOS	2	$\overline{\text{Data}}$ Polling	28-Pin DIP	Now
	KM2865AH-20	8K × 8	200	NMOS	2	$\overline{\text{Data}}$ Polling, Ready/$\overline{\text{Busy}}$	28-Pin DIP	Now
	KM2865AH-25	8K × 8	250	NMOS	2	$\overline{\text{Data}}$ Polling, Ready/$\overline{\text{Busy}}$	28-Pin DIP	Now
	KM2865AH-30	8K × 8	300	NMOS	2	$\overline{\text{Data}}$ Polling, Ready/$\overline{\text{Busy}}$	28-Pin DIP	Now
	KM28C64-20	8K × 8	200	CMOS	5	$\overline{\text{Data}}$ Polling, Page Mode	28-Pin DIP	Now
	KM28C64-25	8K × 8	250	CMOS	5	$\overline{\text{Data}}$ Polling, Page Mode	28-Pin DIP	Now
	KM28C65-20	8K × 8	200	CMOS	5	Ready/$\overline{\text{Busy}}$, Page Mode	28-Pin DIP	Now
	KM28C65-25	8K × 8	250	CMOS	5	Ready/$\overline{\text{Busy}}$, Page Mode	28-Pin DIP	Now
256K	††KM28C256-15	32K × 8	130	CMOS	5	$\overline{\text{Data}}$ Polling, Toggle bit	28-Pin DIP	under development
	††KM28C256-20	32K × 8	200	CMOS	5	$\overline{\text{Data}}$ Polling, Toggle bit	28-Pin DIP	under development
	††KM28C256-25	32K × 8	250	CMOS	5	$\overline{\text{Data}}$ Polling, Toggle bit	28-Pin DIP	under development

† New Product
††Under Development

2K x 8 Bit EEPROM with Latches and Auto-Write

FEATURES

- **Simple Byte Write**
  - **— Single TTL Level Write Signal**
  - **— Latched Address and Data**
  - **— Automatic Internal Erase-before-Write**
  - **— Automatic Write Timing**
- **Enhanced Write Protection**
- **Single 5 volt Supply**
- **Byte Write: 10ms max**
- **Fast Access Time: 250ns**
- **Power: 50mA—Standby (max)**
  110mA—Operating (max)
- **Two Line Control-Eliminates Bus Contention**
- **10,000 Cycle Endurance**
- **JEDEC Byte-wide Memory Pinout**

GENERAL DESCRIPTION

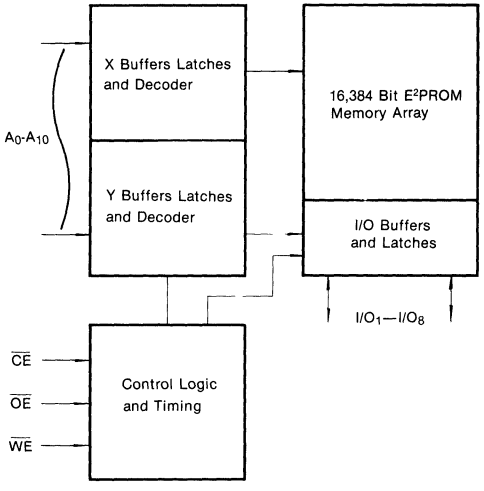
The KM2816A is a 16,384 bit Electrically Erasable and Programmable Read-Only-Memory organized as 2,048 words by 8-bits. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

Writing data into the KM2816A is very simple. The internally self-timed write cycle latches both address and data to provide a free system bus during the 10ms (max) write period.

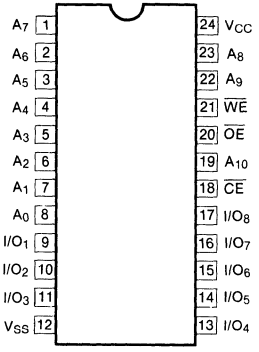
The KM2816A is fabricated with the well defined floating gate NMOS technology using Fowler-Nordheim tunneling for erasing and programming.

4

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{10}	Address Inputs
I/O_1—I/O_8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}	−1 to +7.0	V
Temperature Under Bias	T_{bias}	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Short Circuit Output Current	I_{OS}	5	mA

*NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltages referenced to V_{SS}, $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	$V_{CC}+1$	V
Input Low Voltage	V_{IL}	−1	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Max	Units
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$ All I/O's = OPEN Other Inputs = V_{CC}	—	110	mA
Standby Current	I_{SB}	$\overline{CE} = V_{IH}$ All I/O's = OPEN Other Inputs = V_{CC}	—	50	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Output High Voltage Level	V_{OH}	$I_{OH} = -400$ μA	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1$ mA	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.5	—	V

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, $f = 1.0$ MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

($T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0 to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and $C_L = 100$ pF

READ CYCLE

Parameter	Symbol	KM2816A-25		KM2816A-30		KM2816A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	250		300		350		ns
Chip Enable Access Time	t_{CE}		250		300		350	ns
Address Access Time	t_{AA}		250		300		350	ns
Output Enable Access Time	t_{OE}		120		120		120	ns
Chip Enable to Output in Low-Z	t_{LZ}	10		10		10		ns
Chip Disable to Output in High-Z	t_{HZ}	10	100	10	100	10	100	ns
Output Enable to Output in Low-Z	t_{OLZ}	50		50		50		ns
Output Disable to Output in High-Z	t_{OHZ}	10	60	10	80	10	100	ns
Output Hold from Address Change	t_{OH}	20		20		20		ns

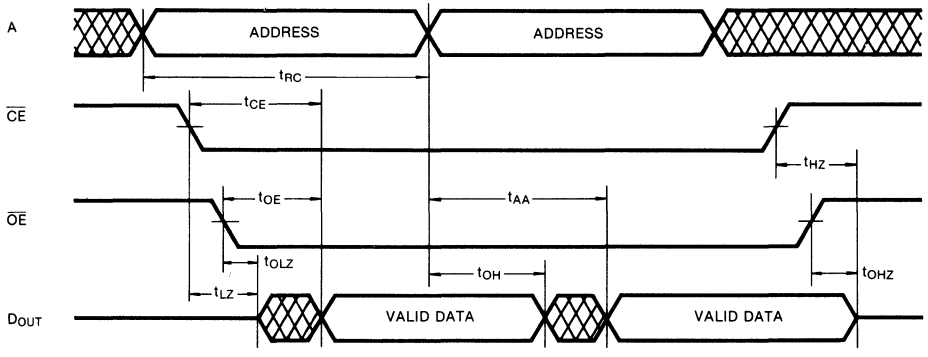
WRITE CYCLE

Parameter	Symbol	Min	Max	Units
Write Cycle Time	t_{WC}	10		ms
Address Set-up Time	t_{AS}	10		ns
Address Hold Time	t_{AH}	70		ns
Write Set-up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
Chip Enable to End of Write Input	t_{CW}	100		ns
Output Enable Set-up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
Write Pulse Width	t_{WP}	100		ns
Data Latch Time	t_{DL}	50		ns
Data Valid Time	t_{DV}		1	μs
Data Set-up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	15		ns

TIMING DIAGRAMS

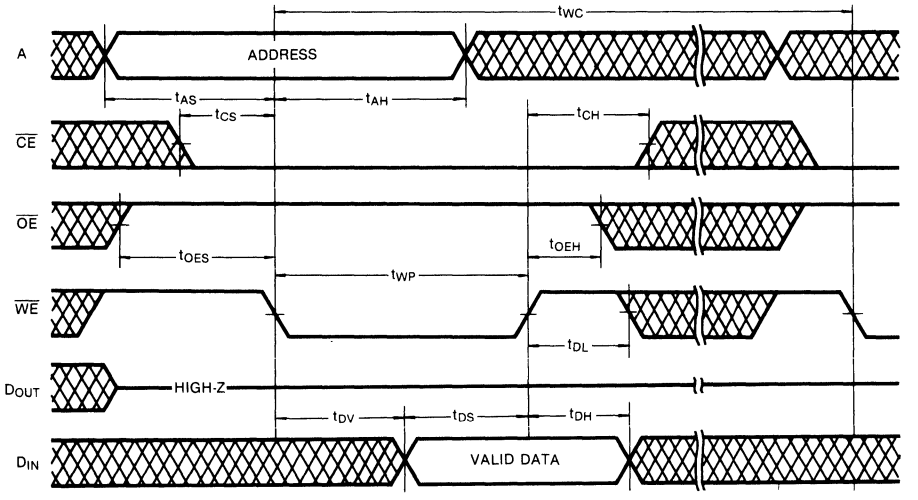
READ CYCLE

$\overline{WE} = V_{IH}$

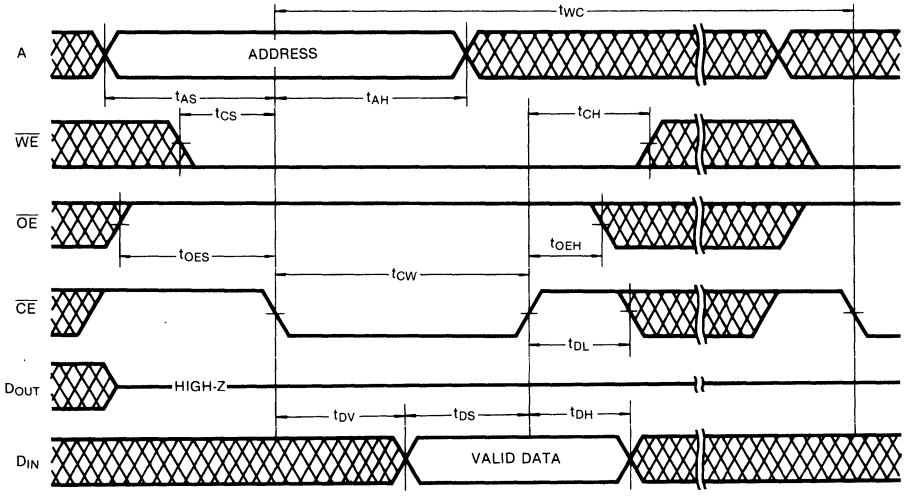


TIMING DIAGRAMS (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE



$\overline{CE}$ CONTROLLED WRITE CYCLE



DEVICE OPERATION

Read

Reading data from the KM2816A is similar to reading data from a static RAM. A read cycle occurs when $\overline{WE}$ is high and both $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high.

Write

Writing data into the KM2816A is very easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a static RAM.
A write cycle occurs when $\overline{OE}$ is high and both $\overline{CE}$ and $\overline{WE}$ are low. The address is latched by the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first. Address and data are conveniently latched in less than 200ns during a write operation. Once a byte write cycle is initiated it will automatically continue to completion within 10 ms or less. The existing data at the selected address is automatically erased and the new data is automatically written.

Standby

Power consumption may be reduced about 60% by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and $I/O_1 - I/O_8$ are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

Data Protection

Features have been designed into the KM2816A that prevent unwanted write cycles during power supply transitions and system noise periods.
Write cycles are inhibited when V_{CC} is less than $V_{WI} = 3.5$ volts, the Write Inhibit V_{CC} level. During power-up the KM2816A automatically prevents any write operation for a period of 9 ms (Typical) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ or $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period.
Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off with inhibit inadvertent writes.

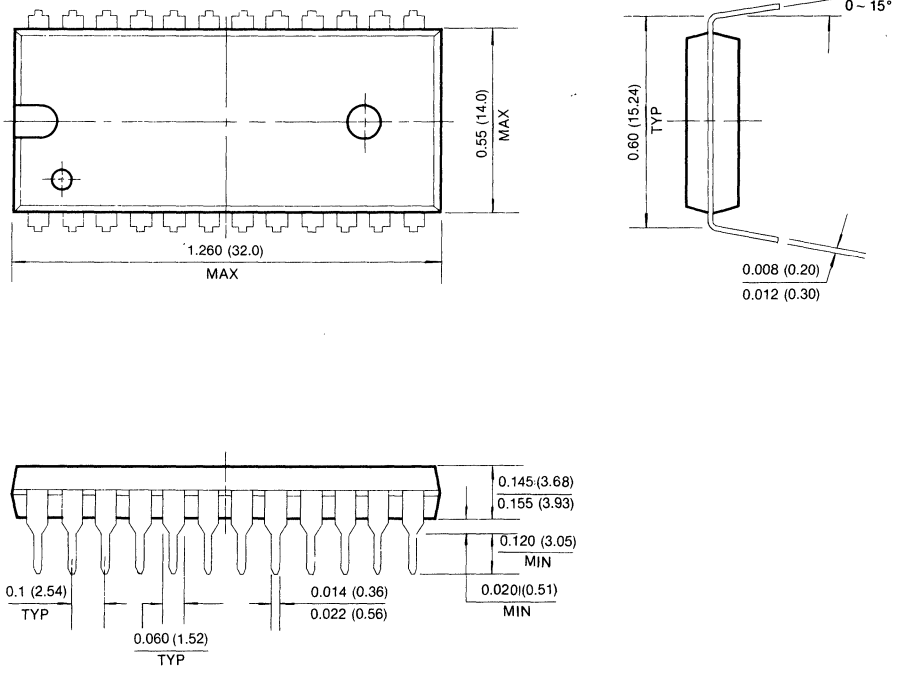
Endurance and Data Retention

The KM2816A is designed for applications requiring, up to 10,000 write cycles per E^2PROM byte and ten years of data retention. This means that each byte may be reliably written 10,000 times without degrading device operation, and that the data in the byte will remain valid after its last write operation for ten years with or without power applied.

PACKAGE DIMENSIONS

24 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



2K x 8 Bit EEPROM with Ready/$\overline{\text{Busy}}$ Function

FEATURES

- **Simple Byte Write**
  - **— Single TTL Level Write Signal**
  - **— Latched Address and Data**
  - **— Automatic Internal Erase-before-Write**
  - **— Automatic Write Timing**
  - **— Ready/$\overline{\text{Busy}}$ Output Pin**
- **Enhanced Write Protection**
- **Single 5 volt Supply**
- **Byte Write: 10ms (max)**
- **Fast Access Time: 250ns**
- **Power: 50mA—Standby (max)**
  110mA—Operating (max)
- **Two Line Control-Eliminates Bus Contention**
- **10,000 Cycle Endurance**
- **JEDEC Byte-wide Memory Pinout**

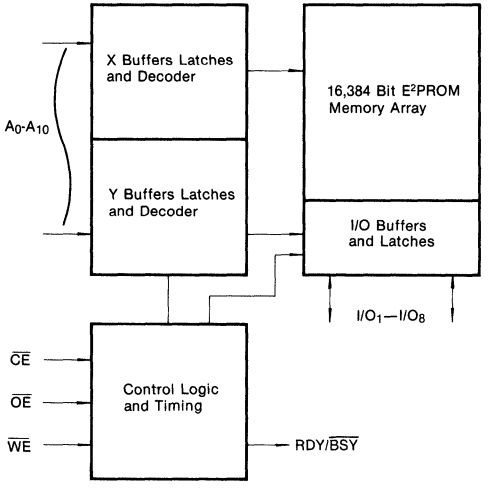
GENERAL DESCRIPTION

The KM2817A is a 16,384 bit Electrically Erasable and Programmable Read-Only-Memory organized as 2,048 words by 8-bits. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

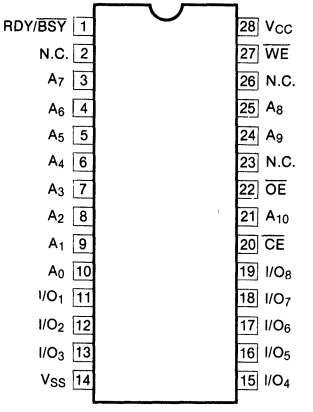
Writing data into the KM2817A is very simple. The internally self-timed write cycle latches both address and data to provide a free system bus during the 10ms (max) write period.

The KM2817A has an open-drain Ready/$\overline{\text{Busy}}$ output on pin 1 which signals when the write operation is complete. This device is fabricated with the well defined floating gate NMOS technology using Flowler-Nordheim tunneling for erasing and programming.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{10}	Address Inputs
I/O_1—I/O_8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BSY}$	Ready/$\overline{\text{Busy}}$ Output
N.C.	No Connection
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}	−1 to +7.0	V
Temperature Under Bias	T_{bias}	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Short Circuit Output Current	I_{OS}	5	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltages referenced to V_{SS}, $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	$V_{CC}+1$	V
Input Low Voltage	V_{IL}	−1	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Max	Units
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$ All I/O's = OPEN Other Inputs = V_{CC}	—	110	mA
Standby Current	I_{SB}	$\overline{CE} = V_{IH}$ All I/O's = OPEN Other Inputs = V_{CC}	—	50	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Output High Voltage Level	V_{OH}	$I_{OH} = -400$ μA	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1$ mA	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.5	—	V

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, $f = 1.0$ MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

($T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0 to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and $C_L = 100$ pF

READ CYCLE

Parameter	Symbol	KM2817A-25		KM2817A-30		KM2817A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	250		300		350		ns
Chip Enable Access Time	t_{CE}		250		300		350	ns
Address Access Time	t_{AA}		250		300		350	ns
Output Enable Access Time	t_{OE}		120		120		120	ns
Chip Enable to Output in Low-Z	t_{LZ}	10		10		10		ns
Chip Disable to Output in High-Z	t_{HZ}	10	100	10	100	10	100	ns
Output Enable to Output in Low-Z	t_{OLZ}	50		50		50		ns
Output Disable to Output in High-Z	t_{OHZ}	10	60	10	80	10	100	ns
Output Hold from Address Change	t_{OH}	20		20		20		ns

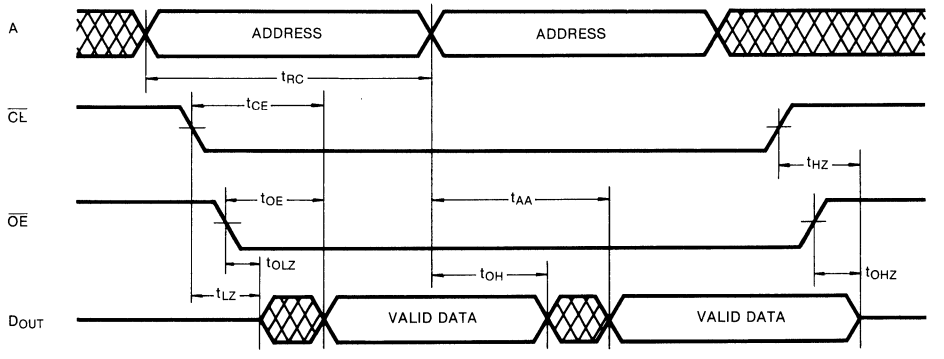
WRITE CYCLE

Parameter	Symbol	Min	Max	Units
Write Cycle Time	t_{WC}	10		ms
Address Set-up Time	t_{AS}	10		ns
Address Hold Time	t_{AH}	70		ns
Write Set-up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
Chip Enable to End of Write Input	t_{CW}	100		ns
Output Enable Set-up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
Write Pulse Width	t_{WP}	100		ns
Data Latch Time	t_{DL}	50		ns
Data Valid Time	t_{DV}		1	μs
Data Set-up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	15		ns
Time to Device Busy	t_{DB}		120	ns
Busy to Write Recovery Time	t_{BWR}	50		ns

TIMING DIAGRAMS

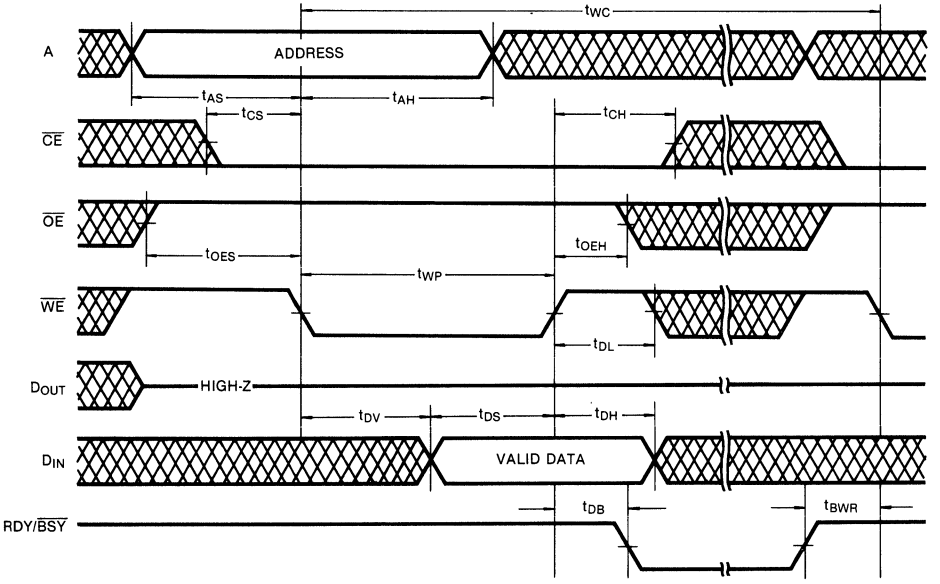
READ CYCLE

$\overline{WE} = V_{IH}$

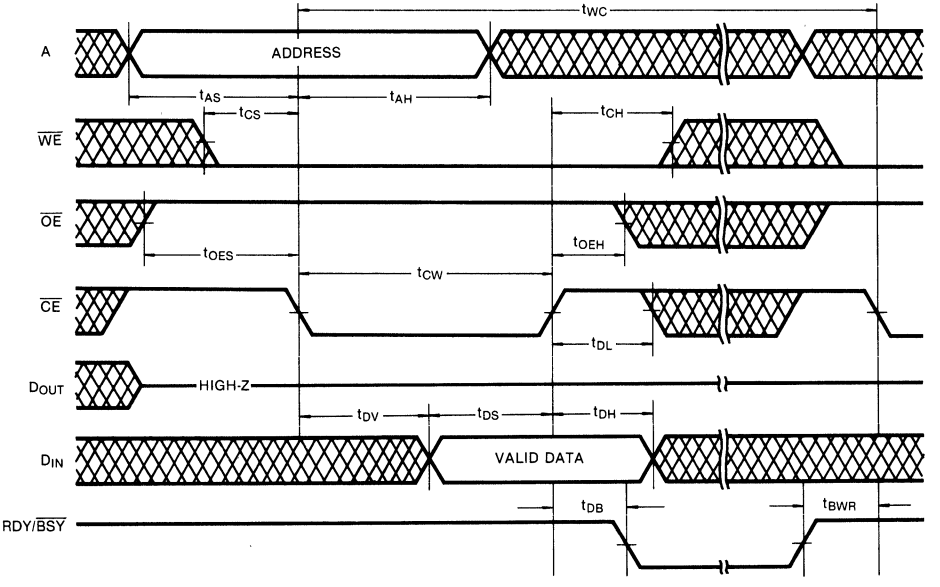


TIMING DIAGRAMS (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE



$\overline{CE}$ CONTROLLED WRITE CYCLE



DEVICE OPERATION

Read

Reading data from the KM2817A is similar to reading data from a static RAM. A read cycle occurs when $\overline{WE}$ is high and both $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high.

Write

Writing data into the KM2817A is very easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a static RAM.
A write cycle occurs when $\overline{OE}$ is high and both $\overline{CE}$ and $\overline{WE}$ are low. The address is latched by the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first. Address and data are conveniently latched in less than 200ns during a write operation. Once a byte write cycle is initiated,it will automatically continue to completion within 10 ms or less. The existing data at the selected address is automatically erased and the new data is automatically written.

Standby

Power consumption may be reduced about 60% by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and $I/O_1 - I/O_8$ are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

Data Protection

Features have been incorporated into the KM2817A design that prevent unwanted write cycles during power supply transitions and system noise periods.

Write cycles are inhibited when V_{CC} is less than 3.5 volts, the Write Inhibit V_{CC} level. During power-up the KM2817A automatically prevents any write operation for a period of 9 ms (Typical) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ or $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period.
Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off with inhibit inadvertent writes.

Ready/$\overline{Busy}$

The KM2817A has a Ready/$\overline{Busy}$ output pin that indicates when the write cycle is complete. The pin is normally high except when a nonvolatile write cycle is in progress, in which case the pin is low.
The Ready/$\overline{Busy}$ output is configured as open-drain driver there-by allowing two or more Ready/$\overline{Busy}$ output to be or-tied. This pin requires an appropriate pull-up register for proper operation. The pull-up resistor value for the Ready/$\overline{Busy}$ output maybe calculated as follows:

$$R_p = \frac{V_{CC}\,(MAX) - V_{OL}\,(MAX)}{I_{OL} + I_L} = \frac{5.1V}{2.1mA + I_L}$$

Where I_L is the sum of the input currents of all devices tied to the Ready/$\overline{Busy}$ pin.

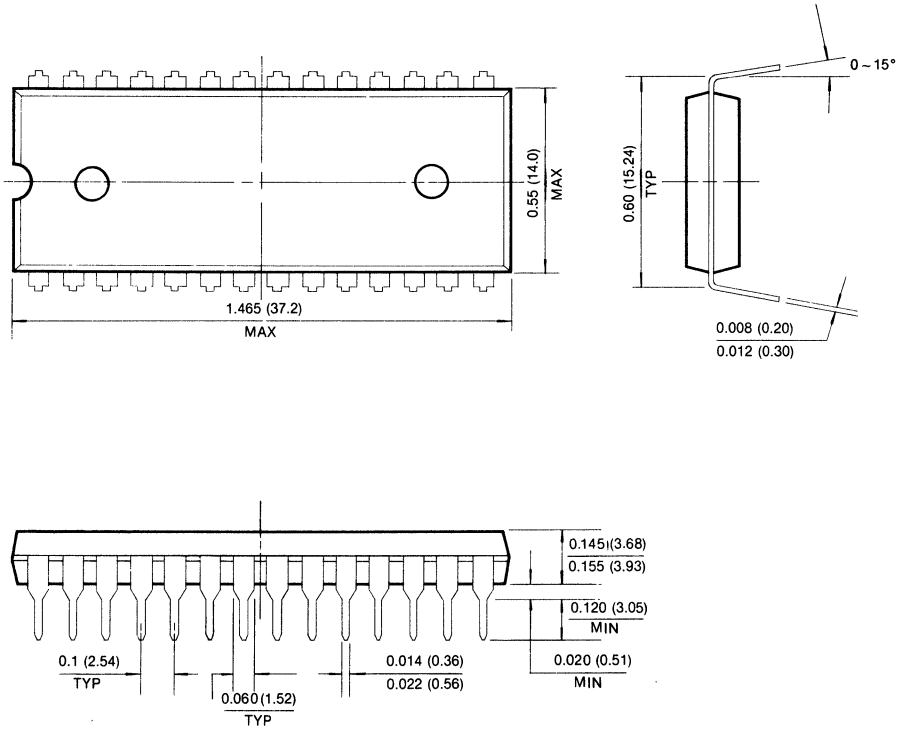
Endurance and Data Retention

The KM2817A is designed for applications requiring, up to 10,000 write cycles per E²PROM byte and ten years of data retention. This means that each byte may be reliably written 10,000 times without degrading device operation, and that the data in the byte will remain valid after its last rewrite operation for ten years with or without power applied.

PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



2K x 8 CMOS Electrically Erasable PROM

FEATURES

- **Simple Byte Write**
  - **Single TTL Level Write Signal**
  - **Latched Address and Data**
  - **Automatic Internal Erase-Before-Write**
  - **Automatic Write Timing**
  - **$\overline{\text{DATA}}$ Polling and Verification**
- **32-byte page Write 2ms max**
  - **Effective 62.5μs/byte write**
- **Enhanced Write Protection**
- **Single 5 volt Supply**
- **Fast Access Time: 150ns**
- **Power: 100μA—Standby (max)**
  30mA—Operating (max)
- **Two Line Control-Eliminates Bus Contention**
- **10,000 Cycle Endurance**
- **JEDEC Byte-wide Memory Pinput**

GENERAL DESCRIPTION

The KM28C16 is a 2,048 x 8 bit electrically erasable and programmable read-only-memory. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

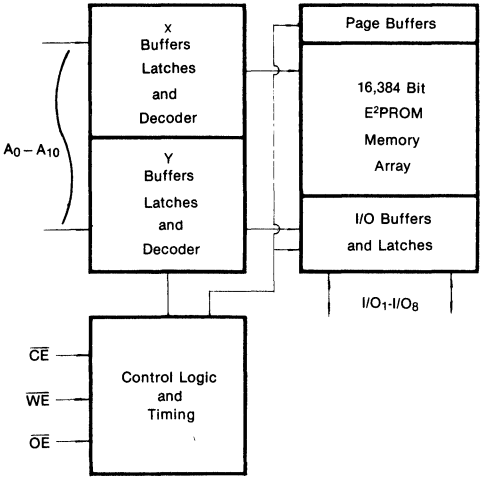
Writing data into the KM28C16 is very simple. The internally self-timed write cycle latches both address and data to provide a free system bus during the 2ms (max) write period.

A 32-byte page write enables an entire chip written in 128ms.

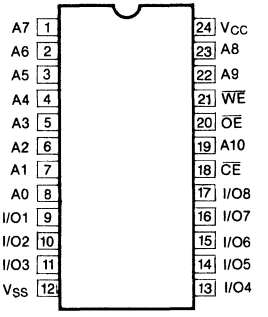
The KM28C16 features $\overline{\text{DATA}}$-polling, which enables the EEPROM to signal the processor that a write operation is complete without requiring the use of any external hardware.

The KM28C16 is fabricated with the well defined floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
I/O_1-I/O_8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5V
V_{SS}	Ground

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Short Circuit Output Current	I_{OS}	5	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage, all Inputs	V_{IH}	2.0	—	$V_{CC}+0.3$	V
Input Low Voltage, all Inputs	V_{IL}	−0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ All I/O's = OPEN All Addresses* (note 1)	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$ All I/O's = OPEN		1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} \geq V_{CC} - 0.2$ All I/O's = OPEN	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.5	—	V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 5MHz

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, f = 1.0 MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	6	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	10	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{DATA}$-Polling	$I/O_8 = \overline{D}_8$	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS ($T_A = 0°C$ to $70°C$ $V_{CC} = 5V \pm 10\%$, unless otherwise noted).

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	20 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM28C16-15		KM28C16-20		KM28C16-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{CE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		60		80		100	ns
Chip Enable to Output in Low-Z	t_{LZ}	0		0		0		ns
Chip Disable to Output in High-Z	t_{HZ}	5	50	5	70	5	90	ns
Output Enable to Output in Low-Z	t_{OLZ}	5		5		5		ns
Output Disable to Output in High-Z	t_{OHZ}	5	50	5	70	5	90	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

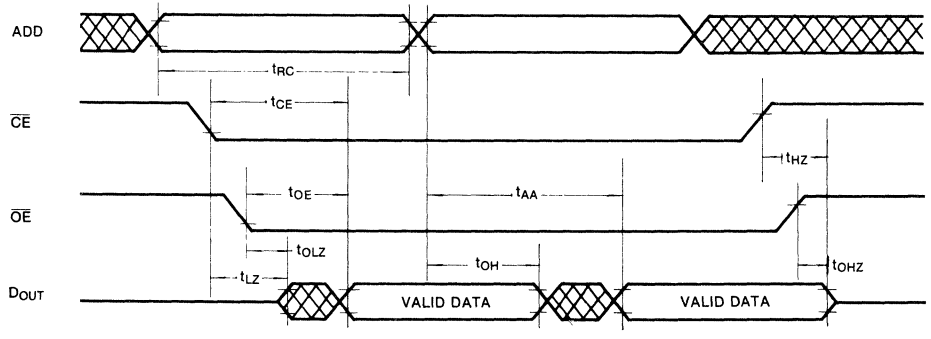
WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}	2		ms
Address Set-Up Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	80		ns
Write Set-Up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
Chip Enable to End of Write Input	t_{CW}	100		ns
Output Enable Set-Up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
Write Pulse Width	t_{WP}	100		ns
Data Set-Up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	10		ns
Byte Load Cycle	t_{BLC}	0.2	100	μs

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and starts at a rising edge of $\overline{WE}$.

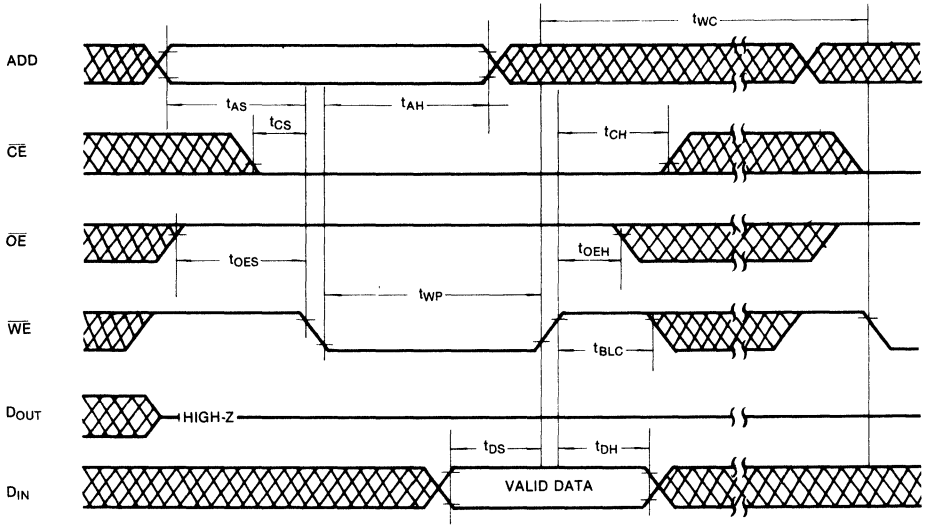
TIMING DIAGRAMS

READ CYCLE $\overline{WE} = V_{IH}$

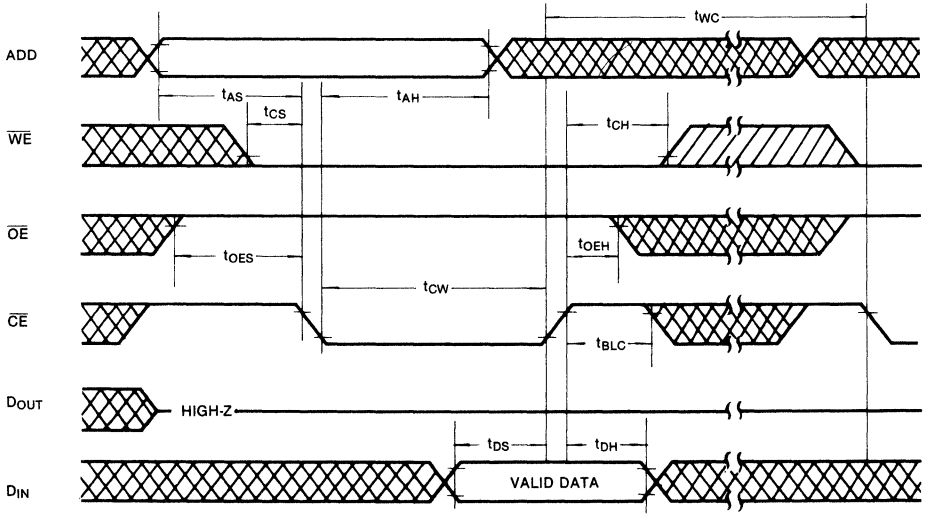


TIMING DIAGRAMS (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE

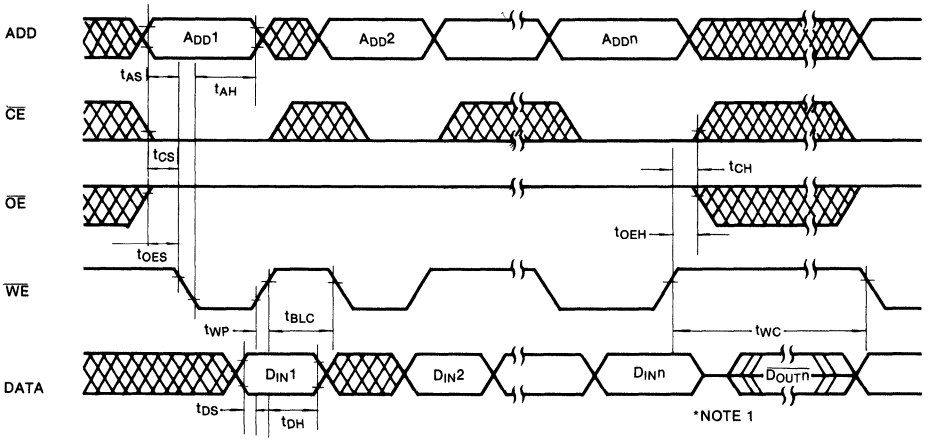


$\overline{CE}$ CONTROLLED WRITE

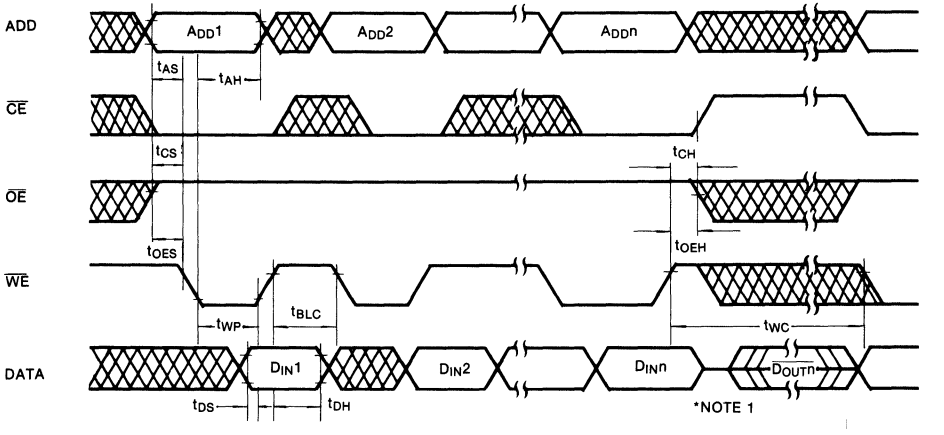


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE ($\overline{WE}$ CONTROLLED WRITE CYCLE)



PAGE MODE WRITE ($\overline{CE}$ CONTROLLED WRITE CYCLE)



*NOTE 1. Tristate for I/O_1-I/O_7, $\overline{D_{OUTn}}$ for I/O_8 if the chip is read. (See $\overline{Data}$-polling)

DEVICE OPERATION

READ

Reading data from the KM28C16 is similar to reading data from a SRAM. A read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

WRITE

Writing data into the KM28C16 is very easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write mode of the KM28C16 is only a part of the page write mode. A single byte data loading followed by a t_{BLC} time-out and by a nonvolatile write cycle will complete a byte mode write. In this mode, the write is exactly identical to that of the KM2816A.

**** PAGE WRITE MODE ****

The KM28C16 allows up to 32 byte to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 32 byte data are loaded into the KM28C16 internal registers and a nonvolatile write period, in which the loaded data in the registers are written to the EEPROM cells of the selected page.

Data are loaded into the KM28C16 by sequentially pulsing $\overline{WE}$ with $\overline{CE}$ low and $\overline{OE}$ high. ON each $\overline{WE}$, address is latched on the falling edge of the $\overline{WE}$ and data is latched on the rising edge of the $\overline{WE}$. The data can be loaded in any "Y" address order and can be renewed in a data loading period.

Since the timer for the data loading period (t_{BLC}) is reset at the falling edge of $\overline{WE}$ and starts at every rising edge of $\overline{WE}$, the only requirement on $\overline{WE}$ to continue the data loading is that the interval between $\overline{WE}$ pulses does not exceed the maximum t_{BLC} (100μs). If $\overline{OE}$ goes Low during the data loading period, further attempt to load the data will be ignored because the external $\overline{WE}$ signal is blocked by $\overline{OE}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{WE}$ pulse if $\overline{OE}$ is low.

The page address for the nonvolatile write is the "X" address (A5-A10) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase cycle and a program cycle. During the erase cycle, the existing data of the locations being addressed are erased. The new data latched at the register are written into the locations during the program cycle. Note that only the addressed location in a page are rewritten during a page write cycle.

The KM28C16 also supports $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch address and data as well as $\overline{WE}$.

STANDBY

Power consumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and I/O_1-I/O_8 are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM28C16 that prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C16 has a protection feature against $\overline{WE}$ noises: a $\overline{WE}$ noise the width shorter than 20ns (typ.) will not start any unwanted write cycle.
Write cycles are also inhibited when V_{CC} is less than $V_{WI} = 3.5$ volts, the Write Inhibits V_{CC} level.
During power-up, the KM28C16 automatically prevents any write operation for a period of 2ms (typ.) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ and $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit inadvertent writes.

$\overline{DATA}$ POLLING

The KM28C16 features $\overline{DATA}$-Polling at I/O_8 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not require any external hardware. Reading the device at any time during a write operation will produce, at I/O_8, an inverted vale of last data loaded in to the EEPROM (I/O_1-I/O_7 are at the high impedance state). True data will be produced at all I/O's once the write cycle has been completed.

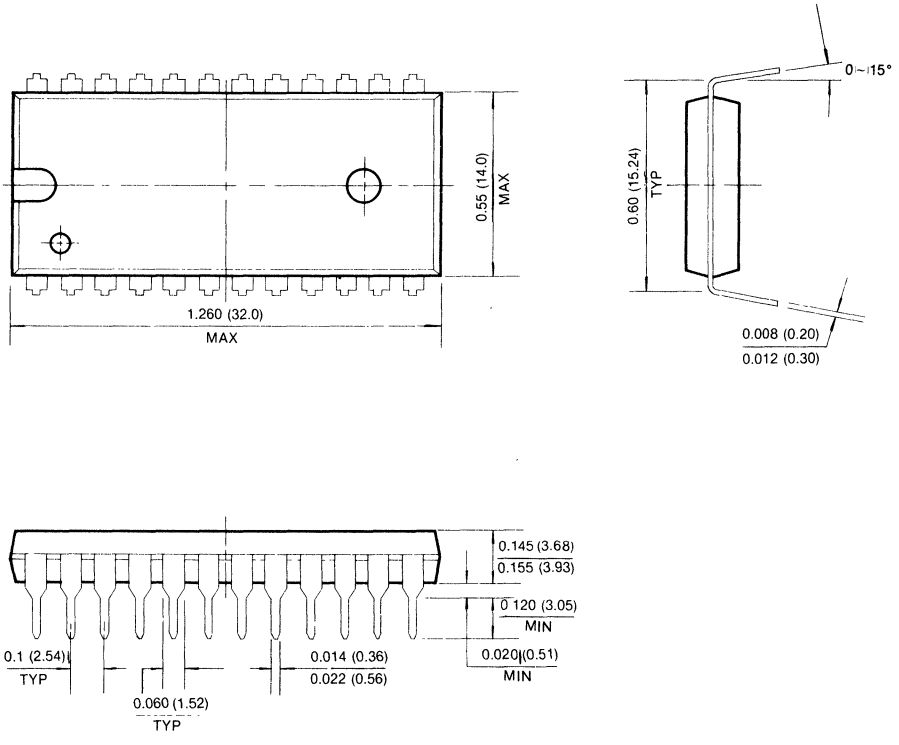
ENDURANCE AND DATA RETENTION

KM28C16 is designed for applications requiring up to 10,000 write cycles per EEPROM byte and ten years of data retention. This means that each byte may be reliably written 10,000 times without degrading device operation and that the data in the byte will remain valid after its last write operation for ten years with or without power applied.

PACKAGE DIMENSIONS

24 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



2K x 8 CMOS Electrically Erasable PROM

FEATURES

- **Simple Byte Write**
  - **Single TTL Level Write Signal**
  - **Latched Address and Data**
  - **Automatic Internal Erase-Before-Write**
  - **Automatic Write Timing**
  - **$\overline{\text{DATA}}$ Polling and Verification**
  - **Ready/$\overline{\text{Busy}}$ Output Pin (KM28C17)**
- **32-byte page Write 2ms max**
  - **Effective 62.5μs/byte write**
- **Enhanced Write Protection**
- **Single 5 volt Supply**
- **Fast Access Time: 150ns**
- **Power: 100μA—Standby (max)**
  30mA—Operating (max)
- **Two Line Control-Eliminates Bus Contention**
- **10,000 Cycle Endurance**
- **JEDEC Byte-wide Memory Pinput**

GENERAL DESCRIPTION

The KM28C17 is a 2,048 x 8 bit electrically erasable and programmable read-only-memory. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

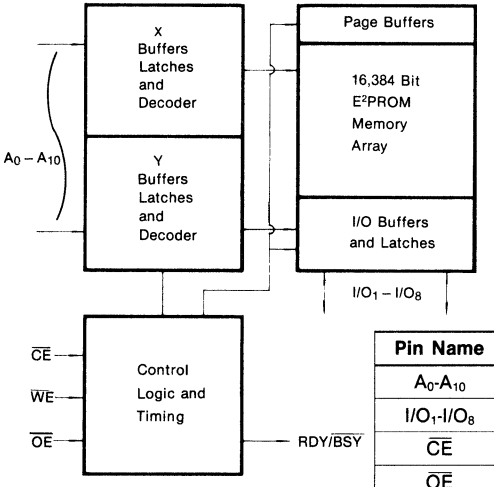
Writing data into the KM28C17 is very simple. The internally self-timed write cycle latches both address and data to provide a free system bus during the 2ms (max) write period.

A 32-byte page write enables an entire chip written in 128ms.

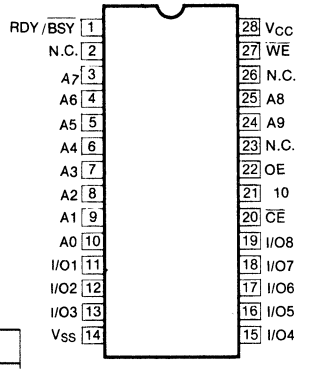
The KM28C17 features $\overline{\text{DATA}}$-polling, which enables the EEPROM to signal the processor that a write operation is complete without requiring the use of any external hardware. Ready/$\overline{\text{Busy}}$ is a hardware scheme in which Pin 1 is used to signal the status of the write operation and is especially useful in interrupt driven systems.

The KM28C17 is fabricated with the well defined floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{10}	Address Inputs
I/O_1-I/O_8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BSY}$	Ready/$\overline{Busy}$ Output
N.C.	No Connection
V_{CC}	+5V
V_{SS}	Ground

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Short Circuit Output Current	I_{OS}	5	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage, all Inputs	V_{IH}	2.0	—	$V_{CC}+0.3$	V
Input Low Voltage, all Inputs	V_{IL}	−0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ All I/O's = OPEN All Addresses* (note 1)	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$ All I/O's = OPEN		1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} \geq V_{CC} - 0.2$ All I/O's = OPEN	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.5	—	V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 5MHz

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, f = 1.0 MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	6	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	10	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{DATA}$-Polling	$I/O_8 = \overline{D}_8$	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted).

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	20 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM28C17-15		KM28C17-20		KM28C17-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{CE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		60		80		100	ns
Chip Enable to Output in Low-Z	t_{LZ}	0		0		0		ns
Chip Disable to Output in High-Z	t_{HZ}	5	50	5	70	5	90	ns
Output Enable to Output in Low-Z	t_{OLZ}	5		5		5		ns
Output Disable to Output in High-Z	t_{OHZ}	5	50	5	70	5	90	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

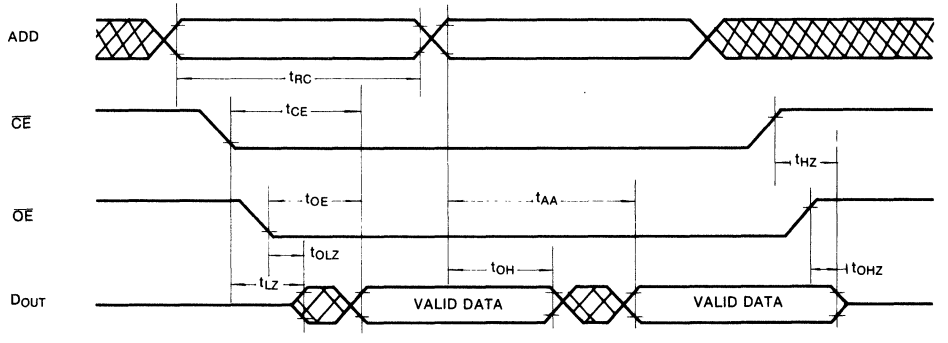
WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}	2		ms
Address Set-Up Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	80		ns
Write Set-Up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
Chip Enable to End of Write Input	t_{CW}	100		ns
Output Enable Set-Up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
Write Pulse Width	t_{WP}	100		ns
Data Set-Up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	10		ns
Time to Device Busy	t_{DB}		100	ns
Busy to Write Recovery Time	t_{BWR}	50		ns
Byte Load Cycle	t_{BLC}	0.2	100	μs

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and starts at a rising edge of $\overline{WE}$.

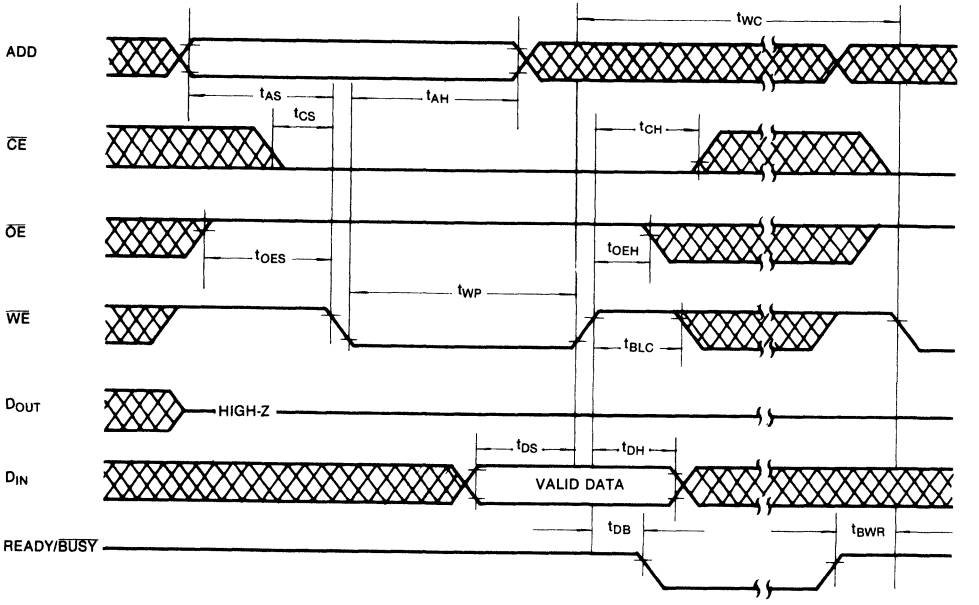
TIMING DIAGRAMS

READ CYCLE $\overline{WE} = V_{IH}$

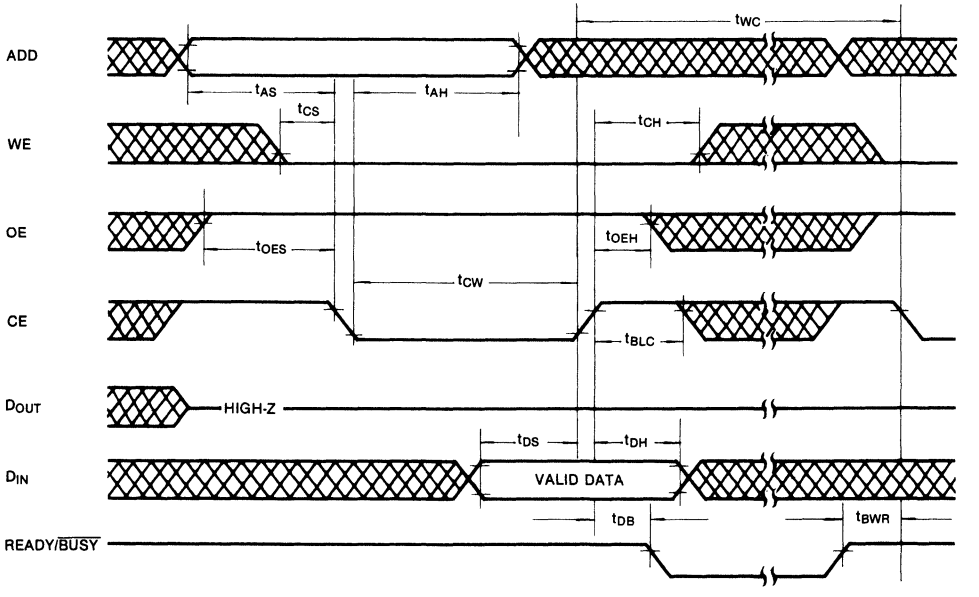


TIMING DIAGRAMS (Continued)

WE CONTROLLED WRITE CYCLE

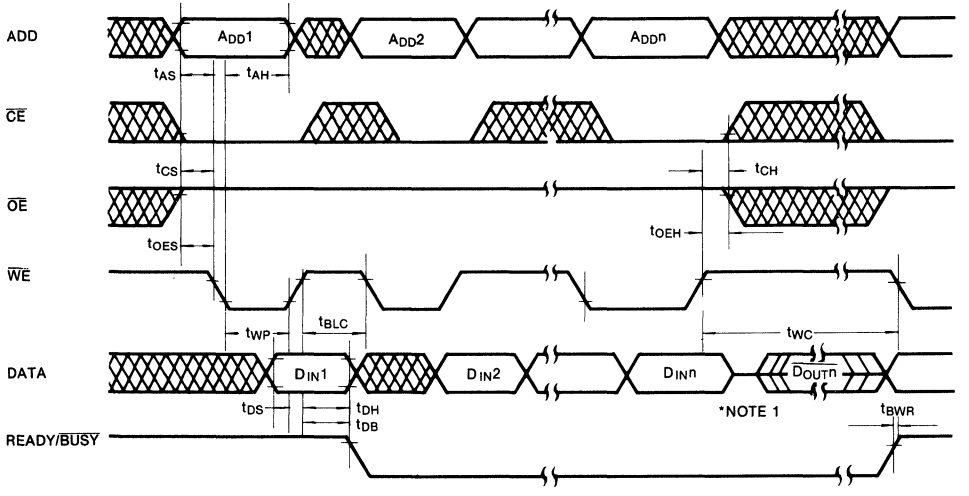


CE CONTROLLED WRITE

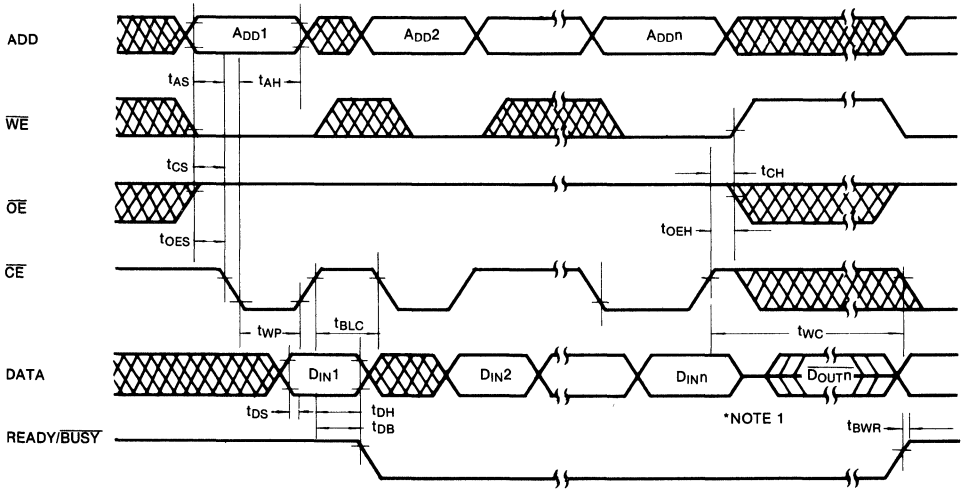


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE ($\overline{WE}$ CONTROLLED WRITE CYCLE)



PAGE MODE WRITE ($\overline{CE}$ CONTROLLED WRITE CYCLE)



*NOTE 1. Tristate for I/O_1-I/O_7, $\overline{D_{OUTn}}$ for I/O_8 if the chip is read. (See $\overline{Data}$-polling)

DEVICE OPERATION

READ

Reading data from the KM28C17 is similar to reading data from a SRAM. A read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

WRITE

Writing data into the KM28C17 is very easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write mode of the KM28C17 is only a part of the page write mode. A single byte data loading followed by a t_{BLC} time-out and by a nonvolatile write cycle will complete a byte mode write. In this mode, the write is exactly identical to that of the KM2817A.

**** PAGE WRITE MODE ****

The KM28C17 allows up to 32 byte to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 32 byte data are loaded into the KM28C17 internal registers and a nonvolatile write period, in which the loaded data in the registers are written to the EEPROM cells of the selected page.

Data are loaded into the KM28C17 by sequentially pulsing $\overline{WE}$ with $\overline{CE}$ low and $\overline{OE}$ high. ON each $\overline{WE}$, address is latched on the falling edge of the $\overline{WE}$ and data is latched on the rising edge of the $\overline{WE}$. The data can be loaded in any "Y" address order and can be renewed in a data loading period.

Since the timer for the data loading period (t_{BLC}) is reset at the falling edge of $\overline{WE}$ and starts at every rising edge of $\overline{WE}$, the only requirement on $\overline{WE}$ to continue the data loading is that the interval between $\overline{WE}$ pulses does not exceed the maximum t_{BLC} (100μs). If $\overline{OE}$ goes Low during the data loading period, further attempt to load the data will be ignored because the external $\overline{WE}$ signal is blocked by $\overline{OE}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{WE}$ pulse if $\overline{OE}$ is low.

The page address for the nonvolatile write is the "X" address (A5-A10) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase cycle and a program cycle. During the erase cycle, the existing data of the locations being addressed are erased. The new data latched at the register are written into the locations during the program cycle. Note that only the addressed location in a page are rewritten during a page write cycle.

The KM28C17 also supports $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch address and data as well as $\overline{WE}$.

STANDBY

Power consumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and I/O_1-I/O_8 are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM28C17 that prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C17 has a protection feature against $\overline{WE}$ noises: a $\overline{WE}$ noise the width shorter than 20ns (typ.) will not start any unwanted write cycle.
Write cycles are also inhibited when V_{CC} is less than V_{WI} = 3.5 volts, the Write Inhibits V_{CC} level.
During power-up, the KM28C17 automatically prevents any write operation for a period of 2ms (typ.) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ and $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit inadvertent writes.

$\overline{DATA}$ POLLING

The KM28C17 features $\overline{DATA}$-Polling at I/O_8 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not require any external hardware. Reading the device at any time during a write operation will produce, at I/O_8, an inverted value of last data loaded in to the EEPROM (I/O_1-I/O_7 are at the high impedance state). True data will be produced at all I/O's once the write cycle has been completed.

DEVICE OPERATION

READY/$\overline{BUSY}$

The KM28C17 has a Ready/$\overline{Busy}$ output on pin 1 that indicates when the write cycle is complete. The pin is normally high except when a write cycle is in progress in which case the pin is low.

The Ready/$\overline{Busy}$ output is configured as open-drain driver there-by allowing two or more Ready/$\overline{Busy}$ output to be OR-tied. This pin requires an appropriate pull-up resistor for proper operation. The pull-up resistor value maybe calculated as follows.

$$RP = \frac{V_{CC}(max) - V_{OL}(max)}{I_{OL} + I_L} = \frac{5.1V}{2.1mA + I_L}$$

where I_L is the sum of the input currents of all devices tied to the Ready/$\overline{Busy}$ pin.

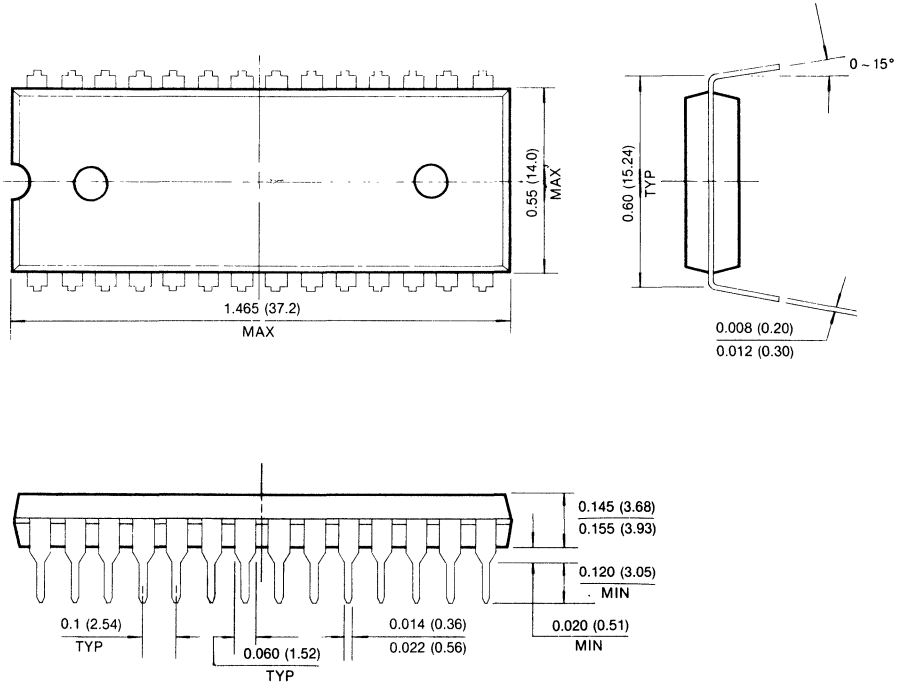
ENDURANCE AND DATA RETENTION

KM28C17 is designed for applications requiring up to 10,000 write cycles per EEPROM byte and ten years of data retention. This means that each byte may be reliably written 10,000 times without degrading device operation and that the data in the byte will remain valid after its last write operation for ten years with or without power applied.

PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



8K x 8 Bit EEPROM with Latches and Auto-Write

FEATURES

- **Simple Byte Write**
  - **Single TTL Level Write Signal**
  - **Latched Address and Data**
  - **Automatic Internal Erase-before-Write**
  - **Automatic Write Timing**
  - **$\overline{\text{DATA}}$ Polling and Verification**
- **Enhanced Write Protection**
- **Single 5 volt Supply**
- **Byte Write: 10ms (max)—KM2864A**
  2ms (max)—KM2864AH
- **Fast Access Time: 200ns**
- **Power: 50mA—Standby (max)**
  120mA—Operating (max)
- **Two Line Control-Eliminates Bus Contention**
- **10,000 Cycle Endurance**
- **JEDEC Byte-wide Memory Pinout**

GENERAL DESCRIPTION

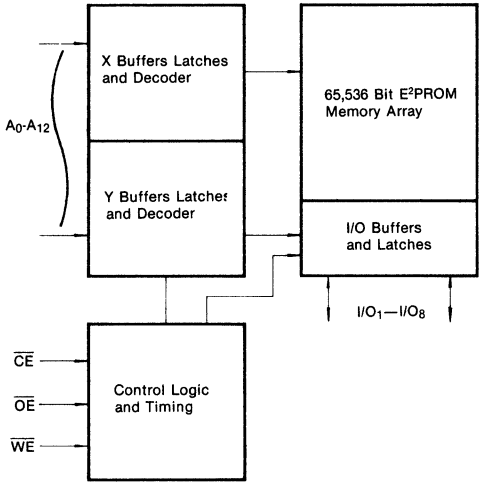
The KM2864A/AH is a 65,536 bit Electrically Erasable and Programmable Read-Only-Memory organized as 8,192 words by 8-bits. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

Writing data into the KM2864A/AH is very simple. The internally self-timed write cycle latches both address and data to provide a free system bus during the write period which is 10ms (max) for the KM2864A or 2ms (max) for the KM2864AH.

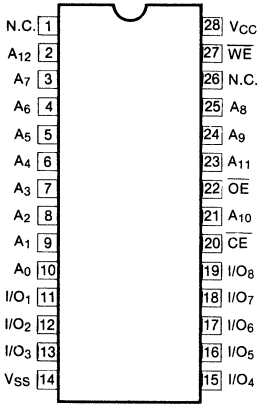
The KM2864A/AH features $\overline{\text{DATA}}$ Polling, a software scheme to detect the early completion of a write cycle without requiring the use of any additional external hardware. The KM2864A/AH is fabricated with the well defined floating gate NMOS technology using Fowler-Nordheim tunneling for erasing and programming.

4

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{12}	Address Inputs
I/O_1—I/O_8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
N.C.	No Connection
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}	−1 to +6.0	V
Temperature Under Bias	T_{bias}	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Short Circuit Output Current	I_{OS}	5	mA

*NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltages referenced to V_{SS}, $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	−1	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Max	Units
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$ All I/O's = OPEN Other Inputs = V_{CC}	—	120	mA
Standby Current	I_{SB}	$\overline{CE} = V_{IH}$ All I/O's = OPEN Other Inputs = V_{CC}	—	50	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Output High Voltage Level	V_{OH}	$I_{OH} = -400$ μA	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1$ mA	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.5	—	V

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, f = 1.0 MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

($T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0 to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and $C_L = 100$ pF

READ CYCLE

Parameter	Symbol	KM2864A-20 KM2864AH-20		KM2864A-25 KM2864AH-25		KM2864A-30 KM2864AH-30		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		250		300		ns
Chip Enable Access Time	t_{CE}		200		250		300	ns
Address Access Time	t_{AA}		200		250		300	ns
Output Enable Access Time	t_{OE}		100		120		150	ns
Chip Enable to Output in Low-Z	t_{LZ}	10		10		10		ns
Chip Disable to Output in High-Z	t_{HZ}	10	100	10	100	10	100	ns
Output Enable to Output in Low-Z	t_{OLZ}	50		50		50		ns
Output Disable to Output in High-Z	t_{OHZ}	10	60	10	80	10	100	ns
Output Hold from Address Change	t_{OH}	20		20		20		ns

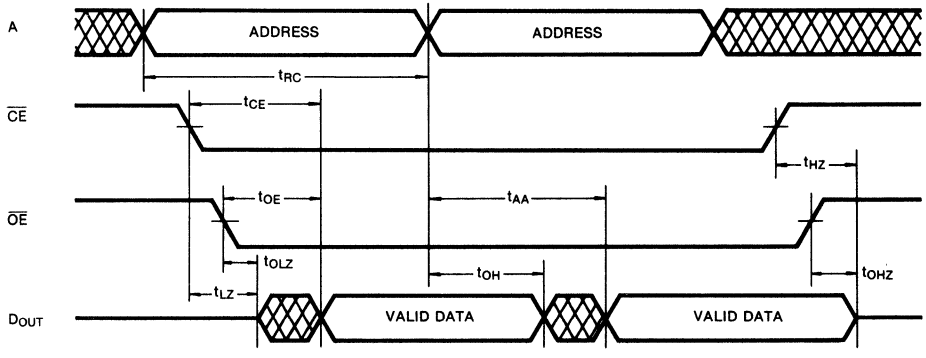
WRITE CYCLE

Parameter		Symbol	Min	Max	Units
Write Cycle Time	KM2864A	t_{WC}	10		ms
	KM2864AH		2		
Address Set-up Time		t_{AS}	10		ns
Address Hold Time		t_{AH}	120		ns
Write Set-up Time		t_{CS}	0		ns
Write Hold Time		t_{CH}	0		ns
Chip Enable to End of Write Input		t_{CW}	150		ns
Output Enable Set-up Time		t_{OES}	10		ns
Output Enable Hold Time		t_{OEH}	10		ns
Write Pulse Width		t_{WP}	150		ns
Data Latch Time		t_{DL}	50		ns
Data Valid Time		t_{DV}		1	μs
Data Set-up Time		t_{DS}	50		ns
Data Hold Time		t_{DH}	10		ns

TIMING DIAGRAMS

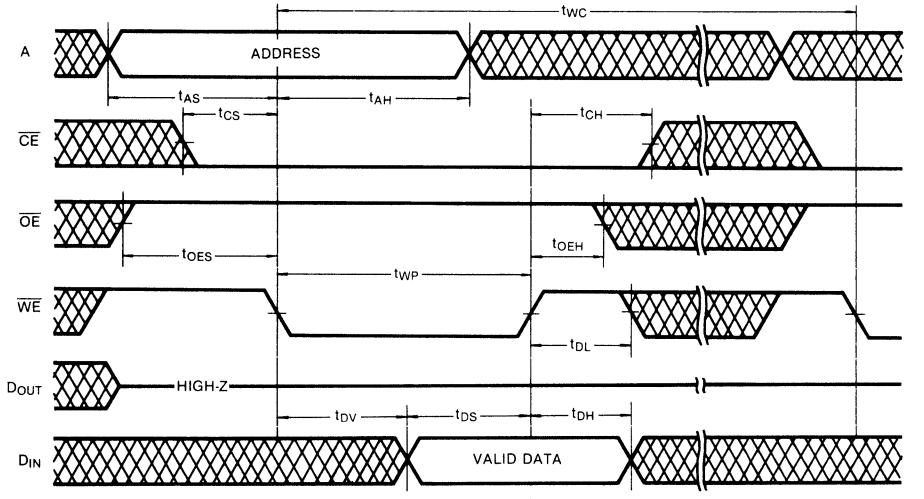
READ CYCLE

$\overline{WE} = V_{IH}$

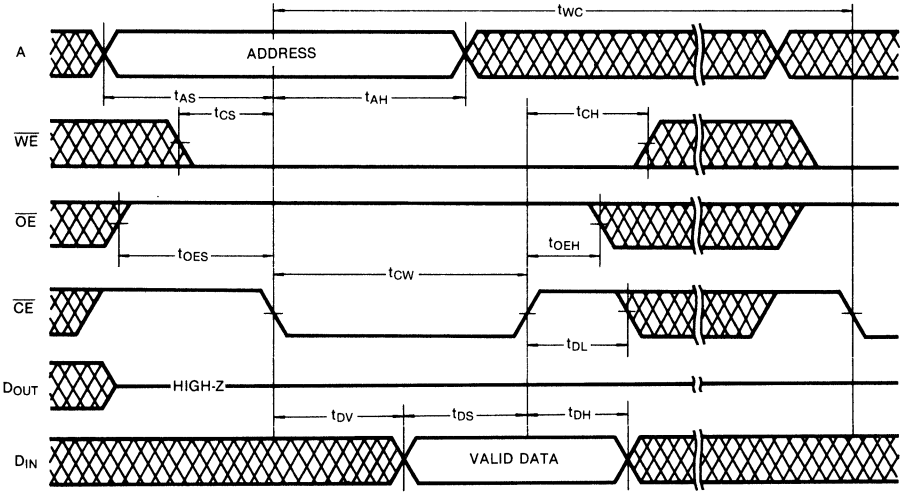


TIMING DIAGRAMS (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE



$\overline{CE}$ CONTROLLED WRITE CYCLE



DEVICE OPERATION

Read

Reading data from the KM2864A/AH is similar to reading data from a static RAM. A reading cycle occurs when $\overline{WE}$ is high and both $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high, the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

Write

Writing Data into the KM2864A/AH is very easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a static RAM.
A write cycle occurs when $\overline{OE}$ is high and both $\overline{CE}$ and $\overline{WE}$ are low. The address is latched by the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first. Address and data are conveniently latched in less than 200ns during a write operation. Once a byte write cycle is initiated, it will automatically continue to completion within 10ms (max) for the KM2864A or 2ms (max) for the KM2864AH. The existing data at the selected address is automatically erased and the new data is automatically written.

Standby

Power consumption may be reduced about 60% by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and $I/O_1 - I/O_8$ are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

Data Protection

Features have been designed into the KM2864A/AH that prevent unwanted write cycles during power supply transitions and system noise periods.

Write cycles are inhibited when V_{CC} is less than $V_{WI} = 3.5$ volts, the Write Inhibit V_{CC} level.

During power-up the KM2864A/AH automatically prevents any write operaion for a period of 9ms for the KM2864A or 2ms for the KM2864AH after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ or $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period.

Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit inadvertent writes.

$\overline{\text{Data}}$ Polling

The KM2864A/AH features $\overline{DATA}$ Polling to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not required any external hardware. During a write cycle the most significant bit of the byte written to the KM2864A/AH is inverted and routed to the output buffer. The I/O pins, I/O_1-I/O_7, remain in a high impedance state until a read command is initiated. Reading the device during the write operation will produce this inverted bit at I/O_8 (I/O_1-I/O_7 are indeterminate). True data will be produced at I/O_8 once the write cycle has been completed.

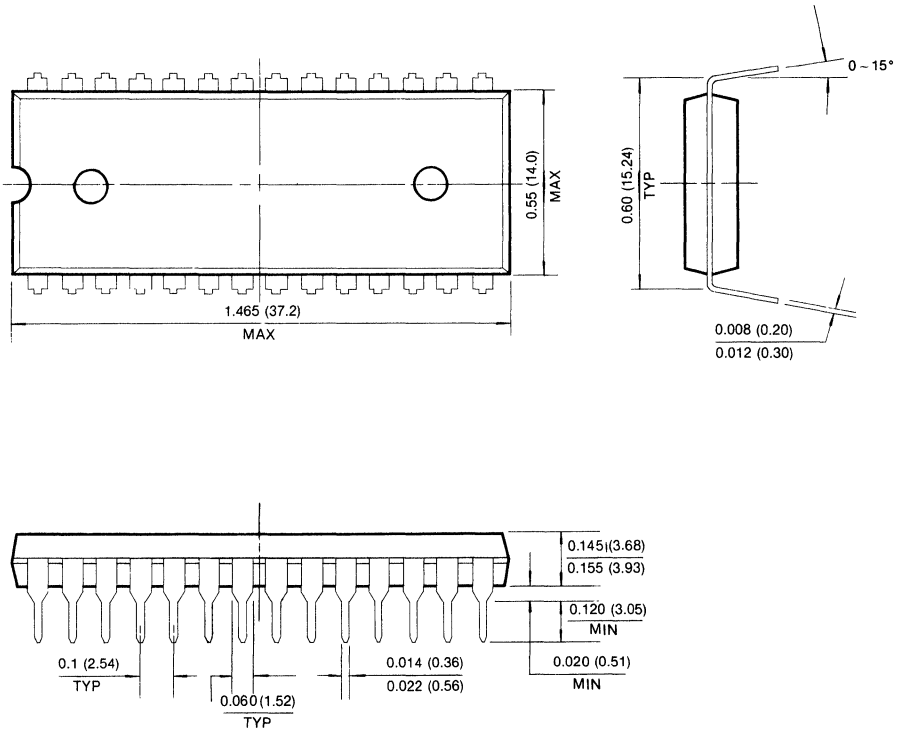
Endurance and Data Retention

The KM2864A/AH is designed for applications requiring, up to 10,000 write cycles per E^2PROM byte and ten years of data retention. This means that each byte may be reliably written 10,000 times without degrading device operation, and that the data in the byte will remain valid after its last rewrite operation for ten years with or without power applied.

PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



8K x 8 Bit EEPROM with Latches and Auto-Write

FEATURES

- **Simple Byte Write**
  - **Fast Byte Write Time**
  - **Single TTL Level Write Signal**
  - **Latched Address and Data**
  - **Automatic Internal Erase-before-Write**
  - **Automatic Write Timing**
  - **$\overline{\text{DATA}}$ Polling and Verification**
  - **Ready/$\overline{\text{Busy}}$ Output Pin**
- **Enhanced Write Protection**
- **Single 5 volt Supply**
- **Byte Write: 10ms (max)—KM2865A**
  2ms (max)—KM2865AH
- **Fast Access Time: 200ns**
- **Power: 50mA—Standby (max)**
  120mA—Operating (max)
- **Two Line Control-Eliminates Bus Contention**
- **10,000 Cycle Endurance**
- **JEDEC Byte-wide Memory Pinout**

GENERAL DESCRIPTION

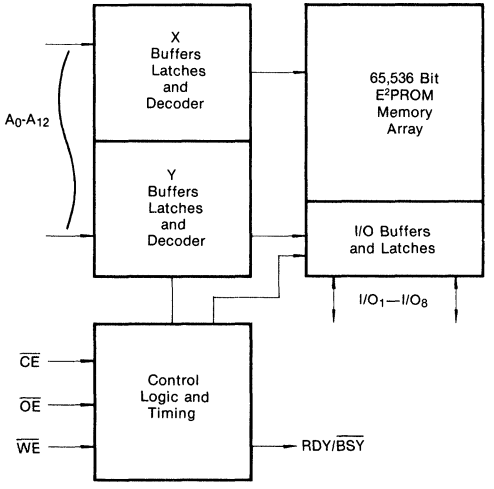
The KM2865A/AH is a 65,536 bit Electrically Erasable and Programmable Read-Only-Memory organized as 8,192 words by 8-bits. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

Writing data into the KM2865A/AH is very simple. The internally self-timed write cycle latches both address and data to provide a free system bus during the write period which is 10ms (max) for the KM2865A or 2ms (max) for the KM2865AH.

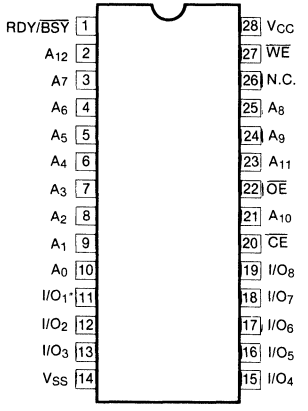
The KM2865A/AH features two end of write detection schemes to provide maximum design flexibility while enhancing the system performance. $\overline{\text{DATA}}$ Polling is a software scheme to detect the early completion of a write cycle without using any additional hardware. Ready/$\overline{\text{Busy}}$ is a hardware scheme in which Pin 1 is used to signal the status of the write operation and is especially useful in interrupt driven systems.

The KM2865A/AH is fabricated with the well defined floating gate NMOS technology using Fowler-Nordheim tunneling for erasing and programming.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{12}	Address Inputs
I/O_1—I/O_8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BSY}$	Ready/$\overline{Busy}$ Output
N.C.	No Connection
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}	−1 to +6.0	V
Temperature Under Bias	T_{bias}	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Short Circuit Output Current	I_{OS}	5	mA

*NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4

RECOMMENDED OPERATING CONDITIONS

(Voltages referenced to V_{SS}, $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	−1	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Max	Units
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$ All I/O's = OPEN Other Inputs = V_{CC}	—	120	mA
Standby Current	I_{SB}	$\overline{CE} = V_{IH}$ All I/O's = OPEN Other Inputs = V_{CC}	—	50	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Output High Voltage Level	V_{OH}	$I_{OH} = -400$ μA	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1$ mA	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.5	—	V

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, $f = 1.0$ MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

($T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0 to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and $C_L = 100$ pF

READ CYCLE

Parameter	Symbol	KM2865A-20 KM2865AH-20		KM2865A-25 KM2865AH-25		KM2865A-30 KM2865AH-30		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		250		300		ns
Chip Enable Access Time	t_{CE}		200		250		300	ns
Address Access Time	t_{AA}		200		250		300	ns
Output Enable Access Time	t_{OE}		100		120		150	ns
Chip Enable to Output in Low-Z	t_{LZ}	10		10		10		ns
Chip Disable to Output in High-Z	t_{HZ}	10	100	10	100	10	100	ns
Output Enable to Output in Low-Z	t_{OLZ}	50		50		50		ns
Output Disable to Output in High-Z	t_{OHZ}	10	60	10	80	10	100	ns
Output Hold from Address Change	t_{OH}	20		20		20		ns

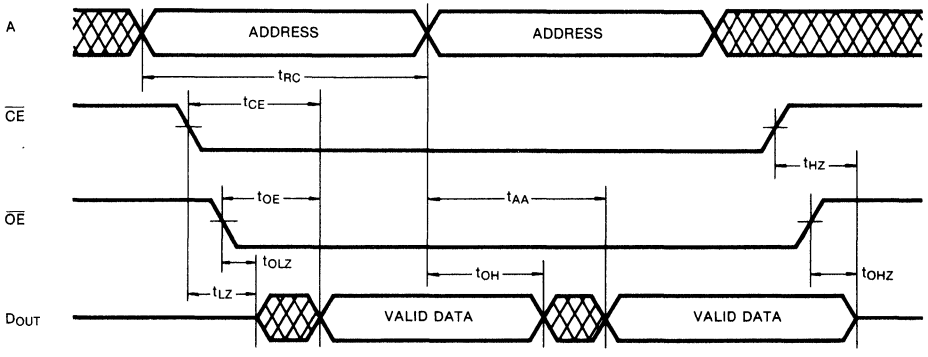
WRITE CYCLE

Parameter		Symbol	Min	Max	Units
Write Cycle Time	KM2865A	t_{WC}	10		ms
	KM2865AH		2		
Address Set-up Time		t_{AS}	10		ns
Address Hold Time		t_{AH}	120		ns
Write Set-up Time		t_{CS}	0		ns
Write Hold Time		t_{CH}	0		ns
Chip Enable to End of Write Input		t_{CW}	150		ns
Output Enable Set-up Time		t_{OES}	10		ns
Output Enable Hold Time		t_{OEH}	10		ns
Write Pulse Width		t_{WP}	150		ns
Data Latch Time		t_{DL}	50		ns
Data Valid Time		t_{DV}		1	μs
Data Set-up Time		t_{DS}	50		ns
Data Hold Time		t_{DH}	10		ns
Time to Device Busy		t_{DB}		120	ns
Busy to Write Recovery Time		t_{BWR}	50		ns

TIMING DIAGRAMS

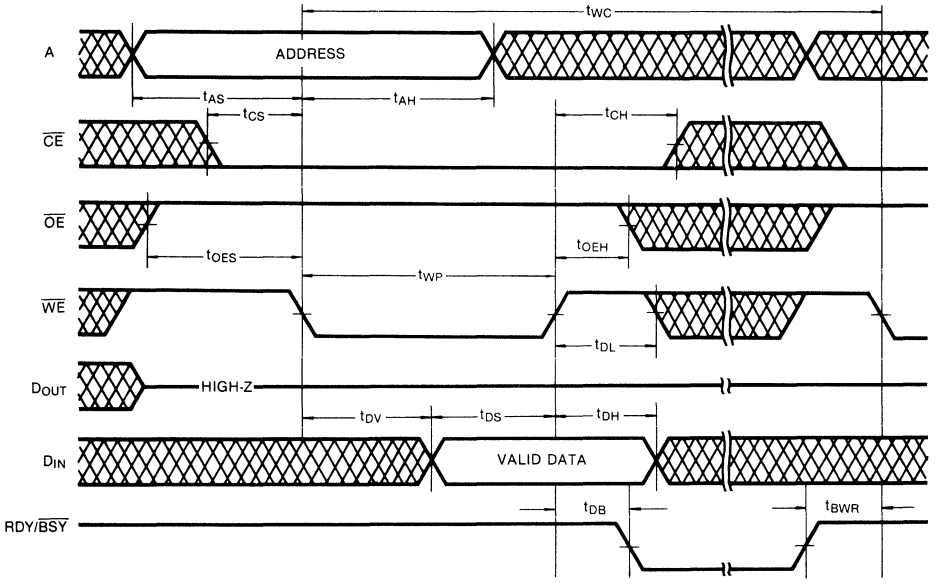
READ CYCLE

$\overline{WE} = V_{IH}$

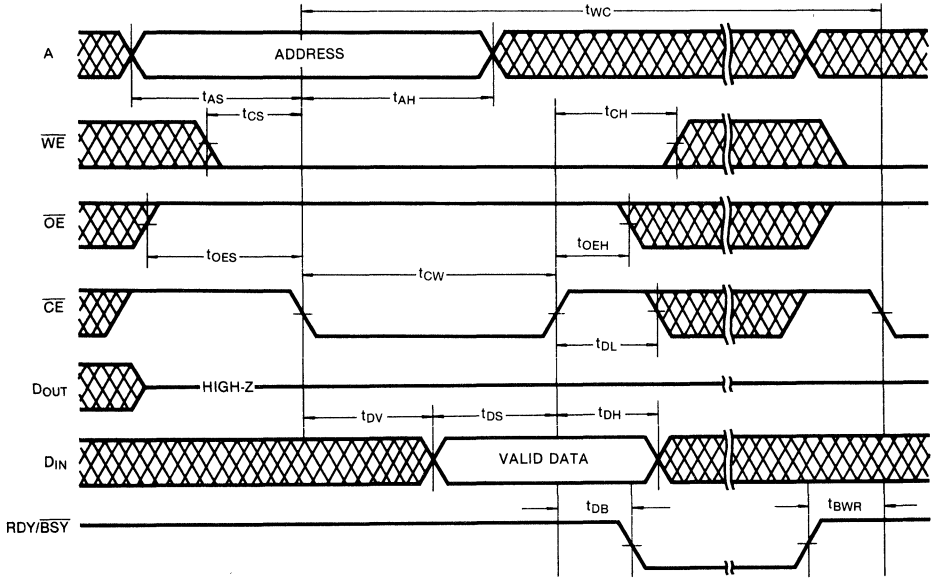


TIMING DIAGRAMS (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE



$\overline{CE}$ CONTROLLED WRITE CYCLE



DEVICE OPERATION

Read

Reading data from the KM2865A/AH is similar to reading data from a static RAM. A reading cycle occurs when $\overline{WE}$ is high and both $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high, the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

Write

Writing Data into the KM2865A/AH is very easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a static RAM.
A write cycle occurs when $\overline{OE}$ is high and both $\overline{CE}$ and $\overline{WE}$ are low. The address is latched by the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first. Address and data are conveniently latched in less than 200ns during a write operation. Once a byte write cycle is initiated it will automatically continue to completion within 10ms (max) for the KM2865A or 2ms (max) for the KM2865AH. The existing data at the selected address is automatically erased and the new data is automatically written.

Standby

Power consumption may be reduced about 60% by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and $I/O_1 - I/O_8$ are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

Data Protection

Features have been designed into the KM2865A/AH that prevent unwanted write cycles during power supply transitions and system noise periods.

Write cycles are inhibited when V_{CC} is less than $V_{WI} = 3.5$ volts, the Write Inhibit V_{CC} level.

During power-up the KM2865A/AH automatically prevents any write operaion for a period of 9ms for the KM2865A or 2ms for the KM2865AH after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ or $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period.

Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit inadvertent writes.

$\overline{\text{Data}}$ Polling

The KM2865A/AH features $\overline{DATA}$ Polling to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not required any external hardware. During a write cycle the most significant bit of the byte written to the KM2865A/AH is inverted and routed to the output buffer. The I/O pins, I/O_1-I/O_7, remain in a high impedance state until a read command is initiated. Reading the device during the write operation will produce this inverted bit at I/O_8 (I/O_1-I/O_7 are indeterminate). True data will be produced at I/O_8 once the write cycle has been completed.

Ready/$\overline{\text{Busy}}$

The KM2865AH has a Ready/$\overline{Busy}$ output pin that indicates when the write cycle is complete. The pin is normally high except when a write cycle is in progress, in which case the pin is low.
The Ready/$\overline{Busy}$ output is configured as open-drain driver there-by allowing two or more Ready/$\overline{Busy}$ output to be or-tied. This pin requires an appropriate pull-up register for proper operation. The pull-up resistor value for the Ready/$\overline{Busy}$ output maybe calculated as follows:

$$R_p = \frac{V_{CC}\,(MAX) - V_{OL}\,(MAX)}{I_{OL} + I_L} = \frac{5.1V}{2.1mA + I_L}$$

Where I_L is the sum of the input currents of all devices tied to the Ready/$\overline{Busy}$ pin.

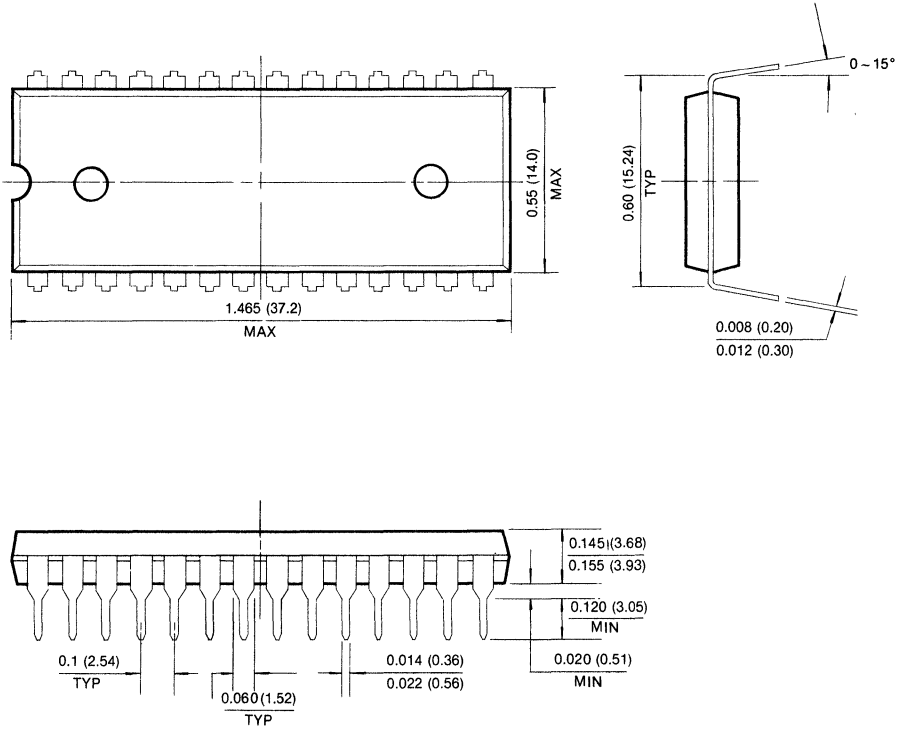
Endurance and Data Retention

The KM2865A/AH is designed for applications requiring, up to 10,000 write cycles per E^2PROM byte and ten years of data retention. This means that each byte may be reliably written 10,000 times without degrading device operation, and that the data in the byte will remain valid after its last rewrite operation for ten years with or without power applied.

PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



8K x 8 Bit CMOS EEPROM

FEATURES

- **Simple Byte Write**
  - **Single TTL Level Write Signal**
  - **Latched Address and Data**
  - **Automatic Internal Erase-before-Write**
  - **Automatic Write Timing**
  - **$\overline{\text{DATA}}$ Polling and Verification**
  - **Ready/$\overline{\text{Busy}}$ Output Pin (KM28C65)**
- **32-byte page write: 5ms max**
  - **Effective 150μS/byte write**
- **Enhanced Write Protection**
- **Single 5 volt Supply**
- **Fast Access Time: 200ns**
- **Power: 100 μA — Standby (max)**
  30 mA — Operating (max)
- **Two Line Control-Eliminates Bus Contention**
- **10,000 Cycle Endurance**
- **JEDEC Byte-wide Memory Pinout**

GENERAL DESCRIPTION

The KM28C64/C65 is a 65,536 bit electrically erasable and programmable Read-Only-Memory. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

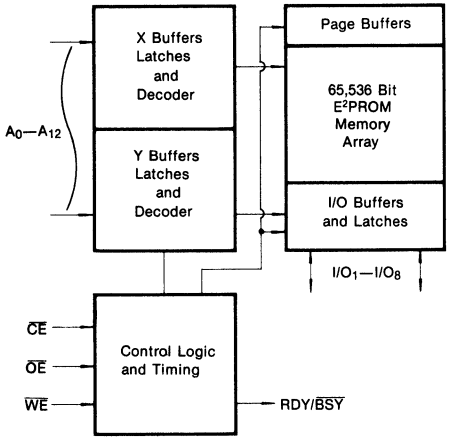
Writing data into the KM28C64/C65 is very simple. The internally self-timed write cycle latches both address and data to provide a free system bus during the 5ms (max) write period.

A 32-byte page write enables an entire chip written in 1.3 second.

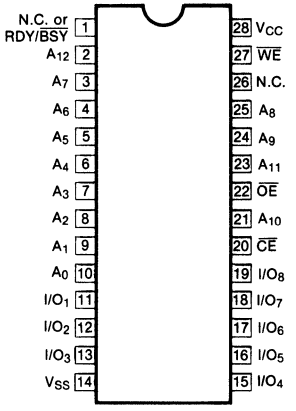
The KM28C64/C65 features $\overline{\text{DATA}}$-polling, which enables the EEPROM to signal the processor that a write operation is complete without requiring the use of any external hardware. Ready/$\overline{\text{Busy}}$ is a hardware scheme in which Pin 1 is used to signal the status of the write operation and is especially useful in interrupt driven systems.

The KM28C64/C65 is fabricated with the well defined floating gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0—A_{12}	Address Inputs
I/O_1—I/O_8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BSY}$	Ready/Busy Output
N.C.	No Connection
V_{CC}	+5V
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Rating	Symbol	Value	Units
Voltage on any Pin Relative to V_{SS}	V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Short Circuit Output Current	I_{os}	5	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltages referenced to V_{SS}, $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage, Inputs	V_{IH}	2.0	—	$V_{CC}+0.3$	V
Input Low Voltage, all Inputs	V_{IL}	−0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Max	Units
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ all I/O's = open all addresses* (NOTE 1)		30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$ all I/O's = open		1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC} - 0.2V$ all I/O's = open		100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}		10	μA
Output Leakage Current	I_{LO}	$V_{in} = 0$ to V_{CC}		10	μA
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4		V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$		0.4	V
Write Inhibit V_{CC} Level	V_{WL}		3.5		V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 5MHz

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, $f = 1.0$ MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE	OE	WE	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
L	L	H	$\overline{\text{Data}}$-Polling	$I/O_8 = \overline{D}_8$	Active
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

($T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100$ pF

READ CYCLE

Parameter	Symbol	KM28C64-20 KM28C65-20		KM28C64-25 KM28C65-25		Units
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		250		ns
Chip Enable Access Time	t_{CE}		200		250	ns
Address Access Time	t_{AA}		80		100	ns
Output Enable Access Time	t_{OE}		80		100	ns
Chip Enable to Output in Low-Z	t_{LZ}	0		0		ns
Chip Disable to Output in High-Z	t_{HZ}	5	70	5	90	ns
Output Enable to Output in Low-Z	t_{OLZ}	5		5		ns
Output Disable to Output in High-Z	t_{OHZ}	5	70	5	90	ns
Output Hold from Address Change	t_{OH}	10		10		ns

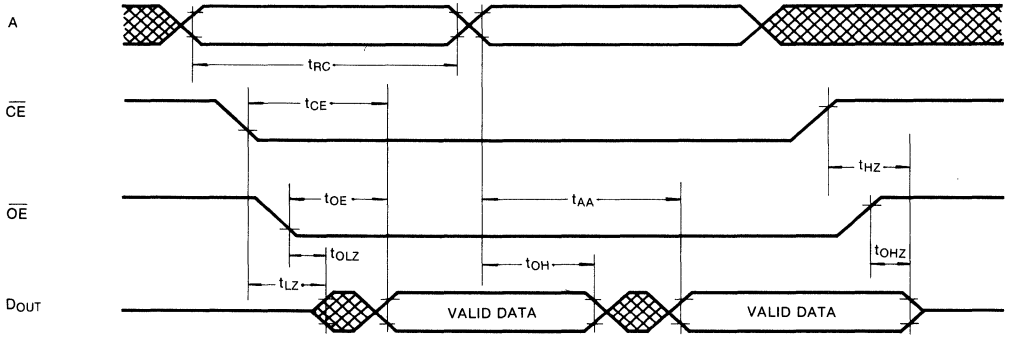
WRITE CYCLE

Parameter	Symbol	Min	Max	Units
Write Cycle Time	t_{WC}	5		ms
Address Set-Up Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	80		ns
Write Set-Up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
Chip Enable to End of Write Input	t_{CW}	100		ns
Output Enable Set-Up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
Write Pulse Width	t_{WP}	100		ns
Data Set-Up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	10		ns
Time to Device Busy	t_{DB}		100	ns
Busy to Write Recovery Time	t_{BWR}	50		ns
Byte Load Cycle	t_{BLC}	0.2	30	μs

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and start at a rising edge of $\overline{WE}$.

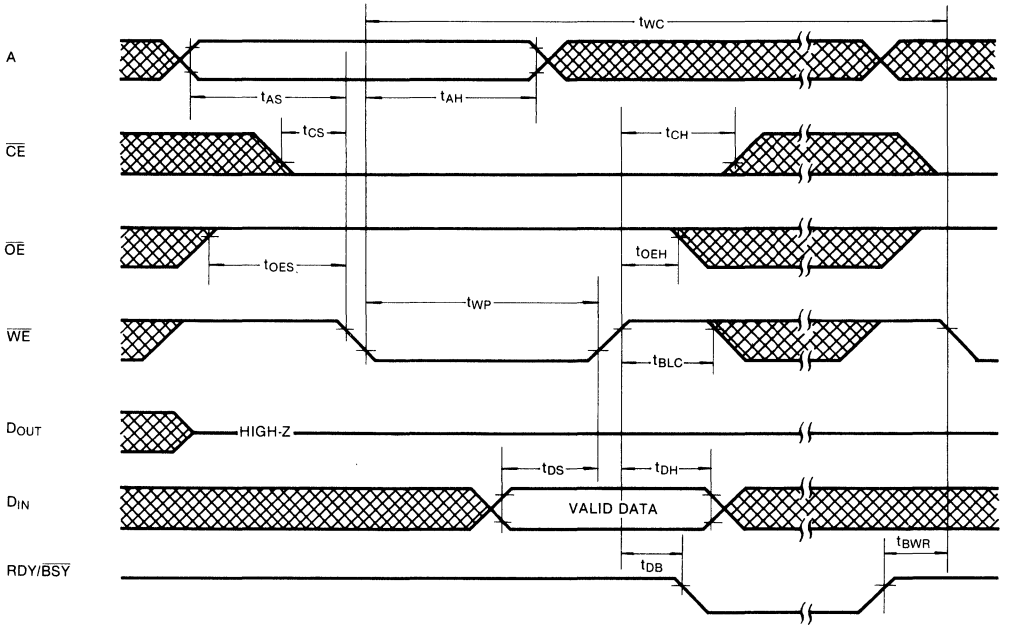
TIMING DIAGRAMS

READ CYCLE $\overline{WE} = V_{IH}$

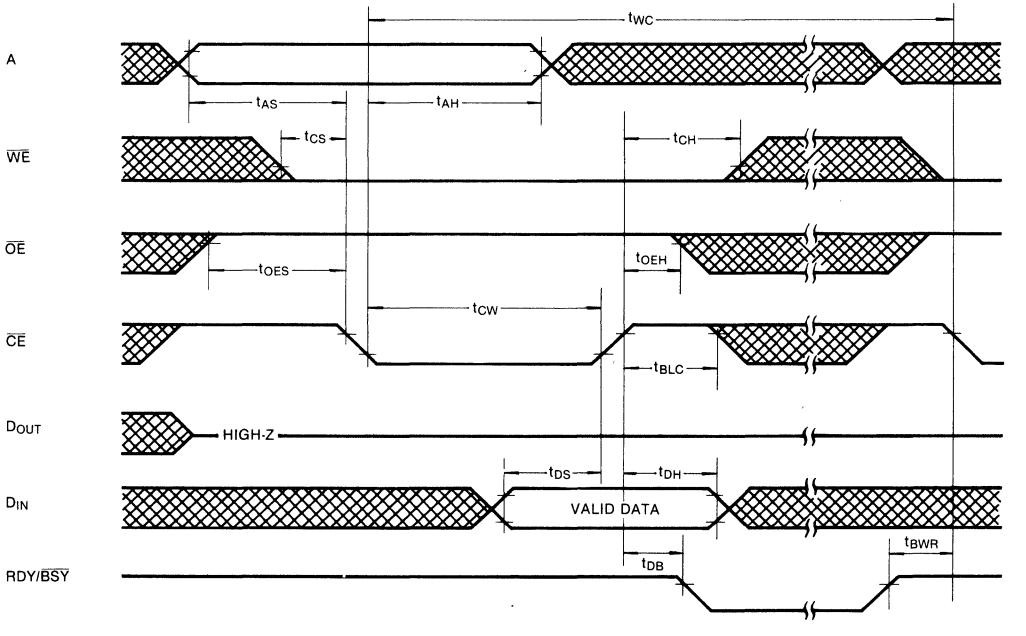


TIMING DIAGRAMS (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE

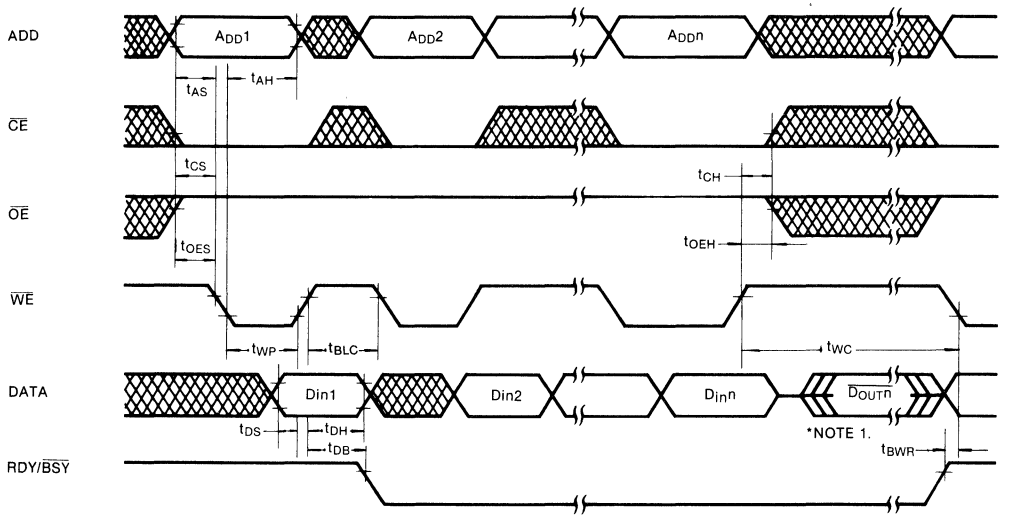


$\overline{CE}$ CONTROLLED WRITE CYCLE

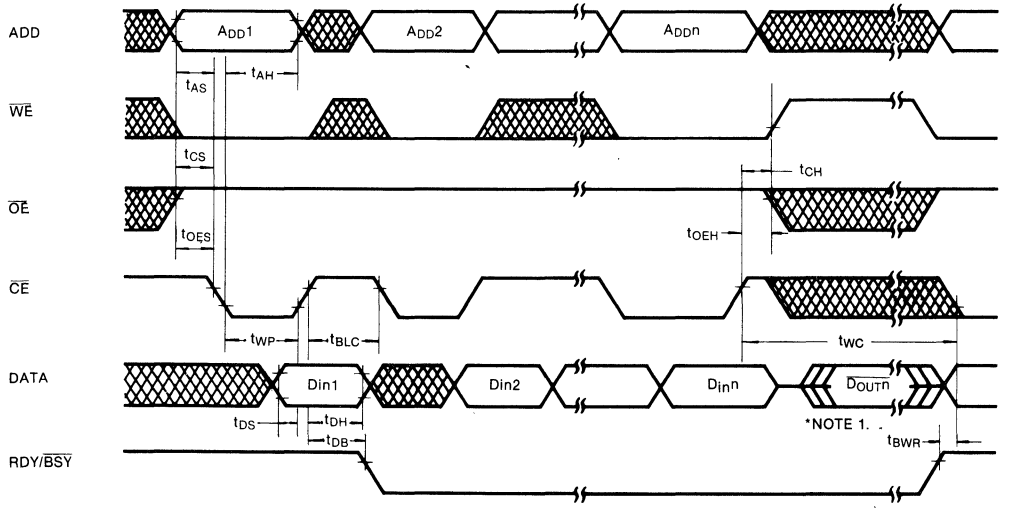


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE ($\overline{WE}$ CONTROLLED WRITE CYCLE)



PAGE MODE WRITE ($\overline{CE}$ CONTROLLED WRITE CYCLE)



*Note 1. Tristate for I/O_1-I/O_7, $\overline{D_{outn}}$ for I/O_8 if the chip is read (see $\overline{Data}$-polling)

DEVICE OPERATION

Read

Reading data from the KM28C64/C65 is similar to reading data from a SRAM. A read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

Write

Writing data into the KM28C64/C65 is very easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write mode of the KM28C64/C65 is only a part of the page write mode. A single byte data loading followed by a t_{BLC} time out and by a write cycle will complete a byte mode write. In this mode, the write is exactly identical to that of the KM2864A/65A.

**** PAGE WRITE MODE ****

The KM28C64/C65 allows up to 32 bytes to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 32 bytes data are loaded into the KM28C64/C65 internal registers and a write period, in which the loaded datas in the registers are written to the EEPROM cells of the selected page.

Data are loaded into the KM28C64/C65 by sequentially pulsing $\overline{WE}$ with $\overline{CE}$ LOW and $\overline{OE}$ HIGH. On each $\overline{WE}$, address is latched on the falling edge of the $\overline{WE}$ and data is latched on the rising edge of the $\overline{WE}$. The data can be loaded in any "Y" address order and can be renewed in the data loading period.

Since the timer for the data loading period (t_{BLC}) is reset at the falling edge of $\overline{WE}$ and starts at every rising edge of $\overline{WE}$, the only requirement on $\overline{WE}$ to continue the data loading is that the interval between $\overline{WE}$ pulses does not exceed the maximum t_{BLC} (30μs). If $\overline{OE}$ goes LOW during the data loading period, further attempt to load the data will be ignored because the external $\overline{WE}$ signal is blocked by $\overline{OE}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{WE}$ pulse if $\overline{OE}$ is LOW.

The page address for the write is the "X" address (A5-A12) latched on the last $\overline{WE}$. The write period consists of an erase cycle followed by a program cycle. During the erase cycle the existing data of the locations being addressed are erased. The new data latched at the registers are written into the locations during the program cycle. Note that only the addressed locations in a page are rewritten during a page write cycle.

The KM28C64/C65 also supports $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch address and data as well as $\overline{WE}$.

Standby

Power consumption may be reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and I/O_1-I/O_8 are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

Data Protection

Features have been designed into the KM28C64/C65 that prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C64/C65 has an protection feature against $\overline{WE}$ noises, a $\overline{WE}$ noise having width shorter than 20ns (typ.) will not start any unwanted write cycle.

Write cycles are also inhibited when V_{CC} is less than $V_{WI} = 3.5$ volts, the Write Inhibits V_{CC} level.

During power-up, the KM28C64/C65 automatically prevents any write operation for a period of 5ms (max.) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ and $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period.

Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-On and power-Off will inhibit inadvertent writes.

$\overline{\text{Data}}$ Polling

The KM28C64/C65 features $\overline{\text{DATA}}$-Polling at I/O_8 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not require any external hardware. Reading the device at any time during a write operation will produce, at I/O_8 an inverted value of Last data loaded into the EEPROM (I/O_1-I/O_7 are at the high impedance state). True data will be produced at I/O_8 once the write cycle has been completed.

Ready/$\overline{\text{Busy}}$

The KM28C65 has a Ready/$\overline{\text{Busy}}$ output on pin 1 that indicates when the write cycle is complete. The pin is normally high except when a write cycle is in progress, in which case the pin is low.

DEVICE OPERATION (Continued)

The Read/$\overline{\text{Busy}}$ output is configured as open-drain driver there-by allowing two or more Ready/$\overline{\text{Busy}}$ output to be OR-tied. This pin requires an appropriate pull-up resistor for proper operation. The pull-up resistor value maybe calculated as follows

$$R_P = \frac{V_{CC}(max) - V_{OL}(max)}{I_{OL} + I_L} = \frac{5.1V}{2.1mA + I_L}$$

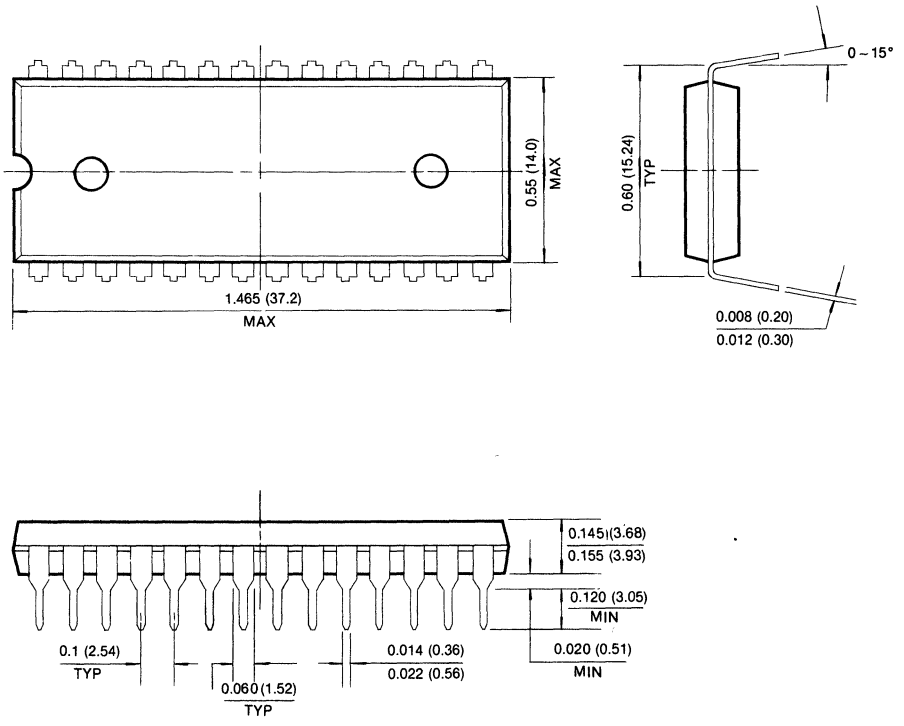
where I_L is the sum of the input currents of all devices tied to the Ready/Busy pin.

Endurance and Data Retention

The KM28C64/C65 is designed for applications requiring up to 10,000 write cycles per EEPROM byte and ten years of data retention. This means that each byte may be reliably written 10,000 times without degrading device operation and that the data in the byte will remain valid after its last write operation for ten years with or without power applied.

PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE

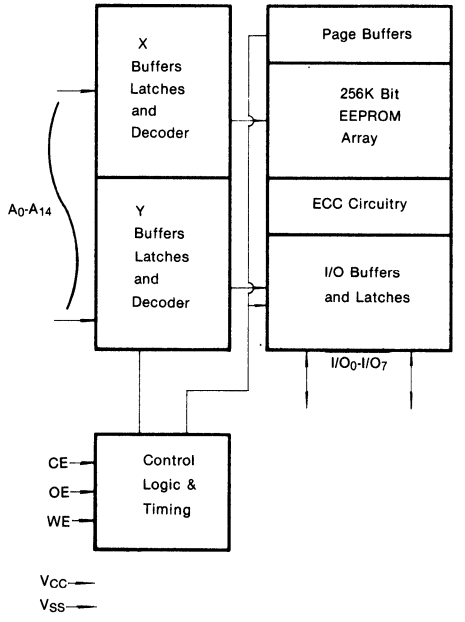


256K CMOS EEPROM

FEATURES

- **High Performance Advanced CMOS Technology**
- **150 nsec maximum Access Time**
- **Low Power**
  - **— 100μA Standby Current**
  - **—60mA Active Current**
- **Fast Write Cycle times**
  - **—Byte or Page Write Cycle: 5ms Typical**
  - **—64-Byte Page Write**
  - **—Effective 80μsec/Byte Write**
  - **—Complete Memory Rewite: 2.5 sec**
- **Write Cycle Completion Indication**
  - **—Data Polling**
  - **—Toggle bit**
- **Enhanced Write Protection**
  - **—Software Write Protection**
  - **—Hardware Write Protection**
  - **—Programmable Write Inhibit V_{CC} Level**
- **High Endurance**
  - **—10,000 Cycle Endurance/Byte**
  - **—10 Year Data Retention**
- **JEDEC Approved Byte-wide Pinout**

FUNCTIONAL BLOCK DIAGRAM



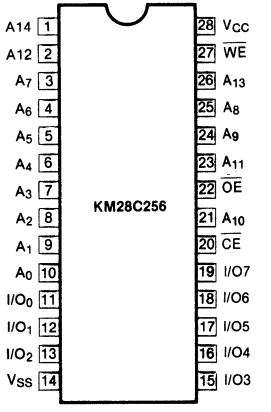
DESCRIPTION

The KM28C256 is a CMOS 5V Only 32K x 8 Electrically Erasable Programmable Read Only Memory. It is fabricated with the well defined floating gate CMOS technology using Fowler-Nordheim tunnelling for erasing and programming.

The KM28C256 provides easy of use features. The internally self-timed write cycle latches both address and data to give a free system bus during the 5ms(max) write period. A 64-byte page write enables an entire chip written in less than 2.5 seconds. The data polling scheme enables the EEPROM to signal the processor that a write operation is complete without requiring the use of any external hardware.

The KM28C256 is designed for applications up to 10,000 write cycles per byte and over 10 years of data retention. The chip, however, endures typically 50,000 write cycles per byte without any failure.

PIN CONFIGURATION



PIN NAMES

Pin Name	Pin Function
A_0-A_{14}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5V
V_{SS}	Ground

NOTES

SALES OFFICES and MANUFACTURER'S REPRESENTATIVES 5

1. U.S.A

SALES OFFICES

CALIFORNIA

201 East Sandpoint
Suite 220 Santa Ana 92707
714-662-3406

2700 Augustine Drive
Suite 198 Santa Clara 95054
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617-273-4888

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312-852-2011

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919-294-5141

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HAAS & ASSOC., INC.

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Scottsdale 85252
602-994-3813

CALIFORNIA

SYN PAC

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Santa Clara 95054
408-988-6988

WESTAR REP COMPANY

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714-835-4711

QUEST-REP, INC.

San Diego, CA.
619-546-1933

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416-622-7558

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ELECTRODYNE

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303-695-8903

CONNECTICUT

PHOENIX SALES

257 Main Street
Torrington, 06790
203-476-7709

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