# Radiated Emissions and CRT Displays

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## INTRODUCTION

Electromagnetic compatibility (EMC) is a vital concern for anyone who produces or uses electronic equipment. As the performance of computer systems continues to improve, designing for EMC will become more challenging. This makes it very important to address EMC right at the start of the product design. Doing this will minimize the product development costs attributable to EMC and avoid unnecessary delays in product release. This application note addresses the fundamental EMC concerns for the CRT display. It provides information to help the engineer design for EMC and bypass easily avoidable emissions problems. The primary focus will be on radiated emissions.

## WHY REGULATIONS?

Regulations are needed to avoid the malfunctioning of a piece of electronic equipment due to the electromagnetic interference caused by another piece of electronic equipment. There are two ways to solve this problem. The first is to limit the emissions of electronic equipment and the second is to make a piece of electronic equipment immune to the interference. You can do one or both. Presently, most regulations are for emissions rather than immunity. The European Community is planning to require immunity testing and certification starting in 1996.

## REGULATING AGENCIES

In 1934, the International Special Committee on Radio Interference (CISPR) was formed to determine measurement methods and limits for radio-frequency (RF) emissions. CISPR which is part of the International Electrotechnical Commission (IEC) is not a regulating agency, but its standards have either been adopted by or used as a guide to establish regulations by many countries. In 1985, CISPR adopted Publication 22 for Information Technology Equipment. This standard applies to computers and display devices.

Nations that endorse CISPR regulations include the United States, Germany, France, Canada, Sweden and the United Kingdom. Each of these nations has released an emissions standard for computer products. Table I below summarizes their standards.

**TABLE I. Regulating Agencies and Computer Products Standards by Country**

| Country | Regulating Agency | Computer Products Standard |
|---|---|---|
| Canada | CSA | CSA C 108.8 |
| France | NFC | NFC91.022 |
| Germany | Verband Deutscher Elektrotechniker | VDE0871 |
| Sweden | SEN | SEN 471010 |
| United Kingdom | BS | BS 6527 |
| United States | Federal Communications Commission | FCC Part 15J |

## TYPES OF EMISSIONS

There are two types of emissions that must be kept under control; radiated and conducted. They can be described as follows:

**Radiated Emissions**—Unwanted electromagnetic energy that is sourced from an electronic system or a part of that system by way of an electric or magnetic field.

**Conducted Emissions**—Unwanted energy that is sourced from one electronic circuit to another through a common impedance such as power or ground.

## CHALLENGES OF CRT DISPLAY DESIGNS

The challenges of today's CRT display designs include meeting the performance requirements of the end user, meeting the cost objectives of the end user (which translates to a set of design and production cost objectives), and meeting the regulatory agency requirements of the intended market(s).

With the advent of more sophisticated uses for the CRT display, the performance requirements are becoming more demanding. Applications such as desktop publishing, computer aided design and multi-tasking have demanded higher resolution as well as higher overall picture quality. Supplying the needed resolution, brightness, stability, aspect ratio, distortion limits and convergence (for color displays) provide a tough challenge for all the designers involved. User adjustments are being added beyond the standard contrast and brightness controls. These include controls for size, pincushion, trapezoid, as well as color temperature. Often these controls may be exercised using an on-screen display (OSD).

Design for EMC adds to this challenge. We have previously mentioned some regulatory agencies. Meeting the requirements of these agencies requires up front design methodology in order to keep test time and production costs to a minimum. The graph in *Figure 1* shows that the cost for EMC solutions increase exponentially as the EMC design is delayed with respect to the start of the product design. Using well established design guidelines as well as beginning EMC testing early in the design cycle will minimize cost and avoid last minute EMC fire drills.

The law of supply and demand primarily determines what the CRT display producer may sell his product for on the open market. This price will set the cost goals for the design and production of the display. The CRT display market is very competitive which tells us that keeping EMC costs at a minimum may give a particular manufacturer a market advantage. Addressing the EMC issues as early in the design phase as possible will allow the designers more time to implement the most cost effective solution.

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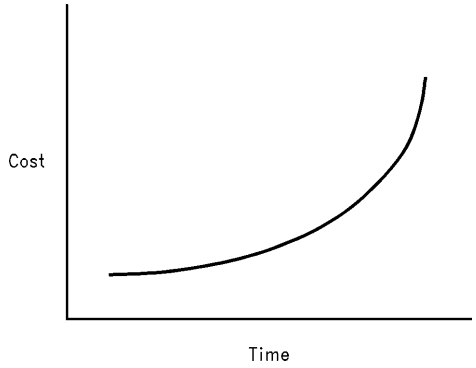


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**FIGURE 1. EMC Solution Cost as EMC Design is Delayed in Monitor Design Cycle**

## TEST CONFIGURATION

In general, the display would be tested with the rest of the system that it would be marketed with. In the case where the monitor is sold as a separate item, there are minimum test configurations specified by the regulatory agencies. For example, the minimum configuration for FCC Class B testing is as follows:

- Computer with Graphics Card
- Keyboard
- Serial port device
- Parallel port device
- Monitor

Examples of serial and parallel port devices are printers, modems or a mouse. The monitor is tested at a maximum of three resolutions (and therefore scan rates). Table I lists the documents for various regulatory agencies that should be referenced for specific test configuration information.

## MAJOR CONTRIBUTORS OF HIGH FREQUENCY EMISSIONS

The configuration of the computer system that would be tested was discussed in the previous section. Most high frequency emissions will emanate from the *computer (and graphics card)* and the *display monitor*. The computer contains high frequency clock signals and other signals generated from this clock. These signals are routed over a large area on printed circuit boards (PCBs) and ribbon or other cables. As you already know, long PCB traces and cables are the primary source of emissions because they are more efficient transmitters at the frequencies present in these systems.

The graphics card generates the video signal that drives the CRT display monitor (in our case). The high frequency pixel clock as well as the video signal itself may contain harmonics that can cause emission problems out to 1 GHz. The monitor takes these high frequency video signals and amplifies them by as much as 60 V/V which produces a signal with an amplitude as large as 50 $V_{P-P}$ at the cathode of the CRT. All of these signals are rich in high frequency harmonics (this will be discussed further later). The large amplitude at the CRT cathode provides for some interesting emission control challenges. When designing a computer system, a general rule of thumb to use is to divide the allowable emissions equally between the PC (with a properly terminated video cable attached) and the CRT display. For example, if you wanted to pass FCC class B testing with 6 dB margin, the PC and video cable by themselves should have 12 dB margin. We will look more closely at the CRT display monitor later in this article.

Most of the high frequency energy is contained in waveforms that the monitor design engineer will look at in the time domain. Open site tests are performed in the frequency domain, therefore, the EMI engineer will need to convert these time domain signals to their frequency equivalents in order to more effectively do his job. This leads us to our next topic.

## TRANSFORMING FROM THE TIME TO THE FREQUENCY DOMAIN

Inside a display monitor we have synchronization pulses, video pulses, pulses that drive the switching power supplies, as well as blanking and clamp pulses. Attention is given to rise and fall times, pulse widths, ringing and flatness. These are all time domain parameters. When we go out to the open site for emissions testing everything is measured in the frequency domain. How do we make this transformation? The answer is to perform a Fourier analysis of the time domain waveforms.

A rigorous Fourier analysis is not necessary. It is simpler to construct a Fourier envelope of our time domain signals. The Fourier series for a periodic pulse waveform will consist of a series of discrete sine waves comprised of the fundamental ($F_0$) and integer multiples of it. The Fourier envelope for the periodic waveform shown in *Figure 2* is shown in *Figure 3.* The frequency components of the time domain waveform will be contained inside this envelope. *Figure 3* shows that between the first and second break points ($F_1$ and $F_2$), the envelope rolls off at 20 dB/Dec. After the second break point, the envelope rolls off at 40 dB/Dec.

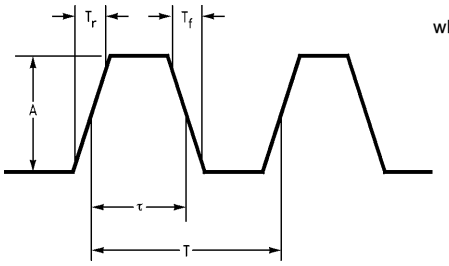
The value of the envelope at a specific frequency ($F_X$) can be calculated using one of the following equations:

$$\text{for } F_x < F_1,\ V = \frac{2\,A\,\tau}{T} \qquad (1a)$$

$$\text{for } F_1 < F_X < F_2,\ V = \frac{0.64\,A}{T \times F_X} \qquad (1b)$$

$$\text{for } F_X > F_2,\ V = \frac{0.2\,A}{T \times T_r \times F_X^2} \qquad (1c)$$

(If $T_f < T_r$, use $T_f$)

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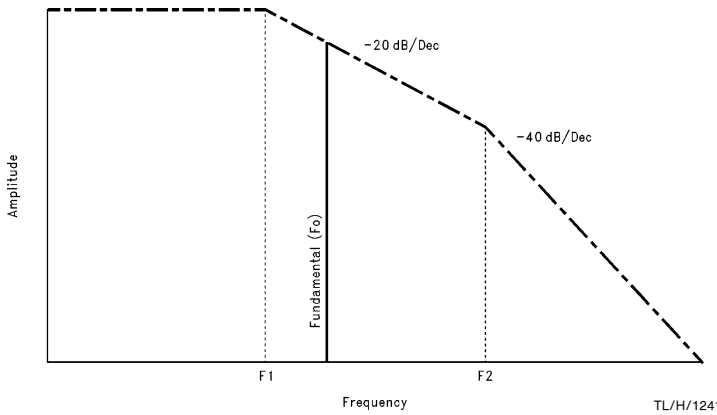
where **T** = the period of the repetitive waveform
$\tau$ = pulsewidth at the 50% points
**A** = Pulse amplitude
$\mathbf{T_r/T_f}$ = the 10%–90% rise and fall times

**FIGURE 2. Generic Periodic Pulse**

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Where $F_0 = \frac{1}{T}$

$F_1 = \frac{0.32}{\tau}$

and $F_2 = \frac{0.32}{T_r}$

(If $T_r < T_r$, use $T_f$)

**FIGURE 3. Generic Graph of The Fourier Envelope of a Periodic Pulse**

*Figure 4* shows the Fourier envelopes for a 50 MHz square wave with a 2 ns, 4 ns and 6 ns rise time. The first breakpoint ($F_1$ = 32 MHz) is the same for all three envelopes. Note the significant increase in high frequency signal content as the rise time is reduced (the second breakpoints are at different frequencies).

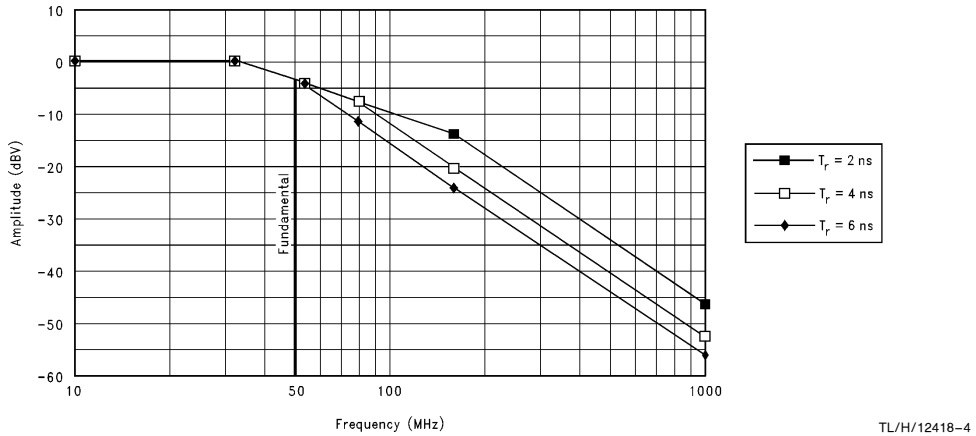


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**FIGURE 4. Spectral Envelope for a 1 $V_{P-P}$, 50 MHz Square Wave with Various Rise Times**

It is also interesting to compare the Fourier envelopes of two square waves with the same rise and fall times but of different frequencies. *Figure 5* shows the comparison of 1 $V_{P-P}$ 25 MHz and 50 MHz square waves each with 4 ns rise and fall times. In this case the first break points are at different frequencies and the second break points are at the same frequency. This is representative of the effect that the Video format (pixel rate) has on the high frequency energy that is fed to the monitor by the PC, given that the same graphics card is used.

**PREDICTING RADIATED EMISSIONS**

Far field emissions of conductors that carry high frequency signals can be estimated using the following equation:

$$E_{(dB\ \mu V/m)} = 20 \log \left( \frac{1.3}{D} \times \frac{V}{Z_C} \times A \times F^2_{MHz} \right) \quad (2)$$

where E = The electromagnetic field in dB $\mu$V/m
D = Observation distance in meters
A = Circuit area in $cm^2$ (A = l x s, where l = trace length and s = average distance to ground trace)
V = Signal amplitude in volts
$Z_C$ = Impedance of the circuit
F = Frequency of interest in MHz

Table II shows the calculated emissions for a 6 cm length signal trace on a PCB that carries a 1 $V_{P-P}$ signal for various frequencies. This demonstrates that it doesn't take a very large loop area to cause a significant emission at high frequencies. Frequency components whose amplitudes are greater than 1 $V_{P-P}$ are guaranteed at XGA and higher resolution video formats.

**TABLE II. Emissions at 3m for a 1V Signal from a 6 cm Signal Trace**

| Frequency (MHz) | Avg dist to ground (cm) | $Z_C$ ($\Omega$) | Emission (dB $\mu$V) |
|---|---|---|---|
| 50 | 0.5 | 377 | 19 |
| 100 | 0.5 | 377 | 31 |
| 200 | 0.5 | 377 | 43 |
| 300 | 0.5 | 377 | 50 |
| 400 | 0.5 | 377 | 55 |
| 500 | 0.5 | 377 | 59 |

The Fourier envelope along with equation 2 can be used to estimate the emissions of a monitor in the design stage. These estimates can be used to help define the requirements for circuit boards and shielding needs (for cables, boards or even the complete monitor) of a monitor system early in the design process. For additional information on calculating emissions, please refer to Reference 1.

**CRT MONITOR HIQH FREQUENCY EMISSIONS**

We have presented a simple method that can be used to predict and also to understand the sources and causes of high frequency emissions. Now let's move on and discuss areas that relate directly to the CRT monitor. *Figure 6* shows a simplified block diagram of a CRT monitor. The main areas where HF signals are present are the video channel, CRT and the switching power supplies.

Before we start it is important to note that the presence of high frequency signals in itself does not cause high frequency emissions. It is the lack of control of the paths (and the length of the paths) that these signal voltages and currents follow that creates the problem. We will discuss the following topics with respect to the CRT monitor: *grounding, cabling, PCB layout, shielding and the role of ferrite*.

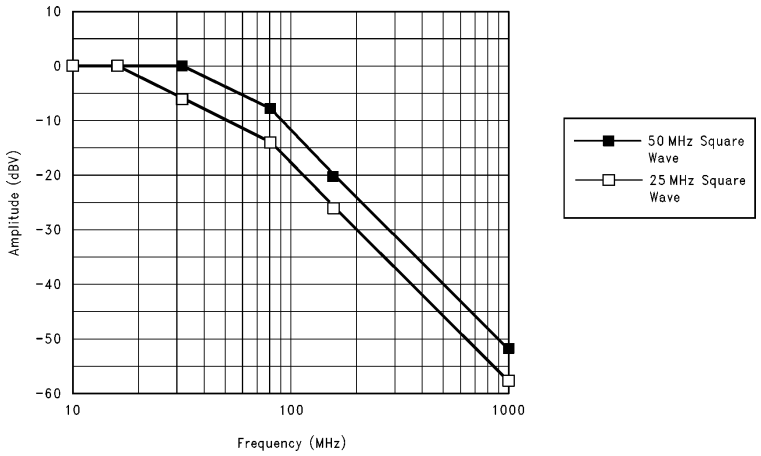


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**FIGURE 5. Fourier Envelopes of 4 ns Rise Time, 1 $V_{P-P}$ Square Waves**

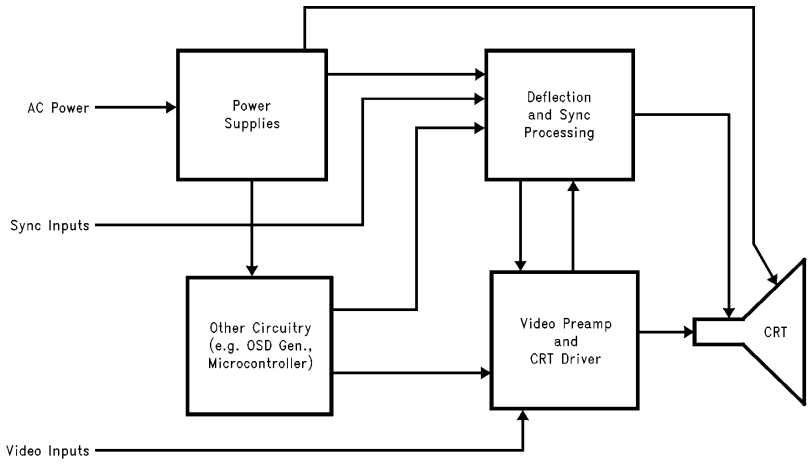


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**FIGURE 6. Simplified Block Diagram of a CRT Monitor**

**Grounding**

The three grounding practices that are used are single point, multi-point and hybrid. These practices can be summarized as follows:

- **Single Point**—The 0V references of all circuits/PCB's/assemblies are tied together at only one point on the chassis.
- **Multi-Point**—The 0V references of all circuits/PCB's/assemblies are tied together at various points along a common reference plane or chassis.
- **Hybrid**—A combination of both of the above approaches is used.

In general, the single point grounding practice works well at low frequencies because the inductance of the wire used for the ground connections will not be significant. At high frequencies ($>$ 10 MHz) the multi-point approach is needed to minimize the effects of the wire inductance. In addition to connections by wire or straps, inductors can be used to make low frequency ground connections (and high frequency opens), while capacitors can be used to make HF ground connections (and low frequency opens). In the CRT monitor, the final ground configuration will most likely be hybrid due to the wide frequency range of signals used. It is also important to note that parasitic capacitance will cause HF ground connections that are not intended in the design.

For more information on these grounding approaches please consult the references at the end of this article. The grounding scheme used or options available in a monitor will vary depending on such factors as cost, performance and even the system it will be used with. Remember that the control of signal currents and voltages is important to optimize performance for picture quality as well as EMI. Therefore, the **most** important thing is to know and understand how the system ground is set up so that you may tailor your circuit design to best use the available resources in that system.

Some of the important attributes of a good ground scheme are:

1. Low impedance at frequencies of interest.
2. Shortest possible return path to minimize the size of the current loop.
3. Controlled paths of return currents.
4. Provide a solid 0V reference for all signals (especially low level analog signals). The availability of a 0V reference at the input signal connectors establishes a good reference.

It is important that grounding be addressed in all areas of design and it will be a part of the discussion in all the following sections.

**Grounding for Arc Protection**

The CRT requires high voltages to perform the beam acceleration and focus functions. These voltages range from 1 KV to 30 KV which present the possibility of an arc. Therefore, safeguards must be implemented to protect the monitor electronics against damage that can be caused by the energy present in the arc. One common protection scheme is to use a ground for the CRT that is isolated from the video electronics circuit ground as shown in *Figure 7*. The CRT ground would be connected to the Heater return as well as the ground pin for the focus arc protection (which may be built into the CRT connector). A ground strap is usually connected to the CRT DAG coating (which is connected to the monitor chassis ground).

This technique works well to protect the electronics against damage that can be produced by an arc because it provides a controlled path for the arc current to return back to its source, which is internal to the CRT. However, this technique elongates the return path of the video signal current which consists of the electron beam, currents to charge the cathode capacitance and any stray capacitance in the CRT connector and PCB. These longer and uncontrolled current paths may and usually do cause a worse scenario for the EMI engineer.

**Cabling**

Inside a monitor, cables/wires are used to distribute DC power, Ground, RGB video signals, synchronization (sync) signals, deflection currents and various control signals which depend upon the complexity of the monitor. Looking at this list, the only intended high frequency signal carriers are the video cables and possibly the cable that carries the sync signals (due to the edge speed). There are many types of cables and wires that can be used to distribute these signals. They include single wire, twisted pair, shielded twisted pair, coax, triax, ribbon cable and various versions of these types. Which type is used depends on EMC design practice as well as cost and performance requirements.

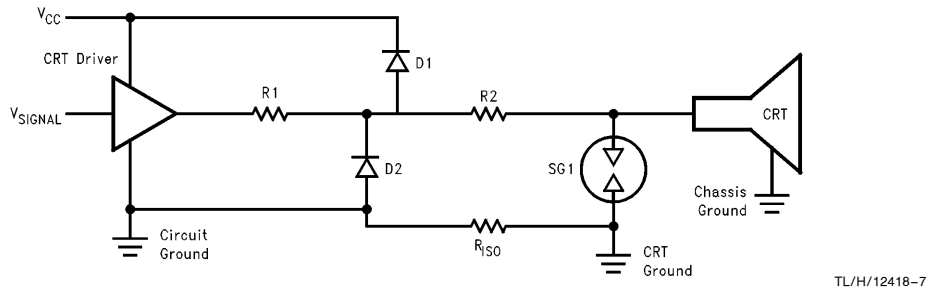


**FIGURE 7. Grounding for CRT Arc Protection**

Due to their long length, cables are one of the primary sources of EMI. Table III below lists the wavelength, ¼ wavelength and 1/20 wavelength of a wire or cable at various frequencies. The 1/20 wavelength is the point where the conductor makes the transition from electrically short to electrically long. At this point the conductor can no longer be treated as a simple wire, but transmission line effects must be considered. Notice how short the 1/20 wavelength numbers get at the higher frequencies. The ¼ wavelength is important because that is the point where a conductor is a good RF transmitter or receiver. When we look at the ¼ wavelength numbers, it is apparent that we really need to keep high frequency signals and noise from undesired cables. This is not always a simple task. It is of no surprise then that cables are one of our primary sources of emissions.

**TABLE III. Conductor Wavelengths at Various Frequencies**

| Freq. | Wavelength | | ¼ Wavelength | | 1/20 Wavelength | |
|---|---|---|---|---|---|---|
| (MHz) | (cm) | (in) | (cm) | (in) | (cm) | (in) |
| 50 | 600.0 | 236.2 | 150.0 | 59.1 | 30.0 | 11.8 |
| 100 | 300.0 | 118.1 | 75.0 | 29.5 | 15.0 | 5.9 |
| 200 | 150.0 | 59.1 | 37.5 | 14.8 | 7.5 | 3.0 |
| 300 | 100.0 | 39.4 | 25.0 | 9.8 | 5.0 | 2.0 |
| 400 | 75.0 | 29.5 | 18.8 | 7.4 | 3.8 | 1.5 |
| 500 | 60.0 | 23.6 | 15.0 | 5.9 | 3.0 | 1.2 |

If we refer back to equation 2, we see that emissions are directly proportional to the area of the path that a signal will follow. Cable/wire lengths are usually quite long (15 cm to 45 cm). When we add to this that many are not near a ground wire or ground plane because they are *intended to carry only low frequency or DC signals*, the loop areas can be very large. Cables that penetrate an EMI shield can pick up noise, carry it outside the shield and radiate this energy to the outside world. Let's take a look at how a cable can cause a problem. Suppose we wanted to know the noise level at 300 MHz that would potentially cause an FCC Class B emissions problem (if $>$ 46 dB $\mu$V/m) for a 10 inch long cable whose average distance from ground is 1 inch. Rearranging equation 2 to solve for V yields:

$$V = \frac{10^{\left(\frac{E_{dB\mu V/m}}{20}\right)}}{\frac{1.3}{D} \times \frac{1}{Z_C} \times A \times F_{MHz}^2} \qquad (3)$$

Substitution of the knowns leads to:

$$V = \frac{10^{\left(\frac{46}{20}\right)}}{\frac{1.3}{3} \times \frac{1}{377} \times 62.5 \times 300^2} \approx 30\ mV$$

This calculation neglects the lengths of the signal trace that is on the assemblies that this wire connects. As we can see, this is not very much noise. If we would like 6 dB margin, this noise level would have to be reduced to 15 mV. I think this example makes it clear that a small noise level in the wrong place can cause trouble. One way to keep cables and wiring clean is to use filters at the I/O's of the assembly or PCB. If that is not possible, a twisted pair (only effective for differential noise) or a shielded cable can be used.

This leads to another question; should the shield be grounded at one or both ends? For low frequency shielding, grounding at one end will do the job. For high frequencies, grounding at both ends is necessary. If grounding at both ends causes a low frequency problem, then one end can be connected to ground through a capacitor to eliminate the low frequency ground loop.

How about cables that are *intended* to carry high frequency signals? The video input cable is one of the major concerns when addressing this category. Coaxial cable, at a minimum, should be used for both internal and external video signals. I have observed two basic interconnect schemes. The first is a shielded video cable (group of coax cables with a shield over them) that is an integral part of the monitor and is routed directly to the video board. This method makes it easy to avoid discontinuities in the shield. The second uses a separate set of cables for the inside and the outside of the monitor. The connector interface to the monitor can be one of several types (e.g., a single connector (D type) or a group of coax connectors) that are located at the back panel of the monitor. An external video cable(s) which is usually shielded or of the coax type is used to interface the video source to the monitor. Another set of cables would then be used to route the signals from these connectors to the video board. With either approach the important thing is to get the video and sync signals to their destinations without imposing high frequency signals on other conductors or circuits and not radiate a significant amount of energy by themselves. Therefore it is important to:

1. Avoid discontinuities in the shield.
2. Terminate the cables in their characteristic impedance.
3. The cable shield should be connected to chassis, assembly shield or other destination around the full circumference of the cable.

Another question that often comes up is: what type of cable shield or shielded cable should be used? There are two types of shields used in commercial designs (unless of course you want to use a rigid conduit). They are braids and foil. Cable shields must be able to tolerate movement and flexing without compromising their effectiveness. The main advantage of a braid is it can meet these mechanical requirements. The main disadvantage is that it does not provide 100% coverage of the cable you want to shield. On the contrary, foil can provide 100% coverage but is not as tolerant of the movement and flexing that is required. A good alternative is to use both. This way if the foil is compromised, you will still have the protection of the braid. Another alternative would be to use a double braid which will increase coverage of the cable.

**The Use of Ferrites**

Ferrite beads are often used by the EMI Engineer as the last minute fix for an emission problem. The fact is that they can be designed in to absorb high frequency (HF) energy that is headed towards your low frequency and DC circuits and eliminate potential EMI problems before the equipment gets out to the test site.

The impedance of a ferrite bead can be expressed using equation 4.

$$Z = \sqrt{R^2 + \omega^2 L^2} \quad (4)$$

where R = equivalent resistance of the bead
L = equivalent reactance of the bead
and $\omega = 2\pi f$ where f is frequency

Both R and L are dependent on frequency. This equation does not specifically show the impedance roll off at high frequency. Presently available ferrite beads have a maximum impedance of 100Ω–600Ω which occurs between 10 MHz and 300 MHz. The peak impedance and the frequency at which it occurs depends on the composition of and the size and shape of the ferrite bead. Since the insertion loss provided by a ferrite bead is what matters most, it is important to realize that they work best in low impedance circuits such as power supplies.

The insertion loss can be calculated using equation 5.

$$A_{dB} = 20 \log \frac{Z_G + Z_L + Z_B}{Z_G + Z_L} \quad (5)$$

where $A_{dB}$ = Insertion loss in dB
$Z_G$ = The impedance of the source
$Z_L$ = The impedance of the load
$Z_B$ = The impedance of the bead

Ferrite beads can be used to control differential mode (DM) and common mode (CM) noise. *Figures 8(a)* through *8(c)* show how this can be done. It is important to know what type of noise you are working with in order to effectively use a ferrite bead.

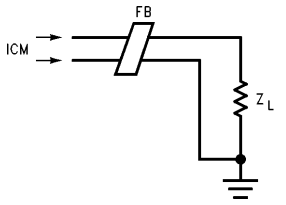


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**FIGURE 8(a). CM Noise Suppression**

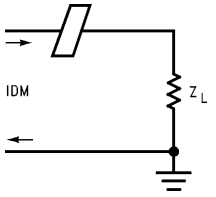


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**FIGURE 8(b). DM Noise Suppression**

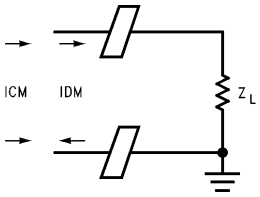


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**FIGURE 8(c). CM and DM Noise Suppression**

Let's take a look at some ways that ferrite beads will help reduce noise and emissions in a display monitor. *Figure 9* shows a schematic diagram of how a ferrite bead can be used to filter a DC power supply for a video CRT driver. Filter capacitors C3 and C4 should be chosen to supply the required HF energy for the CRT Driver. The ferrite bead along with C1 and C2 will then function to isolate and filter any transients caused by the operation of the CRT Driver.

I will note that it is important to have a good ground for the video circuit to prevent noise from coupling through the common ground.

Another example would be using a ferrite bead on the G2 lead at the video board end. It is not uncommon for the HF video signal to couple unto this wire due to stray capacitance between the video signal paths and the G2 supply path. *Figure 10* shows this. Multiple turns can be used to increase the effectiveness of the ferrite.

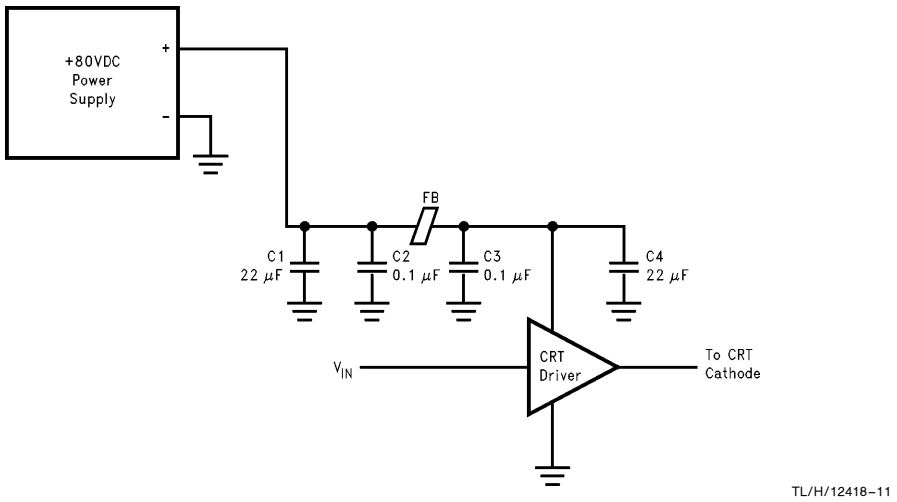


**FIGURE 9. A Ferrite Bead Used for Power Supply Filtering**

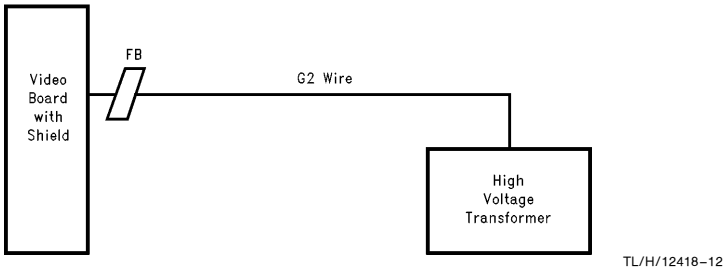


**FIGURE 10. A Ferrite Bead Used on the G2 Wire**

**Shielding**

After we have estimated the potential emissions or measured the actual emissions of our monitor or its sub-assemblies, we can define the trouble areas and look at our shielding requirements. For most commercial monitor applications the concern is for radiated emissions from 30 MHz to 1 GHz. Materials such as aluminum, copper and steel all have good high frequency (HF) shielding characteristics. Aluminum is probably the most common in commercial monitors. Let's quickly review how a shield works and then we can discuss the two important considerations that will control the effectiveness of a shield design. For a more in depth study of shielding refer to references 1 and 2.

There are two basic shielding mechanisms: *reflection* and *absorption*. Shielding effectiveness (SE) can be described by the following equation:

$$SE_{dB} = R_{dB} + A_{dB} \quad (6)$$

where R is the loss due to reflection and A is the loss due to absorption. *Figure 11* is a simple model that shows these basic mechanisms. The reflective loss is due to the part of the field that does not penetrate (is reflected by) the shield and is a function of the impedance difference between the field and the shield (often called the barrier). The reflective loss for highly conductive shields can be approximated by

$$R_{dB} = 20 \log \left( \frac{Z_W}{4 Z_B} \right) \quad (7)$$

where $Z_W$ is the wave (electric or magnetic) impedance in ohms and $Z_B$ is the impedance of the barrier in ohms/square. $Z_B$ can be calculated using the following equation:

$$Z_B = 3.68 \times 10^{-7} \sqrt{\frac{\mu_r}{\sigma_r}} \sqrt{F} \quad (8)$$

where $\mu_r$ is the relative permeability of the material, r is the relative coductivity of the material and F is the frequency of interest.

Reflection is the dominant effect for electric fields because there is a large impedance mismatch ($Z_W > 377\Omega$). The closer the barrier is to the source of the electric field the higher the reflective loss will be since $Z_w$ gets larger. As you move up to and beyond a distance of $\lambda/2\pi$ from the source, where $\lambda$ is the wavelength of the signal of interest, we make the transition from the near field to the far field. At this point $Z_W = 377\Omega$ which is the impedance of free space. Therefore, to maximize the electric field losses due to reflection, the shield should be as close as possible to the energy source.

The absorption loss can be approximated by the following equation:

$$A_{dB} = 131\, t \sqrt{\mu_r \sigma_r F} \quad (9)$$

where $\mu_r$ is the relative permeability of the material, $\sigma_r$ is the relative conductivity of the material, t is the thickness of the material in mm and F is the frequency of interest in MHz. This equation tells us two things: 1) Absorption loss is directly proportional to the thickness of the shield, and 2) Absorption loss will increase as frequency increases. Note that absorption loss is not dependent on the distance from the energy source.

One topic I haven't discussed is re-reflection. If we refer to *Figure 11* we can see that as the field moves through the shield it is also reflected at the second boundary. This will occur over and over as the field moves back and forth through the thickness of the shield, some of the energy escaping at each point of reflection. In our application, this effect is usually negligible.

If there were no openings in a shield, it would be easy for us to pass emissions testing. However, that is not possible in the real world. Since we have cables to interface with, CRT's to connect to and we need openings for ventilation, maximizing the effectiveness of our shield is more challenging. Let's discuss the two categories that will have the greatest effect on the effectiveness of our shield: 1) Openings in the shield and 2) Penetrations by cables and wires.

Openings in the shield may be intended or not intended. We intentionally put openings in to interface with the outside

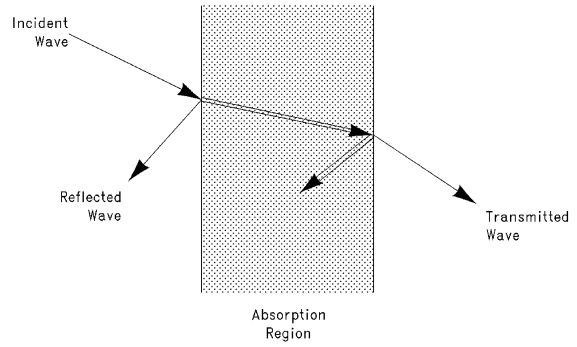


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**FIGURE 11. Simple Shielding Model**

world. Unintentional openings are usually due to a poor connection between two mating surfaces. In either case the effectiveness of the shield will degrade as a function of the maximum length of the opening. The shielding effectiveness for an opening in a box shield is given by the following equation:

$$SE_{dB} = 20 \log \left( \frac{150}{FL} \right) \quad (10)$$

where F is frequency in MHz and L is the maximum length of the opening in meters. Keeping the maximum length less than $\lambda/20$ will yield 20 dB minimum shielding effectiveness. Table III shows the maximum length opening ($\lambda/20$ lengths) which will yield 20 dB of shielding effectiveness for various frequencies. When there are multiple openings on the same surface of the box shield the reduction in SE can be approximated by the following equation:

$$SE_{dB} = -20 \log \sqrt{n} \quad (11)$$

where n is the number of openings.

Cables and wires that penetrate a shield not only require an opening in the shield to do so, but they are prime candidates to pick up noise and carry it outside of the shield. This is the second consideration that must be addressed in order to maintain the effectiveness of the shield. Due to their long length they are also effective transmitters of this noise. Filtering of the input and output signals (this may not always be desired) as close as possible to the point of entry into the shield can be very effective in controlling EMI. Cables, such as the video cable, are required to carry HF signals. Depending on the speed of the video signal, these cables may need to be shielded. See the section on cabling for more information.

Example 1

Design a box shield for a video board that will mount directly to the neck of the CRT. The emissions have been calculated and measured and the shielding requirements are defined as in Table IV below.

**TABLE IV. Video Board Box Shield Requirements**

| Frequency Range (MHz) | Required SE (dB) | Required SE (dB) for 6 dB Margin |
|---|---|---|
| 30–100 | 22 | 28 |
| 100–300 | 16 | 22 |
| 300–500 | 10 | 16 |

The shield requires some openings for interconnect and ventilation. Our list of openings is as follows:

1. 3 cable connectors - connector size is 0.8″ × 0.25″ 1″ × 0.5″ opening
2. 3 0.3″ holes for the G2, focus and a ground wire
3. Ventilation holes at the top and bottom - 25 0.25″ diameter holes on each surface.
4. Opening for CRT socket to connect to CRT - 1″ diameter circle

Let's assume that we will build our shield with two mil thick aluminum ($\sigma_r = 0.61$ and $\mu_r = 1$). Since the openings in the shield will have the greatest control over its effectiveness, we will start there. First let's decide where the openings will go. Items 2 and 4 will be on the front or CRT side of the shield. The cable connector openings will be on the sides. Let's use equations 10 and 11 and make some calculations. Table V summarizes the results.

Table V shows that if we put all three cable connectors on the same side of the shield we will not meet our objectives. If we move one cable connector to the other side we will improve our result by 1.8 dB and meet our objective. The three wires and the CRT connector opening are on the same side of the box shield, therefore we must integrate their effect. Having two one inch holes on the same side of a shield would yield SE's of 32.4 dB, 22.9 dB, and 18.4 dB at 100 MHz, 300 MHz and 500 MHz respectively. Since the three holes for the wires together have a smaller max length (0.9 inches) than a 1 inch hole we can assume that the total result for the three wire holes and the CRT connector hole will be slightly better than this. Therefore, if we properly locate the necessary openings we can meet our objectives.

As a check on our shield material, let's take a look at the effectiveness of our shield with no openings. We can do this using equations 6, 7, 8 and 9. The lowest impedance in the video signal path will be at the output of the CRT driver section. Lets estimate it to be about 10 pF. At 500 MHz, the impedance of 10 pF is approximately $30\Omega$ $[1/(2\pi fC)]$. For simplicity we will use $Z_W = 30$, which will give us a conservative estimate. Table VI summarizes the results. These numbers are much higher than the calculations for the openings. All that we have to do is to pay careful attention to the penetrations by the cables and wires that interface with the video board.

**TABLE V. SE Calculations for Openings in the Box Shield**

| | Max Length | | | SE (dB) for One Opening at F (MHz) | | | Correction for Multiple Opening | SE (dB) with Multiple Opening at F (MHz) | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Openings for | Inches | Meters | Qty | 100 | 300 | 500 | | 100 | 300 | 500 |
| Cable Conn. | 1.12 | 0.0284 | 3 | 34.4 | 24.9 | 20.5 | −4.8 | 29.7 | 20.1 | 15.7 |
| Wires | 0.3 | 0.0076 | 3 | 45.9 | 36.3 | 31.9 | −4.8 | 41.1 | 31.6 | 27.1 |
| Ventilation | 0.25 | 0.0064 | 25 | 47.5 | 37.9 | 33.5 | −14.0 | 33.5 | 23.9 | 19.5 |
| CRT Conn. | 1 | 0.0254 | 1 | 35.4 | 25.9 | 21.4 | 0.0 | 35.4 | 25.9 | 21.4 |

**TABLE VI. SE for a 2 mil Thick Aluminum Box Shield with No Openings**

| Frequency | $Z_B$ (Ω/Sq.) | R (dB) | A (dB) | SE (dB) |
|---|---|---|---|---|
| 100 | .0047 | 64.0 | 52.0 | 116.3 |
| 300 | .0082 | 59.3 | 90.0 | 149.3 |
| 500 | .0105 | 57.0 | 116.2 | 173.3 |

In summary, once we have measured or estimated the shielding requirements we can design a shield that will meet them. For our application (30 MHz–1 GHz), the openings in the shield and the penetrations into the shield will have the greatest control over the effectiveness of the box shield.

**Printed Circuit Board (PCB) Design**

Commercial monitors will contain at least two PCB's (one for power supplies and deflection control and one for video). Since the main HF threat is from the video signal itself, our discussion will be focused there. However, all the principles discussed are applicable to any board design. As you move from the lower to the higher resolution monitors, you will usually find additional PCB's. Careful attention to PCB design is a very significant part of controlling EMI. I will discuss *PCB type, component placement and interconnection, minimizing loop areas, power and ground, crosstalk and power supply filtering*. All of these categories are dependent upon each other, so the choice made in one area will affect your design in another area. For example if you choose to use a single sided (SS) PCB, you will also choose larger loop areas (for signals and their returns and power supply filters) and a higher impedance ground.

**PCB Type**

Inside the video monitor the PCB's will usually be either single sided (SS) or double sided (DS). SS PCB's offer a significant cost advantage but make the control of EMI a greater challenge. Based on some monitor experience, SS PCB's are usually used for the power supply and deflection circuits (often called the main board) and for the video board in monitors with a maximum display resolution of 1024 × 768. DS PCB's allow the designer greater control in minimizing loop areas, lower impedance power and ground distribution, as well as the capability of designing 75Ω microstrip for the video input signal trace (for cases where the preamp is not in close proximity to the video input connector). The ability to have a large ground plane is an important attribute to help control EMI.

**Component Placement and Interconnection**

The component placement on a video board will be a function of the size and shape of the PCB as well as its interconnect scheme in the monitor. Optimal parts placement will be different for a PCB that mounts directly to the CRT versus one that is wired to a CRT connector board. However, the rules for optimal parts placement will be the same. Mechanical and thermal considerations will also affect the size and shape of the PCB. Following is a list for the objectives of the parts placement:

1. Allow minimum lengths for all HF signal traces and return paths.
2. Allow low impedance ground and power connections over the frequency range of interest.
3. Allow signal flow that supports adequate separation or isolation between HF signal paths and other signal paths in order to minimize crosstalk.

Once the system design is completed and the size and shape of the video board are defined, what procedure or strategy should be followed to optimize placement? It makes sense to start with the portion of the circuit which poses the greatest EMI threat (processes the most HF energy) and then work our way down to the less threatening circuits as we go along. Fortunately, this also is in the best interest for performance. The following basic guideline is recommended:

1. First locate the CRT driver circuit as close as possible to the video output connector. Be sure to leave room for arc protection, AC coupling/clamp or other support circuitry that is required. It is important to keep the video output nodes as short as possible. Therefore, any components that connect to them should be as close as possible.
2. Then locate the video preamp as close to the driver as possible with the video output signal points as close as possible to the driver video inputs.
3. Then locate the video input connector as close as possible to the video input section of the preamp.

*Figure 12* shows the ideal parts placement for a video channel that is comprised of a monolithic preamp and a hybrid (or monolithic) CRT driver that is part of a video board that would mount directly to the CRT. In an actual application, this parts placement would probably not be possible. The important thing is to keep the video signal flow over the smallest area possible. The closer we can come to the ideal parts placement, the better the performance will be and the lower the emissions of the board will be.

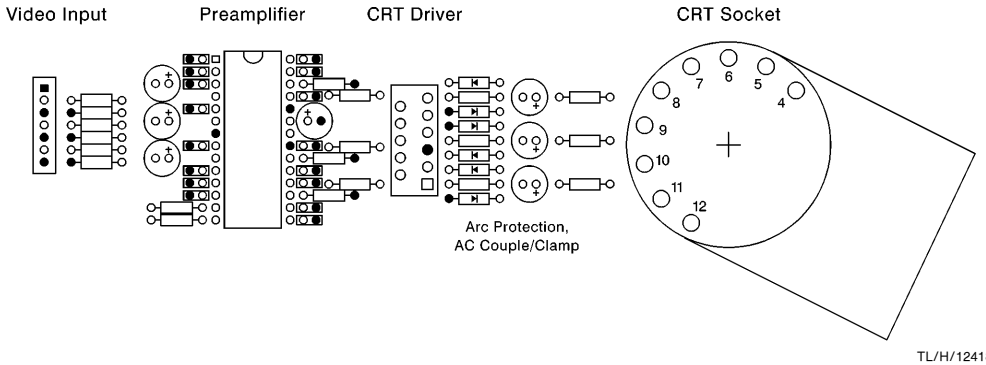


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**FIGURE 12. Ideal Video Channel Parts Placement**

After the parts are placed, the trace routing should be done using a prioritized list with the HF signals, power and ground at the top of the list. Following should be the low frequency signals and then finally any DC signals. Attention must also be paid to avoid coupling the HF signals unto the low frequency signal traces (crosstalk). Crosstalk will be discussed later in this article.

**Minimizing Loop Areas**

Looking at equation 2 we can see that emissions are proportional to the log of the loop area. Therefore, if the loop area is doubled, we should expect emissions from that particular loop to be doubled (6 dB higher). Looking at it from the other side, if we cut the loop area in half we should expect 6 dB lower emissions. Kirchoff's current law says that any current that is sourced from a circuit must return to it (the net current through any closed area must equal zero). Therefore we must pay attention to the complete current loop. In order to keep loop areas as small as possible, the following two guidelines should be followed:

1. All HF signal traces should be as short as possible.
2. All HF signals should have a return trace. On DS boards this can be through the ground plane. The ground plane should cover the complete trace length. On SS boards a return trace should be routed right next to the signal trace.

An area of exception is at the CRT driver outputs. Having a ground plane underneath these traces usually adds a significant amount of capacitance to the load. A 10 mil wide trace over a ground plane on a 60 mil thick PCB has about 1.25 pF of capacitance per inch in length. If the performance requirements do not allow this extra capacitance, the EMI design may require some additional shielding. The arc protection design may also require some isolation between the CRT ground and circuit ground. This was discussed in the section on grounding.

**Power Supply Filtering**

Proper power supply filtering (also called bypassing) on PCB's plays a vital role in the control of EMI. HF power supply currents supplied to fast circuits must be treated the same as HF signal currents. The HF currents can also cause voltage spikes which can be introduced as noise to other circuits. If these noise transients find their way past the I/O connector to a cable or wire, we can have an emissions disaster. Remember, we saw in our section on cabling that noise levels in the *tens of millivolts can cause problems*. The purpose of filtering the DC power on the PCB is to provide a local AC energy source where it is needed most and keep HF power transients from traveling to/from other circuits on the PCB or I/O cabling.

*Figure 13* shows a PCB that contains a high speed circuit (such as a video amplifier) that is supplied with DC power from another assembly or PCB. The power is connected through a wire bundle or cable. The PCB requires filtering at two points. The first place to filter is right at the power input connector. A large electrolytic capacitor (10 $\mu$F–100 $\mu$F typically) and one or more small ceramic capacitors (0.001 $\mu$F–0.1 $\mu$F) for high frequency filtering usually will do the job. The function of these capacitors is to replenish the energy drawn from the local bypassing located over the rest of the PCB which will relieve the power supply from doing this over a long distance (and generating some undesired emissions). The second place to filter is right next to the power and ground pins of high speed IC's or in areas of discrete circuits where HF transient currents are drawn. Ceramic capacitors (0.001 $\mu$F–0.1 $\mu$F) will do the job here. If the local IC or circuit also draws a significant amount of average current an electrolytic may also be required. This is typically the case for video preamps and CRT drivers. The power supply will also have its own filter caps to keep noise and ripple below the required levels.

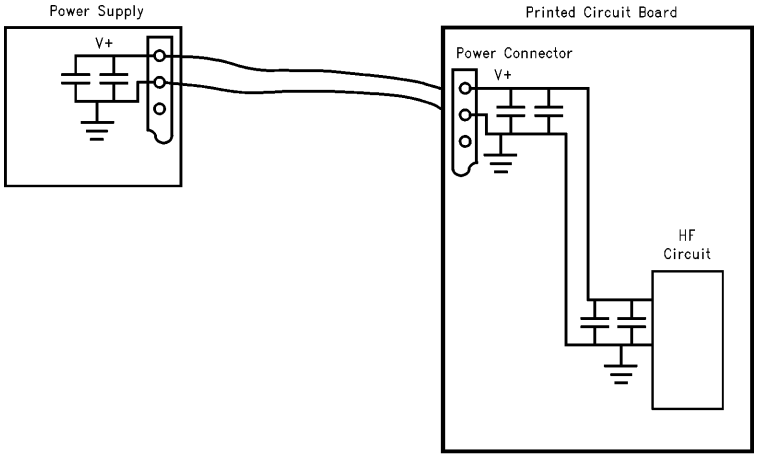


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**FIGURE 13. DC Power Supply Filtering Scheme**

One way to determine if the power supply filtering is adequate is to measure the noise voltage across our filters or between the power and ground pins of the critical IC. This can be done using a probe and oscilloscope. Be sure that the measurement system has enough bandwidth to take measurements over the frequency range of interest. If the noise level at specific frequencies is of interest (and it may be), a spectrum analyzer can also be used. Many oscilloscopes have a 50Ω output that can be connected directly to the spectrum analyzer input. Before taking the actual noise measurement it is important to determine how much noise the probe is picking up from near field radiation. This can be done by connecting both the signal and ground of the probe to the ground side of the filter cap across which the noise measurement will be taken (hopefully this is a low impedance ground plane). This measurement can then become our ''noise floor'' which the noise across the filter can be compared to. It is also very important to keep the ground lead of the probe as short as possible.

Other considerations for filtering are:

- Component leads should be as short as possible to minimize lead inductance.
- Local HF filter capacitors should be as close as possible to the power and ground leads of the IC it is supplying energy to in order to minimize the loop size of the circuit and the effects of trace inductance.
- Use the lowest value HF filter capacitor that provides enough energy for the circuit. This will move the self resonance of the circuit up in frequency.
- Ferrite can also be used for isolation between filters on a PCB. Please see the section on the use of ferrites.

**Power/Ground**

The main goals for the power and Ground distribution on a PCB are to keep loop areas as small as possible (for intended and unintended signals) and to provide low impedance distribution of power and ground so that it does not cause and distribute noise. For DS PCB's this is somewhat easier because we can put a ground plane on one side. It is important to remember that power supply current transients will radiate just like signal currents. I recommend the following guidelines for DS and SS boards.

For DS boards:

1. The power routing should be over the ground plane over its full length. Avoid as many discontinuities as possible (unfortunately we can't have a solid plane unless we could use all surface mount components).
2. Avoid routing power etch that feeds high speed circuits near the edge of the PCB where there won't be significant overlap of the ground plane. You may even consider routing a ground trace to the outside of the power trace.
3. Use as wide of etch as possible for power distribution in order to minimize trace inductance.

For SS boards:

1. Route power and ground right next to each other right from the input connector to the destination. Because space will be limited give priority to the high speed circuits. Remember that power supply current will radiate just like signal currents.
2. Use as wide of etch as possible for both the power and ground distribution in order to minimize trace inductance.

**Crosstalk**

HF signals can be coupled from one trace (source trace) to another (victim trace) on a PCB due to the capacitance between them. This is known as crosstalk. We can avoid crosstalk by not routing a second trace next to a high speed signal trace for any significant distance. As the length of the parallel run increases so will the capacitance between the traces and hence, the crosstalk. Crosstalk can be reduced by increasing the distance between the traces. Inserting a ground trace between the traces will significantly reduce crosstalk.

On DS PCB's, the close proximity of the victim trace to the ground plane will reduce crosstalk in comparison to a SS board due to the capacitance from the victim trace to ground. This capacitance reduces the impedance of the victim trace at high frequencies which will reduce crosstalk. For a more in depth study of crosstalk please refer to the references listed at the end of this application note.

**EMI PHILOSOPHY**

We have discussed many topics that are part of the EMI engineers tool kit which is used to predict, minimize and control emissions. We know from the relationships that we have discussed that the emissions potential is directly related to the performance of the display. In other words, as resolution, picture quality and edge speeds increase it will take a better EMI design to meet emissions requirements. In order to design for EMC (lack of EMI), emissions should be considered from the start of the product design cycle. In order to do this the complete system design must be considered. This includes the PC and graphics card at a minimum. The following list of guidelines has been put together for use throughout the product design cycle. It is not exhaustive, but hopefully the reader will find it of interest.

1. *The speed (rise and fall times) of the input video signal(s) should not be any faster than necessary*. This will minimize the HF energy in the input signals. Then the CRT display will have less HF signal to amplify and radiate. The speed of this signal is dependent on the PC graphics card design and therefore not under the control of the display designer. However, in the cases where the whole computer system is being designed together, we can work with the graphics card designer to target the desired video speed. If the monitor will be a stand alone product, then we can choose a graphics card that is designed to meet our performance criteria but is not over designed for the application.
2. *Don't use a higher bandwidth amplifier than necessary*. The video channel bandwidth should be adequate to provide the desired signal speed at the CRT cathode when driven by the selected graphics card. Having too much bandwidth will allow unnecessary HF signals (including noise) to be amplified, which will produce higher emission levels at these frequencies.

3. *Test printed circuit boards as soon as they are available*. There is no need to wait until the first monitor is completed. Testing early can flag a problem that can be corrected easier (and less expensively) earlier in the design cycle.
4. *Weigh the tradeoffs between EMI Design and product volume*. For high volume products fine tuning the EMI design will be worth the cost of the testing and troubleshooting necessary to minimize the unit cost of the EMI solution. For low volume products, it may cost more for testing and troubleshooting than will be saved in the unit cost over the life of the product. The length of the product design cycle must also be considered. There is always a limit to how much time can be spent reducing the unit cost of an EMI solution.
5. *It is easier to remove than add*. When doing your up front EMI design, if you think you need a shield, filter, ground connection or anything else, design it in or at least put in the provisions for it so you can easily add it. It can be very costly and painful to try to add a fix that the product won't accommodate. If you end up not needing the items, simply don't install them and remove the provisions for them during the next design update. No one will argue with you when you take things out.
6. *Before you test the monitor, know the emissions of the PC, graphics card and cable*. I recommend dividing the emission level allotment between the PC (with the graphics card and cable) and the CRT Display. Therefore, if our overall goal is 6 dB margin, the PC with the graphics card and a properly terminated video cable should have 12 dB margin when tested alone. If the PC system doesn't have much margin at video signal frequencies, passing the test with the monitor will be quite a challenge.

**ACRONYMS**

EMC — Electromagnetic Compatibility
EMI — Electromagnetic Interference
HF — High frequency
SS — Single-sided
DS — Double-sided
CRT — Cathode ray tube
PCB — Printed circuit board
SE — Shielding Effectiveness

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## SUBJECT INDEX



## TABLE INDEX



## FIGURE INDEX

**LIFE SUPPORT POLICY**

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