DP83905EB-AT AT/LANTIC™ Hardware Users' Guide

National Semiconductor
Application Note 897
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INTRODUCTION

The AT/LANTIC Ethernet controller provides a simple method of interfacing a PC ISA (Industry Standard Architecture) bus based system to Ethernet. The AT/LANTIC controller emulates a popular adapter card for PC compatibles: the Novell® NE2000 *Plus* card. The AT/LANTIC also implements a shared memory mode that provides added flexibility and performance. The high level of integration ensures a small and cost-effective solution. In order to use a network interface, driver software is required that is specific to the network interface and the network operating system. Since the AT/LANTIC is compatible with the most popular adapter cards, driver support is second to none.

ABOUT THIS GUIDE

This guide is written for hardware design engineers wishing to develop an Ethernet interface using AT/LANTIC. The guide is written in two sections. The first part is a step-by-step examination of the design process. The second section provides reference material with additional detailed information.

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1.0 DP83905 ETHERNET INTERFACE DESIGN

1.1 Design Decisions and Implementation Details

This section of the AT/LANTIC guide is intended to ask the designer to choose which options are best for each application, whether it is an adapter card, a motherboard or some other embedded design. (Note that Application Note AN-844 *"DP83905EB-AT AT/LANTIC™ Demonstration Board"* shows detailed schematics of an AT/LANTIC solution.)

1.1.1 ISA Bus Connection

The AT/LANTIC supports both 8- and 16-bit ISA bus configurations. An 8-bit interface is cheaper than 16-bit (less board space and only one SRAM), but has lower performance. There are three options for connecting the bus interface as described:

1. For an 8-bit interface, pins SD8–15, SBHE, LA17–23, MWR, MRD, M16, and I016 should be left unconnected, and DWID should be tied low.
2. For a 16-bit interface, DWID should be tied high.
3. For a 16-bit adapter card that can be used in 8- and 16-bit slots, DWID should be connected to pin D29 of the ISA bus. In a 16 bit slot this is +5V. In an 8-bit slot, this is unconnected, and a pull-down within AT/LANTIC will ensure that 8-bit mode is selected.

1.1.2. Interrupts

The AT/LANTIC has 4 dedicated interrupt output pins. This allows the user to select the required interrupt without changing jumpers on the board. In some applications, the choice of 4 interrupts may not be sufficient. The AT/LANTIC allows you to use an external decoder to expand the choice to 8 interrupts.

For 4 interrupts, connect each of the pins INT0–3 directly to the interrupt signals. We strongly recommend using the following scheme to promote software compatibility across AT/LANTIC platforms:

AT/LANTIC	PC
INT0	IRQ3
INT1	IRQ4
INT2	IRQ5
INT3	IRQ9

Configuration register C bit 5 "INTMOD" should be set to "0" (see Section 1.1.9).

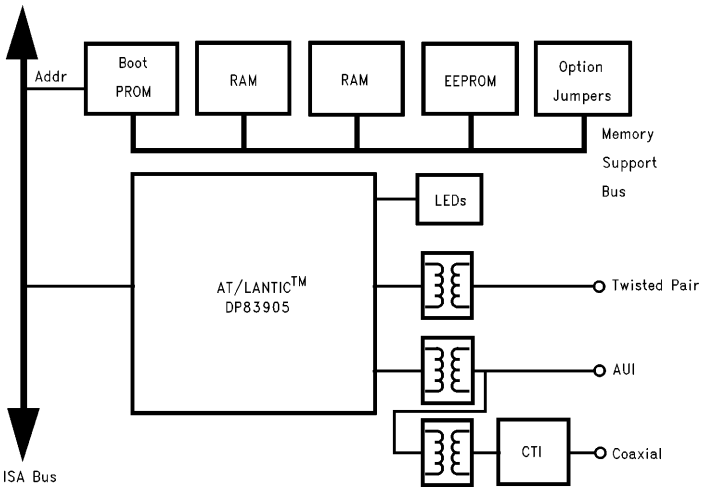

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FIGURE 1. Simplified Block Diagram of AT/LANTIC Application

For 8 interrupts, an external decoder is required. This decoder must have the following properties:

INT0–2 selects which 1 of the 8 outputs is driven. This output follows the logic level of INT3. The 7 unselected outputs must remain high impedence.

The decoder outputs are connected to 8 ISA interrupts. We recommend using the following scheme to promote software compatibility across AT/LANTIC platforms:

AT/LANTIC			PC
INT2	INT1	INT0	
0	0	0	IRQ3
0	0	1	IRQ4
0	1	0	IRQ5
0	1	1	IRQ9
1	0	0	IRQ10
1	0	1	IRQ11
1	1	0	IRQ12
1	1	1	IRQI5

Configuration register C bit 5 ''INTMOD'' should be set to ''1'' (see Section 1.1.9). The 8 interrupt mode interface can be implemented in a single GAL as shown in *Figure 2.*

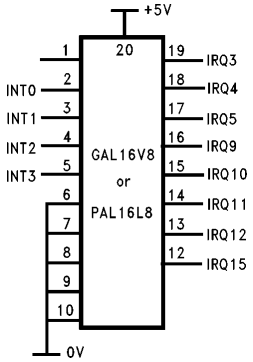

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FIGURE 2. GAL/PAL Circuit Diagram

The PAL or GAL equations should be:

```
IRQ3 = INT3;
IRQ4 = INT3;
IRQ5 = INT3;
IRQ9 = INT3;
IRQ10 = INT3;
IRQ11 = INT3;
IRQ12 = INT3;
IRQ15 = INT3;
IRQ3.oe  = /INT2 & /INT1 & /INT0;
IRQ4.oe  = /INT2 & /INT1 &  INT0;
IRQ5.oe  = /INT2 &  INT1 & /INT0;
IRQ9.oe  = /INT2 &  INT1 &  INT0;
IRQ10.oe =  INT2 & /INT1 & /INT0;
IRQ11.oe =  INT2 & /INT1 &  INT0;
IRQ12.oe =  INT2 &  INT1 & /INT0;
IRQ15.oe =  INT2 &  INT1 &  INT0;
```

1.1.3. Buffer RAM

The standard RAM sizes for 8- and 16-bit cards are 8k and 16k respectively, using one or two 8k x 8 RAMs. The AT/LANTIC will also support the use of 32k x 8 RAMs giving 4 times the standard RAM capacity. Using additional memory can provide a performance boost in server applications.

Note that the use of 32k x 8 RAMs will make the design INCOMPATIBLE with NE2000.

For 8k x 8 RAMS, MSA1–13 are used. Configuration register C bit 4 ''COMP'' should be set to ''0''.

For 32k x 8 RAMS, MSA1–15 are used. Configuration register C bit 4 ''COMP'' should be set to ''1''.

When making an 8-bit-only interface, only one RAM is required, connected to MSD0–7. For a standard ISA bus configuration, 100 ns RAMs, or faster, should be used. Details of how to calculate RAM speeds are given in Section 2.5.

1.1.4 Crystal/Oscillators

1.1.4.1 20 MHz Clock

AT/LANTIC requires a 20 MHz ±0.01% clock. Both crystal and oscillator solutions are supported. In general, a crystal solution is cheaper, however if a suitable clock is already available on your board, it could be used.

To use a crystal, use the following circuit.

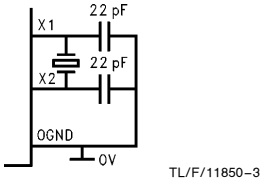

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FIGURE 3. Crystal Circuit

The value of the capacitors should be 26 pF minus the printed circuit board trace capacitance. (Typical trace and pin capacitance is about 4 pF).

1. Note that the following rules should be applied:
2. The signal traces should be short.
3. The ground return path to the capacitors should be short, and should connect to the AT/LANTIC OGND pin.
4. There should not be other signal traces through the region of the crystal.
5. It may help to place a ground plane under the crystal.
6. The crystal should conform to the following specifications:
   - AT cut parallel resonant crystal
   - Series resistance ≤ 25Ω
   - Specified load capacitance ≤ 20 pF
   - Accuracy 0.005% (50 ppm)
   - Typical load 50 μW–75 μW
7. Do not connect X1 or X2 to anything else.

Alternately, an oscillator may be used. If used the oscillator output should be connected directly to X1. X2 should be left unconnected. The clock should be better than 40:60 duty cycle, and should have a good quality waveform.

1.1.4.2 BSCLK

The AT/LANTIC core can be clocked either by the 20 MHz clock, or by a separate clock input ''BSCLK''. The maximum clock rate is 20 MHz, so the 20 MHz clock is usually used.

To use the 20 MHz clock, connect the BSCLK pin to 0V, and set Configuration register C bit 6 ''CLKSEL'' to ''0''. To use another clock source, connect the clock source to the BSCLK pin, and set Configuration register C bit 6 ''CLKSEL'' to ''1''. See Section 1.1.9 for more information about configuration data.

1.1.5 Boot ROM (Remote Program Load PROM)

Depending on the intended use of your design, you may wish to provide a boot PROM, or a socket for a boot PROM. A boot PROM allows the PC to load the operating system from a server on the network, without needing a disk drive on the PC. AT/LANTIC supports boot PROM sizes of 8k, 16k, 32k and 64k. The AT/LANTIC also supports the use of FLASH ROM through the use of a write signal. This may be used to allow in-situ programming, or updating of boot PROM code by the user.

Adaptor cards are typically supplied with an empty boot PROM socket. Boot PROMs are available from network operating system vendors or third parties. They are typically 8 kbytes or 16 kbytes in a 28-pin package. The boot prom size can be configured by the user to be any size and at any address between C0000h and DFFFFh, using configuration register C bits 0–3 ''BPS0–3''.

Configuration register B bit 6 ''BPWR'' specifies if the AT/LANTIC will allow write access to the PROM: ''0'' = read only, ''1'' = write enabled. (See Section 1.1.9, Configuration.)

For a standard ISA bus configuration, 250 ns PROM, or faster, should be used. Details of how to calculate boot PROM speeds are given in Section 2.5.

1.1.6 Cable Interfaces

AT/LANTIC supports three types of cable interface:

TPI 10Base-T, Twisted Pair

AUI for connection to 10Base5, also known as ''thick'' Ethernet

Coax 10Base2, also known as thin Ethernet

The TPI interface connects to the AT/LANTIC as follows:

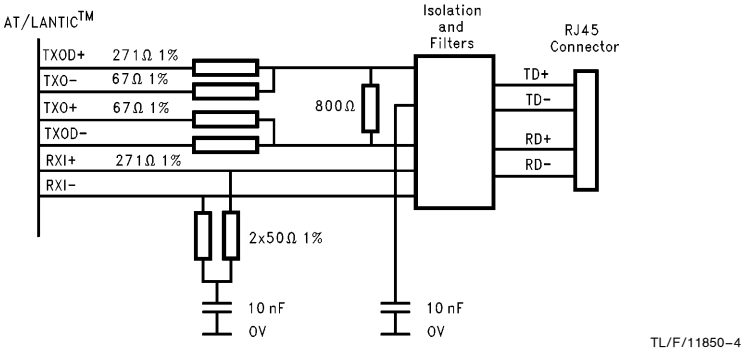

FIGURE 4. Twisted Pair Interface

The AT/LANTIC selects between the AUI/coax interfaces and TPI internally. Note that, in addition to 10Base-T compatible twisted pair, the AT/LANTIC supports the use of higher loss cable systems. This allows cables to be longer than the 10Base-T specification, or allows the use of shielded cables. Refer to Section 4.8 of the AT/LANTIC data sheet.

The AUI interface requires an isolation transformer, and resistors, as shown in *Figure 5.* The AUI interface enables the use of an off board transceiver to connect to other types of media such as Thick Ethernet or Fiber Optic cabling.

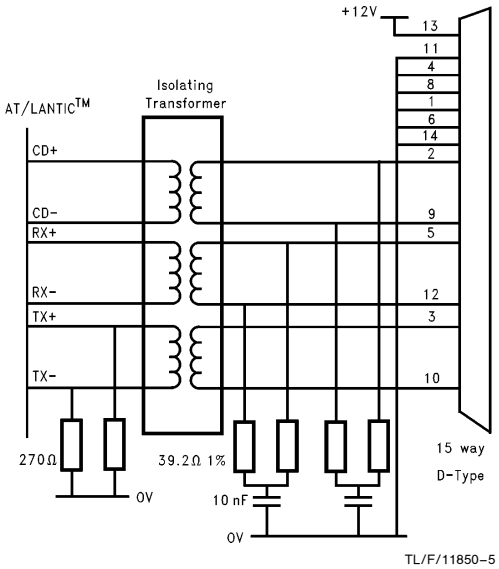

FIGURE 5. AUI Interface Circuit

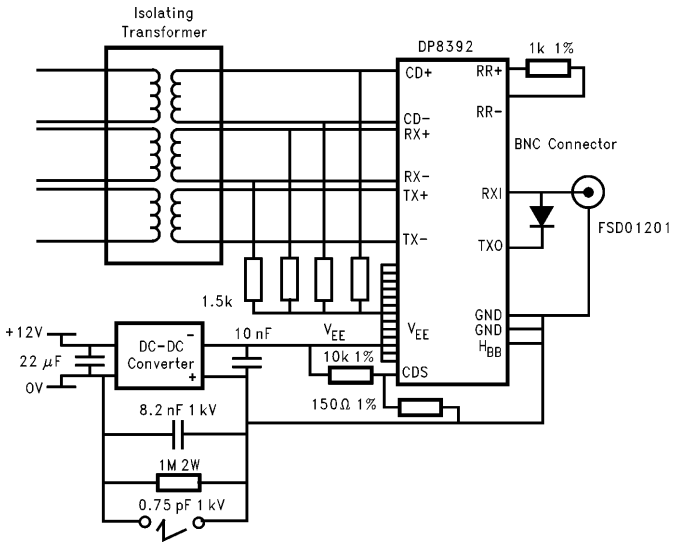

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FIGURE 6. Coax Interface Circuit

The Coax interface requires an isolation transformer, a DC-DC converter and the DP8392 Coax Transceiver Interface as shown in *Figure 6*.

If it is desirable to implement a design that supports both AUI and Thin Ethernet cabling schemes, and provides for selection between the two interfaces the coax interface should connect to the AUI interface as shown in *Figure 7*. In order to use the AUI connector, the coax interface must be disabled. AT/LANTIC selects AUI or coax with an output pin, called ''THIN''. This signal is used to switch-on the DC-DC converter of the coax interface when THIN is high. When coax is selected, an AUI cable must not be connected to the AUI connector.

Figure 7 shows a DC-DC converter with an enable input. A DC-DC converter without an enable input can be used, if the supply to the converter is switched by an FET.

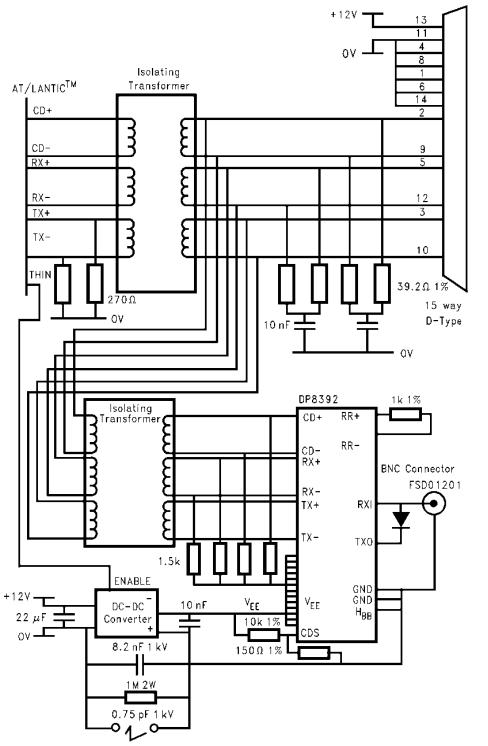

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FIGURE 7. AUI and Coax Interface Circuit

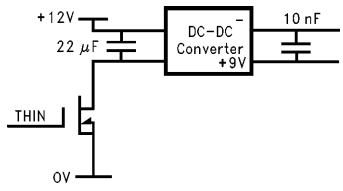

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FIGURE 8. FET Switch for DC-DC Converter

The cable interfaces utilize a number of magnetic components as shown in the previous figures. The specifications for these components are shown below.

AUI and Coax Interface isolation transformer:

1:1 turns ratio

100 μH inductance

500V isolation

Coax DC-DC converter:

+12V input (could use +5V connected to the +5V supply)

9V output voltage

200 mA output current

500V isolation

Active-high enable input (if required)

The 10BASE-T interface uses an integrated Filter-Transformer-Choke combination.

Specific component recommendations are listed in the Local Area Networks Data Book in the Magnetics Vendors Application Note.

1.1.7 LED Interface Options

AT/LANTIC has dedicated outputs for driving several LEDs. These outputs are capable of a maximum current per LED output of 16 mA. Do not decrease the resistor value below 330Ω, or the AT/LANTIC maximum current will be exceeded.

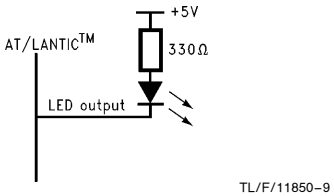

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FIGURE 9. LED Circuit

It may be desirable to connect LEDs to any or all of the possible outputs. When used the LEDs can provide the following information:

TxLED Transmit activity

RxLED Receive activity (all packets on network)

COLED Collision

GDLNK TPI Link Ok, or testing disabled

POLED TPI Polarity reversed

In some cases the polarity of the LED is reversed from that which the designer would like to use (e.g., the LED is off under a condition that the designer would like it to be on). To handle this, it is possible to use the following circuit, *Figure 10,* to invert the meaning of an LED (e.g., instead of a ''Good Link'' LED the LED can be defined as ''Link fail''):

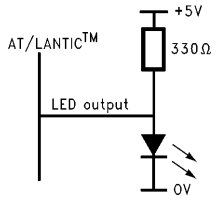

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FIGURE 10. Inverted LED Circuit

1.1.8 Low Power

In some portable applications it is necessary to shut-off subsystems in order to conserve power. AT/LANTIC has been designed so that it is possible to remove the power from the majority of the chip whilst still powering the ISA interface circuit, thus protecting the ISA bus. In low power state, the current drain is less than 100 μA.

If ''Low Power'' is not required, tie the LOWPWR pin to 0V.

If ''Low Power'' operation is required, the following must be noted:

1. An external device is required to disconnect the $PLLV_{CC}$, PV_{CC}, OV_{CC} and V_{CC} pins. This device must have a low voltage drop when ''on''. A suitable device is the NDS9400 which has a 0.25Ω on-resistance.
2. When the supply to the $PLLV_{CC}$, PV_{CC}, OV_{CC} and V_{CC} pins is turned off, the LOWPWR pin must be driven high. This disables internal buffers and reduces current drain to a minimum.
3. When recovering from low power state to normal operation, after restoring the power and driving LOWPWR low, the RESET pin must be driven high for more than 400 μs to reset the controller.
4. Note that the DWID pin has an internal pull down. If this is tied high for 16-bit operation, it should be tied to the switched V_{CC} to minimize current drain in the low power state.

1.1.9 Configuration

Three registers in the AT/LANTIC are loaded with configuration data at reset. This configuration specifies all the design choices (e.g., 4 or 8 interrupts) and the user installation choices (e.g., the I/O address).

This data can either be stored in the EEPROM, or be specified by resistors optionally connected to the CA0–7, CB0–7 and CC0–7 pins (also known as MSD0–15 and MSA1–8).

The benefits of the Jumperless EEPROM solution are that it is smaller and cheaper (no resistors or jumpers), and that the user can change the configuration without opening the computer. This may be especially important in a motherboard application. Additionally, the software used to change the configuration can attempt to check for address conflicts etc., and protect the user from making mistakes.

One potential problem with this solution, for adapter cards, is that the default settings as shipped may cause an address conflict in some cases. Such a conflict would prevent accesses to the card which are needed to change the address to a safe one.

To overcome this problem, AT/LANTIC has a ''disabled'' option. Configuration software can find an I/O address that is free, and then wake up the AT/LANTIC. Whilst disabled, AT/LANTIC monitors I/O accesses to 278h (a printer port). On the fourth consecutive write to 278h, AT/LANTIC loads the configuration from the write data, and wakes up.

The benefits of the Jumpered solution are that no software is needed to set the configuration. This may be important to system builders when choosing an adapter card, for whom jumpers may be faster to use than software.

Whichever configuration method you choose, you will need to determine, for each configuration bit, what the default value should be, and whether the bit can be changed by a user or is fixed by design. The following tables may assist you in this. Note that a full description of each configuration bit can be found in Section 5 of the AT/LANTIC data sheet.

Bit	Use
Config A:	
0	I/O Address
1	I/O Address
2	I/O Address
3	Interrupt
4	Interrupt
5	Interrupt (if 8 selected)
6	Fast read (See Section 1.1.9)
7	NE2000/Shared Memory
Config B:	
0	AUI/Coax/TPI
1	AUI/Coax/TPI
2	Good Link Test Disable
3	IO16 Bug Fix Enable
4	IO CHRDY Bug Fix Enable
5	—
6	Boot PROM Write Enable
7	—
Config C:	
0	Boot PROM Addr and Size
1	Boot PROM Addr and Size
2	Boot PROM Addr and Size
3	Boot PROM Addr and Size
4	RAM Size 8k or 32k
5	4 or 8 Interrupts
6	Core CLK = 20 MHz or BSCLK
7	Allow Access to Configure Regs(1)

Note 1: Config C bit 7 ''SOFTEN'' allows configuration software to read and write config registers A & B. Any changes to the config registers are overwritten by the EEPROM or jumper configuration the next time that the AT/LANTIC is fully reset. If access to the contig registers is disabled, it is also not possible to change the EEPROM contents.

To implement a Jumperless (EEPROM) solution, the EECONFIG pin should be tied to +5V. The default configuration must be programmed into the EEPROM during manufacture. See Section 1.3 for details of how to program the EEPROM.

If config register C bit 7 ''SOFTEN'' is ''0'':

1. Config registers A and B can be examined by software (to check the configuration).
2. Config registers A and B can be modified by software to temporarily change the adapter settings. The settings are resored to the values in the EEPROM when the AT/LANTIC is next fully reset.
3. The values for config registers A, B and C that are held in the EEPROM can be changed by software. This can include setting config register C bit 7 to ''1'', which will prevent further access to config registers. If this is done, the settings can only be changed again if AT/LANTIC is reset with EECONFIG pulled low (i.e., jumpered mode).

If config register C bit 7 ''SOFTEN'' is ''1'':

1. Config registers A and B cannot be read or written by software.
2. The values for config registers A, B and C that are held in the EEPROM cannot be changed by software.

To implement a Jumpered solution, the EECONFIG pin should be tied to 0V. For each configuration bit you must define the state of the corresponding AT/LANTIC pin at reset. If the bit is fixed by design, you should connect 47k or 10k pull-up for a ''1'', or leave alone for a ''0''. If it is user-selectable, you should connect a pull-up via a jumper.

If config register C bit 7 ''SOFTEN'' is ''0'':

1. Config registers A and B can be examined by software (to check the configuration).
2. Config registers A and B can be modified by software to temporarily change the adapter settings. The settings are restored according to the jumpers when the AT/LANTIC is next fully reset.

If config register C bit 7 ''SOFTEN'' is ''1'':

1. Config registers A and B cannot be read or written by software.

OTHER CONFIGURATION OPTIONS

There are two other methods of configuring the AT/LANTIC. If using these methods, the interface will not properly emulate NE2000 adapter cards, and will not work with standard drivers.

Partially Jumpered Solution: This is a jumpered solution where only some of the options are jumpered, e.g., I/O address and boot PROM address. Since configuration registers A and B can be rewritten by software, a program could be used to complete the configuration process as part of the software boot sequence.

No EEPROM, partially jumpered solution: This is the same as the above solution, except that the EEPROM is not fitted. The purpose is to reduce cost. In this case, there is no Ethernet node address available, so a non-standard driver is required, which obtains its Ethemet address from another source.

1.2 Layout Considerations

1.2.1 ISA Bus

In a multi-layer PCB with good ground plane, there should be little risk of difficulty due to layout. However, if a 2 layer design is envisaged, a lot of care is required for the ground track routing. The AT/LANTIC drives 16 data lines (SD0–15) with fast high-current drivers. Ground routing should be arranged as a grid, so that there is a good return current path between the AT/LANTIC and all the ISA bus 0V connections.

1.2.2 Twisted Pair (TPI)

The length of tracks in the TPI circuit should be kept short and straight, and the lengths of the differential signal tracks should be kept approximately equal. If using a multi-layer board, the power and ground planes should be removed in the area of the TPI to reduce capacitive coupling of noise from the power planes. The area should not have other signals passing through it. It may be desirable to have chassis ground used around the area of the connector to provide a shield for EMI noise radiation.

Tracks between the filter/isolation transformer and the RJ45 ''telephone'' socket should have an isolation barrier of at least 2mm to any other track or component.

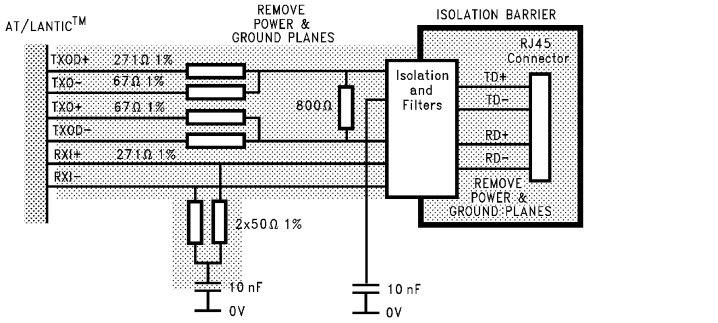

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FIGURE 11. TPI Layout

1.2.3 Attachment Unit Interface (AUI)

Tracks should be kept short and straight where possible. The D-type shell (and the metal bracket it is fitted to) should be connected to digital ground via a 10 nF capacitor.

1.2.4 Thin Ethernet (Coax)

The DP8392C Coax Tranceiver Interface should be placed close to the BNC connector, so that the connection between them is short. There should be no other tracks in this area, and on multi-layer PCBs the power and ground layers should be removed.

The DP8392CV requires an area of copper on the PCB surface to act as a heatsink. This is documented in the DP8392CV data sheet.

All the coax interface components between the isolation transformer and the BNC must be surrounded by an isolation barrier of at least 2mm, which must include the power and ground layers of a multi-layer PCB. The isolation transformer and the DC-DC converter bridge the isolation barrier, plus a resistor, a capacitor and a spark gap. On a multi-layer PCB the isolated power and ground planes should be used for VEE and ISOLATED__GND.

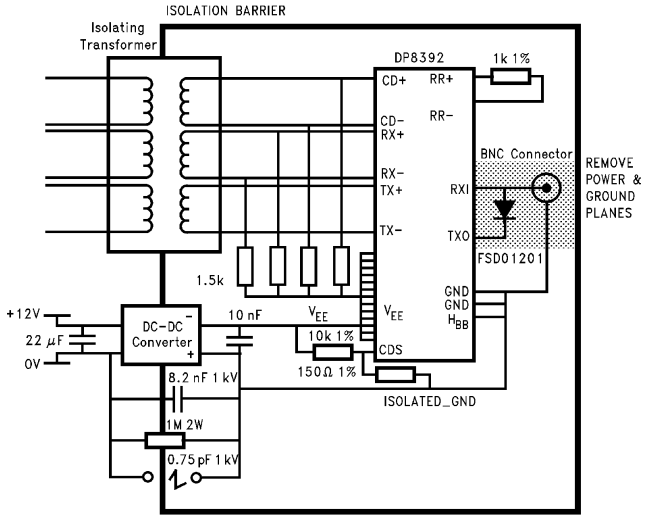

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FIGURE 12. Coax Layout

1.2.5 PLL

In order to improve performance of the receiver PLL, the PLL supply pin should be connected via a simple RC filter, located close to the AT/LANTIC $PLLV_{CC}$ pin.

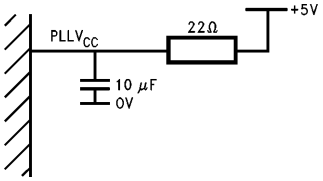

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FIGURE 13. PLL Supply Decoupling

1.3 EEPROM Programming

Initial values must be placed in the EEPROM before it can be used. The following table shows the EEPROM address map (all values in HEX):

Addr	Bits 15–8	Bits 7–0
00	Node Addr 1	Node Addr 0
01	Node Addr 3	Node Addr 2
02	Node Addr 5	Node Addr 4
03	Checksum	05 (8013 Type)
04	00 (Not Used)	00 (Not Used)
05	00 (Not Used)	00 (Not Used)
06	00 (Not Used)	00 (Not Used)
07	57 (ASCII "W")	57 (ASCII "W")
08	42 (ASCII "B")	42 (ASCII "B")
09	00 (Not Used)	00 (Not Used)
0A	00 (Not Used)	00 (Not Used)
0B	00 (Not Used)	00 (Not Used)
0C	00 (Not Used)	00 (Not Used)
0D	00 (Not Used)	00 (Not Used)
0E	Config B	Config A
0F	73H (Note 1)	Config C

Note 1: In initial documentation in the data sheet this byte was listed as having a value of FFH. In order to accomodate future expansion of features on the AT/LANTIC, this byte should be programmed with a 73H.

In a jumperless solution, Config A, B and C values must be set according to the default configuration, as discussed in Section 1.1.9.

Config A, B and C are ignored in a jumpered configuration.

The Checksum is calculated so that the least significant byte of the sum of the first 8 bytes in the EEPROM is FF (hex).

i.e., (Node Addr 0
+ Node Addr 1
+ Node Addr 2
+ Node Addr 3
+ Node Addr 4
+ Node Addr 5
+ 05
+ Checksum) and FFh = FFh

The Ethernet node address must be unique to each unit produced.

Note that only Config A, B and C bytes can be changed by user software.

How to Program the EEPROM

The simplest way to program the EEPROM is before it is fitted into the PCB.

In some cases, however, it may be preferable to be able to program the EEPROM after board manufacture. This requires either a special programming connector on the PCB, or a "bed of nails" programming jig to access signals on the board. Additionally, a series resistor is required in the EECS signal between AT/LANTIC and the EEPROM.

To program the EEPROM, power must be applied to the PCB and the RESET pin must be forced high on AT/LANTIC. You can then apply the programming waveforms to the EEPROM.

Refer to the 93C06 data sheet for programming details.

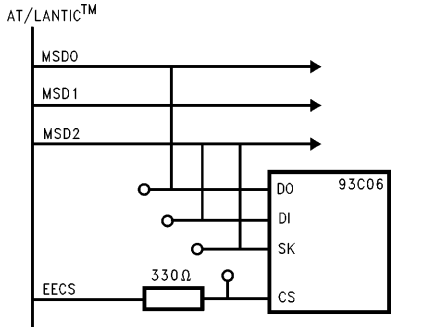

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FIGURE 14. EEPROM In-Situ Programming

1.4 Additional End-User Requirements

The end user may require some of the following items:

1.4.1 Configuration Software

If you are offering a jumperless solution, the user will require configuration software. National Semiconductor is able to offer source code for a configuration software package.

Configuration software is unnecessary for jumpered solutions.

1.4.2 Driver Software

You may wish to offer drivers with your solution. National Semiconductor offers a selection of drivers for popular network operating systems—contact your representative for the latest list. At the time of printing, National Semiconductor offers the following drivers:

Novell Netware ODI for DOS
Novell Netware ODI for OS/2
Novell Netware ODI for server
NDIS 2.0
NDIS 3.0 (available soon)
SCO UNIX
PC TCP Packet Driver

1.4.3 Documentation (Installation Guide)

We suggest that your documentation includes the following topics:

Configuration

If you have a jumpered solution, the user will have no software assistance, and you will have to document how to choose addresses and interrupts without causing conflicts, and how to set the jumpers.

In a jumperless solution, some assistance is given by the configuration program in determining addresses and interrupts currently in use. You will have to document how to run the software, and, for adapter cards, how to cope with installation into systems that require manual installation (for example, it may not be possible to detect I/O space usage if there are no pull-ups on the data bus).

Bus Compatibility Modes

Some PC's use chip sets that have impossible timing requirements. If this is the case, the driver or configuration software tests will report a problem with the buffer RAM.

In machines with this timing problem, AT/LANTIC offers two ''fixes''. We recommend trying the ''IO16'' fix first. If that is not successful, use the ''CHRDY'' fix instead.

See Section 2.3.6 for a description of how these ''fixes'' work.

SOFTWARE INSTALLATION

You may wish to describe how to install the configuration and driver software in a typical application.

2.0 REFERENCE INFORMATION

2.1 Architecture

2.1.1 NIC Core

The AT/LANTIC controller contains a DP8390 NIC (Network Interface Controller) core. This controller was used as a discrete part on the NE2000 and WD Ethercard Plus adapter cards. The operation of the NIC core is fundamental to the NE2000, WD Plus and consequently the AT/LANTIC.

All packets transmitted and received are sent via a dedicated buffer memory. A ''local'' DMA controller within the NIC transfers the data between the buffer RAM and the NIC's serializer/deserializer. This approach means that there are no critical performance requirements placed on the host computer (i.e., the PC).

At initialization time, the network software (the driver) tells the NIC to reserve a section of the buffer RAM for receive packet data. Since packets may be received without warning, the receive buffer is usually as large as possible. The NIC uses the receive buffer as a cyclic buffer, and maintains hardware pointers to put data in the correct place and ensure that data not yet read by the host is not overwritten.

When transmitting a packet, the host places the data into the buffer RAM (not in the receive buffer area), and issues a transmit command to the NIC, specifying RAM start address and length.

The host may access the buffer RAM in one of two ways:

Using the remote DMA channel: The NIC has another DMA controller for host transfers. This allows the host to transfer a block of data to or from the buffer RAM by writing to or reading from a single data transfer port. The NE2000 adapter uses this technique. The data transfer port is I/O mapped, and this method is often called ''I/O MODE''.

Memory mapped: Alternatively, the buffer memory can be mapped into the host address space. This allows the host to directly access any buffer RAM location. Each access requires arbitration between the NIC and the host. This method is used by the WD Plus adapter, and is commonly refered to as ''SHARED MEMORY MODE'' because the memory is shared between the NIC and the host.

In the AT/LANTIC, all arbitration and handshaking is handled internally for both I/O and Shared Memory modes.

2.1.2 NE2000

The key features of the NE2000 are:

1. The NIC registers and the data transfer port are I/O mapped on the ISA bus.
2. The boot PROM is memory mapped on the ISA bus.
3. There is an Ethernet address PROM mapped onto the NIC buffer RAM bus. The PROM is 32 bytes, but only 16 bytes can be read. Which 16 bytes depends on whether the card is in an 8- or 16-bit slot.

In the AT/LANTIC, the Ethernet address PROM is implemented as registers, which are loaded at reset from the EEPROM.

2.1.3 Shared Memory Mode

The key features of the shared memory mode are:

1. NIC core and ''shared memory control registers'' are I/O mapped on the ISA bus.
2. A PROM containing Ethernet address is also I/O mapped on the ISA bus.
3. Buffer memory is memory mapped on the ISA bus at an address determined by the ''shared memory control registers''.
4. The boot PROM is memory mapped on the ISA bus.

In the AT/LANTIC, the Ethernet address PROM is implemented as registers, which are loaded at reset from the EEPROM.

It should be noted that although the shared memory mode is hardware compatible with the WD Plus architecture, drivers written by WD/SMC check for a specific IEEE address range before enabling the driver.

2.2 Memory and I/O Maps

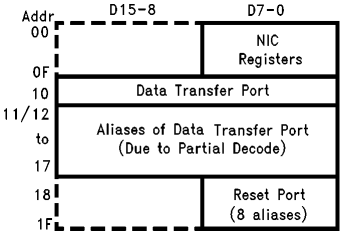
Please refer to Section 5 of the AT/LANTIC data sheet for details of how to use the registers shown here.

2.2.1 NE2000 8-Bit and 16-Bit

The ISA I/O map comprises a block of 32 addresses which can be located at one of 7 base addesses (240h, 280h, 2C0h, 300h, 320h, 340h and 360h).

The NIC registers and reset port are BYTE wide.

The data transfer port is the same width as the interface.



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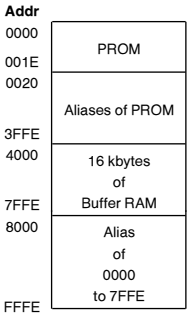
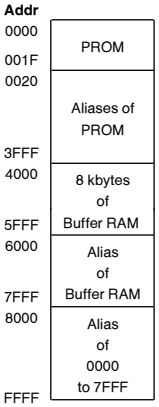
The NIC buffer memory map varies according to the RAM size, and also the interface width as programmed into an NIC register. This register should be set according to whether the interface is 8- or 16-bit.

Note that an 8 bit interface can be either an 8-bit design or a 16-bit adapter in an 8-bit slot.

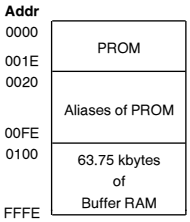
8k x 8 RAMs, 16-Bit Interface



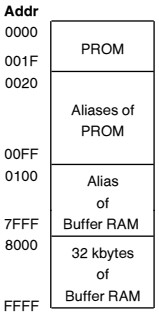
8k x 8 RAMs, 8-Bit Interface



32k x 8 RAMs, 16-Bit Interface



32k x 8 RAMs, 8-Bit Interface



The PROM is always read-only.

In a 16-bit configuration, the PROM is arranged as follows:

Addr	D15–8	D7–0
00	Invalid	Node Addr 0
02	Invalid	Node Addr 1
04	Invalid	Node Addr 2
06	Invalid	Node Addr 3
08	Invalid	Node Addr 4
0A	Invalid	Node Addr 5
0C to 1A	Invalid	00h
1C	Invalid	42h/57h*
1E	Invalid	42h/57h*

In an 8-bit configuration, the PROM is arranged as follows:

Addr	D7–0
00	Node Addr 0
01	Node Addr 0
02	Node Addr 1
03	Node Addr 1
04	Node Addr 2
05	Node Addr 2
06	Node Addr 3
07	Node Addr 3
08	Node Addr 4
09	Node Addr 4
0	Node Addr 5
0A	Node Addr 5
0C to 1B	00h
1C	42h/57h*
1D	42h/57h*
1E	42h/57h*
1F	42h/57h*

*The value found at PROM addresses 1C to 1F is determined by the logic level on the DWID pin:

42h (“B”) if DWID = 0 8-bit (byte) interface

57h (“W”) if DWID = 1 16-bit (word) interface

The NIC must be programmed for 8- or 16-bit operation before it is possible to read the PROM. It is therefore normal practice for software to set 8-bit mode and read the PROM using 8-bit I/O instructions in order that the actual bus size can be determined from the value at PROM address 1C–1F.

2.2.2 Shared Memory Mode

The ISA I/O map comprises a block of 32 addresses which can be located at one of 7 base addresses (240h, 280h, 2C0h, 300h, 320h, 340h and 360h).

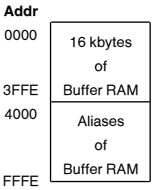
All the registers are BYTE wide.

Addr	D7-0	
00	Control 1	
01	AT detect	(Read only)
02	Unused	
03	Unused	
04	Unused	
05	Control 2	
06	Unused	
07	Unused	
08	Node Addr 0	(Read Only)
09	Node Addr 1	(Read Only)
0A	Node Addr 2	(Read Only)
0B	Node Addr 3	(Read Only)
0C	Node Addr 4	(Read Only)
0D	Node Addr 5	(Read Only)
0E	05h	(Read Only)
0F	Checksum	(Read Only)
10 to 1F	NIC registers	

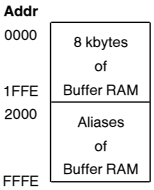
The NIC buffer memory map varies according to the RAM size, and the bus width which is programmed into an NIC register. This should be set according to whether the interface is 8- or 16-bit. The bus size is detected by the hardware on the DWID pin. This information is available to software by reading the AT Detect register.

Note that an 8-bit interface can be either an 8-bit design or a 16-bit adapter in an 8-bit slot.

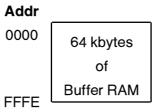
8k x 8 RAMs, 16-Bit Interface



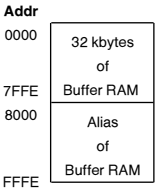
8k x 8 RAMs, 8-Bit Interface



32k x 8 RAMs, 16-Bit Interface



32k x 8 RAMs, 8-Bit Interface



2.3 ISA Bus Description

This section is a brief tutorial for those unfamiliar with the ISA bus.

For the most part, the ISA bus should be considered asynchronous. There are two ISA bus address spaces: I/O and memory.

2.3.1 I/O Cycles

I/O cycles are generated when the CPU performs IN or OUT instructions. An I/O cycle is signalled on the bus by IORD (read) or IOWR (write) strobes being active (low). During IORD or IOWR cycles, the address is given on SA0–9. I/O devices must qualify the IORD or IOWR strobe with a valid address, and the AEN signal, which must be low.

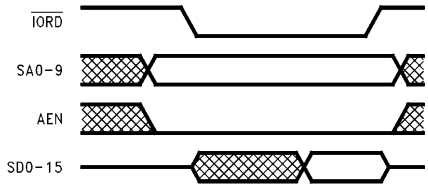


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FIGURE 15. I/O Read Cycle

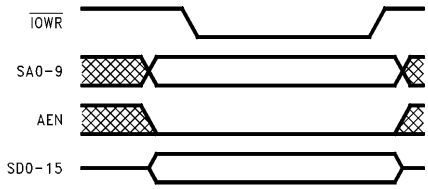

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FIGURE 16. I/O Write Cycle

2.3.2 Memory Cycles

Memory cycles are generated when the CPU performs MOV instructions. In most PC systems, memory accesses to system RAM are private to the motherboard and do not cause ISA bus activity.

Thus it is usual to only see accesses to devices on the ISA bus.

Similar to I/O cycles, memory cycles have memory read and write strobes. Unlike I/O cycles, however, there are two of each.

For an 8-bit adapter card, memory strobes SMRD and SMWR are used, together with address SA0–19. This allows the memory device to decode any address range in the bottom 1 Mbyte of the CPU address space. SMRD and SMWR strobes are not active for memory accesses above 1 Mbyte (≥100000h).

For a 16-bit adapter, memory strobes MRD and MWR are used. These are active for memory accesses to any address. The adapter card must therefore additionally test address lines LA17–23.

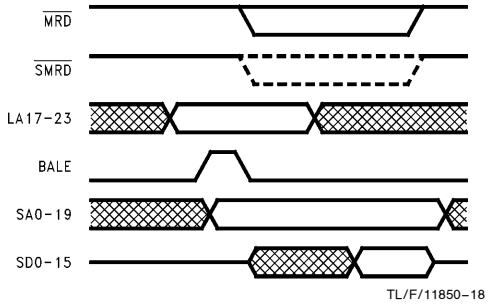

FIGURE 17. Memory Read Cycle

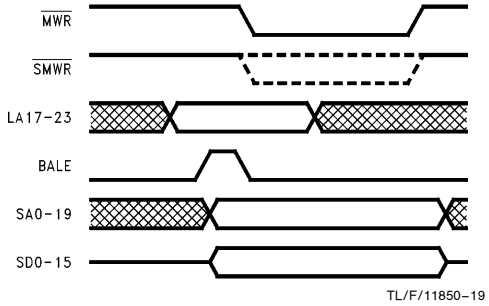

FIGURE 18. Memory Write Cycle

2.3.3 Cycle Timing

For all cycles, the system will use a set of default timings. These vary according to whether the access is I/O or memory, and whether the adapter card is 8- or 16-bit.

Adaptor cards can extend any cycle beyond the default timing by driving the CHRDY (Channel Ready) signal to 0V (meaning not ready). The cycle will be extended until CHRDY is released. A pull up on the system board pulls CHRDY high again—adapter cards are not allowed to drive it high.

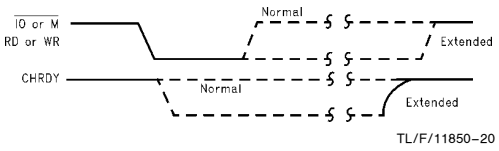

FIGURE 19. Extended ISA Cycle

Some cycles can also be shortened by adapter cards by driving a signal OWS low. This signal is not used by AT/LANTIC.

2.3.4 8-Bit and 16-Bit Cycles

For all cycles, the system will assume that an 8-bit device is being accessed. If a 16-bit transfer is requested by the CPU, the system will automatically convert it into two 8-bit cycles. When a 16-bit device is accessed, it informs the system of its presence, so that the data can be transferred in one cycle.

Timing requirements for memory accesses mean that the system needs to know the size of the device being accessed (8- or 16-bits) before the strobe is asserted. At this time, the device does not know whether the address corresponds to I/O or memory space. The ISA bus therefore uses two signals to indicate that a device is 16 bits: IO16 and M16.

IO16 is driven low by a device that detects an address on SA0–9 according to a word I/O port.

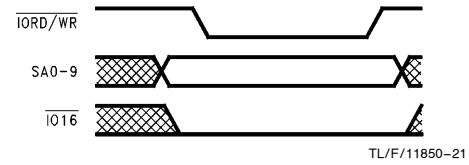

FIGURE 20. IO16 Cycle

M16 is driven low by a device that detects a valid address on LA17–23 for 16-bit memory. LA17–23 are unlatched address lines that are valid earlier than SA0–19. They become invalid before the end of the cycle. M16 is latched by the system. The device is required to latch LA17–23 for use by its address decoder. The BALE signal should be used as the latch enable for the LA address latch.

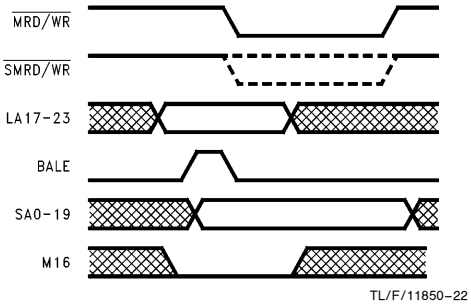

FIGURE 21. M16 Cycle

The size of the system transfer is indicated on signals SA0 and SBHE:

SAO	SBHE	
L	H	Byte transfer, even address
H	L	Byte transfer, odd address
L	L	Word transfer
H	H	Not used

SBHE has the same timing as SAO-19.

2.3.5 DMA and Refresh Cycles

DMA cycles are direct transfers between an I/O port and memory. One I/O strobe and one memory strobe are used together for the cycle. The I/O device is selected by one of 7 DACK signals. The memory device is selected by the LA17–23 and SA0–19 address lines. In order that the I/O device corresponding to SA0–9 does not respond, the AEN signal is driven high; I/O devices are only allowed to respond if AEN is low. ISA DMA is not used by AT/LANTIC.

Refresh cycles occur every 15.6 μs. They are similar to memory read cycles, except that the REFRESH signal is active. Refresh is not used by AT/LANTIC.

2.3.6 Bus Timing Compatibility Modes

In some PCs using certain chipsets, the timing requirement for an adapter card to drive CHRDY from receiving an active IORD or IOWD is impossible to meet. The consequence is that the ISA bus completes the cycle even though the AT/LANTIC requires more time. AT/LANTIC incorporates logic to detect this condition, and has two ways of overcoming the problem.

If the condition occurs, configuration register B bit 5 ''BE'' is set to ''1''. This can be used by software to warn that a fix is required.

The two timing change modes are:

IO16 Mode

The problem only occurs for 16-bit cycles. IO16 is normally asserted whenever the address SA0–9 is valid. By additionally requiring that IORD or IOWR is asserted before IO16 is driven low, the offending chipsets are fooled into accepting 8-bit timing for CHRDY, while still transferring 16-bits correctly.

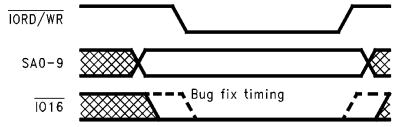

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FIGURE 22. IO16 Timing Change Mode

CHRDY Mode

It is possible to drive CHRDY low early, qualified by SA0–9 and AEN without IORD or IOWR. If a valid address is present, and AT/LANTIC requires a longer-than-default cycle, this circuit starts driving CHRDY low as soon as BALE is active. If, at any time, MRD or MWR memory strobes become asserted, then CHRDY is released immediately. Otherwise, CHRDY is held low until the next falling edge of ISACLK after BALE has gone low. In a typical system, this clock edge is immediately followed by IORD or IOWR being asserted. The small ''gap'' between ISACLK and IORD or IOWR will not normally be long enough for CHRDY to be pulled high by the pull-up resistor.

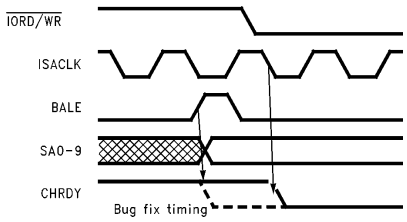

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FIGURE 23. CHRDY Fix

2.4 Boot PROM

The boot PROM interface uses the AT/LANTIC to decode the ISA address, and to provide data bus drivers onto the ISA bus. Because the PROM data is connected to the NIC memory support data bus, arbitration is required to access the PROM. The boot PROM is not mapped onto the NIC memory map.

If the MSWR signal is connected, a FLASH boot PROM can be used, allowing in-situ programming or updating.

If the PROM is read-only, the configuration register B bit 6 ''BPWR'' should be set to ''0'' to prevent bus contention if write cycles are attempted.

The boot PROM appears as an 8-bit device, regardless of the size of the interface. However there is a special case where it will not work properly. When emulating a WD Plus adapter, AT/LANTIC uses 16-bit wide buffer RAM, which it declares as 16-bit to the ISA bus by driving M16 low. The decode logic for M16 uses only LA17–23, i.e., a 128 kbyte region—this is an ISA bus limitation. If the boot PROM and the buffer memory are placed within the same 128 kbyte region, the boot PROM will appear to the ISA bus as a 16-bit device. Since the PROM can only produce 8-bits of data, it will fail.

Boot PROMs can be written to overcome this problem by first copying the PROM contents to system memory, and then executing from the copy instead. The PROM therefore need not be accessed at the same time as the shared RAM is enabled.

2.5 Boot PROM and RAM Timing Calculations

Boot PROM timings are derived from the ISA bus timings minus AT/LANTIC propagation delays.

RAM timings are the worst case of two situations: ISA bus accesses, similar to the Boot PROM, and AT/LANTIC DMA channel accesses.

For 8-bit cards, 8-bit ISA timings should be used for both RAM and boot PROM.

For 16-bit cards, 16-bit ISA timings should be used for the buffer RAM, and 8-bit timings should be used for the boot PROM.

2.5.1 Boot PROM/RAM ISA Read Timing

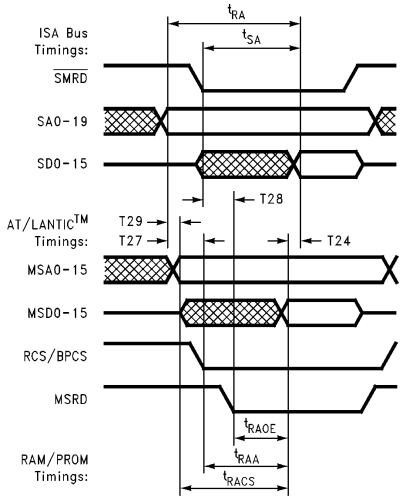

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FIGURE 24. Boot PROM/RAM ISA Read

Access time from OE:

$$t_{RAOE} = t_{RA}\ \text{min} - T28\text{max} - T24\text{max}$$

Access time from address:

$$t_{RAA} = t_{SA}\ \text{min} - T29\text{max} - T24\text{max}$$

Access time from CS:

$$t_{RACS} = t_{SA}\ \text{min} - T27\text{max} - T24\text{max}$$

For a typical 8 MHz ISA bus:

t_{RA} min = 480 ns (8 bit) or 160 ns (16 bit),
t_{SA} min = 570 ns (8 bit) or 200 ns (16 bit).

2.5.2 Boot PROM/RAM ISA Write Timing

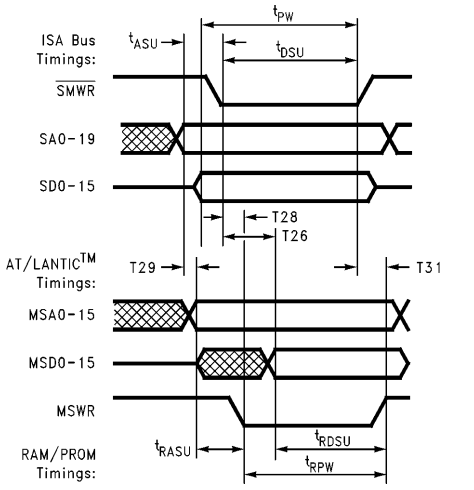

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FIGURE 25. Boot PROM/RAM ISA Write

Address setup time:

$$t_{RASU} = t_{ASU}\ \text{min} + t28\text{min} - T29\text{max}$$

Data setup time:

$$t_{RDSU} = t_{DSU}\ \text{min} + t31\ \text{min} - T26\text{max}$$

Write pulse width:

$$t_{RPW} = t_{PW}\ \text{min} + t31\ \text{min} - T28\text{max}$$

For a typical 8 MHz ISA bus:

t_{RASU} min = 90 ns (8 bit) or 28 ns (16 bit),
t_{RPW} min = 530 ns (8 bit) or 154 ns (16 bit),
t_{RDSU} min = 470 ns (8 bit) or 105 ns (16 bit).

2.5.3 RAM DMA Timing

These timings are given in the AT/LANTIC data sheet Section 8, under ''I/O port or FIFO transfers''.

t_{RAOE} = T3 − T7,
t_{RAA} = T2 + T3 − T7,
t_{RACS} = T4 − T7,
t_{RASU} = T2,
t_{RDSU} = T9,
t_{RPW} = T3

2.6 Fast Read Feature

This is a feature designed into AT/LANTIC to improve the performance of the remote DMA channel in NE2000 mode. The actual performance measured will depend on the platform that AT/LANTIC is used with, and the test configuration used.

The architecture of the remote DMA channel is as shown:

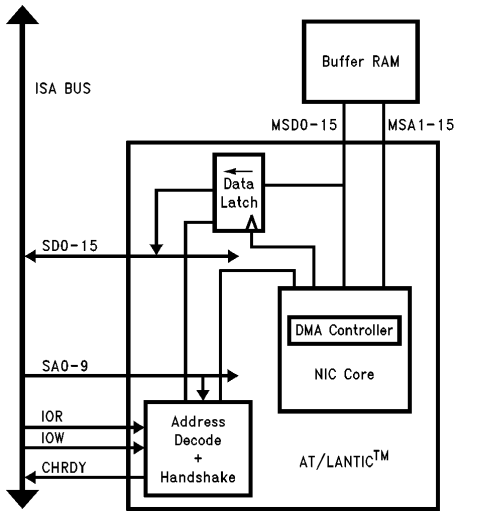

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FIGURE 26. Remote DMA Controller

When the remote DMA read is started, by I/O writes to the NIC remote DMA controller, the buffer RAM is accessed at the first address and the data is latched in the data transfer latch. The PC then reads this data over the ISA bus. At the end of the IORD strobe, the DMA controller fetches data from the next RAM address and latches it into the latch. Hardware handshake logic prevents the PC from completing a read cycle until the data is ready.

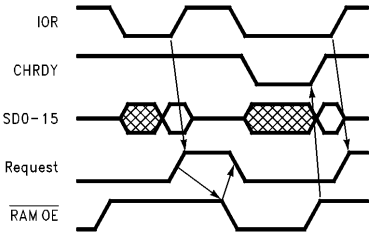

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FIGURE 27. Remote DMA Read Timing

The request for more data from the DMA controller is not made until the end of the IORD strobe. When fast read operation is enabled, the request for more data is made as soon as CHRDY is released, before the end of the IORD. For cycles that do not require CHRDY, i.e. the data is already in the latch, more data is requested at the start of the IORD strobe.

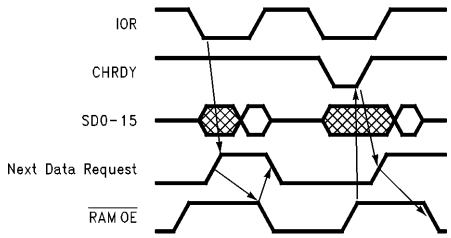

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FIGURE 28. Fast Read Remote DMA Timing

There is a danger, in very slow machines, that the new data will be latched into the data transfer latch before the end of the current IORD cycle. For this reason, Fast Read is not recommended for 8-bit systems.

The NIC core is specified to take a minimum of 11 clocks between data being requested and the latch being updated. A typical system with an NIC core clock of 20 MHz will therefore take at least 550 ns. Fast Read mode is safe in any system where the IORD strobe width, or the CHRDY to IORD high delay does not exceed 550ns.

2.7 Reset Operation

AT/LANTIC has different degrees of RESET according to the duration of the RESET pulse. The pulse width is measured by counting X1 clocks (20 MHz), so the timing period can only begin after the oscillator has started.

In order to prevent noise problems, a RESET pulse of less than 350 ns will be ignored. The RESET pulse must be at least 400 ns to be guaranteed to be recognized.

A RESET pulse of at least 400 ns will reset the internal logic, including the 8390 NIC core, and will tristate all I/O pins. A 60k pull down will be enabled for each configuration pin MSD0–15 and MSA1–8.

If the RESET pulse is more than 400 ns long, configuration data and Ethernet node address will be loaded. The load sequence begins when RESET goes low, and can take up to 320 μs. During this time, all ISA bus cycles are ignored.

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