

Low Power Ethernet with the CMOS DP83910 Serial Network Interface

National Semiconductor
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INTRODUCTION

This application note discusses the features of, and implementation techniques for, National Semiconductor's CMOS Serial Network Interface (SNI), the DP83910. Also, a comparison of the CMOS SNI to National's bipolar SNI (DP8391) on several key issues will be provided. In general, the DP83910 provides a low power Attachment Unit Interface (AUI) for a Carrier-Sense Multiple Access with Collision Detect (CSMA/CD) Ethernet system. In fact, when used in conjunction with National Semiconductor's Network Interface Controller (NIC, DP8390) and Coaxial Transceiver Interface (CTI, DP8392), the DP83910 provides for a complete IEEE 802.3 Ethernet and/or thin wire Ethernet solution, as shown in *Figure 1*.

FUNCTIONAL DESCRIPTION OF THE DP83910

The CMOS SNI operates as an interface between an Ethernet transceiver and a local area network data controller. A functional block diagram of the DP83910 is shown in *Figure 2*. The primary function of this interface is to perform the encoding and decoding that is necessary for the differential pair Manchester encoded data of the transceiver and the Non-Return-to-Zero (NRZ) serial data of the NIC to be compatible with each other. In the case of a transmission, the SNI translates the NRZ serial data from a network controller's transmit data line into differential pair Manchester encoded data on a transceiver's transmit pair. In order to

perform this operation, the NRZ bit stream is first received by the Manchester encoder block of the SNI. Once the bit stream is encoded, it is transmitted out differentially on to the transmit differential pair through the transmit driver. When a reception takes place, the differential receive data from a transceiver is converted from Manchester encoded data into NRZ serial data and a receive clock, which are passed to the receive data and receive clock inputs of the Network Interface Controller. In executing this sequence, the DP83910's data receiver takes the Manchester data from the differential receive lines and passes it to the phase locked loop (PLL) decoder block. The PLL block then decodes the data and generates a data receive clock and a stream of NRZ serial data, which is presented to the NIC. In the case of National Semiconductor's Network Interface Controller, the DP8390, the serial NRZ signals are called TXD and RXD.

In addition to performing the Manchester encoding and decoding function, the DP83910 also provides several important network signals to the network controller. A diagram of the interface between National Semiconductor's NIC and the CMOS SNI can be found in *Figure 3*. The first of these signals is carrier sense (CRS), which indicates to the controller that data is present on the SNI's receive differential pair. Secondly, the SNI provides the network controller with a collision detection signal (COL), which informs the controller that a collision is taking place somewhere on the net-

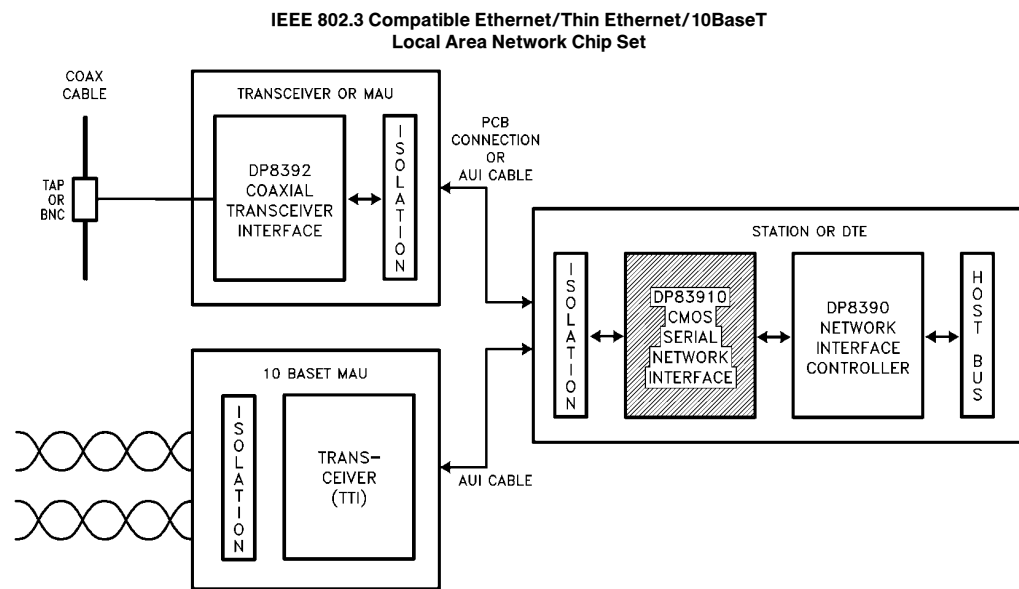


FIGURE 1. A Block Level Diagram of an Ethernet Node

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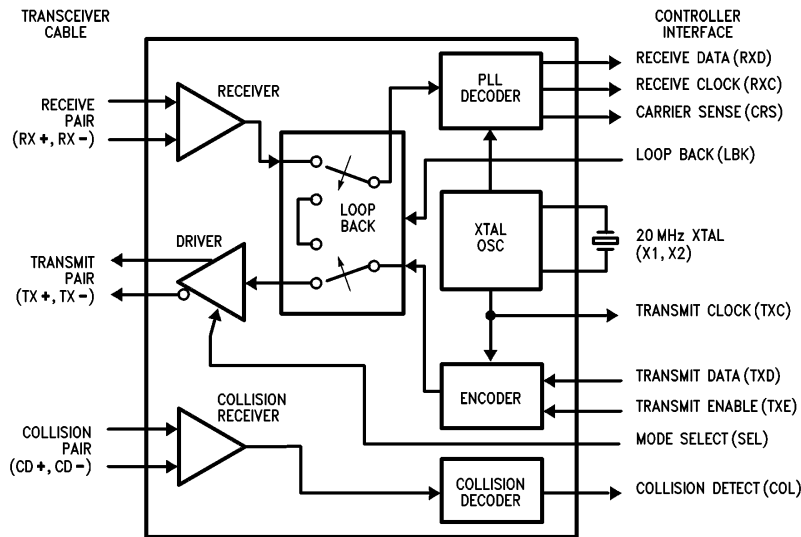


FIGURE 2. DP83910 Block Diagram

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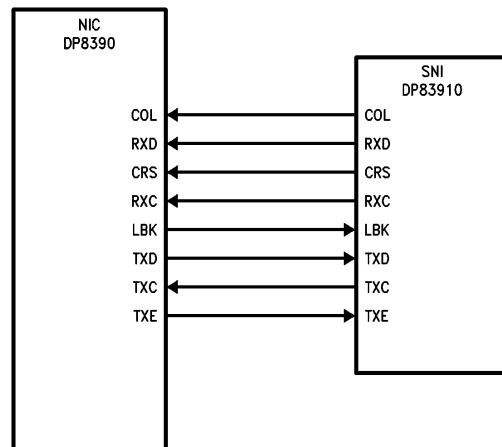


FIGURE 3. Interface between the DP8390 and DP83910

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work. The SNI itself is informed of the collision when its collision receiver detects a 10 MHz signal on the differential collision input pair. Finally, the DP83910 provides both the receive and transmit clocks (RXC and TXC, respectively). The transmit clock is a divide by two derivative of the SNI's oscillator inputs (X1 and X2), while the receive clock is generated directly from the frequency of the input data to the PLL.

The DP83910 can also be placed in a loopback mode, in order to check the SNI's receive and transmit interface to the network controller. In loopback, as pictured above, the SNI's Manchester encoder block is essentially connected directly to the PLL decoder block. This allows for the validation of the Manchester encoding and decoding process without the variable of random network traffic. The SNI is placed in loopback mode when the loopback pin (LBK) is driven high.

COMPARING THE DP83910 WITH THE DP8391

The DP83910 is basically a CMOS version of the existing National Semiconductor bipolar SNI, the DP8391. The functionality of the two parts is identical. However, there are a few differences that exist between the two parts, in spite of the fact that they can be implemented as pin for pin compatible. The most fundamental difference between the two parts is the process under which each is manufactured. The DP83910 SNI is fabricated in a CMOS process, while the DP8391 is made in a bipolar process. As a result of this, the level of average power supply current needed by the DP83910 is approximately 75 percent less than the 270 mA required by the DP8391. Another significant difference between the two parts is the CMOS SNI's need for a pulse transformer to be placed between all of its differential signals and those of the transceiver, regardless of whether a drop cable or thin wire Ethernet configuration is being imple-

mented. This is necessary due to the fact that the CMOS process will not guarantee the IEEE 802.3 16V fail safe specification if no isolation is provided to the differential signals that go to the AUI cable. One consequence of the transformer requirement is that National Semiconductor defines the AUI interface at the transceiver side of the transformer and only guarantees the correct operation of the CMOS SNI when the pulse transformer is employed in the system.

In addition to the above process related differences, there are still two non-process related differences, which need to be mentioned. First, the phase locked loop in the bipolar SNI is digital, while the phase locked loop of the CMOS SNI is analog. This is functionally transparent when designing with the DP83910; however, it does provide for a significant savings in power consumption. Finally, it should be noted that pin 17 (TEST) on the bipolar SNI is required to be tied to ground through a capacitor, while the same pin on the CMOS SNI can either be implemented in the same manner or connected directly to ground. A list of all the above mentioned differences can be found in Table I.

DESIGNING WITH THE DP83910

In developing the DP83910, National Semiconductor performed extensive testing in its own Local Area Network Laboratory to assure that the CMOS SNI would provide an easily implemented low power controller/transceiver interface for Ethernet system designers. This development and testing assured that the DP83910 was IEEE 802.3 and Ethernet compatible, able to interface with industry standard transceivers (Ethernet, Twisted Pair Ethernet, and Fiber Optic Ethernet), and is capable of having the National Semiconductor DP8391 as a pin-for-pin replacement. In *Figures 4* and *5*, two methods of implementing the DP83910 with the DP8392 are demonstrated. One significant feature of both designs is that it is possible to directly substitute a DP8391 for the CMOS SNI and maintain the same functional quality.

The DP83910 Transmitter Operation

When operating as a transmitter, the DP83910 combines NRZ data received from the controller with a clock signal, which the SNI generates, and encodes them into a Manchester serial bit stream. This encoded signal then appears differentially at the SNI's TX± output. In Ethernet (10Base5) applications, this signal is sent to the transceiver or the Medium Attachment Unit (MAU) through an AUI transceiver cable. This cable, which can be up to 50 meters

in length, typically consists of four individually shielded twisted wire pairs (TX±, RX±, CD±, and PWR/GND), which are covered by an additional overall shield. The transmit signal pair, which has a differential characteristic impedance of 78Ω, should be terminated at the receiving end of the cable. It should be noted that each of the TX+ and TX− source follower outputs needs to be connected to ground through a 270Ω pull down resistor.

When employing the CMOS SNI, it is important to place a pulse transformer between the differential transmit pair on the DP83910 and the differential transmit signal on the AUI cable or CTI, as shown in *Figures 4* and *5*. This transformer is required in order to provide the necessary isolation for the CMOS SNI to meet the IEEE 802.3 16V fail safe specification. However, the pulse transformer does reduce the transmission of noise onto the transceiver cable. Also, it should be noted that more inductive transformers will decrease the magnitude of the undershoot. Furthermore, it is imperative that the designer guarantee the inductive load seen between the DP83910's AUI interface and the CTI receiver be greater than 27 μH. Transformers with 50 μH to 150 μH loading, such as the Pulse Engineering PE64103 and Nano Pulse NP5417, are recommended, since they will minimize the inductive undershoot on the SNI's TX± output pair and reduce the noise seen by the CTI's differential transmit input pair. It is important that the selected pulse transformer doesn't excessively increase the rise and fall time nor lower the output amplitude despite the fact that it reduces the undershoot.

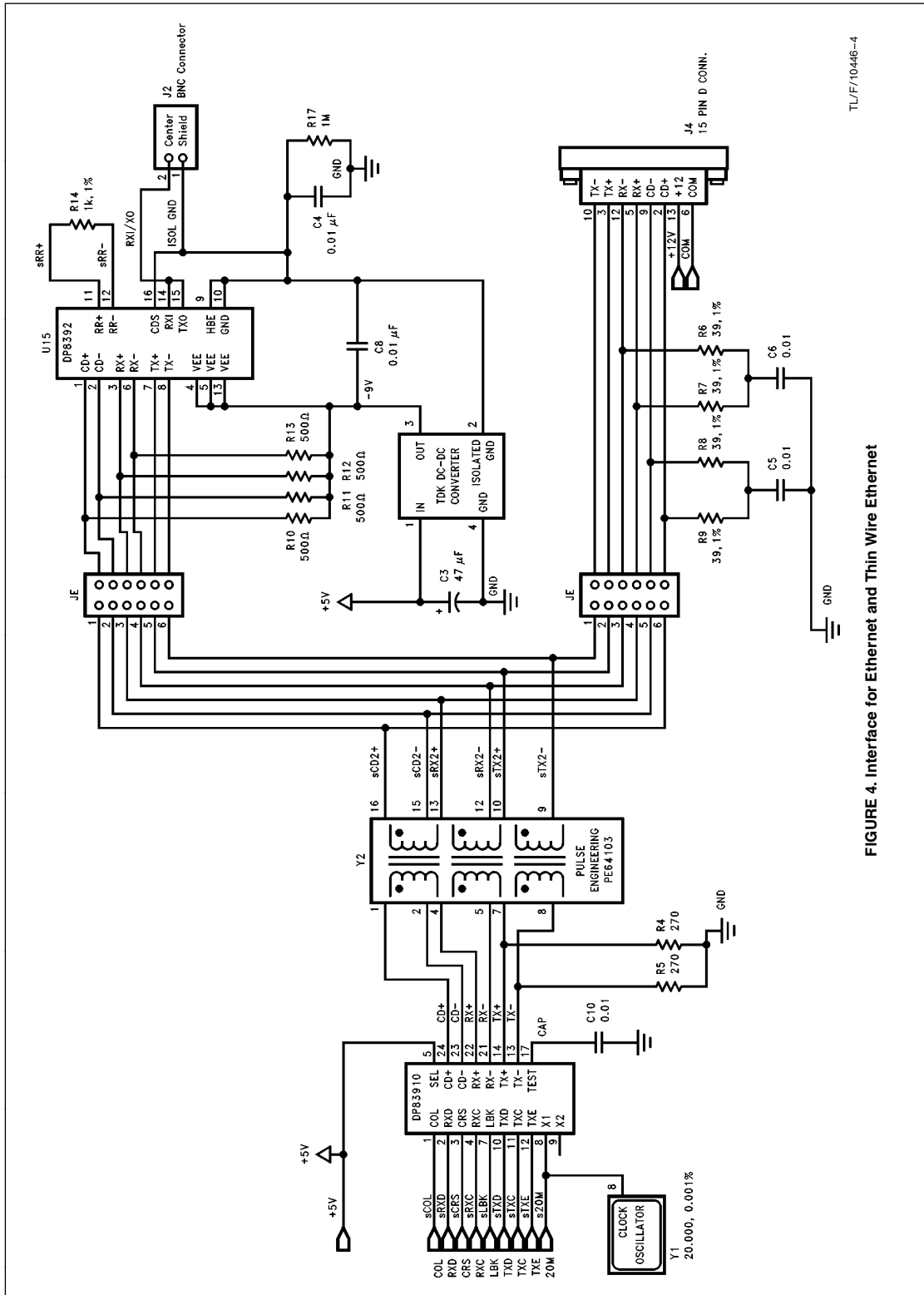
The DP83910 provides both half and full step modes. The IEEE 802.3 standard requires the use of half step mode, in which the transmit output goes to differential zero in idle. In full step mode, the transmitter enters idle and stays at a fixed level. This will eventually allow the pulse transformer to completely saturate. The desired mode of operation is chosen through the Mode Select pin (SEL) on the SNI.

The DP83910 Data Receiver Operation

While performing reception, the CMOS SNI receives differential Manchester encoded serial data and converts it into NRZ serial data and a receive clock. The Manchester encoded data, which is received from the CTI or AUI cable, must be isolated before it reaches the SNI. Hence, the DP83910 requires that there be a pulse transformer on the SNI's side of the AUI interface. The actual employment of this transformer can be seen in both *Figures 4* and *5*. This

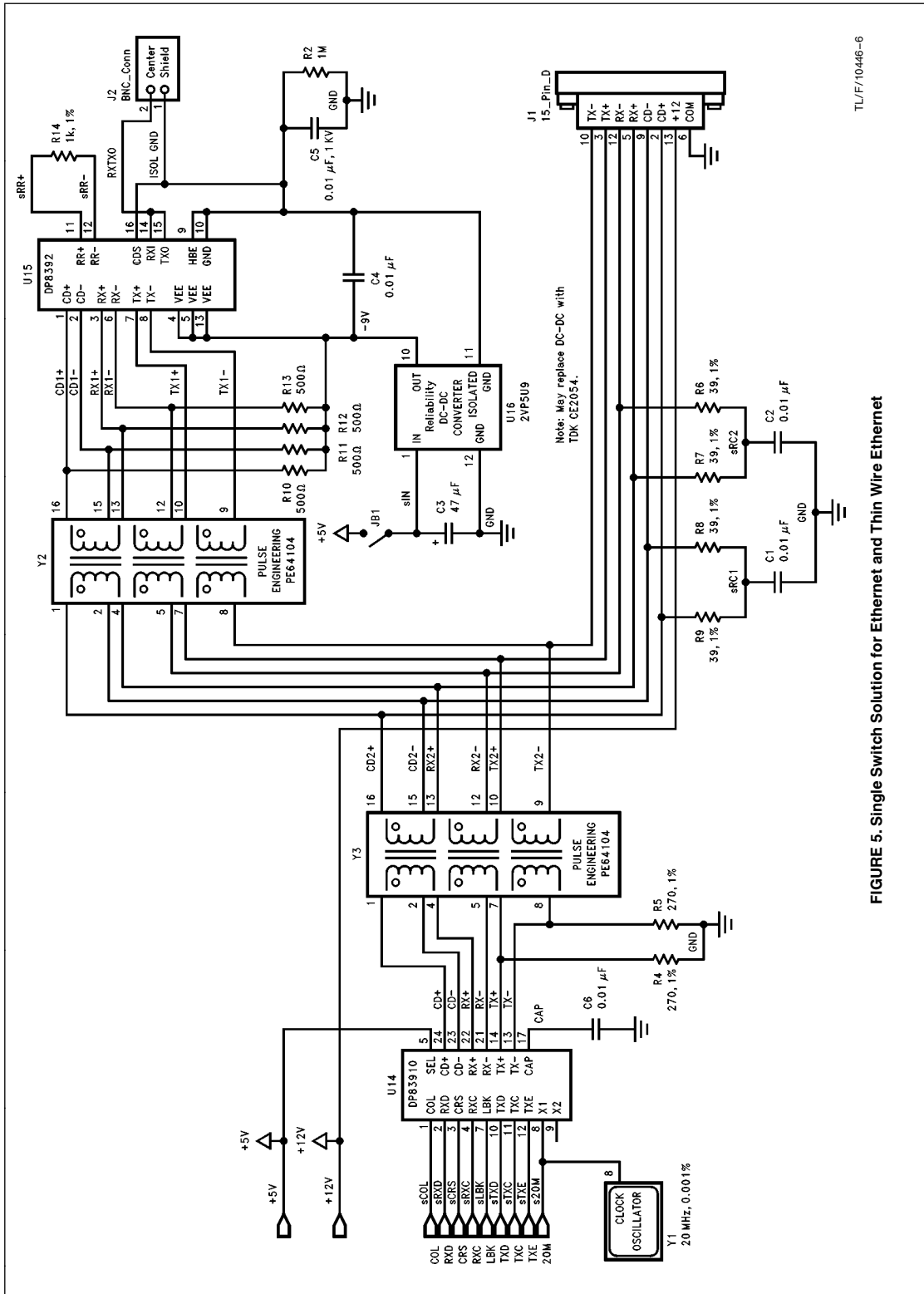
TABLE I. Comparison of the DP8391 and DP83910

	DP8391	DP83910
Process	Bipolar	CMOS
Power Consumption (Typical)	270 mA	70 mA
Pulse Transformer (At DTE Side of AUI Interface)	Optional	Required
Phase Locked Loop	Digital	Analog
Pin 17	PLL Filter/Capacitor Required	Test Pin/Capacitor Optional



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FIGURE 4. Interface for Ethernet and Thin Wire Ethernet



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FIGURE 5. Single Switch Solution for Ethernet and Thin Wire Ethernet

transformer is mandatory and it forms part of the internal DC biasing circuit used for the differential receivers. Furthermore, the transformer is also needed to isolate the transceiver cable against the 16V voltage fault specification in the IEEE 802.3 standard. The performance of the differential receiver is not greatly affected by the selection of a pulse transformer. As a result, the pulse transformer selected for the transmitter design will also work correctly for the RX± data receiver. It should be noted here that the collision receiver is very similar to the data receiver and requires the same isolation. The collision input will be discussed more in the following section.

Once the data arrives at the receiver inputs of the SNI, it is amplified and then decoded by the analog phase locked loop, which can receive Manchester data with ±20 ns of random jitter. During the decoding process, the incoming signal is converted into NRZ data and a receive clock, which are sent to a network controller. Also, the differential data receiver has a built in filter to provide a static noise margin. This filter enables the SNI to reject signals that do not exceed the input squelch voltage and have less than a 30 ns pulse width.

Furthermore, since the DP83910 and pulse transformer constitute the AUI interface, the physical connection between the AUI and the MAU interfaces is defined as being on the MAU side of the pulse transformer. In light of this, it is permissible, when incorporating the CMOS SNI in a thin wire Ethernet application, to have a 78Ω resistance appear across the differential receive and collision inputs to the CTI, as shown in *Figure 5*.

The DP83910 Collision Pair Operation

In addition to the data receiver, the DP83910 also provides a differential receiver for the collision pair, which is driven by the transceiver. This 10 MHz active signal, from the AUI Interface, is converted to a TTL signal, digitally stretched, and sent to the controller as the Collision Detect Output (COL). Just as with the data receiver, the differential collision receiver has a built in filter that rejects pulses that do not exceed the input squelch voltage level and have a pulse width less than 30 ns.

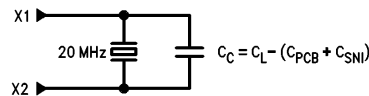
Optimal Ethernet and Thin Wire Ethernet Interface

If it is necessary to design a LAN board that minimizes the number of switching devices (jumpers) to alternate between Ethernet and thin wire Ethernet, the solution in *Figure 5* could be employed. This solution, in contrast to the six jumper solution in *Figure 4*, requires only one switch, which enables and disables the power supply to the CTI. In the case of thin wire Ethernet, power would be supplied to the CTI, while during drop cable Ethernet operation the unused CTI would be powered down. Hence, no excessive power is required when thin wire Ethernet is not in use. Furthermore, since there is only one switch, it may be feasible to implement that switch with a transistor as opposed to a jumper. The advantage to using a transistor is that the Ethernet/thin wire Ethernet option can now be made to be software selectable. This is accomplished by developing a control signal, which the software can issue to switch the transistor. Also, in looking at *Figure 5*, it is seen that two pulse transformers are used. The first transformer (Y3) is required by the CMOS SNI, for the reasons previously mentioned. The second pulse transformer (Y2), however, is used to isolate the powered-down CTI from the AUI cable interface, when Ethernet is being used. As in *Figure 4*, the application in *Figure 5* allows the direct substitution of a bipolar SNI, the DP8391, for the CMOS SNI.

The DP83910 Oscillator Inputs

The oscillator inputs of the CMOS SNI can be driven with a crystal or an oscillator. In either case, the SNI oscillator must be driven with a 20 MHz signal that provides for the transmitted frequency to be accurate within 0.01% as specified in IEEE 802.3 standard. When using an oscillator, the output of the oscillator should be tied to input X1 of the SNI and the X2 input of the SNI should be left unconnected or grounded. However, the employment of a crystal to generate the 20 MHz signal at the SNI's oscillator inputs requires a great deal of care. The frequency of the crystal is usually measured with a fixed load capacitance (C_L , typically 20 pF), which is specified in the crystal's data sheet. In order to prevent any distortion in the transmitted frequency, the total capacitance across the crystal's leads should equal its specified load capacitance. The capacitance that is seen by the crystal's leads is the sum of the stray PC board capacitance (C_{PCB}) and the capacitance looking into the X1 and X2 inputs (C_{SNI}). If this capacitance is smaller than the crystal's load capacitance, a correctional capacitance (C_C) can be placed across the crystal's leads. This correctional capacitance would equal the difference between the crystal's load capacitance and the sum of the stray PC board capacitance and the SNI's X1 and X2 input capacitance. It should be noted that the input capacitance of the SNI that is seen across X1 and X2 is approximately a negligible 0.5 pF. *Figure 6* displays a possible crystal setup. The selected crystal should meet the following specifications:

Resonant frequency	20 MHz
Tolerance	± 0.001% at 25°C
Stability	± 0.005% at 0°C–70°C
Type	AT cut
Circuit	Parallel Resonance

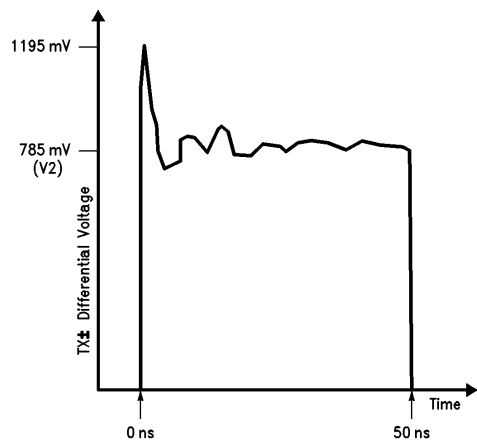


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FIGURE 6. SNI Oscillator Input Circuit

Improving Transmitter Overshoot

Upon transitioning from a differential voltage of one polarity to another polarity (i.e., positive to negative), the magnitude of the differential transmit signal will reach a peak value. This peak at the transition points in the differential transmit waveform is referred to as the overshoot voltage. The overshoot voltage of the DP83910 is below the maximum allowable 1315 mV value that appears in the IEEE 802.3 standard. However, the IEEE standard also defines the overshoot voltage to be no greater than 1.12 times the nominal value (IEEE calls this nominal value V2). The DP83910 exceeds this particular segment of the overshoot specification, as shown in *Figure 7*. However, exceeding the allowable overshoot voltage value, as the CMOS SNI does, will have no functional affect on a system. Furthermore, the overshoot voltage can be altered to adhere to the IEEE 802.3 specification by placing a capacitor across the differential transmit pair at the primary (SNI side) of the required pulse transformer. This capacitor should be in the range of 40 pF to 50 pF and will not degrade the performance of the CMOS SNI or system in any way. It should also be mentioned that the DP8391, the bipolar SNI, will still be a pin-for-pin replacement for the CMOS SNI, in a design which employs the capacitor for improving the overshoot.



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FIGURE 7. TX ± Differential Overshoot Voltage

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