Interfacing the DP8420A/21A/22A to the Z280/Z80000/Z8000 Microprocessor

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I INTRODUCTION

This application note describes how to interface the Z280 microprocessor to the DP8422A DRAM controller (also applicable to DP8420A/21A). It is assumed that the reader is already familiar with Z280 and the DP8422A modes of operation. The interface to the Z80000 and Z8000 is similar to the interface described in this application note.

II DESCRIPTION OF DESIGN, ALLOWING OPERATION AT 10 MHz (AND ABOVE) WITH 1 WAIT STATE IN NORMAL ACCESSES AND 1 WAIT STATE DURING BURST ACCESSES

The block diagram of this design is shown driving two banks of DRAM, each bank being 16 bits in width, giving a maximum memory capacity of up to 16 Mbytes (using 4 M-bit × 1 DRAMs). By choosing a different $\overline{RAS}$ and $\overline{CAS}$ configuration mode (see programming mode bits section of DP8422A data sheet) this application can support 4 banks of DRAM, giving a memory capacity of up to 32 Mbytes (using 4 M-bit × 1 DRAMs).

The memory banks are interleaved on every four word (16-bit word) boundry. This means that the address bit (A3) is tied to the bank select input of the DP8422A (B1).

Address bits A2,1 are tied to the most significant row and column address inputs (R9,C9 for 1 Mbit DRAMs) to support burst accesses using static column mode DRAMs. Since this application assumes the use of static column DRAMs the column address strobe ($\overline{CAS}$) is left low throughout the entire burst access. If the user desires to use nibble mode or page mode DRAMs the $\overline{CAS}$ outputs must be toggled, the $\overline{ECAS}$ inputs the DP8422A can be used for this purpose ($\overline{DS}$ of the Z280 could be ''OR''ed with the current $\overline{ECAS}$ inputs). If nibble mode DRAMs are used the COLINC input of the DP8422A need not be driven.

Address bit A0 is used to produce the two byte select data strobes along with the byte/word signal (B/W). These byte selects (Byte 0 $\overline{ECAS}$ and Byte 1 $\overline{ECAS}$) are used in byte reads and writes as well as selects for the transceivers.

If the majority of accesses made by the Z280 are sequential, the Z280 can be doing burst accesses most of the time. Each burst of four words can alternate memory banks, allowing one memory bank to be precharging ($\overline{RAS}$ precharge) while the other bank is being accessed (Bank select, B1, tied to address A3). This is a higher performance memory system then a non-interleaved memory system (bank select on the higher address bits). Each separate memory access to the same memory bank may require extra wait states to be inserted into the CPU access cycles to allow for the $\overline{RAS}$ precharge time, if two periods or more of $\overline{RAS}$ precharge were programmed.

This application allows 1 or more wait states to be inserted in normal accesses and 1 or more wait states to be inserted during burst accesses of the Z280. The number of wait states can be adjusted through the $\overline{WAITIN}$ input of the DP8422A.

The logic shown in this application note forms a complete Z280 memory sub-system, no other logic is needed. This sub-system automatically takes care of:

A. arbitration between Port A, Port B, and refreshing the DRAM;

B. the insertion of wait states to the processor (Port A and Port B) when needed (i.e., if $\overline{RAS}$ precharge is needed, refresh is happening during a memory access, the other Port is currently doing an access . . .etc);

C. performing byte writes and reads to the 16-bit words in memory;

D. normal and burst access operations.

The external wait logic (U1, U2, U3, U4; see *Figure 1*) is needed to support burst accesses of the Z280. During burst accesses the Z280 $\overline{WAIT}$ input is sampled every falling clock edge. What is worse is that the $\overline{WAIT}$ input needs one half clock period setup time and the $\overline{DS}$ signal (used to toggle $\overline{ECAS}0-3$ and thereby toggle the DP8422A $\overline{WAIT}$ output) takes close to one half of a clock period to transition high. This leaves no time for the DP8422A $\overline{WAIT}$ output to transition between states. The external flip-flop is used to provide extra fast response time for normal access wait states and to toggle when doing a burst mode access. If the user is not going to do burst accesses the $\overline{WAIT}$ output can be tied directly to the $\overline{WAIT}$ input of the Z280 (U1, U2, U3, U4 would not be needed). Also all this logic could easily be put into a PAL® if desired.

By using the ''output control'' pins of some external latches (74ALS373's), this application can easily be used in a dual access application. The addresses could be TRI-STATE® through these latches, the write input ($\overline{WIN}$), lock input ($\overline{LOCK}$), and $\overline{ECAS}0-3$ inputs must also be able to be TRI-STATE (a 74AS244 could be used for this purpose). By multiplexing the above inputs (through the use of the above parts and similar parts for Port B) the DP8422A can be used in a dual access application. If this design is used in a dual access application the t_{RAC} and t_{CAC} (required $\overline{RAS}$ and $\overline{CAS}$ access time required by the DRAM) will have to be recalculated since the time to $\overline{RAS}$ and $\overline{CAS}$ is longer for the dual access application (see TIMING section of this application note).

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III Z280 DESIGN, 10 MHz WITH 1 WAIT STATE DURING NORMAL ACCESSES AND 1 WAIT STATE DURING BURST ACCESSES, PROGRAMMING MODE BITS

Programming Bits	Description
R0 = 0	$\overline{RAS}$ low two clocks, $\overline{RAS}$ precharge
R1 = 1	of two clocks, this setup will only guarantee 93.5 ns $\overline{RAS}$ precharge (at 10 MHz) from refresh $\overline{RAS}$ high to access $\overline{RAS}$ low. If more $\overline{RAS}$ precharge is desired the user should program three periods of $\overline{RAS}$ precharge.
R2 = 0	$\overline{DTACK}$ one half is chosen. $\overline{DTACK}$
R3 = 1	low first rising CLK edge after access $\overline{RAS}$ is low.
R4 = 0	No WAIT states during burst accesses
R5 = 0	
R6 = 0	If $\overline{WAITIN}$ = 0, add one clock to $\overline{DTACK}$. $\overline{WAITIN}$ may be tied high or low in this application depending upon the number of wait states the user desires to insert into the access.
R7 = 1	Select $\overline{DTACK}$
R8 = 1	Non-interleaved Mode
R9 = X	
C0 = X	Select based upon the input
C1 = X	''DELCLK'' frequency. Example: if the
C2 = X	input clock frequency is 10 MHz then choose C0,1,2 = 1,0,1 (divide by five, this will give a frequency of 2 MHz).
C3 = X	
C4 = 0	$\overline{RAS}$ groups selected by ''B1''. This
C5 = 0	mode allows two $\overline{RAS}$ outputs to go
C6 = 1	low during an access, and allows byte writing in 16- or 32-bit words.
C7 = 1	Column address setup time of 0 ns
C8 = 1	Row address hold time of 15 ns
C9 = 1	Delay $\overline{CAS}$ during write accesses to one clock after $\overline{RAS}$ transitions low
B0 = 0	Latches latch on ALE input low
B1 = 0	Access mode 0
$\overline{ECAS}$0 = 0	$\overline{CAS}$n not extended beyond $\overline{RAS}$n

0 = Program with low voltage level
1 = Program with high voltage level
X = Program with either high or low voltage level (don't care condition)

IV Z280 TIMING CALCULATIONS FOR DESIGN AT 10 MHz WITH 1 WAIT STATE DURING NORMAL ACCESSES AND 1 WAIT STATE DURING BURST ACCESSES

1. Minimum ALE high setup time to CLOCK high if using the on-chip latches and more then one $\overline{RAS}$ bank (DP8422A-20 needs 29 ns, #301b):

   100 ns (one clock period) − 20 ns ($\overline{AS}$ valid maximum delay, #3 of Z280 data sheet) − 11 ns (74ALS04B max delay) = 69 ns

2A. Minimum address setup time to ALE low (DP8422A-20 needs 3 ns, #306):

   25 ns (address setup to $\overline{AS}$ high, #20 Z280 data sheet) + 1 ns (74ALS04B min delay) = 26 ns

2B. Minimum address hold time to ALE low (DP8422A-20 needs 10 ns, #305):

   20 ns (address hold from $\overline{AS}$ high, #22 of Z280 data sheet) + 1 ns (74ALS04B min delay) = 21 ns

2C. Minimum address setup to CLOCK high (DP8422A-20 needs bank address setup to CLOCK of 20 ns, #303):

   100 ns (one clock period) − 20 ns (max clock to address valid, Z280 data sheet #2) = 80 ns

3. Minimum $\overline{CS}$ setup time to clock high (DP8422A-20 needs 14 ns, #300): 80 ns (#2C above) − 22 ns (max 74ALS138 decoder) = 58 ns

4. Determining t_{RAC} during a normal access ($\overline{RAS}$ access time needed by the DRAM):

   250 ns (two and one half clock periods to do the access) − 32 ns (CLK to $\overline{RAS}$ low max, DP8422A-20 #307) − 30 ns (Z280 data setup time, #9) − 10 ns (74ALS245A max delay) = 178 ns

   Therefore the t_{RAC} of the DRAM must be 178 ns or less. (One can see that if zero wait states would have been programmed the t_{RAC} would have been 84 ns (using DP8422A-25, has faster CLK to $\overline{RAS}$ low of 26 ns) 184−100 (one clock)).

5. Determining t_{CAC} during a normal access ($\overline{CAS}$ access time) and column address access time needed by the DRAM:

   250 ns − 89 ns (CLK to $\overline{CAS}$ low on DP8422A-20, #308a) − 30 ns − 10 ns = 121 ns

   Therefore the t_{CAC} of the DRAM must be 121 ns or less.

6. Determining the column address access time needed during a static column mode burst access:

   20 ns (two clocks to do the access, Ex. mid T3 to mid TBW to mid T4) − 35 ns ($\overline{DS}$ high, Z280 parameter #8) − 43 ns (COLINC asserted to address outputs of DP8420A-20 incremented, #27) − 30 ns (Z280 data setup time, #9) − 10 ns (74ALS245A max delay) = 82 ns

   Therefore the column address access time of the DRAM must be 82 ns or less. (One can see that if zero wait states would have been programmed the column address access time would have been less then 0 ns (82 − 100 (one clock))).

7. Maximum time to $\overline{DTACK}$ one half low (74ALS374 D type flip-flop needs 10 ns setup to CLK):

   100 ns (One clock, mid T2 in mid TW) − 33 ns ($\overline{DTACK}$ one half low from CLK high on DP8422A-20, #18) − 12 ns (max delay on 74ALS02 = 55 ns

8. Minimum $\overline{WAIT}$ setup time to CLK low (Z280 $\overline{WAIT}$ input needs 50 ns, #14):

   100 ns (one clock period) − 16 ns (74ALS374 max delay) − 14 ns (74ALS08 max delay) = 70 ns

9. Minimum $\overline{RAS}$ precharge (DP8422A programmed with 2 clock periods of $\overline{RAS}$ precharge):

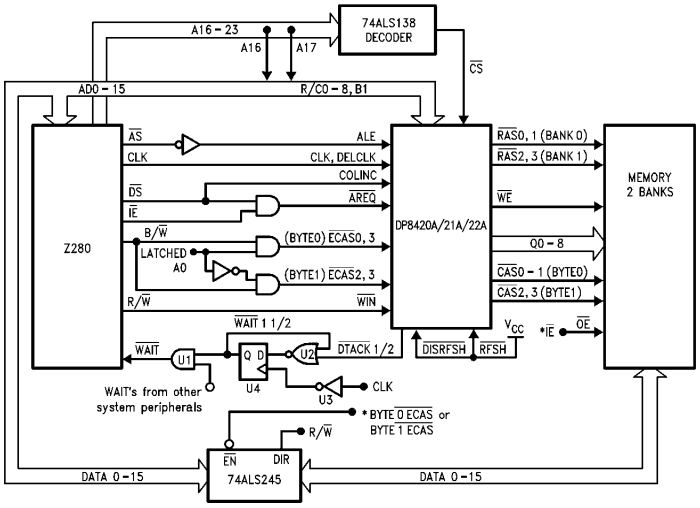
   Since the $\overline{AREQ}$ input of the DP8422A will go high from $\overline{DS}$ and $\overline{IE}$ both being high the $\overline{AREQ}$ high setup to clock rising edge (DP8422A parameter #29b, 19 ns) parameter is violated. This means that the rising clock edge following $\overline{AREQ}$ high may or may not be counted.

Since that first rising clock edge could be counted, and would give less $\overline{RAS}$ precharge time, we must assume this condition in the calculation of the minimum $\overline{RAS}$ precharge. Therefore:

200 ns (2 clock periods) − 50 ns (half clock period before both $\overline{IE}$ and $\overline{DS}$ transition high) − 35 ns ($\overline{IE}$ and $\overline{DS}$ high, Z280 parameters #8 and #19) − 5.5 ns (74AS08 max delay) − 16 ns (DP8422A $\overline{RAS}$ high to $\overline{RAS}$ low difference parameter #50) = 93.5 ns

Therefore, the user should guarantee that the DRAM he is using needs a $\overline{RAS}$ precharge time of 93.5 ns or less. If more $\overline{RAS}$ precharge time is needed the user should program the DP8422A with 3 periods of $\overline{RAS}$ precharge (R0, R1) during programming.

Note: Calculations can be performed for different frequencies and/or different combinations of wait states by substatuting the appropriate values into the above equations.



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*The user may want to gate $\overline{CS}$ ("OR" Gate) with the signals that produce $\overline{OE}$ to the DRAMs and $\overline{EN}$ to the transceivers

FIGURE 1. 10 MHz Z280 Design (Z-bus Interface), 1 Wait State in Normal Accesses, 1 Wait State in Burst Accesses

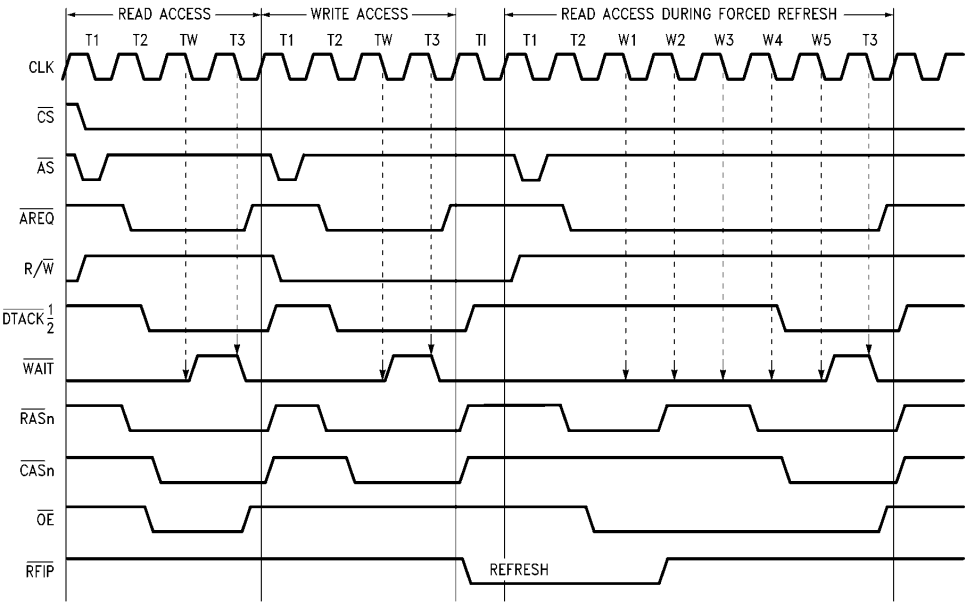

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FIGURE 2. Z280 Access Cycles and Refresh (1 Wait State during Normal Access Cycles)

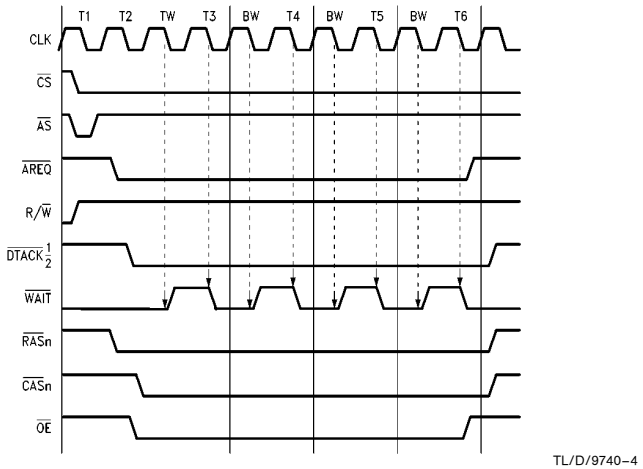
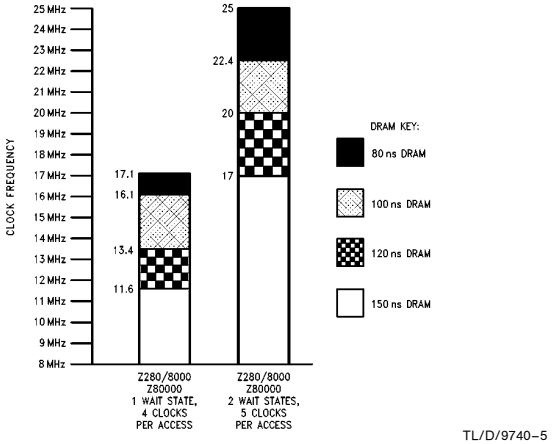


FIGURE 3. Z280 Burst Access Cycle (1 Wait State in Normal and Burst Accesses)

DRAM Speed vs Processor Speed (DRAM Speed References the RAS Access Time, t_{RAC}, of the DRAM. Using DP8422A-25 Timing Specifications)



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