Precautions to Take When Driving Memories

National Semiconductor
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As memory prices continue their relentless reduction of cost per bit, more and more systems designers are incorporating memories into their designs. In general these memories comprise a number of dynamic RAMs, such as the 64k x 1. In this x 1 configuration, the number of RAMs required is a multiple of the bus width. Most new system designs use 16-bit microprocessors, so that a typical memory will comprise from 16 to 64 DRAMs, thus providing from 64k to 256k addressing capability. This means the memory drivers have to drive upwards of 16 RAMs. The drivers may be part of an integrated circuit dynamic RAM controller such as the DP8408A/DP8409A, or they may be on a separate chip such as the DP84240/DP84244 octal memory drivers. The recommendations in this article are valid for any type of memory driver. The purpose of the article is to forewarn new designers using memories of problems they will encounter if adequate precautions are not taken.

A typical configuration of a 16-bit wide memory is shown in *Figure 1*. Each driver address output goes to every dynamic RAM, as does $\overline{WE}$. $\overline{CAS}$ outputs go to half the number of RAMs assuming byte writing is required. $\overline{RAS}$ outputs each go only to one bank. Note that these loads are not true for the data inputs and outputs. Each data I/O only connects to its respective bit, so the loading is only one RAM per bank for data. In general, this is why buffers are not required on the data bus when interfacing to memory. Data In of the RAMs can be linked directly to Data Out for any one bit, and also to the corresponding bit on the data bus. This is true for normal read and write operations, but if read-modify-write cycles are employed, the Data Out signals must be buffered from the data bus.

Using this typical memory configuration may not be as simple as it seems. Without care and attention, problems can arise for the unprepared, and there are two areas in particular which may cause memory errors or memory damage: one is voltage overshoot caused by inductive traces and high capacitive loads, the other is switching spikes caused by switching high capacitive loads.

OVERSHOOT AND UNDERSHOOT

(Undershoot is Negative Overshoot)

When a system requires a number of dynamic RAMs, the result is high capacitance loads, caused by a combination of RAM input capacitance and trace capacitance. Each dynamic RAM has a specified input capacitance of 10 pF maximum, but most dynamic RAMs are closer to 2 to 3 pF. Very few actually get close to 10 pF, even under worst case conditions of high temperature and V_{CC}. It is safe, therefore, to assume a much lower average input capacitance when using 16 or more RAMs.

In fact, the input capacitance of most inputs is due more to the package than the input gating, because the silicon gate inputs of the transistors in today's market have such high impedance. A typical maximum would be 2.5 pF. Control inputs such as $\overline{RAS}$ and $\overline{CAS}$ connect to more than one transistor input. For example, on the National Semiconductor 64k x 1 dynamic RAM, the NMC4164, $\overline{RAS}$ goes to two transistors and $\overline{CAS}$ to four. In general, this is true for most manufacturers' RAMs, so a more typical maximum input capacitance would be 3 pF for $\overline{RAS}$ and 3.5 pF for $\overline{CAS}$. RAM input currents are so small as to be negligible. The input current is quoted as 10 μA maximum, but again most RAMs are much less than this in a typical memory. Driving DRAMs, therefore, is not a problem of DC drive capability, but rather a problem of capacitance drive capability.

Driving DRAM input capacitance is further compounded by printed circuit traces, and even more so by wire-wrapping. Both can be represented by a transmission line with distributed capacitance and inductance. Thus, the total load is equivalent to a complex impedance comprising the distributed trace inductance, and a capacitance comprising distributed trace capacitance and RAM input capacitance as shown in *Figure 2a*.

The effect is an overshoot or undershoot at the dynamic RAM inputs that occurs each time a memory driver changes state, as shown in *Figure 2b*. As the driver output changes state, the load capacitance cannot be instantaneously charged or discharged because the current available is limited both by the driver transistor impedance, and the equivalent series resistance from the supply rail through the chip to the trace resistance. This current will be similar in value to the quoted short circuit current of the driver stage; therefore there is a spike of current that lasts as long as it takes to change the voltage of all the capacitances. For the driver stages of the DP8408A/DP8409A, or the DP84240/DP84244, the typical short circuit current is 100 mA per stage. This is true for either direction, so that the high-to-low transition takes roughly the same time as the low-to-high transition, minimizing skew times on all the driver outputs, as they transition in either direction. Assuming the output low voltage, V_{OL}, is 0.2V and the output high voltage, V_{OH}, is 3.2V, and that the charge/discharge current is constant at I_{SC}, then the current spike will exist for a time, T, where,

$$T = C_{IL} \times (V_{OH} - V_{OL})/I_{SC}$$
$$= 500\ pF \times 3.0V/100\ mA = 15\ ns$$

C_L (500 pF) is the load capacitance of typically 64 to 88 dynamic RAMs, in other words, four banks comprising 16 data bits and possibly six check bits if error correction is required.

In fact, due to the trace inductance, the rate of change of current will not be a step function, so that the current waveform looks like a spike. Even so, the rapid rate of change of current, di/dt, into the trace inductance L, will create a potentially excessive voltage "e" across this inductance. As an example, if the current changes from 0 to 100 mA in 6 ns, and the composite trace inductance is 0.3 μH, then the voltage across this inductance is "e," where,

$$e = L\ di/dt$$
$$= 0.3\ \mu H \times 100\ mA/6\ ns = 5V$$

In other words, at this rate of change in current, even a small inductance can be dangerous for two reasons. First, the dynamic RAMs at the far end of the trace could be destroyed, unless they have clamping diodes to V_{CC} and GND (most do not), or second, the returning voltage may exceed the threshold it has just passed causing a second

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and then third change of state. If this sudden glitch occurs on a control signal input such as $\overline{RAS}$, the memory contents may be inadvertently changed.

It is therefore necessary to remove the spike. The most common approach is to insert a damping resistor in the path between the driver and the RAMs, fairly close to the driver, as shown by R_D in *Figure 2a*. The best value for the resistor is the critical value giving a critically damped transition. Too high a value will cause overdamping which results in a slow transition. This slow edge may create excessive skew problems and slow down the memory cycle, or even worse, the edge may be slow enough that the RAM cycle never begins internally. If the damping resistor value is too low, the undershoot or overshoot may not be removed. It is therefore recommended that the resistor be determined on the first prototypes (not wire-wrapped prototypes because the value will be different due to the larger distributed inductance and capacitance). Also, the values may be different for the control lines, particularly $\overline{CAS}$. If there are a number of banks, and a $\overline{RAS}$ is used to select each bank, then the damping resistor in this line will be higher.

Typical values for the damping resistors will be between 15Ω and 100Ω, the lower the loading, the higher the values.

Some IC manufacturers offer octal memory drivers with on-chip series resistors fixed at ≈25Ω. Unless this is the critical value required for all the lines, problems will arise. The DP8400 family has been designed with equivalent internal values of approximately 10Ω, allowing for any external value of damping resistor.

SWITCHING CURRENT SPIKES

Another major undesirable effect of the fast current spikes is the effect on the V_{CC} and GND pins. The worst case is when all eight or nine address outputs switch in the same direction at the same time, as shown in *Figure 3a*. If each driver can source or sink 100 mA, then a current of approximately 1A could enter or exit the driver chip in a period of 20 ns. The resistance and inductance of the V_{CC} and GND lines to the chip can cause excessive drops during this switching time (see waveforms in *Figure 3a*), which may, in turn, upset latches either in the DP8408A/DP8409A, or externally. A ceramic capacitor connected across V_{CC} and GND pins will largely remove the spike. A 1 μF multilayer ceramic is recommended. This should be fitted as close as possible to the pins in order to reduce lead inductance. The DP8408A/DP8409A pin configuration facilitates this with

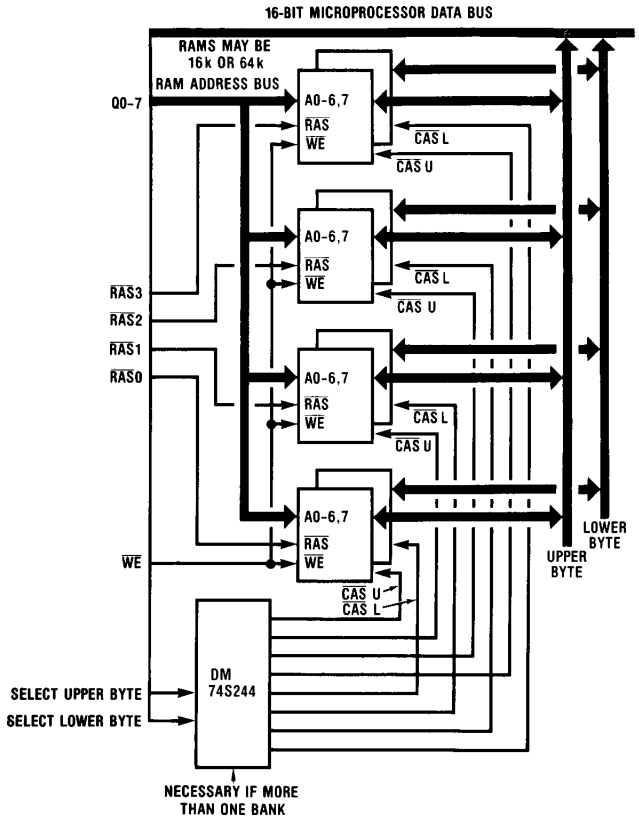

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FIGURE 1. Typical 16-Bit Memory with Byte Write Address

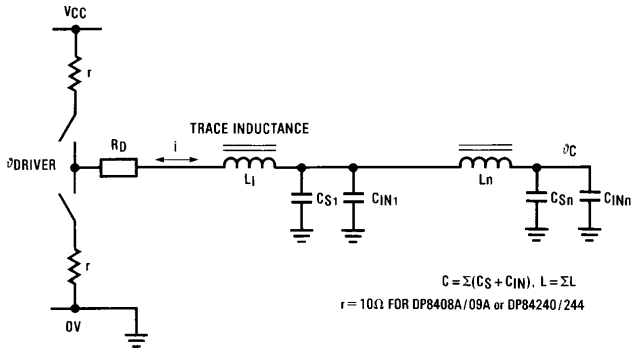

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FIGURE 2a. Complex Load Impedance Caused by Distributed Trace Inductance L and Capacitance C_S, and RAM Input Capacitance C_{IN}

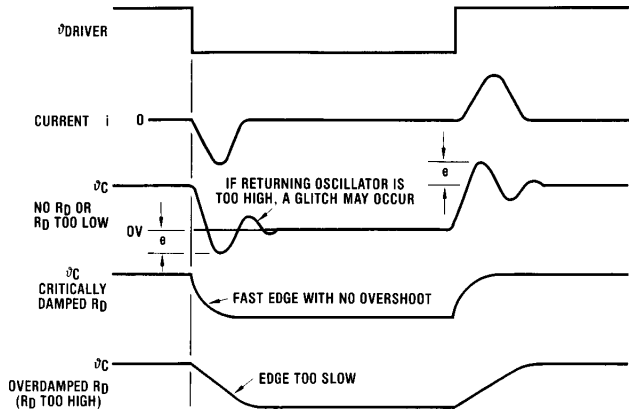

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FIGURE 2b. Timing Waveforms Showing the Effect of Variations of R_D on Signals Appearing at the RAM

GND and V_{CC} pins 0.2″ apart so that the ceramic capacitor can be fitted as close to the chip as possible. The second GND pin should also be decoupled. These GND and V_{CC} pins are located in the center of the package to reduce bonding lead lengths. In fact, the lead resistance is five times lower than if the supply pins were in the corners. An example of how this spike can be reduced would be the previous example of a 1A change in supply current switching in 20 ns with a 1 μF ceramic capacitor decoupling GND and V_{CC}. The voltage drop "v" is 1A$\times$20 ns/1 μF, or 20 mV.

If the decoupling capacitor was 0.01 μF, the drop would be 2V. Tantalum or other types of capacitors are lower frequency capacitors and have only a small effect in reducing the voltage spike. Ceramic capacitors are high frequency, and multilayer capacitors with lower inductance have a greater effect in reducing the voltage spike and are therefore recommended. As a further recommendation, the dynamic RAMs should be similarly decoupled with approximately a 0.1 μF ceramic capacitor on each RAM. Wire-wrapped boards, in particular, need special attention.

There are some other precautions that may be considered when driving memories. First, be aware that IC sockets increase load capacitance and inductance, so it becomes a matter of the importance of removability of chips, and maintainability. Also, shorter, thicker trace lengths will reduce the load, and good GND and V_{CC} connections will help reduce the voltage spikes around the memory board. For wire-wrapped designs, GND and V_{CC} should be multiwired.

With proper decoupling and correct selection of damping resistors, integrated circuit dynamic RAM controllers will function as expected to ease the burden of the system designer.

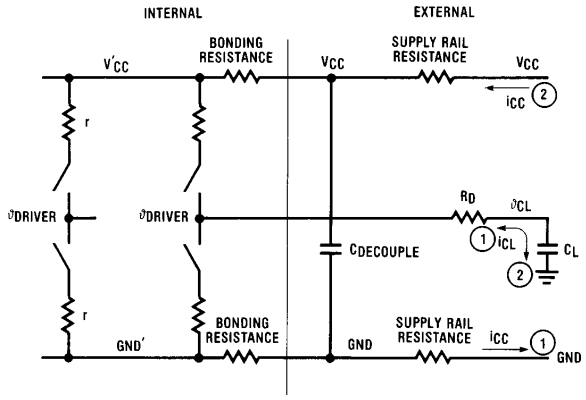

FIGURE 3a. Effect of Switching All Outputs Simultaneously in the Same Direction

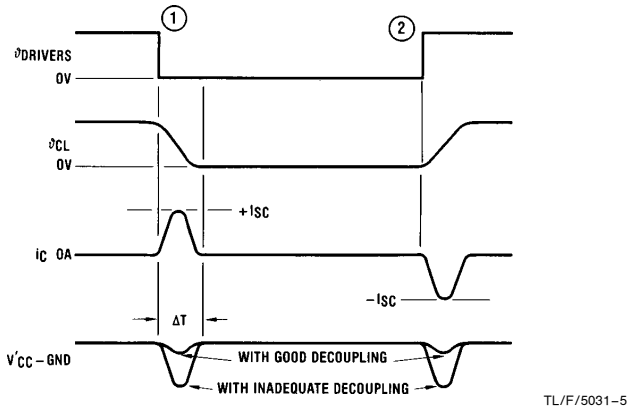

FIGURE 3b. Timing Waveforms Showing Internal Supply Rail Drops During Output Switching

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