MX·COM, INC.

1994 PRODUCT HANDBOOK

Mixed Signal ICs

1994

MX·COM, INC.

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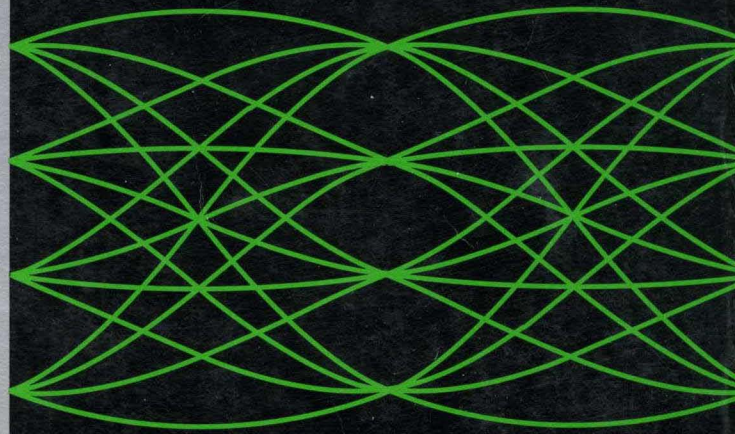

MiXed Signal ICs

Wireless Data Modems
Secure Speech
Continuous Tone Signaling
Sequential Tone Signaling
Voice Codecs
Audio Processors

MX•COM, INC.

MiXed Signal Integrated Circuit

Product Handbook

INTRODUCTION

This handbook presents technical specifications and application notes for MX•COM's MiXed signal integrated circuits.

MX•COM specializes in the development of high-performance, MiXed signal Application Specific Standard IC's for communication tasks such as:

- wireless modems
- sub-audio tone signaling
- speech security
- and voice storage/retrieval.

MX•COM offers quick turn-around design methodologies supported by specialized manufacturing facilities, comprehensive test, quality assurance, and prototype assembly backed by more than 10 years of telecommunication product design experience.

Call us at (910) 744-5050 or Toll-Free in the Continental U.S., Alaska and Canada at (800) 638-5577. Or Fax us at (910) 744-5054 for price, availability and applications assistance.

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MX118	Full-Duplex Scrambler for Cordless Telephones	p. 360			✔				✔	
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MX709	Voice Storage and Retrieval (VSR) Codec w/ SRAM	p. 403	✔			✔			✔	✔
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COMPANY PROFILE

MX•COM, INC., a member of CML Microsystems Plc. group of Witham, Essex, England, designs, manufactures and sells radio, telecommunication, and wireless data communications IC's. The company products utilize a mixed analog and digital CMOS process. The combination of detailed system knowledge and integrated circuit design capability has resulted in high-quality products for:

- Two-Way Mobile Radio
- Cellular Radio
- Modems for Radio Data Communications
- Voice Security/Voice Coding
- Paging
- Cordless Telephones
- Military Communications

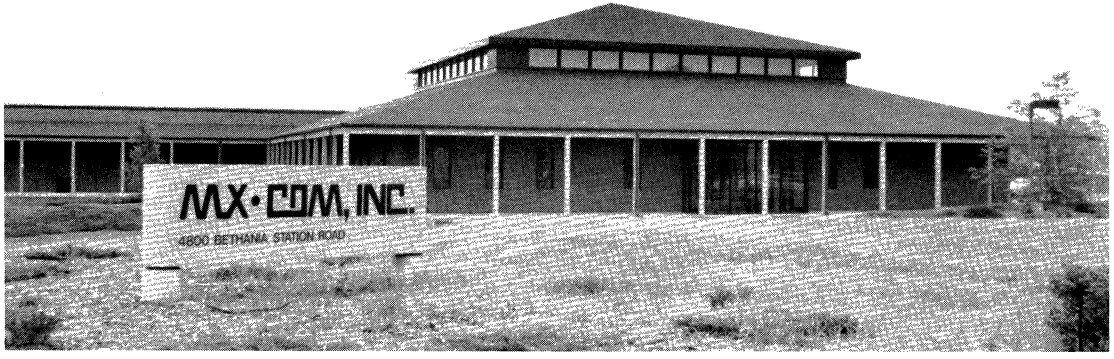
Although manufactured in separate facilities in North Carolina and the UK, the monolithic products of MX•COM and Consumer Microcircuits Ltd. (also a member of CML Microsystems Plc.) share similar form, fit and function. Each thereby serves as a 2nd source back-up of the other — unique among niche market IC suppliers.

FACILITIES

MX•COM occupies a 28,000 square foot purpose-built facility in Winston-Salem, NC. Product design, packaging and testing are performed at the Winston-Salem facility. Qualified foundries are used for wafer fabrication. All subcontractors are subject to stringent MX•COM specifications and oversight -- see "Quality and Reliability."

Customer visits to MX•COM are welcomed and can be arranged by contacting the sales department.

MX•COM has distributors and agents worldwide. See the inside back cover of this catalog for a complete listing.



MX•COM headquarters, Winston-Salem, North Carolina

DEVELOPMENT PROCESS

MX•COM's integrated circuit products focus on baseband signal processing for wireless telecommunication applications. To offer truly integrated solutions it is necessary to combine analog and digital technology on a single monolithic silicon substrate ("mixed signal" technology).

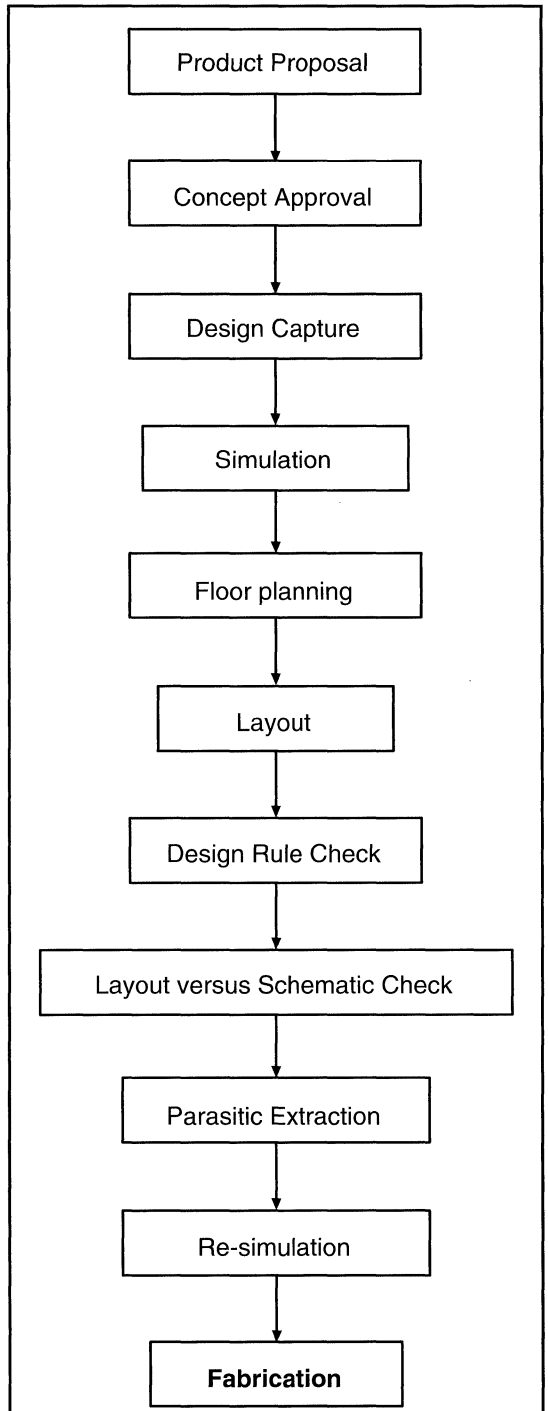
MX•COM's integrated circuit designers follow a clearly defined protocol from the conceptual phase through device fabrication (see figure at right). State of the art CAD tools are a critical component to all phases of this process. Maximizing the usage of CAD tools minimizes the probability of errors from human intervention.

The concept phase involves the use of high-level system simulators for verifying the approach to a particular design. Ultimately, this process yields a top-level block diagram which must be approved by key departments throughout MX•COM. The next step is design capture. This consists of turning the top-level block diagram into a transistor level representation. The transistor level design is then simulated using a proprietary analog simulator (similar to SPICE) in conjunction with an industry standard digital simulator. The simulation results are carefully analyzed, and any necessary improvements are made. When the results are satisfactory the design is ready for the layout phase.

The first step in the layout phase, and the most critical, is "floor planning." In MX•COM's mixed-signal devices high performance analog circuitry is completely isolated from on-chip digital sections, ensuring optimum noise performance. After a suitable floorplan is agreed upon the actual layout begins. Layout is accomplished using a combination of computer generated (auto-routing) and full-custom techniques. Once the layout is complete the verification phase begins.

In the verification phase the layout is first checked for design rule violations. When all design rule violations are removed the layout is compared to the schematic and/or HDL (Hardware Description Language) using a "Layout versus Schematic" CAD tool. After this comparison the design is completely re-simulated. But this time the input for the simulator is extracted from the layout, including the parasitic effects due to routing. When the results of the re-simulation compare favorably to the previous simulation the design is ready for fabrication.

IC design at MX•COM is a highly structured, meticulous process. The end result is a family of products that offer the highest levels of performance and integration attainable.



Integrated Circuit Development Protocol

QUALITY AND RELIABILITY

MX•COM is committed to the quality that grows customers. Our policy is to only provide products that conform to realistic, documented standards that establish fitness for use and assure continued performance over time.

Producing quality products requires:

- Knowledge - knowing what to do,
- Skills - being able to do it,
- and Continuous Improvement - getting better every day.

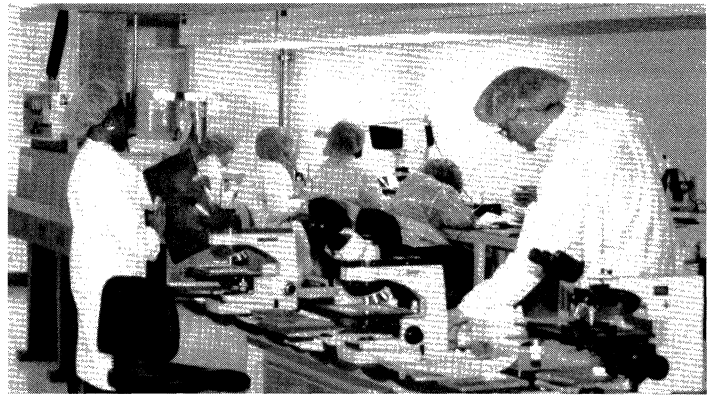
Knowledge is obtained through careful market and product definition which includes the involvement and feedback of valued and potential customers, and by actively participating on industry standards committees.

Skills are provided by talented and dedicated employees. Continuing training is provided to maintain existing skills, to promote employee awareness and to develop needed new skills and knowledge. Additionally, MX•COM continues to make substantial capital investments necessary to support design, manufacturing, and quality activities and objectives.

Continuous Improvement is a necessary element of any quality effort, and MX•COM is no exception. **In 1994, MX•COM expects to complete ISO-9000 certification**, and subsequently intends to build on this through the Malcolm Baldrige process to achieve quality levels second to none.

Quality and reliability are an integral part of product definition objectives and manufacturing practice. For instance, MX•COM products are implemented using conservative design rules and fabricated using well-established processes from qualified foundries. The product is then assembled at the MX•COM facility in North Carolina or by qualified third party assembly operations. The MX•COM assembly process is qualified to Mil Standard 45208. Conformance to specification for sub-contract assembly and wafer production is strictly monitored through inspection and audit procedures. Electrical test, at wafer level and finished assembly, is performed at the Winston-Salem facility using proprietary hardware and software. Product traceability is provided throughout the production cycle.

MX•COM's quality objective is total customer satisfaction.



IC Assembly is Performed in MX•COM's Clean Room

DATA SHEET IDENTIFIERS

All products in this catalog may be classified in one of the following ways:

Identifier	Product Status	Comments
None	Full Production	Guaranteed limits will not be changed except through formal change procedures that update specifications upon the next publication issue -- contact MX•COM,INC for current information.
Preliminary	Pre-Production	The test limits specified are predicated on an incomplete statistical sampling, possibly taken from only an initial production batch, and are therefore likely to change.
Advance	Samples Pending	Specificatons are based on unproved design targets of products in development.

CUSTOMER SUPPORT

Backing up our products is a team of factory and worldwide manufacturing reps (see inside back cover) staffed by sales and application engineers who can provide a wealth of information, as well as identify additional resources to help develop customer products. In addition, our technical literature discusses radio and modem technology and applications. Other services include on-site design support or factory analysis of any issues our customer may have.

ORDERING INFORMATION

Please specify the device package type when placing an order. Package type suffix codes are defined below. See the last section of the catalog for package dimensions.

Example: MX165BP

- Device
- Major Revision Level (A, B, C, etc.)
- Package Style
  - J = Ceramic Dual In-Line
  - P = Plastic Dual In-Line
  - LH, LH8 = Plastic Leaded Chip Carrier
  - DW = Small Outline Integrated Circuit
  - TG = Thin Quad Flat Pack
  - TS = Thin Shrink Small Outline Package

SECOND SOURCE: A qualified second source for MX•COM integrated circuits is Consumer Microcircuits Limited. Device numbers on Consumer's and MX•COM's products are the same with the following exceptions:

- Where MX•COM products bear an "MX" prefix, Consumer's products bear an "FX" prefix. For example, a Consumer's FX365A is the equivalent of an MX•COM MX365A.
- MX•COM's and Consumer's products may not have identical pin-outs or package styles. Call the factory for more information.
- Some MX•COM and Consumer's package styles have different suffixes:

	MX•COM	Consumer's
24-lead Plastic Leaded Chip Carrier	LH	LS
28-lead Plastic Leaded Chip Carrier	LH8	LH

TO PLACE AN ORDER:
In the U.S. and Canada, call or write the MX•COM sales department:

Attn: Sales Dept.
MX•COM, Inc.
4800 Bethania Station Rd.
Winston-Salem, NC 27105

Phone: (910) 744-5050 OR (800) 638-5577 (Toll-Free in the Continental U.S., Alaska and Canada)
Fax (910) 744-5054.

The phones are staffed from 8AM to 5PM E.S.T., Monday through Friday.
Terms of payment are net 30 days with approved credit, F.O.B. Winston-Salem, NC.
In the Far East or Europe, please contact the authorized distributors listed on the inside back cover of this catalog.

Final Test is Performed in Clean, Controlled Environment

Technical Specifications

MiXed Signal
Integrated Circuits

The following sections contain specifications on
MX•COM's MiXed Signal IC's.

Section 1: Wireless Modems

The following section contains specifications on MX•COM's Wireless Modem IC's

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MX439	1200 bps MSK Modem with Serial Control	p. 29	
MX469	1200/2400 bps MSK Modem with Serial Control	p. 35	
MX589	40k bps GMSK Modem with Serial Control	p. 43	
MX809	1200 bps MSK Modem with C-BUS Control	p. 57	
MX909	High-Speed and MOBITEX GMSK Modem	p. 70	**NEW**
MX919/929	High-Speed 4-Level FSK Modem/ARDIS	p. 103	**NEW**
MX939	CDPD/AMPS-WBD Full-Duplex Modem	p. 140	**NEW**

GUIDE TO MX-COM MODEMS

MODEM	SPEED (BPS)	DUPLEX	µP INTERFACE	POWERSAVE MODES	XTAL (MHz)	PROTOCOLS STANDARDS	ADDITIONAL FEATURES
MX429	1200 MSK	FULL	8-BIT PARALLEL	YES 1mA TYP.	4.032	TRUNKED RADIO BAND III MPT 1317/1327	HIGH INTELLIGENCE ERROR CHECKING IN RX ERROR CHECK WORD GENERATION FRAME SYNC/SYNT DETECTION
MX529	1200 MSK	FULL	8-BIT PARALLEL	YES 1mA TYP.	4.032	TRUNKED RADIO PAA 1382 ETSI/EBSS 1200	HIGH INTELLIGENCE ERROR CHECKING IN RX ERROR CHECK WORD GENERATION FRAME SYNC/SYNT DETECTION PIN/FUNCTION COMPATIBLE WITH MX429
MX439	1200 MSK	FULL	NO	YES 650µA TYP.	4.032 or 1.008	GEN. DATA TRUNKED RADIO ZVEI/BOS/R2000 NMT 450/900	ON-CHIP RX & TX BANDPASS FILTERS ON-CHIP CLOCK RECOVERY PIN-SELECTABLE XTAL/CLOCK FREQ.
MX469	1200 2400 MSK	FULL	NO	YES 650µA TYP.	4.032 or 1.008	GEN. DATA TRUNKED RADIO BAND III ZVEI/BOS/R2000 NMT 450/900	ON-CHIP RX & TX BANDPASS FILTERS ON-CHIP CLOCK RECOVERY PIN-SELECTABLE XTAL/CLOCK FREQ. PIN/FUNCTION COMPATIBLE WITH MX439
MX589	4k TO 40k GMSK	FULL OR HALF	NO	YES 1mA TYP.	4.096 4.9152 2.048 2.4576	CDPD RAM-MOBITEX HIGH-SPEED DATA UNIVERSAL DATA	RX & TX DATA CLOCK GENERATION SERIAL RX & TX DATA INTERFACES SELECTABLE BT (0.3 OR 0.5) PIN/FUNCTION COMPATIBLE WITH MX489
MX809	1200 MSK	HALF	SERIAL "C-BUS"	YES 2mA TYP.	4.032	UNIVERSAL TRUNKED RADIO MODEM	HIGH INTELLIGENCE MPT1327 ERROR CHECKING SELECTABLE CHECKSUM GEN.
MX909	4.8/9.6/19.2k OR 4/8/16k	HALF	8-BIT PARALLEL	YES 1mA TYP.	1 to 10	RAM-MOBITEX	AUTO. HANDLES MOBITEX FRAME STRUCT. HIGH-SPEED DATA TRANSMISSION
MX919	4.8/9.6/19.2k 4-Level FSK	HALF	8-BIT PARALLEL	YES 1mA TYP.	2 to 10	UNIVERSAL	AUTO. HANDLES GEN/PURP. FRAME STRUCT. "SOFT" VITERBI RX SIGNAL DECODING & ERROR CORRECTION
MX929	4.8/9.6/19.2k 4-Level FSK	HALF	8-BIT PARALLEL	YES 1mA TYP.	2 to 10	RD-LAP	AUTO. HANDLES RD-LAP FRAME STRUCT. "SOFT" VITERBI RX SIGNAL DECODING & ERROR CORRECTION
MX939	10/19.2k GMSK	FULL	8-BIT PARALLEL	YES 1mA TYP.	1.44	CDPD AMPS-WBD	SAT TONE DETECTION & REGENERATION SERIAL RX & TX DATA INTERFACES

MX-COM, INC.

MX429
MX529

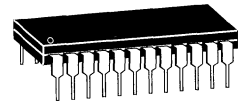
STANDARD PROTOCOL MSK MODEM FOR TRUNKED RADIO

FEATURES

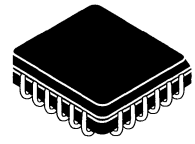
- **Full-duplex Operation**
- **Generates Preamble / Detects Carrier**
- **Flags Both Control & Traffic Frames**
- **Detects Errors / Outputs Symptom**
- **High Data Throughput for 2-way Radio**

APPLICATIONS

- **Standard Protocol Radio Trunking Systems**
- **Mobile Radio SELCALL, ANI, Status, Data**
- **MX429: British MPT1327 Signaling**
- **MX529: French PAA 1382 Signaling**



MX429J/529J (CDIP)
MX429P (PDIP)
24 pins



MX429LH/529LH
24-pin PLCC

DESCRIPTION

The MX429 and MX529 are single-chip, low-power CMOS 1200 baud MSK Modems, designed primarily for use in trunked radio, telemetry and packet radio applications. The MX429 has been designed to conform to the MPT1317/1327 UK Band III trunked radio protocols. The MX529 has been designed for both the PAA 1382 French trunked radio and the proposed ETSI EBSS 1200 Digital Signaling Specifications.

The devices are full-duplex at 1200 baud and include an 8-bit parallel microprocessor interface. The on-chip programmable timer may be set for interrupt periods of 8 to 120 bits. Preamble and an error check word are automatically generated in Transmit mode. Error checking is performed and the 16-bit SYNC or SYNT words are detected in Receive.

An on-chip xtal/clock generator which requires an external 4.032 MHz xtal or clock input provides 4.032 and 1.008 MHz outputs. In addition, it performs all modem timings. The MX429/MX529 requires a single 5 volt power supply and has powersave circuitry. They are available in 24-pin Cerdip, 24-pin PDIP or 24-lead PLCC packages.

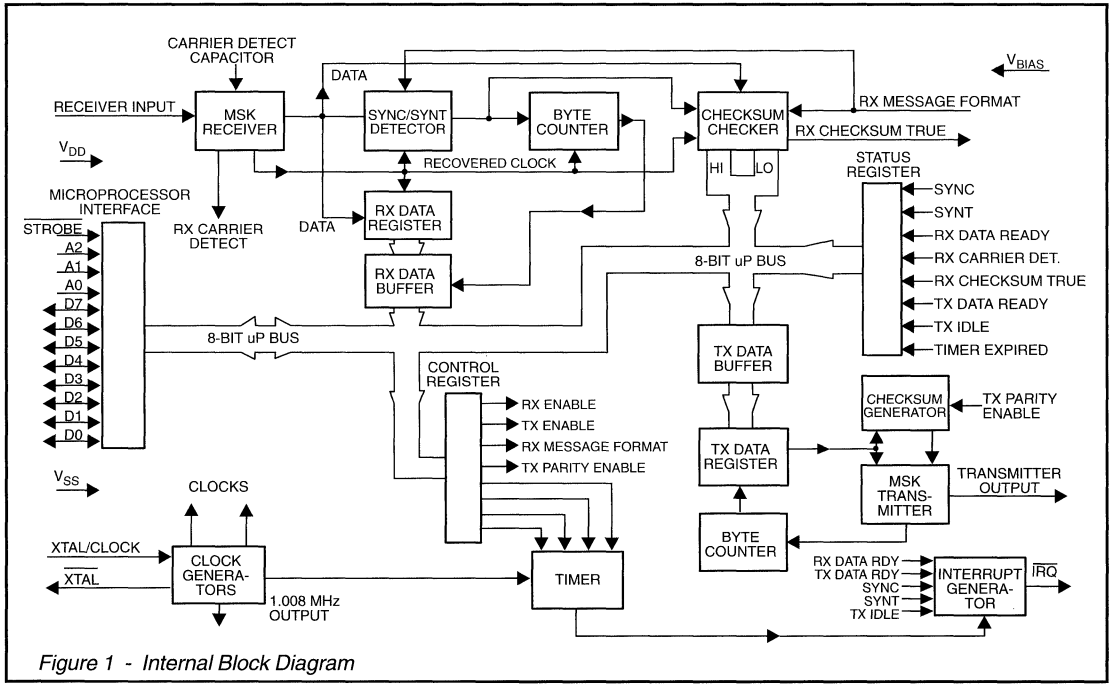


Figure 1 - Internal Block Diagram

PIN FUNCTION TABLE

Pin J,P	Pin LH	Function
1	1	V_{BIAS}: The internal circuitry bias line, held at $V_{DD}/2$. This pin must be decoupled to V_{SS} by capacitor C_4. See Figure 3.
2	2	TRANSMIT OUTPUT: The 1200 baud, 1200/1800Hz MSK TX output. When not enabled by the Control Register (D_0), the output is set to a high impedance state.
3	4	RECEIVER INPUT: The 1200 baud received MSK signal input. The 1200/1800 Hz audio to this pin must be a.c. coupled via capacitor C_3. See Figure 3.
5	5	V_{DD}: Positive supply. A single +5V regulated supply is required. It is recommended that this power rail be decoupled to V_{SS} by capacitor C_6. See Figure 3.
6	6	CARRIER DETECT TIME CONSTANT: The on-chip carrier detect integration function requires a capacitor, C_5, to V_{SS}, together with a resistor, R_2, to V_{DD}, that determine the carrier detect response time.
7	7	XTAL/CLOCK: The input to the clock oscillator inverter. A 4.032 MHz Xtal or externally derived clock pulse input should be connected here. See Figure 3.
8	8	$\overline{XTAL}$: The output of the 4.032 MHz clock oscillator.
9 10 11 12 13 14 15 16	9 10 11 12 13 14 15 16	D_0: Microprocessor Data Interface D_1: D_2: D_3: These eight lines are used by the device to communicate with a D_4: microprocessor, and with the A_0, A_1 and A_2 inputs D_5: determining register selection. D_6: D_7:
17 18	17 18	A_0: REGISTER SELECTION: These inputs, with the A_2 input,select the A_1: required register to the data bus as shown in Table 1 (below).
19	19	$\overline{STROBE}$: This input performs the dual functions of selecting the device for Read or Write and strobing data in or out. It should be generated by gating high order address bits with a read-write clock. This device is selected when $\overline{STROBE}$ = 0 (see Figure 5). NOTE: If data at inputs D0-D7 changes during $\overline{STROBE}$ an interrupt may occur.
20	20	A_2: This input determines which internal registers are connected to the Data Interface pins (D0-D7) during $\overline{STROBE}$ (see Table 1 and Figure 5).
21	21	$\overline{IRQ}$: Interrupt Request. This line will go to a logic "0" when an interrupt occurs. This output can be "wire OR'd" with other active low components (100 kΩ pullup to V_{DD}).The conditions that cause the interrupts are indicated at the Status Register and are as follows: Timer Expired — RX Data Ready — TX Data Ready TX Idle — RX SYNC Detect — RX SYNT detect

Table 1

Register	A_2	A_0	A_1
Control	0	1	1
Status	1	1	1
RX Data	1	0	1
TX Data	0	0	1
Syndrome Low	1	0	0
Syndrome High	1	1	0

PIN FUNCTION TABLE

Pin		Function
J,P	LH	
23	22	V_{SS}: Negative Supply (GND)
24	23	CLOCK÷4: A 1.008 MHz ($X_1 \div 4$) clock is available at this output for external circuit use. Note the source impedance and source current limits.
4,22	3,24	These pins are not connected. Leave open circuit.

Modems in Mobile Data Signaling...An Introduction

Digital Code Format

The MPT1327 Signaling Standard for Trunked LMR Systems protocol is used by the MX429 for communication between a trunking system controller (TSC) and users' radio units. The PAA 1382 Signaling standard protocol is used for the MX529. These data stream formats are summarized in Figure 2.

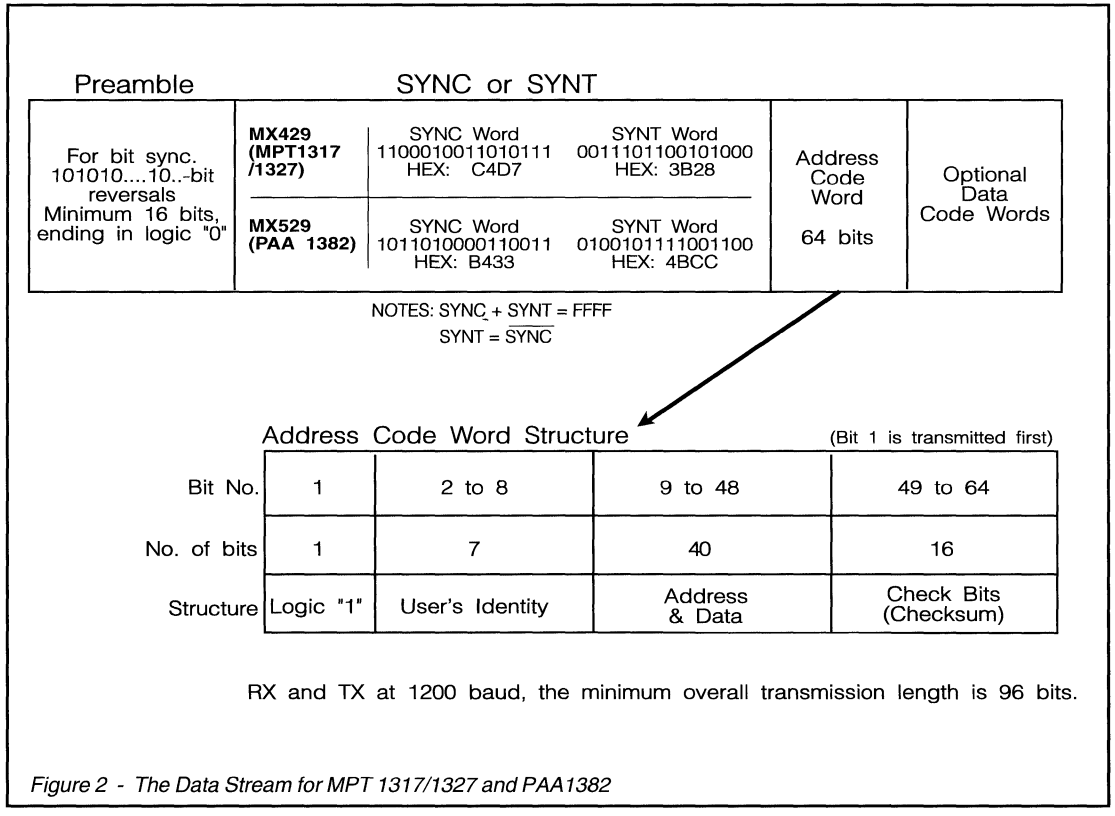


Figure 2 - The Data Stream for MPT 1317/1327 and PAA1382

Modems in Mobile Data Signaling...An Introduction (Cont.)

Operation

The MX429/529 can be used in full-duplex mode in conjunction with a host microprocessor. The µP operates on the data, while the MX429/529 handles all other signaling routines and requirements.

In the TX mode, the MX429/529 will:

(1) Internally generate and transmit a preamble for system bit synchronization,

(2) Accept from the host and transmit a 16-bit SYNC or SYNT word,

(3) Accept from the host and transmit 6 bytes of data (Address Code Word) and, upon a software command,

(a) internally calculate and transmit a 2-byte checksum based on the previous 6 data bytes, or
(b) disable internal checksum generation and allow continuous data transmission, and

(4) Transmit one "hang bit" and go idle when all loaded data traffic has been sent (followed by a "TX Idle" interrupt).

In the RX mode, the MX429/529 will:

(1) Detect and achieve bit synchronization within 16 bits,

(2) Search for and detect the 16-bit SYNC or SYNT word,

(3) Output all received data after SYNC/SYNT in byte form, and

(4) Upon a software command (RX Message Format), use the received checksum to calculate the presence (if any) of errors and advise the host with an interrupt and a 16-bit Syndrome word.

Note: In the RX mode, a software command tells the MX429/529 to expect either a SYNC/SYNT word every 8 received bytes (6 data + 2 checksum) or a continuous data stream. Normally the SYNC word is used on the Control channel and the SYNT word is used on the Traffic data channel.

Non-MPT Application (Full-Duplex)

The functions described here can be accessed via the commands and indications detailed in the Register Instructions pages.

Transmit: When enabled, the device transmits a "101010...010" preamble until data for transmission is loaded by the host microprocessor. The MX429/529 will transmit 6 bytes of the loaded data followed by a 2 byte checksum based on that data. As long as TX data is being loaded, the transmitter will transmit in the 6 byte data/2 byte checksum format.

Automatic checksum generation can be inhibited by a software command, allowing transmission of continuous data streams.

Receive: A 16-bit SYNC or SYNT word is required (see note above) before output of data bytes. The modem receiver will then output continuous bytes of data. After every 6 bytes, a 2-byte checksum word will be generated, which can be ignored or used for error checking.

Control Register $A_1 = 1$ $A_0 = 1$ $A_2 = 0$ Write Only

The Control Register, when selected, directs the modem's operation as described below.

Bit	Description	Function	Set = logic "1" (High)	Clear = logic "0" (low)
Bit 0 D_0	**TX Enable ***	**Set** - D_0 enables the transmitter for operation. A "0-1" transition causes bit synchronization and the start of 1010.....10 preamble pattern transmission. At least one byte of preamble will be transmitted. If data is loaded into the TX Data Buffer before one byte has been sent, then that data will follow. Otherwise, whole bytes of preamble will continue until data is loaded. **Clear**- The Transmitter Output pin is set to a high impedance and no transmitter interrupts are produced.		

Control Register $A_1 = 1$ $A_0 = 1$ $A_2 = 0$ Write Only

Bit 1 **D_1** **TX Parity Enable**

Set - D_1 indicates to the transmitter that 2-byte checksums are to be generated by the modem. A "0-1" transition starts checksum generation on the next six bytes loaded from the TX Data Buffer into the TX Data Register. Checksum generation continues for every six bytes loaded until this bit is cleared. The transmitter will send the generated checksum (2 bytes) after the last of each 6 bytes have been sent. If an underrun (no more data loaded) condition occurs before 6 bytes have been loaded, checksum generation will abort, the transmission will cease after one "hang" bit has been sent, and Bit 4 in the Status Register (TX Idle) will be set. No checksum will be transmitted.
Clear - No checksum generation is carried out and the host may supply the checksum bytes. The output is then "as written."

Bit 2 **D_2** **RX Enable ***

Set - D_2 enables the receiver for operation. No data is produced (i.e. no RX Ready interrupts) until a SYNC or SYNT word is found in the received bit stream.
Clear - The receiver is disabled and all interrupts caused by the receiver are inhibited.

Bit 3 **D_3** **RX Message Format**

Set - D_3 is sampled after a checksum has been received and allows the host to control the way the receiver handles the following data bits. If set, the receiver will assume that the next 6 bytes are data and will start error checking accordingly.
Clear - The receiver will stop data transfer to the host after the 2 checksum bytes until another SYNC or SYNT frame word is received.

Bit 4 **D_4** **Timer LSB**

Bit 5 **D_5** **Timer**

Bit 6 **D_6** **Timer**

Bit 7 **D_7** **Timer MSB**

These 4 bits control the timer as follows:

D_7	D_6	D_5	D_4		
0	0	0	0	Reset Counter and disable timer interrupts	
0	0	0	1	Count and interrupt every	8 bits
0	0	1	0	" " "	16 bits
0	0	1	1	" " "	24 bits
0	1	0	0	" " "	32 bits
0	1	0	1	" " "	40 bits
0	1	1	0	" " "	48 bits
0	1	1	1	" " "	56 bits
1	0	0	0	" " "	64 bits
1	0	0	1	" " "	72 bits
1	0	1	0	" " "	80 bits
1	0	1	1	" " "	88 bits
1	1	0	0	" " "	96 bits
1	1	0	1	" " "	104 bits
1	1	1	0	" " "	112 bits
1	1	1	1	" " "	120 bits

If a new timer value is written to these inputs within 1 byte period of the last timer interrupt, the next timer period will be correct without first having to reset the timer. Otherwise, the timer must be reset to zero and then set to the new time.

***Note:**

Enabling Times - The time taken to enable one section (receiver or transmitter) when both sections are initally disabled is 16 bit periods. If one section (receiver or transmitter) is already enabled this time is reduced to 1/2 bit period.

TX Enable - If using the internal TX Preamble generation circuitry, e.g. with the internal timer setting the preamble length, the device occasionally produces a TX Data Ready interrupt immediately after a TX Enable. Software should handle this by either:

1) Detecting that the Timer Interrupt status bit is not set and that it is not appropriate to load data for TX at that time.

or 2) By not using the timer, i.e. immediately after TX Enable, reading the status register and loading a byte of preamble. This resets any interrupt. The length of the preamble transmitted is now controlled by the number of bytes loaded.

Status Register $A_1 = 1$ $A_0 = 1$ $A_2 = 1$ Read Only

When an interrupt is generated the $\overline{IRQ}$ output goes Low with the Status Register bits indicating the sources of the interrupt.

Bit	Description	Function	Set = logic "1" (High)	Clear = logic "0" (low)

Bit 0 D_0 — RX Data Ready

D_0, when set, causes an interrupt indicating that received data is ready to be read from the RX Data Buffer. This data must be read within 8 bit periods.
Set - when a byte of data is loaded into the RX Data Buffer, if a frame (SYNC/SYNT) word has been received.
Bit and Interrupt Cleared - a) by a read of the Status Register followed by a read of the RX Data Buffer or b) by RX Enable going Low.

Bit 1 D_1 — RX Checksum True

D_1, when set, indicates that the error checking on the previous 6 bytes agreed with the received checksum. This function, which is valid when the RX Data Ready bit (D0) is set for the second byte of received checksum, does not cause an interrupt.
Set - by a correct comparison between the received and generated checksums.
Cleared - a) by a read of the Status Register followed by a read of the RX Data Buffer, or b) by RX Enable going Low.

Bit 2 D_2 — RX Carrier Detect

D_2 is a "real time" indication from the modem receiver's carrier detect dircuit and does not cause an interrupt. When MSK tones are present at the receiver input, this bit goes High. With no MSK input, it goes Low. When the RX Enable bit (D_2 - Control Register) is Low, RX Carrier Detect will go Low.

Bit 3 D_3 — TX Data Ready

D_3, when set, causes an interrupt to indicate that a byte of data should be written to the TX Data Buffer within 8 bit periods.
Set - a) when the contents of the TX Data Buffer are transferred to the TX Data Register, or b) when theTX Enable is set--No interrupt is generated in this case.
Bit Cleared - a) by a read of the Status Register followed by a write to the TX Data Buffer, or b) by TX Enable going Low.
Interrupt Cleared - a) by a read of the Status Register, or b) by TX Enable going Low.

Bit 4 D_4 — TX Idle

D_4 causes an interrupt when set to indicate that all loaded data and one "hang" bit have been transmitted.
Set - one bit period after the last byte is transmitted. This last byte could be either "checksum" or "loaded data" depending on the TX Parity Enable state (Control Register D_1).
Bit Cleared - a) by a write to the TX Data Buffer, or b) by TX Enable going Low.
Interrupt Cleared - a) by a read of the Status Register, or b) by TX Enable going Low.

Bit 5 D_5 — Timer Interrupt

D_5, when set, causes an interrupt to indicate that the set timer period has expired. (Control Register D_4 - D_7).
Set - by the timer.
Bit and Interrupt Cleared - by a read of the Status Register.

Bit 6 D_6 — RX SYNC Detect *

D_6, when set, causes an interrupt to indicate that a 16-bit SYNC word (see Figure 2) has been detected in the received bit stream.
Set - on receipt of the 16th bit of a SYNC word.
Bit Interrupt and Cleared - a) by a read of the Status Register, or b) by RX Enable going Low.

Bit 7 D_7 — RX SYNT Detect *

D_7, when set, causes an interrupt to indicate that a 16-bit SYNT word (see Figure 2) has been detected in the received bit stream.
Set - on receipt of the 16th bit of a SYNT word.
Bit and Interrupt Cleared - a) by a read of the Status Register, or b) by RX Enable going Low.

***Note**

SYNC and SYNT Detection is disabled while the checksum checker is running.

RX Data Buffer $A_1 = 1$ $A_0 = 0$ $A_2 = 1$ **Read Only**

These 8 bits are the last byte of data received. Bit 7 is received first. *Note the relative positions of the MSB and LSB presented in this stream: the position may be different from the convention used in other microprocessor peripherals.*

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
LSB	-	-	-	-	-	-	MSB

TX Data Buffer $A_1 = 1$ $A_0 = 0$ $A_2 = 0$ **Write Only**

These 8 bits loaded into the TX Data Buffer are the next byte of data that will be transmitted (bit 7 first). *Note the relative positions of the MSB and LSB presented in this stream: the position may be different from the convention used in other microprocessor peripherals.* If the TX Parity Enable bit (Control Register D_1) is set, a 2-byte checksum will be inserted and transmitted by the modem after every 6 transmitted "message" bytes.

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
LSB	-	-	-	-	-	-	MSB

The Syndrome Word

This 16-bit word (both Low and High bytes) may be used to correct errors.

Bits S_1 to S_{15} are the 15 bits remaining in the polynomial divider of the checksum checker at the end of 6 bytes of "received message." For a correct message all 15 bits (S_1 to S_{15}) will be zero.

The 2 Syndrome bytes are valid when the RX Data Ready bit (Status Regiser D_0) is set for the second byte of the received checksum and should be read, if required, before 8 byte periods.

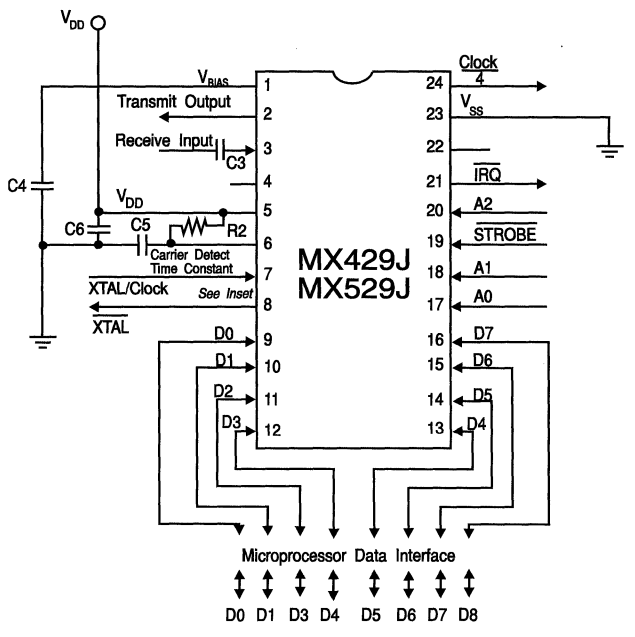
Syndrome Low Byte $A_1 = 0$ $A_0 = 0$ $A_2 = 1$ **Read Only**

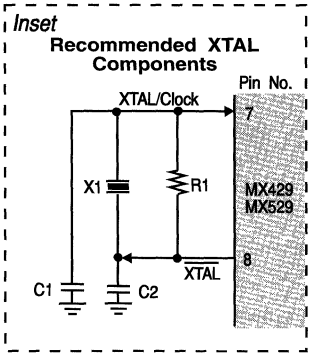
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
S1	S2	S3	S4	S5	S6	S7	S8

Syndrome High Byte $A_1 = 0$ $A_0 = 1$ $A_2 = 1$ **Read Only**

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
S9	S10	S11	S12	S13	S14	S15	Parity Error

D_7 is a "Parity Error Bit" indicating an error between the received parity bit and the parity bit internally generated from the incoming message. So for a correctly received message all 16 bits of the Syndrome Word (S_1 to S_{15} and Parity Error) will be zero.





Component References

Component	Unit Value
R1	1M
R2	1M
C1	33p
C2	33p
C3	0.1µ
C4	1.0µ
C5	1.0µ
C6	1.0µ
X1	4.032MHz

Tolerances: Resistors ±10%
Capacitors ±20%

Figure 3 - Recommended External Components

Carrier Detect Capacitor

The value of the Carrier Detect Capacitor, C_5, determines the carrier detect time constant. A long time constant (larger value C_5) results in improved noise immunity but increased response time. C_5 may be varied to optimize noise immunity/response time.

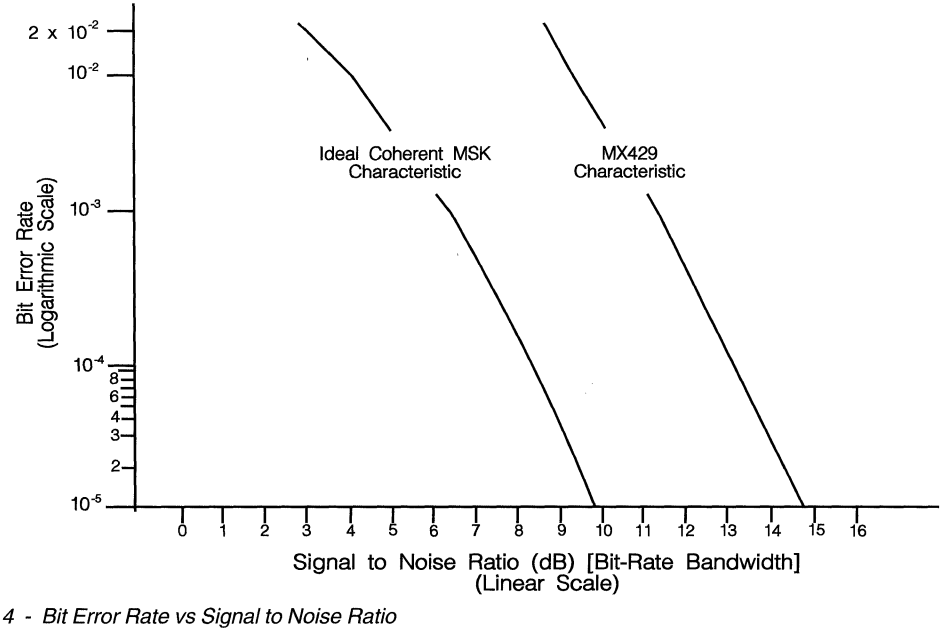


Figure 4 - Bit Error Rate vs Signal to Noise Ratio

Timing Information

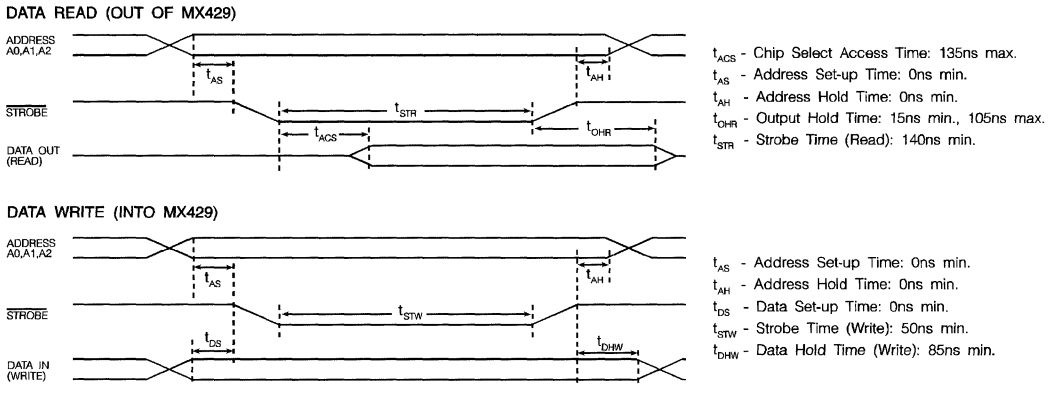


Figure 5 - Read and Write Timing Diagram

RX Operation

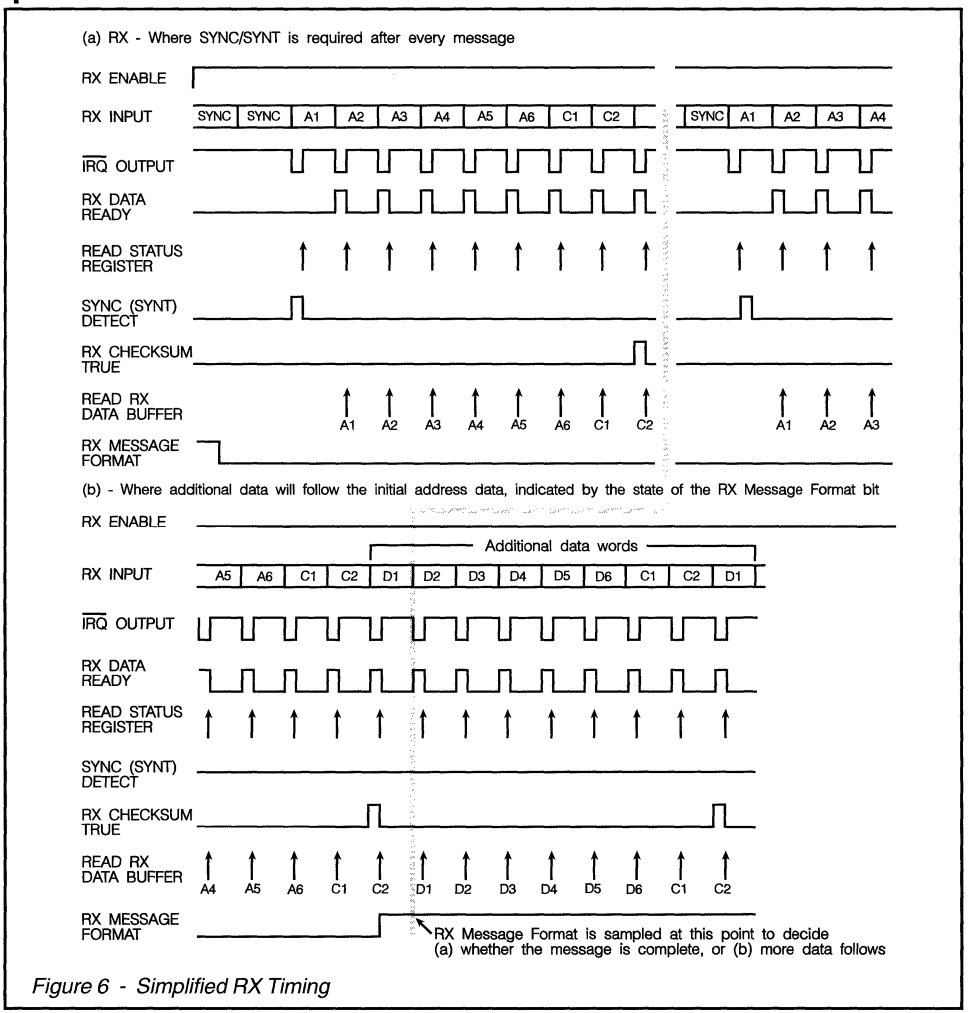


Figure 6 - Simplified RX Timing

TX Operation

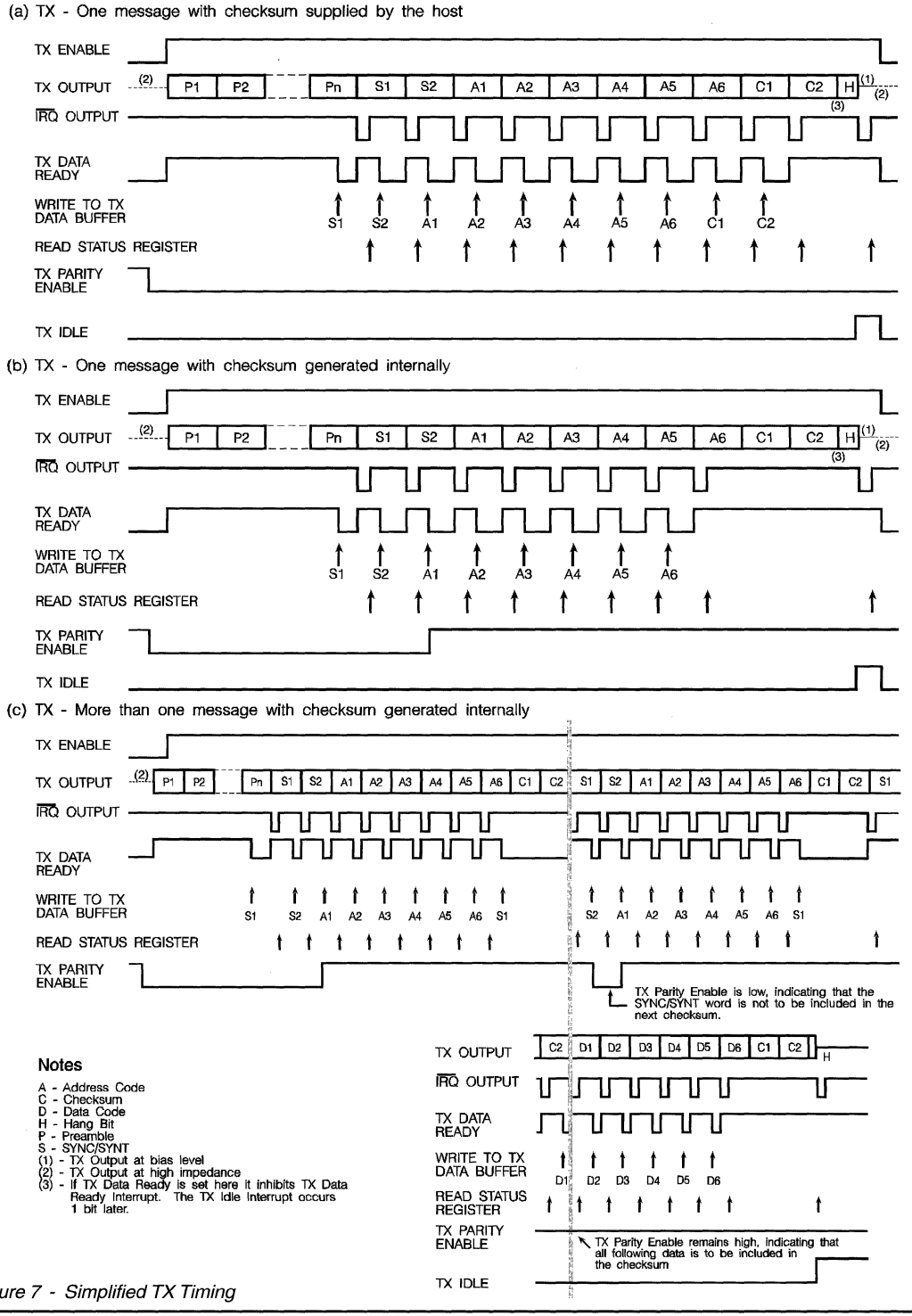


Figure 7 - Simplified TX Timing

Basic Power-up Software

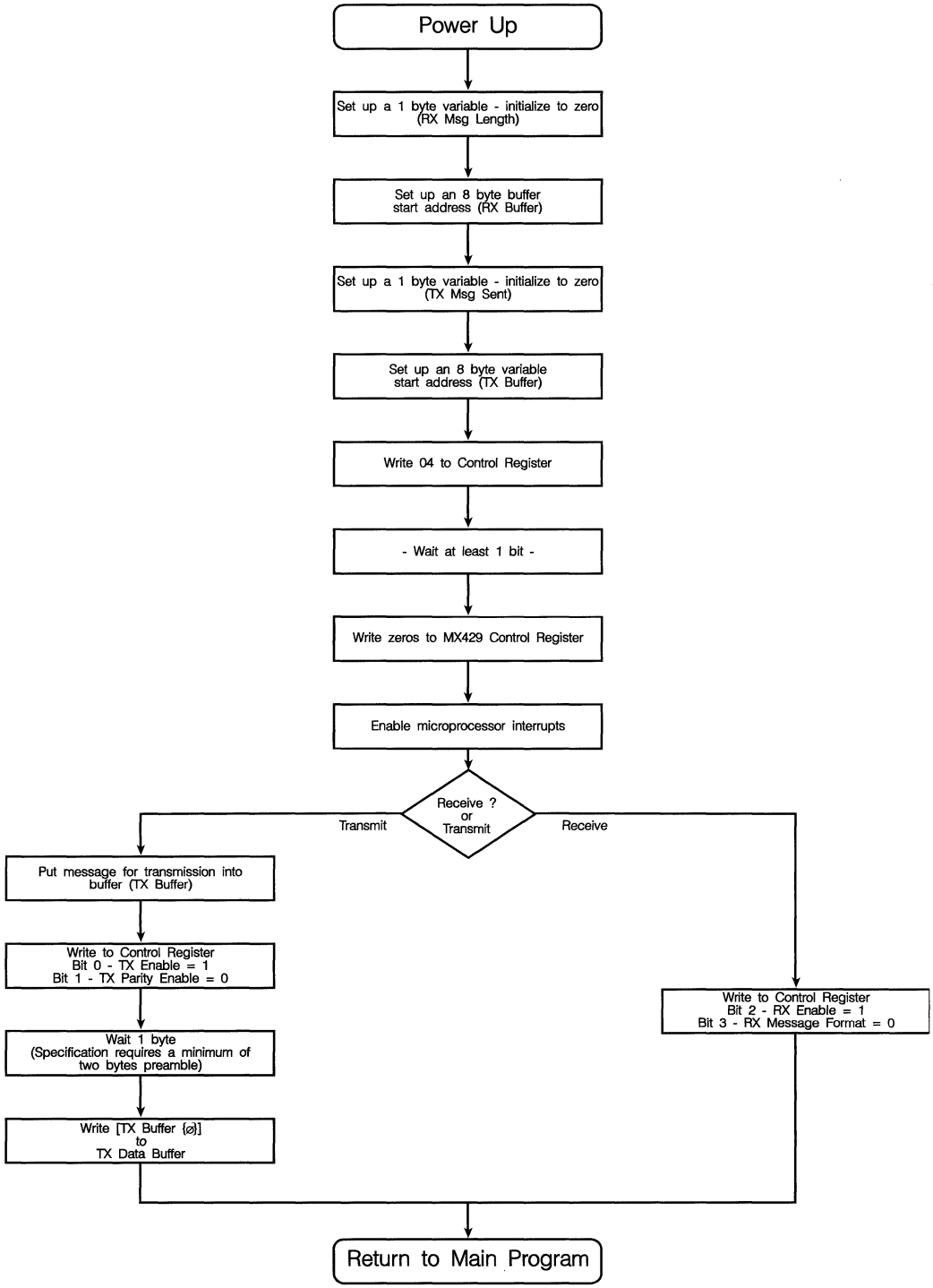


Figure 8 - Power-up Flow

Basic Software Interrupt Flow

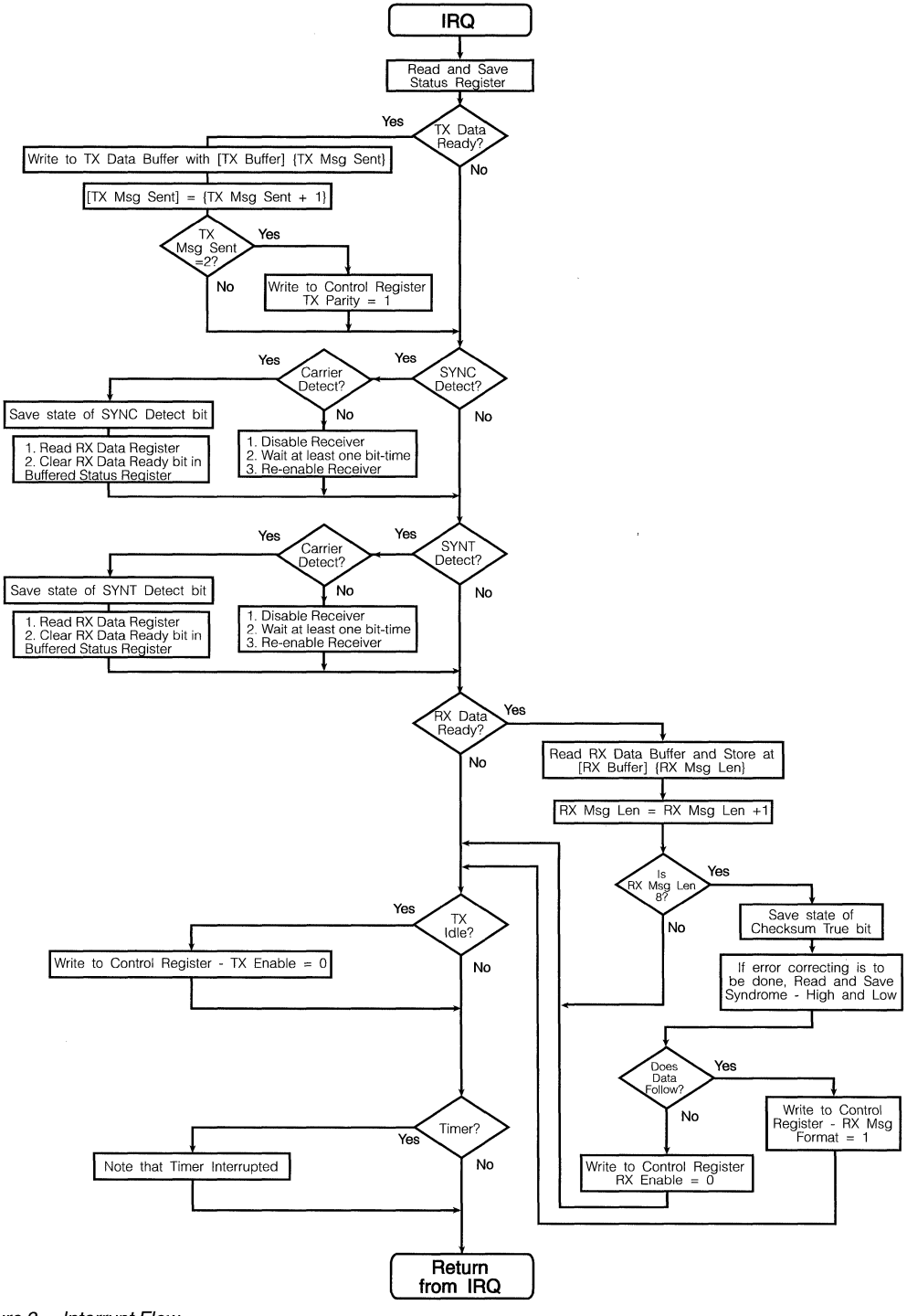


Figure 9 - Interrupt Flow

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 V to V_{DD} + 0.3 V
Sink/Source Current	
(supply pins)	±30mA
(other pins)	±20mA
Total Device Dissipation @ T_{AMB} = 25°C	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.

V_{DD}=5.0V

T_{AMB}=25°C

Xtal/Clock fo = 4.032 MHz

Audio Level 0dB ref. = 300 mVrms

1

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	-	5.5	V
Supply Current Ranges					
RX & TX Enabled		-	5.0		mA
RX Enabled, TX Disabled		-	5.0	-	mA
RX Disabled, TX Enabled		-	5.0	-	mA
RX & TX Disabled	10	-	1	-	mA
Dynamic Values					
Modem Internal Delay		-	1.5	-	ms
Interface Levels					
Output Logic "1" Source Current	2	-	-	120	µA
Output Logic "0" Sink Current	3	-	-	360	µA
Three State Output Leakage Current		-	-	4.0	µA
D_0 - D_7 Data In/Out	1				
Logic "1" Level		3.5	-	-	V
Logic "0" Level		-	-	1.5	V
A_1, A_0, A_2, STROBE, $\overline{IRQ}$	4				
Logic "1" Level		4.0	-	-	V
Logic "0" Level		-	-	1.0	V
Analog Impedances					
RX Input		100	-	-	kΩ
TX Output (Enabled)		-	10	-	kΩ
TX Output (Disabled)		-	5	-	MΩ
On-Chip Xtal Oscillator					
R_{IN}		10	-	-	MΩ
R_{OUT}	5	5.0	-	15	kΩ
Oscillator Gain		-	15	-	dB
Xtal Frequency		-	4.032		MHz
Timing (See Fig. 5)					
Chip Select Access Time (t_{ACS})		-	-	135	ns
Address Hold Time (t_{AH})		0	-	-	ns
Address Set-up Time (t_{AS})		0	-	-	ns
Data Hold Time (Write) - (t_{DHW})		85	-	-	ns
Data Set-up Time - (t_{DS})		0	-	-	ns
Output Hold Time (Read) - (t_{OHR})		15	-	105	ns
Strobe Time (Read) - (t_{STR})		140	-	-	ns
Strobe Time (Write) - (t_{STW})		50	-	-	ns

Characteristics	See Note	Min.	Typ.	Max.	Unit
Receiver					
Signal Input Levels	6	-9.0	-2.0	+10.5	dB
Bit Error Rate	7				
@ 12 dB Signal/Noise Ratio		-	7.0	-	10^{-4}
@ 20 dB Signal/Noise Ratio		-	1.0	-	10^{-8}
Synchronization @ 12 dB S/N Ratio	8				
Probability of Bit 16 being correct		-	99.5	-	%
Carrier Detect Response Time	8	-	13.0	-	ms
Transmitter					
Output Level		-	8.25	-	dB
Output Level Variation		-1.0	-	+1.0	dB
Output Distortion		-	3.0	5.0	%
3rd Harmonic Distortion		-	2.0	3.0	%
Logic "1" Frequency	9	-	1200	-	Hz
Logic "0" Frequency	9	-	1800	-	Hz
Isochronous Distortion					
1200-1800 Hz		-	25	40	µs
1800-1200 Hz		-	20	40	µs

Notes
1. With each data line loaded as C = 50 pf and R = 10 kΩ.
2. V_{OUT} = 4.6 V.
3. V_{OUT} = 0.4 V.
4. Sink/Source currents ≤ 0.1 mA.
5. Both Xtal and Xtal ÷ 4 Outputs.
6. With 50 dB S/N ratio.
7. See Figure 3, Bit Error Rate.
8. This response time is measured using a 10101010101...01 pattern input signal at a level of 230 mVrms (-2.3 dB) with no noise.
9. Dependent upon Xtal tolerance.
10. Powersave is only active when both RX and TX functions are disabled.

Checksum Generation and Checking

Generation - The checksum generator takes the 48 bits from the 6 bytes loaded into the TX Data Buffer and divides them modulo-2, by the generating polynomial:

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial 48 bits and the 15 bit remainder (with the last bit inverted).
The 16-bit word is used as the "checksum."

Checking - The checksum generator does two things:
It takes the first 63 bits of a received message, inverts bit 63, and divides them modulo-2, by the generating polynomial:

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

The 15 bits remaining in the polynomial divider are checked for all zero.

Second, it generates an EVEN parity bit from the first 63 bits of a received message and compares this bit with the received parity bit (bit 64). If the 15 bits in the polynomial divider are all zero, and the two parity bits are equal, then the RX Checksum True bit (SR D_1) is set.

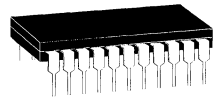
MSK MODEM

FEATURES

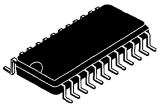
- 1200 Baud MSK Modem
- Meets Cellular & Trunked Radio Specifications
- Full-Duplex 1200 Baud
- On-Chip RX and TX Bandpass Filters
- Clock Recovery and Carrier Detect
- Pin Selectable Xtal/Clock Frequencies

APPLICATIONS

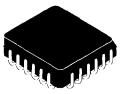
- Mobile & Cellular Radio Data Signaling
- Personal Radio
- Portable Data Terminals
- General Purpose Applications



MX439J: 22 pin CDIP
MX439P: 22 pin PDIP



MX439DW
24-pin SOIC



MX439LH
24-pin PLCC

DESCRIPTION

The MX439 is a single-chip CMOS LSI circuit which operates as a 1200 baud MSK modem. The mark and space frequencies are 1200Hz and 1800Hz phase continuous, and the frequency transitions occur at the zero crossing point. The transmitter and receiver will work independently, thus providing full-duplex operation at 1200 baud. The baud rate, transmit mark and space frequencies, and the TX and RX synchronization are all derived from a highly stable Xtal oscillator. The on-chip oscillator is capable of working at one of two input frequencies: 1.008MHz or 4.032MHz external Xtal/clock input. Frequency is pin-selectable with the "Clock Rate" logic input. The device includes circuitry for carrier detect and facility for the RX clock recovery. An on-board switched capacitor 900Hz - 2100Hz bandpass filter provides optimum carrier filtering. The use of switched capacitor analog filters and digital signal processing results in excellent dynamic performance with few external components; the CMOS process and current-saving techniques offer low standby supply current for portable battery-powered applications.

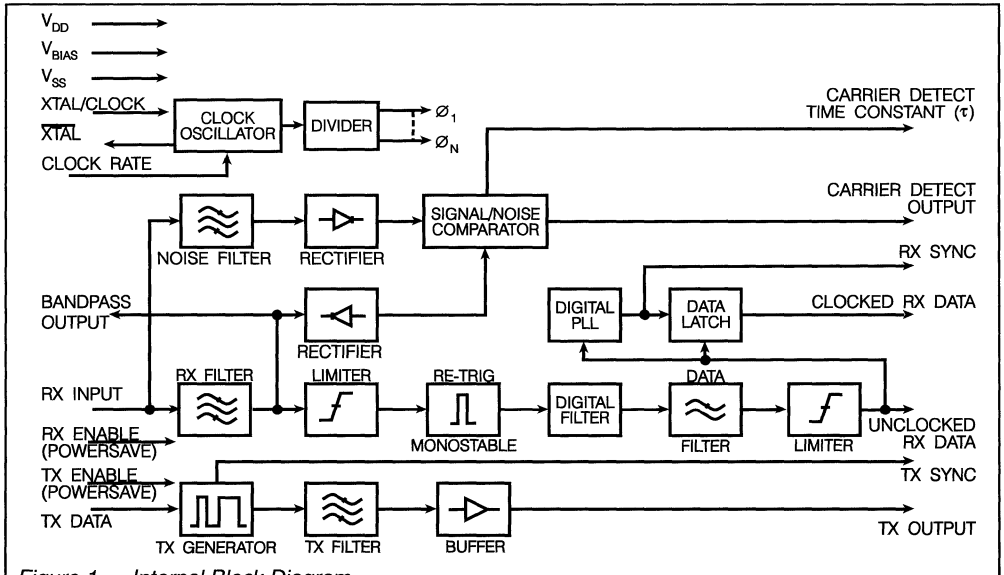


Figure 1 - Internal Block Diagram

PIN FUNCTION TABLE

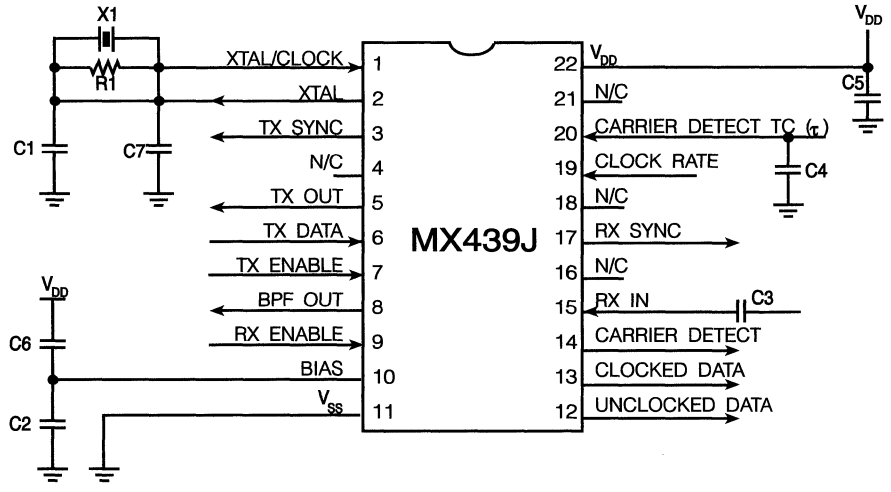
Pin			Function
DW	J,P	LH	
1	1	1	Xtal/Clock: The input to an on-chip inverter for use with either a 1.008MHz or a 4.032MHz Xtal. Alternatively, an external clock may be used. Xtal frequency is selectable on the "Clock Rate" input pin.
2	2	2	$\overline{\text{Xtal}}$: Output of the on-chip inverter. (See Figure 2.)
3	3	3	TX Sync O/P: MSK signal centered at a DC level of V_{BIAS} - 0.7V. (See Figure 5.)
5	5	5	TX Signal O/P: With the transmitter disabled, this pin is set to a high impedance state. When the transmitter is enabled, this pin outputs the 1200/1800Hz MSK signal centered at a DC level of V_{BIAS} - 0.7 V. (See Figure 5.)
7	6	7	TX Data I/P: Serial logic data to be transmitted is input to this pin and synchronized by the "TX Sync O/P." (See Figure 5.)
8	7	8	$\overline{\text{TX Enable}}$: A logic "1" applied to this input will put the transmitter into powersave while forcing "TX Sync O/P" to a logic "1" and "TX Signal O/P" to a high impedance state. A logic "0" will enable the transmitter (See Figure 5). This pin is internally pulled to V_{DD}.
9	8	9	Bandpass O/P: This is the output of the RX 900Hz-2100Hz bandpass filter. The output impedance of this pin is typically 10kΩ and may require buffering prior to use.
10	9	10	RX Enable: This is the control of the RX function. The state of other outputs is given below:
11	10	11	Bias: Provides bias internally and should be decoupled externally to V_{ss} by capacitor (C_2). (See Fig. 2.)
12	11	12	V_{ss}: Negative supply rail (GND).
13	12	13	Unclocked Data O/P: This pin outputs recovered asynchronous serial data from the receiver.
14	13	14	Clocked Data O/P: This pin outputs recovered synchronous serial data from the receiver and is internally latched out by a recovered clock appearing on the "RX Sync O/P" pin. (See Figure 6.)
15	14	15	Carrier Detect O/P: This pin will output a logic "1" when an MSK signal is being received.
16	15	16	RX Signal I/P: This is the MSK signal input for the receiver. It should be decoupled using capacitor C_3.
18	17	18	RX Sync O/P: This is a flywheel 1200Hz squarewave output which, upon presentation of the MSK data signal, is synchronized internally to the incoming data. (See Figure 6.)

RX Enable	RX Function	Clock Data O/P	Carrier Detect	RX Sync Out
"1"	Enabled	Enabled	Enabled	Enabled
"0"	Powersave	"0"	"0"	"1" or "0"

When both TX and RX functions are disabled, the bias voltage is switched internally to V_{SS} and Bias pin output impedance is approximately 12.5kΩ. When the Bias pin is decoupled by a 1.0μF capacitor (C2) the MX439 may require up to 25ms to establish correct operation after enabling the RX function. This period may be decreased by either reducing the value of C2, lowering the Bias pin impedance externally, or adopting a different powersaving strategy (such as using C2 and C5 and supplying V_{DD} via a series switch). This pin is internally pulled to V_{DD}.

Pin			Function
DW	J,P	LH	
21	19	21	Clock Rate: This logic input selects and allows the use of either a 1.008MHz or 4.032MHz Xtal/clock input to the on-chip inverter. Logic "1" = 4.032MHz; logic "0" = 1.008MHz. This input has an internal pulldown resistor (1.008MHz).
22	20	22	Carrier Detect Time Constant (τ): This input forms part of the carrier detect integration function. The value of C_4 connected to this pin will affect the carrier detect response time and hence noise performance. (See Figure 2, Note 3.)
24	22	24	V_{DD}: Positive supply rail. A single 5 volt supply is required.
4,6,17 19,20 23	4,16, 18,21	4,6,17 19,20, 23	No Connection.

Note: Output Loading. Large capacitive loads could cause the output pins of this device to oscillate. If capacitive loads in excess of 200pF are unavoidable, a resistor of (typically) 100Ω put in series with the load should minimize this effect.



Component References	
Component	Value
R1	1M
C1	33p
C2	1.0µ
C3	0.1µ
C4	0.1µ
C5	1.0µ
C6	1.0µ
C7	33p
X1	1.008MHz or 4.032 MHz

Tolerances: R = ±10%
C = ±20%

Notes:

1. Bias may be decoupled to V_{SS} and V_{DD} using C2 and C6 when input signals are referenced to the bias pin. For input signals referenced to V_{SS}, decouple Bias to V_{SS} using C2 only.

2. Use C5 when input signals are referenced to V_{SS} to decouple V_{DD}.

3. The value of C4 determines the carrier detect time constant. A long time constant results in improved noise immunity but increased response time. C4 may be varied to trade-off response time for noise immunity.

4. The value of C7 reduces XTAL voltage overshoot. Refer to MX-COM's Crystal Oscillator Application Note (see Appendix).

5. X1 can be either a 1.008 MHz or 4.032 MHz crystal, depending on the Clock Rate setting.

Figure 2 - External Component Connections

DIAGRAMS

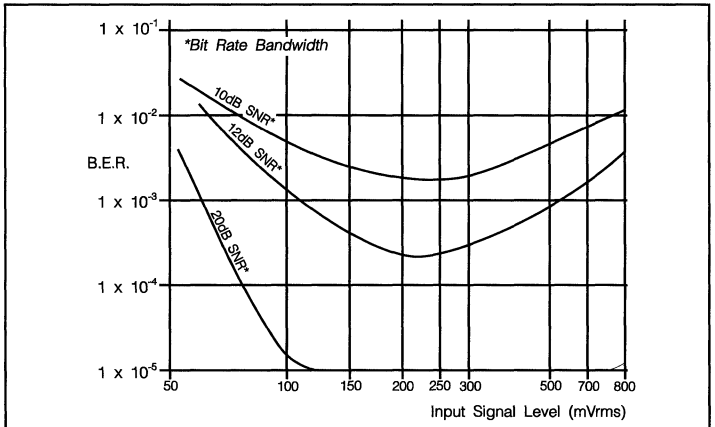


Figure 3 - Typical Variation of "B.E.R." with Input Signal Level

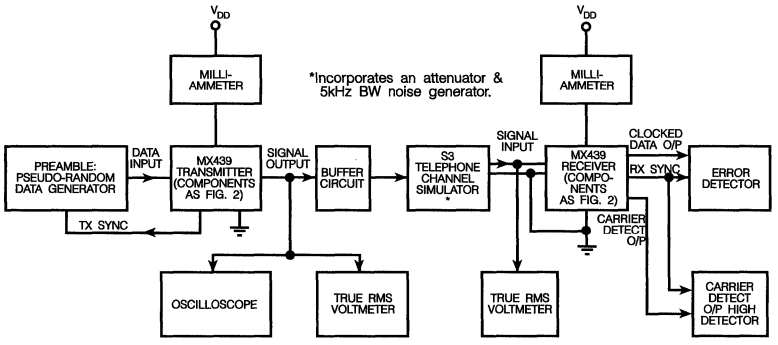
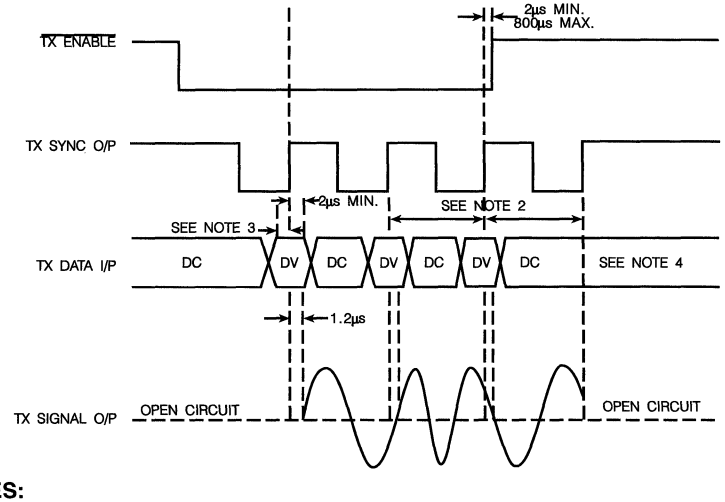


Figure 4 - MX439 Test Set-up



NOTES:

1. All timings are related to the TX SYNC OUTPUT.
2. 0.833ms for 1.008MHz or 4.032MHz Xtal.
3. 2µs min. + crystal tolerance.
4. DC = Don't Care. DV = Data Valid.

Figure 5 - Transmitter Timing Diagram

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 V to V_{DD} + 0.3 V
Sink/Source Current (Total)	20mA
Total Device Dissipation @ T_{AMB} = 25°C	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All charactistics are measured using the standard test circuit (Figure 4) with the following test parameters and is valid for all tests unless otherwise stated:

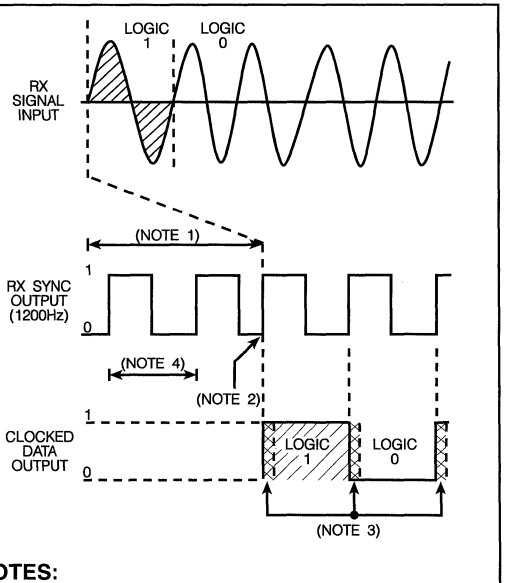
V_{DD} = +5V
T_{AMB} = 25°C
Xtal (X1) Frequency: 1.008MHz
0dB reference = 300 mVrms
Noise (band limited 5kHz gaussian white noise)
SNR ratio measured in bit rate bandwidth (1200Hz)

1

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Volts		4.5	5.0	5.5	V
Supply Current:					
RX Enabled, TX Disabled		-	3.6	-	mA
RX Enabled, TX Enabled		-	4.5	-	mA
RX Disabled, TX Disabled		-	650	-	µA
Logic "1" level		80%V_{DD}	-	-	V
Logic "0" level	-	-	-	20%V_{DD}	V
Digital Output Impedance		-	4	-	kΩ
Analog and Digital Input Impedance		100	-	-	kΩ
TX Output Impedance		-	10	-	kΩ
On-Chip Crystal Oscillator:					
R_{in}		10	-	-	MΩ
R_{out}		5	-	15	kΩ
Inverter Gain		10	-	20	dB
Gain Bandwidth Product		3 x 10^6	-	-	
Crystal Frequency	1,9	-	1.008	-	MHz
Crystal Frequency	1,10	-	4.032	-	MHz
Dynamic Values					
Receiver:					
Signal Input: Dynamic Range (50dB SNR)	2,3	100	230	1000	mVrms
Bit Error Rate:					
12dB SNR	3	-	7.0	-	10^{-4}
20dB SNR	3	-	1.0	-	10^{-8}
Receiver Synchronization 12dB SNR:	6				
Probability of Bit 8 being correct			99	-	%
Probability of Bit 16 being correct			99.5	-	%
Carrier Detect	4				
Sensitivity	6,7	-	-	125	mVrms
Probability of Carrier Detect being high:					
12dB SNR after Bit 8	4,8	-	98	-	%
12dB SNR after Bit 16	4,8	-	99.5	-	%
0dB Noise (No Signal)	8	-	5	-	%

Characteristics	See Note	Min.	Typ.	Max.	Unit
Transmitter Output					
TX Output Level		-	775	-	mVrms
Output Level Variation 1200/1800Hz		0	-	±1.00	dB
Output Distortion		-	3	5	%
3rd Harmonic Distortion		-	2	3	%
Logic "1" Carrier Frequency	5	-	1200	-	Hz
Logic "0" Carrier Frequency	5	-	1800	-	Hz
Isochronous Distortion					
1200Hz - 1800Hz		-	25	40	µs
1800Hz - 1200Hz		-	20	40	µs

Notes:
1. Crystal frequency, type and tolerance depends on system requirements.
2. See Figure 3.
3. SNR (Bit Rate Bandwidth).
4. See Figure 2, Note 3.
5. Depending on crystal tolerance.
6. 10101010101... pattern.
7. Measured with 100 mVrms signal (No noise).
8. 0dB level for CD probability measurements is 230mVrms.
9. Clock rate pin at logic "0."
10. Clock rate pin at logic "1."



NOTES:
1. Internal delay typically 1.5ms.
2. From freely running to Sync in 8 data bits (See spec).
3. Undetermined state: 2µs max.
4. Min 800µs, Max. 865µs.

Figure 6 - Receiver Timing Diagram

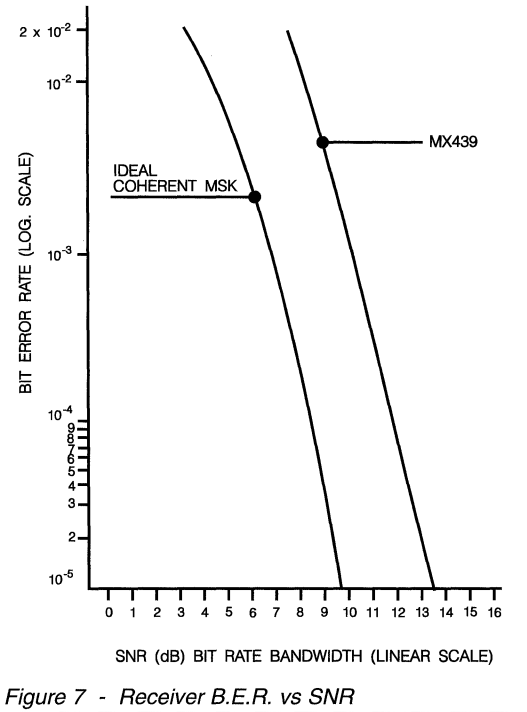


Figure 7 - Receiver B.E.R. vs SNR

MX•COM, INC.

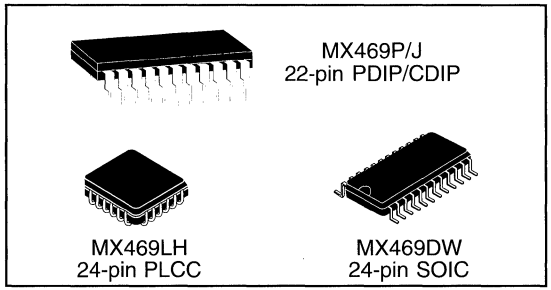
MX469

Preliminary Information

1200 AND 2400 BPS MSK MODEM

Features

- **Selectable Data Rates:*1200 and 2400 bps***
- **Full-Duplex MSK**
- **RX and TX Bandpass Filters**
- **Clock Recovery and Carrier Detect Cababilities**
- **Pin Selected Xtal/Clock Inputs**
  1.008MHz or 4.032MHz
- **Radio and General Applications**
  - **Data-Over-Radio • PMR/Cellular Signaling**
  - **Portable Data Terminals**
  - **Personal/Cordless Telephone**



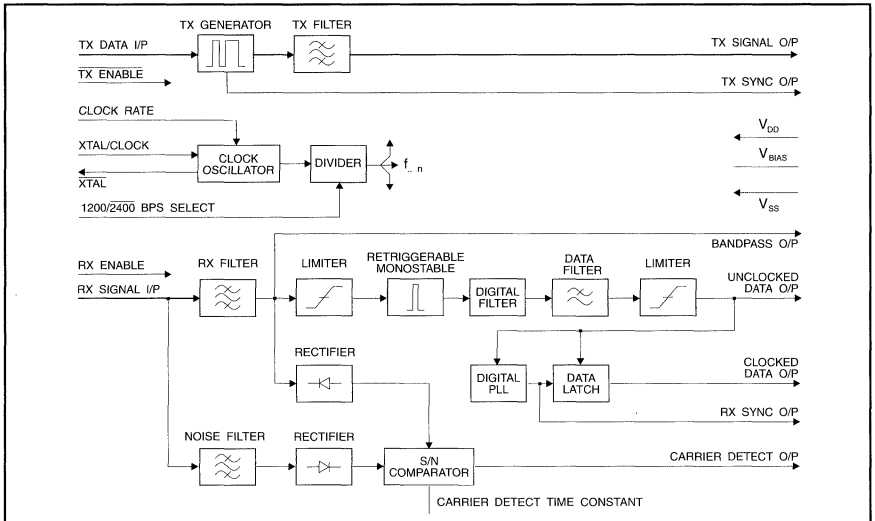


Figure 1 - Functional Block Diagram

Description

The MX469 is a full-duplex pin-selectable 1200 or 2400 bps Minimum Shift Key (MSK) Modem for FM radio links. The mark and space frequencies are 1200/1800 and 1200/2400Hz respectively. Tone frequencies are phase continuous; transitions occur at the zero crossing point.

Use of a common Xtal oscillator with a choice of two clock frequencies (1.008MHz or 4.032MHz) provides data-rate, transmit frequencies and RX/TX synchronization. The transmitter and receiver operate entirely independently including individual section powersave functions.

The MX469 includes on-chip circuitry for Carrier Detect and RX Clock Recovery, both of which are made available at output pins.

RX, TX and Carrier Detect paths each contain a bandpass filter to make sure you get the best quality signal in the Modem and TX modulation circuitry.

The MX469 demonstrates a high sensitivity and good bit-error-rate even under adverse signal conditions.

The carrier detect time constant is set by an external capacitor, whose value should be arranged as required to further enhance this product's performance in high-noise environments.

This low-power device requires few external components and is available in SOIC (small outline), CDIP, PDIP and PLCC packages.

Pin Function Table

Pin Number MX469 DW	J/P	LH	Function
1	1	1	**Xtal/Clock:** The input to the on-chip inverter, for use with either a 1.008MHz or a 4.032MHz Xtal or external clock. Clock frequency selection is by the "Clock Rate" input pin. The selection of this frequency will affect the operational Data Rate of this device. Refer to 1200/2400 BPS Selection information on the next page. Operation of any MX•COM IC without a Xtal or clock input may cause device damage. To minimize damage in the event of a Xtal/drive failure, it is recommended that a current limiting device (resistor or fast-reaction fuse) in installed on the power supply (V_{DD}).
2	2	2	**$\overline{\text{Xtal}}$:** Output of the on-chip inverter.
3	3	3	**TX Sync O/P:** A squarewave, produced on-chip, to synchronize the input of logic data and transmission of the MSK signal (See Figure 4).
5	5	5	**TX Signal O/P:** When the transmitter is enabled, this pin outputs the (140-step pseudo sinewave) MSK signal (See Figure 4). With the transmitter disabled, this output is set to a high-impedance state.
7	6	7	**TX Data I/P:** Serial logic data to be transmitted is input to this pin.
8	7	8	**$\overline{\text{TX Enable}}$:** A logic '0' will enable the transmitter (See Figure 4). A logic '1' at this input will put the transmitter into powersave while forcing "TX Sync Out" to a logic '1' and "TX Signal Out" to a high-impedance state. This pin is internally pulled to V_{DD}.
9	8	9	**Bandpass O/P:** The output of the RX Bandpass Filter. This output impedance is typically 10kΩ and may require buffering prior to use.
10	9	10	**RX Enable :** The control of the RX function. The control of other outputs is given below.

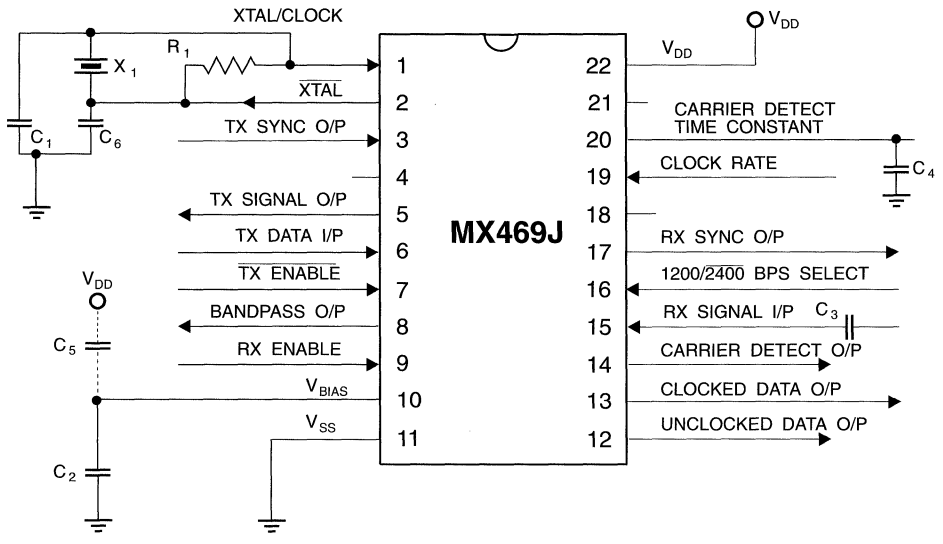
RX Enable	=	RX Function	Clock Data O/P	Carrier Detect	Rx Sync Out
"1"	=	Enabled	Enabled	Enabled	Enabled
"0"	=	Powersave	"0"	"0"	"1" or "0"

11	10	11	**V_{BIAS}:** The output of the on-chip analog bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to V_{SS} by a capacitor (C_2). See Figure 2 and RX Enable notes. This bias voltage is maintained under all powersave conditions.
12	11	12	**V_{SS}:** Negative supply rail (GND).

Pin Number			Function
	MX469		
DW	J/P	LH	
13	12	13	**Unclocked Data O/P:** The recovered asynchronous serial data output from the receiver.
14	13	14	**Clocked Data O/P:** The recovered synchronous serial data output from the receiver. Data is latched out by the recovered clock, available at the "RX Sync O/P", (See Fig. 5).
15	14	15	**Carrier Detect O/P:** When an MSK signal is being received this output is a logic '1'.
16	15	16	**RX Signal I/P:** The MSK signal input for the receiver. This input should be coupled via a capacitor, C_3.
18	17	18	**RX Sync O/P:** A flywheel squarewave output. This clock will synchronize to incoming RX MSK data (See Figure 5).
19	16	19	**1200/2400 BPS Select:** A logic '1' on this pin selects the 1200 bps option. Tone frequencies are: one cycle of 1200Hz represents a logic '1', one-and-a-half cycles of 1800Hz represents a logic '0'. A logic '0' on this pin selects the 2400 bps option. Tone frequencies are: one-half cycle of 1200Hz represents a logic '1', one cycle of 2400Hz represents a logic '0'. This pin has an internal 1MΩ pullup resistor. **Operational Data Rate Configurations** are illustrated in the table below.
20	18	20	Internally connected, leave open circuit.
21	19	21	**Clock Rate:** A logic input to select and allow the use of either a 1.008MHz or 4.032MHz Xtal/clock. Logic '1' = 4.032MHz, logic '0' = 1.008MHz. This input has an internal pulldown resistor (1.008MHz).
23	20	22	**Carrier Detect Time Constant :** Part of the carrier detect integration function. The value of C_4 connected to this pin will affect the carrier detect response time and hence noise performance (See Figure 2, Note 3).
24	22	24	V_{DD}: Positive supply. A single 5-volt supply is required.
4,6, 17, 22	4, 21	4, 6, 17, 23	No internal connection, do not use.

Xtal/Clock Frequency	1.008MHz		4.032MHz	
Clock Rate pin	0	0	1	1
1200/2400 Select pin	1	0	1	0
Data Rate (bps)	**1200**	**2400**	**1200**	**2400**

Application Information



Component	Value	Tolerance
R_1	1.0MΩ	±10%
C_1	33pF	±5%
C_2	1.0µF	±20%
C_3	0.1µF	±20%
C_4	0.1µF	±10%
C_5	1.0µF	±25%
C_6	33pF	±5%
X_1	1.008MHz or 4.032MHz	See 'Clock-Rate' Pin

Notes

1. V_{BIAS} may be decoupled to V_{SS} and V_{DD} using C_2 and C_5 when input signals are referenced to the V_{BIAS} pin. For input signals referenced to V_{SS}, decouple V_{BIAS} to V_{SS} using C_2 only.
2. The value of C_4 determines the Carrier Detect time constant. A long time constant results in improved noise immunity but increased response time. C_4 may be varied to trade-off response time for noise immunity.
3. C_6 reduces Xtal voltage overshoot. Refer to MX•COM Xtal Application Note (see Application section).

Figure 2 - External Components

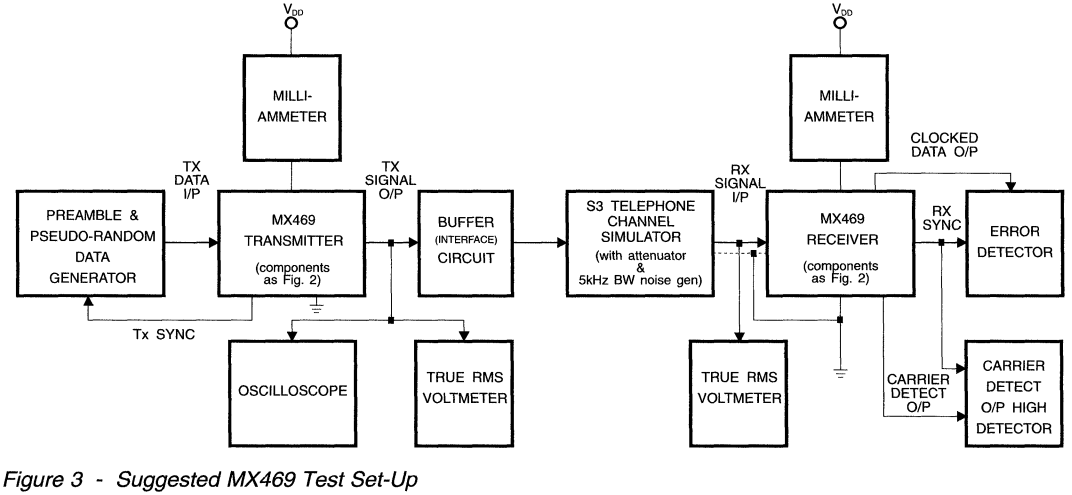


Figure 3 - Suggested MX469 Test Set-Up

Application Information .....

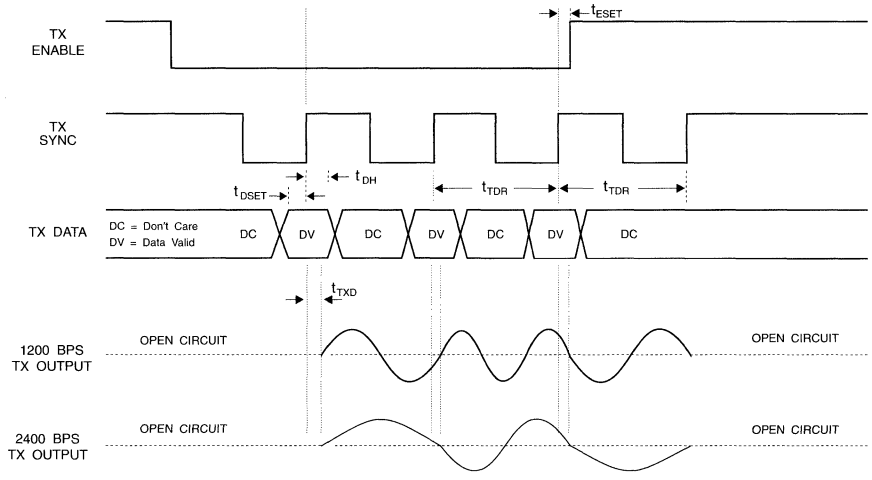


Figure 4 - Transmitter Timing

Characteristics		Note	Min.	Typ.	Max.	Unit
TX Delay, Signal to Disable Time	t_{ESET}		2.0	-	800	µs
Data Set-Up Time	t_{DSET}	1	2.0	-	-	µs
Data Hold Time	t_{DH}		2.0	-	-	µs
TX Delay to O/P Time	t_{TxD}		-	1.2	-	µs
TX Data Rate Period	t_{TDR}		-	833	-	µs
RX Data Rate Period	t_{RDR}		800	-	865	µs
Undetermined State			-	-	2.0	µs
Internal RX Delay	t_{ID}		-	1.5	-	ms

1. Consider the Xtal/Clock tolerance.
2. All TX timings are related to the TX Sync Output.

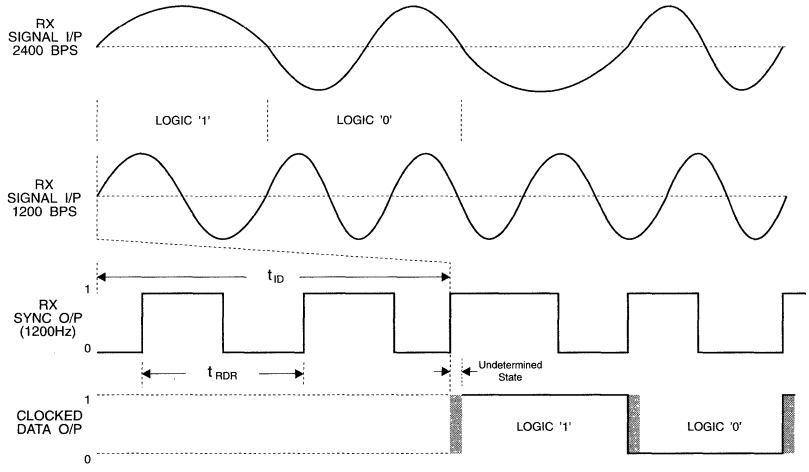


Figure 5 - RX Timing Diagram

Application Information .....

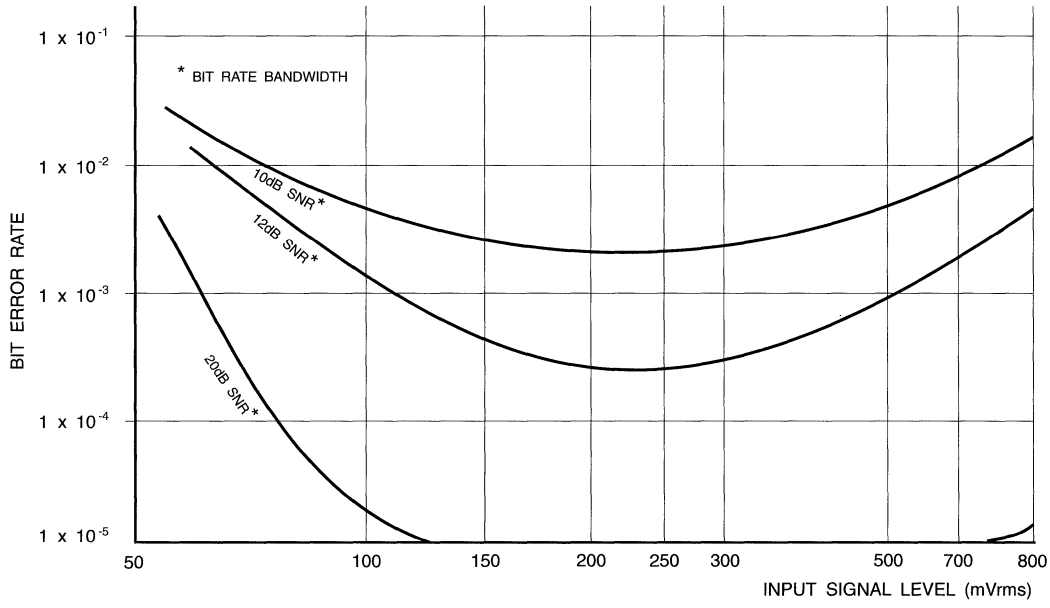


Figure 6 - Typical Variation of Bit Error Rate with Input Level

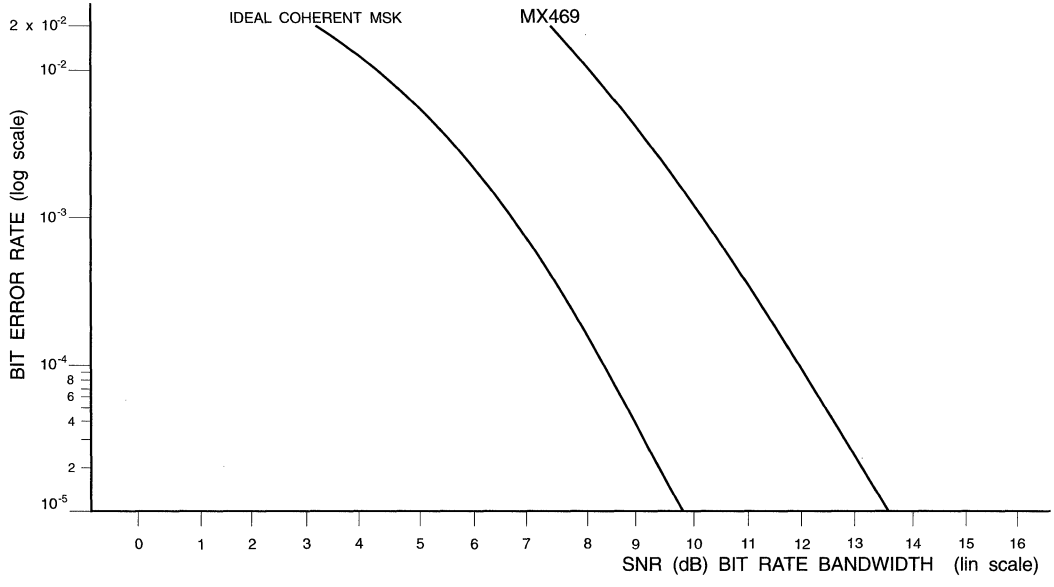


Figure 7 - RX Bit-Error-Rate vs Signal-to-Noise Ratio

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0V
Input Voltage at any pin (ref V_{SS}=0V)	-0.3 to (V_{DD}+ 0.3V)
Sink/Source Current (supply pins)	±30mA
(other pins)	±20mA
Total Device Dissipation (@ T_{AMB}=25°C)	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Audio Level 0dB ref = 300 mVrms

Xtal/Clock = 4.032 MHz

Signal-to-Noise Ratio measured in the Bit-Rate Bandwidth (1200 bps BRB = 1200 Hz
2400 bps BRB = 2400 Hz)

1

Characteristics		See Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Voltage			4.5	5.0	5.5	V
Supply Current	RX Enabled, TX Disabled		-	3.6	-	mA
	RX and TX Enabled		-	4.5	-	mA
	RX and TX Disabled		-	650	-	µA
Logic '1' Level		1	4.0	-	-	V
Logic '0' Level		1	-	-	1.0	V
Digital Output Impedance			-	4.0	-	kΩ
Analog and Digital Input Impedance			100	-	-	kΩ
TX Output Impedance			-	10.0	-	kΩ
On-Chip Xtal Oscillator						
	R_{IN}		10.0	-	-	MΩ
	R_{OUT}		-	10.0	-	kΩ
Inverter d.c. Voltage Gain			-	10.0	-	V/V
Gain Bandwidth Product			-	10.0	-	MHz
Xtal Frequency		2	-	1.008 or 4.032	-	MHz
Dynamic Values						
Receiver						
Signal Input Dynamic Range	SNR = 50dB	3, 4	100	230	1000	mVrms
Bit Error Rate	SNR = 12dB	4	-	7.0	-	10^{-4}
	SNR = 20dB	4	-	1.0	-	10^{-8}
Receiver Synchronization	**SNR =12dB**	7				
Probability of Bit 8 Being Correct			-	99	-	%
Probability of Bit 16 Being Correct			-	99.5	-	%
Carrier Detect		5				
Sensitivity		7, 8	-	-	150	mVrms
Probabilty of C.D. Being High						
After Bit 8	(1200 bps) SNR = 12dB	5, 9	-	98	-	%
After Bit 16	SNR = 12dB	5, 9	-	99.5	-	%
0dB Noise	No Signal	9	-	5	-	%

Characteristics		See Note	Min.	Typ.	Max.	Unit
Transmitter Output						
TX Output Level			-	775	-	mVrms
Output Level Variation						
1200/1800Hz or 1200/2400Hz			0	-	±1.0	dB
Output Distortion			-	3.0	5.0	%
3rd Harmonic Distortion			-	2.0	3.0	%
Logic '1' Carrier Frequency	1200 bps	6	-	1200	-	Hz
	2400 bps	6	-	1200	-	Hz
Logic '0' Carrier Frequency	1200 bps	6	-	1800	-	Hz
	2400 bps	6	-	2400	-	Hz
Isochronous Distortion						
1200Hz - 1800Hz/1200Hz - 2400Hz			-	25.0	40.0	µs
1800Hz - 1200Hz/2400Hz - 1200Hz			-	20.0	40.0	µs

Notes
1. With reference to V_{DD} = 5.0 volts.
2. Xtal frequency (ref. Clock Rate pin), type and tolerance depends upon system requirements.
3. See Figure 5 (variation of BER with Input Signal Level).
4. SNR = Signal-to-Noise in the Bit-Rate Bandwidth.
5. See Figure 2.
6. Dependent upon Xtal tolerance.
7. 10101010101 ...01 pattern.
8. Measured with a 150mVrms input signal (no noise).
9. Reference (0dB) level for C.D. probability measurements is 230mVrms.

Preliminary Information

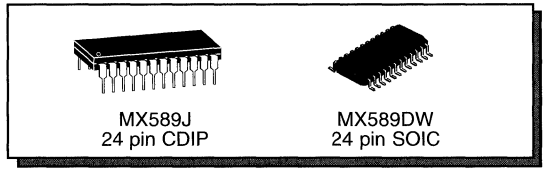
LOW VOLTAGE, HIGH SPEED GMSK MODEM
4 kbps to 40 kbps

FEATURES

- **MX•COM MX'D SIGNAL CMOS**
- **FULL- OR HALF-DUPLEX OPERATION**
- **DATA RATES FROM 4KBPS TO 40KBPS**
- **SELECTABLE BT: 0.3 OR 0.5**
- **LOW VOLTAGE OPERATION**
  3 TO 5.5 V
- **LOW POWER USAGE**
- **LOW PIN COUNT**
- **MEETS RCR STD-18 (JAPAN)**

APPLICATIONS

- **PORTABLE WIRELESS DATA**
  - **CELLULAR DIGITAL PACKET DATA (CDPD)**
  - **MOBITEX* MOBILE DATA SYSTEM**
- **DATA FOR GPS/DIFFERENTIAL GPS**
- **WIRELESS BAR CODE READERS**
- **WIRELESS LANS**



MX589J
24 pin CDIP

MX589DW
24 pin SOIC

Description

The MX589 is a single-chip synchronous Modem designed for wireless data applications. Employing Gaussian Minimum Shift Keying (GMSK) baseband modulation, the MX589 features a wide range of available data rates: 4,000 to 40,000 bits per second.

The data rate and choice of BT (0.3 or 0.5) are pin-programmable to provide for different system requirements.

The TX and RX digital data interfaces are bit serial, synchronized to TX and RX data clocks generated by the modem. Separate TX and RX Powersave inputs allow full or half-duplex operation. RX input levels can be set by a suitable a.c. and d.c. level adjusting circuit built with external components around an on-chip RX input amplifier.

Acquisition, lock and hold of RX data signals is made easier and faster by the use of RX Control Inputs to clamp, detect and/or hold input data levels and can be set by the µProcessor as required.

The RX S/N output gives an indication of the quality of the received signal.

The MX589 features a mixed signal CMOS process that offers considerably lower current drain than DSP technology. For data rates up to 20kbps, drain is typically 1.5mA at 3V, and for data rates up to 40kbps at 5V, it is typically 4.0mA.

The MX589 is available in 24-pin SOIC and CDIP packages.

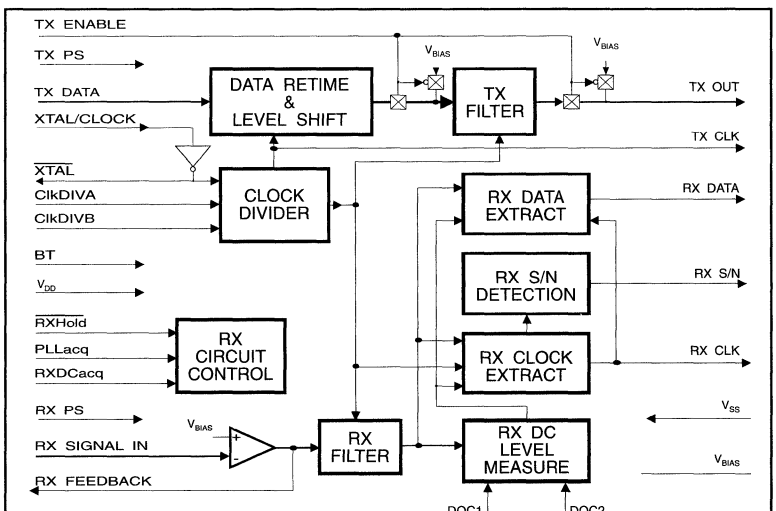


Figure 1 - Functional Block Diagram

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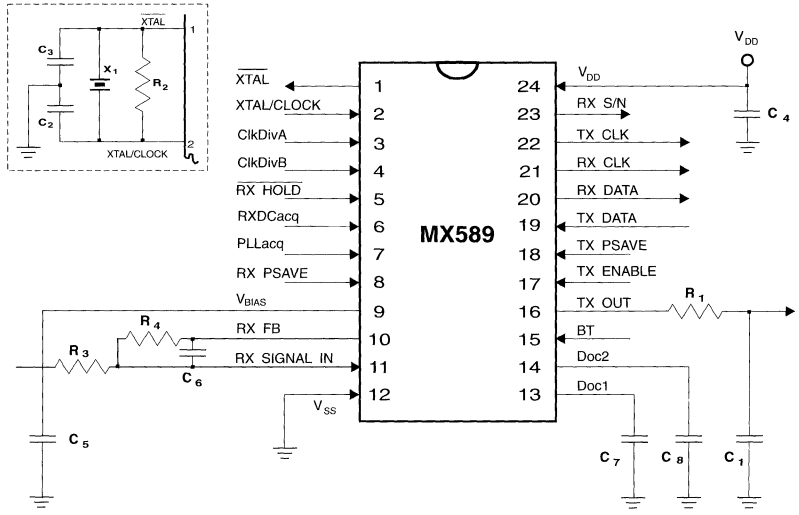
Pin	Function
1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator.
2	**Xtal/Clock:** The input to the on-chip Xtal oscillator. A Xtal, or externally derived clock (f_{XTAL}) pulse input should be connected here. If an externally generated clock is to be used, it should be connected to this pin and the "$\overline{\text{Xtal}}$" pin left unconnected. Note that operation of the MX589 without a suitable Xtal or clock input may cause device damage.
3 4	**ClkDivA:** These two logic level inputs control the internal clock divider and hence the transmit **ClkDivB:** and receive data rate. See Table 1.
5	**$\overline{\text{RX Hold}}$:** A logic "0" applied to this input will 'freeze' the Clock Extraction and Level Measurement circuits unless they are in 'acquire' mode.
6	**RXDCacq:** A logic "1" applied to this input will set the RX Level Measurement circuitry to the 'acquire' mode.
7	**PLLacq:** A logic "1" applied to this input will set the RX Clock Extraction circuitry to 'acquire' mode (see Table 2).
8	**RX PSAVE:** A logic "1" applied to this input will powersave all receive circuits except for RX CLK output (which will continue at the set bit-rate) and cause the RX Data and RX S/N outputs to go to a logic "0".
9	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$, this pin must be decoupled to V_{SS} by a capacitor mounted close to the pin.
10	**RX FB:** The output of the RX Input Amplifier/The input to the RX Filter.
11	**RX Signal In:** The input to RX input amplifier.
12	**V_{SS}:** Negative supply rail. Signal ground.
13 14	**Doc1:** Connections to the RX Level Measurement Circuitry. A capacitor should be **Doc2:** connected from each pin to V_{SS}.
15	**BT:** A logic level to select the modem BT (the ratio of the TX Filter's -3dB frequency to the Bit-Rate). A logic "1" sets the modem to a BT of 0.5, a logic "0" to a BT of 0.3.
16	**TX Out:** The TX signal output from the MX589 GMSK Modem.
17	**TX Enable:** A logic "1" applied to this input enables the transmit data path through the TX Filter to the TX Out pin. A logic "0" will put the TX Out pin to V_{BIAS} via a high impedance.
18	**TX PSAVE:** A logic "1" applied to this input will powersave all transmit circuits except for the TX Clock.
19	**TX Data:** The logic level input for the data to be transmitted. This data should be synchronous with TX CLK.
20	**RX Data:** A logic level output carrying the received data, synchronous with RX CLK.
21	**RX CLK:** A logic level clock output at the received data bit-rate.
22	**TX CLK:** A logic level clock output at the transmit-data rate.
23	**RX S/N:** A logic level output which may be used as an indication of the quality of the received signal.
24	**V_{DD}:** Positive supply rail. A single +5 volt power supply is required. Levels and voltages within this modem are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the pin.



Component	Value	Tolerance	Component	Value	Tolerance
R_1	Note 1	±5%	C_3	Note 5	
R_2	1.0MΩ	±10%	C_4	0.1µF	±20%
R_3	Note 2	±10%	C_5	1.0µF	±20%
R_4	100kΩ	±10%	C_6	22.0pF	±20%
C_1	Note 1	±10%	C_7	Note 4	
C_2	Note 5		C_8	Note 4	
			X_1	Note 3	

Figure 2 - External Components

Notes

1. The RC network formed by R_1 and C_1 is required between the TX Out pin and the input to the modulator. This network, which can form part of any d.c. level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to the capacitor C_1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.

   The component values should be chosen so that the product of the resistance (Ohms) and the capacitance (Farads) is:

   BT of 0.3 = 0.34/bit rate (bits/second)
   BT of 0.5 = 0.22/bit rate (bits/second)
   with suitable values for common bit rates being:

		R_1	C_1
8000 bps	BT = 0.3	91.0kΩ	470pF
4800 bps	BT = 0.5	100kΩ	470pF
9600 bps	BT = 0.5	47.0kΩ	470pF
19,200 bps	BT = 0.5	22.0kΩ	470pF
32,000 bps	BT = 0.3	47.0kΩ	220pF
32,000 bps	BT = 0.5	47.0kΩ	150pF
38,400 bps	BT = 0.3	47.0kΩ	180pF
38,400 bps	BT = 0.5	47.0kΩ	120pF

   Note that in all cases the value of R_1 should not be less than 20.0 kΩ, and that the calculated value of C_1 includes calculated parasitic capacitances.

2. R_3, R_4 and C_6 form the gain components for the RX Input signal. R_3 should be chosen as required by the signal input level.

3. The MX589 can operate correctly with Xtal/Clock frequencies between 1.0MHz and 6.5MHz (see Table 1). Operation of this device without a Xtal or Clock input may cause device damage.

4. C_7 and C_8 should both be 15.0nF for a data rate of 8kbps, and inversely proportional to the data rate for other data rates, e.g. 30.0nF at 4kbps, 3.0nF at 40kbps.

5. The values chosen for C_2 and C_3, including strays, should be suitable for the frequency of X1 and the supply voltage:

   5V $C_2 = C_3 = 33$pF at 1MHz falling to 18pF at 6.5MHz
   3V $C_2 = C_3 = 33$pF at 1MHz falling to 18pF at 5MHz
   The ESR of X1 should be less than 2kΩ at 1 MHz falling to 150Ω at the maximum frequency.

Application Information

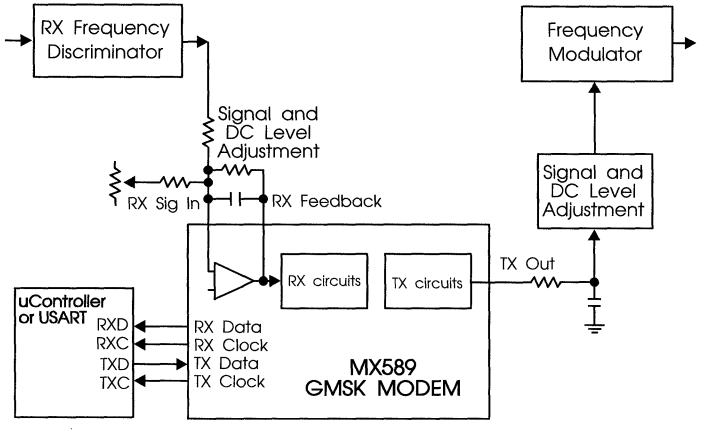


Figure 3 - External Signal Paths

Clock Oscillator and Dividers

The TX and (nominal) RX data rates are determined by division of the frequency present at the Xtal pin, which may be generated by the on-chip Xtal oscillator or derived from an external source. Any Xtal/clock frequency in the range 1.0 to 5.0 MHz for V_{DD}=3.0V, or 1.0 to 6.5 MHz for V_{DD}=5.0V may be used, depending on the desired data rate.

The division ratio is controlled by the logic level inputs on ClkDivA/B (pins 3 & 4), and is shown in the table below - together with an indication of how various 'standard' data rates may be derived from common µP Xtal frequencies.

$$\text{Data Rate} = \frac{\text{Xtal/clock Frequency}}{\text{Division Ratio (Clk DivA/B)}}$$

Pin 3	Pin 4	Division Ratio	Xtal/Clock Frequency (MHz)			
			4.096	4.9152	2.048	2.4576
0	0	128	32kbps	38.4kbps	16 kbps	19.2 kbps
0	1	256	16 kbps	19.2 kbps	8 kbps	9.6 kbps
1	0	512	8 kbps	9.6 kbps	4 kbps	4.8 kbps
1	1	1024	4 kbps	4.8 kbps	-	-

Table 1 - Xtal/Clock Frequencies and Corresponding Data Rates

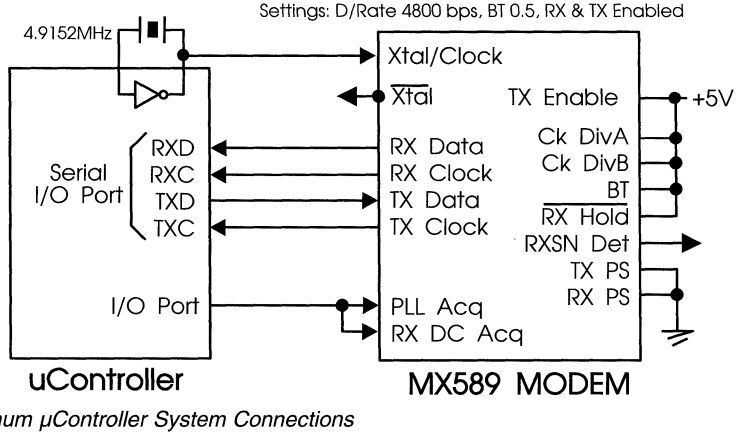


Figure 4 - Minimum µController System Connections

Application Information .....

RX Clock Extraction

The 'RX Clock Extraction' circuit is based on a zero crossing tracking loop which uses a multimode or multiresolution digital PLL. The lowest timing resolution option (Acquire mode) allows for fast initial phase acquisition. At most 8 zero crossings are required for initial acquisition. The loop can be programmed to operate in this mode using the $\overline{\text{RX Hold}}$ and the PLLacq pins (see Table 2).

The highest timing resolution, which is 1/64 bit-period, is obtained when the PLL is in its track mode. This mode of operation yields the least amount of phase jitter, which is desirable to limit the associated BER performance degradation. The loop can be set up to operate in this mode as shown in Table 2.

The loop also has a medium resolution (i.e. medium bandwidth) which is activated only when the MX589 controls are such that the PLL is switching from its acquire to its track mode. In such cases the medium setting is used automatically for a limited time (30 bits) after which the loop goes into its track mode. The medium bandwidth setting offers a compromise between fast acquisition and low jitter requirements.

The PLL can also be placed in a HOLD mode, where the RX Clock phase corrections are completely stopped. This mode of operation can be selected as shown in Table 2.

RX DC Level Measurement

The MX589 provides three user-programmable modes of operation for DC level measurement:

1) **Fast Peak Detect** - the detectors rapidly capture the positive and negative going signal peaks (more susceptible to noise).
2) **Averaging Peak Detect** - gives a slower but more accurate measurement of the signal peak amplitudes.
3) **Hold** - the outputs of the voltage detectors remain essentially at the last reading.

A fourth **"Clamp"** mode operates for one bit-time after a LO to HI transition of the RXDCacq input.

These modes of operation can be selected, one at a time, by applying the appropriate logic levels to the $\overline{\text{RX Hold}}$ and RXDCacq inputs (see Table 2).

RX Data Extraction

The 'RX Data Extraction' circuit decides whether each received bit is a "1" or "0" by sampling the received signal, after filtering, and comparing the sample values to an adaptive threshold derived from the 'Level Measuring' circuit. This threshold is adapted from bit to bit to compensate for intersymbol interference caused by the bandlimiting of the overall transmission path and the Gaussian premodulation filter.

Extracted data is output from the 'RX Data' pin, and should be sampled externally on the rising edge of the 'RX CLK.'

RX Data Formats

The receive section of the MX589 works best with data which has a reasonably 'random' structure --the data should contain approximately the same number of 'ones' as 'zeroes' with no long sequences (>100 bits) of consecutive 'ones' or 'zeroes'. Also, long sequences (>100 bits) of '10101010 ...' patterns should be avoided.

For this reason, it is recommended that data is made random in some manner before transmission, for example by 'exclusive-ORing' it with the output of a binary pseudo-random pattern generator.

Where data is transmitted in bursts, each burst should be preceded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble for BT=0.3 should be at least 16 bits long, and should preferably consist of alternating pairs of '1's and '0's i.e. '110011001100 .....'; the eye of pattern '10101010....' has the most gradual slope and will yield poor peak levels for the RX circuits. For BT=0.5 the eye pattern of '10101010...' has reduced intersymbol interference and may be used as the preamble (DC Acq pin should be held high during preamble). See Fig. 10.

RX S/N Detection

The 'RX S/N Detector' system classifies the incoming zero-crossings as GOOD or BAD depending upon the time when each crossing actually occurs with respect to its expected time as determined by the Clock Extraction PLL. This information is then processed to provide a logic level output at the 'RX S/N' pin. A high level indicates a series of GOOD crossings; a low level indicates a BAD crossing.

By averaging this output it is possible to derive a measure of the Signal-to-Noise-Ratio and hence the Bit-Error-Rate of the received signal (see Fig. 5).

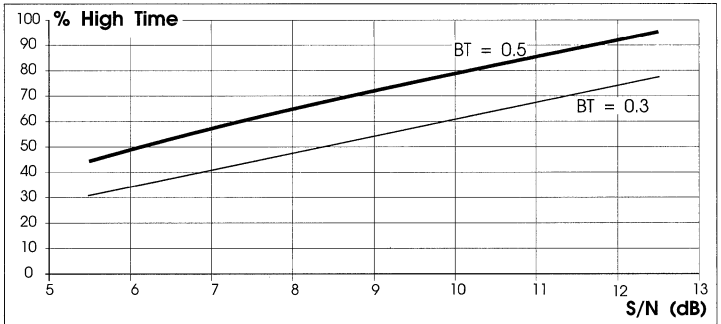


Figure 5 - Typical Rx S/N Output 'High-Time' (%) vs Input S/N

Application Information .....

RX Signal Path Description

The function of the RX circuitry is to:

1. Set the incoming signal to a usable level.
2. Clean the signal by filtering.
3. Provide DC level thresholds for clock and data extraction.
4. Provide clock timing information for data extraction and external circuits.
5. Provide RX data in a binary form.
6. Assess signal quality and provide Signal-to-Noise information.

The output of the radio receiver's Frequency Discriminator should be fed to the MX589's RX Filter by a suitable gain and DC level adjusting circuit. This circuit can be built with external components around the on-chip RX Input Amplifier. The gain should be set so that the signal level at the RX Feedback pin is nominally 1V peak to peak (for V_{DD}=5.0V) centered around V_{BIAS} when receiving a continuous "1111000011110000.." data pattern.

Positive going signal excursions at RX Feedback pin will produce a logic "0" at the RX Data Output. Negative going excursions will produce a logic "1."

The received signal is fed through the lowpass RX Filter, which has a -3dB corner frequency of 0.56 times the data bit-rate, before being applied to the Level Measure and Clock and Data extraction blocks.

The Level Measuring block consists of two voltage detectors, one of which measures the amplitude of the 'positive' parts of the received signal. The other measures the amplitude of the 'negative' portions. (Positive refers to signal levels higher than $V_{DD}/2$, and negative to levels lower than $V_{DD}/2$.)

External capacitors are used by these detectors, via the Doc1 & Doc2 pins, to form voltage 'hold' or 'integrator' circuits. These two levels are then used to establish the optimum DC level decision-thresholds for the Clock and Data extraction, depending upon the RX signal amplitude and any DC offset.

RX Circuit Control Modes

The RX Circuit blocks are controlled by externally applied logic levels to the PLLacq, $\overline{\text{RX Hold}}$ and RXDCacq pins (see Table 2). Table 2 shows control signals, the functions they control and their modes of operation.

RX Hold	RXDCacq	PLLacq	RX Level Measurement Mode	PLL Mode
LO	LO	LO	Hold	Hold
LO	LO	HI	Hold	Acquire
HI	LO	LO	Averaging Peak Detect	Track
HI	LO	HI	Averaging Peak Detect	Acquire
X	LO to HI	X	Clamp	X
HI	HI	HI	Fast Peak Detect	Acquire
LO	HI	LO	Fast Peak Detect	Hold
HI	LO	HI to LO	Averaging Peak Detect	Medium Bandwidth
HI	HI	LO	Fast Peak Detect mode	Track

X=Don't Care

PLL Acquire: Sets the PLL bandwidth wide enough to allow a lock to the received signal in less than 8 zero crossings. The Acquire mode will operate as long as PLLacq is a logic "1".

PLL Medium Bandwidth: The correction applied to the extracted clock is limited to a maximum of ±1/16th bit-period for every two received zero-crossings. The PLL operates in this mode for a period of about 30 bits immediately following a "1" to "0" transition of the PLLacq input, provided that the RX Hold input is a logic "1".

PLL Track Mode (Narrow Bandwidth): The correction applied to the extracted clock is limited to a maximum of ±1/64th bit-period for every two received zero-crossings. The PLL operates in this mode whenever the RX Hold Input is a logic "1" and PLLacq has been a logic "0" for at least 30 bit periods (after Medium Bandwidth operation for instance).

PLL Hold: The PLL feedback loop is broken, allowing the RX Clock to freewheel during signal fade periods.

RX Level Measurement Clamp: Operates for one bit-time after a "0" to "1" transition of the RXDCacq input. The external capacitors are rapidly charged towards a voltage mid-way between the received signal input level and V_{BIAS}, with the charge time-constant being of the order of 0.5bit-time.

RX Level Measurement Fast Peak Detect: The voltage detectors act as peak-detectors, one capacitor is used to capture the 'positive'-going signal peaks of the RX Filter output signal and the other capturing the 'negative'-going peaks. The detectors operate in this mode whenever the RXDCacq input is at a logic "1," except for the initial 1-bit Clamp-mode time.

RX Level Measurement Averaging Peak Detect: Provides a slower but more accurate measurement of the signal peak amplitudes.

RX Level Measurement Hold: The capacitor charging circuits are disabled so that the outputs of the voltage detectors remain substantially at the last readings (discharging very slowly [time-constant approx. 2,000 bits] towards V_{BIAS}).

Table 2 - RX Circuit Controls

Application Information .....

RX Circuit Control Sequence

As shown in Figure 6, a data transmission generally begins with a preamble of, for example, "1100110011001100," to allow the receive modem to establish timing- and level- lock as quickly as possible. During the time that the preamble is expected, the RXDCacq and PLLacq inputs should be switched from a logic "0 to 1" so that the Level Measuring and Clock Extraction modes are operated and sequenced as shown.

The RX Hold input should normally be held at a logic "1" while data is being received, but may be driven to a logic "0" to freeze the Level Measuring and Clock Extraction circuits during a fade. If the fade lasts for less than 200 bit periods, normal operation can be resumed by returning the RX Hold input to a logic "1" at the end of the fade. For longer fades, it may be better to reset the Level Measuring circuits by placing the RXDCacq to a logic "1" for 10 to 20 bit periods.

RX Hold has no effect on the Level Measuring circuits while RXDCacq is at a logic "1," and has no effect on the PLL while PLLacq is at a logic "1."

A logic "0" on RX Hold does not disable the RX Clock output, and the RX Data Extraction and S/N Detector circuits will continue to operate.

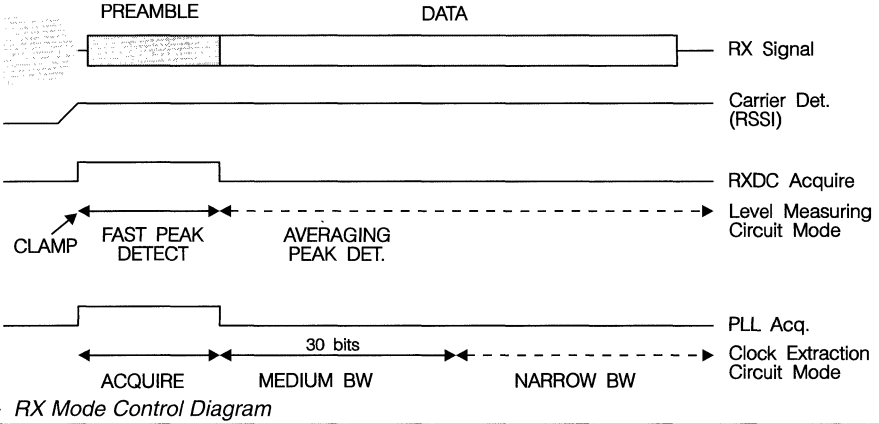


Figure 6 - RX Mode Control Diagram

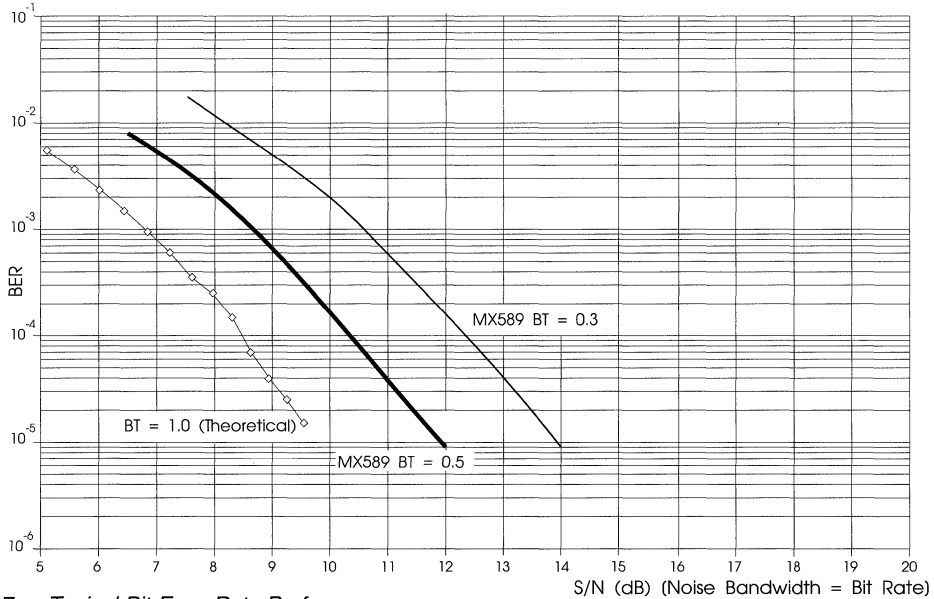


Figure 7 - Typical Bit-Error-Rate Performance

Application Information .....

TX Signal Path Description

The binary data applied to the 'TX Data' input is retimed within the chip on each rising edge of the 'TX Clock' and then converted to a 1-volt peak-to-peak binary signal centered about V_{BIAS} (for V_{DD}= 5.0V)

If the 'TX Enable' input is 'high,' then this internal binary signal will be connected to the input of the lowpass TX Filter, and the output of the filter connected to the 'TX Out' pin.

TX Enable	TX Filter Input	TX Out Pin
'1' (high)	1 volt p-p Data In	Filtered Data
"0" (low)	V_{BIAS}	V_{BIAS} via 500kΩ

A 'low' input to the 'TX Enable' will connect the input of the TX Filter to V_{BIAS}, and disconnect the 'TX Out' pin from the filter, connecting it instead to V_{BIAS} through a high resistance (nominally 500kΩ).

The TX Filter has a lowpass frequency response, which is approximately gaussian in shape as shown in Figure 9, to minimize amplitude and phase distortion of the binary signal while providing sufficient attenuation of the high frequency-components which would otherwise cause interference into adjacent radio channels. The actual filter bandwidth to be used in any particular application will be determined by the overall system requirements. The attenuation-vs-frequency response of the transmit filtering provided by the MX589 have been designed to meet the specifications for most GMSK modem systems, having a -3dB bandwidth switchable between 0.3 and 0.5 times the data bit-rate (BT).

Note that an external RC network is required between the 'TX Out' pin and the input to the Frequency Modulator (see Figures 2 and 3). This network, which can form part of any d.c. level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to capacitor C_1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.

The component values should be chosen so that the product of the resistance (Ω) and the capacitance (Farads) is:

BT of 0.3 = 0.34/bit rate (bits/second)
BT of 0.5 = 0.22/bit rate (bits/second)
with the following suitable values for common bit rates:

Data Rate	BT	R	C
8000 bps	0.3	91.0kΩ	470pF
4800 bps	0.5	100kΩ	470pF
9600 bps	0.5	47.0kΩ	470pF
19,200 bps	0.5	22.0kΩ	470pF
32,000 bps	0.3	47.0kΩ	220pF
32,000 bps	0.5	47.0kΩ	150pF
38,400 bps	0.3	47.0kΩ	180pF
38,400 bps	0.5	47.0kΩ	120pF

The signal at 'TX Out' is centered around V_{BIAS}, going positive for logic "1" (high) level inputs to the 'TX Data' input and negative for logic "0" (low) inputs.

When the transmit circuits are put into a 'powersave' mode (by a logic "1" to the 'TX PS' pin) the output voltage of the TX Filter will go to V_{SS}. When power is subsequently restored to the TX Filter, its output will take several bit-times to settle. The 'TX Enable' input can be used to prevent these abnormal voltages from appearing at the 'TX Out' pin.

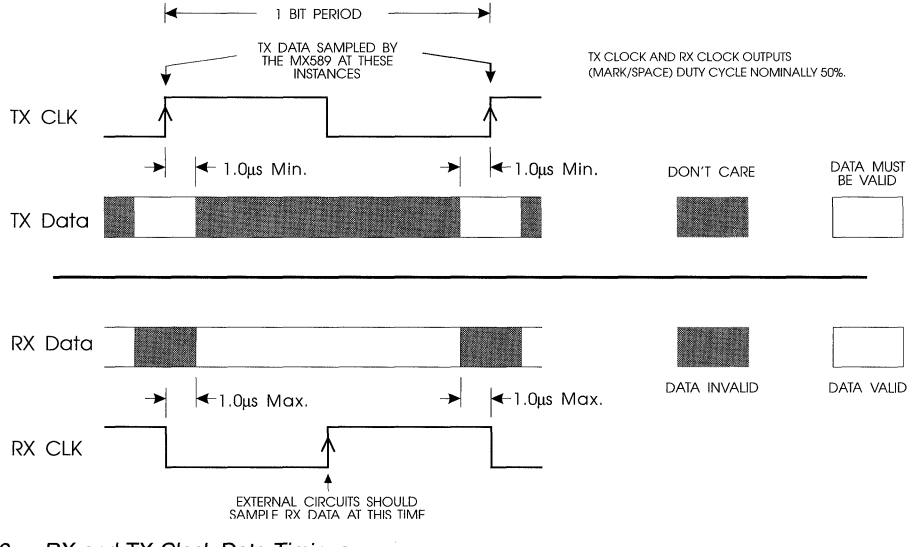


Figure 8 - RX and TX Clock Data Timings

Application Information .....

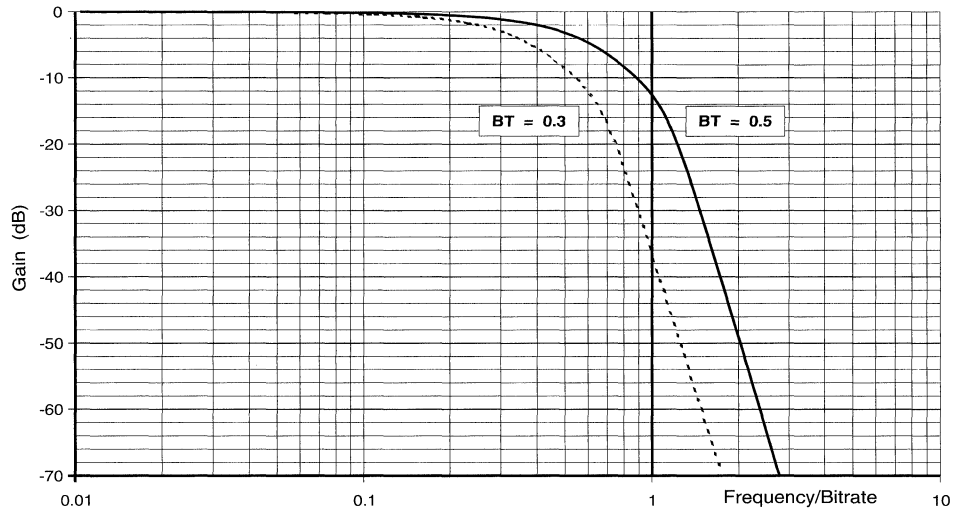


Figure 9 - TX Filter Response

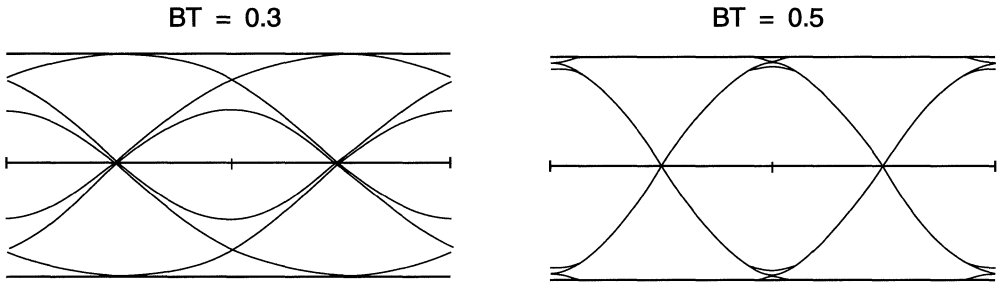


Figure 10 - Typical Transmit Eye Patterns

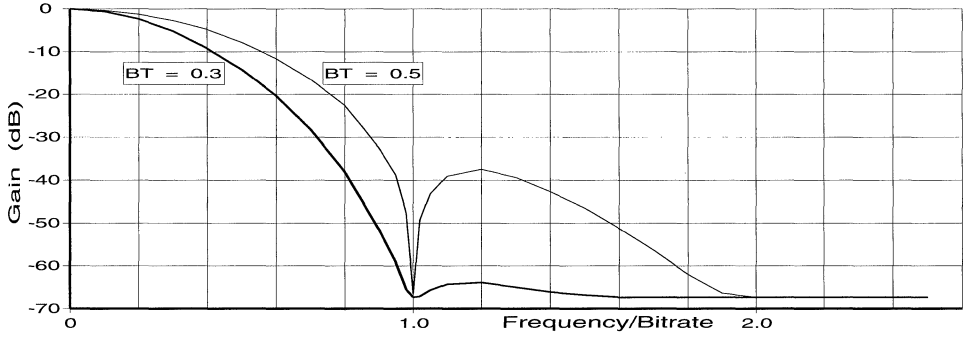


Figure 11 - TX Output Spectrum (Random Data)

Application Information .....

Radio Channel Requirements

To achieve legal adjacent channel performance at high bit-rates, a radio with an accurate carrier frequency and an accurate modulation index is required.

For optimum channel utilization, (eg. low BER and high data-rates) attention must be paid to the phase and frequency response of both the IF and baseband circuitry.

Bitrate, BT and Bandwidth

The maximum data rate that can be transmitted over a radio channel depends on the following:

- Channel spacing
- Allowable adjacent channel interference
- TX filter bandwidth
- Peak carrier deviation (Modulation Index)
- TX and RX carrier frequency accuracies
- Modulator and Demodulator linearity
- RX IF filter frequency and phase characteristics
- Use of error correction techniques
- Acceptable error-rate

As a guide to MOBITEX operation, a raw data-rate of 8kbps at 12.5kHz channel spacing may be achievable - depending on local regulatory requirements- using a ±2kHz maximum deviation, a BT of 0.3, and no more than 1.5kHz discrepancy between TX & RX carrier frequencies.

Forward error correction (FEC) could then be used with interleaving to reduce the effect of burst errors.

Reducing the data-rate to 4,800bps would allow the BT to be increased to 0.5, improving the error-rate performance.

For CDPD operation, a raw data-rate of 19.2kbps at 30kHz channel spacing may be utilized with a ±8kHz maximum deviation, a BT of 0.5, and no more than 3kHz discrepancy between TX & RX carrier frequencies.

The above values should be used as a guide only. Regulatory compliance of a design should be verified.

FM Modulator, Demodulator and IF

For optimum performance, the 'eye' pattern of the received signal (when receiving random data) applied to the MX589 should be as close as possible to the Transmit 'eye' pattern examples shown in Figure 11.

Of particular importance are general symmetry, cleanliness of the zero-crossings, and for a BT of 0.3, the relative amplitude of the inner eye opening.

To achieve this, attention must be paid to -

- Linearity and frequency/phase response of the TX frequency modulator. Unless the transmit data is especially encoded to remove low frequency components, the modulator frequency response should extend down to a few hertz. This is because two-point modulation is necessary for synthesized radios.
- Bandwidth & phase response of the RX IF filters.
- Accuracy of the TX and RX carrier frequencies - any difference will shift the received signal towards one of the skirts of the IF filter response.

Ideally, the RX demodulator should be d.c. coupled to the MX589 'RX Signal In' pin (with a d.c. bias added to center the signal at the RX Feedback pin around $V_{DD}/2$ [V_{BIAS}]). However a.c. coupling can be used provided that:

- The 3 dB cut-off frequency is 20Hz or below (i.e. a 0.1µF capacitor in series with 100kΩ).
- The data does not contain long sequences of consecutive ones or zeroes.
- Sufficient time is allowed after a step change at the discriminator output (resulting from channel changing or the appearance of an RF carrier) for the voltage into the MX589 to settle before the 'RXDCacq' line is strobed.

Application Information .....

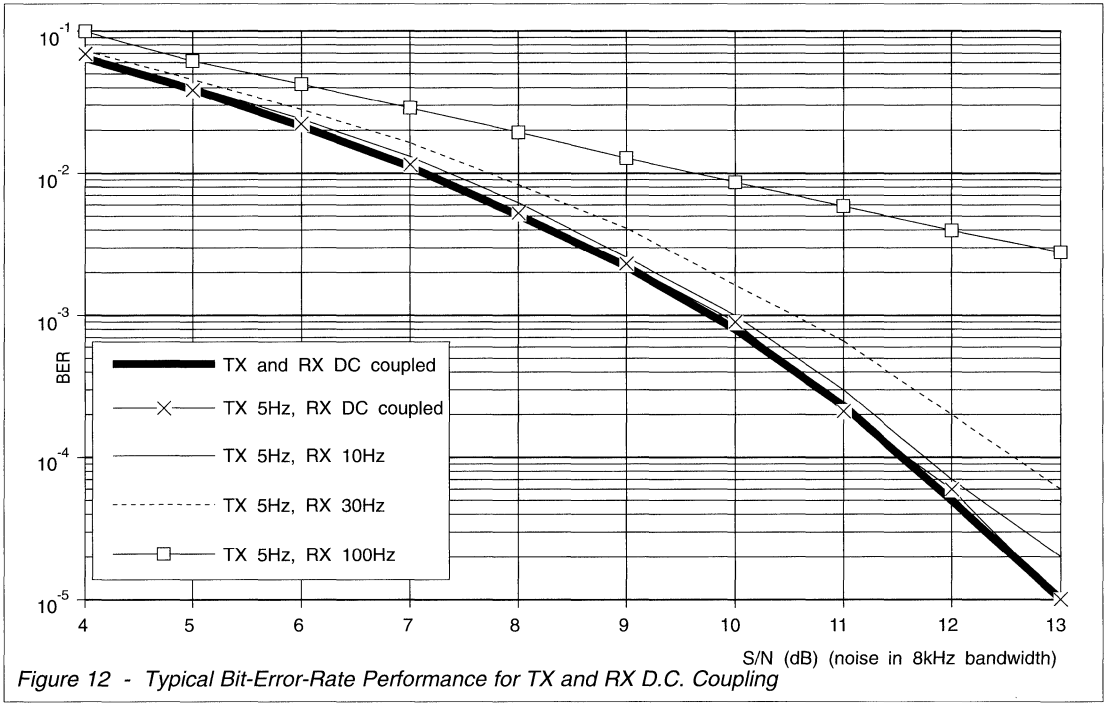


Figure 12 - Typical Bit-Error-Rate Performance for TX and RX D.C. Coupling

A.C. Coupling of TX and RX Signals

Practical applications may require AC coupling from the MX589's TX Output to the frequency modulator and between the receiver's frequency discriminator and the MX589's RX Input. This creates two problems:

1) AC coupling of the signal degrades the Bit Error Rate (BER) performance of the MX589. Figure 12 (above) shows the typical static BER performance of the MX589 at 8kbps (without FEC) for different levels of AC coupling.

2) AC coupling at the RX Input will transform a step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the MX589's level measuring circuits. The time for this step to decay to 37% of its original value is "RC":

$$RC = \frac{1}{2\pi \cdot \text{the 3dB cut-off frequency of the RC network}}$$

and is 8ms (64 bit-times) at 8kbps for a 20Hz network.

For these reasons, the optimum -3dB cut-off frequencies are approximately 5.0Hz in the TX path and 20.0Hz in the RX path under the following conditions:

Data Rate = 8kbps TX BT = 0.3
V_{DD} = 5.0V T_{AMB} = 25°C

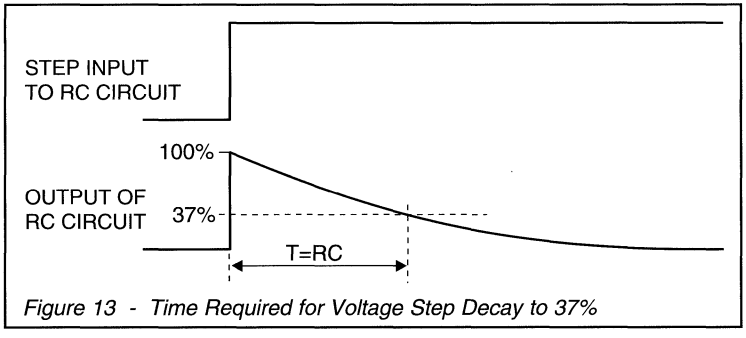


Figure 13 - Time Required for Voltage Step Decay to 37%

Application Information .....

Two Point Modulation

When designing the MX589 into a radio that uses a frequency synthesizer, a two-point modulation technique is recommended. This is both to prevent the radio's PLL circuitry from counteracting the modulation process, and to provide a clean flat modulation response down to d.c.

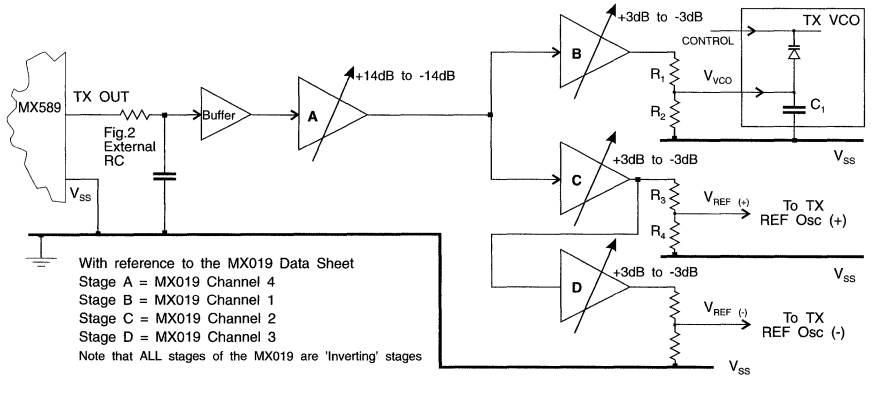
Figure 14 shows a suggested basic configuration to provide a two-point modulation drive from the MX589 TX Output using MX•COM's MX019 Digitally Controlled 'Quad' Amplifier Array. The MX019 elements provide individual set-up, calibration and dynamic control of modulation levels. Level setting control of the amplifiers/ attenuators of the MX019 is via an 8-bit data word.

With reference to Figure 14, the buffer amplifier is required to prevent loading of the MX589 external RC circuit.

Stage B, with R_1/R_2, provides suitable signal and d.c. levels for the VCO varactor; C_1 is RF decoupling. The drive level should be adjusted (digitally) to provide the desired deviation.

Stage C, with R_3/R_4, provides the Reference Oscillator drive (application dependent). This parameter is set by adjusting for minimum a.c. signal on the PLL control voltage with a low-frequency modulating signal (inside the PLL bandwidth) applied.

Stage D could be used with the components shown if a negative reference drive is required. Stage A provides buffering and overall level control.



Note: this example has not been verified.

Figure 14 - An Example of Two-Point Modulation Drive with Individual Adjustment Using the MX019

'Acquisition' and 'Hold' Modes

The 'RXDCacq' and 'PLLacq' inputs must be pulsed 'High' for about 16 bits at the start of reception to ensure that the DC measurement and timing extraction circuits lock-on to the received signal correctly. Once lock has been achieved, then the above inputs should be taken 'Low' again.

In most applications, there will be a DC step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the distant transmitter is turned on.

The MX589 can tolerate DC offsets in the received signal of at least ±0.5V with respect to V_{BIAS}, (measured at the RX Feedback pin). However, to ensure that the DC offset compensation circuit operates correctly and with minimum delay, the 'Low' to 'High' transition of the 'RXDCacq' and 'PLLacq' inputs should occur after the mean input voltage to the MX589 has settled to within about 0.1V of its final value. (Note that this can place restrictions on the value of any series signal coupling capacitor.)

As well as using the 'RX Hold' input to freeze the Level Measuring and Clock Extraction circuits during a signal 'fade', it may also be used in systems which use a continuously transmitting control channel to freeze the RX circuitry during transmission of a data packet, allowing reception to resume afterwards without losing bit synchronization. To achieve this, the MX589 'Xtal' clock needs to be accurate enough that the derived 'RXClock' output does not drift by more than about 0.1 bit time from the actual received data-rate during the time that the 'RXHold' input is 'Low'.

The 'RXDCacq' input, however, may need to be pulsed 'High' to re-establish the level measurements if the 'RXHold' input is 'Low' for more that a few hundred bit-times.

The voltages on the Doc1 and Doc2 pins reflect the average peak positive and negative excursions of the (filtered) receive signal, and could therefore be used to derive a measure of the data signal amplitude. Note however, that these pins are driven from very high-impedance circuits, so that the DC load presented by any external circuitry should exceed 10MΩ to V_{BIAS}.

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0V
Input Voltage at any pin (ref V_{SS}=0V)	-0.3 to (V_{DD}+ 0.3V)
Sink/Source Current (supply pins)	±30mA
(other pins)	±20mA
Total Device Dissipation (@ T_{AMB}=25°C)	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Characteristics

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Data Rate = 8000 bps

Xtal/Clock f_0 = 4.096 MHz

Noise bandwidth = bit rate

1

Operating Limits			Remarks		Min.	Max.	Unit
Supply Voltage (V_{DD})					3.0	5.5	V
Operating Temperature					-40	+85	°C
RX & TX Data Rate			$V_{DD} \geq$ 3.0V		4,000	20,000	bps
			$V_{DD} \geq$ 4.5 V		4,000	40,000	bps
Xtal/Clock Frequency			$V_{DD} \geq$ 3.0V		1.0	5.0	MHz
			$V_{DD} \geq$ 4.5 V		1.0	6.5	MHz
"High" Pulse Width			Note 10		60.0	-	ns
"Low" Pulse Width			Note 10		60.0	-	ns
Static Values							
Supply Current							
(for V_{DD}=3.0V)	**TX PS**	**RX PS**	1				
	1	1		-	0.5	-	mA
	0	1		-	1.0	-	mA
	1	0		-	1.0	-	mA
	0	0		-	1.5	-	mA
(for V_{DD}=5.0V)	**TX PS**	**RX PS**	1				
	1	1		-	1.0	-	mA
	0	1		-	2.0	-	mA
	1	0		-	3.0	-	mA
	0	0		-	4.0	-	mA
Input Logic Levels							
Logic "1"				3.5	-	-	V
Logic "0"				-	-	1.5	V
Logic Input Current			2	-5.0	-	5.0	µA
Logic "1"Output Level at IOH = -120µA				4.6	-	-	V
Logic "0"Output Level at IOL = 120µA				-	-	0.4	V

Characteristics	See Note	Min.	Typ.	Max.	Unit
Transmit Parameters					
TX Output Impedance	3	-	1.0	-	kΩ
TX Output Level	4,11	0.8	1.0	1.2	V p-p
TX Data Delay (BT = 0.3)	5	-	2.0	2.5	bit-periods
(BT = 0.5)	5	-	1.5	2.0	bit-periods
TX PS to Output-Stable Time	6	-	4.0	-	bit-periods
Receive Parameters					
RX Amplifier -					
Input Impedance		1.0	-	-	MΩ
Output Impedance	7	-	10.0	-	kΩ
Voltage Gain		-	50.0	-	dB
RX Filter Signal Input Level	8,11	0.7	1.0	1.3	V p-p
RX Time Delay	9	-	-	3.0	bit-periods
On-Chip Xtal Oscillator					
R_{IN}		10.0	-	-	MΩ
R_{OUT}	12	-	50.0	-	kΩ
Voltage Gain	12	-	25.0	-	dB

Notes

1. Not including current drawn from the MX589 pins by external circuitry. See Absolute Maximum Ratings.
2. For V_{IN} in the range V_{SS} to V_{DD}.
3. For a load of 10kΩ or greater. TX PS input at logic "0"; TX Enable = "1".
4. Data pattern of "1111000011110000 .."
5. Measured between the rising edge of 'TX Clock' and the center of the corresponding bit at 'TX Out.'
6. Time between the falling edge of 'TX PS' and the 'Tx Out' voltage stabilising to normal output levels.
7. For a load of 10kΩ or greater. RX PS input at logic "0".
8. For optimium performance, Measured at the 'RX Feedback' pin for a "1111000011110000 ..." pattern.
9. Measured between the center of bit at 'RX Signal In' and corresponding rising edge of the 'RX Clock'.
10. Timing for an external clock input to the Xtal/clock pin.
11. Typical level shown is at V_{DD}=5.0V; actual levels are proportional to applied V_{DD}.
12. Small signal measurement at 1.0kHz with no load on $\overline{Xtal}$ output.

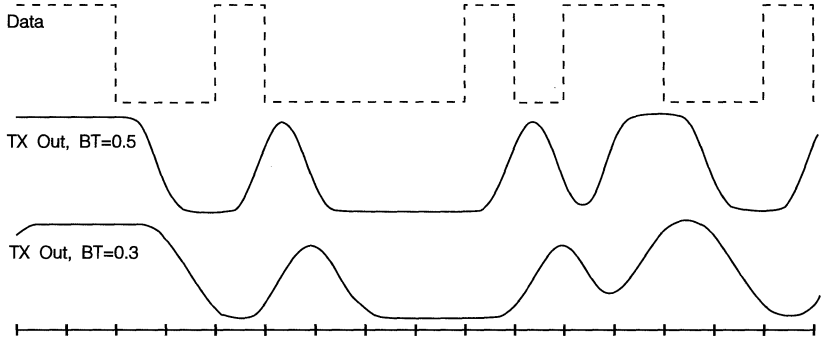


Figure 15 - Typical Signal Waveforms

MX•COM, INC.

Preliminary Information

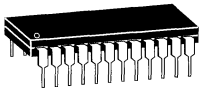
MX809

C-BUS COMPATIBLE

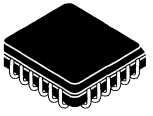
MSK MODEM

DESCRIPTION

The MX809 is an intelligent, half-duplex 1200 baud MSK Modem which operates under C-BUS control. This modem provides software selectable checksum generation and error checking in accordance with MPT1327.



MX809J
24-pin CDIP



MX809LH
24-pin PLCC

In TX Mode the MX809 will:

1. a) Accept from the host and transmit 8-bit bytes of data as instructed (preamble, sync, address and data).

b) Internally calculate and insert a 2 byte checksum based on the preceding 6 bytes of data, or

c) Disable the internal checksum generator and continuously transmit the data supplied.

2. Transmit 1 hang-bit and go to TX Idle when all loaded data bytes have been transmitted.

In RX Mode the MX809 will:

1. Detect and carry out bit synchronization within 16 bits.

2. a) Search and detect the user-programmed Sync (or its opposite logic sense) Word and carry out frame synchronization. Data will then be output in 8-bit bytes via the RX Data Buffer.

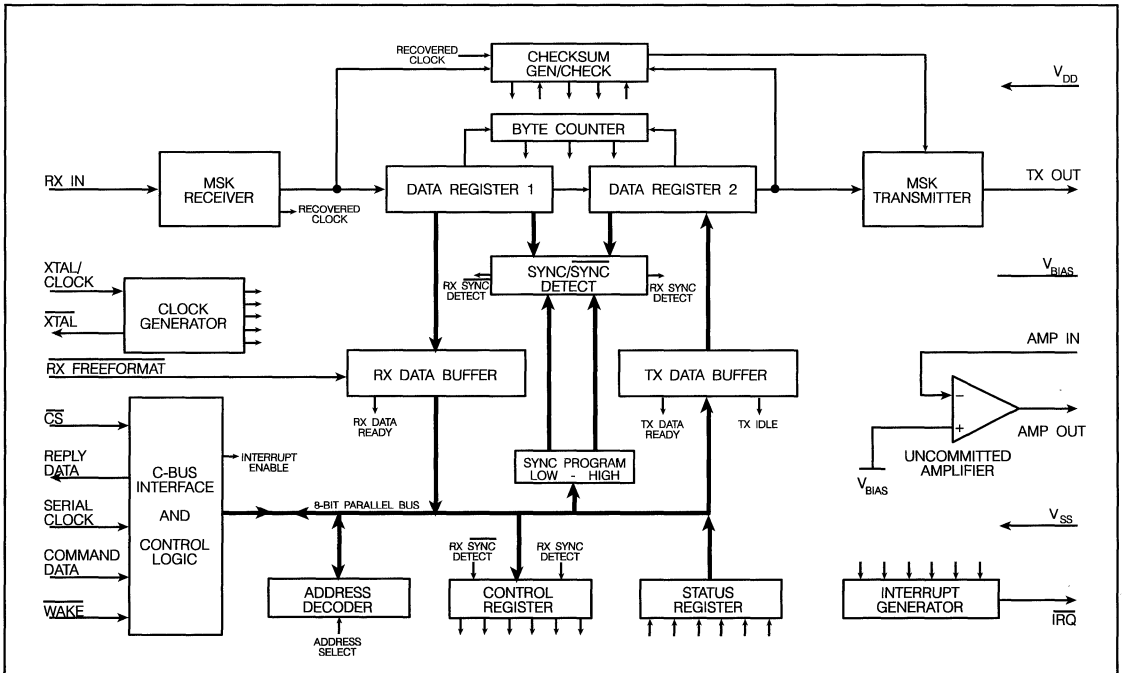


Figure 1 - MX809 1200 Baud MSK Modem

DESCRIPTION...

b) Use the received checksum to calculate the presence of any errors, setting the Status Register accordingly.

3. Make the incoming data directly available via the RX Data Buffer (RX Freeformat), overriding the synchronization requirements.

RX input timing is achieved by recovering an RX clock from the incoming data stream. Output tones are timed to the internally generated TX clock. Filter, register clocks, and transmit MSK tone frequencies are derived internally from the external Xtal or clock pulse input.

A 4.032 MHz Xtal or clock input is required for compliance with the MPT1327 Signalling Specification. *Note: All information contained in this data bulletin is specified using a 4.032 MHz Xtal, 1200 bps baud rate, with Mark and Space frequencies of 1200 Hz and 1800 Hz.* The MX809 has a non-committed amplifier on-chip for general applications in the DBS 800 serie. The MX809 is a low-power 5V integrated circuit that incorporates Powersave modes to further reduce power requirements. It is available in 24-pin Cerdip and 24-lead SMT Packages.

PIN FUNCTION CHART

Pin	Function
1	**$\overline{\text{Xtal}}$**: This is the output of the on-chip clock oscillator. External components are required at this input when a Xtal input is used. See Figure 2, Inset.
2	**Xtal/Clock**: This is the input to the on-chip clock oscillator inverter. A Xtal or externally derived clock should be connected here. See Figure 2, Inset.
3	**Interrupt Request ($\overline{\text{IRQ}}$)**: The output of this pin indicates an interrupt condition to the microcontroller by going to a logic "0." This is a "wire-or able" output that enables the connection of up to 8 peripherals to 1 interrupt port on the microcontroller. This pin is an open-drain output, and therefore has a low impedance pulldown to logic "0" when active and a high impedance when inactive. The conditions that cause interrupts are indicated in the Status Register and are shown below: TX Idle — RX Data Ready — TX Data Ready RX SYNC Detect — RX SYNC Detect Interrupt outputs can be disabled by bit 3 of the Control Register.
4	**N/C**
5	**N/C**
6	**$\overline{\text{RX Freeformat}}$**: When this input is logic "0" in the RX Mode, it allows received data to be read from the RX Data Buffer via the Reply Data line without having to achieve byte synchronization (SYNC/$\overline{\text{SYNC}}$) first. Data will continue to be available after this input goes to a logic "1" until either a SYNC or $\overline{\text{SYNC}}$ Prime Bit is set or the modem is set to TX Mode. When held at a logic "1" the modem operates normally. This pin has an internal 1MΩ pullup resistor. Note: If this input is held at a logic "0" in the TX Mode, the RX Data Ready bit in the Status Register may occasionally be set, but not cause an interrupt. If this input is a logic "0" when going into the RX Mode, an RX Data Ready interrupt may be generated immediately (in this case the first byte of RX data should be ignored).
7	**V_{BIAS}**: The internal circuitry bias line, this is held at $V_{DD}/2$. This pin must be decoupled to V_{SS} by capacitor C_3. See Figure 2.
8	**Amp In**: The inverting input to the on-chip uncommitted amplifier.
9	**Amp Out**: The output of the on-chip uncommitted amplifier.
10	**RX In**: This is the 1200 baud, 1200Hz/1800Hz received MSK signal input. The input signal to this pin must be a.c. coupled via capacitor C_4. See Figure 2.

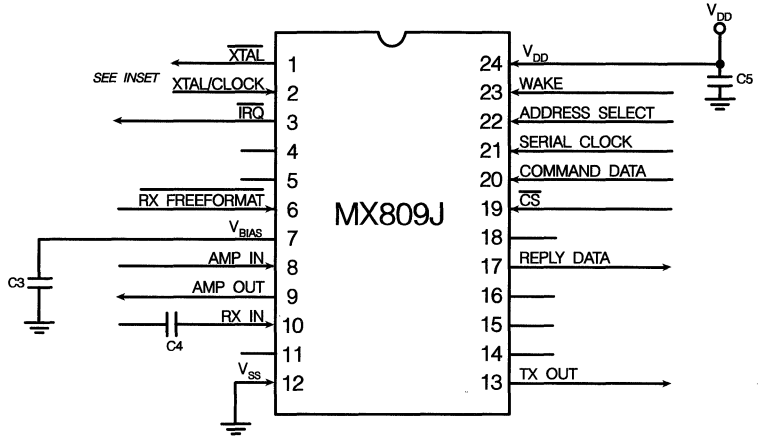
PIN FUNCTION CHART

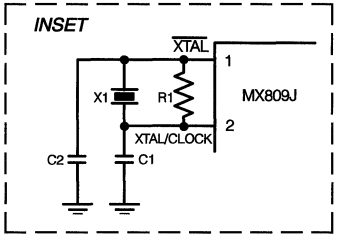
Pin	Function
11	**N/C**
12	V_{SS}: Negative Suply (GND).
13	**TX Out**: This is the 1200 baud, 1200Hz/1800Hz MSK TX output. When not transmitting data the output impedance of this pin is high. On power-up this output can be any level. A General Reset command is required to ensure that this output attains V_{BIAS} initially.
14	**N/C**
15	**N/C**
16	**N/C**
17	**Reply Data**: This is the C-BUS serial data output to the microcontroller. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the microcontroller. See Timing Diagrams.
18	**N/C**
19	**Chip Select (CS)**: The C-BUS data loading control function, this input is provided by the microcontroller. Data transfer sequences are initiated, completed or aborted by the CS signal. See Timing Diagrams.
20	**Command Data**: This is the C-BUS serial data input from the microcontroller. Data is loaded to this device in 8-bit bytes, MSB (bit7) first, and LSB (bit 0) last, synchronized to the Serial Clock. See Timing Diagrams.
21	**Serial Clock**: This is the C-BUS serial clock input. This clock, produced by the microcontroller, is used for transfer timing of commands and data to and from the MSK Modem. See Timing Diagrams.
22	**Address Select**: This pin enables two MX809s to be used on the same C-BUS, providing full-duplex operation. When at a logic "1" Address/Command bytes (with the exception of a General Reset) must have bit 3 set to a logic "1" to address this device. See Tables 1 and 2.
23	**$\overline{\text{Wake}}$**: This input can be used to reactivate the MX809 from Powersave. The device will be in Powersave when both this pin and bit 2 of the Control Register are set to a logic "1." Recovery from Powersave is achieved by putting either the $\overline{\text{Wake}}$ pin or the Powersave bit in the Control Register to logic "0." This allows MX809 activation by the microcontroller or an external signal, such as R.S.S.I. or Carrier Detect.
24	V_{DD}: Positive supply. A single +5V power supply is required. Levels and voltages within the MSK Modem are dependent upon this supply.

Powersave (CR bit 2)	$\overline{\text{Wake}}$	MX809 Condition
1	1	Powersave
0	1	Enabled
1	0	Enabled
0	0	Enabled

Note: Pins 4, 5, 11, 14, 15, 16 and 18 may be connected to V_{SS} to improve screening.

External Components





Component	Value
R_1	1.0MΩ
C_1	33.0pF
C_2	33.0pF
C_3	1.0µF
C_4	0.1µF
C_5	1.0µF
X_1	4.032MHz

Tolerance: R = ±10%; C = ±20%

NOTE: XTAL circuit capacitors C_1 (C_D) and C_2 (C_G) shown in the inset are recommended in accordance with MX-COM's Crystal Oscillator Application Note, March 1990.

Figure 2 - External Components

Modem Performance

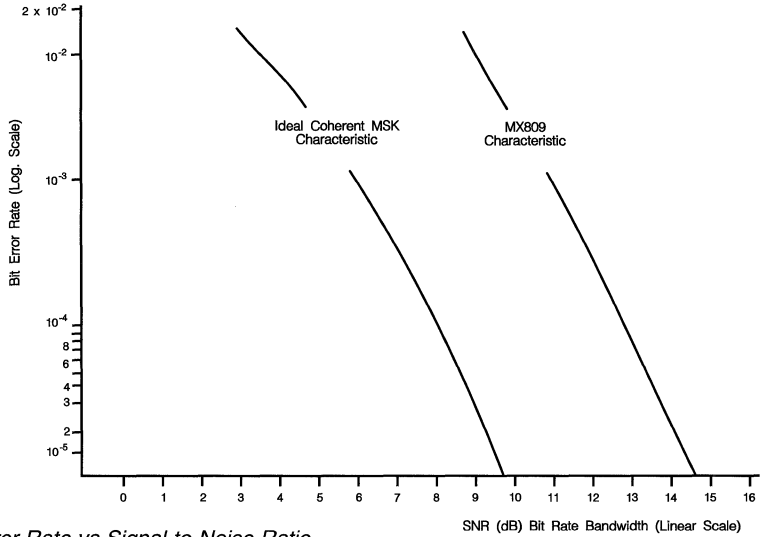


Figure 3 - Bit Error Rate vs Signal-to-Noise Ratio

Controlling Protocol

Control of the functions within the MX809 MSK Modem is by a group of Address/Commands (A/Cs) and appended data to and from the system microcontroller via the C-BUS. Two separate MSK Modems can be addressed. The use of these A/Cs is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB LSB	Notes
General Reset	01	0 0 0 0 0 0 0 1 +	Control Register bits set to logic "0"
Write to Control Register	40	0 1 0 0 0 0 0 0 +	1 byte instruction to Control Register
Read Status Register	41	0 1 0 0 0 0 0 1 +	1 byte reply from Status Register
Read RX Data Buffer	42	0 1 0 0 0 0 1 0 +	1 byte of data from RX Data Buffer
Write to TX Data Buffer	43	0 1 0 0 0 0 1 1 +	1 byte of data to TX Data Buffer
Write to SYNC Program	44	0 1 0 0 0 1 0 0 +	2 bytes of SYNC Word to SYNC Prog. Reg.

Table 1 - Modem No. 1 C-BUS Address/Commands - (Address Select input at a logic "0")

Address/Commands

Instructions and data transactions to and from the MX809 consist of an Address/Command (A/C) byte followed by either further instructions or data, or a Status or RX data Reply.

Control and configuration is by writing instructions from the microcontroller to the Control Register [40_H (48_H)].

Reporting of the MX809 configurations is by reading the Status Register [41_H (49_H)]. Instructions and data are transferred via C-BUS in accordance with the timing information given in Figure 4.

Data to be transmitted as MSK is sent to the TX Data Buffer via the Command Data line. Received data is read from the RX Data Buffer via the Reply Data line.

Instructions and data transactions to and from this device are preceded by the relevant A/C.

C-BUS allocations for the MX809 are shown in Tables 1 and 2.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB LSB	Notes
General Reset	01	0 0 0 0 0 0 0 1 +	Control Register bits set to logic "0"
Write to Control Register	48	0 1 0 0 1 0 0 0 +	1 byte instruction to Control Register
Read Status Register	49	0 1 0 0 1 0 0 1 +	1 byte reply from Status Register
Read RX Data Buffer	4A	0 1 0 0 1 0 1 0 +	1 byte of data from RX Data Buffer
Write to TX Data Buffer	4B	0 1 0 0 1 0 1 1 +	1 byte of data to TX Data Buffer
Write to SYNC Program	4C	0 1 0 0 1 1 0 0 +	2 bytes of SYNC Word to SYNC Prog. Reg.

Table 2 - Modem No. 2 C-BUS Address/Commands - (Address Select input at a logic "1")

Address Select

This input allows 2 MSK Modems on the same BUS, using the correct addressing.

When operating in a system using 2 MSK Modems, one MSK Modem is designated No. 1 and requires its Address Select input to be held at a logic "0." The second Modem (No. 2) requires its Address Select input to be held at logic "1."

All C-BUS transactions with Modem 1 will use Address/Command allocations 40_H to 44_H (Table1) and transactions with Modem 2 will use 48_H to $4C_H$ (Table 2).

For explanation purposes, further descriptions of MX809 MSK Modem internal register functions will deal primarily with MSK Modem No. 1 (Address Select at logic "0").

Controlling Protocol

"Write to Control Register"

This "Write Only" register directs the Modem's operation.

Setting	Control Bits
MSB Bit 7	***Transmitted First*** Not used Set to "0"
6	Not used Set to "0"
5 0 1	**$\overline{\text{SYNC}}$ Prime** Primed
4 0 1	**SYNC Prime** Primed
3 0 1	**Interrupt Enable** Disable Enable
2 0 1	**Powersave** Normal Operation Powersave
1 0 1	**Checksum Enable** Disable Enable
0 0 1	**RX/TX Mode** RX TX

Table 3 - Control Register

$\overline{\text{SYNC}}$ Prime: When set, this bit enables $\overline{\text{SYNC}}$ Word detection. It is cleared on a successful $\overline{\text{SYNC}}$ Word detection.

SYNC Prime: When set, this bit enables SYNC Word detection. It is cleared on a successful SYNC Word detection.

Interrupt Enable: When set, this bit allows interrupts to be output by the MX809 on the $\overline{\text{IRQ}}$ line.

Powersave: Used in conjunction with the $\overline{\text{Wake}}$ input (see Pin Functions) to control the Powersave state of the MX809.

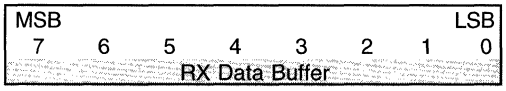
Checksum Enable: When set:

In TX: A 2-byte checksum is generated and transmitted after every 6 bytes transmitted.

In RX: After every 8 received bytes (6 information + 2 checksum) the checksum word is checked. If the checksum is correct, the RX Checksum True bit in the Status Register is set to a logic "1." When this bit is a logic "0" no checksums are generated or checked.

NOTE: Checksum operation is inhibited during the SYNC/$\overline{\text{SYNC}}$ search period.

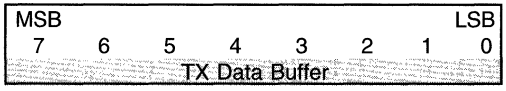
"Read RX Data Buffer"



RX Data Buffer

This "Read Only" register contains the last byte of data received from the Data Register. Data is received Bit 7 (MSB) first.

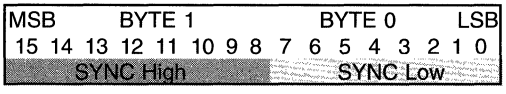
"Write to TX Data Buffer"



TX Data Buffer

This "Write Only" register contains the next byte of data to be transmitted. Bit 7 (MSB) is transmitted first.

"Write to SYNC Program"



SYNC Program

This "Write Only" register is loaded with the required SYNC word. This word (or its opposite logic sense, $\overline{\text{SYNC}}$) is compared with the received synchronization word. If the required SYNC Word is less than 16 bits, the remaining bits must be programmed as preamble (10101010...etc.). Bit 15 (MSB) is loaded first.

Controlling Protocol

"Read Status Register"

This "Read Only" register indicates the source of MX809 interrupts ($\overline{IRQ}$s).

Reading	Status Bits
MSB	***Received First***
Bit 7	**Undefined**
0	"0" or
1	"1"
6	**Undefined**
0	"0" or
1	"1"
5	**RX $\overline{SYNC}$ Detect**
0	
1	$\overline{SYNC}$
4	**RX SYNC Detect**
0	
1	SYNC
3	**TX Idle**
0	
1	Idle
2	**TX Data Ready**
0	
1	TX Data Ready
1	**RX Checksum True**
0	
1	True
0	**RX Data Ready**
0	
1	RX Data Ready

Table 4 - Status Register

RX Checksum True
This is set and an Interrupt is generated by a successful comparison of the received and self-generated checksums.

It is cleared by (1) reading the Status Register and the RX Data Buffer, and (2) $\overline{RX}$/TX being taken to logic "1."

RX $\overline{SYNC}$ Detect
This is set and an Interrupt is generated when the correct $\overline{SYNC}$ Word is detected (if $\overline{SYNC}$ Prime is set).

It is cleared by (1) reading the Status Register, and (2) setting $\overline{RX}$/TX to logic "1."

RX SYNC Detect
This is set and an Interrupt is generated when the correct SYNC Word is detected (if SYNC Prime is set).

It is cleared by (1) reading the Status Register, and (2) setting $\overline{RX}$/TX to logic "1."

TX Idle
This is set and an Interrupt is generated when all loaded TX data and 1 "hang-bit" have been transmitted.

It is cleared by (1) writing to the TX Data Buffer, and (2) setting $\overline{RX}$/TX to logic "0."

TX Data Ready
This is set and an Interrupt generated indicating that a byte of data should be written to the TX Data Buffer.

It is cleared by (1) reading the Status Register and writing a byte of data to the TX Data Buffer, and (2) setting $\overline{RX}$/TX to logic "0."

RX Data Ready
When this is set and an Interrupt generated, it indicates that the RX Data Buffer is full, and that a byte of data is to be read from the RX Data Buffer. This must be read within 8 bit periods.

It is cleared by (1) reading the Status Register and the RX Data Buffer, and (2) Setting $\overline{RX}$/TX to logic "1."

Interrupt Requests ($\overline{IRQ}$)

The conditions that cause interrupts to be output (if enabled by the Control Register) from the MX809 are:

TX Idle
TX Data Ready
RX $\overline{SYNC}$ Detect
RX Data Ready
RX SYNC Detect

The Status Register should be read to find the cause of the interrupt. Interrupts are cleared by (1) reading the Status Register, or (2) changing the state of the $\overline{RX}$/TX bit.

General Reset

Upon power-up, the bits in the MX809 Modem register, and buffers will be random (either "0" or "1"). The General Reset command (01_H) will "reset" all microcircuits on the C-BUS and has the following effect on the MX809:

All bits in the Control Register will be set to logic "0." The TX Out output will be set to V_{BIAS}.

NOTE: The Status Register, RX Data Buffer, TX Data Buffer, and SYNC Program register are not affected by the General Reset Command.

C-BUS Timing Information

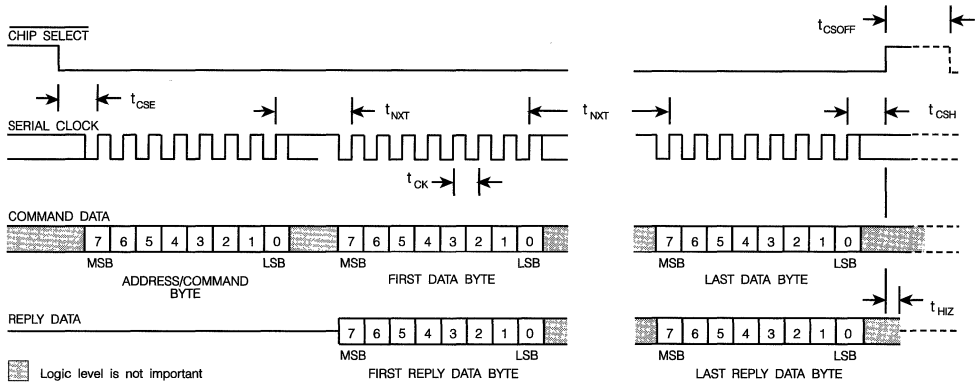


Figure 4 - C-BUS Timing

Parameter		Min.	Max.	Unit
t_{CSE}	Chip Select Low to First Serial Clock Rising Edge	2.0	-	µs
t_{CSH}	Last Serial Clock Rising Edge to Chip Select High	4.0	-	µs
t_{HIZ}	Chip Select High to Reply Data High - Z	-	2.0	µs
t_{CSOFF}	Chip Select High	2.0	-	µs
t_{NXT}	Command Data Inter-Byte Time	4.0	-	µs
t_{CK}	Serial Clock Period	2.0	-	µs

Notes:

1. Depending on the command, 1 or 2 bytes of Command Data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. Reply Data is read from the peripheral MSB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into and out of the peripheral on the rising Serial Clock edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing microcontroller serial interface formats, C-BUS compatible ICs are able to work with either polarity Serial Clock pulses.

Modem Timing Information

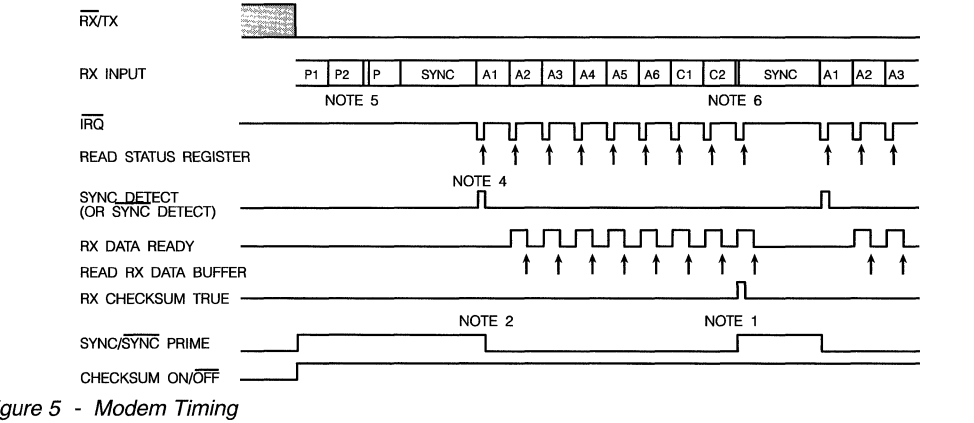
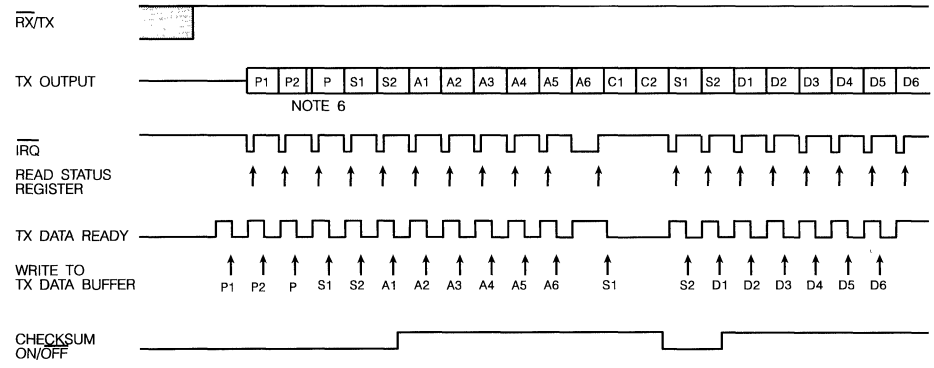


Figure 5 - Modem Timing

Notes: 1. The SYNC and SYNC detector searches the incoming bit stream starting at the end of the byte in which SYNC/SYNC Prime was set.
2. After detection of a SYNC/SYNC word, the SYNC/SYNC prime bits automatically go low (control bits 5 and 6: detector off).
3. The checksum checker is inhibited during the time SYNC/SYNC search is operating.
4. The status register will indicate whether SYNC or SYNC was detected here.
5. Any number of preamble bits can occur here.
6. Any number of bits can occur here.
7. RX Freeformat set high.

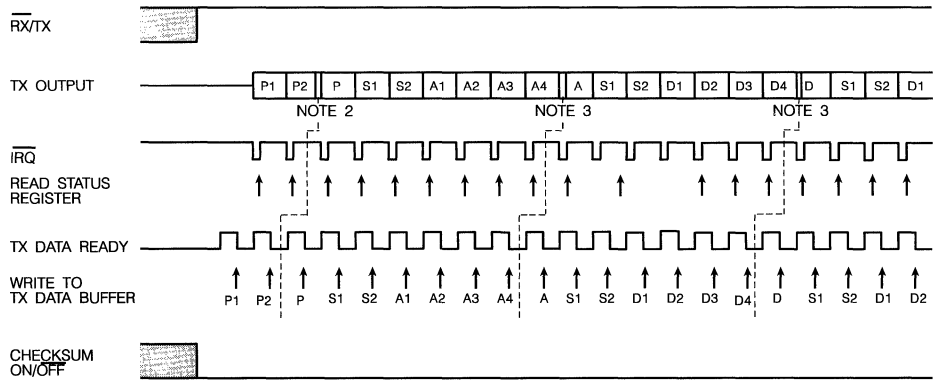
TX Timing Information

(a) TX MORE THAN ONE MESSAGE, SYNC BEFORE EVERY MESSAGE, TX CHECKSUM ENABLED



NOTES
1. Preamble and SYNC bytes are loaded as data from the microcontroller.
2. The TX output will be held at bias level when no data is being transmitted.
3. TX byte synchronization is established by the loading of the first preamble byte from the microcontroller.
4. Checksum must be turned off during preamble and SYNC words.
5. When RX/TX is low, TX output is at bias.
6. Any number of preamble bytes can occur here.

(b) TX MORE THAN ONE MESSAGE, TX CHECKSUM NOT ENABLED



NOTES
1. Preamble, SYNC words and checksums are supplied by the microcontroller in this format as data bytes.
2. Any number of preamble bytes can occur here.
3. Any number of address/data bytes can occur here.

A - Address bytes
C - Checksum bytes
D - Data bytes
H - Hang bit
P - Preamble bytes

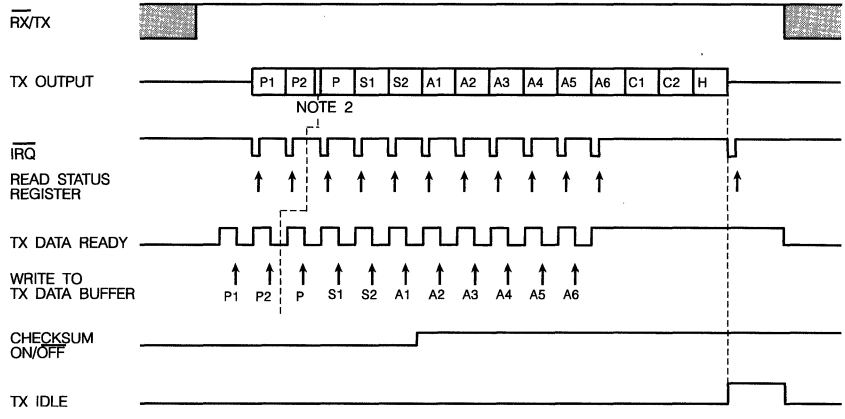
- Don't care state

TX only - In TX, Preamble and SYNC are loaded as data from the microcontroller

Figure 6 - TX Timing

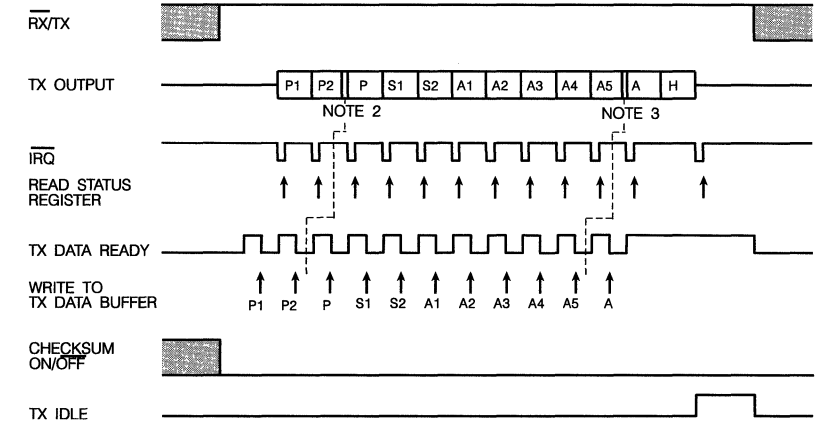
TX Timing Information

(a) TX ONE MESSAGE, TX CHECKSUM ENABLED



NOTES
1. H is the "Hangover bit" (Logic 1) appended to the transmitted message before transmission is terminated.
2. Any number of preamble bytes can occur here.
3. Transmission terminates after C1, C2 and H. Termination occurs when no further data bytes are written to the TX data buffer.

(b) TX ONE MESSAGE, TX CHECKSUM NOT ENABLED



NOTES
1. H is the "Hangover bit" (Logic 1) appended to the transmitted message before transmission is terminated.
2. Any number of preamble bytes can occur here.
3. Any number of address/data bytes can occur here.
4. Transmission terminates when no further data bytes are loaded into the TX data buffer.

A - Address bytes
C - Checksum bytes
D - Data bytes
H - Hang bit
P - Preamble bytes

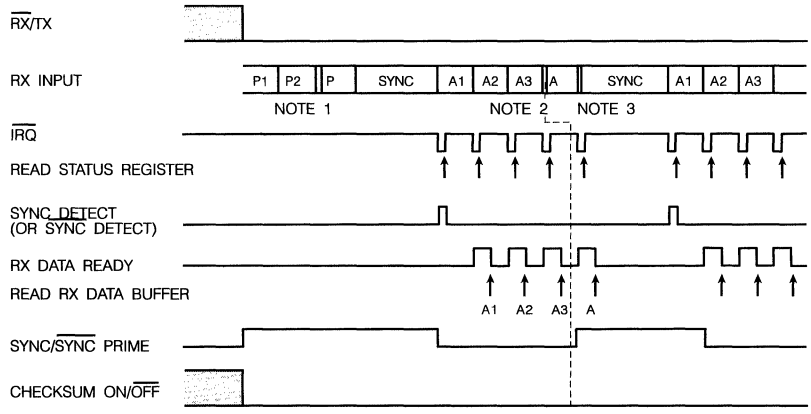
- Don't care state

TX only - In TX, Preamble and SYNC are loaded as data from the microcontroller

Figure 7 -- TX Timing

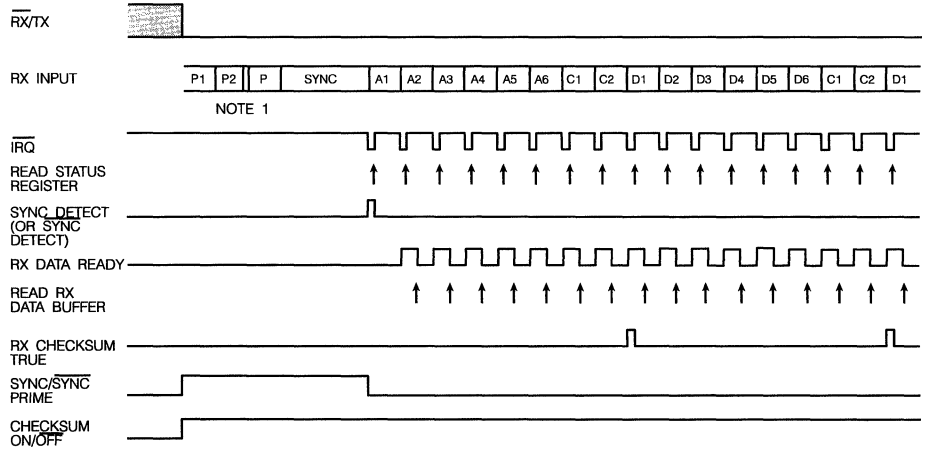
RX Timing Information

(a) RX SYNC/$\overline{\text{SYNC}}$ REQUIRED BEFORE EVERY MESSAGE, RX CHECKSUM NOT ENABLED



NOTES
1. Any number of preamble bits can occur here.
2. Any number of address/data bytes can occur here.
3. Any number of bits can occur here.
4. RX Freeformat set high.

(b) RX ADDITIONAL DATA FOLLOWS INITIAL ADDRESS (6 DATA & 2 CHECKSUM BYTES) DATA, RX CHECKSUM ENABLED



NOTES
1. Any number of preamble bits can occur here.
2. RX Freeformat set high.

A - Address bytes
C - Checksum bytes
D - Data bytes
H - Hang bit
P - Preamble bytes

- Don't care state

TX only - In TX, Preamble and SYNC are loaded as data from the microcontroller

Figure 8 - RX Timing

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin	-0.3V to (V_{DD}+0.3 V)
Sink/source current	
(supply pins)	±30mA
(other pins)	±20mA
Total device dissipation (@T_{AMB} 25°C)	800 mW max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/clock f_0 = 4.032MHz

Audio level 0dB ref = 308 mVrms @ 1kHz

Bit Rate = 1200 bps

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD})		4.5	5.0	5.5	V
Supply current (enabled)		-	5.0	-	mA
Supply current (powersave)		-	2.0	-	mA
Dynamic Values					
Digital Interface					
Input Logic "1"	1	3.5	-	-	V
Input Logic "0"	1	-	-	1.5	V
Output Logic "1" (IOH = -120µA)	2	4.6	-	-	V
Output Logic "0" (IOL = 360µA)	2,3	-	-	0.4	V
Digital Input Current					
V_{IN} = Logic "1" or "0"	1	-	-	1.0	µA
Digital Input Capacitance	1	-	-	7.5	pF
Tri-state "Off" Leakage Current	8	-4.0	-	4.0	µA
Analog Impedance					
Input Impedance		100	-	-	kΩ
Output Impedance					
Transmitting Data		-	6.0	10.0	kΩ
Not Transmitting Data		-	1.0	-	MΩ
On-Chip Xtal Oscillator					
R_{IN}		10.0	-	-	MΩ
R_{OUT}		5.0	-	15.0	kΩ
Gain		-	15.0	-	dB
Frequency	4	-	4.032	-	MHz
Receiver					
Signal Input Levels	5	-9.0	-2.0	10.5	dB
Bit Error Rate					
at 12dB SNR		-	7.0	-	10^{-4}
at 20dB SNR		-	1.0	-	10^{-8}
Synchronization at 12dB SNR	6				
Probability of Bit 8 being correct		-	99.0	-	%
Probability of Bit 16 being correct		-	99.5	-	%

Characteristics	See Note	Min.	Typ.	Max.	Unit
Transmitter					
Output Level		-	0	-	dB
Output Level Variation		-1.0	-	1.0	dB
Output Distortion		-	3.0	5.0	%
Third Harmonic Distortion		-	2.0	3.0	%
Logic "1" Frequency	7	-	1200	-	Hz
Logic "0" Frequency	7	-	1800	-	Hz
Isochronous Distortion					
1200Hz-1800Hz		-	25.0	40.0	µs
1800Hz-1200Hz		-	20.0	40.0	µs
Uncommitted Amplifier					
Bandwidth		-	200	-	kHz
Gain		-	50.0	-	dB
Input Impedance		1.0	-	-	MΩ
Output Impedance		-	-	10.0	kΩ

Notes
1. Device control pins: Serial Clock, Command Data, $\overline{\text{Wake}}$ and $\overline{\text{CS}}$.
2. Reply Data output.
3. $\overline{\text{IRQ}}$ output.
4. For baud rate specified (1200 baud).
5. Signal-to-Noise Ratio = 50dB.
6. The response time is measured using a 10101010....101 signal input pattern at 230mVrms (-2.5dB) with no noise.
7. Dependant upon Xtal tolerance.
8. $\overline{\text{IRQ}}$ and Reply Data outputs for $V_{SS} < V_{OUT} < V_{DD}$.

Checksum Generation and Checking

Generation

The checksum generator takes the 48 bits from the 6 bytes loaded into the TX Data Buffer and divides them modulo-2 by the generating polynomial:

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial 48 bits and the 15 bit remainder (with the last bit inverted). This 16 bit word is used as the "Checksum."

Checking

The checksum checker does two things:

1) It takes the first 63 bits of a received messge, inverts bit 63, and divides them modulo-2 by the generating polynomial:

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

The 15 bits remaining in the polynomial divider are checked to make sure that they are all zero.

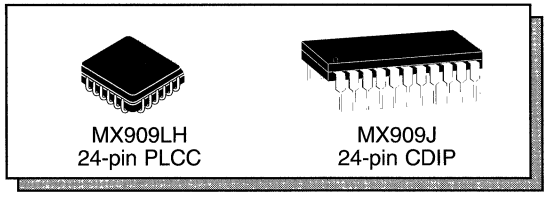
2) It generates an even parity bit from the first 63 bits of a received message and compares this bit with the received parity bit (bit 64).

If the 15 bits in the polynomial divider are all zero and the two parity bits are equal, then the RX Checksum True (Status Register bit 1) is set.

HIGH-SPEED AND MOBITEX* GMSK MODEM

Features

- **MX•COM MX'D SIGNAL CMOS**
- **MOBITEX AND GENERAL-PURPOSE PACKET DATA APPLICATIONS**
  - **WIRELESS DATA**
  - **RADIO TELEMETRY**
  - **POINT-OF-SALE & "SWIPE" TERMINALS**
  - **BAR-CODE READERS**
- **FLEXIBLE FRAME STRUCTURE** [MOBITEX & CUSTOM FRAME FORMATS]
- **HALF-DUPLEX GMSK MODEM: 4 to 19.2 kbps**
- **GMSK SIGNAL FILTERING (TX BT = 0.3)**
- **RECEIVED DATA QUALITY MONITOR**
- **AUTOMATIC PROTOCOL HANDLING** [BIT AND FRAME SYNC, BLOCK FORMATTING, CRC AND FEC, INTERLEAVING & SCRAMBLING]
- **LOW VOLTAGE OPERATION: 4.5 TO 5.5 V**
- **PCMCIA PACKAGING AVAILABLE****



Description

The MX909 single-chip half-duplex GMSK modem offers many benefits to the manufacturer and programmer of medium to high-speed radio packet-data links using Mobitex or general-purpose packet protocol.

- **Automatic handling (TX/RX) of Frame structure and Data Blocks .....** will reduce the processing load on the host µController. Requiring service by the µController only once per TX or RX Data Block, the MX909 will perform as much as possible of the computationally intensive work involved in the handling of packet-type protocol, including CRC and FEC operations, Frame Sync detection, Interleaving and Scrambling.
- **Gaussian Minimum Shift Keying (GMSK) modulation .....** provides the basis for an extremely good relationship between the RF bandwidth, Data bit-rate and Bit-error-rate.
- **Low-power, high-speed operation with powersave mode .....** selectable 4 kbps to 19.2 kbps with a typical operating current of only 4mA at 5 volts.
- **Signal acquisition and tracking .....** allows for the rapid acquisition of received signals, followed by automatic tracking of signal variations. Both PLL bandwidth and RX level measurement circuitry will react automatically as programmed.

RX and TX data and control between the host µController and the MX909 is via an 8-bit bi-directional parallel interface; input and output signals to and from the radio system are in analog form suitable for connection to the radio's discriminator and frequency modulator.

The MX909 is available in DIP and Surface Mount packages, as well as PCMCIA-compatible packaging.

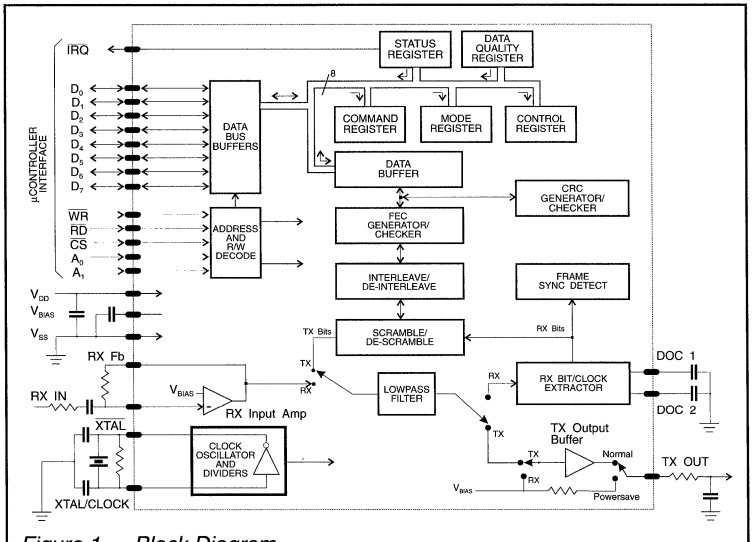


Figure 1 - Block Diagram

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*** Contact MX-COM for more information.*

Introduction: MX909 Circuit Descriptions

Data Bus Buffers

Eight bi-directional 3-state logic-level buffers between the modem's internal registers and the controlling µController's data-bus lines.

R/W, CS and Address Lines

Control the transfer of data bytes between the µController and the modem's internal registers, according to the state of the Write and Read Enable ($\overline{WR}$ and $\overline{RD}$) inputs, the Chip Select ($\overline{CS}$) input and the Register Address inputs (A_0 and A_1).

The Data Bus Buffers and Address & R/W Decode blocks provide a byte-wide parallel µController interface.

Status and Data Quality Registers

8-bit registers which the µController can read to determine the status of the modem and the received data quality.

Command, Mode and Control Registers

The values written by the µController to these 8-bit registers control the operation of the modem.

Data Buffer

An 18-byte buffer used to hold RX or TX data to or from the µController.

CRC Generator/Checker

A circuit which generates (transmit mode) or checks (receive mode) the Cyclic Redundancy Checksum bits which are included in transmitted Mobitex Data Blocks so that the receive modem can detect transmission errors.

FEC Generator/Checker

In transmit mode this circuit calculates and adds the Forward Error Correction information (4 bits) to each byte presented to it. In receive mode the FEC information is used to correct most transmission errors that may have occurred in a Mobitex Data Block or in Frame Head control bytes.

TX Output Buffer

A unity-gain amplifier used in the transmit mode to buffer the output of the TX Lowpass Filter. In receive mode, the input of this buffer is connected to V_{BIAS}. When changing from RX to TX mode the input to this buffer will be connected to V_{BIAS} for 2 bit periods to prevent unwanted signals, from the lowpass filter, appearing at the TX OUT pin.

When the modem is set to the powersave mode, the buffer is turned off and the TX Output pin connected to V_{BIAS} via a high value resistance. When exiting from powersave the TX output is only reconnected to the buffer after 2 bit times to prevent unwanted signals, from the lowpass filter, appearing at the TX OUT pin.

Interleave/De-Interleave Buffer

Interleaves data bits within a data block before transmission and de-interleaves the received data block so that the FEC system is best able to handle short noise bursts or fades.

RX Input Amp

Allows the received signal input to the modem to be set to the optimum level by suitable selection of the external components.

Frame Sync Detect

This circuit, which is only active in the receive mode, is used to look for the user-specified 16-bit Frame Synchronization pattern which is transmitted to mark the start of every frame.

Scramble/De-Scramble

This block may be used to scramble/descramble the transmitted/received Mobitex Data Block by modulating it with a 511-bit pseudo-random sequence. Scrambling smooths the transmitted spectrum especially when repetitive sequences are to be transmitted.

(TX/RX) Lowpass Filter

This filter, which is used in both transmit and receive modes, is a low-pass transitional gaussian filter.

In TX mode the filter bandwidth is set for a loss of 3dB at 0.3 times the selected bit rate (BT = 0.3) and the bits are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels.

In RX mode this filter is used with an increased BT factor (0.56) to reject HF noise so that the signal is in a suitable condition for extracting the received data.

RX Bit/Clock Extraction

These circuits, which operate only in receive mode, extract a bit-rate clock from the received signal, and measure the received signal amplitude and its dc offset.

This information is then used to extract the received bits and also to provide an input to the received Data Quality measuring circuit.

Clock Oscillator and Dividers

This circuit derives the transmit bit rate (and the nominal receive bit rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or fed from an external source.

MX909
Pin Function Table

Pin	Function
1	**$\overline{IRQ}$:** A 'wire-ORable' output for connection to the controlling µController's Interrupt Request input. This output has a low-impedance pull-down to V_{SS} when active, and is high-impedance when inactive.
2	**D_7:**
3	**D_6:**
4	**D_5:**
5	**D_4:** 8 bi-directional 3-state µController interface data lines.
6	**D_3:**
7	**D_2:**
8	**D_1:**
9	**D_0:**
10	**$\overline{RD}$:** An active-low logic level input used to control the reading of data from the modem into the controlling µController.
11	**$\overline{WR}$:** An active-low logic level input used to control the writing of data into the modem from the controlling µController.
12	**V_{SS}:** The negative supply (ground).
13	**$\overline{CS}$:** An active-low logic level input to the modem used to enable a data Read or Write operation (see Figure 24, Timing).
14	**A_0:** Two logic-level modem register selection inputs.
15	**A_1:**
16	**$\overline{Xtal}$:** The output of the on-chip Xtal oscillator.
17	**Xtal/Clock:** The input to the on-chip Xtal oscillator. Operation of the MX909 without a suitable Xtal or clock input may cause device damage.
18	**Doc 2:** Connections to the internal RX signal level measurement circuitry. Capacitors as
19	**Doc 1:** described in Figure 2 should be installed between each of these pins and V_{SS}.
20	**TX Out:** The TX signal output from the modem.
21	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$, this pin must be decoupled to V_{SS} by a capacitor mounted close to the device pins.
22	**RX In:** The input to the RX input amplifier.
23	**RX Feedback:** The output of the RX input amplifier, and the input to the (RX) Lowpass Filter.
24	**V_{DD}:** The positive supply. Levels and voltages within the modem are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the device pins.

Installation Information

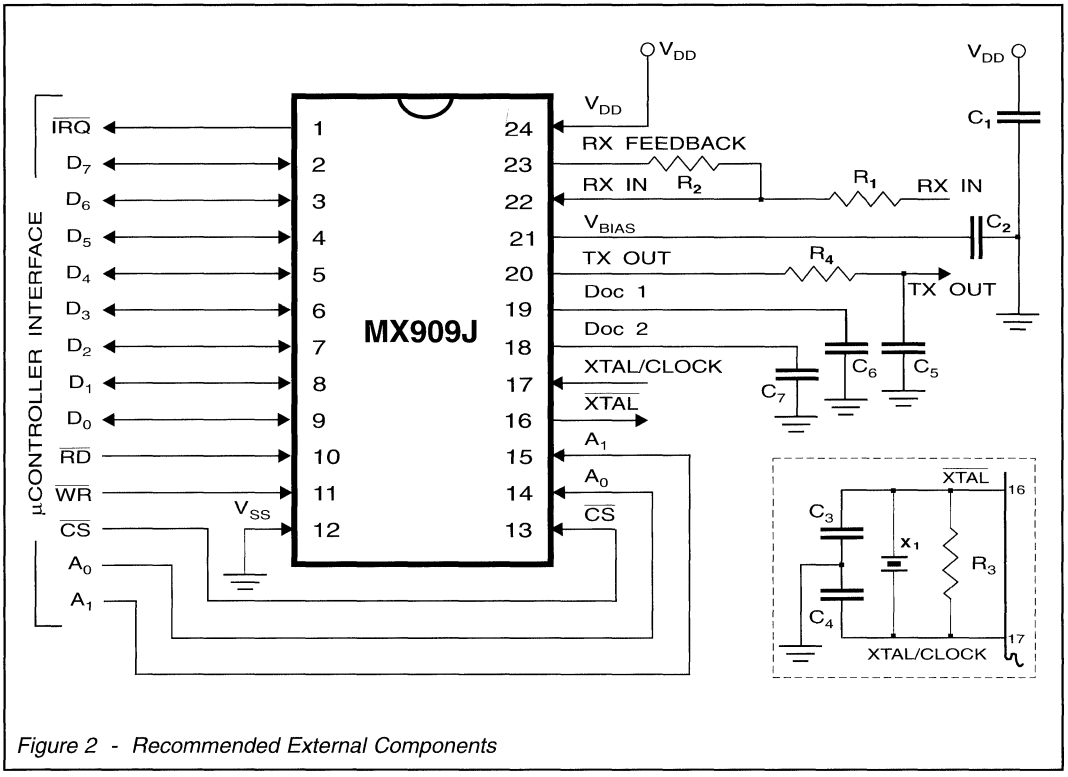


Figure 2 - Recommended External Components

Component	Value	Tolerance
R_1	Note 1	±10%
R_2	100kΩ	±10%
R_3	1.0MΩ	±20%
R_4	Note 2	±5%
C_1	0.1µF	±20%
C_2	0.1µF	±20%
C_3	Note 3	±20%
C_4	Note 3	±20%
C_5	Note 2	±10%
C_6	Note 4	±20%
C_7	Note 4	±20%
X_1	Note 5	

Installation Notes

1. Resistors R_1 and R_2, with the RX Input Amplifier, set the signal input level to the modem.
   The value of R_1 should be calculated to give 1.0v p-p at the RX Feedback pin for a received 11110000... sequence. The dc level of the received signal should be adjusted so that the signal at the modem's RX Feedback pin is centered around V_{BIAS}.

2. External components R_4 and C_5 form an RC lowpass filter between the TX Buffer output (TX OUT) and the input to the radio's frequency modulator; this is an important part of the TX signal filtering. These components may form a part of any dc level shifting and gain adjustment circuitry.
   The ground connection (V_{SS}) of C_5 should be positioned to give maximum attenuation of high frequency noise into the modulator.
   R_4 and C_5 should be chosen so that the product of R_4 (Ohms) and C_5 (Farads) is:

$$\frac{0.34}{\text{bit rate}} \text{ (bits per sec)}$$

   R_4 should be not less than 20kΩ and the value used for C_5 should take into account parasitic capacitance.

Examples	R_4	C_5
8000b/s	100kΩ	430pF
4800b/s	100kΩ	710pF

The 'eye' diagram of the transmitted signal (after the external R_4/C_5 network) is shown in Figure 4.

Continued on next page .....

Installation Information ...

3. The values used for C_3 and C_4 should be suitable for the frequency of X_1.
   As a guide:
   $C_3 = C_4 = 33pF$ for $X_1 < 5.0MHz$.
   $C_3 = C_4 = 18pF$ for $X_1 > 5.0MHz$.

4. External capacitors C_6 and C_7 form part of the received signal level measuring circuit; the values of C_6 and C_7 should satisfy the following: C (F) x Data Rate (bps) = 120 x 10^{-6}.

D/Rate(kb/s)	$C_6/C_7(\mu F)$	D/Rate(kbps)	$C_6/C(\mu F)$
4	.030	4.8	.022
8.0	.015	9.6	.012
16.0	.0068	19.2	.0068

5. If the on-chip Xtal oscillator is to be used, then the external components X_1, C_3, C_4, and R_3 are required as shown in Figure 2 (inset).

   If an external clock source is to be used these components are not required; the input should be connected to the Xtal/clock pin and the $\overline{\text{Xtal}}$ pin left unconnected.

   Table 4 (Clock/Data Rates) provides advice on the selection of the correct Xtal value.

External Signal Paths

The diagram below shows signal connections to and from the MX909. Inputs and outputs are shown with DC coupling and level-shifting components; the notes and diagrams on the following page (Figures 5 and 6) describe how, if acceptable, AC coupling may be used (see notes on the following page).

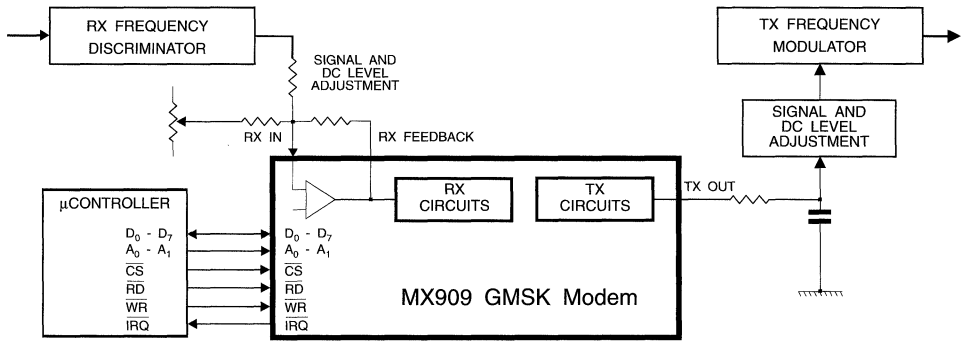


Figure 3 - External Signal Paths

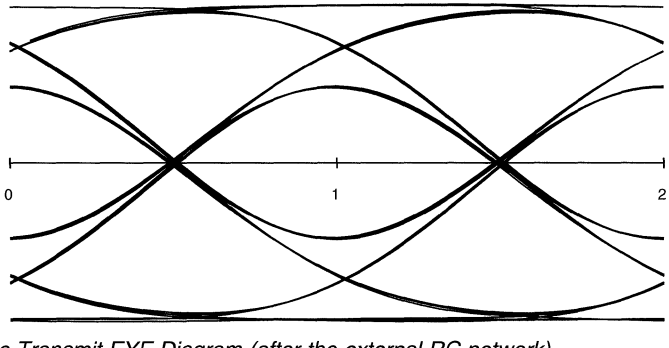


Figure 4 - Example Transmit EYE Diagram (after the external RC network)

Installation Information .....

AC Coupling

For a practical application, AC coupling from the modem's transmit output to the Frequency Modulator and from the receiver's Frequency Discriminator to the receive input of the modem may be desired. There are, however, two problems.

1) AC coupling of the signal degrades the bit-error-rate performance of the modem. Figure 5 illustrates the typical bit error rates at 8kbps (without FEC) for differing degrees of AC coupling.

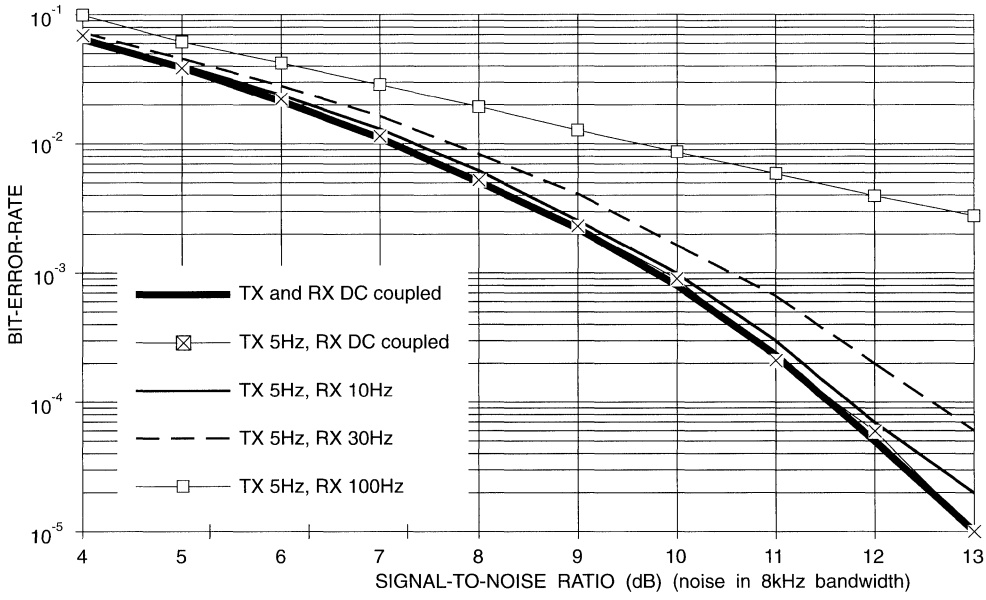


Figure 5 - Examples of BER Performance Degradation Due to Varying Degrees of AC Coupling

2) Any AC coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits. As illustrated below, the time for this voltage step to decay to 37% of its original value is:

$$T = \frac{1}{(2\Pi \times f)}$$

Where f is the 3dB cut-off frequency of the AC coupling network and is 8 ms (or 64 bit-times at 8 kbps) for a 20Hz network.

For these reasons the maximum -3dB cut-off frequencies would seem to be around 5Hz in the TX path and 20Hz in receive at 8 kbps.

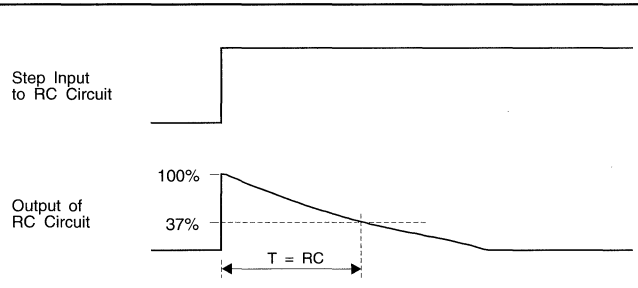


Figure 6 - Decay Problems of the AC Coupling Network

Radio Performance

The maximum data rate that can be transmitted over a radio channel using this modem depends on:

- RF channel spacing.
- Allowable adjacent channel interference.
- Bit rate.
- Peak carrier deviation (modulation index).
- TX and RX reference oscillator accuracies.
- Modulator and demodulator linearity.
- Receiver IF filter frequency and phase characteristics.
- Use of error correction techniques.
- Acceptable error rate.

As a guide, 8 kbps can be achieved - subject to local regulatory requirements - over a system with 12.5kHz channel spacing if the transmitter frequency deviation is set to ± 2kHz peak for a repetitive ' 1100... ' pattern and the maximum difference between transmitter and receiver 'carrier' frequencies is less than 1500Hz.

The modulation scheme employed by this modem is designed to achieve high data throughput by exploiting as much as possible of the RF channel bandwidth. This does, however, place constraints on the performance of the radio.

In particular, attention must be paid to:

- Linearity, frequency and phase response of the TX Frequency Modulator.
- The bandwidth and phase response of the receiver's IF filters.
- Accuracy of the TX and RX reference oscillators, as any difference will shift the received signal towards the skirts of the IF filter response and cause a DC offset at the discriminator output.

Viewing the received signal eye (at the MX909 RX Feedback pin) gives a good indication of the overall transmitter/receiver performance.

Modem to µController Interface

The Data Bus Buffers and Address and Read/Write Decode blocks form a byte-wide parallel µController interface. This diagram shows how this function can be memory mapped.

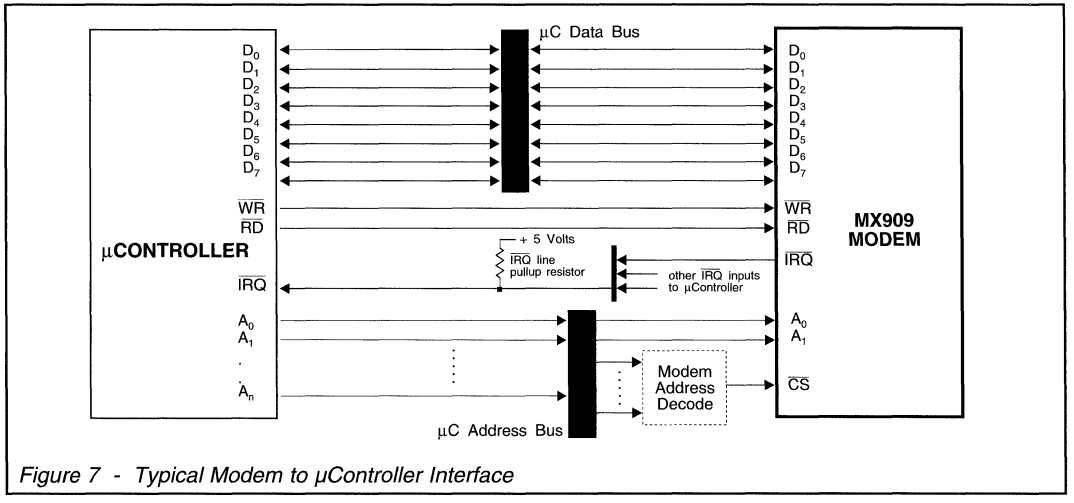


Figure 7 - Typical Modem to µController Interface

Installation Information .....

Baseband and RF Frequency Requirements

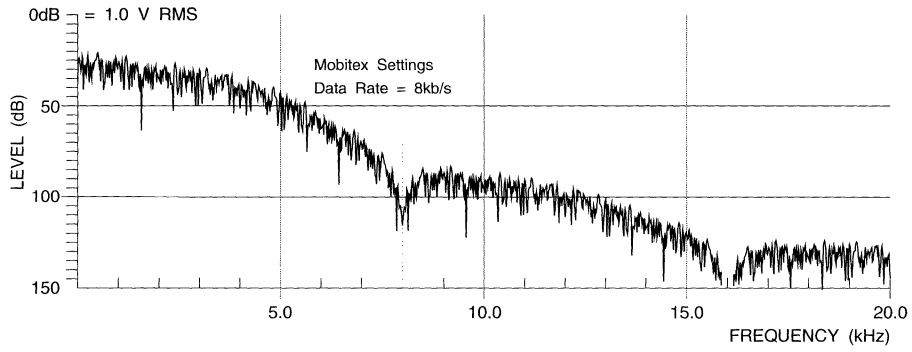


Figure 8 - Typical TX Out Frequency Spectrum for a Random Data Input

RF Channel Occupancy

The diagram below shows the theoretical RF bandwidth requirements when interfacing the MX909 baseband (TX OUT) signal (Figure 8, above) to a radio transmitter. This plot assumes a perfect frequency modulator.

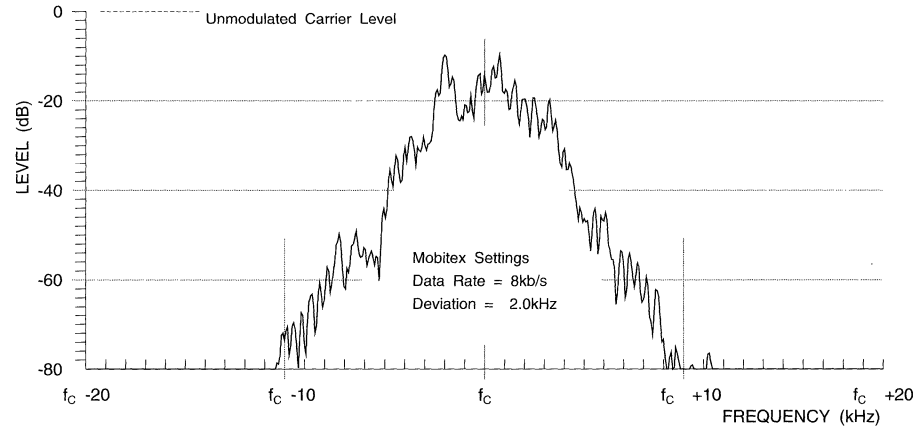


Figure 9 - Theoretical TX RF Frequency Spectrum Resulting from a Random Data Input to the MX909

Data Formats

Mobitex Frame and Data Structures

The Mobitex format for transmitted data is in the form of a Frame Head immediately followed by a number of Data Blocks (0 to 32).

The Frame Head consists of 7 bytes .....

2 bytes of Bit Sync:
1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 – from base, or
0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 – from mobile
(sent L to R).

2 bytes of Frame Sync:
System specific.

2 bytes of Control Data:
– System specific ID and control information.

1 byte of FEC Code (generated by the MX909):
– 4 bits for each of the control bytes:
– bits 7 - 4 operate on the first control byte.
– bits 3 - 0 operate on the second control byte.

Each byte in the Frame Head is transmitted bit 7 (MSB) first, bit 0 (LSB) last.

The Data Block consists of .....

18 bytes of Data:
2 bytes of CRC are calculated by the MX909 from the 18 Data Bytes.
4 bits of FEC code are calculated for each of the Data and CRC bytes

The resulting 240 bits are interleaved and scrambled before transmission; see Figure 22, (Interleaving).

Figure 10 shows how the over-air signal is built up from Frame Sync and Bit Sync patterns, Control Bytes and Data Blocks.

The binary data transferred between the modem and the controlling µController is that shown enclosed in the heavily outlined rectangles.

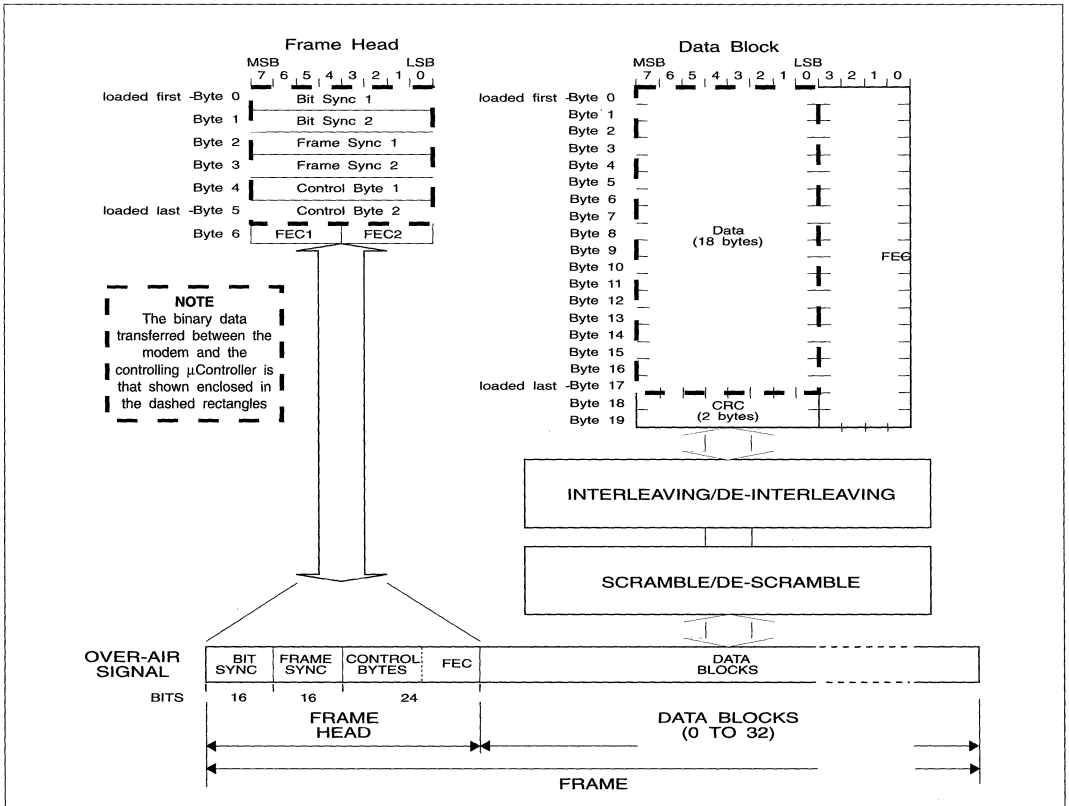


Figure 10 - MX909 Mobitex System Data Format

Programming Information .....

Modem/µController Interaction

In general, data is transmitted over-air in the form of messages, or 'Frames', consisting of a 'Frame Head' optionally followed by one or more formatted Data Blocks.

The Frame Head includes a Frame Synchronization pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (cyclic redundancy checksum) generation, Forward Error Correction (FEC) coding, Interleaving and Scrambling.

To reduce the processing load on the host µController, the MX909 has been designed to perform as much as possible of the computationally intensive work involved in Frame formatting and de-formatting and, when in receive mode, in searching for and synchronizing onto the Frame Head.

In normal operation the modem will only require servicing by the µController once per received or transmitted data block. Thus, to transmit a block, the controlling µController has only to load the unformatted (raw) binary data into the modem's data buffer then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result with FEC coding, interleave then scramble the bits before transmission.

In receive mode, the MX909 modem can be instructed to assemble a block's worth of received bits, de-scramble and de-interleave the bits, check and correct (using the FEC coding) and check the resulting CRC before placing the received binary data into the Data Buffer for the µController to read. The MX909 modem can also handle the transmission and reception of un-formatted data; to allow for example, the transmission of special Bit and Frame Synchronization sequences or test patterns.

1

Register Selection

The MX909 modem appears to the programmer as 4 write-only 8-bit registers shadowed by 3 read-only registers. Individual registers are selected by the A_1 and A_0 inputs; see Read and Write cycle timing diagrams (Figure 24).

Table 1 - Register Selection

A_1	A_0	Write to Modem	Read from Modem
0	0	Data Buffer	Data Buffer
0	1	Command Register	Status Register
1	0	Control Register	DQ Register
1	1	Mode Register	not used

Data Buffer

An 18-byte read/write buffer which is used to transfer data (as opposed to Command, Status, Mode, Data-Quality and Control information) between the modem and the controlling µController.

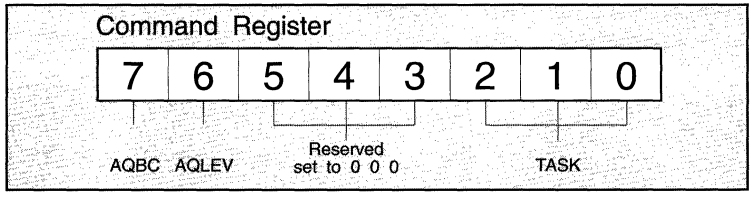
The Data Buffer appears to the µController as a single 8-bit register; the modem ensures that sequential µController 'read' or 'write' actions to the buffer are routed to the correct locations within this buffer.

The µController should only access this buffer when the Status Register BFREE (Buffer Free) bit is at a logic '1'. The buffer should only be written to while in the TX mode and read from in the RX mode (except when loading Frame Sync detection bytes in the RX mode). See Figure 24 for data Read/Write Timing information.

Command Register

Writing to this register instructs the modem to perform a specific action or actions, depending upon the setting of the TASK, AQLEV, and AQBC bits (see Figure 11/Table 1).

Figure 11 - The Command Register



When it has no action to perform (but is not powersaved), the modem will be in an idle state, and if it is in the TX mode the input to the TX (Lowpass) Filter will be connected to V_{BIAS}.

When it has no action to perform in the RX mode the modem will continue to measure the received data quality and extract bits from the received signal, feeding them into the De-Interleave Buffer, but will otherwise ignore the received data.

Command Register

B7
AQBC

Acquire Bit Clock: This bit has no effect in the TX mode.

In the RX mode, whenever a byte with the AQBC bit set to logic '1' is written to the Command Register, it initiates an automatic sequence designed to achieve bit-timing synchronization with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received bit-timing extraction circuits to their widest bandwidth, then gradually reducing the bandwidth as timing synchronization is achieved, until it reaches the 'normal' value set by the PLLBW bits of the Control Register.

Setting this bit to logic '0' (or changing it from '1' to '0') has no effect. Note that the acquisition sequence will be re-started every time that a byte written to the Command Register has the AQBC bit set to logic '1'.

The AQBC bit will normally be set at the same time as an SFS (Search for Frame Sync) or SFH (Search for Frame Head) task, however it may also be used independently to re-establish clock synchronization quickly after a long fade. Alternatively, an SFS or SFH task may be written to the Command Register with the AQBC bit at logic '0' if it is known that clock synchronization does not need to be re-established.

More details of the Bit Clock Extraction Sequence are given in the Operational Information section of this Data Sheet

B6
AQLEV

Acquire Receive Signal Levels: This bit has no effect in the TX mode.

In receive mode, whenever a byte with the AQLEV bit set to a logic '1' is written to the Command Register, it initiates an automatic sequence designed to measure the amplitude and DC offset of the received signal as rapidly as possible. This sequence involves setting the measurement circuits to respond quickly at first, then gradually increasing their response time -improving the measurement accuracy- until the 'normal' value set by the LEVRES bits of the Control Register is reached. See Figure 12.

Setting this bit to a logic '0' (or changing it from '1' to '0') has no effect; note that the acquisition sequence will be re-started every time that a byte written to the Command Register has the AQLEV bit set to a logic '1'.

The AQLEV bit will normally be set at the same time as an SFS (Search for Frame Sync) or SFH (Search for Frame Head) task is initiated, however it may also be used independently to re-establish signal levels quickly after a long fade. Alternatively, a SFS or SFH task may be written to the Command Register with the AQLEV bit at logic '0' if it is known that there is no need to re-establish the received signal levels. Refer to the Clock Extraction (Operational Information section) notes.

B5
B4
B3

These bits should each be set to a logic '0'.

B2
B1
B0
TASK

Task: Operations such as transmitting a data block are treated by the modem as 'tasks'. Information on Task functions is given on the following pages. A task is initiated when the µController writes a byte to the Command Register with the Task bits set to anything other than the 'NULL' ('0' '0' '0') code.

The µController should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer if the BFREE (Buffer Free) bit of the Status Register is a logic '0'.

Different tasks apply in receive and transmit modes.

TX Mode: All tasks other than NULL, RESET and TSO instruct the modem to transmit data from the Data Buffer, formatting it as required. For these tasks the µController should wait until the BFREE (Buffer Free) bit of the Status Register is a logic '1', before writing the data to the Data Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Buffer, byte number '0' of the block should be written first.

Once the byte containing the desired task has been written to the Command Register, the modem will: Set the BFREE (Buffer Free) bit of the Status Register to a logic '0', take the data from the Data Buffer as quickly as it can -transferring it to the Interleave Buffer for eventual transmission.

Programming Information .....

Command Register .....

B2
B1
B0
TASK .....

Task: ..... This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer. Once all of the data has been transferred from the Data Buffer the modem will set the BFREE and IRQ bits of the Status Register to a logic '1', (causing the $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to a logic '1') to tell the µController that it may write new data and the next task to the modem.

In this way the µController can write a task -and the associated data- to the modem while the modem is still transmitting the data from the previous task.

RX Mode: The µController should wait until the BFREE bit of the Status Register is a logic '1', then write the desired task to the Command Register. Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE bit of the Status Register to a logic '0'.

Wait until enough received bits are in the De-Interleave Buffer.

Decode them as needed, and transfer any resulting data to the Data Buffer.

Then the modem will set the BFREE and IRQ bits of the Status Register to logic '1', (causing the $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to a logic '1') to tell the µController that it may read from the Data Buffer and write the next task to the modem. If more than 1 byte is contained in the Data Buffer, byte number '0' of the data will be read first.

In this way the µController can read data and write a new task to the modem while the received bits needed for this new task are being stored in the De-Interleave Buffer. The above is not true for loading the Frame Sync detection bytes (LFSB); the bytes to be compared with the incoming data must be loaded prior to the task bits being written. Detailed timings for the various tasks are given in later sections.

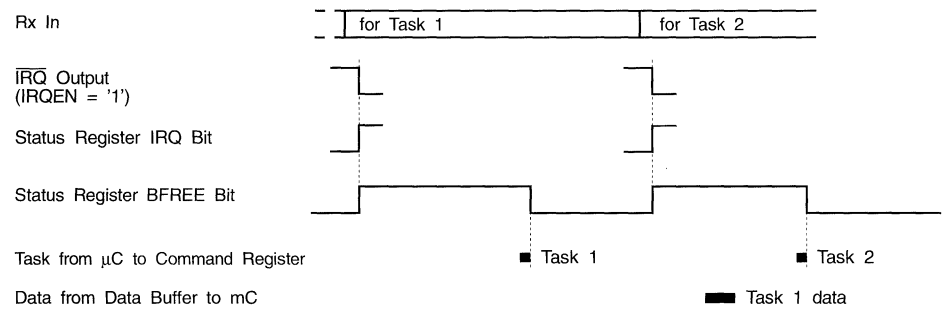


Figure 12 - The Receive Process

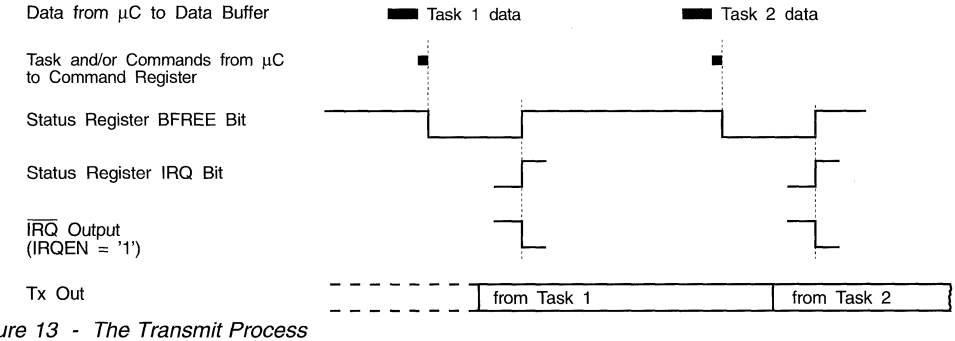


Figure 13 - The Transmit Process

Programming Information .....

Modem Tasks in Detail

The following describes the setting and format of the Command Register 'task' bits (bits 2, 1 and 0). Note that before a task is programmed the TX/RX bit in the Mode Register must be set to the required level.

Command Bits 2	1	0	Receive Mode		Transmit Mode	
0	0	0	NULL		NULL	
0	0	1	SFH	Search for Frame Head	T7H	Transmit 7 Byte Frame Head
0	1	0	R3H	Read 3 Byte Frame Head	Reserved	.. ..
0	1	1	RDB	Read Data Block	TDB	Transmit Data Block
1	0	0	SFS	Search for Frame-Sync	TQB	Transmit 4 Bytes
1	0	1	RSB	Read Single Byte	TSB	Transmit Single Byte
1	1	0	LFSB	Load Frame-Sync Bytes	TSO	Transmit Scrambler Output
1	1	1	RESET	Cancel any Current Action	RESET	Cancel any Current Action

Table 2 Modem Task Allocations

Modem Tasks

NULL **No Effect.** This task is provided so that an AQBC or AQLEV (Command Register) command can be initiated without loading a new task.

SFH **Search for Frame Head.** Causes the modem to search the received signal for a valid Mobitex Frame Head. The Frame Head will consist of a 16-bit Frame Sync followed by control data which has no uncorrectable errors (see Figure 10, Data Format). The search will continue until a valid Frame Head has been found, or until the RESET task is loaded. The search is carried out by the modem in 3 stages:

1. Attempt to match the incoming bits against the previously programmed (task LFSB) 16-bit Frame Sync pattern (allowing up to any one bit (of 16) in error).
2. When a match has been found, the modem will read the next 3 received bytes as Frame Head bytes; these bytes will be checked using the FEC bits. If the FEC indicates uncorrectable errors (Status Register) the modem will resume the search, looking for a new Frame Sync pattern.
3. If the received bytes are error free or correctable, BFREE and IRQ bits (Status Register) are set to a logic '1' and the CRCFEC bit set to a logic '0'; the two corrected (by the modem) Frame Head Control Data bytes are then placed into the Data Buffer. The MOBAN bit (Mobile or Base) in the Status Register will be set according to the polarity of the 3 bits that preceded the Frame Sync pattern.

On detecting that the BFREE bit of the Status Register has gone to a logic '1', the µController should read the 2 Frame Head control data bytes from the Data Buffer and then write the next task to the modem's Command Register.

R3H **Read 3 Byte Frame Head.** This task, which would normally follow an SFS task, will cause the modem to place the next 3 bytes directly into the Data Buffer and, concurrently, check those 3 bytes as Frame Head Control Data bytes; the modem will set the CRCFEC bit to a logic '1' (high) if errors are detected. Note: This task will not correct any errors. The BFREE and IRQ bits of the Status Register will be set to a logic '1' when the task is complete; this is to indicate that the µController may read the data from the Data Buffer and write the next task to the Command Register. The CRCFEC bit in the Status Register will be set according to the validity of the received FEC bits.

RDB **Read Data Block.** Causes the modem to read the next 240 bits (see Data Formats -Mobitex Frame and Data Structures) as a Mobitex data block. This task will de-scramble and de-interleave the received bits, FEC correct and CRC check the resulting 18 data bytes placing them in the Data Buffer. When the task is complete the BFREE and IRQ bits of the Status Register are set to a logic '1' to indicate that the µController may read the data from the Data Buffer and write the next task to the Command Register. The CRCFEC bit in the Status Register will be set according to the outcome of the CRC check. Note that in the receive mode the checksum circuits are initialized (ready for operation) on completion of any task other than NULL.

Programming Information .....

Modem Tasks .....

SFS — **Search for Frame Sync.** Intended for special test and monitoring purposes, this task performs the first part only of an SFH task. It causes the modem to search the received signal for a 16-bit sequence which matches the previously programmed Frame Sync pattern (allowing up to any one bit (in 16) in error). When a match is found the modem will set the BFREE and IRQ bits of the Status Register to a logic '1' and update the MOBAN bit. The µController may then write the next task to the Command Register.

RSB — **Read Single Byte.** This task, which is intended for special tests and channel monitoring - perhaps preceded by an SFS task, causes the modem to read the next 8 bits and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Buffer (B7 will represent the earliest bit received). The BFREE and IRQ bits of the Status Register will then be set to a logic '1' to indicate that the µController may read the data byte from the Data Buffer and write the next task to the Command Register.

LFSB — **Load Frame Sync Bytes.** This task is unlike other RX tasks in that the Data Buffer must be loaded (with the 2 Frame Sync bytes) before the task is issued and the task must only be issued 'between' received messages; i.e. before the first task for receiving a message and after the last data is read out of the Data Buffer. It takes 2 bytes from the Data Buffer and loads them into the MX909's internal Frame Sync pattern store. The MSB of byte 0 represents the first bit of a received Frame Sync pattern and the LSB of byte 1 is compared to the last bit of a received Frame Sync pattern that will be looked for when a SFS or SFH task is executing. The LFSB task itself does not initiate a search for a received Frame Sync pattern.

Once the modem has read the Frame Sync bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating that the µController may write the next task to the modem.

T7H — **Transmit 7-Byte Frame Head.** Takes 6 bytes of data from the Data Buffer, calculates and appends 8 bits of FEC from bytes 4 and 5 then transmits the result as a complete Mobitex Frame Head. Bytes 0 and 1 form the bit -sync pattern, bytes 2 and 3 form the frame-sync pattern and bytes 4 and 5 are the Frame Head control bytes. Bit 7 of byte 0 of the Data Buffer is sent first and bit 0 of the FEC byte last.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating that the µController may write the next task and its data to the modem.

TQB — **Transmit 4 Bytes.** Takes 4 bytes of data from the Data Buffer and transmits them, bit 7 of byte 0 first, bit 0 of byte 3 last.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating that the µController may write the next task and its data to the modem.

TDB — **Transmit Data Block.** Takes 18 bytes of data from the Data Buffer, calculates and applies a 16-bit CRC and forms the FEC for the 18 data bytes and the CRC; the resulting 240 bits are then interleaved and passed through the scrambler, if enabled, before being transmitted as a Mobitex Data Block. Note that in transmit mode the CRC checksum circuit is initialized on completion of any task other than NULL.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating that the µController may write the next task data to the modem.

TSO — **Transmit Scrambler Output.** Intended for channel set-up, this task enables the scrambler and transmits its output (which will be 9-bit pseudo-random). When the modem has started this task the Status Register bits will not be changed and hence an IRQ will not be raised. The µController may write data and the next task to the modem at any time and the scrambler output will stop when the new task has produced its first data. See Mode Register SCREN.

Modem Tasks	
RESET	**Stop any Current Action.** This 'task' takes effect immediately, and terminates any current action (Task, AQBC or AQLEV) the modem may be performing and sets the BFREE bit of the Status Register to a logic '1', without setting the IRQ bit. RESET should be used when V_{DD} is applied to set the modem into a known state. Note that due to delays in the TX Lowpass Filter filter, it will take approximately 2 bit-times for any change to become apparent at the TX Out pin.
TSB	**Transmit Single Byte.** Takes a byte from the Data Buffer and transmits the 8 bits, bit 7 first. Once the modem has read the data byte from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating to the µController that it may write the next task and its data to the modem.

1

Lowpass Filter Delay

The Task Timing figures detailed in Table 2 are based upon: the signal at the input to the TX lowpass Filter in the transmit mode, or the signal at the input to the de-interleave circuits in the receive mode. As can be seen from the diagram in Figure 14, there is an additional delay of approximately 2 (two) bit-times in both TX and RX modes due to the (TX/RX) Lowpass Filter.

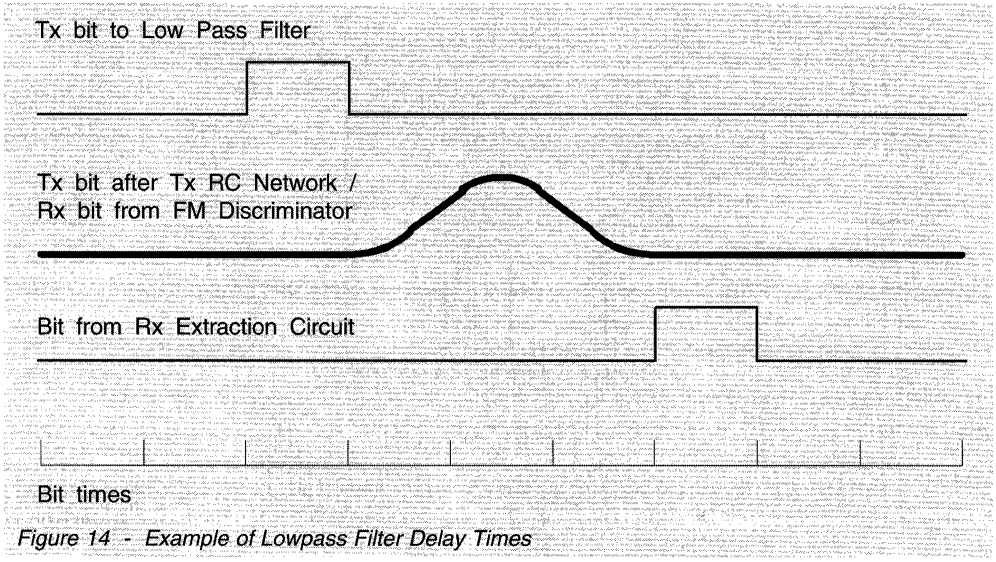


Figure 14 - Example of Lowpass Filter Delay Times

Programming Information .....

Transmit and Receive Task Timing

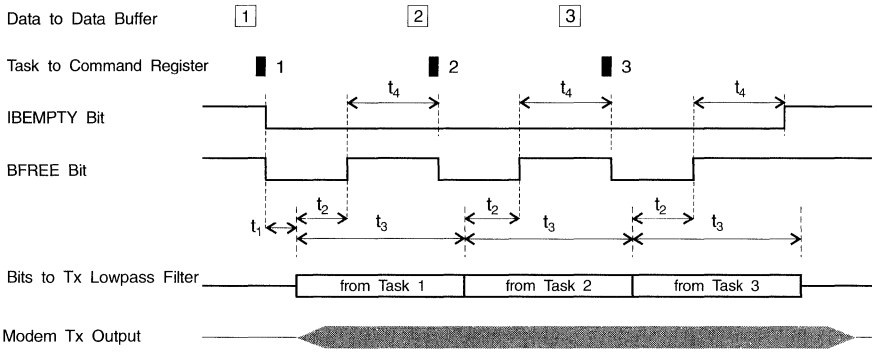


Figure 15 - TX Task Timing Diagram

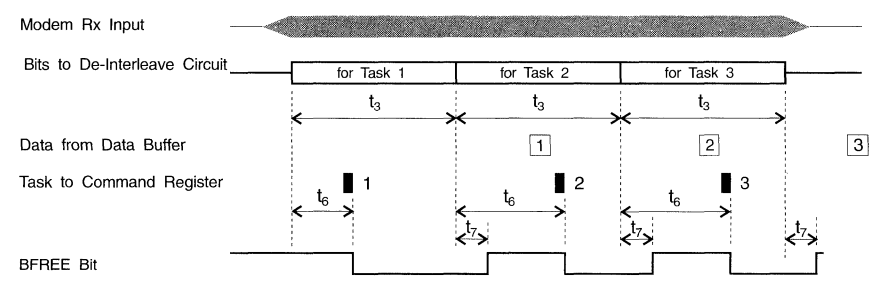


Figure 16 - RX Task Timing Diagram

Timing	Notes	Task	Typical (Bit) Time
t_1	Modem in idle state. Time from writing first task to the application of the first TX bit to the TX Lowpass Filter.	Any	1
t_2	Time from the application of the first bit of the task to the TX Lowpass Filter until BFREE goes to a logic '1' (high).	T7H TQB TDB TSB	36 24 20 1
t_3	Time to transmit all bits of the task. or Time to receive all bits of the task	T7H/SFH TQB R3H TDB/RDB TSB/RSB	56 32 24 240 8
t_4	Maximum time allowed from BFREE going to a logic '1' for the next task (and data) to be written to the modem.	T7H TQB TDB TSB	18 6 218 6
t_6	Maximum time between the first bit of the task entering the de-interleave circuit and the task being written to the modem.	SFH R3H RDB RSB	14 18 218 6
t_7	Time from last bit for task entering the de-interleave circuit to BFREE going to a logic '1'.	Any	1

Table 3 - Typical RX/TX Task Load Timings

Programming Information .....

Control Register

This 8-bit write-only register controls the modem's bit-rate, response times of the receive clock extraction and signal level measurement circuits and the internal analog filters.

Figure 17 - The Control Register

1

Control Register

B7, B6 CKDIV

Table 4 shows how bit-rates of 4000/8000/16000 or 4800/9600/19200 bits per second may be obtained from common Xtal/clock frequencies. The values of C_3 and C_4 should be suitable for the frequency of the Xtal X_1.
For X_1 < 5.0MHz, $C_3 = C_4$ = 33.0pF; for X_1 > 5.0MHz, $C_3 = C_4$ = 18.0pF .

Clock Division Ratio: These bits, together with the HI/LO bit, control a frequency divider driven from the Xtal/clock signal; this ratio and signal input will determine the nominal bit-rate.

B5 HI/LO

High or Low Xtal Range Selection: see Table 4 below.

		B5		Xtal/Clock Frequency (MHz)					
		'1'	High	8.192	9.8304	4.096 (12.288/3)	4.9152	2.048 (6.144/3)	2.4576 (12.288/5)
		'0'	Low	4.096 (12.288/3)	4.9152	2.048 (6.144/3)	2.4576 (12.288/5)	1.024	1.2288
B7	**B6**	**Division Ratio: Xtal/Clock Data Rate**		**Data Rate (bits per second)**					
0	0	256	128			16000	19200	8000	9600
0	1	512	256	16000	19200	8000	9600	4000	4800
1	0	1024	512	8000	9600	4000	4800		
1	1	2048	1024	4000	4800				

Table 4 - Clock/Data Rates

***Note** that device operation is not guaranteed or specified above 19.2 kbps or below 4 kbps*

B4 DARA

Data Rate: Employed in both RX and TX, this bit optimizes the modem's internal signal filtering circuitry to the relevant bit-rate.
For bit-rates above 10 kbps this bit (B4) should be set to a logic '1', for bit-rates at or below 10kbps set to a logic '0'.

B3, B2 LEVRES

Level Measurement Response Time: These bits are only used in the RX mode and have no effect in the TX mode; they set the 'normal' response time of the RX signal amplitude and DC offset measuring circuits. This setting will be temporarily overriden by the automatic sequence of an AQLEV command. See Table 5.
For Mobitex systems, and most general-purpose applications using this modem, these bits should be set to 'Peak Averaging', except when the µController detects a receive signal fade, when 'Hold' should be selected.

Programming Information .....

Control Register.....

B3, B2 ..... LEVRES

LEVRES .....: The 'Lossy Peak Detect' setting is intended for systems where the µController cannot detect signal fades or the start of a received message; this setting allows the modem to respond quickly to fresh messages and recover rapidly after a fade without µController intervention -this however will be at the cost of reduced Bit-Error-Rate vs Signal-to-Noise performance.

Note that as the measured levels are stored on capacitors C_6 and C_7 via pins Doc 1 and Doc 2, these levels will decay gradually towards V_{BIAS} when the 'Hold' setting is used; the discharge time-constant is approximately 2000 bit-times. Table 4 details bit-setting application.

B3	B2	Setting	Action
0	0	Hold	Keep current values of amplitude and offset
0	1	Peak Averaging	Track input signal using bit peak averaging
1	0	Peak Detect	Track input signal using peak detection
1	1	Lossy Peak Detect	Track input signal using lossy peak detection

Table 5

B1, B0 PLLBW

PLL Bandwidth: For use in the RX mode only (no effect in TX).
In the receive mode these two bits set the 'normal' bandwidth of the RX Clock Extraction phase locked loop circuit to allow for RX and TX Xtal tolerances. This setting will be temporarily overridden by the automatic sequence of an AQBC (Command Register Bit 7) command.

B1	B0	PLL Bandwidth (±ppm)	Note
0	0	0 (Hold)	For use during signal fades
0	1	30	
1	0	250	
1	1	50,000	

Table 6

The minimum bandwidth consistent with the RX and TX modem bit-rate tolerances should be chosen; e.g. if the Xtals used with both modems have accuracies of ±100ppm, the PLLBW bits (B1, B0) should be set to '1', '0'.
The very wide bandwidth ('1', '1') is intended for systems where the µController cannot detect signal fades or the start of a receive message; it allows the modem to respond rapidly to fresh messages and recover rapidly after a fade without µController intervention. This action however is at the expense of reduced Bit-Error-Rate vs Signal-to-Noise performance.
Note that PLL bandwidth figures are intended for 'a reasonably random received signal.'

LEVRES and PLLBW Operational Notes

Any new setting written to the Control Register will be implemented immediately regardless of any acquisition sequence; any acquisition sequence in progress will be cancelled.
e.g. Changing B1 or B0 will set the PLL to the new setting and cancel an AQBC sequence if running. The AQLEV sequence, if running, will continue as normal (and vice versa).
Thus if an acquisition sequence is to be started using different 'normal' settings, then the new settings must be written before triggering the acquisition sequence.

See the Operational Information section of this Data Bulletin for further details.

Programming Information .....

Mode Register

This 8-bit write-only register controls the basic operating modes of the modem.

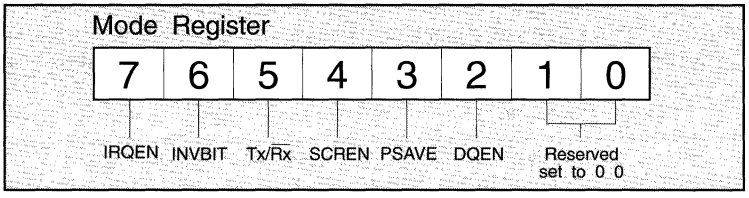


Figure 18 - The Mode Register

Mode Register

B7 IRQEN

IRQ Output Enable: When set to a logic '1' the Interrupt Request output will be pulled low (to V_{SS}) whenever the IRQ bit (BIT 7) of the Status Register is set by the modem to a logic '1'. When set to a logic '0' the Interrupt Request output will not function and will remain in its high-impedance state (see Pin Functions and Figure 7 - µController Interface).

B6 INVBIT

Invert Bits: When set to a logic '1', all data (sense) voltages to and from the modem's RX and TX paths are inverted.

For example:

B6	TX/RX Logic '1'	TX/RX Logic '0'
'0'	High (above V_{BIAS})	Low (below V_{BIAS})
'1'	Low (below V_{BIAS})	High (above V_{BIAS})

Data will be affected immediately after B6 is set and so this bit should not be changed whilst the modem is decoding or transmitting data. This bit only operates on data bits, there is no effect upon functional logic inputs.

B5 TX/RX

TX/$\overline{RX}$ Mode: When set to a logic '1' places the modem in the Transmit mode; when set to a logic '0' places the modem in the Receive mode. To allow the lowpass filter to stabilize, when changing from RX to TX there must be a 2 bit pause before setting a new task. Note that changing between Transmit and Receive modes will cancel any current task.

B4 SCREN

Scramble Enable: Setting this bit to a logic '1' enables data scrambling; setting it to a logic '0' disables scrambling. The scrambler only takes effect during the transmission or reception of a Mobitex Data Block (see Figure 10 -System Data Format) and during TSO (Transmit Scrambler Output) task. The scrambler is only operative if enabled by B4, during TSO, RDB or TDB (see Modem Tasks), it is held in the reset state at all other times. This bit should not be changed while the modem is decoding or transmitting a Mobitex Data Block.

B3 PSAVE

Powersave: When set to a logic '1' this bit places the modem in its Powersave mode. In this mode the following circuits only are disabled: Internal Filters, RX Level and Clock Extraction Circuits and the TX Output Buffer; the TX Out pin is connected to V_{BIAS} through a high-value resistance. Xtal oscillator circuits and the µController Interface logic continue to operate. When set to a logic '0' restores power to all of the device circuitry and the modem is in its operational mode. Note that the internal filters will take about 2 bit-times to settle after this bit is taken from a logic '1' to '0'. Note that RX-bit and levels will be lost if the Powersave mode is selected.

B2 DQEN

Data Quality IRQ Enable: For use in the RX mode only (no effect in TX).
In the RX mode, setting this bit to a logic '1' causes the IRQ bit (of the Status Register) to be set to a logic '1' whenever a new Data Quality reading is ready; the DQRDY bit of the Status Register will also be set to a logic '1' at the same time.

B1, B0

These bits should be set to a logic '0'.

Programming Information .....

Status Register

This register may be read by the µController to determine the current state of the modem.

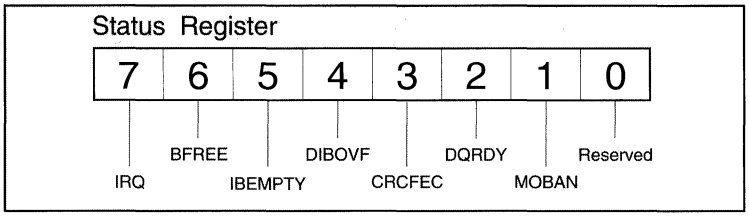


Figure 19 - The Status Register

Status Register

B7 IRQ

Interrupt Request: This bit is set to a logic '1' by:

The Status Register BFREE bit going from a logic '0' to '1', unless this transition is caused by a RESET Task or by a change to the Mode Register's PSAVE or TX/RX bits.

or

The Status Register IBEMPTY bit going from a logic '0' to '1', unless this transition is caused by a RESET Task or by a change to the Mode Register's PSAVE or TX/RX bits.

or

The Status Register DQRDY bit going from a logic '0' to '1' (if DQEN = '1').

or

The Status Register DIBOVF bit going from a logic '0' to '1'.

This (IRQ) bit is cleared to a logic '0' immediately after a read of the Status Register. If the IRQEN bit of the Mode Register is a logic '1', the MX909 $\overline{IRQ}$ output pin will be pulled low (to V_{SS}) whenever the Status Register IRQ bit is a logic '1'.

B6 BFREE

Data Buffer Free: BFREE reflects the availability of the Data Buffer; BFREE is cleared to a logic '0' *(Buffer NOT Free)* whenever a task other than NULL, RESET or TSO is written to the Command Register.
In Transmit mode, the BFREE bit will be set to a logic '1' (setting the Status Register IRQ bit to a logic '1) when the modem is ready for the µController to write new data to the Data Buffer and the next task to the Command Register.
In Receive mode, the BFREE bit is set to a logic '1' (setting the Status Register IRQ bit to a logic '1) when it has completed a task and any data associated with that task has been placed into the Data Buffer. The µController may then read that data and write the next task to the Command Register.
The BFREE bit is also set to a logic '1' -but without setting the IRQ bit- by a RESET task or when the Mode Register PSAVE or TX/RX bits are changed.

B5 IBEMPTY

Interleave Buffer Empty: In Transmit mode, IBEMPTY is set to a logic '1' (also setting the IRQ bit) when less than two bits remain in the Interleave Buffer. Any transmit task written to the modem after IBEMPTY goes to a logic '1' will be too late to avoid a gap in the transmit output signal (see Figure 15 and Table 3, TX Task Timing)
IBEMPTY is also set to a logic '1' by a RESET task and by a change of the Mode Register PSAVE or TX/RX bits, but in these cases the IRQ bit will not be set.
IBEMPTY is cleared to a logic '0' by writing a task other than NULL, RESET or TSO to the Command Register.
Note that when the modem is in the transmit mode and the Interleave Buffer is empty, a mid-level (V_{BIAS}) voltage will be fed to the TX Lowpass Filter.
In Receive mode this bit is a logic '0'.

Status Register .....

B4 DIBOVF

De-Interleave Buffer Overflow: In Receive mode DIBOVF is set to a logic '1' (also setting the IRQ bit) when a task is written to the Command Register too late to allow continuous reception (see Figure 16 and Table 3, RX Task Timing).

DIBVOF is cleared to a logic '0' by reading the Status Register, by writing a RESET task to the Command Register or by changing the PSAVE or TX/RX bits of the Mode Register.
In Transmit mode this bit is a logic '0'.

B3 CRCFEC

CRC or FEC Error: In Receive mode CRCFEC will be updated at the end of a Mobitex Data Block task, after checking the CRC, and at the end of receiving Frame Head control bytes, after checking the FEC.

A logic '0' indicates that the CRC was received correctly or that the FEC found no uncorrectable errors. A logic '1' indicates that errors are present. CRCFEC is cleared to a logic '0' by a RESET task, or by changing the PSAVE or TX/RX bits of the Mode Register.
In Transmit mode this bit is a logic '0'.

B2 DQRDY

Data Quality Reading Ready: In Receive mode DQRDY is set to a logic '1' whenever a Data Quality reading has been completed (see Figure 20, data quality graph). DQRDY is cleared to a logic '0' by a read of the Data Quality Register, or by changing the PSAVE or TX/RX bits of the Mode Register.

B1 MOBAN

Mobile or Base Bit-Sync Received: In Receive mode the MOBAN bit is updated at the end of the SFS and SFH tasks. MOBAN is set to a logic '1' whenever the 3 bits immediately preceding a detected Frame Sync are '0' '1' '1' (received left to right), with up to any one bit in error.

MOBAN is set to a logic '0' if the bit pattern is '1' '0' '0', again with up to any one bit in error. Thus if this bit is set to a logic '1' then the received message is likely to have originated from a mobile station, and if set to a logic '0' the call is likely to have originated from a base station. The Data Formats section of this document describes the different mobile and base sync structures.
In Transmit mode this bit is a logic '0'.

B0 *Reserved*

This bit is always set to a logic '0'.

Programming Information .....

The Data Quality Register

The information presented in this 8-bit register is intended to indicate the quality of the receive signal during a Mobitex Data Block or 30 single bytes.

In Receive Mode, the modem measures the quality of the received signal by comparing the actual received zero-crossing time against an internally generated time. This value is averaged over 240 bits and at the end of the measurement the Data Quality Register and the Data Quality Reading Ready (DQRDY) bit in the Status Register are updated. An interrupt will only occur at this time if the DQEN bit in the Mode Register = logic '1'.

In Transmit Mode all bits are set to a logic '0'.

To provide synchronization with Data Blocks, and thereby ensure that the DQ Register is updated ready to be read when the RDB task finishes, the measurement process is reset at the end of Tasks SFH, SFS, RDB and R3H.

Figure 20 shows how the value (0 - 240) read from the Data Quality Register varies with received signal-to-noise ratio.

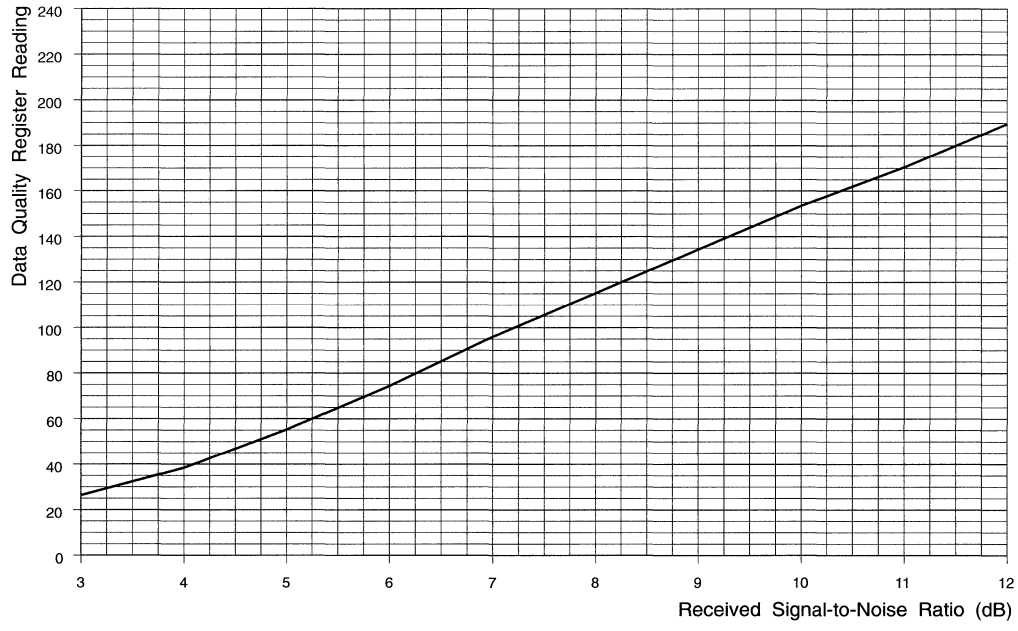
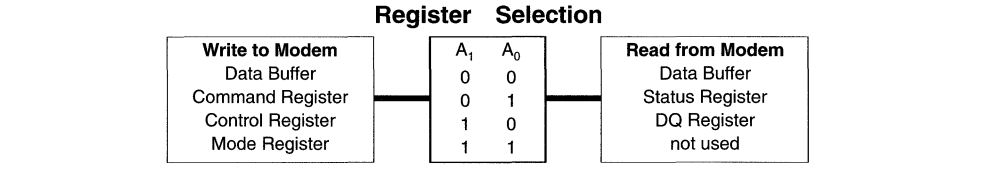


Figure 20 - Typical Data Quality Reading vs RX Signal-to-Noise Ratio (calculated for noise in a bit-rate bandwidth)

Programming Information .....

MX909 Registers

The following diagram is a quick-reference to MX909 register allocations.



Command Register

7	6	5	4	3	2	1	0
AQBC	AQLEV	Reserved set to 0 0 0				TASK	

AQBC - Acquire Bit Clock
AQLEV - Acquire Receive Signal Levels
TASK:

B2	B1	B0	RX Mode	
0	0	0	NULL	
0	0	1	SFH	Search For Frame Head
0	1	0	R3H	Read 3-byte Frame Head
0	1	1	RDB	Read Data Block
1	0	0	SFS	Search For Frame Sync
1	0	1	RSB	Read Single Byte
1	1	0	LFSB	Load Frame Sync Bytes
1	1	1	RESET	

B2	B1	B0	TX Mode	
0	0	0	NULL	
0	0	1	T7H	Transmit 7-Byte Frame Head
0	1	0		Reserved
0	1	1	TDB	Transmit Data Block
1	0	0	TQB	Transmit 4 Bytes
1	0	1	TSB	Transmit Single Byte
1	1	0	TSO	Transmit Scrambler Output
1	1	1	RESET	

Control Register

7	6	5	4	3	2	1	0
CKDIV		HI/LO	DARA		LEVRES		PLLBW

CKDIV - Clock Division Ratio

B7	B6	B5 = 1	B5 = 0	
0	0	256	128	Xtal Bit-Rate
0	1	512	256	
1	0	1024	512	
1	1	2048	1024	

HI/LO - High or Low Xtal Range Selection
DARA - Data Rate
LEVRES - Level Measurement Response Time

B3	B2	
0	0	Hold
0	1	Peak Averaging
1	0	Peak Detect
1	1	Lossy Peak Detect

PLLBW - PLL Bandwidth

B1	B0	Bandwidth (+/- ppm)
0	0	0 (Hold)
0	1	30
1	0	250
1	1	50,000

Mode Register

7	6	5	4	3	2	1	0
IRQEN	INVBIT	TX/$\overline{RX}$	SCREN	PSAVE	DQEN	Reserved set to 0 0	

IRQEN - IRQ Output Enable
INVBIT - Invert Bit
TX/RX - Transmit or Receive Mode
SCREN - Scramble Enable
PSAVE - Powersave
DQEN - Data Quality IRQ Enable

Status Register

7	6	5	4	3	2	1	0
IRQ	BFREE	IBEMPTY	DIBOVF	CRCFEC	DQRDY	MOBAN	Reserved

IRQ - Interrupt Request
BFREE - Data Buffer Free
IBEMPTY- Interleave Buffer Empty
DIBOVF - De-Interleave Buffer Overflow
CRCFEC - CRC or FEC Error
DQRDY - Data Quality Reading Ready
MOBAN - Mobile or Base Bit-Sync Received

Figure 21 - Ready-Use Guide to Register Functions

Operational Information

Cyclic Redundancy Code (CRC)

A 16-bit CRC code is used in the Mobitex Data Block.

In Transmit Mode the CRC is calculated by the modem from the 18 data bytes (see Figure 10, Mobitex System Data Format) using the following generator polynomial:

$$g(x) = x^{16} + x^{12} + x^5 + 1 \qquad [\text{CCITT}]$$

This code detects all (single) error bursts of up to 16 bits in length and about 99.998% of all other error patterns.

The CRC Register is intialized to all logic '1's and the CRC is calculated octet by octet starting with the LSB of byte 0. The CRC calculated is bit-wise inverted and appended to the data bytes with the MSB transmitted earliest.

In Receive Mode a 16-bit CRC code is generated from the 18 data bytes of each Mobitex Data Block as described above and the bit-wise inverted value is compared with the received CRC bytes, if a mis-match is present then an error has been detected.

Forward Error Correction (FEC)

In Transmit Mode, during T7H and TDB, the modem generates a 4-bit Forward Error Correction code for each coded byte.

The FEC is defined by the following H matrix:

	DATA BYTE								*FEC*			
	MSB							LSB	MSB			LSB
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**3**	**2**	**1**	**0**
	1	1	1	0	1	1	0	0	1	0	0	0
H =	1	1	0	1	0	0	1	1	0	1	0	0
	1	0	1	1	1	0	1	0	0	0	1	0
	0	1	1	1	0	1	0	1	0	0	0	1

Generation of the FEC consists of logically ANDing the byte to be transmitted with bits 7 to 0 of each row of the H matrix. Even parity is generated for each of the 4 results and these 4 parity bits, in the positions indicated by the last 4 columns of the H matrix, form the FEC code.

Receive Mode: In checking the FEC the received 12-bit word is logically ANDed with each row of the H matrix (earliest bit received compared with the first column). Again even parity is generated for the 4 resulting words and these parity bits form a 4-bit nibble. If this nibble = 0 then no errors have been detected. Other results 'point' to the bit in error or indicate that uncorrectable errors have occured.

This code can correct any single error that has occured in each 12-bit (8 data + 4 FEC) section of the message.

Example of FEC Generation

If the byte to be coded is **'0 0 1 0 1 1 0 0'**, then the FEC is derived as follows:

H Matrix Row	1	2	3	4
A	1 1 1 0 1 1 0 0	1 1 0 1 0 0 1 1	1 0 1 1 1 0 1 0	0 1 1 1 0 1 0 1
B	**0 0 1 0 1 1 0 0**	**0 0 1 0 1 1 0 0**	**0 0 1 0 1 1 0 0**	**0 0 1 0 1 1 0 0**
A 'AND' B	0 0 1 0 1 1 0 0	0 0 0 0 0 0 0 0	0 0 1 0 1 0 0 0	0 0 1 0 0 1 0 0
Even Parity	1	0	0	0

With reference to the table above, Row A is bit 7 to 0 of one row of the H matrix and Row B is the byte to be coded. The Even Parity bits refer to the result of 'A' AND 'B'.

Therefore the word formed will be: **'0 0 1 0 1 1 0 0 1 0 0 0'** -sent left to right.

When the same process is carried out on these 12 bits (**'0 0 1 0 1 1 0 0 1 0 0 0'**), using all 12 bits of each H matrix row, the resulting parity bits will be **'0 0 0 0'.**

Operational Information .....

Interleaving

The 240 bits of a Mobitex Data Block are interleaved by the modem before transmission to give protection against noise bursts and short fades. Interleaving is not performed on any bits in the Mobitex Frame Head.

Considering the 240 bits to be numbered sequentially before interleaving as 0 to 239 (0 = bit 7 of byte 0, 11 = bit 0 of the FEC for byte 0, and ..... ,239 = bit 0 of the FEC for byte 19), then they will be transmitted as shown in Figure 22.

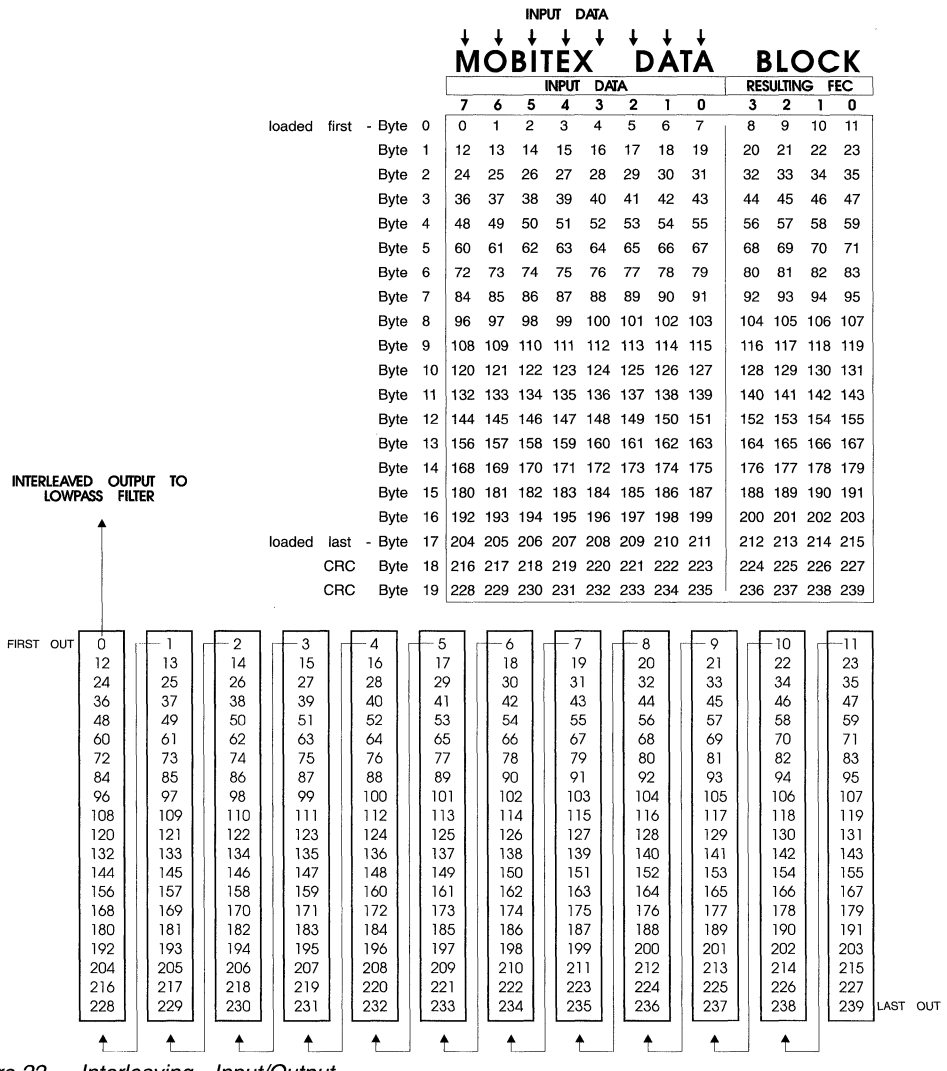


Figure 22 - Interleaving - Input/Output

Scrambling

The Mobitex Data Block may be transmitted or recieved as scrambled information in accordance with the setting of the Scramble Enable bit (Mode Register SCREN).

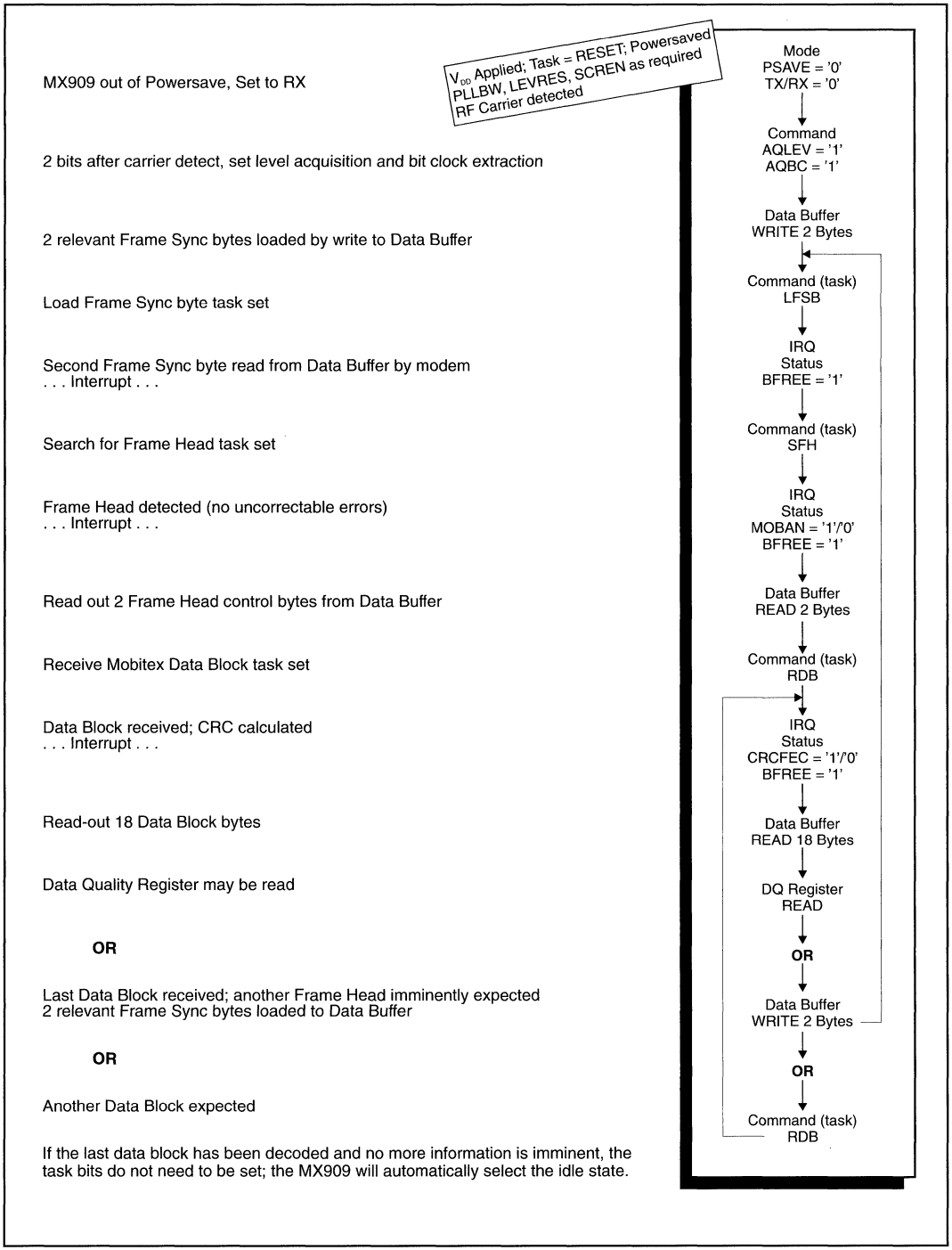
All formatted bits of a Mobitex Data Block are passed through a 9-bit scrambler. This scrambler is initialized at the beginning of the first data block in every frame.

The 511-bit sequence is generated with a 9-bit shift register with the output of the 5th and 9th stages being Exclusive OR'd and fed back to the input of the 1st stage. The scrambler is enabled when SCREN = logic '1' or when the Transmit Scrambler Output (TSO) task is selected but disabled during all others.

Operational Information .....

"Receive (Mobitex) Frame" Example

If the MX909 is required to receive a Mobitex Frame, assuming that the device starts from a powersave state, the following sequences of control and data will have to be issued:



Operational Information .....

"Transmit (Mobitex) Frame" Example

If the MX909 is required to send a Mobitex Frame, assuming that the device starts from a powersave state, the following sequences of control and data will have to be issued:

MX909 out of Powersave, set to TX

V_{DD} Applied; Task = RESET; Powersaved; SCREN, DARA, CKDIV and DQEN as required

A 2 bit pause is required to allow the lowpass filter to stabilize. During this time the 6 bytes forming the Frame Head may be loaded to the Data Buffer by the µController

Transmit Frame Head task set

Last (6th byte) of Frame Head read from Data Buffer by modem
- - - Interrupt - - -

Load 18 data bytes into the Data Buffer

Transmit Data Block task set

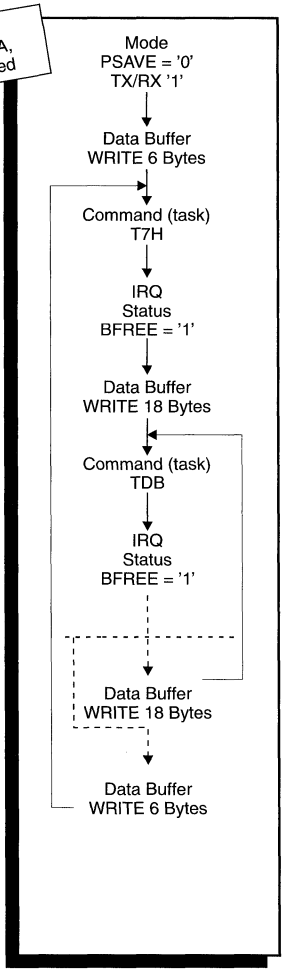
Last (18th) byte of the loaded data read from the Data Buffer by modem
- - - Interrupt - - -

Load data and set tasks as required

Another Data Block in this current frame is to be transmitted
Load 18 data bytes into the Data Buffer

Last Data Block has been transmitted... another frame is to be transmitted
Transmit Frame Head
6 bytes forming the Frame Head are loaded to the Data Buffer by the µController, followed by a 2-bit pause to allow the Lowpass Filter to stabilize

If the last Data Block has been transmitted and another frame is not to be sent, then a new task need not be written and the µController can wait for the (Status Register) IBEMPTY interrupt when, after a few bits pause, to allow for the TX Lowpass Filter delay, it can shut down the RF circuitry if required.



Operational Information .....

Received Signal Acquisition

Level Measurement and Clock Extraction

To achieve reasonable error rates the MX909 modem needs to make accurate measurements of the received signal amplitude, DC offset and bit-timing. Accurate measurements, especially in the presence of noise, are best made by averaging over a relatively long time period.

In most cases the modem will be used to receive isolated messages from a distant transmitter that is only turned on for a very short time before the message starts; also, the received baseband signal from the radio's frequency discriminator will have a DC offset due to small differences between the receiver and transmitter reference oscillators and hence their 'carrier' frequencies.

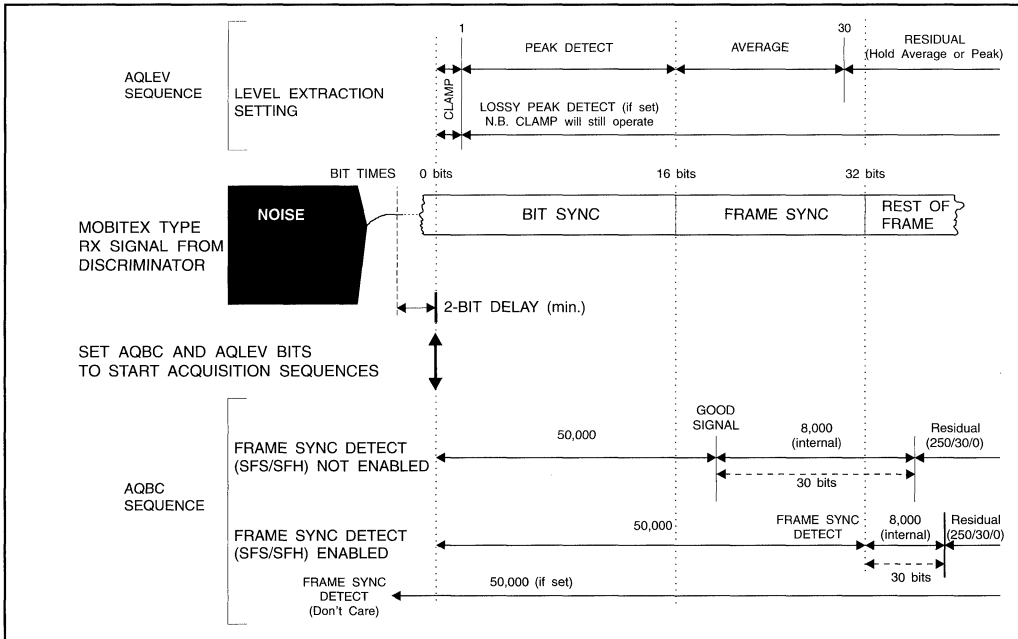
To allow for this situation, AQBC and AQLEV (Acquire Bit Clock and Level) commands cause the modem to follow an automatic sequence designed to perform the measurements as quickly as possible.

The complete AQBC and AQLEV sequence is illustrated in Figure 23; in the described situation the µController can detect the received carrier and therefore knows when to issue the AQBC and AQLEV commands.

Note that due to the delay through the RX low pass filter, the AQBC and AQLEV sequences should not be started until about 2-bit times after the RX carrier has been detected at the discriminator output.

In a system where the controlling µController is not able to detect the RX carrier, the AQBC and AQLEV sequences may be started at any time; possibly when no carrier is being received. However in this case the clock and level acquisition operation will take longer as the circuits will have to recover from the change from a large amplitude noise signal at the output of the frequency discriminator to the wanted signal, probably with a DC offset. In this type of system the time between the turn-on of the transmitter and the start of the Frame Sync pattern should be extended -preferably by extending the Bit Sync sequence to 32 or even 48 bits.

Note that the clock extraction circuits work by detecting the timing of received edges, i.e. a change from '0' to '1' or '1' to '0'. They will eventually fail if logic '1's or logic '0's are transmitted continuously. Similarly, the level measuring circuits require '00' and '11' bit pairs to be received at reasonably frequent intervals.



GOOD SIGNAL is determined if the last 4 zero-crossings have been detected as clean. i.e. little jitter
If Frame Sync is not set, then the '8,000' setting will start
when either: 1 GOOD signal is detected
2 Frame Sync is set and detected -- WHICHEVER OCCURS FIRST

The acquisition sequences AQLEV and AQBC can be set independantly and at any time.

If AQBC is set with Frame Sync Detect (SFS) active then the 50,000 setting will continue until Frame Sync is received, or the PLLBW bits are changed, or the device is reset .

Figure 23 - Bit-Clock and Level Acquisition Example

Operational Information .....

Received Signal Acquisition .....

Acquire Receive Signal Levels
AQLEV **Command Register**

The Acquire Receive Signal Levels (AQLEV) sequence starts with a measurement of the average signal voltage over a period of 1 bit-time (CLAMP). If the LEVRES bits are not set to 'Lossy Peak Detect' ('1' '1') the sequence continues by measuring the positive-going and negative-going peaks of the signal.

The attack and decay times used in this 'peak detect' mode are such that a sufficiently accurate measurement can be made within 16 bits of a '11001100 ...' pattern (i.e the bit-sync sequence) to allow the bit-clock extraction circuits to operate.

Once the bit-clock extraction circuits have detected the presence of a sufficiently coherent signal, then -provided that the LEVRES bits of the Control Register have been set to the 'Peak Averaging' settings or 'Hold'- the level measurement circuits will switch to the 'Peak Averaging' mode, in which they calculate the average of the peak voltages due to received bits.

If the LEVRES bits are set to 'Hold' the 'Peak Averaging' measurement will cease after 16 bit times -and the final values kept- otherwise the circuits will continue in the operation as previously described.

For normal operation the LEVRES bits would only be set by the controlling µController to 'Hold' for the duration of a "fade".

Acquire Bit Clock
AQBC **Command Register**

The Acquire Bit Clock (AQBC) sequence follows a similar pattern; starting with a very fast initial estimate of the received bit timing, then reducing the bandwidth of the Phase Locked Loop as a coherent signal is detected until the limit reached by the (Control Register) PLLBW bits is reached.

LEVRES Peak Detect and Peak Averaging Operation

Further information on this subject is currently unavailable in this "Advance Information" Document

Operational Information .....

Control and Data Load Timing

Control Instructions, Task and Data is loaded to the MX909 in a parallel form as detailed in the relevant Programming Information sections of this Data Sheet. Timing information for Read and Write operations is given in Figure 24; timing parameters are provided in the Specification section.

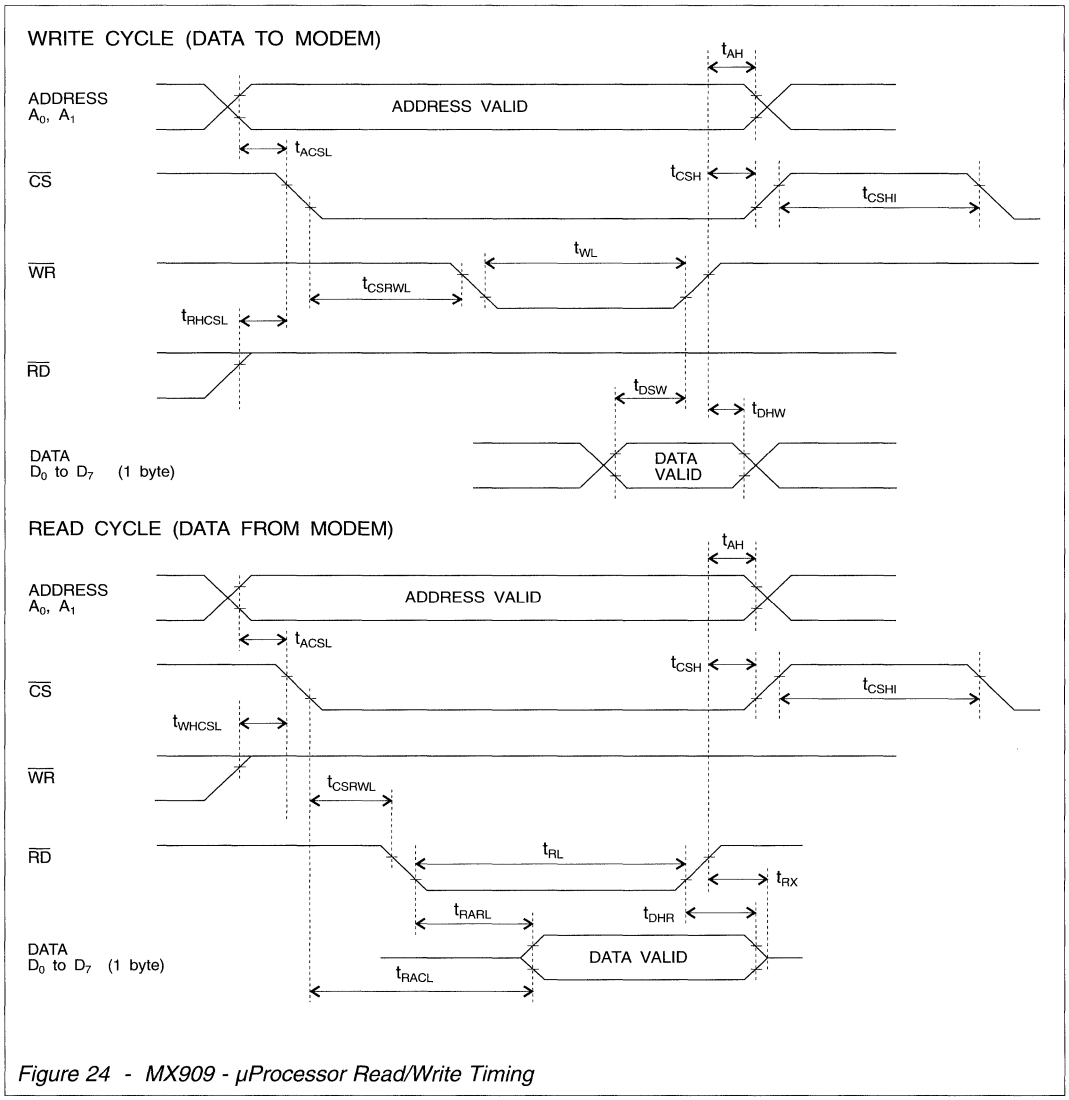


Figure 24 - MX909 - µProcessor Read/Write Timing

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0V
Input Voltage at any pin (ref V_{SS}=0V)	-0.3 to (V_{DD}+ 0.3V)
Sink/Source Current (supply pins)	±30mA
(other pins)	±20mA
Total Device Dissipation (@ T_{AMB}=25°C)	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Bit Rate = 8 kbps

Xtal/Clock = 4.096 MHz

Noise Bandwidth = Bit Rate

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	-	5.5	V
I_{DD} (powersaved)	1	-	1.0	1.5	mA
I_{DD} (not powersaved)	1	-	8.0	12.0	mA
TX Output					
Impedance (not powersaved)	2	-	1.0	2.5	kΩ
Impedance (powersaved)	2	300	500	-	kΩ
Signal Level	3	0.9	1.0	1.1	Vp-p
TX Data Delay	4	-	4.0	6.0	bits
Power-up to TX Out Stable Time	5	-	3	5	bits
TX Low Pass Filter	6				
RX Input					
Impedance (RX In pin)		10.0	-	-	MΩ
RX Input Amp Voltage Gain		-	500	-	V/V
Input Signal Level	7	0.7	1.0	1.3	Vp-p
RX Data Delay	8	-	3.5	-	bits
Xtal/Clock					
Xtal/Clock Frequency		1.0	-	10.0	MHz
'High' pulse width	9	40.0	-	-	ns
'Low' pulse width	9	40.0	-	-	ns
Input Impedance		10.0	-	-	MΩ
Inverter Gain (I/P = 1mV rms @ 1kHz)		20.0	-	-	dB
µController Interface					
Input logic '1' level	10, 11	V_{DD} -1.5	-	-	V
Input Logic '0' level	10, 11	-	-	1.5	V
Input Leakage Current (V_{IN} = 0V to V_{DD})	10, 11	-5.0		+5.0	µA
Input Capacitance	10,11	-	10.0	-	pF
Output Logic '1' Level (IOH = 120µA	11	V_{DD} -0.4			V
Output Logic '0' Level (IOL = 360µA)	11,12	-	-	0.4	V
'Off' State Leakage Current (V = V_{DD})	12	-	-	10	µA

Specifications .....

Modem Read/Write Load Timing

Description		Note	Min.	Typ.	Max.	Unit
t_{ACSL}	"Address Valid" to "CS Low" time		0	-	-	ns
t_{AH}	"Address Hold" time		0	-	-	ns
t_{CSH}	"CS Hold" time		0	-	-	ns
t_{CSHI}	"CS High" time	14	6.0	-	-	Xtal/Clock Cycles
t_{CSRWL}	"CS" to "WR" or "RD" Low time		0	-	-	ns
t_{DHR}	"Read-Data Hold" time		0	-	-	ns
t_{DHW}	Write-Data Hold time		0	-	-	ns
t_{DSW}	Write-Data Set-Up" time		90.0	-	-	ns
t_{RHCSL}	"RD High" to "CS Low" time (write cycle)		0	-	-	ns
t_{RACL}	"Read Access" time from "CS Low"	13	-	-	175	ns
t_{RARL}	"Read Access" time from "RD Low"	13	-	-	145	ns
t_{RL}	"RD" Low time		200	-	-	ns
t_{RX}	"RD High" to "D_0-D_7 3-State" time		-	-	50.0	ns
t_{WHCSL}	"WR High" to "CS Low" time (read cycle)		0	-	-	ns
t_{WL}	"WR" Low time		200	-	-	ns

Notes:

1. Not including any current drawn from the modem pins by external circuitry.
2. Small signal impedance (dynamic measurement).
3. Measured after external CR (R_4/C_6) filter, for 1111000011110000.. bit sequence; at V_{DD} = 5.0V (output level is proportional to V_{DD}).
4. Measured between issuing first task after idle and the center of the first bit at TX Out (see Figure 13, 'The TX Process').
5. Measured between setting PSAVE = '0' and TX output becoming stable.
6. See Figure 25, Lowpass filter response.
7. For optimum performance, measured at the RX Feedback pin, for a '...11110000...' bit sequence.
8. Measured between center of last bit of an RX single byte or Frame Sync at RX In and an IRQ interrupt to the µController.
9. Timing for an external input to the Xtal/Clock pin.
10. $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A_0 and A_1 pins.
11. D_0 - D_7 pins.
12. $\overline{IRQ}$ pin.
13. With 30pF (Max.) to V_{SS} on D_0 - D_7 pins.
14. Xtal/Clock cycles at the Xtal/clock pin.

Lowpass Filter Response

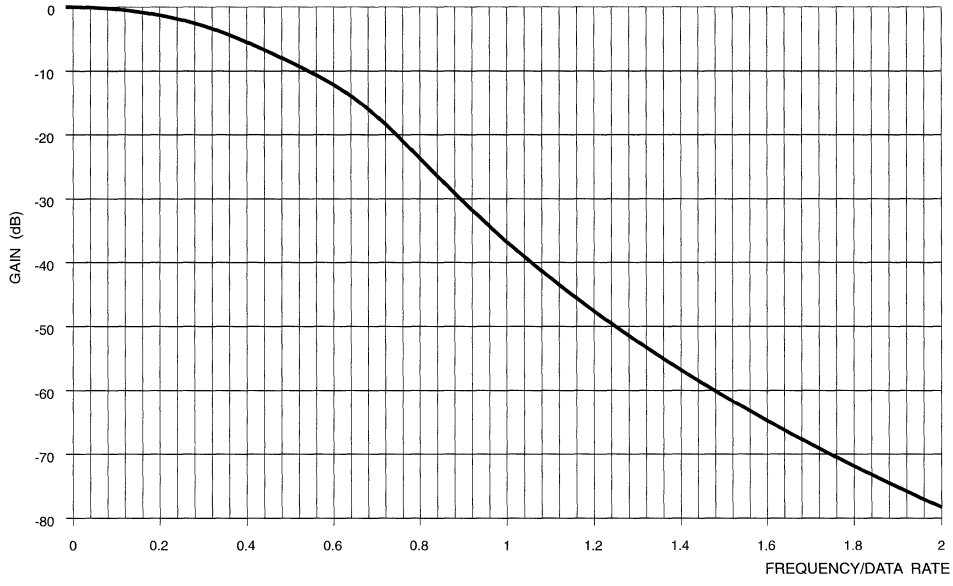


Figure 25 - Lowpass Filter Response (Including the External RC Filter Components) in the TX Mode

Signal-to-Noise Performance

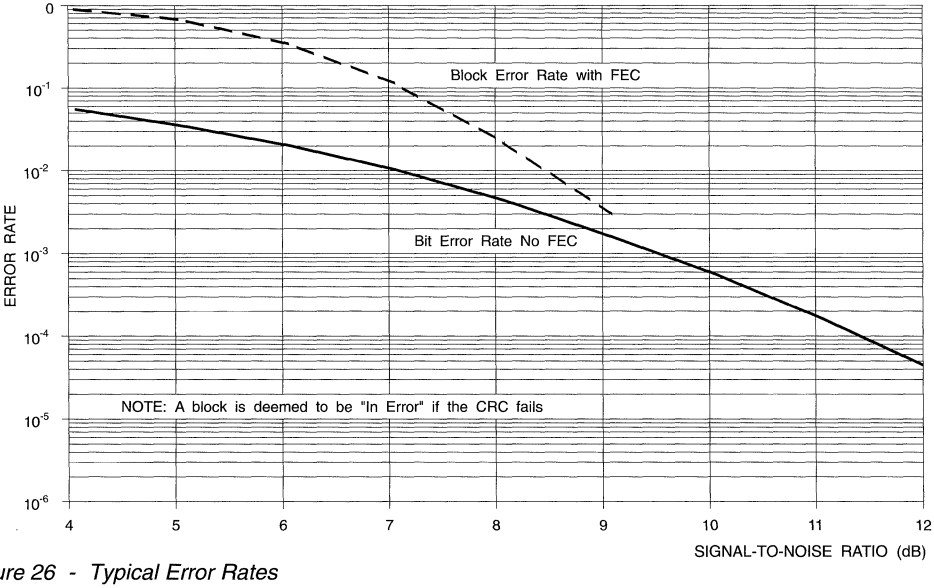


Figure 26 - Typical Error Rates

Bit and Block Errors

The figure above shows both bit and block error possibilities for a received signal with a specific signal-to-noise performance. Bit Errors are individually detected errors in the raw data stream.

Block Errors are those where a complete block of data (240 bits; see Figure 10, Data Format) is in error, as indicated by the CRC. Note that signal-to-noise ratios illustrated in this Data Bulletin are calculated for noise in a bit-rate bandwidth.

MX•COM, INC.

Advance Information

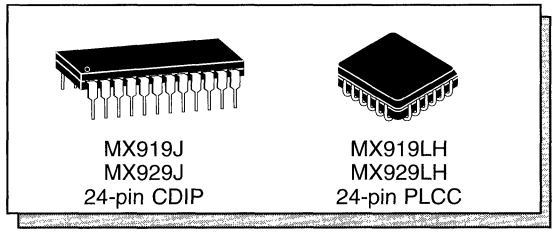
MX919
MX929

HIGH-SPEED FOUR-LEVEL FSK "PACKET DATA" MODEMS

MX919: General Purpose ***MX929: RD-LAP* (ARDIS**)***

Features

- **MX-COM MX'D Signal CMOS**
- **FM Radio Packet Data Applications**
  - **Wireless Data Systems**
  - **Radio Telemetry**
  - **Mobile Data Links**
  - **Wireless LANs**
  - **Medical Telemetry**
  - **Wireless Bar-Code Readers**
- **4-Level FSK - 4.8/9.6/19.2 kbps**
- **Low Power Requirement**
- **Custom Frame Capabilities (MX919)**
- **Automatic Protocol Handling (General Purpose & RD-LAP)**
  - **Symbol and Frame Sync**
  - **Block Formatting**
  - **Forward Error Correction**
  - **CRC Check and Generation**
  - **Interleaving**
- **PCMCIA Packaging Available*****



MX919J
MX929J
24-pin CDIP

MX919LH
MX929LH
24-pin PLCC

Description

The MX919 and MX929 are half-duplex high-speed, 4-level FSK 'packet data' modems. They work with a host µController to provide packet data transfer via FM radio systems.

The MX919 provides a versatile frame structure for general-purpose applications. The MX929 is designed specifically for the ARDIS RD-LAP network.

Having a low power requirement of 5.0mA at 5 volts, the MX919 and MX929 modems provide:

- Automatic handling of general purpose (MX919) and RD-LAP (MX929) frame structures, including RX symbol and frame synchronization, block formatting, CRC generation and checking, Forward Error Correction and Interleaving to reduce the processing load on the host µController.
- Selectable data rates of 2400/4800/9600 symbols/s (4.8/9.6/19.2 kbps) for high-speed operation.
- 4-Level FSK (2 bits per baud) baseband modulation enables high-speed, economical data rates in a narrow RF bandwidth.
- On-chip baseband processing and filtering.
- Pre-selectable signal acquisition and tracking permits the rapid acquisition of received signals, followed by automatic tracking of signal dc level variations.

Clock recovery PLL bandwidth and RX signal level measurement circuitry will react automatically when set.

RX and TX data and control between the host µController and this microcircuit is via an 8-bit bi-directional parallel interface; input and output signals to and from the radio system are in analog form suitable for connection to the radio's discriminator and frequency modulator.

The MX919 and MX929 modems are available in 24-pin CDIP and Surface Mount packages, as well as packaging for PCMCIA applications***.

**RD-LAP is a trademark of Motorola, Inc.*
***ARDIS is a service mark of ARDIS.*
****Contact MX-COM for more information.*

MX919 and MX929 Circuit Descriptions

Data Bus Buffers

Eight bi-directional 3-state logic-level buffers between the modem's internal registers and the controlling µController's data-bus lines.

R/W, CS and Address Lines

Control the transfer of data bytes between the µController and the modem's internal registers, according to the state of the Write and Read Enable ($\overline{WR}$ and $\overline{RD}$) inputs, the Chip Select ($\overline{CS}$) input and the Register Address inputs (A_0 and A_1).

The Data Bus Buffers and Address & R/W Decode blocks provide a byte-wide parallel µController interface.

Status and Data Quality Registers

8-bit registers which the µController can read to determine the status of the modem and the received data quality.

Command, Mode and Control Registers

The values written by the µController to these 8-bit registers control the operation of the modem.

Data Block Buffer

An 12-byte buffer used to hold RX or TX data to or from the µController.

CRC Generator/Checker

A circuit which generates (transmit mode) or checks (receive mode) the Cyclic Redundancy Checksum bits which may be included in transmitted data blocks so that the receive modem can detect transmission errors.

FEC Generator/Checker

In transmit mode, this circuit adds Forward Error Correction bits to the transmitted data, then converts the resulting binary data to 4-level symbols. In receive mode, it translates received 4-level symbols to binary data, using the FEC information to correct a large proportion of transmission errors. The 4 possible levels of a symbol are referred to in this Data Sheet as: +3, +1, -1 and -3.

Interleave/De-interleave Buffer

Interleaves data symbols within a data block before transmission and de-interleaves the received data so that the FEC system is best able to handle short noise bursts or fades.

RX Input Amp

The amplifier that allows the received signal input to the modem to be set to the optimum level by suitable selection of the external components.

Frame Sync Detect

This circuit, which is only active in the receive mode, is used to look for the user-specified 24-symbol Frame Synchronization pattern which is transmitted to mark the start of every frame.

Root Raised Cosine (RRC) Filter

This filter, which is used in both transmit and receive modes, is a linear-phase lowpass filter with a 'Root Raised Cosine' frequency response.

In TX mode, the 4-level symbols are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels.

In RX mode this filter is used to reject HF noise and to equalize the received signal to a form suitable for extracting the 4-level symbols.

RX Symbol/Clock Extraction

These circuits, which operate only in receive mode, extract a symbol-rate clock from the received signal, and measure the received signal amplitude and its dc offset.

This information is then used to extract the received 4-level symbols and also to provide an input to the received Data Quality measuring circuit.

Clock Oscillator and Dividers

This circuit derives the transmit symbol-rate (and the nominal receive symbol-rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or fed from an external source.

TX Output Buffer

A unity-gain amplifier used in the transmit mode to buffer the output of the RRC filter. In receive mode, the input of this buffer is normally connected to V_{BIAS} unless the RXEYE bit of the Control Register is set. When the modem is set to the powersave mode, the buffer is turned off and the TX Output pin connected to V_{BIAS} via a high value resistance.

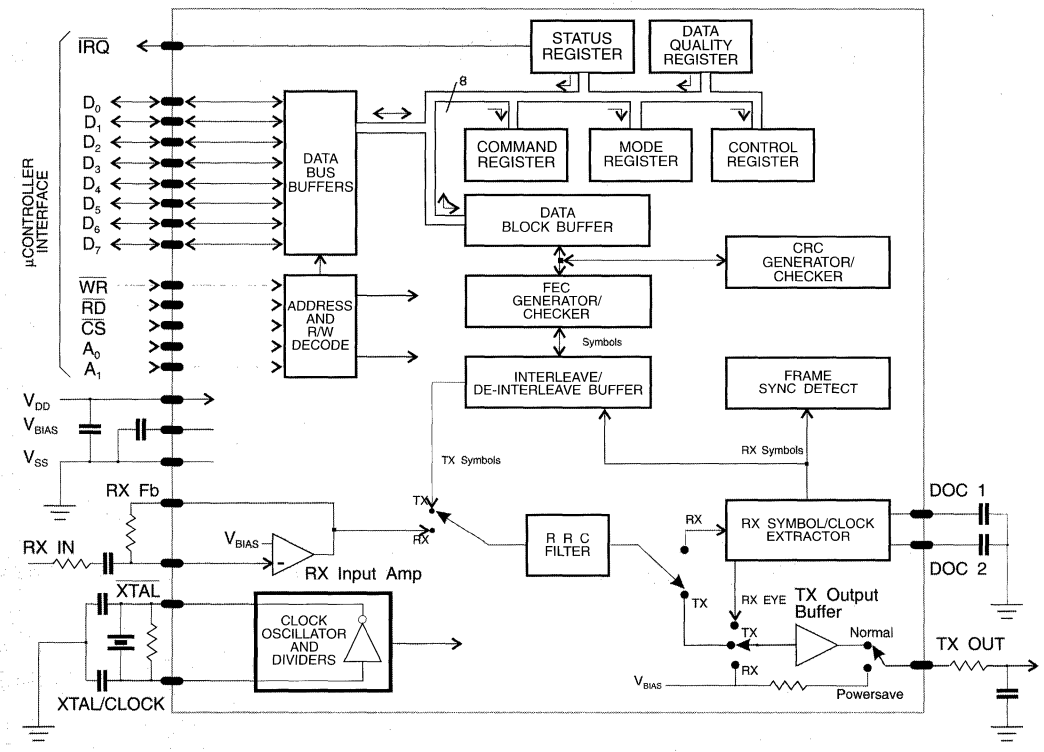


Figure 1 - MX919/MX929 Functional Block Diagram

MX919 and MX929 Pin Functions

Pin	Function
1	**$\overline{IRQ}$:** A 'wire-ORable' output for connection to the controlling µController's Interrupt Request input. This output has a low-impedance pull-down to V_{SS} when active, and is high-impedance when inactive.
2	**D_7:**
3	**D_6:**
4	**D_5:**
5	**D_4:** 8 bi-directional 3-state µController interface data lines.
6	**D_3:**
7	**D_2:**
8	**D_1:**
9	**D_0:**
10	**$\overline{RD}$:** An active-low logic level input used to control the reading of data from the modem into the controlling µController.
11	**$\overline{WR}$:** An active-low logic level input used to control the writing of data into the modem from the controlling µController.
12	**V_{SS}:** The negative supply rail (ground).
13	**$\overline{CS}$:** An active-low logic level input to the modem used to enable a data Read or Write operation (see Figure 26, Timing).
14	**A_0:** Two logic-level modem register selection inputs.
15	**A_1:**
16	**$\overline{Xtal}$:** The output of the on-chip Xtal oscillator.
17	**Xtal/Clock:** The input to the on-chip Xtal oscillator. Operation of the MX919/MX929 without a suitable Xtal or clock input may cause device damage.
18	**Doc 2:** Connections to the internal RX signal level measurement circuitry. Capacitors as
19	**Doc 1:** shown in Figure 2 should be installed from each of these pins to V_{SS}.
20	**TX Out:** The TX signal output from the modem.
21	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$, this pin must be decoupled to V_{SS} by a capacitor mounted close to the device pins.
22	**RX In:** The input to the RX input amplifier.
23	**RX Feedback:** The output of the RX input amplifier, and the input to the (RX) Lowpass Filter.
24	**V_{DD}:** The positive supply. Levels and voltages within the modem are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the device pins.

Installation Information

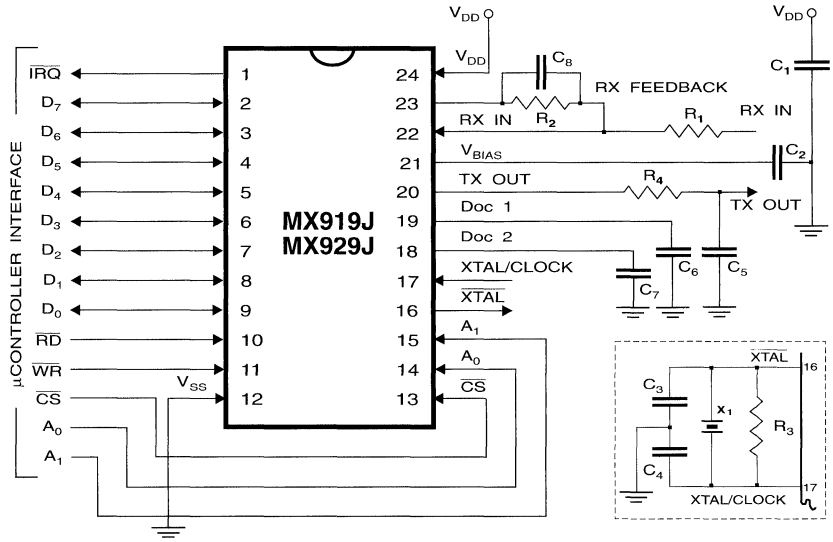


Figure 2 - Recommended External Components

Component	Value	Tolerance
R_1	Note 1	±10%
R_2	100kΩ	±10%
R_3	1.0MΩ	±20%
R_4	**Note 2**	
C_1	0.1µF	±20%
C_2	0.1µF	±20%
C_3	Note 3	±20%
C_4	Note 3	±20%
C_5	**Note 2**	
C_6	**Note 2**	±20%
C_7	Note 4	±20%
C_8	**TBD**	
X_1	Note 3	

Installation Notes

1. Resistors R_1 and R_2, with the RX Input Amplifier, set the signal input level to the modem. The value of R_1 should be calculated to give 1.0v p-p at the RX Feedback pin for a received +3 +3 -3 -3 +3 +3 -3 -3 sequence. The dc level of the received signal should be adjusted so that the signal at the modem's RX Feedback pin is centered around V_{BIAS}.

2. External components R_4 and C_5 form an RC lowpass filter between the TX Buffer output and the input to the radio's frequency modulator; this is an important part of the TX signal filtering. These components may form a part of any dc level shifting and gain adjustment circuitry. The ground connection (V_{SS}) of C_5 should be positioned to give maximum attenuation of high frequency noise into the modulator.

   R_4 and C_5 should be chosen so that the product of R_4 (Ohms) and C_5 (Farads) is:

   $$\frac{0.34}{\text{bit rate (bits per sec)}}$$

   R_4 should be not less than 20kΩ; the value used for C_5 should take into account parasitic capacitance.

Examples	R_4	C_5
8000bps	100kΩ	430pF
4800bps	100kΩ	710pF

3. The values used for C_3 and C_4 are determined by the frequency of X_1.

   As a guide:

   $C_3 = C_4 = 33pF$ for $X_1 < 5.0MHz$.

   $C_3 = C_4 = 18pF$ for $X_1 > 5.0MHz$.

   If the on-chip Xtal oscillator is to be used, then the external components X_1, C_3, C_4, and R_3 are required as shown in Figure 2 (inset). If an external clock source is used these components are not required; the input should be connected to the Xtal/clock pin and the Xtal pin left unconnected. Table 8 provides advice on the selection of the correct Xtal value.

4. External capacitors C_6 and C_7 form part of the received signal level measuring circuit. For optimum performance the values of these components should be as shown below.

For	C_6 and C_7
2400 symbols/sec	0.02µF
4800 symbols/sec	0.01µF
9600 symbols/sec	0.0047µF

Installation Information...

Binary to Symbol Translation

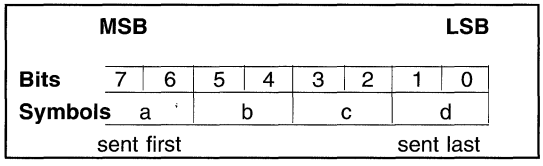
Although the over-air signal, and hence the signals at the modem TX Out and RX In pins, consists of 4-level symbols, the raw data passing between the modems and the µController is in binary form. The MX919/929 translates between binary data and the 4-level symbols in one of two ways, depending on the task being performed:

Direct

The simplest form, which converts between 2 binary bits and one symbol according to the table below.

Symbol	MSB	LSB
+3	1	1
+1	1	0
-1	0	0
-3	0	1

This scheme can be expanded so that an 8-bit byte translates to four symbols:



With Forward Error Correcting (FEC)

This is more complicated, but essentially translates 3 binary bits to two 4-level symbols using an FEC coding scheme which lets the receiving modem detect and correct a large proportion of transmission errors. Full details are given later in this document

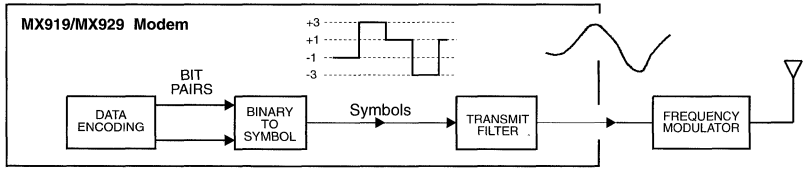


Figure 3 - Flow Through the MX919

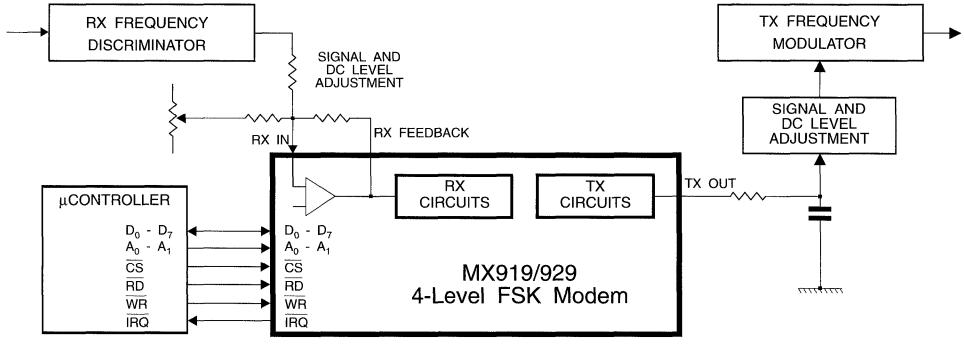


Figure 4 - External Signal Paths

Installation Information .....

AC Coupling

For a practical application, AC coupling from the modem's transmit output to the Frequency Modulator and from the receiver's Frequency Discriminator to the receive input of the modem may be desired. There are, however, two problems.

1) AC coupling of the signal degrades the bit-error-rate performance of the modem. Figure 5 illustrates the typical bit error rates at 4800 symbols/sec (without FEC) for differing degrees of AC coupling;

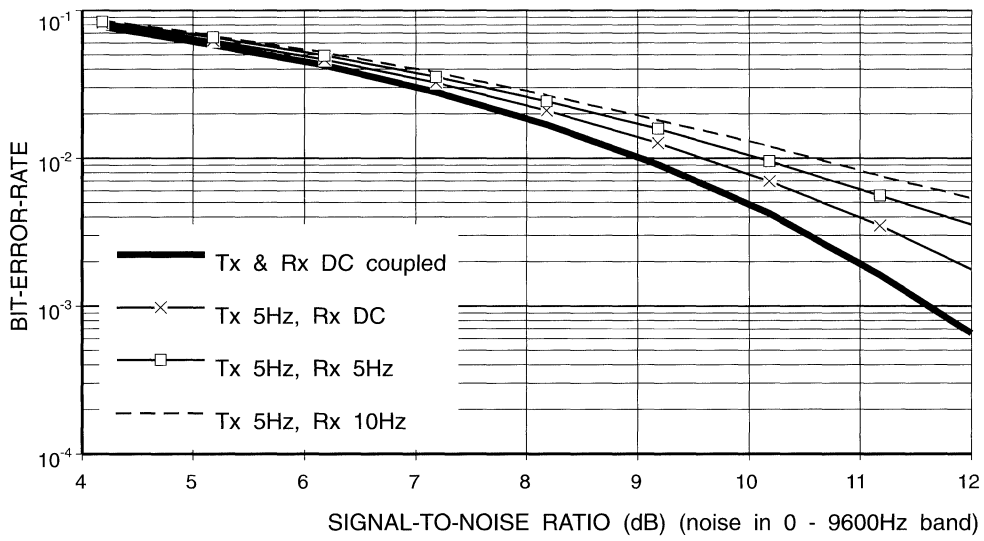


Figure 5 - Examples of BER Performance Degradation Due to Varying Degrees of AC Coupling

2) Any AC coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits. As illustrated below, the time for this voltage step to decay to 37% of its original value is:

$$RC = \frac{1}{(2\Pi \times f)}$$

Where f is the 3dB cut-off frequency of the AC coupling network; RC is 32msec -or 153 symbol-times at 4800symbols/sec- for a 20Hz network.

In general, it will be best to DC couple the receive discriminator to the modem, and to ensure that any AC coupling to the transmitter's frequency modulator has a -3dB cut-off frequency of no higher than 5Hz (for 4800symbols/sec).

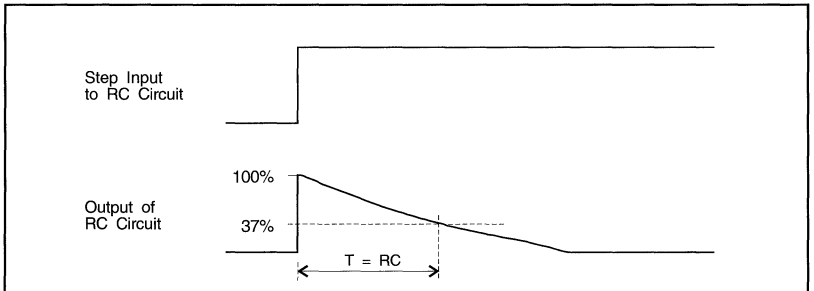


Figure 6 - Decay Problems of the RC Network

Radio Performance

The maximum data rate that can be transmitted over a radio channel using the MX919/929 depends on:

- RF channel spacing.
- Allowable adjacent channel interference.
- Symbol rate.
- Peak carrier deviation (modulation index).
- TX and RX reference oscillator accuracies.
- Modulator and demodulator linearity.
- Receiver IF filter frequency and phase characteristics.
- Use of error correction techniques.
- Acceptable error rate.

As a guide, 4800 symbols/sec can be achieved -subject to local regulatory requirements- over a system with 12.5kHz channel spacing if the transmitter frequency deviation is set to ±2.5kHz peak for a repetitive +3 +3 -3 -3 pattern and the maximum difference between transmitter and receiver "carrier" frequencies is less than 2400Hz.

The modulation scheme employed by these modems is designed to achieve high data throughput by exploiting as much as possible of the RF channel bandwidth. This does, however, place constraints on the performance of the radio. In particular, attention must be paid to:

- Linearity, frequency and phase response of the TX Frequency Modulator. For a 4800 symbol/sec system, the frequency response should be within ±2dB over a range 3Hz to 5Hz, relative to 2400Hz.
- The bandwidth and phase response of the receiver's IF filters.
- Accuracy of the TX and RX reference oscillators, as any difference will shift the received signal towards the skirts of the IF filter response and cause a DC offset at the discriminator output.

Viewing the received signal eye (using the Mode Register RX Eye function) gives a good indication of the overall transmitter/receiver performance. See Figure 7 for the appearance of the RX Signal Eye.

RX Mode,
RX EYE bit = '1'
(Mode Register B4)

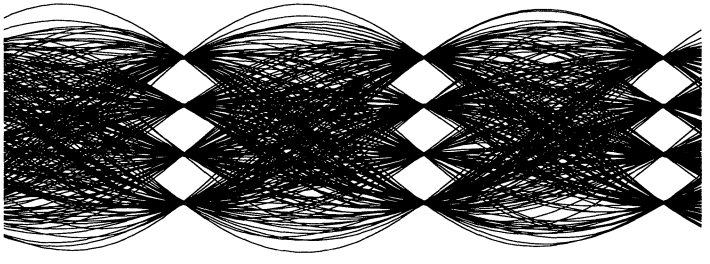


Figure 7 - RX Eye Signal at the TX Out pin for Pseudo-Random Received Data

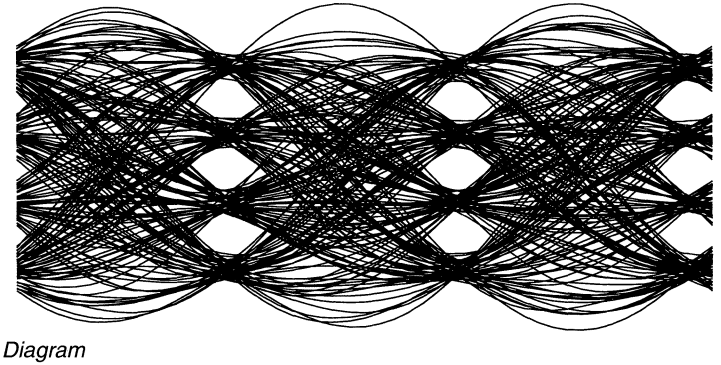


Figure 8 - TX Eye Diagram

Baseband and RF Frequency Requirements

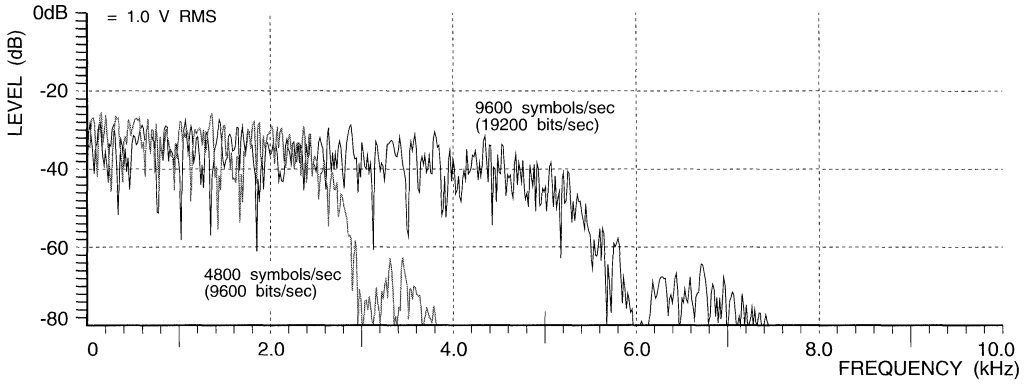


Figure 9 - "TX Out" Spectrum Plot

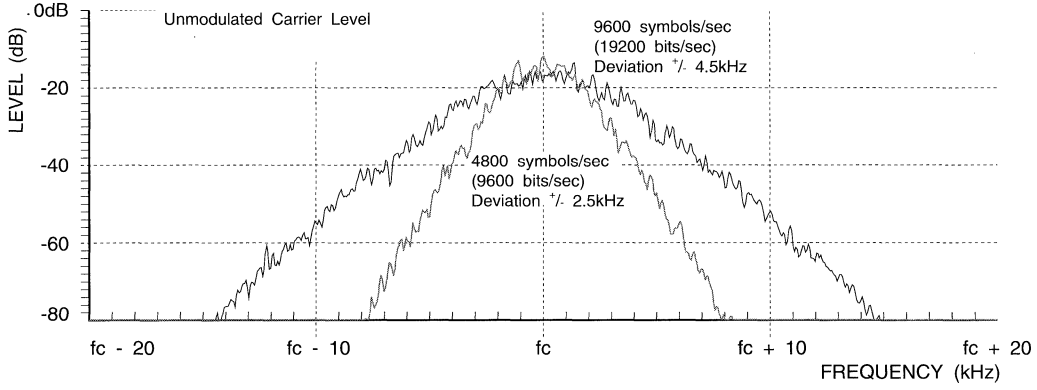
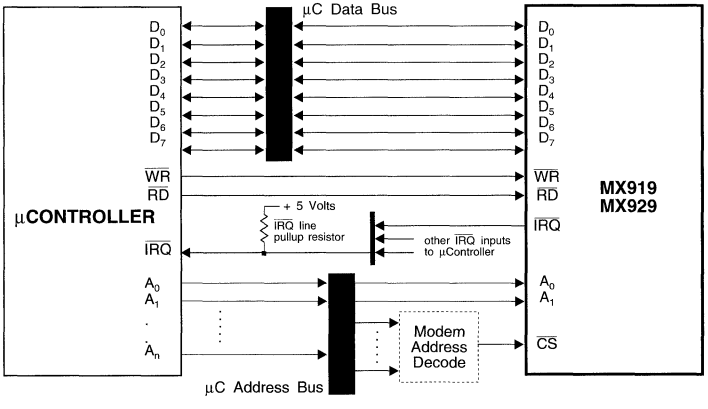


Figure 10 - Theoretical RF Spectrum Plot



The Data Bus Buffers and Address and Read/Write Decode blocks form a byte-wide parallel µController interface.
This diagram shows how this function can be memory mapped.

Figure 11 - Typical Modem to µController Interface

Programming Information

Data Formats

Frame and Data Structures

The MX919 Frame and data structures are illustrated in Figure 12, and the MX929 in Figure 13. The structures consist of a Frame Preamble (comprising Symbol and Frame Synchronization patterns) followed by one or more 'Header', 'Intermediate' or 'Last' blocks. The binary data transferred between the modem and the controlling µController is that shown in the shaded area near the top of the diagram.

The 'Header' block is self-contained in that it includes its own CRC, and would normally carry information such as the addresses of the called and calling parties, the number of following blocks in the frame (if any), and miscellaneous control information.

The 'Intermediate' block(s) contain only data, the CRC checksum for all of the data in the 'Intermediate' and 'Last' blocks is contained at the end of the 'Last' block.

This arrangement, while efficient in terms of data capacity, may not be optimum for poor signal-to-noise conditions, since a reception error in any one of the 'Intermediate' or 'Last' blocks would invalidate the whole frame. In these conditions, increased throughput may be obtained by using the 'Header' block format for all blocks of the frame, so that blocks which are received correctly can be identified, and need not be retransmitted.

In the TX mode, the modem translates the 96 bits of the block into 66 4-level symbols as follows:

The 12 bytes are divided into 32 groups of three bits each (Tri-bits). An extra tri-bit ('0' '0' '0') is added giving a total of 33 tri-bits.

The 33 tri-bits are then passed to the Trellis Encoder which provides 66 4-level symbols.

In the RX mode, the modem takes the 66 received symbols and decodes them into tri-bits.

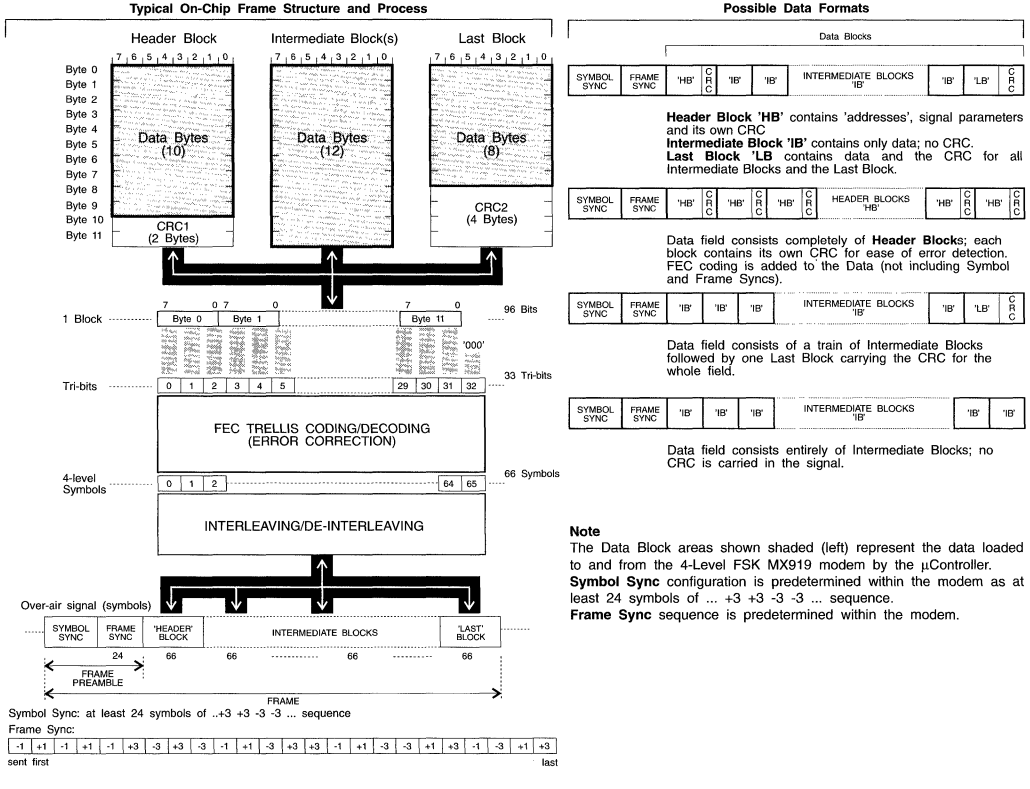
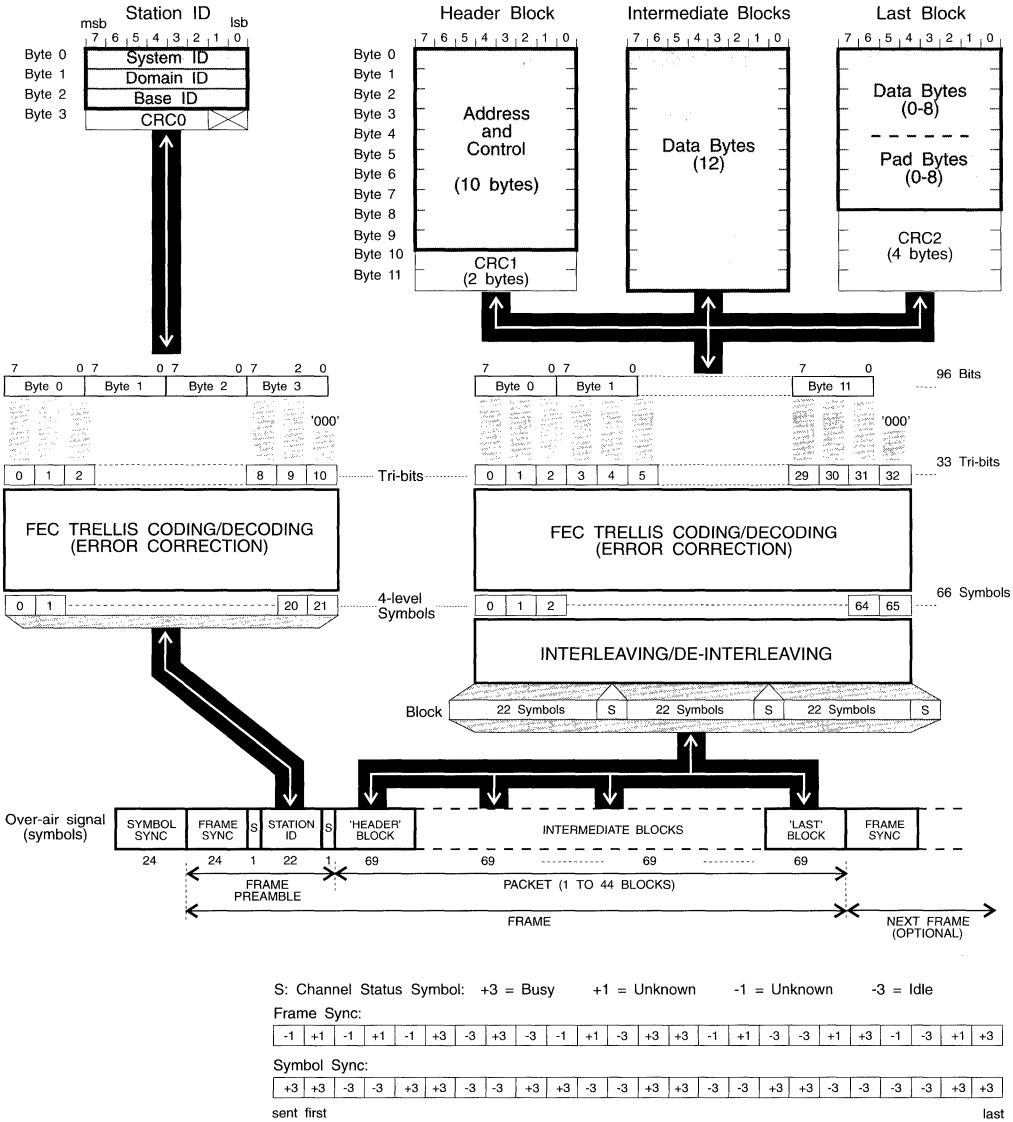


Figure 12 - MX919 System Data Format



Note
The Data Block areas shown shaded represent the data loaded to and from the MX929 modem by the µController.

Figure 13 - MX929 System Data Format

Programming Information .....

Modem/µController Interaction

In general, data is transmitted over-air in the form of messages, or 'Frames', consisting of a 'Frame Preamble' followed by one or more formatted data blocks. The Frame Preamble includes a Frame Synchronization pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (cyclic redundancy checksum) generation, Forward Error Correction coding and Interleaving. Details of the message format handled by the MX919 is shown in Figure 12; the format of the MX929 is in Figure 13.

To reduce the processing load on the associated µController, the MX919/929 has been designed to perform as much as possible of the computationally intensive work involved in Frame formatting and de-formatting and - when in receive mode - in searching for and synchronizing onto the Frame Preamble. In normal operation the modem will only require servicing by the µController once per received or transmitted block.

Thus, to transmit a block, the controlling µController has only to load the -unformatted - 'raw' binary data into the modem's Data Block Buffer then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result as 4-level symbols (with Forward Error Correction coding) and interleave the symbols before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received symbols, de-interleave the symbols, translate them to binary -using the FEC coding to correct as many errors as possible- and check the resulting CRC before placing the received binary data into the Data Block Buffer for the µController to read.

The MX919/929 can also handle the transmission and reception of unformatted data -to allow for example the transmission of Symbol and Frame Synchronization sequences or special test patterns.

Register Selection

The MX919 modem appears to the programmer as 4 write-only 8-bit registers shadowed by 3 read-only registers. Individual registers are selected by the A_1 and A_0 inputs; see Read and Write cycle timing diagrams (Figure 26).

Table 1 Register Selection

A_1	A_0	Write to Modem	Read from Modem
0	0	Data Block Buffer	Data Block Buffer
0	1	Command Register	Status Register
1	0	Control Register	D Q Register
1	1	Mode Register	not used

Data Block Buffer

A 12-byte read/write buffer is used to transfer data (as opposed to Command, Status, Mode, Data-Quality and Control information) between the modem and the controlling µController.

The Data Block Buffer appears to the µController as a single 8-bit register; the modem ensures that sequential µController 'read' or 'write' actions to the buffer are routed to the correct locations within this buffer. When the modem is in the TX mode, any attempt by the µController to 'read' from this buffer will have no effect. Similarly, any attempt to 'write' to this buffer will have no effect when the modem is in the RX mode.

Command Register

Writing to this register instructs the modem to perform a specific action or actions, depending upon the setting of the TASK, AQLEV, and AQSC bits.

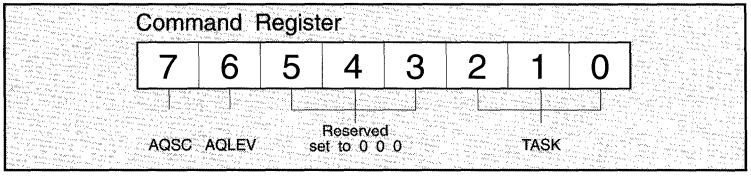


Figure 14 - The Command Register

When it has no action to perform (but is not powersaved), the modem will be in an idle state, and if it is in the TX mode the input to the TX Filter will be connected to a voltage mid-way between the '+1' and '-1' symbol voltages.

In the RX mode the modem will continue to measure the received data quality and extract bits from the received signal, feeding them into the De-Interleave Buffer, but will otherwise ignore the received data.

Programming Information .....

Command Register

B7
AQSC

Acquire Symbol Clock: This bit has no effect in the TX mode.

In the RX mode, whenever a byte with the AQSC bit set to logic '1' is written to the Command Register, it initiates an automatic sequence designed to achieve timing synchronization with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received symbol-timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing synchronization is achieved, until it reaches the 'normal' value set by the PLLBW bits of the Control Register.

Setting this bit to logic '0' (or changing it from '1' to '0') has no effect, however note that the acquisition sequence will be restarted every time that a byte written to the Command Register has the AQSC bit set to logic '1'. The AQSC bit will normally be set at the same time as a SFS (Search for Frame Sync) or SFSH/SFP (Search for Frame Sync + Header for MX919 / Search for Frame Preamble for MX929) task, however it may also be used independently to re-establish clock synchronization quickly after a long fade. Alternatively, an SFS or SFSH/SFP task may be written to the Command Register with the AQSC bit at logic '0' if it is known that clock synchronization does not need to be re-established. Refer to the Operational Information section for further details.

B6
AQLEV

Acquire Receive Signal Levels: This bit has no effect in the TX mode.

In receive mode, whenever a byte with the AQLEV bit set to a logic '1' is written to the Command Register, it initiates an automatic sequence designed to measure the amplitude and DC offset of the received signal as rapidly as possible. This sequence involves setting the measurement circuits to respond quickly at first, then gradually increasing their response time -hence improving the measurement accuracy- until the 'normal' value set by the LEVRES bits of the Control Register is reached.

Setting this bit to a logic '0' (or changing it from '1' to '0') has no effect. Note that the acquisition sequence will be re-started every time that a byte written to the Command Register has the AQLEV bit set to a logic '1'.

The AQLEV bit will normally be set at the same time as an SFS (Search for Frame Sync) or SFSH/SFP (Search for Frame Sync + Header for MX919 / Search for Frame Preamble for MX929) task is initiated, however it may also be used independently to re-establish signal levels quickly after a long fade. Alternatively, a SFS or SFSH/SFP task may be written to the Command Register with the AQLEV bit at logic '0' if it is known that there is no need to re-establish the received signal levels. Refer to the Operational Information section of this publication for further details.

B5
B4
B3

These bits should each be set to a logic '0'.

B2
B1
B0
TASK

Task: Operations such as transmitting a data block are treated by the modem as 'Tasks'. Information on Task functions is given on the following pages.

A task is initiated when the µController writes a byte to the Command Register with the Task bits set to anything other than the 'NULL' ('0' '0' '0') code.

The µController should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status Register is a logic '0'.

Different tasks apply in receive and transmit modes.

TX Mode: All tasks other than NULL, RESET instruct the modem to transmit data from the Data Block Buffer, formatting it as required. For these tasks the µController should wait until the BFREE (Buffer Free) bit of the Status Register is a logic '1', before writing the data to the Data Block Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Block Buffer, byte number '0' of the block should be written first.

Once the byte containing the desired task has been written to the Command Register, the modem will: Set the BFREE (Buffer Free) bit of the Status Register to a logic '0', take the data from the Data Buffer as quickly as it can -transferring it to the Interleave Buffer for eventual transmission. (continued...)

Programming Information .....

Command Register

B2
B1
B0
TASK

Task: ..... This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer. Once all of the data has been transferred from the Data Block Buffer the modem will set the BFREE and IRQ bits of the Status Register to a logic '1', (causing the $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to a logic '1') to tell the µController that it may write new data and the next task to the modem.

In this way the µController can write a task -and the associated data- to the modem while the modem is still transmitting the data from the previous task.

RX Mode: The µController should wait until the BFREE bit of the Status Register is a logic '1', then write the desired task to the Command Register. Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE bit of the Status Register to a logic '0'.

Wait until enough received bits are in the De-Interleave Buffer.

Decode them as needed, and transfer any resulting data to the Data Block Buffer.

Then the modem will set the BFREE and IRQ bits of the Status Register to logic '1', (causing the $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to a logic '1') to tell the µController that it may read from the Data Buffer and write the next task to the modem.

In this way the µController can read data and write a new task to the modem while the received symbols needed for this new task are being stored in the De-Interleave Buffer.

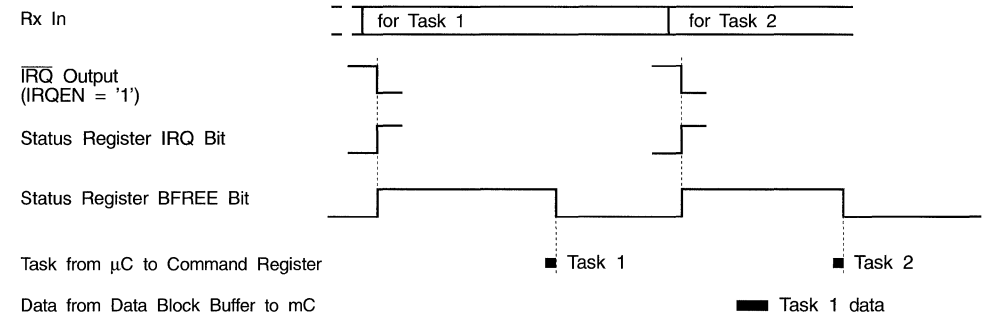


Figure 15 - The Receive Process

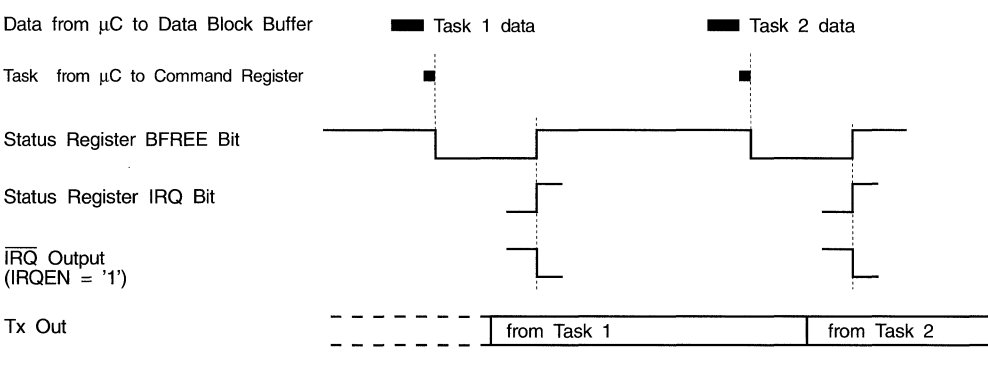


Figure 16 - The Transmit Process

Programming Information .....

Modem Tasks in Detail

The following tables describe the setting and format of the Command Register 'task' bits (bits 2, 1 and 0). Note that before a task is programmed the TX/RX bit in the Mode Register must be placed in the relevant position.

MX919 General Purpose Modem Tasks

Command Bits 2	1	0		Receive Mode		Transmit Mode
0	0	0	NULL	.. ..	NULL	.. ..
0	0	1	SFSH	Search for Frame Sync + Header	T24S	Transmit 24 Symbols
0	1	0	RHB	Read Header Block	THB	Transmit Header Block
0	1	1	RILB	Read Intermediate or Last Block	TIB	Transmit Intermediate Block
1	0	0	SFS	Search for Frame Sync	TLB	Transmit Last Block
1	0	1	R4S	Read 4 Symbols	T4S	Transmit 4 Symbols
1	1	0	NULL	.. ..	NULL	.. ..
1	1	1	RESET	Cancel any Current Action	RESET	Cancel any Current Action

Table 2 - MX919 Modem Task Details

MX929 RD-LAP Modem Tasks

Command Bits 2	1	0		Receive Mode		Transmit Mode
0	0	0	NULL	.. ..	NULL	.. ..
0	0	1	SFP	Search for Frame Preamble	T24S	Transmit 24 Symbols
0	1	0	RHB	Read Header Block	THB	Transmit Header Block
0	1	1	RILB	Read Intermediate or Last Block	TIB	Transmit Intermediate Block
1	0	0	SFS	Search for Frame Sync	TLB	Transmit Last Block
1	0	1	R4S	Read 4 Symbols	T4S	Transmit 4 Symbols
1	1	0	RSID	Read Station ID	TSID	Transmit Station ID
1	1	1	RESET	Cancel any Current Action	RESET	Cancel any Current Action

Table 3 - MX929 Modem Task Details

MX919 Modem Tasks

NULL **No Effect.** This task is provided so that an AQSC or AQLEV (Command Register) command can be initiated without loading a new task.

SFSH **Search for Frame Sync + Header Block.** Causes the MX919 to search the received signal for a valid 24-symbol Frame Sync sequence followed by a Header Block which has a correct CRC1 checksum.

This task continues until a valid Frame Sync + Header Block has been found.

The search consists of two stages:

1. The MX919 will attempt to match the incoming symbols against the General Purpose Modem Frame Synchronization pattern to within

MX929 Modem Tasks

NULL **No Effect.** This task is provided so that an AQSC or AQLEV (Command Register) command can be initiated without loading a new task.

SFP **Search for Frame Preamble.** Causes the MX929 to search the received signal for a valid RD-LAP Frame Preamble, consisting of a 24-symbol Frame Sync sequence followed by Station ID data which has a correct CRC0 checksum.

This task continues until a valid Frame Preamble has been found.

The search consists of four stages:

1. The MX929 will attempt to match the incoming symbols against the RD-LAP Frame Synchronization pattern

MX919 Modem Tasks

the tolerance defined by the Frame Sync Tolerance (FSTOL) bits of the Control Register.

2. Once a match has been found, the MX919 will read the next 66 symbols as if they were a 'Header' block, decoding the symbols and checking the CRC1 checksum. If the CRC1 checksum is incorrect the modem will resume the search, looking for a fresh Frame Sync pattern. If the CRC1 is correct, the 10 decoded data bytes will be placed into the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set high to a logic '1' and the CRC Checksum Error (CRCERR) bit cleared low to a logic '0'.

On detecting that the BFREE bit of the Status Register has gone to a logic '0', the µController should read the 10 bytes from the Data Block Buffer and then write the next task to the MX919's Command Register.

RHB **Read Header Block.** Causes the MX919 to read the next 66 symbols as a 'Header' block, decoding them, placing the resulting 10 data bytes and the 2 received CRC bytes into the Data Block Buffer, and setting the BFREE and IRQ bits of the Status Register high to a logic '1' when the task is complete to indicate that the µController may read the data from the Data Block Buffer and write the next task to the modem's Command Register.

The CRCERR bit of the Status Register will be set to a logic '1' or '0' depending on the validity of the received CRC1 checksum bytes.

MX929 Modem Tasks

to within the tolerance defined by the Frame Sync Tolerance (FSTOL) bits of the Control Register

2. Once a match has been found, the MX929 will read the next 'S' symbol, then update the SVAL bits of the Status Register and set the SRDY bit to '1'. (The IRQ bit of the Status Register will also be set to '1' at this time if the SSIEN bit of the Mode Register is '1'.)
3. The MX929 will then read the next 22 symbols as Station ID data. The 22 Station ID symbols will be decoded and the CRC0 checked. If this is incorrect the MX929 will resume the search, looking for a fresh Frame Sync pattern.
4. If the received CRC0 is correct, the next 'S' symbol will be read, the SVAL bits of the Status Register updated and the SRDY, BFREE and IRQ bits set to a logic '1'. The CRC Checksum Error (CRCERR) bit will be cleared to a logic '0', and the three decoded Station ID bytes placed into the Data Block Buffer.

On detecting that the BFREE bit of the Status Register has gone to a logic '1', the µController should read the 3 Station ID bytes from the Data Block Buffer and then write the next task to the MX929's's Command Register.

RHB **Read Header Block.** Causes the MX929 to read the next 69 symbols as a 'Header' block. It will strip out the 'S' symbols, then de-interleave and decode the remaining 66 symbols, placing the resulting 10 data bytes into the Data Block Buffer. It also sets the BFREE and IRQ bits of the Status Register to a logic '1' when the task is complete to indicate that the µController may read the data from the Data Block Buffer and write the next task to the modem's Command Register.

The CRCERR bit of the Status Register will be set to a logic '1' or '0' depending on

Programming Information .....

MX919 Modem Tasks

RILB **Read 'Intermediate' or 'Last' Block.** Causes the modem to read the next 66 symbols as an 'Intermediate' or 'Last' block (the µController should be able to tell from the received 'Header' block how many blocks are in the frame, and hence when to receive the 'Last' block).

In each case, the modem will decode the 66 symbols and place the resulting 12 bytes into the Data Block Buffer, setting the BFREE and IRQ bits of the Status Register high to a logic '1' when the task is complete to indicate that the µController may read the data from the Data Block Buffer and write the next task to the modem's Command Register. If an 'Intermediate Block is received then the µController should read-out all 12 bytes from the Data Block Buffer and ignore the CRCERR bit of the Status Register, for a 'Last' block the µController need only read the first 8 bytes from the Data Block Buffer, and the CRCERR bit in the Status Register will reflect the validity of the received CRC2 checksum. Note that in the RX mode the CRC2 checksum circuits are initialized on completion of any task other than NULL or RILB.

MX929 Modem Tasks

the validity of the received CRC1 checksum bytes.

As each of the 3 'S' symbols of a block is received, the SVAL bits of the Status Register will be updated and the SRDY bit set to '1'. (If the SSIEN bit of the Mode Register is '1' the Status Register IRQ bit will also be set to '1'.)

RILB **Read 'Intermediate' or 'Last' Block.** Causes the modem to read the next 69 symbols as an 'Intermediate' or 'Last' block (the µController should be able to tell from the received 'Header' block how many blocks are in the frame, and hence when to receive the 'Last' block).

In each case, the MX929 will strip out the 3 'S' symbols, de-interleave and decode the remaining 66 symbols and place the resulting 12 bytes into the Data Block Buffer. The BFREE and IRQ bits of the Status Register are set to a logic '1' when the task is complete to indicate that the µController may read the data from the Data Block Buffer and write the next task to the MX929's Command Register.

If an 'Intermediate Block is received then the µController should read all 12 bytes from the Data Block Buffer and ignore the CRCERR bit of the Status Register. For a 'Last' block the µController needs only to read the first 8 bytes from the Data Block Buffer, and the CRCERR bit in the Status Register will reflect the validity of the received CRC2 checksum. Note that in the RX mode the CRC2 checksum circuits are initialized on completion of any task other than NULL or RILB.

As each of the 3 'S' symbols of a block is received, the SVAL bits of the Status Register will be updated and the SRDY bit set to '1'. (If the SSIEN bit of the Mode Register is '1' the Status Register IRQ bit will also be set to '1'.) Note that when the third 'S' symbol is received the SRDY bit will be set to '1' at the same time the BFREE bit is set to '1'.

Programming Information .....

MX919 Modem Tasks

SFS **Search for Frame Sync.** Causes the MX919 to search the received signal for a 24-symbol sequence which matches the Frame Synchronization pattern to within the tolerance defined by the FSTOL bits of the Mode Register.

When a match is found the modem will set the BFREE and IRQ bits of the Status Register high to a logic '1' to indicate to the µController that it should write the next task to the Command Register.

R4S **Read 4 Symbols.** This task is intended for special tests and channel monitoring - perhaps preceded by an SFS task. Causes the modem to read the next 4 symbols and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Block Buffer. The BFREE and IRQ bits of the Status Register will then be set high to a logic '1' to indicate that the µController may read the data byte from the Data Block Buffer and write the next task to the Command Register.

MX929 Modem Tasks

SFS **Search for Frame Sync.** This task is intended for special test and channel monitoring purposes. It performs the first two parts of an SFP task.

SFS causes the MX929 to search the received signal for a 24-symbol sequence which matches the RD-LAP Frame Synchronization pattern to within the tolerance defined by the FSTOL bits of the Mode Register.

When a match is found the MX929 will read the following 'S' symbol, then set the BFREE, IRQ and SRDY bits of the Status Register to a logic '1' and update the SVAL bits. The µController may then write the next task to the Command Register.

R4S **Read 4 Symbols.** This task is intended for special test and channel monitoring purposes, perhaps preceded by an SFS task. It causes the MX929 to read the next 4 symbols and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Block Buffer. The BFREE and IRQ bits of the Status Register will then be set to a logic '1' to indicate that the µController may read the data byte from the Data Block Buffer and write the next task to the Command Register.

RSID **Read Station ID.** This task causes the MX929 to read and decode the next 23 symbols as Station ID data followed by an 'S' symbol. It is similar to the last two parts of an SFP task except that it will not re-start if the received CRC0 is incorrect. It normally follows an SFS operation.

The decoded System, Domain and Base ID bytes will be placed into the Data Buffer, and the CRCERR bit of the Status Register will be set to '1' if the received CRC0 is incorrect. Otherwise it will be cleared to '0'. The SVAL bits of the Status Register will be updated and the BFREE, SRDY and IRQ bits will be set to '1' to indicate that the µC may read the 3 Station ID bytes from the Data Block Buffer and write the next task to the MX929's Command Register.

Programming Information .....

MX919 Modem Tasks

T24S **Transmit 24 Symbols.** This task, which is intended to facilitate the transmission of Symbol and Frame Sync patterns as well as special test sequences, takes 6 bytes of data from the Data Block Buffer and transmits them as 24 4-level symbols without any CRC or FEC.

Byte '0' of the Data Block Buffer is sent first, byte '5' last.

Once the modem has has read all the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set high to a logic '1', indicating to the µController that it may write the next task and its data to the modem.

Table 4 shows what data has to be written to the Data Block Buffer to transmit the modem Symbol and Frame Sync Sequences.

THB **Transmit Header Block.** Takes 10 bytes of data (Address & Control) from the Data Block Buffer, calculates and appends the 2-byte CRC1 checksum, translates the result to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Header' Block.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set high to a logic '1', indicating to the µController that it may write the next task and its data to the modem.

TIB **Transmit Intermediate Block.** Takes 12 bytes of data from the Data Block Buffer, updates the 4-byte CRC2 checksum for inclusion in the 'Last' block, translates the 12 data bytes to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Intermediate' Block. Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set high to a logic '1', indicating to the µController that it may write the next task and its data to the modem.

Note that in TX mode the CRC2 checksum circuits are initialized on completion of any

MX929 Modem Tasks

T24S **Transmit 24 Symbols.** This task, which is intended to facilitate the transmission of Symbol and Frame Sync patterns as well as special test sequences, takes 6 bytes of data from the Data Block Buffer and transmits them as 24 4-level symbols without any CRC or FEC, interleaving or adding any 'S' symbols.

Byte '0' of the Data Block Buffer is sent first, byte '5' last.

Once the MX929 has has read all the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating to the µController that it may write the next task and its data to the modem.

Table 5 shows what data has to be written to the Data Block Buffer to transmit the modem Symbol and Frame Sync Sequences.

THB **Transmit Header Block.** Takes 10 bytes of data (Address & Control) from the Data Block Buffer, calculates and appends the 2-byte CRC1 checksum, translates the result to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Header' Block, inserting 'S' symbols at 22-symbol intervals.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating to the µController that it may write the next task and its data to the modem.

TIB **Transmit Intermediate Block.** Takes 12 bytes of data from the Data Block Buffer, updates the 4-byte CRC2 checksum for inclusion in the 'Last' block, translates the 12 data bytes to 4-level symbols (with FEC), interleaves the symbols and transmits the result as an RD-LAP formatted 'Intermediate' Block, inserting 'S' symbols at 22-symbol intervals.

Once the MX929 has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating to the

MX919 Symbol and Frame Sync Sequences

'Symbol Sync' Symbols	Values written to Data Block Buffer		
		Binary	Hex
+3 +3 -3 -3	Byte 0 :	11110101	F5
+3 +3 -3 -3	Byte 1 :	11110101	F5
+3 +3 -3 -3	Byte 2 :	11110101	F5
+3 +3 -3 -3	Byte 3 :	11110101	F5
+3 +3 -3 -3	Byte 4 :	11110101	F5
+3 +3 -3 -3	Byte 5 :	11110101	F5

'Frame Sync' Symbols	Values written to Data Block Buffer		
		Binary	Hex
-1 +1 -1 +1	Byte 0 :	00100010	22
-1 +3 -3 +3	Byte 1 :	00110111	37
-3 -1 +1 -3	Byte 2 :	01001001	49
+3 +3 -1 +1	Byte 3 :	11110010	F2
-3 -3 +1 +3	Byte 4 :	01011011	5B
-1 -3 +1 +3	Byte 5 :	00011011	1B

Table 4 - MX919 Symbol and Frame Sync Sequences (T24S)

MX929 Symbol and Frame Sync Sequences

'Symbol Sync' Symbols	Values written to Data Block Buffer		
		Binary	Hex
+3 +3 -3 -3	Byte 0 :	11110101	F5
+3 +3 -3 -3	Byte 1 :	11110101	F5
+3 +3 -3 -3	Byte 2 :	11110101	F5
+3 +3 -3 -3	Byte 3 :	11110101	F5
+3 +3 -3 -3	Byte 4 :	11110101	F5
-3 -3 +3 +3	Byte 5 :	01011111	5F

'Frame Sync' Symbols	Values written to Data Block Buffer		
		Binary	Hex
-1 +1 -1 +1	Byte 0 :	00100010	22
-1 +3 -3 +3	Byte 1 :	00110111	37
-3 -1 +1 -3	Byte 2 :	01001001	49
+3 +3 -1 +1	Byte 3 :	11110010	F2
-3 -3 +1 +3	Byte 4 :	01011011	5B
-1 -3 +1 +3	Byte 5 :	00011011	1B

Table 5 - MX929 Symbol and Frame Sync Sequences (T24S)

Programming Information .....

MX919 Modem Tasks

task other than NULL, TIB or TLB.

TLB **Transmit 'Last' Block.** Takes 8 bytes of data from the Data Block Buffer, updates and appends the 4-byte CRC2 checksum, translates the resulting 12-bytes to 4-level symbols with (FEC), interleaves the symbols and transmits the result as a formatted 'Last' Block. Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set high to a logic '1', indicating to the µController that it may write the next task and its data to the modem.

T4S **Transmit 4 Symbols.** This task is similar to T24S but takes only one byte from the Data Block Buffer, transmitting it as four 4-level symbols.

RESET **RESET.** Stop any current action. This 'task' takes effect immediately, and terminates any current action (task , AQSC or AQLEV) the modem may be performing and sets the BFREE bit of the Status Register high to a logic '1', without setting the IRQ bit. RESET should be used to set the modem into a known state when V_{DD} is applied.

Note that due to delays in the transmit filter, it will take several symbol-times for any change to become apparent at the TXOp pin.

MX929 Modem Tasks

µController that it may write the next task and its data to the modem.

Note that in TX mode the CRC2 checksum circuits are initialized on completion of any task other than NULL, TIB or TLB.

TLB **Transmit 'Last' Block.** Takes 8 bytes of data from the Data Block Buffer, updates and appends the 4-byte CRC2 checksum, translates the resulting 12-bytes to 4-level symbols with (FEC), interleaves the symbols and transmits the result as an RD-LAP formatted 'Last' Block, inserting 'S' symbols at 22-symbol intervals.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating to the µController that it may write the next task and its data to the modem.

T4S **Transmit 4 Symbols.** This task is similar to T24S but takes only one byte from the Data Block Buffer, transmitting it as four 4-level symbols.

TSID **Transmit Station ID.** This task takes 3 ID bytes from the Data Block Buffer, calculates and appends the 6-bit CRC0 checksum, translates the result to 4-level symbols (with FEC) and transmits the resulting 22 symbols preceded and followed by 'S' symbols.

RESET **RESET.** Stop any current action. This 'task' takes effect immediately, and terminates any current action (task , AQSC or AQLEV) the MX929 may be performing and sets the BFREE bit of the Status Register high to a logic '1', without setting the IRQ bit. RESET should be used to set the modem into a known state when V_{DD} is applied.

Note: due to delays in the transmit filter, it will take several symbol-times for any change to become apparent at the TXOp pin.

Programming Information .....

RRC Filter Delay

The Task Timing figures detailed in Tables 6 and 7 are based upon: the signal at the input to the RRC Filter in the transmit mode, or the signal at the input to the de-interleave circuits in the receive mode. As can be seen from the diagram in Figure 17, there is an additional delay of approximately 8 (eight) symbol-times in both TX and RX modes due to the (TX/RX) RRC Filter.

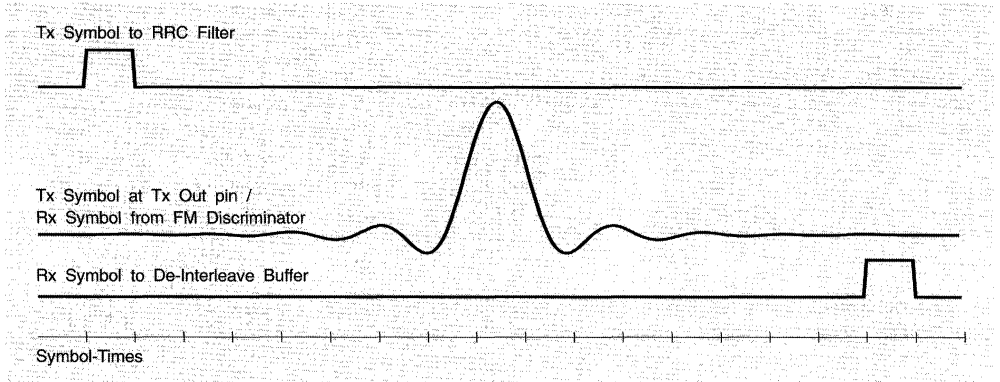


Figure 17 - Examples of Filter Delay Times

Transmit and Receive Task Timing

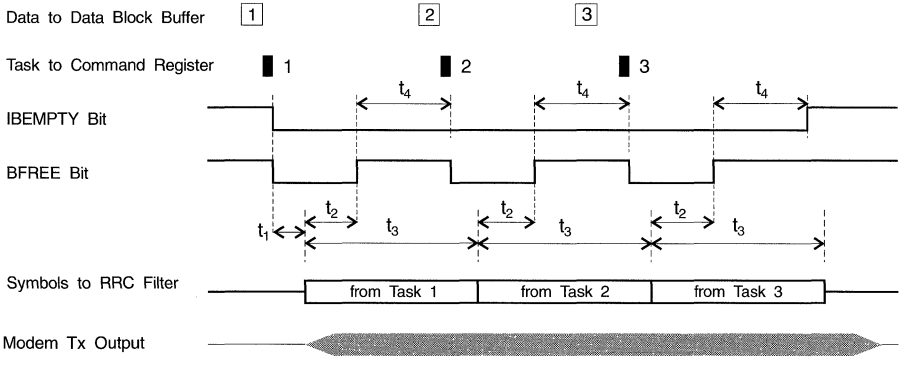


Figure 18 - MX919/929 TX Task Timing Diagram

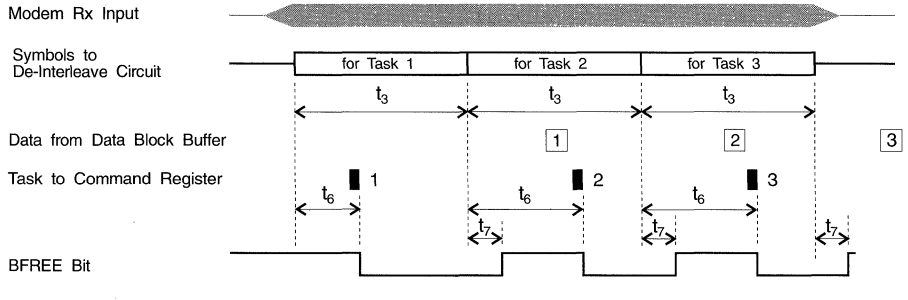


Figure 19 - MX919/929 RX Task Timing Diagram

Timing	MX919 Timing Notes	Task	Typical (Symbol) Time
t_1	Modem in idle state. Time from writing first task to the application of the first TX symbol to the RRC Filter.	Any	1
t_2	Time from the application of the first symbol of the task to the RRC Filter until BFREE goes to a logic '1' (high).	T24S/TSID THB/TIB/TLB T4S	5 16 1
t_3	Time to transmit all symbols of the task. or Time to receive all symbols of the task	T24S THB/TIB/TLB RHB/RILB T4S SFS SFSH R4S	24 66 66 4 <24 <90 4
t_4	Maximum time allowed from BFREE going to a logic '1' for the next task (and data) to be written to the modem.	T24S THB/TIB/TLB T4S	18 49 2
t_6	Maximum time between the first symbol of the task entering the de-interleave circuit and the task being written to the modem.	SFSH RHB/RILB SFS R4S	21 49 21 3
t_7	Time from last symbol of task entering the de-interleave circuit to BFREE going to a logic '1'.	Any	1

Table 6 - Typical RX/TX Task Load Timings (MX919)

Timing	MX929 Timing Notes	Task	Typical (Symbol) Time
t_1	Modem in idle state. Time from writing first task to the application of the first TX symbol to the RRC Filter.	Any	1
t_2	Time from the application of the first symbol of the task to the RRC Filter until BFREE goes to a logic '1' (high).	T24S/TSID THB/TIB/TLB T4S	5 16 1
t_3	Time to transmit all symbols of the task. or Time to receive all symbols of the task	T24S/TSID THB/TIB/TLB RSID RHB/RILB T4S/R4S SFP SFS	24 69 23 69 4 <48 <25
t_4	Maximum time allowed from BFREE going to a logic '1' for the next task (and data) to be written to the modem.	T24S THB/TIB/TLB TSID T4S	18 52 18 2
t_6	Maximum time between the first symbol of the task entering the de-interleave circuit and the task being written to the modem.	SFP/SFS RHB/RILB RSID R4S	21 51 15 3
t_7	Time from last symbol of task entering the de-interleave circuit to BFREE going to a logic '1'.	Any	1

Table 7 - Typical RX/TX Task Load Timings (MX929)

Programming Information .....

Control Register

This 8-bit write-only register controls the modem's symbol-rate, the response times of the receive clock extraction and signal level measurement circuits and the Frame Sync pattern recognition tolerance.

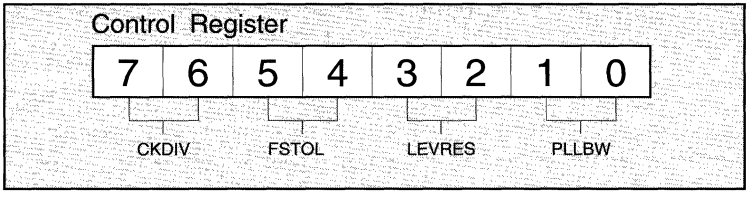


Figure 20 - The Control Register

1

Control Register

Table 8 shows how bit-rates of 2400/4800/9600 symbols per second may be obtained from common Xtal/clock frequencies. The values of C_3 and C_4 should be suitable for the frequency of the Xtal X_1. For $X_1 < 5.0$MHz, $C_3 = C_4 = 33.0$pF; for $X_1 > 5.0$MHz, $C_3 = C_4 = 18.0$pF.

B7, B6 CKDIV

Clock Division Ratio: These bits control a frequency divider driven from the clock signal present at the Xtal pin; this ratio and Xtal input will determine the nominal bit-rate.

			Xtal Frequency (MHz)		
			2.4576	4.9152	9.8304
		Division Ratio Xtal Freq.	Symbol Rate (symbols/sec.)		
B7	B6	Symbol Rate			
0	0	512	4800	9600	
0	1	1024	2400	4800	9600
1	0	2048		2400	4800
1	1	4096			1200

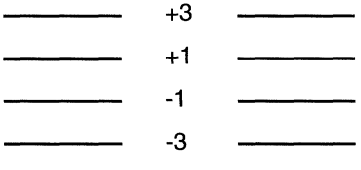
Table 8 - Clock/Data Rates ***Note*** *that device operation is not guaranteed or specified above 9,600symbols/s or below 2,400symbols/s*

B5, B4 FSTOL

Frame Sync Tolerance: For use in the RX mode only; these bits have no effect in the RX mode. These bits define the maximum number of mismatches which will be allowed during a search for the Frame Sync pattern:

B5	B4	Mismatches Allowed
0	0	0
0	1	2
1	0	4
1	1	6

Note that a single 'mismatch' is defined as the difference between two adjacent symbol levels; if the symbol '+1' were expected, then the received symbol values of '+3' and '-1' would count as 1 mismatch, a received symbol value of '-3' would count as 2.



Symbol Levels

Programming Information .....

Control Register .....

B3, B2 LEVRES

Level Measurement Response Time: These bits are only used in the RX mode and have no effect in the TX mode; they set the 'normal' response time of the RX signal amplitude and dc offset measuring circuits. This setting will be temporarily overriden by the automatic sequencing of an AQLEV command.
For most general-purpose applications using this modem, these bits should normally be set to 'Peak Averaging', except when the µController detects a receive signal fade, when 'Hold' should be selected. The 'Peak Detect' setting is intended for systems where the µController cannot detect signal fades or the start of a received message; this setting allows the modem to respond quickly to fresh messages and recover rapidly after a fade without µController intervention -this however will be at the cost of reduced Bit-Error-Rate vs Signal-to-Noise performance.
The Signal Average setting is a test mode and should not normally be used.
Note that as the measured levels are stored on capacitors C_6 and C_7 via pins Doc 1 and Doc 2, these levels will decay gradually towards V_{BIAS} when the 'Hold' setting is used; the discharge time-constant is approximately 1000 symbol-times.
Table 9 details the bit-setting application.

B3	B2	Setting	Action
0	0	Hold	Keep current values of amplitude and offset
0	1	Peak Averaging	Track input signal using bit peak averaging
1	0	Peak Detect	Track input signal using peak detection
1	1	Signal Average	Measure average signal level

Table 9

B1, B0 PLLBW

PLL Bandwidth: For use in the RX mode only (no effect in TX).
In the receive mode these two bits set the 'normal' bandwidth of the RX Clock Extraction Phase Locked Loop circuit. This setting will be temporarily overridden by the automatic sequence of an AQSC (Command Register Bit 7) command.

B1	B0	PLL Bandwidth (±ppm)	Note
0	0	0 (Hold)	For use during signal fades
0	1	30	
1	0	250	
1	1	50,000	

Table 10

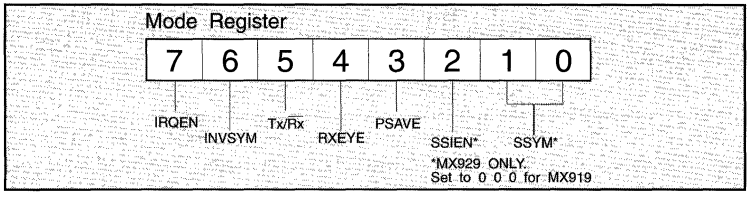
The 'Hold' setting is intended for use during signal fades otherwise the minimum bandwidth consistent with the RX and TX modem symbol-rate tolerances should be chosen, i.e. if the Xtals used with both modems have accuracies of ±100ppm, the PLLBW bits (B1, B0) should be set to '1', '0'.
The very wide bandwidth ('1', '1') is intended for systems where the µController cannot detect signal fades or the start of a receive message; it allows the modem to respond rapidly to fresh messages and recover rapidly after a fade without µController intervention. This action however is at the expense of reduced Bit-Error-Rate vs Signal-to-Noise performance.
Note that PLL bandwidth figures are intended for 'a reasonably random received signal.'

Programming Information .....

Mode Register

This 8-bit write-only register controls the basic operating modes of the modem.

Figure 21 - The Mode Register



1

Mode Register

B7 IRQEN

IRQ Output Enable: When set to a logic '1' the Interrupt Request output will low (logic '0') whenever the IRQ bit (BIT 7) of the Status Register is set by the modem to a logic '1'. When set to a logic '0' the Interrupt Request output will not function and will remain in its high-impedance state (see Pin Functions and Figure 11 - µController Interface).

B6 INVSYM

Invert Symbols: Controls the polarity (sense) inversion of transmitted and received symbol voltages.

B6	Symbol	Signal at TX Out	Signal at RX Feedback
'0'	'+3'	above V_{BIAS}	below V_{BIAS}
'0'	'-3'	below V_{BIAS}	above V_{BIAS}
'1'	'+3'	below V_{BIAS}	above V_{BIAS}
'1'	'-3'	above V_{BIAS}	below V_{BIAS}

B5 TX/RX

TX/$\overline{RX}$ Mode: When set to a logic '1' places the modem in the Transmit mode; when set to a logic '0' places the modem in the Receive mode. Note that changing between Transmit and Receive modes will cancel any current task.

B4 RX Eye

Show RX Eye: This bit should be set to a logic '0' for normal RX operation and always for TX operation. Setting this bit to a logic '1' in the receive mode configures the modem into a special test mode, in which the input to the TX Output Buffer is connected to the RX Symbol/Clock Extraction circuit at a point which carries the equalized receive signal. This may be monitored with an oscilloscope (at the TX Out pin *before* the external RC filter), to assess the quality of the complete radio channel including the TX and RX modem filters, the TX modulator and the RX IF filters and FM demodulator. The resulting 'eye' diagram (for reasonably random data) should ideally be as shown in Figure 7, with 4 'crisp' and equally spaced crossings.

B3 PSAVE

Powersave: When set to a logic '1' places the modem in its Powersave mode. In this mode the following circuits only are disabled: Internal Filters, RX Symbol and Clock Extraction Circuits and the TX Output Buffer; the TX Out pin is connected to V_{BIAS} through a high-value resistance. Xtal oscillator circuits and the µController Interface logic and the RX Input Amplifier continue to operate. Note that RX clock and levels will be lost if Powersave mode is selected.
Setting to a logic '0' restores power to all of the device circuitry and the modem is in its operational mode. Note that the internal filters -and hence the TX Out pin in the TX mode- will take about 20 symbol-times to settle after this bit is taken from a logic '1' to '0'.

B2 SSIEN (MX929)

'S' Symbol IRQ Enable (MX929 only): **In Receive mode**, setting this bit to '1' causes the IRQ bit of the Status Register to be set to '1' whenever a new 'S' symbol has been received. (The SRDY bit of the Status Register will be set to '1' at the same time, and the SVAL bits updated to reflect the received 'S' symbol.) **In Transmit mode**, setting this bit to '1' causes the IRQ bit of the Status Register to be set to '1' whenever an 'S' symbol has been transmitted. (The SRDY bit of the Status Register will be set to '1' at the same time).
On the MX919, this bit should always be set to a logic '0'.

B1, B0 SSYM (MX929)

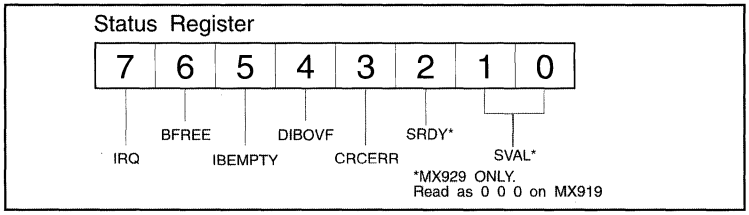
'S' Symbol to be Transmitted (MX929 only): For the MX929, these bits have no effect in RX mode. **In Transmit mode**, these bits define the next 'S' symbol to be transmitted.
On the MX919, these bits should always be set to a logic '0'.

Programming Information .....

Status Register

This register may be read by the µController to determine the current state of the modem.

Figure 22 - The Status Register



Status Register

B7 IRQ

Interrupt Request: This bit is set to a logic '1' by:

The Status Register BFREE bit going from a logic '0' to '1', unless this transition is caused by a RESET Task or by a change to the Mode Register's PSAVE or TX/RX bits.

or

The Status Register IBEMPTY bit going from a logic '0' to '1', unless this transition is caused by a RESET Task or by a change to the Mode Register's PSAVE or TX/RX bits.

or

The Status Register DIBOVF bit going from a logic '0' to '1'.

This (IRQ) bit is cleared to a logic '0' immediately after a read of the Status Register.
If the IRQEN bit of the Mode Register is a logic '1', the MX919/929 $\overline{IRQ}$ output pin will be pulled low (to V_{SS}) whenever the Status Register IRQ bit is a logic '1'.

B6 BFREE

Data Block Buffer Free: BFREE reflects the availability of the Data Block Buffer; BFREE is cleared to a logic '0' *(Buffer NOT Free)* whenever a task other than NULL or RESET is written to the Command Register.
In Transmit mode, the BFREE bit will be set to a logic '1' (also setting the Status Register IRQ bit to a logic '1) when the modem is ready for the µController to write new data to the Data Block Buffer and the next task to the Command Register.
In Receive mode, the BFREE bit is set to a logic '1' (also setting the Status Register IRQ bit to a logic '1) by the modem when it has completed a task and any data associated with that task has been placed into the Data Block Buffer. The µController may then read that data and write the next task to the Command Register.
The BFREE bit is also set to a logic '1' -but without setting the IRQ bit- by a RESET task or when the Mode Register PSAVE or TX/RX bits are changed.

B5 IBEMPTY

Interleave Buffer Empty: In Transmit mode, IBEMPTY is set to a logic '1' (also setting the IRQ bit) when less than two symbols remain in the Interleave Buffer or the Interleave Buffer is empty. Any transmit task written to the modem after IBEMPTY goes to a logic '1' will be too late to avoid a gap in the transmit output signal (see Figure 18 and Tables 6 & 7, TX Task Timing)
IBEMPTY is also set to a logic '1' by a RESET task and by a change of the Mode Register PSAVE or TX/RX bits, but in these cases the IRQ bit will not be set.
IBEMPTY is cleared to a logic '0' within 1-symbol time after a task other than NULL or RESET is written to the Command Register.
Note that when the modem is in the transmit mode and the Interleave Buffer is empty, a mid-level (half-way between '+1' and '-1') will be fed to the RRCFilter.
In Receive mode this bit is a logic '0'.

Programming Information .....

Status Register .....

B4 DIBOVF	**De-Interleave Buffer Overflow: In Receive mode** DIBOVF is set to a logic '1' (also setting the IRQ bit) when an RHB, RILB, RSID or R4S task is written to the Command Register too late to allow continuous reception (see Figure 19 and Tables 6 & 7, RX Task Timing). DIBVOF is cleared to a logic '0' by reading the Status Register, by writing a RESET task to the Command Register or by changing the PSAVE or TX/RX bits of the Mode Register. **In Transmit mode** this bit is a logic '0'.
B3 CRCERR	**CRC Checksum Error: In Receive mode** CRCFEC will be updated at the end of an SFSH, RHB, or RILB task to reflect the result of the receive CRC check. A logic '0' indicates that the CRC was received correctly. A logic '1' indicates that an error is present. Note that this bit should be ignored when an 'Intermediate' block (which does not have an integral CRC) is received. CRCERR is cleared to a logic '0' by a RESET task, or by changing the PSAVE or TX/RX bits of the Mode Register. **In Transmit mode** this bit is a logic '0'.
B2 SRDY (MX929)	**'S' Symbol Ready (MX929 only): In Receive mode**, this bit is set to '1' whenever an 'S' symbol has been received. The µC may then read the value of the symbol from the SVAL field of the Status Register. **In Transmit mode**, this bit is set to '1' whenever an 'S' symbol has been transmitted. The bit is cleared to '0' by a read of the Status Register, by a RESET task or by changing the PSAVE or TXRXN bits of the Mode Register. **On the MX919**, this bit should always be set to a logic '0'.
B1, B0 SVAL (MX929)	**Received 'S' Symbol Value (MX929 only): In Receive mode**, these bits reflect the value of the latest received 'S' symbol. **In Transmit mode**, these bits will be '0'. **On the MX919**, these bits should always be set to a logic '0'.

The Data Quality Register

In Receive Mode, the modem continuously measures the quality of the received signal by comparing the actual received waveform over the previous 64 symbol times against an internally generated "ideal". The result is placed into bits 3 to 7 of the Data Quality Register for the µController to read at any time, bits 0 to 2 being always set to '0'. Figure 22 shows how the value (0 to 255) read from the Data Quality Register varies with the received signal-to-noise ratio. In Transmit Mode all bits are set to a logic '0'.

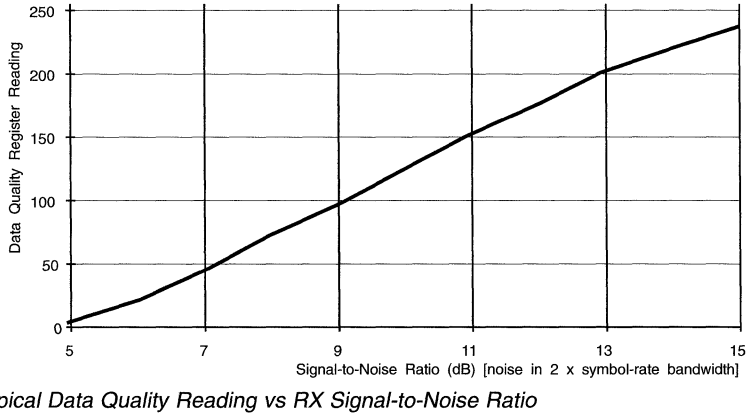


Figure 22 - Typical Data Quality Reading vs RX Signal-to-Noise Ratio

Programming Information .....

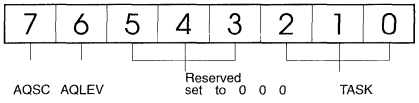
MX919 & MX929 Modem Register Selection

The following diagram is a quick-reference to MX919/MX929 register allocations. The MX919/MX929 modem appears to the programmer as 4 write-only 8-bit registers shadowed by 3 read-only registers. Individual registers are selected by the A_1 and A_0 inputs.

Register Selection

Write to Modem	A_1	A_0	Read from Modem
Data Block Buffer	0	0	Data Block Buffer
Command Register	0	1	Status Register
Control Register	1	0	DQ Register
Mode Register	1	1	not used

Command Register

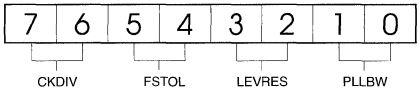


AQSC - Acquire Symbol Clock
AQLEV - Acquire Receive Signal Levels
TASK:

B2	B1	B0	RX Mode	
0	0	0	NULL	
0	0	1	SFSH	Search For Frame Sync + Head
0	1	0	RHB	Read Header Block
0	1	1	RILB	Read Intermediate or Last Block
1	0	0	SFS	Search For Frame Sync
1	0	1	R4S	Read 4 Symbols
1	1	0	NULL	
1	1	1	RESET	Cancel any Current Action

B2	B1	B0	TX Mode	
0	0	0	NULL	
0	0	1	T24S	Transmit 24 Symbols
0	1	0	THB	Transmit Header Block
0	1	1	TIB	Transmit Intermediate Block
1	0	0	TLB	Transmit Last Block
1	0	1	T4S	Transmit 4 Symbols
1	1	0	NULL	
1	1	1	RESET	Cancel any Current Action

Control Register



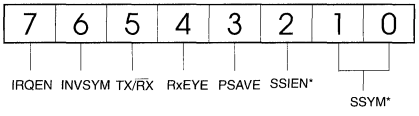
CKDIV - Clock Division Ratio
FSTOL - Frame Sync Tolerance
LEVRES - Level Measurement Response Time

B3	B2	
0	0	Hold
0	1	Peak Averaging
1	0	Peak Detect
1	1	Signal Average

PLLBW - PLL Bandwidth

B1	B0	Bandwidth (+/-ppm)
0	0	0 (Hold)
0	1	30
1	0	250
1	1	50,000

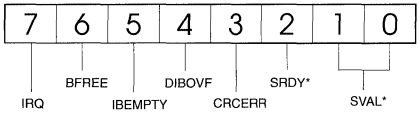
Mode Register



IRQEN - IRQ Output Enable
INVSYM - Invert Symbol
TX/RX - Transmit or Receive Mode
RXEYE - Show RX Eye
PSAVE - Powersave
*SSIEN - S Symbol IRQ Enable (MX929 only)
*SSYM - S Symbol to TX (MX929 only)

*Bits 2, 1 and 0 are all set to '0' for MX919

Status Register



IRQ - Interrupt Request
BFREE - Data Block Buffer Free
IBEMPTY - Interleave Buffer Empty
DIBOVF - De-Interleave Buffer Overflow
CRCERR - CRC Checksum Error
*SRDY - S Symbol Ready (MX929 only)
*SVAL - Received S Symbol Value (MX929 only)

*Bits 2, 1 and 0 are all held to '0' for MX919

Data Block Buffer A 12-byte read/write buffer used to hold and transfer receive or transmit data to or from the controlling µController.

DQ (Data Quality) Register The information presented in this 8-bit register is intended to indicate the 'quality' of the received signal.

Figure 23 - Ready-Use Guide to Register Functions

Operational Information

MX919/929 "Transmit Frame" Example

The operations needed to transmit a single Frame consisting of Symbol and Frame Sync sequences and one each Header, Intermediate and Last blocks are shown in Figure 24 (below).

MX919 out of Powersave Set to TX Interrupt Enable as required RXEYE disabled Invert Symbol as required	V_{DD} Applied; Task = RESET; Device Powersaved CKDIV as required Mode PSAVE = '0' TX/RX '1' IRQEN = 'X' RXEYE = '0' INVSYM = 'X'
Ensure Data Block Buffer is FREE	Status BFREE = '1'
Write 6 Symbol Sync bytes to Data Block Buffer	Data Block Buffer Write 6 Bytes
Transmit 24 Symbols	Command (task) T24S
Wait Interrupt - Interrupt occurs - Read Status Register	Status IRQ = '1' BFREE = '1'
Write 6 Frame Sync bytes to Data Block Buffer	Data Block Buffer Write 6 Bytes
Transmit 24 Symbols	Command (task) T24S
Wait Interrupt - Interrupt occurs - Read Status Register	Status IRQ = '1' BFREE = '1'
MX929 Only: Write 3 Station ID bytes to the Data Block Buffer and a TSID task to the Command Register	Data Block Buffer Write 3 Bytes
MX929 only: Wait Interrupt - Interrupt occurs - Read Status Register	Status IRQ = '1' BFREE = '1'
Write 10 Header Block bytes to Data Block Buffer	Data Block Buffer Write 10 Bytes
Transmit Header Block	Command (task) THB
Wait Interrupt - Interrupt occurs - Read Status Register	Status IRQ = '1' BFREE = '1'
Write 12 Intermediate Block bytes to Data Block Buffer	Data Block Buffer Write 12 Bytes
Transmit Intermediate Block	Command (task) TIB
Wait Interrupt - Interrupt occurs - Read Status Register	Status IRQ = '1' BFREE = '1'
Write 8 Last Block bytes to Data Block Buffer	Data Block Buffer Write 8 Bytes
Transmit Last Block	Command (task) TLB
Wait Interrupt - Interrupt occurs - Read Status Register	Status IRQ = '1' BFREE = '1'
Wait another Interrupt - Interrupt occurs - Read Status Register	Status IRQ = '1' BFREE = '1' IBEMPTY = '1'

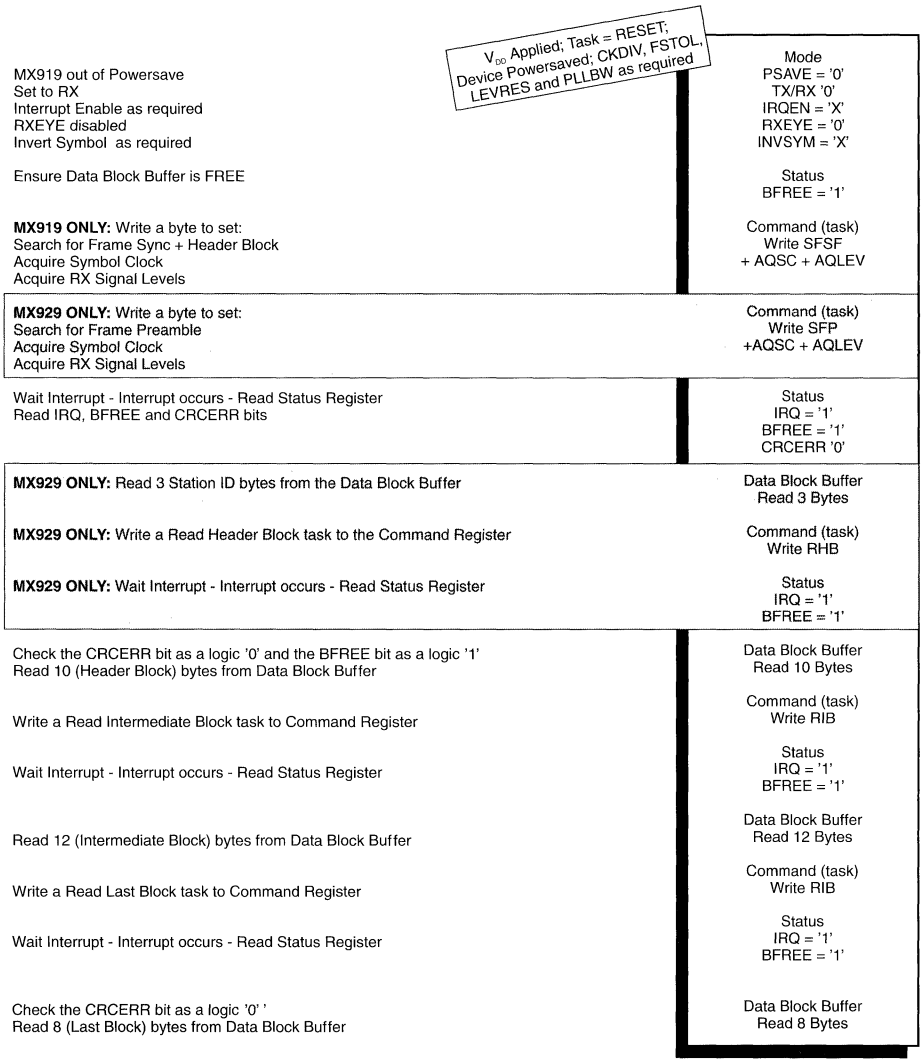
NOTE: The final symbol of the frame will appear at the TX OUT pin approximately 8 symbol-times after the Status Register IBEMPTY bit goes to a logic '1'; a further 16 symbol-times should be allowed for a symbol to pass completely through the RRC Filter.

NOTE: MX929 Only: The SSYM bits of the Mode Register may be altered at any time to change the transmitted 'S' symbols. If a timing reference is required, then setting the Mode Register SSIEN bit to '1' will cause a µC interrupt after every 'S' symbol transmitted - in which case the µC will have to distinguish between interrupts caused by the BFREE bit going to '1', and those caused by the SRDY bit being set to '1'.

Figure 24 - MX919/929 "Transmit Frame" Example

Operational Information .....

MX919/929 "Receive Frame" Example



NOTE: MX929 ONLY: The value of the latest 'S' symbol received will be contained in the SVAL bits each time the Status Register is read. If desired, the Mode Register SSIEN bit may be set to '1', which will cause a µC interrupt after every 'S' symbol is received - in which case the µC will have to distinguish between interrupts caused by the BFREE bit going to '1', and those caused by the SRDY bit being set to '1'.

Figure 25 - MX919/929 "Receive Frame" Example

Operational Information .....

Operation Details

Forward Error Correction

Header/Intermediate/Last Block FEC

Transmit Mode, the MX919/929 translates the 96 bits of the block (12 bytes) into 66 4-level symbols as follows:

The 12 bytes are divided into 32 groups of three bits each (called tri-bits). An extra tri-bit '000' is added giving a total of 33 tri-bits. The 33 tri-bits are then passed to a Trellis Encoder to give 66 4-level symbols.

Receive Mode, the MX919/929 takes the 66 received signals and decodes them into tri-bits.

Cyclic Redundancy Codes

CRC0 (MX929 only)

This is a six-bit CRC check code used in the Station ID Block. It is calculated by the modem from the first 24 bits of the block (Bytes 0, 1 & 2) as follows:

The 24 bits are considered as the coefficients of a polynomial M(x) of degree 23, such that the bit (7) of byte 0 is the coefficient of x^{23}, and bit 0 of byte 2 is the coefficient of X^0.

The polynomial F(x) of degree 5 is calculated as being the remainder of the division

$x^6M(x)/(x^6 + x^4 + x^3 + 1)$

where division is performed modulo-2 .

The polynomial $x^5 + x^4 + x^3 + x^2 + x^1 + x^0$ is added (modulo-2) to F(x)

The coefficients of F(x) are placed in the 6-bit CRC0 field, such that the coefficient of x^5 corresponds to the MSB of CRC0.

CRC1 (MX919/929)

This is a sixteen-bit CRC check code used in the Header Block. It is calculated by the modem from the first 80 bits of the block (Bytes 0 to 9 inclusive) as follows:

The 80 bits are considered as the coefficients of a polynomial M(x) of degree 79, such that the bit (7) of byte 0 is the coefficient of x^{79}, and bit 0 of byte 9 is the coefficient of X^0.

The polynomial F(x) of degree 15 is calculated as being the remainder of the division

$x^{16}M(x)/(x^{16} + x^{12} + x^5 + 1)$

where division is performed modulo-2 .

The polynomial $x^{15}\, x^{14} \ldots + x^4 + x^3 + x^2 + x^1 + x^0$ (all coefficients = 1) is added (modulo-2) to F(x)

The coefficients of F(x) are placed in the 16-bit CRC1 field, such that the coefficient of x^{15} corresponds to the MSB of byte 10 of the header block.

CRC2 (MX919/929)

This is a thirty-two-bit CRC check code transmitted at the end of the 'Last' Block. It is calculated by the modem from all of the data and pad bytes in the Intermediate Blocks and in the first 8 bytes of the Last Block as follows:

Let k be the total number of bits in all of the bytes over which the CRC is to be calculated.

These k bits are considered as the coefficients of a polynomial M(x) of degree (k-1), such that the bit (7) of byte 0 is the coefficient of x^{k-1}, and bit 0 of the last byte is the coefficient of x^0.

The polynomial F(x) of degree 31 is calculated as being the remainder of the division

$x^{32}M(x)/(x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + 1)$

where division is performed modulo-2 .

The polynomial $x^{31}\, x^{30} \cdots + x^4 + x^3 + x^2 + x^1 + x^0$ (all coefficients = 1) is added (modulo-2) to F(x)

The coefficients of F(x) are placed in the 32-bit CRC2 field, such that the coefficient of x^{31} corresponds to the msb of byte 8 of the 'last' block.

Operational Information .....

Interleaving

The 66 symbols of a 'Header', 'Intermediate' or 'Last' block are interleaved by the modem before transmission to give protection against noise bursts and short fades.
Interleaving is not performed on the Frame or Symbol Synchronization sequences.

0	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*	*13*	*14*	*15*	*16*	*17*	*18*
19	*20*	*21*	*22*	*23*	*24*	*25*	*26*	*27*	*28*	*29*	*30*	*31*	*32*	*33*	*34*	*35*	*36*
37	*38*	*39*	*40*	*41*	*42*	*43*	*44*	*45*	*46*	*47*	*48*	*49*	*50*	*51*	*52*	*53*	*54*
55	*56*	*57*	*58*	*59*	*60*	*61*	*62*	*63*	*64*								

Considering the 66 4-level symbols to be numbered sequentially (as above) before interleaving, then after interleaving the symbols will be transmitted in the sequence shown below:

First

0	*1*	*8*	*9*	*16*	*17*	*24*	*25*	*32*	*33*	*40*	*41*	*48*	*49*	*56*	*57*	*64*	*65*
2	*3*	*10*	*11*	*18*	*19*	*26*	*27*	*34*	*35*	*42*	*43*	*50*	*51*	*58*	*59*	*4*	*5*
12	*13*	*20*	*21*	*28*	*29*	*36*	*37*	*44*	*45*	*52*	*53*	*60*	*61*	*6*	*7*	*14*	*15*
22	*23*	*30*	*31*	*38*	*39*	*46*	*47*	*54*	*55*	*-----Last*							

The inverse operation (De-Interleaving) is performed in the receive mode.

Operational Information .....

Received Signal Acquisition

Level Measurement and Clock Extraction

To achieve reasonable error rates the MX919/929 needs to make accurate measurements of the received signal amplitude, DC offset and symbol timing, and of course accurate measurements -especially in the presence of noise- are best made by averaging over a relatively long time period.

In most cases the modem will be used to receive isolated messages from a distant transmitter that is only turned on for a very short time before the message starts; also, the received baseband signal from the radio's frequency discriminator will have a dc offset due to small differences between the receiver and transmitter reference oscillators and hence their 'carrier' frequencies.

To provide for this situation, AQSC and AQLEV (Acquire Symbol Clock and Level) commands are provided which, when triggered, cause the modem to follow an automatic sequence designed to perform the measurements as quickly as possible. See the section on the Command Register.

Acquire Receive Signal Levels AQLEV Command Register

The Acquire Receive Signal Levels (AQLEV) sequence starts with a measurement of the average signal voltage over a period of 1 symbol-time to provide a reference for the next stage, which is to measure the positive-going and negative-going peaks of the signal.

The attack and decay times used in this 'peak detect' mode are such that a sufficiently accurate measurement can be made within 16 symbols of a '+3 +3 -3 -3 . . .' pattern (i.e the Symbol-Sync sequence) to allow the Symbol-Clock Extraction circuits to operate.

Once the symbol-clock extraction circuits have detected the presence of a sufficiently coherent signal then, provided that the LEVRES bits of the Control Register have been set to the 'Peak Averaging' setting or 'Hold', this measurement will cease after 16 symbol-times, and the final values kept; otherwise the circuits will continue in the 'Peak Averaging' mode.

Acquire Symbol Clock (AQSC) Command Register

The Acquire Symbol Clock (AQSC) sequence follows a similar pattern; starting with a very fast initial estimate of the received symbol timing, then reducing the bandwidth of the Phase Locked Loop as a coherent signal is detected until the limit reached by the (Control Register) PLLBW bits is reached.

A µController is able to detect the received carrier and therefore knows when to issue the AQSC and AQLEV commands. Note that due to a delay through the RRC filter, the AQSC and AQLEV sequences should not be started until about 8-symbol times after the RX carrier has been detected at the discriminator output.

In a system where the controlling µController is not able to detect the RX carrier, the AQSC and AQLEV sequences may be started at any time; possibly when no carrier is being received. However in this case the clock and level acquisition operation will take longer as the circuits will have to recover from the change from a large amplitude noise signal at the output of the frequency discriminator to the wanted signal, probably with a dc offset. In this type of system the time between the turn-on of the transmitter and the start of the Frame Sync pattern should be extended -preferably by extending the Symbol Sync sequence to 32 or even 48 symbols.

Note that the clock extraction circuits work by detecting the timing of changes between opposite polarity symbols, i.e. a change from '+3' to '-3' or '-1' to '+1'. They will eventually fail if only 1 symbol is transmitted continuously. Similarly, the level measuring circuits require '+3' and '-3' symbols to be received at reasonably frequent intervals.

LEVRES Peak Detect and Peak Averaging

Further information on this subject is currently unavailable in this "Advance Information" Document

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0V
Input Voltage at any pin (ref V_{SS}=0V)	-0.3 to (V_{DD}+ 0.3V)
Sink/Source Current	
(supply pins)	±30mA
(other pins)	±20mA
Total Device Dissipation (@ T_{AMB}=25°C)	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Symbol Rate = 4800 symbols/sec

Xtal/Clock = 4.9152 MHz

1

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD})		4.5	-	5.5	V
Supply Current (powersaved)	1	-	1.0	1.5	mA
Supply Current (not powersaved)	1	-	11.0	16.0	mA
Symbol Rate		2400	-	9600	symbols/sec
TX Output					
Impedance (not powersaved)	2	-	1.0	2.5	kΩ
Impedance (powersaved)	2	-	500	-	kΩ
Signal Level	3	0.8	1.0	1.2	Vp-p
RX Input					
Impedance (RX In pin)		-	10.0	-	MΩ
RX Input Amp Voltage Gain		-	500	-	V/V
Input Signal Level	4	0.7	1.0	1.3	Vp-p
Input dc Offset (wrt V_{DD}/2)	4	-0.5	-	0.5	V
Xtal/Clock Input					
'High' pulse width	5	40.0	-	-	ns
'Low' pulse width	5	40.0	-	-	ns
Input Impedance		10.0	-	-	MΩ
Inverter Gain (I/P = 1mV rms @ 1kHz)		20.0	-	-	dB
Xtal/Clock Frequency		2.0	-	10.0	MHz
µController Interface					
Input logic '1' level	6, 7	V_{DD} -1.5	-	-	V
Input Logic '0' level	6, 7	-	-	1.5	V
Input Leakage Current (V_{IN} = 0V to V_{DD})	6, 7	-5.0		+5.0	µA
Input Capacitance	6, 7	-	10.0	-	pF
Output Logic '1' Level (IOH = 120µA	7	V_{DD} -0.4			V
Output Logic '0' Level (IOL = 360µA)	7, 8	-	-	0.4	V
'Off' State Leakage Current (V = V_{DD})	8	-	-	10	µA

Specifications .....

Modem Read/Write Load Timing

Conditions: V_{DD} = 4.5 to 5.5V; T_{OP} = -40°C to +85°C; with a maximum load of 30pF to V_{SS} on pins D_0 toD_7.

Description		Note	Min.	Typ.	Max.	Unit
t_{ACSL}	"Address Valid" to "CS Low" time		0	-	-	ns
t_{AH}	"Address Hold" time		0	-	-	ns
t_{CSH}	"CS Hold" time		0	-	-	ns
t_{CSHI}	"CS High" time		6.0	-	-	Xtal/Clock Cycles
t_{CSRWL}	"CS" to "WR" or "RD" Low time		0	-	-	ns
t_{DHR}	"Read-Data Hold" time		0	-	-	ns
t_{DHW}	Write-Data Hold time		0	-	-	ns
t_{DSW}	Write-Data Set-Up" time		90.0	-	-	ns
t_{RHCSL}	"RD High" to "CS Low" time (write cycle)		0	-	-	ns
t_{RACL}	"Read Access" time from "CS Low"		-	-	175	ns
t_{RARL}	"Read Access" time from "RD Low"		-	-	145	ns
t_{RL}	"RD" Low time		200	-	-	ns
t_{RX}	"RD High" to "D_0-D_7 3-State" time		-	-	50.0	ns
t_{WHCSL}	"WR High" to "CS Low" time (read cycle)		0	-	-	ns
t_{WL}	"WR" Low time		200	-	-	ns

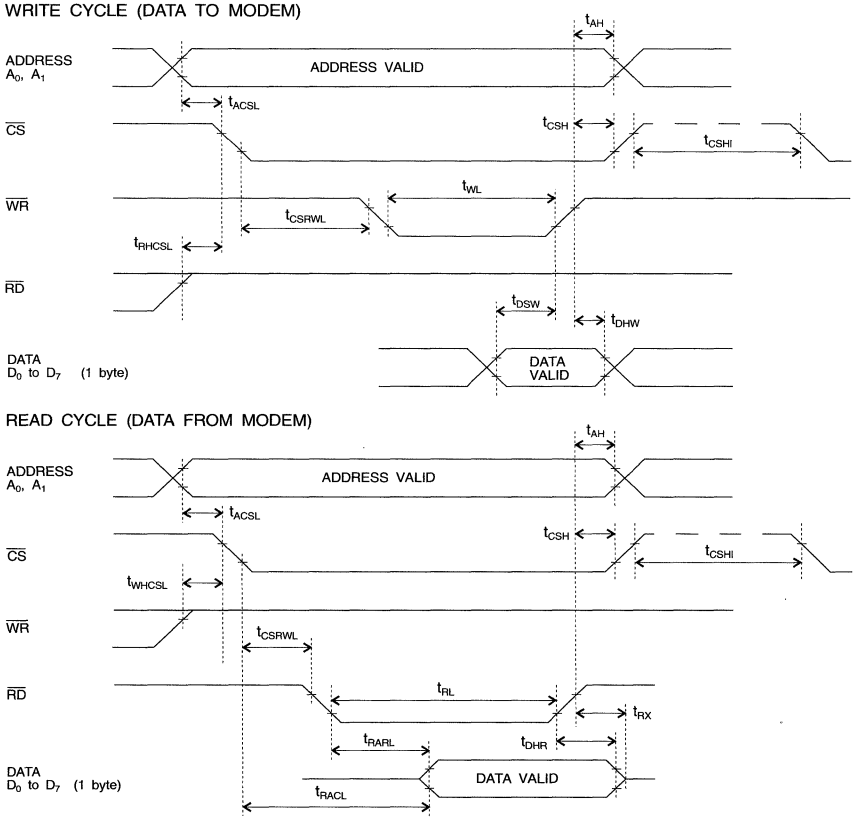


Figure 26 - MX919/929 - µProcessor Read/Write Timing

Specification Notes:

1. V_{DD} = 5.0V, T_{OP} = 25°C; not including any current drawn from the modem pins by external circuitry.
2. Small signal impedance (dynamic measurement) at 1kHz.
3. Measured after the external CR filter, for a '+3 +3 -3 -3 +3 +3 -3 -3 ... symbol sequence; at V_{DD} = 5.0V (output level is proportional to V_{DD}).
4. For optimum performance, measured at the RX Feedback pin, for a '+3 +3 -3 -3 +3 +3 -3 -3 ... symbol sequence.
5. Timing for an external input to the Xtal/Clock pin.
6. $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A_0 and A_1 pins.
7. D_0 - D_7 pins.
8. $\overline{IRQ}$ pin.

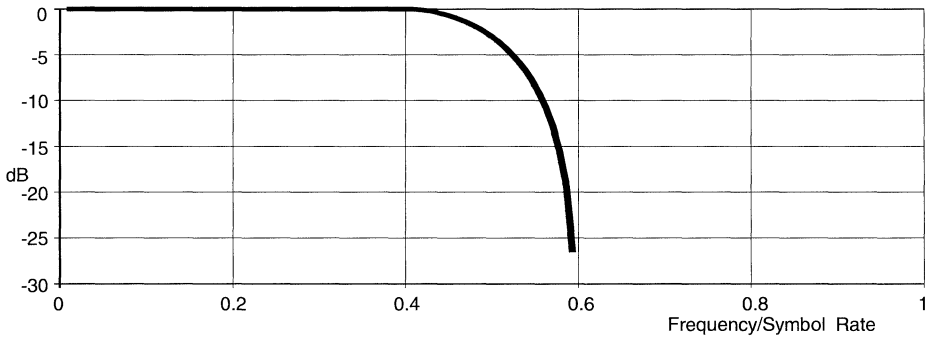


Figure 27 - RRC Filter Response

Signal-to-Noise Performance

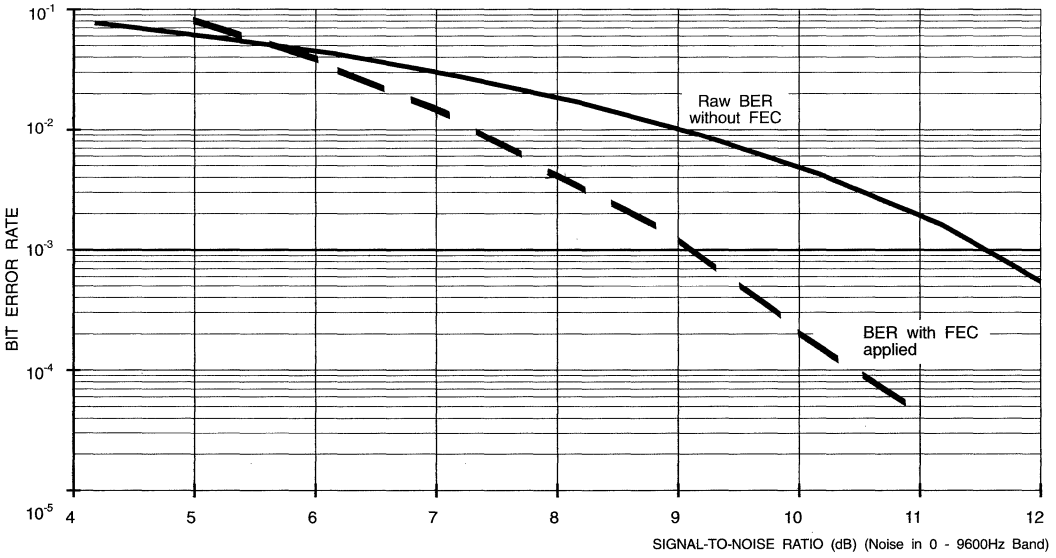


Figure 28 - Typical Error Rates at 4800 Symbols/sec

Advance Information

LOW VOLTAGE DUAL MODE CDPD/AMPS-WBD FULL-DUPLEX DATA MODEM

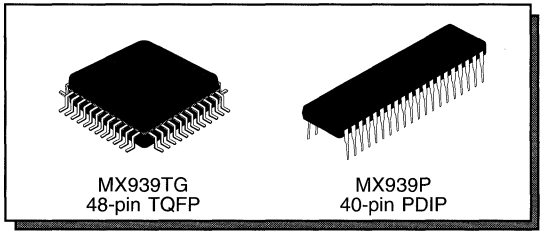
1

FEATURES

- **MX•COM MiXed SIGNAL CMOS**
- **FULL-DUPLEX GMSK MODEM**
- **SAT TONE DETECTION & REGENERATION**
- **WIDE BAND DATA (WBD) MODEM**
- **LOW VOLTAGE OPERATION**
  3 TO 5.5 V
- **POWERSAVING MANAGEMENT MODES**
- **DIGITALLY CONTROLLED I/O SIGNAL LEVELS**
- **180° TWO-POINT TX OUTPUT**
- **SERIAL PORT COMPATIBLE WITH DSP INTERFACE**
- **PARALLEL µP CONTROL INTERFACE**
- **COMPLIES WITH CDPD 1.0 STANDARD**

APPLICATIONS

- **CDPD FULL-DUPLEX DATA MODEM**
- **AMPS WIDE BAND FULL-DUPLEX DATA MODEM WITH SAT CONTROL**
- **TQFP PACKAGE FITS PCMCIA**



MX939TG
48-pin TQFP

MX939P
40-pin PDIP

Description

The MX939 is a synchronous Modem IC designed for wireless data applications. Employing Gaussian Minimum Shift Keying (GMSK) baseband modulation, the MX939 provides a BT of 0.5 and data rates at 19.2 kbps for Cellular Digital Packet Data (CDPD) and 10 kbps for Wide Band Data (WBD).

The MX939 is programmable via an 8-bit parallel bus to support packet switched CDPD full-duplex GMSK operation. Optionally, the MX939 may be programmed for AMPS circuit switched WBD operation including SAT tone detection and regeneration. In this mode an interrupt occurs whenever the SAT tone is detected.

In its AMPS WBD capacity, the MX939 accepts NRZ data and converts it to Manchester encoded data for transmission. It also receives Manchester encoded data and outputs sliced data directly at 10kbps.

Input and output signal levels can be adjusted using the digitally controlled gain blocks. 180° out of phase outputs are possible using the additional inverting digitally controlled gain block, allowing two-point modulation.

The TX and RX data interfaces are bit serial, synchronized to TX and RX data clocks generated by the modem.

A programmable Powersave mode ensures minimum power consumption. The MX939 is available in DIP and TQFP (Thin Quad Flat Pack) packages.

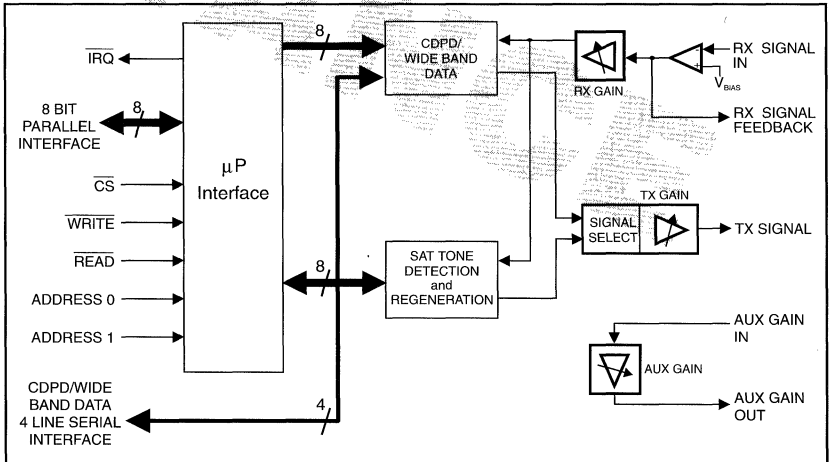


Figure 1 - Block Diagram

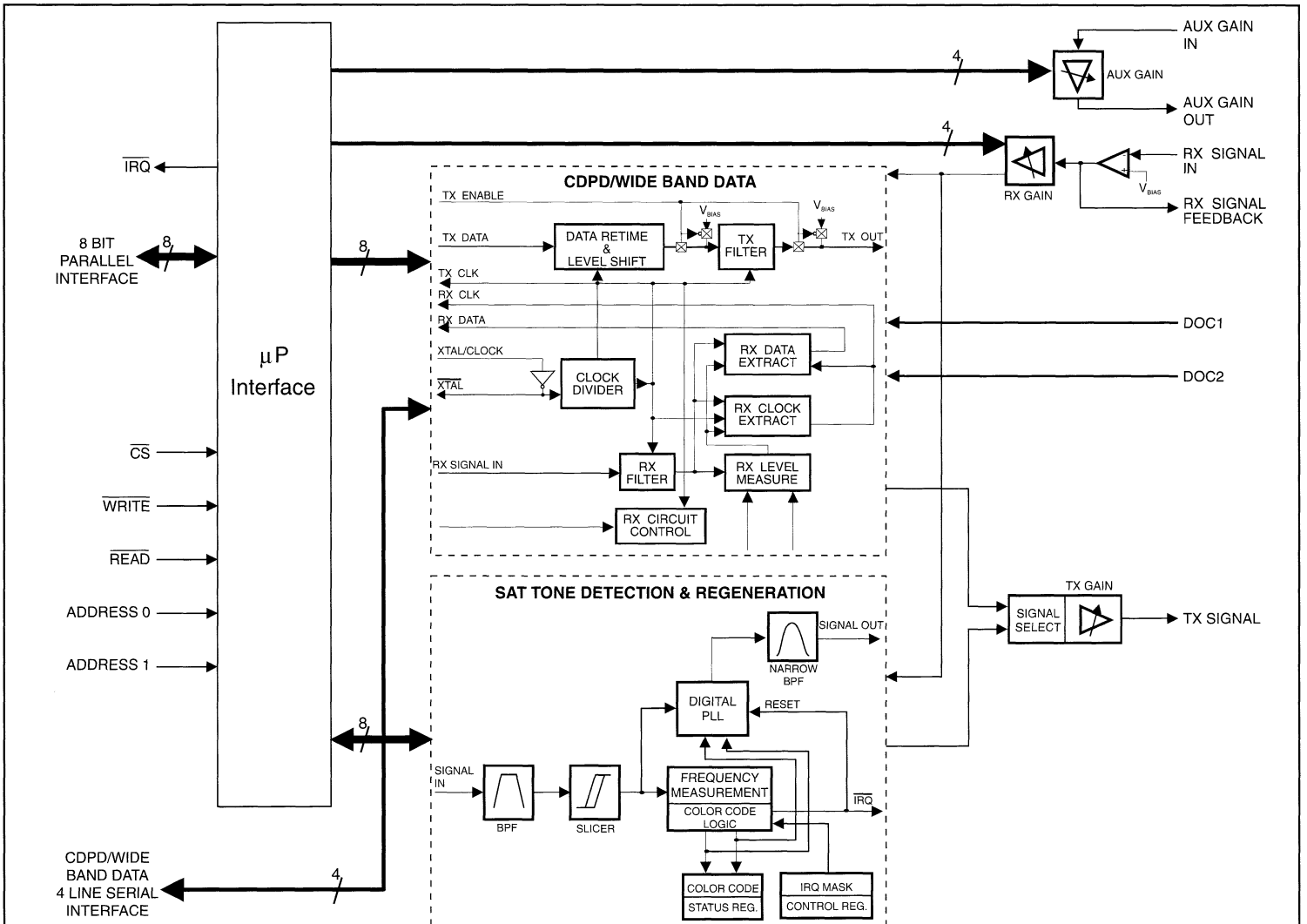


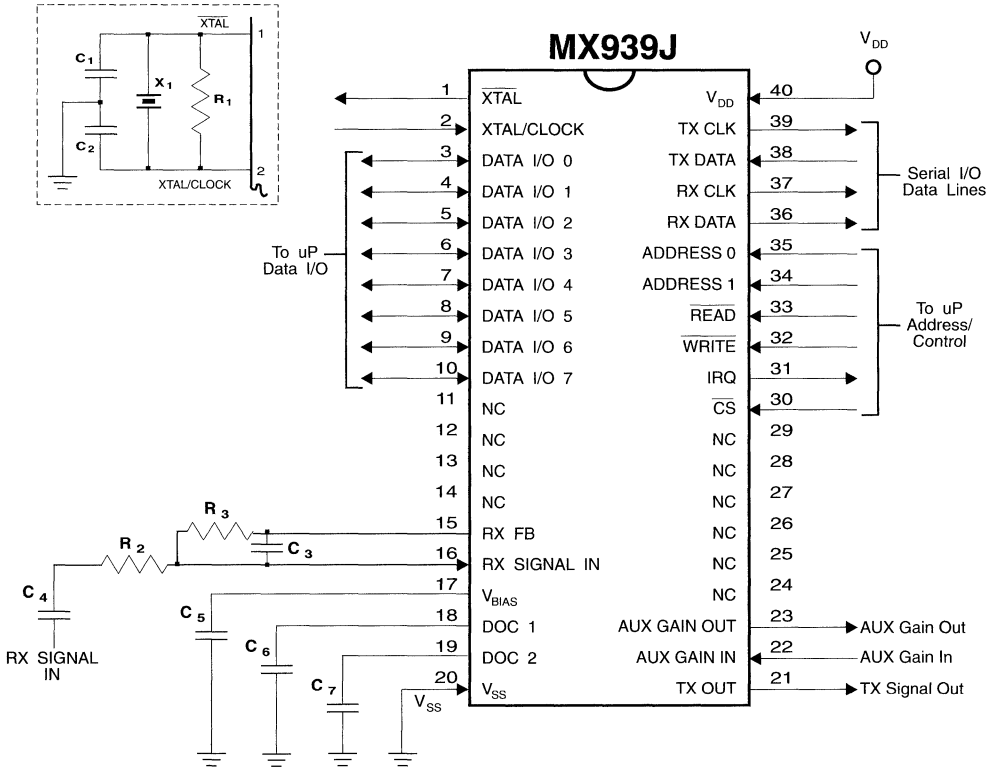
Figure 2 - Detailed Block Diagram

Pin	Function
1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator.
2	**Xtal/Clock:** The input to the on-chip Xtal oscillator. A Xtal, or externally derived clock (f_{XTAL}) pulse input should be connected here. If an externally generated clock is to be used, it should be connected to this pin and the "$\overline{\text{Xtal}}$" pin left unconnected. Note that operation of the MX939 without a suitable Xtal or clock input may cause device damage.
3-10	**DATA I/O 0-7:** 8 bi-directional 3-state µP interface data lines.
15	**RX FB:** The output of the RX Input Amplifier and the input to the RX Filter.
16	**RX Signal In:** The input to RX input amplifier.
17	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$. This pin must be decoupled to V_{SS} by a capacitor mounted close to the pin.
18 19	**Doc1:** **Doc2:** Connections to the RX Level Measurement Circuitry. A capacitor should be connected from each pin to V_{SS}.
20	**V_{SS}:** Negative supply rail. Signal ground.
21	**TX Out:** The TX signal output from the MX939 GMSK Modem.
22 23	**AUX Gain In:** **AUX Gain Out:** These pins form the input and output of the auxiliary inverting digitally controlled variable gain amplifier.
30	**$\overline{\text{CS}}$ (Chip Select):** This is an active low logic level input to the MX939 used to enable a data read or write operation.
31	**$\overline{\text{IRQ}}$:** This is a "wire-ORable" output for connection to the controlling µP's Interrupt Request input. It has a low impedance pull-down to V_{ss} when active, and has a high impedance when inactive.
32	**$\overline{\text{WRITE}}$:** This active low logic level input is used to control the writing of data to the MX939 from the controlling µP.
33	**$\overline{\text{READ}}$:** This active low logic level input is used to control the reading of data from the MX939 into the controlling µP.
34 35	**ADDRESS 1:** These are logic level register select inputs. **ADDRESS 0:**
36	**RX Data:** A logic level output carrying the received data, synchronous with RX CLK.
37	**RX CLK:** A logic level clock output at the received data bit-rate.
38	**TX Data:** The logic level input for the data to be transmitted. This data should be synchronous with TX CLK.
39	**TX CLK:** A logic level clock output at the transmit-data rate. TX & RX Data, and TX & RX Clk form the serial I/O interface for the CDPD or wide band data modems with the bit rate frequencies listed below:

Modem Type	RX Data	RX Clk	TX Data	TX Clk
CDPD	9.6kHz max.	19.2kHz	9.6kHz max.	19.2kHz
AMPS WBD	10kHz max.	20kHz	5kHz max.	10kHz

40	**V_{DD}:** Positive supply rail. A single +5 volt power supply is required. Levels and voltages within this modem are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the pin.

Note: Pin-out for the 48-pin TQFP is T.B.D.



Component	Value	Component	Value
R_1	1.0MΩ	C_3	33pF
R_2	Note 1	C_4	Note 1
R_3	100kΩ	C_5	1.0µF
C_1	T.B.D.	C_6	15pF
C_2	T.B.D.	C_7	15pF
		X_1	1.44MHz

Notes

1. R_2, R_3, C_3 and C_4 form the gain components for the RX Input signal. They should be chosen as required by the signal input level.

Figure 3 - External Components *Actual Pin-out T.B.D.*

Application Information for CDPD/Wide Band Data

RX Signal Path Description

The function of the RX circuitry is to:

1. Set the incoming signal to a usable level.
2. Clean the signal by filtering.
3. Provide d.c. level thresholds for clock and data extraction.
4. Provide clock timing information for data extraction and external circuits.
5. Provide RX data in a binary form.

1

The output of the radio receiver's Frequency Discriminator should be fed to the MX939's RX Filter via a suitable gain and d.c. level adjusting circuit. This gain circuit can be built, with external components, around the on-chip RX Input Amplifier.

Positive going signal excursions at RX Feedback pin will produce a logic "0" at the RX Data Output. Negative going excursions will produce a logic "1."

The received signal is fed through the lowpass RX Filter, which has a -3dB corner frequency of 0.56 times the data bit-rate, before being applied to the Level Measure and Clock and Data extraction blocks.

The Level Measuring block consists of two voltage detectors, one of which measures the amplitude of the 'positive' parts of the received signal. The other measures the amplitude of the 'negative' portions. External capacitors are used by these detectors, via the Doc 1/2 pins, to form voltage 'hold' or 'integrator' circuits. Results of the two measurements are then processed to establish the optimum d.c. level decision-thresholds for the Clock and Data extraction, depending upon the RX signal amplitude and any d.c. offset present.

RX Circuit Control Modes

The operating characteristics of the RX Level Measurement and Clock Extraction circuits are controlled, as shown in Table 1, by logic level inputs applied to the 'PLLacq,' 'RX Hold' and 'RXDCacq.'

As shown in Figure 4, a data transmission generally begins with a preamble such as "1010101010," to allow the receiving modem to establish timing- and level-lock as quickly as possible. During the time that the preamble is expected, the 'RXDCacq' and 'PLLacq' inputs should be switched from a logic "0 to 1" so that the Level Measuring and Clock Extraction modes are operated and sequenced as shown.

The 'RX Hold' input should normally be held at a logic "1" while data is being received, but may be driven to a logic "0" to freeze the Level Measuring and Clock Extraction circuits during a fade. If the fade lasts for less than 200 bit periods, normal operation can be resumed by returning the 'RX Hold' input to a logic "1" at the end of the fade. For longer fades, it may be better to reset the Level Measuring circuits by placing the 'RXDCacq' to a logic "1" for 10 to 20 bit periods.

'RX Hold' has no effect on the Level Measuring circuits while 'RXDCacq' is at a logic "1," and has no effect on the PLL while 'PLLacq' is at a logic "1."

A logic "0" on 'RX Hold' does not disable the 'RX Clock' output, and the RX Data Extraction and S/N Detection circuits will continue to operate.

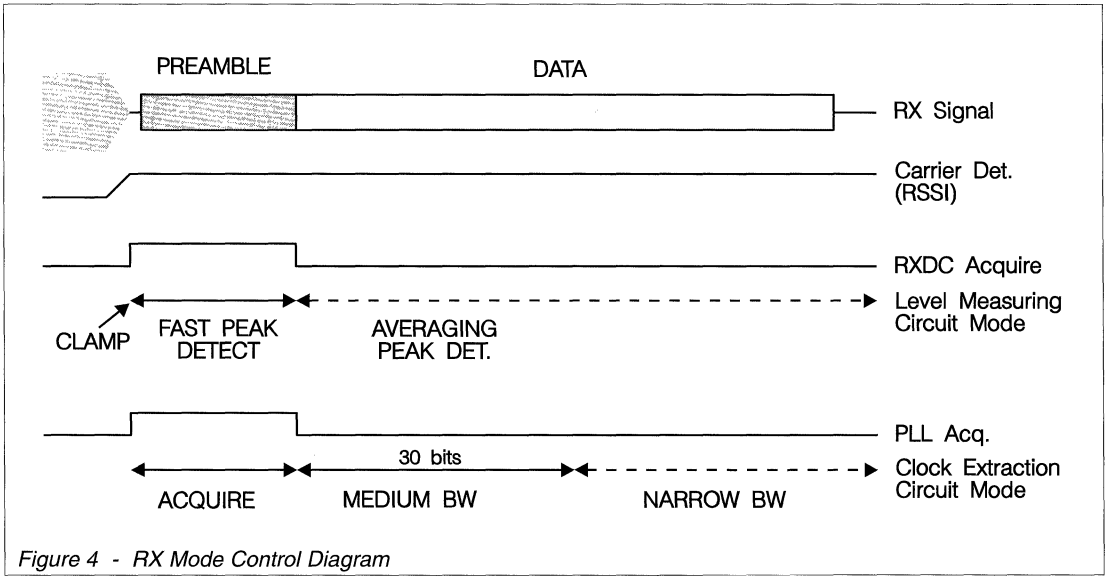


Figure 4 - RX Mode Control Diagram

Application Information .....

PLLacq	RX Hold	PLL Action
"1"	X	**Acquire:** Sets the PLL bandwidth wide enough to allow a lock to the received signal in less than 8 zero crossings. The Acquire mode will operate as long as PLLacq is a logic "1".
"1" to "0"	"1"	**Medium Bandwidth:** The correction applied to the extracted clock is limited to a maximum of ±T.B.D. bit-periods for every two received zero-crossings. The PLL operates in this mode for a period of about 30 bits immediately following a "1" to "0" transition of the PLLacq input, provided that the RX Hold input is a logic "1".
"0"	"1"	**Narrow Bandwidth:** The correction applied to the extracted clock is limited to a maximum of ±T.B.D. bit-periods for every two received zero-crossings. The PLL operates in this mode whenever the RX Hold Input is a logic "1" and PLLacq has been a logic "0" for at least 30 bit periods (after Medium Bandwidth operation, for instance).
"0"	"0"	**Hold:** The PLL feedback loop is broken, allowing the RX Clock to freewheel during signal fade periods.
RXDCacq	**RX Hold**	**RX Level Measure Action**
"0" to "1"	X	**ClGain:** Operates for one bit-time after a "0" to "1" transition of the RXDCacq input. The external capacitors are rapidly charged toward a voltage halfway between the received signal input level and V_{BIAS}, with the charge time-constant being approximately 0.5bit-time.
"1"	X	**Fast Peak Detect:** The voltage detectors act as peak-detectors. One capacitor is used to capture the 'positive'-going signal peaks of the RX Filter output signal; the other captures the 'negative'-going peaks. The detectors operate in this mode whenever the RXDCacq input is at a logic "1," except for the initial 1-bit ClGain-mode time.
"0"	"1"	**Averaging Peak Detect:** Provides a slower but more accurate measurement of the signal peak amplitudes.
"0"	"0"	**Hold:** The capacitor charging circuits are disabled so that the outputs of the voltage detectors remain substantially at the last readings (discharging very slowly [time-constant approx. 2,000 bits] towards V_{BIAS}).

Table 1 - PLL and RX Level Measurement Operational Modes

RX Clock Extraction

Synchronized by a phased locked loop (PLL) circuit to zero-crossings of the incoming data, the 'RX Clock Extraction' circuitry controls the 'RX CLK' output. The RX Clock is also used internally by the Data Extraction circuitry. The PLL parameters can be varied by the 'RX Circuit Control' inputs PLLacq and RX Hold to operate in one of four PLL modes as described in Table 1.

RX Data Extraction

The 'RX Data Extraction' circuit decides whether each received bit is a "1" or "0" by sampling the output of the RX Filter in the middle of each bit-period, and comparing the sampled voltage against a threshold derived from the 'Level Measuring' circuit. This threshold is varied on a bit-by-bit basis to compensate for intersymbol interference. The extracted data is output from the 'RX Data' pin, and should be sampled externally on the rising edge of the 'RX CLK.'

TX Signal Path Description

The binary data applied to the 'TX Data' input is retimed within the chip on each rising edge of the 'TX Clock' and then converted to a binary signal centered about V_{BIAS}.

The TX Filter has a lowpass frequency response, which is designed to minimize amplitude and phase distortion of the binary signal while providing sufficient attenuation of the high frequency-components which would otherwise cause interference into adjacent radio channels.

The signal at 'TX Out' is centered around V_{BIAS}, going positive for logic "1" (high) level inputs to the 'TX Data' input and negative for logic "0" (low) inputs.

Application Information .....

FM Modulator, Demodulator and IF

For optimum performance, the 'eye' pattern of the received signal (when receiving random data) applied to the MX939 should be as close as possible to the Transmit 'eye' pattern example shown in Figure 5. Of particular importance are general symmetry and cleanliness of the zero-crossings.

To achieve this, attention must be paid to:

- Linearity and frequency/phase response of the TX frequency modulator. Unless the transmit data is encoded to remove low frequency components, the modulator frequency response should extend down to a few Hz. This is because two-point modulation is necessary for synthesized radios.
- Bandwidth and phase response of the RX IF filters.
- Accuracy of the TX and RX carrier frequencies -any difference will shift the received signal towards one of the skirts of the IF filter response.

Ideally, the RX demodulator should be d.c. coupled to the MX939 'RX Signal In' pin (with a d.c. bias added to center the signal at the RX Feedback pin around $V_{DD}/2$ [V_{BIAS}]), however a.c. coupling can be used provided that:

- The 3 dB cut-off frequency is 20Hz or below (i.e. a 0.1µF capacitor in series with 100kΩ).
- The data does not contain long sequences of consecutive ones or zeroes.
- Sufficient time is allowed after a step change at the discriminator output (resulting from channel changing or the appearance of an RF carrier) for the voltage into the MX939 to settle before the 'RXDCacq' line is strobed.

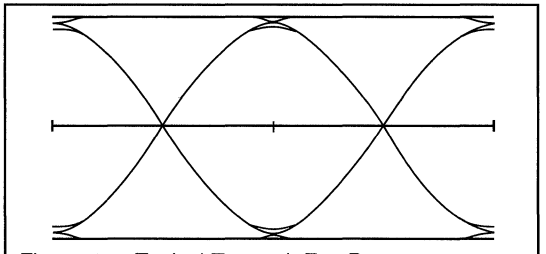


Figure 5 - Typical Transmit Eye Pattern

Data Formats

The receive section of the MX939 works best with data which has a reasonably 'random' structure --the data should contain approximately the same number of 'ones' as 'zeroes' with no long sequences of consecutive 'ones' or 'zeroes'. Also, long sequences (>100 bits) of '10101010 ...' patterns should be avoided.

For this reason, it is recommended that data is randomized in some manner before transmission, for example by 'exclusive-ORing' it with the output of a binary pseudo-random pattern generator.

Where data is transmitted in bursts, each burst should be preceded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble should be at least 16 bits long, and should preferably consist of alternating pairs of '1's and '0's i.e. '110011001100 .....'; the pattern '10101010 ....' should not be used.

'Acquisition' and 'Hold' Modes

The 'RXDCacq' and 'PLLacq' inputs must be pulsed 'High' for about 16 bits at the start of reception to ensure that the d.c. measurement and timing extraction circuits lock-on to the received signal correctly. Once lock has been achieved, then the above inputs should be taken 'Low' again.

In most applications, there will be a d.c. step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the distant transmitter is turned on.

The MX939 can tolerate d.c. offsets in the received signal of at much as ±0.5V with respect to V_{BIAS}, (measured at the RX Feedback pin). However, to ensure that the d.c. offset compensation circuit operates correctly and with minimum delay, the 'Low' to 'High' transition of the 'RXDCacq' and 'PLLacq' inputs should occur after the mean input voltage to the MX939 has settled to within about 0.1V of its final value. (Note that this can place restrictions on the value of any series signal coupling capacitor.)

As well as using the 'RX Hold' input to freeze the Level Measuring and Clock Extraction circuits during a signal 'fade,' RX Hold may also be used in systems which employ a continuously transmitting control channel to freeze the receive circuitry during transmission of a data packet, allowing reception to resume afterwards without losing bit synchronization. To achieve this, the MX939 'Xtal' clock needs to be accurate enough that the derived 'RXClock' output does not drift by more that about 0.1 bit time from the actual received data-rate during the time that the 'RXHold' input is 'Low'.

The 'RXDCacq' input, however, may need to be pulsed 'High' to re-establish the level measurements if the 'RXHold' input is 'Low' for more that a few hundred bit-times.

The voltages on the Doc1 and Doc2 pins reflect the average peak positive and negative excursions of the (filtered) receive signal, and could therefore be used to derive a measure of the data signal amplitude. Note however, that these pins are driven from very high-impedance circuits, so that the d.c. load presented by any external circuitry should exceed 10MΩ to V_{BIAS}.

Read and Write Registers - Memory Map

Read Only	HEX	READ	WRITE	CS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1 BIT 0
Status Register	$0	0	1	0	0	0	0	0	0	0	COLOR CODE
Write Only											
GAIN 1 Register	$0	1	0	0	—	—	— AUX GAIN —		—	—	— — — — TX GAIN — — — —
GAIN 2 Register	$1	1	0	0	x	x	x	x	— — — — RX GAIN — — — —		
Control Register	$2	1	0	0	x	x	IRQ Mask	Hold	PLLacq	DCacq	MODE

x = don't care

Read Only Register

STATUS Register (HEX address $0)

This read only register contains the status of the color code as described below:

COLOR CODE (Bits 0 and 1)

Bits 0 and 1 indicate the SAT tone frequency or "COLOR CODE" of the incoming signal according to the table below. Whenever the COLOR CODE changes an interrupt may occur, depending on the state of the IRQ mask (Bit 5) in the control register.

Measured Frequency of Incoming Signal	Measured SAT Determination	Where	COLOR CODE Bit 1	COLOR CODE Bit 0
$f \leq f_1$	No valid SAT	f_1 = 5955 ± 5Hz	1	1
$f_1 \leq f < f_2$	SAT = 5970	f_2 = 5985 ± 5Hz	0	0
$f_2 \leq f < f_3$	SAT = 6000	f_3 = 6015 ± 5Hz	0	1
$f_3 \leq f < f_4$	SAT = 6030	f_4 = 6045 ± 5Hz	1	0
$f_4 \leq f$	No valid SAT		1	1
No SAT Received	No valid SAT		1	1

Table 2 - Color Code Frequencies

Write Only Register

GAIN 1 Register (HEX address $0)

This write only register controls the MX939's gain functions as described below:

AUX GAIN (Bits 7, 6, 5 and 4)

This 4-bit number specifies the gain of the auxiliary amplifier. The desired gain is selected according to Table 3. In the OFF state the amplifier is in a powersave mode, and the output is taken to bias via a 500kΩ resistor.

TX GAIN (Bits 3, 2, 1 and 0)

This 4-bit number specifies the TX gain. The desired gain is selected according to Table 4. In the OFF state the amplifier is in a powersave mode, and the output is taken to bias via a 500kΩ resistor.

Bit 7	Bit 6	Bit 5	Bit 4	Gain dB
0	0	0	0	OFF
0	0	0	1	-3.0
0	0	1	0	-2.571
0	0	1	1	-2.143
0	1	0	0	-1.714
0	1	0	1	-1.286
0	1	1	0	-0.857
0	1	1	1	-0.428
1	0	0	0	0
1	0	0	1	0.428
1	0	1	0	0.857
1	0	1	1	1.286
1	1	0	0	1.714
1	1	0	1	2.143
1	1	1	0	2.573
1	1	1	1	3.0

Table 3 - AUX Gain Register

Bit 3	Bit 2	Bit 1	Bit 0	Gain dB
0	0	0	0	OFF
0	0	0	1	-3.0
0	0	1	0	-2.571
0	0	1	1	-2.143
0	1	0	0	-1.714
0	1	0	1	-1.286
0	1	1	0	-0.857
0	1	1	1	-0.428
1	0	0	0	0
1	0	0	1	0.428
1	0	1	0	0.857
1	0	1	1	1.286
1	1	0	0	1.714
1	1	0	1	2.143
1	1	1	0	2.573
1	1	1	1	3.0

Table 4 - TX Gain Register

GAIN 2 Register (HEX address $1)

This write only register controls the MX939's gain functions as described below:

RX GAIN (Bits 3, 2, 1 and 0)

This 4-bit number specifies the RX gain. The desired gain is selected according to Table 5 below.

Bit 3	Bit 2	Bit 1	Bit 0	Gain dB
0	0	0	0	OFF
0	0	0	1	-3.0
0	0	1	0	-2.571
0	0	1	1	-2.143
0	1	0	0	-1.714
0	1	0	1	-1.286
0	1	1	0	-0.857
0	1	1	1	-0.428
1	0	0	0	0
1	0	0	1	0.428
1	0	1	0	0.857
1	0	1	1	1.286
1	1	0	0	1.714
1	1	0	1	2.143
1	1	1	0	2.573
1	1	1	1	3.0

Table 5 - RX Gain Register

CONTROL Register (HEX address $2)

This register controls the MX939's functions as described below:

MODE (Bits 1 and 0)

This 2-bit number configures the MX939 to function as a CDPD, SAT Tone or Wide Band Data Modem described in Table 6 below.

Bit 1	Bit 0	CDPD	SAT Tone	Wide Band Data
0	0	Powersaved	Powersaved	Powersaved
0	1	Enabled	Powersaved	Powersaved
1	0	Powersaved	Enabled	Powersaved
1	1	Powersaved	Powersaved	Enabled

Table 6 - Mode Control Register

RXDCAcq (Bit 2)

A logic "1" applied to this bit will set the RX Level Measurement circuitry to the acquire mode. This applies to both the CDPD and the Wide Band Data Modem functions.

PLLAcq (Bit 3)

A logic "1" applied to this bit will set the RX Clock Extraction circuitry to the acquire mode. This applies to both the CDPD and the Wide Band Data Modem functions.

Hold (Bit 4)

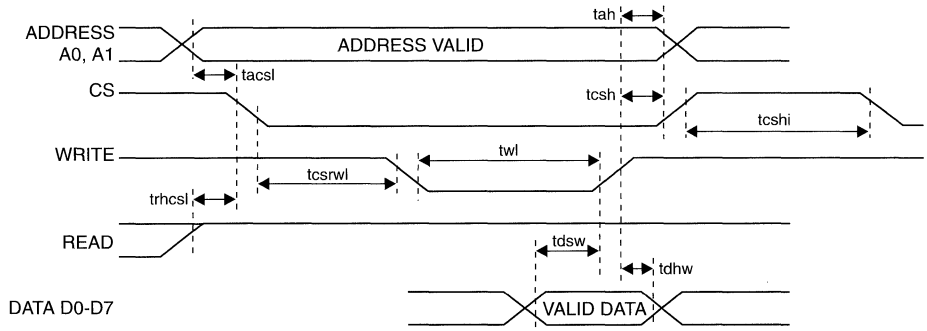
A logic "0" applied to this bit will "freeze" the Clock Extraction and Level Measurement circuits unless they are in the acquire mode. This applies to both the CDPD and the Wide Band Data Modem functions.

IRQ Mask (Bit 5)

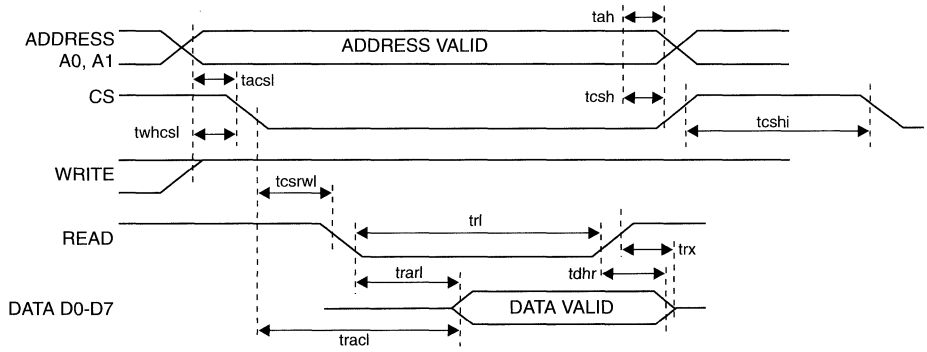
When this bit is set to "1" the COLOR CODE interrupt will be gated out to the IRQ pin. When this bit is set to "0" the COLOR CODE interrupt will be inhibited.

Timing Information

WRITE CYCLE (DATA TO MX939)



READ CYCLE (DATA FROM MX939)



Period		Note	Min.	Typ.	Max.	Units
tacsl:	Address valid to CS low time		0	-	-	ns
tah:	Address hold time		0	-	-	ns
tcsh:	CS hold time		0	-	-	ns
tcshi:	CS high time		6	-	-	xtal cycles
tcsrwl:	CS to WRITE or READ low time		0	-	-	ns
tdhr:	Read data hold time		0	-	-	ms
tdhw:	Write data hold time		0	-	-	ns
tdsw:	Write data setup time		90	-	-	ns
trhcsl:	READ high to CS low time (write)		0	-	-	ns
tracl:	Read access time from CS low	1	-	-	175	ns
trarl:	Read access time from READ low	1	-	-	145	ns
trl:	READ low time		200	-	-	ns
trx:	READ high to D0-D7 3-state time		-	-	50	ns
twhcsl:	WRITE high to CS low time (read)		0	-	-	ns
twl:	WRITE low time		200	-	-	ns

Note 1: With 30pF max. to V_{SS} on D0-D7 pins.

Figure 6 - Parallel µP Interface Timing

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0V
Input Voltage at any pin (ref V_{SS}=0V)	-0.3 to (V_{DD}+ 0.3V)
Sink/Source Current	
(supply pins)	±30mA
(other pins)	±20mA
Total Device Dissipation (@ T_{AMB}=25°C)	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Characteristics

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/Clock f_0 = 1.44 MHz

Noise bandwidth = bit rate

Characteristics	See Note	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD})		3.0	-	5.5	V
Static Values					
Supply Current					
Powersaved	1	-	1.0	TBD	mA
Enabled	1	-	8	TBD	mA
Transmit Parameters					
TX Output Impedance					
Enabled	2	-	1.0	TBD	kΩ
Powersaved	2	TBD	500	TBD	kΩ
TX Signal Level					
CDPD	3,5	TBD	1.0	TBD	V p-p
AMPS WBD	3,5	TBD	1.7	TBD	V p-p
SAT	3,5	TBD	0.4	TBD	V p-p
Receive Parameters					
RX Input Impedance		TBD	-	-	MΩ
RX In Amp Voltage Gain		-	500	-	V/V
RX Input Signal Level					
CDPD	4,5	TBD	1.0	TBD	V p-p
AMPS WBD	4,5	TBD	1.7	TBD	V p-p
SAT	4,5	TBD	0.4	TBD	V p-p
Xtal/Clock Input					
High Pulse Width	6	TBD	-	-	ns
Low Pulse Width	6	TBD	-	-	ns
Input Impedance		TBD	-	-	MΩ
Voltage Gain (i/p = 1mVrms @ 1kHz)		TBD	-	-	dB

Characteristics	See Note	Min.	Typ.	Max.	Unit
µP Interface					
Input Logic "1" Level	17,18	V_{DD}-1.15	-	-	V
Input Logic "0" Level	17,18	-	-	1.5	V
Input Leakage Current	17,18	TBD	-	TBD	µA
Input Capacitance	17,18	-	10.0	-	pF
Logic "1"Output Level at IOH = 120µA	18	V_{DD}-0.4	-	-	V
Logic "0"Output Level at IOL = 360µA	18,19	-	-	0.4	V
"Off" State Leakage Current (V = V_{DD})	19	-	-	TBD	µA
AUX Gain					
Input Impedance		TBD	-	-	kΩ
Output Impedance Enabled		-	1	-	kΩ
Powersave		-	500	-	kΩ
Bandwidth (-3dB)		TBD	-	-	kΩ
Total Harmonic Distortion	7	-	0.35	TBD	%
Output Noise Level	8	-	180	TBD	mVrms
Onset of Clipping	9	TBD	-	-	V p-p
RX Gain, TX Gain, AUX Gain					
Gain	10	TBD	-	TBD	dB
Gain per Step	10	-	0.43	-	dB
Step Error	10	-	-	TBD	dB
SAT Characteristics					
SAT RX Decode Response	16	-	200	TBD	ms
SAT RX Not Decode Level			TBD		
SAT TX Phase Step Response	11	-	-	TBD	ms
SAT TX Phase Jitter		TBD	-	TBD	degrees
SAT TX S/N		-	-	TBD	%
CDPD Characteristics					
CDPD RX Bit Rate		-	19.2	-	kbps
CDPD RX Data Delay	13	-	-	TBD	bit periods
CDPD RX BER			TBD		
CDPD TX Bit Rate		-	19.2	-	kbps
CDPD TX BT		-	0.5	-	
CDPD TX Data Delay	12	-	1.5	TBD	bit periods
AMPS WIDE BAND DATA (WBD) Characteristics					
WBD RX Bit Rate	15	-	20	-	kbps
WBD RX Data Delay	13	-	-	TBD	bit periods
WBD RX BER			TBD		
WBD TX Bit Rate	14	-	10	-	kbps
WBD TX Data Delay	12	-	1.5	TBD	bit periods

Notes

1. Not including current drawn from the MX939 pins by external circuitry.
2. Small signal impedance.
3 Measured with a 5V supply and the TX gain amplifier set to 0dB.
4. Measured with a 5V supply, the RX gain amplifier set to 0dB, and 0dB gain in the input amplifier.
5. Typical levels equate to carrier deviations of ±8kHz for WBD, ±4.8kHz for CDPD, and ±2kHz for SAT. The levels are directly proportional to the supply voltage.
6. Timing for an external clock input to the Xtal/clock pin.
7. Gain set to 0dB, input level of 549mVrms at 1kHz.
8. With an A.C. short-circuit input, measured in a 30kHz bandwidth.
9. With a 5 volt supply.
10. With reference to a 1kHz signal.
11. Time to settle to within 10° of final steady state phase.
12. Measured between the rising edge of 'TX Clock' and the center of the corresponding bit at 'TX Out.'
13. Measured between the center of bit at 'RX Signal In' and corresponding rising edge of the 'RX Clock'.
14. Input as NRZ data and converted on chip to Manchester encoded data.
15. Output as Manchester encoded data at a frequency of twice the NRZ data rate.
16. S/N T.B.D.
17. $\overline{\text{WRITE}}$, $\overline{\text{READ}}$, $\overline{\text{CS}}$, A0 and A1 pins.
18. D0-D7 pins.
19. $\overline{\text{IRQ}}$ pin.

Section 2: Sub-Audio Tone Signaling/Detection

The following section contains specifications on MX•COM's Sub-Audio Tone Signaling/Detection IC's. Included in this section are digital, CTCSS and *Pvt* SQUELCH™ devices. *Pvt* SQUELCH, MX•COM's "privacy" method, is a combination of CTCSS and speech inversion.

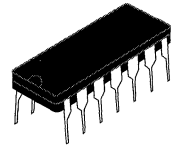
A thorough explanation of *Pvt* SQUELCH is given in the Applications section of this book (see Appendices).

Device	Description	Page	
MX315A	CTCSS Encoder	p. 155	
MX165B	CTCSS Encoder/Decoder with Audio Filter	p. 160	
MX165C	CTCSS Encoder/Decoder with Audio Filter	p. 169	**NEW**
MX365A	CTCSS Encoder/Decoder with Audio Filter	p. 178	
MX275	*Pvt* SQUELCH™ CTCSS Encoder/Decoder	p. 187	
MX375	*Pvt* SQUELCH™ CTCSS Encoder/Decoder	p. 195	
MX805A	Sub-Audio Signaling Processor	p. 204	

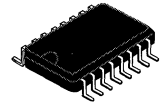
CTCSS ENCODER

Features

- **Field Programmable Tone Encoder**
- **40 CTCSS Frequencies**
- **Crystal-Controlled Frequency Stability**
- **Low Distortion Sinewave Output**
- **Few External Components Required**
- **CMOS Low Power Requirements**



MX315AJ (CDIP)
MX315AP (PDIP)
14 pins



MX315ADW
(SOIC)
16 pins

Applications

- **Mobile Radio Base Stations & Repeater Stations**
- **Mobile Radios**
- **Hand-Held Radios**
- **Industrial Controls**
- **Intercom Systems**
- **Door-Entry Systems**

Description

The MX315A is a monolithic CMOS tone encoder for sub-audible tone squelch systems. It provides three more frequencies than the earlier MX315: 69.3, 97.4 and 206.5 Hz. The tone frequencies are derived from an input reference frequency. An on-chip inverter is provided to drive an external crystal circuit.

Tone selection is achieved through six programming inputs and two control inputs (which allow either a logic "1" or "0" to enable the device). A low distortion sinewave is generated at the TX Tone Output when the MX315A is enabled. The emitter follower output stage can source 1mW directly into a 600Ω load (0dBm).

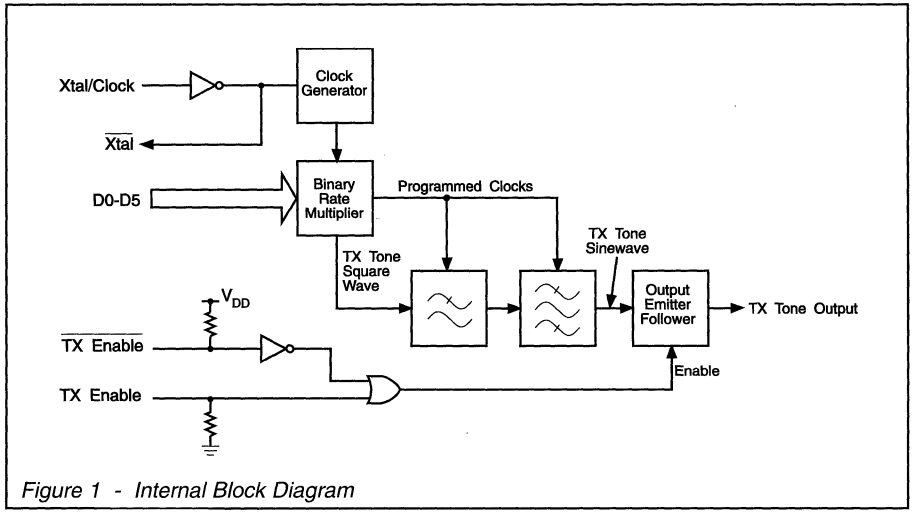


Figure 1 - Internal Block Diagram

Pin Function Chart

Pin		Function
J,P	DW	
1	1	**D3** D0-D5 are tone select inputs with internal pull-up resistors. The logic combination at
2	2	**D2** these inputs determines the encoded CTCSS tone. See Table 1.
3	3	**D1** The input sequence is not latched and may be changed at any time. A logic "1" will
4	4	**D0** be programmed if the input is open circuit, allowing the use of SPST switches.
5	5	**D4**
6	6	**D5**
7	7	**V_{SS}:** Negative Supply Voltage.
8	8	**Xtal/Clock In:** This is the input to the CMOS inverter. It can be used in conjunction with the Xtal output to form the active element in a crystal oscillator circuit. Alternatively, a logic level 1MHz frequency can be injected at this pin. However, the supply voltage should never be applied without the input clock signal.
9	9	**$\overline{\text{Xtal}}$ Output:** This is the output of the CMOS inverter. When used as a crystal oscillator, track lengths and loading of this pin should be minimized.
10	10	Internal Connection: Do not use.
	11	N/C
	12	N/C
11	13	**TX Tone Output:** This is the tone output pin. It includes a low impedance emitter follower stage for sourcing sinusoidal tone. The tone is generated about a DC level of approximately 1/2 V_{DD}. The pin is high impedance when not encoding.
12	14	**$\overline{\text{TX Enable}}$ Input:** This logic input has an internal pull-up resistor. A logic "0" at this pin enables the MX315A.
13	15	**TX Enable Input**: This logic input has an internal pull-down resistor. A logic "1" at this pin enables the MX315A.
14	16	**V_{DD}**: Positive Supply Voltage.

MX315A External Components (See Figure 2)

Figure 2 illustrates the required external components:

- The 1MΩ resistor is used to bias the internal CMOS inverter into its linear mode. A tolerance of ±20% is acceptable.
- "X1" is a parallel resonant crystal. A reference frequency of 1 MHz ±0.19% is required to maintain a tone accuracy within 0.5%.

Where two or more circuits are required to use a single oscillator (i.e. repeater applications), the signal at $\overline{\text{Xtal}}$ can be used to drive one additional Xtal/Clock input. Any further circuits can be driven from the buffered $\overline{\text{Xtal}}$ output of the second device.

The program code can be set on the D0-D5 inputs by hardwired logic levels or SPST switches to V_{SS}, as illustrated in Figure 2 (allowing the internal pull-up resistors to program a logic "1").

The MX315A provides both a $\overline{\text{TX Enable}}$ input and a TX Enable input. Either input can be used to enable the tone output, with the unused pin left open circuit (internal resistors establish a valid logic level and prevent damage). Any configuration of PTT switch or TX signal can therefore be interfaced.

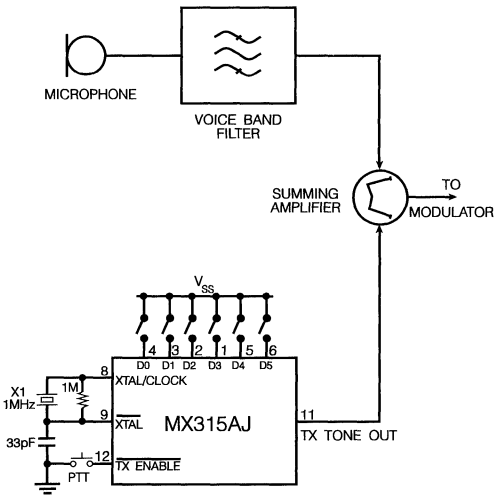


Figure 2 - External Components and Typical Application

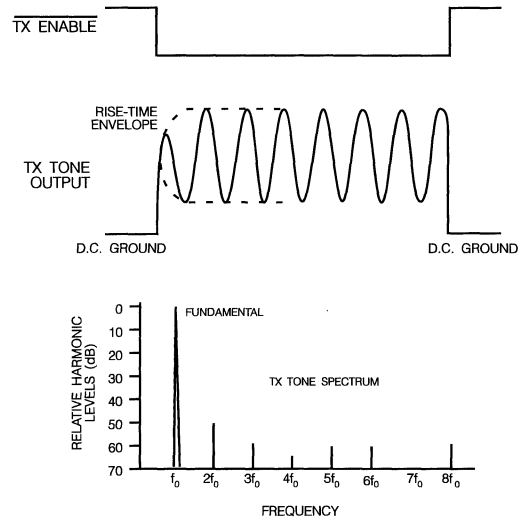


Figure 3 - Tone Encoding Sequence and Spectral Response

Application Notes

The MX315A is dedicated to Continuous Tone-controlled Squelch Systems (CTCSS) in radio applications. However, it can be used wherever encoding of low-frequency tones is required, such as intercoms, door-entry systems and various industrial applications.

The performance of a CTCSS system can be degraded if speech frequencies in the signaling spectrum are not removed prior to transmission. This can be accomplished by filtering the microphone signals to attenuate frequencies below 250 Hz. Figure 2 illustrates the addition of TX Tone Output to the filtered microphone signals prior to modulation. Figure 3 illustrates the TX Tone Output sequence and a typical spectral analysis.

Interfacing and Electromagnetic Capability

The MX315A requires a clock of 1 MHz, which is internally converted to logic level square waves. Consideration should therefore be given to possible interference problems with RF or IF circuitry caused by 1 MHz or its harmonics.

A decoupling capacitor can be used to reduce ripple on the power supply. This will reduce the level of superimposed noise on the supply caused by internal switching transients (particularly at 1 MHz and f_0).

Nominal Frequency (Hz)	MX315A Freq. (Hz)	Δfo (%)	Programming Inputs D5	D4	D3	D2	D1	D0	Hex
67.0	67.06	+.10	1	1	1	1	1	1	3F
69.3	69.37	+.10	1	1	1	0	0	1	39
71.9	71.84	-.08	0	1	1	1	1	1	1F
74.4	74.33	-.10	1	1	1	1	1	0	3E
77.0	76.99	-.02	0	0	1	1	1	1	0F
79.7	79.65	-.06	1	1	1	1	0	1	3D
82.5	82.50	0.0	0	1	1	1	1	0	1E
85.4	85.34	-0.7	1	1	1	1	0	0	3C
88.5	88.62	+.14	0	0	1	1	1	0	0E
91.5	91.38	-.13	1	1	1	0	1	1	3B
94.8	94.88	+.08	0	1	1	1	0	1	1D
97.4	97.46	+.06	1	1	1	0	1	0	3A
100.0	99.87	-.13	0	0	1	1	0	1	0D
103.5	103.39	-.11	0	1	1	1	0	0	1C
107.2	107.17	-.03	0	0	1	1	0	0	0C
110.9	110.85	-.04	0	1	1	0	1	1	1B
114.8	114.80	0.0	0	0	1	0	1	1	0B
118.8	118.60	-.17	0	1	1	0	1	0	1A
123.0	123.12	+.10	0	0	1	0	1	0	0A
127.3	127.50	+.16	0	1	1	0	0	1	19
131.8	131.67	-.10	0	0	1	0	0	1	09
136.5	136.69	+.14	0	1	1	0	0	0	18
141.3	141.48	+.13	0	0	1	0	0	0	08
146.2	145.96	-.16	0	1	0	1	1	1	17
151.4	151.45	+.03	0	0	0	1	1	1	07
156.7	156.59	-.07	0	1	0	1	1	0	16
162.2	162.10	-.06	0	0	0	1	1	0	06
167.9	168.01	+.07	0	1	0	1	0	1	15
173.8	173.43	-.21	0	0	0	1	0	1	05
179.9	180.21	+.17	0	1	0	1	0	0	14
186.2	186.46	+.14	0	0	0	1	0	0	04
192.8	193.16	+.19	0	1	0	0	1	1	13
203.5	202.88	-.31	0	0	0	0	1	1	03
206.5	206.78	+.14	1	1	1	0	0	0	38
210.7	210.84	+.07	0	1	0	0	1	0	12
218.1	217.96	-.07	0	0	0	0	1	0	02
225.7	225.58	-.05	0	1	0	0	0	1	11
233.6	233.75	+.07	0	0	0	0	0	1	01
241.8	242.54	+.31	0	1	0	0	0	0	10
250.3	250.06	+.10	0	0	0	0	0	0	00
Test	4032	0.0	1	1	0	0	1	1	33 (or any invalid address)

Table 1 - CTCSS Tone Programming

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3V to 7.0 V
Device Dissipation @ 85°C	100mW
Operating Temperature	-30°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5V

T_{AMB} = 25°C

Clock = 1MHz

Characteristics	See Note	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD})		4.5	5.0	5.5	V
Supply Current (operating)		-	1.5	4.5	mA
Input Impedance	1	-	500	-	kΩ
Input Impedance	2	-	10	-	MΩ
Logic Input "1"		3.5	-	-	V
Logic Input "0"		-	-	1.5	V
TX Output EMF	3	550	775	-	mVrms
TX Risetime		-	1	-	ms
TX Tone Output Load Current		-	-	5	mA
TX Distortion	3	-	2	5	%
Variation in Output Level Between Tones	3	-	0.1	-	dB

Notes:

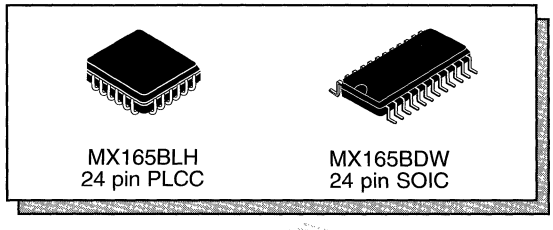
1. Refers to D0, D1, D2, D3, D4, D5, TX Enable and $\overline{\text{TX Enable}}$ inputs.
2. Refers to Xtal/Clock input.
3. Any program tone and R_L = 600, C_L = 15pF. THD measurements are taken in the 0-6 kHz bandwidth.

CTCSS ENCODER/DECODER
WITH TX/RX AUDIO FILTERS

FEATURES
- 39 CTCSS Tones + Notone
- TX/RX Audio Filters
- TX Tone Phase Reversals
- Serial or Parallel Programming
- Low Voltage Supply: 3.0 to 5.5 V

BENEFITS
- Scanning of any Channel
- Improved Sinad
- Squelch Tail Elimination
- Easy µP Interface

APPLICATIONS
- Mobile Radio Channel Sharing
- Wireless Intercom
- TIA/EIA-603 - 37 Tone Plus 97.4Hz & 69.3Hz
- Serves 3-Cell Applications



Description

Voice on shared radio channels is multiplexed with a subaudible CTCSS tone as a means of directing messages among user groups sharing the same RF frequency. Continuous Tone Controlled Squelch System (CTCSS) modulates the transmitter with a discrete tone, taken from a field of 39 in the range of 67 to 250 Hz, according to TIA/EIA-603 Standard plus 69.3Hz and 97.4Hz. Groups of radio receivers, segregated by common interest and assigned tone, demodulate the voice/tone mixture for voice messages to be heard.

The MX165B CTCSS Encoder/Decoder enhances voice/tone multiplexing with an on-chip filter that attenuates TX speech 36dB at 250Hz, while passing signals >300Hz with only ±1dB of ripple.

Early CTCSS designs did not filter TX speech, depending instead on the host transmitter's pre-emphasis network. At only 6dB/octave, their attenuation of speech components at the higher CTCSS tones was only a few dB, which resulted in "talk-off" (low frequency voice components unsquelching the receiver audio).

The MX165B features TX/RX selection and a LOAD/$\overline{\text{LATCH}}$ pin. A Notone program code has been included to permit scanning channels without CTCSS. A choice of serial or parallel tone programming is offered. Operation of the PTL signal during TX reverses the phase of the transmitted CTCSS tone by 180°. This is used in some radios to eliminate squelch tails.

The MX165B requires a single 3.75- or 5-volt supply and a 1 MHz clock or crystal.

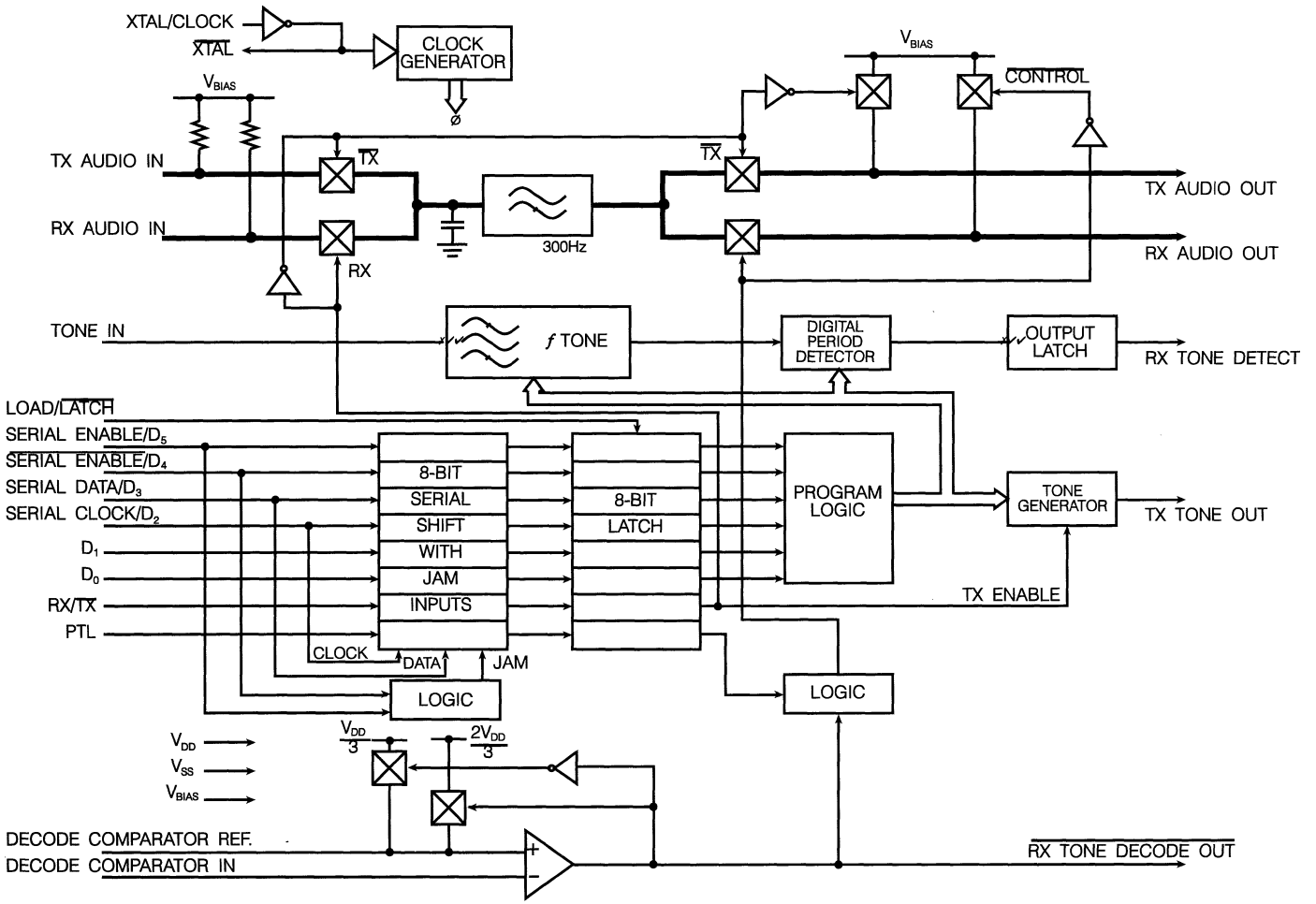


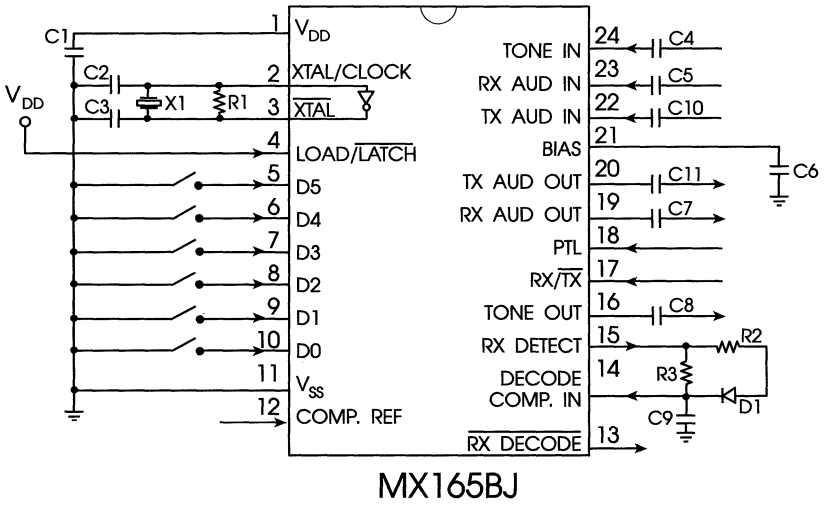
Figure 1 - MX165B Internal Block Diagram

PIN FUNCTION TABLE

Pin	Function
MX165A MX365A	
1	**V_{DD}:** Positive Supply.
2	**Xtal/Clock:** Input to the on-chip inverter used with a 1 MHz Xtal or external clock source.
3	**$\overline{\text{Xtal}}$:** Output of the on-chip inverter (clock output).
4	**Load/$\overline{\text{Latch}}$:** Controls 8 on-chip latches and is used to latch RX/TX, PTL, and D0-D5. This pin is internally pulled to V_{DD}. A logic "1" applied to this input puts the 8 latches in "transparent" mode. A logic "0" applied to this input puts the 8 latches in the "latched" mode. In parallel mode data is loaded and latched by a logic 1-0 transition (see Fig. 3). In serial mode data is loaded and latched by a 0-1-0 strobe pulse on this pin (see Fig. 4).
5	**D5/Serial Enable 1:** Data input D5 (in parallel mode). A logic "1" applied to this input together with a logic "0" applied to D4/Serial Enable 2 will put the device in serial mode (see Fig. 4). This pin is internally pulled to V_{DD}.
6	**D4/$\overline{\text{Serial Enable 2}}$:** Data input D4 (in parallel mode). A logic "0" applied to this input together with a logic "1" on pin 5 will place the device in serial mode (see Fig. 5). This pin is internally pulled to V_{DD}.
7	**D3/Serial Data Input:** Data input D3 (in parallel mode). In serial mode this pin becomes the serial data input for D5-D0, RX/TX and PTL (see Fig. 4). D5 is clocked first and PTL last. This pin is internally pulled to V_{DD}.
8	**D2/Serial Clock:** Data input D2 (in parallel mode). In serial mode this pin becomes the serial clock input. Data is clocked on the positive going edge (see Fig. 4). This pin is internally pulled to V_{DD}.
9	**D1:** Data input D1 (in parallel mode). This pin is internally pulled to V_{DD}.
10	**D0:** Data input D0 (in parallel mode). This pin is internally pulled to V_{DD}.
11	**V_{SS}:** Negative supply.
12	**Decode Comparator Ref.:** This pin is internally biased to $V_{DD}/3$ or $2V_{DD}/3$ via 1M resistors depending on the logical state of the RX Tone Decode Out pin. RX Tone Decode Out = 1 will bias this input $2V_{DD}/3$; a logic "0" will bias this input $V_{DD}/3$. This input provides the decode comparator reference voltage, and switching of bias voltages provides hysteresis to reduce "chatter" under marginal conditions.
13	**$\overline{\text{RX Tone Decode Out}}$:** This is the gated output of the decode comparator. This output is used to gate the RX Audio path. A logic "0" on this pin indicates a successful decode and that the Decode Comparator Input pin is more positive than the Decode Comparator Ref. input (see Table 1).
14	**Decode Comparator Input:** This is the inverting input of the decode comparator. This pin is normally connected to the integrated output of the RX Tone Detect line.
15	**RX Tone Detect:** In RX mode this output will go to logic "1" during a successful decode. It must be externally integrated to control response and deresponse times (see Table 1).
16	**TX Tone Out:** The CTCSS sinewave output appears on this pin under control of the RX/$\overline{\text{TX}}$ pin. This pin, when not transmitting a tone, may be biased to V_{DD}-0.7V or O/C (see Table 1). This pin is an emitter follower output with high impedance load, requiring capacitive coupling or a low impedance (<1kΩ) load to ground.

PIN FUNCTION TABLE

Pin	Function
17	**RX/$\overline{TX}$:** This input (in parallel mode) selects RX or TX modes (see Fig. 2). In serial mode this function is serially loaded. This pin is internally pulled to V_{DD} via a 1MΩ resistor.
18	**PTL:** In parallel RX mode this pin operates as a "Push To Listen" function by enabling the RX audio path, thus overriding the tone squelch function. In parallel TX mode this pin reverses the phase of the transmitted CTCSS tone (used for squelch tail elimination). In serial mode this function is serially loaded (see Fig. 2).
19	**RX Audio Out:** This is the high pass filtered receive audio output pin. This pin outputs audio when RX Tone Decode = 0, or PTL = 1, or when Notone is programmed (see Table 2). In TX mode this pin is biased to $V_{DD}/2$.
20	**TX Audio Out:** This is the high pass filtered transmit audio output pin. In TX mode this pin outputs audio present at the TX Audio Input pin. In RX mode this pin is biased to $V_{DD}/2$.
21	**Bias:** This pin is the output of an internally generated $V_{DD}/2$ bias level and would normally be externally decoupled to V_{SS} via capacitor C7.
22	**TX Audio In:** This is the TX Audio input pin. In TX mode it may be prefiltered, using the TX audio path, thus helping to aviod talkoff due to intermodulation of speech frequencies with the transmitted CTCSS tone. This pin is internally biased to $V_{DD}/2$.
23	**RX Audio In:** This is the input to the audio high pass filter in RX mode. It is internally biased to $V_{DD}/2$.
24	**Tone Input:** This is the input to the CTCSS tone detector. It is internally biased to $V_{DD}/2$.
	NOTE: Pins labeled "N/C" (no connect) may have internal connections. Do Not Use.



MX165BJ

Component	Values
R1	1MΩ
R2	560kΩ
R3	820kΩ
X1	1MHz
C1	0.1µF
C2	68pF
C3	33pF
C4	0.1µF
C5	0.1µF
C6	0.47µF
C7	0.1µF
C8	0.1µF
C9	0.1µF
C10	0.1µF
C11	0.1µF
D1	small signal

Tolerances: Resistors: ±10%
Capacitors: ±20%
Xtal: ±0.1%

Figure 2 - External Component Diagram

I/O CONDITIONS

	INPUT PIN CONDITION			OUTPUT PIN CONDITION		RESULT/FUNCTION					
D0-D5	RX/$\overline{TX}$	PTL	Decode Comp. Input	RX Tone Detect	$\overline{\text{Tone}}$ Decode	Tone Transmitter Enabled	TX Tone Phase Reversed	TX Audio Path Enabled	Tone Decoder Enabled	RX Audio Path Enabled	Notes
Tone	0	0	X	0	1	Yes	No	Yes	No	No (bias)	1a
Tone	0	1	X	0	1	Yes	Yes	Yes	No	No (bias)	1b
No tone	0	X	X	0	1	No (bias)	X	Yes	No	No (bias)	2
Tone	1	0	0	0	1	No (o/c)	X	No	Yes	No (bias)	3a
Tone	1	1	0	0	1	No (o/c)	X	No	Yes	Yes	3b
Tone	1	X	1	1	0	No (o/c)	X	No	Yes	Yes	4
No tone	1	X	X	X	0	No (o/c)	X	No	Yes	Yes	5

Table 1 - Combinations of Input/Output Conditions

o/c = open circuit
X = don't care

Notes:

1a. Normal tone transmit condition.
1b. Tone transmit with phase reversed.
2 Notone programmed in TX mode, tone transmit O/P set to $V_{DD}/2$ - 0.7V. TX audio path enabled.
3a. Normal decode standby.
3b. Normal decode standby with PTL used to enable audio.
4. Normal decode of correct CTCSS tone condition, PTL has no effect.
5. Notone programmed in RX mode, tone transmit O/P (o/c). RX audio path enabled.

FILTER RESPONSE

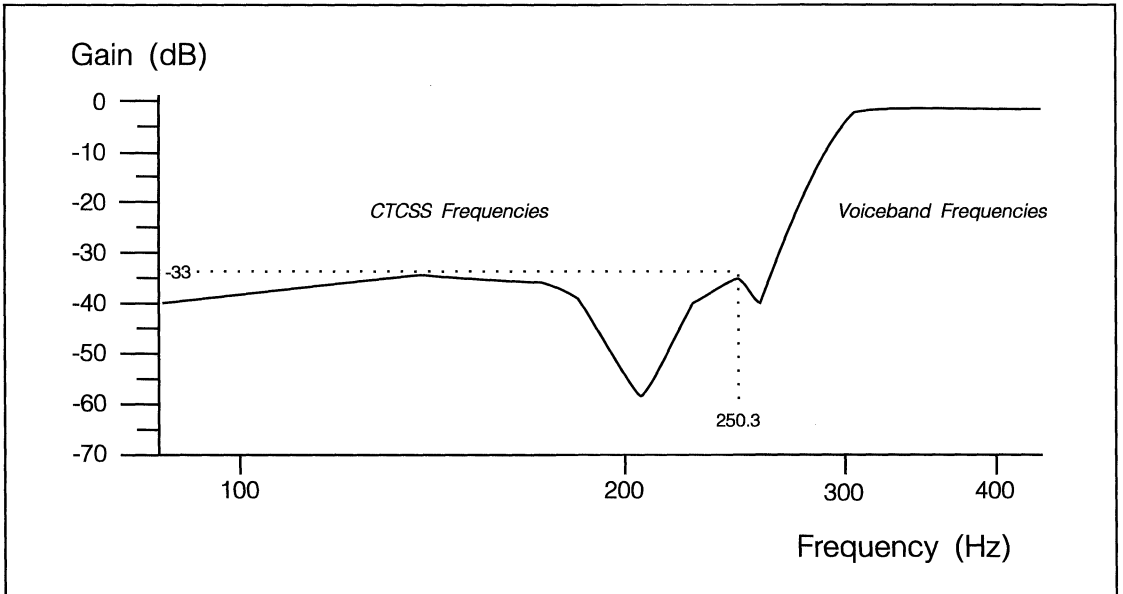
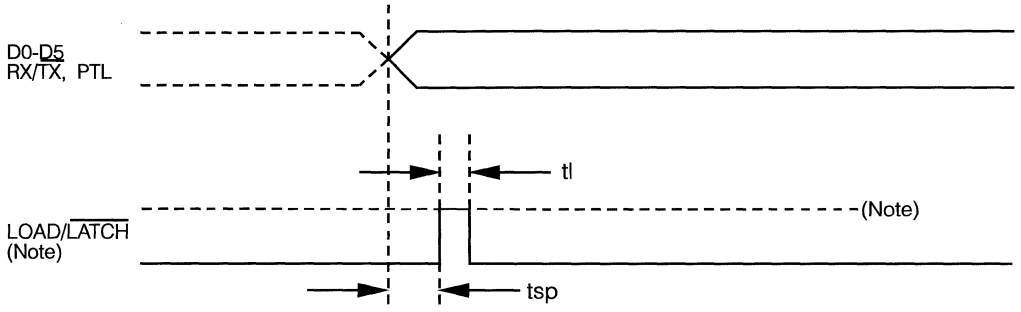


Figure 3 - Voiceband Filter Response

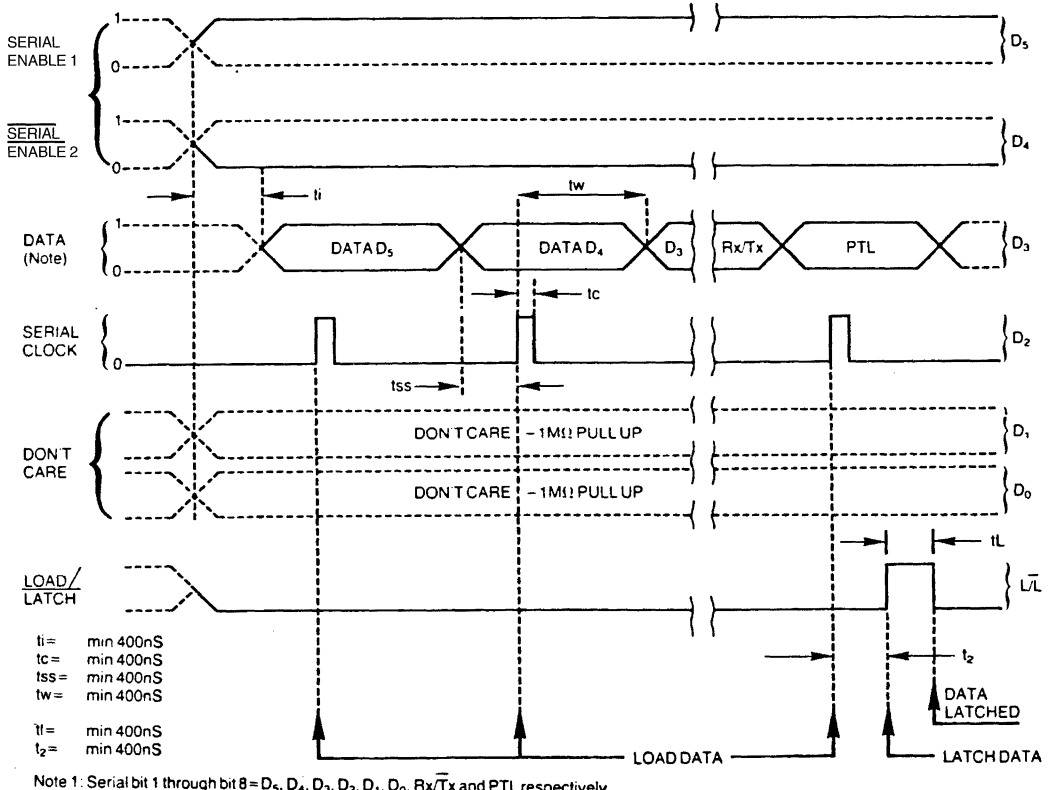
SERIAL AND PARALLEL MODE TIMING



Note: For wired, non microprocessor applications Load/Latch should be connected to V_{DD}.

tl min. = 400ns
tsp min. = 400ns

Figure 4 - Parallel Mode (not to scale)



Note 1: Serial bit 1 through bit 8 = D_5, D_4, D_3, D_2, D_1, D_0, Rx/$\overline{Tx}$ and PTL respectively.
Load bit 1 first, bit 8 last.

Figure 5 - Serial Mode (not to scale)

CTCSS PROGRAMMING TABLE

Tone			Programming Inputs						
Nominal Frequency (Hz)	MX165B Freq. (Hz)	△fo (%)	D5	D4	D3	D2	D1	D0	Hex
67.0	67.05	+0.07	1	1	1	1	1	1	3F
69.3	69.32	+.03	1	1	1	0	0	1	39
71.9	71.9	0	0	1	1	1	1	1	1F
74.4	74.35	-0.07	1	1	1	1	1	0	3E
77.0	76.96	-0.05	0	0	1	1	1	1	0F
79.7	79.77	+0.09	1	1	1	1	0	1	3D
82.5	82.59	+0.1	0	1	1	1	1	0	1E
85.4	85.38	-0.2	1	1	1	1	0	0	3C
88.5	88.61	+0.13	0	0	1	1	1	0	0E
91.5	91.58	+0.09	1	1	1	0	1	1	3B
94.8	94.76	-0.04	0	1	1	1	0	1	1D
97.4	97.29	-0.11	1	1	1	0	1	0	3A
100.0	99.96	-0.04	0	0	1	1	0	1	0D
103.5	103.43	-0.07	0	1	1	1	0	0	1C
107.2	107.15	-0.05	0	0	1	1	0	0	0C
110.9	110.77	-0.12	0	1	1	0	1	1	1B
114.8	114.64	-0.14	0	0	1	0	1	1	0B
118.8	118.8	0	0	1	1	0	1	0	1A
123.0	122.8	-0.17	0	0	1	0	1	0	0A
127.3	127.08	-0.17	0	1	1	0	0	1	19
131.8	131.67	-0.10	0	0	1	0	0	1	09
136.5	136.61	+0.08	0	1	1	0	0	0	18
141.3	141.32	+0.02	0	0	1	0	0	0	08
146.2	146.37	+0.12	0	1	0	1	1	1	17
151.4	151.09	-0.2	0	0	0	1	1	1	07
156.7	156.88	+0.11	0	1	0	1	1	0	16
162.2	162.31	+0.07	0	0	0	1	1	0	06
167.9	168.14	+0.14	0	1	0	1	0	1	15
173.8	173.48	-0.19	0	0	0	1	0	1	05
179.9	180.15	+0.14	0	1	0	1	0	0	14
186.2	186.29	+0.05	0	0	0	1	0	0	04
192.8	192.86	+0.03	0	1	0	0	1	1	13
203.5	203.65	+0.07	0	0	0	0	1	1	03
210.7	210.17	-0.25	0	1	0	0	1	0	12
218.1	218.58	+0.22	0	0	0	0	1	0	02
225.7	226.12	+0.18	0	1	0	0	0	1	11
233.6	234.19	+0.25	0	0	0	0	0	1	01
241.8	241.08	-0.30	0	1	0	0	0	0	10
250.3	250.28	-0.01	0	0	0	0	0	0	00
Notone		N/A	1	1	0	0	0	0	30
Serial Input Mode		N/A	1	0	Data	Clock	X	X	2X
Test	4082	N/A	1	1	0	0	1	1	33 or any invalid address

Table 2 - CTCSS Tones

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 V to V_{DD} + 0.3 V
Sink/Source Current (supply pins)	±30mA
(other pins)	±20mA
Maximum Device Dissipation	100mW
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 3.75V
T_{AMB}=25°C
Xtal/Clock f_0 = 1.0 MHz
0dB ref. = 100mVrms @ 1kHz

Composite signal: 1kHz test tone at 300 mVrms, 75 mVrms noise (band limited 6kHz gaussian white noise), 30 mVrms CTCSS tone.

2

Characteristics	See Note	Min.	Typ.	Max.	Unit
STATIC VALUES					
Supply Voltage		3.0	3.75	5.5	V
Supply Current					
TX		-	-	3.5	mA
RX		-	-	3.5	mA
Tone Input Impedance		-	1	-	MΩ
Tone Output Impedance		-	4	-	kΩ
Audio Input Impedance		-	1	-	MΩ
Audio Output Impedance		-	1	-	kΩ
Digital Input Impedance	1	-	1	-	MΩ
Input logic"1"	1	70%V_{DD}	-	-	V
Input logic "0"	1	-	-	30%V_{DD}	V
Logic "1" output 1' source = 0.1mA	2	80%V_{DD}	-	-	V
Logic "0" output 1' sink - 0.1mA	2	-	-	20%V_{DD}	V
DYNAMIC VALUES					
Decoder					
Decode Input Signal Level	3	30	-	-	mVrms
Decode Response Time	3,6,10	-	-	250	ms
Deresponse Time	3,6,10	-	180	250	ms
Decode Selectivity (see Fig. 6)	3,12	±0.5	-	-	%f_0

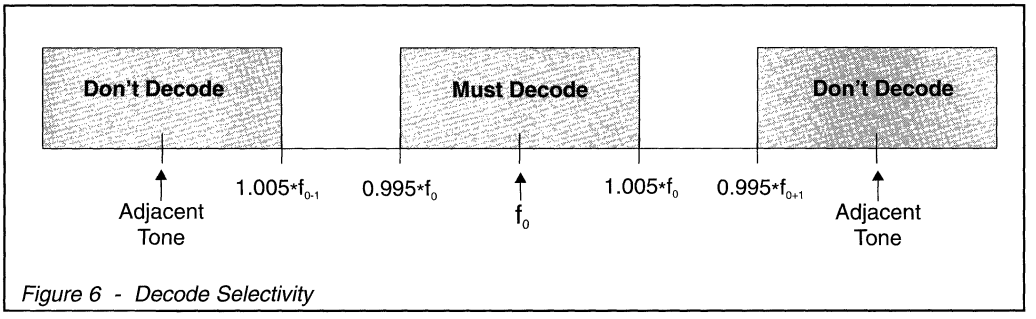


Figure 6 - Decode Selectivity

Characteristics	See Note	Min.	Typ.	Max.	Unit
Encoder					
Tone Output Level		400	627	800	mVrms
Tone Frequency Accuracy (f error)		-0.3	-	+0.3	$\%f_0$
Risetime to 90% nominal O/P:					
f_0>100Hz	4,10	-	55	-	ms
f_0<100Hz	4,10	-	70	-	ms
Tone Output Load Current		-	-	5	mA
Total Harmonic Distortion		-	2	5	%
Output Level Variation Between Tones	11	-1.0	-	+1.0	dB
TX Output Impedance		-	2.0	-	kΩ
Audio Filter					
Total Harmonic Distortion	5,10	-	2	5	%
Output Noise Level	8	-	2	-	mVrms
(input a.c. short circuit, audio switch enabled)					
Sinad	9	36	40	-	dB
Spurious Emissions	13	-	-48	-	dB
Cutoff Frequency	7	-	300	-	Hz
Passband		300	-	3000	Hz
Bandpass Ripple		-	-	2	dB
Stopband Attenuation <250Hz	5,7	33	36	-	dB
Passband Gain 1kHz		-2.0	-	0.5	dB
Audio Switch					
Isolation	5	-	60	-	dB
Serial/Parallel Inputs (See Figures 3 &4)					
Parallel Set-up Time t_{SP}		400	-	-	ns
Load/Latch Pulse Width t_l		400	-	-	ns
Serial Clock Pulse Width t_C		400	-	-	ns
Serial Set-up Time t_{SS}		400	-	-	ns
Serial Clock Frequency		-	1	-	MHz

NOTES:

1. Refers to RX/TX, PTL, Decode Comparator Input, D0-D5.
2. All logic outputs.
3. Composite Signal Test Condition.
4. Any programming tone and RL = 10,000, CL = 15pF. This includes response to a phase reversal instruction.
5. 1kHz references = 0dB.
6. f_0>100Hz (for 100 Hz>f_0>67Hz: t = 100/f_0Hz x 250ms)
7. See Figure 3.
8. Measured in a 30kHz bandwidth.
9. Measured with an input level of 100 mV @ 1kHz, in a 30 kHz bandwidth.
10. Per TIA/EIA-603.
11. Ref. to 100 Hz.
12. Complies with TIA/EIA-603, must not decode adjacent fo ±0.5%.
13. Test system resolution is ≈ -35dB.

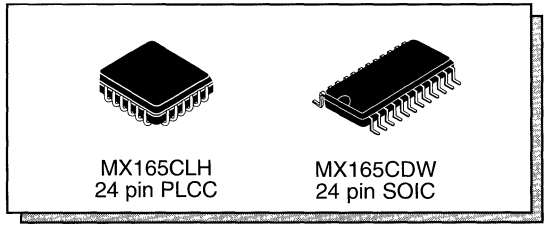
Advance Information

LOW VOLTAGE CTCSS ENCODER/DECODER
WITH TX/RX AUDIO FILTERS

FEATURES
- **MX•COM MiXed Signal CMOS**
- **47 CTCSS Tones + Notone**
- **TX/RX Audio Filters**
- **TX Tone Phase Reversals**
- **Serial or Parallel Programming**
- **Meets TIA/EIA-603 Land Mobile Standard***

BENEFITS
- **Scanning of any Channel**
- **Improved Sinad**
- **Squelch Tail Elimination**
- **Easy µP Interface**

APPLICATIONS
- **Mobile Radio Channel Sharing**
- **Wireless Intercom**
- **Serves 3-Cell Applications**



Description

Voice on shared radio channels is multiplexed with a subaudible CTCSS tone as a means of directing messages among user groups sharing the same RF frequency. Continuous Tone Controlled Sub-audible Squelch (CTCSS) modulates the transmitter with a discrete tone, taken from a field of 39 in the range of 67 to 250 Hz, according to TIA/EIA-603 Standard plus 159.8Hz, 183.5Hz, 189.9Hz, 196.6Hz, 199.5Hz, 206.5Hz, 229.1Hz, and 254.1Hz. Groups of radio receivers, segregated by common interest and assigned tone, demodulate the voice/tone mixture for voice messages to be heard.

The MX165C CTCSS Encoder/Decoder enhances voice/tone multiplexing with an on-chip filter that attenuates TX speech 36dB at frequencies below 250Hz, while passing signals >300Hz with only ±1dB of ripple.

Early CTCSS designs did not filter TX speech, depending instead on the host transmitter's pre-emphasis network. At only 6dB/octave, their attenuation of speech components at the higher CTCSS tones was only a few dB, which resulted in "talk-off" (low frequency voice components unsquelching the receiver audio).

The MX165C features TX/RX selection and a LOAD/LATCH pin. A Notone program code has been included to permit scanning channels without CTCSS. A choice of serial or parallel tone programming is offered. Operation of the PTL signal during TX reverses the phase of the transmitted CTCSS tone by 180°. This is used in some radios to eliminate squelch tails.

The MX165C requires a single 3.75-volt supply and a 1 MHz clock or crystal.

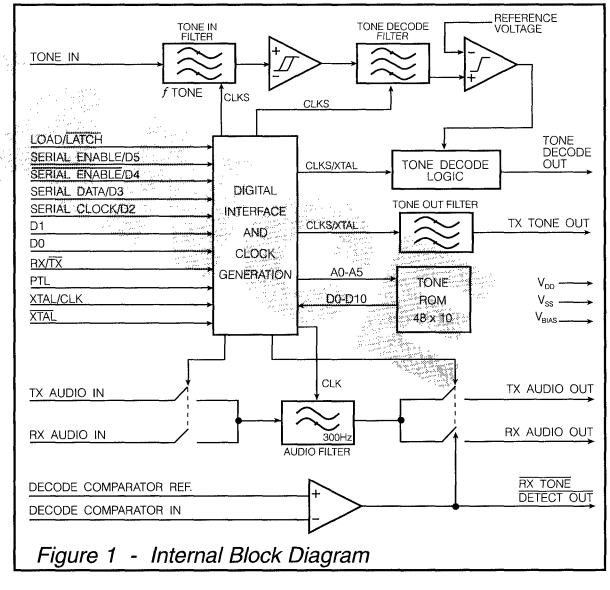


Figure 1 - Internal Block Diagram

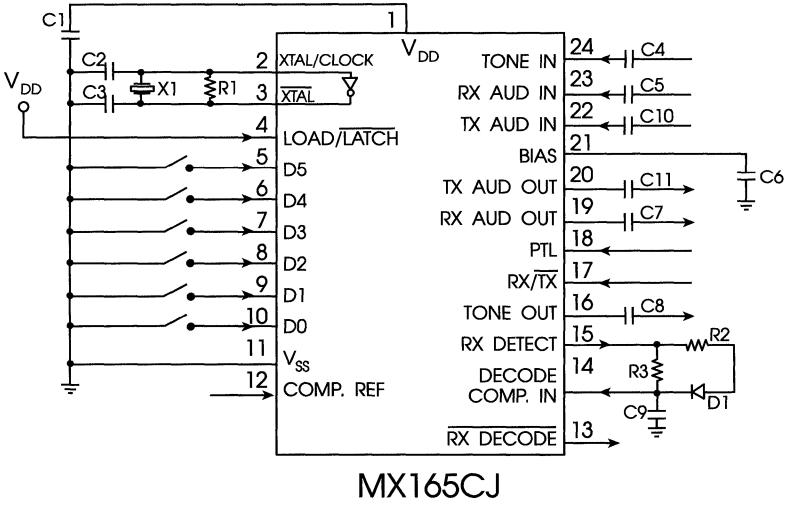
** The following tones are not specified in the TIA/EIA-603 Standard, and do not meet the Standard when used with their adjacent tones: 159.8Hz, 183.5Hz, 189.9Hz, 196.6Hz, 199.5Hz, 206.5Hz, 229.1Hz, and 254.1Hz.*

PIN FUNCTION TABLE

Pin	Function
1	**V_{DD}:** Positive Supply.
2	**Xtal/Clock:** Input to the on-chip inverter used with a 1 MHz Xtal or external clock source.
3	**$\overline{\text{Xtal}}$:** Output of the on-chip inverter (clock output).
4	**Load/$\overline{\text{Latch}}$:** Controls 8 on-chip latches and is used to latch RX/TX, PTL, and D0-D5. This pin is internally pulled to V_{DD}. A logic "1" applied to this input puts the 8 latches in "transparent" mode. A logic "0" applied to this input puts the 8 latches in the "latched" mode. In parallel mode data is loaded and latched by a logic 1-0 transition (see Fig. 3). In serial mode data is loaded and latched by a 0-1-0 strobe pulse on this pin (see Fig. 4).
5	**D5/Serial Enable 1:** Data input D5 (in parallel mode). A logic "1" applied to this input together with a logic "0" applied to D4/Serial Enable 2 will put the device in serial mode (see Fig. 4). This pin is internally pulled to V_{DD}.
6	**D4/$\overline{\text{Serial Enable 2}}$:** Data input D4 (in parallel mode). A logic "0" applied to this input together with a logic "1" on pin 5 will place the device in serial mode (see Fig. 5). This pin is internally pulled to V_{DD}.
7	**D3/Serial Data Input:** Data input D3 (in parallel mode). In serial mode this pin becomes the serial data input for D5-D0, RX/TX and PTL (see Fig. 4). D5 is clocked first and PTL last. This pin is internally pulled to V_{DD}.
8	**D2/Serial Clock:** Data input D2 (in parallel mode). In serial mode this pin becomes the serial clock input. Data is clocked on the positive going edge (see Fig. 4). This pin is internally pulled to V_{DD}.
9	**D1:** Data input D1 (in parallel mode). This pin is internally pulled to V_{DD}.
10	**D0:** Data input D0 (in parallel mode). This pin is internally pulled to V_{DD}.
11	**V_{SS}:** Negative supply.
12	**Decode Comparator Ref.:** This pin is internally biased to $V_{DD}/3$ or $2V_{DD}/3$ via 1M resistors depending on the logical state of the RX Tone Decode Out pin. RX Tone Decode Out = 1 will bias this input $2V_{DD}/3$; a logic "0" will bias this input $V_{DD}/3$. This input provides the decode comparator reference voltage, and switching of bias voltages provides hysteresis to reduce "chatter" under marginal conditions.
13	**$\overline{\text{RX Tone Decode Out}}$:** This is the gated output of the decode comparator. This output is used to gate the RX Audio path. A logic "0" on this pin indicates a successful decode and that the Decode Comparator Input pin is more positive than the Decode Comparator Ref. input (see Table 1).
14	**Decode Comparator Input:** This is the inverting input of the decode comparator. This pin is normally connected to the integrated output of the RX Tone Detect line.
15	**RX Tone Detect:** In RX mode this output will go to logic "1" during a successful decode. It must be externally integrated to control response and deresponse times (see Table 1).
16	**TX Tone Out:** The CTCSS sinewave output appears on this pin under control of the RX/$\overline{\text{TX}}$ pin. This pin, when not transmitting a tone, may be biased to V_{DD}-0.7V or O/C (see Table 1).

PIN FUNCTION TABLE

Pin	Function
17	**RX/$\overline{TX}$:** This input (in parallel mode) selects RX or TX modes (see Fig. 2). In serial mode this function is serially loaded. This pin is internally pulled to V_{DD} via a 1MΩ resistor.
18	**PTL:** In parallel RX mode this pin operates as a "Push To Listen" function by enabling the RX audio path, thus overriding the tone squelch function. In parallel TX mode this pin reverses the phase of the transmitted CTCSS tone (used for squelch tail elimination). In serial mode this function is serially loaded (see Fig. 2).
19	**RX Audio Out:** This is the high pass filtered receive audio output pin. This pin outputs audio when RX Tone Decode = 0, or PTL = 1, or when Notone is programmed (see Table 2). In TX mode this pin is biased to $V_{DD}/2$.
20	**TX Audio Out:** This is the high pass filtered transmit audio output pin. In TX mode this pin outputs audio present at the TX Audio Input pin. In RX mode this pin is biased to $V_{DD}/2$.
21	**Bias:** This pin is the output of an internally generated $V_{DD}/2$ bias level and would normally be externally decoupled to V_{SS} via capacitor C7.
22	**TX Audio In:** This is the TX Audio input pin. In TX mode it may be prefiltered, using the TX audio path, thus helping to aviod talkoff due to intermodulation of speech frequencies with the transmitted CTCSS tone. This pin is internally biased to $V_{DD}/2$.
23	**RX Audio In:** This is the input to the audio high pass filter in RX mode. It is internally biased to $V_{DD}/2$.
24	**Tone Input:** This is the input to the CTCSS tone detector. It is internally biased to $V_{DD}/2$.



Component	Values
R1	1MΩ
R2	560kΩ
R3	820kΩ
X1	1MHz
C1	0.1µF
C2	68pF
C3	33pF
C4	0.1µF
C5	0.1µF
C6	0.47µF
C7	0.1µF
C8	0.1µF
C9	0.1µF
C10	0.1µF
C11	0.1µF
D1	small signal

Tolerances: Resistors: ±10%
Capacitors: ±20%
Xtal: ±0.1%

Figure 2 - External Components

I/O CONDITIONS

	INPUT PIN CONDITION			OUTPUT PIN CONDITION		RESULT/FUNCTION					
D0-D5	RX/$\overline{TX}$	PTL	Decode Comp. Input	RX Tone Detect	$\overline{\text{Tone}}$ Decode	Tone Transmitter Enabled	TX Tone Phase Reversed	TX Audio Path Enabled	Tone Decoder Enabled	RX Audio Path Enabled	Notes
Tone	0	0	X	0	1	Yes	No	Yes	No	No (bias)	1a
Tone	0	1	X	0	1	Yes	Yes	Yes	No	No (bias)	1b
No tone	0	X	X	0	1	No (bias)	X	Yes	No	No (bias)	2
Tone	1	0	0	0	1	No (o/c)	X	No	Yes	No (bias)	3a
Tone	1	1	0	0	1	No (o/c)	X	No	Yes	Yes	3b
Tone	1	X	1	1	0	No (o/c)	X	No	Yes	Yes	4
No tone	1	X	X	X	0	No (o/c)	X	No	Yes	Yes	5

Table 1 - Combinations of Input/Output Conditions

o/c = open circuit
X = don't care

Notes:

1a. Normal tone transmit condition.
1b. Tone transmit with phase reversed.
2 Notone programmed in TX mode, tone transmit O/P set to $V_{DD}/2$. TX audio path enabled.
3a. Normal decode standby.
3b. Normal decode standby with PTL used to enable audio.
4. Normal decode of correct CTCSS tone condition, PTL has no effect.
5. Notone programmed in RX mode, tone transmit O/P (o/c). RX audio path enabled.

FILTER RESPONSE

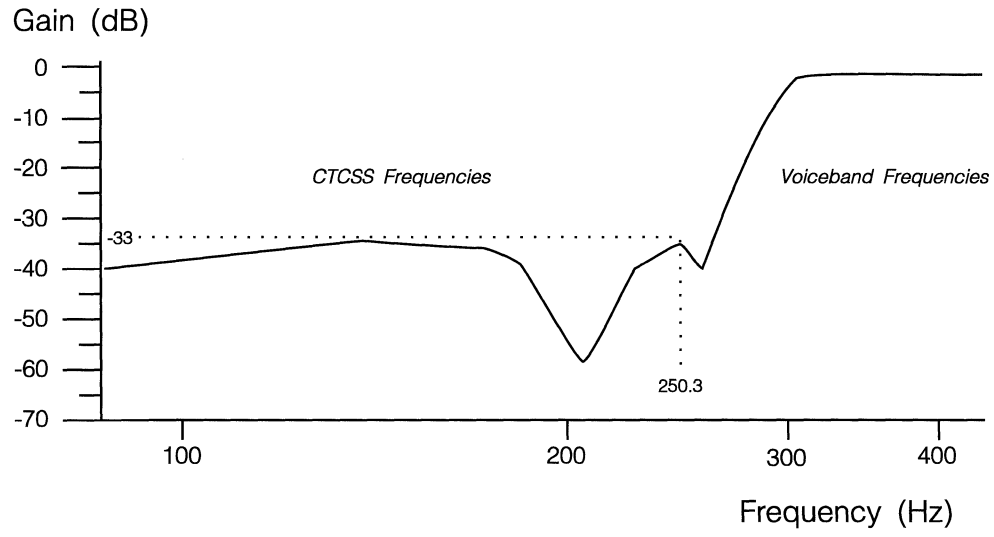
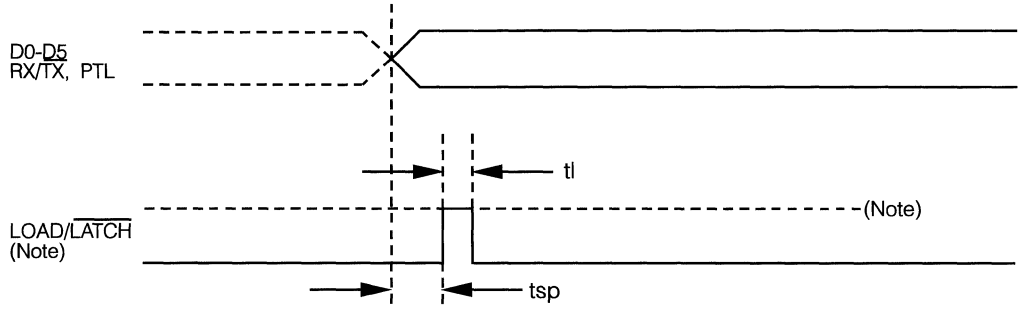


Figure 3 - Voiceband Filter Response

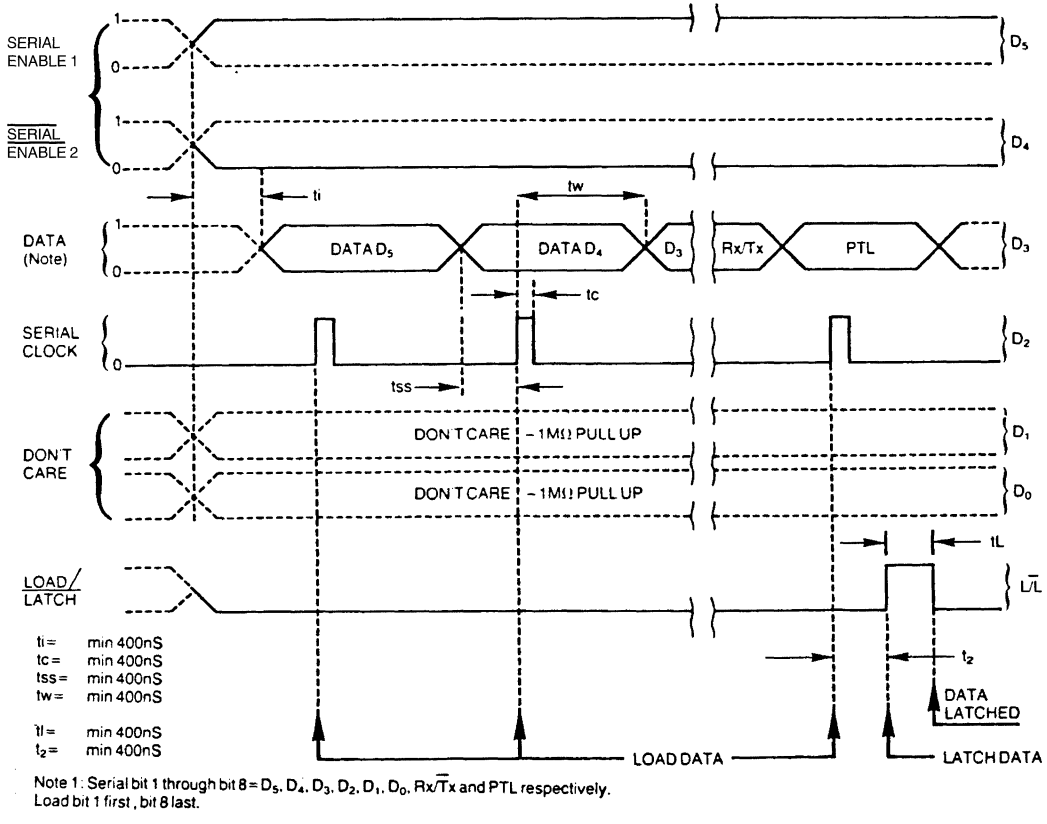
SERIAL AND PARALLEL MODE TIMING



Note: For wired, non microprocessor applications Load/Latch should be connected to V_{DD}.

tl min. = 400ns
tsp min. = 400ns

Figure 4 - Parallel Mode (not to scale)



Note 1: Serial bit 1 through bit 8 = D_5, D_4, D_3, D_2, D_1, D_0, Rx/$\overline{Tx}$ and PTL respectively.
Load bit 1 first, bit 8 last.

Figure 5 - Serial Mode (not to scale)

CTCSS PROGRAMMING TABLE

Tone			Programming Inputs						
TIA/EIA-603 Nominal Frequency (Hz)	MX165C Freq. (Hz)	Δf_0 (%)	D5	D4	D3	D2	D1	D0	Hex
67.0	66.98	-0.029	1	1	1	1	1	1	3F
69.3	69.32	0.024	1	1	1	0	0	1	39
71.9	71.901	0.001	0	1	1	1	1	1	1F
74.4	74.431	0.042	1	1	1	1	1	0	3E
77.0	76.965	-0.046	0	0	1	1	1	1	0F
79.7	79.677	-0.029	1	1	1	1	0	1	3D
82.5	82.483	-0.021	0	1	1	1	1	0	1E
85.4	85.383	-0.020	1	1	1	1	0	0	3C
88.5	88.494	-0.007	0	0	1	1	1	0	0E
91.5	91.456	-0.048	1	1	1	0	1	1	3B
94.8	94.76	-0.042	0	1	1	1	0	1	1D
97.4	97.435	-0.036	1	1	1	0	1	0	3A
100.0	99.96	-0.040	0	0	1	1	0	1	0D
103.5	103.429	-0.069	0	1	1	1	0	0	1C
107.2	107.147	-0.05	0	0	1	1	0	0	0C
110.9	110.954	0.049	0	1	1	0	1	1	1B
114.8	114.84	0.035	0	0	1	0	1	1	0B
118.8	118.793	-0.006	0	1	1	0	1	0	1A
123.0	123.028	0.023	0	0	1	0	1	0	0A
127.3	127.328	0.022	0	1	1	0	0	1	19
131.8	131.674	-0.095	0	0	1	0	0	1	09
136.5	136.612	0.082	0	1	1	0	0	0	18
141.3	141.323	0.016	0	0	1	0	0	0	08
146.2	146.044	-0.107	0	1	0	1	1	1	17
151.4	151.441	0.027	0	0	0	1	1	1	07
156.7	156.875	0.112	0	1	0	1	1	0	16
• 159.8	159.936	0.085	1	1	0	0	0	1	31
162.2	162.311	0.069	0	0	0	1	1	0	06
167.9	167.708	-0.114	0	1	0	1	0	1	15
173.8	173.936	0.078	0	0	0	1	0	1	05
179.9	179.654	-0.137	0	1	0	1	0	0	14
• 183.5	183.680	0.098	1	1	0	0	1	0	32
186.2	186.289	0.048	0	0	0	1	0	0	04
• 189.9	190.069	0.089	1	1	0	0	1	1	33
192.8	192.864	0.033	0	1	0	0	1	1	13
• 196.6	196.329	-0.138	1	1	0	1	0	0	34
• 199.5	199.312	-0.094	1	1	0	1	0	1	35
203.5	203.645	0.071	0	0	0	0	1	1	03
• 206.5	206.207	-0.142	1	1	0	1	1	0	36
210.7	210.848	0.070	0	1	0	0	1	0	12
218.1	217.853	-0.113	0	0	0	0	1	0	02
225.7	225.339	-0.160	0	1	0	0	0	1	11
• 229.1	229.279	0.078	1	1	0	1	1	1	37
233.6	233.359	-0.103	0	0	0	0	0	1	01
241.8	241.970	0.070	0	1	0	0	0	0	10
250.3	250.282	-0.007	0	0	0	0	0	0	00
• 254.1	254.162	0.024	1	1	1	0	0	0	38
Notone		N/A	1	1	0	0	0	0	30
Serial Input Mode		N/A	1	0	Data	Clock	X	X	2X

Table 2 - CTCSS Tones

•Not specified in the TIA/EIA-603 tone set, and does not meet the TIA/EIA-603 specification when used with their adjacent tones.

CTCSS Decode Performance

F_N (Hz)	Band Separation- (Hz)	F_A -1.23% (Hz)	F_A (Hz)	F_A +1.23% (Hz)	Band Separation+ (Hz)
67.000	NA	66.157	66.980	67.804	1.150
69.300	1.130	68.465	69.317	70.169	1.371
71.900	1.371	71.017	71.901	72.785	1.243
74.400	1.256	73.516	74.431	75.346	1.269
77.000	1.246	76.018	76.965	77.911	1.391
79.700	1.312	78.697	79.677	80.656	1.431
82.500	1.370	81.469	82.483	83.497	1.476
85.400	1.420	84.333	85.383	86.432	1.526
88.400	1.461	87.288	88.374	89.461	1.582
91.500	1.489	90.331	91.456	92.580	1.746
94.800	1.637	93.595	94.760	95.925	0.988
97.400	0.963	96.237	97.435	98.633	0.867
100.000	0.844	98.731	99.960	101.189	1.793
103.500	1.657	102.157	103.429	104.700	1.964
107.200	1.812	105.829	107.147	108.464	1.881
110.900	1.854	109.590	110.954	112.318	1.908
114.800	1.974	113.428	114.840	116.252	1.954
118.800	1.958	117.332	118.793	120.254	2.131
123.000	2.121	121.515	123.028	124.540	2.123
127.300	2.147	125.762	127.328	128.893	2.248
131.800	2.119	130.055	131.674	133.293	2.524
136.500	2.473	134.932	136.612	138.292	2.302
141.300	2.403	139.585	141.323	143.060	2.409
146.200	2.242	144.248	146.044	147.840	2.803
151.400	2.648	149.579	151.441	153.303	2.614
156.700	2.789	154.946	156.875	158.804	0.197
159.800	0.486	157.970	159.936	161.902	-0.513
162.200	-0.283	160.316	162.311	164.307	2.754
167.900	2.635	165.646	167.708	169.770	3.161
173.800	3.058	171.797	173.936	176.074	2.926
179.900	2.776	177.445	179.654	181.863	0.719
183.500	0.622	181.422	183.680	185.938	-0.669
186.200	-0.419	183.999	186.289	188.580	0.371
189.900	0.601	187.732	190.069	192.406	-0.570
192.800	-0.357	190.493	192.864	195.235	0.382
196.600	0.151	193.915	196.329	198.743	-0.240
199.500	-0.721	196.862	199.312	201.763	0.720
203.500	0.644	201.141	203.645	206.149	-0.682
206.500	-0.846	203.671	206.207	208.742	0.904
210.700	0.723	208.256	210.848	213.441	3.569
218.100	3.421	215.175	217.853	220.532	4.040
225.700	3.378	222.569	225.339	228.110	-0.155
229.100	-0.369	226.460	229.279	232.098	0.334
233.600	0.244	230.489	233.359	236.228	4.363
241.800	4.227	238.995	241.970	244.945	4.104
250.300	4.195	247.204	250.282	253.359	-0.529
254.100	-0.515	251.037	254.162	257.287	NA

Band Separation- = $DB_L[i] - 1.005*F_N[i-1]$
Band Separation+ = $0.995*F_N[i+1] - DB_H[i]$

Table 3 - CTCSS Decode Performance for the MX165C

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 V to V_{DD} + 0.3 V
Sink/Source Current	
(supply pins)	±30mA
(other pins)	±20mA
Total Device Dissipation	800mW max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V
V_{SS} = 0V
T_{AMB}=25°C
Xtal/Clock f_0 = 1.0 MHz
0dB ref. = 300mVrms @ 1kHz

Composite signal: 300 mVrms 1kHz test tone, 75 mVrms noise (band limited 6kHz gaussian white noise), 30 mVrms CTCSS tone.

2

Characteristics	See Note	Min.	Typ.	Max.	TIA/EIA -603	Unit
STATIC VALUES						
Supply Voltage		2.75	3.75/5.0	5.5	-	V
Supply Current						
TX		-	3.0	-	-	mA
RX		-	3.0	-	-	mA
RX Monitor		-	2.0	-	-	mA
Tone Input Impedance		-	1	-	-	MΩ
Tone Output Impedance		-	1	-	-	kΩ
RX and TX Audio Input Impedance		-	1	-	-	MΩ
RX and TX Audio Output Impedance		-	1	-	-	kΩ
Digital Input Impedance	1	-	1	-	-	MΩ
Input logic"1"	1	70%V_{DD}	-	-	-	V
Input logic "0"	1	-	-	30%V_{DD}	-	V
Logic "1" output 1' source = 0.1mA	2	80%V_{DD}	-	-	-	V
Logic "0" output 1' sink - 0.1mA	2	-	-	20%V_{DD}	-	V
DYNAMIC VALUES						
Decoder						
Decode Input Signal Level	3	30	-	436	-	mVrms
Decode Response Time	3,6,7,10	-	-	250	250	ms
Deresponse Time	3,6,7,10	-	180	250	250	ms
Decode Selectivity						
Upper Decode Band Edge	3,11	1.005 F_i	-	.995 F_{i-1}	±0.5%f_i	Hz
Lower Decode Band Edge	3,11	1.005 F_{i-1}	-	.995 F_i	±0.5%f_i	Hz
Encoder						
Tone Output Level (relative to 775 mVrms)		548	775	-	-	mVrms
Tone Frequency Accuracy (f error)		-0.3	-	+0.3	-	%f_0
Risetime to 90% nominal O/P:						
f_0>100Hz	4,10	-	15	75	150	ms
f_0<100Hz	4,10	-	45	120	150	ms
Total Harmonic Distortion		-	2	5	-	%
Output Level Variation Between Tones	11	-1.0	-	+1.0	-	dB

Characteristics	See Note	Min.	Typ.	Max.	TIA/EIA -603	Unit
Audio Filter						
Total Harmonic Distortion	5,10	-	2	5	-	%
Output Noise Level	8	-	2	-	-	mVrms
(input a.c. short circuit, audio switch enabled)						
Sinad	9	36	40	-	-	dB
Spurious Emissions		-	-	-48	-	dB
Cutoff Frequency		-	300	-	-	Hz
Passband		300	-	3000	-	Hz
Bandpass Ripple	5	-1	-	+1	-	dB
Stopband Attenuation <250Hz	5	33	36	-	-	dB
Passband Gain 1kHz		-	0	-	-	dB
Audio Switch						
Isolation	9	-	60	-	-	dB
Serial/Parallel Inputs (See Figures 3 &4)						
Parallel Set-up Time t_{SP}		400	-	-	-	ns
Load/Latch Pulse Width t_l		400	-	-	-	ns
Serial Clock Pulse Width t_c		400	-	-	-	ns
Serial Set-up Time t_{SS}		400	-	-	-	ns
Serial Clock Frequency		-	1	-	-	MHz

NOTES:

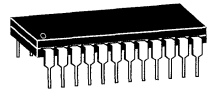
1. Refers to RX/TX, PTL, Decode Comparator Input, D0-D5.
2. All logic outputs.
3. Composite Signal Test Condition.
4. Any programming tone and RL = 10kΩ, CL = 15pF. This includes response to a phase reversal instruction.
5. 1kHz references = 0dB.
6. f_0>100Hz (for 100 Hz>f_0>67Hz: t=100/f_0Hz x 250ms)
7. See Figure 3.
8. Measured in a 30kHz bandwidth referenced to 300 mV.
9. Measured with an input level of 300 mV @ 1kHz, in a 30 kHz bandwidth.
10. Per TIA/EIA-603.
11. Only for the F_i in TIA/EIA-603, where F_i is the program tone.

CTCSS ENCODER/DECODER
WITH TX/RX AUDIO FILTERS

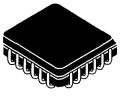
FEATURES
- **39 CTCSS Tones + Notone**
- **TX/RX Audio Filters**
- **TX Tone Phase Reversals**
- **Serial or Parallel Programming**
- **Low Voltage: 4.5 to 5.5 V**

BENEFITS
- **Scanning of any Channel**
- **Improved Sinad**
- **Squelch Tail Elimination**
- **Easy µP Interface**

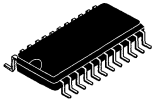
APPLICATIONS
- **Mobile Radio Channel Sharing**
- **Wireless Intercom**
- **TIA/EIA-603 - 37 Tone Plus 97.4Hz & 69.3Hz**



MX365AJ (CDIP)
MX365AP (PDIP)
24 pins



MX365ALH
24 pin PLCC



MX365ADW
24 pin SOIC

Description

Voice on shared radio channels is multiplexed with a subaudible CTCSS tone as a means of directing messages among user groups sharing the same RF frequency. Continuous Tone Controlled Squelch System (CTCSS) modulates the transmitter with a discrete tone, taken from a field of 39 in the range of 67 to 250 Hz, according to TIA/EIA-603 Standard plus 69.3Hz and 97.4Hz. Groups of radio receivers, segregated by common interest and assigned tone, demodulate the voice/tone mixture for voice messages to be heard.

The MX365A CTCSS Encoder/Decoder enhances voice/tone multiplexing with an on-chip filter that attenuates TX speech 36dB at 250Hz, while passing signals >300Hz with only ±1dB of ripple.

Early CTCSS designs did not filter TX speech, depending instead on the host transmitter's pre-emphasis network. At only 6dB/octave, their attenuation of speech components at the higher CTCSS tones was only a few dB, which resulted in "talk-off" (low frequency voice components unsquelching the receiver audio).

The MX365A features TX/RX selection and a LOAD/$\overline{\text{LATCH}}$ pin. A Notone program code has been included to permit scanning channels without CTCSS. A choice of serial or parallel tone programming is offered. Operation of the PTL signal during TX reverses the phase of the transmitted CTCSS tone by 180°. This is used in some radios to eliminate squelch tails.

The MX365A requires a single 5-volt supply and a 1MHz clock or crystal.

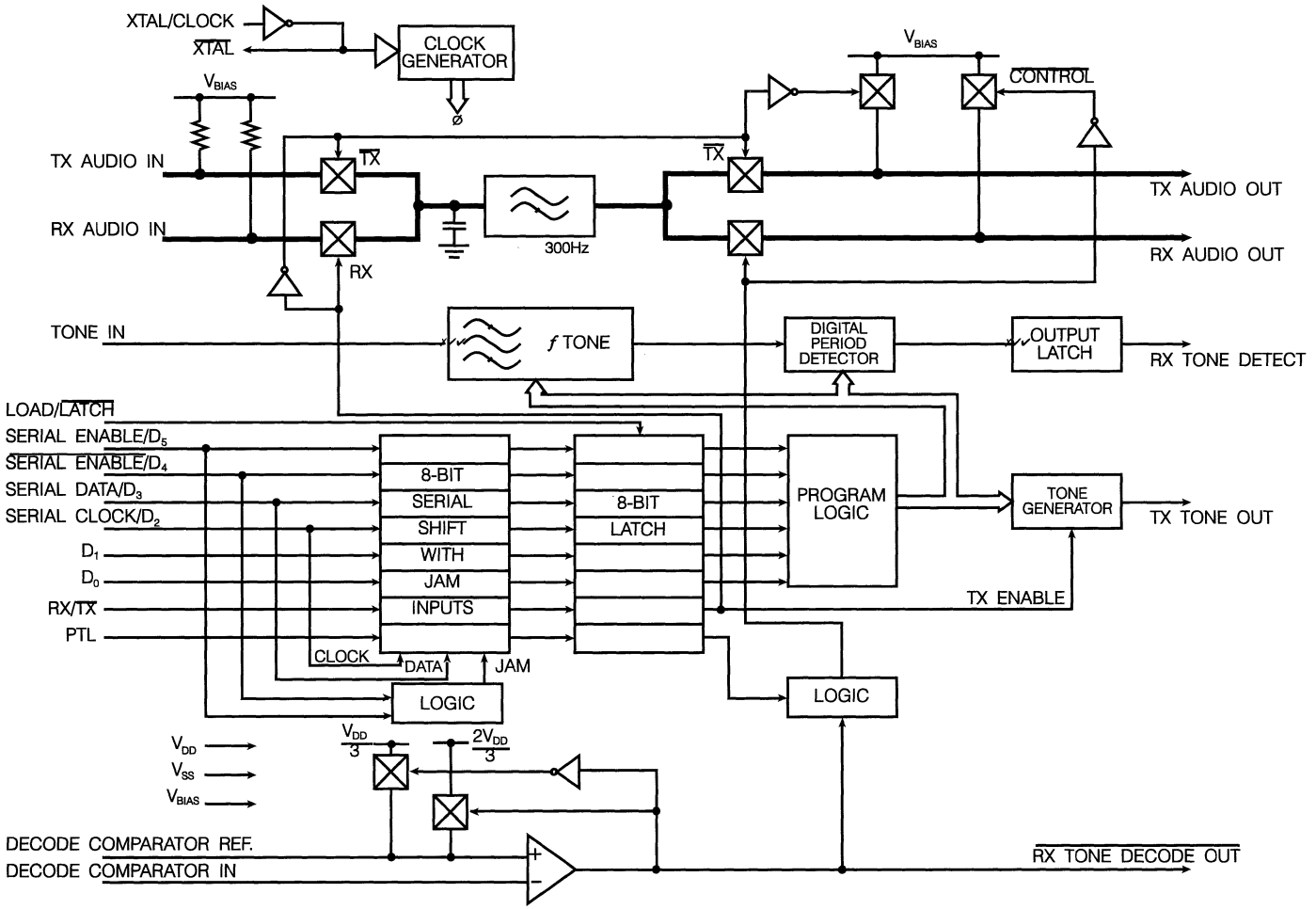


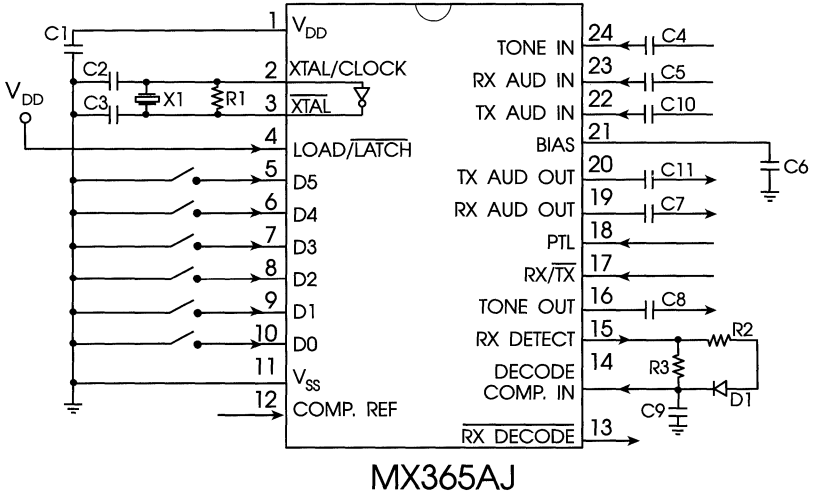
Figure 1 - MX365A Internal Block Diagram

PIN FUNCTION TABLE

Pin	Function
MX165A MX365A	
1	**V_{DD}:** Positive Supply.
2	**Xtal/Clock:** Input to the on-chip inverter used with a 1 MHz Xtal or external clock source.
3	**$\overline{\text{Xtal}}$:** Output of the on-chip inverter (clock output).
4	**Load/$\overline{\text{Latch}}$:** Controls 8 on-chip latches and is used to latch RX/TX, PTL, and D0-D5. This pin is internally pulled to V_{DD}. A logic "1" applied to this input puts the 8 latches in "transparent" mode. A logic "0" applied to this input puts the 8 latches in the "latched" mode. In parallel mode data is loaded and latched by a logic 1-0 transition (see Fig. 3). In serial mode data is loaded and latched by a 0-1-0 strobe pulse on this pin (see Fig. 4).
5	**D5/Serial Enable 1:** Data input D5 (in parallel mode). A logic "1" applied to this input together with a logic "0" applied to D4/Serial Enable 2 will put the device in serial mode (see Fig. 4). This pin is internally pulled to V_{DD}.
6	**D4/$\overline{\text{Serial Enable 2}}$:** Data input D4 (in parallel mode). A logic "0" applied to this input together with a logic "1" on pin 5 will place the device in serial mode (see Fig. 5). This pin is internally pulled to V_{DD}.
7	**D3/Serial Data Input:** Data input D3 (in parallel mode). In serial mode this pin becomes the serial data input for D5-D0, RX/TX and PTL (see Fig. 4). D5 is clocked first and PTL last. This pin is internally pulled to V_{DD}.
8	**D2/Serial Clock:** Data input D2 (in parallel mode). In serial mode this pin becomes the serial clock input. Data is clocked on the positive going edge (see Fig. 4). This pin is internally pulled to V_{DD}.
9	**D1:** Data input D1 (in parallel mode). This pin is internally pulled to V_{DD}.
10	**D0:** Data input D0 (in parallel mode). This pin is internally pulled to V_{DD}.
11	**V_{SS}:** Negative supply.
12	**Decode Comparator Ref.:** This pin is internally biased to $V_{DD}/3$ or $2V_{DD}/3$ via 1M resistors depending on the logical state of the RX Tone Decode Out pin. RX Tone Decode Out = 1 will bias this input $2V_{DD}/3$; a logic "0" will bias this input $V_{DD}/3$. This input provides the decode comparator reference voltage, and switching of bias voltages provides hysteresis to reduce "chatter" under marginal conditions.
13	**$\overline{\text{RX Tone Decode Out}}$:** This is the gated output of the decode comparator. This output is used to gate the RX Audio path. A logic "0" on this pin indicates a successful decode and that the Decode Comparator Input pin is more positive than the Decode Comparator Ref. input (see Table 1).
14	**Decode Comparator Input:** This is the inverting input of the decode comparator. This pin is normally connected to the integrated output of the RX Tone Detect line.
15	**RX Tone Detect:** In RX mode this output will go to logic "1" during a successful decode. It must be externally integrated to control response and deresponse times (see Table 1).
16	**TX Tone Out:** The CTCSS sinewave output appears on this pin under control of the RX/$\overline{\text{TX}}$ pin. This pin, when not transmitting a tone, may be biased to V_{DD}-0.7V or O/C (see Table 1). This pin is an emitter follower output with high impedance load, requiring capacitive coupling or a low impedance (<1kΩ) load to ground.

PIN FUNCTION TABLE

Pin	Function
17	**RX/$\overline{TX}$:** This input (in parallel mode) selects RX or TX modes (see Fig. 2). In serial mode this function is serially loaded. This pin is internally pulled to V_{DD} via a 1MΩ resistor.
18	**PTL:** In parallel RX mode this pin operates as a "Push To Listen" function by enabling the RX audio path, thus overriding the tone squelch function. In parallel TX mode this pin reverses the phase of the transmitted CTCSS tone (used for squelch tail elimination). In serial mode this function is serially loaded (see Fig. 2).
19	**RX Audio Out:** This is the high pass filtered receive audio output pin. This pin outputs audio when RX Tone Decode = 0, or PTL = 1, or when Notone is programmed (see Table 2). In TX mode this pin is biased to $V_{DD}/2$.
20	**TX Audio Out:** This is the high pass filtered transmit audio output pin. In TX mode this pin outputs audio present at the TX Audio Input pin. In RX mode this pin is biased to $V_{DD}/2$.
21	**Bias:** This pin is the output of an internally generated $V_{DD}/2$ bias level and would normally be externally decoupled to V_{SS} via capacitor C7.
22	**TX Audio In:** This is the TX Audio input pin. In TX mode it may be prefiltered, using the TX audio path, thus helping to aviod talkoff due to intermodulation of speech frequencies with the transmitted CTCSS tone. This pin is internally biased to $V_{DD}/2$.
23	**RX Audio In:** This is the input to the audio high pass filter in RX mode. It is internally biased to $V_{DD}/2$.
24	**Tone Input:** This is the input to the CTCSS tone detector. It is internally biased to $V_{DD}/2$.
	NOTE: Pins labeled "N/C" (no connect) may have internal connections. Do Not Use.



Component Values

R1	1MΩ
R2	560kΩ
R3	820kΩ
X1	1MHz
C1	0.1µF
C2	68pF
C3	33pF
C4	0.1µF
C5	0.1µF
C6	0.47µF
C7	0.1µF
C8	0.1µF
C9	0.1µF
C10	0.1µF
C11	0.1µF
D1	small signal

Tolerances: Resistors: ±10%
Capacitors: ±20%
Xtal: ±0.1%

Figure 2 - External Component Diagram

I/O CONDITIONS

	INPUT PIN CONDITION			OUTPUT PIN CONDITION		RESULT/FUNCTION					
D0-D5	RX/$\overline{TX}$	PTL	Decode Comp. Input	RX Tone Detect	$\overline{\text{Tone}}$ Decode	Tone Transmitter Enabled	TX Tone Phase Reversed	TX Audio Path Enabled	Tone Decoder Enabled	RX Audio Path Enabled	Notes
Tone	0	0	X	0	1	Yes	No	Yes	No	No (bias)	1a
Tone	0	1	X	0	1	Yes	Yes	Yes	No	No (bias)	1b
No tone	0	X	X	0	1	No (bias)	X	Yes	No	No (bias)	2
Tone	1	0	0	0	1	No (o/c)	X	No	Yes	No (bias)	3a
Tone	1	1	0	0	1	No (o/c)	X	No	Yes	Yes	3b
Tone	1	X	1	1	0	No (o/c)	X	No	Yes	Yes	4
No tone	1	X	X	X	0	No (o/c)	X	No	Yes	Yes	5

Table 1 - Combinations of Input/Output Conditions

o/c = open circuit
X = don't care

Notes:

1a. Normal tone transmit condition.
1b. Tone transmit with phase reversed.
2 Notone programmed in TX mode, tone transmit O/P set to $V_{DD}/2$ - 0.7V. TX audio path enabled.
3a. Normal decode standby.
3b. Normal decode standby with PTL used to enable audio.
4. Normal decode of correct CTCSS tone condition, PTL has no effect.
5. Notone programmed in RX mode, tone transmit O/P (o/c). RX audio path enabled.

FILTER RESPONSE

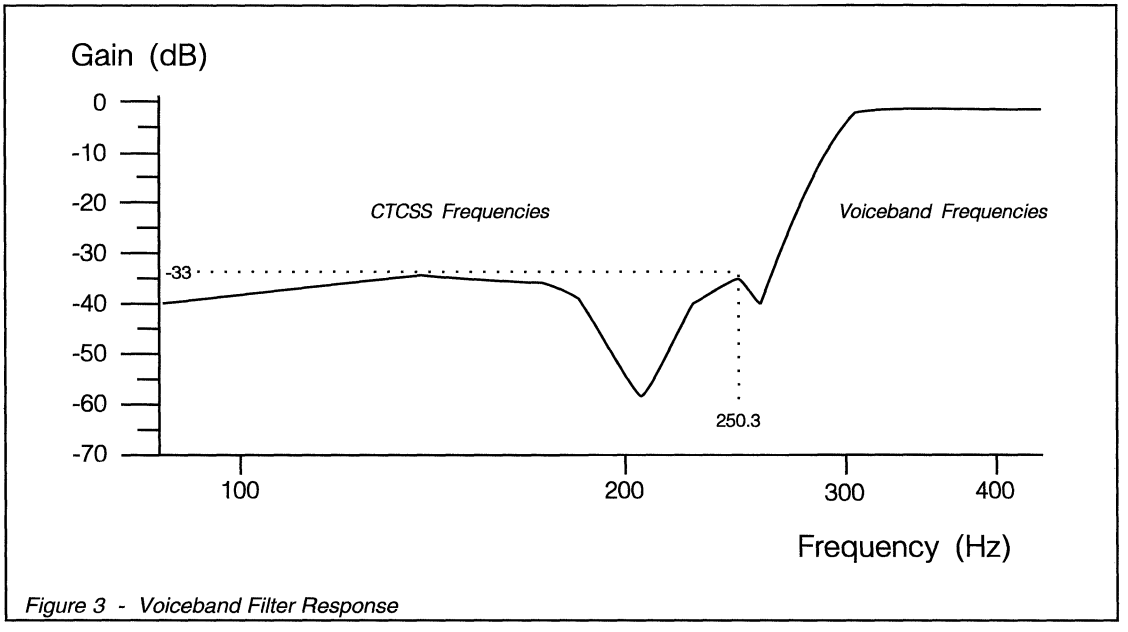
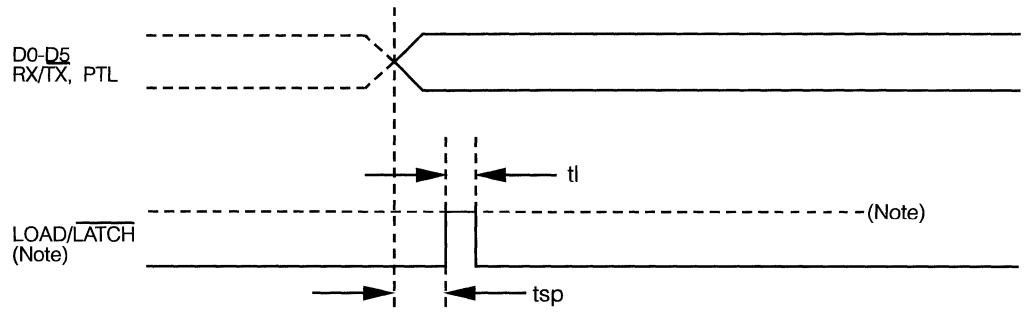


Figure 3 - Voiceband Filter Response

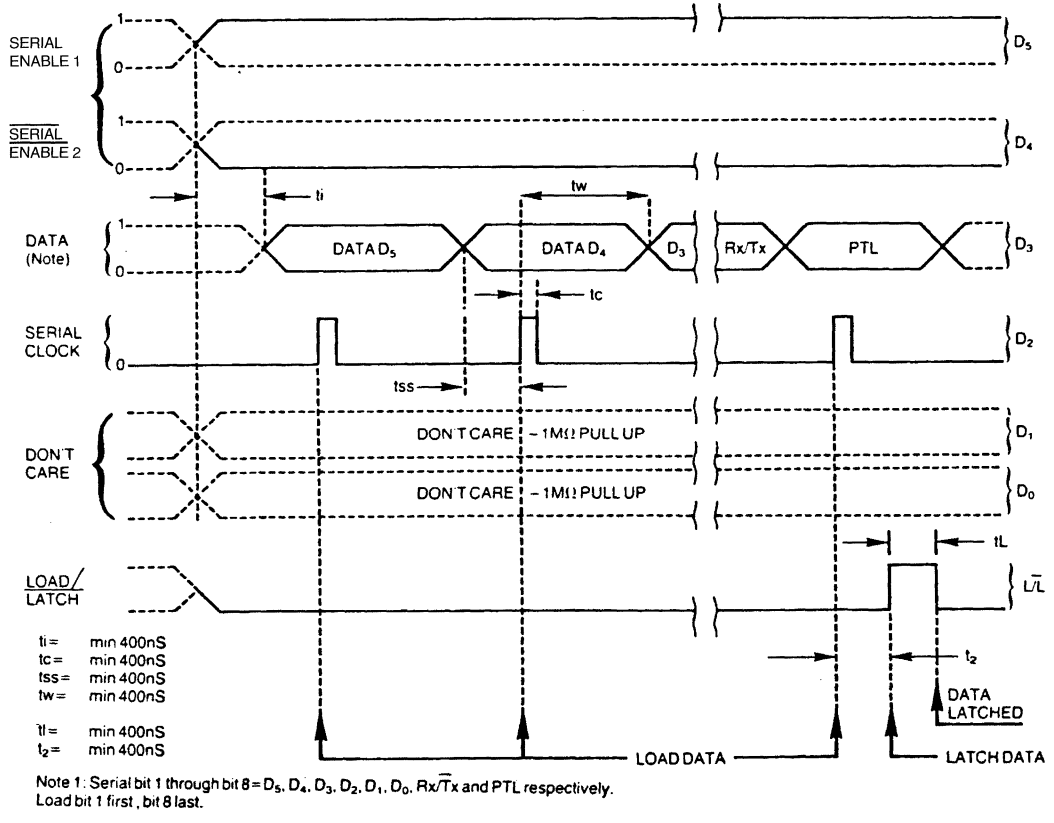
SERIAL AND PARALLEL MODE TIMING



Note: For wired, non microprocessor applications Load/Latch should be connected to V_{DD}.

tl min. = 400ns
tsp min. = 400ns

Figure 4 - Parallel Mode (not to scale)



Note 1: Serial bit 1 through bit 8 = D_5, D_4, D_3, D_2, D_1, D_0, Rx/$\overline{Tx}$ and PTL respectively.
Load bit 1 first, bit 8 last.

Figure 5 - Serial Mode (not to scale)

CTCSS PROGRAMMING TABLE

Tone			Programming Inputs						
Nominal Frequency (Hz)	MX365A Freq. (Hz)	△fo (%)	D5	D4	D3	D2	D1	D0	Hex
67.0	67.05	+0.07	1	1	1	1	1	1	3F
69.3	69.32	+.03	1	1	1	0	0	1	39
71.9	71.9	0	0	1	1	1	1	1	1F
74.4	74.35	-0.07	1	1	1	1	1	0	3E
77.0	76.96	-0.05	0	0	1	1	1	1	0F
79.7	79.77	+0.09	1	1	1	1	0	1	3D
82.5	82.59	+0.1	0	1	1	1	1	0	1E
85.4	85.38	-0.2	1	1	1	1	0	0	3C
88.5	88.61	+0.13	0	0	1	1	1	0	0E
91.5	91.58	+0.09	1	1	1	0	1	1	3B
94.8	94.76	-0.04	0	1	1	1	0	1	1D
97.4	97.29	-0.11	1	1	1	0	1	0	3A
100.0	99.96	-0.04	0	0	1	1	0	1	0D
103.5	103.43	-0.07	0	1	1	1	0	0	1C
107.2	107.15	-0.05	0	0	1	1	0	0	0C
110.9	110.77	-0.12	0	1	1	0	1	1	1B
114.8	114.64	-0.14	0	0	1	0	1	1	0B
118.8	118.8	0	0	1	1	0	1	0	1A
123.0	122.8	-0.17	0	0	1	0	1	0	0A
127.3	127.08	-0.17	0	1	1	0	0	1	19
131.8	131.67	-0.10	0	0	1	0	0	1	09
136.5	136.61	+0.08	0	1	1	0	0	0	18
141.3	141.32	+0.02	0	0	1	0	0	0	08
146.2	146.37	+0.12	0	1	0	1	1	1	17
151.4	151.09	-0.2	0	0	0	1	1	1	07
156.7	156.88	+0.11	0	1	0	1	1	0	16
162.2	162.31	+0.07	0	0	0	1	1	0	06
167.9	168.14	+0.14	0	1	0	1	0	1	15
173.8	173.48	-0.19	0	0	0	1	0	1	05
179.9	180.15	+0.14	0	1	0	1	0	0	14
186.2	186.29	+0.05	0	0	0	1	0	0	04
192.8	192.86	+0.03	0	1	0	0	1	1	13
203.5	203.65	+0.07	0	0	0	0	1	1	03
210.7	210.17	-0.25	0	1	0	0	1	0	12
218.1	218.58	+0.22	0	0	0	0	1	0	02
225.7	226.12	+0.18	0	1	0	0	0	1	11
233.6	234.19	+0.25	0	0	0	0	0	1	01
241.8	241.08	-0.30	0	1	0	0	0	0	10
250.3	250.28	-0.01	0	0	0	0	0	0	00
Notone		N/A	1	1	0	0	0	0	30
Serial Input Mode		N/A	1	0	Data	Clock	X	X	2X
Test	4082	N/A	1	1	0	0	1	1	33 or any invalid address

Table 2 - CTCSS Tones

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 V to V_{DD} + 0.3 V
Sink/Source Current (Total)	20mA
Maximum Device Dissipation	100mW
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.

MX365A V_{DD} = 5.0V
T_{AMB} = 25°C
MX365A 0dB ref. = 308mVrms @ 1kHz

Composite signal: 0dB 1kHz test tone, 75 mVrms noise (band limited 6kHz gaussian white noise), 30 mVrms CTCSS tone.

2

Characteristics	See Note	Min.	Typ.	Max.	Unit
STATIC VALUES					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
TX		-	3.5	-	mA
RX		-	3.5	-	mA
RX Monitor		-	2.5	-	mA
Tone Input Impedance		-	1	-	MΩ
Audio Input Impedance		-	1	-	MΩ
Audio Output Impedance		-	1	-	kΩ
Digital Input Impedance	1	-	1	-	MΩ
Input logic"1"	1	70%V_{DD}	-	-	V
Input logic "0"	1	-	-	30%V_{DD}	V
Logic "1" output 1' source = 0.1mA	2	80%V_{DD}	-	-	V
Logic "0" output 1' sink - 0.1mA	2	-	-	20%V_{DD}	V
DYNAMIC VALUES					
Decoder					
Decode Input Signal Level	3	-20	-	+3	dB
Decode Response Time	3,6,10	-	-	250	ms
Deresponse Time	3,6,10	-	180	250	ms
Decode Selectivity (see Fig. 6)	3,12	±0.5	-	±3	%f_0
Encoder					
Tone Output Level (relative to 775mVrms)		-3	0	-	dB
Tone Frequency Accuracy (f error)		-0.3	-	+0.3	%f_0
Risetime to 90% nominal O/P:					
f_0>100Hz	4,10	-	15	75	ms
f_0<100Hz	4,10	-	45	120	ms
Tone Output Load Current		-	-	5	mA
Total Harmonic Distortion		-	2	5	%
Output Level Variation Between Tones	11	-1.0	-	+1.0	dB
TX Output Impedance		-	2.0	-	kΩ

Characteristics	See Note	Min.	Typ.	Max.	Unit
Audio Filter					
Total Harmonic Distortion	5,10	-	2	5	%
Output Noise Level	8	-	-54	-48	dB
(input a.c. short circuit, audio switch enabled)					
Sinad	9	36	40	-	dB
Spurious Emissions		-	-	-48	dB
Cutoff Frequency	7	-	300	-	Hz
Bandpass Ripple (300-3000Hz)		-	-	2	dB
Stopband Attenuation <250Hz	5,7	33	36	-	dB
Passband Gain 1kHz		-	0	-	dB
Audio Switch					
Isolation	5	-	60	-	dB
Serial/Parallel Inputs (See Figures 3 &4)					
Parallel Set-up Time t_{SP}		400	-	-	ns
Load/Latch Pulse Width t_l		400	-	-	ns
Serial Clock Pulse Width t_C		400	-	-	ns
Serial Set-up Time t_{SS}		400	-	-	ns
Serial Clock Frequency		-	1	-	MHz

NOTES:

1. Refers to RX/TX, PTL, Decode Comparator Input, D0-D5.
2. All logic outputs.
3. Composite Signal Test Condition.
4. Any programming tone and RL = 10,000, CL = 15pF. This includes response to a phase reversal instruction.
5. 1kHz references = 0dB.
6. f_0>100Hz (for 100 Hz>f_0>67Hz: t = 100/f_0Hz x 250ms)
7. See Figure 3.
8. Measured in a 30kHz bandwidth.
9. The MX365A is measured with an input level of 308mV @ 1kHz, in a 30 kHz bandwidth.
10. Per TIA/EIA-603.
11. Ref. to 100 Hz.
12. Complies with TIA/EIA-603, must not decode adjacent f_0 ±0.5%.

MX•COM, INC. MX275

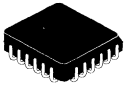
LOW VOLTAGE *Pvt* SQUELCH™ CTCSS ENCODER/DECODER

Features

- MX•COM MiXed SIGNAL CMOS
- PRIVATE/CLEAR CAPABILITY
- ON-CHIP TX AUDIO PRE-/DE-EMPHASIS
- ALTERNATIVE TO CTCSS "PARTY LINE"
- LOW VOLTAGE
- EXCEEDS TIA/EIA-603 LAND MOBILE RADIO STANDARD

SIX SIGMA BASED

2



MX275LH
24-lead PLCC

Applications

- MOBILE RADIOS
- COMMUNITY REPEATERS
- TELEPHONE/RADIO INTERCONNECT SYSTEMS
- SPORT RADIOS
- SERVES 2- and 3-CELL APPLICATIONS

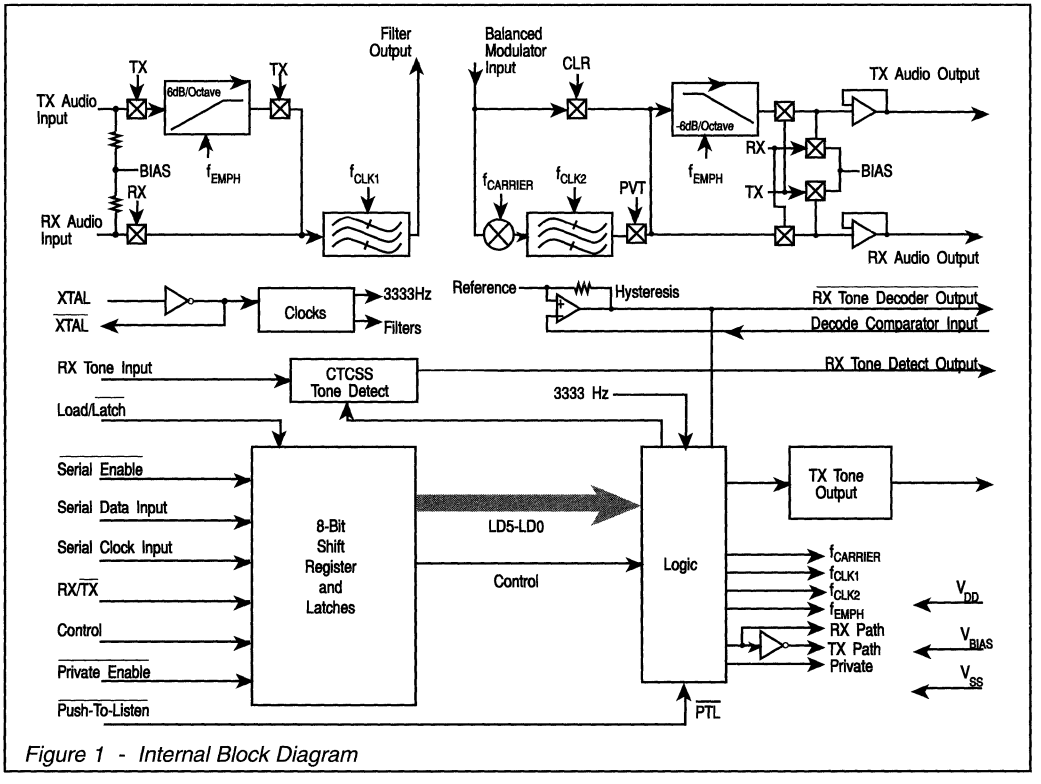


Figure 1 - Internal Block Diagram

Description

The MX275 is a CMOS LSI combination of a CTCSS encoder/decoder and a simple (frequency inversion) speech scrambler. CTCSS (Continuous Tone-Controlled Squelch System) multiplexes a sub-audible tone (1 of 38) with speech. This is performed continuously in 2-Way Radio systems -- as a means of segregating the traffic of co-channel talk groups. The MX275 integrated circuit carries this process an extra step called *Pvt* SQUELCH™. This uses the detection of the CTCSS tone to enable the clear recovery of scrambled speech. As talk groups are assigned unique CTCSS tones, their voice traffic is rendered intelligible only among its own members. The audio monitored by co-channel users with different talk group tones is unintelligible.

The MX275 Features

1) Serial control, but with parallel PTT, PTL and PVT/CLR options.
2) Squelch Tail Elimination facilitated by 180° reverse burst option.
3) On-chip speech filters aid FDM (CTCSS+audio) multiplexing.
4) *Pvt* SQUELCH™ operation.
5) Grants to the 2-Way Radio protection under the ECPA.

Why not Busy Channel Lock Out? (sometimes called Privacy Lock Out)

While BCLO also affords co-channel users privacy, its implementation is at the discretion of the receiver, not the sender. BCLO prevents inadvertant PTT keying and impolite disruptions by co-channel users who fail to monitor before transmitting. But BCLO provides no protection against scanners nor under the ECPA. BCLO assures politeness, *Pvt* SQUELCH™ privacy.

Application Notes

Pre- and de-emphasis (6dB/octave) filters are included on-chip in the transmit path, so that the use of this device will produce natural sounding audio (clear or private modes) when installed in modern radio communication transceivers, with or without existing audio processing circuitry. The recommended layout is shown in block form below.

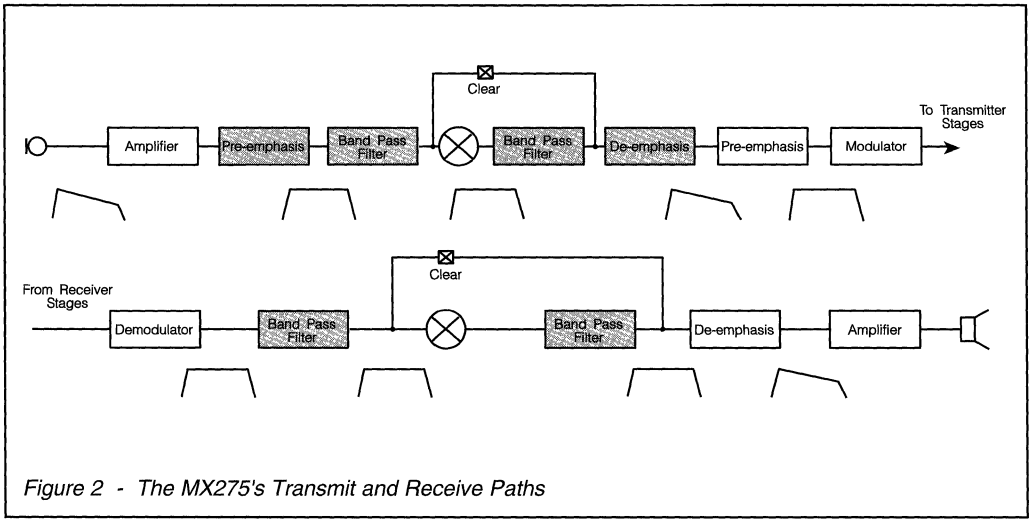


Figure 2 - The MX275's Transmit and Receive Paths

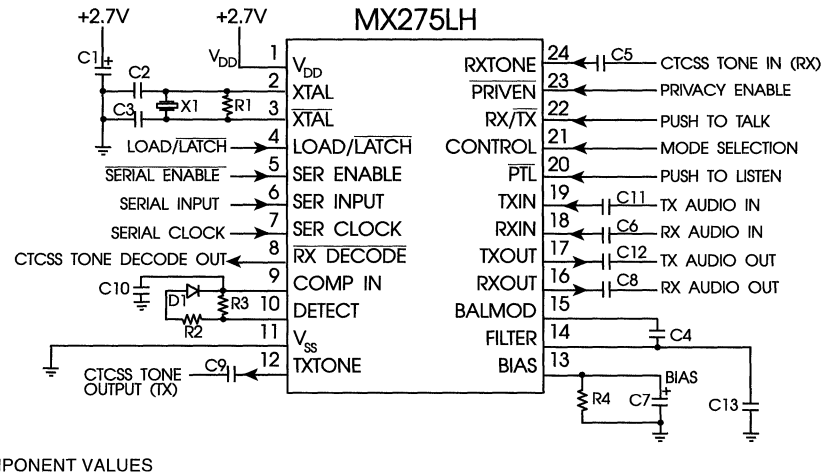
** Electronic Communications Privacy Act of 1986.*

Pin Function Chart

Pin	Function
1	**V_{DD}**: The positive 2.7V supply pin.
2	**XTAL/CLOCK**: This is the input to the clock oscillator inverter. An external 4 MHz xtal or clock input should be applied to this pin.
3	**$\overline{\text{XTAL}}$**: This is the 4 MHz output of the clock oscillator inverter.
4	**LOAD/$\overline{\text{LATCH}}$**: This input controls the eight input latches: RX/$\overline{\text{TX}}$, $\overline{\text{Private Enable}}$, and D0-D5, as detailed in Table 2(a). Alternatively, the RX/$\overline{\text{TX}}$ and $\overline{\text{Private Enable}}$ inputs can be addressed separately by setting the Load/$\overline{\text{Latch}}$ and Control inputs as shown in Table 2(b). 1 MΩ pullup. An external pull-up or active CMOS drive is recommended.
5-7	**Programming Inputs**: These are the RX/$\overline{\text{TX}}$ tone programming and function inputs which enable the serial programming mode. With Load/$\overline{\text{Latch}}$ at logic "0" data is loaded in the following sequence: D5, D4, D3, D2, D1, D0, RX/$\overline{\text{TX}}$, $\overline{\text{Private Enable}}$. When these 8 bits have been clocked in on the rising clock edge, data is latched by strobing the Load/$\overline{\text{Latch}}$ input "0 - 1 - 0" (See Figure 4). Pin 5 = $\overline{\text{Serial Enable}}$ Pin 6 = Serial Data Input Pin 7 = Serial Clock Input
8	**$\overline{\text{RX TONE DECODE}}$**: The gated output of the decode comparator. In RX, a logic "0" indicates a valid CTCSS tone decode condition, or the presence of NOTONE programming. A logic "0" enables the RX audio path. In TX this output is held at logic "1."
9	**DECODE COMPARATOR**: The voltage level at this pin is compared internally with a switched $^1/_3$-$^2/_3$ V_{DD} reference that provides hysteresis. An input level exceeding the reference results in a logic "0" at the RX Tone Decode output. This input should be externally connected to the RX Tone Detect output via external integration components C_{10}, R_2, R_3, and D_1 (see Figure 3).
10	**RX TONE DETECT**: In RX, this pin outputs a logical "1" when a valid programmed CTCSS tone is received at the RX TONE INPUT. This input should be externally connected to the Decode Comparator input via external integration components C_{10}, R_2, R_3, and D_1 (see Figure 3).
11	**V_{SS}**: The negative supply pin (ground).
12	**TX TONE OUTPUT**: The buffered CTCSS sinewave tone output appears on this pin. In TX mode, the tone frequency is selected by program code (see Table 1); if NOTONE is programmed, the output is at V_{BIAS}-0.7V. In RX mode, the output goes open circuit. This is an emitter follower output with an internal 10 kΩ load.
13	**BIAS**: This pin is set internally to approximately $V_{DD}/2$. It must be externally connected to V_{SS} using capacitor C_7 and resistor R_4. See Figure 3.
14	**FILTER OUTPUT**: This is the output of the Input Audio Bandpass Filter. It must be A.C. coupled to the Balanced Modulator Input via capacitor C_4. See Figure 3.
15	**BALANCED MODULATOR INPUT**: This is the input to the balanced modulator. It must be A.C. coupled to the Filter Output via capacitor C_4. See Figure 3.

Pin Function Chart

Pin	Function
16	**RX AUDIO OUTPUT:** Outputs the received audio from a buffered output stage and is held at V_{BIAS} when in TX. Capacitive loads exceeding 15pF should be avoided.
17	**TX AUDIO OUTPUT:** Outputs the transmitted audio in TX. In RX, this pin is held at V_{BIAS}. Capacitive loads exceeding 15pF should be avoided.
18	**RX AUDIO INPUT**: The audio input for the RX mode. Input signals should be AC coupled via external capacitor C_6. See Figure 3.
19	**TX AUDIO INPUT:** This is the TX Audio voice input. Signals should be AC coupled via external capacitor C_{11}. See Figure 3.
20	**$\overline{\text{PTL}}$**: The "press to listen" function input. In RX mode, a logic "0" enables the RX Audio Output directly, overriding tone squelch but not intercepting a private conversation; in TX mode, a logic "0" reverses the phase of the TX Tone Output for "squelch tail" reduction (see Table 2).
21	**CONTROL:** This input, together with Load/$\overline{\text{Latch}}$, selects the operational mode of the RX/$\overline{\text{TX}}$ and $\overline{\text{Private Enable}}$ functions. See Table 2(b).
22	**RX/$\overline{\text{TX}}$**: This input selects the RX or TX mode (RX = 1, TX = 0). See Table 2.
23	**$\overline{\text{PRIVATE ENABLE}}$**: This input selects either Private or Clear mode (Clear = 1, Private = 0), and is loaded as described in Table 2. This input has an internal 1 MΩ pullup resistor.
24	**RX TONE INPUT**: This is the received audio input to the on-chip CTCSS tone decoder. It should be A.C. coupled via capacitor C_5.



COMPONENT VALUES

R1 = 1MΩ	C1 = 1μF	C6 = 0.1μF	C11 = 0.1μF
R2 = 560kΩ	C2 = 33pF	C7 = 1μF	C12 = 0.1μF
R3 = 820kΩ	C3 = 33pF	C8 = 0.1μF	C13 = 0.001μF
R4 = 560kΩ	C4 = 0.1μF	C9 = 0.1μF	D1 = small signal
X1 = 4MHz	C5 = 0.1μF	C10 = 0.1μF	

Tolerances: Resistors: ±5% Capacitors: ±10%

XTAL: At cut, fundamental, parallel resonant 20pF load capacitance, tolerance 100 PPM.

Figure 3 - External Component Connections

CTCSS PROGRAMMING TABLE

TIA/EIA-603 Nominal Frequency(Hz)	Frequency (Hz)	Δf_o (%)	Programming Inputs D5	D4	D3	D2	D1	D0	HEX
67.0	67.05	+0.07	1	1	1	1	1	1	3F
71.9	71.9	0	0	1	1	1	1	1	1F
74.4	74.35	-0.07	1	1	1	1	1	0	3E
77.0	76.96	-0.05	0	0	1	1	1	1	0F
79.7	79.77	+0.09	1	1	1	1	0	1	3D
82.5	82.59	+0.1	0	1	1	1	1	0	1E
85.4	85.38	-0.2	1	1	1	1	0	0	3C
88.5	88.61	+0.13	0	0	1	1	1	0	0E
91.5	91.58	+0.09	1	1	1	0	1	1	3B
94.8	94.76	-0.04	0	1	1	1	0	1	1D
97.4	97.29	-0.11	1	1	1	0	1	0	3A
100.0	99.96	-0.04	0	0	1	1	0	1	0D
103.5	103.43	-0.07	0	1	1	1	0	0	1C
107.2	107.15	-0.05	0	0	1	1	0	0	0C
110.9	110.77	-0.12	0	1	1	0	1	1	1B
114.8	114.64	-0.14	0	0	1	0	1	1	0B
118.8	118.8	0	0	1	1	0	1	0	1A
123.0	122.8	-0.17	0	0	1	0	1	0	0A
127.3	127.08	-0.17	0	1	1	0	0	1	19
131.8	131.67	-0.10	0	0	1	0	0	1	09
136.5	136.61	+0.08	0	1	1	0	0	0	18
141.3	141.32	+0.02	0	0	1	0	0	0	08
146.2	146.37	+0.12	0	1	0	1	1	1	17
151.4	151.09	-0.2	0	0	0	1	1	1	07
156.7	156.88	+0.11	0	1	0	1	1	0	16
162.2	162.31	+0.07	0	0	0	1	1	0	06
167.9	168.14	+0.14	0	1	0	1	0	1	15
173.8	173.48	-0.19	0	0	0	1	0	1	05
179.9	180.15	+0.14	0	1	0	1	0	0	14
186.2	186.29	+0.05	0	0	0	1	0	0	04
192.8	192.86	+0.03	0	1	0	0	1	1	13
203.5	203.65	+0.07	0	0	0	0	1	1	03
210.7	210.17	-0.25	0	1	0	0	1	0	12
218.1	218.58	+0.22	0	0	0	0	1	0	02
225.7	226.12	+0.18	0	1	0	0	0	1	11
233.6	234.19	+0.25	0	0	0	0	0	1	01
241.8	241.08	-0.30	0	1	0	0	0	0	10
250.3	250.28	-0.01	0	0	0	0	0	0	00
Notone			1	1	0	0	0	0	30

Table 1 - CTCSS Programming Chart

(A)Explanation of Load/Latch function

Load Configuration	Load/$\overline{\text{Latch}}$	Result
Data loading	0	No change while serial data train is loaded
Data loaded	0 - 1 - 0	Loaded serial data is latched

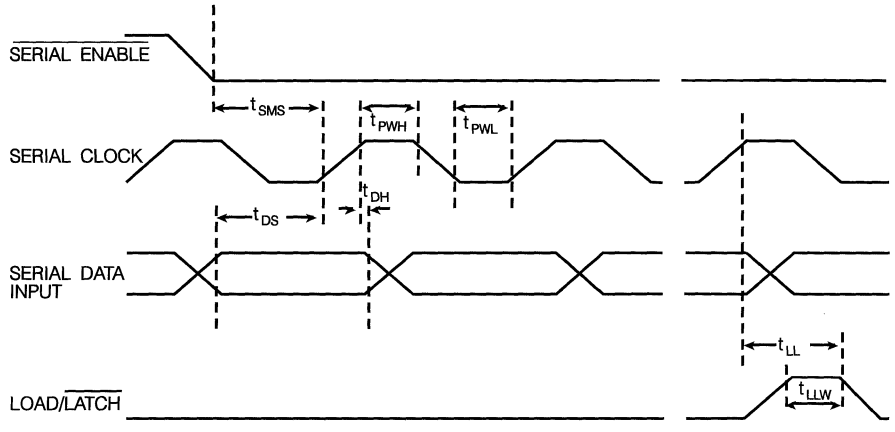
(B) Explanation of Control Input

Load Configuration	Load/$\overline{\text{Latch}}$	Control	RX/$\overline{\text{TX}}$, $\overline{\text{Private Enable}}$
Serial Control Input	0 - 1 - 0	0	Serial Load
Serial Control Input	X	1	Transparent

Notes: "0 - 1 - 0" is a strobe pulse as shown in Figures 4 and 5 (Timing).
"X" denotes any logical state.

Table 2 - Load/$\overline{\text{Latch}}$ and Control Functions

Control instructions are input to the MX275 by serial means, using Data Inputs and Load/Latch as shown below.



	Min.	Typ.	Max.	Unit
Serial Mode Enable Set Up Time (t_{SMS})	250	-	-	ns
Clock "High" Pulse Width (t_{PWH})	250	-	-	ns
Clock "Low" Pulse Width (t_{PWL})	250	-	-	ns
Data Set Up Time (t_{DS})	150	-	-	ns
Data Hold Time (t_{DH})	50	-	-	ns
Load/Latch Set Up Time (t_{LL})	250	-	-	ns
Load/Latch Pulse Width (t_{LLW})	150	-	-	ns

Figure 4 - Serial Load Timing (see notes 1 and 9 in Specification section)

D0-D5	NOTONE	RX/TX	PRIVATE ENABLE	PTL	RXTONE DETECT	RXTONE DECODER	TONE OUTPUT	TONE PHASE	TX PATH	RX PATH	PATH STATE	TONE
TONE	1	0	0	1	0	1	YES	0°	OPEN	BIAS	INV	TX, TONE
TONE	1	0	0	0	0	1	YES	180°	OPEN	BIAS	INV	TX, TONE REV
NOTONE	0	0	0	X	0	1	BIAS	X	OPEN	BIAS	CLR	TX, NOTONE
TONE	1	1	0	1	0	1	BIAS	X	BIAS	BIAS	X	INCOMPATIBLE
TONE	1	1	0	0	0	1	BIAS	X	BIAS	OPEN	CLR	INCOMPATIBLE
TONE	1	1	0	X	1	0	BIAS	X	BIAS	OPEN	INV	COMPATIBLE
NOTONE	0	1	0	X	X	0	BIAS	X	BIAS	OPEN	CLR	RX, NOTONE
TONE	1	0	1	1	0	1	YES	0°	OPEN	BIAS	CLR	TX, TONE
TONE	1	0	1	0	0	1	YES	180°	OPEN	BIAS	CLR	TX, TONE REV
NOTONE	0	0	1	X	0	1	BIAS	X	OPEN	BIAS	CLR	TX, NOTONE
TONE	1	1	1	1	0	1	BIAS	X	BIAS	BIAS	X	INCOMPATIBLE
TONE	1	1	1	0	0	1	BIAS	X	BIAS	OPEN	CLR	INCOMPATIBLE
TONE	1	1	1	X	1	0	BIAS	X	BIAS	OPEN	CLR	COMPATIBLE
NOTONE	0	1	1	X	X	0	BIAS	X	BIAS	OPEN	CLR	RX, NOTONE

ALGEBRAIC FUNCTIONS:
RX PATH ON = RX✳ (PTL + RX TONE DECODER)
CLEAR PATH = NOTONE + PRIVATE ENABLE + (PTL ✳ RX ✳ RX TONE DECODER)
NOTONE (D0-D5) = 000011
CARRIER FREQUENCY = 3333Hz DURING INVERTED PATH(TX or RX)

NOTES: 1. The Pre- and De-emphasis circuits remain in the transmit path in both Clear and Invert modes.
2. Power remains applied to the CTCSS tone decoder at all times.
3. During Clear operation the carrier frequency is turned off to reduce spurious emissions.

Table 4 - Functions and Outputs

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 4.0 V
Input Voltage at any pin	-0.3V to (V_{DD} + 0.3 V)
Sink/Source Current	
(Supply pins)	±30 mA
(Other pins)	±20 mA
Total Device Dissipation	
@ T_{AMB} 25°C	800 mW max.
Derating	10 mW/°C
Operating Temperature	-15°C to +60°C
Storage Temperature	-55°C to +125°C

Operating Limits

Measured using the standard test circuit (Fig. 3) and under the following conditions unless otherwise noted.

V_{DD}	2.7V
T_{AMB}	25°C
Xtal/Clock f_0	4.0 MHz
Audio level 0dB ref	250 mVrms

Composite input signal = 300 mVrms, 1 kHz tone in, 75 mVrms (6 kHz band limited) gaussian noise, and a 30 mVrms CTCSS tone.

2

Characteristics		Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Voltage		2.2	2.7	3.2		V
Supply Current	TX		-	4.0	10.0	mA
	RX		-	3.0	4.6	mA
Impedances	Speech In	1	87	155	223	kΩ
	Speech Out	1,8	500	850	1200	Ω
	Tone In	1	410	540	664	kΩ
	Tone Out	1,2,8	616	1800	2966	Ω
I/O Logic	Input "1"	1,9,10	70%	-	-	V_{DD}
	Input "0"	1	-	-	30%	V_{DD}
	Output "1" (source 0.1mA)	1	80%	-	-	V_{DD}
	Output "0" (sink 0.1mA)	1	-	-	20%	V_{DD}
Serial Clock		1	250	-	-	ns
Dynamic Values						
CTCSS Encode						
Tone Output Level		2	350	400	460	mVrms
Tone Accuracy			-0.3	f_o	0.3	$\%f_o$
Distortion			-	3.5	5	%
T-T Level D			-	13	47	mVrms
Risetime to 90%	≥100Hz	1	-	10	50	ms
180°Phase Reversal	90% ≥100Hz	1	-	10	50	ms
CTCSS Decode						
Signal Threshold		4	30	10	-	mVrms
Must Decode B/E			-0.5	±2	0.5	$\%f_o$

Characteristics		Note	Min.	Typ.	Max.	Unit
CTCSS Decode...						
Response Time	>100 Hz	4,5	-	170	250	ms
Deresponse Time	>100 Hz	4	-	150	250	ms
Don't Decode B/E	Adjacent Tone		0.5	±1	-0.5	%

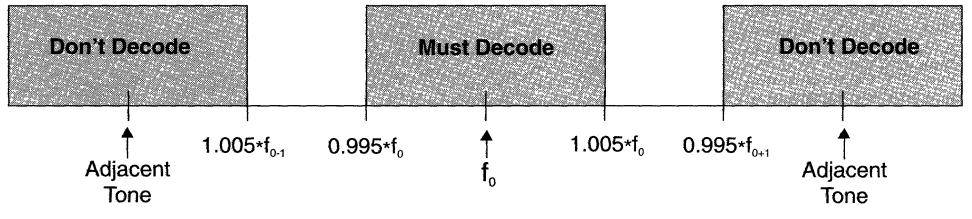


Figure 5 - Do Not Decode Band-edge Adjacent Tone

Speech Filter	**TX/RX**					
Passband		3	300	-	3000	Hz
Passband Gain		3,7	-1.5	0	1	dB
Ripple		3,7	-3	-	1	dB
Distortion	Clear	3	-	6	10	%
CTCSS Rejection	f_{in}<250Hz	3	25	32		dB
AC/SC Noise		6	-	2.5	7.9	mVrms

Scrambling	**TX/RX**					
Inversion Carrier			3329.7	3333	3336.3	Hz
Carrier Breakthrough		1,3	-	-58	-46	dB
Baseband Breakthrough		1,3	-	-54	-42	dB
Carrier Rejection	f_{in}>3333Hz	3	20	-	-	dB
Baseband Reject	f_{in}>3633Hz	3	45	-	-	dB

NOTES

1. Untested parameter — derived by statistical characterization.
2. An emitter follower output.
3. With reference to an input signal of 1 kHz @ 0dB.
4. Composite signal.
5. f_o > 100 Hz, (for 100Hz > f_o > 67Hz: t = [100/f_o(Hz)] x 250ms), per ANSI/TIA/EIA-603.
6. AC Short-Circuit input, speech path enabled.
7. <6dB per octave roll-off, <500 Hz >2500 Hz per ANSI/TIA/EIA-603
8. Capacitive loads not to exceed 15pf.
9. External Pull-Up or active CMOS drive recommended.
10. Includes LOAD/LATCH don't load immunity testing.

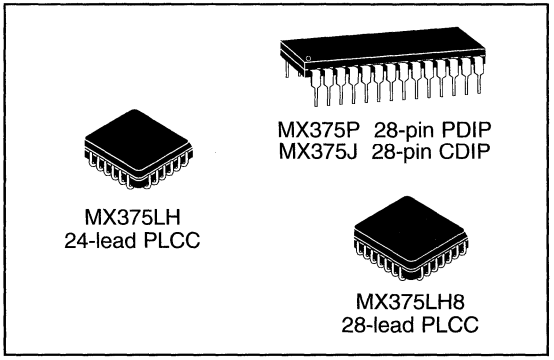
Pvt SQUELCH™ CTCSS ENCODER/DECODER

Features

- PRIVATE/CLEAR CAPABILITY
- ON-CHIP TX AUDIO PRE/DEEMPHASIS
- POWERSAVE OPTION
- ALTERNATIVE TO STANDARD CTCSS "PARTY LINE"

Applications

- MOBILE RADIOS
- COMMUNITY REPEATERS
- TELEPHONE/RADIO INTERCONNECT SYSTEMS



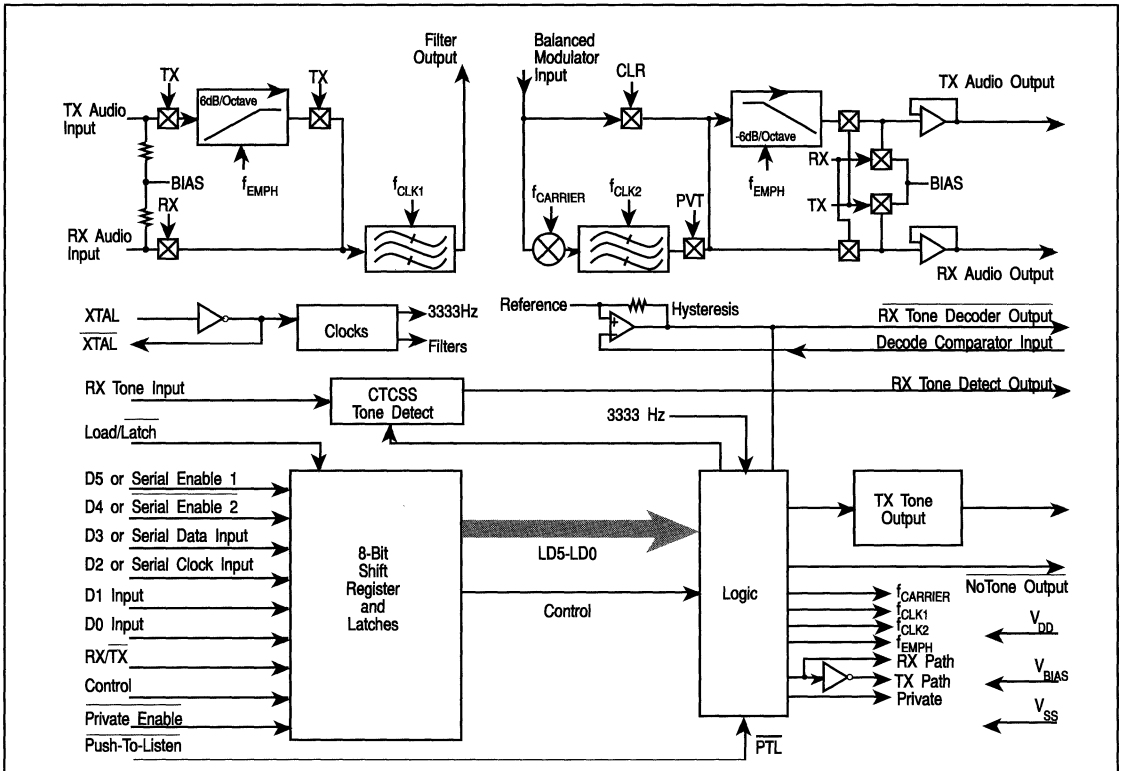


Figure 1 - Internal Block Diagram

DESCRIPTION

The MX375 is a CMOS LSI microcircuit which combines CTCSS Encode/Decode operation with voice band frequency inversion. Frequency inversion is achieved by modulating the input audio with a 3333 Hz carrier frequency. Higher voice band frequencies are translated downward, and lower frequencies upward, resulting in a "mirror image" voice transmission.

Device features:

1) serial or parallel tone programming capability (serial **or** parallel offered on MX375J, P & LH8),
2) the ability to operate under NOTONE conditions,
3) on-chip Tx and Rx audio filtering,
4) pin-selectable Private/Clear operation, and
5) pre/deemphasis filters in the Tx path, for optimal recovered audio quality.

The MX375 is fabricated using CMOS technology. It is offered in 28 pin PDIP, CDIP and PLCC packages. It is also offered in a 24-pin PLCC package. A low-cost 4 MHz crystal/clock and a single 5V supply are required.

What is *Pvt* SQUELCH ?

Pvt SQUELCH™ combines CTCSS with inverted speech to prevent users from understanding each other's communications unless the transmissions are accompanied by the group's assigned tone. Its net effect is to eliminate casual eavesdropping and give mobile radio users a certain degree of privacy at a minimal price. Up to 38 *Pvt* SQUELCH user groups (one per CTCSS tone) can share a single radio channel. With *Pvt* SQUELCH, competing businesses can share a radio channel without compromising communications security.

APPLICATION NOTES

Pre- and De-emphasis (6dB/octave) filters are included on-chip in the transmit path, so that the use of this device will produce natural sounding audio (clear or private modes) when installed in modern radio communication transceivers, with or without existing audio processing circuitry. The recommended layout is shown in block form below.

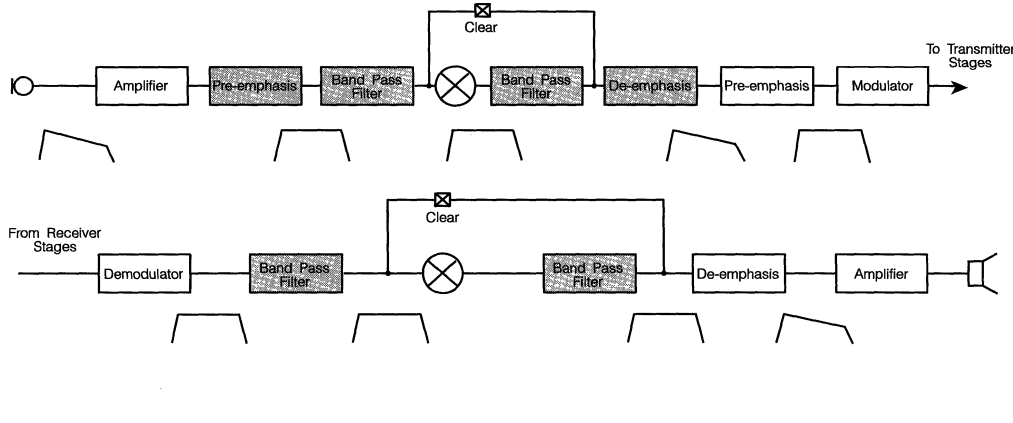


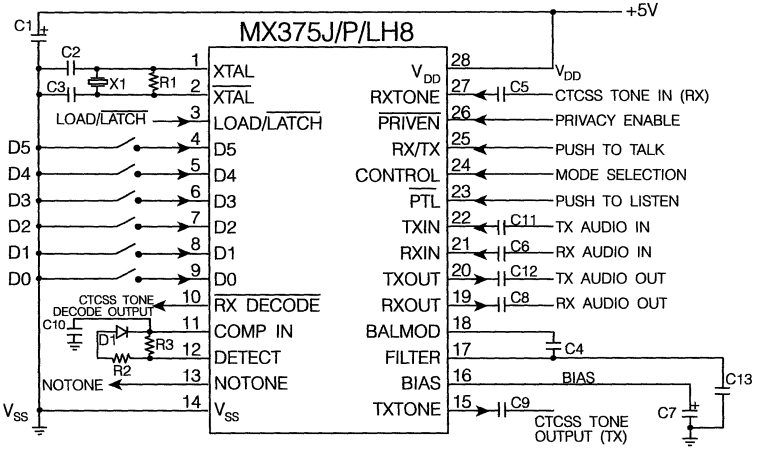
Figure 2 - Transmit and Receive Paths

PIN FUNCTION CHART

Pin		Function
LH	J,P,LH8	*Note: The MX375LH package is available in serial mode only.*
1	28	V_{DD}: The positive 5V supply pin.
2	1	XTAL/CLOCK (I/P): This is the input to the clock oscillator inverter. An external 4 MHz xtal or clock input should be applied to this pin.
3	2	$\overline{\text{XTAL}}$ (O/P): This is the 4 MHz output of the clock oscillator inverter.
4	3	LOAD/$\overline{\text{LATCH}}$ (I/P): This input controls the eight input latches: RX/$\overline{\text{TX}}$, $\overline{\text{Private Enable}}$, and D0-D5, as detailed in Table 2(a). Alternatively, the RX/$\overline{\text{TX}}$ and $\overline{\text{Private Enable}}$ inputs can be addressed separately by setting the Load/$\overline{\text{Latch}}$ and Control inputs as shown in Table 2(b). 1 MΩ pullup.
5-7		D4-D2 (I/P) Programming Inputs (Serial Mode Only): These are the RX/$\overline{\text{TX}}$ tone programming and function inputs which enable the serial programming mode. With Load/$\overline{\text{Latch}}$ at logic "0" serial data is loaded in the following sequence: D5, D4, D3, D2, D1, D0, RX/$\overline{\text{TX}}$, $\overline{\text{Private Enable}}$. When these 8 bits have been clocked in on the rising clock edge, data is latched by strobing the Load/$\overline{\text{Latch}}$ input "0 - 1 - 0" (See Figure 5). Pin 5 (D4) = $\overline{\text{Serial Enable 2}}$ Pin 6 (D3) = Serial Data Input Pin 7 (D2) = Serial Clock Input
	4-9	D5-D0 (I/P) Parallel Programming Inputs: These are the RX/$\overline{\text{TX}}$ tone programming and function inputs which select the CTCSS tone (See Table 1). *For both Serial and Parallel Modes*: In RX, a NOTONE program enables RX Audio Output and forces the RX Tone Decode Output to a logic "0". In TX, a NOTONE program generates a constant V_{bias}-0.7V condition at the TX Tone Output pin. Each input has a 1 MΩ pullup resistor.
8	10	$\overline{\text{RX TONE DECODE}}$ (O/P): The gated output of the decode comparator. In RX, a logic "0" indicates a valid CTCSS tone decode condition, or the presence of NOTONE programming. A logic "0" enables the RX audio path. In TX, this output is held at logic "1".
9	11	DECODE COMPARATOR (I/P): The voltage level at this pin is compared internally with a fixed reference level. A greater input level compared to the reference will result in a logic "0" at the RX Tone Decode output. This input should be externally connected to the RX Tone Detect output via external integration components C_7, R_2, R_3, and D_1 (see Figure 3).
10	12	RX TONE DETECT (O/P): In RX, this pin outputs a logical "1" when a valid programmed CTCSS tone is received at the RX TONE INPUT. This input should be externally connected to the Decode Comparator input via external integration components C_7, R_2, R_3, and D_1 (see Figure 3).
N/A	13	NOTONE (O/P): This pin outputs a logic "0" when a notone CTCSS code has been programmed in RX. It is typically used to enable carrier squelch circuits under notone RX conditions.
11	14	V_{SS}: The negative supply pin (ground).
12	15	TX TONE OUTPUT: The buffered CTCSS sinewave tone output appears on this pin. In TX mode, the tone frequency is selected by program code (see Table 1); if NOTONE is programmed, the output is at V_{bias}-0.7V. In RX mode, the output goes open circuit. This is an emitter follower output with an internal 10 kΩ load.
13	16	BIAS: This pin is set internally to V_{DD}/2. It must be externally decoupled using a capacitor (C_8) to V_{SS}. See Figure 3.
14	17	FILTER OUTPUT: This is the output of the Input Audio Bandpass Filter. It must be A.C. coupled to the Balanced Modulator Input via capacitor C_6. See Figure 3.
15	18	BALANCED MODULATOR INPUT: This is the input to the balanced modulator. Must be A.C. coupled to the Filter Output via capacitor C_6. See Figure 3.

PIN FUNCTION CHART

Pin		Function
LH	J,P,LH8	
16	19	RX AUDIO OUTPUT: Outputs the received audio from a buffered output stage and is held at V_{bias} when in TX.
17	20	TX AUDIO OUTPUT: Outputs the transmitted audio in TX. In RX, this pin is held at V_{bias}.
18	21	RX AUDIO INPUT (I/P): The audio input for the RX mode. Input signals should be AC coupled via external capacitor C4. See Figure 3.
19	22	TX AUDIO INPUT (I/P): This is the TX Audio voice input. Signals should be AC coupled via external capacitor C_3. See Figure 3.
20	23	$\overline{PTL}$ (I/P): The "press to listen" function input. In RX mode, a logic "0" enables the RX Audio Output directly, overriding tone squelch but not intercepting a private conversation; in TX mode, a logic "0" reverses the phase of the TX Tone Output for "squelch tail" reduction (see Table 2).
21	24	CONTROL: This input, together with Load/$\overline{Latch}$, selects the operational mode of the RX/$\overline{TX}$ and $\overline{Private\ Enable}$ functions. See Table 2(b).
22	25	RX/$\overline{TX}$ (I/P): This input selects the RX or TX mode (RX = 1, TX = 0). This can be loaded in Serial or Parallel modes as described in Table 2.
23	26	$\overline{PRIVATE\ ENABLE}$: This input selects either Private or Clear mode (Clear = 1, Private = 0), and can be loaded by Serial or Parallel modes as described in Table 2. This input has an internal 1 MΩ pullup resistor.
24	27	RX TONE INPUT: This is the received audio input to the on-chip CTCSS tone decoder. It should be A.C. coupled via capacitor C_5.



COMPONENT VALUES

R1 = 1MΩ	C1 = 1μF	C5 = 0.1μF	C10 = 0.1μF
R2 = 560kΩ	C2 = 33pF	C6 = 0.1μF	C11 = 0.1μF
R3 = 820kΩ	C3 = 33pF	C7 = 1.0μF	C12 = 0.1μF
X1 = 4MHz	C4 = 0.1μF	C8 = 0.1μF	C13 = 0.001μF
		C9 = 0.1μF	D1 = small signal

Tolerances: Resistors: ±10% Capacitors: ±20%

XTAL: At cut, fundamental, parallel resonant 20pF load capacitance, 0.05% tolerance

Figure 3 - External Component Connections

CTCSS PROGRAMMING TABLE

Nominal Frequency(Hz)	Frequency(Hz)	$\triangle f_o$ (%)	Program Inputs D5	D4	D3	D2	D1	D0
67.0	67.05	+0.07	1	1	1	1	1	1
71.9	71.9	0	0	1	1	1	1	1
74.4	74.35	-0.07	1	1	1	1	1	0
77.0	76.96	-0.5	0	0	1	1	1	1
79.7	79.77	+0.09	1	1	1	1	0	1
82.5	82.59	+0.1	0	1	1	1	1	0
85.4	85.38	-0.2	1	1	1	1	0	0
88.5	88.61	+0.13	0	0	1	1	1	0
91.5	91.58	+0.09	1	1	1	0	1	1
94.8	94.76	-0.04	0	1	1	1	0	1
97.4	97.29	-0.11	1	1	1	0	1	0
100.0	99.96	-0.04	0	0	1	1	0	1
103.5	103.43	-0.07	0	1	1	1	0	0
107.2	107.15	-0.05	0	0	1	1	0	0
110.9	110.77	-0.12	0	1	1	0	1	1
114.8	114.64	-0.14	0	0	1	0	1	1
118.8	118.8	0	0	1	1	0	1	0
123.0	122.8	-0.17	0	0	1	0	1	0
127.3	127.08	-0.17	0	1	1	0	0	1
131.8	131.67	-0.10	0	0	1	0	0	1
136.5	136.61	+0.08	0	1	1	0	0	0
141.3	141.32	+0.02	0	0	1	0	0	0
146.2	146.37	+0.12	0	1	0	1	1	1
151.4	151.09	-0.2	0	0	0	1	1	1
156.7	156.88	+0.11	0	1	0	1	1	0
162.2	162.31	+0.07	0	0	0	1	1	0
167.9	168.14	+0.14	0	1	0	1	0	1
173.8	173.48	-0.19	0	0	0	1	0	1
179.9	180.15	+0.14	0	1	0	1	0	0
186.2	186.29	+0.05	0	0	0	1	0	0
192.8	192.86	+0.03	0	1	0	0	1	1
203.5	203.65	+0.07	0	0	0	0	1	1
210.7	210.17	-0.25	0	1	0	0	1	0
218.1	218.58	+0.22	0	0	0	0	1	0
225.7	226.12	+0.18	0	1	0	0	0	1
233.6	234.19	+0.25	0	0	0	0	0	1
241.8	241.08	-0.30	0	1	0	0	0	0
250.3	250.28	-0.01	0	0	0	0	0	0
Notone			1	1	0	0	0	0

Table 1 - CTCSS Programming Chart

(A)Explanation of Load/Latch function in Serial and Parallel Modes

Load Configuration	Load/Latch	Result
Parallel	1	Transparent, the data acts directly
Parallel	1 - 0	Latches present data in
Parallel	0	No further changes except to allow serial mode selection
Serial (data loading)	0	No change while serial data train is loaded
Serial (data loaded)	0 - 1 - 0	Loaded serial data is latched

(B) Explanation of Control Input

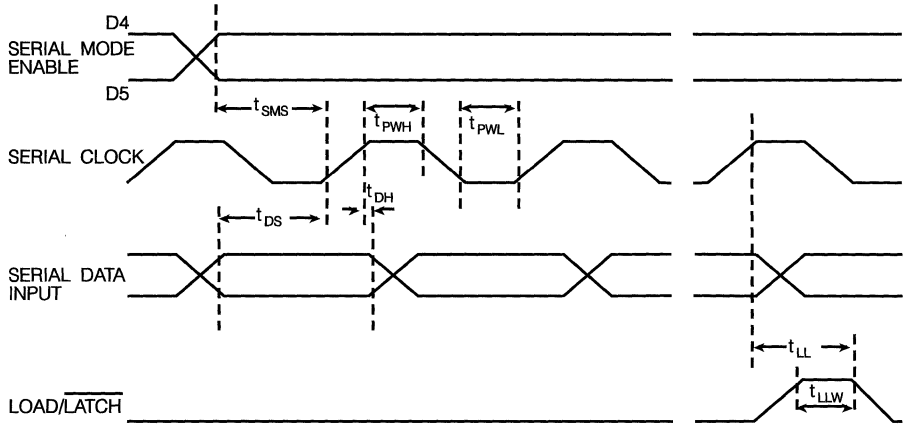
Load Configuration	Load/Latch	Control	RX/TX, Private Enable
Parallel	0	0	Latched
Parallel	1	0	Transparent
Parallel	X	1	Transparent
Serial	0 - 1 - 0	0	Serial Load
Serial	X	1	Transparent

Notes: "0 - 1 - 0" is a strobe pulse as shown in Figures 4 and 5 (Timing).
"X" denotes any logical state.

Table 2 - Load/Latch and Control Functions

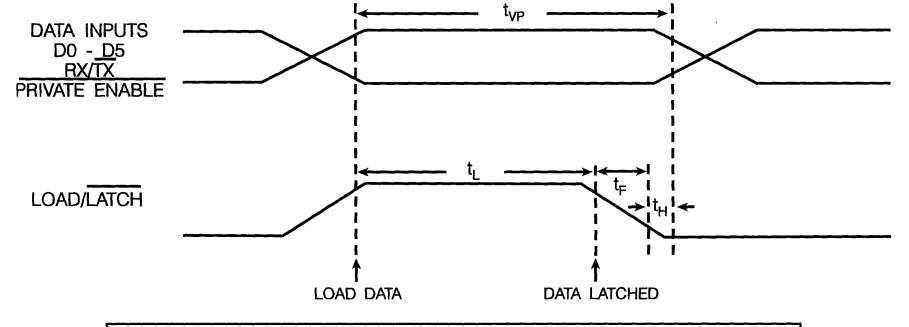
TIMING INFORMATION

Control instructions are input by serial (Figure 4) or parallel (Figure 5) means, using Data Inputs and Load/Latch as shown.



	Min.	Typ.	Max.	Unit
Serial Mode Enable Set Up Time (t_{SMS})	250	-	-	ns
Clock "High" Pulse Width (t_{PWH})	250	-	-	ns
Clock "Low" Pulse Width (t_{PWL})	250	-	-	ns
Data Set Up Time (t_{DS})	150	-	-	ns
Data Hold Time (t_{DH})	50	-	-	ns
Load/Latch Set Up Time (t_{LL})	250	-	-	ns
Load/Latch Pulse Width (t_{LLW})	150	-	-	ns

Figure 4 - Serial Load Timing



	Min.	Typ.	Max.	Unit
Data Valid Time (t_{VP})	200	-	-	ns
Load Time (t_L)	150	-	-	ns
Fall Time (t_F)	-	-	50	ns
Data Hold Time (t_H)	50	-	-	ns

Figure 5 - Parallel Load Timing

SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin	-0.3V to (V_{DD} + 0.3 V)
Sink/Source Current	
(Supply pins)	±30 mA
(Other pins)	±20 mA
Total Device Dissipation	
@ T_{AMB} 25°C	800 mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted:

T_{AMB} = 25°C

Xtal/Clock f_0 = 4.0 MHz

V_{DD} = 5.0V

Audio level 0dB ref = 300 mVrms.

Composite input signal = 0dB, 1 kHz tone in, -12dB (6kHz band limited) gaussian white noise with a -20dB CTCSS tone.

2

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
TX (Private)		-	-	15.0	mA
TX (Operating)		-	-	12.0	mA
RX (Operating)		-	-	7.0	mA
Analog Input Impedance			0.5	-	MΩ
Analog Output Impedance		-	0.5	-	kΩ
Tone Input Impedance		-	0.5	-	MΩ
Input Logic "1"		3.5	-	-	V
Input Logic "0"		-	-	1.5	V
Output Logic "1" (I=-0.1mA)		4.0	-	-	V
Output Logic "0" (I=-0.1mA)		-	-	1.0	V
Dynamic Values					
Decoder					
Input Signal Level	1,4	-20	-	-	dB
Response Time	1,4,6	-	-	250	ms
Deresponse Time	1,4,6	-	-	250	ms
Selectivity	4	±0.5	-	±3.0	$\%f_o$
Encoder					
Tone Output Level (775mV_{rms} ref)		-3.0	0	+3.0	dB
Tone Frequency Accuracy		-0.3	-	+0.3	$\%f_o$
Tone Harmonic Distortion		-	2.0	5.0	%
Tone Output Load Current	2	-	-	5.0	mA
Output Level Variation between Tones	9	-1.0	-	1.0	dB
Risetime (to 90% nominal level)					
(f_o>100 Hz)	5	-	15	-	ms
(f_o<100 Hz)	5	-	45	-	ms
RX Clear					
Total Harmonic Distortion	3	-	2	5	%
Output Noise Level	7	-	-43	-	dB
Passband Gain (300-3033Hz)	3	-1	0	+1	dB
Passband Ripple (300-3033Hz)	3	-	-	3	dB

Characteristics	See Note	Min.	Typ.	Max.	Unit
Audio Stopband Attenuation					
(f_{in}>3333Hz)	8	-	-20	-	dB
(f_{in}>3633Hz)	8	-	-45	-	dB
(f_{in}<250Hz)		-	-42	-	dB
RX Invert					
Total Harmonic Distortion	3,8	-	4	10	%
Baseband Breakthrough	3	-	-40	-	dB
Carrier Breakthrough		-	-40	-	dB
Output Noise Level	7,8	-	-37	-	dB
Passband Ripple (300-3000Hz)	3	-	-	4	dB
Audio Stopband Attenuation					
(f_{in}>3333Hz)	8	-	-50	-	dB
(f_{in}>3633Hz)	8	-	-60	-	dB
(f_{in}<250Hz)		-	-60	-	dB
TX Clear					
Total Harmonic Distortion	3	-	3	5	%
Output Noise Level	7	-	-43	-	dB
Passband Gain (300-3033Hz)	3	-	0	-	dB
Passband Ripple (300-3033Hz)	3	-	-	3	dB
Audio Stopband Attenuation					
(f_{in}>3333Hz)	8	-	-20	-	dB
(f_{in}>3633Hz)	8	-	-45	-	dB
(f_{in}<250Hz)		-	-42	-	dB
TX Invert					
Total Harmonic Distortion	3,8	-	4	10	%
Baseband Breakthrough		-	-40	-	dB
Carrier Breakthrough		-	-40	-	dB
Output Noise Level	7,8	-	-37	-	dB
Passband Ripple (300-3033Hz)	3,8	-	-	4	dB
Audio Stopband Attenuation					
(f_{in}>3333Hz)	8	-	-50	-	dB
(f_{in}>3633Hz)	8	-	-60	-	dB
(f_{in}<250Hz)	8	-	-60	-	dB

2

NOTES:

1. These values are obtained using the external integrating components given in Figure 3.
2. An emitter follower output
3. With an input signal of 1 kHz @ 0dB.
4. Under Composite Signal test conditions.
5. Any programmed tone with R_L=600 Ω, C_L=15pF, including any response to a phase reversal instruction.
6. f_o > 100 Hz, (for 100Hz > f_o > 67Hz: t = [100/f_o(Hz)] x 250ms).
7. Input ac short-circuit, audio path enabled.
8. Due to frequency inversion, these figures reflect the difference from the ideal response.
9. Reference 156.7 Hz (MX175 and MX275).

D0-D5	NOTONE	RX/TX	PRIVATE ENABLE	PTL	RXTONE DETECT	RXTONE DECODER	TONE OUTPUT	TONE PHASE	TX PATH	RX PATH	PATH STATE	TONE
TONE	1	0	0	1	0	1	YES	0°	OPEN	BIAS	INV	TX, TONE
TONE	1	0	0	0	0	1	YES	180°	OPEN	BIAS	INV	TX, TONE REV
NOTONE	0	0	0	X	0	1	BIAS	X	OPEN	BIAS	CLR	TX, NOTONE
TONE	1	1	0	1	0	1	BIAS	X	BIAS	BIAS	X	INCOMPATIBLE
TONE	1	1	0	0	0	1	BIAS	X	BIAS	OPEN	CLR	INCOMPATIBLE
TONE	1	1	0	X	1	0	BIAS	X	BIAS	OPEN	INV	COMPATIBLE
NOTONE	0	1	0	X	X	0	BIAS	X	BIAS	OPEN	CLR	RX, NOTONE
TONE	1	0	1	1	0	1	YES	0°	OPEN	BIAS	CLR	TX, TONE
TONE	1	0	1	0	0	1	YES	180°	OPEN	BIAS	CLR	TX, TONE REV
NOTONE	0	0	1	X	0	1	BIAS	X	OPEN	BIAS	CLR	TX, NOTONE
TONE	1	1	1	1	0	1	BIAS	X	BIAS	BIAS	X	INCOMPATIBLE
TONE	1	1	1	0	0	1	BIAS	X	BIAS	OPEN	CLR	INCOMPATIBLE
TONE	1	1	1	X	1	0	BIAS	X	BIAS	OPEN	CLR	COMPATIBLE
NOTONE	0	1	1	X	X	0	BIAS	X	BIAS	OPEN	CLR	RX, NOTONE

ALGEBRAIC FUNCTIONS:
RX PATH ON = RX * (PTL + RX TONE DECODER)
CLEAR PATH = NOTONE + PRIVATE ENABLE + (PTL * RX * RX TONE DECODER)
NOTONE (D0-D5) = 000011
CARRIER FREQUENCY = 3333Hz DURING INVERTED PATH (TX OR RX)

NOTES:
1. The Pre- and De-emphasis circuits remain in the transmit path in both Clear and Invert Modes.
2. Power remains applied to the CTCSS tone decoder at all times.
3. During Clear operation the carrier frequency is turned off to reduce spurious emissions.

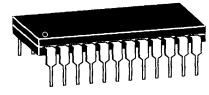
Table 4 - Functions and Outputs

SUB-AUDIO SIGNALING PROCESSOR

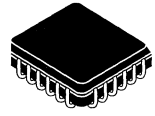
DESCRIPTION

The MX805A, a member of the DBS800 IC family, is a sub-audio frequency signaling processor that provides outband audio and digital signaling capability for LMR systems.

The MX805A is designed for the transmission and non-predictive reception of 1) Continuous Tone Controlled Sub-audible Squelch (CTCSS) tones and other non-standard frequencies, and 2) Non-Return-to-Zero (NRZ) data reception and transmission to provide Digitally Coded Squelch (DCS/DPL™) and LTR™ signaling.



MX805AJ
24-pin CDIP



MX805ALH
24-pin PLCC

The MX805A contains the following:

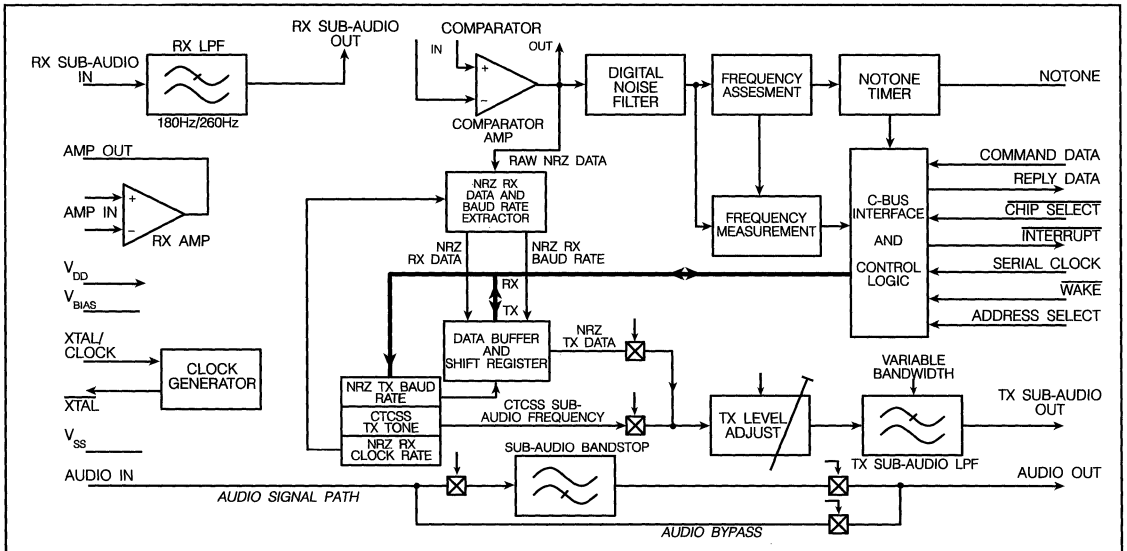
- •A non-predictive CTCSS Tone Decoder and DCS sub-audio signal demodulator.
- •A CTCSS/NRZ Encoder with TX level adjustment and lowpass filter output stage with optional NRZ pre-emphasis.
- •A selectable sub-audio bandstop filter.
- •A Notone (CTCSS RX) period timer.

Setting of the MX805A functions and modes is by data loaded from the microcontroller to the controlling registers within the device. Reply Data and Interrupt protocol keep the microcontroller up to date on the operational status of the circuitry.

CTCSS tone data for transmission is generated in the microcontroller, loaded to the CTCSS TX Frequency Register, encoded and output as a tone via the TX Sub-Audio LPF.

Received non-predicted CTCSS tone frequencies are measured and the resulting data, in the form of a 2-byte data word, is presented to the microcontroller for matching against a look-up table. Noise filtering is provided to improve the signal quality prior to measurement.

NRZ coded data streams for transmission, when generated within a microcontroller, are loaded to the NRZ TX Data



MX805A Sub-Audio Signaling Processor

DPL is a trademark of Motorola, Inc. LTR is a trademark of E.F. Johnson Co.

DESCRIPTION...

Buffer and output, in 8-bit bytes, through the lowpass filter circuitry as sub-audible signals. DCS turn-off tones can be added to the data signals by switching the MX805A to the CTCSS transmit mode at the appropriate time. NRZ coding is produced by the microcontroller and translated to sub-audio signals by the MX805A.

Received NRZ data is filtered, detected, and placed into the NRZ RX Data Register, which is then available for transfer (one byte at a time) to the microcontroller for decoding by software. Clock extraction circuitry is provided on-chip. TX and RX baud rates are selectable.

Hardware and software are designed to allow consecutive addressing of two MX805A Sub-Audio Signaling Processors to achieve multi-mode duplex operation. Powersaving may be controlled by software or an input dedicated to the purpose.

The MX805A is a low-power 5 volt CMOS IC available in 24-pin Cerdip and 24-lead plastic SMT packages. It is pin-compatible with the earlier MX805.

PIN FUNCTION CHART

Pin	Function
1	**$\overline{\text{Xtal}}$:** The output from the on-chip clock oscillator inverter. External components are required at this input when a Xtal input is used. See Figure 2.
2	**Xtal/Clock:** The input to the clock oscillator inverter. A Xtal or externally derived clock should be connected here.
3	**Address Select:** This input enables two MX805As to be used on the same C-BUS to provide full-duplex operation. See Tables 1 and 2.
4	**$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$):** The output of this pin indicates an interrupt condition to the microcontroller by going to a logic "0." This "wire-or-able" output allows the connection of up to 8 peripherals to 1 interrupt port on the microcontroller. This pin has a low impedance pulldown to logic "0" when active, and a high impedance when inactive. The system $\overline{\text{IRQ}}$ line requires 1 pullup resistor to V_{DD}. The conditions that cause interrupts are indicated in the Status Register (Table 4) and are shown below: RX CTCSS Tone Measurement Completed CTCSS NOTONE Timer Expired 1 NRZ RX Data Byte Received New NRZ Data Received Before Last Byte Read NRZ TX Buffer Ready NRZ Data Transmission Complete
5	**Serial Clock:** This is the "C-BUS" serial clock input. This clock, produced by the microcontroller, is used for transfer timing of commands and data to and from the MX805A. See timing diagrams.
6	**Command Data:** This is the C-BUS serial data input from the microcontroller. Data is loaded to this device in 8-bit bytes, MSB (bit 7) first and LSB (bit 0) last, synchronized to the Serial Clock. See timing diagrams.
7	**$\overline{\text{Chip Select}}$ ($\overline{\text{CS}}$):** This is the "C-BUS" data loading control function. This input is provided by the microcontroller. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See timing diagrams.
8	**Reply Data:** This is the C-BUS serial data output to the microcontroller. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the $\overline{\text{Chip Select}}$ input. This 3-state output is held at high impedance when not sending data to the microcontroller. See timing diagrams.
9	**TX Sub-Audio Out:** This is the sub-audio output (pure or NRZ derived). Signals are band limited. The TX Output Filter has a variable bandwidth (see Table 6). This output is at V_{BIAS} (a) when the NRZ Encoder is enabled but no data is being transmitted, (b) when the MX805A is placed in the Powersave All condition.

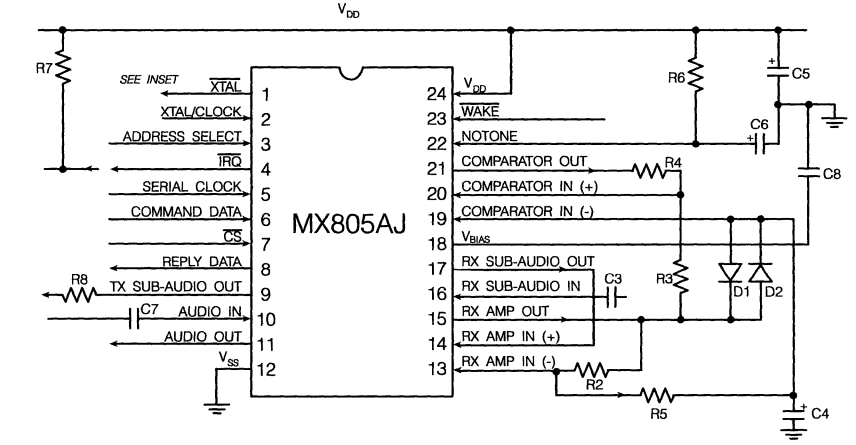
PIN FUNCTION CHART

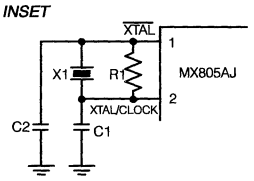
Pin	Function
10	**Audio In:** This is the input to the switched sub-audio bandstop (highpass) filter. It is internally biased, and should be a.c. coupled by capacitor C_7.
11	**Audio Out**: This is the output of the audio signal path (filter or bypass). It is controlled by the Control Register. When disabled, the pin is held at V_{BIAS}.
12	**V_{SS}:** Negative supply (GND).
13	**RX Amp In (-):** This is the inverting input to the on-chip RX Input Amp (see Figures 2, 3 and 4).
14	**RX Amp In (+):** This is the non-inverting input to the on-chip RX Input Amp.
15	**RX Amp Out:** This is the output of the on-chip RX Input Op-Amp. This circuit may be used, with external components, as a signal amplifier and anti-aliasing filter prior to the RX Lowpass Filter. or for other purposes. See Figure 2 for component details.
16	**RX Sub-Audio In:** This is the received Sub-Audio (CTCSS/NRZ) input. It is internally referenced to V_{BIAS}. The signal to this pin should be a.c. coupled or biased. See Figure 2.
17	**RX Sub-Audio Out:** This is the output of the RX lowpass filter. It may be coupled into the on-chip amplifier or comparator as required.
18	**V_{BIAS}:** The internal circuitry bias line, held at »V_{DD}/2. This pin must be decoupled to V_{ss} by capacitor C_8 (see Figure 2).
19	**Comparator In (-):** This is the inverting input to the on-chip "comparator" amplifier. See Figures 2, 3 and 4.
20	**Comparator In (+):** This is the non-inverting input to the on-chip "comparator" amplifier. See Figures 2, 3 and 4.
21	**Comparator Out:** This is the output of the "comparator" amplifier. This node is also connected internally to the input of the Digital Noise Filter (See Figure 1). When both decoders (CTCSS or NRZ) are powersaved, this output is at logic "0."
22	**Notone Timing:** External RC components connected to this pin form the timing mechanism of a Notone period timer. The external network determines the "charge rate" of the timer to V_{BIAS}. The expiration of the timer will cause an interrupt. This function is only used in the CTCSS RX mode. See page 9.
23	**$\overline{\text{Wake}}$:** This "real time" input can be used to reactivate the MX805A from the "Powersave All" condition using an externally derived signal. The MX805A will be in a "Powersave All" condition when both this pin and bit 0 of the Control Register are set to a logic "1." Recovery from "Powersave All" is achieved by putting either the $\overline{\text{Wake}}$ pin or the "Powersave All" bit at logic "0." This allows MX805A activation by the microcontroller or an external signal, such as RSSI or Carrier Detect.
24	**V_{DD}:** Positive supply. A single +5 volt regulated supply is required.

NOTES:
More information on external components and the DBS 800 system integration of the MX805A are contained in the DBS 800 System Support Document. Guidance on the generation and manipulation of NRZ and RX and TX data is given in the DBS 800 Application support document.

C-BUS is MX-COM's proprietary standard for the transmission of commands and data between a microcontroller and DBS 800 microcircuits. It may be used with any microcontroller, and can, if desired, take advantage of the hardware and serial I/O functions embodied into many types of microcontrollers. The C-BUS data rate is determined by the microcontroller.

Application Information





Component	Value		
R1	1.0MΩ	C1	See Note 5
R2	360kΩ	C2	See Note 5
R3	10.0kΩ	C3	1.5µF
R4	150kΩ	C4	15.0µF, 6V Tant. ±20%
R5	100kΩ	C5	1.0µF, 10V Tant. ±20%
R6	150kΩ	C6	1.0µF, 10V Tant. ±20%
R7	22.0kΩ	C7	0.1µF, 25V x 7R ±20%
R8	360kΩ	C8	1.0µF
		D1	silicon small signal
		D2	silicon small signal
Tolerance: R = ±5%		X1	4.00MHz

Figure 2 - Recommended External Components

Notes

1. Xtal/Clock circuitry components shown in INSET are recommended in accordance with MX-COM's "Standard and DBS 800 Crystal Oscillators" application note.

2. Resistor R8 is a System Component. Its value is chosen together with the MX806A Modulation Summing Amplifier to provide a sub-audio signal level of -11.0dB to the system modulator.

3. Figures 3 and 4 illustrate alternative input component configurations.

4. The value of R5 is dependent on the input signal level. Values given are for the specified composite signal of 40 mVrms. R4 adds hysteresis to the comparator and is not always required.

5. The values used for C_1 and C_2 are determined by the frequency of X_1.

As a guide:

$C_1 = C_2 = 33pF$ for $X_1 < 5.0MHz$.

$C_1 = C_2 = 18pF$ for $X_1 > 5.0MHz$.

If the on-chip Xtal oscillator is to be used, then the external components X_1, C_1, C_2, and R_1 are required as shown in Figure 2 (inset). If an external clock source is used these components are not required; the input should be connected to the Xtal/clock pin and the Xtal pin left unconnected.

6. Resistor R7 is used as the DBS 800 system common pullup for the C-BUS Interrupt Request (IRQ) line. The optimum value of this component will depend upon the circuitry connected to the IRQ line.

7. The level at this point should be approximately 900mV peak to peak.

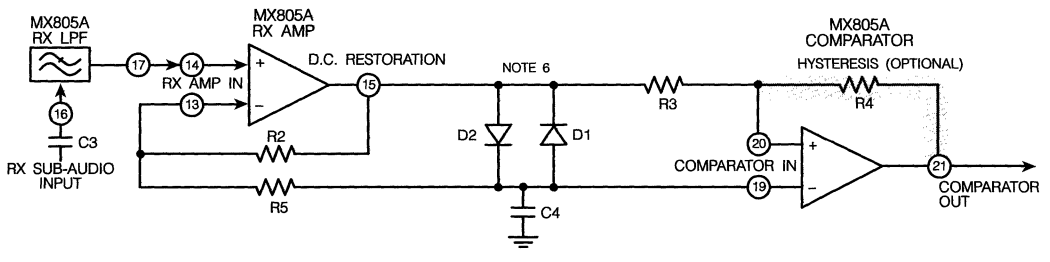


Figure 3 - MX805A Input Components

Application Information

Figure 3 shows an input configuration that is generally for use for CTCSS signal and NRZ data reception.

Input coupling capacitor C3 is required because the RX Sub-Audio Input is held at V_{BIAS} during all powered conditions of the MX805A. Diodes D_1 and D_2 can be any silicon small-signal diode.

The output resistance (open loop) of the on-chip RX Amp is ≈6kΩ. In the configuration shown in Figure 3, the (RX Amp) RC time constant is therefore 90ms. If this period is too long for some systems, ie. those using half-duplex, short data burst, an external amplifier should be considered in place of the on-chip RX Amp.

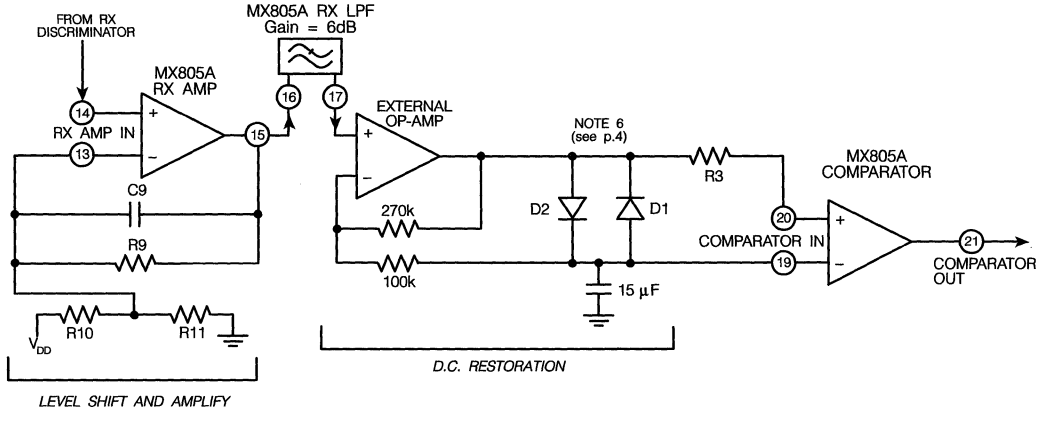


Figure 4 - MX805 Input Components using an External Op-Amp

Using An External Op-Amp

For d.c. coupling the MX805A to the receiver's discriminator output when using burst mode NRZ communication, it is recommended that an additional, external Op-Amp is employed as configured in Figure 4. This configuration will quickly compensate for sudden shifts of DC input bias.

Components R_9, R_{10}, and R_{11} should be calculated to provide an accurate potential of 2.5 Vd.c. (equal to V_{BIAS}) at pin junction 15/16 when using a discriminator input and 900 mV peak to peak at the output of the external op-amp. Note that the MX805A LPF has a 6 dB gain. If additional filtering is required, C_9 should be used; it should be calculated with R_9 to provide a lowpass cut-off frequency (f_{CO}) of 500 Hz.

Operating Modes

NRZ Encoding

The NRZ Encoder is formed by a shift register and the TX Sub-Audio Lowpass Filter. Data loaded from the Command Data line is output one 8-bit byte at a time from the NRZ TX Data Register. The output data level may be adjusted and filtered. Data may be pre-emphasized via a C-BUS command. The expected RX baud rate is programmed as the NRZ TX Baud Rate ($R_{NRZ\,TX}$). See Table 5.

CTCSS Encoding

The CTCSS Tone Encoder is comprised of a clock-divider programmed by an 11-bit binary number (Q) loaded to the CTCSS TX Frequency Register (see Table 5) via the C-BUS Command Data line.

The square-wave output of the encoder is fed through the TX Level Adjust variable gain block to the TX Sub-Audio lowpass filter, a variable bandwidth circuit controlled by 4 bits (P) of the CTCSS TX Frequency Register. The TX Sub-Audio output is a sine-wave. Standard and non-standard sub-audio tones are available. A CDCS turn-off tone may also be generated.

NRZ Decoding

Input (NRZ type) sub-audio signals are filtered and the data clock extracted. Decoded data is serially loaded into a shift register buffer. This data is output one 8-bit byte at a time as Reply Data from the NRZ RX Data Register to the microcontroller. The expected RX baud rate is programmed as the NRZ RX Baud Rate ($R_{NRZ\,RX}$). See Table 5. Any codeword recognition can be carried out by software.

CTCSS Decoding

Received CTCSS signals are filtered, and coherence is increased by the digital noise filter. The quality of the signal is assessed by measurement of the cycle-to-cycle period variance and, provided it is sufficiently good, the frequency is measured over a period of 122.64 milliseconds (4.0 MHz xtal).

If the average signal quality is consistently too low, Notone is indicated; if not, the input frequency is precisely indicated in the CTCSS RX Frequency Register in a binary form.

Any single sub-audio tone within the specified range may be selected, enabling a DCS turn-off tone (of 134 Hz) to be decoded while in the NRZ RX mode.

Controlling Protocol

Control of the MX805A Sub-Audio Signaling Processor's operation is by communication between the microcontroller and the MX805A internal registers on the C-BUS, using Address/Commands (A/Cs) and appended instructions or data (see Figure 9). The use and content of these instructions is detailed in the following paragraphs and tables. The Address Select Input enables the addressing of 2 separate MX805As on the C-BUS to provide full-duplex signaling.

MX805A Internal Registers

MX805A Internal Registers are detailed as follows:

Control Register ($70_H/78_H$) -- Write only, control and configuration of the MX805.

Status Register ($71_H/79_H$) -- Read only, reporting of device functions.

CTCSS RX Frequency Register ($72_H/7A_H$) -- Read only, a 2-byte binary word indicating the frequency of the received sub-audio input.

CTCSS TX Frequency/NRZ TX or RX Baud Rate Register ($73_H/7B_H$) -- Write only, a 2-byte command to set the relevant parameters.

NRZ RX Data Register ($74_H/7C_H$) -- Read only, a single byte of received NRZ data.

NRX TX Data Register ($75_H/7D_H$) -- Write only, to load a single byte of NRZ data for transmission.

Gain Set Register ($76_H/7E_H$) -- Write only, a single byte to set the gain of the TX Lowpass Filter.

2

Address/Commands

The first byte of a loaded data sequence is always recognized by the C-BUS as an Address/Command (A/C) byte. Instruction and data transactions to and from this device consist of an Address/Command byte followed by either:

(i) further instructions or data
or (ii) a Status or data Reply.

Instructions and data are loaded and transferred, via C-BUS, in accordance with the timing information in Figures 9 and 10.

Placing the Address Select input at a logic "0" will address MX805A #1, a logic "1" will address MX805 #2.

Tables 1 and 2 show the list of A/C bytes relevant to the MX805A.

Command Assignment	Address/Command (A/C) Byte + Hex.	Binary MSB LSB		Data Bytes
General Reset	01	0 0 0 0 0 0 0 1		
Write to Control Register	70	0 1 1 1 0 0 0 0	+	1 byte instruction to Control Register
Read Status Register	71	0 1 1 1 0 0 0 1	+	1 byte reply from Status Register
Read CTCSS RX Freq. Reg.	72	0 1 1 1 0 0 1 0	+	2 byte reply of CTCSS RX Data
Write to CTCSS TX Freq./ NRZ Baud Rate Reg.	73	0 1 1 1 0 0 1 1	+	2 byte instruction for TX Frequency and NRZ TX/RX baud rates
Read NRZ RX Data Reg.	74	0 1 1 1 0 1 0 0	+	1 byte binary data Reply
Write to NRZ TX Data Reg.	75	0 1 1 1 0 1 0 1	+	1 byte binary data Command
Write to Gain Set Reg.	76	0 1 1 1 0 1 1 0	+	1 byte instruction for TX Output

Table 1 - MX805A #1 C-BUS Address/Commands - (Address Select input at a logic "0")

Command Assignment	Address/Command (A/C) Byte + Hex.	Binary MSB LSB		Data Bytes
General Reset	01	0 0 0 0 0 0 0 1		
Write to Control Register	78	0 1 1 1 1 0 0 0	+	1 byte instruction to Control Register
Read Status Register	79	0 1 1 1 1 0 0 1	+	1 byte reply from Status Register
Read CTCSS RX Freq. Reg.	7A	0 1 1 1 1 0 1 0	+	2 byte reply of CTCSS RX Data
Write to CTCSS TX Freq./ NRZ Baud Rate Reg.	7B	0 1 1 1 1 0 1 1	+	2 byte instruction for TX Frequency and NRZ TX/RX baud rates
Read NRZ RX Data Reg.	7C	0 1 1 1 1 1 0 0	+	1 byte binary data Reply
Write to NRZ TX Data Reg.	7D	0 1 1 1 1 1 0 1	+	1 byte binary data Command
Write to Gain Set Reg.	7E	0 1 1 1 1 1 1 0	+	1 byte instruction for TX Output

Table 2 - MX805A #2 C-BUS Address/Commands - (Address Select input at a logic "1")

Controlling Protocol...

"Write to Control Register" -- A/C 70_H (78_H), followed by 1 byte of Command Data

Table 3 below shows the configurations available to the MX805A. Bits 5, 6 and 7 are used together to Enable and Powersave circuit sections as required.

Setting			Control Bits	
MSB			Transmitted First	
7	6	5	Enabled	Powersaved
0	0	0	CTCSS Decoder	NRZ Decoder and Both Encoders
0	0	1	NRZ Decoder	CTCSS Decoder and Both Encoders
0	1	0	CTCSS Encoder	All Decoders
0	1	1	NRZ Encoder	All Decoders
1	0	0	CTCSS Encoder and Decoder	NRZ Encoder and Decoder
1	0	1	NRZ Encoder and CTCSS Decoder	No circuits
1	1	0	NRZ Decoder and CTCSS Decoder	All Encoders
1	1	1	NRZ Decoder	All Encoders except TX Sub-Audio LPF and CTCSS Decoder

4	
1	Enable Audio Output -- Used with Bit 3
0	Disable Audio Output -- Output to V_{BIAS}
3	
1	Enable Sub-Audio Bandstop Filter (Audio Signal Path)
0	Bypass Sub-Audio Bandstop Filter
2	
1	Enable All MX805A Interrupts
0	Disable All MX805A Interrupts
1	
1	Set RX Lowpass Filter Bandwidth to 180Hz -- For low CTCSS tones or NRZ data
0	Set RX Lowpass Filter Bandwidth to 260Hz
0	
1	All Encoders and Decoders Powersaved
0	All Encoders and Decoders Enabled unless individually Powersaved

Table 3 - Control Register

General Reset

Upon power-up the bits in the MX805A registers will be random (either "0" or "1"). A General Reset Command 01_H) will be required to reset all ICs on the C-BUS. It has the following effect on the MX805A:

Control Register	Set as 00_H
Status Register	Set as 00_H
Notone Timer	Discharged

Warning: The following MX805A register configurations are not affected by a General Reset Command:

CTCSS RX Frequency
CTCSS TX Frequency/NRZ Baud Rate Register
NRZ RX Data Register
NRZ TX Data Register
Gain Set Register

Note that setting the Control Register in this way will set the MX805A to the CTCSS decode mode and overwrite a "Powersave All" instruction. It should also be considered that a General Reset command will reset ALL DBS 800 ICs operating on the C-BUS.

Glossary of Abbreviations

Below is a list of abbreviations used in this Data Bulletin.

DCS	Continuous Digitally Coded Squelch
CTCSS	Continuous Tone Controlled Sub-Audible Squelch
DPL™	Digital Private Line
LTR™	Logic Trunked Radio
NRZ	Non-Return-to Zero
f_{CO}	Filter Cut-off frequency
$f_{CTCSS\ IN}$	Sub-Audio RX frequency
$f_{CTCSS\ OUT}$	Sub-Audio TX frequency
f_{TONE}	Tone frequency
f_{XTAL}	Xtal/Clock frequency
$R_{NRZ\ RX}$	NRZ RX baud rate
$R_{NRZ\ TX}$	NRZ TX baud rate
S_{INPUT}	Audio input signal

Controlling Protocol...

"Read Status Register" -- A/C 71_H (79_H), followed by 1 byte of Reply Data

The Status Register indicates the operational condition of the MX805A. Bits 0 to 5 are set individually to indicate specific actions within the device. When a Status bit is set to a logic"1," an Interrupt Request (IRQ) output is generated. A read of the Status Register will reset the Interrupt and ascertain the state of this register. Table 4 shows the conditions indicated by the Status bits.

Setting	Set By	Logic	Cleared By	Logic
MSB	***Received First***			
7, 6	Not used	"0"	Not used	"0"
5	NRZ data transmission complete. No new data is loaded.	"1"	1. Write to NRZ TX Data Reg., or 2. General Reset, or 3. NRZ Encoder Powersave	"0"
4	NRZ TX Data Buffer ready for next data byte.	"1"	1. Write to NRZ TX Data Reg., or 2. General Reset, or 3. NRZ TX Powersave	"0"
3	New NRZ RX data received before last byte was read.	"1"	1. Read NRZ RX Data Reg., or 2. General Reset, or 3. NRZ Decoder Powersave	"0"
2	1 byte of NRZ RX data received.	"1"	1. Read NRZ RX Data Reg., or 2. General Reset, or 3. NRZ Decoder Powersave	"0"
1	Notone Timer period expired.	"1"	1. Read Status Register, or 2. General Reset, or 3. CTCSS Decoder Powersave	"0"
0	RX Tone Measurement Complete	"1"	1. Read Status Register, or 2. General Reset, or 3. CTCSS Decoder Powersave	"0"

Table 4 - Status Register

"Read CTCSS RX Frequency Register" -- A/C 72_H ($7A_H$), followed by 2 bytes of Reply Data

Measurement of CTCSS RX Frequency ($f_{CTCSS\ IN}$)

The input sub-audio signal ($f_{CTCSS\ IN}$) is filtered, doubled and measured in the Frequency Counter over the "measurement period" (122.64ms) (4.0 MHz Xtal).

The measuring function counts the number of complete input cycles occurring within the measurement period and then the number of measuring-clock cycles necessary to make up the period.

When the measurement period of a successful decode is complete, the RX Tone Measurement bit in the Status Register and the Interrupt bit are set.

The CTCSS RX Frequency Register will now indicate the sub-audio signal frequency ($f_{CTCSS\ IN}$) in the form of 2 data bytes (1 and 0) as illustrated in Figure 6.

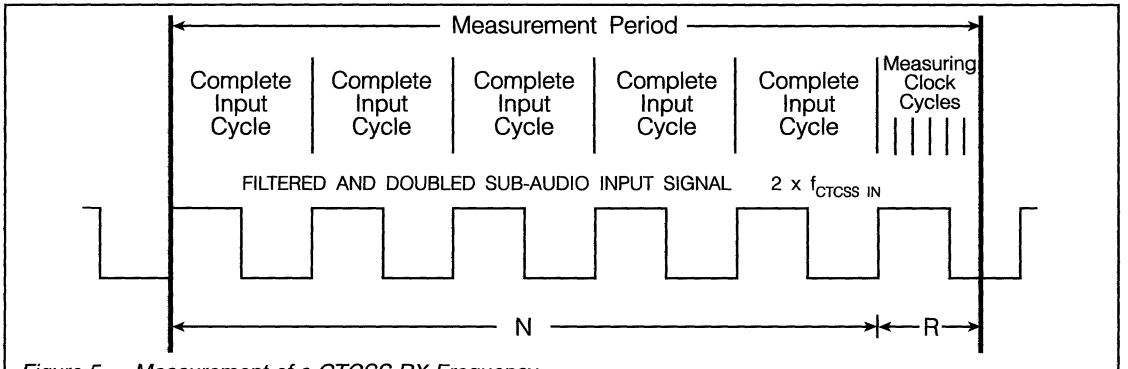


Figure 5 - Measurement of a CTCSS RX Frequency

Controlling Protocol...

"Read CTCSS RX Frequency Register"...

The Integer (N) -- Byte 1
A binary number representing twice the number of complete input sub-audio cycle periods counted during the measurement period of 122.64ms (4.0 MHz Xtal).

The Remainder (R) -- Byte 0
A binary number representing the remainder part, R, of 2 x the Sub-Audio Input Frequency. R = number of specified measuring-clock cycles required to complete the specified measurement period (See N). The clock cycle frequency is 4166.6Hz (4.0 MHz Xtal).

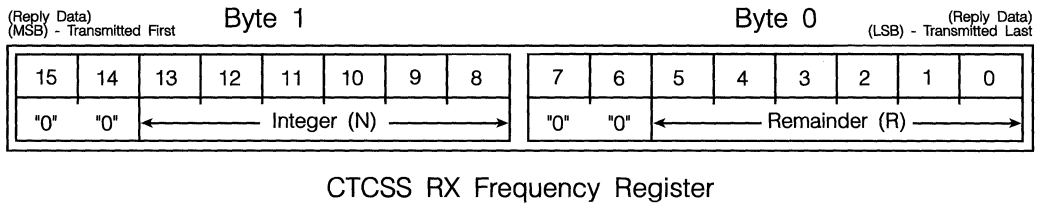


Figure 6 - Format of the CTCSS RX Frequency Register

CTCSS RX Frequency Register

Figure 6 above shows the format of the CTCSS RX Frequency Register.

Bits 8 (LSB) to 13 (MSB) are used to represent the Integer (N). From Byte 1, valid values of $N = 16 \leq N \leq 61$.

ie. values of N less than 16 and greater than 61 are not within the specified frequency band.

Bits 0 (LSB) to 5 (MSB) are used to represent the Remainder (R). From Byte 0, valid values of $R \leq 31$.

This register is not affected by the General Reset command (01_H) and may adopt any random configuration at Power-Up.

CTCSS RX Frequency Measurement Formulas

To assist in the production of "look-up" tables and limit-values in the microcontroller, and to provide guidance upon the determination of N and R from a measured CTCSS frequency, the following formulas show the derivation of the CTCSS RX Frequency ($f_{CTCSS\ IN}$) from the measured data bytes (N and R).

$f_{CTCSS\ IN}$

In the measurement period of 122.64ms there are N cycles at $2 \times f_{CTCSS\ IN}$ and R clock cycles at 4166.6Hz, for any input frequency.

So,

$$f_{CTCSS\ IN} = \frac{N \times f_{XTAL}}{1920 \times (511-R)} \text{ Hz} \quad [1]$$

$$N = \text{INT}\left[\frac{1920 \times 511 \times f_{CTCSS\ IN}}{f_{XTAL}}\right] \quad [2]$$

$$R = \text{INT}\left[511 - \left[\frac{N \times f_{XTAL}}{1920 \times f_{CTCSS\ IN}}\right] + 0.5\right] \quad [3]$$

Calculate N first

Examples (f_{XTAL} = 4.00MHz): $f_{CTCSS\ IN}$ = 100Hz N = 24 R = 11; $f_{CTCSS\ IN}$ = 250Hz N = 61 R = 3

Notone Timing

The input sub-audio signal is monitored by the Frequency Assessment circuitry. Before any Notone action is enabled, the MX805A must have achieved at least one successful "Tone Measurement Complete" action.

If there is no signal or the signal is of a consistently poor quality, the Notone Timer will start to charge via the timing components. When the timing period has expired (at $V_{DD}/2$), an Interrupt and a Status bit (Notone Timer Expired) are generated. This is a one-shot function which is reset by a "Tone Measurement Complete" interrupt.

Controlling Protocol...

"Write to CTCSS TX Frequency/NRZ Baud Rate Register" -- A/C 73_H ($7B_H$), followed by 2 bytes of Command Data

The information loaded to this register will set either the:

(a) CTCSS TX Tone Frequency $f_{CTCSS\ OUT}$
(b) NRZ TX Baud Rate $R_{NRZ\ TX}$
(c) NRZ RX Baud Rate $R_{NRZ\ RX}$

The chosen mode for this register (a, b or c) is determined by the MX805A modes enabled by the Control Register, as shown in the table below.

Control Register Bits 7	6	5	MX805 Mode Enabled	CTCSS TX/NRZ Baud Rate Register Function
0	0	0	CTCSS Decode	
0	0	1	NRZ Decode	NRZ RX Baud Rate
0	1	0	CTCSS Encode	CTCSS TX Frequency
0	1	1	NRZ Encode	NRZ TX Baud Rate
1	0	0	CTCSS Encode and Decode	CTCSS TX Frequency
1	0	1	NRZ Encode & CTCSS Decode	NRZ TX Baud Rate
1	1	0	NRZ & CTCSS Decode	NRZ RX Baud Rate
1	1	1	NRZ Decode	NRZ RX Baud Rate

Table 5 - CTCSS Frequency/NRZ Baud Rate Register Configurations

Data Format

Data is transmitted to this register as 2 bytes of Command Data in the form illustrated in the diagram below. This register is not affected by the General Reset Command (01_H) and may adopt any random configuration at power-up.

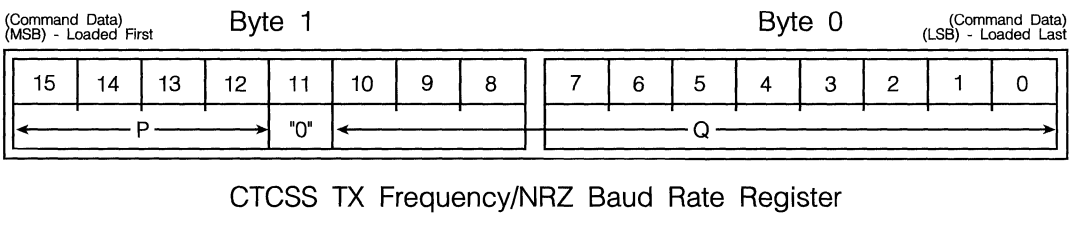


Figure 7 - Format of the CTCSS TX Frequency/NRZ Baud Rate Register

Command Words P and Q

The two data words, P and Q, loaded to this register are interpreted as:

P = a binary number to set the TX Sub-Audio Lowpass Filter bandwidth (applicable to NRZ and CTCSS modes).
Q = a binary number to set the frequency or baud rate of the selected function.

Command Word P

Bits 15	14	LSB 13	12	P	LPF Bandwidth
0	0	1	0	2	300Hz
0	0	1	1	3	200Hz
0	1	0	0	4	150Hz
0	1	0	1	5	120Hz
0	1	1	0	6	100Hz
0	1	1	1	7	85.7Hz
1	0	0	0	8	75Hz

Table 6 - Valid Values of P

Bits 12 to 15 are used to produce the data word "P" as shown in the table at left. The cut-off frequency $f_{C/O}$ (0.5dB point) of the TX Sub-Audio Lowpass filter is calculated as:

$$f_{C/O} = \frac{f_{XTAL}}{32 \times 208.33 \times P}$$

$$\text{so } P = \frac{f_{XTAL}}{32 \times 208.33 \times f_{CO}}$$

Table 6 is given as an example and calculated using a Xtal/Clock (f_{XTAL}) frequency of 4.00MHz. As illustrated, only values of "P" of 2 to 8 are usable.

Controlling Protocol...

"Write to CTCSS TX Frequency/NRZ Baud Rate Register"...

Command Word "Q"

Bits 0 to 10 (see Figure 7) are used to produce the data word "Q" which sets one of the parameters described below. As you can see, Command Word "Q" could be used to produce a parameter outside that specified in the "Characteristics" section of this data bulletin. Care should be taken not to do this. Examples for limits of "Q" in each operational configuration are included. "Q" = 0 is not valid in the following calculations. Bit 11 is not used and must be set to logic "0."

(a) CTCSS TX Tone Frequency ($f_{CTCSS\ OUT}$)

$$f_{CTCSS\ OUT} = \frac{f_{XTAL}}{32 \times \text{"Q"}}\ \text{Hz}$$

$$\text{so "Q"} = \frac{f_{XTAL}}{32 \times f_{CTCSS\ OUT}}\ \text{Hz}$$

Example Limits

$f_{CTCSS\ OUT}$	=	67Hz	
so "Q"	=	1866	"11101001010"
$f_{CTCSS\ OUT}$	=	250Hz	
so "Q"	=	500	"00111110100"

(b) NRZ TX Baud Rate ($R_{NRZ\ TX}$)

$$R_{NRZ\ TX} = \frac{f_{XTAL}}{32 \times \text{"Q"}}\ \text{bits/sec.}$$

$$\text{so "Q"} = \frac{f_{XTAL}}{32 \times R_{NRZ\ TX}}$$

Example Limits

$R_{NRZ\ TX}$	=	67bits/sec.	
so "Q"	=	1866	"11101001010"
$R_{NRZ\ TX}$	=	300bits/sec.	
so "Q"	=	417	"00110100001"

(c) NRZ RX Baud Rate ($R_{NRZ\ RX}$)

$$R_{NRZ\ RX} = \frac{f_{XTAL}}{32 \times 11 \times \text{"Q"}}\ \text{bits/sec.}$$

$$\text{so "Q"} = \frac{f_{XTAL}}{352 \times R_{NRZ\ RX}}$$

Example Limits

$R_{NRZ\ RX}$	=	100bits/sec.	
so "Q"	=	114	"00001110010"
$R_{NRZ\ RX}$	=	300bits/sec.	
so "Q"	=	38	"00000100110"

Controlling Protocol...

"Read NRZ RX Data Register" -- A/C 74_H ($7C_H$), followed by 1 byte of Reply Data

Received NRZ data bits are organized into bytes and made available to the microcontroller via the Reply Data line. As 8 bits are received into this register an interrupt is generated to indicate that a complete byte has been received. This byte must be read before the arrival of the last (8th) bit of the next incoming byte. If this is not done, an interrupt to indicate this condition will be generated and the previous RX data is discarded. (See Table 4.)

Word synchronization is not provided. Byte synchronization and any codeword recognition will be performed by the host microcontroller. The RX baud rate is set by writing to the CTCSS TX Frequency/NRZ Baud Rate Register (73_H/$7B_H$). The first bit received is the first bit sent to the microcontroller.

This register is not affected by the General Reset Command (01_H), and may adopt any random configuration at Power-Up.

"Write to NRZ TX Data Register" -- A/C 75_H ($7D_H$), followed by 1 byte of Command Data

A byte for transmission is loaded from the C-BUS Command Data line with this A/C. The first data bit received via the C-BUS is transmitted first. This transmitter operation is non-inverting.

The first data byte loaded after the NRZ Encoder is enabled (Control Register) initiates the transmission sequence and an interrupt will be generated when the NRZ TX Data Buffer is ready for the next data byte. Subsequently, interrupts occur for every 8 bits transmitted.

Transmission is terminated, the TX Sub-Audio Output is placed at V_{BIAS}, and an interrupt is generated if the next byte is not loaded within 7 bit periods (see Table 4).

This register is not affected by the General Reset Command (01_H), and may adopt any random configuration at Power-Up.

"Write to Gain Set Register" -- A/C 76_H ($7E_H$), followed by 1 byte of Command Data

Setting				Gain Setting
MSB				
7	***6***	***5***	***4***	***Transmitted Bit 7 First***
0	0	0	0	These 4 bits must be "0"
			3	**Pre-Emphasis Setting**
			1	1.72dB Gain Enabled
			0	1.72dB Gain Disabled
		2	***1***	***0***	**TX Level Adjust Gain Setting**
		0	0	0	-2.58dB
		0	0	1	-1.72dB
		0	1	0	-0.86dB
		0	1	1	0dB
		1	0	0	+0.86dB
		1	0	1	+1.72dB
		1	1	0	+2.58dB
		1	1	1	Not Used

Table 7 - Gain Set Register Settings

The Gain Set Register Settings

The settings of this register control the CTCSS and NRZ signal level that is presented at the TX Sub-Audio Output.

Bit 3, when enabled, is used to produce a pre-emphasis effect on the NRZ TX Data by increasing the gain of the data bit before a level change (see Figure 8), by 1.72dB to make that data pulse level slightly more positive (or negative). The signal level will be 1.72dB greater than that set by Bits 0 to 2. If the TX Sub-Audio Output level is set to +2.58dB, the pre-emphasized level will be +4.3dB.

The pre-emphasis function will remain enabled until disabled by setting Bit 3 to a logic"0." If this function remains enabled when using the CTCSS Encoder, the output signal may be adversely affected. Therefore this function should only be enabled when in the NRZ Encode mode.

This register is not affected by the General Reset Command (01_H), and may adopt any random configuration at Power-Up.

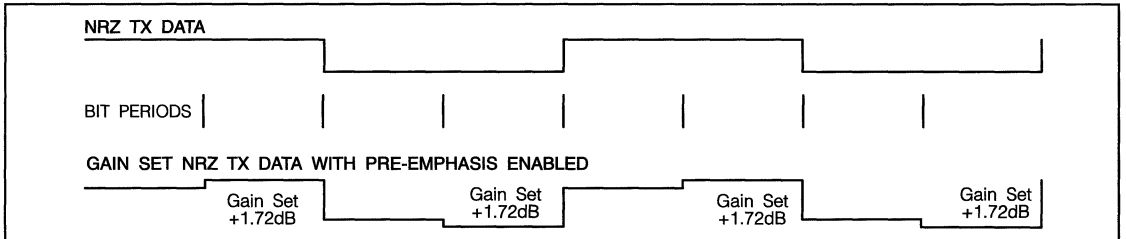


Figure 8 - Gain Set With Pre-Emphasis

Timing Information

Figure 9 shows the timing parameters for two-way communication between the µC and the MX805A on the C-BUS.

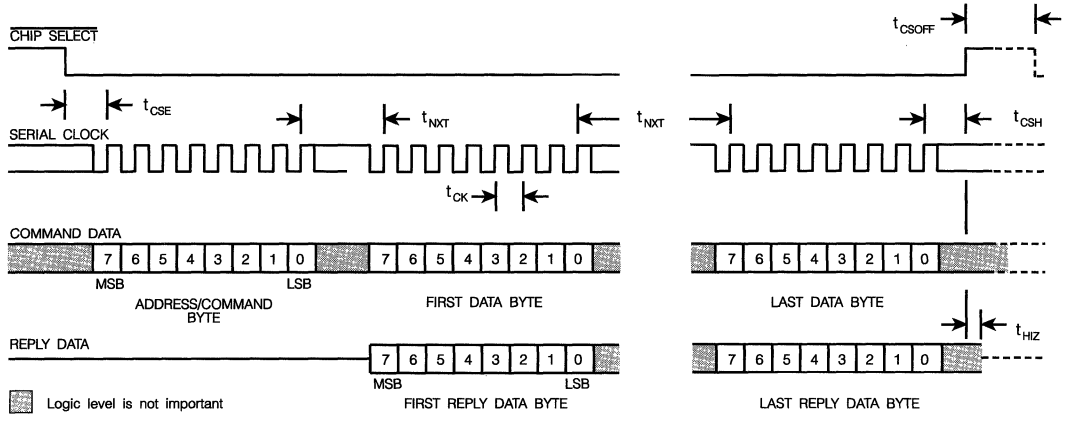


Figure 9 - C-BUS Timing

Parameter		Min.	Typ.	Max.	Unit
t_{CSE}	Chip Select Low to First Serial Clock Rising Edge	2.0	-	-	µs
t_{CSH}	Last Serial Clock Rising Edge to Chip Select High	4.0	-	-	µs
t_{CSOFF}	Chip Select High	2.0	-	-	µs
t_{NXT}	Command Data Inter-Byte Time	4.0	-	-	µs
t_{CK}	Serial Clock Period	2.0	-	-	µs
t_{CH}	Decoder or Encoder Clock High	500	-	-	ns
t_{CL}	Decoder or Encoder Clock Low	500	-	-	ns
t_{CDS}	Command Data Set-Up Time	250	-	-	ns
t_{CDH}	Command Data Hold Time	0	-	-	ns
t_{RDS}	Reply Data Set-Up Time	250	-	-	ns
t_{RDH}	Reply Data Hold Time	50.0	-	-	ns
t_{HIZ}	Chip Select High to Reply Data High - Z	-		2.0	µs

Notes: 1. Command Data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. Reply Data is read from the MX805A MSB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into the MX805A and into the microcontroller on the rising Serial Clock edge.
3. Loaded data instructions are acted upon at the end of each individual, loaded byte.
4. To allow for differing microcontroller serial interface formats, the MX805A will work with either polarity Serial Clock pulses.

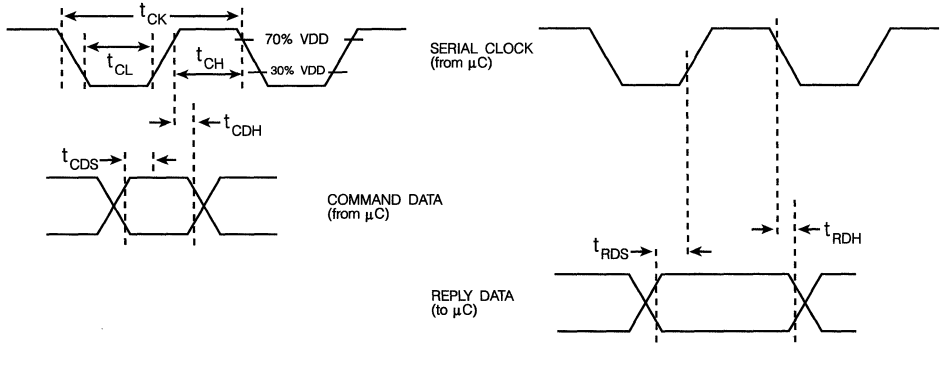


Figure 10 - Timing Relationships for C-BUS Information Transfer

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref. V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/Source Current	
(supply pins)	±30mA
(other pins)	±20mA
Total device dissipation @ T_{AMB} 25°C	800mW max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

XTAL/Clock frequency = 4.0MHz

Audio level 0dB ref. = 308mVrms @ 1kHz

Composite Signal = 308mVrms @ 1kHz +75mVrms Noise + 31mVrms Sub-Audio Signal

Noise Bandwidth = 5kHz Band Limited Gaussian

2

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current (All Functions Enabled)		-	5.0	7.0	mA
(Decoders only Enabled)		-	1.9	2.5	mA
(Powersave All)		-	0.9	1.5	mA
Analog Impedances					
RX Sub-Audio Input		350	-	-	kΩ
Audio Input		350	-	-	kΩ
Audio Bypass Switch On	5	-	2.0	-	kΩ
Audio Bypass Switch Off	5	1.0	10.0	-	MΩ
RX Amp Input (+ and -)		1.0	10.0	-	MΩ
Comparator Input (+ and -)		1.0	10.0	-	MΩ
RX Sub-Audio Output		-	2.0	-	kΩ
TX Sub-Audio Output (Encoder Enabled)	5	-	2.0	-	kΩ
(Encoder Disabled)	5	-	500	-	kΩ
Audio Output (Enabled)	5	-	2.0	-	kΩ
(Disabled)	5	-	500	-	kΩ
RX Amp and Comparator Outputs					
(Large Signal)		-	6.0	-	kΩ
(Small Signal)		-	600	-	Ω
Dynamic Values					
Digital Interface					
Input Logic "1"	1	3.5	-	-	V
Input logic "0"	1	-	-	1.5	V
Output Logic "1" (IOH = -120µA)	2	4.6	-	-	V
Output Logic "0" (IOL - 360µA)	3	-	-	0.4	V
I_{OUT} Tristate (Logic "1" or "0")	3	-	-	4.0	µA
Input Capacitance	1	-	-	7.5	pF
Logic Input Current (V_{IN} = 0 to 5.0V)	1	-	-	1.0	µA
IOX (V_{OUT} = 5.0V)	4	-	-	4.0	µA

Characteristics	See Note	Min.	Typ.	Max.	Unit
Overall Performance					
CTCSS - Decode					
Sensitivity (Pure CTCSS Tone)	6	-20	-26.0	-	dB
Response Time (Composite Signal)					
100 Hz to 257 Hz Tone		-	-	250	ms
65 Hz Tone	9	-	-	375	ms
Tone Measurement Resolution		-	0.2	-	%
Tone Measurement Accuracy		-0.5	-	+0.5	%
Notone Response Time (Composite Signal)	7	-	-	250	ms
False Tone Interrupts (Noise Input only)	10	-	20.0	-	/Hr.
CTCSS - Encode					
Frequency Range		65.0	-	257	Hz
Tone Frequency Resolution		-	-	0.2	%
Tone Amplitude Tolerance		-1.0	-	+1.0	dB
Rise Time (to 90%)		-	-	30.0	ms
Fall Time (to 10%)		-	-	50.0	ms
Total Harmonic Distortion		-	-	5.0	%
NRZ - Decode					
RX Bit Rate Sync Time		-	2	-	edges
RX Bit Error Rate	11	-	$1x10^{-3}$	-	$P_{(error)}$
NRZ - TX					
TX Bit Rate		67.0	-	300	bits/s
TX LPF (3dB) Bandwidth		75	-	300	Hz
Sub-Audio TX Output Level					
CTCSS		-	0	-	dB
NRZ		-	0.871	-	V p-p
Amplitude Adjustment Range		-2.58	-	2.58	dB
Adjustment Step Size (7 steps)	8	-	0.86	-	dB
Sub-Audio Bandstop Filter					
Passband		297	-	3000	Hz
Passband Gain		-	0	-	dB
Passband Gain (w.r.t. gain at 1.0 kHz)		-1.5	-	0.5	dB
Stopband Attenuation					
at 250 Hz		36.0	-	-	dB
at150 Hz		24.0	-	-	dB
at 100 Hz		18.0	-	-	dB
Residual Hum and Noise		-	-50.0	-45.7	dBp
Alias Frequency		-	-	62.5	kHz
Receive Lowpass Filter (see Figure 10)					
Cut-off Frequency (-3dB)		-	280	-	Hz
Passband Gain		-	6	-	dB

Characteristics		See Note	Min.	Typ.	Max.	Unit
Receive Lowpass Filter (cont'd)						
Stopband Attenuation	@ 300 Hz		-	6	-	dB
	@ 350 Hz		-	12	-	dB
Residual Hum and Noise			-	-50	-	dB
Xtal/Clock Frequency (f_{XTAL})			-	4.0	6.1	MHz

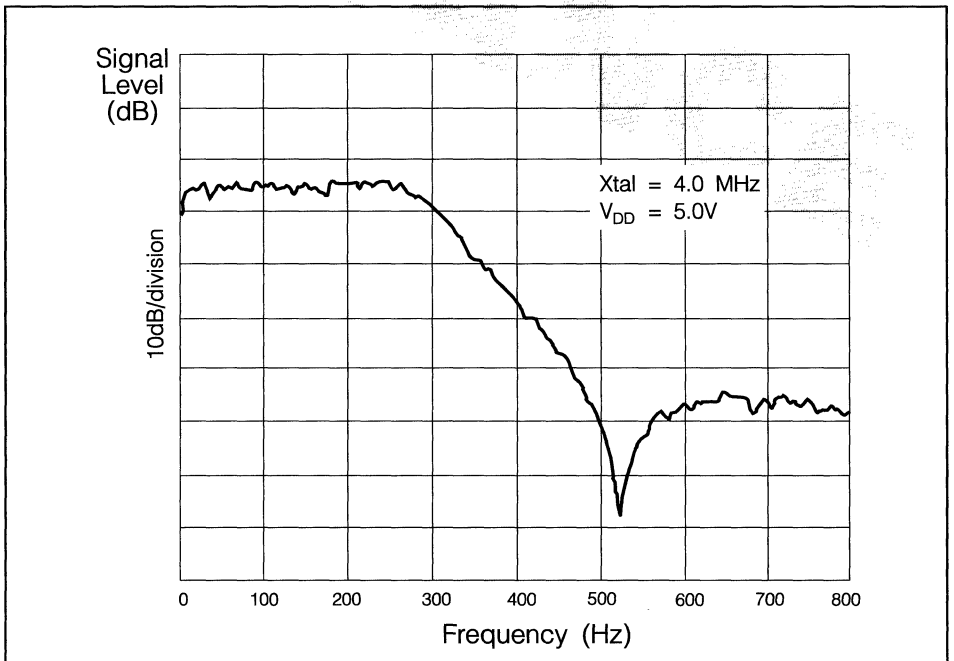


Figure 10 - Typical Frequency Response of RX Lowpass Filter

NOTES:

1. Device control pins: Serial Clock, Command Data, $\overline{\text{Wake}}$ and $\overline{\text{CS}}$.
2. Reply Data output.
3. Reply Data and $\overline{\text{IRQ}}$ outputs.
4. Leakage current into the "Off" $\overline{\text{IRQ}}$ output.
5. See Control Register
6. With input gain components set as recommended in Figure 2.
7. Probability 97%.
8. See Gain Set Register.
9. For $f_{CTCSSIN}$ of 65 Hz to 100 Hz, Response Time $t_R = (100/f_{TONE}) \times 250$ ms.
10. Distributed across the RX frequency band.
11. With 10dB signal-to-noise ratio in a bit-rate bandwidth.

Section 3: Sequential Tone Encoders/Decoders

The following section contains specifications on MX•COM's Sequentially Coded and Selective Call tone products

Device	Description	Page
MX013	HSC Tone Decoder	p. 229
MX203	Selective Call Codec	p. 234
MX503	Sequential Tone Encoder	p. 242
MX803A	Audio Signaling Processor	p. 249

HEXADECIMAL SEQUENTIAL CODE (HSC) SIGNALING SYSTEMS OVERVIEW

By William Farlow
MX-COM, INC.

INTRODUCTION

The Hexadecimal Sequential Code (HSC) is an MX•COM sequential tone signaling protocol which utilizes the non-predictive capabilities of the MX'03 series of monolithic tone processors.

HSC permits address codes, instruction codes and informational messages (data blocks) to be exchanged on an unrestricted basis between all units in a network. HSC provides the key to designing fully integrated base/mobile/personal communications supervisory control and data retrieval systems. The use of tone encoded information insures that signaling integrity is maintained under poor communications conditions — often conditions too poor for voice. HSC allows the transmission of messages and unit addresses without cross-code falsing. It allows different length addresses to be used within the same network. HSC also confers virtual immunity to noise or voice falsing while providing a high signaling probability. MX•COM's HSC products interface easily with microprocessors to minimize the required system hardware.

Subsets within the set of HSC tones are compatible with the frequencies and protocols used for a variety of international "5/6 tone sequential" selective signaling conventions. These national or international conventions dictate the use of specific tones, tone durations, etc. — each of which is accommodated by chip mask changes for some of our devices or software control in the case of the MX803A. Compliance with a particular national tone format merely requires selection of the desired component or microprocessor software.

Table 1: MX-COM HSC IC BUILDING BLOCKS[1]

* Suffix Code	National Tone Sets	MX013Q(*)	MX503(*)	MX203Q(*)	MX803A
A	Metropage U.S.A.	X	X	-	X
C	CCIR International	-	X	X	X
E	EEA United Kingdom	-	X	-	X
Z	ZVEI Germany	-	X	-	X
	HSC Function				
	ENCODE	-	X	X	X
	DECODE	X	-	X	X

[1] *Application Notes for the MX'03 HSC Series are available on request.*

The HSC concept provides two information level capacities, or data payloads: quadradecimal and hexadecimal. The part suffix "Q" represents a quadradecimal (14 information levels) system specifically structured around the needs of personal radio selective calling with an added data transfer capability. Selective calling uses an ID much like a telephone number to allow selective radio-to-radio addressing. In this quadradecimal system some HSC characters are reserved for system control purposes to provide group calls, multiple audible alert patterns, mixed address lengths, and the transmission of data blocks. A hexadecimal set, possible with the MX503 or MX803A, affords a full 16 level data transmission capability, providing a reliable means for transferring 4-bit data between microprocessors over a noisy channel. System control, for other than pure data transmission purposes, is then dependent upon the processor's programming. With a hexadecimal tone set, a seventeenth tone is then required for the REPEAT function.

GENERAL DESCRIPTION

This application note describes the coding rules and tone parameters used for quadradecimal HSC tone sets. Data bulletins for each of the MX'03 Series products are included in this catalog. A closed code protocol (i.e. no tone separation) is employed, in which each sequence of information characters is preceded and terminated by a "boundary" character. A particular boundary character initiates signal activity and directs the type of processing to be performed on the characters that follow. Two process modes are allowed — one which uses unit address information of finite length

and another which simply has informational messages (data blocks) of any length.

Within the finite address mode are found several special function capabilities. These are: a) group-call and all-call codes which may be programmed to output a distinctive audible alerting sound, b) primary and secondary addresses with distinct audible sounds, and c) a special function suffix code that inhibits the audible output entirely while erasing any call message previously stored in memory. Further, signaling compatibility with systems employing a "preamble tone" is provided.

Beyond mere compatibility with six tone signaling, HSC affords a flexible means of achieving battery saving independent of the preamble tone method. This is accomplished by using the data block suffix capability in a manner that directs variable length dormancy periods. The length of the dormancy period is controlled by the dispatch control center. Thus a receiver or group of receivers might be commanded into a battery saving state for several seconds, minutes or overnight. During a dormancy period the only current drain requirement would be for a timing circuit. The receiver's active duty cycle can then be reduced to just a few milliseconds at appointed times separated by lengthy quiescent intervals - the length of which may be dictated by the user's type of service, duty roster assignment, system traffic loading, etc.

The combination of address and data processing modes permits HSC units to be selectively addressed, and an informational message appended. An example might be the transmission of a phone number to a pager equipped with a digital display. The subscriber's paging address may be followed by a phone number that he or she is to call. The "air time" consumed in the transmission of such a message varies with the tone durations specified by different national protocols.

In the U.S. "Metropage"[1] convention the entire transmission comprising a five-digit discrete address and seven digit phone number consumes less than 1/2 second. This, of course, contrasts quite favorably with the air time used for an equivalent tone and voice message which typically lasts several seconds.

Another example, using an address followed by control data and also a voice message, could be a taxicab dispatching system where the dispatcher sends an address or instructions to a specified cab driver. The message could be directed to a voice storage and retrieval system based the MX802 or MX812.

International 5/6 Tone Sequential Signaling Conventions

Four national 5/6 tone sequential selective signalling tone sets are currently offered: The international Telecommunications Union's CCIR recommendation, the United Kingdom's EEA standard, the German ZVEI standard, and in the U.S.A., a de facto standard employed by the Bell System and Radio Common Carriers compatible with Motorola's Metropage terminal. These tone sets are described in the tables that follow.

Table 2: Nominal Tone Frequencies (in Hertz)

Character	Binary code	Metropage	CCIR	EEA	ZVEI
0	0 0 0 0	600	1981	1981	2400
1	0 0 0 1	741	1124	1124	1060
2	0 0 1 0	882	1197	1197	1160
3	0 0 1 1	1023	1275	1275	1270
4	0 1 0 0	1164	1358	1358	1400
5	0 1 0 1	1305	1446	1446	1530
6	0 1 1 0	1446	1540	1540	1670
7	0 1 1 1	1587	1640	1640	1830
8	1 0 0 0	1728	1747	1747	2000
9	1 0 0 1	1869	1860	1860	2200
A	1 0 1 0	2151	2400	1055	2800
B	1 0 1 1	2435	930	930	810
C[2]	1 1 0 0	2007	2247	2247	970
D	1 1 0 1	2295	991	991	886
E	1 1 1 0	459	2110	2110	2600
F	1 1 1 1	NOTONE	NOTONE	NOTONE	NOTONE

[1]Metropage is a registered trademark of Motorola, Inc.
[2]Note: HSC tones not specified by national convention.

Table 3: Encoder Requirements

Parameter	Metropage	CCIR	EEA	ZVEI
Tolerance	f_0 ±0.1%	f_0 ±8Hz	f_0 ±1%	f_0 ±1.5%
Duration	33 ±0.5ms	100 ±10ms	40 ±4ms	70 ±15ms
Maximum Inter-tone Gap	none	7.5ms	4ms	15ms
Minimum Inter-sequence Gap	33ms	290ms	100ms	140ms

Table 4: Decoder Requirements

Parameter	Metropage	CCIR	EEA	ZVEI
Must Decode	f_0 ±16Hz	f_0 ±1%	f_0 ±1%	f_0 ±2%
Must Not Decode	not specified	f_0 ±3%	f_0 ±3%	f_0 ±4.5%

HSC CHARACTER SET

In the system with a quadradecimal data capacity (part number suffix "Q") sixteen characters (four binary line levels) are employed. Fifteen of these characters have unique tone coded frequencies; the sixteenth character, the hexadecimal "F," is the code assigned to the NOTONE state. The NOTONE "F" code and two of the fifteen tone coded frequencies, the hexadecimal "B" and "E," are reserved for system control purposes. Alternate use of "B" (when it is contained within an established data block) creates the code for a hyphen (or optionally a character blank), thus yielding fourteen usable data codes. The quadradecimal four line binary code assignments follow industry practice.

HSC BUILDING BLOCKS: THE MX-03 SERIES

The functional blocks of the HSC system are enumerated and briefly described below. Operation is collectively governed by a set of HSC Operating Rules which are presented in the next section.

MX013Q* Sequential Tone Receiver: A twenty-four pin PLCC on 0.6 inch centers requires an external 560kHz ceramic resonator. Performs the system A to D function, decoding tones to output 4-bit binary words.

MX503* Sequential Tone Transmitter: A sixteen pin DIP generates all hexadecimal and quadradecimal frequencies for tone coding in any one of the four national sequential tone signaling formats according to HSC rules.

MX203Q* HSC Encoder/Decoder: A twenty-four pin PLCC or DIP full duplex HSC device for the CCIR International tone set. Operates under microprocessor control via a 4-bit I/O data port.

MX803A Audio Signalling Processor: A twenty-four pin PLCC or DIP full duplex device capable of working in any standard or custom tone system through serial microprocessor control of the tone set, timing, etc. The MX803A is the most flexible member of our HSC product family.

HSC SYSTEM OPERATING RULES

Transmit: Tones are transmitted as individual single frequencies, without inter-tone gaps, until the code sequence is complete. Where an inter-tone gap is unavoidable, the gap duration should not exceed 15ms.

Each consecutive tone in a transmission must be of a different frequency. Where consecutive characters are identical a dedicated "REPEAT" character (E) should be substituted automatically.

Consecutively transmitted addresses or data blocks are separated by an interval during which no tones are transmitted. This interval should not be less than 28ms.

Receive: HSC Tone Receivers process all valid single tone coded characters (from the HSC tone sets of the appropriate national convention) without regard for their sequence. To be valid, a character's tone frequency must fall within the band limits established for the national tone set. Further, the tone's duration must be at least 25ms. The presence of an invalid tone frequency at the input to an HSC tone receiver yields a NOTONE output code. This resets the address decoder or transponder software, as the case may be.

Group Calling: To effect a group or all call, the tone code character "A" is substituted as an address digit. "A" represents all digit values "0 through 9." In a system employing 5-digit addresses, an "A" encoded once

in an address will signal a group of ten units. Two "A" entries increases the group size to 100. Three "A" entries yields 1000 units in a group; four yields 10,000; and, five yields 100,000. The latter comprises an all call (in a five-digit address system). Sample group calls and an all-call are listed below:

Table 5: Group Call Example

5-Digit Address	Entry	Addresses Responding
1 2 3 4 A	(10 Units)	12340 thru 12349
1 2 3 A 5	(10 Units)	12305, 12315, 12325, ... , 12395
1 2 3 A A	(100 Units)	12300 thru 12399
A A A A A	(100K Units)	00000 thru 99999

Note that according to HSC rules, repeated characters are automatically transmitted as an "E." Thus, the actual transmission of the above all call example would be "AEAEA."

3

Preamble Tone Operation: A preamble tone is used as one method of reducing the continuous battery drain of pagers in some systems. It may also be used as a repeater wake-up tone. But, it can also offer a means of expanding a system's code capacity. When the preamble mode is selected each address decoder should be assigned a tone code that it must first detect in order to enable normal 1 to 5 digit decoding. A Preamble Tone must be transmitted for slightly longer than the device power-down time to ensure that the receiver will enable when it "awakens." If an address decoder's assigned preamble tone is not detected on power up the unit can power down immediately for a preset period of time. The addition of an external timer that periodically powers up the unit is assumed. The NOTONE "F" detected between the preamble digit and the first digit of the address should, in this case, be accepted without resetting the address decoder. Systems that do not need the extra capacity can use the first digit of the address as the preamble tone.

Examples of preamble tone operation follow. In these examples a receiver is assumed to have the digit "6" as preamble/enable with an address "12345."

Table 6: Preamble Tone Example

Address Received	Does Receiver Respond?
F6F12345F	YES
F7F12345F	NO (different preamble)
F6F1234F	NO (different address)

Tone Period Envelope Restriction: Some national tone signalling protocols impose limits on tone or address envelope duration greater than those required for HSC operation. These timing restrictions can be handled in software with the aid of on-chip timers on the MX803A and MX203Q(*), while external timing is required for the MX503(*) and MX013Q(*).

Data Mode Operation: Data mode operation commences upon receipt of the assigned DATA PREFIX code "B," following either a valid address or the, NOTONE code. The "B" code serves both to inhibit address mode operation and to initiate the data mode. All characters in a data block up to a NOTONE code can thus be processed as data including characters/tones normally reserved for system control purposes.

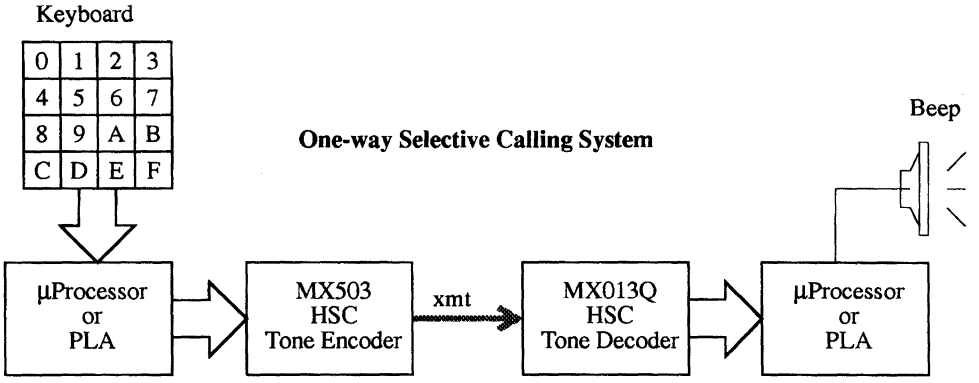
Crosscode Falsing: The prevention of crosscode falsing of non-HSC capable receivers by the transmission of HSC data blocks to MX•COM receivers may require special attention. First, the code reset means of the non-HSC receivers must be considered. Generally this is a time dependent control in which each succeeding digit must be detected within a minimum period. If the minimum period is known, it is a simple matter to sustain an HSC special function character, typically "B," for the reset interval of any non-HSC units. Crosscode falsing is prevented because non-HSC receivers detect the special function HSC tones as tone-gaps. Insertion of an HSC special function character may be required only once, or, if the data sequence is lengthy, at periodic intervals. A phone number is an example of a transmission in which the data prefix "B" will typically

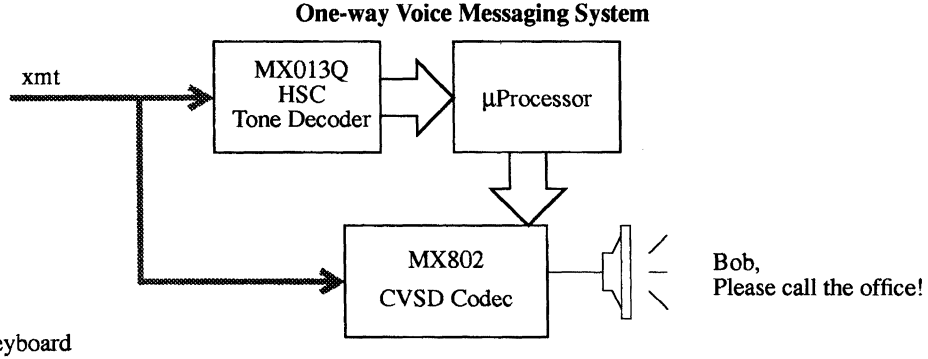
be followed by 7 to 10 decimal digits. To prevent these digits from being decoded as paging addresses by non-HSC receivers, the "B" code should be entered as a tone-gap at additional points to induce reset before a cross coded error results. For example, the phone number 7480505 could be transmitted as 748B0505. Within a data block "B" may optionally be treated as a character blank, hyphen, or simply discarded by the HSC receiver.

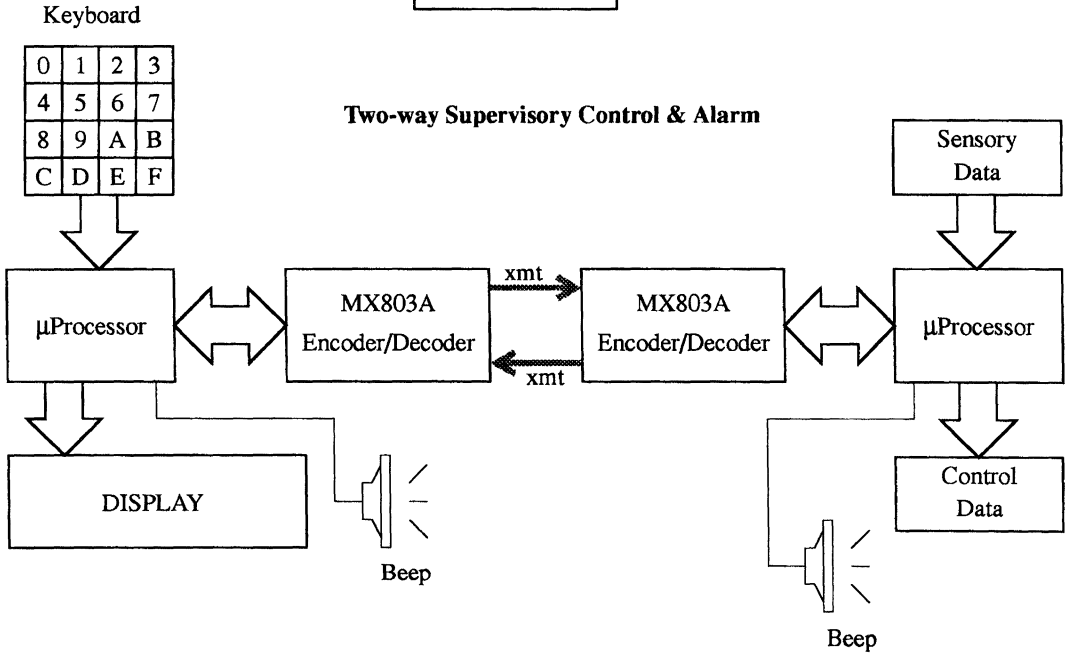
Transpond Mode Operation: Transponding serves an echo function that acknowledges receipt of discrete unit calls and serves polled status report data gathering applications.

Automatic Number Identification (ANI): ANI serves the function of identifying the caller's ID and can easily be implemented within the HSC framework using the data payload portion of a tone sequence.

*note: Add suffix letter codes for national tone set designation as follows: A=Metropage, C=CCIR, E=EEA, Z=ZVEI. This only applies to MX013, MX203, and MX503.


Keyboard
0 1 2 3
4 5 6 7
8 9 A B
C D E F
One-way Selective Calling System
Beep
µProcessor or PLA
MX503 HSC Tone Encoder
xmt
MX013Q HSC Tone Decoder
µProcessor or PLA

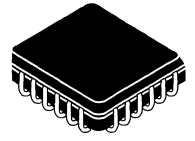

One-way Voice Messaging System
xmt
MX013Q HSC Tone Decoder
µProcessor
MX802 CVSD Codec
Bob,
Please call the office!


Keyboard
0 1 2 3
4 5 6 7
8 9 A B
C D E F
Two-way Supervisory Control & Alarm
Sensory Data
µProcessor
MX803A Encoder/Decoder
xmt
xmt
MX803A Encoder/Decoder
µProcessor
DISPLAY
Beep
Control Data
Beep

HSC TONE DECODER

FEATURES

- **Operates on 2.5 V Supply**
- **Low Current Drain**
- **USA METRO Toneset**
- **Chip Enable, Clock Frequency Select and Interrupt Request Pin Functions**



MX013QALH
PLCC-24

APPLICATIONS

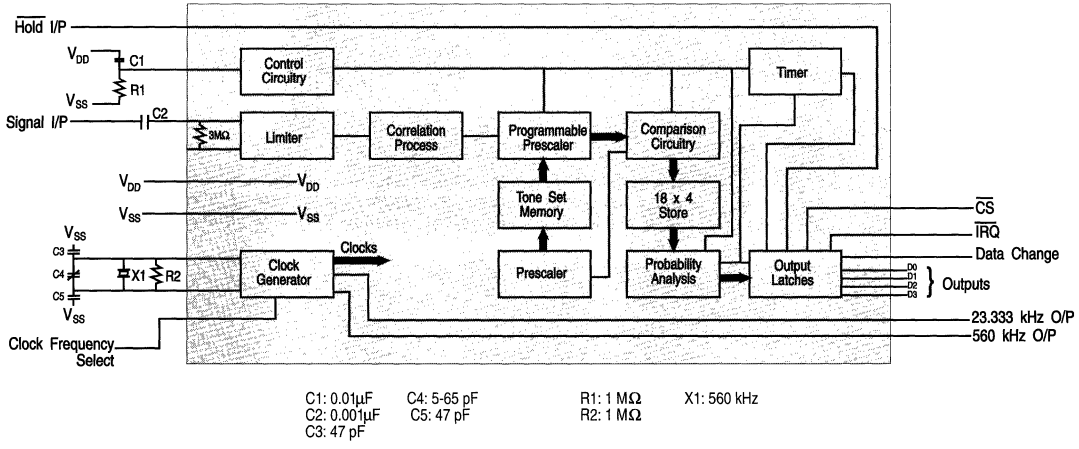
- **Pagers**
- **Mobile Radio Selective Call**
- **Remote Signaling**

Description

The MX013QALH HSC Tone Decoder combines the functions of the MX102LH and MX202QALH into a single PLCC package. To the circuit designer, the MX013 offers a smaller device "footprint", reduced power and current requirements, and a lower device cost. The MX013's patented autocorrelation algorithm ensures high signaling reliability in noisy environments.

The MX013 operates within a 2.5V to 5.5V supply voltage range and draws approximately half the current of the older MX003 design. It is available exclusively in a 24-pin PLCC package.

Three new pin selectable functions are incorporated on the MX013 : Chip Enable, Clock Frequency Select and Interrupt Request.



C1: 0.01µF C4: 5-65 pF R1: 1 MΩ X1: 560 kHz
C2: 0.001µF C5: 47 pF R2: 1 MΩ
C3: 47 pF

Figure 1 - External Components

PIN FUNCTION CHART

Pin	Function
3	**Signal Input**: HSC tones are AC coupled to this pin by a 1000pF capacitor. DC bias of the internal high gain limiter is set up by an internal 3 MΩ bias resistor connected between this pin and the signal bias pin. These pins should not be loaded with any other circuitry.
5	**Signal Bias**: See signal input.
7	**23.33 kHz Clock O/P**: A 23.333 kHz buffered squarewave logic output directly derived from the oscillator frequency (nominally 560.0 kHz). This pin may be used for auxiliary functions, e.g. external timing of received tone periods and for other '03 series devices.
8	**$\overline{\text{Xtal}}$:** Output from on-chip inverter (See Xtal/Clock).
9	**Xtal/Clock:** Input to on-chip inverter. May be used in conjunction with Xtal O/P and a 560 kHz ceramic resonator and trimming capacitor or a 4.48 MHz quartz crystal and fixed passive components. May also be used as a buffered input to an externally derived 560.0 kHz or 4.48 MHz clock.
10	**560 kHz buffered O/P:** A buffered 560 kHz signal is output from this pin.
11	**Clock Frequency Select:** This pin is normally at logic "1" if a 560 kHz resonator is being used. If held at logic "0," a divide by 8 is switched in after the oscillator circuit to divide down the 4.48 MHz frequency to 560 KHz. This pin has a 1 MΩ pullup.
12	**V_{SS}:** Negative Supply (GND).
13	**$\overline{\text{Hold}}$ I/P**: If taken to V_{SS} and a tone is input, the resulting Data Change output latches to logic "1" and the Data lines output the code for the detected tone regardless of subsequent changes to the input tone, until Hold is returned to V_{DD}. This facilitates Interrupt/Handshake routines for microprocessors when used in conjunction with the Data change O/P. This pin has a 1 MΩ pullup.
14	**Power-up Reset:** A logic level "1" is required at this pin for a duration of at least 1 ms after clock is applied to reset internal circuitry on power-up. For slow rising supplies the recommended time constant should be increased accordingly.
15	**$\overline{\text{IRQ}}$:** $\overline{\text{Interrupt Request}}$, an output, is latched to logic "0" when a tone is detected and the $\overline{\text{CS}}$ pin is at V_{DD}, i.e. chip disabled. This pin is reset to logic "1," enabling is for use in wire-OR-ing with similar outputs from other peripherals.
16	**$\overline{\text{CS}}$:** $\overline{\text{Chip Select}}$. When this pin is taken to V_{DD}, the chip is disabled and the data outputs Q0-Q3 and Data Change output go open circuit. When taken to V_{SS} the chip is enabled and the $\overline{\text{IRQ}}$ output is reset to logic "1."
17	**Data Change:** A 1 ms pulse is generated at this pin upon detection of a valid tone and new data is presented to the Q0-Q3 outputs. The signal from this pin can be latched at a logic "1" after detection of a tone (see $\overline{\text{Hold}}$ input). This output is tri-state.
19	Q3 Data Outputs: A 4-bit word is output from these pins
20	Q2 after successful decode and represents
22	Q1 the HEX value of the decoded tone
23	Q0 frequency. These outputs are tri-state.
24	**V_{DD}:** Positive Supply

1,2,4,6,18,21: Unused pins.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 V to V_{DD} + 0.3 V
Sink/Source Current (Total)	20mA
Total Device Dissipation @ T_{AMB} = 25°C	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.

V_{DD}=5.0V

T_{AMB}=25°C

Xtal/Clock f_0 = 560 kHz

Characteristics are valid for all tones unless otherwise stated.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{SS}=0V)		2.5	-	5.5	V
Supply Current		-	500	-	µA
Logic "1" Output					
1 Source = 1 mA		4.5	-	-	V
Logic "0" Output					
1 Sink = 1 mA		-	-	0.5	V
Logic "1" Input Level is 3.5 V min.					
Logic "0" Input Level is 1.5 V max.					
Dynamic Values					
Signal Input Range	1	35	-	V_{DD}/2	mVrms
Decode Bandwidth when P>0.995	2	±20	-	-	Hz
Not-Decode Bandwidth when P<0.03	3	-	-	±60	Hz
Noise Response Rate (hours per F - F - F single character response with no input tone).	4	-	0.15	-	hour
Decode Response Time:					
Notone to tone (F - F)	5	20	25	33	ms
Tone to notone, Tf (F - F)	5	33	-	53	ms
Min. intertone gap for "F"	6	15	-	28	ms

Notes:

1) A.C. coupled sine/squarewave.
2) With minimum tone period (Tp) specified for toneset. P = Decode Probability. SNR = 3dB.
3) All conditions of input SNR and amplitude with maximum Tp specified for toneset.
4) Gaussian input noise, bandwidth 6 kHz, maximum input level corresponds to 1-digit code falsing rate. F=random single character.
5) Delay from change of input (tone applied/removed) to change at Q0-Q3 outputs (see Figure 2).
6) Included in t_{NT}. Minimum tone gap requirement for "notone" recognition. Outputs = F after delay (see Figure 2).

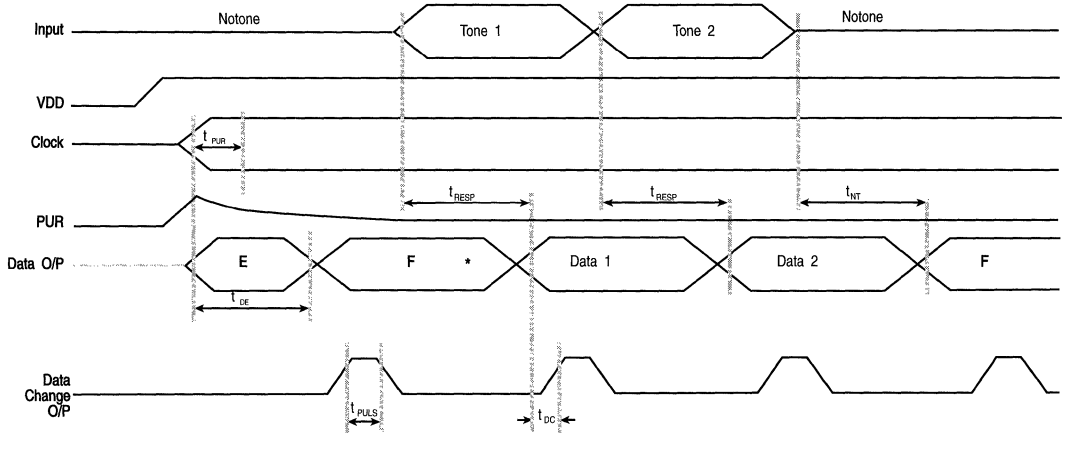
MX013QALH Tone Table

Input Tone Frequency (f_0 in Hz) MX013QA	Binary Coded Output D3	D2	D1	D0	Quadradecimal Data Character
600	0	0	0	0	0
741	0	0	0	1	1
882	0	0	1	0	2
1023	0	0	1	1	3
1164	0	1	0	0	4
1305	0	1	0	1	5
1446	0	1	1	0	6
1587	0	1	1	1	7
1728	1	0	0	0	8
1869	1	0	0	1	9
2151	1	0	1	0	A
2435	1	0	1	1	B
2007	1	1	0	0	C
2295	1	1	0	1	D
459	1	1	1	0	E
NOTONE	1	1	1	1	F

Table 1 - MX013 Tone Table

3

Timing



* 00-03 represents the input frequency present during and after PUR [shown as F (Notone)] in this example

t_{PUR} (PUR Time): 2 ms Min.

t_{DE} (Data "E" Time): 33 ms Typ.

t_{PULS} (DC Pulse Duration): 1 ms Typ.

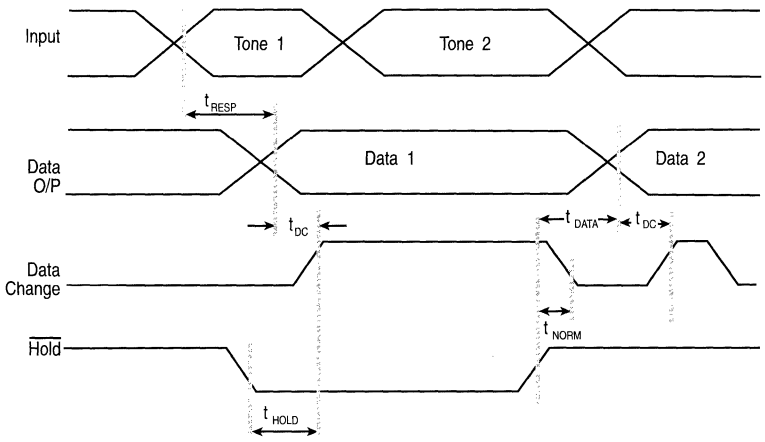
t_{DC} (Data to DC Pulse Time): .5 ms Min., 1 ms Max.

t_{RESP} (Tone Response Time): 20 ms Min., 33 ms Max.

t_{NT} (Notone Response Time): 33 ms Min., 53 ms Max.

Figure 2 - Normal Timing Operation (not drawn to scale)

Timing



t_{RESP} : 20 ms Min., 33 ms Max.

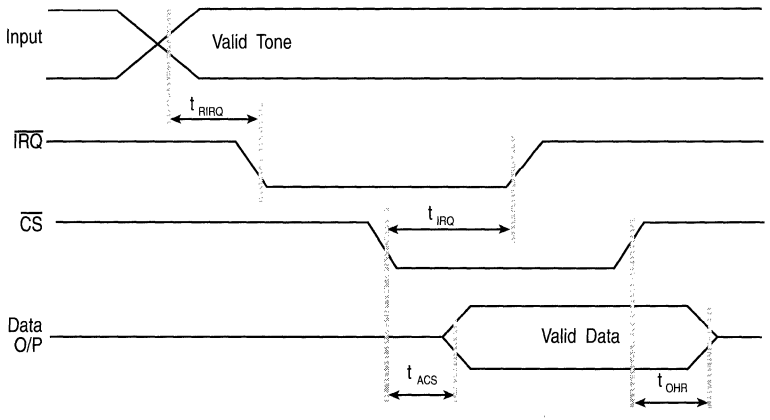
t_{DATA} : 2 ms Max.

t_{DC} : .5 ms Min., 1 ms Max.

t_{NORM}: 120 µs Max.

t_{HOLD} : 50 µs Min.

Figure 3 - $\overline{HOLD}$ Operation (not drawn to scale)



t_{RIRQ} : 20.5 ms Min., 34 ms Max.

t_{IRQ} : 10 µs Max. (reduced if an external pullup is used)

t_{ACS} : 250 ns Max.

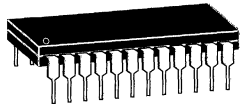
t_{OHR} : 100 ns Max.

Figure 4 - $\overline{CS}$ and $\overline{IRQ}$ Operation (not drawn to scale)

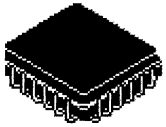
HSC ENCODER/DECODER

FEATURES

- **HSC (5-tone) Encoding/Decoding**
- **CCIR, EEA or ZVEI/SZVEI Tonesets**
- **Separate General Purpose 4-bit Input/2-bit Output port**
- **Mobile or Handheld SelCall**
- **4-bit Microprocessor I/O Data Port**
- **Powersave Ability**
- **Low-Power 5-volt CMOS**



MX203Q*J
24-pin CDIP



MX203Q*LH
24-pin PLCC

3

Description

The MX203Q* HSC Encoder/Decoder is a µP peripheral intended for radio-selective calling systems. Three international tone sets are supported: CCIR (C), EEA (E) or ZVEI/SZVEI (Z), as indicated by a letter suffix.

A 4-bit bi-directional data bus provides 2-bit address, chip select, read/write and interrupt request to the µP. Separate 4-bit input and 2-bit output ports allow µP access by external keyboards or hexadecimal switches through the MX203. Functions such as PTT, RX Squelch, Beepalerts and Lamp Drivers can operate through this bus.

An on-chip General Purpose Timer is provided for such functions as RX and TX tone period timing. Time periods of between 10ms and 140 ms may be programmed in 10 ms steps by the µP interface.

The MX203 reference oscillator uses a low cost 4.0 MHz xtal or externally derived clock. The divide by 4 (1.0 MHz) output may be used to drive the clock circuitry of other devices such as the MX365A CTCSS Encoder/Decoder, MX004 Voice Band Inverter, or the MX214 VSB Audio Scrambler.

The MX203 requires a single 5V supply and utilizes Chip Enable and Powersave functions for reduced current usage in the Standby mode. It is available in 24-pin PLCC and CDIP packages.

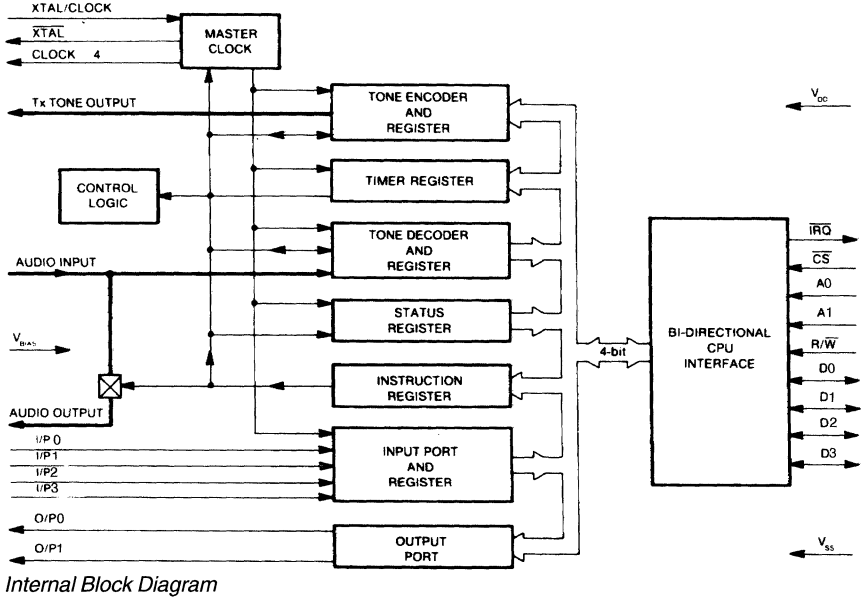


Figure 1 - Internal Block Diagram

(*) specify CCIR (C), EEA (E) or ZVEI/SZVEI (Z) tonesets.

PIN FUNCTION CHART

Pin	Function
1	V_{DD}: Positive Supply
2	Audio Output: The received audio output, selected by the Audio Output Enable bit, D1, in the instruction Register. This output could be the result of a squelch function.
3	Audio Input: The audio input to the Tone Decoder and audio output switching. The composite (voice and tone) received audio requires coupling to this pin by capacitor C3. See Figures 1 and 2.
4	V_{SS}: Negative supply (GND).
5	Xtal/Clock: Input to clock oscillator inverter. A 4.0 MHz xtal or externally derived clock pulse input should be connected here. See Figure 2.
6	$\overline{\text{Xtal}}$: The output of the 4.0 MHz clock oscillator. See Figure 2.
7	Clock÷4: a 1.0 MHz (X1÷4) clock is available at this output for external use. Note the output impedance and source current limits.
8	$\overline{\text{CS}}$: Chip Select. The chip select input. A logic "0" on this pin will select the MX203. See Figure 3.
9	$\overline{\text{IRQ}}$: The interrupt logic output. An active interrupt is set as a logic "0." This pin can be wire-OR-ed to external circuitry. An external pullup resistor may be required on this output. Conditions that cause Interrupt Requests are: 1) RX Ready (tone decoded) $\overline{\text{IRQ}}$ and Status bit D0 2) Timer cycle expired $\overline{\text{IRQ}}$ and Status bit D1 3) Input Port data change $\overline{\text{IRQ}}$ and Status bit D2
10 11	A0: A1: Register address pins. These inputs, together with the R/$\overline{\text{W}}$ input, select the internal register to be addressed by the CPU Interface (D0-D3) using the logic states as detailed below. Register information is detailed in the following pages.
12 13 14 15	D0 D1 D2 D3 The tri-state 4-bit microprocessor interface for communication with the internal registers as directed by the A0, A1 and R/$\overline{\text{W}}$ inputs.

	R/$\overline{\text{W}}$	A1	A0	Register
	0	0	0	Tone Encode
Write	0	0	1	Instruction
	0	1	0	Timer
	1	0	0	Tone Decode
Read	1	0	1	Status
	1	1	0	Input Port

Pin	Function
16	R/$\overline{W}$: The Read/Write logic. which with the A_0 and A_1 address inputs determines the Microprocessor/ Register communication. Read = logic "1", Write = logic "0".
17	TX Tone Output: The transmitted tone output of the Tone Encoder. Tone "0" (Notone) will cause this output to go to V_{BIAS}. When not enabled this output is high impedance.
18	V_{BIAS}: The output of the on-chip bias circuitry, held at $V_{DD}/2$. When the Encoder is not enabled this pin will be at V_{SS}. This pin requires decoupling to V_{SS} with a capacitor, C4.
19	O/P_0: The 2-bit logic output port whose state is controlled by the
20	O/P_1: Instruction Register (D_2, D_3).
21	I/P_0: The 4-bit logic input
22	I/P_1: port. (See Figure 2.)
23	I/P_2: These pins each have an internal
24	I/P_3: 1 MΩ pullup resistor.

3

General and Operational Notes

Power-up Arrangements

It is recommended that the following sequence is used to set all internal registers to a start-up state upon power-up.

Write - Hex "0" to Timer Register for a period greater than Power-Up Reset Time (TS).

The following actions clear the Status Register and reset all interrupts.

Read - Status Register.
Read - Input Port Register.
Write - To Output Port as required.

The data in the Decoder Register is not valid until after the first active Decoder interrupt has been received.

Operation

Operation of the MX203 is Full Duplex. The receive mode is achieved by writing any Timer setting except Hex "0."

The Tone Decode Register must be read before the expected arrival of the next tone, as register contents are overwritten.

Data written to the device by the CPU Interface is acted upon at the end of the Data Set-up Time (t_{DSW}), when the $\overline{CS}$ input goes high (logic "1").

The Timer may be written to at any time. The Timer is reset when data is written to it. The new Timer period starts when the $\overline{CS}$ input goes high (logic "1").

Layout

All external components (as recommended in Figure 2) should be kept close to the package.

Tracks should be kept short, particularly the Audio and V_{SS} inputs.

Xtal/clock and digital tracks should be kept away from analog circuitry. Analog inputs and outputs should be screened whenever possible, and high level TX Tone Output kept separate from other analog inputs and outputs.

A "ground plane" connected to V_{SS} will assist in eliminating external pick-up.

External Register States

The following descriptions show the condition of each of the 6 registers used by the MX203 to communicate with microprocessor and radio systems. Table 1 details the hexadecimal 4-bit data words used in these registers. Timing information for the CPU Interface is given in Figure 3.

Instruction Register — Write Only — $R/\overline{W} = 0, A_1 = 0, A_0 = 1$

The Instruction Register addresses the functions of the MX203

Bit No	Logic	Function	
D_0	1	Tx Enable:	Enables the Transmitter circuitry
	0		Disables the Transmitter circuitry
D_1	1	Audio Output Enable:	Switches from Audio Input to Audio Output
	0		Disables the Audio Output Switch (S1)
D_2	1 or 0	Output Port O/P_0:	The logic state of this line
D_3	1 or 0	Output Port O/P_1:	The logic state of this line

Tone Encode Register — Write Only — $R/\overline{W} = 0, A_1 = 0, A_0 = 0$

D_0 D_1 D_2 D_3

LSB MSB

The 4-bit Hex. word written to this register will produce the required tone (Table 1) at the TX Tone Output.

Tone Decode Register — Read Only — $R/\overline{W} = 1, A_1 = 0, A_0 = 0$

D_0 D_1 D_2 D_3

LSB MSB

The 4-bit Hex. word in this register will indicate the frequency (Table 1) of the received tone.

Timer Register — Write Only — $R/\overline{W} = 0, A_1 = 1, A_0 = 0$

D_0 D_1 D_2 D_3

LSB MSB

The 4-bit Hex. word written to this register wili automatically reset the timer and start a timing cycle as shown:

Hex Code	Function/Tone Period
0	Disable Receiver, Transmitter and Timer
	Reset and start tone period of:
1	10ms
2	20ms
3	30ms
4	40ms
5	50ms
6	60ms
7	70ms
8	80ms
9	90ms
A	100ms
B	110ms
C	120ms
D	130ms
E	140ms
F	Disable Timer Operation Only

Status Register — Read Only — $R/\overline{W} = 1, A_1 = 0, A_0 = 1$

The Status Register indicates the source of any interrupt.

Bit No. Condition [A logic "1" in the Status Register indicates that the bit is Set. The Interrupt line (IRQ) is a logic "0" when active.]

D0 Rx Ready:
D0 and an interrupt are Set when the Tone Decoder has decoded a received tone and latched the 4-bit Hex. word into the tone Deocde Register. This register must be read before the next tone is decoded or the information will be overwritten.
D and the interrupt are Cleared by reading the Status Register followed by reading the Tone Decode Register.

D1 Timer:
D1 and an interrupt are Set when the intervals programmed by the Timer Register have expired. D1 and the interrupt are Cleared after reading the Status Register.

D2 Input Port (I/P_0 - I/P_3):
D and an interrupt are Set when the data state at the Input Port changes. D., and the interrupt are Cleared by reading the Status Register followed by reading the Input Port Register.

D3 This bit is unallocated. Set at logic "0."

Input Port — Read Only — $R/\overline{W} = 1, A_1 = 1, A_0 = 0$

D_0 D_1 D_2 D_3

LSB MSB

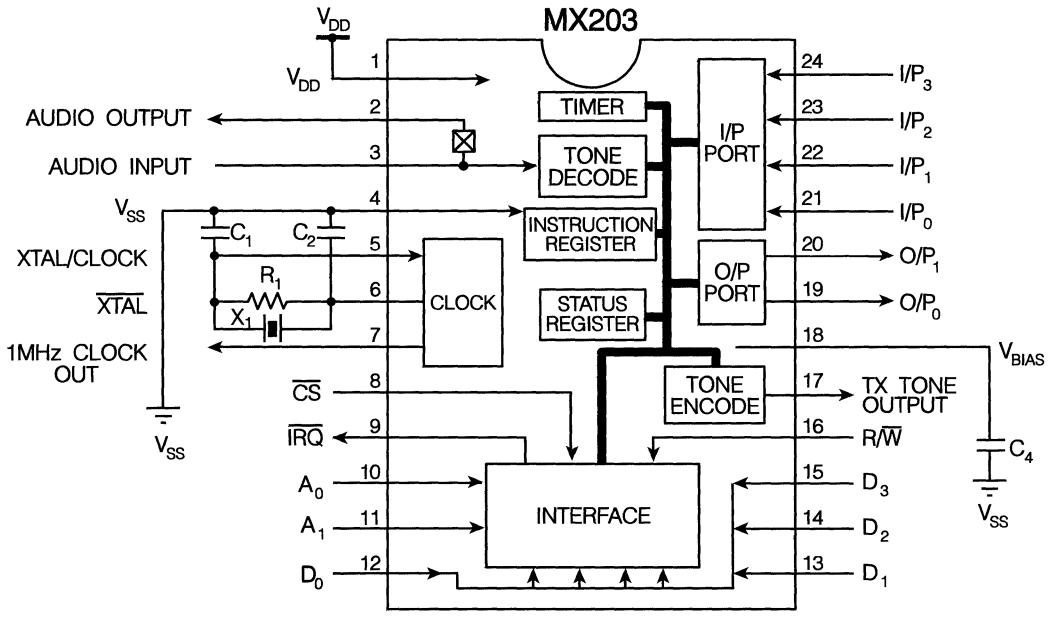
By reading this register the microprocessor can monitor the state of the 4 logic input pins (I/P_0 - I/P_3). This facility allows external systems to communicate with the microprocessor through this device.

The MX203 caters to CCIR, EEA and ZVEI/Suppressed ZVEI sequential tone system frequencies in three tone sets, "C," "E, "and "Z" respectively, as shown in Table 1. See the "Specifications" pages for overall MX203 Tone performance characteristics.

Hex. Input/Output	D_3	D_2	D_1	D_0	"C" Tone Set f_0 (Hz)	"E" Tone Set f_0 (Hz)	"Z/SZ" Tone Set f_0 (Hz)
0	0	0	0	0	1981	1981	2400
1	0	0	0	1	1124	1124	1060
2	0	0	1	0	1197	1197	1160
3	0	0	1	1	1275	1275	1270
4	0	1	0	0	1358	1358	1400
5	0	1	0	1	1446	1446	1530
6	0	1	1	0	1540	1540	1670
7	0	1	1	1	1640	1640	1830
8	1	0	0	0	1747	1747	2000
9	1	0	0	1	1860	1860	2200
A	1	0	1	0	2400	1055	2800
B	1	0	1	1	930	930	810
C	1	1	0	0	2247	2247	970
D	1	1	0	1	991	991	886
E	1	1	1	0	2110	2110	2600
F	1	1	1	1	Notone	Notone	Notone

Table 1 - Tone Frequency Programming Codes

External Components



Component	Value	Component	Value
R1	1MΩ	C3	0.1µF
C1	33pF	C4	1.0µF
C2	33pF	X1	4.0MHz

Tolerances: R = ±10%, C = ±20%

Figure 2 - External Component Connections

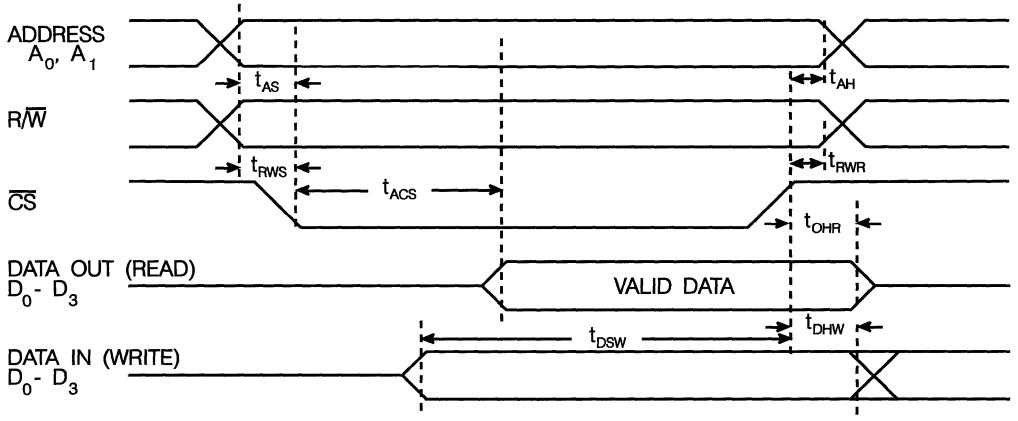


Figure 3 - CPU Interface Timing Diagram

SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{ss} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)	±30mA
(other pins)	±20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating temperature range:	-40°C to +85°C
Storage temperature range:	-55°C to +125°C

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C. Xtal/Clock f_0 = 4.0 MHz. Audio level 0dB ref: 775 mVrms.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current—					
RX on, TX and Timer Disabled		—	1.25	—	mA
RX on, TX Enabled, Timer Running	1	—	3.0	—	mA
Interface Levels					
CPU Data Port (D_0 - D_3) In/Out	8				
Logic "1"		3.5	—	—	V
Logic "0"		—	—	1.5	V
Output Logic "1" Source Current	9	—	—	120.0	µA
Output Logic "0" Sink Current	10	—	—	360.0	µA
Three State Output Leakage Current		—	—	4.0	µA
Input Port (I/P_0 - I/P_3) & (R/W, A_0, A_1, CS)					
Logic "1"		3.5	—	—	V
Logic "0"		—	—	1.5	V
Output Port (O/P_0 - O/P_1), ($\overline{IRQ}$)	2				
Logic "1"		4.0	—	—	V
Logic "0"		—	—	1.0	V
Impedances					
Input Port		0.1	1.0	—	MΩ
Output Port		—	15.0	50.0	kΩ
Audio Input	11	0.1	1.0	—	MΩ
Audio Switch S1 "ON"	11	—	2.0	5.0	kΩ
Audio Switch S1 "OFF"	11	1.0	10.0	—	MΩ
Tx Tone Output (Enabled)	14	—	1.0	—	kΩ
Tx Tone Output (Disabled)		1.0	10.0	—	MΩ
Clock - 4 Output		—	3.0	10.0	kΩ

Characteristics		See Note	Min.	Typ.	Max.	Unit
$\overline{IRQ}$ Output (Logic "1")			—	25.0	100.0	kΩ
$\overline{IRQ}$ Output (Logic "0")			—	150.0	500.0	Ω
Encoder						
Tone Output Level		1	-1.0	0	+1.0	dB
Tone Frequency Accuracy "C"			-4.0	*fo*	+4.0	Hz
Tone Frequency Accuracy "E"			-0.3	*fo*	+0.3	%
Tone Frequency Accuracy "Z"			-0.3	*fo*	+0.3	%
Tone Output Risetime		3	—	1.0	—	ms
Total Harmonic Distortion			—	—	5.0	%
Decoder						
Signal Inpput Range		4	-28.0	—	+7.0	dB
Decode Bandwidth—						
Probability > 0.995	"C"	5	±1.0	—	—	%
Probability > 0.995	"E"	5	±1.0	—	—	%
Probability > 0.995	"Z"	5	±2.0	—	—	%
Not Decode Bandwidth—						
Probability < 0.03	"C"	6	—	—	±3.0	%
Probability < 0.03	"E"	6	—	—	±3.0	%
Probability < 0.03	"Z"	6	—	—	±4.5	%
Noise Response Rate	"C"	7,12	—	1.0	—	Digits
Noise Response Rate	"E"	7,12	—	1.0	—	Digits
Noise Response Rate	"Z"	7,13	—	1.0	—	Digits
Decode Response Time						
Notone to Tone		5	20	25	Tp	ms
Tone to Notone			33	—	53	ms
Timing — (Figure 3)						
Address Set Up Time	t_{AS}		50	—	—	ns
Read/Write Set Up Time	t_{RWS}		50	—	—	ns
Address Hold Time	t_{AH}		0	—	—	ns
Read/Write Recovery Time	t_{RWR}		0	—	—	ns
Chip Select Access Time	t_{ACS}	8	—	—	250	ns
Output Hold Time (Read)	t_{OHR}		0	—	100	ns
Data Set Up Time (Write)	t_{DSW}		150	—	—	ns
Data Hold Time (Write)	t_{DHW}		20	—	—	ns
Power Up Reset Time	TS		3.0	—	—	ms

Notes

1. No TX Tone load.
2. Sink/Source currents ≤ 0.1 mA.
3. To 90% of nominal output, (from "F tone" to "not-F tone").
4. Sine or Square, a.c. coupled input.
5. With minimum tone period (Tp) for the tone set, S/N ratio 0dB.
6. Under all conditions of input amplitude and S/N ratio, with maximum Tp specified for the tone set.
7. Gaussian Noise Input 6kHz band limited with a maximum input level corresponding to 1-digit code falsing rate. (Random to random single characters.)
8. With each data line loaded as C = 50pf and R = 10kΩ.
9. V_{out} = 4.6V
10. V_{out} = 0.4V
11. External connections on the Audio Output may alter these values.
12. Single digit response in a 40.0-hour period.
13. Single digit response in a 1.0-hour period.
14. An emitter follower output with an internal 10kΩ pulldown resistor.

MX•COM, INC. MX503

3

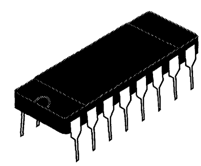
SEQUENTIAL TONE ENCODER

FEATURES

- CMOS Low Power Requirements
- No External Prefilters Needed
- 0dB Signal to Noise Performance
- >30dB Dynamic Range
- 25 ms Typical Response Time
- Quadradecimal Throughput
- Automatic Repeat Tone Translation

APPLICATIONS

- MX503QA: Metropage** - USA
- MX503C: CCIR - International
- MX503E: EEA - United Kingdom
- MX503Z: ZVEI - West Germany
- MX503ZS: Suppressed ZVEI



MX503*
16-pin side braize

MX503QA (USA), MX503C (CCIR), MX503E (EEA), MX503Z (ZVEI) or MX503ZS (SZVEI).

Description

The MX503 Sequential Tone Encoder accepts digital binary inputs to output audible tones that are compatible with one of four international sequential tone signaling conventions. Fifteen individual frequencies are synthesized from an external 560kHz ceramic resonator or quartz crystal. The output waveform is a sixteen step approximated sinewave output V_{DD}-V_{SS} peak to peak amplitude with a nominal 1kΩ source impedance. Total harmonic distortion without external filtering is less than 10%. Unwanted harmonic signals are down at least 20dB from the fundamental over a 50 kHz bandwidth, and down 44dB in the 5 kHz voice bandwidth.

Designed to perform the signal encoding function in the Hexadecimal Sequential Coding system, the MX503 permits tone coded data, address codes and control commands to be transmitted manually through a keyboard or automatically from stored programs. On-chip timing provides an elapsed tone period (T_P) marker flag according to the tone duration standard of the corresponding signal convention.

The MX503 Data Strobe/Latch input allows manual keyboard entry of data in real time. New data is entered by a 0-1 transition and latched by a 1-0 transition, so that a pulse from a keyswitch latches on a tone until the next key entry. In quadradecimal operation, entry of the hexadecimal "F" terminates the transmission. For hexadecimal systems, the No Char input yields a Notone output.

The MX503's low power consumption permits data origination from hand-held transceivers. Manual data entry requires only a keyboard-to-binary encoder as supplemental hardware. To accomodate system rise time needs, the initial output tone in a sequence may be delayed by using an external R-C time constant to control a Schmitt trigger provided on the Output Enable input.

***Metropage is a trademark of Motorola, Inc.*

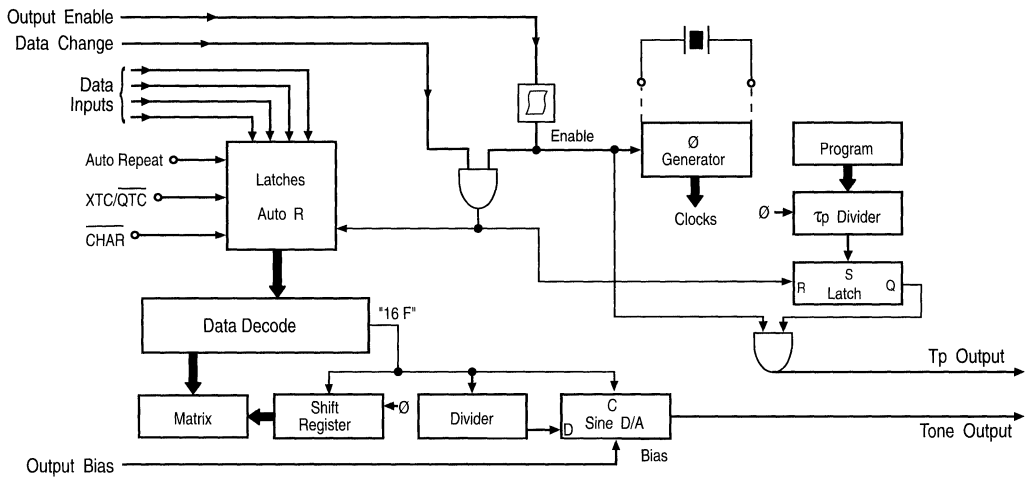


Figure 1 - Internal Block Diagram

PIN	FUNCTION/DESCRIPTION
1	**TONE OUTPUT**: V_{DD}-V_{SS} peak-to -peak, 16 step pseudo sine-wave output, with nominal 1kΩ source impedance.
2	**T_P OUTPUT**: This is the tone period expired output. It switches to logic "1" following a Data Strobe input after tone interval (established by international convention) has elapsed.
3	**OUTPUT BIAS**: A logic "1" input here sets a $V_{DD}/2$ bias on pin 1 (TONE OUTPUT).
4	**OUTPUT ENABLE**: A logic "1" input enables the TONE OUTPUT. The internal Schmitt trigger on this input allows an external R-C time constant to create a transmission delay, if required (see Fig. 5 and 6).
5	**DATA STROBE/$\overline{\text{LATCH}}$**: This input should be left low, but strobed on data entry. A 0-1 transition strobes data in and resets the T_P OUTPUT. A 1-0 transition latches that data and tone output until the next 0-1 input.
6	**AUTO REPEAT**: A mode select input. A HIGH on this pin programs the MX503 to automatically substitute the repeat tone frequency if the same data character is entered twice in succession.
7	**$\overline{T_P}$ OUTPUT**: For the MX503QA only: The inverse of pin 2. **HEX/$\overline{\text{QUAD}}$ SELECT**: For the MX503C, E and Z, this is a mode select input. A HIGH on this pin programs the MX503 to transmit hexadecimal data (using 17 distinct tones). A LOW on this pin programs quadradecimal data transfer capacity (comprised of 14 data characters or symbols and a 15th system control tone).
8	**V_{SS}**: Negative supply voltage.
9	**D_0**: Data input: Least significant bit.
10	**D_1**: Data input.
11	**D_2**: Data input.
12	**D_3**: Data input: Most significant bit.
13	**NO CHAR**: Used only for hexadecimal operation of the MX503. A logic "1" on this line along with a 1-0 transition on the DATA STROBE/$\overline{\text{LATCH}}$ (pin 5) results in a Notone output. The T_P OUTPUT operates and the DC bias of the TONE OUTPUT line (pin 1) is set at $V_{DD}/2$. The DATA INPUT lines will be data entry and quadradecimal operation.
14	**CLOCK IN**: This is the input to an internal inverter associated with the clock.
15	**$\overline{\text{CLOCK}}$**: This is the output from the internal inverter clock circuit.
16	**V_{DD}**: Positive supply voltage.

MX503 Quadradecimal Tone Table

Tone Frequencies Output (in Hz)					Data Input				Code
MX503QA	MX503C	MX503E	MX503Z	MX503ZS	8	4	2	1	Symbol
600	1981	1981	2400	2400	0	0	0	0	0
741	1124	1124	1060	1060	0	0	0	1	1
882	1197	1197	1160	1160	0	0	1	0	2
1023	1275	1275	1270	1270	0	0	1	1	3
1164	1358	1358	1400	1400	0	1	0	0	4
1305	1446	1446	1530	1530	0	1	0	1	5
1446	1540	1540	1670	1670	0	1	1	0	6
1587	1640	1640	1830	1830	0	1	1	1	7
1728	1747	1747	2000	2000	1	0	0	0	8
1869	1860	1860	2200	2200	1	0	0	1	9
2151	2400	1055	2800	886	1	0	1	0	A
2435	930	930	810	810	1	0	1	1	B
2007	2247	2247	970	740	1	1	0	0	C
2295	991	991	886	680	1	1	0	1	D
459	2110	2110	2600	970	1	1	1	0	E
NOTONE	NOTONE	NOTONE	NOTONE	NOTONE	1	1	1	1	F

Table 1 - Quadradecimal Tone Table

3

NOTES: *1. By national or international convention, code A used in an address transmission is the Group Call flag, and code E substitutes a sequentially repeated frequency.*
2. Code F initiates and sometimes terminates each address transmission. (Refer to HSC System Overview at the beginning of the HSC section.)
3. Tones for codes B, C and D are not specified by international convention.

MX503 Hexadecimal Tone Table

Tone Frequencies Output (in Hz)			Data Input				Code
MX503C	MX503E	MX503Z	8	4	2	1	Symbol
1981	1981	2400	0	0	0	0	0
1124	1124	1060	0	0	0	1	1
1197	1197	1160	0	0	1	0	2
1275	1275	1270	0	0	1	1	3
1358	1358	1400	0	1	0	0	4
1446	1446	1530	0	1	0	1	5
1540	1540	1670	0	1	1	0	6
1640	1640	1830	0	1	1	1	7
1747	1747	2000	1	0	0	0	8
1860	1860	2200	1	0	0	1	9
2400	1055	2800	1	0	1	0	A
930	930	810	1	0	1	1	B
2247	2247	970	1	1	0	0	C
991	991	886	1	1	0	1	D
873	873	740	1	1	1	0	E
1055	2400	680	1	1	1	1	F
2110	2110	2600		REPEAT			X
NOTONE	NOTONE	NOTONE		DON'T CARE			NO CHAR

Table 2 - Hexadecimal Tone Table

NOTES: *1. The tone frequency associated with code X is automatically substituted for the tone of any sequentially repeated character, provided the Auto Repeat (pin 6) has been set HI.*
2. NO CHAR operation blanks the data input lines and inhibits tone output; DC bias is maintained at $V_{DD}/2$, Tp line outputs.
3. Tones for codes B, C, D and F are not specified by international convention.

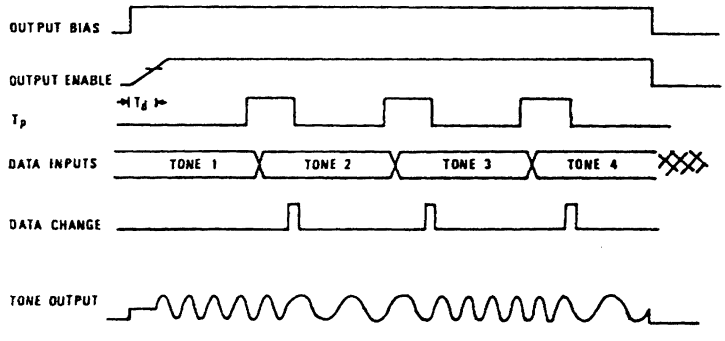
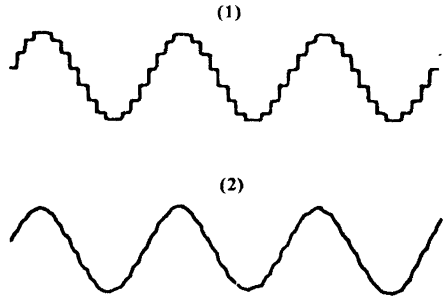


Figure 2 - Timing Diagram



1. 16-step pseudo-sinewave MX503 output
2. Same tone after simple filtering.

Figure 3 - Typical Waveform

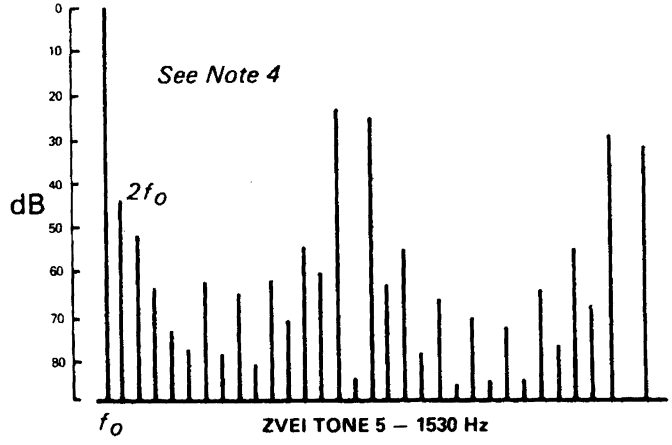


Figure 4 - Output Frequency Spectrum

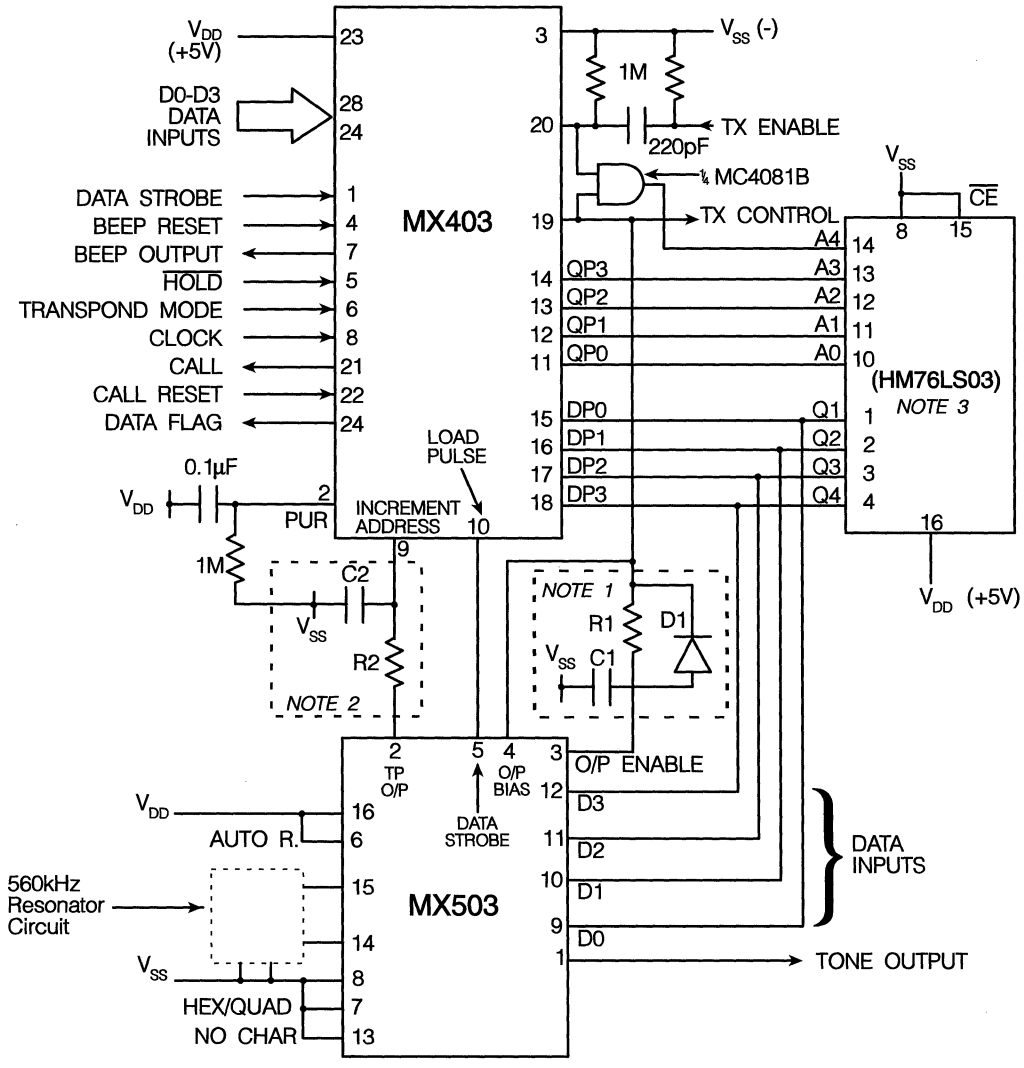


Figure 5 - Circuit Connection Diagram (1)

Notes:

1) Include these components to provide a transmit delay.

2) Include these components to increase transmitted tone periods.

3) The system illustrated contains the local decode address (and transmit) code starting at memory address location 00001. The transpond code is programmed starting from memory location 11001.

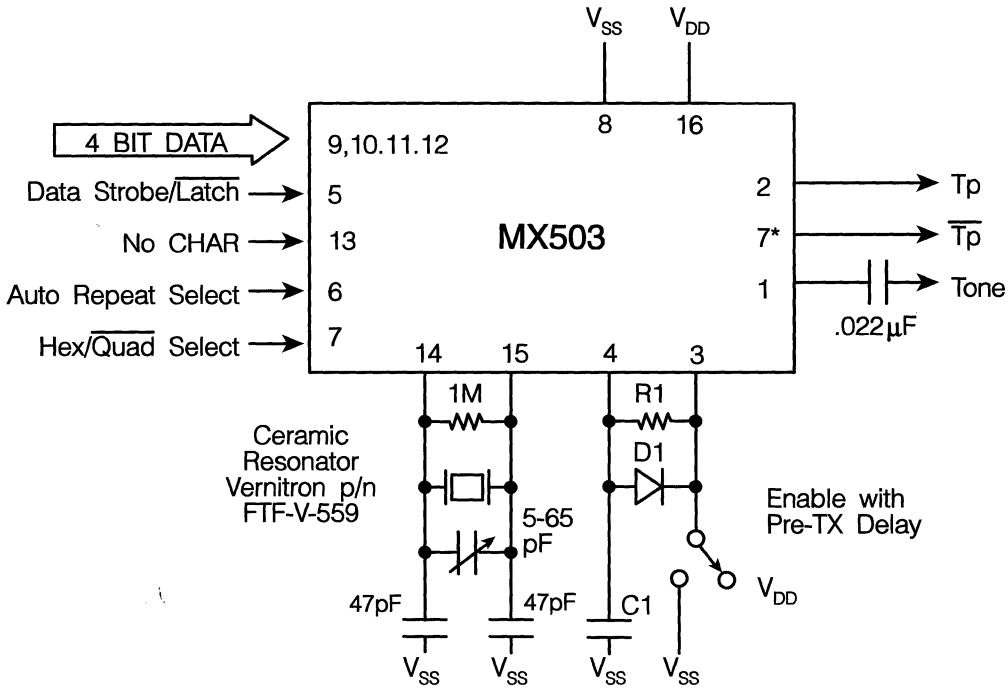


Figure 6 - Circuit Connection Diagram (2)

3

Notes:

1) Select values for R1 and C1 appropriate to the desired pre-transmit delay, if any.

2) Ceramic resonator sources are:
   a. Raltron, part number POE-B560 kHz
   b. Murata, part number BFB-560J

3) * $\overline{\text{Tp}}$ Output is available only on the MX503QA.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 V to V_{DD} + 0.3 V
Sink/Source Current (Total)	20mA
Operating Temperature	-30°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.

V_{DD}=5.0V

T_{AMB}=25°C

Xtal/Clock fo = 560 kHz

Characteristics are valid for all tones unless otherwise stated.

Characteristics	Min.	Typ.	Max.	Unit
Static Values				
Supply Voltage (V_{DD})	4.5	5.0	5.5	V
Supply Current	1	3	4	mA
Logic 1 Output Level (1 source = 0.1mA)	4.5	-	-	V
Logic 0 Output Level (1 sink = 0.1mA)	-	-	0.5	V
Logic 1 Input Level	3.5	-	-	V
Logic 0 Input Level	-	-	1.5	V
Dynamic Values				
Tone Output Level	4.5	-	-	V p-p
Tone Source Impedance	-	1	-	kΩ
THD	-	-	10	%

Tone Period Expired (T_P OUTPUT, Pin 2) Time Table

Model	Signaling Convention	T_P
MX503QA	"Metropage"	33ms ±0.1%
MX503C	CCIR	100ms ±0.1%
MX503E	EEA	40ms ±0.1%
MX503Z/ZS	ZVEI/SZVEI	70ms ±0.1%

Frequency Accuracy @560kHz

Model	f_0 ±	Signaling Convention	f_0 ±
MX503QA	0.13%*	"Metropage"	0.1%
MX503C	7 Hz	CCIR	7 Hz
MX503E	0.3%	EEA	0.3%
MX503Z/ZS	0.5%	ZVEI/ZVEI	0.5%

*NOTE: The MX503QA's f_0 of ±0.13% provides a worst case transmit error of 2.85 Hz, well within the ±16 Hz "must accept" bandwidth of the receiver.

MX•COM, INC.

MX803A

Advance Information

C-BUS COMPATIBLE

AUDIO SIGNALING PROCESSOR

DESCRIPTION

The MX803A, a member of the DBS800 IC family, is an audio signaling processor that provides an inband tone signaling capability for LMR radio systems. Signaling systems supported include SelCall (CCIR, EEA, ZVEI I, II, and III) 2-Tone SelCall and DTMF encode.

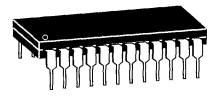
Using a non-predictive decoder and versatile encoder gives the MX803A the capability to work in any standard or non-standard tone system.

The MX803A is a full-duplex device for use with Single Tone or Selective Call systems. It consists of:

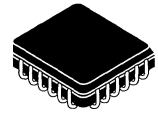
- A tone decoder with programmable NOTONE timer.
- Two individual tone encoders and a programmable TX period timer.
- An on-chip summing amplifier.

Under the control of the microcontroller (via C-BUS, the DBS800 serial interface) the MX803A will simultaneously encode and transmit 1 or 2 audio tones in the 208-3000Hz range. It also will detect, decode, and indicate the frequency of any non-predicted input tone in the frequency range of 313 to 6000Hz.

A general purpose logic input, interfacing directly with the Status Register, is provided. This could be used as an auxiliary method of routing digital information to the



MX803AJ
24-pin CDIP



MX803ALH
24-pin PLCC

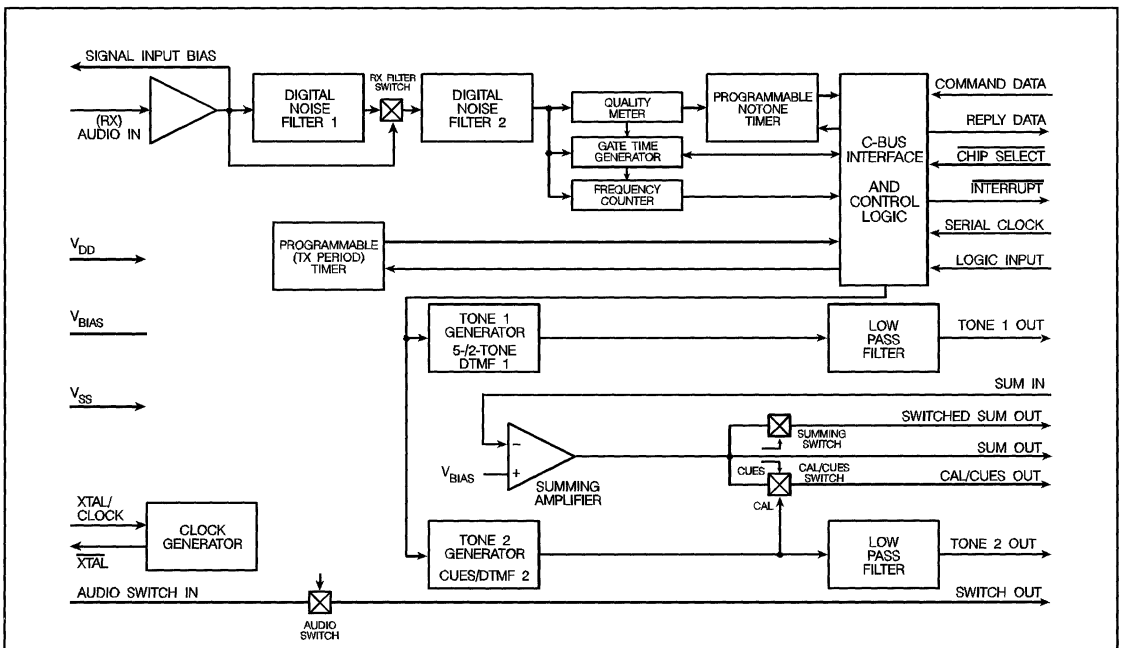


Figure 1 - MX803A Audio Signaling Processor

DESCRIPTION...

microcontroller via the C-BUS. Output frequencies are produced from data loaded to the device. A programmable, general purpose, on-chip timer sets the tone transmit periods. A Dual-Tone Multi-Frequency (DTMF) output is obtained by combining the 2 independent output frequencies in the integral summing amplifier. This process can also be used for level correction.

Tones produced by the MX803A can be used in the system as modulation calibration inputs and as "CUE" audio indications to the operator. Received tones are measured and their frequency indicated to the microcontroller in the form of a received data word. A poor quality or incoherent tone will indicate Notone.

The MX803A is a low-power 5-volt CMOS IC available in 24-pin CDIP and 24-lead plastic SMT packages.

PIN FUNCTION CHART

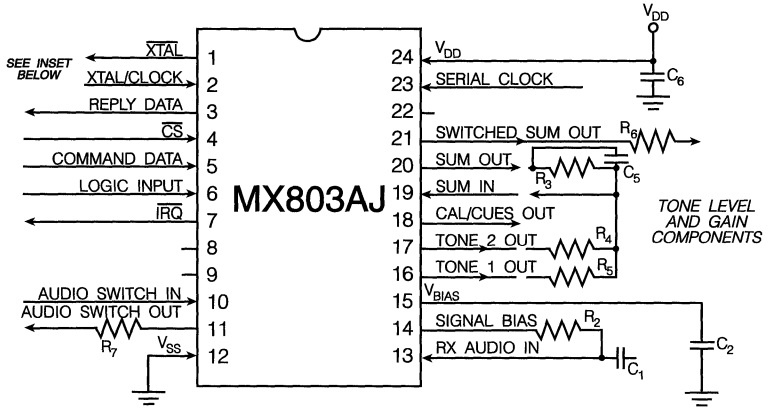
Pin	Function
1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. External components are required at this output when a Xtal is used. See Figure 2.
2	**Xtal/Clock:** The input to the on-chip clock oscillator inverter. A Xtal or externally derived clock should be connected here. See Figure 2.
3	**Reply Data:** This is the C-BUS serial data output to the microcontroller. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the $\overline{\text{Chip Select}}$ input. This 3-state output is held at high impedance when not sending data to the microcontroller. See Timing Diagrams.
4	**$\overline{\text{Chip Select}}$ ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the microcontroller. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Timing Diagrams.
5	**Command Data:** The "C-BUS" serial data input from the microcontroller. Data is loaded to this device in 8-bit bytes, MSB (B7) first and LSB (B0) last, synchronized to the Serial Clock. See Timing diagrams.
6	**Logic Input:** This "real-time" input is available as a general purpose logic input port which can be read from the Status Register (see Table 3).
7	**$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$):** The output of this pin indicates an interrupt condition to the microcontroller by going to a logic "0." This is a "wire-or-able" output, allowing the connection of up to 8 peripherals to 1 interrupt port on the microcontroller. This pin has a low impedance pulldown to logic "0" when active and a high impedance when inactive. The system $\overline{\text{IRQ}}$ line requires one pullup resistor to V_{DD}. The conditions that cause interrupts are indicated in the Status Register and are shown below: G/Purpose Timer Period Expired NOTONE Timer Period Expired RX Tone Measurement Complete These interrupts are inactive during relevant powersave conditions and can be disabled by bits 5 and 6 in the Control Register.
8	**N/C:** No internal connection.
9	**N/C:** No internal connection.
10	**Audio Switch In:** This is the input to the stand-alone on-chip Audio Switch. This function (Control Register bit 7) may be used to break the system transmitter modulation path when it is required to provide a CUE (beep) from Tone Generator 2 to the loudspeaker via the MX806A LMR Audio Processor.
11	**Audio Switch Out**: The output of the stand-alone on-chip Audio Switch.
12	**V_{SS}:** Negative supply (GND).

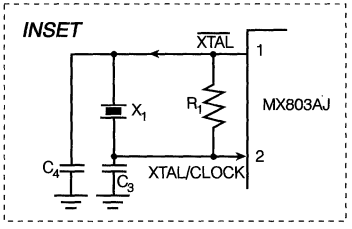
PIN FUNCTION CHART

Pin	Function
13	**RX Audio In:** The received audio tone signaling input. This input must be a.c. coupled and connected, using external components, to the Signal Input Bias pin (See Figure 2).
14	**Signal Input Bias:** External components are required between this input and the RX Audio In pin (See Figure 2).
15	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C_2. See Figure 2.
16	**Tone 1 Out:** This is the Tone 1 Generator (2-/5-tone Selcall or DTMF 1) output. External gain and coupling components will be required at this output when operating in a complete DBS 800 audio installation. The frequency of this output is determined by writing to the TX Tone Generator 1 Register (Table 5). See Figure 2.
17	**Tone 2 Out:** This is the Tone 2 Generator (2-/5-tone Selcall, CUES or DTMF 2) output. External gain and coupling components will be required at this output when operating in a complete DBS 800 audio installation. The frequency of this output is determined by writing to the TX Tone Generator 2 Register (Table 5). See Figure 2.
18	**CAL/CUES Out:** An auxiliary, selectable tone frequency output, providing a square wave CALibration signal from the Tone 2 Generator or a sine wave CUES (beep) signal from the Summing Amplifier. The output mode (CAL or CUES) is selected by bit 14 in the TX Tone Generator 2 Register (Table 5). In a DBS 800 audio installation, this output should be connected to the Calibration Input of the MX806A LMR Audio Processor. When Tone Generator 2 is set to Notone, the CAL input is pulled to V_{BIAS}; during a powersave of Tone Generator 2 it is held at V_{SS}.
19	**Sum In:** The input to the on-chip Summing Amplifier. This amplifier is available for combining Tone 1 and Tone 2 outputs (DTMF). Gain and coupling components should be used at this input to provide the required system gains. See Figures 2 and 3.
20	**Sum Out:** The output of the on-chip summing amplifier. Combined tones (1 and 2) are available at this output. See Figures 2 and 3.
21	**Switched Sum Out:** This is the combined tone output available for transmitter modulation. The switch allows control of the MX803A final output to the MX806A. Control of this switch is by bit 4 of the Control Register. See Figures 2 and 3.
22	No internal connection.
23	**Serial Clock:** The "C-BUS" serial clock input. This clock, produced by the microcontroller, is used for transfer timing of commands and data to and from the Audio Signaling Processor. See Timing diagrams.
24	**V_{DD}:** Positive supply. A single +5 volt power supply is required. Levels and voltages within this Audio Signaling Processor are dependent upon this supply. ***NOTE:*** *1) Pins 8, 9, and 22 may be connected to V_{SS} to improve screening.* *2) A glossary of abbreviations used in this document can be found on page 12.* *C-BUS is MX-COM's proprietary standard for the transmission of commands and data between a µController and DBS 800 ICs. It may be used with any µController, and can, if desired, take advantage of hardware serial I/O functions embodied into many types of µController. The C-BUS data rate is determined solely by the µController.*

3

Analog Application Information





Component	Value	Component	Value
R_1	1.0MΩ	C_1	0.1µF
R_2	2.0MΩ	C_2	1.0µF
*R_3	100kΩ	C_3	33.0pF*
*R_4	82.0kΩ	C_4	33.0pF*
*R_5	122kΩ	C_5	22.0pF
*R_6	100kΩ	C_6	1.0µF
*R_7	100kΩ	X_1	4.00MHz

Tolerances : R = ±10%, C = ±20%

*Note: For X_1 > 5MHz, $C_3 = C_4$ = 18pF

Figure 2 - External Components

NOTES

1. Xtal/clock components described are recommended in accordance with MX-COM's Application Note on Standard and DBS 800 Crystal Oscillator Circuits (April 1990).

2. Resistors marked with an asterisk (*) are System Components whose values are calculated to allow the MX803A to operate with other DBS 800 microcircuits. Figure 3 shows these components used in the system signal paths.

3. R_3, R_4, R_5 and C_5 are tone mixing components calculated to provide a 3dB tone differential (twist) for use in a DTMF configuration. Single tone output levels are set independently or by the MX806A Modulator Drivers. R_7 provides modulation level and matching for inputs to the MX806A.

4. To improve screening and reduce noise levels around the MX803A, pins 8, 9 and 22 should be connected to V_{SS}.

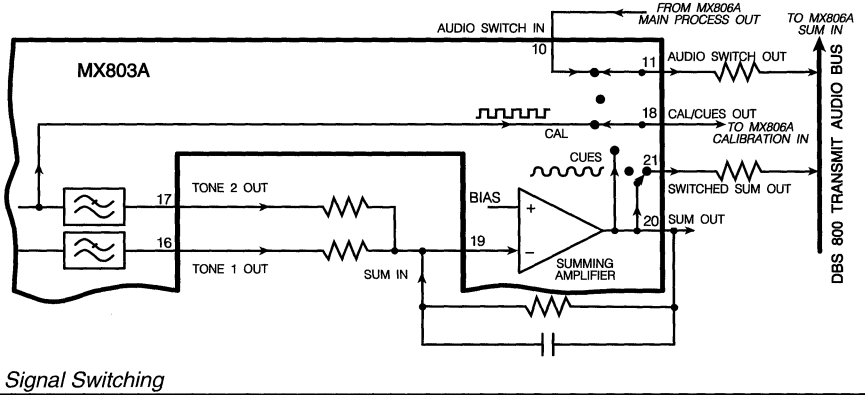


Figure 3 - Signal Switching

Controlling Protocol

Control of the MX803A Audio Signaling Processor's operation is by communication between the µController and the MX803A internal registers on the C-BUS using Address/Commands (A/Cs) and appended instructions or data (see Figure 7). The use and content of these instructions is detailed in the following pages.

MX803A Internal Registers

Control Register (30_H) -- Write only, control and configuration of the MX803A.

Status Register (31_H) -- Read only, reporting of device functions.

RX Tone Frequency Register (32_H) -- Read only, indicates frequency of the last received input.

RX Notone Timer (33_H) -- Write only, setting of the RX Notone period.

TX Tone Generator 1 Register (34_H) -- Write only, setting the required output frequency from TX Tone Generator 1.

TX Tone Generator 2 Register (35_H) -- Write only, setting the required output frequency from TX Tone Generator 2.

General Purpose Timer Register (36_H) -- Write only, setting of a general purpose sequential time period.

Address/Commands

The first byte of a loaded data sequence is always recognized by the C-BUS as an Address/Command (A/C) byte. Instruction and data transactions to and from this device consist of an A/C byte followed by further instruction/data or a status/data reply.

Instructions and data are loaded and transferred via C-BUS in accordance with the timing information given in Figures 7 and 8.

Table 1 shows the list of A/C bytes relevant to the MX803A.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB LSB	Data Byte(s)
General Reset	01	0 0 0 0 0 0 0 1	
Write to Control Register	30	0 0 1 1 0 0 0 0	+ 1 byte instruction to Control Register
Read Status Register	31	0 0 1 1 0 0 0 1	+ 1 byte reply from Status Register
Read RX Tone Frequency	32	0 0 1 1 0 0 1 0	+ 2 bytes reply from RX Tone Register
Write to Notone Timer	33	0 0 1 1 0 0 1 1	+ 1 byte instruction to Notone Register
Write to TX Tone Gen. 1	34	0 0 1 1 0 1 0 0	+ 2 bytes instruction to TX Tone Gen. 1
Write to TX Tone Gen. 2	35	0 0 1 1 0 1 0 1	+ 2 bytes instruction to TX Tone Gen. 2
Write to G/Purpose Timer	36	0 0 1 1 0 1 1 0	+ 1 byte instruction to G/Purpose Timer

Table 1 - C-BUS Address/Commands

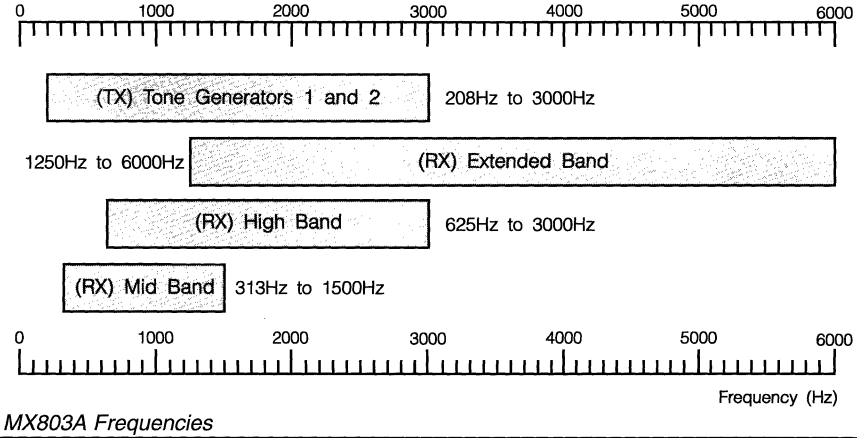


Figure 4 - MX803A Frequencies

Controlling Protocol...

"Write to Control Register" - A/C 30_H, followed by 1 byte of Command Data

Audio Switch
See the signal switching diagram (Figure 3) for application examples.

General Purpose Timer
This should be set up before interrupts are enabled since a General Reset command will set the timer period to 00_H - 0ms (permanent interrupt).

Interrupt Enable Instructions
Status bits 0, 1 and 2 are produced regardless of the state of these settings.

Band Selection
Bits 2 and 3 set the required frequency range. (See Figure 4, MX803A Frequencies.)

Summing Switch
Used to interrupt the MX803A drive to the MX806A Audio Processor (see Figure 3, Signal Switching).

Interrupt Designation
Decoder Interrupts:
Notone Timer and RX Tone Measurement
Transmitter Interrupt:
G/Purpose Timer Interrupt

Setting		Control Bits
MSB		***Transmitted First***
Bit 7		Audio Switch
1		Enable
0		Disable
6		***G/Purpose Timer Interrupt***
1		Enable
0		Disable
5		***Decoder Interrupts***
1		Enable
0		Disable
4		***Summing Switch***
1		Enable
0		Disable
3	***2***	***Band Selection***
0	0	High Band
0	1	Mid Band
1	0	Extended Band
1	1	Do not use this setting
1		Set to
0		"0"
0		Set to
0		"0"

Table 2 - Control Register

"Read Status Register" - A/C 31_H, followed by 1 byte of Reply Data

Setting	Status Bits
MSB	***Received First***
Bit 7	Set to
0	"0"
6	Set to
0	"0"
5	Set to
0	"0"
4	Set to
0	"0"
3	***Logic Input Status***
1	"1"
0	"0"
2	***G/Purpose Timer Period***
1	Expired (Interrupt Generated)
1	***Notone Timer Period***
1	Expired (Interrupt Generated)
0	***RX Tone Measurement***
1	Complete (Interrupt Generated)

Table 3 - Status Register

Interrupt Requests ($\overline{IRQ}$)
Interrupts on this device are available to draw the attention of the microcontroller to a change in the condition of the bit in the status register. However, bits are set in the status register irrespective of the setting of interrupt enable bits (Table 2) and these changes may be recognized by polling the register.

General Purpose Timer Period
Set to a logic "1" when the timer period has expired. Cleared to a logic "0" by:
a) Reading the Status Register, or
b) New G/Purpose Timer information, or
c) General Reset command

Notone Timer Period
Set to a logic "1" when the timer period has expired. Cleared to a logic "0" by:
a) Reading the Status Register, or
b) New Notone Timer information, or
c) General Reset command

RX Tone Measurement
Set to a logic "1" when the RX Tone Measurement is complete. Cleared to a logic "0" by:
a) Reading the Status Register, or
b) General Reset command

Controlling Protocol...

TX Tone Generator Regsiters 1 and 2

Each TX Tone Generator is controlled individually by writing a two-byte command to the relevant TX Tone Generator Register. The format of this command word, which is different for each tone generator, is shown below with the calculations required for tone frequency (f_{TONE}) generation described in the following text.

"Write to TX Tone Generator 1 Register" - A/C 34_H, followed by 2 bytes of Command Data

MSB (loaded first)			Bit Numbers											LSB (loaded last)	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	Notone/ Enable	These 13 bits (0 to 12) are used to produce a binary number, designated "A." "A" is used in the formulas below to set the TX Tone 1 frequency (f_{TONE} 1).												

Table 4 - TX Tone Generator 1

SETTING TX TONE GENERATOR 1

The binary number produced by bits 0 to 12 (MSB) is designated "A." If "A" = all logic "0" TX Tone Generator 1 is Powersaved.

Bit 13 at logic "1" = Tone 1 Output at V_{BIAS} (NOTONE)
"0" = Tone 1 Output Enabled
Bits 14 and 15 (MSB) must be logic "0."

SETTING TX TONE GENERATOR 2

The binary number produced by bits o to 12 (MSB) is designated "B." If "B" = all logic "0" then TX Tone Generator 2 is Powersaved.

Bit 13 at logic "1" = Tone 1 Output at V (NOTONE)
"0" = Tone 1 Output Enabled.
Bit 14 at logic "1" = Squarewave CAL Output.
"0" = Sinewave CUES Output.
Bit 15 (MSB) must be a logic "0."

3

"Write to TX Tone Generator 2 Register" - A/C 35_H, followed by 2 bytes of Command Data

MSB (loaded first)				Bit Numbers										LSB (loaded last)	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CAL/ CUES	Notone/ Enable	These 13 bits (0 to 12) are used to produce a binary number, designated "B." "B" is used in the formulas below to set the TX Tone 2 frequency (f_{TONE} 2).												

Table 5 - TX Tone Generator 2

Notes: (1) Programming Tone Generator 2 to Notone will place the CAL/CUES output at V_{BIAS} via a 40kΩ internal resistor.
(2) Programming Tone Generator 2 to Powersave will place the CAL/CUES output at V_{SS}.
(3) If both Tone Generators are Powersaved, the Input Amplifier is also Powersaved.

CALCULATIONS

As can be seen from Tables 4 and 5 (above), a binary number ("A" or "B" - bits 0 to 12) is loaded to the respective TX Tone Generator. The formulas described below are used to produce the required output frequency.

Required TX Tone output frequency = f_{TONE} 1 or 2
Xtal/clock frequency = f_{XTAL}
Input Data Word (bits 0 to 12) = "A" or "B"

Formula

$$f_{TONE} = \frac{f_{XTAL}}{4 \times \text{"A" or "B"}} \text{ (Hz)} \quad \text{or} \quad \text{Input "A" or "B"} = \frac{f_{XTAL}}{4 \times f_{TONE}} \text{ (Hz)}$$

TX TONE FREQUENCIES

With reference to Tables 4 and 5 (above), while Input Data Words "A" or "B" can be programmed for frequencies outside the stated limits of 208Hz and 3000Hz, any output frequencies obtained may not be within specified parameters (see Specification page).

Controlling Protocol...

"Read RX Tone Frequency Register" - A/C 32_H, followed by 2 bytes of Reply Data

Measurement of RX Signal Frequency S_{INPUT}

The measurements on this and the following page are for a clock frequency of 4.032 MHz (see the bottom of the page for a scaling formula for other crystal values).

The input audio signal, S_{INPUT}, is measured in the Frequency Counter over a specified measurement period (9.125ms or 18.250ms).

The measuring function counts the number of complete input cycles occuring within the count period and then the number of measuring clock cycles necessary to make up the period.

When the count period of a successful decode is complete, the RX Tone Measurement bit in the Status Register and the Interrupt bit are set.

The RX Tone Frequency Register will now indicate the signal frequency S_{INPUT} in the form of 2 bytes (1 and 0) as illustrated in Figure 6 below.

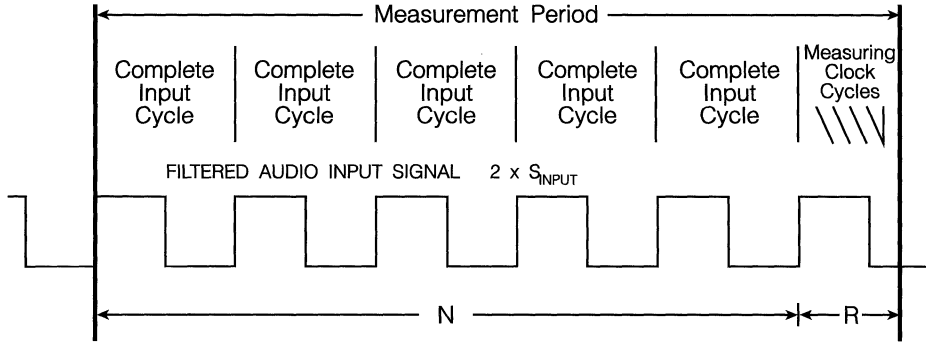


Figure 5 - Measurement of an RX Frequency

The Integer (N) - Byte 1

This is a binary number representing twice the number of complete input audio cycle periods. It is counted during the specified measurement period, which is:

High Band Decode	=	9.125 ms = "t"
Mid Band Decode	=	18.250 ms = "t"
Extended Band Decode	=	9.125 ms = "t"

See below for "t" and "f" scaling factors.

The Remainder (R) - Byte 0

This is a binary number representing the remainder part, R, of twice the Input Signal Frequency. R = "the number of specified measuring-clock cycles" required to complete the specified measurement period (See N). The clock cycle frequencies are:

High Band Decode	=	56.00 kHz = "f"
Mid Band Decode	=	28.00 kHz = "f"
Extended Band Decode	=	56.00 kHz = "f"

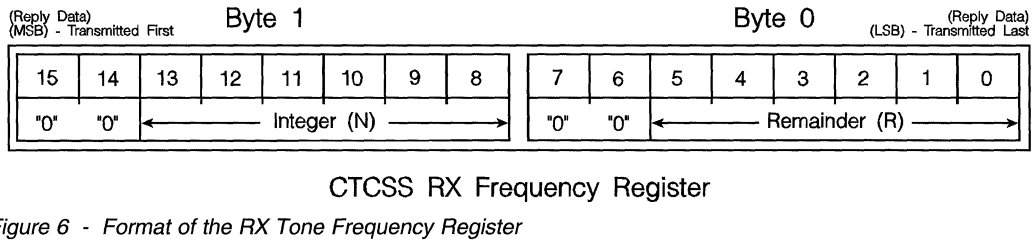


Figure 6 - Format of the RX Tone Frequency Register

f_{XTAL} Scaling Factors

The calculations above are for a Xtal of 4.032 MHz. The following formulas allow calculation of these values using any Xtal value.

$$\text{"t" scaled} = t \times \left(\frac{4.032}{f_{XTAL}}\right)$$

$$\text{"f" scaled} = f \times \left(\frac{f_{XTAL}}{4.032}\right)$$

Controlling Protocol...

Frequency Measurement: The following formulas show the derivation of the RX frequency S_{INPUT} from the measured data bytes (N and R).

High Band Measurement

S_{INPUT} - High Band
In the measurement period of 9.198ms, there are N cycles at $2S_{INPUT}$ and R clock cycles at 56.000kHz.

So $\frac{N}{2S_{INPUT}} + \frac{R}{56000} = 9.125ms$

from which $S_{INPUT} = \frac{28000 \times N}{(511-R)}$ Hz [1]

N and R - High Band
The measurement period = 9.125ms
Clock frequency = 56.000kHz
The measured frequency = $2S_{INPUT}$ Hz
In the measurement period there are:
$2S_{INPUT} \times 9.125 \times 10^{-3}$ cycles

Nh is the lower integer value of this decimal number:
$N = INT(9.125 \times 10^{-3} \times 2S_{INPUT})$ [4]

Rh is the lower integer value of this decimal number:
$R = INT(9.125 \times 10^{-3} - \frac{N) \times 56000}{2S_{INPUT}}$ [5]

Mid Band Measurement

S_{INPUT} - Mid Band
In the measurement period of 18.250ms, there are N cycles at $2S_{INPUT}$ and R clock cycles at 28.000kHz.

So $\frac{N}{2S_{INPUT}} + \frac{R}{28000} = 18.250ms$

from which $S_{INPUT} = \frac{14000 \times N}{(511-R)}$ Hz [2]

N and R - Mid Band
The measurement period = 18.250ms
Clock frequency = 28.000kHz
The measured frequency = $2S_{INPUT}$Hz
In the measurement period there are:
$2S_{INPUT} \times 18.250 \times 10^{-3}$ cycles

Nm is the lower integer value of this decimal number:
$N = INT(18.250 \times 10^{-3} \times 2S_{INPUT})$ [6]

Rm is the lower integer value of this decimal number:
$R = INT(18.250 \times 10^{-3} - \frac{N) \times 28000}{2S_{INPUT}}$ [7]

Extended Band Measurement

S_{INPUT} - Extended Band
In the measurement period of 9.125ms, there are N cycles at S_{INPUT} and R clock cycles at 56.000kHz.

So $\frac{N}{S_{INPUT}} + \frac{R}{56000} = 9.125ms$

from which $S_{INPUT} = \frac{56000 \times N}{(511-R)}$ Hz [3]

N and R - Extended Band
The measurement period = 9.125ms
Clock frequency = 56.000kHz
The measured frequency = S_{INPUT} Hz
In the measurement period there are:
$S_{INPUT} \times 9.125 \times 10^{-3}$ cycles

N is the lower integer value of this decimal number:
$N = INT(9.125 \times 10^{-3} \times S_{INPUT})$ [8]

R is the lower integer value of this decimal number:
$R = INT(9.125 \times 10^{-3} - \frac{N) \times 56000}{S_{INPUT}}$ [9]

Controlling Protocol...

"Write to RX Notone Timer Register" - A/C 33_H, followed by 1 byte of Command Data

Setting				Function/Period	
MSB					
7	6	5	4	Transmitted Bit 7 First	
0	0	0	0	These 4 bits must be "0"	
3	2	1	0	High Band	Mid Band
0	0	0	0	period (ms) 0	0
0	0	0	1	20 ±1%	40 ±1%
0	0	1	0	40 "	80 "
0	0	1	1	60 "	120 "
0	1	0	0	80 "	160 "
0	1	0	1	100 "	200 "
0	1	1	0	120 "	240 "
0	1	1	1	140 "	280 "
1	0	0	0	160 "	320 "
1	0	0	1	180 "	360 "
1	0	1	0	200 "	400 "
1	0	1	1	220 "	440 "
1	1	0	0	240 "	480 "
1	1	0	1	260 "	520 "
1	1	1	0	280 "	560 "
1	1	1	1	300 "	600 "

Table 6 - RX Notone Timer Settings

Operation of the RX Notone Timer

A NOTONE period is that period when no signal or a consistently bad quality signal is received. The NOTONE Timer is employed to indicate to the microcontroller that a NOTONE situation has existed for a predetermined period.

The NOTONE Timer period is "primed" by writing to the NOTONE Timer Register (33) using the instructions and information (1 data byte) given in Table 6. This timer register can be written-to and set in any mode of the MX803A except "Notone Timer Powersave." Priming the timer sets the timing period; this period will not be allowed to start until at least one frequency (tone) measurement has been sucessfully completed.

The NOTONE Timer is a one-shot timer that is reset only by successful tone measurements.

If the quality of the received signal drops to an unusable level the NOTONE Timer will start its run-down. On completion of this timer period, the NOTONE Timer Period Expired bit in the Status Register and an Interrupt are set.

Upon detection of the Interrupt, the Status Register should be read by the Controller to ascertain the source of the Interrupt.

The NOTONE Timer Period Expired bit is cleared:

i By a read of the Status Register
ii New NOTONE Timer Information
iii General Reset Command

The timer is set to 00_H by a General Reset command.

The following situations may be encountered by the NOTONE Timer circuitry:

NO SIGNAL

The NOTONE Timer can only start its run down on completion of a valid frequency measurement.

NO SIGNAL AFTER A VALID TONE MEASUREMENT

The timer will start to run down when the last RX Tone Measurement complete bit is set. At the end of the "primed" period the NOTONE Timer Period Expired bit in the Status Register and the Interrupt will be set.

SIGNAL FADES AFTER A VALID TONE MEASUREMENT

The timer will start to run down when the signal becomes unreadable to the device. At the end of the "primed" period the NOTONE Timer Period Expired bit in the Status Register and the Interrupt will be set.

SIGNAL APPEARS AFTER THE TIMER HAS STARTED

If the frequency measurement is more than 75% complete when the timer period expires, neither the NOTONE bit nor the Interrupt will be set unless that frequency measurement is subsequently aborted.

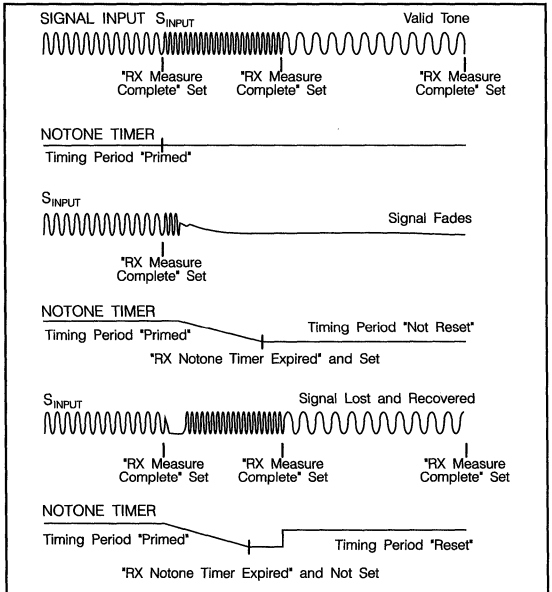


Figure 7 - Notone Timing

Controlling Protocol...

"Write to General Purpose Timer Register" - A/C 36_H, followed by 1 byte of Command Data

Setting				Function/Period	
MSB					
7	6	5	4	Transmitted Bit 7 First	
0	0	0	0	These 4 bits must be "0"	
3	2	1	0	High Band	Mid Band
				Reset Timer and Start Timing	
0	0	0	0	period of 0	0
0	0	0	1	10ms ±1%	20ms ±1%
0	0	1	0	20 "	40 "
0	0	1	1	30 "	60 "
0	1	0	0	40 "	80 "
0	1	0	1	50 "	100 "
0	1	1	0	60 "	120 "
0	1	1	1	70 "	140 "
1	0	0	0	80 "	160 "
1	0	0	1	90 "	180 "
1	0	1	0	100 "	200 "
1	0	1	1	110 "	220 "
1	1	0	0	120 "	240 "
1	1	0	1	130 "	260 "
1	1	1	0	140 "	280 "
1	1	1	1	150 "	300 "

Table 7 - General Purpose Timer Settings

Operation of the General Purpose Timer

This timer, which is not dedicated to any specific function within the MX803A, can be used within the DBS 800 system to indicate time-elapsed periods of between 10-150ms in the High Band or 20-300ms in the Mid Band to the microcontroller. Setting of the timer is by loading a single byte data word via the C-BUS (see Table 7 at left) to the MX803A through the Command Data line.

The timer will be reset and the run-down started on completion of Timer Data Word loading.

When the programmed time period has expired, the General Purpose Timer Expired bit (bit 2) in the Status Register and the Interrupt are set.

The General Purpose Timer Expired bit is cleared:
(i) By a read of the Status Register, or
(ii) New G/P Timer information, or
(iii) General Reset Command.

When the programmed time period has expired, this timer will reset, restart itself and continue sequencing until:
(i) New G/P Timer information is written, or
(ii) A General Reset Command is received.

The General Purpose Timer Expired bit and the interrupt will remain set until cleared.

The timer is set to 00_H (0ms) by a General Reset command.

3

Powersave

Various sections of the MX803A can be placed independently into a power-economical condition. Table 8 (below) gives a summary of these states available to the MX803A.

Powersaved Section	Instruction Source		Table
Tone Encoder 1	TX Tone Gen. 1 Reg. (34_H)	All bits = "0"	4
Tone Encoder 2	TX Tone Gen. 2 Reg. (35_H)	All bits = "0"	5
Input Amplifier	This action is automatic when both Tone Encoders are in the Powersave condition.		

Table 8 - MX803A Powersave Functions

Powersave Conditions

Xtal/Clock and C-BUS: This circuitry is always active, on all DBS 800 ICs, under any depowered/powersaved conditions

Controlling Protocol...

Interrupt Requests

An Interrupt ($\overline{IRQ}$), when enabled, is provided by the MX803A to indicate the following conditions to the μController.

Notone Timer Period Expired

Enabled: By Control Register bit 5.
Set: When the preset Notone Flag is set.
Identified: By Status Register bit 1.
Cleared: By reading the Status Register.

G/Purpose Timer Period Expired

Enabled: By Control Register bit 6.
Set: When the General Purpose Timer has timed out.
Identified: By Status Register bit 2.
Cleared: By reading the Status Register.

RX Tone Measurement Complete

Enabled: By Control Register bit 5.
Set: When an RX Frequency Measurement has been successfully completed.
Identified: By Status Register bit 0.
Cleared: By reading the Status Register.

On recognition of the "Read Status" Command byte, the interrupt output is cleared, the Status bits are transferred to the μController via the C-BUS Reply Data line and the internal Status bits are cleared.

Operational Recommendations

Following initial system power-up, a General Reset command should be sent.

Receive Sequence

1. Send Control Command for RX: Select Midband/ Highband and Digital Filter length.
2. Disable transmitters if desired by writing to Tone Frequency registers.
3. Prime the Notone timer by sending the required period byte.
4. Enable/disable interrupts as desired.
5. When a valid tone has been detected by a successfully completed measurement the Status Register is set to "Tone Measurement Complete" and an interrupt is set to the μC.
6. The μC examines the Status Register. If tone measurement is complete, it reads in the RX Tone Frequency in the form N + R (Fig. 6).
7. RX Tone Measurement Complete interrupts are periodically sent to the μC unless Notone is detected, in which case a Notone Interrupt is sent.

Transmit Sequence

1. Set Tone Frequency Generators to Notone during the transmitter initialization period.
2. Send Control Command for TX: Select Sum/Switched Sum o/p and Audio Switch states.
3. Send General Purpose (GP) Timer information for the Notone transmitter initialization period. This will initiate the timer.
4. Enable/disable interrupts as desired.
5. μC waits for "GP Timer Expired," reads the Status Register to check interrupts due to timer, and resets the Status Bit. If required, the μC sends the next timer period followed by the next tone(s) frequency information. A new timer period sent will reset the timer, otherwise the timer is self-resetting.
6. The μC monitors the interrupts and repeats 5 & 6 as required.
7. After last loaded tone, μC turns off Tone Generator(s).

General Reset

Upon power-up the bits in the MX803A registers will be random (either "0" or "1"). A General Reset Command 01_H will be required to reset all microcircuits on the C-BUS. It has the following effect on the MX803A:

Control Register	Set as 00_H
Status Register (bits 0, 1, 2)	Set as 00_H
Notone Timer	Set as 00_H
Tone Gen. 1 Reg. (2 bytes)	Set as 0000_H
Tone Gen. 2 Reg. (2 bytes)	Set as 0000_H
Gen. Purpose Reg.	Set as 00_H

This sets the MX803A to Encoder High Band (625Hz to 3000Hz) with interrupts disabled and both timers set to 00_H.

Both timers should be set up before interrupts are enabled to prevent initial, undesired interrupts.

Glossary of Abbreviations

Below is a list of abbreviations used in this Data Bulletin.

f_{XTAL} Xtal/Clock frequency.

S_{INPUT} Audio input signal.

f_{TONE} Tone frequency.

Timing Information

Figure 8 shows timing parameters for two-way communication between the µController and the MX803A on the C-BUS.

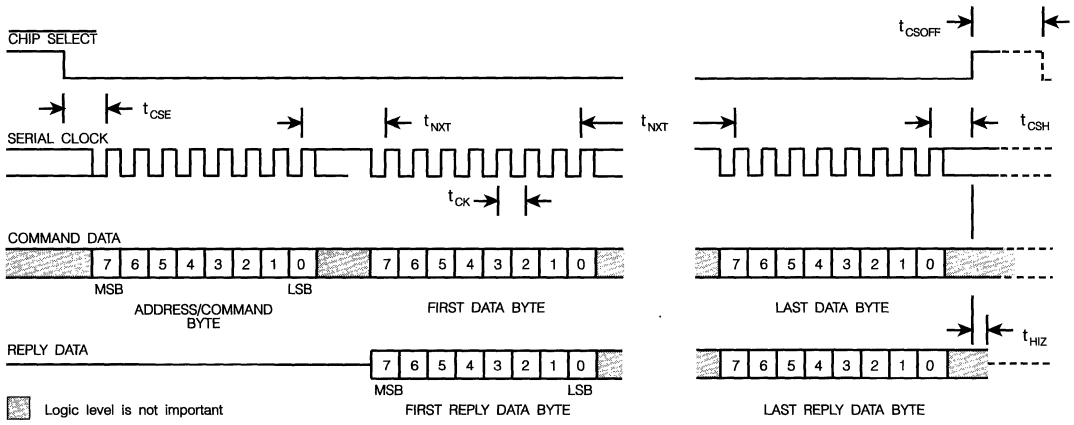


Figure 8 - C-BUS Timing

Parameter		Min.	Typ.	Max.	Unit
t_{CSE}	Chip Select Low to First Serial Clock Rising Edge	2.0	-	-	µs
t_{CSH}	Last Serial Clock Rising Edge to Chip Select High	4.0	-	-	µs
t_{CSOFF}	Chip Select High	2.0	-	-	µs
t_{NXT}	Command Data Inter-Byte Time	4.0	-	-	µs
t_{CK}	Serial Clock Period	2.0	-	-	µs
t_{CH}	Decoder or Encoder Clock High	500	-	-	ns
t_{CL}	Decoder or Encoder Clock Low	500	-	-	ns
t_{CDS}	Command Data Set-Up Time	250	-	-	ns
t_{CDH}	Command Data Hold Time	0	-	-	ns
t_{RDS}	Reply Data Set-Up Time	250	-	-	ns
t_{RDH}	Reply Data Hold Time	50.0	-	-	ns
t_{HIZ}	Chip Select High to Reply Data High - Z	-		2.0	µs

Notes: 1. Command Data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. Reply Data is read from the MX803A MSB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into the MX803A and into the microcontroller on the rising Serial Clock edge.
3. Loaded data instructions are acted upon at the end of each individual, loaded byte.
4. To allow for differing microcontroller serial interface formats, the MX803A will work with either polarity Serial Clock pulses.

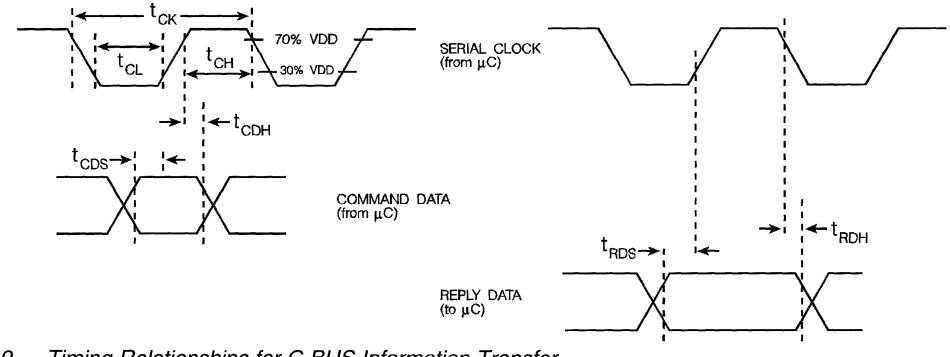


Figure 9 - Timing Relationships for C-BUS Information Transfer

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin	
(Ref V_{SS} = 0V)	-0.3V to (V_{DD} + 0.3V)
Sink/source Current	
(Supply pins)	±30mA
(Other pins)	±20mA
Total Device Dissipation	
@T_{AMB} 25°C	800mW max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/clock f_{XTAL} = 4.0MHz

Audio level 0dB ref. = 308mVrms @ 1kHz *(60% deviation, FM)*

Noise Bandwidth = 5.0kHz Band-Limited Gaussian

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
Decoder + Both Timers		-	2.0	-	mA
Decoder, Both Timers + One TX only		-	4.0	-	mA
All Functions Enabled		-	5.0	-	mA
Analog Impedances					
RX Audio Input		-	20.0	-	MΩ
Summing Amp Input		-	20.0	-	MΩ
Switch		-	1.0	-	kΩ
Tones 1 and 2 Outputs		-	10.0	-	kΩ
CAL/CUES Output		-	5.0	-	kΩ
Summing Outputs		-	10.0	-	kΩ
Dynamic Values					
Digital Interface					
Input Logic "1"	1	3.5	-	-	V
Input Logic "0"	1	-	-	1.5	V
Output Logic "1" (IOH = -120µA)	2	4.6	-	-	V
Output Logic "0" (IOL = 360µA)	3	-	-	0.4	V
I_{OUT} Tristate (Logic "1" or "0")	3	-	-	4.0	µA
Input Capacitance	1	-	-	7.5	pF
IOX (V_{OUT} = 5V)	4	-	-	4.0	µA
Overall Performances					
RX - Decoding					
High Band					
Sensitivity		-	-20.0	-	dB
Tone Response Time					
Good Signal	5,10	-	-	30.0	ms
Tone-to-Noise Ratio = 0dB	5,6,10	-	-	40.0	ms
Frequency					
Band		625	-	3000	Hz
Measurement Resolution		-	0.2	-	%
Measurement Accuracy	9	-	0.5	-	%

Characteristics	See Note	Min.	Typ.	Max.	Unit
Mid-Band					
Sensitivity		-	-20.0	-	dB
Tone Response Time					
Good Signal	7,10	-	-	60.0	ms
Tone-to-Noise Ratio = 0dB	6,7,10	-	-	80.0	ms
Frequency					
Band		313	-	1500	Hz
Measurement Resolution		-	0.2	-	%
Measurement Accuracy	9	-	0.5	-	%
Extended Band					
Sensitivity		-	-20.0	-	dB
Tone Response Time					
Good Signal	5,10	-	-	20.0	ms
Frequency					
Band		1250	-	6000	Hz
Measurement Resolution		-	0.2	-	%
Measurement Accuracy	9	-	0.5	-	%
TX - Encoders 1 and 2					
Tone Frequency		208	-	3000	Hz
Period ($1/f_{TONE}$) Error		-	-	1.0	λs
Tone Amplitude		-1.5	-	1.5	dB
Total Harmonic Distortion		-	-	5.0	%
Rise Time to 90%		-	$3/f_{TONE}$	-	ms
Fall Time to 10%	8	-	-	5.0	ms
Frequency Change Time		-	$3/f_{TONE}$	-	ms
Timers					
General Purpose					
Timing Period Range					
High-Band		10.0	-	150	ms
Mid-Band		20.0	-	300	ms
RX Notone					
Timing Period Range					
Hi-Band		20.0	-	300	ms
Mid-Band		40.0	-	600	ms
Xtal/Clock Frequency (f_{XTAL})		-	4.0	6.0	MHz

Notes: 1. Device control pins: Serial Clock, Command Data, and $\overline{CS}$.
2. Reply Data output.
3. Reply Data and $\overline{IRQ}$ outputs.
4. Leakage current into the "Off" $\overline{IRQ}$ output.
5. Measurement period = 9.198ms.
6. Decode Probability = 0.993.
7. Measurement period = 18.396ms.
8. When set to Powersave.
9. For a good input signal.
10. Inversely proportional to Xtal frequency, i.e. Spec * 4MHz/F_{XTAL}. So, for a 6MHz clock a 30ms tone response time becomes 20ms.

Section 4: Voice Processors

The following section contains specifications on several types of filters, including AMPS/TACS/NMT, audio bandpass and audio/ sub-audio filters.

Device	Description	Page
MX316	NMT Audio Filter Array	p. 267
MX336	Audio/Subaudio Filter Array	p. 272
MX346	Cellular Audio Processing Array	p. 278
MX366	Quad Filter Array (NAMPS/ETACS)	p. 285
MX386	Quad Filter Array (NAMPS/TACS/AMPS/ACSB)	p. 291
MX806A	Audio Processor	p. 295
MX816	NMT Audio Processor	p. 307
MX826	AMPS/NAMPS Audio Processor	p. 319
MX836	R2000 Audio Processor	p. 331

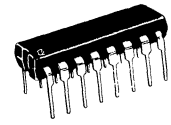
NMT AUDIO FILTER ARRAY

FEATURES:

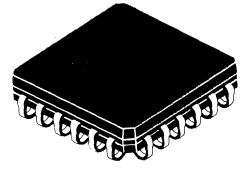
- **12th Order Lowpass Filter for S.A.T.* Rejection**
- **4 KHz S.A.T. Recovery Bandpass Filter**
- **Low Group Delay Distortion**
- **Single 5V CMOS Power Requirement**

APPLICATIONS:

- **Nordic Mobile Telephone (NMT) 450/900 MHz Mobile and Base Specifications**



MX316J (CDIP)
MX316P (PDIP)
16 pins



MX316LH
(24p PLCC)

DESCRIPTION:

The MX316 is a low power CMOS switched capacitor filter array designed to meet Nordic Mobile Telephone base and mobile specifications. As depicted in Figure 1, the device is comprised of:

1) a 12th order, 3.4 KHz lowpass filter which meets NMT 450 and 900 MHz base and mobile filter response specifications. Group delay distortion is minimized through this filter.
2) a 6th order, 4 KHz narrow bandpass filter which meets NMT 450 and 900 MHz S.A.T. recovery specifications.
3) an uncommitted amplifier, which may be used for a variety of applications, such as pre-emphasis, de-emphasis, and buffering.

An on-chip oscillator is driven by a 1 MHz crystal and provides all reference clocks for the switched capacitor filters via a divider chain. Alternatively, an external clock may be used. In standby mode, the chip enable feature is used to disable the three circuit elements.

*Supervisory Audio Tone

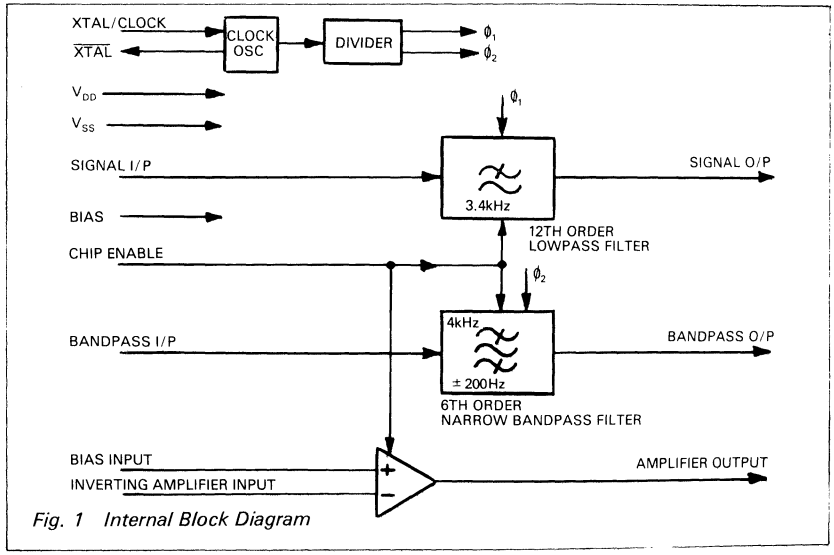
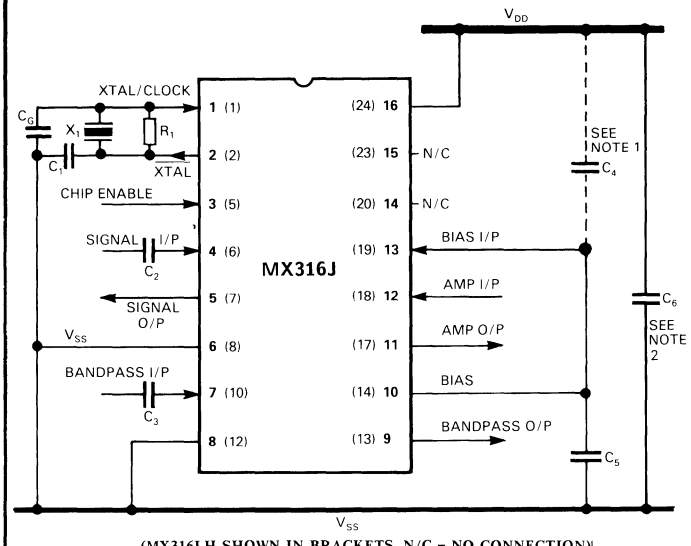


Fig. 1 Internal Block Diagram

MX316 PIN FUNCTION TABLE

PIN		FUNCTION	DESCRIPTION
MX316J MX316P	MX316LH		
1	1	**Xtal/Clock**	Connect 1 MHz crystal or externally derived clock to this input. Drives the on-chip inverting oscillator.
2	2	**$\overline{\text{Xtal}}$**	1 MHz crystal O/P. Inverting output of on-chip oscillator.
3	5	**Chip Enable**	Internally pulled to V_{dd}. A logic "0" applied to this pin will disable all filters and the uncommitted amplifier (powersave).
4	6	**Signal I/P**	Input to the lowpass filter. This input is internally biased and externally a.c. coupled by C2.
5	7	**Signal O/P**	Lowpass filter output internally biased to $V_{dd}/2$.
6	8	**V_{ss}**	Negative supply voltage
7	10	**BP I/P**	Input to bandpass filter. Internally biased and externally a.c. coupled by C3.
8	12	**V_{ss}**	Negative supply voltage
9	13	**BP O/P**	Bandpass filter output. Internally biased to $V_{dd}/2$.
10	14	**Bias**	$V_{dd}/2$ Bias Pin. Externally decoupled by C5 (see fig. 2, note 1).
11	17	**Amp O/P**	Uncommitted amplifier output
12	18	**Amp I/P**	Uncommitted amplifier inverting input
13	19	**Bias I/P**	Connect externally to "Bias" pin.
14	20	**N/C**	Internally connected. Leave open circuit.
15	23	**N/C**	Internally connected. Leave open circuit.
16	24	**V_{dd}**	Positive supply voltage

Note: MX316LH pin numbers 3,4,9,11,15,16,21, and 22 are not connected.



Component References

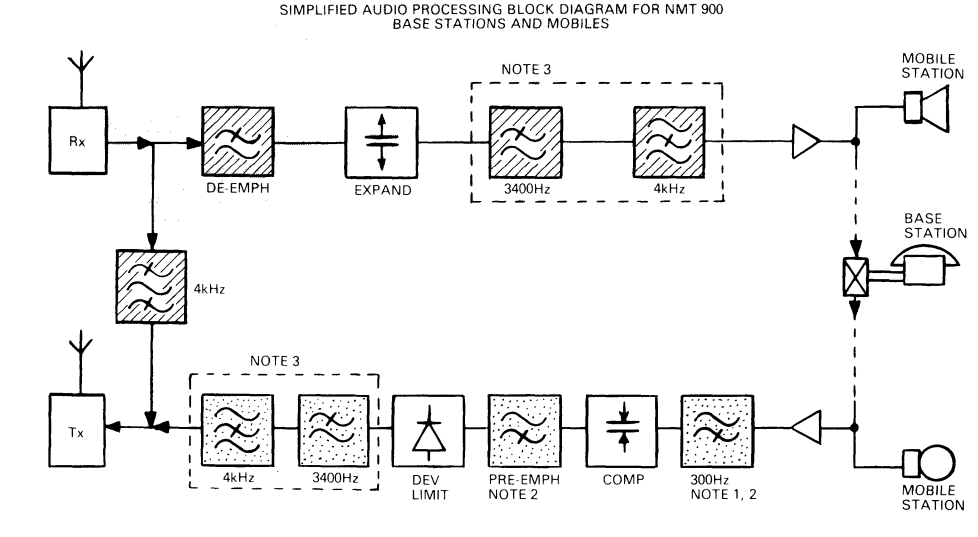
Component	Typical Unit Value	
R_1	1M	10%
C_1	33p	20%
C_2	0.1µ	20%
C_3	0.1µ	20%
C_4	0.1µ	20%
C_5	0.1µ Min.	20%
C_6	0.1µ	20%
C_G	68p	20%
X_1	1MHz	

NOTES:

1. *Bias may be decoupled to V_{SS} and V_{DD} using C_4, C_5 when input signals are referenced to the bias pin. For input signals referenced to V_{SS}, decouple Bias to V_{SS} using C_5 only.*
2. *Use C_6, when input signals are referenced to V_{SS}, to decouple V_{DD}.*

Fig. 2 External Component Connections

4



NOTES:

1). Not required in base station.
2). Pre-emph and highpass filter may be constructed using on-chip amplifier.
3). MX316 Lowpass Filter achieves both these functions.

MX316 (DEVICE A) MX316 (DEVICE B) BASE STATION ONLY

FIG. 3: MX316 TYPICAL APPLICATION

MX316 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		−0.3V to (V_{DD} + 0.3V)
Output sink/source current (total)		20mA
Operating temperature range:	MX316J	−30°C to +85°C
	MX316LH, MX316P	−30°C to +70°C
Storage temperature range:	MX316J	−55°C to +125°C
	MX316LH, MX316P	−40°C to +85°C
Maximum device dissipation:		All versions 100mW

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
V_{DD} = 5V, T_{amb} = 25°C, ∅ = 1MHz, $\Delta f_{\varnothing}$ = 0, f_{in} = 1kHz.

Characteristics		See Note	Min	Typ	Max	Unit
Static Characteristics						
Supply voltage			4.5	5	5.5	V
Supply current (Enabled)			—	6.0		mA
Supply current (Disabled)			—	700		µA
Input impedance (Filters & Amplifier)			100	1000	—	kΩ
Output impedance (Filters)			—	3	—	kΩ
Output impedance (Amplifier open loop)			—	800	—	Ω
Output impedance (Amplifier closed loop)			—	6	—	Ω
Input logic '1'			3.5	—	—	V
Input logic '0'			—	—	1.5	V
Dynamic Characteristics						
Passband Ripple	(300-3000Hz) LP	5	—	—	2	dB
	(4kHz±55Hz) BP	5	—	—	2	dB
Cut off frequency	(−3dB) LP	4,5	3000	3450	3800	Hz
	(−6dB) BP	4,5	4200	—	3800	Hz
Attenuation	(3800-4200Hz) LP	4,5	36	46	—	dB
	(<2000Hz,>6000Hz) BP	4,5	35	37	—	dB
Group Delay Distortion	(900-2100Hz) LP		—	80	—	µs
	(600-3000Hz) LP		—	450	—	µs
Output Noise (rms)	LP	1	—	1.6	—	mV
	BP	1	—	1	—	mV
Signal Input (rms)	LP	2	—	0.4	1.0	V
	BP	2	—	0.4	1.0	V
Insertion loss (1kHz)	LP		—	0	—	dB
(4kHz)	BP		—	0	—	dB
Aliasing Frequency			50	—	—	kHz
Inverting Amplifier						
Open loop gain		3	—	30	—	dB
Gain bandwidth product			—	1	—	MHz

Note: *1. Measured with input a.c. s/c.*
2. 'MAX' figure specified for nominal 3% distortion (30dB SINAD).
'TYP' figure specified for minimum distortion (MAX SINAD).
3. Relative to 1kHz. 100mV rms input level.
4. Refer to Figs. 4 and 5.
5. Specified over the full operating voltage and temperature range.

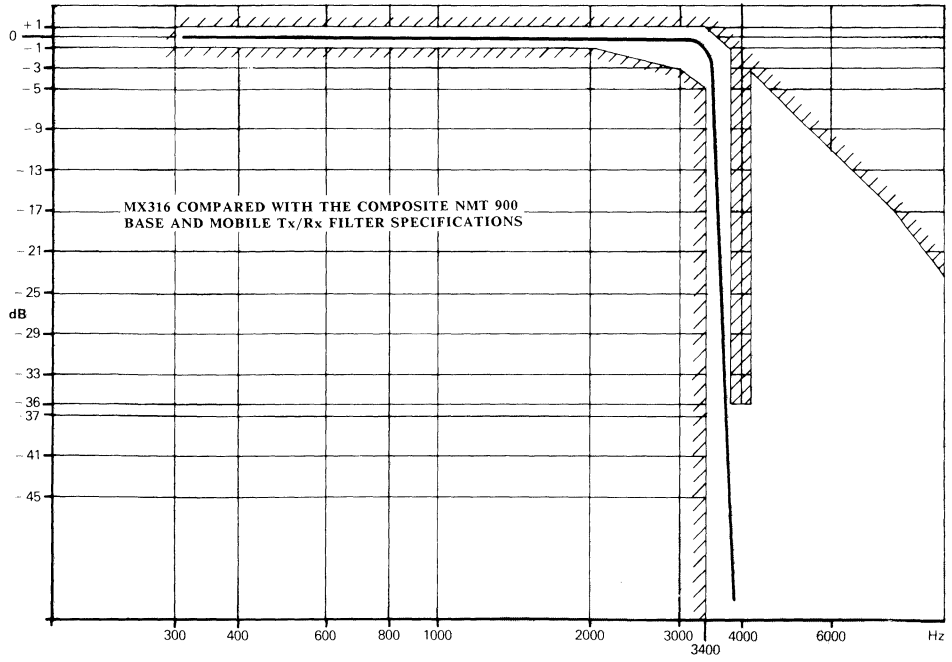


FIG. 4: TYPICAL MX316 LOWPASS FILTER RESPONSE

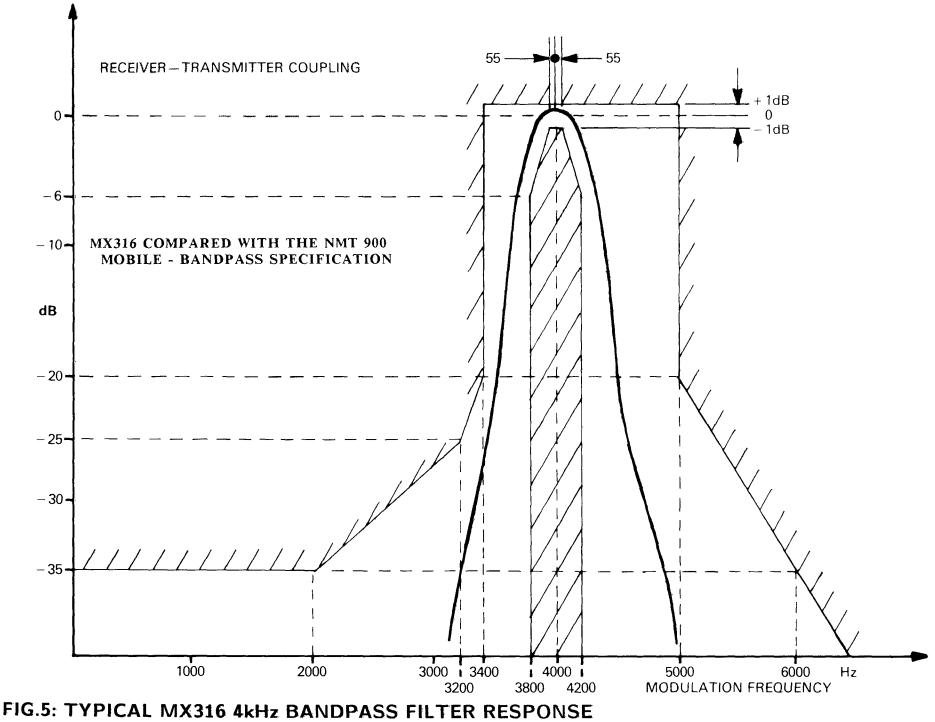
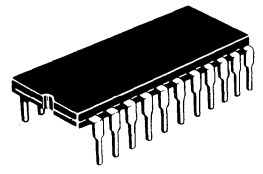
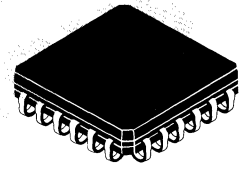


FIG.5: TYPICAL MX316 4kHz BANDPASS FILTER RESPONSE

AUDIO/SUB-AUDIO FILTER ARRAY



MX336J (CDIP)
MX336P (PDIP)
22 pins



MX336LH
(24p PLCC)

FEATURES:

- **High Order 300 Hz Highpass Filter**
- **Low Group Delay 2550 Hz Lowpass Filter**
- **On-chip 120-175 Hz Bandpass Filter**
- **Uncommitted Amplifier and Analog Switch**
- **50 dB Rejection Below 170 Hz**
- **Low Power CMOS**
- **Powersave Feature**

APPLICATIONS:

- **R2000 Mobile Radio Trunking System**
- **Other Trunking Systems with Sub-Audible Control Tones**

DESCRIPTION:

The MX336 is a CMOS switched capacitor filter array used to process speech and sub-audible data. As depicted in Figure 1, the device consists of:

1) a highpass audio filter with additional attenuation of signals below 170 Hz.
2) a lowpass audio filter for band-limiting speech. Group delay characteristics are controlled over the 900 to 2100 Hz range, allowing passage of 1200 Baud MSK data.
3) a narrow bandpass filter for sub-audio data processing.
4) an uncommitted audio amplifier
5) a mute switch with external control

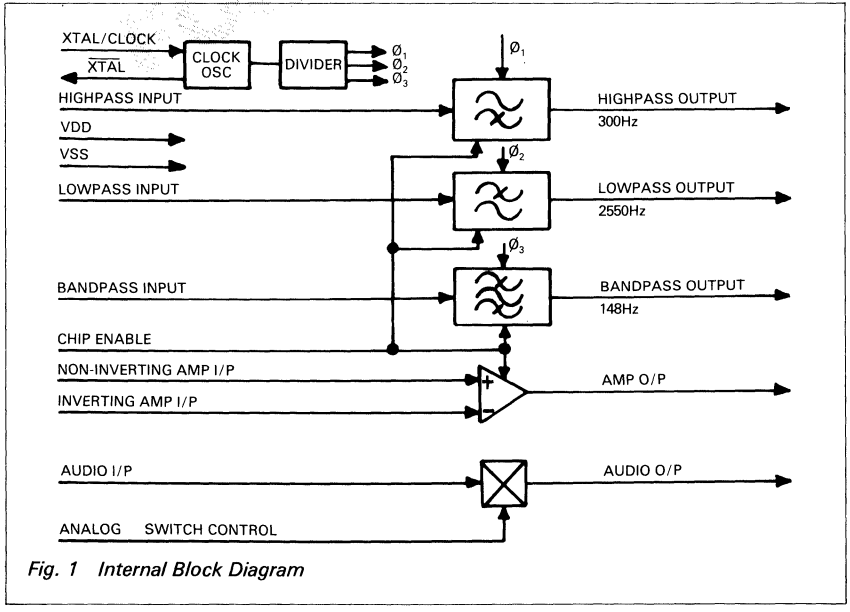
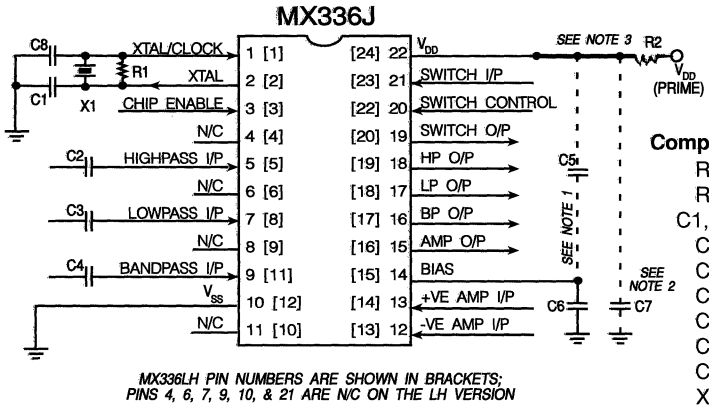


Fig. 1 Internal Block Diagram

MX336 PIN FUNCTION TABLE

PIN		FUNCTION/DESCRIPTION
MX336P	MX336LH	
1	1	**Xtal/Clock:** This is the input to the clock oscillator inverter. 1MHz crystal input or externally derived clock can be injected into this input.
2	2	**$\overline{\text{Xtal}}$:** Output of clock oscillator inverter.
3	3	**Chip Enable:** This input has an internal 1MΩ pull up resistor to V_{dd}. When pulled to V_{ss} (logic '0') all internal amplifiers are disabled and current consumption is reduced.
4	4	**No Connection.**
5	5	**HP I/P:** Input to highpass filter.
6	6 & 7	**No Connection.**
7	8	**LP I/P:** Input to lowpass filter.
8	9 & 10	**No Connection.**
9	11	**BP I/P:** Input to narrow bandpass filter.
10	12	**V_{ss}:** Negative supply.
11	—	**No Connection.**
12	13	**Amp Negative:** Inverting input of uncommitted amplifier.
13	14	**Amp Positive:** Non-inverting input of uncommitted amplifier.
14	15	**Bias:** This is the bias or analog ground pin and is set internally at $V_{dd}/2$. It should be decoupled to V_{ss} by an externally connected 0.1μF (min) capacitor.
15	16	**Amp Output:** Output of uncommitted amplifier.
16	17	**BP Output:** Output of narrow bandpass filter.
17	18	**LP Output:** Output of lowpass filter.
18	19	**HP Output:** Output of highpass filter.
19	20	**SW Output:** Output of analog switch.
—	21	**No connection.**
20	22	**SW Control:** Control input of analog switch, internally pulled to V_{dd} by 1MΩ resistor with switch in 'closed' position. When this input is pulled to VSS, the switch is in 'open' position.
21	23	**SW Input:** Input of analog switch.
22	24	**V_{dd}:** Positive supply.



Component	Value	Tolerance
R1	1MΩ	±10%
R2	-	±10% (Note 3)
C1, C8	33pF	±20%
C2	0.1µF	±20%
C3	0.1µF	±20%
C4	0.1µF	±20%
C5	0.1µF	±20% (Note 1)
C6	0.1µF	±20% (Note 1)
C7	-	Notes 2 and 3
X1	$1x10^6$Hz	Selectable

Notes:

1. Bias may be decoupled to V_{SS} and V_{DD} using C5 and C6 when input signals are referenced to the bias pin. For input signals referenced to V_{SS}, decouple Bias to V_{SS} using C6 only.

2. Use C1 when input signals are referenced to V_{SS}, to decouple V_{DD}.

3. Use R2 to assist decoupling of high frequency power supply noise (R2, C1, typically 300µs)

Figure 2 - External Component Connections

4

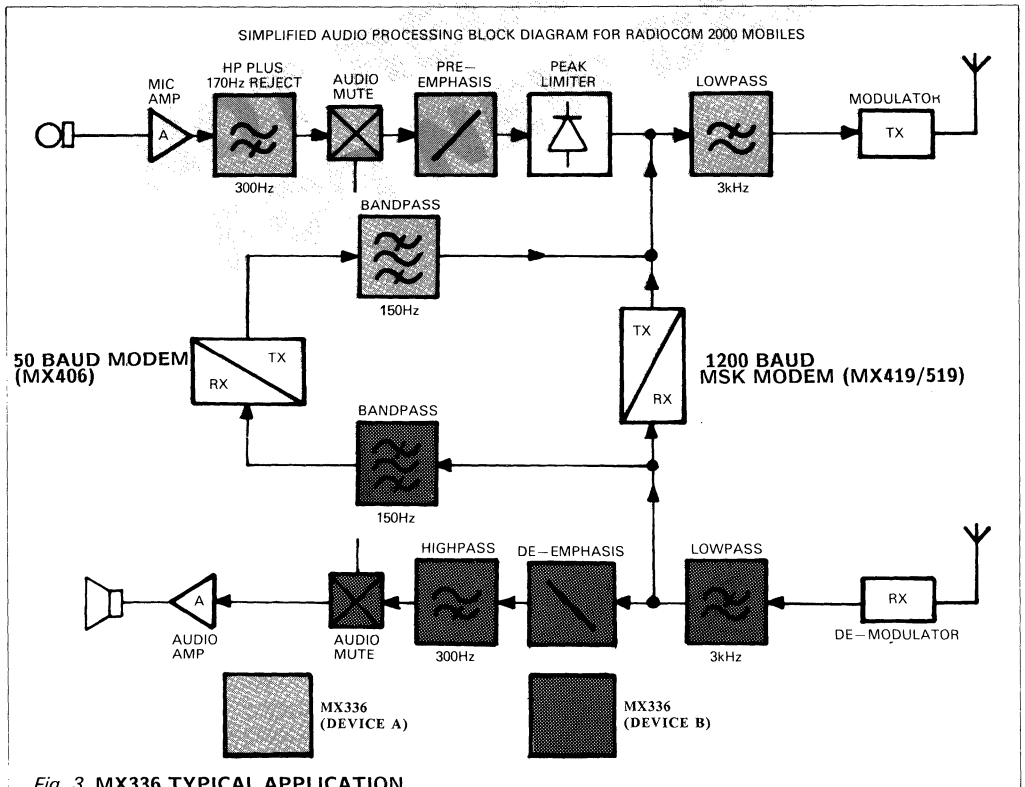


Fig. 3 **MX336 TYPICAL APPLICATION**

MX336 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref VSS = OV)		−0.3V to (VDD + 0.3V)
Output sink/source current (total)		20mA
Operating temperature range:	MX336J	−30°C to +85°C
	MX336LH, MX336P	−30°C to +70°C
Storage temperature range:	MX336J	−55°C to +125°C
	MX336LH, MX336P	−40°C to +85°C

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
VDD = 5V, T_{amb} = 25°C, ∅ = 1MHz, $\Delta f_{\varnothing}$ = 0, f_{in} = 1kHz

Characteristics			See Note	Min	Typ	Max	Unit
Static Characteristics							
Supply voltage				4.5	5	5.5	V
Supply current (Enabled)				—	3	—	mA
Supply current (Disabled)				—	500	—	µA
Input impedance (Filters & Amplifier)				100	2000	—	kΩ
Output impedance (Filters)				—	1.0	—	kΩ
Output impedance (Amplifier open loop)				—	800	—	Ω
Output impedance (Amplifier closed loop)				—	6	—	Ω
Input logic '1'				3.5	—	—	V
Input logic '0'				—	—	1.5	V
Dynamic Characteristics							
Passband Ripple	(300-2550Hz)	HP+LP	1	—	—	2	dB
	(120-175Hz)	BP	2	—	—	3	dB
Cut-off Frequency	(−3dB)	HP		—	265	—	Hz
	(−3dB)	LP		—	3800	—	Hz
	(−6dB)	BP		110	—	180	Hz
Attenuation	<170Hz	HP		43	55	—	dB
	>9000Hz	LP		40	47	—	dB
	<65Hz>290Hz	BP		30	40	—	dB
Group Delay Distortion	(900-2100Hz)	LP		—	30	60	µs
	(900-2100Hz)	HP+LP		—	200	—	µs
	(136-164Hz)		3	—	100	—	µs
Output Noise	(rms)	LP	4	—	1	—	mV
		HP	4	—	1	—	mV
		BP	4	—	4	—	mV
Signal Input	(rms)	LP	5	—	0.4	1.0	V
		HP	5	—	0.4	1.0	V
		BP	5	—	0.4	1.0	V
Insertion Loss	(1kHz)	HP+LP		−1	0	+1	dB
	(150Hz)	BP		−1	0	+1	dB
Aliasing Frequency				50	—	—	kHz

4

Characteristics	See Note	Min	Typ	Max	Unit
Audio Switch					
Output Noise (rms)	4	—	—	1	mV
Channel Resistance (on)		—	10	—	kΩ
Channel Resistance (off)		10	—	—	MΩ
Uncommitted Amplifier					
Open loop gain		35	50	—	dB
Bandwidth		—	200	—	kHz

Notes: *1. Absolute ripple — see Fig. 4.*
2. Absolute ripple — see Fig. 5.
3. Relative delay between 136 and 164Hz.
4. Measured with input a.c. s/c.
5. 'MAX' figure specified for nominal 3% distortion (30dB)
'TYP' figure specified for minimum distortion (MAX SINAD).

Fig. 4 Typical audio bandpass filter frequency response versus R2000 filter specification.

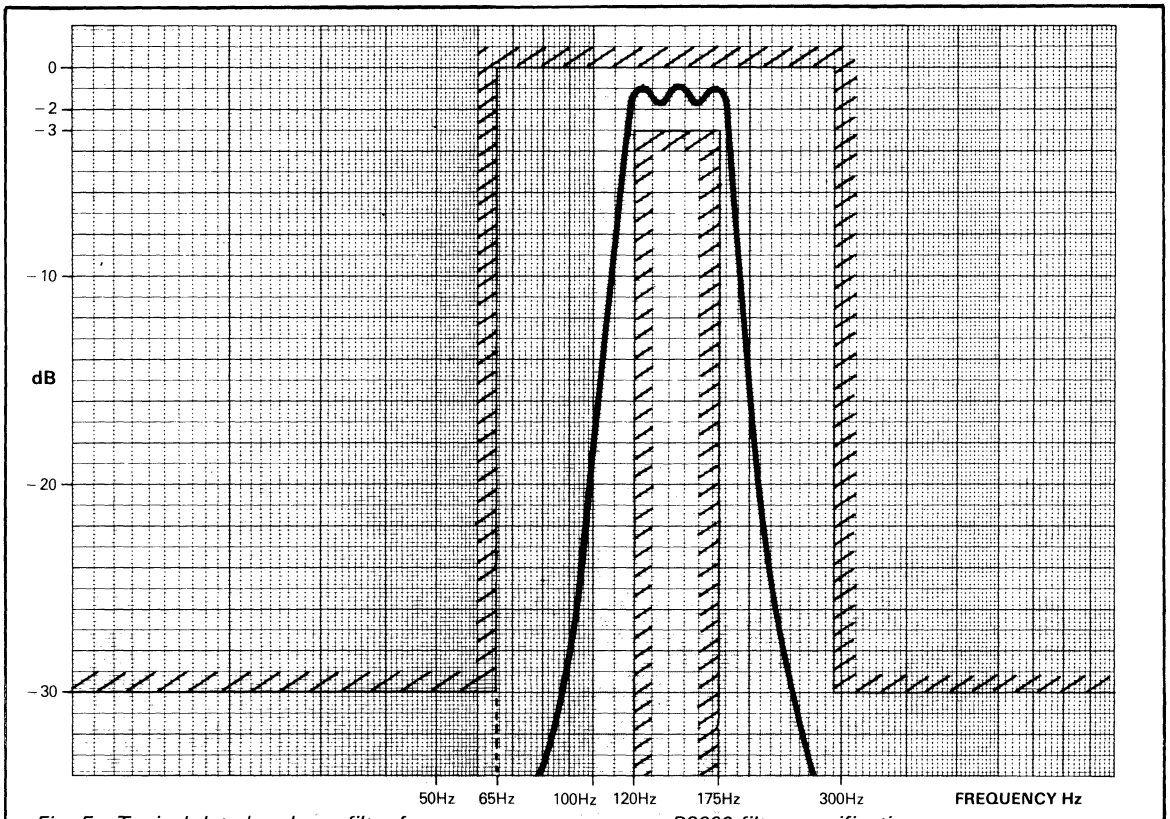


Fig. 5 Typical data bandpass filter frequency response versus R2000 filter specification.

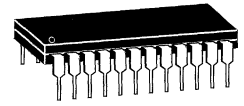
4

MX-COM, INC. MX346

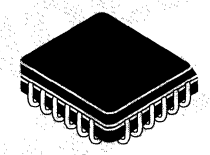
AUDIO PROCESSING ARRAY FOR CELLULAR TELEPHONES

FEATURES

- AMPS, TACS, NMT Audio + Data Processing
- Speech, SAT and Data—Full Duplex Filtering
- Speech Bandpass and Deviation Limiter Filters
- SAT 4/6kHz Bandpass Filters
- 8/10kbit RX Wideband Data Filter and Limiter
- Filters for Speech/MSK, Pre/De-emphasis
- Input Gain Adjustment



MX346J (CDIP)
MX346P (PDIP)
24 pins



MX346LH
PLCC-24

DESCRIPTION

The MX346 Audio Processing Array is a full-duplex Speech, SAT and Data Processor designed to meet the composite specifications of AMPS (Advanced Mobile Phone Service), TACS (Total Access Communication System), and NMT 450/900 (Nordic Mobile Telephone) cellular systems.

The RX Audio Path consists of a twelfth order lowpass filter, a fourth order highpass filter, and Input gain adjustment and de-emphasis.

The TX Audio Path consists of separate sixth and twelfth order lowpass filters, a fourth order highpass filter, a linear deviation limiter, and input gain adjustment and pre-emphasis.

The RX SAT and Data Path consists of a 13kHz wideband data filter and limiter, a switchable sixth order 4/6kHz SAT bandpass filter, and a 1200 baud MSK signal de-emphasis on chip.

All filter stages, excluding the RX data paths, may be de-powered for minimum current drain in the powersave mode. Operation in AMPS/TACS or NMT mode is controlled by a single logic input. A combination of the MX346 and the MX009 Digitally Controlled Amplifier Array, together with analog switches, offers a complete speech and processing soultion for cellular radio. All filter-sampling clocks are generated on-chip using an external 4.0MHz Xtal or clock pulse input. The MX346 is a low-power, single 5-volt device available in 24-pin cerdip, PDIP, or PLCC.

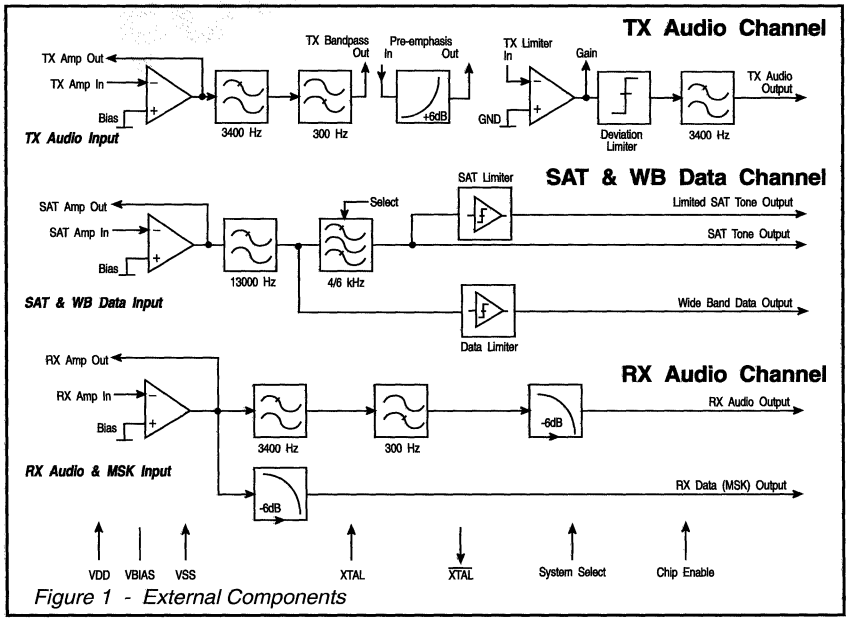


Figure 1 - External Components

PIN FUNCTION TABLE

Pin	Function
1	Xtal/Clock: The input to the clock oscillator circuitry. The clock oscillator components are on chip and require only a single 4MHz Xtal or clock pulse input. Clock oscillations are maintained in "powersave" (Chip Enable = "0"). See Figure 2.
2	$\overline{\text{Xtal}}$: The output of the clock oscillator circuitry. See Figure 2.
3	Chip Enable: The Chip Enable logic input. When at logic "0," the chip is put into the Powersave mode (with a minimum amount of monitoring circuitry enabled) to reduce current consumption. A logic "1" will enable all circuitry. This input operates in conjunction with the System Select Input; signal paths are as shown in Table 1.
4	System Select: A logic input to select signal paths to either the AMPS/TACS or NMT specification. This input operates in conjunction with the Chip Enable Input. Signal paths are shown in Table 1. Logic "1" = AMPS/TACS, logic "0" = NMT.
5	TX Amp Out: The "gain output" pin of the Transmit Audio Channel input amplifier. This output, together with the TX Amp In pin and external components, is used to set the required input gain/attenuation of this channel. See Figures 1 and 2.
6	TX Amp In: The input pin to the Transmit Audio Channel. This inverting input, together with the TX Amp Out pin and external components, is used to set the required input gain/attenuation of the channel. See Figures 1 and 2.
7	V_{BIAS}: The output of the on-chip analog bias circuitry, internally set to $V_{DD}/2$, this pin requires decoupling to V_{ss} with a capacitor, C_1. V_{BIAS} is maintained during powersave (Chip Enable = "0".) See Figure 2 and Table 1.
8	SAT Amp In: The input to the Supervisory Audio Tone (SAT) and Wideband Data Channel. This inverting input, together with the SAT Amp Out pin and external components, is used to set the required input gain/attenuation of the channel. See Figures 1 and 2.
9	SAT Amp Out: The "gain output" pin of the Supervisory Audio Tone (SAT) and Wideband Data Channel. This pin, together with the SAT Amp In pin and external components, is used to set the required input gain/attenuation of the channel. Special attention should be paid to the data circuit sensitivity (Specifications). See Figures 1 and 2.
10	RX Amp Out: The "gain output" pin of the Receive Audio Channel. This pin, together with the RX Amp In pin and external components, is used to set the required input gain/attenuation of the channel. See Figures 1 and 2.

PIN FUNCTION TABLE

Pin	Function
11	RX Amp In: The input to the Receive Audio Channel. This inverting input, together with the RX Amp Out pin and external components, is used to set the required input gain/attenuation of the channel. See Figures 1 and 2.
12	V_{SS}: Negative supply rail (GND).
13	SAT Tone Out: The filtered Supervisory Audio Tone (SAT) output. AMPS/TACS (-6dB) = 6kHz ± 200Hz. NMT (-6dB) = 4kHz ± 200Hz.
14	RX Wideband Data Out: The filtered, limited, wideband data output. This data channel produces a limited rectangular wave output. Special attention should be given to the data circuit sensitivity (Specifications). See Figures 1 and 2.
15	Limited SAT Tone Out: The filtered, limited Supervisory Audio Tone (SAT). Special attention should be given to the data circuit sensitivity (Specifications). See Figures 1 and 2.
16	RX Audio Out: The bandpass filtered, de-emphasized audio output of the RX Audio Channel.
17	RX Data Out: The de-emphasized, received data output. This data process may require filtering by low group delay filters before demodulation by modems such as the MX419, MX429, or MX439.
18	TX Audio Out: The processed audio to the transmission mixing and modulation circuitry.
19	TX Limiter Gain: The "gain output" of the TX Limiter Amplifier. This amplifier, using gain setting components, is used to produce the correct signal level for application to the Deviation Limiter. For limiter levels refer to the Specifications page. Recommended circuitry is shown in Figure 2.
20	TX Limiter In: The input to the TX Limiter Amplifier. This input should be connected by external components to the TX Pre-emphasis Out pin as shown in Figure 2.
21	TX Pre-emphasis Out: The output of the on-chip +6dB/octave pre-emphasis circuitry. This output should be connected to the TX Limiter Amplifier by external components as shown in Figure 2.
22	TX Pre-emphasis In: The input to the on-chip transmitter pre-emphasis circuitry. This input would normally be connected to the output of an external audio compressor circuit.
23	TX Bandpass Out: The output of the first stage of bandpass filtering in the Transmit Audio Channel. This output will normally be connected to the input of an external audio compressor circuit. See Figures 1 and 2.
24	V_{DD}: Positive supply rail. A single +5 volt power supply is required.

External Components

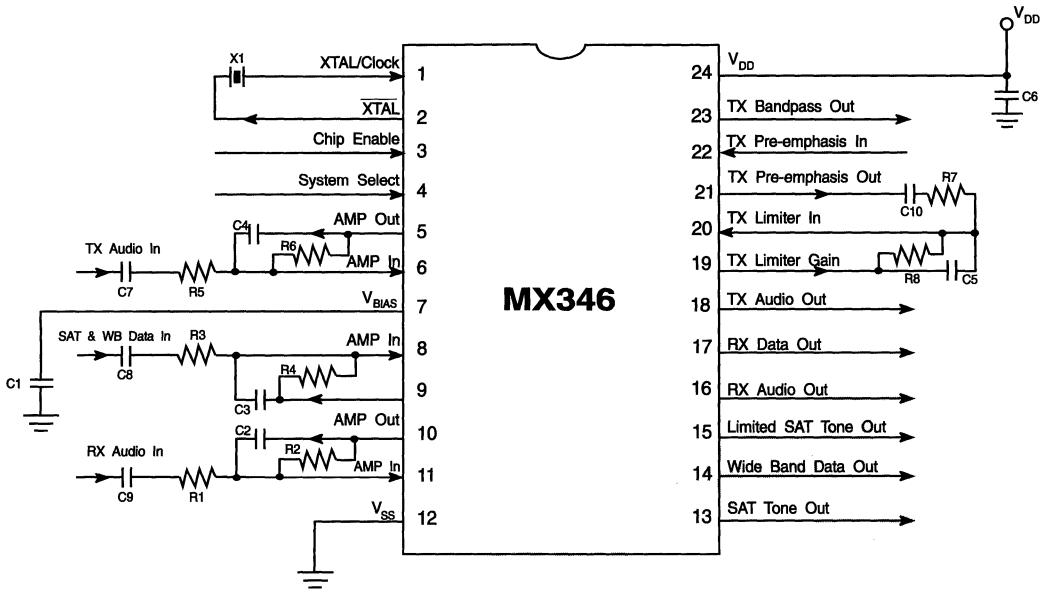


Figure 2 - External Component Connections

Component Value Notes

R_2 / R_1, R_4 / R_3, R_6 / R_5, and R_8 / R_7
Gain component combinations set the gains of the TX Audio, SAT and WB Data, RX Audio and Limiter inputs. Gain is calculated using the following formula and taking into account the effect of the parallel feedback capacitor.

$$\text{Gain} = \frac{R_{feedback}}{R_{input}}$$

It is recommended that all gain resistor values are kept above 10kΩ.

C_1
V_{BIAS} decoupling capacitor = 1.0 µF.

C_2, C_4, and C_5
Feedback capacitor values should be calculated (taking into account gain resistors R_1, R_2, and R_5 - R_8) to give a -3dB point at approximately 15kHz for RX and TX Channels for anti-alias filtering.

C_3
Feedback capacitor = 10.0pF

C_6
Power supply decoupling capacitor = 1.0 µF.

C_8
Input coupling capacitor = 0.1µF.

C_7, C_9, and C_{10}
Input coupling capacitors = 1.0µF.

Component Tolerances
Resistors ± 10%
Capacitors ± 20%

To maintain low current consumption, Output Buffers, anti-alias Clock Frequency Filters, and input internal pullup or pulldown resistors are not included on-chip.

A noisy or badly regulated power supply can cause instability and/or variance of selected gains.

Application Information

The diagram in Figure 3 (below) demonstrates the audio and data functions performed by the MX346 Audio Processing Array when employed in the audio stages of either an NMT or AMPS/TACS mobile application.

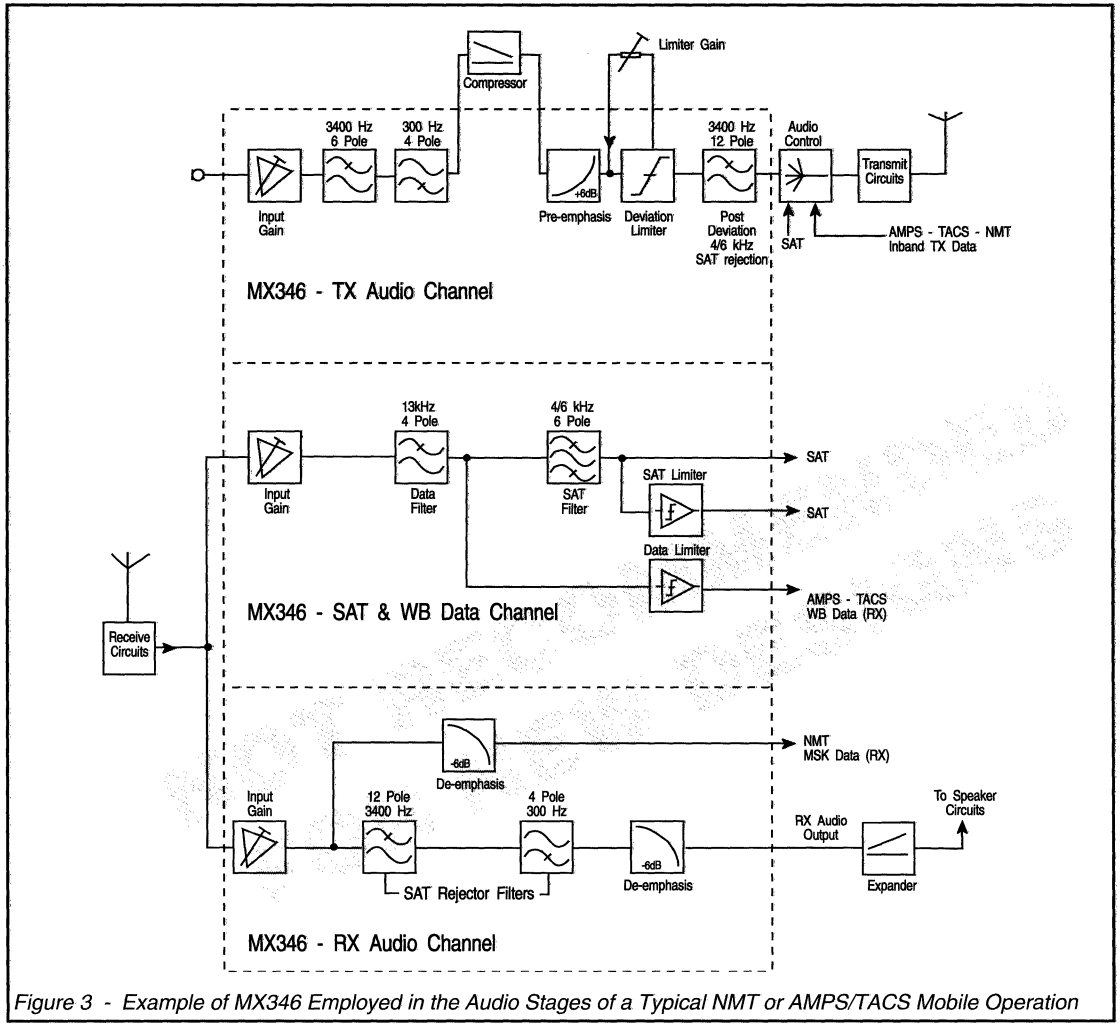


Figure 3 - Example of MX346 Employed in the Audio Stages of a Typical NMT or AMPS/TACS Mobile Operation

Table 1 (below) shows the signal and data path conditions relevant to the System Select and Chip Enable inputs. Note that the oscillator circuitry and V_{BIAS} line are active under all conditions.

FUNCTION				SIGNAL PATH			
	Oscillator	V_{BIAS}	TX Audio	SAT Tone	WB Data	RX Audio	RX Data
AMPS/TACS							
Chip Enable = "1"	Enabled	Enabled	Enabled	6kHz, Enabled	Enabled	Enabled	Enabled
Chip Enable = "0"	Enabled	Enabled	Disabled	Disabled	Enabled	Disabled	Disabled
NMT							
Chip Enable = "1"	Enabled	Enabled	Enabled	4kHz, Enabled	Enabled	Enabled	Enabled
Chip Enable = "0"	Enabled	Enabled	Disabled	Disabled	Disabled	Disabled	Enabled

Table 1 - Signal Path Selection

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 V to V_{DD} + 0.3 V
Sink/Source Current	
(supply pins)	±30mA
(other pins)	±20mA
Total Device Dissipation (@ 25°C)	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.

V_{DD}=5.0V

T_{AMB}=25°C

Xtal/Clock fo = 4.0 MHz

Audio level 0dB ref. = 300 mVrms

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage(V_{DD})		4.5	5.0	5.5	V
Input Logic "1"	3	3.5	-		V
Input Logic "0"	3	-	-	1.5	V
Supply Current	6				
- Enabled		-	-	15.0	mA
- Disabled (Chip Enable = 0)					
AMPS/TACS		-	-	2.5	mA
NMT		-	-	2.75	mA
Impedance					
Audio Amplifier Input		10.0	-	-	kΩ
Audio Op-Amp Output		-	6.0	10.0	kΩ
Audio Output		-	-	10.0	kΩ
Digital Input		100	1,000	-	kΩ
Digital Output		-	6.0	10.0	kΩ
Dynamic Values					
Xtal/Clock Frequency		-	4.0	-	MHz
Input Amplifier Gains		-	-	40.0	dB
TX Audio Channel					
Audio Input Level	1	-	300	-	mVrms
Overall Gain	1,7,8	-1.0	-	1.0	dB
Deviation Limiter Levels	3,5	1.0	-	4.0	V
Bandpass Frequency Range (-3dB)	8	300	-	3,400	Hz
Pre-emphasis:					
- Passband		300	-	3,400	Hz
- Response		-	6.0	-	dB/oct.
- Gain at 1kHz		-1.0	-	1.0	dB
- Passband Deviation from Ideal		-1.0	-	1.0	dB
Channel Stopband Attenuation					
≤160 Hz		-	-	-20	dB
≥5500 Hz		-	-	-35	dB
Output Noise		-	1.50	-	mVrms

Characteristics	See Note	Min.	Typ.	Max.	Unit
SAT and Wideband Data Channel					
Input Level	1	-	300	-	mVrms
Data Limiter Sensitivity	1,10				
- Limited SAT Tone (4 & 6 kHz)		-	10	-	mVrms
- Wideband Data		-	20	-	mVrms
13kHz Lowpass Filter					
- Passband (-3dB)		-	-	15.0	kHz
- Passband Gain (0 - 13kHz)		-1.0	-	1.0	dB
- Passband Ripple (0 - 13kHz)		-	2.0	-	dB
- Stopband Attenuation (≥25kHz)		-	30.0	-	dB
SAT Bandpass Filter					
NMT 4kHz -	4,9				
- Passband Frequency Range (-6dB)		3,800	-	4,200	Hz
- Passband Gain		-	11.5	-	dB
- Passband Ripple (4kHz ± 55Hz)		-	-	2.0	dB
- Stopband Attenuation (<2kHz, >6kHz)		-	-	-23.5	dB
- Output Noise	2	-	-	25	mVrms
- Aliasing Frequency		50.0	-	-	kHz
AMPS/TACS 6kHz	9				
- Passband Frequency Range (-6dB)		5,800	-	6,200	Hz
- Passband Gain		-	12.0	-	dB
- Passband Ripple (6kHz ± 55Hz)		-	2.0	3.0	dB
- Stopband Attenuation (<4kHz, >8kHz)		-	-	-21	dB
- Output Noise	2	-	7.5	-	mVrms
RX Audio Channel					
Input Level (RX Audio, RX Data)	1	-	300	-	mVrms
Gain 1,7,8	-2.0	-	+2.0	dB	
Passband Frequency Range (-3dB)	4	260	-	3,400	Hz
Output Noise	2	-	1.5	-	mVrms
RX Data Channel					
De-emphasis (Audio and Data)—					
- Passband		300	-	3,400	Hz
- Response		-	-6.0	-	dB/oct.
- Gain at 1kHz		-1.0	-	1.0	dB
- Passband Deviation from Ideal		-1.0	-	1.0	dB

Notes

1. With the Input Op-Amp gain(s) at unity.
2. Measured at the output with the channel input a.c. short circuit.
3. These levels are referenced to V_{DD}.
4. Specified over the full operating voltage and temperature range.
5. Limiter Input at V_{BIAS}.
6. To maintain low current consumption, buffers and clock filters are not included on-chip in series with outputs.
7. Input frequency is 1.0kHz.
8. With no pre-/de-emphasis effect.
9. Shows the SAT Tone Output specification in the selected mode.
10. The minimum level at the SAT Amp Input to produce a valid logic output.

Preliminary Information

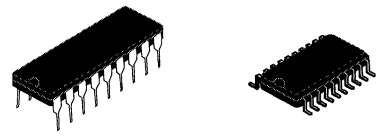
QUAD FILTER ARRAY

Features

- **Pair of Independent Lowpass Filters**
- **Pair of Audio Bandpass Filters (300-3000 Hz)**
- **Input Gain Adjustments**
- **Output Enable/Mute for Squelch Functions**
- **Low Power CMOS**

Applications

- **ACSB**
- **AMPS/TACS/N-AMPS**
- **Cellular Phones**



MX366P (PDIP)
18 Pins

MX366DW
20-Pin SOIC

DESCRIPTION

The MX366 Quad Filter Array is comprised of 4 separate filter/gain blocks on a single IC as described below:

1) A pair of 10th order 3.1 kHz lowpass filters.
2) A pair of 14th order channel bandpass filters (300-3000 Hz).
3) Op-amps that allow external components to set input gains and pre- or de-emphasis.
4) A buffered low noise output with switching clock filter.
5) Output-enabled switching circuitry for squelch control.

This simple, comprehensive amplifier/filter combination eliminates the need for several separate ICs, and therefore saves power and space.

The MX366 uses CMOS switched-capacitor filter technology and requires a supply of 4.5 V to 5.5 V to facilitate battery operation.

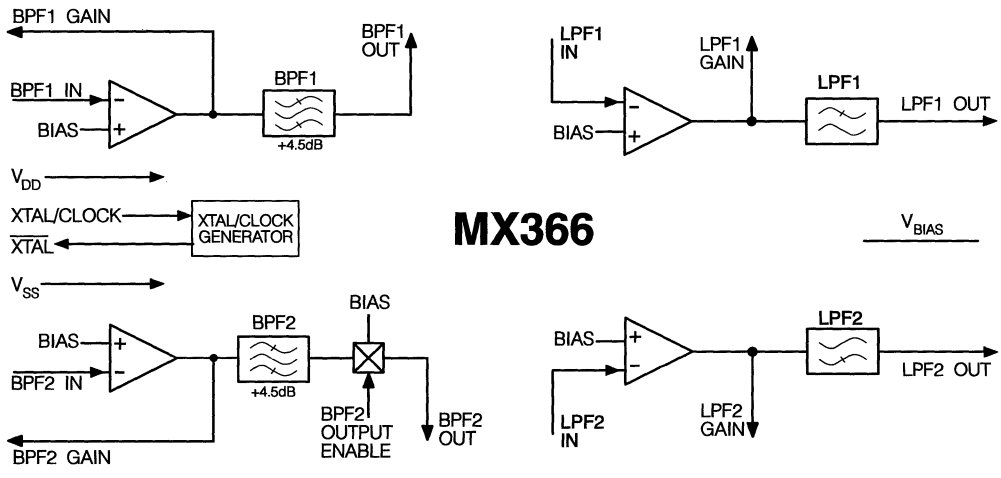
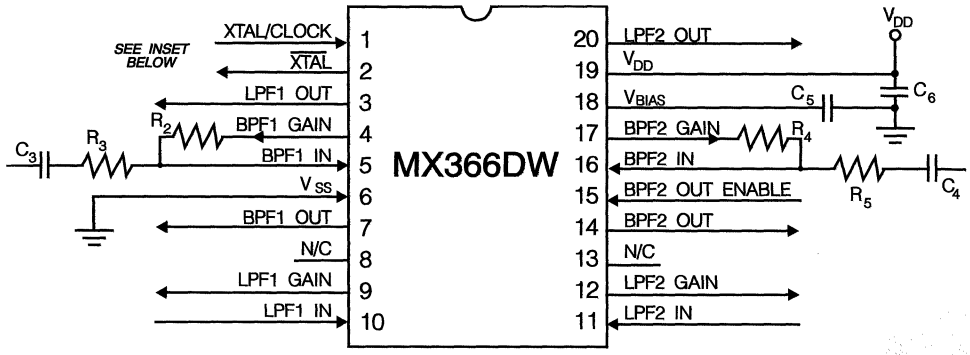
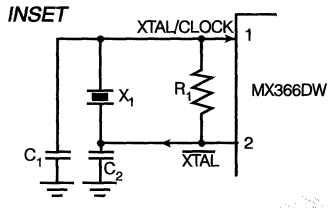


Figure 1 - Simplified Signal Paths





Component	Value
R1	100kΩ
C1	33pF
C2	47pF
C5	1.0µF
C6	0.47µF
X1	See Table 1

Tolerances: R = ±10%, C = ±20%

Notes: *1. R2, R3, C3, R4, R5 and C4 should be chosen with respect to the specific configuration used.*

2. Xtal circuitry shown is in accordance with MX-COM's Application Note on Crystal Oscillators (page 354 of the 1991 Product Handbook).

3. Operation of any MX-COM IC without a Xtal or clock may cause damage to the device. To minimize damage in the event of a Xtal/drive failure, a current limiting device (resistor fast-reaction fuse) should be installed on the power supply line (VDD).

Figure 2 - Recommended External Components

TABLE 1 - MX366 CRYSTAL FREQUENCY/FILTER RELATIONSHIP

Crystal Frequency	Bandpass Filter	Lowpass Filter
4.433619 MHz	300 - 3000 Hz	3100 Hz
4.40 MHz	298 - 2977 Hz	3076 Hz
4.096 MHz	277 - 2772 Hz	2864 Hz
4.032 MHz	272 - 2728 Hz	2819 Hz
4.00 MHz	270 - 2706 Hz	2797 Hz
3.579545 MHz	242 - 2422 Hz	2503 Hz

PIN FUNCTION CHART

Pin		Function
MX366J/P	MX366DW	
1	1	**Xtal/Clock:** A Xtal per Table 1 or an externally derived clock is injected at this pin.
2	2	**$\overline{\text{Xtal}}$:** This is the output of the clock oscillator inverter.
3	3	**LPF1 Out:** This is the output of the LPF1 filter/gain block.
4	4	**BPF1 Gain:** This is the output of the BPF1 gain-adjusting amplifier. This output is used with BPF1 In and external components.
5	5	**BPF1 In:** This is the input to the BPF1 filter/gain block.
6	6	**V_{SS}:** Negative supply (GND).
7	7	**BPF1 Out:** This is the output of BPF1.
	8	No Connect.
8	9	**LPF1 Gain:** This is the output of LPF1 gain-adjusting amplifier. This output is used with LPF1 Input and external components.
9	10	**LPF1 In:** This is the input to the LPF1 filter/gain block.
10	11	**LPF2 In:** This is the input to the LPF2 filter/gain block.
11	12	**LPF2 Gain:** This is the output of LPF2 gain-adjusting amplifier. This output is used with LPF2 Input and external components.
	13	No Connect.
12	14	**BPF2 Out:** This is the output of BPF2. It is under the control of the BPF2 Output Enable Input.
13	15	**BPF2 Output Enable**: This controls the status of BPF2 Out. Logic 1 = Enable, Logic 0 = Muted. This pin has an internal 1MΩ pullup resistor.
14	16	**BPF2 In**: This is the input to the BPF2 gain/filter block.
15	17	**BPF2 Gain**: This is the output of the BPF2 gain-adjusting amplifier. This output is used with BPF2 In and external components.
16	18	**Bias**: This is the analog bias line at $V_{DD}/2$. It should be coupled to V_{SS} by a 1.0 µF or greater capacitor.
17	19	**V_{DD}**: Positive supply. A single +5 volt power supply is required. Levels and voltages within this device are dependent upon this supply.
18	20	**LPF2 Out**: This is the output of LPF2.

The MX366 in a System

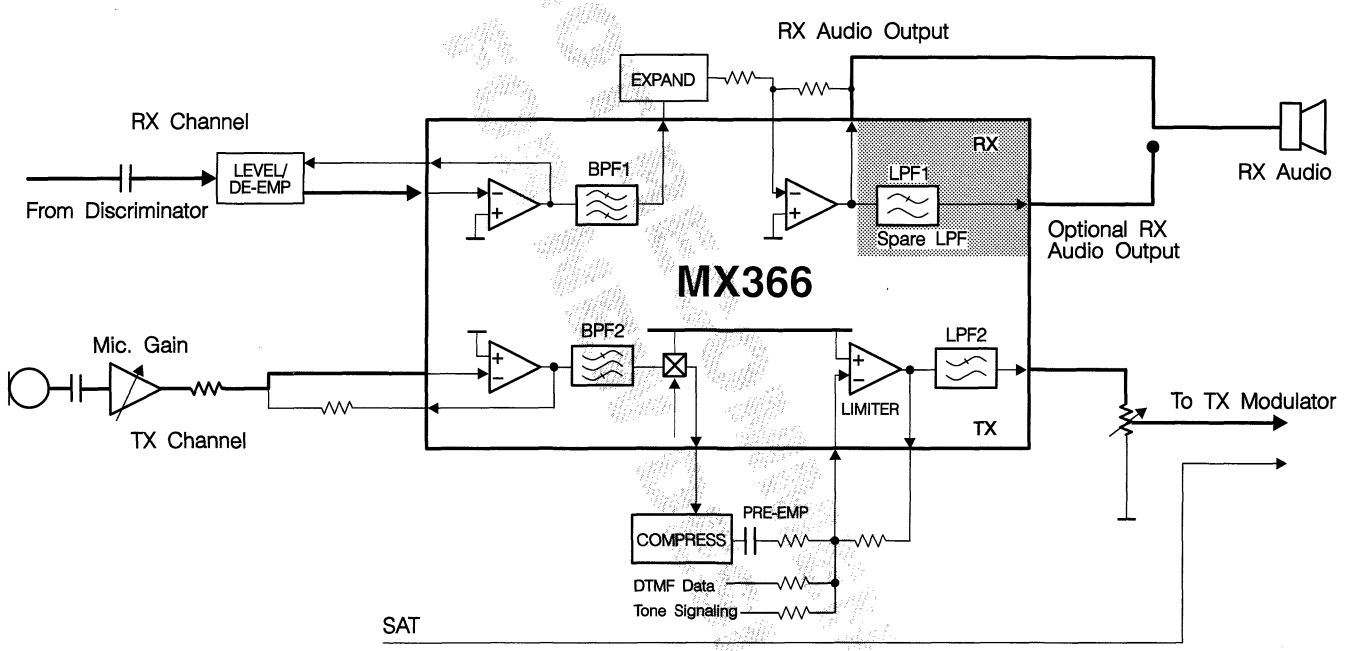


Figure 3 - Example of the MX366 Used in the Audio Stages of a TACS Operation

APPLICATION INFORMATION

Bandpass Section Performance

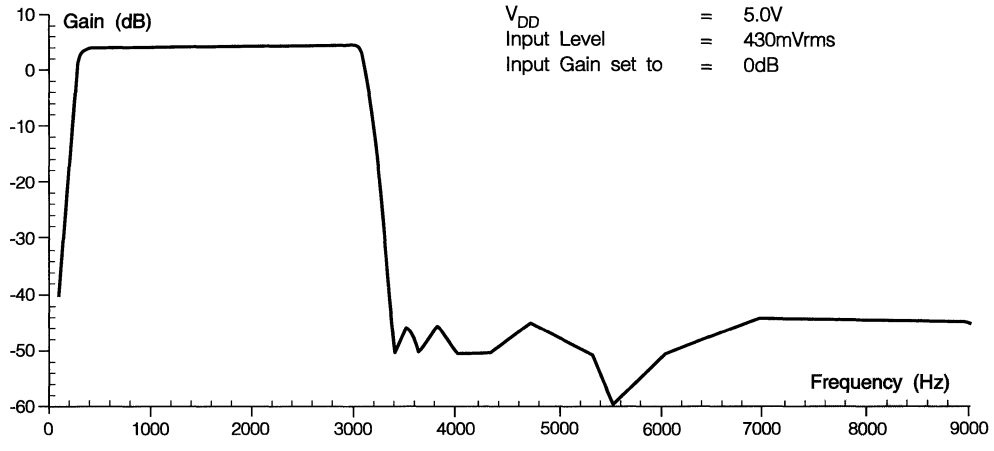


Figure 4 - Example of the MX366 Bandpass (BPF1/BPF2) Frequency Response

When using the MX366 Quad Filter Array within a cellular system, the following should be considered:

(1) Each bandpass filter section has a frequency range of 300 Hz to 3000 Hz and a typical passband gain of 4.5 dB.

(2) Each lowpass filter section has a cut-off frequency of 3100 Hz and a typical passband gain of 0.5 dB

(3) BPF2 Output Enable has an enable/disable operating time as shown in "Specifications."

Lowpass Section Performance

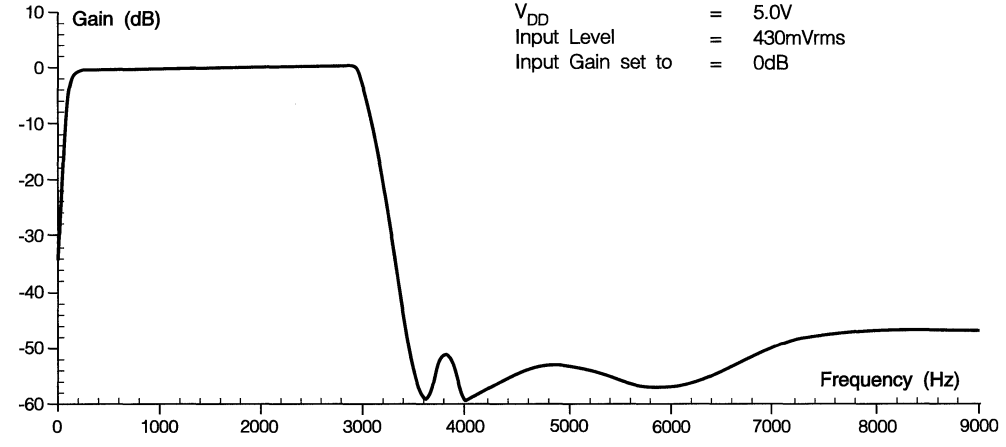


Figure 5 - Example of the MX366 Lowpass (LPF1/LPF2) Frequency Response

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (Ref. V_{SS} = 0V)	-0.3V to (V_{DD} + 0.3V)
Output sink/source current	
supply pins	±30mA
other pins	±20mA
Total Device Dissipation @ 25°C	800mW max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-40°C to +85°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0 V

T_{AMB} = 25°C

Clock = 4.433619 MHz

Audio Level 0dB Ref. = 775 mVrms @ 1 kHz

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current		-	5.0	8.5	mA
Input Impedance (Amplifiers)		1.0	10.0	-	MΩ
Input Impedance (Digital)		100	-	-	kΩ
Output Impedance (LP & BP Filters)		-	2.0	-	kΩ
On-Chip Xtal Oscillator					
R_{IN}		10.0	-	-	MΩ
R_{OUT}		-	10.0	-	kΩ
Inverter D.C. Voltage Gain		-	10.0	-	V/V
Gain/Bandwidth Product		-	10.0	-	MHz
Dynamic Values					
Input Logic 1 Voltage		3.5	-	-	V
Input Logic 0 Voltage		-	-	1.5	V
Analog Signal Input Levels					
Lowpass Filter		-30.0	-	4.5	dB
Bandpass Filter		-30.0	-	-1.5	dB
Analog Signal Output Levels					
Lowpass Filter		-29.5	-	5.0	dB
Bandpass Filter		-26.0	-	2.5	dB
Analog Output Noise	2	-	-50.0	-	dBp
Bandpass Filter	1,3				
Passband Frequencies		300	-	3000	Hz
Passband Ripple		-	±1.0	-	dB
Low Frequency Roll-off (<200 Hz)		12	-	-	dB/oct.
High Frequency Attenuation at 3.4 kHz		-	48.0	-	dB
Passband Gain		3.5	4.5	5.5	dB
BPF2 Output Enable Time		-	8.0	-	µs
BPF2 Output Disable Time		-	20.0	-	µs
Lowpass Filter	1,3				
Cut-off Frequency (-3dB)		-	3100	-	Hz
Passband Ripple (300 to 3000 Hz)		-	±1.0	-	dB
Attenuation at 3.3 kHz		-	30.0	-	dB
Attenuation at 3.6 kHz		-	45.0	-	dB
Passband Gain		-	0.5	-	dB
Distortion	1,4	-	2.0	-	%

NOTES:
1. Measured with Input Level -3.8 dB (500 mVrms).
2. Short circuit input, at any analog output and the measurement psophometrically weighted.
3. Op Amp gain 0 dB.
4. Measured in a 30 kHz bandwidth.

Preliminary Information

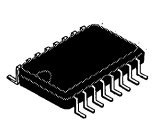
QUAD FILTER ARRAY

Features

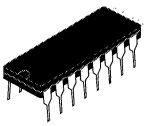
- **Pair of Independent Lowpass Filters**
- **Pair of Audio Bandpass Filters (300-3000 Hz)**
- **Input Gain Adjustments**
- **Low Power CMOS**

Applications

- **ACSB**
- **AMPS/TACS/N-AMPS**
- **Cellular Phones**



MX386DW
16-Pin SOIC



MX386P
16-pin PDIP

Description

The MX386 Quad Filter Array is comprised of 4 separate filter/gain blocks on a single IC as described below:

1) A pair of 10^{th} order 3.1 kHz lowpass filters.
2) A pair of 14^{th} order channel bandpass filters (300-3000 Hz).
3) Op-amps that allow external components to set input gains and pre- or de-emphasis.
4) A buffered low noise output with switching clock filter.

This simple, comprehensive amplifier/filter combination eliminates the need for several separate ICs, and therefore saves power and space.

The MX386 uses CMOS switched-capacitor filter technology and requires a supply of 4.5 V to 5.5 V to facilitate battery operation.

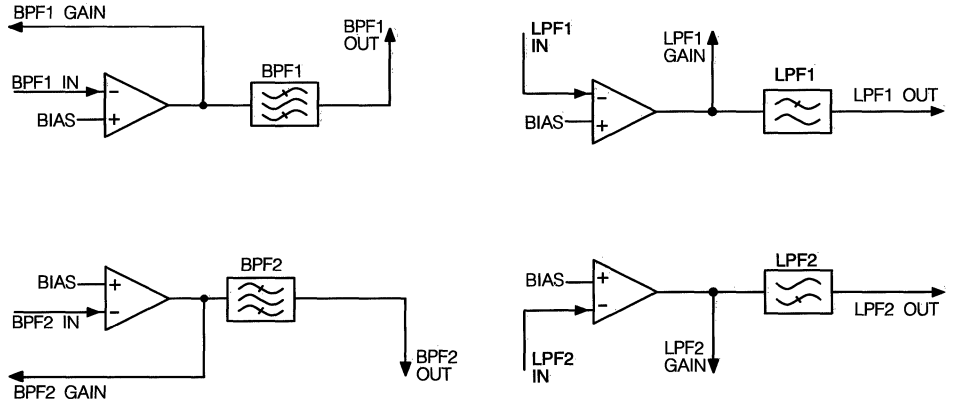
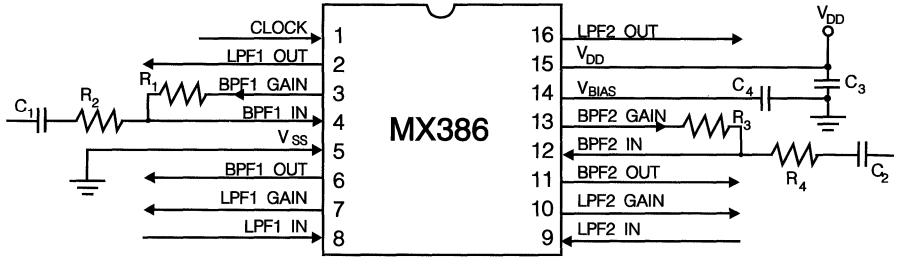


Figure 1 - Simplified Signal Paths



Component	Value
C3	0.47µF
C4	1.0µF

Tolerances: R = ±10%, C = ±20%

Notes:
1. *R1, R2, C1, R3, R4 and C2 should be chosen with respect to the specific application.*
2. *Operation of any MX-COM IC without a clock may cause damage to the device. To minimize damage in the event of a drive failure, the power supply line (VDD) should have a current limiting device (resistor fast-reaction fuse) installed.*

Figure 2 - Recommended External Components

4

TABLE 1 - MX386 CLOCK FREQUENCY/FILTER RELATIONSHIP

Clock Frequency	Bandpass Filter	Lowpass Filter
4.433619 MHz	300 - 3000 Hz	3100 Hz
4.40 MHz	298 - 2977 Hz	3076 Hz
4.096 MHz	277 - 2772 Hz	2864 Hz
4.032 MHz	272 - 2728 Hz	2819 Hz
4.00 MHz	270 - 2706 Hz	2797 Hz
3.579545 MHz	242 - 2422 Hz	2503 Hz

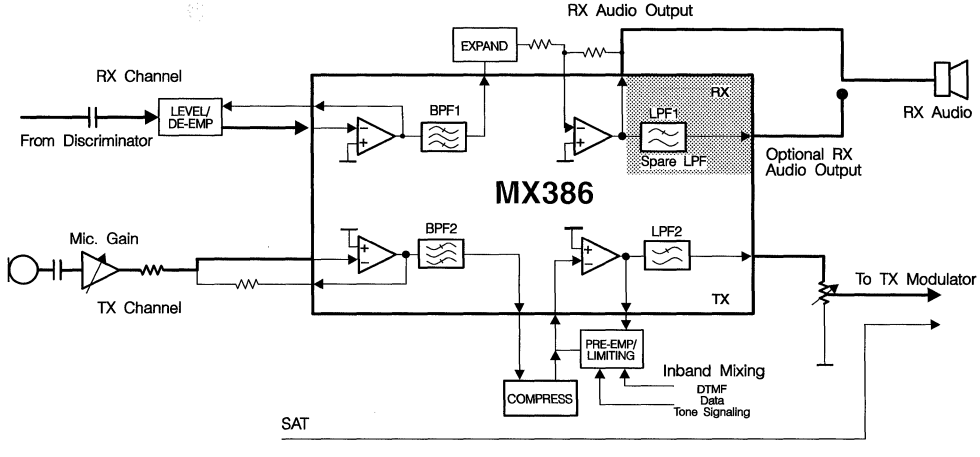


Figure 3 - Example of the MX386 in the Audio Stages of a TACS Operation

PIN FUNCTION CHART

Pin		Function
MX386P	MX386DW	
1	1	**Clock:** An externally derived clock (see Table 1) is injected at this pin.
2	2	**LPF1 Out:** This is the output of the LPF1 filter/gain block.
3	3	**BPF1 Gain:** This is the output of the BPF1 gain-adjusting amplifier. This output is used with BPF1 In and external components.
4	4	**BPF1 In:** This is the input to the BPF1 filter/gain block.
5	5	**V_{SS}:** Negative supply (GND).
6	6	**BPF1 Out:** This is the output of BPF1.
7	7	**LPF1 Gain:** This is the output of LPF1 gain-adjusting amplifier. This output is used with LPF1 Input and external components.
8	8	**LPF1 In:** This is the input to the LPF1 filter/gain block.
9	9	**LPF2 In:** This is the input to the LPF2 filter/gain block.
10	10	**LPF2 Gain:** This is the output of LPF2 gain-adjusting amplifier. This output is used with LPF2 Input and external components.
11	11	**BPF2 Out:** This is the output of BPF2.
12	12	**BPF2 In**: This is the input to the BPF2 gain/filter block.
13	13	**BPF2 Gain**: This is the output of the BPF2 gain-adjusting amplifier. This output is used with BPF2 In and external components.
14	14	**Bias**: This is the analog bias line at $V_{DD}/2$. It should be coupled to V_{SS} by a 1.0 µF or greater capacitor.
15	15	**V_{DD}**: Positive supply. A single +5 volt power supply is required. Levels and voltages within this device are dependent upon this supply.
16	16	**LPF2 Out**: This is the output of LPF2.

SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (Ref. V_{SS} = 0V)	-0.3V to (V_{DD} + 0.3V)
Output sink/source current	
supply pins	±30mA
other pins	±20mA
Total Device Dissipation @ 25°C	800mW max.
Derating	10mW/°C
Operating Temperature	-30°C to +70°C
Storage Temperature	-40°C to +85°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0 V

T_{AMB} = 25°C

Clock = 4.433619 MHz

Audio Level 0dB Ref. = 500 mVrms @ 1 kHz

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current		-	5.0	8.5	mA
Input Impedance					
Digital		100	-	-	kΩ
Amplifiers		1.0	10.0	-	MΩ
Output Impedance, LP & BP Filters		-	2.0	-	kΩ
On-Chip Xtal Oscillator					
R_{IN}		10.0	-	-	MΩ
R_{OUT}		-	10.0	-	kΩ
Inverter D.C. Voltage Gain		-	10.0	-	V/V
Gain/Bandwidth Product		-	10.0	-	MHz
Dynamic Values					
Input Logic 1 Voltage		70% V_{DD}	-	-	
Input Logic 0 Voltage		-	-	30% V_{DD}	
Analog Signal Input Levels					
Lowpass Filter		-26.0	-	8.5	dB
Bandpass Filter		-26.0	-	2.5	dB
Analog Signal Output Levels					
Lowpass Filter		-25.5	-	9.0	dB
Bandpass Filter		-22.0	-	6.5	dB
Analog Output Noise	2	-	-42.0	-	dB
Distortion	1	-	2.0	-	%
Lowpass Filter	1				
Cut-off Frequency (-3dB)		-	3100	-	Hz
Passband Ripple (300 to 3000 Hz)		-	±1.0	-	dB
Attenuation at 3.3 kHz		-	30.0	-	dB
Attenuation at 3.6 kHz		-	45.0	-	dB
Passband Gain		-	0.5	-	dB
Bandpass Filter	1,3				
Passband Frequencies		300	-	3000	Hz
Passband Ripple		-	±1.0	-	dB
Low Frequency Roll-off (<200 Hz)		12	-	-	dB/oct.
High Frequency Attenuation at 3.4 kHz		-	48.0	-	dB
Passband Gain		3.5	4.5	5.5	dB

NOTES:
1. Measured with Input Level -3 dB.
2. Short circuit input, any analog output, in 30 kHz bandwidth.
3. Op Amp gain 0 dB.

MX-COM, INC.

MX806A

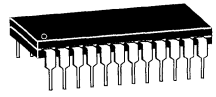
C-BUS COMPATIBLE

AUDIO PROCESSOR

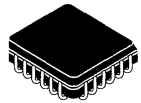
Description

The MX806A LMR audio processor is intended primarily to operate as the "Audio Terminal" of radio systems using the DBS 800 Digitally-integrated Baseband Sub-system.

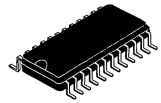
The MX806A half-duplex device has signal paths and level setting elements that are configured and adjusted by digital information sent from the radio microcontroller using C-BUS protocol. (C-BUS is the serial interface for all DBS 800 ICs.)



MX806AJ
24-pin CDIP



MX806ALH
24-lead PLCC



MX806ADW
24-pin SOIC

The signal path of the MX806A can be divided into three sections:

- **Input Process**
  This stage has selectable TX/RX paths. Transmit voice signals pass through microphone pre-amplifier, voltage controlled gain (VOGAD) and highpass filter stages. Received audio is de-emphasized. This initial audio, after in-line gain adjustment, may be switched to external audio processes (such as scrambling) or to the internal Main Process stages.
- **Main Process**
  Conditioning for the input or external process signals is completed in this stage. It is comprised of pre-emphasis, high and lowpass switched-capacitor filters and a deviation limiter.
- **Mixing and Output Drives**
  Main audio for transmission is mixed with signaling and data from external sources (other DBS 800 ICs) to provide the composite signal for the digitally adjustable transmitter modulation drives. Received audio level is adjusted for output to loudspeaker circuitry.

If selected, signal level stability and output accuracy of the MX806A is maintained by a voltage-controlled gain system using selectable signal-level detectors. Signal levels can be dynamically controlled to provide "dynamic compensation" for factors such as temperature drift, VCO non-linearity, etc.

MX806A audio output stages can be completely disabled - or the whole IC can be placed into powersave mode, leaving only clock and C-BUS circuitry active.

The MX806A is a low-power 5V CMOS integrated circuit. It is available in 24-pin CDIP and SMT packages.

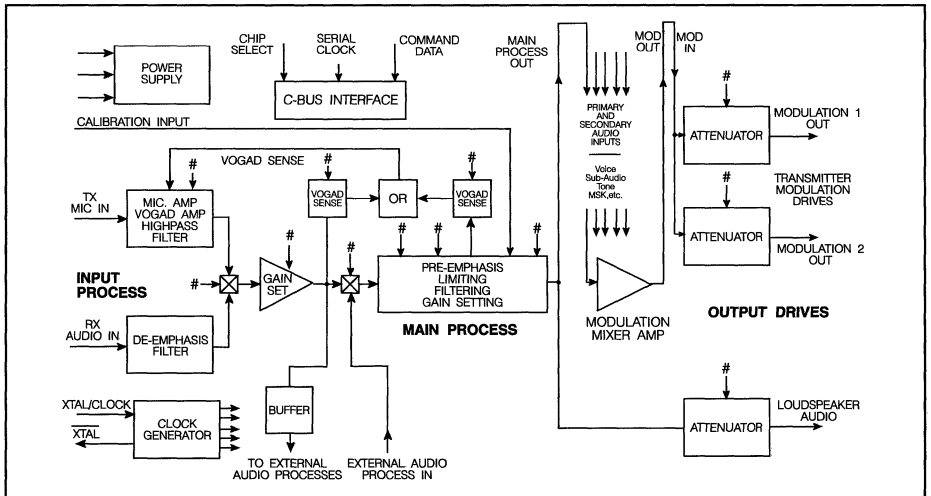


Figure 1 - MX806A Audio Processor

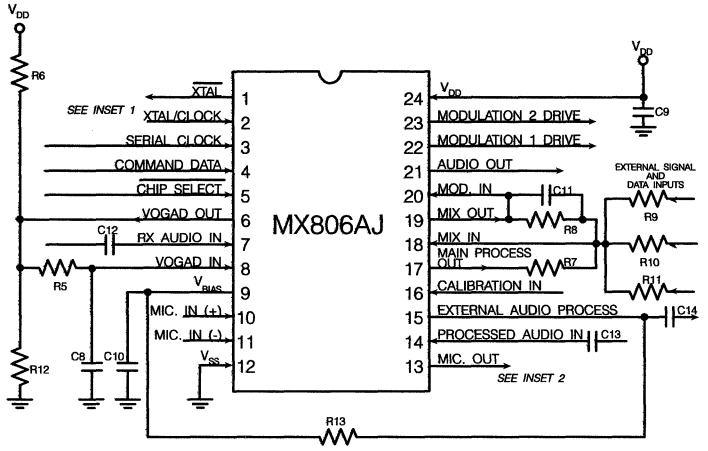
PIN FUNCTION CHART

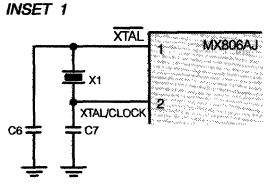
Pin	Function
1	**$\overline{\text{Xtal}}$:** The output of the 4.032 MHz on-chip clock oscillator. External components are required at this output when a Xtal is used. See Figure 2.
2	**Xtal/Clock:** The input to the on-chip 4.032 MHz clock oscillator inverter. A 4.032 MHz Xtal or externally derived clock should be connected here. See Figure 2. This clock provides timing for on-chip elements, filters, etc.
3	**Serial Clock:** The "C-BUS" serial data loading clock input. This clock, produced by the microcontroller, is used for transfer timing of Command Data to the Audio Processor. See Timing diagrams.
4	**Command Data:** The "C-BUS" serial data input from the microcontroller. Command Data is loaded to this device in 8-bit bytes, MSB (B7) first and LSB (B0) last, synchronized to the Serial Clock. The Command/Data instruction is acted upon at the end of loading the whole instruction. Command information is detailed in Tables 1 - 5. See Timing diagrams.
5	**$\overline{\text{Chip Select}}$ ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the microcontroller. Command Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Timing Diagrams.
6	**VOGAD Out:** The error-voltage output of the selected VOGAD sensor. This output, with external attack and decay setting components, should be connected as in Figures 2 and 3, to the VOGAD In pin.
7	**RX Audio In:** The audio input to the MX806A from the radio receiver's demodulator circuits. This input, which requires a.c. coupling with capacitor C_{12}, is selected via a Control Command bit.
8	**VOGAD In:** The gain control signal from the selected VOGAD sensor (VOGAD Out) to the Input Process voltage-controlled amplifier. The required sensor is selected via a Mode Command. The choice of two sensors enables gain control from either the Input Process or an External Process. External attack and decay setting components should be applied as recommended in Figures 2 and 3.
9	**V_{BIAS}:** The output of the on-chip analog circuitry bias system, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C_{10}. See Figure 2.
10	**Mic In (+):** The non-inverting input to the microphone Op-Amp. This input requires external components for Op-Amp gain/attenuation setting as shown in Figure 2.
11	**Mic In (-):** The inverting input to the microphone Op-Amp. This input requires external components for Op-Amp gain/attenuation setting as shown in Figure 2.
12	**V_{SS}:** Negative supply (GND).

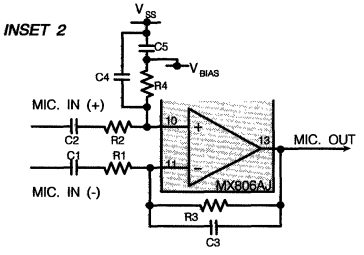
PIN FUNCTION CHART

Pin	Function
13	**Mic Out:** The output of the Microphone Op-Amp, used with the Mic In (-) input to provide the required gain/attenuation using external components as shown in Figure 2. The external components shown are to assist in the use of this amplifier with either inverting or non-inverting inputs. During Powersave (Volume Command) this output is placed at V_{SS}.
14	**Processed Audio In:** The input to the device from such external audio processes as Voice Store and Retrieve or Frequency Domain Scrambling. This input, which requires a.c. coupling with capacitor C_{13}, is selected by a Mode Command bit.
15	**External Audio Process:** The buffered output of the Input Processing Stage. Its purpose is to further external audio processing stages prior to re-introduction at the Processed Audio In pin.
16	**Calibration Input:** A unique audio input to be used for dynamic balancing of the modulator drives and for measuring Deviation Limiter levels. A CUE (beep) input from the MX803 Audio Tone Processor can be entered on this line. This audio input must be externally biased. It is selected via a Mode Command bit.
17	**Main Process Out:** The output of the Main Process stage. This output should be mixed with any additional system audio inputs (Audio, Sub-Audio Signaling, MSK) in the on-chip Modulation Summing Amplifier. External components shown in Figure 2 should be used as required.
18	**Sum In:** The input and output terminals of the on-chip Modulation Summing Amplifier. External components are required for input signals and gain/attenuation setting as shown in Figure 2. For single-signal, no-gain requirements, Main Process Out may be linked directly to Modulation In.
19	**Sum Out:**
20	**Modulation In:** The final, composite modulating signal to VCO (Mod 1) and Reference (Mod 2) Output Drives.
21	**Audio Output**: The processed audio signal output intended as a received audio (volume) output. Though normally used in the RX mode, operation in TX is permitted. The output level of this attenuator is controlled via a Volume Set command. During Powersave this output is placed at V_{SS}.
22	**Modulation 1 Drive:** The drive to the radio modulator Voltage Controlled Oscillator (VCO) from the composite audio summing stage.
23	**Modulation 2 Drive:** The drive to the radio modulator Reference Oscillator from the composite audio summing stage. NOTE: These VCO output attenuators are individually adjustable using the Modulator Level command. During Powersave these outputs are placed at V_{SS}.
24	**V_{DD}:** Positive supply. A single, stable +5 volt supply is required. Levels and voltages within this Audio Processor are dependent upon this supply.

Analog Application Information







Component	Value	Component	Value	Component	Value
R_1	10kΩ	R_{10}	100kΩ	C_6	33pF
R_2	10kΩ	R_{11}	100kΩ	C_7	5-65pF
R_3	20kΩ	R_{12}	2.2MΩ	C_8	1.0µF
R_4	20kΩ	R_{13}	470kΩ	C_9	1.0µF
R_5	10kΩ	C_1	.47µF	C_{10}	1.0µF
R_6	2.2MΩ	C_2	.47µF	C_{11}	22pF
R_7	100kΩ	C_3	270pF	C_{12}	0.1µF
R_8	100kΩ	C_4	270pF	C_{13}	0.01µF
R_9	100kΩ	C_5	0.1µF	C_{14}	0.01µF
				X_1	4.0MHz

Figure 2 - Recommended External Components

Tolerance: R=±10%. C=±20%.

Notes:

Input Op-Amp gain/attenuation components (voltage gain = 6.0dB) are shown in Inset 1 in a differential configuration to demonstrate the versatility of this input. Components for a single (+ or -) input may be used.

Resistor values R_7 to R_{11} (summation components) are dependent upon application and configuration requirements.

Xtal circuit capacitors C_6 (C_D) and C_7 (C_G) shown in Inset 2 are recommended in accordance with MX-COM's Crystal Oscillator Application Note, March 1990. Circuit drive and drain resistors are incorporated on-chip. Operation of any MX-COM IC without a Xtal or clock input may cause device damage. To minimize damage in the event of a Xtal/drive failure, you should install a current limiting device (resistor or fast-reaction fuse) on the power input (V_{DD}).

Analog Application Information

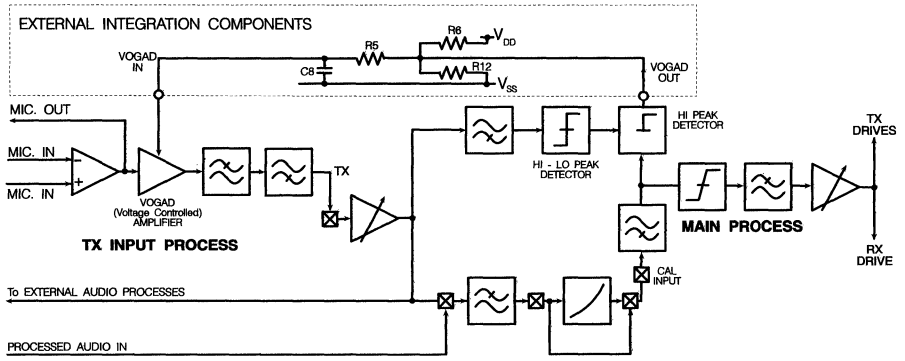


Figure 3 - VOGAD Sensors and Timing Components (from Fig. 5)

The overall Gain Control system of the MX806A consists of 2 selectable signal peak detectors whose output is fed via external integrating components to adjust the gain of the Voltage Controlled Amplifier positioned in the TX Input Process Path. The transmit input signal is presented to Peak Detector 1 or 2. The Peak Detectors are enabled individually by a Mode command. When the input signal exceeds the peak-to-peak threshold of the detector, a 5 volt level is produced at the VOGAD Out pin. This level remains for as long as the signal exceeds the threshold. The integrated level to the VOGAD In pin causes the Voltage Controlled Amplifier gain to be reduced. As can be seen from Figures 3 and 5, Peak Detector 1 allows control of the audio level to the external audio process and Peak Dector 2 allows control of transmit deviation levels.

VOGAD attack and decay times are set using the external components shown in Figures 2 and 3. They are calculated as described below.

4

VOGAD Components Calculations - Figures 2 and 5

Provided $R_5 >> 1.0k\Omega$ and $R_6 = R_{12} >> R_5$

Then

$$\text{Attack Time } (T_A) = R_5 \times C_8$$

$$\text{Decay Time } (T_D) = \frac{R_6 \times C_8}{2}$$

Suggested Calibration Methods

To effectively null all internal IC tolerances, the following initial calibration routine is suggested:

TX Calibration: From Mic. In to Modulator Drives Out

Disable Peak Detectors (Mode Command).
Set Transmitter Drives to 0dB (Mod. Levels Set).
Pre-emphasis may be employed as required (Control Command).
Set Input Level Amp to 0dB (Control Command).

1) Mic. In = 250 mVrms at 1kHz. Set Process Gain Amp for output of 1440 mV p-p (100% deviation).
2) With Process Gain Amp set as 1 and with Mic. In = 25 mVrms at 1 kHz, set the Input Level Amp for an output level of 308 mVrms (60% deviation).

RX Calibration: From RX Audio In to Audio Out

Set Audio Output Drive to 0dB (Volume Set)
Leave Process Gain Amp set as 1 (see above).
3) With an RX Audio In level of between 154 mVrms and 308 mVrms (see Specifications) at 1 kHz, set the Input Level Amp for an output level of 308 mVrms.

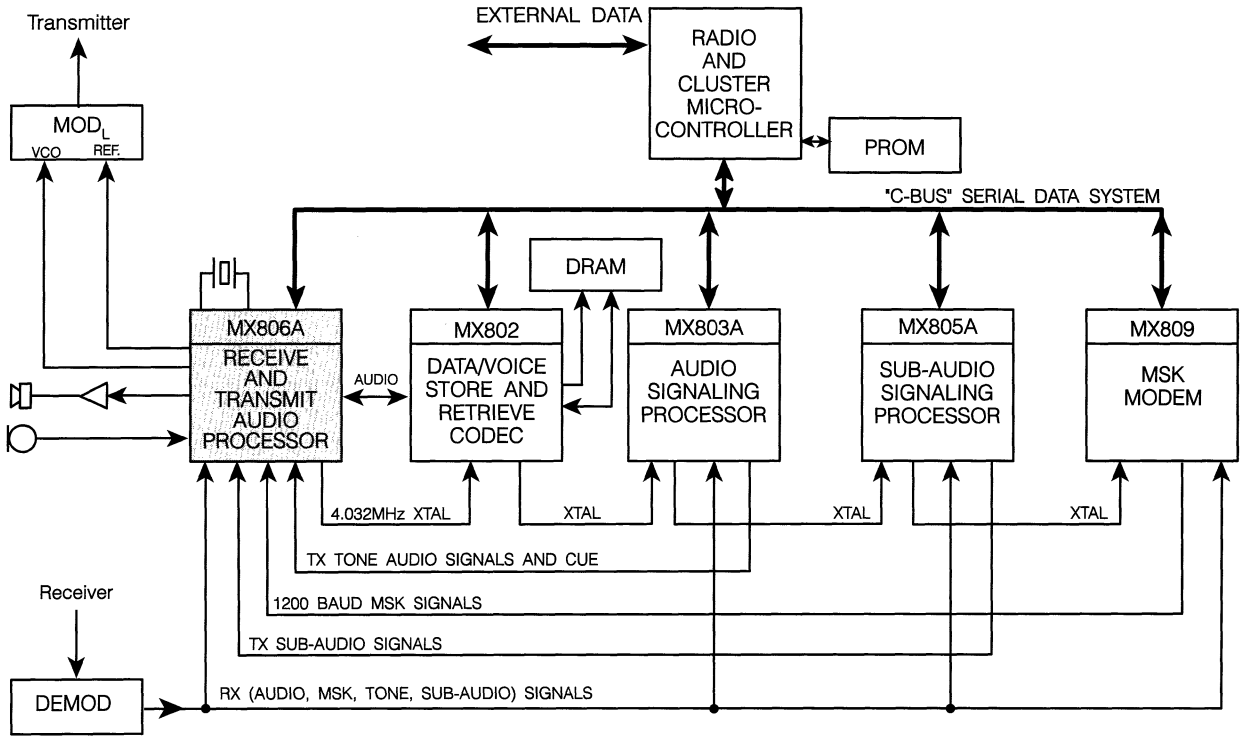


Figure 4 - MX806A Interfaced with Other DBS800 Elements

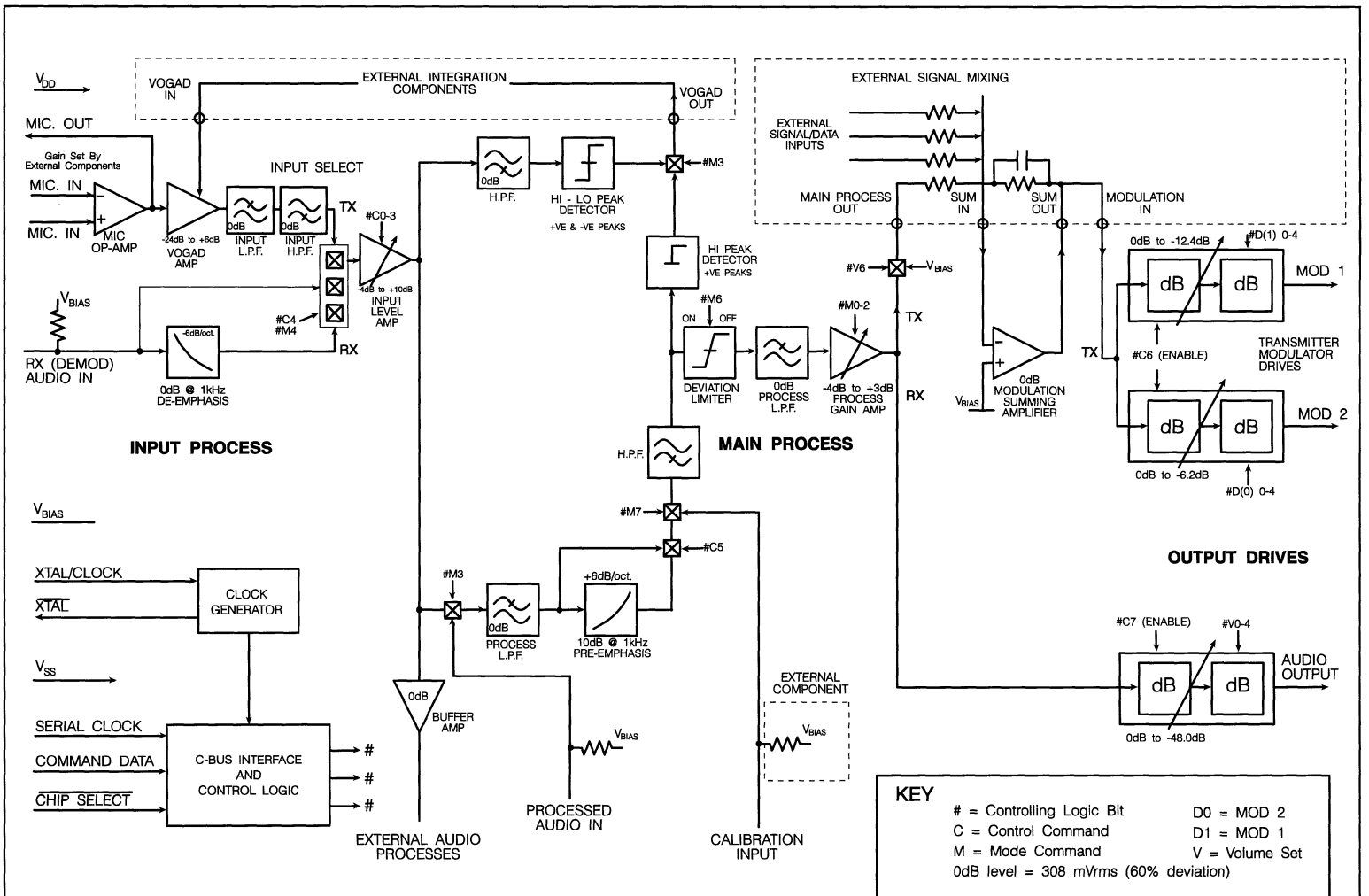


Figure 5 - LMR Audio Processor Explanatory Block Diagram

Controlling Protocol

Control of the functions and levels within the MX806A LMR Audio Processor is by a group of Address/Commands and appended data instructions from the system microcontroller. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Hex.	Address/Command Binary MSB LSB		Command Data	Table
General Reset	01	0 0 0 0 0 0 0 1			
Control Command	10	0 0 0 1 0 0 0 0	+	1 byte	2
Mode Command	11	0 0 0 1 0 0 0 1	+	1 byte	3
Mod. Levels Set	12	0 0 0 1 0 0 1 0	+	2 bytes	4
Volume Set	13	0 0 0 1 0 0 1 1	+	1 byte	5

Table 1 - C-BUS Address/Commands

In "C-BUS" protocol the MX806A is allocated Address/Command values 10_H to 13_H. C-BUS Command, Mode, Modulation and Volume assignments and data requirements are given in Table 1 and illustrated in Figure 5.

Commands and Data are only to be loaded in the group configurations detailed since the "C-BUS" interface recognizes the first byte after Chip Select (logic"0") as an Address/Command.

Function or Level control data, which is detailed in Tables 2, 3, 4, and 5, is acted upon at the end of the loaded instruction.

Upon power-up the value of the "bits" in this device will be random (either "0" or "1"). A General Reset Command (01_H) is required. This command is provided to "reset" all devices on the Command Data line and has the following effect on the MX806A:

Control Address Command	Loaded as 00_H
Mode Address Command	Loaded as 00_H
Volume Set	Loaded as 00_H

Control Command *(Preceded by A/C 10_H)*

Setting	Control Bits
(MSB) Bit 7	**Audio Output (RX)**
0	Disabled
1	Enabled
6	**Modulation Drives**
0	Disabled
1	Enabled
5	**Pre-Emphasis**
0	Bypass
1	Enabled
4	**Input Select**
0	RX In
1	Mic. In
3 2 1 0	**Input Level Set**
0 0 0 0	Input Amp Disabled
0 0 0 1	-4.0dB
0 0 1 0	-3.0dB
0 0 1 1	-2.0dB
0 1 0 0	-1.0dB
0 1 0 1	0dB
0 1 1 0	1.0dB
0 1 1 1	2.0dB
1 0 0 0	3.0dB
1 0 0 1	4.0dB
1 0 1 0	5.0dB
1 0 1 1	6.0dB
1 1 0 0	7.0dB
1 1 0 1	8.0dB
1 1 1 0	9.0dB
1 1 1 1	10.0dB

Table 2 - Control Commands

Mode Command *(Preceded by A/C 11_H)*

Setting	Mode Bits
(MSB) Bit 7	**Drive Source**
0	Signals
1	Calibration
6	**Deviation Limiter**
0	Disabled
1	Enabled
5	**VOGAD**
0	Disabled
1	Enabled
4	**De-Emphasis**
0	Enabled
1	Bypassed
3	**Signal Select**
0	Internal
1	External
2 1 0	**Process Gain Set**
0 0 0	-4.0dB
0 0 1	-3.0dB
0 1 0	-2.0dB
0 1 1	-1.0dB
1 0 0	0dB
1 0 1	1.0dB
1 1 0	2.0dB
1 1 1	3.0dB

Table 3 - Mode Commands

Modulator Levels *(Preceded by A/C 12_H)*

Setting	Modulator Drives
Byte 1 (MSB)	***First byte for transmission***
7 6 5	
0 0 0	Must be "0"
4 3 2 1 0	**VCO Drive Attenuation**
0 0 0 0 0	12.4dB
0 0 0 0 1	12.0dB
0 0 0 1 0	11.6dB
0 0 0 1 1	11.2dB
0 0 1 0 0	10.8dB
0 0 1 0 1	10.4dB
0 0 1 1 0	10.0dB
0 0 1 1 1	9.6dB
0 1 0 0 0	9.2dB
0 1 0 0 1	8.8dB
0 1 0 1 0	8.4dB
0 1 0 1 1	8.0dB
0 1 1 0 0	7.6dB
0 1 1 0 1	7.2dB
0 1 1 1 0	6.8dB
0 1 1 1 1	6.4dB
1 0 0 0 0	6.0dB
1 0 0 0 1	5.6dB
1 0 0 1 0	5.2dB
1 0 0 1 1	4.8dB
1 0 1 0 0	4.4dB
1 0 1 0 1	4.0dB
1 0 1 1 0	3.6dB
1 0 1 1 1	3.2dB
1 1 0 0 0	2.8dB
1 1 0 0 1	2.4dB
1 1 0 1 0	2.0dB
1 1 0 1 1	1.6dB
1 1 1 0 0	1.2dB
1 1 1 0 1	0.8dB
1 1 1 1 0	0.4dB
1 1 1 1 1	0dB
Byte 0 (MSB)	***Last byte for transmission***
7 6 5	
0 0 0	Must be "0"
4 3 2 1 0	**VCO (Ref.) Drive Attenuation**
0 0 0 0 0	6.2dB
0 0 0 0 1	6.0dB
0 0 0 1 0	5.8dB
0 0 0 1 1	5.6dB
0 0 1 0 0	5.4dB
0 0 1 0 1	5.2dB
0 0 1 1 0	5.0dB
0 0 1 1 1	4.8dB
0 1 0 0 0	4.6dB
0 1 0 0 1	4.4dB
0 1 0 1 0	4.2dB
0 1 0 1 1	4.0dB
0 1 1 0 0	3.8dB
0 1 1 0 1	3.6dB
0 1 1 1 0	3.4dB
0 1 1 1 1	3.2dB
1 0 0 0 0	3.0dB
1 0 0 0 1	2.8dB
1 0 0 1 0	2.6dB
1 0 0 1 1	2.4dB
1 0 1 0 0	2.2dB
1 0 1 0 1	2.0dB
1 0 1 1 0	1.8dB
1 0 1 1 1	1.6dB
1 1 0 0 0	1.4dB
1 1 0 0 1	1.2dB
1 1 0 1 0	1.0dB
1 1 0 1 1	0.8dB
1 1 1 0 0	0.6dB
1 1 1 0 1	0.4dB
1 1 1 1 0	0.2dB
1 1 1 1 1	0dB

Table 4 - Modulator Drive Levels

Volume Set *(Preceded by A/C 13_H)*

Setting	Volume Set
(MSB) 7 6	**Main Process Out**
0 0	Enabled
0 1	Biased
5	**Powersave**
0	Chip Enabled
1	Powersaved
4 3 2 1 0	**Volume Set Attenuation**
0 0 0 0 0	Off
0 0 0 0 1	48.0dB
0 0 0 1 0	46.4dB
0 0 0 1 1	44.8dB
0 0 1 0 0	43.2dB
0 0 1 0 1	41.6dB
0 0 1 1 0	40.0dB
0 0 1 1 1	38.4dB
0 1 0 0 0	36.8dB
0 1 0 0 1	35.2dB
0 1 0 1 0	33.6dB
0 1 0 1 1	32.0dB
0 1 1 0 0	30.4dB
0 1 1 0 1	28.8dB
0 1 1 1 0	27.2dB
0 1 1 1 1	25.6dB
1 0 0 0 0	24.0dB
1 0 0 0 1	22.4dB
1 0 0 1 0	20.8dB
1 0 0 1 1	19.2dB
1 0 1 0 0	17.6dB
1 0 1 0 1	16.0dB
1 0 1 1 0	14.4dB
1 0 1 1 1	12.8dB
1 1 0 0 0	11.2dB
1 1 0 0 1	9.6dB
1 1 0 1 0	8.0dB
1 1 0 1 1	6.4dB
1 1 1 0 0	4.8dB
1 1 1 0 1	3.2dB
1 1 1 1 0	1.6dB
1 1 1 1 1	0dB

Table 5 - Volume Set

Notes

Command Loading: Address/Commands and data bytes must be loaded in accordance with the information given in Figure 6.

The **Powersave** function is enabled by bit 5 of the Volume Set Command (Table 5).

During Powersave all internal elements except the Clock Generator and "C-BUS" interface are off. The Mic Op-Amp and Output Drive stage outputs are connected to V_{SS}.

Modulator Drives are controlled separately, but the whole two-byte Modulator Drive command must be loaded for each requirement adjustment.

$\overline{\text{Chip Select}}$ must be held at a logic "1" for the period "t_{CSOFF}" between transactions.

Timing Information

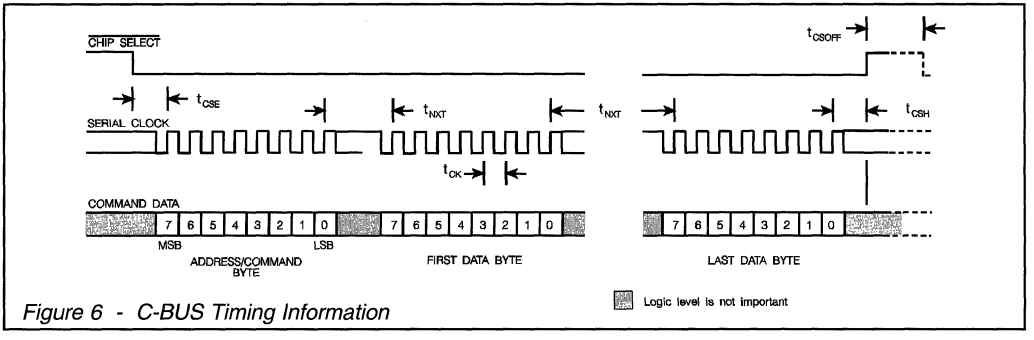


Figure 6 - C-BUS Timing Information

Parameter	Abbreviation	Min.	Typ.	Max.	Unit
"$\overline{CS}$ Enable" to "clock high"	t_{CSE}	2.0	-	-	µs
Last "clock high" to "CS high"	t_{CSH}	4.0	-	-	µs
"$\overline{CS}$ high" time between transactions	t_{CSOFF}	2.0	-	-	µs
Inter byte time	t_{NXT}	4.0	-	-	µs
Serial Clock Period	t_{CK}	2.0	-	-	µs

Notes
Command data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last.
Data is clocked into the peripheral on the rising clock edge.
Loaded data instructions are acted upon at the end of each individual, loaded byte.
To allow for different microcontroller serial interface formats, the MX806A is able to work with either polarity Serial Clock pulses.

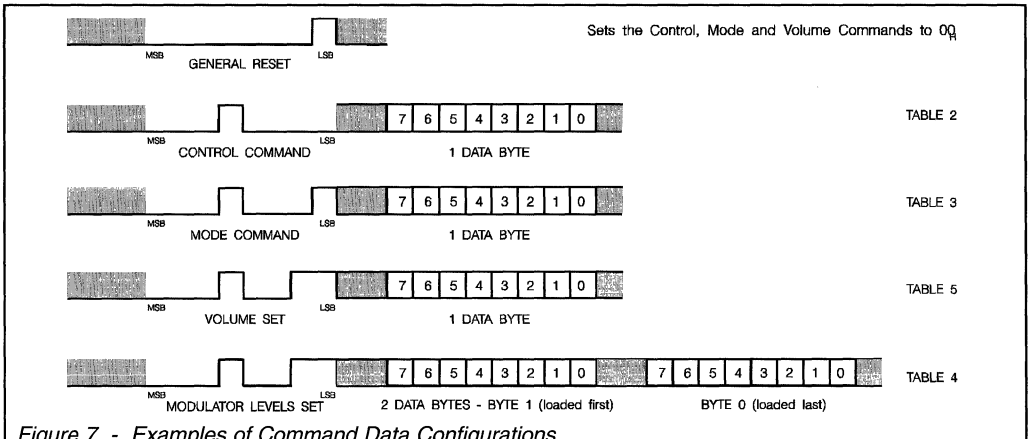


Figure 7 - Examples of Command Data Configurations

Application Information
To assist in rapid setting, this quick-reference list should be used with Figure 5.

Control	A/C = 10_H
7	Audio Out (RX) Enable
6	Modulator Drive Enable
5	Pre-Emphasis Select
4	Input Select (RX/TX)
3-0	Input Level Set (-4dB to 10dB)

Mode	A/C = 11_H
7	Drive Source
6	Deviation Limiter Enable
5	VOGAD Enable
4	De-Emphasis Enable
3	Signal Select
2-0	Process Gain Set (-4dB to 3dB)

Modulator Levels	A/C = 12_H
Byte1	
7-5	"0"
4-0	Mod 1 Attenuation (0 to 12.4dB)
Byte 2	
7-5	"0"
4-0	Mod 2 Attenuation (0 to 6.2dB)

Volume Set	A/C = 13_H
7-6	"0"
5	Powersave
4-0	Volume Set Attenuation (0 to 48dB)

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin	
(ref V_{SS} = 0V)	-0.3 to (V_{DD}+0.3V)
Sink/source current	
(supply pins)	±30mA
(other pins)	±20mA
Total device dissipation	
@ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/Clock f_0 = 4.0MHz

Audio Level 0dB ref = 308mVrms @ 1kHz
(60% deviation, FM)

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current (All elements enabled)		-	8.0	15.0	mA
(Maximum Powersave)		-	.7	1.5	mA
"C-BUS" Interface					
Input Logic "1"	3.5	-	-	V	
Input Logic "0"	-	-	1.5	V	
Input Current		-1.0	-	1.0	µA
Input Capacitance		-	-	7.5	pF
Overall Performance					
Microphone Input Level	1,2		25		mVrms
Discriminator Input Level	2,3	154	-	308	mVrms
Output Drive Level					
(60% deviation)	2,4	291	308	326	mVrms
(100% deviation)	2,4,5	-	1440	-	mV pk-pk
Passband	6	297	-	3000	Hz
Passband Ripple	7	-2	-	0.5	dB
Stopband Attenuation	6,8				
@150Hz		10	12	-	dB
@3400Hz		-	2	-	dB
@6000Hz		30	36	-	dB
@8000 to 20,000 Hz		-	60	-	dB
Signal Path Noise TX		-	-50	-	dBp
	9	-	-45	-	dB
RX		-	-60	-	dB
	9	-	-55	-	dB
Total Harmonic Distortion					
(RX or TX, 60% deviation)		-	1.0	-	%
Circuit Elements - Figure 5					
Mic. Amp or Mod. Summation Amp					
Open Loop Gain		-	50.0	-	dB
Bandwidth		20.0	-	-	kHz
Input Impedance		10.0	-	-	MΩ
Output Impedance (Open Loop)		-	6.0	-	kΩ
(Closed Loop)		-	600	-	Ω
De-emphasis					
Slope		-	-6.0	-	dB/oct.
Gain (at 1.0kHz)		-	0	-	dB
Input Impedance		-	1	-	MΩ
Voltage Controlled Gain Amp (VOGAD)					
Gain (Non-Compressing)	2	-	6.0	-	dB
(Full Compression)		-	-24	-	dB

Characteristics	See Note	Min.	Typ.	Max.	Unit
Input Impedance		10.0	-	-	MΩ
VOGAD Peak Detectors					
Output Impedance Logic "1" (Compress)		-	1	-	kΩ
Logic "0"		-	10	-	MΩ
Hi/Lo Peak Detector Threshold	10	-	1,300	-	mV p-p
Hi Peak Detector Threshold	10	-	650	-	mV+ve pk
Input (Low + Highpass) Filter					
Gain (at 1.0 kHz)		-1.0	0	1.0	dB
Input Level Amp					
Gain Range		-	0	-	dB
Overall Tolerance		-1.0	-	1.0	dB
Step Size		0.75	1.0	1.25	dB
External Audio Buffer					
Gain		-0.1	0	0.1	dB
Pre-emphasis (Main Process and VOGAD)					
Slope		-	6.0	-	dB/oct.
Gain (at 1.0kHz)		-	10.0	-	dB
Process Highpass Filter					
Gain (at 1.0 kHz)		-0.1	0	0.1	dB
Deviation Limiter					
Threshold		708	1300	1413	mVrms
Gain		-0.5	-	0.5	dB
Process Lowpass Filter					
Gain (at 1.0 kHz)		-0.1	0	0.1	dB
Process Gain Amp					
Gain Range		-4.0	-	3.0	dB
Overall Tolerance		-0.5	-	0.5	dB
Step Size		0.75	1.0	1.25	dB
Output Impedance		-	600	-	Ω
Transmitter Modulator Drives					
Input Impedance		-	15.0	-	kΩ
Mod. 1 Attenuator					
Attenuation Range		0	-	12.4	dB
Overall Tolerance		-1	-	1	dB
Step Size		0.2	0.4	0.6	dB
Output Impedance		-	600	-	Ω
Mod. 2 Attenuator					
Attenuation Range		0	-	6.2	dB
Overall Tolerance		-0.5	-	0.5	dB
Step Size		0.1	0.2	0.3	dB
Output Impedance		-	600	-	Ω
Audio Output Attenuator					
Attenuation Range		0	-	48.0	dB
Overall Tolerance		-1.0	-	1.0	dB
Step Size		1.1	1.6	2.1	dB
Output Impedance		-	600	-	Ω
Miscellaneous Impedances					
Processed Audio Input		-	500	-	kΩ
Calibration Input		-	500	-	kΩ
External Process Out		-	100	-	Ω
RX with De-emphasis Bypass		-	25.0	-	kΩ

Notes

1. Producing an output of 0dB with the Mic. Op-Amp set to 6dB (as shown in Figure 2) and the Modulator Drives set to 0dB.
2. With Output Drives set to 0dB and the system calibrated as described in the Application Notes.
3. Input level range for 0dB output, by adjustment of the Input Level Amp.
4. It is recommended that these output levels will produce 60% or 100% deviation in the transmitter.
5. With the microphone input level 20dB above the level required to produce 0dB at the Output Drives.
6. Between Microphone or RX inputs to Modulator or Audio Outputs.
7. Deviation from the ideal overall response including the pre- or de-emphasis slope.
8. Excluding the effect of pre- or de-emphasis slope.
9. In a 30kHz bandwidth.
10. Using pre-emphasis in the TX path.

MX•COM, INC.

Preliminary Information

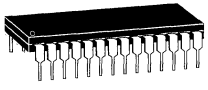
MX816

C-BUS COMPATIBLE

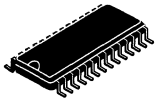
NMT AUDIO PROCESSOR

Features

- **Full-Duplex Audio Processing for NMT Cellular System**
- **On-Chip Speech and SAT Abilities**
  TX/RX/SAT Filtering & Gain -- VOGAD -- Pre-/De-Emphasis -- Deviation Limiter
- **Serial Microprocessor Interface**
- **Separate SAT Channel**
- **Sidetone Output Available**
- **HandsFree Compatibility**
- **Access to External Processes**
  Compression -- Expansion -- Signaling/Data Mixing -- VSR Codec (Store/Play)
- **Powersave (Low Current) Settings**



MX816J
28-pin CDIP



MX816DW
28-pin SOIC

4

Description

The MX816 is a microprocessor controlled full-duplex audio processor on a single chip with separate TX and RX paths to provide all the filter/gain/limiting functions necessary to pre-process audio, data and signaling in the Nordic Mobile Telephone (NMT) cellular communications system.

Selectable inputs to the transmit path include a choice of two microphones, DTMF/signaling or MSK/data with access in this path to external compression circuitry. The TX path provides input/gain filtering, VOGAD, a deviation limiter and TX Modulation Drive controls.

In the RX path the SAT signal is separated from the incoming audio via a gain/filter block and made available at a separate pin for mixing externally with the TX Modulation Drive.

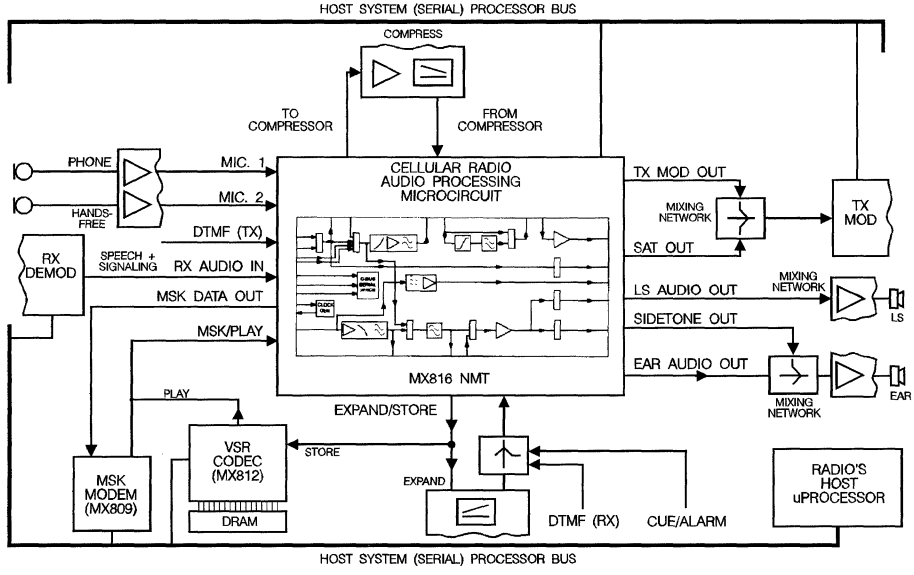


Figure 1 - MX816 NMT Audio Processor Installed in a Cellular System

Description...

The RX path consists of an input gain/filter block for voice and data, inputs from an external audio expansion system and an output gain (volume) control driving either a loudspeaker (handsfree) system or earpiece.

Unique to the MX816/826/836 cellular audio processors is the ability to route audio (TX or RX) to an external Voice Storage and Retrieval device such as the MX802 or MX812, thus providing the radio system with a voice answering and announcement capability using external DRAM.

The MX816, a low-power 5V CMOS integrated circuit, reduces the amount of components required in a cellular audio system by providing more functions on a single chip. It is available in 28-pin Cerdip and small outline (SOIC) packages.

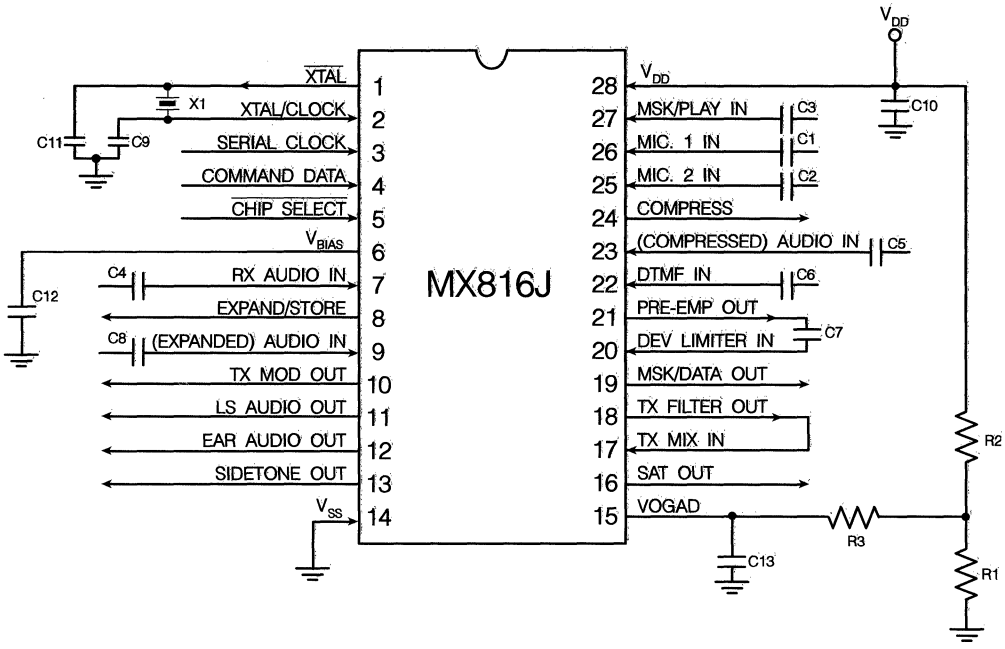
Pin Function Chart

Pin	Function
1	**$\overline{\text{Xtal}}$:** The output of the 4.032 MHz on-chip clock oscillator. External components are required at this output when a Xtal is used. See Figure 2.
2	**Xtal/Clock:** The input to the on-chip clock oscillator. A Xtal or externally derived clock should be connected here. Note that operation of the MX816 without a suitable Xtal or clock input may cause device damage. See Figure 2 (notes).
3	**Serial Clock:** The "C-BUS" serial data clock input. This clock, produced by the microcontroller, is used for transfer timing of commands and data to the MX816. See Timing diagrams.
4	**Command Data:** The "C-BUS" serial data input from the microcontroller. Data is loaded to this device in 8-bit bytes, MSB (B7) first and LSB (B0) last, synchronized to the Serial Clock. See Timing diagrams.
5	**$\overline{\text{Chip Select (CS)}}$:** The "C-BUS" data loading control function. This input is provided by the microcontroller. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Timing Diagrams.
6	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$. This pin should be decoupled to V_{SS}. See Figure 2.
7	**RX Audio In:** The audio input to the MX816. Normally taken from the radio's discriminator output, this input has a 1MΩ internal resistor to V_{BIAS}, and must be connected with a capacitor.
8	**Expand/Store:** This is a common output that can be used as either an input to an external audio expander or the input to a voice storage medium such as the MX812. Components relevant to the external device requirements should be used at this output. See Figures 2 and 3.
9	**Expanded Audio In:** This is the audio input, via SW5, from an external expander or audio mixing function. This input has a 1MΩ internal resistor to V_{BIAS}, and must be connected via a capacitor. See Figures 2 and 3.
10	**TX Mod Out:** This is the composite TX audio output to the transmitter modulator from a variable attenuation stage (11_H). This output is set to V_{BIAS} via an internal 1MΩ resistor when set to Powersave or OFF.
11	**LS Audio Out:** This is an audio output of the RX path (or selected audios - see Figures 3 and 4) for a loudspeaker system. This is available for handsfree operation. This output can be connected to V_{BIAS} when not required, by SW6 (Configuration Command 10_H). A driver amplifier may be required.
12	**Ear Audio Out:** This is an audio output of the RX path (or selected audios - see Figures 3 and 4), available as an output for a handset earpiece. This output in parallel with the LS Audio Out function can be connected to V_{BIAS} when not required by SW7 (Configuration Command 10_H). A driver amplifier may be required.
13	**Sidetone:** This is a switched "sidetone" from the microphone inputs made available for mixing externally with the Ear audio. See Figure 3.
14	**V_{SS}:** Negative supply (GND).

Pin Function Chart

Pin	Function
15	**VOGAD:** External components (R and C) at this pin control the attack and decay time constants of the on-chip VOGAD function.
16	**SAT Out:** This is the output of the SAT bandpass filter. This level is recovered from the Input RX Audio. This tone level can be modified by the SAT and Powersave Command (13_H) and is available for mixing internally with the transmitter modulation. See Figures 3 and 4.
17	**TX Mix In:** An input and an output available, with external components, to introduce signaling tones into the TX Path prior to the final level adjustments.
18	**TX Filter Out:**
19	**MSK Out:** This is the de-emphasized RX audio output available for access to the received MSK data. It could be directed to an MSK Modem such as the MX439.
20	**Deviation Limiter In:** This is the input to the on-chip deviation limiter. This input should be a.c. coupled to the Pre-Emphasis Out pin. The a.c. coupling will achieve macimum possible symmetry of limiting as this input has a 1MΩ reisistor to V_{BIAS}. See Figure 2.
21	**Pre-Emphasis Out:** Audio output from the VOGAD circuitry in the TX Input Gain/Pre-Emphasis function. This output should be a.c. coupled to the Deviation Limiter In pin. See Figure 2.
22	**DTMF In:** This input, which introduces DTMF type audio to the TX path at a suitable level for transmission, is controlled by SW2 (Configuration Command 10_H). This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
23	**Compression In:** This is the audio input from an external compression system. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
24	**Compression:** This is the output to an external audio compression system. Currently available compressor/expanders have op-amps incorporated. The compressor can be bypassed by SW2.
25	**Mic 2 In:** These TX voice (Mic.) inputs, selectable by SW1, are available for handsfree mic./ handset mic. or and TX audio input. Pre-amplification may be required at these inputs.
26	**Mic 1 In:** These inputs each have an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
27	**MSK/Play In:** This is the TX MSK data input via SW2. This can also be used to input (replay) from a voice storage device such as the MX812. This "replayed" audio can be sent to RX or TX paths, allowing a Messaging/Voice Notepad/Answering function. Both the MX439 MSK Modem and the MX812 VSR Codec outputs can be wired directly to this pin if the functions are activated one at a time. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
28	**V_{DD}:** Positive supply. A single, stable +5 volt supply is required. Levels and voltages within this Audio Processor are dependent upon this supply. *C-BUS is MX-COM's proprietary standard for the transmission of commands and data between a µController and DBS 800 IC's. It may be used with any µController, and can, if desired, take advantage of hardware serial I/O functions embodied into many types of µController. The C-BUS data rate is determined solely by the µController.* ***Notes on Inputs:** To minimize aliasing effects, lowpass filtering may be required at the inputs to this device (especially thise supplied from switched-capacitor-type devices) to ensure the input spectrum is kept below 63 kHz.*

4



Component	Value	Component	Value
R_1	100kΩ	C_7	0.1µF
R_2	100kΩ	C_8	0.1µF
R_3	2.2MΩ	C_9	33pF
C_1	0.1µF	C_{10}	0.1µF
C_2	0.1µF	C_{11}	33pF
C_3	0.1µF	C_{12}	1.0µF
C_4	0.1µF	C_{13}	0.1µF
C_5	0.1µF	X_1	4.032MHz
C_6	0.1µF		

Tolerance: R=±10%. C=±20%.

Figure 2 - Recommended External Components

Notes:

1. **Xtal/clock Operation**

Operation of any MX-COM IC without a Xtal or clock input may cause device damage. To minimize damage in the event of a Xtal/drive failure, you should install a current limiting device (resistor or fast-reaction fuse) on the power input (V_{DD}).

2. **VOGAD Components**

R_1, R_2, R_3, C_{13} and the VOGAD Pin internal impedance form the VOGAD timing circuitry.

Control-Voltage Attack Time is set by
C_{13} x Internal Impedance
Control-Voltage Decay Time is set by
C_{13} x R_3 (assuming R_3>>R_1 and R_2).

3. **MSK Modem**

The MX439, a general purpose MSK Modem, could be used within this NMT system Audio Processor. The MX439 is a non-formatted modem, which with due regard to Xtal/clock frequencies and Microprocessor interface, is compatible with both Mobile/Portable and Base Station applications.

4. **SAT Output**

Due to the high output impedance of this output, an external buffer amplifier may be required at this output when interfacing or mixing with other system sections.

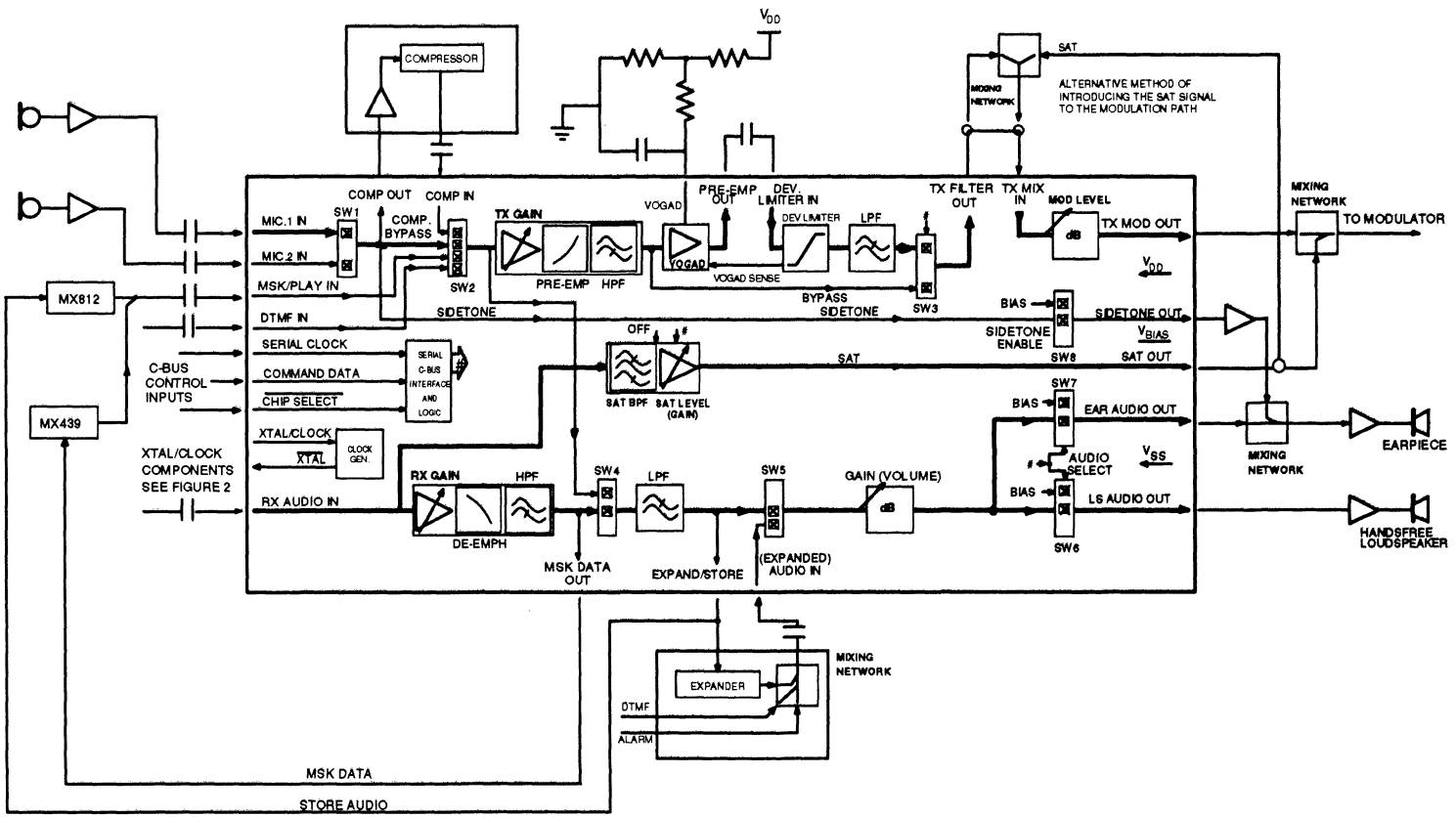


Figure 3 - The MX816 Within an NMT Cellular Radio System

The Controlling System

C-BUS is designed for low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software. It may be used with any µController, and can, if desired, take advantage of the hardware and serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data rate is determined solely by the µController, the system designer has complete freedom to choose a µController appropriate to the overall system processing requirements.

Control of the functions and levels within the MX816 NMT Audio Processor is by a group of Address/Commands and appended data instructions from the system microcontroller. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Hex.	Address/Command Binary MSB LSB		Command Data	Table
General Reset	01	0 0 0 0 0 0 0 1			
Configuration Command	10	0 0 0 1 0 0 0 0	+	1 byte	2
TX Gain & Mod. Command	11	0 0 0 1 0 0 0 1	+	1 byte	3
RX Gain & Vol. Command	12	0 0 0 1 0 0 1 0	+	1 byte	4
Volume Set	13	0 0 0 1 0 0 1 1	+	1 byte	5

Table 1 - C-BUS Address/Commands

In C-BUS protocol the MX816 is allocated Address/Command values 10_H to 13_H. Configuration, TX/RX Gains, and SAT/Powersave assignments and data requirements are given in Table 1.

Each instruction consists of an Address/Command (A/C) byte followed by a data instruction formulated from the following tables.

Commands and Data are only to be loaded in the group configurations detailed, as the C-BUS interface recognized the first byte after $\overline{\text{Chip Select}}$ (logic 0) as an Address/Command. Function or Level control data, which is detailed in Tables 2, 3, 4, and 5, is acted upon at the end of the loaded instruction. See Timing Diagrams, Figures 5 and 6.

Upon power-up the value of the "bits" in this device will be random (either "0" or "1"). A General Reset Command (01_H) is required to set all MX816 registers to 00_H.

Configuration Command *(Preceded by A/C 10_H)*

Setting	Control Bits
(MSB) Bit 7	***Transmitted First*** **SW8 Sidetone**
0	Sidetone Bias
1	Sidetone Enabled
6	**SW6/7 RX Audio**
0	Ear Enabled, LS Bias
1	LS Enabled, Ear Bias
5	**SW5 Expander**
0	Expander Bypass
1	Expander Route
4	**SW4 TX/RX Audio**
0	TX Store/Audio
1	RX Store/Audio
3	**SW3 Dev. Limiter**
0	Dev. Limiter Bypass
1	Dev. Limiter Route
2	**SW1 Mic. Inputs**
0	Mic. 1 Input
1	Mic. 2 Input
1 0	**SW2 TX Function**
0 0	DTMF In
0 1	Compressor In
1 0	Compressor Bypass
1 1	MSK/Play In

Table 2 - Configuration Commands

TX Gain & Mod. Command *(Preceded by A/C 11_H)*

Setting	Gain (dB)
(MSB) 7 6 5 4	***Transmitted First*** **TX Mod. Level**
0 0 0 0	OFF (Low Z to V_{BIAS})
0 0 0 1	-5.6dB
0 0 1 0	-5.2dB
0 0 1 1	-4.8dB
0 1 0 0	-4.4dB
0 1 0 1	-4.0dB
0 1 1 0	-3.6dB
0 1 1 1	-3.2dB
1 0 0 0	-2.8dB
1 0 0 1	-2.4dB
1 0 1 0	-2.0dB
1 0 1 1	-1.6dB
1 1 0 0	-1.2dB
1 1 0 1	-0.8dB
1 1 1 0	-0.4dB
1 1 1 1	0dB
3 2 1 0	**TX Input Gain**
0 0 0 0	-2.65dB
0 0 0 1	-2.05dB
0 0 1 0	-1.50dB
0 0 1 1	-0.95dB
0 1 0 0	-0.45dB
0 1 0 1	0dB
0 1 1 0	0.45dB
0 1 1 1	0.85dB
1 0 0 0	1.25dB
1 0 0 1	1.65dB
1 0 1 0	2.05dB
1 0 1 1	2.40dB
1 1 0 0	2.70dB
1 1 0 1	3.05dB
1 1 1 0	3.35dB
1 1 1 1	3.65dB

Table 3 - TX Gain & Mod. Commands

The Controlling System

Configuration Command *(Preceded by A/C 10_H)*

Setting				Control Bits
(MSB)				*Transmitted First*
7	***6***	***5***	***4***	**RX LS Volume**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-28.0dB
0	0	1	0	-26.0dB
0	0	1	1	-24.0dB
0	1	0	0	-22.0dB
0	1	0	1	-20.0dB
0	1	1	0	-18.0dB
0	1	1	1	-16.0dB
1	0	0	0	-14.0dB
1	0	0	1	-12.0dB
1	0	1	0	-10.0dB
1	0	1	1	-8.0dB
1	1	0	0	-6.0dB
1	1	0	1	-4.0dB
1	1	1	0	-2.0dB
1	1	1	1	0dB
3	***2***	***1***	***0***	**RX Input Gain**
0	0	0	0	3.75dB
0	0	0	1	4.30dB
0	0	1	0	4.80dB
0	0	1	1	5.30dB
0	1	0	0	5.80dB
0	1	0	1	6.20dB
0	1	1	0	6.55dB
0	1	1	1	7.05dB
1	0	0	0	7.40dB
1	0	0	1	7.80dB
1	0	1	0	8.15dB
1	0	1	1	8.50dB
1	1	0	0	8.80dB
1	1	0	1	9.10dB
1	1	1	0	9.40dB
1	1	1	1	9.70dB

Table 4 - RX Gain and Volume Commands

TX Gain & Mod. Command *(Preceded by A/C 11_H)*

Setting				Gain (dB)
(MSB)				*Transmitted First*
Bit 7				
0				Must be a logic "0"
6				
0				Must be a logic "0"
5	***4***	***3***	***2***	**SAT Tone Level**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-1.95dB
0	0	1	0	-1.40dB
0	0	1	1	-0.90dB
0	1	0	0	-0.45dB
0	1	0	1	0dB
0	1	1	0	0.40dB
0	1	1	1	0.85dB
1	0	0	0	1.20dB
1	0	0	1	1.60dB
1	0	1	0	1.95dB
1	0	1	1	2.30dB
1	1	0	0	2.60dB
1	1	0	1	2.90dB
1	1	1	0	3.25dB
1	1	1	1	3.50dB
		1		**Powersave RX Gain Element**
		0		Powersave Element
		1		Enable Element
		0		**Powersave MX816**
				(except RX Gain Element)
		0		Powersave MX816
		1		Enable MX816

Table 5 - SAT and Powersave Commands

Reference Signal Levels

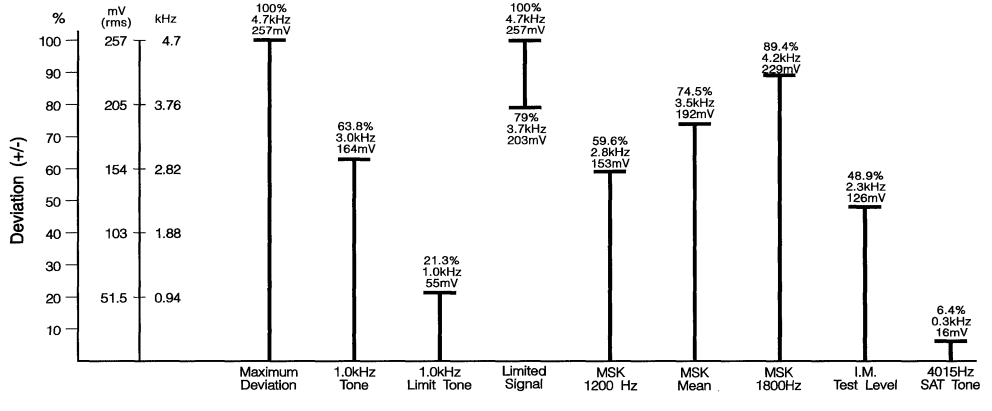


Figure 4 - NMT Signal Deviation Levels and Corresponding TX Mod Outputs with the Mod Level set to 0dB

Timing Information

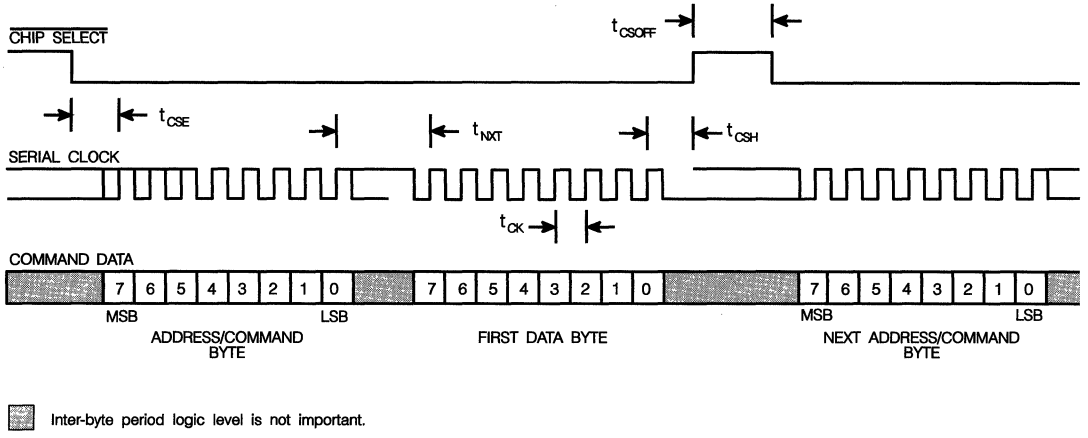


Figure 5 - Control Timing Information

Parameter		See Note	Min.	Typ.	Max.	Unit
"$\overline{CS}$ Enable" to "clock high"	t_{CSE}	1	2.0	-	-	µs
Last "clock high" to "CS high"	t_{CSH}	1	4.0	-	-	µs
"$\overline{CS}$ high" time between transactions	t_{CSOFF}	1,2	2.0	-	-	µs
Clock Cycle Time	t_{CK}	1	2.0	-	-	µs
Inter byte time	t_{NXT}	1	4.0	-	-	µs
Serial Clock-High Period	t_{CH}		500	-	-	ns
Serial Clock-Low Period	t_{CL}		500	-	-	ns
Command Data Set-up Time	t_{CDS}		250	-	-	ns
Command Data Hold Time	t_{CDH}		0	-	-	ns

Notes

1. These minimum timing values are altered during operation of the MX812 VSR Codec.
2. Chip Select must be taken to a logic "1" between each individual transaction.

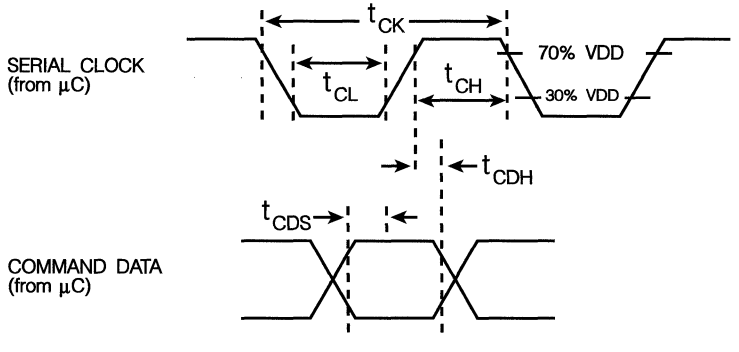


Figure 6 - Control Timing Relationships

System Performance

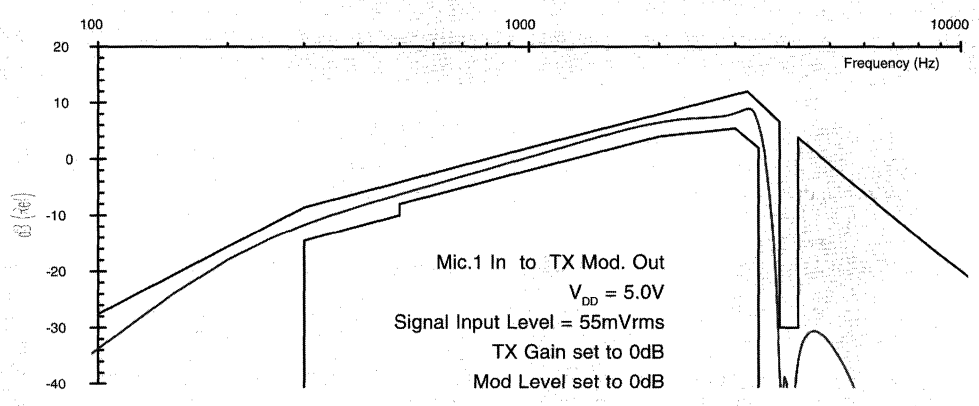


Figure 7 - TX Frequency Response

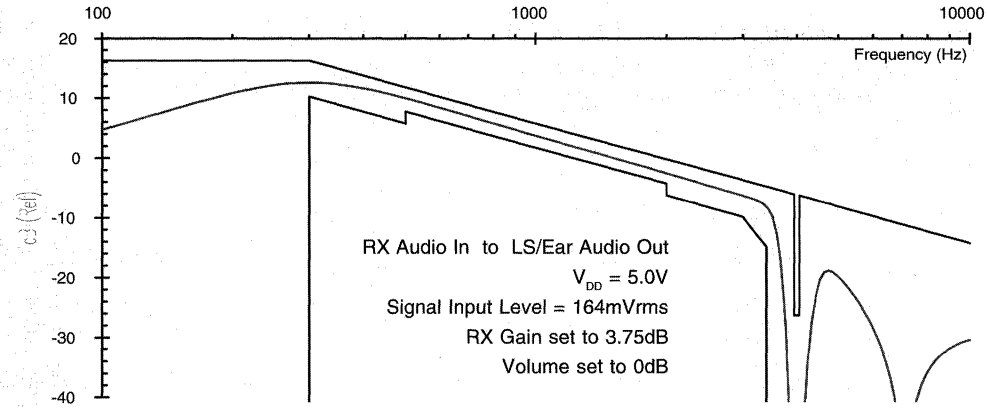


Figure 8 - RX Frequency Response

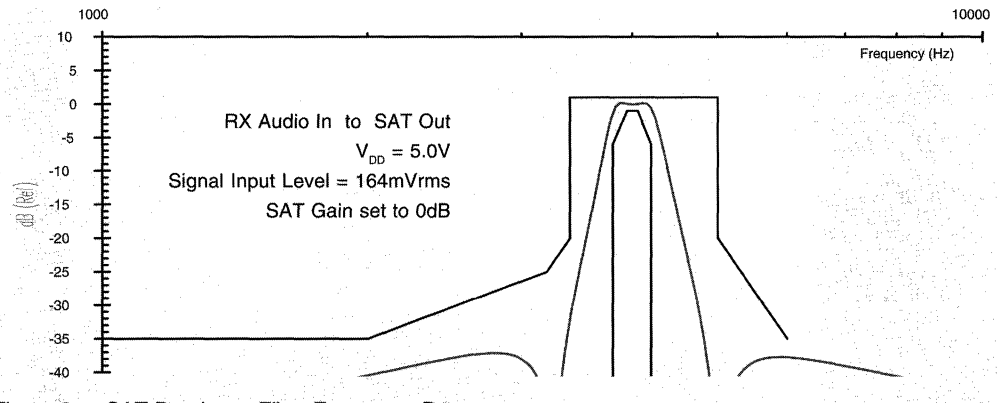


Figure 9 - SAT Bandpass Filter Frequency Response

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD}+0.3V)
Sink/source current (supply pins)	±30mA
(other pins)	±20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/Clock f_0 = 4.032MHz

Audio Level 0dB ref = 164mVrms @ 1kHz

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current (All elements enabled)		-	6.0	-	mA
(RX Data Mode)		-	1.0	-	mA
(Maximum Powersave)		-	0.6	-	mA
Alias Frequency		-	63.0	-	kHz
On-Chip Xtal Oscillator					
R_{IN}		10.0	-	-	MΩ
R_{OUT}		-	10.0	-	kΩ
Inverter DC Voltage Gain		-	10.0	-	V/V
Gain/Bandwidth Product		-	10.0	-	MHz
Analog Input Impedances					
Mic. 1 & 2		-	500	-	kΩ
MSK/Play		-	500	-	kΩ
Comp. In		-	500	-	kΩ
DTMF In		-	500	-	kΩ
Deviation Limiter In		-	100	-	kΩ
Expanded Audio In		-	47.0	-	kΩ
TX Mix In		-	100	-	kΩ
RX Audio In		-	100	-	kΩ
Analog Output Impedances					
Pre-Emphasis Out		-	600	-	Ω
TX Mod Out		-	600	-	Ω
Expand/Store		-	600	-	Ω
LS and Ear Audio		-	1.0	-	kΩ
MSK Data Out		-	600	-	Ω
SAT Out		-	10.0	-	kΩ
TX Filter Out		-	600	-	Ω
VOGAD		-	500	-	Ω
Switches - ON		-	1.0	-	kΩ
- OFF		10.0	-	-	MΩ
Control Interface Parameters					
Input Logic "1"	2	3.5	-	-	V
Input Logic "0"	2	-	-	1.5	V
Input Current	2	-1.0	-	1.0	µA
Input Capacitance	2	-	-	7.5	pF

4

Characteristics	See Note	Min.	Typ.	Max.	Unit
Channel Performance, TX Signal Path					
Analog Signal Input Levels					
Mic. 1 & 2	3	-	0	-	dB
MSK/Play	3	-	0	-	dB
DTMF	3	-	0	-	dB
Comp. In	3	-	0	-	dB
TX Mix In	3	-	0	-	dB
Analog Signal Output Levels					
Pre-Emphasis Out	3	-	0	-	dB
TX Filter Out	3	-	0	-	dB
TX Mod. Out	3	-	0	-	dB
Sidetone Out	3	-	0	-	dB
Path Gains/Levels					
TX Gain - 11_H					
Adjustment Range		-2.65	-	3.65	dB
Step Error		-0.2	-	0.2	dB
VOGAD					
Gain (Non-Compressing)		-	0	-	dB
(Full Compression)		-	-15.0	-	dB
Attack Time	4	-	3.0	-	ms
Deviation Limiter					
Threshold		-	713	-	mV p-p
Symmetry		-	7	-	%
Mod. Level Attenuation - 11_H					
Adjustment Range		-5.6	-	0	dB
Step Size		0.2	0.4	0.6	dB
Error of any Setting		-1.0	-	1.0	dB
Overall					
TX Distortion		-	-40.0	-32.0	dB
TX Hum and Noise		-	-40.0	-20.0	dB
Channel Performance, RX Signal Path					
RX Audio Input Level	3	-	-7.0	-	dB
LS/Ear Audio Output Level	3	-	0	-	dB
Path Gains/Levels					
RX Gain - 12_H					
Adjustment Range		3.75	-	9.70	dB
Error of any Setting		-0.2	-	0.2	dB
MSK Output					
Frequency Range		900	-	2100	dB
Gain at 1kHz		-1.0	0	1.0	dB
Response		-	6.0	-	dB/oct.
Volume - 12_H					
Adjustment Range		-28.0	-	0	dB
Step Size		1.5	2.0	2.5	dB
Error of any Setting		-1.0	-	1.0	dB
Overall					
RX Distortion		-	-40.0	-32.0	dBp
RX Hum and Noise		-	-40.0	-34.0	dB

4

Characteristics	See Note	Min.	Typ.	Max.	Unit
Channel Performance, SAT Signal Path					
Bandpass Filter					
Frequency Range		3945	-	4055	Hz
Gain		-1.0	-	1.0	dB
SAT Level - 13_H					
Adjustment Range		-1.95	-	3.50	dB
Step Error		-0.2	-	0.2	dB

Notes

1. With reference to the Powersave Command and Figure 3, all functions with the exception of the RX Gain Element may be powersaved. This will still allow signaling data through the MX816 to activate the system via the µProcessor.

2. Serial Clock, Command Data and Chip Select Inputs.

3. Levels equivalent to ±3.0 kHz deviation with the settings below:

TX Gain = 0dB	Mod Level = 0dB
RX Gain = 7.05dB	Volume = 0dB
SAT Level = 0dB	

Other levels can be achieved by adjusting the above variable gain blocks in accordance with Tables 1 - 5.

4. Using the components shown in Figure 2.

MX-COM, INC.

Preliminary Information

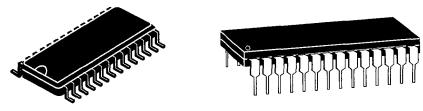
MX826

C-BUS COMPATIBLE

AMPS/NAMPS SYSTEM AUDIO PROCESSOR

Features

- **Full-Duplex Audio Processing for AMPS/ NAMPS Cellular Systems**
- **On-Chip Speech and SAT Capabilities**
  – TX/RX Filtering & Gain – SAT Channel Pre-/De-Emphasis – Deviation Limiter
- **Serial µProcessor Interface**
- **"Sidetone" Output Available**
- **Access to External Processes**
  – Compression – Expansion – Signaling – VSR Codec (Store/Play)
- **HandsFree Compatibility**
- **Powersave (Low-Current) Settings**



MX826DW
28-pin SOIC

MX826J
28-pin CDIP

4

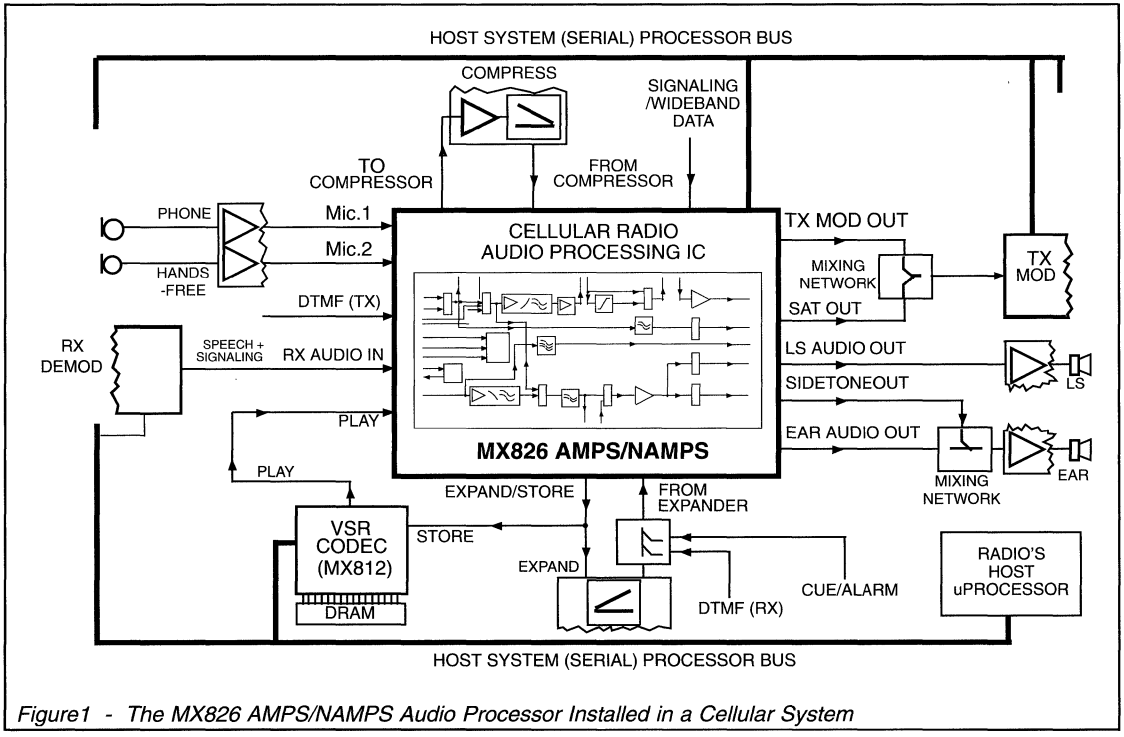


Figure1 - The MX826 AMPS/NAMPS Audio Processor Installed in a Cellular System

Description

The MX826 is a µProcessor controlled full-duplex audio processor on a single-chip with separate TX and RX paths to provide all the filter/gain/limiting functions necessary to pre-process audio, wideband-data and signalling in cellular communications systems using the AMPS/NAMPS or TACS/ETACS/JTACS specifications.

Selectable inputs available to the transmit path are: a choice of two microphones and DTMF/signaling, with access, in this path, to external compression circuitry. Operationally the TX path provides input gain/filtering, a deviation limiter and TX Modulation Drive controls.

In the RX path the SAT signal is separated from the incoming audio via a filter block and made available at a separate pin for mixing externally with the TX Modulation Drive.

The RX path consists of an input gain/filter block for voice, inputs from an external audio expansion system and an output gain control driving either a loudspeaker system or earpiece.

Unique to the MX816/826/836 cellular audio processors is the ability to route audio (TX or RX) to an external Voice Store and Retrieve (VSR) device such as the MX802 or MX812 thus providing the radio system with a voice answering and announcement facility using external DRAM.

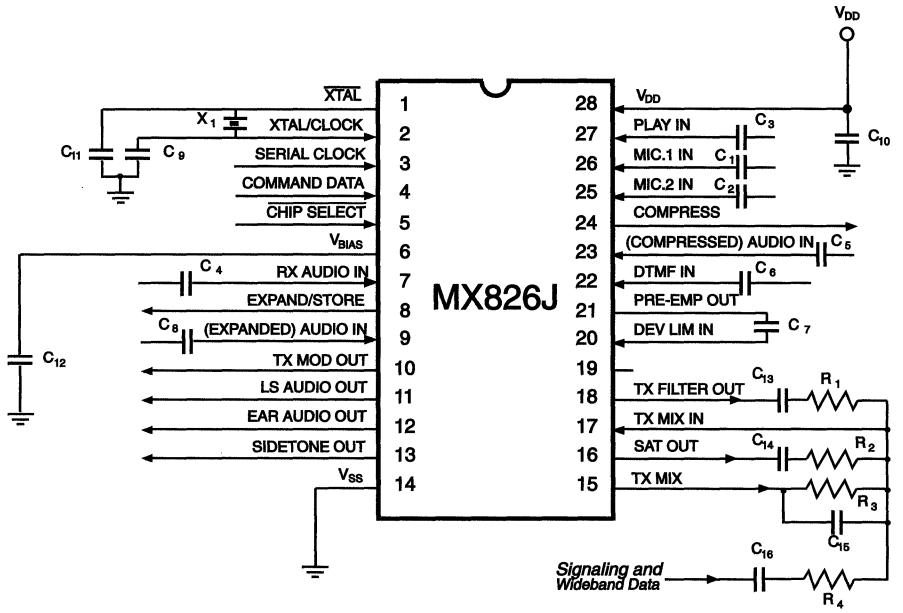
As a member of the DBS800 family, the MX826 follows C-BUS protocol. (C-BUS is the serial interface used by all DBS800 integrated circuits.)

The MX826, a low-power CMOS device which reduces the amount of microcircuits and components required in a cellular audio system by providing more functions on a single chip, is available in 28-pin SOIC and CDIP packages.

Pin	Function
1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator.
2	**Xtal/Clock:** The input to the on-chip clock oscillator. A Xtal or externally derived clock (f_{XTAL}) should be connected here. Note that operation of the MX826 without a suitable Xtal or clock input may cause device damage. See Figure 2 (notes).
3	**Serial Clock:** The "C-BUS" serial data clock input. This clock, produced by the µController, is used for transfer timing of commands and data to the MX826. See Timing Diagrams.
4	**Command Data:** The "C-BUS" serial data input from the µController. Data is loaded to the MX826 in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams.
5	**Chip Select ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the µController. Data transfer sequences are initiated, completed or aborted by this signal. See Timing Diagrams.
6	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS}. See Figure 2.
7	**Rx Audio In:** Normally taken from the radio's discriminator output, this input has a 1MΩ internal resistor to V_{BIAS} and requires to be connected via a capacitor.
8	**Expand/Store:** A common output that can be used as either an input to an external audio expander or the input to a voice storage medium such as the MX812. Components relevant to the external device requirements should be used at this output. See Figures 2 and 3.
9	**(Expanded) Audio In:** The audio input, via SW5, from an external expander or audio mixing function. This input has a 1MΩ internal resistor to V_{BIAS} and requires to be connected via a capacitor. See Figures 2 and 3.
10	**TX Mod Out:** The composite TX audio output to the transmitter modulator from a variable attenuation stage (11_H). This output is set to V_{BIAS} via an internal 1MΩ resistor when set to Powersave or OFF.
11	**LS Audio Out:** An audio output of the Rx path (or selected audios, see Figure 3) for a loudspeaker system. This is available for handsfree operation. This output can be connected to V_{BIAS} when not required, by SW6 (Configuration Command (10_H)). A driver amplifier may be required.
	Notes on Inputs: *To minimize aliasing effects, lowpass filtering may be required at the inputs to this device (especially those supplied from switched-capacitor-type devices) to ensure the input spectrum is kept below 63kHz.*

Pin	Function
12	**Ear Audio Out:** An audio output of the Rx path (or selected audios), available as an output for a handset earpiece. This output, in parallel with the LS Audio Out function, can be connected to V_{BIAS} when not required, by SW7 (Configuration Command (10_H)). A driver amplifier may be required.
13	**Sidetone:** A switched "sidetone" from the microphone inputs made available for mixing externally with the "Ear" audio. See Figure 3.
14	**V_{SS}:** Negative supply rail. Signal ground.
15	**TX Mix:** The output of the TX Mix Amplifier. Used with external components, it allows the TX Filter Out output to mix with externally generated signalling tones prior to the final level adjustment.
16	**SAT Out:** The output of the SAT Bandpass filter. This level is recovered from the input RX audio and is available for mixing externally with the transmitter modulation. See Figure 3.
17	**TX Mix In:** The input to the TX Mix Amplifier. Used with external components, it allows the TX Filter Out output to mix with externally generated signalling tones prior to the final level adjustment. The recovered SAT signal may be introduced at this point. See Figures 2 and 3.
18	**TX Filter Out:** The output of the Deviation Limiter/Lowpass Filter stage. This stage can be by-passed using SW3 (Configuration Command). See Figure 3.
19	No internal connection – Leave open circuit.
20	**Dev**iation **Limiter In:** Input to the on-chip deviation limiter. This input should be a.c. coupled to the Pre-Emphasis Out pin. The a.c. coupling will achieve maximum possible symmetry of limiting as this input has a 1MΩ internal resistor to V_{BIAS}. See Figure 2.
21	**Pre-Emphasis Out:** Audio output from the TX Gain/Pre-Emphasis function. This output should be a.c. coupled to the Deviation Limiter In pin. See Figures 2 & 3.
22	**DTMF In:** To introduce DTMF type audio, at a suitable level for transmission, to the TX Path, controlled by SW2 (Configuration Command (10_H)). This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
23	**Comp**ression **In:** The audio input from an external compression system. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
24	**Comp**ression**:** The output to an external audio compression system. Currently available compressor/ expanders have Op-Amps incorporated. The compressor can be by-passed by SW2.
25	**Mic.2 In:** TX voice (Mic.) inputs, selectable by SW1 available for handsfree mic./handset mic. or any TX audio input. Pre-amplification may be required at these inputs. These inputs
26	**Mic.1 In:** each have an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
27	**Play In:** The input via SW2 from a voice storage device such as the MX812. This "replayed" audio can be sent to RX or TX paths allowing a Messaging/Voice Notepad/Answering facility. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
28	**V_{DD}:** Positive supply rail. A single +5-volt power supply is required. Levels and voltages within this Audio Processor are dependent upon this supply.
	***C-BUS** is MX-COM's proprietary standard for the transmission of commands and data between a µController and the relevant Cellular microcircuits. It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions embodied into many types of µController. The "C-BUS" data rate is determined solely by the µController.*

Application Information



R_1	= 100kΩ	C_3	= 100nF	C_8	= 100nF	C_{13}	= 100nF
R_2	as required	C_4	100nF	C_9	33pF	C_{14}	100nF
R_3	100kΩ	C_5	100nF	C_{10}	100nF	C_{15}	100pF
R_4	as required	C_6	100nF	C_{11}	33pF	C_{16}	100nF
C_1	100nF	C_7	100nF	C_{12}	1.0µF	X_1	4.000MHz
C_2	100nF						

Tolerances – Capacitors ±20%

Figure 2 - Recommended External Components

Notes

1. **Xtal/clock operation**
   Operation of any MX-COM IC without a Xtal or clock input may cause device damage. To minimize damage in the event of a Xtal/drive failure, you should install a current limiting device (resistor or fast-reaction fuse) on the power input (V_{DD}).

2. **SAT Output**
   It is possible, due to the impedance of this output, that an external buffer amplifier will be required when interfacing or mixing with other cellular system sections.

3. **TX Mix Gain**
   The value of R_4 should be chosen with R_3/C_{15} in order to provide the required gain.

AMPS/NAMPS Cellular System Interfaces

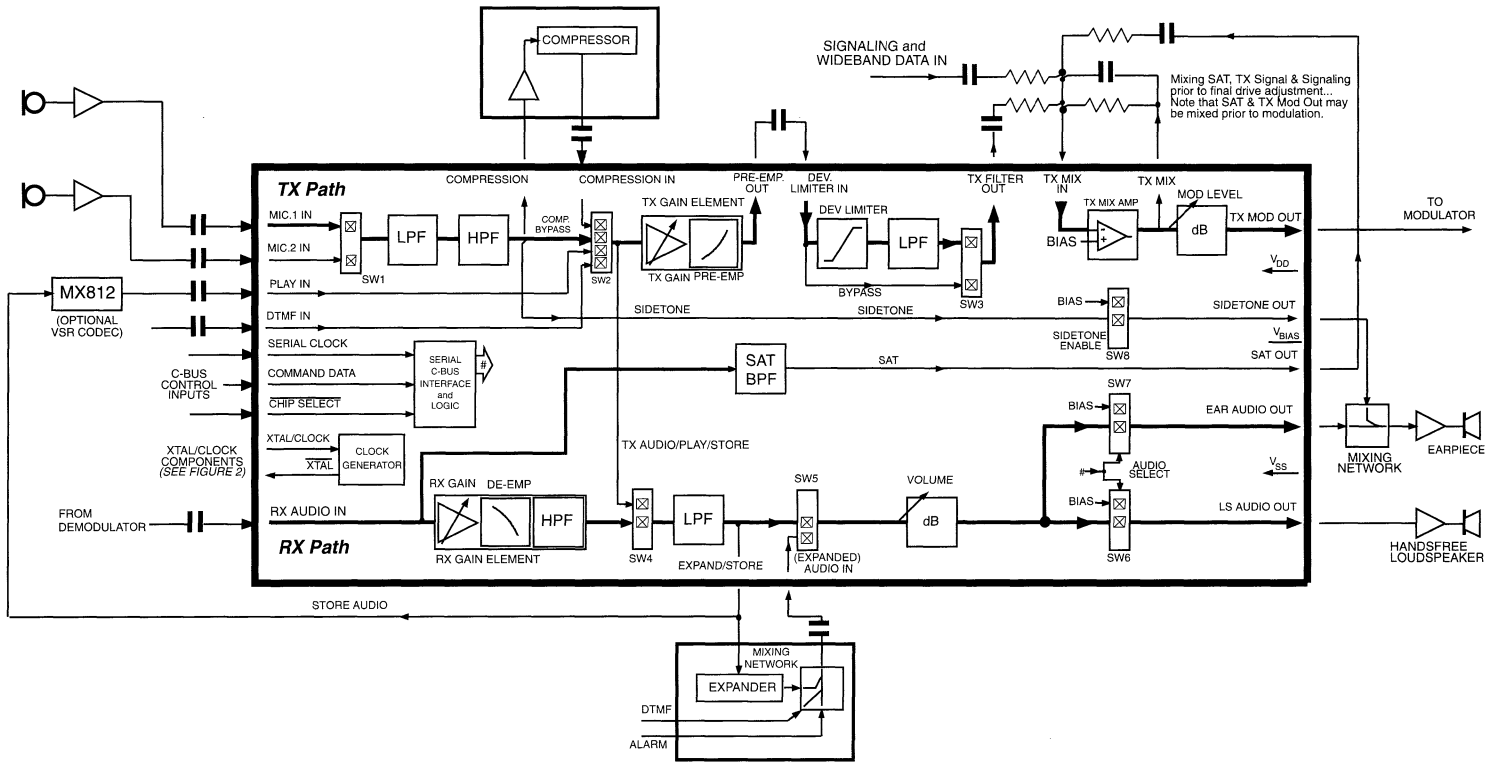


Figure 3 - The MX826 Internal and External Signal Paths within a AMPS/NAMPS Cellular Radio System

The Controlling System: C-BUS Hardware Interface

C-BUS is MX-COM's proprietary standard for the transmission of commands and data between a µController and MX-COM's New Generation integrated circuits. C-BUS has been designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer has complete freedom to choose a µController appropriate to the overall system processing requirements.

Control of the functions and levels within the MX826 is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the device. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex	Binary MSB							LSB		Command Data	Table
General Reset	01	0	0	0	0	0	0	0	1			
Configuration Command	10	0	0	0	1	0	0	0	0	+	1 byte	2
TX Gain & Mod. Command	11	0	0	0	1	0	0	0	1	+	1 byte	3
RX Gain & Vol. Command	12	0	0	0	1	0	0	1	0	+	1 byte	4
Powersave Command	13	0	0	0	1	0	0	1	1	+	1 byte	5

Table 1 "C-Bus" Address/Commands

In C-BUS protocol the audio processor is allocated Address/Command (A/C) values 10_H to 13_H. Configuration, TX/RX Gains, Powersave assignments and data requirements are given in Table 1. Each instruction consists of an Address/Command (A/C) byte followed by a data instruction formulated from the following tables.

Commands and Data are only to be loaded in the group configurations detailed, as the C-BUS interface recognizes the first byte after Chip Select (logic "0") as an Address/Command. Function or Level control data, which is detailed in Tables 2, 3, 4 and 5, is acted upon at the end of the loaded instruction. See Timing Diagrams, Figures 5 and 6.

Upon Power-Up the value of the "bits" in this device will be random (either "0" or "1"). A **General Reset Command (01_H)** will be required to set all MX826 registers to 00_H.

Configuration Command *(Preceded by A/C 10_H)*

Setting		Control Bits
MSB		***Transmitted First***
Bit 7		**Sw8 Sidetone**
0		Sidetone Bias
1		Sidetone Enabled
6		**Sw6/7 RX Audio**
0		Ear Enabled, LS Bias
1		LS Enabled, Ear Bias
5		**Sw5 Expandor**
0		Expander By-Pass
1		Expander Route
4		**Sw4 TX/RX Audio**
0		Tx Store/Audio
1		Rx Store/Audio
3		**Sw3 Dev. Limiter**
0		Dev. Limiter Bypass
1		Dev. Limiter Route
2		**Sw1 Mic. Inputs**
0		Mic. 1 Input
1		Mic.2 Input
1	***0***	**Sw2 TX Function**
0	0	DTMF In
0	1	Compressor Bypass
1	0	Compressor In
1	1	Play In

Table 2 Configuration Commands

TX Gain & Mod. Command *(Preceded by A/C 11_H)*

Setting				Gain (dBs)
MSB				***Transmitted First***
7	***6***	***5***	***4***	**Tx Mod. Level**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-5.6
0	0	1	0	-5.2
0	0	1	1	-4.8
0	1	0	0	-4.4
0	1	0	1	-4.0
0	1	1	0	-3.6
0	1	1	1	-3.2
1	0	0	0	-2.8
1	0	0	1	-2.4
1	0	1	0	-2.0
1	0	1	1	-1.6
1	1	0	0	-1.2
1	1	0	1	-0.8
1	1	1	0	-0.4
1	1	1	1	0
3	***2***	***1***	***0***	**TX Input Gain**
0	0	0	0	-2.65
0	0	0	1	-2.05
0	0	1	0	-1.50
0	0	1	1	-0.95
0	1	0	0	-0.45
0	1	0	1	0
0	1	1	0	0.45
0	1	1	1	0.85
1	0	0	0	1.25
1	0	0	1	1.65
1	0	1	0	2.05
1	0	1	1	2.40
1	1	0	0	2.70
1	1	0	1	3.05
1	1	1	0	3.35
1	1	1	1	3.65

Table 3 TX Gain & Mod. Commands

The Controlling System .....

RX Gain & Vol. Command *(Preceded by A/C 12_H)*

Setting				Gain (dBs)
MSB				Transmitted First
7	6	5	4	RX Volume
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-28.0
0	0	1	0	-26.0
0	0	1	1	-24.0
0	1	0	0	-22.0
0	1	0	1	-20.0
0	1	1	0	-18.0
0	1	1	1	-16.0
1	0	0	0	-14.0
1	0	0	1	-12.0
1	0	1	0	-10.0
1	0	1	1	-8.0
1	1	0	0	-6.0
1	1	0	1	-4.0
1	1	1	0	-2.0
1	1	1	1	0
3	2	1	0	RX Input Gain
0	0	0	0	3.75
0	0	0	1	4.30
0	0	1	0	4.80
0	0	1	1	5.30
0	1	0	0	5.80
0	1	0	1	6.20
0	1	1	0	6.55
0	1	1	1	7.05
1	0	0	0	7.40
1	0	0	1	7.80
1	0	1	0	8.15
1	0	1	1	8.50
1	1	0	0	8.80
1	1	0	1	9.10
1	1	1	0	9.40
1	1	1	1	9.70

Table 4 - RX Gain and Vol. Commands

Powersave Command *(Preceded by A/C 13_H)*

Setting							Control Bits
MSB Bit 7							Transmitted First
7	6	5	4	3	2	1	
0	0	0	0	0	0	0	All must be a logic "0"
			0				Powersave Setting
			0				Powersave MX826
			1				Enable MX826

Table 5 - Powersave Command

Reference Signal Levels

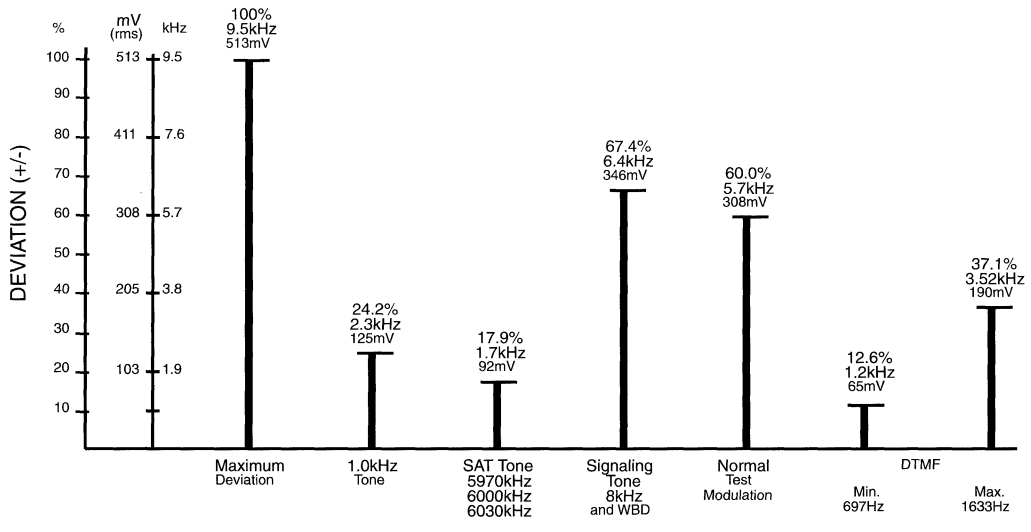


*Figure 4 - Signal Deviation Levels and corresponding **TX Mod Outputs** with the Mod Level set to 0dB*

Control Timing Information

Characteristics		See Note	Min.	Typ.	Max.	Unit
t_{CSE}	"CS-Enable to Clock-High"	1	2.0	–	–	µs
t_{CSH}	Last "Clock-High to CS-High"	1	4.0	–	–	µs
t_{CSOFF}	"CS-High" Time between transactions	1, 2	2.0	–	–	µs
t_{CK}	"Clock-Cycle" Time	1	2.0	–	–	µs
t_{NXT}	"Inter-Byte" Time	1	4.0	–	–	µs
t_{CH}	"Serial Clock-High" Period		500	–	–	ns
t_{CL}	"Serial Clock-Low" Period		500	–	–	ns
t_{CDS}	"Command Data Set-Up" Time		250	–	–	ns
t_{CDH}	"Command Data Hold" Time		0	–	–	ns

Notes

1. These Minimum Timing values are altered during operation of the MX812 VSR Codec.
2. Chip Select must be taken to a logic "1" between each individual transaction.

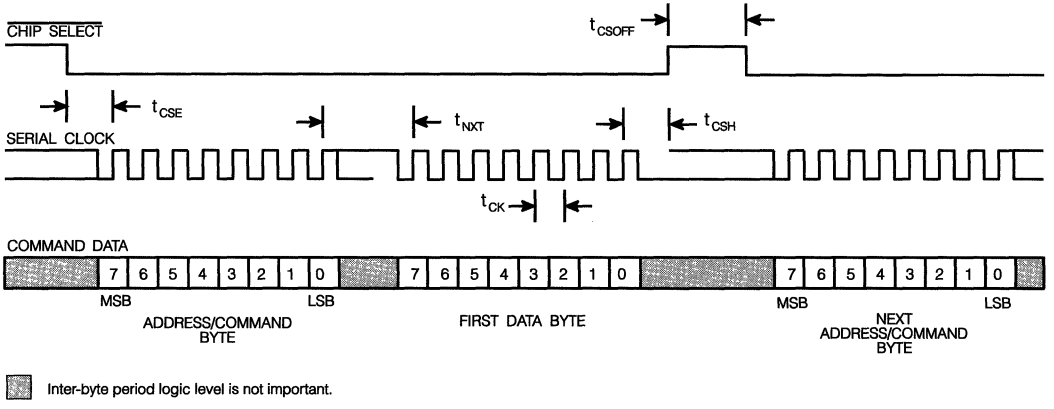


Figure 5 - Control Timing Information

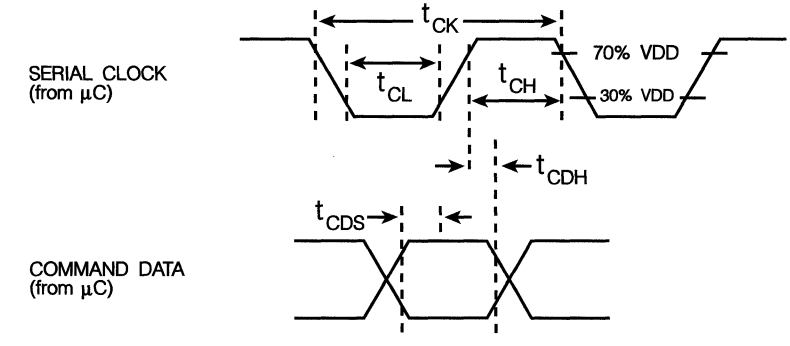


Figure 6 - Control Timing Relationships

Frequency Responses

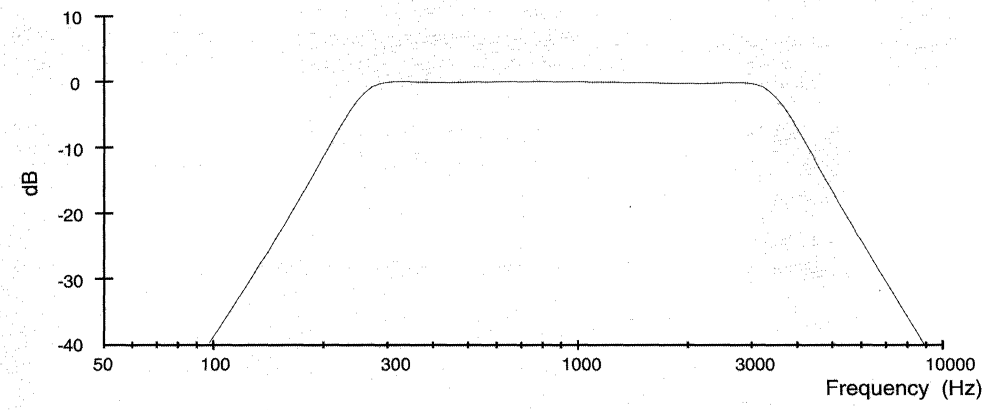


Figure 7 - Microphone Input Stages -Combined Low and Highpass Filter Frequency Response

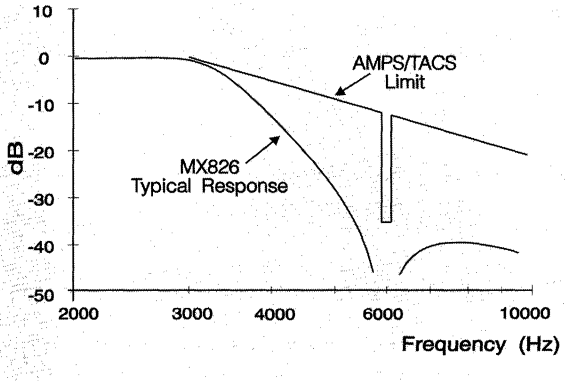


Figure 8 - Post Deviation Limiter Lowpass Filter Response

Figure 7
Mic.1/2 In to Compression Out

V_{DD} = 5.0V

Signal Input Level = 55.0mVrms

Figure 8
Dev Limiter In to TX Filter Out

V_{DD} = 5.0V

Signal Input Level = 55.0mVrms

Figure 9

RX Audio In to SAT out

V_{DD} = 5.0V

Signal Input Level = 100mVrms

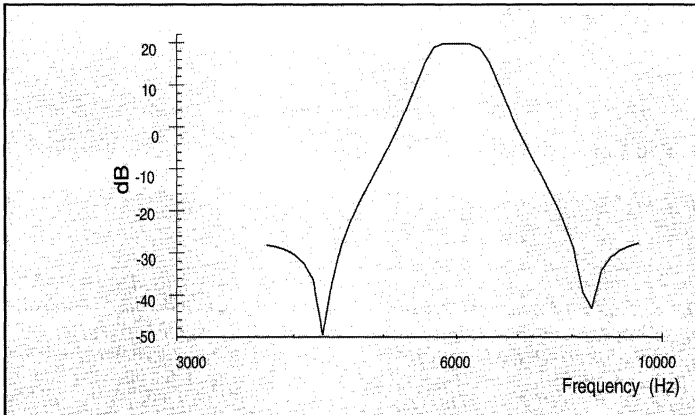


Figure 9 - RX SAT Path Bandpass Filter Response

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (Ref V_{SS} = 0V)	-0.3V to (V_{DD} + 0.3V)
Sink/source Current (Supply pins)	±30mA
(Other pins)	±20mA
Total Device Dissipation @T_{AMB} 25°C	800mW max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/clock f_{XTAL} = 4.0MHz

Audio level 0dB ref. = 308mVrms @ 1kHz

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
Operating		–	6.5	–	mA
Powersave		–	0.5	–	mA
Alias Frequency		–	63.0	–	kHz
On-Chip Xtal Oscillator					
R_{IN}		10.0	–	–	MΩ
R_{OUT}		–	10.0	–	kΩ
Inverter d.c. Voltage Gain		–	10.0	–	V/V
Gain/Bandwidth Product		–	10.0	–	MHz
TX Mix Amp (Open Loop Gain)		–	50.0	–	dB
(Bandwidth)		20.0	–	–	kHz
Analog Input Impedances					
Mic.1 & 2		–	500	–	kΩ
Play		–	500	–	kΩ
Comp In		–	500	–	kΩ
DTMF In		–	500	–	kΩ
Dev. Limiter In		–	100	–	kΩ
(Expanded) Audio In		–	47.0	–	kΩ
TX Mix In		10.0	–	–	MΩ
RX Audio In		–	100	–	kΩ
Analog Output Impedances					
Pre-Emp Out		–	600	–	Ω
TX Mod Out		–	600	–	Ω
Expand/Store		–	600	–	Ω
LS and Ear Audio		–	1.0	–	kΩ
SAT Out	3	–	1.0	–	kΩ
TX Filter Out		–	600	–	Ω
Comp Out		–	600	–	Ω
Sidetone Out		–	2.0	–	kΩ
TX Mix (Open Loop)		–	6.0	–	kΩ
(Closed Loop)		–	600	–	Ω
Switches – ON		–	1.0	–	kΩ
– OFF		10.0	–	–	MΩ

Characteristics	See Note	Min.	Typ.	Max.	Unit
Control Interface Parameters					
Input Logic Levels					
Logic "1"	1	3.5	–	–	V
Logic "0"	1	–	–	1.5	V
I_{IN} (logic "1" or "0")	1	-1.0	–	1.0	µA
Input Capacitance	1	–	–	7.5	pF
Channel Performances					
TX Path					
Filter Specifications					
Pre-Compression L/HPF Combination					
Passband		300		3000	Hz
Slope - below 300Hz		+24.0	–	–	dB/oct.
above 3000Hz		-24.0	–	–	dB/oct.
TX Gain Pre-Emphasis					
Gain at 1.0kHz		–	0	–	dB
Slope (300Hz - 3000Hz)		–	6.0	–	dB/oct.
Post Deviation Limiter LPF					
Attenuation Relative to 1.0kHz					
3.0kHz - 5.9kHz		-	40 log(f/3000)	-	dB
5.9kHz - 6.1kHz		-	35.0	-	dB
6.1kHz - 15kHz		-	40 log(f/3000)	-	dB
>15kHz		-	28.0	-	dB
Analog Signal Input Levels					
Mic. 1 and 2	2	–	0	–	dB
Play	2	–	0	–	dB
DTMF	2	–	0	–	dB
Comp. In	2	–	0	–	dB
TX Mix In	2	–	0	–	dB
Analog Signal Output Levels					
Pre-Emp Out	2	–	0	–	dB
TX Filter Out	2	–	0	–	dB
TX Mod Out	2	–	0	–	dB
Sidetone Out	2	–	0	–	dB
Path Gains/Levels					
TX Gain – 11_H					
Nominal Adjustment Range		-2.65	–	3.65	dB
Error of any Setting		-0.2	–	0.2	dB
Dev Limiter					
Threshold		–	1086	–	mVp-p
Symmetry		–	7.0	–	%
Mod Level Attenuation – 11_H					
Nominal Adjustment Range		-5.6		0	dB
Step Size		0.2	0.4	0.6	dB
Error of any Setting		-1.0	–	1.0	dB
Overall					
TX Distortion		–	-40.0	-32.0	dBp
TX Hum and Noise		–	-40.0	-20.0	dB
RX Signal Path					
Filter Specifications					
RX Gain De-Emphasis					
Gain at 1.0kHz		–	3.75	–	dB
Slope (300Hz - 3000Hz)		–	-6.0	–	dB/oct.
RX Channel Bandpass		300		3000	Hz
Slope - below 300Hz		+24.0	–	–	dB/oct.
above 3000Hz		-36.0	–	–	dB/oct.

4

Characteristics	See Note	Min.	Typ.	Max.	Unit
RX Signal Path (cont'd)					
Analog Signal Levels					
RX Audio Input Level	2	–	-7.0	–	dB
LS/Ear Audio Output Level	2	–	0	–	dB
Path Gains/Levels					
RX Gain – 12_H					
Nominal Adjustment Range		3.75		9.70	dB
Error of any Setting		-0.2	–	0.2	dB
Volume – 12_H					
Nominal Adjustment Range		-28.0		0	dB
Step Size		1.5	2.0	2.5	dB
Error of any Setting		-1.0	–	1.0	dB
Overall					
RX Distortion		–	-40.0	-32.0	dBp
RX Hum and Noise		–	-40.0	-34.0	dB
SAT Signal Path					
Bandpass Filter					
Frequency Range		5970		6030	Hz
Gain		19.0	20.0	21.0	dB

Notes

1. Serial Clock, Command Data and Chip Select inputs.
2. Levels equivalent to ±3.0kHz deviation with the settings below:
   TX Gain = 0dB *Mod Level = 0dB*
   RX Gain = 7.05dB *Volume = 0dB*
   Other levels can be achieved by adjusting the above variable gain blocks in accordance with Tables 1 to 5.
3. Recommended load >10.0kΩ.

MX•COM, INC.

Preliminary Information

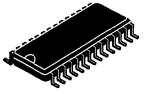
MX836

C-BUS COMPATIBLE

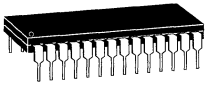
RADIOCOM 2000 SYSTEM AUDIO PROCESSOR

Features

- **Full-Duplex Audio Processing for R2000 Cellular System**
- **On-Chip Speech and Data Facilities**
  - ***TX/RX/Data Filtering & Gain***
  - ***Pre-/De-Emphasis – Deviation Limiter***
- **Serial µProcessor Interface**
- **TX and RX LF-Data Paths**
- **MSK and (50 Baud) LF-Data Facilities**
- **Hands-Free Compatibility**
- **Powersave (Low-Current) Settings**
- **Access to External Processes**
  - ***Compression – Expansion***
  - ***Signaling/Data Mixing***
  - ***VSR Codec (Store/Play)***



MX836DW
28-pin SOIC



MX836J
28-pin CDIP

4

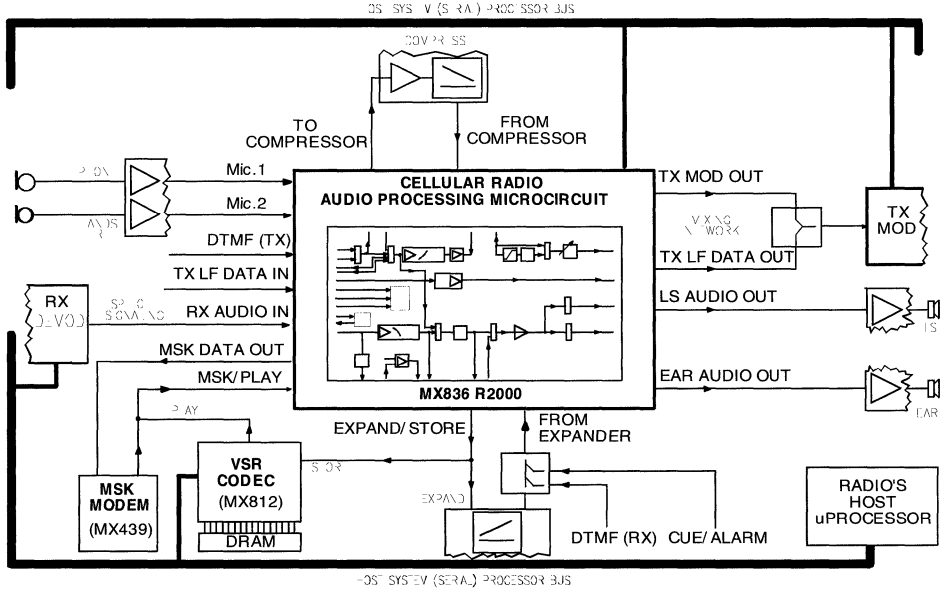


Figure 1 - The MX836 R2000 Audio Processor within a Cellular System

Description

The MX836 is a µProcessor-controlled full-duplex audio processor on a single-chip with separate TX, RX and LF (50 baud) data paths to provide all the filter/gain/limiting functions necessary to pre-process audio, data and signaling in the Radiocom 2000 (R2000) Cellular communications system.

Selectable inputs available for transmission include a choice of two microphones, DTMF/signaling or MSK/data, with access, in this path, to external voice compression circuitry. Operationally the TX path provides input gain/filtering, pre-emphasis, a deviation limiter and TX Modulation Drive controls. Available to the transmit function is a separate path to process LF system control data for amalgamation externally with TX voiceband audio.

The RX path consists of an input gain/de-emphasis/filter block for voice and data, inputs from an external audio expansion system and output gain controls driving loudspeaker and earpiece circuitry.

In the RX path LF data signals are separated from the incoming audio via an LF filter and made available at a separate pin for use by the system µProcessor

Unique to the MX816/826/836 cellular audio processors is the ability to route audio (TX or RX) to an external Voice Store and Retrieve (VSR) device such as the MX802 or MX812, thus providing the radio system with a voice answering and announcement facility using external DRAM.

The MX836, a low-power CMOS device, which reduces the amount of microcircuits and components required in a cellular audio system by providing more functions on a single chip, is available in 28-pin plastic small outline (S.O.I.C.) surface mount and cerdip DIL packages.

Pin	Function
1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator.
2	**Xtal/Clock:** The input to the on-chip clock oscillator. A Xtal or externally derived clock (f_{XTAL}) should be connected here. Note that operation of the MX836 without a suitable Xtal or clock input may cause device damage. See Figure 2 (notes).
3	**Serial Clock:** The "C-BUS" serial data clock input. This clock, produced by the µController, is used for transfer timing of commands and data to the MX836. See Timing Diagrams.
4	**Command Data:** The "C-BUS" serial data input from the µController. Data is loaded to the MX836 in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams.
5	**Chip Select ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Timing Diagrams.
6	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS}. See Figure 2.
7	**RX Audio In:** Normally taken from the radio's discriminator output. This input has a 1MΩ internal resistor to V_{BIAS} and requires connecting via a capacitor.
8	**Expand/Store:** A common output that can be used as either an input to an external audio expandor or the input to a voice storage medium such as the MX812. Components relevant to the external device requirements should be used at this output. See Figures 2 and 4.
9	**(Expanded) Audio In:** The audio input, via SW5, from an external expander or audio mixing function. This input has a 1MΩ internal resistor to V_{BIAS} and requires connecting via a capacitor. See Figures 2 and 4.
10	**TX Mod Out:** The composite TX audio output to the transmitter modulator from a variable attenuation stage (11_H). This output is set to V_{BIAS} via an internal 1MΩ resistor when set to Powersave or OFF.
11	**LS Audio Out:** An audio output of the RX Path (or audio selected by SW2 and SW4 Figure 4) for a loudspeaker system. Available for handsfree operation this output is controlled by the RX Gain and LS Volume Command (12_H) and is internally connected to V_{BIAS} when not required. A driver amplifier may be required at this output.

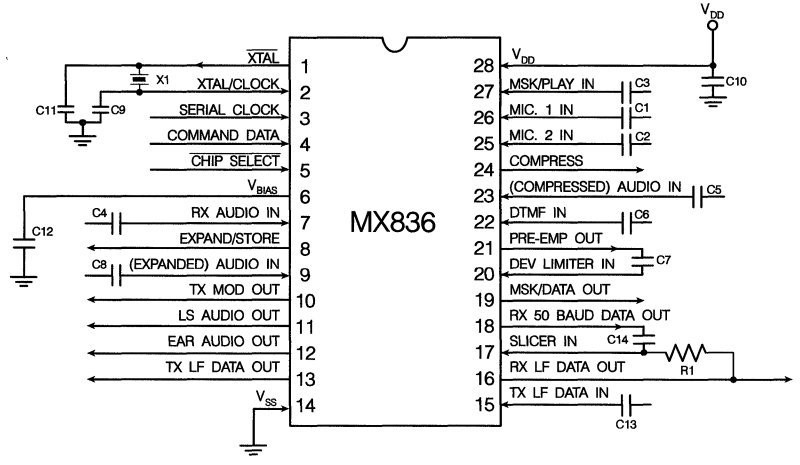
Note: *To minimize aliasing effects, lowpass filtering may be required at the inputs to this device (especially those supplied from switched-capacitor-type devices) to ensure the input spectrum is kept below 63kHz.*

Pin	Function
12	**Ear Audio Out:** An audio output of the RX Path (or audio selected by SW2 and SW4–Figure 4), available as an output for a handset earpiece. Separate from the LS Audio Out function, this output is controlled by the LF Data Gain and Ear Volume Command (13_H) and is internally connected to V_{BIAS} when not required. A driver amplifier may be required at this output.
13	**TX LF Data Out:** The output, if required, to the TX Modulator, of LF (50 baud) filtered and level-adjusted digital data.
14	**V_{SS}:** Negative supply. Signal ground.
15	**TX LF Data In:** The input of LF (50 baud) digital data for transmission, from an external modem. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
16	**RX LF Data Out:** The output, to a 50 baud modem, of the received, filtered, LF data. This pin is used with the 50 Baud Data, Slicer In pins and external components to filter and limit the received LF data. See Figure 4.
17	**Slicer In:** The input to the data slicer. Employed as shown in Figure 4 to filter and limit the received LF data.
18	**RX 50 Baud Data Out:** The output of the received 50 baud data. See Figures 2 and 4.
19	**MSK Out:** The de-emphasized RX audio output available for access to the received MSK data. This output could be directed to an MSK Modem such as the MX439.
20	**Deviation Limiter In:** Input to the on-chip deviation Limiter. This input should be a.c. coupled to the Pre-Emphasis Out pin. The a.c. coupling is required to achieve the best possible symmetry of limiting as this input has a 1MΩ internal resistor to V_{BIAS}. See Figure 2.
21	**Pre-Emphasis Out:** Audio output from the TX Input Gain/Pre-Emphasis function. This output should be a.c. coupled to the Deviation Limiter In pin. See Figures 2 and 4.
22	**DTMF In:** To introduce DTMF type audio, at a suitable level for transmission, to the TX Path, controlled by SW2 (Configuration Command (10_H)). This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
23	**Compression In:** The audio input from an external compression system. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
24	**Compression:** The output to an external audio compression system. Currently available compressor/expanders have Op-Amps incorporated. The compressor can be bypassed by SW2.
25	**Mic.2 In:** TX voice (Mic.) inputs, selectable by SW1 available for handsfree mic./handset mic. or any TX audio input. Pre-amplification may be required prior to these inputs. Each
26	**Mic.1 In:** input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
27	**MSK/Play In:** The TX MSK data input via SW2. This can also be used to input (replay) from a voice storage device such as the MX812. This "replayed" audio can be sent to RX or TX paths allowing a Messaging/Voice Notepad/Answering facility. Both MX439 MSK Modem and MX812 VSR Codec outputs can be wired together at this pin (OR'd) if the functions are activated one-at-a-time. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
28	**V_{DD}:** Positive supply. A single +5 volt power supply is required. Levels and voltages within this audio processor are dependent upon this supply.

C-BUS *is MX-COM's proprietary standard for the transmission of commands and data between a µController and the relevant Cellular IC's. It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions embodied into many types ofµµController. The "C-BUS" data rate is determined solely by the µController. For further details refer to the DBS 800 System Information Document.*

4

Application Information



R_1	=	1.0MΩ	C_4	=	0.1µF	C_8	=	0.1µF	C_{12}	=	1.0µF
C_1		0.1µF	C_5		0.1µF	C_9		33pF	C_{13}		0.1µF
C_2		0.1µF	C_6		0.1µF	C_{10}		0.1µF	C_{14}		0.1µF
C_3		0.1µF	C_7		0.1µF	C_{11}		33pF	X_1		4.032MHz

Tolerances – Resistors ±10% Capacitors ±20%

Figure 2 - Recommended External Components

1. Xtal/clock operation

Operation of any MX-COM IC without a Xtal or clock input may cause device damage. To minimize damage in the event of a Xtal/drive failure, it is recommended that a current limiting device (resistor or fast-reaction fuse) is installed on the power supply (V_{DD}).

2. MSK Modem

The MX439, a general purpose MSK Modem, could be used with this R2000 system Audio Processor. The MX439 is a non-formatted modem, which, with regard to Xtal/clock frequencies and µProcessor interface, is compatible with both Mobile/Portable and Base Station applications.

Reference Signal Levels

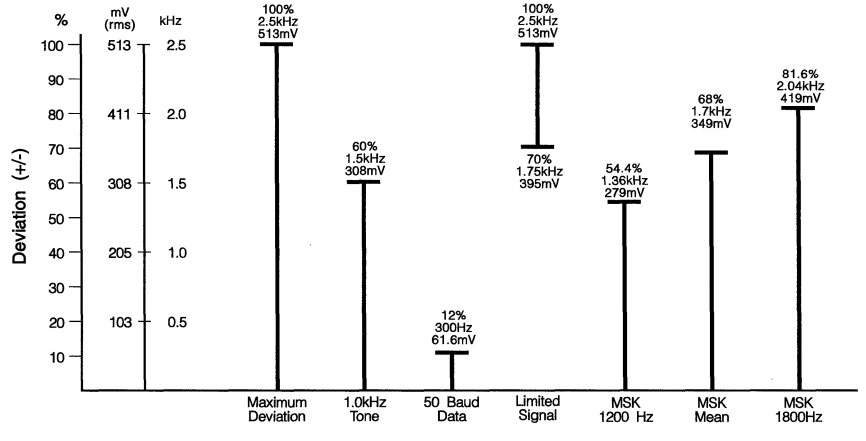


*Figure 3 - R2000 Signal Deviation Levels and corresponding **TX Mod Outputs** with the Mod Level set to 0dB*

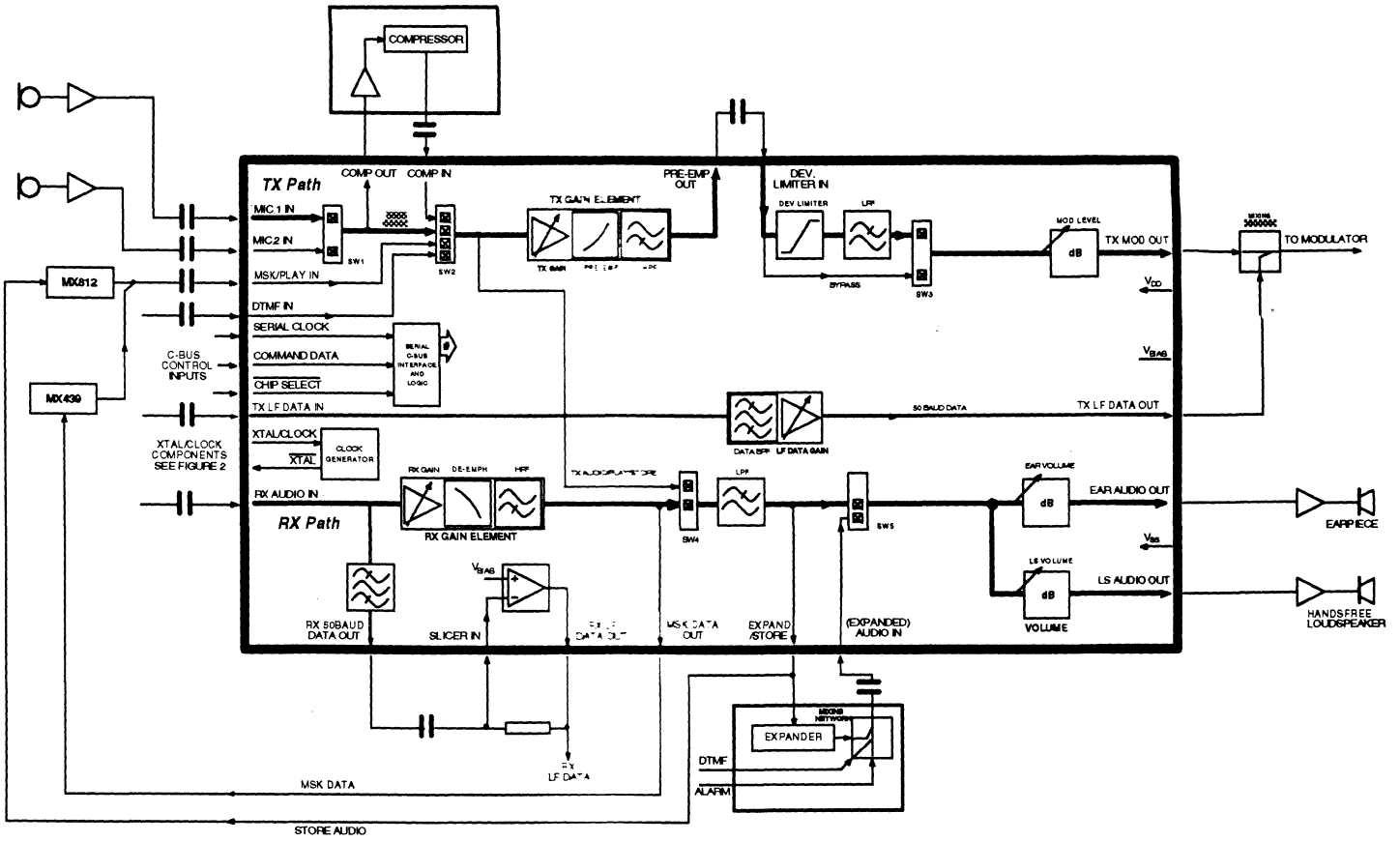


Figure 4 - The MX836 Within an R2000 Cellular System

The Controlling System

C-BUS is designed for low IC pin-count, flexibility in handling variable amounts of data, and ease of design and µController software. It may be used with any µController, and can, if desired, take advantage of hardware and serial I/O functions built into many types of µController. Because of this flexibility and because the data rate is determined solely by the µController, the system designer has complete freedom to choose a µC appropriate to the overall system processing requirements.

Control of the functions and levels within the MX836 R2000 Audio Processor is by a group of Address/Command and appended data instructions from the system microcontroller. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Hex.	Address/Command Binary MSB LSB		Command Data	Table
General Reset	01	0 0 0 0 0 0 0 1			
Configuration Command	10	0 0 0 1 0 0 0 0	+	1 byte	2
TX Gain & Mod. Command	11	0 0 0 1 0 0 0 1	+	1 byte	3
RX Gain & LS Vol.	12	0 0 0 1 0 0 1 0	+	1 byte	4
LF Data Gain & Ear Vol.	13	0 0 0 1 0 0 1 1	+	1 byte	5

Table 1 - C-BUS Address/Commands

In C-BUS protocol the MX836 is allocated Address/Command values 10_H to 13_H. Configuration, TX/RX Gains, and SAT/Powersave assignments and data requirements are given in Table 1.

Each instruction consists of an Address/Command (A/C) byte followed by a data instruction formulated from the following tables.

Commands and Data are only to be loaded in the group configurations detailed, as the C-BUS interface recognized the first byte after $\overline{\text{Chip Select}}$ (logic 0) as an Address/Command. Function or Level control data, which is detailed in Tables 2, 3, 4, and 5, is acted upon at the end of the loaded instruction. See Timing Diagrams, Figures 5 and 6.

Upon power-up the value of the "bits" in this device will be random (either "0" or "1"). A General Reset Command (01_H) is required to set all MX816 registers to 00_H.

Configuration Command *(Preceded by A/C 10_H)*

Setting	Control Bits
(MSB) Bit 7	*Transmitted First* **RX Gain Element**
0	Powersave
1	Enable
6	**All Functions** (except RX Gain Element)
0	Powersave
1	Enable
5	**SW5 Expander**
0	Expander Bypass
1	Expander Route
4	**SW4 TX/RX Audio**
0	TX Store/Audio
1	RX Store/Audio
3	**SW3 Dev. Limiter**
0	Dev. Limiter Bypass
1	Dev. Limiter Route
2	**SW1 Mic. Inputs**
0	Mic. 1 Input
1	Mic. 2 Input
1 0	**SW2 TX Function**
0 0	DTMF In
0 1	Compressor In
1 0	Compressor Bypass
1 1	MSK/Play In

Table 2 - Configuration Commands

TX Gain & Mod. Command *(Preceded by A/C 11_H)*

Setting (MSB) 7 6 5 4	Gain (dB) *Transmitted First* **TX Mod. Level**
0 0 0 0	OFF (Low Z to V_{BIAS})
0 0 0 1	-5.6dB
0 0 1 0	-5.2dB
0 0 1 1	-4.8dB
0 1 0 0	-4.4dB
0 1 0 1	-4.0dB
0 1 1 0	-3.6dB
0 1 1 1	-3.2dB
1 0 0 0	-2.8dB
1 0 0 1	-2.4dB
1 0 1 0	-2.0dB
1 0 1 1	-1.6dB
1 1 0 0	-1.2dB
1 1 0 1	-0.8dB
1 1 1 0	-0.4dB
1 1 1 1	0dB
3 2 1 0	**TX Input Gain**
0 0 0 0	-2.65dB
0 0 0 1	-2.05dB
0 0 1 0	-1.50dB
0 0 1 1	-0.95dB
0 1 0 0	-0.45dB
0 1 0 1	0dB
0 1 1 0	0.45dB
0 1 1 1	0.85dB
1 0 0 0	1.25dB
1 0 0 1	1.65dB
1 0 1 0	2.05dB
1 0 1 1	2.40dB
1 1 0 0	2.70dB
1 1 0 1	3.05dB
1 1 1 0	3.35dB
1 1 1 1	3.65dB

Table 3 - TX Gain & Mod. Commands

The Controlling System

RX Gain & LS Vol. *(Preceded by A/C 12_H)*

Setting				Gain (dB)
(MSB)				*Transmitted First*
7	*6*	*5*	*4*	**RX LS Volume**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-28.0dB
0	0	1	0	-26.0dB
0	0	1	1	-24.0dB
0	1	0	0	-22.0dB
0	1	0	1	-20.0dB
0	1	1	0	-18.0dB
0	1	1	1	-16.0dB
1	0	0	0	-14.0dB
1	0	0	1	-12.0dB
1	0	1	0	-10.0dB
1	0	1	1	-8.0dB
1	1	0	0	-6.0dB
1	1	0	1	-4.0dB
1	1	1	0	-2.0dB
1	1	1	1	0dB
3	*2*	*1*	*0*	**RX Input Gain**
0	0	0	0	3.75dB
0	0	0	1	4.30dB
0	0	1	0	4.80dB
0	0	1	1	5.30dB
0	1	0	0	5.80dB
0	1	0	1	6.20dB
0	1	1	0	6.55dB
0	1	1	1	7.05dB
1	0	0	0	7.40dB
1	0	0	1	7.80dB
1	0	1	0	8.15dB
1	0	1	1	8.50dB
1	1	0	0	8.80dB
1	1	0	1	9.10dB
1	1	1	0	9.40dB
1	1	1	1	9.70dB

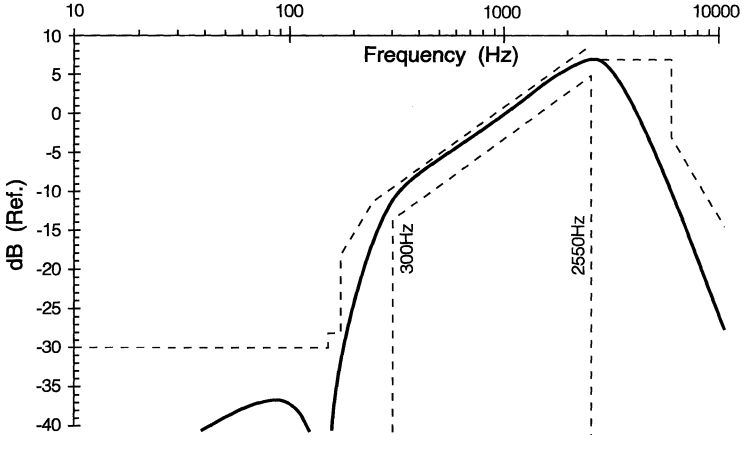
Table 4 - RX Gain and Volume Commands

LF Data Gain & Ear Vol. *(Preceded by A/C 13_H)*

Setting				Gain (dB)
MSB				*Transmitted First*
7	*6*	*5*	*4*	**RX Ear Volume**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-28.0
0	0	1	0	-26.0
0	0	1	1	-24.0
0	1	0	0	-22.0
0	1	0	1	-20.0
0	1	1	0	-18.0
0	1	1	1	-16.0
1	0	0	0	-14.0
1	0	0	1	-12.0
1	0	1	0	-10.0
1	0	1	1	-8.0
1	1	0	0	-6.0
1	1	0	1	-4.0
1	1	1	0	-2.0
1	1	1	1	0
3	*2*	*1*	*0*	**LF** (50 Baud) **Data Gain**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-2.60
0	0	1	0	-2.20
0	0	1	1	-1.80
0	1	0	0	-1.40
0	1	0	1	-1.00
0	1	1	0	-0.70
0	1	1	1	-0.35
1	0	0	0	0
1	0	0	1	0.30
1	0	1	0	0.60
1	0	1	1	0.90
1	1	0	0	1.20
1	1	0	1	1.50
1	1	1	0	1.75
1	1	1	1	2.00

Table 5 - LF Data Gain and RX Ear Vol. Command

System Performance



Mic.1 In to TX Mod Out

V_{DD} = 5.0V

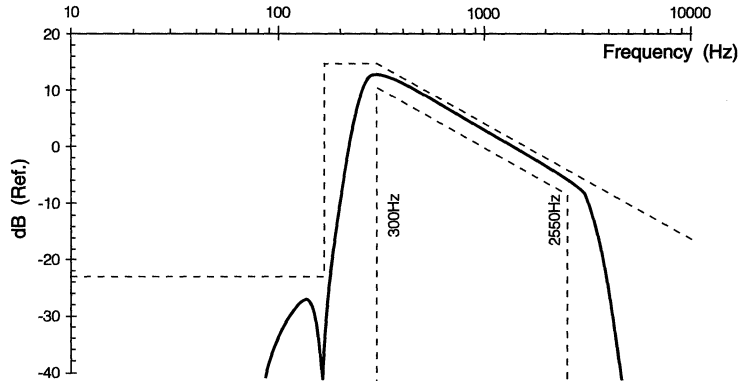
Signal Input Level = 55mVrms

TX Gain set to 0dB

Mod Level set to 0dB

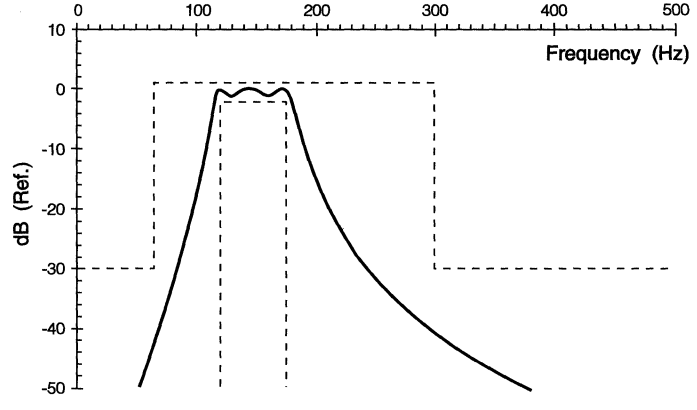
Figure 5 - TX Voiceband Frequency Response

System Performance .....



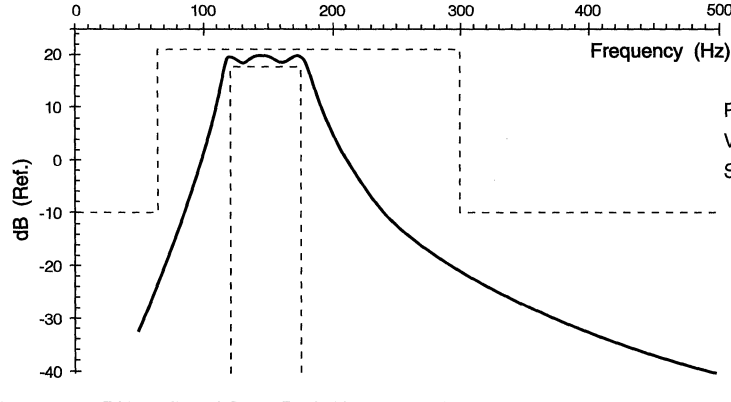
RX Audio In to LS/Ear Audio Out
V_{DD} = 5.0V
Signal Input Level = 68mVrms
RX Gain set to 3.75dB
LS/Ear Volume set to 0dB

Figure 6 - RX Voiceband Frequency Response



TX LF Data In to TX LF Data Out
V_{DD} = 5.0V
Signal Input Level = 55mVrms
LF Data Gain set to 0dB

Figure 7 - TX LF Channel Frequency Response



RX Audio In to RX 50 Baud Data Out
V_{DD} = 5.0V
Signal Input Level = 55mVrms

Figure 8 - RX 50-Baud Data Path Frequency Response

Timing Information

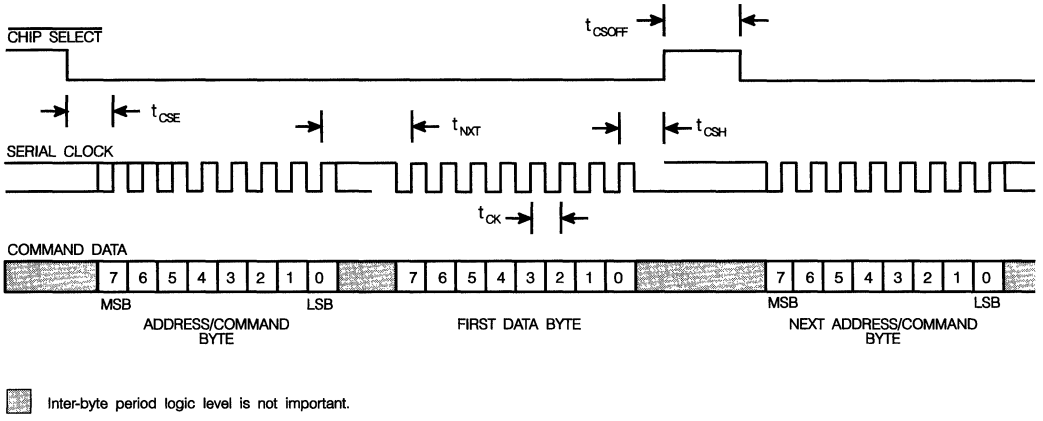


Figure 9 - Control Timing Information

Parameter		See Note	Min.	Typ.	Max.	Unit
"$\overline{CS}$ Enable" to "clock high"	t_{CSE}	1	2.0	-	-	µs
Last "clock high" to "CS high"	t_{CSH}	1	4.0	-	-	µs
"$\overline{CS}$ high" time between transactions	t_{CSOFF}	1,2	2.0	-	-	µs
Clock Cycle Time	t_{CK}	1	2.0	-	-	µs
Inter byte time	t_{NXT}	1	4.0	-	-	µs
Serial Clock-High Period	t_{CH}		500	-	-	ns
Serial Clock-Low Period	t_{CL}		500	-	-	ns
Command Data Set-up Time	t_{CDS}		250	-	-	ns
Command Data Hold Time	t_{CDH}		0	-	-	ns

Notes

1. These minimum timing values are altered during operation of the MX812 VSR Codec.
2. Chip Select must be taken to a logic "1" between each individual transaction.

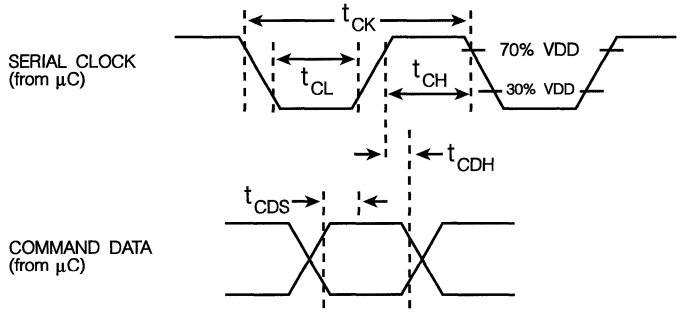


Figure 10 - Control Timing Relationships

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage		-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD}+0.3V)
Sink/source current	(supply pins)	±30mA
	(other pins)	±20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating Temperature		-40°C to +85°C
Storage Temperature		-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/Clock f_0 = 4.032MHz

Audio Level 0dB ref = 308mVrms @ 1kHz

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current - All Operating		–	10.0	–	mA
- RX Data Mode	1	–	2.5	–	mA
- Powersave All		–	0.6	–	mA
Alias Frequency		–	63.0	–	kHz
On-Chip Xtal Oscillator					
R_{IN}		10.0	–	–	MΩ
R_{OUT}		–	10.0	–	kΩ
Inverter Gain		–	10.0	–	V/V
Gain/Bandwidth Product		–	10.0	–	MHz
Analog Input Impedances					
Mic.1 & 2, MSK/Play, Comp. In, DTMF In, TX LF Data In		–	500	–	kΩ
Dev. Limiter In, RX Audio In		–	100	–	kΩ
(Expanded) Audio In		–	47.0	–	kΩ
Slicer In		10.0	–	–	MΩ
Analog Output Impedances					
Pre-Emp Out, TX Mod. Out, Expand/Store, MSK Data Out, TX 50 Baud Data Out		–	600	–	Ω
LS and Ear Audio		–	1.0	–	kΩ
RX LF Data Out		–	2.0	–	kΩ
Switches – ON		–	1.0	–	kΩ
– OFF		10.0	–	–	MΩ
Input Logic "1" Level	2	3.5	–	–	V
Input Logic "0" Level	2	–	–	1.5	V
I_{IN} (Logic "1" or "0")	2	-1.0	–	1.0	µA
Input Capacitance	2	–	–	7.5	pF
TX Signal Path					
Analog Signal Input Levels					
Mic. 1 and 2, MSK/Play, DTMF, Comp. In	3	–	0	–	dB
TX LF Data In		–	0	–	dB
Analog Signal Output Levels					
Pre-Emp Out, TX Mod Out	3	–	0	–	dB
Tx LF Data Out		–	0	–	dB
Path Gains/Levels					
TX Gain – 11_H					
Nominal Adjustment Range		-2.65		3.65	dB
Error of any Setting		-0.2	–	0.2	dB
Dev Limiter					
Threshold		–	1375	–	mVp-p
Symmetry		–	7.0	–	%
Mod Level Attenuation – 11_H					
Nominal Adjustment Range		-5.6		0	dB
Step Size		0.2	0.4	0.6	dB
Error of any Setting		-1.0	–	1.0	dB

Characteristics	See Note	Min.	Typ.	Max.	Unit
TX LF Data Signal Path					
Bandpass Filter					
Passband		120		175	Hz
Gain		–	0	–	dB
LF Data Gain Level – 13_H					
Nominal Adjustment Range		-2.6		2.0	dB
Error of any Setting		-0.2	–	0.2	dB
Overall					
TX Distortion		–	-40.0	-32.0	dBp
TX Hum and Noise		–	-40.0	-20.0	dB
RX Signal Path					
RX Audio Input Level	3	–	-7.0	–	dB
LS/Ear Audio Output Level	3	–	0	–	dB
Path Gains/Levels					
RX Gain – 12_H					
Nominal Adjustment Range		3.75		9.70	dB
Error of any Setting		-0.2	–	0.2	dB
De-Emphasis					
Frequency Range		900	–	2100	Hz
Gain at 1kHz		-1.0	0	1.0	dB
Response		–	-6.0	–	dB/oct
LS/Ear Volume – $12_H/13_H$					
Nominal Adjustment Range		-28.0		0	dB
Step Size		1.5	2.0	2.5	dB
Error of any Setting		-1.0	–	1.0	dB
Overall					
RX Distortion		–	-40.0	-32.0	dBp
RX Hum and Noise		–	-40.0	-34.0	dB
RX 50 Baud AudioPath					
Bandpass Filter					
Passband		120		175	Hz
Gain		19.0	20.0	21.0	dB

Notes

1. With reference to the Configuration Command and Figure 3, all functions with the exception of the RX Gain Element may be powersaved. This will still allow signaling data through the MX836 to activate the system via the µProcessor.
2. Serial Clock, Command Data and Chip Select inputs.
3. Levels equivalent to ±1.5kHz deviation with the settings below:

   TX Gain = 0dB *Mod Level = 0dB*
   RX Gain = 7.05dB *LS/Ear Volume = 0dB*

   Other levels can be achieved by adjusting the above variable gain blocks in accordance with Tables 1 to 5.

4

Section 5: Voice Security

The following section contains specifications on MX•COM's voice inversion devices. For more information see the application note on Variable Split Band (VSB) scrambling in the Applications section of this catalog.

Device	Description	Page	
MX014	Voice Band Inverter	p. 345	
MX214/224	VSB Inverter	p. 351	
MX118	Full-Duplex Scrambler for Cordless Telephones	p. 360	
MX128	Full-Duplex Scrambler for Cordless Telephones	p. 366	**NEW**

SECURITY TYPE	MX-COM DEVICE	SECURITY LEVEL	DESCRIPTION
1. Single Band Frequency Inversion	MX014	Low	Casual eavesdropping prevented. Low-cost.
2. Variable Split Band Frequency Inversion			
a. Fixed Code	MX214 MX224	Low	32 different split points available, of which a handfull are mutually exclusive.
b. Rolling Code	MX1204	Medium	Excellent cost/benefit ratio. Variation of split points, hop rates, and synchronization methods require sophisticated descrambling techniques.
3. Digital Scrambling	MX609 MX619 MX629	High*	All are CVSD Codecs that reduce the size, complexity, and cost of digital scrambling. Speech is converted into binary digits through Continuously Variable Slope Delta modulation technique, then transmitted by digital or analog means.

** depending on encryption algorithm*

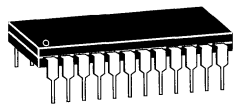
VOICE BAND INVERTER

Features

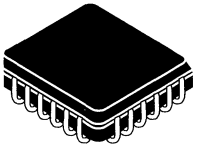
- CTCSS Compatible
- Fixed Frequency Inversion
- Low Power CMOS

Applications

- Land Mobile Radio Systems
- Community Repeaters



MX014J (CDIP)
MX014P (PDIP)
24 pins



MX014LH
(PLCC-24)

Description

The MX014 Voice Band Inverter gives the security of private voice communications to land mobile radio users, as well as to the users of other shared radio channel systems. Designed for use in half-duplex systems, the MX014 exchanges high and low frequencies in the voiceband and renders transmitted messages unintelligible. This privacy function is achieved by a single frequency inversion. When used with CTCSS, *Pvt* SQUELCH™ privacy adaptor operation is achieved.

Sharp cut-off in the internal voiceband filters permits operation with CTCSS and similar sub-audio signaling schemes. This results in high quality recovered audio.

The core of the MX014 consists of two audio band pass filters and a balanced modulator. The device uses a programmable clock divider which controls the carrier and filter cut-off frequencies. Control of the RX/TX, PTL and privacy function is by pin selection.

The MX014 operates from a single 5V supply and uses a 4 MHz crystal oscillator to ensure the correct pitch in recovered speech. Signal coupling and decoupling are the only external components needed.

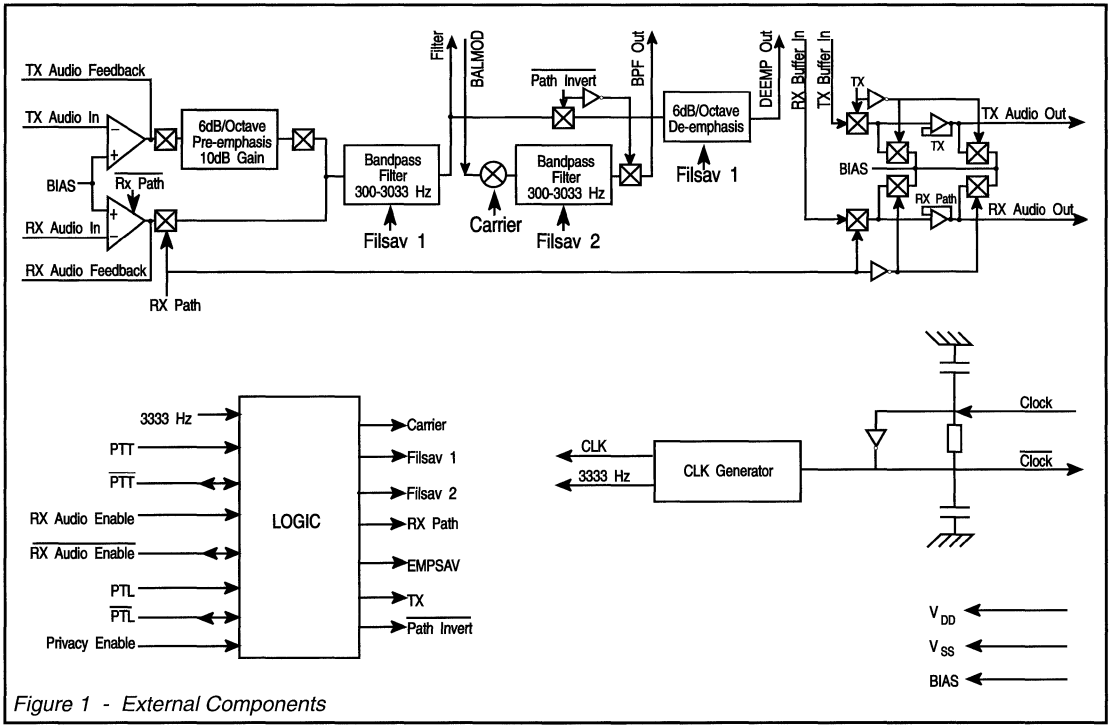


Figure 1 - External Components

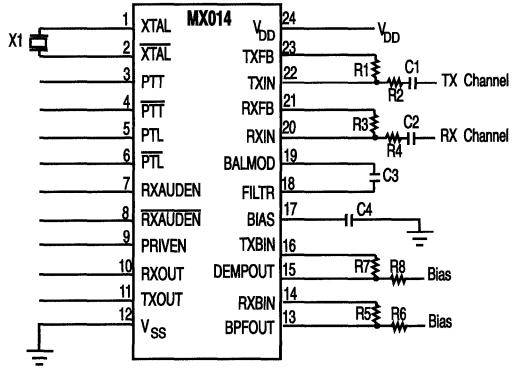
PIN FUNCTION TABLE

Pin	Function
1	XTAL: An external 4 MHz clock can be applied to this input. The clock circuit on chip has a resistor and capacitors so that only one external crystal is required.
2	$\overline{\text{XTAL}}$: This is the inverted 4 MHz clock output for use when a crystal oscillator is used, or as a buffer for driving other clocked devices.
3	PTT: Push To Talk is an input with a 3 MΩ pull-down resistor.
4	$\overline{\text{PTT}}$: This is the inverted PTT output. It has a 100 kΩ output impedance.
5	PTL: Push To Listen is an input with a 3 MΩ pull-down resistor.
6	$\overline{\text{PTL}}$: $\overline{\text{Push To Listen}}$ is the inverted output of PTL; it has a 100 kΩ output impedance.
7	RXAUDEN: RX Audio Enable is an input with a 3 MΩ pull-down resistor.
8	$\overline{\text{RXAUDEN}}$: $\overline{\text{RX Audio Enable}}$ is the inverted output of RX Audio Enable; it has a 100 kΩ output impedance.
9	PRIVEN: Privacy Enable controls the input action of the balanced modulator by switching the carrier clock. When audio signals are inverted, the signal path gain is adjusted automatically to compensate for the upper sideband loss. It contains a 3MΩ pull-up resistor.
10	RXOUT: This is the receive audio output pin. It is biased at $V_{DD}/2$ when in the TX mode.
11	TXOUT: This is the "send" voice output pin. It is biased at $V_{DD}/2$ when in RX mode.
12	V_{SS}: The negative supply pin (ground).
13	BPFOUT: For a gain of one in the RX Output stage, these two pins are wire linked together. However, if gain is introduced
14	RXBIN: at the RX input, attenuation may be introduced at the RX Output using these pins and two resistors.
15	DEMPOUT: The pre-emphasis circuit has a 10 dB gain at 1 kHz. Additional gain or attenuation can be
16	TXBIN: introduced as in the RX path.
17	BIAS: This is the internally generated $V_{DD}/2$ decoupling pin.
18	FILTR: This filter is the output of the Input Audio BPF and must be a.c. coupled into the Balanced Modulator Input through a 0.1 μF capacitor.
19	BALMOD: This is the input to the balanced modulator. It must be a.c. coupled to the Filter Output.
20	RXIN: This is a negative input of an op-amp at the input of the RX path. It can be used, along with RX Audio Feedback and two external resistors, to increase the signal to its optimum level prior to frequency inversion/filtering. This may improve the S/N.
21	RXFB: RX Audio Feedback is the output of an op-amp at the input of the RX path. See RXIN.

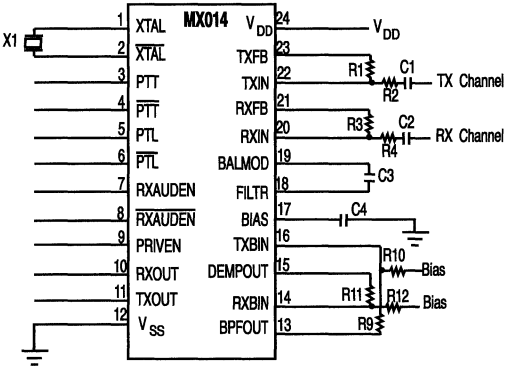
PIN FUNCTION TABLE

Pin	Function
22	TXIN: The negative input of an op-amp at the input of the TX path. It can be used, along with TX Audio Feedback and two external resistors, to increase the signal to its optimum level prior to frequency inversion/filtering. This may improve S/N.
23	TXFB: TX Audio Feedback is the output of an op-amp at the input of the TX path. See TXIN.
24	V_{DD}: The positive supply pin.

Configuration for Radios with Existing Pre- and De-emphasis.



For Use in Radios without Pre- and De-emphasis.



TX Attenuation = $\frac{R8}{R7 + R8}$

For a gain of 1,
R8 = ∞, R7 = 0

RX Attenuation = $\frac{R6}{R5 + R6}$

For a gain of 1,
R6 = ∞ , R5 = 0

TX Attenuation = $\frac{R10}{R9 + R10}$

For a gain of 1,
R9 = 0 , R10 = ∞

RX Attenuation = $\frac{R12}{R11 + R12}$

For a gain of 1,
R11 = 0 , R12 = ∞

Component Values: C1- C3 = 0.1 µF, C4 = 1.0 µF, X1 = 4 MHz crystal
R1 to R12 values will depend on the configuration and the gain or attenuation required. However R1, R3, R5, R7, and R11 should be 100 kΩ or greater. To add gain or attenuate, use R5-R12 as shown. See pin descriptions for more information.

Figure 2 - External Component Connections

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 V to V_{DD} + 0.3 V
Current:	
into or out of V_{DD} or V_{SS} pins	30mA max.
into or out of any other pin	20 mA max.
Maximum Device Dissipation @ T_{AMB} = 25°C	800mW
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.

V_{DD}=5.0V

T_{AMB}=25°C

0 dB ref. = 300 mVrms *

Clock Frequency = 4 MHz

*NOTE: Measured at pin 18, the FILTR output. This pin must not exceed 300 mVrms at 1 kHz in TX and 500 mVrms at any frequency in RX, or clipping may occur. The difference in levels is due to the pre-emphasis filter in the TX path.

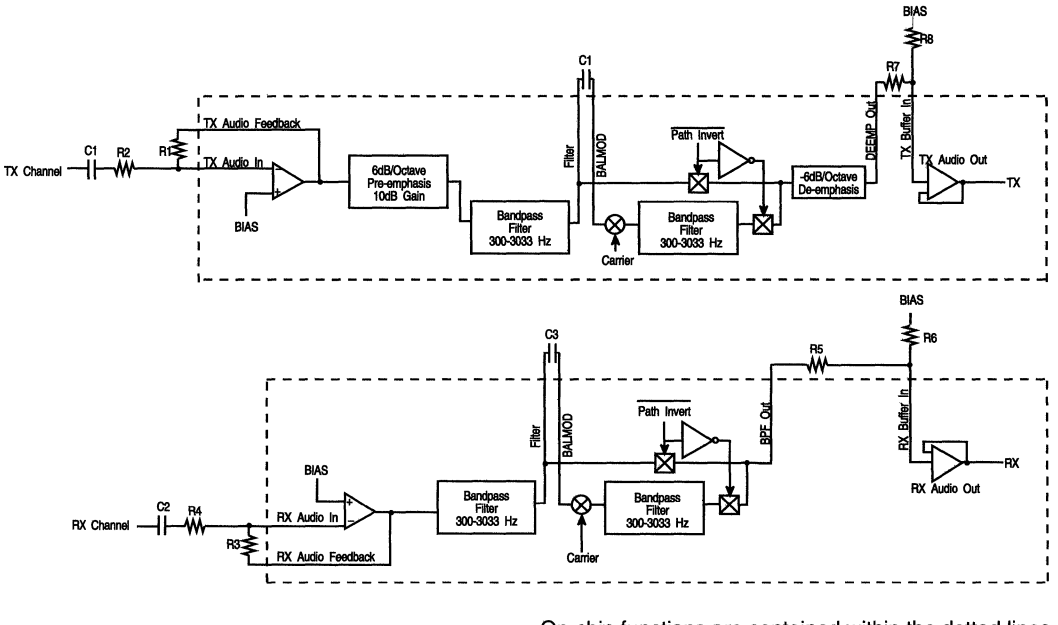
Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V_{DC}
Supply Current:					
RX/TX Operating (Private)				9.0	mA
RX/TX Operating (Clear)				6.0	mA
Standby	4			1.8	mA
Audio Input Impedance			10		MΩ
Audio Output Impedance	5		0.5		kΩ
Digital Output Impedance(Pulldown)		1			MΩ
Digital I/O Impedance			100		kΩ
Input Logic "1"		70%			V_{DD}
Input Logic "0"				30%	V_{DD}
RX Clear Performance					
Total Harmonic Distortion	1		2	5	%
Output Noise Level	2		2		mVrms
Passband Gain			0		dB
Passband Ripple (300-3033 Hz)	1	-2		+2	dB
Stopband Attenuation					
(fin > 3333 Hz)			20		dB
(fin > 3633 Hz)			45		dB
(fin < 250 Hz)			42		dB
RX Inverted					
Total Harmonic Distortion	1,3		4		%
Output Noise Level	2,3		4		mVrms
Passband Ripple (300 - 3033 Hz)	3			4	dB
Stopband Attenuation					
(fin > 3333 Hz)			50		dB
(fin > 3633 Hz)			60		dB

5

Characteristics	See Note	Min.	Typ.	Max.	Unit
Highpass Attenuation					
(fin < 250 Hz)			60		dB
TX Clear					
Total Harmonic Distortion	1		2	5	%
Output Noise Level	2		2		mVrms
Passband Gain					
(fin = 300 - 3033 Hz)	1		0		dB
Passband ripple					
(fin = 300 - 3033 Hz)	1			3	dB
Stopband Attenuation					
(fin > 3333 Hz)	2		20		dB
(fin > 3633 Hz)			45		dB
(fin < 250 hz)			42		dB
TX Inverted					
Total Harmonic Distortion	1,3		4		%
Output Noise Level	2		4		mVrms
Passband Ripple					
(fin = 300 - 3333 Hz)	1,3			4	dB
Stopband Attenuation					
(fin > 3333 Hz)	3		50		dB
(fin > 3633 Hz)	3		60		dB
(fin < 250 Hz)	3		60		dB
Pre-Emphasis					
Frequency Response			6		dB/Octave
Gain at 1 kHz			10		dB
De-emphasis					
Frequency response			-6		dB/Octave
Gain at 1 kHz			0		dB

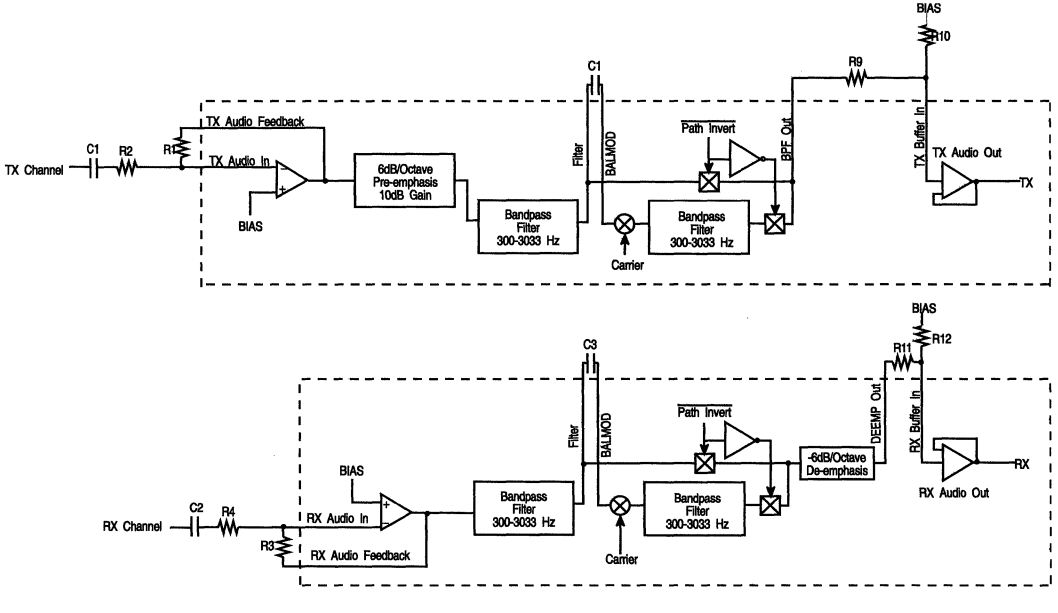
Notes:

1. *Input signal = 1kHz tone 0dB (300 mV rms).*
2. *Input AC short circuit, audio path enabled. Measured in 30 kHz band.*
3. *Due to frequency inversion (and pre- and de-emphasis), this refers to deviation from expected ideal response.*
4. *Standby occurs in RX with RX Audio Enable = 0, RX Audio Enable = 1, and PTL = 1.*
5. *TX Audio Out and RX Audio Out only.*



On-chip functions are contained within the dotted lines.

Figure 3 - Voice Privacy Application (Add-on)



On-chip functions are contained within the dotted lines.

Figure 4 - Voice Processing Application (OEM)

MX·COM, INC.

MX214
MX224

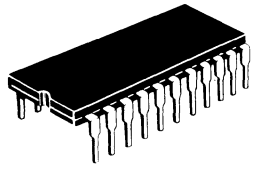
VARIABLE SPLIT BAND INVERTER

FEATURES:

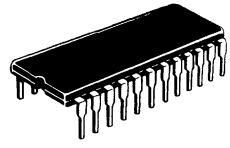
- CTCSS Highpass Filter
- Good Recovered Audio Quality
- Fixed and Rolling Code Modes
- Serial/Parallel Loading Options
- 32 Programmable Split Points
- Half-Duplex Capability

APPLICATIONS:

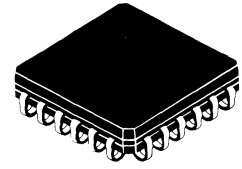
- Mobile Radio Voice Security
- Cellular Telephone Voice Security



MX214J (CDIP)
MX214P (PDIP)
22 pins



MX224J (CDIP)
MX224P (PDIP)
24 pins



MX214LH
MX224LH
(24p PLCC)

5

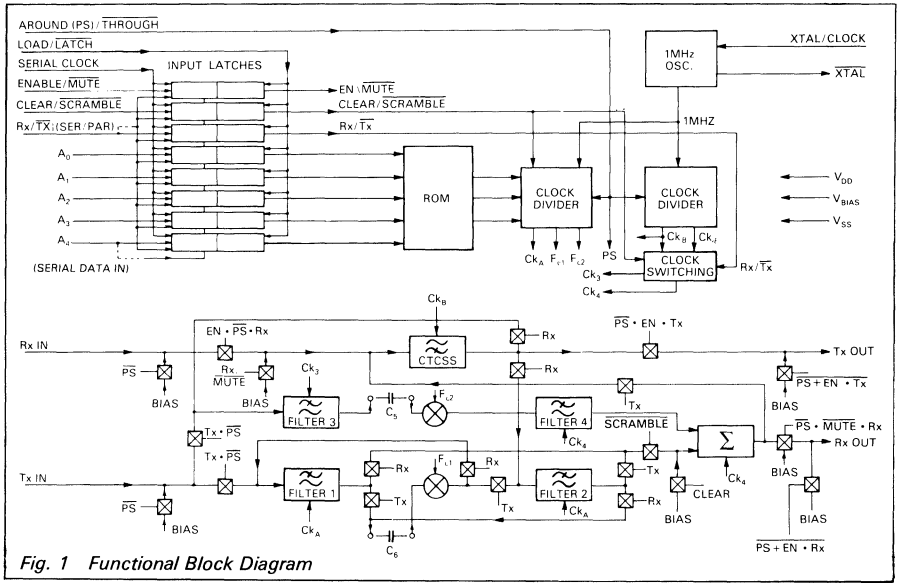


Fig. 1 Functional Block Diagram

DESCRIPTION:

The MX214/MX224 Variable Split Band Inverters are designed for mobile and cellular radio voice security applications. Digital control functions are loaded serially into the MX214. The MX224 is loaded in parallel.

The MX214/MX224 ICs include a highpass filter which rejects subaudio frequencies, ensuring full CTCSS compatibility. This CTCSS filter is not included on the earlier-generation MX204 VSB Inverter.

The MX214/ MX224 splits the voiceband (300-2700 Hz) into upper and lower subbands, and inverts each subband about itself. The "split point" (defined as the frequency where the voice band is subdivided), is externally programmable to 32 distinct values in the 300 to 3000 Hz range. In the "fixed code" mode, a single split point is used. Fixed mode operation nets approximately 4 mutually exclusive voice channels.

In "rolling code" mode, the split point is changed many times per second, usually under control of a microprocessor. Rolling code scrambling requires synchronization, offers higher security than fixed code operation, and provides a much greater number of mutually exclusive secure channels.

The MX214/224 offers a recovered audio product close to that of a telephone. The on-chip "Mute" function is useful when implementing rolling code continuous synchronization schemes. "Powersave" and "Clear/Scramble" controls are also included on-chip. Timing and filter clocks are derived internally from an on-chip 1 MHz reference oscillator driven by a 1 MHz crystal or clock pulse input.

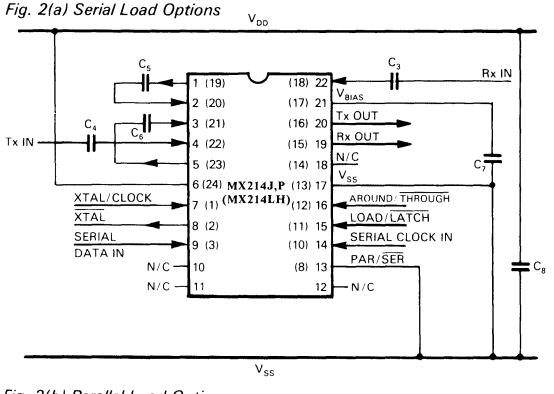
APPLICATIONS INFORMATION:

Recommended external component connections are shown in Figure 2. In "Scramble" mode, split point frequencies are selected and set in accordance with the ROM address code present at the inputs A_0 to A_4(see Table 2). In "Clear" mode, both the Upper and Lowerband filter limits are used (see Figures 5 or 6), the carrier frequencies are turned off, and the balanced modulators are bypassed internally. The Low Band audio is removed from the output signal prior to summing.

The MUTE function disables the MX214/224's audio outputs to allow periodic transmission of synchronization data. A logic "0" at this input isolates the device while leaving the audio input and output pins at bias level (see Table 1). When the MX214/224 is in POWERSAVE mode, audio signals may be hardwired around the device since the input and output pins are open circuit (see Table 1).

Component Connections

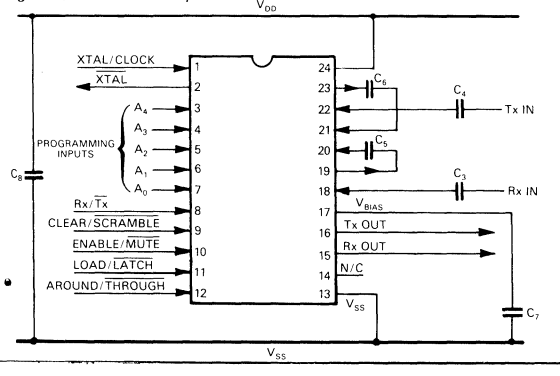
Fig. 2(a) Serial Load Options

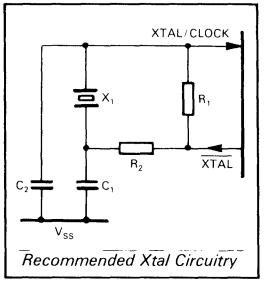


Component References	
Component	Unit Value
R_1	1M
R_2	Selectable
C_1	33p
C_2	68p
C_3	15n
C_4	15n
C_5	1.0µ
C_6	1.0µ
C_7	1.0µ
C_8	1.0µ
X_1	1MHz

Tolerance Resistors ± 10%
Capacitors ± 20%
C_5 and C_6 are coupling capacitors between filter outputs and balanced modulator inputs.

Fig. 2(b) Parallel Load Options





Recommended Xtal Circuitry

MX214/224 PIN FUNCTION TABLE

PIN NUMBER				FUNCTION
214 J,P	224 J,P	214 LH	224 LH	
7	1	1	1	**Xtal/Clock:** Input to the clock oscillator inverter. A 1 MHz xtal input or externally derived 1 MHz clock is injected here.
8	2	2	2	**$\overline{\text{Xtal}}$:** Output of the clock oscillator inverter.
9	—	3	—	**Serial Data Input:** This pin is used to input an 8-bit word representing the digital control functions. This word is loaded using the serial data clock and is input in the following sequence: MUTE, CLEAR, Rx/$\overline{\text{Tx}}$, A_0, A_1, A_2, A_3, A_4. The load/$\overline{\text{latch}}$ pin is operated on completion. Reference the timing diagram in Figure 7.
—	3	—	3	A_4 ┐ **Programming Inputs:** In parallel mode, these five digital inputs define the
—	4	—	4	A_3 ┤ split point frequency. Each of the 5 input pins have a 1MΩ internal pullup
—	5	—	5	A_2 ┤ resistor. See Table 2 for programming information.
—	6	—	6	A_1 ┤
—	7	—	7	A_0 ┘
—	8	—	8	**Rx/$\overline{\text{Tx}}$:** This digital input selects the Receive or Transmit paths and configures upperband and lowerband filter bandwidths while setting the CTCSS highpass filter position on the signal path. See Table 1 and Figures 5 and 6. 1MΩ internal pullup resistor (Rx).
13	—	8	—	**Parallel/$\overline{\text{Serial}}$:** This pin must be connected to V_{ss} for serial loading. Internal 1MΩ pullup resistor.
—	9	—	9	**Clear/$\overline{\text{Scramble}}$:** This digital input puts the device into "Clear" or "Scramble" mode by controlling the application of carrier frequency to the Upper and Lower band balanced modulators. In "Scramble" mode, the balanced modulator carrier frequency values are selected by the split point address A_0-A_4 (Table2). In "Clear" mode, the carriers are disabled and the balanced modulators are bypassed internally, i.e. the lower band signal is not added to the output signal. 1MΩ internal pullout resistor (Clear).
—	10	—	10	**Enable/$\overline{\text{Mute}}$:** This digital function is used to disable Receive or Transmit signal paths for rolling code synchronization while maintaining bias conditions. Synchronization data can be transmitted during the Mute periods, as is done in the MX1204 VSB Scrambler module. Internal 1MΩ pullup resistor (Enable).
14	—	10	—	**Serial Clock Input:** This is the externally applied data clock frequency used to shift input data along on devices wired in the Serial loading mode. One full data clock cycle is required to shift one data bit completely into the register. See Timing Diagram (Figure 7). 1MΩ internal pullup resistor.
15	11	11	11	**Load/$\overline{\text{Latch}}$:** This pin controls the loading of the 8 digital function inputs (ENABLE, CLEAR, Rx/Tx, A_0-A_4) into the internal register. When this pin is at logic "1," all eight inputs are transparent and new data acts directly. For controlled changing of parameters in the parallel mode, Load/$\overline{\text{Latch}}$ must be kept at logic "0" while a new function is loaded, then strobed 0-1-0 to latch the inputs in. For serial loading, the serial data should be loaded with Load/$\overline{\text{Latch}}$ at logic "0" and then Load/$\overline{\text{Latch}}$ strobed 0-1-0 on completion of data loading. Internal 1MΩ pullup resistor (Load). See Figure 7.

5

MX214/224 PIN FUNCTION TABLE

PIN NUMBER				FUNCTION
214 J,P	224 J,P	214 LH	224 LH	
16	12	12	12	**Powersave:** This digital input is used to place the MX214/224 into Powersave mode, where all parts of the device except for the 1 MHz oscillator are shut down. All signal input and output lines are made open circuit, free of all bias. This allows signal paths to be routed externally around the device, while reducing current consumption. A logic "0" at this input enables the device to work normally as shown in Table 1. Internal 1MΩ pullup resistor.
17	13	13	13	**V_{SS}:** Negative Supply (GND).
18	14	14	14	**Internal Connection:** This pin is internally connected. Leave open circuit.
19	15	15	15	**Rx Output:** This is the processed received audio signal output. This pin is held at a DC "bias" voltage for all functions except Powersave. This buffered output is driven by the Summing circuit in the Rx mode. Signal paths and bias levels are detailed in Table 1 and Figure 6.
20	16	16	16	**Tx Output:** This is the processed audio output for the transmission channel. This pin is held at a DC "bias" for all functions except Powersave. This summed and buffered signal is passed through the CTCSS High Pass Filter to the output pin in the Tx mode. Signal paths and bias levels are detailed in Table 1 and Figure 5.
21	17	17	17	**V_{BIAS}:** Normally at $V_{DD}/2$, this pin requires an external decoupling capacitor (C_7) to V_{SS}.
22	18	18	18	**Rx Input:** This is the analog received audio signal input. This pin is held at a DC "bias" voltage by a 300 Kohm on-chip bias resistor which is selected for all functions except Powersave. It must be connected to external circuitry by capacitor C_3 (See Figure 2). This input is routed through the CTCSS High Pass Filter in Rx mode to remove subaudio frequencies from the voiceband. Signal paths and bias levels are detailed in Table 1 and Figure 6.
1	19	19	19	**Highband Filter Output:** The output of the Input Filter of the Upperband limit. The $Rx/\overline{Tx}$ function sets the lowpass filter at 3400 Hz or 2700 Hz respectively. This output must be connected to the Highband Balanced Modulator input via capacitor C_5 (See Figure 2).
2	20	20	20	**Highband Balanced Modulator Input:** The input to the Balanced Modulator of the Upperband limit. This input must be connected to the Highband Filter Output via capacitor C_5 (See Figure 2).
3	21	21	21	**Lowband Balanced Modulator Input:** The input to the Balanced Modulator of the Lowerband limit. This input must be connected to the Lowband Filter Output via capacitor C_6 (See Figure 2).
4	22	22	22	**Tx Input:** This is the analog "Clear" audio input for the VSB scrambler. This pin is held at a DC "bias" voltage by a 300 Kohm on-chip bias resistor, which is selected for all functions except Powersave. It must be connected to external circuitry by capacitor C_4 (See Figure 2). This input, in the Tx mode, is connected to Upper and Lowerband input filters. Signal paths and bias levels are detailed in Table 1 and Figure 5.

MX214/224 PIN FUNCTION TABLE

PIN NUMBER				FUNCTION
214 J,P	224 J,P	214 LH	224 LH	
5	23	23	23	**Lowband Filter Output:** The output of the Input Filter of the Lowerband limit. The Rx/$\overline{Tx}$ function determines which filter is used (Filter 1 or 2). See figures 5 and 6. This output must be connected to the Lowband Balanced Modulator Input via capacitor C_6 (See Figure 2).
6	24	24	24	**V_{DD}:** A single + 5V supply is required.

Note: Pins 10, 11, and 12 on the MX214J and MX214P are not connected. Pins 4, 5, 6, 7 and 9 on the MX214LH are not connected.

MX214/224 TRUTH TABLE

	Rx/$\overline{Tx}$ = 1	Rx/$\overline{Tx}$ = 0	$\overline{MUTE}$ = 0	POWERSAVE
Rx Path	Enabled	Disabled	Disabled	Disabled
Rx Out Level	Bias	Bias	Bias	High Impedance
Tx Path	Disabled	Enabled	Disabled	Disabled
Tx Out Level	Bias	Bias	Bias	High Impedance

TABLE 1 FUNCTIONS INFLUENCING SIGNAL PATHS

5

APPLICATIONS INFORMATION

The term "MX214" can be taken to mean MX214 or MX224.

Audio Quality

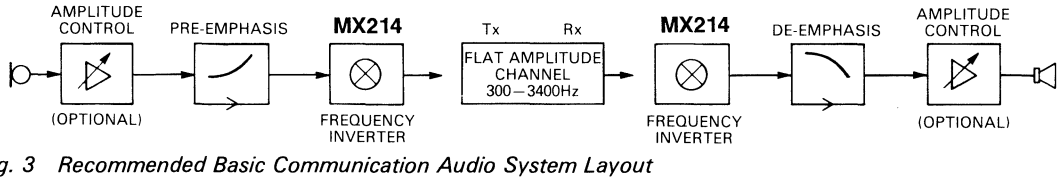


Fig. 3 Recommended Basic Communication Audio System Layout

Figure 3 shows the recommended basic audio system layout using added pre- and deemphasis circuitry to maintain good recovered speech quality. In the Transmit mode, *Do Not* preemphasise the audio output of the MX214. In the Receive mode, deemphasis should be used after the MX214.

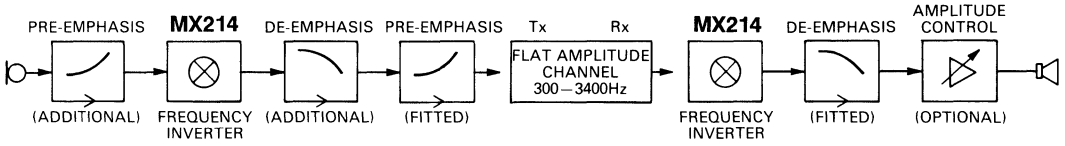


Fig. 4 Recommended Basic Radio Communication Audio System Layout

Figure 4 shows the recommended basic audio system layout if it is necessary to install the MX214 within a radio having pre- and deemphasis circuitry as a standard. This is where post-emphasis access is not possible in the transmitter.

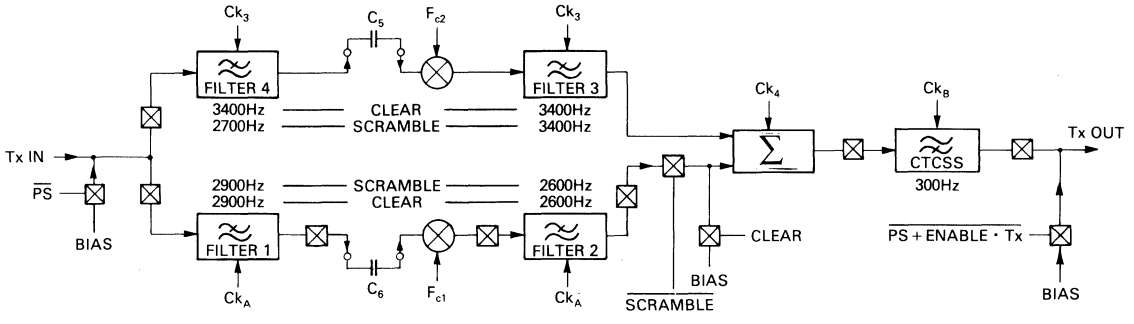


Fig. 5 Basic Tx Path

During the Transmit function the Low Pass and CTCSS filters are configured automatically as shown in Figure 5, with cut-off frequencies (-3dB) indicated.

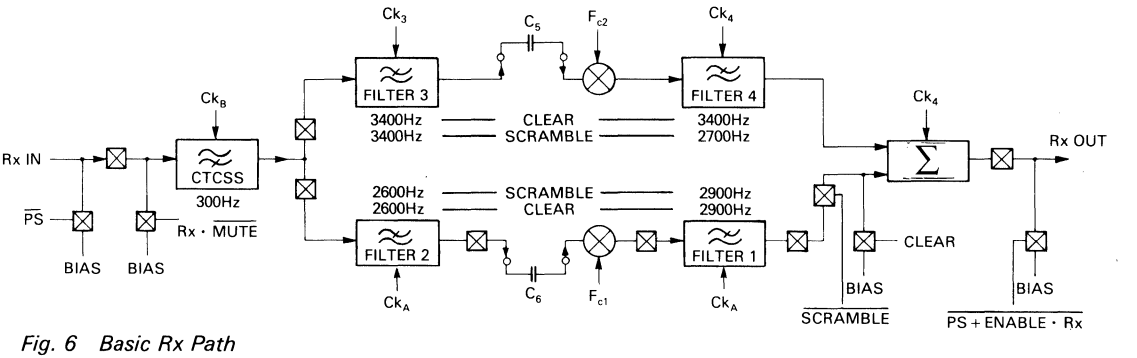


Fig. 6 Basic Rx Path

During the Receive function the Low Pass and CTCSS filters are configured automatically as shown in Figure 6, with cut-off frequencies (-3dB) indicated.

MX214/224 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref. V_{ss} = 0V)		−0.3V to (V_{DD} + 0.3V)
Sink/source current (supply pins)		±30mA
(other pins)		±20mA
Total device dissipation @ 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	MX214J/224J	−30°C + 85 °C (Ceramic)
	MX214P/214LH/224P/224LH	−30°C + 70°C (Plastic)
Storage temperature range:	MX214J/224J	−55°C to + 125° (Ceramic)
	MX214P/214LH/224P/224LH	−40° to + 85°C (Plastic)

Operating Limits:

All characteristics measured using the following parameters unless otherwise specified:

V_{DD} = 5.0V, T_{amb} = 25°C, F_{clk} = 1.0MHz, Audio Level Ref: 0dB = 775 mVrms.

Characteristics	See Note	Min	Typ	Max	Unit
Static Values					
Supply Voltage		4.5	5	5.5	V
Supply Current (Enabled)		—	8	—	mA
Supply Current (Powersave)		—	1.2	—	mA
Analog Input Impedances					
Tx/Input (Enabled)		—	100	—	kΩ
Tx/Rx Input (Powersave)		1	—	—	MΩ
Balanced Modulator		—	40	—	kΩ
Analog Output Impedances					
Rx Output (Tx Mode)		—	100	—	kΩ
Rx Output (Rx Mode)		—	—	2	kΩ
Rx Output (Powersave)		1	—	—	MΩ
Tx Output (Tx Mode)		—	—	2	kΩ
Tx Output (Rx Mode)		—	100	—	kΩ
Tx Output (Powersave)		1	—	—	MΩ
Input LPF		—	—	1	kΩ
Digital Values					
Digital Input Impedance		100	—	—	kΩ
Dynamic Values					
Input Logic '1'		3.5	—	—	V
Input Logic '0'		—	—	1.5	V
Xtal/Clock Frequency		—	1	—	MHz
Analog Input Level		−18	—	+6	dB
Carrier Breakthrough	1	—	−55	—	dB
Baseband Breakthrough	1, 2 or 3	—	−33	—	dB
Filter Clock Breakthrough	1, 2, or 3	—	−50	—	dB
Output Noise	1, 4	—	−45	—	dB

MX214/224 ELECTRICAL SPECIFICATIONS (cont.)

Characteristics	See Note	Min	Typ	Max	Unit
Passband Characteristics					
Clear Mode	7				
Passband Gain		—	0	—	dB
Output Lower 3dB Point (Rx or Tx)		—	300	—	Hz
Output Upper 3dB Point (Rx or Tx)		—	3400	—	Hz
Scramble-Descramble	5				
Received Signal Passband Gain	6	—	0	—	dB
Received Signal Lower 3dB Point		—	400	—	Hz
Received Signal Upper 3dB Point		—	2700	—	Hz
Transmitted Signal Lower 3dB Point		—	300	—	Hz
Transmitted Signal Upper 3dB Point		—	3400	—	Hz
CTCSS (Highpass Filter)					
−3dB Point		—	300	—	Hz
Passband Gain		—	0	—	dB
Stopband Attenuation at f < 250 Hz		—	40	—	dB
Timing *(Figure 7)*					
Serial Mode Enable Set Up (t_{SMS})		250	—	—	ns
Serial Clock 'High' Pulse Width (t_{PWH})		250	—	—	ns
Serial Clock 'Low' Pulse Width (t_{PWL})		250	—	—	ns
Data Set Up Time (t_{DS})		150	—	—	ns
Data Hold Time (t_{DHS})		50	—	—	ns
Load/$\overline{\text{Latch}}$ Set Up Time (t_{LL})		250	—	—	ns
Load/$\overline{\text{Latch}}$ Pulse Width (t_{LLW})		150	—	—	ns
Data Set Up Time(t_{DSP})		150	—	—	ns
Data Hold Time (t_{DHP})		20	—	—	ns

Notes: *1. Measured at the output of a single device.*
2. Tx Mode.
3. Rx Mode.
4. With input A.C. short-circuited to V_{ss}.
5. Measured at the output of a receiving device in a scrambler-descrambler system with a transmission channel having a flat amplitude response and a bandwidth of 300Hz to 3400 Hz and measured relative to the input signal at the transmitting device.
6. Excluding split point ± 150 Hz.
7. Measured at the Rx or Tx output pin of a single device.

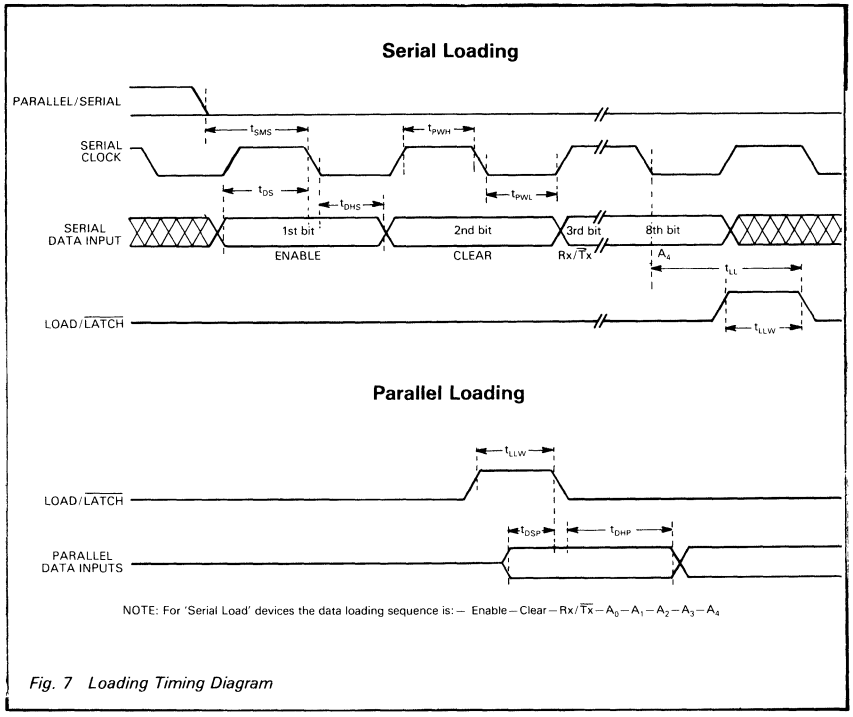


Fig. 7 Loading Timing Diagram

ROM Address A_4–A_0	Split Point Hz	Low Band Carrier, Hz f_{c_1}	High Band Carrier, Hz f_{c_2}	ROM Address A_4–A_0	Split Point Hz	Low Band Carrier, Hz f_{c_1}	High Band Carrier, Hz f_{c_2}
00000	2800	3105	6172	10000	1135	1436	4504
00001	2625	2923	6024	10001	1050	1351	4424
00010	2470	2777	5813	10010	976	1278	4347
00011	2333	2631	5681	10011	913	1213	4310
00100	2210	2512	5555	10100	857	1157	4273
00101	2100	2403	5494	10101	792	1094	4166
00110	2000	2304	5376	10110	736	1037	4132
00111	1909	2212	5263	10111	688	988	4065
01000	1826	2127	5208	11000	636	936	4032
01001	1750	2049	5102	11001	591	891	3968
01010	1680	1984	5050	11010	552	853	3937
01011	1555	1858	4950	11011	512	813	3906
01100	1448	1748	4807	11100	471	772	3846
01101	1354	1655	4716	11101	428	728	3816
01110	1272	1572	4629	11110	388	688	3787
01111	1200	1501	4587	11111	350	650	3731

Table 2 ROM Address Programming Table

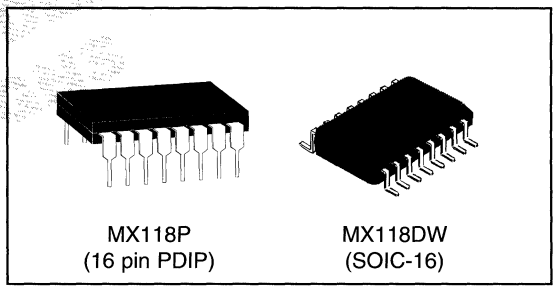
FULL-DUPLEX SCRAMBLER FOR CORDLESS TELEPHONES

Features

- **Full-Duplex Audio Processing**
- **On-Chip "Brick-wall" Filters (300-3000 Hz)**
- **Low Voltage CMOS**
- **High Baseband and Carrier Rejection**
- **Excellent Audio Quality**
- **ECPA* Qualified Voice Protection**

Applications

- **Cordless Telephones & Wireless PBXs**
- **Battery Powered Portability**



MX118P (16 pin PDIP) MX118DW (SOIC-16)

Description

The MX118 is a full-duplex frequency inversion scrambler that secures cordless telephone conversations. The two audio paths, C1 and C2, are identical and independent. Each consists of the following:

1) A 10th order lowpass filter cut off at 3.1 kHz.
2) A balanced modulator with high baseband and carrier rejection.
3) A 3.3 kHz inversion carrier (injection tone).
4) A 14th order bandpass filter (300-3000 Hz).
5) Input op-amps with externally adjustable gain.

The MX118 uses CMOS switched-capacitor filter technology and operates from a single supply in the range of 3.0 V to 5.5 V. The inversion carrier's frequency and filter switching clock are generated on-chip using an external 4.433619 MHz crystal or clock input.

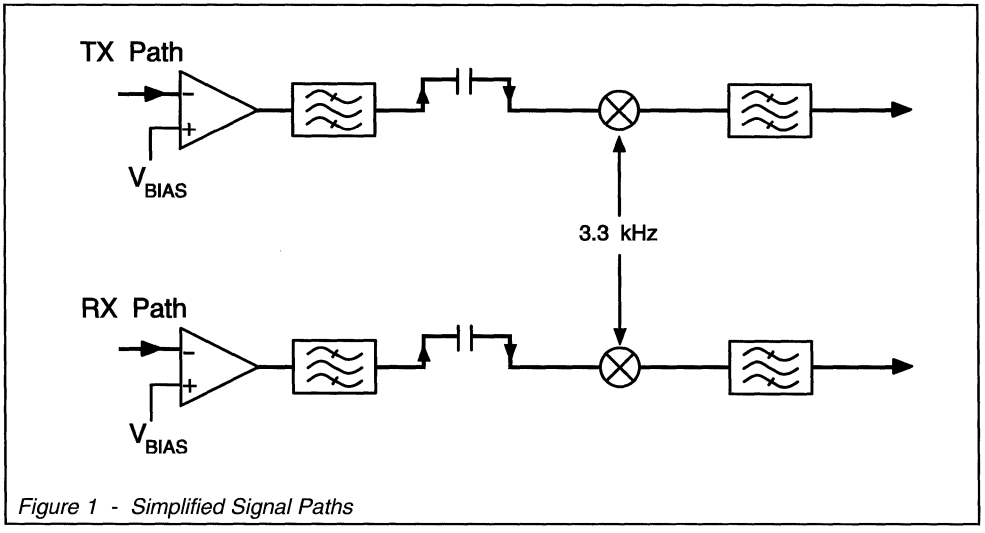


Figure 1 - Simplified Signal Paths

* Electronics Communications Privacy Act (Title 18 US Code 2510 et seq.).

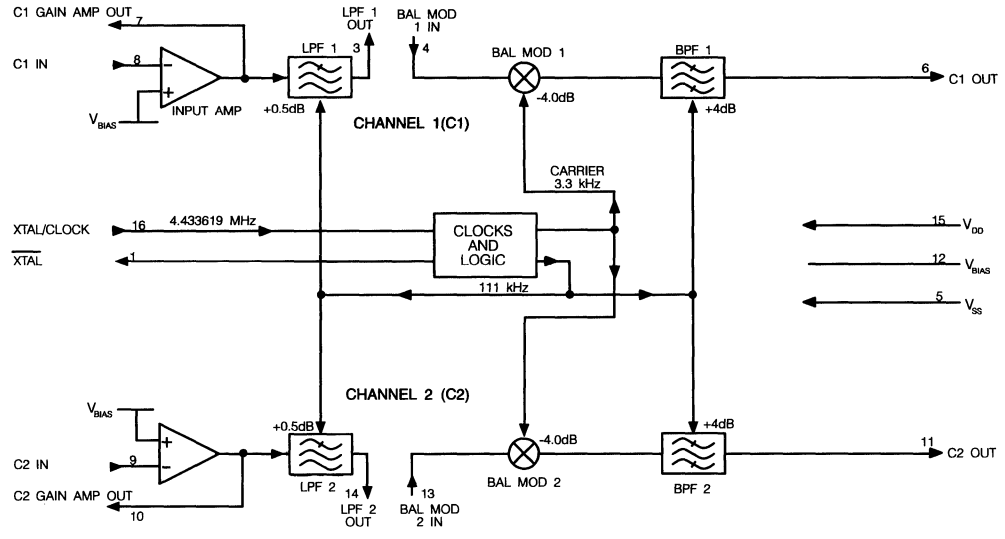
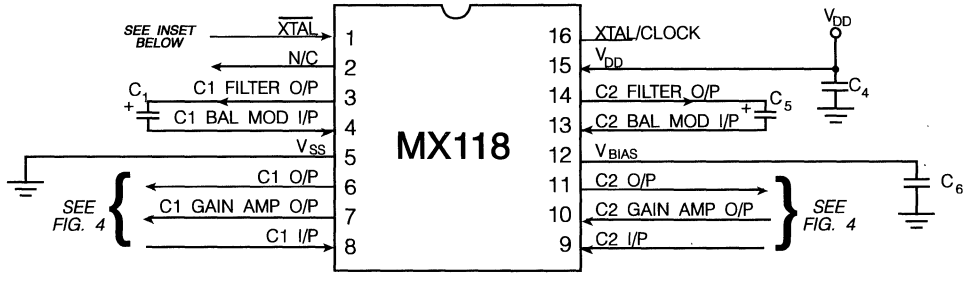
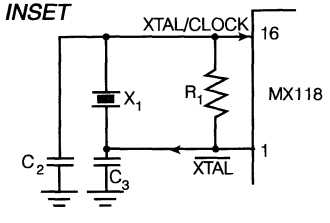


Figure 2 - Block Diagram





Component	Value
R1	1.0MΩ
C1	1.0µF
C2	33.0pF
C3	47.0pF
C4	0.47µF
C5	1.0µF
C6	1.0µF
X1	4.433619 MHz

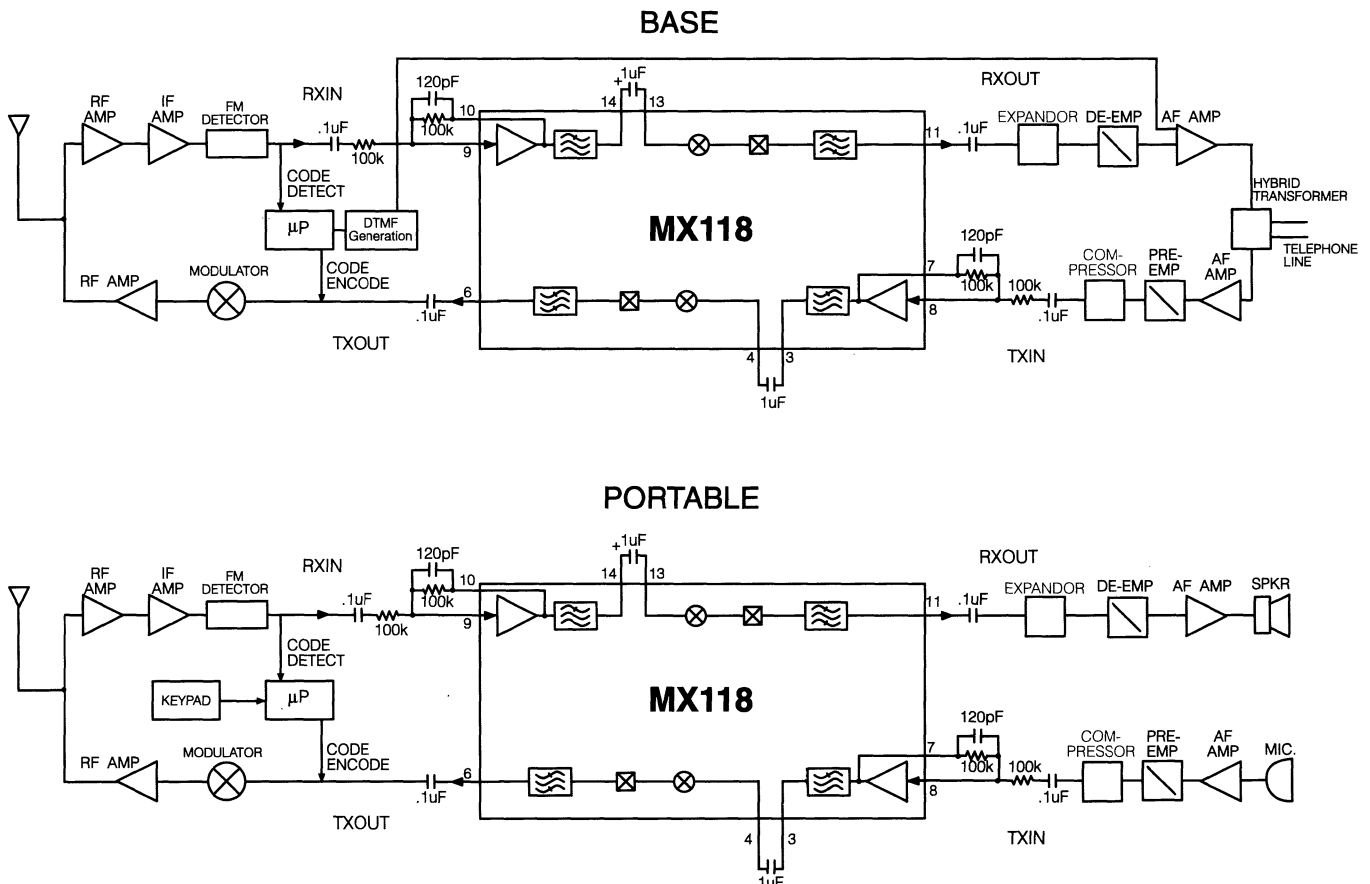
Tolerances: R = ±10%, C = ±20%

Notes: *1. Xtal circuitry shown is in accordance with MX-COM's Application Note on Crystal Oscillators (see Appendix).*

Figure 3 - Recommended External Components

Pin Function Chart

Pin	Function
1	**$\overline{\text{Xtal}}$:** This is the output of the clock oscillator inverter.
2	No Connection.
3	**C1 Filter Output:** This is the output of the channel 1 input filter. It should be coupled to pin 4 (C1 Balanced Modulator Input) by a 1.0 µF cap. See Figure 3.
4	**C1 Balanced Modulator Input:** This is the input to the channel 1 balanced modulator. Internally biased at $V_{DD}/2$, it should be coupled to pin 3 (C1 Filter Output) by capacitor C_2.
5	**V_{SS}:** Negative supply (GND).
6	**C1 Output:** This is the analog output of channel 1. It is internally biased at $V_{DD}/2$.
7	**C1 Gain Amp Output:** This is the output pin of the channel 1 gain adjusting op-amp. See Figure 4 for test gain setting components.
8	**C1 Input:** This is the analog signal input to channel 1. This input is to a gain adjusting op-amp whose gain is set by internal components. See Figure 4.
9	**C2 Input:** This is the analog signal input to channel 2. This input is to a gain adjusting op-amp whose gain is set by internal components. See Figure 4.
10	**C2 Gain Amp Output:** This is the output pin of the channel 2 gain adjusting op-amp. See Figure 4 for test gain setting components.
11	**C2 Output:** This is the analog output of channel 2. It is internally biased at $V_{DD}/2$.
12	**V_{BIAS}:** This is the analog bias line at $V_{DD}/2$. It should be coupled to V_{SS} by a 1.0 µF or greater capacitor. See Figure 3.
13	**C2 Balanced Modulator Input:** This is the input to the channel 2 balanced modulator. Internally biased at $V_{DD}/2$, it should be coupled to pin 14 (C2 Filter Output) by capacitor C_7.
14	**C2 Filter Output:** This is the output of the channel 1 input filter. It should be coupled to pin 13 (C2 Balanced Modulator Input) by a 1.0 µF capacitor. See Figure 3.
15	**V_{DD}:** Positive supply of 3.0 V to 5.5 V.
16	**Xtal/Clock:** 4.433619 MHz or an externally derived clock is injected at this pin. (See Figure 3.)



Note: Components shown set a gain of 0dB.

Figure 4 - Block Diagram of the MX118 in a Typical Application (Cordless Phone)

Application Information

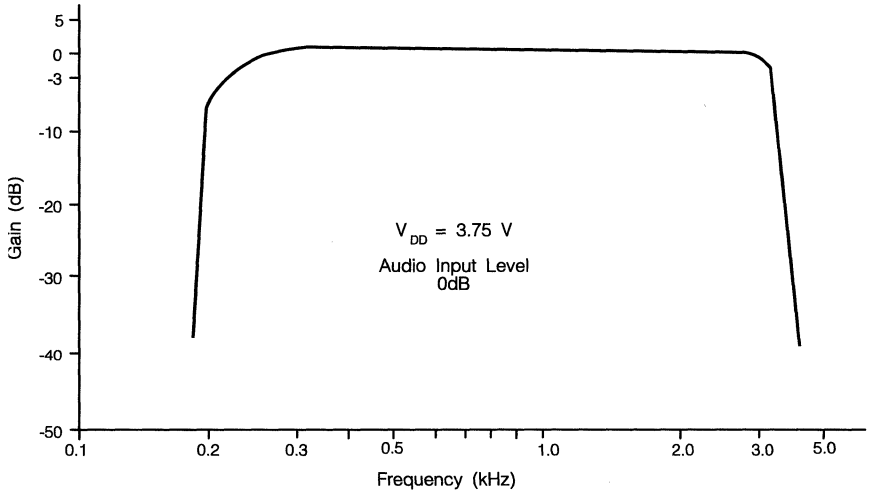


Figure 5 - Typical Audio Frequency Response of a Single Scrambled or De-scrambled Channel

System Gains

When calculating the external components for the operation of the MX118 the following should be considered:

a) The input Lowpass Filter has a typical gain of 0.5 dB.

b) The Balanced Modulator has a typical attenuation of 4.0 dB.

c) The Output Bandpass Filter has a typical gain of 4.5 dB.

5

How the Inverter Works

Carrier Frequency *minus* Input Voice Frequency *equals* Scrambled Voice Frequency.

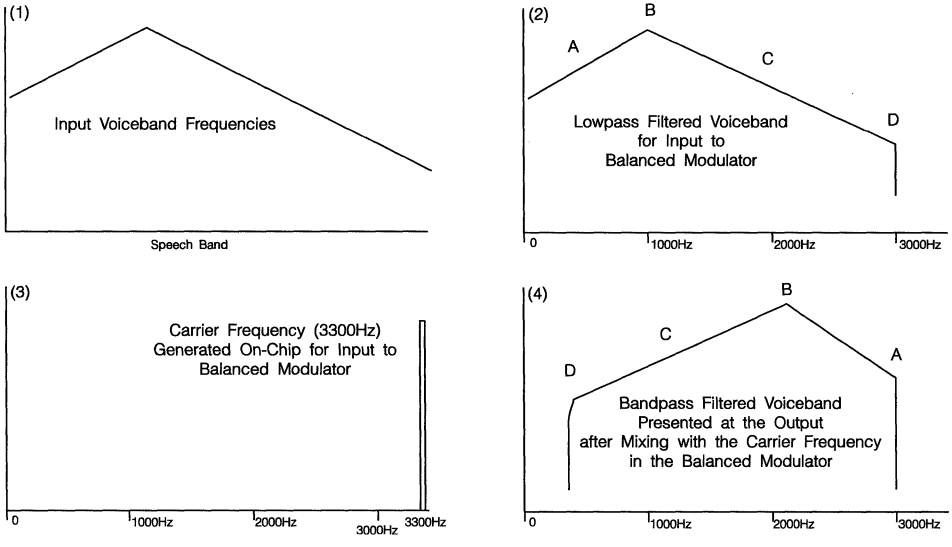


Figure 6 - An Explanation of the MX118 Scramble Operation

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (Ref. V_{SS} = 0V)	-0.3V to (V_{DD} + 0.3V)
Output sink/source current	
supply pins	±30mA
other pins	±20mA
Total Device Dissipation @ 25°C	800mW max.
Derating	10mW/°C
Operating Temperature	-10°C to +70°C
Storage Temperature	-40°C to +85°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 3.75 V

T_{AMB} = 25°C

Clock = 4.433619 MHz

Audio Level 0dB Ref. = 387 mVrms @ 1 kHz

Noise Bandwidth = 30kHz

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		3.0	3.75	5.5	V
Supply Current		-	3.0	4.0	mA
Input Impedance, Amplifiers		1.0	10.0	-	MΩ
Output Impedance					
C1, C2		-	200	-	Ω
Amplifiers		-	10.0	-	kΩ
Logic 1 Voltage		70% V_{DD}	-	-	
Logic 0 Voltage		-	-	30% V_{DD}	
On-Chip Xtal Oscillator					
R_{IN}		10.0	-	-	MΩ
R_{OUT}		-	10.0	-	kΩ
Inverter Gain		-	10.0	-	V/V
Gain/Bandwidth Product		-	10.0	-	MHz
Dynamic Values (Single Channel)					
Analog Signal Input Levels		-16.0	-	+3	dB
Carrier Breakthrough	1,2	-	-64.0	-	dB
Baseband Breakthrough	1,2	-	-50.0	-	dB
Carrier Frequency	5	-	3299	-	Hz
Analog Output Noise	3	-	-47.0	-42.0	dB
Upper Cut-off Frequency (-3dB)		3100	-	-	Hz
Passband Ripple (300 to 2950 Hz)		-1.5	-	+1.5	dB
Attenuation at 3.3 kHz		30.0	34.0	-	dB
Passband Gain		-2	0.5	+3	dB
Overall Modulated or De-Modulated Channel Response (Scrambler-Descrambler End-to-End)					
Passband Frequencies		300	-	2950	Hz
Passband Ripple		-3	-	+2	dB
Passband Gain @ 1 kHz	4	0	1.0	3.0	dB
Distortion	1	-	-	3.0	%
Low Frequency Attenuation @ 150 Hz		26	34	-	dB

NOTES

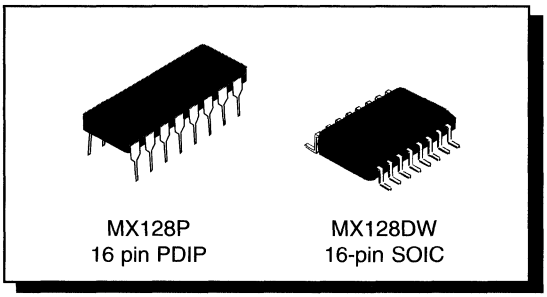
1. Measured with Input Level -3 dB.
2. Single Modulated Channel.
3. Short circuit input, any analog output, in 30 kHz bandwidth.
4. Op Amp gain 0 dB.
5. Accuracy dependent on Xtal/clock.

Advance Information

LOW COST CORDLESS TELEPHONE SCRAMBLER

Features

- **MX-COM MiXed Signal CMOS**
- **Full-Duplex Audio Processing**
- **On-Chip Filters**
- **High Baseband and Carrier Rejection**
- **Two Selectable Clock Inputs**
- **Excellent Audio Quality**
- **Low Voltage, 3-Cell Operation**
- **ECPA* Qualified Voice Protection**



MX128P
16 pin PDIP

MX128DW
16-pin SOIC

Applications

- **Battery Powered Portability**
- **Cordless Telephones & Wireless PBXs**

Description

The MX128 is a full-duplex frequency inversion scrambler designed to provide secure conversations for cordless telephone users. The RX and TX audio paths consist of the following:

1) A switched-capacitor balanced modulator with high baseband and carrier rejection.
2) A 3.3 kHz inversion carrier (injection tone).
3) A 3100 Hz lowpass filter.
4) Input op-amps with externally adjustable gain.

The MX128 uses mixed signal CMOS switched-capacitor filter technology and operates from a single supply in the range of 2.7 to 5.5 volts. The inversion carrier's frequency and filter switching clock are generated on-chip using an external 10.24 MHz or 3.58/3.6864 MHz crystal or clock input (selectable).

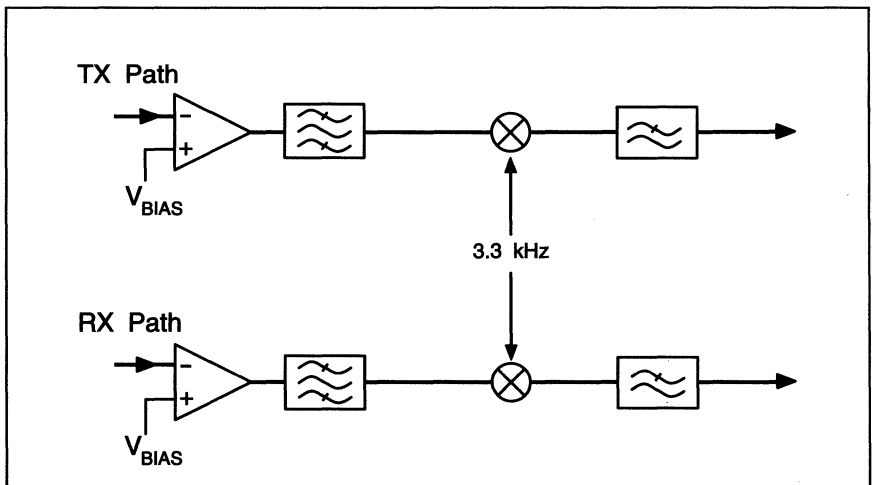


Figure 1 - Simplified Signal Paths

*Electronics Communications Privacy Act (Title 18, US Code 2510 et seq.).

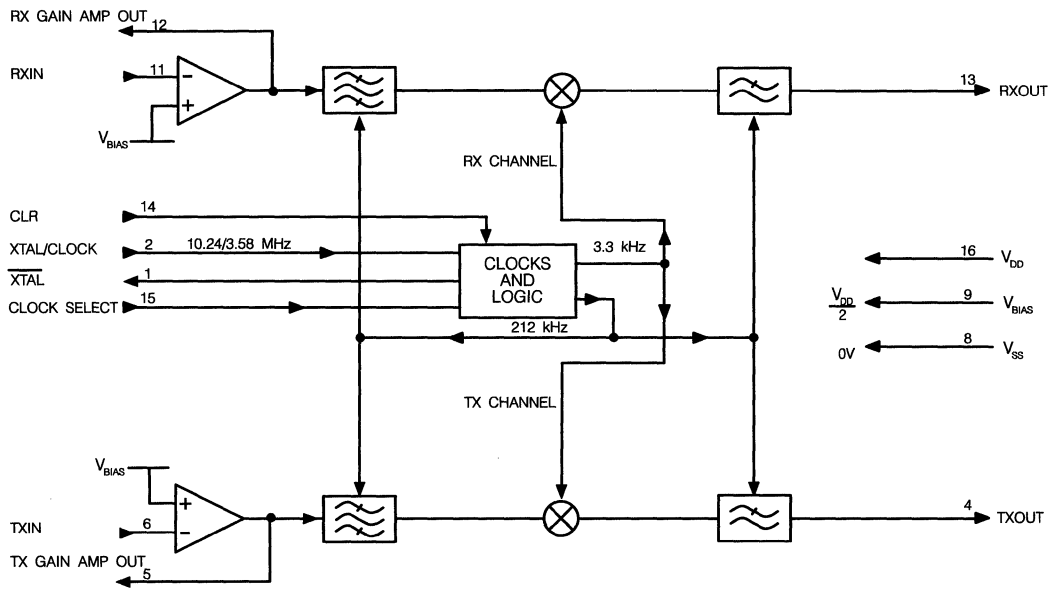
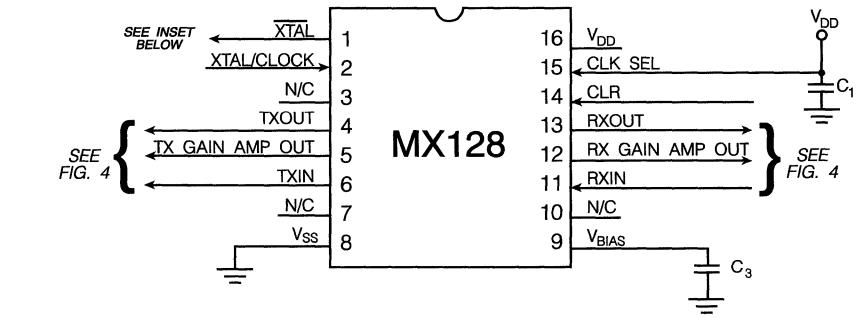
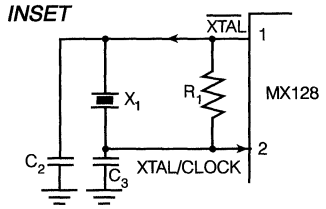


Figure 2 - Schematic Block Diagram





Component	Value	Value
R1	1.0MΩ	1.0MΩ
C1	0.47µF	0.47µF
C2	22.0pF	33.0pF
C3	22.0pF	47.0pF
X1	10.24 MHz	3.58/3.6864 MHz

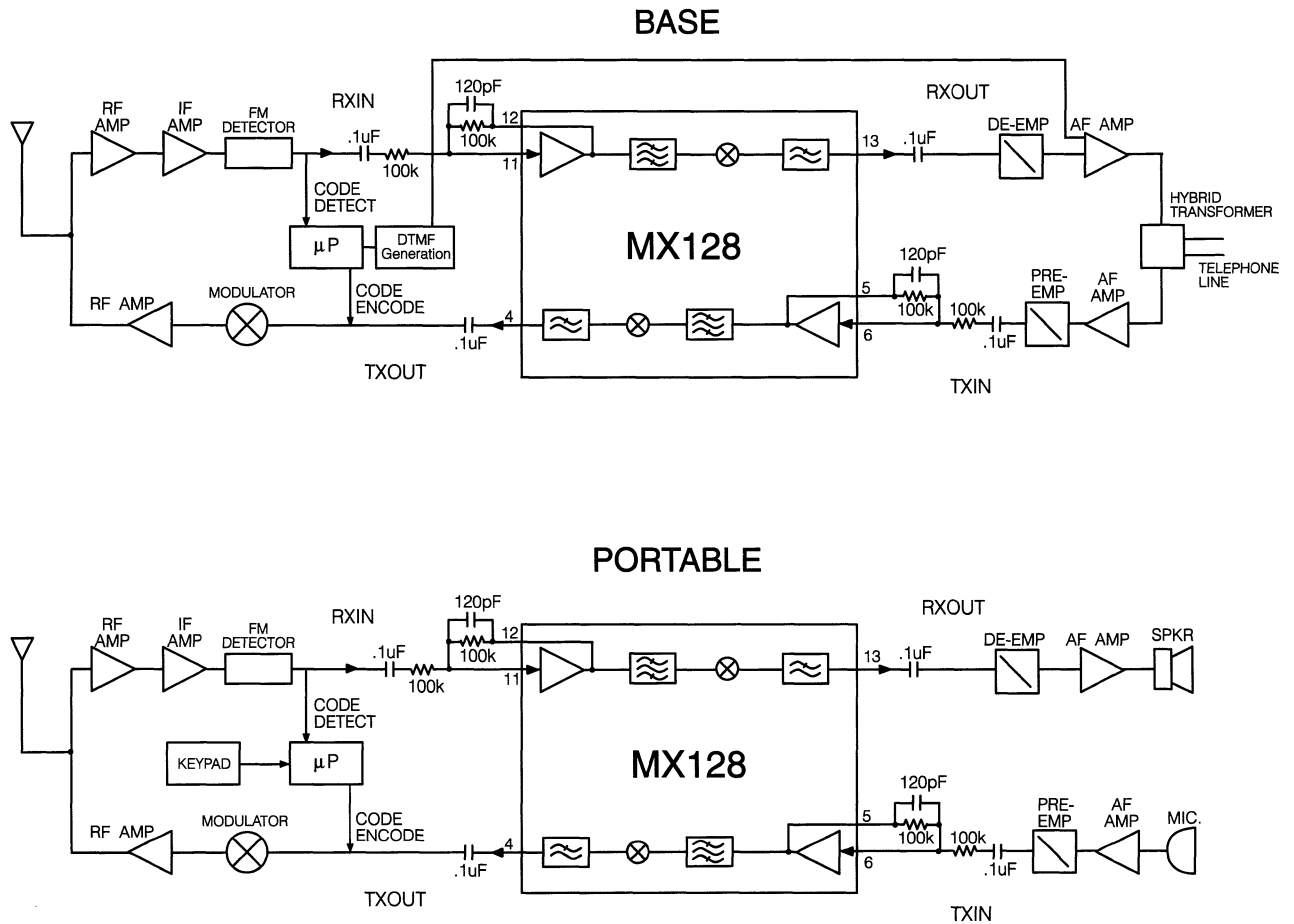
Tolerances: R = ±10%, C = ±20%

Note: *Xtal circuitry shown is in accordance with MX-COM's Application Note on Crystal Oscillators (see Applications Section).*

Figure 3 - Recommended External Components

Pin Function Chart

Pin	Function
1	**$\overline{\text{Xtal}}$:** This is the output of the clock oscillator inverter.
2	**Xtal/Clock:** 10.24 MHZ or 3.58/3.6864 MHz or an externally derived clock is injected at this pin. See Figure 3.
3	No connect.
4	**TX Output:** This is the analog output of the transmit channel. It is internally biased at $V_{DD}/2$.
5	**TX Gain Amp Output:** This is the output pin of the channel 1 gain adjusting op-amp. See Figure 4 for gain setting components.
6	**TX Input:** This is the analog signal input to channel 1. This input is to a gain adjusting op-amp whose gain is set by internal components. See Figure 4.
7	No connect.
8	**V_{SS}:** Negative supply (GND).
9	**V_{BIAS}:** This is the analog bias line at $V_{DD}/2$. It should be coupled to V_{SS} by a 1.0 µF or greater capacitor. See Figure 3.
10	No connect.
11	**RX Input:** This is the analog signal input to the receive channel. This input is to a gain adjusting op-amp whose gain is set by internal components. See Figure 4.
12	**RX Gain Amp Output:** This is the output pin of the receive channel gain adjusting op-amp. See Figure 4 for gain setting components.
13	**RX Output:** This is the analog output of the receive channel. It is internally biased at $V_{DD}/2$.
14	**CLR:** A logic 1 on this input selects the invert mode. A logic 0 selects the bypass mode.
15	**Clock Select:** Selects either 10.24 or 3.58/3.6864 MHz clock frequency. A logic "1" selects 10.24 MHz, and a logic "0" selects 3.58/3.6864 MHz. This input is internally pulled high.
16	**V_{DD}:** Positive supply of 2.7 V to 5.5 V.



Note: Components shown set a gain of 0dB.

Figure 4 - Block Diagram of a Typical Application of the MX128 (Cordless Phone)

Passband

Figure 5 shows the MX128 overall frequency response of high and low-pass filters followed by a notch centered at the carrier frequency.

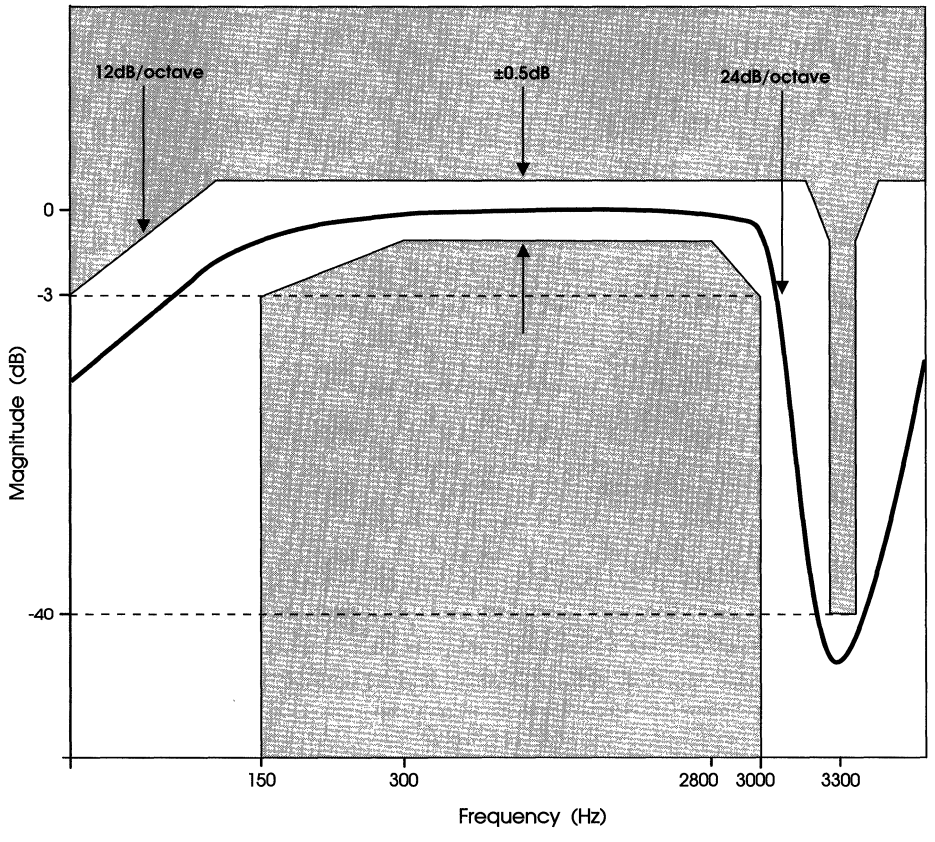


Figure 5 - Overall Frequency Response of the MX128

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (Ref. V_{SS} = 0V)	-0.3V to (V_{DD} + 0.3V)
Output sink/source current	
supply pins	±30mA
other pins	±20mA
Total Device Dissipation @ 25°C	800mW max.
Derating	10mW/°C
Operating Temperature	-10°C to +60°C
Storage Temperature	-40°C to +85°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 3.3 V

T_{AMB} = 25°C

Clock = 10.24 MHz

Audio Level 0dB Ref. = 250 mVrms @ 1 kHz

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		2.7	-	5.5	V
Supply Current		-	4.0	6.0	mA
Input Impedance					
Digital		100	-	-	kΩ
Amplifiers		1.0	10.0	-	MΩ
Output Impedance (RXOUT, TXOUT)		-	1.0	-	kΩ
Input Logic 1 Voltage		70%	-	-	V_{DD}
Input Logic 0 Voltage		-	-	30%	V_{DD}
Dynamic Values					
Analog Signal Input Levels		-16.0	-	3	dB
Unwanted Modulation Products	1,2	-	-40.0	-	dB
Carrier Breakthrough	1,2	-	-55.0	-	dB
Baseband Breakthrough	1,2	-	-40.0	-	dB
Carrier Frequency		-	3299	-	Hz
Analog Output Noise	3	-	1.59	-	mVrms
Cut-off Frequency (-3dB)		-	3000	-	Hz
Passband Ripple (300 to 3000 Hz)		-1.5	-	+1.5	dB
Filter Attenuation at 3.3 kHz		-	30.0	-	dB
Filter Attenuation at 3.6 kHz		-	45.0	-	dB
Passband Gain		-2.0	-	3.0	dB
Passband Frequency		300	-	3000	Hz
Low Frequency Roll-off (<200 Hz)		12	-	-	dB/oct.
Switched-Capacitor Filter Sampling Frequency		-	211.169	-	kHz
Overall Modulated or De-Modulated Channel Response					
Passband Frequencies		300	-	3000	Hz
Passband Ripple		-3	-	2.0	dB
Low Frequency Roll-off (<150 Hz)		12	-	-	dB/oct.
Passband Gain	4	-	0	-	dB
Distortion	1	-	-	2.5	%

SPECIFICATION NOTES

1. Measured with Input Level 0 dB.
2. Single Modulated Channel.
3. Short circuit input, any analog output, in 30 kHz bandwidth.
4. Op Amp gain 0 dB.

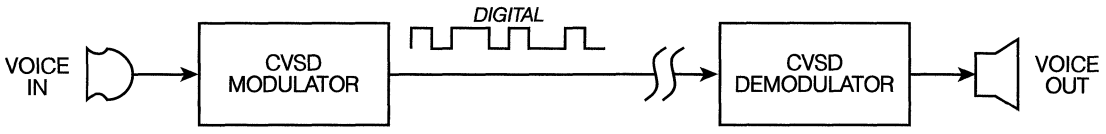
Section 6: CVSD CODECS

The following section contains specifications on MX•COM's CVSD Codecs. A brief description of CVSD begins on the following page. For an audio delay application, see the *Applications* section of this catalog.

Device	Description	Page	
MX109	Full Duplex CVSD Codec with Serial Control	p. 377	**NEW**
MX609	Full Duplex CVSD Codec with Companding	p. 384	
MX619/629	Delta Modulation Codec	p. 391	
MX709	Voice Storage and Retrieval (VSR) Codec w/ SRAM	p. 403	
MX802	VSR Codec with filter and DRAM Control	p. 420	
MX812	VSR Codec with DRAM Control	p. 434	

CVSD

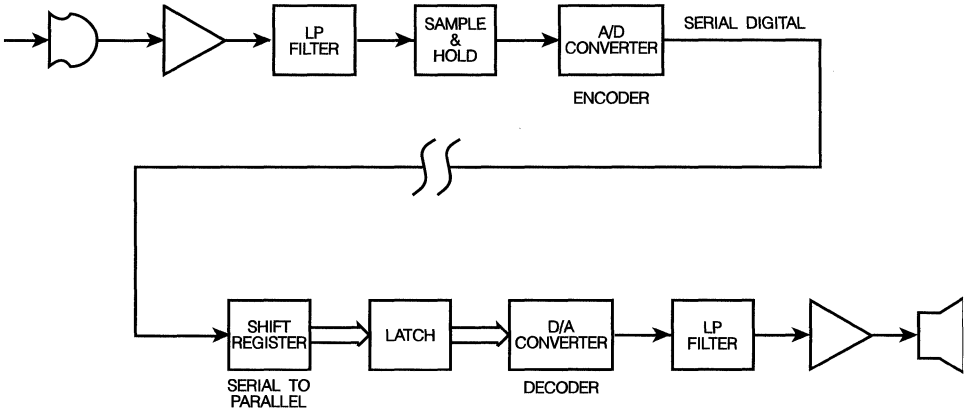
CVSD, or Continuously Variable Slope Delta Modulation, is a method by which a voice signal is converted into a digital data stream for transmission, and then changed back into the analog voice signal for reception. The digitization of voice signals is used in MX-COM's voice storage and retrieval devices. Advantages to digitization include making encryption easier and being able to multiplex many channels on a single wideband channel with inexpensive digital hardware. The reduction of channel crosstalk and noise interference are also results of digitization.



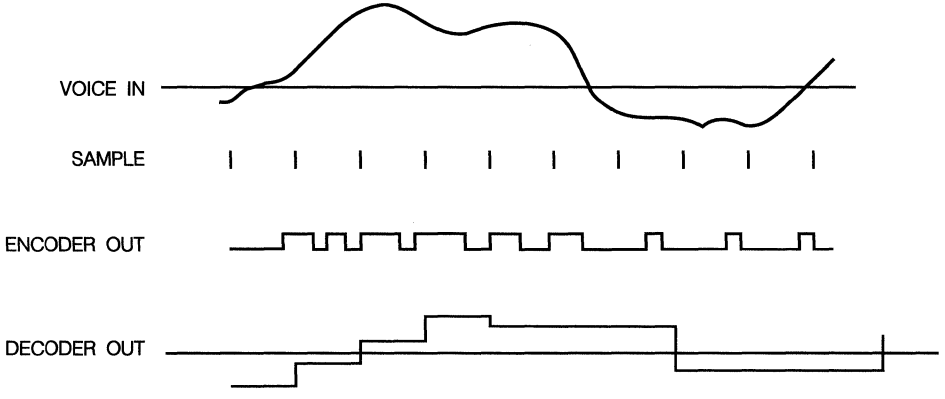
CVSD Compared to A to D and D to A PCM Transmission

CVSD and PCM (Pulse Code Modulation) can both be used to digitize voice. The methods of digitization are, however, quite different.

The PCM system is as follows:

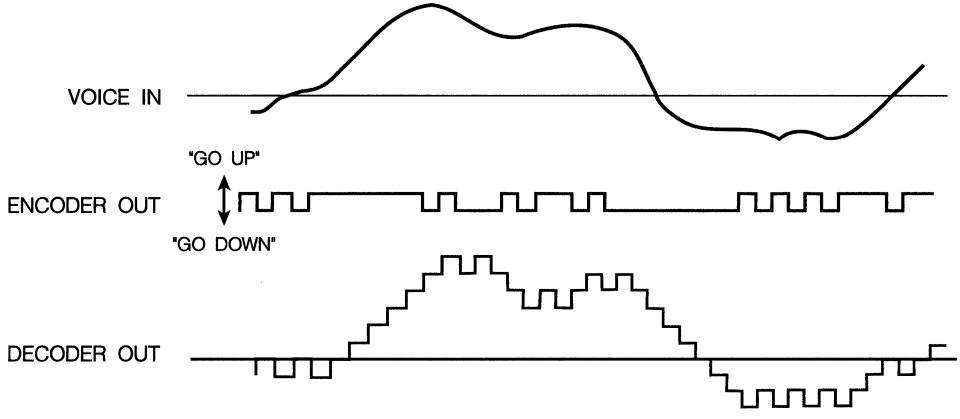


The following diagram shows a sampling of voice signal level using PCM.



Simple Delta Modulation

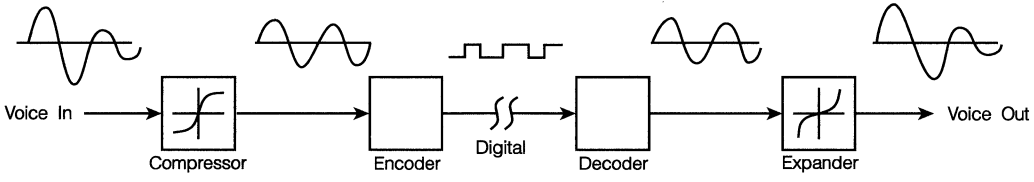
PCM can respond to quick level changes between samples, such as an analog signal which has been analog multiplexed. Delta modulation, however, takes advantage of the fact that voice signals do not change abruptly. There is usually only a small level change from one sample to the next. A good reproduction of the original voice waveform can therefore be obtained by transmitting directions that tell whether the output needs to go "up" or "down" in a given time interval. The following diagram shows a sampling of voice signal level using delta modulation.



CVSD

Simple delta modulation is most efficient when voice signals are close to full scale input to the modulator. However, severe distortion occurs when signal levels are very low.

To get around this problem, delta modulation can be combined with "companding" (compressing-expanding) of the voice input and output. Low level signals are given increased gain during modulation, then restored to their proper relative levels when demodulated. Because the CVSD companding scheme takes into account the characteristics of human voice, excellent quality voice transmissions are the end result.



Simplified Companding

CVSD allows lower data rates than PCM. More channels can therefore be multiplexed at the same bit rate. The companded PCM used in standard US telephone systems requires a sample rate of 8,000 samples per second and 8 bits per sample, which is the equivalent of 64kbits per second per channel. With CVSD, transmissions of equal or higher quality are obtained at 32kbits per second. Twice as many channels can be multiplexed on the same transmission medium. CVSD also suffers from less serious sound degradation in the presence of digital noise interference.

Digital CVSD is achieved with just one IC package which requires no initial or periodic adjustments. It includes features such as automatic noise squelch during quiet intervals and a signal that can be used for automatic gain control. CVSD is excellent for military communications, telephone systems and digital data transmission systems. It can also be used in commercial radio communications where a number of channels are multiplexed. Voice and data for storage and display can be intermixed, and security provisions added to prevent unauthorized interception.

Advance Information

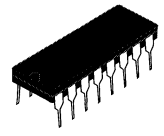
LOW VOLTAGE, FULL DUPLEX CVSD CODEC WITH SERIAL CONTROL

FEATURES

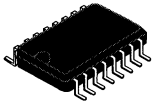
- **Single Chip Full Duplex CVSD CODEC**
- **On-chip Input & Output Filters**
- **On-chip Volume Control**
- **3V Operating Voltage**
- **Wide Frequency Reference using Ceramic Oscillator**
- **Low Power, Single Supply Analog CMOS**

APPLICATIONS

- **Digital Cordless Phones**
- **Digital PCN/PCS Systems**
- **Digital Delay Lines**
- **Digital Voice Storage**
- **Multiplexers, Switches & Phones**
- **Time Domain Scramblers**
- **Rechargeable Cell Operation**



MX109J (CDIP)
MX109P (PDIP)
16 pins



MX109DW
16 pin SOIC

Description

The MX109 is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in cordless telephones. The device is suitable for applications in delta multiplexers, switches and phones. Encoder input and decoder output switched capacitor filters are incorporated on-chip.

Sampling clock rates can be externally injected in the 8 to 64K bits/second range. The internal clocks are derived from an on-chip reference oscillator driven by an externally connected crystal or ceramic resonator. The sampling clock frequency is output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. When not enabled the encoder output remains in a high-impedance "tri-state" mode.

The MX109 is a low-power CMOS device. It is available in PDIP, CDIP and SOIC packages.

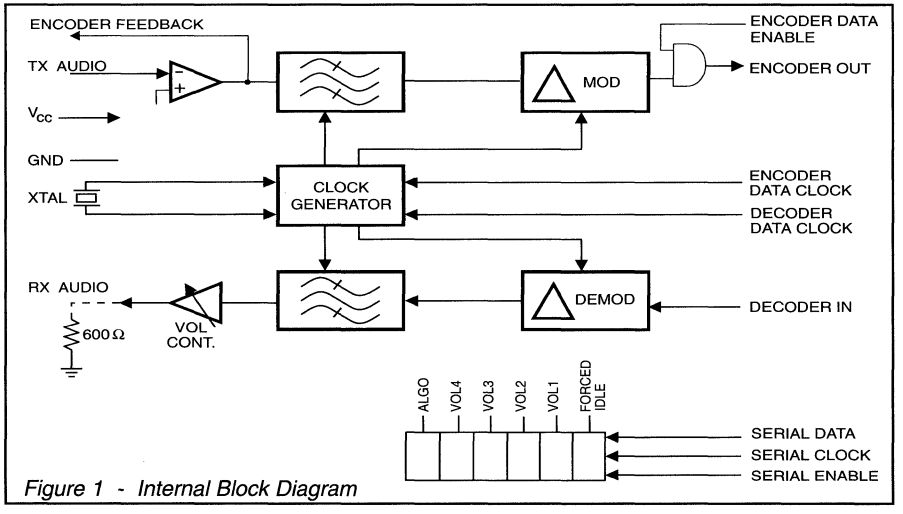


Figure 1 - Internal Block Diagram

PIN FUNCTION CHART

Pin	Function
1	**Xtal/Clock (I/P):** Input to the clock oscillator inverter. A 3.58 MHz Xtal input or externally derived clock is injected here. See Figure 3.
2	**$\overline{\text{Xtal}}$ (O/P):** The 3.58 MHz output of the clock oscillator inverter.
3	**Encoder Data Clock:** A logic I/O port. External encode clock input.
4	**Encoder Output:** The encoder digital output.
5	**Data Enable:** Data is made available at the encoder output pin by control of this input. Internal 1 MΩ pullup.
6	**Encoder Feedback:** The output of the encoder input amplifier / the input to the encoder filter.
7	**Encoder Input:** The analog signal input. Internally biased at $V_{DD}/2$, this input requires an external coupling capacitor. The source impedance should be less than 100Ω. Output channel noise levels will improve with an even lower source impedance. See Figure 3.
8	**V_{SS}:** Negative Supply
9	**Bias Out:** Normally at $V_{DD}/2$ bias.
10	**Decoder Output:** The recovered analog signal is output at this pin. It is the buffered output of a bandpass filter and requires external components.
11	**Decoder Input:** The received digital signal input. Internal 1 MΩ pullup.
12	**Decoder Data Clock:** A logic I/O port. External decode clock input.
13	**Serial Clock:** This is the serial clock input.
14	**Serial Data:** This is the serial data input. Data is loaded in the following order: ALGO, VOL4, VOL3, VOL2, VOL1, FORCE IDLE.
15	**Serial I/O Enable:** A logic 1 applied to this input will enable serial programming.
16	**V_{DD}:** Positive Supply.

CODEC INTEGRATION

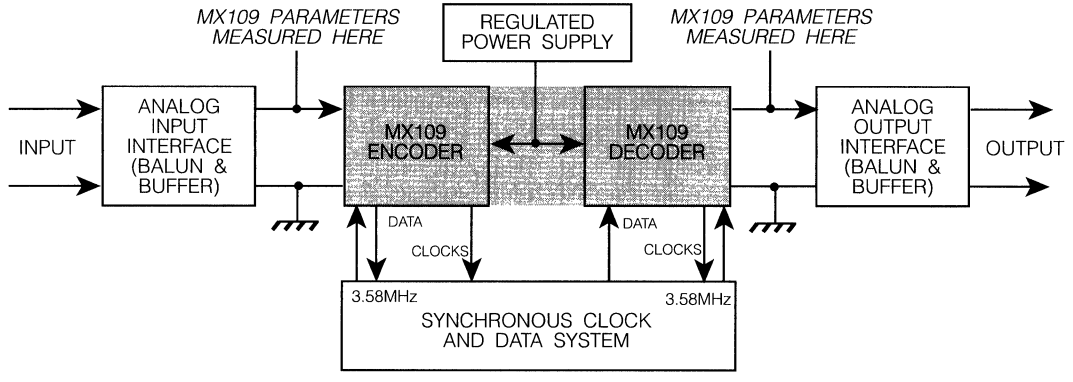
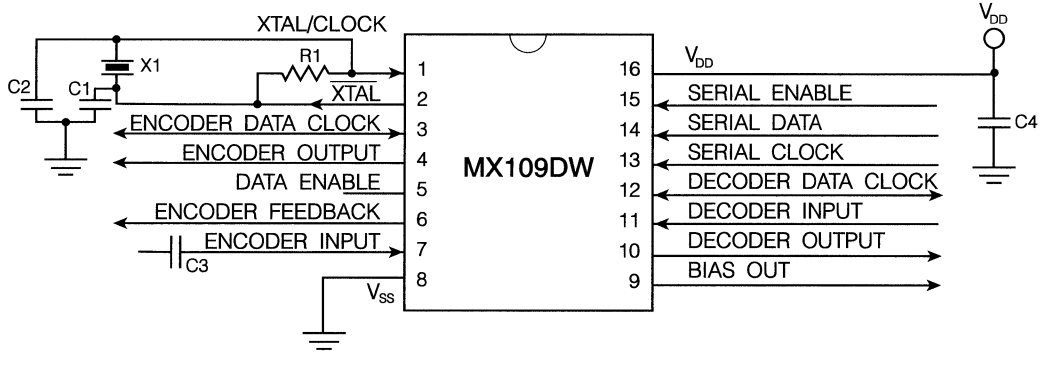


Figure 2 - System Configuration Showing the MX109



Component	Value	Note
R1	1M	Oscillator inverter bias resistor.
C1	33p	Xtal circuit load capacitor.
C2	27p	Xtal circuit load capacitor.
C3	1.0µ	Encoder input coupling capacitor. The drive source impedance to this input should be less than 100Ω. Output idle channel noise levels will improve with an even lower source impedance.
C4	0.47µ	V_{DD} decoupling capacitor.
X1	3.58MHz	Xtal circuitry shown is in accordance with MX-COM's Xtal Oscillator Application Note (see Appendix).

Tolerances: Resistors = 10%, Capacitors = 20%.

Figure 3 - Recommeded External Components

CODEC TIMING INFORMATION

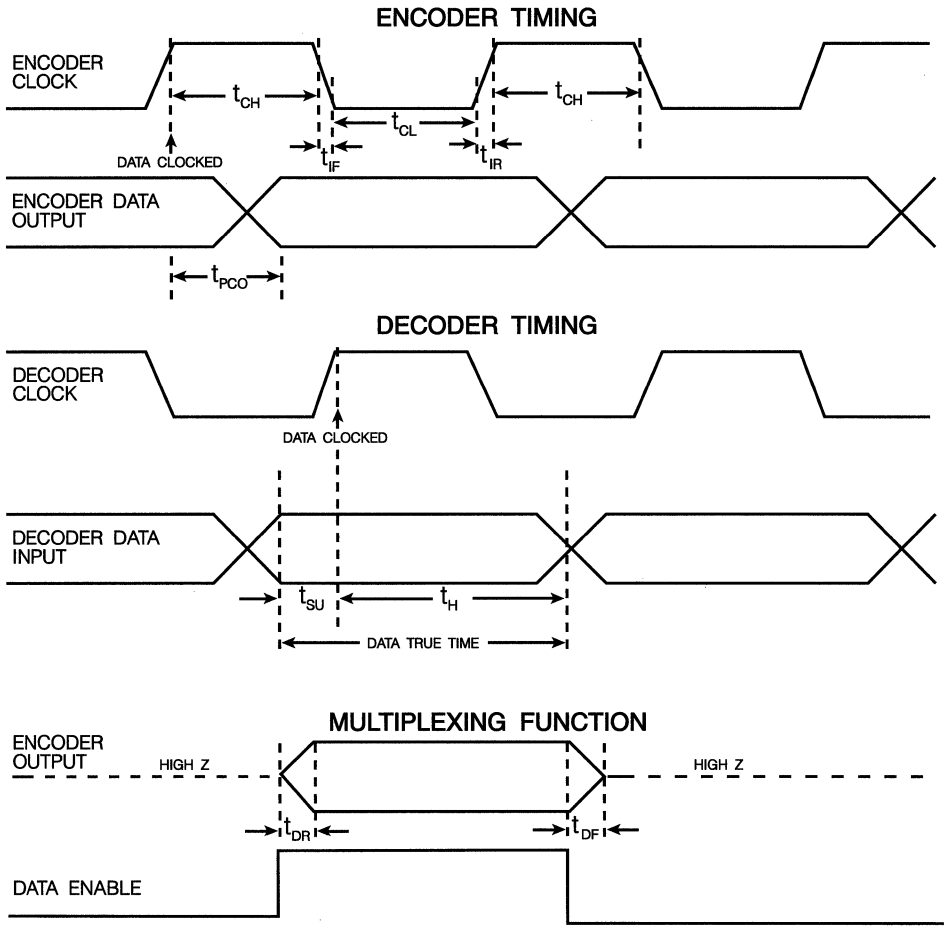


Figure 4 - Codec Timing

Abbreviation	Description	Time
t_{CH}	Clock pulse width (logic 1)	1.0µs min.
t_{CL}	Clock pulse width (logic 0)	1.0µs min.
t_{IR}	Clock rise time	100ns typ.
t_{IF}	Clock fall time	100ns typ.
t_{SU}	Data set-up time	450ns max.
t_H	Data hold time	600ns min.
$t_{SU} + t_H$	Data true time	1.5µs typ.
t_{PCO}	Clock to output delay time	750ns typ.
t_{DR}	Data rise time	100ns typ.
t_{DF}	Data fall time	100ns typ.
	Xtal input frequency	3.58MHz

CODEC PERFORMANCE

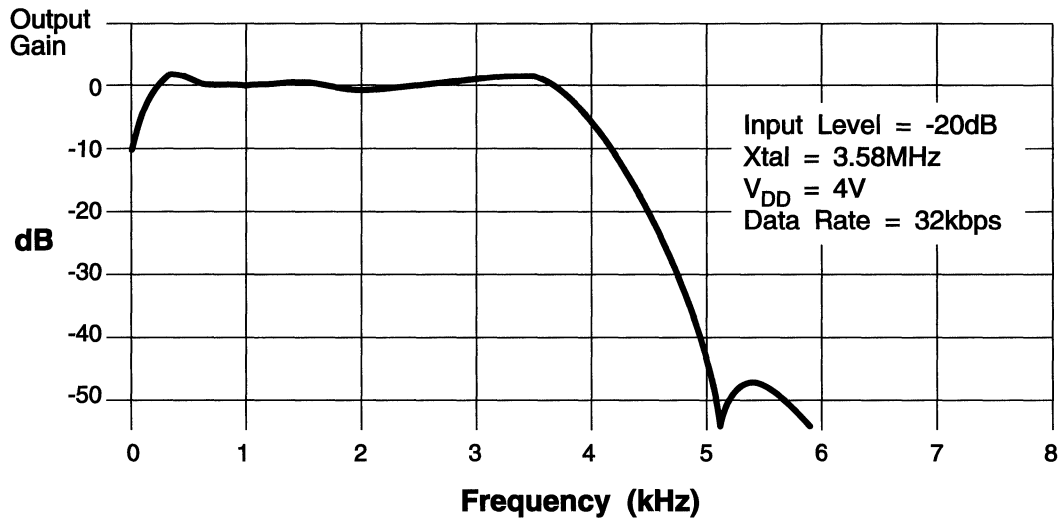


Figure 5 - Typical Codec Frequency Response

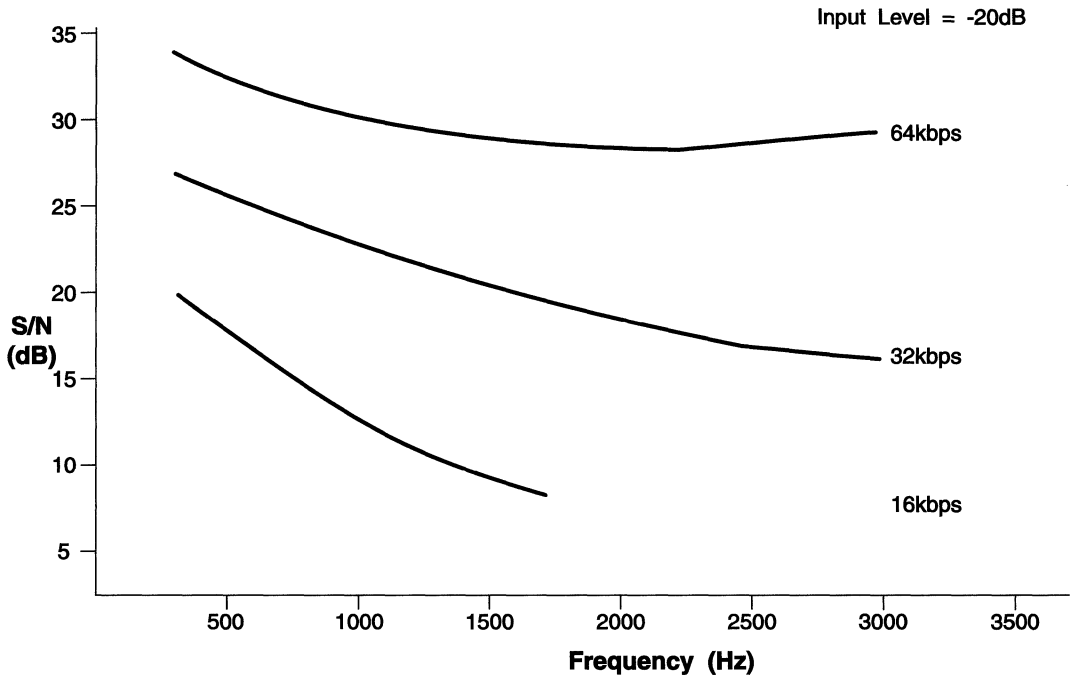


Figure 6 - Typical S/N Ratio with Input Frequency

6

SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0V
Input Voltage at any pin (ref V_{ss}=0V)	-0.3 to (V_{DD}+ 0.3V)
Sink/Source Current (Supply)	±30mA
(Other Pins)	±20mA
Total Device Dissipation (@ T_{amb}=25°C)	800mW max.
Derating	10 mW/°C
Operating Temperature	-30°C to +70°C
Storage Temperature	-40°C to +85°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 4.0V

Audio Test Frequency = 820Hz

T_{AMB} = 25°C

Sample Clock Rate = 32 kbps

Xtal/Clock f_o = 3.58MHz

Audio level 0dB ref (0 dBmO) = 500mVrms

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage	1	2.7	-	5.5	V
Supply Current		-	3.5	-	mA
Input Logic "1"		70%V_{DD}	-	-	V
Input Logic "0"		-	-	30%V_{DD}	V
Output Logic "1"		80%V_{DD}	-	-	V
Output Logic "0"		-	-	20%V_{DD}	V
Digital Input Impedance					
Logic I/O Pins		-	10	-	MΩ
Logic Input Pins, Pullup Resistor	2	300	-	-	kΩ
Digital Output Impedance		-	4	-	kΩ
Analog Input Impedance		-	100	-	kΩ
Analog Output Impedance	6	-	200	-	Ω
Insertion Loss	2	-	0	-	dB
Dynamic Values	1				
Encoder:					
Analog Signal Input Levels	6	-30	-	+6	dB
Principal Integrator Frequency		-	275	-	Hz
Encoder Passband		-	3700	-	Hz
Compand Time Constant		-	4	-	ms
Decoder:					
Analog Signal Output Levels	6	-30	0	+6	dB
Decoder Passband	3	-	3700	-	Hz

Characteristics	See Note	Min.	Typ.	Max.	Unit
Encoder/Decoder (Full Codec):					
Passband		300	-	3400	Hz
Stopband		6	-	10	KHz
Stopband Attenuation		-	60	-	dB
Passband Gain		-	0	-	dB
Passband Ripple		-3	-	+3	dB
Output Noise (Input Short Circuit)		-	-60	-	dB
Group Delay Distortion	4				
(1000Hz-2600Hz)		-	-	450	µs
(600Hz-2800Hz)		-	-	750	µs
(500Hz-3000Hz)		-	-	1.5	ms
Xtal/Clock Frequency		3.0	3.58	4.0	MHz

NOTES:

1. Dynamic characteristics specified at 4V only.
2. All logic inputs except Encoder and Decoder Data Clocks.
3. With passband gain of ±1dB.
4. Group Delay Distortion for the full codec is relative to the delay with an 820Hz, -20dB signal at the encoder input.
5. Relative Timings are shown in Figure 4.
6. Recommended values.

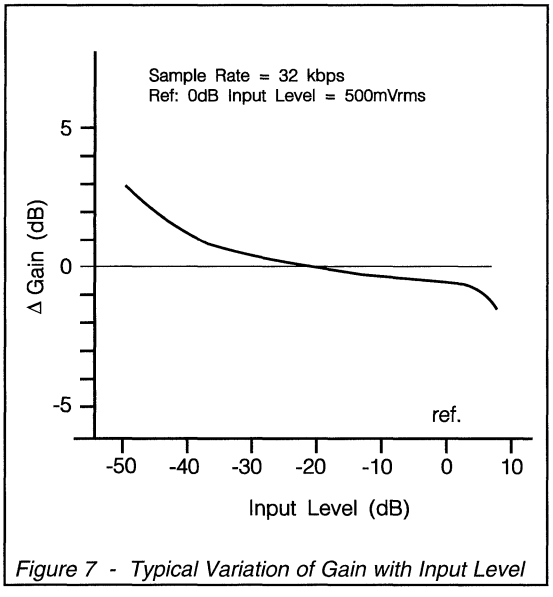


Figure 7 - Typical Variation of Gain with Input Level

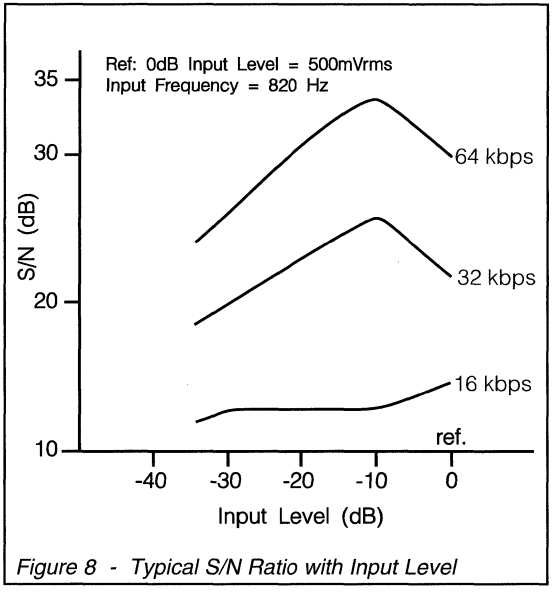


Figure 8 - Typical S/N Ratio with Input Level

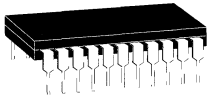
PCN/PCS DELTA MODULATION CODEC

FEATURES

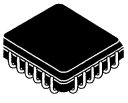
- **Single Chip Full Duplex CVSD CODEC**
- **On-chip Input & Output Filters**
- **Programmable Sampling Clocks**
- **3- or 4-bit Companding Algorithm**
- **Powersave Capabilities**
- **Low Power, Single 5V CMOS**

APPLICATIONS

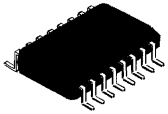
- **Digital PCN/PCS System**
- **Digital Cordless Phones**
- **Digital Delay Lines**
- **Digital Voice Storage**
- **Multiplexers, Switches & Phones**
- **Time Domain Scramblers**



MX609J (CDIP)
MX609P (PDIP)
22 pins



MX609LH
24 pin PLCC



MX609DW
16 pin SOIC

Description

The MX609 is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in cordless telephones. The device is suitable for applications in delta multiplexers, switches and phones. Encoder input and decoder output switched capacitor filters are incorporated on-chip.

Sampling clock rates can be programmed to 16, 32 or 64K bits/second from an internal clock generator or externally injected in the 8 to 64K bits/second range. The internal clocks are derived from an on-chip reference oscillator driven by an externally connected crystal. The sampling clock frequency is output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. When not enabled the encoder output remains in a high-impedance "tri-state" mode.

Companding circuits may be operated with an externally selectable 3- or 4-bit algorithm. The device may be put in standby mode when Powersave is selected.

The MX609 is a low-power 5V CMOS device. It is available in PDIP, CDIP, PLCC and SOIC packages.

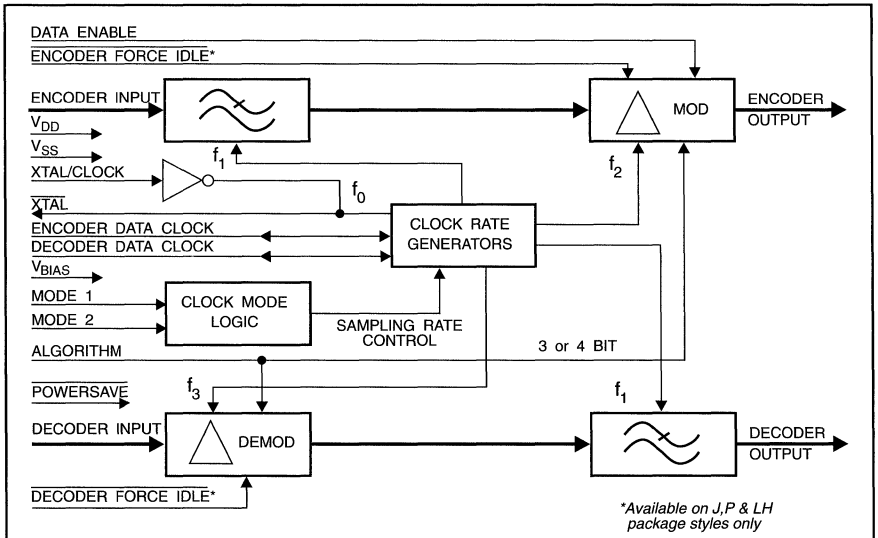


Figure 1 - Internal Block Diagram

PIN FUNCTION CHART

Pin			Function
J/P	LH	DW	
1	1	1	**Xtal/Clock (I/P):** Input to the clock oscillator inverter. A 1.024 MHz Xtal input or externally derived clock is injected here. See Clock Mode pins and Figure 3.
	2		N/C
2	3	2	**Xtal (O/P):** The 1.024 MHz output of the clock oscillator inverter.
3	4		N/C
4	5	3	**Encoder Data Clock:** A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependent upon clock mode 1,2 inputs and xtal frequency (see Clock Mode pins).
5	6	4	**Encoder Output:** The encoder digital output. This is a three-state output whose condition is set by the Data Enable and Powersave inputs, as shown below: Data Enable / Powersave / Encoder Output 1 / 1 / Enabled 0 / 1 / High Z (open circuit) 1 / 0 / V_{SS}
6	7	--	**$\overline{\text{Encoder Force Idle}}$:** When this pin is at a logical "0" the encoder is forced to an idle state and the encoder digital output is 0101, a perfect idle pattern. When this pin is a logical "1" the encoder encodes as normal. Internal 1MΩ pullup.
7	8	5	**Data Enable:** Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1 MΩ pullup.
8	9		N/C
9	10	6	**Bias:** Normally at $V_{DD}/2$ bias, this pin should be externally decoupled by capacitor C_4. Internally pulled to V_{SS} when "Powersave" is a logical "0".
10	11	7	**Encoder Input:** The analog signal input. Internally biased at $V_{DD}/2$, this input requires an external coupling capacitor. The source impedance should be less than 100Ω. Output channel noise levels will improve with an even lower source impedance. See Figure 3.
11	12	8	**V_{SS}:** Negative Supply
12	13		N/C
13	14	9	**Decoder Output:** The recovered analog signal is output at this pin. It is the buffered output of a lowpass filter and requires external components. During "Powersave" this output is open circuit.
14	15		N/C
15	16	10	**Powersave:** A logic "0" at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical "1", the codec operates normally. Internal 1 MΩ pullup.
	17		N/C
16	18	--	**$\overline{\text{Decoder Force Idle}}$:** A logic "0" at this pin gates a 0101... pattern internally to the decoder so that the Decoder Output goes to $V_{DD}/2$. When this pin is a logical "1" the decoder operates as normal. Internal 1MΩ pullup.
17	19	11	**Decoder Input:** The received digital signal input. Internal 1 MΩ pullup.
18	20	12	**Decoder Data Clock:** A logic I/O port. External decode clock input or internal data clock output, dependent upon clock mode 1,2 inputs. See Clock Mode pins.
19	21	13	**Algorithm:** A logic "1" at this pin sets this device for a 3-bit companding algorithm. A logical "0" sets a 4-bit companding algorithm. Internal 1 MΩ pullup.

Pin			Function			
J/P	LH	DW				
20	22	14	**Clock Mode 2:**	**Clock Mode 1**	**Clock Mode 2**	**Facility**
21	23	15	**Clock Mode 1:**	0	0	External Clocks
			Internal 1 MΩ	0	1	Internal,64kb/s=f÷16
			Pullups.	1	0	Internal,32kb/s=f÷32
				1	1	Internal,16kb/s=f÷64
			Clock rates refer to f = 1.024MHz Xtal/clock input. During internal operation the data clock frequencies are available at the ports for external circuit synchronization. Independent or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode.			
22	24	16	**V_{DD}:** Positive Supply. A single +5 volt power supply is required.			

CODEC INTEGRATION

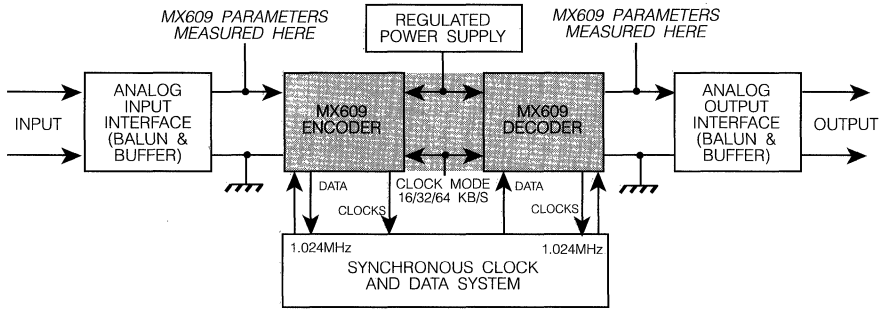
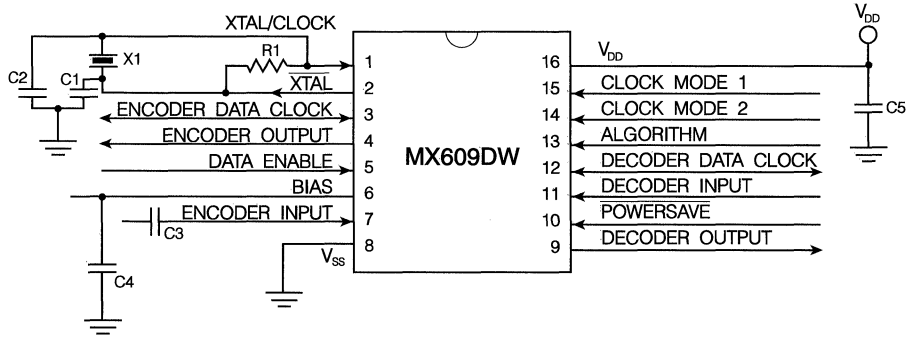


Figure 2 - System Configuration Showing the MX609



Component	Value	Note
R1	1M	Oscillator inverter bias resistor.
C1	33p	Xtal circuit load capacitor.
C2	68p	Xtal circuit load capacitor.
C3	1.0µ	Encoder input coupling capacitor. The drive source impedance to this input should be less than 100Ω. Output idle channel noise levels will improve with an even lower source impedance.
C4	1.0µ	Bias decoupling capacitor.
C5	1.0µ	V_{DD} decoupling capacitor.
X1	1.024MHz	A 1.024 MHz xtal/clock input will yield exactly 16/32/64 kb/s data clock rates. Xtal circuitry shown is in accordance with MX-COM's Xtal Oscillator Application Note (see Appendix).

Figure 3 - Recommeded External Components

Tolerances: Resistors = 10%, Capacitors = 20%.

CODEC TIMING INFORMATION

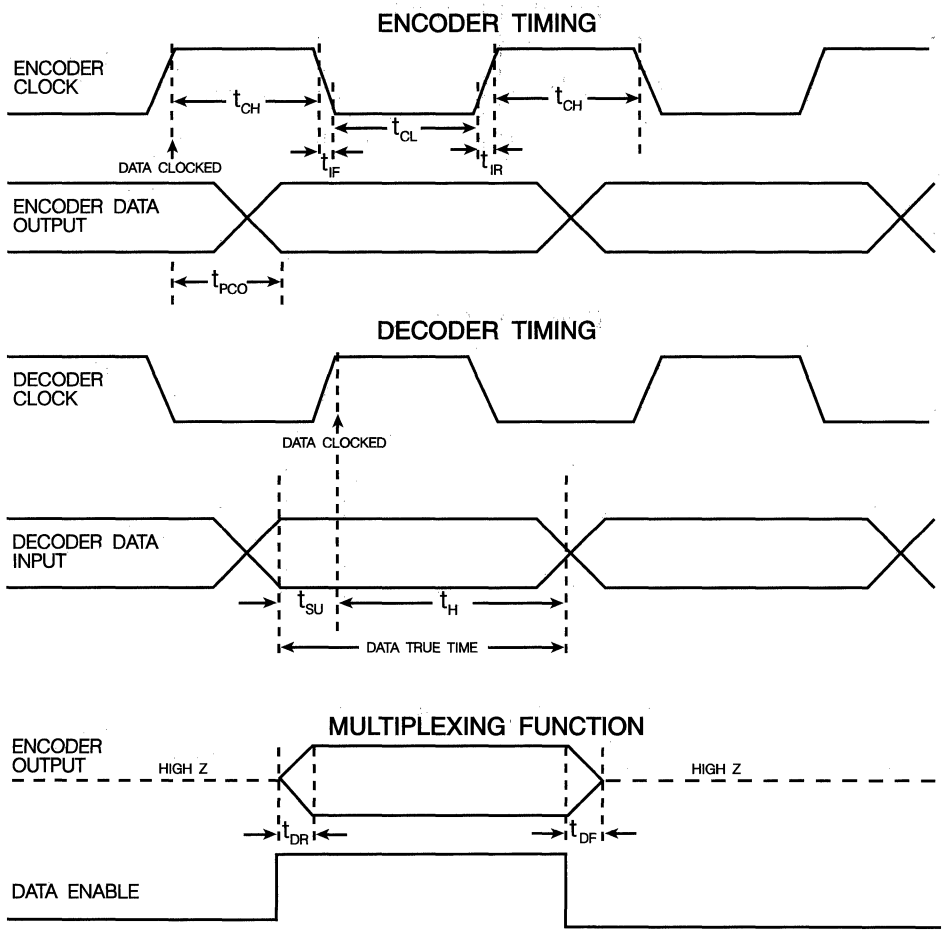


Figure 4 - Codec Timing

Abbreviation	Description	Time
t_{CH}	Clock 1 pulse width	1.0µs min.
t_{CL}	Clock 0 pulse width	1.0µs min.
t_{IR}	Clock rise time	100ns typ.
t_{IF}	Clock fall time	100ns typ.
t_{SU}	Data set-up time	450ns max.
t_H	Data hold time	600ns min.
$t_{SU} + t_H$	Data true time	1.5µs typ.
t_{PCO}	Clock to output delay time	750ns typ.
t_{DR}	Data rise time	100ns typ.
t_{DF}	Data fall time	100ns typ.
	Xtal input frequency	1.024MHz

CODEC PERFORMANCE

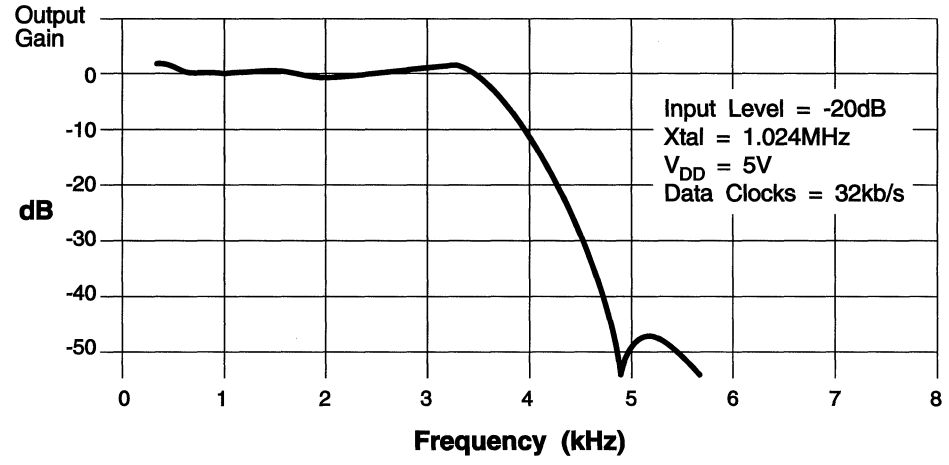


Figure 5 - Typical Codec Frequency Response

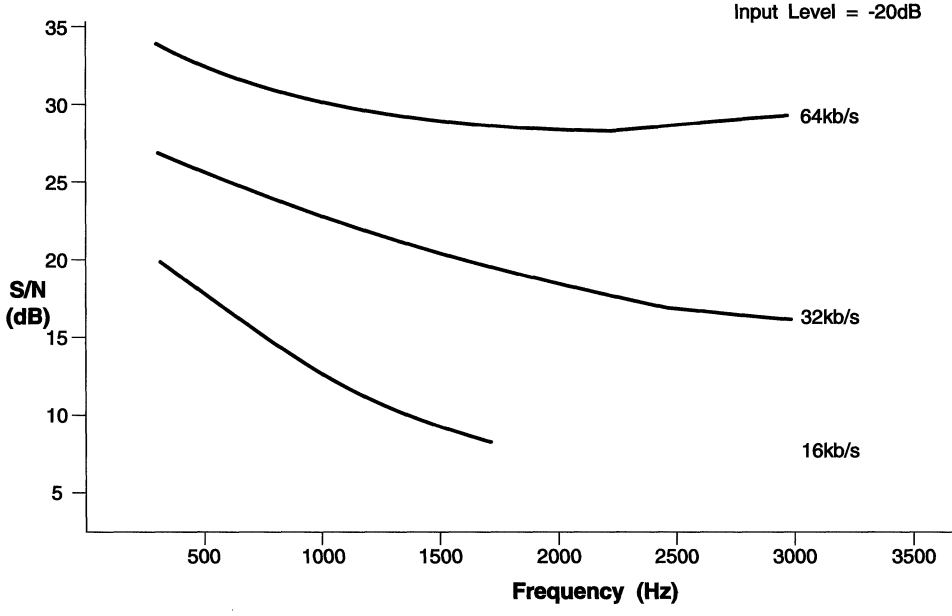


Figure 6 - Typical S/N Ratio with Input Frequency

SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0V
Input Voltage at any pin	
(ref V_{ss}=0V)	-0.3 to (V_{DD}+ 0.3V)
Sink/Source Current	
(Supply)	±30mA
(Other Pins)	±20mA
Total Device Dissipation	
(@ T_{amb}=25°C)	800mW max.
Derating	10 mW/°C
Operating Temperature	-30°C to +70°C
Storage Temperature	-40°C to +85°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

Audio Test Frequency = 820Hz

T_{AMB} = 25°C

Sample Clock Rate = 32 kb/sec

Xtal/Clock f_o = 1.024MHz

Audio level 0dB ref (0 dBm0) = 489mVrms

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage	1	4.5	5.0	5.5	V
Supply Current (Enabled)		-	3.5	-	mA
Supply Current (Powersave)		-	500	-	µA
Input Logic "1"		3.5	-	-	V
Input Logic "0"		-	-	1.5	V
Output Logic "1"		4.0	-	-	V
Output Logic "0"		-	-	1.0	
Digital Input Impedance					
Logic I/O Pins		-	10	-	MΩ
Logic Input Pins, Pullup Resistor	2	300	-	-	kΩ
Digital Output Impedance		-	4	-	kΩ
Analog Input Impedance		-	100	-	kΩ
Analog Output Impedance	6	-	800	-	Ω
Three State Output Leakage		-	±4	-	µA
Insertion Loss	2	-	0	-	dB
Dynamic Values	1				
Encoder:					
Analog Signal Input Levels	6	-30	-	+8	dB
Principal Integrator Frequency		-	275	-	Hz
Encoder Passband		-	3400	-	Hz
Compand Time Constant		-	4	-	ms
Decoder:					
Analog Signal Output Levels	6	-30	0	+8	dB
Decoder Passband	3	-	3400	-	Hz

Characteristics	See Note	Min.	Typ.	Max.	Unit
Encoder Decoder (Full Codec):					
Passband		300	-	3400	Hz
Stopband		6	-	10	KHz
Stopband Attenuation		-	60	-	dB
Passband Gain		-	0	-	dB
Passband Ripple		-3	-	+3	dB
Output Noise (Input Short Circuit)		-	-60	-	dB
Perfect Idle Channel Noise					
(Encode Forced)	7	-	-63	-	dB
Group Delay Distortion	4				
(1000Hz-2600Hz)		-	-	450	µs
(600Hz-2800Hz)		-	-	750	µs
(500Hz-3000Hz)		-	-	1.5	ms
Xtal/Clock Frequency		500	1024	1500	kHz

NOTES:

1. Dynamic characteristics specified at 5V only.
2. All logic inputs except Encoder and Decoder Data Clocks.
3. With passband gain of ±1dB.
4. Group Delay Distortion for the full codec is relative to the delay with an 820Hz, -20dB signal at the encoder input.
5. Relative Timings are shown in Figure 4.
6. Recommended values.
7. Forced Idle Encode/Decode not available on DW package.

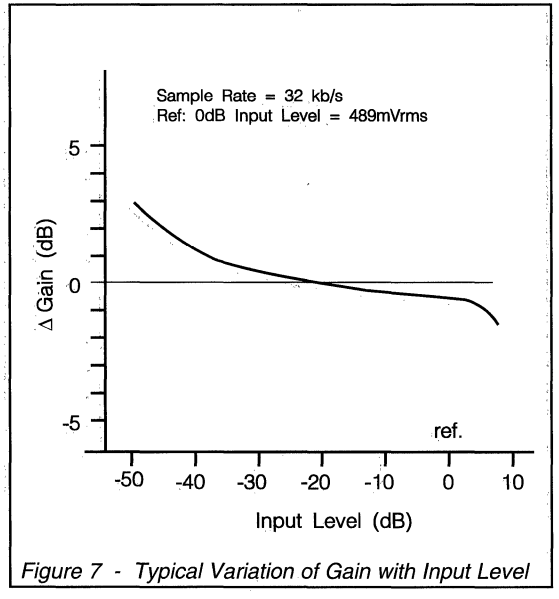


Figure 7 - Typical Variation of Gain with Input Level

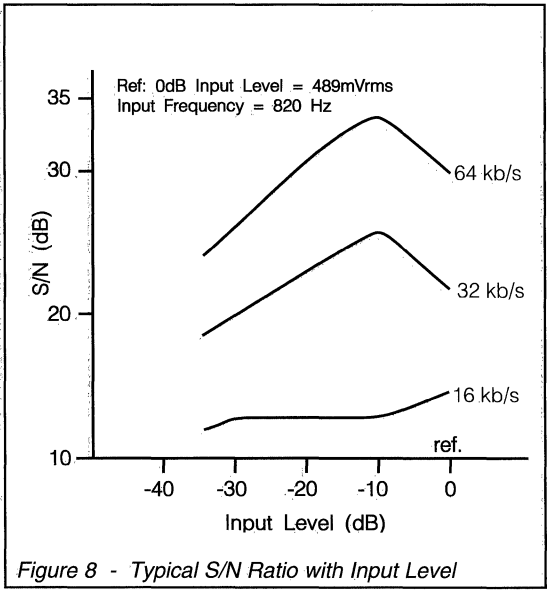


Figure 8 - Typical S/N Ratio with Input Level

MX-COM, INC.

MX619
MX629

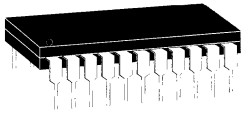
DELTA MODULATION CODEC

FEATURES

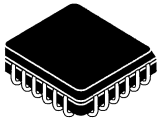
- **MX619 Meets EUROCOM D1-IA8**
- **MX629 Meets Mil-Std-188-113**
- **Single Chip Full Duplex CODEC**
- **On-chip Input & Output Filters**
- **Programmable Sampling Clocks**
- **3- or 4-bit Companding Algorithm**
- **Forced Idle & Powersave**

APPLICATIONS

- **Military Communications**
- **Multiplexers, Switches & Phones**



MX619J
MX629J
22-pin CDIP



MX619LH
MX629LH
24-lead PLCC

DESCRIPTION

The MX619 and MX629 are Continuously Variable Slope Delta Modulation (CVSD) Codecs designed for use in military communications systems. The device is suitable for applications in military Delta Multiplexers, switches and phones. The MX619 is designed to meet EUROCOM D1-IA8. The MX629 is designed to meet Mil-Std-188-113.

Encoder input and decoder output filters are incorporated on-chip. Sampling clock rates can be programmed to 16, 32 or 64K bits/second from an internal clock generator or externally injected in the 8 to 64K bits/second range. Sampling clock frequencies are output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. Encoder and Decoder forced idle capabilities are provided forcing a 10101010... pattern in encode and a $V_{DD}/2$ bias in decode. The companding circuits may be operated with an externally selectable 3- or 4-bit algorithm. The device may be put in standby mode by selecting Powersave. A reference 1.024MHz oscillator uses an external clock or crystal. The MX619 and MX629 are low-power 5V CMOS devices available in a 22-pin CDIP package or a 24-lead PLCC package.

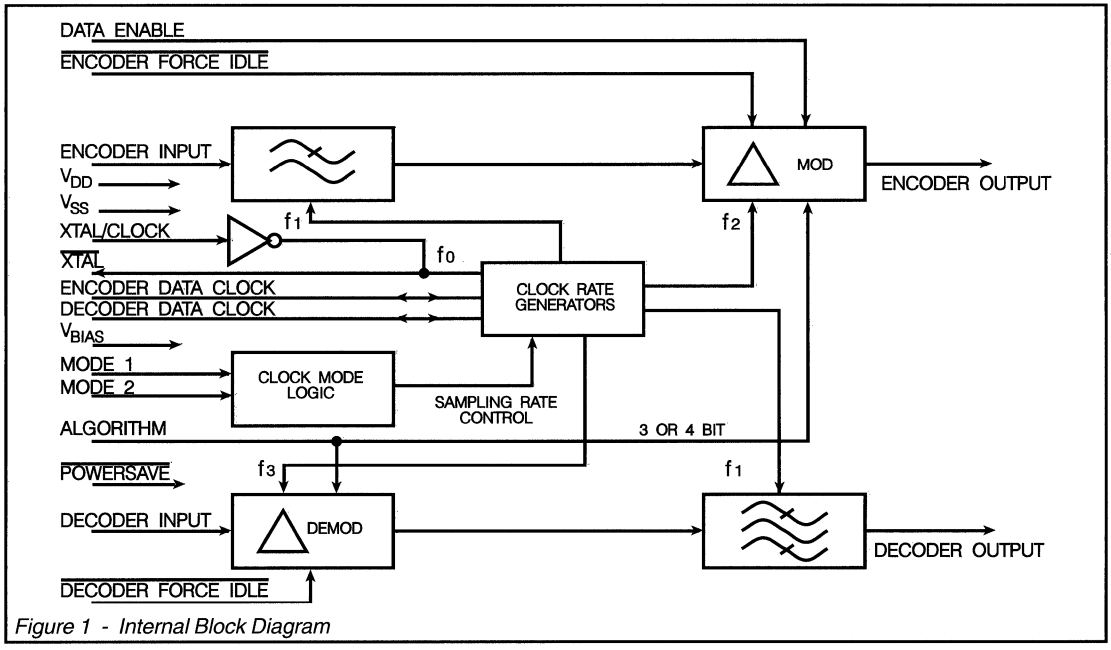


Figure 1 - Internal Block Diagram

PIN FUNCTION TABLE

Pin J	Pin LH	Function
1	1	Xtal/Clock (I/P): Input to the clock oscillator inverter. A 1.024 MHz Xtal input or externally derived clock is injected here. See Clock Mode pins and Figure 3.
	2	No Connection.
2	3	$\overline{\text{Xtal}}$ (O/P): The 1.024 MHz output of the clock oscillator inverter.
3	4	No Connection.
4	5	Encoder Data Clock: A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependent upon clock mode 1 and 2 inputs and xtal frequency (see Clock Mode pins).
5	6	Encoder Output: The encoder digital output. This is a three-state output whose condition is set by the Data Enable and Powersave inputs, as shown below:
6	7	$\overline{\text{Encoder Force Idle}}$: When this pin is a logical "0", the encoder is forced to an idle state and the encoder digital output is 0101..., a perfect idle pattern. When this pin is a logical "1", the encoder encodes as normal. This pin has an internal 1 MΩ pullup.
7	8	Data Enable: Data is made available at the encoder output pin by control of this input. See Encoder Output pin. This pin has an internal 1 MΩ pullup.
8	9	No Connection
9	10	Bias: Normally at $V_{DD}/2$ bias, this pin should be externally decoupled by capacitor C_4. Internally pulled to V_{SS} when "Powersave" is a logical "0".
10	11	Encoder Input: The analog signal input. Internally biased at $V_{DD}/2$, this input requires an external coupling capacitor. The source impedance should be less than 100Ω. Output channel noise levels will improve with an even lower source impedance. See Figure 3.
11	12	V_{SS}: Negative Supply.
12	13	No Connection.
13	14	Decoder Output: The recovered analog signal is output at this pin. It is the buffered output of a bandpass filter and requires external components. During "Powersave" this output is o/c.
14	15	No Connection.
15	16	$\overline{\text{Powersave}}$: A logical "0" at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical "1", the codec operates normally. This pin has an internal 1 MΩ pullup.

Data Enable	$\overline{\text{Powersave}}$	Encoder Output
1	1	Enabled
0	1	High Z (o/c)
1	0	V_{SS}

6

Pin J	Pin LH	Function
	17	No Connection
16	18	Decoder Force Idle: A logical "0" at this pin gates a 0101... pattern internally to the decoder so that the decoder output goes to $V_{DD}/2$. When this pin is at a logical "1", the decoder operates as normal. This pin has an internal 1 MΩ pullup.
17	19	Decoder Input: The received digital signal input. This pin has an internal 1 MΩ pullup.
18	20	Decoder Data Clock: A logic I/O port. External decode clock input or internal data clock output, dependent upon clock mode 1,2 inputs. See Clock Mode pins.
19	21	Algorithm: A logical "1" at this pin sets this device for a 3-bit companding algorithm. A logical "0" sets a 4-bit companding algorithm. This pin has an internal 1 MΩ pullup.
20 21	22 23	Clock Mode 2: Clock Mode 1: *Internal 1 MΩ Pullups.*

Clock Mode 1	Clock Mode 2	Facility
0	0	External Clocks
0	1	Internal, 64kb/s = f/16
1	0	Internal, 32kb/s = f/32
1	1	Internal, 16kb/s = f/64

Clock rates refer to f = 1.024MHz Xtal/clock input. During internal operation the data clock frequencies are available at the ports for external circuit synchronization. Independent or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode. Optimum performance will be achieved when the applied external clocks are synchronous with the master Xtal/clock, and a sub-multiple of 128kHz.

22	24	V_{DD}: Positive Supply. A single +5 volt power supply is required.

6

Application Recommendations

Due to the very low levels of signal idle channel noise specified for military applications, a noisy or badly regulated power supply could cause instability, putting the overall system performance out of specification. Adherence to the points listed below will assist in minimizing this problem.

(a) Care should be taken in the design and layout of the printed circuit board.

(b) All external components (as recommended in Figure 3) should be kept close to the package.

(c) Tracks should be kept short, particularly the Encoder Input capacitor and the V_{BIAS} capacitor.

(d) Xtal/clock tracks should be kept well away from analog inputs and outputs.

(e) Inputs and outputs should be screened whenever possible.

(f) A "ground plane" connected to V_{SS} will assist in eliminating external pick-up on the input and output pins.

(g) It is recommended that the power supply rails have less than 1mVrms of noise allowed.

(h) The source of impedance to the Encoder Input pin must be less than 100Ω; Output Idle channel noise levels will improve with even lower source impedances.

CODEC Integration

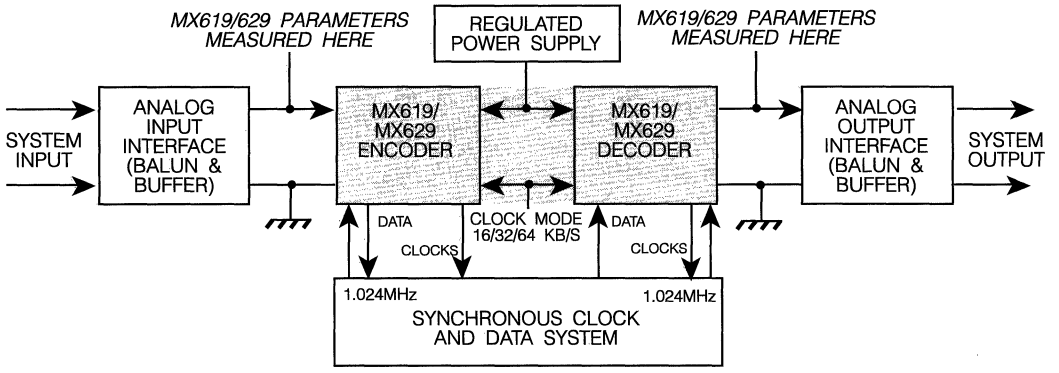
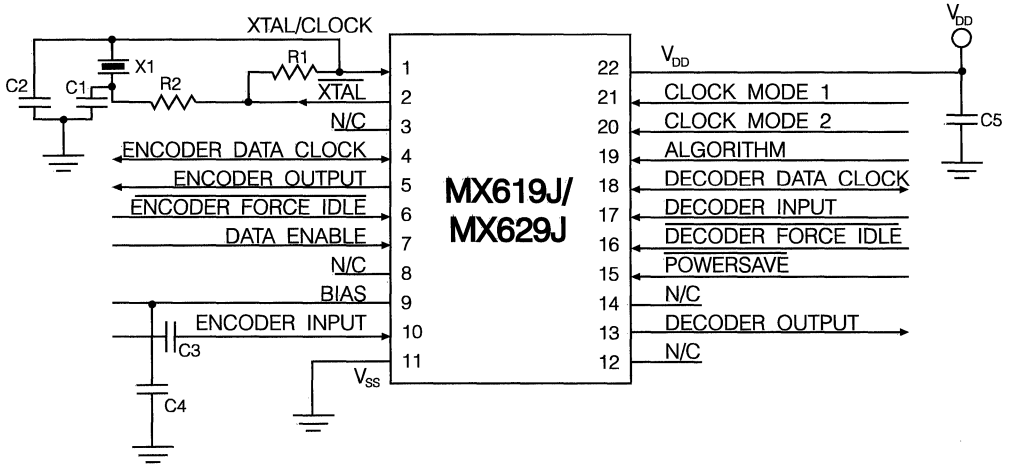


Figure 2 - System Configuration showing the MX619/MX629, which with the indicated interfacing will conform to the EUROCOM D1-IA8 or Mil-Std-188-113 specification, respectively.

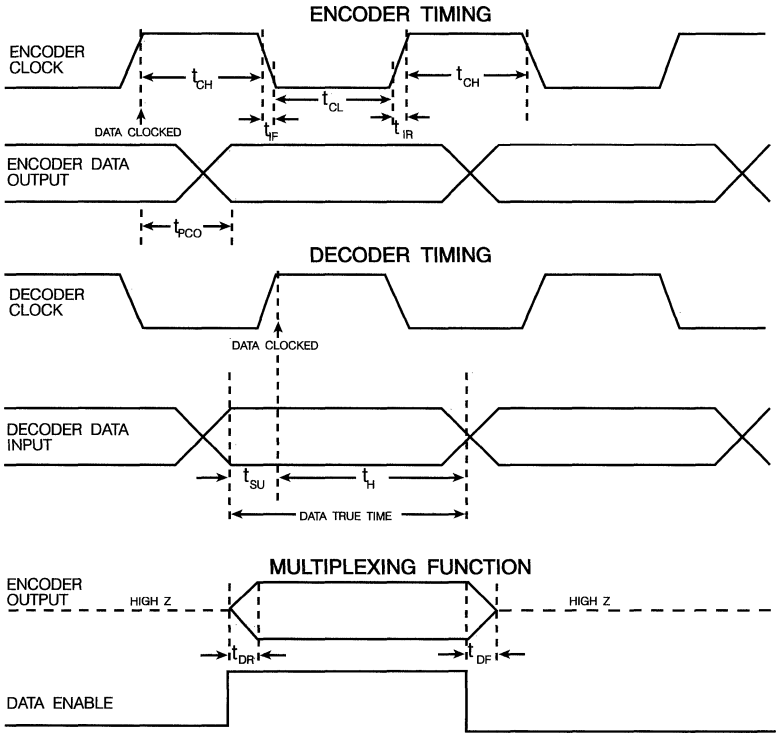


Component	Unit Value	Note
R_1	1M	Oscillator Inverter bias resistor.
R_2	Selectable	Xtal Drive limiting resistor.
C_1	33p	Xtal Circuit load capacitor.
C_2	33p	Xtal Circuit load capacitor.
C_3	1.0µ	Encoder Input coupling capacitor. The drive source impedance to this input should be less than 100Ω. Output Idle channel noise levels will improve with an even lower source impedance.
C_4	1.0µ	Bias decoupling capacitor.
C_5	1.0µ	V_{DD} decoupling capacitor.
X_1	1.024MHz	A 1.024 MHz Xtal/clock input will yield exactly 16/32/64 kb/s data clock rates.

Tolerance: Resistors ± 10%, Capacitors ± 20%

Figure 3 - Recommended External Components

CODEC Timing Information



TIMING

t_{CH}: Clock 1 Pulse Width 1.0µs min.

t_{CL}: Clock 0 Pulse Width 1.0µs min.

t_{IR}: Clock Rise Time 100ns typ.

t_{IF}: Clock Fall Time 100ns typ.

t_{SU}: Data Set-Up Time 450ns max.

t_H: Data Hold Time 600ns min.

$t_{SU} + t_H$: Data True Time

t_{PCO}: Clock to Output Delay Time. 750ns max.

t_{DR}: Data Rise Time 100ns typ.

t_{DF}: Data Fall Time 100ns typ.

XTAL Input Frequency: 1.024 MHz

Figure 4 - CODEC Timing Diagrams

6

Codec Performance (MX619)

Using the Bit Sequence Tests (a - g) at the Decoder Input pin in accordance with the Eurocom Specification D1-IA8, the decoder output is as shown in Table 1.

Test	Sample Rate	Bit Sequence at Decoder Input	MLA Duty Cycle	Typical Output Level
a.	16kbit/s	10110100100100101101	0	-41.5dBm0
	32kbit/s	10110110101010010010010010010101011101101	0	-42.0dBm0
b.	16kbit/s	11011001001001001101	0.05	-25.0dBm0
	32kbit/s	10110110101010010010001001001010111011011	0.05	-25.0dBm0
c.	16kbit/s	10110101000100101011	0.1	-19.0dBm0
	32kbit/s	11011011010100100010001001001010111011101	0.1	-18.5dBm0
d.	16kbit/s	11011001000010011011	0.2	-11.0dBm0
	32kbit/s	11011101100101000100001000100110101110111	0.2	-11.5dBm0
e.	16kbit/s	11011010000010010111	0.3	-6.5dBm0
	32kbit/s	11101110110010001000000100100110111011	0.3	-6.5dBm0
f.	16kbit/s	11011010000001001111	0.4	-3.0dBm0
	32kbit/s	11110111010100010000000010001010111011111	0.4	-3.0dBm0
g.	16kbit/s	11101010000000010111	0.5	0dBm0
	32kbit/s	11111011101000100000000001000101110111111	0.5	0dBm0

Table 1 - Bit Sequence Test Table

Digital to Analog Performance (MX629)

Using the bit sequence tests shown in Table 2 (below) at the Decoder Input pin, the analog signals measured at the Decoder Output pin are 800 Hz ± 10 Hz at the levels described.

Sample Rate	Bit Sequence at Decoder Input	"Run of Threes" (%)	Output Level (dBm0)
16 kbit/s	11011011010010010010	0	-29.2 ± 2
32 kbit/s	11011011010101001001001001001010101110110	0	-30.0 ± 2
16 kbit/s	11111011010000010010	30	0 ± 1
32 kbit/s	11111101101010100001000000100101010111110	30	0 ± 1
			at 800 Hz

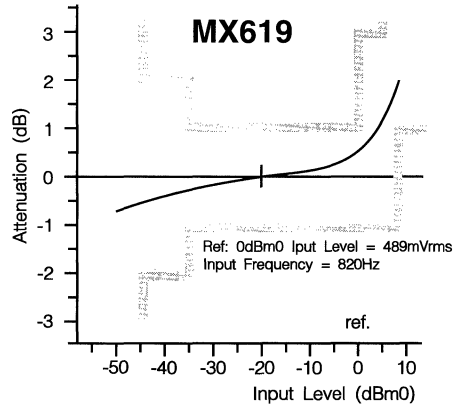
Table 2 - Bit Sequence Tests and Results (MX629)

MX619 Codec Performance...

relative to the EUROCOM D1-IA8 Specification

MX629 Codec Performance...

relative to the Mil-Std-188-113 Specification



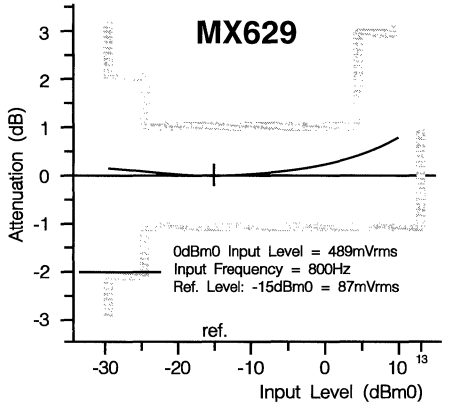
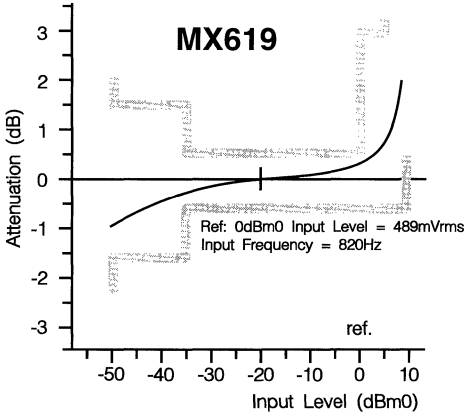


Figure 5 - Gain vs Input Level (16kbit/s)



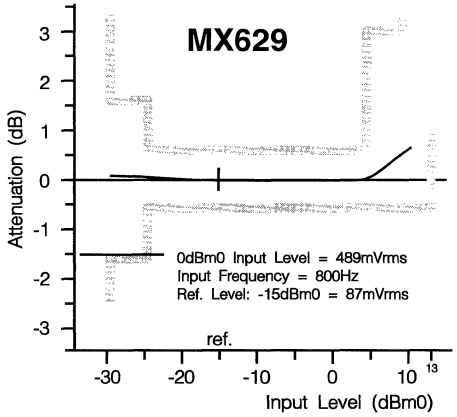
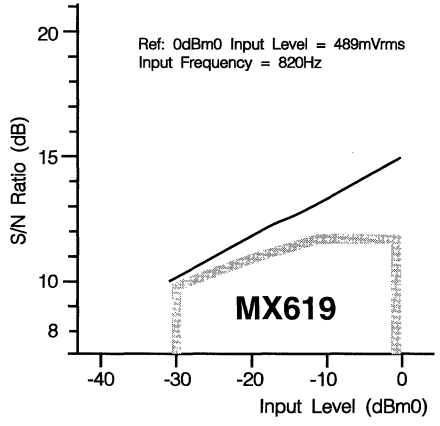


Figure 6 - Gain vs Input Level (32kbit/s)

Note: Spec of ±1dB sums a Mil-Std-188-113 spec of ±0.5dB with a test measurement limitation of ±0.5dB (with 0dB = 87mVrms, 0.5dB = 1.2mVrms).



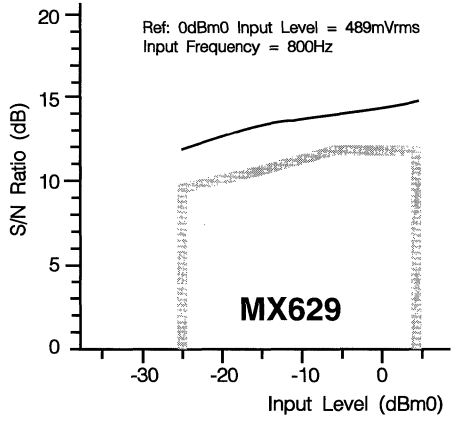


Figure 7 - S/N vs Input Level (16kbit/s)

MX619 Codec Performance...

relative to the EUROCOM D1-IA8 Specification

MX629 Codec Performance...

relative to the Mil-Std-188-113 Specification

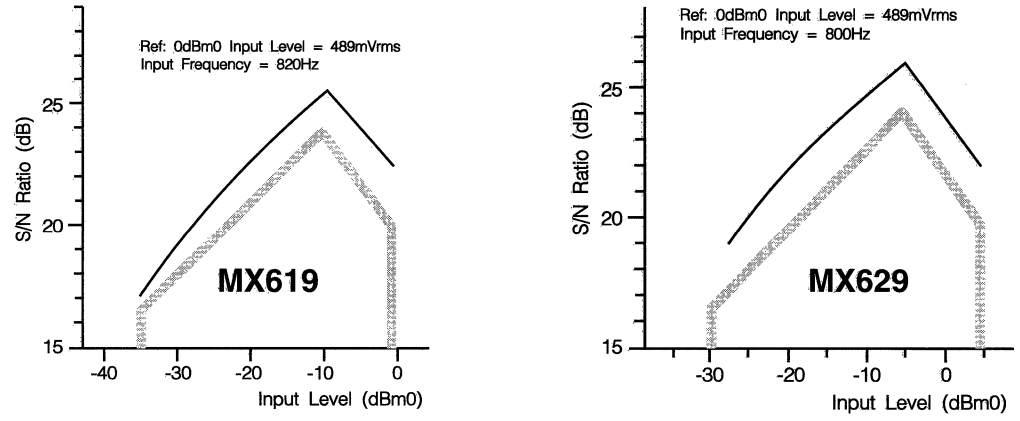


Figure 8 - S/N vs Input Level (32kbit/s)

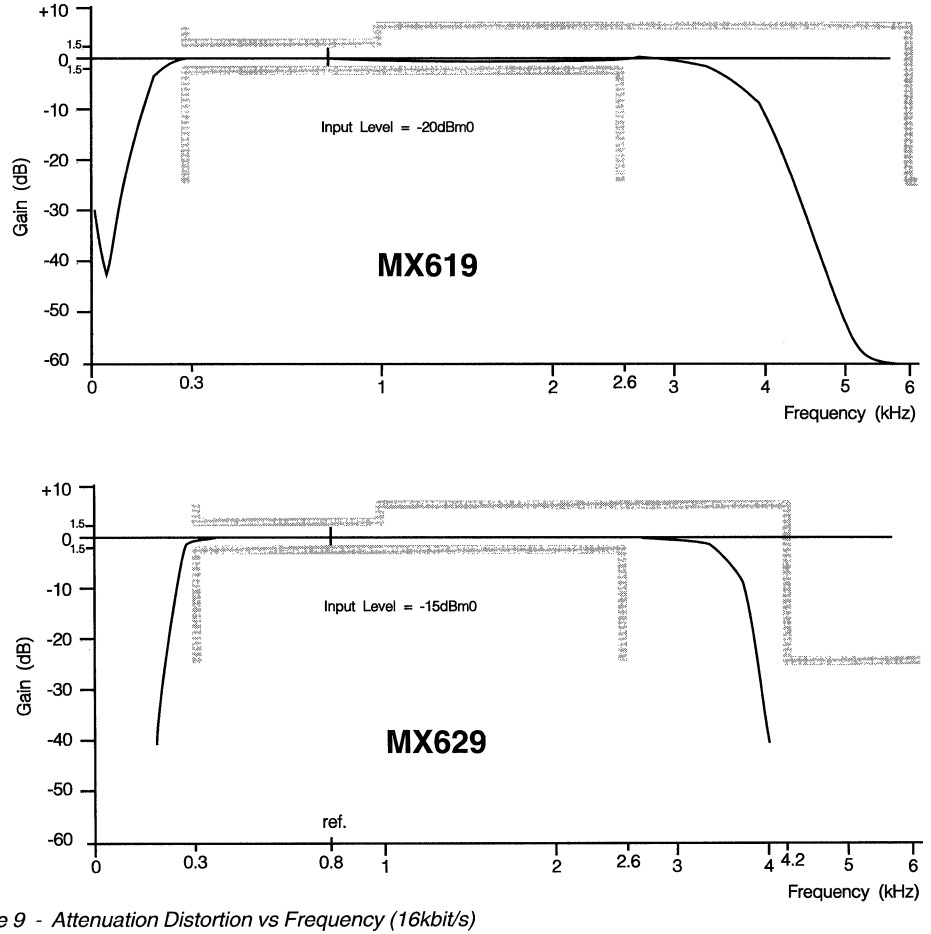


Figure 9 - Attenuation Distortion vs Frequency (16kbit/s)

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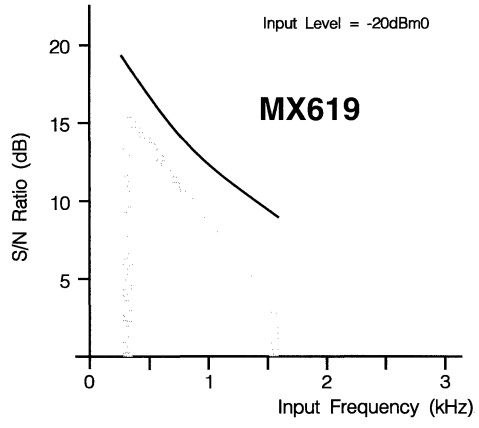
MX619 Codec Performance...

relative to the EUROCOM D1-IA8 Specification

MX629 Codec Performance...

relative to the Mil-Std-188-113 Specification



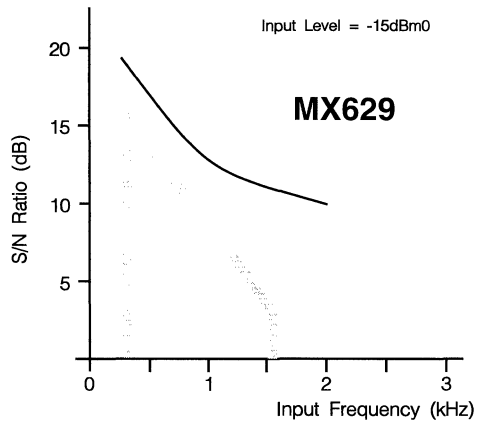
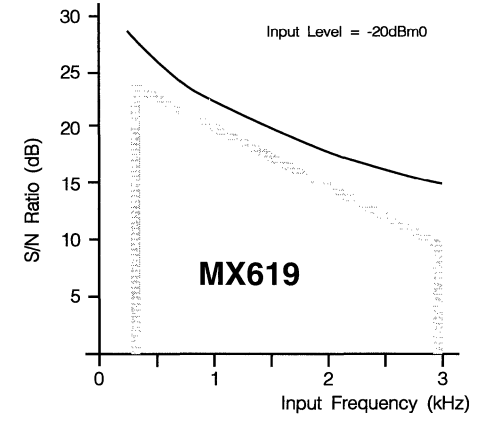


Figure 10 - S/N vs Input Frequency (16kbit/s)



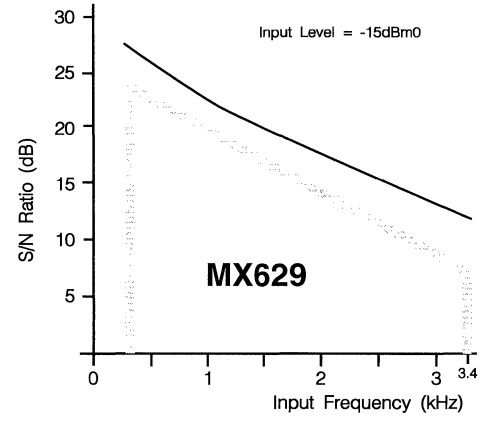
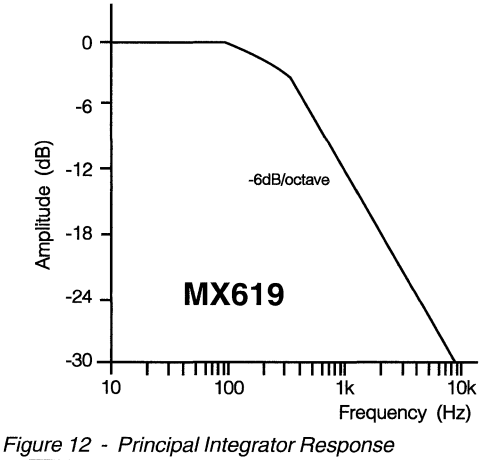


Figure 11 - S/N vs Input Frequency (32kbit/s)



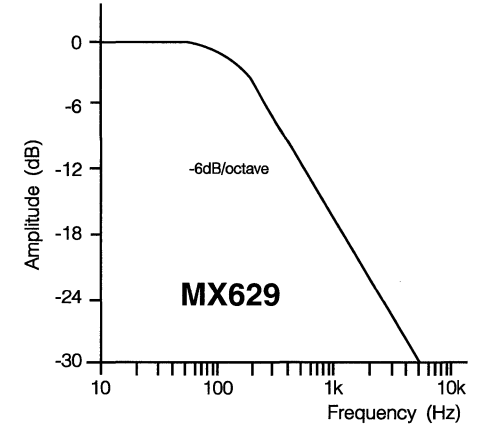


Figure 12 - Principal Integrator Response

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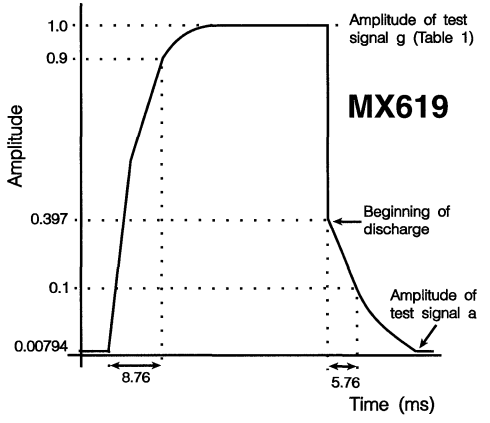
MX619 Codec Performance...

relative to the EUROCOM D1-IA8 Specification

MX629 Codec Performance...

relative to the Mil-Std-188-113 Specification



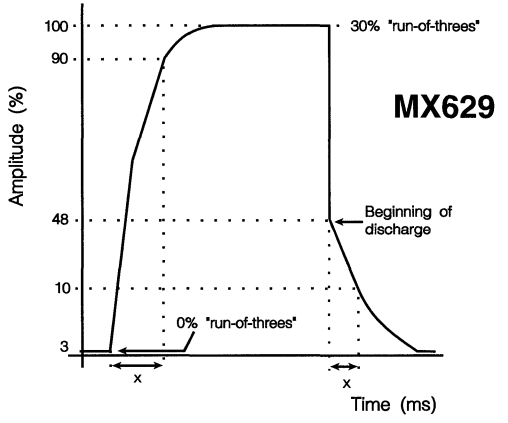
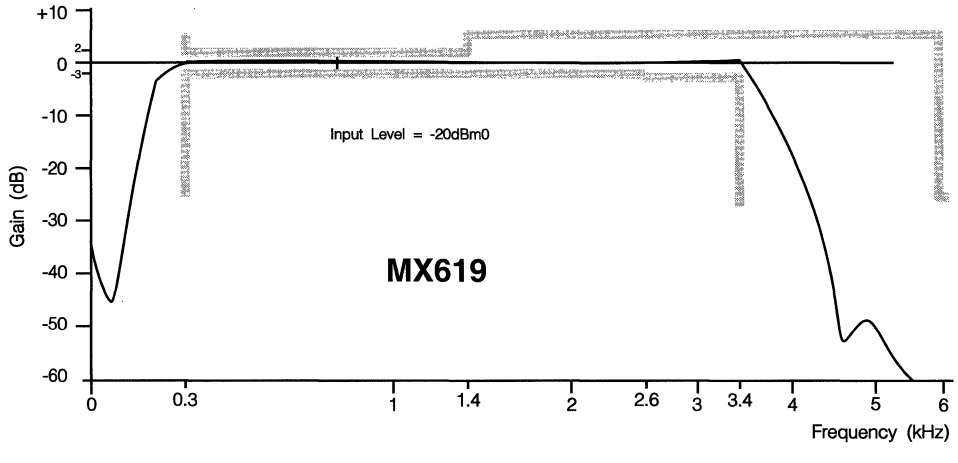


Figure 13 - Compand Envelope



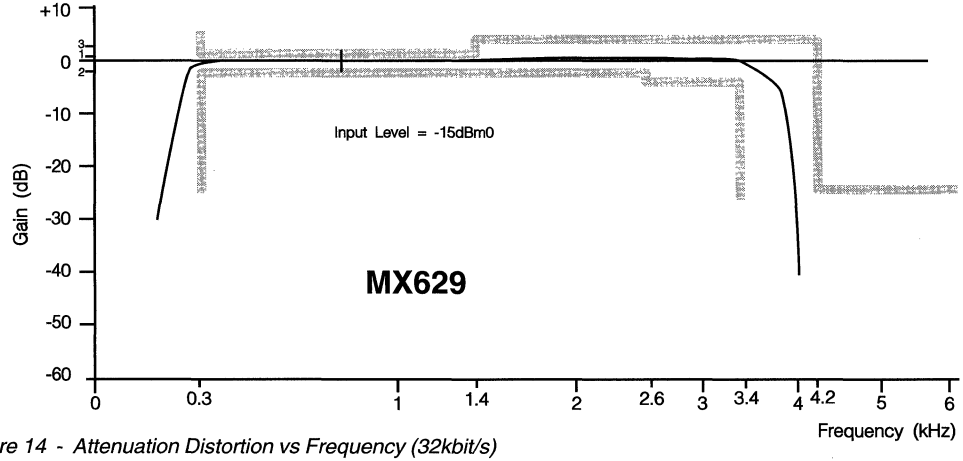


Figure 14 - Attenuation Distortion vs Frequency (32kbit/s)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 V to V_{DD} + 0.3 V
Sink/Source Current: supply pins	±30mA
other pins	±20mA
Total Device Dissipation @ T_{AMB} = 25°C	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Audio Test Frequency = 800 Hz (MX619)
820 Hz (MX629)

Sample Clock Rate = 32kb/sec

Xtal/Clock f_0 = 1.024 MHz

3-bit Compand Algorithm

Audio Level 0dB ref. (0 dBmO) = 489 mVrms

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage	1	4.5	5.0	5.5	V
Supply Current (Enabled)					
MX619		-	4.5		mA
MX629		-	5.5	-	mA
Supply Current (Powersave)					
MX619		-	1.0	-	mA
MX629		-	0.4	-	mA
Input Logic "1"	8	3.5	-	-	V
Input Logic "0"	8	-	-	1.5	V
Output Logic "1"	8	4.0	-	-	V
Output Logic "0"	8	-	-	1.0	
Digital Input Impedance					
Logic I/O Pins		1.0	10	-	MΩ
Logic Input Pins, Pullup Resistor	2	300	-	-	kΩ
Digital Output Impedance					
MX619		-	4	-	kΩ
MX629		-	-	4	kΩ
Analog Input Impedance	4	-	1	-	kΩ
Analog Output Impedance	7	-	-	800	Ω
Three State Output Leakage					
Current (output disabled)		-4	-	+4	µA
Insertion Loss	3	-2	-	+2	dB
Dynamic Values	1,9				
Encoder:					
Analog Signal Input Levels					
MX619	5,9	-35	-	+6	dBmO
MX629	5,9	-35	-	+12	dBmO
Principal Integrator Frequency					
MX619		-	275	-	Hz
MX629		127	159	212	Hz

6

Characteristics	See Note	Min.	Typ.	Max.	Unit
Encoder Passband		-	3400	-	Hz
Compand Time Constant					
MX619		-	4	-	ms
MX629		4.0	5.0	6.0	ms
Decoder:					
Analog Signal Output Levels					
MX619	5,9	-35	-10	+6	dBmO
MX629	5,9	-35		+12	dBmO
Decoder Passband		300	-	3400	Hz
Encoder Decoder (Full Codec)					
Compression Ratio					
MX619 (Cd=0.5 to Cd=0.0)		50	-	-	
MX629 (Cd=0.3 to Cd=0.0)		-	16:1	-	
Passband		300	-	3400	Hz
Stopband					
MX619		6	-	10	kHz
MX629		4.2	-	-	kHz
Stopband Attenuation					
MX619		-	60	-	dB
MX629 (4200Hz to 6000Hz)		25	-	-	dB
(>6kHz)		-	60	-	dB
Passband Gain		-	0	-	dB
Passband Ripple (300Hz-1400Hz)		-1	-	+1	dB
(1400Hz-2600Hz)		-1	-	+3	dB
(2600Hz-3400Hz)		-2	-	+3	dB
Output Noise (Input Short Circuit)					
MX619	9	-	-	-60	dBmOp
MX629	9	-	-55	-	dBmO
Perfect Idle Channel Noise (Encoder Forced)					
MX619	-	-	-63	-	dBmOp
MX629	9	-	-57	-	dBmO
Group Delay Distortion (1000Hz-2600Hz)	6	-	-	450	µs
(600Hz-2800Hz)	6	-	-	750	µs
(500Hz-3000Hz)	6	-	-	1.5	ms
Xtal/Clock Frequency		-	1024	-	kHz

NOTES:

1. Dynamic characteristics are specified at 5V unless otherwise specified.
2. All logic inputs except Encoder and Decoder Data Clocks.
3. For an Encoder/Decoder combination, Insertion Loss contributed by a single component is half this figure.
4. Driven with a source impedance of <100 Ω.
5. Recommended values - See Figures 5, 6, 7 and 8.
6. Group Delay Distortion for the full codec is relative to the delay with an 820Hz, -20dB signal at the encoder input.
7. An Emitter Follower output stage.
8. 4V = 80% V_{DD}, 3.5V = 70% V_{DD}, 1.5V = 30% V_{DD}, 1V = 20%V_{DD}.
9. Analog Voltage Levels used: 0dBmO = 489mVrms = -4dBm = 0dB. -15dBmO = 87mVrms. -20dBmO = 49mVrms = -24dBm.

MX·COM, INC.

MX709

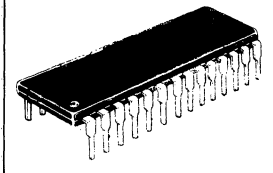
Voice Store Retrieve CVSD Codec

FEATURES:

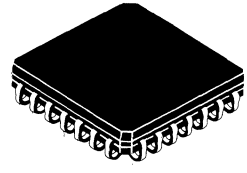
- **Delta Modulation Encoding**
- **Bytewide Storage and Control**
- **Programmable Sampling Rate and Filter**
- **Low Power CMOS Requirements**
- **Microprocessor-Friendly**

APPLICATIONS:

- **Digital Speech Communications**
- **Digital Scrambling**
- **Voice Message Mailbox**
- **Speech Analysis**
- **Voice Multiplexing**
- **Speech Compression**



MX709J (CDIP)
MX709P (PDIP)
28 pins



MX709LH8
(28p PLCC)

DESCRIPTION:

The MX709 is a continuously variable slope delta modulation (CVSD) codec for a wide variety of digital audio processing applications. Its primary use is in microprocessor-controlled voice storage and retrieval systems.

In the encode mode, audio input signals are band-limited by a lowpass filter and digitized by a CVSD 1-bit serial encoder. After conversion to 8-bit parallel format, encoded data is read to the data bus for storage in memory.

In the decode mode, memory contents written into the data bus are converted back to 1-bit serial form and decoded by a CVSD decoder. The decoder output is lowpass filtered and output as retrieved audio.

The audio encode/decode functions are independently controlled, permitting concurrent or asynchronous VSR operations. Time and frequency companding is available via independently programmable encode/decode data rates and filter cut-offs.

Support of VOX functions and "Pause" memory management is provided by the power assessment register. This register contains two 4-bit numbers representing the average signal levels into the data encoder and a replica encoder over a programmable averaging period.

The device instruction set includes input/output signal switching and a standby power-save function. The MX709 is a low power CMOS circuit and requires only a single 5V supply.

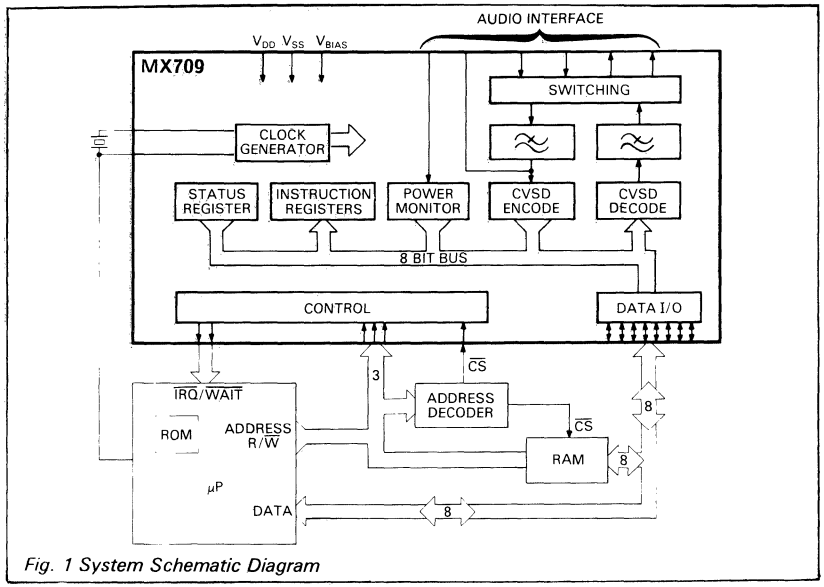


Fig. 1 System Schematic Diagram

MX709 PIN FUNCTION TABLE

PIN	FUNCTION/DESCRIPTION

MX709J, P
MX709LH

1 **$\overline{\text{Xtal}}/\overline{\text{Clock}}$:** Output of a clock oscillator inverter.

2 A_0
3 A_1 ┐ These pins determine which register may be addressed via the I/O Port.
4 $R/\overline{W}$ ┘

Table

A_0	A_1	$R/\overline{W}$	Register
0	0	0	'A' instruction
1	0	0	'B' instruction
0	1	0	Decoder
1	1	0	No register
0	0	1	Status
1	0	1	Power
0	1	1	Encoder
1	1	1	No register

5 **$\overline{\text{CS}}$:** Chip select input, this input has 1MΩ pullup to V_{DD}.

6 D_0 ┐
7 D_1 │
8 D_2 │
9 D_3 ├ **I/O port**
10 D_4 │
11 D_5 │
12 D_6 │
13 D_7 ┘

14 **$\overline{\text{IRQ}}$:** Interrupt request output (100KΩ pullup), this pin is the output of the interrupt request generator. This device can be "wire OR'd" with other active low components. See section on Interrupt Requests.

15 **No Connection**

16 **No Connection**

17 **Analog output B:** *(See Fig. 4.)*

18 **Analog output A:** *(See Fig. 4.)*

19 **V_{Bias}:** This is the bias or analog ground pin and is internally set to $V_{DD}/2$. It should be decoupled to V_S with a capacitor of 1.0μF (min.).

20 **Analog input A:** *(See Fig. 2, Note 4 and Fig.4)*

21 **V_{DD}:** Positive supply.

22 **Analog input B:** *(See Fig. 2, Note 4 and Fig. 4)*

23 **No Connection.**

24 **Analog input C:** This is the analog input to the power encoder.

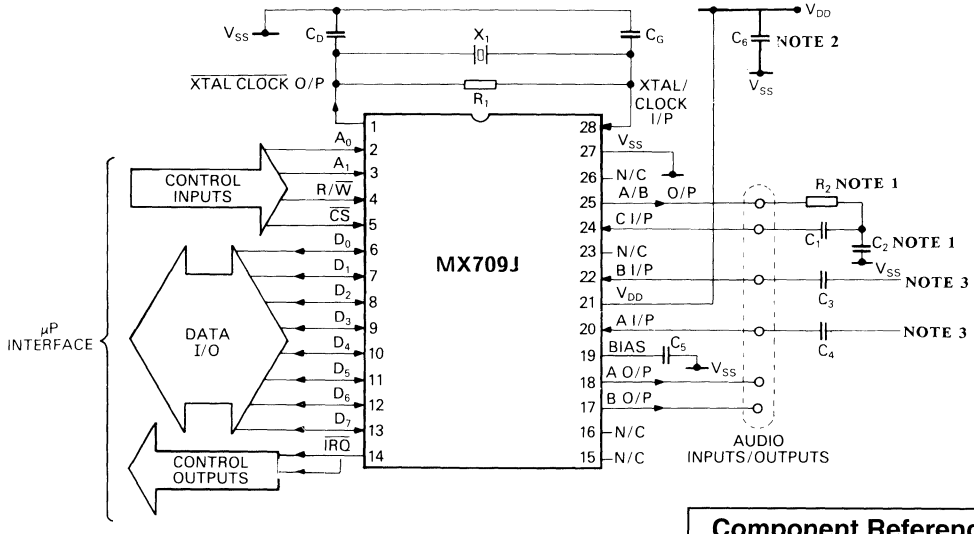
25 **Analog output A/B:** *(See Fig. 4.)*

26 **No Connection.**

6

MX709 PIN FUNCTION TABLE

PIN	FUNCTION/DESCRIPTION
MX709J, P **MX709LH**	
27	**V_{SS}:** Negative supply.
28	**Xtal/Clock Input:** This is the input to the clock oscillator inverter. 1MHz Xtal input or externally derived clock is injected at this pin.



NOTES:

1. R_2, C_2 forms a lowpass filter input to "C" input power assessment circuit. The values shown represent a 820 Hz lowpass although other cutoff frequencies may be selected depending on the application.

2. Additional decoupling may be necessary for noisy supplies.

3. To prevent unwanted internal oscillations at the Encoder Input pins, the source impedance to these inputs must be less than 1 Kohm. Ideally, the source impedance should be less than 50 ohms to minimize granular noise.

Component References

Component	Value	Tolerance
R_1	>1M	±10%
R_2	5.6k	±10%
C_G	68p	
C_D	33p	
C_1	0.1μ	±20%
C_2	.033p	±20%
C_3	0.1μ	±20%
C_4	0.1μ	±20%
C_5	1.0μ min.	±20%
C_6	0.1μ	±20%

FIG. 2: EXTERNAL COMPONENT CONNECTIONS

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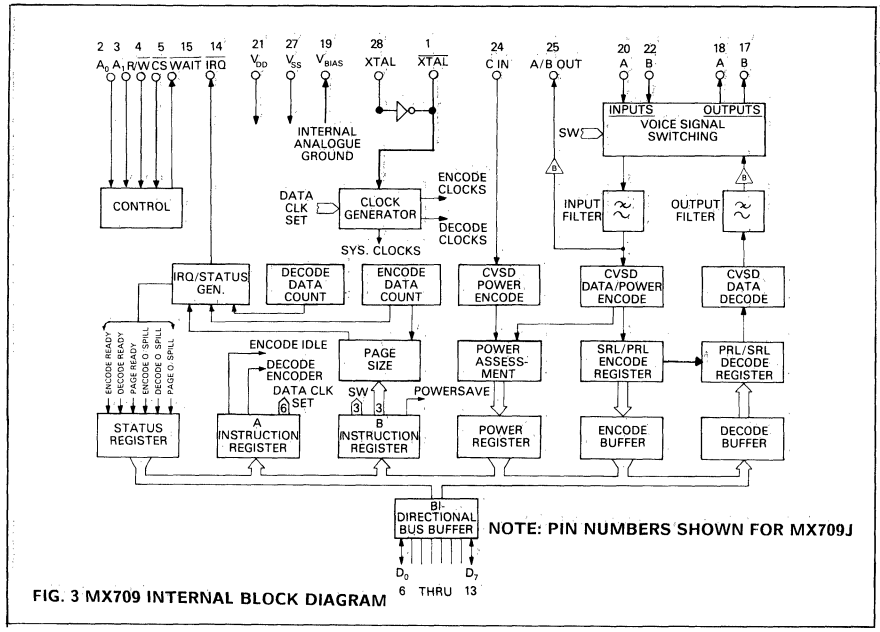
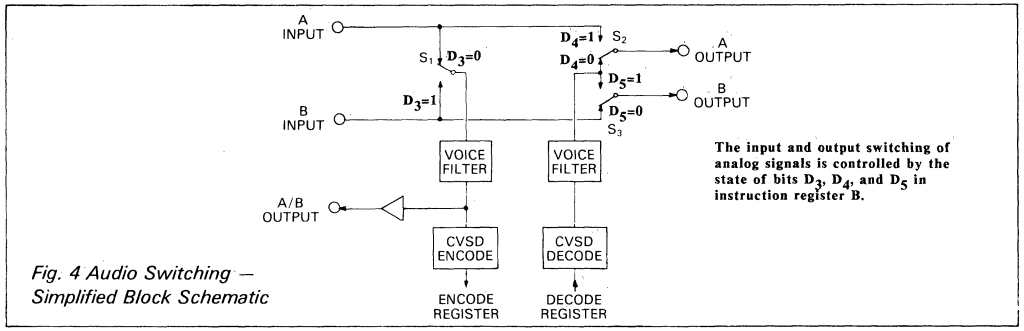


FIG. 3 MX709 INTERNAL BLOCK DIAGRAM

ANALOG SWITCHING



The input and output switching of analog signals is controlled by the state of bits D_3, D_4, and D_5 in instruction register B.

Fig. 4 Audio Switching — Simplified Block Schematic

Frequency and Data Rate Control

Six bits of Instruction Register A **(D_2-D_7)** control the data rates of the encoder and decoder and the bandwidths of the filters for the encoder and decoder. The configuration of the frequency dividers is as shown in the diagrams below and obtainable combinations of frequencies with various input clocks are listed.

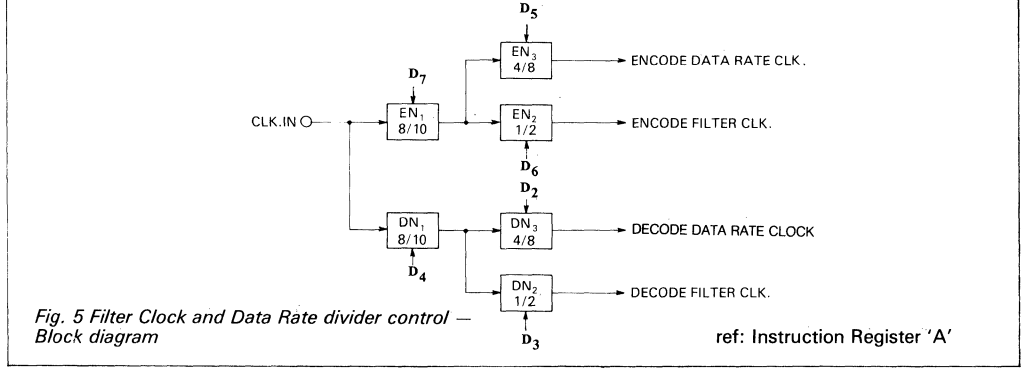


Fig. 5 Filter Clock and Data Rate divider control — Block diagram

Clock Input	Encoder Clock Programming Bits in Register A	Decoder Clock Programming Bits in Register A	Filter Clock (Hz)	Lowpass Filter BW pb. ±1dB	Data Clock (kbs)
2MHz	010xxxxx	xxx010xx	125k	3320	62.5
"	011xxxxx	xxx011xx	125k	3320	31.25
"	110xxxxx	xxx110xx	100k	2656	50.0
"	111xxxxx	xxx111xx	100k	2656	25.0
1MHz	000xxxxx	xxx000xx	125k	3320	31.25
"	001xxxxx	xxx001xx	125k	3320	15.625
"	010xxxxx	xxx010xx	62.5k	1660	31.25*
"	011xxxxx	xxx011xx	62.5k	1660	15.625*
"	100xxxxx	xxx100xx	100k	2656	25.0
"	101xxxxx	xxx101xx	100k	2656	12.5
"	110xxxxx	xxx110xx	50k	1328	25.0*
"	111xxxxx	xxx111xx	50k	1328	12.5*
2.048MHz	010xxxxx	xxx010xx	128k	3400	64.0
"	011xxxxx	xxx011xx	128k	3400	32.0
"	110xxxxx	xxx110xx	102.4k	2720	51.2
"	111xxxxx	xxx111xx	102.4k	2720	25.6
1.024MHz	000xxxxx	xxx000xx	128k	3400	32.0
"	001xxxxx	xxx001xx	128k	3400	16.0
"	010xxxxx	xxx010xx	64k	1700	32.0*
"	011xxxxx	xxx011xx	64k	1700	16.0*
"	100xxxxx	xxx100xx	102.4k	2720	25.6
"	101xxxxx	xxx101xx	102.4k	2720	12.6
"	110xxxxx	xxx110xx	51.2k	1360	25.6*
"	111xxxxx	xxx111xx	51.2k	1360	12.6*
614.4kHz	001xxxxx	xxx001xx	76.8k	2040	9.6*
768.0kHz	101xxxxx	xxx101xx	76.8k	2040	9.6*

Table 1 Possible combinations of clock input frequency, filter cutoff (Hz) and Data Clock (kbs)

**Caution: Although possible, the Codec insertion loss is not according to the specification at these settings.*

Register Truth Tables

The following tables describe the function of each bit within each register. 'Address Input' logic states are shown in the top right hand corner of each table. The following registers are described below:

Instruction Register 'A' [IRA]
Instruction Register 'B' [IRB]
Status Register [SR]
Power Register [PR]

IRA **INSTRUCTION REGISTER 'A'**

$A_0 = 0$
$A_1 = 0$
$R/\overline{W} = 0$

Bit	Function Name	Logic State	References	NOTES
D_0	Encoder Idle		SRD_3	D_0 sets the encoder idle/normal mode of operation.
		1		**FORCED:** Forces the encode register to fill with a 1010101... idle pattern. *Note: incoming encoded data is still available for the power assessment circuits.*
		0		**NORMAL:** Allows the encode register to fill with encoded data. Data is transferred to the encode buffer during the last bit of the encode byte.
D_1	Decoder Data Source		SRD_4	D_1 determines the source of data for the decoder.
		1		**ENCODER:** Internally connects the output of the encode register to the input of the decode register. This condition effectively connects the audio straight through. The encoded data may still be accessed via the encode buffer, and data bus.
		0		Fills the decoder register with idle pattern. In either case data may be loaded into the decoder register via the data bus. This automatically overwrites the current contents of the decoder register.
D_2	Decode Data Rate Clock Divider		Fig. 5 Table 1	D_2 sets the Decode data rate divider.
		1		÷ 8
		0		÷ 4
D_3	Decode Filter Clock Divider		Fig. 5 Table 1	D_3 sets the Decode Filter Clock Divider and hence the Filter Cut-off Frequency.
		1		÷ 2
		0		÷ 1
D_4	Decode Master Clock Divider		Fig. 5 Table 1	D_4 sets the Decode Master clock divider.
		1		÷ 10
		0		÷ 8

IRA — INSTRUCTION REGISTER 'A'

$A_0 = 0$
$A_1 = 0$
$R/\overline{W} = 0$

Bit	Function Name	Logic State	References	NOTES
D_5	Encode Clock Divider		Table 1	D_5 sets the Encode Data Rate Divider.
		1		÷ 8
		0		÷ 4
D_6	Encode Filter Clock Divider		Table 1	D_6 sets the Encode Filter Clock Divider and hence the filter cut-off frequency.
		1		÷ 2
		0		÷ 1
D_7	Encode Master Clock Divider	1	Table 1	D_7 sets the Encode Master Clock Divider ÷ 10
		0		÷ 8

IRB — INSTRUCTION REGISTER 'B'

$A_0 = 1$
$A_1 = 0$
$R/\overline{W} = 0$

Bit	Function Name	Logic State	References	NOTES
D_0, D_1, D_2	Page Size Set			D_0-D_2 set the "page size" in Encode Data bytes. (one byte = 8 serial data bits) in accordance with the table below:

D_2	D_1	D_0	:	PAGE BYTES	Page period @ 32 kbs
0	0	0	:	32	8ms
0	0	1	:	64	16ms
0	1	0	:	96	24ms
0	1	1	:	128	32ms
1	0	0	:	160	40ms
1	0	1	:	192	48ms
1	1	0	:	224	56ms
1	1	1	:	256	64ms

Page Period (sec) = 8 × Page Bytes/Data Rate (b/s)

D_3	"A/B" Encode		Fig. 4	D_3 defines which audio input A or B is connected to the encoder via the encode filter. (See fig. 4).
		0		**AUDIO INPUT "A":** Internally connects the "A" audio input to the encode filter input. The "A/B OUT" pin outputs filtered audio "A." Audio input "B" set to $V_{DD}/2$.
		1		**AUDIO INPUT "B":** Internally connects the "B" audio input to the encode filter input. The "A/B OUT" pin controls filtered audio "B." Audio input "A" set to $V_{DD}/2$.

6

IRB **INSTRUCTION REGISTER 'B'**

$A_0 = 1$
$A_1 = 0$
$R/\overline{W} = 0$

Bit	Function Name	Logic State	References	NOTES
D_4	Switch Audio Output		Fig. 4	D_4 controls the Output Audio Switch to determine which source audio is connected to Audio Output "A" pin.
	"A"	1		Input "A" to Output "A" (direct).
		0		Decoder to Output "A."
D_5	Switch Audio Output		Fig. 4	D_5 controls the Output Audio Switch to determine which source audio is connected to Audio Output "B" pin.
	"B"	1		Decoder to Output "B."
		0		Input "B" to Output "B" (direct).
D_6	Powersave			D_6 controls the enablement and disablement of all analog circuit elements.
		1		**POWERSAVE MODE:** Disables the circuit elements, thereby effectively reducing current consumption.
		0		**OPERATING MODE:** All circuit elements enabled.
				NOTE: During POWERSAVE, inputs are biased $V_{DD}/2$. Outputs are biased $V_{DD}/2$ if IRB D_4/D_5 are set to "direct."
D_7	Power Sensitivity			D_7 determines the sensitivity range of the power measuring circuits.
		1		**HIGH:** Low power input, assessment circuits have + 12dB gain over LOW Setting.
		0		**LOW:** Normal power assessment sensitivity range.
				NOTE: High input levels in the HIGH condition may lead to overflow, producing an ambiguous reading.

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SR	STATUS REGISTER	$A_0 = 0$ $A_1 = 0$ $R/\overline{W} = 1$

Bit	Function Name	Logic State	References	NOTES
D_0	Encode Data Ready			D_0 indicates that a byte of data has been encoded and can be read from the encode buffer.
		1		**READ BYTE:** Set high during the last bit of the byte shifted into the encode register. This condition causes an interrupt request.
		0		**NOT READY/OVERSPILL:** This condition occurs when: 1. The last data byte in the encode data register has been read. 2.Encode data overspill bit = 1 i.e. $SRD_3 = 1$.
D_1	Decode Data Ready			D_1 indicates that a byte of data has been decoded and a new byte should be written to the decode buffer.
		1	SRD_4	**WRITE BYTE:** This condition occurs when the decode register has been loaded from its buffer, i.e. after the last bit of the previous byte has been clocked out of the register.
		0		**NOT READY/OVERSPILL:** This condition occurs when data has been written into the decode buffer or the decode data overspill condition is valid (**$SRD_4 = 1$**).
D_2	Page Ready			This bit indicates that a page of bytes has been encoded.
		1		**READ PAGE:** This condition occurs when the page counter has completed the last byte of a page. This is after power measurements have been written into PRD_0 to PRD_7 inclusive.
		0	SRD_5	**NOT READY/OVERSPILL:** This condition occurs when Power Register "PR" has been read or the page overspill condition is valid.
D_3	Encode Overspill	1		**OVERSPILL:** Indicates that the encode data was not read between two consecutive "encode data ready" flags. Encoded data bytes have been lost, and no further bytes will be transferred to the encode buffer.
		0		**NORMAL:** This condition occurs when data has been read from the encode buffer, following a data ready flag, $SRD_0 = 1$, or by writing to the decode buffer if both encode and decode overspill bits are set.

SR — STATUS REGISTER

$A_0 = 0$
$A_1 = 0$
$R/\overline{W} = 1$

Bit	Function Name	Logic State	References	NOTES
D_4	Decode Overspill	1		**OVERSPILL:** When this bit is set data transfer from the decode buffer to the decode register is inhibited. If the "DECODER/ENCODER BUS" **($IRAD_1$)** is not set then the decode register will fill with idle pattern.
		0		**NORMAL:** This condition occurs when data has been written to the decode buffer following a data ready flag, $SRD_1 = 1$, or by reading the contents of the encode buffer if both encode and decode overspill bits are set.
D_5	Page Overspill	1		**OVERSPILL:** This state indicates that the power register was not read before the next page was completed.
		0		**NORMAL:** Power register "read" or IRB written.

PR — POWER REGISTER

$A_0 = 1$
$A_1 = 0$
$R/\overline{W} = 1$

Bit	Function Name	Logic State	NOTES
D_0	"A/B" Power LSB		D_0-D_3 represent the average signal level of the last page of data in the range from + 6dBm to - 24dBm (at 1kHz) for the A or B input. (0dBm = 775mVRMS)
D_1			The relationship between binary value and signal level is frequency dependent and exhibits pre-emphasis characteristics. (see fig. 8.)
D_2			
D_3	"A/B" Power MSB		
D_4	"C" Power LSB		
D_5			D_4-D_7 represent the average signal level of the last page of data in the range from + 6dBm to - 24dBm (at 1kHz) for the C input.
D_6			
D_7	"C" Power MSB		

Interrupts

Three conditions can cause interrupt requests to the host microprocessor.
(i) The encoder buffer contains an unread byte of data which is the most recent byte encoded.
(ii) The decode buffer is ready to receive the next consecutive byte for decoding.
(iii) The power register contains a power assessment for the most recent whole page encoded.

The status register indicates which of the above conditions are true.

If an interrupt condition remains unserviced and the condition becomes irrecoverably untrue, the status bit is cleared, the corresponding overspill bit is set, and further interrupts are automatically inhibited. Also the encode and decode data buffers retain the data present when the data bit was set, i.e. register-buffer update is inhibited. The power register is updated at all times.

Condition (i) is serviced by a valid address to the encode buffer. Condition (ii) is serviced by a valid address to the decode buffer. If conditions (i) and (ii) have both become UNTRUE, servicing either buffer resets both to a clear start position. Condition (iii) is serviced by reading the Power Register.

The C Input

By careful selection of the audio frequency filtering to the C input, the A/B and C power words can be used in the processor to provide frequency as well as power information. This facility could be used for word, pause or voice recognition.

MX709 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref. V_{ss} = OV)		−0.3V to (V_{DD} + 0.3V)
Output sink/source current (total)		20mA
Operating temperature range:	MX709J	−30°C to + 85°C
	MX709LH,P	−30°C to + 70°C
Storage temperature range:	MX709J	−55°C to + 125°C
	MX709LH,P	−40°C to + 85°C

Operating Limits

All characteristics measured using the following parameters unless otherwise specified: V_{DD} = 5V, T_{amb} = 25°C, ∅ = f_{in} = 1MHz

Characteristics	See Note	Min	Typ	Max	Unit
Static Characteristics					
Supply Voltage		4.5	5.0	5.5	V
Supply Current		—	6	—	mA
Supply Current (Power Save)		—	1	—	mA
Supply Ripple		—	50	—	mV
Input Impedance (Audio)		100	—	—	kΩ
Output Impedance (Audio)		—	—	6	kΩ
Input Logic '1'		3.5	—	—	V
Input Logic '0'		—	—	1.5	V
Output Logic '1'	1	3.5	—	—	V

MX709 ELECTRICAL SPECIFICATIONS (cont.)

Characteristics		See Note	Min	Typ	Max	Unit
Static Characteristics (cont.)						
Output Logic '0'		1	—	—	1.5	V
Input Current (Logic I/P's)			—	—	1.0	μA
Input Capacitance (Logic I/P's)			—	—	7.5	pF
Output Logic '1' Source current		2	—	—	120	μA
Output Logic '0' Sink current		3	—	—	360	μA
Three State output leakage current			—	—	4	μA
Dynamic Characteristics						
Audio Input Level			—	500	—	mV (rms)
Insertion Loss (Direct)		4, 7	-1.5	—	+1.5	dB
Attenuation distortion (See fig. 6)						
Clock bit Rate		5	8	—	64	k bits/sec
Idle Channel Noise		4, 6	—	2.5	—	mV (rms)
Signal/Noise Ratio (see fig. 8)						
Timing Information						
Address Set up time	(tAS)	8	50	—	—	ns
Read Write Set up time	(tRWS)	8	50	—	—	ns
Address Hold time	(tAH)	8	0	—	—	ns
Read Write Recovery time	(tRWR)	8	0	—	—	ns
Chip Select Access time	(tACS)	8	—	—	250	ns
Output Hold time (read)	(tOHR)	8	0	—	100	ns
Data Set up time (write)	(tDSW)	8	150	—	—	ns
Data Hold time (write)	(tDHW)	8	50	—	—	ns

Notes

1. *Load 50pF, 200kΩ*
2. *V_{out} = 4.6V, not pins 12 ($\overline{IRQ}$) and 15 ($\overline{Wait}$), these pins have 100kΩ pullups to VDD.*
3. *V_{out} = 0.4V*
4. *Measured from Codec audio input to audio output.*
5. *2.048MHz master clock ÷ 32*
6. *32kHz clock.*
7. *For a load of > 100kΩ, serial switch impedance is 3kΩ/switch (See Fig. 4).*
8. *See Figure 7 Timing Diagram*

Typical Performance

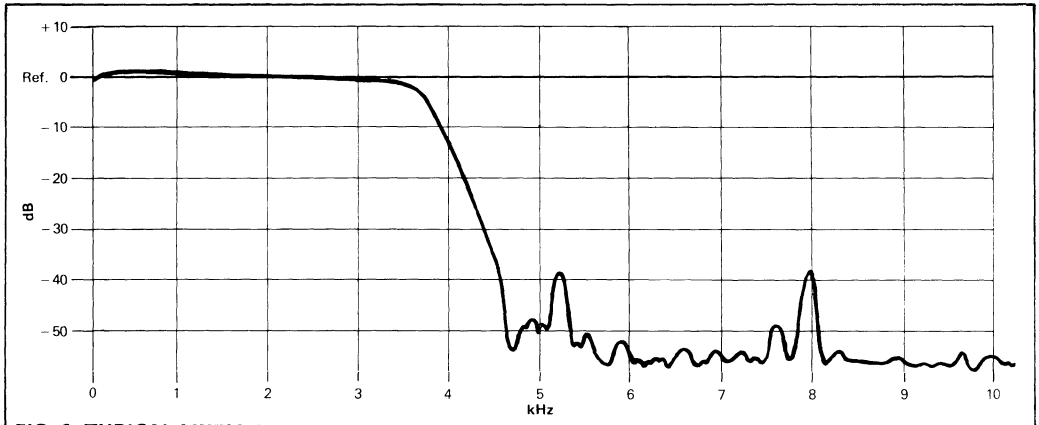
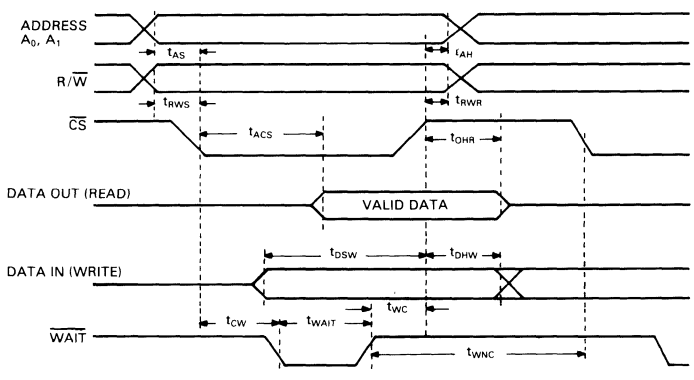


FIG. 6: TYPICAL MX709 SYSTEM RESPONSE MEASURED AT: FILTER 3320 HZ, V_{IN} -24 dBm, 32 KB/SEC



t=	Min.	Typ.	Max.	Units
t_{AS}	50	–	–	ns
t_{RWS}	50	–	–	ns
t_{AH}	0	–	–	ns
t_{RWR}	0	–	–	ns
t_{ACS}	–	–	250	ns
t_{OHR}	0	–	100	ns
t_{DSW}	150	–	–	ns
t_{DHW}	50	–	–	ns
t_{CW}	–	–	100	ns
t_{WAIT}	2	–	3	Xtal Cycle
t_{WC}	0	–	–	ns
t_{WNC}	2	–	–	Xtal Cycle

KEY

t_{AS} – Address Set Up Time
t_{RWS} – Read/Write Set Up Time
t_{AH} – Address Hold Time
t_{RWR} – Read/Write Recovery Time
t_{ACS} – Chip Select Access Time
t_{OHR} – Output Hold Time (Read)
t_{DSW} – Data Set Up Time (Write)
t_{DHW} – Data Hold Time (Write)
t_{CW} – Chip Select to WAIT Output
t_{WAIT} – WAIT Time
t_{WC} – WAIT High to Chip Select High
t_{WNC} – End of Wait to Next Chip Select

Fig. 7 Timing Diagram

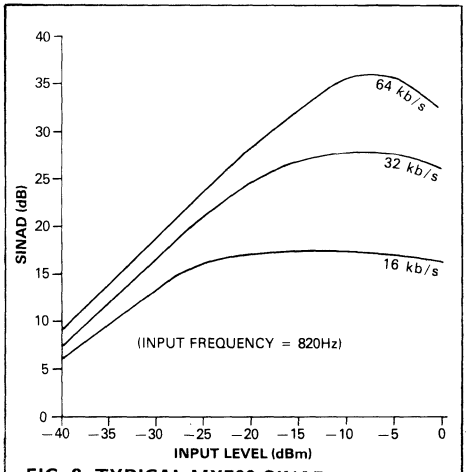


FIG. 8: TYPICAL MX709 SINAD VERSUS INPUT LEVEL

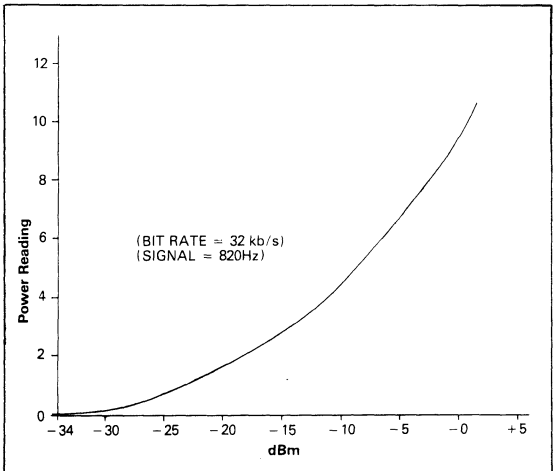
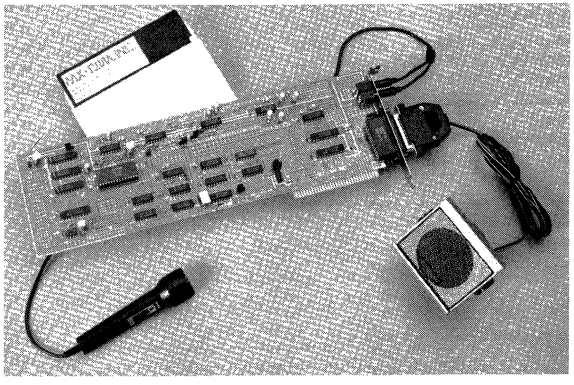


FIG. 9: POWER READING VS. INPUT LEVEL

VSR CODEC EVALUATION SYSTEM

FEATURES:

- **Voice Storage and Retrieval**
- **Speech Power Assessment**
- **Pause Elimination**
- **Digitally Controlled Attenuators**
- **User Program Supplied on Floppy Disk**
- **IBM PC-XT or Similar Compatible**
- **Color Graphic Displays**
- **Audio Mixing Options**
- **Choice of Programming Languages (Pascal or Assembly)**
- **Microphone and Loudspeaker Supplied**



DESCRIPTION:

The PC7090 VSR Evkit is an evaluation card that plugs into the option card slot of any IBM PC-XT or XT-compatible personal computer with a minimum 256K of RAM.

Software provided on floppy disk enables full demonstration and investigation of the MX709 VSR Codec's basic voice storage and retrieval functions via external audio inputs and outputs. The processor-controlled features include:

1) Full keyboard control of storage duration, filter cut-off frequencies, page size, and data clock rates.
2) Programmable attenuators in the A and B audio inputs for setting storage levels.
3) Two selectable 64K audio buffers which are maintained in the host computer for direct comparison of storage and replay methods.
4) Color graphics displays that are available for power assessment and similar statistical presentations.
5) Adjustable pause elimination threshold settings for storage and/or retrieval to demonstrate time and storage space saving.
6) Keyboard selectable audio paths allowing either "line" or the supplied microphone to be switched to any audio channel input.
7) A full VSR status available on the PC display.
8) Loudspeaker output level controlled from the keyboard.

The program's source code, written in both Turbo Pascal and Assembly language, can be used to investigate other PC7090 applications such as time domain scrambling, digital filtering, voice mail, and voice operated relays.

The PC7090 is supplied with a comprehensive instruction manual, software on floppy disk, and a microphone and speaker.

COMMAND DESCRIPTIONS

The EVKIT program is controlled by the following keyboard commands:

1 **Select Buffer 1:** Two independent 64k byte audio buffers are maintained in the main processor.
2 **Select Buffer 2:** Switching between them does not disturb stored data.

S **Store:** Stores the input audio into the selected buffer. The ON/OFF switch on the microphone will pause storage. See <N> for audio source.

R **Retrieve:** Replays the stored audio from the selected audio buffer. Conditions of storage are saved and retrieved with the audio data.

T **Set Storage Duration:** Sets the basic audio storage time. This time will be amended by the software with regard to clock rates and page size.

C **Set Clock Rate:** Selects one of 6 stored sampling rates:

12.5 kb/sec	15.625 kb/sec
25.0 kb/sec	31.25 kb/sec
50.0 kb/sec	62.5 kb/sec

Z **Set Page Size:** Determines the measurement for the MX709 power assessment circuits by setting the page size in bytes. 8 selections in the range 32 bytes to 256 bytes are available.

P & I **Set Retrieval Pause Elimination Parameters:** For setting power threshold and intervals to produce compression of speech pauses on replay.

^P **Set Storage Pause Elimination:** Sets the A:B power threshold. Any page with input power value less than threshold is not stored.

A **Select Assembly/Pascal Routines:** Two languages for assessment with different speed systems.

V **Control Audio Levels:** A and B input and speaker gains are independently variable. The current A and B levels are displayed as vertical bars on the right of the 'menu.'

M **Modify Buffer Clock Rate:** Alters the stored clock rate in a buffer to demonstrate compression or expansion on retrieve.

? **Display Parameters:** Displays current parameters controlling program operation. See Fig. 1.

W **Set Bus Switches:** This command controls the switches for special purpose routing of audio signals.

N **MX709 Configuration:** Sets the switch settings in the three evaluation program modes: Storage, Retrieval, and Standby.

G & D **Graph Page Power:** To graph recorded page power against time. The <D> command sets the graph scales. *See Fig 2.
F **Histogram Audio Data:** A statistical facility for examining the audio data.*

L & / **Page Power Ratios:** A:B and C input power values for the active buffer are listed in tabular form.

*Graphics are only available on machines with a color adaptor.

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Other Peripheral Commands Are:

E	Erase Buffer.
^S	Store Buffer to Disk.
^R	Retrieve Buffer from Disk.
H	Help: Describes fully the instructions above.
Q	Quit.

SCREEN DISPLAYS

Basic Storage and Retrieval routines are demonstrated on the selected audio buffer using <S> and <R> commands. These commands are also programmed in function keys for ease of operation. All available EVKIT commands are displayed by the program menu. The full instructions, with comprehensive explanations, can be selected by the <H> or 'Help' function key.

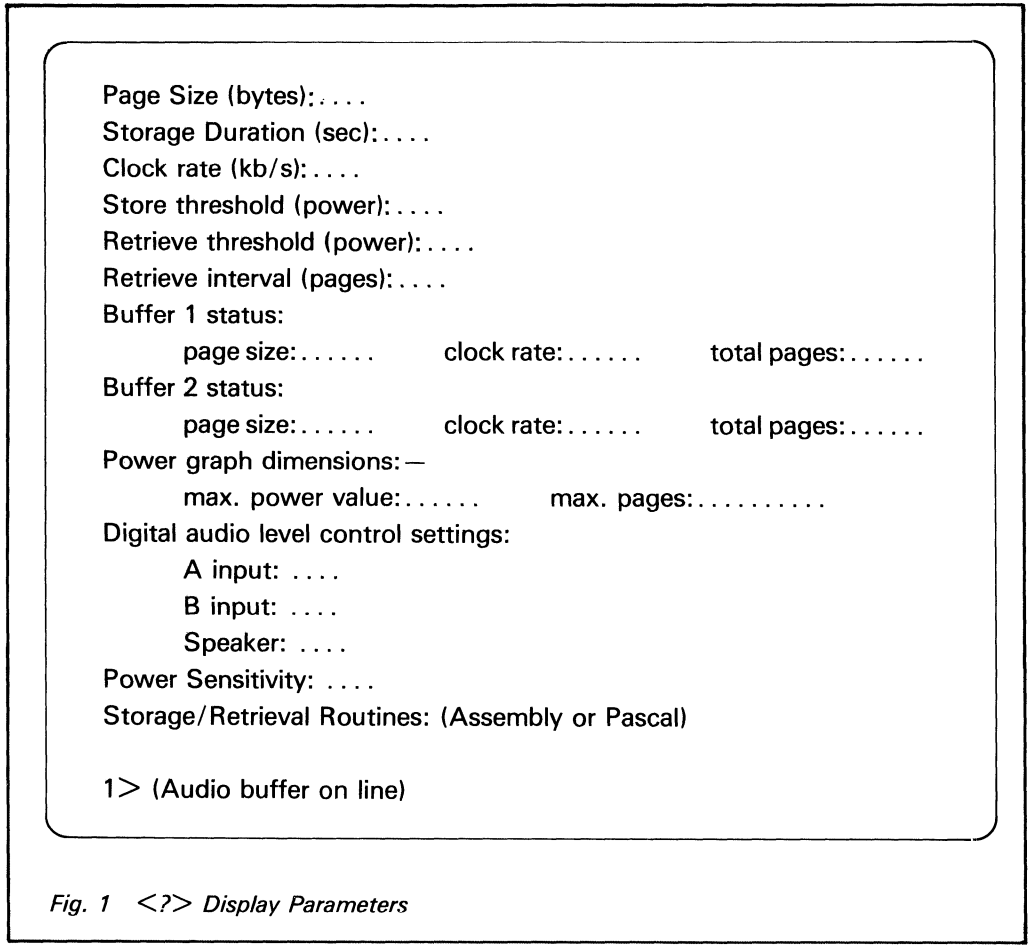


Fig. 1 <?> Display Parameters

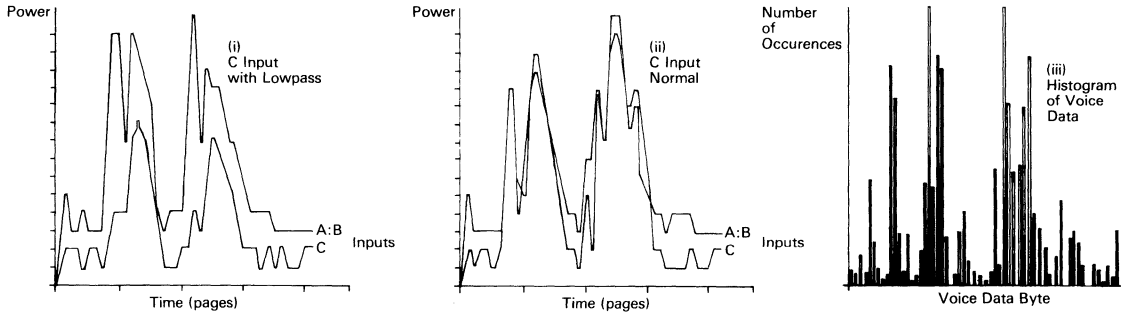


Fig. 2 Typical Graphical Displays Available

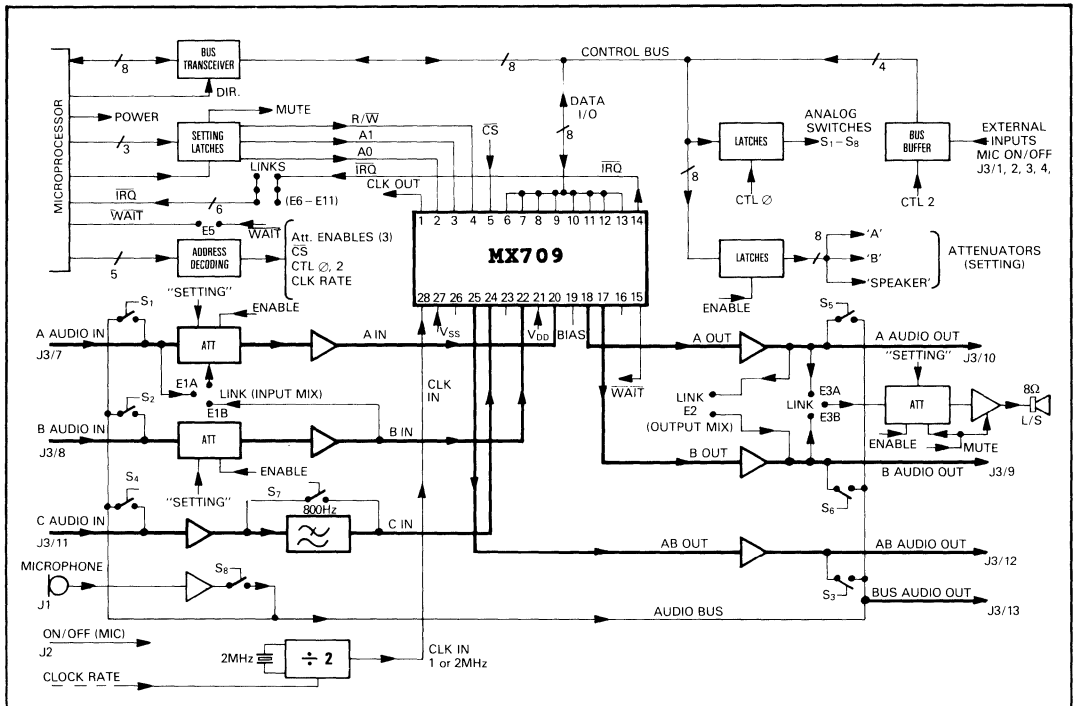


Fig. 3 PC7090 Basic Functional Block Diagram.

ORDERING INFORMATION

PC7090 EVKIT

comprises: **Plug-in printed circuit board.**
Program on floppy disk.
Instruction manual.
Loudspeaker.
Microphone.

Physical dimensions PCB 13.4 in. × 3.94 in.

DVSR CODEC

Description

The MX802 Data/Voice Storage and Retrieval (DVSR) Codec contains a Continuosly Variable Slope Delta Modulation (CVSD) encoder and decoder, as well as control and timing circuitry for up to 4 Mbits of external DRAM. As a member of the DBS 800 series, it also contains interface and control logic for the "C-BUS" serial interface.

When used with external DRAM, the MX802 has four primary functions:

- **Speech Storage**

Speech signals present at the Audio Input may be digitized by the CVSD encoder. The resulting bit stream is stored in DRAM. This process also provides readings of the speech signal power level. These readings are used by the system microcontroller for pause reduction.

- **Speech Playback**

Digitzed speech may be read from DRAM and converted back into analog form by the CVSD decoder.

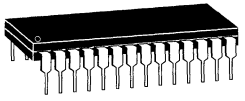
- **Data Storage**

Digital data derived via the C-BUS from the Modem or system data may be stored in DRAM.

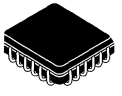
- **Data Retrieval**

Digital data may be read from DRAM and sent over the C-BUS to the system microcontroller.

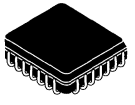
Speech storage and playback may be performed concurrently with data storage or retrieval.



MX802J
28-pin CDIP



MX802LH
PLCC-24



MX802LH8
PLCC-28

The MX802 may also be used without DRAM (as a "stand alone" CVSD codec), in which case direct access is provided to the CVSD Codec digital data and clock signals. All functions are controlled by C-BUS commands from the system microcontroller.

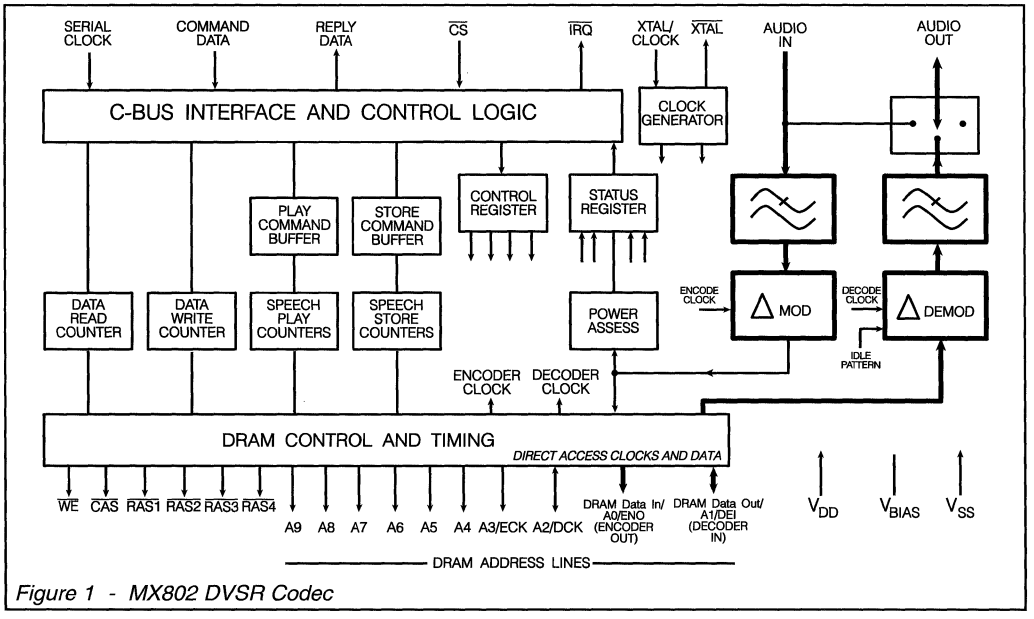


Figure 1 - MX802 DVSR Codec

The storage, recovery and replay functions of the MX802 can be used for:

- •Answering Machine applications, where an incoming speech message is stored for later recall.
- •Busy Buffering, in which an outgoing speech message is stored temporarily until the TX channel becomes free.
- •Automatic transmission of pre-recorded alarm or status announcements.
- •Time Domain Scrambling of speech messages.
- •VOX control of transmitter functions.
- •Temporary Data Storage applications, such as buffering of over-air data transmissions.

On-chip the Delta Codec is supported by input and output analog switched-capacitor filters and audio output switching circuitry. The DRAM control and timing circuitry provides all the necessary address, control and refresh signals to interface to external DRAM.

The MX802 is a low-power 5-volt CMOS LSI device. It is offered in 24- and 28-lead SMT packages, as well as 28-pin DIP packages.

Pin Function Chart

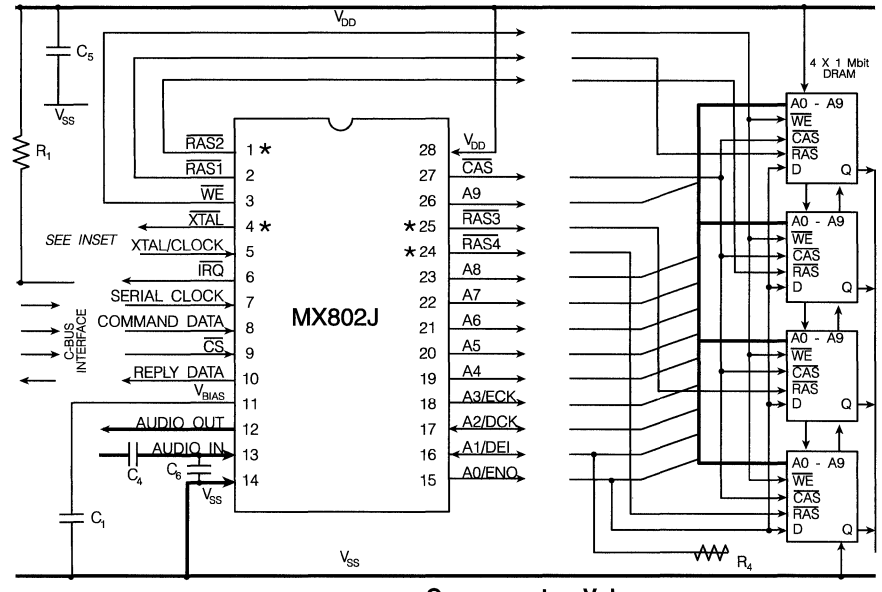
Pin		Function
J/LH8	LH	
1		**Row Address Strobe 2 ($\overline{RAS2}$):** This pin should be connected to the Row Address Strobe input of the second 1 Mbit DRAM chip (if used).
2	1	**Row Address Strobe 1 ($\overline{RAS1}$):** This pin should be connected to the Row Address Strobe input of the first DRAM chip.
3	2	**Write Enable ($\overline{WE}$):** The DRAM Read/Write control pin.
4		**$\overline{Xtal}$:** This is the output of the 4.0 MHz on-chip clock oscillator. External components are required at this output when a Xtal is used. A Xtal cannot be used with the 24-pin version.
5	3	**Xtal/Clock:** This is the input to the on-chip clock oscillator inverter. A 4.0MHz Xtal or externally derived clock should be connected here (see component diagram). This clock provides timing for on-chip elements, filters, etc. A Xtal cannot be used with the 24-pin version. Various Xtal frequencies can be used with this device; see Table 3 for sampling rate variations.
6	4	**Interrupt Request ($\overline{IRQ}$):** The output of this pin indicates an interrupt condition to the microcontroller by going to logic "0." This is a "wire-or able" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the microcontroller. This pin is an open drain output. It therefore has a low impedance pulldown to logic "0" when active and a high impedance when inactive. Conditions indicated by this function are Power Reading Ready, Play Command Complete and Store Command Complete.
7	5	**Serial Clock:** This is the C-BUS serial clock input. This clock, produced by the microcontroller, is used for transfer timing of commands and data to and from the DVSR Codec. See timing diagrams. Clock rate requirements vary for different MX802 functions.
8	6	**Command Data:** This is the C-BUS serial data input from the microcontroller. Data is loaded to this device in 8-bit bytes, MSB (bit 7) first, and LSB (bit 0) last, synchronized to the Serial Clock. See timing diagrams.
9	7	**Chip Select ($\overline{CS}$):** The C-BUS data transfer control function, this input is provided by the microcontroller. Command Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. See timing diagrams.
10	8	**Reply Data:** This is the C-BUS serial data output to the microcontroller. The transmission of Reply Data bytes is synchronized to the Serial Data Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the microcontroller. See timing diagrams.

Pin Function Chart

Pin		Function
J/LH8	LH	
11	9	**V_{BIAS}:** This is the output of the on-chip analog circuitry bias system, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C_1. See Figure 2.
12	10	**Audio Out:** This is the analog signal output.
13	11	**Audio In:** This is the audio (speech) input. The signal to this pin must be a.c. coupled by capacitor C_4 and decoupled to V_{SS} by HF capacitor C_6. For optimum noise performance this input should be driven from a source impedance of less than 100Ω.
14	12	**V_{SS}:** Negative Supply (GND).
15	13	**DRAM Data In/A0/Direct Access -- Encoder Out (ENO):** This is connected to the DRAM data input and address line A0. With no DRAM used, this output is available in a Direct Access mode as the Delta Encoder digital data Output. Direct Access control is achieved by Control Register byte 1, bit 7.
16	14	**DRAM Data Out/A1/Direct Access -- Decoder In (DEI):** This is connected to the DRAM data output and address line A1. With no DRAM used, this pin is available in a Direct Access mode as the Delta Decoder Clock input. Direct Access control is achieved by Control Register byte 1, bit 6.
17	15	**DRAM A2/Direct Access -- Decoder Clock (DCK):** This is the DRAM address line A2. With no DRAM employed, this pin is available in a Direct Access mode as the Delta Decoder Clock Input. Direct Access control is achieved by Control Register byte 1, bit 6.
18	16	**DRAM A3/Direct Access -- Encoder Clock (ECK):** This is the DRAM address line A3. With no DRAM employed, this pin is available in a Direct Access mode as the Delta Encoder Clock Output. Direct Access control is achieved by Control Register byte1, bit 6.
19	17	**DRAM A4:** DRAM address line A4.
20	18	**DRAM A5:** DRAM address line A5.
21	19	**DRAM A6:** DRAM address line A6.
22	20	**DRAM A7:** DRAM address line A7.
23	21	**DRAM A8:** DRAM address line A8.
24		**Row Address Strobe 4 ($\overline{RAS4}$):** This pin should be connected to the Row Address Strobe input of the fourth 1 Mbit DRAM chip (if used).
25		**Row Address Strobe 3 ($\overline{RAS3}$):** This pin should be connected to the Row Address Strobe input of the third 1 Mbit DRAM chip (if used).
26	22	**DRAM A9:** This is DRAM address line A9. This pin is not connected when a 256 kbit DRAM is used. Note: To simplify PCB layout, the DRAM address inputs A0-A8 may be connected in any physical order to the DVSR Codec output pins A0-A8.
27	23	**Column Address Strobe ($\overline{CAS}$):** This is the DRAM Column Address Strobe pin. It should be connected to the $\overline{CAS}$ pins of all DRAM chips.
28	24	**V_{DD}:** Positive supply. A single, stable +5 volt supply is required. Levels and voltages within the DVSR Codec are dependent upon this supply.

6

External Components



Component	Value		
R_1	22.0kΩ	C_4	1.0µF
R_2	1.0MΩ	C_5	1.0µF
R_3	See Note 1	C_6	.001µF
R_4	1.0kΩ	X_1	4.00MHz
C_1	1.0µF		or 4.032MHz
C_2	33.0pF		or 4.096MHz
C_3	33.0pF		

Tolerance: R = ±10%, C = ±20%

*See Note 3

Figure 2 - Recommended External Component and DRAM Connections

Notes

1. Xtal circuitry shown in Inset is in accordance with the MX-COM Standard and DBS 800 Crystal Oscillator Application Note.

2. External Xtal circuitry is not applicable to the 24 pin/lead versions of this device. Only an externally derived clock input can be used.

3. Functions whose pins are marked with an asterisk* in Figure 2 are not available on the 24-pin/lead versions of this device. Pin numbers illustrated are for 28-pin versions.

4. Table 3 details the actual encoder/decoder sample rates available using the Xtal frequencies recommended above.

5. Resistor R_1 is used as the DBS 800 system common pullup for the C-BUS Interrupt Request ($\overline{IRQ}$) line. The optimum value will depend on the circuitry connected to the $\overline{IRQ}$ line. Up to 8 peripherals may be connected to this line.

6. Recommended DRAM Parameters:
256 kbit x 1 or 1 Mbit x 1 Dynamic Random Access Memory with "$\overline{CAS}$ before $\overline{RAS}$" refresh mode. Maximum Row address access time = .200 µsec.

Example DRAM types:

256kbit (262,144 bits)	
Texas Instruments	TMS4256-20
Hitachi	HM51256-15
1Mbit (1,048,576 bits)	
Texas Instruments	TMS4C1024-15
Hitachi	HM511000-15

7. Figure 2 above shows connections to 4 x 1 Mbit sections of DRAM. If desired, to simplify PCB layout, the DRAM inputs A0-A8 may be connected in any order to the MX802 DVSR Codec output pins A0-A8. Connections to 256 kbit DRAM are similar, but A9 is left unconnected.

8. When using the MX802 "stand alone" (Direct Access), no DRAM sections should be connected.

Controlling Protocol

Control of the functions of the MX802 DVSR Codec is by a group of Address/Commands (A/Cs) and appended instructions or data to and from the system microcontroller (See Figure 4). The use and content of these instructions is detailed in the following pages.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB LSB	Data Byte(s)
General Reset	01	0 0 0 0 0 0 0 1	
Write to Control Register	60	0 1 1 0 0 0 0 0	+ 2 byte instruction to Control Register
Read Status Register	61	0 1 1 0 0 0 0 1	+ 1 byte reply from Status Register
Store "N" pages. Start page "X"	62	0 1 1 0 0 0 1 0	+ 2 bytes Command -- Immediate
Store "N" pages. Start page "X"	63	0 1 1 0 0 0 1 1	+ 2 bytes Command -- Buffered
Play "N" pages. Start page "X"	64	0 1 1 0 0 1 0 0	+ 2 bytes Command -- Immediate
Play "N" pages. Start page "X"	65	0 1 1 0 0 1 0 1	+ 2 bytes Command -- Buffered
Write Data. Start page "P"	66	0 1 1 0 0 1 1 0	+ 2 bytes "P" + Write Data
Read Data. Start page "P"	67	0 1 1 0 0 1 1 1	+ 2 bytes "P" + Read Data
Write Data -- Continue	68	0 1 1 0 1 0 0 0	+ Write data
Read Data -- Continue	69	0 1 1 0 1 0 0 1	+ Read data

Table 1 - C-BUS Address/Commands

Address/Commands

Instruction and data transactions to and from this device consist of an Address/Command (A/C) byte followed by further instruction/data or a status/data reply.

Control and configuration is by writing instructions from the microcontroller to the Control Register (60_H). Reporting of MX802 configurations is by reading the Status Register (61_H).

6

Operation with DRAM

The MX802 can operate with up to 4 Mbits of Dynamic RAM (DRAM). When used with DRAM, the MX802 performs four main functions under the control of commands received over the C-BUS interface from the microcontroller:

Stores Speech: The MX802 stores speech by digitally encoding the analog input signal and writing the resulting digital data into the associated DRAM.

Plays Speech: The MX802 plays back stored speech by reading the digital data stored in the DRAM and decoding it to provide an analog output signal.

Writes Data: The MX802 writes data sent over the C-BUS from the microcontroller to DRAM.

Reads Data: The MX802 reads data from DRAM, sending it to the microcontroller over the C-BUS.

Data is directed to and from DRAM by the on-chip DRAM Controller.

Controlling Protocol

Speech

The CVSD encoder and decoder sampling rates are independently set via the Control Register (see Tables 2, 3 & 4) to 16, 25, 32, 50 or 64 kbps. This allows the user to choose between speech quality and storage time while providing for time compression or expansion of the speech signals.

The DVSR Codec can handle from 256 kbits to 4 Mbits of DRAM, giving, in the case of the 32 kbps sampling rate, from 8 to 131 seconds of speech storage.

For speech storage purposes, the memory is divided into "pages" of 1024 bits each, corresponding to 32ms at a 32 kbps sampling rate.

A 256 kbit DRAM contains	256 "pages."
A 1 Mbit DRAM contains	1024 "pages."
A 4 Mbit DRAM contains	4096 "pages."

When used without DRAM, the decoder sampling rate (8-64 kbps) is determined by an external clock source applied to the Decoder Clock pin.

Store and Play Speech Commands

Speech storage and playback may take place simultaneously. These commands are transmitted, via C-BUS, to the MX802 in the following form:

STORE OR PLAY "N" (1024-bit) PAGES (of encoded speech data) STARTING AT PAGE "X."

"N" can be any number between 0 and F (1-16 pages). "X" can be any number from 0 to 4095 (4Mbit DRAM), as shown below. Preceded by A/C, this command writes 16 bits (byte 1 and byte 0) of data from the microcontroller to the Store or Play Command Buffer.

MSB BYTE 1								BYTE 0							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N								X							

Speech Store Commands

62_H STORE "N" PAGES -- START PAGE "X" (immediate)

63_H STORE "N" PAGES -- START PAGE "X" (buffered)

The digitized speech from the CVSD encoder is stored in consecutive DRAM locations with the Speech Store Counters sequencing through the DRAM addresses and counting the number of complete pages stored since the start of the execution of the command.

As soon as the command has terminated, the following events take place:

1. The Store Command Complete bit in the Status Register (Table 5) is set.

2. An Interrupt Request ($\overline{IRQ}$) is sent, if enabled, to the microcontroller.

3. The next speech storage command (if present) is immediately taken from the Store Command Buffer and execution of the new command commences.

The $\overline{IRQ}$ output is cleared by reading the Status Register:

61_H READ STATUS REGISTER (Table 6).

To provide continuity of speech commands, both Store and Play Commands can be presented to eh MX802 in one of two formats: *immediate or buffered.*

An *immediate* command will be started on completion of its loading, irrespective of the condition of the current command.

A *buffered* command will begin after the completion of the current Store or Play command, unless Speech Synchronization Bits (Control Register) are set.

Buffering of commands lets the DVSR Codec execute a series of commands without intervening gaps even though the microcontroller may take several milliseconds to respond to each "Command Complete" Interrupt Request.

In either case, the Store or Play Command Complete bit of the status register will be cleared.

Speech Playback is controlled by similar commands using the Speech Play Counters and Play Command Buffer:

64_H PLAY "N" PAGES -- START PAGE "X" (immediate)

65_H PLAY "N" PAGES -- START PAGE "X" (buffered).

As soon as the Play Command has completed, the "Play Command Complete" bit in the Status Register is set, and an Interrupt Request is generated (if enabled).

If no "next" command is waiting in the Play Command Buffer when a speech play command finishes, a continuous idle code (0101....0101) will be fed to the delta decoder.

Speech data is stored or recovered at the selected Encode or Decode sample rate (Table 3). Store or Play Command Complete bits in the Status Register are cleared by the next Store or Play Command received from the microcontroller, or by a General Reset (01_H).

Controlling Protocol

Speech...

Store/Play Speech Synchronization (Table 4)

This capability is provided primarily for Time Domain Scrambling applications.

Speech Synchronization bits in the Control Register will produce the effects described below:

No Speech Sync Set: Store and Play operations may take place completely independently.

Store after Play: The next buffered store command will start on completion of a play command, while the next play command sequence (if any) continues normally.

Play after Store: The next buffered play command will start on completion of a store command, while the next store command sequence (if any) continues normally.

These actions will continue while Speech Sync bits are set.

Data Handling

For the purpose of storing data sent via C-BUS from the microcontroller, the memory (DRAM) is divided into "data pages" of 64 bits (8 bytes).

A 256kbit DRAM contains	4096 data pages.
A 1Mbit DRAM contains	16384 data pages.
4Mbit DRAM contains	65536 data pages.

In accordance with C-BUS timing specifications, data is handled 8 bits (1 byte) at a time, although any number of 8-bit blocks of data may be written to or read from the DRAM by a single command.

Data transfer is terminated by the Chip Select line going to a logic "1."

C-BUS Data Transfer Limitations

For those commands which transfer data over the C-BUS between DRAM and the microcontroller (Write and Read data), the C-BUS serial clock rate is limited to a maximum of:

125kHz if the VSR Codec is executing store and play commands.

250kHz if no speech Store or Play commands are active.

This limitation is due to the rate at which data goes into and out of the DRAM. All other commands and replies (Control, Status, Reset) may use a maximum clock rate of 500kHz. See Figure 4.

Read Data

67_H READ DATA -- START PAGE "P"

This command sets the Data Read Counter to "P," page, and then reads data bytes from successive DRAM locations, sending them to the microcontroller as Reply Data bytes. The Data Read Counter is incremented by 1 for each bit read.

69_H READ DATA CONTINUE

This command reads data bytes from successive DRAM locations determined by the Data Read Counter, incrementing the counter by 1 for each bit read.

Write Data

66_H WRITE DATA -- START PAGE "P"

This command sets the Data Write Counter to "P" page, and then writes data bytes to successive DRAM locations, incrementing the Data Write Counter by 1 for each bit received via the C-BUS.

The Start Page, "P," is indicated by loading a 2-byte word after the relevant Address/Command byte. This 16-bit word allows data page addresses from 0 to 65535 (4Mbits DRAM).

68_H WRITE DATA CONTINUE

This command writes data bytes to successive DRAM locations determined by the Data Write Counter, incrementing the counter by 1 for each bit received over the C-BUS.

Controlling Protocol

DRAM Speech Capacity

28-pin/lead versions of the MX802 may be used with a single 256kbit DRAM, or with up to 4 x 1Mbit of DRAM. 24-pin/lead versions may only be used with a single 256kbit or 1Mbit DRAM. The different encode and decode sampling clock rates available enable the user to set voice store and play times against recovered speech quality. Table 2 gives information on storage capacity and Store/Playback times. Speech data can be replayed at a different sample rate or in a reversed sequence (see Control Register for details).

DRAM Size	Available Bits	Speech Pages	Nominal Sample Rates (kbps) 16	25	32	50	64
256kbps	262144	256	16.0	10.0	8.0	5.0	4.0
1024kbps	1048576	1024	65.0	42.0	32.0	20.0	16.0
2Mbps	2097152	2048	131.0	84.0	65.0	42.0	32.0
3Mbps	3145728	3072	196.0	126.0	98.0	63.0	49.0
4Mbps	4194304	4096	262.0	168.0	131.0	84.0	65.5
			Store and Play Times (seconds)				

Table 2 - Sampling Clock Rates vs Speech Storage/Playback Times

Encoder and Decoder Sampling Clocks

Encoder and decoder sampling clock rates are programmable via the Control Register. Table 3 shows the range of sampling rates available for different Xtal/clock input frequencies and the counter ratios used to produce them. Consideration should be given to the effect of different Xtal/clock frequencies upon the audio frequency performance of the device.

Control Register *Byte 0, Bits* 5 4 3 Dec. / 2 1 0 Enc.	Internal Counter Division Ratio	Xtal.clock Frequency (MHz) 4.0	4.032 Sampling Rate kbps	4.096
0 1 1	256	15.625	15.75	16.0
1 0 0	160	25.0	25.20	25.60
1 0 1	128	31.25	31.50	32.0
1 1 0	80	50.0	50.4	51.20
1 1 1	64	62.50	63.0	64.0

Table 3 - Sampling Clock Rates Available

With respect to using a single Xtal/clock frequency for all DBS 800 devices in use, it should be noted that

(a) a 4.032MHz Xtal/clock input will produce an accurate 1200-baud rate for the MX809 MSK Modem.

(b) a 4.096MHz Xtal/clock input will generate exactly 16kbps, 32kbps and 64kbps Codec sampling clock rates.

"Write to Control Register" - Address/Command 60_H, followed by 2 bytes of Command Data

Setting	Function
Byte 1	***First Byte for Transmission***
(MSB) Bit 7	Not used - Set to "0"
6	**Direct Access**
1	-- Encoder Data out to A0/ENO -- Encoder Clock to A3/ECK -- Decoder Input from A1/DEI -- Decoder Clock from A2/DCK
0	Normal DVSR Operation
5	**Play Counter**
1	Decrement
0	Increment
4	**DRAM Control**
1	Disable DRAM
0	Enable DRAM
3	**Codec Powersave**
1	Powersave MX802
0	MX802 Enable
2	**Store Command Interrupt**
1	Enable Interrupt
0	Disable
1	**Play Command Interrupt**
1	Enable Interrupt
0	Disable
0	**Power Reading Interrupt**
1	Enable Interrupt
0	Disable
Byte 0	***Last Byte for Transmission***
(MSB) ***7 6***	**Store/Play Speech Sync.**
0 0	No Sync
0 1	No Sync
1 0	Sync - Play after Store
1 1	Sync - Store after Play
5 4 3	**Decoder Control**
0 0 0	Idle (32kbps); Aud O/P from LPF
0 0 1	Idle (32kbps); Aud bypass
0 1 0	Idle (32kbps); Aud O/P at high Z
0 1 1	On - Sampling Rate 16kbps
1 0 0	On - 25kbps
1 0 1	On - 32kbps
1 1 0	On - 50kbps
1 1 1	On - 64kbps
2 1 0	**Encoder Control**
0 0 0	I/P at V_{BIAS}; F/Idle (32kbps)
0 0 1	I/P at high Z; F/Idle (32kbps)
0 1 0	I/P at high Z; F/Idle (32kbps)
0 1 1	On - Sampling Rate 16kbps
1 0 0	On - 25kbps
1 0 1	On - 32kbps
1 1 0	On - 50kbps
1 1 1	On - 64kbps

Table 4 - Control Register

General Reset

Upon power-up the bits in the MX802 registers will be random (either 0 or 1). A General Reset Command (01_H) will be required to reset all devices on the C-BUS. It has the following effect on the MX802:

Control Register	Set to 00_H
Status Register	Set to 00_H
Clear Store and Play Command Bufers	

Direct Access

External circuitry is allowed direct access to the Delta Codec data and sampling clocks, disabling the DRAM timing circuitry. This permits the Delta Codec section of the MX802 to be used as a Delta Modulation voice encoder and decoder.

Input audio is encoded and made available at the Encoder Out (ENO) pin. Speech data input to the Decoder In (DEI) pin is decoded to give voice-band audio at the Audio Output.

Analog output switching remains under the control of the Control Register, but the decoder sampling clock rate (8kbps to 64kbps) must be provided from an external source to the Decoder Clock (DCK) pin. To ensure correct filter setting, Decoder Control bits (byte 0, bits 5, 4, 3) should be set to binary 1,1,1, where the required rate approximates to a multiple of 25kbps.

Both the encoder internal sampling clock rate and input switching (Table 5) remain under the control of the Control Register. The encoder internal sampling clock rate is available to external circuitry at the Encoder Clock Out (ECK) pin.

Play Counter

The Play Counter direction may be set to run backward as well as forward. This can be used in a scrambling system by replaying speech data in reverse order.

DRAM Control

A logic "1" will disable the DRAM Control Timing circuits and associated counters. The C-BUS Interface, Clock Generator, Delta Codec and filters remain active. This bit should be set to logic "1" when the MX802 is used in the Direct Access Mode.

Minimum DVSR Codec power consumption is achieved by setting both DRAM Control and Powersave bits to logic "1."

Codec Powersave

A logic "1" puts the Delta Codec and filters into Powersave Mode with V_{BIAS} maintained. The Clock Generator, C-BUS Interface, and DRAM Control and Timing remain active.

Command Interrupt Enable

A logic "1" set at the relevant bit will enable Interrupt Requests to the microcontroller when that command operation is complete.

Store and Play Speech Synchronization

This is intended primarily for Time Domain Scrambling.

Decoder and Encoder Control

This individually sets decoder and encoder sampling clock rates, as well as the source of the audio output.

Encoder and Decoder Control: Analog Input and Output Switching

The Control Register, Byte 0: bits 0 to 5, are used together with the codec Powersave Bit (Byte 1: bit 3) to control codec input/output conditions and sample rates. Figure 3 shows the codec functional situation.

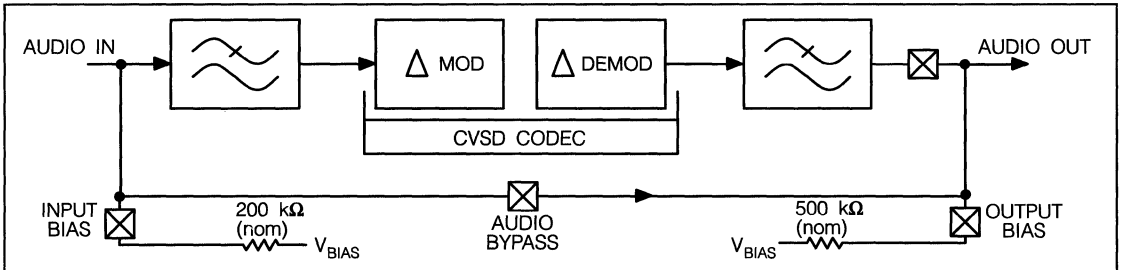


Figure 3 - Analog Control (with reference to Figure 1)

CONTROL REGISTER				CIRCUIT SWITCHES				
Codec Powersave Bit	Decoder Control 5	4	3	Audio Bypass	Audio Out	Output Bias	*OFF = Switch Open ON = Switch Closed*	Note
0	0	0	0	OFF	ON	OFF	Decoder idling fed with "1010101..." pattern at 32 kbps	1
0	0	0	1	ON	OFF	OFF		
0	0	1	0	OFF	OFF	OFF		
0	0	1	1	OFF	ON	OFF	Decoder running at the selected sampling rate	1
-	-	-	-	-	-	-		
0	1	1	1	OFF	ON	OFF		
1	0	0	0	OFF	OFF	ON	Decoder circuits powersaved	
1	0	0	1	ON	OFF	OFF		
1	0	1	0	OFF	OFF	ON		
1	0	1	1	OFF	OFF	ON		
-	-	-	-	-	-	-		
1	1	1	1	OFF	OFF	ON		
	Encoder Control 2	1	0	Input Bias				2
0	0	0	0	ON			Encoder running at 32 kbps but Encoder Data O/P forced to idle pattern "01010..."	
0	0	0	1	OFF				
0	0	1	0	OFF				
0	0	1	1	OFF			Encoder running at selected sampling rate	
-	-	-	-	-				
0	1	1	1	OFF				
1	0	0	0	ON			Encoder circuits powersaved	
-	-	-	-	-				
1	1	1	1	ON				

Table 5 - Analog Control (refer to Figure 3)

Notes

1. If the Delta Codec is in the Direct Access mode, these sampling rates will be as provided by the externally applied clock.
2. The input bias switch is operated by the Control Register Codec Powersave and Encoder Control bits to provide a relatively low impedance path for V_{BIAS} to charge the input coupling capacitor whenever the codec is powersaved, or the encoder control bits are set to 0, so that input bias can be established quickly prior to operation.

Time Compression of Speech

The 25 kbps and 50 kbps sampling rate options are provided for time compression and subsequent expansion of speech signals.

For example, 1.0 seconds of speech stored at 50 kbps may be transmitted in 0.8 seconds if played out at 64 kbps, and finally restored to its original speed at the receiver by storing at 64 kbps and playing out at 50 kbps. A similar result (with a degraded SINAD) may be achieved by using 25 kbps and 32 kbps sampling rates.

However, the speech frequencies are raised by time compression, and since the signal transmitted to air must be band limited to 3400 Hz, the effective end-to-end bandwidth is 0.8 x 3400 Hz, which is approximately 2700 Hz.

"Read Status Register" - Address/Command 61_H, followed by 1 byte of Reply Data

Reading					Function	
MSB Bit 7					**Power Reading** Ready	
1						
6					**Store Command** Complete	
1						
5					**Play Command** Complete	
1						
					Power Register	
4	3	2	1	0	Pwr	Compand Bits/pg.
0	0	0	0	0		0
0	0	0	0	1		1
0	0	0	1	0		2
0	0	0	1	1		3
0	0	1	0	0		4
0	0	1	0	0		5
0	0	1	1	0		6
0	0	1	1	1		7
0	1	0	0	0	-39.0 dB	8
0	1	0	0	1		10
0	1	0	1	0	-36.0	12
0	1	0	1	1		14
0	1	1	0	0	-33.5	16
0	1	1	0	1		18
0	1	1	1	0	-30.0	20
0	1	1	1	1		22
1	0	0	0	0	-28.0	24
1	0	0	0	1		32
1	0	0	1	0	-25.0	40
1	0	0	1	1		48
1	0	1	0	0	-22.0	56
1	0	1	0	1		64
1	0	1	1	0	-19.0	72
1	0	1	1	1		80
1	1	0	0	0	-16.0	88
1	1	0	0	1		128
1	1	0	1	0	-10.0	192
1	1	0	1	1		256
1	1	1	0	0	-6.0	320
1	1	1	0	1		384
1	1	1	1	0	0 dB	448
1	1	1	1	1		512

Table 6 - Status Register

Interrupts

If enabled by the Control Register, an Interrupt Request ($\overline{IRQ}$), is produced by the MX802 to report the following actions:

Power Reading Ready
Store Command Complete
Play Command Complete

When an Interrupt is produced, the Status Register must be read to determine the source of the interrupt. This action will clear the $\overline{IRQ}$ output.

The **Store Command Complete** bit (and an interrupt) is set on completion of a Store Command. This bit is cleared by loading the next Store Command, or by a General Reset Command (01_H).

The **Play Command Complete** bit (and an interrupt) is set on completion of a Play Command. This bit is cleared by loading the next Play Command, or by a General Reset Command (01_H).

The **Power Reading Ready** bit (and an interrupt) is set for every 1024 voice-data bits (1 page) from the Encoder. This bit is cleared after reading the Status Register, or by a General Reset Command (01_H).

Power Register

The power assessment element shown in Figure 1 assesses the input signal power for each encoded "page" (every 1024 encoder output bits) by counting the number of "compand bits" (000 or 111 sequences in the output bit stream) produced during that page (see Table 6) with typical encoder input power levels (dB).

At the end of each "page" the power reading ready bit of the status register is set, and an interrupt request is generated (if enabled). The resulting count is converted to a 5-bit quasi-logarithmic form. The Power Register reading is interpreted as follows:

00000 represents 0 compand bits
00001 represents 1 compand bit
11111 represents 512 compand bits, the maximum.

This power reading is placed in the status register to be read by the microcontroller. Figure 4 shows this output, indicating the input power level.

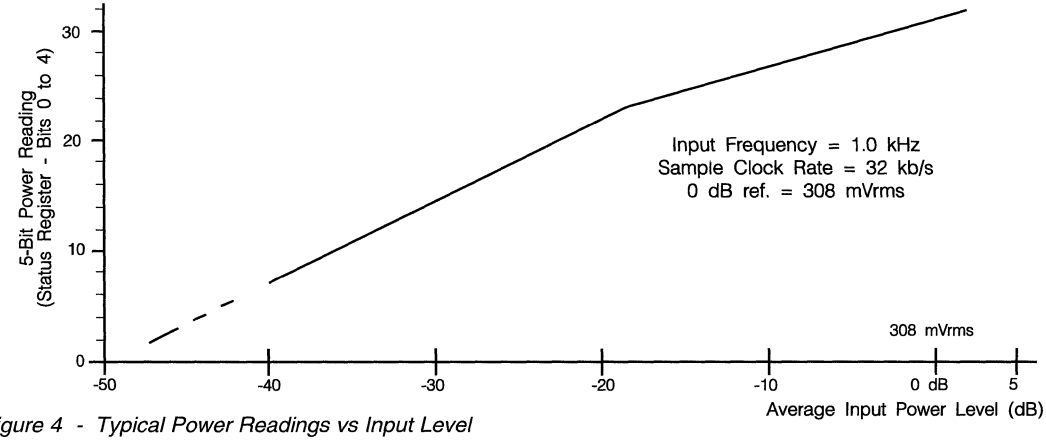


Figure 4 - Typical Power Readings vs Input Level

Timing Information

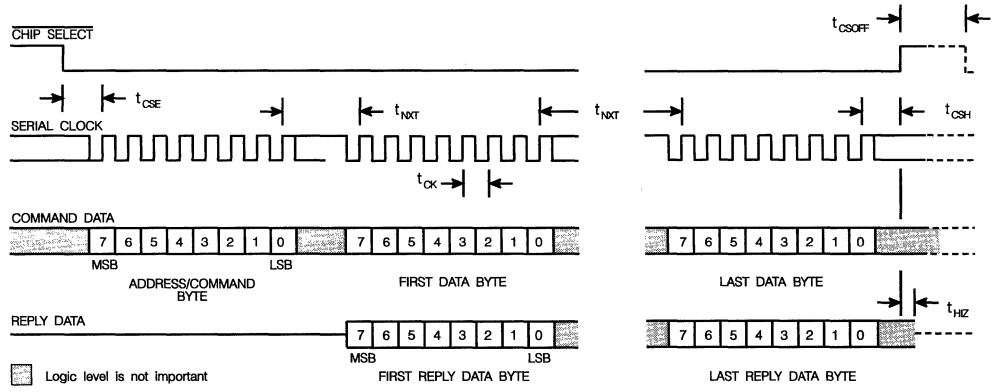


Figure 5 - C-BUS Timing Information

C-BUS Timing (Figure 5)		Min. a	Min. b	Min. c	Max.	Unit
t_{CSE}	Chip Select Low to First Serial Clock Rising Edge	2.0	4.0	8.0	-	µs
t_{CSH}	Last Serial Clock Rising Edge to Chip Select High	4.0	4.0	8.0	-	µs
t_{HIZ}	Chip Select High to Reply Data High - Z	-	-	-	2.0	µs
t_{CSOFF}	Chip Select High	2.0	4.0	8.0	-	µs
t_{NXT}	Command Data Inter-Byte Time	4.0	8.0	16.0	-	µs
t_{CK}	Serial Clock Period	2.0	4.0	8.0	-	µs

Direct Address Timing (Figure 6)		Min.	Typ.	Max.	Unit
t_{CH}	Decoder or Encoder Clock High	1.0	-	-	µs
t_{CL}	Decoder or Encoder Clock Low	1.0	-	-	µs
t_{SU}	Decoder Data Set Up Time	.45	-	-	µs
t_{H}	Decoder Data Hold Time	.60	-	-	µs
t_{PCO}	Encoder Clock High to Encoder Data Valid	-	-	.75	µs
$t_{SU}+t_{H}$	= Data True Time				

6

Notes

1. Minimum Timing Values
   (a) For all commands except "Read Data" and "Write Data" commands.
   (b) For "Read Data" and "Write Data" commands when *no* "Speech Store" or "Speech Play" commands are active.
   (c) For "Read Data" and "Write Data" commands when "Speech Store" or "Speech Play" commands are active.
2. Depending on the command, 1 or 2 bytes of Command Data are transmitted to the peripheral MSB (bit7) first, and LSB (bit0) last. Reply data is read from the peripheral MSB (bit7) first, and LSB (bit0) last.
3. To allow for different microcontroller serial interface formats, C-BUS compatible ICs are able to work with either polarity Serial Clock pulses.
4. Data is clocked into and out of the peripheral on the rising Serial Clock edge.
5. Loaded commands are acted upon at the end of each command.

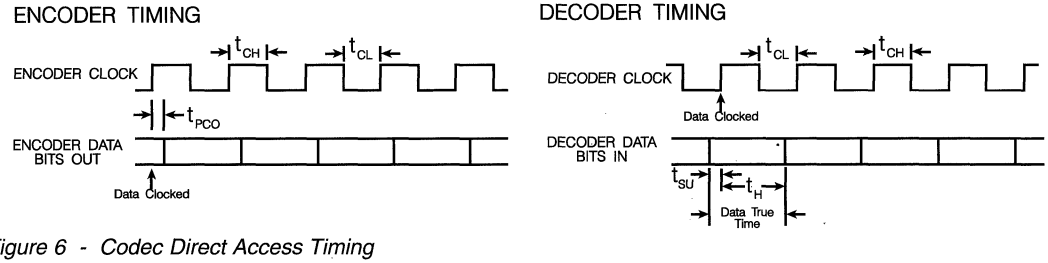


Figure 6 - Codec Direct Access Timing

Codec Performance

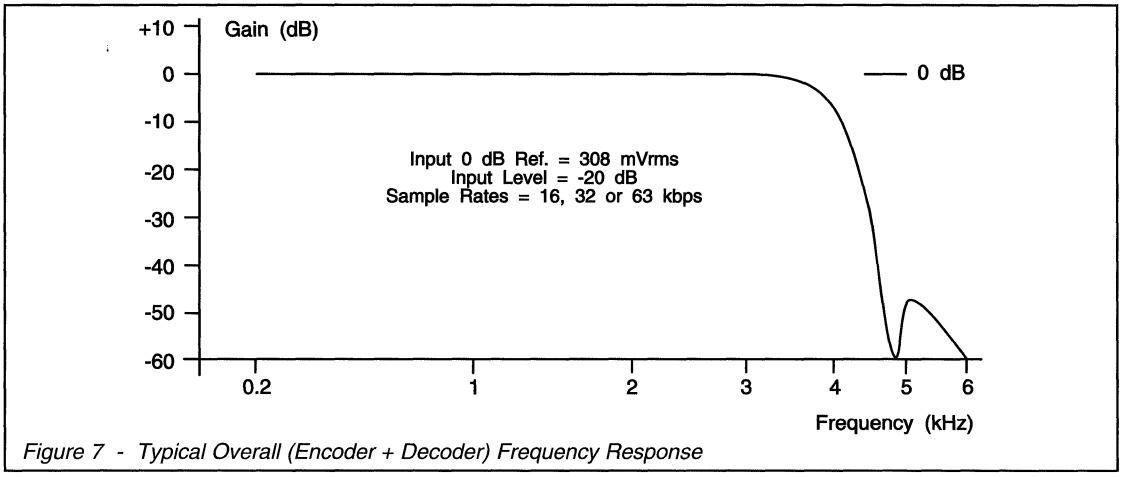


Figure 7 - Typical Overall (Encoder + Decoder) Frequency Response

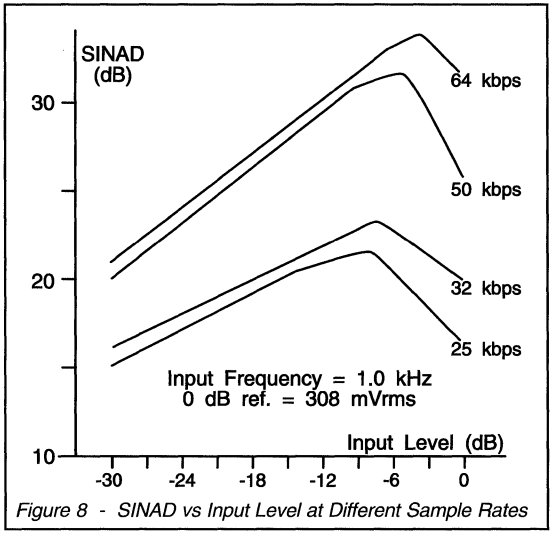


Figure 8 - SINAD vs Input Level at Different Sample Rates

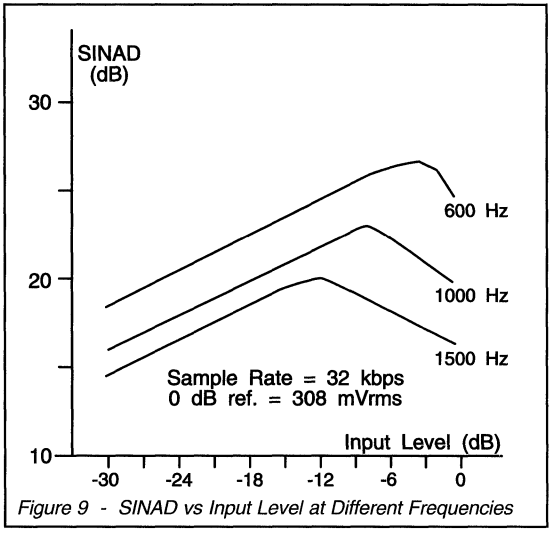


Figure 9 - SINAD vs Input Level at Different Frequencies

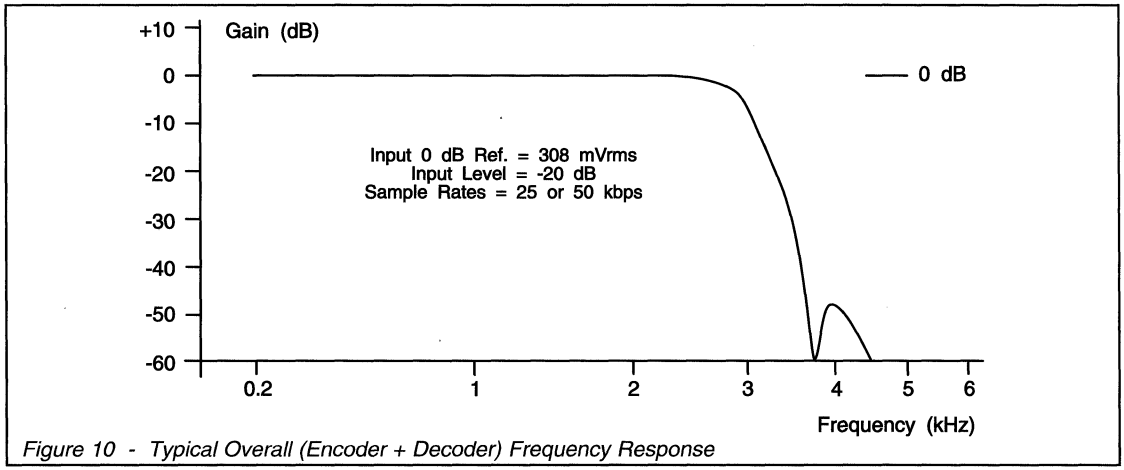


Figure 10 - Typical Overall (Encoder + Decoder) Frequency Response

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin	-0.3V to (V_{DD}+0.3 V)
Sink/source current	
(supply pins)	±30mA
(other pins)	±20mA
Total device dissipation (@T_{AMB} 25°C)	800 mW max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/clock f_0 = 4.0MHz

Audio level 0dB ref = 308 mVrms

Standard test signal f_0 = 820Hz

Sample Rate = 31.25kbps

Characteristics

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD})		4.5	5.0	5.5	V
Supply current (enabled)	1	-	7.0	10.0	mA
Supply current (powersave)	1	-	2.0	4.0	mA
Digital Interface					
Input Logic "1"	2	3.5	-	-	V
Input Logic "0"	2	-	-	1.5	V
Output Logic "1" at IOH = -120mA	7	4.6	-	-	V
at IOH = -50mA	3	4.6	-	-	V
at IOH = 20mA	9	4.6	-	-	V
Output Logic "0" at IOL = 20mA	9	-	-	0.4	V
at IOL = 100mA	3	-	-	0.4	V
at IOL = 360mA	7,8	-	-	0.4	V
Digital Input Current					
V_{IN} = Logic "1" or "0"	2	-	-	1.0	µA
Leakage Current into $\overline{IRQ}$ "OFF" Output	4	-	-	4.0	µA
Digital Input Capacitance	2	-	-	7.5	pF
Analog Impedance					
Input Impedance	12	-	500	-	kΩ
Output Impedance		-	1.5	-	kΩ
Dynamic Values					
Encoder					
Analog Signal Input Levels	5	-24.0	-	4.0	dB
Passband	10,11	-	3400	-	Hz
Decoder					
Analog Signal Output Levels	5	-24.0	-	4.0	dB
Passband	10,11	300	-	3400	Hz
Encoder/Decoder (Full Codec)					
Passband	10,11	300	-	3400	Hz
Passband Gain	11	-	0	-	dB
Passband Ripple	11	-3.0	-	3.0	dB
Stopband		6.0	-	10	kHz
Stopband Attenuation		-	50.0	-	dB
SINAD Level		-	23.0	-	dB
Output Noise (Input short circuit)		-	-50	-	dBp
Idle Channel Noise (Forced)		-	-55	-	dBp
Xtal/clock Frequency	6	-	4.0	-	MHz

Notes
1. Does not include current drawn by any attached DRAM.
2. Serial Clock, Command Data, Chip Select, A1/DEI and A2/DCK inputs.
3. $\overline{CAS}$, $\overline{WE}$ and A0 to A9 outputs.
4. When the $\overline{IRQ}$ outuput is at V_{DD}.
5. The optimum range of levels for a good Signal-to Noise ratio.
6. Audio frequency responses will vary with respect to Xtal/clock frequency.
7. Reply Data output.
8. $\overline{IRQ}$ output.
9. RAS output.
10. Passband is reduced to (typically) 2700 Hz when a sample rate of 25 kbps or 50 kbps is used.
11. Measured with a -20dB input level to avoid codec slope-overload.
12. For optimum noise performance this input should be driven from a source impedance of less than 100Ω.

MX•COM, INC.

Preliminary Information

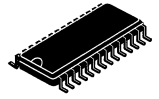
MX812

C-BUS COMPATIBLE

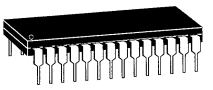
VOICE STORE AND RETRIEVE CODEC

Features and Applications

- **Half-Duplex Voice Storage and Retrieval**
- **Serial Bus µProcessor Control**
- **On-Chip DRAM Controller**
- **Up To 2 Minutes of High-Quality Recorded Audio**
- **Answering Functions and Voice-Notepad**
- **Low-Power 5-Volt CMOS**
- **Selectable Sample Rates and "Memory Size"**



MX812DW
28-pin SOIC



MX812J
28-pin CDIP

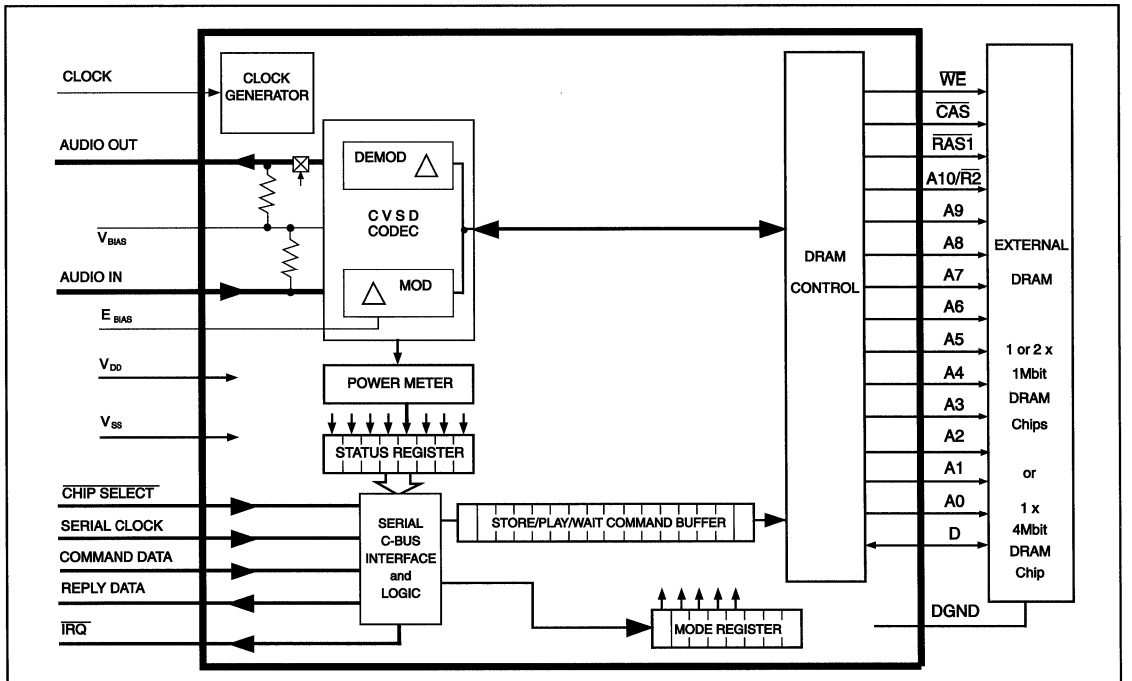


Figure 1 - MX812 Voice Store and Retrieve Codec

DESCRIPTION

The MX812 is a half-duplex VSR Codec, which when connected to an audio processing microcircuit (such as the MX816, 826 or 836), provides the storage and recovery of speechband audio in attached Dynamic RAM. The addition of this device will enhance the communications system by providing cellular radios with Answering Functions, "Message-Notepad" and general announcement cababilities.

The MX812 will enable:

- Storage of a speech message for transmission (replay) at a later time.
- Storage of a received speech message when the operator is not attending.
- The storage and subsequent replay of speech.

All VSR operating functions are controlled by a simple serial µProcessor interface which may operate from the radio's own µProcessor/Controller.

Input audio from the "Store" output of the audio processor is digitized by delta modulation and stored via the DRAM controller, in attached memory.

Audio for replay is recovered from the assigned memory locations and after demodulation made available for supply to the "Play" input of the audio processor. For use with other audio systems, the input/output audio can be connected to relevant points in circuit.

The MX812 has no on-chip input or output audio filtering; this capability must therefore be provided by the host system. Sampling rates and memory capacity are selectable to 32kb/s or 63kb/s and 1 x 4Mbit or 2 x 1Mbit respectively, which when used in conjunction allow control of audio-quality and storage-time.

This low-power CMOS device is available 28-pin plastic SOIC and 28-pin Cerdip packages.

Pin	Function
1	**$\overline{\text{CAS}}$:** This output should be connected to the "Column Address Strobe" input pin(s) of all DRAM devices installed.
2	**$\overline{\text{WE}}$:** This output should be connected to the "Write Enable" input pin(s) of all DRAM devices installed.
3	**D:** Digital (speech) data into and out of the VSR Codec. This pin should be connected to the "Data In" and "Data Out" pins ("D" and "Q") of DRAM devices.
4	**Xtal:** The nominal 4.0MHz clock input to the VSR Codec. The signal applied to this device may be derived from the attached Audio Processor on-chip Xtal Oscillator circuits (see Figures 2 and 3). **Note** that the VSR Codec will be able to function and maintain correct DRAM refresh, with Xtal input frequencies down to 2.0MHz. Compand and Local Decoder time constants will change accordingly and minimum "C-BUS" timings (Figures 6 and 7) would have to be increased pro-rata.
5	**Interrupt Request ($\overline{\text{IRQ}}$):** This Interrupt Request output from the MX812 is 'wire-OR able' allowing the Interrupt Outputs of other peripherals to be commoned and connected to the Interrupt input of the µProcessor (see the C-BUS Interface and System Applications document). This input has a low-impedance pulldown to V_{SS} when active, and a high-impedance when inactive.
6	**Serial Clock:** The C-BUS serial clock input. This clock produced by the µController, is used for transfer timing of commands and data to and from the VSR Codec. See Timing Diagrams.
7	**Command Data:** The C-BUS serial (command) data input from the µController. Data is loaded to this device in 8-bit bytes MSB (B7) first and LSB (B0) last, synchronized to the Serial Clock.
8	**Chip Select ($\overline{\text{CS}}$):** The C-BUS data transfer control function. This input is provided by the µController. Transfer sequences are initiated, completed or aborted by this signal. See Timing Diagrams.
9	**Reply Data:** The C-BUS serial data output to the µController. The transmission of reply bytes is synchronized to the Serial Clock under the control of the Chip Select input. This is a 3-state output which is held at a high-impedance when not sending data to the µController.
10	**V_{BIAS}:** The output of the internal analog circuitry bias line, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C_2 (see Figure 2).

Pin	Function
11	**Audio Out:** The analog output to the Audio Processor "Play" input when the VSR Codec is configured as a Decoder. When configured as an active Decoder but with no Play Page commands (62_H) active, the VSR Codec will play-out an idle pattern of "101010.....10^s". When not configured as a Decoder, or Powersaved (Mode Register), this output will be held at V_{BIAS} via an internal 500kΩ resistor. The output at this pin is unfiltered; an external speechband filter – such as that included on the MX816/826/836 Audio Processors – will be required. Since this output is centered around $V_{DD}/2$ a coupling capacitor is required.
12	**E_{BIAS}:** The Encoder d.c. internal balancing circuitry line. This pin should be decoupled to V_{SS} by capacitor C_4 (see Figure 2). **Note** that in the 'Encode' mode (Mode Register DE and PS both "0") the Codec drives this pin to approximately $V_{DD}/2$ through a very high impedance; it can take more than one second for the E_{BIAS} voltage to stabilize when power is first applied to this device. A faster start-up can be achieved by setting Bit DE or PS to "1" for 250mS (approx) during power-up. This will cause the E_{BIAS} pin to be connected to V_{BIAS} through a resistance of approximately 100kΩ.
13	**Audio In:** The analog input to the VSR Codec in the Encode mode. When not configured as an Encoder, or Powersaved (Mode Register), this input will be held at V_{BIAS} via an internal 500kΩ resistor. This pin should be coupled via a capacitor, see Figure 2. As this input does not contain an internal audio filter, the audio to this pin should be limited to a 3400Hz "speechband" by an external audio filter – such as included in the MX816/826/836 Audio Processors.
14	**V_{SS}:** The "analog" ground connection. See D_{GND} description.
15	**A0:**
16	**A1:**
17	**A2:**
18	**A3:**
19	**A4:** — DRAM address line outputs from the MX812. These pins should be connected to the corresponding address inputs of the associated DRAM.
20	**A5:**
21	**A6:**
22	**A7:**
23	**A8:**
24	**A9:**
25	**A10/$\overline{R2}$:** A dual function output pin selected by the memory size (MS) bit (Mode Register), as detailed in the table below:
26	**$\overline{RAS}$:** An output from the VSR Codec which should be connected to the "Row Address Strobe" pin of the 4Mbit DRAM or the first 1Mbit DRAM, see Figure 4, Example DRAM connections.
27	**D_{GND}:** The digital signal ground connection to the VSR Codec. Both D_{GND} and V_{SS} pins should be connected to the negative side of the d.c. power supply. However, a printed circuit board should be laid out so that D_{GND} is connected as closely as possible to the DRAM section ground pins.
28	**V_{DD}:** Positive supply rail. A single, stable +5-volt supply is required. Levels and voltages within the VSR Codec are dependent upon this supply. This pin should be decoupled to V_{SS} via capacitor C_5, located close to the MX812 pins.

MS bit	DRAMs	Connected To	This Output
"0"	1Mbits'	DRAM No 2 $\overline{RAS}$	RAS2
"1"	4Mbit	DRAM A10	A10 Signal

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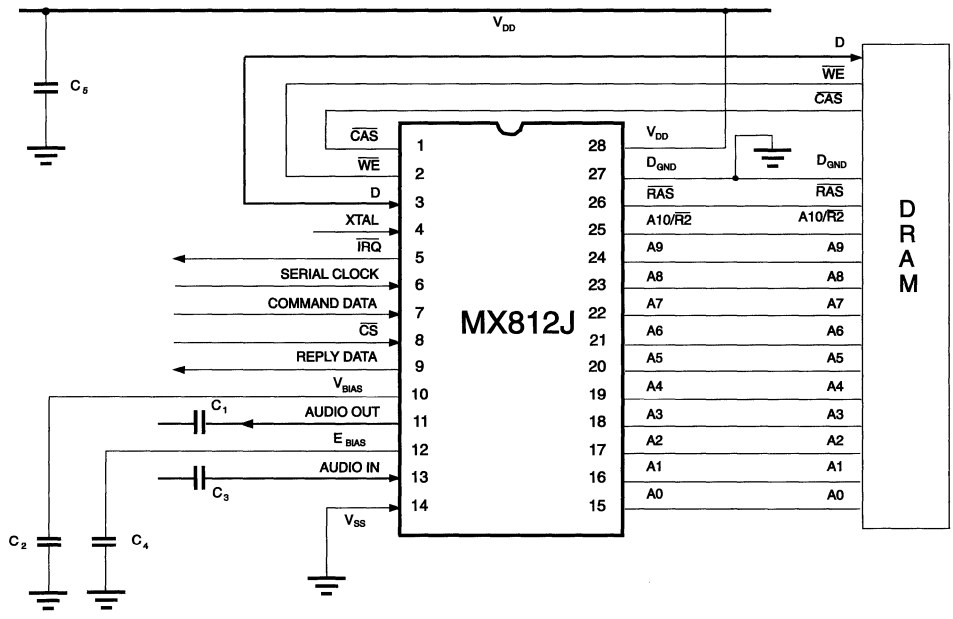
Application Information



Component	Value
C_1	Dependent upon the input impedance of the driven stage
C_2	1.0µF
C_3	0.1µF
C_4	1.0µF non-electrolytic

Tolerance: Capacitors = -50/+100%

Figure 2 - Recommended External Components

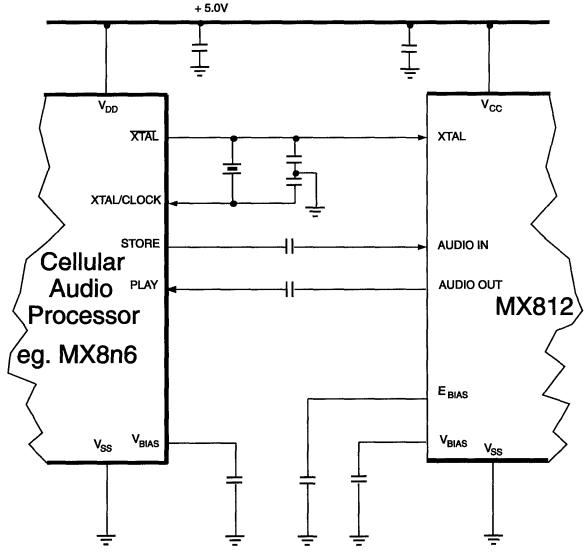


Figure 3 - Interfacing to an Audio Processor

Application Information .....

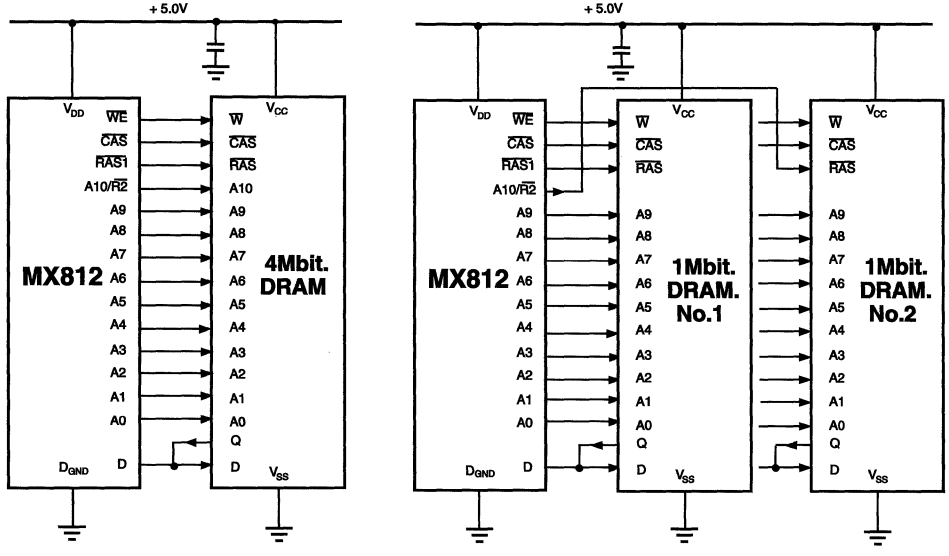


Figure 4 - Example DRAM Connections

Choice of DRAM Devices

DRAM devices chosen should be standard 1,048,576 x 1 or 4,194,304 x 1 Dynamic Random Access memories, with 'CAS before RAS' refresh, and a Row Address access time of 200 nano-seconds or less.

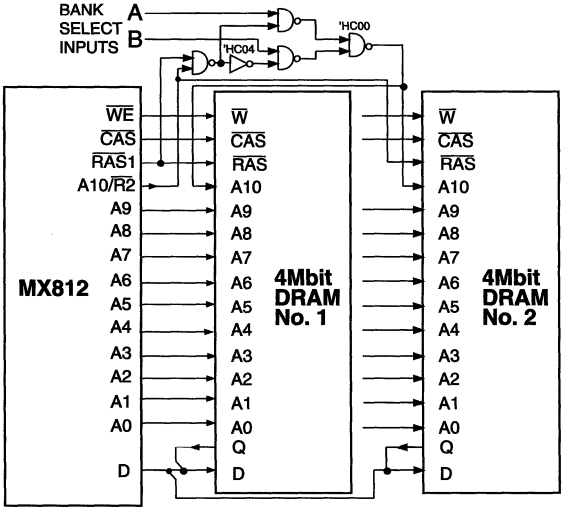


Figure 5 - Use of External Elements to Drive Two 4-MBit DRAM Chips

Driving Two 4-MBit DRAM Sections

By adding external logic circuitry, the MX812 can be configured to drive two 4-MBit DRAM sections. This will have the effect of doubling the available storage time. i.e. 4 minutes at 32kbps.

With reference to the circuitry shown in Figure 5: With the Mode Register **MS** Bit set to "0" the MX812 treats the DRAM sections as two 1-Mbit devices. The external logic makes each 4-MBit DRAM appear as four 1-MBit banks selected by the Bank Select lines '**A**' and '**B**.'

Bank Select Inputs A	B	DRAM No 1 Pages 0 – 1023	DRAM No 2 Pages 1024 – 2047
0	0	■	■
1	0	■	■
0	1	■	■
1	1	■	■

The Controlling System: C-BUS Hardware Interface

C-BUS is MX-COM's proprietary standard for the transmission of commands and data between a µController and MX-COM's New Generation integrated circuits. C-BUS is designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer can choose a µController appropriate to the overall system processing requirements.

Control of the functions and levels within the MX812 VSR Codec is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the MX812. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB							LSB	+	Data Byte/s
General Reset	01	0	0	0	0	0	0	0	1		
Write to Mode Register	60	0	1	1	0	0	0	0	0	+	1 byte Instruction to Mode Register
Read Status Register	61	0	1	1	0	0	0	0	1	+	1 byte Reply from Status Register
Store/Play Page	62	0	1	1	0	0	0	1	0	+	2 bytes Command
Wait	63	0	1	1	0	0	0	1	1		

Table 1 – C-BUS Address/Commands

"Write to Mode Register"

– A/C 60_H, followed by 1 byte of Command Data.

Interrupt Output – IE

Controls the MX812 IRQ output driver.

Sampling Rates – SR

The CVSD Codec sampling rates. Accurate rates depend upon the applied Xtal/clock frequency (see Table 5).

Memory Size – MS

The MX812 can operate with 1 x 1Mbit, 2 x 1Mbit or 1 x 4Mbit of DRAM (see Figure 4).

Powersave – PS

Powersaves the CVSD Codec only. Logic functions and DRAM refresh are maintained.

Decode/Encode – DE

The Codec and DRAM operational mode."
"Play" or "Store"

Setting	*Mode Bits*
MSB	***Transmitted to 812 First***
7	**Interrupt Output**
1	Enable
0	Disable
6	**Sampling Rate**
1	63kb/s
0	32kb/s
5	**Memory (DRAM) Size**
1	Single 4Mbit
0	1 or 2 x 1Mbit
4	**Powersave**
1	CVSD Codec Powersaved
0	CVSD Codec Powered
3	**Decode/Encode**
1	Decode – Play Mode
0	Encode – Store Mode
2 1 0	**Not Used**
0 0 0	Set to 'zeros'

Table 2 - Control Register

Interrupts

The MX812's Interrupt Output is driven by the Status Bit 7 (IF) when the Mode Register Bit7 (IE) is set to a "1."

The IF bit and the Interrupt Output (If enabled) are set when the Store/Play/Wait command Buffer is emptied (MT bit) by transferring from the buffer to the DRAM control circuits.

and/or

The IF bit and the Interrupt Output (if enabled) are set when a Store, Play or Wait command has finished **and** the Command Buffer is empty.

The notes below illustrate the $\overline{IRQ}$ pin conditions:

IF Bit	IE Bit	$\overline{IRQ}$
"0" cleared	"0" disable	High Z
"0" cleared	"1" enable	High Z
"1" Interrupt	"0" disable	High Z
"1" Interrupt	"1" enable	V_{SS} (logic "0")

"General Reset" – A/C 01_H

Upon Power-Up the "bits" in the MX812 registers will be random (either "0" or "1"). A General Reset Command (01_H) will be required to "reset" all microcircuits on the C-BUS, and has the following effect upon the MX812.

Clear all Mode Register bits to "0"

Status Register Bit 7 (IF) to "0"

Bits 5 and 6 (MT and I) to "1"

Halt any current Store, Play or Wait execution

Clear the Store/Play/Wait Command Buffer

6

The Controlling System .....

"Read Status Register" – A/C 61_H, followed by 1 byte of Reply Data.

Reading	*Status Bits*
MSB	*Received from 812 First*
7	**Interrupt Condition (Flag)**
1	Bit 6 or 5 set to a "1"
0	Cleared condition
6	**Command Buffer**
1	Buffer Empty
0	Cleared condition
5	**Device Condition**
1	Idle
0	Storing, Playing or Waiting
4 3 2 1 0	**Input Power Level**

Table 3 Status Register

Interrupt Condition (Flag) – IF
Set to a logic "1" whenever Bit 6 or Bit 5 goes from "0" to "1" (unless the transition is caused by a General Reset command 01_H). This indication allows monitoring by 'poll' while Interrupts are disabled.
Cleared to a logic "0" by a General Reset command or immediately following a read of the Status Register.

Command Buffer Status – MT
Set to a logic "1" when the Command Buffer is empty or by a General Reset command.
Cleared to a logic "0" by loading a new Store, Play, Wait commands.

Device Condition – I
Set to a logic "1" when **NO** Store, Play or Wait command is being executed or by a General Reset command.
Set to a logic "0" while a Store, Play or Wait command is being executed.

Encode Input Power Level – POWER
Available in the Encode mode, a 5-bit representation of the analog signal input level, updated at the end of every Store or Wait command.

Store/Play/Wait Command Buffer

A buffer used to accept and hold the latest Store, Play or Wait command received over the C-BUS while the MX812 is executing the previous command. The Status Register, bit 6, indicates the condition of this buffer.

When a command is received it is first loaded into this buffer. If the MX812 is already executing a previously loaded Store, Play or Wait command the new command will be stored temporarily in the Command Buffer, from where it will be taken on completion of the previous command.

This permits the MX812 to perform a continuous sequence of Store, Play or Wait commands, without gaps and without requiring an unduly fast response from the mController.

Note that this Command Buffer can only hold one Store, Play or Wait instruction, each new command received into this buffer will overwrite any previously loaded contents.

To Store or Play a sequence of pages the relevant commands should be loaded with sequential page numbers while observing the Status Register – Bit 6.

6

"Store/Play Page" – A/C 62_H, followed by 2 bytes of Command Data.

For the purposes of storage and replay, the attatched DRAM is divided into 'data-pages' of 1024 bits (1kbit).

One Store/Play command (loaded MSB first) will instruct the MX812 to store or play (depending upon the setting of the Mode Register, Bit-3) to or from 1 x 1024 "page" of DRAM. The Store/Play/Wait command buffer will allow continuity of operation.

The particular page selected is identified by the 12 lowest bits of the 2 x Store/Play bytes as shown below.

If a Store command is loaded and executed whilst the Codec is "Powersaved" in the Encode mode, the selected DRAM page will be filled with an idle pattern ("101010.....").

					Bit Number												
	MSB – Loaded to MX812 First															*Loaded Last – LSB*	
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Bit**
Value	**x**	**x**	**x**	**x**	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	**Value**
Page	"0"	"0"	"0"	"0"	DRAM Page Number												**Page**

DRAM Size	Valid Page Nos	Bit Nos
4Mbit	0 – 4095	0 – 11
1 + 1Mbit	0 – 2047	0 – 10
1Mbit	0 – 1023	0 – 9

"Wait" – A/C 63_H, — Wait for 1024 bit periods

Causes the MX812 to wait for 1024 bit periods (approximately 16 or 32ms).

If the Codec is set to the Encode mode, a new "Power" reading that is relevant to the input audio level, will be loaded into the Status Register at the end of the Wait period.

If the Codec is set to the Decode mode it will 'Play' a perfect idle pattern ("101010.....") during the Wait period.

Control Timing Information

Figure 6 shows the timing parameters for two-way communication between the µController and Cellular peripherals on the "C-BUS." Figure 7 shows the timing relationships between the Serial Clock and Data.

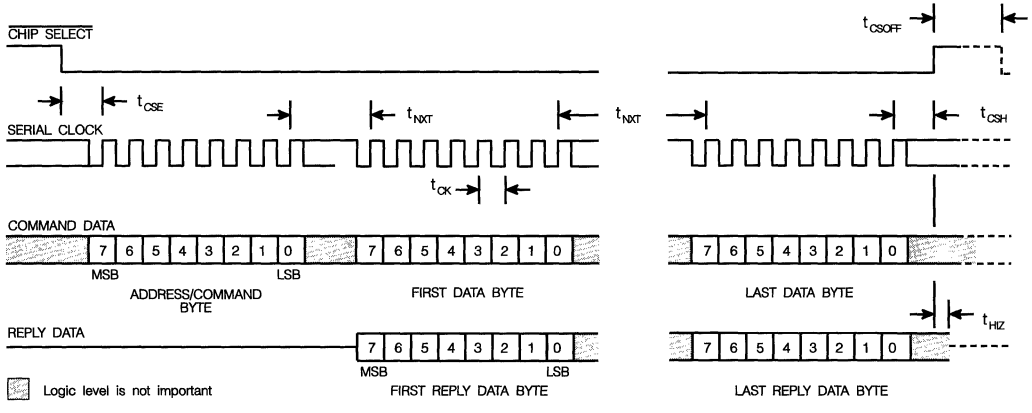


Figure 6 - Control Timing Information

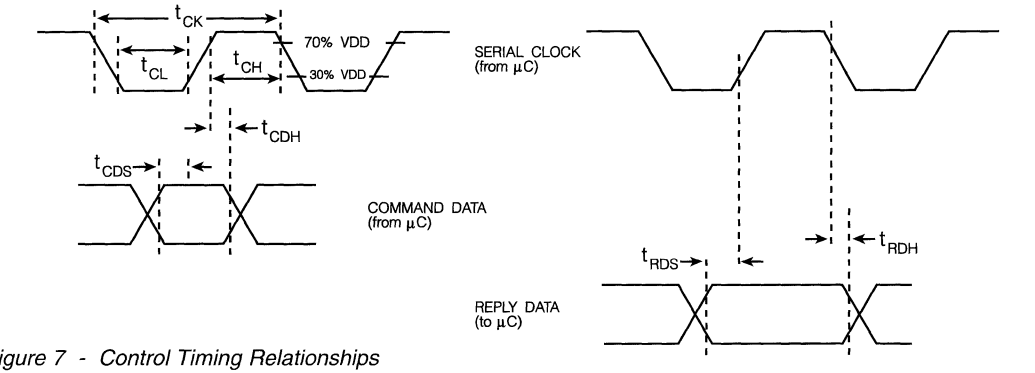


Figure 7 - Control Timing Relationships

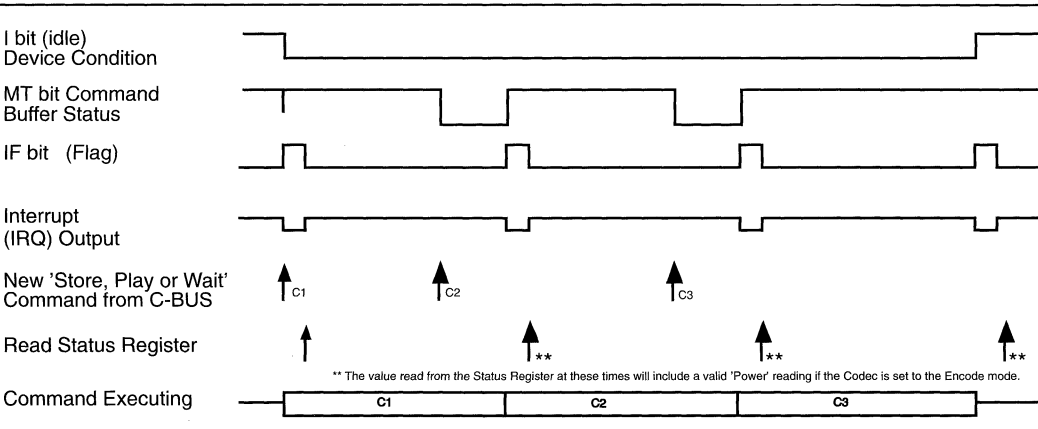


Figure 8 - Typical Command Sequences

6

Control Timing Information .....

Timing Specification – Figures 6 and 7

Characteristics		See Note	Min.	Typ.	Max.	Unit
t_{CSE}	"CS-Enable to Clock-High"		2.0	–	–	µs
t_{CSH}	Last "Clock-High to CS-High"		4.0	–	–	µs
t_{HIZ}	"CS-High to Reply Output Tri-state"		–	–	2.0	µs
t_{CSOFF}	"CS-High" Time between transactions		2.0	–	–	µs
t_{CK}	"Clock-Cycle" Time		2.0	–	–	µs
t_{NXT}	"Inter-Byte" Time		4.0	–	–	µs
t_{CH}	"Serial Clock-High" Period		500	–	–	ns
t_{CL}	"Serial Clock-Low" Period		500	–	–	ns
t_{CDS}	"Command Data Set-Up" Time		250	–	–	ns
t_{CDH}	"Command Data Hold" Time		0	–	–	ns
t_{RDS}	"Reply Data Set-Up" Time		250	–	–	ns
t_{RDH}	"Repy Data Hold" Time		50.0	–	–	ns

Address Line Decoding

MA0 to MA21 are the outputs of the internal 22-bit DRAM address counter, which are time multiplexed as 'Row' and 'Column' addresses onto the DRAM address lines A0 to A10 etc., as shown below.

Memory Size (MS) Bit = "1" – 4Mbit DRAM

Pin	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10/R2
Row Address	MA0	MA2	MA4	MA6	MA8	MA10	MA12	MA14	MA16	MA18	MA20
Column Address	MA1	MA3	MA5	MA7	MA9	MA11	MA13	MA15	MA17	MA19	MA21

Memory Size (MS) Bit = "0" – 1Mbit DRAM(s)

Pin	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9
Row Address	MA0	MA2	MA4	MA6	MA8	MA10	MA12	MA14	MA16	MA18
Column Address	MA1	MA3	MA5	MA7	MA9	MA11	MA13	MA15	MA17	MA19

MA20	MA21	RAS1	A10/R2	DRAM Selected
0	x	active		"first"
1	x		active	"second"

x = don't care

Table 4 Address Line Decoding

Sample Rate (SR) Bit	Division Ratio	Xtal/clock Frequency (MHz) 4.0	4.032	4.096
SR = "1"	64 kbps	62.5 kbps	63 kbps	64 kbps
SR = "0"	128 kbps	31.25 kbps	31.5 kbps	32 kbps
			Internal Clock Rate	
Local Decoder Clock		125 kHz	126 kHz	128 kHz

Table 5 Sampling Clock Rates Available

Performance

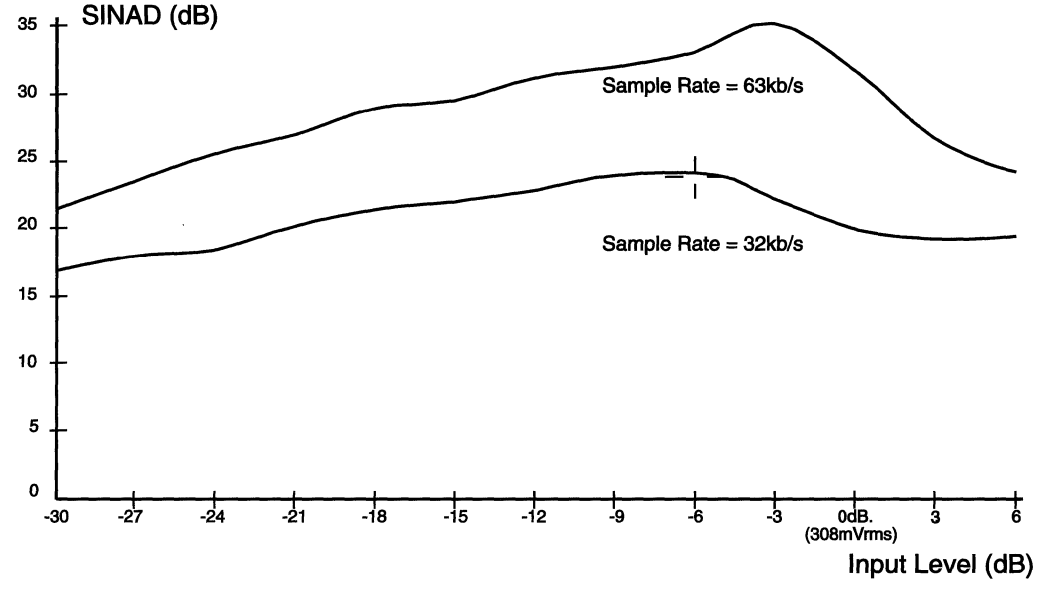


Figure 9 - Typical "SINAD vs Input Level" Plot

Performance

Figure 9 Shows a typical graph of SINAD vs Input Level produced for both 32kbps and 63kbps sample rates at an input frequency of 1.0kHz.

Figure 10 shows a typical graph of the "Power" reading for increasing input signal levels. The "Power" figure (0 to 31) is the binary figure obtained from the 5-bit representation in the Status Register - Bits 0, 1, 2, 3 and 4 while the Codec is selected to the Encode mode.

This reading is updated at the end of every Store or Wait command; Excessive input signal levels will record "11111_2" (31_{10}).

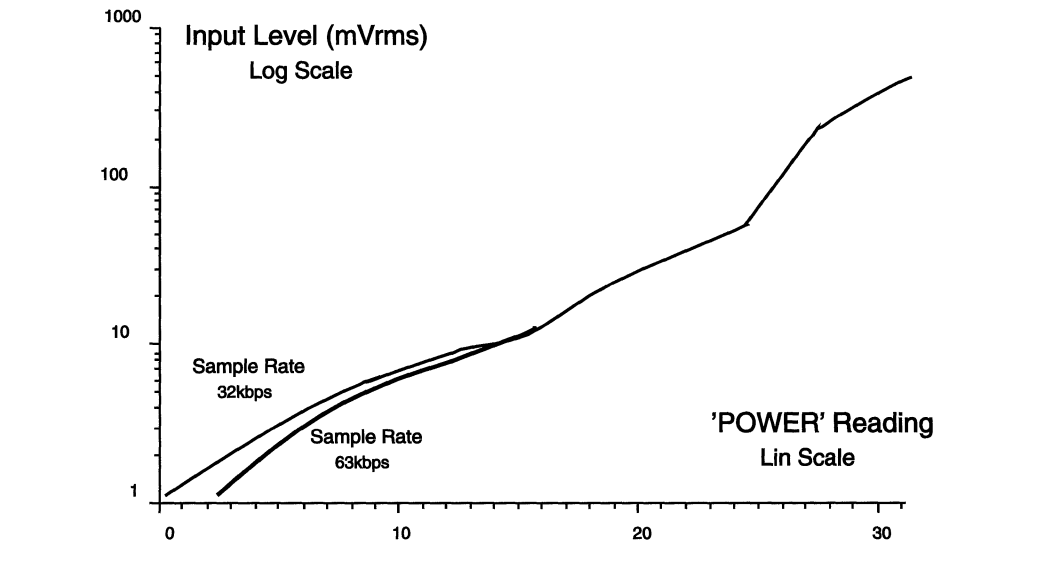


Figure 10 - Typical "Power Reading vs Input Level" Plot

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD}+0.3V)
Sink/source current (supply pins)	±30mA
(other pins)	±20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/Clock f_0 = 4.00MHz

Audio Level 0dB ref = 308mVrms @ 1kHz

Reply Data Line loaded with 50pF/200kΩ to V_{SS}

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
Enabled	1	–	3.0	–	mA
Powersaved	1	–	1.0	–	mA
Analog Input Impedance		–	100	–	kΩ
Analog Output Impedance (Decode)		–	1.0	–	kΩ
Analog Output Impedance (Encode or Powersave)		–	500	–	kΩ
DRAM Interface					
Input Logic "1"	2	3.5	–	–	V
Input Logic "0"	2	–	–	1.5	V
Output Logic "1" (at I_o = -120µA)	3	2.7	–	–	V
Output Logic "0" (at I_o = 120µA)	3	–	–	0.4	V
Input Leakage Current (at V_{IN} = 0 to V_{DD})	4	-1.0	–	1.0	µA
Input Capacitance	2	–	10.0	–	pF
Digital Interface					
Input Logic "1"	5	3.5	–	–	V
Input Logic "0"	5	–	–	1.5	V
I_{IN} (logic "1" or "0")	5	-1.0	–	1.0	µA
Output Logic Levels					
Output Logic "1" (-120µA)	6	4.6	–	–	V
Output Logic "0" (360µA)	7	–	–	0.4	V
I_{Out} Tri-state (logic "1" or "0")	6	-4.0	–	4.0	µA
Input Capacitance	5	–	–	7.5	pF
IOX (V_{Out} = 5V)	8	–	–	4.0	µA

Characteristics	See Note	Min.	Typ.	Max.	Unit
Dynamic Values					
"Xtal" Pin Input Frequency Range	12	4.0		4.1	MHz
Store Mode					
Analog Input Signal Levels	9	-24.0	–	4.0	dB
Analog Input Signal Frequency Range	9, 10	300		3400	Hz
Recommended Signal Source Impedance	9	–	–	2.0	kΩ
Play Mode					
Analog Output Signal Levels	13	-7.0	–	-5.0	dB
Output Noise (idle)	11	–	-55.0	–	dBp
Overall 'Store to Play' Performance					
Output Noise (Input Short Circuit)	11	–	-50.0	–	dBp
SINAD (**SR** = 32kb/s)					
(Input = 1.0kHz @ -6.0dB)	11	–	23.0	–	dB

Notes

1. Not including DRAM current.
2. D input from DRAM
3. Outputs to DRAM.
4. All digital inputs.
5. Serial Clock, Command Data and Chip Select inputs.
6. Reply Data output.
7. Reply Data and Interrupt ($\overline{IRQ}$) outputs.
8. Leakage current into the "Off" Interrupt ($\overline{IRQ}$) output.
9. For optimum performance.
10. Input filtering must be performed at the source.
11. Measured in conjunction with the FX836 R2000 system Audio Processor.
12. For full C-BUS compatibility.
13. Playback of a stored "-6.0dB 1.0kHz Test Signal."

Section 7: Digital Control Amplifiers

The following section contains specifications on MX•COM's devices used for digital control.

Device	Description	Page	
MX009	Octal Digital Control Amplifier	p. 449	
MX019	Quad Digital Control Amplifier	p. 455	
MX029	Dual Digital Control Amplifier	p. 460	**NEW**

MX•COM, INC. MX009

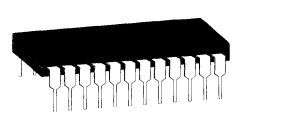
OCTAL DIGITALLY CONTROLLED AMPLIFIER ARRAY

Features

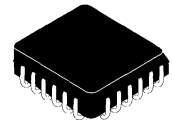
8 Digitally Controlled Amplifiers
15 Gain/Attenuation Steps + Mute
7 Trimmers with a ±3dB Range in 0.43dB Steps
1 "Volume" Control with a ±14dB Range in 2.0 dB Steps
Individual Control with an 8-Bit Serial Word
Output Mute/Powersave Function
Digitally Set Audio Control Levels

Applications

Cellular and LMR Radios, PABX's, Electronic Mail
Automatic Test Equipment, Remote Gain Adjustments



MX009J (CDIP)
MX009P (PDIP)
24 pins



MX009LH
(24 pin PLCC)

Description

The MX009 Digitally Controlled Amplifier Array replaces trimmers and one volume control in radio and wireline communications applications in which voice or data signals need adjusting. The MX009 is a single-chip LSI circuit comprised of eight discrete, digitally controlled amplifiers, each with 15 distinct gain/attenuation steps plus a MUTE. Control of each amplifier is by an 8-bit serial word.

Seven of the amplifiers have a ±3dB range stepped in 15 increments of 0.43dB each. The remaining amplifier has a ±14dB range in 15 steps of 2dB, and is intended for volume control applications. Each digitally controlled amplifier includes a sixteenth "Mute" state which sets the output to bias ($V_{DD}/2$) and powersaves the section addressed. Minimum current drain results from muting all eight sections.

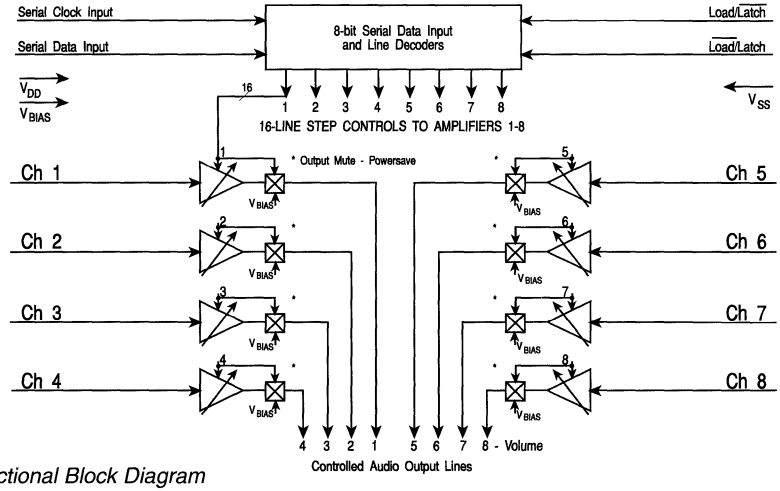
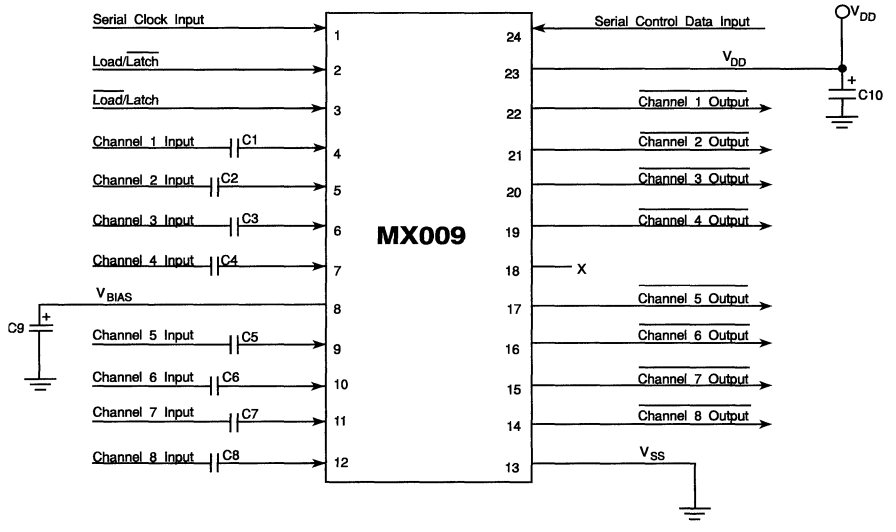


Figure 1 - Functional Block Diagram

Pin Function Table

Pin	Function
1	Serial Clock: This external clock pulse input is used to "clock in" the Control Data. See Figure 4, Data Load timing. This input has an internal 1MΩ pullup resistor.
2	Load/$\overline{\text{Latch}}$: This function governs the loading and execution of the control data. During serial data loading this input should be kept at a logical "0" to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded this input should be strobed "0 -> 1 -> 0" to latch the new data in. Data is executed on the falling edge of the strobe. If the $\overline{\text{Load}}$/Latch input is used this pin should be left open circuit — This input has an internal 1MΩ pullup resistor.
3	$\overline{\text{Load}}$/Latch: This is the inverted Load/Latch input. This function governs the loading and execution of the control data. During serial data loading this input should be kept at a logical "1" to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded this input should be strobed "1 -> 0 -> 1" to latch the new data in. Data is executed on the rising edge of the strobe. If the Load/$\overline{\text{Latch}}$ input is used this pin should be left open circuit — This input has an internal 1MΩ pulldown resistor.
4	Ch 1 Input: Analog Inputs: These individual amplifier inputs are self-biasing; input analog signals must be a.c. coupled to these pins, as shown in Figure 2. In the powersave modes the inputs are biased at $V_{DD}/2$. Ch1 to Ch7 range from -3dB to +3dB in 0.43dB steps. Ch8 could be utilized as a volume control ranging from -15dB to +15dB in 2.0 dB steps.
5	Ch 2 Input:
6	Ch 3 Input:
7	Ch 4 Input:
8	V_{BIAS}: The output of the on-chip bias circuitry, held at $V_{DD}/2$. This pin should be decoupled to V_{ss} as shown in Figure 2.
9	Ch 5 Input: Analog Inputs
10	Ch 6 Input:
11	Ch 7 Input:
12	Ch 8 Input:
13	V_{ss}: Negative supply rail (GND).
14	$\overline{\text{Ch 8}}$ Output: Analog Outputs: These are the individual "Gain Controlled" amplifier outputs.
15	$\overline{\text{Ch 7}}$ Output: Ch1 to Ch7 range from -3dB to +3dB in 0.43dB steps. Ch8 could be
16	$\overline{\text{Ch 6}}$ Output: used as a volume control, ranging from -14dB to +14dB in 2.0dB steps.
17	$\overline{\text{Ch 5}}$ Output: In the powersave modes the selected output is biased at $V_{DD}/2$.
18	No internal connection. Do not use.
19	$\overline{\text{Ch 4}}$ Output: Analog Outputs
20	$\overline{\text{Ch 3}}$ Output:
21	$\overline{\text{Ch 2}}$ Output: Note that amplifiers Ch1 to Ch8
22	$\overline{\text{Ch 1}}$ Output: are "inverting amplifiers."
23	V_{DD}: Positive supply. A single +5-volt power supply is required.
24	Control (Data) Input: Operation of the 8 amplifier channels (Ch1 - Ch8) is controlled by the 8 bits of data entered serially at this pin. The data is entered (bit 7 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Tables 1, 2 and Figure 4. This input has an internal 1MΩ pullup resistor.

Application Notes



Notes

(1) Channel Amplifiers 1 to 8 are inverting amplifiers.

(2) Analog input capacitors C_1 to C_8 are only required for a.c. input signals; d.c. input signals do not require these components.

Component	Unit Value
C_1 to C_8	0.1µF
C_9	1.0µF
C_{10}	1.0µF

Tolerances ± 20%

Fig. 2 - External Component Connections

Application Recommendations

To avoid noise and instability the following practices are recommended:

(a) Use a clean, well-regulated power supply.

(b) Keep leads short.

(c) Inputs and outputs should be shielded wherever possible.

(d) Analog tracks should not run parallel to digital tracks.

(e) A "Ground Plane" connected to V_{ss} will assist in eliminating external pick-up on the channel input and output pins.

(f) Avoid running High Level Outputs adjacent to Low Level Inputs.

(g) Input signal amplitudes should be applied with regard to Figure 3.

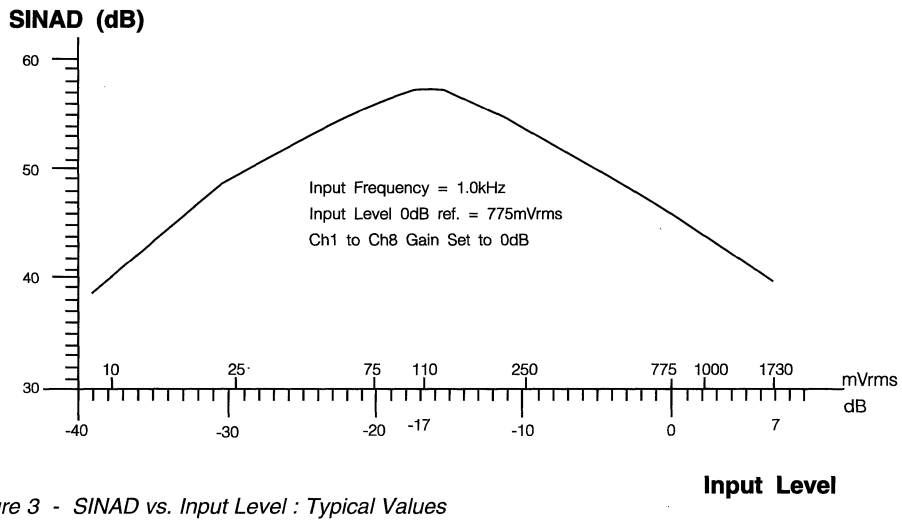


Figure 3 - SINAD vs. Input Level : Typical Values

Control Data and Timing

The gain of each amplifier block (Channels 1 to 8) in the MX009 is set individually by an 8-bit data word (bit 7 to bit 0). This 8-bit word, consisting of 4 Address bits (bit 7 to bit 4) and 4 Gain Control bits (bit 3 to bit 0) is serially loaded to the Control Data Input using the external data clock. Data is loaded to the MX009 on the rising edge of the Serial Clock. Loaded data is executed on the falling edge of the Load/$\overline{\text{Latch}}$ pulse and on the rising edge of the Load/$\overline{\text{Latch}}$ pulse. Table 1 shows the format of each 4-bit Address word. Table 2 shows the format of each Gain Control word and Figure 4 shows the data loading operation and timing.

Table 1 Address Word Format

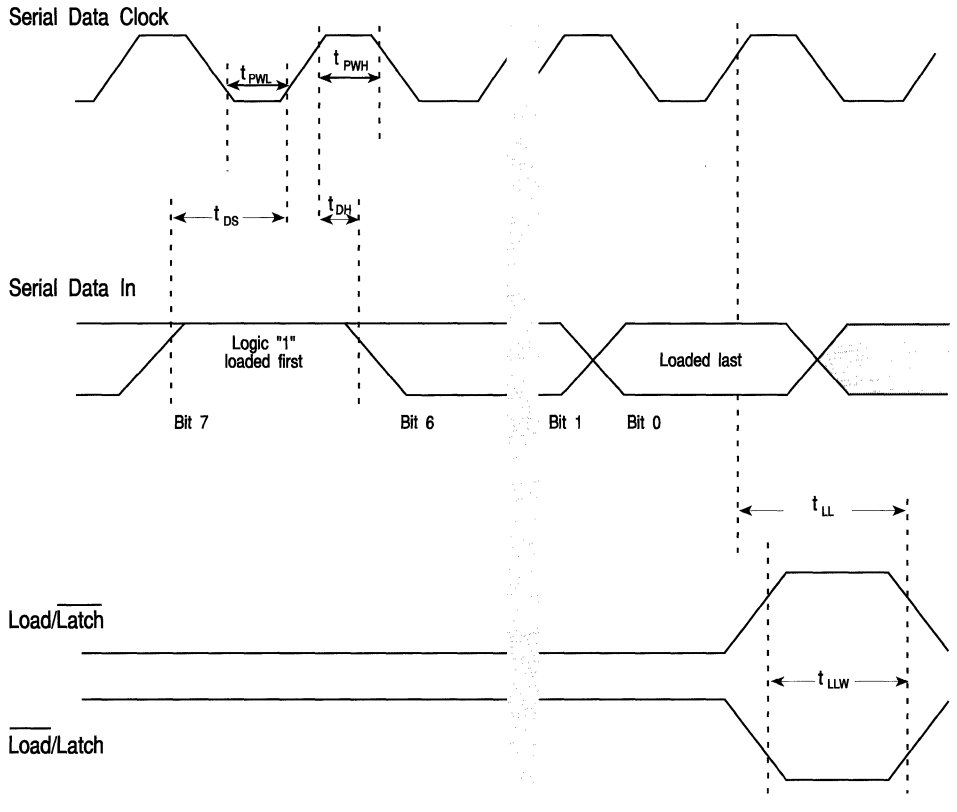
Bit 7 MSB	Bit 6	Bit 5	Bit 4 LSB	Channel Selected
1	0	0	0	1
1	0	0	1	2
1	0	1	0	3
1	0	1	1	4
1	1	0	0	5
1	1	0	1	6
1	1	1	0	7
1	1	1	1	8

Table 2 Gain Control Word Format

Bit 3 MSB	Bit 2	Bit 1	Bit 0 LSB	Stage 1 to 7 2dB	Stage 8 0.43dB
0	0	0	0	Powersave	Powersave
0	0	0	1	-3.0	-14.0dB
0	0	1	0	-2.571	-12.0dB
0	0	1	1	-2.143	-10.0dB
0	1	0	0	-1.714	-8.0dB
0	1	0	1	-1.286	-6.0dB
0	1	1	0	-0.857	-4.0dB
0	1	1	1	-0.428	-2.0dB
1	0	0	0	0	0.0dB
1	0	0	1	0.428	2.0dB
1	0	1	0	0.857	4.0dB
1	0	1	1	1.286	6.0dB
1	1	0	0	1.714	8.0dB
1	1	0	1	2.143	10.0dB
1	1	1	0	2.571	12.0dB
1	1	1	1	3.0	14.0dB

Data Loading

The 8-bit data word is loaded bit 7 first and bit 0 last. Bit 7 must be a logic "1" to address the chip. If bit 7 in the word is a logic "0" that 8-bit word will not be executed. Figure 4 (below) shows the timing information required to load and operate this device.



Timing

t_{PWH}	t_{DS}	t_{LL}
Serial Clock "High" Pulse Width	Data Set-up Time	Load/Latch Set-up Time
t_{PWL}	t_{DH}	t_{LLW}
Serial Clock "Low" Pulse Width	Data Hold Time	Load/Latch Pulse Width

Figure 4 - Serial Control Data Loading Diagram

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3V to (V_{DD} + 0.3V)
Sink/source current (supply pins)	±30mA
(other pins)	±20mA
Total device dissipation (@T_{AMB} 25°C)	800mW Max.
Derating	10mW/°C
Operating temperature:	-40°C to + 85°C
Storage temperature:	-55°C to +125°C

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V

T_{AMB} = 25°C

Audio level 0dB ref = 775 mVrms.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD})		4.5	5.0	5.5	V
Supply Current -Powersave		—	0.16	1.0	mA
-All Stages Operating		—	4.0	8.0	mA
Dynamic Values					
Input Logic "1"		3.5	—	—	V
Input Logic "0"		—	—	1.5	V
Digital Input Impedances		0.5	1.0	—	MΩ
Amplifier Stages (General)					
Bandwidth (-3dB)		15.0	—	- -	kHz
Output Impedance		—	0.8	3.0	kΩ
Total Harmonic Distortion	1	—	0.35	0.5	%
Output Noise Level (per stage)	2	- -	65.0	- -	µVrms
Onset of Clipping	3	—	1.73	—	Vrms
Gain Variation	4	- -	- -	0.1	dB
Interstage Isolation		—	60.0	- -	dB
"Trimmer" Stages (Ch 1 - Ch 7)					
Gain		-3.0		+3.0	dB
Gain Steps (15 in No.)		—	0.43	—	dB
Step Error	5	—	—	±0.2	dB
Input Impedance		100.0	—	—	kΩ
"Volume" Stage (Ch 8)					
Gain		-14.0		+14.0	dB
Gain Steps (15 in No.)		—	2.0	—	dB
Step Error	5	—	—	±0.4	dB
Input Impedance		50.0	—	—	kΩ
Timing (See Figure 4)					
Serial Clock "High" Pulse Width (t_{PWH})		250	—	—	ns
Serial Clock "Low" Pulse Width (t_{PWL})		250	—	—	ns
Data Set-up Time (t_{DS})		150	—	—	ns
Data Hold Time (t_{DH})		50	—	—	ns
Load/Latch Set-up Time (t_{LL})		250	—	—	ns
Load/Latch Pulse Width (t_{LLW})		150	—	—	ns
Serial Data Clock Frequency		—	—	2.0	MHz

Notes

1. *Gain Set 0dB. Input Level 1kHz -3.0dB (549mVrms).*
2. *a.c. short-circuit input, measured in a 30 kHz bandwidth.*
3. *See Figure 3.*
4. *Over temperature and supply voltage range.*
5. *With reference to a 1.0 kHz signal.*

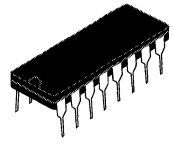
MX·COM, INC. MX019

Preliminary Information

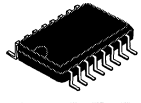
QUAD DIGITAL CONTROL AMPLIFIER

Features

- **4 Digitally Controlled Amplifiers**
- **15 Gain/Attenuation Steps**
- **3 Amplifiers with a ± 3dB Range in 0.43dB Steps**
- **1 'Volume' Amplifier with a ± 14dB Range in 2dB Steps**
- **8-Bit Serial Data Control**
- **Output Mute Function**
- **Audio and Data Gain Control Applications**
- **Telecommunications, Radio and Industrial Applications**



MX019J
(16-pin CDIP)
MX019P
(16-pin PDIP)



MX019DW
16-pin SOIC

DESCRIPTION

The MX019 Digitally Adjustable Amplifier Array replaces trimmer potentiometers and volume controls in Cellular, LMR, Telephony and Communications applications where voice or data signals need adjustment.

The MX019 is a single-chip LSI consisting of four digitally controlled amplifier stages, each with 15 distinct gain/attenuation steps. Control of each individual amplifier is by an 8-bit serial data stream. Three of the amplifier stages offer a +/-3dB range in steps of 0.43dB, while the remaining amplifier offers a +/-14dB range in steps of 2dB, and is suggested for volume control applications. Each amplifier includes a 16th 'Off' state which, when applied, mutes the output audio from that channel. This array uses a Chip Select input to select one of two MX019s in a system.

This product uses the host microprocessor to digitally control the set-up of all audio levels during development, production/calibration and operation.

Applications include:

(i) Control, adjustment and set-up of communications equipment by an Intelligent ATE without manual intervention – eg. Deviation, Microphone and L/S Levels, RX Audio Level etc.

(ii) Automatic Dynamic Compensation of drift caused by variations in temperature, linearity, etc.

(iii) Fully automated servicing and re-alignment.

The MX019 is a low-power, single 5-volt CMOS device available in 16-pin CDIP, PDIP and SOIC package versions.

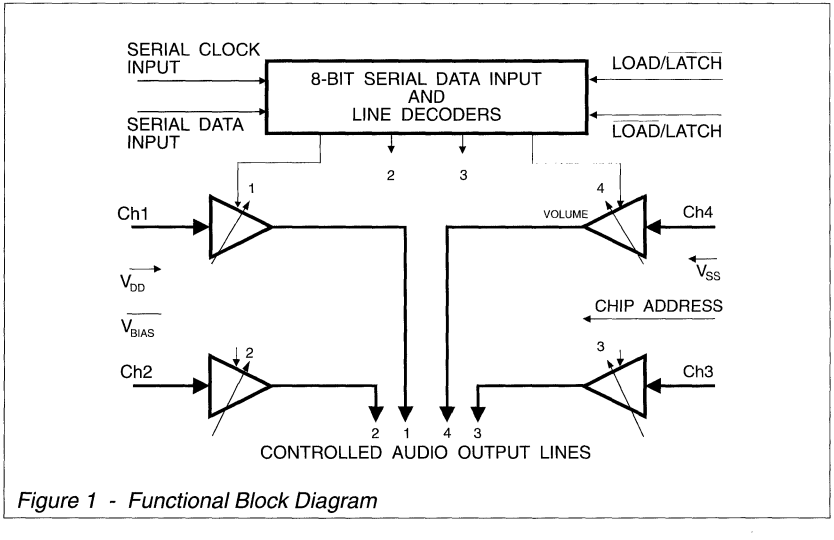
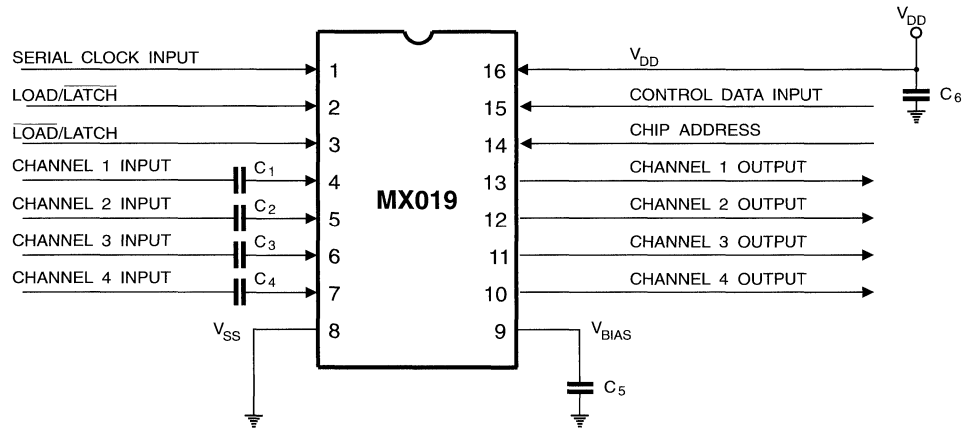


Figure 1 - Functional Block Diagram

PIN FUNCTION TABLE

Pin	Function
1	**Serial Clock :** This external clock pulse input is used to "clock in" the Control Data. See Figure 4, Serial Control Data Load Timing. This input has an internal 1MΩ pullup resistor.
2	**Load/Latch :** This input governs the loading and execution of the control data. During serial data loading this input should be kept at a logical '0' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '0 - 1 - 0' to latch the new data in. Data is executed on the falling edge of the strobe. If the Load/Latch input is used this pin should be left open circuit. This input has an internal 1MΩ pullup resistor.
3	**Load/Latch :** This inverted Load/Latch input governs the loading and execution of control data. During serial data loading this input should be kept at a logical '1' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '1' - '0' - '1' to latch the new data in. Data is executed on the rising edge of the strobe. If the Load/Latch input is used this pin should be left open circuit. This input has an internal 1MΩ pulldown resistor.
4	**Ch1 Input :**
5	**Ch2 Input :**
6	**Ch3 Input :**
7	**Ch4 Input :**
	Analog Inputs : These individual amplifier inputs are self-biasing, a.c. input analog signals must be capacitively coupled to these pins, as shown in Figure 2. Note that amplifiers Ch1 to Ch4 are 'inverting amplifiers.'
8	V_{SS} : Negative supply rail (GND).
9	V_{BIAS} : The output of the on-chip bias circuitry, held at $V_{DD}/2$. This pin should be decoupled to V_{SS} as shown in Figure 2.
10	**Ch4 Output :**
11	**Ch3 Output :**
12	**Ch2 Output :**
13	**Ch1 Output :**
	Controlled Analog Outputs : These are individual "Gain Controlled" amplifier outputs. Ch1 to Ch3 range from -3dB to +3dB in 0.43dB steps, Ch4 can be utilized as a volume control, ranging from -14dB to +14dB in 2.0dB steps. In the "OFF" mode there is no output from the selected amplifier.
14	**Chip Address :** A logic input to select one of two MX019 ICs in a system (see Table 1). This input has an internal 1MΩ pulldown resistor.
15	**Control Data Input :** Operation of the 4 amplifier channels (Ch1 – Ch4) is controlled by the 8 bits of data entered serially at this pin. The data is entered (bit 7 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Tables 1, 2 and Figure 4. This input has an internal 1MΩ pullup resistor.
16	V_{DD} : Positive supply rail. A single +5-volt power supply is required.



Notes

(1) Channel Amplifiers 1 to 4 are inverting amplifiers.

(2) Analog input capacitors C_1 to C_4 are only required for a.c. input signals, d.c. input signals do not require these components.

Component	Value
C_1 to C_4	0.1µF
C_5	1.0µF
C_6	1.0µF

Tolerances: C = ± 20%

Figure 2 - External Component Connections

Application Recommendations

To avoid excess noise and instability you should take note of the following:

(a) A noisy or badly regulated power supply can cause instability and/or variance of selected gains.

(b) Care should be taken on the design and layout of the printed circuit board.

(c) All external components (Figure 2) should be kept close to the MX019 package.

(d) Inputs and outputs should be shielded wherever possible.

(e) Tracks should be kept short.

(f) Analog tracks should not run parallel to digital tracks.

(g) A "Ground Plane" connected to V_{SS} will assist in eliminating external pick-up on the channel input and output pins.

(h) Do not run high-level output tracks close to low-level input tracks.

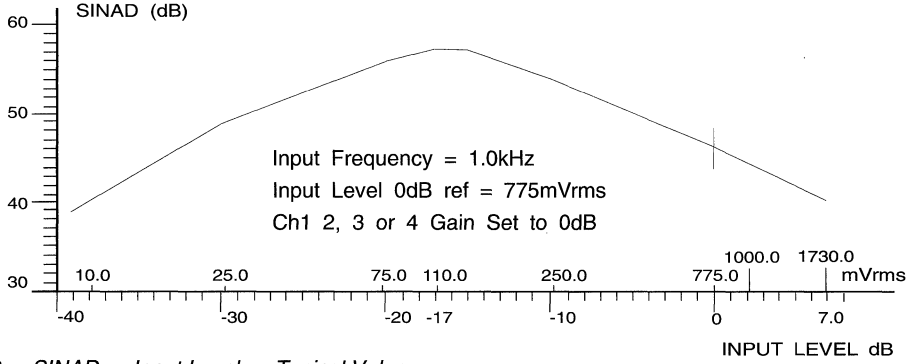


Figure 3 - SINAD vs Input Level – Typical Values

Control Data and Timing

The gain of each amplifier block (Channel 1 to Channel 4) in the MX019 is set by a separate 8-bit data word (bit 7 to bit 0). This 8-bit word, consisting of 4 Address bits (bit 7 to bit 4) and 4 Gain Control bits (bit 3 to bit 0), is loaded to the Control Data Input in serial format using the external data clock.

Data is loaded to the MX019 on the rising edge of the Serial Clock. Loaded data is executed on the falling (rising) edge of the Load/Latch (Load/Latch) pulse. Table 1 shows the format of each 4-bit Address word, Table 2 shows the format of each Gain Control word with Figure 4 describing the data loading operation and timing.

Table 1 Address Bits Format

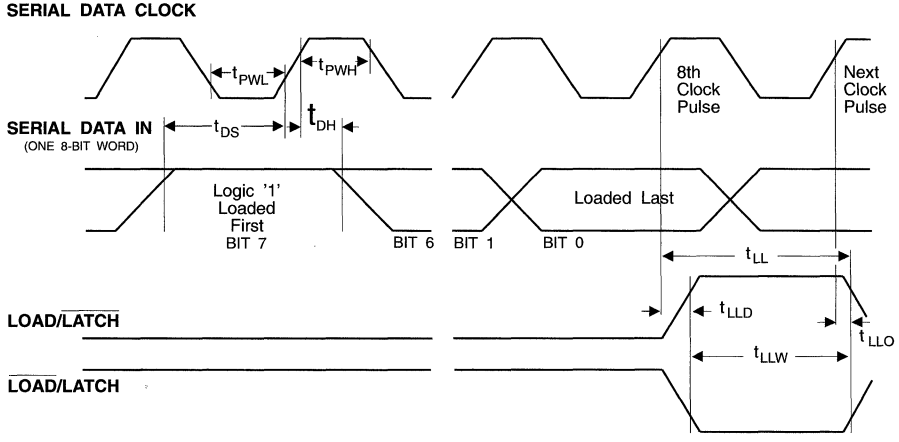
Bit 7 MSB	Bit 6	Bit 5	Bit 4 LSB	Channel Address	Chip Address	Chip Number
1	0	0	0	1	0	
1	0	0	1	2	0	Chip
1	0	1	0	3	0	1
1	0	1	1	4	0	
1	1	0	0	1	1	
1	1	0	1	2	1	Chip
1	1	1	0	3	1	2
1	1	1	1	4	1	

Table 2 Gain Control Bits Format

Bit 3 MSB	Bit2	Bit 1	Bit 0 LSB	Stage 1, 2, 3 (0.43dB)	Stage 4 (2.0dB)
0	0	0	0	OFF	OFF
0	0	0	1	-3.0	-14.0dB
0	0	1	0	-2.571	-12.0
0	0	1	1	-2.143	-10.0
0	1	0	0	-1.714	-8.0
0	1	0	1	-1.286	-6.0
0	1	1	0	-0.857	-4.0
0	1	1	1	-0.428	-2.0
1	0	0	0	0	0
1	0	0	1	0.428	2.0
1	0	1	0	0.857	4.0
1	0	1	1	1.286	6.0
1	1	0	0	1.714	8.0
1	1	0	1	2.143	10.0
1	1	1	0	2.571	12.0
1	1	1	1	3.0	14.0

Data Loading

The 8-bit data word is loaded *bit 7 first and bit 0* last. Bit 7 must be a logic "1" to address the chip.
If bit 7 in the word is a logic "0" that 8-bit word will not be executed. The Chip Address input permits the use of two devices in a system by indicating to the chip what its address is, a "1" or a "0." Bit 6 in the address section of the control word is then used to select which device is being controlled. Figure 4 (below) shows the timing information required to load and operate this device.



Timing

t_{PWH}
Serial Clock "High" Pulse Width

t_{PWL}
Serial Clock "Low" Pulse Width

t_{DS}
Data Set-up Time

t_{DH}
Data Hold Time

t_{LLD}
Load/Latch Delay

t_{LL}
Load/Latch Set-up Time

t_{LLW}
Load/Latch Pulse Width

t_{LLO}
Load/Latch Over Time

Fig.4 Serial Control Data Loading Diagram

SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3V to (V_{DD} + 0.3V)
Sink/Source Current (supply pins)	±30mA
(other pins)	±20mA
Total Device Dissipation @ T_{AMB} 25°C	800mW max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD}=5.0V

T_{AMB}=25°C

Audio Level 0dB ref. = 775mVrms

Amplifier Gain Set = 0dB

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD})		4.5	5.0	5.5	V
Supply Current		-	1.5	-	mA
Dynamic Values					
Control Functions					
Input Logic '1'		3.5	–	–	V
Input Logic '0'		–	–	1.5	V
Digital Input Impedances		0.5	1.0	–	MΩ
Amplifier Stages (General)					
Bandwidth (-3dB)		20.0	–	–	kHz
Output Impedance		–	1.0	-	kΩ
Total Harmonic Distortion	1	–	0.35	0.5	%
Output Noise Level (per stage)	2	–	180.0	400.0	µVrms
Onset of Clipping	3	–	1.73	–	Vrms
Gain Variation	4	–	–	0.1	dB
Interstage Isolation		–	60.0	–	dB
"Trimmer" Stages (Ch1 – Ch3)					
Gain		-3.0		+3.0	dB
Gain per Step (15 in No.)		–	0.43	–	dB
Step Error		–	–	0.2	dB
Input Impedance		100.0	–	–	kΩ
"Volume" Stage (Ch4)					
Gain		-14.0		+14.0	dB
Gain per Step (15 in No.)		–	2.0	–	dB
Step Error		–	–	0.4	dB
Input Impedance		50.0	–	–	kΩ
Timing (Figure 4)					
Serial Clock "High" Pulse Width (t_{PWH})		250	–	–	ns
Serial Clock "Low" Pulse Width (t_{PWL})		250	–	–	ns
Data Set-up Time (t_{DS})		150	–	–	ns
Data Hold Time (t_{DH})		50.0	–	–	ns
Load/Latch Set-up Time (t_{LL})		250	–	–	ns
Load/Latch Pulse Width (t_{LLW})		150	–	–	ns
Load/Latch Delay (t_{LLD})		200	–	–	ns
Load/Latch Over (t_{LLO})		–	–	50.0	ns
Serial Data Clock Frequency		–	–	2.0	MHz

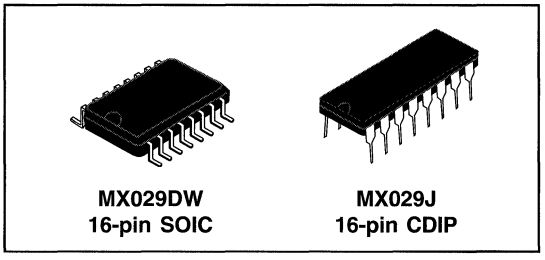
Notes
1. Gain Set 0dB, Input Level 1kHz -3.0dB (549mVrms).
2. With an a.c short-circuit input, measured in a 30kHz bandwidth.
3. See Figure 3.
4. Over the temperature and supply voltage range.

Preliminary Information

DUAL DIGITALLY CONTROLLED AMPLIFIER

FEATURES

- 2 Digitally Controlled Amplifiers
- ±48dB Gain/Attenuation in 2dB Steps + Mute
- Individual Control with a 14-Bit Serial Word
- Output Mute/Powersave Function
- Digitally Set Audio Control Levels
- Separate Fixed Gain Buffer Amplifier



MX029DW
16-pin SOIC

MX029J
16-pin CDIP

APPLICATIONS

- Cellular and LMR Radios
- PABX's, Electronic Mail, TAM's
- Automatic Test Equipment
- Remote Gain Adjustments

DESCRIPTION

The MX029 Digitally Controlled Amplifier Array replaces audio level controls in radio and wireline communications applications. It is a single-chip LSI circuit comprised of two discrete, digitally controlled gain sections. Each section has 48 distinct gain steps (+/-48dB of range in 2dB steps) plus MUTE. The "MUTE" state sets the output to bias (VDD/2) and powersaves the addressed section. Minimum current drain results from muting both sections.

As shown in Figure 1, both gain stages have switchable inputs. This switching allows for selection of three different input signals on one channel and two on the other channel. One of the channels also has output switching.

In addition to two digitally controlled gain stages, there is a general purpose inverting amplifier. The gain of this amplifier is controlled externally via negative feedback. Control of each gain control section is accomplished through the serial interface. All switching is accomplished using controlled rise and fall times, thereby assuring no transients (clicks or pops).

The MX029 requires a single 5-volt supply and is available in 16-pin CDIP and SOIC packages.

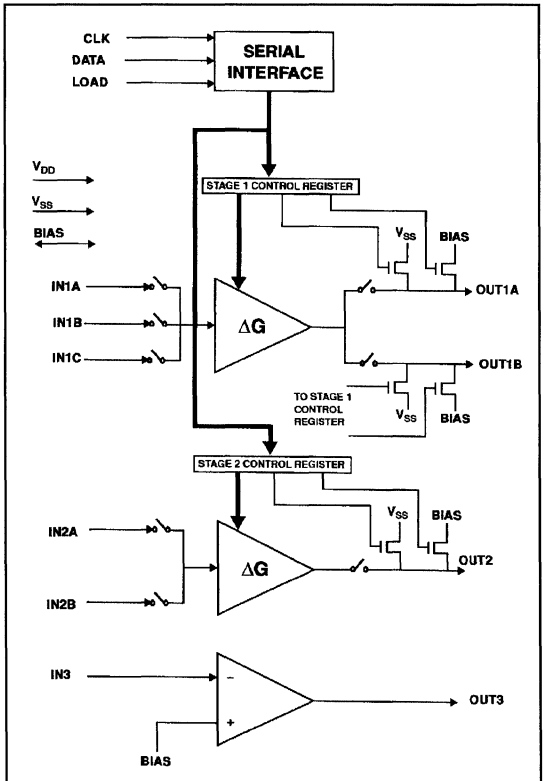
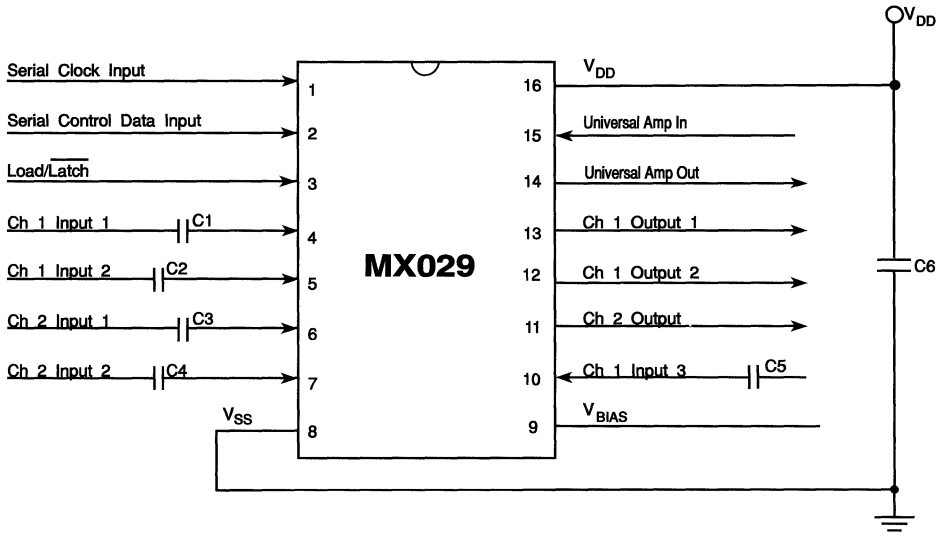


Figure 1 - Functional Block Diagram

7

Pin Function Table

Pin	Function
1	Serial Clock: This external clock input is used to "clock in" the Control Data. See Figure 4 for timing information. This input has an internal 1MΩ pullup resistor.
2	Control (Data) Input: Operation of the two amplifier channels (Ch1 - Ch2) is controlled by the data entered serially at this pin. The data is entered (bit 13 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Tables 1-5 and Figure 3. This input has an internal 1MΩ pullup resistor.
3	Load/$\overline{\text{Latch}}$: This function governs the loading and execution of the control data. During serial data loading this input should be kept at a logical "1" to ensure that data rippling past the latches has no effect. When all 14 bits have been loaded this input should be strobed "1 -> 0 -> 1" to latch the new data in. Data is executed on the rising edge of the strobe.
4	Ch 1 Input 1: Analog Input.
5	Ch 1 Input 2: Analog Input.
6	Ch 2 Input 1: Analog Input.
7	Ch 2 Input 2: Analog Input.
8	V_{SS}: Negative supply rail (GND).
9	V_{BIAS}: The output of the on-chip bias circuitry, held at $V_{DD}/2$. This pin should be decoupled to V_{SS} as shown in Figure 2.
10	Ch 1 Input 3: Analog Input. Normally used for FSK data.
11	Ch 2 Output 1: Analog Output.
12	Ch 1 Output 1: Analog Output.
13	Ch 1 Output 2: Analog Output.
14	Universal Amplifier Output: Output from general purpose amplifier.
15	Universal Amplifier Input: Inverting input to general purpose amplifier.
16	V_{DD}: Positive supply rail. A single +5-volt power supply is required.



Analog input capacitors C1 to C5 are only required for a.c. input signals; d.c. input signals do not require these components.

Component	Value
C1 to C5	0.1µF
C6	1.0µF

Tolerances 20%

Figure 2 - External Component Connections

Application Recommendations

To avoid noise and instability the following practices are recommended:

(a) Use a clean, well-regulated power supply.

(b) Keep leads short.

(c) Inputs and outputs should be shielded wherever possible.

(d) Analog tracks should not run parallel to digital tracks.

(e) A "Ground Plane" connected to Vss will assist in eliminating external pick-up on the channel input and output pins.

(f) Avoid running High Level Outputs adjacent to Low Level Inputs.

(g) The serial clock should not be running consecutively when not in the process of actually loading data.

Control Data and Timing

The gain and I/O signal path for each section (Channels 1 and 2) is set individually by a 14-bit data word (D0 to D13). Data is loaded on the rising edge of the Serial Clock. Loaded data is executed on the rising edge of the Load/Latch pulse.The 14-bit word consists of 1 channel address bit (D7) for selection of the channel to be programmed, 6 bits for setting the gain/attenuation level (D8-D13), 3 bits for input selection (D4 and D6), and 4 bits for output settings (D0-D3). This format is illustrated below in Figure 3.

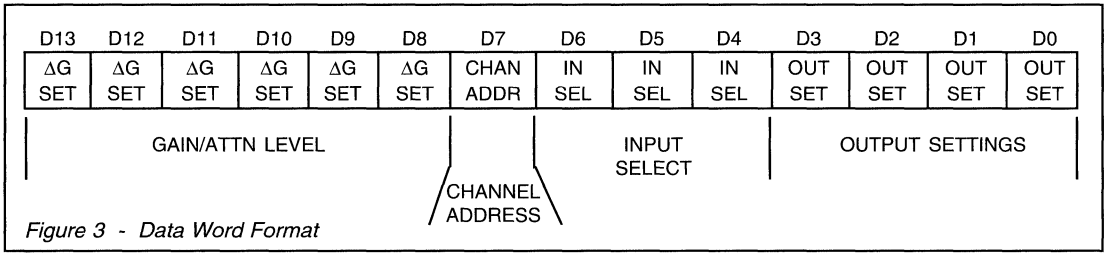


Figure 3 - Data Word Format

Tables 1-5 show how the data word is used to control channel selection, gain/attenuation, input selection and output settings, respectively.

To calculate the data word used to control channel gain/attenuation use the following formula:

$$25 + \left(\frac{\text{gain dB}}{2}\right) = \text{the decimal equivalent of binary Data Word}$$

For example:
using a gain value of +34dB,

$$25 + \left(\frac{+34\ \text{dB}}{2}\right) = 42 = \$2A = \begin{matrix}\text{D13-D8}\\ 101010\end{matrix}$$

D13	D12	D11	D10	D9	D8	GAIN SET (dB)
0	0	0	0	0	0	MUTE
0	0	0	0	0	1	-48
0	0	0	0	1	0	-46
0	0	0	0	1	1	-44
-	-	-	-	-	-	-
-	-	-	-	-	-	-
-	-	-	-	-	-	-
0	1	1	0	0	1	0
-	-	-	-	-	-	-
-	-	-	-	-	-	-
-	-	-	-	-	-	-
1	0	1	1	1	0	+42
1	0	1	1	1	1	+44
1	1	0	0	0	0	+46
1	1	0	0	0	1	+48
1	1	0	0	1	0	+48
1	1	0	0	1	1	+48

Table 1 - Gain/Attenuation Level

D7	CHANNEL SELECTED
0	1
1	2

Table 2 - Channel Selection

D6	D5	D4	INPUTS SELECTED
0	0	0	NONE
0	0	1	1
0	1	0	2
0	1	1	1 & 2
1	0	0	3
1	0	1	1 & 3
1	1	0	2 & 3
1	1	1	1, 2, & 3

Table 3 - Input Select

D3	D2	OUTPUT 2 SETTINGS
0	0	high impedance
0	1	amplifier output
1	0	VSS
1	1	VBIAS

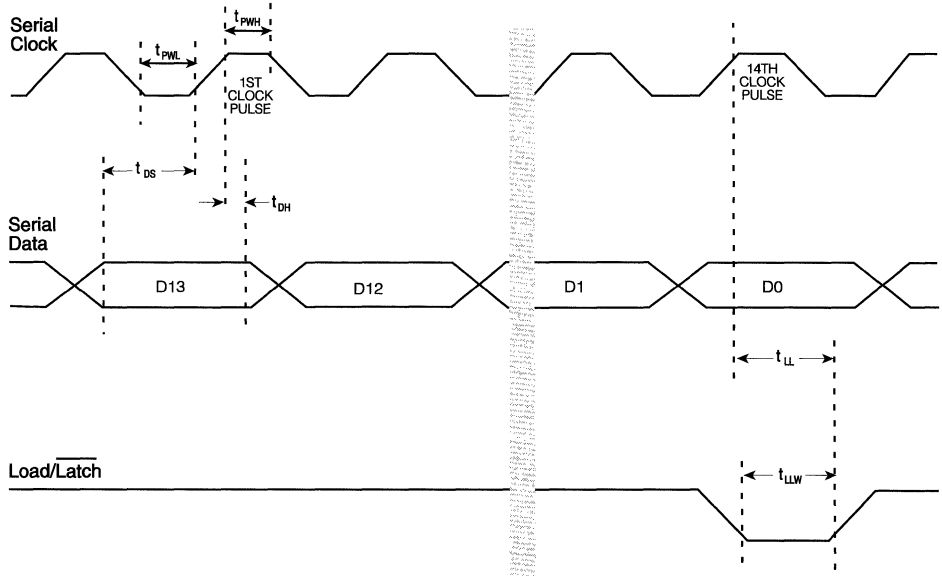
Table 4 - Settings for Output 2 (Ch 1 only)

D1	D0	OUTPUT 1 SETTINGS
0	0	high impedance
0	1	amplifier output
1	0	VSS
1	1	VBIAS

Table 5 - Settings for Output 1

Serial Interface Timing

Figure 4 shows the timing relationships for the serial interface. See specifications page for more information.



t_{PWH}	Serial Clock "High" Pulse Width	t_{PWL}	Serial Clock "Low" Pulse Width
t_{DS}	Data Set-up Time	t_{DH}	Data Hold Time
t_{LL}	Load/Latch Set-up Time	t_{LLW}	Load/Latch Pulse Width

Figure 4 - Serial Timing Diagram

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3V to (V_{DD} + 0.3V)
Sink/source current (supply pins)	±30mA
(other pins)	±20mA
Total device dissipation (@T_{AMB} 25°C)	800mW Max.
Derating	10mW/°C
Operating temperature:	-40°C to + 85°C
Storage temperature:	-55°C to +125°C

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V

T_{AMB} = 25°C

Audio level 0dB ref = 775 mVrms.

External Components as shown in Figure 2.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Supply Voltage		4.5	5.0	5.5	V
Current - All Stages Mute		-	0.1	-	mA
- All Stages Operating		-	3.0	-	mA
Digital Inputs					
Input Logic "1"		3.5	-	-	V
Input Logic "0"		-	-	1.5	V
Digital Input Impedances		0.5	1.0	-	MΩ
Gain Control Amplifier Stages					
Bandwidth (-3dB)	1	3.3	-	-	kHz
Output Impedance		-	1.0	2.0	kΩ
Total Harmonic Distortion	2	-	0.35	0.5	%
Interstage Isolation		-	60.0	-	dB
Gain/Attenuation		46	48	-	dB
Gain/Attenuation Steps (48 total)		-	2.0	-	dB
Step Error		-	-	0.4	dB
Input Impedance		50.0	-	-	kΩ
Input Referred Offset Voltage (V_{IOS})		-	10	-	mV
Universal Amplifier					
Bandwidth (-3dB)	3	10	-	-	kHz
Output Impedance		-	1.0	2.0	kΩ
Total Harmonic Distortion	3	-	0.35	0.5	%
Open Loop DC Gain		-	60	-	dB
Timing (See Figure 4)					
Serial Clock "High" Pulse Width (t_{PWH})		250	-	-	ns
Serial Clock "Low" Pulse Width (t_{PWL})		250	-	-	ns
Data Set-up Time (t_{DS})		150	-	-	ns
Data Hold Time (t_{DH})		50	-	-	ns
Load/Latch Set-up Time (t_{LL})		250	-	-	ns
Load/Latch Pulse Width (t_{LLW})		150	-	-	ns
Serial Data Clock Frequency		-	-	2	MHz

Notes on Characteristics:

1. Gain set to maximum (+48 dB)
2. Gain Set 0dB. Input Level 1kHz -3.0dB (549mVrms).
3. Gain externally set to 10 dB.

Section 8: Telephony

The following section contains specifications on MX-COM's SPM devices for telephone systems.

Subscriber Pulse Metering (SPM) is a poular method of charge metering telephone calls at the PABX and subscriber level in Europe. Belgium, Finland, France, Germany, Spain, Switzerland and Sweden are among the countries with SPM standards. Each specifies unique tone pulse repetition rates, pulse lengths, pulse pause lengths, pulse levels and frequency "must" and "must not" decode bandwidths.

Device	Description	Page	
MX613	Global Call Progress Detector	p. 469	**NEW**
MX623	Line-Powered Call Progress Detector	p. 477	**NEW**
MX631	Low-Power SPM Detector	p. 483	**NEW**
MX641	Dual SPM Detector	p. 490	**NEW**

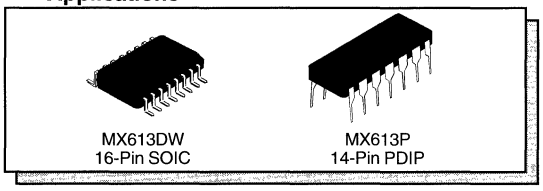
MX•COM, INC. MX613

Advance Information

GLOBAL CALL PROGRESS DETECTOR

Features

- **MX•COM MiXed Signal CMOS**
- **Covers Worldwide Call Progress Frequencies (300Hz to 2,150Hz)**
- **3 Volt <1mA Requirement**
- **Decodes Single or Modulated Tones**
- **Analog In/Serial Data Out**
- **Speech Discrimination Ability**
- **µProcessor Compatible Outputs**
- **Telephone/Telecoms, Radio and Fax/Modem Applications**



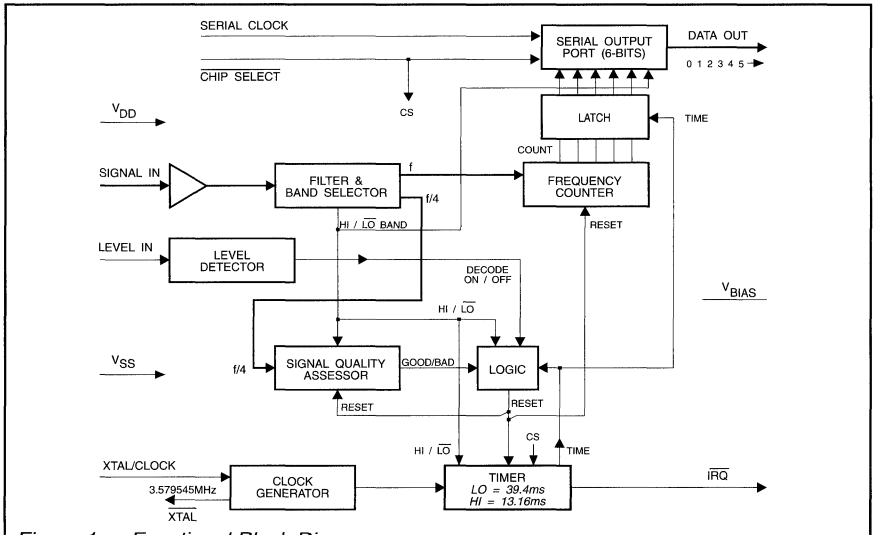


Figure 1 - Functional Block Diagram

Description

The MX613 is a wide-band, 'N-Tone' non-predictive tone decoder that measures telephone system call progress tones in PABX, Pay/Feature-Phone, Fax and Modem systems.

Adhering to Must/Must-Not Decode limits and able to measure inband frequencies in outband modulation, this decoder measures the frequency of input signals in the range 300 to 2,150Hz. The result of each measurement is presented to a system µProcessor as a 6-bit serial word.

The decode frequency range, which covers the world's call progress application spectrum, is processed internally as two bands: LO = 300 to 660Hz and HI = 900 to 2150Hz. Frequency measurement is achieved by counting the number of cycles in a set time period (LO = 39.47ms or HI = 13.16ms). Bad signal/level quality or NOTONE results in a count-abort, timing-reset and no output from the decoder.

Front-end filtering is achieved using MX•COM's patented Auto-Correlator. Current frequency information is output for the µProcessor using a Serial Data, Clock and Interrupt interface.

Data from the MX613 should be processed by a µProcessor whose algorithms are able to recognize the frequency, sequence and/or cadence of input signals as national call progress information; e.g.: 'Dial,' 'Busy,' 'Number-Unobtainable,' 'Ringing' and automatic tones used by fax and modem systems. Software can be simply configured to reject speech frequencies.

Available in SOIC and PDIP packages, this low-cost, mixed signal IC has a typical power requirement of less than 1mA at 3 volts and utilizes a telecom-system clock input of 3.579545MHz to maintain frequency accuracy.

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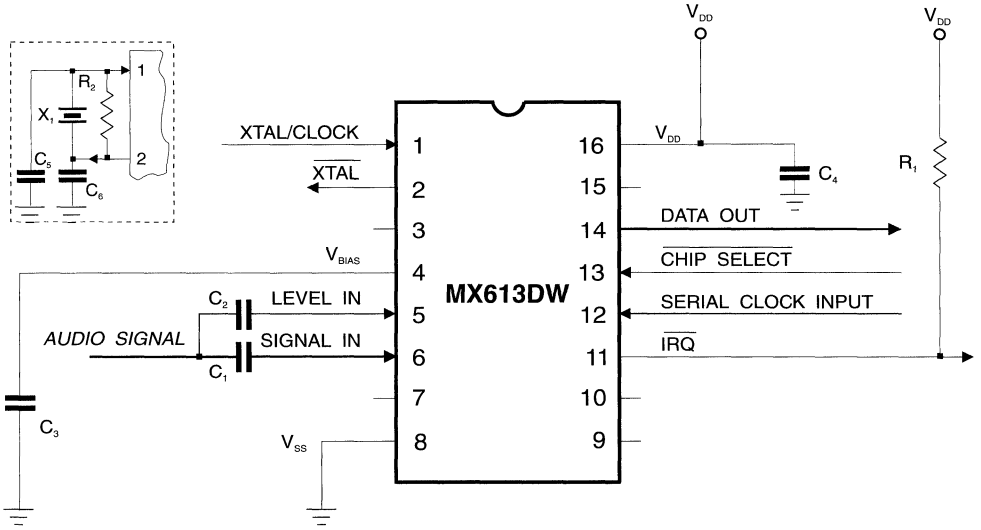
Pin Number		Function
MX613DW	MX613P	
1	1	**Xtal/Clock**: The input to the on-chip clock oscillator inverter. A 3.579545MHz Xtal or externally derived telephone system clock (f_{XTAL}) should be connected here. Operation of the MX613 without a suitable Xtal/Clock input may cause device damage.
2	2	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator inverter. See Figure 2.
3	3	No internal connection.
4	4	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS}.
5	5	**Level In:** The input for level discrimination. This input is internally biased to V_{BIAS}. Signals must be a.c. coupled, and the audio signal must be fed to both this pin and the Signal In pin. Correct level detection determines the operation of this device (see Principles of Decoder Operation). But if you wish to disregard the amplitude of the input levels, the MX613 may be permanently enabled by pulling this pin to V_{DD} and disabled by pulling to V_{SS}.
6	6	**Signal In:** The input for frequency discrimination and decoding. This input is internally biased to V_{BIAS}. Signals must be a.c. coupled. The audio signal must be fed to both this pin and the Level In pin.
7		No internal connection.
8	7	**V_{SS}:** Signal ground (GND).
9	8	No internal connection.
10		No internal connection.
11	9	**$\overline{\text{IRQ}}$:** This Interrupt Request output from the MX613 is 'wire-OR able' allowing the interrupt outputs of other peripherals to be combined and connected to the Interrupt input of a µProcessor. This input has a low-impedance pulldown to V_{SS} when active and a high-impedance when inactive. An interrupt is produced on completion of a HI or LO frequency measurement.
12	10	**Serial Clock:** The serial clock from the µProcessor. Data Out is clocked into the µProcessor on the rising edge of the Serial Clock. See Data-Read Timing diagram.
13	11	**$\overline{\text{Chip Select}}$:** A logic "0" at this input will select this device.
14	12	**Data Out:** The serial data output. Under the control of the Chip Select and Serial Clock inputs, data should be read from this output in 6-bit blocks MSB (Bit-5) first. If 8 serial clock pulses are applied, two additional logic "0s" will be output after Bit-0.
15	13	No internal connection.
16	14	**V_{DD}:** Positive supply input. A single, stable supply is required. Levels and voltages within the MX613 are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor located close to the MX613 pins.

Application Information



Notes

(1) The Xtal/Clock input may be driven from the host telephone system's 3.579545MHz clock; if a Xtal drive is required, the configuration shown in the INSET is recommended.

(2) The audio signal should be input to both Signal In and Level In pins via separate coupling capacitors. If it is wished to operate the device with disregard to on-chip level thresholds and permanently enable the MX613, the Level In pin should be held at V_{DD}. To disable the MX613 the Level In pin should be held at V_{SS}. Level thresholds are preset internally.

Component	Value
R_1	22.0kΩ
R_2	1.0MΩ
C_1	0.01µF
C_2	0.1µF
C_3	1.0µF
C_4	1.0µF
C_5	33.0pF
C_6	33.0pF
X_1	3.579545MHz

Tolerances: C = ± 20% R = ± 10%

Figure 2 - External Component Connections

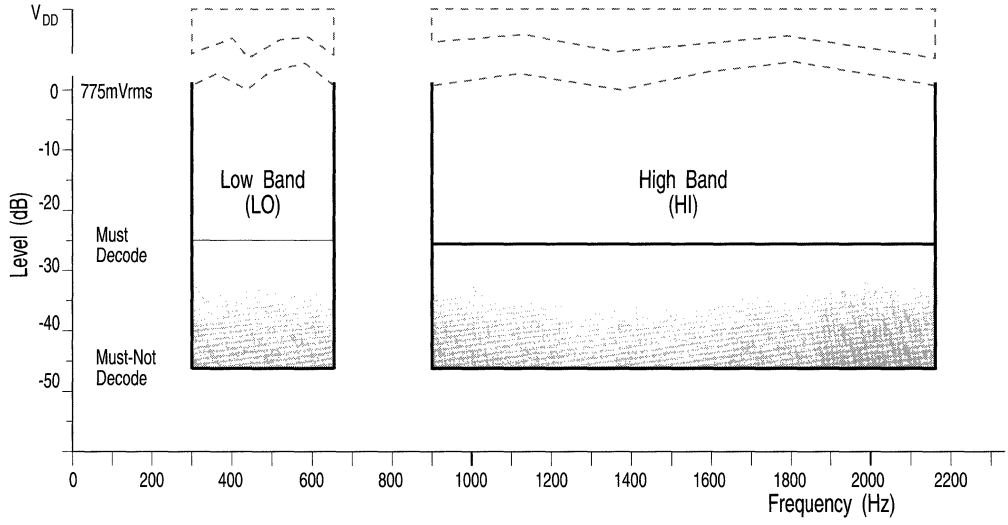


Figure 3 - HI/LO Decode Bands

Application Information .....

Principles of Decoder Operation

Level Detection

Because level and frequency discrimination operations take place in parallel, the audio signal should, under normal circumstances, be input to both Signal In and Level In pins via coupling capacitors.

If the input signal level (Level In) is outside the preset 'Must/Must Not Decode' thresholds (see Specifications), the Universal Call Progress Decoder will be disabled.

If it is wished to disregard signal input *levels* at the Level In pin and attempt to decode under all conditions, the decoder may be permanently enabled by holding the Level In pin at V_{DD}.

The MX613 can disabled by pulling Level In to V_{SS}.

NOTONE Recognition

The NOTONE condition can be recognized using µProcessor software timing as below.

a. Set the µP timer period to a period greater than the relevant frequency-band measurement period (13.16ms or 39.47ms).

b. Each 'Tone Measurement Complete' interrupt from the MX613 must reset the µP timer.

c. With NOTONE or white noise at the decoder input, the MX613 on-chip timer will be continually reset.

ii No 'Tone Measurement Complete' interrupt will occur - the µP timer will run.

ii The µP Timer time-out can be considered as a **NOTONE** indication.

Level In	Timer	IRQ	Data Out	
In Limits	Running	Enabled	Enabled	
Out of Limits	Reset	Disabled	Disabled	(frozen to previous bit-5 level
V_{DD}	Running/Reset	Enabled/Disabled	Enabled	(dependent upon Quality measurement)
V_{SS}	Reset	Disabled	Disabled	(frozen to previous bit-5 level)

Frequency Band Discrimination

The input signal is amplified by a self-biased (zero-crossing) inverting amplifier and then 'filtered' to remove high-frequency noise and jitter.

High (HI) and Low (LO) counters are employed to determine the input frequency band (HI = 900Hz to 2150Hz, LO = 300Hz to 660Hz).

If the input frequency is in the LO Band, the device will operate as a LO Band decoder and will remain so until a HI frequency signal is detected. If the input frequency is in the HI Band, the device will operate as a HI Band decoder and will remain so until a LO frequency signal is detected.

Frequency band monitoring is continuous with the band selection taking place every 9.8ms. It will therefore take 9.8ms from Power-Up to set up the initial correct decode frequency band.

On-Chip Timer Operation

For frequency measurement, the MX613 counts the number of input cycles in a fixed time period. This fixed period, measured by the continuous on-chip timer, is set to 13.16ms for HI Band inputs and 39.47ms for LO Band inputs.

On-Chip Timer Operation .....

When the timer expires the following actions take place:

a. A HI or LO ("1" or "0") band indication bit is latched into Bit-5 of the Serial Output Port.

b. The Frequency Counter count of 5-bits is latched into the Serial Output Port (Bit-4 [MSB] to Bit-0). The Serial Output Port Contains 6-bits, if 8 Serial Clock edges are employed, two extra "0s", which should be ignored, will be output last.

c. An interrupt is generated ($\overline{IRQ}$) to the µProcessor. The contents of the Serial Output Port should be read before the next interrupt is expected; if not data will be overwritten.

When the Chip Select input is set to "0" the interrupt is reset.

The On-Chip Timer and Frequency Counter will be reset in mid-count, and therefore unable to allow a valid measurement, under the following conditions:

a. A change of decode frequency band.

b. Decoder disabled; signal input level out of specification or Level Detect input set to V_{SS}.

c. Signal Quality Assessment considered 'Bad'.

d. Input signal frequency outside limits.

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Application Information .....

N = int (Frequency x Measurement Period)

Measurement Period = 39.47ms for Low Band (300Hz to 660Hz)
= 13.16ms for High Band (900Hz to 2150Hz)

Note: For input frequencies of between 661Hz and 899Hz the MX613 will give no reliable output.

When a 'correct' decode has been allowed and an interrupt generated, a 6-bit data word is presented at the Serial Output Port. This 6-bit word indicates the input frequency's band (Bit 5) and value 'N' as indicated below.

Bit 5 Output First	Band Bit (5)	MSB (4)	(3)	(2)	(1)	LSB (0)	Bits 0 to 4 = N
	HI-"1"/LO-"0"	Bits 0 to 4 represent the measured frequency in the selected band					

When a 'correct' decode has been allowed and an interrupt generated, a 6-bit data word will be presented at the Serial Output Port. This 6-bit word indicates the input frequency's band and value as described below.

As an example, the following binary-word presented at the Serial Output Port **(1 1 0 1 1 0)** will indicate a frequency in the **HI Band** of between **1680Hz** and **1740Hz (Bit-5 = "1" = HI, 'N' = 22)**.

LO Band	HI Band	N	B_5	B_4	B_3	B_2	B_1	B_0	LO Band	HI Band	N	B_5	B_4	B_3	B_2	B_1	B_0
280	*840*	11	H/L	0	1	0	1	1	505	1515	19	H/L	1	0	0	1	1
285	*855*	11							510	1530	20	H/L	1	0	1	0	0
290	*870*	11							515	1545	20						
295	885	11							520	1560	20						
300	900	11							525	1575	20						
305	915	12	H/L	0	1	1	0	0	530	1590	20						
310	930	12							535	1605	21	H/L	1	0	1	0	1
315	945	12							540	1620	21						
320	960	12							545	1635	21						
325	975	12							550	1650	21						
330	990	13	H/L	0	1	1	0	1	555	1665	21						
335	1005	13							560	1680	22	H/L	1	0	1	1	0
340	1020	13							565	1695	22						
345	1035	13							570	1710	22						
350	1050	13							575	1725	22						
355	1065	14	H/L	0	1	1	1	0	580	1740	22						
360	1080	14							585	1755	23	H/L	1	0	1	1	1
365	1095	14							590	1770	23						
370	1110	14							595	1785	23						
375	1125	14							600	1800	23						
380	1140	14							605	1815	23						
385	1155	15	H/L	0	1	1	1	1	610	1830	24	H/L	1	1	0	0	0
390	1170	15							615	1845	24						
395	1185	15							620	1860	24						
400	1200	15							625	1875	24						
405	1215	15							630	1890	24						
410	1230	16	H/L	1	0	0	0	0	635	1905	25	H/L	1	1	0	0	1
415	1245	16							640	1920	25						
420	1260	16							645	1935	25						
425	1275	16							650	1950	25						
430	1290	16							655	1965	25						
435	1305	17	H/L	1	0	0	0	1	660	1980	26	H/L	1	1	0	1	0
440	1320	17							*665*	1995	26						
445	1335	17							*670*	2010	26						
450	1350	17							*675*	2025	26						
455	1365	17							*680*	2040	26						
460	1380	18	H/L	1	0	0	1	0	*685*	2055	27	H/L	1	1	0	1	1
465	1395	18							*690*	2070	27						
470	1410	18							*695*	2085	27						
475	1425	18							*700*	2100	27						
480	1440	18							*705*	2115	27						
485	1455	19	H/L	1	0	0	1	1	*710*	2130	28	H/L	1	1	1	0	0
490	1470	19							*715*	2145	28						
495	1485	19							*720*	2160	28						
500	1500	19							*725*	*2175*	28						

Table 1 - Decode Frequency Data

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Application Information .....

Decoder Timing

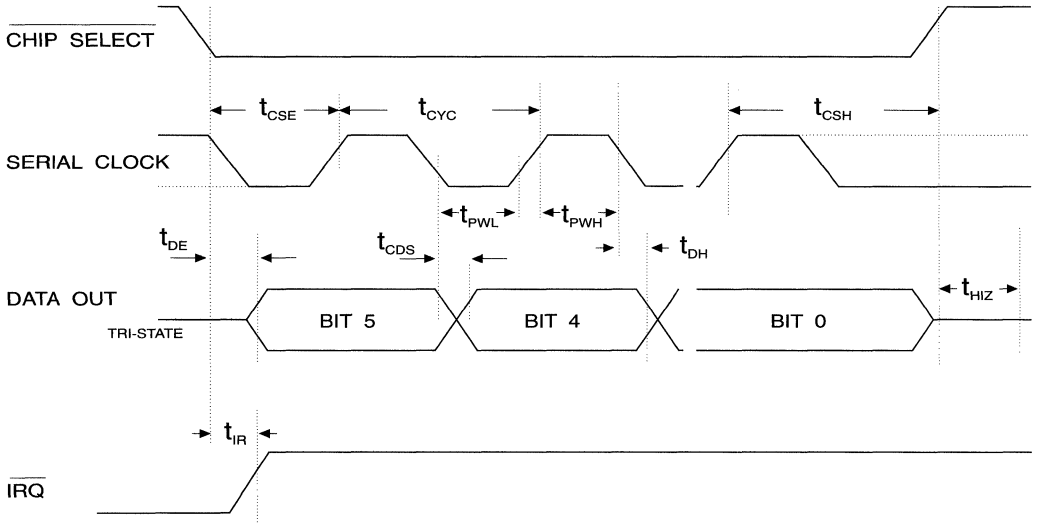

Figure 4 - Data-Read Timing

Decoder Timing Characteristics

With reference to Figure 4, *Data-Read Timing.*

	Characteristics	Min.	Typ.	Max.	Unit
t_{PWH}	Serial Clock "High" Pulse Width	250	-	-	ns
t_{PWL}	Serial Clock "Low" Pulse Width	250	-	-	ns
t_{CYC}	Serial Clock-Cycle Time	600	-	-	ns
t_{CSE}	Chip Select Low to Clock "High" Edge	450	-	-	ns
t_{CSH}	Last Clock "High" Edge to CS "High"	600	-	-	ns
t_{DH}	Data Out Hold Time	0	-	-	ns
t_{CDS}	Clock Edge to Data Out Set Time	-	-	200	ns
t_{IR}	Interrupt (IRQ) Reset Time	-	-	200	ns
t_{DE}	Chip Select "Low" to Data Enable	-	-	200	ns
t_{HIZ}	Chip Select "High" to Output Tri-State	-	-	1000	ns

Notes

1 Data is output bit 5 first. Bit 5 can be clocked into the µProcessor by the first Serial Clock rising edge. If 8 Serial Clock pulses are employed the last 2 data-bits will be "0" and should be ignored by the software.

2 Chip Select should be used to react to Interrupts and then returned to a logic "1". If Chip Select stays low there will be no further Interrupts and no Data Output update.

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Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0V
Input Voltage at any pin (ref V_{SS}=0V)	-0.3 to (V_{DD}+ 0.3V)
Sink/Source Current (supply pins)	± 30mA
(other pins)	±20mA
Total Device Dissipation (@ T_{AMB}=25°C)	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 3.3V

T_{OP} = -40 to +85°C

Audio Level 0dB ref = 775 mVrms

Xtal/Clock f_0 = 3.579545 MHz

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD}) at 25°C		3.0	-	5.5	V
Supply Current		-	0.3	1.0	mA
Input Logic "1"		70.0	-	100	% V_{DD}
Input Logic "0"		0	-	30.0	% V_{DD}
Output Logic "1"	1	90.0	-	100	% V_{DD}
Output Logic "0"	1	-	-	10.0	% V_{DD}
Impedances					
Chip Select and Serial Clock Input		10.0	-	-	MΩ
Signal Input		-	50.0	-	kΩ
Level Input		-	210	-	kΩ
IRQ Output (Logic "0")		-	-	500	Ω
Data Output (Logic "0")		-	500	-	Ω
(Logic "1")		-	-	2.5	kΩ
Dynamic Values					
On-Chip Xtal Oscillator					
R_{IN}		10.0	-	-	MΩ
R_{OUT}		-	230	825	kΩ
DC Voltage Gain		25.0	42.0	-	V/V
Bandwidth at Unity Gain		5.0	11.0	-	MHz
Single Tone Operation					
Must-Decode Input Level	2	-25.2	-	-	dB

8

Characteristics	See Note	Min.	Typ.	Max.	Unit
Must-Not Decode Input Level	2	-	-	-46.0	dB
LO Band Frequency Range	4	300		660	Hz
HI Band Frequency Range	4	900		2150	Hz
Frequency Resolution (Table 1)					
LO Band		-	-	25.0	Hz
HI Band		-	-	75.0	Hz
Input Signal/White-Noise Ratio (HI & LO Bands)		-	18.0	-	dB
Interrupt Rate (LO Band)	3	19.0	-	-	/sec
(HI Band)	3	57.0	-	-	/sec
False Decodes Due to Noise	6	-	1.0	-	/2 secs
Outband modulation level limits for correct decode (f_{IN} = 340Hz to 620Hz)	5	-	-	10.0	%

Notes

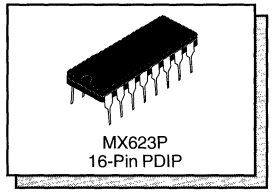
1. Into a high-impedance load (>1.0MΩ).
2. Must decode signal above -25.2dB; Must Not decode signal below -46.0dB.
   If a supply other than 3.3 volts is used, levels will change pro-rata.
3. Under 'Pure Tone' input conditions.
4. For input frequencies of between 661Hz and 899Hz the MX613 will provide reliable output.
5. With an amplitude modulating frequency of between 16.0Hz and 100Hz.
6. Test noise input = 5.0kHz at 100mVrms

Advance Information

LINE-POWERED CALL PROGRESS TONE DETECTOR

Features

- **MX•COM MiXed Signal CMOS**
- **Measures Call Progress Tone Frequencies ('Busy', 'Dial', 'Fax-Tone' etc.)**
- **Telephone, PABX, Fax and Dial-Up Modem Applications**
- **Low-Power Requirement (600µA at 3.3 Volts$_{TYP}$) for Line-Powered Applications**
- **Custom Tone Decoder (13 Call-Progress Frequencies Recognized)**
- **Operates to a 3.579545MHz Telephone System Clock**
- **Operates Under Simple Logic or µProcessor System Control**



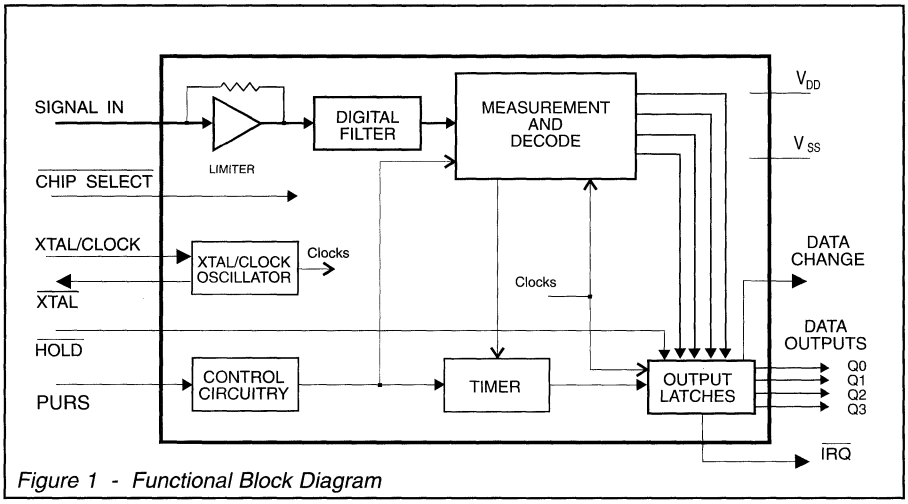


Figure 1 - Functional Block Diagram

Description

The MX623 is a low-power decoding integrated circuit that measures the frequency of telephone system call progress tones.

With progress signals input from the telephone line, this single-chip product is programmed to recognize up to thirteen of the World's most commonly used call-progress frequencies, analyze signal quality, and present the measured result as a 4-bit parallel data word at the tri-state Data Output.

Using the parallel information from the MX623, the host system, can recognize such call progress information as: 'Dial', 'Busy', 'Number Unobtainable', 'Ringing' and Fax/Modem system signals.

This information can then be used in simple or complex applications to control telephone operations. The data output will require a software format that can analyze the frequency information from the MX623.

Requiring only a single 3.0$_{[MIN]}$ volt power supply, the MX623 may be line-powered and will operate under simple logic or system µProcessor control using the 'Data-Change, 'Hold' and 'Chip-Select' functions.

The MX623, whose small size and low power consumption makes it ideal for remote applications, requires a 3.579545MHz telephone system clock or Xtal input, is available in a 16-pin PDIP.

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Pin	Function
1 2 3 4	**Q3:** **Data Outputs:** A 4-bit parallel data word, forming a HEX character representing the **Q2:** decoded tone frequency. This word is output after a successful decode. Table 1 details the **Q1:** Hex character output codes for the relevant decoded tone frequencies. Upon power-up this **Q0:** output is set to 'E_H', but no Data Change pulse generated. These are tri-state outputs.
5	**V_{DD}:** Positive supply rail. A minimum supply voltage of 3.0 volts is required. Levels and voltages within this decoder are dependent upon this supply.
6	**Signal In:** The composite audio input. Signals to this pin should be a.c. coupled. The d.c. bias of the limiter section is set internally; this pin should not be loaded with any other circuitry.
7	No internal connection. Leave open circuit.
8	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator inverter.
9	No internal connection. Leave open circuit.
10	**Xtal/Clock:** The input to the clock oscillator inverter. A 3.579545MHz Xtal or externally derived clock should be connected here (see Figure 2).
11	**V_{SS}:** Negative supply rail (GND).
12	**$\overline{\text{Hold}}$:** An input to control the Output Latch condition; employed in combination with the Data Change output to facilitate, if required, Interrupt and/or handshake operations with a µProcessor. With Hold placed "Low", with a tone input, the Data Change output will be held "High" at the next data change, and the current output code is locked in the Output Latches regardless of any changes to the input signal. The output code remains as held until this input is returned "High" (see Figure 3). Whilst this input is "High" the output data, Q0 - Q3, cycles normally with the input audio. This pin has an internal 1.0MΩ pullup resistor.
13	**PURS:** Power-Up ReSet. To reset internal circuitry at power-up; a logic "1" level is required at this pin for a duration of at least 2.5ms after the Xtal/Clock input and full V_{DD} levels are applied. The component configuration shown in Figure 2 is recommended; for slow-rising power supplies the time constant of components should be increased accordingly.
14	**$\overline{\text{IRQ}}$:** Interrupt Request. An output for µProcessor operation; normally "High" this output is latched "Low" when an internal data change occurs if the Chip Select input is "High". This output is reset ("High") the when Chip Select line is taken "Low". To permit "wire-OR" connection with other peripherals, this output has a low-impedance when "Low" and a high-impedance when "High".
15	**$\overline{\text{CS}}$:** Chip Select- A controlling function. When held "High" the Data Outputs Q0, Q1, Q2 and Q3 and the Data Change output are disabled. When taken "Low" the Data Outputs Q0, Q1, Q2 and Q3 and the Data Change output are enabled; the Interrupt Request (IRQ) is reset ("High") when CS is taken "Low". See Figures 3 and 4.
16	**Data Change:** A positive-going pulse is generated at this output when the data changes (Tone or NoTone). New tone-data is presented to the Q0, Q1, Q2 and Q3 Data Outputs if the Hold input is set "High". This is a tri-state output.

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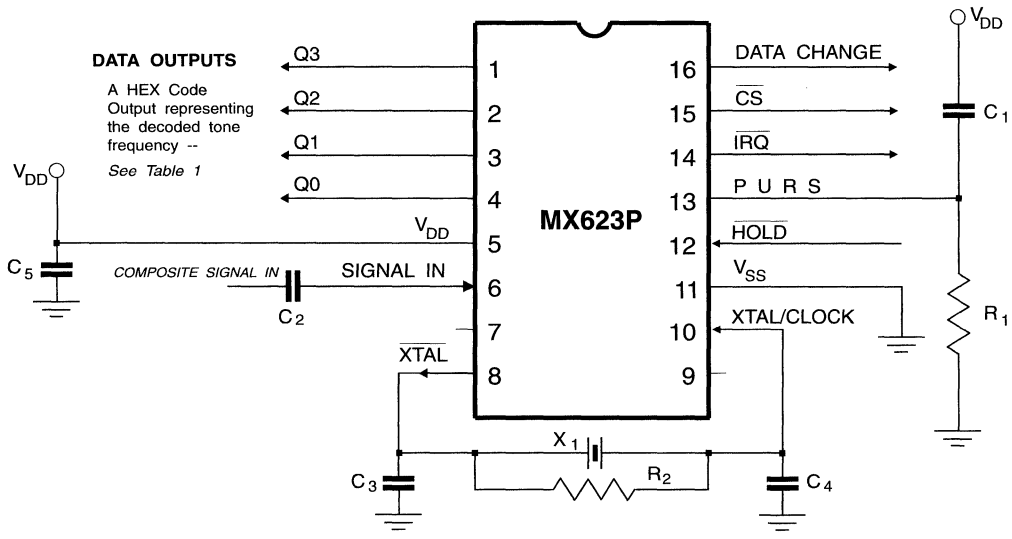
Application Information



Component	Value	Component	Value
R_1	1.0MΩ	C_3	33.0pF
R_2	1.0MΩ	C_4	33.0pF
C_1	.047µF	C_5	1.0µF
C_2	.0047µF	X_1	3.579545MHz

Tolerances R = ±10%, C = ±20%

Figure 2 - Recommended External Components

Hex Character	Output Code Q3 Q2 Q1 Q0	Band Edges (Hz) Lower Edge	Upper Edge	Nominal Center Freq.
0	0 0 0 0	364	386	*375*
1	0 0 0 1	488	520	*500*
2	0 0 1 0	520	580	*550*
3	0 0 1 1	580	618	*600*
4	0 1 0 0	386	412	*400*
5	0 1 0 1	412	436	*425*
6	0 1 1 0	436	463	*450*
7	0 1 1 1	463	487	*475*
8	1 0 0 0	900	1008	*950*
9	1 0 0 1	1273	1325	*1300*
A	1 0 1 0	1350	1455	*1400*
B	1 0 1 1	1750	1855	*1800*
C	1 1 0 0	2062	2140	*2100*
D	1 1 0 1	frequency not guaranteed		
E	1 1 1 0	frequency not guaranteed		
F	1 1 1 1	NOTONE		

Table 1 - Tone Decode Frequencies

Timing Information

With CS Low - Figure 3

After initial power-up and the Hold input inactive (High), as frequencies are input, with the Data Change output as an active (High) indicator, the data is presented at the Data Outputs.

If/when the Hold input is placed active (Low), the data at the Data Outputs is frozen and the Data Change output held High at its next active excursion -until the Hold input is returned High.

With the Hold input held High - Figure 4

As frequencies are input a correct decode will produce an active (Low) interrupt level.

This interrupt (IRQ) is serviced and reset by an active (Low) CS input.

Note the 'valid data' period at the Data Outputs.

8

Application Information - Decoder Timing

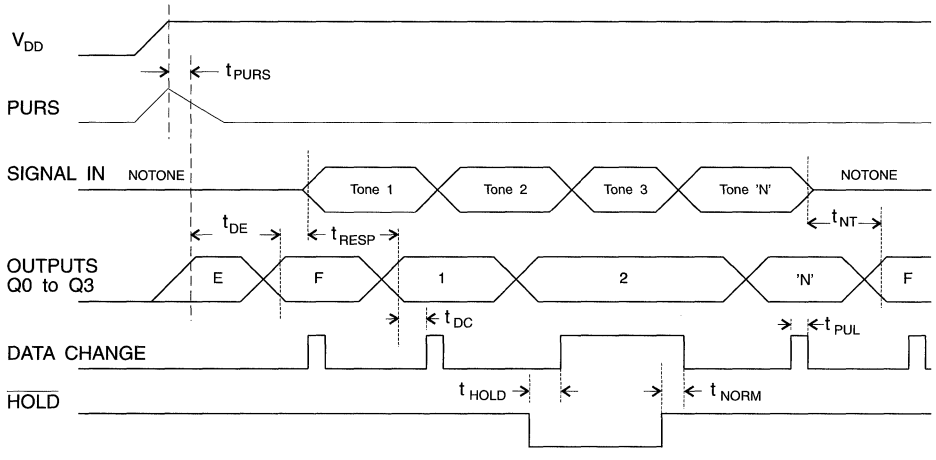


Figure 3 - Timing with the Chip Select Input Held "Low"; CS and IRQ are not used

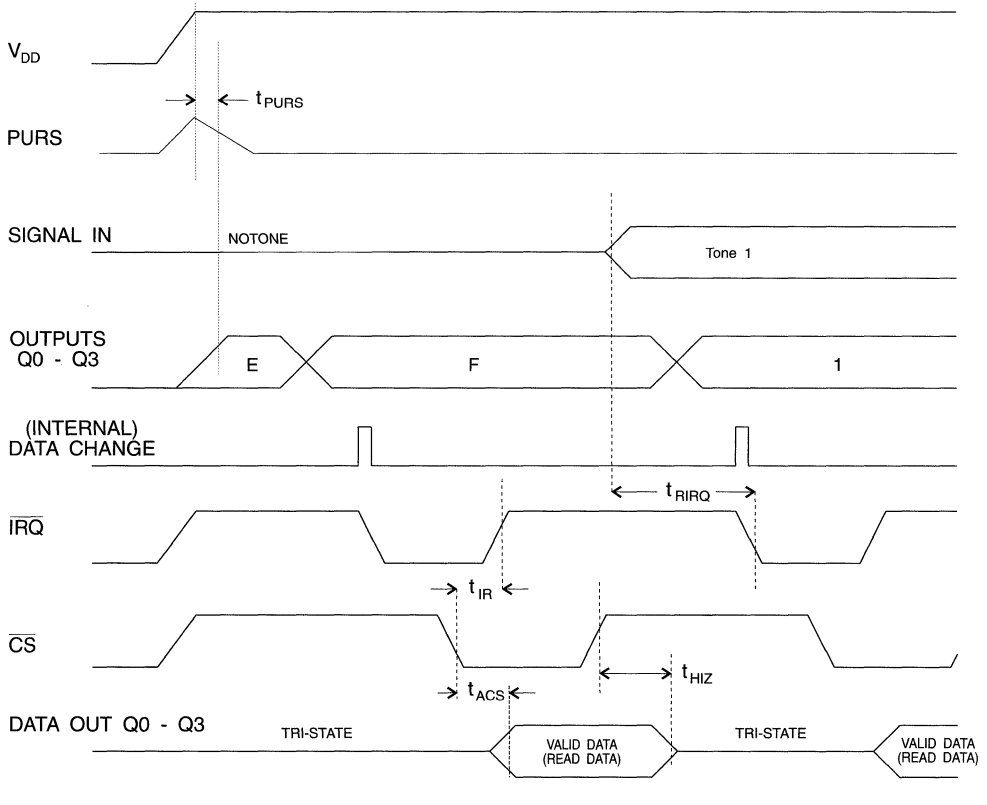


Figure 4 - Timing with the HOLD Input Held "High"; CS and IRQ are used

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)	+/- 30mA
(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Storage temperature range	-40°C to +85°C

Operating Limits

	Min.	Max.	Unit
Supply Voltage (V_{DD}) at 25°C	3.0	5.5	V
Operating Temperature	-40	+85	°C

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 3.3V
T_{OP} = -40 to +85 °C
Audio Level 0dB ref: = 775mVrms
Xtal/Clock Frequency = 3.579545MHz

Characteristics		See Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Current			-	0.6	1.0	mA
Input Logic "1"			0.7	-	-	$\%V_{DD}$
Input Logic "0"			-	-	0.3	$\%V_{DD}$
Output Logic "1"			0.8	-	-	$\%V_{DD}$
Output Logic "0"			-	-	0.2	$\%V_{DD}$
Impedance						
CS and PURS Input			10.0	-	-	MΩ
Hold Input		1	0.5	-	-	MΩ
Signal Input			0.1	-	-	MΩ
IRQ Output (logic "1")			-	30.0	100	kΩ
IRQ Output (logic "0")			-	175	500	Ω
Q0 - Q3 & Data-Change Outputs (logic "1")			-	0.7	2.0	kΩ
Q0 - Q3 & Data-Change Outputs (logic "0")			-	175	500	Ω
Q0 - Q3 & Data-Change Outputs (high Z)			1.0	-	-	MΩ
Dynamic Values						
Signal Input Range		2, 5	35.0		1,166	mVrms
Decode Bandedge Tolerance		3	-1.0	-	1.0	%
Xtal Inverter						
Voltage Gain			20.0	-	-	V/V
Input Impedance			10.0	-	-	MΩ
Output Impedance			-	-	160	kΩ
Decoder Timing - *Figures 3 and 4*						
Power Up Reset Time	t_{PURS}		2.5	-	-	ms
Data 'E' Time	t_{DE}		31.0	-	-	ms
NOTONE to Tone Response Time	t_{RESP}	4	-	27.0	50.0	ms

8

Characteristics		See Note	Min.	Typ.	Max.	Unit
Tone to NOTONE Response Time	t_{NT}	4	-	-	60.0	ms
Data to Data-Change Pulse Time	t_{DC}		0.625	-	1.15	ms
Data-Change Pulse Width	t_{PUL}		-	1.25	-	ms
Hold to Data-Change Rise Time	t_{HOLD}		63.0	-	-	µs
HOLD to Data-Change Fall Time	t_{NORM}		-	-	150	µs
IRQ Tone Response Time	t_{RIRQ}		-	29.0	52.0	ms
IRQ Reset Time	t_{IR}		-	-	250	ns
Data Access Time	t_{ACS}		-	-	250	ns
CS High to Output Tri-State Time	t_{HIZ}		-	-	100	ns

Notes

1. This pin has an on-chip 1.0MΩ pullup resistor.
2. An a.c. coupled sine or squarewave.
3. See Table 1, Tone Decode Frequencies.
4. Delay between the change of input (Tone/NOTONE) and the change at the Q0 - Q3 outputs.
5. The signal input maximum value is determined by the formula $V_{DD}/2.83$.

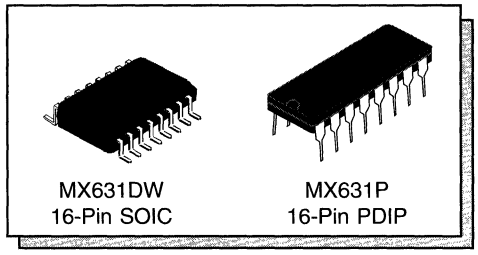
8

Advance Information

LOW VOLTAGE SPM DETECTOR

Features

- **Detects 12 & 16kHz SPM Frequencies**
- **Low Power (3.0 Volt$_{MIN}$ <1.0mA) Operation**
- **High Speechband Rejection Properties**
- **Tone-Follower and Packet Mode Outputs**
- **Applications**
  - **Complex and/or Simple Telephone Systems**
  - **Call-Charge/-Logging Systems**



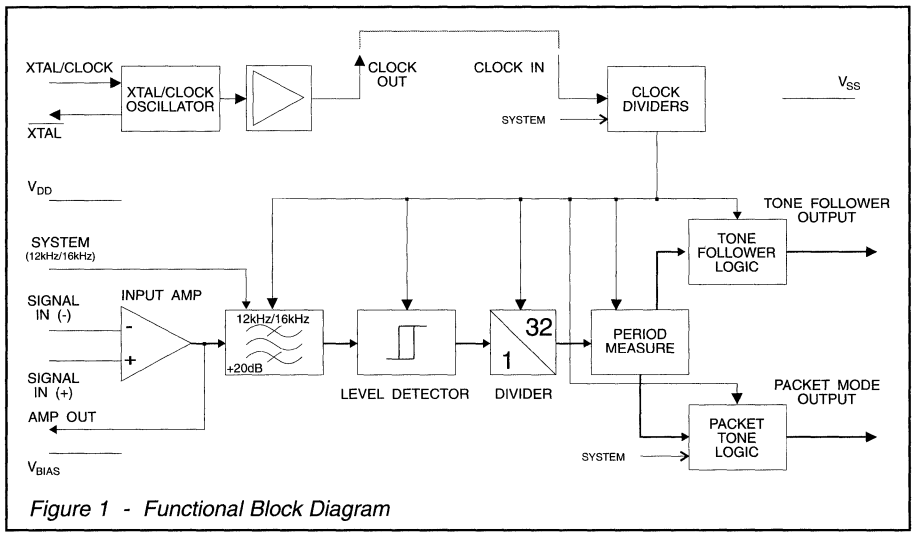


Figure 1 - Functional Block Diagram

Description

The MX631 is a low-power, system-selectable Subscriber Pulse Metering (SPM) detector that indicates the presence of both 12kHz or 16kHz telephone call-charge frequencies on a telephone line.

Deriving its input directly from the telephone line, input amplitude/sensitivities are component adjustable to the user's national 'Must/Must-Not Decode' specifications via an on-chip input amplifier, while the 12kHz and 16kHz frequency limits are accurately defined by the use of an external 3.579545MHz telephone-system Xtal or clock-pulse input.

The MX631, which demonstrates high 12kHz and 16kHz performance in the presence of both voice and noise, can operate from either a single or differential analog signal input from which it will produce two individual logic outputs:

1. Tone Follower Output - A 'tone-following' logic output producing a "Low" level for the period of a correct decode and a "High" level for a bad decode or NOTONE.
2. Packet (Cumulative Tone) Mode Output - To respond and/or de-respond after a cumulative 40ms of good tone (or NOTONE) in any 48ms period. This process will ignore small fluctuations or fades of a valid frequency input and is available for µProcessor 'Wake-Up', Minimum Tone detection, NOTONE indication or transient avoidance.

This system (12kHz/16kHz) selectable integrated circuit, which may be line-powered, is available in 16-pin plastic DIP and SOIC surface mount packages.

8

Pin	Function
1	**Xtal/Clock :** The input to the on-chip clock oscillator; for use with a 3.579545MHz Xtal in conjunction with the $\overline{\text{Xtal}}$ output (see Figure 2). Circuit components are on-chip. Using this mode of clock operation, the Clock Out pin should be connected directly to the Clock In pin. If a clock pulse input is employed to the Clock In pin, this pin must be connected directly to V_{DD} (see Figure 2).
2	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator inverter.
3	**Clock Out:** The buffered output of the on-chip clock oscillator inverter. If a Xtal input is employed this output should be connected directly to the Clock In pin.
4	**Clock In:** The 3.579545MHz clock pulse input to the internal clock-dividers. In the clock pulse input mode the Xtal/Clock input (pin 1) should be connected to V_{DD}. (See Figure 2.)
5	No internal connection, leave open circuit.
6	No internal connection, leave open circuit.
7	**V_{BIAS}:** The output of the on-chip analog bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to V_{SS} (see Figure 2).
8	**V_{SS}:** Negative supply (GND).
9 10 11	**Signal In (+):** **Signal In (-):** **Amp Out:** The positive and negative inputs to, and the output from, the input gain adjusting signal amplifier. Refer to Figure 4 for guidance on setting level sensitivities to national specifications, and the selection of gain adjusting components.
12	No internal connection, leave open circuit.
13	**Tone Follower Output:** This output provides a logic "0" (Low) for the period of a detected tone and a logic "1" (High) for NOTONE detection. See Figure 5.
14	**Packet Mode Output:** A logic output that will be available after a cumulation of 40ms of 'good' tone has been received. This packet tone follower will only respond when a tone frequency of sufficient quality has been received for sufficient time, i.e. a cumulation of 40ms in any 48ms; short tone bursts or breaks will be ignored. This output provides a logic "0" (Low) for a detected tone and a logic "1" (High) for NOTONE detection. See Figure 6.
15	**System:** The logic input to select device operation to either 12kHz (logic "1" - High) or 16kHz (logic "0" - Low) SPM systems. This input has an internal 1MΩ pullup resistor (12kHz).
16	**V_{DD}:** Positive supply. A single, stable power supply is required. Critical levels and voltages within the MX631 are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the pin. Note that if this device is 'line' powered, the resulting supply must be stable. See notes on IC Protection from high and spurious line voltages.

8

Application Information: External Components

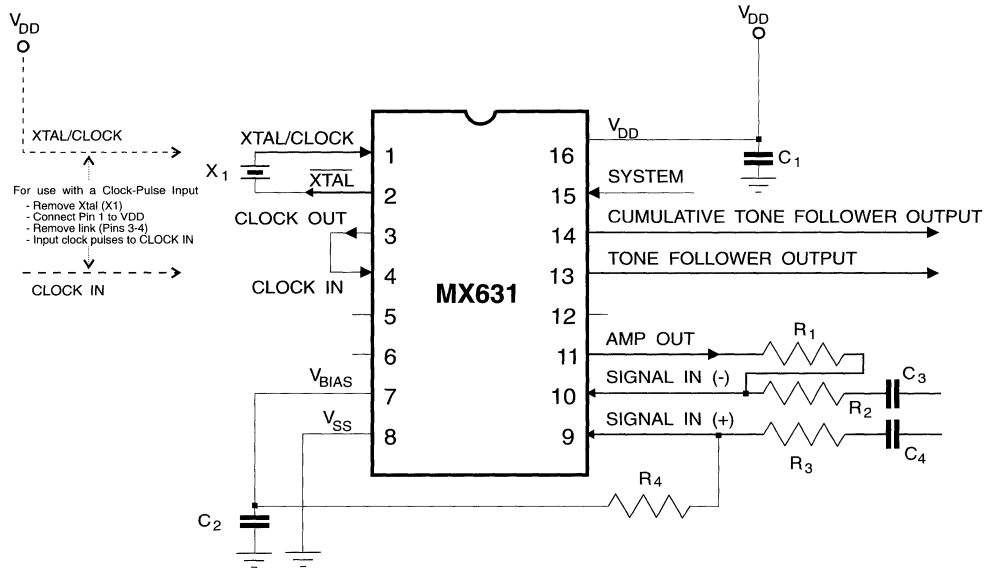


Figure 2 - Recommended External Components - Differential Input Mode

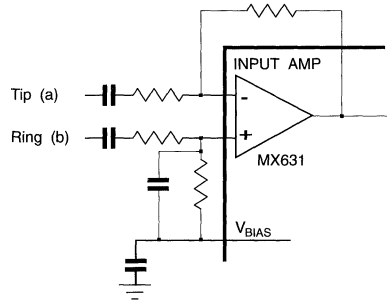
Component	Value
R_1	$R_{FEEDBACK}$
R_2	$R_{IN(-)}$
R_3	$R_{IN(+)}$
R_4	R_{BIAS}
C_1	1.0µF ±20%
C_2	1.0µF ±20%
C_3	$C_{IN(-)}$
C_4	$C_{IN(+)}$
X_1	3.579545MHz

External Components

1. The values of the Input Amp gain components illustrated are calculated using the Input Gain Calculation Graph (Figure 4).
   When calculating input gain components, for correct operation, it is recommended that the values of resistors R_1 and R_4 do not go below 100kΩ.

2. Refer to following pages for advice on IC Protection from high and spurious line voltages.

Differential Input



Common Mode Input

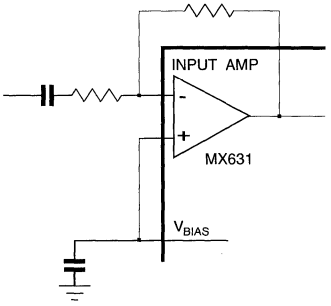


Figure 3 - Example Input Configurations

Application Information .....

Application Information .....

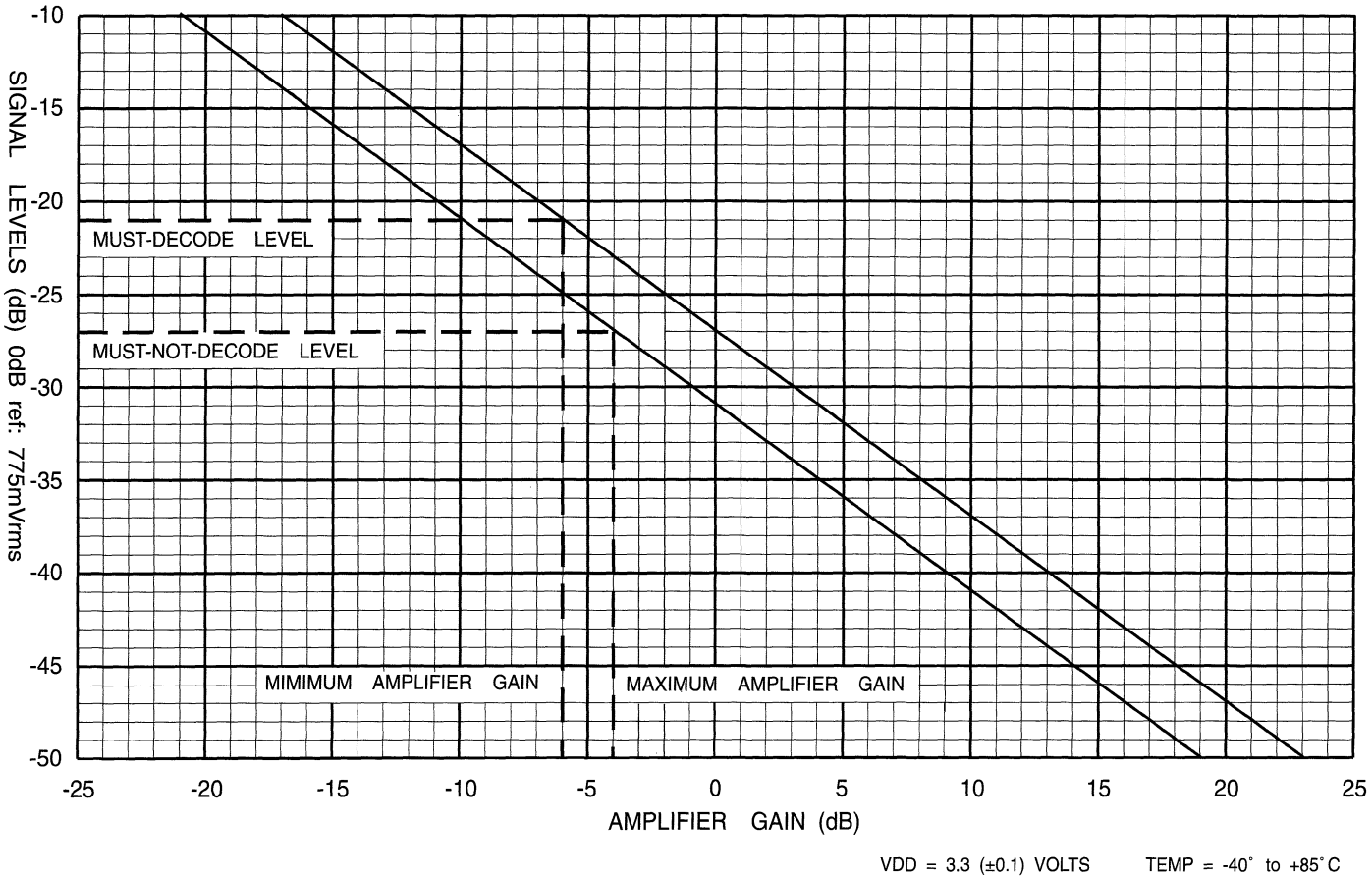


Figure 4 - Input Gain Calculation Graph

Application Information .....

Input Gain Calculation

The input amplifier, with its external circuitry, is provided on-chip to set the sensitivity of the MX631 to conform to the user's national level specification with regard to 'Must' and 'Must-Not' decode signal levels.

With reference to Figure 4, the following steps will assist in the determination of the required gain/ attenuation.

Step 1

Draw two horizontal lines from the Y-axis (Signal Levels (dB)). The upper line represents your required 'Must' decode level. The lower line represents your required 'Must-Not' decode level.

Step 2

Mark the intersection of the upper horizontal line and the upper sloping line; drop a vertical line from this point to the X-axis (Amplifier Gain (dB)).

The point where the vertical line meets the X-axis indicates the MINIMUM Input Amp gain required for reliable decoding of valid signals.

Step 3

Mark the intersection of the lower horizontal line and the lower sloping line; drop a vertical line from this point to the X-axis.

The point where the vertical line meets the X-axis indicates the MAXIMUM allowable Input Amp gain.

Input signals at or below the 'Must-Not' decode level will not be detected as long as the amplifier gain is no higher than this level.

Input Gain Components

The following paragraphs refer to the gain components shown in Figures 2 and 3.

The user should calculate and select external components (R_1, R_2/C_3, R_3/C_4, R_4) to provide an amplifier gain within the limits obtained in Steps 2 and 3.

Component tolerances should not move the gain-figure outside these limits.

It is recommended that the designed gain is near the center of the calculated range. The graph in Figure 4 is for calculations for the input gain components for an MX631 using a V_{DD} of 3.3 (±0.1) volts.

Use this area to keep a permanent record of your calculated gains and components

Implementation Notes

Aliasing

Due to the switched-capacitor filters employed in the MX631, be careful to avoid the effects of alias distortion with the external components you choose.

Possible Alias Frequencies:
12kHz Mode= 52kHz
16kHz Mode= 69kHz

If these alias frequencies are liable to cause problems and/or interference, it is recommended that anti-alias capacitors are used across input resistors R_1 and R_4.

Values of anti-alias capacitors should be chosen to provide a highpass cutoff frequency, in conjunction with R_1 (R_4) of approximately 20kHz to 25kHz (12kHz system) or 25kHz to 30kHz (16kHz system).

$$\text{i.e. } C = \frac{1}{2 \times \pi \times f_0 \times R_1}$$

When anti-alias capacitors are used, make allowance for reduced gain at the SPM frequency (12kHz or 16kHz).

Signal Input Protection

Telephone systems may have high d.c. and a.c. voltages present on the line. If the MX631 is part of host equipment that has its own signal input protection circuitry, there will be no need for further protection as long as the voltage on any pin is limited to within V_{DD} + 0.3V and V_{SS} -0.3V.

If the host system does not have input protection, or there are signals present outside the device's specified limits, the MX631 will require protection diodes at its signal inputs (+ and -). The breakdown voltage of capacitors and the peak inverse voltage of the diodes must be sufficient to withstand the sum of the d.c. voltages plus all expected signal peaks.

8

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} +0.3V)
Sink/source current (supply pins)	±30mA
(other pins)	±20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage temperature range	-40°C to +85°C

Functional Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 3.3V

T_{AMB} = +25 °C

Audio Level 0dB ref: = 775mVrms

Noise Bandwidth = 50kHz

Xtal/Clock or 'Clock In' Frequency = 3.579545MHz

12kHz or 16kHz System Setting

Characteristics	See Note	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD}) at 25°C		3.0	-	5.5	V
Supply Current		-	-	1.0	mA
Input Logic "1" (High)		2.3	-	-	V
Input Logic "0" (Low)		-	-	1.0	V
Output Logic "1" (High)		2.9	-	-	V
Output Logic "0" (Low)		-	-	0.4	V
Xtal/Clock or Clock In Frequency		3.558918	-	3.589368	MHz
"High" External Clock Pulse Width		0.1	-	-	µs
"Low" External Clock Pulse Width		0.1	-	-	µs
Input Amp					
D.C. Gain		60.0	-	-	dB
Bandwidth (-3dB open loop)		-	100	-	Hz
Input Impedance		-	1.0	-	MΩ
Logic Impedances					
Input (System)		0.7	-	3.8	MΩ
(Clock In)		10.0	-	-	MΩ
Output		-	14.0	30.0	kΩ
Overall Performance					
12kHz Detect Bandwidth	1	11.820		12.180	kHz
12kHz Not-Detect Frequencies (below 12kHz)	1	-	-	11.520	kHz
12kHz Not-Detect Frequencies (above 12kHz)	1	12.480	-	-	kHz
16kHz Detect Bandwidth	1	15.760		16.240	kHz
16kHz Not-Detect Frequencies (below 16kHz)	1	-	-	15.360	kHz
16kHz Not-Detect Frequencies (above 12kHz)	1	16.640	-	-	kHz
Sensitivity	2	7.8	10.0	15.5	mVp-p
Tone Operation Characteristics					
Signal-to-Noise Requirements (Amp Input)	3,4,5,6	22.0	20.0	-	dB
Signal-to-Voice Requirements (Amp Input)	3,4,5,7	-36.0	-40.0	-	dB
Signal-to-Voice Requirements (Amp Output)	5,6	-25.0	-	-29.0	dB
Tone Follower Output					
Response and De-Response Times	1,8	-	-	10.0	ms
Packet Mode Output					
Response and De-Response Times	1,8	40.0	-	48.0	ms

8

Characteristics Notes

1. With adherence to Signal-to-Voice and Signal-to Noise specifications.
2. With Input Amp gain setting: $15.5dB_{MIN}/19.5dB_{MAX}$.
3. Common Mode SPM and balanced voice signal.
4. Immune to false responses.
5. Immune to false de-responses
6. With SPM and voice signal amplitudes balanced; To avoid false de-responses due to saturation, the peak-to-peak voice+noise level at the output of the Input Amp (12/16kHz Filter Input) should be no greater than the dynamic range of the device.
7. Maximum voice frequencies = 3.4kHz
8. Response, De-Response and Power-up Response Timing.

Application Information .....

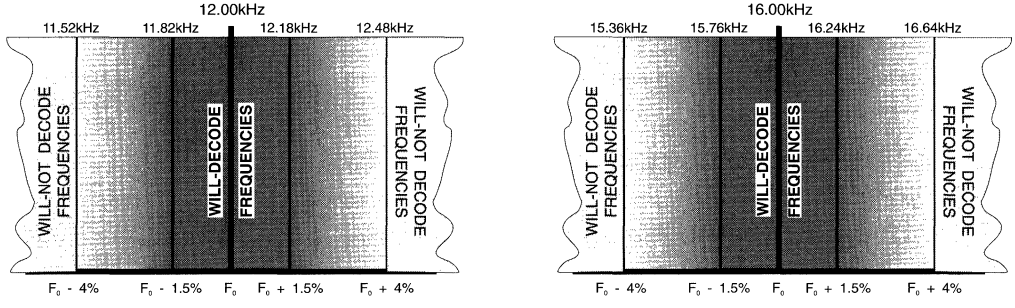


Figure 5 - Will/Will-Not Decode Frequencies

System Timing

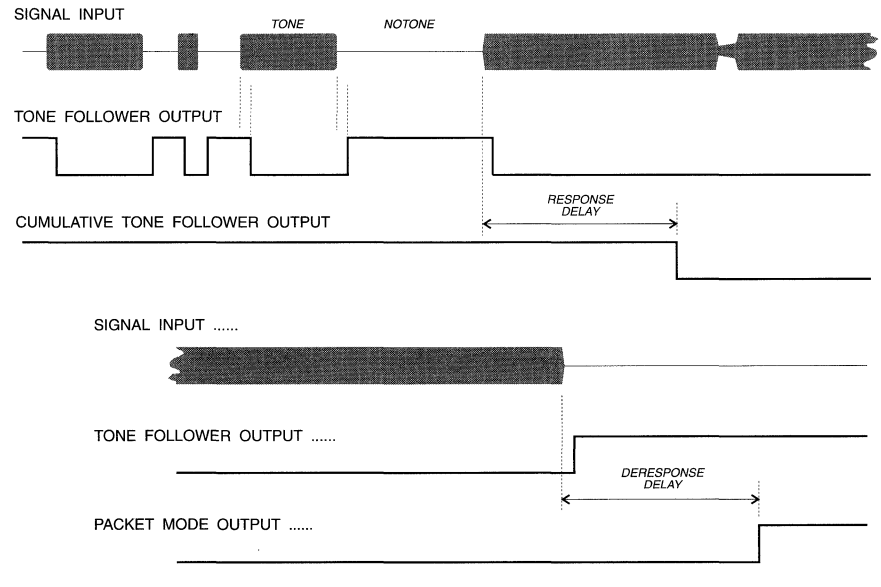


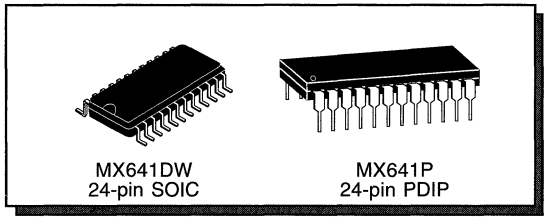
Figure 6 - Examples of Input and Output Relationships

Advance Information

DUAL SUBSCRIBER PRIVATE METERING (SPM) DETECTOR

Features

- **MX•COM MiXed Signal CMOS**
- **Two (12kHz/16kHz) SPM Detectors on a Single Chip**
- **Detects 12 or 16kHz SPM Frequencies**
- **"Controlled" (µC) & "Fixed" Signal Sensitivity Modes**
- **Selectable Tone Follower or Packet Mode Outputs**
- **High Speech-Band Rejection Properties**
- **"Output Enable" Multiplexing Facility**
- **Call-Charge Applications on PABX Line Cards**



MX641DW
24-pin SOIC

MX641P
24-pin PDIP

Description

The MX641 low-power, system-selectable Dual Subscriber Private Metering (SPM) Detector has *two detectors on a single chip* to indicate the presence, on a telephone line, of either 12kHz or 16kHz telephone call-charge frequencies. It is is designed for PBX and PABX line-card and remote telephone installations.

Under µProcessor control via a common serial interface, each channel of the MX641 will detect call-charge pulses from a telephone line and provide a digital output for recording, billing or security purposes.

A common set of external components and a stable 3.579545MHz Xtal/clock input ensures that the MX641 adheres accurately to most national "Must and Must-Not" decode band-edges and threshold levels.

The digital output is pin-selectable to one of three modes:

(1) Tone Follower mode -a logic level for the period of a correct decode.

(2) Packet mode -respond/ de-respond after a cumulative period of tone or notone in a preset period.

(3) High-impedance output -for device multiplexing.

For non-µProcessor systems a preset sensitivity/ system input allows external channel level and system setting.

The MX641 is available in 24-pin plastic DIP and small outline (SOIC) packages. It requires a supply of 4.5mA at 5 volts.

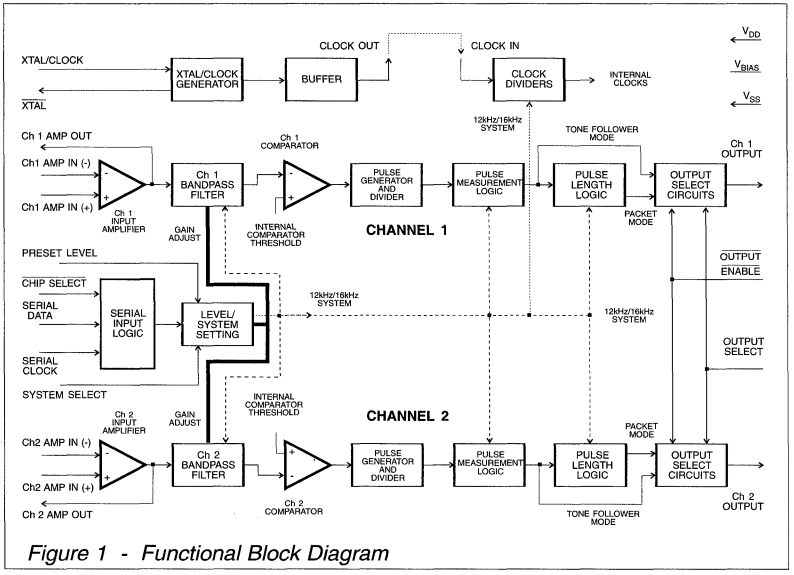


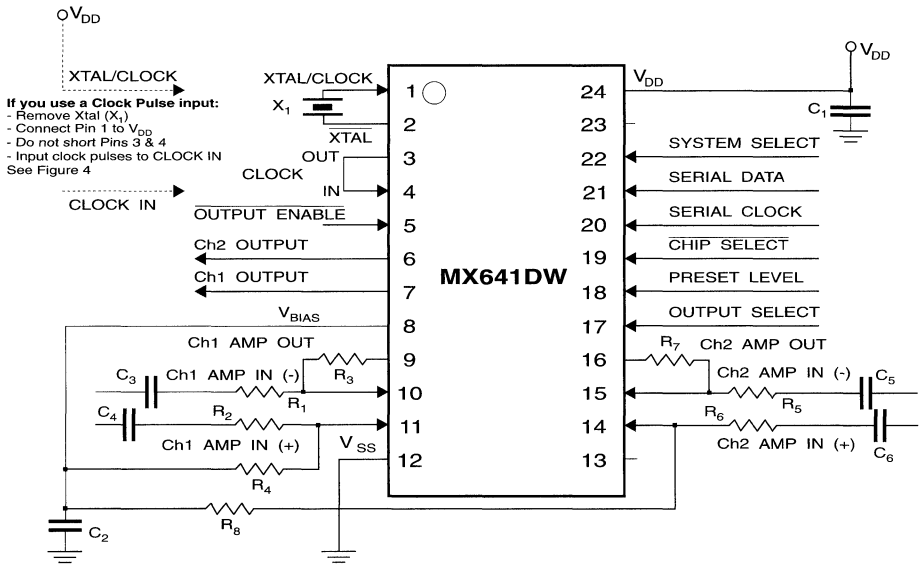
Figure 1 - Functional Block Diagram

Pin	Function
1	**Xtal/Clock:** The input to the on-chip clock oscillator; for use with a 3.579545MHz Xtal in conjunction with the $\overline{\text{Xtal}}$ output; circuit components are on-chip. When using a Xtal input, the Clock Out pin should be connected directly to the Clock In pin. If a clock pulse input is used at the Clock In pin, this (Xtal/Clock) pin must be connected directly to V_{DD} (see Figure 2). See Figure 4 for details of clock frequency distribution.
2	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator inverter.
3	**Clock Out:** The buffered output of the on-chip-clock oscillator inverter. If a Xtal input is used, this output should be connected directly to the Clock In pin. This output can support up to 3 additional MX641 ICs. See Figure 4 for details of clock frequency distribution.
4	**Clock In:** The 3.579545 clock pulse input to the internal clock dividers. If an externally generated clock pulse input is used, the Xtal/Clock input pin should be connected to V_{DD}.
5	**$\overline{\text{Output Enable}}$:** For multi-chip output multiplexing; controls the state of both Ch1 and Ch2 outputs. When this input is placed high (logic '1') both outputs are set to a high impedance. When placed low (logic '0') both outputs are enabled.
6	**Ch 2 Output:** The digital output of the Channel 2 SPM detector when enabled. The format of the signal at this pin, in common with Ch 1, is selectable to either 'Tone Follower' or 'Packet' mode via the Output Select input.
7	**Ch 1 Output:** The digital output of the Channel 1 SPM detector when enabled. The format of the signal at this pin, in common with Ch 2, is selectable to either 'Tone Follower' or 'Packet' mode via the Output Select input.
8	**V_{BIAS}:** The output of the on-chip analog bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to V_{SS} (see Figure 2).
9	**Ch 1 Amp Out:** The output of the Channel 1 Input Amplifier. See Figures 2 and 3.
10	**Ch 1 Amp In (-):** The negative input to the Channel 1 Input Amplifier. See Figures 2 and 3.
11	**Ch 1 Amp In (+):** The positive input to the Channel 1 Input Amplifier. See Figures 2 and 3.
12	**V_{SS}:** Negative supply rail (GND).

Pin	Function
13	No internal connection; leave open circuit.
14	**Ch 2 Amp In (+):** The positive input to the Channel 2 Input Amplifier. See Figures 2 and 3.
15	**Ch 2 Amp In (-):** The negative input to the Channel 2 Input Amplifier. See Figures 2 and 3.
16	**Ch 2 Amp Out:** The output of the Channel 2 Input Amplier. See Figures 2 and 3.
17	**Output Select:** A logic input to set the Channel 1 and Channel 2 output modes. When high (logic '1'), the outputs are in the Tone Follower mode; when low (logic '0'), the outputs are in the Packet mode.
18	**Preset Level:** A logic input to set the sensitivity mode of the MX641. When high (logic '1'), both channels are in the Fixed Sensitivity mode. The external components govern the input sensitivity; the System Select input selects 12kHz or 16kHz operation. When low (logic '0'), both channels are in the Controlled Sensitivity mode. Device sensitivities and system selection are via the Chip Select/Serial Data/Serial Clock inputs. This input has an internal pullup resistor on chip (Fixed Sensitivity Mode).
19	**$\overline{\text{Chip Select}}$:** The Chip Select input for use in data loading when using the MX641 in the Controlled Sensitivity mode (see Figure 9). The device is selected when this input is set low (logic '0'). When the MX641 is in the Fixed Sensitivity mode this input should be connected to either V_{SS} or V_{DD}.
20	**Serial Clock:** The Serial Clock input for use in data loading when using the MX641 in the Controlled Sensitivity mode (see Figure 9). Data is loaded to the MX641 on this clock's rising edge. When the MX641 is in the Fixed Sensitivity mode this input should be connected to either V_{SS} or V_{DD}.
21	**Serial Data:** The Serial Data input for use in data loading when using the MX641 in the Controlled Sensitivity mode (see Figure 9 and Table 2). When the device is in the Fixed Sensitivity mode this input should be connected to either V_{SS} or V_{DD}.
22	**System Select:** In the Fixed Sensitivity mode this pin selects the system frequency. High (logic '1') = 12kHz; Low (logic '0') = 16kHz. In the Controlled Sensitivity mode this pin is inactive and may be left unconnected. This pin has an internal pullup resistor on chip.
23	No internal connection; leave open circuit.
24	**V_{DD}:** Positive supply rail; a single, stable power supply is required. Critical levels and voltages within the MX641 are dependant upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the pin.

8

Application Information



Component	Value	Tolerance			
R_1	68kΩ	± 1%	C_1	1.0µF	±20%
R_2	68kΩ	±1%	C_2	1.0µF	±20%
R_3	820kΩ	±1%	C_3	270pF	±5%
R_4	820kΩ	±1%	C_4	270pF	±5%
R_5	68kΩ	± 1%	C_5	270pF	±5%
R_6	68kΩ	± 1%	C_6	270pF	±5%
R_7	820kΩ	±1%			
R_8	820kΩ	±1%	X_1	3.579545MHz	

Figure 2 - Recommended External Components

Fixed Sensitivity Setting

Note that when calculating/selecting gain components, R_3, R_4, R_7 and R_8 should always be greater than or equal to 100kΩ.

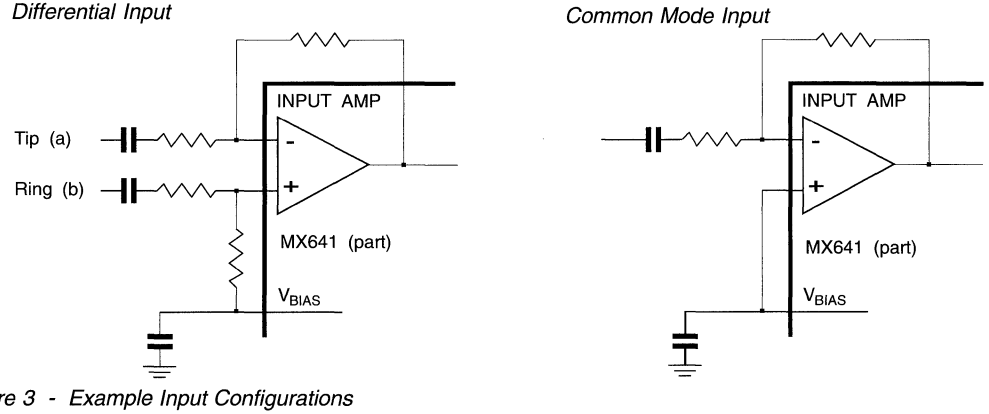
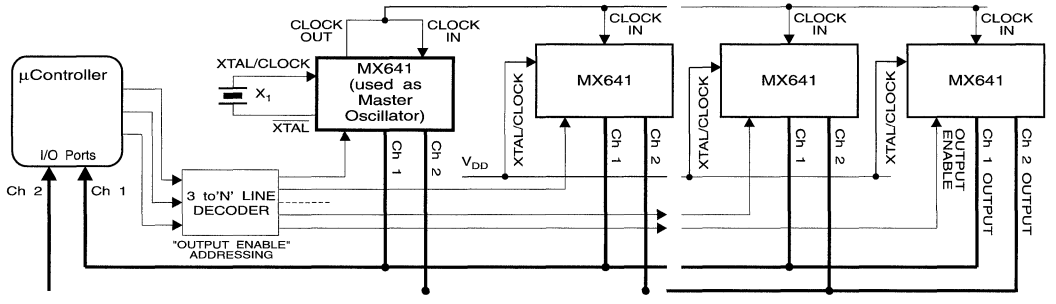


Figure 3 - Example Input Configurations



Maximum number of driven clocks (including Master) = 4
Maximum capacitive load on Clock Out output = 15.0pF

Figure 4 - Examples of Xtal/Clock Distribution and Output Multiplexing

Xtal/Clock Distribution

The MX641 requires a 3.579545MHz Xtal or clock pulse input. With the exception of the Xtal, all oscillator components are incorporated on chip. If a Xtal input is employed the Clock Out pin should be directly linked to the Clock In pin.

To reduce component and layout complexity, the clock requirements of up to 3 additional MX641 microcircuits may be supplied from a Xtal-driven MX641 acting as the system master clock. With reference to Figure 4, the clock should be distributed as illustrated and the Xtal/Clock pins of the driven microcircuits should be connected directly to V_{DD}. Note that the maximum load on the master Clock Out pin should not be exceeded.

Channel Outputs

Channels 1 and 2 outputs operate together under the control of the Output Enable and Output Select inputs. Table 3 describes the operations.

The Front Page description describes the output formats.

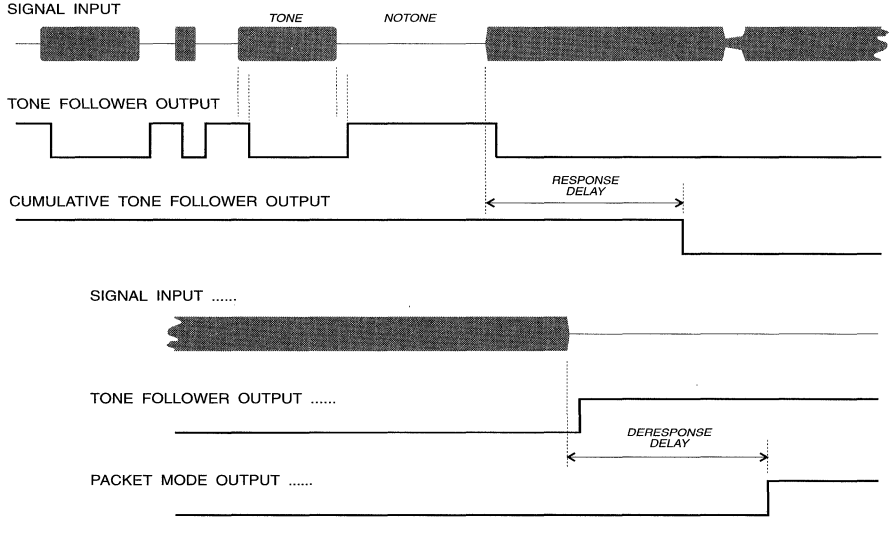


Figure 5 - Tone Follower and Packet Mode Outputs

Sensitivity Setting

To enable the MX641 to operate correctly to most national 12kHz and 16kHz SPM specifications, the input sensitivity can be accurately adjusted and set.

There are two different pin-selectable modes of sensitivity setting available to the MX641: Controlled Sensitivity Mode and Fixed Sensitivity Mode

The Controlled Sensitivity mode allows the sensitivity setting from a µController via a 6-bit serial data input. This same serial input also sets operation (bit 0) to either 12kHz or 16kHz systems. Both channels are set identically.

The Fixed Sensitivity mode allows the sensitivity of each channel to be set to a fixed "gain" by external components at the input amplifiers. Operation to either 12kHz or 16kHz is by the System Select input.

Controlled Sensitivity Setting

Serial Data Bits D_5 - D_1	Bandpass Filter Gain (dB)	12kHz System Bit D_0 = '1' Minimum Sensitivity dB(ref.)	12kHz System Bit D_0 = '1' Nominal Sensitivity dB(ref.)	12kHz System Bit D_0 = '1' Maximum Sensitivity dB(ref.)	16kHz System Bit D_0 = '0' Minimum Sensitivity dB(ref.)	16kHz System Bit D_0 = '0' Nominal Sensitivity dB(ref.)	16kHz System Bit D_0 = '0' Maximum Sensitivity dB(ref.)
0 0 0 0 0	0	-16.2	-17.5	-18.8	-16.9	-18.2	-19.5
0 0 0 0 1	1.0	-17.2	-18.5	-19.8	-17.9	-19.2	-20.5
0 0 0 1 0	2.0	-18.2	-19.5	-20.8	-18.9	-20.2	-21.5
0 0 0 1 1	3.0	-19.2	-20.5	-21.8	-19.9	-21.2	-22.5
0 0 1 0 0	4.0	-20.2	-21.5	-22.8	-20.9	-22.2	-23.5
0 0 1 0 1	5.0	-21.2	-22.5	-23.8	-21.9	-23.2	-24.5
0 0 1 1 0	6.0	-22.2	-23.5	-24.8	-22.9	-24.2	-25.5
0 0 1 1 1	7.0	-23.2	-24.5	-25.8	-23.9	-25.2	-26.5
0 1 0 0 0	8.0	-24.2	-25.5	-26.8	-24.9	-26.2	-27.5
0 1 0 0 1	9.0	-25.2	-26.5	-27.8	-25.9	-27.2	-28.5
0 1 0 1 0	10.0	-26.2	-27.5	-28.8	-26.9	-28.2	-29.5
0 1 0 1 1	11.0	-27.2	-28.5	-29.8	-27.9	-29.2	-30.5
0 1 1 0 0	12.0	-28.2	-29.5	-30.8	-28.9	-30.2	-31.5
0 1 1 0 1	13.0	-29.2	-30.5	-31.8	-29.9	-31.2	-32.5
0 1 1 1 0	14.0	-30.2	-31.5	-32.8	-30.9	-32.2	-33.5
0 1 1 1 1	15.0	-31.2	-32.5	-33.8	-31.9	-33.2	-34.5
1 0 0 0 0	16.0	-32.2	-33.5	-34.8	-32.9	-34.2	-35.5
1 0 0 0 1	17.0	-33.2	-34.5	-35.8	-33.9	-35.2	-36.5
1 0 0 1 0	18.0	-34.2	-35.5	-36.8	-34.9	-36.2	-37.5
1 0 0 1 1	19.0	-35.2	-36.5	-37.8	-35.9	-37.2	-38.5
1 0 1 0 0	20.0	-36.2	-37.5	-38.8	-36.9	-38.2	-39.5
1 0 1 0 1	21.0	-37.2	-38.5	-39.8	-37.9	-39.2	-40.5
1 0 1 1 0	22.0	-38.2	-39.5	-40.8	-38.9	-40.2	-41.5
1 0 1 1 1	23.0	-39.2	-40.5	-41.8	-39.9	-41.2	-42.5
1 1 0 0 0	24.0	-40.2	-41.5	-42.8	-40.9	-42.2	-43.5
1 1 0 0 1	25.0	-41.2	-42.5	-43.8	-41.9	-43.2	-44.5
1 1 0 1 0	26.0	-42.2	-43.5	-44.8	-42.9	-44.2	-45.5
1 1 0 1 1	27.0	-43.2	-44.5	-45.8	-43.9	-45.2	-46.5
1 1 1 0 0	28.0	-44.2	-45.5	-46.8	-44.9	-46.2	-47.5
1 1 1 0 1	29.0	-45.2	-46.5	-47.8	-45.9	-47.2	-48.5
1 1 1 1 0	30.0	-46.2	-47.5	-48.8	-46.9	-48.2	-49.5
1 1 1 1 1	31.0	-47.2	-48.5	-49.8	-47.9	-49.2	-50.5

Table 2 - Controlled Sensitivity Setting Information

Notes:
1. The recommended amplifier components (see Figure 2) are used, providing an amplifier gain at 16kHz of 20.5dB ±0.3dB or at 12kHz of 19.8dB ±0.3dB.
2. A comparator sensitivity of 2.3dB(ref.) ±1dB (the variation is due to filter gain error, filter output offset, comparator input offset or a combination of all 3).
3. The applied V_{DD} is 5.0 volts; 0dB (ref.) = 775mVrms.

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Controlled Sensitivity Setting .....

With the external gain (sensitivity) components used as shown in Figure 2, the gain of the input stages is 19.8dB (12kHz) or 20.5dB (16kHz). For controlled sensitivity setting the gain of each bandpass filter, and therefore the device sensitivity, is adjusted by the applied serial bits D_1 to D_5.

In the Controlled Sensitivity mode the system frequency is selected by bit D_0 ('1' = 12kHz; '0' = 16kHz). Data is loaded Bit 5 (D_5) first. Table 2 details the serial data inputs for the required sensitivity. Minimum, Nominal and Maximum Sensitivity figures are provided to make complete allowance for internal circuit offsets and component tolerances. 0dB(ref.) = 775mVrms at V_{DD} = 5.0 volts; varies directly with V_{DD}. Examples are provided as a guide to meeting different national specifications.

German FTZ Specification 16kHz

The FTZ system has a Must Decode level of -21dB (ref.) and a Must-Not Decode level of -27dB (ref.). Reference to Table 2 shows that Bandpass Filter Gain settings of 5dB, 6dB or 7dB will enable an MX641 channel to meet this level specification. Figure 6 illustrates the range of these various settings.

To meet the German FTZ specification, the input data (D_5 to D_0) can be:

	0 0 1 0 1	**0**	**5.0dB**
or	***0 0 1 1 0***	***0***	***6.0dB***
or	**0 0 1 1 1**	**0**	**7.0dB**

Selecting the middle setting would give the greatest noise immunity.

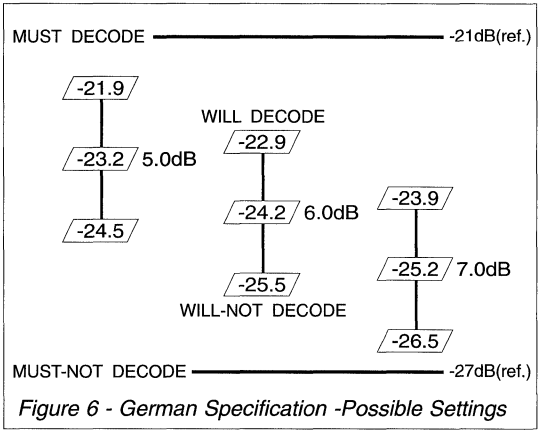


Figure 6 - German Specification -Possible Settings

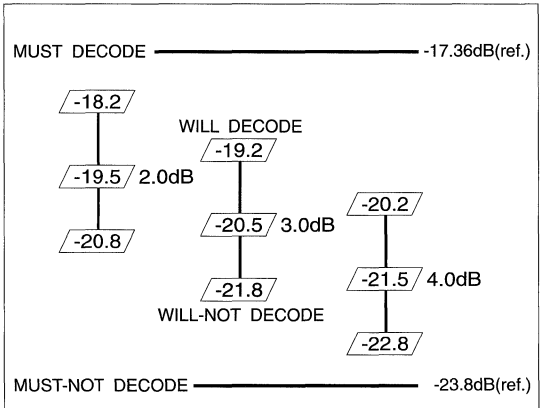


Figure 7 - French Specification -Possible Settings

French Specification 12kHz

This system has a Must Decode level of -17.36dB (ref.) and a Must-Not Decode level of -23.8dB (ref.). Reference to Table 2 shows that Bandpass Filter Gain settings of 2dB, 3dB or 4dB will enable an MX641 channel to meet this level specification. Fig 7 illustrates the range of these various settings.

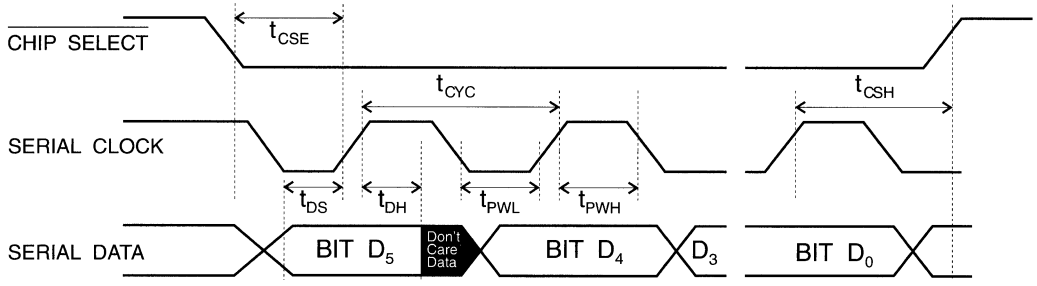
To meet the French SPM specification, the input data (D_5 to D_0) can be:

	0 0 0 1 0	**1**	**2.0dB**
or	***0 0 0 1 1***	***1***	***3.0dB***
or	**0 0 1 0 0**	**1**	**4.0dB**

Selecting the middle setting would give the greatest noise immunity.

System Select	Preset Level	Output Select	Output Enable	Operating Mode	
X	0	0	0	Packet Mode Output;	Serial Data Control
X	0	1	0	Tone Follower Output;	Serial Data Control
0	1	0	0	Packet Mode Output;	Preset Sensitivity 16kHz
1	1	0	0	Packet Mode Output;	Preset Sensitivity 12kHz
0	1	1	0	Tone Follower Output;	Preset Sensitivity 16kHz
1	1	1	0	Tone Follower Output;	Preset Sensitivity 12kHz
X	X	X	1	Tristate Output	High Z

Table 3 Operating Mode Configurations *X = don't care*



Parameter		Min.	Typ.	Max.	Unit
t_{PWH}	Serial Clock 'High' Pulse Width	250	-	-	ns
t_{PWL}	Serial Clock 'Low' Pulse Width	250	-	-	ns
t_{CYC}	Serial Clock Period	600	-	-	ns
t_{CSE}	Chip Select 'Low' to Clock 'High' Edge	450	-	-	ns
t_{DH}	Data Hold Time	50.0	-	-	ns
t_{DS}	Data Setup Time	250	-	-	ns

Figure 8 - Data Load Timing for the Controlled Sensitivity Mode

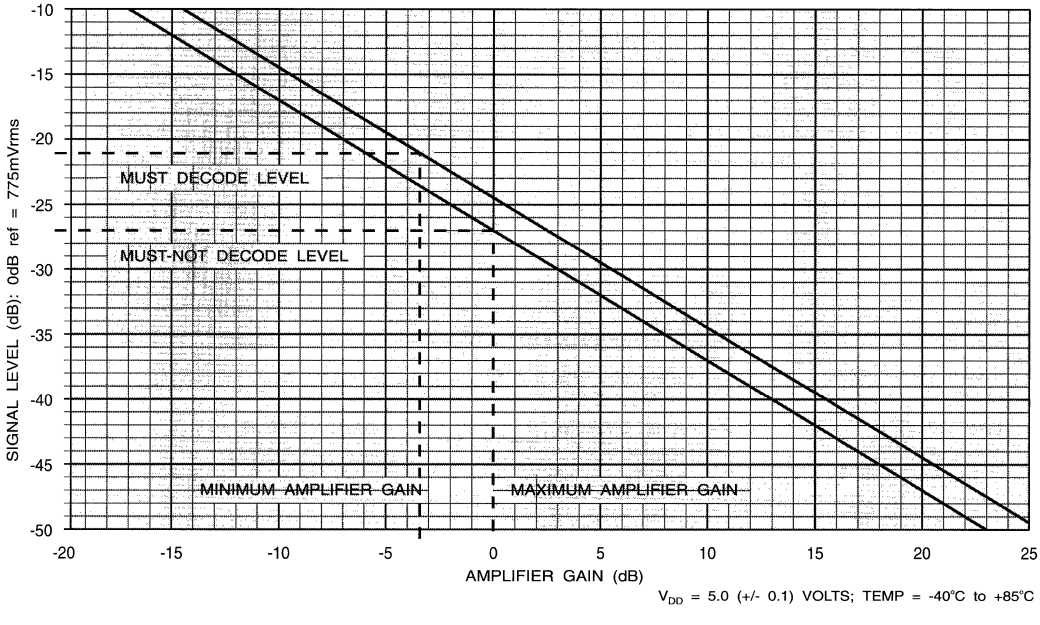


Figure 9 - Input Gain Calculation Graph for use in the Fixed Sensitivity Mode

Fixed Sensitivity Setting

In this mode the sensitivity of each channel is set by the correct selection of the components around the Channel Input Amplifier. Note that the device sensitivity is directly proportional to the applied power supply (V_{DD}).

Input Gain Calculation

The input amplifier, with external circuitry, is used to set the sensitivity of the MX641 to conform to the user's national level specification with regard to 'Must' and 'Must-Not' decode signal levels.

With reference to the graph in Figure 9, the following steps will assist in the determination of the required gain/ attenuation.

Step 1

Draw two horizontal lines from the Y-axis (Signal Level) in Figure 9. The upper line represents your required 'Must' decode level. The lower line represents your required 'Must-Not' decode level.

Step 2

Mark the intersection of the upper horizontal line and the upper sloping line; drop a vertical line from this point to the X-axis (Amplifier Gain (dB)).

The point where the vertical line meets the X-axis indicates the MINIMUM Input Amp gain required for reliable decoding of valid signals.

Step 3

Mark the intersection of the lower horizontal line and the lower sloping line; drop a vertical line from this point to the X-axis.

The point where the vertical line meets the X-axis will indicate the MAXIMUM allowable Input Amp gain.

Input signals at or below the 'Must-Not' decode level will not be detected as long as the amplifier gain is no higher than this level.

Select the *Input Gain Components* as described.

Input Gain Components

Refer to the gain components shown in Figure 2. The user should calculate and select external components ($R_1/R_3/C_3$, $R_2/R_4/C_4$ and $R_5/R_7/C_5$, $R_6/R_8/C_6$) to provide amplifier gains within the limits obtained in Steps 2 and 3.

Component tolerances should not move the gain-figure outside these limits. The graph in Figure 9 is for the calculation of input gain components for an MX641 using a V_{DD} of 5.0 (±0.1) volts.

It is recommended that the designed gain is near the center of the calculated range.

Protection Against High Voltages

Telephone systems may have high d.c. and a.c. voltages present on the line. If the MX641 is part of a host equipment that has its own signal input protection circuitry, there will be no need for further protection as long as the voltage on any pin is limited to within V_{DD} +0.3V and V_{SS} -0.3V.

If the host system does not have input protection, or there are signals present outside the device's specified limits, the MX641 will require protection diodes at its signal inputs (+ and -). The breakdown voltage of capacitors and the peak inverse voltage of the diodes must be sufficient to withstand the sum of the d.c. voltages plus all expected signal peaks.

Aliasing

Due to the sampling nature of switched-capacitor filters used in the MX641, high frequency noise or unwanted signals can alias into the passband, disrupting detection. External components must be chosen carefully to avoid alias effects.

Possible Alias Frequencies:

12kHz Mode = 52kHz
16kHz Mode = 69kHz

If other filtering in the system has not attenuated these alias frequencies, capacitors should be employed across resistors R_3, R_4, R_7 and R_8 to provide anti-alias filtering.

The lowpass cutoff frequency should be chosen to be approximately 20kHz to 25kHz for a 12kHz system, or 25kHz to 30kHz for a 16kHz system.

$$\text{i.e. } C = \frac{1}{2 \times \pi \times f_0 \times R_3}$$

When anti-alias capacitors are used, there will be reduced gain at the SPM frequency (12kHz or 16kHz).

8

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)	±30mA
(other pins)	±20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage temperature range	-40°C to +85°C

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V

T_{AMB} = +25 °C

Audio Level 0dB ref: = 775mVrms

Noise Bandwidth = 50kHz

Xtal/Clock or 'Clock In' Frequency = 3.579545MHz

12kHz or 16kHz System Setting

Characteristics	See Note	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD})		4.5	-	5.5	V
Supply Current		-	4.5	6.0	mA
Xtal/Clock/Clock In Frequency		3.558918	-	3.589368	MHz
Input/Output Parameters					
Clock Out Load		-	-	15.0	pF
Logic Inputs					
Input Logic '1' (High)		3.5	-	-	V
Input Logic '0' (Low)		-	-	1.5	V
Input Leakage Current (V_{IN} = 0 to V_{DD})	13	-5.0	-	5.0	µA
Input Current (V_{IN} = 0)	14	-15.0	-	-	µA
Channel Outputs					
Output Logic '1' (I_{OH}) = 120µA) (Enabled)	1	4.6	-	-	V
Output Logic '0' (I_{OL}) = 360µA) (Enabled)	1	-	-	0.4	V
Output Leakage Current (High-Z Output)	2	-5.0	-	5.0	µA
Input Amplifier					
D. C. Gain		60.0	-	-	dB
Bandwidth (-3dB)		-	100	-	Hz
Input Impedance		1.0	-	-	MΩ
Overall Performance					
12kHz Upper Decode Band Edge	3	12.18	-	12.48	kHz
12kHz Lower Decode Band Edge	3	11.82	-	11.52	kHz
16kHz Upper Decode Band Edge	3	16.24	-	16.64	kHz
16kHz Lower Decode Band Edge	3	15.76	-	15.36	kHz
Level Sensitivity					
Controlled Sensitivity Mode	3,4,12,15	3.3	2.3	1.3	dB(ref.)
Preset Sensitivity Mode	3,4,5,16	-24.7	-25.7	-26.7	dB(ref.)
Signal Quality Requirements					
Signal-to-Noise (Amp Input)	4,8,9,10	22.0	20.0	-	dB
Signal-to-Voice (Amp Input)	4,8,9,11	-36.0	-40.0	-	dB
Signal-to-Voice (Amp Output)	4,8,10,11	-25.0	-	-29.0	dB
Channel Outputs (Ch1 and Ch2) Figure 5					
Mode Change Time	6	-	-	500	ns
Tone Follower Mode (Table 3)					
Response and De-Response Time	3, 4, 7	-	-	10.0	ms
Packet Mode (Table 3)					
Response and De-Response Time	3, 4, 7	40.0	-	48.0	ms

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Specification Notes

1. Tone Follower or Packet mode enabled; see Table 3.
2. Tristate selected; see Table 3.
3. With adherence to Signal-to-Voice and Signal-to Noise specifications.
4. 12kHz and/or 16kHz system.
5. With Input Amp gain setting = 0dB.
6. Time taken to change between any two of the operational modes: Tone Follower, Packet or Tristate, and with a maximum capacitive load of 30pF on an output.
7. The time delay, after a valid serial data load (or after device powerup), before the condition of the outputs can be guaranteed correct.
8. Immunity to false responses and/or de-responses.
9. Common Mode SPM and balanced voice input signal.
10. With SPM and voice signal amplitudes balanced; To avoid false de-responses due to saturation, the peak-to-peak voice + noise level at the output of the Input Amp should be no greater than the dynamic range of the device.
11. Maximum voice frequencies = 3.4kHz.
12. With the Input Amplifier gain at 0dB and the Bandpass Filter gain set at 0dB (Table 2); subtract 1.0dB from this specification for each extra single dB of Bandpass Filter gain programmed.
    Alternatively, with the input components as recommended in Figure 2, the sensitivity is as defined in Table 2.
13. Logic inputs with no internal pullup; Chip Select, Serial Data, Serial Clock, Output Enable, Output Select and Clock In pins.
14. Logic inputs with an internal pullup; Preset Level and System Select pins.
15. Preset Level= '0', System Select = don't care; Chip Select, Serial Clock and Serial Data inputs active; see Table 3.
16. Preset Level = '1', System Select = input active; Chip Select, Serial Clock and Serial Data inputs inactive; see Table 3.

Section 9: Signal Processing

The following section contains specifications on MX•COM's devices used for signal processing.

Device	Description	Page
MX102	Autocorrelator	p. 503
MX105	Tone Detector	p. 509

MX-COM, INC. MX102

AUTOCORRELATING SIGNAL PROCESSOR

FEATURES

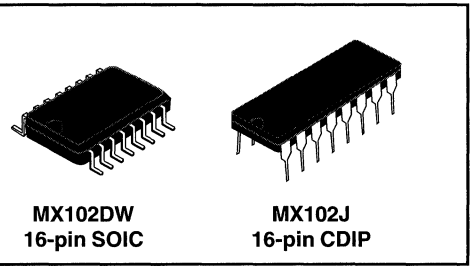
- Low Signal Level Input of 20mVrms
- Wide Signal Frequency Range from 2Hz to 12kHz
- On-Chip Gain Amplifier
- On-Chip Xtal Oscillator
- Low Supply Voltage Operation of 2.5 V
- Low Current Drain
- SMT Package

BENEFITS

- Improved Signal Sensitivity
- No Timing Required
- Digital Output Signal
- Serves 2-Cell Applications

APPLICATIONS

- Medical Instruments
- Sonar Detection
- Remote Signaling
- Pagers
- Mobile Radio



MX102DW
16-pin SOIC

MX102J
16-pin CDIP

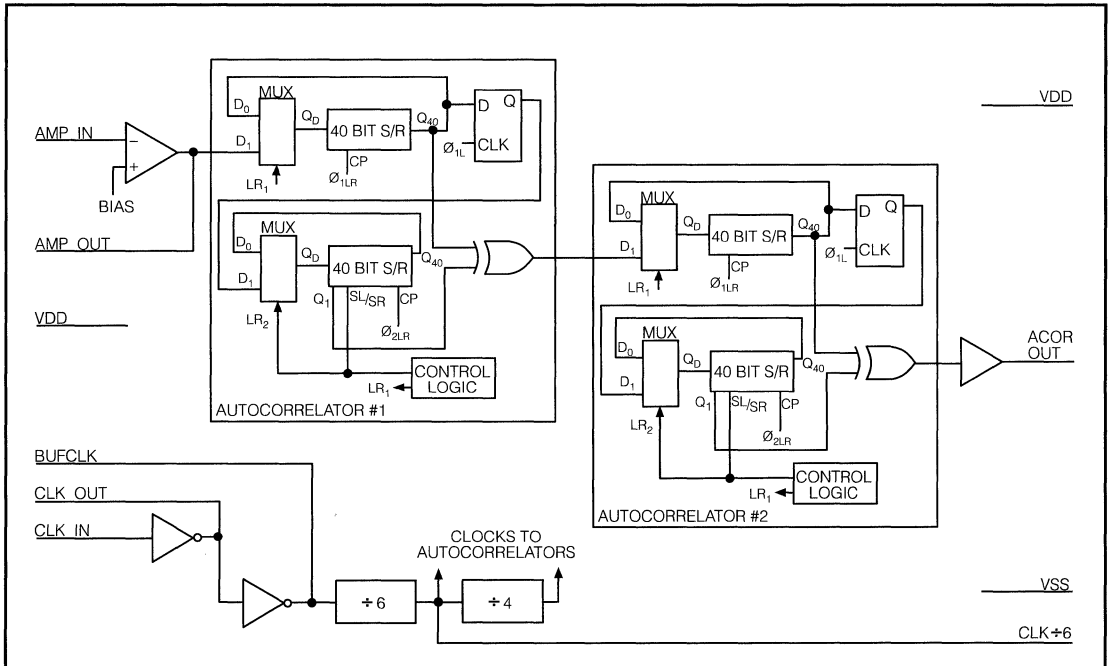


Figure 1 - Block Diagram

Description

The MX102 low power CMOS Autocorrelator extracts periodic signals from random noise environments. The amplitude of non-periodic components is substantially reduced. Its patented autocorrelator compares the incoming signal to itself. The more elements of the waveform that are seen as periodic, the higher the energy at the output at 4 times the input frequency.

The MX102 cascades two autocorrelators, each one improving the signal to noise ratio. The signal between these two autocorrelators is centered at twice the incoming frequency, and the output signal is centered at four times the incoming signal, as shown in Figure 2. With random noise applied the output will swing rail-to-rail at random (peak-limited). The output signal delay is fixed by the chip clock frequency and the length of the internal register.

The MX102 contains an input operational amplifier. The frequency response is shown in Figure 6. The low end 3dB frequency response can be adjusted to 2.0 Hz using an 0.68 µF input capacitor.

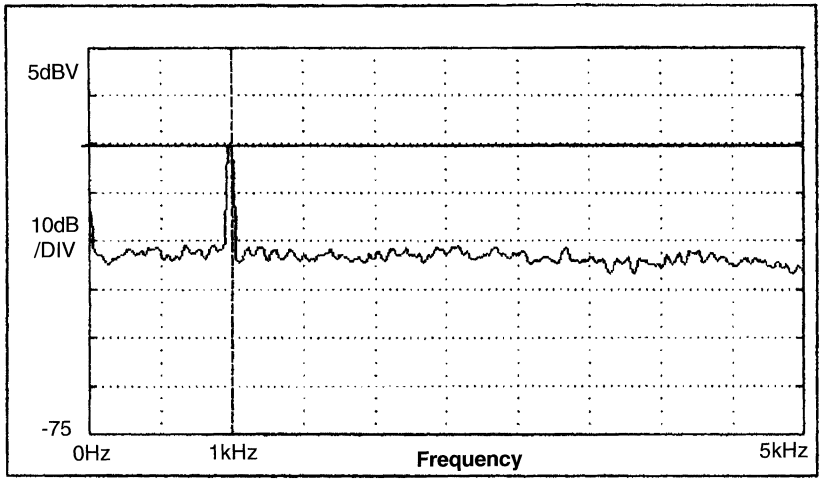


Figure 2a - Input Signal-to-Noise = dB

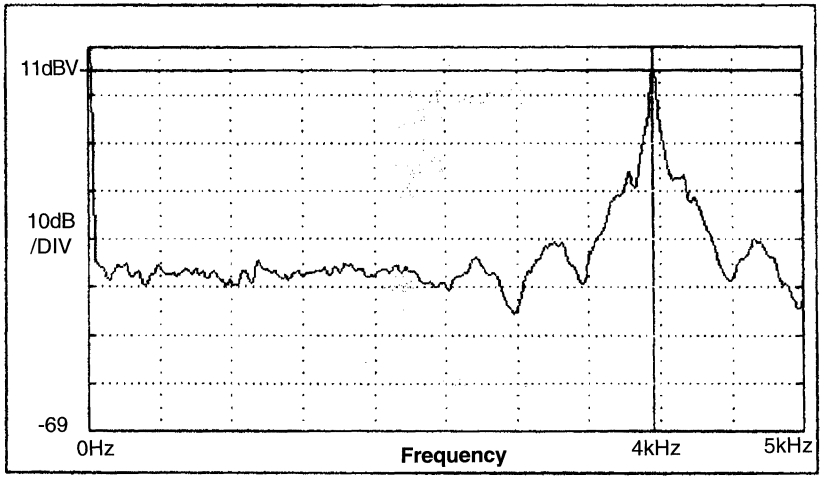


Figure 2b - Output Signal

Note: All measurements made with 47.7 kHz bandwidth.

Input Frequency Range

The MX102 has a wide input frequency range, but care must be taken to choose the xtal frequency appropriate for your application. The input frequency range is from 1/1200 to 1/190 of the xtal frequency. This results in the following design equation:

$$f_{in}\ max \times 190 \leq f_{xtal} \leq f_{in}\ min \times 1200$$

Once your xtal frequency is chosen, it can be compared against Figure 3 to find the valid range of supply voltages. The constraint on supply voltage is only important at the extremes of the frequency input range.

For example, if your maximum input frequency is 12kHz,

$f_{xtal} \geq 2.28MHz$

and $V_{DD} \geq 4\ @\ f_{xtal} = 2.28MHz$

If your minimum input frequency is 2Hz,

$f_{xtal} \leq 2400Hz$

and $V_{DD} \leq 4.5\ @\ f_{xtal} = 2400Hz$

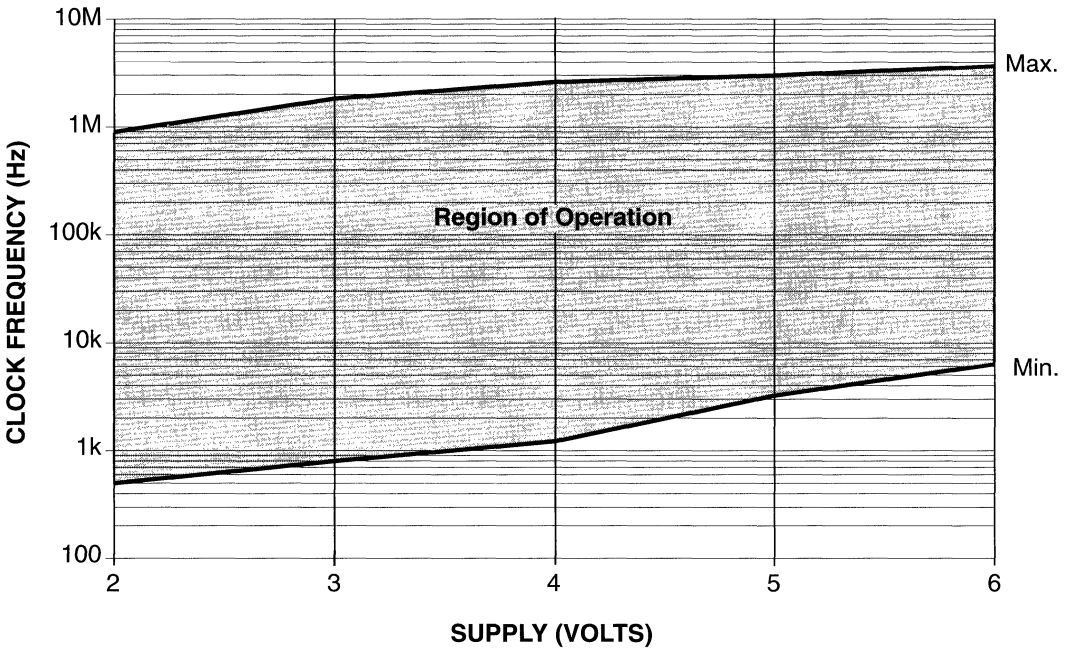


Figure 3 - Clock Frequency vs Supply Voltage

Note: this graph is intended as a guideline; the limits are not production-tested.

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PIN FUNCTIONS

Pin	Function
1	**AMP IN**: Inverting input to analog amplifier/comparitor. This pin is normally 'AC' coupled to the incoming signal with a feedback resistor to its output.
3	**AMP OUT**: Output of analog amplifier/comparitor. This pin does not have the drive capacity for any off chip signaling. Feedback resistance should be greater than 200 kΩ.
4	**V_{DD}**: Positive Supply
5	**BUFCLK**: Buffered inverter oscillator digital output. May be used as test point to align clock frequency or to drive other circuitry.
6	**CLK OUT**: Output of oscillator inverter.
8	**CLK IN**: Input to oscillator inverter.
9	**V_{SS}**: Negative Supply
11	**CLK ÷ 6**: A digital output signal derived by dividing the clock input frequency by 6.
13	**ACOR**: Autocorrelator digital output signal. Frequency is at four times the input frequency.
16	**V_{DD}**: Positive Supply

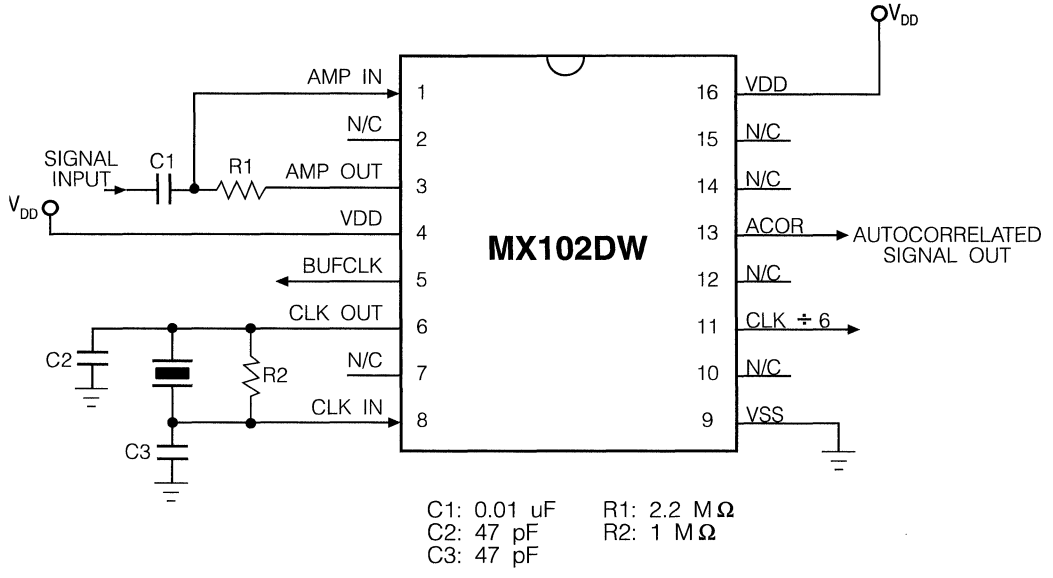


Figure 4 - External Components

TIMING

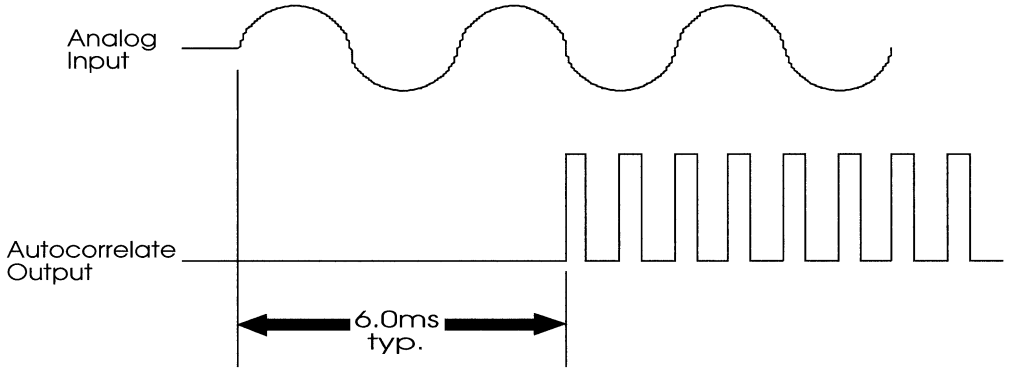


Figure 5 - Timing Diagram

AMPLIFIER FREQUENCY RESPONSE

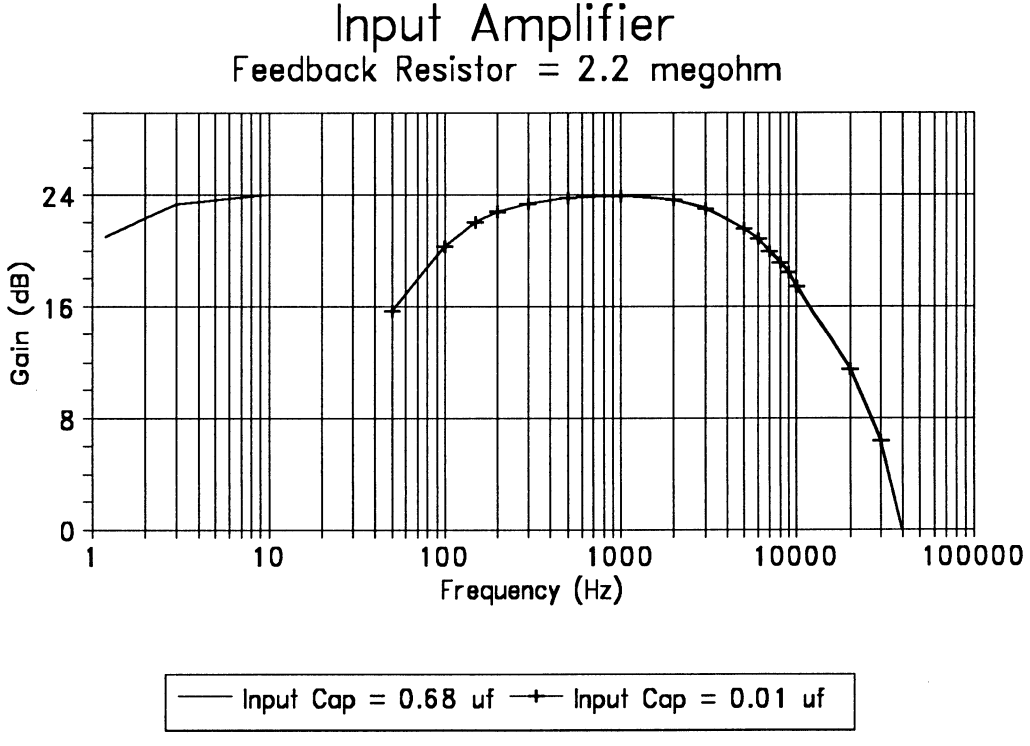


Figure 6 - Input Amplifier Frequency Response

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 volts
Input Voltage at any pin	-0.3 to (Vdd+0.3 volts)
Sink/Source Current (Total)	20 mA
Maximum Device Dissipation	100 milliwatts
Operating Temperature	-30°C to +85°C
Storage Temperature	-40°C to +125°C

OPERATING LIMITS

All devices are measured under the following conditions unless otherwise noted.

V_{DD}	5.0 volts
T_{AMB}	25°C
Xtal/Clock	560 kHz
Input Test Signal	1 kHz at 200 mV rms
External Connections	see Figure 1

Characteristics	See Note	Min	Typ	Max	Unit
Supply Voltage	1	2.5	5.0	5.5	V
Supply Current		-	1.0	2.0	mA
	2	-	4.0	-	mA
Logic '1' Level		4.0	-	-	V
Logic '0' Level		-	-	1.0	V
Digital Output Impedance		-	4.0	-	kΩ
Analog Amplifier DC voltage gain		-	50	-	dB
Dynamic Values					
Signal Input	3	20	100	1000	mVrms
Analog Amplifier Gain	4	20	-	-	dB
	5	9.0	-	-	dB
	6	10.0	-	-	dB
Minimum Input Waveform Duty Cycle		-	35	-	%
Freq Out/Frequency In Ratio		4	-	4	
Maximum Clock Frequency		2.5	-	-	MHz
Frequency Input Range	7	500	-	3000	Hz
Input to Output Delay	8	-	-	5.9	ms
	9	-	1.4	-	ms
Capture Range	10	-	-	3	dB

NOTES

1. Maximum Clock frequency varies with supply voltage.
2. Operating current at 2.24 MHz clock.
3. Signal input required to provide constant autocorrelated output.
4. Measured at 6000 kHz.
5. Measured at 2.5 vdc input.
6. Measured with 12 kHz input signal.
7. The frequency input range is 1/190 to 1/1200 of the xtal clock frequency (see "Frequency Input Range" section).
8. Time from pulsed input signal to correlation output.
9. Time from pulsed input signal to correlation output with 2.24 MHz clock.
10. Two tone input, level difference

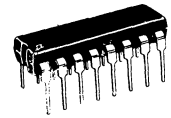
MX·COM, INC.

MX105

TONE DETECTOR

FEATURES:

- **Operates in High Noise Conditions**
- **≥40dB Signal Input Range**
- **Simultaneous Tone Detection**
- **Adjustable Bandwidth**
- **Hermetically Sealed Ceramic Package**
- **Wide Frequency Range**



MX105J (CDIP)
MX105P (PDIP)
16 pins

APPLICATIONS:

- **Tone Decoding in Single and Multitone Signaling Systems**
- **Decoding of Sequential or Simultaneous Tone Signaling Systems**

DESCRIPTION

The MX105 is a monolithic PMOS tone operated switch, designed for tone decoding in single and multitone signaling systems.

The device employs decoding techniques which allow tones to be recognized in the presence of high noise levels or strong adjacent channel tones.

Tone channel center frequency and channel bandwidth can each be adjusted independently. The circuit has a high noise immunity against harmonic and sub-harmonic responses and is able to maintain a constant bandwidth and high noise immunity over a wide range of input signal levels.

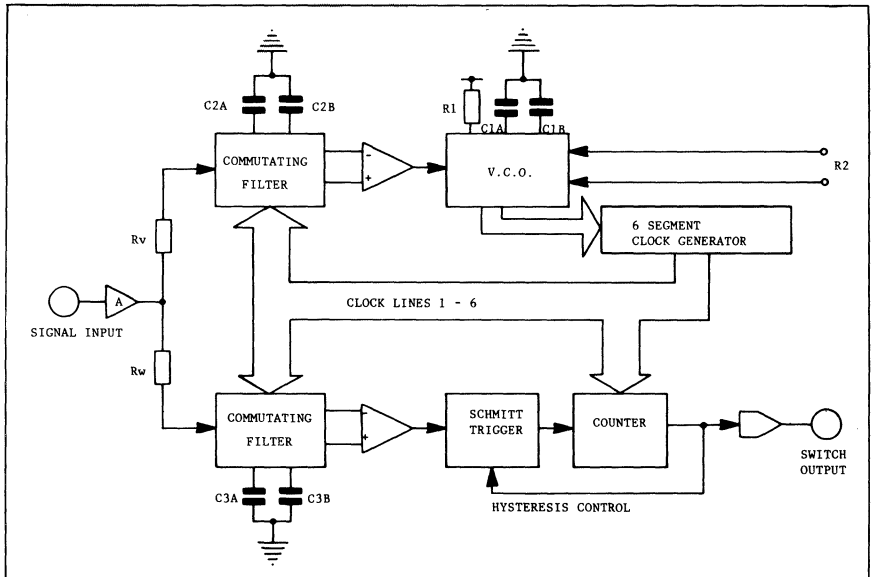


FIG. 1: MX105 INTERNAL BLOCK DIAGRAM

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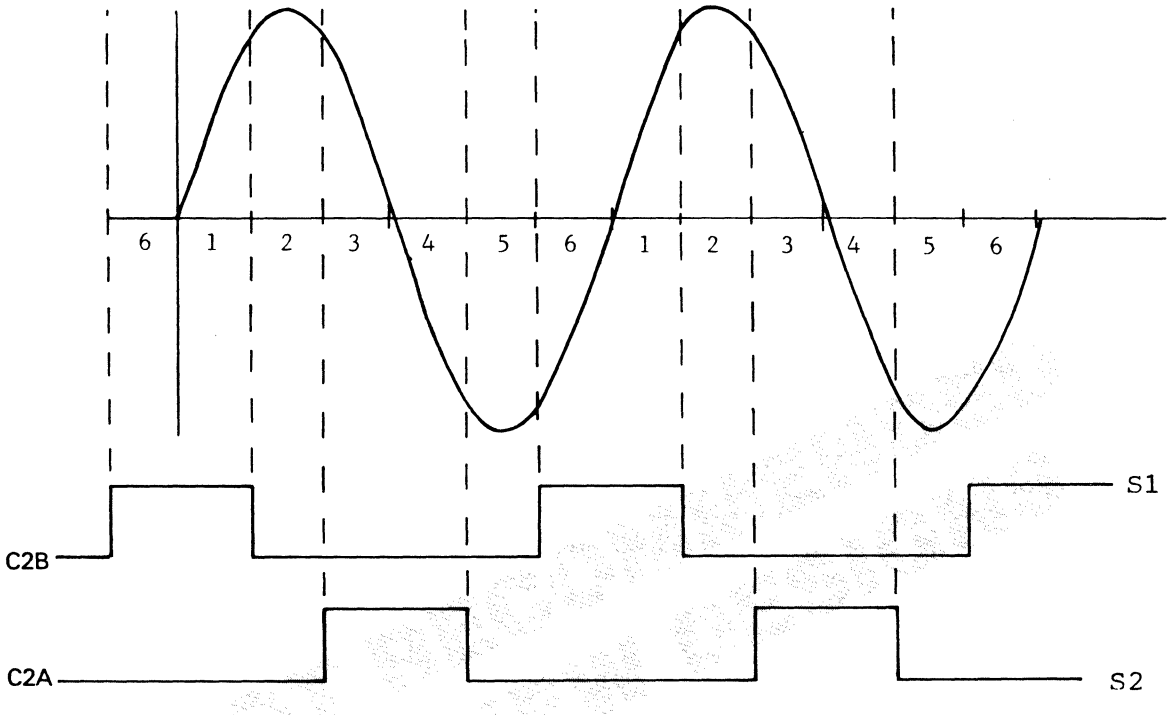
FIG. 2: V.C.O. SAMPLING WAVEFORMS



DEVICE OPERATION

Input signals are A.C. coupled to the buffer input, which is internally biased at 50% of supply voltage. The signal appears at the output of the buffer as an A.C. voltage superimposed on the D.C. bias level. The signal is then coupled via RV and RW to the voltage controlled oscillator and word sampling switches, which sequentially connect C2 and C3 into circuit to form four sample and hold RC integrators.

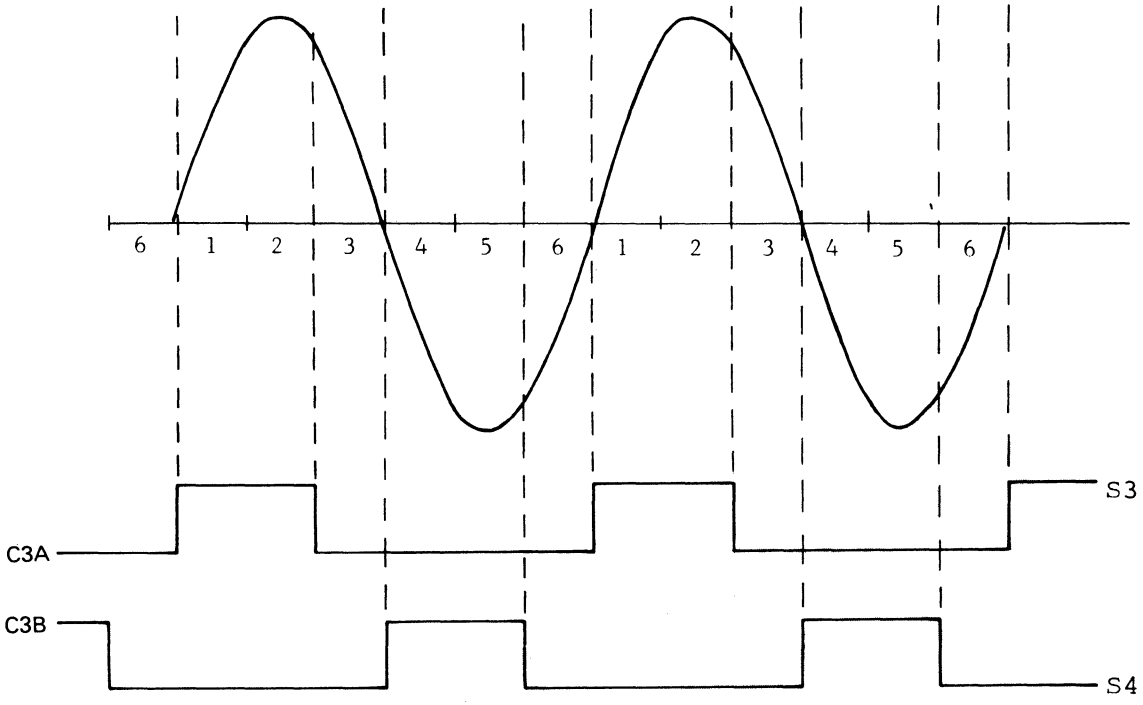
With no input signal, each capacitor charges to the D.C. bias level and differential voltages are zero. When an input signal is applied, each capacitor receives an additional charge. This charge is determined by the integrated average of the signal waveform during the interval the capacitor is switched into circuit.

Figure 2 shows the operating sequence of the V.C.O. sampling switches and their phase relationship to a locked-on inband signal. As can be seen, C2A and C2B should not receive any additional charge, since they always sample the input as it crosses the D.C. bias level. Should the signal not be locked to the V.C.O., then a positive or negative charge voltage will appear on C2A or C2B. This voltage, when differentially amplified, is applied to the V.C.O. as an error correcting signal to enable V.C.O. "lock."

Figure 3 shows the operating sequence of the 'Word' sampling switches and their relationship to a locked-on inband signal. As can be seen, the charge being applied to C3A should always be positive and the charge applied to C3B should always be negative (with respect to the common bias level).

These capacitor potentials are differentially amplified and applied to a D.C. comparator, which switches at a pre-determined threshold voltage. The comparator output is a logic signal used to control a counter. This counter switches the MX105 output ON when the comparator output is maintained in the 'Word Present' state for a minimum number of consecutive signal samples. The activated output switch reduces the comparator threshold by 50%, introducing threshold hysteresis. Output chatter with marginal input signal amplitudes is minimized.

FIG. 3: WORD SAMPLING WAVEFORMS

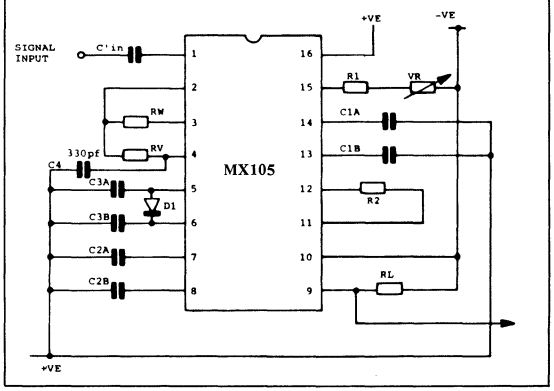


METHOD FOR CALCULATING EXTERNAL COMPONENT VALUES

The external components shown in Figure 4 are used to adjust the various performance parameters of the MX105. The signal to noise performance, turn on delay and signal bandwidth are all interrelated factors which should be optimized to meet the requirements of the application.

By selecting component values in accordance with the following graphs, nominally optimum circuit performance is obtained for any given application.

FIG. 4: EXTERNAL COMPONENT CONNECTIONS



The user should first define the following application parameters:

A. The center frequency to be detected (f'o).
B. The MX105 Minimum Usable Bandwidth (MUBW). This is obtained by taking into account the worst case tolerances on the input tone frequency and variations in the MX105 f'o due to supply voltage (0.07%/%) and ambient temperature (0.02%/°C) changes.
C. The maximum permissible MX105 response time.
D. The minimum input signal amplitude.

Using this information, the appropriate component values can be calculated, and the signal to noise performance can be read from a chart.

Using graphs 1-10, the following example is used to demonstrate the calculation of component values for any given application.

A. MX105 centre band frequency (f'o) = 2800Hz.
B. MX105 bandwidth = 6%.
C. MX105 maximum response time = 50ms.
D. Minimum input signal amplitude = 200mVrms.

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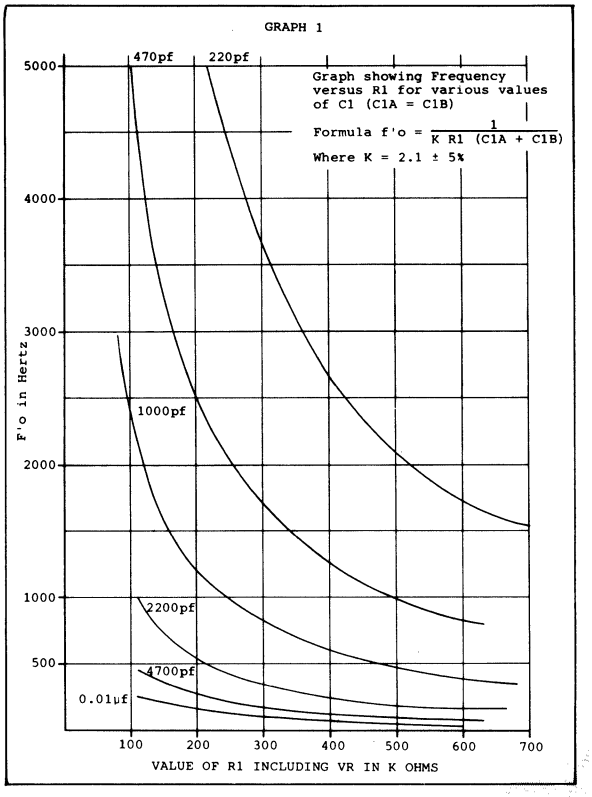


R1 C1A C1B

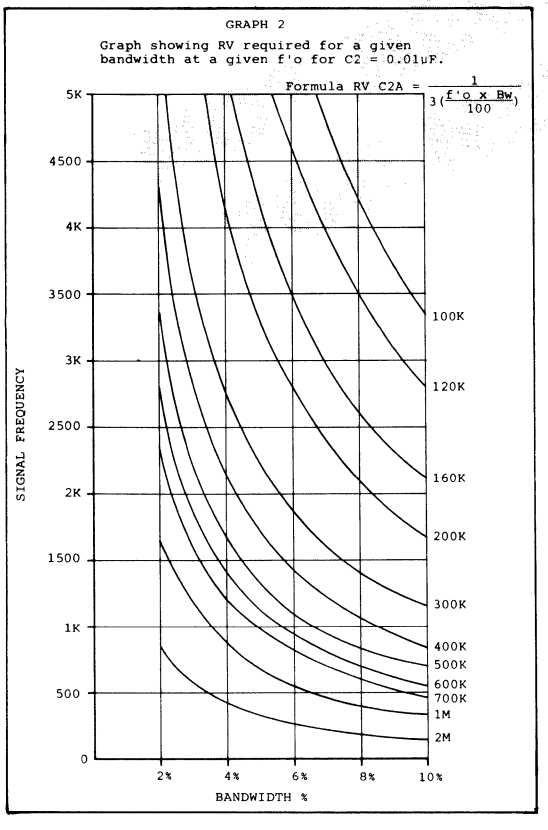
These components set the free running frequency of the V.C.O. and thereby the center band frequency of the MX105.

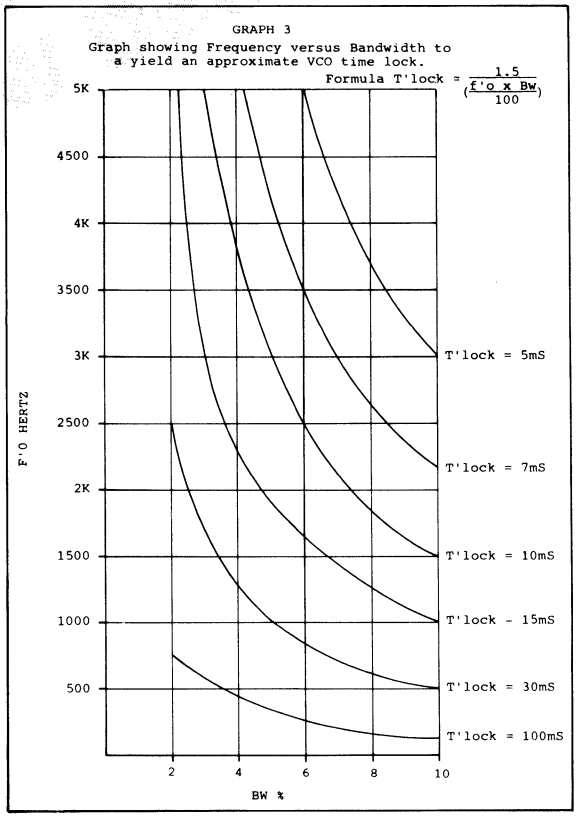
By using graph number 1, the frequency 2800Hz can be seen to correspond to a capacitor value of 220 picofarads and a resistor value of 385k ohms. This resistance can be achieved with a 300k ohm fixed resistor for R1 and a 100k ohm potentiometer.

Graph number 2 shows that for a frequency of 2800Hz and a bandwidth of 6%, a resistor RV of 200k ohms and a capacitance for C2A and C2B of 0.01 microfarads will be required.

The response time of the MX105 is the sum of the V.C.O. 'Lock' time (T'lock) and the 'Word' integration time (T'word).

Graph number 3 shows that for a frequency of 2800Hz and a bandwidth of 6% the approximate 'Lock' time will be 9 milliseconds. Since the maximum response time is 50 milliseconds, a 'Word' time of 41 milliseconds is allowed.





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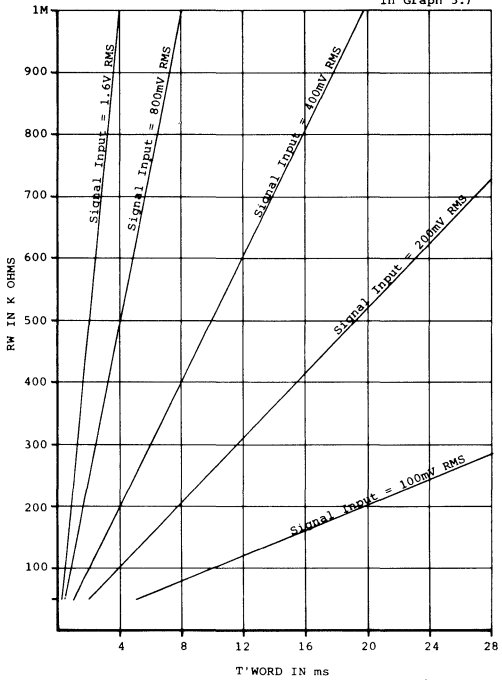
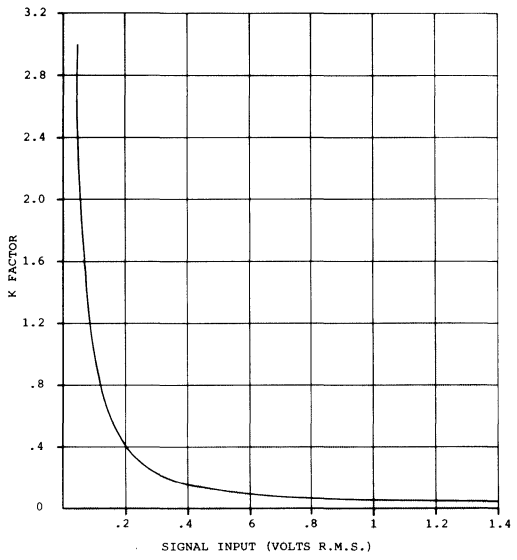
GRAPH 4

Graph showing RW required for T'word for a given signal input assuming C3A = C3B = 0.1µF. Formulae T'word = RwC3A x K(given in Graph 5.)



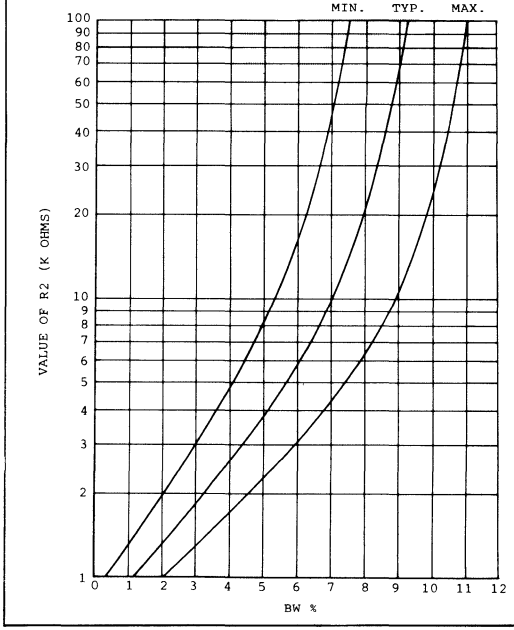
GRAPH 5

GRAPH SHOWING K FACTOR VS SIGNAL INPUT AMPLITUDE.



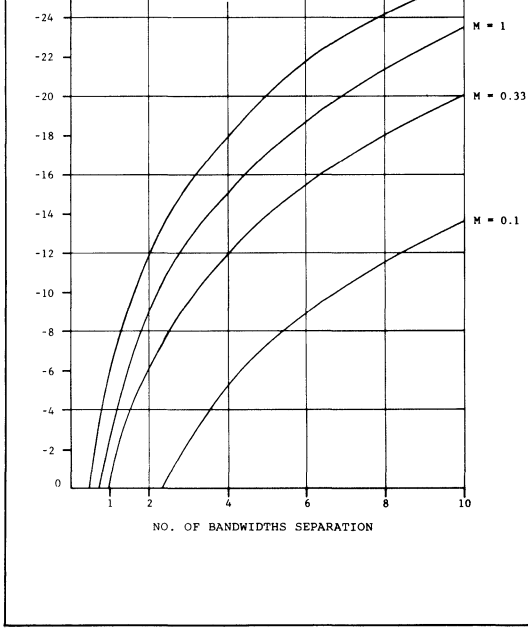
GRAPH 6

GRAPH SHOWING VALUE OF R2(KΩ) TO YIELD SELECTED BANDWIDTH(%)



GRAPH 7

$\frac{S}{N}$ dB GRAPH SHOWING SIGNAL TO NOISE RATIO (dB) VS DISTANCE FROM f'o (MEASURED UNITS OF Bw)



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Graph number 4 shows that for a signal amplitude of 200mVolts, a resistor value RW of 510k ohms with a 0.1 microfarad capacitor for C3A and C3B will yield a 'Word' time of 20ms. This in turn yields a response time of 9ms + 20ms = 29ms.

Graph 6 shows the range of values for R2 to yield a given bandwidth. The exact bandwidth given by any value of R2 will vary with differing production batches. Therefore, in applications where an exact bandwidth is required, R2 should be a variable resistor which is adjusted on test.

- Worst-case signal to noise calculations depend on calculation of an "M" value using the following formula:

$$M = \frac{f'o \times Bw}{100} \times (Rw \cdot C3A)$$

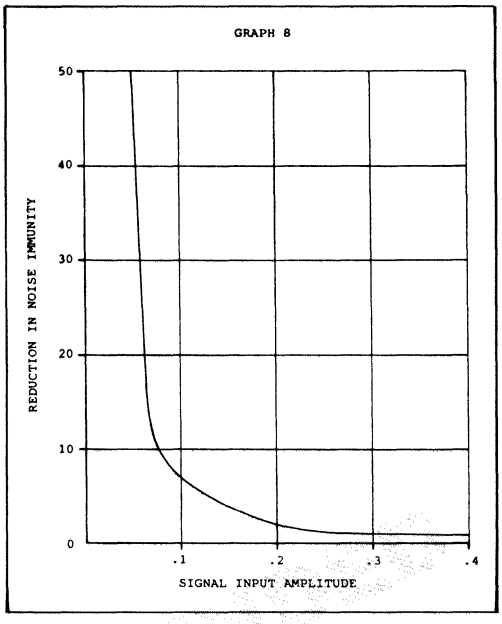
- substituting our example values:

$$\therefore M = \frac{2800 \times 6}{100} \times (0.51m\Omega \times 0.1\mu F)$$

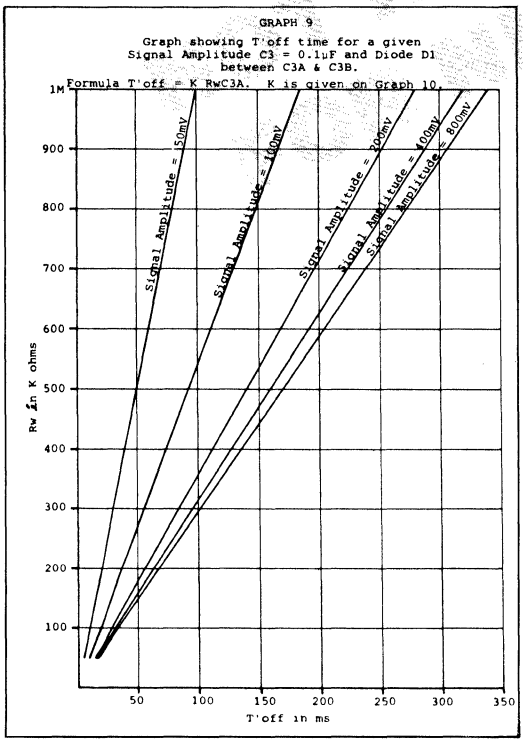
$$\therefore M = 168 \times 0.051$$

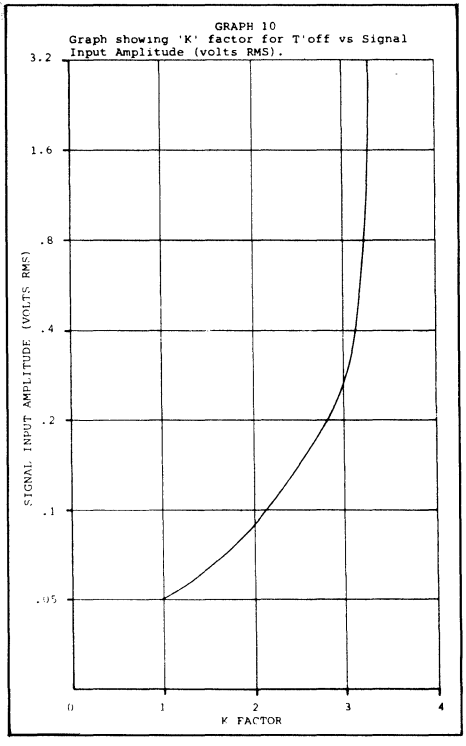
$$\therefore M \simeq 8.57$$

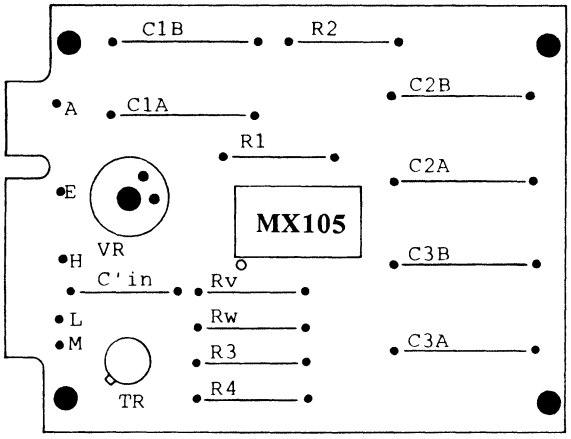
By substituting the value for M of 8.57 in graph number 7, the signal to noise ratio of an adjacent tone can be found. This then has to be decreased depending upon the tone amplitude. The figure to decrease SNR by is calculated from graph 8.



Graphs 9 and 10 show the approximate time the MX105 will take to turn off after an inband signal has been removed. The turn-off time is calculated with a diode (1N914 or similar) between pins 5 and 6, as shown in Figure 4. The effect of this diode is to greatly reduce the turn-off time with signal input amplitudes greater than 300mV R.M.S.





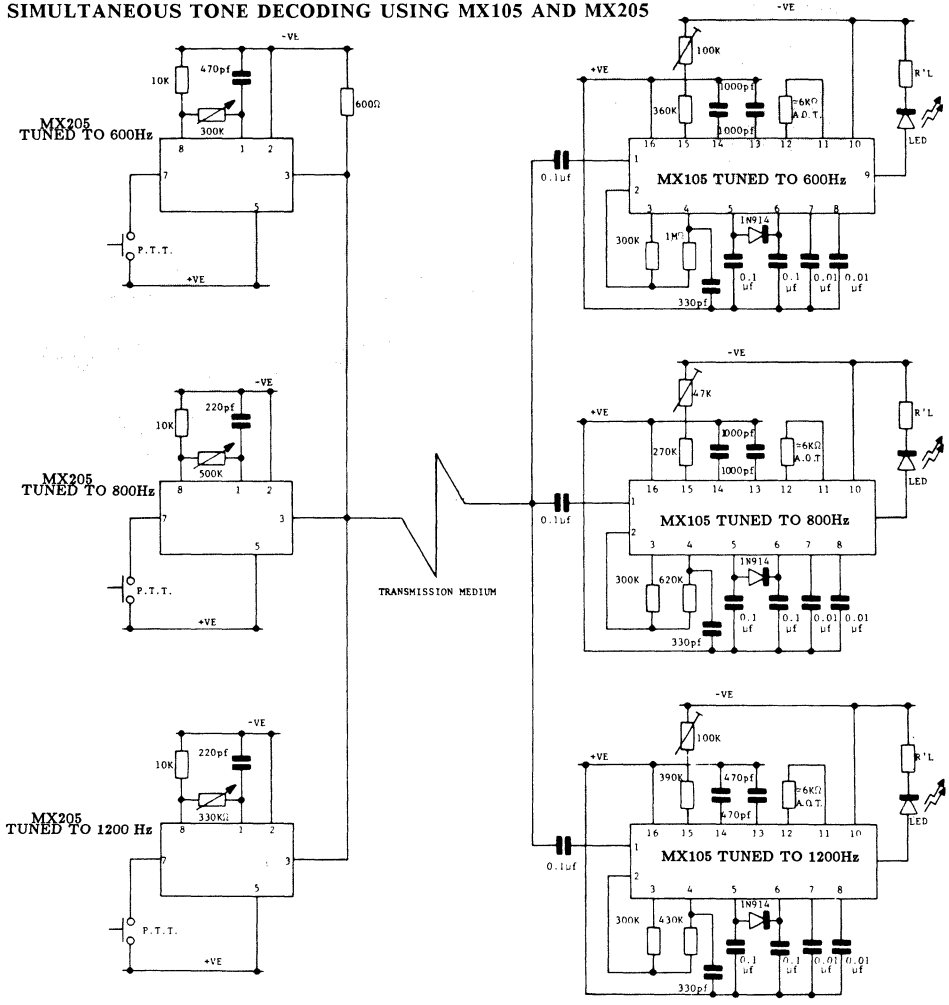


EDGE CONNECTIONS.
A = +ve
E = -ve
H = Signal Input
L = Switch Output
M = Buffer Output

To assist engineers in designing systems utilizing the MX105, MX-COM has produced a printed circuit board with the necessary external component outlines (see Fig. 5), that demonstrates a full working system. Please note there is no provision on the P.C.B. for capacitor C4 or diode D1 and it is recommended that these components are added for improved system operation.

Due to the MX105's ability to decode tones in the presence of adjacent channel tones or noise, the device is ideally suited to applications where a number of tones are sequentially or simultaneously transmitted over a common link. In the example shown in Figure 6, a number of single tone transmitters (MX205) are transmitting over a common link such as cable, radio, optical, etc., to a number of receivers (MX105). The transmitters may transmit either individually or simultaneously to the MX105s without the possibility of missing a call or receiving a false call.

FIG. 6: SIMULTANEOUS TONE DECODING USING MX105 AND MX205



MX105 ELECTRICAL SPECIFICATION

MAX. RATINGS Failure to observe may result in device damage.

MAX. VOLTAGE BETWEEN ANY PIN AND +VE SUPPLY (pin 16) ..... −20V and +0.3V
OPERATING TEMPERATURE RANGE ..... −30°C to +85°C
STORAGE TEMPERATURE RANGE ..... −55°C to +125°C
DEVICE DISSIPATION (at 20°C ambient temperature) 400mW
MAX. OUTPUT SWITCH LOAD CURRENT 10mA

CHARACTERISTICS

Note: Due to A.C. signal coupling either supply polarity may be 'ground.'

SYMBOL	PARAMETER	NOTES	MIN.	TYP.	MAX.	UNITS
V_s	Supply voltage	Operating range	10	12	15	Volts
I_s	Supply current	Total, excluding loads		5		mA
	Signal input	Signal + noise range	0.055		5[1]	Volts R.M.S.
F'o	Channel Frequency		0.04		5	kHz
Bw	Bandwidth		2%		10%	
	O/P switch load current				10	mA
Z_{in}	Input impedance			200		k ohm
	Frequency Stability	vs T'AMB		0.02%/°C		
	Frequency Stability	Per 1% change in supply volts		0.07%		

NOTE
1. For input voltages greater than VDD × 0.143, pins 1 and 2 should be open circuit and the signal applied via C'in to the junction of RV and RW.

9

Section 10: Appendix

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NOTE: Application Notes are available for DCS, LTR, CTCSS and N-Tone Signaling applications using our DBS800 IC set. Call us at 1-800-638-5577 for more information.

Appendix

STANDARDS & REFERENCES

Related Mobile Communications Industry Standards

CDPD (Cellular Digital Packet Data) Specification:

CDPD Industry Input Coordinator
650 Town Center Dr., Suite 820, Costa Mesa, CA 92626
Phone : 714-545-9400, ext. 235 Fax: 714-545-8600

MOBITEX protocol:

RAM Mobile Data
10 Woodbridge Center Drive, Woodbridge, NJ 07095
Phone: 908-602-5543 Fax: 908-750-0209

RCR STD-17, -18, -21, -29 & -30:

Research and Development Center for Radio Systems (RCR)
5-16 Toranomon 1, Minato-Ku, Tokyo 105, Japan
Phone: 813-3592-1101 Fax: 813-3592-1103

RD-LAP protocol:

ARDIS
300 Knightsbridge Parkway, Lincolnshire, IL 60069
Phone: (708) 913-1215

Mobile Communications Industry Standards Organizations

MX•COM is an early implementor of standards-based technology. As active participants in today's standards committees, we will continue to give you early access to standard-based ICs.

The Telecommunications Industry Association (TIA) publishes bulletins, recommendations and standards applicable to telecommunications equipment. The following subcommittees address mobile communications equipment:

1. TR-8 Land Mobile Services

Land Mobile radio products and systems including voice and data applications. TR-8 is responsible for all technical matters of industry concern and the promulgation of standards including definition of terms, methods of measurement and equipment specifications.

2. TR-32 Personal Communications Equipment

Standards for wireless consumer communications devices such as cordless telephones, citizen band radio, and the like.

3. TR-45 Cellular and Common Carrier Mobile Radio System Standards

Performance, compatibility, inter-operability, and service standards for all cellular and common carrier systems. These standards apply to service definition, wireless telephone equipment, wireless base station equipment, wireless telephone switching office equipment, ancillary apparatus, inter-system operation and interfaces. The TR-45 Committee shall coordinate, for the purposes of consistency, with other TR committees, and with other national standards bodies and appropriate organizations as their work requires.

Other agencies that publish relevant standards are the European Telecommunications Standards Institute (ETSI), the Consultive Committee of the International Telephone and Telegraph (CCITT), the Electronics Industries Association (EIA), and the Institute of Electrical and Electronics Engineers (IEEE). Addresses of these organizations are provided below.

TIA **Telecommunications Industry Association**
2001 Pennsylvania Avenue, NW
Suite 800
Washington, DC 2006-1813
USA
Phone: (202) 457-5430
Fax: (202) 457-4939

ETSI **European Telecommunications Standards Institute**
06921 Sophia Antipolis Cedex
FRANCE
Phone: 33 92 94 42 00
Fax: 33 93 65 47 16

ITU-T **(Formerly CCITT and CCIR)**
International Telecommunications Union
Place Des Nations
CH-1211 Geneva
Switzerland
Phone: (011) 4122 730 5851

EIA **Electronic Industries Association**
1722 Eye Street, NW
Suite 440
Washington, DC 20006
USA
Phone (Headquarters): (202) 457-4936
Phone (Standards): (202) 457-4966

IEEE **Institute of Electrical and Electronics Engineers**
Headquarters:
345 East 47th Street
New York, NY 10017
USA
Phone: (212) 705-7900

Standards Office:
IEEE Service Center
PO Box 1331
Piscataway, NJ 00855
USA
Phone: (201) 981-0060

PRODUCT LISTING REFERENCES

MX•COM product information is available from a variety of sources, including electronic listing services. Some of the sources for information are listed below:

CAPS (Computer Aided Product Selection) -- CD-ROM

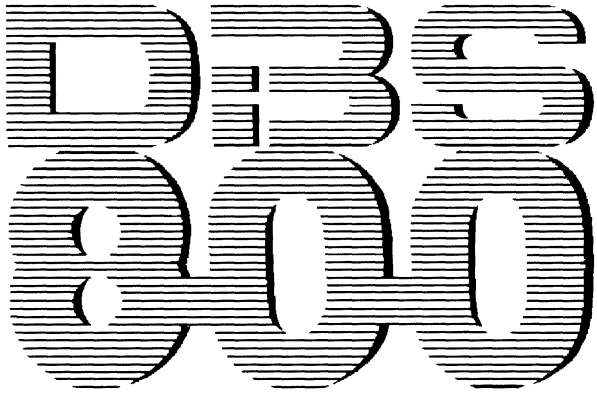
Cahners Technical Information Service
275 Washington St.
Newton, MA 02158-1630
USA
Phone: 617-558-4960
Fax: 617-630-2168
CAPS Support Hotline: 408-257-0552

IC MASTER

Hearst Business Publishing, UTP Division
645 Stewart Ave.
Garden City, NY 11530
Phone: 516-227-1300
Fax: 516-227-1901

INFORMATION HANDLING SERVICES -- CD-ROM

Technical Information Data Service
15 Inverness Way East
PO Box 1154
Englewood, CO 80150
USA
Phone: 800-525-7052 or 303-790-0600



Digitally-integrated Baseband Subsystem

System Overview Including C-BUS Applications and DBS 800 Development Kit

This application note contains an introduction to the DBS800 devices and their potential applications in Mobile Radio equipment, a description of MX-COM's 'C-BUS,' and information about design & development support. Data bulletins on individual devices can be found in the Technical Specifications section of this catalog.

C-BUS COMPATIBLE

Digitally-integrated Baseband Sub-system (DBS800) System Overview

MX802 • MX803A • MX805A • MX806A • MX809

This family of audio processing and signaling devices is designed for use in two-way mobile or trunked radio. While supporting all internationally mandated or system-specific requirements for processing and signaling, DBS 800 also includes many high-level functions which offer a flexible, low-cost route to the "Added Value" opportunities in the LMR market.

DBS 800 was created with the mobile radio hardware and software development engineer in mind. All IC's were designed as peripherals to the radio's host microprocessor. They require a minimum amount of control software. A single address and data hardware bus (C-BUS) is used on all IC's for easy connections to the host microprocessor and minimum track layout.

To support the product's functions there is a development kit including all DBS 800 integrated circuits, a support microprocessor and software. It allows evaluation, demonstration and software development to be completed in a fraction of the time normally required (see pages 532-533).

Features

Complete audio processing (CEPT, EIA, etc.)

Universal Signaling:
- *SelCall (CCIR, ZVEI I, II, III, EEA, etc.)*
- *CTCSS (EIA, EEA)*
- *DPL™, Digital Coded Squelch (DCS)*
- *Digital Selcall, 1200 Baud MSK (MPT 1317/1327)*
- *DTMF encode*
- *LTR™, NRZ Data*
- *2-Tone, Special Tones*

Data Communications with data storage and buffering

Voice/Data Scrambling

Voice Management
- *Voice storage, Mailbox, delay, busy buffer, alarms and status -- Reduced airtime usage -- Increased spectrum efficiency -- VOX/Handsfree operation*

System Management
- *Over-air programming/re-configuration and cloning -- Call billing/monitoring/blocking -- TX time-out/ selective lockout -- Repeater access/control -- Direct control of all system radio units*

ANI (Automatic Number Identification)

Half-duplex repeater

Common Control and Data Bus ("C-BUS")

Hardware Development Kit

Software Support:
- *Evaluation - Demonstration - Development*

Electronic digital trimming and volume control

Adaptive compensation for non-linear and temperature effects

Two-Point Modulation for trunked/scanning schemes

Fully automated test/alignment/servicing

Self-test mode

Single hardware design approach
- *Software reconfigurable*

Full integration reduces PCB area

Greatly reduced development time

Multi-level powerdown modes

Benefits

- DBS 800 is compatible with most Selcall schemes such as DTMF, 5/6-Tone, 2-Tone and MSK. It is also compatible with Sub-Audio CTCSS, DCS and LTR™.
- Allows advanced signaling: Digital Selcall, ANI, overair re-configuration, cloning, channel dependent signaling.
- A single design concept can be used for all models of mobile radio with different features or market destinations. Software is reconfigurable.
- One microprocessor is required to control all radio functions. DBS 800 devices contain additional hardware to minimize software overhead.
- Digitally controlled trimmers allow for "adaptive adjustment" of non-linear VCO conversion gain and temperature effects. This allows use of cheaper, lower-tolerance components.
- Non-predictive decoding of signaling devices gives total design flexibility.
- Smaller, lighter equipment design possible, e.g. handhelds.
- Non-predictive decoding offers features such as recognition and identification of own repeater CTCSS tone, multiple group call, etc.
- Voice management features voice security, voice mailbox, voice status, voice alarm, and voice buffering when a channel busy condition exists.
- For data communications, there is the ability to connect directly to mobile radio with no external interface, laptop PC's, printers, etc. RS232 interface or others are possible. Data storage and security are software dependent.
- Inventory is simplified by using the standard DBS 800 chip set.
- Radios can be calibrated and tested when completely assembled by using a single external audio/data/RF connection.
- Self test modes with audible/visual alert outputs.
- Simple field test unit can be used to test or reconfigure radios incorporating DBS 800.

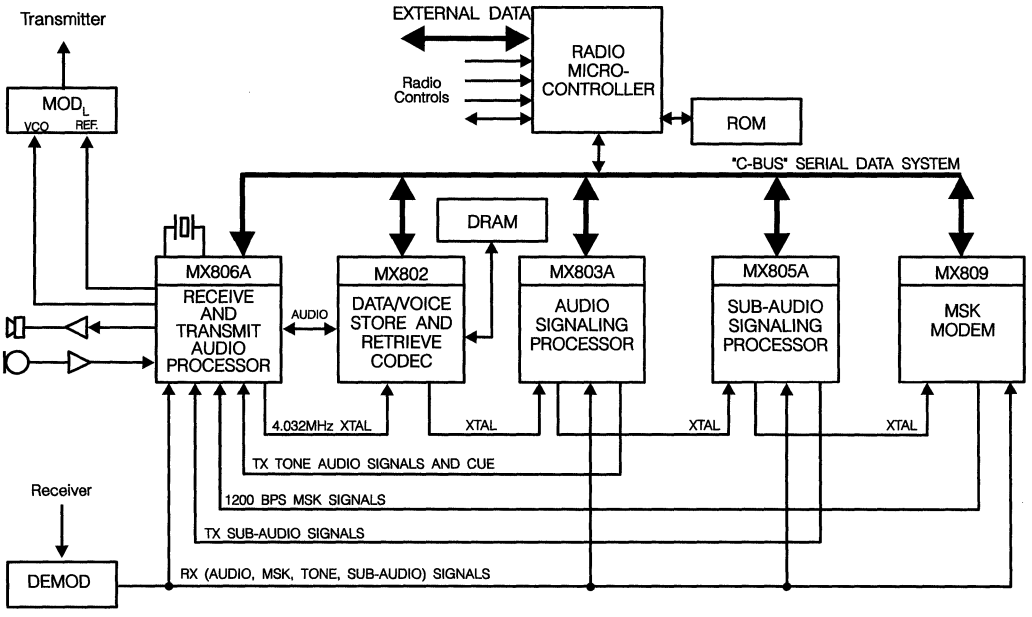


Figure 1 - DBS 800 Audio System

DBS800

The Digitally-Integrated Baseband Sub-system (DBS 800) is a family of low-power CMOS integrated circuits which provide a comprehensive range of audio processing and signaling functions for use within two-way radio systems.

Each IC can be used as part of the complete DBS 800 audio system, or as a "stand alone." The system and ICs are partitioned in such a way that radio designers can easily select the device(s) appropriate to their needs.

DBS800 ICs currently available are:

- **MX802 DVSR Codec**
  This is a Continuously Variable Slope Delta Modulation (CVSD) speech encoder and decoder with the ability to store and retrieve voice and data within attached external Dynamic Random Access Memory (DRAM) using an on-chip DRAM controller.

- **MX803A Audio Signaling Processor**
  This provides an inband tone signaling ability to LMR Systems.

- **MX805A Sub-Audio Signaling Processor**
  This provides a sub-audio and digital signaling (NRZ) ability to LMR Systems.

- **MX806A LMR Audio Processor**
  This is a half-duplex audio processor providing all DBS 800 system audio signal conditioning and filtering capabilities for the system transmit and receive paths.

- **MX809 MSK Modem**
  This is an intelligent, half-duplex 1200 baud MSK/FFSK Modem with a software programmable byte-synchronization system and checksum generation and checking.

Control of all DBS 800 ICs is by "C-BUS," a simple hardware and software system for the two-way transmission of commands and data between a microcontroller and the ICs.

C-BUS may be used with any microcontroller and allows the BUS data rate to be determined solely by the microcontroller. Control may be achieved by either the radio's microcontroller or a separate microcontroller dedicated to the purpose.

This section provides information on DBS 800 IC analog interconnections, including recommendations on application-specific gain and mixing components. It also provides C-BUS hardware and software information, including a complete list of address allocations and software commands.

System Audio Interconnections

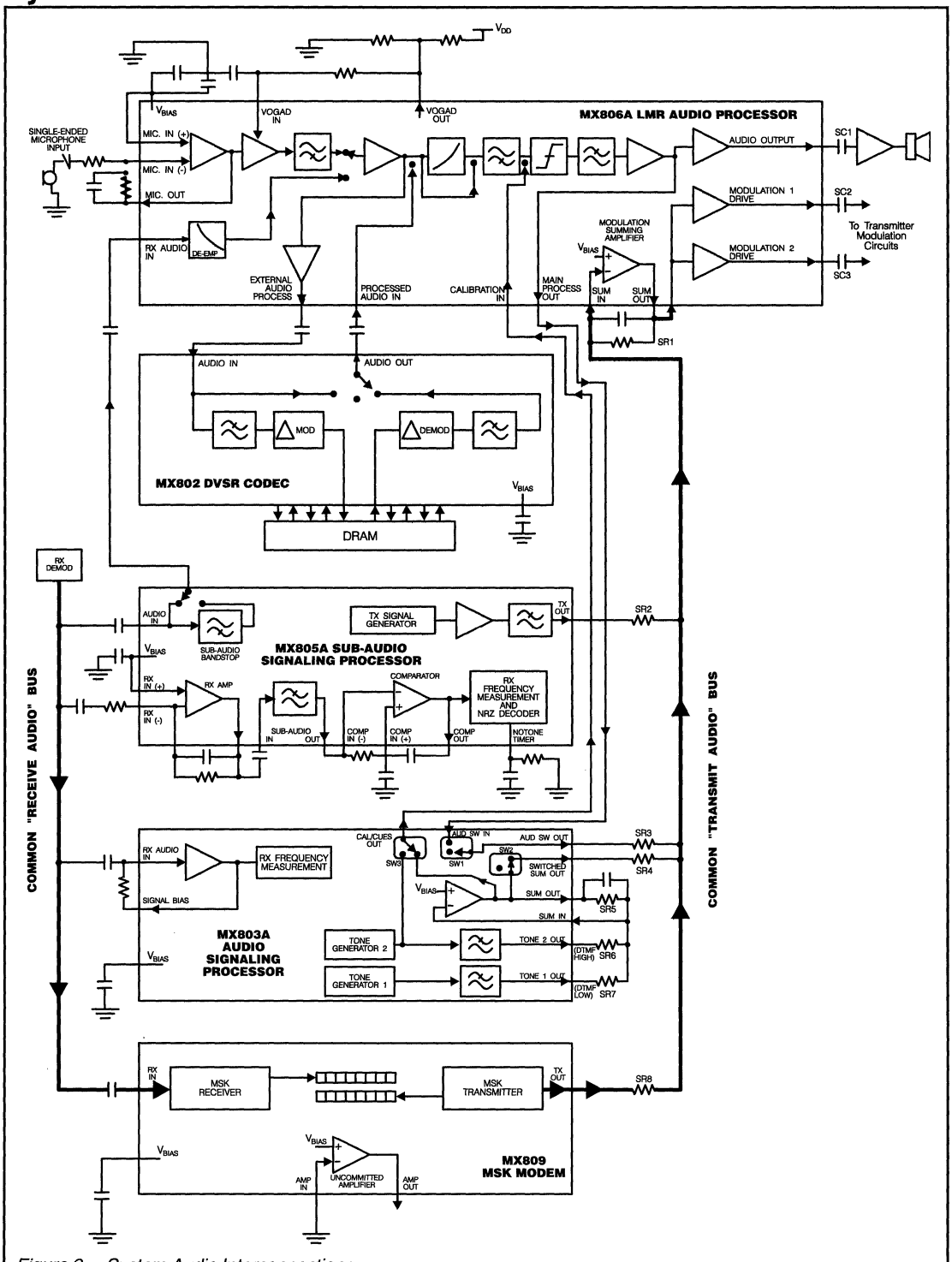


Figure 2 - System Audio Interconnections

System Audio Interconnections

Figure 2 is an example of DBS 800 IC transmit and receive audio paths and interconnections. External components shown are those recommended in the individual Data Bulletins. Components identified by an "S" are illustrated as system components, which means that they are calculated to perform a specific function within the system. Table 1 shows recommended system component values and notes on their calculation.

System Component	Recommended Value	Notes - *(refer to Figure 2)*
SC_1 SC_2 SC_3	See Notes	These modulation drive coupling component values should be chosen with respect to the operational audio requirements and the radio's input specifications.
SR_1	100kΩ	The feedback resistor of the MX806A modulation summing amplifier. This amplifier satisfies the input gain and matching requirements of the remaining DBS 800 devices.
SR_2	1.0MΩ	Configured in conjunction with SR_1 to present a sub-audio signal content of -20.0dB to the modulator.
SR_3 SR_4	100kΩ 100kΩ	Configured in conjunction with SR_1 to present an audio signal level of 0dB to the modulator.
SR_5	100kΩ	The feedback resistor of the MX803A summing amplifier. This amplifier regulates the signal level output of Tone Generators 1 and 2, which in turn are input to the Transmit Audio BUS by switch 2 and SR_4.
SR_6 SR_7	62.0kΩ 122kΩ	Configured in conjunction with SR5 to produce a 3.0dB tone-differential (twist) when the MX803A is used as a DTMF decoder. For selcall applications different output levels may be required, or the signal level from Tone Generator 1 may be attenuated by the MX806A modulator drivers.
SR_8	100kΩ	Configured in conjunction with SR_1 to present an audio signal level of 0dB to the modulator.

Table 1 - Recommended System Component Values

MX803A Sub-Audio Signaling Processor

The audio switch (SW1) is used in this example application to allow interruption of the transmitter modulation path if it is required to provide a Calibration tone from the tone generator to the loudspeaker.

Xtal/Clock Frequencies

All DBS 800 ICs will operate with Xtal/Clock frequencies between 4.00 MHz and 4.10MHz. When considering a common Xtal/Clock frequency for all DBS 800 ICs in a system, it should be noted that:

a) A 4.032 MHz Xtal/Clock input will produce an accurate 1200 bps rate in the MX809 MSK Modem.

b) A 4.096 MHz Xtal/Clock input will generate an accurate 16kbps and 32kbps sampling clock rate in the MX802 DVSR Codec.

c) Driving all DBS 800 IC clock generators from a single Xtal/clock source prevents possible "beat-frequencies" and is therefore preferable.

DBS 800 IC audio frequency responses and internal sampling clock rates vary with respect to Xtal/Clock frequency (see Table 3).

Unused Pins

To improve screening and reduce noise levels around DBS 800 ICs, it is recommended that any unused pins are connected to VSS. This includes inputs to on-chip amplifiers and switches if not used within an application.

MX806A LMR Audio Processor

This is the audio terminal of any DBS 800 "core" audio installation. To demonstrate the versatility of the MX806A microphone input stage, Figure 2 shows the microphone input components in a single-ended configuration, with Figure 2 in the MX806A Data Bulletin showing a differential input configuration. Relevant component values are the same for both applications.

DBS 800 System Audio Level References

Table 2 gives a guide to the relevant signal levels used in the DBS 800 system.

Signal Level (dB)	Amplitude (mVrms)	TX Deviation (%)
-30.0	9.7	
-20.0	30.8	
-15.5	51.3	10
-9.6	102	20
-6.0	154	30
-3.5	205	40
-1.6	256	50
0	308	60
1.3	359	70
2.5	410	80
3.5	462	90
4.4	513	100

Table 2 - Audio Signal Levels

"C-BUS" Controlling System

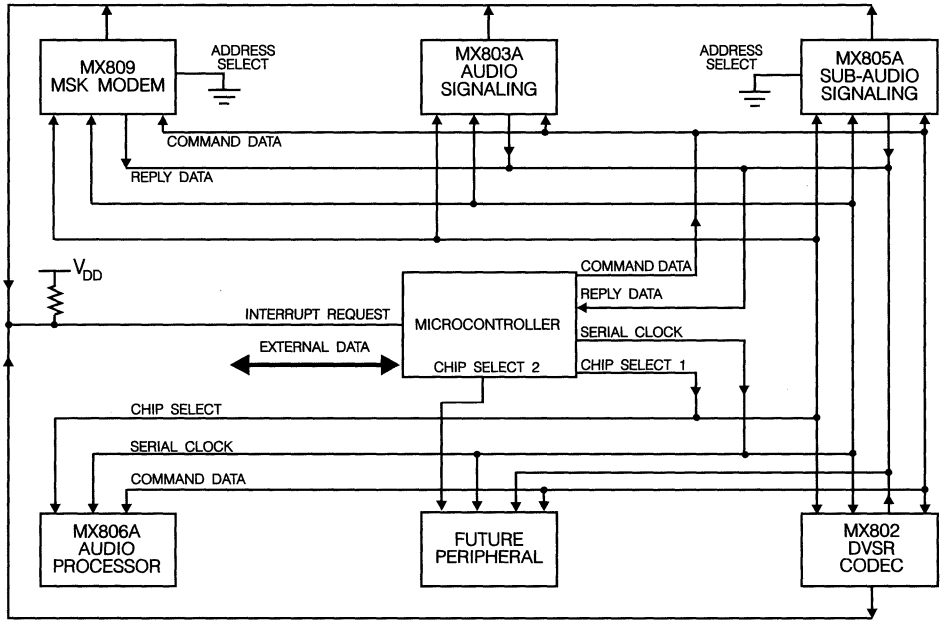


Figure 3 - Example C-BUS Hardware Interconnections

C-BUS Serial Interfacing

C-BUS is the controlling hardware and software interface for all members of the DBS 800 family. It enables the serial, bi-directional transfer of commands and data throughout the system, allowing total flexibility of operational control and data handling. System upgrades can be achieved by a simple software or firmware change.

C-BUS Hardware Interface

The BUS physically consists of 5 lines:

- **Serial Clock line** - driven by the microcontroller to all peripherals. All C-BUS commands and data transfers are synchronized, in bursts of 8 bits, to this clock.
- **Command Data** - to address, command, and transfer data from the microcontroller to a selected peripheral.
- **Reply Data line** - transfer of requested (commanded) data from the addressed peripheral as the result of a specific Address/Command (A/C).
- **Chip Select (CS) line** - carries the CS timing command from the microcontroller to all peripherals. All C-BUS sequences are initiated, completed, or aborted by this CS signal. (See Timing Diagrams in respective DBS 800 data bulletins.) All peripherals on the C-BUS will receive the CS signal, but only the peripheral that is addressed will react. Table 4 contains a list of all DBS 800 C-BUS Address allocations.
- **Interrupt Request (IRQ) line** - interactive peripherals have an Interrupt output (IRQ) for connection to the microcontroller interrupt input.

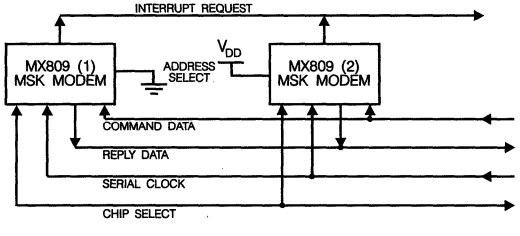


Figure 4 - MX809 Modems for Full-Duplex Operation

Full-Duplex Configuration

Figure 4 shows the configuration of the Address Select inputs when using 2 MX809 Modems on the C-BUS. MX805A Sub-Audio Signaling Processors should be embodied in the same manner when full-duplex operation is required.

C-BUS Serial Clock Rate

Generally, C-BUS Serial Clock rates that are harmonically related to the Xtal/Clock = 32 frequency cannot produce alias effects within a microcircuit, therefore using a C-BUS Serial Clock rate at this frequency is preferable. If is proves impractical to select a synchronous C-BUS clock, coupling between sensitive analog inputs (such as the MX806A Mic. Inputs) and the C-BUS should be avoided.

10

"C-BUS" Controlling System

The Use of C-BUS Software and Protocol

Each individual DBS 800 Data Bulletin contains a table listing the C-BUS commands and instructions relevant to that peripheral. Table 4 gives an abridged list of all DBS 800 address allocations.

All transactions begin with the CS line going to a logic "0" level (Figure 5). The first byte that must be transmitted to the peripheral, on the Command Data line, is an Address/Command (A/C) byte. Generally, all bytes are transmitted MSB first.

Address/Command (A/C) Byte

Part of this byte is the "Address" that specifies which IC (or ICs) has been selected for that particular transaction. The second part of the A/C is the "Command" to fulfill a particular function (see Table 4).

The A/C may be followed by either

(a) a qualifying instruction, or

(b) data bytes from the microcontroller via the Command Data line or from the peripheral via the Reply Data line.

Example C-BUS Transactions

Address/Command byte $\mathbf{61}_H$ is recognized as:

Address	/	Command
MX802 DVSR Codec	/	*Read Status Register*

- and in this case would be followed by 1 byte of Status data transmitted on the Reply Data line from the MX802 to the microcontroller.

Address/Command byte $\mathbf{10}_H$ is recognized as:

Address	/	Command
MX806A Audio Processor	/	*Control Command*

- and in this case would be followed by 1 byte of Control data transmitted on the Command Data line from the microcontroller to the MX806A.

Address/Command byte $\mathbf{01}_H$ is recognized as:

Address	/	Command
General Reset		

- and in this case will reset ALL DBS 800 ICs connected to the C-BUS. (Individual IC Data Bulletins give details of the General Reset actions.)

DBS 800 IC Sampling Rates

IC Functions		Xtal/Clock Frequencies (MHz) 4.00	4.032	4.096
		Sample Clock Rates (kbit/s)		
MX802DVSR Codec				
Voice Filters	at 16, 32 & 64 kbps	125	126	128
Voice Filters	at 25 & 50 kbps	100	100.8	102.4
Voice Sample Rates	16.0kbps	15.625	15.75	16.0
	25.0kbps	25.0	25.2	25.8
(Nominal)	32.0kbps	31.25	31.5	32.0
	50.0kbps	50.0	50.4	51.2
	64.0kbps	62.5	63.0	64.0
MX803A Audio Signaling Processor				
Tone Filters	Max	166	168	170
	Min.	13.15	13.28	13.47
Digital Filters	High	13.8	14.0	14.2
	Mid.	6.9	7.0	7.1
	Ext.	27.0	28.0	28.4
MX805A Sub-Audio Signaling Processor				
Voice Filters		125	126	
TX Filters	Max.	62.5	63.0	
	Min.	12.5	12.6	
RX Filters		35.7	36.0	
	or	25.0	25.2	
Digital Filters		1.04	1.05	
MX806A LMR Audio Processor				
Voice Filters		125	126	
MX809 MSK Modem				
TX Filters		250	252	
	or	166	168	
RX Filters		125	126	

If the Xtal/Clock frequency 4.096 MHz is used with the MX805A, MX806A, or MX809, it may result in sampling clock rates that place the voice-filter passband frequencies outside CEPT specifications.

Table 3 - Examples of DBS 800 IC sample rates relative to Xtal/Clock inputs

10

"C-BUS" Controlling Protocol

(a) C-BUS Address Listing: C-BUS Addresses (HEX) currently allocated to DBS 800 ICs.

C-BUS Performance Testing	00
General (all device) Reset	01
Audio Processor	**MX806A**
Control Command	10
Mode Command	11
Modulator Levels Set	12
Volume Set	13
Audio Signaling Processor	**MX803A**
Write to Control Register	30
Read Status Register	31
Read RX Tone Frequency	32
Write to Notone Timer	33
Write to TX Tone Generator 1	34
Write to TX Tone Generator 2	35
Write to G/Purpose Timer	36
MSK Modem 1	**MX809**
Write to Control Register	40
Read Status Register	41
Read RX Data Buffer	42
Write to TX Data Buffer	43
Write to Sync Program	44
MSK Modem 2	**MX809**
Write to Control Register	48
Read Status Register	49
Read RX Data Buffer	4A
Write to TX Data Buffer	4B
Write to Sync Program	4C
C-BUS Performance Testing	55

DVSR Codec	**MX802**
Write to Control Register	60
Read Status Register	61
Store "N" pages, Start page X (immediate)	62
Store "N" pages, Start page X (buffered)	63
Play "N" pages, Start page X (immediate)	64
Play "N" pages, Start page X (buffered)	65
Write Data, Start page P	66
Read Data, Start page P	67
Write Data, Continue	68
Read Data, Continue	69
Sub-Audio Signaling Processor 1	**MX805A**
Write to Control Register	70
Read Status Register	71
Read CTCSS RX Data	72
Write to CTCSS/NRZ TX	73
Read NRZ RX Data	74
Write to NRZ Data TX	75
Write to Gain Set	76
Sub-Audio Signaling Processor 2	**MX805A**
Write to Control Register	78
Read Status Register	79
Read CTCSS RX Data	7A
Write to CTCSS/NRZ TX	7B
Read NRZ RX Data	7C
Write to NRZ Data TX	7D
Write to Gain Set	7E
C-BUS Performance Testing	AA
C-BUS Performance Testing	FF

(b) Reserved Addresses: C-BUS Addresses (HEX) reserved for future DBS 800 IC/system use.

General Functions	02 to 07	Future Sub-Audio Signaling Processors	77
Future Audio Processors	14 to 1F	Future Sub-Audio Signaling Processors	7F
Future Speech Products	20 to 2F	Future Products	80 to 8F
Future Audio Signaling Processors	37 to 3F	Future Products	90 to 9F
Future MSK Modems	45 to 47	Future Products	D0 to DF
Future MSK Modems	4D to 4F	Future Products	E0 to EF
Future DVSR Codecs	6A to 6F		

(c) Spare Addresses: C-BUS Addresses (HEX) that will not be allocated for DBS 800 IC/system use and are available for custom use.

08 to 0F	50 to 54	56 to 5F	A0 to A9
AB to AF	B0 to BF	C0 to CF	F0 to FE

Table 4 - C-BUS Address Allocations

General Reset

The General Reset command (01_H), when transmitted from the microcontroller, is non-selective and will reset all DBS 800 ICs connected to the C-BUS. Detailed information on the way this command affects each DBS 800 device can be found in individual Data Bulletins.

C-BUS Performance Testing

To enable the effect of C-BUS activity on audio noise levels to be assessed, 4 addresses are allocated for C-BUS performance testing:

00_H	00000000	-all 0's
55_H	01010101	-bit reversals
AA_H	10101010	-bit reversals
FF_H	11111111	-all 1's

These bytes, which do not produce any changes in current, active DBS 800 settings and configurations, provide C-BUS activity. These A/C bytes, when following a $\overline{CS}$ edge, are ignored by the DBS 800 chip set and can be loaded as Command Data individually, or in common or mixed groups.

DBS800 Devkit Introduction

OVERVIEW

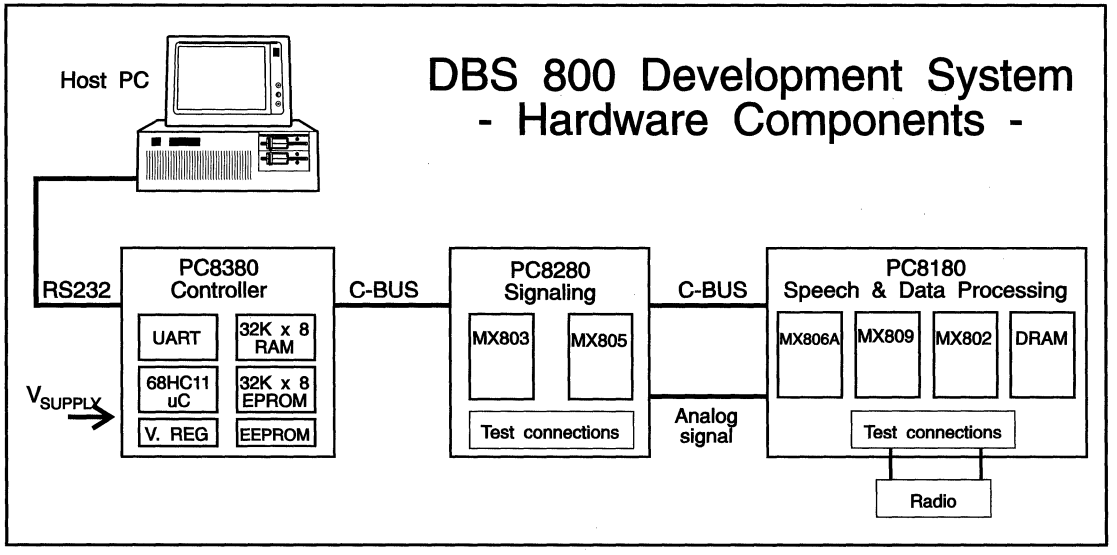
The DBS800 Development System (Devkit) is a general purpose hardware and software platform for:

- The evaluation and functional testing of DBS800 devices (the MX802, MX803A, MX805A, MX806A & MX809).
- The demonstration and evaluation of DBS800 group functions.
- A base for use in developing application-specific software routines.

This document provides a general introduction to the Development System. Additional software and supporting documentation is available that demonstrates DBS800 application-specific functions, such as Voice Management, Data Communications, Sub-Audio Signaling and Selective Calling.

SYSTEM COMPONENTS

The complete DBS800 Development System consists of three printed circuit boards (PC8380, PC8280 & PC8180) with their interconnecting cables, software on diskette and EPROM, and supporting documentation. Access to the system is through a 'Host' PC.



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HARDWARE

The PC8180 Speech and Data Board is used for the evaluation of the MX802 DVSR Codec, MX806A Audio Processor and MX809 MSK Modem devices. It is controlled by a C-BUS link from the PC8380 controller board, and includes peripheral components, test links and connectors to allow the devices to be tested individually or in several representative combinations. For a detailed description of this board, see the document "PC8180 Speech and Data DevKit Documentation."

The PC8280 Signaling Board provides a similar hardware platform for evaluation of the MX803 Audio Signaling Processor and MX805 Sub-Audio Signaling Processor and is fully described in "PC8280 Signaling DevKit Documentation."

The PC8380 Controller Board contains a 68HC11 microcontroller with RAM, EPROM, EEPROM, C-BUS and RS232 ports, and is used to control the DBS800 devices on the attached PC8180 and/or PC8280 boards. For DBS800 device evaluation, the PC8380 may run under the direct control of the 'Host' PC or it may run a special test program downloaded from the 'Host' PC. "PC8380 Controller DevKit Documentation" gives a complete description of this board.

In some circumstances you may wish to use two sets of boards, for example to evaluate the end to end performance of a link using the (half duplex) MX809 MSK Modem devices. You could use a separate 'Host' PC to control each set of boards, but the Development System also lets you connect two sets of PC8180/8280/8380 boards to a single PC.

The **'Host' PC** can be any IBM compatible 80*88 or 80*86 based computer running MS-DOS (or PC-DOS) V 2.0 or greater with at least 512k bytes of RAM, a disk drive and an RS232 port (COM1 or COM2) capable of running at 9600 baud. A color graphics display, hard disk drive, and a second RS232 port are useful but not essential. Although the software will run on a PC/XT, a faster machine will give a smoother response to the user's input.

SOFTWARE

The **software components** of the Development System are DLINK86 (the 'Host' PC control software), DLINK11 (which controls the 68HC11 microcontroller on the PC8380 board), and various special DBS800 device evaluation programs. DLINK11 is contained in an EPROM on the PC8380 board. Other software is supplied on a diskette.

The Evaluation diskette supplied with the DBS800 Development System contains all of the programs needed to run the system:

DLINK86.EXE:	the 'Host' PC software.
Various '.HEX' files:	specific device test programs.

You will also receive a diskette for LTR evaluation (p/n 40450005.001) and one for DCS evaluation (p/n 40450006.001).

The diskettes also contain contain source files, of interest to a programmer but not needed to actually run the system. In addition, there may be a READ.ME text file on the disk, giving details of any recent updates to the programs or their use. The DBS800 Development System software may be run from diskette or from a hard disk.

Pvt SQUELCH: COMBINING CTCSS WITH VOICE BAND INVERSION

By Chris Hayes

Radio channels are in short supply, and putting two or more plumbers, electrical contractors or other competing businesses on the same shared frequency can conserve spectrum. Radio system operators have been reluctant to do so because customers dislike knowing that competitors can overhear their communications.

Private squelch combines continuous tone-controlled squelch system (CTCSS) with inverted speech to prevent users from understanding each others' communications unless the transmissions are accompanied by the group's assigned tone. Such privacy is easy to implement under CTCSS control, and it is available to all, making it possible for competitors to share the same radio frequency with a minimum risk of complaints.

CTCSS background

CTCSS equipment was first installed around 1956. Those early "Private Line" or "PL" systems employed tuning forks to generate and detect subaudible tones, tones still commonly used throughout the two-way radio industry. Since 1956, vacuum tubes have been set aside for transistors, and later, transistors combined by the thousands into integrated circuits, but CTCSS still dominates as the simplest, most dependable way to segregate the voice traffic of diverse user groups sharing the same radio channel.

Private squelch carries this process one step further. Speech transmissions are made private through fixed frequency inversion. Only the detection of the user group's unique CTCSS tone assignment enables clear recovery of inverted speech. As with any CTCSS application, the subaudible tone unmutes the radio's speaker; remove the tone and the speaker is silent.

Thus, before making a call, the caller must check the channel's occupancy to avoid "stepping on" the conversation of others. This necessary monitoring process allows eavesdropping. In fact, monitoring requires eavesdropping. Private squelch conversations are audible, but those outside the group cannot understand what is being said.

Voice band inverter

Privacy is achieved with a monolithic voice band inverter. This CMOS IC includes switched capacitor high-pass and low-pass filters, a double-balanced mixer, a fixed-inversion carrier and analog gates for receive/transmit and private/clear switching. Filtering and carrier frequency generation derive from an external 1MHz clock of the same kind most CTCSS encoder-decoder ICs use.

To invert, speech first passes through the high-pass filter and then mixes with the carrier in the double-balanced mixer. The resultant sum and difference product is fed to the low-pass filter, which attenuates all components except the lower sideband. The lower sideband modulates the RF carrier. The net effect is that low-frequency speech components are translated to the high end of the speech band, and frequencies in the high end are translated to the low end. Because speech is, in effect, frequency-coded in the human brain, this translation procedure renders the code unfamiliar and, therefore, unintelligible.

To recover clear speech, the process is reversed. In the private squelch application, the user's assigned CTCSS tone controls clear recovery. Because modern CTCSS encoder-decoders are programmable to 38 CTCSS tones, there are 38 privacy keys per radio channel.

Private squelch should be equally compatible with digitally coded squelch, such as the Digital Private Line or the Logic Trunked Radio trunking system, because they use signaling frequencies in the subaudible range.

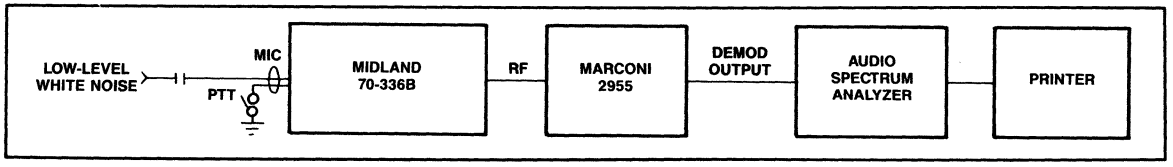

FIGURE 1. To record and produce private squelch spectrum diagrams, low-level white noise is fed to a two-way radio mic input. A radio communications test set demodulates the RF output and feeds it to an audio spectrum analyzer. The analyzer drives a printer that draws the diagrams.

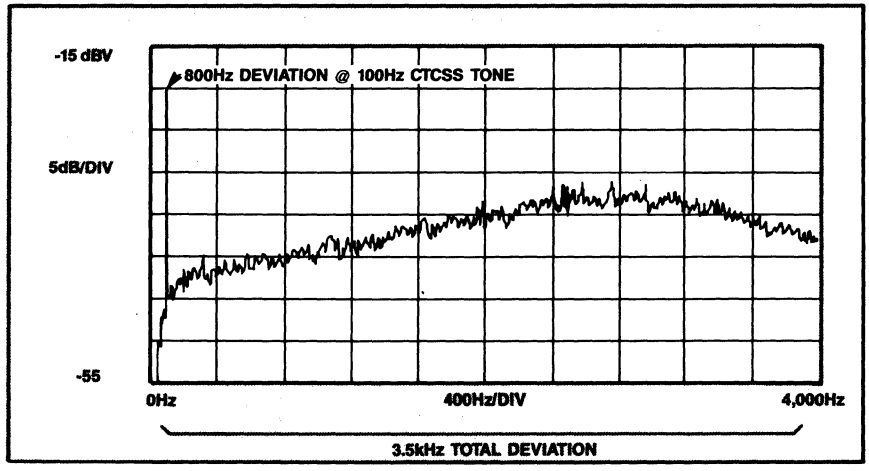

Figure 2. The private squelch voice band inverter's filtered but uninverted audio, transmitted by a typical radio, is shown with a 71.9Hz CTCSS frequency. The tone's deviation is set to the usual 500 Hz.

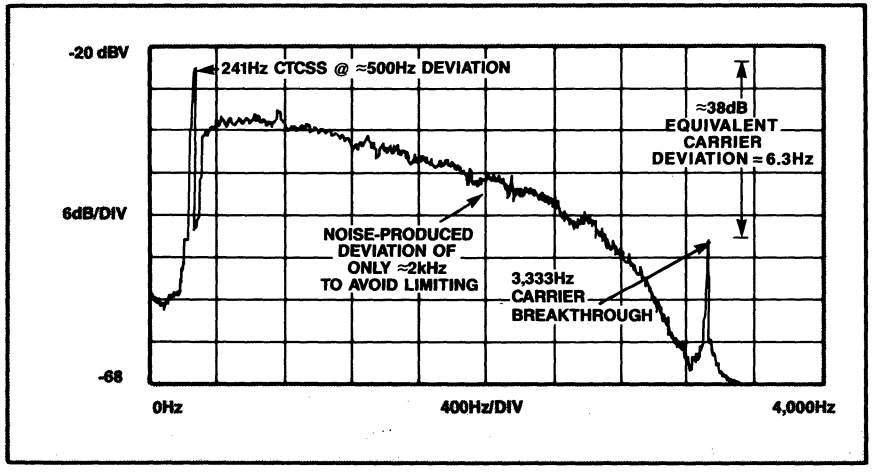

Figure 3. The private squelch voice band inverter's passband is shown inverted. Low-frequency speech components appear to the right; high frequencies to the left. At the far left is an undisturbed 241.8Hz CTCSS tone. At the far right, an undesired residual 3,333Hz carrier with a deviation level of only 6.3Hz at a level 38dB down from the CTCSS tone.

Pre-emphasis effects

Speech inversion scrambling introduces some special application problems. The power spectrum of speech is not flat but exhibits a peak near 800Hz. Radio transmitters require voice to be pre-emphasized before modulation. Receivers then must de-emphasize the recovered speech equally to compensate for the original pre-emphasis. The ideal result achieves a flat power spectrum for transmission.

But when speech is modulated with a carrier for inversion, the speech power spectrum shifts away from the normal 800Hz center on which the radio transmitter's pre-emphasis filter design is based. The recovered voice sounds distorted and unnatural.

To overcome this problem, the voice band inverter is treated as a radio. Audio is pre-emphasized 6dB/octave on its way in, and de-emphasized the same amount on

its way out. This renders an inverted product with a power spectrum the radio can process at its microphone port the same way it processes natural speech. The result sounds sufficiently natural, and few can distinguish the recovered audio from the original. Some, perhaps with a trained ear and the knowledge of which is which, report they can hear a single-sideband radio quality in the recovered audio.

The coexistence of voice with a CTCSS tone makes private squelch filtering requirements more demanding. Low-level CTCSS tones become prominent if translated to the high end of the voice band. The fact that few systems adequately block speech from the sub-300Hz region where CTCSS tones are assigned aggravates the problem.

Most radio transmitters provide only the 6dB/octave pre-emphasis filter the FCC rules mandate for the 300Hz to 3,000Hz voice band. A linear extrapolation of this curve into the subaudio band yields an attenuation of speech energy at 250Hz (the highest of the CTCSS tones) of only 1.6dB with reference to 300Hz. No doubt this is why many CTCSS systems do not offer tones much above 200Hz. But even at 200Hz, voice is down only 3.4dB from the bottom of the speech band, 100Hz removed. At that level, speech tends to interfere with CTCSS decoding or, just as bad, the tone is audible in speech.

The voice band inverter offers a solution. Used simply as a microphone filter, it attenuates frequencies below 300Hz by 36dB to 40dB, providing effective use of all CTCSS tones (even in the clear mode) and preventing CTCSS tones from being heard in the voice band. This not only separates CTCSS from voice, but it assumes ready passage of the joint tone and voice product through repeaters.

If DTMF signals are used, they should be injected at the radio's tone port, bypassing the audio inversion process.

It would be a mistake to offer private squelch as a speech security system. Although simple fixed-inversion products traditionally are called "scramblers" and their inversion carriers are considered a "secret," such "codes" easily are broken with ordinary laboratory equipment. Even so, units of comparable security have sold for as much as $1,000.

Ask the typical radio users, "Do you have anything to hide?" "No," they answer. Then ask, "What rights do others have to your radio dispatches?" That answer is, "None." That is because a taxi dispatch is not ordinarily viewed as something to hide. Why would such users pay an appreciable sum to buy a scrambler for which they do not perceive a need?

Private squelch is not designed for the radio user with something to hide; it is offered rather as an enhanced form of CTCSS. It offers a simple, low-cost method for achieving privacy of the two-way radio: just enough privacy, at an incidental cost, such that radio users are blocked from an opportunity to eavesdrop. The perception of two-way radio is changed from that of an open-channel free-for-all to something substantially less public.

The security of any single-band inversion system may be breached easily by the dedicated eavesdropper with a signal generator and some filter expertise. The anal-

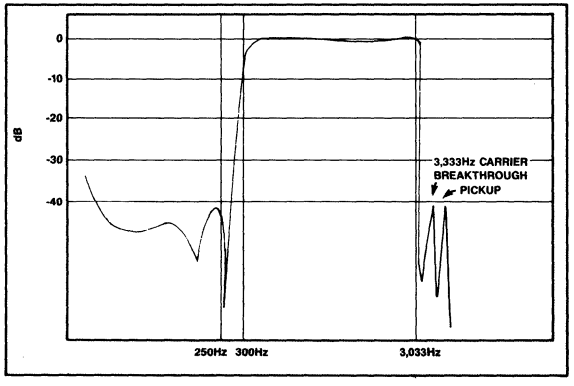

Figure 4. The audio response characteristics of a private squelch voice band inverter, before pre-emphasis or de-emphasis and before installation.

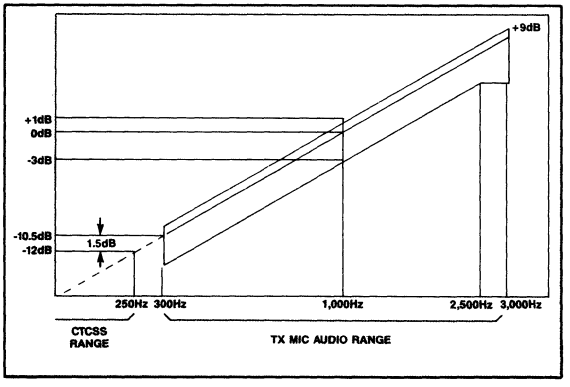

Figure 5. The EIA-152-B Minimum Standard for Land Mobile FM or PM Transmitters gives a 6dB/octave pre-emphasis characteristic for a radio transmitter's 300Hz to 3,000Hz voice band. Notice that CTCSS audio at 250Hz is down only 1.5dB from the filter's 300Hz passband on this slope.

ogy might be made to a sealed letter, in contrast to a postcard. Although easy for anyone to open, generally only the addressee reads a letter.

With private squelch, perhaps the letter is locked in a mailbox. To get the information, one must either have a key or pick the lock. Without private squelch, radio messages are like postcards, with a content available to anyone. This is no public right to the content, only ready access.

Private squelch offers a simple form of privacy to millions who use radio party lines. The privacy is achieved without reducing audio quality or adding high-priced hardware. It is achieved by applying integrated circuit technology to a signaling system an early CTCSS equipment manufacturer had the foresight to call "Private Line."

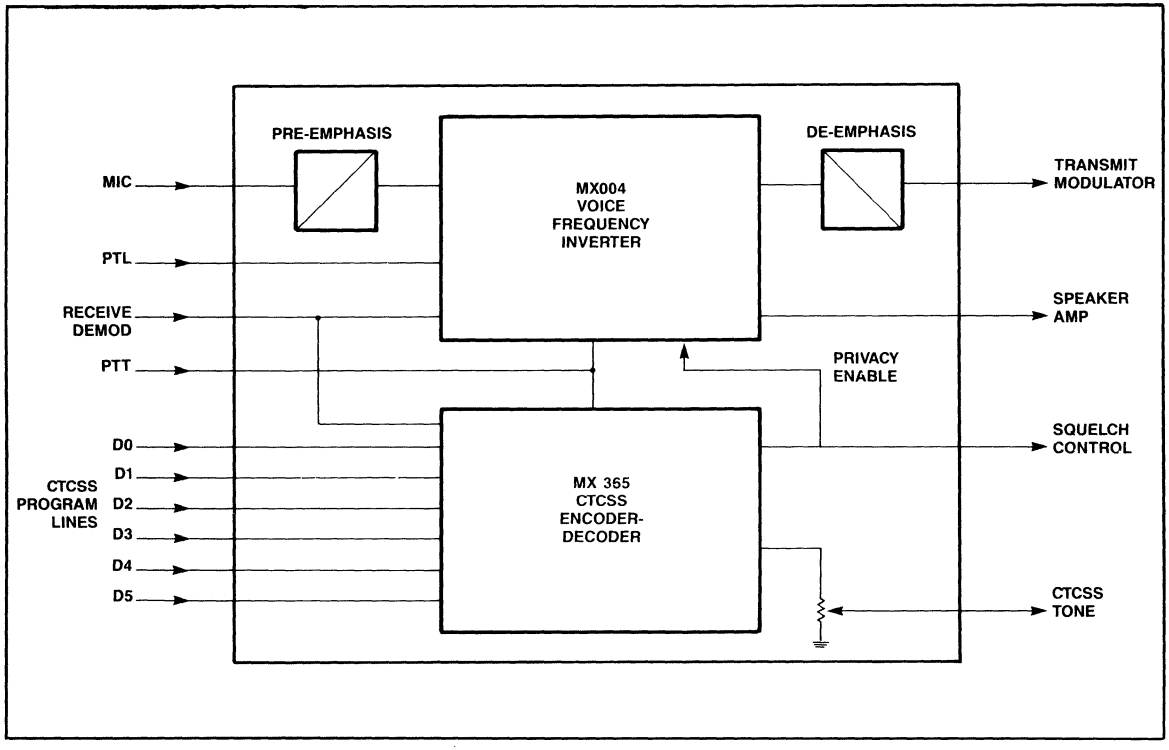

FIGURE 6. A block diagram of the typical private squelch encoder-decoder. A private squelch adapter, for systems in which the CTCSS encoder-decoder already exists, need only include emphasis and speech inverting filters. The adapter's monolithic implementation allows a board the size of a postage stamp, a board that fits most radios.

Generation of Non-Standard CTCSS Tones

MX•COM manufactures several integrated circuits which encode and decode CTCSS tones at the EIA RS-220 standard frequencies. In many instances, however, using tones of slightly different frequencies may be desirable. Because these MX•COM ICs use switched capacitor technology, tone frequencies may shifted simply by changing the crystal or clock input. The following three tables list alternative tones which can be encoded and decoded by the MX365A and the MX375, and encoded by the MX315A.

Each table lists the tone frequencies for three crystal values for each chip. The MX315A and MX365A use a nominal crystal value of 1.0 MHz; the table lists tone frequencies for 1.008 MHz and 1.024 MHz crystals as well as for 1.0 MHz. The MX375 uses a 4.0 MHz nominal crystal value; its table lists frequencies for 4.0 MHz, 4.032 MHz, and 4.096 MHz crystals. The column labeled as "Divisor" for each table lists the quotient of the clock frequency divided by the tone frequency. This column can be used to calculate the clock frequency required to generate other tone frequencies. Each table also lists the (D5-D0) program code input associated with each divisor and tone frequency group. Each code is listed in both binary and hexadecimal formats. As an example, to encode a 70.0 Hz tone with the program code input D5-D0 = 011111 (1F Hex), the required clock would be calculated in the following manner:

D5	D4	D3	D2	D1	D0
0	1	1	1	1	1

Divisor = 13908
Tone frequency = 70.0 Hz
Required clock frequency = Divisor * Tone Frequency
= 13908 * 70.0 Hz
= 973560 Hz

When using these ICs in this manner, you must remember the following:

1) When the clock is changed, the audio pass band limits will change proportionately. These changes will be fairly small, however. For example, in the MX365A using a 1.024 MHz crystal, the lower limit will change to (1.024/1.0) * 300 = 307 Hz, and the upper limit will change to (1.024/1.0) * 3000 = 3072 Hz.

2) In the MX375, the frequency inversion carrier frequency will also change proportionately from its nominal value of 3333 Hz. For example, with a 4.096 MHz clock, the carrier frequency will change to (4.096/4.0) * 3333 Hz = 3413 Hz. For proper communication, the transmitter and receiver must use the same inversion carrier frequency.

Device: MX365A

Divisor	Xtal Freq 1.0 MHz	Xtal Freq 1.008 MHz	Xtal Freq 1.024 MHz	Program Codes Binary D5	D4	D3	D2	D1	D0	Hex
14914	67.05	67.59	68.66	1	1	1	1	1	1	3F
14426	69.32	69.87	70.98	1	1	1	0	0	1	39
13908	71.90	72.48	73.63	0	1	1	1	1	1	1F
13450	74.35	74.94	76.13	1	1	1	1	1	0	3E
12994	76.96	77.58	78.81	0	0	1	1	1	1	0F
12536	79.77	80.41	81.68	1	1	1	1	0	1	3D
12108	82.59	83.25	84.57	0	1	1	1	1	0	1E
11712	85.38	86.06	87.43	1	1	1	1	0	0	3C
11285	88.61	89.32	90.74	0	0	1	1	1	0	0E
10919	91.58	92.31	93.78	1	1	1	0	1	1	3B
10553	94.76	95.52	97.03	0	1	1	1	0	1	1D
10279	97.29	98.07	99.62	1	1	1	0	1	0	3A
10004	99.96	100.76	102.36	0	0	1	1	0	1	0D
9668	103.43	104.26	105.91	0	1	1	1	0	0	1C
9333	107.15	108.01	109.72	0	0	1	1	0	0	0C
9028	110.77	111.66	113.43	0	1	1	0	1	1	1B
8723	114.64	115.56	117.39	0	0	1	0	1	1	0B
8418	118.80	119.75	121.65	0	1	1	0	1	0	1A
8143	122.80	123.78	125.75	0	0	1	0	1	0	0A
7869	127.08	128.10	130.13	0	1	1	0	0	1	19
7595	131.67	132.72	134.83	0	0	1	0	0	1	09
7320	136.61	137.70	139.89	0	1	1	0	0	0	18
7076	141.32	142.45	144.71	0	0	1	0	0	0	08
6832	146.37	147.54	149.88	0	1	0	1	1	1	17
6619	151.09	152.30	154.72	0	0	0	1	1	1	07
6374	156.88	158.14	160.65	0	1	0	1	1	0	16
6161	162.31	163.61	166.21	0	0	0	1	1	0	06
5947	168.14	169.49	172.18	0	1	0	1	0	1	15
5764	173.48	174.87	177.64	0	0	0	1	0	1	05
5551	180.15	181.59	184.47	0	1	0	1	0	0	14
5368	186.29	187.78	190.76	0	0	0	1	0	0	04
5185	192.86	194.40	197.49	0	1	0	0	1	1	13
4910	203.65	205.28	208.54	0	0	0	0	1	1	03
4758	210.17	211.85	215.21	0	1	0	0	1	0	12
4575	218.58	220.33	223.83	0	0	0	0	1	0	02
4422	226.12	227.93	231.55	0	1	0	0	0	1	11
4270	234.19	236.06	239.81	0	0	0	0	0	1	01
4148	241.08	243.01	246.87	0	1	0	0	0	0	10
3996	250.28	252.28	256.29	0	0	0	0	0	0	00

Device: MX375

Divisor	Xtal Freq 4.0 MHz	Xtal Freq 4.032 MHz	Xtal Freq 4.096 MHz	Program Codes Binary D5	D4	D3	D2	D1	D0	Hex
59657	67.05	67.59	68.66	1	1	1	1	1	1	3F
55633	71.90	72.48	73.63	0	1	1	1	1	1	1F
53800	74.35	74.94	76.13	1	1	1	1	1	0	3E
51975	76.96	77.58	78.81	0	0	1	1	1	1	0F
50144	79.77	80.41	81.68	1	1	1	1	0	1	3D
48432	82.59	83.25	84.57	0	1	1	1	1	0	1E
46849	85.38	86.06	87.43	1	1	1	1	0	0	3C
45142	88.61	89.32	90.74	0	0	1	1	1	0	0E
43678	91.58	92.31	93.78	1	1	1	0	1	1	3B
42212	94.76	95.52	97.03	0	1	1	1	0	1	1D
41114	97.29	98.07	99.62	1	1	1	0	1	0	3A
40016	99.96	100.76	102.36	0	0	1	1	0	1	0D
38673	103.43	104.26	105.91	0	1	1	1	0	0	1C
37331	107.15	108.01	109.72	0	0	1	1	0	0	0C
36111	110.77	111.66	113.43	0	1	1	0	1	1	1B
34892	114.64	115.56	117.39	0	0	1	0	1	1	0B
33670	118.80	119.75	121.65	0	1	1	0	1	0	1A
32573	122.80	123.78	125.75	0	0	1	0	1	0	0A
31476	127.08	128.10	130.13	0	1	1	0	0	1	19
30379	131.67	132.72	134.83	0	0	1	0	0	1	09
29280	136.61	137.70	139.89	0	1	1	0	0	0	18
28305	141.32	142.45	144.71	0	0	1	0	0	0	08
27328	146.37	147.54	149.88	0	1	0	1	1	1	17
26474	151.09	152.30	154.72	0	0	0	1	1	1	07
25497	156.88	158.14	160.65	0	1	0	1	1	0	16
24644	162.31	163.61	166.21	0	0	0	1	1	0	06
23790	168.14	169.49	172.18	0	1	0	1	0	1	15
23057	173.48	174.87	177.64	0	0	0	1	0	1	05
22204	180.15	181.59	184.47	0	1	0	1	0	0	14
21472	186.29	187.78	190.76	0	0	0	1	0	0	04
20740	192.86	194.40	197.49	0	1	0	0	1	1	13
19642	203.65	205.28	208.54	0	0	0	0	1	1	03
19032	210.17	211.85	215.21	0	1	0	0	1	0	12
18300	218.58	220.33	223.83	0	0	0	0	1	0	02
17690	226.12	227.93	231.55	0	1	0	0	0	1	11
17080	234.19	236.06	239.81	0	0	0	0	0	1	01
16592	241.08	243.01	246.87	0	1	0	0	0	0	10
15982	250.28	252.28	256.29	0	0	0	0	0	0	00

Device: MX315A

Divisor	Xtal Freq 1.0 MHz	Xtal Freq 1.008 MHz	Xtal Freq 1.024 MHz	Program Codes Binary D5	D4	D3	D2	D1	D0	Hex
14912	67.06	67.60	68.67	1	1	1	1	1	1	3F
14415	69.37	69.93	71.04	1	1	1	0	0	1	39
13920	71.84	72.41	73.56	0	1	1	1	1	1	1F
13454	74.33	74.92	76.11	1	1	1	1	1	0	3E
12989	76.99	77.61	78.84	0	0	1	1	1	1	0F
12555	79.65	80.29	81.56	1	1	1	1	0	1	3D
12121	82.50	83.16	84.48	0	1	1	1	1	0	1E
11718	85.34	86.02	87.39	1	1	1	1	0	0	3C
11284	88.62	89.33	90.75	0	0	1	1	1	0	0E
10943	91.38	92.11	93.57	1	1	1	0	1	1	3B
10540	94.88	95.64	97.16	0	1	1	1	0	1	1D
10261	97.46	98.24	99.80	1	1	1	0	1	0	3A
10013	99.87	100.67	102.27	0	0	1	1	0	1	0D
9672	103.39	104.22	105.87	0	1	1	1	0	0	1C
9331	107.17	108.03	109.74	0	0	1	1	0	0	0C
9021	110.85	111.74	113.51	0	1	1	0	1	1	1B
8711	114.80	115.72	117.56	0	0	1	0	1	1	0B
8432	118.60	119.55	121.45	0	1	1	0	1	0	1A
8122	123.12	124.10	126.07	0	0	1	0	1	0	0A
7843	127.50	128.52	130.56	0	1	1	0	0	1	19
7595	131.67	132.72	134.83	0	0	1	0	0	1	09
7316	136.69	137.78	139.97	0	1	1	0	0	0	18
7068	141.48	142.61	144.88	0	0	1	0	0	0	08
6851	145.96	147.13	149.46	0	1	0	1	1	1	17
6603	151.45	152.66	155.08	0	0	0	1	1	1	07
6386	156.59	157.84	160.35	0	1	0	1	1	0	16
6169	162.10	163.40	165.99	0	0	0	1	1	0	06
5952	168.01	169.35	172.04	0	1	0	1	0	1	15
5766	173.43	174.82	177.59	0	0	0	1	0	1	05
5549	180.21	181.65	184.54	0	1	0	1	0	0	14
5363	186.46	187.95	190.94	0	0	0	1	0	0	04
5177	193.16	194.71	197.80	0	1	0	0	1	1	13
4929	202.88	204.50	207.75	0	0	0	0	1	1	03
4836	206.78	208.44	211.75	1	1	1	0	0	0	38
4743	210.84	212.53	215.90	0	1	0	0	1	0	12
4588	217.96	219.70	223.19	0	0	0	0	1	0	02
4433	225.58	227.38	230.99	0	1	0	0	0	1	11
4278	233.75	235.62	239.36	0	0	0	0	0	1	01
4123	242.54	244.48	248.36	0	1	0	0	0	0	10
3999	250.06	252.06	256.06	0	0	0	0	0	0	00

The EIA RS-220 specification divides the standard frequencies into three groups. They are tabulated below with the program codes used in MX-COM ICs:

Group A		Group B		Group C	
Freq	**Code**	**Freq**	**Code**	**Freq**	**Code**
67.0	3F	71.9	1F	74.4	3E
77.0	0F	82.5	1E	79.7	3D
88.5	0E	94.8	1D	85.4	3C
100.0	0D	103.5	1C	91.5	3B
107.2	0C	110.9	1B		
114.8	0B	118.8	1A	97.4	3A
123.0	0A	127.3	19	69.3	39
131.8	09	136.5	18	206.5	38
141.3	08	146.2	17		
151.4	07	156.7	16		
162.2	06	167.9	15		
173.8	05	179.9	14		
186.2	04	192.8	13		
203.5	03	210.7	12		
218.1	02	225.7	11		
233.6	01	241.8	10		
250.3	00				

Note that with the exception of the 67.0 Hz tone in Group A, the programming codes are in reverse sequential order in relation to the tone frequencies for each group. Again, with the exception of 67.0 Hz, also note that the first hexadecimal digit for Group A is 0, the first digit for Group B is 1, and the first digit for group C is 3.

For more general information about these ICs, see the MX-COM Product Handbook and the MX-COM MX315A and MX365A Data Bulletins.

MX-COM does not test its CTCSS ICs (MX315A, MX365A, MX375) at crystal or clock frequencies other than the nominal frequency specified in the Product Handbook or Data Bulletin, and as such, makes no guarantee of the performance of the device when used with a non-specified crystal or clock frequency. MX-COM does not assume responsibility for the use of its ICs in the manner described in this application note in any circuit or product.

Split-Band Scrambling Furnishes Voice Security

Voice scrambling offers tactical security for radio dispatch communications. It takes so long, even for a dedicated eavesdropper, to unscramble your transmissions that the information would be worthless by then.

By Steve Kelley and Hank Wallace

Unwanted consequences of third-party radio communications eavesdropping include foiled drug busts, unsolved burglaries and pirated business opportunities. Some mobile radio users employ voice privacy and voice security devices to scramble their communications. Most users who need voice security continue to communicate in the clear, however, for several reasons:

(1) Cost --They cannot justify the captial expense.

(2) Technology -- The poor quality of recovered audio and the radio range reduction common to many voice security systems discourage their use.

(3) Availability -- Two principal scrambling alternatives, frequency inversion and digital encryption, are not suitable for many applications. Frequency inversion offers privacy but not security; digital encryption offers high security but with a high price tag.

Semiconductor technology advances have reduced costs and improved the quality of voice security products. Variable Split-Band (VSB) scrambling has become economical because of such advances.

How it works

Filters separate the voice band (400Hz to 2700Hz) into a pair of subbands (32 pairs are possible). (See Figures 1A, 1B and 1C.) A mixer fed with a carrier signal inverts the subbands; a summing amplifier recombines them. Ordinary radio transceiv-

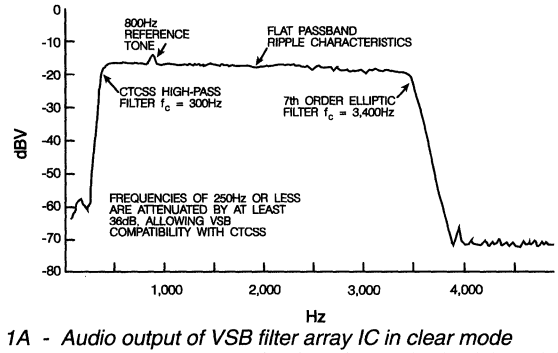

Figure 1A - Audio output of VSB filter array IC in clear mode

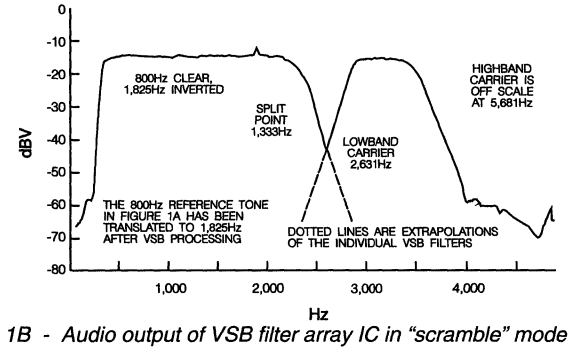

Figure 1B - Audio output of VSB filter array IC in "scramble" mode with split point at 2,333Hz.

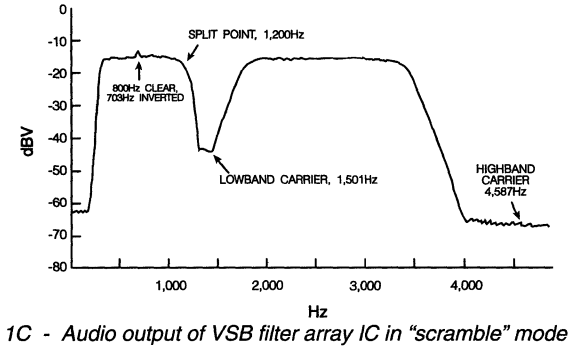

Figure 1C - Audio output of VSB filter array IC in "scramble" mode with split point at 1,200Hz.

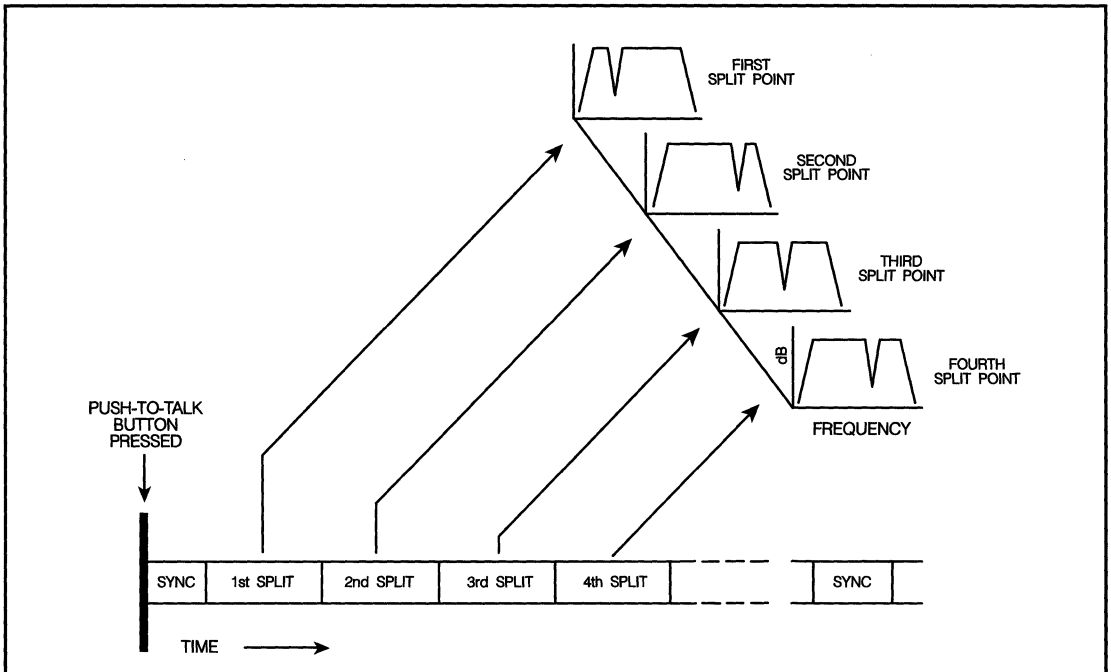

Figure 2 - The effect of rolling code split points on the transmitted radio spectrum

ers transmit the resulting variable split-band-scrambled output via an ordinary radio communications channel.

Microprocessor outputs control the split point (the frequency at which the voice band is subdivided) and change it from 4 to 60 times per second. Figure 2 reveals the "rolling code" nature of VSB scrambling. One of more than 65,000 unique user-programmable code keys initializes the pseudorandom sequence of split points. User programming commands the split point's rate of change, or "hop rate," to vary pseudorandomly or in a fixed fashion.

Filtering Accuracy

Optimum recovered audio quality depends upon highly accurate voice filtering. Two pairs of 7th order, switched-capacitor, elliptic filters in the VSB filter array integrated circuit (IC, on-chip) accomplish all the filtering (See Figure 3).

The transceiver's mic. audio pre-amplifier or receiver audio demodulator output feeds the VSB filter array IC's highband and lowband inputs. Within the IC, audio from each subband passes through a lowpass filter, a frequency inverter and another lowpass filter. A summing amplifier recombines the subbands. The chip includes a highpass filter that permits VSB scrambling to be used with continuous-tone controlled squelch systems (CTCSS) and other sub-audible signaling schemes.

On-chip programmable dividers with a 5-bit logic address control the 32 split points and their highband and lowband carrier frequencies. The VSB microprocessor uses the 5-bit address to generate a rapidly changing sequence of split points. Table 1 shows the exact relationship between each split point and its associated carrier frequencies.

Microprocessor Control

The VSB microprocessor performs scramble system control functions, including:

- generation of split-point sequences
- control of system synchronization
- monitoring of the push-to-talk (PTT) line
- code key selection
- code key loading
- selection of the secure or clear mode.

The microprocessor generates pseudorandom strings of split points initialized by one of four user-programmable code keys. Non-volatile, electrically erasable, programmable read-only memory (EEPROM) stores the code keys and other user-programmable system information (see Figure 4).

To decode a rolling, VSB-scrambled message properly, the receiver(s) must "hop" in unison with the transmitter from one split point to the next. A continuous synchronization scheme accomplishes this task. The scheme transmits 1200-baud minimum-shift keyed (MSK) data bursts every three seconds. Authorized parties can descramble transmissions even if the beginning of the message is missed, preserving mobile radio's inherent "late joining" feature.

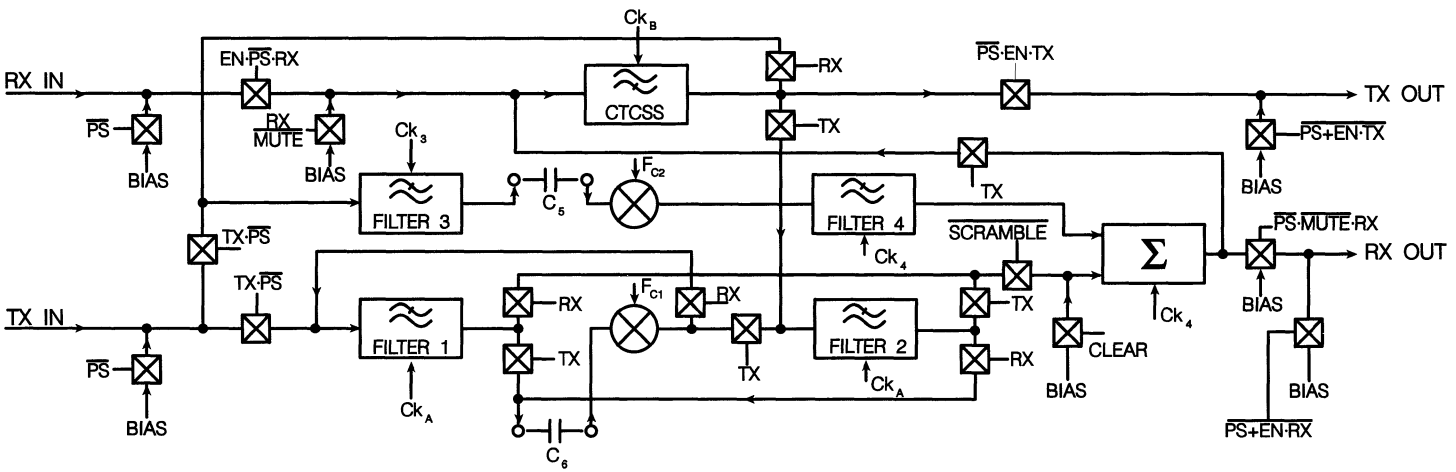

Figure 3 - Functional block diagram of the VSB filter array

ROM Address A_4-A_0	Split Point Hz	Low Band Carrier, Hz f_{c1}	High Band Carrier, Hz f_{c2}	ROM Address A_4-A_0	Split Point Hz	Low Band Carrier, Hz f_{c1}	High Band Carrier, Hz f_{c2}
00000	2800	3105	6172	10000	1135	1436	4504
00001	2625	2923	6024	10001	1050	1351	4424
00010	2470	2777	5813	10010	976	1278	4347
00011	2333	2631	5681	10011	913	1213	4310
00100	2210	2512	5555	10100	857	1157	4273
00101	2100	2403	5494	10101	792	1094	4166
00110	2000	2304	5376	10110	736	1037	4132
00111	1909	2212	5263	10111	688	988	4065
01000	1826	2127	5208	11000	636	936	4032
01001	1750	2049	5102	11001	591	891	3968
01010	1680	1984	5050	11010	552	853	3937
01011	1555	1858	4950	11011	512	813	3906
01100	1448	1748	4807	11100	471	772	3846
01101	1354	1655	4716	11101	428	728	3816
01110	1272	1572	4629	11110	388	688	3787
01111	1200	1501	4587	11111	350	650	3731

Table 1 - ROM Address Programming

In the absence of valid synchronization bursts, receivers revert to clear mode. The automatic reversion to clear mode ("clear voice override") makes scrambling easier to use in systems that include some radios not equipped for scrambling.

Only transmitting VSB units generate synchronizing data bursts, so the system resynchronizes at the transmitting station's command. Transceivers automatically transmit 80ms data bursts every three seconds after beginning a transmission. Each data burst includes:

Unit System Address -- Identifies the scrambler as part of a designated group.

Code Key File Number -- Identifies which of the four stored code keys to use.

Time Of Day -- When mixed with the secret code key, which never is transmitted, time of day tells the receiver on which part of the 50-hour long split-point sequence to begin "hopping."

Synchronization Cue -- Tells the receiver when to change split points.

In the standby mode, VSB scrambling units scan continuously for incoming synchronization bursts that have the proper system address and file number. After receiving one such data burst, a VSB unit uses the time-of-day signal and synchronization cue to descramble the incoming message properly. Unless the receiving unit receives the proper address and file combination, it processes incoming transmissions as though they were unscrambled.

A robust error-detection algorithm, based on the British MPT 1317 signaling protocol, minimizes synchronization errors. As a safeguard, VSB scramblers retain synchronization even if a single synchronization burst is missed. If the scrambler misses two synchronization bursts in a row,

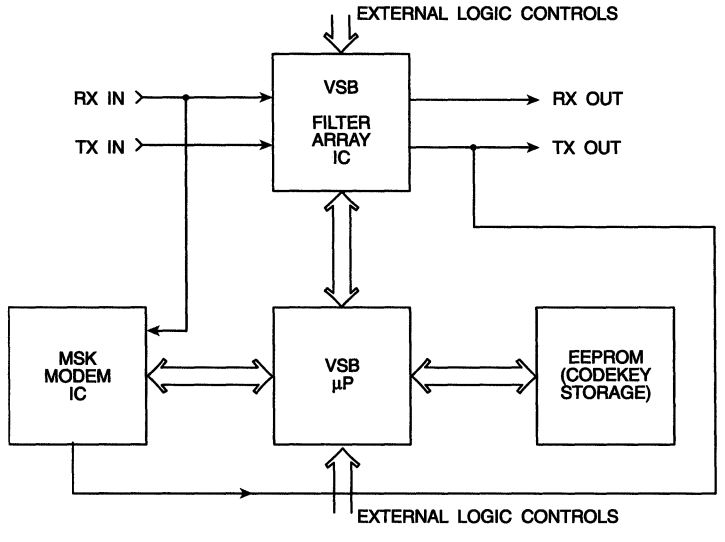

Figure 4 - Block diagram of VSB scrambler mode

Voice Security Market

Potential markets for economical voice security products include:

- Taxi
- Towtruck
- Marine and other dispatch operations whose managers previously have been unsatisfied with the price or performance of voice security products.
- Municipal law enforcement agencies that lack voice security systems or that are committed to a digital encryption system that is too expensive to install into every radio in the organization.

the system reverts to the standby mode and scans once again for synchronization burst data.

Minimum-shift keyed modulation offers excellent narrowband transmission properties and superior noise performance. With MSK modulation, voice intelligibility and synchronization are lost more or less concurrently in fringe reception areas and without an appreciable loss in radio range.

An eavesdropper monitoring a VSB-scrambled transmission hears an unintelligible jumble, interrupted by bursts of digital "static" every three seconds. Consider VSB scrambling's security features:

(1) The split-point sequence permutation, which is based on a mixture of the secret code key and the time-of-day signal, changes automatically every three seconds. The code knowledge that may be obtained from one descrambled three-second sequence cannot be applied to descramble subsequent segments because they are based on different sets of pseudorandom permutations.

(2) The split-point "hop rate" may be varied pseudorandomly, further complicating the task.

(3) Each VSB-equipped radio can transmit and receive four programmed code keys, and VSB systems can accomodate as many as 16 unique code keys. Thus, a unit can transmit on one code key and receive on another.

(4) The code keys may be changed at any time. They never are transmitted. They cannot be deduced by visual or mechanical means.

Given these security features, how difficult is it to

VSB Scrambling Multiple Codekey Capability

Within a VSB scrambling network, up to 16 codekeys can be allocated. Four of the sixteen codekeys can be installed per radio. As illustrated below, this capability can create interesting subgroup segregation possibilities:

Scenario: Public safety departments of medium-sized cities need interagency, as well as private, intradepartmental secure communications.

Solution: A VSB Scrambling codekey allocation scheme allocates seven codekeys (A-G), four to the police force, and two each to the fire department, ambulance service, and detective unit.

USER SUBGROUP	INSTALLED CODEKEYS	COMMUNICATIONS CAPABILITY
1) HQ/Supv.	All	Monitor all channels
2) Police	A	Intradepartment only
	B	Police and fire
	C	Police and detectives
	D	Police and ambulance
3) Fire	B	Police and fire
	E	Intradepartment only
4) Detectives	C	Police and detectives
	F	Detectives only
5) Ambulance	D	Police and ambulance
	G	Intrasquad, ambulance and hospital

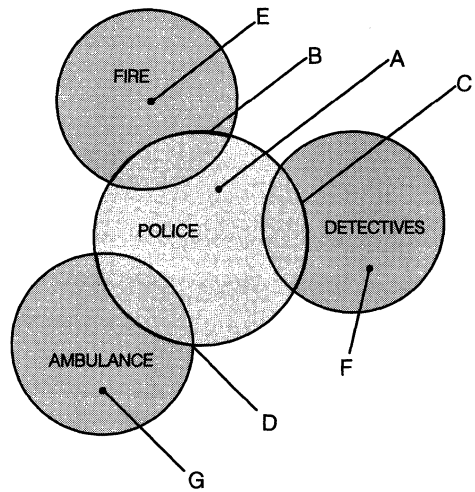

Figure 5 - Multiple codekeys extend subgroup segregation possibilities in a medium-sized city's public safety department

descramble such a garbled transmission? According to two experts, it is not easy.

According to Michael Washvill, a voice and data security specialist with a federal agency, "VSB scrambling can be broken, but not in real time. The only practical attack is through trial and error. The scrambled speech must first be recorded, then divided into finite time segments according to the hop rate. Each segment is processed through a variety of split point combinations until clear speech results."

A TRW systems engineer and former U.S. Department of Defense employee, Jim Walker, concurs: "The 'brute force' method of trial and error is the only way to break VSB-scrambled speech. Assuming that the 'bad guys' have a stolen VSB unit and no prior knowledge of the code key or code keys, 50 to 100 minutes of dedicated effort are required to descramble one minute of VSB-scrambled speech. A rule of thumb is 60:1 'grunt time to clear speech time'."

Walker continued, "For most eavesdroppers, the potential rewards do not justify the time and effort. Two additional factors come into play. First, by the time the information is decrypted, will it still be of any use? Second, what percentage of the descrambled radio traffic will be of value?"

Given the time and perseverance required to break a VSB-scrambled transmission, two alternatives become much more attractive to those who want to eavesdrop: Steal a VSB-equipped radio or bribe someone who knows the codekey. Strict code key management procedures reduce system vulnerability to these attack methods.

To reduce the possibility of bribery, restrict code key knowledge to one person. To guard against stolen VSB units, change system code keys on a regular basis by using the VSB keyloader.

The keyloader is a portable tool that reprograms VSB-equipped radios in the field. A technician connects the keyloader's data-loading cable to a VSB-equipped radio and presses the load button to install as many as four new codekeys into each radio. Only the person with codekey management authority can program the keyloader or read its contents.

Tactical vs. Strategic

Voice security requirements can be divided into two broad categories: tactical and strategic. Tactical applications are those in which the secrecy of the message is time-dependent, such as battlefield tactical communications, most municipal police communications and nearly all dispatch communications. The tactical message retains its value for one or two hours at most. VSB scrambling serves tactical security requirements.

James Bramford, in his book *The Puzzle Palace*, defines strategic communications as "the high-level diplomatic, commercial and military communications that might give away a nation's foreign policy venture, where and with whom it was doing business, or what new weapons were being developed over the next few years." Today's strategic applications demand some form of digital encryption.

In addition to the message security afforded by digital encryption or VSB scrambling, transmission security can be assured through spread-spectrum techniques, such as frequency hopping, which render the radio signal both undetectable and immune to jamming.

Most mobile radio users have tactical voice security requirements. For these applications, VSB scrambling offers a practical, economical alternative to digital encryption systems. VSB scrambling requires no modification of the installed communications network. It has little or no impact on radio range.

As dealers and users become more comfortable with VSB and other new scrambling technologies, foiled drug busts, unsolved burglaries and pirated business opportunities resulting from unauthorized eavesdropping will become things of the past.

MX•COM, INC.

SWITCHED CAPACITOR INTERFACING

Anti-Aliasing and Smoothing Filters

By Jim Kemerling
MX-COM, INC.

1.0 Introduction

Switched capacitor networks (SCNs) are sampled data systems and therefore are governed by the principles of discrete time signal processing. In this context, "discrete time" means the signal is sampled prior to processing. However, the amplitude is continuous – unlike digital signal processing (DSP) systems where both amplitude and time are discrete.

VLSI technology (generally CMOS) has facilitated complete integration of SCNs on a single monolithic chip. Filters utilizing switched capacitor techniques (SCFs) are composed of switches, capacitors and opamps. Notice resistors are not mentioned. The resistors normally present in active filters are approximated by switched capacitors. By taking advantage of matching properties of CMOS capacitors, SCFs can be fabricated with low tolerance levels (less than 0.1%) and virtually any order.

The wireless and wireline telecom industries have made extensive use of SCFs. Even with the move towards digital technology and the ensuing popularity of DSP in the communications industry, SCNs are frequently employed where cost and power consumption are critical. SCNs generally have relatively high sampling rates (typically greater than 20 times the bandwidth of the interest) due to their discrete time nature, so aliasing and output smoothing must be addressed. Often a simple single pole filter (R-C network) suffices, but the location of these poles must be carefully thought out in the design process. The world is still analog.

The purpose of this paper is to address the need for anti-aliasing and smoothing filters for SCFs. First, the basics of sampling will be reviewed. The fundamentals of SCNs will follow this, and finally the design of antialiasing and smoothing filters for SCFs is addressed.

2.0 Sampling [3]

Before a continuous signal is processed by a discrete time filter it must first be sampled. Referring to Figure 1a, sampling is the process of instantaneously capturing the level of a continuous signal at some predetermined rate. This predetermined rate is the sampling frequency. As the sampling rate increases (Figure 1b) the sampled signal begins to approximate the original continuous signal.

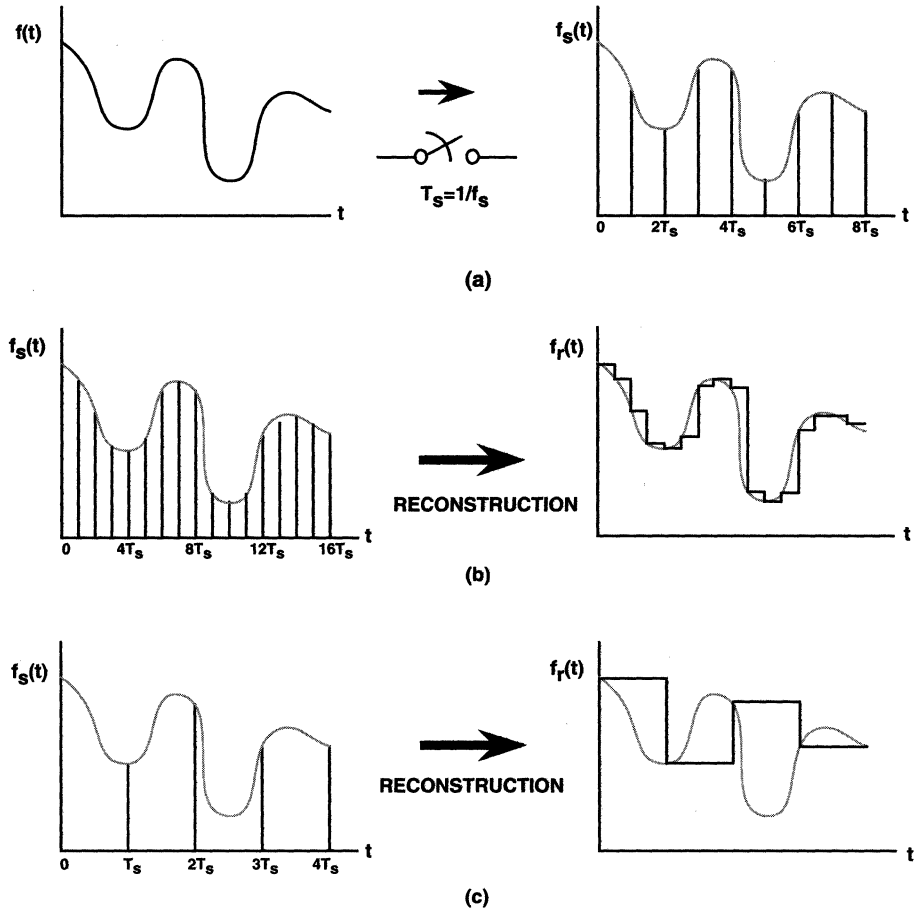

Figure 1 - Waveform sampling: (a) sampling process, (b) reconstruction with acceptable sampling rate, (c) reconstruction with unacceptable sampling rate.

On the other hand, as the sampling frequency decreases (Figure 1c) the samples move further apart in time, yielding a reconstructed signal that does not resemble the original. The limit on how far apart these samples can become without losing information is the basis for Shannon's sampling theorem.

Shannon's original work on sampling and information theory [3] stated the sampling theorem as:

> "If a function f(t) contains no frequencies higher than *f* cycles per second it is completely determined by giving its ordinates at a series of points spaced (1/2*f*) seconds apart."

A formal derivation is obtained by convolving the Fourier transform of the continuous signal with the Fourier transform of an infinite sequence of impulse functions.

$$Fs(\omega) = \frac{1}{2\pi} (F(\omega)*S(\omega)) \quad (1)$$

$$Fs(\omega) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(x)S(\omega-x)dx \quad (2)$$

Where, $F_S(\omega)$ = sampled signal spectrum
$F(\omega)$ = original signal spectrum
$S(\omega)$ = spectrum for a sequence of impulses
ω = radian frequency ($2\pi f$).

The result of the convolution is the original signal spectrum repeated at multiples of the sampling frequency as shown in Figure 2. Notice that if the sampling frequency is less than twice the bandwidth of the original signal then the replica centered at the sampling frequency will overlap and distort the original. This undesirable phenomenon is aliasing. Aliasing will be avoided if,

$$f_S \geq 2B \quad (3)$$

Where, f_S= sampling frequency , Hz
B = bandwidth of original signal, Hz.

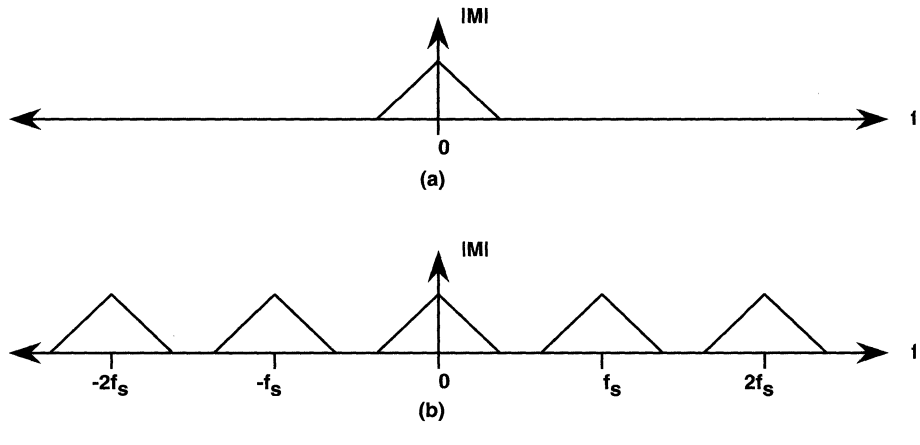

Figure 2 - Frequency Spectrum of (a) continuous time signal; (b) sampled signal

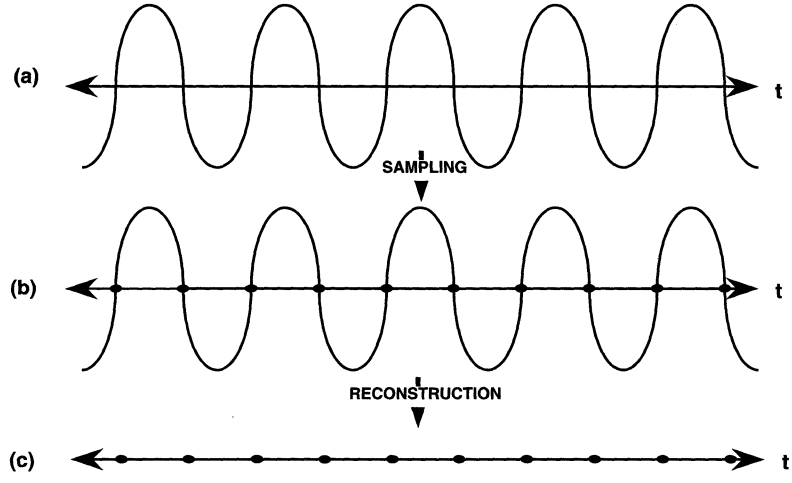

Figure 3 - Time domain representation of sampling at $f_s = 2B$; (a) continuous signal; (b) sampled signal; (c) reconstructed signal

Shannon's sampling theorem is mathematically sound although, in most cases, it is not practical to sample a signal at exactly twice its highest frequency component. Figure 3 shows a sinewave sampled at **2B** samples per second, where **B = 1/T** and **T** is the period of the sinewave. Notice the difference between the reconstructed wave shapes and the original unsampled signal. This type of error is not the result of aliasing, yet it could cause deceptive results. A mathematician might claim that there is no information in a continuous sinewave that never changes amplitude or frequency. This is a fact. However, if a signal is sampled at exactly **2B**, some of the original signal may be lost or distorted.

If the system designer is not concerned with the possibility of losing some of the original signal, and wanted to sample at **2B**, he or she would still be facing the problem of bandlimiting. Bandlimiting is necessary to avoid aliasing. Figure 4 shows the spectrum of a sampled signal. Notice that for f_S**=2B** the bandlimiting filter must have infinite attenuation at the frequency **B**. A filter that matches this requirement is physically unrealizable.

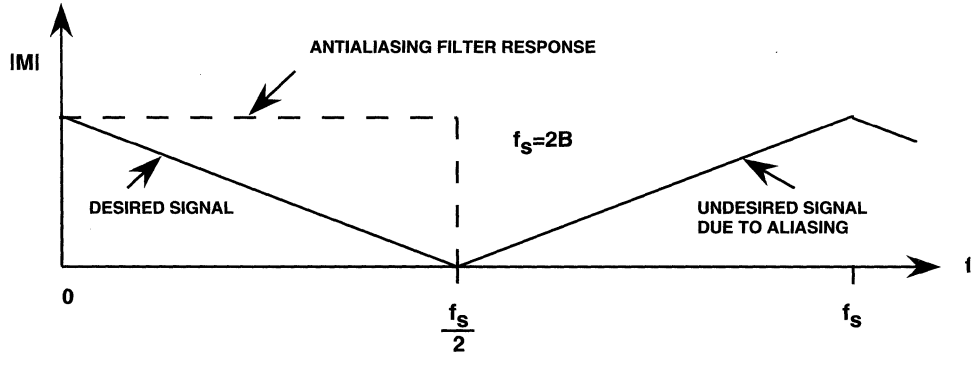

Figure 4 - Antialiasing filter required for sampling at exactly 2B

3.0 SCN Concepts [1]

A single pole active filter (inverting integrator) is shown in Figure 5. This circuit is the primary building block for most active filters.

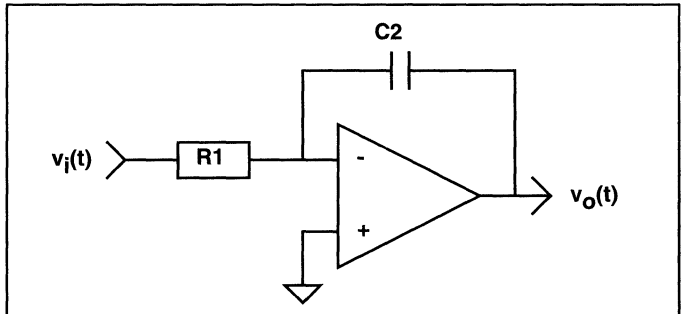

Figure 5 - Active R-C integrator.

The output is defined by

$$vo\ (t) = -\frac{1}{RC}\int_0^t v_i\ (\tau)\ d\tau \qquad (4)$$

Hence, the output is an integrated version of the input, scaled by **-1/RC**. The pole frequency is determined by the value of **R** and **C**

$$f_p = \frac{1}{2\pi RC} \qquad (5)$$

For a pole frequency of 3000Hz, (5) implies RC=53.05μs. A possible implementation, selecting C=10pf (relatively large capacitor for CMOS technology), requires R=5.305MΩ. A monolithic resistor of this value would consume excessive amounts of silicon and is subject to significant variation with process and temperature. Integrated capacitors are also subject to variation with process and temperature. In addition, capacitor variations are independent of resistor variations.

A more practical realization is shown in Figure 6.

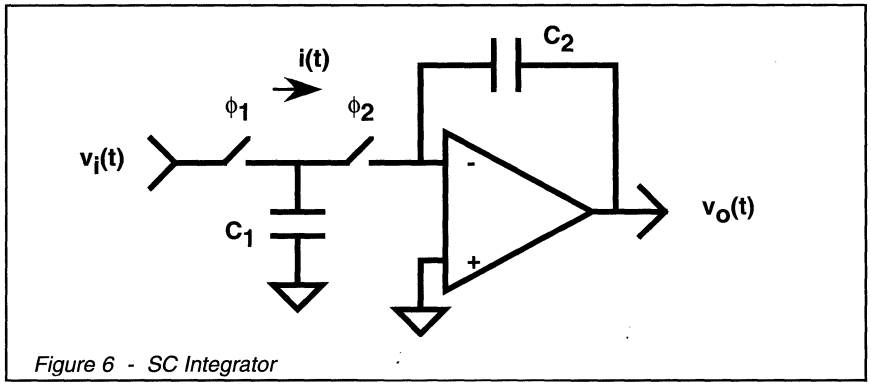

Figure 6 - SC Integrator

Notice **R** is replaced by a capacitor and two switches. The function of the resistor is now approximated by transferring charge from vi(t) to the inverting input of the opamp at intervals determined by clocks $\phi 1$ and $\phi 2$. To ensure complete charge transfer $\phi 1$ and $\phi 2$ must not overlap as shown in Figure 7.

An approximate analysis of Figure 6 reveals the average current through the switches is

$$i = \frac{\Delta q}{T} = \frac{C_1}{T}(v_i - v_1) \quad (6)$$

or

$$i = \frac{1}{R}(v_i - v_1) \quad (7)$$

Where, $R = T/C_1$

Looking back at the previous example for a pole frequency of 3000Hz, using $T = 10\mu s$ (f_{clk}=100kHz), yields C_1=1.885 pf. Hence, the integrator can be realized with two capacitors that will track with process and temperature. No longer is the absolute value of the capacitors important, only their ratio.

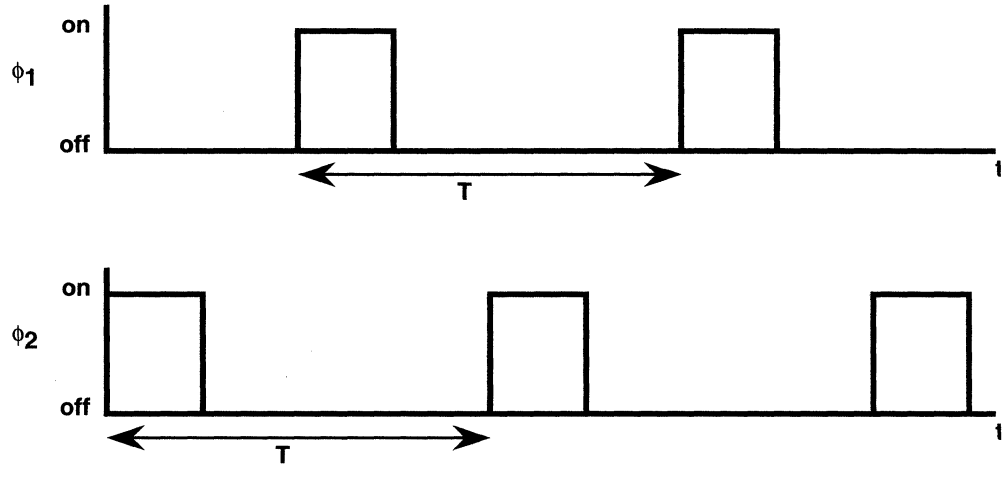

Figure 7 - Non-overlapping clocks for SC integrator

4.0 Anti-aliasing and Smoothing Filters for SCNs [2]

SCFs approximate active-RC filters by replacing resistors with switched capacitors. As the clock frequency (sampling rate) tends towards infinity the SCF becomes equivalent to the continuous time filter. In other words, higher clock frequency yields a better approximation of the desired response. Also, higher clock frequency lessens the requirements of the anti-aliasing filter (AAF) and smoothing filter (SMF). However, there are upper limits on clock frequency. Although SCFs have been implemented with clock frequencies greater than 1MHz, typical telecom filters (BW less than 10kHz) are clocked at or below 250kHz.

One factor which opposes higher clock frequencies is large capacitor ratios. Referring to the example in section

3.0, using 1MHz in place of 100kHz, C_1 becomes 0.1885 pf. The ratio between C_1 and C_2 is now 53.05 where it was 5.305. Large capacitor ratios consume more silicon area and are more sensitive to process and temperature variations. Hence, the final sampling rate is a compromise between SCF implementation complexity and SMF/AAF requirements.

SMFs and AAFs can be integrated, but they are subject to the same problems associated with the continuous time RC integrator discussed in section 3.0 and are generally implemented externally. In some cases, where input and output signals are band limited externally, additional circuitry for AAFs and SMFs is not required. A block diagram of a typical SCF system, including AAF and SMF is shown in Figure 8.

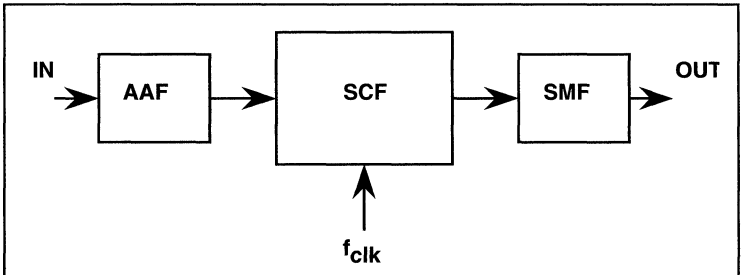

Figure 8 - SCF system with AAF and SMF

To determine AAF and SMF requirements the system designer must know the sampling frequency (f_{clk}) and the bandwidth (BW) or cutoff frequency (f_{co}) of the SCF. For discussion purposes, assume f_{clk}=100kHz and f_{co}=5kHz. Recall from section 2.0, if any signal energy is present at the input, with frequency f_S greater than $1/2f_{clk}$, it will be aliased to $f_{clk} - f_S$. Hence, an input with f_S=99kHz will be aliased to 1kHz. This aliased signal will appear as noise in the passband of the SCF. To eliminate or reduce the effect of this noise the AAF must band limit the input signal to $f_{clk} - f_{co}$ (see Figure 9).

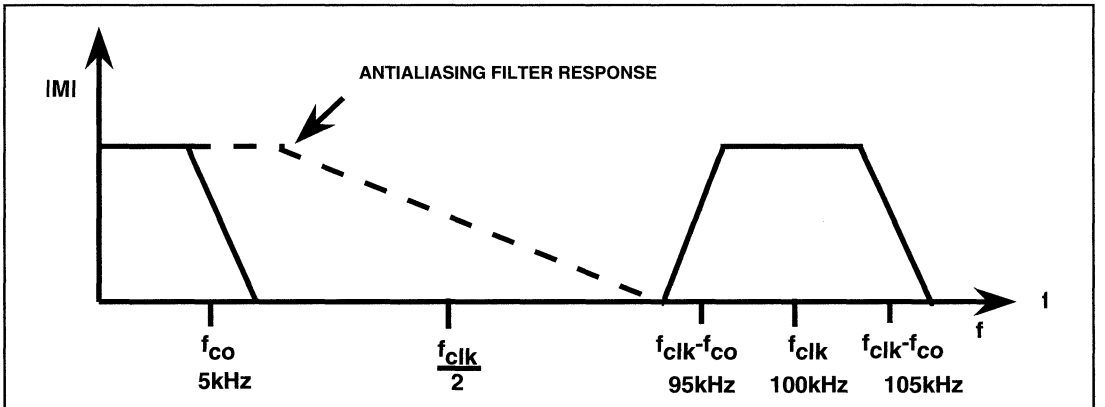

Figure 9 - AAF requirements for SCF system

To obtain 20 dB suppression of aliased noise the minimum requirement for the AAF is a first order section (single pole) with it's cutoff frequency set to 9.5kHz. (20 dB/decade/pole). Placing the pole at 9.5kHz minimizes the effect on the SCF passband response. To obtain further suppression more poles are necessary.

The single pole AAF can be implemented with a simple RC at the input to the SCF. The values for can be arrived at by using

$$RC = \frac{1}{2\pi f_p} \quad (8)$$

where, f_p = pole frequency.

For the AAF response depicted in Figure 9, **RC** = 16.75ms. Setting **C** = 0.1μf yields **R** = 168Ω. The simple RC network should be used with caution–capacitive loading can cause stability problems. Also, the value of the resistor should be insignificant compared to the SCF input impedance.

A superior solution makes use of an additional opamp forming a damped integrator (see Figure 10). Often this opamp will be available on the SCF chip.

The complete network, including R1, C1, R2 and C2, forms a bandpass filter with a frequency response characteristic as shown in Figure 11.

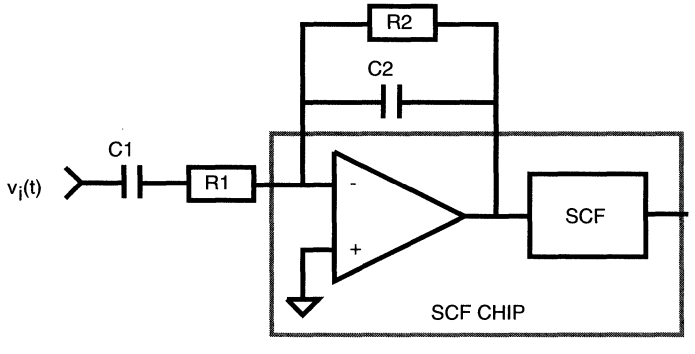

Figure 10 - Active RC AAF

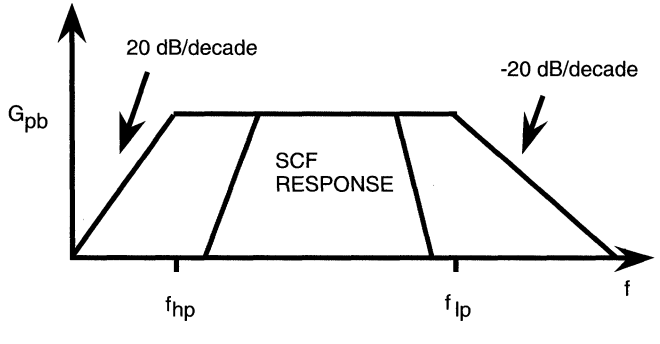

Figure 11 - AAF frequency response

The highpass cutoff (f_{hp}) and lowpass cutoff (f_{lp}) are determined by

$$f_{hp} = \frac{1}{2\pi R_1 C_1} \quad (9)$$

and

$$f_{lp} = \frac{1}{2\pi R_2 C_2} \quad (10)$$

The passband gain is set by

$$G_{pb} = R_2/R_1 \quad (11)$$

C_1 is not required if the input signal is biased properly (SCF internal bias = external bias).

To meet the AAF requirements shown in figure 9 (assuming unity passband gain, f_{lp} = 9.5kHz and f_{hp} = 100 Hz) $R_1 = R_2$ = 100KΩ, C_2 = 168pf and C_1 = 0.0159μf.

SMF requirements are similar to those of the AAF. The SCF output is a sampled signal and therefore contains replicas of the SCF response at multiples of the sampling frequency. If left unfiltered these replicas appear as high frequency (clock) noise. In some cases this is tolerable. However, in systems where minimum noise is critical the SMF is required.

5.0 Conclusion

Switched capacitor filters are sampled data systems and hence require anti-aliasing filters at their inputs and smoothing filters at their outputs. The simplest form (and often sufficient) of these filters is the single pole RC network. Other forms such as active RC networks and higher order filters can yield distinct benefits. In any case, application of switched capacitor filters must be viewed at the system level in order to realize optimum performance.

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[2] L. P. Huelsman and P. E. Allen, Introduction to the Theory and Design of Active Filters, McGraw-Hill, New York, 1980.

[3] A. B. Jerri, "The Shannon Sampling Theorem - Its Various Extensions and Applications: A Tutorial Review," Proceedings of the IEEE, pp. 1565-1596, November 1977.

An Audio Delay Circuit Based on the MX609 CVSD Codec

The schematic diagram shown on the following page is an audio delay circuit based on the MX609 CVSD Codec. In addition to the MX609, the circuit uses a Fujitsu MB81C71 64K x 1 bit RAM, two 4520 counter ICs, and a 4069 inverter chip. It provides up to two seconds of delay. This circuit provides a starting point for a designer who wishes to implement an audio delay circuit. MX-COM makes no guarantee of its performance and assumes no responsibility for its use in any product.

Circuit Operation

In the following operational description, a bar over a signal name is used to indicate an active low signal. For example, $\overline{W}$ is an active low write enable signal. On the MX609P, Clock Mode 1, pin 22, is tied to V_{DD} and Clock Mode 2, pin 21, is tied to ground to set the encode and decoder clocks for a sampling rate of 32 kb/s. The Encoder Force Idle, Powersave, and Decoder Force Idle inputs, pins 6, 15, and 16, respectively, are tied to V_{DD} to set them inactive. The Data Enable input, pin 7, is tied to V_{DD} to make the encoded data available at the Encoder Output, pin 5. Pin 19, the Algorithm select input, is tied to ground to select a four-bit companding algorithm. The other inputs are the same as recommended for "External Component Connections" shown in the MX-COM data book.

The audio signal to be delayed is input to pin 10 of the MX609, the Encoder Input, and is converted to a serial stream of digital data. The serial data are output on pin 5, the Encoder Output, and connected to pin 13, the D input, of the MB81C71 memory chip. The Decoder Data Clock output from pin 18 of the MX609 is connected to pin 1 of the 4069 inverter. The output of the inverter, pin 2, is connected to pin 10 of the MB81C71, the $\overline{W}$ input, and to pin 3 of the 4069, the input to second inverter. Pin 4, the inverter output, is connected to the enable input of the first 4520 counter.

The enable input is taken from the second inverter to ensure that the 4520 counters increment after the $\overline{W}$ signal into the 81C71 transitions from low to high. The clock inputs of each of the 4520s, pins 1 and 9, are tied to ground so that only the enable inputs control when the counters increment. The reset inputs, pins 7 and 15, are also tied to ground so that they never reset the counters. The individual four bit counters in the 4520s are cascaded to produce a 16 bit counter. The counter outputs, Q15 - Q0, are connected to the address inputs, A15 - A0, of the MB81C71.

There are switches between Q15 and A15 and between Q14 and A14. The switches allow the number of bits of the counter, and therefore the length of the delay, to be adjusted. When the Decoder Data Clock falls from high to low, the counter, and therefore the address, increments. Since the $\overline{W}$ input to the memory, pin 17, is the complement of the clock, it rises from low to high, latching the encoded data bit at the D input. The $\overline{E}$ input to the MB81C71, pin 12, is tied to ground so that the memory is always selected. When $\overline{W}$ is high and the address is stable, a valid data bit appears at the Q output, pin 17, of the MB81C71. The address of the data bit appearing at Q is one greater than the address of the bit that was just written, so the counter must cycle through its entire range before a data bit that has been written into the memory can be read. Therefore, a data bit output from the MX609 at the Encoder Output pin is delayed by the number of clock periods of the range of the counter. The delay is given by

$$\text{Delay} = (\text{T sec/cycle}) * (2^{N} \text{ cycles})$$

where

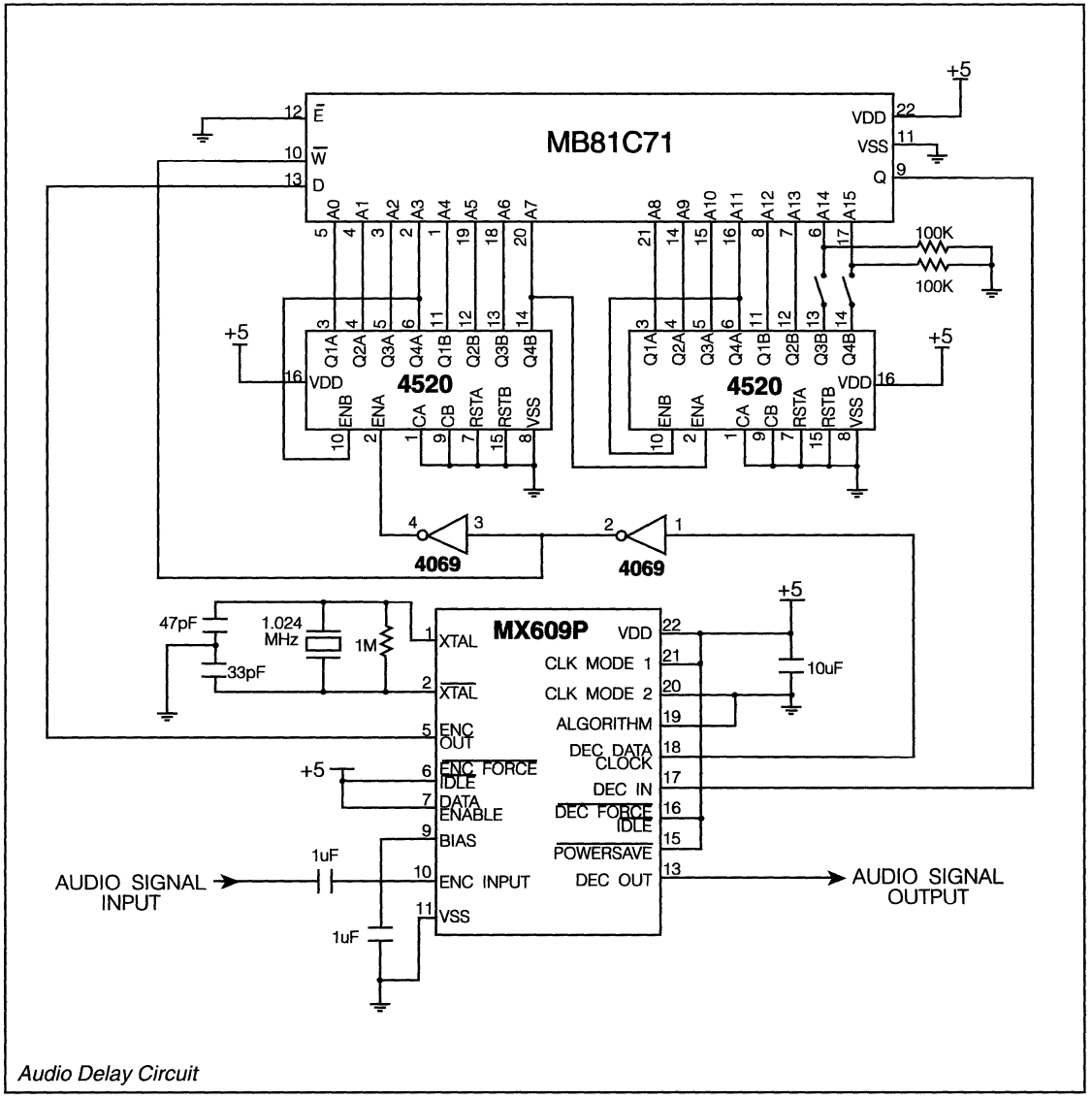
T = period of Decoder Data Clock

N = number of bits used in counter

If all 16 bits of the counter are used, and the decoder clock frequency is 32 kHz, then the delay would be

$$\text{Delay} = (1/32000) \text{ sec/cycle} * (216) \text{ cycles}$$
$$= 2.048 \text{ seconds}$$

In this example, all locations of the memory are used. If a shorter delay is desired, the switches connecting the counter outputs and address inputs can be opened. If only 14 bits of the counter are used, then the delay is reduced by a factor of four, to 0.512 seconds. The range of delays could be increased even more by adding more switches and by making the sampling clock frequency adjustable. The Q output, pin 9, of the MB81C71 is connected to the Decoder Input, pin 17, of the MX609. The decoder clocks in the serial digital data stream from the memory and converts it to an analog signal which is output at pin 13, the Decoder Output. The Decoder Output is the delayed audio signal.



Audio Delay Circuit

MX•COM Standard and DBS800 Crystal Oscillator Circuits

The DBS800 IC family can use an external clock (output from a microprocessor, for example) or can generate its own clock with an on-chip oscillator. This application note discusses both a generic oscillator circuit used for most MX•COM ICs and the oscillator circuit to be used with the DBS800 ICs.

The standard MX•COM on-chip oscillator circuit functions correctly with the majority of crystals, but the use of this circuit with a few crystal types may cause the following events:

1. Excessive drive level to the crystal.

2. Excessive over-voltage -- outside the maximum ratings -- at the oscillator input pin. This over-voltage may show itself as degraded device performance.

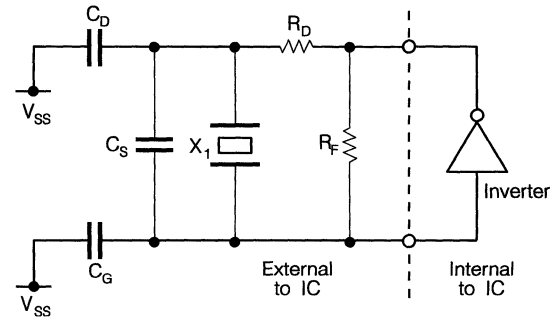


Figure 1 - Standard Crystal Oscillator Circuit

The oscillator circuit pictured in Figure 1 may be used when the above conditions apply or when specified by the crystal manufacturer.

Component	Notes
X_1	**Crystal** Typically 4MHz or 4.032MHz (Parallel resonant).
R_1	**Feedback Resistor** Sets the bias point for the amplifier. Low values of R_1 will reduce loop gain and disturb the phase of the feedback network. Typical Value is 1MΩ ±10% (Range 1 - 20 MΩ).
R_D	**Drive Resistor** Resistor R_D is used to limit the crystal drive level by forming a voltage divider between R_D and C_D. R_D also stabilizes the oscillator against changes in the output impedance of the inverter. To verify that the maximum operating supply voltage does not overdrive the crystal, observe the output frequency as a function of voltage at the buffered output. Under proper operating conditions the frequency should increase slightly (a few ppm) as the supply voltage increases. If the crystal is being overdriven, an increase in supply will normally cause a decrease in frequency or instability. If the latter is the case (i.e. crystal being overdriven), increase the value of R_D (refer to crystal manufacturer's recommendations).
C_D	**Drain Capacitor** Capacitor C_D provides phase shift and reduces crystal drive. Large values of C_D tend to stabilize the oscillator against variations in power supply voltage. Large values also reduce the tuning capability of the oscillator and overtone activity. Typical value is 33 pF ±20% (crystal manufacturer may recommend 5 - 40 pF).
C_G	**Gate Capacitor** This capacitor provides phase shift and input voltage for the amplifier. In some oscillator circuits C_G is used to adjust the oscillator to frequency, although this generally may not be required. Large values reduce loop gain and increase stability. This capacitor may be used to reduce over-voltage at the inverter input. However, the reduction in loop gain may cause oscillator start-up problems. The value of C_G will typically be in the range 5 - 65 pF ±20% (refer to crystal manufacturer's recommendations).

C_S **Stray Capacitance**

Due to the low motional capacitance of small crystals and the high inverter input impedance the designer should be concerned with circuit board layout. For best oscillator performance C_S should be less than 1 pF.

DBS800 Crystal Oscillator Circuit

The oscillator circuit for the MX806A is similar to the standard circuit described above, but there are some important differences. Figure 2 shows the MX806A oscillator circuit. Note that the feedback resistor, R_1, is internal to the IC and that drive resistor R_D has been omitted. External capacitors C_1 and C_2 must be provided in addition to crystal X_1. The values of C_1 and C_2 are typically 33 pF.

In a system that does not include the MX809 1200 bps Modem, a 4 MHz crystal is specified. But if the system design includes the MX809, or will be upgraded in the future to include it, a 4.032 MHz crystal must be used for proper operation of the MX809. The other chips will also function properly with this clock frequency.

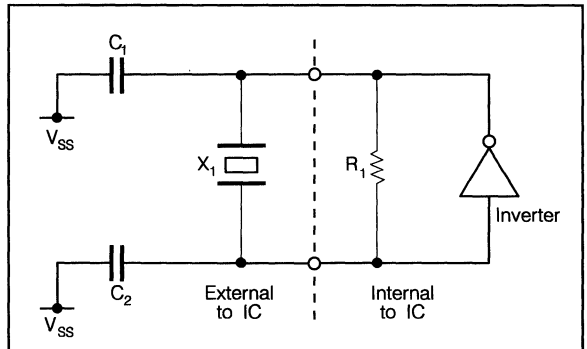


Figure 2 - Oscillator Circuit for the MX806A

For systems that include more than one DBS800 IC, the clock for the MX806A may be generated with a single crystal using the on-chip oscillator of the MX806A. The output clock signal from the MX806A is then cascaded from chip to chip within the system. This configuration is shown in Figure 3.

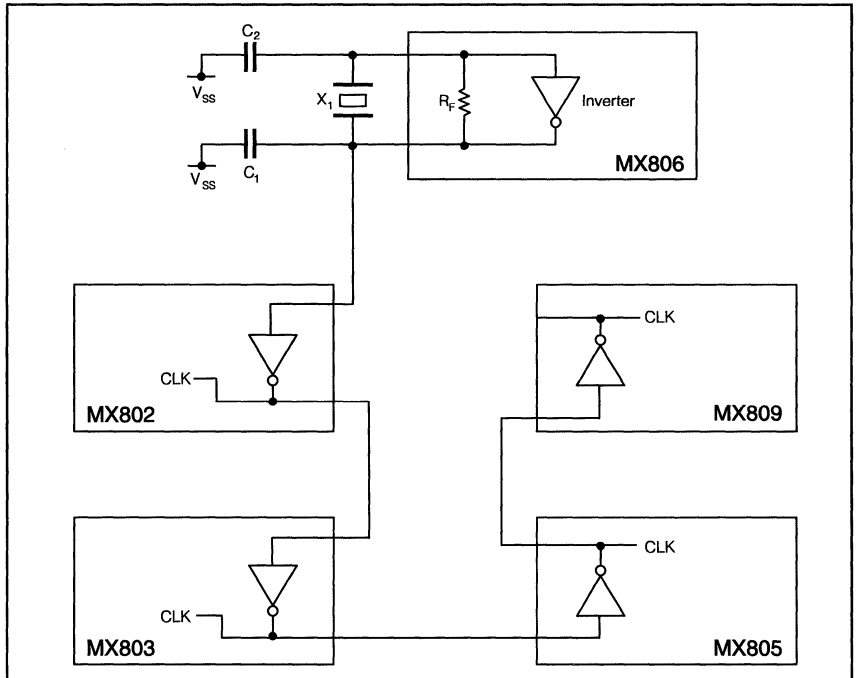


Figure 3 - Cascaded Clocks for the DBS800 System

Wireless Data Modems: Getting the Best Performance

By Bud Simciak and Sam Rizk

MX•COM'S Wireless Data Modem ICs

MX•COM's complete product line of wireless data modem ICs offers OEMs full product migration from speeds of 1200 bps to 40 kbps.

Our first modem (the MX409) appeared in 1984. Today the MX439 serves a similar bit-serial Minimum Shift Key (MSK, or Fast Frequency Shift Key (FFSK)) 1200 bps application. Uses of MSK modems are numerous, from the recovery of stolen vehicles to the elimination of red cabooses. Yes, cabooses. Traditionally the person in the caboose signaled the conductor regarding information critical to the safe operation of a train — like airbrake pressure and current to a taillamp. Now this data can be handled by MSK-1200 radio telemetry signals instead -- an entire train car is replaced by a modem. Greater reliability *and* less cost are achieved through radio modems.

Byte-wide, protocol-specific units serve trunked mobile systems in the UK (MX429 w/MPT-1327) and France (MX529 w/PAA-1382). These are excellent, field proven protocols useful for just about any radio system data application, trunked or not. Selective Calling Protocol is supported by MSK-1200 and exists as an ETSI draft (EBSS 1200) in Europe. In the USA, 1200 bps MSK is marketed by Motorola as the MDC-1200 system, using a unique 1200/1800Hz preamble as a "data squelch."

The MX809 combines many of the best features of the serial and byte-wide devices. Receive and transmit data is exchanged in byte length serial bursts allowing both free format and protocol-specific operation. Interface to a microcontroller is provided using the C-BUS (MX•COM's DBS800 System BUS) and addressable registers.

All MX•COM 1200 bps modems use 1200/1800 (mark/space) frequencies: one cycle of 1200Hz constitutes a bit "1," one-and-a-half cycles of 1800Hz a bit "0." Each bit period is a constant 1/1200 of a second. One-zero bit transitions occur at the sinewave's zero crossing, as a phase coherent frequency shift — from which the Minimum Shift Keying name is taken. The occupied bit-rate bandwidth is 900 to 2100Hz.

Our newest product releases are a High-Speed and MOBITEX GMSK Modem (MX909), two high-speed 4-Level FSK modems, one for general purpose (MX919) and one for ARDIS systems (MX929), and a CDPD/AMPS-Wide Band Data fulll-duplex modem (MX939). Other modems are a 1200/2400 bps MSK model (the MX469) and the MX589, a GMSK unit that operates at 4800, 8000, 9600, 19200 and 40000 bps.

Device	Description	Two-Way Radio	Cellular Radio	Wireless Data Modems
MX439	1200 bps MSK Modem with Serial Control	✔	✔	✔
MX469	1200/2400 bps MSK Modem with Serial Control	✔		✔
MX489	19.2k bps GMSK Modem with Serial Control	✔		✔
MX809	1200 bps MSK Modem with C-BUS Control	✔		✔
MX589	40k bps GMSK Modem with Serial Control	✔		✔
MX909	High-Speed and MOBITEX GMSK Modem	✔		✔
MX919/929	High-Speed 4-Level FSK Modem/ARDIS	✔		✔
MX939	CDPD/AMPS-WBD Full-Duplex Modem	✔	✔	✔

Table 1 - MX•COM Modem ICs

Principals of FSK/MSK/GMSK

Frequency Shift Keying (FSK) functions by assigning one carrier frequency (f1) to the "0" binary state and a second carrier frequency (f2) to the "1" binary state. Abrupt changes in carrier phase can occur as transitions take place between the two frequency states, as shown in Figure 1.

Defining the modulation index, m, as

$$m = \Delta f \times T$$

where, $\Delta f = f2 - f1$

T = binary state duration (inverse of bit rate, 1/bps)

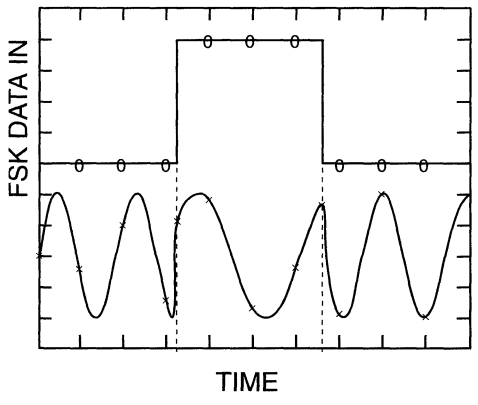


Figure 1 - Frequency Shift Keying (FSK)

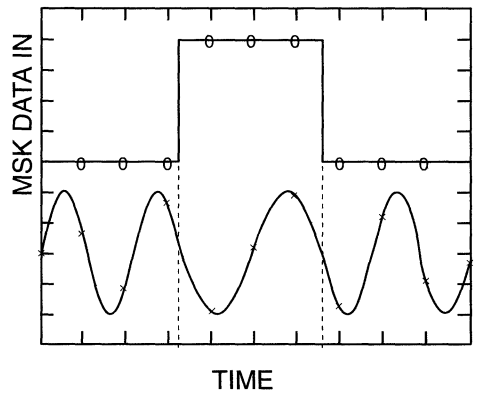


Figure 2 - Minimum Shift Keying (MSK)

CPFSK is defined as continuous phase FSK. MSK is defined as a special case of CPFSK where m=0.5, and results in minimum difference in signaling frequencies equal to bit rate/2. Continuous phase in MSK is also maintained by constraining the frequency changes to take place at the carrier zero crossing as shown in Figure 2.

Althrough phase continuity has been achieved, there remains a frequency discontinuity at each symbol transition, and to remove this requires pre-shaping of the baseband bit stream with an appropriate filter. Use of a pre-modulation low pass filter with a Gaussian charactersitics in conjunction with the MSK achives this (GMSK). Spectrum charactersitics of representative CPFSK, MSK and GMSK are shown in Figures 3 and 4.

CPFSK modulation has been adopted as the modulation standard for the Bell 202 type modem. MSK modulation was selected for RF data communications for low signal to noise environment or situations that require less bandwidth than the FSK approach. GMSK has been adopted as the modulation standard for the pan European GSM cellular network, RAM/Mobitex at 8kbps, and Cellular Digital Packet Data (CDPD) at 19.2kbps.

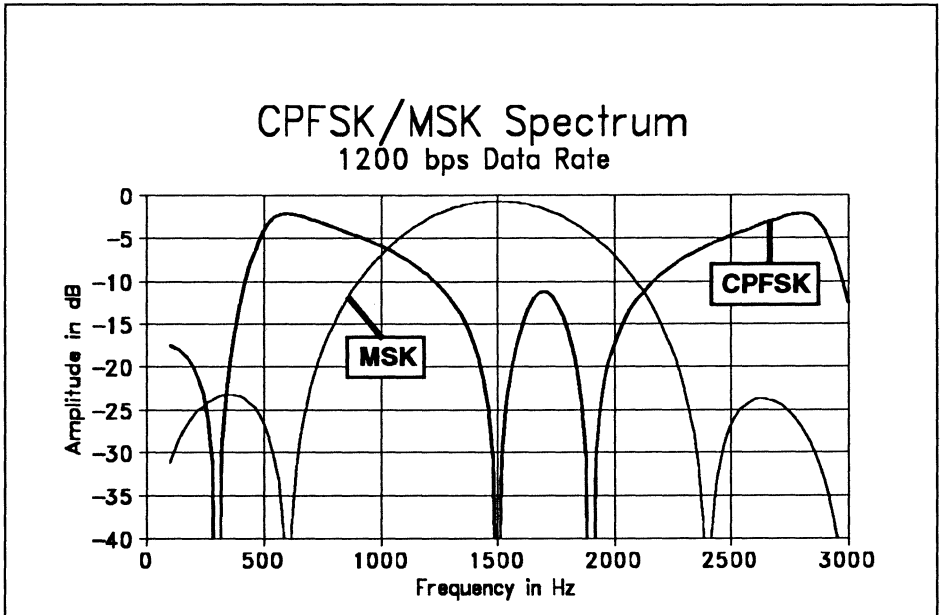


Figure 3 - MSK vs CPFSK

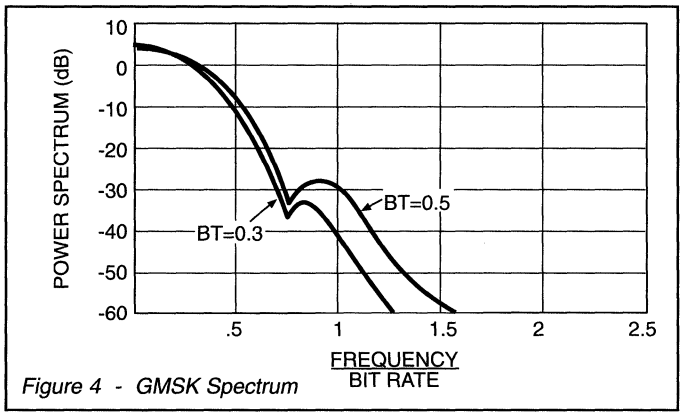


Figure 4 - GMSK Spectrum

The Effect of Modem Bandwidth on Bit Error Rate (BER)

The basic measure for rating one modem against another is its BER performance. BER is the ratio of error bits to the total transmitted bits for a given level of signal-to-noise (SNR). BER performance is dependent on the noise bandwidth at the modem's internal data detector circuit. The narrower the modem's bandwidth, the better BER for same SNR at the modem's inputs. An MSK modem has a 1200Hz noise bandwidth where a Bell 202 type has approximately 2500Hz. The improved performance using a typical FM receiver is shown in Figure 5, with the MSK modem outperforming the Bell 202 by several dB.

In a given radio link, BER performance varies with signal-to-noise, and fringe area service decreases SNR. Noise increases errors (see Figure 6). MSK-1200 performs several dB better than voice, on the premise that voice follows. In trunking and SelCall systems, the data is used to set up a voice link, so there is no point in grossly over-reaching the radio's voice range. A SINAD of 12 dB is the accepted limit of voice intelligibility, and 8 to 10 dB SINAD is the goal of MSK-1200 service.

Poor performance under good signal conditions points to elements in the detection process that are not correctly aligned. Modems made from discrete components typically need periodic re-alignment. Data carriers drift or the PLL goes off center. IC Modems lock onto quartz crystals, use digital frequency dividers and switched capacitor filters that don't drift, and don't need alignment because there's nothing to align.

Once the modem is in your radio system, you will test it. Modem testing is optimized for test time (cost) and

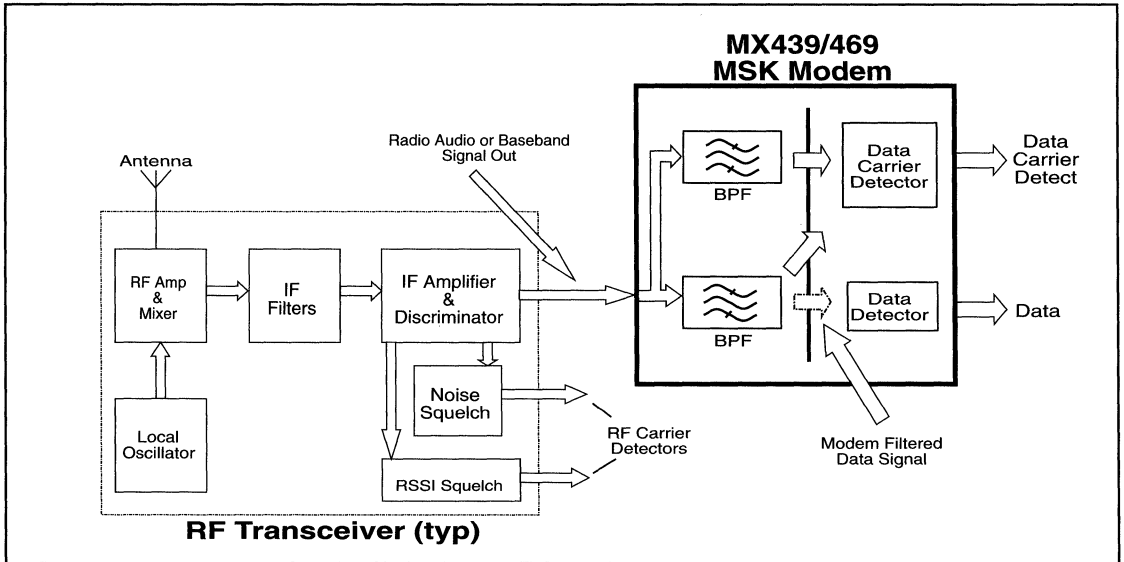


Figure 5 - MSK Modem Together With a Typical FM Receiver

statistical significance of the test results. For example, the MX439 1200 bps modem, rated at 10-3 BER at -117 dBm RF signal level, will require 12000 bits to detect up to 12 errors and will take 10 seconds to test. That is a reasonable amount of test time. However, if this modem is tested for BER of 10-4 at another RF signal level, this will require 120,000 bits for the same statistical test significance and the test time will zoom to over 100 seconds!

What happens to BER as RF levels are varied? The result of comparative testing performed with an MX439 and a typical Bell 202 IC modem installed in a typical UHF receiver is shown in Figure 6. With a signal of -117dBm (0.3μV) the MX439 delivers a BER of about 1 x 10^{-4} compared to the Bell 202 units about 1 x 10^{-3}. MSKs inherent narrower bandwidth allows filtering to remove more noise than the Bell FSK modem. This results in fewer bit errors.

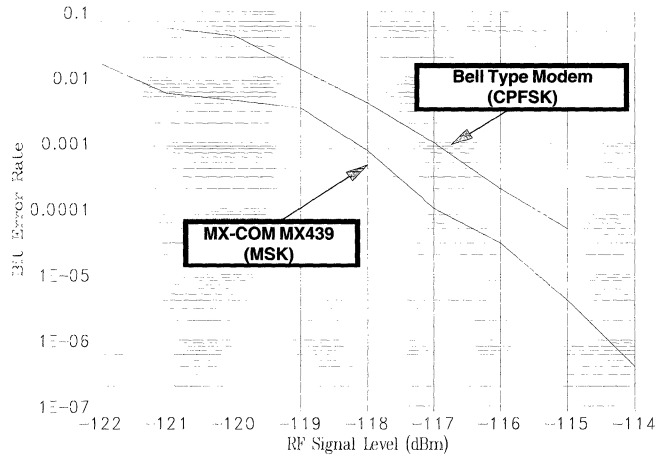


Figure 6 - Bit Error Performance

Synchronous vs. Asynchronous Data

Data transmission systems are designed to operate with either synchronous or asynchronous serial data formats. In a synchronous system, each bit is clocked in synchronism with the system master clock. The synchronizing signal may be embedded in the data signal or provided on a separate clock line. In addition, synchronous transmission requires the use of frame sync preamble to allow the receiver to determine the beginning and end of blocks of data.

This is achieved in MSK synchronous modems by encoding a preamble of 1-0-1-0 transitions (16 bits by convention), allowing receiving stations time to lock onto the edges of the received data. This is done in MX•COM modems with a digital PLL that controls a frequency divider incremented in 1/28th bit steps. A misaligned worst-case signal may take as many as 14 bit times to lock. Lacking edges on which to lock, the DPLL free runs at 1200 bps.

In asynchronous systems, each character (or word) consists of a "start bit" that starts the receiver clock and concludes with a "stop bit" that terminates the clocking. Typically, slower wireline modems use asynchronous modulation while fast ones are synchronous. All benefit from a great deal of handshaking, and smart ones default to slower speeds when the going gets tough.

FM Mobile radio is characterized by noise and fading, over a few short hops. Wirelines have noise, but little fading

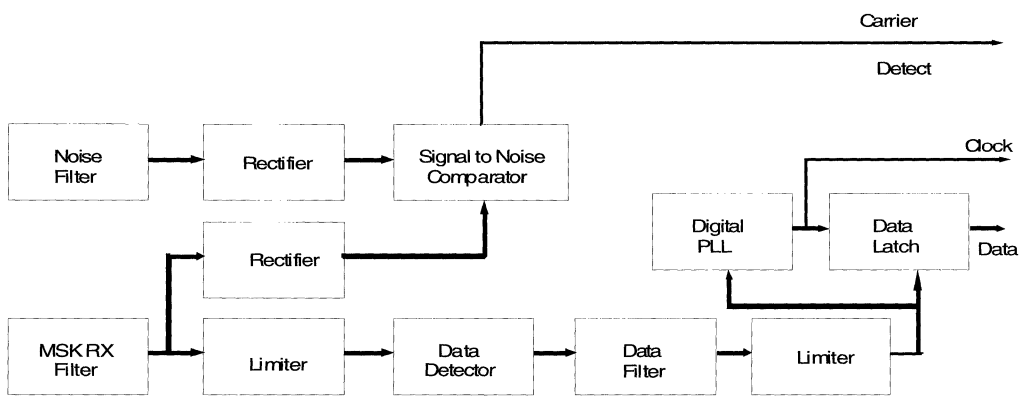


Figure 7 - MSK Receiver Block Diagram

and fewer hops. These introduce group delay and isochronous distortion or jitter -- a source of difficulty for synchronization and high Bit Error Rates (BER).

Forward Error Correction (FEC) functions best with synchronous data streams. If any single bit is corrupted, all other bits stay in position and FEC can act to correct the bit error. In asynchronous data streams, any "start" corrupted bit will result in offsetting all subsequent data bits, rendering the FEC useless.

Detecting Data Carriers in Wireline vs. Wireless

Data carrier detection methods vary depending on the transmission media characteristics. Wireline modem data carrier detectors look for broadband energy. Detectors can differentiate between white noise and signal. But wireless data carrier detection, as in the MX439, looks for a level differential between the energy in the data passband and the energy at the MSK first null point (2400HZ). That's because the output of unsquelched RF discriminator is characterized by high levels of broadband white noise which wireline broadband detectors will not be able to differentiate from signal. The circuitry in the MX439 is a pair of envelope detectors looking for a signature characteristic of MSK data.

One of the application problems of any carrier detection technique is trading off response time for false alarms. The value of the detector integration capacitor shown on the data sheet is 0.1uf. Naturally, it plays an important role in determining detector response time, but also affects the false alarm rate. Increasing the capacitor value, decreases the false alarm rate but increases the time to detect the carrier. The level of the noise which drives the detectors also controls the false alarm rate. Care must be taken not to saturate the filters in the MX439 or provide too low of a level. In the particular receiver used for our tests, RMS levels of unsquelched noise were twice that of data (data @ 3kHz deviation). The result of substituting other values of integration capacitors is shown in Figure 8. The MX439's data carrier detect threshold is 125 mVrms. For best operation noise should be kept in the 250 to 400 mVrms range. Some RF receivers may require a pad or attenuator to provide this optimum detection level. Another option might be to adjust the Q of the radio receiver's quadrature detector coil to establish the desired recovered audio level that way.

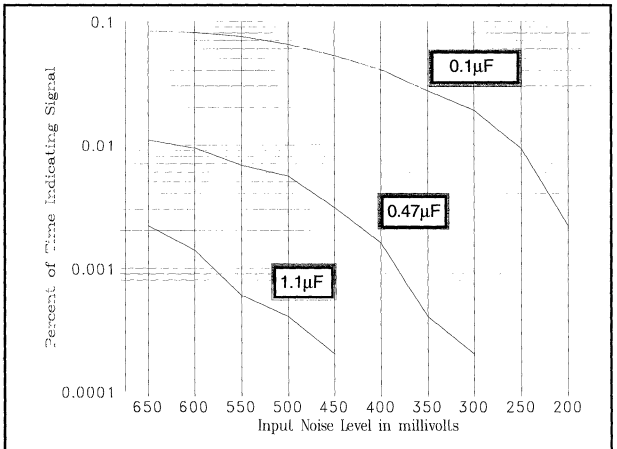


Figure 8 - False Alarm Rates

A by-product of increasing the size of the capacitor on the carrier detector pin is chatter or multiple edges in the carrier detector output. As the detected data signal appears at the carrier detect time constant pin, there is a much slower rise time due to the increased size of the time constant capacitor. As this signal has some of the detected audio components present, it causes multiple edges on the leading edge of the carrier detect output as the signal passes through the threshold point of the comparator.

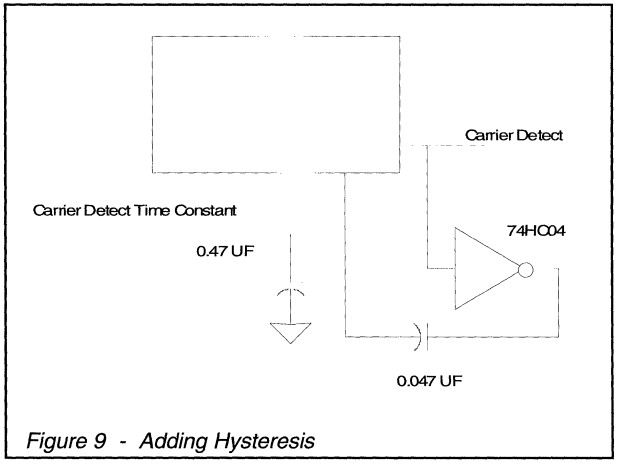


Figure 9 - Adding Hysteresis

Modems working in concert with microprocessors may be able to overcome this with software by multiple samples over time of the carrier detect signal. An alternative is to add an inverter to the output of the carrier detector and apply positive feedback at the carrier detector time constant pin to accomplish a Schmidt trigger effect. This is shown in Figure 9. Capacitive feedback was selected instead of resistive feedback because capacitor feedback is easier to control in this application.

Using an MSK Synchronous Modem with an Asynchronous Data I/O

By Bud Simciak

Asynchronous Modem Circuitry

This application note, used with current MX439/MX469 product information, outlines the construction of a low-cost asynchronous modem for the transmission of RS-232 data in the form of Minimum Shift Keying (MSK), between terminals by a radio or line medium (see page 157-170 for MX439/469 information).

The modem circuitry shown in Figure 1 accepts asynchronous data while transmitting synchronous data using the MX439/469 series modem. The MX469 may be used to transmit data at either 1200 or 2400 bps, depending on the setting of Switch 1 shown in Figure 1. The MX439 always transmits data at 1200 bps. Switch 1 must be set in position A to use the MX439. The chart below details the devices used in this application.

Performance Requirement	Associated Circuitry
RS-232 Driver/Receiver Level Translator	Maxim MAX-232
Async to Sync, Sync to Async Conversion	Exar XR-2135 or Sipex MAS7838
Data Carrier Detection	MX•COM MX439/469
Controlled RTS/CTS Delay	74HC04 Delay Element
Generation of MSK Signals	MX•COM MX439/469
Reception of MSK Signals	MX•COM MX439/469
Interface into Radio System	MX•COM MX439/469
RS-232 Handshake	Misc Circuitry

The signals required for an RS-232 handshake for asynchronous data are as follows. A complete definition of each is given at the end of this application note.

DTR	Data Terminal Ready
DSR	Data Set Ready
RTS	Request to Send
CTS	Clear to Send
TXD	Transmit Data
RXD	Receive Data

The Maxim MAX-232 converts the TTL/COMS input/output levels to ±10V RS-232 input/output levels. On power-up, the data set ready (DSR) signal is set by the MAX-232's DC to DC converter. The incoming data terminal ready (DTR) signal enables the transmitter keying signal.

The request to send (RTS) and clear to send (CTS) signals are level shifted from the RS-232 interface to TTL/CMOS signal levels. When the modem receives an RTS, the RF transmitter and the MSK tone are keyed immediately and a 30 ms to 100 ms timer is started. At the completion of the timing, a CTS signal is generated for the data terminal to allow serial data flow.

The transmit data (TXD) signal is level shifted to the TTL/CMOS levels, and applied to the Exar 2135 sync to async converter circuit. The random timed asynchronous input from the data terminal is synchronized with the transmit clock pulses of the MX439/469. If a timing error builds up due to the difference of the external asynchronous clock and the synchronous internal timing on the modem, the XR-2135 will skip a stop pulse to allow an adjustment to occur. The receiving end XR-2135 will generate a stop pulse and add it into the data flow so that no information is lost.

From the sync to async convertor, synchronous information is then sent into the MX439/469, which converts the digital '1' into one cycle of 1200 Hz sinewave and a digital '0' into one and a half cycles of 1800 Hz sinewave for 1200 bps and 1200 and 2400 Hz for 2400 bps. This sinewave is then sent on the transmitter through a level adjustment. The

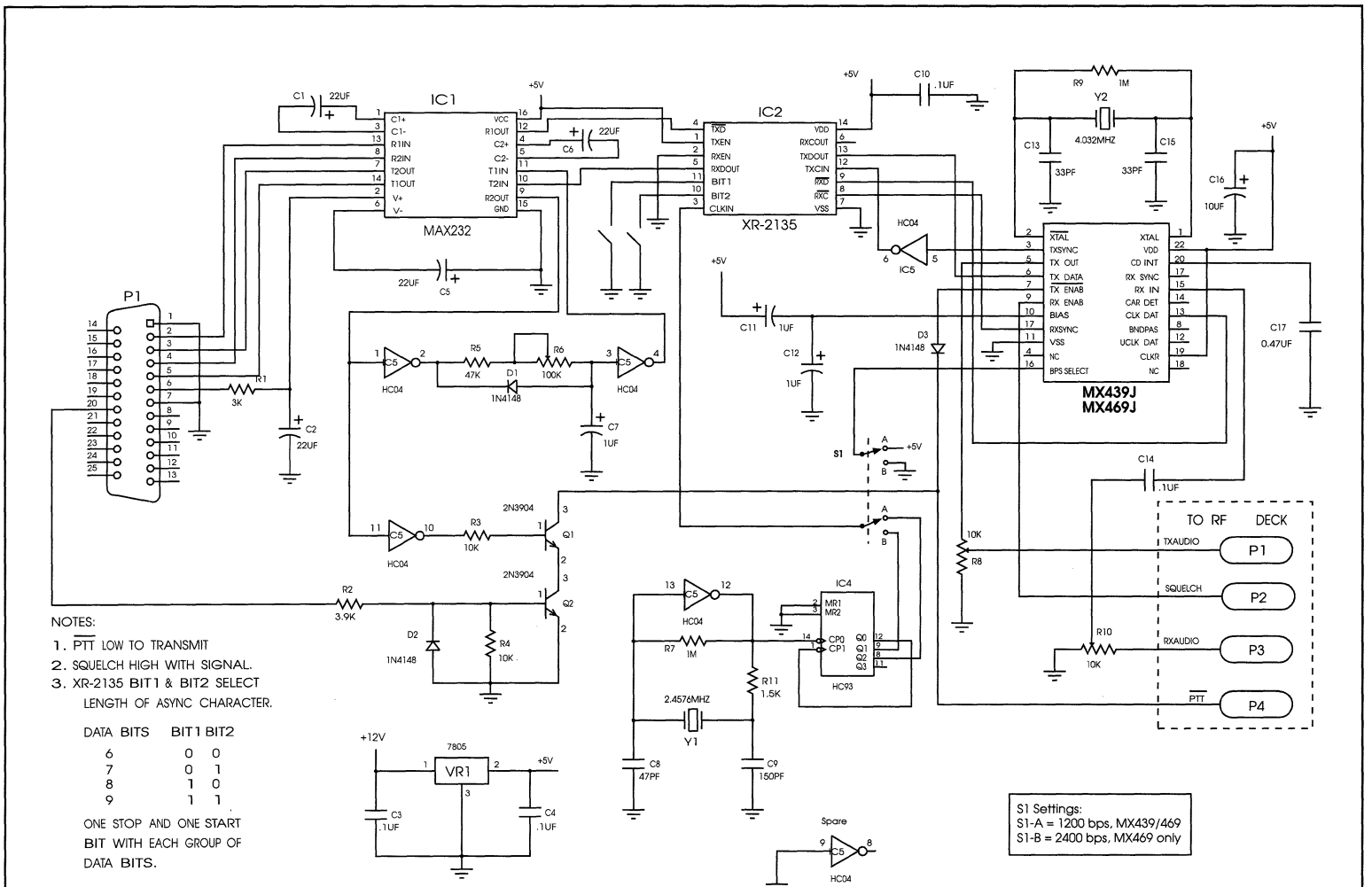


Figure 1 - Schematic Diagram of an MX439/469 in a Typical Application

signal is sufficiently band limited and level controlled to pass FCC type acceptance testing without any additional in-band filtering.

The incoming receiver signal is fed into the MX439/469 which is held in a power down mode until an RF carrier is detected by the receiver squelch circuitry. This minimizes power drain and also prohibits false information from being sent to the data terminal. If the receiver does not have a noise squelch signal, the chip's carrier detect must be used. It will detect within 12 ms the presence of the data modulation tone. This event is output on the carrier detect pin which should be used to disable the data output to minimize random data at the terminal. The use of the Schmidt trigger circuitry would minimize the 'clatter' at the beginning of the detection signal.

The tones are translated into logic levels and a digital phase lock loop is locked onto the incoming data steam within 16 bit reversals. The detected synchronous data and the recovered receive clock are sent into the XR-2135 for conversion back into asynchronous data. This information is then sent out to the data terminal through the Maxim MAX-232.

Operation in either a synchronous or asynchronous mode is achieved with a jumper. If additional RS-232 level shifting is needed for transmit and receive clocks and TX and RX enable, pins on the XR-2135 are brought low. Bringing these pins low bypasses the conversion process and allows synchronous data to pass directly through the device.

Proper clock frequency for the MX439 device is provided by a 4.032 MHz crystal. Clock frequency for the XR-2135 must be provided at 256 times the bit rate. This is accomplished by using a 2.4576 MHz crystal and dividing down by eight to 301.2 kHz (1200 bps) or by four to 602.4 kHz (2400 bps). Power is derived from a single 7805 voltage regulator. DC current measured on the first model is 12.75 mA.

Software Considerations

As with many data systems, there are certain items that should be addressed within software for proper operation. These items are:

Bit Sync Pattern
Bit Sync Time
Noise Bits at End of Transmission

Since the MSK modem is a synchronous device, a pattern must be transmitted at the beginning of each RF burst to allow the DPLL sufficient time and data transitions (a change from a one to a zero or a change from a zero to a one) to synchronize. The device requires at least sixteen of these transitions for sync to occur. This may be accomplished by appending two bytes of $55 or $AA onto the message. Once this is accomplished, adding a beginning of text character and an end of text character would ensure a correct decode at the receiving end. This is especially true at the end of the transmission. Once the RF signal ends, high level noise will be emitted from the receiver. Even if the data carrier detect or the noise squelch signals are used to gate the data off, there will be a period of noise while these circuits are making their decision. It is this random data which many times will cause a programmable logic controller or point of sale terminal to lock up. Having the message bracketed and only dealing with the information between the start and stop characters is one method of prohibiting random data from entering the actual message.

Operation with CTCSS or DCS Sub-Carriers

Because the MX439/469 modems contain a bandpass filter on the input, CTCS/DCS sub-carriers are filtered out without extra circuitry.

It is important that no energy from the tone section appears within the transmitted data signal passband of 900 to 2100 Hz for 1200 bps or 600 to 3000 Hz for 2400 bps. It is equally important that the tone and data signals are not summed together and sent into the limiter section of the transmitter. The limiter represents a nonlinearity and would generate intermodulation products within the data bandpass which when received generate errors in the decoding of the data. Tone is normally summed into an FM transmitter after the limiting.

Radios designed only for data do not require a speech limiter, allowing tone and data to be summed directly.

RS-232 Handshake

The RS-232 handshake for asynchronous data requires the following signals:

Data Terminal Ready is a signal from the terminal or computer that indicates to the modem that the unit is powered and active. An RF transmission should not be enabled if the Data Terminal is not active.

Data Set Ready is a signal from the modem that indicates to the terminal that the unit is powered and active. Many terminals or computers will not allow data to flow without this condition being true.

Request to Send emanates from the terminal or computer. The software or user has decided that transmission should begin and requests that the RF carrier be turned on.

Clear to Send is a signal that originates from the modem. It is sent in response to a RTS, the request to send signal from the terminal or computer after certain criteria have been met. It is not sent until sufficient time has expired after the transmitter keyed to allow adequate settling time for both the RF transmitter and receiver. It would not be sent if there is an RF carrier on the channel indicating another user. Finally, it would not be sent if a high VSWR were detected on the transmitter when it was keyed. (Not all transmitters are provided with a VSWR detector.)

Transmit Data and Receive Data is the actual asynchronous data flow. Transmit data is data coming from the terminal and Receive data is data flowing into the terminal.

Another term often heard is DTE and DCE ends of RS-232. This refers to what part of the handshake is expected and what the functions of the RS-232 connectors would be. Most often a computer would be programmed to be a DTE or data terminal end of the information flow. When one computer wishes to talk to another computer, it's like two people transmitting on their radios at the same time. Nobody hears the other! If one were to use a 'null' modem cable, the wires are interchanged such that one of the data terminals is now wired like a data communication device. The same is true of two modem devices. A modem device is a DCE (data communication device) which cannot be plugged into another DCE. However, if a few additional signals are available, one DCE could be used to daisy chain into another DCE as shown in Figure 2. As can be seen the data carrier detect lines are used to key the companion modem unit. The originating end must be programmed with sufficient delay to allow the RTS/CTS delay of the modems to occur prior to the beginning of any information transfer.

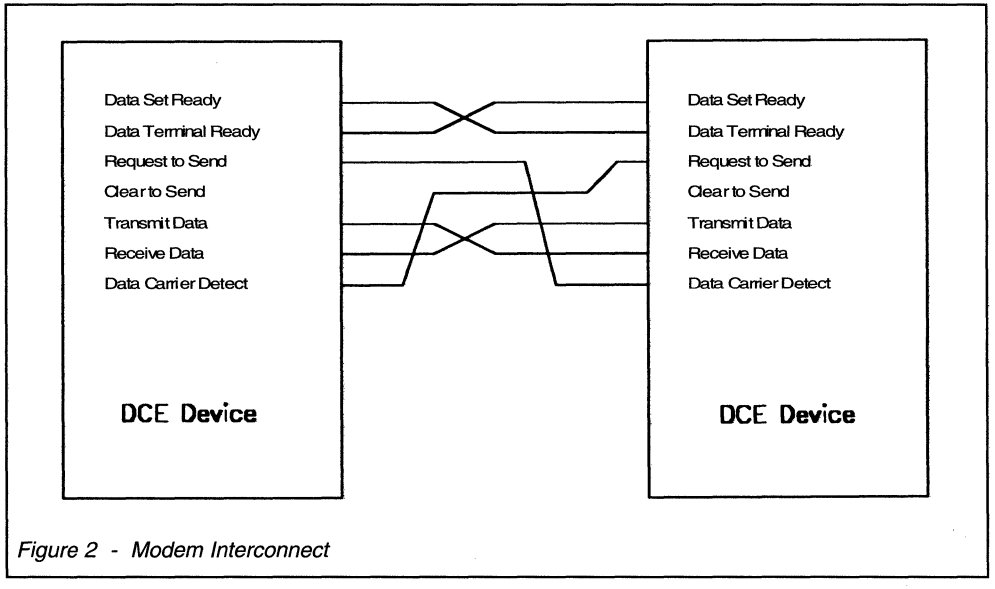


Figure 2 - Modem Interconnect

Error Detection & Correction of MPT1327 Formatted Messages

using MX419, MX429, MX439, MX469, MX489 or MX809 devices

by Pam Roberts

1.1 Background

MPT1327 messages are transmitted as 64-bit 'codewords', where each codeword contains 48 information bits followed by 16 check bits:

Bit No:	1 48	49 64
	information field	check bits

(Bit number 1 is transmitted first.)

These check bits allow the receive terminal to *detect* all odd numbers of errors, any 2 or 4 errors, and any error-burst up to length 16 in a codeword, and also to *correct* errors in the received codeword, although it should be noted that the higher the degree of error correction applied, the more likely is false decoding.

This document gives algorithms for:

Generation of the check bits of a transmitted codeword.
Received codeword *error detection.*
Limited *error correction* of a received codeword.

These algorithms may be used with any bit or byte oriented modem, such as the **MX419**, **429**, **439, 469, 489** or **809**, although the **MX429** and **MX809** devices can perform *check bit generation* and *error detection* automatically and the **MX429** also provides a 16-bit 'Syndrome' output which may be used to aid *error correction.*

1.2 Generation of Transmit Codeword Check Bits

1.2.1 Theory

The first 15 check bits are derived from a (63,48) cyclic code by using codeword bits 1 to 48 as the coefficients X^{62} to X^{15} (in that order) of a 63 bit polynomial, which is then divided modulo-2 by the generating polynomial;

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + X^0 \qquad (11101000\ 00010101 \text{ binary})$$

On completion of the division, the 15 coefficients X^{14} to X^0 of the remainder are used as the first 15 check bits (codeword bits 49 to 63), with the X^0 coefficient (bit 63 of the complete codeword) inverted.
Finally, bit 64 of the codeword is added to provide an even parity check of the whole 64-bit codeword.

1.2.2 Example of Transmit Codeword Generation

Information field; 6 data bytes

```
      89       AB       CD       EF       12       34      Hex
10001001 10101011 11001101 11101111 00010010 00110100  Binary
```

Polynomial division

```
X62 ..................................................................... X0
10001001 10101011 11001101 11101111 00010010 00110100 00000000 0000000
11101000 00010101
 1100001 10111110 1
 1110100 00001010 1
   10101 10110100 010
   11101 00000010 101
    1000 10110110 1110
    1110 10000001 0101
     110 00110111 10111
     111 01000000 10101
       1 01110111 0001010
       1 11010000 0010101
         10100111 00111111
         11101000 00010101
          1001111 00101010 1
          1110100 00001010 1
           111011 00100000 01
           111010 00000101 01
                1 00100101 0010111
                1 11010000 0010101
                  11110101 00000101
                  11101000 00010101
                     11101 00010000 000
                     11101 00000010 101
                             10010 10110010 001
                             11101 00000010 101
                              1111 10110000 1001
                              1110 10000001 0101
                                 1 00110001 1100010
                                 1 11010000 0010101
                                   11100001 11101110
                                   11101000 00010101
                                       1001 11111011 0000
                                       1110 10000001 0101
                                        111 01111010 01010
                                        111 01000000 10101
                                             111010 11111000 00
                                             111010 00000101 01
                                                    11111101 0100000
```

Remainder with last bit inverted:

```
                                                    11111101 0100001
```

Complete codeword, including parity bit:

```
Bit; 1                                                              64
     10001001 10101011 11001101 11101111 00010010 00110100 11111101 01000010
        89       AB       CD       EF       12       34       FD       42
```

1.2.3 'C' Language Algorithm

```
/*****************************************************************************/
/*    Function gen_ckbits() returns the first 15 check bits of a transmit  */
/*    codeword (codeword bits 49 to 63). Bit 15 of the returned value will */
/*    be codeword bit 49, bit 1 of the returned value will be codeword bit */
/*    63, and the lsb (bit 0) should be ignored.                           */
/*    The last bit (64) of the codeword must be derived separately, to     */
/*    give even parity of the whole 64-bit codeword.                       */

gen_ckbits()
    {
    int n,bit;
    unsigned int ckbits = 0;                    /* Clear check bits         */
    for(n=1;n <= 48;n++)                        /* 48 information bits......*/
        {                                       /*                          */
        bit = getbit_tx(n);                     /* Get each bit in turn ... */
        if( 1 & (bit ^ (ckbits >> 15)))         /*     XOR tx bit with MSB  */
                                                /*     of checkbits and if  */
                                                /*     the result == 1      */
            ckbits ^= 0x6815;                   /*     then XOR checkbits   */
                                                /*     with 6815 Hex        */
        ckbits <<= 1;                           /* ... Shift check bit word */
                                                /*        one bit left,     */
        }
    return(ckbits ^ 0x0002);                    /* Return checkbits with    */
                                                /* codeword bit 63 inverted */
    }

/*    Function getbit_tx(n) should return bit 'n' (1 to 48) of the transmit*/
/*    codeword information field.                                          */

getbit_tx(n)
    {
    return(/* 1 or 0 */);
    }
```

1.3 Receive Codeword Checking & Error Correction

1.3.1 Theory

The parity of the received 64-bit codeword is checked, then bit 63 of the codeword is inverted. The first 63 bits of the resulting codeword are then used as the coefficients X77 to X15 of a 77 bit polynomial, which is then divided modulo-2 by the 'generating polynomial'. If the remainder is zero, and the parity check is met, then no errors have been detected.

The 15-bit remainder of this division is used as the least significant 15 bits of the 16-bit 'Syndrome' word generated by the MX429 (and by the algorithm of section 3.4), while the msb of the Syndrome word is set to '1' if the parity of the received codeword is incorrect. The resulting Syndrome word value can give an indication of which bit(s) of the codeword have been received incorrectly; see section 3.4.

1.3.2 Example of Receive Codeword Checking: No Errors

Received codeword: 6 bytes:

```
         89       AB       CD       EF       12       34       FD       42
      10001001 10101011 11001101 11101111 00010010 00110100 11111101 01000010
  Bit;1                                                                    64
```

Step 1: even parity checked OK

Step 2: invert bit 63 then divide first 63 bits (shifted left 15 places) by generating polynomial:

```
X77 ..........................................................................X0
10001001 10101011 11001101 11101111 00010010 00110100 11111101 01000000 00000000 000000
11101000 00010101
 1100001 10111110 1
 1110100 00001010 1
   10101 10110100 010
   11101 00000010 101
    1000 10110110 1110
    1110 10000001 0101
     110 00110111 10111
     111 01000000 10101
       1 01110111 0001010
       1 11010000 0010101
         10100111 00111111
         11101000 00010101
          1001111 00101010 1
          1110100 00001010 1
           111011 00100000 01
           111010 00000101 01
                1 00100101 0010111
                1 11010000 0010101
                  11110101 00000101
                  11101000 00010101
                     11101 00010000 000
                     11101 00000010 101
                           10010 10110010 001
                           11101 00000010 101
                            1111 10110000 1001
                            1110 10000001 0101
                               1 00110001 1100010
                               1 11010000 0010101
                                 11100001 11101110
                                 11101000 00010101
                                     1001 11111011 1111
                                     1110 10000001 0101
                                      111 01111010 10101
                                      111 01000000 10101
                                            111010 00000101 01
                                            111010 00000101 01
                                            000000 00000000 00000000 00000000 000000
```

Remainder = zero
MX429 'Syndrome' word: 00000000 00000000
No errors detected

1.3.3 Example of Receive Codeword Checking: 2 Errors

Received codeword: 6 bytes: bits 9 & 10 in error

```
         89       6B       CD       EF       12       34       FD       42
      10001001 01101011 11001101 11101111 00010010 00110100 11111101 01000010
       errors; xx
  Bit;1                                                                    64
```

Step 1: even parity checked OK

Step 2: invert bit 63 then divide first 63 bits (shifted left 15 places) by generating polynomial:

x^{77} ..... x^{0}

```
10001001 01101011 11001101 11101111 00010010 00110100 11111101 01000000 00000000 000000
11101000 00010101
 1100001 01111110 1
 1110100 00001010 1
   10101 01110100 010
   11101 00000010 101
    1000 01110110 1110
    1110 10000001 0101
     110 11110111 10111
     111 01000000 10101
       1 10110111 0001010
       1 11010000 0010101
          1100111 00111111 1
          1110100 00001010 1
            10011 00110101 011
            11101 00000010 101
             1110 00110111 1100
             1110 10000001 0101
                  10110110 10011111
                  11101000 00010101
                   1011110 10001010 0
                   1110100 00001010 1
                    101010 10000000 10
                    111010 00000101 01
                     10000 10000101 110
                     11101 00000010 101
                      1101 10000111 0111
                      1110 10000001 0101
                        11 00000110 001000
                        11 10100000 010101
                           10100110 01110110
                           11101000 00010101
                            1001110 01100011 0
                            1110100 00001010 1
                             111010 01101001 10
                             111010 00000101 01
                                    1101100 11110100 1
                                    1110100 00001010 1
                                      11000 11111110 011
                                      11101 00000010 101
                                        101 11111100 11011
                                        111 01000000 10101
                                         10 10111100 011101
                                         11 10100000 010101
                                          1 00011100 0010000
                                          1 11010000 0010101
                                            11001100 00001011
                                            11101000 00010101
                                              100100 00011110 01
                                              111010 00000101 01
                                               11110 00011011 000
                                               11101 00000010 101
                                                  11 00011001 101000
                                                  11 10100000 010101
```

```
10111001 11110100
11101000 00010101
 1010001 11100001 0
 1110100 00001010 1
  100101 11101011 10
  111010 00000101 01
   11111 11101110 110
   11101 00000010 101
      10 11101100 011000
      11 10100000 010101
       1 01001100 0011010
       1 11010000 0010101
         10011100 00011110
         11101000 00010101
          1110100 00001011 0
          1110100 00001010 1
```

Remainder; non zero

```
                                                    1 100000
```

MX429 'Syndrome' word: `00000000 01100000`

Therefore, from the table in section 3.4, codeword bits 9 & 10 of the received codeword are incorrect.

1.3.4 'C' Language Algorithm

The following algorithm produces a 16-bit 'Syndrome'similar to that generated by the MX429, which will have a value of zero only if no errors have been detected in the received codeword.

```
/*************************************************************************/
/*    Function calc_syndrome() returns the 16-bit 'Syndrome' of a received */
/*    MPT1327 64-bit codeword.                                             */

calc_syndrome()
    {
    int n,bit;
    int parity=0;                              /* Clear parity register    */
    int syndrome=0;                            /* Clear 16-bit syndrome    */
    for(n = 1;n <= 64;n++)                     /* 64-bit codeword...       */
        {                                      /*                          */
         bit = getbit_rx(n);                   /* Get each bit in turn;..  */
         parity ^= bit;                        /* .. update parity         */
         if(n == 63) bit ^= 1;                 /* .. then invert bit 63    */
         if(n < 64)                            /* .. for bits 1 to 63;.... */
            {                                  /*    .. shift parity word  */
            syndrome <<= 1;                    /*          one bit left.   */
            if( 1 & (bit ^ (syndrome >> 15)))  /*    .. XOR rx bit with    */
                                               /*       MSB of parity word,*/
                                               /*       and if result == 1 */
                syndrome ^= 0x6815;            /*       then XOR syndrome  */
                                               /*       with 6815 Hex.     */
            }                                  /*                          */
        }
    syndrome &= 0x7FFF;                        /* Finally, replace MSB of  */
    if(parity)                                 /*  syndrome word with the  */
        syndrome |= 0x8000;                    /*  calculated parity bit   */
    return(syndrome);
    }

/*    Function getbit_rx(n) should return the bit 'n' of the received      */
/*    codeword; Bit '1' is the first bit to be received, bit '64' the last.*/

getbit_rx(n)
    {
    return(/* 1 or 0 */);
    }
```

1.4 Error Correction

Single-bit and bit-pair errors in a received codeword may be corrected by comparing the 'Syndrome' word (generated by the MX429 or the algorithm of section 3.4) against the entries in the following table, and if a match is found inverting the corresponding bits.

Syndrome (Hex)	Error bits	Syndrome (Hex)	Error bits	Syndrome (Hex)	Error bits	Syndrome (Hex)	Error bits
0003	14, 15	468D	40, 41	8001	15	B456	25
0006	13, 14	4841	61, 62	8002	14	B484	19
000C	12, 13	4989	33, 34	8004	13	B83F	62
0018	11, 12	4B7B	45, 46	8008	12	B887	34
0030	10, 11	4BD7	22, 23	8010	11	B929	46
0060	9, 10	4E0F	16, 17	8020	10	B94D	23
00C0	8, 9	502A	62, 63	8040	9	BA05	17
0180	7, 8	50CE	34, 35	8080	8	C000	1
0300	6, 7	51B7	46, 47	8100	7	C02E	36
0600	5, 6	51E1	23, 24	8200	6	C31C	50
0C00	4, 5	530D	17, 18	8400	5	C60A	39
15D3	43, 44	574C	41, 42	8800	4	C748	57
1763	20, 21	5A62	48, 49	88E9	60	C885	28
1800	3, 4	5CD1	47, 48	8A09	32	CA3E	54
18CD	28, 29	5CFA	24, 25	8CB1	44	D048	29
193B	59, 60	5D8C	18, 19	8D21	21	E401	38
1E1B	31, 32	6000	1, 2	9000	3	E588	41
21CD	56, 57	6039	36, 37	90C7	52	E685	56
220B	38, 39	6292	50, 51	91D2	59	E815	63
2867	35, 36	6334	26, 27	9412	31	E849	35
2BA6	42, 43	64EC	57, 58	9962	43	E89E	47
2D31	49, 50	650F	39, 40	9A2B	26	E8AC	24
2E7D	25, 26	6815	63, 64	9A42	20	E908	18
2EC6	19, 20	6CAE	52, 53	A000	2	EE2D	49
3000	2, 3	6F21	54, 55	A017	37	F07E	61
3149	51, 52	740B	15, 16	A18E	51	F10E	33
319A	27, 28	786C	29, 30	A305	40	F252	45
3276	58, 59	7897	60, 61	A3A4	58	F29A	22
3657	53, 54	7B07	32, 33	A51F	55	F40A	16
3C36	30, 31	7EE3	44, 45	A824	30	F91F	27
439A	55, 56	7FBB	21, 22	B2C4	42	FC69	53
4416	37, 38	8000	64	B44F	48		

Example:
Transmitted codeword:

```
Bit; 1                                                                  64
     10001001 10101011 11001101 11101111 00010010 00110100 11111101 01000010
      errors; xx
```

Received codeword:

```
     10001001 01101011 11001101 11101111 00010010 00110100 11111101 01000010
```

For this received codeword, the 'Syndrome' will be 0060H, which appears in the table, indicating that the 9th & 10th bits received are incorrect and should be inverted.

GMSK for High Speed Wireless Modems

By Bud Simciak and Sam Rizk

I. Introduction

FCC regulations limit the spectral emissions of mobile FM radio transmissions. These regulations state that out-of-band radiated power in adjacent channels should be generally bounded 60-80 dB below that in the desired channel, as shown in Figure 1. To meet these constraints, it is necessary to band-limit the RF output signal spectrum. The RF power spectrum envelope is easier to control via the intermediate-frequency (IF) or the baseband rather than the final RF stage because the transmitted power is variable. Gaussian filtered MSK (applied to the baseband, i.e. premodulation) yields a constant envelope, facilitating FCC compliance.

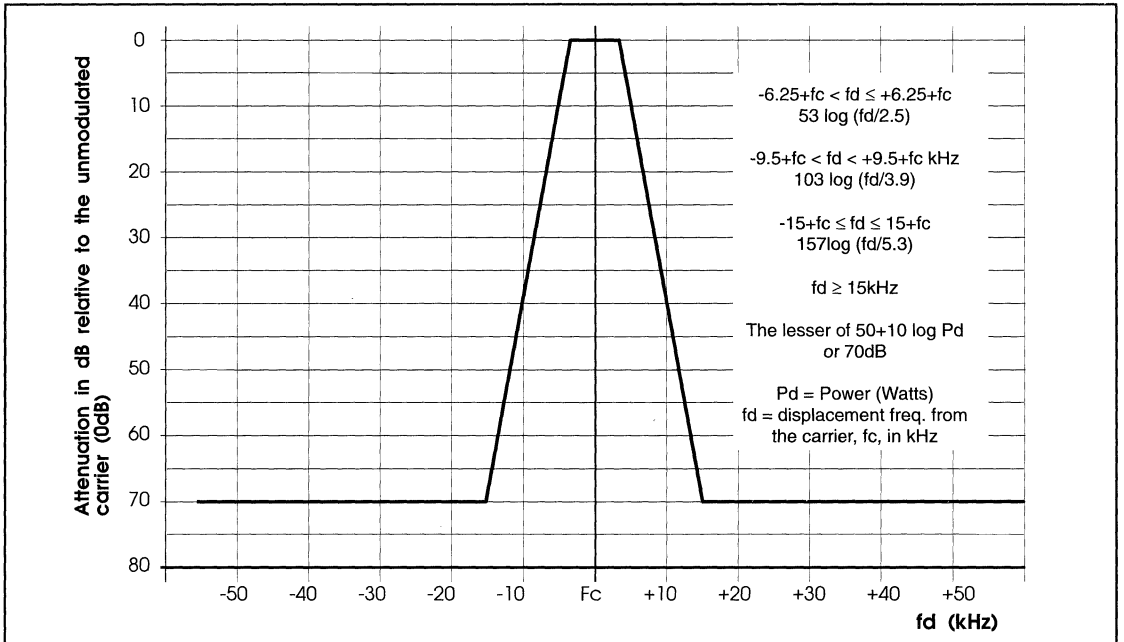


Figure 1 - Out-of-band Emission Attenuation Data Input [2]

II. What is GMSK?

GMSK uses a premodulation low-pass filter with a Gaussian (bell-shaped) characteristic to smooth out the symbol edges, narrowing the spectral bandwidth of the baseband data signal. The filtered symbol is then applied to the MSK modulator as shown in Figure 2 [1]. MSK is a binary digital frequency modulation technique with a modulation index of 0.5.

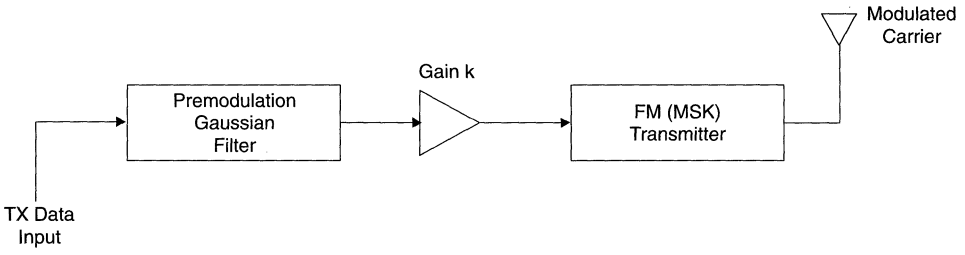
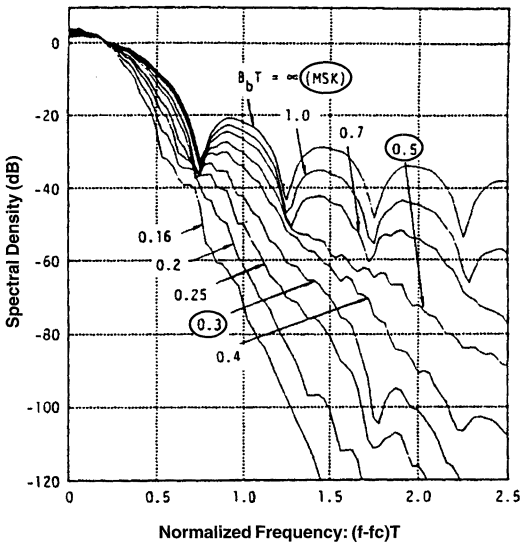


Figure 2 - A Typical GMSK Transmitter

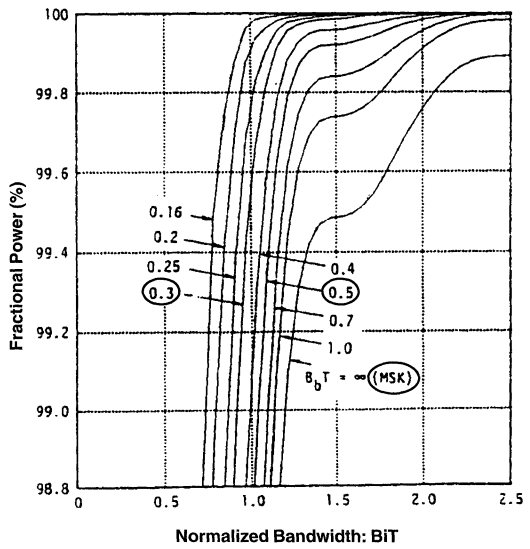
III. GMSK Power Spectral Density (PSD)

The GMSK output power spectrum is more compact than that of MSK, as shown in the following graphs.



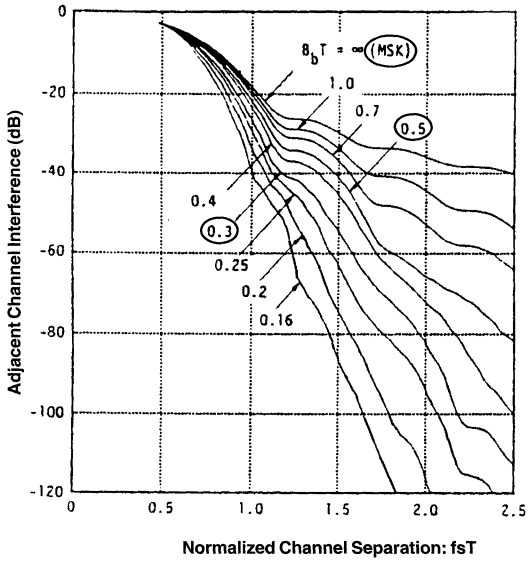
This figure shows Power Spectral Density versus the normalized frequency difference from the carrier center frequency (f-fc)T, where the normalized 3 dB bandwidth of the premodulation Gaussian LPF (BT) is a parameter.

Figure 3 - Power Spectra of GMSK [1]



This figure shows the fractional power in the desired channel versus the normalized bandwidth of the LPF (BT).

Figure 4 - Fractional Power Ratio of GMSK [1]



This figure shows the out-of-band radiation power in the adjacent channel to the total power in the desired channel where the normalized channel spacing (fsT) is a parameter.

Figure 5 - GMSK Adjacent Power Interference [1]

IV. GMSK Demodulator

Figure 6 shows a typical GMSK receiver block diagram. The received RF modulated carrier is down-converted in multiple stages. The output of the last stage is usually centered at an intermediate frequency (IF) of 455 kHz . The modulated IF carrier is applied to a bandpass filter. The filtered signal is then applied to an amplitude limiter and the output is applied to a conventional frequency discriminator. The discriminator output is passed through the premodulation filter and timing recovery subsystem. The data detector processes the analog waveform in order to decide which bit has been transmitted.

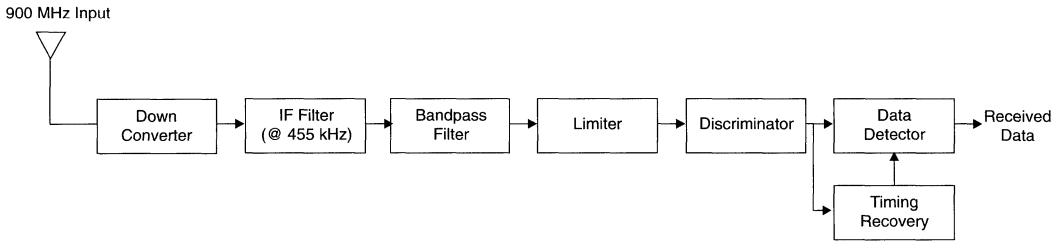


Figure 6 - Functional Block Diagram of a GMSK Receiver

V. Bit Error Rate (BER)

The reliability of the data message produced by the GMSK receiver is highly dependent on the following:

1. Receiver thermal noise: this is introduced partly by the receive antenna and mostly by the radio receiver front end.
2. Channel fading: This is caused by the multipath propagation nature of the radio channel.
3. Bandlimiting: This is mostly associated with the receiver IF frequency and phase characteristics.
4. DC drifts: may be caused by a number of factors such as temperature variations, asymmetry of the frequency response of the receiver, frequency drifts of the receiver local oscillator.
5. Frequency offset: this refers to the receiver carrier frequency drift relative to the frequency transmitted caused by the finite stability of all the frequency sources in the receiver. The shift is also caused partly by Doppler shifts which result due to the relative transmitter/receiver motion. The frequency offset causes the received IF signal to be off-center with respect to the IF filter response, and this causes more signal distortion. The frequency offset also results in a proportional DC component at the discriminator output.
6. Timing errors: The timing reference causes the sampling instants to be offset from the center of the transmit eye.

Figures 7 & 8 [2] show the theoretical BER performance of GMSK, with the receiver frequency offset as a parameter and IF filter responses of non-equalized and phase equalized 8-pole Butterworth, respectively.

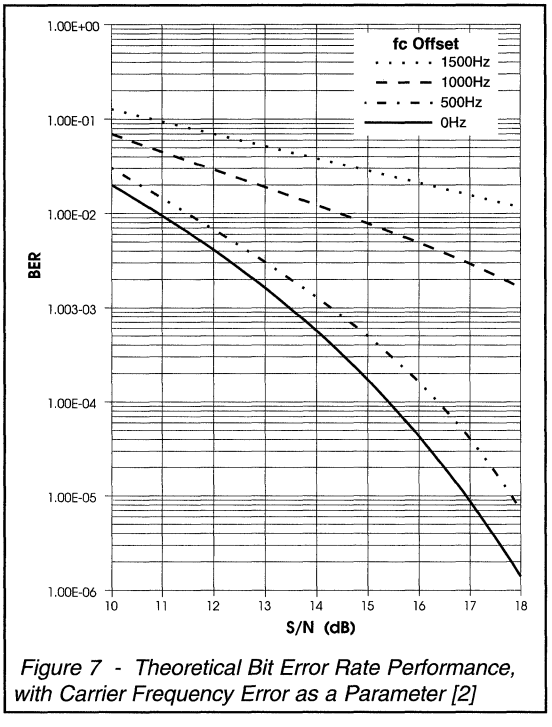


Figure 7 - Theoretical Bit Error Rate Performance, with Carrier Frequency Error as a Parameter [2]

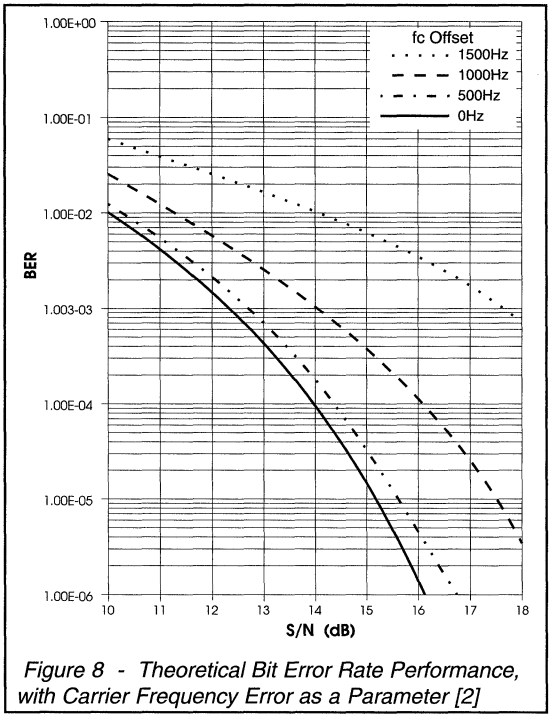


Figure 8 - Theoretical Bit Error Rate Performance, with Carrier Frequency Error as a Parameter [2]

VI. MX•COM GMSK Modem IC's

For optimum performance, the received signal applied to the MX589 for random transmitted data should be as close as possible to the eye diagrams shown in Figure 9. The eye diagram is a measure of the Inter-Symbol-Interference (ISI) caused by channel filtering. Of particular importance are general symmetry, cleanliness of the zero crossings, and — for a BT of 0.3 — the relative amplitude of the inner eye opening.

To achieve this, attention must be paid to:

- Linearity and frequency/phase response of the TX frequency modulator. Unless the transmit data is especially encoded to remove low frequency components, the modulator frequency response should extend down to a few Hz, two-point modulation being necessary for synthesized radios.

- Bandwidth and phase response of the RX IF filters.

- Accuracy of the TX and RX carrier frequencies, as any difference will shift the received signal towards one of the skirts of the IF filter response.

Ideally the RX demodulator should be DC coupled to the MX589 RX Signal In pin (with a DC bias added to center the signal around $V_{DD}/2$), however AC coupling can be used if the following is true:

- The 3 dB cut-off frequency is 20 Hz or below (i.e. a 0.1 μF capacitor in series with 100kΩ).

- The data does not contain long sequences of consecutive ones or zeroes.

- Sufficient time is allowed after a step change at the discriminator output (resulting from channel changing or the appearance of an RF carrier) for the voltage into the MX589 to settle before the RXDCacq line is strobed.

VII. Data Formats

The receive section of the MX589 works best with data which has a reasonably 'random' structure —the data should contain approximately the same number of 'ones' as 'zeroes' with no long sequences (>100 bits) of consecutive 'ones' or 'zeroes'.

Several techniques have been devised to randomize the data [5]. For example, a common method is 'exclusive-ORing' it with the output of a binary pseudo-random pattern generator.

Where data is transmitted in bursts, each burst should be preceded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble for BT=0.3 should be at least 16 bits long, and should preferably consist of alternating pairs of '1's and '0's i.e. '110011001100 .....'; the eye of pattern '10101010 ....' has the most gradual slope and will yield poor peak levels for the RX circuits. For BT=0.5 the eye pattern of '10101010...' has less intersymbol interference (DC Acq pin should be held high during preamble) and may be used as the preamble (see Figure 9).

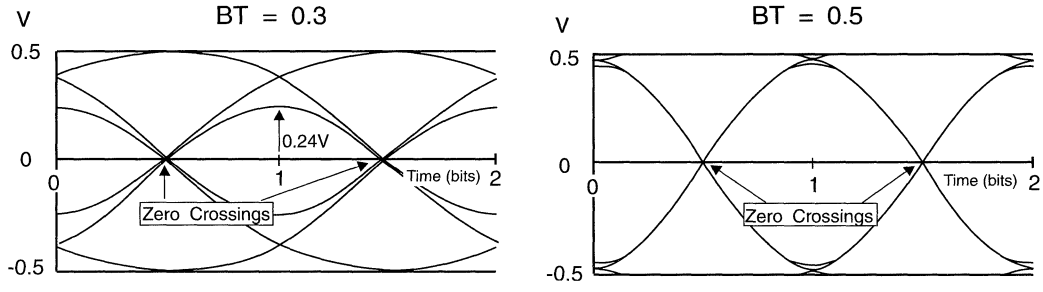


Figure 9 -- Voltages with respect to $V_{DD}/2$

VIII. Acquisition & Hold Modes

The RXDCacq and PLLacq inputs must be held "high" for about 16 bit-times at the start of reception to ensure that the DC measurement and Timing Extraction circuits lock onto the received signal correctly. Once lock has been achieved, then the inputs should be taken "low" again.

In most applications, there will be a DC step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the distant transmitter is turned on. The MX589 can tolerate DC offsets in the received signal of at least ±0.5V with respect to V_{BIAS}. However to ensure that the DC offset compensation circuit operates correctly and with minimum delay, the "low" to "high" transition of the RXDCacq and PLLacq inputs should occur after the mean input voltage to the MX589 has settled to within about 0.1V of its final value. (Note that this can place restrictions on the value of any series signal coupling capacitor.)

The RXHold input may be usued to freeze the Level Measuring and Clock Extraction circuits during a fade. It may also be used in systems which employ a continuously transmitting control channel to freeze the receive circuitry during transmission of a data packet, allowing reception to resume afterwards without losing bit synchronization. To achieve this the MX589 Xtal clock needs to be accurate enough that the derived RXClock output does not drift by more than about 0.1 bit time from the actual received data rate during the time that the RXHold input is "low." The RXDCacq input, however, may need to be pulsed "high" to re-establish the level measurements if the RXHold input is "low" for more than a few hundred bit-times.

The voltages on the Doc1 and Doc2 pins reflect the average peak positive and negative excursions of the (filtered) receive signal, and could therefore be used to drive a measure of the data signal amplitude. Note, however, that these pins are driven from very high impedance circuits, so that the DC load presented by any external circuitry should exceed 10 MΩ to V_{BIAS}.

IX. Conclusion

The maximum data rate that can be transmitted over a radio channel depends on:

- Channel spacing
- Allowable adjacent channel interference
- TX filter bandwidth (BT)
- Peak carrier deviation (modulation index)
- TX & RX carrier frequency accuracies and stabilities.
- Modulator & Demodulator linearity
- RX IF filter frequency & phase characteristics
- Use of radom data and block interleaving techniques
- Use of error correction techniques
- Acceptable error rate.

As a guide:

- For Mobitex operation, a raw data rate of 8000 bps at 12.5 kHz channel spacing is achievable using at BT of 0.3, ±2 kHz maximum deviation and no more than 1500 Hz discrepancy between TX & RX carrier frequencies.

- For CDPD operation, a raw data rate of 19.2 kbps at 30 kHz channel spacing is achievable using at BT of 0.5, ±8 kHz maximum deviation and no more than 3 kHz discrepancy between TX & RX carrier frequencies.

- Forward Error Correction (FEC) and interleaving are commonly incorporated in the protocols to reduce the effect of burst errors.

- Reducing the data rate to 4800 bps is an alternative that would allow the BT to be increased to 0.5, improving the error rate performance.

References

1. Murota, K., et al., "GMSK Modulation for Digital Mobile Radio Telephony", IEEE transactions on communications. Vol.COM-29, NO.7 July 1981
2. RAM Mobile Data, Radio "Modem Reference Design Guide", Woodbridge, New Jersey, USA.
3. Anderson, J., et al., "Digital Phase Modulation" Plenum, 1986.
4. Smith, D., "Digital Transmission Systems" Van Nostrand Reinhold, 1985
5. Couch II, L., "Digital and Analog Communication Systems" MacMillan, 1990.
6. Varrall, G., et al., "Data Over Radio" Quantum, 1992.

GLOSSARY

AMPS/NAMPS	Advanced Mobile Phone Service is a cellular system used in the United States. NAMPS (Narrow AMPS) uses FDMA techniques to derive three voice channels from one AMPS channel.
ANI	Automatic Number Identification: Identification of the transmitting party by a preassigned number.
ANSI	American National Standards Institute: A voluntary organization in the United States that coordinates standards.
Asynchronous transmission	A mode of data transmission in which each bit is not in sync. regarding frequency or timing. Signals are sent as groups of a specified length with start and stop bit indicators at the beginning and end of each group.
Bandwidth	The range of frequencies within which a device can transmit or receive.
Baseband	The band of frequencies which is modulated on a carrier or subcarrier in a wire or radio transmission system to form the transmitted signal.
Baud	A unit that measures signaling speed in signal events per second. This may not be the same as bits per second.
BCD	Binary Coded Decimal: A binary (1,0) numbering system in which the digits 0 through 9 are represented by four bits.
BER	Bit Error Rate: A ratio of the number of transmitted bits that are incorrectly received to the number that are correctly received.
Bit Rate	The speed at which bits are transmitted over a data channel, given in bits per second (bps).
Carrier	A carrier is a wave capable of being modulated by an information-carrying signal. The use of multiple carriers permits multiple voice frequency signals in the same transmission, as in frequency division multiplexing.
C-BUS	MX-COM's serial control bus used to communicate digital information between a CPu and a peripheral IC such as the MX802, MX803A, MX805A, MX806A and MX809.
CCIR	International Radio Consultative Committee, a subisdiary organization of the International Telegraphic Union dealing in radio standards (CCIR was recently renamed ITU-T - see ITU-T for more information).
CCITT	The Consultative Committee on International Telegraph and Telephone is an international telecommunications standard agency. It was recently renamed ITU-T (see ITU-T).
CDPD	Cellular Digital Packet Data - an industry standard for data transmission. CDPD utilizes the analog cellular networks already in place in the U.S. and Canada to provide 2-way data communications for users of devices such as laptops and PDAs.
Channel, Voice Grade	A channel with a frequency range of about 300 to 3400 Hz which is suitable for transmission of data or speech in analog form.
CMOS	Complementary Metal-Oxide Semiconductor (an integrated circuit manufacturing process). MX-COM uses both Metal gate CMOS and Silicon gate CMOS processes.

GLOSSARY

CODEC	A single device comprising both an Encoder and a Decoder.
Compander	Acronym for Compressor-Expander, a circuit that compresses the dynamic range of an input signal and expands it almost back to its original form on the output.
Concatenation	Combining multiple data packets or frames in a contiguous series.
Crosstalk	Undesired crossover of voice transmissions from one circuit to another.
CS	Carrier Sense, a logic level supplied by the radio when an RF carrier is detected.
CTCSS	Continuous Tone-Controlled Squelch System: A type of tone coding used in two-way radio systems in which a sub-audible tone, taken from a field of 32 or more in the 67 to 250Hz range, is multiplexed continuously with speech to engage repeaters and allocate traffic among talk groups on shared channels. Trademarked by Motorola as Private Line or PL.
CVSD	Continuously Variable Slope Delta Modulation: A method by which a voice signal is digitized for transmission, and then changed back to the analog voice signal for reception.
DCE	Data Communications Equipment or Data Circuit-Terminating Equipment. This equipment functions to establish and maintain a connection, and provides signal conversion between a terminal and data or telephone line.
DSP	Digital Signal Processing.
DCS/CDCSS	Digital Coded Squelch (similar to CTCSS, but digital). Trademarked by Motorola as Digital Private Line or DPL.
DTMF	Dual Tone Multi-Frequency: a telephone signaling system employing four tones from a low group and three or four from a high group comprising twelve to sixteen unique tone pairs. Radio applications of DTMF should avoid "twist" (differences in level between tone pairs) and time-limit digits to prevent signaling errors caused by fades.
DVSR	Data/Voice Storage & Retrieval, or at MX•COM, INC., Radio MailVox™.
ECPA	Electronic Communications Privacy Act of 1986: This amendment to Section 2510 of title 18, United States Code, established the illegality of intercepting protected (i.e., scrambled) communications.
EIA	Electronics Industry Association: A United States Manufacturer's group which, as part of its function, sets and publishes electronics standards.
Eye Pattern/Eye Diagram	An oscilloscope display of the detector voltage waveform in a modem. The openness of the eye gives a representation of the bit error rate (the more open, the less distortion).
FSK	Frequency Shift Keying: A form of frequency modulation used to transmit two states of a signal as two separate frequencies. FSK is characterized by frequency spacing of 1.
FFSK	Fast Frequency Shift Keying. See MSK.
Full-Duplex	Simultaneous two-way communication.

GLOSSARY

Gaussian Filter	A filter having the symmetrical bell shape of a Gaussian curve (normal distribution).
GMSK	Gaussian Minimum Shift Keying: A type of FSK that uses premodulation Gaussian filtering to achieve high data rates in an FM communication channel bandwidth.
GPS	Global Positioning System.
Half-duplex	Communications in which both transmit and receive occur, but not at the same time.
HSC	Hexadecimal Sequential Coding, a tone signaling protocol comprising 16 tone states. Ten represent decimals 0-9, a NOTONE, a Repeat tone, a Group tone, an address/DATA frame Delineator, plus Reset and Control -- totaling 16 tone-coded logic states. HSC operation is predicated on a decoding technique able to detect tones in random order. These must be contained within a frame preceded and concluded by NOTONE.
	HSC tonesets:
	HSC-A: USA or Metropage™ A Motorola radio paging system employing sequential tones comprising ten decimal and two special function tones ("R" for repeat and "X" as an alternate address) and NOTONE in a predictive code format.
	HSC-C: CCIR toneset. A toneset developed by the International Radio Consultative Committee (see separate listing under CCIR).
	HSC-E: EEA toneset, An EEA (UK) variation of the CCIR HSC toneset in which the lowest frequency tone is 930Hz, and the highest is 2247Hz. Duration is 40ms.
	HSC-Z: The ZVEI German HSC toneset.
	HSC-ZS: SZVEI or Suppressed ZVEI HSC toneset.
IEEE	The Institute of Electrical and Electronics Engineers: one of the functions of this association of engineers is to publish standards defining technical terms.
ITU-T	International Telegraphic Union - Telecommunications (includes the CCITT and CCIR) is an international telecommunications standards agency.
Jitter	Small, abrupt, spurious variations in a waveform due to time, amplitude, frequency or phase.
LMR	Land Mobile Radio System.
LSI	Large-Scale Integration.
LTR™	EF Johnson trademarked trunking system.
MOBITEX	A data transmission protocol developed by Swedish Telecom.
MODEM	Modulator/Demodulator: This is a type of DCE that connects data terminal equipment to a communication line/channel. It converts data to and from the signal form needed for the communication channel.

GLOSSARY

Modulation	The process of modulating a carrier or signal for transmission, also the result of this process.
Monolithic	Constructed from a single crystal or piece of material.
MSK	Minimum Shift Keying: continuous phase FSK modulation (also called FFSK) used to transmit two states of a signal as two separate frequencies using coherent detection and a frequency spacing of 0.5.
Multiplexing	Combining multiple signals for transmission as a group over a single transmission facility.
NMT	Nordic Mobile Telephone is a cellular communications system used primarily in Europe.
PABX	Private Automatic Branch Exchange.
PCM	Pulse Code Modulation: A process in which an analog signal is sampled and converted to a binary code for transmission.
PCMCIA	Personal Computer Memory Card International Association: This association defines and promotes an interchangeable standard for PC memory and expansion cards. The PCMCIA standard applies to 68-pin I/O or interchange type cards.
PDA	Personal Digital Assistant: A handheld computer that provides functions like a notepad or messagepad. PDAs often include data transmission capabilities.
PL	Private Line (a Motorola trademarked name for CTCSS).
PSK	Phase Shift Keying: A form of phase modulation requiring coherent detection. The most straightforward type of PSK shifts the carrier by 0° or 180°.
Psophometric	A weighting curve used to represent the energy density of speech.
PTM/PTL	"Push to Monitor" or "Push to Listen" is a control on two-way portable and mobile radios that allows channel monitoring.
PTT	"Push to talk" is a control on two-way portable and mobile radios that enables transmission.
PSTN	Public Switched Telephone Network.
Pvt SQUELCH	MX-COM's combination of CTCSS and voice inversion to provide voice privacy.
QAM	Quadrature Amplitude Modulation: A hybrid amplitude/phase modulation technique that allows the transmission of four bits of information during a signaling interval, and therefore requires less bandwidth than normal amplitude or phase modulation techniques.
Quick Call II™	A Motorola trademarked 2-Tone sequential signaling format comprising 80 tones arranged in eight tone groups.
R2000	R2000 is a trunked communication system used in France.

GLOSSARY

RD-LAP™	A FM radio data system that operates at 9.6 and 19.2 kbps. (RD-LAP is a trademark of Motorola, Inc.)
Repeater	A device used as an intermediate point in a communications system to receive and retransmit signals, often for the purpose of extending range.
SAT	Supervisory Audio Tone used in cellular systems.
SiGATE	Silicon Gate: a CMOS process used in manufacturing ICs that is smaller and more modern than metal gate.
Simplex	A circuit which can communicate information in one direction only.
SINAD	A ratio of the total output power to the power of noise plus distortion only: $\frac{\text{signal + noise + distortion}}{\text{noise + distortion.}}$
SMD/SMT	Surface Mount Device / Surface Mount Technology.
SMR	Specialized Mobile Radio system.
SS	Spread Spectrum: The spreading of a signal over a wider bandwidth than the minimum required for transmission of the information.
Synchronous transmission	A type of data transmission in which the sending and receiving ends operate continuously at the same frequency and in phase.
TACS/ETACS	Total Access Communication System is a cellular system used in the U.K. ETACS is used in Europe and Japan.
TIA	Telecommunications Industry Association: A United States Manufacturer's group which, as part of its function, sets and publishes telecommunications standards.
Type 99™	A General Electric trademarked 2-Tone sequential format comprising 30 tones.
Trunking	A system sharing communication channels.
VCO	Voltage Controlled Oscillator.
VLSI	Very Large Scale Integration.
VOGAD	Voice Operated Gain Adjusting Device, similar in concept to an AGC (Automatic Gain Control) amplifier, used to ensure full modulation of all speech levels.
VOX	Voice Operated Switching.
VSB	Variable Split Band: A type of high-level analog voice scrambling which splits and inverts the voice band. VSB is utilized in MX•COM's IC and board level products (see MX214/224).

Appendix

Packaging & Handling

The following section gives guidelines for the proper handling of MX•COM integrated circuits.

It also contains illustrations and measurements of MX•COM's package offerings. Both standard and special styles are included.

IC's may be shipped in anti-static tubes, conducting foam, or tape and reel. Tape and reel packaging information begins on page 611.

Handling Precautions for Semiconductor Components

To minimize the risk of ESD-induced device damage, the following handling precautions are strongly recommended:

1) Upon removal from their shipping material (anti-static tubes, conducting foam or tape and reel), CMOS IC's should be placed leads down on a grounded surface. Under no circumstances should they be placed in polystyrene foam or non-conducting plastic.

2) Individuals and tools should be grounded before coming in contact with CMOS IC's.

3) Do not insert or remove devices in sockets with power applied. Ensure that power supply transients, such as occur during power turn-on or off, do not exceed maximum ratings.

4) In the system, all unused inputs must be grounded or otherwise connected to a constant, unvarying input voltage level.

5) After assembly on PC boards, ensure that static discharge cannot occur during handling, storage, or maintenance. Boards may be stored with their connectors surrounded with conductive foam.

Soldering PLCC Packages

1. By hand-held soldering iron or pulse-heated solder tool.
Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300°C.

2. By wave.
Maximum permissable solder temperature is 260°C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150°C within 6 seconds. Typical dwell time is 4 seconds at 250°C.

3. By solder paste reflow.
Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing or pressure-syringe dispensing before device displacement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapor-phase reflow. Dwell times vary between 8 and 60 seconds according to method. Typical reflow temperatures range from 215 to 250°C.

Pre-heating is necessary to dry paste and evaporate binding agent, and to reduce thermal shock on entry to reflow zone.

4. Repairing soldered joints.
The same precautions and limits apply as in (1) above.

Source: Signetics Corp.

NUMBER OF DEVICES SHIPPED PER REEL/TUBE/TRAY

Number of packaged ICs on a reel:

Package Style	Qty.
LH	700
DW-16	1200
DW-24	1200

Number of packaged ICs in a tube:

Package Style	Qty.
LH	45
LH8	28
DW-14	46
DW-16	46
DW-24	30
J-14	25
J-16	25
J-22	18
J-24	15
P-14	25
P-16	25
P-22	18
P-24	15

Number of die in "waffle packs":

Most waffle packs contain 50 components.

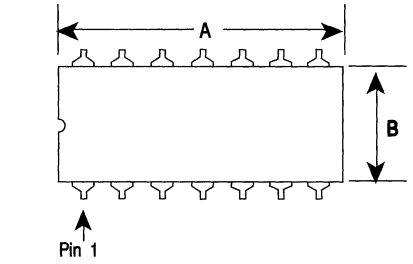
PACKAGE/PRODUCT CROSS-REFERENCE GUIDE

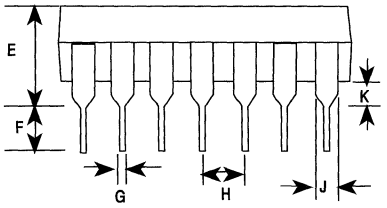
PINS	PRODUCTS	DIMENSIONS
I. PLASTIC DUAL IN-LINE (PDIP)		
14	MX315AP, MX326P, MX613P	p. 599
16	MX105P, MX109P, MX118P, MX128P, MX316P, MX386P, MX623P, MX631P	p. 599
18	MX366P	p. 600
22	MX214P, MX336P, MX406P, MX439P, MX609P	p. 600
24	MX009P, MX014P, MX203Q*P, MX224P, MX346P, MX365AP,	p. 601
28	MX375P, MX709P	p. 601
40	MX939P	p. 602
II. CERAMIC DUAL IN-LINE (CDIP)		
14	MX315AJ	p. 602
16	MX019J, MX029J, MX102J, MX105J, MX109J, MX316J	p. 603
22	MX214J, MX336J, MX406J, MX439J, MX469J, MX609J, MX619J, MX629J	p. 603
24	MX203Q*J, MX803AJ, MX014J, MX224J, MX346J, MX365AJ, MX429J MX529J, MX806AJ, MX009J, MX589J, MX809J, MX909J, MX919J, MX929J	p. 604
28	MX375J, MX709J, MX802J, MX812J, MX816J, MX826J, MX836J	p. 604
III. PLASTIC J-LEADED CHIP CARRIER (PLCC)		
24	MX009LH, MX013Q*LH, MX014LH, MX165BLH, MX165CLH, MX203Q*LH, MX214LH, MX224LH, MX275LH, MX316LH, MX336LH, MX346LH, MX365ALH, MX375LH, MX406LH, MX429LH, MX439LH, MX469LH, MX529LH, MX609LH, MX619LH, MX629LH, MX802LH, MX803ALH, MX805ALH, MX806ALH, MX809LH, MX909LH, MX919LH, MX929LH	p. 605
28	MX375LH8, MX709LH8, MX802LH8	p. 605
IV. SMALL OUTLINE IC (SOIC)		
16	MX019DW, MX029DW, MX102DW, MX109DW, MX118DW, MX128DW, MX315ADW, MX386DW, MX609DW, MX613DW, MX631DW	p. 606
20	MX366DW	p. 606
24	MX165BDW, MX165CDW, MX365ADW, MX439DW, MX469DW, MX589DW, MX641DW, MX806ADW	p. 607
28	MX812DW, MX816DW, MX826DW, MX836DW	p. 607

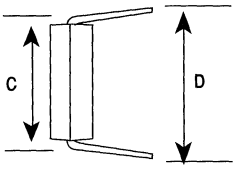
V. SPECIAL PACKAGES

16 Pin Hybrid (MX003Q)	p. 608
16 Pin Dual In-Line Side Braize (MX503)	p. 608
16 Pin Thin Shrink Small Outline Package	p. 609
28 Pin Thin Shrink Small Outline Package	p. 609
48 Pin Thin Quad Flat Pack (MX939TG)	p. 610

14 PIN PLASTIC DUAL IN-LINE "P"



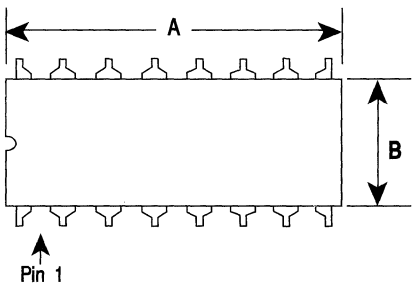


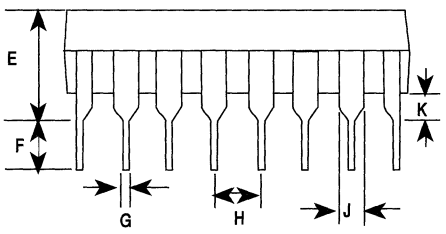


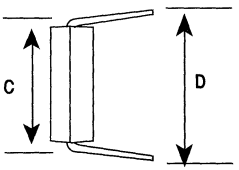
Package Tolerances

Dimension in, (mm)	Min.	Max.
A	.740 (18.796)	.770 (19.558)
B	.240 (6.096)	.260 (6.604)
C	.290 (7.366)	.310 (7.874)
D	.330 (8.382)	.370 (9.398)
E	.150 (3.175)	.200 (5.080)
F	.125 (3.175)	.150 (3.810)
G	.015 (0.381)	.020 (0.508)
H	.090 (2.286)	.110 (2.794)
J	.040 (1.016)	.065 (1.651)
K	.020 (0.508)	.070 (1.778)

16 PIN PLASTIC DUAL IN-LINE "P"





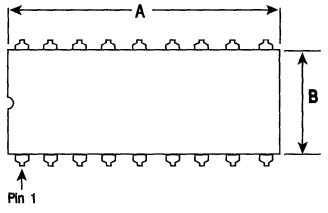


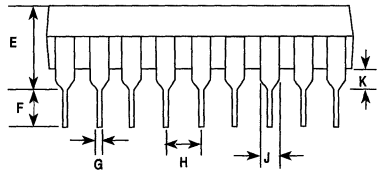
Package Tolerances

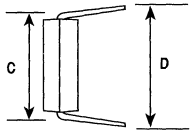
Dimension in, (mm)	Min.	Max.
A	.740 (18.796)	.770 (19.558)
B	.240 (6.096)	.260 (6.604)
C	.290 (7.366)	.310 (7.874)
D	.330 (8.382)	.370 (9.398)
E	.150 (3.175)	.200 (5.080)
F	.125 (3.175)	.150 (3.810)
G	.015 (0.381)	.020 (0.508)
H	.090 (2.286)	.110 (2.794)
J	.040 (1.016)	.065 (1.651)
K	.020 (0.508)	.070 (1.778)

1

18-PIN PLASTIC DUAL IN-LINE "P"



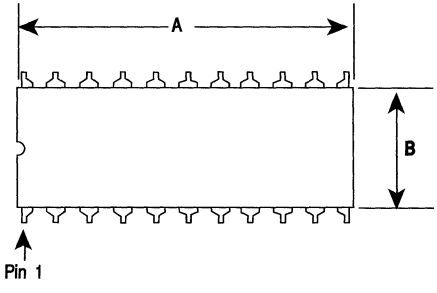


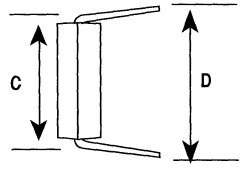


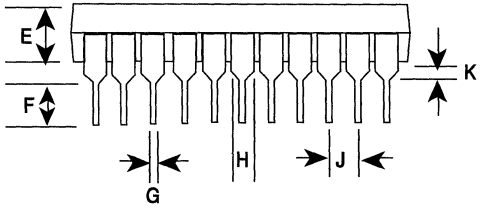
Package Tolerances

Dimension in, (mm)	Min.	Max.
A	.830 (19.1)	.880 (22.35)
B	.240 (6.096)	.260 (6.604)
C	.290 (7.366)	.310 (7.874)
D	.330 (8.382)	.370 (9.398)
E	.150 (3.175)	.200 (5.080)
F	.125 (3.175)	.150 (3.810)
G	.015 (0.381)	.020 (0.508)
H	.090 (2.286)	.110 (2.794)
J	.040 (1.016)	.065 (1.651)
K	.020 (0.508)	.070 (1.778)

22 PIN PLASTIC DUAL IN-LINE "P"



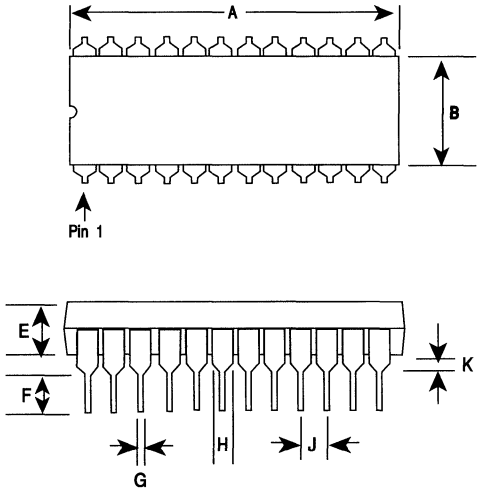


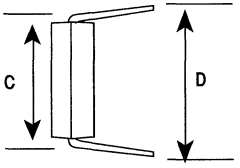


Package Tolerances

Dimension [in. (mm)]	Min.	Max.
A	1.080 (27.432)	1.10 (27.940)
B	0.330 (8.382)	0.360 (8.382)
C	0.390 (9.906)	0.410 (10.414)
D	0.430 (10.922)	0.470 (11.938)
E	0.150 (3.175)	0.200 (5.080)
F	0.125 (3.175)	0.160 (4.064)
G	0.015 (.381)	0.020 (0.508)
H	0.040 (1.016)	0.065 (1.651)
J	0.090 (2.286)	0.110 (2.794)
K	0.020 (0.508)	0.070 (1.778)

24 PIN PLASTIC DUAL IN-LINE "P"

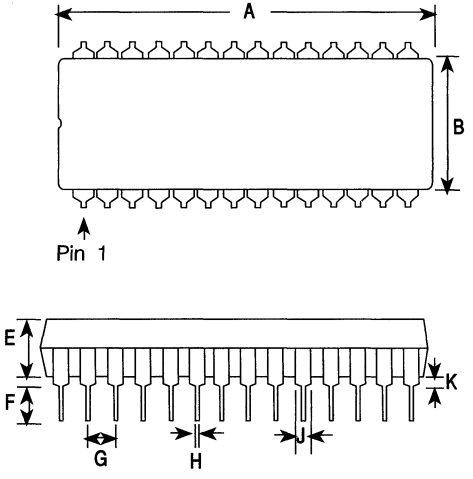


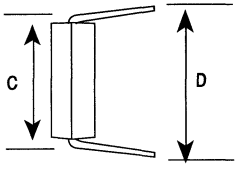


Package Tolerances

Dimension [in. (mm)]	Min.	Max.
A	1.23 (31.24)	1.26 (32.004)
B	0.53 (13.46)	0.55 (13.97)
C	0.59 (14.98)	0.610 (15.49)
D	0.63 (16.002)	0.67 (17.018)
E	0.170 (4.318)	0.220 (5.588)
F	0.125 (3.175)	0.160 (4.064)
G	0.015 (.381)	0.020 (.508)
H	0.040 (1.016)	0.065 (1.651)
J	0.090 (2.286)	0.110 (2.794)
K	0.015 (0.381)	0.065 (.165)

28 PIN PLASTIC DUAL IN-LINE "P"

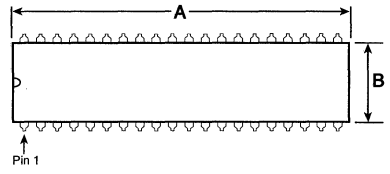


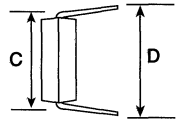


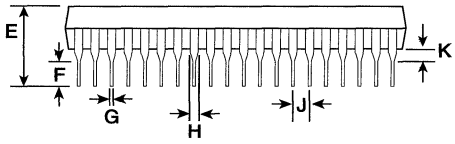
Package Tolerances

Dimension in,(mm)	Min.	Min.
A	1.44 (36.58)	1.47 (37.338)
B	0.530 (13.46)	0.550 (13.970)
C	0.590 (14.986)	0.610 (15.494)
D	0.630 (16.002)	0.670 (17.018)
E	0.170 (4.318)	0.220 (5.588)
F	0.125 (3.175)	0.160 (4.064)
G	0.090 (2.286)	0.110 (2.794)
H	0.015 (0.381)	0.020 (.508)
J	0.040 (1.016)	0.065 (1.651)
K	0.015 (.381)	0.065 (1.651)

40 PIN PLASTIC DUAL IN-LINE "P"



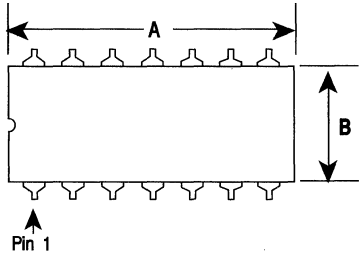


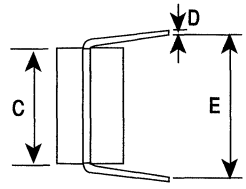


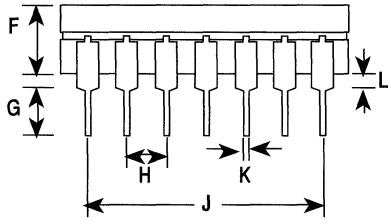
Package Tolerances

Dimension	Min. in. (mm)	Max. in. (mm)
A	2.04 (51.82)	2.06 (52.32)
B	.53 (13.46)	.55 (13.97)
C	.595 (15.11)	.625 (15.88)
D	.600 (15.24)	.660 (16.76)
E	-----	.310 (7.87)
F	.128 (3.25)	-----
G	.018 (.457)	typical
H	.050 (1.27)	typical
J	.100 (2.54)	typical
K	.015 (0.381)	-----

14 PIN CERAMIC DUAL IN-LINE "J"





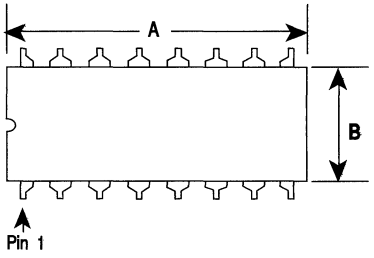


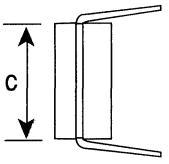
Package Tolerances

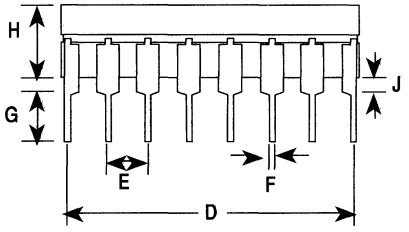
Dimension in,(mm)	Min.	Max.
A	.754 (19.15)	.766 (19.45)
B	.24 (6.22)	.25 (6.38)
C	.31 (7.75)	.315 (8.00)
D	.0098 (.25)	typical
E	.38 (9.65)	.42 (10.67)
F	.161 (4.10)	typical
G	.199 (5.06)	typical
H	.10 (2.54)	typical
J	.60 (15.24)	typical
K	.018 (.46)	typical
L	.015 (.38)	typical

10

16 PIN CERAMIC DUAL IN-LINE "J"



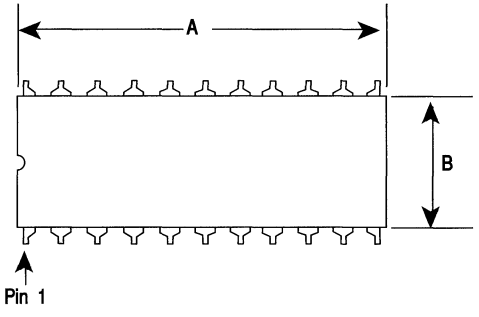


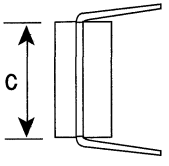


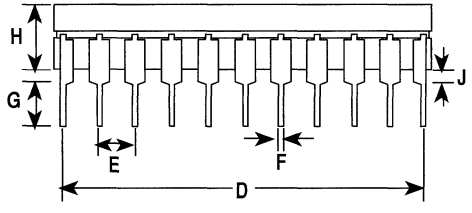
Package Tolerances

Dimension in,(mm)	Min.	Max.
A	.753 (19.12)	.767 (19.48)
B	.285 (7.24)	.290 (7.40)
C	.30 (7.80)	.31 (8.00)
D	.70 (17.78)	typical
E	.10 (2.54)	typical
F	.018 (0.46)	typical
G	.153 (3.89)	typical
H	.168 (4.27)	typical
J	.020 (0.50)	-------

22 PIN CERAMIC DUAL IN-LINE "J"



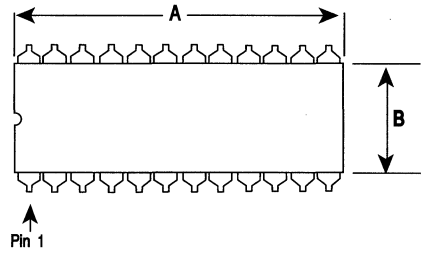


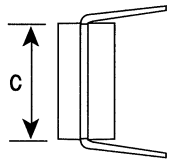


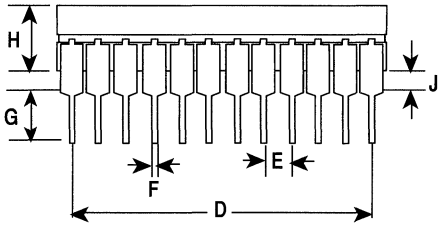
Package Tolerances

Dimension in,(mm)	Min.	Max.
A	1.06 (26.98)	1.08 (27.38)
B	0.376 (9.55)	0.384 (9.75)
C	0.410 (10.40)	0.417 (10.60)
D	0.996 (25.30)	1.00 (25.50)
E	0.10 (2.54)	typical
F	0.018 (0.46)	typical
G	0.171 (4.35)	typical
H	0.157 (3.99)	0.170 (4.27)
J	0.020 (0.50)	-------

24 PIN CERAMIC DUAL IN-LINE "J"



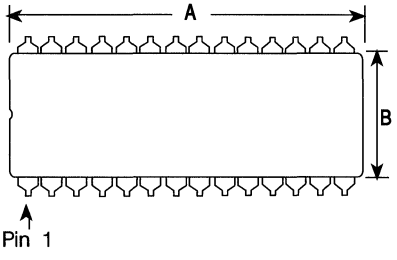


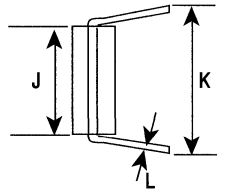


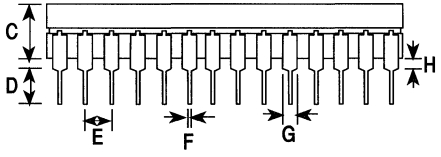
Package Tolerances

Dimension [in. (mm)]	Min.	Max.
A	1.24 (31.50)	1.26 (32.03)
B	0.514 (13.06)	0.583 (14.81)
C	0.60 (15.14)	0.615 (15.61)
D	1.10 (27.84)	1.11 (28.04)
E	.100 (2.54)	typical
F	.018 (0.46)	typical
G	.171 (4.35)	typical
H	.171 (4.35)	.196 (4.99)
J	.020 (0.50)	--------

28 PIN CERAMIC DUAL IN-LINE "J"





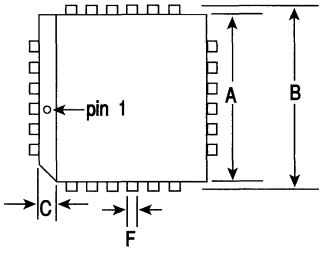


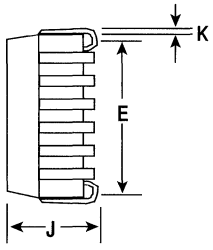
Package Tolerances

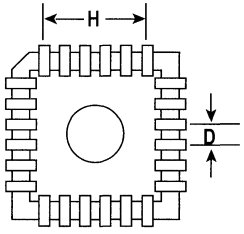
Dimension in,(mm)	Min.	Max.
A	1.44 (36.58)	1.46 (37.05)
B	0.51 (13.06)	0.53 (13.36)
C	0.18 (4.49)	0.220 (5.57)
D	0.12 (3.0)	0.15 (3.81)
E	0.10 (2.54)	typical
F	0.018 (0.45)	typical
G	0.055 (1.39)	typical
H	0.02 (.50)	0.05 (1.30)
J	0.61 (15.50)	0.62 (15.70)
K	0.670 (17.0)	typical
L	0.009 (0.25)	typical

10

24 LEAD PLASTIC LEADED CHIP CARRIER "LH"



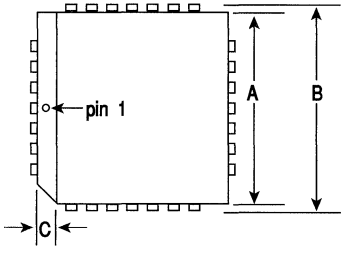


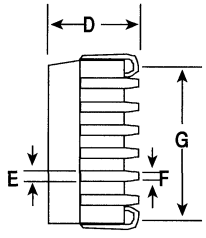


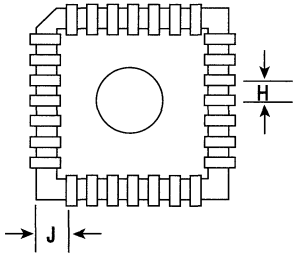
Package Tolerances

Dimension in,(mm)	Min.	Max.
A	.382 (9.7)	.410 (10.40)
B	.417 (10.60)	.435 (11.05)
C	.045 (1.15)x45°	typical
D	.050 (1.27)	typical
E	.366 (9.30)	typical
F	.018 (0.45)	.022 (.55)
H	.250 (6.35)	typical
J	.128 (3.25)	.146 (3.70)
K	.007 (.17)	.011 (.27)

28 LEAD PLASTIC LEADED CHIP CARRIER "LH8"



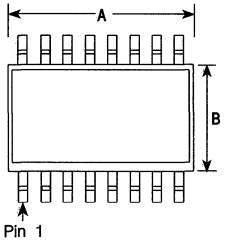


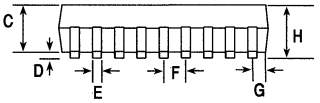


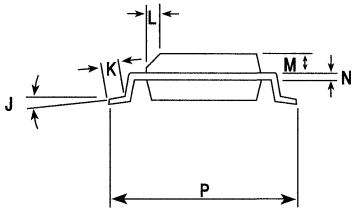
Package Tolerances

Dimension in,(mm)	Min.	Max.
A	.450 (11.43)	.453 (11.51)
B	.485 (12.32)	.495 (12.57)
C	.045x45°	typical
D	.165 (4.20)	.180 (4.57)
E	.026 (0.66)	.030 (0.76)
F	.017 (0.43)	.021 (0.53)
G	.410 (10.41)	.430 (10.92)
H	.050 (1.27)	typical
J	.070 (1.78)	.085 (2.16)

16-PIN SMALL OUTLINE INTEGRATED CIRCUIT "DW"



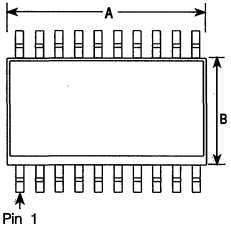


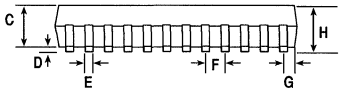


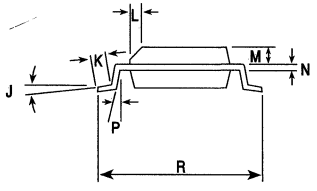
Package Tolerances

Dimension in,(mm)	Min.	Max.
A	0.398 (10.11)	0.406 (10.31)
B	0.291 (7.39)	0.299 (7.59)
C	0.092 (2.33)	typical
D	0.004 (0.102)	0.012 (0.304)
E	0.014 (0.36)	0.018 (0.46)
F	0.050 (1.27)	typical
G	0.026 (0.66)	typical
H	0.096 (2.43)	0.104 (2.64)
J	5°	typical
K	0.020 (0.51)	0.040 (1.02)
L	0.025 (0.63)	typical
M	0.041 (1.04)	typical
N	0.009 (0.23)	0.011 (0.28)
P	0.39 (9.91)	0.414 (10.51)

20-PIN SMALL OUTLINE INTEGRATED CIRCUIT "DW"



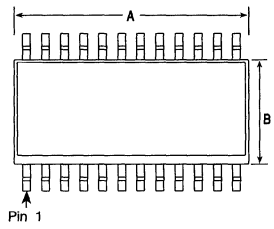


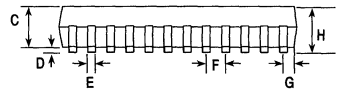


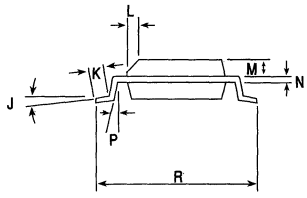
Package Tolerances

Dimension in,(mm)	Min.	Max.
A	0.496 (12.62)	0.506 (12.87)
B	0.291 (7.39)	0.299 (7.59)
C	0.092 (2.33)	typical
D	0.004 (0.102)	0.012 (0.304)
E	0.014 (0.36)	0.018 (0.46)
F	0.050 (1.27)	typical
G	0.026 (0.66)	typical
H	0.096 (2.43)	0.104 (2.64)
J	5°	typical
K	0.020 (0.51)	0.040 (1.02)
L	0.025 (0.63)	typical
M	0.041 (1.04)	typical
N	0.009 (0.23)	0.011 (0.28)
P	5°	typical
R	0.39 (9.91)	0.414 (10.51)

24-PIN SMALL OUTLINE INTEGRATED CIRCUIT "DW"



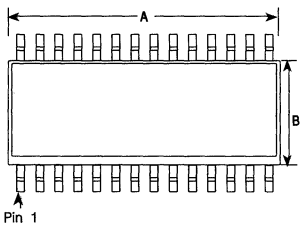


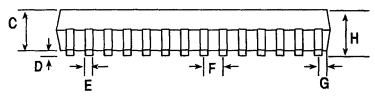


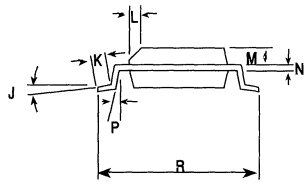
Package Tolerances

Dimension in,(mm)	Min.	Max.
A	0.598 (15.19)	0.606 (15.41)
B	0.291 (7.39)	0.299 (7.59)
C	0.092 (2.33)	typical
D	0.004 (0.102)	0.012 (0.304)
E	0.014 (0.36)	0.018 (0.46)
F	0.050 (1.27)	typical
G	0.026 (0.66)	typical
H	0.096 (2.43)	0.104 (2.64)
J	5°	typical
K	0.020 (0.51)	0.040 (1.02)
L	0.025 (0.63)	typical
M	0.041 (1.04)	typical
N	0.009 (0.23)	0.011 (0.28)
P	5°	typical
R	0.39 (9.91)	0.414 (10.51)

28-PIN SMALL OUTLINE INTEGRATED CIRCUIT "DW"



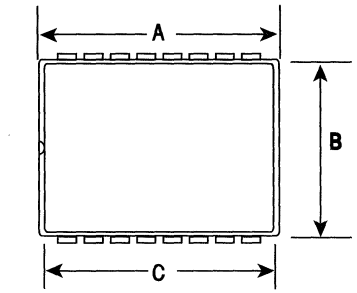


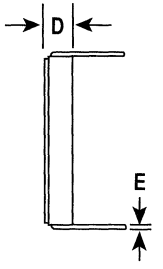


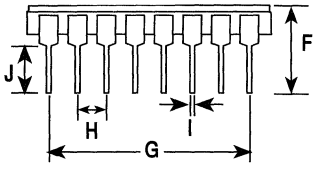
Package Tolerances

Dimension in,(mm)	Min.	Max.
A	0.698 (17.72)	0.706 (17.97)
B	0.291 (7.39)	0.299 (7.59)
C	0.092 (2.33)	typical
D	0.004 (0.102)	0.012 (0.304)
E	0.014 (0.36)	0.018 (0.46)
F	0.050 (1.27)	typical
G	0.026 (0.66)	typical
H	0.096 (2.43)	0.104 (2.64)
J	5°	typical
K	0.020 (0.51)	0.040 (1.02)
L	0.025 (0.63)	typical
M	0.041 (1.04)	typical
N	0.009 (0.23)	0.011 (0.28)
P	5°	typical
R	0.39 (9.91)	0.414 (10.51)

16 LEAD DUAL IN-LINE HYBRID



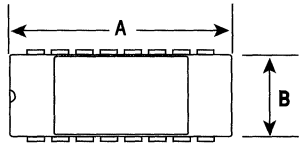


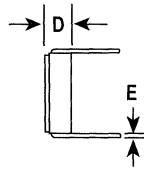


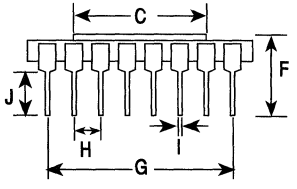
Nominal Package Dimensions

Dimension	in. (mm)
A	.80 (20.32)
B	.59 (15.0)
C	.77 (19.56)
D	.11 (2.79)
E	.01 (0.25)
F	.30 (7.62)
G	.70 (17.78)
H	.10 (2.54)
I	.018 (0.46)
J	.155 (3.94)

16 LEAD DUAL IN-LINE SIDE-BRAIZE



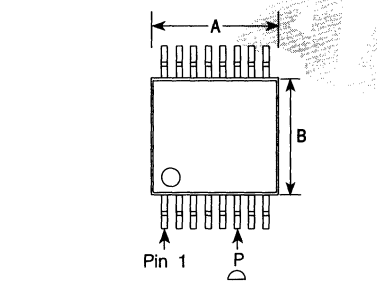


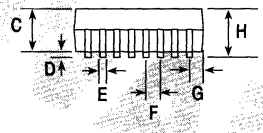


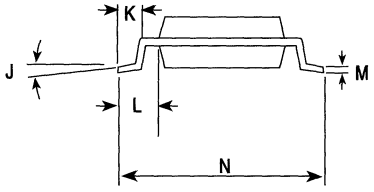
Nominal Package Dimensions

Dimension	in. (mm)
A	.81 (20.6)
B	.30 (7.60)
C	.5 (12.7)
D	.11 (2.79)
E	.01 (0.25)
F	.26 (6.6)
G	.70 (17.78)
H	.10 (2.54)
I	.018 (0.46)
J	.13 (3.3)

16-PIN THIN SHRINK SMALL OUTLINE PACKAGE "TS"



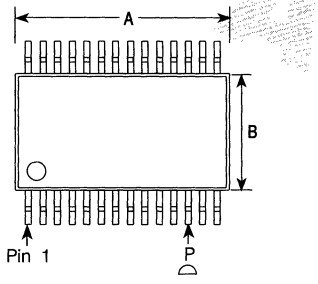


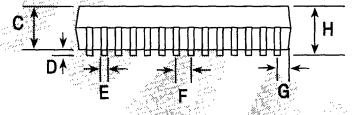


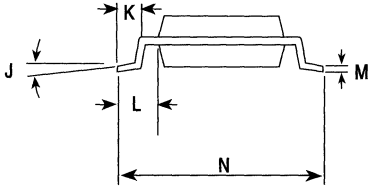
Package Tolerances

Dimension in,(mm)	Min.	Max.
A	0.240 (6.11)	0.256 (6.51)
B	0.295 (7.49)	0.305 (7.75)
C	0.035 (0.90)	0.043 (1.10)
D	0.0004 (0.01)	0.006 (0.15)
E	0.0086 (0.22)	0.015 (0.38)
F	0.0256 (0.65)	typical
G	0.037 (0.95)	typical
H	--------	0.047 (1.20)
J	5°	typical
K	0.014 (0.35)	0.0256 (0.65)
L	0.024 (0.60)	0.039 (1.00)
M	0.0047 (0.12)	0.0062 (0.16)
N	0.355 (9.02)	0.371 (9.42)
P	0.00	0.004 (0.10)

28-PIN THIN SHRINK SMALL OUTLINE PACKAGE "TS"



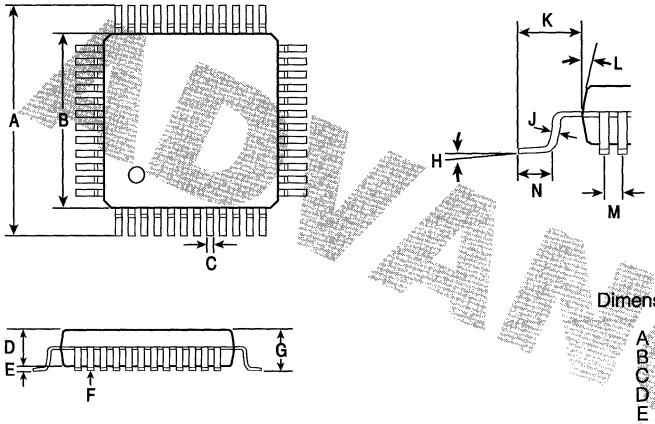




Package Tolerances

Dimension in,(mm)	Min.	Max.
A	0.394 (10.01)	0.410 (10.41)
B	0.295 (7.49)	0.305 (7.75)
C	0.035 (0.90)	0.043 (1.10)
D	0.0004 (0.01)	0.006 (0.15)
E	0.0086 (0.22)	0.015 (0.38)
F	0.0256 (0.65)	typical
G	0.037 (0.95)	typical
H	--------	0.047 (1.20)
J	5°	typical
K	0.014 (0.35)	0.0256 (0.65)
L	0.024 (0.60)	0.039 (1.00)
M	0.0047 (0.12)	0.0062 (0.16)
N	0.355 (9.02)	0.371 (9.42)
P	0.00	0.004 (0.10)

48 PIN THIN QUAD FLAT PACKAGE "TG"



Package Tolerances

Dimension	Min. in. (mm)	Max. in. (mm)
A	.346 (8.8)	.362 (9.2)
B	.272 (6.9)	.280 (7.1)
C	.005 (0.11)	.011 (0.27)
D	.053 (1.35)	.057 (1.45)
E	.002 (0.05)	.006 (0.15)
F	.003 (0.08)	typical
G	———	.063 (1.6)
H	0°	7°
J	.004 (0.09)	.008 (0.20)
K	.040 (1.0)	ref.
L	12°	typical
M	.020 (0.50)	typical
N	.014 (0.35)	.026 (0.65)

0

MX-COM Tape and Reel Specifications

1. Scope

The specification relates to the tape packaging of integrated circuits suitable for use in "surface mount" assembly. It includes only those dimensions which are essential for the purchaser to use the product.

2. Dimensions (Refer to Figure 1)

2.1 Tape Width	LG, LH, DW-24		W = 24 ± 0.3 mm
	DW-16		W = 16 ± 0.3 mm
2.2 Carrier Tape Thickness	DW-16, DW-24		t = 0.3 mm max.
	LG, LH		t = 0.3 ± 0.05 mm
2.3 Pitch of Sprocket Holes			Po = 4.0 ± 0.1 mm
2.4 Diameter of Sprocket Holes	DW-16, DW-24		D = 1.5 + 0.5 mm = 1.5 - 0.0 mm
	LG, LH		D = 1.5 + 0.1 mm
2.5 Distance			E = 1.75 ± 0.1 mm
2.6 Distance, center to center	LG, LH, DW-24		F = 11.5 ± 0.1 mm
	DW-16		F = 7.7 ± 0.1 mm
2.7 Dimension, center of pocket to center of divider			
2.7.1		LG	P2 = 10 ± 0.1 mm
2.7.2		LH	P2 = 8 ± 0.1 mm
2.7.3		DW-16	P2 = 6 ± 0.1 mm
2.7.4		DW-24	P2 = 6 ± 0.1 mm
2.8 Embossed Pocket Dimension Ao and Bo			
2.8.1		LG	Ao = 15.8 ± 0.1 mm
2.8.2		LG	Bo = 15.8 ± 0.1 mm
2.8.3		LH	Ao = 11.5 ± 0.1 mm
2.8.4		LH	Bo = 11.5 ± 0.1 mm
2.8.5		DW-16	Ao = 10.9 ± 0.1 mm
2.8.6		DW-16	Bo = 10.7 ± 0.1 mm
2.8.7		DW-24	Ao = 10.9 ± 0.1 mm
2.8.8		DW-24	Bo = 16.0 ± 0.1 mm
2.9 Embossed Tape Dimension K			
2.9.1		LG	K = 2.9 ± 0.1 mm
2.9.2		LH	K = 4.1 ± 0.1 mm
2.9.3		DW-16	K = 3.0 ± 0.1 mm
2.9.4		DW-24	K = 3.0 ± 0.1 mm
2.10 Pitch of Component Compartments			
2.10.1		LG	P = 20 ± 0.1 mm
2.10.2		LH	P = 16 ± 0.1 mm
2.10.3		DW-16	P = 12 ± 0.1 mm
2.10.4		DW-24	P = 12 ± 0.1 mm

2.11 Outside Dimension of Pocket

2.11.1	LG	B1 = 16.5 ± 0.2 mm
2.11.2	LH	B1 = 12.4 ± 0.1 mm
2.11.3	DW-16	B1 = 11.3 ± 0.1 mm
2.11.4	DW-24	B1 = 16.2 ± 0.1 mm

2.12 Pocket Center Holes

2.12.1	LG	D1 = 1.55 +1.0/-0.05 mm
2.12.2	LH	D1 = 1.55 +1.0/-0.05 mm
2.12.3	DW-16	D1 = 2.0 mm min
2.12.4	DW-24	D1 = 2.0 mm min

3. Polarity and Orientation of Components in Tape

3.1 All components will be placed so that Pin 1 is adjacent to the sprocket holes. (See Fig. 6.)

3.2 The mounting side of the component will be oriented to the bottom side of the tape. (See Fig. 2.)

4. Fixing of Components in Tape

4.1 Cover tapes will not cover the sprocket holes.

4.2 Tapes in adjacent layers will not stick together in the packing.

4.3 The adhesive of the cover tape will not adversely effect the mechanical and electrical characteristics and marking of the components.

4.4 Components will not stick to the carrier tape or the cover tape.

4.5 The tapes will be suitable to withstand storage of the taped components without danger or migration of the terminations or the giving off of vapors which would impair soldering or deteriorate the component properties or termination by chemical action.

4.6 When the tape is bent with a minimum radius (See Fig. 5) of 30 mm, the tape shall not be damaged and the components shall remain in their position and orientation in the tape.

4.7 Carrier tape will be conductive.

4.8 Cover tape will be anti-static.

4.9 The peel strength of the cover tape will be 70 + 40 grams measured at 175° to 180° with respect to the carrier tape along its longitudinal axis. The peel speed will be 240mm/min.

4.10 After baking at 60° for 24 hours or storage in ideal condition for two months, the peel strength shall remain within the specified limits.

5. Packaging

5.1 Tape will be wound on plastic reels (See Fig. 4).

	Dimensions				
	A	C	N	W1	W2
5.1.1	330mm	12.7mm	62.5mm	24.5mm	28.8mm
5.1.2	180mm	12.7mm	62.5mm	24.5mm	28.8mm

5.2 There will be a leader of 230mm min. followed by a minimum of 40 empty compartments at the start of each carrier tape (See Fig. 3).

5.3 There will be no missing components between the first and last part of working tape in any reel.

5.4 At the end of the tape there will be a trailer of a minimum of 75 empty compartments (cover tape sealed). (See Fig. 3.)

5.5 The tape will release from the reel hub as the last portion of the carrier tape unwinds from the reel.

5.6 Components on a reel.

		13"
5.6.1	LG	700
5.6.2	LH	700
5.6.3	DW-16	1200
5.6.4	DW-24	1200

5.7 The tape will be prevented from unreeling by winding a paper tape around the reel and fixing with adhesive tape.

5.8 All reels will display the following:
- Manufacturer's device type number
- Quantity on reel
- Date code
- A static hazard warning label

5.9 Ideal storage conditions are 15° to 20°C with a relative humidity of 60-70%.

6.0 Maximum estimated shelf life when stored as above: 6 months.

Package Types
LG: 24-lead Plastic Gull Wing Package
LH: 24-lead Plastic Leaded Chip Carrier (PLCC)
DW-16: 16-lead Small Outline IC (SOIC)
DW-24: 24-lead Small Outline IC (SOIC)

Embossed Carrier Dimensions

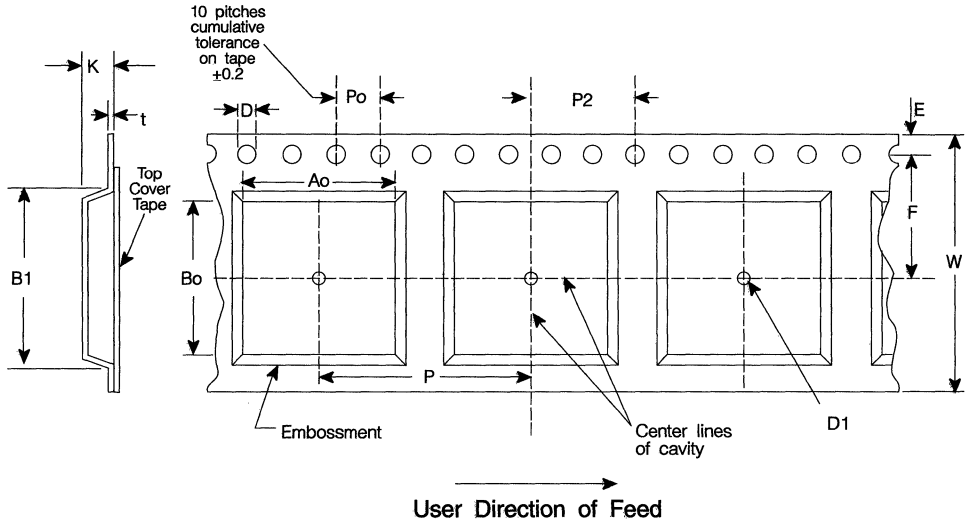


Figure 1

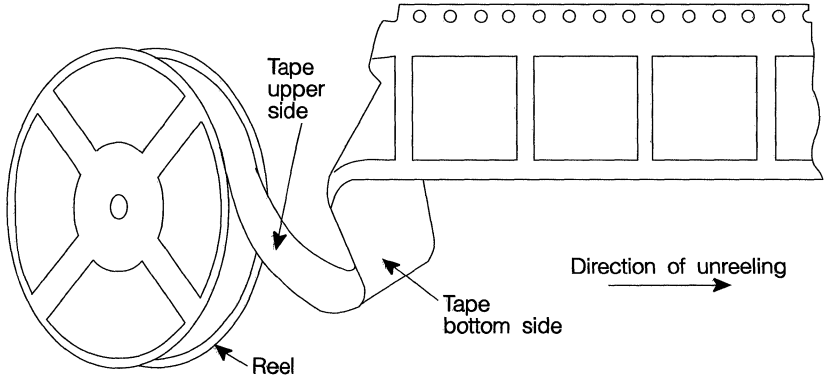


Figure 2 - Tape Top and Bottom Orientation

10

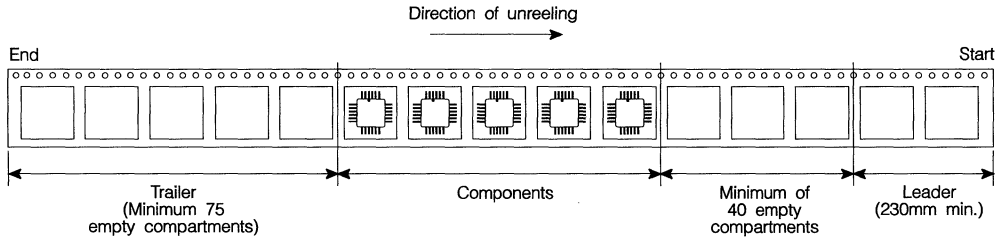


Figure 3 - Layout of Tape

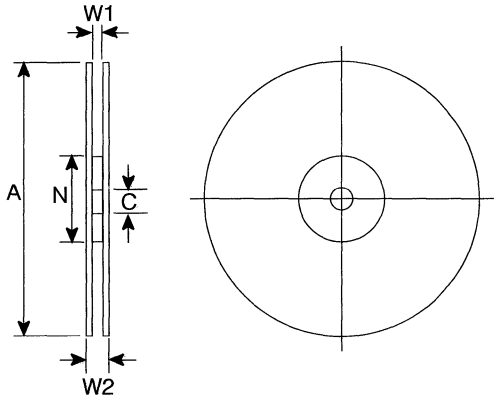


Figure 4 - Reel Dimensions

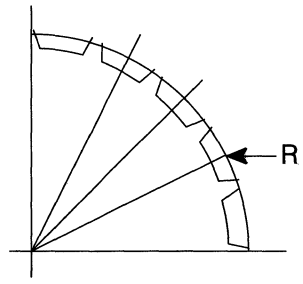
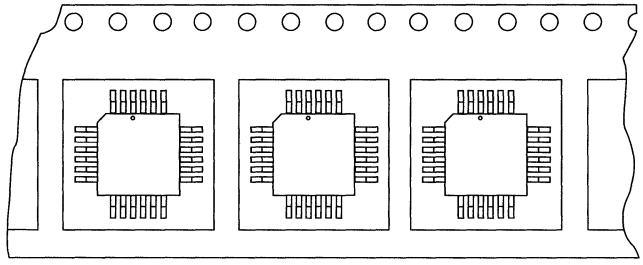
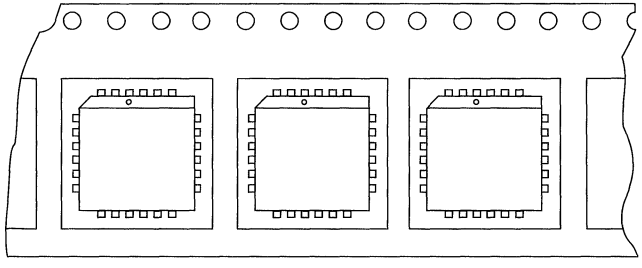


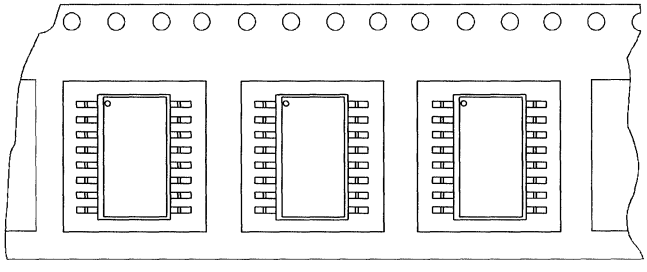
Figure 5 - Minimum Radius = 30mm.



LG Package User direction of feed



LH Package User direction of feed



DW Package User direction of feed

Figure 6 - Component Orientation

REPLACEMENT PRODUCT GUIDE

Device	Description	2-Way Mobile Radio	Cellular Phones	Cordless Phones	Telephony	Wireless Modems	Paging	Voice Security	General Purpose	Recommended Replacement
MX003	Selective Call Tone Decoder	✔								MX203/803A
MX004	Voice Band Inverter	✔								MX014
MX103	Address Selector	✔					✔			
MX165	CTCSS Encoder/Decoder with Audio Filter	✔				✔				MX165C
MX205	Tone Generator								✔	MX805A
MX265	CTCSS Encoder/Decoder	✔								MX165C
MX313/323	MUX/Display Driver	✔					✔			
MX315	CTCSS Encoder	✔				✔				MX315A
MX326	Audio Bandpass Filter								✔	
MX335	CTCSS Encoder/Decoder	✔				✔				MX165C/805
MX355	CTCSS Encoder/Decoder	✔				✔				MX165C
MX365	CTCSS Encoder/Decoder	✔				✔				MX165C
MX403	Sequential Tone Transponder	✔					✔			
MX409	1200 bps MSK Modem	✔	✔			✔				MX469
MX419/519	1200 bps MSK Modem	✔	✔			✔				MX469
MX489	19.2 k bps GMSK Modem	✔	✔			✔				MX589
MX611	SPM Detector				✔					MX631
MX621	Low-Power SPM Detector				✔					MX631
MX803	Audio Signaling Processor	✔			✔					MX803A
MX805	Sub-Audio Signaling Processor	✔								MX805A
MX806	Audio Processor	✔								MX806A

Manufacturers of Compatible Xtals for use with MX-COM IC's

This is not a complete list of xtal manufacturers, but it should provide a few sources for xtals that can be used with MX•COM ICs.

CTS Corporation
1201 Cumberland Ave.
West Lafayette, IN 47906
Phone: 317-463-2565

Ecliptek Corporation
3545-B Cadillac Ave.
Costa Mesa, CA 92626-1401
Phone: 714-433-1200

Relm Communications
7707 Records St.
Indiannapolis, IN 46226
Phone: 800-228-8108

INDEX BY PART NUMBER

MX009	Octal Digital Control Amplifier	p. 449
MX013	HSC Tone Decoder	p. 229
MX014	Voice Band Inverter	p. 345
MX019	Quad Digital Control Amplifier	p. 455
MX029	Dual Digital Control Amplifier	p. 460
MX102	Autocorrelator	p. 503
MX105	Tone Detector	p. 509
MX109	Full Duplex CVSD Codec with Serial Control	p. 377
MX118	Full-Duplex Scrambler for Cordless Telephones	p. 360
MX128	Full-Duplex Scrambler for Cordless Telephones	p. 366
MX165B	CTCSS Encoder/Decoder with Audio Filter	p. 160
MX165C	CTCSS Encoder/Decoder with Audio Filter	p. 169
MX203	Selective Call Codec	p. 234
MX214	VSB Inverter	p. 351
MX224	VSB Inverter	p. 351
MX275	Pvt SQUELCH™ CTCSS Encoder/Decoder	p. 187
MX315A	CTCSS Encoder	p. 155
MX316	NMT Audio Filter Array	p. 267
MX336	Audio/Subaudio Filter Array	p. 272
MX346	Cellular Audio Processing Array	p. 278
MX365A	CTCSS Encoder/Decoder with Audio Filter	p. 178
MX366	Quad Filter Array (NAMPS/ETACS)	p. 285
MX375	Pvt SQUELCH™ CTCSS Encoder/Decoder	p. 195
MX386	Quad Filter Array (NAMPS/TACS/AMPS/ACSB)	p. 291
MX429	1200 bps MSK Modem with Parallel BUS Control	p. 15
MX439	1200 bps MSK Modem with Serial Control	p. 29
	An RS-232 Asynchronous Modem using the MX439	p. 567
MX469	1200/2400 bps MSK Modem with Serial Control	p. 35
MX503	Sequential Tone Encoder	p. 242
MX529	1200 bps MSK Modem with Parallel BUS Control	p. 15
MX589	40k bps GMSK Modem with Serial Control	p. 43
MX609	Full Duplex CVSD Codec with Companding	p. 384
	An Audio Delay Circuit Based on the MX609	p. 558
MX613	Global Call Progress Detector	p. 469
MX619	Delta Modulation Codec	p. 391
MX629	Delta Modulation Codec	p. 391
MX623	Line-Powered Call Progress Detector	p. 477
MX631	Low-Power SPM Detector	p. 483
MX641	Dual SPM Detector	p. 490

MX709	Voice Storage and Retrieval (VSR) Codec w/ SRAM	p. 403
MX802	Full Duplex VSR Codec with DRAM Control	p. 420
MX812	Half Duplex VSR Codec with DRAM Control	p. 434
MX803A	Audio Signaling Processor	p. 249
MX805A	Sub-Audio Signaling Processor	p. 204
MX806A	Audio Processor	p. 295
MX809	1200 bps MSK Modem with C-BUS Control	p. 57
MX816	NMT Audio Processor	p. 307
MX826	AMPS/NAMPS Audio Processor	p. 319
MX836	R2000 Audio Processor	p. 331
MX909	High-Speed and MOBITEX GMSK Modem	p. 70
MX919	High-Speed 4-Level FSK Modem/ARDIS	p. 103
MX929	High-Speed 4-Level FSK Modem/ARDIS	p. 103
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HSC Product Overview ..... p. 223
Packaging and Handling ..... p. 591
Product Replacement Guide ..... p. 617
Pvt SQUELCH: Combining CTCSS with Voice Band Inversion ..... p. 534
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Variable Split Band Scrambling ..... p. 543
Wireless Data Modems: Getting the Best Performance ..... p. 562
Wireless Modem Guide ..... p. 14
Xtals Compatible with MX-COM ICs ..... p. 619

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Room #1301-1, Yoido Department Store Bldg.
36-2, Yoido Dong, Yeongdeungpo-Ku
Seoul, 150-010, Korea
Phone: (02) 784-6800
Fax: (02) 784-8600
Telex: K23456 STECI

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Phone: (02) 709-7626
Fax: (02) 755-3394

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Fax: (852) 710-9220
Telex: 38513 TEKHL HX

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Fax: 61-3-808-5473

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Fax: (972) 3-498745

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TEKSEL CO., LTD.
TBC, Higashi 2-27-10
Shibuya-ku, Tokyo 150 Japan
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Fax: (03) 5467-0777

Osaka Office
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Suita-shi, Osaka-fu 564 Japan
Phone: (06) 368-9000
Fax: (06) 368-8880

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Nichiei-Ohkusu Bldg., 3F
2-6-9 Ohkusu, Minami-ku
Fukuoka-shi,
Fukuoka-ken 815 Japan
Phone: (092) 524-6401
Fax: (092)524-6566

Nagano Office
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2-1-22 Tenjin, Ueda-shi,
Nagano-ken 386 Japan
Phone: (0268) 23-7411
Fax: (0268) 23-7412

Nagoya Office
Wakayama Bldg.,
1-8-11 Ikeshita, Chikusa-ku,
Nagoya-shi, Aichi-ken 464 Japan
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Fax: (052) 761-9883

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Rolling Meadows, IL 60008 USA
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Huntington, NY 11743 USA
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Fax: (516) 673-2848

■ In Northwest USA
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Lake Oswego, OR 97034 USA
Phone: (503) 697-7768
Fax: (503) 697-7764

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Mountlake Terrace, WA 98043 USA
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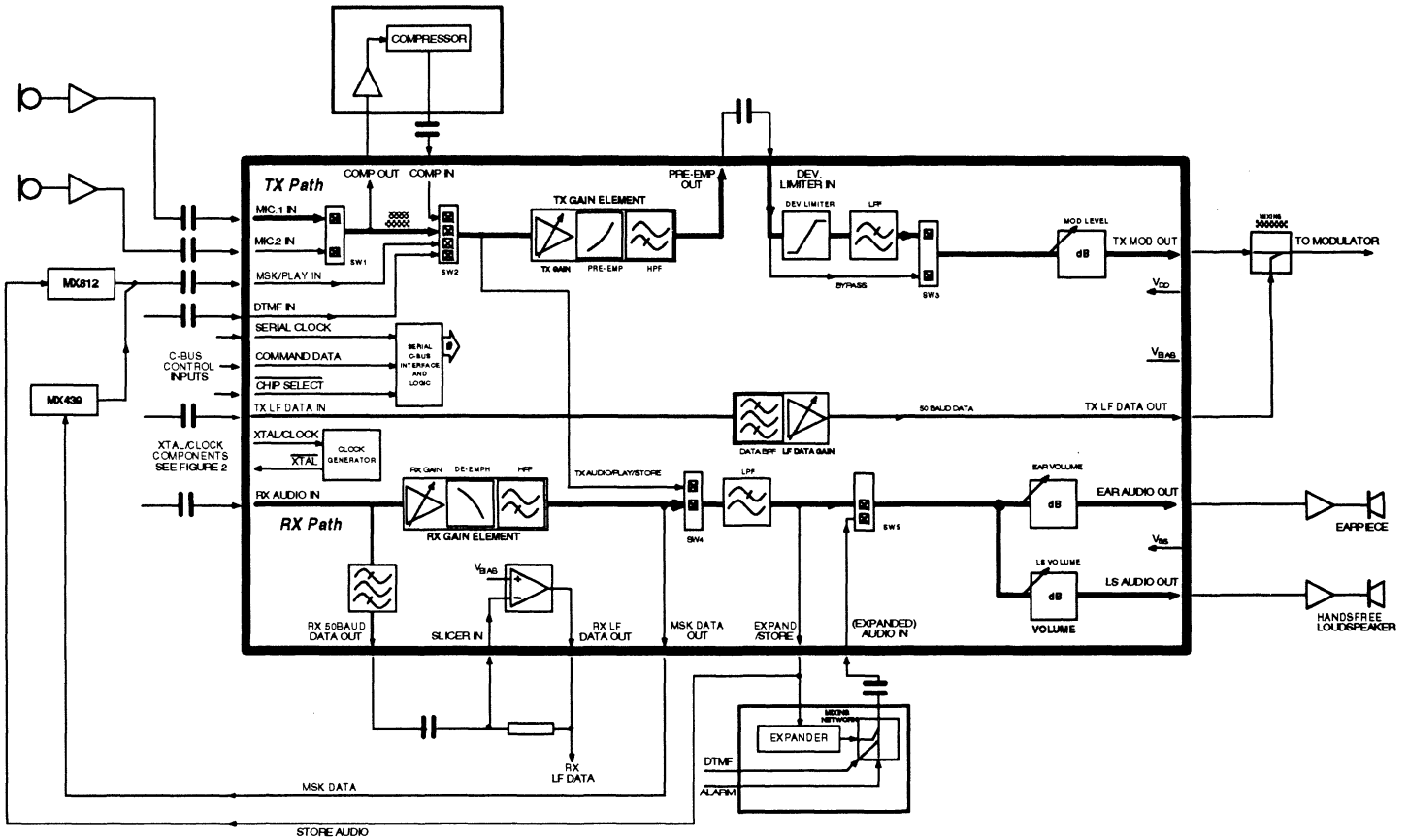

Figure 4 - The MX836 Within an R2000 Cellular System

The Controlling System

C-BUS is designed for low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software. It may be used with any µController, and can, if desired, take advantage of the hardware and serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data rate is determined solely by the µController, the system designer has complete freedom to choose a µController appropriate to the overall system processing requirements.

Control of the functions and levels within the MX836 R2000 Audio Processor is by a group of Address/Commands and appended data instructions from the system microcontroller. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Hex.	Address/Command Binary MSB LSB		Command Data	Table
General Reset	01	0 0 0 0 0 0 0 1			
Configuration Command	10	0 0 0 1 0 0 0 0	+	1 byte	2
TX Gain & Mod. Command	11	0 0 0 1 0 0 0 1	+	1 byte	3
RX Gain & LS Vol.	12	0 0 0 1 0 0 1 0	+	1 byte	4
LF Data Gain & Ear Vol.	13	0 0 0 1 0 0 1 1	+	1 byte	5

Table 1 - C-BUS Address/Commands

In C-BUS protocol the MX836 is allocated Address/Command values 10_H to 13_H. Configuration, TX/RX Gains, and SAT/Powersave assignments and data requirements are given in Table 1.

Each instruction consists of an Address/Command (A/C) byte followed by a data instruction formulated from the following tables.

Commands and Data are only to be loaded in the group configurations detailed, as the C-BUS interface recognized the first byte after $\overline{\text{Chip Select}}$ (logic 0) as an Address/Command. Function or Level control data, which is detailed in Tables 2, 3, 4, and 5, is acted upon at the end of the loaded instruction. See Timing Diagrams, Figures 5 and 6.

Upon power-up the value of the "bits" in this device will be random (either "0" or "1"). A General Reset Command (01_H) is required to set all MX816 registers to 00_H.

Configuration Command *(Preceded by A/C 10_H)*

Setting		Control Bits
(MSB)		*Transmitted First*
Bit 7		**RX Gain Element**
0		Powersave
1		Enable
6		**All Functions** (except RX Gain Element)
0		Powersave
1		Enable
5		**SW5 Expander**
0		Expander Bypass
1		Expander Route
4		**SW4 TX/RX Audio**
0		TX Store/Audio
1		RX Store/Audio
3		**SW3 Dev. Limiter**
0		Dev. Limiter Bypass
1		Dev. Limiter Route
2		**SW1 Mic. Inputs**
0		Mic. 1 Input
1		Mic. 2 Input
1	*0*	**SW2 TX Function**
0	0	DTMF In
0	1	Compressor In
1	0	Compressor Bypass
1	1	MSK/Play In

Table 2 - Configuration Commands

TX Gain & Mod. Command *(Preceded by A/C 11_H)*

Setting				Gain (dB)
(MSB)				*Transmitted First*
7	*6*	*5*	*4*	**TX Mod. Level**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-5.6dB
0	0	1	0	-5.2dB
0	0	1	1	-4.8dB
0	1	0	0	-4.4dB
0	1	0	1	-4.0dB
0	1	1	0	-3.6dB
0	1	1	1	-3.2dB
1	0	0	0	-2.8dB
1	0	0	1	-2.4dB
1	0	1	0	-2.0dB
1	0	1	1	-1.6dB
1	1	0	0	-1.2dB
1	1	0	1	-0.8dB
1	1	1	0	-0.4dB
1	1	1	1	0dB
3	*2*	*1*	*0*	**TX Input Gain**
0	0	0	0	-2.65dB
0	0	0	1	-2.05dB
0	0	1	0	-1.50dB
0	0	1	1	-0.95dB
0	1	0	0	-0.45dB
0	1	0	1	0dB
0	1	1	0	0.45dB
0	1	1	1	0.85dB
1	0	0	0	1.25dB
1	0	0	1	1.65dB
1	0	1	0	2.05dB
1	0	1	1	2.40dB
1	1	0	0	2.70dB
1	1	0	1	3.05dB
1	1	1	0	3.35dB
1	1	1	1	3.65dB

Table 3 - TX Gain & Mod. Commands

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