MITSUBISHI SEMICONDUCTORS 1990

MICROPROCESSORS AND PERIPHERAL CIRCUITS

DATA BOOK

MITSUBISHI ELECTRIC

All values shown in this catalogue are subject to change for product improvement.

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INDEX BY FUNCTION

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics: Typ. pwr dissipation (mW)	Electrical characteristics: Max. access time (ns)	Electrical characteristics: Min. cycle time (ns)	Electrical characteristics: Max frequency (MHz)	Package	Page
■MELPS 85 NMOS MICROPROCESSORS									
M5L8085AP	8-Bit Parallel Microprocessor	N,Si,ED	5±5%	600	300	320	3	40P4	2—19
M5L8212P	8-Bit Input/Output Port with 3-State Output	B,LS	5±5%	450	30☆	—	—	24P4	2—34
M5L8216P	4-Bit Parallel Bidirectional Bus Driver (Non Inverting)	B,LS	5±5%	475	25☆	—	—	16P4	2—38
M5L8226P	4-Bit Parallel Bidirectional Bus Driver (Inverting)	B,LS	5±5%	425	25☆	—	—	16P4	2—38
■MELPS 85 CMOS MICROPROCESSORS									
M5M80C85AP-2	CMOS 8-bit Parallel Microprocessor	C,Si	5±10%	100	150	200	5	40P4	2—3
M5M80C85AFP-2		C,Si	5±10%	100	150	200	5	40P2R	2—3
M5M80C85AJ-2		C,Si	5±10%	100	150	200	5	44P0	2—3
■MELPS 86/88 MICROPROCESSORS									
M5L8282P	Octal Latch (Non Inverting)	B,LS	5±10%	250	—	—	—	20P4	3—3
M5L8283P	Octal Latch (Inverting)	B,LS	5±10%	250	—	—	—	20P4	3—3
M5L8284AP	Clock Generator and Driver for 8086/8088/8089 Processors	B,LS	5±10%	490	—	—	—	18P4	3—7
M5L8286P	Octal Bus Transceiver (Non Inverting)	B,LS	5±10%	400	—	—	—	20P4	3—16
M5L8287P	Octal Bus Transceiver (Inverting)	B,LS	5±10%	400	—	—	—	20P4	3—16
M5L8288P	Bus Controller	B,LS	5±10%	500	—	—	—	20P4	3—20
M5L8289P	Bus Arbiter	B,LS	5±10%	350	—	—	—	20P4	3—28
■NMOS PERIPHERAL CIRCUITS									
M5L8155P	2048-Bit Static RAM with I/O Ports and Timer ($\overline{CE}$="L" active)	N,Si,ED	5±5%	500	170	320	3	40P4	5—3
M5L8156P	2048-Bit Static RAM with I/O Ports and Timer (CE="H" active)	N,Si,ED	5±5%	500	170	320	3	40P4	5—11
M5L8251AP-5	Programmable Communication Interface	N,Si,ED	5±5%	300	250	320	3	28P4	5—19
M5L8253P-5	Programmable Interval Timer	N,Si,ED	5±10%	300	200	380	2.6	24P4	5—36
M5L8255AP-5	Programmable Peripheral Interface	N,Si,ED	5±5%	250	200	1150	—	40P4	5—44
M5L8257P-5	Programmable DMA Controller	N,Si,ED	5±5%	300	200	320	3	40P4	5—62
M5L8259AP	Programmable Interrupt Controller	N,Si,ED	5±10%	275	200	395	—	28P4	5—72
M5L8279P-5	Programmable Keyboard/Display Interface	N,Si,ED	5±10%	250	150	320	3	40P4	5—86

B = Bipolar. C = CMOS. ED = Enhancement depletion mode.
N = N-channel. Si = Silicon gate LS = Low power Schottkey.
☆Indicates propagation time.

INDEX BY FUNCTION

■CMOS PERIPHERAL CIRCUITS

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics: Typ pwr dissipation (mW)	Max access time (ns)	Min cycle time (ns)	Max frequency (MHz)	Package	Page
M5M81C55P-2	CMOS 2048-bit Static RAM with I/O Ports and Timer ($\overline{CE}$="L" active)	C,Si	5±10%	35	120	200	5	40P4	4—3
M5M81C55FP-2		C,Si	5±10%	35	120	200	5	40P2R	4—3
M5M81C55J-2		C,Si	5±10%	35	120	200	5	44P0	4—3
M5M81C56P-2	CMOS 2048-bit Static RAM with I/O Ports and Timer (CE="H" active)	C,Si	5±10%	35	120	200	5	40P4	4—13
M5M81C56FP-2		C,Si	5±10%	35	120	200	5	40P2R	4—13
M5M81C56J-2		C,Si	5±10%	35	120	200	5	44P0	4—13
M5M82C37AP-5	CMOS Programmable DMA Controller	C,Si	5±10%	22.5	140	200	5	40P4	4—23
M5M82C37AFP-5		C,Si	5±10%	22.5	140	200	5	40P2R	4—23
M5M82C37AJ-5		C,Si	5±10%	22.5	140	200	5	44P0	4—23
M5M82C51AP	CMOS Programmable Communication Interface	C,Si	5±10%	6	170	320	3	28P4	4—43
M5M82C51AFP		C,Si	5±10%	6	170	320	3	28P2W	4—43
M5M82C51AJ		C,Si	5±10%	6	170	320	3	28P0	4—43
M5M82C54P	CMOS Programmable Interval Timer	C,Si	5±10%	35	120	125	8	24P4	4—61
M5M82C54FP		C,Si	5±10%	35	120	125	8	24P2W	4—61
M5M82C54J		C,Si	5±10%	35	120	125	8	28P0	4—61
M5M82C55AP-2	CMOS Programmable Peripheral Interface	C,Si	5±10%	—	120	320	—	40P4	4—72
M5M82C55AFP-2		C,Si	5±10%	—	120	320	—	40P2R	4—72
M5M82C55AJ-2		C,Si	5±10%	—	120	320	—	44P0	4—72
M5M82C59AP-2	CMOS Programmable Interrupt Controller	C,Si	5±10%	—	120	310	—	28P4	4—88
M5M82C59AFP-2		C,Si	5±10%	—	120	310	—	28P2W	4—88
M5M82C59AJ-2		C,Si	5±10%	—	120	310	—	28P0	4—88
M5M82C255ASP	CMOS Programmable Peripheral Interface	C,Si	5±10%	—	120	320	—	64P4B	4—105

■32-BIT MICROPROCESSORS G_{MICRO}™ · M32 FAMILY

Type No	Circuit function	Structure	Supply voltage (V)	Electrical characteristics: Typ. power dissipation (mW)	Max frequency (MHz)	Package	Page
M33210GS/FP-20 ★★	32-Bit Microprocessor(M32/100)	C,Si	5±5%	—	20	135S8/160P6	7—3
M33220GS-20 ★★	32-Bit Microprocessor(M32/200)	C,Si	5±5%	—	20	135S8X-A	7—5
M33230GS-20 ★★	32-Bit Microprocessor(M32/300)	C,Si	5±5%	—	20	179S8X-B	7—7
M33241GS ★★	DMA Controller(M32/DMAC)	C,Si	5±5%	1200	20	179S8X-A	8—3
M33242SP/J ★★	Interrupt Request Controller(M32/IRC)	C,Si	5±5%	200	20	64P4X-A/68P0X-A	8—5
M33243GS-25,-30 ★★	TAG Memory(M32/TAGM)	C,Si	5±10%	1250	—	64S8X-A	8—7
M33244T-16,-20 ★★	Clock Pulse Generator for M32/200(CPG/200)	—	5±5%	—	16/20	14T4X-A	8—9
M33245GS ★★	Cache Controller/Memory(M32/CCM)	C,Si	5±5%	—	—	135S8	8—10
M33281GS-20 ★★	Floating Point Processing Unit(M32/FPU)	C,Si	5±5%	—	20	135S8X-A	8—12

The G_{MICRO}™ trade mark indicates a G-MICRO group thoron type micro processor

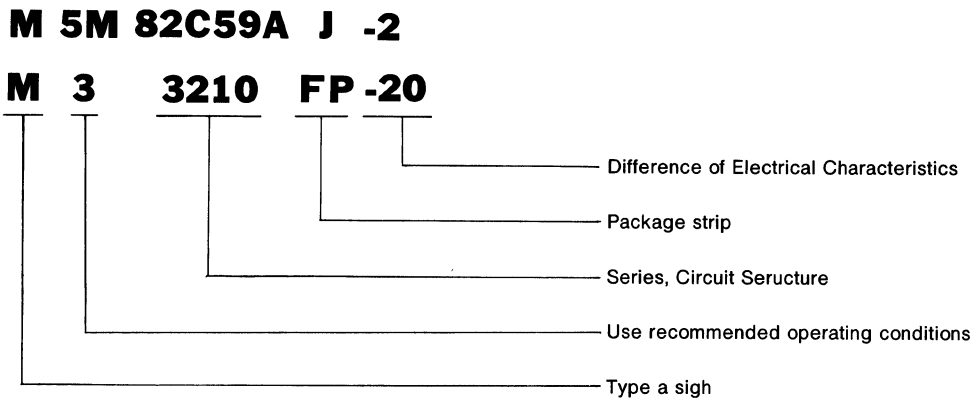
★★ : Under development

C = CMOS. Si = Silicon gate

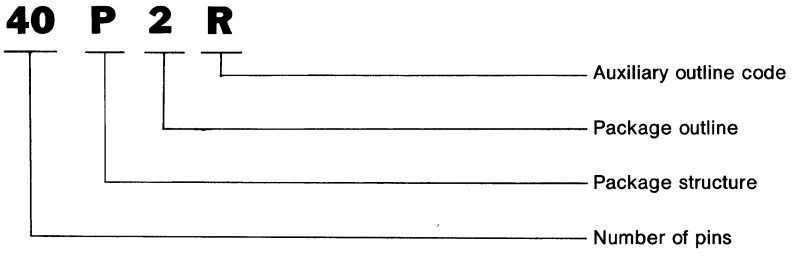
Understanding the Type-Designation Code

Type-designation examples are provided below to provide information about the products and their packages. These type designations are comprised of code elements. The blanks in some of the examples indicate that a code element is not necessary. When writing the type designation, the blank spaces are closed.

Example 1. (Device)



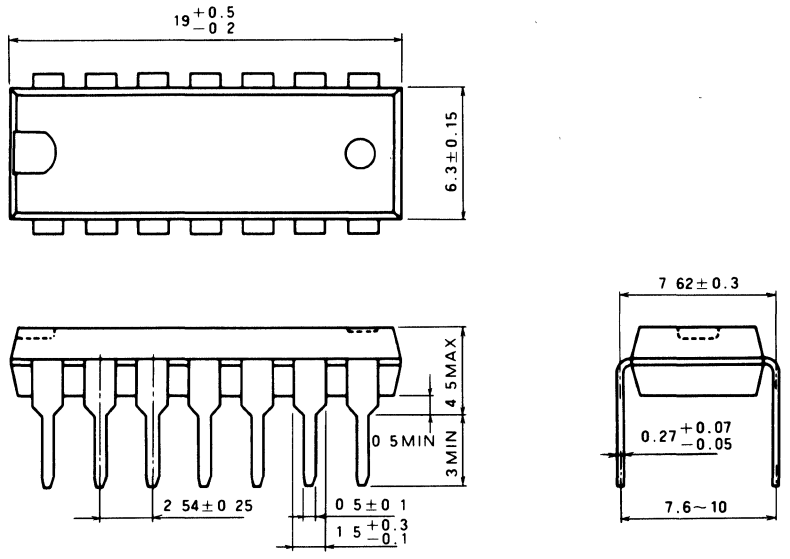
Example 2. (Package)



PACKAGE OUTLINES

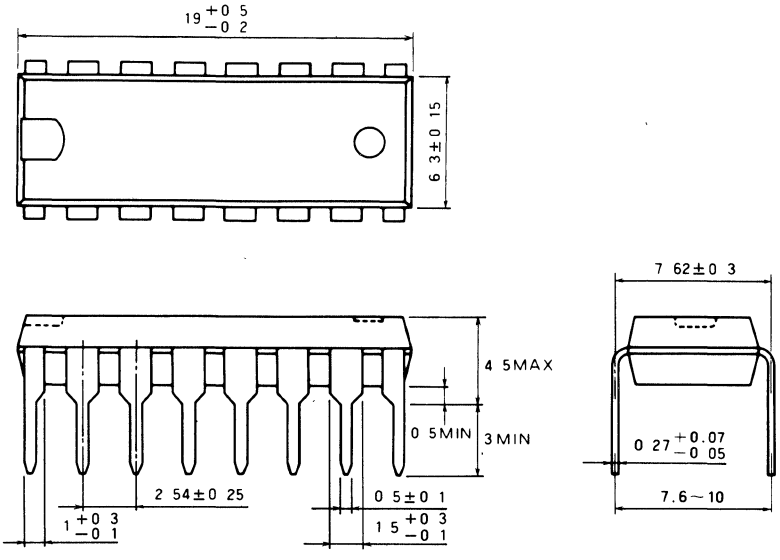
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm



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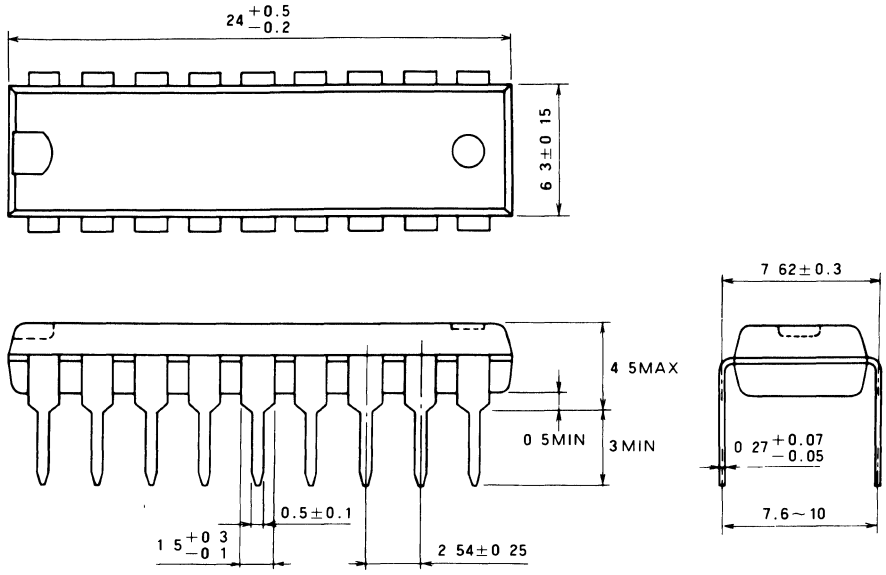
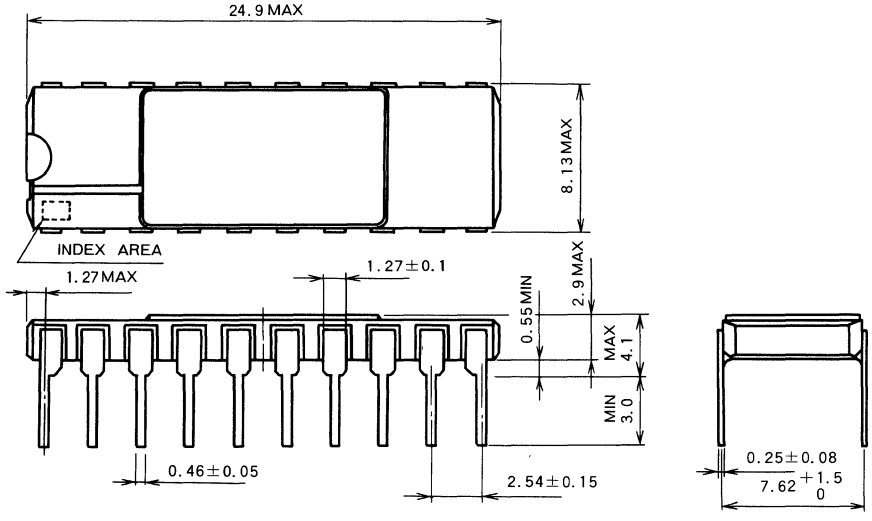
TYPE 18P4 18-PIN MOLDED PLASTIC DIP

Dimension in mm



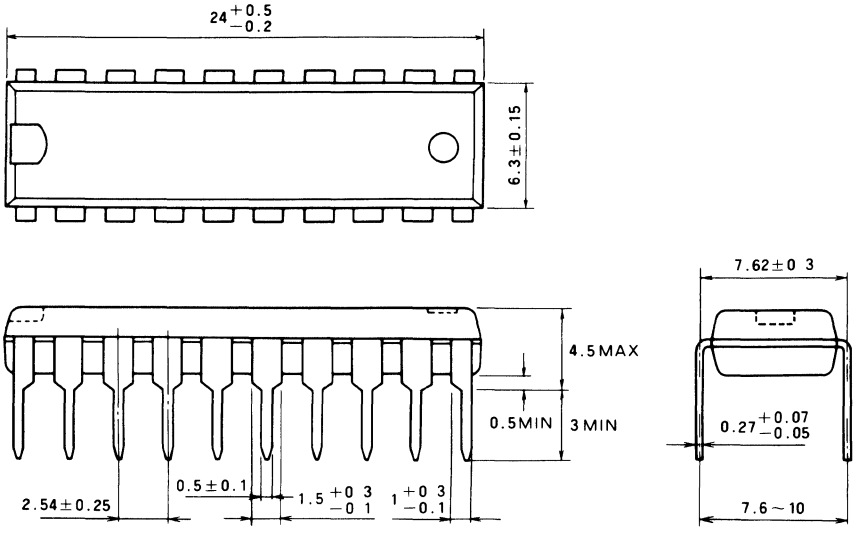
TYPE 20S1 20-PIN METAL-SEALED CERAMIC DIP

Dimension in mm



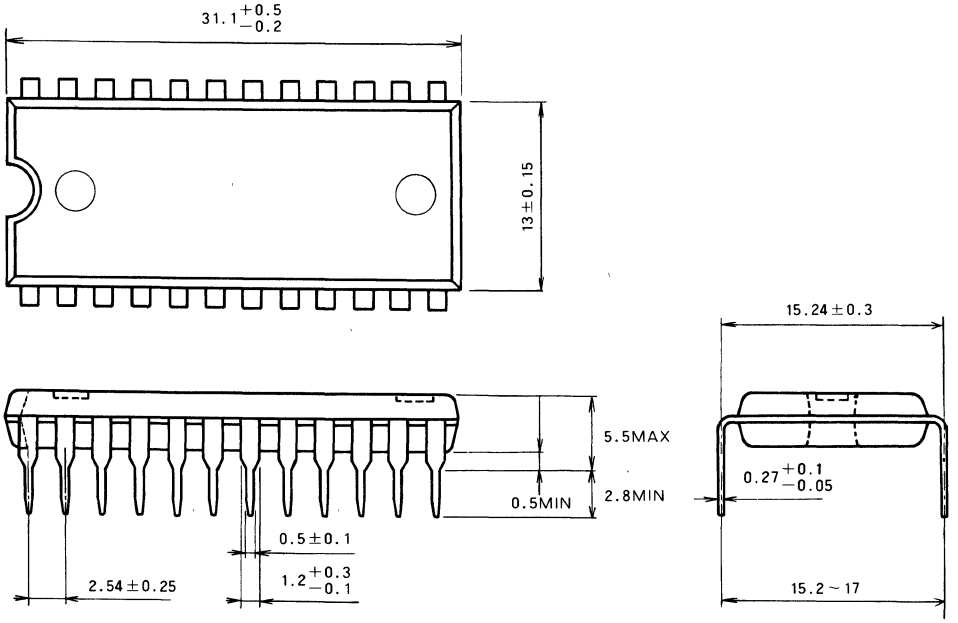
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4 24-PIN MOLDED PLASTIC DIP

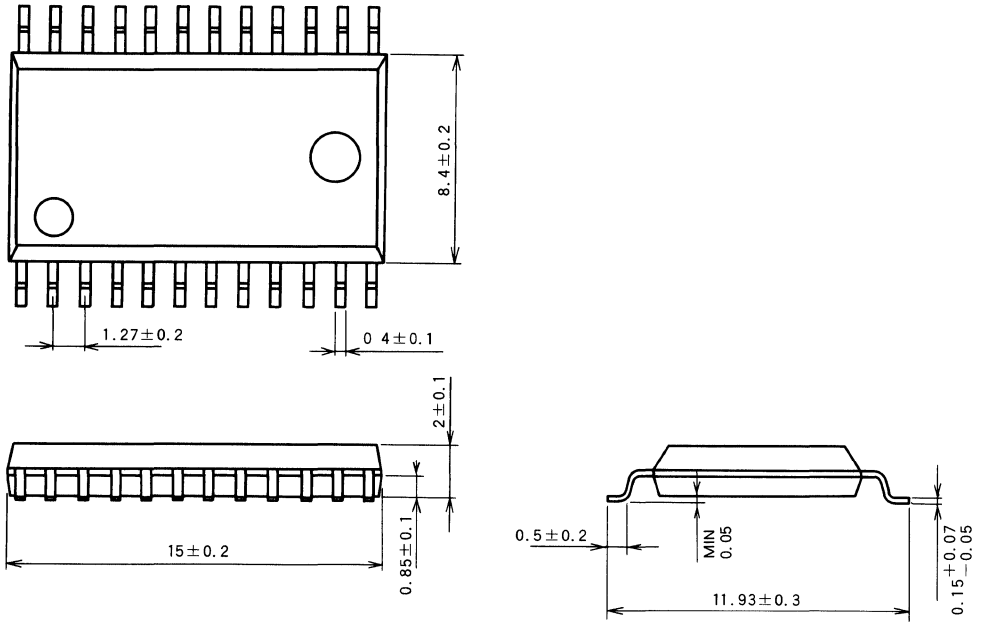
Dimension in mm



MITSUBISHI ELECTRIC

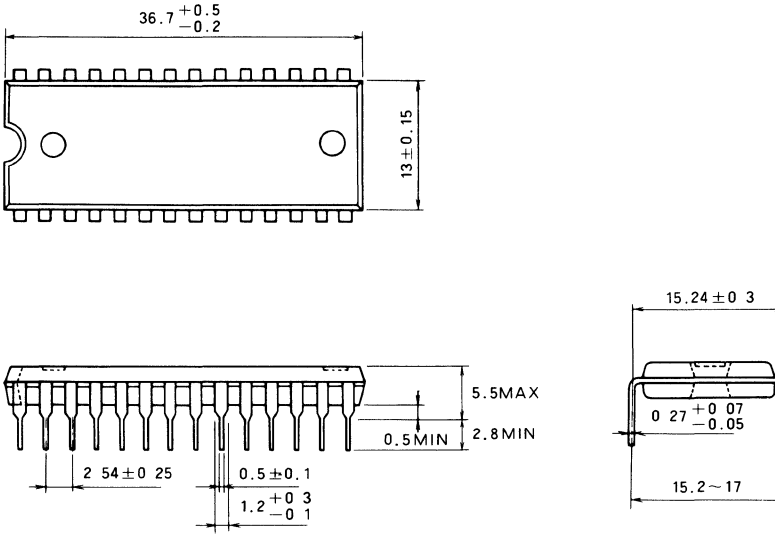
TYPE 24P2W 24-PIN MOLDED PLASTIC FLAT

Dimension in mm



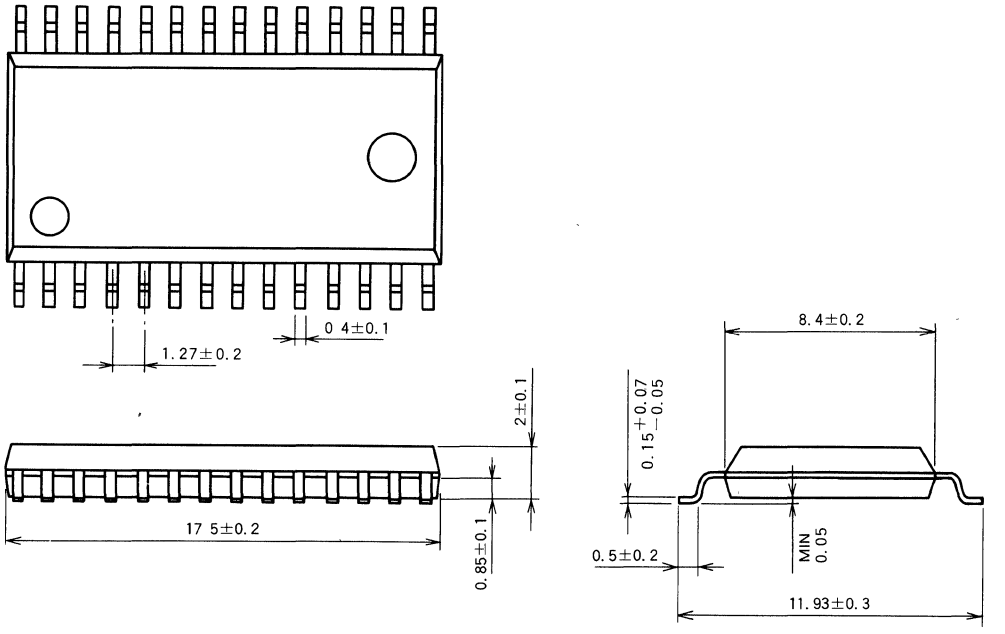
TYPE 28P4 28-PIN MOLDED PLASTIC DIP

Dimension in mm



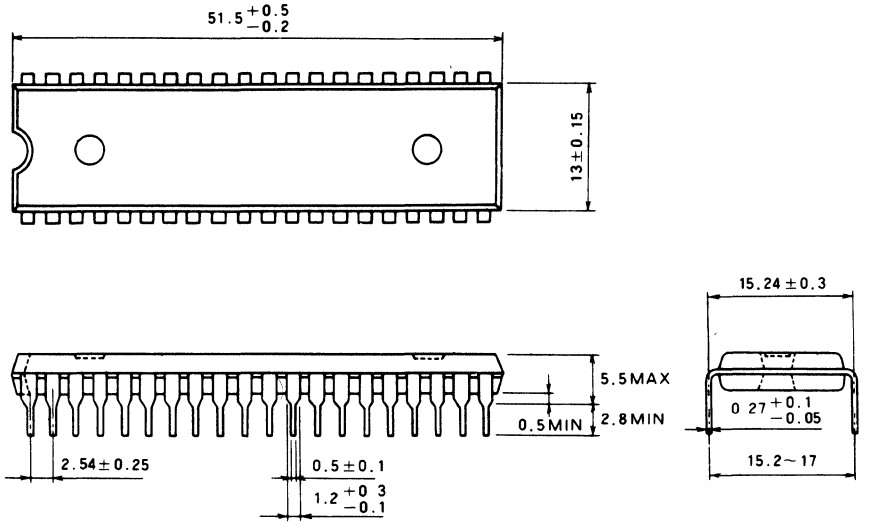
TYPE 28P2W 28-PIN MOLDED PLASTIC FLAT

Dimension in mm



TYPE 40P4 40-PIN MOLDED PLASTIC DIP

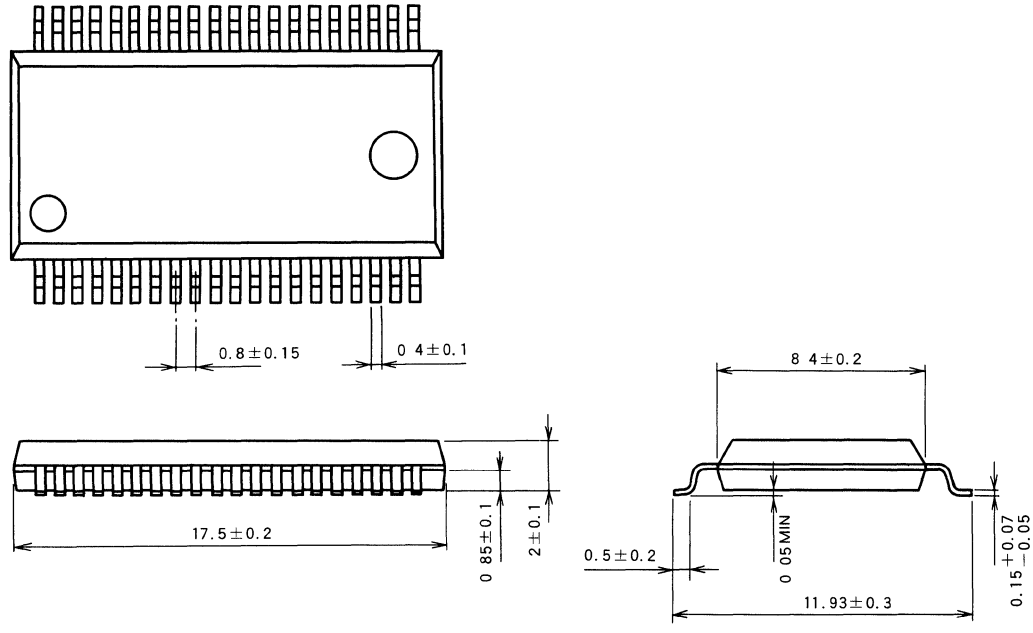
Dimension in mm



MITSUBISHI ELECTRIC

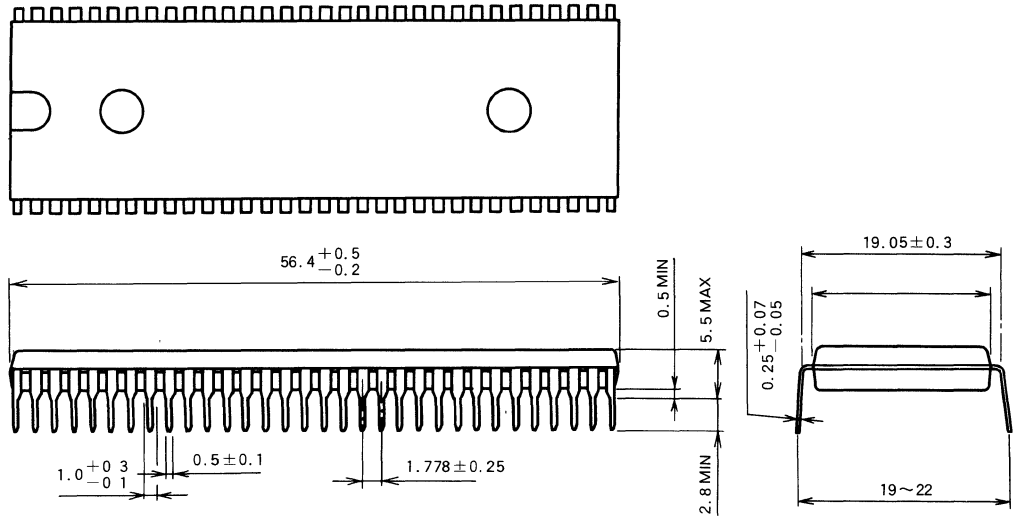
TYPE 40P2R 40-PIN MOLDED PLASTIC FLAT

Dimension in mm



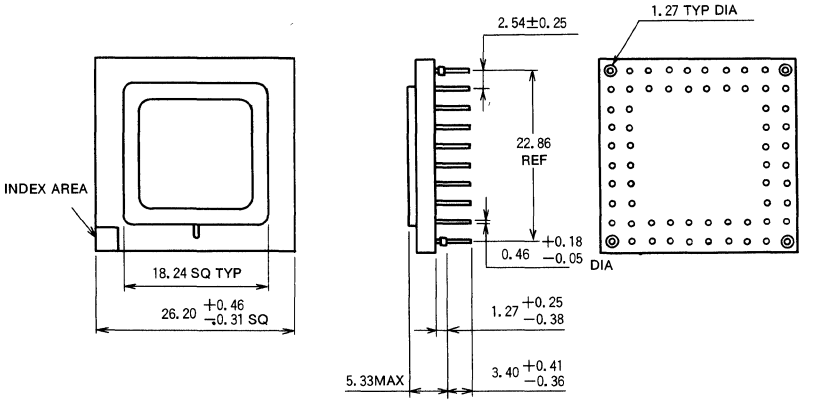
TYPE 64P4B 64-PIN MOLDED PLASTIC DIP (LEAD PITCH 1.78mm)

Dimension in mm



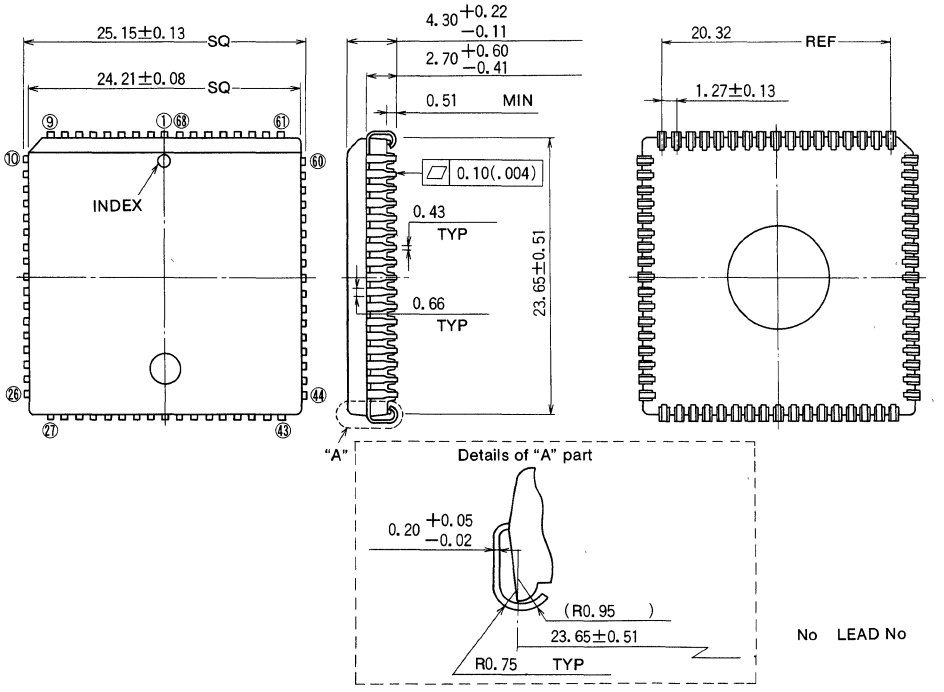
TYPE 64S8X-A 64-PIN METAL-SEALED CERAMIC PGA (GMICRO™)

Dimension in mm



TYPE 68P0X-A 68-PIN MOLDED PLASTIC LEADED CHIP CARRIER (GMICRO™)

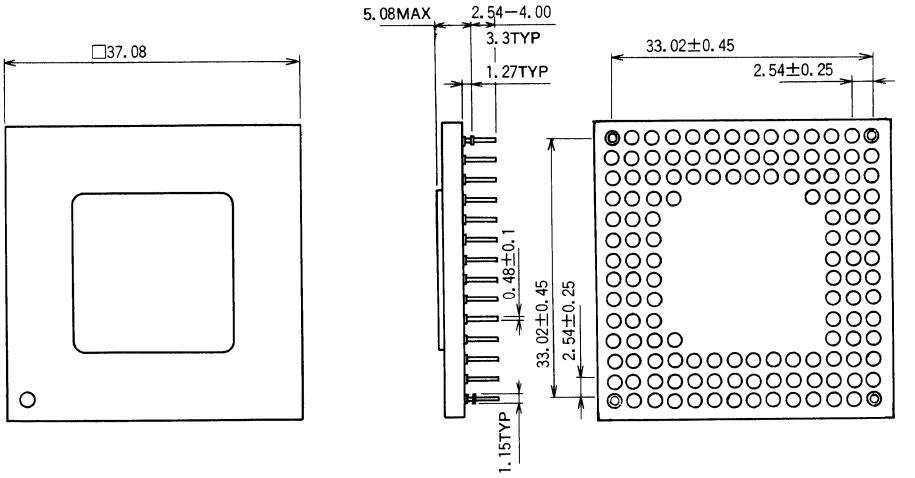
Dimension in mm



MITSUBISHI ELECTRIC

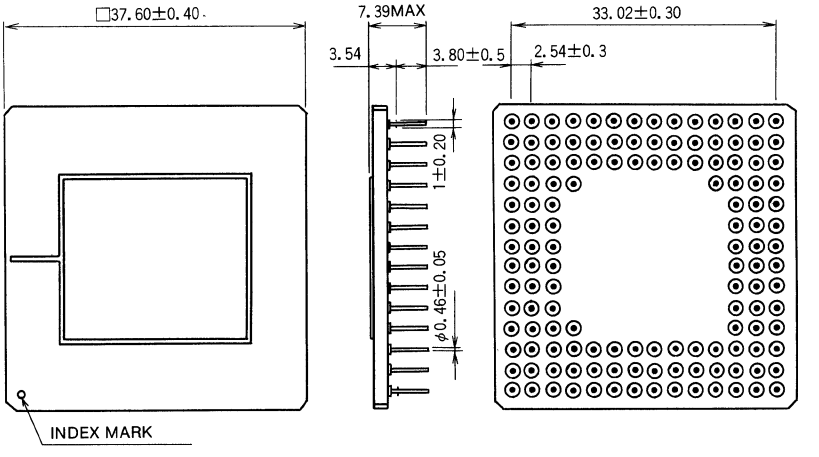
TYPE 135S8X-A 135-PIN METAL-SEALED CERAMIC PGA (GMICRO™)

Dimension in mm



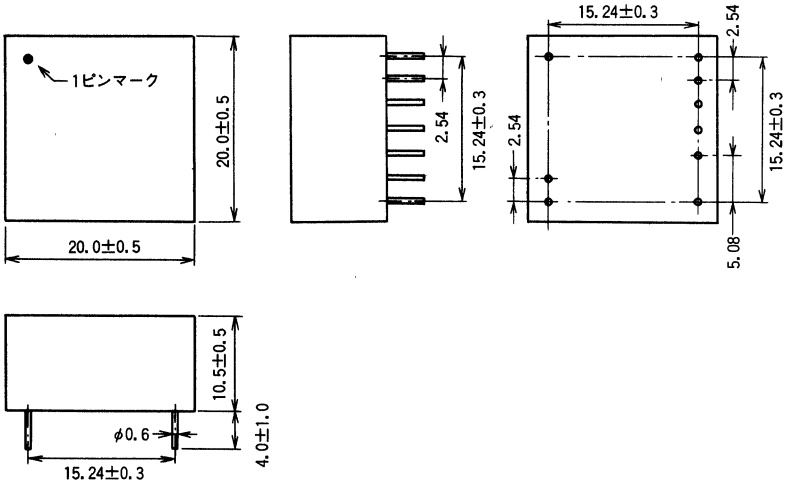
TYPE 135S8 135-PIN METAL-SEALED CERAMIC PGA (GMICRO™)

Dimension in mm



TYPE 14T4X-A 14-PIN HERMETIC-SEALED PACKAGE (GMICRO™)

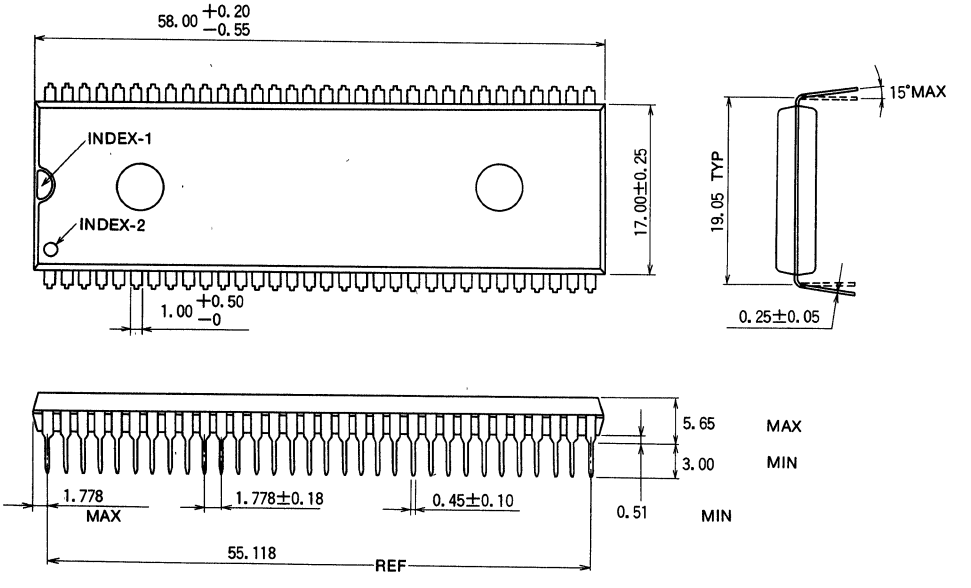
Dimension in mm



TYPE 64P4X-A 64-PIN MOLDED PLASTIC DIP (LEAD PITCH 1.778mm)

Dimension in mm

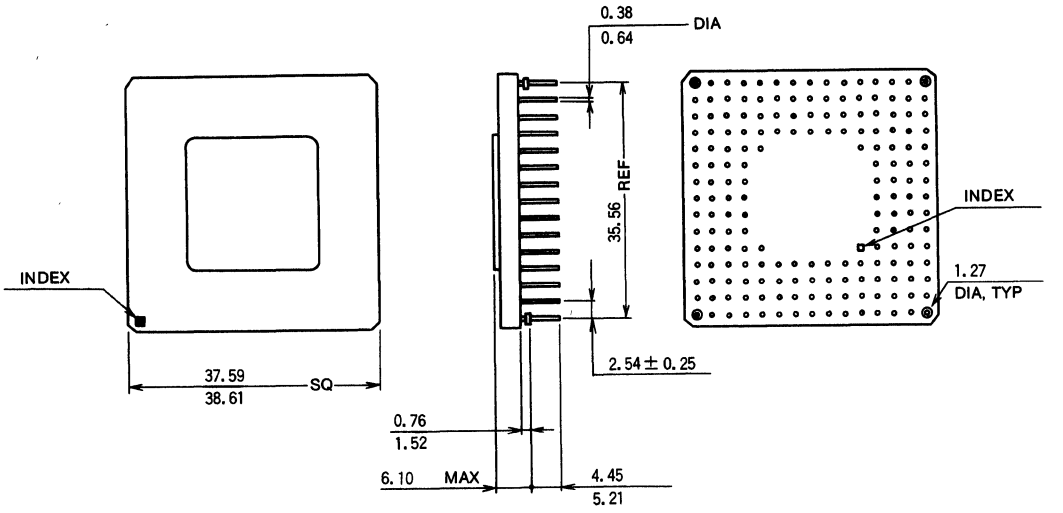
(GMICRO™)



MITSUBISHI ELECTRIC

TYPE 179S8X-A 179-PIN METAL-SEALED CERAMIC PGA (GMICRO™)

Dimension in mm



LETTER SYMBOLS FOR THE DYNAMIC PARAMETERS

1. INTRODUCTION

A system of letter symbols to be used to represent the dynamic parameters of intergrated circuit memories and other sequential circuits especially for single-chip microcomputers, microprocessors and LSIs for peripheral circuits has been discussed internationally in the TC47 of the International Electrotechnical Committee (IEC). Finally the IEC has decided on the meeting of TC47 in February 1980 that this system of letter symbols will be a Central Office document and circulated to all countries to vote which means this system of letter symbols will be a international standard.

The system is applied in this LSI data book for the new products only. Future editions of this data book will be applied this system. The IEC document which describes "Letter symbols for dynamic parameters of sequential integrated circuits, including memories" is introduced below. In this data book, the dynamic parameters in the IEC document are applied to timing requirements and switching characteristics.

2. LETTER SYMBOLS

The system of letter symbols outlined in this document enables symbols to be generated for the dynamic parameters of complex sequential circuits, including memories, and also allows these symbols to be abbreviated to simple mnemonic symbols when no ambiguity is likely to arise.

2.1. General Form

The dynamic parameters are represented by a general symbol of the form:

$$t_{A(BC-DC)F} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

where :

Subscript A indicates the type of dynamic parameter being represented, for example; cycle time, setup time, enable time, etc.

Subscript B indicates the name of the signal or terminal for which a change of state or level (or establishment of a state or level) constitutes a signal event assumed to occur first, that is, at the beginning of the time interval. If this event actually occurs last, that is, at the end of the time interval, the value of the time interval is negative.

Subscript C indicates the direction of the transition and/or the final state or level of the signal represented by B. When two letters are used, the initial state or level is also indicated.

Subscript D indicates the name of the signal or terminal for which a change of state or level (or establishment of a state or level) constitutes a signal event assumed to occur last, that is, at the end of the time interval. If this event actually occurs first, that is, at the beginning of the time interval, the value of the time interval is negative.

Subscript E indicates the direction of the transition and/or the final state or level of the signal represented by D. When two letters are used, the initial state or level is also indicated.

Subscript F indicates additional information such as mode of operation, test conditions, etc.

Note 1 Subscripts A to F may each consists of one or more letters

2 Subscripts D and E are not used for transition times

3 The "–" in the symbol (1) above is used to indicate "to", hence the symbol represents the time interval from signal event B occuring to signal event D occuring, and it is important to note that this convention is used for all dynamic parameters including hold times Where no misunderstanding can occur the hyphen may be omitted

2.2. Abbreviated Form

The general symbol given above may be abbreviated when no misunderstanding is likely to arise. For example to :

$t_{A(B-D)}$

or $t_{A(B)}$

or $t_{A(D)}$ – often used for hold times

or t_{AF} – no brackets are used in this case

or t_{A}

or t_{BC-DE} – often used for unclassified time intervals

2.3. Allocation of Subscripts

In allocating letter symbols for the subscripts, the most commonly used subscripts are given single letters where practicable and those less commonly used are designated by up to three letters. As far as possible, some form of mnemonic representation is used. Longer letter symbols may be used for specialised signals or terminals if this aids understanding.

3. SUBSCRIPT A (For Type of Dynamic Parameter)

The subscript A represents the type of dynamic parameter to be designated by the symbol and, for memories, the parameters may be divided into two classes :

a) those that are timing requirements for the memory and

LETTER SYMBOLS FOR THE DYNAMIC PARAMETERS

b) those that are characteristics of the memory.
The letter symbols so far proposed for memory circuits are listed in sub-clauses 3.1 and 3.2 below.
All subscripts A should be in lower-case.

3.1. Timing Requirements

The letter symbols for the timing requirements of semiconductor memories are as follows :

Term	Subscript
Cycle time	c
Time interval between two signal events	d
Fall time	f
Hold time	h
Precharging time	pc
Rise time	r
Recovery time	rec
Refresh time interval	rf
Setup time	su
Transition time	t
Pulse duration (width)	w

3.2. Characteristics

The letter symbols for the dynamic characteristics of semiconductor memories are as follows :

Characteristic	Subscript
Access time	a
Disable time	dis
Enable time	en
Propagation time	p
Recovery time	rec
Transition time	t
Valid time	v

Note Recovery time for use as a characteristic is limited to sense recovery time

4. SUBSCRIPTS B AND D (For Signal Name or Terminal Name)

The letter symbols for the signal name or the name of the terminal are as given below.
All subscripts B and D should be in upper-case.

Signal or terminal	Subscript
Address	A
Clock	C
Column address	CA
Column address strobe	CAS
Data input	D
Data input/output	DQ
Chip enable	E
Erasure	ER
Output enable	G
Program	PR
Data output	Q
Read	R
Row address	RA
Row address strobe	RAS
Refresh	RF
Read/Write	RW
Chip select	S
Write (write enable)	W

Note 1 In the letter symbols for time intervals, bars over the subscripts, for example CAS, should not be used
2 It should be noted, when further letter symbols are chosen, that the subscript should not end with H, K, V, X, or Z (See clause 5)
3 If the same terminal, or signal, can be used for two functions (for example Data input/output, Read/Write) the waveform should be labelled with the dual function, if appropriate, but the symbols for the dynamic parameters should include only that part of the subscript relevant to the parameter

5. SUBSCRIPTS C AND E (For Transition of Signal)

The following symbols are used to represent the level or state of a signal :

Transition of signal	Subscript
High logic level	H
Low logic level	L
Valid steady-state level (either low or high)	V
Unknown, changing, or 'don't care' level	X
High-impedance state of three-state output	Z

The direction of transition is expressed by two letters, the direction being from the state represented by the first letter to that represented by the second letter, with the letters being as given above.
When no misunderstanding can occur, the first letter may be omitted to give an abbreviated symbol for subscripts C and E as indicated below.
All subscripts C and E should be in upper-case.

Examples	Subscript	
	Full	Abbreviated
Transition from high level to low level	HL	L
Transition from low level to high level	LH	H
Transition from unknown or changing state to valid state	XV	V
Transition from valid state to unknown or changing state	VX	X
Transition from high-impedance state to valid state	ZV	V

Note Since subscripts C and E may be abbreviated, and since subscripts B and D may contain an indeterminate number of letters, it is necessary to put the restriction on the subscripts B and D that they should not end with H, L, V, X, or Z, so as to avoid possible confusion

6. SUBSCRIPT F (For Additional Information)

If necessary, subscript F is used to represent any additional qualification of the parameter such as mode of operation, test conditions, etc. The letter symbols for subscript F are given below.
Subscript F should be in upper-case.

Modes of operation	Subscript
Power-down	PD
Page-mode read	PGR
Page-mode write	PGW
Read	R
Refresh	RF
Read-modify-write	RMW
Read-write	RW
Write	W

FOR DIGITAL INTEGRATED CIRCUITS

New symbol	Former symbol	Parameter–definition
C_I		Input capacitance
C_O		Output capacitance
$C_{I/O}$		Input/output terminal capacitance
$C_{I(\phi)}$		Input capacitance of clock input
f		Frequency
$f_{(\phi)}$		Clock frequency
I		Current–the current into an integrated circuit terminal is defined as a positive value and the current out of a terminal is defined as a negative value
I_{BB}		Supply current from V_{BB}
$I_{BB(AV)}$		Average supply current from V_{BB}
I_{CC}		Supply current from Vcc
$I_{CC(AV)}$		Avarage supply current from Vcc
$I_{CC(PD)}$		Power-down supply current from Vcc
I_{DD}		Supply current from V_{DD}
$I_{DD(AV)}$		Average supply current from V_{DD}
I_{GG}		Supply current from V_{GG}
$I_{GG(AV)}$		Average supply current from V_{GG}
I_I		Input current
I_{IH}		High-level input current–the value of the input current when V_{OH} is applied to the input considered
I_{IL}		Low-level input current–the value of the input current when V_{OL} is applied to the input considered
I_{OH}		High-level output current–the value of the output current when V_{OH} is applied to the output considered
I_{OL}		Low-level output current–the value of the output current when V_{OL} is applied to the output considered
I_{OZ}		Off-state (high-impedance state) output current–the current into an output having a three-state capability with input condition so applied that it will establish according to the product specification, the off (high-impedance) state at the output
I_{OZH}		Off-state (high-impedance state) output current, with high-level voltage applied to the output
I_{OZL}		Off-state (high-impedance state) output current, with low-level voltage applied to the output
I_{OS}		Short-circuit output current
I_{SS}		Supply current from V_{SS}
Pd		Power dissipation
N_{EW}		Number of erase/write cycles
N_{RA}		Number of read access unrefreshed
R_i		Input resistance
R_L		External load resistance
R_{OFF}		Off-state output resistance
R_{ON}		On-state output resistance
t_a		Access time–the time interval between the application of a specified input pulse during a read cycle and the availability of valid data signal at an output
$t_{a(A)}$	$t_{a(AD)}$	Address access time–the time interval between the application of an address input pulse and the availability of valid data signals at an output
$t_{a(CAS)}$		Column address strobe access time
$t_{a(E)}$	$t_{a(CE)}$	Chip enable access time
$t_{a(G)}$	$t_{a(OE)}$	Output enable access time
$t_{a(PR)}$		Data access time after program
$t_{a(RAS)}$		Row address strobe access time
$t_{a(S)}$	$t_{a(CS)}$	Chip select access time
t_C		Cycle time
t_{CR}	$t_{C(RD)}$	Read cycle time–the time interval between the start of a read cylce and the start of the next cycle
t_{CRF}	$t_{C(REF)}$	Refresh cycle time–the time interval between successive signals that are intended to restore the level in a dynamic memory cell to its original level
t_{CPG}	$t_{C(PG)}$	Page-mode cycle time
t_{CRMW}	$t_{C(RMR)}$	Read-modify-write cycle time–the time interval between teh start of a cycle in which the memory is read and new data is entered, and the start of the next cycle
t_{CW}	$t_{C(WR)}$	Write cycle time–the time interval between the start of a write cycle and the start of the next cycle

New symbol	Former symbol	Parameter—definition
t_d		Delay time—the time between the specified reference points on two pulses
$t_{d(\phi)}$		Delay time between clock pulses—e g , symbology, delay time, clock 1 to clock 2 or clock 2 to clock 1
$t_{d(CAS\text{-}RAS)}$		Delay time, column address strobe to row address strobe
$t_{d(CAS\text{-}W)}$	$t_{d(CAS\ WR)}$	Delay time, column address strobe to write
$t_{d(RAS\text{-}CAS)}$		Delay time, row address strobe to column address strobe
$t_{d(RAS\text{-}W)}$	$t_{d(RAS\text{-}WR)}$	Delay time, row address strobe to write
$t_{dis(R\text{-}Q)}$	$t_{dis(R\text{-}DA)}$	Output disable time after read
$t_{dis(S)}$	$t_{PXZ(CS)}$	Output disable time after chip select
$t_{dis(W)}$	$t_{PXZ(WR)}$	Output disable time after write
t_{DHL}		High-level to low-level delay time } the time interval between specified reference points on the input and on the output pulses, when the
t_{DLH}		Low-level to high-level delay time } output is going to the low (high) level and when the device is driven and loaded by specified networks
$t_{en(A\text{-}Q)}$	$t_{PZV(A\text{-}DQ)}$	Output enable time after address
$t_{en(R\text{-}Q)}$	$t_{PZV(R\text{-}DQ)}$	Output enable time after read
$t_{en(S\text{-}Q)}$	$t_{PZX(CS\text{-}DQ)}$	Output enable time after chip select
t_f		Fall time
t_h		Hold time—the interval time during which a signal at a specified input terminal after an active transition occurs at another specified input terminal
$t_{h(A)}$	$t_{h(AD)}$	Address hold time
$t_{h(A\text{-}E)}$	$t_{h(AD\text{-}CE)}$	Chip enable hold time after address
$t_{h(A\text{-}PR)}$	$t_{h(AD\text{-}PRO)}$	Program hold time after address
$t_{h(CAS\text{-}CA)}$		Column address hold time after column address strobe
$t_{h(CAS\text{-}D)}$	$t_{h(CAS\text{-}DA)}$	Data-in hold time after column address strobe
$t_{h(CAS\text{-}Q)}$	$t_{h(CAS\text{-}OUT)}$	Data-out hold time after column address strobe
$t_{h(CAS\text{-}RAS)}$		Row address strobe hold time after column address strobe
$t_{h(CAS\text{-}W)}$	$t_{h(CAS\text{-}WR)}$	Write hold time after column address strobe
$t_{h(D)}$	$t_{h(DA)}$	Data-in hold time
$t_{h(D\text{-}PR)}$	$t_{h(DA\text{-}PRO)}$	Program hold time after data-in
$t_{h(E)}$	$t_{h(CE)}$	Chip enable hold time
$t_{h(E\text{-}D)}$	$t_{h(CE\text{-}DA)}$	Data-in hold time after chip enable
$t_{h(E\text{-}G)}$	$t_{h(CE\text{-}OE)}$	Output enable hold time after chip enable
$t_{h(R)}$	$t_{h(RD)}$	Read hold time
$t_{h(RAS\text{-}CA)}$		Column address hold time after row address strobe
$t_{h(RAS\text{-}CAS)}$		Column address strobe hold time after row address strobe
$t_{h(RAS\text{-}D)}$	$t_{h(RAS\text{-}DA)}$	Data-in hold time after row address strobe
$t_{h(RAS\text{-}W)}$	$t_{h(RAS\text{-}WR)}$	Write hold time after row address strobe
$t_{h(S)}$	$t_{h(CS)}$	Chip select hold time
$t_{h(W)}$	$t_{h(WR)}$	Write hold time
$t_{h(W\text{-}CAS)}$	$t_{h(WR\text{-}CAS)}$	Column address strobe hold time after write
$t_{h(W\text{-}D)}$	$t_{h(WR\text{-}DA)}$	Data-in hold time after write
$t_{h(W\text{-}RAS)}$	$t_{h(WR\text{-}RAS)}$	Row address hold time after write
t_{PHL}		High-level to low-level propagation time } the time interval between specified reference points on the input and on the output pulses when the
t_{PLH}		Low-level to high-level propagation time } output is going to the low (high) level and when the device is driven and loaded by typical devices of stated type
t_r		Rise time
$t_{rec(W)}$	t_{wr}	Write recovery time—the time interval between the termination of a write pulse and the initiation of a new cycle
$t_{rec(PD)}$	$t_{R(PD)}$	Power-down recovery time
t_{su}		Setup time—the time interval between the application of a signal which is maintained at a specified input terminal and a consecutive active tarnsition at another specified input terminal
$t_{su(A)}$	$t_{su(AD)}$	Address setup time
$t_{su(A\text{-}E)}$	$t_{su(AD\text{-}CE)}$	Chip enable setup time before address
$t_{su(A\text{-}W)}$	$t_{su(AD\text{-}WR)}$	Write setup time before address
$t_{su(CA\text{-}RAS)}$		Row address strobe setup time before column address

New symbol	Former symbol	Parameter—definition
$t_{su(D)}$	$t_{su(DA)}$	Data-in setup time
$t_{su(D-E)}$	$t_{su(DA-CE)}$	Chip enable setup time before data-in
$t_{su(D-W)}$	$t_{su(DA-WR)}$	Write setup time before data-in
$t_{su(E)}$	$t_{su(CE)}$	Chip enable setup time
$t_{su(E-P)}$	$t_{su(CE-P)}$	Precharge setup time before chip enable
$t_{su(G-E)}$	$t_{su(OE-CE)}$	Chip enable setup time before output enable
$t_{su(P-E)}$	$t_{su(P-CE)}$	Chip enable setup time before precharge
$t_{su(PD)}$		Power-down setup time
$t_{su(R)}$	$t_{su(RD)}$	Read setup time
$t_{su(R-CAS)}$	$t_{su(RA-CAS)}$	Column address strobe setup time before read
$t_{su(RA-CAS)}$		Column address strobe setup time before row address
$t_{su(S)}$	$t_{su(CS)}$	Chip select setup time
$t_{su(S-W)}$	$t_{su(CS-WR)}$	Write setup time before chip select
$t_{su(W)}$	$t_{su(WR)}$	Write setup time
t_{THL}		High-level to low-level transition time } the time interval between specified reference points on the edge of the output pulse when the output is going to the low (high) level and when a specified input signal is applied through a specified network and the output is loaded by another specified network
t_{TLH}		Low-level- to high-level transition time }
$t_{v(A)}$	$t_{dv(AD)}$	Data valid time after address
$t_{v(E)}$	$t_{dv(CE)}$	Data valid time after chip enable
$t_{v(E)PR}$	$t_{v(CE)PR}$	Data valid time after chip enable in program mode
$t_{v(G)}$	$t_{v(OE)}$	Data valid time after output enable
$t_{v(PR)}$		Data valid time after program
$t_{v(S)}$	$t_{v(CS)}$	Data valid time after chip select
t_w		Pulse width (pulse duration) the time interval between specified reference points on the leading and training edges of the waveforms
$t_{w(E)}$	$t_{w(CE)}$	Chip enable pulse width
$t_{w(EH)}$	$t_{w(CEH)}$	Chip enable high pulse width
$t_{w(EL)}$	$t_{w(EL)}$	Chip enable low pulse width
$t_{w(PR)}$		Program pulse width
$t_{w(R)}$	$t_{w(RD)}$	Read pulse width
$t_{w(S)}$	$t_{w(CS)}$	Chip select pulse width
$t_{w(W)}$	$t_{w(WR)}$	Wrtie pulse width
$t_{w(\phi)}$		Clock pulse width
Ta		Ambient temperature
Topr		Operating temperature
Tstg		Storage temperature
V_{BB}		V_{BB} supply voltage
V_{CC}		V_{CC} supply voltage
V_{DD}		V_{DD} supply voltage
V_{GG}		V_{GG} supply voltage
V_I		Input voltage
V_{IH}		High-level input voltage—the value of the permitted high-state voltage at the input
V_{IL}		Low-level input voltage—the value of the permitted low-state voltage at the input
V_O		Output voltage
V_{OH}		High-level output voltage—the value of the guaranteed high-state voltage range at the output
V_{OL}		Low-level output voltage—the value of the guaranteed low-state voltage range at the output
V_{SS}		V_{SS} supply voltage

QUALITY ASSURANCE AND RELIABILITY TESTING

1 INTRODUCTION

IC & LSI have made rapid technical progress in electrical performances of high integration, high speed, and sophisticated functionality. And now they have got boundless wider applications in electronic systems and electrical appliances.

To meet the above trend of expanding utilization of IC & LSI, Mitsubishi considers that it is extremely important to supply stable quality and high reliable products to customers.

Mitsubishi Electric places great emphasis on quality as a basic policy "Quality First", and has striven always to improve quality and reliability.

Mitsubishi has already developed the Quality Assurance System covering design, manufacturing, inventory and delivery for IC & LSI, and has supplied highly reliable products to customers for many years. The following articles describe the Quality Assurance System and examples of reliability control for Mitsubishi Microprocessor and Peripheral Circuits ICs.

2. QUALITY ASSURANCE SYSTEM

The Quality Assurance System places emphasis on built-in reliability in designing and built-in quality in manufacturing. The System from development to delivery is summarized in Figure 1.

2.1 Quality Assurance in Designing

The following steps are applied in the designing stage for a new product.

(1). Setting of perfomance, quality and reliability target for new product.
(2) Discussion of performance and quality for circuit design, device structure, process, material and package.
(3) Verification of design by CAD system to meet standardized design rule.
(4) Functional evaluation for bread-board device to confirm electrical performance.
(5) Reliability evaluation for TEG (Test Element Group) chip to detect basic failure mode and investigate failure machanism.
(6) Reliability test (In-house qualification) for new product to confirm quality and reliability target.
(7) Decision of pre-production from the standpoint of performance, reliability, production flow/conditions, production capability, delivery and etc.

2.2 Quality Assurance in Manufacturing

Quality assurance in manufacturing is performed as follows

(1) Environment control such as temperature, humidity and dust as well as deionized water and utility gases.
(2) Maintenance and calibration control for automatized manufacturing equipment, automatic testing equipment, and measuring instruments.
(3) Material control such as silicon wafer, lead frame, packaging material, mask and chemicals.
(4) In-process inspections in wafer-fabrication, assembly and testing.
(5) 100% final inspection of electrical characteristics, visual inspection and burn-in, if necessary.
(6) Quality assurance test
-Electrical characteristics and visual inspection, lot by lot sampling
-Environment and endurance test, periodical sampling.
(7) Inventory and shipping control, such as storage environment, date code identification, handling and ESD (Electro Static Discharge) preventive procedure.

2.3 Reliability Test

To verify the reliability of a product as described in the Mitsubishi Quality Assurance System, reliability tests are performed at three different stages : new product development, pre-production, and mass-production.

At the development of a new product the reliability test plan is fixed corresponding to the quality and reliability target of each product, respectively. The test plan includes in-house qualification test, and TEG evaluation, if necessary. TEG chips are designed and prepared for new device structure, new process and new material.

After the proto-type product has passed the in-house qualification test, the product advances to the pre-production. In the pre-production stage, the specific reliability tests are programmed and performed again to verify the quality of pre-production product.

In the mass production, the reliability tests are performed periodically to confirm the quality of the mass production product according to the quality assurance test program.

Table 1 TYPICAL RELIABILITY TEST PROGRAM FOR PLASTIC ENCAPSULATED IC & LSI

Group	Test	Test condition
1	Solderability	230℃, 5sec Rosin flux
2	Soldering heat	260℃, 10sec
	Thermal shock	−55℃, 125℃, 15cycles
	Temperature cycling	−65℃, 150℃, 100cycles
3	Lead fatigue	250gr, 90°, 2arcs
4	Shock	1500G, 0.5msec
	Vibration	20G, 100~2000Hz X, Y, Z direction 4min /cycle, 4cycles/direction
	Constant acceleration	20000G, Y direction, 1min
5	Dynamic operation life	T_a=Toprmax, Vccmax 1000hours
6	High temperature storage life	T_a=150℃, 1000hours
7	High temperature and high humidity	85℃, 85%, 1000hours
	Pressure cooker	121℃, 100%, 100hours

QUALITY ASSURANCE AND RELIABILITY TESTING

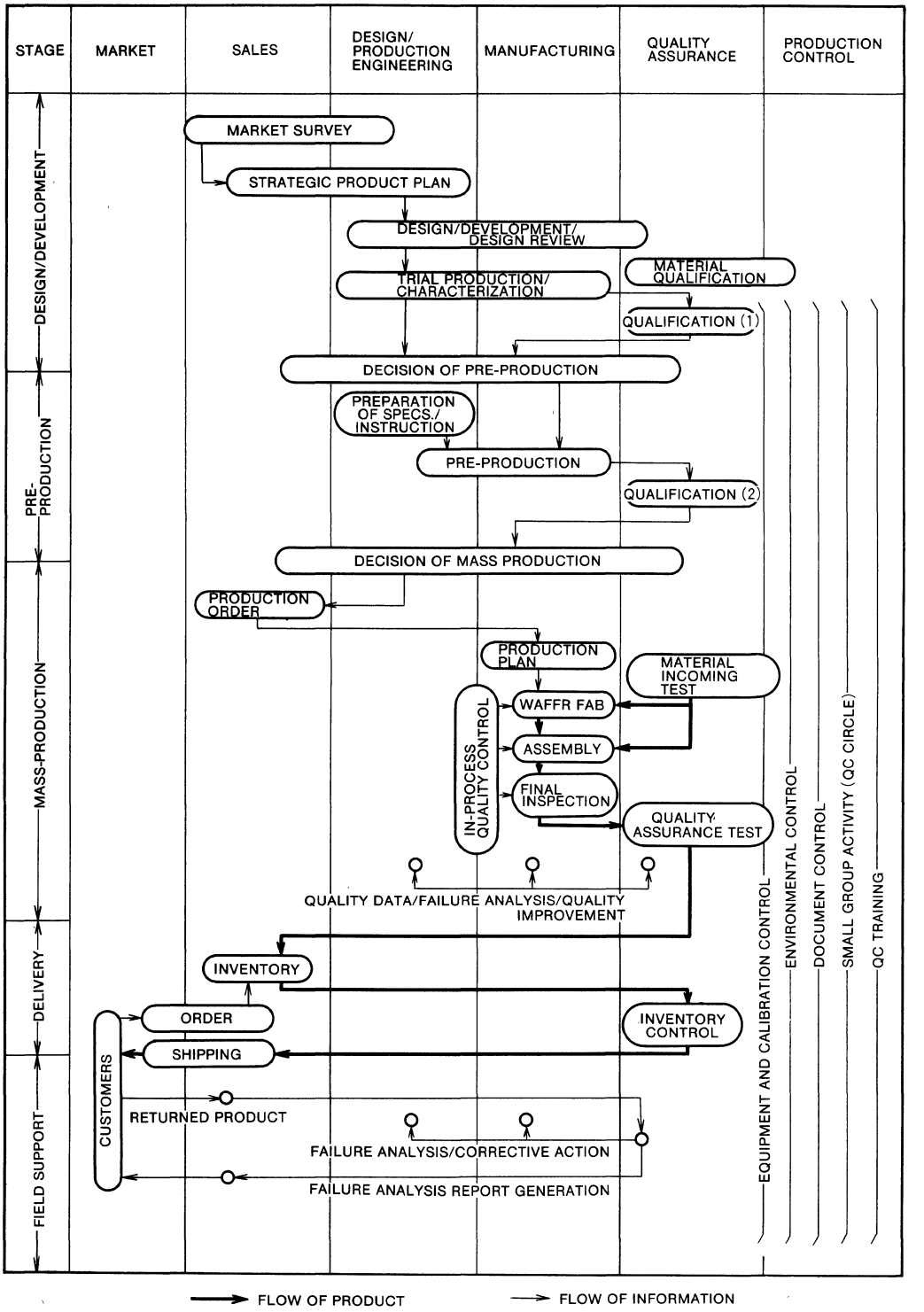


Fig.1 FLOW CHART OF QUALITY ASSURANCE SYSTEM

Table 1 shows an example of reliability test program for plastic encapsulated IC & LSI.

2.4 Returned Product Control

When failure analysis is requested by a customer, the failed devices are returned to Mitsubishi Electric via the sales office of Mitsubishi using the form of "Analysis Request of Returned Product"

Mitsubishi provides various failure analysis equipment to analyze the returned product. A failure analysis report is generated to the customer upon completion of the analysis. The failure analysis result enforces taking corrective action for the design, fabrication, assembly or testing of the product to improve reliability and realize lower failure rate.

Figure 2 shows the procedure of returned product control from customer.

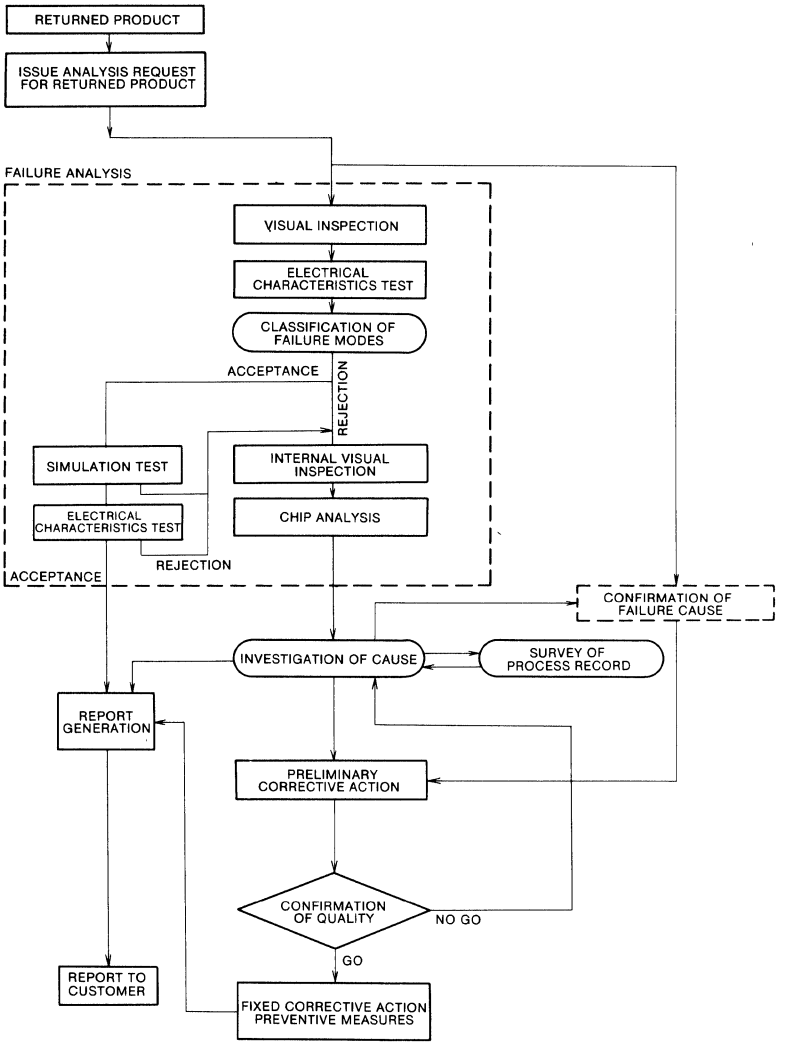


Fig.2 PROCEDURE OF RETURNED PRODUCT CONTROL

3 RELIABILITY TEST RESULTS

The reliability test results for Mitsubishi General Purpose ICs are shown in Table 2, Table 3 and Table 4.

Table 2 shows the result of endurance tests of dynamic operation life and high temperature storage life test for representative types of General Purpose ICs, Operational Amplifier, Voltage Comparator, Timer, Motor Driver, Voltage Regulator and Transistor Array. From Table 2, the combined failure rate of Mitsubishi Microprocessor and Peripheral Circuits ICs is calculated 0.15%/1000hours (60% confidence level) at maximum rating of operating condition.

Table 3 shows the results of the environment tests of thermal stress, high temperature/high humidity and pressure cooker test for the same type of products in regards to endurance tests.

Table 4 shows the results of mechanical tests for representative products of various package types

Table 2 ENDURANCE TEST RESULTS

Application	Test / Test Condition / Type Number	Operating Life Test: T_a=125℃ $V_{CC} \leqq V_{CC}max$ Number of Samples	Device Hours	Number of Failures	High Temperature Storage Life: T_a=150℃ Number of Samples	Device Hours	Number of Failures
MELPS 85 MPU	M5L8085AP	22	22,000	0	22	22,000	0
	M5L8212P	38	38,000	0	22	44,000	0
MELPS 86/88 MPU	M5L8284AP	38	38,000	0	22	44,000	0
	M5L8288S	38	38,000	0	22	44,000	0
	M5L8289P	38	38,000	0	22	44,000	0
NMOS Peripheral Circuit	M5L8251AP-5	22	22,000	0	22	22,000	0
	M5L8253P-5	88	88,000	0	22	22,000	0
	M5L8255AP-5	88	88,000	0	44	22,000	0
	M5L8259AP	22	22,000	0	22	22,000	0
CMOS Peripheral Circuit	M5M82C37AP-4	22	22,000	0	22	22,000	0
	M5M82C37AFP-4	22	22,000	0	22	22,000	0
	M5M82C54P-6	22	22,000	0	22	22,000	0
	M5M82C54FP-6	22	22,000	0	22	22,000	0
	M5M82C55AP-5	22	22,000	0	22	22,000	0
	M5M82C55AFP-5	22	22,000	0	22	22,000	0
	M5M81C55P-2	22	22,000	0	22	22,000	0
	M5M81C55FP-2	22	22,000	0	22	22,000	0
	M5M82C59AP-2	22	22,000	0	22	22,000	0
	M5M82C55AFP-2	22	22,000	0	22	22,000	0

Table 3 ENVIRONMENTAL TEST RESULTS

Application	Test / Test Condition / Type Number	Soldering Heat Thermal Shock Temperature Cycling: 260℃, 10sec −55℃, 125℃, 15cycles −65℃, 150℃, 100cycles Number of Samples	Number of Failures	High Temperature/High Humidity: 85℃, 85% 1000hours V_{CC}=5V~5.5V Number of Samples	Number of Failures	Pressure Cooker: 121℃, 100%RH 240hours Number of Samples	Number of Failures
MELPS 85 MPU	M5L8085AP	22	0	44	0	88	0
	M5L8212P	38	0	22	0	22	0
MELPS 86/88 Microprocssors	M5L8284AP	38	0	22	0	22	0
	M5L8288S	38	0	22	0	22	0
	M5L8289P	38	0	22	0	22	0
NMOS Peripheral Circuit	M5L8251AP-5	22	0	22	0	44	0
	M5L8253P-5	22	0	88	0	220	0
	M5L8255AP-5	22	0	88	0	176	0
	M5L8259AP	22	0	22	0	22	0
CMOS Peripheral Circuit	M5M82C37AP-4	22	0	22	0	22	0
	M5M82C37AFP-4	22	0	22	0	22	0
	M5M82C54P-6	22	0	22	0	22	0
	M5M82C54FP-6	22	0	22	0	22	0
	M5M82C55AP-5	22	0	22	0	22	0
	M5M82C55AFP-5	22	0	22	0	22	0
	M5M81C55P-2	22	0	22	0	22	0
	M5M81C55FP-2	22	0	22	0	22	0
	M5M82C59AP-2	22	0	22	0	22	0
	M5M82C59AFP-2	22	0	22	0	22	0

Table 4 MECHANICAL TEST RESULTS

Test		Solderability		Lead Fatigue		Shock Vibration Constant Acceleration	
Test Condition		See Table 1		See Table 1		See Table 1	
Package Pin Count	Type Number	Number of Samples	Number of Failures	Number of Samples	Number of Failures	Number of Samples	Number of Failures
24P4	M5L8253P-5	60	0	30	0	22	0
28P4	M5L8251AP-5	30	0	30	0	22	0
	M5L8259AP	30	0	15	0	22	0
40P4	M5L8085AP	30	0	30	0	22	0
	M5L8255AP-5	30	0	30	0	22	0
28P2W	M5M8259AFP	15	0	15	0	22	0
40P2W	M5M82C55AFP-5	15	0	15	0	22	0

4 FAILURE ANALYSIS

Accelerated reliability tests are applied to observe failures casued by temperature, voltage, humidity, current, mechanical stress and those combined stresses on chips and packages

Examples of typical failure modes are shown below.

(1) Wire Bonding Failure by Thermal Stress

Figure 3, Figure 4 and Figure 5 are examples of a failure which occurs by high temperature storage test of 225℃, 1000hours.

Au-Al intermetallic formation, so-called "Purple plague", by thermal overstress makes Au wire lift off from aluminum metallization. The activation energy of this failure mode is estimated at approximately 1.0eV and no failure has been observed so far in practical uses.

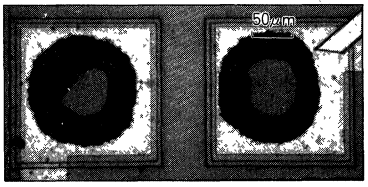


Fig.3
Micrograph of lifted Au ball trace on Al bonding pad

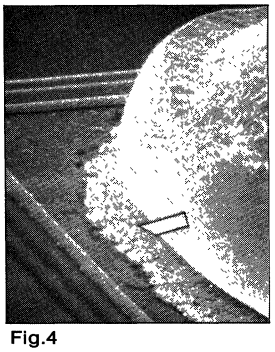


Fig.4
Au-Al plague formation on bonding pad

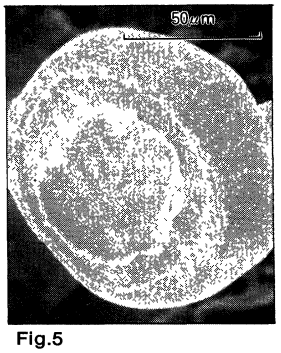


Fig.5
Lifted Au wire ball base

(2) Aluminum Corrosion Failure by Temperature/Humidity Stress.

Figure 6, Figure 7 and Figure 8 are examples of corroded failure of aluminum metallization of plastic encapsulated IC after accelerated temperature/humidity storage test (pressure cooker test) of 121℃, 100%RH, 1000hours duration.

Aluminum bonding pad is dissolved by penetrated water from plastic package, and chlorine concentration is observed on corroded aluminum bonding pad as shown in Figure 8.

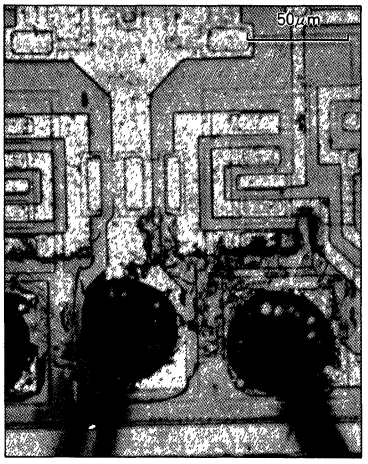


Fig.6
Micrograph of corroded Aluminum metallization

(3) Destructive Failure by Electrical Overstress

Surge voltage marginal tests have been performed to reproduce the electrical overstress failure in field uses. Figure 9 and Figure 10 are examples of failure observed by surge voltage test. The trace of destruction is verified as the aluminum bridge by X ray micro analysis.

Fig.7 Enlarged micrograph of corroded Aluminum bonding pad

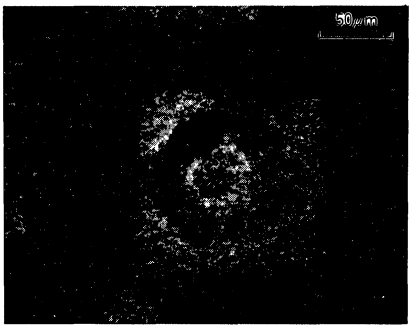


Fig.8 Cl distribution on corroded Aluminum bonding pad

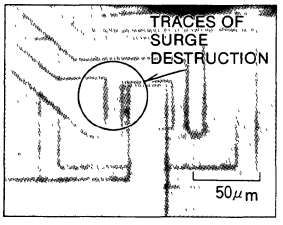


Fig.9 Micrograph of surge voltage destruction

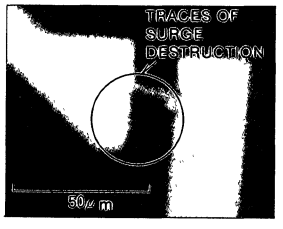


Fig.10 Aluminum trace of destructive spot

(4) Aluminum Electromigration

Figure 11 shows an open circuit of aluminum metallization in high current density region caused by accelerated operation life test. This failure is due to aluminum electromigration. Voids and hillock have been formed in aluminum metallization by high current density operation.

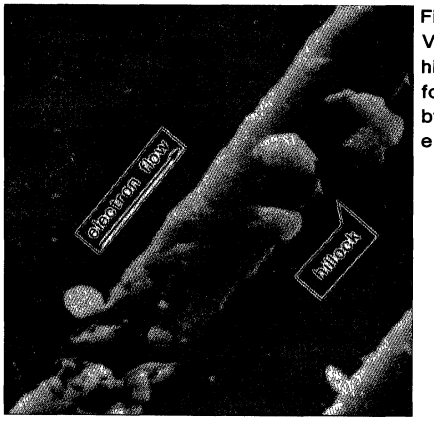


Fig.11 Voids and hillocks formation by Aluminum electromigration

5 SUMMARY

The Mitsubishi quality assurance system and examples of reliability control have been discussed. The customer's interests and requirements for high reliability IC & LSI are increasing significantly. To satisfy the customer's expectancy, Mitsubishi as an IC vendor, would like to make perpetual efforts in the following areas.

(1) Emphasis on built-in reliability at design stage and reliability evaluation to investigate latent failure modes and acceleration factors.

(2) Execution of periodical endurance, environment and mechanical test to verify reliability target and realize higher reliability.

(3) Focus on development of advanced failure analysis techniques. Detail failure analysis, intensive corrective action, and quick response to customer's analysis request.

(4) Collection of customer's quality data in qualification, incoming inspection, production and field use to improve PPM, fraction defective and FIT, failure rate.

Mitsubishi would highly appreciate it if the customer would provide quality and reliability data of incoming inspection or field failure rate essential to verify and improve the quality/reliability of IC & LSI.

PRECAUTIONS IN HANDLING MOS ICs

A MOS transistor has a very thin oxide insulator under the gate electrode on the silicon substrate. It is operated by altering the conductance (g_m) between source and drain to control mobile charges in the channel formed by the applied gate voltage.

If a high voltage were applied to a gate terminal, the insulator-film under the gate electrode could be destroyed, and all Mitsubishi MOS IC/LSIs contain internal protection circuits at each input terminal to prevent this. It is inherently necessary to apply reverse bias to the P-N junctions of a MOS IC/LSI.

Under certain conditions, however, it may be impossible to completely avoid destruction of the thin insulator-film due to the application of unexpectedly high voltage or thermal destruction due to excessive current from a forward biased P-N junction. The following recommendations should be followed in handling MOS devices.

1. KEEPING VOLTAGE AND CURRENT TO EACH TERMINAL BELOW MAXIMUM RATINGS

1. The recommended ranges of operating conditions provide adequate safety margins. Operating within these limits will assure maximum equipment performance and quality.
2. Forward bias should not be applied to any terminal since excessive current may cause thermal destruction.
3. Output terminals should not be connected directly to the power supply. Short-circuiting of a terminal to a power supply having low impedance may cause burn-out of the internal leads or thermal destruction due to excessive current.

2. KEEPING ALL TERMINALS AT THE SAME POTENTIAL DURING TRANSPORT AND STORAGE

When MOS IC/LSIs are not in use, both input and output terminals can be in a very high impedance state so that they are easily subjected to electrostatic induction from AC fields of the surrounding space or from charged objects in their vicinity. For this reason, MOS IC/LSIs should be protected from electrostatic charges while being transported and stored by conductive rubber foam, aluminum foil, shielded boxes or other protective precautions.

3. KEEPING ELECTRICAL EQUIPMENT, WORK TABLES AND OPERATING PERSONNEL AT THE SAME POTENTIAL

1. All electric equipment, work table surfaces and operating personnel should be grounded. Work tables should be covered with copper or aluminum plates of good conductivity, and grounded. One method of grounding personnel, after making sure that there is no potential difference with electrical equipment, is by the use of a wristwatch metallic ring, etc. attached around the wrist and grounded in series with a 1M Ω resistor. Be sure that the grounding meets national regulations on personnel safety.
2. Current leakage from electric equipment must be prevented not only for personnel safety, but also to avert the destruction of MOS IC/LSIs, as described above. Items such as testers, curve-tracers and synchroscopes must be checked for current leakage before being grounded.

4. PRECAUTIONS FOR MOUNTING OF MOS IC/LSIs

1. The printed wiring lines to input and output terminals of MOS IC/LSIs should not be close to or parallel to high-voltage or high-power signal lines. Turning power on while the device is short-circuited, either by a solder bridge made during assembly or by a probe during adjusting and testing, may cause maximum ratings to be exceeded, which may result in the destruction of the device.
2. When input/output, or input and/or output, terminals of MOS IC/LSIs (now open-circuits) are connected, we must consider the possibility of current leakage and take precautions similar to §2 above. To reduce such undesirable trouble, it is recommended that an interface circuit be inserted at the input or output terminal, or a resistor with a resistance that does not exceed the output driving capability of the MOS IC/LSI be inserted between the power supply and the ground.
3. A filter circuit should be inserted in the AC power supply line to absorb surges which can frequently be strong enough to destroy a MOS IC/LSI.
4. Terminal connections should be made as described in the catalog while being careful to meet specifications.
5. Ungrounded metal plates should not be placed near input or output terminals of any MOS IC/LSIs, since destruction of the insulation may result if they become electrostatically charged.
6. Equipment cases should provide shielding from electrostatic charges for more reliable operation. When a plastic case is used, it is desirable to coat the inside of the case with conductive paint and to ground it. This is considered necessary even for battery-operated equipment.

MELPS 85 MICROPROCESSORS

2

M5M80C85AP-2/FP-2/J-2

CMOS 8-BIT PARALLEL MICROPROCESSOR

DESCRIPTION

The M5M80C85AP-2 is a family of single-chip 8-bit parallel central processing units (CPUs) developed using the silicon gate CMOS process. It has a basic clock rate of 5MHz. It is housed in a 40-pin plastic molded DIP.
And preparatory for surface equipment M5M80C85AFP-2 (SOP) and M5M80C85AJ-2 (PLCC).

FEATURES

- Single 5V supply voltage
- Clock period ..... DC~5MHz
- Instruction cycle ..... 0.8 μs (min.)
- Software compatible with the M5L8085AP
- Pin connection conpatible with the M5L8085AP (except M5M80C85AJ-2)
- Clock generator (with an external crystal)
- Built-in system controller
- Four vectored interrupts (one of which is non-maskable).
- Serial I/O port ..... 1 each
- Decimal, binary, and double precision arithmetic operations
- Low power dissipation
  Operation I_{CC}=15mA (TYP)(V_{CC}=5V, Ta=25 ℃, tc (CLK)=200ns)
  HALT instruction I_{CC}=7mA (TYP)(V_{CC}=5V, Ta=25 ℃, tc (CLK)=200ns)
  Power down I_{CC}=20 μ A (TYP)(V_{CC}=5V, Ta=25 ℃, X_1=tixing on V_{CC})
- Having bus hold circuit on AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$
- Power down in HALT

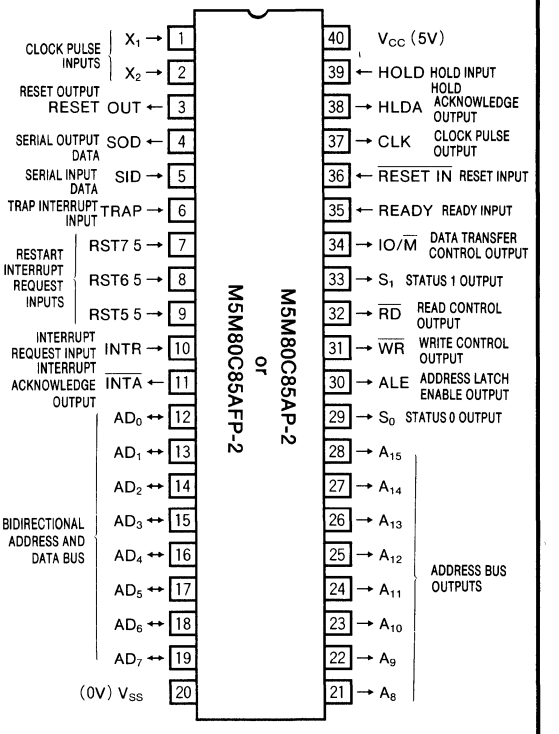
APPLICATION

Central processing unit for a microcomputer

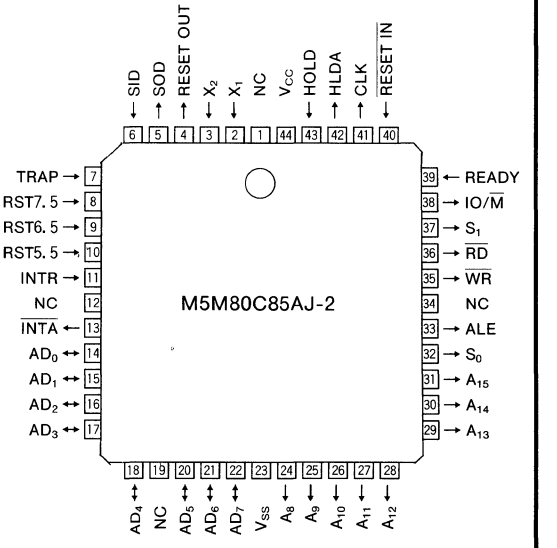
FUNCTION

Under the multiplexed data bus concept adopted, the high-order 8-bit of the address are used only as an adress bus and the low-order 8-bit are used as an address/data bus. During the first clock cycle of an instruction cycle, the address is transferred. The low-order 8-bit of the address are stored in the external latch by the address latch enable (ALE) signal. During the second and third clock cycles, the address/data bus functions as the data bus, transferring the data to memory or to the I/O. For bus control, the device provides $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ signals and an interrupt acknowledge signal ($\overline{INTA}$). The HOLD, READY and all interrupt signals are synchronized with the clock pulse. For simple serial data transfer it provides both a serial input data (SID) line and a serial output data (SOD) line. It also has three maskable restart interrupts and one non-maskable trap interrupt.

PIN CONFIGURATION (TOP VIEW)



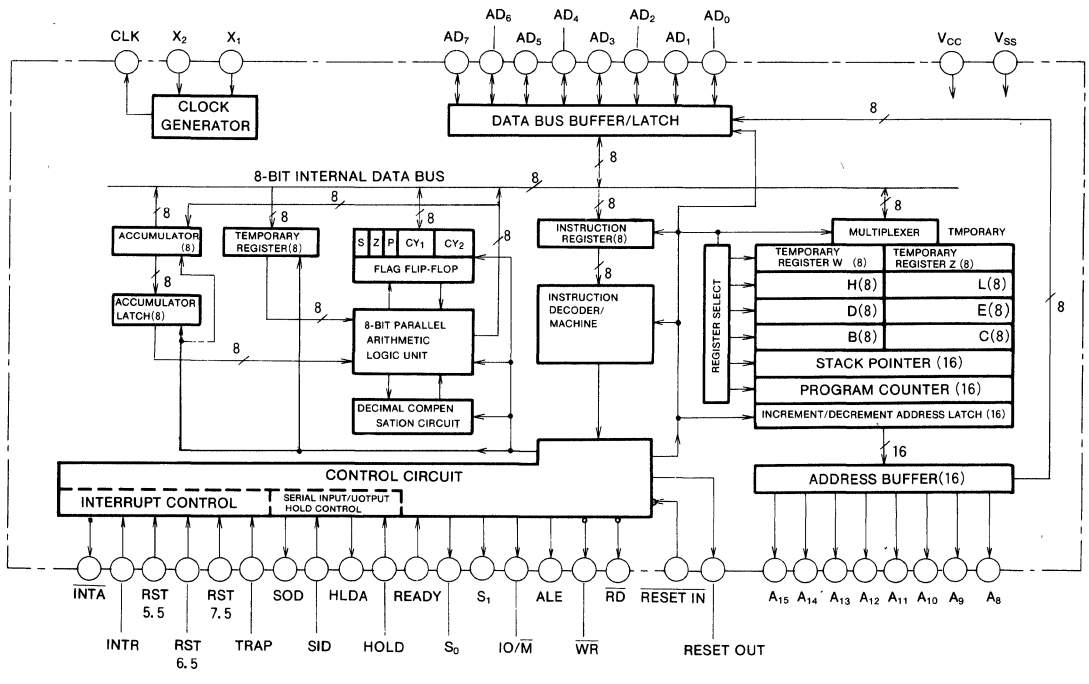
Outline 40P4 (M5M80C85AP-2)
40P2R (M5M80C85AFP-2)



Outline 44P0

NC : NO CONNECTION

BLOCK DIAGRAM



ADDITIONAL FUNCTIONS OF M5M80C85AP-2

M5M80C85AP-2 has the following additional functions to the ones of M5L8085AP (NMOS).

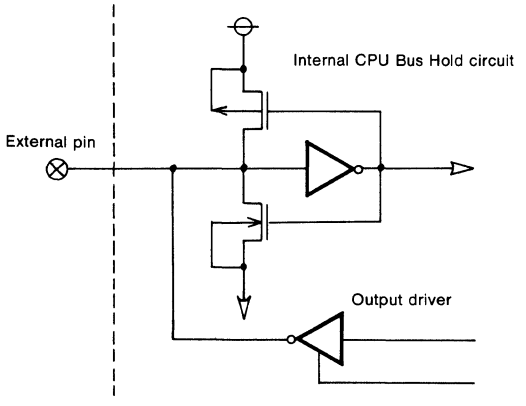
(1) POWER DOWN IN HALTING

After the execution of the HALT instruction, the CPU enters in the power down mode. In the power down mode, the internal clock is stopped. And the internal power dissipation is minimized. All internal status (registers, latches, ·····) is reserved, and the clock output is not stopped in this mode.
To exit the power down mode, RESET input or interrupt signal input is needed. These signals activate the internal clock signal and the power down mode is released.

(2) BUS HOLD CIRCUIT

M5M80C85AP-2 has the bus hold circuit. It holds the output pins H-level or L-level when the output buffer goes to the tri-state. If the input voltage is equal to the threthold voltage of the CMOS device, the large current flows through the P-channel transistor and N-channel transistor.
The addition of this circuit prevents the pass through current of the input circuit of M5M80C85AP-2 and the CMOS device which is connected with this pin.
This circuit realize the low power system configuration.
Following diagram shows the bus hold circuit.

The I/O or output pins which contain the bus hold circuit are
····· AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$



THE CLOCK INPUT FREQUENCY

M5M80C85AP-2 can operate at DC ~ 5MHz clock rate (input clock is DC~10MHz). As the internal circuits are designed with the static circuit, the clock input can be stopped. So the single step function by the clock input is possible.

PIN DESCRIPTIONS

Pin	Name	Input or output	Functions
X_1, X_2	Clock input	In	These pins are used to connect an external crystal to the internal clock generator An external clock pulse can also be input through X_1
RESET OUT	Reset output	Out	This signal indicates that the CPU is in the reset mode It can be used as a system RESET The signal is synchronised to the processor clock
SOD	Serial output data	Out	This is an output data line for selial data. The output SOD may be set or reset by means of the SIM instruction. It returns to high-level after the RESET.
SID	Serial input data	In	This is an input data line for serial data, and the data on this line is moved to the 7th bit of the accumulator whenever a RIM instruction is executed
TRAP	Trap interrupt	In	A non-maskable restart which is recognized at the same time as an INTR it is not affected by any mask or another interrupt It has the highest interrupt priority
RST5. 5 RST6. 5 RST7. 5	Restart interrupt request	In	Input timing is the same as for INTR for these three signals They all cause an automatic insertion of an internal RESTART RST 7.5 has the highest priority while RST 5.5 has the lowest All three signals have a higher priority than INTR
INTR	Interrupt request signal	In	This signal is for a general purpose interrupt and is sampled only during the last clock cycle of the instruction When an interrupt is acknowledged, the program counter (PC) is held and an $\overline{INTA}$ signal is generated During this cycle, a RESTART or CALL can be inserted to jump to an interrupt service routine. The interrupt request may be enable and disable by means of software But it is disable by the RESET and immeadiately after an accepted interrupt.
$\overline{INTA}$	Interrupt acknowledge control signal	Out	This signal is used instead of $\overline{RD}$ during the instruction cycle after an INTR is accepted
AD_0~AD_7	Bidirectional address and data bus	In/out	The low-order (I/O address) appears during the first clock cycle During the second and third clock cycles, it becomes the data bus It remains in the bus hold state during the HOLD and HALT modes.
A_8~A_{15}	Address bus	Out	Output the high-order 8 bits of the memory address or the 8 bits of the I/O address It remains in the bus hold state during the HOLD and HALT modes.
S_0, S_1	Status	Out	Indicates the status of the bus S_1 S_0 HALT 0 0 WRITE 0 1 READ, DAD 1 0 FETCH 1 1 The S_1 signal can be used as an advanced R/$\overline{W}$ status
ALE	Address latch enable	Out	This signal is generated during the first clock cycle, to enable the address to be latched into the latches of peripherals The falling edge of ALE is guaranteed to latch the address information The ALE can also be used to strobe the status information, but it is kept in the low-level state during bus idle machine cycles
$\overline{WR}$	Write control	Out	Indicates that the data on the data bus is to be written into the selected memory at the falling edge of the signal $\overline{WR}$ It remains the bus hold state during the HOLD and HALT modes
$\overline{RD}$	Read control	Out	Indicates that the selected memory or I/O address is to be read and that the data bus is active for data transfer It remains in the bus hold state during the HOLD and HALT modes.
IO/$\overline{M}$	Data transfer control output	Out	This signal indicates whether the read/write is to memory or to I/O_s It remains in the bus hold state during the HOLD and HALT modes
READY	Ready input	In	When it is at high-level during a read or write cycle, the READY indicates that the memory or peripheral is ready to send or receive date. When the signal is at low-level, the CPU will wait for the signal to turn high-level before completing the read or write cycle
$\overline{RESET\ IN}$	Reset input	In	This signal (at least three clock cycles are necessary) sets the program counter to zero and resets the interrupt enable and HLDA flip-flops None of the other flags or registers (except the instruction register) are affected The CPU is held in the reset mode as long as the signal is applied
CLK	Clock output	Out	Clock pulses are available from this pin when a crystal is used as an input to the CPU
HLDA	Hold acknowledge signal	Out	By this signal the processor acknowledges the HOLD request signal and indicates that it will relinquish the buses in the next clock cycle The signal is returned to the low-level state after the HOLD request is completed The processor resumes the use of the buses one half clock cycle after the signal HLDA gose low-level
HOLD	Hold request signal	In	When the CPU receives a HOLD request It relinquishes the use of the buses as soon as the current machine cycle is completed The CPU can regain the use of buses only after the HOLD state is removed Upon acknowledging the HOLD signal, the address bus, the data bus, $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$ lines are put in the bus hold state

Note : HOLD, READY and all interrupt signals are synchronous with clock signal

STATUS INFORMATION

Status information can be obtained directly from the M5M80C85AP-2. ALE is used as a status strobe. As the status is partially encoded, it informs the user in advance what type of bus transfer is being performed. The IO/$\overline{M}$ cycle status signal is also obtained directly. Decoded S_0 and S_1 signals carry:

	S_1	S_0	
HALT	0	0	
WRITE	0	1	
READ	1	0	(except for second and third machine cycles of DAD instruction)
FETCH	1	1	

S_1 can be used in determining the R/$\overline{W}$ status of all bus transfers.

In the M5M80C85AP-2 the low-order 8 bits of the address are multiplexed with date. When entering the low-order of the address into memory or peripheral latch circuits, the ALE is used as a strobe.

INTERRUPT AND SERIAL I/O

The M5M80C85AP-2 has five interrupt inputs—INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. The three RST inputs, 5.5, 6.5, 7.5, are provided with programmable masks. TRAP has the same function as the restart interrupt, except that it is non-maskable.

When an interrupt is enabled and the corresponding interrupt mask is not set, the three RST interrupts will cause the internal execution of the RST. When non-maskable TRAP is applied, it causes the internal execution of an RST regardless of the state of the interrupt enable or masks. The restart addresses (hexadecimal) of the interrupts are:

Interrupt	Adress
TRAP	24_{16}
RST 5.5	$2C_{16}$
RST 6.5	34_{16}
RST 7.5	$3C_{16}$

Two different types of signal are used for restart interrupts. Both RST 5.5 and RST 6.5 are sensitive to high-level, and are acknowledged in the same timing as INTR. RST 7.5 is sensitive to rising-edge, and existence of a pulse sets the RST 7.5 interrupt request. This condition will be maintained until the request is fulfilled or reset by a SIM or RESET instruction.

Each of the restart interrupts may be masked independently to avoid interrupting the CPU. An interrupt requested by an RST 7.5 will be stored even when its mask is set and the interrupt is disabled. Masks can be changed in a SIM instruction or the RESET. When two enabled interrupts are requested at the same time, the interrupt with the highest priority will be accepted. The TRAP has the highest priority followed in order by RST 7.5, RST 6.5, RST 5.5 and INTR. This priority system dose not take into consideration the priority of an interrupt routine that is already started. In other words, when an RST 5.5 interrupt is reenabled before the termination of the RST 7.5 interrupt routine, it will interrupt the RST 7.5.

The TRAP interrupt is very useful in preventing disastrous errors and bus errors resulting from power failures. The TRAP input is recognized in the same manner as any other interrupt, but it has the highest priority, and is not affected by any flags or masks. The TRAP input can be sensed by both edge and level. TRAP should be maintained high-level until it is acknowledged. But, it will not be acknowledged again unless it turns low-level and high-level again. In this manner, faulty operation due to noise or logic glitches is prevented.

The selial I/O system is also considered to be an interrupt as it is controlled by instructions RIM and SIM. The SID is read by instruction RIM and the SOD data is set by instruction SIM.

BASIC TIMING

The M5M80C85AP-2 is provided with a multiplexed data bus. The ALE is utilized as a strobe with which the low-order 8 bits of the address on the data bus are sampled. Fig.1 shows the basic cycle in which an out instruction is fetched, and memory is read and written to the I/O port. The I/O port address is stored in both the address bus and the address/data bus during the I/O write and read cycle. To enable the M5M80C85AP-2 to be used with a slow memory, the READY line is used for extending the read and write pulse width.

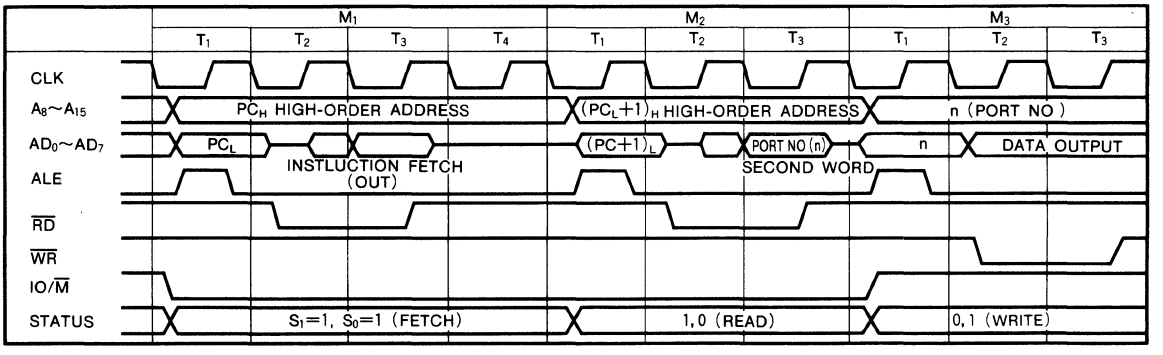


Fig. 1 Basic cycle

MACHINE INSTRUCTIONS

Item: Instr class	Mnemonic	Instruction code D7 D6 D5 D4 D3 D2 D1 D0	16mal notatn	No. of states	No. of bytes	No. of cycles	Functions	Flags S Z P CY2 CY1	Address bus: Contents	Address bus: Mach cycle*	Data bus: Contents	Data bus: I/O	Data bus: Mach cycle**
Data transfer	MOV r1, r2	0 1 D D D S S S		4	1	1	(r1) ← (r2)	X X X X X					
	MOV M, r	0 1 1 1 0 S S S		7	1	2	(M) ← (r) Where, M = (H) (L)	X X X X X	M	M4	(r)	O	M4
	MOV r, M	0 1 D D D 1 1 0		7	1	2	(r) ← (M) Where, M = (H) (L)	X X X X X	M	M4	(M)	I	M4
	MVI r, n	0 0 D D D 1 1 0 <B2>		7	2	2	(r) ← n	X X X X X			<B2>	I	M4
	MVI M, n	0 0 1 1 0 1 1 0 <B2>	3 6	10	2	3	(M) ← n Where, M = (H) (L)	X X X X X	M	M5	<B2>	I	M5
	LXI B, m	0 0 0 0 0 0 0 1 <B2> <B3>	0 1	10	3	3	(C) ← <B2> (B) ← <B3> Where, m = <B3> <B2>	X X X X X			<B2> <B3>	I I	M2 M3
	LXI D, m	0 0 0 1 0 0 0 1 <B2> <B3>	1 1	10	3	3	(E) ← <B2> (D) ← <B3> Where, m = <B3> <B2>	X X X X X			<B2> <B3>	I I	M2 M3
	LXI H, m	0 0 1 0 0 0 0 1 <B2> <B3>	2 1	10	3	3	(L) ← <B2> (H) ← <B3> Where, m = <B3> <B2>	X X X X X			<B2> <B3>	I I	M2 M3
	LXI SP, m	0 0 1 1 0 0 0 1 <B2> <B3>	3 1	10	3	3	(SP) ← m	X X X X X			<B2> <B3>	I I	M2 M3
	SPHL	1 1 1 1 1 0 0 1	F 9	6	1	1	(SP) ← (H) (L)	X X X X X					
	STAX B	0 0 0 0 0 0 1 0	0 2	7	1	2	((B) (C)) ← (A)	X X X X X	(B) (C)	M4	(A)	O	M4
	STAX D	0 0 0 1 0 0 1 0	1 2	7	1	2	((D) (E)) ← (A)	X X X X X	(D) (E)	M4	(A)	O	M4
	LDAX B	0 0 0 0 1 0 1 0	0 A	7	1	2	(A) ← ((B) (C))	X X X X X	(B) (C)	M4	((B) (C))	I	M4
	LDAX D	0 0 0 1 1 0 1 0	1 A	7	1	2	(A) ← ((D) (E))	X X X X X	(D) (E)	M4	((D) (E))	I	M4
	STA m	0 0 1 1 0 0 1 0 <B2> <B3>	3 2	13	3	4	(m) ← (A)	X X X X X	m	M4	(A)	O	M4
	LDA m	0 0 1 1 1 0 1 0 <B2> <B3>	3 A	13	3	4	(A) ← (m)	X X X X X	m	M4	(m)	I	M4
	SHLD m	0 0 1 0 0 0 1 0 <B2> <B3>	2 2	16	3	5	(m) ← (L) (m + 1) ← (H)	X X X X X	m m + 1	M4 M5	(L) (H)	O O	M4 M5
	LHLD m	0 0 1 0 1 0 1 0 <B2> <B3>	2 A	16	3	5	(L) ← (m) (H) ← (m + 1)	X X X X X	m m + 1	M4 M5	(m) (m + 1)	I I	M4 M5
	XCHG	1 1 1 0 1 0 1 1	E B	4	1	1	(H) (L) ↔ (D) (E)	X X X X X					
	XTHL	1 1 1 0 0 0 1 1	E 3	16	1	5	(H) (L) ↔ ((SP) + 1) ((SP))	X X X X X	(SP) (SP) + 1	M2 M3	((SP)) ((SP) + 1)	I I	M2 M3
Arithmetic logical compare	ADD r	1 0 0 0 0 S S S		4	1	1	(A) ← (A) + (r)	O O O O O					
	ADD M	1 0 0 0 0 1 1 0	8 6	7	1	2	(A) ← (A) + (M) Where, M = (H) (L)	O O O O O	M	M4	(M)	I	M4
	ADI n	1 1 0 0 0 1 1 0 <B2>	C 6	7	2	2	(A) ← (A) + n	O O O O O			<B2>	I	M4
	ADC r	1 0 0 0 1 S S S		4	1	1	(A) ← (A) + (r) + (CY2)	O O O O O					
	ADC M	1 0 0 0 1 1 1 0	8 E	7	1	2	(A) ← (A) + (M) + (CY2) Where M = (H) (L)	O O O O O	M	M4	(M)	I	M4
	ACI n	1 1 0 0 1 1 1 0 <B2>	C E	7	2	2	(A) ← (A) + n + (CY2)	O O O O O			<B2>	I	M4
	DAD B	0 0 0 0 1 0 0 1	0 9	10	1	3	(H) (L) ← (H) (L) + (B) (C)	X X X O X					
	DAD D	0 0 0 1 1 0 0 1	1 9	10	1	3	(H) (L) ← (H) (L) + (D) (E)	X X X O X					
	DAD H	0 0 1 0 1 0 0 1	2 9	10	1	3	(H) (L) ← (H) (L) + (H) (L)	X X X O X					
	DAD SP	0 0 1 1 1 0 0 1	3 9	10	1	3	(H) (L) ← (H) (L) + (SP)	X X X O X					
	SUB r	1 0 0 1 0 S S S		4	1	1	(A) ← (A) − (r)	O O O O O					
	SUB M	1 0 0 1 0 1 1 0	9 6	7	1	2	(A) ← (A) − (M) Where, M = (H) (L)	O O O O O	M	M4	(M)	I	M4
	SUI n	1 1 0 1 0 1 1 0 <B2>	D 6	7	2	2	(A) ← (A) − n	O O O O O			<B2>	I	M4
	SBB r	1 0 0 1 1 S S S		4	1	1	(A) ← (A) − (r) − (CY2)	O O O O O					
	SBB M	1 0 0 1 1 1 1 0	9 E	7	1	2	(A) ← (A) − (M) − (CY2) Where, M = (H) (L)	O O O O O	M	M4	(M)	I	M4
	SBI n	1 1 0 1 1 1 1 0 <B2>	D E	7	2	2	(A) ← (A) − n − (CY2)	O O O O O			<B2>	I	M4
	ANA r	1 0 1 0 0 S S S		4	1	1	(A) ← (A) ∧ (r)	O O O 0 1					
	ANA M	1 0 1 0 0 1 1 0	A 6	7	1	2	(A) ← (A) ∧ (M) Where, M = (H) (L)	O O O 0 1	M	M4	(M)	I	M4
	ANI n	1 1 1 0 0 1 1 0 <B2>	E 6	7	2	2	(A) ← (A) ∧ n	O O O 0 1			<B2>	I	M4
	XRA r	1 0 1 0 1 S S S		4	1	1	(A) ← (A) ∀ (r)	O O O 0 0					
	XRA M	1 0 1 0 1 1 1 0	A E	7	1	2	(A) ← (A) ∀ (M) Where, M = (H) (L)	O O O 0 0	M	M4	(M)	I	M4
	XRI n	1 1 1 0 1 1 1 0 <B2>	E E	7	2	2	(A) ← (A) ∀ n	O O O 0 0			<B2>	I	M4
	ORA r	1 0 1 1 0 S S S		4	1	1	(A) ← (A) ∨ (r)	O O O 0 0					
	ORA M	1 0 1 1 0 1 1 0	B 6	7	1	2	(A) ← (A) ∨ (M) Where, M = (H) (L)	O O O 0 0	M	M4	(M)	I	M4
	ORI n	1 1 1 1 0 1 1 0 <B2>	F 6	7	2	2	(A) ← (A) ∨ n	O O O 0 0			<B2>	I	M4
	CMP r	1 0 1 1 1 S S S		4	1	1	(A) − (r)	O O O O O					
	CMP M	1 0 1 1 1 1 1 0	B E	7	1	2	(A) − (M) Compare, Where, M = (H) (L)	O O O O O	M	M4	(M)	I	M4
	CPI n	1 1 1 1 1 1 1 0 <B2>	F E	7	2	2	(A) − n	O O O O O			<B2>	I	M4
Register increment/decrement	INR r	0 0 D D D 1 0 0		4	1	1	(r) ← (r) + 1	O O O X O					
	INR M	0 0 1 1 0 1 0 0	3 4	10	1	3	(M) ← (M) + 1 Where, M = (H) (L)	O O O X O	M	M4	(M)	I	M4
	DCR r	0 0 D D D 1 0 1		4	1	1	(r) ← (r) − 1	O O O X O					
	DCR M	0 0 1 1 0 1 0 1	3 5	10	1	3	(M) ← (M) − 1 Where M = (H) (L)	O O O X O	M	M4	(M)	I	M4
	INX B	0 0 0 0 0 0 1 1	0 3	6	1	1	(B) (C) ← (B) (C) + 1	X X X X X					
	INX D	0 0 0 1 0 0 1 1	1 3	6	1	1	(D) (E) ← (D) (E) + 1	X X X X X					
	INX H	0 0 1 0 0 0 1 1	2 3	6	1	1	(H) (L) ← (H) (L) + 1	X X X X X					
	INX SP	0 0 1 1 0 0 1 1	3 3	6	1	1	(SP) ← (SP) + 1	X X X X X					
	DCX B	0 0 0 0 1 0 1 1	0 B	6	1	1	(B) (C) ← (B) (C) − 1	X X X X X					
	DCX D	0 0 0 1 1 0 1 1	1 B	6	1	1	(D) (E) ← (D) (E) − 1	X X X X X					
	DCX H	0 0 1 0 1 0 1 1	2 B	6	1	1	(H) (L) ← (H) (L) − 1	X X X X X					
	DCX SP	0 0 1 1 1 0 1 1	3 B	6	1	1	(SP) ← (SP) − 1	X X X X X					
Rotate & shift contents of accumulator	RLC	0 0 0 0 0 1 1 1	0 7	4	1	1	Left shift CY2 ← A7 A6 … A1 A0 ← A7	X X X O X					
	RRC	0 0 0 0 1 1 1 1	0 F	4	1	1	Right shift CY2 → A7 A6 … A1 A0 → CY2	X X X O X					
	RAL	0 0 0 1 0 1 1 1	1 7	4	1	1	Left shift CY2 ← A7 A6 … A1 A0 ← CY2	X X X O X					
	RAR	0 0 0 1 1 1 1 1	1 F	4	1	1	Right shift CY2 → A7 A6 … A1 A0 → CY2	X X X O X					
Accumu compen	CMA	0 0 1 0 1 1 1 1	2 F	4	1	1	(A) ← $\overline{(A)}$	X X X X X					
	DAA	0 0 1 0 0 1 1 1	2 7	4	1	1	Results of binary addition are adjusted to BCD	O O O O O					
Carry set	STC	0 0 1 1 0 1 1 1	3 7	4	1	1	(CY2) ← 1	X X X 1 X					
	CMC	0 0 1 1 1 1 1 1	3 F	4	1	1	(CY2) ← $\overline{(CY2)}$	X X X O X					

* State is T1 ** State is T2

MITSUBISHI ELECTRIC

CMOS 8-BIT PARALLEL MICROPROCESSOR

Item / Instr class	Mnemonic	Instruction code	16mal notatn	No of states	No of bytes	No of cycles	Functions	Flags S Z P CY2 CY1	Address bus Contents	Address bus Mach cycle*	Data bus Contents	Data bus I/O	Data bus Mach cycle**
Jump	JMP m	1 1 0 0 0 0 1 1 <B2> <B3>	C3	10	3	3	(PC)←m	X X X X X			<B2> <B3>	I I	M2 M3
	PCHL	1 1 1 0 1 0 0 1	E9	6	1	1	(PC)←(H)(L)	X X X X X					
	JC m	1 1 0 1 1 0 1 0 <B2> <B3>	DA	10/7	3	3/2	(CY2)=1	X X X X X	If condition is true		<B2> <B3>	I I	M2 M3
	JNC m	1 1 0 1 0 0 1 0 <B2> <B3>	D2	10/7	3	3/2	(CY2)=0 If condition is true (PC)←m	X X X X X					
	JZ m	1 1 0 0 1 0 1 0 <B2> <B3>	CA	10/7	3	3/2	(Z)=1	X X X X X			<B2> <B3>	I I	M2 M3
	JNZ m	1 1 0 0 0 0 1 0 <B2> <B3>	C2	10/7	3	3/2	(Z)=0	X X X X X					
	JP m	1 1 1 1 0 0 1 0 <B2> <B3>	F2	10/7	3	3/2	(S)=0 If condition is false (PC)←(PC)+3	X X X X X					
	JM m	1 1 1 1 1 0 1 0 <B2> <B3>	FA	10/7	3	3/2	(S)=1	X X X X X					
	JPE m	1 1 1 0 1 0 1 0 <B2> <B3>	EA	10/7	3	3/2	(P)=1	X X X X X					
	JPO m	1 1 1 0 0 0 1 0 <B2> <B3>	E2	10/7	3	3/2	(P)=0	X X X X X					
Subroutine call	CALL m	1 1 0 0 1 1 0 1 <B2> <B3>	CD	18	3	5	((SP)−1)((SP)−2)←(PC)+3 (PC)←m	X X X X X			<B2> <B3>	I I	M2 M3
							(SP)←(SP)−2		(SP)−1	M4	(PC)+3	O	M4
	RST n	1 1 A A A 1 1 1		12	1	3	((SP)−1)((SP)−2)←(PC)+1 (PC)←n×8, (SP)←(SP)−2 Where 0≦n≦7	X X X X X	(SP)−2	M5	(PC)+3	O	M5
									(SP)−1	M4	(PC)+1	O	M4
									(SP)−2	M5	(PC)+1	O	M5
	CC m	1 1 0 1 1 1 0 0 <B2> <B3>	DC	18/9	3	5/2	(CY2)=1	X X X X X					
	CNC m	1 1 0 1 0 1 0 0 <B2> <B3>	D4	18/9	3	5/2	(CY2)=0 If condition is true	X X X X X	If condition is true				
	CZ m	1 1 0 0 1 1 0 0 <B2> <B3>	CC	18/9	3	5/2	(Z)=1 ((SP)−1)((SP)−2)←(PC)+3 (PC)←m	X X X X X			<B2> <B3>	I I	M2 M3
									(SP)−1	M4	(PC)+3	O	M4
	CNZ m	1 1 0 0 0 1 0 0 <B2> <B3>	C4	18/9	3	5/2	(Z)=0 (SP)←(SP)−2	X X X X X	(SP)−2	M5	(PC)+3	O	M5
	CP m	1 1 1 1 0 1 0 0 <B2> <B3>	F4	18/9	3	5/2	(S)=0	X X X X X					
	CM m	1 1 1 1 1 1 0 0 <B2> <B3>	FC	18/9	3	5/2	(S)=1 If condition is false (PC)←(PC)+3	X X X X X					
	CPE m	1 1 1 0 1 1 0 0 <B2> <B3>	EC	18/9	3	5/2	(P)=1	X X X X X					
	CPO m	1 1 1 0 0 1 0 0 <B2> <B3>	E4	18/9	3	5/2	(P)=0	X X X X X					
Return	RET	1 1 0 0 1 0 0 1	C9	10	1	3	(PC)←((SP)+1)((SP)) (SP)←(SP)+2	X X X X X	(SP)	M4	((SP))	I	M4
									(SP)+1	M5	((SP)+1)	I	M5
	RC	1 1 0 1 1 0 0 0	D8	12/6	1	3/1	(CY2)=1 If condition is true	X X X X X	If condition is true				
	RNC	1 1 0 1 0 0 0 0	D0	12/6	1	3/1	(CY2)=0	X X X X X					
	RZ	1 1 0 0 1 0 0 0	C8	12/6	1	3/1	(Z)=1 (PC)←((SP)+1)((SP))	X X X X X	(SP)	M4	((SP))	I	M4
	RNZ	1 1 0 0 0 0 0 0	C0	12/6	1	3 1	(Z)=0 (SP)←(SP)+2	X X X X X	(SP)+1	M5	((SP)+1)	I	M5
	RP	1 1 1 1 0 0 0 0	F0	12/6	1	3/1	(S)=0	X X X X X					
	RM	1 1 1 1 1 0 0 0	F8	12/6	1	3/1	(S)=1 If condition is false	X X X X X					
	RPE	1 1 1 0 1 0 0 0	E8	12/6	1	3/1	(P)=1 (PC)←(PC)+1	X X X X X					
	RPO	1 1 1 0 0 0 0 0	E0	12/6	1	3/1	(P)=0	X X X X X					
Input/ output control	IN n	1 1 0 1 1 0 1 1 <B2>	DB	10	2	3	(A)←(Input buffer)←(Input device of number n) (Input data)	X X X X X			<B2>	O	M4
	OUT n	1 1 0 1 0 0 1 1 <B2>	D3	10	2	3	(Output device of number n)←(A)	X X X X X	<B2> B2>	M5	(Input data) <B2>	I O	M5 M4
									<B2> <B2>	M5	(A)	O	M5
Interrupt control	EI	1 1 1 1 1 0 1 1	FB	4	1	1	(INTE)←1	X X X X X					
	DI	1 1 1 1 0 0 1 1	F3	4	1	1	(INTE)←0	X X X X X					
Stack control	PUSH PSW	1 1 1 1 0 1 0 1	F5	12	1	3	((SP)−1)←(A) ((SP)−2)←(F) (SP)←(SP)−2	X X X X X	(SP)−1	M4	(A)	O	M4
									(SP)−2	M5	(F)	O	M5
	PUSH B	1 1 0 0 0 1 0 1	C5	12	1	3	((SP)−1)←(B) ((SP)−2)←(C) (SP)←(SP)−2	X X X X X	(SP)−1	M4	(B)	O	M4
									(SP)−2	M5	(C)	O	M5
	PUSH D	1 1 0 1 0 1 0 1	D5	12	1	3	((SP)−1)←(D) ((SP)−2)←(E) (SP)←(SP)−2	X X X X X	(SP) 1	M4	(D)	O	M4
									(SP)−2	M5	(E)	O	M5
	PUSH H	1 1 1 0 0 1 0 1	E5	12	1	3	((SP)−1)←(H), ((SP)−2)←(L) (SP)←(SP)−2	X X X X X	(SP)−1	M4	(H)	O	M4
									(SP)−2	M5	(L)	O	M5
	POP PSW	1 1 1 1 0 0 0 1	F1	10	1	3	(F)←((SP)) (A)←((SP)+1) (SP)←(SP)+2	O O O O O	(SP)	M4	(SP))	I	M4
									(SP)+1	M5	((SP)+1)	I	M5
	POP B	1 1 0 0 0 0 0 1	C1	10	1	3	(C)←((SP)) (B)←((SP)+1) (SP)←(SP)+2	X X X X X	(SP)	M4	((SP))	I	M4
									(SP)+1	M5	((SP)+1)	I	M5
	POP D	1 1 0 1 0 0 0 1	D1	10	1	3	(E)←((SP)) (D)←((SP)+1) (SP)←(SP)+2	X X X X X	(SP)	M4	((SP))	I	M4
									(SP)+1	M5	((SP)+1)	I	M5
	POP H	1 1 1 0 0 0 0 1	E1	10	1	3	(L)←((SP)) (H)←((SP)+1) (SP)←(SP)+2	X X X X X	(SP)	M4	((SP))	I	M4
									(SP)+1	M5	((SP)+1)	I	M5
Others	HLT	0 1 1 1 0 1 1 0	76	5	1	1	(PC)←(PC)+1	X X X X X					
	NOP	0 0 0 0 0 0 0 0	00	4	1	1	(PC)←(PC)+1	X X X X X					
Mask set instructions	RIM	0 0 1 0 0 0 0 0	20	4	1	1	All RST interrupt masks, any pending RST interrupt requests and the serial input data from the SID pin are read into the accumulator	X X X X X					
	SIM	0 0 1 1 0 0 0 0	3	4	1	1	Mask is enabled (or disabled) to the RST interrupt corresponding to the contents (bit pattern) of the accumulator. The serial output is enabled and the serial output bit is loaded into the SOD latch	X X X X X					

* State is T_1 **. State is T_2

MACHINE INSTRUCTIONS SYMBOL MEANING

Symbol	Meaning
r	Register
m	Two-byte data
n	One-byte data
<B2>	Second byte of instruction
<B3>	Third byte of instruction
AAA	Binary representation for RST instruction n
F	8-bit data from the most to the least significant bit S, Z, X, CY1, 0, P, X, CY2 (X is indefinite)
PC	Program counter
SP	Stack pointer

Symbol	Meaning
S S S or D D D	Bit pattern designating register or memory Where M = (H) (L)

Register or memory	S S S or D D D
B	0 0 0
C	0 0 1
D	0 1 0
E	0 1 1
H	1 0 0
L	1 0 1
M	1 1 0
A	1 1 1

Symbol	Meaning
←	Data is transferred in direction shown
( )	Contents of register or memoy location
V	Inclusive OR
⊻	Exclusive OR
∧	Logical AND
$\overline{\ }$	1 s complement
X	Content of flag is not changed after execution
O	Content offlag is set or reset after execution
I	Input mode
O	Output mode

INSTRUCTION CODE LIST

$D_3 \sim D_0$ \ $D_7 \sim D_4$	Hex-adecimal notation	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	NOP	(—)	RIM	SIM	MOV B, B	MOV D, B	MOV H, B	MOV M, B	ADD B	SUB B	ANA B	ORA B	RNZ	RNC	RPO	RP
0001	1	LXI B	LXI D	LXI H	LXI SP	MOV B, C	MOV D, C	MOV H, C	MOV M, C	ADD C	SUB C	ANA C	ORA C	POP B	POP D	POP H	POP PSW
0010	2	STAX B	STAX D	SHLD	STA	MOV B, D	MOV D, D	MOV H, D	MOV M, D	ADD D	SUB D	ANA D	ORA D	JNZ	JNC	JPO	JP
0011	3	INX B	INX D	INX H	INX SP	MOV B, E	MOV D, E	MOV H, E	MOV M, E	ADD E	SUB E	ANA E	ORA E	JMP	OUT	XTHL	DI
0100	4	INR B	INR D	INR H	INR M	MOV B, H	MOV D, H	MOV H, H	MOV M, H	ADD H	SUB H	ANA H	ORA H	CNZ	CNC	CPO	CP
0101	5	DCR B	DCR D	DCR H	DCR M	MOV B, L	MOV D, L	MOV H, L	MOV M, L	ADD L	SUB L	ANA L	ORA L	PUSH B	PUSH D	PUSH H	PUSH PSW
0110	6	MVI B	MVI D	MVI H	MVI M	MOV B, M	MOV D, M	MOV H, M	HLT	ADD M	SUB M	ANA M	ORA M	ADI	SUI	ANI	ORI
0111	7	RLC	RAL	DAA	STC	MOV B, A	MOV D, A	MOV H, A	MOV M, A	ADD A	SUB A	ANA A	ORA A	RST 0	RST 2	RST 4	RST 6
1000	8	(—)	(—)	(—)	(—)	MOV C, B	MOV E, B	MOV L, B	MOV A, B	ADC B	SBB B	XRA B	CMP B	RZ	RC	RPE	RM
1001	9	DAD B	DAD D	DAD H	DAD SP	MOV C, C	MOV E, C	MOV L, C	MOV A, C	ADC C	SBB C	XRA C	CMP C	RET	(—)	PCHL	SPHL
1010	A	LDAX B	LDAX D	LHLD	LDA	MOV C, D	MOV E, D	MOV L, D	MOV A, D	ADC D	SBB D	XRA D	CMP D	JZ	JC	JPE	JM
1011	B	DCX B	DCX D	DCX H	DCX SP	MOV C, E	MOV E, E	MOV L, E	MOV A, E	ADC E	SBB E	XRA E	CMP E	(—)	IN	XCHG	EI
1100	C	INR C	INR E	INR L	INR A	MOV C, H	MOV E, H	MOV L, H	MOV A, H	ADC H	SBB H	XRA H	CMP H	CZ	CC	CPE	CM
1101	D	DCR C	DCR E	DCR L	DCR A	MOV C, L	MOV E, L	MOV L, L	MOV A, L	ADC L	SBB L	XRA L	CMP L	CALL	(—)	(—)	(—)
1110	E	MVI C	MVI E	MVI L	MVI A	MOV C, M	MOV E, M	MOV L, M	MOV A, M	ADC M	SBB M	XRA M	CMP M	ACI	SBI	XRI	CPI
1111	F	RRC	RAR	CMA	CMC	MOV C, A	MOV E, A	MOV L, A	MOV A, A	ADC A	SBB A	XRA A	CMP A	RST 1	RST 3	RST 5	RST 7

This list shows the machine codes and corresponding machine instruction. $D_3 \sim D_0$ indicate the low-order 4 bits of the machine code and $D_7 \sim D_4$ indicate the high-order 4 bits. Hexadecimal numbers are also used to indicate this code. The instruction may consists of 1, 2, or 3-byte, but only the first byte is listed.

□ indicates a 3-byte instruction.

▨ indicates a 2-byte instruction.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3~7	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		−0.3~V_{CC}+0.3	V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current.	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current.	2.5	mA
Topr	Operating free-air temperature range		−20~75	℃
Tstg	Storge temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=−20~75℃unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (Ta=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{IHX}	X_1, X_2 High-level voltage		4.0		V_{CC}+0.3	V
$V_{IH(\overline{RESIN})}$	High-level reset input voltage		2.4		V_{CC}+0.3	V
$V_{IL(\overline{RESIN})}$	Low-level reset input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
		I_{OH}=−20μA	4.4			
V_{OL}	Low-level output voltage	I_{OL}=2mA			0.45	V
I_{CC}	Supply current from (Operation)			15	20	mA
	Supply current from V_{CC} (HALT)			7	10	mA
I_{CCS}	Supply current from V_{CC} (Stand by)	(Note 1)		20	30	μA
I_I	Input leak current	V_I=0V, V_{CC}	−10		10	μA
I_{OZ}	Off-state output current	V_O=0V~V_{CC}	−10		10	μA
I_{BHH}	Input current bus hold high	V_I=3.0V (Note 2)	−50		−400	μA
I_{BHL}	Input current bus hold low	V_I=0.8V (Note 3)	50		400	μA
C_i	Input terminal capacitance	V_{CC}=V_{SS}, f=1MHz 25mVrms, T_a=25℃ (Note 4)			10	pF
C_O	Output terminal capacitance	V_{CC}=V_{SS}, f=1MHz 25mVrms, T_a=25℃ (Note 4)			15	pF
$C_{I/O}$	Input/Output terminal capacitance	V_{CC}=V_{SS}, f=1MHz 25mVrms, T_a=25℃ (Note 4)			20	pF

Note 1 : I_{CCS} should be measured after execution HALT instruction and then fixing clock on V_{CC} or V_{SS} V_I=V_{CC} or V_{SS}, V_{CC}=5.5V, outputs unloaded.

Note 2 : I_{BHH} should be measured after rasing V_{IN} in bushold status to V_{CC} and setting it for 3.0V. Measurable pins ; AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$

Note 3 : I_{BHL} should be measured after lowering V_{IN} in bushold status to V_{SS} and setting it for 0.8V. Measurable pins ; AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$

Note 4 : Unmeasured pins should be connected to V_{SS}.

TIMING REQUIREMENTS (Ta=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

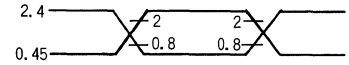
Symbol	Paramater	Test condtions	Limits			Unit
			Min	Typ	Max	
$t_{C(CLK)}$	Clock cycle time	$t_{C(CLK)}$≧200ns, C_L=150pF	200		DC	ns
$t_{su(DA-AD)}$	DA input setup time		−350			ns
$t_{su(DA-\overline{RD})}$	DA input setup time		−150			ns
$t_{h(DA-\overline{RD})}$	DA input hold time		0			ns
$t_{su(RDY-AD)}$	READY input setup time		−100			ns
$t_{su(RDY-CLK)}$	READY input setup time				−100	ns
$t_{h(RDY-CLK)}$	READY input hold time		0			ns
$t_{su(DA-ALE)}$	DA input setup time		−270			ns
$t_{su(HLD-CLK)}$	HOLD input setup time		120			ns
$t_{h(HLD-CLK)}$	HLD input hold time		0			ns
$t_{su(INT-CLK)}$	Interrupt setup time		150			ns
$t_{h(INT-CLK)}$	Interrupt hold time		0			ns
$t_{su(RDY-ALE)}$	READY input setup time		−30			ns

SWITCHING CHARACTERISTICS (Ta=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{W(\overline{CLK})}$	CLK output low-level pulse width		$t_{C(CLK)}$≧200ns, C_L=150pF	40			ns
$t_{W(CLK)}$	CLK output high-level pulse width			70			ns
$t_{r(CLK)}$	CLK output rise time					30	ns
$t_{f(CLK)}$	CLK output fall time					30	ns
$t_{d(X1-CLK)}$	Delay time, X_I to CLK			20		100	ns
$t_{d(X1-\overline{CLK})}$	Delay time, X_I to $\overline{CLK}$			25		110	ns
$t_{d(AD-ALE)}$	Delay time, address output to ALE signal	AD_0~AD_7		50			ns
		A_8~A_{15}		50			
$t_{d(ALE-AD)}$	Delay time, ALE signal to address output			50			ns
$t_{W(ALE)}$	ALE pulse width			80			ns
$t_{d(ALE-CLK)}$	Delay time, ALE to CLK			50			ns
$t_{d(ALE-\overline{CONT})}$	Delay time, ALE to control signal			60			ns
$t_{DXZ(\overline{RD}-AD)}$	Address disable time from read					0	ns
$t_{DZX(\overline{RD}-AD)}$	Address enable time from read			90			ns
$t_{d(CONT-AD)}$	Address valid time after control signal			60			ns
$t_{d(DA-\overline{WR})}$	Delay time, date output to $\overline{WR}$ signal			230			ns
$t_{d(\overline{WR}-DA)}$	Delay time, $\overline{WR}$ signal to data output			60			ns
$t_{W(\overline{CONT})}$	Control signal pulse width			230			ns
$t_{d(CONT-ALE)}$	Delay time, CLK to ALE signal			25			ns
$t_{d(CLK-HLDA)}$	Delay time, CLK to HLDA signal			40			ns
$t_{DXZ(HLDA-BUS)}$	Bus disable time from HLDA					150	ns
$t_{DZX(HLDA-BUS)}$	Control signal disable time					150	ns
$t_{d(CONT-\overline{CONT})}$	Control signal disable time			220			ns
$t_{d(AD-\overline{CONT})}$	Delay time, address output to control signal	AD_0~AD_7		115			ns
		A_8~A_{15}		115			
$t_{d(ALE-DA)}$	Delay time, ALE to data output					140	ns
$t_{d(WRHL-DA)}$	Delay time, $\overline{WR}$ signal to data output					20	ns

Note 5 : A. C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	10ns
Input pulse fall time	10ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V



Parameters described in the timing requirements and switching characteristics take relevant values in accordance with the relational expression shown in the following tables when the frequency is varied.

Relational expression with the frequency T ($t_{C(CLK)}$) in the M5M80C85AP-2

TIMMING REQUIREMENTS (Ta=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Relational expression (Note 6)	Limit
$t_{su(DA-AD)}$	DA input setup time	C_L = 150pF	170−(5/2+N)T	Min
$t_{su(DA-\overline{RD})}$	DA input setup time		150−(3/2+N)T	Min
$t_{su(RDY-AD)}$	READY input setup time		200−(3/2)T	Min
$t_{su(DA-ALE)}$	DA input setup time		150−(2+N)T	Min

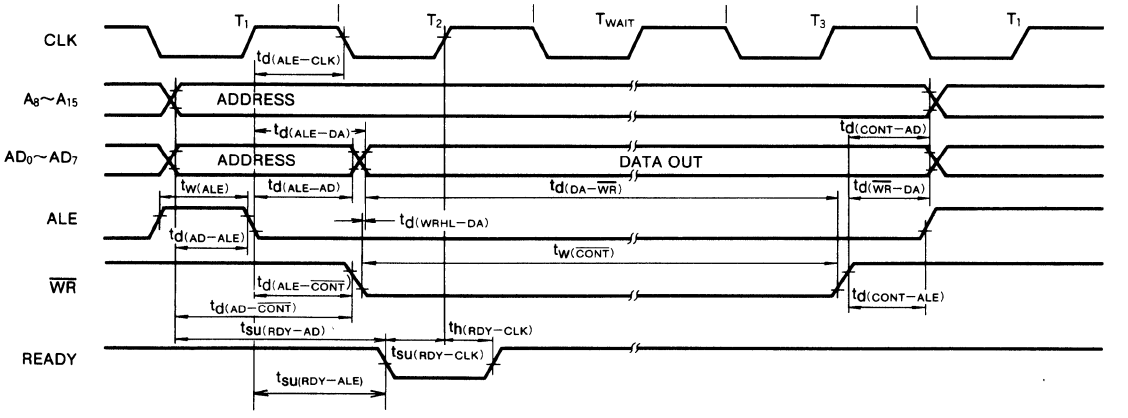
SWITCHING CHARACTERISTICS (Ta=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Palameter		Test conditions	Relational expression (Note 6)	Limit
$t_{w(\overline{CLK})}$	CLK output low-level pulse width		C_L=150pF	(1/2)T−60	Min
$t_{w(CLK)}$	CLK output high-level pulse width			(1/2)T−30	Min
$t_{d(AD-ALE)}$	Delay time, address output to ALE signal	AD_0~AD_7		(1/2)T−50	Min
		A_8~A_{15}		(1/2)T−50	
$t_{d(ALE-AD)}$	Delay time, ALE signal to address output			(1/2)T−50	Min
$t_{w(ALE)}$	ALE pulse width			(1/2)T−20	Min
$t_{d(ALE-CLK)}$	Delay time, ALE to CLK			(1/2)T−50	Min
$t_{d(ALE-\overline{CONT})}$	Delay time, ALE to control signal			(1/2)T−40	Min
$t_{DZX(\overline{RD}-AD)}$	Address enable time from read			(1/2)T−10	Min
$t_{d(CONT-AD)}$	Address valid time after control signal			(1/2)T−40	Min
$t_{d(DA-\overline{WR})}$	Delay time, data output to $\overline{WR}$ signal			(3/2+N)T−70	Min
$t_{d(\overline{WR}-DA)}$	Delay time $\overline{WR}$ signal to data output			(1/2)T−40	Min
$t_{w(\overline{CONT})}$	Control signal pulse width			(3/2+N)T−70	Min
$t_{d(CONT-ALE)}$	Delay time, CONT to ALE signal			(1/2)T−75	Min
$t_{d(CLK-HLDA)}$	Delay time, CLK to HLDA signal			(1/2)T−60	Min
$t_{DXZ(HLDA-BUS)}$	Bus disable time from HLDA			(1/2)T+50	Max
$t_{DZX(HLDA-BUS)}$	Bus enable time from HLDA			(1/2)T+50	Max
$t_{d(CONT-\overline{CONT})}$	Control signal disable time			(3/2)T−80	Min
$t_{d(AD-\overline{CONT})}$	Delay time, address output to control signal	AD_0~AD_7		T−85	Min
		A_8~A_{15}		T−85	

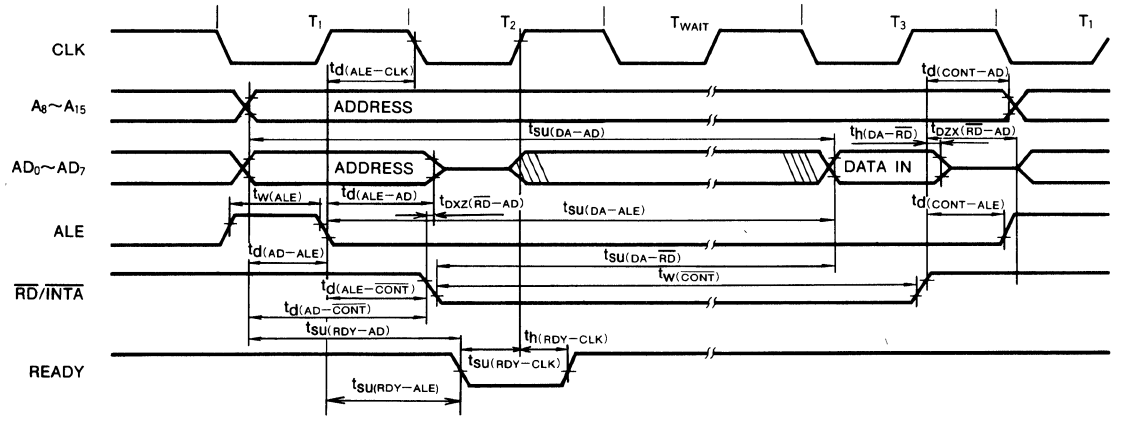
Note 6 N indicates the total number of wait cycles
T=$t_{C(CLK)}$

TIMING DIAGRAM

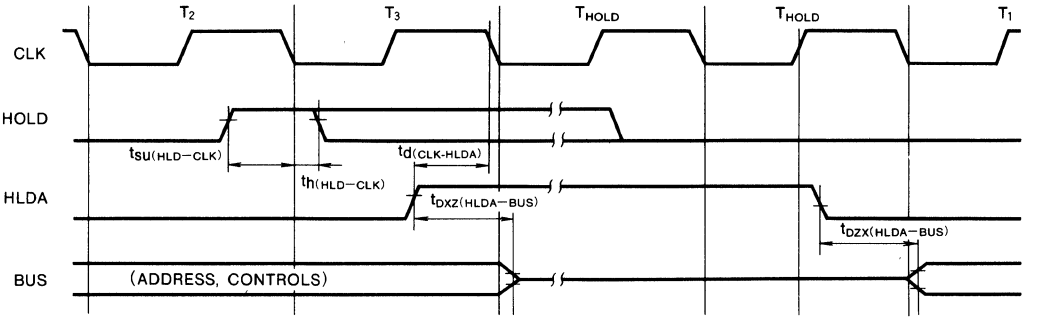
Write Cycle



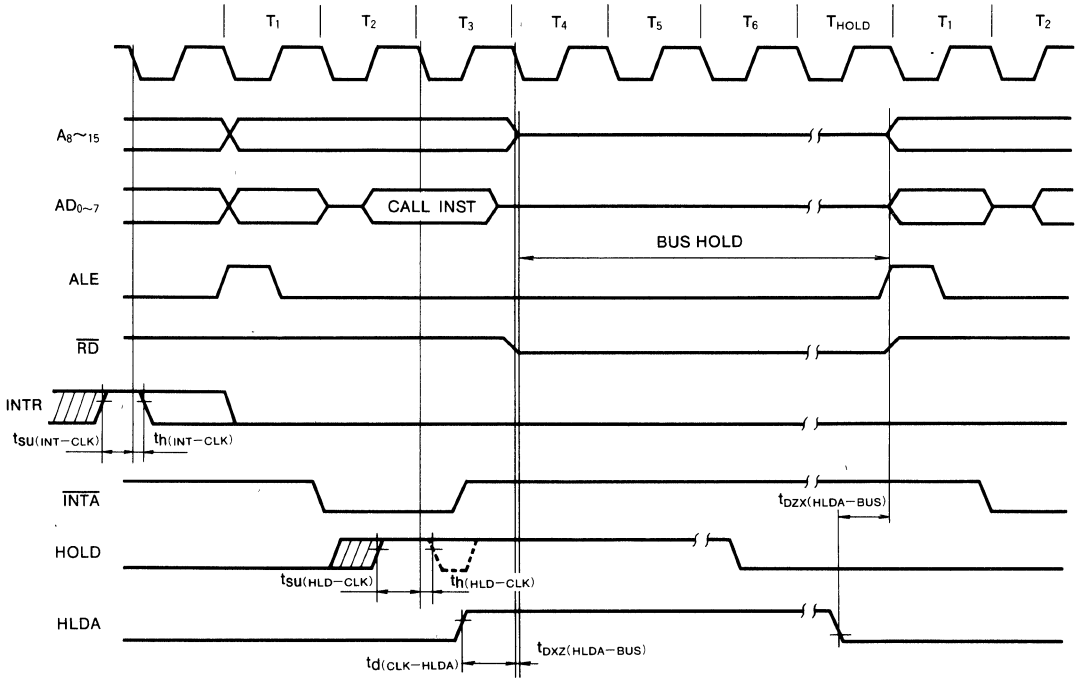
Read Cycle



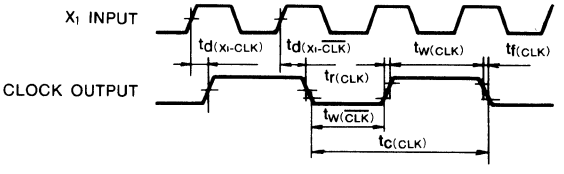
Hold Cycle



Interrupt and Hold Cycle



Clock Output Timing Waveform



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TRAP INTERRUPT AND RIM INSTRUCTIONS

TRAP generates interrupts regardless of the interrupt enable filp-flop (INTE FF). The current state of the INTE FF is stored in flip flop A (A FF) of the CPU and then the INTE FF is reset. The first RIM instruction after the generation of a TRAP interrupt differs in function from the ordinary RIM instruction. That is, the bit 3 (INTE FF information) in the accumulator ($(A)_3$) after the execution of the RIM instruction contains the contents of the A FF, regardless of the state of the INTE FF at the time the RIM instruction is executed. These details are shown in Figs.2 and 3, Table 1 .

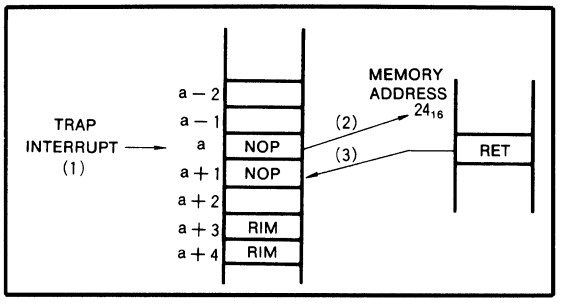


Fig. 2 TRAP interrupt processing

Below are the explanations of Fig. 2 .

1. The TRAP interrupt request is issued while the instruction in address a is being executed.
2. The TRAP interrupt causes the same action as an RST instruction and then jumps to address 24_{16}.
3. It returns to address a+1 after executing the RET instruction.

Table 1 shows the information in the INTE FF at address a+3 and a+4 when the instructions EI and/or DI are executed at addresses a−1 and a+2.

Fig. 4 is a flow chart of the TRAP interrupt processing routine.

Table 1 TRAP interrupt and RIM instructions

Condition \ Number	1	2	3	4	5	6
Instruction in address a-1	EI	EI	EI	DI	DI	DI
Instruction in address a+2	EI	NOP	DI	EI	NOP	DI
Contents of $(A)_3$ after the execution of the RIM instruction in address a+3	1	1	1	0	0	0
State of INTE FF after the execution of the RIM instruction in address a+3	1	0	0	1	0	0
Contents of $(A)_3$ after the execution of the RIM instruction in address a+4	1	0	0	1	0	0
State of INTE FF after the execution of the RIM instruction in address a+4	1	0	0	1	0	0

Note 7 The contents of $(A)_3$ after the excution of the RIM instruction is an information of the INTE FF The INTE FF assumes state 1 when it is in the EI state, and 0 when it is in the DI state

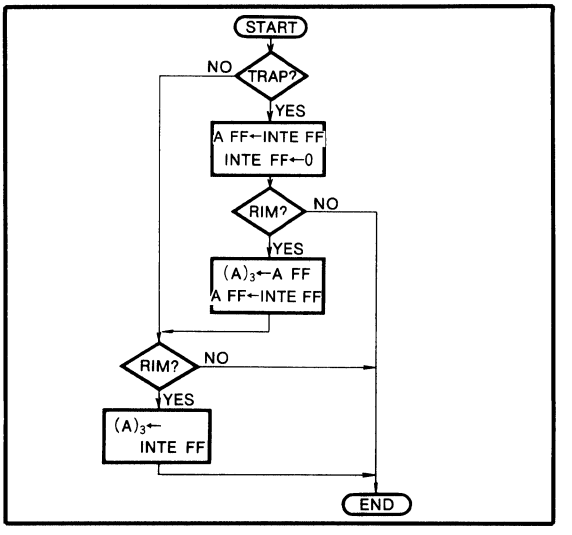


Fig.3 TRAP interrupt and INTE FF processing

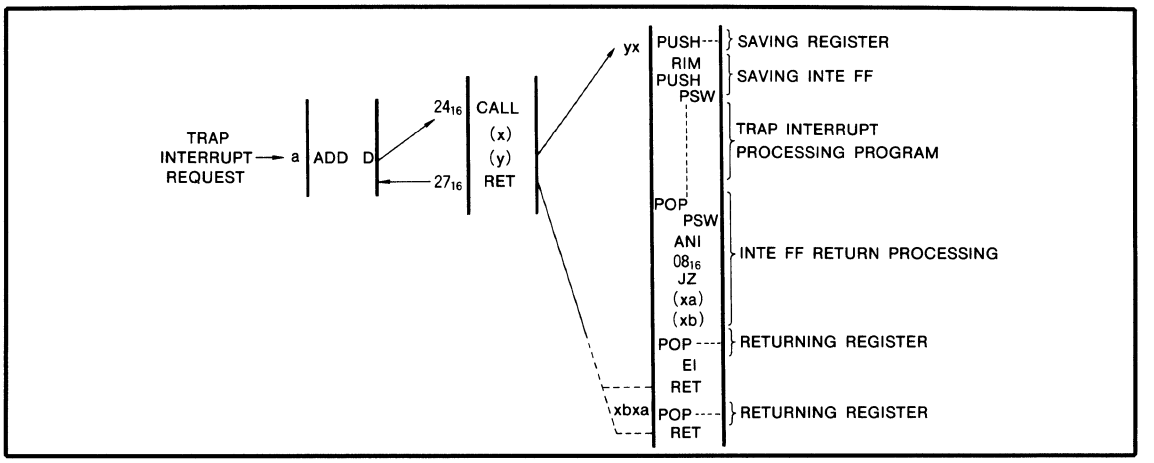


Fig. 4 TRAP interrupt processing routine

DRIVING CIRCUIT OF X_1 AND X_2 INPUTS

Input terminals, X_1 and X_2 of the M5M80C85AP-2 can be driven by either a crystal or external clock. Since the driver clock frequency is divided to 1/2 internally, the input frequency required is twice the actual execution frequency (10MHz for the M5M80C85AP-2 which is operated at 5MHz)

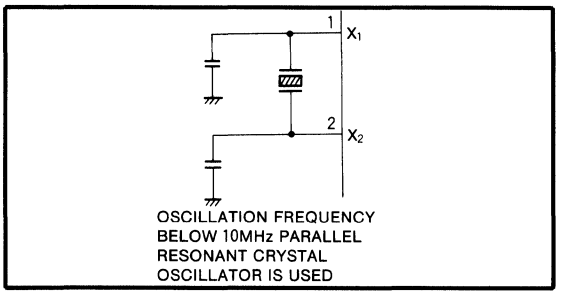
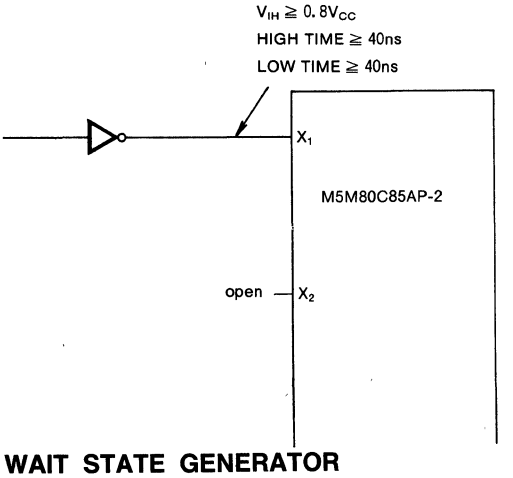


Fig. 5 Connections when crystal is used for X_1 and X_2 inputs

Fig. 5 is a typical connection diagrams for a crystal respectively.

External Clock Driver Circuit



WAIT STATE GENERATOR

Fig. 6 shows a typical 1-wait state generator for low speed RAM and ROM applications.

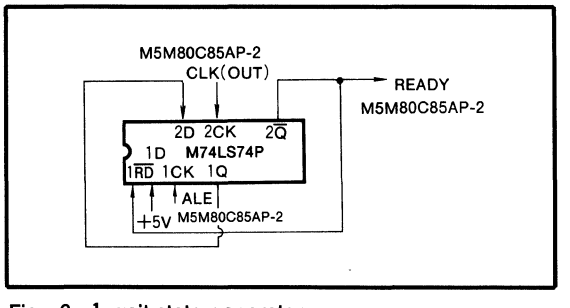


Fig. 6 1-wait state generator

RELATION OF RIM AND SIM INSTRUCTIONS WITH THE ACCUMULATOR (SUPPLEMENTARY DESCRIPTION).

The contents of the accumulator after the execution of a RIM instruction is shown in Fig. 7 .

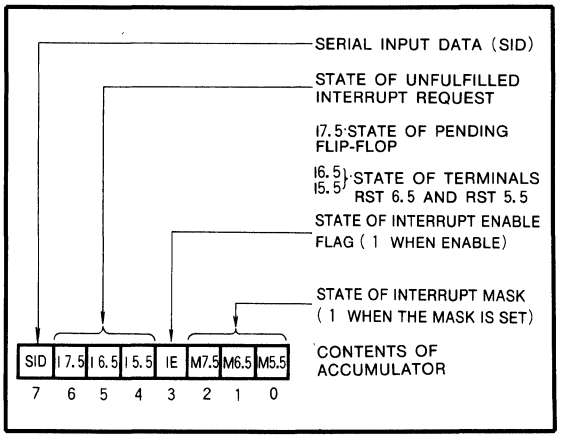


Fig.7 Relation of the SIM instruction RIM with the accumulator

The contents of the accumulator after the execution of a SIM instruction is shown in Fig. 8 .

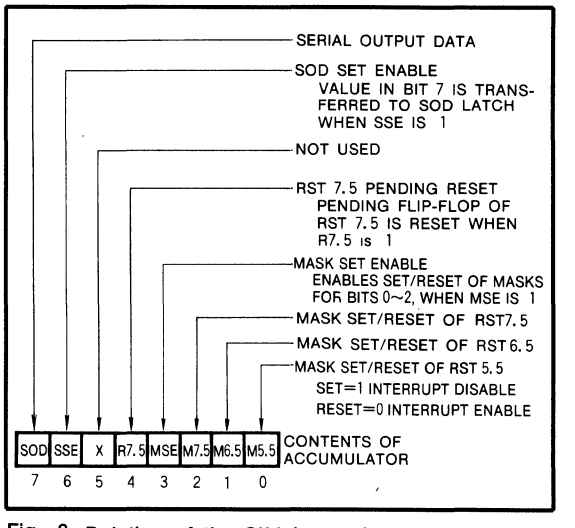


Fig. 8 Relation of the SIM instruction with the accumulator

M5L8085AP

8-BIT PARALLEL MICROPROCESSOR

DESCRIPTION

The M5L8085AP is a family of single-chip 8-bit parallel central processing units (CPUs) developed using the N-channel silicon-gate ED-MOS process. It requires a single 5V power supply and has a basic clock rate of 3MHz.

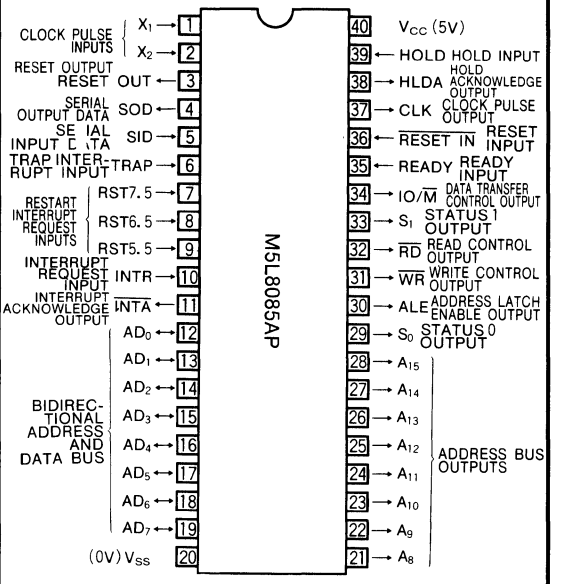
FEATURES

- Single 5V supply voltage
- TTL compatible
- Instruction cycle ..... 1.3 μs (min.)
- Clock generator (with an external crystal or RC circuit)
- Built-in system controller
- Four vectored interrupts (one of which is non-maskable)
- Serial I/O port ..... 1 each
- Decimal, binary, and double precision arithmetic operations
- Direct Addressing capability to 64K bytes of memory

APPLICATION

Central processing unit for a microcomputer

PIN CONFIGURATION (TOP VIEW)

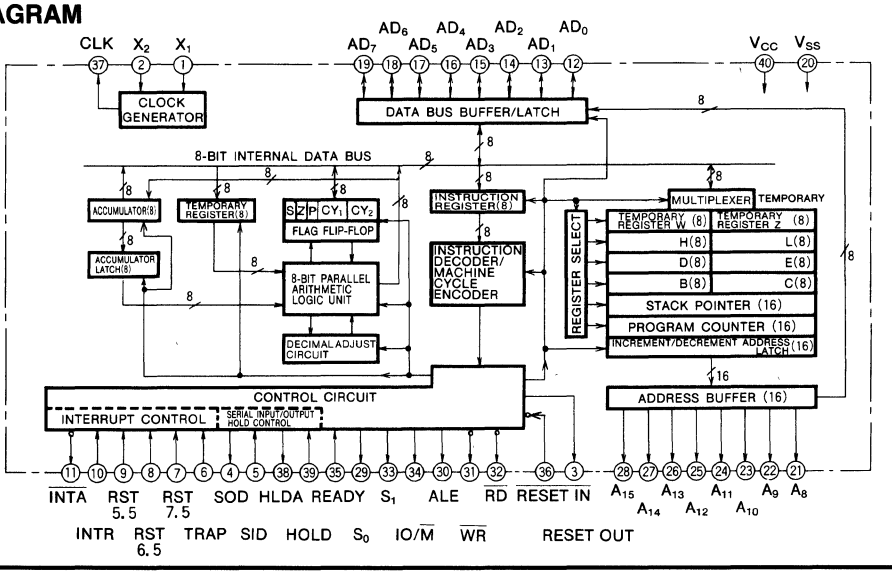


Outline 40P4

FUNCTION

Under the multiplexed data bus concept adopted, the high-order 8 bits of the address are used only as an adress bus and the low-order 8 bits are used as an address/data bus. During the first clock cycle of an instruction cycle, the address is transferred. The low-order 8 bits of the address are stored in the external latch by the address latch enable (ALE) signal. During the second and third clock cycles, the address/data bus functions as the data bus, transferring the data to memory or to the I/O. For bus control, the device provides $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ signals and an interrupt acknowledge signal ($\overline{INTA}$). The HOLD, READY and all interrupt signals are synchronized with the clock pulse. For simple serial data transfer it provides both a serial input data (SID) line and a serial output data (SOD) line. It also has three maskable restart interrupts and one non-maskable trap interrupt.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin	Name	Input or output	Functions
X_1, X_2	Clock input	In	These pins are used to connect an external crystal or RC circuit to the internal clock generator An external clock pulse can also be input through X_1
RESET OUT	Reset output	Out	This signal indicates that the CPU is in the reset mode It can be used as a system RESET The signal is synchronised to the processor clock
SOD	Serial output data	Out	This is an output data line for serial data The output SOD may be set or reset by means of the SIM instruction It returns to high-level after the RESET
SID	Serial input data	In	This is an input data line for serial data, and the data on this line is moved to the 7th bit of the accumulator whenever a RIM instruction is executed.
TRAP	Trap interrupt	In	A non-maskable restart which is recognized at the same time as an INTR it is not affected by any mask or another interrupt It has the highest interrupt priority
RST5. 5 RST6. 5 RST7. 5	Restart interrupt request	In	Input timing is the same as for INTR for these three signals They all cause an automatic insertion of an internal RESTART RST 7. 5 has the highest priority while RST 5. 5 has the lowest All three signals have a higher priority than INTR
INTR	Interrupt request signal	In	This signal is for a general purpose interrupt and is sampled only during the last clock cycle of the instruction When an interrupt is acknowledged, the program counter (PC) is held and an $\overline{INTA}$ signal is generated During this cycle, a RESTART or CALL can be inserted to jump to an interrupt service routine The interrupt request may be enable and disable by means of software But it is disable by the RESET and immeadiately after an accepted interrupt
$\overline{INTA}$	Interrupt acknowledge control signal	Out	This signal is used instead of $\overline{RD}$ during the instruction cycle after an INTR is accepted
AD_0~AD_7	Bidirectional address and data bus	In/out	The low-order (I/O address) appears during the first clock cycle During the second and third clock cycles, it becomes the data bus It remains in the high-impedance state during the HOLD and HALT modes
A_8~A_{15}	Address bus	Out	Output the high-order 8 bits of the memory address or the 8 bits of the I/O address It remains in the high-impedance state during the HOLD and HALT modes
S_0, S_1	Status	Out	Indicates the status of the bus HALT 0 0 WRITE 0 1 READ, DAD 1 0 FETCH 1 1 The S_1 signal can be used as an advanced R/$\overline{W}$ status
ALE	Address latch enable	Out	This signal is generated during the first clock cycle, to enable the address to be latched into the latches of peripherals The falling edge of ALE is guaranteed to latch the address information The ALE can also be used to strobe the status information, but it is kept in the low-level state during bus idle machine cycles.
$\overline{WR}$	Write control	Out	Indicates that the data on the data bus is to be written into the selected memory at the falling edge of the signal $\overline{WR}$ It remains the high-impedance state during the HOLD and HALT modes
$\overline{RD}$	Read control	Out	Indicates that the selected memory or I/O address is to be read and that the data bus is active for data transfer It remains in the high-impedance state during the HOLD and HALT modes
IO/$\overline{M}$	Data transfer control output	Out	This signal indicates whether the read/write is to memory or to I/Os It remains in the high-ipedance state during the HOLD and HALT modes
READY	Ready input	In	When it is at high-level during a read or write cycle, the READY indicates that the memory or peripheral is ready to send or receive date When the signal is at low-level, the CPU will wait for the signal to turn high-level before completing the read or write cycle
$\overline{RESET\ IN}$	Reset input	In	This signal (at least three clock cycles are necessary) sets the program counter to zero and resets the interrupt enable and HLDA flip-flops None of the other flags or registers (except the instruction register) are affected The CPU is held in the reset mode as long as the signal is applied
CLK	Clock output	Out	Clock pulses are available from this pin when a crystal or RC circuit is used as an input to the CPU
HLDA	Hold acknowledge signal	Out	By this signal the processor acknowledges the HOLD request signal and indicates that it will relinquish the buses in the next clock cycle The signal is returned to the low-level state after the HOLD request is completed The processor resumes the use of the buses one half clock cycle after the signal HLDA gose low-level
HOLD	Hold request signal	In	When the CPU receives a HOLD request It relinquishes the use of the buses as soon as the current machine cycle is completed The CPU can regain the use of buses only after the HOLD state is removed Upon acknowledging the HOLD signal, the address bus, the data bus, $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$ lines are put in the high-impedance state

Note HOLD, READY and all interrupt signals are synchronous with clock signal

STATUS INFORMATION

Status information can be obtained directly from the M5L8085AP. ALE is used as a status strobe. As the status is partially encoded, it informs the user in advance what type of bus transfer is being performed. The IO/$\overline{M}$ cycle status signal is also obtained directly. Decoded S_0 and S_1 signals carry:

	S_1	S_0	
HALT	0	0	
WRITE	0	1	
READ	1	0	(except for second and third machine cycles of DAD instruction)
FETCH	1	1	

S_1 can be used in determining the R/$\overline{W}$ status of all bus transfers.

In the M5L8085AP the low-order 8 bits of the address are multiplexed with data. When entering the low-order of the address into memory or peripheral latch circuits, the ALE is used as a strobe.

INTERRUPT AND SERIAL I/O

The M5L8085AP has five interrupt inputs—INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. The three RST inputs, 5.5, 6.5, 7.5, are provided with programmable masks. TRAP has the same function as the restart interrupt, except that it is non-maskable.

When an interrupt is enabled and the corresponding interrupt mask is not set, the three RST interrupts will cause the internal execution of the RST. When non-maskable TRAP is applied, it causes the internal execution of an RST regardless of the state of the interrupt enable or masks. The restart addresses (hexadecimal) of the interrupts are:

Interrupt	Adress
TRAP	24_{16}
RST 5.5	$2C_{16}$
RST 6.5	34_{16}
RST 7.5	$3C_{16}$

Two different types of signal are used for restart interrupts. Both RST 5.5 and RST 6.5 are sensitive to high-level as in INTR, and are acknowledged in the same timing as INTR. RST 7.5 is sensitive to rising-edge, and existence of a pulse sets the RST 7.5 interrupt request. This condition will be maintained until the request is fulfilled or reset by a SIM or RESET instruction.

Each of the restart interrupts may be masked independently to avoid interrupting the CPU. An interrupt requested by an RST 7.5 will be stored even when its mask is set and the interrupt is disabled. Masks can be changed in a SIM instruction or the RESET. When two enabled interrupts are requested at the same time, the interrupt with the highest priority will be accepted. The TRAP has the highest priority followed in order by RST 7.5, RST 6.5, RST 5.5 and INTR. This priority system dose not take into consideration the priority of an interrupt routine that is already started. In other words, when an RST 5.5 interrupt is reenabled before the termination of the RST 7.5 interrupt routine, it will interrupt the RST 7.5.

The TRAP interrupt is very useful in preventing disastrous errors and bus errors resulting from power failures. The TRAP input is recognized in the same manner as any other interrupt, but it has the highest priority, and is not affected by any flags or masks. The TRAP input can be sensed by both edge and level. TRAP should be maintained high-level until it is acknowledged. But, it will not be acknowledged again unless it turns low-level and high-level again. In this manner, faulty operation due to noise or logic glitches is prevented.

The selial I/O system is also considered to be an interrupt as it is controlled by instructions RIM and SIM. The SID is read by instruction RIM and the SOD data is set by instruction SIM.

BASIC TIMING

The M5L8085AP is provided with a multiplexed data bus. The ALE is utilized as a strobe with which the low-order 8 bits of the address on the data bus are sampled. Fig.1 shows the basic cycle in which an out instruction is fetched, and memory is read and written to the I/O port. The I/O port address is stored in both the address bus and the address/data bus during the I/O write and read cycle. To enable the M5L8085AP to be used with a slow memory, the READY line is used for extending the read and write pulse width.

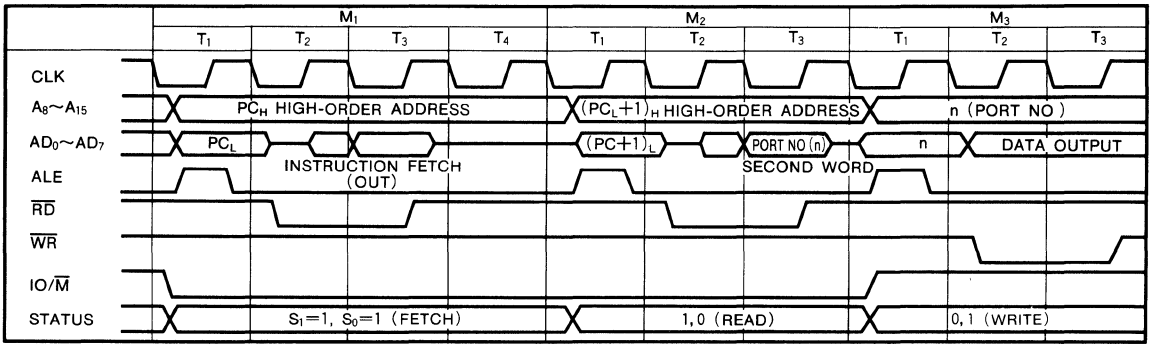


Fig. 1 Basic cycle

MACHINE INSTRUCTIONS

Instr. class	Mnemonic	Instruction code D7 D6 D5 D4 D3 D2 D1 D0	16mal notatn	No. of states	No. of bytes	No. of cycles	Functions	Flags S Z P CY2 CY1	Address bus Contents	Address bus Mach cycle*	Data bus Contents	Data bus I/O	Data bus Mach cycle**
Data transfer	MOV r1, r2	0 1 D D D S S S		4	1	1	(r1) ← (r2)	X X X X X					
	MOV M, r	0 1 1 1 0 S S S		7	1	2	(M) ← (r) Where M = (H)(L)	X X X X X	M	M4	(r)	O	M4
	MOV r, M	0 1 D D D 1 1 0		7	1	2	(r) ← (M) Where M = (H)(L)	X X X X X	M	M4	(M)	I	M4
	MVI r, n	0 0 D D D 1 1 0 <B2>		7	2	2	(r) ← n	X X X X X			<B2>	I	M4
	MVI M, n	0 0 1 1 0 1 1 0 <B2>	3 6	10	2	3	(M) ← n Where M = (H)(L)	X X X X X	M	M5	<B2>	I	M5
	LXI B, m	0 0 0 0 0 0 0 1 <B2> <B3>	0 1	10	3	3	(C) ← <B2> (B) ← <B3> Where, m = <B3><B2>	X X X X X			<B2> <B3>	I I	M2 M3
	LXI D, m	0 0 0 1 0 0 0 1 <B2> <B3>	1 1	10	3	3	(E) ← <B2> (D) ← <B3> Where m = <B3><B2>	X X X X X			<B2> <B3>	I I	M2 M3
	LXI H, m	0 0 1 0 0 0 0 1 <B2> <B3>	2 1	10	3	3	(L) ← <B2> (H) ← <B3> Where m = <B3><B2>	X X X X X			<B2> <B3>	I I	M2 M3
	LXI SP, m	0 0 1 1 0 0 0 1 <B2> <B3>	3 1	10	3	3	(SP) ← m	X X X X X			<B2> <B3>	I I	M2 M3
	SPHL	1 1 1 1 1 0 0 1	F 9	6	1	1	(SP) ← (H)(L)	X X X X X					
	STAX B	0 0 0 0 0 0 1 0	0 2	7	1	2	((B)(C)) ← (A)	X X X X X	(B)(C)	M4	(A)	O	M4
	STAX D	0 0 0 1 0 0 1 0	1 2	7	1	2	((D)(E)) ← (A)	X X X X X	(D)(E)	M4	(A)	O	M4
	LDAX B	0 0 0 0 1 0 1 0	0 A	7	1	2	(A) ← ((B)(C))	X X X X X	(B)(C)	M4	((B)(C))	I	M4
	LDAX D	0 0 0 1 1 0 1 0	1 A	7	1	2	(A) ← ((D)(E))	X X X X X	(D)(E)	M4	((D)(E))	I	M4
	STA m	0 0 1 1 0 0 1 0 <B2> <B3>	3 2	13	3	4	(m) ← (A)	X X X X X	m	M4	(A)	O	M4
	LDA m	0 0 1 1 1 0 1 0 <B2> <B3>	3 A	13	3	4	(A) ← (m)	X X X X X	m	M4	(m)	I	M4
	SHLD m	0 0 1 0 0 0 1 0 <B2> <B3>	2 2	16	3	5	(m) ← (L) (m + 1) ← (H)	X X X X X	m m + 1	M4 M5	(L) (H)	O O	M4 M5
	LHLD m	0 0 1 0 1 0 1 0 <B2> <B3>	2 A	16	3	5	(L) ← (m) (H) ← (m + 1)	X X X X X	m m + 1	M4 M5	(m) (m + 1)	I I	M4 M5
	XCHG	1 1 1 0 1 0 1 1	E B	4	1	1	(H)(L) ↔ (D)(E)	X X X X X					
	XTHL	1 1 1 0 0 0 1 1	E 3	16	1	5	(H)(L) ↔ ((SP) + 1)((SP))	X X X X X	(SP) (SP) + 1	M2 M3	((SP)) ((SP) + 1)	I I	M2 M3
Arithmetic logical compare	ADD r	1 0 0 0 0 S S S		4	1	1	(A) ← (A) + (r)	O O O O O					
	ADD M	1 0 0 0 0 1 1 0	8 6	7	1	2	(A) ← (A) + (M) Where M = (H)(L)	O O O O O	M	M4	(M)	I	M4
	ADI n	1 1 0 0 0 1 1 0 <B2>	C 6	7	2	2	(A) ← (A) + n	O O O O O			<B2>	I	M4
	ADC r	1 0 0 0 1 S S S		4	1	1	(A) ← (A) + (r) + (CY2)	O O O O O					
	ADC M	1 0 0 0 1 1 1 0	8 E	7	1	2	(A) ← (A) + (M) + (CY2) Where M = (H)(L)	O O O O O	M	M4	(M)	I	M4
	ACI n	1 1 0 0 1 1 1 0 <B2>	C E	7	2	2	(A) ← (A) + n + (CY2)	O O O O O			<B2>	I	M4
	DAD B	0 0 0 0 1 0 0 1	0 9	10	1	3	(H)(L) ← (H)(L) + (B)(C)	X X X O X					
	DAD D	0 0 0 1 1 0 0 1	1 9	10	1	3	(H)(L) ← (H)(L) + (D)(E)	X X X O X					
	DAD H	0 0 1 0 1 0 0 1	2 9	10	1	3	(H)(L) ← (H)(L) + (H)(L)	X X X O X					
	DAD SP	0 0 1 1 1 0 0 1	3 9	10	1	3	(H)(L) ← (H)(L) + (SP)	X X X O X					
	SUB r	1 0 0 1 0 S S S		4	1	1	(A) ← (A) − (r)	O O O O O					
	SUB M	1 0 0 1 0 1 1 0	9 6	7	1	2	(A) ← (A) − (M) Where M = (H)(L)	O O O O O	M	M4	(M)	I	M4
	SUI n	1 1 0 1 0 1 1 0 <B2>	D 6	7	2	2	(A) ← (A) − n	O O O O O			<B2>	I	M4
	SBB r	1 0 0 1 1 S S S		4	1	1	(A) ← (A) − (r) − (CY2)	O O O O O					
	SBB M	1 0 0 1 1 1 1 0	9 E	7	1	2	(A) ← (A) − (M) − (CY2) Where M = (H)(L)	O O O O O	M	M4	(M)	I	M4
	SBI n	1 1 0 1 1 1 1 0 <B2>	D E	7	2	2	(A) ← (A) − n − (CY2)	O O O O O			<B2>	I	M4
	ANA r	1 0 1 0 0 S S S		4	1	1	(A) ← (A) ∧ (r)	O O O 0 1					
	ANA M	1 0 1 0 0 1 1 0	A 6	7	1	2	(A) ← (A) ∧ (M) Where M = (H)(L)	O O O 0 1	M	M4	(M)	I	M4
	ANI n	1 1 1 0 0 1 1 0 <B2>	E 6	7	2	2	(A) ← (A) ∧ n	O O O 0 1			<B2>	I	M4
	XRA r	1 0 1 0 1 S S S		4	1	1	(A) ← (A) ∀ (r)	O O O 0 0					
	XRA M	1 0 1 0 1 1 1 0	A E	7	1	2	(A) ← (A) ∀ (M) Where M = (H)(L)	O O O 0 0	M	M4	(M)	I	M4
	XRI n	1 1 1 0 1 1 1 0 <B2>	E E	7	2	2	(A) ← (A) ∀ n	O O O 0 0			<B2>	I	M4
	ORA r	1 0 1 1 0 S S S		4	1	1	(A) ← (A) ∨ (r)	O O O 0 0					
	ORA M	1 0 1 1 0 1 1 0	B 6	7	1	2	(A) ← (A) ∨ (M) Where, M = (H)(L)	O O O 0 0	M	M4	(M)	I	M4
	ORI n	1 1 1 1 0 1 1 0 <B2>	F 6	7	2	2	(A) ← (A) ∨ n	O O O 0 0			<B2>	I	M4
	CMP r	1 0 1 1 1 S S S		4	1	1	(A) − (r)	O O O O O					
	CMP M	1 0 1 1 1 1 1 0	B E	7	1	2	(A) − (M) Compare, Where M = (H)(L)	O O O O O	M	M4	(M)	I	M4
	CPI n	1 1 1 1 1 1 1 0 <B2>	F E	7	2	2	(A) − n	O O O O O			<B2>	I	M4
Register increment/decrement	INR r	0 0 D D D 1 0 0		4	1	1	(r) ← (r) + 1	O O O X O					
	INR M	0 0 1 1 0 1 0 0	3 4	10	1	3	(M) ← (M) + 1 Where M = (H)(L)	O O O X O	M	M4	(M)	I	M4
	DCR r	0 0 D D D 1 0 1		4	1	1	(r) ← (r) − 1	O O O X O					
	DCR M	0 0 1 1 0 1 0 1	3 5	10	1	3	(M) ← (M) − 1 Where, M = (H)(L)	O O O X O	M	M4	(M)	I	M4
	INX B	0 0 0 0 0 0 1 1	0 3	6	1	1	(B)(C) ← (B)(C) + 1	X X X X X					
	INX D	0 0 0 1 0 0 1 1	1 3	6	1	1	(D)(E) ← (D)(E) + 1	X X X X X					
	INX H	0 0 1 0 0 0 1 1	2 3	6	1	1	(H)(L) ← (H)(L) + 1	X X X X X					
	INX SP	0 0 1 1 0 0 1 1	3 3	6	1	1	(SP) ← (SP) + 1	X X X X X					
	DCX B	0 0 0 0 1 0 1 1	0 B	6	1	1	(B)(C) ← (B)(C) − 1	X X X X X					
	DCX D	0 0 0 1 1 0 1 1	1 B	6	1	1	(D)(E) ← (D)(E) − 1	X X X X X					
	DCX H	0 0 1 0 1 0 1 1	2 B	6	1	1	(H)(L) ← (H)(L) − 1	X X X X X					
	DCX SP	0 0 1 1 1 0 1 1	3 B	6	1	1	(SP) ← (SP) − 1	X X X X X					
Rotate & shift contents of accumulator	RLC	0 0 0 0 0 1 1 1	0 7	4	1	1	Left shift CY2 ← A7 A6 … A1 A0 ←	X X X O X					
	RRC	0 0 0 0 1 1 1 1	0 F	4	1	1	Right shift CY2 → A7 A6 … A1 A0 →	X X X O X					
	RAL	0 0 0 1 0 1 1 1	1 7	4	1	1	Left shift CY2 ← A7 A6 … A1 A0 ←	X X X O X					
	RAR	0 0 0 1 1 1 1 1	1 F	4	1	1	Right shift CY2 → A7 A6 … A1 A0 →	X X X O X					
Accumu compen	CMA	0 0 1 0 1 1 1 1	2 F	4	1	1	(A) ← $\overline{(A)}$	X X X X X					
	DAA	0 0 1 0 0 1 1 1	2 7	4	1	1	Results of binary addition are adjusted to BCD	O O O O O					
Carry set	STC	0 0 1 1 0 1 1 1	3 7	4	1	1	(CY2) ← 1	X X X 1 X					
	CMC	0 0 1 1 1 1 1 1	3 F	4	1	1	(CY2) ← $\overline{(CY2)}$	X X X O X					

* State is T1 ** State is T2

MITSUBISHI ELECTRIC

8-BIT PARALLEL MICROPROCESSOR

Instr class	Mnemonic		D7 D6 D5 D4 D3 D2 D1 D0	16mal notatn	No. of states	No. of bytes	No. of cycles	Functions	S Z P CY2 CY1	Address bus Contents	Address bus Mach cycle*	Data bus Contents	Data bus I/O	Data bus Mach cycle**
Jump	JMP	m	1 1 0 0 0 0 1 1 <B2> <B3>	C3	10	3	3	(PC)←m	X X X X X			<B2> <B3>	I I	M2 M3
	PCHL		1 1 1 0 1 0 0 1	E9	6	1	1	(PC)←(H)(L)	X X X X X					
	JC	m	1 1 0 1 1 0 1 0 <B2> <B3>	DA	10/7	3	3/2	(CY2) = 1	X X X X X	If condition is true				
	JNC	m	1 1 0 1 0 0 1 0 <B2> <B3>	D2	10/7	3	3/2	(CY2) = 0 If condition is true (PC)←m	X X X X X	If condition is true				
	JZ	m	1 1 0 0 1 0 1 0 <B2> <B3>	CA	10/7	3	3/2	(Z) = 1	X X X X X			<B2> <B3>	I I	M2 M3
	JNZ	m	1 1 0 0 0 0 1 0 <B2> <B3>	C2	10/7	3	3/2	(Z) = 0	X X X X X					
	JP	m	1 1 1 1 0 0 1 0 <B2> <B3>	F2	10/7	3	3/2	(S) = 0 If condition is false (PC)← (PC) + 3	X X X X X					
	JM	m	1 1 1 1 1 0 1 0 <B2> <B3>	FA	10/7	3	3/2	(S) = 1	X X X X X					
	JPE	m	1 1 1 0 1 0 1 0 <B2> <B3>	EA	10/7	3	3/2	(P) = 1	X X X X X					
	JPO	m	1 1 1 0 0 0 1 0 <B2> <B3>	E2	10/7	3	3/2	(P) = 0	X X X X X					
Subroutine call	CALL	m	1 1 0 0 1 1 0 1 <B2> <B3>	CD	18	3	5	((SP) - 1) ((SP) - 2)←(PC) + 3 (PC)←m (SP) ← (SP) - 2	X X X X X	(SP) - 1 (SP) - 2	M4 M5	<B2> <B3> (PC)+3 (PC)+3	I I O O	M2 M3 M4 M5
	RST	n	1 1 A A A 1 1 1		12	1	3	((SP) - 1) ((SP) - 2)←(PC) + 1 (PC)←n×8, (SP) ← (SP) - 2 Where 0≦n≦7	X X X X X	(SP) - 1 (SP) - 2	M4 M5	(PC)+1 (PC)+1	O O	M4 M5
	CC	m	1 1 0 1 1 1 0 0 <B2> <B3>	DC	18/9	3	5/2	(CY2) = 1	X X X X X	If condition is true				
	CNC	m	1 1 0 1 0 1 0 0 <B2> <B3>	D4	18/9	3	5/2	(CY2) = 0 If condition is true	X X X X X	If condition is true				
	CZ	m	1 1 0 0 1 1 0 0 <B2> <B3>	CC	18/9	3	5/2	(Z) = 1 ((SP) 1) ((SP) - 2)←(PC) + 3 (PC)←m	X X X X X	(SP) - 1	M4	<B2> <B3> (PC) + 3	I I O	M2 M3 M4
	CNZ	m	1 1 0 0 0 1 0 0 <B2> <B3>	C4	18/9	3	5/2	(Z) = 0 (SP)← (SP) 2	X X X X X	(SP) - 2	M5	(PC) + 3	O	M5
	CP	m	1 1 1 1 0 1 0 0 <B2> <B3>	F4	18/9	3	5/2	(S) = 0	X X X X X					
	CM	m	1 1 1 1 1 1 0 0 <B2> <B3>	FC	18/9	3	5/2	(S) = 1 If condition is false (PC)←(PC) + 3	X X X X X					
	CPE	m	1 1 1 0 1 1 0 0 <B2> <B3>	EC	18/9	3	5/2	(P) = 1	X X X X X					
	CPO	m	1 1 1 0 0 1 0 0 <B2> <B3>	E4	18/9	3	5/2	(P) = 0	X X X X X					
Return	RET		1 1 0 0 1 0 0 1	C9	10	1	3	(PC) ←((SP) + 1) ((SP)) (SP)←(SP) + 2	X X X X X	(SP) (SP) + 1	M4 M5	((SP)) ((SP) + 1)	I I	M4 M5
	RC		1 1 0 1 1 0 0 0	D8	12/6	1	3/1	(CY2) = 1 If condition is true	X X X X X	If condition is true				
	RNC		1 1 0 1 0 0 0 0	D0	12/6	1	3/1	(CY2) = 0	X X X X X					
	RZ		1 1 0 0 1 0 0 0	C8	12/6	1	3/1	(Z) = 1 (PC)←((SP) + 1) ((SP))	X X X X X	(SP)	M4	((SP))	I	M4
	RNZ		1 1 0 0 0 0 0 0	C0	12/6	1	3/1	(Z) = 0 (SP)←(SP) + 2	X X X X X	(SP) + 1	M5	((SP) + 1)	I	M5
	RP		1 1 1 1 0 0 0 0	F0	12/6	1	3/1	(S) = 0	X X X X X					
	RM		1 1 1 1 1 0 0 0	F8	12/6	1	3/1	(S) = 1 If condition is false	X X X X X					
	RPE		1 1 1 0 1 0 0 0	E8	12/6	1	3/1	(P) = 1 (PC)←(PC) + 1	X X X X X					
	RPO		1 1 1 0 0 0 0 0	E0	12/6	1	3/1	(P) = 0	X X X X X					
Input/ output control	IN	n	1 1 0 1 1 0 1 1 <B2>	DB	10	2	3	(A) ← (Input buffer) ← (Input device of number n) (Input data)	X X X X X	<B2> B2>	M5	<B2> (Input data)	I I	M4 M5
	OUT	n	1 1 0 1 0 0 1 1 <B2>	D3	10	2	3	(Output device of number n) ← (A)	X X X X X	<B2> <B2>	M5	<B2> (A)	O O	M4 M5
Interrupt control	EI		1 1 1 1 1 0 1 1	FB	4	1	1	(INTE)← 1	X X X X X					
	DI		1 1 1 1 0 0 1 1	F3	4	1	1	(INTE)← 0	X X X X X					
Stack control	PUSH	PSW	1 1 1 1 0 1 0 1	F5	12	1	3	((SP) - 1)←(A) ((SP) - 2)←(F) (SP) ←(SP) - 2	X X X X X	(SP) - 1 (SP) - 2	M4 M5	(A) (F)	O O	M4 M5
	PUSH	B	1 1 0 0 0 1 0 1	C5	12	1	3	((SP) - 1)←(B) ((SP) - 2)←(C) (SP) ←(SP) - 2	X X X X X	(SP) - 1 (SP) - 2	M4 M5	(B) (C)	O O	M4 M5
	PUSH	D	1 1 0 1 0 1 0 1	D5	12	1	3	((SP) - 1)←(D), ((SP) - 2)←(E) (SP) ←(SP) - 2	X X X X X	(SP) - 1 (SP) - 2	M4 M5	(D) (E)	O O	M4 M5
	PUSH	H	1 1 1 0 0 1 0 1	E5	12	1	3	((SP) - 1)←(H) ((SP) - 2)←(L) (SP) ←(SP) - 2	X X X X X	(SP) - 1 (SP) - 2	M4 M5	(H) (L)	O O	M4 M5
	POP	PSW	1 1 1 1 0 0 0 1	F1	10	1	3	(F) ←((SP)), (A) ←((SP) + 1) (SP) ←(SP) + 2	O O O O O	(SP) (SP) + 1	M4 M5	((SP)) ((SP) + 1)	I I	M4 M5
	POP	B	1 1 0 0 0 0 0 1	C1	10	1	3	(C) ←((SP)), (B) ←((SP) + 1) (SP) ←(SP) + 2	X X X X X	(SP) (SP) + 1	M4 M5	((SP)) ((SP) + 1)	I I	M4 M5
	POP	D	1 1 0 1 0 0 0 1	D1	10	1	3	(E) ←((SP)) (D) ←((SP) + 1) (SP) ←(SP) + 2	X X X X X	(SP) (SP) + 1	M4 M5	((SP)) ((SP) + 1)	I I	M4 M5
	POP	H	1 1 1 0 0 0 0 1	E1	10	1	3	(L) ←((SP)) (H) ←((SP) + 1) (SP) ←(SP) + 2	X X X X X	(SP) (SP) + 1	M4 M5	((SP)) ((SP) + 1)	I I	M4 M5
Others	HLT		0 1 1 1 0 1 1 0	76	5	1	1	(PC) ←(PC) + 1	X X X X X					
	NOP		0 0 0 0 0 0 0 0	00	4	1	1	(PC) ← (PC) + 1	X X X X X					
Mask set instructions	RIM		0 0 1 0 0 0 0 0	20	4	1	1	All RST interrupt masks, any pending RST interrupt requests, and the serial input data from the SID pin are read into the accumulator	X X X X X					
	SIM		0 0 1 1 0 0 0 0	30	4	1	1	Mask is enabled (or disabled) to the RST interrupt corresponding to the contents (bit pattern) of the accumulator The serial output is enabled and the serial output bit is loaded into the SOD latch	X X X X X					

* State is T_1. ** State is T_2.

MACHINE INSTRUCTIONS SYMBOL MEANING

Symbol	Meaning
r	Register
m	Two-byte data
n	One-byte data
⟨B2⟩	Second byte of instruction
⟨B3⟩	Third byte of instruction
AAA	Binary representation for RST instruction n
F	8-bit data from the most to the least significant bit S, Z, X, CY1, 0, P, X, CY2 (X is indefinite)
PC	Program counter
SP	Stack pointer

Symbol	Meaning
S S S or D D D	Bit pattern designating register or memory Where M = (H) (L)

Register or memory	S S S or D D D
B	0 0 0
C	0 0 1
D	0 1 0
E	0 1 1
H	1 0 0
L	1 0 1
M	1 1 0
A	1 1 1

Symbol	Meaning
←	Data is transferred in direction shown
( )	Contents of register or memoy location
V	Inclusive OR
⊻	Exclusive OR
∧	Logical AND
$\overline{\ }$	1 s complement
X	Content of flag is not changed after execution
O	Content of flag is set or reset after execution
I	Input mode
O	Output mode

INSTRUCTION CODE LIST

$D_3 \sim D_0$ \ $D_7 \sim D_4$	Hexadecimal notation	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	NOP	(—)	RIM	SIM	MOV B, B	MOV D, B	MOV H, B	MOV M, B	ADD B	SUB B	ANA B	ORA B	RNZ	RNC	RPO	RP
0001	1	LXI B	LXI D	LXI H	LXI SP	MOV B, C	MOV D, C	MOV H, C	MOV M, C	ADD C	SUB C	ANA C	ORA C	POP B	POP D	POP H	POP PSW
0010	2	STAX B	STAX D	SHLD	STA	MOV B, D	MOV D, D	MOV H, D	MOV M, D	ADD D	SUB D	ANA D	ORA D	JNZ	JNC	JPO	JP
0011	3	INX B	INX D	INX H	INX SP	MOV B, E	MOV D, E	MOV H, E	MOV M, E	ADD E	SUB E	ANA E	ORA E	JMP	OUT	XTHL	DI
0100	4	INR B	INR D	INR H	INR M	MOV B, H	MOV D, H	MOV H, H	MOV M, H	ADD H	SUB H	ANA H	ORA H	CNZ	CNC	CPO	CP
0101	5	DCR B	DCR D	DCR H	DCR M	MOV B, L	MOV D, L	MOV H, L	MOV M, L	ADD L	SUB L	ANA L	ORA L	PUSH B	PUSH D	PUSH H	PUSH PSW
0110	6	MVI B	MVI D	MVI H	MVI M	MOV B, M	MOV D, M	MOV H, M	HLT	ADD M	SUB M	ANA M	ORA M	ADI	SUI	ANI	ORI
0111	7	RLC	RAL	DAA	STC	MOV B, A	MOV D, A	MOV H, A	MOV M, A	ADD A	SUB A	ANA A	ORA A	RST 0	RST 2	RST 4	RST 6
1000	8	(—)	(—)	(—)	(—)	MOV C, B	MOV E, B	MOV L, B	MOV A, B	ADC B	SBB B	XRA B	CMP B	RZ	RC	RPE	RM
1001	9	DAD B	DAD D	DAD H	DAD SP	MOV C, C	MOV E, C	MOV L, C	MOV A, C	ADC C	SBB C	XRA C	CMP C	RET	(—)	PCHL	SPHL
1010	A	LDAX B	LDAX D	LHLD	LDA	MOV C, D	MOV E, D	MOV L, D	MOV A, D	ADC D	SBB D	XRA D	CMP D	JZ	JC	JPE	JM
1011	B	DCX B	DCX D	DCX H	DCX SP	MOV C, E	MOV E, E	MOV L, E	MOV A, E	ADC E	SBB E	XRA E	CMP E	(—)	IN	XCHG	EI
1100	C	INR C	INR E	INR L	INR A	MOV C, H	MOV E, H	MOV L, H	MOV A, H	ADC H	SBB H	XRA H	CMP H	CZ	CC	CPE	CM
1101	D	DCR C	DCR E	DCR L	DCR A	MOV C, L	MOV E, L	MOV L, L	MOV A, L	ADC L	SBB L	XRA L	CMP L	CALL	(—)	(—)	(—)
1110	E	MVI C	MVI E	MVI L	MVI A	MOV C, M	MOV E, M	MOV L, M	MOV A, M	ADC M	SBB M	XRA M	CMP M	ACI	SBI	XRI	CPI
1111	F	RRC	RAR	CMA	CMC	MOV C, A	MOV E, A	MOV L, A	MOV A, A	ADC A	SBB A	XRA A	CMP A	RST 1	RST 3	RST 5	RST 7

This list shows the machine codes and corresponding machine instruction. $D_3 \sim D_0$ indicate the low-order 4 bits of the machine code and $D_7 \sim D_4$ indicate the high-order 4 bits. Hexadecimal numbers are also used to indicate this code.

The instruction may consists of 1 , 2 , or 3 bytes, but only the first byte is listed.

□ indicates a 3 -byte instruction.

▨ indicates a 2 -byte instruction.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5~7	V
V_I	Input voltage		−0.5~7	V
Pd	Power dissipation	T_a=25℃	1.5	W
Topr	Operating free-air temperature range		−20~75	℃
Tstg	Storge temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage (Except for X_1, X_2)		2.2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage		−0.5		0.6	V
$V_{IH(\overline{RESIN})}$	High-level reset input voltage		2.4		V_{CC}+0.5	V
$V_{IL(\overline{RESIN})}$	Low-level reset input voltage		−0.5		0.8	V
V_{IHX}	X_1, X_2 High-level voltage		4.0		V_{CC}+0.5	V
V_{OH}	High-level output voltage	I_{OH}=−400 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL}=2mA			0.45	V
I_{CC}	Supply current from V_{CC}	(Note 2)			200	mA
I_I	Input leak current, except $\overline{RESET\ IN}$ (Note 1)	V_I=V_{CC}	−10		10	μA
I_{OZL}	Output floating leak current	V_O=0.45V~V_{CC}	−10		10	μA
V_{IH}−V_{IL}	Hysterisis $\overline{RESET\ IN}$ input		0.25			V

Note 1 The input $\overline{RESET\ IN}$ is pulled up to V_{CC} with the resistor 3kΩ (typ) when $V_I \geqq V_{IH(\overline{RESIN})}$
2 Maximum I_{CC} is 170mA at T_a = 0~70℃

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

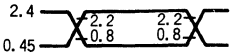
Symbol	Paramater	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{C(CLK)}$	Clock cycle time	$t_{C(CLK)} \geqq 320$ns C_L=150pF	320		2000	ns
$t_{su(DA-AD)}$	DA input setup time		−575			ns
$t_{su(DA-\overline{RD})}$	DA input setup time		−300			ns
$t_{h(DA-\overline{RD})}$	DA input hold time		0			ns
$t_{su(RDY-AD)}$	READY input setup time		−220			ns
$t_{su(RDY-CLK)}$	READY input setup time				−110	ns
$t_{h(RDY-CLK)}$	READY input hold time		0			ns
$t_{su(DA-ALE)}$	DA input setup time		−460			ns
$t_{su(HLD-CLK)}$	HOLD input setup time		170			ns
$t_{h(HLD-CLK)}$	HLD input hold time		0			ns
$t_{su(INT-CLK)}$	Interrupt setup time		160			ns
$t_{h(INT-CLK)}$	Interrupt hold time		0			ns
$t_{su(RDY-ALE)}$	READY input setup time		−110			ns

SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

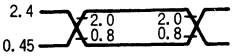
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{W(\overline{CLK})}$	CLK output low-level pulse width			80			ns
$t_{W(CLK)}$	CLK output high-level puls width			120			ns
$t_{r(CLK)}$	CLK output rise time					30	ns
$t_{f(CLK)}$	CLK output fall time					30	ns
$t_{d(X1-CLK)}$	Delay time, X_1 to CLK			30		120	ns
$t_{d(X1-\overline{CLK})}$	Delay time, X_1 to $\overline{CLK}$			30		150	ns
$t_{d(AD-ALE)}$	Delay time, address output to ALE signal	AD_0~AD_7		90			ns
		A_8~A_{15}		115			
$t_{d(ALE-AD)}$	Delay time, ALE signal to address output			100			ns
$t_{W(ALE)}$	ALE pulse width			140			ns
$t_{d(ALE-CLK)}$	Delay time, ALE to CLK			100			ns
$t_{d(ALE-\overline{CONT})}$	Delay time, ALE to control signal			130			ns
$t_{DXZ(\overline{RD}-AD)}$	Address disable time from read		$t_{C(CLK)}$≧320ns			0	ns
$t_{DZX(\overline{RD}-AD)}$	Address enable time from read		C_L=150pF	150			ns
$t_{d(\overline{CONT}-AD)}$	Address valid time after control signal			120			ns
$t_{d(DA-\overline{WR})}$	Delay time, data output to $\overline{WR}$ signal			420			ns
$t_{d(\overline{WR}-DA)}$	Delay time, $\overline{WR}$ signal to data output			100			ns
$t_{W(\overline{CONT})}$	Control signal pulse width			400			ns
$t_{d(CONT-ALE)}$	Delay time, CLK to ALE signal			50			ns
$t_{d(CLK-HLDA)}$	Delay time, CLK to HLDA signal			110			ns
$t_{DXZ(HLDA-BUS)}$	Bus disable time from HLDA					210	ns
$t_{DZX(HLDA-BUS)}$	Control signal disable time					210	ns
$t_{d(CONT-\overline{CONT})}$	Control signal disable time			400			ns
$t_{d(AD-\overline{CONT})}$	Delay time, address output to control signal	AD_0~AD_7		240			ns
		A_8~A_{15}		270			
$t_{d(ALE-DA)}$	Delay time, ALE to data output					200	ns
$t_{d(WRHL-DA)}$	Delay time, $\overline{WR}$ signal to data output					40	ns

Note 3 : at A_8~A_{15}, and IO/$\overline{M}$ $t_{d(AD-\overline{CONT})}$ after the release of the high-impedance state is 200ns
4 $t_{W(\overline{CLK})}$, $t_{W(CLK)}$ are 100ns(Min), 150ns(Min) respectively when 50pF+1TTL loaded
5 : A. C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	20ns
Input pulse fall time	20ns
Reference level input	V_{IH}=2.2V, V_{IL}=0.8V
output	V_{OH}=2.0V, V_{OL}=0.8V



Input



Output

Parameters described in the timing requirements and switching characteristics take relevant values in accordance with the relational expression shown in the following tables when the frequency is varied.

Relational Expression with the frequency T ($t_{C(CLK)}$) in the M5L8085AP

TIMMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Relational expression (Note 6)	Limit
$t_{su(DA-AD)}$	DA input setup time	C_L=150pF	225−(5/2+N)T	Min
$t_{su(DA-\overline{RD})}$	DA input setup time		180−(3/2+N)T	Min
$t_{su(RDY-AD)}$	READY input setup time		260−(3/2)T	Min
$t_{su(DA-ALE)}$	DA input setup time		180−2T	Min

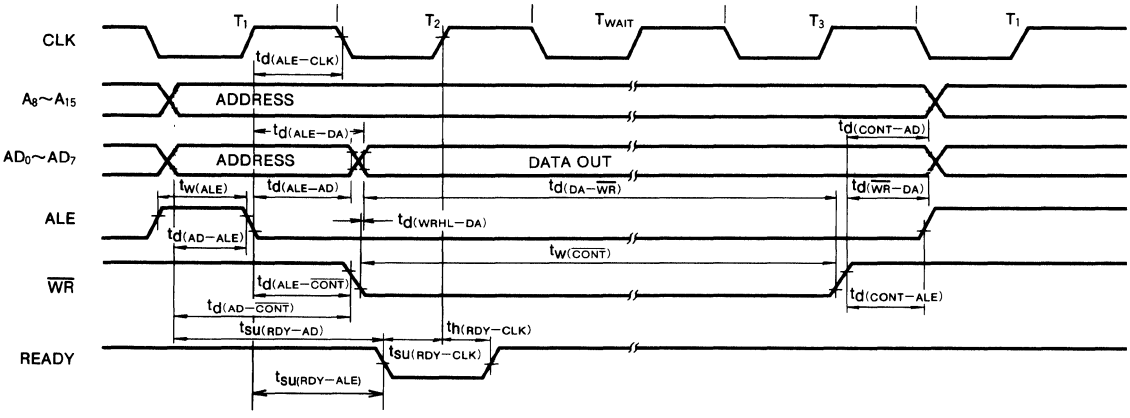
SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise notes)

Symbol	Palameter		Test conditions	Relational expression (Note 6)	Limit
$t_{W(\overline{CLK})}$	CLK output low-level pulse width		C_L=150pF	(1/2)T−80	Min
$t_{W(CLK)}$	CLK output high-level pulse width			(1/2)T−40	Min
$t_{d(AD-ALE)}$	Delay time, address output to ALE signal	AD_0~AD_7		(1/2)T−70	Min
		A_8~A_{15}		(1/2)T−45	
$t_{d(ALE-AD)}$	Delay time, ALE signal to address output			(1/2)T−60	Min
$t_{W(ALE)}$	ALE pulse width			(1/2)T−20	Min
$t_{d(ALE-CLK)}$	Delay time, ALE to CLK			(1/2)T−60	Min
$t_{d(ALE-\overline{CONT})}$	Delay time, ALE to control signal			(1/2)T−30	Min
$t_{DZX(\overline{RD}-AD)}$	Address enable time from read			(1/2)T−10	Min
$t_{d(CONT-AD)}$	Address valid time after control signal			(1/2)T−40	Min
$t_{d(DA-\overline{WR})}$	Delay time, data output to $\overline{WR}$ signal			(3/2+N)T−60	Min
$t_{d(\overline{WR}-DA)}$	Delay time $\overline{WR}$ signal to data output			(1/2)T−60	Min
$t_{W(\overline{CONT})}$	Control signal pulse width			(3/2+N)T−80	Min
$t_{d(CONT-ALE)}$	Delay time, CONT to ALE signal			(1/2)T−110	Min
$t_{d(CLK-HLDA)}$	Delay time, CLK to HLDA signal			(1/2)T−50	Min
$t_{DXZ(HLDA-BUS)}$	Bus disable time from HLDA			(1/2)T+50	Max
$t_{DZX(HLDA-BUS)}$	Bus enable time from HLDA			(1/2)T+50	Max
$t_{d(CONT-\overline{CONT})}$	Control signal disable time			(3/2)T−80	Min
$t_{d(AD-\overline{CONT})}$	Delay time, address output to control signal	AD_0~AD_7		T−80	Min
		A_8~A_{15}		T−50	

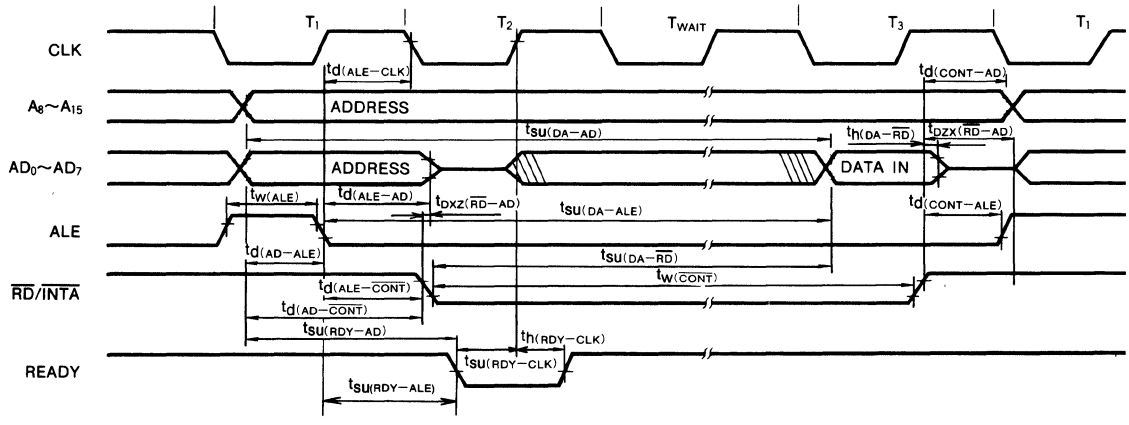
Note 6 N indicates the total number of wait cycles
$T=t_{C(CLK)}$

TIMING DIAGRAM

Write Cycle

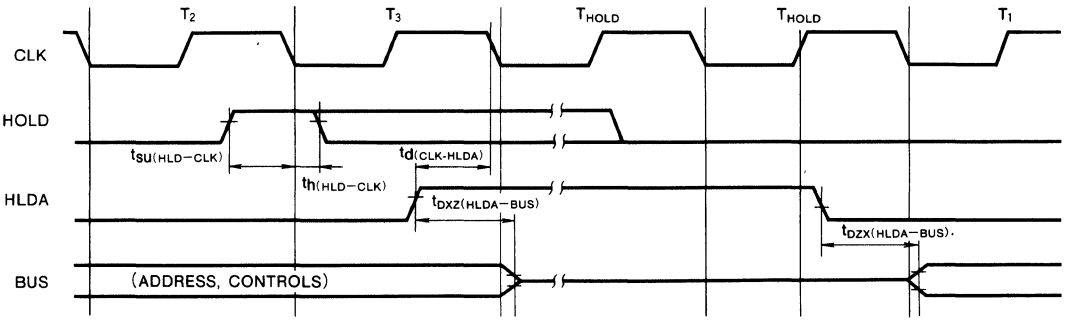


Read Cycle

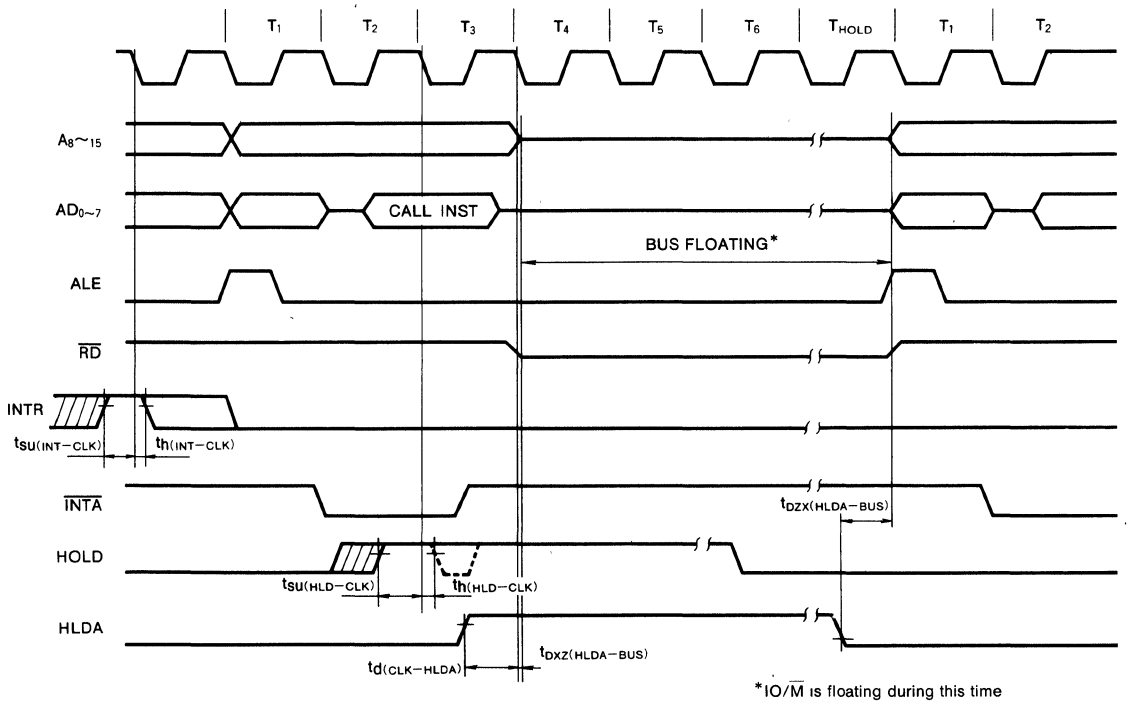


Note : READY must remain stable during setup and hold times

Hold Cycle

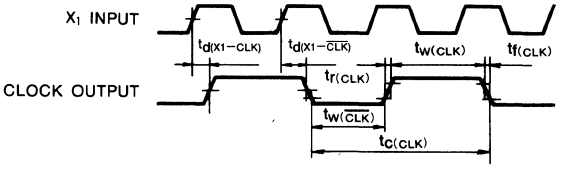


Interrupt and Hold Cycle



*IO/$\overline{M}$ is floating during this time

Clock Output Timing Waveform



MITSUBISHI ELECTRIC

TRAP INTERRUPT AND RIM INSTRUCTIONS

TRAP generates interrupts regardless of the interrupt enable filp-flop (INTE FF). The current state of the INTE FF is stored in flip flop A (A FF) of the CPU and then the INTE FF is reset. The first RIM instruction after the generation of a TRAP interrupt differs in function from the ordinary RIM instruction. That is, the bit 3 (INTE FF information) in the accumulator ($(A)_3$) after the execution of the RIM instruction contains the contents of the A FF, regardless of the state of the INTE FF at the time the RIM instruction is executed. These details are shown in Figs.2 and 3, Table 1.

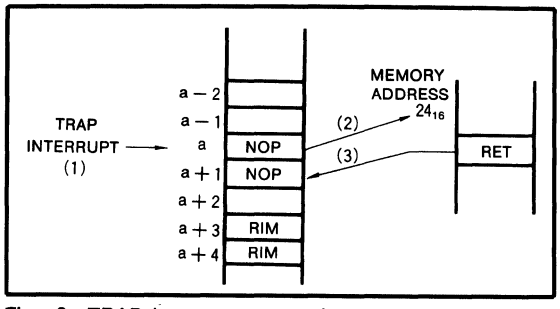


Fig. 2 TRAP interrupt processing

Below are the explanations of Fig. 2.

1. The TRAP interrupt request is issued while the instruction in address a is being executed.
2. The TRAP interrupt causes the same action as an RST instruction and then jumps to address 24_{16}.
3. It returns to address a+1 after executing the RET instruction.

Table 1 shows the information in the INTE FF at address a+3 and a+4 when the instructions EI and/or DI are executed at addresses a−1 and a+2.

Fig. 4 is a flow chart of the TRAP interrupt processing routine.

Table 1 TRAP interrupt and RIM instructions

Condition \ Number	1	2	3	4	5	6
Instruction in address a-1	EI	EI	EI	DI	DI	DI
Instruction in address a+2	EI	NOP	DI	EI	NOP	DI
Contents of $(A)_3$ after the execution of the RIM instruction in address a+3	1	1	1	0	0	0
State of INTE FF after the execution of the RIM instruction in address a+3	1	0	0	1	0	0
Contents of $(A)_3$ after the execution of the RIM instruction in address a+4	1	0	0	1	0	0
State of INTE FF after the execution of the RIM instruction in address a+4	1	0	0	1	0	0

Note 7 · The contents of $(A)_3$ after the excution of the RIM instruction is an information of the INTE FF The INTE FF assumes state 1 when it is in the EI state, and 0 when it is in the DI state

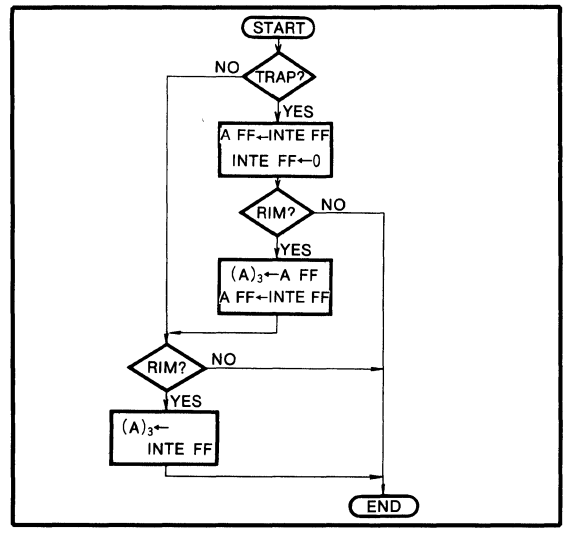


Fig.3 TRAP interrupt and INTE FF processing

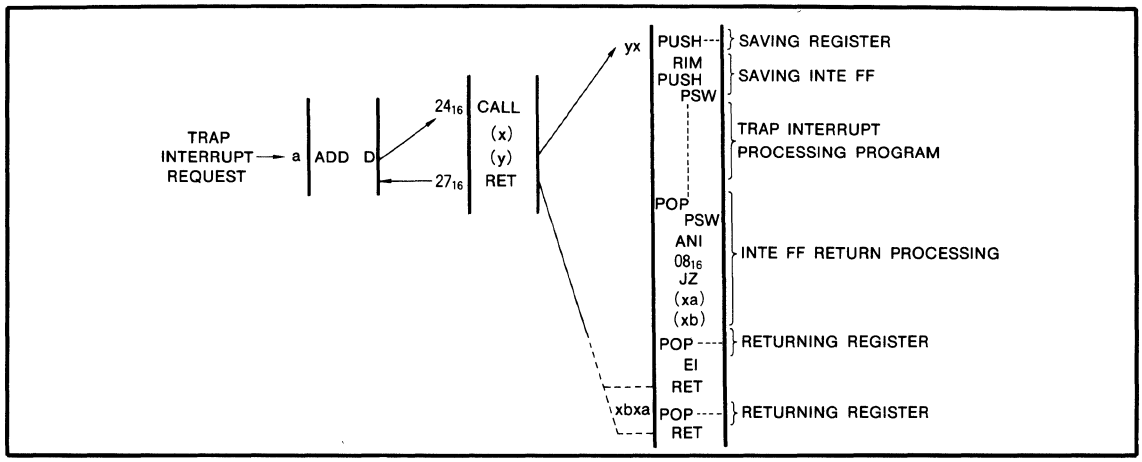


Fig. 4 TRAP interrupt processing routine

PULL-UP OF THE $\overline{\text{RESET IN}}$ INPUT

In order to increase the noise margin, the $\overline{\text{RESET IN}}$ input terminal is pulled up by about 3kΩ (typ) when the condition $V_I \geqq V_{IH(\overline{RESIN})}$ is satisfied. Fig. 5 is a connection diagram of the $\overline{\text{RESET IN}}$ input, and Fig. 6 shows the relation between input voltage and input current.

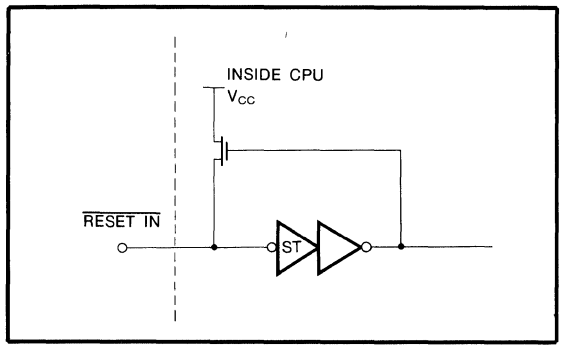


Fig. 5 Connections of $\overline{\text{RESET IN}}$ input

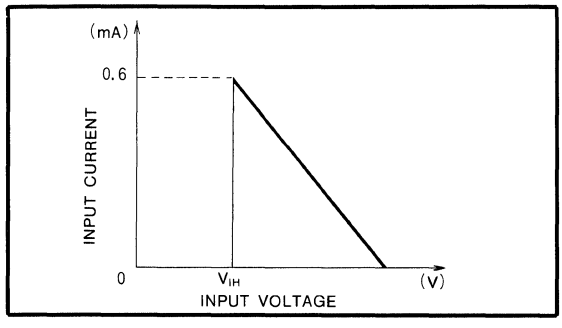


Fig. 6 $\overline{\text{RESET IN}}$ input current vs input voltage

DRIVING CIRCUIT OF X_1 AND X_2 INPUTS

Input terminals, X_1 and X_2 of the M5L8085AP can be driven by either a crystal, RC network, or external clock. Since the driver clock frequency is divided to 1/2 internally, the input frequency required is twice the actual execution frequency (6MHz for the M5L8085AP which is operated at 3MHz). Fig. 7 are typical connection diagram for a crystal circuit respectively.

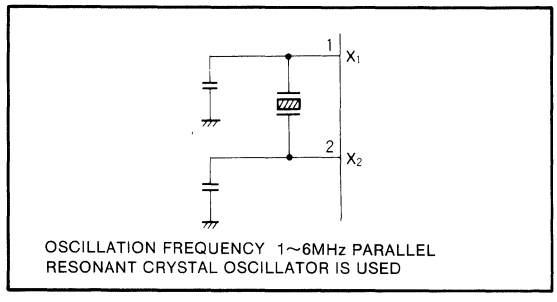


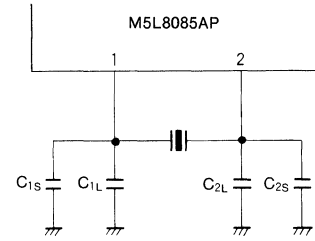
Fig. 7 Connections when crystal is used for X_1 and X_2 inputs

Conditions for Using a Quartz Crystal Element

1. Quartz Crystal Specifications

- Parallel resonance
- The frequency is 2 times the operation frequency (2 ~ 6.25MHz)
- Internal load capacitance: Approx. 16pF
- Parallel capacitance: Below 7pF
- Equivalent resistance: Below 75 Ω (for operation above 4MHz)
- For operation in the range 2 ~ 4MHz, the resistance showld be made as small as possible.
- Drive capability: Above 5mW (the power at which the crystal will be destoryed)

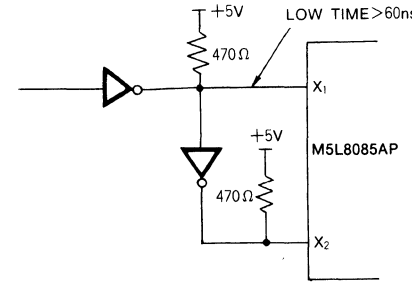
2. External Circuitry



C_{1S} Writing capacitance of pin X_1
C_{2S} Writing capacitance of pin X_2
C_{1S}: External capacitance at pin X_1
C_{2L} External capacitance at pin X_2
$C_1 = C_{1L} + C_{1S}$
$C_2 = C_{2L} + C_{2S}$

- For operation above 4MHz:
  $C_1 = C_2 = 10pF$
- For operation below 4MHz:
  $C_1 = C_2 = 15pF$

External Clock Driver Circuit



Pullup resistors are required to assure that the high level voltage of the input is at least 4V

MITSUBISHI ELECTRIC

WAIT STATE GENERATOR

Fig. 8 shows a typical 1-wait state generator for low speed RAM and ROM applications.

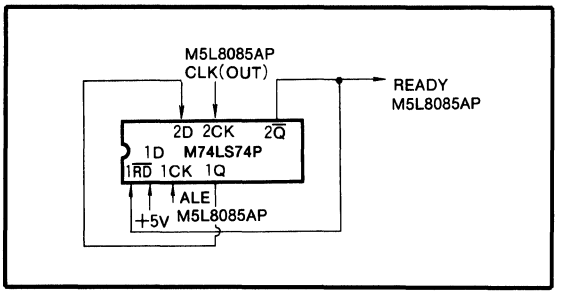


Fig. 8 1-wait state generator

Relation of Rim and Sim Instructions With The Accumulator (Supplementary Description).

The contents of the accumulator after the execution of a RIM instruction is shown in Fig. 9 .

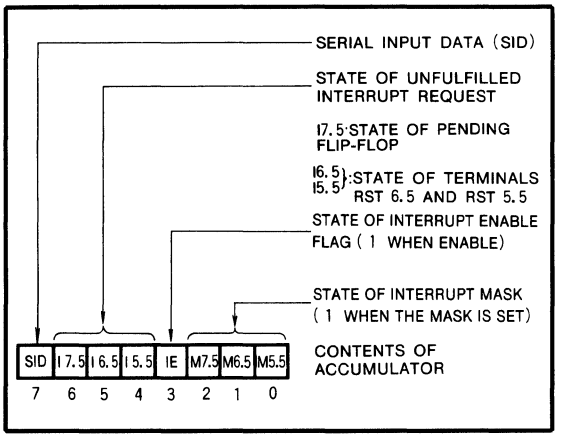


Fig. 9 Relation of the instruction RIM with the accumulator

The contents of the accumulator after the execution of a SIM instruction is shown in Fig.10.

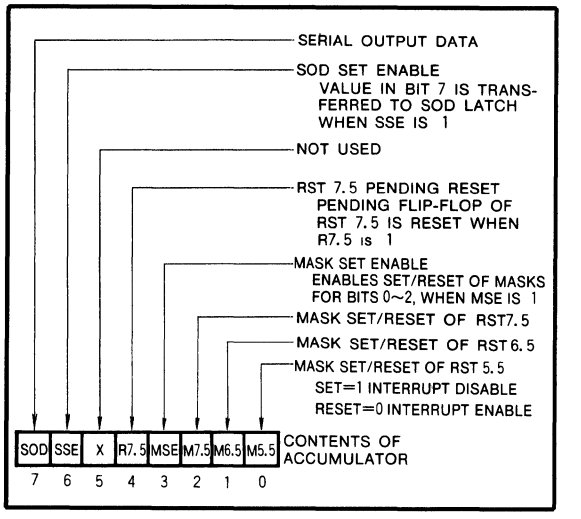


Fig. 10 Relation of the SIM instruction with the accumulator

M5L8212P

8-BIT INPUT/OUTPUT PORT WITH 3-STATE OUTPUT

DESCRIPTION

The M5L8212P is an input/output port consisting of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also a service request flip-flop for the generation and control of interrupts to a microprocessor is included.

FEATURES

- Parallel 8-bit data register and buffer
- Service request flip-flop for interrupt generation
- Three-state outputs
- Low input load current: I_{IL}=−250μA(max.)
- High output sink current: I_{OL}=16mA(max.)
- High-level output voltage for direct interface to a M5L8085AP, CPU: V_{OH}=3.65V(min.)

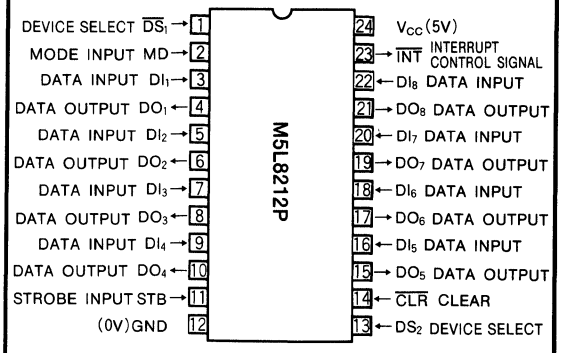
APPLICATION

Input/output port for a M5L8085AP
Latches, gate buffers or multiplexers
Peripheral and input/output functions for microcomputer systems

FUNCTION

Device select 1 ($\overline{DS_1}$) and device select 2 (DS_2) are used for chip selection when the mode input MD is low. When $\overline{DS_1}$ is low and DS_2 is high, the data in the latches is transferred to the data outputs $DO_1 \sim DO_8$, and the service request flip-flop SR is set. Also, the strobed input STB is active, the data inputs $DI_1 \sim DI_8$ are latched in the data latches, and the service request flip-flop SR is reset.

PIN CONFIGURATION (TOP VIEW)



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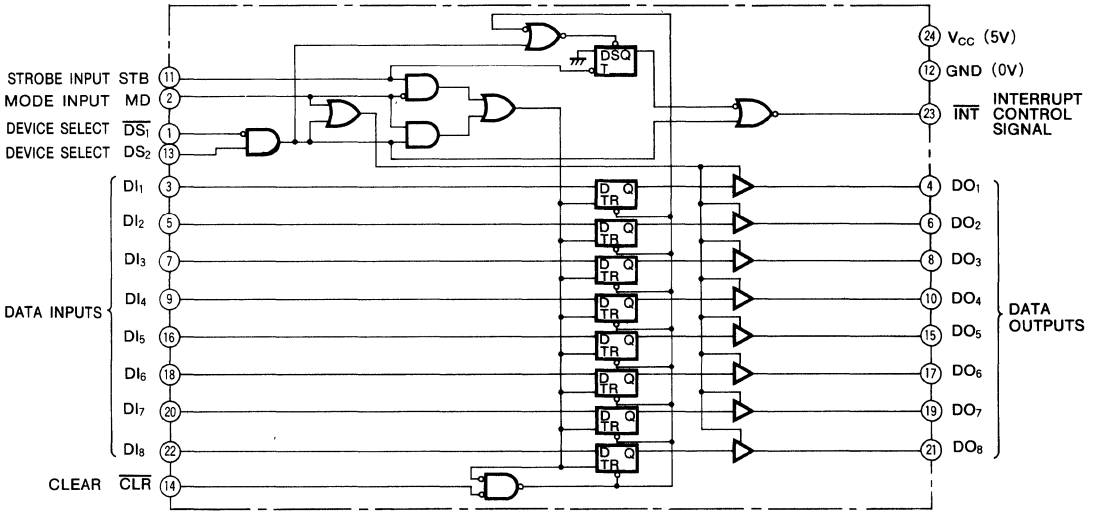
When MD is high, the data in the data latches is transferred to the data outputs. When $\overline{DS_1}$ is low and DS_2 is high, the data inputs are latched in the data latches. The low-level clear input $\overline{CLR}$ resets the data latches and sets the service request flip-flop SR, but the state of the output buffers is not changed.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7.0	V
V_I	Input voltage $\overline{DSI}$, MD inputs		V_{CC}	V
V_I	Input voltage all other inputs except $\overline{DSI}$, MD		5.5	V
V_O	Output voltage		V_{CC}	V
P_d	Power dissipation		800	mW
T_{opr}	Operating free-air temperature range		0~75	℃
T_{stg}	Storage temperature range		−55~125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			16	mA

ELECTRICAL CHARACTERISTICS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.85	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−5mA			−1	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_{IH}=2V V_{IL}=0.85V, I_{OH}=−1mA	3.65			V
V_{OL}	Low-level output voltage	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.85V, I_{OL}=15mA			0.45	V
I_{OZ}	Three-state output current	V_{CC}=5.25V, V_{IH}=2V, V_{IL}=0.85V, V_C=5.25V			20	μA
I_{OZ}	Three-state output current	V_{CC}=5.25V, V_{IH}=2V, V_{IL}=0.85V, V_O=0.45V			−20	μA
I_{IH}	High-level input current, STB DS2, $\overline{CLR}$, DI_1~DI_8 inputs	V_{CC}=5.25V, V_I=5.25V			10	μA
I_{IH}	High-level input current. MD input	V_{CC}=5.25V, V_I=5.25V			30	μA
I_{IH}	High-level input current, $\overline{DS_1}$ input	V_{CC}=5.25V, V_I=5.25V			40	μA
I_{IL}	Low-level input current. STB, DS2, $\overline{CLR}$, DI_1~DI_8 inputs	V_{CC}=5.25V, V_I=0.5V			−0.25	mA
I_{IL}	Low-level input current. MD input	V_{CC}=5.25V, V_I=0.5V			−0.75	mA
I_{IL}	Low-level input current. $\overline{DS_1}$ input	V_{CC}=5.25V, V_I=0.5V			−1	mA
I_{OS}	Short-circuit output current (Note 3)	V_{CC}=5.0V	−15		−75	mA
I_{CC}	Supply current from V_{CC}	V_{CC}=5.25V			130	mA

Note 1 : All voltage are with respect to GND terminal Reference voltage (pin 12) is considered as 0V and all maximum and minimum values are defined in absolute values.
2 : Current flowing into an IC is positive, out is negative. The maximum and minimum values are defined in absolute values
3 : All measurements should be done quickly, and two outputs should not be measured at the same time

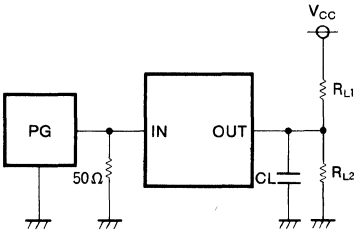
TIMING REQUIREMENTS (T_a=0~75℃, V_{CC}=5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(DS2)}$	Input pulse width, $\overline{DS_1}$, DS_2 and STB		30			ns
$t_{su(DA)}$	Data setup time with respect to $\overline{DS_1}$, DS_2 and STB		15			ns
$t_{h(DA)}$	Data hold time with respect to $\overline{DS_1}$, DS_2 and STB		20			ns

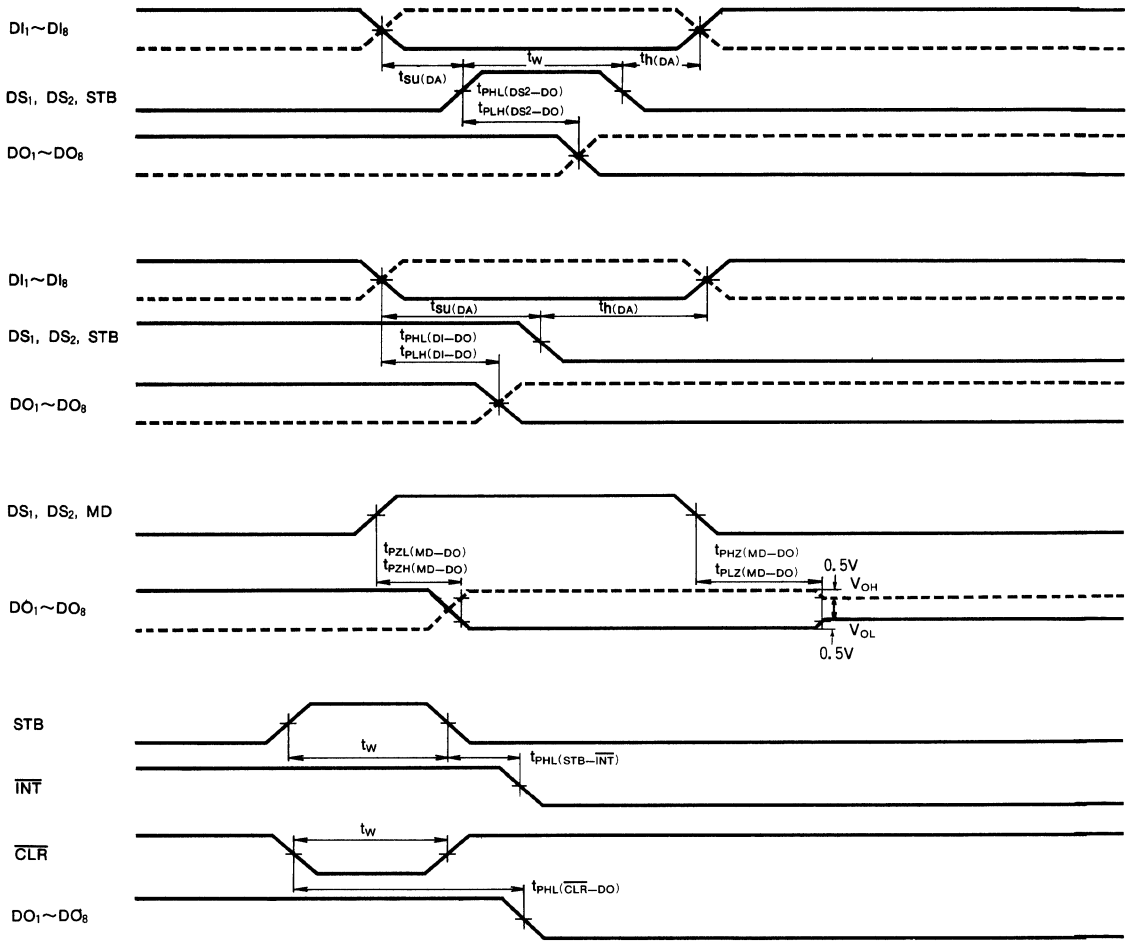
SWITCHING CHARACTERISTICS (T_a=0~75℃, V_{CC}=5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions (Note 4)	Limits			Unit
			Min	Typ	Max	
$t_{PHL(DI-DO)}$ / $t_{PLH(DI-DO)}$	High-to-low-level and low-to-high-level output propagation time, from input DI to output DO	C_L=30pF, R_{L1}=300Ω, R_{L2}=600Ω			30	ns
$t_{PHL(DS2-DO)}$ / $t_{PLH(DS2-DO)}$	High-to-low-level and low-to-high-level output propagation time. from input $\overline{DS1}$, DS2 and STB to output DO				40	ns
$t_{PHL(STB-\overline{INT})}$	High-to-low-level output propagation time, from input STB to output $\overline{INT}$				40	ns
$t_{PZL(MD-DO)}$	Z-to-low-level and Z-to-high-level output propagation	C_L=30pF, R_{L1}=300Ω, R_{L2}=600Ω			45	ns
$t_{PZH(MD-DO)}$	time, from inputs MD, $\overline{DS1}$ and DS2 to output DO	C_L=30pF, R_{L1}=10kΩ, R_{L2}=1kΩ				
$t_{PHZ(MD-DO)}$	High-to-Z-level and low-to-Z-level output propagation	C_L=5pF, R_{L1}=10kΩ, R_{L2}=1kΩ			45	ns
$t_{PLZ(MD-DO)}$	time, from inputs MD, $\overline{DS1}$ and DS2 to output DO	C_L=5pF, R_{L1}=300Ω, R_{L2}=600Ω				
$t_{PHL(\overline{CLR}-DO)}$	High-to-low-level output propagation time, from input $\overline{CLR}$ to output DO	C_L=30pF, R_{L1}=300Ω, R_{L2}=600Ω			55	ns

Note 4 : Test circuit



TIMING DIAGRAMS REFERENCE LEVEL=1.5V



M5L8216P / M5L8226P

4-BIT PARALLEL BIDIRECTIONAL BUS DRIVERS

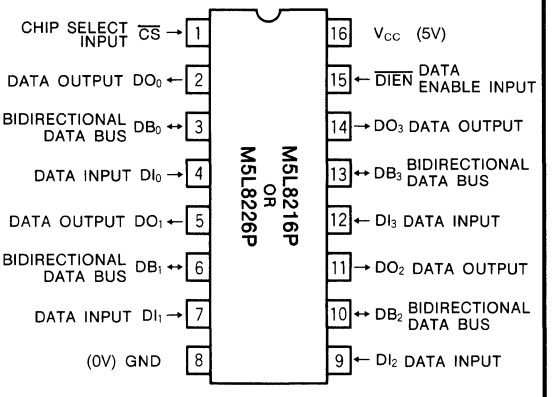
DESCRIPTION

The M5L8216P and M5L8226P are 4-bit bidirectional bus drivers and suitable for the 8-bit parallel CPU M5L8085AP.

FEATURES

- Parallel 8-bit data bus buffer driver
- Low input current $\overline{DIEN}$, $\overline{CS}$: $I_{IL}=-500\mu A$(max.)
  DI, DB: $I_{IL}=-250\mu A$(max.)
- High output current **M5L8216P**
  DB: $I_{OL}=55mA$(max.)
  $I_{OH}=-10mA$(max.)
  DO: $I_{OH}=-1mA$(max.)
  M5L8226P
  DB: $I_{OL}=50mA$(max.)
  $I_{OH}=-10mA$(max.)
  DO: $I_{OH}=-1mA$(max.)
- Outputs can be connected with the CPU M5L8085AP: $V_{OH}=3.65V$(min.)
- Three-state output

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

APPLICATION

Bidirectional bus driver/receiver for various types of microcomputer systems.

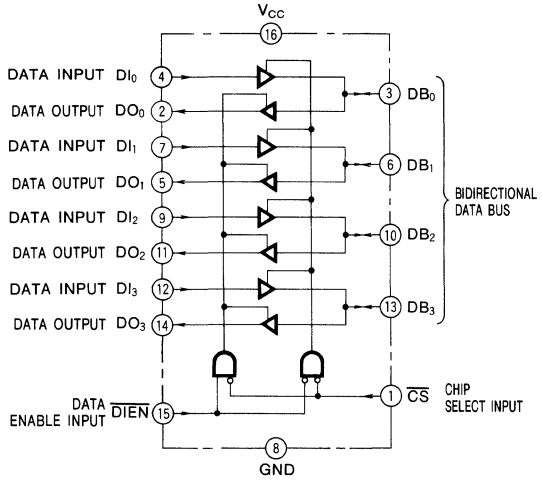
FUNCTION

The M5L8216P is a non-inverting and the M5L8226P is an inverting 4-bit bidirectional bus driver.

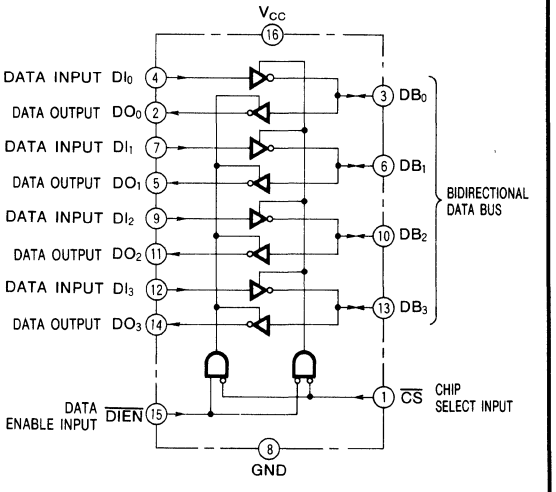
When the terminal $\overline{CS}$ is high-level, all outputs are in high-impedance state, and when low-level, the direction of the bidirectional bus can be controlled by the terminal $\overline{DIEN}$.

The terminal $\overline{DIEN}$ controls the data flow. The data flow control is performed by placing one of a pair of buffers in high-impedance state and allowing the other to transfer the data.

BLOCK DIAGRAM



M5L8216P



M5L8226P

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	7	V
V_I	Input voltage, $\overline{CS}$ $\overline{DIEN}$. DI inputs		5.5	V
V_I	Input voltage. DB input		V_{CC}	V
V_O	High-level output voltage		V_{CC}	V
P_d	Power dissipation	T_a=25℃	700	mW
T_{opr}	Operating free-air temperature range		0~75	℃
Tstg	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITONS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
I_{OH}	High-level output current. DO output			−1	mA
I_{OH}	High-level output current. DB output			−10	mA
I_{OL}	Low-level output current. DO output			15	mA
I_{OL}	Low-level output current. DB output			25	mA

ELECTRICAL CHARACTERISTICS (T_a=0~75℃, unless otherwise noted)

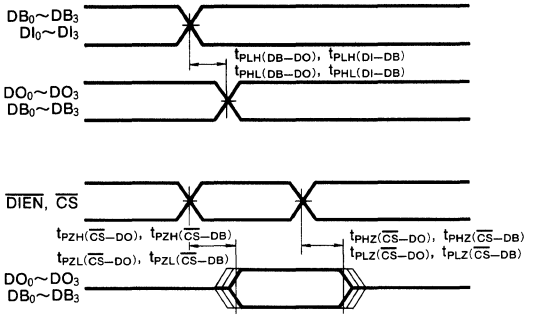
Symbol	Parameter		Conditions		Limits			Unit
					Min	Typ	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.95	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−5mA				−1	V
V_{OH}	High-level output voltage DO output		V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.95V	I_{OH}=−1mA	3.65			V
V_{OH}	High-level output voltage DB output			I_{OH}=−10mA	2.4			V
V_{OL1}	Low-level output voltage DO output			I_{OL}=15mA			0.45	V
V_{OL1}	Low-level output voltage. DB output			I_{OL}=25mA			0.45	V
V_{OL2}	Low-level output voltage DB output	M5L8216P		I_{OL}=55mA			0.6	V
		M5L8226P		I_{OL}=50mA			0.6	
I_{OZH}	Off-state output current. DO output		V_{CC}=5.25V	V_O=5.25V			20	μA
I_{OZH}	Off-state output current. DB output						100	μA
I_{OZL}	Off-state output current. DO output			V_O=0.45V			−20	μA
I_{OZL}	Off-state output current DB output						−100	μA
I_{IH}	High-level input current $\overline{DIEN}$ $\overline{CS}$ inputs		V_{CC}=5.25V, V_{IH}=4.5V				20	μA
I_{IH}	High-level input current. DI, DB inputs						10	μA
I_{IL}	Low-level input current. $\overline{DIEN}$ $\overline{CS}$ inputs		V_{CC}=5.25V, V_{IH}=4.5V				−500	μA
I_{IL}	Low-level input current. DI, DB input						−250	μA
I_{OS}	Short-circuit output DO output (Note 2)		V_{CC}=5.25V, V_O=0V		−15		−65	mA
I_{OS}	Short-circuit output DB output (Note 2)				−30		−120	mA
I_{CC}	Supply current	M5L8216P	V_{CC}=5.25V				100	mA
		M5L8226P					100	
I_{CCZ}	Supply current z	M5L8216P					120	mA
		M5L8226P					100	

Note 1 · Current flowing into an IC is postive, out is negative
2 · All measurements should be done quickly, and not more than one output should be shorted at a time

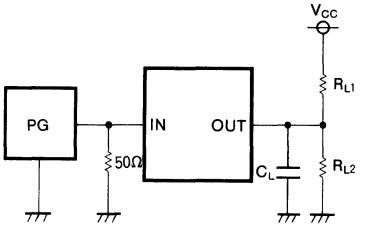
SWITCHING CHARACTERISTICS (V_{CC}=5V±5%, T_a=25℃, unless otherwise noted)

Symbol	Parameter		Test conditions (Note 3)	Limits Min	Limits Typ	Limits Max	Unit
$t_{PHL(DB-DO)}$ $t_{PLH(DB-DO)}$	High-to-low and low-to-high output propagation time. from input DB to output DO		C_L=30pF, R_{L1}=300Ω, R_{L2}=600Ω			25	ns
$t_{PHL(DI-DB)}$ $t_{PLH(DI-DB)}$	High-to-low and low-to-high output propagation time. from input DI to output DB	M5L8216P	C_L=300pF, R_{L1}=90Ω, R_{L2}=180Ω			30	ns
		M5L8226P				25	
$t_{PHZ(\overline{CS}-DO)}$ $t_{PLZ(\overline{CS}-DO)}$	High-to-Z and low-to-Z output propagation time. from inputs $\overline{DIEN}$ $\overline{CS}$. to output DO		C_L=5pF, R_{L1}=10kΩ, R_{L2}=1kΩ C_L=5pF, R_{L1}=300Ω, R_{L2}=600Ω			35	ns
$t_{PZH(\overline{CS}-DO)}$	Output enable time. from inputs $\overline{DIEN}$ $\overline{CS}$ to output DO	M5L8216P	C_L=30pF, R_{L1}=10kΩ, R_{L2}=1kΩ			65	ns
		M5L8226P				54	
$t_{PZL(\overline{CS}-DO)}$		M5L8216P	C_L=30pF, R_{L1}=300Ω, R_{L2}=600Ω			65	ns
		M5L8226P				54	
$t_{PHZ(\overline{CS}-DB)}$ $t_{PLZ(\overline{CS}-DB)}$	Output disable time. from inputs $\overline{DIEN}$. $\overline{CS}$ to output DB		C_L=5pF, R_{L1}=10kΩ, R_{L2}=1kΩ C_L=5pF, R_{L1}=90Ω, R_{L2}=180Ω			35	ns
$t_{PZH(\overline{CS}-DB)}$	Output enable time from inputs $\overline{DIEN}$. $\overline{CS}$. to output DB	M5L8216P	C_L=300pF, R_{L1}=10kΩ, R_{L2}=1kΩ			65	ns
		M5L8226P				54	
$t_{PZL(\overline{CS}-DB)}$		M5L8216P	C_L=300pF, R_{L1}=90Ω, R_{L2}=180Ω			65	ns
		M5L8226P				54	

TIMING DIAGRAM (Reference level=1.5V)



Note 3 : Test circuit



APPLICATION EXAMPLES

Fig. 1 shows a pair of M5L8216Ps or M5L8226Ps which are directly connected with the 8080A CPU data bus, and their control signal. Fig. 2 shows an example circuit in which the M5L8216P or M5L8226P is used as an interface for memory and I/O to a bidirectional bus.

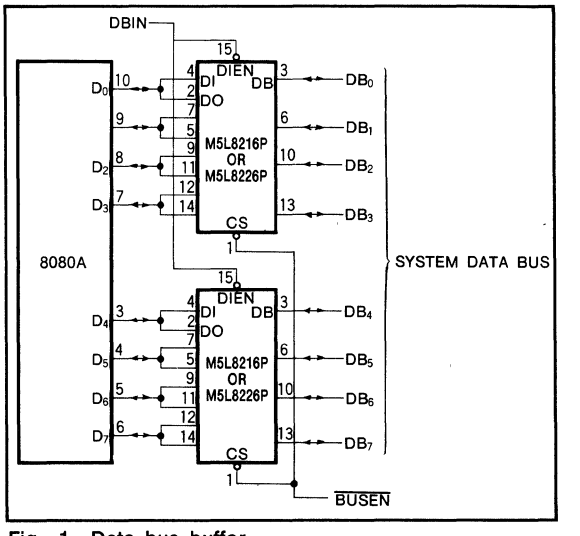


Fig. 1 Data bus buffer

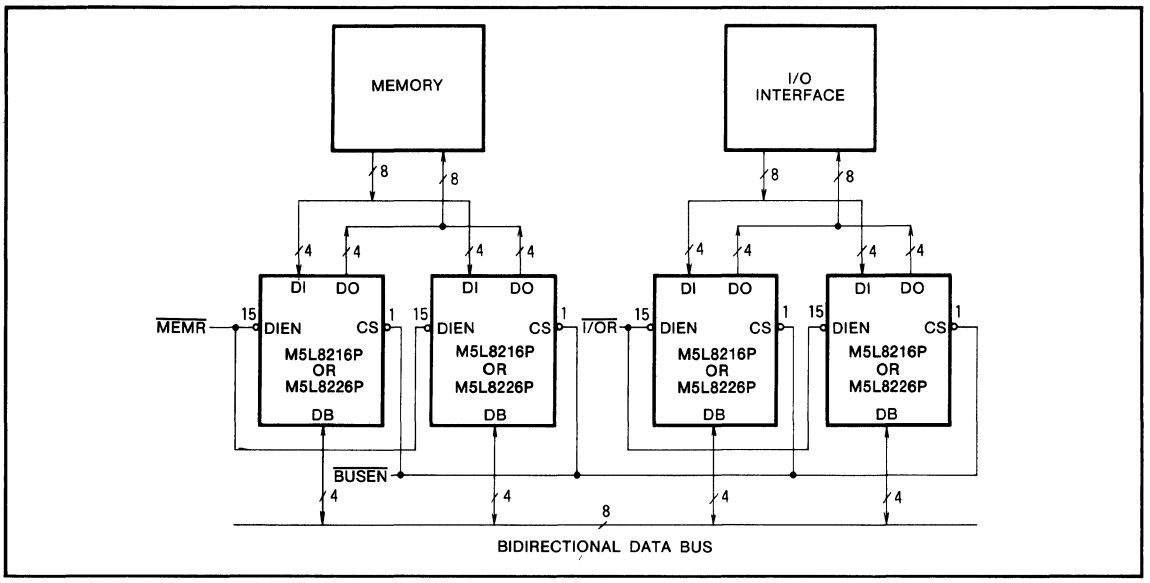


Fig. 2 Memory and I/O interface to bidirectional data bus

PRECAUTIONS FOR USE

When the M5L8216P data input or two-way data bus is set to high to disable-output from the two-way bus or data output, care is required as a low glitch of approximate width 10ns will be generated.

MELPS 86/88 MICROPROCESSORS

3

M5L8282P/M5L8283P

OCTAL LATCH

DESCRIPTION

The M5L8282P and M5L8283P are semiconductor integrated circuits consisting of sets of eight 3-state latches for use with various types of microprocessors.

FEATURES

- 3-state, high-fanout output ····· (I_{OL}=32mA, I_{OH}=−5mA)
- Low power dissipation

APPLICATION

Data latches for various microcomputer systems

FUNCTION

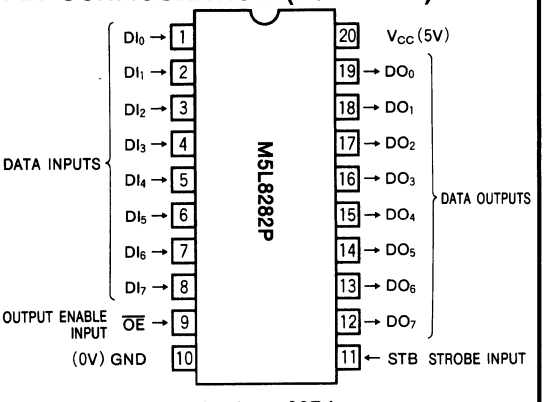
The M5L8282P and M5L8283P are latches with non-inverted and inverted outputs, respectively.

When the strobe input STB is high, the data inputs DI_0~DI_7 are passed through the data outputs DO_0 ~ DO_7 (M5L8282P) or to the data outputs $\overline{DO_0}$~$\overline{DO_7}$ (M5L8283P), changes in the DI_0~DI_7 signals being reflected in the data outputs.

If the STB is changed from high to low, the data DI_0~DI_7 just before the change is latched. If the DI data is changed while STB is low, this change is not reflected in the data outputs.

When $\overline{OE}$ is made high, all the data outputs go into the high-impedance state, the data latched prior to $\overline{OE}$ going high being held.

PIN CONFIGURATION (TOP VIEW)



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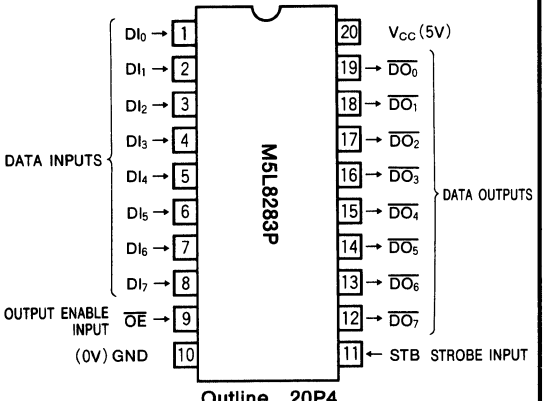
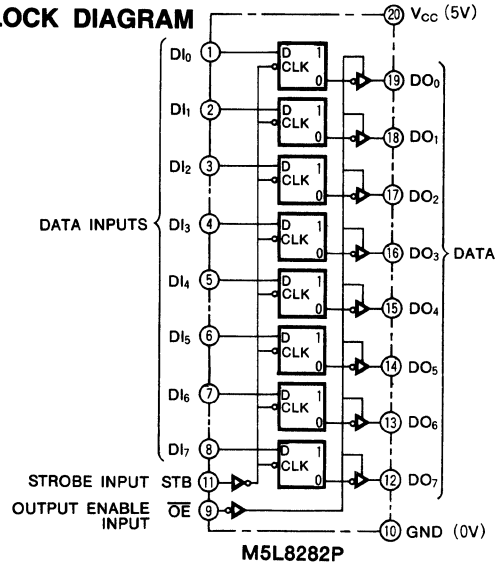
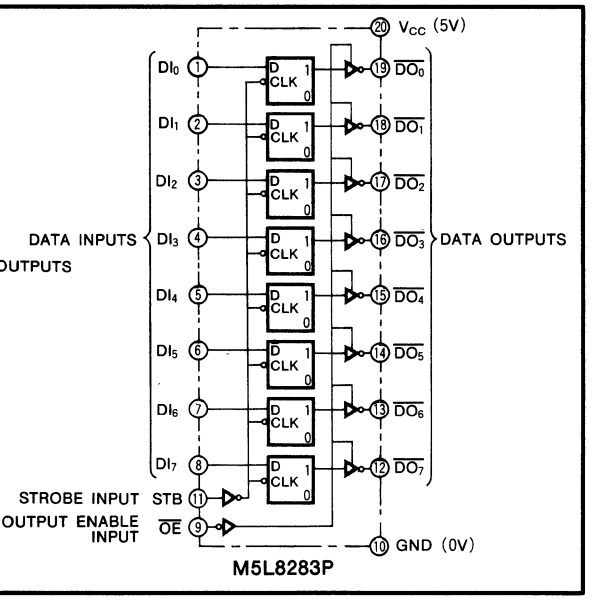


Outline 20P4

BLOCK DIAGRAM



M5L8282P



M5L8283P

ABSOLUTE MAXIMUM RATINGS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7	V
V_I	Input voltage		−0.5~+5.5	V
V_O	Output voltage		−0.5~V_{CC}	V
T_{opr}	Operating free-air temperature range		0~+75	℃
T_{stg}	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
I_{OH}	High-level output current	V_{OH}≧2.4V	0		−5	mA
I_{OL}	Low-level output current	V_{OL}≦0.45V	0		32	mA

ELECTRICAL CHARACTERISTICS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−5mA			−1	V
V_{OH}	High-level output voltage	V_{CC}=4.5V, I_{OH}=−5mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=32mA			0.45	V
I_{OZH}	Off-state output current, high-level applied to the output	V_{CC}=5.5V, V_I=2V, V_O=5.25V			50	μA
I_{OZL}	Off-state output current, low-level applied to the output	V_{CC}=5.5V, V_I=2V, V_O=0.4V			−50	μA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=5.25V			50	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.45V			−0.2	mA
I_{CC}	Supply current	V_{CC}=5.5V			80	mA
C_{IN}	Input capacitance	F=1MHz, V_{BIAS}=2.5V, V_{CC}=5V, T_a=25℃			12	pF

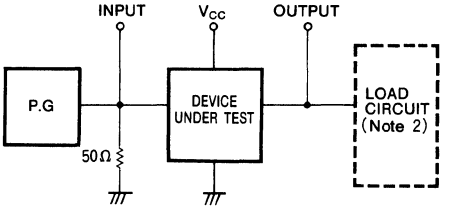
SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Alternate symbol	Test conditions	M5L8282P			M5L8283P			Unit
				Limits			Limits			
				Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation time from DI input to DO or $\overline{DO}$ for low-to-high or high-to-low change	T_{IVOV}	(Note 1)	5		30	5		22	ns
t_{PLH} t_{PHL}	Propagation time from STB input to DO or $\overline{DO}$ for low-to-high and high-to-low change	T_{SHOV}		10		45	10		40	ns
t_{PZH} t_{PZL}	Propagation time from $\overline{OE}$ input to DO or $\overline{DO}$ output when output is enabled	T_{ELOV}		10		30	10		30	ns
t_{PHZ} t_{PLZ}	Propagation time from $\overline{OE}$ input to DO or DO output when the output is disabled	T_{EHOV}		5		18	5		18	ns

TIMING REQUIREMENTS (V_{CC}=5V±10%, T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Alternate symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{W(STBH)}$	Strobe STB high pulse width	T_{SHSL}		15			ns
t_{su}	Strobe STB setup time for DI_0~DI_7	T_{IVSL}		0			ns
t_h	STB hold time for DI_0~DI_7	T_{SLIX}		25			ns

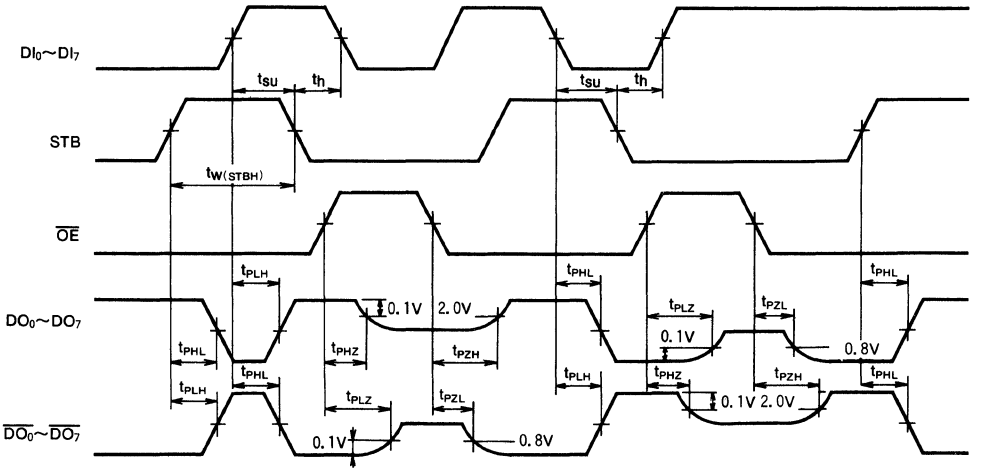
Note 1 : Test Circuit



Note 2 :

TEST ITEM	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
LOAD CIRCUIT	2.14V, 52.7Ω, 300pF	1.5V, 33Ω, 300pF	1.5V, 180Ω, 300pF

TIMING DIAGRAM (Reference voltage=1.5V)

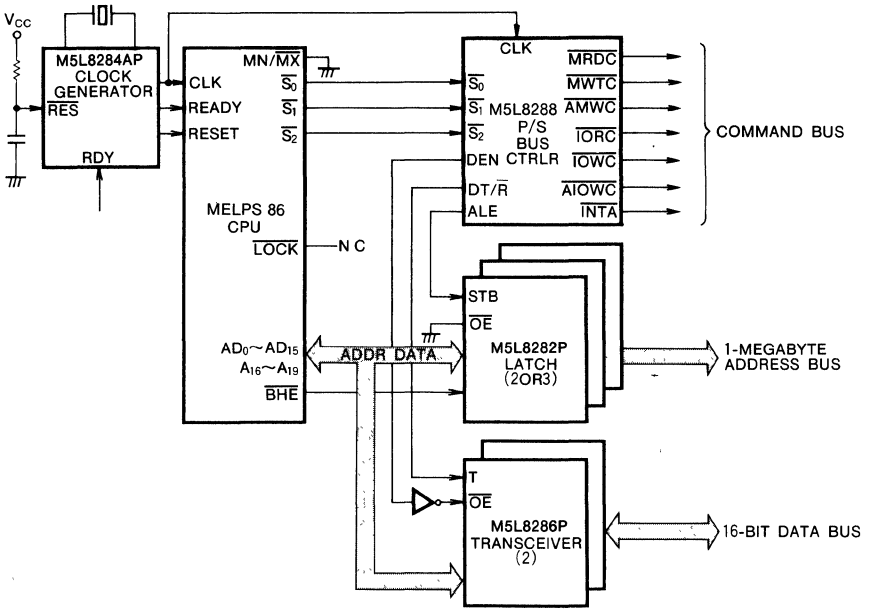


PRECAUTIONS FOR USE

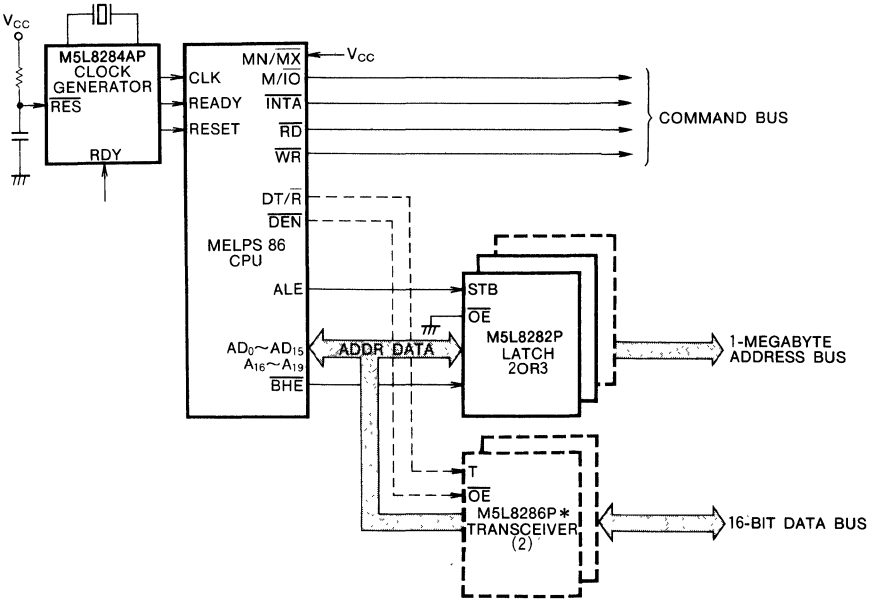
Care should be taken to accommodate the glitch that is generated when STB goes from low to high with the output low for the M5L8283P.

APPLICATION EXAMPLES

(1) Use in the maximum mode



(2) Use in the minimum mode



* : Option
Required when the number of devices driving the bus increases

M5L8284AP

CLOCK GENERATOR AND DRIVER

DESCRIPTION

The M5L8284AP is a clock generator and driver for use with the MELPS 86, 88 processors.

It has a synchronous delay circuit and synchronous control circuit capable of controlling two Multibus (Intel trademark) circuits.

FEATURES

- Crystal controlled stable output frequency
- Capable of synchronous operation with other M5L8284APs
- External frequency input
- A power-on reset by means of an external capacitor and resistor

APPLICATION

Clock driver and generators and driver for MELPS 86, 88

FUNCTION

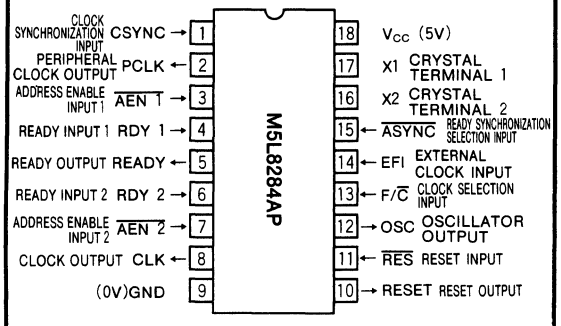
The M5L8284AP is a clock generator/driver for the MELPS 86, 88 microprocessors.

The chip contains a crystal controlled oscillator, a divided-by-3 counter, a peripheral clock output provided divided-by-2 counter, a reset circuit and ready circuit to ensure synchronization to the CLK signal.

The reset input $\overline{RES}$ is used to generate the reset output $\overline{RESET}$ as the CPU reset synched to the CLK signal. A Schmitt trigger is used at the input side.

Thus, a reset signal can be output at power on by connecting a capacitor and resistor to the $\overline{RES}$ input.

PIN CONFIGURATION (TOP VIEW)



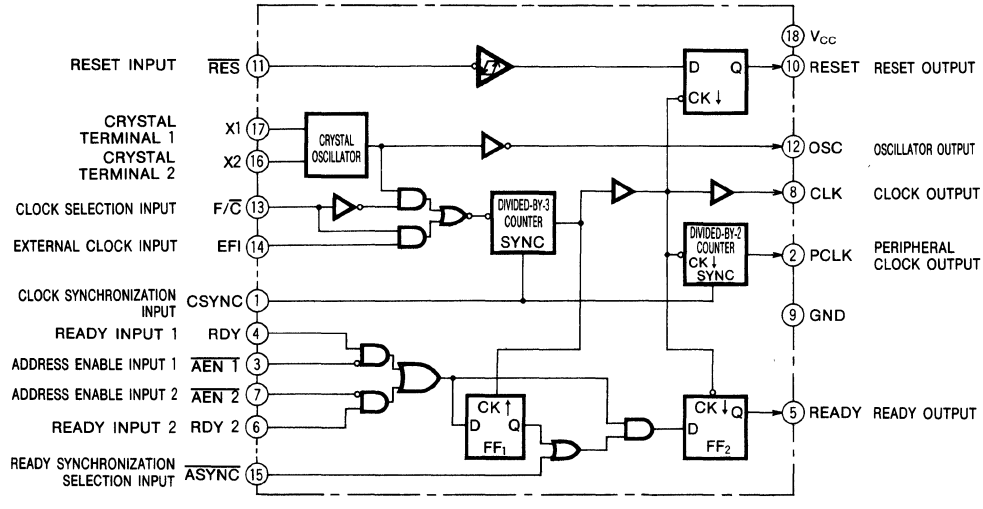
Outline 18P4

The frequency/crystal selection input F/$\overline{C}$ can be used to select the crystal oscillator circuit output or an external clock input as the input for the divide-by-three counter.

By using these pins, the M5L8284AP output can be used to drive multiple M5L8284AP devices.

The clock synchronization input CSYNC is used to operate multiple M5L8284APs in sync.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin	Name	Input or output	Function
$\overline{AEN1}$, $\overline{AEN2}$	Address enable input	Input	When $\overline{AEN1}$ and $\overline{AEN2}$ are set low, RDY1 and RDY2 are enabled, respectively. By using these two inputs separately, the CPU can be used to access two Multibusses. When not used as a multimaster, $\overline{AEN}$ should be set to low. These inputs are active low.
RDY1, RDY2	Bus ready input	Input	These inputs are connected to the output signal indicating the completion of data reception from a system bus device or, indicating that data is valid RDY1 and RDY2 are enabled when AEN1 and AEN2 are low, respectively. These inputs are active high.
$\overline{ASYNC}$	Active low input	Input	This signal is used to select the synchronization mode of the READY signal generation circuit. When the $\overline{ASYNC}$ signal is set low, the READY signal is generated in two synchronization steps. When the $\overline{ASYNC}$ signal is set high, the READY signal is generated in one step
READY	Ready output	Output	The state of RDY appears at this output in synchronization with the CLK output This is done to synchronize the READY output to the M5L8284AP internal clock because the RDY input generation is unrelated to the CLK signal. This pin is normally connected to the CPU ready input and cleared after the required hold CPU time has elapsed.
X_1, X_2	Crystal element terminals	Input	These pins are used to connect the crystal. The crystal frequency is 3 times of CPU clock frequency The crystal should be in the 12-25MHz range with the series resistance as possible as small. Care should be taken that these pins are not shorted to ground
F/$\overline{C}$	Clock selection input	Input	When F/$\overline{C}$ is set low, CLK and PCLK outputs are driven from the crystal oscillator circuit When it is set high, they are driven from the EFI input.
EFI	External clock input	Input	When F/$\overline{C}$ is set high, CLK and PCLK output signals are driven from this pin. A TTL level rectangular signal and three times of the CPU frequency should be used.
CLK	Clock output	Output	This output is connected to the clock inputs of the CPU and the peripheral devices on the local bus. The output waveform is 1/3 the frequency of the crystal oscillator connected at X_1 and X_2 or the signal applied to the FEI input, and has a duty cycle of 1/3. Since for V_{CC}=5V, V_{OH}=4.5V, this output can be directly drive the CPU clock input.
PCLK	Peripheral clock output	Output	This output provides a clock signal for use with peripheral devices. The output waveform is 50% duty cycle TTL level rectangular waveform with a frequency 1/2 that of the clock output.
OSC	Oscillator output	Output	This output is a TTL level crystal oscillator output. The frequency is the same as that of the crystal connected at X_1 and X_2, but care should be taken as the frequency will be unstable if these pins are left open.
$\overline{RES}$	Reset input	Input	This active low input is used to generate the reset output signal for the CPU The input is a schmitt trigger input so that by connecting a capacitor and a resistor, the CPU reset signal can be generated at power on.
RESET	Reset output	Output	This pin is connected to the CPU reset input. The signal at this pin is synchronized the $\overline{RES}$ input with the CLK signal. This output is active high.
CSYNC	Clock synchronization input	Input	When using multiple M5L8284AP devices, this input is used as a clock synchronization input When CSYNC is high, the internal counter of the M5L8284AP is reset and when CSYNL is low, it begins operation. CSYNC must be synchronized with EFI. See application notes.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~7	V
V_I	Input voltage		−0.5~5.5	V
V_O	Output voltage		−0.5~V_{CC}	V
T_{opr}	Operating free-air temperature range		0~75	℃
T_{stg}	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
I_{OH}	High-level output current	CLK V_{OH}=4V	0		−1	mA
		Other outputs V_{OH}=2.4V				
I_{OL}	Low-level output current	V_{OL}≦0.45V	0		5	mA

ELECTRIC CHARACTERISTICS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	$\overline{RES}$		2.6			V
		Other inputs $\overline{RES}$		2			
V_{IL}	Low-level input voltage					0.8	V
$V_{T+}-V_{T-}$	Hysteresis width	$\overline{RES}$	V_{CC}=5V	0.25			V
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−5mA			−1	V
V_{OH}	High-level output voltage	CLK	V_{CC}=4.5V, I_{OH}=−1mA	4			V
		Other outputs CLK		2.4			
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=5mA			0.45	V
I_{IH}	High-level input current		V_{CC}=5.5V, V_I=5.25V			50	μA
I_{IL}	Low-level input current	ASYNC	V_{CC}=5.5V, V_I=0.45V			−1.3	mA
		Other inputs ASYNC				−0.5	
I_{CC}	Supply current		V_{CC}=5.5V			162	mA

SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Alternate symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
T_C	CLK repetition period	t_{CLCL}		100			ns
$T_{W(CLKH)}$	CLK high pulse width	t_{CHCL}	(Note 5 a, b) $CLKF_{req}$≦8MHz	($\frac{1}{3}t_{CLCL}$)+2			ns
			$CLKF_{req}$=10MHz	39			
$T_{W(CLKL)}$	CLK low pulse width	t_{CLCH}	(Note 5 a, b) $CLKF_{req}$≦8MHz	($\frac{2}{3}t_{CLCL}$)−15			ns
			$CLKF_{req}$=10MHz	53			
t_{TLH}	CLK low-high transition time	t_{CH1CH2}	1~3.5V			10	ns
t_{THL}	CLK high-low transition time	t_{CL2CL1}	3.5~1V			10	ns
$T_{W(PCLKH)}$	PCLK high pulse width	t_{PHPL}		t_{CLCL}−20			ns
$T_{W(PCLKL)}$	PCLK low pulse width	t_{PLPH}		t_{CLCL}−20			ns
t_{dIV}	READY inhibit time with respect to CLK (Note 1)	t_{RYLCL}	(Note 5 c, d)	−8			ns
t_{dV}	READY enable time with respect to CLK (Note 2)	t_{RYHCH}	(Note 5 c, d) $CLKF_{req}$≦8MHz	53			ns
			$CLKF_{req}$=10MHz				
$T_{DHL(CLK-RESET)}$	High-low delay time from CLK to RESET	t_{CLIL}				40	ns
$T_{DLH(CLK-PCLK)}$	Low-high delay time from CLK to PCLK	t_{CLPH}				22	ns
$T_{DHL(CLK-PCLK)}$	High-low delay time from CLK to PCLK	t_{CLPL}				22	ns
$T_{DLH(OSC-CLK)}$	Low-high delay time from OSC to CLK	t_{OLCH}		−5		22	ns
$T_{DHL(OSC-CLK)}$	High-low delay time from OSC to CLK	t_{OLCL}		2		35	ns
T_r	Output rise time	t_{OLOH}	0.8~2V (except CLK)			20	ns
t_f	Output fall time	t_{OHOL}	2~0.8V (except CLK)			12	ns

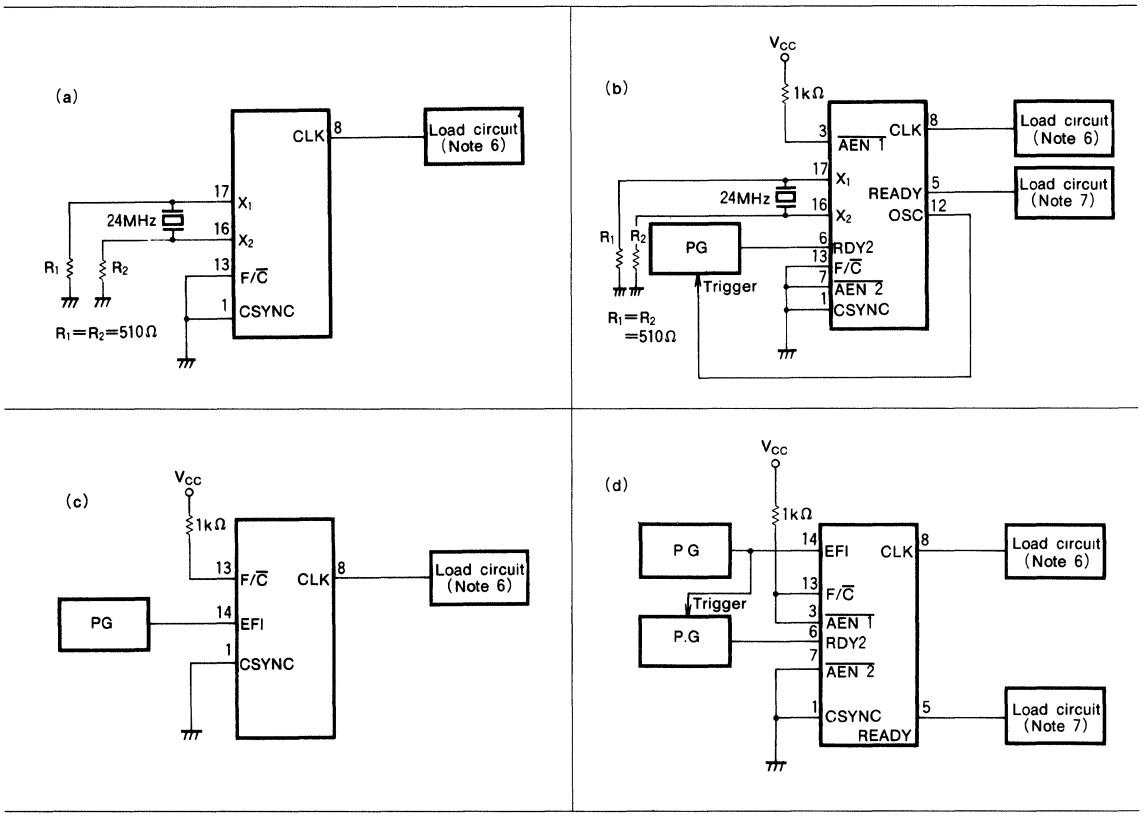
Note 1 : Applies to T2 state time
2 : Applies to T3 and TW state times

TIMING REQUIREMENTS (V_{CC}=5V ±10%, T_a=0~75℃, unless otherwise noted)

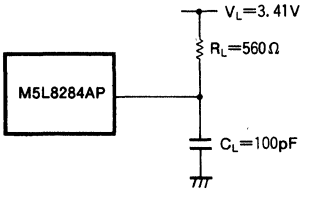
Symbol	Parameter	Alternate symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$f_{(xtal)max}$	Crystal frequency			12		25	MHz
$t_{W(EFIH)}$	EFI high pulse width	t_{EHEL}	90%−90%V_{IN}	13			ns
$t_{W(EFIL)}$	EFI low pulse width	t_{ELEH}	10%−10%V_{IN}	13			ns
$T_{C(EFI)}$	EFI repetition period (Note 3)	t_{ELEL}		$t_{EHEL}+t_{ELEH}+\delta$			ns
$t_{SU(RDY)}$	RDY1 and RDY2 active setup time with respect to CLK	t_{RIVCL}	$\overline{ASYNC}$=HIGH	35			ns
$t_{SU(RDY)}$	RDY1 and RDY2 active hold time with respect to CLK	t_{RIVCH}	$\overline{ASYNC}$=LOW	35			ns
$t_{SU(RDY)}$	RDY1 and RDY2 inactive setup time with respect to CLK	t_{RIVCL}		35			ns
$t_{h(RDY)}$	RDY1 and RDY2 hold time with respect to CLK	t_{CLRIX}		0			ns
$t_{SU(\overline{ASYNC})}$	$\overline{ASYNC}$ setup time with respect to CLK	t_{AYVCL}		50			ns
$t_{h(\overline{ASYNC})}$	$\overline{ASYNC}$ hold time with respect to CLK	t_{CLAYX}		0			ns
$t_{SU(AEN)}$	$\overline{AEN1}$ and $\overline{AEN2}$ setup time with respect to RDY1 and RDY2	t_{AIVRIV}		15			ns
$t_{h(AEN)}$	$\overline{AEN1}$ and $\overline{AEN2}$ hold time with respect to CLK	t_{CLAIX}		0			ns
$t_{SU(CSYNC)}$	CSYNC setup time with respect to EFI	t_{YHEH}		20			ns
$t_{h(CSYNC)}$	CSYNC hold time with respect to EFI	t_{EHYL}		20			ns
$t_{W(CSYNC)}$	CSYNC pulse width	t_{YHYL}		$2t_{ELEL}$			ns
$t_{SU(\overline{RES})}$	$\overline{RES}$ setup time with respect to CLK (Note 4)	t_{I1HCL}		65			ns
$t_{h(\overline{RES})}$	$\overline{RES}$ hold time with respect to CLK (Note 4)	t_{CLI1H}		20			ns
t_r	Input rise time	t_{ILIH}	0.8~2V			20	ns
t_f	Input fall time	t_{IHIL}	2~0.8V			12	ns

Note 3 : $\delta = t_r$(5ns max)+EFI + t_f(5ns max)+EFI
4 : $t_{SU(\overline{RES})}$ and $t_{h(\overline{RES})}$ are theoretically only to guarantee logic in the next clock period

Note 5 : Test Circuits

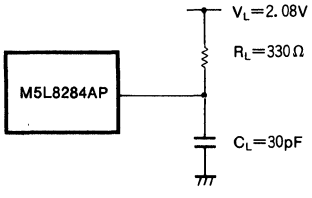


Note 6 : Load Circuit



CLK pins

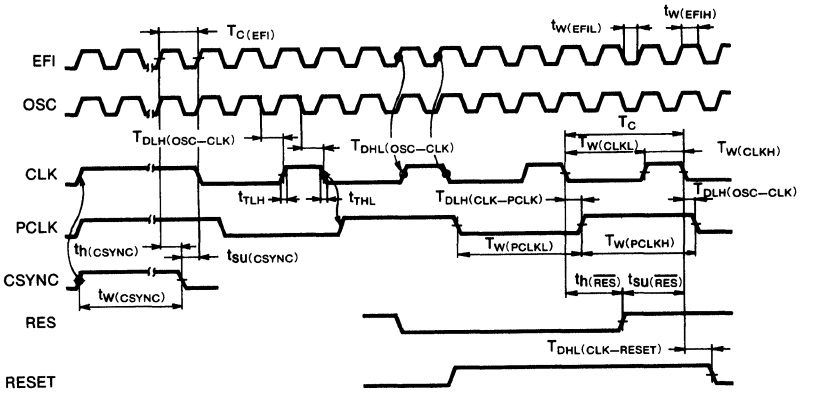
Note 7 : Load circuit



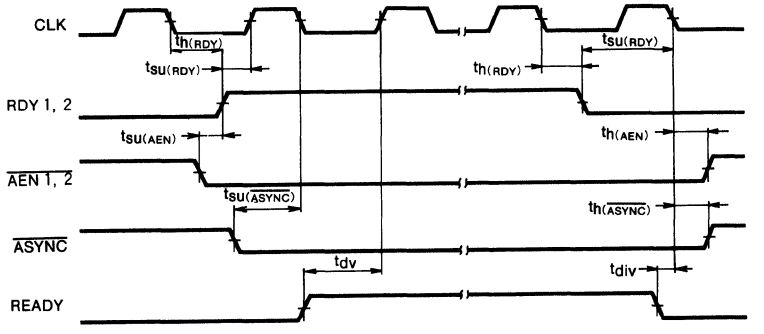
Other pins

TIMING DIAGRAM (Reference level=1.5V)

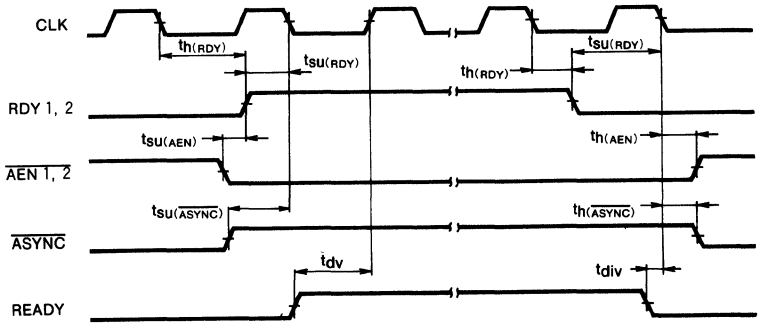
CLK, RESET Signals



READY Signal (with asynchronous device)

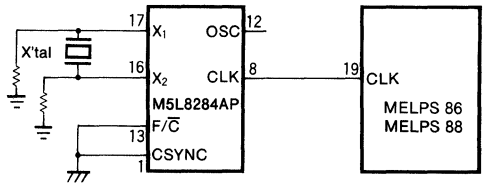


READY Signal (with synchronous device)



APPLICATION NOTES

(1) Connecting the crystal

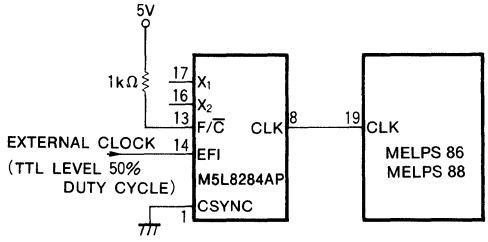


The crystal frequency should be three times the cycle time of the 8086, 8088 or 8089, and the crystal should be located as close to the M5L8284AP as possible.

PRECAUTIONS FOR USE

(1) The oscillator circuit of the M5L8284AP is designed for use with the fundamental mode crystal.
If noise is allowed to enter the XTAL1, XTAL2 or V_{CC} pins, the oscillator frequency will be pulled of the parallel resident frequency and the stray capacitance between XTAL1 and XTAL2 may cause the circuit to go into relaxation oscillation. To prevent this, care should be given to the following points.
(1) The should be one with a small parallel capacitance.
(2) A 0.01 — 0.1μF capacitor should be connected between V_{CC} and ground. This capacitor should be located as close as possible to the IC.

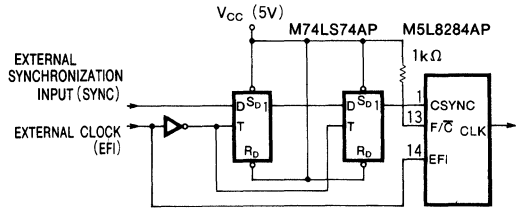
(2) External clock connections



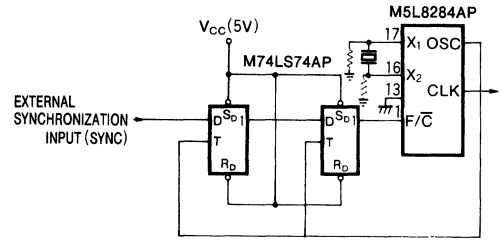
The frequency should be three times the CPU cycle frequency

(3) Synchronizing using the CSYNC input

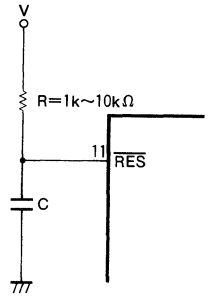
● When the EFI input is used



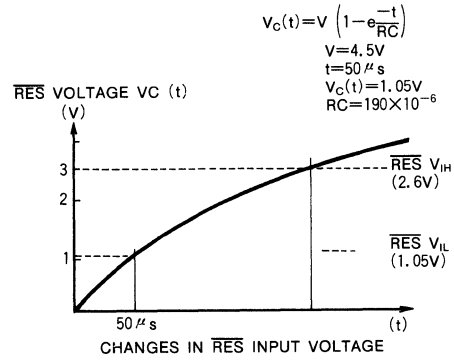
● When the EFI input is not used



(4) Power-on reset circuit



Since the MELPS 86, 88 require a reset pulse over 50μs after V_{CC} reaches 4.5V upon power on, the capacitor value should be determined by the graph shown below. Note that the time for V_{CC} to reach 4.5V has not been considered, so that it is necessary to choose the characteristics value of capacitance under consideration of the power supply.

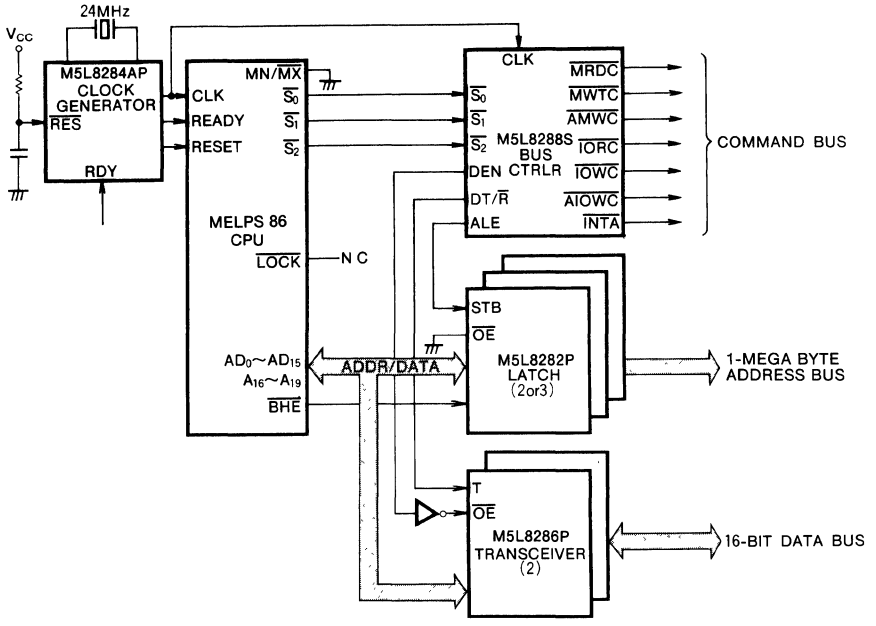


CHANGES IN $\overline{RES}$ INPUT VOLTAGE

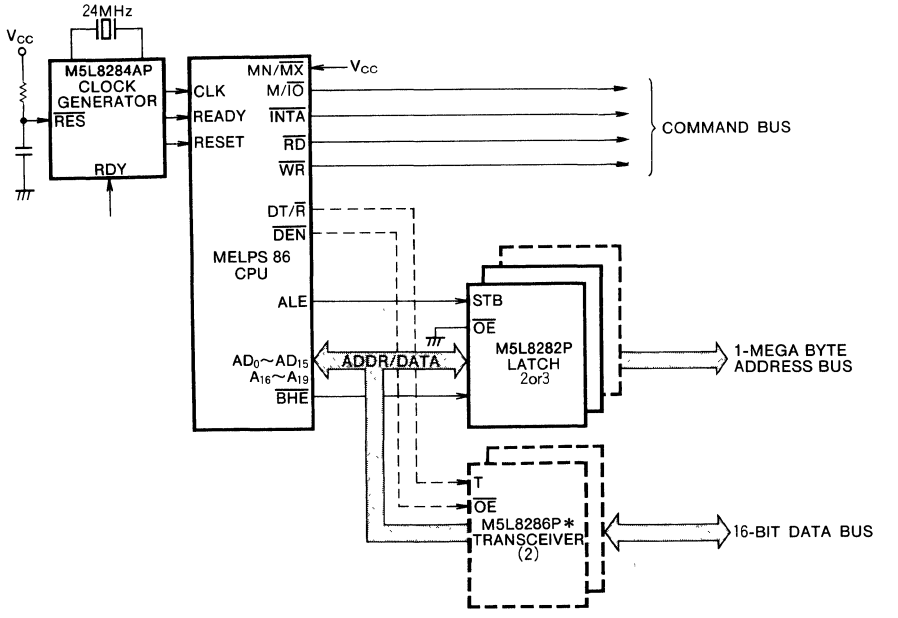
MITSUBISHI ELECTRIC

APPLICATION EXAMPLES

(1) Use in the maximum mode



(2) Use in the minimum mode



* : Option
Required when the number of devices driving the bus increases

M5L8286P/M5L8287P

OCTAL BUS TRANSCEIVER

DESCRIPTION

The M5L8286P and M5L8287P are semiconductor integrated circuits consisting of a set of eight 3-state output bus transceivers for use with a variety of microprocessor systems.

FEATURES

- 3-state, high-fanout outputs (I_{OL}=16mA, I_{OH}=−1mA for the A outputs and I_{OL}=32mA, I_{OH}=−5mA for the B outputs)
- Low power dissipation

APPLICATION

Two-way bus transceivers for microcomputer systems

FUNCTION

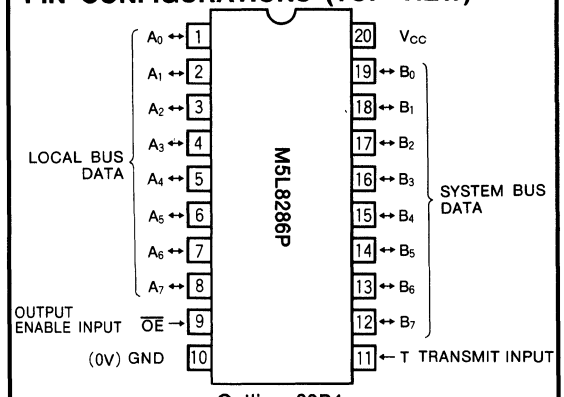
The M5L8286P and M5L8287P are two-way bus transceivers with non-inverted and inverted outputs respectively.

When the output enable input $\overline{OE}$ is high, the local bus data pins $A_0 \sim A_7$ and system data pins $B_0 \sim B_7$ are both placed in the high-impedance state.

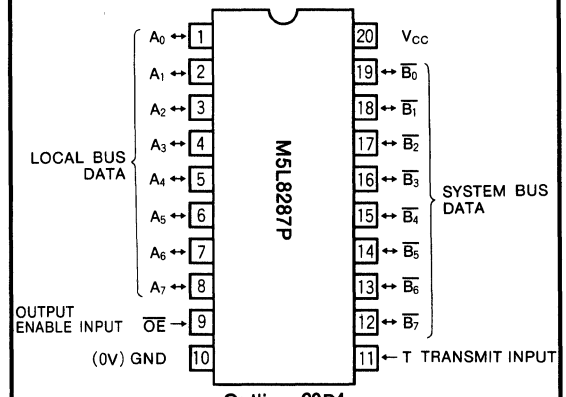
When the output enable input $\overline{OE}$ is low, the input and output states are controlled by the transmit input T.

When T is high, $A_0 \sim A_7$ are input pins and $B_0 \sim B_7$ are output pins. When T is low, $B_0 \sim B_7$ are input pins and $A_0 \sim A_7$ are output pins.

PIN CONFIGURATIONS (TOP VIEW)

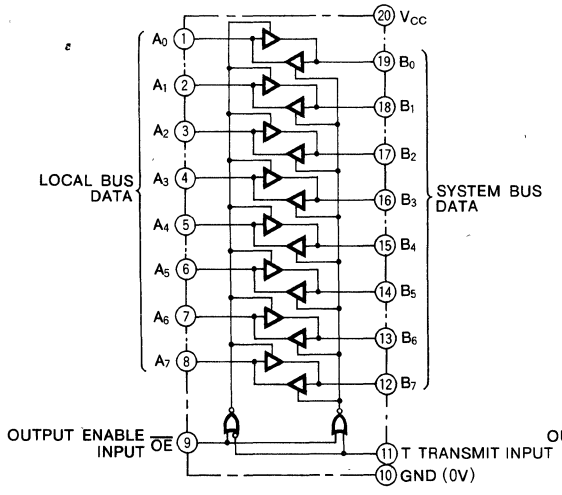


Outline 20P4

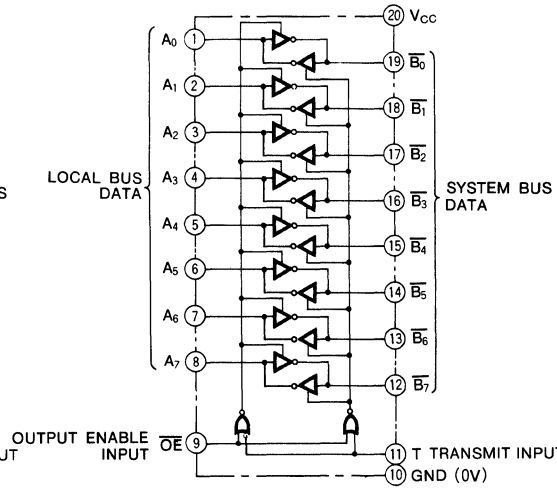


Outline 20P4

BLOCK DIAGRAM



M5L8286P



M5L8287P

MITSUBISHI ELECTRIC

FUNCTION TABLES (Note 1)

M5L8286P

$\overline{OE}$	T	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

M5L8287P

$\overline{OE}$	T	A	B
L	L	$\overline{O}$	I
L	H	I	$\overline{O}$
H	X	Z	Z

Note 1 : I : Input pin
O, $\overline{O}$: Output pin (non-inverted for the M5L8286P and inverted for the M5L8287P)
Z : Indicated the high-impedance state (A and B are separated)
X : Either high or low

ABSOLUTE MAXIMUM RATINGS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7	V
V_I	Input voltage		−0.5~+5.5	V
V_C	Output voltage		−0.5~V_{CC}	V
T_{opr}	Operating free-air temperature range		0~+75	℃
T_{stg}	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min	Nom	Max	
V_{CC}	Supply voltage			4.5	5	5.5	V
I_{OH}	High-level output current	V_{OH}≧2.4V	A output	0		−1	mA
			B output	0		−5	
I_{OL}	Low-level output current	V_{OL}≦0.45V	A output	0		16	mA
			B output	0		32	

ELECTRICAL CHARACTERISTICS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage	A input					0.8	V
		B input					0.9	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−5mA				−1	V
V_{OH}	High-level output voltage	A output	V_{CC}=4.5V, I_{OH}=−1mA		2.4			V
		B output	V_{CC}=4.5V, I_{OH}=−5mA		2.4			V
V_{OL}	Low-level output voltage	A output	V_{CC}=4.5V, I_{OL}=16mA				0.45	V
		B output	V_{CC}=4.5V, I_{OL}=32mA				0.45	V
I_{OZH}	Off-state output current with high-level applied at the output	A output	V_{CC}=5.5V, V_I=2V	V_I=0.8V			50	μA
		B output	V_O=5.25V	V_I=0.9V				
I_{OZL}	Off-state output current with low-level applied the output	A output	V_{CC}=5.5V, V_I=2V	V_I=0.8V			−0.2	mA
		B output	V_O=0.45V	V_I=0.9V				
I_{IH}	High-level input current		V_{CC}=5.5V, V_I=5.25V				50	μA
I_{IL}	Low-level input current		V_{CC}=5.5V, V_I=0.45V				−0.2	mA
I_{CC}	Supply current	M5L8286P	V_{IC}=5.5V				110	mA
		M5L8287P					110	
C_{IN}	Input capacitance		F=1MHz, V_{BIAS}=2.5V V_{CC}=5V, T_a=25℃				12	pF

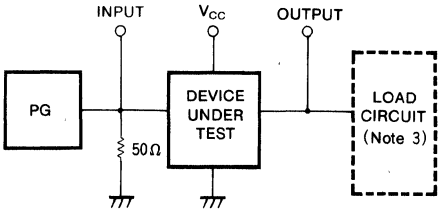
SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Alternate symbol	Test conditions	M5L8286P Limits			M5L8287P Limits			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Low-level to high-level and high-level and low-level transition time from input A B to outputs B, A	TIVOV	(Note 2)	5		30	5		22	ns
t_{PZH} t_{PZL}	Output enable time from $\overline{OE}$ input to A or B output	TELOV		10		30	10		30	ns
t_{PHZ} t_{PLZ}	Output disable time from $\overline{OE}$ input to A or B output	TEHOZ		5		18	5		18	ns

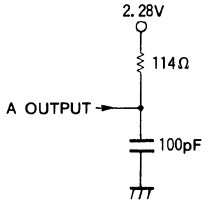
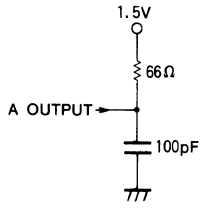
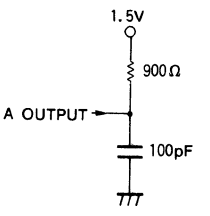
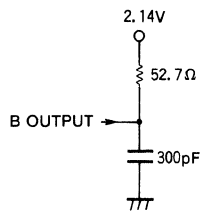
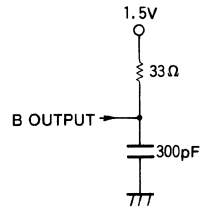
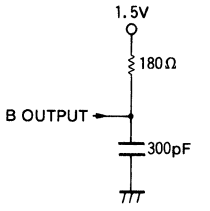
TIMING REQUIREMENTS (V_{CC}=5V±10%, T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Alternate Symbol	Test conditions	Limits Min	Typ	Max	Unit
t_{su}	T setup time with respect to $\overline{OE}$	T_{TVFL}		10			ns
t_h	T hold time with respect to $\overline{OE}$	T_{EHTV}		5			ns

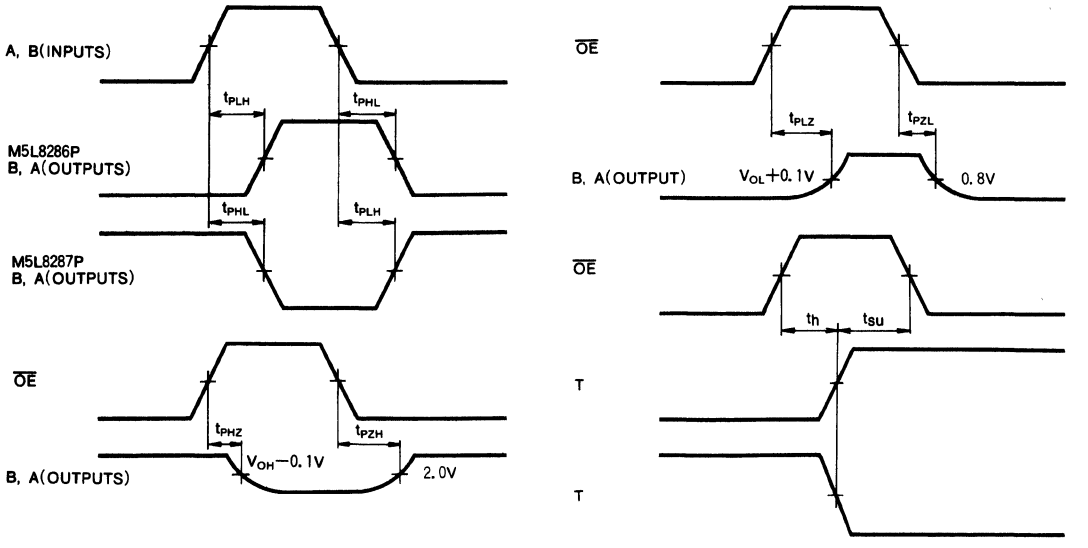
Note 2 : Test Circuit



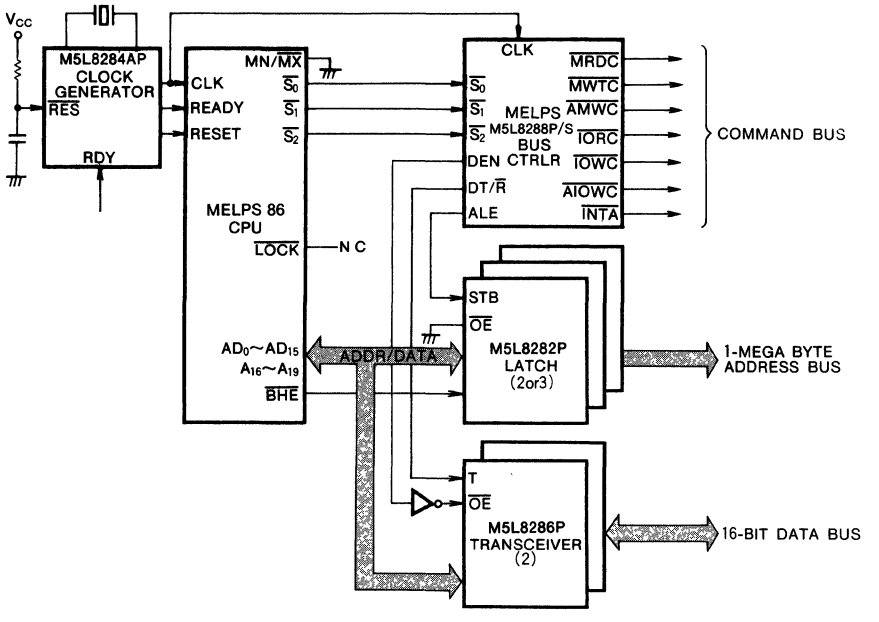
Note 3

Test Item	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
A OUTPUT LOAD CIRCUIT			
B OUTPUT LOAD CIRCUIT			

TIMING DIAGRAM (Reference voltage=1.5V)



APPLICATION EXAMPLE



M5L8288P

BUS CONTROLLER

DESCRIPTION

The M5L8288P is a semiconductor integrated circuit consisting of a bus controller and bus driver for the MELPS 86, 88, 16-bit microprocessors. By using the status signals from the CPU a Multibus (Intel trademark) control signal is generated.

FEATURES

- High-fanout outputs
  Command output I_{OL}=32mA, I_{OH}=−5mA
  Control output I_{OL}=16mA, I_{OH}=−1mA
- Advanced command outputs ($\overline{AIOWC}$ and $\overline{AMWC}$ outputs)
- Low power dissipation

APPLICATION

Bus controller and bus driver for maximum mode operation of the MELPS 86, 88

FUNCTION

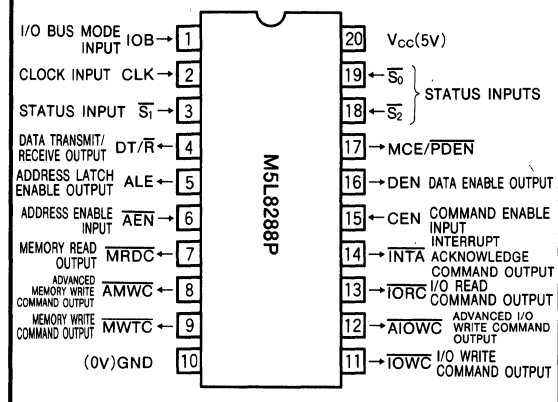
The M5L8288P is a bus controller and driver for maximum mode operation of theMELPS 86, 88 processors.

The command signals and control signals are decoded by means of the $\overline{S_0}$~$\overline{S_2}$ outputs from the CPU and the control signals for I/O devices and memory are output.

The device can be used in the Multimaster mode in which several CPUs acting as masters are connected to one data bus. An input pin for the control signal $\overline{AEN}$ from an 8289 bus arbiter is provided.

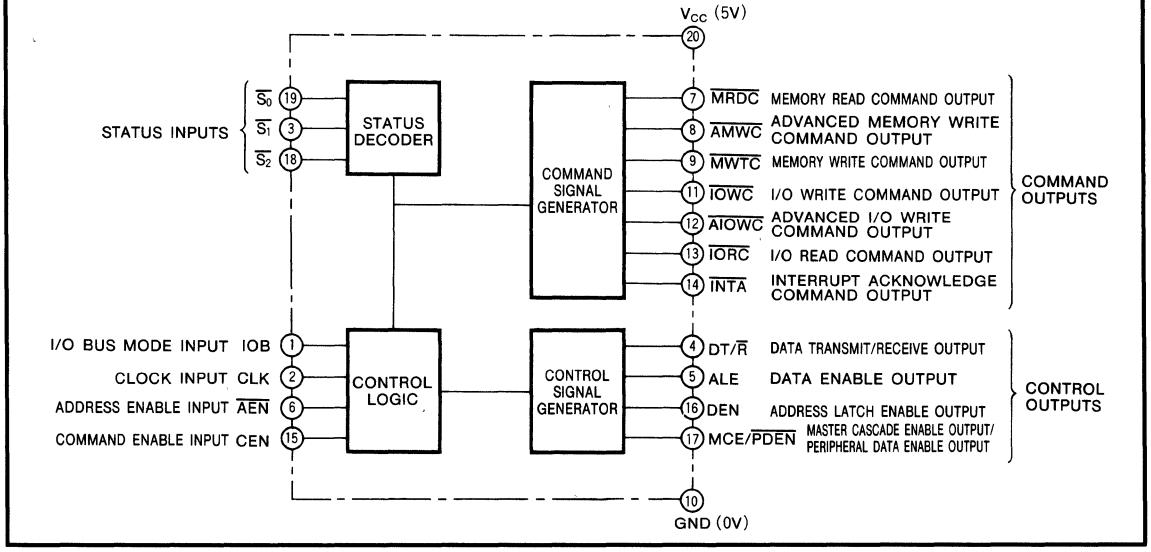
By using the M5L8288P as a bus controller, a highperformance 16-bit microcomputer system can be configured.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DESCRIPTIONS

Pin	Name	Input of output	Functions
$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	Status input	Input	These are connected to the CPU status output $\overline{S_0}$~$\overline{S_2}$ The M5L8288P uses these signals to generate the proper timing command signals and control signals All pins are provided with internal pull-up resistors.
CLK	Clock input	Input	Used to connect the clock generator M5L8284AP clock output CLK All outputs of the M5L8288S change in synchronization with the clock input.
ALE	Address latch enable output	Output	Provides the strobe signal output for the address latches. This pin is connected to the STB pin of the M5L8282P or M5L8283P and used to latch the address from the CPU When using any other address latch, the following conditions must be satisfied 1. The enable input must be active high. 2. Data reading is always performed while the enable input is high 3. The latching operation is performed as the enable input goes from high to low
DEN	Data enable	Output	Provides the data enable signal for the local bus or a data transceiver on the system bus. Operates in active high mode
DT/$\overline{R}$	Data transmit/receive control output	Output	Controls the flow of data between CPU and memory or peripheral I/O devices When this pin is high, the CPU can write data to the peripheral devices When it is low, it can read data from the peripheral devices It is connected to the transmit input T of the M5L8286P or M5L8287P bus transceivers
$\overline{AEN}$	Address enable input	Input	When the IOB input is low and the $\overline{AEN}$ input is set to high, all command outputs are put in the high-impedance state. When the IOB input is high, there is no effect on the $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, and $\overline{INTA}$ outputs, the command output other than these four going into the high-impedance state None of the command outputs will go low until at least 115ns after $\overline{AEN}$ transits from high to low.
CEN	Command enable input	Input	When this pin is set to low, all command outputs and DEN are prohibited by the $\overline{PDEN}$ control output (not high-impedance state) When set to high, the above outputs are enabled
IOB	Input/output bus mode input	Input	When this pin is set to high, the M5L8288P functions in the I/O bus mode, and when set to low it functions in the system bus mode. (The I/O bus mode and system bus mode are described in the functional description)
$\overline{AIOWC}$	Advanced I/O write command output	Output	The $\overline{AIOWC}$ issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction its timing is the same as a read command signal Active low
$\overline{IOWC}$	I/O write command output	Output	Instructs an I/O device to read the data on the data bus Active low.
$\overline{IORC}$	I/O read command output	Output	Instructs an I/O device to drive its data onto the data bus Active low
$\overline{AMWC}$	Advanced write command output	Output	The $\overline{AMWC}$ issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction Its timing is the same as a read command signal Active low
$\overline{MWTC}$	Memory write command output	Output	Provides a write instruction to memory for the current data on the bus Active low
$\overline{MRDC}$	Memory read command output	Output	Provides an output instruction to memory for the present data on the bus Active low
$\overline{INTA}$	Interrupt acknowledge command output	Output	This output informs an interrupting device that it has accepted the interrupt, outputting a vector address output instruction to the data bus $\overline{IORC}$ operates in the same manner for interrupt cycles Active low
MCE/ $\overline{PDEN}$	Master cascade Enable output/ Peripheral data Enable output	Output	This output pin has two functions 1. When the IOB input is set to low The MCE function is enabled The signal acts as the enable signal which allows a slave PIC (M5L8259AP) to read the cascade address output to the bus by the master PIC during an interrupt sequence Active high 2. When the IOB input is set to high The $\overline{PDEN}$ function is enabled This output provides the enable signal to the data bus transceiver connected to the I/O interface bus when an instruction occurs ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) Operates the same way as DEN with respect to the system bus

FUNCTIONAL DESCRIPTION

The state of the command outputs and control outputs are determined by the CPU status outputs $\overline{S_0} \sim \overline{S_2}$. The table summarizes the states of the outputs $\overline{S_0} \sim \overline{S_2}$ and their corresponding valid command output names.

Depending upon whether the M5L8288S is in the I/O bus mode or system bus mode, the command output sequence will vary.

STATUS INPUTS AND COMMAND OUTPUTS RELATIONSHIPS

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	8086, 8088 status	Valid command output name
L	L	L	Interrupt acknowledge	$\overline{INTA}$
L	L	H	Data read from an I/O port	$\overline{IORC}$
L	H	L	Data write to an I/O port	$\overline{IOWC}$, $\overline{AIOWC}$
L	H	H	Halt	—
H	L	L	Instruction fetch	$\overline{MRDC}$
H	L	H	Read data from memory	$\overline{MRDC}$
H	H	L	Write data to memory	$\overline{MWTC}$, $\overline{AMWC}$
H	H	H	Passive state	—

1. I/O bus mode operation

When IOB is high, the M5L8288S function in the I/O bus mode.

In the I/O Bus mode all I/O command lines ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (i.e., not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the 8288 immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one 8288 Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a "Bus Ready" signal ($\overline{AEN}$ LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.

2. System bus mode operation

When IOB is set to low, the M5L8288S enters the system bus mode. In this mode no command is issued until 115 ns after the $\overline{AEN}$ Line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the $\overline{AEN}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

3. $\overline{AMWC}$ and $\overline{AIOWC}$ outputs

With respect to the normal write control signals $\overline{MWTC}$ and $\overline{IOWC}$, the advanced-write command signals $\overline{AMWC}$ and $\overline{AIOWC}$ transit low one clock cycle earlier and remain low for two clock cycles.

These signals are used with peripheral devices or static RAM devices which require a long write pulse, so that the CPU does not go into an unnecessarily wait cycle.

ABSOLUTE MAXIMUM RATINGS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7	V
V_I	Input voltage		−0.5~+5.5	V
V_O	Output voltage		−0.5~V_{CC}	V
P_d	Power dissipation		1.5	W
T_{opr}	Operating free-air temperature range		0~75	℃
T_{stg}	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
I_{OH}	High-level output current	Command outputs			−5	mA
		Control outputs			−1	
I_{OL}	Low-level output current	Command outputs			32	mA
		Control outputs			16	

ELECTRICAL CHARACTERISTICS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage						−1	V
V_{OH}	High-level output voltage	Command outputs	V_{CC}=4.5V, V_I=2V	I_{OH}=−5mA	2.4			V
		Control outputs	V_I=0.8V	I_{OH}=−1mA	2.4			
V_{OL}	Low-level output voltage	Command outputs	V_{CC}=4.5V, V_I=2V	I_{OL}=32mA			0.5	V
		Control outputs	V_I=0.8V	I_{OL}=16mA			0.5	
I_{IH}	High-level input voltage		V_{CC}=5.5V, V_I=5.5V				50	μA
I_{IL}	Low-level input voltage		V_{CC}=5.5V, V_I=0.45V				−0.7	mA
I_{OZH}	Off-state output current with high-level applied to output		V_{CC}=5.5V, V_O=5.25V				100	μA
I_{OZL}	Off-state output current with low-level applied to output		V_{CC}=5.5V, V_O=0.4V				−100	μA
I_{CC}	Supply current		V_{CC}=5.5V				160	mA

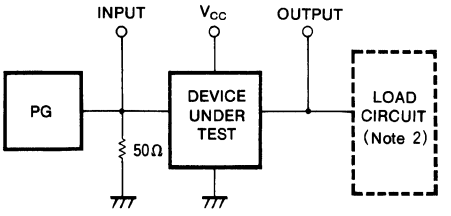
SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Alternate symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Output low-level to high-level propagation time From CLK input to DEN output	TCVNV		5		45	ns
t_{PHL}	Output high-level to low-level propagation time From CLK input to $\overline{PDEN}$ output						
t_{PLH}	Output low-level to high-level propagation time From CLK input to DEN output	TCVNX		10		45	ns
t_{PHL}	Output high-level to low-level propagation time From CLK input to $\overline{PDEN}$ output						
t_{PLH}	Output low-level to high-level propagation time From CLK input to ALE output	TCLLH				20	ns
t_{PLH}	Output low-level to high-level propagaion time From CLK input to MCE output	TCLMCH				20	ns
t_{PLH}	Output low-level to high-level propagation time From $\overline{S_0}$~$\overline{S_1}$ inputs to ALE output	TSVLH				20	ns
t_{PLH}	Output low-level to high-level propagation time From $\overline{S_0}$~$\overline{S_1}$ inputs to MCE output	TSVMCH				20	ns
t_{PHL}	Output high-level to low-level propagation time From CLK input to ALE output	TCHLL		4		15	ns
t_{PHL}	Output high-level to low-level propagation time From CLK input to $\overline{MRDC}$, $\overline{IORC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{MWTC}$, $\overline{AIOWC}$, and $\overline{IOWC}$ outputs	TCLML		10		35	ns
t_{PLH}	Output low-level to high-level propagation time From CLK input to $\overline{MRDC}$, $\overline{IORC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{MWTC}$, $\overline{AIOWC}$, and $\overline{IOWC}$ outputs	TCLMH		10		35	ns
t_{PHL}	Output high-level to low-level propagation time From CLK input to DT/$\overline{R}$ output	TCHDTL	(Note 1)			50	ns
t_{PLH}	Output low-level to high-level propagation time From CLK input to DT/$\overline{R}$ output	TCHDTH				30	ns
t_{PZH}	High-level output enable time From $\overline{AEN}$ input to $\overline{MRDC}$, $\overline{IORC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{MWTC}$, $\overline{AIOWC}$, and $\overline{IOWC}$ outputs	TAELCH				40	ns
t_{PHZ}	High-level output disable time From $\overline{AEN}$ input to $\overline{MRDC}$, $\overline{IORC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{MWTC}$, $\overline{AIOWC}$, and $\overline{IOWC}$ outputs	TAEHCZ				40	ns
t_{PHL}	Output high-level to low-level propagation time From $\overline{AEN}$ input to $\overline{MRDC}$, $\overline{IORC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{MWTC}$, $\overline{AIOWC}$, and $\overline{IOWC}$ outputs	TAELCV		115		200	ns
t_{PLH} t_{PHL}	Output low-level to high-level and high-level to low-level propagation time From $\overline{AEN}$ input to DEN output	TAEVNV				20	ns
t_{PLH} t_{PHL}	Output low-level to high-level and high-level to low-level propagation time From CEN input to $\overline{DEN}$ and PDEN outputs	TCEVNV				25	ns
t_{PLH} t_{PHL}	Output low-level to high-level and high-level to low-level propagation time. From CEN input to $\overline{MRDC}$, $\overline{IORC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{MWTC}$, $\overline{AIOWC}$ and $\overline{IOWC}$ outputs	TCELRH				35	ns

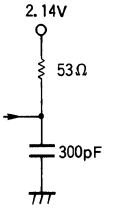
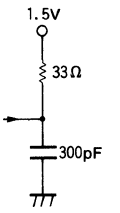
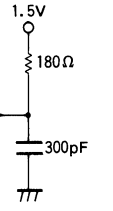
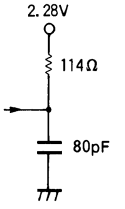
TIMING REQUIREMENTS (V_{CC}=5V±10%, T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Alternate symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
t_C	Clock CLK cycle time	TCLCL		100			ns
$t_{W(CLKL)}$	Clock CLK low pulse width	TCLCH		50			ns
$t_{W(CLKH)}$	Clock CLK high pulse width	TCHCL		30			ns
$t_{su(\overline{S_0}\sim\overline{S_2})}$	$\overline{S_0}$~$\overline{S_2}$ setup time with respect to T for the T_1 state	TSVCH		35			ns
$t_{h(\overline{S_0}\sim\overline{S_2})}$	$\overline{S_0}$~$\overline{S_2}$ hold time with respect to T for the T_4 state	TCHSV		10			ns
$t_{su(\overline{S_0}\sim\overline{S_2})}$	$\overline{S_0}$~$\overline{S_2}$ setup time with respect to T for the T_3 state	TSHCL		35			ns
$t_{h(\overline{S_0}\sim\overline{S_2})}$	$\overline{S_0}$~$\overline{S_2}$ hold time with respect to T for the T_3 state	TCLSH		10			ns

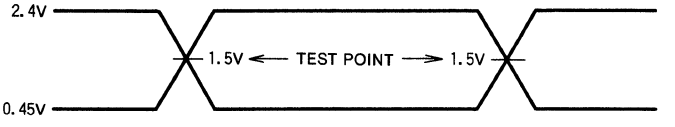
Note 1 : Test Circuit



Note 2

Load circuit	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
Command output load circuit			
Control output load circuit		—	—

Note 3 : AC TEST WAVE FORM

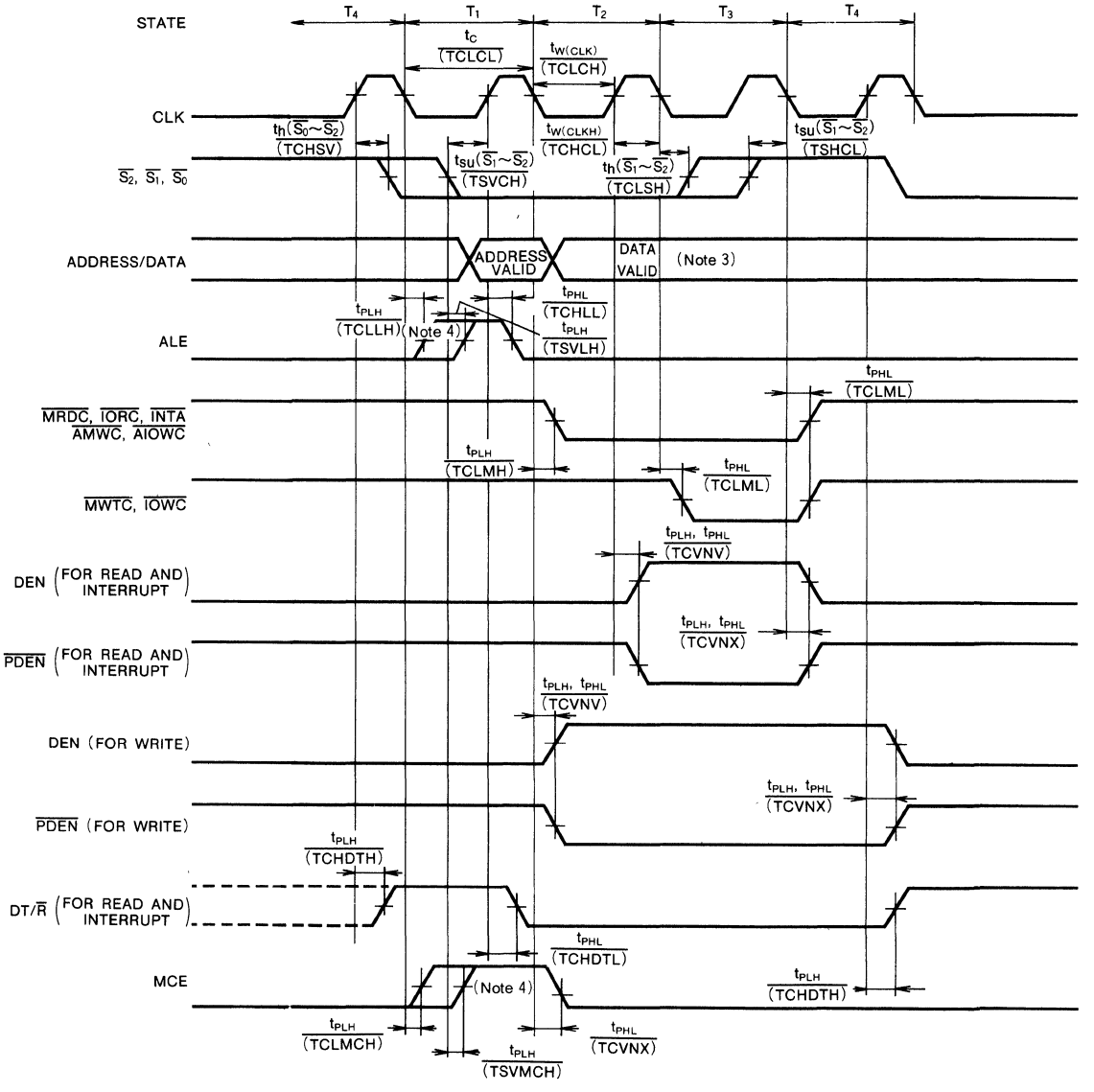


INPUT PULSE LEVEL : 0.45~2.4V

TIMING MEASUREMENT POINT : 1.5V

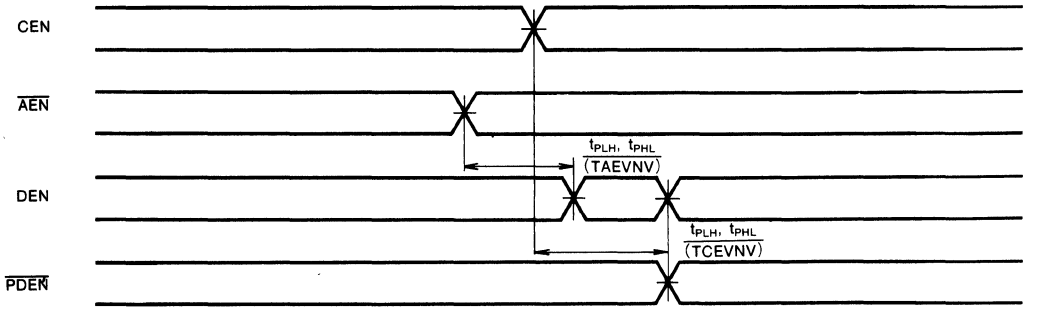
TIMING DIAGRAM

1. Command output timing

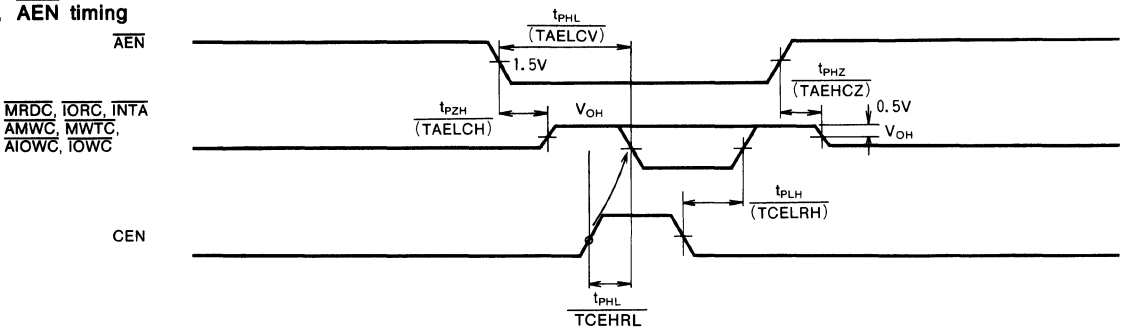


Note 3 : The address/data bus signals are shown only for reference
4 : The ALE and MCE leading edge occurs in synchronization with the falling edge of CLK or $\overline{S_0}$~$\overline{S_2}$, whichever is later
5 : Unless otherwise noted, the timing of all signals is respect to 1.5V

2. DEN and $\overline{PDEN}$ timing

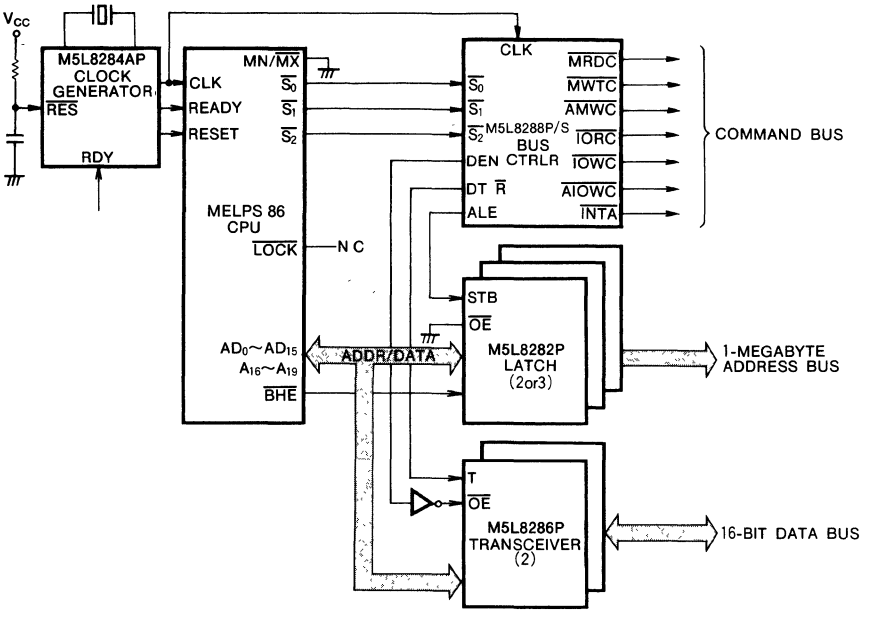


3. $\overline{AEN}$ timing



Note 6 : CEN must be low or valid prior to T_2 to prevent the command from being generated.

APPLICATION EXAMPLE



M5L8289P

BUS ARBITER

DESCRIPTION

The M5L8289P is a system bus (®MULTIBUS) arbiter for the MELPS 86, 88 16-bit microprocessors. When a request for access to the system bus is made by any of these microprocessors, the M5L8289P prevents simultaneous access by two or more processors by allowing only the first processor which requests access to access the system, preventing all others from accessing the system bus. It generates the required signals for bus access. (®MULTIBUS is a registered trademark of Intel Corporation.)

FEATURES

- ®MULTIBUS compatible
- Usable in multiprocessing systems using the MELPS 86, 88 microprocessors
- Four modes of request and bus surrender are possible
- Low power dissipation

APPLICATION

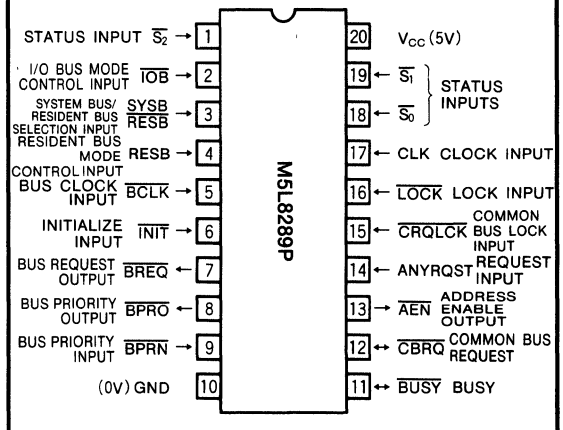
Bus arbitration for MULTIBUS boards using the MELPS 86, 88 or 8089

FUNCTION

The M5L8289P is a bus arbiter for ®MULTIBUS boards using the MELPS 86, 88 microprocessors. When several processors are connected to the system bus (®MULTIBUS), it is necessary to prevent two or more processors from attempting to access the system bus simultaneously.

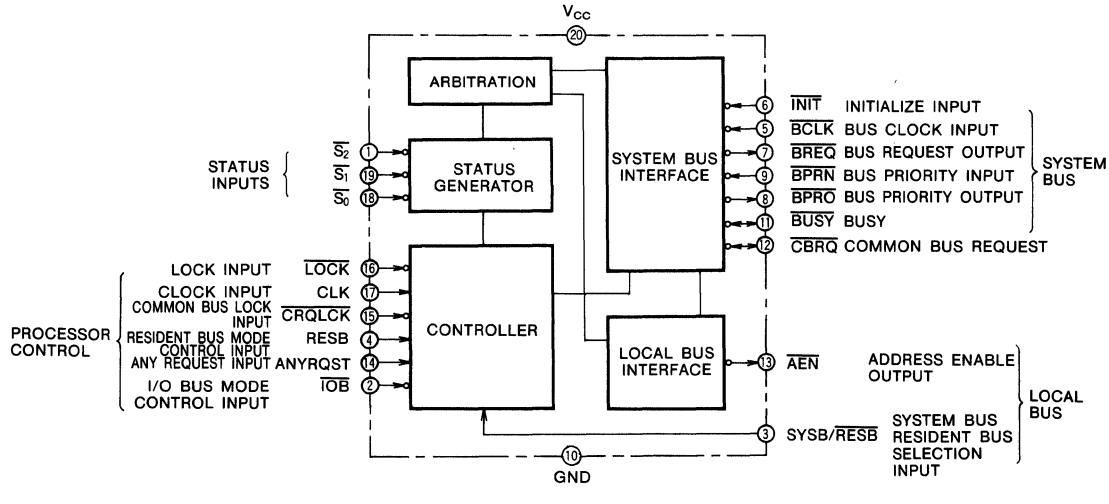
This function is performed by the M5L8289P, which decodes the processor status, and if access to the system bus is required, prevents other processors from attempting system bus access by generating the required control signals.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONAL DESCRIPTION

The M5L8289P decodes the status signals $\overline{S_0} \sim \overline{S_2}$ from the processor, and requests system bus privileges or surrenders them. The conditions for such operation are shown in Table 1. As shown in the Table 1, the following four modes are possible for use with boards of various types.

(1) Single Bus Mode

In this mode there is neither memory nor I/O ports on the board, and the processor accesses only the system bus.

(2) I/O Bus Mode

In this mode I/O ports exist on the board, and the processor accesses only these. For this mode the M5L8289P outputs a system bus request signal only for memory access.

(3) Resident Bus Mode

In this mode both memory and/or I/O port(s) exist on the board and the processor can access both on the system bus. In this mode the chip select signal (active low) for I/O ports and memory on the system bus is input to SYSB/$\overline{\text{RESB}}$. By doing this, when the I/O port(s) and memory on the board are accessed, the M5L8289P does not output a request signal to the system bus.

(4) I/O Bus Mode Resident Bus Mode

In this mode both I/O ports and memory are existent on the board, and only the I/O port on the board is accessed.

In this mode the chip select signal (active low) for memory on the board is input to SYSB/$\overline{\text{RESB}}$. By doing this, the M5L8289P outputs a request signal to the system bus when system memory is accessed.

In addition, the M5L8289P has the following control inputs.

- $\overline{\text{LOCK}}$
  This signal locks the bus arbitrate function when it is low, the M5L8289P continues to output a request signal to the system bus, and once acquired, setting $\overline{\text{LOCK}}$ to a high level retains bus privileges until the conditions listed in Table 1 are satisfied. Normally, this input is connected to th $\overline{\text{LOCK}}$ output of the processor.
- $\overline{\text{CRQLCK}}$
  This signal locks the arbitrate function by CBRQ. When set to low, the bus privilege surrender conditions listed in Table 1 in which CBRQ are input, are ignored. This input is set to low level when it is desired to prevent low-priority arbiters from acquiring bus privileges.
- ANYRQST
  Even after one bus access has been completed, the M5L8289P does not surrender bus privileges until the surrender conditions listed in Table 1 are satisfied. However, by setting the ANYRQST input to high, the bus can be freed after each single access, thereby facilitating the acquisition of bus privileges by low-priority arbiters.

Table 1 M5M8289P Modes and Bus Request and surrender Conditions

Status				I/O Bus mode only	Resident bus mode only		I/O Bus mode resident bus mode		Single bus mode
				$\overline{IOB}$=L RESB=L	$\overline{IOB}$=H RESB=H		$\overline{IOB}$=L RESB=H		$\overline{IOB}$=H RESB=L
Command	$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$		SYSB/$\overline{RESB}$=H	SYSB/$\overline{RESB}$=H	SYSB/$\overline{RESB}$=H	SYSB/$\overline{RESB}$=L	
Interrupt acknowledge	0	0	0	×	○	×	×	×	○
I/O Port read	0	0	1	×	○	×	×	×	○
I/O Write	0	1	0	×	○	×	×	×	○
Halt	0	1	1	×	×	×	×	×	×
Instruction fetch	1	0	0	○	○	×	○	×	○
Memory read	1	0	1	○	○	×	○	×	○
Memory write	1	1	0	○	○	×	○	×	○
Passive cycle	1	1	1	×	×	×	×	×	×

○ ····· A request signal is output by the system bus.
× ····· The system bus privileges are surrendered

Mode	Input		Bus request condition (excluding halt and passive cycles)	Bus surrender condition (Note 1)
	$\overline{IOB}$	RESB		
Single bus mode	H	L	All bus access states	HLT+(TI-CBRQ)+HPBRQ
Resident bus mode only	H	H	(SYSB/$\overline{RESB}$=high)·(Bus access state)	((SYSB/$\overline{RESB}$=L+T1)·CBRQ) +HLT+HPBRQ
I/O Bus mode only	L	L	All memory access states	(I/O Access state+T1)·CBRQ)+HLT +HPERQ
I/O Bus mode resident bus mode	L	H	(SYSB/$\overline{RESB}$=high)·(Memory access states)	((I/O Access state +(SYSB/$\overline{RESB}$=low))· CBRQ + HPBRQ HLT +HPBRQ

Note 1 : When $\overline{LOCK}$=low, the bus is not released under any circumstances.
When $\overline{CRQLCK}$=low, the bus is not released even when low-priority arbiters request it
2 : HLT·····Halt state
TI·····Idle (passive) state
CBRQ·····$\overline{CBRQ}$=low
HPBRQ ·····Indicates that a high-priority arbiter is requesting the bus ($\overline{BPRN}$=high)

PIN DESCRIPTION

Pin	Name	Input or output	Function
$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	Status input	In	Status input from the processor. The M5L8289P decodes this signal and based on it, requests or surrenders bus privileges.
CLK	Clock input	In	This is the same clock input as used on the processor, and used for decoding of the status It receives the clock from the M5L8284AP
$\overline{LOCK}$	Lock input	In	This is the lock input signal from the processor When $\overline{LOCK}$=low, the M5L8289P will, in no circumstances, surrender bus privileges.
$\overline{CRQLCK}$	Common bus request lock input	In	This is the lock signal for arbitration from a common bus request When $\overline{CRQLCK}$=low, the M5L8289P ignores bus surrendering conditions by signal CBRQ
RESB	Resident bus mode control input	In	This is the M5L8289P mode setting input When RESB=high, the M5L8289P is in the resident bus mode
$\overline{IOB}$	I/O Bus mode control input	In	This is an M5L8289P mode setting input. When $\overline{IOB}$=low, the M5L8289P is in the I/O bus mode.
ANYRQST	Any request input	In	This controls the bus surrendering conditions for the M5L8289P When ANYRQST=low, the M5L8289P releases the bus under the conditions listed in Table 1 When ANYRQST=high, as soon as $\overline{CBRQ}$ goes low, the bus is released. Therefore, by setting ANYRQST to high and $\overline{CBRQ}$ to low, the M5L8289P can be made to release the bus after a single access
SYSB/$\overline{RESB}$	System bus/resident bus selection input	In	This input is valid when the M5L8289P is in the resident bus mode. When SYSB/$\overline{RESB}$=low, this means that the processor is accessing the bus on the board, and the M5L8289P does not output a request to the system bus. When SYSB/$\overline{RESB}$=high, this indicates that the processor is accessing the system bus, and the M5L8289P outputs the request signal to the system bus
$\overline{BCLK}$	Bus lock input	In	This is the clock for arbitration of other boards. The M5L8289P performs arbitration in synchronous with this clock. It is fed from the system bus $\overline{BCLK}$ signal.
$\overline{INIT}$	Initialize input	In	This line resets the arbitration circuit. Immediately after resetting, none of the arbiters have system bus privileges. This input is fed from the system bus $\overline{INIT}$ signal
$\overline{BREQ}$	Bus request output	Out	This signal requests system bus privileges It is used as the system bus $\overline{BREQ}$ signal
$\overline{BPRN}$	Bus priority input	In	This signal indicates whether a high-priority arbiter has requested privileges or not When $\overline{BPRN}$=low, a high-priority arbiter has not requested privileges and when $\overline{BPRN}$=high, this indicates that a high-priority arbiter has requested privileges This input is fed from the system bus $\overline{BPRN}$ signal.
$\overline{BPRO}$	Bus priority output	Out	This signal indicates whether the M5L8289P or high-order arbiter has requested the bus When $\overline{BPRO}$=low, there was a bus request and when $\overline{BPRO}$=high, there was no bus request This signal is used as the system bus $\overline{BPRO}$ signal
$\overline{BUSY}$	Busy	In/Out	This signal indicates that the system bus has been acquired When $\overline{BUSY}$=low, the bus is busy and when $\overline{BUSY}$=high, it indicates that no arbiter has acquired the bus privileges. When the M5L8289P has acquired bus privileges, a low-level output (open collector) is made This signal is used as the system bus $\overline{BUSY}$ signal.
$\overline{CBRQ}$	Common bus request	In/Out	This signal indicates when any arbiter has requested the system bus. When $\overline{CBRQ}$=low, the M5L8289P releases the bus according to the conditions listed in Table1. When making a request of the system bus, $\overline{CBRQ}$ is output as low (open collector) This signal is used as the system bus $\overline{CBRQ}$ signal.
$\overline{AEN}$	Address enable input	Out	This signal informs the bus buffer on the board that the system bus has been acquired It is connected to the address and data buffer outputs, and the output enable line on the board as well as the M5L8288P $\overline{AEN}$ line

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～7	V
V_I	Input voltage		−1～5.5	V
V_O	Output voltage		−0.5～7	V
T_{opr}	Operating temperature		0～75	℃
T_{stg}	Storage temperature		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0～75℃, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min	Nom	Max	
V_{CC}	Supply voltage			4.5	5	5.5	V
I_{OH}	High-level output current	$\overline{BUSY}$, $\overline{CBRQ}$,	V_{OH}≧2.4V	Open collector			μA
		Other output,	V_{OH}≧2.4V	0		400	
I_{OL}	Low-level output current	$\overline{BUSY}$, $\overline{CBRQ}$,	V_{OL}≦0.45V	0		20	mA
		$\overline{AEN}$	V_{OL}≦0.45V	0		16	
		$\overline{BPRO}$, $\overline{BREQ}$,	V_{OL}≦0.45V	0		10	

ELECTRICAL CHARACTERISTICS (T_a=0～75℃, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{OL}	Low-level output voltage	$\overline{BUSY}$, $\overline{CBRQ}$	I_{OL}=20mA			0.45	V
		$\overline{AEN}$	I_{OL}=16mA			0.45	
		$\overline{BPRO}$, $\overline{BREQ}$	I_{OL}=10mA			0.45	
V_{OH}	High-level output voltage	$\overline{BUSY}$, $\overline{CBRQ}$		Open collector			V
		$\overline{AEN}$, $\overline{BPRO}$, $\overline{BREQ}$	I_{OH}=400μA	2.4			
V_{IC}	Input clamp voltage		V_{CC}=4.50V, I_C=−5mA			−1	V
I_{IL}	Low-level input current		V_{CC}=5.50V, V_F=0.45V			−0.5	mA
I_{IH}	High-level input current		V_{CC}=5.50V, V_R=5.50V			60	μA
I_{CC}	Supply current					120	mA
C_{IN}	Input capcitance	Status	f=1MHz, V_{B2AS}=2.5V			25	pF
		Others				12	

TIMING REQUIREMENT (T_a=0~75℃, V_{CC}=5V±10%, unless otherwise noted)

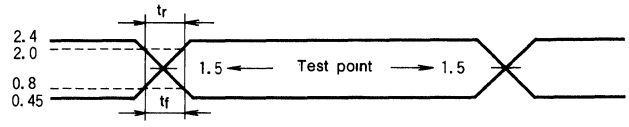
Symbol	Parameter	Alternate symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{C(CLK)}$	CLK cycle period	t_{CLCL}		125			ns
$t_{W(CLKL)}$	CLK"L" pulse width	t_{CLCH}		65			ns
$t_{W(CLKH)}$	CLK"H" pulse width	t_{CHCL}		35			ns
$t_{su(\overline{S0}\sim\overline{S2})}$	Status active setup time	t_{SVCH}		65		t_{CLCL}-10	ns
$t_{h(\overline{S0}\sim\overline{S2})}$	Status active hold time	t_{CHSV}		10		t_{CLCL}-10	ns
$t_{su(\overline{S0}\sim\overline{S2})}$	Status inactive setup time	t_{SHCL}		50			ns
$t_{h(\overline{S0}\sim\overline{S2})}$	Status inactive hold time	t_{CLSH}		10			ns
$t_{h(\overline{LOCK})}$	$\overline{LOCK}$ inactive hold time	t_{CLLL1}		10			ns
$t_{su(LOCK)}$	LOCK active setup time	t_{CLLL2}		40			ns
$t_{su(SYSB/\overline{RESB})}$	SYSB/$\overline{RESB}$ setup time	t_{CLSR1}		0			ns
$t_{h(SYSB/\overline{RESB})}$	SYSB/$\overline{RESB}$ hold time	t_{CLSR2}		20			ns
$t_{C(\overline{BCLK})}$	$\overline{BCLK}$ cycle time	t_{BLBL}		100			ns
$t_{W(\overline{BCLKH})}$	$\overline{BCLK}$"H" pulse width	t_{BHBL}		30			ns
$t_{su(\overline{BPRU})}$	$\overline{BPRN}$ ↑ ↓ to $\overline{BCLK}$ setup time	t_{PNSBL}		15			ns
$t_{su(\overline{BUSY})}$	$\overline{BUSY}$ ↑ ↓ to $\overline{BCLK}$ ↓ setup time	t_{BYSBL}		20			ns
$t_{su(\overline{CBRQ})}$	$\overline{CBRQ}$ ↑ ↓ to $\overline{BCLK}$ ↓ setup time	t_{CBSBL}		20			ns
$t_{W(INIT)}$	INIT pulse width	t_{IVIH}		$3t_{BLBL}+3t_{CLCL}$			ns
t_r	Input rise time	t_{ILIH}	0.8~2V			20	ns
t_f	Input fall time	t_{IHIL}	2~0.8V			12	ns

SWITCHING CHARACTERISTICS (T_a=0~75℃, V_{CC}±5V±5%, unless otherwise noted)

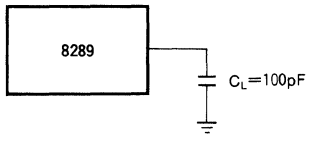
Symbol	Parameter	Alternate symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{PHL(\overline{BREQ})}$	$\overline{BCLK}$→$\overline{BREQ}$ ↑, ↓ Delay time	t_{BLBRL}				35	ns
$t_{PLH(\overline{BPRO})}$	$\overline{BCLK}$→$\overline{BPRO}$ ↑, ↓ Delay time (See note 2)	t_{BLPOH}				40	ns
$t_{PHL(\overline{BPRO})}$	$\overline{BPRN}$ ↑, ↓→$\overline{BPRO}$ ↑ ↓ Delay time (See note 2)	t_{PNPO}				25	ns
$t_{PHL(\overline{BUSY})}$	$\overline{BCLK}$→$\overline{BUSY}$ ↓ Delay time	t_{BLBYL}				60	ns
$t_{PLZ(\overline{BUSY})}$	$\overline{BCLK}$→$\overline{BUSY}$ Float time (See note 3)	t_{BLBYH}				35	ns
$t_{PLH(\overline{AEN})}$	CLK→$\overline{AEN}$, ↑ Delay time	t_{CLAEH}				65	ns
$t_{PHL(\overline{AEN})}$	$\overline{BCLK}$→$\overline{AEN}$, ↓ Delay time	t_{BLAEL}				40	ns
$t_{PHL(\overline{CBRQ})}$	$\overline{BCLK}$→$\overline{CBRQ}$, ↓ Delay time	t_{BLCBL}				60	ns
$t_{PLZ(\overline{CBRQ})}$	$\overline{BCLK}$→$\overline{CBRQ}$ Delay time (See note 3)	t_{BLCBH}				35	ns
t_r	Output rise time	t_{OLOH}	0.8V~2.0V			20	ns
t_f	Output fall time (See note 4, 5)	t_{OHOL}	2.0V~0.8V			12	ns

Note 1 : Symbol ↑, ↓ means rise signal and fall signal.
2 : $\overline{BCLK}$ generate the first $\overline{BPRO}$ and then BPRO changes lower in the chain are generated through BPRN.
3 : Measured at 0.5V above GND

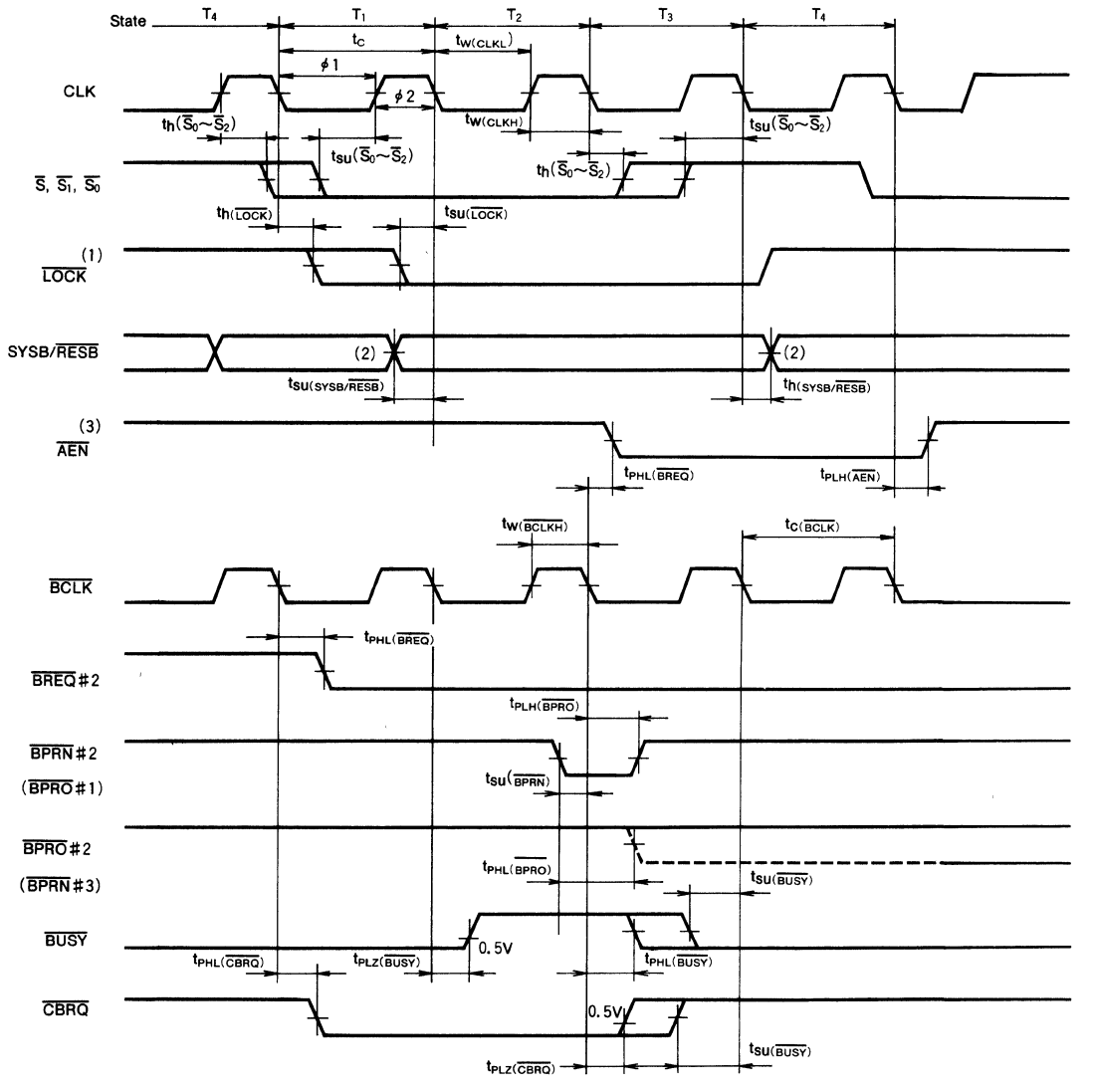
Note 4 A.C. test wave form.



Note 5 : Load circuit



TIMING DIAGRAM



Note 1 : LOCK can be active during any state as long as the relation ships shown above with the respect to CLK are maintained.
LOCK can be inactive asynchronously
CRQLCK is an asynchronous input signal.
2 : Noise is permitted during this time After φ2 of T1 and before φ1 of T4 should be stable
3 : AEN negative-edge is related to CLK, positive-edge to CLK.
ANE positive-edge is generated after as ricrity is lost

CMOS PERIPHERAL CIRCUITS

4

M5M81C55P-2/FP-2/J-2

CMOS 2048-BIT STATIC RAM WITH I/O PORTS AND TIMER

DESCRIPTION

The M5M81C55P-2 is the 2K-bit RAM (256-word by 8-bit) fabricated by the silicon gate CMOS technology. This LSI has 3 I/O ports and a 14-bit counter/timer which make it a good extension of the functions of an 8-bit microcomputer. It is housed in a 40-pin plastic molded DIP.

And preparatory for surface equipment M5M81C55FP-2 (SOP)and M5M81C55J-2 (PLCC).

FEATURES

- Having internal anti-circuit on RESET and ALE
- Single 5V supply voltage
- TTL compatible
- Power down mode
- Timer input : 5MHz (max)
- Read access time : 120ns (max)
- Static RAM: 256-word by 8-bit
- Programmable 8-bit I/O port: 2
- Programmable 6-bit I/O port: 1
- Programmable counter/timer: 14-bit
- Multiplexed address/data bus

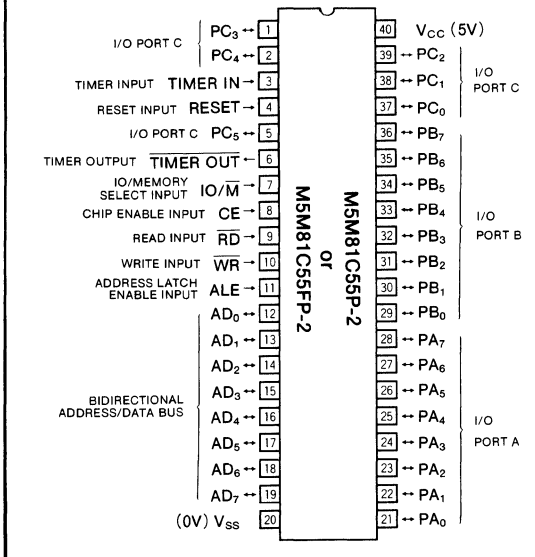
APPLICATION

Extension of I/O ports and timer function for microprocesser

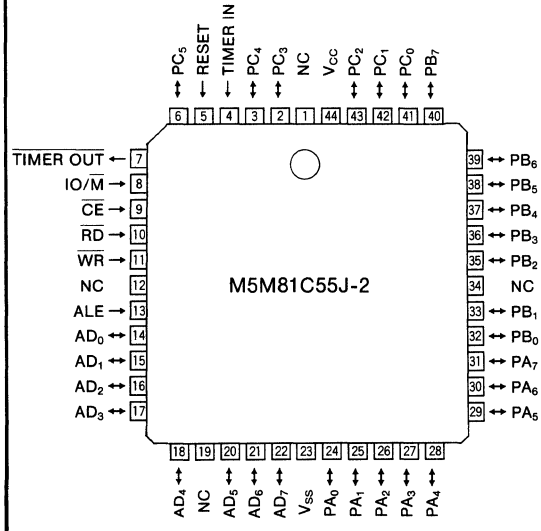
FUNCTION

The M5M81C55P-2 is composed of RAM, I/O ports and counter/timer. The RAM is a 2K-bit static RAM organized as 256-word by 8-bit. The I/O ports consist of 2 programmable 8-bit ports and 1 programmable 6-bit port. The terminals of the 6-bit port can be programmed as control terminals for the 8-bit ports, so that the 8-bit ports can be operated in a handshake mode. The counter/timer is composed of 14-bit down counter (events or time) and it can generate square wave pulses that can be used for counting and timing.

PIN CONFIGURATION (TOP VIEW)



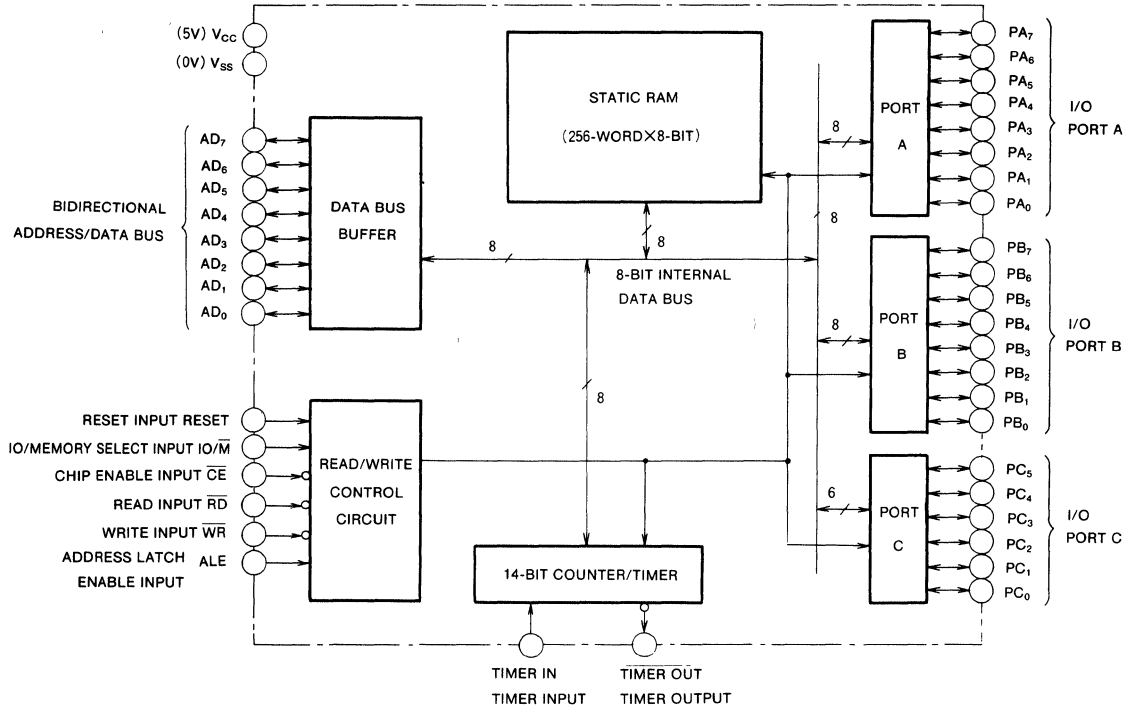
Outline 40P4 (M5M81C55P-2)
40P2R (M5M81C55FP-2)



Outline 44P0

NC : NO CONNECTION

BLOCK DIAGRAM



OPERATION

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to transfer the data while input or output instructions are being executed by the CPU. Command and address information is also transferred through the data bus buffer.

Read/Write Control Logic

The read/write control logic controls the transfer of data and commands by interpreting the signals ($\overline{CE}$, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, ALE, RESET) from CPU.

Bidirectional Address/Data Bus (AD_0~AD_7)

The bidirectional address/data bus is a 3-state 8-bit bus. The 8-bit address is latched in the internal latch by the falling edge of ALE. Then if IO/$\overline{M}$ input signal is at high-level, the address of I/O port, counter/timer, or command register is selected. If it is at low-level, address of RAM is selected. The 8-bit data is transferred by read input ($\overline{RD}$) or write input ($\overline{WR}$).

Chip Enable Input ($\overline{CE}$)

When $\overline{CE}$ is at low-level, the address information on address/data bus is stored in the M5M81C55P-2.

Read Input ($\overline{RD}$)

When $\overline{RD}$ is at low-level, the data bus buffer is active. If IO/$\overline{M}$ input signal is at low-level, the contents of RAM are read through the address/data bus. If IO/$\overline{M}$ input is at high-level, the contents of selected I/O port or counter/timer are read through the address/data bus.

Write Input ($\overline{WR}$)

When $\overline{WR}$ is at low-level, the data on the address/data bus are written into RAM if IO/$\overline{M}$ is at low-level, or they are written into I/O port, counter/timer or command register if IO/$\overline{M}$ is at high-level.

Address Latch Enable Input (ALE)

An address on the address/data bus is latched in the M5M81C55P-2 on the falling edge of ALE along with the levels of $\overline{CE}$ and IO/$\overline{M}$.

IO/Memory Input (IO/$\overline{M}$)

When IO/$\overline{M}$ is at low-level, the RAM is selected, while at high-level the I/O port, counter/timer or command register are selected.

I/O Port A (PA_0~PA_7)

Port A is an 8-bit general-purpose I/O port. Input/output setting is controlled by the system software.

I/O Port B (PB_0~PB_7)

Port B is an 8-bit general-purpose I/O port. Input/output setting is controlled by the system software.

I/O Port C (PC_0~PC_5)

Port C is a 6-bit I/O port that can also be used to output control signals of port A (PA) or port B (PB). The functions of port C are controlled by the system software. When port C is used to output control signals of ports A or B, the assignment of the signals to the pins is as shown in Table 1.

Table 1 Pin assignment of control signals of port C

Pin	Function	
PC_5	$\overline{B\ STB}$	(port B strobe)
PC_4	B BF	(port B buffer full)
PC_3	B INTR	(port B interrupt)
PC_2	$\overline{A\ STB}$	(port A strobe)
PC_1	A BF	(port A buffer full)
PC_0	A INTR	(port A interrupt)

Timer Input (TIMER IN)

The signal on this input terminal is used by the counter/timer for counting events or time. (5MHz max.)

Timer Output ($\overline{TIMER\ OUT}$)

A square wave signal or pulse from the counter/timer is output through this pin when in the operation mode.

Command Register (8-bit)

The command register is an 8-bit latched register. The low-order 4 bits (bits 0~3) are used for controlling and determination of mode of the ports. Bits 4 and 5 are used as interrupt enable flags for ports A and B when port C is used as a control port. Bits 6 and 7 are used for controlling the counter/timer. The contents of the command register are rewritten by output instructions (I/O address XXXXX000). Details of the functions of the individual bits of the command register are shown in Table 2.

Table 2 Bit functions of the command register

Bit	Symbol	Function	
0	PA	PORT A I/O SET	1. Output port A 0: Input port A
1	PB	PORT B I/O SET	1· Output port B 0. Input port B
2	PC_1	PORT C SET	00 ALT1 11. ALT2 01. ALT3 10 ALT4
3	PC_2		
4	IEA	PORT A INTERRUPT ENABLE FLAG	1· Enable interrupt 0. Disable interrupt
5	IEB	PORT B INTERRUPT ENABLE FLAG	1· Enable interrupt 0 Disable interrupt
6	TM1	COUNTER/TIMER CONTROL 00· No influence on counter/timer operation 01· Counter/timer operation discontinued (If not already stopped) 10 Counter/timer operation discontinued after the current counter/timer operation is completed 11. Counter/timer operation started	
7	TM2		

Status Register (7-bit)

The status register is a 7-bit latched register. The low-order 6 bits (bits 0~5) are used as status flags for the I/O ports. Bit 6 is used as a status flag for the counter/timer. The contents of the status register are transferred into the CPU by reading (INPUT instruction, I/O address XXXXX000). Details of the functions of the individual bits of the status register are shown in Table 3.

Table 3 Bit functions of the status register

Bit	Symbol	Function
0	INTR A	PORT A INTERRUPT REQUEST
1	A BF	PORT A BUFFER FULL FLAG
2	INTE A	PORT A INTERRUPT ENABLE
3	INTR B	PORT B INTERRUPT REQUEST
4	B BF	PORT B BUFFER FULL FLAG
5	INTE B	PORT B INTERRUPT ENABLE
6	TIMER	COUNTER/TIMER INTERRUPT (This flag is set to 1 when the final limit of the counter/timer is reached and is reset to 0 when the status is read)
7	—	This bit is not used

I/O PORTS

Command/status registers (8-bit/7-bit)

These registers are assigned address XXXXX000. When an OUTPUT command is executed, the contents of the command register are rewritten. When an INPUT command is executed, the contents of the status register are read.

Port A Register (8-bit)

Port A Register is assigned address XXXXX001. This register can be programmed as an input or output by setting the appropriate bits of the command register as shown in Table 2.

Port A can be operated in basic or strobe mode and is assigned I/O terminal PA_0~PA_7.

Port B Register (8-bit)

Port B register is assigned address XXXXX010. As with Port A register, this register can be programmed as an input or output by setting the appropriate bits of the command register as shown in Table 2. Port B can be operated in basic or strobe mode and is assigned I/O terminals PB_0~PB_7.

Port C Register (6-bit)

Port C register is assigned address XXXXX011. This port is used not only for input or output but also for controlling input/output operations of ports A and B by selectively setting bits 2 and 3 of the command register as shown in Table 2. Details of the functions of the various setting of bits 2 and 3 are shown in Table 4. Port C is assigned I/O terminals PC_0 ~ PC_5. When used as port control signals, the 3 low-order bits are assigned for port A while the 3 high-order bits are assigned for port B.

Table 4 Functions of port C

State Terminal	ALT 1	ALT 2	ALT 3	ALT 4
PC_5	Input	Output	Output	$\overline{\text{B STB}}$ (port B strobe)
PC_4	Input	Output	Output	B BF (port B buffer full)
PC_3	Input	Output	Output	B INTR (port B interrupt)
PC_2	Input	Output	$\overline{\text{A STB}}$ (port A strobe)	$\overline{\text{A STB}}$ (port A strobe)
PC_1	Input	Output	A BF (port A buffer full)	A BF (port A buffer full)
PC_0	Input	Output	A INTR (port A interrupt)	A INTR (port A interrupt)

CONFIGURATION OF PORTS

A block diagram of 1 bit of ports A or B is shown in Fig. 1. While port A or B is programmed as an output port, if the port is addressed by an input instruction, the contents of the selected port can be read. When a port is put in input mode, the output latch is cleared and writing into the output latch is disabled. Therefore when a port is changed to output mode from input mode, low-level signals are output through the port. When a reset signal is applied, all 3 ports (PA, PB, and PC) will be input ports and their output latches are cleared. Port C has the same configuration as ports A and B in modes ALT1 and ALT2.

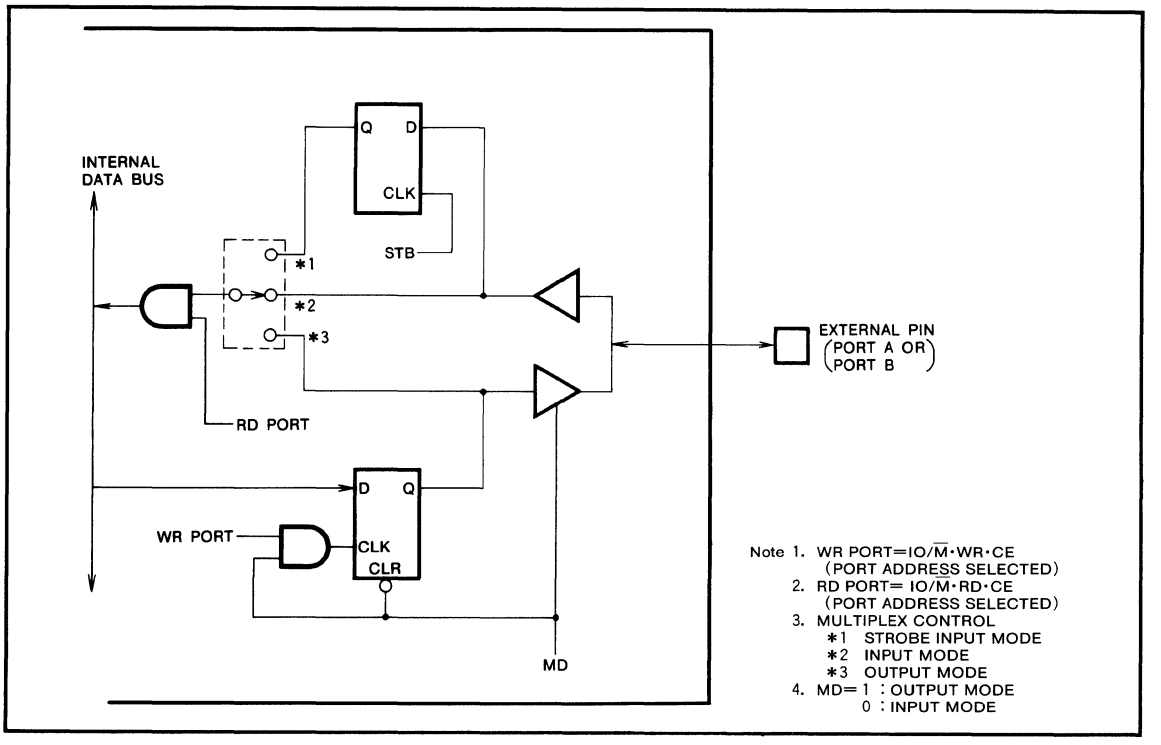


Fig. 1 Configuration for 1 bit of port A or B

Table 5 Basic functions of I/O ports

Address	$\overline{RD}$	$\overline{WR}$	Function
XXXXX000	L	H	AD bus ← Status register
	H	L	Command register ← AD bus
XXXXX001	L	H	AD bus ← Port A
	H	L	Port A ← AD bus
XXXXX010	L	H	AD bus ← Port B
	H	L	Port B ← AD bus
XXXXX011	L	H	AD bus ← Port C
	H	L	Port C ← AD bus

Table 6 Port control signal levels at ALT3 and ALT4

Control Signal	Output mode	Input mode
$\overline{STB}$	Input	Input
BF	"L"	"L"
INTR	"H"	"L"

The basic functions of the I/O ports are shown in Table 5. The control signal levels to ports A and B, when port C is programmed as a control port, are shown in Table 6.

COUNTER/TIMER

The counter/timer is composed of a 14-bit counting register and 2 mode flags. The register has two sections: I/O address XXXXX100 is assigned to the low-order 8 bits and I/O address XXXXX101 is assigned to the high-order 6 bits and timer mode flag 2 bits. The low-order bits 0～13 are used for counting or timing. The counter is initialized by the program and then counted down to 0. The initial value can be ranged from 2_{16} to $3FFF_{16}$. Bits 14 and 15 are used as mode flags.

The mode flags select 1 of 4 modes with functions as follows:

Mode 0: Outputs high-level signal during the former half of the counter operation
Outputs low-level signal during the latter half of the counter operation

Table 7 Format of counter/timer

Address	Bit Number								Function
	7	6	5	4	3	2	1	0	
XXXXX100	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0	The low-order 8 bits of the counter register
XXXXX101	M_2	M_1	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	M2,M1: Timer mode T_{13}~T_8 The high-order 6 bits of the counter register

Table 8 Timer mode

M_2	M_1	Timer operation
0	0	Outputs high-level signal during the former half of the counter operation Outputs low-level signal during the latter half of the counter operation (mode 0)
0	1	Outputs square wave signals in mode 0 (mode 1)
1	0	Outputs a low-level pulse during the final count down (mode 2)
1	1	Outputs a low-level pulse during each final count down (mode 3)

Mode 1: Outputs square wave signals as in mode 0
Mode 2: Outputs a low-level pulse during the final count down
Mode 3: Outputs a low-level pulse during each final count down

Starting and stopping the counter/timer is controlled by bits 6 and 7 of the command register (see Table 2 for details). The format and timer modes of the counter/timer register are shown in Table 7 and Table 8.

The contents of counter/timer is not affected by a reset, but counting is discontinued. To resume counting, a start command must be written into the command register as shown in Table 2. While operating 2n+1 count down in mode 0 and mode 1, a high-level signal is output during the former n+1 counting and a low-level signal is output during the later n counting.

RAM Hold Mode at Low Voltage (Power Down Mode)

Power down mode starts when the ALE input is fixed at low-level and other inputs at high or low-level after high-level of $\overline{CE}$ input in M5M81C55P-2 is latched by the falling edge of the ALE input.

The contents of RAM are not affected, even if V_{CC} falls into 2 V in power down mode.

RESET

The M5M81C55P-2 is reset by 400ns(min) pulse input on RESET pin.

By reset, all 3 ports are set to input mode. And counter/timer stops but contents of counter/timer is not reset. Therefore it is necessary to input start command again.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3~7	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		−0.3~V_{CC}+0.3	V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current	2.5	mA
T_{opr}	Operating free-air temperature range		−20~75	℃
T_{stg}	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~75℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
		I_{OH}=−20μA	4.4			
V_{OL}	Low-level output voltage	I_{OL}=2mA			0.45	V
I_I	Input leak current	V_I=0V, V_{CC}	−10		10	μA
I_{OZ}	Output floating leak current	V_O=0V~V_{CC}	−10		10	μA
C_I	Input terminal capacitance	V_{IL}=0V, f=1MHz, 25mVrms, T_a=25℃			10	pF
$C_I/_O$	Input/output terminal capacitance	$V_{I/OL}$=0V, f=1MHz, 25mVrms, T_a=25℃			20	pF
I_{CC}	Supply current from V_{CC} (operating)	f=5MHz			10	mA
I_{CCS}	Supply current from V_{CC} (stand by)	V_I=0V, V_{CC}			10	μA

Note 5 : Current flowing into an IC is positive, out is negative.

POWER DOWN ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, V_{SS}=0V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2.0			V
$I_{CC(PD)}$	Power down supply current from V_{CC}	V_{CC}=2V, other inputs=0V			10	μA

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{SU(A-L)}$	Address setup time before latch		30			ns
$t_{h(L-A)}$	Address hold time after latch		30			ns
$t_{d(L-RW)}$	Delay time, latch to read/write		40			ns
$t_{W(L)}$	Latch pulse width		70			ns
$t_{d(RW-L)}$	Delay time, read/write to latch		10			ns
$t_{W(RW)}$	Read/write pulse width		200			ns
$t_{SU(DQ-W)}$	Data setup time before write		100			ns
$t_{h(W-DQ)}$	Data hold time after write		0			ns
$t_{C(RW)}$	Read/write cycle time		200			ns
$t_{SU(P-R)}$	Port setup time before read		50			ns
$t_{h(R-P)}$	Port hold time after read		10			ns
$t_{W(STB)}$	Strobe pulse width		150			ns
$t_{SU(P-STB)}$	Port setup time before strobe		0			ns
$t_{h(STB-P)}$	Port hold time after strobe		100			ns
$t_{W(\phi H)}$	Timer input high-level pulse width		70			ns
$t_{W(\phi L)}$	Timer input low-level pulse width		40			ns
$t_{d(W-\phi)}$	Delay time, write to timer input		200			ns
$t_{C(\phi)}$	Timer input cycle time		200		DC	ns
$t_{r(\phi)}$	Timer input rise time				100	ns
$t_{f(\phi)}$	Timer input fall time				100	ns

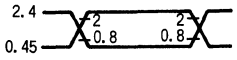
SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Propagation time from read to data output	C_L = 150pF			120	ns
$t_{PZV(A-DQ)}$	Propagation time from address to data output				330	ns
$t_{PVZ(R-DQ)}$	Propagation time from read to data floating (Note 6)		0		80	ns
$t_{PHL(W-P)}$ / $t_{PLH(W-P)}$	Propagation time from write to data output				300	ns
$t_{PLH(STB-BF)}$	Propagation time from strobe to BF flag				300	ns
$t_{PHL(R-BF)}$	Propagation time from read to BF flag				300	ns
$t_{PLH(STB-INTR)}$	Propagation time from strobe to interrupt				300	ns
$t_{PHL(R-INTR)}$	Propagation time from read to interrupt				300	ns
$t_{PHL(STB-BF)}$	Propagation time from strobe to BF flag				300	ns
$t_{PLH(W-BF)}$	Propagation time from write to BF flag				300	ns
$t_{PHL(W-INTR)}$	Propagation time from write to interrupt				300	ns
$t_{PHL(\phi-OUT)}$ / $t_{PLH(\phi-OUT)}$	Propagation time from timer input to timer output				300	ns

Note 6 : Test conditions are not applied.

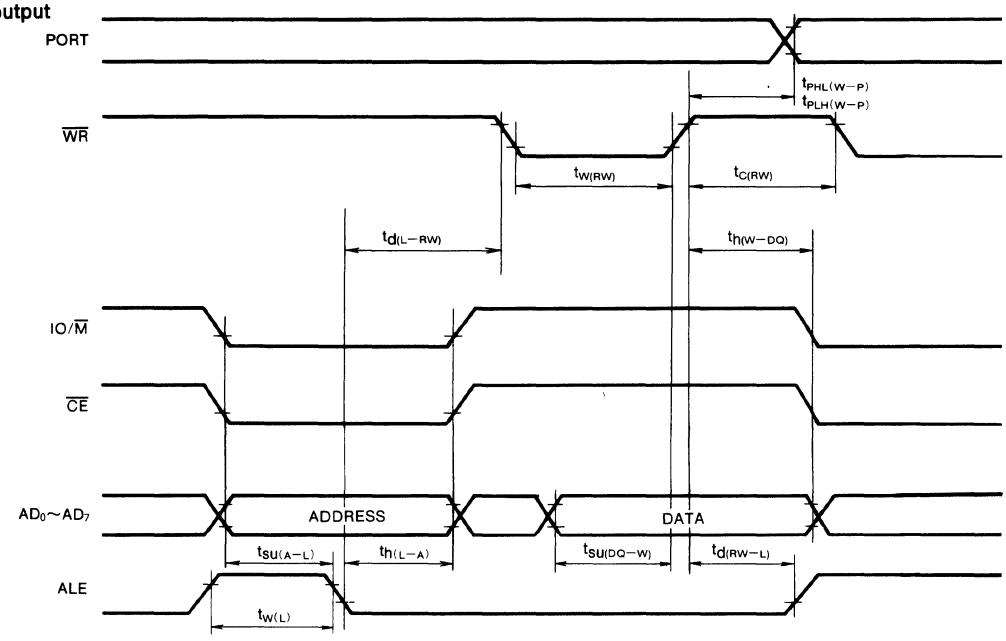
7 : A.C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	10ns
Input pulse fall time	10ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V

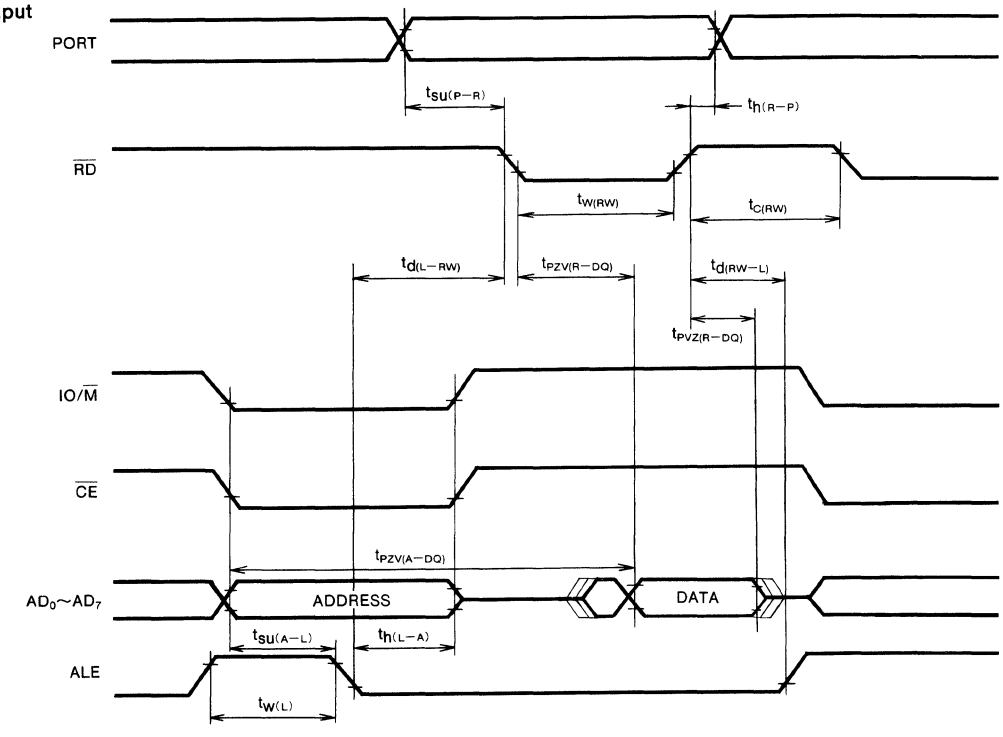


TIMING DIAGRAM

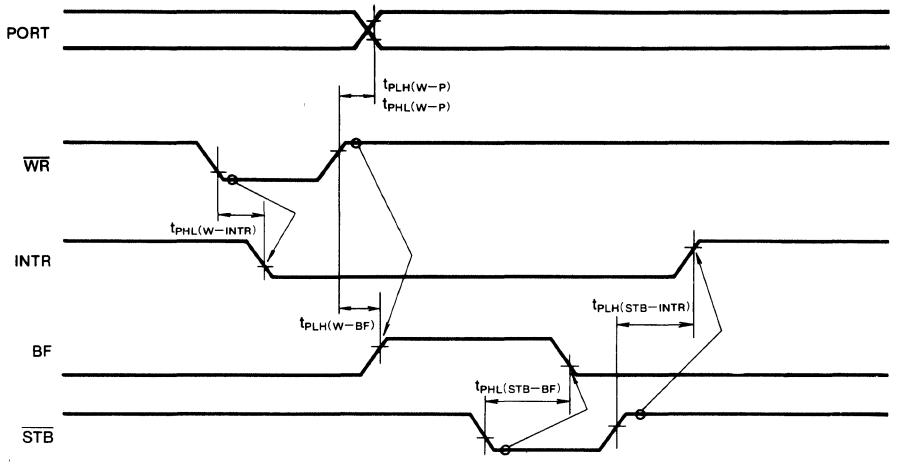
Basic output



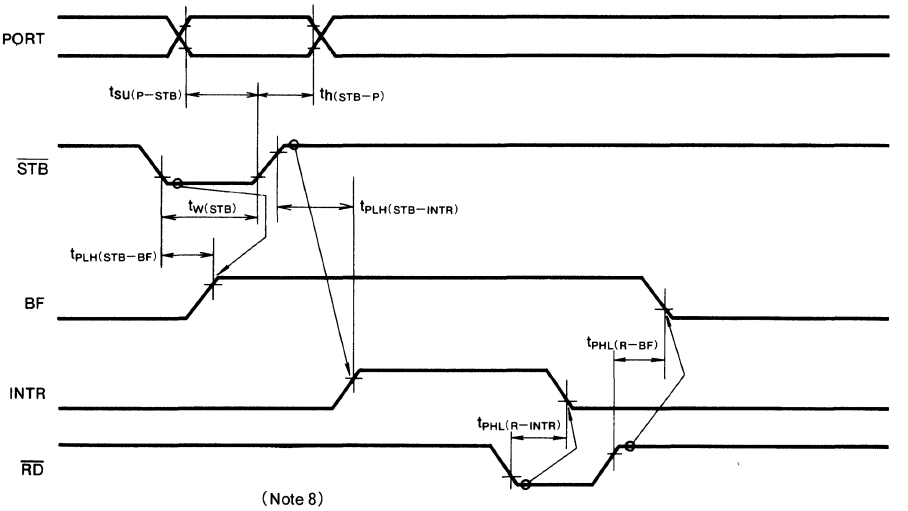
Basic input



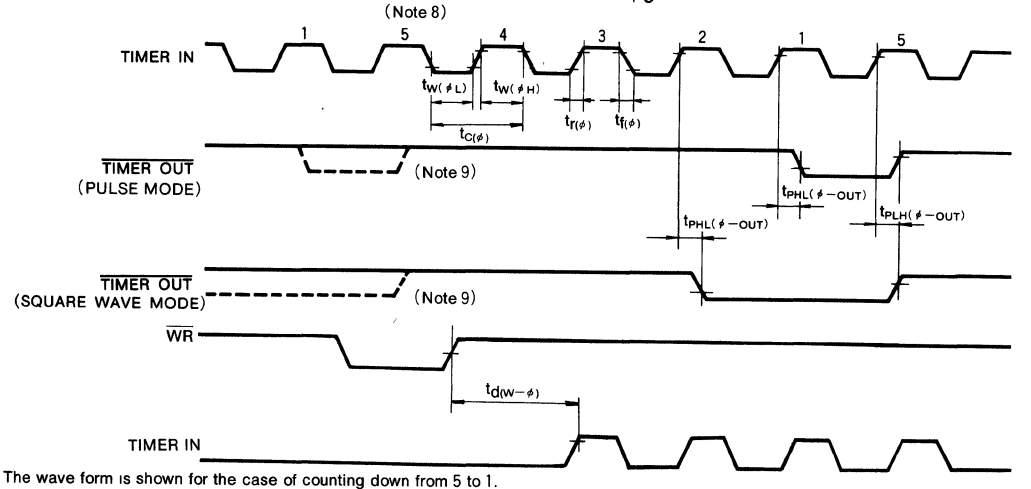
Strobed output



Strobed input



Timer



Note 8 : The wave form is shown for the case of counting down from 5 to 1.
9 : As long as the M1 mode flag of the timer register is at high-level, pulses are continuously output

M5M81C56P-2/FP-2/J-2

CMOS 2048-BIT STATIC RAM WITH I/O PORTS AND TIMER

DESCRIPTION

The M5M81C56P-2 is the 2K-bit RAM (256-word by 8-bit) fabricated by the silicon gate CMOS technology. This LSI has 3 I/O ports and a 14-bit counter/timer which make it a good extension of the functions of an 8-bit microcomputer. It is housed in 40-pin plastic molded DIP.

And preparatory for surface equipment M5M81C56FP-2 (SOP) and M5M81C56J-2 (PLCC).

FEATURES

- Having internal anti-circuit on RESET and ALE
- Single 5V supply voltage
- TTL compatible
- Power down mode
- Timer input : 5MHz (max)
- Read access time : 120ns (max)
- Static RAM: 256-word by 8-bit
- Programmable 8-bit I/O port: 2
- Programmable 6-bit I/O port: 1
- Programmable counter/timer: 14-bit
- Multiplexed address/data bus

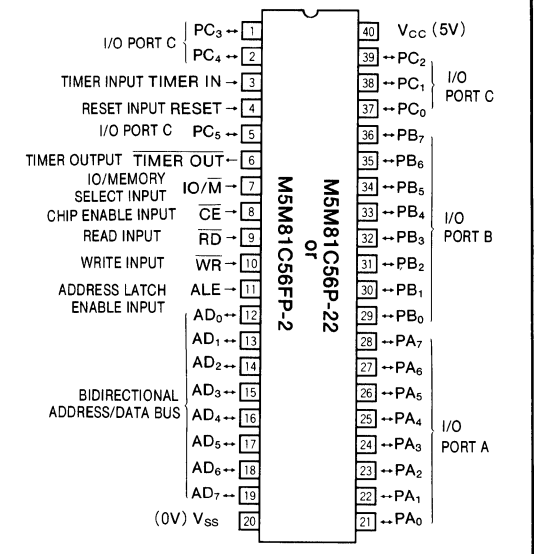
APPLICATION

Extension of I/O ports and timer function for microprocesser

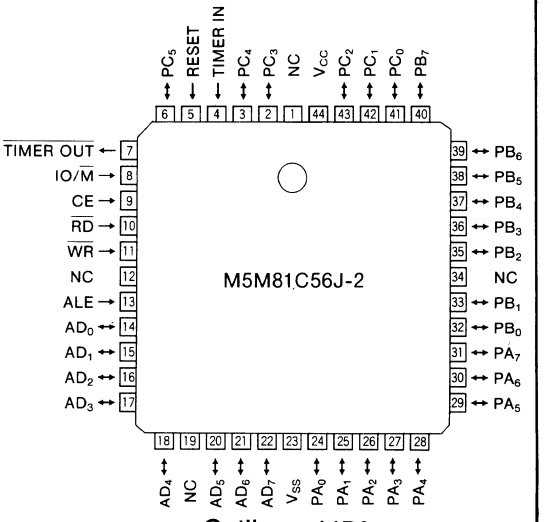
FUNCTION

The M5M81C56P-2 is composed of RAM, I/O ports and counter/timer. The RAM is a 2K-bit static RAM organized as 256-word by 8-bit. The I/O ports consist of 2 programmable 8-bit ports and 1 programmable 6-bit port. The terminals of the 6-bit port can be programmed as control terminals for the 8-bit ports, so that the 8-bit ports can be operated in a handshake mode. The counter/timer is composed of 14-bit down counter (events or time) and it can generate square wave pulses that can be used for counting and timing.

PIN CONFIGURATION (TOP VIEW)



Outline 40P4 (M5M81C56P-2)
40P2R (M5M81C56FP-2)

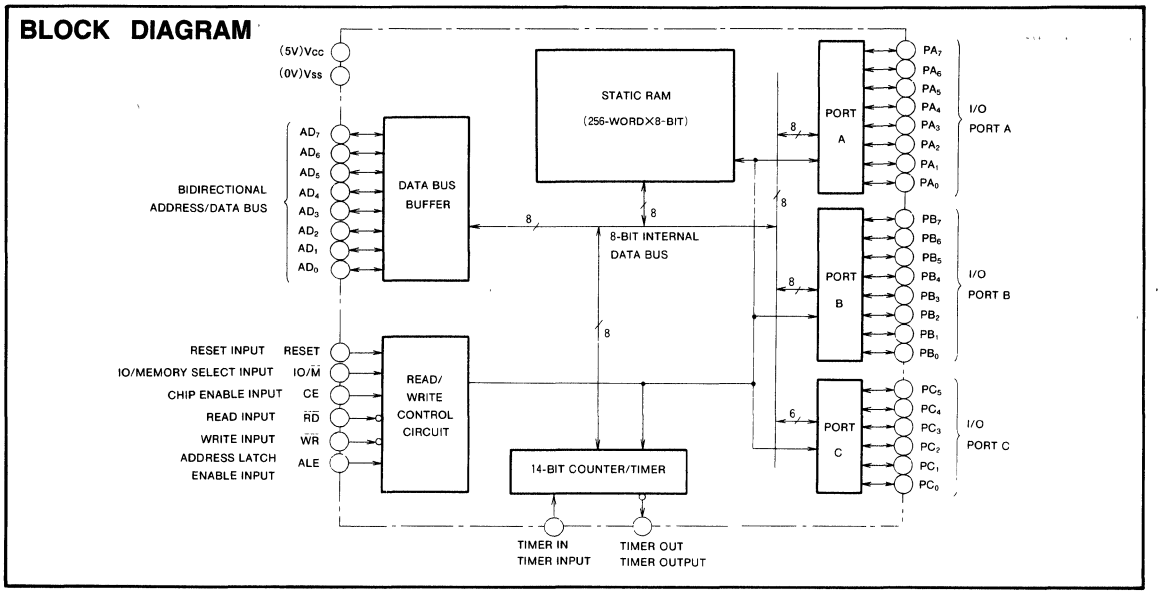


Outline 44P0

NC : NO CONNECTION

CMOS 2048-BIT STATIC RAM WITH I/O PORTS AND TIMER

BLOCK DIAGRAM



OPERATION

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to transfer the data while input or output instructions are being executed by the CPU. Command and address information is also transferred through the data bus buffer.

Read/Write Control Logic

The read/write control logic controls the transfer of data and commands by interpreting the signals (CE, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, ALE, RESET) from CPU.

Bidirectional Address/Data Bus (AD_0~AD_7)

The bidirectional address/data bus is a 3-state 8-bit bus. The 8-bit address is latched in the internal latch by the falling edge of ALE. Then if IO/$\overline{M}$ input signal is at high-level, the address of I/O port, counter/timer, or command register is selected. If it is at low-level, address of RAM is selected. The 8-bit data is transferred by read input ($\overline{RD}$) or write input ($\overline{WR}$).

Chip Enable Input (CE)

When CE is at high-level, the address information on address/data bus is stored in the M5M81C56P-2.

Read Input ($\overline{RD}$)

When $\overline{RD}$ is at low-level, the data bus buffer is active. If IO/$\overline{M}$ input signal is at low-level, the contents of RAM are read through the address/data bus. If IO/$\overline{M}$ input is at high-level, the contents of selected I/O port or counter/timer are read through the address/data bus.

Write Input ($\overline{WR}$)

When $\overline{WR}$ is at low-level, the data on the address/data bus are written into RAM if IO/$\overline{M}$ is at low-level, or they are written into I/O port, counter/timer or command register if IO/$\overline{M}$ is at high-level.

Address Latch Enable Input (ALE)

An address on the address/data bus is latched in the M5M81C56P-2 on the falling edge of ALE along with the levels of CE and IO/$\overline{M}$.

IO/Memory Input (IO/$\overline{M}$)

When IO/$\overline{M}$ is at low-level, the RAM is selected, while at high-level the I/O port, counter/timer or command register are selected.

I/O Port A (PA_0~PA_7)

Port A is an 8-bit general-purpose I/O port. Input/output setting is controlled by the system software.

I/O Port B (PB_0~PB_7)

Port B is an 8-bit general-purpose I/O port. Input/output setting is controlled by the system software.

I/O Port C (PC_0~PC_5)

Port C is a 6-bit I/O port that can also be used to output control signals of port A (PA) or port B (PB). The functions of port C are controlled by the system software. When port C is used to output control signals of ports A or B, the assignment of the signals to the pins is as shown in Table 1.

Table 1 Pin assignment of control signals of port C

Pin	Function	
PC_5	$\overline{B\ STB}$	(port B strobe)
PC_4	B BF	(port B buffer full)
PC_3	B INTR	(port B interrupt)
PC_2	$\overline{A\ STB}$	(port A strobe)
PC_1	A BF	(port A buffer full)
PC_0	A INTR	(port A interrupt)

Timer Input (TIMER IN)

The signal on this input terminal is used by the counter/timer for counting events or time. (5MHz max.)

Timer Output ($\overline{TIMER\ OUT}$)

A square wave signal or pulse from the counter/timer is output through this pin when in the operation mode.

Command Register (8-bit)

The command register is an 8-bit latched register. The low-order 4 bits (bits 0~3) are used for controlling and determination of mode of the ports. Bits 4 and 5 are used as interrupt enable flags for ports A and B when port C is used as a control port. Bits 6 and 7 are used for controlling the counter/timer. The contents of the command register are rewritten by output instructions (I/O address XXXXX000). Details of the functions of the individual bits of the command register are shown in Table 2.

Table 2 Bit functions of the command register

Bit	Symbol	Function	
0	PA	PORT A I/O SET	1 Output port A 0 Input port A
1	PB	PORT B I/O SET	1 Output port B 0 Input port B
2	PC_1	PORT C SET	00 ALT1 11 ALT2 01 ALT3 10 ALT4
3	PC_2		
4	IEA	PORT A INTERRUPT ENABLE FLAG	1 Enable interrupt 0 Disable interrupt
5	IEB	PORT B INTERRUPT ENABLE FLAG	1 Enable interrupt 0 Disable interrupt
6	TM1	COUNTER/TIMER CONTROL 00 No influence on counter/timer operation 01 Counter/timer operation discontinued (If not already stopped) 10 Counter/timer operation discontinued after the current counter/timer operation is completed 11. Counter/timer operation started	
7	TM2		

Status Register (7-bit)

The status register is a 7-bit latched register. The low-order 6 bits (bits 0~5) are used as status flags for the I/O ports. Bit 6 is used as a status flag for the counter/timer. The contents of the status register are transferred into the CPU by reading (INPUT instruction, I/O address XXXXX000). Details of the functions of the individual bits of the status register are shown in Table 3.

Table 3 Bit functions of the status register

Bit	Symbol	Function
0	INTR A	PORT A INTERRUPT REQUEST
1	A BF	PORT A BUFFER FULL FLAG
2	INTE A	PORT A INTERRUPT ENABLE
3	INTR B	PORT B INTERRUPT REQUEST
4	B BF	PORT B BUFFER FULL FLAG
5	INTE B	PORT B INTERRUPT ENABLE
6	TIMER	COUNTER/TIMER INTERRUPT (This flag is set to 1 when the final limit of the counter/timer is reached and is reset to 0 when the status is read)
7	—	This bit is not used

I/O PORTS

Command/status registers (8-bit/7-bit)

These registers are assigned address XXXXX000. When an OUTPUT command is executed, the contents of the command register are rewritten. When an INPUT command is executed, the contents of the status register are read

Port A Register (8-bit)

Port A Register is assigned address XXXXX001. This register can be programmed as an input or output by setting the appropriate bits of the command register as shown in Table 2.

Port A can be operated in basic or strobe mode and is assigned I/O terminal PA_0~PA_7.

Port B Register (8-bit)

Port B register is assigned address XXXXX010. As with Port A register, this register can be programmed as an input or output by setting the appropriate bits of the command register as shown in Table 2. Port B can be operated in basic or strobe mode and is assigned I/O terminals PB_0~PB_7.

Port C Register (6-bit)

Port C register is assigned address XXXXX011. This port is used not only for input or output but also for controlling input/output operations of ports A and B by selectively setting bits 2 and 3 of the command register as shown in Table 2. Details of the functions of the various setting of bits 2 and 3 are shown in Table 4. Port C is assigned I/O terminals PC_0 ~ PC_5. When used as port control signals, the 3 low-order bits are assigned for port A while the 3 high-order bits are assigned for port B.

Table 4 Functions of port C

State / Terminal	ALT 1	ALT 2	ALT 3	ALT 4
PC_5	Input	Output	Output	$\overline{\text{B STB}}$ (port B strobe)
PC_4	Input	Output	Output	B BF (port B buffer full)
PC_3	Input	Output	Output	B INTR (port B interrupt)
PC_2	Input	Output	$\overline{\text{A STB}}$ (port A strobe)	$\overline{\text{A STB}}$ (port A strobe)
PC_1	Input	Output	A BF (port A buffer full)	A BF (port A buffer full)
PC_0	Input	Output	A INTR (port A interrupt)	A INTR (port A interrupt)

CONFIGURATION OF PORTS

A block diagram of 1 bit of ports A or B is shown in Fig. 1. While port A or B is programmed as an output port, if the port is addressed by an input instruction, the contents of the selected port can be read. When a port is put in input mode, the output latch is cleared and writing into the output latch is disabled. Therefore when a port is changed to output mode from input mode, low-level signals are output through the port. When a reset signal is applied, all 3 ports (PA, PB, and PC) will be input ports and their output latches are cleared. Port C has the same configuration as ports A and B in modes ALT1 and ALT2.

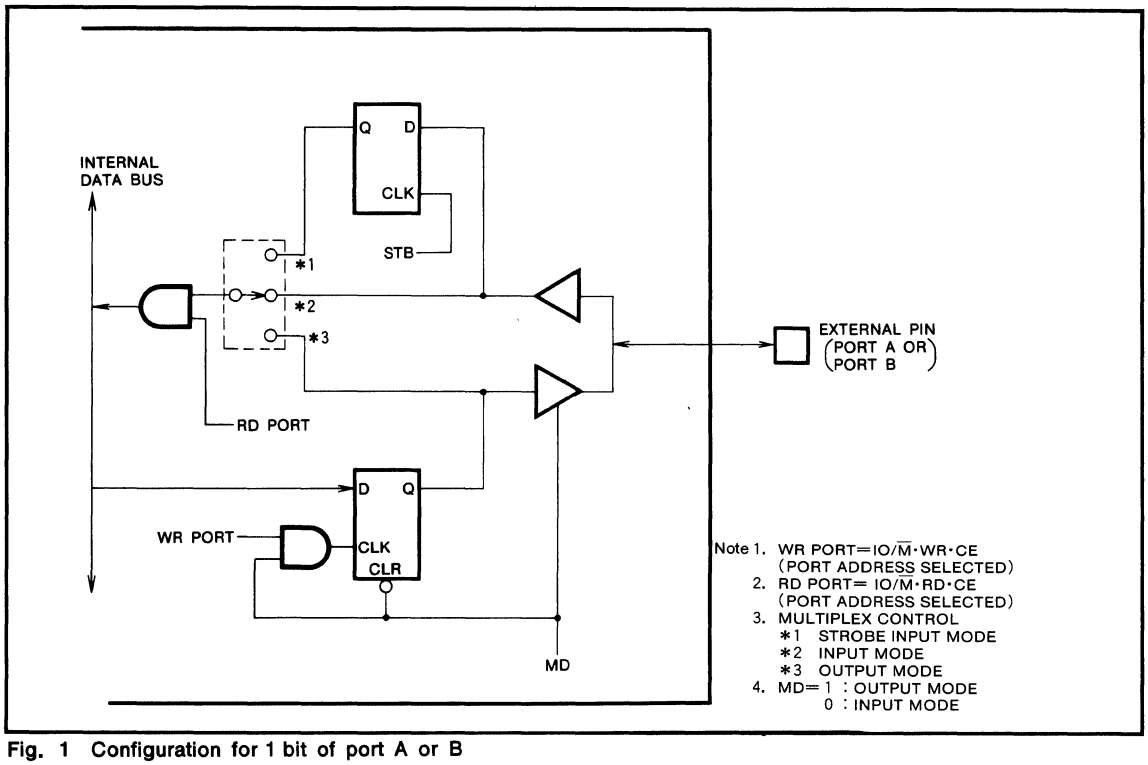


Fig. 1 Configuration for 1 bit of port A or B

Table 5 Basic functions of I/O ports

Address	$\overline{RD}$	$\overline{WR}$	Function
XXXXX000	L	H	AD bus ← Status register
	H	L	Command register ← AD bus
XXXXX001	L	H	AD bus ← Port A
	H	L	Port A ← AD bus
XXXXX010	L	H	AD bus ← Port B
	H	L	Port B ← AD bus
XXXXX011	L	H	AD bus ← Port C
	H	L	Port C ← AD bus

Table 6 Port control signal levels at ALT3 and ALT4

Control Signal	Output mode	Input mode
$\overline{STB}$	Input	Input
BF	"L"	"L"
INTR	"H"	"L"

The basic functions of the I/O ports are shown in Table 5. The control signal levels to ports A and B, when port C is programmed as a control port, are shown in Table 6.

COUNTER/TIMER

The counter/timer is composed of a 14-bit counting register and 2 mode flags. The register has two sections: I/O address XXXXX100 is assigned to the low-order 8 bits and I/O address XXXXX101 is assigned to the high-order 6 bits and timer mode flag 2 bits. The low-order bits 0～13 are used for counting or timing. The counter is initialized by the program and then counted down to zero. The initial value can be ranged from 2_{16} to $3FFF_{16}$. Bits 14 and 15 are used as mode flags.

The mode flags select 1 of 4 modes with functions as follows:

Mode 0: Outputs high-level signal during the former half of the counter operation
Outputs low-level signal during the latter half of the counter operation

Table 7 Format of counter/timer

Address	Bit Number								Function
	7	6	5	4	3	2	1	0	
XXXXX100	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0	The low-order 8 bits of the counter register
XXXXX101	M_2	M_1	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	M2,M1: Timer mode T_{13}~T_8: The high-order 6 bits of the counter register

Table 8 Timer mode

M_2	M_1	Timer operation
0	0	Outputs high-level signal during the former half of the counter operation Outputs low-level signal during the latter half of the counter operation (mode 0)
0	1	Outputs square wave signals in mode 0 (mode 1)
1	0	Outputs a low-level pulse during the final count down (mode 2)
1	1	Outputs a low-level pulse during each final count down (mode 3)

Mode 1: Outputs square wave signals as in mode 0
Mode 2: Outputs a low-level pulse during the final count down
Mode 3: Outputs a low-level pulse during each final count down

Starting and stopping the counter/timer is controlled by bits 6 and 7 of the command register (see Table 2 for details). The format and timer modes of the counter/timer register are shown in Table 7 and Table 8.
The contents of counter/timer is not affected by a reset, but counting is discontinued. To resume counting, a start command must be written into the command register as shown in Table 2. While operating 2n+1 count down in mode 0 and mode 1, a high-level signal is output during the former n+1 counting and a low-level signal is output during the later n counting.

RAM Hold Mode at Low Voltage (Power Down Mode)

Power down mode starts when the ALE input is fixed at low-level and other inputs at high or low-level after low-level of CE input in M5M81C56P-2 is latched by the falling edge of the ALE input.
The contents of RAM are not affected, even if V_{CC} falls into 2 V in power down mode.

RESET

The M5M81C56P-2 is reset by 400ns(min) pulse input on RESET pin.
By reset, all 3 ports are set to input mode. And counter/timer stops but contents of counter/timer is not reset. Therefore it is necessary to input start command again.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3~7	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		−0.3~V_{CC}+0.3	V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current.	2.5	mA
T_{opr}	Operating free-air temperature		−20~75	℃
T_{stg}	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~75℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, V_{CC}= 5 V±10%,V_{SS}=0V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
		I_{OH}=−20μA	4.4			
V_{OL}	Low-level output voltage	I_{OL}=2mA			0.45	V
I_I	Input leak current	V_I=0V, V_{CC}	−10		10	μA
I_{OZ}	Output floating leak current	V_O=0V~V_{CC}	−10		10	μA
C_I	Input terminal capacitance	V_{IL}=0V, f=1MHz, 25mVrms, T_a=25℃			10	pF
$C_{I/O}$	Input/output terminal capacitance	$V_{I/OL}$=0V, f=1MHz, 25mVrms, T_a=25℃			20	pF
I_{CC}	Supply current from V_{CC} (operating)	f=5MHz			10	mA
I_{CCS}	Supply current from V_{CC} (stand by)	V_I=0V, V_{CC}			10	μA

Note 5 : Current flowing into an IC is positive, out is negative.

POWER DOWN ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, V_{SS}=0Vunless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2.0			V
$I_{CC(PD)}$	Power down supply current from V_{CC}	V_{CC}=2V, other inputs=0V			10	μA

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±10%,V_{SS}=0V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(A-L)}$	Address setup time before latch		30			ns
$t_{h(L-A)}$	Address hold time after latch		30			ns
$t_{d(L-RW)}$	Delay time, latch to read/write		40			ns
$t_{w(L)}$	Latch pulse width		70			ns
$t_{d(RW-L)}$	Delay time, read/write to latch		10			ns
$t_{w(RW)}$	Read/write pulse width		200			ns
$t_{su(DQ-W)}$	Data setup time before write		100			ns
$t_{h(W-DQ)}$	Data hold time after write		0			ns
$t_{c(RW)}$	Read/write cycle time		200			ns
$t_{su(P-R)}$	Port setup time before read		50			ns
$t_{h(R-P)}$	Port hold time after read		10			ns
$t_{w(STB)}$	Strobe pulse width		150			ns
$t_{su(P-STB)}$	Port setup time before strobe		0			ns
$t_{h(STB-P)}$	Port hold time after strobe		100			ns
$t_{w(\phi H)}$	Timer input high-level pulse width		70			ns
$t_{w(\phi L)}$	Timer input low-level pulse width		40			ns
$t_{d(W-\phi)}$	Delay time, write to timer input		200			ns
$t_{c(\phi)}$	Timer input cycle time		200		DC	ns
$t_{r(\phi)}$	Timer input rise time				100	ns
$t_{f(\phi)}$	Timer input fall time				100	ns

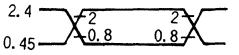
SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}= 5 V±10%, V_{SS}=0V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Propagation time from read to data output	C_L = 150pF			120	ns
$t_{PZV(A-DQ)}$	Propagation time from address to data output				330	ns
$t_{PVZ(R-DQ)}$	Propagation time from read to data floating (Note 6)		0		80	ns
$t_{PHL(W-P)}$ / $t_{PLH(W-P)}$	Propagation time from write to data output				300	ns
$t_{PLH(STB-BF)}$	Propagation time from strobe to BF flag				300	ns
$t_{PHL(R-BF)}$	Propagation time from read to BF flag				300	ns
$t_{PLH(STB-INTR)}$	Propagation time from strobe to interrupt				300	ns
$t_{PHL(R-INTR)}$	Propagation time from read to interrupt				300	ns
$t_{PHL(STB-BF)}$	Propagation time from strobe to BF flag				300	ns
$t_{PLH(W-BF)}$	Propagation time from write to BF flag				300	ns
$t_{PHL(W-INTR)}$	Propagation time from write to interrupt				300	ns
$t_{PHL(\phi-OUT)}$ / $t_{PLH(\phi-OUT)}$	Propagation time from timer input to timer output				300	ns

Note 6 : Test conditions are not applied

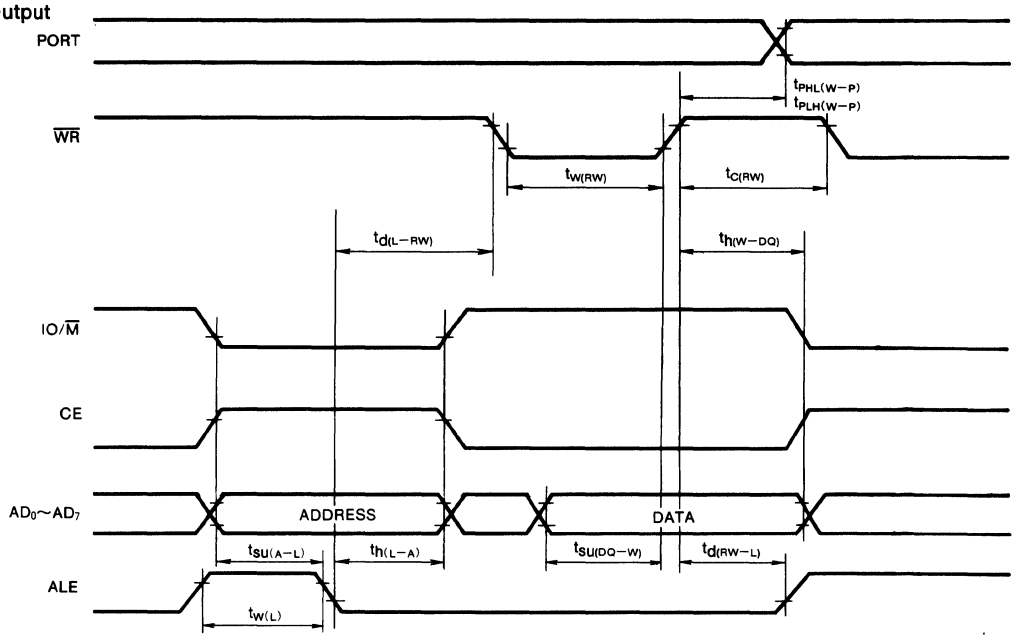
7 : A C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	10ns
Input pulse fall time	10ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V

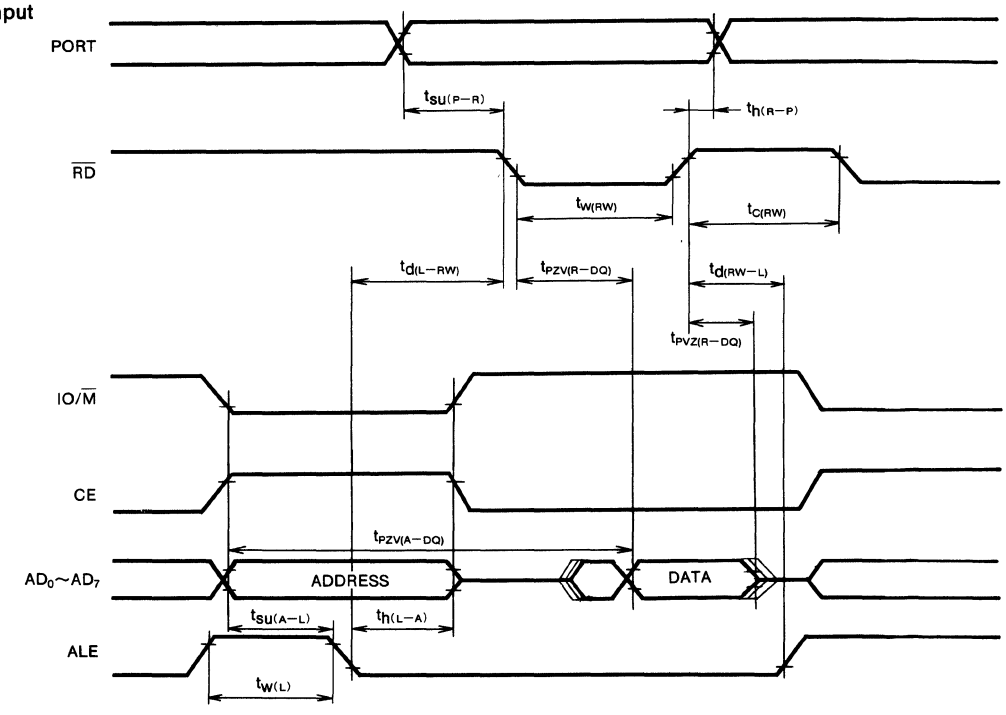


TIMING DIAGRAM

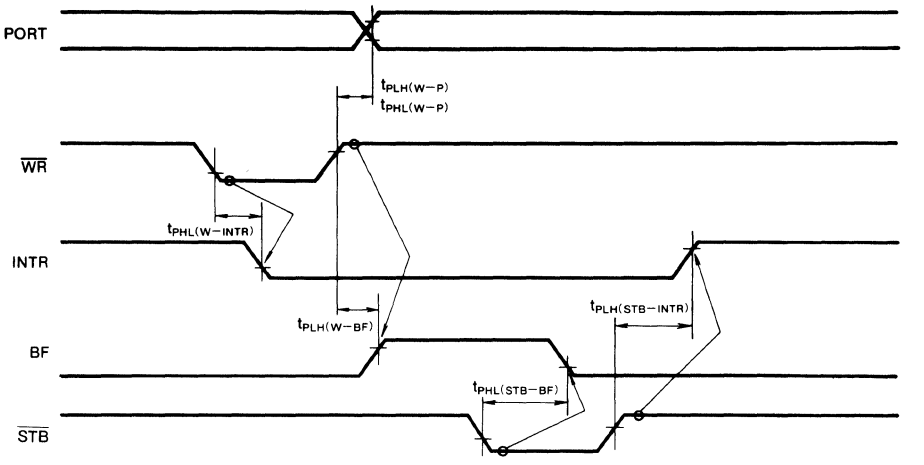
Basic Output



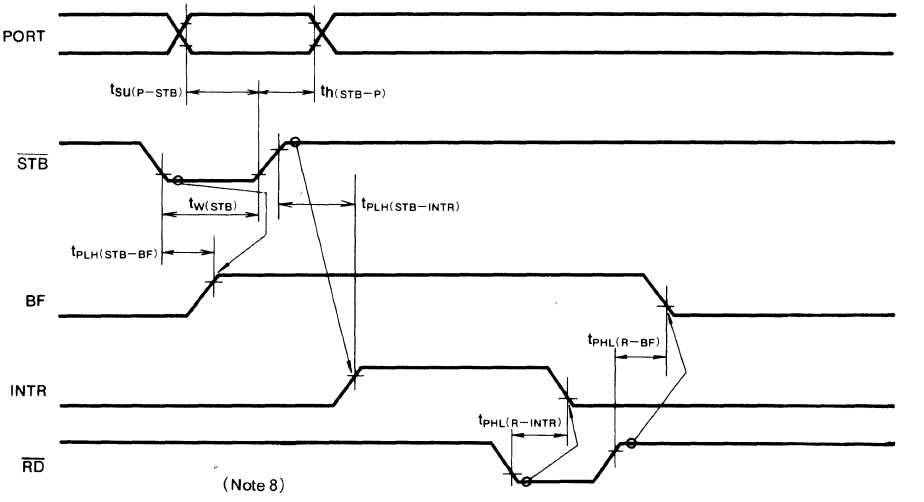
Basic Input



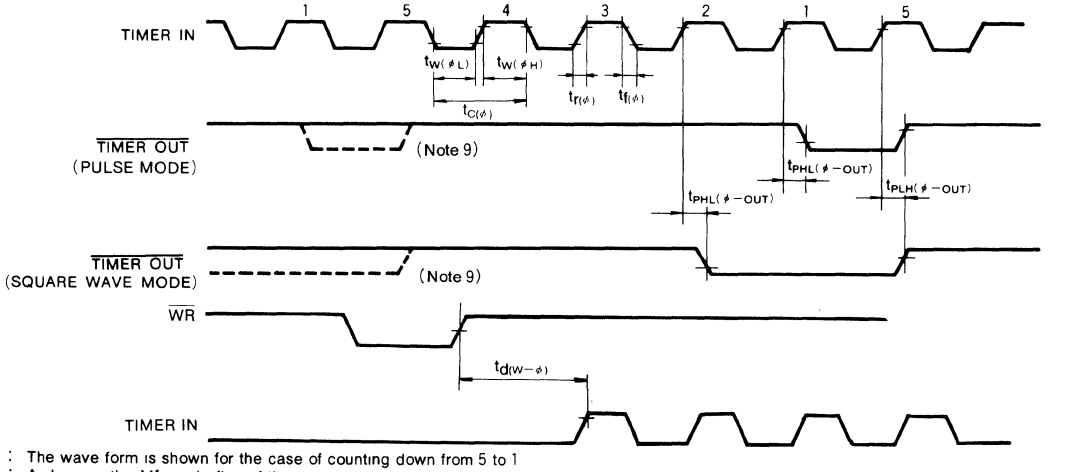
Strobed output



Strobed input



Timer



Note 8 : The wave form is shown for the case of counting down from 5 to 1
9 : As long as the M1 mode flag of the timer register is at high-level, pulses are continuously output

M5M82C37AP-5/FP-5/J-5

CMOS PROGRAMMABLE DMA CONTROLLER

DESCRIPTION

The M5M82C37AP-5 is a programmable 4-channel DMA (Direct Memory Access) controller. This device is specially designed to simplify data transfer at high transfer rate for microcomputer systems.

Fabricated using the silicon-gate CMOS technology. It is housed in a 40-pin plastic molded DIP.

And preparatory for surface equipment M5M82C37AFP-5 (SOP) and M5M82C37AJ-5(PLCC).

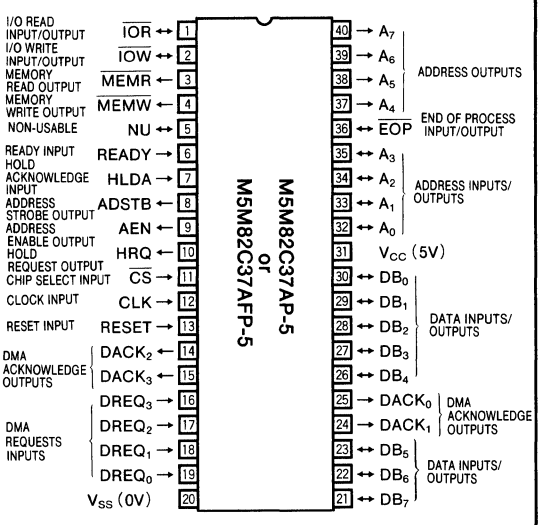
FEATURES

- Single 5V supply voltage
- TTL compatible
- Having internal anti-noise circuit on RESET and $\overline{IOW}$ pins
- Four channel DMA controls with priority DMA request acknowledge functions
- DMA enable/disable, automatic initialization enable/disable, address increment/decrement programmability for each channel
- Programmable DREQ input and DACK output logic polarity
- Direct connecting permits easy DMA channel expansion.
- Memory to memory data transfer
- EOP input/output permits DMA operation completion check as well as forcibly completing DMA operation.

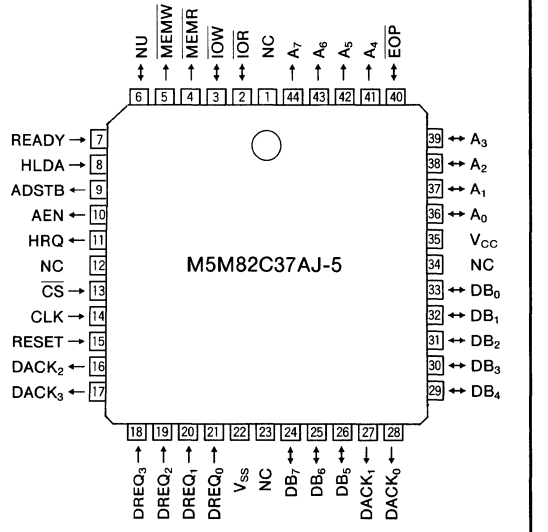
APPLICATION

DMA control of peripheral equipment such as floppy disketes and CRT terminals that require high-speed data transfer.

PIN CONFIGURATION (TOP VIEW)

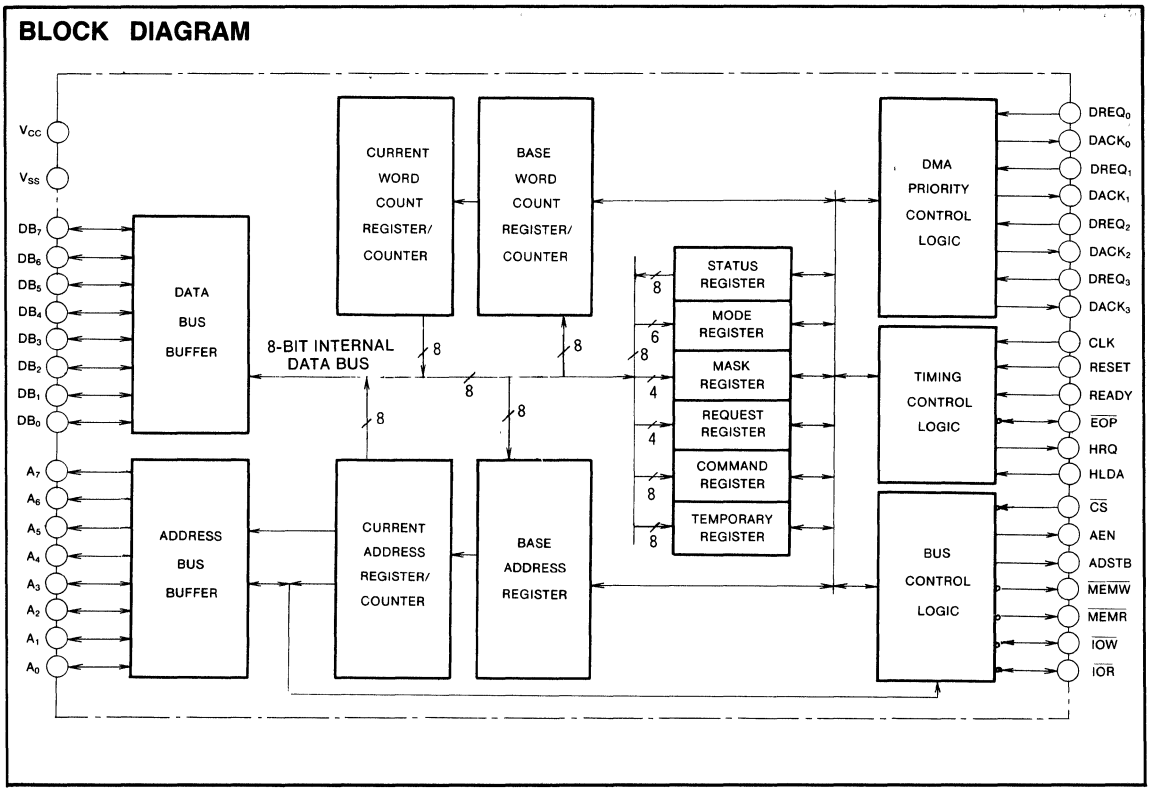


Outline 40P4 (M5M82C37AP-5)
40P2R (M5M82C37AFP-5)



Outline 44P0 NC : NO CONNECTION

BLOCK DIAGRAM



FUNCTION

M5M82C37AP-5 is a programmable DMA controller LSI used in microprocessor systems.

This device basically consists of a DMA request control block for acknowledging DMA requests, a CPU interface for exchanging data and commands with the CPU, a timing control circuit for controlling each of the various types of timing, and a register for holding and counting DMA addresses and number of transfer words.

After setting the transfer mode, starting address, and byte number in each of the registers and when a DMA request is made to an unmasked channel, the M5M82C37AP-5 requires use of the bus to the CPU. When the HLDA signal is received from the CPU, the DMA acknowledge signal is sent to DMA requesting channel with the highest priority and begins DMA operation.

During DMA operation, the contents of the low-byte of the transfer memory address are output through $A_7 \sim A_0$. Every time a change in the high-order 8 bits values is necessitated immediately after DMA operation has begun or due to borrowing or decrement during DMA operation, the change is output via pins $DB_7 \sim DB_0$ to the externally mounted latch circuit. After the address is transmitted, read and write signals are sent to the memories and peripherals activating DMA transfer.

PIN DESCRIPTION

$\overline{IOR}$ input/output (I/O read input/output)

The function of this pin differs depending on the state of the M5M82C37AP-5.

In DMA operation, the $\overline{IOR}$ outputs low-level pulses providing read timing to the peripheral devices.

In cascade mode DMA, this pin becomes high impedance.

In non-DMA mode, $\overline{IOR}$ is an input to read the contents of the registers in the M5M82C37AP-5.

$\overline{IOW}$ input/output (I/O write input/output)

The function of this pin differs depending on the state of the M5M82C37AP-5.

In DMA operation, $\overline{IOW}$ outputs a low-level pulse to denote the write timing to peripheral devices.

In cascade mode DMA, this pin becomes high impedance.

In non-DMA mode, $\overline{IOW}$ is input to write data to the registers of the M5M82C37AP-5.

$\overline{MEMR}$ output (memory read output)

In DMA mode, this pin outputs a low-level pulse to denote the memory read timing.

In cascade mode DMA or in non-DMA operation this pin becomes high-impedance.

$\overline{MEMW}$ output (memory write output)

In DMA mode, this pin outputs a low-level pulse to denote the memory write timing.

In cascade mode DMA or in non-DMA operation this pin becomes high-impedance.

NU pin (non-usable)

Pin 5 (M5M82C37AJ-5 : Pin 6) is a non-usable pin. This pin should be tied to V_{CC}, or it should be left open.

READY input (ready input)

This input is used to extend the read or write pulse in the DMA operation. As long as low-level is input, the DMA transfer period is extended. If no timing extension is needed, this input should be tied to V_{CC}.

Note : The ready input level must be stable near the falling edge of the clock input. If the minimum READY setup time from clock or the minimum READY hold time after clock is violated, M5M82C37AP-5 might go into illegal DMA operations

HLDA input (hold acknowledge input)

This input means that the CPU acknowledges the use of the bus. If M5M82C37AP-5 sets the HRQ output high-level and the HLDA input goes to high-level the M5M82C37AP-5 begins DMA operation.

Note : (i)When HLDA is high-level, $\overline{CS}$ input is disabled and unexpected read or write operation to M5M82C37AP-5 is prevented.

(ii)At least 1 clock period is required from HRQ rising edge to HLDA rising edge

ADSTB output (address strobe output)
This pin outputs a high-level pulse when the higher 8 bits of the transfer address is output through data bus at the DMA operation. This pulse is used as the strobe pulse for the external address latch circuit.
In non-DMA mode or in cascade mode DMA this output remains low-level.

AEN output (address enable output)
AEN is an output which denotes that the bus control signal address output etc. from the M5M82C37AP-5 are valid. When AEN output is high-level, they are valid output, so AEN is used as a control input for an external three-state bus buffer.

HRQ output (hold request output)
This output denotes that the M5M82C37AP-5 requests the use of the bus to the CPU. The M5M82C37AP-5 sets HRQ high in response to the DMA request.

$\overline{CS}$ input (chip select input)
This input is a chip select signal which is set to low-level when the CPU reads or writes data to the M5M82C37AP-5. When HLDA is high-level, this input is masked and the M5M82C37AP-5 is not selected.

CLK input (clock input)
The master clock for the M5M82C37AP-5 is input.

RESET input (reset input)
When a high-level pulse is input from RESET, the M5M82C37AP-5 is set to the initial state.

DACK0, DACK1, DACK2, DACK3 output (DMA acknowledge output)
DMA acknowledge is the signals which shows a peripheral device whether DMA operaiton for its channel is under execution.
By resetting, they become active low outputs, but they can be mode into active high outputs by altering the contents of the command register.

DREQ0, DREQ1, DREQ2, DREQ3 input (DMA request input)
DREQ is an input which shows that a peripheral device requests DMA service. By resetting, they become active high inputs but they can be made into active low inputs by altering the contents of the command register. DREQ should keep in active until the DACK output returns.

V_{SS}
V_{SS} is connected to system ground.

$DB_7 \sim DB_0$ inputs/outputs (data bus inputs/outputs)
In non-DMA mode, the contents of the registers of the M5M82C37AP-5 are read out or written through $DB_7 \sim DB_0$.
In DMA mode, the higher 8 bits of the transfer address are output through $DB_7 \sim DB_0$ in the S_1 state. In the memory to memory DMA mode, data to be transferred between memories via the temporary register are read and written by the M5M82C37AP-5 through $DB_7 \sim DB_0$.

V_{CC}
The 5V power supply is connected through V_{CC}.

$A_7 \sim A_4$ output, $A_3 \sim A_0$ input/output (address output, address input/output)
In the DMA mode, the lower 8 bits of the transfer address are output through $A_7 \sim A_0$.
In cascade mode DMA, they become high-impedance. In the non-DMA mode, $A_3 \sim A_0$ become register select address inputs, while $A_7 \sim A_4$ become high-impedance.

$\overline{EOP}$ input/output (end of process input/output)
$\overline{EOP}$ is an N-channel open drain input/output. When the word count register reaches count-up, a low-level pulse is output from $\overline{EOP}$. (This is called internal $\overline{EOP}$.) $\overline{EOP}$ may be pulled down to low-level. If $\overline{EOP}$ is pulled down during DMA operation, the DMA operation is forcibly terminated. (This is called external $\overline{EOP}$.)

Note : In cascade mode DMA, the $\overline{EOP}$ pulse is not output, and external $\overline{EOP}$ cannot terminate cascade mode DMA operation

OPERATION

The unit of operation of the M5M82C37AP-5 is one clock period long and is called a 'state'. The M5M82C37AP-5 has seven kinds of states.

The following is the description of the basic DMA operation. When the M5M82C37AP-5 is DMA disabled or no DMA request comes for unmasked DMA channel, the M5M82C37AP-5 is in stand-by condition. At this time the M5M82C37AP-5 repeats S_I (Inactive state) until a valid DMA request comes. When the M5M82C37AP-5 is enabled and a valid DMA request arrives, the M5M82C37AP-5 sets HRQ output high-level and waits until the use of the bus is acknowledged. This state is called S_0 state. The M5M82C37AP-5 repeats S_0 state as long as the HLDA input is low-level. When HLDA goes to high, the M5M82C37AP-5 begins DMA operation.

Care must be taken became the M5M82C37AP-5 requires at least 1 clock period from the HRQ rising edge to the HLDA rising edge. (i.e. S_0 state must be repeated at least twice.)

In DMA operation, the M5M82C37AP-5 normally executes four (or three) states per one word transfer.

These four states are called S_1, S_2, S_3 and S_4 state in sequence.

In S_1 state, AEN is set to high-level (if AEN is low-level), the lower 8 bits of data of the transfer address are output through $A_7 \sim A_0$ and the higher 8 bits of address data are output through $DB_7 \sim DB_0$. The higher address data are output only in the S_1 state, so the strobe pulse for the external address latch circuit is output from ADSTB. The S_1 state is not executed if the higher 8 bits of address data are not changed in demand mode DMA or block mode DMA.

In the S_2 state, $\overline{MEMR}$ or $\overline{IOR}$ output is set to low-level. If the S_1 state is not executed, address outputs $A_7 \sim A_0$ are changed at the S_2 state also.

In the S_3 state, $\overline{MEMW}$ or $\overline{IOW}$ output goes down to low-level. The S_4 state is the last state of a word transfer. $\overline{MEMR}$ (or $\overline{IOR}$) and $\overline{IOR}$ (or $\overline{MEMW}$) outputs rise up to high-level. And the contents of the current address register and the current word counter are updated.

If DMA continues in demand mode or block mode, the S_1 or S_2 state follows after the S_4 state.

If not the S_I state follows after S_4. (In single mode DMA, S_I always follows after S_4.)

When the M5M82C37AP-5 returns to the S_I state, the HRQ and AEN outputs are reset, $A_7 \sim A_4$, $DB_7 \sim DB_0$, $\overline{MEMR}$, $\overline{MEMW}$ are set to high-impedance and $A_3 \sim A_0$, $\overline{IOR}$, $\overline{IOW}$ are set to inputs.

If the read or write pulse width is not sufficient for the memories or the peripherals, the transfer time can be extended by setting the READY input to low-level. Until READY goes up to high-level, wait states (S_W) are inserted before S_4 and read , write, and address outputs are hold.

The M5M82C37AP-5 has four type of DMA transfers.

- READ TRANSFER

  This is the transfer operation from memories to peripheral. Low-level pulses are output from $\overline{MEMR}$ and $\overline{IOW}$, while $\overline{MEMW}$, $\overline{IOR}$ remain high-level.

- WRITE TRANSFER

  This is the transfer operation from peripheral to memories. Low-level pulses are output from $\overline{MEMW}$ and $\overline{IOR}$, while $\overline{MEMR}$ and $\overline{IOW}$ remain high-level.

- VERIFY TRANSFER

  This is the dummy transfer, $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$ and $\overline{IOW}$ all remain high-level. (not high-impedance). Low-level input to READY is ignored. AEN, ADSTB, DACK and address information are normally output.

- MEMORY-TO-MEMORY TRANSFER

  This is the transfer from the memory address designated by channel 0 to the memory address designated by channel 1. In this transfer, the channel 0 address and channel 1 address are alternately output. when the channel 0 address is active, the $\overline{MEMR}$ pulse is output at the same time and the memory data are read and written to the temporary register when the channel 1 address is active, the $\overline{MEMW}$ pulse is output and the contents of the temporary register are output from the data bus.

  Accordingly, ϕ1 byte memory transfer is executed by two operations a read operation which consists of S_{11}, S_{12}, S_{13} and S_{14} states and write operation which consists of S_{21}, S_{22}, S_{23} and S_{24} states.

  In memory to memory DMA, The transfer type assignment of ch 0, ch 1 mode register (read, write or verify) is ignored.

Notes for memory-to-memory transfer

Observe the following points when programming memory-to-memory DMA.

- The contents of the word count register of channel 0 and 1 must be programmed identically.
- The transfer mode of channel 0 and 1 must be set to the block transfer mode.
- All the mask bits must be set to inhibit external DMA request input. (Memory-to-memory DMA is started by software DMA request to channel 0.)
- In memory-to-memory DMA operation, all the DACK outputs are inactive. (but AEN is set during transfer.)

PRIORITY

Two kinds of DMA priority can be programmed for the M5M82C37AP-5. (Command register bit 4) If plural channels request DMA at the same time, DMA is acknowledged for the channel which has the highest priority. (Table 1)

(1) Fixed Priority (bit 4=0)
The DMA channel which has the highest priority is channel 0. Channel 1 has the second, channel 2 has the third and channel 3 has the lowest priority.

(2) Rotating Priority (bit 4=1)
This priority mode is that the channel which has serviced the DMA request, has the lowest priority at the next DMA operation. (Just after reset the lowest priority channel is channel 3)
For example, just after channel 1 DMA is executed, channel 2 has the highest priority, channel 3 has the second highest, channel 0 has the third and channel 1 has the lowest priority.

Table 1 DMA priority for the M5M82C37AP-5

Priority type	DMA channel serviced	DMA priority for next transfer			
		Highest	2nd	3rd	Lowest
Fixed priority	————	ch0	ch1	ch2	ch3
Rotating priority	ch0	ch1	ch2	ch3	ch0
	ch1	ch2	ch3	ch0	ch1
	ch2	ch3	ch0	ch1	ch2
	ch3	ch0	ch1	ch2	ch3

DESCRIPTION OF THE TRANSFER MODE

The following is the description of the transfer mode of the M5M82C37AP-5

(1) **Single mode DMA transfer**

In single mode DMA, the M5M82C37AP-5 executes only one word transfer when the bus control is acknowledged by the CPU, and when the S_4 state is ended, the M5M82C37AP-5 reset HRQ output and releases the bus.

If the DMA request input continues at active level, at least one S_I state is executed since the HLDA input falls down to low-level, and HRQ is kept low-level. Accordingly, M5L8085AP CPU etc. can execute at least one instruction between DMA transfer.

(2) **Block mode DMA transfer**

In the block mode, once the DMA request is acknowledged, the DMA is executed continuously until the terminal count (TC) occurs.

TC means that

(I)The contents of the current word count register are about to be counted down from 0000_{16} to $FFFF_{16}$

or that

(II)an external $\overline{EOP}$ pulse is input before the S_2 state.

The DREQ input should be kept active until the DACK output is made active, but once DMA is acknowledged, DMA transfer continues until TC occurs even when DMA request becomes inactive.

When DMA is executed continuously, the S_1 or S_2 state follows directly after S_4. If the contents of the higher 8 bits of the address are not changed at the following word transfer, the S_1 state is skipped and the S_2 state is executed just after S_4.

(3) **Demand mode DMA transfer**

In the demand mode, DMA is executed continuously while the DMA request is active.

Once the DMA is acknowledged to the channel which is programmed for the demand mode, DMA operation is executed continuously until TC occurs or the DMA request becomes inactive.

If DMA stops due to an inactive DREQ before TC, the rest of the DMA will be resumed when DREQ becomes active and the DMA is acknowledged again.

The operation during DMA is almost the same as in the block mode DMA.

(4) **Cascade mode DMA transfer**

This mode is used for DMA channel expansion by cascade connection when more than 4 channels are required. (See fig. 1)

If the DMA request for the channel which is programmed in the cascade mode occurs and the request is acknowledged, only the DACK output becomes active. ($\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$, $DB_7 \sim DB_0$, $A_7 \sim A_0$ become floating. AEN, ADSTB outputs stay at low-level. $\overline{CS}$ and READY inputs are ignored.)

Accordingly the cascade mode DMA operation of the M5M82C37AP-5 is only that it requests a bus hold request for the CPU instead of the low-level M5M82C37AP-5 and transmits the bus acknowledgement signal by setting DACK active.

Note :

- The contents of the base and current address/word count regsiters of channels programmed in the cascade mode are invalid and change unpredictably.
- A software DMA request for the channel which is programmed in cascade mode may cause the system of hang up
- When cascaded M5M82C37AP-5's are connected as shown in fig. 1, the high-level M5M82C37AP-5 should be initialized first and the DACK output set high-active in order to initialize the low-level M5M82C37AP-5's because the registers of the M5M82C37AP-5 cannot be read or written when HLDA input is high-level
- An external $\overline{EOP}$ cannot terminate cascade mode DMA operation.

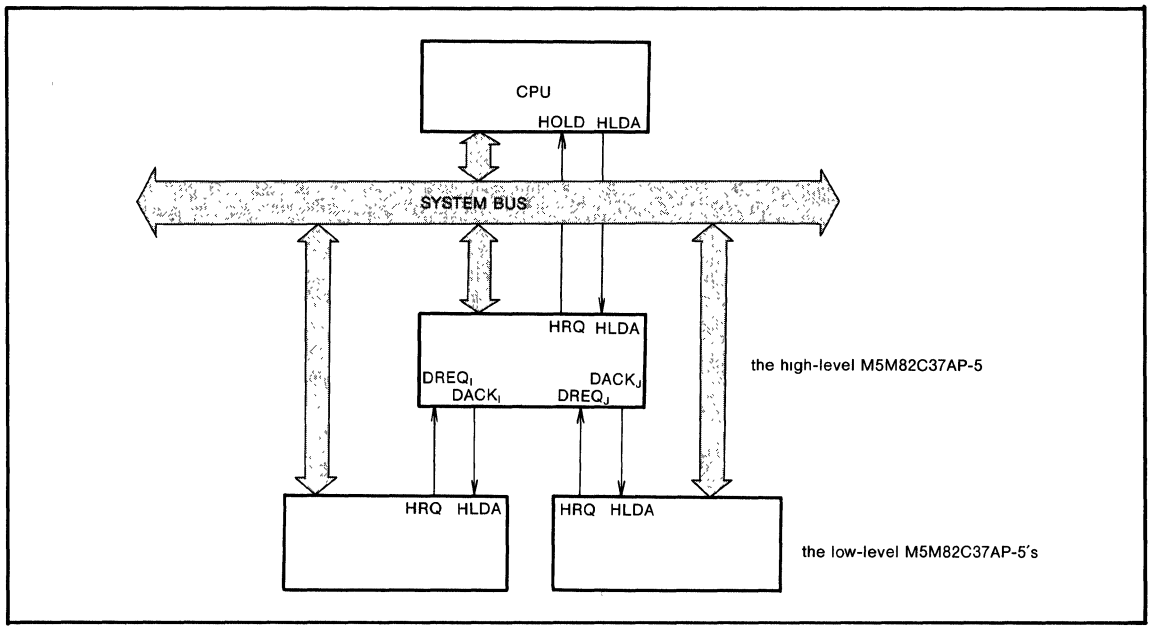


Fig.1 Example of a DMA system using a cascade connection

(5) **Auto initialization feature (mode regsiter bit 4=1)**
When bit 4 of the mode register is set to 1, the programmed channel enters the auto initialization mode. Auto initialization is performed when TC occurs and the contents of the base address/word count registers are loaded in the current address/word count registers. (The contents of the base address/word count registers are programmed to the same value as the current registers, at the same time.)

Note : If a channel is programmed for auto initialization the mask register bit for that channel is not set after TC. If it is not programmed for auto initialization, the mask register bit is set after TC, so the mask register bit must be reset to set this channel to DMA-enable

(6) **Extended write feafure (command register bit 5=1)**
In normal DMA operation, the write pulse $\overline{MEMW}$ (or $\overline{IOW}$) falls down to low-level in the S_3 state. But, if extended write is programmed, the write pulse falls at the S_2 state and the width can be extended for one clock period.

(7) **Compressed timing DMA feafure (command regsiter bit 3=1)**
In normal DMA, the transfer for one word consists of three or four states.
If the compressed timing DMA is programmed, the S_3 state is not executed and the one word transfer consists of two or three states. In this mode, the write output ($\overline{IOW}$, $\overline{MEMW}$) falls to low-level in the S_2 state as well as the read output ($\overline{IOR}$, $\overline{MEMR}$). In memory-to-memory DMA operation, the compressed timing assignment is ignored.

REGISTERS

The following is a description of the registers of M5M82C37AP-5.

(1) **Address registers**
The M5M82C37AP-5 has two 16-bit address registers for each DMA channel.
One is called the current address register. It holds the contents of the memory address at which DMA operation is performed and the contents are incremented (or decremented) at every word transfer. This register is read/write enabled when in the inactive state. The other is the base address register. This register is a write-only register and is written at the same time the current address register is programmed. The contents of the base address register are loaded into the current address register when the channel has reached TC if the channel is programmed in the auto initialize mode.
The registers of the M5M82C37AP-5 are read or written through an 8-bit data bus so the address register must be accessed twice, first the lower 8 bits, second the higher 8 bits. The M5M82C37AP-5 has a first/last flip-flop which is toggled when the 16-bit regsiter is accessed. It selects the lower or higher byte.

(2) **Word count registers**
The M5M82C37AP-5 has two 16-bit word count registers for each DMA channel.
One is called the current word count register. It holds the number of DMA transfer words, and the contents are decremented at the end of every word transfer. TC

occurs when the contents of the word counter about to decrement from 0000_{16} to $FFFF_{16}$.
The other is the base word counter, a write only register that is used for auto initialization like the base address register.
The read/write operation for the word count register is the same as for the address registers.

(3) **Mode registers**

The M5M82C37AP-5 has four 6-bit length registers to select the DMA modes and types for the 4 DMA channels. They are write only registers.
To program one of these registers, the channel selection is done by the 2 LSBs of the written data allowing all four registers to assigned at the same address. The other 6 bits are written to one of the four registers. The bit assignment is shown in fig. 2.

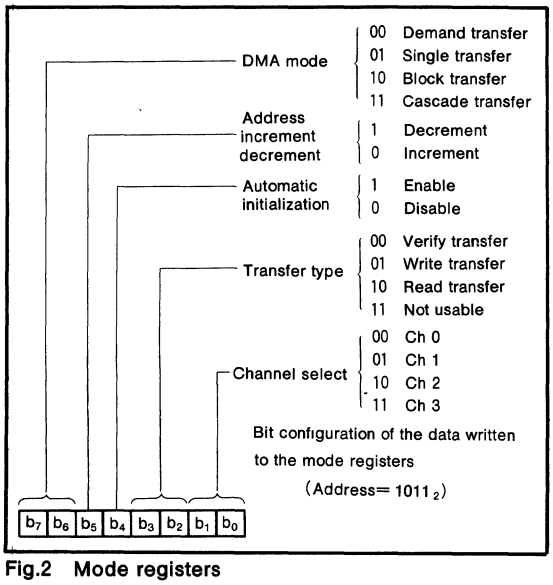


Fig.2 Mode registers

(4) **Command register**

This register is an 8-bit write only register used to define common operations for the four DMA channels. The bit assignment is shown in fig. 3.
Command regsiter is set 00_{16} by reset.

(5) **Mask register**

This register is a 4-bit register with one mask bit for each DMA channel.
The four bits of this regsiter can be programmed simultaneously (fig. 4) or can be set or reset 1-bit at a time (fig. 5). All bits can be cleared by the clear mask register command. (Address= 1110_2)
After reset, the 4 mask bits are all set to 1.

(6) **Request register**

This register is 4-bit register with one software request bit for each DMA channel.
One request bit can be set or reset at a time. (fig. 6)

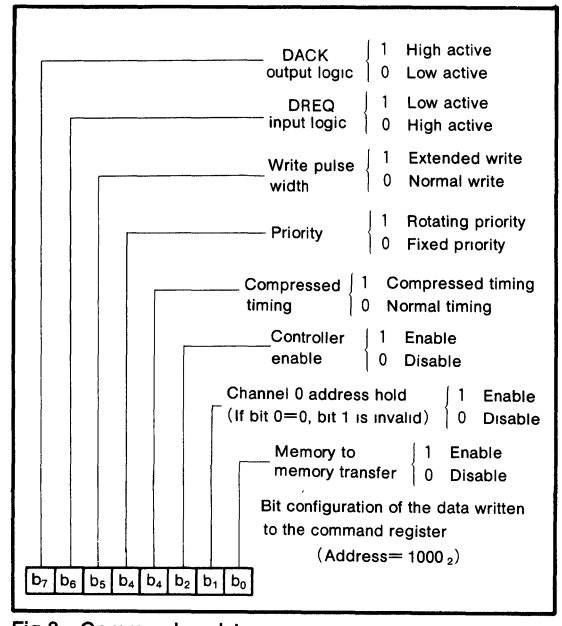


Fig.3 Command register

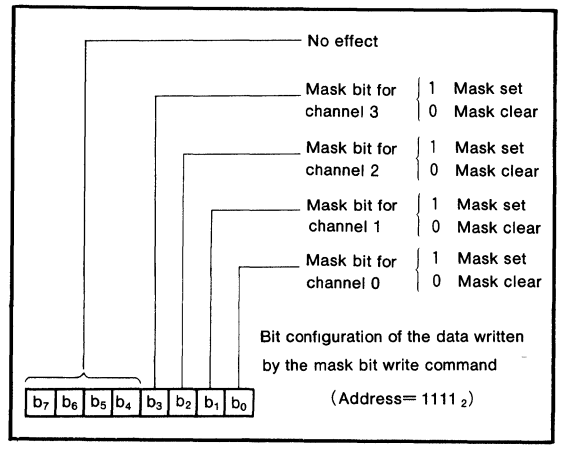


Fig.4 Mask register (write all bit)

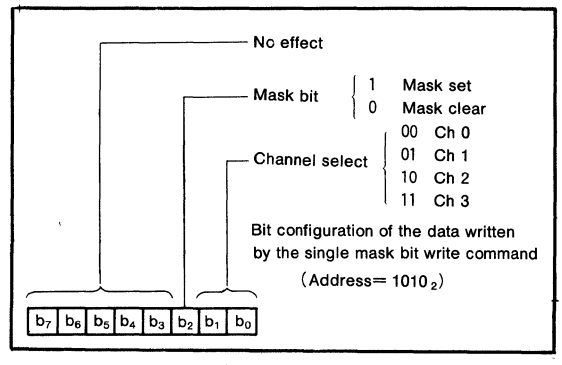


Fig.5 Mask register (write single bit)

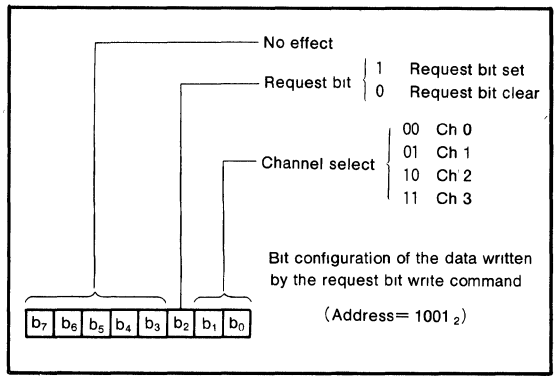


Fig.6 Request register

Note : All the request bits are reset after the DMA operation of one channel So, when the DMA is started by software request, other external DMA requests must be masked by setting all the mask register bits (Software requests are not masked by the mask register) All the request bits are set to 0 after reset.

(7) **Status register**

This register is an 8-bit read only register. The 4 MSBs show the status of the four DREQs. 1 means that the DREQ input is active.

The other 4 bits are the TC bits which are set to 1 when TC occurs. The lower 4 bits are reset after the status registers are read or after reset.

The relation between these bits and the channels is shown in fig. 7.

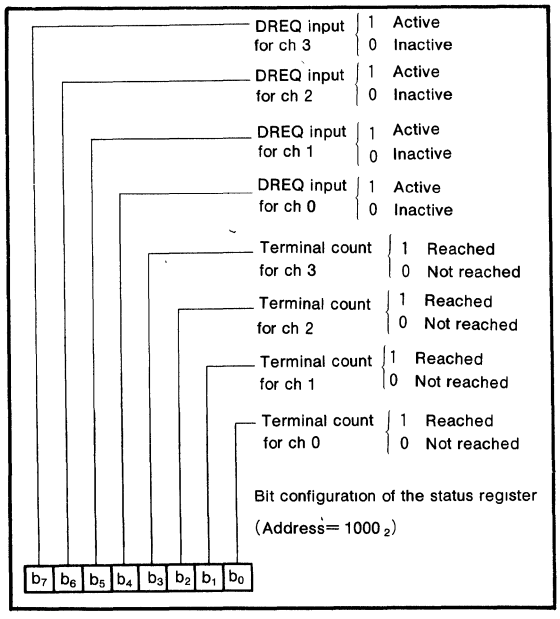


Fig.7 Status register

(8) **Temporary Register**

This register is an 8-bit read only register.

It is used to store temporary data read during the first part of the memory-to-memory DMA operation.

When the CPU reads this register, the register contents are the data which were transfered in memory-to-memory transfer DMA immediately prior to the CPU read.

PROGRAMMING

The registers in the M5M82C37AP-5 can be read or written when $\overline{CS}$ and HLDA inputs are low-level.

The address assignment is shown in Tables 2 and 3 Some of the write operations in these figures do not, in fact, write in any registers. They are called software commands. The following is a description of the software commands.

Clear first/last F/F

In reading or writing a 16-bit register, the higher and lower 8 bits are accessed separately. Selection is done by a first/last flip-flop which toggles when ever one of the 16-bit registers is accessed. This command clears the first/last flip-flop, so after this command is executed, the next access of the 16-bit register is begins at the lower 8 bits.

Master clear

This command executes a software reset.

Note : The following are the effects of the software reset for the M5M82C37AP-5

- Mask bits are set for all the DMA channels
- The command register is cleared to 00_{16} (Note that bit 2 is 0)
- The temporary register is cleared.
- The 4 TC bits of the status register are cleared
- The first/last flip-flop is reset.
- Software DMA request bits are cleared.

(When the hardware reset is performed, together with the above effects, DMA operation is terminated and the M5M82C37AP-5 returns to the S_I state.)

Clear mask register

This command clears all the mask bits and enable DMA for all the channels.

Table 2 Read operation with the M5M82C37AP-5

A_3	A_2	A_1	A_0	$\overline{CS}$	HLDA	$\overline{RD}$	First Last F/F	REGISTER READ
0	0	0	0	L	L	L	0	CH0 Current address register bit7~bit0
0	0	0	0	L	L	L	1	CH0 Current address register bit15~bit8
0	0	0	1	L	L	L	0	CH0 Current word count register bit7~bit0
0	0	0	1	L	L	L	1	CH0 Current word count register bit15~bit8
0	0	1	0	L	L	L	0	CH1 Current address register bit7~bit0
0	0	1	0	L	L	L	1	CH1 Current address register bit15~bit8
0	0	1	1	L	L	L	0	CH1 Current word count register bit7~bit0
0	0	1	1	L	L	L	1	CH1 Current word count register bit15~bit8
0	1	0	0	L	L	L	0	CH2 Current address register bit7~bit0
0	1	0	0	L	L	L	1	CH2 Current address register bit15~bit8
0	1	0	1	L	L	L	0	CH2 Current word count register bit7~bit0
0	1	0	1	L	L	L	1	CH2 Current word count register bit15~bit8
0	1	1	0	L	L	L	0	CH3 Current address register bit7~bit0
0	1	1	0	L	L	L	1	CH3 Current address register bit15~bit8
0	1	1	1	L	L	L	0	CH3 Current word count register bit7~bit0
0	1	1	1	L	L	L	1	CH3 Current word count register bit15~bit8
1	0	0	0	L	L	L	X	Status register
1	0	0	1	L	L	L	X	Invalid
1	0	1	0	L	L	L	X	Invalid
1	0	1	1	L	L	L	X	Invalid
1	1	0	0	L	L	L	X	Invalid
1	1	0	1	L	L	L	X	Temporary register
1	1	1	0	L	L	L	X	Invalid
1	1	1	1	L	L	L	X	Invalid
X	X	X	X	H	X	X	X	Read operation is not executed.
X	X	X	X	X	H	X	X	Read operation is not executed

Table 3 Write operation with the M5M82C37AP-5

A_3	A_2	A_1	A_0	$\overline{CS}$	HLDA	$\overline{WR}$	First Last F/F	REGISTER WRITTEN
0	0	0	0	L	L	L	0	CH0 base and current address register bit7~bit0
0	0	0	0	L	L	L	1	CH0 base and current address register bit15~bit8
0	0	0	1	L	L	L	0	CH0 base and current word count register bit7~bit0
0	0	0	1	L	L	L	1	CH0 base and current word count register bit15~bit8
0	0	1	0	L	L	L	0	CH1 base and current address register bit7~bit0
0	0	1	0	L	L	L	1	CH1 base and current address register bit15~bit8
0	0	1	1	L	L	L	0	CH1 base and current word count register bit7~bit0
0	0	1	1	L	L	L	1	CH1 base and current word count register bit15~bit8
0	1	0	0	L	L	L	0	CH2 base and current address register bit7~bit0
0	1	0	0	L	L	L	1	CH2 base and current address register bit15~bit8
0	1	0	1	L	L	L	0	CH2 base and current word count register bit7~bit0
0	1	0	1	L	L	L	1	CH2 base and current word count register bit15~bit8
0	1	1	0	L	L	L	0	CH3 base and current address register bit7~bit0
0	1	1	0	L	L	L	1	CH3 base and current address register bit15~bit8
0	1	1	1	L	L	L	0	CH3 base and current word count register bit7~bit0
0	1	1	1	L	L	L	1	CH3 base and current word count register bit15~bit8
1	0	0	0	L	L	L	X	Command register
1	0	0	1	L	L	L	X	Request register
1	0	1	0	L	L	L	X	Single mask bit write
1	0	1	1	L	L	L	X	Mode register
1	1	0	0	L	L	L	X	Clear first/last flip-flop software commands
1	1	0	1	L	L	L	X	Master clear software commands
1	1	1	0	L	L	L	X	Clear all mask register bits software commands
1	1	1	1	L	L	L	X	Write all mask bits software commands
X	X	X	X	H	X	X	X	Write is not executed.
X	X	X	X	X	H	X	X	Write is not executed.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3～7	V
V_I	Input voltage		−0.3～V_{CC}+0.3	V
V_O	Output voltage		−0.3～V_{CC}+0.3	V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current.	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current	2.5	mA
Topr	Operating free-air temperature range		−20～75	℃
Tstg	Storage temperature		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～75℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage(GND)		0		V

ELECTRICAL CHARCTERISTICS (T_a=−20～75℃, V_{CC}=5V±10%, V_{SS}=0V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−200μA	2.4			V
		I_{OH}=−20μA	4.4			
		I_{OH}=−100μA(HRQ only)	3.3			
V_{OL}	Low-level output voltage	I_{OL}=2.0mA(data bus) I_{OL}=3.2mA(other outputs)			0.45	V
I_I	Input current	V_I=0V, V_{CC}	−10		+10	μA
I_{OZ}	Off-state output current	V_O=0V～V_{CC}	−10		+10	μA
I_{CC}	Supply current from V_{CC} (operating)	V_I=0V, V_{CC}, f_{CLK}=1/$t_C(\phi)$min.			15	mA
I_{CCS}	Supply current from V_{CC} (stand by)	V_I=0V, V_{CC}			10	μA
C_I	Input terminal capacitance	V_{IL}=V_{SS}, f=1MHz, 25mVrms, T_a=25℃			10	pF
$C_{I/O}$	Input/output terminal capacitance	$V_{I/OL}$=V_{SS}, f=1MHz, 25mVrms, T_a=25℃			20	pF

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V unless otherwise noted)

1. SLAVE MODE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-R)}$ $t_{su(A-R)}$	Address setup time before read		50			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time before write		130			ns
$t_{su(A-W)}$	Address setup time before write		130			ns
$t_{su(DQ-W)}$	Data setup time before write		100			ns
$t_{h(R-CS)}$ $t_{h(R-A)}$	Address hold time after read		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time after write		20			ns
$t_{h(W-A)}$	Address hold after write		20			ns
$t_{h(W-DQ)}$	Data hold after write		30			ns
$t_{w(R)}$	Read pulse width		200			ns
$t_{w(W)}$	Write pulse width		160			ns
$t_{w(RESET)}$	Reset pulse width		300			ns
$t_{su(VCC-RESET)}$	V_{CC} setup time before to reset		500			ns
$t_{su(RESET-R)}$ $t_{su(RESET-W)}$	Reset setup time before read Reset setup time before Write		$2t_{C(\phi)}$			ns

2. DMA MODE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\phi)}$	Clock high-level pulse width		80			ns
$t_{w(\overline{\phi})}$	Clock low-level pulse width		68			ns
$t_{C(\phi)}$	Clock period		200		DC	ns
$t_{su(EOP-\phi)}$	External $\overline{EOP}$ setup time before clock		40			ns
$t_{w(EOP)}$	External $\overline{EOP}$ pulse width		220			ns
$t_{su(DREQ-\phi)}$	DREQ setup time before clock		0			ns
$t_{su(READY-\phi)}$	READY setup time before clock		60			ns
$t_{h(\phi-READY)}$	READY hold time before clock		20			ns
$t_{su(HLDA-\phi)}$	HLDA setup time before clock		75			ns
$t_{su(DQ-MEMR)}$	Data setup time before $\overline{MEMR}$		170			ns
$t_{h(MEMR-DQ)}$	Data hold time after $\overline{MEMR}$		0			ns

SWITCHING CHARACTERISTIC (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V unless otherwise noted)

1. SLAVE MODE

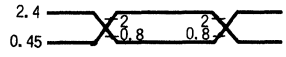
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Data enable time after read	C_L=150pF			140	ns
$t_{PVZ(R-DQ)}$	Data disable time after read		0		70	ns
$t_{PZV(A-DQ)}$	Address access time				250	ns

2. DMA MODE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PLH(\phi-AEN)}$	Propagation time from clock to AEN	C_L=150pF			200	ns
$t_{PHL(\phi-AEN)}$	Propagation time from clock to AEN				130	ns
$t_{PZV(\phi-A)}$	Propagation time from clock to address active				170	ns
$t_{PHL(\phi-A)}$	Propagation time from clock to address stable				170	ns
$t_{PVZ(\phi-A)}$	Propagation time from clock to address floating				90	ns
$t_{PZV(\phi-DQ)}$	Propagation time from clock to data bus				200	ns
$t_{PVZ(\phi-DQ)}$	Propagation time from clock to data bus				170	ns
$t_{PLH(\phi-ADSTB)}$	Propagation time from clock to ADSTB				130	ns
$t_{PHL(\phi-ADSTB)}$	Propagation time from clock to ADSTB				90	ns
$t_{SU(DQ-ADSTB)}$	Data output setup time before ADSTB		100			ns
$t_{h(ADSTB-DQ)}$	Data output hold time before ADSTB		30			ns
$t_{PZV(\phi-R)}$ $t_{PZV(\phi-W)}$	Propagation time from clock to read or write active				150	ns
$t_{PHL(\phi-R)}$ $t_{PHL(\phi-W)}$	Propagation time from clock to read or write				190	ns
$t_{PLH(\phi-R)}$	Propagation time from clock to read				190	ns
$t_{PLH(\phi-W)}$	Propagation time from clock to write				130	ns
$t_{PVZ(\phi-R)}$ $t_{PVZ(\phi-W)}$	Propagation time from clock to read or write floating				120	ns
$t_{h(R-A)}$	Address output hold time after read		$t_{C(\phi)}$−100			ns
$t_{h(W-A)}$	Address output hold time after write		$t_{C(\phi)}$−50			ns
$t_{SU(DQ-MEMW)}$	Data output setup time before $\overline{MEMW}$		125			ns
$t_{h(MEMW-DQ)}$	Data output hold time after $\overline{MEMW}$		10			ns
$t_{PHL(\phi-DACK)}$ $t_{PLH(\phi-DACK)}$	Propagation time from clock to DACK				170	ns
$t_{PHL(\phi-EOP)}$	Propagation time from clock to $\overline{EOP}$				170	ns
$t_{PLH(\phi-EOP)}$	Propagation time from clock to $\overline{EOP}$				170	ns
$t_{PLH(\phi-HRQ)}$ $t_{PHL(\phi-HRQ)}$	Propagation time from clock to HRQ				120	ns

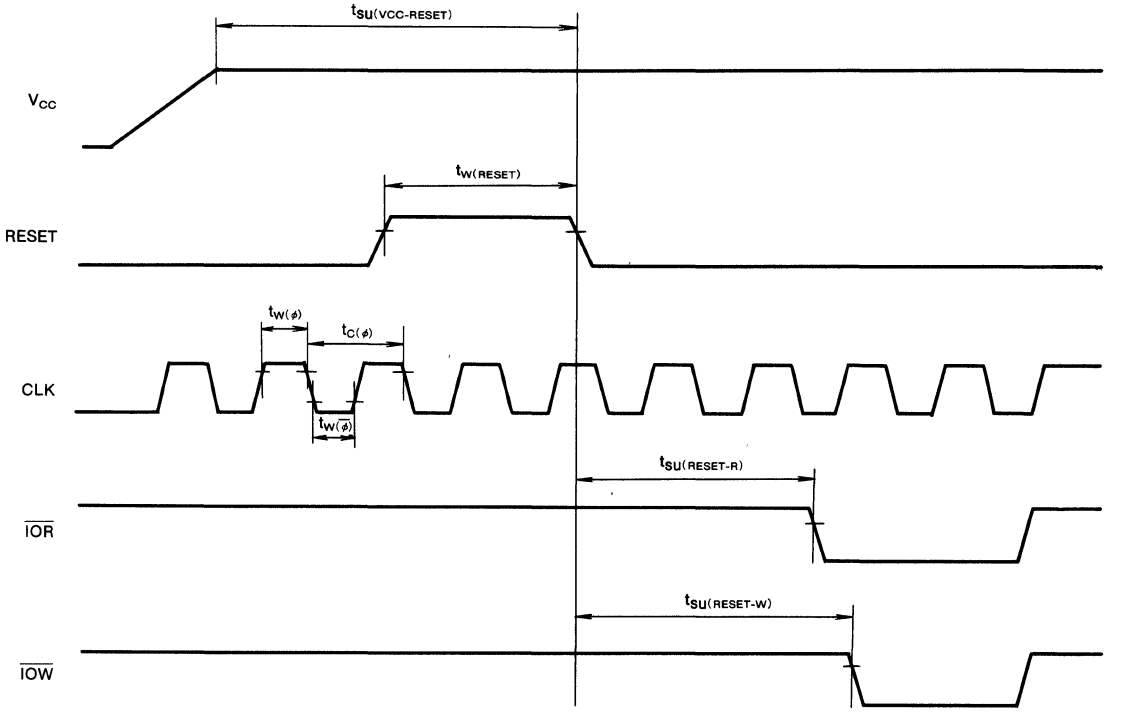
Note : A.C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	10ns
Input pulse fall time	10ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V

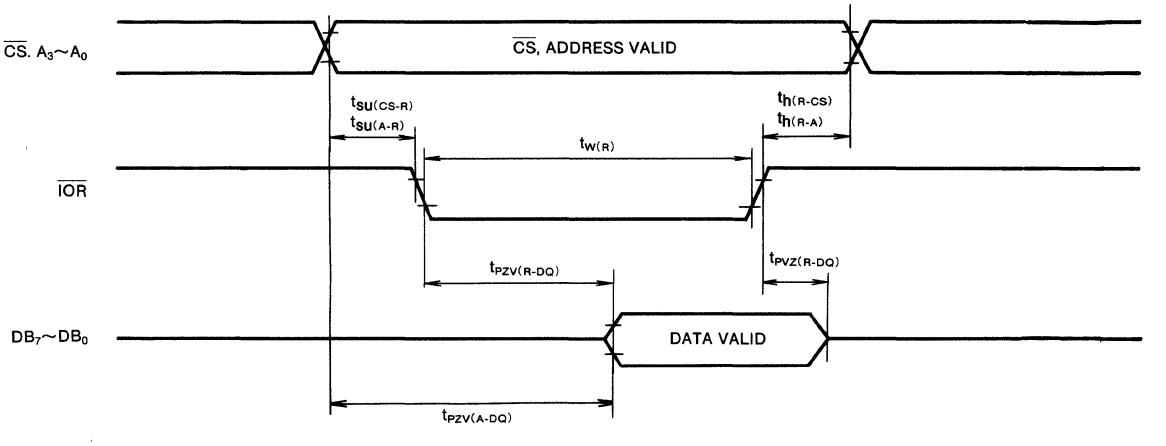


TIMING DIAGRAMS

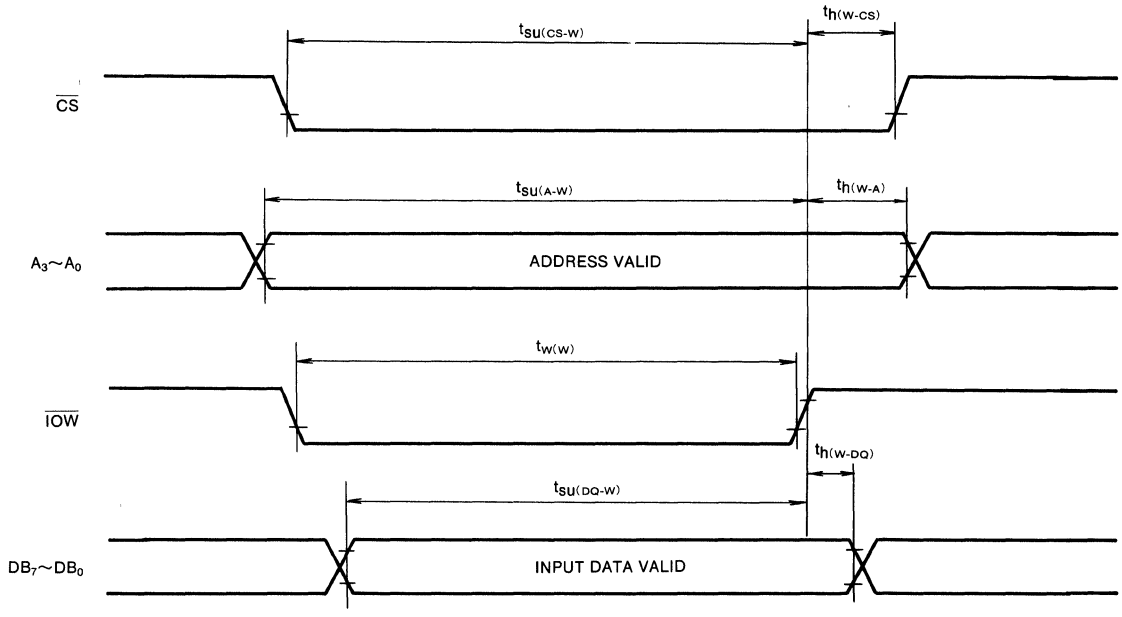
Reset timing



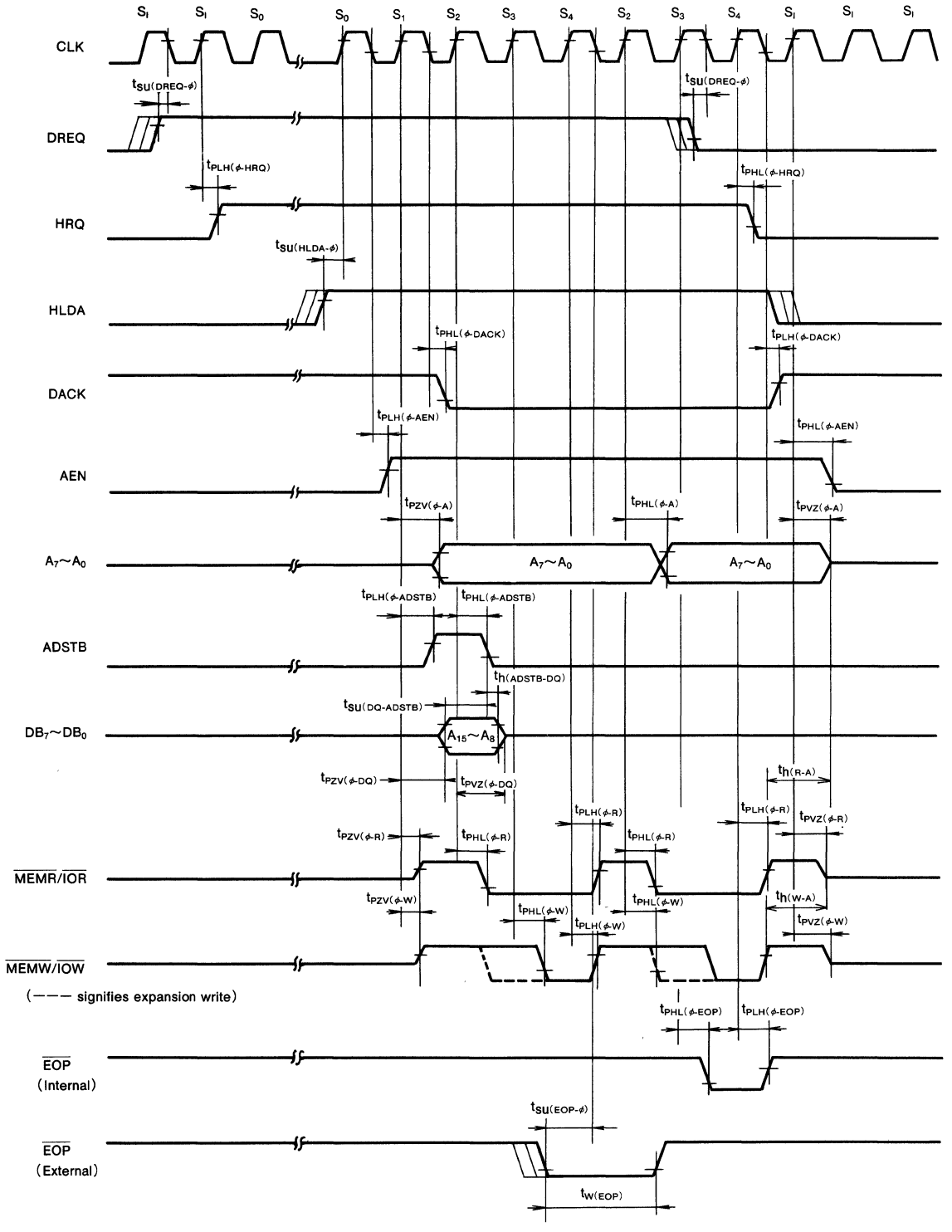
Slave mode timing (READ)



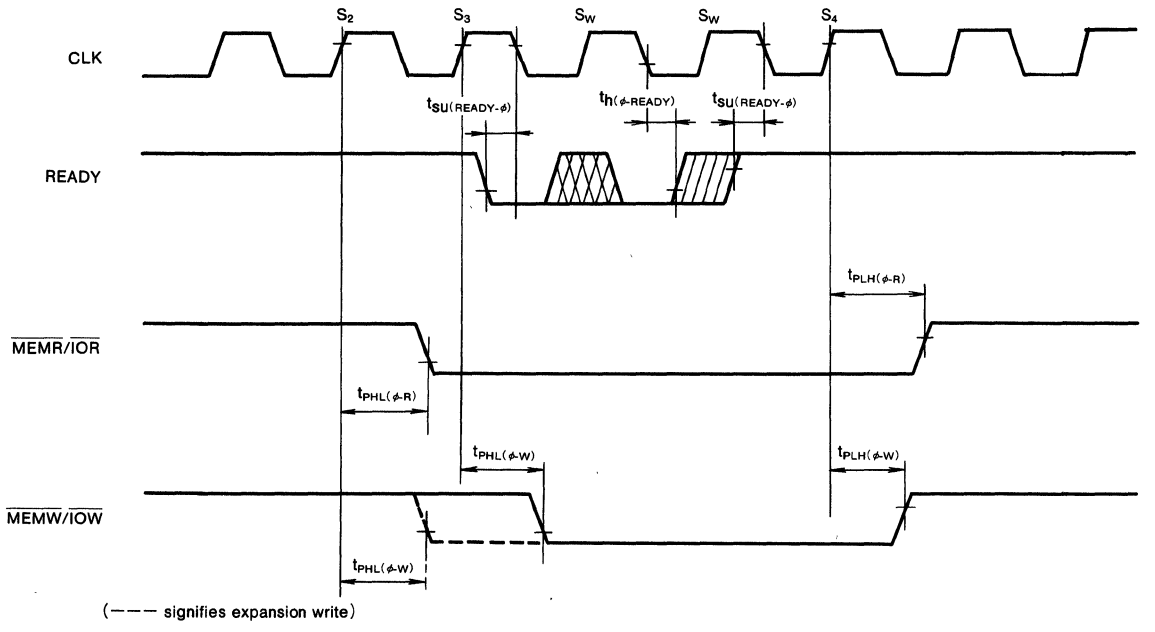
Slave mode timing (WRITE)



DMA transmit timing

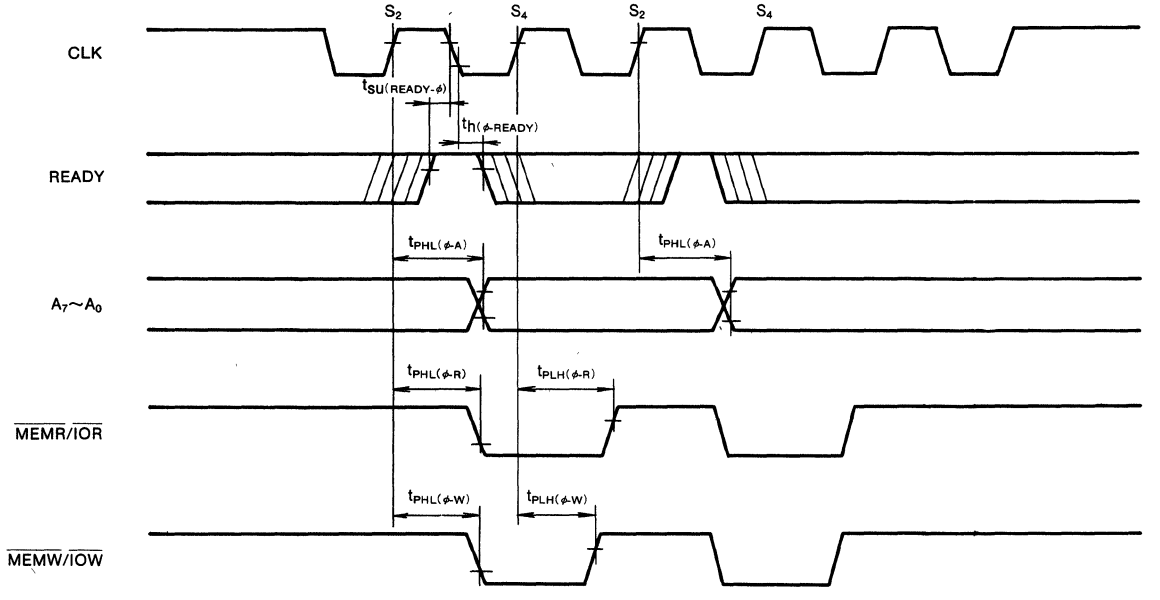


READY input timing

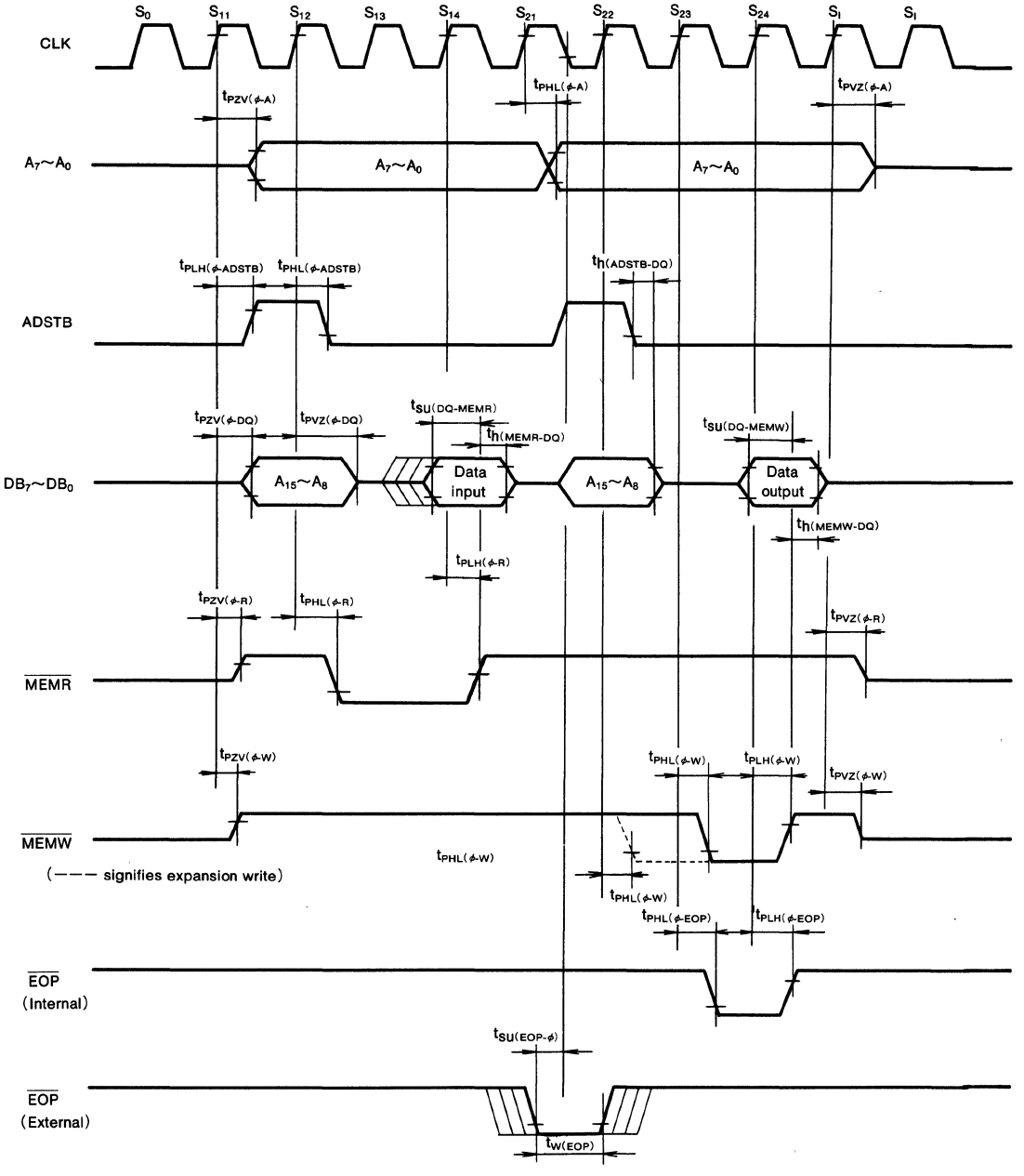


(——— signifies expansion write)

Compressed timing



Inter-memory transmission



M5M82C51AP/FP/J

CMOS PROGRAMMABLE COMMUNICATION INTERFACE

DESCRIPTION

The M5M82C51AP is a universal synchronous/asynchronous receiver/transmitter (USART) IC chip designed for data communications use. It is produced using the silicon-gate CMOS process and is mainly used in combination with 8-bit microprocessors. It is housed in a 28-pin plastic molded DIP.

And preparatory for surface equipment M5M82C51AFP (SOP) and M5M82C51AJ(PLCC).

FEATURES

- Single 5V supply voltage
- TTL compatible
- Synchronous and asynchronous operation
  - Synchronous:
    - 5~8-bit characters
    - Internal or external synchronization
    - Automatic SYNC character insertion
  - Asynchronous system:
    - 5~8-bit characters
    - Clock rate—1, 16 or 64 times the baud rate
    - 1, 1½, or 2 stop bits
    - False-start-bit detection
    - Automatic break-state detection
- Baud rate: DC~64K-baud
- Full duplex, double-buffered transmitter/receiver
- Error detection: parity, overrun, and framing

APPLICATION

Modem control of data communications using microcomputers

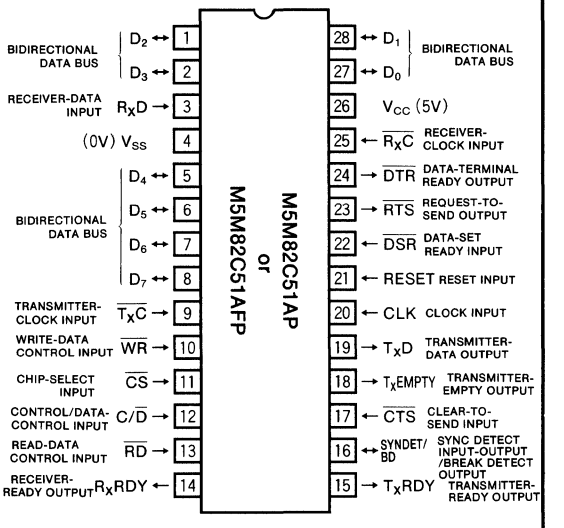
Control of CRT, TTY and other terminal equipment

FUNCTION

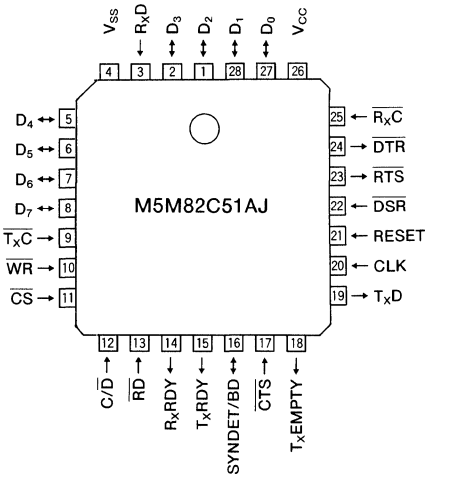
The M5M82C51AP is used in the peripheral circuits of a CPU. It permits assignments, by means of software, of operations in all the currently used serial-data transfer systems.

The M5M82C51AP receives parallel-format data from the CPU, converts it into a serial format, and then transmits via the T_XD pin. It also receives data sent in via the R_XD pin from the external circuit, and converts it into a parallel format for sending to the CPU. On receipt of parallel-format data for transmission from the CPU or serial data for the CPU from external devices, the M5M82C51AP informs the CPU using the T_XRDY or R_XRDY pin. In addition, the CPU can read the M5M82C51AP status at any time. The M5M82C51AP can detect the data received for errors and inform the CPU of the presence of errors as status information. Errors include parity, overrun and frame errors.

PIN CONFIGURATION (TOP VIEW)

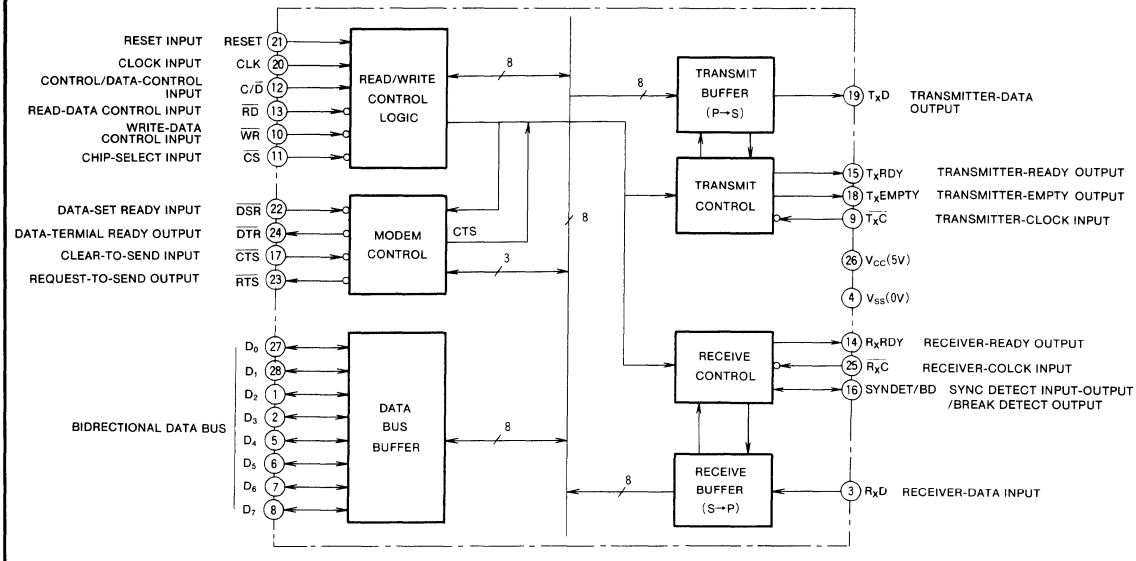


Outline 28P4 (M5M82C51AP)
28P2W (M5M82C51AFP)



Outline 28P0

BLOCK DIAGRAM



OPERATION

The M5M82C51AP interfaces with the system bus as shown in Fig.1, positioned between the CPU and the modem or terminal equipment, and offers all the functions required for data communication.

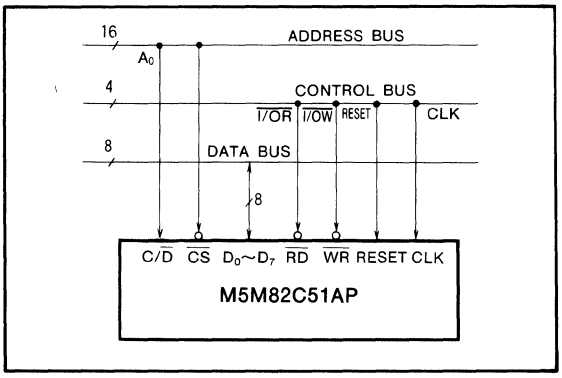


Fig. 1 M5M82C51AP interface to CPU system bus

When using the M5M82C51AP, it is necessary to program, as the initial setting, assignments for synchronous/asynchronous mode selection, baud rate, character length, parity check, and even/odd parity selection in accordance with the communication system used. Once programming is completed, functions appropriate to the communication system can be carried out continuously.

When initial setting of the USART is completed, data communication becomes possible. Though the receiver is always in the enable state, the transmitter is placed in the transmitter-enable state (T_XEN) by a command instruction, and the application of a low-level signal to the $\overline{CTS}$ pin prompts data-transfer start-up. Until this condition is satisfied, transmission is not executed. On receiving data, the receiver informs the CPU that reading for the receiver data in the USART by the CPU has become possible (the R_XRDY terminal has turned to high-level). Since data reception and the entry of the CPU into the data-readable state are output as status information, the CPU can access USART status without accessing the R_XRDY terminal.

During receiving operation, the USART checks errors and gives out status information. There are three types of errors: parity, overrun, and frame. Even though an error occurs, the USART continues its operations, and the error state is retained until error reset (ER) is effected by a command instruction. The M5M82C51AP access methods are listed in Table 1.

Table 1 M5M82C51AP Access Methods

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Function
L	L	H	L	Data bus ← Data in USART
L	H	L	L	USART ← Data bus
H	L	H	L	Data bus ← Status
H	H	L	L	Control ← Data bus
X	H	H	L	3-State ← Data bus
X	X	X	H	3-State ← Data bus

Read/Write Control Logic

This logic consists of a control word register and command word register. It receives signals from the CPU control bus and generates internal-control signals for the elements.

Modem Control Circuit

This is a general-purpose control-signal circuit designed to simplify the interface to the modem. Four types of control signal are available: output signals $\overline{DTR}$ and $\overline{RTS}$ are controlled by command instructions, input signal $\overline{DSR}$ is given to the CPU as status information and input signal $\overline{CTS}$ controls direct transmission.

Data-Bus Buffer

This is an 8-bit 3-state bidirectional bus through which control words, command words, status information, and transfer data are transferred. Fig. 2 shows the structure of the data-bus buffer.

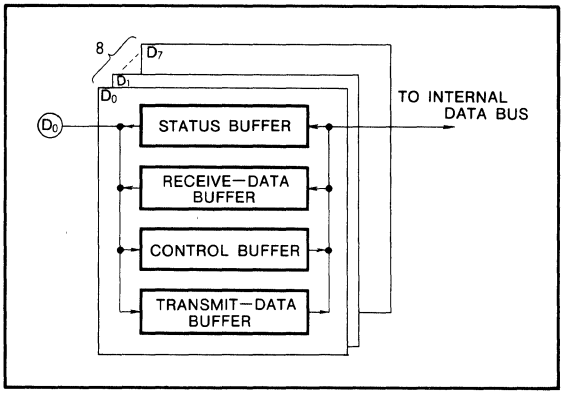


Fig. 2 Data-bus buffer structure

Transmit Buffer

This buffer converts parallel-format data given to the data-bus buffer in to serial data with addition of a start bit, stop bits and a parity bit, and sends out the converted data through the T_XD pin based on the control signal.

Transmit-Control Circuit

This circuit carries out all the controls required for serial data transmission. It controls transmitter data and outputs the signals required by external devices in accordance with the instructions of the read/write control logic.

Receive Control Circuit

This circuit offers all the controls required for normal reception of the input serial data. It controls receiver data and outputs signals for the external devices in accordace with the instructions of the read/write control logic.

Receive Buffer

This buffer converts serial data given via the R_XD pin into a parallel format, checks the bits and characters in accordance with the communication format designated by mode setting, and transfers the assembled characters to the CPU via the data-bus buffer.

Receiver-Data Input (R_XD)

Serial characters sent from another device are input to this pin and converted to a parallel-character format to serve as data for the CPU. Unless the high-level state is detected after a chip-master reset procedure (this resetting is carried out to prevent spurious operation such as that due to faulty connection of the R_XD to the line in a break state), the serial characters are not received. This applies to only the asynchronous mode. When the R_XD line enters the low-level state instantaneously because of noise, etc, the mis-start prevention function starts working. That is, the start bit is detected by its falling edge but in order to make sure that it is the correct start bit, the R_XD line is strobed at the middle of the start bit to reconfirm the low-level state. If it is found to be high-level a faulty-start judgment is made.

Transmitter-Clock Input ($\overline{T_XC}$)

This clock controls the baud rate for character transmission from the T_XD pin. Serial data is shifted by the falling edge of the $\overline{T_XC}$ signal. In the synchronous mode, the $\overline{T_XC}$ frequency is equal to the actual baud rate. In the asynchronous mode, the frequency is specified as 1, 16, or 64 times the baud rate by the mode setting.

Example When the baud rate is 110 bauds:

$\overline{T_XC}$=110Hz(1X)

$\overline{T_XC}$=1.76kHz(16X)

$\overline{T_XC}$=7.04kHz(64X)

Write-Data Control Input ($\overline{WR}$)

Data and control words output from the CPU by the low-level input are written in the M5M82C51AP. This terminal is usually used in a form connected with the control bus $\overline{I/OW}$ of the CPU.

Chip-Select Input ($\overline{CS}$)

This is a device-select signal that enables the USART by a low-level input. Usually, it is connected to the address bus directly or via the decoder. When this signal is in the high-level state, the M5M82C51AP is disabled.

Control/Data Control Input (C/$\overline{D}$)

This signal shows whether the information on the USART data bus is in the form of data characters or control words, or in the form of status information, in accordance with the $\overline{RD}$ and $\overline{WR}$ inputs while the CPU is accessing the M5M82C51AP. The high-level identifies control words or status information, and the low-level, data characters.

Read-Data Control Input ($\overline{RD}$)

Receiver data and status information are output from the CPU by a low-level input for the CPU data bus.

Receiver-Ready Output (R_XRDY)

This signal indicates that the received characters have entered the receiver buffer, and further, the receiver-data buffer in the data-bus buffer shown in Fig. 2. It is possible to confirm the R_XRDY status by using this signal as an interruption signal for the CPU or by allowing the CPU to read the D_1 bit of the status information by polling. The R_XRDY is automatically reset when a character is read by the CPU. Even in the break state in which the R_XD line is held at low-level, the R_XRDY remains active. It can be masked by making the $R_XE(D_2)$ of the command instruction 0.

Transmitter-Ready Output (T_XRDY)

This signal shows that the data is ready for transmission. It is possible to confirm the status of serial-data transmission by using it as an interruption signal for the CPU or by allowing the CPU to read the D_0 bit of the status information by polling. Since the T_XRDY signal shows that the data buffer is empty, it is automatically reset when a transmission character is loaded by the CPU. The T_XRDY bit of the status information means that the transmit-data buffer shown in Fig. 2 has become empty, while the T_XRDY pin enters the high-level state only when the transmit-data buffer is empty, T_XEN equals 1, and a low-level input has been applied to the $\overline{CTS}$ pin.

Status (D_0): When transmit-data buffer (TDB) is empty, it becomes 1.

T_XRDY terminal: When (TDB is empty) · ($T_XEN = 1$) · (CTS = "L") = "H" or resetting, it becomes active.

Sync Detect Input-Output/Break Detect Output (SYNDET/BD)

In the synchronous mode this pin is used for input and output operations. When it is specified for the internal synchronous mode by mode setting, this pin works as an output terminal. It enters the high-level state when a SYNC character is received through the R_XD pin. If the M5M82C51AP has been programmed for double SYNC characters (bi-sync), a high-level is entered in the middle of the last bit of the second SYNC character. This signal is automatically reset by reading the status information.

On designation of the M5M82C51AP to the external synchronous mode, this pin begins to serve for input operations. Applying a high-level signal to this pin prompts the M5M82C51AP to begin assembling data characters at the next rising edge of the $\overline{R_XC}$. For the width of a high-level signal to be input, a minimum $\overline{R_XC}$ period is required.

Designation of the asynchronous mode causes this pin to function as a BD (output) pin. When the start, data, and parity bits and stop bits are all 0 for two characters period, a high-level is entered. The BD (break detect) signal can also be read as the D_6 bit of the status information. This signal is reset by resetting the chip master or by the R_XD line's recovering the high-level state.

Clear-To-Send Input ($\overline{CTS}$)

When the T_XEN bit (D_0) of the command instruction has been set to 1 and the $\overline{CTS}$ input is low-level serial data is sent out from the T_XD pin. Usually this is used as a clear-to-send signal for the modem

Note: CTS indicates the modem status as follows:
ON means data transmission is possible;
OFF means data transmission is impossible.

Transmitter-Empty Output (T_XEMPTY)

When no transmisison characters are left in the transmit buffer, this pin enters the high-level state. In the asynchronous mode, the following transmission character is shifted to the transmit buffer when it is loaded from the CPU. Thus, it is automatically reset. In the synchronous mode, a SYNC character is loaded automatically on the transmit buffer when no transfer-data characters are left. In this case, however, the T_XEMPTY does not enter the low-level state when a SYNC character has been sent out, since T_XEMPTY ="H" denotes the state in which there is no transfer character and one or two SYNC characters are being transferred or the state in which a SYNC character is being transferred as a filler. T_XEMPTY is unrelated to the T_XEN bit of the command instruction.

Transmission-Data Output (T_XD)

Parallel-format transmission characters loaded on the M5M82C51AP by the CPU are assembled into the format designated by the mode instruction and sent in serial-data form via the T_XD pin. Data is output, however, only in cases where the D_0 bit (T_XEN) of the command instruction is 1 and the $\overline{CTS}$ terminal is in the low-level state. Once reset, this pin is kept at the mark status (high-level) until the first character is sent.

Clock Input (CLK)

This system-clock input is required for internal-timing generation and is usually connected to the clock-output (CLK) pin of the M5L8085AP. Although there is no direct relation with the data-transfer baud rate, the clock-input (CLK) frequency is more than 30 times the $\overline{T_XC}$ or $\overline{R_XC}$ input frequency in the case of the synchronous system and more than 4.5 times in the case of the asynchronous system.

Reset Input (RESET)

Once the USART is shifted to the idle mode by a high-level input, this state continues until a new control word is set Since this is a master reset, it is always necessary to load a control word following the reset process. The reset input requires a minimum 6-clock pulse width.

Data-Set Ready Input ($\overline{DSR}$)

This is a general-purpose input signal, but is usually used as a data-set ready signal to test modem status. Its status can be known from the status reading process. The D_7 bit of the status information equals 1 when the $\overline{DSR}$ pin is in the low-level state, and 0 when in the high-level state.

$\overline{DSR}$="L"→D_7 bit of status information=1
$\overline{DSR}$="H"→D_7 bit of status information=0

Note. DSR indicates modem status as follows:
ON means the modem can transmit and receive;
OFF means it cannot.

Request-To-Send Output ($\overline{RTS}$)

This is a general-purpose output signal but is used as a request-to-send signal for the modem. The $\overline{RTS}$ terminal is controlled by the D_5 bit of the command instruction. When D_5 is equal to 1, $\overline{RTS}$="L", and when D_5 is 0, $\overline{RTS}$="H".

Command register D_5=1→$\overline{RTS}$="L"
Command register D_5=0→$\overline{RTS}$="H"

Note: RTS controls the modem transmission carrier as follows:
ON means carrier dispatch;
OFF means carrier stop.

Data-Terminal Ready Output ($\overline{DTR}$)

This is a general-purpose output signal, but is usually used as a data-terminal ready or rate-select signal to the modem. The $\overline{DTR}$ pin is controlled by the D_1 bit of the command instruction; if D_1=1, $\overline{DTR}$="L", and if D_1=0, $\overline{DTR}$="H".

D_1 of the command register=1→$\overline{DTR}$="L"
D_1 of the command register=0→$\overline{DTR}$="H"

Receiver-Clock Input ($\overline{R_XC}$)

This clock signal controls the baud rate for the sending in of characters via the $\overline{R_XD}$ pin. The data is shifted in by the rising edge of the $\overline{R_XC}$ signal. In the synchronous mode, the $\overline{R_XC}$ frequency is equal to the actual baud rate. In the asynchronous mode, the frequency is specified as 1, 16, or 64 times the baud rate by mode setting. This relationship is parallel to that of $\overline{T_XC}$, and in usual communication-line systems the transmission and reception baud rates are equal. The $\overline{T_XC}$ and $\overline{R_XC}$ terminals are, therefore, used connected to the same baud-rate generator.

PROGRAMMING

It is necessary for the M5M82C51AP to have the control word loaded by the CPU prior to data transfer. This must always be done following any resetting operation (by external RESET pin or command instruction IR). There are two types of control words: mode instructions specifying general operations required for communications and command instructions to control the M5M82C51AP actual operations.

Following the resetting operation, a mode instruction must be set first. This instruction sets the synchronous or asynchronous system to be used. In the sysnchronous system, a SYNC character is loaded from the CPU. In the case of the bi-sync system, however, a second SYNC character must be loaded in succession.

Loading a command instruction makes data transfer possible. This operation after resetting must be carried out for initializing the M5M82C51AP. The USART command instruction contains an internal-reset IR instruction (D_6bit) that makes it possible to return the M5M82C51AP to its reset state. The initialization flowchart is shown in Fig. 3 and the mode-instruction and command-instruction formats are shown in Figs. 4 and 5.

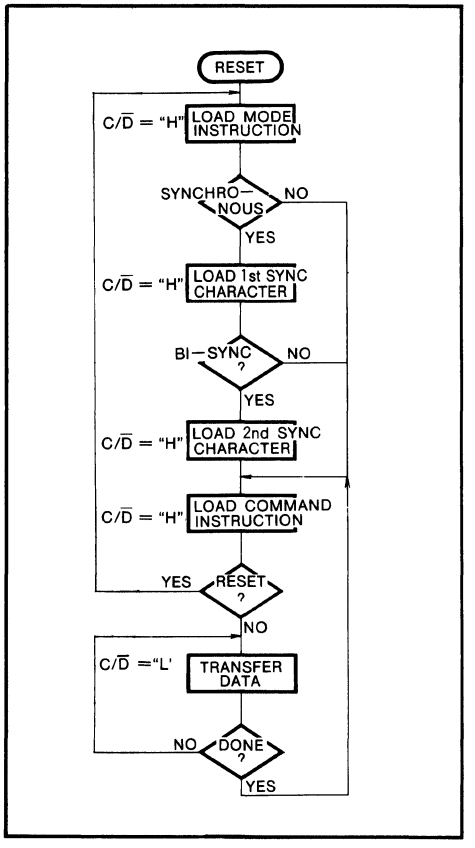


Fig. 3 Initialization flow chart

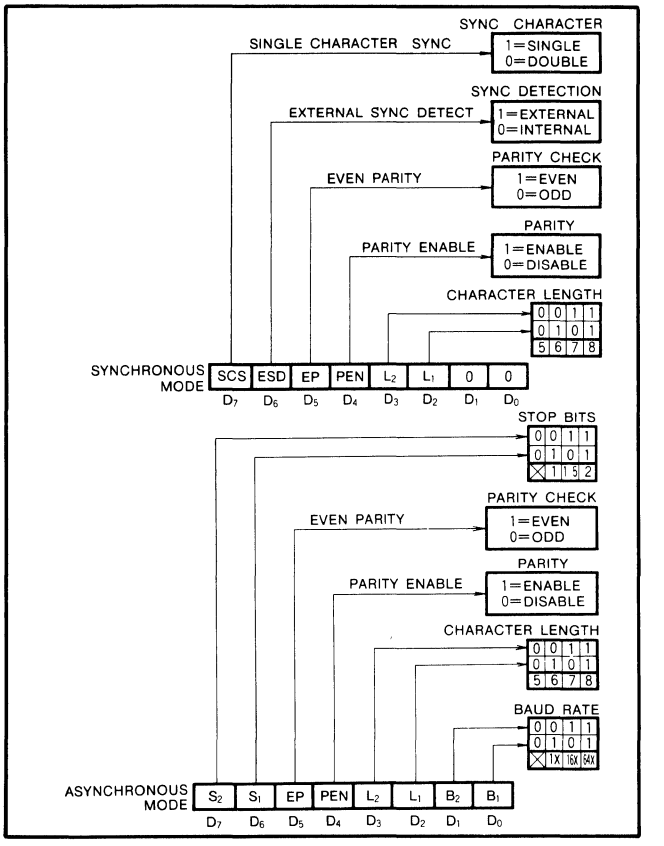


Fig. 4 Mode-instruction format ($C/\overline{D}$="H" $\overline{WR}$="L")

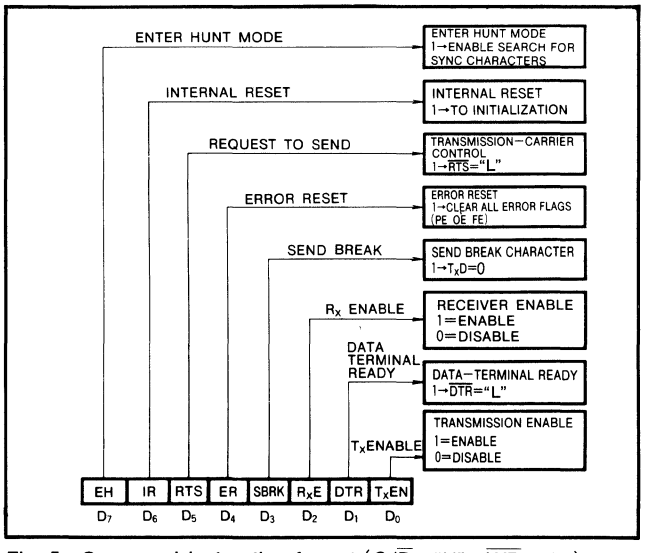


Fig. 5 Command-instruction format ($C/\overline{D}$="H" $\overline{WR}$="L")

Asynchronous Transmission Mode

When data characters are loaded on the M5M82C51AP after initial setting, the USART automatically adds a start bit (0), an odd or even parity bit specified by the mode instruction during initialization, and a specified number of stop bits (1). After that, the assembled data characters are transferred as serial data via the T_XD pin, if transfer is enabled ($T_XEN=1 \cdot \overline{CTS}=$"L"). In this case, the transfer data (baud rate) is shifted by the mode instruction at a rate of 1X, 1/16X, or 1/64X the $\overline{T_XC}$ period.

If the data characters are not loaded on the M5M82C51AP, the T_XD pin enters a mark state ("H"). When SBRK is programmed by the command instruction, break characters (0) are output continuously through the T_XD pin

Asynchronous Reception Mode

The R_XD line usually starts operations in a mark state ("H"), triggered by the falling edge of a low-level pulse when it comes to this line. This signal is again strobe at the middle of the bit to confirm that it is a perfect start bit. The detection of a second low-level indicates the validity of the start bit (again strobe is carried out only in the case of 16X and 64X). After that, the bit counter inside the M5M82C51AP starts operating; each bit of the serial information on the R_XD line is shifted in by the rising edge of $\overline{R_XC}$, and the data bit, parity bit (when necessary), and stop bit are sampled at the middle position.

The occurrence of a parity error causes the setting of a parity-error flag. If the stop bit is 0, a frame error flag is set. Attention should be paid to the fact that the receiver requires only one stop bit even though the program has designated 1.5 or 2 stop bits.

Reception up to the stop bit means reception of a complete character. This character is then transferred to the receiver-data buffer shown in Fig.2, and the R_XRDY becomes active. In cases where this character is not read by the CPU and where the next character is transferred to the receiver-data buffer, the preceding character is destroyed and an overrun-error flag is set.

These error flags can be read as the M5M82C51AP status information. The occurrence of an error does not stop USART operations. The error flags are cleared by the ER (D_4 bit) of the command instruction.

The asynchronous-system transfer formats are shown in Figs. 6 and 7.

Synchronous Transmission Mode

In this mode the T_XD pin remains in the high-level state until initial setting by the CPU is completed. After initialization, the state of $\overline{CTS}=$"L" and $T_XEN=1$ enables serial transmission of characters through the T_XD pin. Then, data characters are sent out and shifted by the falling edge of the $\overline{T_XC}$ signal. The transmission rate equals the $\overline{T_XC}$ rate.

Thus, once data-character transfer starts, it must continue through the T_XD pin at the same rate as that of $\overline{T_XC}$. Unless data characters are provided from the CPU before the transmitter buffer becomes empty, one or two SYNC characters are automatically output from the T_XD pin. In this case, it should be noted that the T_XEMPTY pin enters the high-level state when there are no data characters left in the M5M82C51AP to be transferred, and that the low-level state is not entered until the USART is provided with the next data character from the CPU. Care should also be taken over the fact that merely setting a command instruction does not effect SYNC character insertion, because the SYNC character insertion is enabled after sending out the first data character.

In this mode, too, break characters are sent out in succession from the T_XD pin when SBRK is designated ($D_3=1$) by a command instruction.

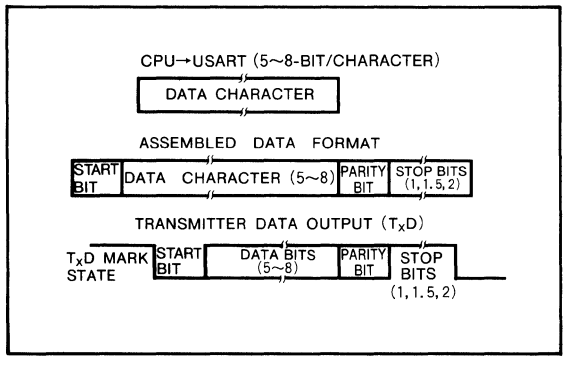
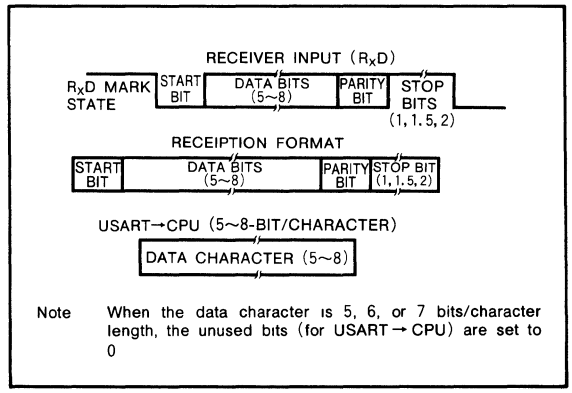


Fig. 6 Asynchronous transmission format I (transmission)



Note When the data character is 5, 6, or 7 bits/character length, the unused bits (for USART → CPU) are set to 0

Fig. 7 Asynchronous transmission format II (reception)

Synchronous Reception Mode

Character synchronization in this mode is carried out internally or externally by initial-setting designation.

Programming in the internal synchronous mode requires that an EH instruction ($D_7=1$, enter hunt mode) is included in the first command instruction. Data on the R_XD pin is sampled by the rising $\overline{R_XC}$ signal, and the receiver-buffer contents are compared with the SYNC character each time a bit is input. Comparison continues until an agreement is reached. When the M5M82C51AP has been programmed in the bi-sync mode, data received in further succession is compared. The detection of two SYNC characters in succession makes the USART end the hunt mode, setting the SYNDET pin to the high-level state. This reset operation is prompted by the reading of the status information. When the parity has been programmed, SYNDET is not set in the middle of the last data bit but in the middle of the parity bit.

In the external synchronous mode, the M5M82C51AP gets out of the hunt mode when a high-level synchronization signal is given to the SYNDET pin. The high-level signal requires a minimum duration of one $\overline{R_XC}$ cycle. In the asynchronous mode, however, the EH signal does not affect the operation at all.

Parity and overrun errors are checked in the same way as in the asynchronous system. During hunt-mode operations the parity bit is not checked, but parity checking is carried out even when the receiver is disabled.

The CPU can command the receiver to enter the hunt mode, if synchronization is lost. This prevents the SYNC character from erroneously becoming equal to the received data when all the data in the receiver buffer is set to 1

Attention should be paid to the fact that the SYNDET F/F is reset each time status information is read irrespective of the synchronous mode's being internal or external. This, however, does not return the M5M82C51AP to the hunt mode. Synchronism detection is carried out even though it is not the hunt mode. The synchronous transfer formats are shown in Figs. 8 and 9.

Command Instruction

This instruction defines actual operations in the communication mode designated by mode setting. Command instructions include transmitter/receiver enable error-reset, internal-reset, modem-control, enter-hunt and break transmission instructions.

The mode is set following the reset operation. A SYNC character is set as required, and the writing of high-level signals on the control/data pin ($C/\overline{D}$) that follows it is regarded as a command instruction. When the mode is set all over again from the beginning, the M5M82C51AP can be reset by using inputting via the reset terminal or by internal resetting based on the command instruction.

Note 1: The command error reset (ER), internal reset (IR) and enter-hunt-mode (EH) operations are only effective when the command instruction is loaded, so that these bits need not be returned to 0.

2: When a break character is sent out by a command, the T_XD set to 0 immediately irrespective of whether or not the USART has sent out data.

3: Operations of the USART's receiver section which is always in the enable state cannot be inhibited. The command instruction $R_XE=0$ does not mean that data reception via the R_XD pin is inhibited; it means that the R_XRDY is masked and error flags are inhibited.

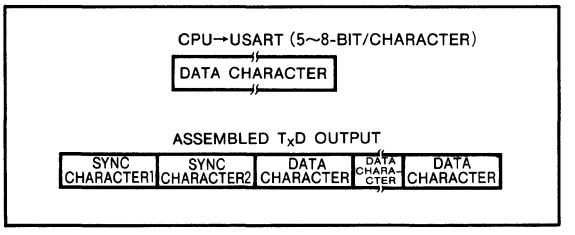
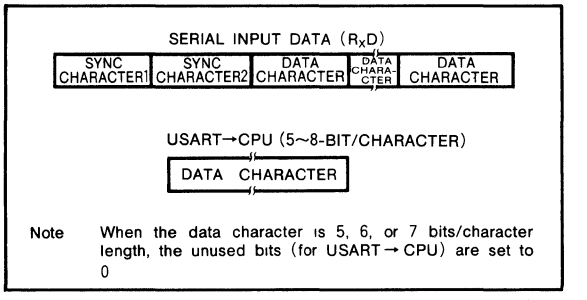


Fig. 8 Synchronous transmission format I (transmission)



Note When the data character is 5, 6, or 7 bits/character length, the unused bits (for USART→CPU) are set to 0

Fig. 9 Synchronous transmission format II (reception)

Status Information

The CPU can always read USART status by setting the C/$\overline{D}$ to high-level and $\overline{RD}$ to low-level.

The status information format is shown in Fig. 10. In this format R_XRDY, T_XEMPTY and SYNDET have the same definitions as those of the pins. This means that these three pieces of status information become high-level when each pin is 1. The other status information is defined as follows:

DSR: When the $\overline{DSR}$ pin is in the low-level state, status information DSR becomes 1.

FE: The occurrence of a frame error in the receiver section makes the status information FE=1.

OE: The occurrence of an overrun error in the receiver section makes the status information OE=1.

PE: The occurrence of a parity error in the receiver section makes this status information PE=1.

T_XRDY: This information becomes 1 when the transmit data buffer is empty. Be careful because this has a different meaning from the T_XRDY pin that enters the high-level state only when the transmitter buffer is empty, when the $\overline{CTS}$ pin is in the low-level state, and when T_XEN is 1.

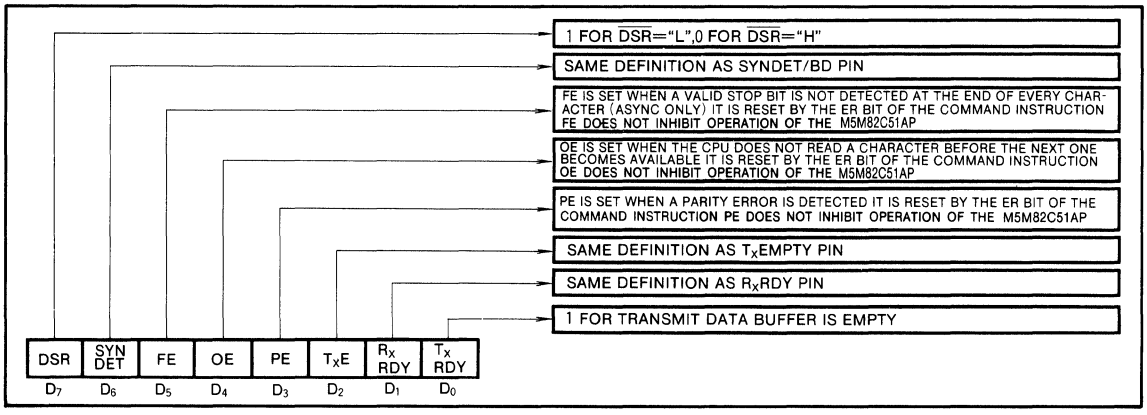


Fig. 10 Status information C/$\overline{D}$="H", $\overline{RD}$="L")

APPLICATION EXAMPLES

Fig. 11 shows an application example for the M5M82C51AP in the asynchronous mode. When the port addresses of the M5M82C51AP are assumed to be 00# and 01# in this figure, initial setting in the asynchronous mode is carried out in the following manner:

```
MVI   A, B6#   Mode setting
OUT   01#
MVI   A, 27#   Command instruction
OUT   01#
```

In this case, the following are set by mode setting:

Asynchronous mode
6-bit/character
Parity enable (even)
1.5 stop bits
Baud rate: 16X

Command instructions set the following

RTS=1→$\overline{RTS}$ pin="L"
R_XE=1
DTR=1→$\overline{DTR}$ pin="L"
T_XEN=1

When the initial setting is complete, transfer operations are allowed. The $\overline{RTS}$ pin is initially set to the low-level by setting RTS to 1, and this serves as a $\overline{CTS}$ input with T_XEN being equal to 1. For this reason the same definition applies to the status and pin of T_XRDY, and 1 is assigned when the transmit-data buffer is empty. Actual transfer of data is carried out in the following way:

```
IN    01#      Status read
```

The IN instruction prompts the CPU to read the USART's status. The result is; if the T_XRDY equals 1 transmitter data is sent from the CPU and written on the M5M82C51AP. Transmitter data is written in the M5M82C51AP in the following manner:

```
MVI   A, 2D#   2D16 is an example of transmitter data.
OUT   00#      USART←(A)
```

Receiver data is read in the following manner:

```
IN    00#      (A)←USART
```

In the above example, the status information is read and as a result, the transmitter data is written and read. Interruption processing by using the T_XRDY and R_XRDY pins is also possible.

Fig. 12 shows the status of the T_XD pin when data written in the USART is transferred from the CPU. When the data shown in Fig.12 enters the R_XD pin, data sent from the M5M82C51AP to the CPU becomes $2D_{16}$ and bits D_6 and D_7 are treated as 0.

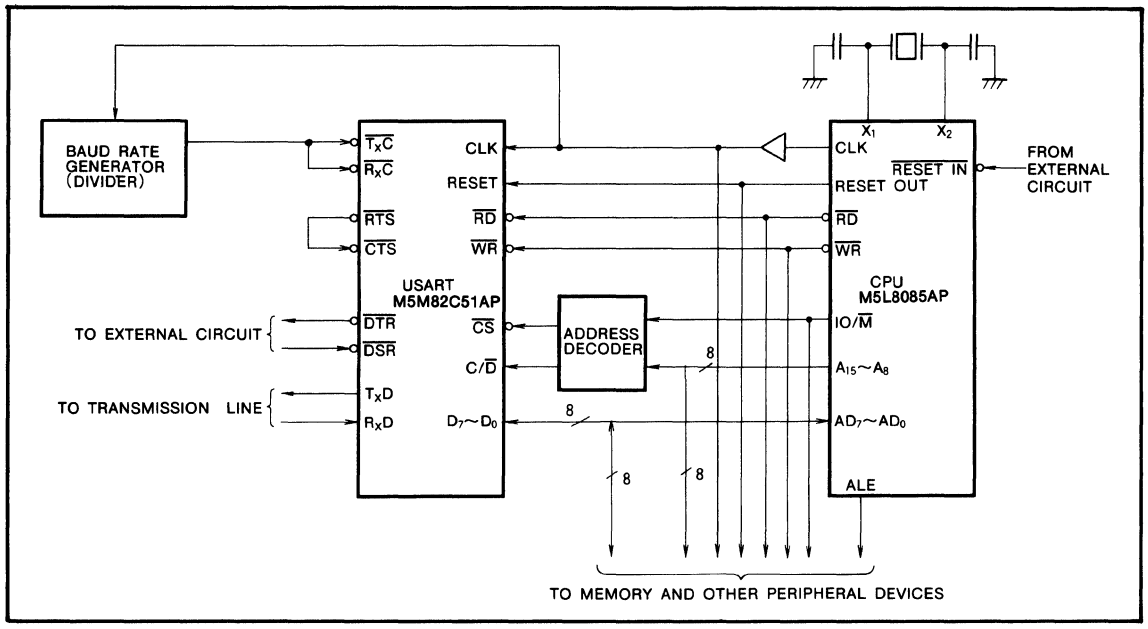


Fig. 11 Example of circuit using the asynchronous mode

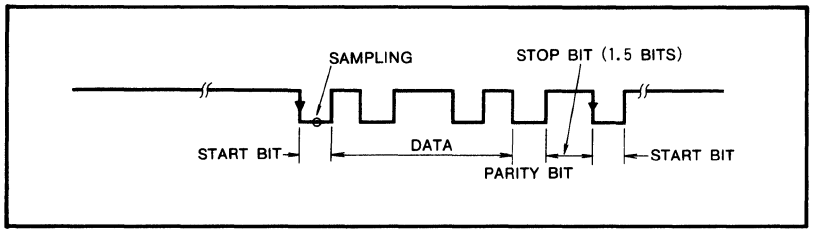


Fig. 12 Example of data transmission

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power-supply voltage	With respect to V_{SS}	−0.3～7	V
V_I	Input voltage		−0.3～V_{CC}+0.3	V
V_O	Output voltage		−0.3～V_{CC}+0.3	V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current	2.5	mA
Topr	Operating free-air temperature range		−20～75	℃
Tstg	Storage temperature range		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～75℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Power-supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20～75℃, V_{CC}=5V±10%, V_{SS}=0V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
		I_{OH}=−20μA	4.4			
V_{OL}	Low-level output voltage	I_{OL}=2.2mA			0.45	V
I_{CC}	Supply current from V_{CC}	All outputs are high-level			5	mA
I_{IH}	High-level input current	V_I=V_{CC}	−10		10	μA
I_{IL}	Low-level input current	V_I=0V	−10		10	μA
I_{OZ}	Off-state input current	V_O=0V～V_{CC}	−10		10	μA
C_I	Input terminal capacitance	V_{CC}=V_{SS}, f=1MHz, 25mV_{rms}, T_a=25℃			10	pF
$C_{I/O}$	Input/output terminal capacitance	V_{CC}=V_{SS}, f=1MHz, 25mV_{rms}, T_a=25℃			20	pF

TIMING REQUIREMENTS (Ta=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V unless otherwise noted)

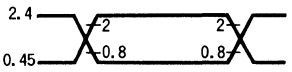
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{C(\phi)}$	Clock cycle time (Notes4, 5)			320		1350	ns
$t_{W(\phi)}$	Clock high pulse width			120		$t_{C(\phi)}$−90	ns
$t_{W(\overline{\phi})}$	Clock low pulse width			90			ns
t_r	Clock rise time					20	ns
t_f	Clock fall time					20	ns
f_{TX}	Transmitter input clock frequency	1X baud rate		DC		64	kHz
		16X baud rate		DC		310	
		64X baud rate		DC		615	
$t_{W(TPWL)}$	Transmitter input clock low pulse width	1X baud rate		12			$t_{C(\phi)}$
		16X, 64X baud rate		1			$t_{C(\phi)}$
$t_{W(TPWH)}$	Transmitter input clock high pulse width	1X baud rate		15			$t_{C(\phi)}$
		16X, 64X baud rate		3			$t_{C(\phi)}$
f_{RX}	Receiver input clock frequency	1X baud rate		DC		64	kHz
		16X baud rate		DC		310	
		64X baud rate		DC		615	
$t_{W(RPWL)}$	Receiver input clock low pulse width	1X baud rate		12			$t_{C(\phi)}$
		16X, 64X baud rate		1			
$t_{W(RPWH)}$	Receiver input clock high pulse width	1X baud rate		15			$t_{C(\phi)}$
		16X, 64X baud rate		3			
$t_{SU(A-R)}$	Address setup time before read ($\overline{CS}$, C/$\overline{D}$) (Note6)			0			ns
$t_{h(R-A)}$	Address hold time after read ($\overline{CS}$, C/$\overline{D}$) (Note6)			0	ns		
$t_{W(R)}$	Read pulse width			250[200]			ns
$t_{SU(A-W)}$	Address setup time before write			0			ns
$t_{h(W-A)}$	Address hold time after write			0			ns
$t_{W(W)}$	Write pulse width			250[200]			ns
$t_{SU(DQ-W)}$	Data setup time before write			150[100]			ns
$t_{h(W-DQ)}$	Data hold time after write			20[0]			ns
$t_{SU(ESD-RxC)}$	E·SYNDET setup time before $\overline{R_XC}$			18			$t_{C(\phi)}$
$t_{SU(C-R)}$	Control setup time before read			20			$t_{C(\phi)}$
t_{RV}	Write recovery time between writes (Note7)			6			$t_{C(\phi)}$
$t_{SU(RxD-IS)}$	R_XD setup time before internal sampling pulse			2			μs
$t_{h(IS-RxD)}$	R_XD hold time after internal sampling pulse			2			μs

Note 4 : The $\overline{T_XC}$ and $\overline{R_XC}$ frequencies have the following limitations with respect to CLK.
For 1X baud rate f_{TX}, $f_{RX} \leqq 1/(30t_{C(\phi)})$. For 16X, 64X baud rate f_{TX}, $f_{RX} \leqq 1/(4.5t_{C(\phi)})$
5 : Reset pulse width=$6t_{C(\phi)}$ minimum. System clock must be running during reset.
6 : $\overline{CS}$, C/$\overline{D}$ are considered as address.
7 : This recovery time is for mode initialization only. Write data is allowed only when T_XRDY=1 Recovery time between writes for asynchronous mode is $8t_{C(\phi)}$, and that for synchronous mode is $16t_{C(\phi)}$.

SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Output data enable time after read (Note8)	C_L=150pF			200[170]	ns
$t_{PVZ(R-DQ)}$	Output data disable time after read		10		100	ns
$t_{PZV(TxC-TxD)}$	T_{XD} enable time after falling edge of $\overline{T_XC}$				1	μs
$t_{PLH(CLB-TxR)}$	Propagation time from center of last bit to T_XRDY (Note9)				8	$t_{C(\phi)}$
$t_{PHL(W-TxR)}$	Propagation time from write data to T_XRDY clear (Note9)				400	ns
$t_{PLH(CLB-RxR)}$	Propagation time from center of last bit to R_XRDY (Note9)				26	$t_{C(\phi)}$
$t_{PHL(R-RxR)}$	Propagation time from read data to R_XRDY clear (Note9)				400	ns
$t_{PLH(RxC-SYD)}$	Propagation time from rising edge of $\overline{R_XC}$ to internal SYNDET (Note9)				26	$t_{C(\phi)}$
$t_{PLH(CLB-TxE)}$	Propagation time from center of last bit to T_XEMPTY (Note9)				20	$t_{C(\phi)}$
$t_{PHL(W-C)}$	Propagation time from rising edge of $\overline{WR}$ to control (Note9)				8	$t_{C(\phi)}$

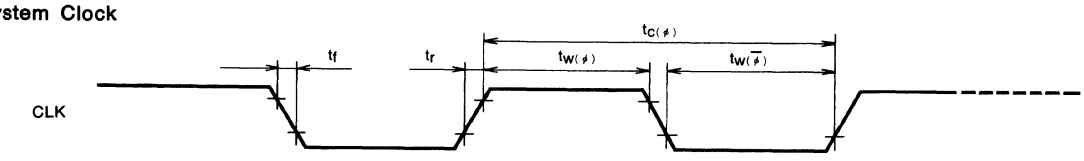
Note 8 : Assumes that address is vaild before falling edge of $\overline{RD}$.
9 : Status-up data can have a maximum delay of 28 clock periods from the event affecting the status.
10 : Input pulse level 0.45~2.4V Reference level Input V_{IH}=2V, V_{IL}=0.8V
Input pulse rise time 10ns Output V_{OH}=2V, V_{OL}=0.8V
Input pulse fall time 10ns



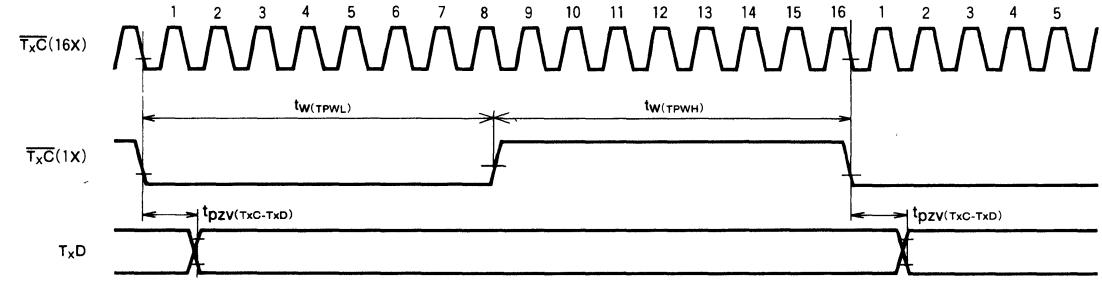
11 : M5M82C51AP is also invested with the extended specification showed in the brackets.

TIMING DIAGRAMS

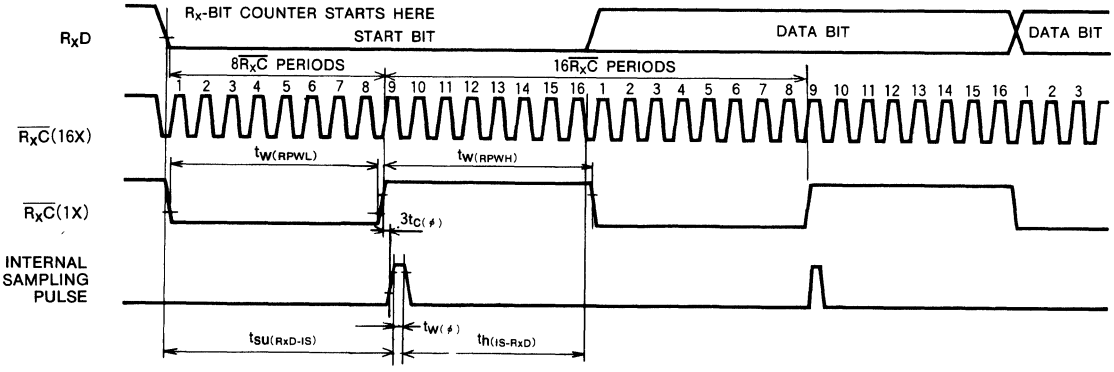
System Clock



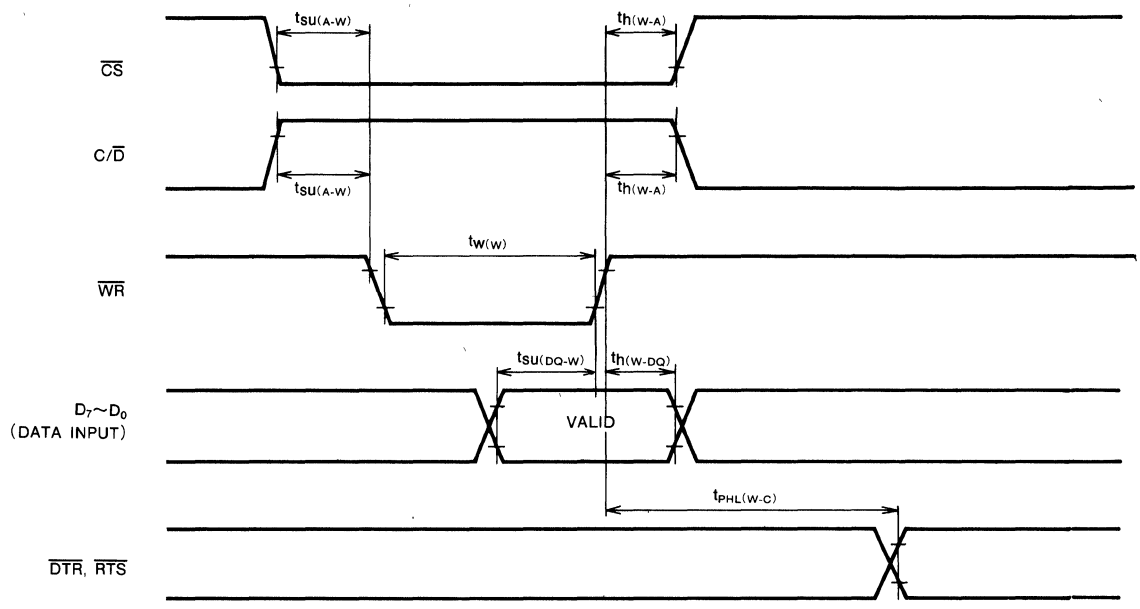
Transmitter Clock & Data



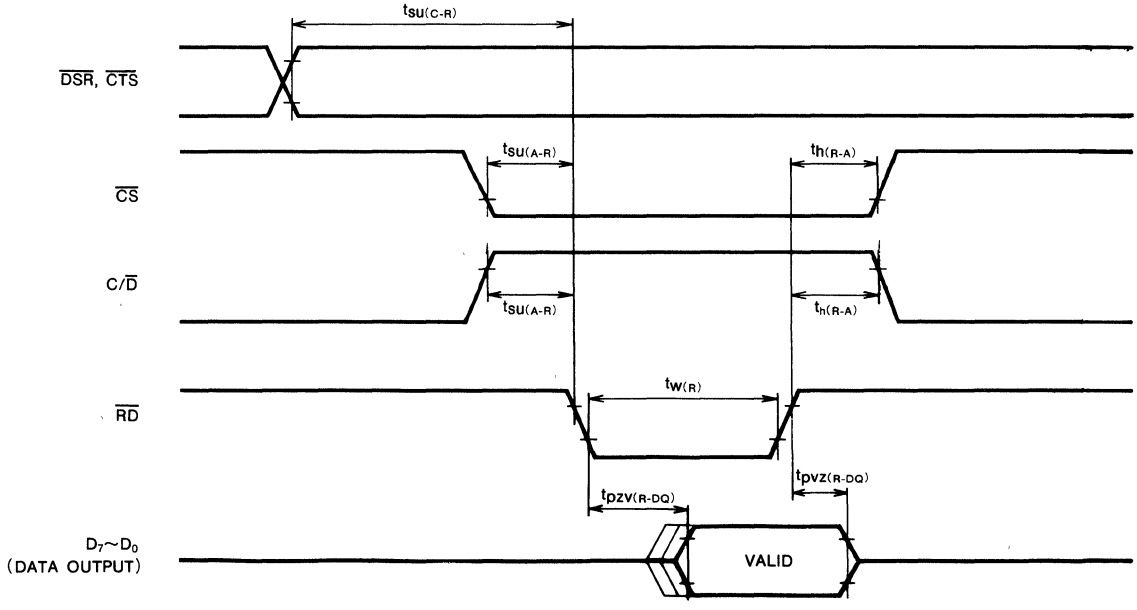
Receiver Clock & Data



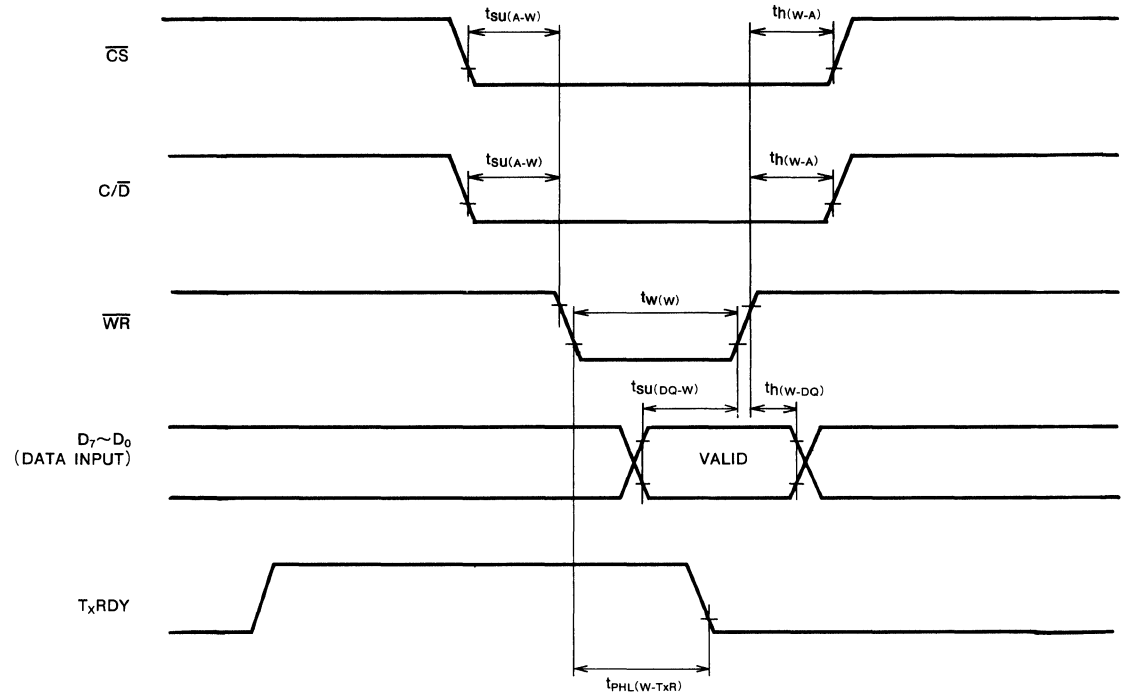
Write Control Cycle (CPU→USART)



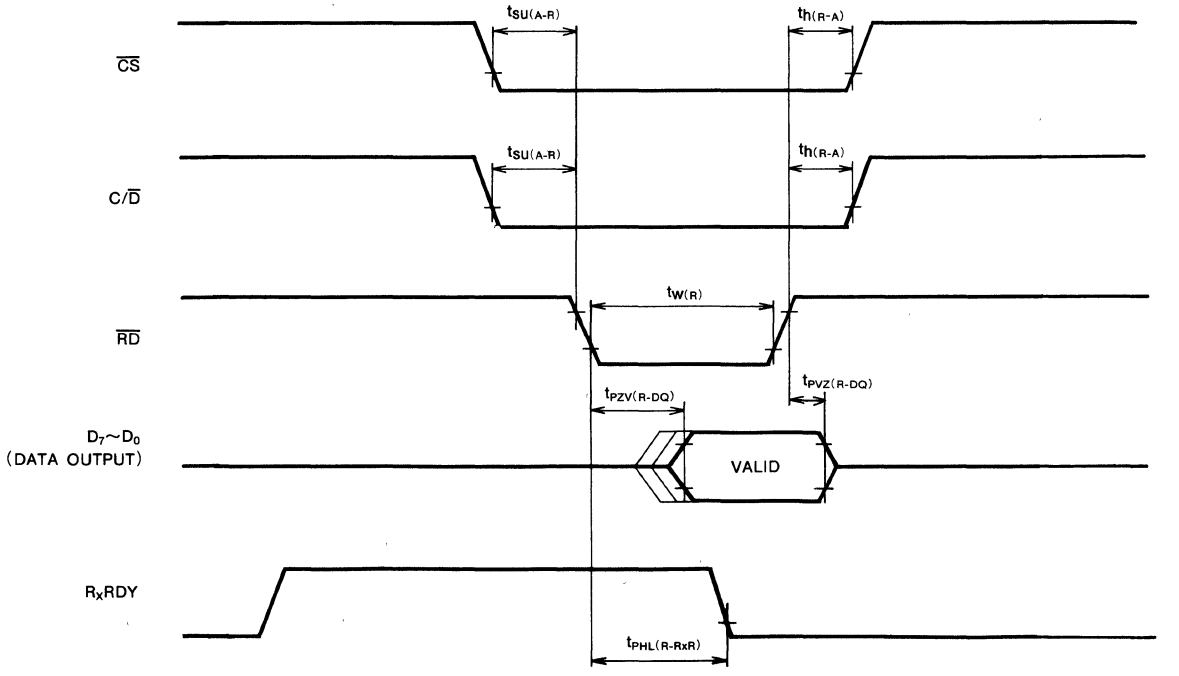
Read Control Cycle (USART→CPU)



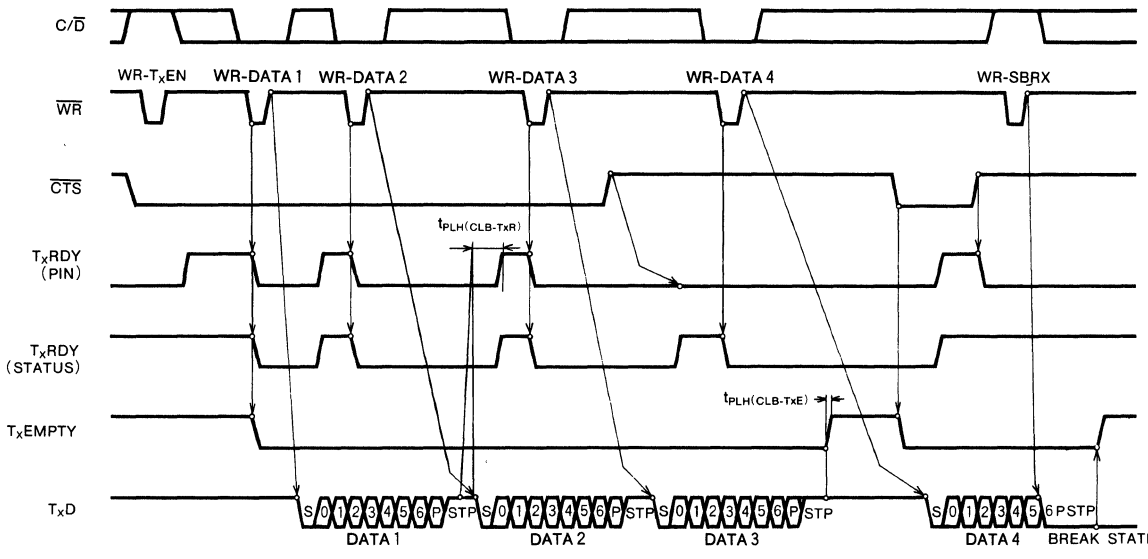
Write Data Cycle (CPU→USART)



Read Data Cycle (USART→CPU)

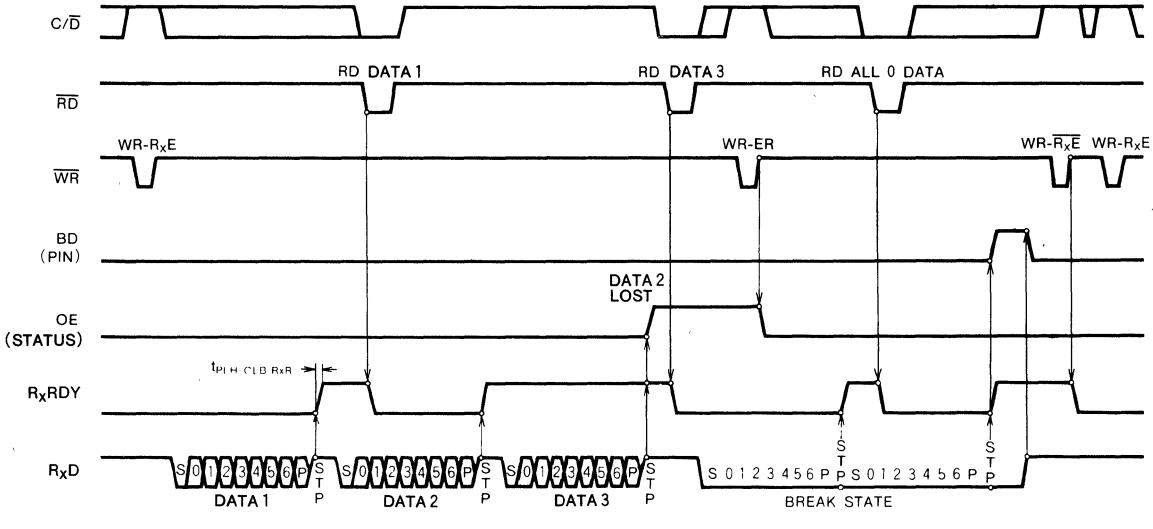


Transmitter Control & Flag Timing (Async Mode)



Note 12 : Example format= 7 bits/character with parity & 2 stop bits
13 : T_xRDY(pin)="H"←(Transmit-data buffer is empty) • (T_xEN= 1) • (CTS="L")
14 : T_xRDY(status)= 1 ←(Transmit-data buffer is empty)

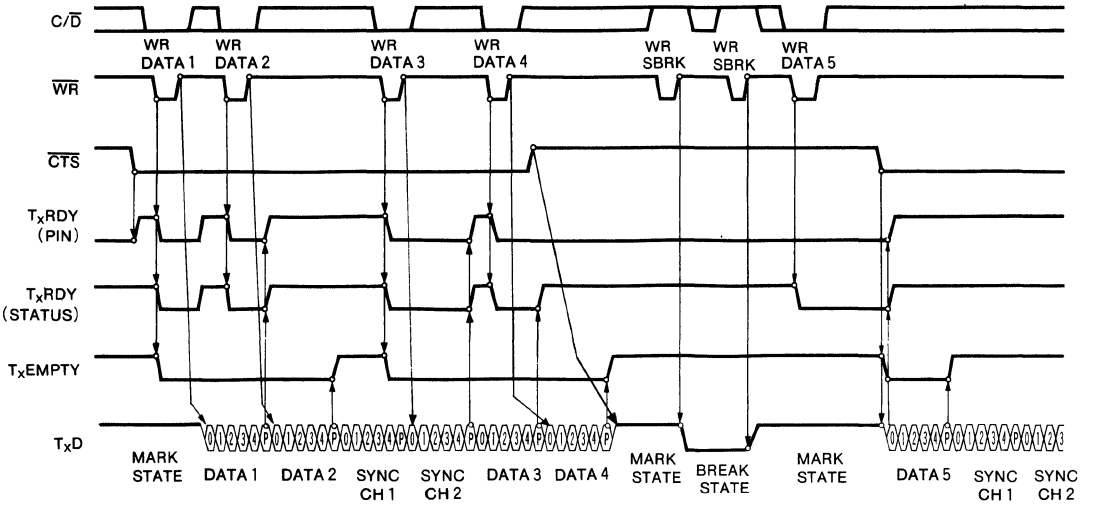
Receiver Control & Flag Timing (Async Mode)



Note 15 : Example format= 7 bits/character with parity & 2 stop bits

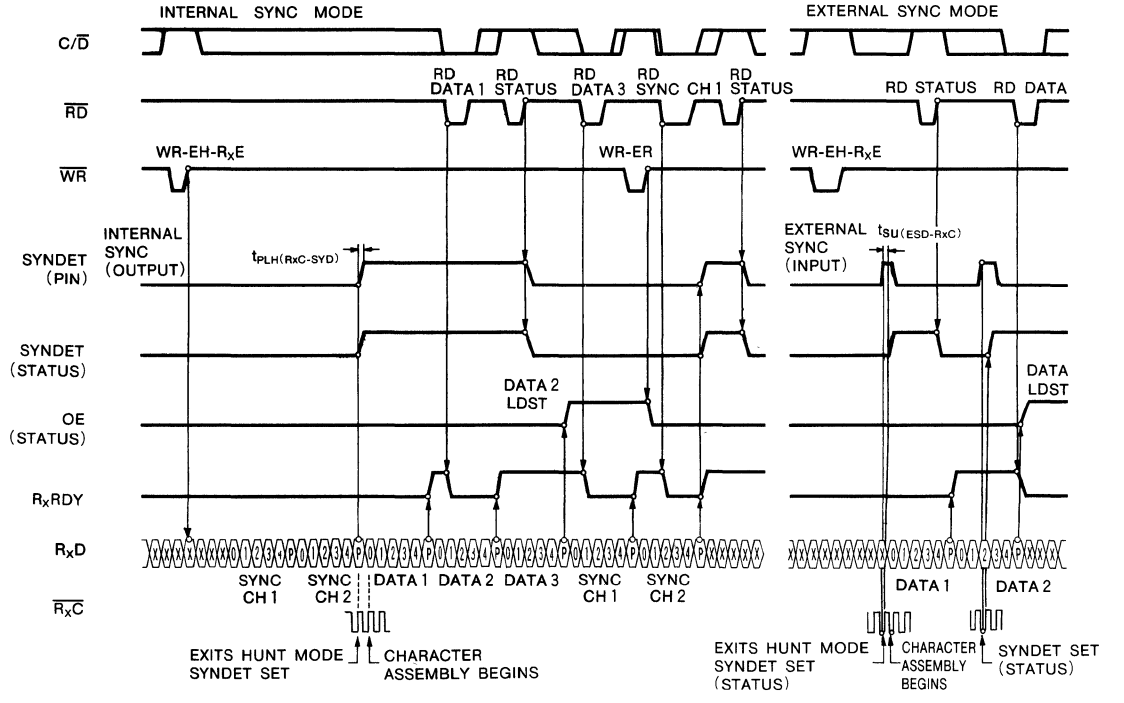
MITSUBISHI ELECTRIC

Transmitter Control & Flag Timing (Sync mode)



Note 16 : Example format= 5 bits/character with parity, bi-sync characters.

Receiver Control & Flag Timing (Sync Mode)



Note 17 : Example format= 5 bits/character with parity, bi-sync characters.

M5M82C54P/FP/J

CMOS PROGRAMMABLE INTERVAL TIMER

DESCRIPTION

The M5M82C54P is a programmable general-purpose timer device developed by using the silicon-gate CMOS process. It offers counter and timer functions in systems using an 8-bit parallel-processing CPU. The use of the M5M82C54P frees the CPU from the execution of looped programs, count-operation programs and other simple processing involving many repetitive operations, thus contributing to improved system throughputs. It is housed in a 24-pin plastic molded DIP.

And preparatory for surface equipment M5M82C54FP (SOP) and M5M82C54J(PLCC).

FEATURES

- Single 5V supply voltage
- TTL compatible
- Pin connection compatible with M5L8253P-5 (except M5M82C54J)
- Clock period : DC~8MHz
- 3 independent built-in 16-bit down counters
- 6 counter modes freely assignable for each counter
- Binary or decimal counts
- Read-back command for monitoring the count and status

APPLICATION

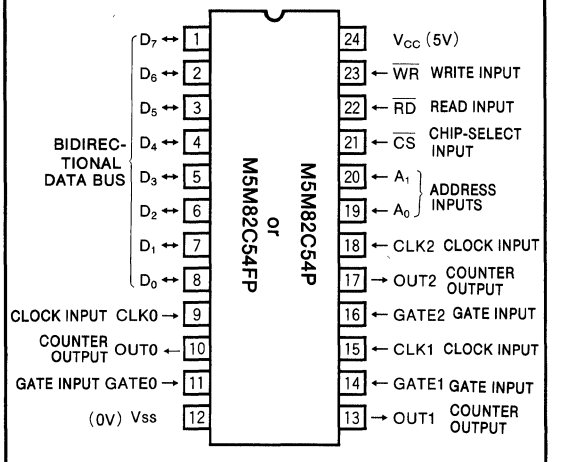
Delayed-time setting, pulse counting and rate generation in microcomputers.

FUNCTION

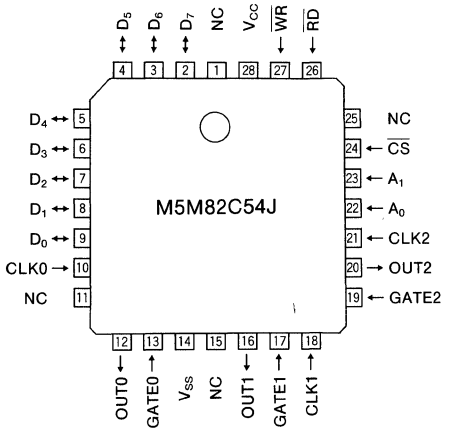
Three independent 16-bit counters allow free programming based on mode-control instructions from the CPU. When roughly classified, there are 6 modes (0~5). Mode 0 is mainly used as an interruption timer and event counter, mode 1 as a digital one-shot, modes 2 and 3 as a rate generator, mode 4 for a software triggered strobe, and mode 5 for a hardware triggered strobe.

The count can be monitored and set at any time. Besides the count, the status of the counter can be monitored by Read-back command. The counter operates with either the binary or BCD system.

PIN CONFIGURATION (TOP VIEW)



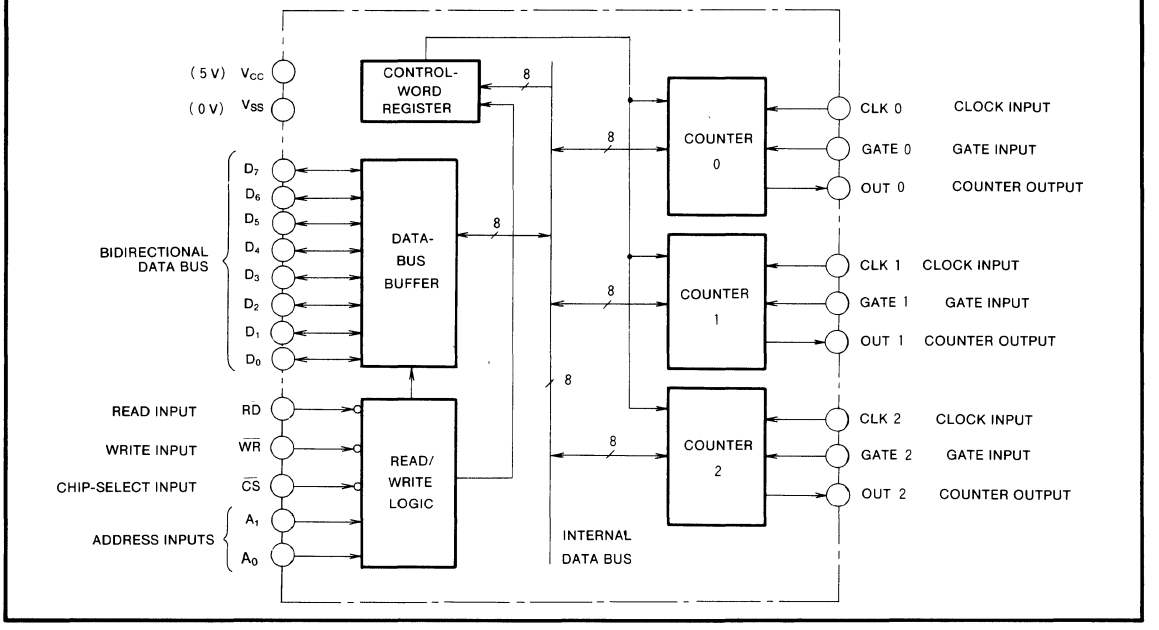
Outline 24P4 (M5M82C54P)
24P2W (M5M82C54FP)



Outline 28P0

NC : NO CONNECTION

BLOCK DIAGRAM



DESCRIPTION OF FUNCTIONS

Data-Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the M5M82C54P to the system-side data bus. Transmission and reception of all the data including control words for mode designation and values written in, and read from, the counters are carried out through this buffer.

Read/Write Logic

The read/write logic accepts control signals ($\overline{RD}$, $\overline{WR}$) from the system and generates control signals for each counter. It is enabled or disabled by the chip-select signal ($\overline{CS}$); if $\overline{CS}$ is at the high-level the data-bus buffer enters a floating (high-impedance) state.

Read Input ($\overline{RD}$)

The count of the counter designated by address inputs A_0 and A_1 on the low-level is output to the data bus.

Write Input ($\overline{WR}$)

Data on the data bus is written in the counter or control-word register designated by address inputs A_0 and A_1 on the low-level.

Address Inputs (A_0, A_1)

These are used for selecting one of the 3 internal counters and either of the control-word registers.

Chip-Select Input ($\overline{CS}$)

A low-level on this input enables the M5M82C54P. Changes in the level of the $\overline{CS}$ input have no effect on the operation of the counters.

Control-Word Register

This register stores information required to give instructions about operational modes and to select binary or BCD counting. It allows reading,using Read back command.

Counters 0,1 and 2

These counters are identical in operation and independent of each other. Each is a 16-bit, presettable, down counter, and has clock-input, gate-input and output pins. The counter can operate in either binary or BCD using the falling edge of each clock. The mode of counter operation and the initial value from which to start counting can be designated by software. The count can be read by input instruction at any time, and there is a "read-on-the-fly" function which enables stable reading by latching each instantaneous count to the registers by a special counter-latch instruction.

CONTROL-WORD AND INITIAL-VALUE LOADING

The function of the M5M82C54P depends on the system software. The operational mode of the counters can be specified by writing control words (A_0, $A_1 = 1$, 1) into the control-word registers.

The programmer must write out to the M5M82C54P the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

Fig. 1 shows control-word format, which consists of 4 fields. Only the counter selected by the D_7 and D_6 bits of the control-word is set for operation. Bits D_5 and D_4 are used for specifying operations to read values in the counter and to initialize. Bits $D_3 \sim D_1$ are used for mode designation, and D_0 for specifying binary or BCD counting. When $D_0=0$, binary counting is employed, and any number from 0000_{16} to $FFFF_{16}$ can be loaded into the count register. The counter is counted down for each clock. The counting of 0000_{16} causes the transmission of a time-out signal from the count-output pin.

The maximum number of counts is obtained when 0000_{16} is set as the initial value. When $D_0=1$, BCD counting is employed, and any number from 0000_{10} to 9999_{10} can be loaded on the counter.

Neither system resetting nor connecting to the power supply sets the control word to any specific value. Thus to bring the counters into operation, the above-mentioned control words for mode designation must be given to each counter, and then 1 ~ 2 byte initial counter values must be set. The following is an example of this programming step.

To designate mode 0 for counter 1 ,with initial value 8254_{16} set by binary count, the following program is used:

MVI	**A, 70_{16}**	Control word 70_{16}
OUT	**n_1**	n_1 is control-word-register address
MVI	**A, 54_{16}**	Low-order 8 bits
OUT	**n_2**	n_2 is counter 1 address
MVI	**A, 82_{16}**	High-order 8 bits
OUT	**n_2**	n_2 is counter 1 address

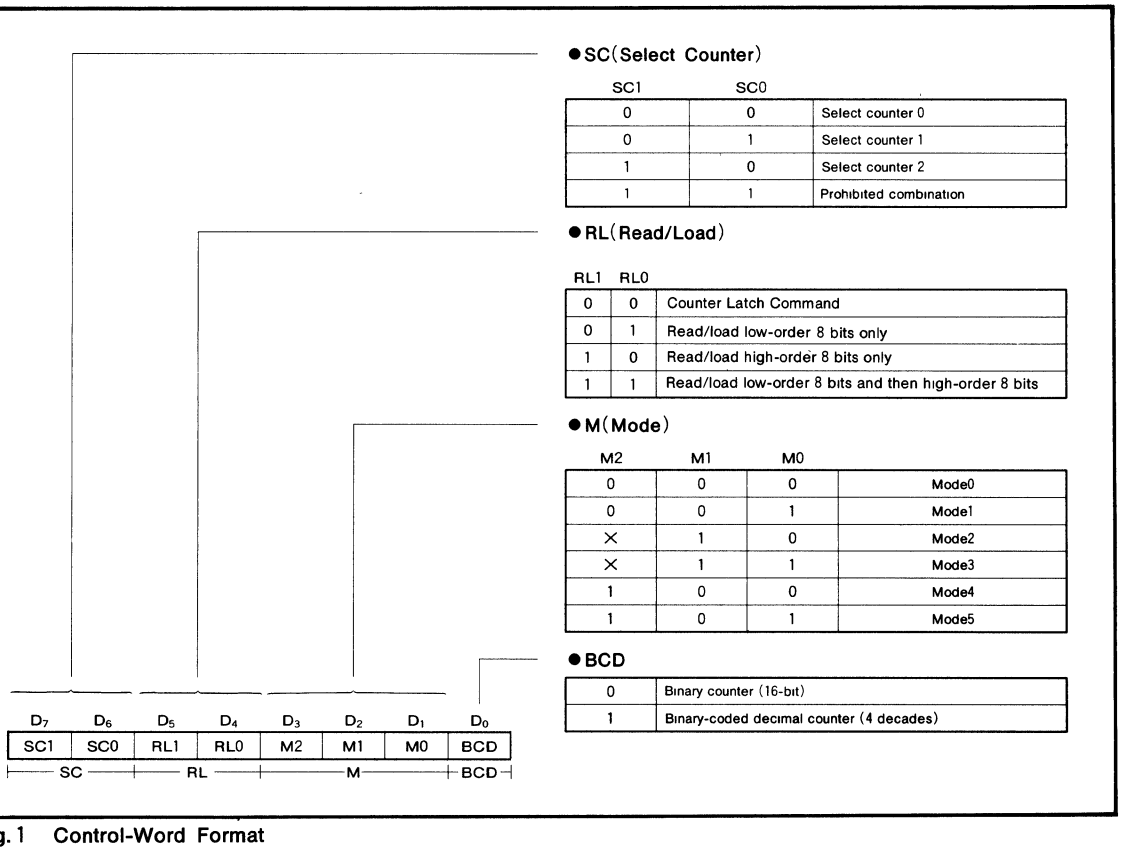
Thus, the program generally has the following sequence:

(1) Control-word output to counter i (i=0, 1, 2).
(2) Initialization of low-order 8 counter bits
(3) Initialization of high-order 8 counter bits

The three counters can be executed in any sequence. It is possible, for instance, to designate the mode of each counter and then load initial values in a different order. Initialization of the counters designated by RL 1 and RL 0 must be executed in the order of the low-order 8 bits and then the high-order 8 bits for the counter in question.

Table 1 Basic Functions

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	Function
L	H	L	0	0	Data bus→Counter 0
L	H	L	0	1	Data bus→Counter 1
L	H	L	1	0	Data bus→Counter 2
L	H	L	1	1	Data bus→Control-word register
L	L	H	0	0	Data bus←Counter 0
L	L	H	0	1	Data bus←Counter 1
L	L	H	1	0	Data bus←Counter 2
L	L	H	1	1	3-state
H	×	×	×	×	3-state
L	H	H	×	×	3-state



● SC(Select Counter)

SC1	SC0	
0	0	Select counter 0
0	1	Select counter 1
1	0	Select counter 2
1	1	Prohibited combination

● RL(Read/Load)

RL1	RL0	
0	0	Counter Latch Command
0	1	Read/load low-order 8 bits only
1	0	Read/load high-order 8 bits only
1	1	Read/load low-order 8 bits and then high-order 8 bits

● M(Mode)

M2	M1	M0	
0	0	0	Mode0
0	0	1	Mode1
×	1	0	Mode2
×	1	1	Mode3
1	0	0	Mode4
1	0	1	Mode5

● BCD

0	Binary counter (16-bit)
1	Binary-coded decimal counter (4 decades)

Fig. 1 Control-Word Format

MODE DEFINITION

Mode 0 (Interrupt on Terminal Count)

Mode set and initialization cause the counter output to go low-level (see Fig. 2). When the counter is loaded with an initial value, it will start counting the clock input. When the terminal count is reached, the output will go high-level and remain high-level until the selected count register is reloaded with the mode. This mode can be used when the CPU is to be interrupted after a certain period or at the time of counting up.

Fig. 2 shows a setting of 4 as the initial value. If gate input goes low-level, counting is inhibited for the duration of the low-level period.

Reloading of the initial value during count operation will stop counting by the loading of the first byte and start the new count by the loading of the second byte.

Mode 1 (Programmable One-Shot)

The gate input functions as a trigger input. A gate-input rising edge causes the generation of low-level one-shot output with a predetermined clock length starting from the next clock. Fig. 3 shows an initial setting of 4. While the counter output is at the low-level (during one-shot), loading of a new value does not change the one-shot pulse width, which has already been output. The current count can be read at any time without affecting the width of the one-shot pulse being output. This mode permits retriggering.

Mode 2 (Rate Generator)

Low-level pulses during one clock operation are generated from the counter output at a rate of one per n clock inputs (where n is the value initially set for the counter). When a new value is loaded during the counter operation, it is reflected on the output after the pulses by the current count have been output. In the example shown in Fig. 4 , n is given as 4 at the outset and is then changed to 3.

In this mode, the gate input provides a reset function. While it is on the low-level, the output is maintained high-level; the counter restarts from the initial value, triggered by a rising gate-input edge. This gate input, therefore, makes possible external synchronization of the counter by hardware.

After the mode is set, the counter does not start counting until the rate n is loaded into the count register, with the counter output remaining at the high-level.

Mode 3 (Square Rate Generator)

This is similar to Mode 2 except that it outputs a square wave with the half count of the set rate. When the set value n is odd, the square-wave output will be high-level for $(n+1)/2$ clock-input counts and low for $(n-1)/2$ counts. When a new rate is reloaded into the count register during its operation, it is immediately reflected on the count directly following the output transition (high-to-low or low-to-high) of the current count. Gate-input operations are exactly the same as in Mode 2. Fig. 5 shows an example of Mode 3 operation.

Mode 4 (Software Triggered Strobe)

After the mode is set, the output will be high-level. By loading a number on the counter, however, clock-input counts can be started and on the terminal count, the output will go low-level for one input-clock period and then will go high-level again. Mode 4 differs from Mode 2 in that pulses are not output repeatedly with the same set count. The pulse output is delayed one clock period in Mode 2, as shown in Fig. 6 . When a new value is loaded into the count register during its count operation, it is reflected on the next pulse output without affecting the current count. The count will be inhibited while the gate input is low-level.

Mode 5 (Hardware Triggered Strobe)

This is a variation of Mode 1. The gate input provides a trigger function, and the count is started by its rising edge. On the terminal count, the counter output goes low for on one clock period and then goes high-level. As in Mode 1, retriggering by the gate input is possible. An example of timing in Mode 5 is shown in Fig. 7 .

As mentioned above, the gate input plays different roles according to the mode. The functions are summarized in Table 3.

Table 2 Gate Operations

Gate / Mode	Low-level or going low-level	Rising	High-level
0	Disables counting		Enables counting
1		(1) Initiates counting (2) Resets output after next clock	
2	(1) Disables counting (2) Sets output high immediately	(1) Reloads counter (2) Initiates counting	Enables counting
3	(1) Disables counting (2) Sets output high immediately	(1) Reloads counter (2) Initiates counting	Enables counting
4	Disables counting		Enables counting
5		Initiates counting	

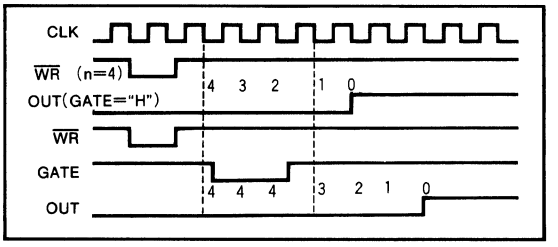


Fig. 2 Mode 0

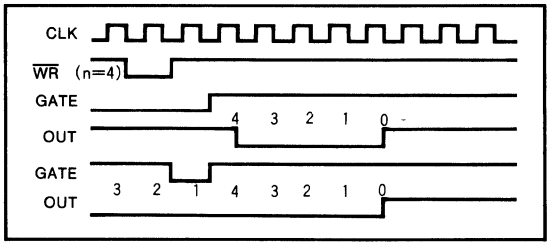


Fig. 3 Mode 1

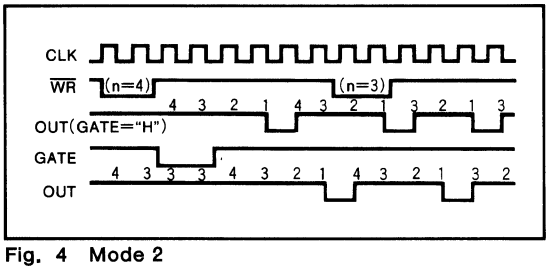


Fig. 4 Mode 2

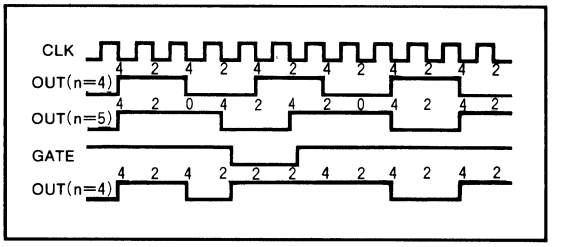


Fig. 5 Mode 3

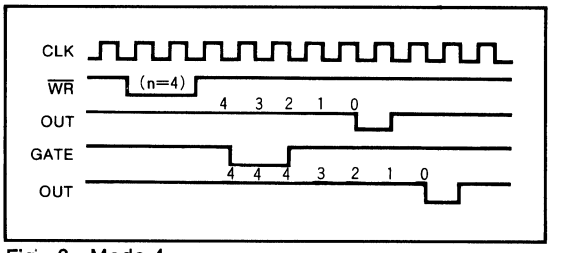


Fig. 6 Mode 4

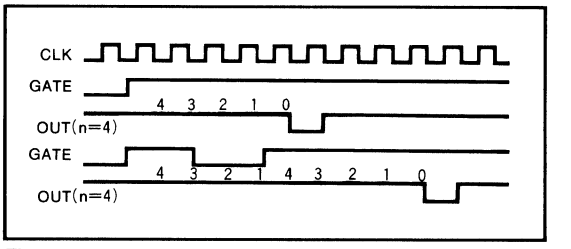


Fig. 7 Mode 5

COUNTER MONITORING

Sometimes the counter must be monitored by reading its count or using it as an event counter. The M5M82C54P offers the following two methods for count reading:

Read Operation

The count can be read by designating the address of the counter to be monitored and executing a simple I/O read operation. In order to ensure correct reading of the count, it is necessary to cause the clock input to pause by external logic or prevent a change in the count by gate input. An example of a program to read the counter 1 count is shown below. If RL1, RL0=1, 1 has been specified in the control word, the first IN instruction enables the low-order 8 bits to be read and the second IN instruction enables the high-order 8 bits.

IN n_2 ····· n_2 is the counter 1 address
MOV **D, A**
IN n_2
MOV **E, A**

The IN instruction should be executed once or twice by the RL1 and RL0 designations in the control-word register.

Read-on-the-Fly Operation

This method makes it possible to read the current count without affecting the count operation at all. A special counter-latch command is first written in the control-word register. This causes latching of all the instantaneous counts to the register, allowing retention of stable counts. An example of a program to execute this operation for counter 2 is given below.

MVI **A, 1000XXXX** ···· $D_5=D_4=0$ designates counter latching
OUT n_1 ···· n_1 is the control-word-register address
IN n_3 ···· n_3 is the counter 2 address
MOV **D, A**
IN n_3
MOV **E, A**

In this example, the IN instruction is executed twice. Due to the internal logic of the M5M82C54P it is absolutely essential to complete the entire reading procedure. If 2 bytes are programmed to be read, then 2 bytes must be read before any OUT instruction can be executed to the same counter.

READ BACK COMMAND

M5M82C54P has a function of reading not only the count but also status (Read Back Command). The read back command enables the next four functions.

(1) read the current count "on the fly"
(2) monitor the current state of the OUT pin
(3) monitor the current state of the counter element (whether the count is loaded into the counter element or not)
(4) read the control-word

Read back operation can be specified by writing read back command into the control word registers (A_0, A_1 =1, 1). Fig. 8 shows the format of read back command.

Bits D_7 and D_6 are used for specifying read back command and fixed 1 (D_7 =1, D_6 =1). Respectively bits D_5 ($\overline{count}$) and D_4 ($\overline{status}$) are used for reading the count and the status of the counter selected by the $D_3 \sim D_1$ bits. Bit D_0 must be fixed 0.

Only the count can be read "on the fly" by setting D_5 =0 and D_4 =1 as well as counter latch command above mentioned. If $D_3 \sim D_1$ are set 1 all, the counts of three counters are simultaneously latched by one read back command. (By counter-latch command, it must be latched for each counter.) Next, by read operation, the latched count is read out.

Only the status can be latched by setting D_5 =1 and D_4 =0. By read operation, the status shown in Fig. 9 can be read.

Bit D_7 gives the current state of OUT pin. When D_7 = 1, OUT = "H", and when D_7 =0, OUT = "L". Bit D_6 indicates the current state of counter element. When D_6 =1, the initial counter value has not been loaded to counter element. This state is following.

(1) The control word is written, but the initial counter value is not loaded
(2) The initial counter value is written to count register, and the CLK inputs are not.

When D_6 = 0, the initial counter value has already been loaded. It is the state when the CLK falls following the rising edge after the initial value is written. Bits $D_5 \sim D_0$ show the current state of the control-word regsiter.

It is possible to read both the count and the status. By setting D_5 =0 and D_4 =0, the status can be read first, and the count next.

The count and/or the status are unlatched when read, so by the next read operation the current counting value can be read. And they are unlatched too when the control-word is set, so the read back command must be set on all such occasions.

If multiple read back commands are written before the read operation, only the first one is valid.

Thus, the read of the status is effective when the state of output and the timing of count reading can be monitored by software.

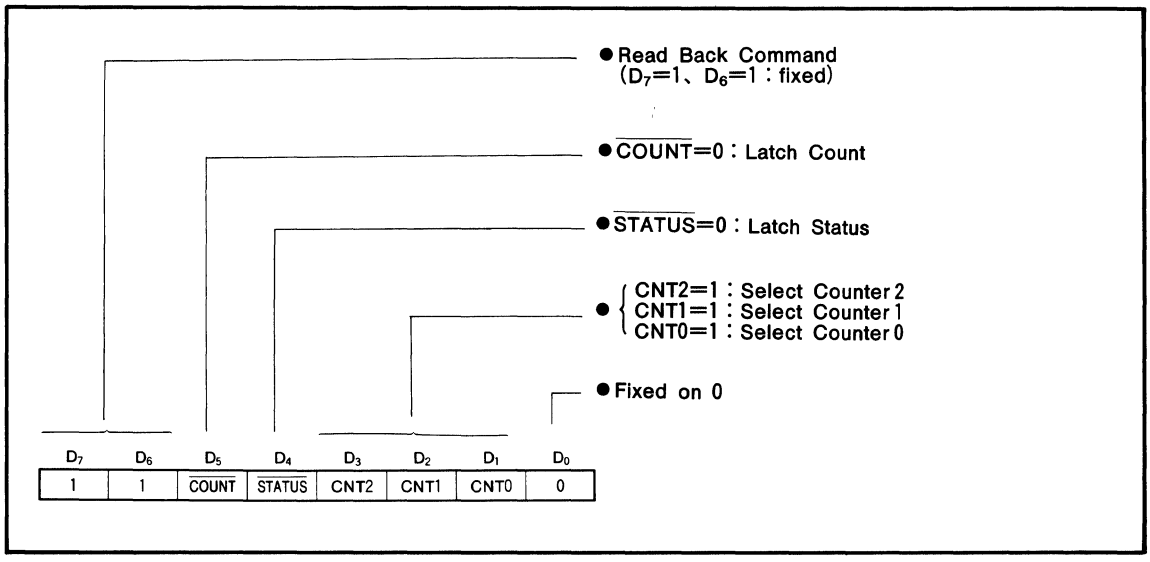


Fig. 8 Read Back Command Format

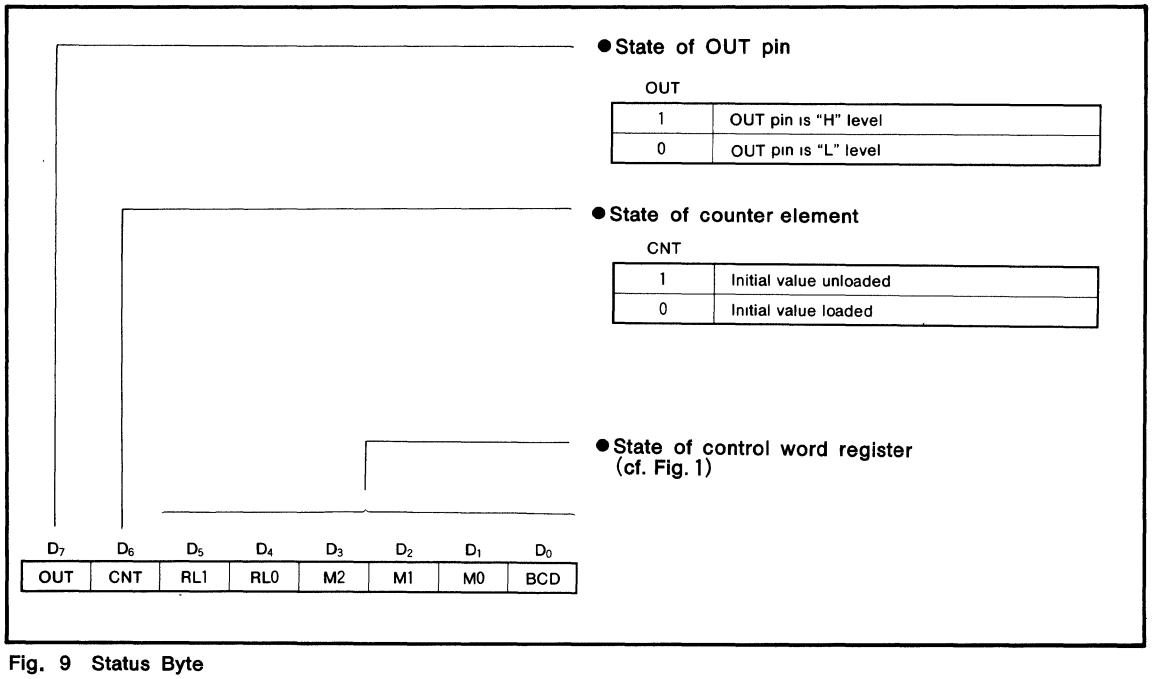


Fig. 9 Status Byte

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power supply voltage	With respect to V_{SS}	−0.3～7	V
V_I	Input voltage		−0.3～V_{CC}+0.3	V
V_O	Output voltage		−0.3～V_{CC}+0.3	V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current	2.5	mA
Topr	Operating free-air temperature range		−20～75	℃
Tstg	Storage temperature range		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=−20～75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Power supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (Ta=−20～75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
		I_{OH}=−20μA	4.4			
V_{OL}	Low-level output voltage	I_{OL}=2.0mA			0.45	V
I_{IH}	High-level input current	V_I=V_{CC}			±10	μA
I_{IL}	Low-level input current	V_I=0V			±10	μA
I_{OZ}	Off-state output current	V_O=0V～V_{CC}			±10	μA
I_{CC}	Supply current from V_{CC} (operating)	f=8MHz			10	mA
I_{CCS}	Supply current from V_{CC} (stand by)	V_I=0V, V_{CC}			10	μA
C_i	Input terminal capacitance	V_{IL}=V_{SS}, f=1MHz, 25mVrms, T_a=25℃			10	pF
$C_{i/o}$	Input/output terminal capacitance	$V_{I/OL}$=V_{SS}, f=1MHz,25mVrms, T_a=25℃			20	pF

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Read cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(R)}$	Read pulse width		150			ns
$t_{su(S-R)}$	$\overline{CS}$ setup time before read		0			ns
$t_{su(A-R)}$	Address setup time before read		45			ns
$t_{h(R-A)}$	Address hold time after read		0			ns
$t_{rec(R)}$	Read recovery time		200			ns

Write cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(W)}$	Write pulse width		150			ns
$t_{su(S-W)}$	$\overline{CS}$ setup time before write		0			ns
$t_{su(A-W)}$	Address setup time before write		0			ns
$t_{h(W-A)}$	Address hold time after write		0			ns
$t_{su(DQ-W)}$	Data setup time before write		120[100]	(Note 1)		ns
$t_{h(W-DQ)}$	Data hold time after write		0			ns
$t_{rec(W)}$	Write recovery time		200			ns

Note 1 : M5M82C54P is also invested with the extended specification showed in the bracket.

Clock and gate timing

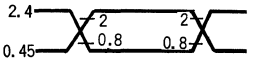
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\phi H)}$	Clock high pulse width		55			ns
$t_{w(\phi L)}$	Clock low pulse width		60			ns
$t_{c(\phi)}$	Clock cycle time		125		DC	ns
$t_{r(\phi)}$	Clock rise time				100	ns
$t_{f(\phi)}$	Clock fall time				100	ns
$t_{w(GH)}$	Gate high pulse width		50			ns
$t_{w(GL)}$	Gate low pulse width		50			ns
$t_{su(G-\phi)}$	Gate setup time before clock		50			ns
$t_{h(\phi-G)}$	Gate hold time after clock		50			ns

SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(A-DQ)}$	Propagation time from address to output	C_L=150pF			220	ns
$t_{PZV(R-DQ)}$	Propagation time from read to output				120	ns
$t_{PVZ(R-DQ)}$	Propagation time from read to output floating (Note 3)		5		90	ns
$t_{PXV(G-OUT)}$	Propagation time from gate to output				120	ns
$t_{PXV(\phi-OUT)}$	Propagation time from clock to output				150	ns

Note 2 : A.C Testing waveform

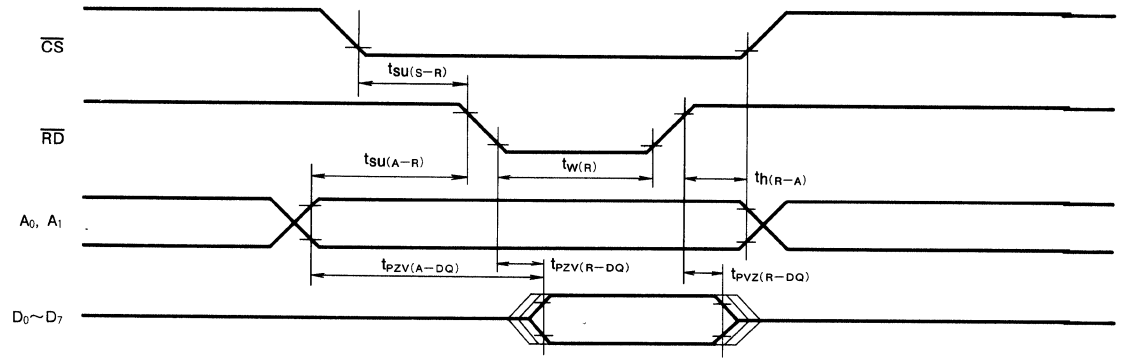
Input pulse level	0.45~2.4V
Input pulse rise time	10ns
Input pulse fall time	10ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V



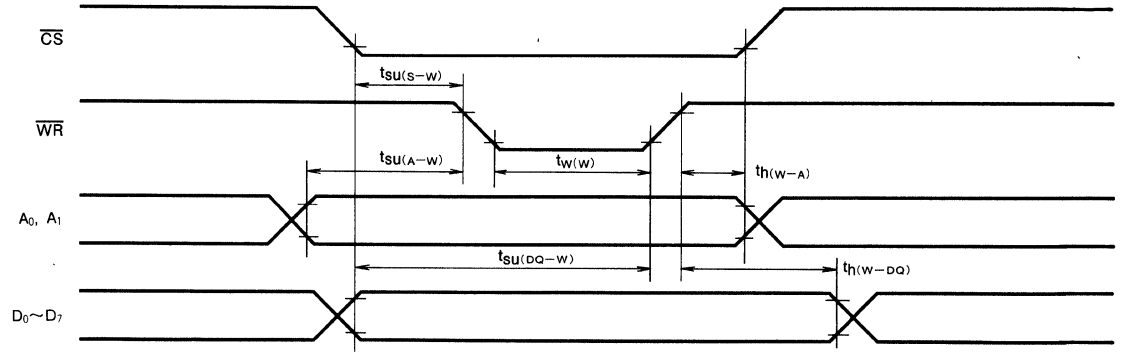
3 : Test condition is not applied

TIMING DIAGRAMS

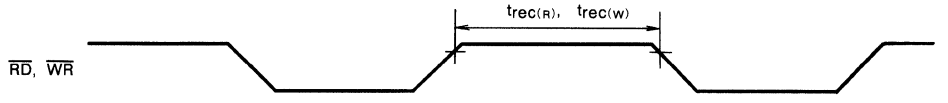
Read Cycle



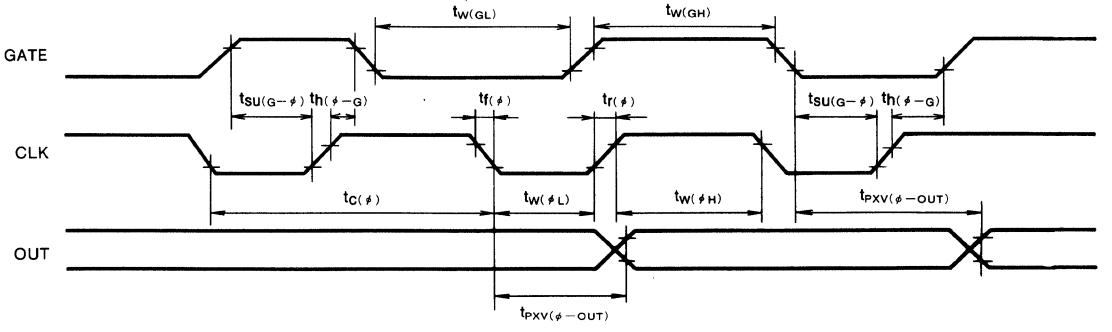
Write Cycle



(Recovery Time)



Clock and Gate Cycle



MITSUBISHI ELECTRIC

M5M82C55AP-2/FP-2/J-2

CMOS PROGRAMMABLE PERIPHERAL INTERFACE

DESCRIPTION

The M5M82C55AP-2 is a family of general-purpose programmable input/ output devices designed for use with the 8/16-bit parallel CPU as input/output ports.

This device is fabricated using silicon-gate CMOS technology for a single supply voltage. This LSI is having 24 input/ output pins which correspond to three 8-bit input/output ports. It is housed in a 40-pin plastic molded DIP.

And preparatory for surface equipment M5M82C55AP-2 (SOP) and M5M82C55AJ-2 (PLCC).

FEATURES

- 120nsec access time
- Having internal anti-noise circuit on RESET, $\overline{ACK}$ and $\overline{STB}$ pins
- Single 5 V supply voltage
- TTL compatible
- Improved DC driving capability
- Improved timing characteristics
- 24 programmable I/O pins
- Direct bit set/reset capability

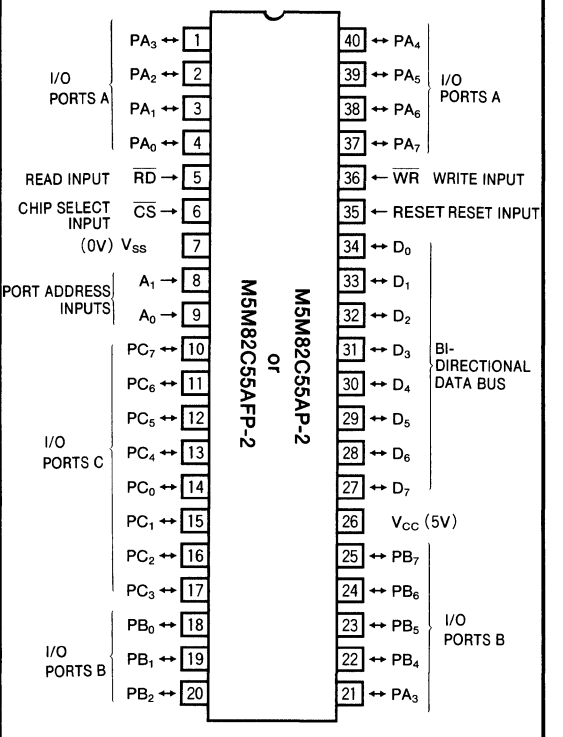
APPLICATION

Input/output ports for microprocessor

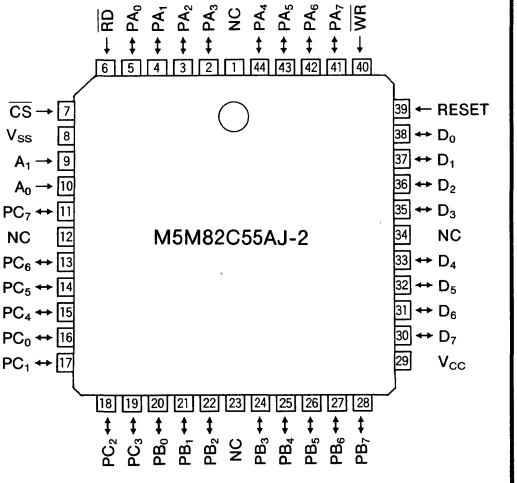
FUNCTION

These PPIs have 24 input/output pins which may be individually programmed in two 12-bit groups A and B with mode control commands from a CPU. They are used in three major modes of operation, mode 0 , mode 1 and mode 2 . Operating in mode 0 , each group of 12 pins may be programmed in sets of 4 to be inputs or outputs. In mode 1 , the 24 I/O terminals may be programmed in two 12-bit groups, group A and group B. Each group contains one 8-bit data port, which may be programmed to serve as input or output, and one 4-bit control port used for handshaking and interrupt control signals. Mode 2 is used with group A only, as one 8-bit bidirectional bus port and one 5-bit control port. Bit set/reset is controlled by CPU. A high-level reset input (RESET) clears control register, and all ports are set to the input mode (high-impedance state).

PIN CONFIGURATION (TOP VIEW)

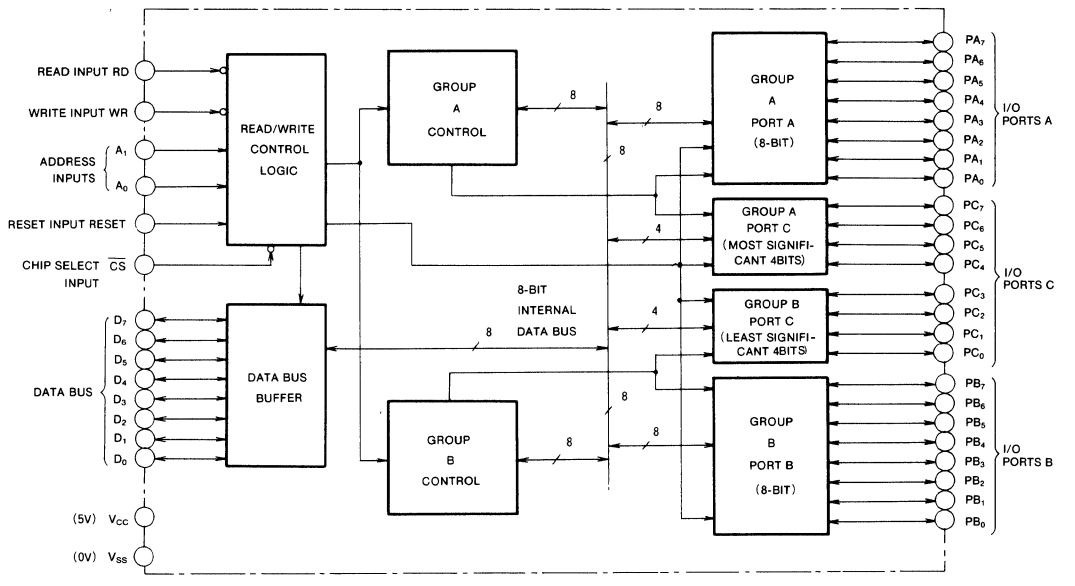


Outline 40P4 (M5M82C55AP-2)
40P2R (M5M82C55AFP-2)



Outline 44P0

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

$\overline{RD}$ (Read) Input

At low-level, the status or the data at the port is transferred to the CPU from the PPI. In essence, it allows the CPU to read data from the PPI.

$\overline{WR}$ (Write) Input

At low-level, the data or control words are transferred from the CPU and written in the PPI.

A_0, A_1 (Port address) Input

These input signals are used to select one of the three ports: port A, port B, and port C, or the control register. They are normally connected to the least significant 2 bits of the address bus.

RESET (Reset) Input

At high-level, the control register is cleared. Then all ports are set to the input mode (high-impedance state).

$\overline{CS}$ (Chip-Select) Input

At low-level, the communication between the PPI and the CPU is enabled. While at high-level, the data bus is kept in the high-impedance state, so that commands from the CPU are ignored. Then the previous data is kept at the output port.

Read/Write Control Logic

The function of this block is to control transfers of both data and control words. It accepts the address signals (A_0, A_1, $\overline{CS}$), I/O control signals ($\overline{RD}$, $\overline{WR}$) and RESET signal, and then issues commands to both of the control groups in the PPI.

Data Bus Buffer

This three-state, bidirectional, 8-bit buffer is used to transfer the data when an input or output instruction is executed by the CPU. Control words and status information are also transferred through the data bus buffer.

Group A and Group B Control

Accepting commands from the read/write control logic, the control blocks (Group A, Group B) receive 8-bit control words from the internal data bus and issue the proper commands for the associated ports. Control group A is associated with port A and the 4 high-order bits of port C. Control group B is associated with port B and the 4 low-order bits of port C. The control register, which stores control words, can only be written into.

Port A, Port B and Port C

The PPI contains three 8-bit ports whose modes and input/output settings are programmed by the system software.

Port A has an output latch/buffer and an input latch/buffer. Port B has an input-output latch/buffer. Port C has an output latch/buffer and an input buffer. Port C can be divided into two 4-bit ports which can be used as ports for control signals for port A and port B.

The basic operations are shown in Table 1.

Table 1 Basic Operations

A_1	A_0	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	Operation
0	0	L	L	H	Data bus ← Port A
0	1	L	L	H	Data bus ← Port B
1	0	L	L	H	Data bus ← Port C
0	0	L	H	L	Port A ← Data bus
0	1	L	H	L	Port B ← Data bus
1	0	L	H	L	Port C ← Data bus
1	1	L	H	L	Control register ← Data bus
X	X	H	X	X	Data bus is in high-impedance state
1	1	L	L	H	Illegal condition

Bit Set/Reset

When port C is used as an output port, any 1bit of the 8-bit can be set (high) or reset (low) by a control word from the CPU. This bit set/reset can be operated in the same way as the mode set, but the control word format is different. This operation is also used for INTE(interrupt enable flag) set/reset in mode 1 and mode 2.

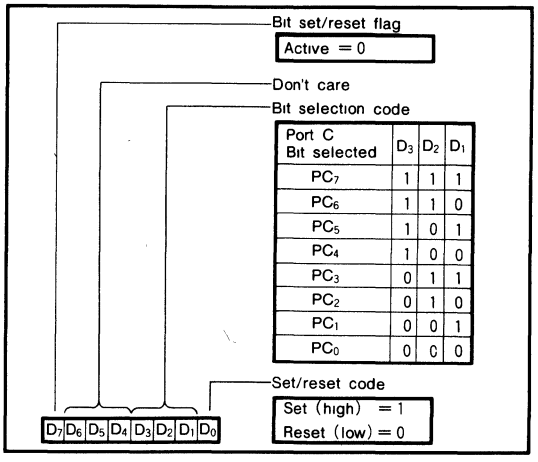


Fig. 1 Control word format for port C set/reset

BASIC OPERATING MODES

The PPI can operate in any one of three selected basic modes.

Mode 0: Basic input/output (group A, group B)
Mode 1: Strobed input/output (group A, group B)
Mode 2: Bidirectional bus (group A only)

The mode of both group A and group B can be selected independently. The control word format for mode set is shown in Fig. 2.

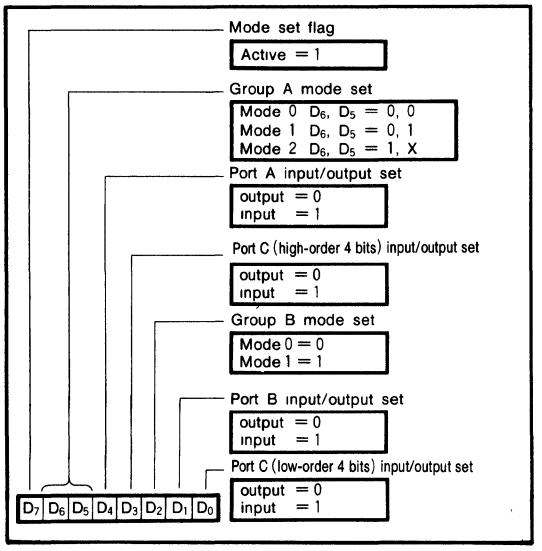
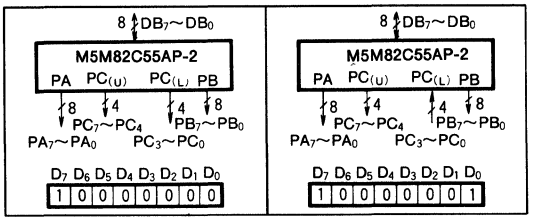
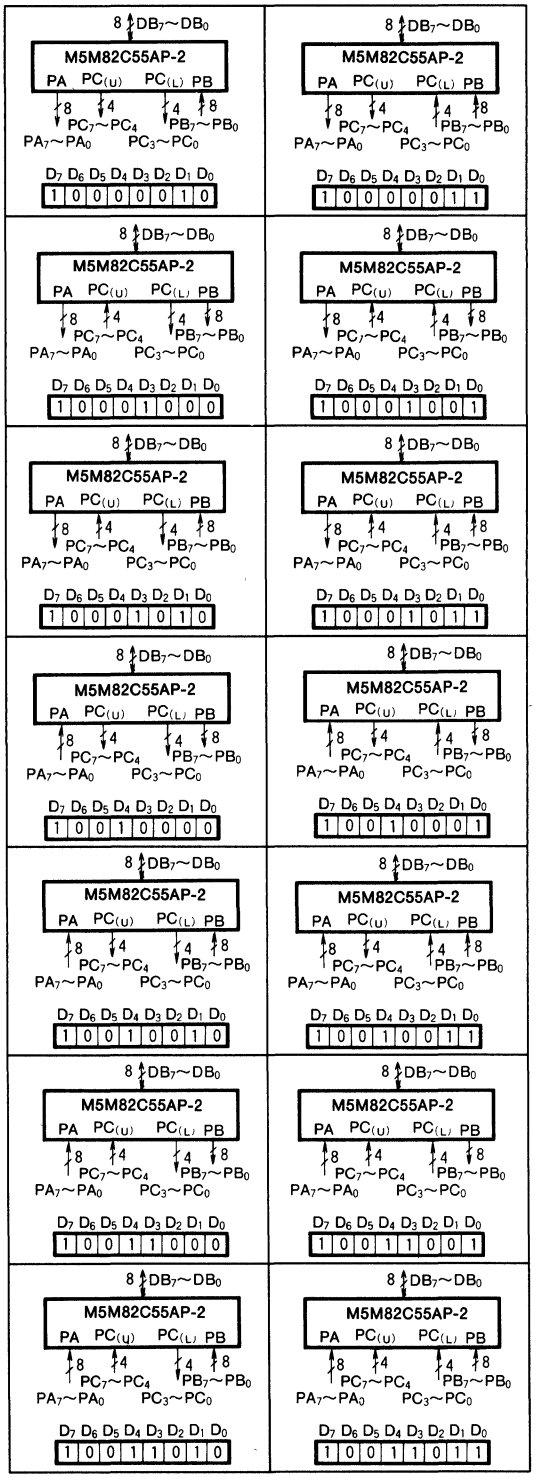


Fig. 2 Control word format for mode set.

1. Mode 0 (Basic Input/Output)

This functional configuration provides simple input and output operations for each of the 3 ports. No "handshaking" is required; data is simply written in, or read from, the specified port. Output data from the CPU to the port can be held, but input data from the port to the CPU cannot be held. Any one of the 8-bit ports and 4-bit ports can be used as an input port or an output port. The diagrams following show the basic input/output operating modes.





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2. Mode 1 (Strobed Input/Output)

This function can be set in both group A and B. Both groups are composed of one 8-bit data port and one 4-bit control data port. The 8-bit port can be used as an input port or an output port. The 4-bit port is used for control and status signals affecting the 8-bit data port. The following shows operations in mode 1 for using input ports.

$\overline{STB}$ (Strobe Input)

A low-level on this input latches the output data from the terminal units into the input register of the port. In short, this is a clock for data latching. The data from the terminal units can be latched by the PPI independent of the control signal from the CPU. This data is not sent to the data bus until the instruction IN is executed.

IBF (Input Buffer Full Flag Output)

A high-level on this output indicates that the data from the terminal units has been latched into the input register. IBF is set to high-level by the falling edge of the $\overline{STB}$ input, and is reset to low-level by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request Output)

This can be used to interrupt the CPU when an input device is requesting service. When INTE (interrupt enable flag) of the PPI is high-level, INTR is set to high-level by the rising edge of the $\overline{STB}$ input and is reset to low-level by the falling edge of $\overline{RD}$ input.

$INTE_A$ of group A is controlled by bit setting of PC_4. $INTE_B$ of group B is controlled by bit setting of PC_2.

Mode 1 input state is shown in Fig. 3, and the timing diagram is shown in Fig. 4.

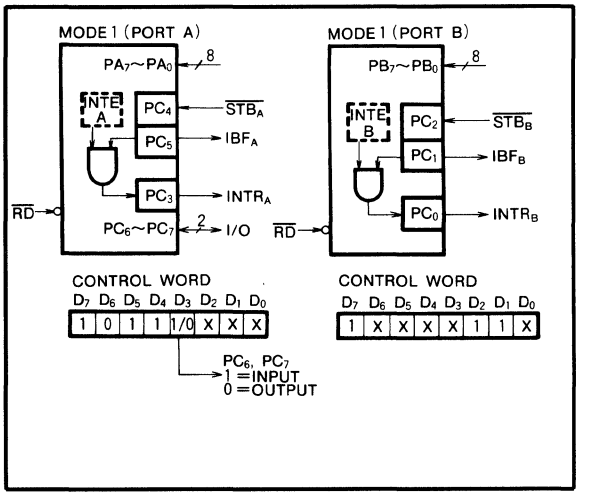


Fig. 3 An example of mode 1 input state

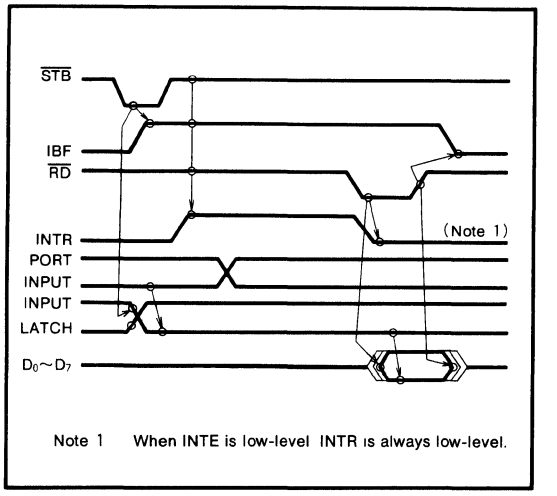


Fig. 4 Timing diagram

The following shows operations using mode 1 for output ports.

$\overline{OBF}$ (Output Buffer Full Flag Output)

This is reset to low-level by the rising edge of the $\overline{WR}$ signal and is set to high-level by the falling edge of the $\overline{ACK}$ (acknowledge input). In essence, the PPI indicates to the terminal units by the $\overline{OBF}$ signal that the CPU has sent data to the port.

$\overline{ACK}$ (Acknowledge Input)

Receiving this signal from a terminal unit can indicate to the PPI that the terminal unit has accepted data from a port.

INTR (Interrupt Request)

When a peripheral unit is accepting data from the CPU, seting INTR to high-level can be used to interrupt the CPU. When INTE (interrupt enable flag) is high-level and $\overline{OBF}$ is set to high-level by the rising edge of an $\overline{ACK}$ signal, then INTR will also be set to high-level by the rising edge of the $\overline{ACK}$ signal. Also, INTR is reset to low-level by the falling edge of the $\overline{WR}$ signal when the PPI has been receiving data from the CPU.

$INTE_A$ of group A is controlled by bit setting of PC_6. $INTE_B$ of group B is controlled by bit setting of PC_2.

Mode 1 output state is shown in Fig. 5, and the timing diagram is shown in Fig. 6.

Combinations for using port A and port B as input or output in mode 1 are shown in Fig. 7 and Fig. 8.

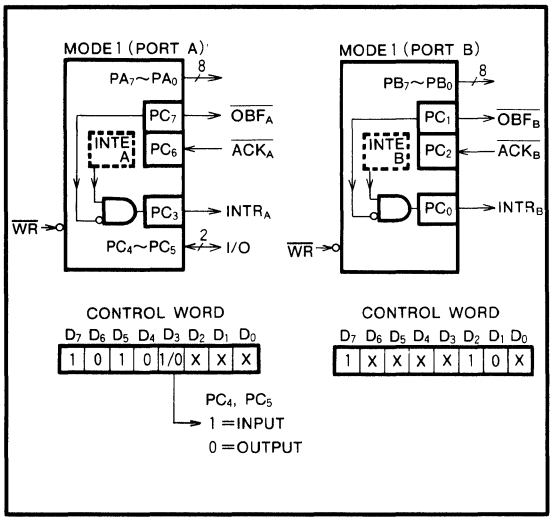


Fig. 5 An example of mode 1 output state

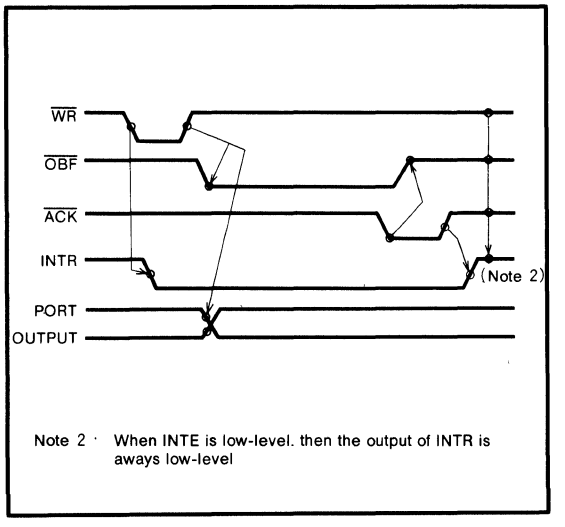


Fig. 6 Timing diagram

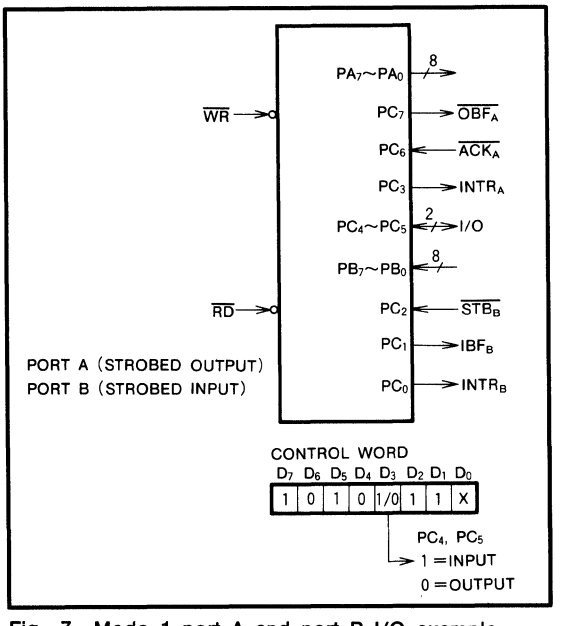


Fig. 7 Mode 1 port A and port B I/O example

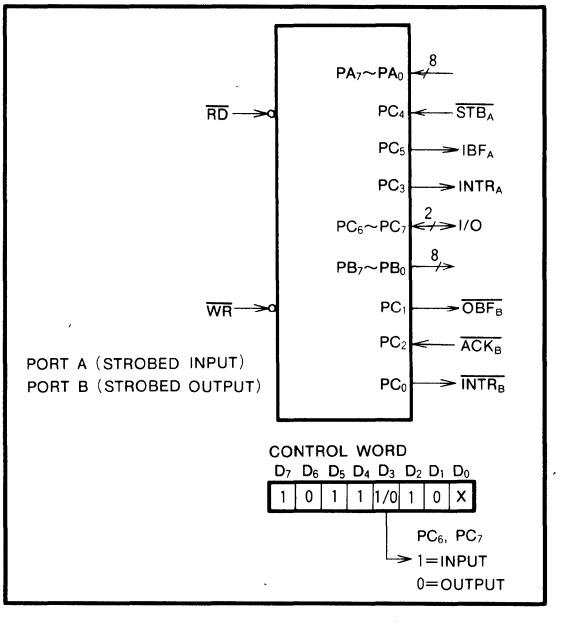


Fig. 8 Mode 1 port A and port B I/O example

3. Mode 2 (Strobed Bidirectional Bus Input/ Output)

Mode 2 can provide bidirectional operations, using one 8-bit bus for communicating with terminal units. Mode 2 is only valid with group A and uses one 8-bit bidirectional bus port (port A) and a 5-bit control port (high-order 5 bits of port C). The bus port (port A) has two internal registers, one for input and the other for output. On the other hand, the control port (port C) is used for communicating control signals and bus-status signals. These control signals are similar to mode 1 and can also be used to control interruption of the CPU. When group A is programmed as mode 2, group B can be programmed independently as mode 0 or mode 1. When group A is in mode 2, the following 5 control signals can be used.

$\overline{OBF}$ (Output Buffer Full Flag Output)

The $\overline{OBF}$ output will go low-level to indicate that the CPU has sent data to the internal register of port A. This signal lets the terminal units know that the data is ready for transfer from the CPU. When this occurs, port A remains in the floating (high-impedance) state.

$\overline{ACK}$ (Acknowledge Input)

A low-level $\overline{ACK}$ input will cause the data of the internal register to be transferred to port A. For a high-level ACK input, the output buffer will be in the floating (high-impedance) state.

$\overline{STB}$ (Strobe Input)

When the $\overline{STB}$ input is low-level, the data from terminal units will be held in the internal register, and the data will be sent to the system data bus with an $\overline{RD}$ signal to the PPI.

IBF (Input Buffer Full Flag Output)

When data from terminal units is held on the internal register, IBF will be high-level.

INTR (Interrupt Request Output)

This output is used to interrupt the CPU and its operations the same as in mode 1. There are two interrupt enable flags that correspond to $INTE_A$ for mode 1 output and mode 1 input.

$INTE_1$ is used in generating INTR signals in combination with $\overline{OBF}$ and $\overline{ACK}$. $INTE_1$ is controlled by bit setting of PC_6.

$INTE_2$ is used in generating INTR signals in combination with $\overline{IBF}$ and $\overline{STB}$. $INTE_2$ is controlled by bit setting of PC_4.

Fig. 9 shows the timing diagram of mode 2, and Fig. 10 is an example of mode 2 operation.

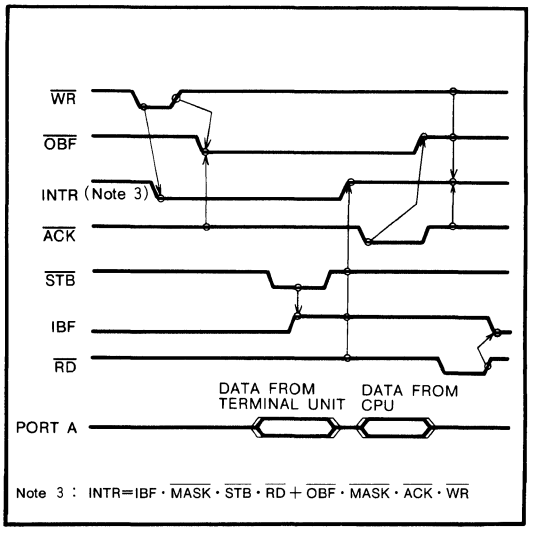


Fig. 9 Mode 2 timing diagram

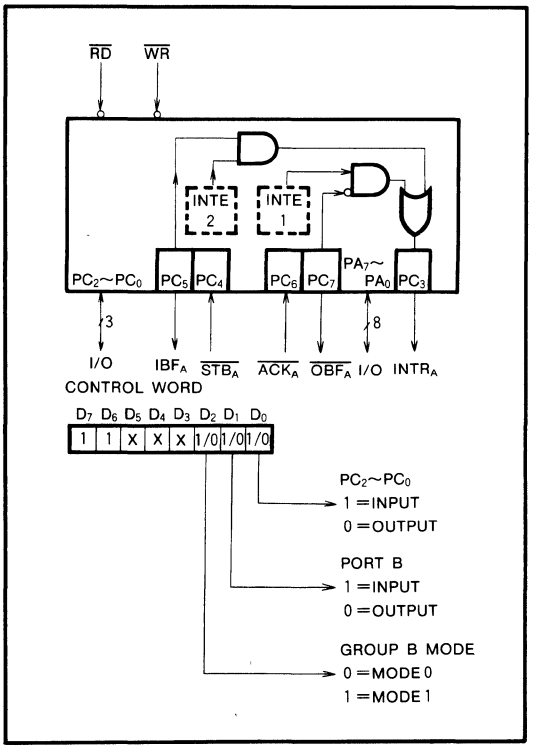


Fig. 10 An example of mode 2 operation

4. Control Signal Read

In mode 1 or mode 2 when using port C as a control port, by CPU execution of an IN instruction, each control signal and bus status from port C can be read.

5. Control Word Tables

Control word formats and operation details for mode 0, mode 1, mode 2 and set/reset control of port C are given in Tables 3, 4, 5 and 6, respectively.

Table 2 Read-out control signals

Data / Mode	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Mode 1, input	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
Mode 1, output	$\overline{OBF_A}$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	$\overline{OBF_B}$	$INTR_B$
Mode 2	$\overline{OBF_A}$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	By group B mode		

Table 3 Mode 0 control words

Control words									Group A		Group B	
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal	Port A	Port C (high-order 4 bits)	Port C (low-order 4 bits)	Port B
1	0	0	0	0	0	0	0	80	OUT	OUT	OUT	OUT
1	0	0	0	0	0	0	1	81	OUT	OUT	IN	OUT
1	0	0	0	0	0	1	0	82	OUT	OUT	OUT	IN
1	0	0	0	0	0	1	1	83	OUT	OUT	IN	IN
1	0	0	0	1	0	0	0	88	OUT	IN	OUT	OUT
1	0	0	0	1	0	0	1	89	OUT	IN	IN	OUT
1	0	0	0	1	0	1	0	8A	OUT	IN	OUT	IN
1	0	0	0	1	0	1	1	8B	OUT	IN	IN	IN
1	0	0	1	0	0	0	0	90	IN	OUT	OUT	OUT
1	0	0	1	0	0	0	1	91	IN	OUT	IN	OUT
1	0	0	1	0	0	1	0	92	IN	OUT	OUT	IN
1	0	0	1	0	0	1	1	93	IN	OUT	IN	IN
1	0	0	1	1	0	0	0	98	IN	IN	OUT	OUT
1	0	0	1	1	0	0	1	99	IN	IN	IN	OUT
1	0	0	1	1	0	1	0	9A	IN	IN	OUT	IN
1	0	0	1	1	0	1	1	9B	IN	IN	IN	IN

Note 4 OUT indicates output port, and IN indicates input port

Table 4 Mode 1 control words

Control words								Hexa-decimal	Group A					Group B			
										Port C					Port C			
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		Port A	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0	Port B
1	0	1	0	0	1	0	X	A4 A5	OUT	$\overline{OBF_A}$	$\overline{ACK_A}$	OUT		$INTR_A$	$\overline{ACK_B}$	$\overline{OBF_B}$	$INTR_B$	OUT
1	0	1	0	0	1	1	X	A6 A7	OUT	$\overline{OBF_A}$	$\overline{ACK_A}$	OUT		$INTR_A$	$\overline{STB_B}$	IBF_B	$INTR_B$	IN
1	0	1	0	1	1	0	X	AC AD	OUT	$\overline{OBF_A}$	$\overline{ACK_A}$	IN		$INTR_A$	$\overline{ACK_B}$	$\overline{OBF_B}$	$INTR_B$	OUT
1	0	1	0	1	1	1	X	AE AF	OUT	$\overline{OBF_A}$	$\overline{ACK_A}$	IN		$INTR_A$	$\overline{STB_B}$	IBF_B	$INTR_B$	IN
1	0	1	1	0	1	0	X	B4 B5	IN	OUT		IBF_A	$\overline{STB_A}$	$INTR_A$	$\overline{ACK_B}$	$\overline{OBF_B}$	$INTR_B$	OUT
1	0	1	1	0	1	1	X	B6 B7	IN	OUT		IBF_A	$\overline{STB_A}$	$INTR_A$	$\overline{STB_B}$	IBF_B	$INTR_B$	IN
1	0	1	1	1	1	0	X	BC BD	IN	IN		IBF_A	$\overline{STB_A}$	$INTR_A$	$\overline{ACK_B}$	$\overline{OBF_B}$	$INTR_B$	OUT
1	0	1	1	1	1	1	X	BE BF	IN	IN		IBF_A	$\overline{STB_A}$	$INTR_A$	$\overline{STB_B}$	IBF_B	$INTR_B$	IN

Note 5 Mode of group A and group B can be programmed independently.
6 · It is not necessary for both group A and group B to be in mode 1

Table 5 Mode 2 control words

Control words								Hexa-decimal (Ex)	Group A						Group B			
									Port A	Port C					PortC			Port B
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0	
1	1	X	X	X	0	0	0	C0	Bidirectional bus	$\overline{OBF_A}$	$\overline{ACK_A}$	IBF_A	$\overline{STB_A}$	$INTR_A$	OUT			OUT
1	1	X	X	X	0	0	1	C1	Bidirectional bus	$\overline{OBF_A}$	$\overline{ACK_A}$	IBF_A	$\overline{STB_A}$	$INTR_A$	IN			OUT
1	1	X	X	X	0	1	0	C2	Bidirectional bus	$\overline{OBF_A}$	$\overline{ACK_A}$	IBF_A	$\overline{STB_A}$	$INTR_A$	OUT			IN
1	1	X	X	X	0	1	1	C3	Bidirectional bus	$\overline{OBF_A}$	$\overline{ACK_A}$	IBF_A	$\overline{STB_A}$	$INTR_A$	IN			IN
1	1	X	X	X	1	0	X	C4	Bidirectional bus	$\overline{OBF_A}$	$\overline{ACK_A}$	IBF_A	$\overline{STB_A}$	$INTR_A$	$\overline{ACK_B}$	$\overline{OBF_B}$	$INTR_B$	OUT
1	1	X	X	X	1	1	X	C6	Bidirectional bus	$\overline{OBF_A}$	$\overline{ACK_A}$	IBF_A	$\overline{STB_A}$	$INTR_A$	$\overline{STB_B}$	IBF_B	$INTR_B$	IN

Table 6 Port C bit set/reset control words

Control words								Hexa-decimal	Port C								Remarks
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0	
0	X	X	X	0	0	0	0	00								0	
0	X	X	X	0	0	0	1	01								1	
0	X	X	X	0	0	1	0	02							0		
0	X	X	X	0	0	1	1	03							1		
0	X	X	X	0	1	0	0	04						0			$INTE_B$ set/reset for mode 1 input
0	X	X	X	0	1	0	1	05						1			$INTE_B$ set/reset for mode 1 output
0	X	X	X	0	1	1	0	06					0				
0	X	X	X	0	1	1	1	07					1				
0	X	X	X	1	0	0	0	08				0					$INTE_A$ set/reset for mode 1 input
0	X	X	X	1	0	0	1	09				1					$INTE_2$ set/reset for mode 2
0	X	X	X	1	0	1	0	0A			0						
0	X	X	X	1	0	1	1	0B			1						
0	X	X	X	1	1	0	0	0C		0							$INTE_A$ set/reset for mode 1 output
0	X	X	X	1	1	0	1	0D		1							$INTE_1$ set/reset for mode 2
0	X	X	X	1	1	1	0	0E	0								
0	X	X	X	1	1	1	1	0F	1								

Note 7 : The terminals of port C should be programmed for the output mode, before the bit set/reset operation is executed.
8 : Also used for controlling the interrupt enable flag(INTE).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings		Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3~7		V
V_I	Input voltage		−0.3~V_{CC}+0.3		V
V_O	Output voltage		−0.3~V_{CC}+0.3		V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current	Port	−4	mA
			Data bus	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current 2	Port	4	mA
			Data bus	2.5	
Topr	Operating free-air temperature renge		−20~75		℃
Tstg	Storage temperature range		−65~150		℃

RECOMMENDED OPERATING CONDITIONS (Ta=−20~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (Ta=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	Output high voltage (Note10)	I_{OH}=−400μA	2.4			V
		I_{OH}=−20μA	4.4			
V_{OL}	Output low voltage (Note10)	I_{OL}=2.5mA			0.4	V
I_{CC}	Supply current from V_{CC}	All input mode RESET=0V. Other pins=V_{CC}.			10	μA
I_{IL}	Input leak current	V_I=0V, V_{CC}			±10	μA
I_{OZ}	Off-state output current	V_O=0V~V_{CC}			±10	μA
C_I	Input terminal capacitance	f=1MHz			10	pF
$C_{I/O}$	Input/output terminal capacitance	Unmeasured pins=0V			20	pF

Note 9 : Current flowing into an IC is positive, out is negative.
10 : Output current must be less than ±4mA for each Port pin

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(R)}$	Read pulse width		160			ns
$t_{SU(PE-R)}$	Peripheral setup time before read		0			ns
$t_{h(R-PE)}$	Peripheral hold time after read		0			ns
$t_{SU(A-R)}$	Address setup time before read		0			ns
$t_{h(R-A)}$	Address hold time after read		0			ns
$t_{W(W)}$	Write pulse width		120			ns
$t_{SU(DQ-W)}$	Data setup time before write		100			ns
$t_{h(W-DQ)}$	Data hold time after write		0			ns
$t_{SU(A-W)}$	Address setup time before write		0			ns
$t_{h(W-A)}$	Address hold time after write		0			ns
$t_{W(ACK)}$	Acknowledge pulse width		300			ns
$t_{W(STB)}$	Strobe pulse width		350			ns
$t_{SU(PE-STB)}$	Peripheral setup time before strobe		0			ns
$t_{h(STB-PE)}$	Peripheral hold time after strobe		150			ns
$t_{C(RW)}$	Read/write cycle time		200			ns

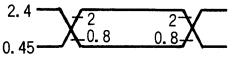
SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PVZ(R-DQ)}$	Propagation time from read to data output	C_L=150pF			120	ns
$t_{PZV(R-DQ)}$	Propagation time from read to data floating (Note11)		10		85	ns
$t_{PHL(W-PE)}$ $t_{PLH(W-PE)}$	Propagation time from write to output				350	ns
$t_{PLH(STB-IBF)}$	Propagation time from strobe to IBF flag				300	ns
$t_{PLH(STB-INTR)}$	Propagation time from strobe to interrupt				300	ns
$t_{PHL(R-INTR)}$	Propagation time from read to interrupt				400	ns
$t_{PHL(R-IBF)}$	Propagation time from read to IBF flag				300	ns
$t_{PHL(W-INTR)}$	Propagation time from write to interrupt				450	ns
$t_{PHL(W-OBF)}$	Propagation time from write to $\overline{OBF}$ flag				300	ns
$t_{PLH(ACK-OBF)}$	Propagation time from acknowledge to $\overline{OBF}$ flag				350	ns
$t_{PLH(ACK-INTR)}$	Propagation time from acknowledge to interrupt				350	ns
$t_{PVZ(ACK-PE)}$	Propagation time from acknowledge to data output				300	ns
$t_{PZV(ACK-PE)}$	Propagation time from acknowledge to data floating (Note11)		20		250	ns

Note 11 : Test conditions are not applied.

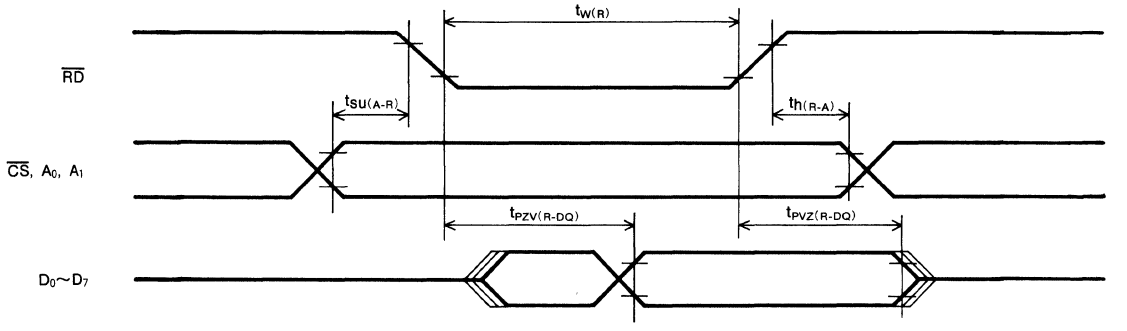
12 : A.C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	10ns
Input pulse fall time	10ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V

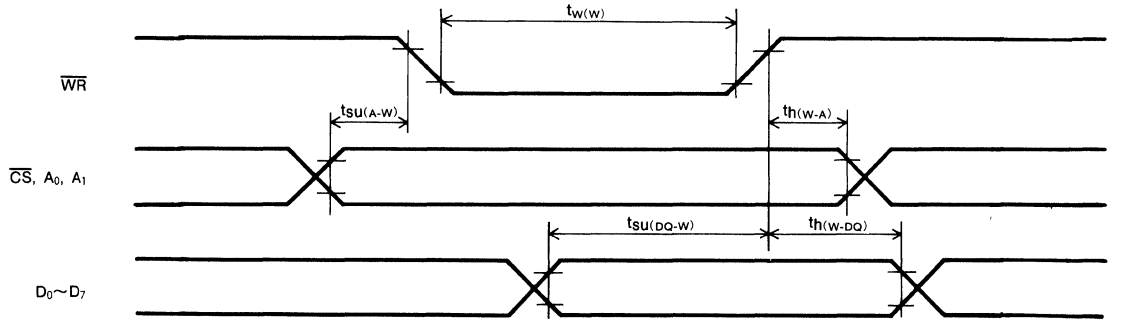


TIMING DIAGRAM

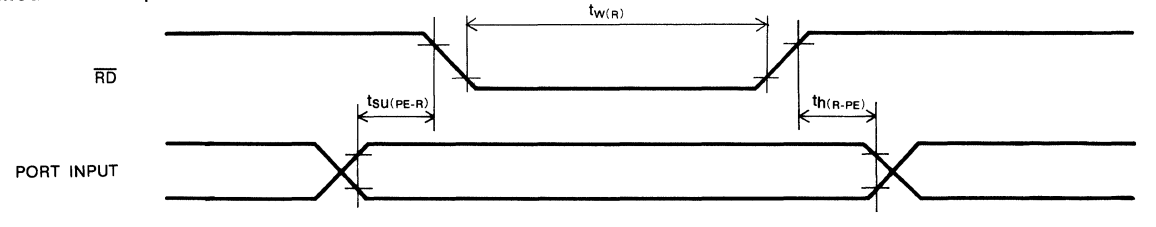
Data Bus Read Operation



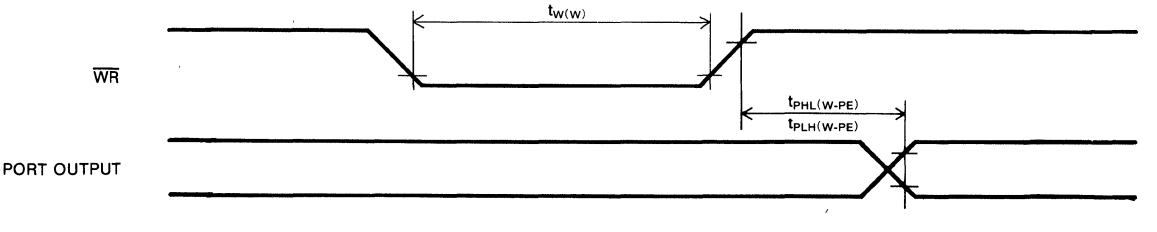
Data Bus Write Operation



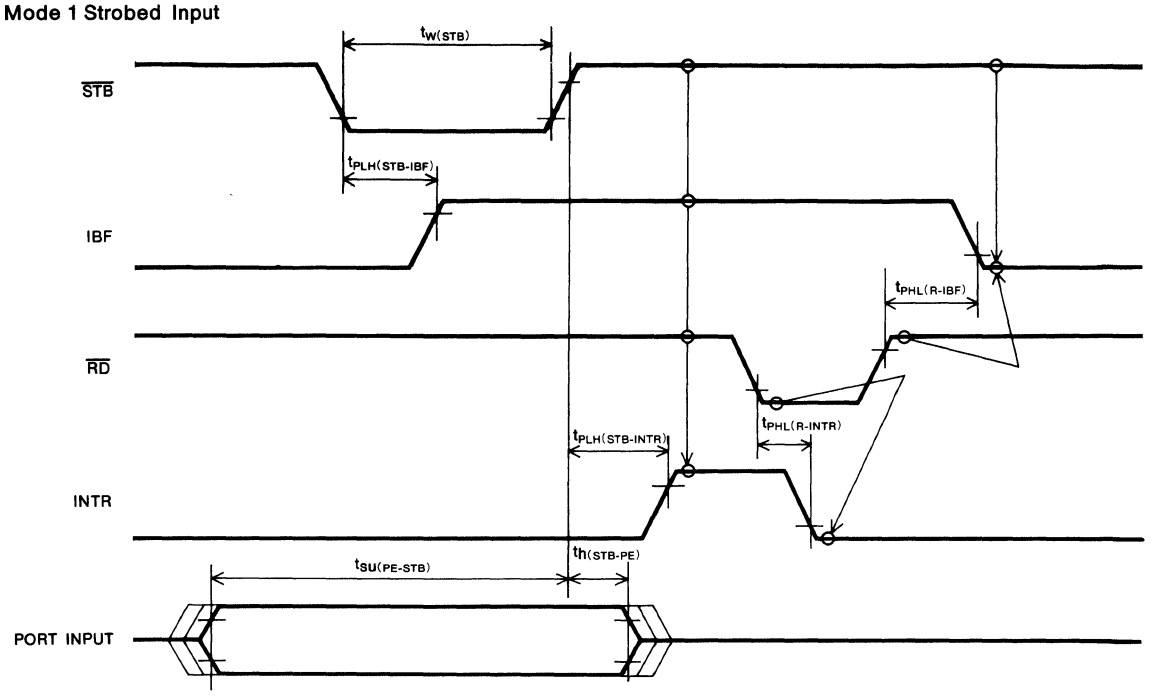
Mode 0 Port Input



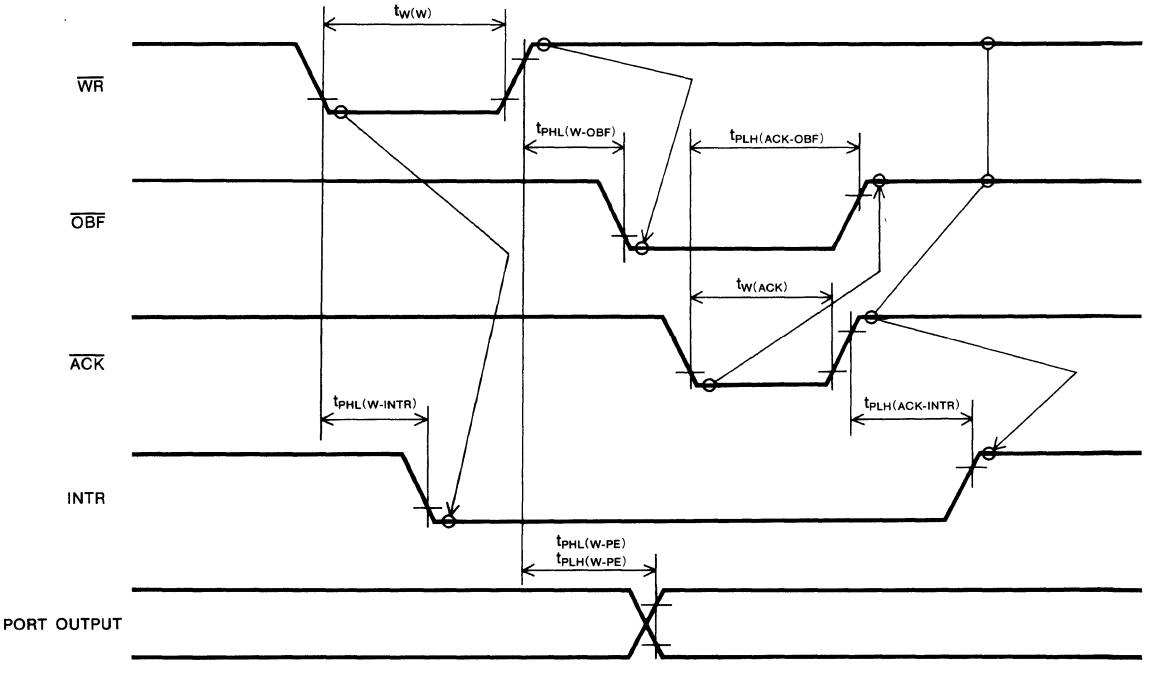
Mode 0, 1 Port Output



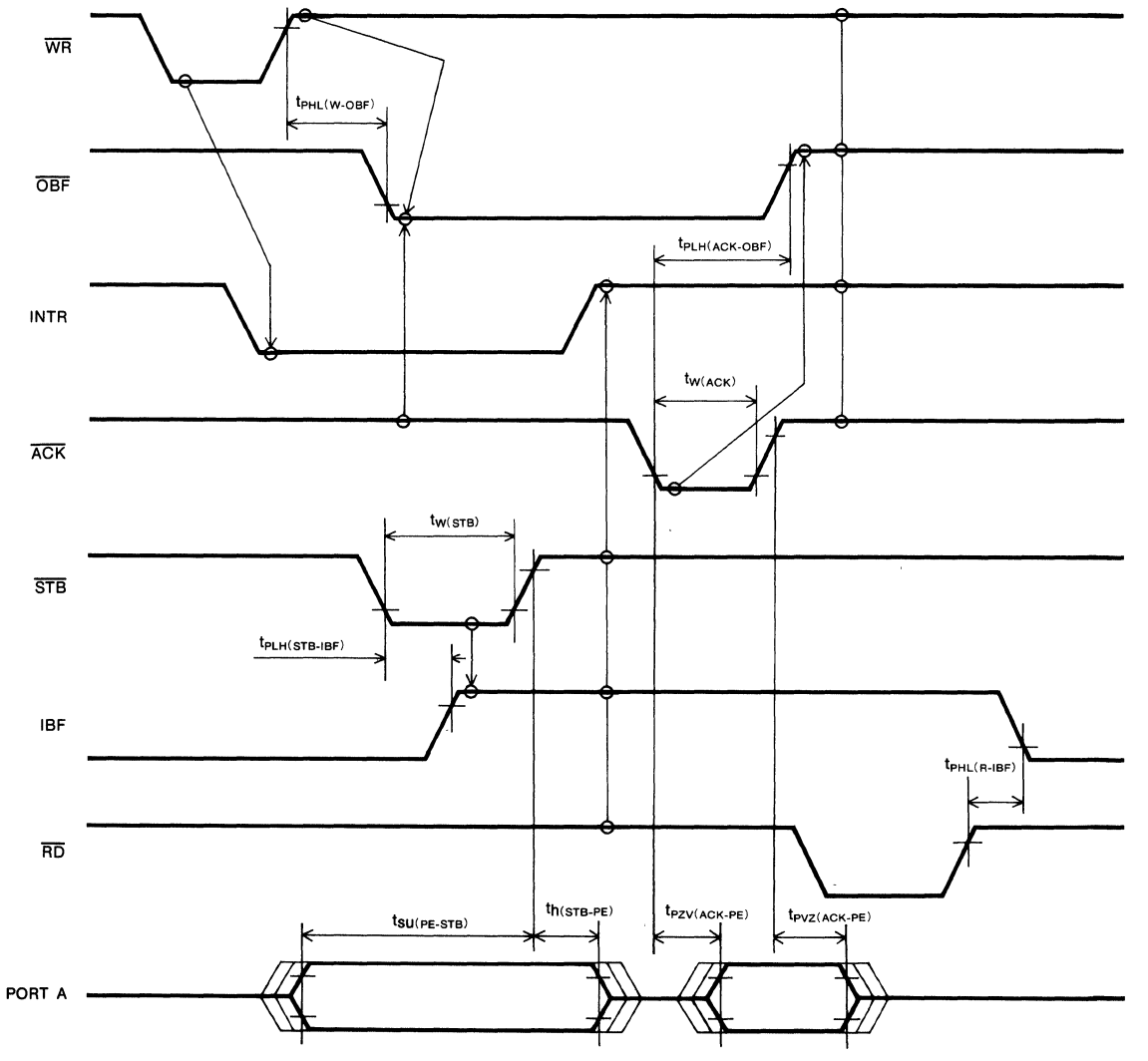
Mode 1 Strobed Input



Mode 1 Strobed Output

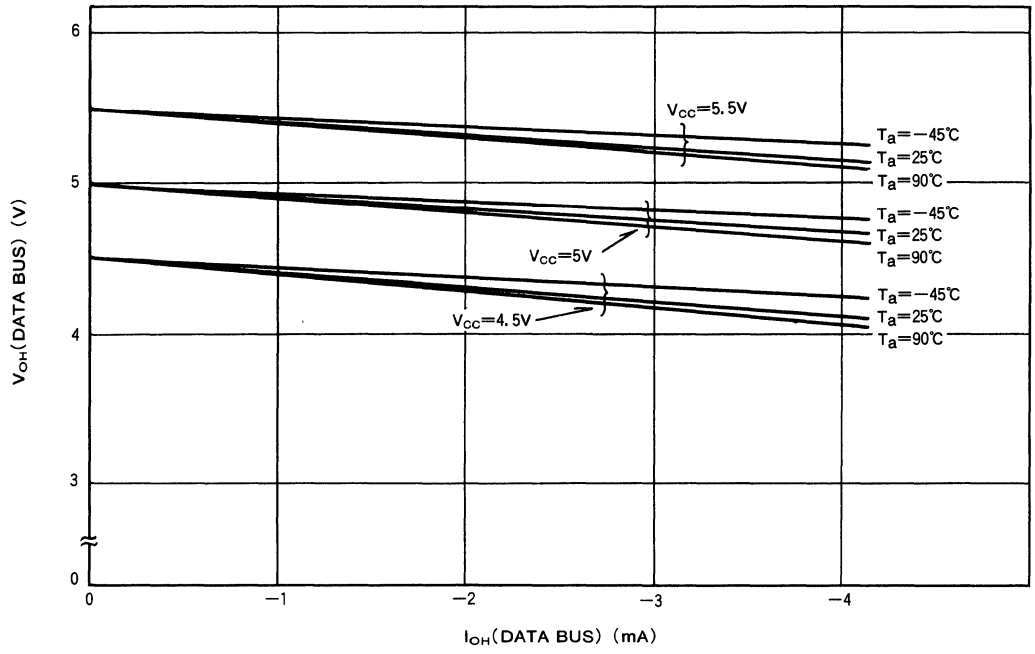


Mode 2 Bidirectional

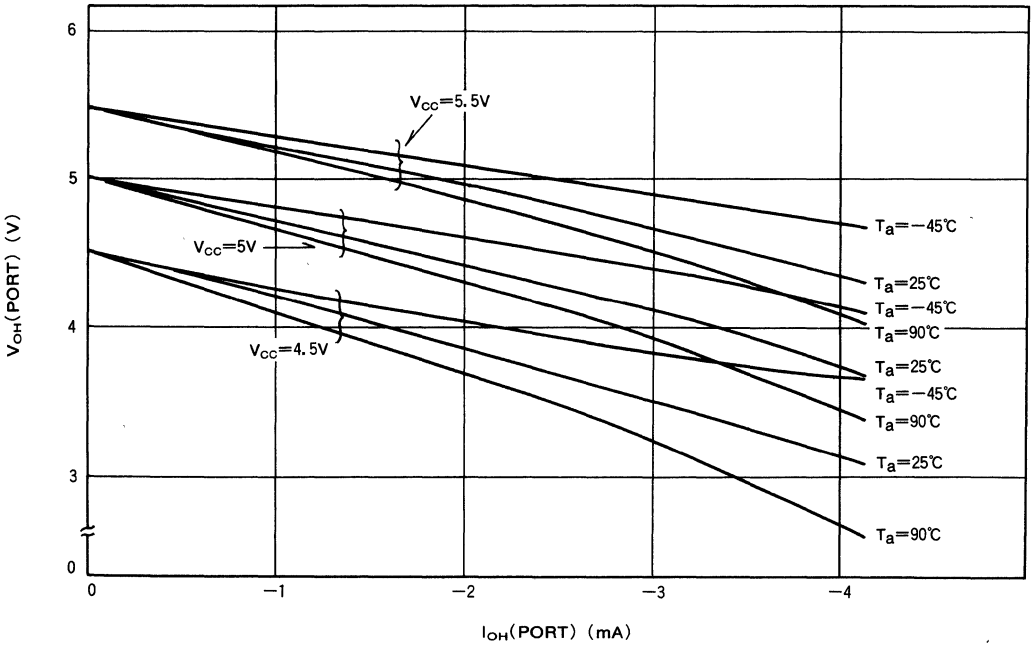


Note 13 : INTR=IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$+$\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$

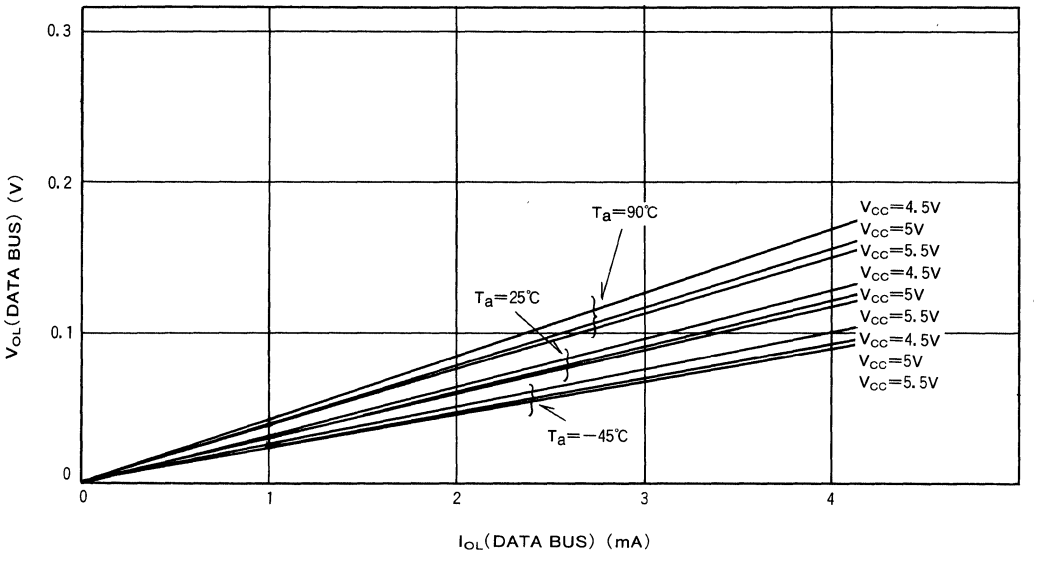
V_{OH}—I_{OH} CHARACTERISTICS (DATA BUS)



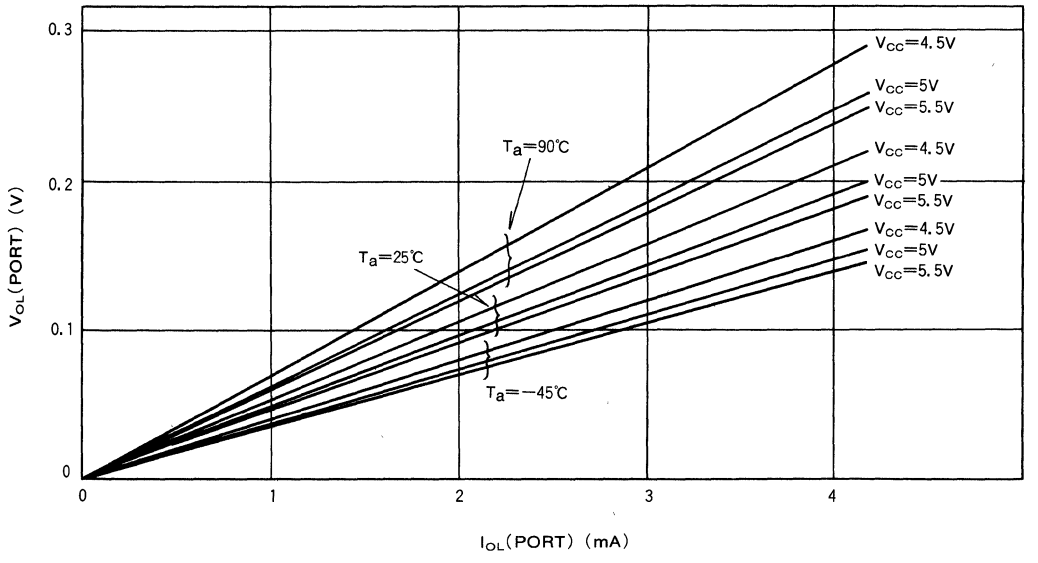
V_{OH}—I_{OH} CHARACTERISTICS (PORT)



V_{OL}—I_{OL} CHARACTERISTICS (DATA BUS)



V_{OL}—I_{OL} CHARACTERISTICS (PORT)



M5M82C59AP-2/FP-2/J-2

CMOS PROGRAMMABLE INTERRUPT CONTROLLER

DESCRIPTION

The M5M82C59AP-2 is a programmable LSI for interrupt control. It is fabricated using silicon-gate CMOS technology.

It is housed in a 28-pin plastic molded DIP.

And preparatory for surface equipment M5M82C59AFP-2 (SOP) and M5M82C59AJ-2 (PLCC).

FEATURES

- Single 5V supply voltage
- TTL compatible
- Pin connection compatible with the M5L8259AP
- CALL instruction to the CPU is generated automatically
- Priority, interrupt mask and vectored address for each interrupt request input are programmable
- Up to 64 levels of interrupt requests can be controlled by cascading with M5M82C59AP-2
- Polling functions

APPLICATION

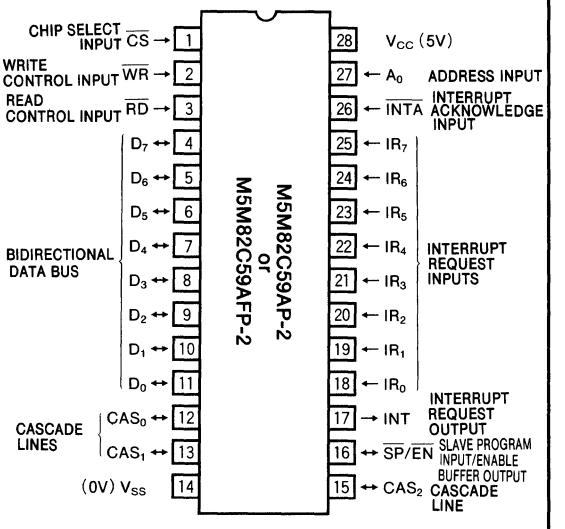
The M5M82C59AP-2 can be used as an interrupt controller for MELPS85, MELPS86 and MELPS88

FUNCTION

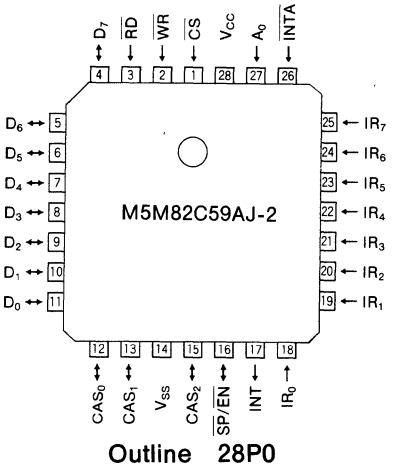
The M5M82C59AP-2 is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight level requests and has built-in features for expandability to other M5M82C59AP-2's. The priority and interrupt mask can be changed or reconfigured at any time by the main program.

When an interrupt is generated because of an interrupt request at 1 of the pins, the M5M82C59AP-2 based on the mask and priority will output an INT to the CPU. After that, when an $\overline{INTA}$ signal is received from the CPU or the system controller, a CALL instruction and a programmed vector address is released onto the data bus.

PIN CONFIGURATION (TOP VIEW)

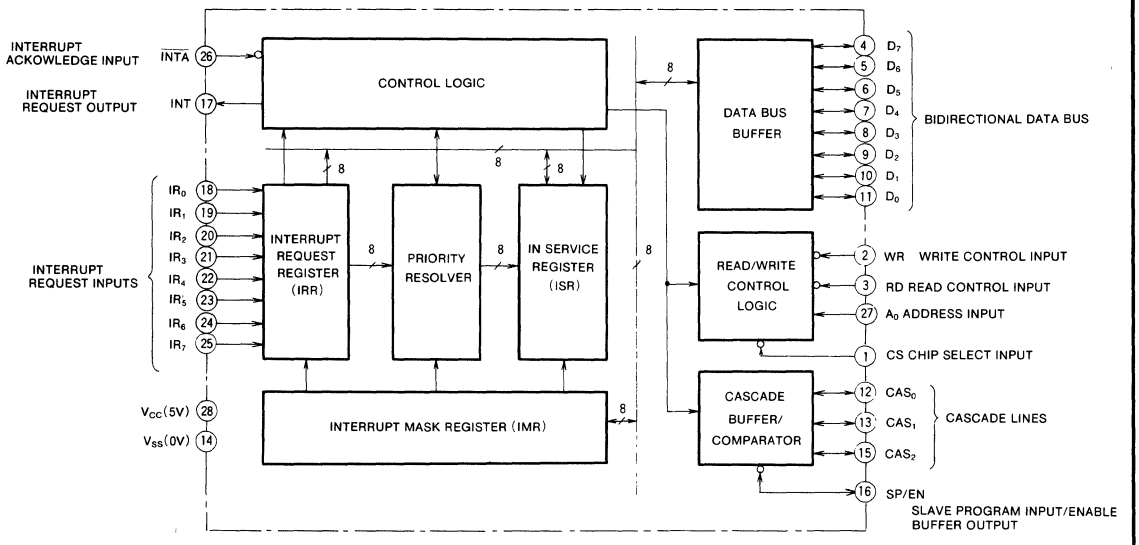


Outline 28P4 (M5M82C59AP-2)
28P2W (M5M82C59AFP-2)



Outline 28P0

BLOCK DIAGRAM



PIN DESCRIPTION

Symbol	Pin name	Input or output	Functional significance
$\overline{CS}$	Chip select input	Input	This input is active at low-level, but may be at high-level during interrupt request input and interrupt processing.
$\overline{WR}$	Write control input	Input	Command write control input from the CPU
$\overline{RD}$	Read control input	Input	Data read control input for the CPU
$D_7 \sim D_0$	Bidirectional data bus	Input/ output	Data and commands are transmitted through this bidirectional data bus to and from the CPU
$CAS_2 \sim CAS_0$	Cascade lines	Input/ output	These pins are outputs for a master and inputs for a slave. And these pins of the master will be able to address each individual slave. The master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of $\overline{INTA}$.
$\overline{SP}/\overline{EN}$	Slave program input/ Enable buffer output	Input/ output	SP: In normal mode, a master is designated when $\overline{SP}/\overline{EN}$="H" and a slave is designated when $\overline{SP}/\overline{EN}$="L". EN: In the buffered mode, whenever the M5M82C59AP-2's data bus output is enabled, its $\overline{SP}/\overline{EN}$ pin will go low-level.
INT	Interrupt request output	Output	This pin goes high-level whenever a valid interrupt is asserted.
$IR_7 \sim IR_0$	Interrupt request input	Input	The asynchronous interrupt inputs are active at high-level. The interrupt mask and priority of each interrupt input can be changed at any time. When using edge triggered mode, the rising edge (low-level to high-level) of the interrupt request and the high-level must be held until the first $\overline{INTA}$. For level triggered mode, the high-level must be held until the first $\overline{INTA}$
$\overline{INTA}$	Interrupt acknowledge input	Input	When an interrupt acknowledge ($\overline{INTA}$) from the CPU is received, the M5M82C59AP-2 releases a CALL instruction or vectored address onto the data bus.
A_0	A_0 address input	Input	This pin is normally connected to one of the address lines and acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ when writing commands or reading status registers.

OPERATION

The M5M82C59AP-2 is interfaced with a standard system bus as shown in Fig. 1 and operates as an interrupt controller.

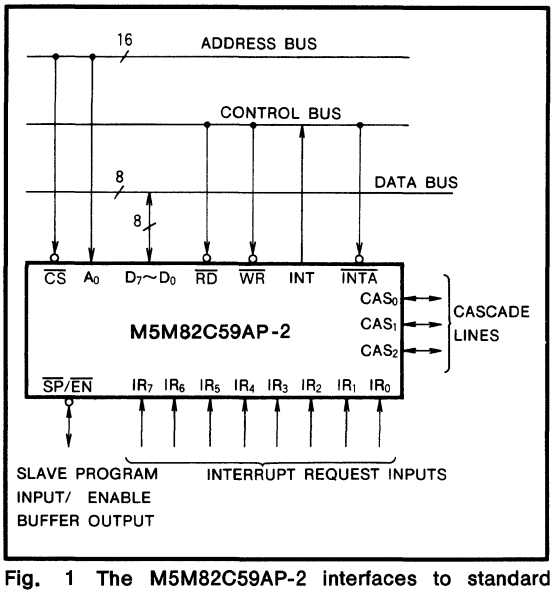


Fig. 1 The M5M82C59AP-2 interfaces to standard system bus.

Table 1 M5M82C59AP-2 basic operation

A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input operation (read)
0			L	H	L	IRR, ISR or interrupting level→data bus
1			L	H	L	IMR→Data bus
						Output operation (write)
0	0	0	H	L	L	Data bus→OCW2
0	0	1	H	L	L	Data bus→OCW3
0	1	X	H	L	L	Data bus→ICW1
1	X	X	H	L	L	Data bus→OCW1, ICW2, ICW3, ICW4
						Disable function
X	X	X	H	H	L	Data bus→High-impedance
X	X	X	X	X	H	Data bus→High-impedance

Interrupt Sequence

1. When the CPU is a MELPS85

(1) When one or more of the interrupt request inputs are raised high, the corresponding IRR bit(s) for the high-level inputs will be set.

(2) Mask state and priority levels are considered and, if appropriate, the M5M82C59AP-2 sends an INT signal to the CPU.

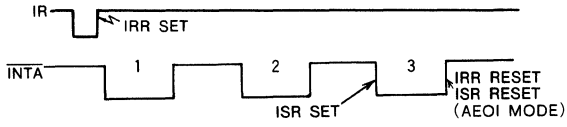
(3) The acknowledgement of the CPU to the INT signal, the CPU issues an $\overline{INTA}$ pulse to the M5M82C59AP-2.

(4) Upon receiving the first $\overline{INTA}$ pulse from the CPU, a CALL instruction is released onto the data bus.

(5) A CALL is a 3-byte instruction, so additional two $\overline{INTA}$ pulses are issued to the M5M82C59AP-2 from the CPU.

(6) These two $\overline{INTA}$ pulses allow the M5M82C59AP-2 to release the program address onto the data bus. The low-order 8 bits vectored address is released at the second $\overline{INTA}$ pulse and the high-order 8 bits vectored address is released at the third $\overline{INTA}$ pulse. The ISR bit corresponding to the interrupt request input is set upon receiving the third $\overline{INTA}$ pulse from the CPU, and the corresponding IRR bit is reset.

(7) This completes the 3-byte CALL instruction and the interrupt routine will be serviced. The ISR bit is reset at the trailing edge of the third $\overline{INTA}$ pulse in the AEOI mode. In the other modes the ISR bit is not reset until an EOI command is issued.



2. When the CPU is a MELPS86 or MELPS88

(1) When one or more of the interrupt request inputs are raised high, the corresponding IRR bit(s) for the high-level inputs will be set.

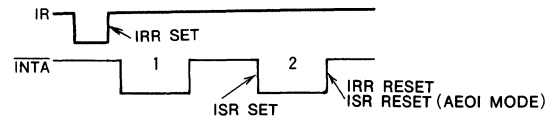
(2) Mask state and priority levels are considered and if appropriated, the M5M82C59AP-2 sends an INT signal to the CPU.

(3) As an acknowledgement to the INT signal, the CPU issues an $\overline{INTA}$ pulse to the M5M82C59AP-2.

(4) Upon receiving the first $\overline{INTA}$ pulse from the CPU, the M5M82C59AP-2 does not drive the data bus, and the data bus keeps high-impedance state.

(5) When the second $\overline{INTA}$ pulse is issued from the CPU, an 8-bit pointer is released onto the data bus.

(6) This completes the interrupt cycle and the interrupt routine will be serviced. The ISR bit is reset at the trailing edge of the second $\overline{INTA}$ pulse in the AEOI mode. In the other modes the ISR bit is not reset until an EOI command is issued from the CPU.



The interrupt request input must be held at high-level until the first $\overline{INTA}$ pulse is issued. If it is allowed to return to low-level before the first $\overline{INTA}$ pulse is issued, an interrupt request in IR_7 is executed However, in this case the ISR bit is not set.

This is a function for a noise countermeasure of interrupt request inputs. In the interrupt routine of IR_7, if ISR is checked by software either the interrupt by noise or real interrupt can be acknowledged. In the state of edge trigger mode normally the interrupt request inputs hold high-level and its input low-level pulse in the case of interrupt.

Interrupt sequence outputs

1. When the CPU is a MELPS85

A CALL instruction is released onto the data bus when the first $\overline{INTA}$ pulse is issued. The low-order 8 bits of the vectored address are released when the second $\overline{INTA}$ pulse is issued, and the high-order 8 bits are released when the third $\overline{INTA}$ pulse is issued. The format of these three outputs is shown in Table 2.

Table 2 Formats of interrupt CALL instruction and vectored address

First $\overline{INTA}$ pulse (CALL instruction)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	1	1	0	1

Second $\overline{INTA}$ pulse (low-order 8 bits of vectored address)

IR	Interval= 4							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_0	A_7	A_6	A_5	0	0	0	0	0
IR_1	A_7	A_6	A_5	0	0	1	0	0
IR_2	A_7	A_6	A_5	0	1	0	0	0
IR_3	A_7	A_6	A_5	0	1	1	0	0
IR_4	A_7	A_6	A_5	1	0	0	0	0
IR_5	A_7	A_6	A_5	1	0	1	0	0
IR_6	A_7	A_6	A_5	1	1	0	0	0
IR_7	A_7	A_6	A_5	1	1	1	0	0

IR	Interval=8							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_0	A_7	A_6	0	0	0	0	0	0
IR_1	A_7	A_6	0	0	1	0	0	0
IR_2	A_7	A_6	0	1	0	0	0	0
IR_3	A_7	A_6	0	1	1	0	0	0
IR_4	A_7	A_6	1	0	0	0	0	0
IR_5	A_7	A_6	1	0	1	0	0	0
IR_6	A_7	A_6	1	1	0	0	0	0
IR_7	A_7	A_6	1	1	1	0	0	0

Third $\overline{INTA}$ pulse (high-order 8 bits of vectored address)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8

2. When the CPU is a MELPS86 or MELPS88

The data bus keeps a high-impedance state when the first $\overline{INTA}$ pulse is issued. Then the pointer $T_7 \sim T_0$ is released when the next $\overline{INTA}$ pulse is issued. The content of the pointer $T_7 \sim T_0$ is shown in Table 3. The $T_2 \sim T_0$ are a binary code corresponding to the interrupt request level, $A_{10} \sim A_5$ are unused and ADI mode control is ignored.

Table 3 Contents of interrupt pointer

Second $\overline{INTA}$ pulse (8-bit pointer)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_0	T_7	T_6	T_5	T_4	T_3	0	0	0
IR_1	T_7	T_6	T_5	T_4	T_3	0	0	1
IR_2	T_7	T_6	T_5	T_4	T_3	0	1	0
IR_3	T_7	T_6	T_5	T_4	T_3	0	1	1
IR_4	T_7	T_6	T_5	T_4	T_3	1	0	0
IR_5	T_7	T_6	T_5	T_4	T_3	1	0	1
IR_6	T_7	T_6	T_5	T_4	T_3	1	1	0
IR_7	T_7	T_6	T_5	T_4	T_3	1	1	1

Interrupt Request Register (IRR), In-service Register (ISR)

As interrupt requests are received at inputs $IR_7 \sim IR_0$, the corresponding bits of IRR are set and as an interrupt request is serviced the corresponding bit of ISR is set. The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are being serviced. The status of these two registers can be read. These two registers are connected through the priority resolver.

An interrupt requst received by IR_n is acknowledged on the leading edge when in the edge triggered mode or it is acknowledged on the level when in the level triggered mode. After that an INT signal is released and the interrupt request signal is latched in the corresponding IRR bit if the high-level is held until the first $\overline{INTA}$ pulse is issued. It is important to remember that the interrupt request signal must be held at high-level until the first $\overline{INTA}$ pulse is issued.

The interrupt request latching in the IRR causes a signal to be sent to the priority resolver unless it is masked out. When the priority resolver receives the signals it selects the highest priority interrupt request latched in IRR. The ISR is set when the last $\overline{INTA}$ pulse is issued while the corresponding bit of IRR is reset and the other bits of IRR are unaffected.

The bit of ISR that was set is not reset during the interrupt routine, but is reset at the end of the routine by the EOI command (end of interrupt) or by the trailing edge of the last $\overline{INTA}$ pulse in AEOI mode.

Priority Resolver

The priority resolver examines all of the interrupt requests set in IRR to determine and selects the highest priority. The ISR bit corresponding to the selected (highest priority) request is set by the last $\overline{INTA}$ pulse.

Interrupt Mask Register (IMR)

The contents of the interrupt mask register are used to mask out (disable) interrupt requests of selected interrupt request pins. Each terminal is independently masked so that masking a high priority interrupt does not influence the lower or higher priority interrupts. Therefore the contents of IMR selectively enable reading.

Interrupt Request Output (INT)

The interrupt request output connects directly to the interrupt input of the CPU. The output level is compatible with the input level required for the CPUs.

The INT output is set to low-level after the interrupt sequence ends, irrespective of the current mode. When the power is turned on, the INT output (high-level output) may appear but is reset to low-level by executing ICW1.

Interrupt Acknowledge Input ($\overline{INTA}$)

The CALL instruction and vectored address are released onto the data bus by the $\overline{INTA}$ pulse.

Data Bus Buffer

The data bus buffer is a 3-state bidirectional data bus buffer that is used to interface with the system bus. Write commands to the M5M82C59AP-2, CALL instructions, vectored addresses, status information, etc. are transferred through the data bus buffer.

Read/Write Control Logic

The read/write control logic is used to control functions such as receiving commands from the CPU and supplying status information to the data bus.

Chip Select Input ($\overline{CS}$)

The M5M82C59AP-2 is selected (enabled) when $\overline{CS}$ is at low-level, but during interrupt request input or interrupt processing it may be high-level.

Write Control Input ($\overline{WR}$)
When $\overline{WR}$ goes to low-level the M5M82C59AP-2 can be written.

Read Control Input ($\overline{RD}$)
When $\overline{RD}$ goes low-level status information in the internal register of the M5M82C59AP-2 can be read through the data bus.

Address Input (A_0)
The address input is normally connected with one of the address lines and is used along with $\overline{WR}$ and $\overline{RD}$ to control write commands and reading status information.

Cascade Buffer/Comparator
The cascade buffer/comparator stores or compares identification codes. The three cascade lines are output when the M5M82C59AP-2 is a master or input when it is a slave. The identification code on the cascade lines select it as master or slave.

PROGRAMMING THE M5M82C59AP-2

The M5M82C59AP-2 is programmed through the Initialization Command Word (ICW) and the Operation Command Word (OCW). The following explains the functions of these two commands.

Initialization Command Words (ICW_S)
The initialization command word is used for the initial setting of the M5M82C59AP-2. There are four commands in this group and the following explains the details of these four commands. The command flow of ICWs is shown Fig. 2.

ICW1
The meaning of the bits of ICW1 is explained in Fig. 3 along with the functions. ICW1 contains vectored address bits $A_7 \sim A_5$, a flag indicating whether interrupt input is edge triggered or level triggered, CALL address interval, whether a single M5M82C59AP-2 or the cascade mode is used, and whether ICW4 is required or not.
Whenever a command is issued with $A_0=0$ and $D_4=1$, this is interpreted as ICW1 and the following will automatically occur.
(a) The interrupt mask register (IMR) is cleared.
(b) The interrupt request input IR_7 is assigned the lowest priority.
(c) The special mask mode is cleared and the status read is set to the interrupt request register (IRR).
(d) When IC4=0 all bits in ICW4 are set to 0.

ICW2
ICW2 contains vectored address bits $A_{15} \sim A_8$ or interrupt type $T_7 \sim T_3$, and the format is shown in Fig. 3.

ICW3
When SNGL = 1 it indicates that only a single M5M82C59AP-2 is used in the system, in which case ICW3 is not valid. When SNGL = 0, ICW3 is valid and indicates cascade connections with other M5M82C59AP-2 devices. In the master mode, a 1 is set for each slave.
When the CPU is a MELPS85 the CALL instruction is released from the master at the first $\overline{INTA}$ pulse and the vectored address is released onto the data bus from the slave at the second and third $\overline{INTA}$ pulses.
When the CPU is a MELPS86 the master and slave are in high-impedance at the first $\overline{INTA}$ pulse and the pointer is

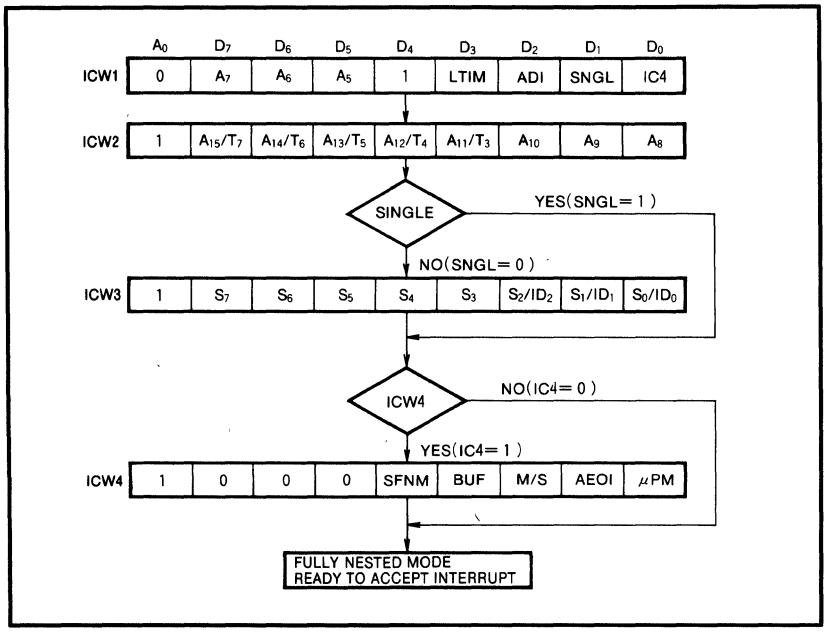


Fig. 2 Initialization sequence

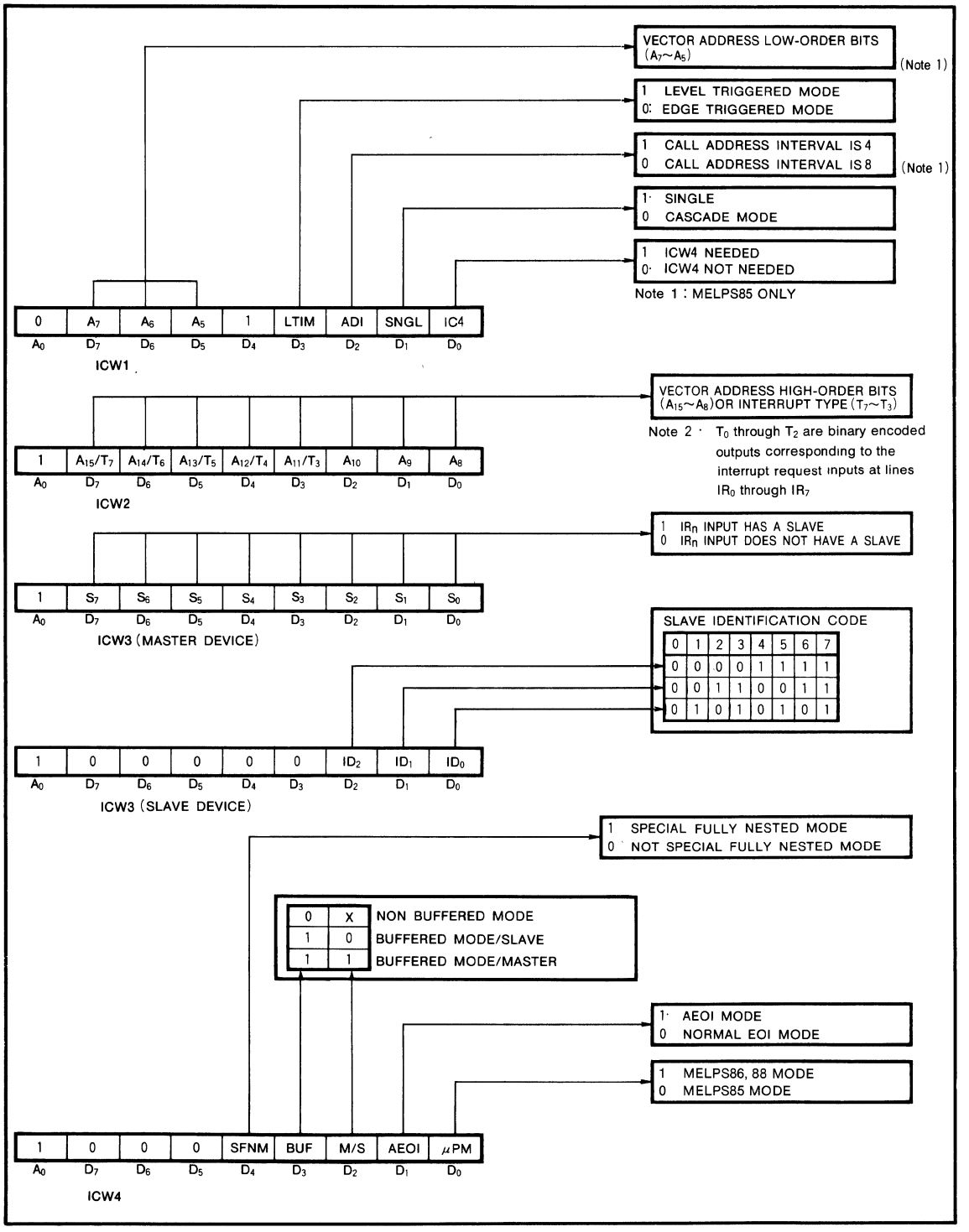


Fig. 3 Initialization command word format

released onto the data bus from the slave at the second $\overline{INTA}$ pulse.

The master mode is specified when $\overline{SP}/\overline{EN}$ pin is high-level or BUF=1 and M/S=1 in ICW4, and slave mode is specified when $\overline{SP}/\overline{EN}$ pin is low-level or BUF=1 and M/S =0 in ICW4. In the slave mode, 3-bit $ID_2 \sim ID_0$ identify the slave. And then when the slave code released on the cascade lines from the master, matches the assigned ID code, the vectored address is released by it onto the data bus at the next $\overline{INTA}$ pulse

ICW4

Only when IC4=1 in ICW1 is ICW4 valid. Otherwise all bits are set to 0. When ICW4 is valid it specifies special fully nested mode, buffer mode master/slave, automatic EOI and microprocessor mode. The format of ICW4 is shown in Fig. 3.

Operation Command Words (OCW_S)

The operation command words are used to change the contents of IMR, the priority of interrupt request inputs and the special mask. After the ICW are programmed into the M5M82C59AP-2, the device is ready to accept interrupt requests. There are three types of OCW_S; explanation of each follows, and the format of OCW_S is shown in Fig 4

OCW1

The meaning of the bits of OCW1 are explained in Fig. 4 along with their functions. Each bit of IMR can be indepen-

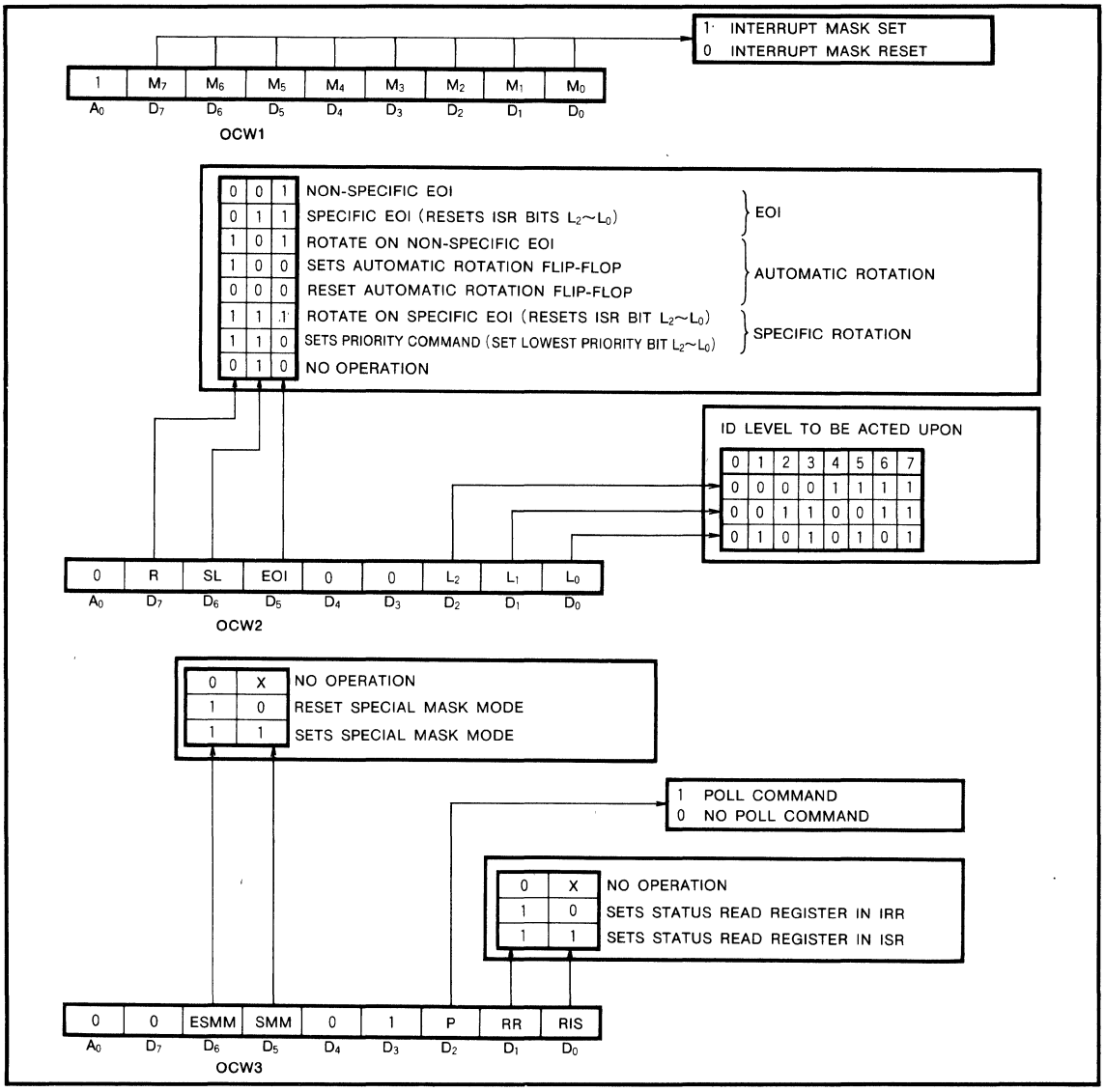


Fig. 4 Operation command word format

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dently changed (set or reset) by OCW1.

OCW2

The OCW2 is used for issuing EOI commands to the M5M82C59AP-2 and for changing the priority of the interrupt request inputs.

OCW3

The OCW3 is used for specifying special mask mode, poll mode and status register read.

FUNCTION OF COMMAND

Interrupt masks

The mask register contains a mask for each individual interrupt request. These interrupt masks can be changed by programming using OCW1.

Special mask mode

When an interrupt request is acknowledged and the ISR bit corresponding to the interrupt request is not reset by EOI command (which means an interrupt service routine is executing) lower priority interrupt requests are ignored.

In special mask mode interrupt requests received at interrupt request inputs which are masked by OCW1 are disabled, but interrupts at all levels that are not masked are possible. This means that in the mask mode all level of interrupts are possible or individual inputs can be selectively programmed so all interrupts at the selected inputs are disabled. The masks are stored in IMR and special mask is set/reset by executing OCW3.

Buffered mode

The buffered mode will structure the M5M82C59AP-2 to send an enable signal on $\overline{SP}/\overline{EN}$ to enable the data bus buffer, when the data bus requires the data bus buffer or when cascading mode is used. In this mode, when data bus output of the M5M82C59AP-2 is enabled, the $\overline{SP}/\overline{EN}$ output becomes low-level. This allows the M5M82C59AP-2 to be programmed whether it is a master or a slave by software. The buffered mode is set/reset by executing ICW4.

Fully nested mode

The fully nested mode is the mode when no mode is specified and is the usual operational mode. In this mode, the priority of interrupt request terminals is fixed from the lowest IR_7 to the highest IR_0. When an interrupt request is acknowledged the CALL instruction and vectored address are released onto the data bus. At the same time the ISR bit corresponding to the accepted interrupt request is set. This ISR bit remains set until it is reset by the input of an EOI command or until the trailing edge of last $\overline{INTA}$ pulse in AEOI mode. While an interrupt service routine is being executed, interrupt requests of same or lower priority are disabled while the bit of ISR remains set. The priorities can be changed by OCW2.

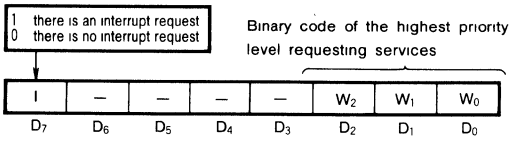
Special fully nested mode

The special fully nested mode will be used when cascading is used and this mode will be programmed to the master by ICW4. The special fully nested mode is the same as the fully nested mode with the following two exceptions.

1. When an interrupt from a certain slave is being serviced, this slave is not locked out from the master priority logic. Higher priority interrupts within the slave will be recognized by the master and the master will initiate an interrupt request to the CPU. In general in the normal fully nested mode, a serviced slave is locked out from the master's priority, and so higher priority interrupts from the same slave are not serviced.
2. When an interrupt from a certain slave is being serviced the software must check ISR to determine if there are additional interrupts requests to be serviced. If the ISR bit is 0 the EOI command may be sent to the master too. But if it is not 0 the EOI command should not be sent to the master.

Poll mode

The poll mode is useful when the internal enable flip-flop of the microprocessor is reset, and interrupt input is disabled. Service to the device is achieved by a programmer initiative using a poll command. In the poll mode the M5M82C59AP-2 at the next $\overline{RD}$ pulse puts 8-bit on the data bus which indicates whether there is an interrupt request and reads the priority level. The format of the information on the data bus is as shown below.



When I=0 (no interrupt request), $W_2 \sim W_0$ is 111. The poll is valid from $\overline{WR}$ to $\overline{RD}$ and interrupt is frozen. This mode can be used for processing common service routines for interrupts from more than one line and does not require any $\overline{INTA}$ sequence. Poll command is issued by setting P=1 in OCW3.

End Of Interrupt (EOI) and Specific EOI (SEOI)

An EOI command is required by the M5M82C59AP-2 to reset the ISR bit. So an EOI command must be issued to the M5M82C59AP-2 before returning from an interrupt service routine.

When AEOI is selected in ICW4, the ISR bit can be reset at the trailing edge of the last $\overline{INTA}$ pulse. When AEOI is not selected the ISR bit is reset by the EOI command issued to the M5M82C59AP-2 before returning from an interrupt service routine. When programmed in the cascade mode the EOI command must be issued to the master once and to corresponding slave once.

There are two forms of EOI command, specific EOI and non-specific EOI. When the M5M82C59AP-2 is used in the fully nested mode, the ISR bit being serviced is reset by the EOI command. When the non-specific EOI is issued the M5M82C59AP-2 will automatically reset the highest ISR bit

of those that are set. Other ISR bits are reset by a specific EOI and the bit to be reset is specified in the EOI by the program. The SEOI is useful in modes other than fully nested mode. When the M5M82C59AP-2 is in special mask mode ISR bits masked in IMR are not reset by EOI. EOI and SEOI are selected when OCW2 is executed.

Automatic EOI (AEOI)

In the AEOI mode the M5M82C59AP-2 executes non-specific EOI command automatically at the trailing edge of the last $\overline{INTA}$ pulse. When AEOI = 1 in ICW4, the M5M82C59AP-2 is put in AEOI mode continuously until re-programmed in ICW4.

Automatic rotation

The automatic rotation mode is used in applications where many interrupt requests of the same level are expected such as multichannel communication systems In this mode when an interrupt request is serviced, that request is assigned the lowest priority so that if there are other interrupt requests they will have higher priorities. This means that the next request on the interrupt request being serviced must wait until the other interrupt requests are serviced (worst case is waiting for all 7 of the other controllers to be serviced). The priority and serving status are rotated as shown in Fig. 5.

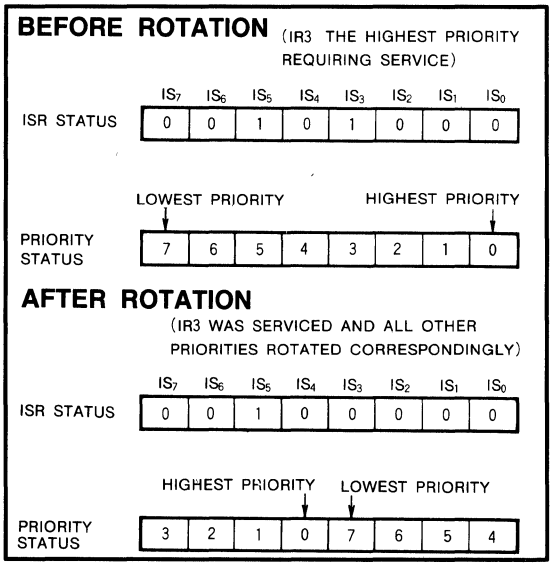


Fig. 5 An example of priority rotation

In the non-specific EOI command automatic rotation mode is selected when R=1, EOI=1, SL=0 in OCW2. The internal priority status is changed by EOI or AEOI commands. The rotation priority A flip-flop is set by R=1, EOI=0 and SL=0 which is useful when the M5M82C59AP-2 is used in the AEOI mode.

Specific rotation

Specific rotation gives the user versatile capabilities in interrupt controlled operations. It serves in those applications in which a specific device's interrupt priority must be altered. As opposed to automatic rotation which automatically sets priorities, specific rotation is completely user controlled. That is, the user selects the interrupt level that is to receive lowest or highest priority. Priority changes can be executed during an EOI command.

Level triggered mode/Edge triggered mode

Selection of level or edge triggered mode of the M5M82C59AP-2 is made by ICW1, When using edge triggered mode not only is a transition from low-level to high-level required, but the high-level must be held until the first $\overline{INTA}$. If the high-level is not held until the first $\overline{INTA}$, the interrupt request will be treated as if it were input on IR_7, except that the ISR bit is not set. When level triggered mode is used the functions are the same as edge triggered mode except that the transition from low-level to high-level is not required to trigger the interrupt request.

In the level triggered mode and using AEOI mode together, if the high-level is held too long the interrupt will occur immediately. To avoid this situation interrupts should be kept disabled until the end of the service routine or until the IR input returns low-level. In the edge triggered mode this type of mistake is not possible because the interrupt request is edge triggered.

Reading the M5M82C59AP-2 internal status

The contents of IRR and ISR can be read by the CPU with status read. When an OCW3 is issued to the M5M82C59AP-2 and an $\overline{RD}$ pulse issued the contents of IRR or ISR can be released onto the data bus. A special command is not required to read the contents of IMR. The contents of IMR can be released onto the data bus by issuing an $\overline{RD}$ pulse when A_0=1. There is no need to issue a read register command every time the IRR or ISR is to be read. Once a read register command is received by the M5M82C59AP-2, it remains valid until it is changed. Remember that the programmer must issue a poll command every time to check whether there is an interrupt request and read the priority level. Polling overrides status read when P=1, RR=1 in OCW3.

CASCADING

The M5M82C59AP-2 can be interconnected in a system of one master with up to 8 slaves to handle up to 64 priority levels. A system of 3 units that can be used with the MELPS85 is shown in Fig. 6.

The master can select a slave by outputting its identification code through the 3 cascade lines. The INT output of each slave is connected to the master interrupt request inputs. When an interrupt request of one of the slaves is to be serviced the master outputs the identification code of the slave through the cascade lines, so the slave will release the vectored address on the next $\overline{INTA}$ pulse.

The cascade lines of the master are nomally low-level, and will contain the slave identification code from the leading edge of the first $\overline{INTA}$ pulse to the trailing edge of the last $\overline{INTA}$ pulse. The master and slave can be programmed to work in different modes. ICWs must be issued for each device, and EOI commands must be issued twice: once for the master and once for the corresponding slave. Each $\overline{CS}$ of the M5M82C59AP-2 requires an address decoder.

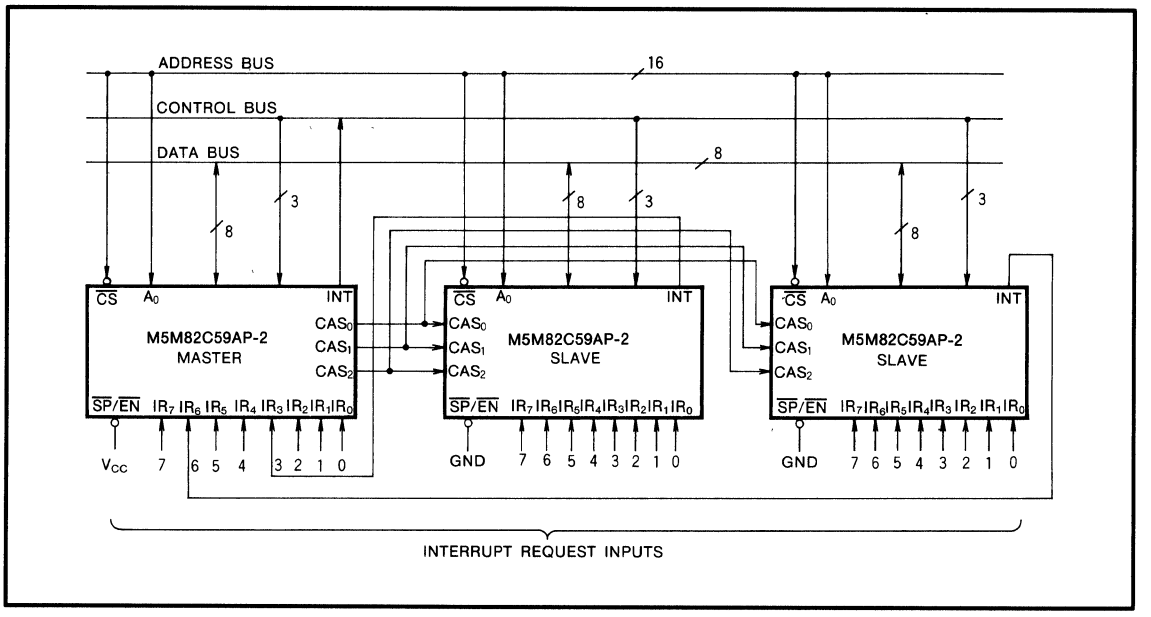
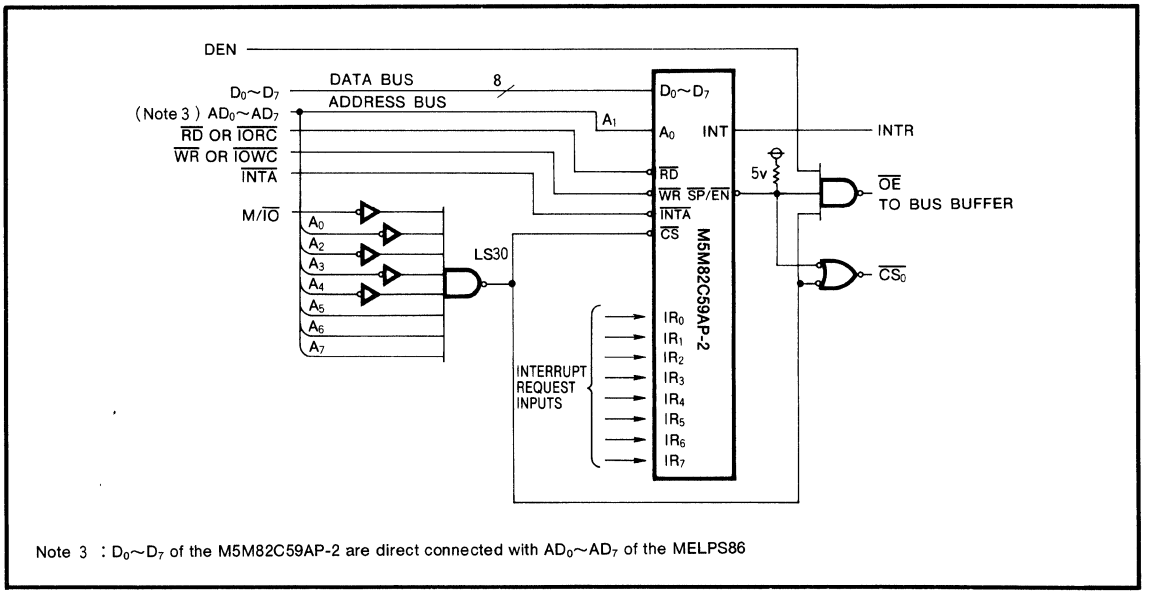


Fig. 6 Cascading the M5M82C59AP-2



Note 3 : D_0~D_7 of the M5M82C59AP-2 are direct connected with AD_0~AD_7 of the MELPS86

Fig. 7 Example of interface with the MELPS86

INSTRUCTION SET

Item / Number	Mnemonic	Instruction code									Function			
		A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	ICW4 required	Intervel	Single	Trigger
1	ICW1 A	0	A_7	A_6	A_5	1	0	1	1	0	N	4	Y	E
2	ICW1 B	0	A_7	A_6	A_5	1	1	1	1	0	N	4	Y	L
3	ICW1 C	0	A_7	A_6	A_5	1	0	1	0	0	N	4	N	E
4	ICW1 D	0	A_7	A_6	A_5	1	1	1	0	0	N	4	N	L
5	ICW1 E	0	A_7	A_6	0	1	0	0	1	0	N	8	Y	E
6	ICW1 F	0	A_7	A_6	0	1	1	0	1	0	N	8	Y	L
7	ICW1 G	0	A_7	A_6	0	1	0	0	0	0	N	8	N	E
8	ICW1 H	0	A_7	A_6	0	1	1	0	0	0	N	8	N	L
9	ICW1 I	0	A_7	A_6	A_5	1	0	1	1	1	Y	4	Y	E
10	ICW1 J	0	A_7	A_6	A_5	1	1	1	1	1	Y	4	Y	L
11	ICW1 K	0	A_7	A_6	A_5	1	0	1	0	1	Y	4	N	E
12	ICW1 L	0	A_7	A_6	A_5	1	1	1	0	1	Y	4	N	L
13	ICW1 M	0	A_7	A_6	0	1	0	0	1	1	Y	8	Y	E
14	ICW1 N	0	A_7	A_6	0	1	1	0	1	1	Y	8	Y	L
15	ICW1 O	0	A_7	A_6	0	1	0	0	0	1	Y	8	N	E
16	ICW1 P	0	A_7	A_6	0	1	1	0	0	1	Y	8	N	L
17	ICW2	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	8-bit vectored address			
18	ICW3 M	1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	Slave connections (master mode)			
19	ICW3 S	1	0	0	0	0	0	ID_2	ID_1	ID_0	Slave identification code (slave mode)			
											SFNM	BUF	AEOI	MELPS86
20	ICW4 A	1	0	0	0	0	0	0	0	0	N	N	N	N
21	ICW4 B	1	0	0	0	0	0	0	0	1	N	N	N	Y
22	ICW4 C	1	0	0	0	0	0	0	1	0	N	N	Y	N
23	ICW4 D	1	0	0	0	0	0	0	1	1	N	N	Y	Y
24	ICW4 E	1	0	0	0	0	0	1	0	0	N	N	N	N
25	ICW4 F	1	0	0	0	0	0	1	0	1	N	N	N	Y
26	ICW4 G	1	0	0	0	0	0	1	1	0	N	N	Y	N
27	ICW4 H	1	0	0	0	0	0	1	1	1	N	N	Y	Y
28	ICW4 I	1	0	0	0	0	1	0	0	0	N	Y S	N	N
29	ICW4 J	1	0	0	0	0	1	0	0	1	N	Y S	N	Y
30	ICW4 K	1	0	0	0	0	1	0	1	0	N	Y S	Y	N
31	ICW4 L	1	0	0	0	0	1	0	1	1	N	Y S	Y	Y
32	ICW4 M	1	0	0	0	0	1	1	0	0	N	Y M	N	N
33	ICW4 N	1	0	0	0	0	1	1	0	1	N	Y M	N	Y
34	ICW4 O	1	0	0	0	0	1	1	1	0	N	Y M	Y	N
35	ICW4 P	1	0	0	0	0	1	1	1	1	N	Y M	Y	Y
36	ICW4 NA	1	0	0	0	1	0	0	0	0	Y	N	N	N
37	ICW4 NB	1	0	0	0	1	0	0	0	1	Y	N	N	Y
38	ICW4 NC	1	0	0	0	1	0	0	1	0	Y	N	Y	N
39	ICW4 ND	1	0	0	0	1	0	0	1	1	Y	N	Y	Y
40	ICW4 NE	1	0	0	0	1	0	1	0	0	Y	N	N	N
41	ICW4 NF	1	0	0	0	1	0	1	0	1	Y	N	N	Y
42	ICW4 NG	1	0	0	0	1	0	1	1	0	Y	N	Y	N
43	ICW4 NH	1	0	0	0	1	0	1	1	1	Y	N	Y	Y
44	ICW4 NI	1	0	0	0	1	1	0	0	0	Y	Y S	N	N
45	ICW4 NJ	1	0	0	0	1	1	0	0	1	Y	Y S	N	Y
46	ICW4 NK	1	0	0	0	1	1	0	1	0	Y	Y S	Y	N
47	ICW4 NL	1	0	0	0	1	1	0	1	1	Y	Y S	Y	Y
48	ICW4 NM	1	0	0	0	1	1	1	0	0	Y	Y M	N	N
49	ICW4 NN	1	0	0	0	1	1	1	0	1	Y	Y M	N	Y
50	ICW4 NO	1	0	0	0	1	1	1	1	0	Y	Y M	Y	N
51	ICW4 NP	1	0	0	0	1	1	1	1	1	Y	Y M	Y	Y
52	OCW1	1	M_7	M_6	M_5	M_4	M_3	M_2	M_1	M_0	Interrupt mask			
53	OCW2 E	0	0	0	1	0	0	0	0	0	EOI			
54	OCW2 SE	0	0	1	1	0	0	L_2	L_1	L_0	SEOI			
55	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate on Non-Specific EOI command (Automatic rotation)			
56	OCW2 RSE	0	1	1	1	0	0	L_2	L_1	L_0	Rotate on Specific EOI command (Specific rotation)			
57	OCW2 R	0	1	0	0	0	0	0	0	0	Rotate in AEOI Mode (SET)			
58	OCW2 CR	0	0	0	0	0	0	0	0	0	Rotate in AEOI Mode (CLEAR)			
59	OCW2 RS	0	1	1	0	0	0	L_2	L_1	L_0	Set priority without EOI			
60	OCW3 P	0	0	0	0	0	1	1	0	0	Poll Mode			
61	OCW3 RIS	0	0	0	0	0	1	0	1	1	Sets Status Read Register in ISR			
62	OCW3 RR	0	0	0	0	0	1	0	1	0	Sets Status Read Register in IRR			
63	OCW3 SM	0	0	1	1	0	1	0	0	0	Sets Special Mask Mode			
64	OCW3 RSM	0	0	1	0	0	1	0	0	0	Reset Special Mask Mode			

Note 4 · Y: yes, N: no, E. edge, L. level, M: master, S: slave

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	−0.3~7	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		−0.3~V_{CC}+0.3	V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current	2.5	mA
T_{opr}	Operating free-air temperature range		−20~75	℃
T_{stg}	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
		I_{OH}=−20μA	4.4			
$V_{OH(INT)}$	High-level output voltage, interrupt request output	I_{OH}=−400μA	2.4			V
		I_{OH}=−100μA	3.5			
		I_{OH}=−20μA	4.4			
V_{OL}	Low-level output voltage	I_{OL}=2.2mA			0.45	V
I_{CC}	Standby supply current from V_{CC}	V_I=0V, V_{CC} output open			10	μA
I_{IH}	High-level input current	V_I=V_{CC}	−10		10	μA
I_{IL}	Low-level input current	V_I=0V	−10		10	μA
I_{OZ}	Off-state output current	V_O=0V~V_{CC}	−10		10	μA
I_{LIR1}	IR pin input current	V_I=0V	−300			μA
I_{LIR2}	IR pin input current	V_I=V_{CC}			10	μA
Ci	Input capacitance	V_{CC}=V_{SS}, f=1MHz, 25mVrms, T_a=25℃			10	pF
$C_{I/O}$	Input/output capacitance	V_{CC}=V_{SS}, f=1MHz, 25mVrms, T_a=25℃			20	pF

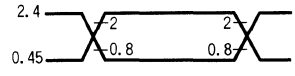
TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(W)}$	Write pulse width		190 [120]			ns
$t_{SU(A-W)}$	Address setup time before write		0			ns
$t_{h(W-A)}$	Address hold time after write		0			ns
$t_{SU(DQ-W)}$	Data setup time before write		160 [100]			ns
$t_{h(W-DQ)}$	Data hold time after write		0			ns
$t_{W(R)}$	Read pulse width		160			ns
$t_{SU(A-R)}$	Address setup time before read		0			ns
$t_{h(R-A)}$	Address hold time after read		0			ns
$t_{W(IR)}$	Interrupt request input width, low-level time, edge triggered mode		100			ns
$t_{SU(CAS-INTA)}$	Cascade setup time after $\overline{INTA}$ (slave)		40			ns
$t_{REC(W)}$	Write recovery time		190			ns
$t_{REC(R)}$	Read recovery time		160			ns
$t_{d(RW)}$	End of Command to next Command (Not same Command type)		400			ns
	End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence.					

SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

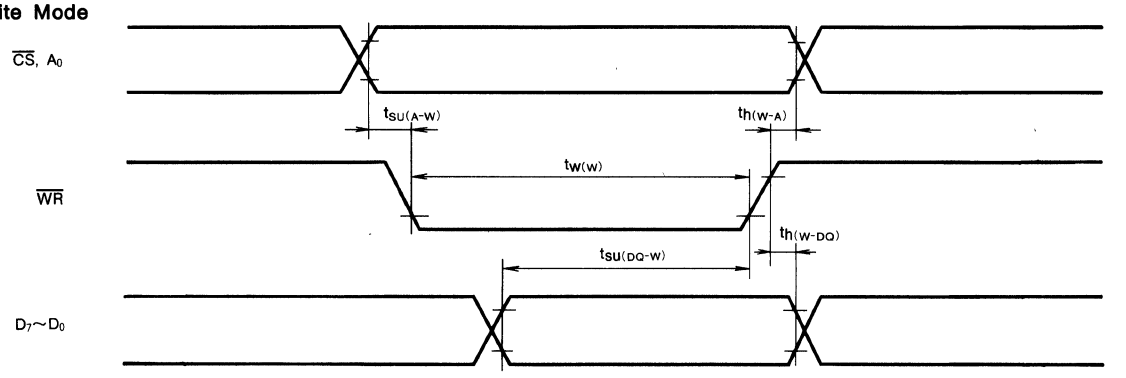
Symbol	Parameter	Test coditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Data output enable time after read				120	ns
$t_{PVZ(R-DQ)}$	Data output disable time after read		10		85	ns
$t_{PZV(A-DQ)}$	Data output enable time after address	C_L=100pF,			200 [170]	ns
$t_{PHL(R-EN)}$	Propagation time from read to enable signal output	Where $\overline{SP}/\overline{EN}$			100	ns
$t_{PLH(R-EN)}$	Propagation time from read to disable signal output	Pin is 15 pF			150	ns
$t_{PLH(IR-INT)}$	Propagation time from interrupt request input to interrupt request output				300	ns
$t_{PLV(INTA-CAS)}$	Propagation time from $\overline{INTA}$ to cascade output (master)				360	ns
$t_{PZV(CAS-DQ)}$	Data output enable time after cascade output (slave)				200	ns

Note 5 : M5M82C59AP-2 is also invested with the extended specification showed in the brackets
6 : $\overline{INTA}$ signal is considered read signal
$\overline{CS}$ signal is considered address signal
Input pulse level 0.45~2.4V
Input pulse rise time 10ns
Input pulse fall time 10ns
Reference level Input V_{IH}=2V, V_{IL}=0.8V
Output V_{OH}=2V, V_{OL}=0.8V

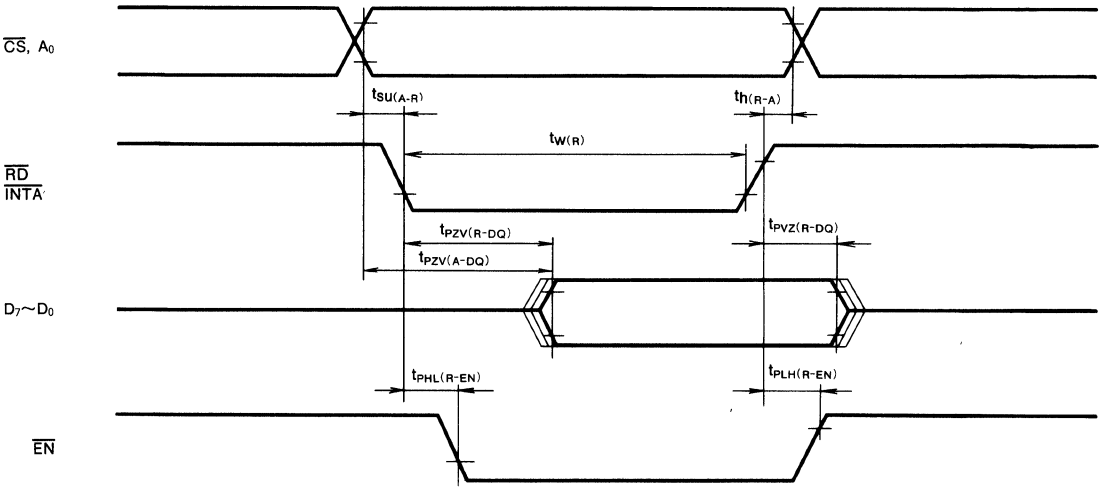


TIMING DIAGRAM

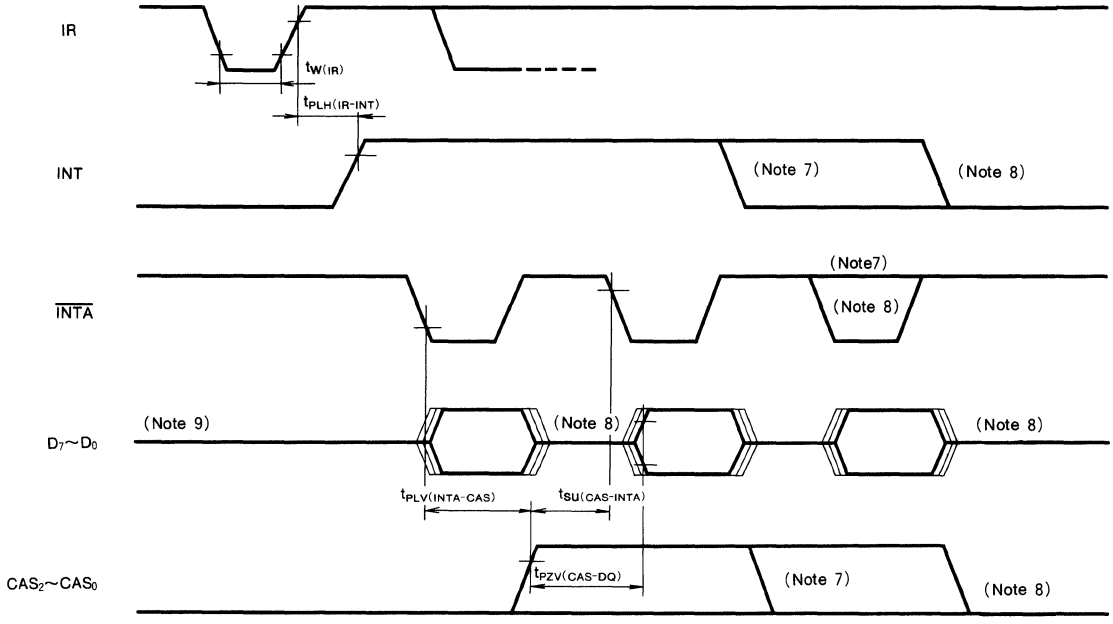
Write Mode



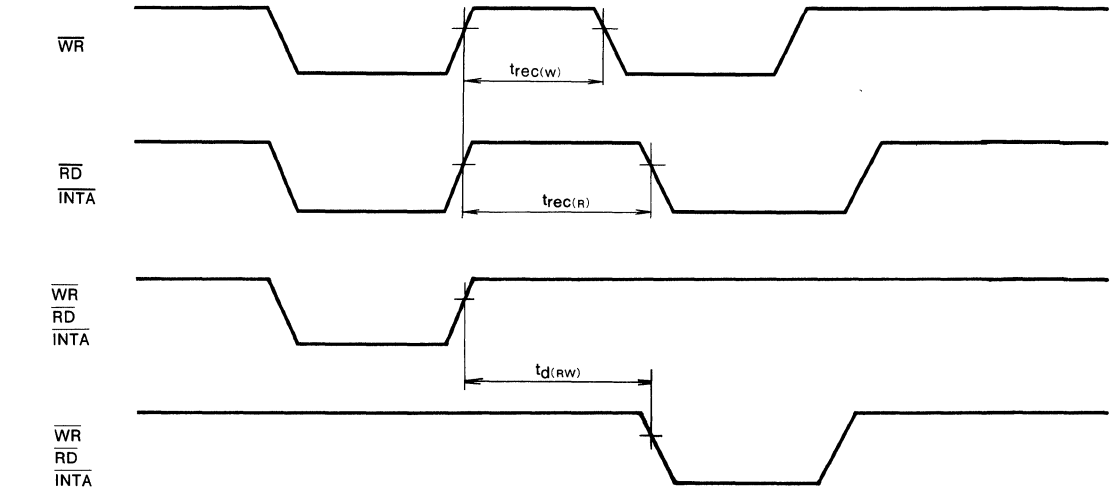
Read Mode



Interrupt Sequence



Other Timing



Note 7 : MELPS86, 88 mode
8 : MELPS85 mode
9 : MELPS86, 88 mode is in high-impedance state, pointer is released during the next INTA. When in single MELPS85 mode, data is released by all INTAs When master, CALL instruction is released during the first INTA, high impedance state during the second and third INTA When slave, high impedance state during the first INTA, vectored address is released during the second and third INTA

M5M82C255ASP

CMOS PROGRAMMABLE PERIPHERAL INTERFACE

DESCRIPTION

The M5M82C255ASP is a LSI equivalent to two M5M82C55AP-2. It is housed in a single 64-pin shrink DIP.
The M5M82C255ASP is fabricated using silicon-gate CMOS technology for a single supply voltage. This LSI is a simple input and output interface for TTL circuits, having 48 input/output pins which correspond to six 8-bit input/output ports.

FEATURES

- Single 5V supply voltage
- Input : TTL compatible (I_{OL}=2.5mA)
  Output : CMOS/TTL compatible
- Each I/O pin has ±4mA driving capability
- Read access time : 120ns
- Timing specification enable easy design of system bus timing
- Noise limiter is built-in to provide high noise margin (RESET, $\overline{ACK}$, $\overline{STB}$)
- 48 programmable I/O pins
- Direct bit set/reset capability
- 64-pin shrink DIL package (lead pitch 0.07 inch) is used for easy mounting

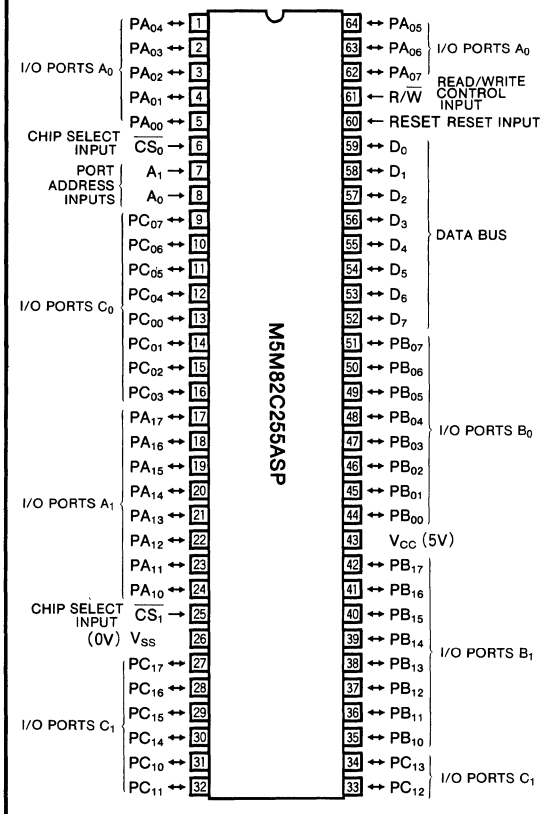
APPLLICATION

Input/output ports for microprocessor

FUNCTION

A Block diagram of the M5M82C255ASP is shown in the following page. The M5M82C255ASP consists of block 0 and block 1 each of which is functionally equivalent to the M5M82C55AP-2. Block 0 and block 1 have independent chip select inputs $\overline{CS_0}$ and $\overline{CS_1}$, and independent ports PA_0, PB_0, PC_0, PA_1, PB_1 and PC_1. The 8-bit data bus, address inputs A_0 and A_1, and the RESET input are shared by block 0 and block 1. The CPU's $\overline{RD}$ signal and $\overline{WR}$ signal must be multiplexed to generate the R/$\overline{W}$ signal.
The 48 I/O pins consist of two blocks each with two 12-bit sub blocks A and B. All four blocks can be programmed independently by three mode control commands from the CPU.
In mode 0, four 8-bit I/O ports and four 4-bit I/O ports are available for use as output ports. In mode 1, the 24 I/O pins of each block are divided into groups A and B. In each group, 8 bits are used for input or output data ports. And 4 bits are used for control data ports. In mode 2, 8 bits of group A are used as a bidirectional bus with a 5-bit control signal.
Any of the 8 data bits at port C of each block can set or reset. When reset input (RESET) is high, all ports are set to the input mode (high-impedance state).

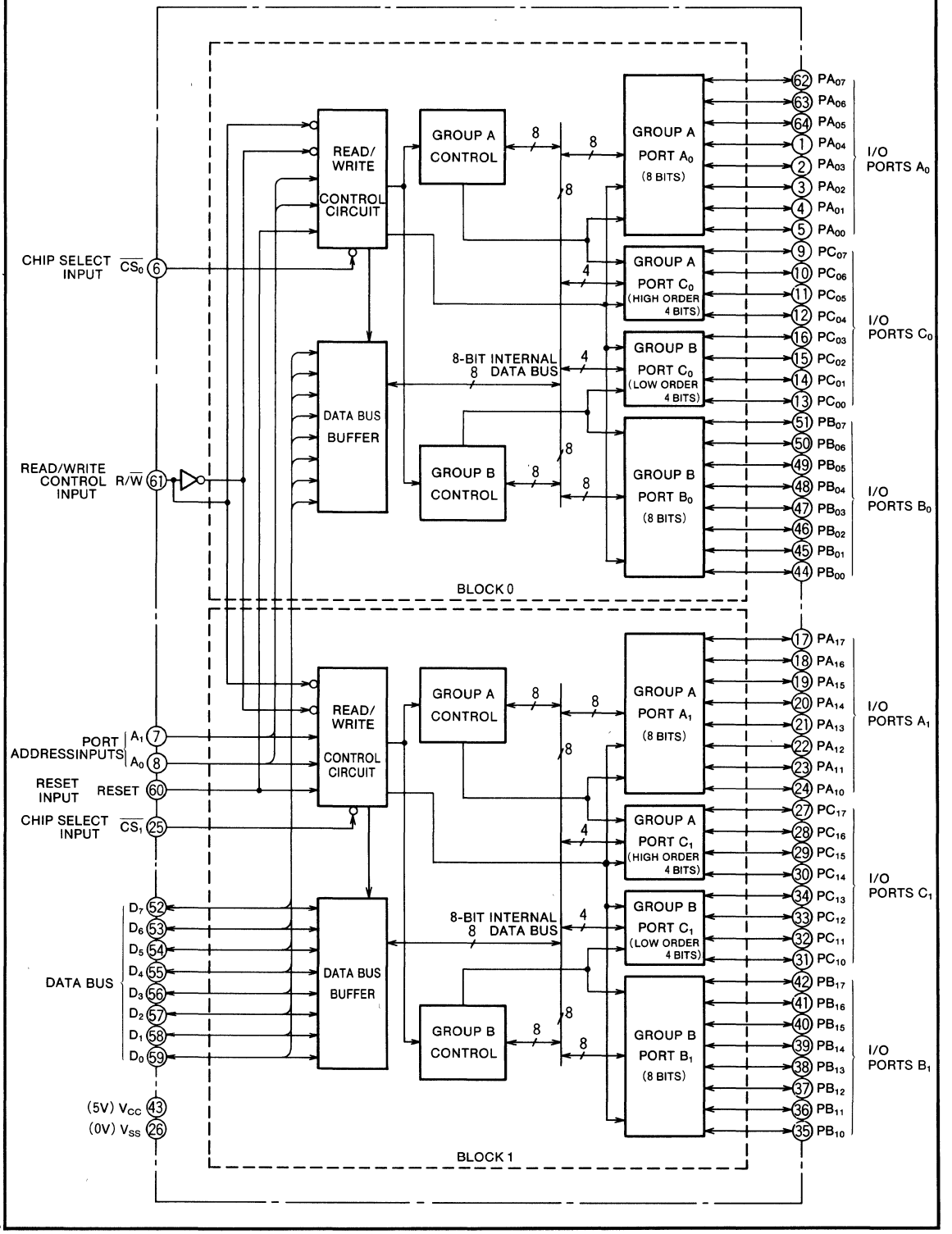
PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

MITSUBISHI ELECTRIC

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Block 0 has the same function as block 1. Therefore, block 0 is explained in the following.

R/$\overline{W}$ (Read/Write) Input

Read function operates when the R/$\overline{W}$ is high-level, and data input at the port is transferred to the CPU. Write function operates when the R/$\overline{W}$ is low-level, and data or control from the CPU are written.

A_0, A_1 (Port address) Input

These input signals are used to select one of the three ports: port A, port B, and port C, or the control register. They are normally connected to the least significant two bits of the address bus.

RESET (Reset) Input

At high-level, the control register is cleared. Then all ports are set to the input mode (high-impedance state).

$\overline{CS_0}$, $\overline{CS_1}$ (Chip-Select) Input

At low-level, the communication between M5M82C255ASP and the CPU is enabled. When $\overline{CS_0}$ is low-level block 0 is selected, and when $\overline{CS_1}$ is low-level, block 1 is selected. When $\overline{CS_0}$ and $\overline{CS_1}$ are both high-level, the data bus maintains high impedance state and control from the CPU is ignored. In modes 0 or 1, the previous data is stored.

Read/Write Control Logic

The function of this block is to control transfers of both data and control words. It accepts the address signals (A_0, A_1, $\overline{CS_0}$, $\overline{CS_1}$), I/O control signals (R/$\overline{W}$) and RESET signal, and then issues commands to both of the control groups.

Data Bus Buffer

This three-state, bidirectional, 8-bit buffer is used to transfer the data when an input or output instruction is executed by the CPU. Control words and status information are also transferred through the data bus buffer.

Group A and Group B Control

Accepting commands from the read/write control logic, the control blocks (Group A, Group B) receive 8 bit control words from the internal data bus and issue the proper commands for the associated ports. Control group A is associated with port A and the 4 high-order bits of port C. Control group B is associated with port B and the 4 low-order bits of port C. The control register, which stores control words, can only be written into.

Port A, Port B and Port C

M5M82C255ASP contains six 8-bit ports whose modes and input/output settings are programmed by the system software.

Port A has an output latch/buffer and an input latch/buffer. Port B has an input-output latch/buffer. Port C has an output latch/buffer and an input buffer. Port C can be divided into two 4-bit ports which can be used as ports for control signals for port A and port B.

The basic operations are shown in Table 1.

Table 1 Basic Operations

A_1	A_0	$\overline{CS_0}$	$\overline{CS_1}$	R/$\overline{W}$	Operation
0	0	L	H	H	Data bus ← Port A_0
0	0	H	L	H	Data bus ← Port A_1
0	1	L	H	H	Data bus ← Port B_0
0	1	H	L	H	Data bus ← Port B_1
1	0	L	H	H	Data bus ← Port C_0
1	0	H	L	H	Data bus ← Port C_1
0	0	L	H	L	Port A_0 ← Data bus
0	0	H	L	L	Port A_1 ← Data bus
0	1	L	H	L	Port B_0 ← Data bus
0	1	H	L	L	Port B_1 ← Data bus
1	0	L	H	L	Port C_0 ← Data bus
1	0	H	L	L	Port C_1 ← Data bus
1	1	L	H	L	Control register 0 ← Data bus
1	1	H	L	L	Control register 1 ← Data bus
X	X	H	H	X	Data bus is high-impedance state
1	1	L	H	H	illegal condition
1	1	H	L	H	

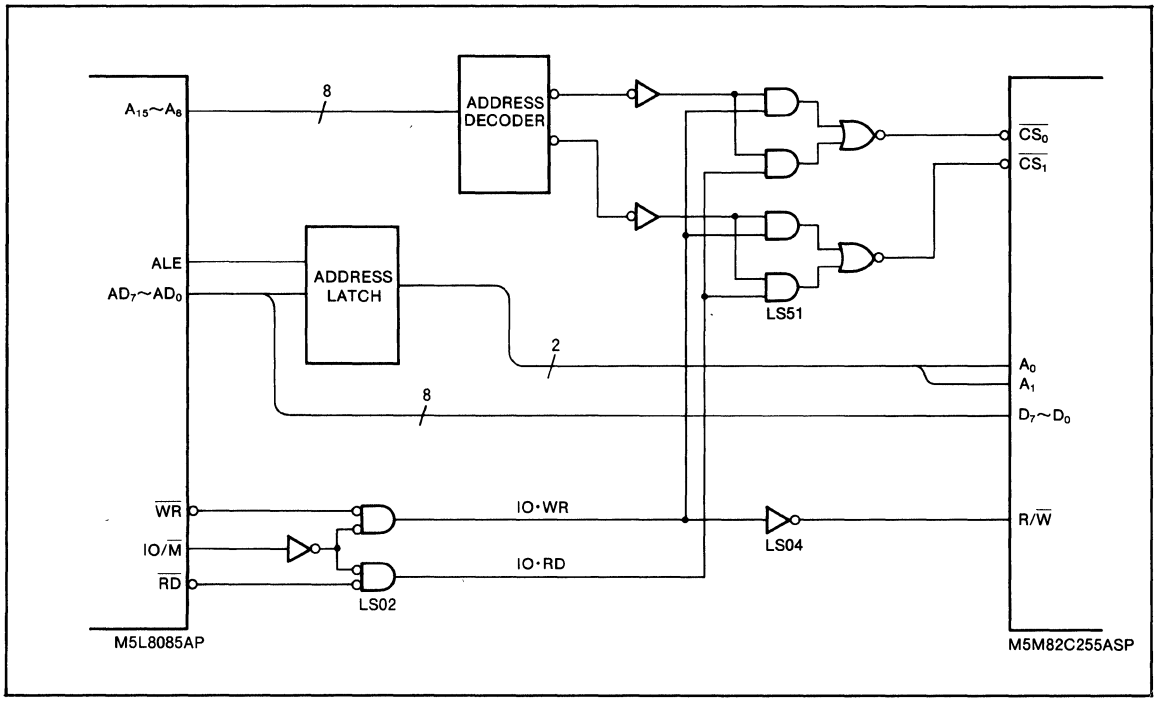


Fig. 1 Connecting the M5L8085AP and M5M82C255ASP

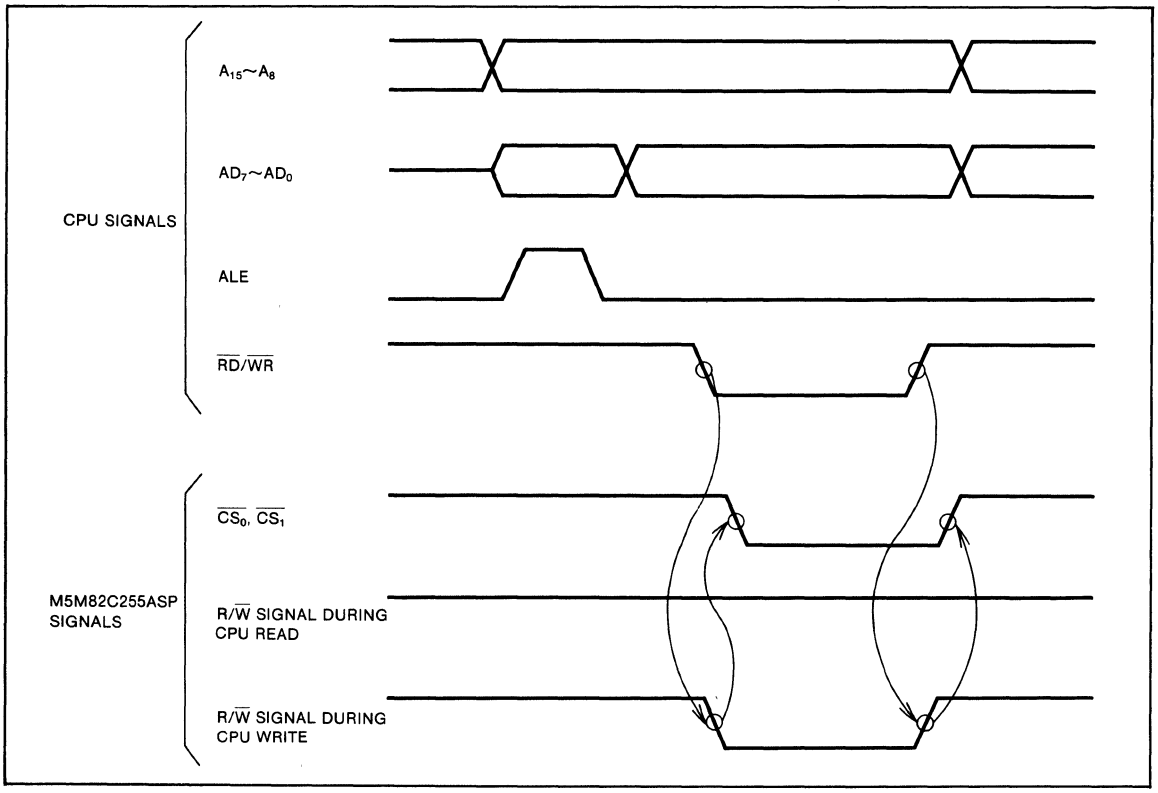


Fig. 2 Timing Diagram

CPU INTERFACE

Fig. 1 shows an application with the M5L8085AP as the CPU. In this figure, the M5M82C255ASP is mapped in the I/O space, but it could also be mapped in the memory space. The following description applies to the circuit in the Fig. 1. Characteristics are shown in Figs. 2, 3 and 4.

Chip select signal

The M5M82C255ASP chip select signal ($\overline{CS_0}$, $\overline{CS_1}$) is the logical product of the IO · RD (IO · WR) signal derived from the read (write) signal and IO/$\overline{M}$ signal from the CPU, and the address decoder output generated by decoding the address. Therefore, the timing of chip select signal ($\overline{CS_0}$, $\overline{CS_1}$) is delayed from that of IO · RD (IO · WR) signal. The chip select signals $\overline{CS_0}$ and $\overline{CS_1}$ must not be active simultaneously.

Read operation

The read operation of M5M82C255ASP starts when $\overline{RD}$ · $\overline{CS}$ = 1, just as with the M5M82C55AP-2. When the M5L8085AP CPU enters into I/O read operation, the M5M82C255ASP R/$\overline{W}$ signal, obtained by inverting the IO · WR signal, is kept at high-level. The actual read operation starts when the chip select signal is activated by the IO · RD signal and address decoder output. The access time of the M5M82C255ASP is specified by the falling edge of the chip select signal, and is defined as $t_{PZV\,(CS\text{-}DQ)}$. Fig. 3 shows the read timing. The delay time (marked by *) extends from the time when the $\overline{RD}$ signal of CPU becomes active until the chip select signal becomes active. It is obtained by adding the delay time of LS02 and LS51 in Fig. 1. Table 2 shows the gate delay time of LS02, LS51, LS04 and LS00 used in the circuit of Fig. 1. The sum of the gate delay times of LS02 and LS51 is 35ns, after which the actual read operation starts. The access time of the M5M82C255ASP is 120ns maximum, so the total access time is 155ns maximum. As the access time of the M5M82C255ASP is specified by the falling edge of the chip select signal, care must be taken when connecting the M5M82C255ASP to a high-speed microprocessor.

The address setup time and hold time of the M5M82C-55AP-2 read signal are defined as $t_{su(A\text{-}R)}$ and $t_{h(R\text{-}A)}$ but, in the M5M82C255ASP, they are defined as $t_{su\,(Ai\text{-}CS)}$ and $t_{h\,(CS\text{-}Ai)}$ due to above reason, where A_i means address inpus of A_0 or A_1. The time is specified to be 0ns minimum for each.

Note (Note) The term "address" used in describing the address setup time and address hold time of M5M82C55AP-2 means the address inputs A_0, A_1 and $\overline{CS}$

Write operation

Fig. 4 shows the write timing. The phase relationship of the R/$\overline{W}$ and chip select signals is marked by a ★. For the M5M82C55AP-2, the phase relationship is defined as the address setup time (Note) $t_{su(A\text{-}W)}$ (or t_{AW}) before $\overline{WR}$, and is specified to be 0ns minimum. In the M5M82C255ASP, however, the phase relationship is reversed by the circuit which generates the control signal (See Fig. 1), when the chip select signal becomes active after the R/$\overline{W}$ signal goes low-level. Therefore, we have discarded the previous definition. The phase difference of write signal and chip select signal is defined as $t_{su\,(CS\text{-}W)}$ and specified as 0ns maximum and −30ns minimum. The phase difference of the write signal and address inputs of A_0 and A_1 is defined as $t_{su(Ai\text{-}W)}$ and the minimum value is −30ns.

This means that the address inputs of A_0 and A_1 and the chip select signal must become stable within 30ns after the R/$\overline{W}$ signal goes low-level. The signals A_0 and A_1 can become stable before R/$\overline{W}$ goes low-level, but the chip select signal must be activated after the R/$\overline{W}$ signal goes low-level. This is required because, if the chip select signal is active before R/$\overline{W}$ signal, the R/$\overline{W}$ signal will be high-level, causing the M5M82C255ASP to enter the read operation. The address inputs of A_0 and A_1 will write properly as long as the minimum value is −30ns.

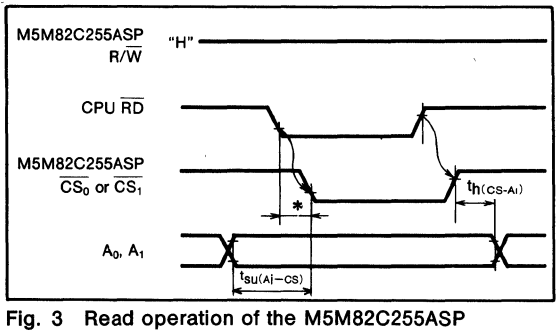


Fig. 3 Read operation of the M5M82C255ASP

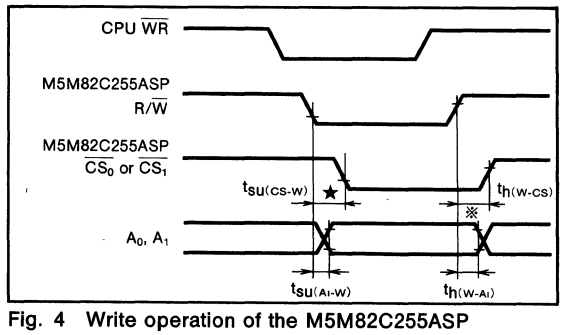


Fig. 4 Write operation of the M5M82C255ASP

Table 2 Gate delay time

Type	LS02		LS51		LS04		LS00		Unit
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
t_{PLH}	6	15	6	20	6	15	6	15	nsec
t_{PHL}	6	15	8	20	6	15	6	15	nsec

(Refer to the Bipolar Digital ICs Section of Mitsubishi Semiconductor Handbook)

Now we will explain the phase relationship between the chip select signal and the time marked by ※ in Fig. 4, the rising edge of R/$\overline{W}$ signal. In the M5M82C55AP-2, the address hold time after write is defined as $t_{h(W-A)}$ (or t_{WA}) (Note) and the specified minimum is 0ns. In the M5M82C255ASP, however, the chip select signal is kept active after the rise of the R/$\overline{W}$ signal, so under these condition, the M5M82C255ASP enters into read operation. This would cause a bus collision or misoperation of the control signal output at port C in mode 1 or mode 2. Therefore, in the M5M82C255ASP, a built-in circuit prohibits the start of read operation after the rise of R/$\overline{W}$ signal from low-level to high-level, even if the chip select signal is held active. The previous definition of $t_{h(W-A)}$ is replaced by $t_{h(W-CS)}$, which is specified as 0ns minimum and 50ns maximum. For address inputs A_0 and A_1, $t_{h(W-Ai)}$ is newly defined and specified as 0ns minimum. This means that A_0 and A_1 can be used freely to select any device after the R/$\overline{W}$ signal rises again to high-level. The data setup time $t_{su(DQ-W)}$ (or t_{DW}) for the rise of R/$\overline{W}$ and data hold time $t_{h(W-DQ)}$ (or t_{WD}) for the fall of R/$\overline{W}$ signal in write operation of the M5M82C255ASP are defined identically as in the M5M82C55AP-2.

Note : The term "address" in the address setup time and address hold time of the M5M82C55AP-2 means the address inputs A_0 A_1 and $\overline{CS}$.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings		Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3∼7		V
V_I	Input voltage		−0.3∼V_{CC}+0.3		V
V_O	Output voltage		−0.3∼V_{CC}+0.3		V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current.	Port	−4	mA
			Data bus	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current.	Port	4	mA
			Data bus	2.5	mA
Topr	Operating temperature range		−20∼75		℃
Tstg	Storage temperature		−65∼150		℃

RECOMMENDED OPERATING CONDITIONS (T_a = −20∼75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a = −20∼75℃, V_{CC} = 5V±10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage (Note 2)	I_{OH}=−400μA	2.4			V
		I_{OH}=−20μA	4.4			
V_{OL}	Low-level output voltage (Note 2)	I_{OL}=2.5mA			0.4	V
I_{CC}	Supply current	All Input Mode RESET=0V, Other Pins=V_{CC}			10	μA
I_{IL}	Input leak current	V_I=0V, V_{CC}			±10	μA
I_{OZ}	Off-state output current	V_O=0V∼V_{CC}			±10	μA
C_i	Input capacitance	f=1MHz, 25mVrms, T_a=25℃			10	pF
$C_{I/O}$	I/O capacitance	0V except test pins			30	pF

Note 1 : Current flowing into an IC is positive (no sign).
2 : The maximum value of the output current should be held within ±4mA at each port pin.

TIMING REQUIREMENTS (T_a = −20~75℃, V_{CC} = 5V±10%, V_{SS} = 0V, unless otherwise noted)

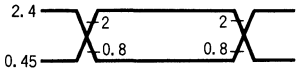
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(CS)}$	Chip select pulse width		160			ns
$t_{su(PE-CS)}$	Peripheral setup time before read		0			ns
$t_{h(CS-PE)}$	Peripheral hold time after read		0			ns
$t_{su(Ai-CS)}$	Address setup time before read		0			ns
$t_{h(CS-Ai)}$	Address hold time after read		0			ns
$t_{W(R/\overline{W})}$	R/$\overline{W}$ pulse width		120			ns
$t_{su(DQ-W)}$	Data setup time before write		100			ns
$t_{h(W-DQ)}$	Data hold time after write		0			ns
$t_{su(Ai-W)}$	Address setup time before write		−30			ns
$t_{h(W-Ai)}$	Address hold time after write		0			ns
$t_{su(CS-W)}$	Chip select setup time before write		−30		0	ns
$t_{h(W-CS)}$	Chip select hold time after write		0		50	ns
$t_{W(ACK)}$	Acknowledge pulse width		300			ns
$t_{W(STB)}$	Strobe pulse width		350			ns
$t_{su(PE-STB)}$	Peripheral setup time before strobe		0			ns
$t_{h(STB-PE)}$	Peripheral hold time after strobe		150			ns
$t_{C(CSW)}$	Read/write cycle time		200			ns

SWITCHING CHARACTERISTICS (T_a = −20~75℃, V_{CC} = 5V±10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(CS-DQ)}$	Propagation time from read to data output	C_L=150pF			120	ns
$t_{PVZ(CS-DQ)}$	Propagation time from read to data floating (Note 3)		10		85	ns
$t_{PHL(W-PE)}$, $t_{PLH(W-PE)}$	Propagation time from write to output				350	ns
$t_{PLH(STB-IBF)}$	Propagation time from strobe to IBF flag				300	ns
$t_{PLH(STB-INTR)}$	Propagation time from strobe to interrupt				300	ns
$t_{PHL(CS-INTR)}$	Propagation time from read to interrupt				400	ns
$t_{PHL(CS-IBF)}$	Propagation time from read to IBF flag				300	ns
$t_{PHL(W-INTR)}$	Propagation time from write to interrupt				450	ns
$t_{PHL(W-OBF)}$	Propagation time from write to $\overline{OBF}$ flag				300	ns
$t_{PLH(ACK-OBF)}$	Propagation time from acknowledge to $\overline{OBF}$ flag				350	ns
$t_{PLH(ACK-INTR)}$	Propagation time from acknowledge to interrupt				350	ns
$t_{PZV(ACK-PE)}$	Propagation time from acknowledge to output				300	ns
$t_{PVZ(ACK-PE)}$	Propagation time from acknowledge to output floating (Note 3)		20		250	ns

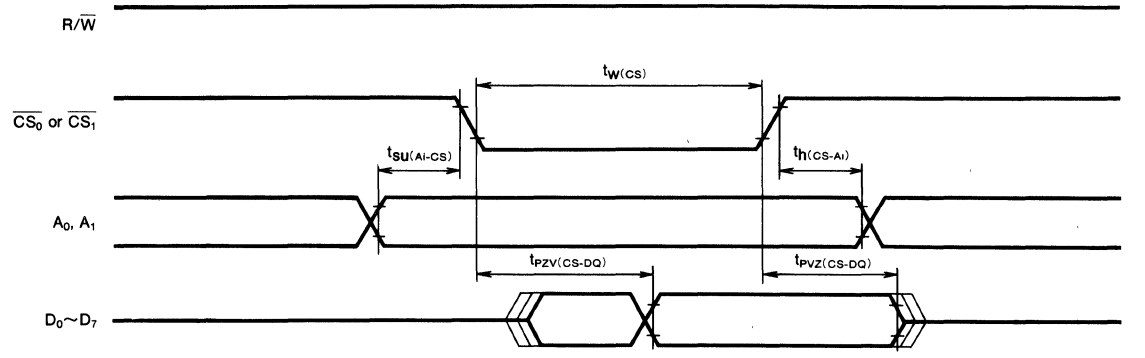
Note 3 : The above test conditions are not applied

4 : Input pulse level 0.45~2.4V Reference level Input V_{IH}=2V, V_{IL}=0.8V
Input pulse rise time 10ns Output V_{OH}=2V, V_{OL}=0.8V
Input pulse fall time 10ns

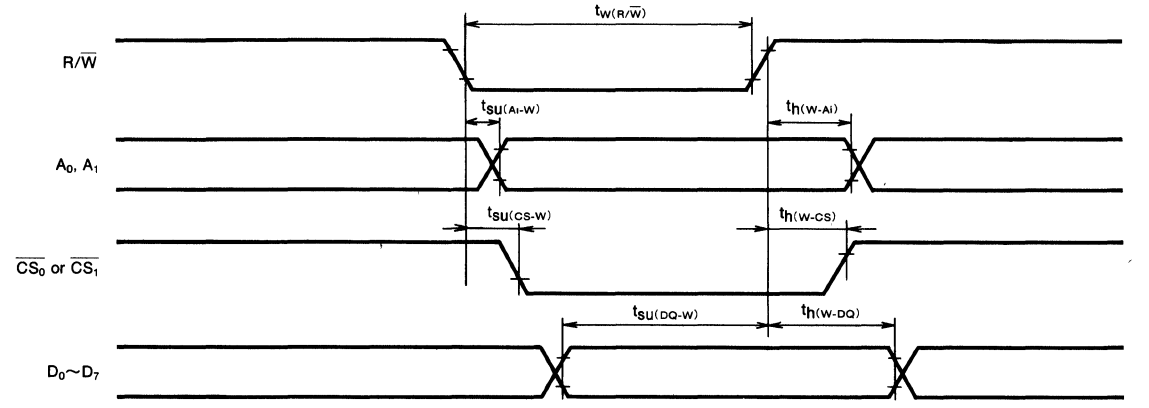


TIMING DIAGRAM

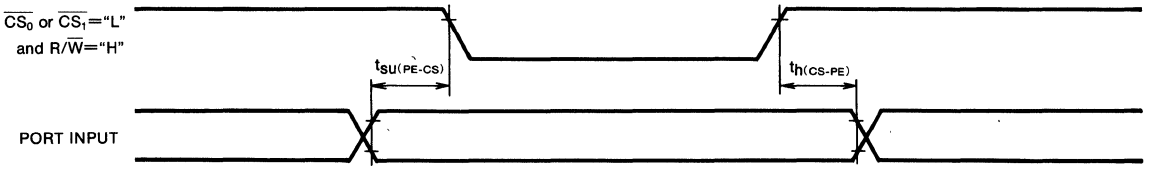
Data Bus Read Timing



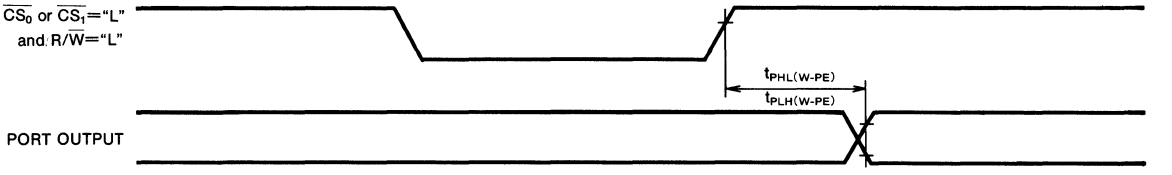
Data Bus Write Timing



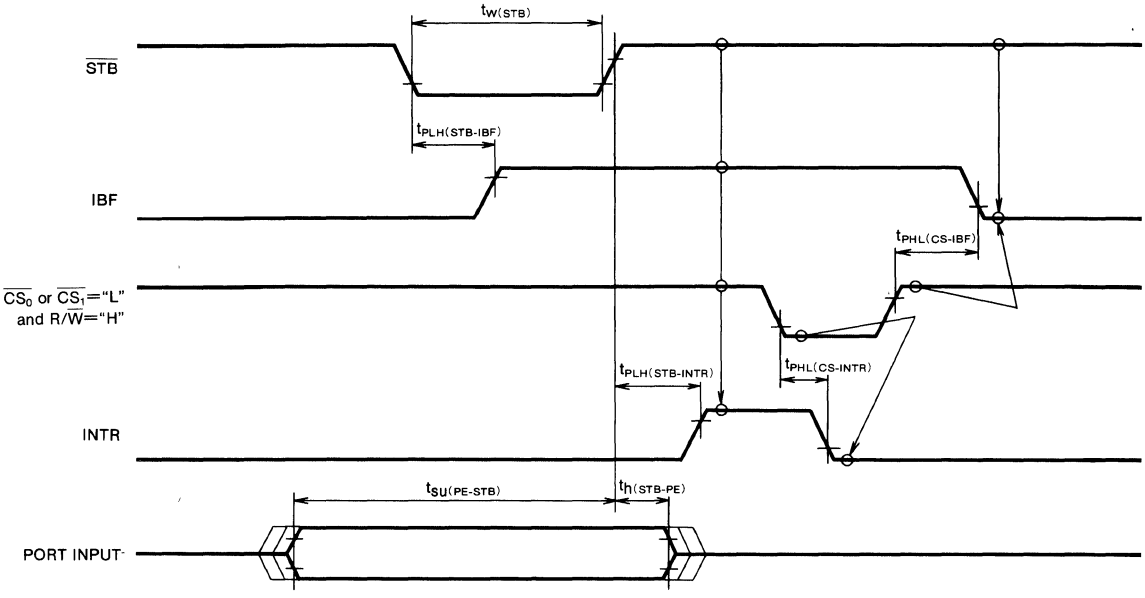
Mode 0 Port Input



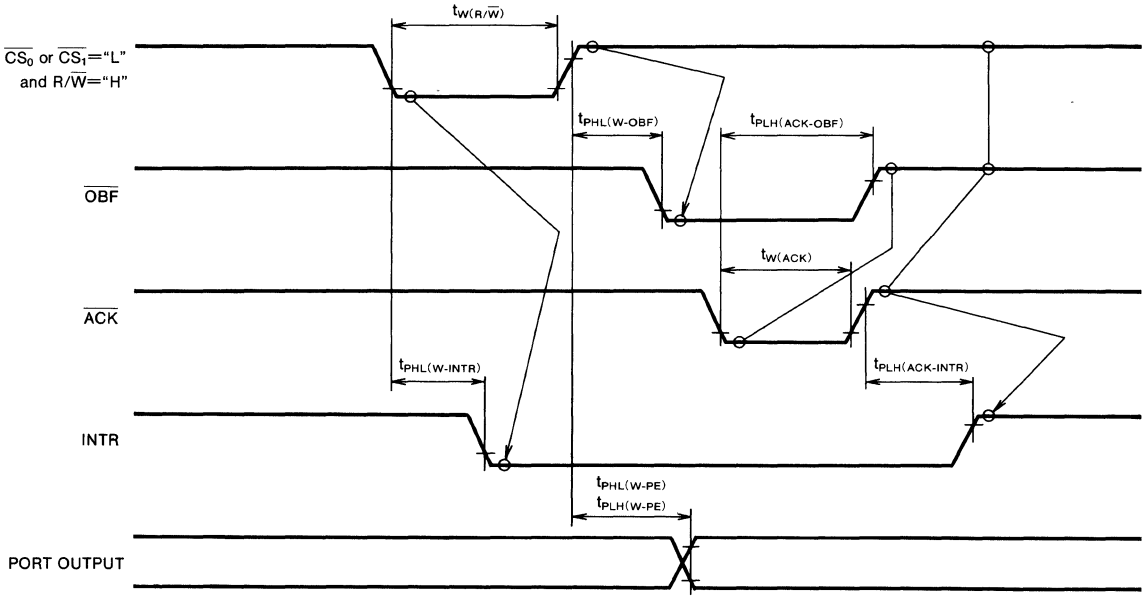
Mode 0, 1 Port Output



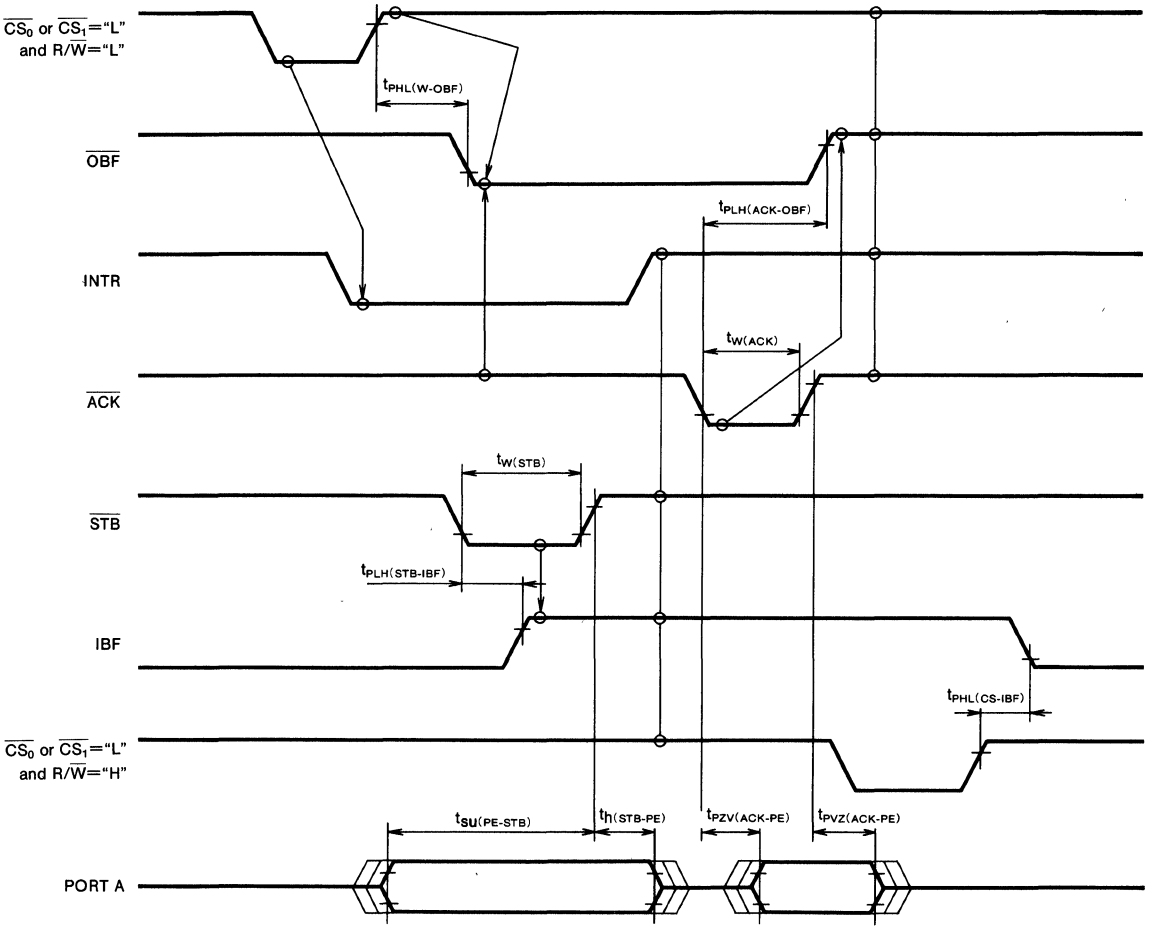
Mode 1 Storbe Input



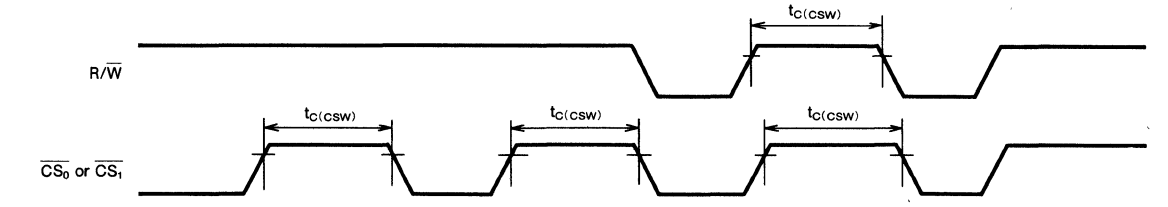
Mode 1 Storbe Output



Mode 2 Bidirectional



Note 5 : INTR=IBF·$\overline{MASK}$·$\overline{STB}$·$\overline{CS_0}$ or $\overline{CS_1}$+$\overline{OBF}$·$\overline{MASK}$·$\overline{ACK}$·R/$\overline{W}$



NMOS PERIPHERAL CIRCUITS

5

M5L8155P

2048-BIT STATIC RAM WITH I/O PORTS AND TIMER

DESCRIPTION

The M5L8155P is a 2K-bit RAM (256-word by 8-bit) fabricated by the N-channel silicon-gate ED-MOS technology. This LSI has 3 I/O ports and a 14-bit counter/timer which make it a good extention of the functions of an 8-bit microcomputer. It is packaged in a 40-pin plastic DIL package and operates with a single 5V power supply.

FEATURES

- Single 5V supply voltage
- TTL compatible
- Static RAM: 256-word by 8-bit
- Programmable 8-bit I/O port: 2
- Programmable 6-bit I/O port: 1
- Programmable counter/timer: 14-bit
- Multiplexed address/data bus

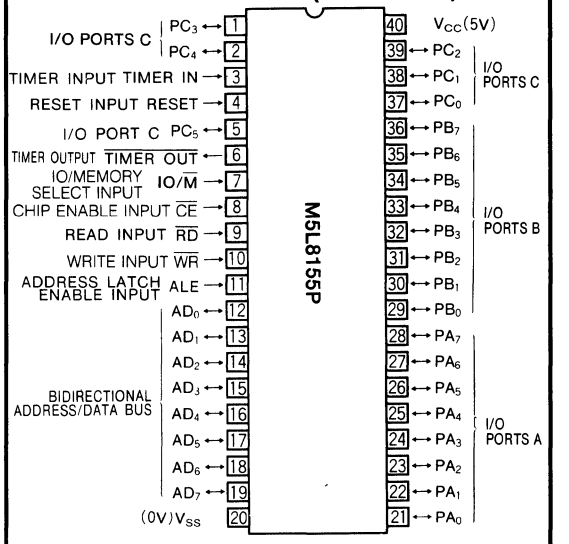
APPLICATION

Extension of I/O ports and timer function for MELPS 85 and MELPS 8-48 devices

FUNCTION

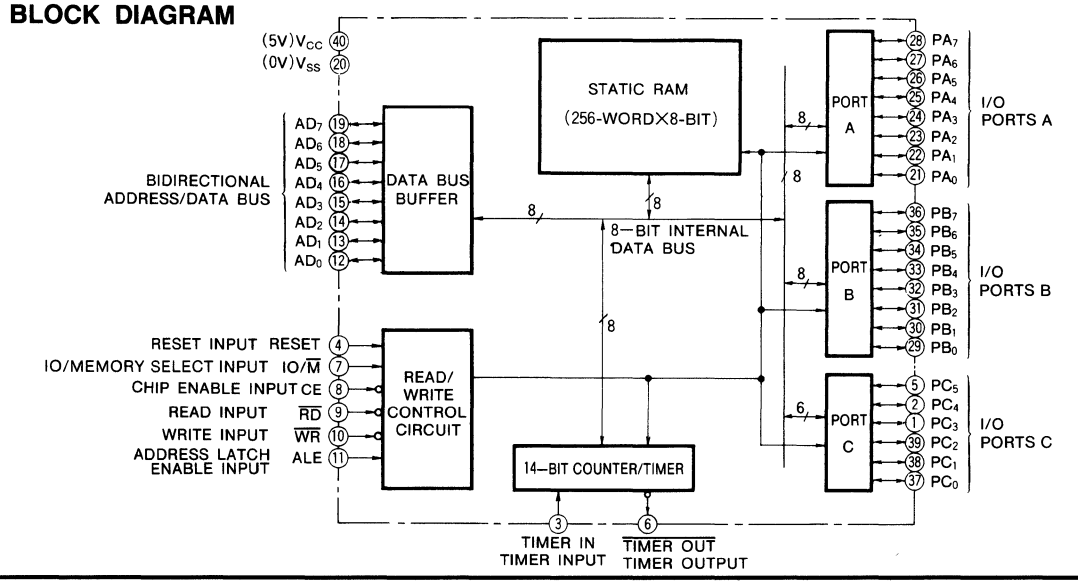
The M5L8155P is composed of RAM, I/O ports and counter/timer. The RAM is a 2K-bit static RAM organized as 256 words by 8 bits. The I/O ports consist of 2 programmable 8-bit ports and 1 programmable 6-bit port. The terminals of the 6-bit port can be programmed as control terminals for the 8-bit ports, so that the 8-bit ports can be operated in a handshake mode. The counter/timer is composed of 14-bit down counter (events or time) and it can generate square wave pulses that can be used for counting and timing.

PIN CONFIGURATION (TOP VIEW)



Outline 40P4

BLOCK DIAGRAM



OPERATION

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to transfer the data while input or output instructions are being executed by the CPU. Command and address information is also transferred through the data bus buffer.

Read/Write Control Logic

The read/write control logic controls the transfer of data and commands by interpreting the signals ($\overline{CE}$, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, ALE and RESET) from CPU.

Bidirectional Address/Data Bus (AD_0~AD_7)

The bidirectional address/data bus is a 3-state 8-bit bus. The 8-bit address is latched in the internal latch by the falling edge of ALE. Then if IO/$\overline{M}$ input signal is at high-level, the address of I/O port, counter/timer, or command register is selected. If it is at low-level, address of RAM is selected. The 8-bit data is transferred by read input ($\overline{RD}$) or write input ($\overline{WR}$).

Chip Enable Input ($\overline{CE}$)

When $\overline{CE}$ is at low-level, the address information on address/data bus is stored in the M5L8155P.

Read Input ($\overline{RD}$)

When $\overline{RD}$ is at low-level, the data bus buffer is active. If IO/$\overline{M}$ input signal is at low-level, the contents of RAM are read through the address/data bus. If IO/$\overline{M}$ input is at high-level, the contents of selected I/O port or counter/timer are read through the address/data bus.

Write Input ($\overline{WR}$)

When $\overline{WR}$ is at low-level, the data on the address/data bus are written into RAM if IO/$\overline{M}$ is at low-level, or they are written into I/O port, counter/timer or command register if IO/$\overline{M}$ is at high-level.

Address Latch Enable Input (ALE)

An address on the address/data bus is latched in the M5L8155P on the falling edge of ALE along with the levels of $\overline{CE}$ and IO/$\overline{M}$.

IO/Memory Input (IO/$\overline{M}$)

When IO/$\overline{M}$ is at low-level, the RAM is selected, while at high-level the I/O port, counter/timer or command register are selected.

I/O Port A (PA_0~PA_7)

Port A is an 8-bit general-purpose I/O port. Input/output setting is controlled by the system software.

I/O Port B (PB_0~PB_7)

Port B is an 8-bit general-purpose I/O port. Input/output setting is controlled by the system software.

I/O Port C (PC_0~PC_5)

Port C is a 6-bit I/O port that can also be used to output control signals of port A (PA) or port B (PB). The functions of port C are controlled by the system software. When port C is used to output control signals of ports A or B, the assignment of the signals to the pins is as shown in Table 1.

Table 1 Pin assignment of control signals of port C

Pin	Function	
PC_5	$\overline{B\ STB}$	(port B strobe)
PC_4	B BF	(port B buffer full)
PC_3	B INTR	(port B interrupt)
PC_2	$\overline{A\ STB}$	(port A strobe)
PC_1	A BF	(port A buffer full)
PC_0	A INTR	(port A interrupt)

Timer Input (TIMER IN)

The signal on this input terminal is used by the counter/timer for counting events or time. (3MHz max.)

Timer Output ($\overline{TIMER\ OUT}$)

A square wave signal or pulse from the counter/timer is output through this pin when in the operation mode.

Command Register (8 bits)

The command register is an 8-bit latched register. The low-order 4 bits (bits 0~3) are used for controlling and determination of mode of the ports. Bits 4 and 5 are used as interrupt enable flags for ports A and B when port C is used as a control port. Bits 6 and 7 are used for controlling the counter/timer. The contents of the command register are rewritten by output instructions (I/O address XXXXX000).

Details of the functions of the individual bits of the command register are shown in Table 2.

Table 2 Bit functions of the command register

Bit	Symbol	Function	
0	PA	PORT A I/O SET	1: Output port A 0: Input port A
1	PB	PORT B I/O SET	1: Output port B 0: Input port B
2	PC_1	PORT C SET	00: ALT1 11. ALT2 01 ALT3 10: ALT4
3	PC_2		
4	IEA	PORT A INTERRUPT ENABLE FLAG	1. Enable interrupt 0. Disable interrupt
5	IEB	PORT B INTERRUPT ENABLE FLAG	1. Enable interrupt 0. Disable interrupt
6	TM1	COUNTER/TIMER CONTROL 00: No influence on counter/timer operation 01: Counter/timer operation discontinued (If not already stopped) 10: Counter/timer operation discontinued after the current counter/timer operation is completed 11: Counter/timer operation started	
7	TM2		

Status Register (7-bit)

The status register is a 7-bit latched register. The low-order 6 bits (bits 0~5) are used as status flags for the I/O ports. Bit 6 is used as a status flag for the counter/timer. The contents of the status register are transferred into the CPU by reading (INPUT instruction, I/O address XXXXX000). Details of the functions of the individual bits of the status register are shown in Table 3.

Table 3 Bit functions of the status register

Bit	Symbol	Function
0	INTR A	PORT A INTERRUPT REQUEST
1	A BF	PORT A BUFFER FULL FLAG
2	INTE A	PORT A INTERRUPT ENABLE
3	INTR B	PORT B INTERRUPT REQUEST
4	B BF	PORT B BUFFER FULL FLAG
5	INTE B	PORT B INTERRUPT ENABLE
6	TIMER	COUNTER/TIMER INTERRUPT (This flag is set to 1 when the final limit of the counter/timer is reached and is reset to 0 when the status is read)
7	—	This bit is not used

I/O PORTS

Command/status registers (8-bit/7-bit)

These registers are assigned address XXXXX000. When an OUTPUT command is executed, the contents of the command register are rewritten. When an INPUT command is executed, the contents of the status register are read.

Port A Register (8-bit)

Port A Register is assigned address XXXXX001. This register can be programmed as an input or output by setting the appropriate bits of the command register as shown in Table 2.

Port A can be operated in basic or strobe mode and is assigned I/O terminal PA_0~PA_7.

Port B Register (8-bit)

Port B register is assigned address XXXXX010. As with Port A register, this register can be programmed as an input or output by setting the appropriate bits of the command register as shown in Table 2. Port B can be operated in basic or strobe mode and is assigned I/O terminals PB_0~PB_7.

Port C Register (6-bit)

Port C register is assigned address XXXXX011. This port is used not only for input or output but also for controlling input/output operations of ports A and B by selectively setting bits 2 and 3 of the command register as shown in Table 2. Details of the functions of the various setting of bits 2 and 3 are shown in Table 4. Port C is assigned I/O terminals PC_0~PC_5. When used as port control signals, the 3 low-order bits are assigned for port A while the 3 high-order bits are assigned for port B.

Table 4 Functions of port C

State Terminal	ALT 1	ALT 2	ALT 3	ALT 4
PC_5	Input	Output	Output	$\overline{\text{B STB}}$ (port B strobe)
PC_4	Input	Output	Output	B BF (port B buffer full)
PC_3	Input	Output	Output	B INTR (port B interrupt)
PC_2	Input	Output	$\overline{\text{A STB}}$ (port A strobe)	$\overline{\text{A STB}}$ (port A strobe)
PC_1	Input	Output	A BF (port A buffer full)	A BF (port A buffer full)
PC_0	Input	Output	A INTR (port A interrupt)	A INTR (port A interrupt)

CONFIGURATION OF PORTS

A block diagram of 1 bit of ports A and B is shown in Fig. 1. While port A or B is programmed as an output port, if the port is addressed by an input instruction, the contents of the selected port can be read. When a port is put in input mode, the output latch is cleared and writing into the output latch is disabled. Therefore when a port is changed to output mode from input mode, low-level signals are output through the port. When a reset signal is applied, all 3 ports (PA, PB, and PC) will be input ports and their output latches are cleared. Port C has the same configuration as ports A and B in modes ALT1 and ALT2.

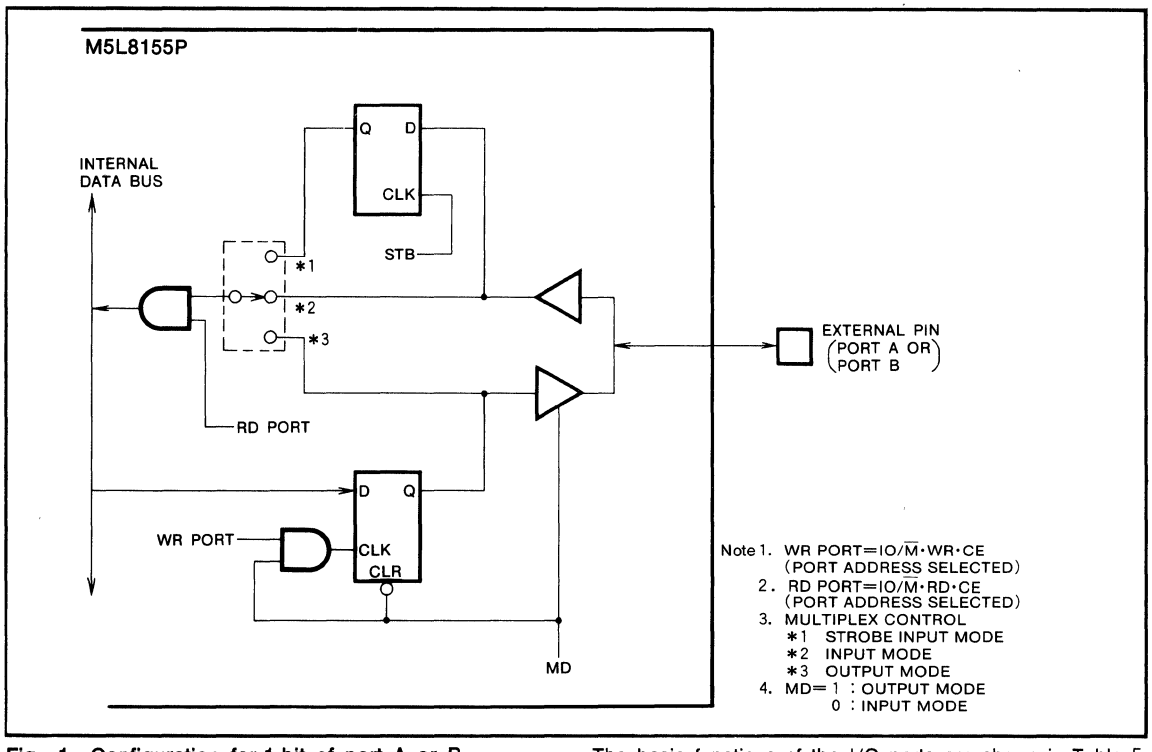


Fig. 1 Configuration for 1 bit of port A or B

Table 5 Basic functions of I/O ports

Address	$\overline{RD}$	$\overline{WR}$	Function
XXXXX000	L	H	AD bus ← Status register
	H	L	Command register ← AD bus
XXXXX001	L	H	AD bus ← Port A
	H	L	Port A ← AD bus
XXXXX010	L	H	AD bus ← Port B
	H	L	Port B ← AD bus
XXXXX011	L	H	AD bus ← Port C
	H	L	Port C ← AD bus

Table 6 Port control signal levels at ALT3 and ALT4

Control Signal	Output mode	Input mode
$\overline{STB}$	Input	Input
BF	"L"	"L"
INTR	"H"	"L"

The basic functions of the I/O ports are shown in Table 5. The control signal levels to ports A and B, when port C is programmed as a control port, are shown in Table 6.

COUNTER/TIMER

The counter/timer is composed of a 14-bit counting register and 2 mode flags. The register has two sections: I/O address XXXXX100 is assigned to the low-order 8 bits and I/O address XXXXX101 is assigned to the high-order 6 bits and timer mode flag 2 bits. The low-order bits 0 ~ 13 are used for counting or timing. The counter is initialized by the program and then counted down to 0. The initial value can be ranged from 2_{16} to $3FFF_{16}$. Bits 14 and 15 are used as mode flags.

The mode flags select 1 of 4 modes with functions as follows:

Mode 0: Outputs high-level signal during the former half of the counter operation
Outputs low-level signal during the latter half of the counter operation

Table 7 Format of counter/timer

Address	Bit Number								Function
	7	6	5	4	3	2	1	0	
XXXXX100	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0	The low-order 8 bits of the counter register
XXXXX101	M_2	M_1	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	M2,M1 Timer mode T_{13}~T_8 The high-order 6 bits of the counter register

Table 8 Timer mode

M_2	M_1	Timer operation
0	0	Outputs high-level signal during the former half of the counter operation Outputs low-level signal during the latter half of the counter operation (mode 0)
0	1	Outputs square wave signals in mode 0 (mode 1)
1	0	Outputs a low-level pulse during the final count down (mode 2)
1	1	Outputs a low-level pulse during each final count down (mode 3)

Mode 1: Outputs square wave signals as in mode 0
Mode 2: Outputs a low-level pulse during the final count down
Mode 3: Outputs a low-level pulse during each final count down

Starting and stopping the counter/timer is controlled by bits 6 and 7 of the command register (see Table 2 for details). The format and timer modes of the counter/timer register are shown in Table 7 and Table 8.

The contents of counter/timer is not affected by a reset, but counting is discontinued. To resume counting, a start command must be written into the command register as shown in Table 2. While operating 2n+1 count down in modes 0 and 1, a high-level signal is output during the former n+1 counting and a low-level signal is output during the later n counting.

RESET

The M5L8155P is reset by 600ns (min) pulse input on RESET pin.

By reset, all 3 ports are set to input mode. And counter/timer stops, but contents of counter/timer is not reset. Therefore it is necessary to input start command again.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5~7	V
V_I	Input voltage		−0.5~7	V
V_O	Output voltage		−0.5~7	V
P_d	Maximum power dissipation	T_a=25℃	1.5	W
T_{opr}	Operating free-air temperature range		−20~75	℃
T_{stg}	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Power-supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5 V±5 %, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.5	V
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL}=2mA			0.45	V
I_I	Input leak current	V_I=0V, V_{CC}	−10		10	μA
$I_{I(\overline{CE})}$	Input leak current, $\overline{CE}$ pin	V_I=0V, V_{CC}	−100		100	μA
I_{OZ}	Output floating leak current	V_O=0V~V_{CC}	−10		10	μA
C_I	Input terminal capacitance	V_{IL}=0V, f=1MHz, 25mVrms, T_a=25℃			10	pF
$C_{I/O}$	Input/output terminal capacitance	$V_{I/OL}$=0V, f=1MHz, 25mVrms, T_a=25℃			20	pF
I_{CC}	Supply current from V_{CC}				180	mA

Note 5 : Current flowing into an IC is positive, out is negative.

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}= 5 V± 5 %, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(A-L)}$	Address setup time before latch		50			ns
$t_{h(L-A)}$	Address hold time after latch		80			ns
$t_{d(L-RW)}$	Delay time, latch to read/write		100			ns
$t_{w(L)}$	Latch pulse width		100			ns
$t_{d(RW-L)}$	Delay time, read/write to latch		20			ns
$t_{w(RW)}$	Read/write pulse width		250			ns
$t_{su(DQ-W)}$	Data setup time before write		150			ns
$t_{h(W-DQ)}$	Data hold time after write		0			ns
$t_{c(RW)}$	Read/write cycle time		300			ns
$t_{su(P-R)}$	Port setup time before read		70			ns
$t_{h(R-P)}$	Port hold time after read		50			ns
$t_{w(STB)}$	Strobe pulse width		200			ns
$t_{su(P-STB)}$	Port setup time before strobe		50			ns
$t_{h(STB-P)}$	Port hold time after strobe		120			ns
$t_{w(\phi H)}$	Timer input high-level pulse width		120			ns
$t_{w(\phi L)}$	Timer input low-level pulse width		80			ns
$t_{c(\phi)}$	Timer input cycle time		320		DC	ns
$t_{r(\phi)}$	Timer input rise time				30	ns
$t_{f(\phi)}$	Timer input fall time				30	ns

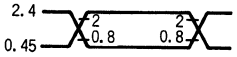
SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}= 5 V± 5 %, V_{SS}=0V, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Propagation time from read to data output	C_L = 150pF			170	ns
$t_{PZV(A-DQ)}$	Propagation time from address to data output				400	ns
$t_{PVZ(R-DQ)}$	Propagation time from read to data floating (Note 6)		0		100	ns
$t_{PHL(W-P)}$ / $t_{PLH(W-P)}$	Propagation time from write to data output				400	ns
$t_{PLH(STB-BF)}$	Propagation time from strobe to BF flag				400	ns
$t_{PHL(R-BF)}$	Propagation time from read to BF flag				400	ns
$t_{PLH(STB-INTR)}$	Propagation time from strobe to interrupt				400	ns
$t_{PHL(R-INTR)}$	Propagation time from read to interrupt				400	ns
$t_{PHL(STB-BF)}$	Propagation time from strobe to BF flag				400	ns
$t_{PLH(W-BF)}$	Propagation time from write to BF flag				400	ns
$t_{PHL(W-INTR)}$	Propagation time from write to interrupt				400	ns
$t_{PHL(\phi-OUT)}$ / $t_{PLH(\phi-OUT)}$	Propagation time from timer input to timer output				400	ns

Note 6 : Test conditions are not applied.

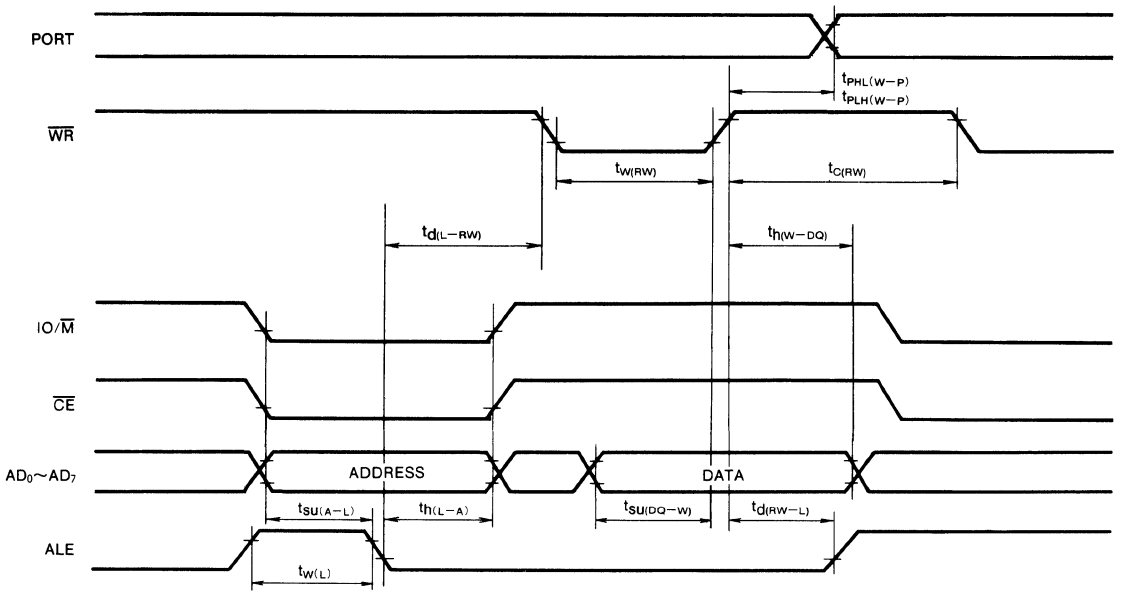
7 : A.C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	20ns
Input pulse fall time	20ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V

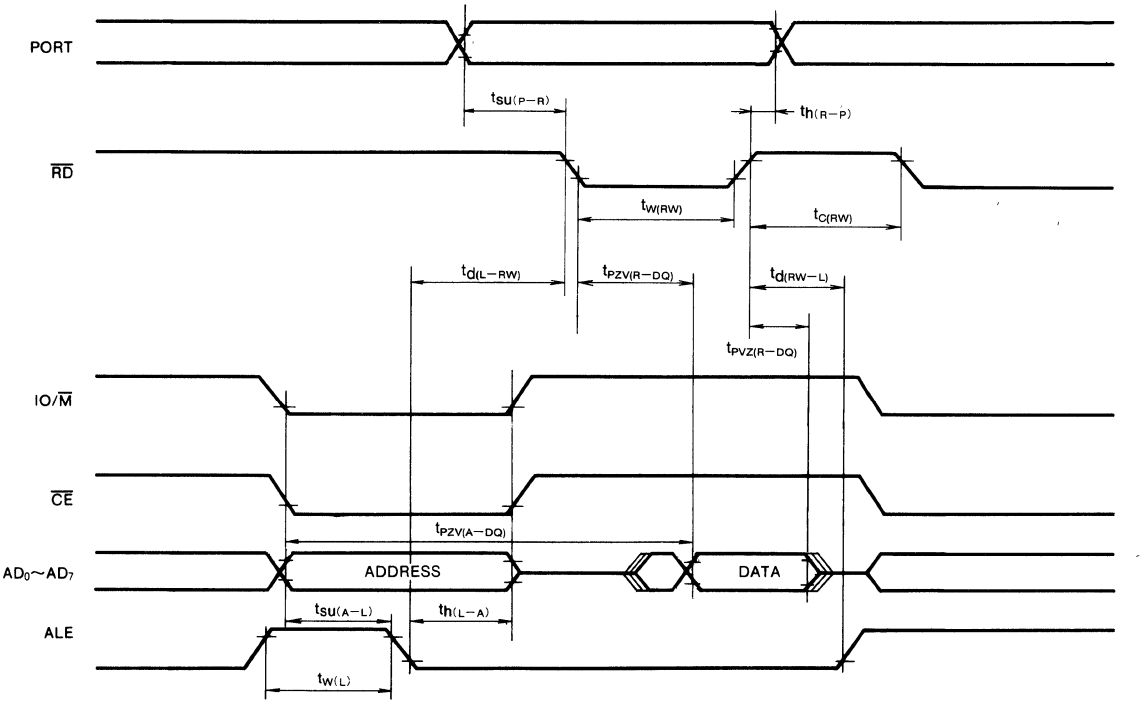


TIMING DIAGRAM

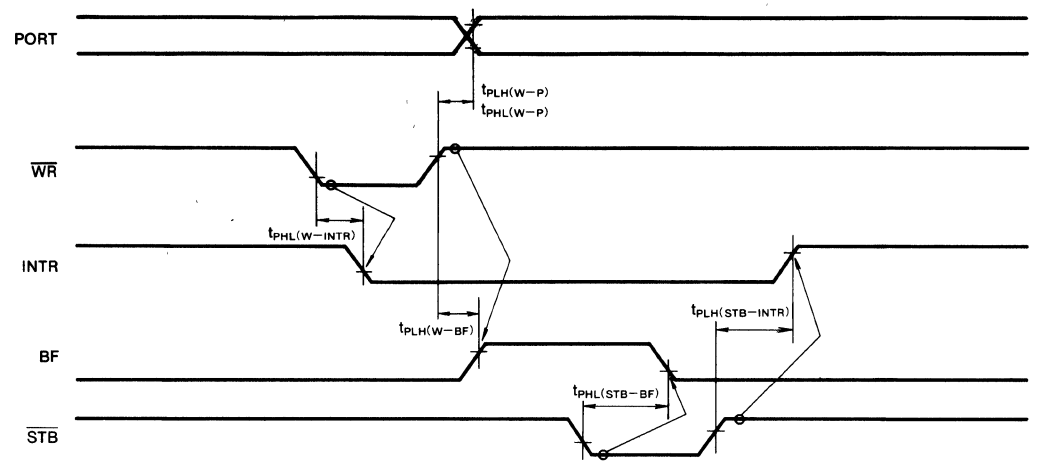
Basic Output



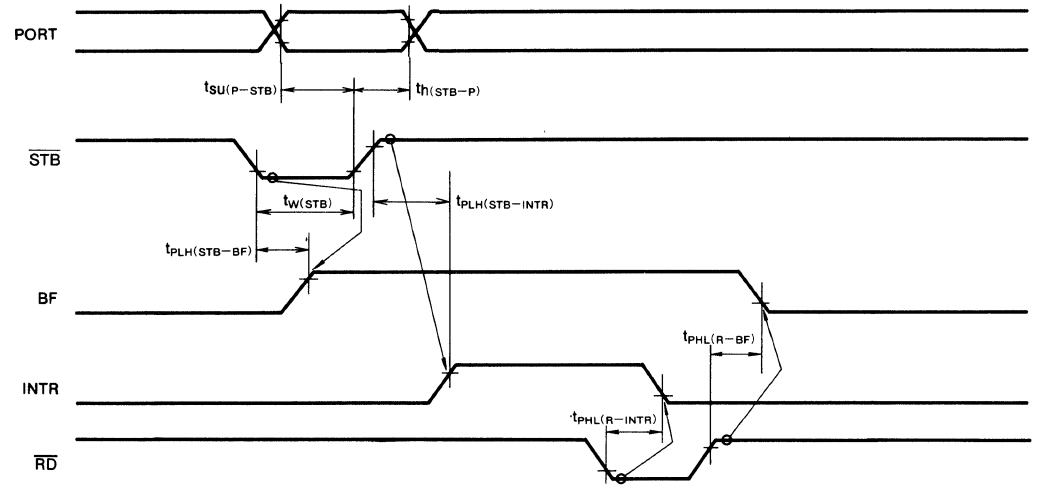
Basic Input



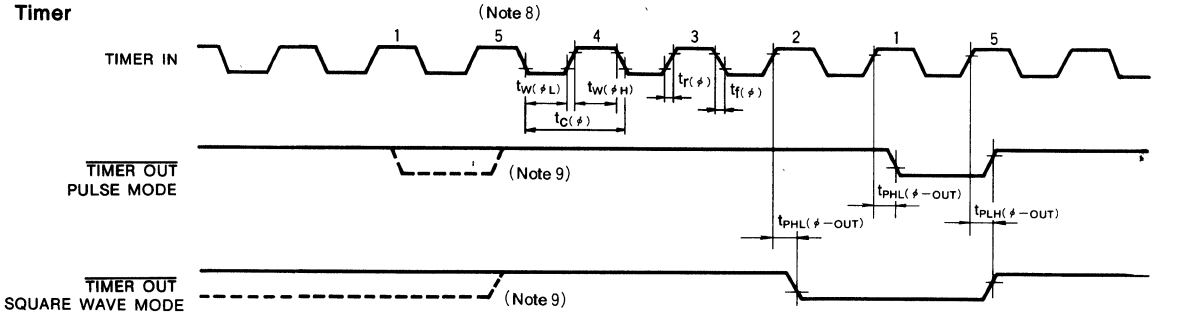
Strobed Output



Strobed Input



Timer



Note 8 : The wave form is shown for the case of counting down from 5 to 1
9 : As long as the M1 mode flag of the timer register is at high-level, pulses are continuously output.

M5L8156P

2048-BIT STATIC RAM WITH I/O PORTS AND TIMER

DESCRIPTION

The M5L8156P is a 2K-bit RAM (256-word by 8-bit) fabricated by the N-channel silicon-gate ED-MOS technology. This LSI has 3 I/O ports and a 14-bit counter/timer which make it a good extention of the functions of an 8-bit microcomputer It is packaged in a 40-pin plastic DIL package and operates with a single 5V power supply.

FEATURES

- Single 5V supply voltage
- TTL compatible
- Static RAM. 256-word by 8-bit
- Programmable 8-bit I/O port: 2
- Programmable 6-bit I/O port: 1
- Programmable counter/timer: 14-bit
- Multiplexed address/data bus

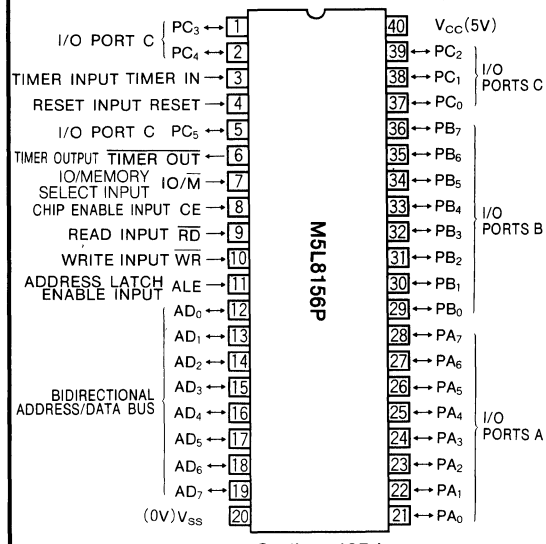
APPLICATION

Extension of I/O ports and timer function for MELPS 85 and MELPS 8-48 devices

FUNCTION

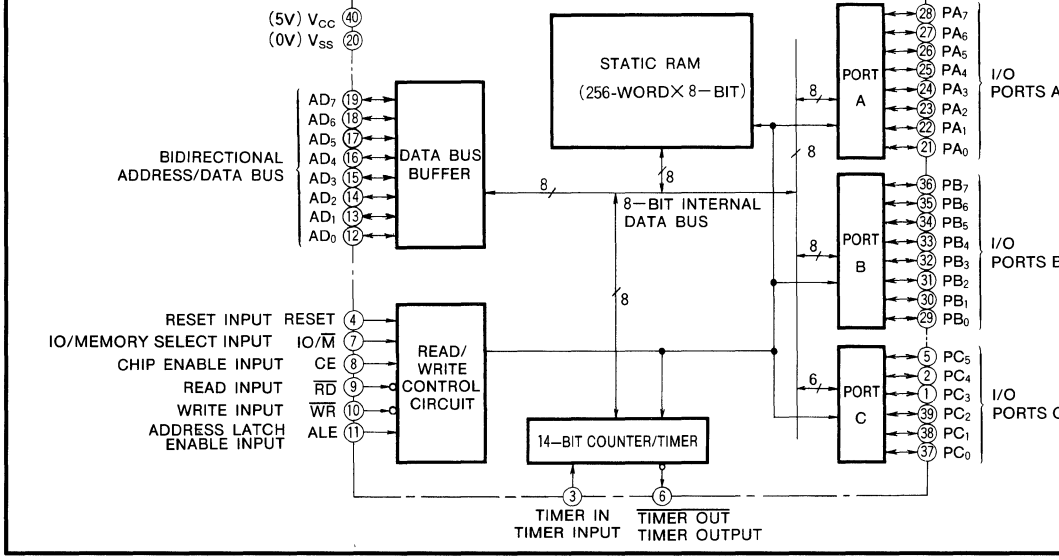
The M5L8156P is composed of RAM, I/O ports and counter/timer. The RAM is a 2K-bit static RAM organized as 256 words by 8 bits. The I/O ports consist of 2 programmable 8-bit ports and 1 programmable 6-bit port. The terminals of the 6-bit port can be programmed as control terminals for the 8-bit ports, so that the 8-bit ports can be operated in a handshake mode. The counter/timer is composed of 14-bit down counter (events or time) and it can generate square wave pulses that can be used for counting and timing.

PIN CONFIGURATION (TOP VIEW)



Outline 40P4

BLOCK DIAGRAM



OPERATION

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to transfer the data while input or output instructions are being executed by the CPU. Command and address information is also transferred through the data bus buffer.

Read/Write Control Logic

The read/write control logic controls the transfer of data and commands by interpreting the signals (CE, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, ALE and RESET) from CPU.

Bidirectional Address/Data Bus (AD_0~AD_7)

The bidirectional address/data bus is a 3-state 8-bit bus. The 8-bit address is latched in the internal latch by the falling edge of ALE. Then if IO/$\overline{M}$ input signal is at high-level, the address of I/O port, counter/timer, or command register is selected. If it is at low-level, address of RAM is selected. The 8-bit data is transferred by read input ($\overline{RD}$) or write input ($\overline{WR}$).

Chip Enable Input (CE)

When CE is at high-level, the address information on address/data bus is stored in the M5L8156P.

Read Input ($\overline{RD}$)

When $\overline{RD}$ is at low-level, the data bus buffer is active. If IO/$\overline{M}$ input signal is at low-level, the contents of RAM are read through the address/data bus. If IO/$\overline{M}$ input is at high-level, the contents of selected I/O port or counter/timer are read through the address/data bus.

Write Input ($\overline{WR}$)

When $\overline{WR}$ is at low-level, the data on the address/data bus are written into RAM if IO/$\overline{M}$ is at low-level, or they are written into I/O port, counter/timer or command register if IO/$\overline{M}$ is at high-level.

Address Latch Enable Input (ALE)

An address on the address/data bus is latched in the M5L8156P on the falling edge of ALE along with the levels of CE and IO/$\overline{M}$.

IO/Memory Input (IO/$\overline{M}$)

When IO/$\overline{M}$ is at low-level, the RAM is selected, while at high-level the I/O port, counter/timer or command register are selected.

I/O Port A (PA_0~PA_7)

Port A is an 8-bit general-purpose I/O port. Input/output setting is controlled by the system software.

I/O Port B (PB_0~PB_7)

Port B is an 8-bit general-purpose I/O port. Input/output setting is controlled by the system software.

I/O Port C (PC_0~PC_5)

Port C is a 6-bit I/O port that can also be used to output control signals of port A (PA) or port B (PB). The functions of port C are controlled by the system software. When port C is used to output control signals of ports A or B, the assignment of the signals to the pins is as shown in Table 1.

Table 1 Pin assignment of control signals of port C

Pin	Function	
PC_5	$\overline{B\ STB}$	(port B strobe)
PC_4	B BF	(port B buffer full)
PC_3	B INTR	(port B interrupt)
PC_2	$\overline{A\ STB}$	(port A strobe)
PC_1	A BF	(port A buffer full)
PC_0	A INTR	(port A interrupt)

Timer Input (TIMER IN)

The signal on this input terminal is used by the counter/timer for counting events or time. (3MHz max.)

Timer Output ($\overline{TIMER\ OUT}$)

A square wave signal or pulse from the counter/timer is output through this pin when in the operation mode.

Command Register (8 bits)

The command register is an 8-bit latched register. The low-order 4 bits (bits 0~3) are used for controlling and determination of the mode of the ports. Bits 4 and 5 are used as interrupt enable flags for ports A and B when port C is used as a control port. Bits 6 and 7 are used for controlling the counter/timer. The contents of the command register are rewritten by output instructions (I/O address XXXXX000). Details of the functions of the individual bits of the command register are shown in Table 2.

Table 2 Bit functions of the command register

Bit	Symbol	Function	
0	PA	PORT A I/O SET	1: Output port A 0: Input port A
1	PB	PORT B I/O SET	1. Output port B 0· Input port B
2	PC_1	PORT C SET	00. ALT1 11. ALT2 01. ALT3 10· ALT4
3	PC_2		
4	IEA	PORT A INTERRUPT ENABLE FLAG	1. Enable interrupt 0: Disable interrupt
5	IEB	PORT B INTERRUPT ENABLE FLAG	1· Enable interrupt 0: Disable interrupt
6	TM1	COUNTER/TIMER CONTROL 00. No influence on counter/timer operation 01. Counter/timer operation discontinued (If not already stopped) 10: Counter/timer operation discontinued after the current counter/timer operation is completed 11: Counter/timer operation started	
7	TM2		

Status Register (7-bit)

The status register is a 7-bit latched register. The low-order 6 bits (bits 0~5) are used as status flags for the I/O ports. Bit 6 is used as a status flag for the counter/timer. The contents of the status register are transferred into the CPU by reading (INPUT instruction, I/O address XXXXX000). Details of the functions of the individual bits of the status register are shown in Table 3.

Table 3 Bit functions of the status register

Bit	Symbol	Function
0	INTR A	PORT A INTERRUPT REQUEST
1	A BF	PORT A BUFFER FULL FLAG
2	INTE A	PORT A INTERRUPT ENABLE
3	INTR B	PORT B INTERRUPT REQUEST
4	B BF	PORT B BUFFER FULL FLAG
5	INTE B	PORT B INTERRUPT ENABLE
6	TIMER	COUNTER/TIMER INTERRUPT (This flag is set to 1 when the final limit of the counter/timer is reached and is reset to 0 when the status is read)
7	—	This bit is not used

I/O PORTS

Command/status registers (8-bit/7-bit)

These registers are assigned address XXXXX000. When an OUTPUT command is executed, the contents of the command register are rewritten. When an INPUT command is executed, the contents of the status register are read.

Port A Register (8-bit)

Port A Register is assigned address XXXXX001. This register can be programmed as an input or output by setting the appropriate bits of the command register as shown in Table 2.

Port A can be operated in basic or strobe mode and is assigned I/O terminal PA_0~PA_7.

Port B Register (8-bit)

Port B register is assigned address XXXXX010. As with Port A register, this register can be programmed as an input or output by setting the appropriate bits of the command register as shown in Table 2. Port B can be operated in basic or strobe mode and is assigned I/O terminals PB_0~PB_7.

Port C Register (6-bit)

Port C register is assigned address XXXXX011. This port is used not only for input or output but also for controlling input/output operations of ports A and B by selectively setting bits 2 and 3 of the command register as shown in Table 2. Details of the functions of the various setting of bits 2 and 3 are shown in Table 4. Port C is assigned I/O terminals PC_0~PC_5. When used as port control signals, the 3 low-order bits are assigned for port A while the 3 high-order bits are assigned for port B.

Table 4 Functions of port C

State Terminal	ALT 1	ALT 2	ALT 3	ALT 4
PC_5	Input	Output	Output	$\overline{\text{B STB}}$ (port B strobe)
PC_4	Input	Output	Output	B BF (port B buffer full)
PC_3	Input	Output	Output	B INTR (port B interrupt)
PC_2	Input	Output	$\overline{\text{A STB}}$ (port A strobe)	$\overline{\text{A STB}}$ (port A strobe)
PC_1	Input	Output	A BF (port A buffer full)	A BF (port A buffer full)
PC_0	Input	Output	A INTR (port A interrupt)	A INTR (port A interrupt)

CONFIGURATION OF PORTS

A block diagram of 1 bit of ports A and B is shown in Fig. 1. While port A or B is programmed as an output port, if the port is addressed by an input instruction, the contents of the selected port can be read. When a port is put in input mode, the output latch is cleared and writing into the output latch is disabled. Therefore when a port is changed to output mode from input mode, low-level signals are output through the port. When a reset signal is applied, all 3 ports (PA, PB, and PC) will be input ports and their output latches are cleared. Port C has the same configuration as ports A and B in modes ALT1 and ALT2.

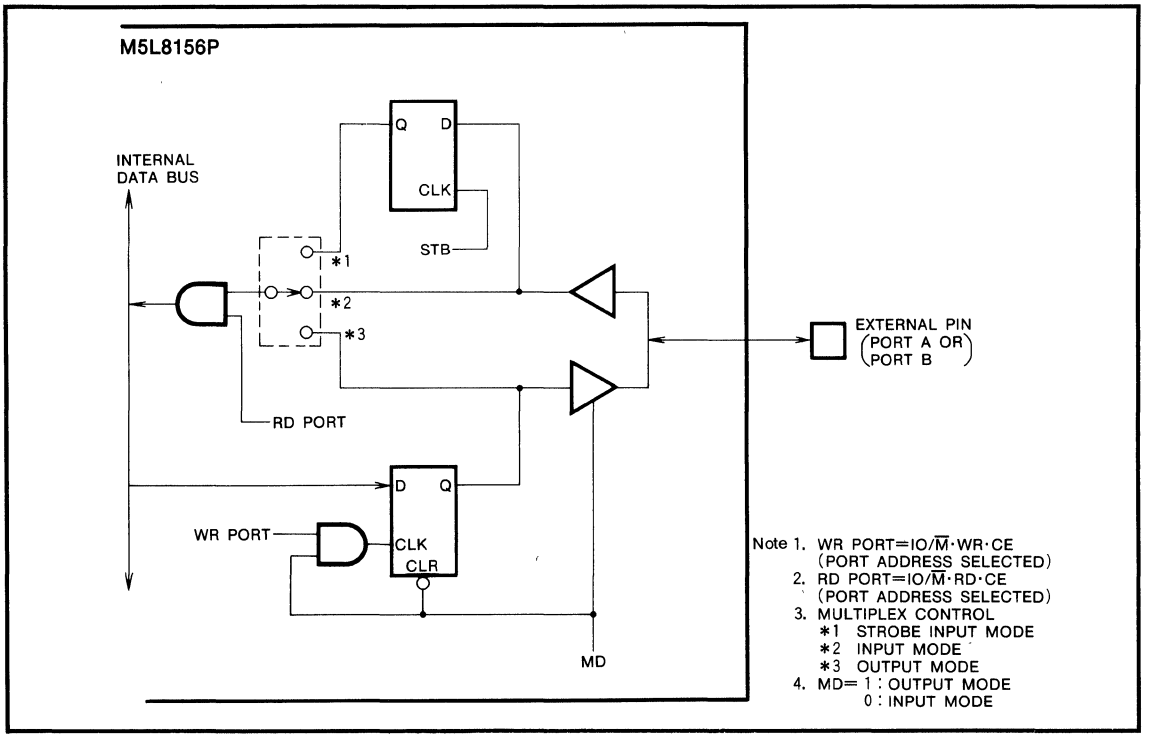


Fig. 1 Configuration for 1 bit of port A or B

Table 5 Basic functions of I/O ports

Address	$\overline{RD}$	$\overline{WR}$	Function
XXXXX000	L	H	AD bus ← Status register
	H	L	Command register ← AD bus
XXXXX001	L	H	AD bus ← Port A
	H	L	Port A ← AD bus
XXXXX010	L	H	AD bus ← Port B
	H	L	Port B ← AD bus
XXXXX011	L	H	AD bus ← Port C
	H	L	Port C ← AD bus

Table 6 Port control signal levels at ALT3 and ALT4

Control Signal	Output mode	Input mode
$\overline{STB}$	Input	Input
BF	"L"	"L"
INTR	"H"	"L"

The basic functions of the I/O ports are shown in Table 5. The control signal levels to ports A and B, when port C is programmed as a control port, are shown in Table 6.

COUNTER/TIMER

The counter/timer is composed of a 14-bit counting register and 2 mode flags. The register has two sections: I/O address XXXXX100 is assigned to the low-order 8 bits and I/O address XXXXX101 is assigned to the high-order 6 bits and timer mode flag 2 bits. The low-order bits 0～13 are used for counting or timing. The counter is initialized by the program and then counted down to 0. The initial value can be ranged from 2_{16} to $3FF_{16}$. Bits 14 and 15 are used as mode flags.

The mode flags select 1 of 4 modes with functions as follows:

Mode 0: Outputs high-level signal during the former half of the counter operation
Outputs low-level signal during the latter half of the counter operation

Table 7 Format of counter/timer

Address	Bit Number								Function
	7	6	5	4	3	2	1	0	
XXXXX100	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0	The low-order 8 bits of the counter register
XXXXX101	M_2	M_1	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	M2,M1 Timer mode T_{13}~T_8 The high-order 6 bits of the counter register

Table 8 Timer mode

M_2	M_1	Timer operation
0	0	Outputs high-level signal during the former half of the counter operation Outputs low-level signal during the latter half of the counter operation (mode 0)
0	1	Outputs square wave signals as in mode 0 (mode 1)
1	0	Outputs a low-level pulse during the final count down (mode 2)
1	1	Outputs a low-level pulse during each final count down (mode 3)

Mode 1: Outputs square wave signals as in mode 0
Mode 2: Outputs a low-level pulse during the final count down
Mode 3: Outputs a low-level pulse during each final count down

Starting and stopping the counter/timer is controlled by bits 6 and 7 of the command register (see Table 2 for details). The format and timer modes of the counter/timer register are shown in Table 7 and Table 8.

The contents of counter/timer is not affected by a reset, but counting is discontinued. To resume counting, a start command must be written into the command register as shown in Table 2. While operating 2n+1 count down in mode 0 and 1, a high-level signal is output during the former n+1 counting and a low-level signal is output during the later n counting.

RESET

The M5L8156P is reset by 600ns (min) pulse input on RESET pin.

By reset, all 3 ports are set to input mode. And counter/timer stops, but contents of counter/timer is not reset. Therefore it is necessary to input start command again.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5~7	V
V_I	Input voltage		−0.5~7	V
V_O	Output voltage		−0.5~7	V
P_d	Maximum power dissipation	T_a=25℃	1.5	W
T_{opr}	Operating free-air temperature range		−20~75	℃
T_{stg}	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Power-supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.5	V
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL}=2mA			0.45	V
I_I	Input leak current	V_I=0V, V_{CC}	−10		10	μA
$I_{I(CE)}$	Input leak current, CE pin	V_I=0V, V_{CC}	−100		100	μA
I_{OZ}	Output floating leak current	V_O=0V~V_{CC}	−10		10	μA
C_i	Input terminal capacitance	V_{IL}=0V, f=1MHz, 25mVrms, T_a=25℃			10	pF
$C_{i/O}$	Input/output terminal capacitance	$V_{I/OL}$=0V, f=1MHz, 25mVrms, T_a=25℃			20	pF
I_{CC}	Supply current from V_{CC}				180	mA

Note 5 : Current flowing into an IC is positive, out is negative.

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}= 5 V± 5 %, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(A-L)}$	Address setup time before latch		50			ns
$t_{h(L-A)}$	Address hold time after latch		80			ns
$t_{d(L-RW)}$	Delay time, latch to read/write		100			ns
$t_{w(L)}$	Latch pulse width		100			ns
$t_{d(RW-L)}$	Delay time, read/write to latch		20			ns
$t_{w(RW)}$	Read/write pulse width		250			ns
$t_{su(DQ-W)}$	Data setup time before write		150			ns
$t_{h(W-DQ)}$	Data hold time after write		0			ns
$t_{c(RW)}$	Read/write cycle time		300			ns
$t_{su(P-R)}$	Port setup time before read		70			ns
$t_{h(R-P)}$	Port hold time after read		50			ns
$t_{w(STB)}$	Strobe pulse width		200			ns
$t_{su(P-STB)}$	Port setup time before strobe		50			ns
$t_{h(STB-P)}$	Port hold time after strobe		120			ns
$t_{w(\phi H)}$	Timer input high-level pulse width		120			ns
$t_{w(\phi L)}$	Timer input low-level pulse width		80			ns
$t_{c(\phi)}$	Timer input cycle time		320		DC	ns
$t_{r(\phi)}$	Timer input rise time				30	ns
$t_{f(\phi)}$	Timer input fall time				30	ns

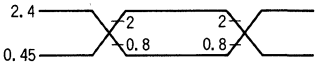
SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}= 5 V± 5 %, V_{SS}=0V, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Propagation time from read to data output	C_L = 150pF			170	ns
$t_{PZV(A-DQ)}$	Propagation time from address to data output				400	ns
$t_{PVZ(R-DQ)}$	Propagation time from read to data floating (Note 6)		0		100	ns
$t_{PHL(W-P)}$ / $t_{PLH(W-P)}$	Propagation time from write to data output				400	ns
$t_{PLH(STB-BF)}$	Propagation time from strobe to BF flag				400	ns
$t_{PHL(R-BF)}$	Propagation time from read to BF flag				400	ns
$t_{PLH(STB-INTR)}$	Propagation time from strobe to interrupt				400	ns
$t_{PHL(R-INTR)}$	Propagation time from read to interrupt				400	ns
$t_{PHL(STB-BF)}$	Propagation time from strobe to BF flag				400	ns
$t_{PLH(W-BF)}$	Propagation time from write to BF flag				400	ns
$t_{PHL(W-INTR)}$	Propagation time from write to interrupt				400	ns
$t_{PHL(\phi-OUT)}$ / $t_{PLH(\phi-OUT)}$	Propagation time from timer input to timer output				400	ns

Note 6 : Test conditions are not applied.

7 : A.C Testing waveform

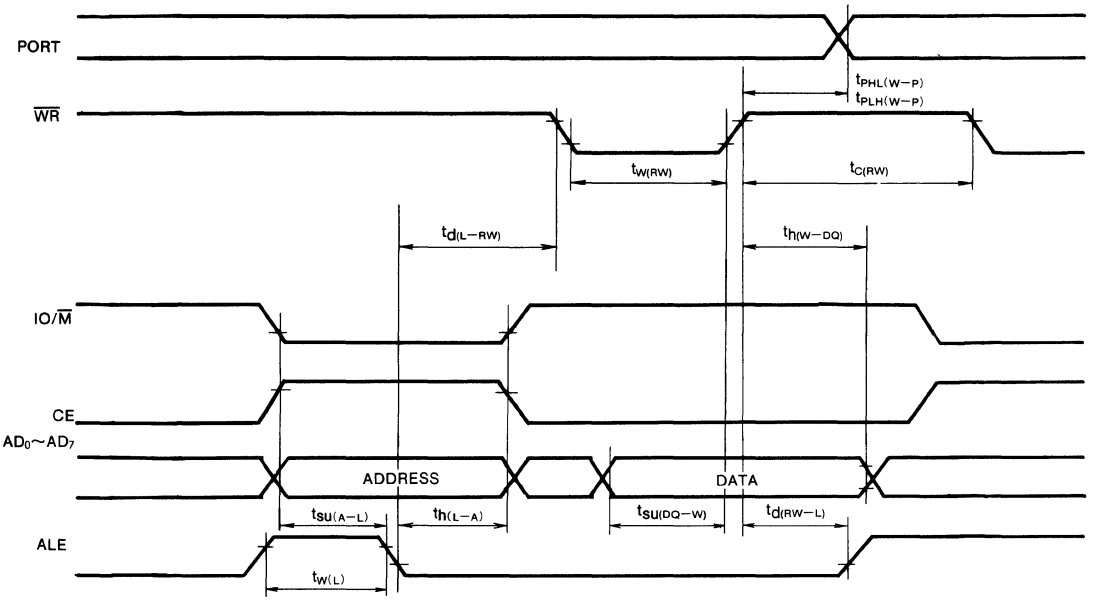
Input pulse level	0.45~2.4V
Input pulse rise time	20ns
Input pulse fall time	20ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V



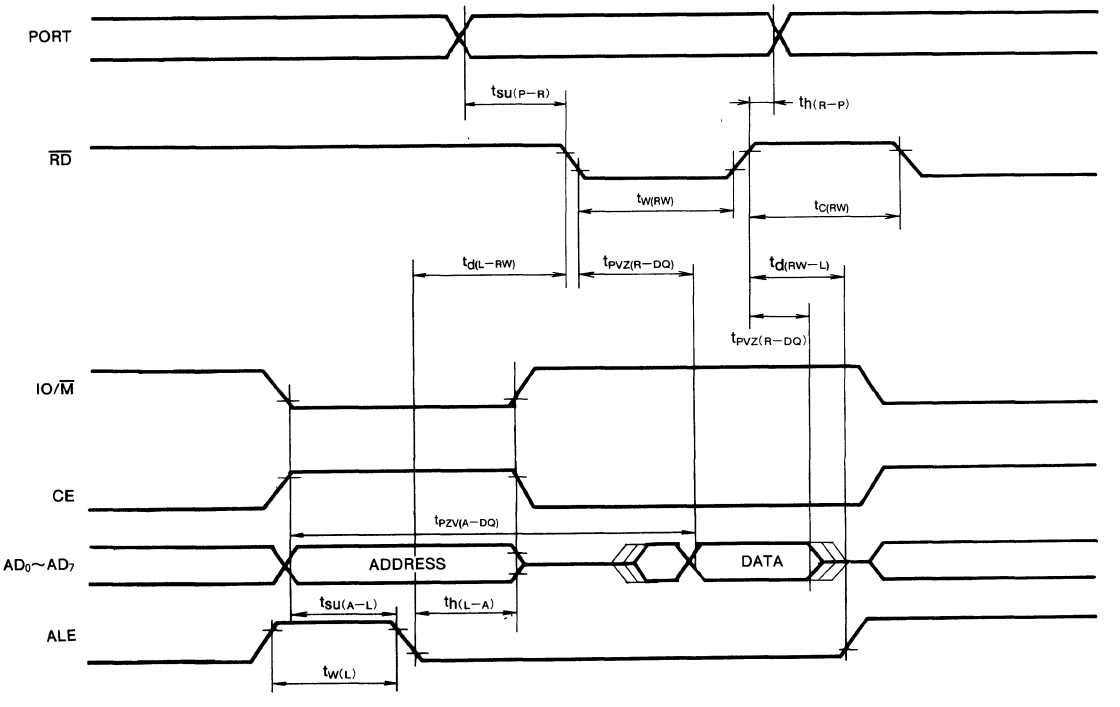
MITSUBISHI ELECTRIC

TIMING DIAGRAM

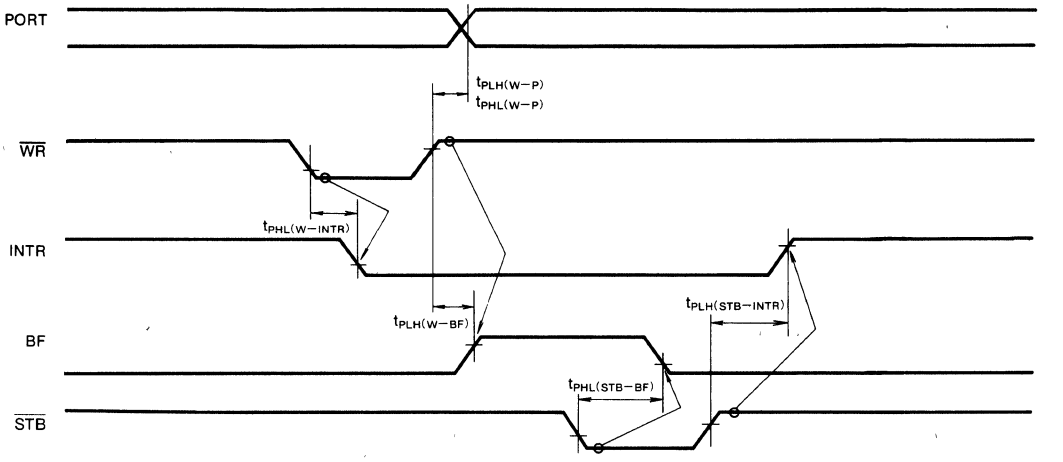
Basic Output



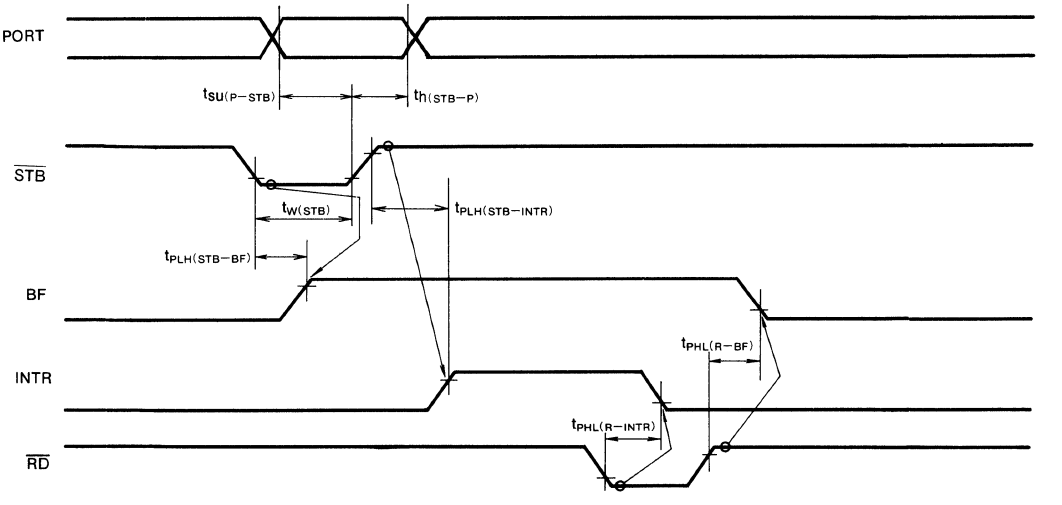
Basic Input



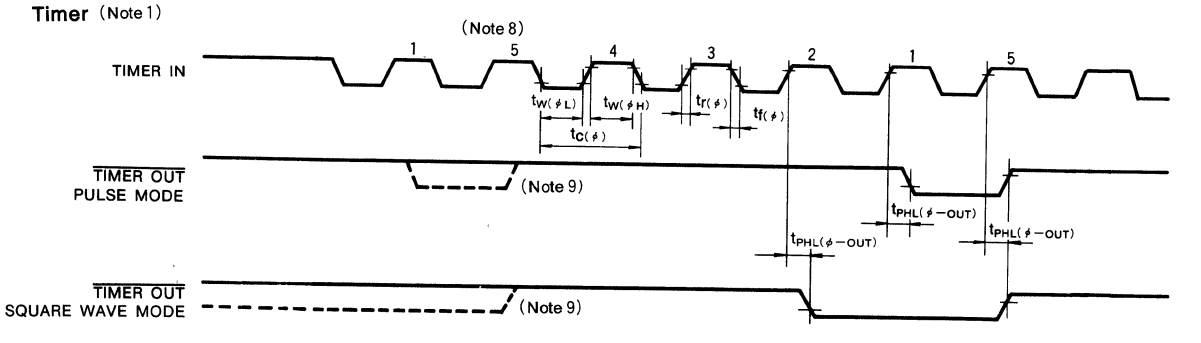
Strobed Output



Basic Input



Timer (Note 1)



Note 8 : The wave form is shown for the case of counting down from 5 to 1
9 : As long as the M1 mode flag of the timer register is at high-level, pulses are continuously output

M5L8251AP-5

PROGRAMMABLE COMMUNICATION INTERFACE

DESCRIPTION

The M5L8251AP-5 is a universal synchronous/asynchronous receiver/transmitter (USART) IC chip designed for data communications use. It is produced using the N-channel silicon-gate ED-MOS process and is mainly used in combination with 8-bit microprocessors.

FEATURES

- Single 5V supply voltage
- TTL compatible
- Synchronous and asynchronous operation
  - Synchronous:
    - 5~8-bit characters
    - Internal or external synchronization
    - Automatic SYNC character insertion
  - Asynchronous system:
    - 5~8-bit characters
    - Clock rate—1, 16or 64 times the baud rate
    - 1, 1½, or 2 stop bits
    - False-start-bit detection
    - Automatic break-state detection
- Baud rate: DC~64k-baud
- Full duplex, double-buffered transmitter/receiver
- Error detection: parity, overrun, and framing

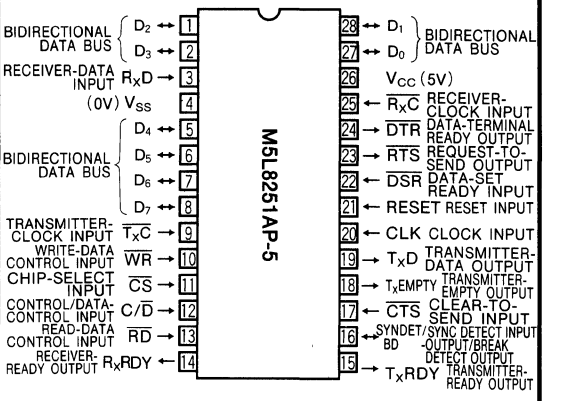
APPLICATION

Modem control of data communications using microcomputers. Control of CRT, TTY and other terminal equipment

FUNCTION

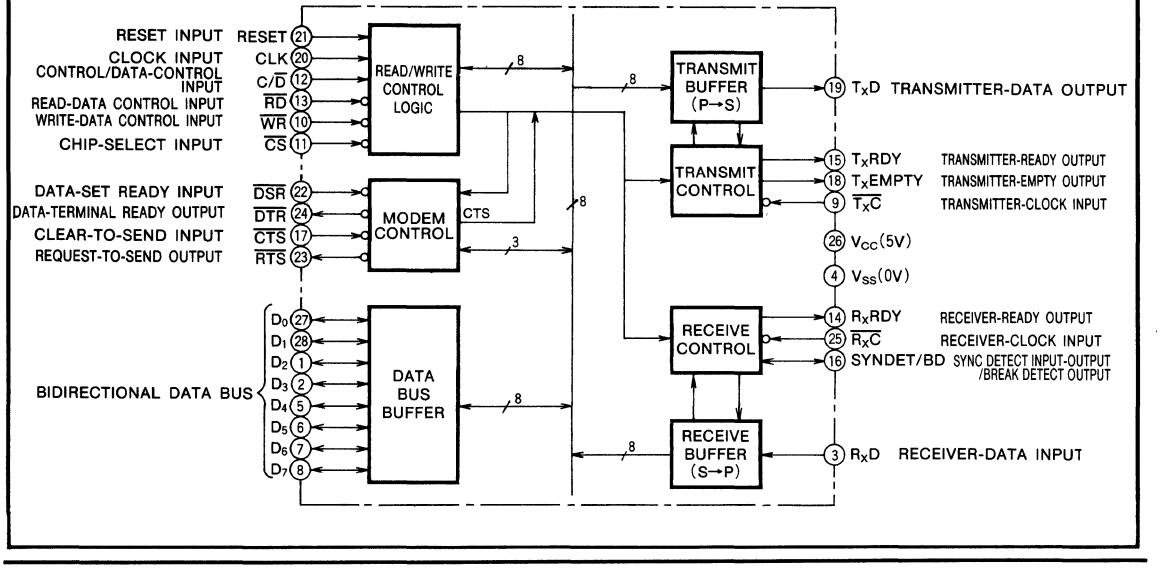
The M5L8251AP-5 is used in the peripheral circuits of a CPU. It permits assignments, by means of software, of operations in all the currently used serial-data transfer systems. The M5L8251AP-5 receives parallel-format data from the CPU, converts it into a serial format, and then transmits via the T_XD pin. It also receives data sent in via the R_XD pin from the external circuit, and converts it into a parallel format for sending to the CPU. On receipt of parallel-format data for transmission from the CPU or serial data for the CPU from external devices, the M5L8251AP-5 informs the CPU using the T_XRDY or R_XRDY pin. In addition, the CPU can read the M5L8251AP-5 status at any time. The M5L8251AP-5 can detect the data received for errors and inform the CPU of the presence of errors as status information. Errors include parity, overrun and frame errors.

PIN CONFIGURATION (TOP VIEW)



Outline 28P4

BLOCK DIAGRAM



OPERATION

The M5L8251AP-5 interfaces with the system bus as shown in Fig.1, positioned between the CPU and the modem or terminal equipment, and offers all the functions required for data communication.

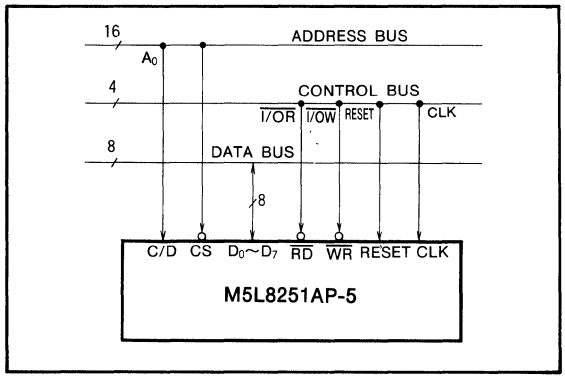


Fig. 1 M5L8251AP-5 interface to CPU system bus

When using the M5L8251AP-5, it is necessary to program, as the initial setting, assignments for synchronous/asynchronous mode selection, baud rate, character length, parity check, and even/odd parity selection in accordance with the communication system used. Once programming is completed, functions appropriate to the communication system can be carried out continuously.

When initial setting of the USART is completed, data communication becomes possible. Though the receiver is always in the enable state, the transmitter is placed in the transmitter-enable state (T_XEN) by a command instruction, and the application of a low-level signal to the $\overline{CTS}$ pin prompts data-transfer start-up. Until this condition is satisfied, transmission is not executed. On receiving data, the receiver informs the CPU that reading for the receiver data in the USART by the CPU has become possible (the R_XRDY terminal has turned to high-level). Since data reception and the entry of the CPU into the data-readable state are output as status information, the CPU can access USART status without accessing the R_XRDY terminal.

During receiving operation, the USART checks errors and gives out status information. There are three types of errors: parity, overrun, and frame. Even though an error occurs, the USART continues its operations, and the error state is retained until error reset (ER) is effected by a command instruction. The M5L8251AP-5 access methods are listed in Table 1.

Table 1 M5L8251AP-5 Access Methods

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Function
L	L	H	L	Data bus ← Data in USART
L	H	L	L	USART ← Data bus
H	L	H	L	Data bus ← Status
H	H	L	L	Control ← Data bus
X	H	H	L	3-State ← Data bus
X	X	X	H	3-State ← Data bus

Read/Write Control Logic

This logic consists of a control word register and command word register. It receives signals from the CPU control bus and generates internal-control signals for the elements.

Modem Control Circuit

This is a general-purpose control-signal circuit designed to simplify the interface to the modem. Four types of control signal are available: output signals $\overline{DTR}$ and $\overline{RTS}$ are controlled by command instructions, input signal $\overline{DSR}$ is given to the CPU as status information and input signal $\overline{CTS}$ controls direct transmission.

Data-Bus Buffer

This is an 8-bit 3-state bidirectional bus through which control words, command words, status information, and transfer data are transferred. Fig. 2 shows the structure of the data-bus buffer.

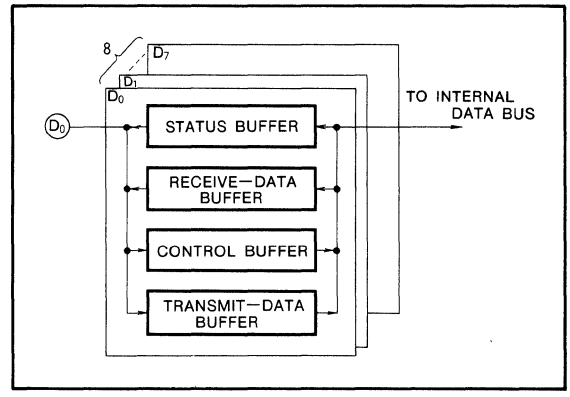


Fig. 2 Data-bus-buffer structure

Transmit Buffer

This buffer converts parallel-format data given to the data-bus buffer in to serial data with addition of a start bit, stop bits and a parity bit, and sends out the converted data through the T_XD pin based on the control signal.

Transmit-Control Circuit

This circuit carries out all the controls required for serial data transmission. It controls transmitter data and outputs the signals required by external devices in accordance with the instructions of the read/write control logic.

Receive Control Circuit
This circuit offers all the controls required for normal reception of the input serial data. It controls receiver data and outputs signals for the external devices in accordace with the instructions of the read/write control logic.

Receive Buffer
This buffer converts serial data given via the R_XD pin into a parallel format, checks the bits and characters in accordance with the communication format designated by mode setting, and transfers the assembled characters to the CPU via the data-bus buffer.

Receiver-Data Input (R_XD)
Serial characters sent from another device are input to this pin and converted to a parallel-character format to serve as data for the CPU. Unless the high-level state is detected after a chip-master reset procedure (this resetting is carried out to prevent spurious operation such as that due to faulty connection of the R_XD to the line in a break state), the serial characters are not received. This applies to only the asynchronous mode. When the R_XD line enters the low-level state instantaneously because of noise, etc, the mis-start prevention function starts working. That is, the start bit is detected by its falling edge but in order to make sure that it is the correct start bit, the R_XD line is strobed at the middle of the start bit to reconfirm the low-level state. If it is found to be high-level a faulty-start judgment is made.

Transmitter-Clock Input ($\overline{T_XC}$)
This clock controls the baud rate for character transmission from the T_XD pin. Serial data is shifted by the falling edge of the $\overline{T_XC}$ signal. In the synchronous mode, the $\overline{T_XC}$ frequency is equal to the actual baud rate. In the asynchronous mode, the frequency is specified as 1, 16, or 64 times the baud rate by the mode setting.

Example When the baud rate is 110 bauds:
$\overline{T_XC}$=110Hz(1X)
$\overline{T_XC}$=1.76kHz(16X)
$\overline{T_XC}$=7.04kHz(64X)

Write-Data Control Input ($\overline{WR}$)
Data and control words output from the CPU by the low-level input are written in the M5L8251AP-5. This terminal is usually used in a form connected with the control bus $\overline{I/OW}$ of the CPU.

Chip-Select Input ($\overline{CS}$)
This is a device-select signal that enables the USART by a low-level input. Usually, it is connected to the address bus directly or via the decoder. When this signal is in the high-level state, the M5L8251AP-5 is disabled.

Control/Data Control Input (C/$\overline{D}$)
This signal shows whether the information on the USART data bus is in the form of data characters or control words, or in the form of status information, in accordance with the $\overline{RD}$ and $\overline{WR}$ inputs while the CPU is accessing the M5L8251AP-5. The high-level identifies control words or status information, and the low-level, data characters.

Read-Data Control Input ($\overline{RD}$)
Receiver data and status information are output from the CPU by a low-level input for the CPU data bus.

Receiver-Ready Output (R_XRDY)
This signal indicates that the received characters have entered the receiver buffer, and further, the receiver-data buffer in the data-bus buffer shown in Fig. 2. It is possible to confirm the R_XRDY status by using this signal as an interruption signal for the CPU or by allowing the CPU to read the D_1 bit of the status information by polling. The R_XRDY is automatically reset when a character is read by the CPU. Even in the break state in which the R_XD line is held at low-level, the R_XRDY remains active. It can be masked by making the $R_XE(D_2)$ of the command instruction 0.

Transmitter-Ready Output (T_XRDY)
This signal shows that the data is ready for transmission. It is possible to confirm the status of serial-data transmission by using it as an interruption signal for the CPU or by allowing the CPU to read the D_0 bit of the status information by polling. Since the T_XRDY signal shows that the data buffer is empty, it is automatically reset when a transmission character is loaded by the CPU. The T_XRDY bit of the status information means that the transmit-data buffer shown in Fig. 2 has become empty, while the T_XRDY pin enters the high-level state only when the transmit-data buffer is empty, T_XEN equals 1, and a low-level input has been applied to the $\overline{CTS}$ pin.

Status (D_0): When transmit-data buffer (TDB) is empty, it becomes 1.
T_XRDY terminal: When (TDB is empty)·(T_XEN=1)·(CTS = "L") = "H" or resetting, it becomes active.

Sync Detect/Break Detect Output-Input (SYNDET/BD)
In the synchronous mode this pin is used for input and output operations. When it is specified for the internal synchronous mode by mode setting, this pin works as an output terminal. It enters the high-level state when a SYNC character is received through the R_XD pin. If the M5L8251AP-5 has been programmed for double SYNC characters (bi-sync), a high-level is entered in the middle of the last bit of the second SYNC character. This signal is automatically reset by reading the status information.

On designation of the M5L8251AP-5 to the external synchronous mode, this pin begins to serve for input operations. Applying a high-level signal to this pin prompts the M5L8251AP-5 to begin assembling data characters at the next rising edge of the $\overline{R_XC}$. For the width of a high-level signal to be input, a minimum $\overline{R_XC}$ period is required.

Designation of the asynchronous mode causes this pin to function as a BD (output) pin. When the start, data, and parity bits and stop bits are all 0 for two characters period, a high-level is entered. The BD (break detect) signal can also be read as the D_6 bit of the status information. This signal is reset by resetting the chip master or by the R_XD line's recovering the high-level state.

Clear-To-Send Input ($\overline{CTS}$)

When the T_XEN bit (D_0) of the command instruction has been set to 1 and the $\overline{CTS}$ input is low-level serial data is sent out from the T_XD pin. Usually this is used as a clear-to-send signal for the modem

Note: CTS indicates the modem status as follows:
ON means data transmission is possible;
OFF means data transmission is impossible.

Transmitter-Empty Output (T_XEMPTY)

When no transmisison characters are left in the transmit buffer, this pin enters the high-level state. In the asynchronous mode, the following transmission character is shifted to the transmit buffer when it is loaded from the CPU. Thus, it is automatically reset. In the synchronous mode, a SYNC character is loaded automatically on the transmit buffer when no transfer-data characters are left. In this case, howeyer, the T_XEMPTY does not enter the low-level state when a SYNC character has been sent out, since T_XEMPTY="H" denotes the state in which there is no transfer character and one or two SYNC characters are being transferred or the state in which a SYNC character is being transferred as a filler. T_XEMPTY is unrelated to the T_XEN bit of the command instruction.

Transmission-Data Output (T_XD)

Parallel-format transmission characters loaded on the M5L8251AP-5 by the CPU are assembled into the format designated by the mode instruction and sent in serial-data form via the T_XD pin. Data is output, however, only in cases where the D_0 bit (T_XEN) of the command instruction is 1 and the $\overline{CTS}$ terminal is in the low-level state. Once reset, this pin is kept at the mark status (high level) until the first character is sent.

Clock Input (CLK)

This system-clock input is required for internal-timing generation and is usually connected to the clock-output (CLK) pin of the M5L8085AP. Although there is no direct relation with the data-transfer baud rate, the clock-input (CLK) frequency is more than 30 times the $\overline{T_XC}$ or $\overline{R_XC}$ input frequency in the case of the synchronous system and more than 4.5 times in the case of the asynchronous system.

Reset Input (RESET)

Once the USART is shifted to the idle mode by a high-level input, this state continues until a new control word is set Since this is a master reset, it is always necessary to load a control word following the reset process. The reset input requires a minimum 6-clock pulse width.

Data-Set Ready Input ($\overline{DSR}$)

This is a general-purpose input signal, but is usually used as a data-set ready signal to test modem status. Its status can be known from the status reading process. The D_7 bit of the status information equals 1 when the $\overline{DSR}$ pin is in the low-level state, and 0 when in the high-level state.

$\overline{DSR}$="L"→D_7 bit of status information=1
$\overline{DSR}$="H"→D_7 bit of status information=0

Note: DSR indicates modem status as follows:
ON means the modem can transmit and receive;
OFF means it cannot.

Request-To-Send Output ($\overline{RTS}$)

This is a general-purpose output signal but is used as a request-to-send signal for the modem. The $\overline{RTS}$ terminal is controlled by the D_5 bit of the command instruction. When D_5 is equal to 1, $\overline{RTS}$="L", and when D_5 is 0, $\overline{RTS}$="H".

Command register D_5=1→$\overline{RTS}$="L"
Command register D_5=0→$\overline{RTS}$="H"

Note: RTS controls the modem transmission carrier as follows:
ON means carrier dispatch;
OFF means carrier stop.

Data-Terminal Ready Output ($\overline{DTR}$)

This is a general-purpose output signal, but is usually used as a data-terminal ready or rate-select signal to the modem. The $\overline{DTR}$ pin is controlled by the D_1 bit of the command instruction; if D_1=1, $\overline{DTR}$="L", and if D_1=0, $\overline{DTR}$="H".

D_1 of the command register=1→$\overline{DTR}$="L"
D_1 of the command register=0→$\overline{DTR}$="H"

Receiver-Clock Input ($\overline{R_XC}$)

This clock signal controls the baud rate for the sending in of characters via the $\overline{R_XD}$ pin. The data is shifted in by the rising edge of the $\overline{R_XC}$ signal. In the synchronous mode, the $\overline{R_XC}$ frequency is equal to the actual baud rate. In the asynchronous mode, the frequency is specified as 1, 16, or 64 times the baud rate by mode setting. This relationship is parallel to that of $\overline{T_XC}$, and in usual communication-line systems the transmission and reception baud rates are equal. The $\overline{T_XC}$ and $\overline{R_XC}$ terminals are, therefore, used connected to the same baud-rate generator.

PROGRAMMING

It is necessary for the M5L8251AP-5 to have the control word loaded by the CPU prior to data transfer. This must always be done following any resetting operation (by external RESET pin or command instruction IR). There are two types of control words: mode instructions specifying general operations required for communications and command instructions to control the M5L8251AP-5 actual operations.

Following the resetting operation, a mode instruction must be set first. This instruction sets the synchronous or asynchronous system to be used. In the sysnchronous system, a SYNC character is loaded from the CPU. In the case of the bi-sync system, however, a second SYNC character must be loaded in succession.

Loading a command instruction makes data transfer possible. This operation after resetting must be carried out for initializing the M5L8251AP-5. The USART command instruction contains an internal-reset IR instruction (D_6bit) that makes it possible to return the M5L8251AP-5 to its reset state. The initialization flowchart is shown in Fig. 3 and the mode-instruction and command-instruction formats are shown in Figs. 4 and 5.

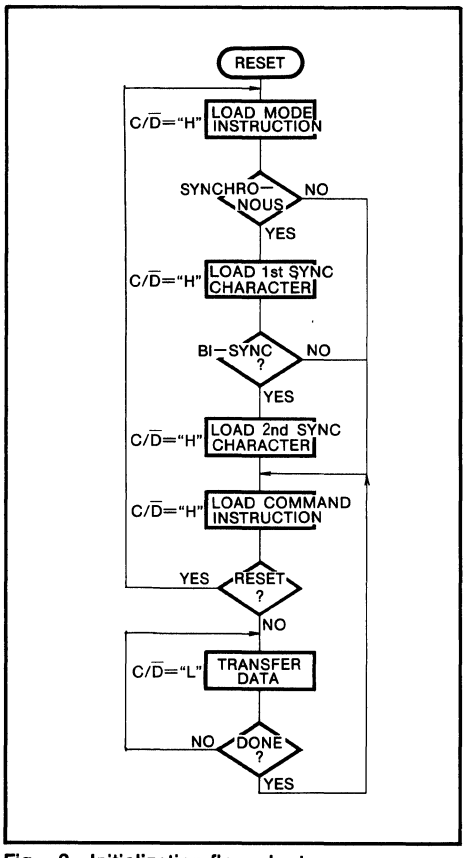


Fig. 3 Initialization flow chart

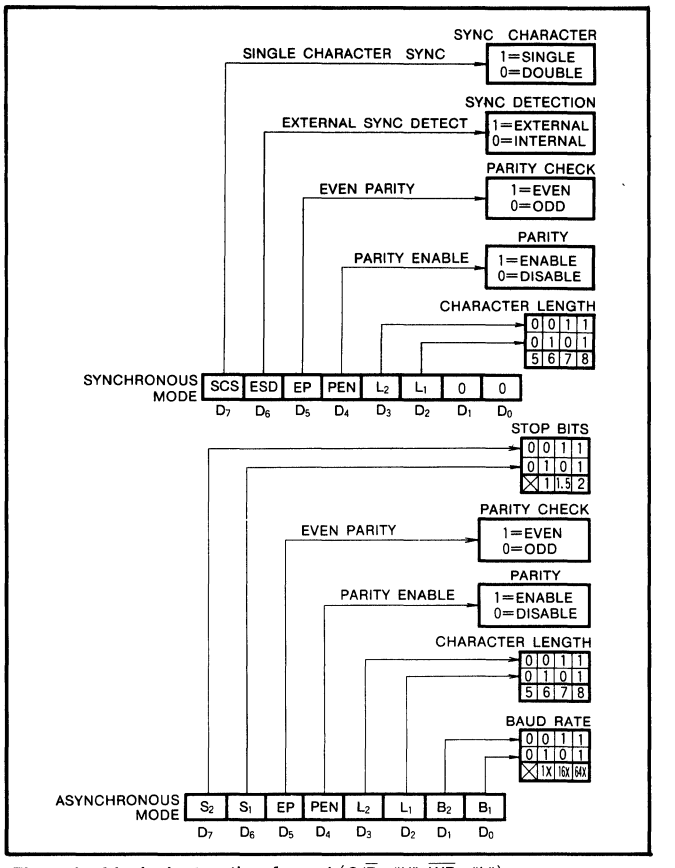


Fig. 4 Mode-instruction format (C/$\overline{D}$="H", $\overline{WR}$="L")

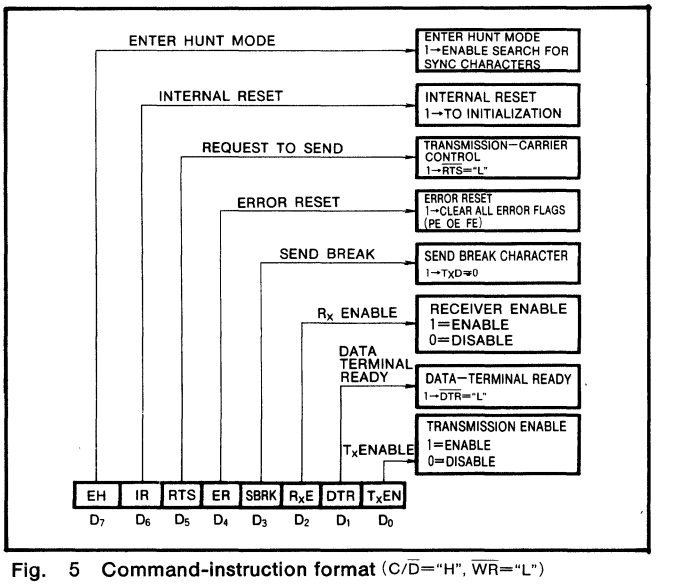


Fig. 5 Command-instruction format (C/$\overline{D}$="H", $\overline{WR}$="L")

Asynchronous Transmission Mode

When data characters are loaded on the M5L8251AP-5 after initial setting, the USART automatically adds a start bit (0), an odd or even parity bit specified by the mode instruction during initialization, and a specified number of stop bits (1). After that, the assembled data characters are transferred as serial data via the T_XD pin, if transfer is enabled ($T_XEN = 1 \cdot \overline{CTS}$ = "L"). In this case, the transfer data (baud rate) is shifted by the mode instruction at a rate of 1X, 1/16X, or 1/64X the $\overline{T_XC}$ period.

If the data characters are not loaded on the M5L8251AP-5, the T_XD pin enters a mark state ("H"). When SBRK is programmed by the command instruction, break characters (0) are output continuously through the T_XD pin.

Asynchronous Reception Mode

The R_XD line usually starts operations in a mark state ("H"), triggered by the falling edge of a low-level pulse when it comes to this line. This signal is again strobe at the middle of the bit to confirm that it is a perfect start bit. The detection of a second low-level indicates the validity of the start bit (again strobe is carried out only in the case of 16X and 64X). After that, the bit counter inside the M5L8251AP-5 starts operating; each bit of the serial information on the R_XD line is shifted in by the rising edge of $\overline{R_XC}$, and the data bit, parity bit (when necessary), and stop bit are sampled at the middle position.

The occurrence of a parity error causes the setting of a parity-error flag. If the stop bit is 0, a frame error flag is set. Attention should be paid to the fact that the receiver requires only one stop bit even though the program has designated 1/1.5 or 2 stop bits.

Reception up to the stop bit means reception of a complete character. This character is then transferred to the receiver-data buffer shown in Fig.2, and the R_XRDY becomes active. In cases where this character is not read by the CPU and where the next character is transferred to the receiver-data buffer, the preceding character is destroyed and an overrun-error flag is set.

These error flags can be read as the M5L8251AP-5 status information. The occurrence of an error does not stop USART operations. The error flags are cleared by the ER(D_4 bit) of the command instruction.

The asynchronous-system transfer formats are shown in Figs. 6 and 7.

Synchronous Transmission Mode

In this mode the T_XD pin remains in the high-level state until initial setting by the CPU is completed. After initialization, the state of $\overline{CTS}$="L" and T_XEN =1 enables serial transmission of characters through the T_XD pin. Then, data characters are sent out and shifted by the falling edge of the $\overline{T_XC}$ signal. The transmission rate equals the $\overline{T_XC}$ rate.

Thus, once data-character transfer starts, it must continue through the T_XD pin at the same rate as that of $\overline{T_XC}$. Unless data characters are provided from the CPU before the transmitter buffer becomes empty, one or two SYNC characters are automatically output from the T_XD pin In this case, it should be noted that the T_XEMPTY pin enters the high-level state when there are no data characters left in the M5L8251AP-5 to be transferred, and that the low-level state is not entered until the USART is provided with the next data character from the CPU. Care should also be taken over the fact that merely setting a command instruction does not effect SYNC-character insertion, because the SYNC character insertion is enabled after sending out the first data character.

In this mode, too, break characters are sent out in succession from the T_XD pin when SBRK is designated (D_3=1) by a command instruction.

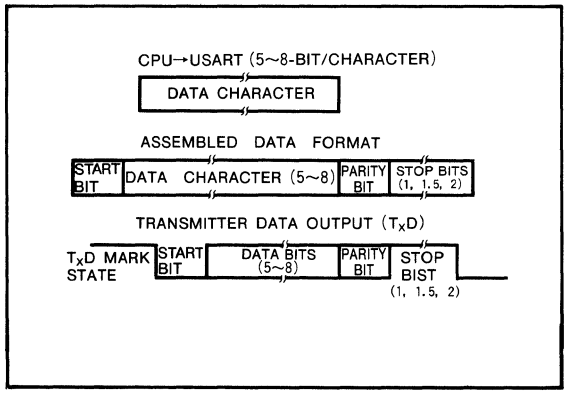
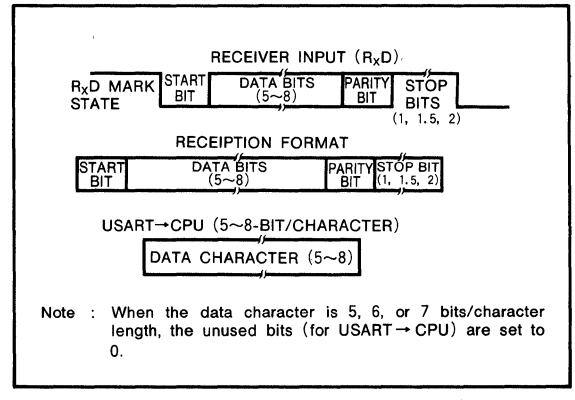


Fig. 6 Asynchronous transmission format I (transmission)



Note : When the data character is 5, 6, or 7 bits/character length, the unused bits (for USART→CPU) are set to 0.

Fig. 7 Asynchronous transmission format II (reception)

Synchronous Reception Mode

Character synchronization in this mode is carried out internally or externally by initial-setting designation.

Programming in the internal synchronous mode requires that an EH instruction ($D_7 = 1$, enter hunt mode) is included in the first command instruction. Data on the R_XD pin is sampled by the rising $\overline{R_XC}$ signal, and the receiver-buffer contents are compared with the SYNC character each time a bit is input. Comparison continues until an agreement is reached. When the M5L8251AP-5 has been programmed in the bi-sync mode, data received in further succession is compared. The detection of two SYNC characters in succession makes the USART end the hunt mode, setting the SYNDET pin to the high-level state. This reset operation is prompted by the reading of the status information. When the parity has been programmed, SYNDET is not set in the middle of the last data bit but in the middle of the parity bit.

In the external synchronous mode, the M5L8251AP-5 gets out of the hunt mode when a high-level synchronization signal is given to the SYNDET pin. The high-level signal requires a minimum duration of one $\overline{R_XC}$ cycle. In the asynchronous mode, however, the EH signal does not affect the operation at all.

Parity and overrun errors are checked in the same way as in the asynchronous system. During hunt-mode operations the parity bit is not checked, but parity checking is carried out even when the receiver is disabled.

The CPU can command the receiver to enter the hunt mode, if synchronization is lost. This prevents the SYNC character from erroneously becoming equal to the received data when all the data in the receiver buffer is set to 1 Attention should be paid to the fact that the SYNDET F/F is reset each time status information is read irrespective of the synchronous mode's being internal or external. This, however, does not return the M5L8251AP-5 to the hunt mode. Synchronism detection is carried out even though it is not the hunt mode. The synchronous transfer formats are shown in Figs. 8 and 9.

Command Instruction

This instruction defines actual operations in the communication mode designated by mode setting. Command instructions include transmitter/receiver enable error-reset, internal-reset, modem-control, enter-hunt and break transmission instructions.

The mode is set following the reset operation. A SYNC character is set as required, and the writing of high-level signals on the control/data pin ($C/\overline{D}$) that follows it is regarded as a command instruction. When the mode is set all over again from the beginning, the M5L8251AP-5 can be reset by using inputting via the reset terminal or by internal resetting based on the command instruction.

Note 1: The command error reset (ER), internal reset (IR) and enter-hunt-mode (EH) operations are only effective when the command instruction is loaded, so that these bits need not be returned to 0.

2: When a break character is sent out by a command, the T_XD set to 0 immediately irrespective of whether or not the USART has sent out data.

3: Operations of the USART's receiver section which is always in the enable state cannot be inhibited. The command instruction $R_XE = 0$ does not mean that data reception via the R_XD pin is inhibited; it means that the R_XRDY is masked and error flags are inhibited.

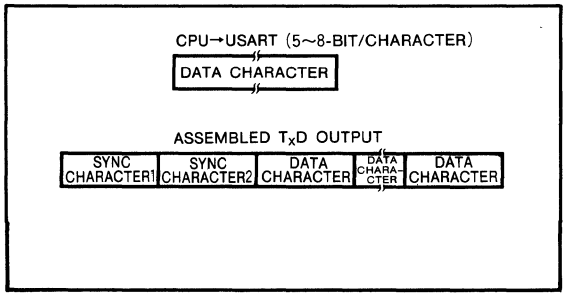


Fig. 8 Synchronous transmission format I (transmission)

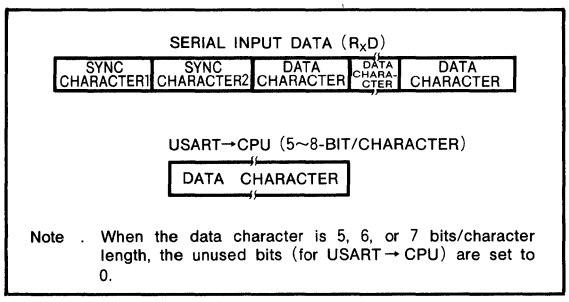


Fig. 9 Synchronous transmission format II (reception)

STATUS INFORMATION

The CPU can always read USART status by setting the C/$\overline{D}$ to high-level and $\overline{RD}$ to low-level.

The status information format is shown in Fig. 10. In this format R_XRDY, T_XEMPTY and SYNDET have the same definitions as those of the pins. This means that these three pieces of status information become high-level when each pin is 1. The other status information is defined as follows:

DSR: When the $\overline{DSR}$ pin is in the low-level state, status information DSR becomes 1.

FE: The occurrence of a frame error in the receiver section makes the status information FE=1.

OE: The occurrence of an overrun error in the receiver section makes the status information OE=1.

PE: The occurrence of a parity error in the receiver section makes this status information PE=1.

T_XRDY: This information becomes 1 when the transmit data buffer is empty. Be careful because this has a different meaning from the T_XRDY pin that enters the high-level state only when the transmitter buffer is empty, when the $\overline{CTS}$ pin is in the low-level state, and when T_XEN is 1.

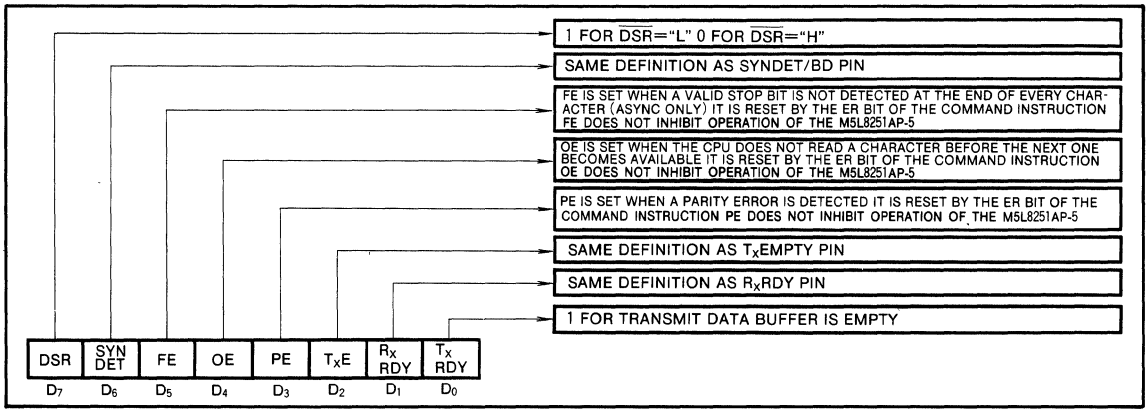


Fig. 10 Status information (C/$\overline{D}$="H", $\overline{WR}$="L")

APPLICATION EXAMPLES

Fig. 11 shows an application example for the M5L8251AP-5 in the asynchronous mode. When the port addresses of the M5L8251AP-5 are assumed to be 00# and 01# in this figure, initial setting in the asynchronous mode is carried out in the following manner:

```
MVI    A, B6#    Mode setting
OUT    01#
MVI    A, 27#    Command instruction
OUT    01#
```

In this case, the following are set by mode setting:

Asynchronous mode
6 bits/character
Parity enable (even)
1.5 stop bits
Baud rate: 16X

Command instructions set the following

RTS=1→$\overline{RTS}$ pin="L"
R_XE=1
DTR=1→$\overline{DTR}$ pin="L"
T_XEN=1

When the initial setting is complete, transfer operations are allowed. The $\overline{RTS}$ pin is initially set to the low-level by setting RTS to 1, and this serves as a $\overline{CTS}$ input with T_XEN being equal to 1. For this reason the same definition applies to the status and pin of T_XRDY, and 1 is assigned when the transmit-data buffer is empty. Actual transfer of data is carried out in the following way:

```
IN     01#       Status read
```

The IN instruction prompts the CPU to read the USART's status. The result is; if the T_XRDY equals 1 transmitter data is sent from the CPU and written on the M5L8251AP-5. Transmitter data is written in the M5L8251AP-5 in the following manner:

```
MVI    A, 2D#    2D16 is an example of transmitter data.
OUT    00#       USART←(A)
```

Receiver data is read in the following manner:

```
IN     00#       (A)←USART
```

In the above example, the status information is read and as a result, the transmitter data is written and read. Interruption processing by using the T_XRDY and R_XRDY pins is also possible.

Fig. 12 shows the status of the T_XD pin when data written in the USART is transferred from the CPU. When the data shown in Fig.12 enters the R_XD pin, data sent from the M5L8251AP-5 to the CPU becomes $2D_{16}$ and bits D_6 and D_7 are treated as 0.

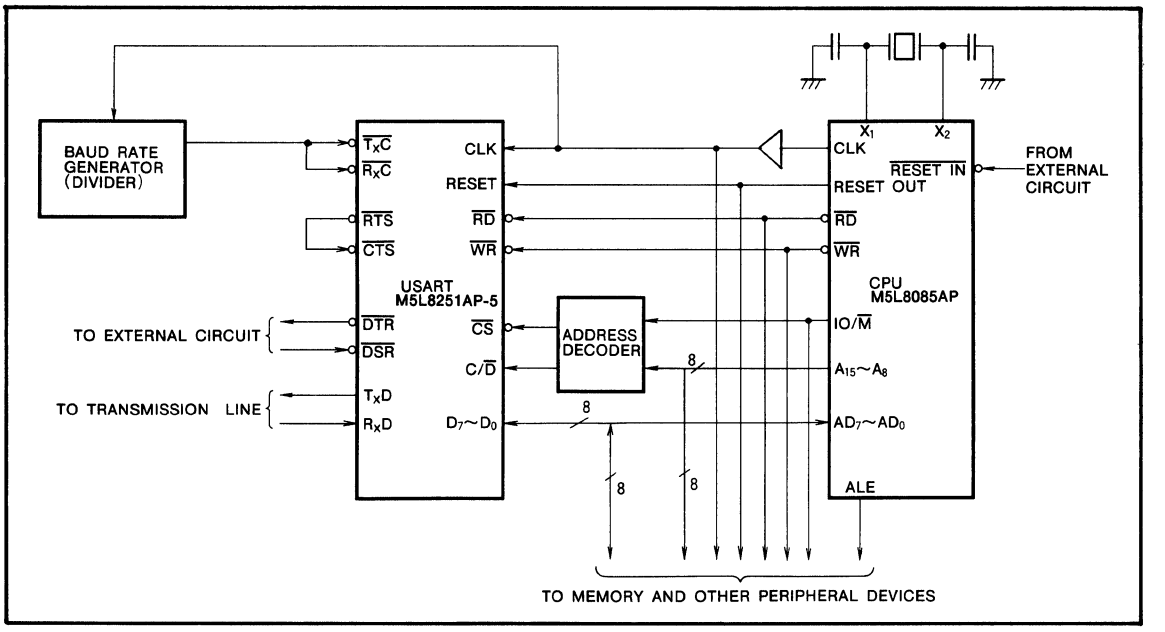


Fig. 11 Example of circuit using the asynchronous mode

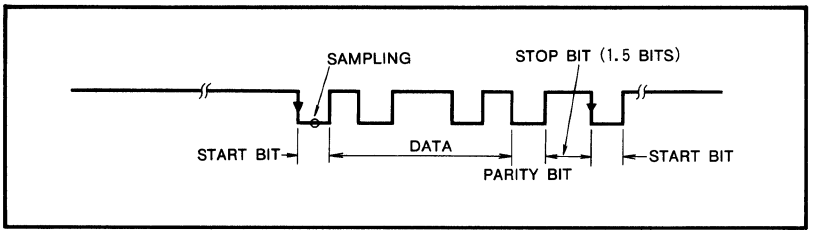


Fig. 12 Example of data transmission

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power-supply voltage	With respect to V_{SS}	−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating free-air temperature range		−20～75	℃
T_{stg}	Storage temperature range		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Power-supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20～75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}	V
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL}=2.2mA			0.45	V
I_{CC}	Supply current from V_{CC}	All outputs are high-level			100	mA
I_{IH}	High-level input current	V_I=V_{CC}	−10		10	μA
I_{IL}	Low-level input current	V_I=0.45V	−10		10	μA
I_{OZ}	Off-state input current	V_O=0.45V～V_{CC}	−10		10	μA
C_I	Input terminal capacitance	V_{CC}=V_{SS}, f=1MHz, 25mV_{rms}, T_a=25℃			10	pF
$C_{I/O}$	Input/output terminal capacitance	V_{CC}=V_{SS}, f=1MHz, 25mV_{rms}, T_a=25℃			20	pF

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

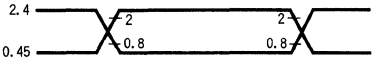
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{C(\phi)}$	Clock cycle time (Notes4, 5)			320		1350	ns
$t_{W(\phi)}$	Clock high pulse width			120		$t_{C(\phi)}$−90	ns
$t_{W(\overline{\phi})}$	Clock low pulse width			90			ns
t_r	Clock rise time					20	ns
t_f	Clock fall time					20	ns
f_{TX}	Transmitter input clock frequency	1X baud rate		DC		64	kHz
		16X baud rate		DC		310	
		64X baud rate		DC		615	
$t_{W(TPWL)}$	Transmitter input clock low pulse width	1X baud rate		12			$t_{C(\phi)}$
		16X, 64X baud rate		1			
$t_{W(TPWH)}$	Transmitter input clock high pulse width	1X baud rate		15			$t_{C(\phi)}$
		16X, 64X baud rate		3			
f_{RX}	Receiver input clock frequency	1X baud rate		DC		64	kHz
		16X baud rate		DC		310	
		64X baud rate		DC		615	
$t_{W(RPWL)}$	Receiver input clock low pulse width	1X baud rate		12			$t_{C(\phi)}$
		16X, 64X baud rate		1			
$t_{W(RPWH)}$	Receiver input clock high pulse width	1X baud rate		15			$t_{C(\phi)}$
		16X, 64X baud rate		3			
$t_{SU(A-R)}$	Address setup time before read ($\overline{CS}$, C/$\overline{D}$) (Note6)			0			ns
$t_{h(R-A)}$	Address hold time after read ($\overline{CS}$, C/$\overline{D}$) (Note6)			0			ns
$t_{W(R)}$	Read pulse width			250			ns
$t_{SU(A-W)}$	Address setup time before write			0			ns
$t_{h(W-A)}$	Address hold time after write			0			ns
$t_{W(W)}$	Write pulse width			250			ns
$t_{SU(DQ-W)}$	Data setup time before write			150			ns
$t_{h(W-DQ)}$	Data hold time after write			20			ns
$t_{SU(ESD-RxC)}$	E·SYNDET setup time before $\overline{R_XC}$			18			$t_{C(\phi)}$
$t_{SU(C-R)}$	Control setup time before read			20			$t_{C(\phi)}$
t_{RV}	Write recovery time between writes (Note7)			6			$t_{C(\phi)}$
$t_{SU(RxD-IS)}$	R_XD setup time before internal sampling pulse			2			μs
$t_{h(IS-RxD)}$	R_XD hold time after internal sampling pulse			2			μs

Note 4 : The $\overline{T_XC}$ and $\overline{R_XC}$ frequencies have the following limitations with respect to CLK.
For 1X baud rate f_{TX}, $f_{RX} \leqq 1/(30t_{C(\phi)})$. For 16X 64X baud rate f_{TX}, $f_{RX} \leqq 1/(4.5t_{C(\phi)})$
5 : Reset pulse width=$6t_{C(\phi)}$ minimum. System clock must be running during reset.
6 : $\overline{CS}$, C/$\overline{D}$ are considered as address.
7 : This recovery time is for mode initialization only. Write data is allowed only when T_XRDY=1. Recovery time between writes for asynchronous mode is $8t_{C(\phi)}$, and that for synchronous mode is $16t_{C(\phi)}$.

SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

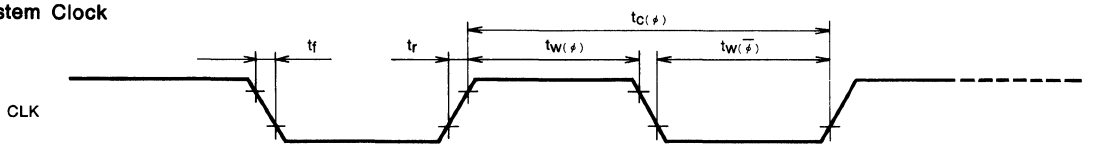
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Output data enable time after read (Note8)	C_L=150pF			200	ns
$t_{PVZ(R-DQ)}$	Output data disable time after read		10		100	ns
$t_{PZV(TxC-TxD)}$	T_XD enable time after falling edge of $\overline{T_XC}$				1	μs
$t_{PLH(CLB-TxR)}$	Propagation time from center of last bit to T_XRDY (Note9)				8	$t_{C(\phi)}$
$t_{PHL(W-TxR)}$	Propagation time from write data to T_XRDY clear (Note9)				400	ns
$t_{PLH(CLB-RxR)}$	Propagation time from center of last bit to R_XRDY (Note9)				26	$t_{C(\phi)}$
$t_{PHL(R-RxR)}$	Propagation time from read data to R_XRDY clear (Note9)				400	ns
$t_{PLH(RxC-SYD)}$	Propagation time from rising edge of $\overline{R_XC}$ to internal SYNDET (Note9)				26	$t_{C(\phi)}$
$t_{PLH(CLB-TxE)}$	Propagation time from center of last bit to T_XEMPTY (Note9)				20	$t_{C(\phi)}$
$t_{PHL(W-C)}$	Propagation time from rising edge of $\overline{WR}$ to control (Note9)				8	$t_{C(\phi)}$

Note 8 : Assumes that address is vaild before falling edge of $\overline{RD}$
9 : Status-up date can have a maximum delay of 28 clock periods from the event affecting the status.
10 : Input pulse level 0.45~2.4V Reference level Input V_{IH}=2V, V_{IL}=0.8V
Input pulse rise time 20ns Output V_{OH}=2V, V_{OL}=0.8V
Input pulse fall time 20ns

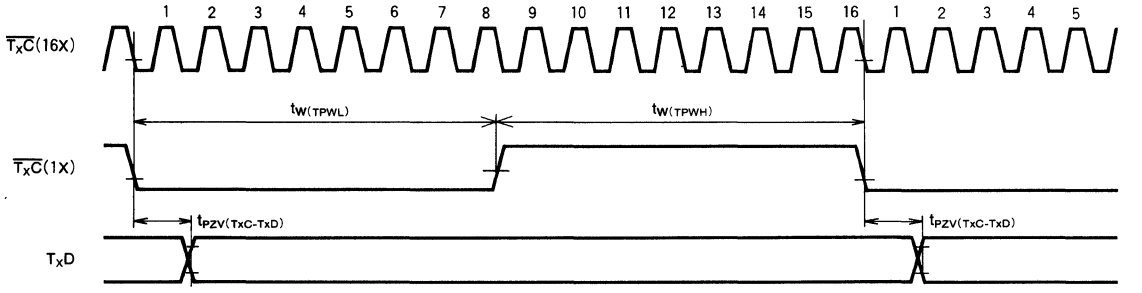


TIMING DIAGRAMS

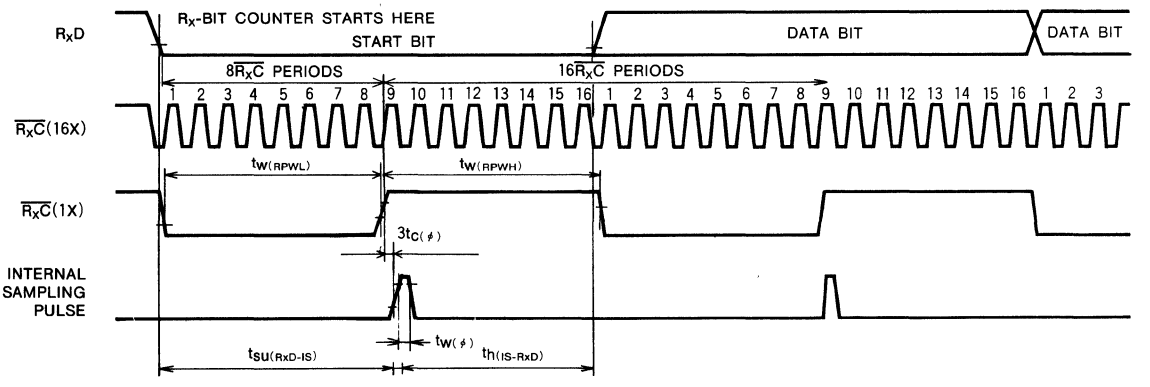
System Clock



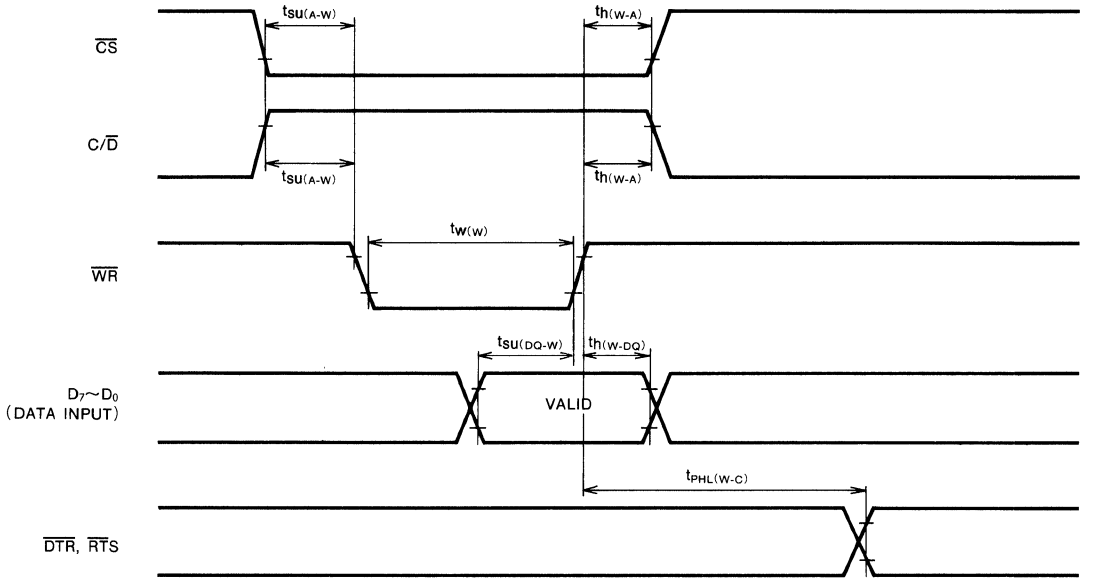
Transmitter Clock & Data



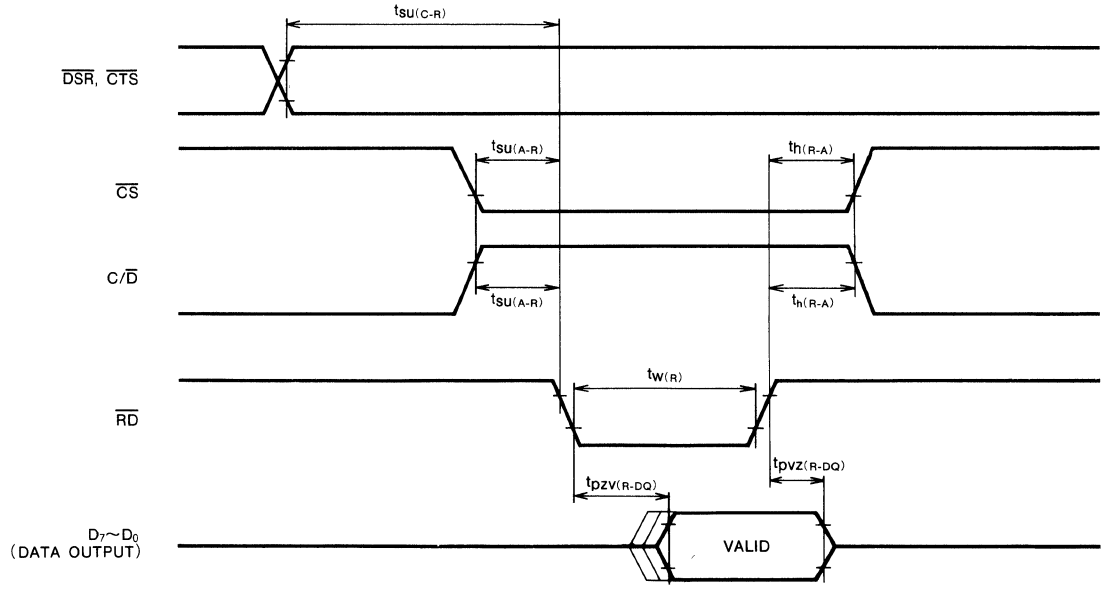
Receiver Clock & Data



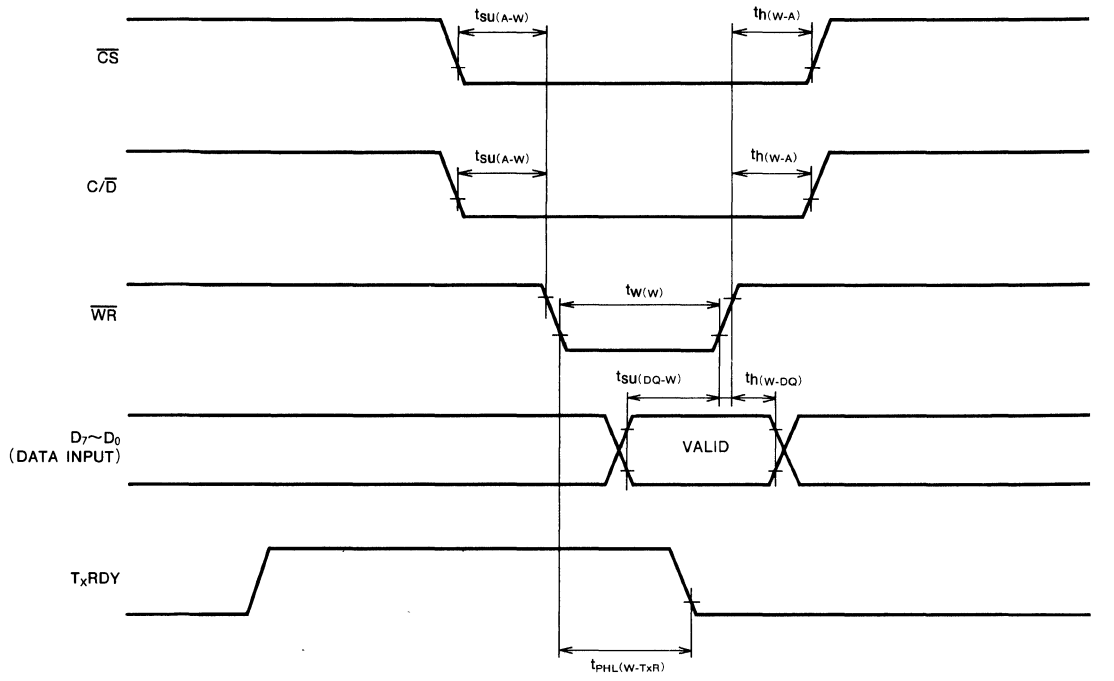
Write Control Cycle (CPU→USART)



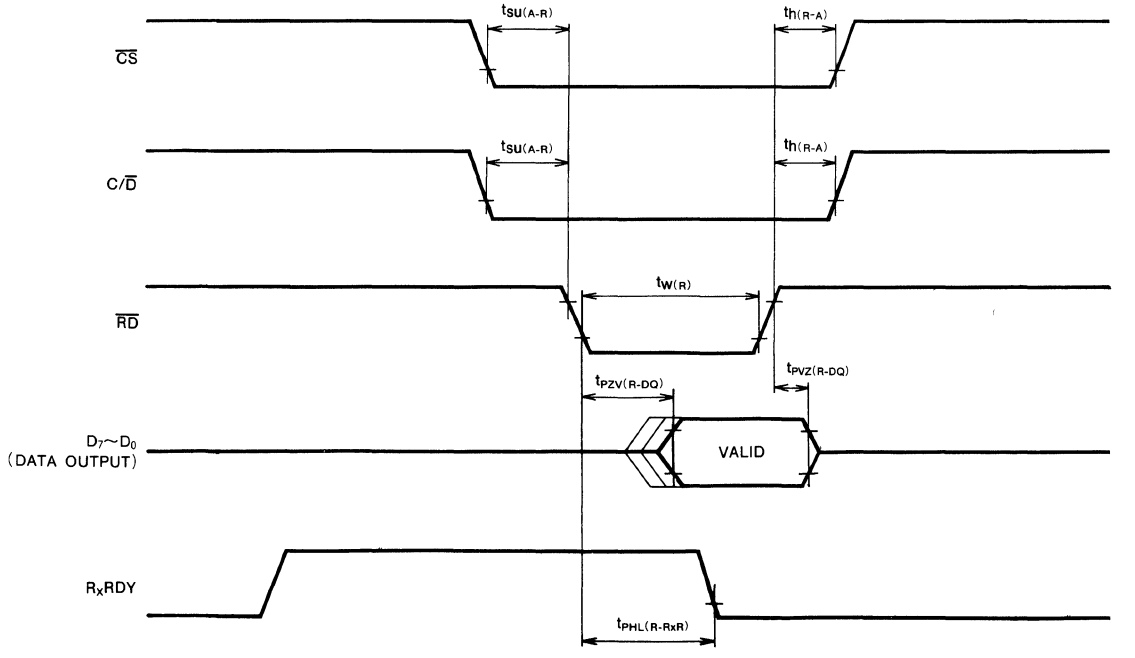
Read Control Cycle (USART→CPU)



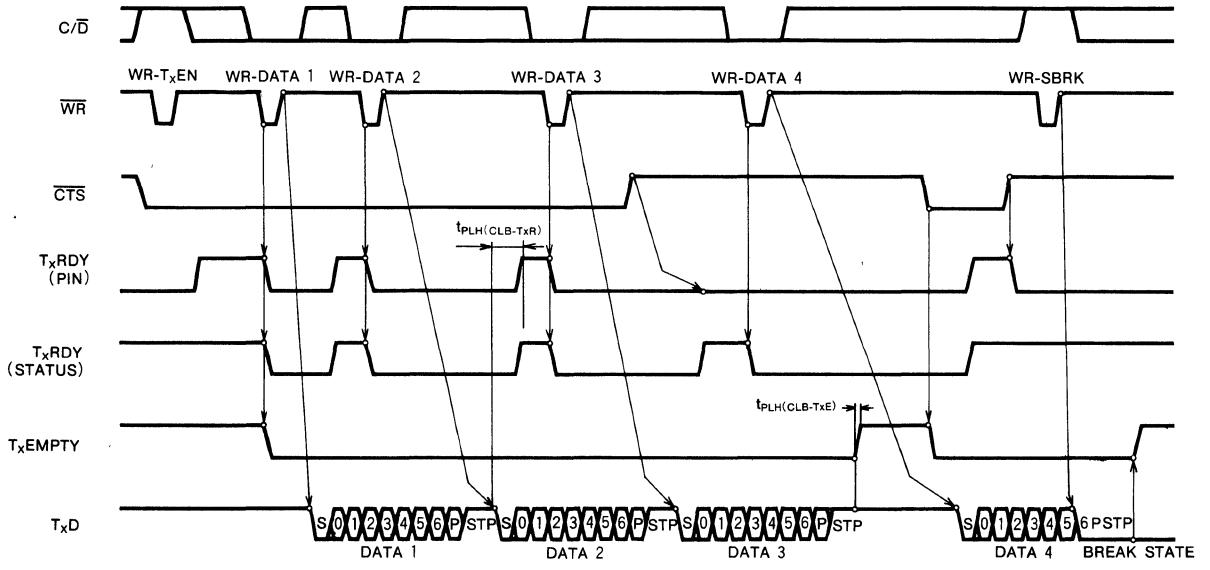
Write Data Cycle (CPU→USART)



Read Date Cycle (USART→CPU)

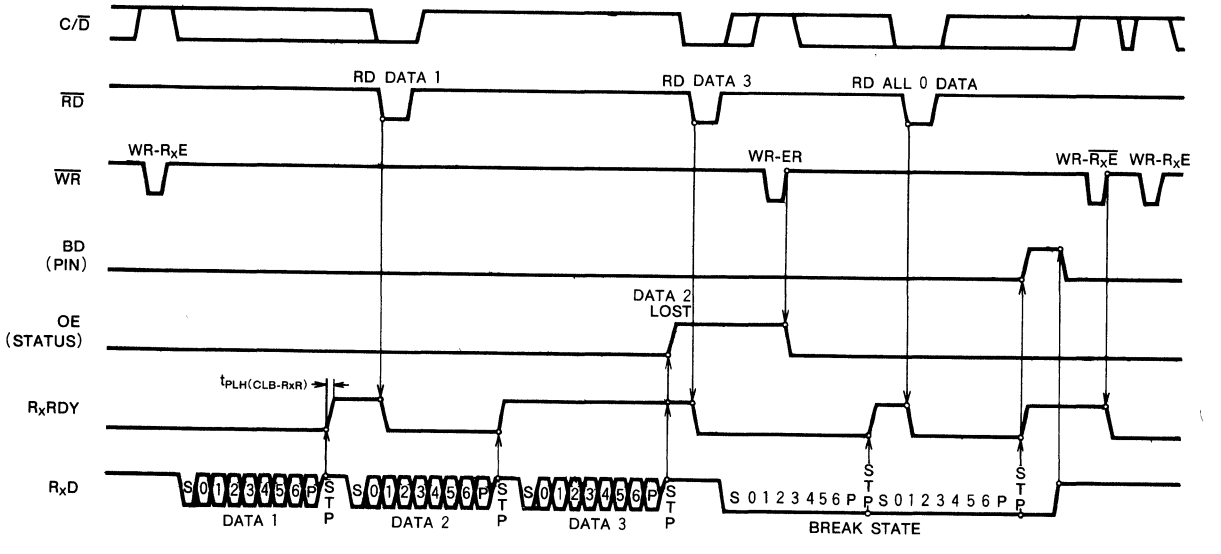


Transmitter Control & Flag Timing (Async Mode)



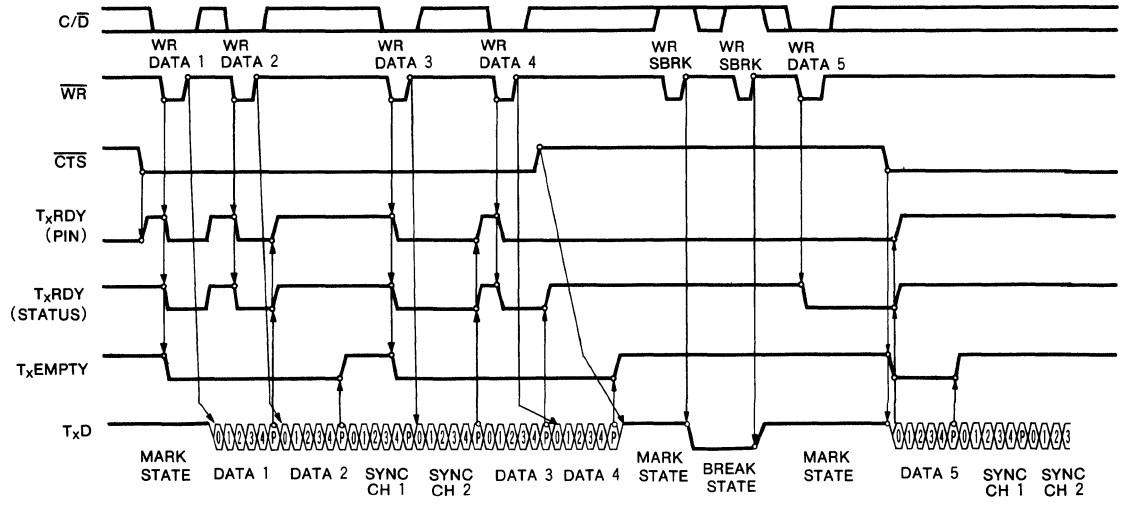
Note 11 : Example format = 7 bits/character with parity & 2 stop bits
12 : $T_xRDY(pin) = "H" \leftarrow (\text{Transmit-data buffer is empty}) \cdot (T_xEN = 1) \cdot (CTS = "L")$
13 : $T_xRDY(status) = 1 \leftarrow (\text{Transmit-data buffer is empty})$

Receiver Control & Flag Timing (Async Mode)



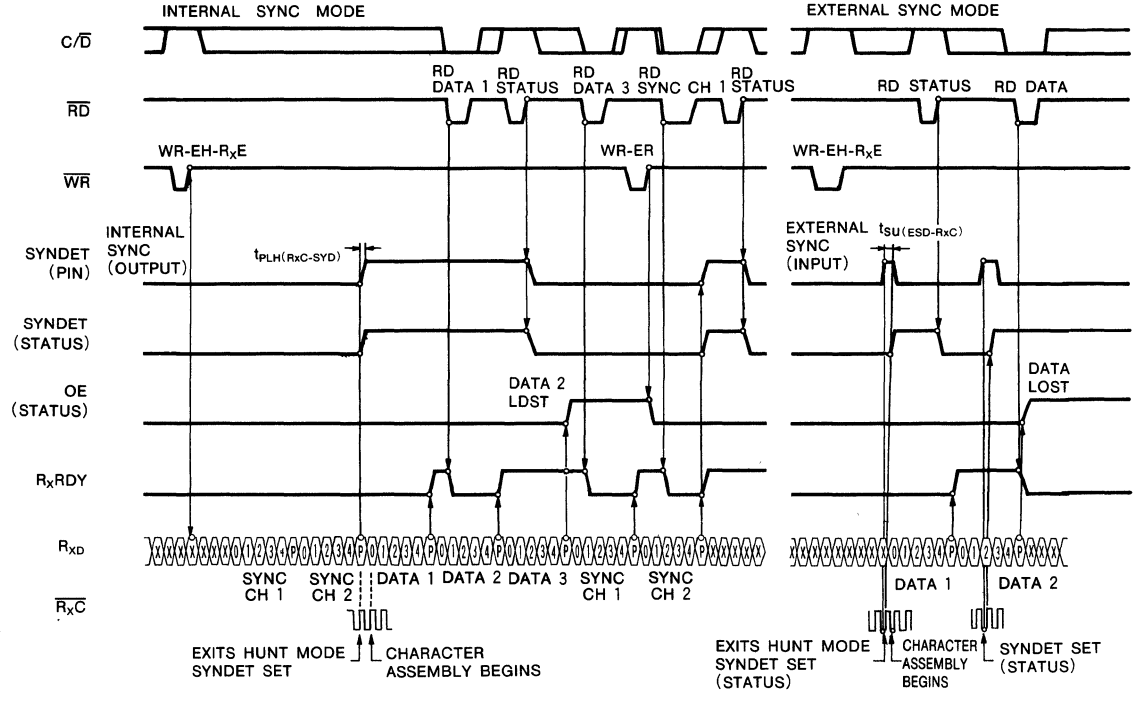
Note 14 : Example format = 7 bits/character with parity & 2 stop bits

Transmitter Control & Flag Timing (Sync Mode)



Note 15 : Example format = 5 bits/character with parity, bi-sync characters.

Receiver Control & Flag Timing (Sync Mode)



Note 16 : Example format = 5 bits/character with parity, bi-sync characters.

M5L8253P-5

PROGRAMMABLE INTERVAL TIMER

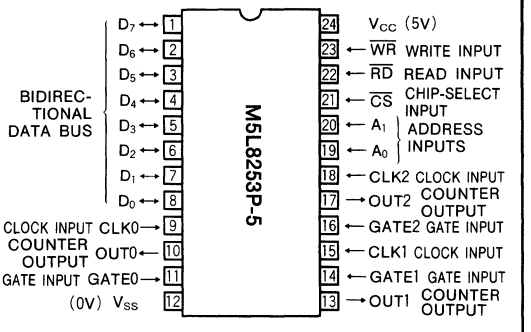
DESCRIPTION

The M5L8253P-5 is a programmable general-purpose timer device developed by using the N-channel silicon-gate ED-MOS process. It offers counter and timer functions in systems using an 8-bit parallel-processing CPU.

The use of the M5L8253P-5 frees the CPU from the execution of looped programs, count-operation programs and other simple processing involving many repetitive operations, thus contributing to improved system throughputs.

The M5L8253P-5 works on a single power supply, and both its input and output can be connected to a TTL circuit.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4

FEATURES

- Single 5V supply voltage
- TTL compatible
- Clock period: DC~2.6MHz
- 3 independent built-in 16-bit down counters
- 6 counter modes freely assignable for each counter
- Binary or decimal counts

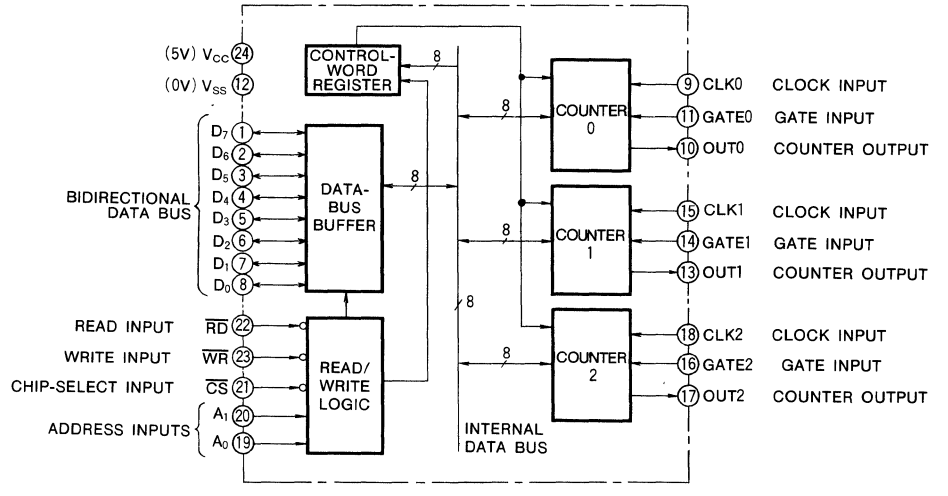
APPLICATION

Delayed-time setting, pulse counting and rate generation in microcomputers.

FUNCTION

Three independent 16-bit counters allow free programming based on mode-control instructions from the CPU. When roughly classified, there are 6 modes (0~5). Mode 0 is mainly used as an interruption timer and event counter, mode 1 as a digital one-shot, modes 2 and 3 as a rate generator, mode 4 for a software triggered strobe, and mode 5 for a hardware triggered strobe. The count can be monitored and set at any time. The counter operates with either the binary or BCD system.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

DESCRIPTION OF FUNCTIONS

Data-Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the M5L8253P-5 to the system-side data bus. Transmission and reception of all the data including control words for mode designation and values written in, and read from, the counters are carried out through this buffer.

Read/Write Logic

The read/write logic accepts control signals ($\overline{RD}$, $\overline{WR}$) from the system and generates control signals for each counter. It is enabled or disabled by the chip-select signal ($\overline{CS}$); if $\overline{CS}$ is at the high-level the data-bus buffer enters a floating (high-impedance) state.

Read Input ($\overline{RD}$)

The count of the counter designated by address inputs A_0 and A_1 on the low-level is output to the data bus.

Write Input ($\overline{WR}$)

Data on the data bus is written in the counter or control-word register designated by address inputs A_0 and A_1 on the low-level.

Address Inputs (A_0, A_1)

These are used for selecting one of the 3 internal counters and either of the control-word registers.

Chip-Select Input ($\overline{CS}$)

A low-level on this input enables the M5L8253P-5. Changes in the level of the $\overline{CS}$ input have no effect on the operation of the counters.

Control-Word Register

This register stores information required to give instructions about operational modes and to select binary or BCD counting. Unlike the counters, it allows no reading, only writing.

Counters 0,1 and 2

These counters are identical in operation and independent of each other. Each is a 16-bit, presettable, down counter, and has clock-input, gate-input and output pins. The counter can operate in either binary or BCD using the falling edge of each clock. The mode of counter operation and the initial value from which to start counting can be designated by software. The count can be read by input instruction at any time, and there is a "read-on-the-fly" function which enables stable reading by latching each instantaneous count to the registers by a special counter-latch instruction.

CONTROL WORD AND INITIAL-VALUE LOADING

The function of the M5L8253P-5 depends on the system software. The operational mode of the counters can be specified by writing control words (A_0, A_1=1, 1) into the control-word registers.

The programmer must write out to the M5L8253P-5 the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

Fig. 1 shows control-word format, which consists of 4 fields. Only the counter selected by the D_7 and D_6 bits of the control word is set for operation. Bits D_5 and D_4 are used for specifying operations to read values in the counter and to initialize. Bits $D_3 \sim D_1$ are used for mode designation, and D_0 for specifying binary or BCD counting. When D_0=0, binary counting is employed, and any number from 0000_{16} to $FFFF_{16}$ can be loaded into the count register. The counter is counted down for each clock. The counting of 0000_{16} causes the transmission of a time-out signal from the count-output pin.

The maximum number of counts is obtained when 0000_{16} is set as the initial value. When D_0=1, BCD counting is employed, and any number from 0000_{10} to 9999_{10} can be loaded on the counter.

Neither system resetting nor connecting to the power supply sets the control word to any specific value. Thus to bring the counters into operation, the above-mentioned control words for mode designation must be given to each counter, and then 1~2 byte initial counter values must be set. The following is an example of this programming step.

To designate mode 0 for counter 1 ,with initial value 8253_{16} set by binary count, the following program is used:

MVI	**A, 70_{16}**	Control word 70_{16}
OUT	**n_1**	n_1 is control-word-register address
MVI	**A, 53_{16}**	Low-order 8 bits
OUT	**n_2**	n_2 is counter 1 address
MVI	**A, 82_{16}**	High-order 8 bits
OUT	**n_2**	n_2 is counter 1 address

Thus, the program generally has the following sequence·

(1) Control-word output to counter i (i=0, 1, 2).
(2) Initialization of low-order 8 counter bits
(3) Initialization of high-order 8 counter bits

The three counters can be executed in any sequence It is possible, for instance, to designate the mode of each counter and then load initial values in a different order. Initialization of the counters designated by RL 1 and RL 0 must be executed in the order of the low-order 8 bits and then the high-order 8 bits for the counter in question.

Table 1 Basic Functions

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	Function
L	H	L	0	0	Data bus→Counter 0
L	H	L	0	1	Data bus→Counter 1
L	H	L	1	0	Data bus→Counter 2
L	H	L	1	1	Data bus→Control-word register
L	L	H	0	0	Data bus←Counter 0
L	L	H	0	1	Data bus←Counter 1
L	L	H	1	0	Data bus←Counter 2
L	L	H	1	1	3-state
H	×	×	×	×	3-state
L	H	H	×	×	3-state

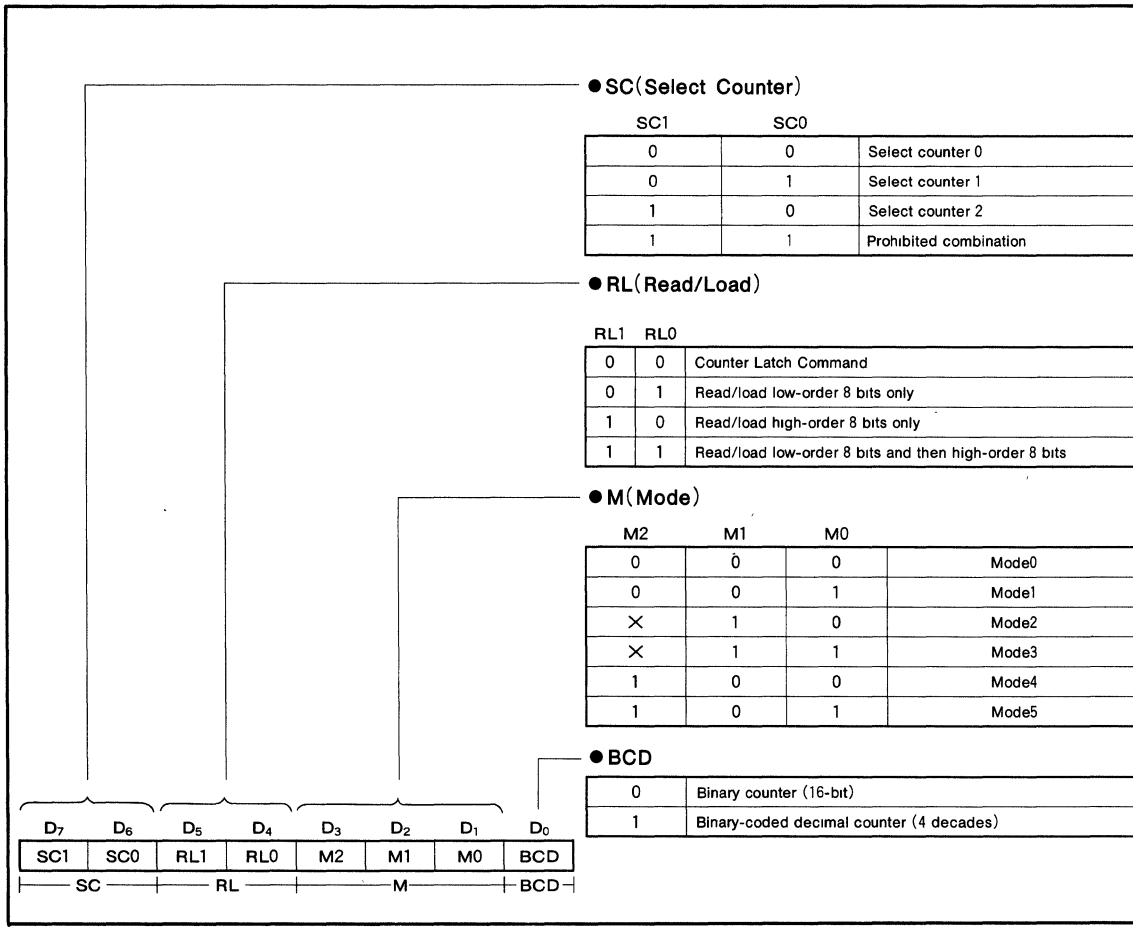


Fig. 1 Control-Word Format

MODE DEFINITION

Mode 0 (Interrupt on Terminal Count)

Mode set and initialization cause the counter output to go low-level (see Fig. 2). When the counter is loaded with an initial value, it will start counting the clock input. When the terminal count is reached, the output will go high-level and remain high-level until the selected count register is reloaded with the mode. This mode can be used when the CPU is to be interrupted after a certain period or at the time of counting up.

Fig. 2 shows a setting of 4 as the initial value. If gate input goes low-level, counting is inhibited for the duration of the low-level period.

Reloading of the initial value during count operation will stop counting by the loading of the first byte and start the new count by the loading of the second byte.

Mode 1 (Programmable One-Shot)

The gate input functions as a trigger input. A gate-input rising edge causes the generation of low-level one-shot output with a predetermined clock length starting from the next clock. Fig. 3 shows an initial setting of 4. While the counter output is at the low-level (during one-shot), loading of a new value does not change the one-shot pulse width, which has already been output. The current count can be read at any time without affecting the width of the one-shot pulse being output. This mode permits retriggering.

Mode 2 (Rate Generator)

Low-level pulses during one clock operation are generated from the counter output at a rate of one per n clock inputs (where n is the value initially set for the counter). When a new value is loaded during the counter operation, it is reflected on the output after the pulses by the current count have been output. In the example shown in Fig. 4, n is given as 4 at the outset and is then changed to 3.

In this mode, the gate input provides a reset function. While it is on the low-level, the output is maintained high-level; the counter restarts from the initial value, triggered by a rising gate-input edge. This gate input, therefore, makes possible external synchronization of the counter by hardware.

After the mode is set, the counter does not start counting until the rate n is loaded into the count register, with the counter output remaining at the high-level.

Mode 3 (Square Rate Generator)

This is similar to Mode 2 except that it outputs a square wave with the half count of the set rate. When the set value n is odd, the square-wave output will be high for $(n+1)/2$ clock-input counts and low-level for $(n-1)/2$ counts. When a new rate is reloaded into the count register during its operation, it is immediately reflected on the count directly following the output transition (high-to-low or low-to-high) of the current count. Gate-input operations are exactly the same as in Mode 2. Fig. 5 shows an example of Mode 3 operation.

Mode 4 (Software Triggered Strobe)

After the mode is set, the output will be high-level. By loading a number on the counter, however, clock-input counts can be started and on the terminal count, the output will go low for one input-clock period and then will go high again. Mode 4 differs from Mode 2 in that pulses are not output repeatedly with the same set count. The pulse output is delayed one clock period in Mode 2, as shown in Fig. 6. When a new value is loaded into the count register during its count operation, it is reflected on the next pulse output without affecting the current count. The count will be inhibited while the gate input is low-level.

Mode 5 (Hardware Triggered Strobe)

This is a variation of Mode 1. The gate input provides a trigger function, and the count is started by its rising edge. On the terminal count, the counter output goes low for on one clock period and then goes high-level. As in Mode 1, retriggering by the gate input is possible. An example of timing in Mode 5 is shown in Fig. 7.

As mentioned above, the gate input plays different roles according to the mode. The functions are summarized in Table 2.

Table 2 Gate Operations

Mode \ Gate	Low-level or going low-level	Rising	High-level
0	Disables counting		Enables counting
1		(1) Initiates counting (2) Resets output after next clock	
2	(1) Disables counting (2) Sets output high immediately	(1) Reloads counter (2) Initiates counting	Enables counting
3	(1) Disables counting (2) Sets output high immediately	(1) Reloads counter (2) Initiates counting	Enables counting
4	Disables counting		Enables counting
5		Initiates counting	

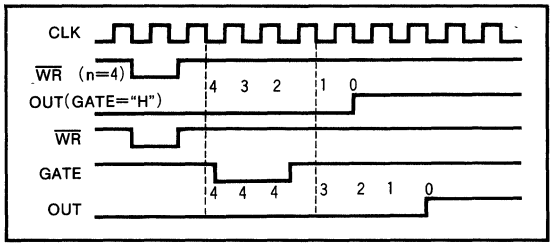


Fig. 2 Mode 0

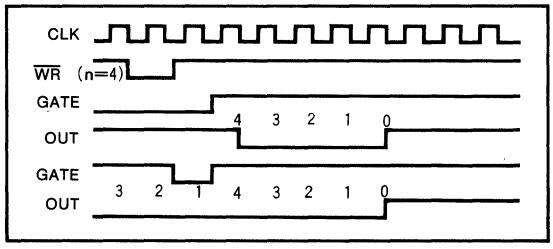


Fig. 3 Mode 1

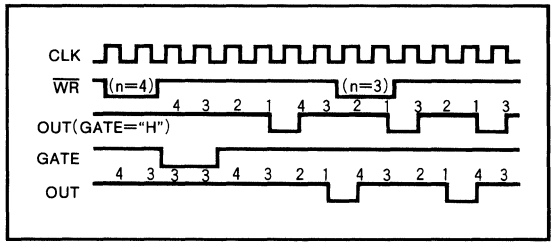


Fig. 4 Mode 2

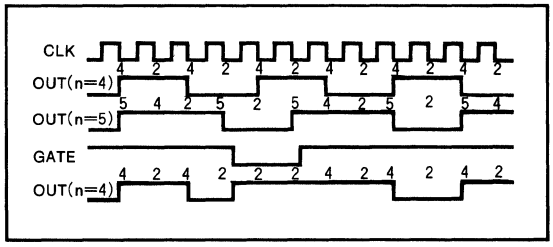


Fig. 5 Mode 3

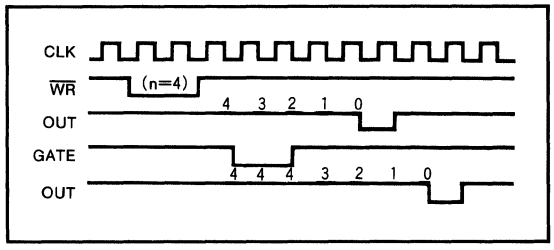


Fig. 6 Mode 4

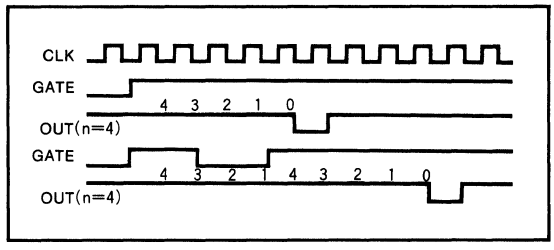


Fig. 7 Mode 5

COUNTER MONITORING

Sometimes the counter must be monitored by reading its count or using it as an event counter. The M5L8253P-5 offers the following two methods for count reading:

Read Operation

The count can be read by designating the address of the counter to be monitored and executing a simple I/O read operation. In order to ensure correct reading of the count, it is necessary to cause the clock input to pause by external logic or prevent a change in the count by gate input. An example of a program to read the counter 1 count is shown below. If RL1, RL0=1, 1 has been specified in the control word, the first IN instruction enables the low-order 8 bits to be read and the second IN instruction enables the high-order 8 bits.

```
IN    n2 ···· n2 is the counter 1 address
MOV   D, A
IN    n2
MOV   E, A
```

The IN instruction should be executed once or twice by the RL1 and RL0 designations in the control-word register.

Read-on-the-Fly Operation

This method makes it possible to read the current count without affecting the count operation at all. A special counter-latch command is first written in the control-word register. This causes latching of all the instantaneous counts to the register, allowing retention of stable counts. An example of a program to execute this operation for counter 2 is given below.

```
MVI   A, 1000XXXX ···· D5 = D4 = 0 designates counter
                        latching
OUT   n1 ···· n1 is the control-word-register address
IN    n3 ···· n3 is the counter 2 address
MOV   D, A
IN    n3
MOV   E, A
```

In this example, the IN instruction is executed twice. Due to the internal logic of the M5L8253P-5 it is absolutely essential to complete the entire reading procedure. If 2 bytes are programmed to be read, then two bytes must be read before any OUT instruction can be executed to the same counter.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power supply voltage	With respect to V_{SS}	−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
Pd	Maximum power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating free-air temperature range		−20～75	℃
T_{stg}	Storage temperature range		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Power supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20～75℃, V_{CC}=5 V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL}=2.2mA			0.45	V
I_{IH}	High-level input current	V_I=V_{CC}			±10	μA
I_{IL}	Low-level input current	V_I=0V			±10	μA
I_{OZ}	Off-state output current	V_O=0V～V_{CC}			±10	μA
I_{CC}	Supply current from V_{CC}	V_{SS}=0V			140	mA
C_I	Input terminal capacitance	V_{IL}=V_{SS}, f=1MHz, 25mVrms, T_a=25℃			10	pF
$C_{I/O}$	Input/output terminal capacitance	$V_{I/OL}$=V_{SS}, f=1MHz,25mVrms, T_a=25℃			20	pF

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}= 5 V±10%, V_{SS}= 0 V, unless otherwise noted)

Read cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(R)}$	Read pulse width		300			ns
$t_{SU(A-R)}$	Address setup time before read		30			ns
$t_{h(R-A)}$	Address hold time after read		5			ns
$t_{rec(R)}$	Read recovery time		1000			ns

Write cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(W)}$	Write pulse width		300			ns
$t_{su(A-W)}$	Address setup time before write		30			ns
$t_{h(W-A)}$	Address hold time after write		30			ns
$t_{su(DQ-W)}$	Data setup time before write		250			ns
$t_{h(W-DQ)}$	Data hold time after write		30			ns
$t_{rec(W)}$	Write recovery time		1000			ns

Clock and gate timing

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\phi H)}$	Clock high pulse width		230			ns
$t_{W(\phi L)}$	Clock low pulse width		150			ns
$t_{C(\phi)}$	Clock cycle time		380		DC	ns
$t_{W(GH)}$	Gate high pulse width		150			sn
$t_{W(GL)}$	Gate low pulse width		100			ns
$t_{su(G-\phi)}$	Gate setup time before clock		100			ns
$t_{h(\phi-G)}$	Gate hold time after clock		50			ns

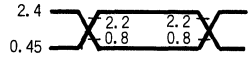
SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}= 5 V±10%, V_{SS}= 0 V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Propagation time from read to output	C_L=150pF			200	ns
$t_{PVZ(R-DQ)}$	Propagation time from read to output floating (Note 2)		25		100	ns
$t_{PXV(G-OUT)}$	Propagation time from gate to output				300	ns
$t_{PXV(\phi-OUT)}$	Propagation time from clock to output				400	ns

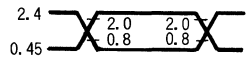
Note 1 : A C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	20ns
Input pulse fall time	20ns
Reference level input	V_{IH}=2.2V, V_{IL}=0.8V
output	V_{OH}=2.0V, V_{OL}=0.8V

2 : Test condition is not applied



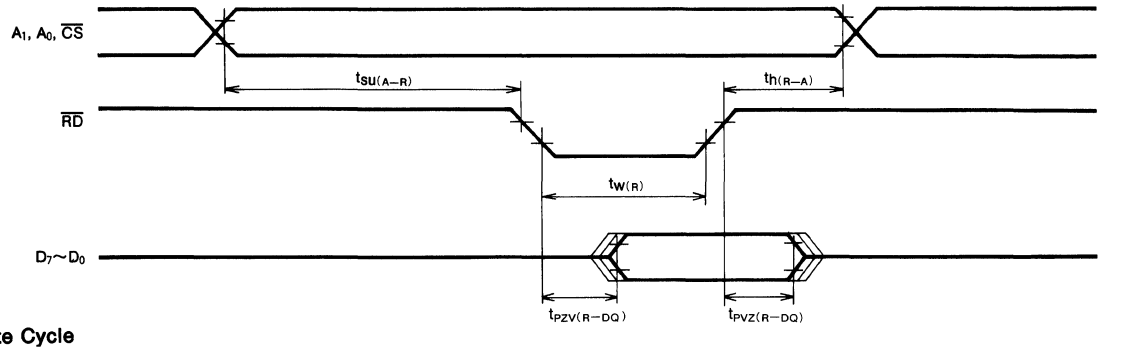
Input



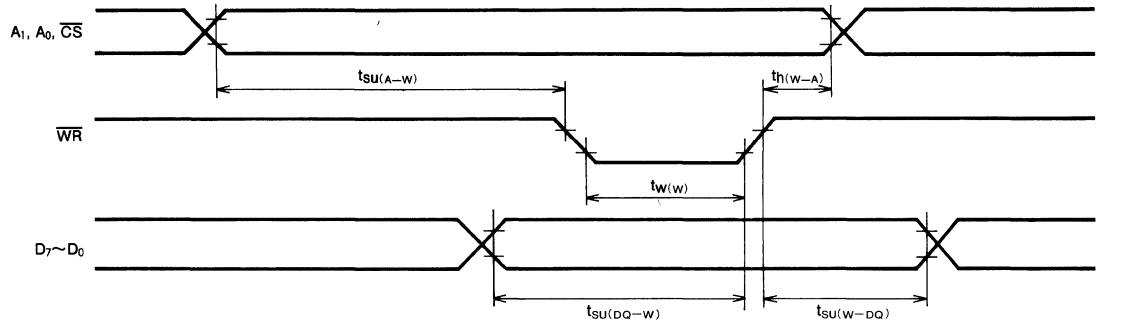
Output

TIMING DIAGRAMS

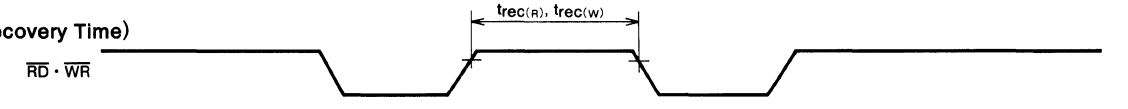
Read Cycle



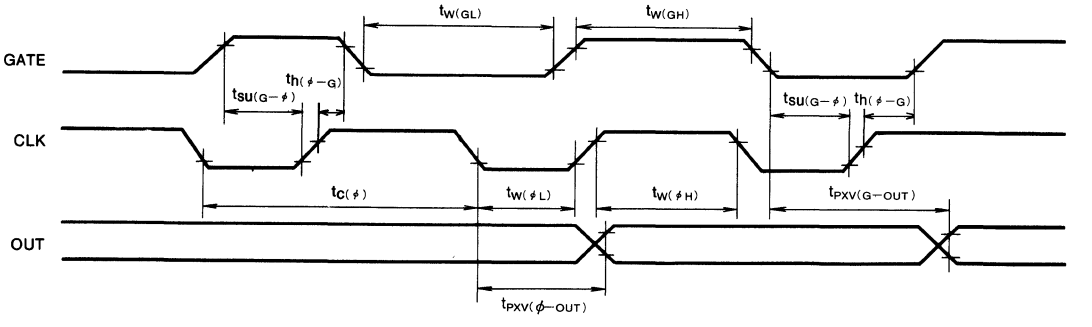
Write Cycle



(Recovery Time)



Clock and Gate Cycle



M5L8255AP-5

PROGRAMMABLE PERIPHERAL INTERFACE

DESCRIPTION

The M5L8255AP-5 is a family of general-purpose programmable input/ output devices designed for use with an 8-bit/16-bit parallel CPU as input/output ports. Device is fabricated using N-channel silicon-gate ED-MOS technology for a single supply voltage. They are simple input and output interfaces for TTL circuits, having 24 input/output pins which correspond to three 8-bit input/output ports.

FEATURES

- Single 5V supply voltage
- TTL compatible
- Darlington drive capability
- 24 programmable I/O pins
- Direct bit set/reset capability

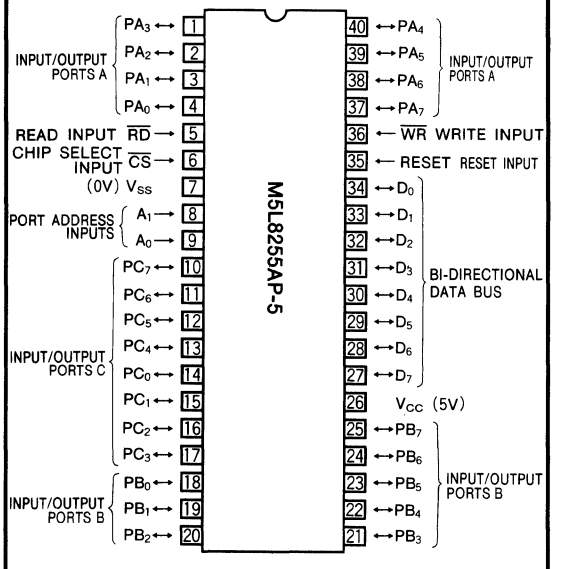
APPLICATION

Input/output ports for microprocessor

FUNCTION

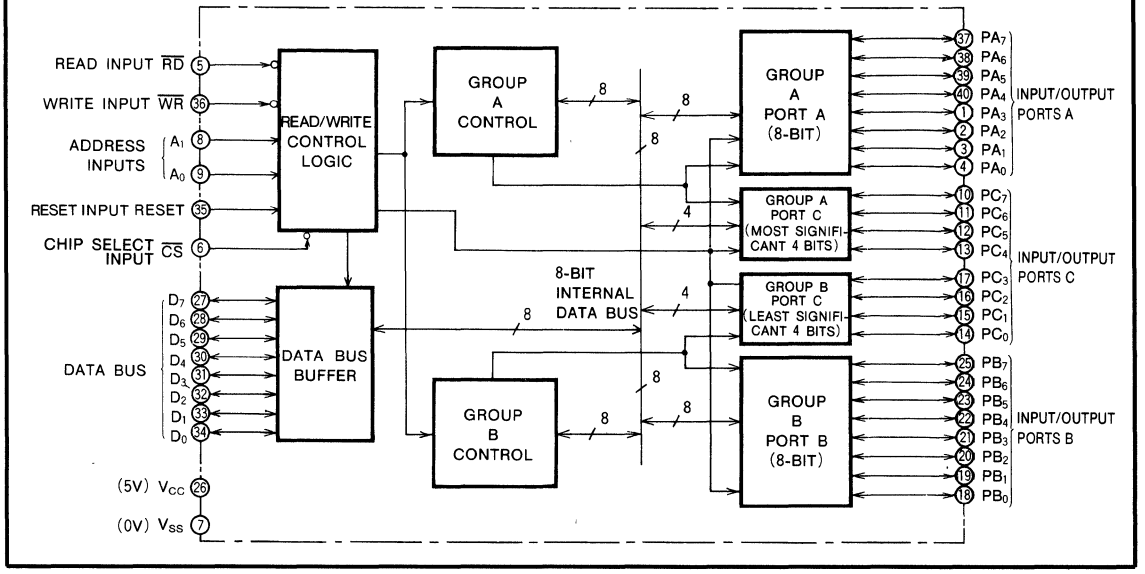
These PPIs have 24 input/output pins which may be individually programmed in two 12-bit groups A and B with mode control commands from a CPU. They are used in three major modes of operation, mode 0, mode 1 and mode 2. Operating in mode 0 , each group of 12 pins may be programmed in sets of 4 to be inputs or outputs. In mode 1, the 24 I/O terminals may be programmed in two 12-bit groups, group A and group B. Each group contains one 8-bit data port, which may be programmed to serve as input or output, and one 4-bit control port used for handshaking and interrupt control signals. Mode 2 is used with group A only, as one 8-bit bidirectional bus port and one 5-bit control port. Bit set/reset is controlled by CPU. A high-level reset input (RESET) clears the control register, and all ports are set to the input mode (high-impedance state).

PIN CONFIGURATION (TOP VIEW)



Outline 40P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONAL DESCRIPTION

$\overline{RD}$ (Read) Input

At low-level, the status or the data at the port is transferred to the CPU from the PPI. In essence, it allows the CPU to read data from the PPI.

$\overline{WR}$ (Write) Input

At low-level, the data or control words are transferred from the CPU and written in the PPI.

A_0, A_1 (Port address) Input

These input signals are used to select one of the three ports: port A, port B, and port C, or the control register. They are normally connected to the least significant 2 bits of the address bus.

RESET (Reset) Input

At high-level, the control register is cleared. Then all ports are set to the input mode (high-impedance state).

$\overline{CS}$ (Chip-Select) Input

At low-level, the communication between the PPI and the CPU is enabled. While at high-level, the data bus is kept in the high-impedance state, so that commands from the CPU are ignored. Then the previous data is kept at the output port.

Read/Write Control Logic

The function of this block is to control transfers of both data and control words. It accepts the address signals (A_0, A_1, $\overline{CS}$), I/O control signals ($\overline{RD}$, $\overline{WR}$) and RESET signal, and then issues commands to both of the control groups in the PPI.

Data Bus Buffer

This three-state, bidirectional, 8-bit buffer is used to transfer the data when an input or output instruction is executed by the CPU. Control words and status information are also transferred through the data bus buffer.

Group A and Group B Control

Accepting commands from the read/write control logic, the control blocks (Group A, Group B) receive 8-bit control words from the internal data bus and issue the proper commands for the associated ports. Control group A is associated with port A and the 4 high-order bits of port C. Control group B is associated with port B and the 4 low-order bits of port C. The control register, which stores control words, can only be written into.

Port A, Port B and Port C

The PPI contains three 8-bit ports whose modes and input/output settings are programmed by the system software.

Port A has an output latch/buffer and an input latch/buffer. Port B has an input-output latch/buffer. Port C has an output latch/buffer and an input buffer. Port C can be divided into two 4-bit ports which can be used as ports for control signals for port A and port B.

The basic operations are shown in Table 1.

Table 1 Basic Operations

A_1	A_0	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	Operation
0	0	L	L	H	Data bus ← Port A
0	1	L	L	H	Data bus ← Port B
1	0	L	L	H	Data bus ← Port C
0	0	L	H	L	Port A ← Data bus
0	1	L	H	L	Port B ← Data bus
1	0	L	H	L	Port C ← Data bus
1	1	L	H	L	Control register ← Data bus
X	X	H	X	X	Data bus is in high-impedance state
1	1	L	L	H	Illegal condition

Bit Set/Reset

When port C is used as an output port, any 1 bit of the 8 bits can be set (high) or reset (low) by a control word from the CPU. This bit set/reset can be operated in the same way as the mode set, but the control word format is different. This operation is also used for INTE (interrupt enable flag) set/reset in mode 1 and mode 2.

different. This operation is also used for INTE set/reset in mode 1 and mode 2.

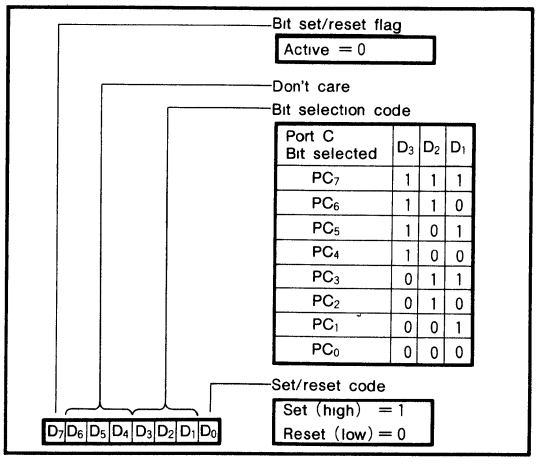


Fig. 1 Control word format for port C set/reset

BASIC OPERATING MODES

The PPI can operate in any one of three selected basic modes.

Mode 0: Basic input/output (group A, group B)
Mode 1: Strobed input/output (group A, group B)
Mode 2: Bidirectional bus (group A only)

The mode of both group A and group B can be selected independently. The control word format for mode set is shown in Fig. 2.

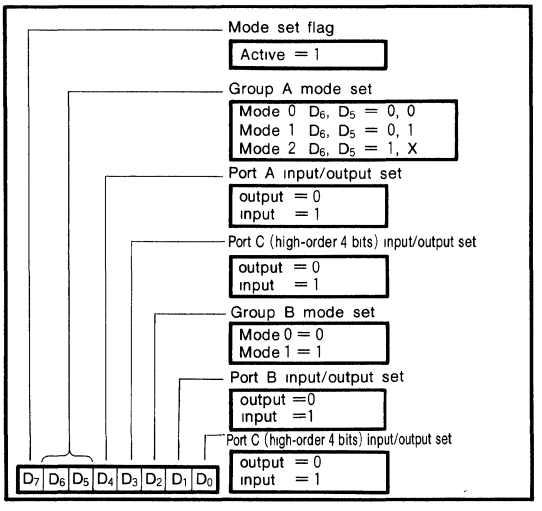
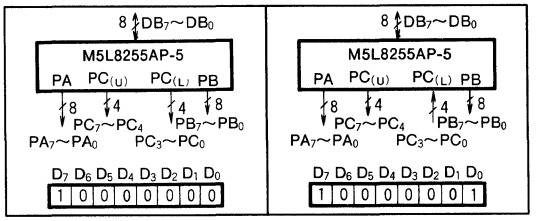
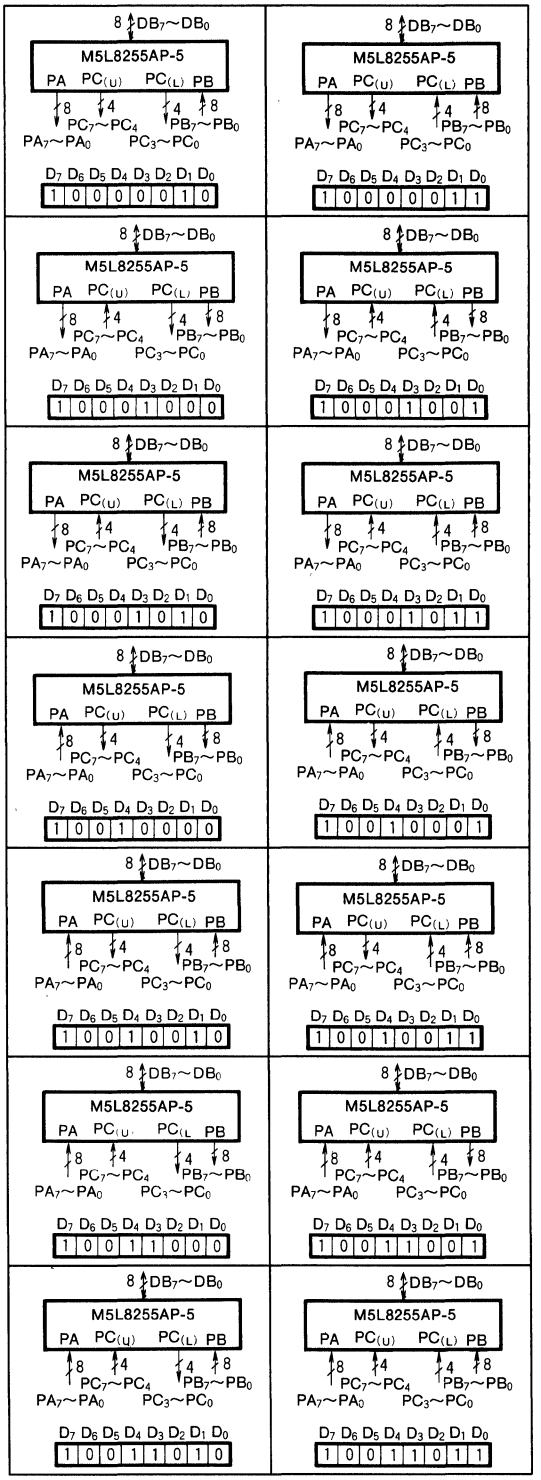


Fig. 2 Control word format for mode set.

1. Mode 0 (Basic Input/Output)

This functional configuration provides simple input and output operations for each of the 3 ports. No "handshaking" is required; data is simply written in, or read from, the specified port. Output data from the CPU to the port can be held, but input data from the port to the CPU cannot be held. Any one of the 8-bit ports and 4-bit ports can be used as an input port or an output port. The diagrams following show the basic input/output operating modes.





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2. Mode 1 (Strobed Input/Output)

This function can be set in both group A and B. Both groups are composed of one 8-bit data port and one 4-bit control data port. The 8-bit port can be used as an input port or an output port. The 4-bit port is used for control and status signals affecting the 8-bit data port. The following shows operations in mode 1 for using input ports.

$\overline{STB}$ (Strobe Input)

A low-level on this input latches the output data from the terminal units into the input register of the port. In short, this is a clock for data latching. The data from the terminal units can be latched by the PPI independent of the control signal from the CPU. This data is not sent to the data bus until the instruction IN is executed.

IBF (Input Buffer Full Flag Output)

A high-level on this output indicates that the data from the terminal units has been latched into the input register. IBF is set to high-level by the falling edge of the $\overline{STB}$ input, and is reset to low-level by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request Output)

This can be used to interrupt the CPU when an input device is requesting service. When INTE (interrupt enable flag) of the PPI is high-level, INTR is set to high-level by the rising edge of the $\overline{STB}$ input and is reset to low-level by the falling edge of $\overline{RD}$ input.

$INTE_A$ of group A is controlled by bit setting of PC_4. $INTE_B$ of group B is controlled by bit setting of PC_2.

Mode 1 input state is shown in Fig. 3, and the timing diagram is shown in Fig. 4.

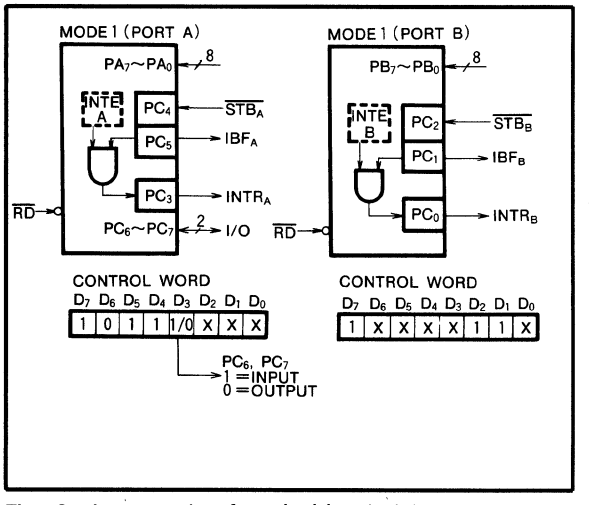


Fig. 3 An example of mode 1 input state

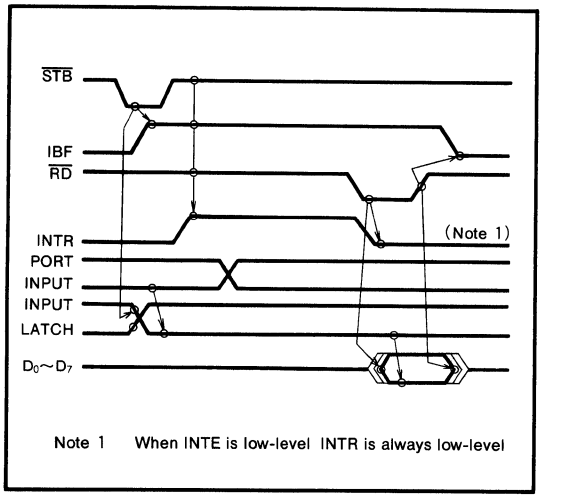


Fig. 4 Timing diagram

The following shows operations using mode 1 for output ports.

$\overline{OBF}$ (Output Buffer Full Flag Output)

This is reset to low-level by the rising edge of the $\overline{WR}$ signal and is set to high-level by the falling edge of the $\overline{ACK}$ (acknowledge input). In essence, the PPI indicates to the terminal units by the $\overline{OBF}$ signal that the CPU has sent data to the port.

$\overline{ACK}$ (Acknowledge Input)

Receiving this signal from a terminal unit can indicate to the PPI that the terminal unit has accepted data from a port.

INTR (Interrupt Request)

When a peripheral unit is accepting data from the CPU, seting INTR to high-level can be used to interrupt the CPU. When INTE (interrupt enable flag) is high-level and $\overline{OBF}$ is set to high-level by the rising edge of an $\overline{ACK}$ signal, then INTR will also be set to high-level by the rising edge of the $\overline{ACK}$ signal. Also, INTR is reset to low-level by the falling edge of the $\overline{WR}$ signal when the PPI has been receiving data from the CPU.

$INTE_A$ of group A is controlled by bit setting of PC_6. $INTE_B$ of group B is controlled by bit setting of PC_2.

Mode 1 output state is shown in Fig. 5, and the timing diagram is shown in Fig. 6.

Combinations for using port A and port B as input or output in mode 1 are shown in Fig. 7 and Fig. 8.

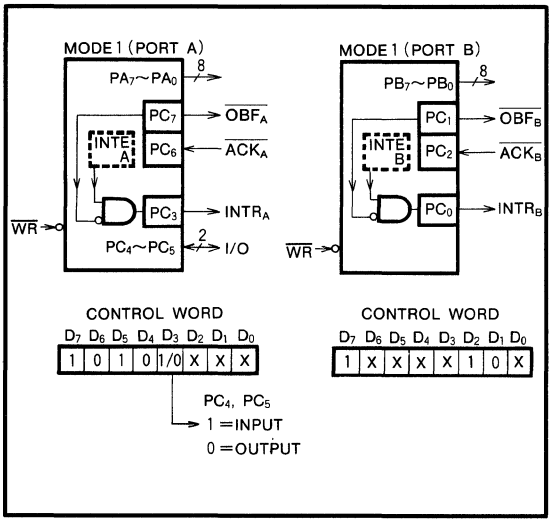


Fig. 5 An example of mode 1 output state

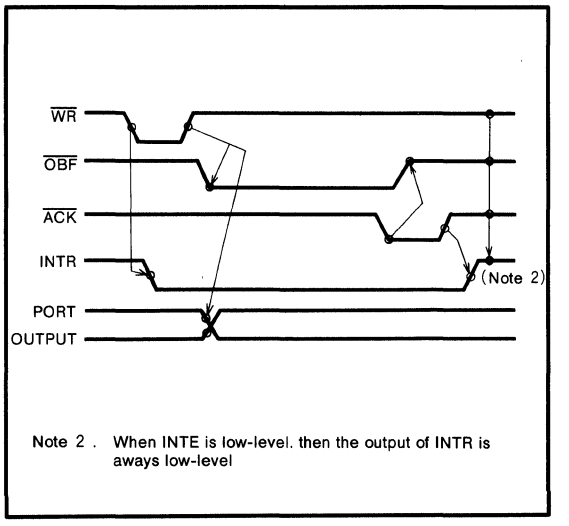


Fig. 6 Timing diagram

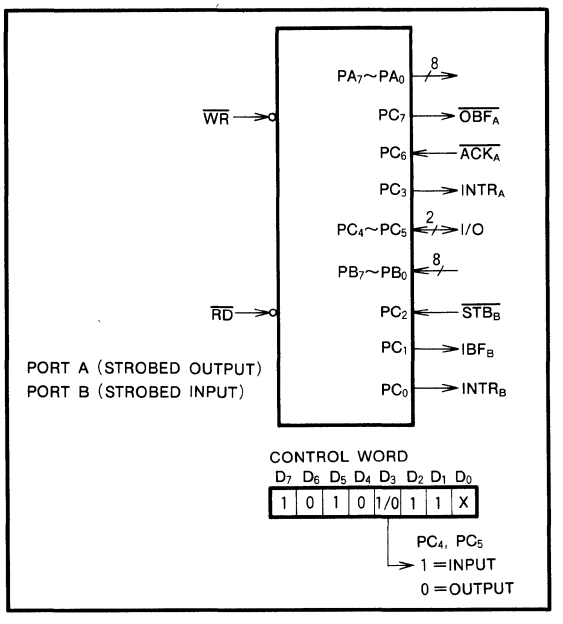


Fig. 7 Mode 1 port A and port B I/O example

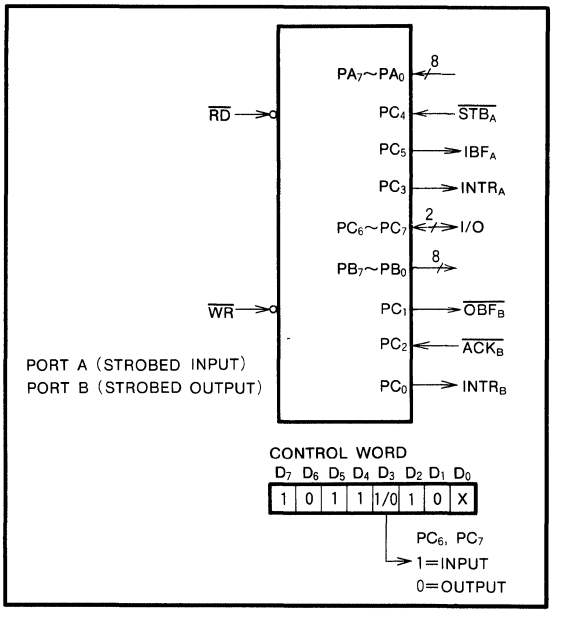


Fig. 8 Mode 1 port A and port B I/O example

3. Mode 2 (Strobed Bidirectional Bus Input/ Output)

Mode 2 can provide bidirectional operations, using one 8-bit bus for communicating with terminal units. Mode 2 is only valid with group A and uses one 8-bit bidirectional bus port (port A) and a 5-bit control port (high-order 5 bits of port C). The bus port (port A) has two internal registers, one for input and the other for output. On the other hand, the control port (port C) is used for communicating control signals and bus-status signals. These control signals are similar to mode 1 and can also be used to control interruption of the CPU. When group A is programmed as mode 2, group B can be programmed independently as mode 0 or mode 1. When group A is in mode 2, the following 5 control signals can be used.

$\overline{OBF}$ (Output Buffer Full Flag Output)

The $\overline{OBF}$ output will go low-level to indicate that the CPU has sent data to the internal register of port A. This signal lets the terminal units know that the data is ready for transfer from the CPU. When this occurs, port A remains in the floating (high-impedance) state.

$\overline{ACK}$ (Acknowledge Input)

A low-level $\overline{ACK}$ input will cause the data of the internal register to be transferred to port A. For a high-level ACK input, the output buffer will be in the floating (high-impedance) state.

$\overline{STB}$ (Strobe Input)

When the $\overline{STB}$ input is low-level, the data from terminal units will be held in the internal register, and the data will be sent to the system data bus with an $\overline{RD}$ signal to the PPI.

IBF (Input Buffer Full Flag Output)

When data from terminal units is held on the internal register, IBF will be high-level.

INTR (Interrupt Request Output)

This output is used to interrupt the CPU and its operations the same as in mode 1. There are two interrupt enable flags that correspond to $INTE_A$ for mode 1 output and mode 1 input.

$INTE_1$ is used in generating INTR signals in combination with $\overline{OBF}$ and $\overline{ACK}$. $INTE_1$ is controlled by bit setting of PC_6.

$INTE_2$ is used in generating INTR signals in combination with $\overline{IBF}$ and $\overline{STB}$. $INTE_2$ is controlled by bit setting of PC_4.

Fig. 9 shows the timing diagram of mode 2, and Fig. 10 is an example of mode 2 operation.

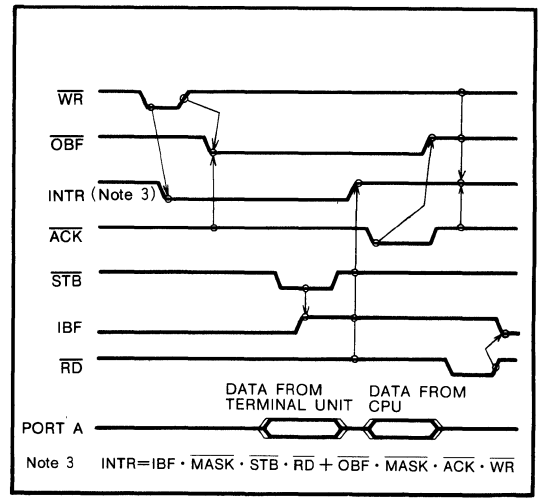


Fig. 9 Mode 2 timing diagram

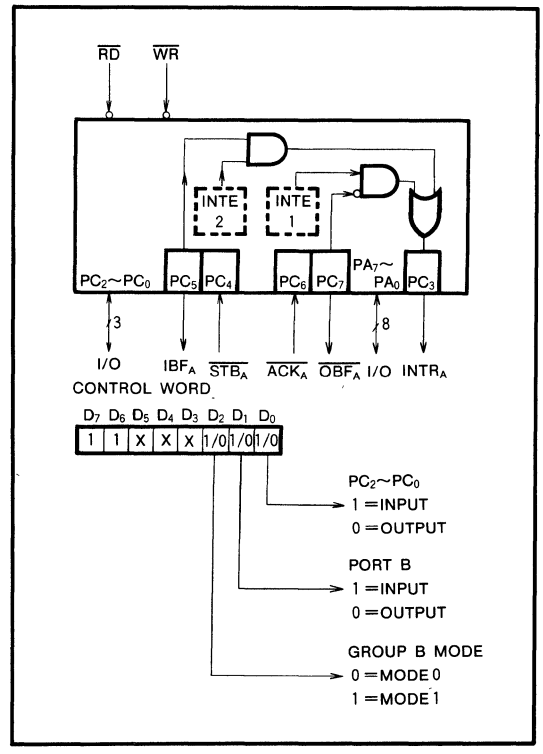


Fig. 10 An example of mode 2 operation

4. Control Signal Read

In mode 1 or mode 2 when using port C as a control port, by CPU execution of an IN instruction, each control signal and bus status from port C can be read.

5. Control Word Tables

Control word formats and operation details for mode 0, mode 1, mode 2 and set/reset control of port C are given in Tables 3, 4, 5 and 6, respectively.

Table 2 Read-out control signals

Data / Mode	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Mode 1, input	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
Mode 1, output	$\overline{OBF_A}$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	$\overline{OBF_B}$	$INTR_B$
Mode 2	$\overline{OBF_A}$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	By group B mode		

Table 3 Mode 0 control words

Control words									Group A		Group B	
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal	Port A	Port C (high-order 4 bits)	Port C (low-order 4 bits)	Port B
1	0	0	0	0	0	0	0	80	OUT	OUT	OUT	OUT
1	0	0	0	0	0	0	1	81	OUT	OUT	IN	OUT
1	0	0	0	0	0	1	0	82	OUT	OUT	OUT	IN
1	0	0	0	0	0	1	1	83	OUT	OUT	IN	IN
1	0	0	0	1	0	0	0	88	OUT	IN	OUT	OUT
1	0	0	0	1	0	0	1	89	OUT	IN	IN	OUT
1	0	0	0	1	0	1	0	8A	OUT	IN	OUT	IN
1	0	0	0	1	0	1	1	8B	OUT	IN	IN	IN
1	0	0	1	0	0	0	0	90	IN	OUT	OUT	OUT
1	0	0	1	0	0	0	1	91	IN	OUT	IN	OUT
1	0	0	1	0	0	1	0	92	IN	OUT	OUT	IN
1	0	0	1	0	0	1	1	93	IN	OUT	IN	IN
1	0	0	1	1	0	0	0	98	IN	IN	OUT	OUT
1	0	0	1	1	0	0	1	99	IN	IN	IN	OUT
1	0	0	1	1	0	1	0	9A	IN	IN	OUT	IN
1	0	0	1	1	0	1	1	9B	IN	IN	IN	IN

Note 4 : OUT indicates output port, and IN indicates input port

Table 4 Mode 1 control words

Control words								Hexa-decimal	Group A					Group B			
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		Port A	Port C				Port C			Port B
										PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0	
1	0	1	0	0	1	0	X	A4 A5	OUT	$\overline{OBF_A}$	$\overline{ACK_A}$	OUT		$INTR_A$	$\overline{ACK_B}$	$\overline{OBF_B}$	$INTR_B$	OUT
1	0	1	0	0	1	1	X	A6 A7	OUT	$\overline{OBF_A}$	$\overline{ACK_A}$	OUT		$INTR_A$	$\overline{STB_B}$	IBF_B	$INTR_B$	IN
1	0	1	0	1	1	0	X	AC AD	OUT	$\overline{OBF_A}$	$\overline{ACK_A}$	IN		$INTR_A$	$\overline{ACK_B}$	$\overline{OBF_B}$	$INTR_B$	OUT
1	0	1	0	1	1	1	X	AE AF	OUT	$\overline{OBF_A}$	$\overline{ACK_A}$	IN		$INTR_A$	$\overline{STB_B}$	IBF_B	$INTR_B$	IN
1	0	1	1	0	1	0	X	B4 B5	IN	OUT		IBF_A	$\overline{STB_A}$	$INTR_A$	$\overline{ACK_B}$	$\overline{OBF_B}$	$INTR_B$	OUT
1	0	1	1	0	1	1	X	B6 B7	IN	OUT		IBF_A	$\overline{STB_A}$	$INTR_A$	$\overline{STB_B}$	IBF_B	$INTR_B$	IN
1	0	1	1	1	1	0	X	BC BD	IN	IN		IBF_A	$\overline{STB_A}$	$INTR_A$	$\overline{ACK_B}$	$\overline{OBF_B}$	$INTR_B$	OUT
1	0	1	1	1	1	1	X	BE BF	IN	IN		IBF_A	$\overline{STB_A}$	$INTR_A$	$\overline{STB_B}$	IBF_B	$INTR_B$	IN

Note 5 : Mode of group A and group B can be programmed independently
6 : It is not necessary for both group A and group B to be in mode 1.

Table 5 Mode 2 control words

Control words								Hexa-decimal (Ex)	Group A						Group B			
									Port A	Port C					PortC			Port B
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0	
1	1	X	X	X	0	0	0	C0	Bidirectional bus	$\overline{OBF_A}$	$\overline{ACK_A}$	IBF_A	$\overline{STB_A}$	$INTR_A$	OUT			OUT
1	1	X	X	X	0	0	1	C1	Bidirectional bus	$\overline{OBF_A}$	$\overline{ACK_A}$	IBF_A	$\overline{STB_A}$	$INTR_A$	IN			OUT
1	1	X	X	X	0	1	0	C2	Bidirectional bus	$\overline{OBF_A}$	$\overline{ACK_A}$	IBF_A	$\overline{STB_A}$	$INTR_A$	OUT			IN
1	1	X	X	X	0	1	1	C3	Bidirectional bus	$\overline{OBF_A}$	$\overline{ACK_A}$	IBF_A	$\overline{STB_A}$	$INTR_A$	IN			IN
1	1	X	X	X	1	0	X	C4	Bidirectional bus	$\overline{OBF_A}$	$\overline{ACK_A}$	IBF_A	$\overline{STB_A}$	$INTR_A$	$\overline{ACK_B}$	$\overline{OBF_B}$	$INTR_B$	OUT
1	1	X	X	X	1	1	X	C6	Bidirectional bus	$\overline{OBF_A}$	$\overline{ACK_A}$	IBF_A	$\overline{STB_A}$	$INTR_A$	$\overline{STB_B}$	IBF_B	$INTR_B$	IN

Table 6 Port C bit set/reset control words

Control words								Hexa-decimal	Port C								Remarks
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0	
0	X	X	X	0	0	0	0	00								0	
0	X	X	X	0	0	0	1	01								1	
0	X	X	X	0	0	1	0	02							0		
0	X	X	X	0	0	1	1	03							1		
0	X	X	X	0	1	0	0	04						0			$INTE_B$ set/reset for mode 1 input
0	X	X	X	0	1	0	1	05						1			$INTE_B$ set/reset for mode 1 output
0	X	X	X	0	1	1	0	06					0				
0	X	X	X	0	1	1	1	07					1				
0	X	X	X	1	0	0	0	08				0					$INTE_A$ set/reset for mode 1 input
0	X	X	X	1	0	0	1	09				1					$INTE_2$ set/reset for mode 2
0	X	X	X	1	0	1	0	0A			0						
0	X	X	X	1	0	1	1	0B			1						
0	X	X	X	1	1	0	0	0C		0							$INTE_A$ set/reset for mode 1 output
0	X	X	X	1	1	0	1	0D		1							$INTE_1$ set/reset for mode 2
0	X	X	X	1	1	1	0	0E	0								
0	X	X	X	1	1	1	1	0F	1								

Note 7 : The terminals of port C should be programmed for the output mode, before the bit set/reset operation is executed.
8 : Also used for controlling the interrupt enable flag(INTE).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
P_d	Power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating free-air temperature range		−20～75	℃
T_{stg}	Storage temperature range		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20～75℃, V_{CC}= 5 V± 5 %, V_{SS}= 0 V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.0		V_{CC}	V
V_{IL}	Low-level input voltage			−0.5		0.8	V
V_{OH}	High-level output voltage	Data bus	I_{OH}=−400μA	2.4			V
		Port	I_{OH}=−200μA				
V_{OL}	Low-level output voltage	Data bus	I_{OL}=2.5mA			0.45	V
		Port	I_{OL}=1.7mA				
I_{OH}	High-level output current (Note10)		V_{OH}=1.5V, R_{EXT}=750Ω	−1		−4	mA
I_{CC}	Supply current from V_{CC}					120	mA
I_{IH}	High-level input current		V_I=V_{CC}			±10	μA
I_{IL}	Low-level input current		V_I=0V			±10	μA
I_{OZ}	Off-state output current		V_O=0V～V_{CC}			±10	μA
C_i	Input terminal capacitance		V_{IL}=V_{SS}, f=1MHz, 25mVrms T_a=25℃			10	pF
$C_{i/o}$	Input/output terminal capacitance		$V_{I/OL}$=V_{SS}, f=1MHz, 25mVrms T_a=25℃			20	pF

Note 9 : Current flowing into an IC is positive, out is negative
10 It is valid only for any 8 input/output pins of PB and PC.

TIMING REQUIREMENTS (T_a=−20～75℃, V_{CC}= 5 V± 5 %, V_{SS}= 0 V, unless otherwise noted)

Symbol	Prameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(R)}$	Read pulse width		300			ns
$t_{su(PE-R)}$	Peripheral setup time before read		0			ns
$t_{h(R-PE)}$	Peripheral hold time after read		0			ns
$t_{su(A-R)}$	Address setup time before read		0			ns
$t_{h(R-A)}$	Address hold time after read		0			ns
$t_{W(W)}$	Write pulse width		300			ns
$t_{su(DQ-W)}$	Data setup time before write		100			ns
$t_{h(W-DQ)}$	Data hold time after write		30			ns
$t_{su(A-W)}$	Address setup time before write		0			ns
$t_{h(W-A)}$	Address hold time after write		20			ns
$t_{W(ACK)}$	Acknowledge pulse width		300			ns
$t_{W(STB)}$	Strobe pulse width		500			ns
$t_{su(PE-STB)}$	Peripheral setup time before strobe		0			ns
$t_{h(STB-PE)}$	Peripheral hold time after strobe		180			ns
$t_{C(RW)}$	Read/write cycle time		850			ns

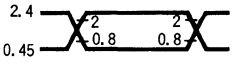
SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}= 5 V± 5 %, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Propagation time from read to data output	C_L=150pF			200	ns
$t_{PVZ(R-DQ)}$	Propagation time from read to data floating (Note11)		10		100	ns
$t_{PHL(W-PE)}$ $t_{PLH(W-PE)}$	Propagation time from write to output				350	ns
$t_{PLH(STB-IBF)}$	Propagation time from strobe to IBF flag				300	ns
$t_{PLH(STB-INTR)}$	Propagation time from strobe to interrupt				300	ns
$t_{PHL(R-INTR)}$	Propagation time from read to interrupt				400	ns
$t_{PHL(R-IBF)}$	Propagation time from read to IBF flag				300	ns
$t_{PHL(W-INTR)}$	Propagation time from write to interrupt				850	ns
$t_{PHL(W-OBF)}$	Propagation time from write to $\overline{OBF}$ flag				650	ns
$t_{PLH(ACK-OBF)}$	Propagation time from acknowledge to $\overline{OBF}$ flag				350	ns
$t_{PLH(ACK-INTR)}$	Propagation time from acknowledge to interrupt				350	ns
$t_{PZV(ACK-PE)}$	Propagation time from acknowledge to data output				300	ns
$t_{PVZ(ACK-PE)}$	Propagation time from acknowledge to data floating (Note11)		20		250	ns

Note 11 : Test conditions are not applied

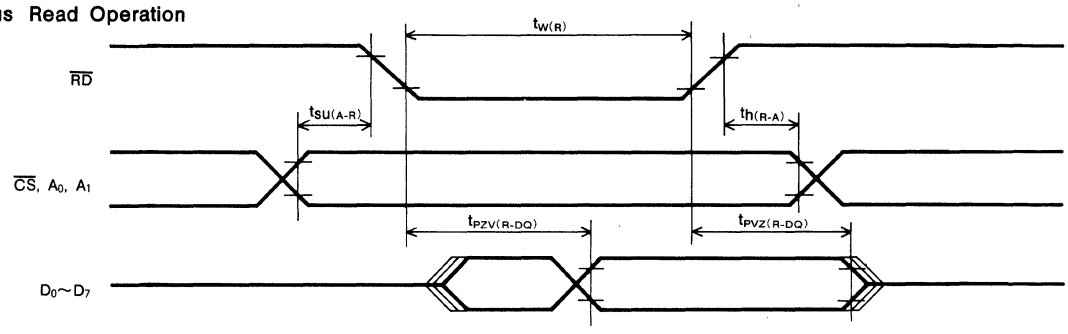
12 : A.C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	20ns
Input pulse fall time	20ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V

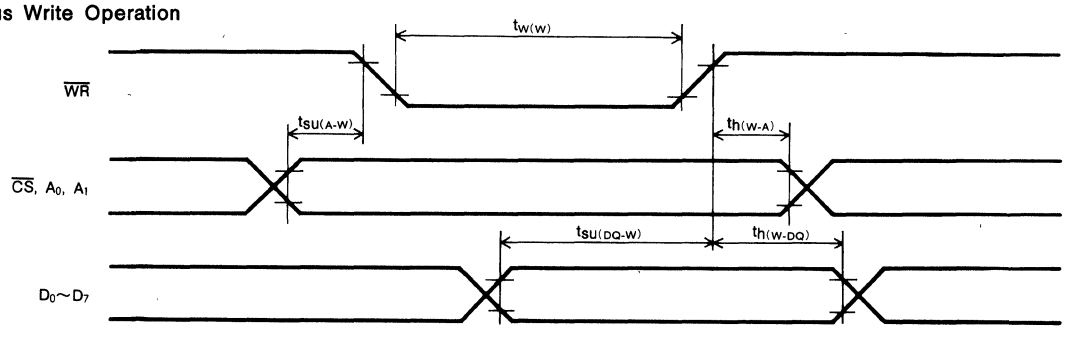


TIMING DIAGRAM

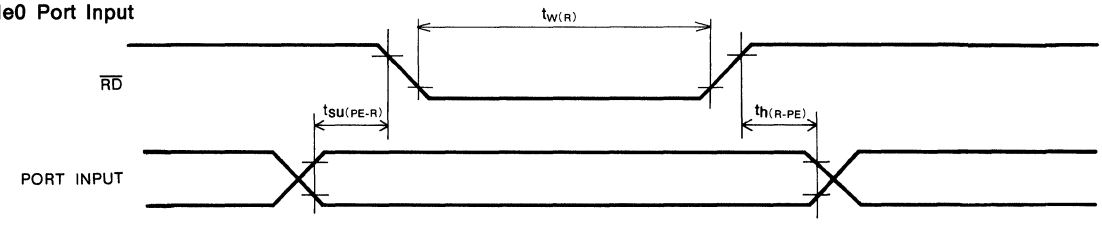
Data Bus Read Operation



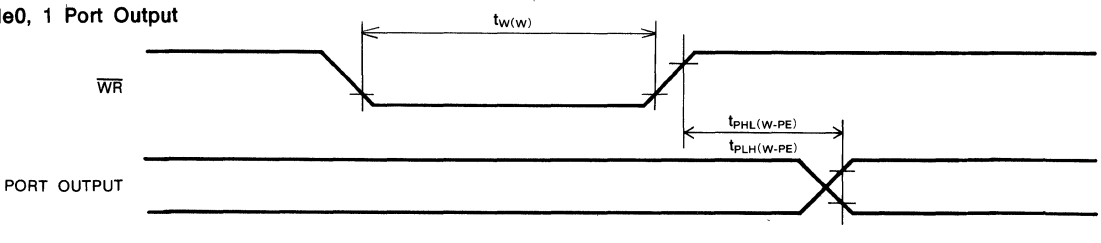
Data Bus Write Operation



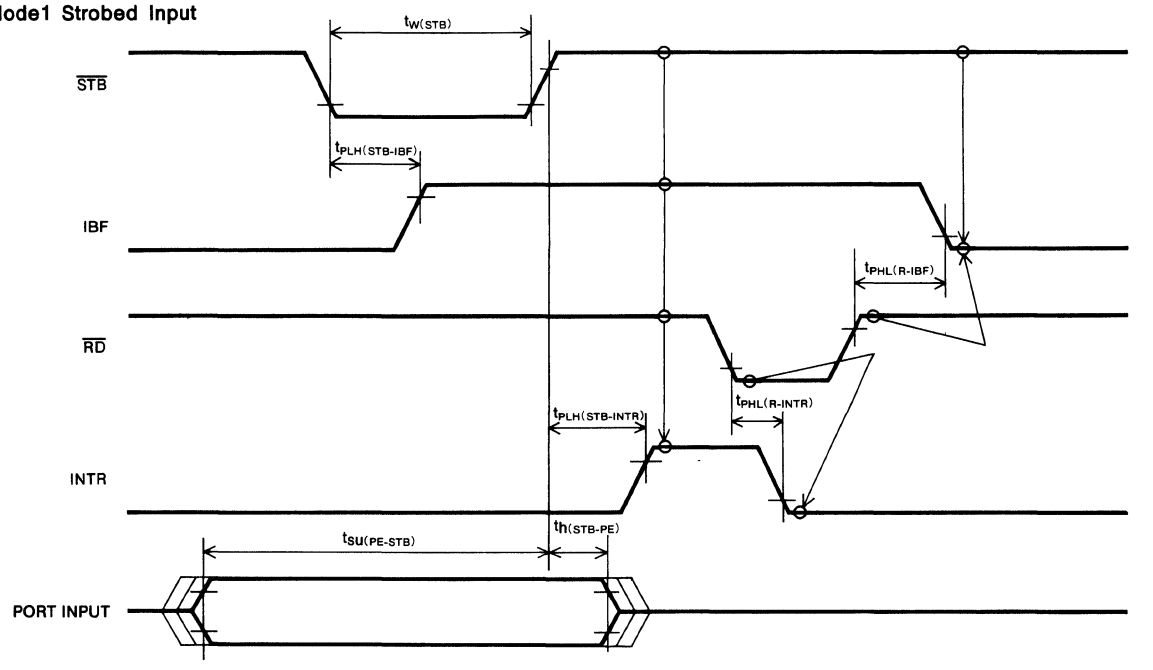
Mode0 Port Input



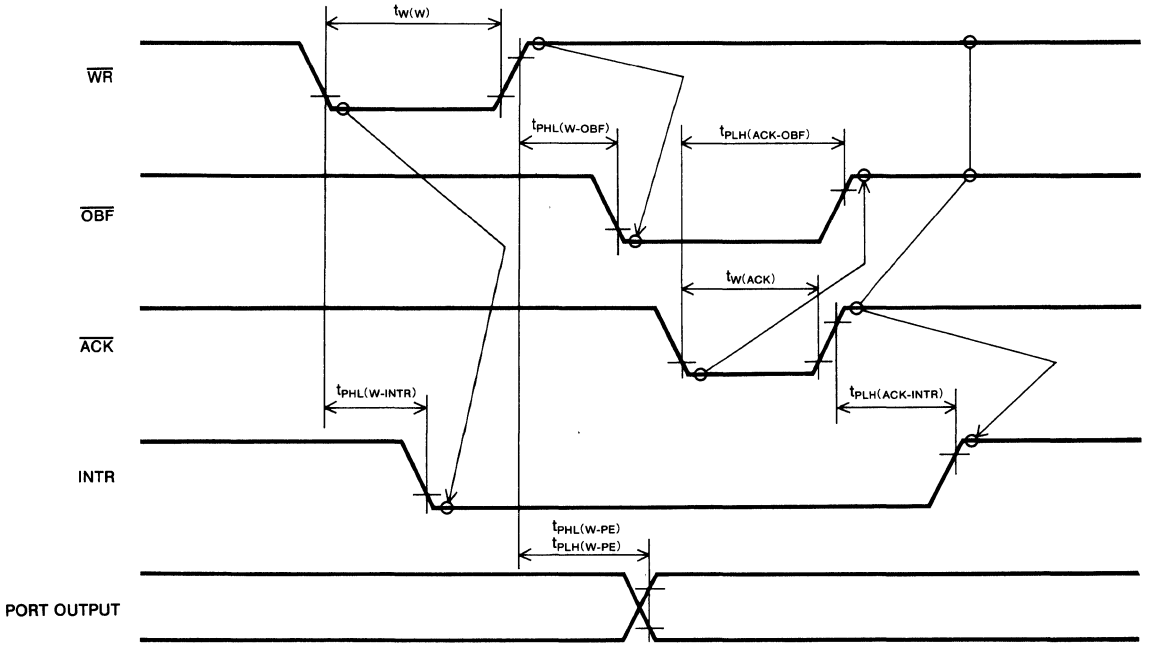
Mode0, 1 Port Output



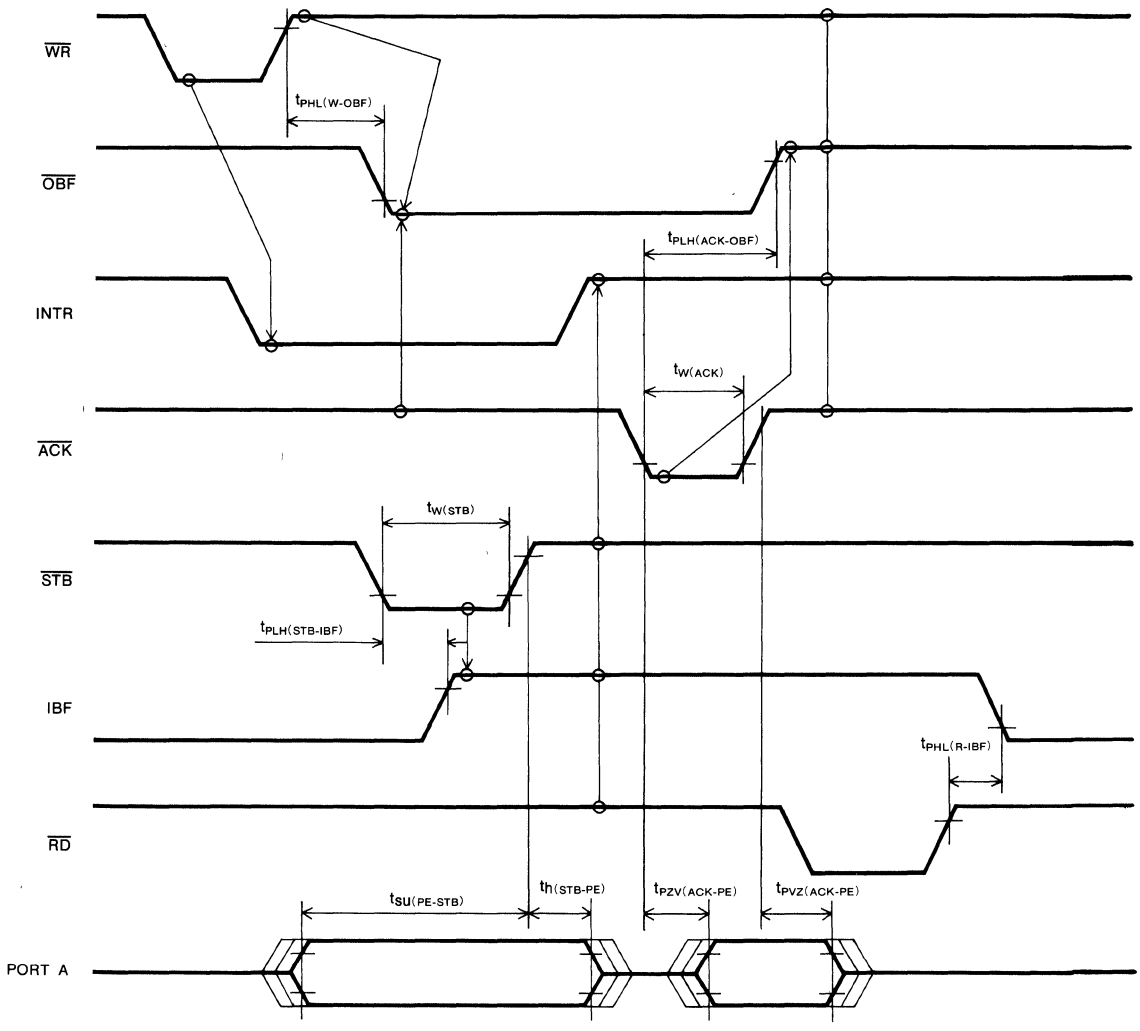
Mode1 Strobed Input



Mode1 Strobed Output



Mode2 Bidirectional



Note 13 INTR=IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$

CIRCUIT EXAMPLES FOR APPLICATIONS

1. Mode 0

An example of a circuit for an application using mode 0 is shown in Fig. 11.

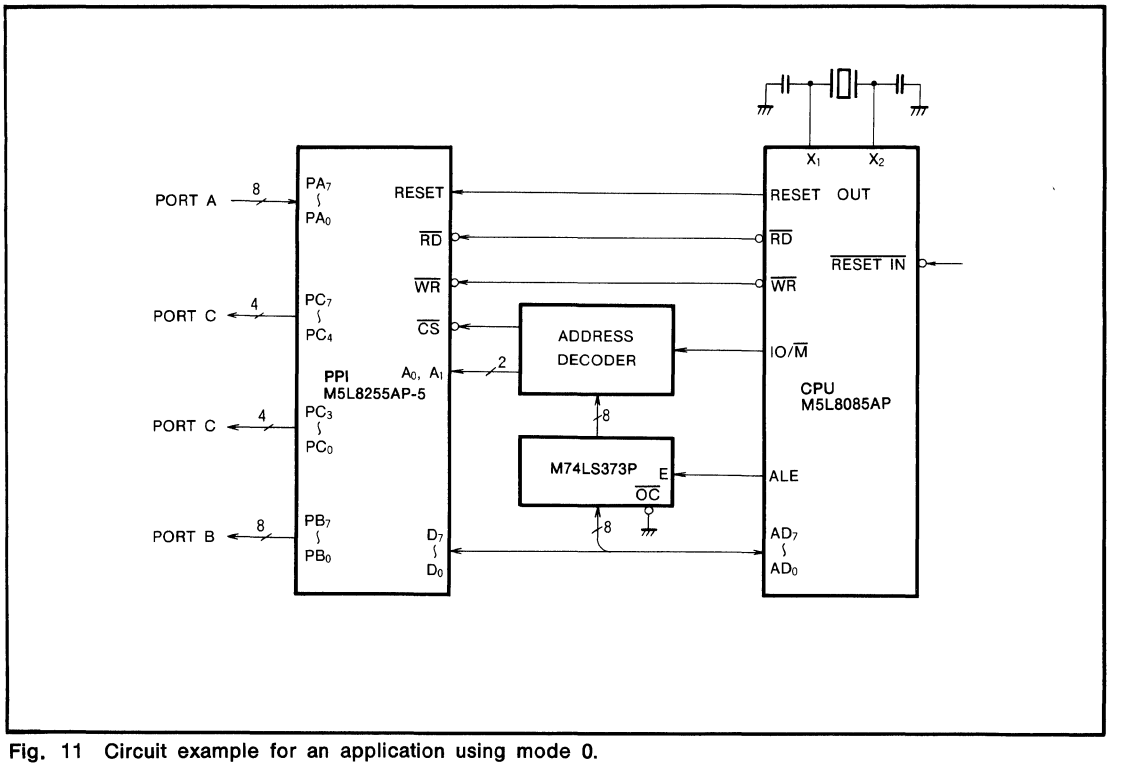


Fig. 11 Circuit example for an application using mode 0.

In this example, the PPI is in mode 0, and the control word should be 10010000 (90_{16})

MVI A, 90#
OUT 03#

The PPI will be initialized by executing the above two instructions.

Then, for example, to read data from port A and to output data to port B and C, the following three instructions can be used.

IN 00# CPU A register ← Port A
OUT 01# Port B ← A register
OUT 02# Port C ← A register

After setting the mode, each port operates as a normal port.

After setting the mode, as shown in Fig. 11, to read data from port A, to output to port B, and to set the first bit of port C=1, the following four instructions can be used.

IN 00# CPU A register ← Port A
OUT 01# Port B ← A register
MVI A, 01# Bit-setting control word for PC_0
OUT 03# Outputting to control address ($\overline{CS}$ = "L", $A_1 = A_0 = 1$)

The other bits of port C, in this case, are not affected.

2. Mode 1

An example of a circuit for an application using mode 1 is shown in Fig. 12.

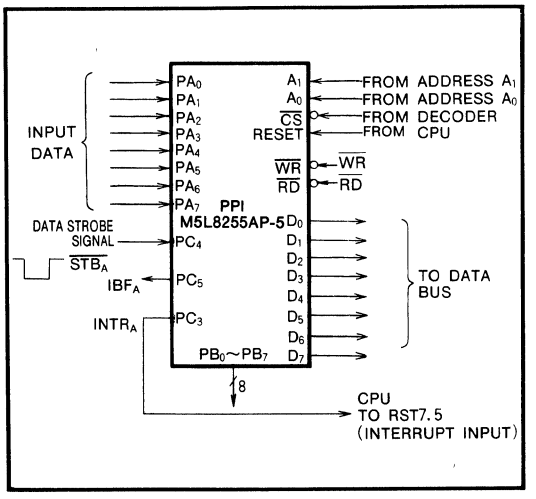


Fig. 12 A circuit for an application using mode 1

Transferring data from a terminal unit to port A and sending a strobe signal to PC_4 will hold the data in the internal latch of the PPI, and PC_5 (IBF input buffer full flag) is set to high-level. If a bit-set of PC_4 has been executed in advance, the CPU can be interrupted by the INTR signal of PC_3 when the input data is latched in the PPI. In this way, port A becomes an interrupting port; and at the same time, port B can select its mode independently.

The actual program for the circuit of Fig. 12 is as follows:

MVI	**A, B0#**	Control word is 10110000, port A is the mode 1 input and the others are output
OUT	**03#**	Outputting to the control address
MVI	**A, 09#**	PC_4bit-set 00001001
OUT	**03#**	Outputting to the control address
EI		Interrupt enable
HLT		Halt

If the data has been set in a terminal unit, and the strobe signal has been input, then the data will be latched in port A and the CPU RST7.5 goes high-level. In the case of Fig. 11, a jump to $003C_{16}$ is executed to continue the program as follows:

$003C_{16}$	**IN**	**00#**	CPU register A ← Port A PC_3 interrupt signal becomes low-level
	EI		
	RET		

3. Mode 2

An example of a circuit for an application using mode 2 is shown in Fig. 13.

In Fig. 13, the data bus of the slave system is connected with the corresponding PPI A bit of the master station. The input port consists of a three-state buffer and gate B which allow the slave CPU to read flag outputs (IBF, $\overline{OBF}$) of the PPI as data.

When the following instruction is executed in this example, the action is as described:

IN 01# (reading in from 01_{16} input port)

The data which is made up of the least significant bit (D_0), the $\overline{OBF}$ (output buffer full flag output) and the next least significant bit (D_1), the IBF (input buffer full flag output) will be read into the slave CPU.

When the following instruction is executed, the action is as described:

IN 00# (reading in from 00_{16} input port)

$\overline{ACK}$ (PC_6) of the PPI becomes low-level by gate C, and the contents of the port A output latch will be read into the slave CPU.

When the following instruction is executed, the action is as described:

OUT 00# (writing out to 00_{16} output port)

$\overline{STB}$ (PC_4) of the PPI becomes low-level by gate D, then the contents of the slave CPU register A will be written into the port A input latch of the PPI.

Actual operations are as follows:

1. PPI is set in mode 2 by the master CPU (03 address).
2. The master CPU writes the data, which is transferred to the slave CPU, into port A of the PPI (in turn, $\overline{OBF}$ becomes low-level).
3. The slave CPU continues to read the state of flags ($\overline{OBF}$ and IBF) as data while $\overline{OBF}$ is high-level (i.e. no data from the master CPU).
4. When the slave CPU senses that $\overline{OBF}$ has become low-level, the slave CPU starts to read the data from 00_{16} (Which is the input address for the preceding data) which is in the output latch of port A (in turn, $\overline{OBF}$ returns to high-level).
5. During this period, the master CPU reads the status flags (reading in from 02 of port C) and checks the states of both the bit 7 ($\overline{OBF}$) and bit 5 (IBF). If $\overline{OBF}$ is low-level, it indicates that the slave CPU has not yet received the data; so the maser does not write new data. If $\overline{OBF}$ is high-level, the master CPU writes the next data.
6. When data is to be transferred to the master CPU, the contents of the slave CPU A register will be transmited to the port input latch of the PPI The slave CPU transfers the data to address 00_{16} (in turn, the IBF becomes high-level).
7. The master CPU transfers data to port C and then checks the status flag. If the input latch contains data from the slave CPU, which is indicated by IBF having a high-level output, the data is read from port (00_{16}) (in turn, the IBF returns to low-level).
8. The slave CPU reads the status flag from 01_{16} to determine if IBF has returned to low-level If it has not, new data will not be written as long as IBF is high-level.
9. In this way, data can be exchanged. Since there are two sets of independent registers, input latch and output latch, used by port A of the PPI, it is not necessary to alternate input/output transfers.

A program which has operating functions as described above, is explained as follows.

The operation, in mode 2, for group A of the PPI is considered here.

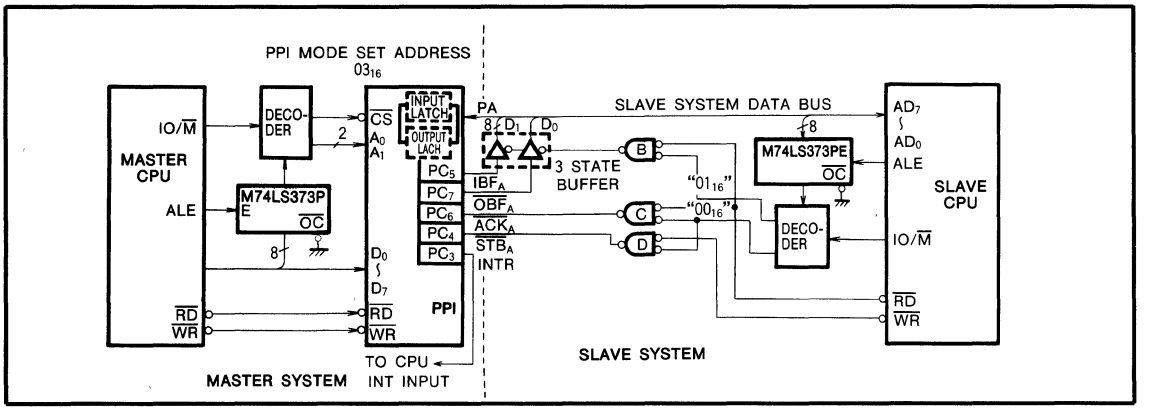
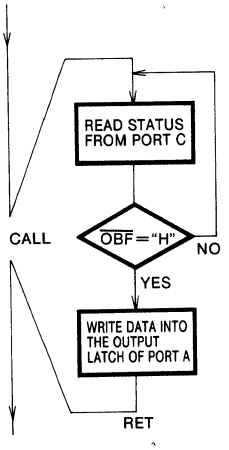


Fig. 13 A circuit for an application using mode 2

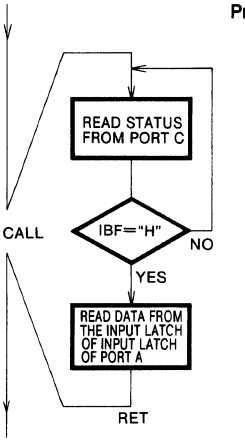
1. Master CPU subroutine for transmitting data to the slave CPU.



Program example

MOUT	PUSH	PSW
OBF	IN	02#
	ANI	80#
	JZ	OBF
	POP	PSW
	OUT	00#
	RET	

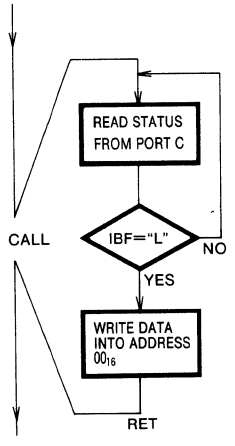
2. Subroutine for receiving data from the slave CPU.



Program example

MIN	IN	02#
	ANI	20#
	JZ	MIN
	IN	00#
	RET	

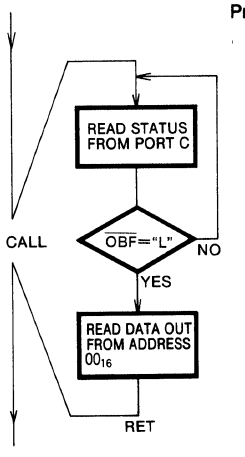
3. Slave CPU subroutine for transmitting data to the master CPU.



Program example

SOUT	PUSH	PSW
IBF	IN	01#
	ANI	02#
	JNZ	IBF
	POP	PSW
	OUT	00#
	RET	

4. Subroutine for receiving data from the master CPU.



Program example

SIN	IN	01#
	ANI	01#
	JNZ	SIN
	IN	00#
	RET	

4. Address Decoding

Address decoding with multiple PPI units is shown in Figs. 14 and 15. These are functionally equal.

The same address data is output to both the upper and lower 8 bits address bus with the execution of IN or OUT instruction by the CPU.

5. PPI Initialization

It is advisable to rest the PPI with a system initial reset and to select the mode at the beginning of a system program. The initial state of the PPI used as an output port is shown in Fig. 16.

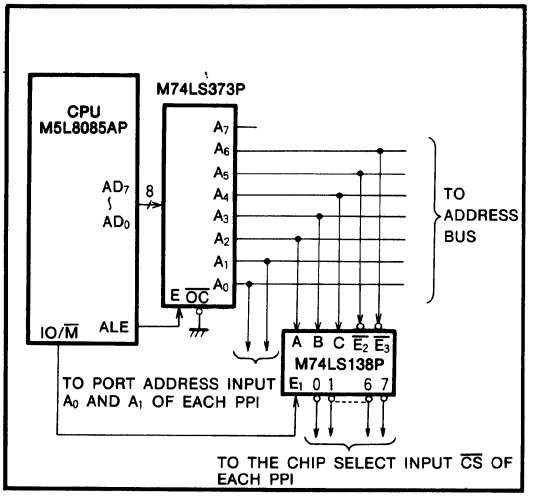


Fig. 14 PPI address decoding (case 1)

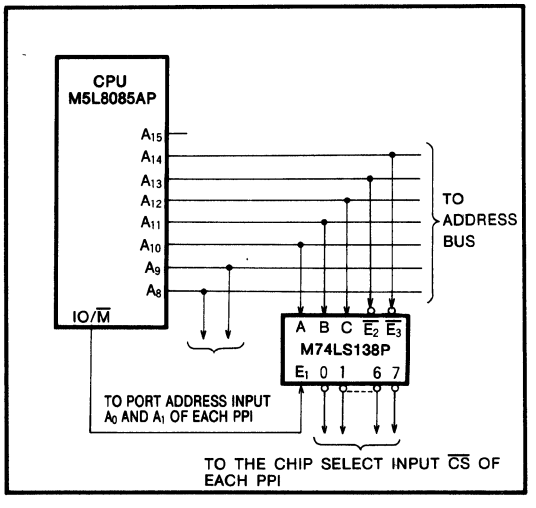


Fig. 15 PPI address decoding (case 2)

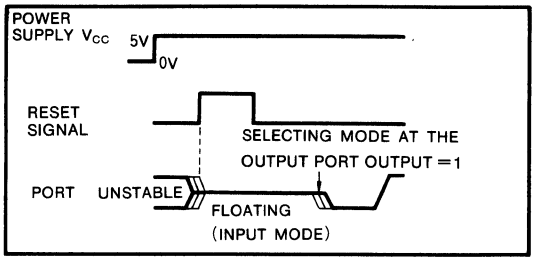


Fig. 16 PPI initialization

Note 14 : Period of reset pulse must be at least 50μs during or after power on. Subsequent reset pulse can be 500ns minimum.

M5L8257P-5

PROGRAMMABLE DMA CONTROLLER

DESCRIPTION

The M5L8257P-5 is a programmable 4-channel direct memory access (DMA) controller. It is produced using the N-channel silicon-gate ED-MOS process and is specifically designed to simplify data transfer at high speeds for microcomputer systems

The LSI operates on a single 5V power supply.

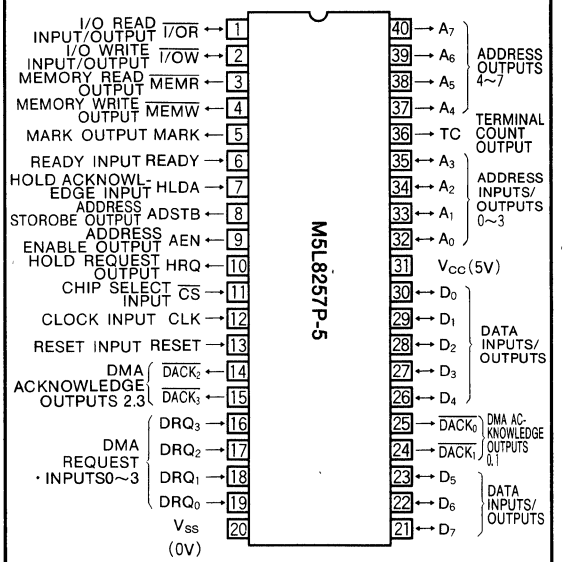
FEATURES

- Single 5V supply voltage
- TTL compatible interface
- Priority DMA request logic
- Channel-masking function
- Terminal count and Modulo 128 outputs
- 4-channel DMA controller
- Compatible with MELPS85 devices

APPLICATION

DMA control of peripheral equipment such as floppy disks and CRT terminals that require high-speed data transfer.

PIN CONFIGURATION (TOP VIEW)

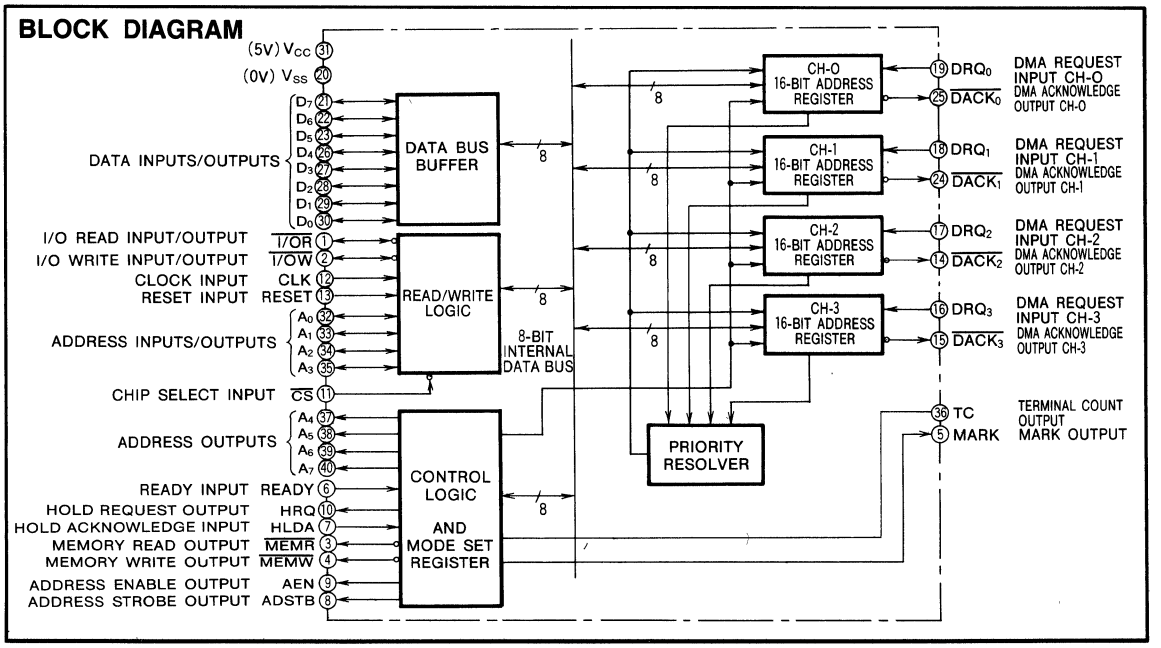


Outline 40P4

FUNCTION

The M5L8257P-5 controller is used in combination with the M5L8212P 8-bit input/output port in 8-bit microcomputer systems. It consists of a channel section to acknowledge DMA requests, control logic to exchange commands and data with the CPU, read/write logic, and registers to hold transfer addresses and count the number of bytes to be transferred. When a DMA request is made to an unmasked channel from the peripherals after setting of the transfer mode, transfer-start address and the number of transferred bytes for the registers, the M5L8257P-5 issues a priority request for the use of the bus to the CPU. On receiving an HLDA signal from the CPU, it sends a DMA acknowledge signal to the channel with the highest priority, starting DMA operation. During DMA operation, the contents of the high-order 8 bits of the transfer memory address are transmitted to the M5L8212P address-latch device through pins $D_0 \sim D_7$. The contents of the low-order 8 bits are transmitted through pins $A_0 \sim A_7$. After address transmission, DMA transfer can be started by dispatching read and write signals to the memories and peripherals.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

OPERATION

I/O Read Input/Output ($\overline{I/OR}$)
When the M5L8257P-5 is in slave-mode operation, this threestate, bidirectional pin serves for inputting and reads the upper/lower bytes of the 8-bit status register or 16-bit DMA address register and the high/low order bytes of the terminal counter.
In the master mode, the pin gives control output and is used to obtain data from a peripheral equipment during the DMA write cycle.

I/O Write Input/Output ($\overline{I/OW}$)
This pin is also of the three-state bidirectional type. When the M5L8257P-5 is in slave-mode operation, it serves for inputting and loads the contents of the data bus on the 8-bit status register and the upper/lower bytes of the 16-bit terminal counter or 16-bit DMA address register.

Memory Read Output ($\overline{MEMR}$)
This active-low three-state output is used to read data from the addressed memory location during DMA read cycles.

Memory Write Output ($\overline{MEMW}$)
This active-low three-state output is used to write data into the addressed memory location during DMA write cycles.

Mark Output (MARK)
This signal notifies that the DMA transfer cycle for each channel is the 128th cycle since the previous MARK output.

Ready Input (READY)
This asynchronous input is used to extend the memory read and write cycles in the M5L8257P-5 with wait states if the selected memory requires longer access time.

Hold Acknowledge Input (HLDA)
This input from the CPU indicates that the system bus is controlled by the M5L8257P-5.

Address Strobe Output (ADSTB)
This output strobes the most significant byte of the memory address into the M5L8212P (8-bit input/output port) through the data bus.

Address Enable Output (AEN)
This signal is used to disable the system data bus and system control bus by means of the bus enable pin on the system controller. It may also be used to inhibit non-DMA devices from responding during DMA cycles.

Hold Request Output (HRQ)
This output requests control of the system bus. HRQ will normally be applied to the HOLD input on the CPU.

Chip-Select Input ($\overline{CS}$)
This pin is active on a low-level. It enable the $\overline{I/OR}$ and $\overline{I/OW}$ signals output from the CPU, when the M5L8257P-5 is in slave-mode operation.
In the master mode, it is disabled to prevent the chip from selecting itself while performing the DMA function.

Clock Input (CLK)
This pin generates internal timing for the M5L8257P-5 and is connected to the ϕ (TTL) output of the system clock.

Reset Input (RESET)
This asynchronous input clears some registers and control lines inside the M5L8257P-5.

DMA Acknowledge Outputs ($\overline{DACK0}$~$\overline{DACK3}$)
These active-low outputs indicate that the peripheral equipment connected to the channel in question can execute the DMA cycle.

DMA Request Inputs (DRQ0~DRQ3)
These independent, asynchronous channel-request inputs are used to secure use of the DMA cycle for the peripherals.

Data-Bus Buffer
This three-state, bidirectional, 8-bit buffer interfaces the M5L8257P-5 to the CPU for data transfer. During a DMA cycle the upper 8 bits of the DMA address are output to the M5L8212P latch device through this buffer.

Address Inputs/Outputs (A_0~A_3)
The four bits of these input/output pins are bidirectional. When the M5L8257P-5 is in slave-mode operation, serve to input and address the internal registers. In the case of master operation, they output the low-order 4 bits of the 16-bit memory address.

Terminal Count Output (TC)
When the terminal count registers became (3FFF)H, terminal count signal is out. And this signal notifies that the present DMA cycle is the last cycle for this data block.

Address Inputs/Outputs (A_4~A_7)
These four address lines are three-state outputs which constitute bits 4 through 7 of the memory address generated by the M5L8257P-5 during all DMA cycles.

Register Initialization

Two 16-bit registers are provided for each of the 4 channels.

DMA Address register

15															0
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

DMA TRANSFER STARTING ADDRESS

Terminal count register

15	14	13													0
Rd	Wr	C_{13}	C_{12}	C_{11}	C_{10}	C_9	C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

DMA MODE — NUMBER OF TRANSFERRED BYTES−1

The DMA transfer starting address, number of transferred bytes, and DMA mode are written for each channel in 2 steps using the 8-bit data bus. The lower-order and upper-order bytes are automatically indicated by the first-last flip-flop for the writing and reading in 2 continuous steps.

The DMA mode (read, write, or verify) is indicated by the upper 2 bits of the terminal count register. The read mode refers to the operation of peripheral devices reading data out of memory. The write mode refers to data from peripheral devices being written into memory. The verify mode sends neither the read nor the write signals and performs a date check at the peripheral device.

In addition to the above-mentioned registers, there is a mode set register and a status register.

Mode set register (write only)

7							0
AL	TCS	EW	RP	EN3	EN2	EN1	EN0

ADDED FUNCTION SETTING BITS — CHANNEL ENABLE BITS

Status Register (read only)

7							0
0	0	0	UP	TC3	TC2	TC1	TC0

The upper-order 4 bits of the mode set register are used to select the added function, as described in 5-66. The lower-order 4 bits are mask bits for each channel. When set to 1, DMA requests are allowed. When the reset signal is input, all bits of the mode set and status registers are reset and DMA is inhibited for all channels. Therefore, to execute DMA operations, registers must first be initialized. An example of such an initialization is shown below.

MODESET:

```
MVI  A, ADDL
OUT  00H:   Channel 0 lower-order address
MVI  A, ADDH
OUT  00H:   Channel 0 upper-order address
MVI  A, TCL
OUT  01H:   Channel 0 terminal count lower-order
MVI  A, TCH
OUT  01H:   Channel 0 terminal count upper-order
MVI  A, XX
OUT  08H:   Mode set resister
```

As can be seen from the above example, until the contents of the address register and terminal count register become valid, the enable bit of the mode set register must not be set. This prevents memory contents from being destroyed by improper DRQ signals from peripheral devices.

DMA OPERATION DESCRIPTION

When a DMA request signal is received at the DRQ pin from a peripheral device after register initialization for a channel that is not masked, the M5L8257P-5 outputs a hold request signal to the CPU to begin DMA operation (S_1).

The CPU, upon receipt of the HRQ signal, outputs the HLDA signal which reserves capture of the bus after it has executed the present instruction to place this system in the hold state.

When the M5L8257P-5 receives the HLDA signal, an internal priority determining circuit selects the channel with the highest priority for the beginning of data transfer (S_0).

Upon the next S_1 state, the address signal is sent. The lower-order 8 bits and upper-order 8 bits are sent by means of the $A_0 \sim A_7$ and $D_0 \sim D_7$ pins respectively, latched into the M5L8212P and output at pins $A_8 \sim A_{15}$. Simultaneous with this, the AEN signal is output to prohibit the selection of a device not capable of DMA.

In the S_2 state, the read, extended write, and DACK signals are output and data transferred from memory or a peripheral device appears on the data bus.

In the S_3 state, the write signal required to write data from the bus is output. At this time if the remaining number of bytes to be transferred from the presently selected channel has reached 0, the terminal count (TC) signal is output. Simultaneously with this, after each 128-byte data transfer a mark signal is output as required. In addition, in this state the READY pin is sampled and, if low-level, the wait state (S_W) is entered. This is used to perform DMA with slow access memory devices. In the verify mode, READY input is ignored.

In the S_4 state, the DRQ and HLDA pins are sampled at the end of a transferred byte as the address signal, control signals, and $\overline{DACK}$ signal are held to determine if transfer will continue.

As described above, transfer of 1 byte requires a minimum of 4 states for execution. For example, if a 2MHz clock input is used, the maximum transfer rate is 500k byte/s.

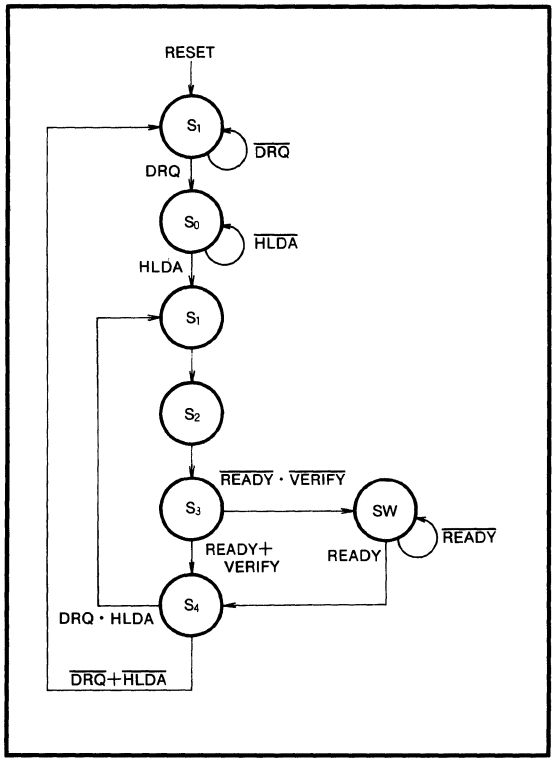


Fig. 1 DMA Operation state transition diagram

MEMORY MAPPED I/O

When using memory mapped I/O, it is neccessary to change the connections for the control signals.

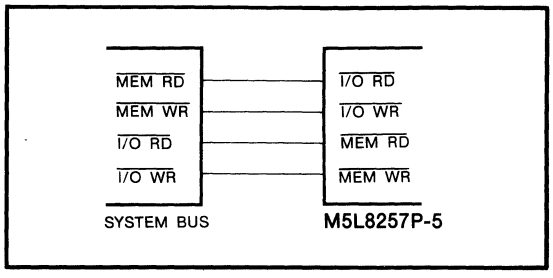
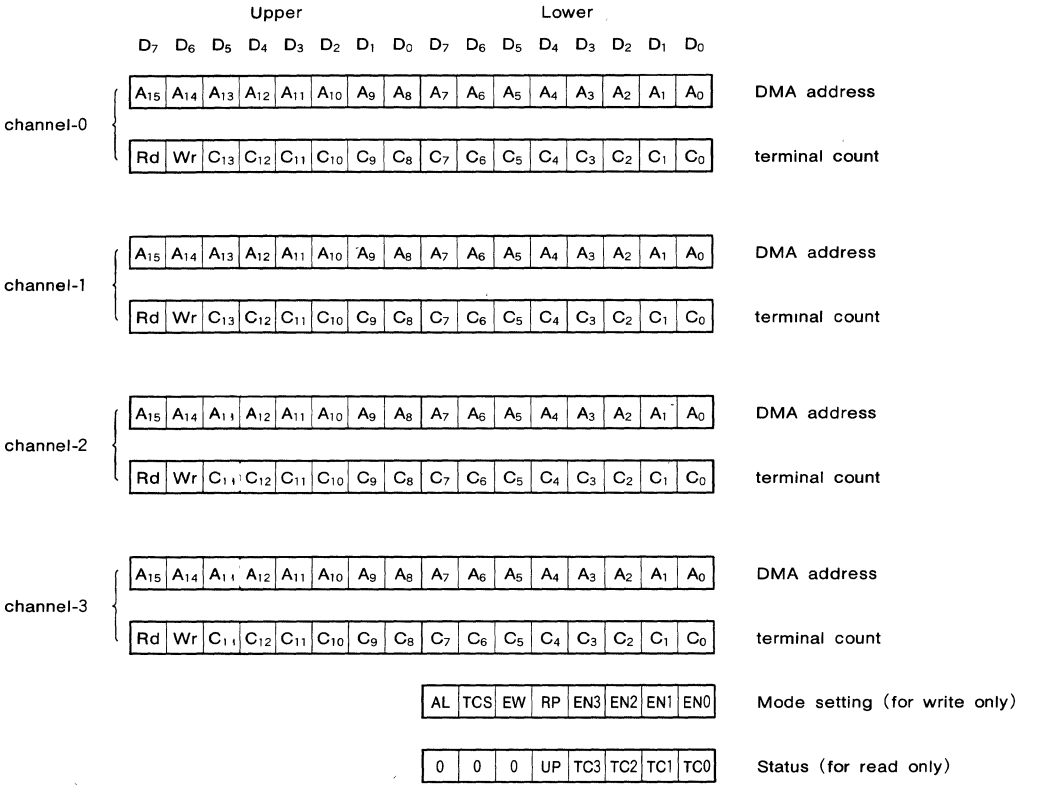


Fig. 2 Memory mapped I/O

Also, the read mode and write mode specifications for setting the mode of the terminal count are reversed.

INTERNAL REGISTERS OF THE M5L8257P-5



$A_0 \sim A_{15}$: Address of the memories for which DMA will be carried out from now on In initialization, DMA start addresses must be written

$C_0 \sim C_{13}$: Terminal counts-in this IC (the number of remaining transfer bytes minus 1) The address is decremented for each DMA transfer of one byte, and when the transfer is finished, becomes $(3FFF)_H$ If additional DRQ signals are input, the address continues to be decremented.

Rd. Wr : Used for DMA-mode setting by the following convention·

Rd	Wr	Mode to be set
0	0	DMA verify
0	1	DMA write
1	0	DMA read
1	1	Prohibition

AL : Automatic load mode. When this bit has been set, contents of the channel 3 register are written, as are on the channel 2 register when channel 2 DMA transfer comes to an end This mode allows quick, automatic chaining operations without intervention of the software

EW : Extended write signal mode When this bit has been set, write signals can be transmitted in advance to memories and peripheral equipment requiring long access time

TCS : Terminal count stop When a DMA transfer process is complete, with terminal-count output, the channel-enable mask of that channel is reset, prohibiting subsequent DMA cycles.

RP : Rotating priority mode The setting of this mode allows the priority order to be rotated by each byte transfer.
The setting priority is fixed with the channel 0 as highest, followed by channel 1 , 2 and 3 in descending order

Channel used for the present data transfer		CH-0	CH-1	CH-2	CH-3
Priority list for the next cycle	1	CH-1	CH-2	CH-3	CH-0
	2	CH-2	CH-3	CH-0	CH-1
	3	CH-3	CH-0	CH-1	CH-2
	4	CH-0	CH-1	CH-2	CH-3

EN0~EN3 : Channel-enable bit. This mask prohibits or allows the DMA request When the reset signal is applied, all channels are disabled.

UP : Update flag. This is set when register contents are transferred in an automatic load mode from channel 3 to channel 2.

TC0~TC3 : Terminal-count status flags. At the time of terminal-count output, the flag corresponding to the channel is set
The flag is, set by reading the status register, annd is unaffected by the TCS bits

REGISTER ADDRESS

Address input				F/L	Register
A_3	A_2	A_1	A_0		
0	0	0	0	0	channel 0 DMA address Low-order
0	0	0	0	1	channel 0 DMA address High-order
0	0	0	1	0	channel 0 terminal count Low-order
0	0	0	1	1	channel 0 terminal count High-order
0	0	1	0	0	channel 1 DMA address Low-order
0	0	1	0	1	channel 1 DMA address High-order
0	0	1	1	0	channel 1 terminal count Low-order
0	0	1	1	1	channel 1 terminal count High-order
0	1	0	0	0	channel 2 DMA address Low-order
0	1	0	0	1	channel 2 DMA address High-order
0	1	0	1	0	channel 2 terminal count Low-order
0	1	0	1	1	channel 2 terminal count High-order
0	1	1	0	0	channel 3 DMA address Low-order
0	1	1	0	1	channel 3 DMA address High-order
0	1	1	1	0	channel 3 terminal count Low-order
0	1	1	1	1	channel 3 terminal count High-order
1	0	0	0	—	Mode Setting (for Write Only)
1	0	0	0	—	Status (for Read Only)

F/L : First/last flip-flop This is toggled when register-write or read operations for each channel are finished, and specifies whether the next write or read operaton is to be for the upper bytes or the lower bytes. This means that write and read operations for each register must be carried out for a set of lower and higher bytes.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power-supply voltage	With respect to V_{SS}	−0.5∼7	V
V_I	Input voltage		−0.5∼7	V
V_O	Output voltage		−0.5∼7	V
P_d	Power dissipation (max)	T_a=25℃	1000	mW
Topr	Operating free-air temperature range		−20∼75	℃
Tstg	Storage temperature range		−65∼150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Power-supply voltage	4.75	5	5.25	V
V_{SS}	Power-supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, V_{CC}= 5 V± 5 %, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}	V
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{OL}	Low-level output voltage	I_{OL}=1.6mA			0.45	V
V_{OH1}	High-level output voltage for AB, DB and AEN	I_{OH}=−150μA	2.4			V
V_{OH2}	High-level output voltage for HRQ	I_{OH}=−80μA	3.3			V
V_{OH3}	High-level output voltage for others		2.4			V
I_{CC}	Supply current from V_{CC}				120	mA
I_I	Input current	V_I=0V, V_{CC}	−10		10	μA
I_{OZ}	Off-state output current	V_O=0V~V_{CC}	−10		10	μA
C_I	Input terminal capacitance	T_a=25℃, V_{CC}=V_{SS} Pins other than that under measurement are set to 0V, f_C=1MHz			10	pF
$C_{I/O}$	Input/output terminal capacitance				20	pF

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}= 5 V± 5 %, V_{SS}= 0 V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(R)}$	Read pulse width		250			ns
$t_{su(A-R)}$ $t_{su(\overline{CS}-R)}$	Address or $\overline{CS}$ setup time before read		0			ns
$t_{h(R-A)}$ $t_{h(R-\overline{CS})}$	Address or $\overline{CS}$ hold time after read		0			ns
$t_{w(W)}$	White pulse width		200			ns
$t_{su(A-W)}$	Address setup time before write		20			ns
$t_{h(W-A)}$	Address hold time after write		0			ns
$t_{su(DQ-W)}$	Data setup time before write		200			ns
$t_{h(W-DQ)}$	Data hold time after write		0			ns
$t_{w(RST)}$	Reset pulse width		300			ns
$t_{su(Vcc-RST)}$	Supply voltage setup time before reset		500			ns
t_r	Input signal rise time				20	ns
t_f	Input signal fall time				20	ns
$t_{su(RST-W)}$	Reset setup time before write		2			$t_{C(\phi)}$
$t_{C(\phi)}$	Clock cycle time		0.32		4	μs
$t_{w(\phi)}$	Clock pulse width high-level		80		$0.8t_{C(\phi)}$	ns
$t_{su(DRQ-\phi)}$	DRQ setup time before clock		70			ns
$t_{h(HLDA-DRQ)}$	DRQ hold time after HLDA		0			ns
$t_{su(HLDA-\phi)}$	HLDA setup time before clock		100			ns
$t_{su(RDY-\phi)}$	Ready setup time before clock		30			ns
$t_{h(\phi-RDY)}$	Ready hold time after clock		20			ns

SLAVE MODE SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}= 5 V± 5 %, V_{SS}= 0 V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Output data enable time after read	C_L=150pF	0		200	ns
$t_{PVZ(R-DQ)}$	Output data disable time after read		20		100	ns

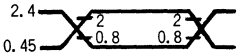
DMA MODE SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PLH(\phi-HRQ)}$ $t_{PHL(\phi-HRQ)}$	Propagation time from clock to HRQ (Note1)				160	ns
$t_{PLH(\phi-HRQ)}$ $t_{PHL(\phi-HRQ)}$	Propagation time from clock to HRQ (Note3)				250	ns
$t_{PLH(\phi-AEN)}$	Propagation time from clock to AEN (Note1)				300	ns
$t_{PHL(\phi-AEN)}$	Propagation time from clock to AEN (Note1)				200	ns
$t_{PZV(AEN-A)}$	Propagation time from AEN to address active (Note4)		20			ns
$t_{PZV(\phi-A)}$	Propagation time from clock to address active (Note2)				250	ns
$t_{PVZ(\phi-A)}$	Propagation time from clock to address floating (Note2)				150	ns
$t_{PLH(\phi-A)}$	Address setup time after clock (Note2)				250	ns
$t_{h(\phi-A)}$	Address hold time after clock (Note2)		$t_{PLH(\phi-A)}-50$			ns
$t_{h(R-A)}$	Address hold time after read (Note4)		60			ns
$t_{h(W-A)}$	Address hold time after write (Note4)		300			ns
$t_{PZV(\phi-DQ)}$	Propagation time from clock to data active				300	ns
$t_{PVZ(\phi-DQ)}$	Propagation time from clock to data floating (Note2)		$t_{PHL(\phi-ASTB)}+20$		170	ns
$t_{PHL(A-ASTB)}$	Propagation time from address to address strobe (Note2)		100			ns
$t_{h(ASTB-A)}$	Propagation time from address strobe to address hold (Note4)		50			ns
$t_{PLH(\phi-ASTB)}$	Propagation time from clock to address strobe (Note1)				200	ns
$t_{PHL(\phi-ASTB)}$	Propagation time from clock to address strobe (Note1)				140	ns
$t_{W(ASTB)}$	Address strobe pulse width (Note4)		$t_{C(\phi)}-100$			ns
$t_{PHL(AS-R)}$ $t_{PHL(AS-WE)}$	Propagation time from address strobe to read or extended write (Note4)		70			ns
$t_{h(DQ-R)}$ $t_{h(DQ-WE)}$	Read or extended write hold time after data (Note4)		20			ns
$t_{PLH(\phi-DACK)}$ $t_{PHL(\phi-TC/MARK)}$ $t_{PLH(\phi-TC/MARK)}$	Propagation time from clock to $\overline{DACK}$ or TC/MARK (Note1, 5)				250	ns
$t_{PHL(\phi-R)}$ $t_{PHL(\phi-W)}$ $t_{PHL(\phi-WE)}$	Propagation time from clock to read, write or extended write (Note2, 6)				200	ns
$t_{PLH(\phi-R)}$ $t_{PLH(\phi-W)}$	Propagation time from clock to read or write (Note2, 7)				200	ns
$t_{PZV(\phi-R)}$ $t_{PZV(\phi-W)}$	Propagation time from clock to read active or write active (Note2)				300	ns
$t_{PVZ(\phi-R)}$ $t_{PVZ(\phi-W)}$	Propagation time from clock to read floating or write floating (Note2)				150	ns
$t_{W(R)}$	Read pulse width (Note4)		$2t_{C(\phi)}+t_{W(\phi)}-50$			ns
$t_{W(W)}$	Write pulse width (Note4)		$t_{C(\phi)}-50$			ns
$t_{W(WE)}$	Extended write pulse width (Note4)		$2t_{C(\phi)}-50$			ns

Note 1 : Load=1TTL
2 : Load=1TTL+50pF
3 : Load=1TTL+(R_L=3.3kΩ), V_{OH}=3.3V
4 : Tracking specification

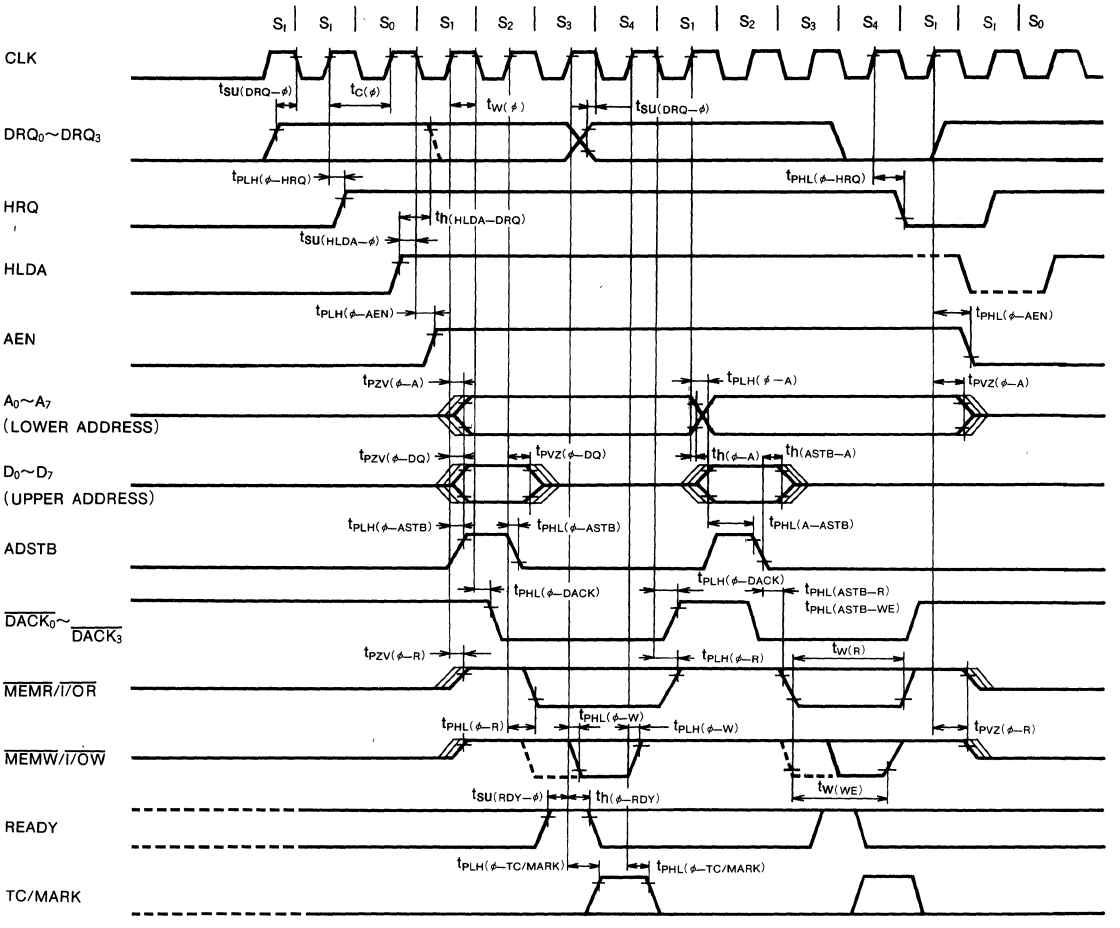
Note 5 : $\Delta t_{PLH(\phi-DACK)}<50ns$, $\Delta t_{PHL(\phi-TC/MARK)}<50ns$, $\Delta t_{PLH(\phi-TC/MARK)}<50ns$
6 : $\Delta t_{PHL(\phi-R)}<50ns$, $\Delta t_{PHL(\phi-W)}<50ns$, $\Delta t_{PHL(\phi-WE)}<50ns$
7 : $\Delta t_{PLH(\phi-R)}<50ns$, $\Delta t_{PLH(\phi-W)}<50ns$
8 : A. C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	20ns
Input pulse fall time	20ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V



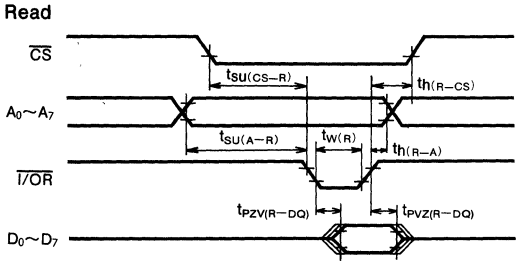
TIMING DIAGRAMS

DMA Mode

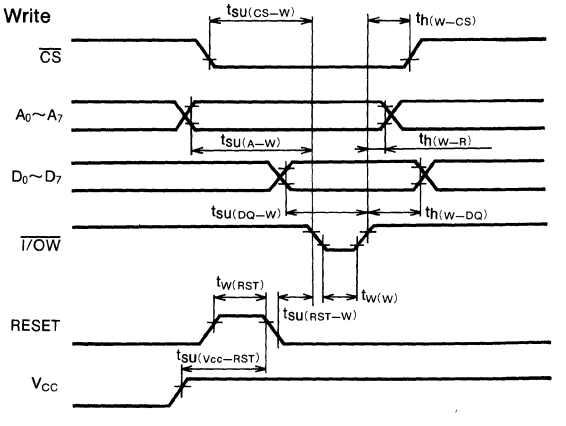


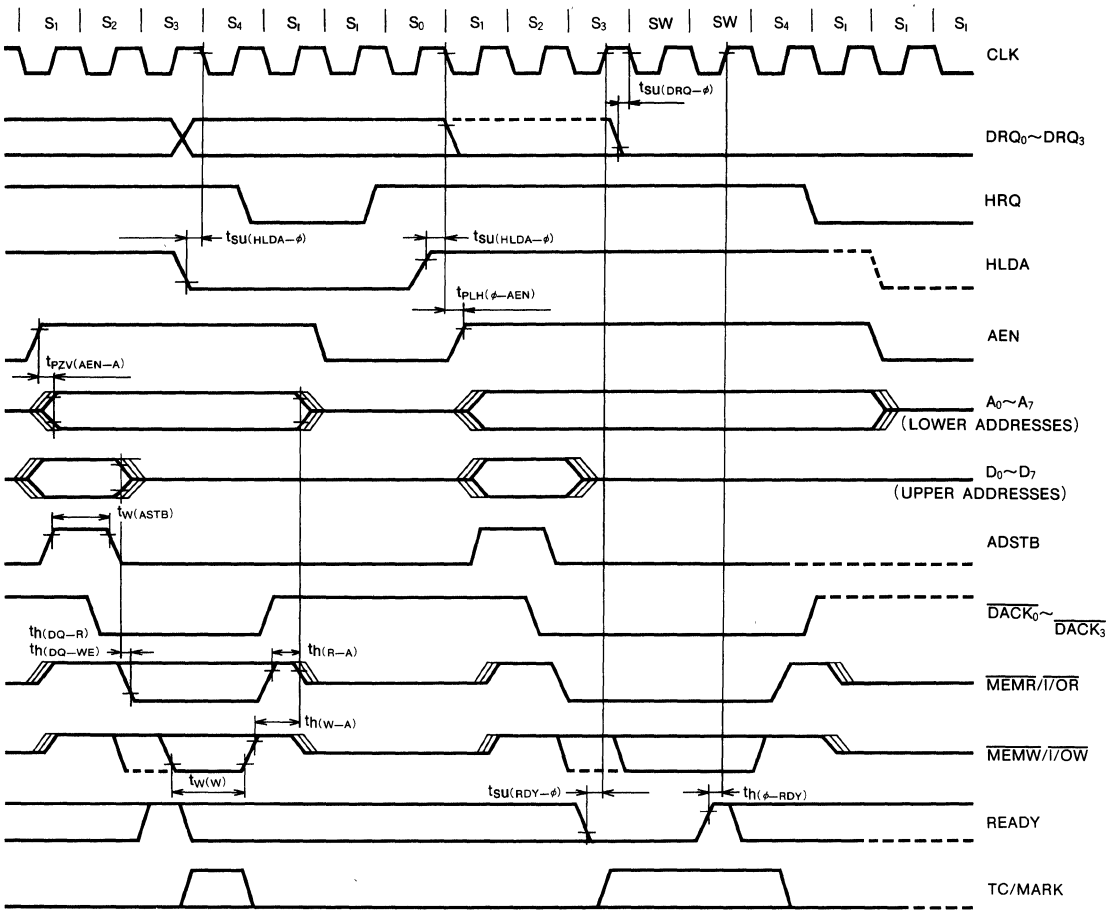
Slave Mode

Read

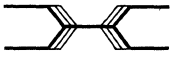


Write





Note 9 :



The center line indicates a floating (high-impedance) state.

M5L8259AP

PROGRAMMABLE INTERRUPT CONTROLLER

DESCRIPTION

The M5L8259AP is a programmable LSI for interrupt control. It is fabricated using N-channel silicon-gate ED-MOS technology and is designed to be used easily in connection with an MELPS85, MELPS86 or MELPS88.

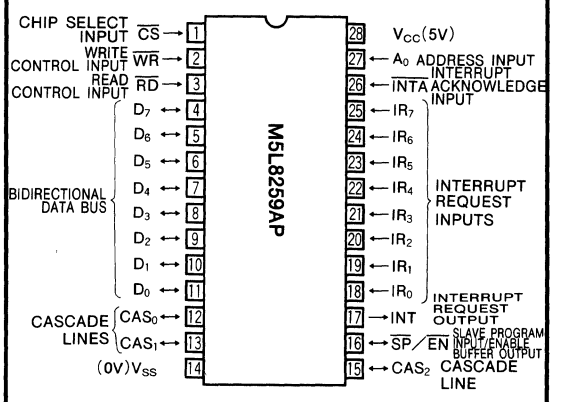
FEATURES

- Single 5V supply voltage
- TTL compatible
- CALL instruction to the CPU is generated automatically
- Priority, interrupt mask and vectored address for each interrupt request input are programmable
- Up to 64 levels of interrupt requests can be controlled by cascading with M5L8259AP
- Polling functions

APPLICATION

The M5L8259AP can be used as an interrupt controller for MELPS85, MELPS86 and MELPS88.

PIN CONFIGURATION (TOP VIEW)



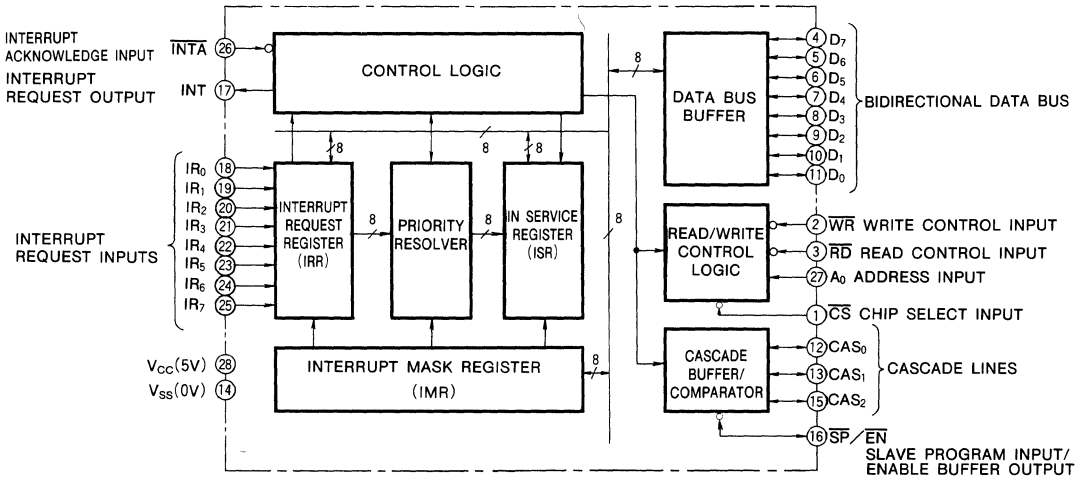
Outline 28P4

FUNCTION

The M5L8259AP is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight level requests and has built-in features for expandability to other M5L8259APs. The priority and interrupt mask can be changed or reconfigured at any time by the main program

When an interrupt is generated because of an interrupt request at 1 of the pins, the M5L8259AP based on the mask and priority will output an INT to the CPU. After that, when an $\overline{INTA}$ signal is received from the CPU or the system controller, a CALL instruction and a programmed vector address is released onto the data bus.

BLOCK DIAGRAM



PIN DESCRIPTION

Symbol	Pin name	Input or output	Functional significance
$\overline{CS}$	Chip select input	Input	This input is active at low-level, but may be at high-level during interrupt request input and interrupt processing
$\overline{WR}$	Write control input	Input	Command write control input from the CPU
$\overline{RD}$	Read control input	Input	Data read control input for the CPU
$D_7 \sim D_0$	Bidirectional data bus	Input/ output	Data and commands are transmitted through this bidirectional data bus to and from the CPU
$CAS_2 \sim CAS_0$	Cascade lines	Input/ output	These pins are outputs for a master and inputs for a slave And these pins of the master will be able to address each individual slave The master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of $\overline{INTA}$
$\overline{SP}/\overline{EN}$	Slave program input/ Enable buffer output	Input/ output	SP In normal mode, a master is designated when $\overline{SP}/\overline{EN}$="H" and a slave is designated when $\overline{SP}/\overline{EN}$="L" EN In the buffered mode, whenever the M5L8259AP's data bus output is enabled, its $\overline{SP}/\overline{EN}$ pin will go low-level
INT	Interrupt request output	Output	This pin goes high-level whenever a valid interrupt is asserted
$IR_7 \sim IR_0$	Interrupt request input	Input	The asynchronous interrupt inputs are active at high-level The interrupt mask and priority of each interrupt input can be changed at any time When using edge triggered mode, the rising edge (low-level to high-level) of the interrupt request and the high-level must be held until the first $\overline{INTA}$ For level triggered mode, the high-level must be held until the first $\overline{INTA}$
$\overline{INTA}$	Interrupt acknowledge input	Input	When an interrupt acknowledge ($\overline{INTA}$) from the CPU is received, the M5L8259AP releases a CALL instruction or vectored address onto the data bus
A_0	A_0 address input	Input	This pin is normally connected to one of the address lines and acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ when writing commands or reading status registers

OPERATION

The M5L8259AP is interfaced with a standard system bus as shown in Fig. 1 and operates as an interrupt controller.

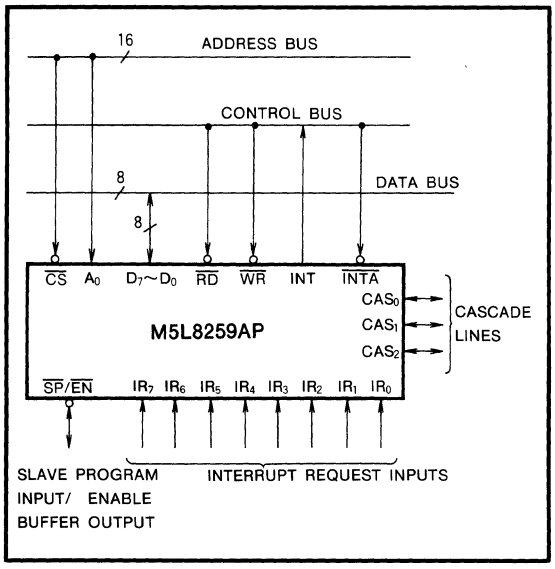


Fig. 1 The M5L8259AP interfaces to standard system bus.

Table 1 M5L8259AP basic operation

A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input operation (read)
0			L	H	L	IRR, ISR or interrupting level→data bus
1			L	H	L	IMR→Data bus
						Output operation (write)
0	0	0	H	L	L	Data bus→OCW2
0	0	1	H	L	L	Data bus→OCW3
0	1	X	H	L	L	Data bus→ICW1
1	X	X	H	L	L	Data bus→OCW1, ICW2, ICW3, ICW4
						Disable function
X	X	X	H	H	L	Data bus→High-impedance
X	X	X	X	X	H	Data bus→High-impedance

Interrupt Sequence

1. When the CPU is a MELPS85

(1) When one or more of the interrupt request inputs are raised high-level, the corresponding IRR bit(s) for the high-level inputs will be set

(2) Mask state and priority levels are considered and, if appropriate, the M5L8259AP sends an INT signal to the CPU.

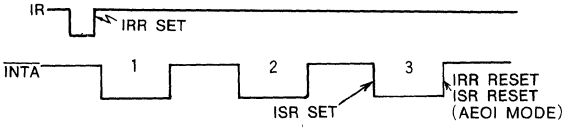
(3) The acknowledgement of the CPU to the INT signal, the CPU issues an $\overline{INTA}$ pulse to the M5L8259AP.

(4) Upon receiving the first $\overline{INTA}$ pulse from the CPU, a CALL instruction is released onto the data bus.

(5) A CALL is a 3-byte instruction, so additional two $\overline{INTA}$ pulses are issued to the M5L8259AP from the CPU.

(6) These two $\overline{INTA}$ pulses allow the M5L8259AP to release the program address onto the data bus. The low-order 8 bits vectored address is released at the second $\overline{INTA}$ pulse and the high-order 8 bits vectored address is released at the third $\overline{INTA}$ pulse. The ISR bit corresponding to the interrupt request input is set upon receiving the third $\overline{INTA}$ pulse from the CPU, and the corresponding IRR bit is reset.

(7) This completes the 3-byte CALL instruction and the interrupt routine will be serviced. The ISR bit is reset at the trailing edge of the third $\overline{INTA}$ pulse in the AEOI mode In the other modes the ISR bit is not reset until an EOI command is issued.



2. When the CPU is a MELPS86 or MELPS88

(1) When one or more of the interrupt request inputs are raised high-level, the corresponding IRR bit(s) for the high-level inputs will be set.

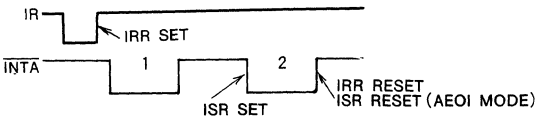
(2) Mask state and priority levels are considered and if appropriated, the M5L8259AP sends an INT signal to the CPU.

(3) As an acknowledgement to the INT signal, the CPU issues an $\overline{INTA}$ pulse to the M5L8259AP.

(4) Upon receiving the first $\overline{INTA}$ pulse from the CPU, the M5L8259AP does not drive the data bus, and the data bus keeps high-impedance state.

(5) When the second $\overline{INTA}$ pulse is issued from the CPU, an 8-bit pointer is released onto the data bus.

(6) This completes the interrupt cycle and the interrupt routine will be serviced. The ISR bit is reset at the trailing edge of the second $\overline{INTA}$ pulse in the AEOI mode. In the other modes the ISR bit is not reset until an EOI command is issued from the CPU.



The interrupt request input must be held at high-level until the first $\overline{INTA}$ pulse is issued. If it is allowed to return to low-level before the first $\overline{INTA}$ pulse is issued, an interrupt request in IR_7 is executed. However, in this case the ISR bit is not set.

This is a function for a noise countermeasure of interrupt request inputs. In the interrupt routine of IR_7, if ISR is checked by software either the interrupt by noise or real interrupt can be acknowledged. In the state of edge trigger mode normally the interrupt request inputs hold high-level and its input low-level pulse in the case of interrupt

Interrupt sequence outputs

1. When the CPU is a MELPS85

A CALL instruction is released onto the data bus when the first $\overline{INTA}$ pulse is issued. The low-order 8 bits of the vectored address are released when the second $\overline{INTA}$ pulse is issued, and the high-order 8 bits are released when the third $\overline{INTA}$ pulse is issued. The format of these three outputs is shown in Table 2.

Table 2 Formats of interrupt CALL instruction and vectored address

First $\overline{INTA}$ pulse (CALL instruction)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	1	1	0	1

Second $\overline{INTA}$ pulse (low-order 8 bits of vectored address)

IR	Interval = 4							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_0	A_7	A_6	A_5	0	0	0	0	0
IR_1	A_7	A_6	A_5	0	0	1	0	0
IR_2	A_7	A_6	A_5	0	1	0	0	0
IR_3	A_7	A_6	A_5	0	1	1	0	0
IR_4	A_7	A_6	A_5	1	0	0	0	0
IR_5	A_7	A_6	A_5	1	0	1	0	0
IR_6	A_7	A_6	A_5	1	1	0	0	0
IR_7	A_7	A_6	A_5	1	1	1	0	0

IR	Interval=8							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_0	A_7	A_6	0	0	0	0	0	0
IR_1	A_7	A_6	0	0	1	0	0	0
IR_2	A_7	A_6	0	1	0	0	0	0
IR_3	A_7	A_6	0	1	1	0	0	0
IR_4	A_7	A_6	1	0	0	0	0	0
IR_5	A_7	A_6	1	0	1	0	0	0
IR_6	A_7	A_6	1	1	0	0	0	0
IR_7	A_7	A_6	1	1	1	0	0	0

Third $\overline{INTA}$ pulse (high-order 8 bits of vectored address)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8

2. When the CPU is a MELPS86 or MELPS88

The data bus keeps a high-impedance state when the first $\overline{INTA}$ pulse is issued. Then the pointer $T_7 \sim T_0$ is released when the next $\overline{INTA}$ pulse is issued. The content of the pointer $T_7 \sim T_0$ is shown in Table 3. The $T_2 \sim T_0$ are a binary code corresponding to the interrupt request level, $A_{10} \sim A_5$ are unused and ADI mode control is ignored.

Table 3 Contents of interrupt pointer

Second $\overline{INTA}$ pulse (8-bit pointer)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_0	T_7	T_6	T_5	T_4	T_3	0	0	0
IR_1	T_7	T_6	T_5	T_4	T_3	0	0	1
IR_2	T_7	T_6	T_5	T_4	T_3	0	1	0
IR_3	T_7	T_6	T_5	T_4	T_3	0	1	1
IR_4	T_7	T_6	T_5	T_4	T_3	1	0	0
IR_5	T_7	T_6	T_5	T_4	T_3	1	0	1
IR_6	T_7	T_6	T_5	T_4	T_3	1	1	0
IR_7	T_7	T_6	T_5	T_4	T_3	1	1	1

Interrupt Request Register (IRR), In-service Register (ISR)

As interrpt requests are received at inputs $IR_7 \sim IR_0$, the corresponding bits of IRR are set and as an interrupt request is serviced the corresponding bit of ISR is set. The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are being serviced. The status of these two registers can be read. These two registers are connected through the priority resolver.

An interrupt requst received by IR_n is acknowledged on the leading edge when in the edge triggered mode or it is acknowledged on the level when in the level triggered mode. After that an INT signal is released and the interrupt request signal is latched in the corresponding IRR bit if the high-level is held until the first $\overline{INTA}$ pulse is issued. It is important to remember that the interrupt request signal must be held at high-level until the first $\overline{INTA}$ pulse is issued.

The interrupt request latching in the IRR causes a signal to be sent to the priority resolver unless it is masked out. When the priority resolver receives the signals it selects the highest priority interrupt request latched in IRR. The ISR is set when the last $\overline{INTA}$ pulse is issued while the corresponding bit of IRR is reset and the other bits of IRR are unaffected.

The bit of ISR that was set is not reset during the interrupt routine, but is reset at the end of the routine by the EOI command (end of interrupt) or by the trailing edge of the last $\overline{INTA}$ pulse in AEOI mode.

Priority Resolver

The priority resolver examines all of the interrupt requests set in IRR to determine and selects the highest priority. The ISR bit corresponding to the selected (highest priority) request is set by the last $\overline{INTA}$ pulse.

Interrupt Mask Register (IMR)

The contents of the interrupt mask register are used to mask out (disable) interrupt requests of selected interrupt request pins Each terminal is independently masked so that masking a high priority interrupt does not influence the lower or higher priority interrupts. Therefore the contents of IMR selectively enable reading.

Interrupt Request Output (INT)

The interrupt request output connects directly to the interrupt input of the CPU.The output level is compatible with the input level required for the CPUs.

The INT output is set to low-level after the interrupt sequence ends, irrespective of the current mode. When the power is turned on, the INT output (high-level output) may appear but is reset to low-level by executing ICW 1 .

Interrupt Acknowledge Input ($\overline{INTA}$)

The CALL instruction and vectored address are released onto the data bus by the $\overline{INTA}$ pulse.

Data Bus Buffer

The data bus buffer is a 3-state bidirectional data bus buffer that is used to interface with the system bus. Write commands to the M5L8259AP, CALL instructions, vectored addresses, status information, etc. are transferred through the data bus buffer.

Read/Write Control Logic

The read/write control logic is used to control functions such as receiving commands from the CPU and supplying status information to the data bus.

Chip Select Input ($\overline{CS}$)

The M5L8259AP is selected (enabled) when $\overline{CS}$ is at low-level, but during interrupt request input or interrupt processing it may be high-level.

Write Control Input ($\overline{WR}$)

When $\overline{WR}$ goes to low-level the M5L8259AP can be written.

Read Control Input ($\overline{RD}$)
When $\overline{RD}$ goes low-level status information in the internal register of the M5L8259AP can be read through the data bus.

Address Input (A_0)
The address input is normally connected with one of the address lines and is used along with $\overline{WR}$ and $\overline{RD}$ to control write commands and reading status information.

Cascade Buffer/Comparator
The cascade buffer/comparator stores or compares identification codes. The three cascade lines are output when the M5L8259AP is a master or input when it is a slave. The identification code on the cascade lines select it as master or slave.

PROGRAMMING THE M5L8259AP

The M5L8259AP is programmed through the Initialization Command Word (ICW) and the operation command word (OCW). The following explains the functions of these two commands.

Initialization Command Words (ICW_S)
The initialization command word is used for the initial setting of the M5L8259AP. There are four commands in this group and the following explains the details of these four commands. The command flow of ICWs is shown Fig. 2.

ICW1
The meaning of the bits of ICW1 is explained in Fig. 3 along with the functions. ICW1 contains vectored address bits A_7~A_5, a flag indicating whether interrupt input is edge triggered or level triggered, CALL address interval, whether a single M5L8259AP or the cascade mode is used, and whether ICW4 is required or not.

Whenever a command is issued with A_0=0 and D_4=1, this is interpreted as ICW1 and the following will automatically occur.

(a) The interrupt mask register (IMR) is cleared.
(b) The interrupt request input IR_7 is assigned the lowest priority.
(c) The special mask mode is cleared and the status read is set to the interrupt request register (IRR).
(d) When IC4=0 all bits in ICW4 are set to 0.

ICW2
ICW2 contains vectored address bits A_{15} ~ A_8 or interrupt type T_7~T_3, and the format is shown in Fig. 3.

ICW3
When SNGL=1 it indicates that only a single M5L8259AP is used in the system, in which case ICW3 is not valid. When SNGL=0, ICW3 is valid and indicates cascade connections with other M5L8259AP devices. In the master mode, a 1 is set for each slave.

When the CPU is a MELPS85 the CALL instruction is released from the master at the first $\overline{INTA}$ pulse and the vectored address is released onto the data bus from the slave at the second and third $\overline{INTA}$ pulses.

When the CPU is a MELPS86 the master and slave are in high-impedance at the first $\overline{INTA}$ pulse and the pointer is released onto the data bus from the slave at the second $\overline{INTA}$ pulse.

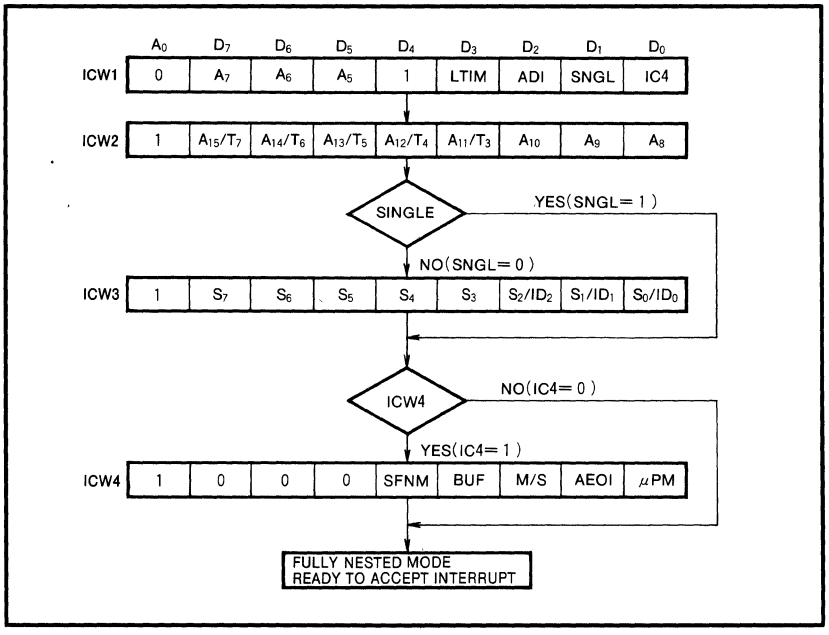


Fig. 2 Initialization sequence

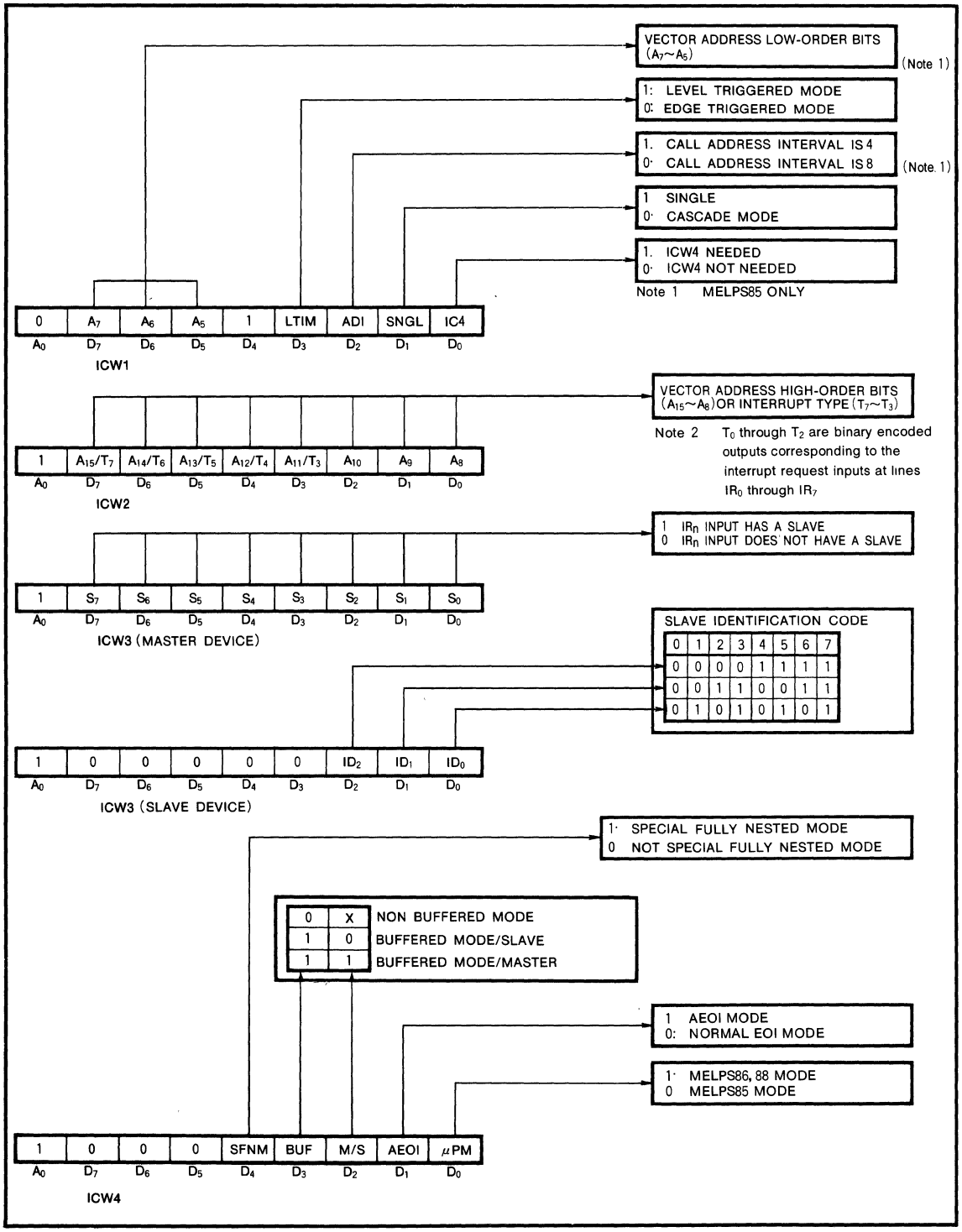


Fig. 3 Initialization command word format

The master mode is specified when $\overline{SP}/\overline{EN}$ pin is high-level or BUF=1 and M/S=1 in ICW4, and slave mode is specified when $\overline{SP}/\overline{EN}$ pin is low-level or BUF = 1 and M/S = 0 in ICW4. In the slave mode, three bits $ID_2 \sim ID_0$ identify the slave. And then when the slave code released on the cascade lines from the master, matches the assigned ID code, the vectored address is released by it onto the data bus at the next $\overline{INTA}$ pulse.

ICW4

Only when IC4=1 in ICW1 is ICW4 valid. Otherwise all bits are set to 0. When ICW4 is valid it specifies special fully nested mode, buffer mode, master/slave, automatic EOI and microprocessor mode The format of ICW4 is shown in Fig. 3.

Operation Command Words (OCW_S)

The operation command words are used to change the contents of IMR, the priority of interrupt request inputs and the special mask. After the ICW are programmed into the M5L8259AP, the device is ready to accept interrupt requests. There are three types of OCW_S; explanation of each follows, and the format of OCW_S is shown in Fig. 4.

OCW1

The meaning of the bits of OCW1 are explained in Fig. 4 along with their functions. Each bit of IMR can be independently changed (set or reset) by OCW1.

OCW2

The OCW2 is used for issuing EOI commands to the M5L8259AP and for changing the priority of the interrupt re-

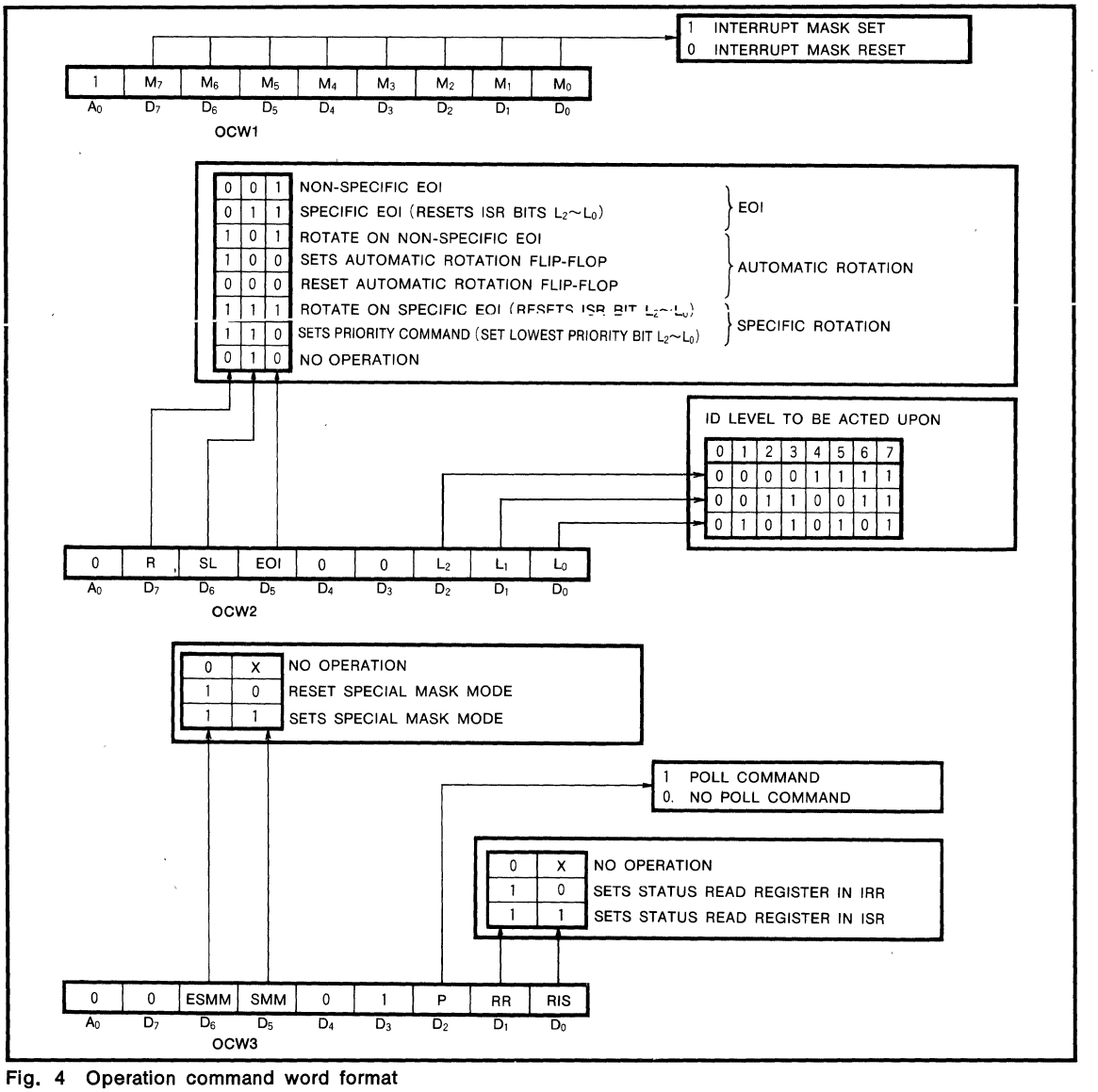


Fig. 4 Operation command word format

quest inputs.

OCW3

The OCW3 is used for specifying special mask mode, poll mode and status register read.

FUNCTION OF COMMAND

Interrupt masks

The mask register contains a mask for each individual interrupt request. These interrupt masks can be changed by programming using OCW1.

Special mask mode

When an interrupt request is acknowledged and the ISR bit corresponding to the interrupt request is not reset by EOI command (which means an interrupt service routine is executing) lower priority interrupt requests are ignored.

In special mask mode interrupt requests received at interrupt request inputs which are masked by OCW1 are disabled, but interrupts at all levels that are not masked are possible. This means that in the mask mode all level of interrupts are possible or individual inputs can be selectively programmed so all interrupts at the selected inputs are disabled. The masks are stored in IMR and special mask is set/reset by executing OCW3.

Buffered mode

The buffered mode will structure the M5L8259AP to send an enable signal on $\overline{SP}/\overline{EN}$ to enable the data bus buffer, when the data bus requires the data bus buffer or when cascading mode is used. In this mode, when data bus output of the M5L8259AP is enabled, the $\overline{SP}/\overline{EN}$ output becomes low-level. This allows the M5L8259AP to be programmed whether it is a master or a slave by software. The buffered mode is set/reset by executing ICW4.

Fully nested mode

The fully nested mode is the mode when no mode is specified and is the usual operational mode. In this mode, the priority of interrupt request terminals is fixed from the lowest IR_7 to the highest IR_0. When an interrupt request is acknowledged the CALL instruction and vectored address are released onto the data bus. At the same time the ISR bit corresponding to the accepted interrupt request is set. This ISR bit remains set until it is reset by the input of an EOI command or until the trailing edge of last $\overline{INTA}$ pulse in AEOI mode. While an interrupt service routine is being executed, interrupt requests of same or lower priority are disabled while the bit of ISR remains set. The priorities can be changed by OCW2.

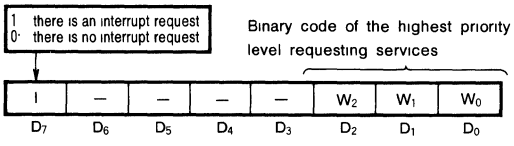
Special fully nested mode

The special fully nested mode will be used when cascading is used and this mode will be programmed to the master by ICW4. The special fully nested mode is the same as the fully nested mode with the following two exceptions.

1. When an interrupt from a certain slave is being serviced, this slave is not locked out from the master priority logic. Higher priority interrupts within the slave will be recognized by the master and the master will initiate an interrupt request to the CPU. In general in the normal fully nested mode, a serviced slave is locked out from the master's priority, and so higher priority interrupts from the same slave are not serviced.
2. When an interrupt from a certain slave is being serviced the software must check ISR to determine if there are additional interrupts requests to be serviced. If the ISR bit is 0 the EOI command may be sent to the master too. But if it is not 0 the EOI command should not be sent to the master.

Poll mode

The poll mode is useful when the internal enable flip-flop of the microprocessor is reset, and interrupt input is disabled. Service to the device is achieved by a programmer initiative using a poll command. In the poll mode the M5L8259AP at the next $\overline{RD}$ pulse puts 8-bit on the data bus which indicates whether there is an interrupt request and reads the priority level. The format of the information on the data bus is as shown below.



When I=0 (no interrupt request), $W_2 \sim W_0$ is 111. The poll is valid from $\overline{WR}$ to $\overline{RD}$ and interrupt is frozen. This mode can be used for processing common service routines for interrupts from more than one line and does not require any $\overline{INTA}$ sequence. Poll command is issued by setting P=1 in OCW3.

End Of Interrupt (EOI) and Specific EOI (SEOI)

An EOI command is required by the M5L8259AP to reset the ISR bit. So an EOI command must be issued to the M5L8259AP before returning from an interrupt service routine.

When AEOI is selected in ICW4, the ISR bit can be reset at the trailing edge of the last $\overline{INTA}$ pulse. When AEOI is not selected the ISR bit is reset by the EOI command issued to the M5L8259AP before returning from an interrupt service routine. When programmed in the cascade mode the EOI command must be issued to the master once and to corresponding slave once.

There are two forms of EOI command, specific EOI and non-specific EOI. When the M5L8259AP is used in the fully nested mode, the ISR bit being serviced is reset by the EOI command. When the non-specific EOI is issued the M5L8259AP will automatically reset the highest ISR bit of those that are set. Other ISR bits are reset by a specific EOI and the bit to be reset is specified in the EOI by the program. The SEOI is useful in modes other than fully nested

mode. When the M5L8259AP is in special mask mode ISR bits masked in IMR are not reset by EOI. EOI and SEOI are selected when OCW2 is executed.

Automatic EOI (AEOI)

In the AEOI mode the M5L8259AP executes non-specific EOI command automatically at the trailing edge of the last $\overline{INTA}$ pulse. When AEOI=1 in ICW4, the M5L8259AP is put in AEOI mode continuously until reprogrammed in ICW4.

The AEOI mode can only be used in a master M5L8259AP and not a slave.

Automatic rotation

The automatic rotation mode is used in applications where many interrupt requests of the same level are expected such as multichannel communication systems. In this mode when an interrupt request is serviced, that request is assigned the lowest priority so that if there are other interrupt requests they will have higher priorities. This means that the next request on the interrupt request being serviced must wait until the other interrupt requests are serviced (worst case is waiting for all 7 of the other controllers to be serviced). The priority and serving status are rotated as shown in Fig. 5.

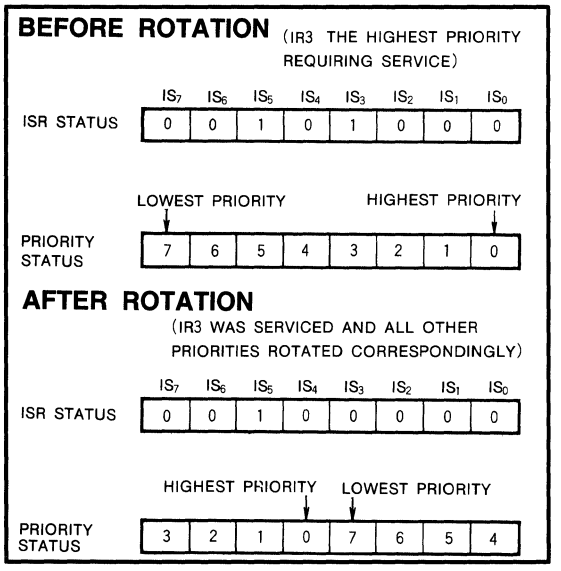


Fig. 5 An example of priority rotation

In the non-specific EOI command automatic rotation mode is selected when R=1, EOI=1, SL=0 in OCW2. The internal priority status is changed by EOI or AEOI commands. The rotation priority A flip-flop is set by R=1, EOI=0 and SL=0 which is useful when the M5L8259AP is used in the AEOI mode.

Specific rotation

Specific rotation gives the user versatile capabilities in interrupt controlled operations. It serves in those applications in which a specific device's interrupt priority must be altered. As opposed to automatic rotation which automatically sets priorities, specific rotation is completely user controlled. That is, the user selects the interrupt level that is to receive lowest or highest priority. Priority changes can be executed during an EOI command.

Level triggered mode/Edge triggered mode

Selection of level or edge triggered mode of the M5L8259AP is made by ICW1, When using edge triggered mode not only is a transition from low-level to high-level required, but the high-level must be held until the first $\overline{INTA}$. If the high-level is not held until the first $\overline{INTA}$, the interrupt request will be treated as if it were input on IR_7, except that the ISR bit is not set. When level triggered mode is used the functions are the same as edge triggered mode except that the transition from low-level to high-level is not required to trigger the interrrupt request.

In the level triggered mode and using AEOI mode together, if the high-level is held too long the interrupt will occur immediately. To avoid this situation interrupts should be kept disabled until the end of the service routine or until the IR input returns low-level. In the edge triggered mode this type of mistake is not possible because the interrupt request is edge triggered.

Reading the M5L8259AP internal status

The contents of IRR and ISR can be read by the CPU with status read. When an OCW3 is issued to the M5L8259AP and an $\overline{RD}$ pulse issued the contents of IRR or ISR can be released onto the data bus. A special command is not required to read the contents of IMR. The contents of IMR can be released onto the data bus by issuing an $\overline{RD}$ pulse when A_0=1. There is no need to issue a read register command every time the IRR or ISR is to be read. Once a read register command is received by the M5L8259AP, it remains valid until it is changed. Remember that the programmer must issue a poll command every time to check whether there is an interrupt request and read the priority level. Polling overrides status read when P=1, RR=1 in OCW3.

CASCADING

The M5L8259AP can be interconnected in a system of one master with up to 8 slaves to handle up to 64 priority levels. A system of 3 units that can be used with the MELPS85 is shown in Fig. 6.

The master can select a slave by outputting its identification code through the 3 cascade lines. The INT output of each slave is connected to the master interrupt request inputs. When an interrupt request of one of the slaves is to be serviced the master outputs the identification code of the slave through the cascade lines, so the slave will release the vectored address on the next $\overline{INTA}$ pulse.

The cascade lines of the master are nomally low-level, and will contain the slave identification code from the leading edge of the first $\overline{INTA}$ pulse to the trailing edge of the last

$\overline{INTA}$ pulse. The master and slave can be programmed to work in different modes. ICWs must be issued for each device, and EOI commands must be issued twice: once for the master and once for the corresponding slave. Each $\overline{CS}$ of the M5L8259AP requires an address decoder.

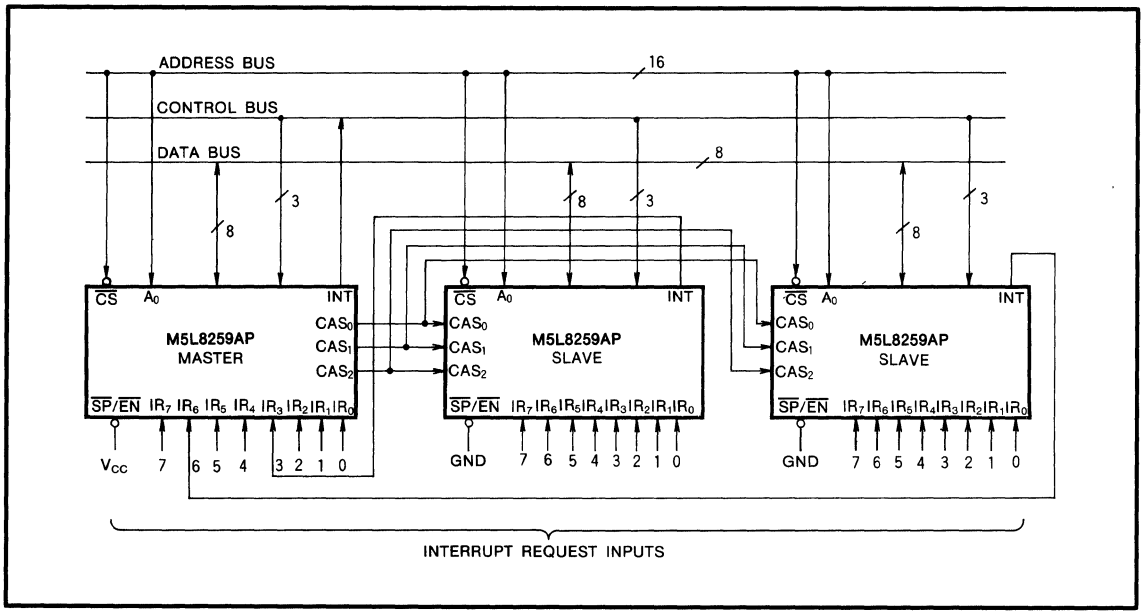
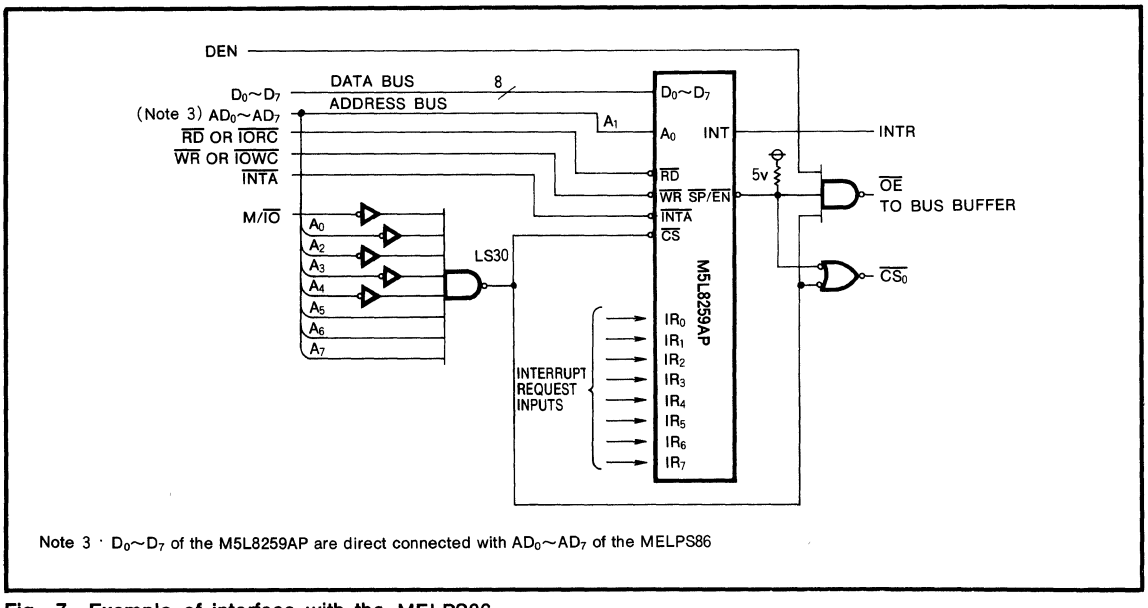


Fig. 6 Cascading the M5L8259AP



Note 3 : $D_0 \sim D_7$ of the M5L8259AP are direct connected with $AD_0 \sim AD_7$ of the MELPS86

Fig. 7 Example of interface with the MELPS86

INSTRUCTION SET

Item / Number	Mnemonic	Instruction code									Function			
		A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	ICW4 required?	Interval	Single	Trigger
1	ICW1 A	0	A_7	A_6	A_5	1	0	1	1	0	N	4	Y	E
2	ICW1 B	0	A_7	A_6	A_5	1	1	1	1	0	N	4	Y	L
3	ICW1 C	0	A_7	A_6	A_5	1	0	1	0	0	N	4	N	E
4	ICW1 D	0	A_7	A_6	A_5	1	1	1	0	0	N	4	N	L
5	ICW1 E	0	A_7	A_6	0	1	0	0	1	0	N	8	Y	E
6	ICW1 F	0	A_7	A_6	0	1	1	0	1	0	N	8	Y	L
7	ICW1 G	0	A_7	A_6	0	1	0	0	0	0	N	8	N	E
8	ICW1 H	0	A_7	A_6	0	1	1	0	0	0	N	8	N	L
9	ICW1 I	0	A_7	A_6	A_5	1	0	1	1	1	Y	4	Y	E
10	ICW1 J	0	A_7	A_6	A_5	1	1	1	1	1	Y	4	Y	L
11	ICW1 K	0	A_7	A_6	A_5	1	0	1	0	1	Y	4	N	E
12	ICW1 L	0	A_7	A_6	A_5	1	1	1	0	1	Y	4	N	L
13	ICW1 M	0	A_7	A_6	0	1	0	0	1	1	Y	8	Y	E
14	ICW1 N	0	A_7	A_6	0	1	1	0	1	1	Y	8	Y	L
15	ICW1 O	0	A_7	A_6	0	1	0	0	0	1	Y	8	N	E
16	ICW1 P	0	A_7	A_6	0	1	1	0	0	1	Y	8	N	L
17	ICW2	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	8-bit vectored address			
18	ICW3 M	1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	Slave connections (master mode)			
19	ICW3 S	1	0	0	0	0	0	ID_2	ID_1	ID_0	Slave identification code (slave mode)			
											SFNM	BUF	AEOI	MELPS86
20	ICW4 A	1	0	0	0	0	0	0	0	0	N	N	N	N
21	ICW4 B	1	0	0	0	0	0	0	0	1	N	N	N	Y
22	ICW4 C	1	0	0	0	0	0	0	1	0	N	N	Y	N
23	ICW4 D	1	0	0	0	0	0	0	1	1	N	N	Y	Y
24	ICW4 E	1	0	0	0	0	0	1	0	0	N	N	N	N
25	ICW4 F	1	0	0	0	0	0	1	0	1	N	N	N	Y
26	ICW4 G	1	0	0	0	0	0	1	1	0	N	N	Y	N
27	ICW4 H	1	0	0	0	0	0	1	1	1	N	N	Y	Y
28	ICW4 I	1	0	0	0	0	1	0	0	0	N	Y S	N	N
29	ICW4 J	1	0	0	0	0	1	0	0	1	N	Y S	N	Y
30	ICW4 K	1	0	0	0	0	1	0	1	0	N	Y S	Y	N
31	ICW4 L	1	0	0	0	0	1	0	1	1	N	Y S	Y	Y
32	ICW4 M	1	0	0	0	0	1	1	0	0	N	Y M	N	N
33	ICW4 N	1	0	0	0	0	1	1	0	1	N	Y M	N	Y
34	ICW4 O	1	0	0	0	0	1	1	1	0	N	Y M	Y	N
35	ICW4 P	1	0	0	0	0	1	1	1	1	N	Y M	Y	Y
36	ICW4 NA	1	0	0	0	1	0	0	0	0	Y	N	N	N
37	ICW4 NB	1	0	0	0	1	0	0	0	1	Y	N	N	Y
38	ICW4 NC	1	0	0	0	1	0	0	1	0	Y	N	Y	N
39	ICW4 ND	1	0	0	0	1	0	0	1	1	Y	N	Y	Y
40	ICW4 NE	1	0	0	0	1	0	1	0	0	Y	N	N	N
41	ICW4 NF	1	0	0	0	1	0	1	0	1	Y	N	N	Y
42	ICW4 NG	1	0	0	0	1	0	1	1	0	Y	N	Y	N
43	ICW4 NH	1	0	0	0	1	0	1	1	1	Y	N	Y	Y
44	ICW4 NI	1	0	0	0	1	1	0	0	0	Y	Y S	N	N
45	ICW4 NJ	1	0	0	0	1	1	0	0	1	Y	Y S	N	Y
46	ICW4 NK	1	0	0	0	1	1	0	1	0	Y	Y S	Y	N
47	ICW4 NL	1	0	0	0	1	1	0	1	1	Y	Y S	Y	Y
48	ICW4 NM	1	0	0	0	1	1	1	0	0	Y	Y M	N	N
49	ICW4 NN	1	0	0	0	1	1	1	0	1	Y	Y M	N	Y
50	ICW4 NO	1	0	0	0	1	1	1	1	0	Y	Y M	Y	N
51	ICW4 NP	1	0	0	0	1	1	1	1	1	Y	Y M	Y	Y
52	OCW1	1	M_7	M_6	M_5	M_4	M_3	M_2	M_1	M_0	Interrupt mask			
53	OCW2 E	0	0	0	1	0	0	0	0	0	EOI			
54	OCW2 SE	0	0	1	1	0	0	L_2	L_1	L_0	SEOI			
55	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate on Non-Specific EOI command (Automatic rotation)			
56	OCW2 RSE	0	1	1	1	0	0	L_2	L_1	L_0	Rotate on Specific EOI command (Specific rotation)			
57	OCW2 R	0	1	0	0	0	0	0	0	0	Rotate in AEOI Mode (SET)			
58	OCW2 CR	0	0	0	0	0	0	0	0	0	Rotate in AEOI Mode (CLEAR)			
59	OCW2 RS	0	1	1	0	0	0	L_2	L_1	L_0	Set priority without EOI			
60	OCW3 P	0	0	0	0	0	1	1	0	0	Poll mode			
61	OCW3 RIS	0	0	0	0	0	1	0	1	1	Sets Status Read Resister in ISR			
62	OCW3 RR	0	0	0	0	0	1	0	1	0	Sets Status Read Resister in IRR			
63	OCW3 SM	0	0	1	1	0	1	0	0	0	Sets Special Mask mode			
64	OCW3 RSM	0	0	1	0	0	1	0	0	0	Reset Special Mask mode			

Note 4 : Y: yes, N: no, E: edge, L: level, M: master, S: slave

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
P_d	Power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating free-air temperature range		−20～75	℃
T_{stg}	Storage temper ature range		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20～75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.5	V
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
$V_{OH(INT)}$	High-level output voltage, interrupt requset output	I_{OH}=−100μA	3.5			V
V_{OL}	Low-level output voltage	I_{OL}=2.2mA			0.45	V
I_{CC}	Supply current from V_{CC}				85	mA
I_{IH}	High-level input current	V_I=V_{CC}	−10		10	μA
I_{IL}	Low-level input current	V_I=0V	−10		10	μA
I_{OZ}	Off-state output current	V_O=0.45V～V_{CC}	−10		10	μA
I_{LIR1}	IR pin input current	V_I=0V	−300			μA
I_{LIR2}	IR pin input current	V_I=V_{CC}			10	μA
Ci	Input capacitance	V_{CC}=V_{SS}, f=1MHz, 25mVrms, T_a=25℃			10	pF
$Ci_{/O}$	Input/output capacitance	V_{CC}=V_{SS}, f=1MHz, 25mVrms, T_a=25℃			20	pF

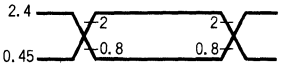
TIMING REQUIREMENTS (T_a=−20～75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(W)}$	Write pulse width		290			ns
$t_{SU(A-W)}$	Address setup time before write		0			ns
$t_{h(W-A)}$	Address hold time after write		0			ns
$t_{SU(DQ-W)}$	Data setup time before write		240			ns
$t_{h(W-DQ)}$	Data hold time after write		0			ns
$t_{W(R)}$	Read pulse width		235			ns
$t_{SU(A-R)}$	Address setup time before read		0			ns
$t_{h(R-A)}$	Address hold time after read		0			ns
$t_{W(IR)}$	Interrupt request input width, low-level time, edge triggered mode		100			ns
$t_{SU(CAS-INTA)}$	Cascade setup time after $\overline{INTA}$ (slave)		55			ns
$t_{rec(W)}$	Write recovery time		190			ns
$t_{rec(R)}$	Read recovery time		160			ns
$t_{d(RW)}$	End of command to next command (Not same command type)		500			ns
	End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence		625			ns

SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

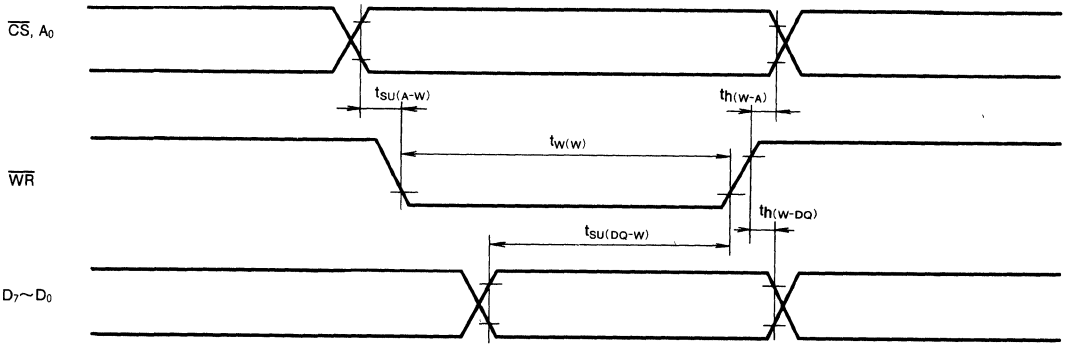
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Data output enable time after read	C_L=100pF Where $\overline{SP}/\overline{EN}$ pin is 15pF			200	ns
$t_{PVZ(R-DQ)}$	Data output disable time after read		10		100	ns
$t_{PZV(A-DQ)}$	Data output enable time after address				200	ns
$t_{PHL(R-EN)}$	Propagation time from read to enable signal output				125	ns
$t_{PLH(R-EN)}$	Propagation time from read to disable signal output				150	ns
$t_{PLH(IR-INT)}$	Propagation time from interrupt request input to interrupt request output				350	ns
$t_{PLV(INTA-CAS)}$	Propagation time from $\overline{INTA}$ to cascade output (master)				565	ns
$t_{PZV(CAS-DQ)}$	Data output enable time after cascade output (slave)				300	ns

Note 5 : $\overline{INTA}$ signal is considered read signal
$\overline{CS}$ signal is considered address signal
Input pulse level 0.45~2.4V
Input pulse rise time 20ns
Input pulse fall time 20ns
Reference level input V_{IH}=2V, V_{IL}=0.8V
output V_{OH}=2V, V_{OL}=0.8V

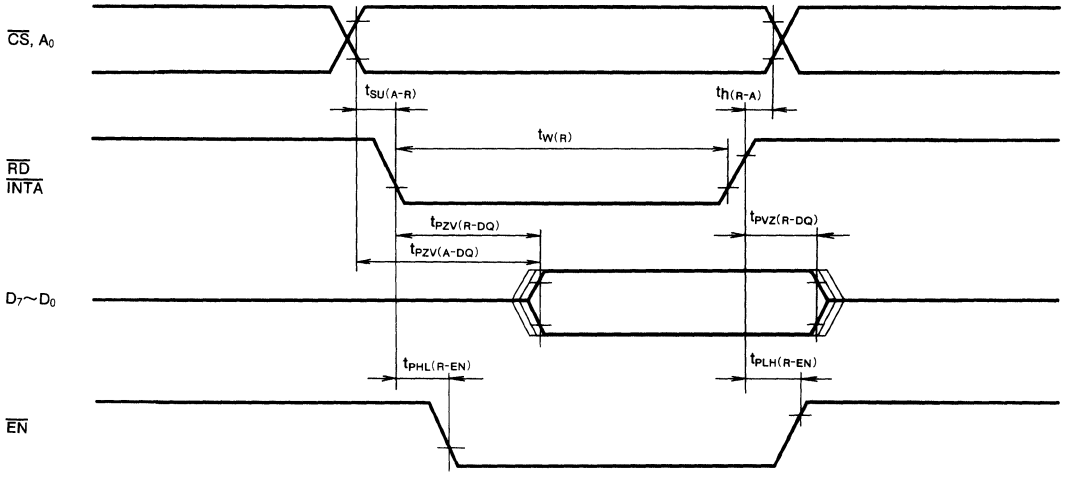


TIMING DIAGRAM

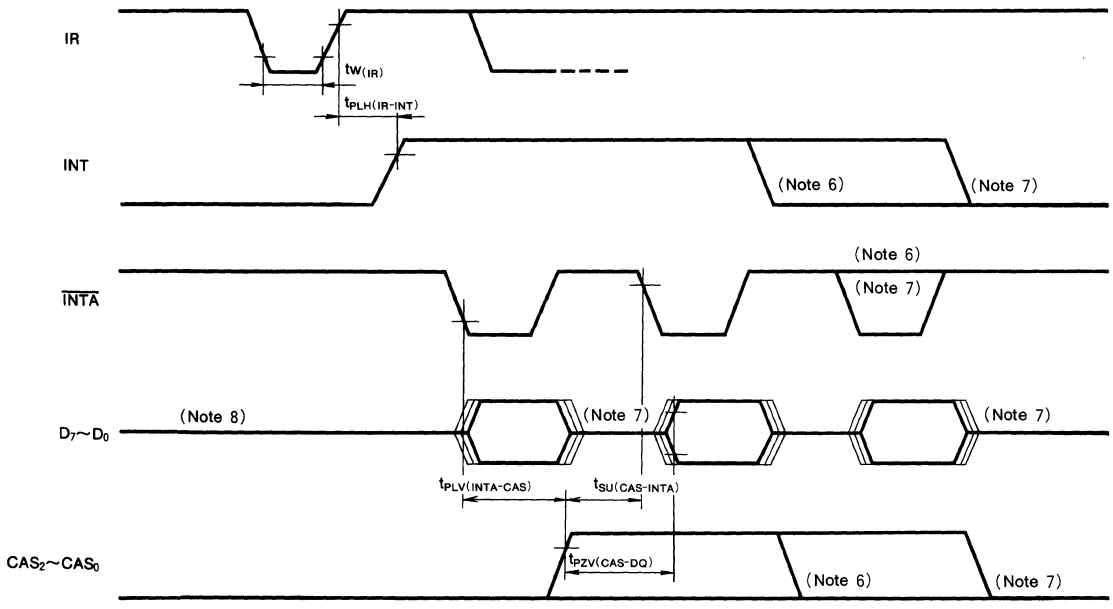
Write Mode



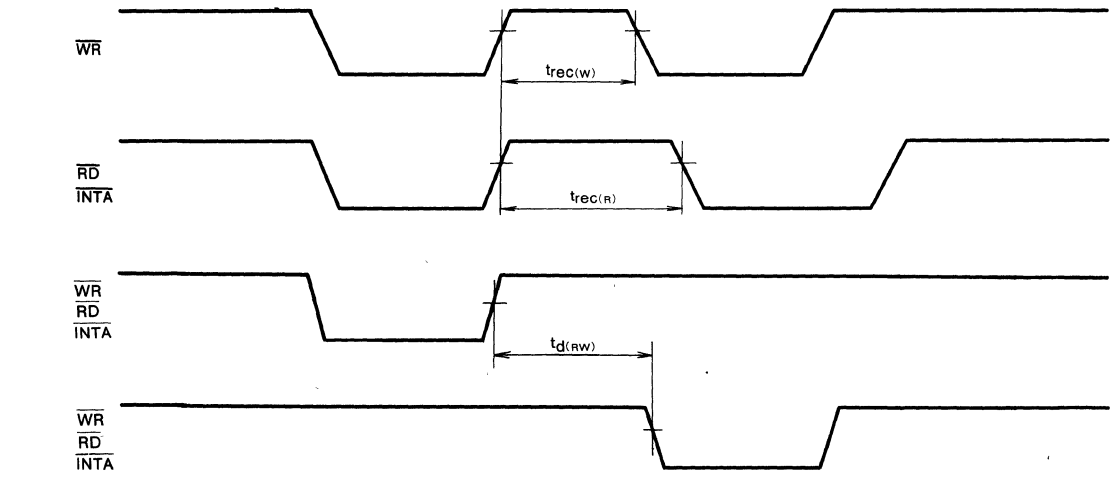
Read Mode



Interrupt Sequence



Other Timing



Note 6 : MELPS86, 88 mode
7 : MELPS85 mode
8 : MELPS86, 88 mode is in high-impedance state, pointer is released during the next $\overline{INTA}$.
When in single MELPS85 mode, data is released by all $\overline{INTA}$s When master, CALL instruction is released during the first $\overline{INTA}$, high impedance state during the second and third $\overline{INTA}$. When slave, high impedance state during the first $\overline{INTA}$, vectored address is released during the second and third $\overline{INTA}$.

M5L8279P-5

PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

DESCRIPTION

The M5L8279P-5 is a programmable keyboard and display interface device that is designed to be used in combination with an 8-bit/16-bit microprocessor. This device is fabricated with N-channel silicon-gate ED-MOS process technology and is packed in a 40-pin DIL package. It needs only single 5V power supply.

FEATURES

- Single 5V supply voltage
- TTL compatible
- Keyboard mode
- Sensor matrix mode
- Strobed mode
- Internally provided key bounce protection circuit
- Programmable debounce time
- 2-key lockout/N-key rollover
- 8-character keyboard FIFO
- Internally contained 16 × 8-bit display RAM
- Programmable right and left entry

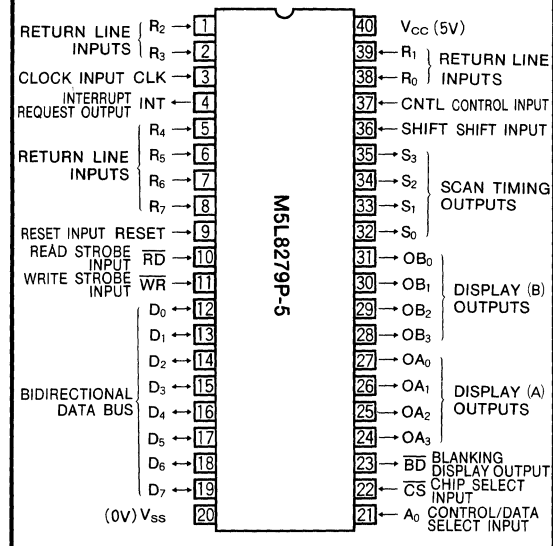
APPLICATION

Microcomputer I/O device

64 contact key input device for such items as electronic cash registers

Dual 8- or single 16-alphanumeric display

PIN CONFIGURATION (TOP VIEW)

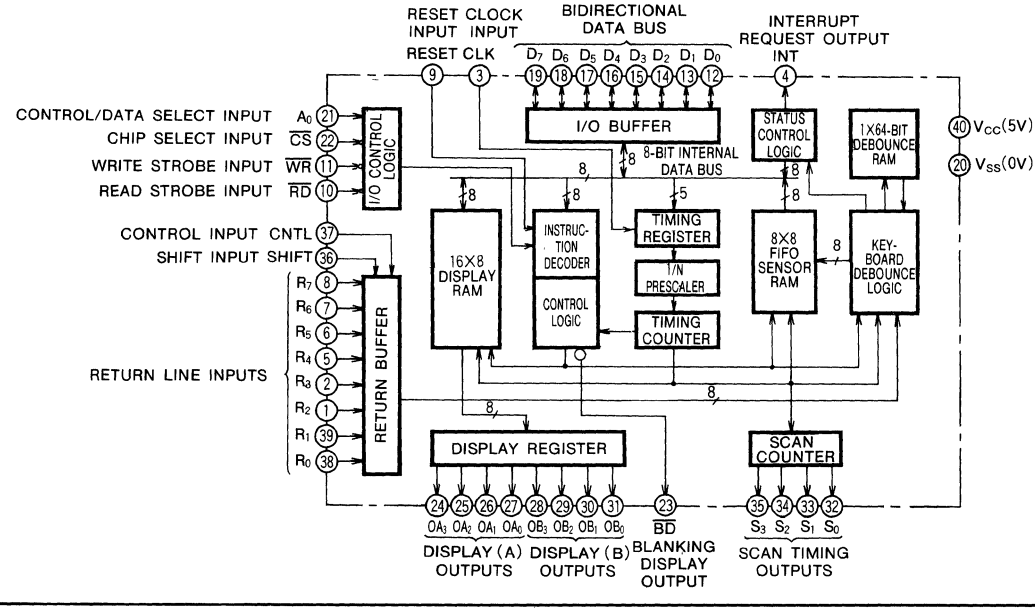


Outline 40P4

FUNCTION

The total chip, consisting of a keyboard interface and a display interface, can be programmed by eight 8-bit commands. The keyboard portion is provided with a 64-bit key debounce buffer and an 8 × 8-bit FIFO/SENSOR RAM. It operates in any one of the scanned keyboard mode, scanned sensor matrix mode or strobed entry mode. The display portion is provided with a 16 × 8-bit display RAM that can be organized into a dual 16× 4 configuration. Also, an 8-digit display configuration is possible by means of programming.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DISCRIPTION

pin	Name	Input or output	Functions
R_0~R_7	Return line inputs	In	These are the return lines which are connected with the scan lines through the keys or sensor switches, and are used for 8-bit input in the strobed entry mode They are provided with internal pullups to maintain them high-level until a switch closure pulls one low-level. They become active at low-level
CLK	Clock input	in	Clock signal from the system which is used to generate internal timing.
INT	Interrupt request output	Out	When there is any data in the FIFO during the keyboard mode or the strobed mode, this signal turns high-level so as to request interrupt to the CPU. It turns low-level each time data is read, but if any data remains in the FIFO it will turn high-level again and request interrupt to the CPU. End Interrupt command resets INT signal.
RESET	Reset input	In	Resets the chip when this signal is high-level. After the reset it assumes 16-digit, left-entry, encode display and 2-key lockout mode, and the prescale value of the clock becomes 31 The display RAM, however, is not cleared.
$\overline{RD}$	Read strobe input	In	Functions to control data transfer to the data bus
$\overline{WR}$	Write strobe input	In	Functions to control command/data transfer from the data bus.
D_0~D_7	Bidirectional data bus	In/out	All data and commands between the CPU and the chip are transferred through these lines.
A_0	Control/data select input	In	When this signal is high-level, it indicates that the signals in and out are either command (in) or status (out). When low-level, it indicates they are data (in/out)
$\overline{CS}$	Chip select input	In	Chip select is enabled when this signal is low-level
$\overline{BD}$	Blanking display output	Out	This signal is used in preventing overlapped display during digit swiching. It also may be brought to low-level by display blanking command.
OA_0~OA_3 OB_0~OB_3	Display (A) and (B) outputs	Out	These output ports can be used either as a dual 4-bit port or a single 8-bit port depending on an application, and the contents of the display RAM are output synchronizing with the scan timing signals These two 4-bit ports may be blanked independently Blanking may be activated with either high- or low-level signal by means of clear command.
S_0~S_3	Scan timing outputs	Out	These signals are used to scan the key switch, the sensor matrix or the display digit They can be either decoded or encoded, but it requres an external decoder in the encode mode. Signals S_0~S_3 are all turned to low-level when RESET is high-level
SHIFT	Shift input	In	In the keyboard mode, the shift input becomes the second highest bit of the key input information and is stored in the FIFO This input is ignored in the other modes. It is constantly kept at high-level by an internal pull resistor. The signal is active at high-level.
CNTL	Control input	In	In the keyboard mode, the control input becomes the most significant bit of the key input information and is stored in the FIFO. The signal is active at high-level In the strobed entry mode, it becomes the strobe signal and stores the return input data in the FIFO at the rising edge of the input It affects nothing internal in the sensor mode It is constantly kept at high-level by an internal pullup resistor

OPERATION

One of the three operating modes, the keyboard mode is the most common, and allows programmed 2-key lockout and N-key rollover. Encoded timing signals corresponding with key input are stored in the FIFO through the keydebounce logic, and the debouncing time of the key is also programmable. In the sensor mode, the contents of the 8 × 8 key contacts are constantly stored in the FIFO/sensor RAM, generating an interrupt signal to the CPU each time there is a change in the contents. In the strobed entry mode, the CNTL input signal is used as a strobe for storing the 8 return line inputs to the FIFO/sensor RAM.

The display portion is provided with a 16 × 8-bit display RAM that can be organized into a dual 16 × 4-bit configuration. Also, an 8-digit display configuration is possible by means of programming. Input to the register can be performed by either left or right entry modes. In the auto increment mode, read and write can be carried out after designating the starting address only.

Both the keyboard and display sections are scanned by common scan timing signals that are derived from the basic clock pulse. This frequency-dividing ratio is changeable by means of programming. There are decode and encode modes for the scanning mode; timing signals that are decoded from the lower 2 bits of the scan counter are output in the decode mode, while the 4-bit binary output from the scan counter is decoded externally in the encode mode.

COMMAND DESCRIPTION

There are eight commands provided for programming the operating modes of the M5L8279P-5. These commands are sent on the data bus with the signal $\overline{CS}$ in low-level and the signal A_0 in 1 and are stored in the M5L8279P-5 at the rising edge of the signal $\overline{WR}$. The order of the command execution is arbitrary.

1. Mode Set Command

	MSB							LSB
Code :	0	0	0	D	D	K	K	K

DD (Display mode set command)

0 0 8—8-bit character display—left entry
0 1 16—8-bit character display—left entry (Note1)
1 0 8—8-bit character display—right entry
1 1 16—8-bit character display—right entry

KKK (Keyboard mode set command)

0 0 0 Encoded display keyboard mode — 2-key lockout (Note1)
0 0 1 Decoded display keyboard mode — 2-key lockout
0 1 0 Encoded display keyboard mode — N-key rollover
0 1 1 Decoded display keyboard mode — N-key rollover
1 0 0 Encoded display, sensor mode
1 0 1 Decoded display, sensor mode
1 1 0 Encoded display, strobed entry mode
1 1 1 Decoded display, strobed entry mode

Note 1 : Default after reset.

2. Program Clock Command

	MSB							LSB
Code :	0	0	1	P	P	P	P	P

The external clock is divided by the prescaler value PPPPP designated by this command to obtain the basic internal frequency.

When the internal clock is set to 100kHz, it will give a 5.1ms keyboard scan time and a 10.3ms debounce time. The prescale value that can be specified by PPPPP is from 2 to 31. In case PPPPP is 00000 or 00001, the prescale is set to 2. Default after a reset pulse is 31, but the prescale value is not cleared by the clear command.

3. Read FIFO Command

	MSB							LSB	
Code :	0	1	0	AI	X	A	A	A	X = Don't care

This command is used to specify that the following data readout ($CS \cdot \overline{A_0} \cdot RD$) is from the FIFO. As long as data is to be read from the FIFO, no additional commands are necessary.

AI and AAA are used only in the sensor mode. AAA designates the address of the FIFO to be read, and AI is the auto-increment flag. Turning AI to 1 makes the address automatically incremented after the second read operation. This auto-increment bit does not affect the auto-increment of the display RAM.

4. Read Display RAM Command

	MSB							LSB
Code :	0	1	1	AI	A	A	A	A

This command is used to specify that the following data readout ($CS \cdot \overline{A_0} \cdot RD$) is from the display RAM. As long as data is to be read from the display RAM, no additional commands are necessary.

The data AAAA is the value with which the display RAM read/write counter is set, and it specifies the address of the display RAM to be read or written next.

AI is the auto-increment flag. Turning AI to 1 makes the address automatically incremented after the second read/write operation. This auto-increment bit does not affect the auto-increment of FIFO readout in the sensor mode.

5. Write Display RAM Command

	MSB							LSB
Code :	1	0	0	AI	A	A	A	A

With this command, following display RAM read/write addressing is achieved without changing the data readout source (FIFO or display RAM). Meaning of AI and AAAA are identical with read display RAM command.

6. Display Write inhibit/Blanking Command

	MSB							LSB	
Code :	1	0	1	X	IW	IW	BL	BL	X = Don't care
					A	B	A	B	

The IW is a write inhibit bit to the display RAM that corresponds with the output A or B. Inhibit is activated by turning the IW 1.

The BL is used in blanking the out A or B. Blanking is activated by turning the BL 1. Setting both BL flags makes the signal $\overline{BD}$ low-level so that it can be used in 8-bit display mode.

Resetting the flags makes all IW and BL turn 0.

7. Clear Command

	MBS							LSB
Code :	1	1	0	C_D	C_D	C_D	C_F	C_A

C_D: Clears the display RAM.

C_D	C_D	C_D	
0	X	X	No specific performance
1	0	X	Entire contents of the display RAM are turned 0.
1	1	0	The contents of the display RAM are turned 20H (00100000 = $0A_30A_20A_10A_0$ $0B_30B_20B_10B_0$).
1	1	1	Entire contents of the display RAM are turned 1.

C_F : Clears the status word and resets the interrupt signal (INT).

C_A : Clears the display RAM and the status word and resets the interrupt signal (INT).

Clearing condition of the display RAM is determined by the lower 2 bits of the C_D.

Clearing the display RAM needs some time (~ 160 μ second) and causes the display-unavailable status (DU) in the status word to be 1. The display RAM is not accessible for the duration of this time, even if the display mode was in 8-digit display mode or a decoded mode.

As both C_F and C_A function to reset the internal keydebounce counter, the key input under counting is ignored, and the internal FIFO counter is reset to make the interrupt signal low-level.

C_A resets the internal timing counter, forcing $S_0 \sim S_3$ to start from $S_3S_2S_1S_0 = 0000$ after the execution of the command.

8. End Interrupt/Error Mode Set Command

	MSB							LSB	
Code :	1	1	1	E	X	X	X	X	X = Don't care

In the sensor matrix mode, an interrupt signal is generated at the beginning of the next key scan time to inhibit further writing to the FIFO when there is a change in the sensor switch. The interrupt request output INT is reset when the sensor RAM is read with the Auto-increment flag 0, or the execution of this command.

When E is kept in 0, depression of any sensor makes the second highest bit of the status word 1. When E is kept in 1, the status is kept 0 all the time.

When E is programmed to 1 in the N-key rollover mode, the execution of this command makes the chip operate in special error mode, during which time depression of more than two keys in a key debounce time causes an error and sets the second highest bit of the status word 1.

STATUS WORD

MSB							LSB
DU	S/E	O	U	F	N	N	N

NNN: Indicates the number of characters in the FIFO during the keyboard and strobed entry modes.

F: Indicates that the FIFO is filled up with 8 characters. The number of characters existing in the FIFO (0 ~ 8 characters) can be known by means of the bits NNN and F (FNNN = 0000~FNNN = 1000).

U: Underrun error flag
This flag is set when a master CPU tries to read an empty FIFO.

O: Overrun error flag
This flag is set when another character is strobed into a full FIFO.
The bits U and O cannot be cleared by status read. They will be cleared by the clear command.

S/E: Sensor closure/multiple error flag
When 111EXXXX is executed by turning E = 0 , the bit S/E in the status word is set when there is at least one sensor closure.
When 111EXXXX is executed by turning E = 1 (special error mode), the bit S/E is set when there are more than two key depressions made in a key scan time.

DU: Display unavailable
This flag is set when a clear display command is executed, and announces that the display RAM is not accessible.

CPU INTERFACE

1. Command Write

A command is written on the rising edge of the signal $\overline{WR}$ with $\overline{CS}$ low-level and A_0 1.

2. Data Write

Data is written to the display RAM on the rising edge of the signal $\overline{WR}$ with $\overline{CS}$ low-level and A_0 0.

The address of the display RAM is also incremented on the rising edge of the signal $\overline{WR}$ if AI is set for the display RAM.

3. Status Read

The status word is read when $\overline{CS}$ and $\overline{RD}$ are low-level and A_0 is 1. The status word appears on the data bus as long as the signal $\overline{RD}$ is low-level.

4. Data Read

Data is read from either the FIFO or the display RAM with $\overline{CS}$ and $\overline{RD}$ are low-level and A_0 is 0. The source of the data (FIFO or display RAM) is decided by the latest command (read display or read FIFO). The data read appears on the data bus as long as the signal $\overline{RD}$ is low-level.

The trailing edge of the signal $\overline{RD}$ increments the address of the FIFO or the display RAM when AI is set. After the reset, data will be read from the FIFO, however.

A_0	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	Operation
1	L	H	L	Command write
0	L	H	L	Data write
1	L	L	H	Status read
0	L	L	H	Data read
X	H	X	X	No operation

KEYBOARD INTERFACE

Keyboard interface is done by the scan timing signals (S_0~S_3), the return line inputs (R_0 ~ R_7), the SHIFT and the CNTRL inputs.

In the decoded mode, the low-order of 2 bits of the internal scan counter are decoded and come out on the timing pins (S_0~S_3). In the encoded mode, the four binary bits of the scan counter are directly output on the timing pins, thus a 3-to-8 decoder must be employed to generate keyboard scan timing.

The return line inputs (R_0~R_7), the SHIFT and the CNTL inputs are pulled up high-level by internal pullup transistors until a switch closure pulls one low.

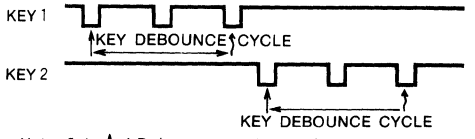
The internal key debounce logic works for a 64-key matrix that is obtained by combining the return line inputs with the scan timing.

For the keyboard interface, M5L8279P-5 has four distinctive modes that allow various kinds of applications. In the following explanation, a "key scan cycle" is the time needed to scan a 64-key matrix, and a "key debounce cycle" needs a duration of two "key scan" cycles. (In the decoded mode 32 keys, unlike 64 keys in the encoded mode, can be employed for a maximum key matrix due to the limit of timing signals However, both the key scan cycle and the key debounce cycle are the same as in the encoded mode.)

1. 2-Key Lockout (Scanned Keyboard Mode)

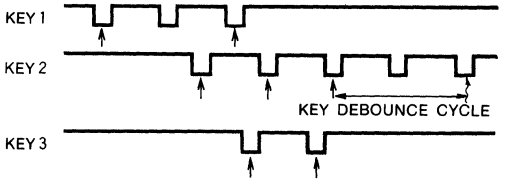
The detection of a new key closure resets the internal debounce counter and starts counting. At the end of a key debounce cycle, the key is checked and entered into the FIFO if it is still down. An entry in the FIFO sets the INT output high. If any other keys are depressed in a key debounce cycle, the internal key debounce counter is reset each time it encounters a new key. Thus only a single-key depression within a key debounce duration is accepted, but all keys are ignored when more than two keys are depressed at the same time.

Example 1 : Accepting two successive key depressions



Note 2 : ↑ : Debounce counter reset
↑ : Key input

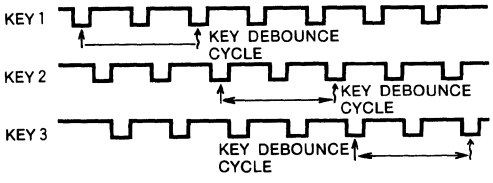
Example 2 : Overlapped depression of three keys



Note 3 : Only key 2 is acceptable

2. N-Key Rollover (Scanned Keyboard Mode)

Each key depression is treated independently from all others so as to allow overlapped key depression. Detection of a new key depression makes the internal key debounce counter reset and start to count in a same manner as in the case of 2-key lockout. But, in N-key rollover, other key closures are entirely ignored within a key debounce cycle so that depression of any other keys would not reset the key debounce counter. In this way, overlapped key depression is allowed so as to enable the following key input:

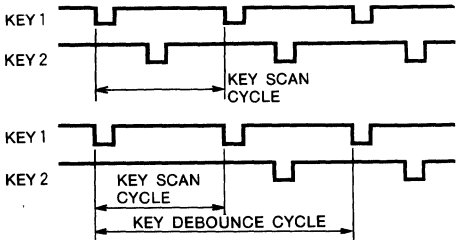


The scanned key input signal does not always reflect the actual key depressing action, as the key matrix is scanned by the timing signal.

With N-key rollover, there is a mode provided with which error is caused when there are more than 2 key inputs in a key debounce cycle, which can be programmed by using the end interrupt/error mode set command. In this mode (special error mode), recognition of the above error sets the INT signal to high-level and sets the bit S/E in the status word.

In case 2 key entries are made separately in more than a debounce cycle, there would be no problem, as key depression is clearly identified. And no problem exists for 2-key lockout, as the both keys are recognized invalid.

Example of error (Special error mode)



3. Sensor Matrix Mode

The key debounce logic is disabled in this mode. As the image of the sensor switch is kept in the FIFO, any change in this status is reported to the CPU by means of the interrupt signal INT. Although a debounce circuit is not used in this mode, it has an advantage in that the CPU is able to know how long and when the sensor was depressed.

In the sensor matrix mode with the bit E = 0 of the end interrupt/error mode set command, the second most significant bit of the status word (S/E bit) is set to 1 when any sensor switch is depressed.

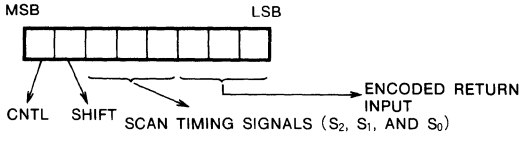
Any sensor change detected by the M5L8279P-5 in one key scan cycle causes only once INT generation at the first timing of the next scan cycle.

4. Strobe Mode

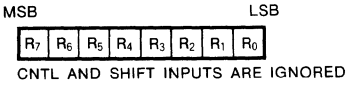
The data is entered into the FIFO from the return lines (R_0~R_7) at the rising edge of a CNTL pulse. The INT goes high while any data exists in the FIFO, in the same manner as in the keyboard mode. The key debounce circuit will not operate.

Formats of data entered into the FIFO in each of the above modes are described in the following:

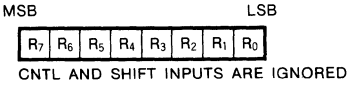
Keyboard matrix



Sensor matrix mode



Storobe mode



DISPLAY INTERFACE

The display interface is done by 8 display outputs ($OA_0 \sim OA_3$, $OB_0 \sim OB_3$), a blanking signal ($\overline{BD}$), and scan timing outputs ($S_0 \sim S_3$).

The relation between the data bus and the display outputs is as shown below:

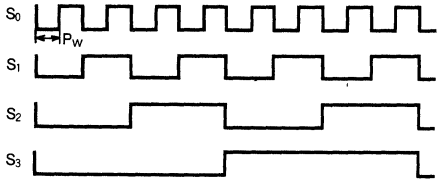
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
↓	↓	↓	↓	↓	↓	↓	↓
OA_3	OA_2	OA_1	OA_0	OB_3	OB_2	OB_1	OB_0

Clearing the display RAM is not achieved by the reset signal (9-pin) but requires the execution of the clear command.

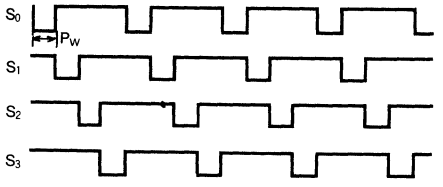
The timing diagrams for both the encoded and decoded modes are shown below.

For the encoded mode, a 3-to-8 or 4-to-16 decoder is required, according to whether eight or sixteen digit display used.

(1) Encoded mode

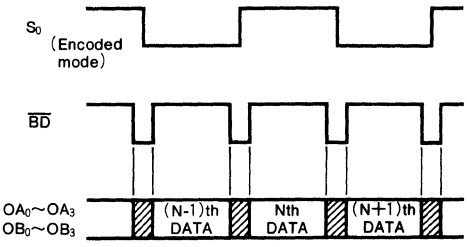


(2) Decoded mode



Note 4 : Here P_W is 640μs if the internal clock frequency is set to 100kHz.

Timing relations of S_0, $\overline{BD}$, and display outputs ($OA_0 \sim OA_3$, $OB_0 \sim OB_3$) are shown below.



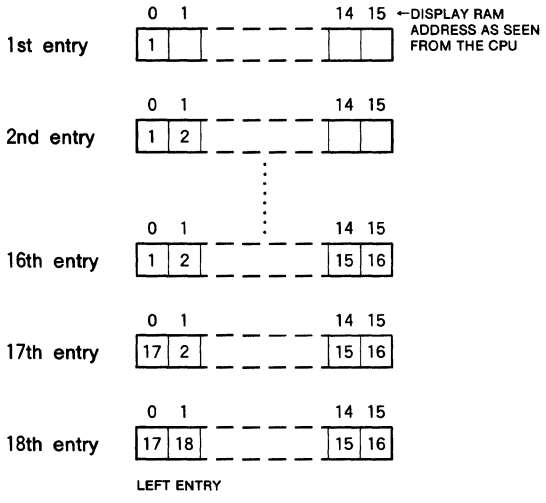
Note 5 : Values of the output data shown in the slanted line areas are decided upon the clear command executed last to become the value of the display RAM after the reset. The values in the slanted areas after reset will go low-level. In the same manner, the values $OA_0 \sim OA_3$, $OB_0 \sim OB_3$ are dependent on the clear command executed last. When the both A and B are blanked, the signal $\overline{BD}$ will be in low-level.

KEY ENTRY METHODS

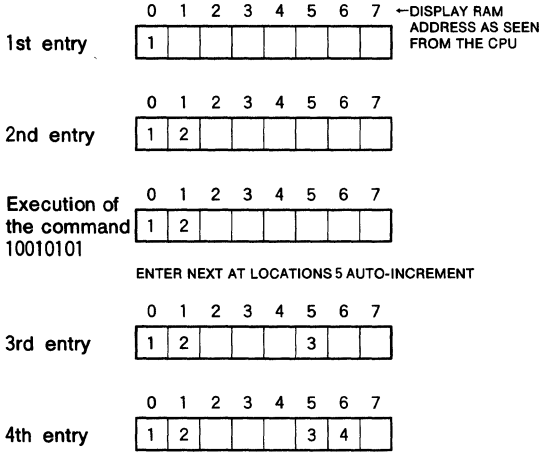
1. Left Entry

Address 0 in the display RAM corresponds to the leftmost position ($S_3S_2S_1S_0 = 0000$) of a display and address 15 (or address 7 in 8-character display) to the rightmost position ($S_3S_2S_1S_0 = 1111$ or $S_2S_1S_0 = 111$). The 17th (9th) character is entered back into the leftmost position.

Auto-increment mode



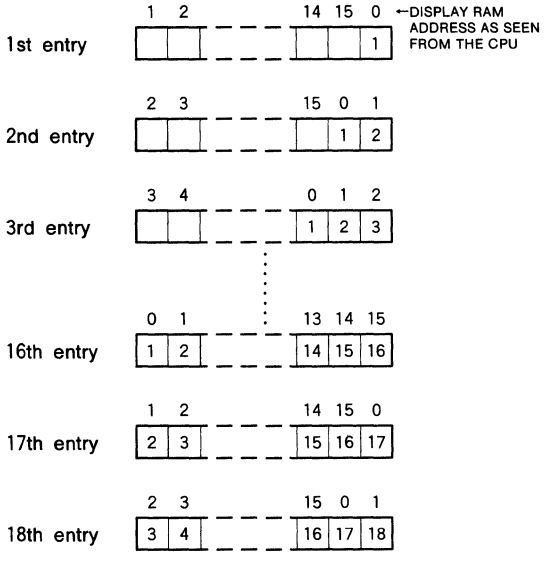
Auto-increment mode



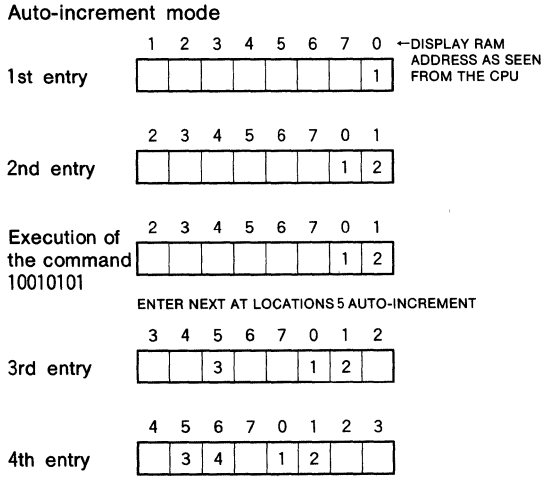
2. Right Entry

The first data is entered in the rightmost position of a display. From the next entry, the display is shifted left one character and the new data is placed in the rightmost position. A display position and a register address as viewed from the CPU change each time and do not correspond.

Auto-increment mode



Auto-increment mode



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
P_d	Maximum power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating free-air temperature range		−20～75	℃
T_{stg}	Storage temperature range		−60～150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～75℃, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20～75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{IH(RL)}$	High-level input voltage, for return line inputs		2.2			V
V_{IH}	High-level input voltage, all others		2.0			V
$V_{IL(RL)}$	Low-level input voltage, for return line inputs		V_{SS}-0.5		1.4	V
V_{IL}	Low-level input voltage, all others		V_{SS}-0.5		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
$V_{OH(INT)}$	High-level output voltage, interrupt request output	I_{OH}=−400μA	3.5			V
V_{OL}	Low-level output voltage	I_{OL}=2.2mA			0.45	V
I_{CC}	Supply current from V_{CC}				120	mA
$I_{I(RL)}$	Input current, return line inputs, shift input and control input	V_I=V_{CC}			10	μA
		V_I=0V	−100			
I_I	Input current, all others	V_I=0V, V_{CC}	−10		10	μA
I_{OZ}	Off-state output current	V_O=0V～V_{CC}	−10		10	μA
C_I	Input terminal capacitance	V_I=V_{CC}	5		10	pF
C_O	Output terminal capacitance	V_O=V_{CC}	10		20	pF

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted.)

Read Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{C(R)}$	Read cycle time		1000			ns
$t_{W(R)}$	Read pulse width		250			ns
$t_{SU(A-R)}$	Address setup time befor RD		0			ns
$t_{h(R-A)}$	Address setup time after RD		0			ns

Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{C(W)}$	Write cycle time		1000			ns
$t_{W(W)}$	Write pulse width		250			ns
$t_{SU(A-W)}$	Address setup time before WR		0			ns
$t_{h(W-A)}$	Address hold time after WR		0			ns
$t_{SU(DQ-W)}$	Data input setup time before WR		150			ns
$t_{h(W-DQ)}$	Data input hold time after WR		0			ns

Other Timing

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{C(\phi)}$	Clock cycle time		320		DC	ns
$t_{W(\phi)}$	Clock pulse width		120			ns

For an internal clock frequency of 100kHz

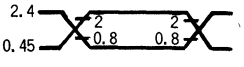
- Key scan cycle time: ~ 5.1ms
- Key debounce cycle time: ~10.3ms
- Single-key scan time: 80μs
- Display scan time: ~10.3ms
- Single digit display time: 490μs
- Blanking time: 150μs
- Internal clock cycle: 10μs

SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Output enable time after read	C_L=150pF			150	ns
$t_{PZV(A-DQ)}$	Output enabl time after address				250	ns
$t_{PVZ(R-DQ)}$	Output disable time after read		10		100	ns

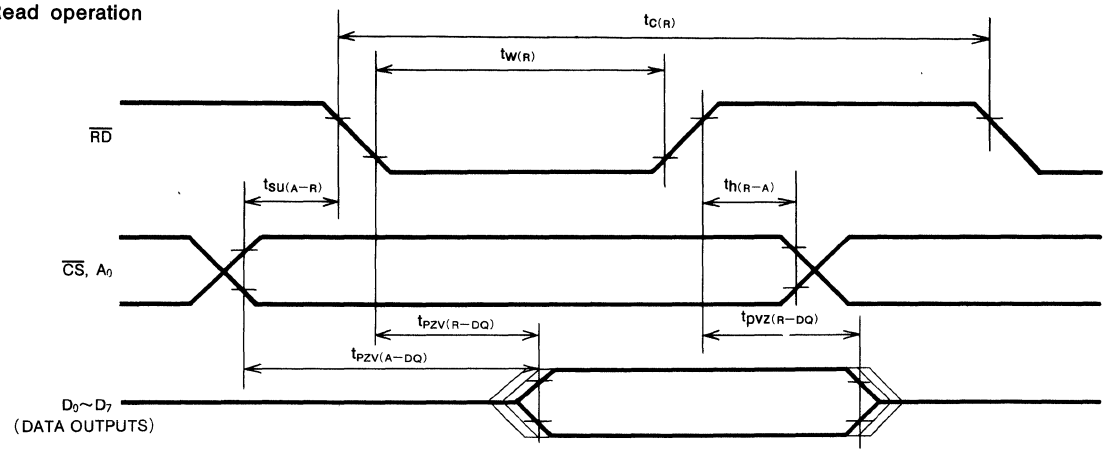
Note 6 : A. C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	20ns
Input pulse fall time	20ns
Referens level input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V

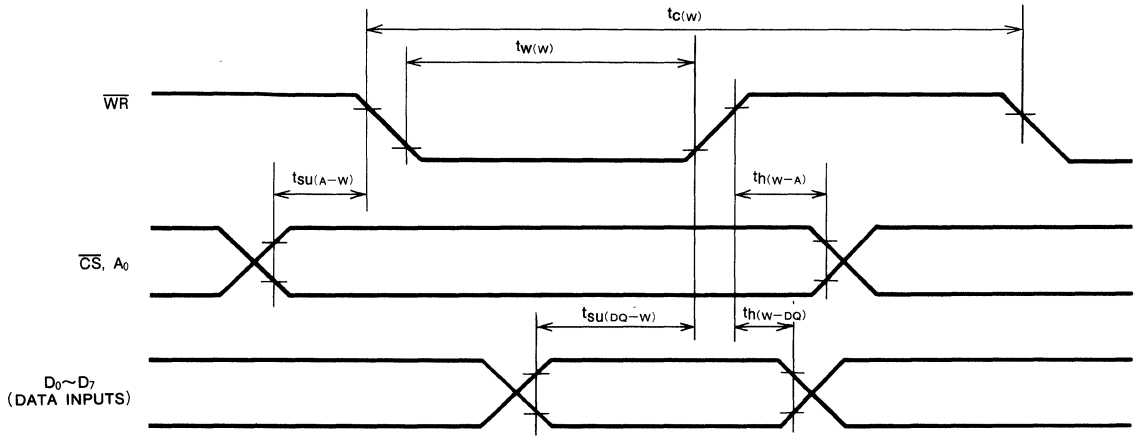


TIMING DIAGRAM

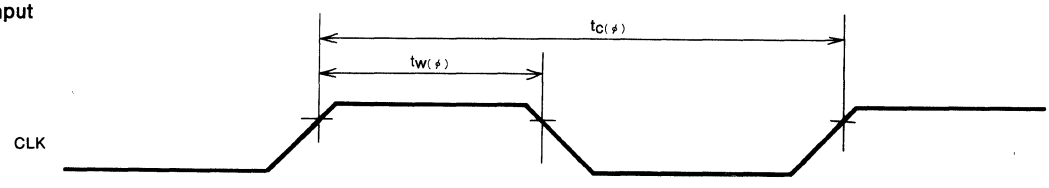
Read operation



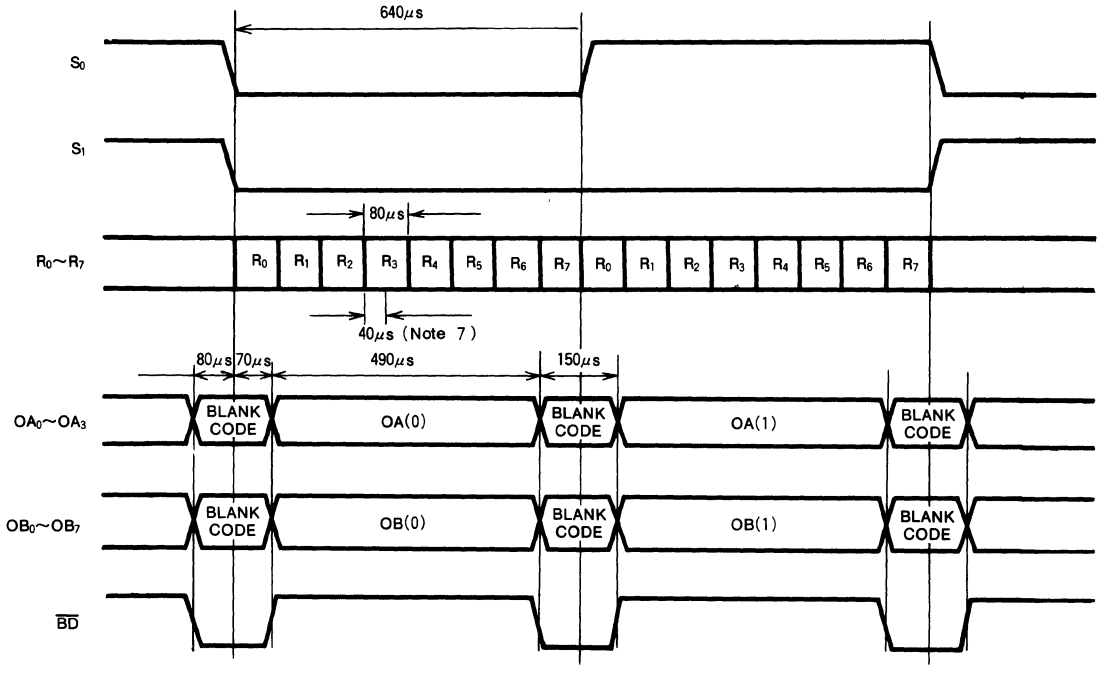
Write operation



Clock input

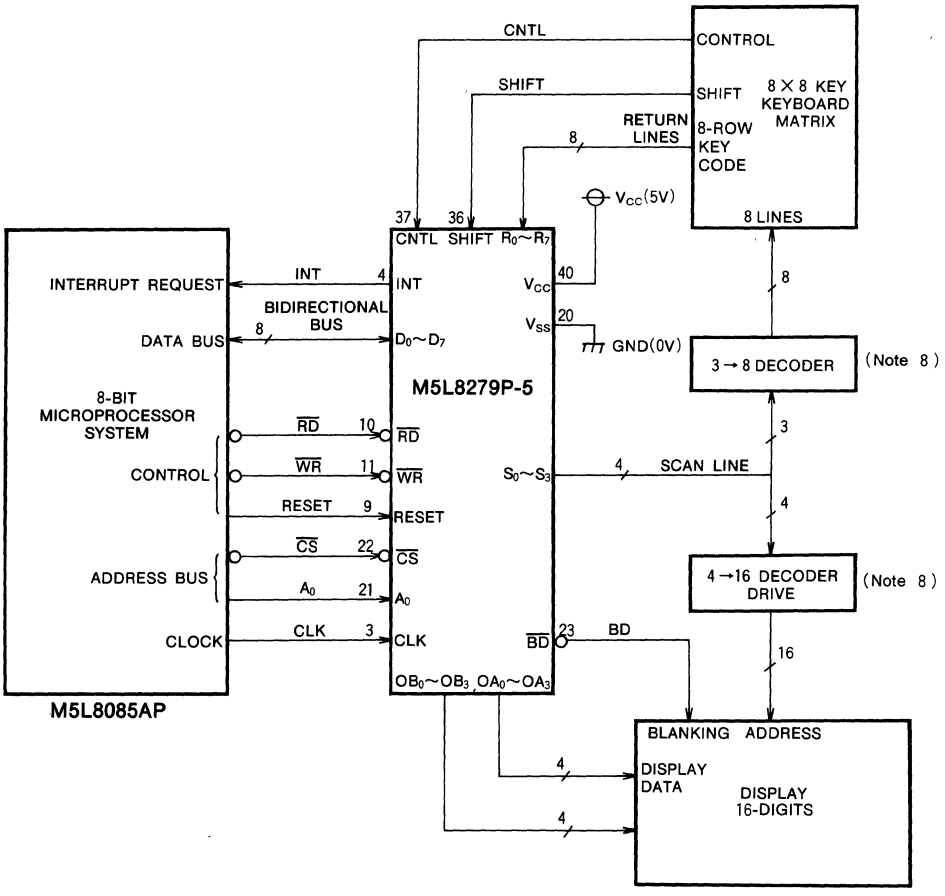


DISPLAY (This example is encoded display, left entry mode with internal clock cycle 10μsec. Scan timing output S_2, S_3 are not shown.)



Note 7 : The scanned data on the return line is sampled serialy from R_0 to R_7. Each data is latched in the middle of the each sampling period.

APPLICATION EXAMPLE



Note 8 : When using an 8-bit character display of more than 9 digits for the decoder display, it is necessary to provide two decoders for example 4→10 decoder, 4→16 decoder and key scan 3→8 decoder.
Only S_0, S_1 and S_2 may be used as inputs to the key scan 3→8 decoder.
(Don't drive the keyboard decoder with the MSB of the scan line)

APPLICATION

6

NOTICE FOR CMOS PERIPHERALS

1. INTRODUCTION

Mitsubishi Electric's microprocessor-support CMOS peripheral LSI devices are compatible with current NMOS peripheral devices, and feature the additional advantages listed below.

- Low power dissipation
- Wide supply voltage range, V_{CC}=5V±10%
- Wide operating temperature range, T_a=−20~75℃
- Improved timing conditions

Due to these advantageous features, CMOS peripheral devices can be used to replace conventional NMOS devices in their typical applications, and can additionally be used in applications requiring low power dissipation.

The following sections describe the basic characteristics of Mitsubishi Electric's CMOS peripheral LSI devices for microprocessor support, and explain precautions and methods of use.

2. BASIC CIRCUITS AND CONSTRUCTION

The internal circuitry of CMOS devices consist of both p-channel and n-channel transistors.

There are two types of NMOS transistors. In the depletion-type, drain-to-source remains on even when gate-to-source voltage is 0V, and with the enhancement-type device, dropping gate-to-source voltage below the threshold voltage level turns the transistor off. CMOS devices employ the enhancement type, regardless of whether they are p-channel or n-channel devices.

Fig. 1 shows the typical inverter construction, which is the basis of CMOS peripherals and Fig. 2 illustrates its equivalent circuit diagram.

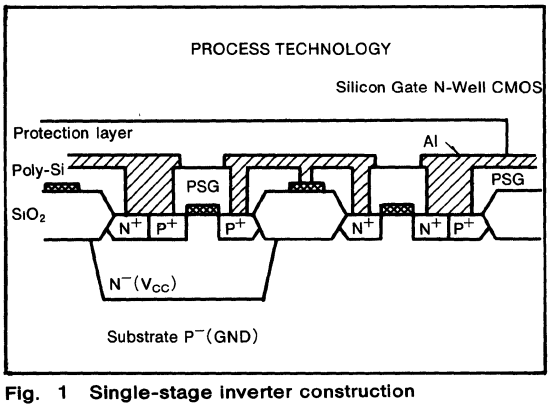


Fig. 1 Single-stage inverter construction

3. OPERATIONAL DESCRIPTION

Fig. 3 illustrates what happens when supply voltage (V_{CC}) is applied to the circuit shown in Fig. 2, varying input voltage from V_{SS} to V_{CC}. The V_O curve indicates the change in output voltage and supply current (I_{CC}).

As illustrated, these characteristics depend on input voltage, so can be better understood by dividing V_I into three regions, Ⅰ~Ⅲ.

Ⅰ : In this region, only the p-channel transistor T_2 is on, so that the V_O output voltage becomes V_{CC}. In this condition, practically no current I_{CC} flows.

Ⅱ : In this region, V_O varies in accordance with V_I. When V_I is increased from region Ⅰ, the n-channel transistor T_1 begins to turn on, so that V_O gradually decreases and at some point begins to decrease rapidly. The value of V_I at this point of rapid V_O decrease is known as the circuit threshold voltage.

When this voltage is exceeded, as V_I is increased, V_O approaches V_{SS}.

In the region Ⅱ, V_O is determined by the ratio of the on resistances of T_1 and T_2.

I_{CC} is always flowing in this region, and becomes maximum when V_I is at the circuit threshold voltage.

Ⅲ : In this region, since only T_1 is on, V_O becomes the voltage V_{SS}. In this region, as was the case for region Ⅰ, virtually no I_{CC} current flows.

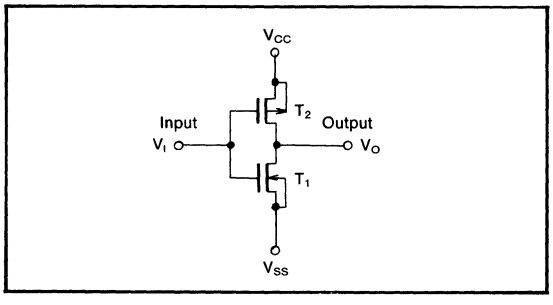


Fig. 2 Single-stage inverter circuit

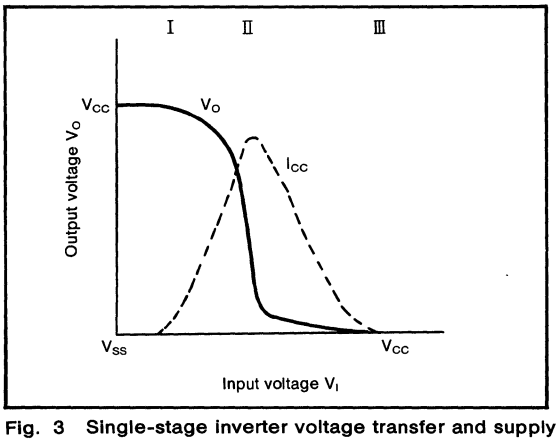


Fig. 3 Single-stage inverter voltage transfer and supply current vs. input voltage characteristics

4. TRANSFER CHARACTERISTICS AND POWER DISSIPATION

For COMS devices, the circuit threshold voltage is approximately one-half of V_{CC}. Contrasted with NMOS logic, where threshold voltage is a fixed level not related to supply voltage, ideal transfer characteristics can be achieved.

In order to maintain compatibility with the conventional NMOS devices, transfer characteristics of CMOS peripherals I/O circuits have been established at TTL level.

Fig. 4 illustrates input voltage V_{IN} versus supply current I_{CC} for M5M82C55AP-2. Here, when V_{IN} reaches 1.3 to 1.5V, the resulting switch in internal circuits causes a sharp increase in I_{CC} flow.

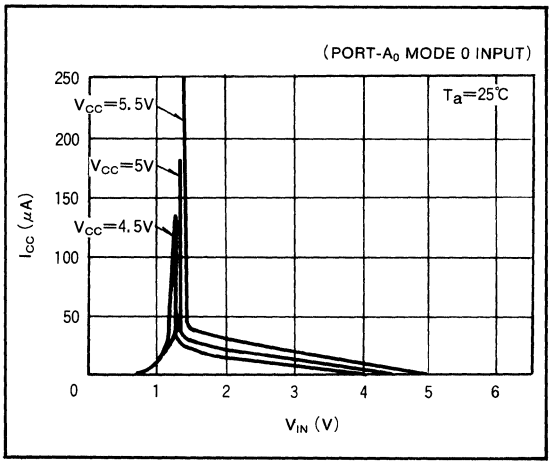


Fig. 4 Input voltage vs. dissipation current M5M82C55AP-2

In a CMOS curcuit, since p-channel and n-channel transistors are connected in series between the V_{CC} and V_{SS}, as long as gate voltage is at the V_{CC} or V_{SS} level, one of the two transistors will be in an off state. Consequently, fixing the input pin at the V_{CC} or V_{SS} level causes the static dissipation current (I_{CC}) flow from the V_{CC} to V_{SS} pin to consist only of p-n junction leakage current. As a consequence, the per-gate static dissipation current remains at about 50pA at T_a = 25℃, and will not go over more than a few nanoamperes even at T_a=85℃. This is the primary reason behind CMOS devices low power dissipation.

Note however that power dissipation does increase when CMOS circuits are used in the switching mode. As was mentioned in the transfer characteristic description, transients in the input voltage cause current to flow from the V_{CC} to V_{SS}. The amount of current flow increases relative to higher V_{CC} values and operating frequency. Additionally, when capacitive loads (load capacitance also varies depending on the number of fanouts) are connected to the device, charging currents will be requied, which also increases power dissipation.

The M5M82C55AP-2 illustrated in Fig. 4 has parallel-connected I/O ports, and is relatively limited in switching operations. However, devices such as the programmable timer M5M82C54P are subjected to constant clock operations, and the current flow for each CMOS circuit must be added to get the total for the device. As shown in Fing. 5, currnet dissipation increases along with increases in operating frequency.

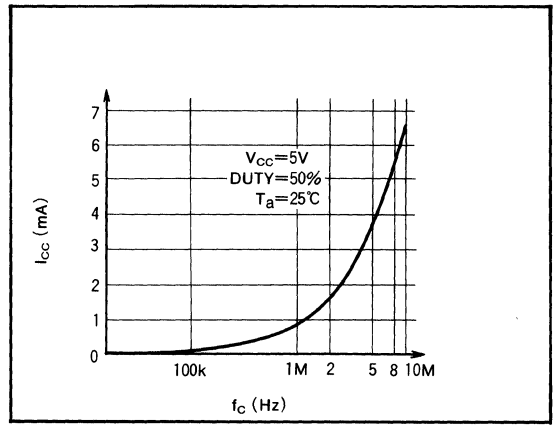


Fig. 5 Operating frequency vs. power dissipation M5M82C54P

The power dissipation characteristics of DMA controller M5M82C37AP-5 are illustrated in Fig.6.

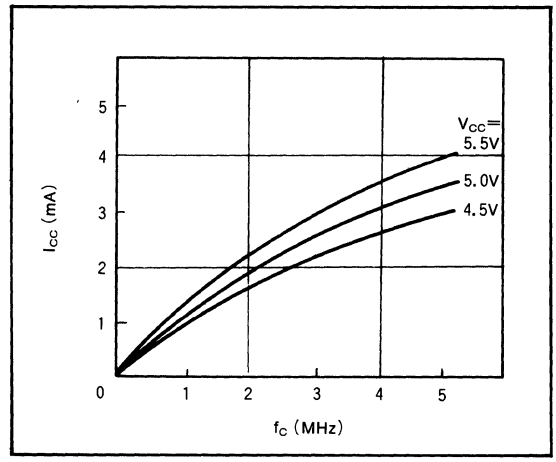


Fig. 6 Operating frequency vs. power dissipation M5M82C37AP-5

5. NOISE MARGIN

As was noted in section 4, I/O levels for CMOS peripheral LSI devices have been established for TTL interface compatibility. Fig. 7 shows a comparison of DC noise margins when CMOS peripheral devices are interfaced with other logic devices. As seen here, with CMOS-to-CMOS interfaces, V_{IH}(min) remains very tolerable. However, since the CMOS peripheral device standard provides for TTL interface, V_{OH}(min) is defined for states where I_{OH} flow is substantial ($I_{OH} = -400\mu A$). When actually connected to a CMOS logic gate, the required value for I_{OH} is only the small current required to drive the gate-to-gate capacitance. So $V_{IH\,(MIN)}$ for a CMOS gate satisfies this requirement with room to spare. Fig. 8 shows the V_{OH} characteristics for the M5M82C55AP-2 data bus. As seem here, the margin between the standard and actual performance is substantial.

Low-speed CMOS gates have high internal propagation delay times, which further increases their noise margin. However, the CMOS gates used in peripheral devices still hold delay time to less than 1ns per stage. They are therefore capable of responding to pulses which transient at extermely high speeds, and noise margins are as good as similar type NMOS devices.

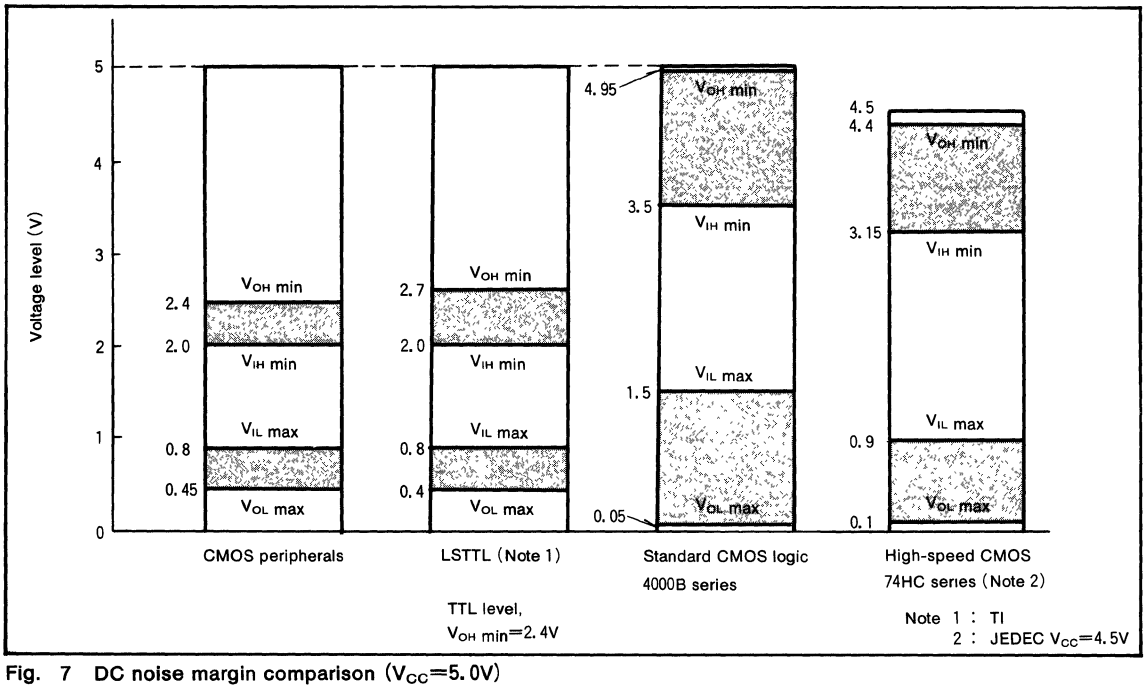


Fig. 7 DC noise margin comparison (V_{CC}=5.0V)

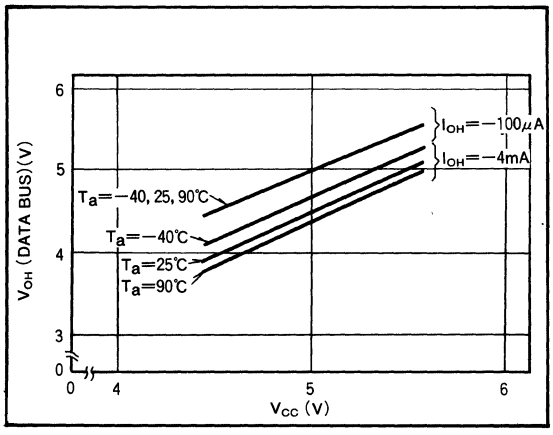


Fig. 8 V_{OH} characteristics M5M82C55AP-2

6. FANOUT

The drive capability of CMOS peripheral devices generally exceeds that of NMOS logic devices. Drive capability at "H" level is noticeably better than NMOS. This defference between logic types provides a slight difference when actually applied to driving a load such as a transistor, and the value of the load resistance can affect fanout capability. This point will be covered in more detail later.

For reference purposes, V_{OH} characteristics of M5M82C55AP-2 is illustarted in Fig. 8, and the "L" level drive capability of M5M82C55AP-2 is illustrated in Fig. 9.

When driving a MOS-IC with a peripheral LSI, since it is only necessary to drive the input leakage current of the DC-connected IC, fanout capability is quite good. However, where devices having many components (e.g., data bus, etc.) are connected, the stray capacitance of the wiring and device input capacitance (generally about 5pF) must also

be driven, so signal switching response is slower. In this case, the load (s) to be driven must be divided (or allocated to several devices) as with previous devices.

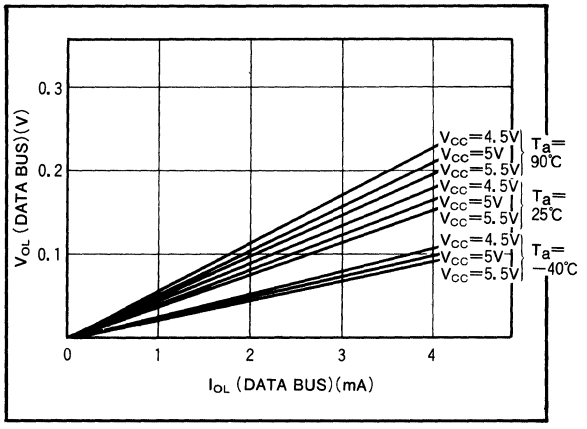


Fig. 9 I_{OL}-V_{OL} characteristics M5M82C55AP-2

7. INPUT CIRCUIT

Fig. 10 shows an equivalent circuit diagram of the input circuit for CMOS peripheral devices. The gate oxide layer of the transistors is extremely thin, and high voltages applied directly to the gates are likely to rupture their insulation, causing permanent demage to the device. To prevent gate damage, the diodes and input resistor shown in the diagram form a protection circuit.

Since threshold voltage for the input transistor is set at approximately 1.5V, as noted in section 4, if the input voltage is held at this level, a through current starts to flow from V_{CC} to V_{SS}. In systems where low dissipation current is required, this characteristic can cause problems in the design of the power supply.

Where a data bus is left floating, through current is likely to become a particular problem, so bus lines should be fixed at a certain level with a pull-up (or pull-down) circuit having high resistance values.

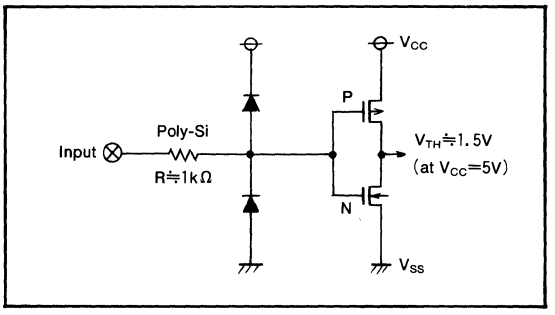
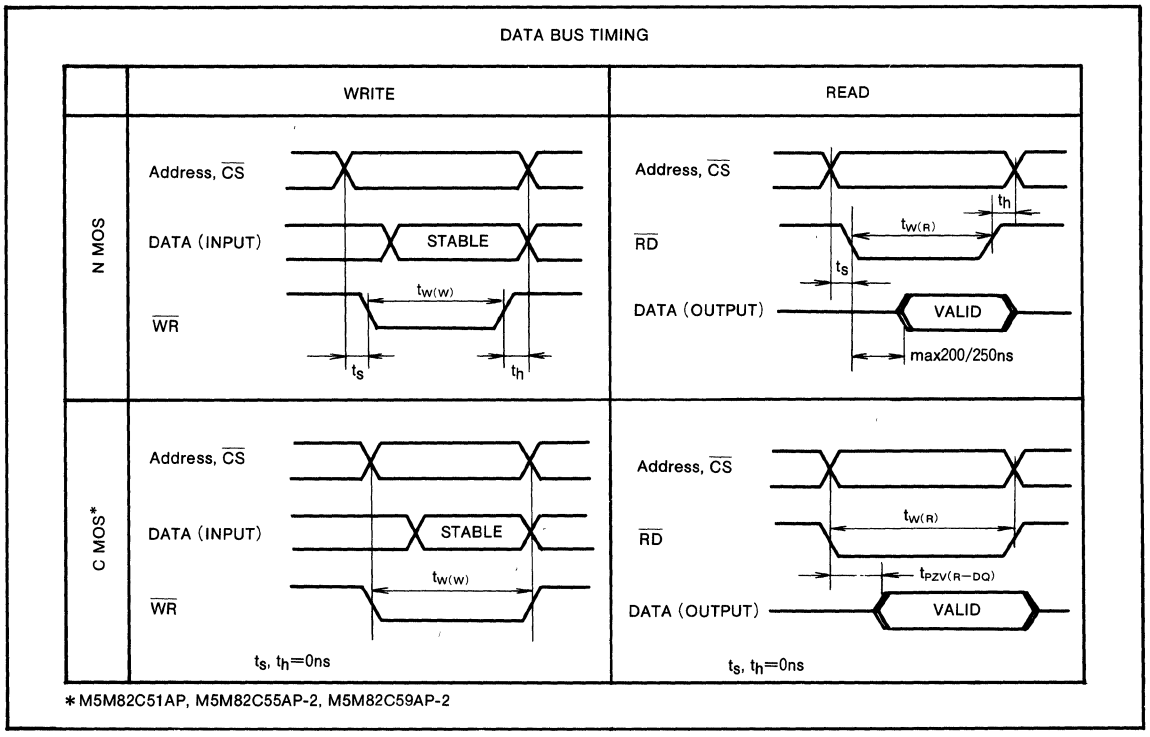


Fig. 10 CMOS peripheral device input circuit (equivalent diagram)



*M5M82C51AP, M5M82C55AP-2, M5M82C59AP-2

Fig. 11 Bus timing characteristics

8. TIMING CHARACTERISTICS

The timing conditions between the system and CMOS peripheral LSI devices have been improved over their NMOS type counterparts. Improvements include better setup and hold times, and microprocessor interfacing is easier. Fig. 11 summarizes there differences in comparison form. Whereas NMOS devices required t_s and t_h time, these have been eliminated with CMOS peripherals by setting t_s and t_h 0ns.

9. USAGE PRECAUTIONS

(1) Dealing with NC input pins

Leaving unused input pins open results in instability input voltage, which in turn can produce errors in output logic levels and increase current dissipation. Unused input pins should therefore be tied to V_{CC} or V_{SS}.

(2) Voltage supply lines

Power dissipation of CMOS peripherals whose internal changes are small such as M5M82C55AP-2 and M5M82C59AP-2 is extremely low. However, the through current spikes that occur during switching are dealt with using the traditional method applied to older ICs; by reducing power line impedance to filter the spikes. Penetrating currents flow in the form of spikes during switching. In the M5M82C37AP-5, large spike currents flow when a clock pulse caused the state of many output pins to change simultaneously. Therefore, as with previous CMOS LSIs, it is necessary to lower the impedance of the power supply circuit to absorb the spike current in the supply current. To accomplich this, each device should be fitted with a ceramic capacitor (having good high frequency characteristics and a capacitance of approx. 0.1μF) wired close between V_{CC} and V_{SS}.

Also, when devices such as M5M82C55AP-2 are used with a high current drive circuit connected to output, power lines should be run independently from the logic system and driver circuit to reduce adverse affect on the logic system.

(3) Latchup

CMOS LSIs are subject to a phenomenon known as latch-up. All CMOS circuits have parasitic bipolar transistors with a thyristor- like structure. If one of the parasitic thyristors is triggered by an external surge, it turns on and excessive current continues to flow even after the surge is removed.

Latch-up currents are large and may destroy the LSI unless they are reset by lowering the supply voltage to a certain level, (the holding voltage of the parasitic thyristors) or by turning off the power supply.

Latchup occurs under the five conditions listed below.

(a) $V_I > V_{CC} + V_F$
(b) $V_O > V_{CC} + V_F$
(c) $V_I < V_{SS} - V_F$
(d) $V_O < V_{SS} - V_F$
(e) Excessive V_{CC}

V_F:Forward voltage of the clamping diode used at input.

Conditions (a) or (c)

● When using a dual power supply

When dual power supplies serve CMOS logic devices, differences in the rising edge of the power line signal tend to cause latchup. This can be eliminated by using a series

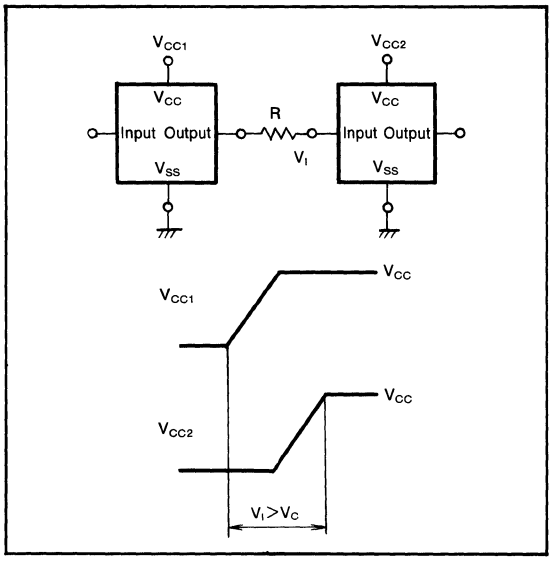


Fig. 12 Preventing latchup when dual power supplies are used

connected resistor (R) to limit current flow to a maximum of 10mA. (Refer to Fig. 12)

● When using differential circuits

When differential circuits are used, it is possible for input voltage to exceed V_{CC} or V_{SS}, which could result in latchup. In this case, use a diode for voltage clamping, combined with a resistor (R) to limit current flow. (Refer to Fig. 13)

● When driving large current circuits

When connecting transistors to CMOS output and operating large current circuits (e.g., relays, motors, etc.) of the same power supply as the CMOS device, coil reactance will produce voltage spikes at switching time. This causes fluctuations in the power supply voltage, which can cause the condition $V_I > V_{CC}$. Where possible, separate power supplies should be used. If a common power supply must be used, power supply impedance must be lowered by connecting a capacitor (0.01~0.22μF) having good frequency characteristics between V_{CC} and V_{SS}.

Current should also be limited by connecting a resistor (R) to input. (Refer to Fig. 14)

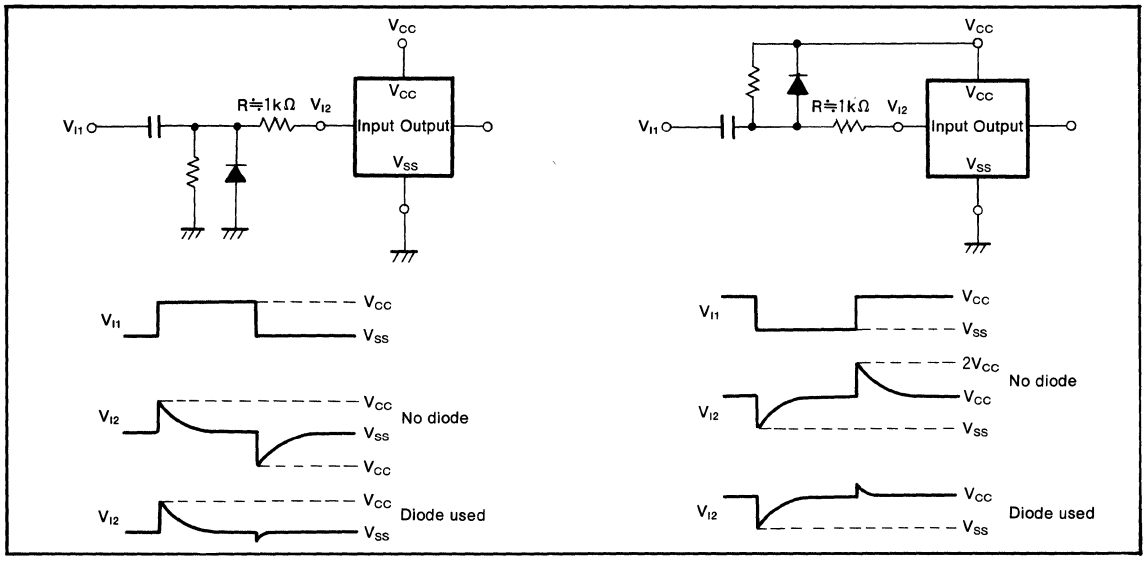


Fig. 13 Preventing latchup when using differential circuits

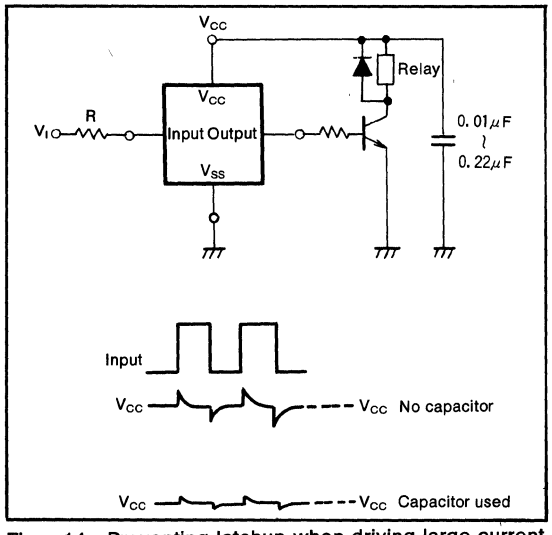


Fig. 14 Preventing latchup when driving large current circuits

Conditions (b) or (d)

Applying a constant voltage to an output pin is not one of the normal usage configurations of a CMOS device, but a capacitor connected between output and V_{CC} (or V_{SS}) would be a cause for latchup. This is due to the high impedance created in the power supply line, combined with the fact that switching the power supply on and off produces fluctuations in the power supply line which causes the capacitor to discharge a trigger current.

Condition (e)

Condition (e) can be created by exceeding the absolute maximum voltage ratings at the V_{CC} pin. Also, even though V_{CC} is within the recommended operating conditions, device latchup can be caused by the surge voltage superimposing at power ON, or crosstalk between lines. The voltage at V_{CC} should never exceed absolute maximum rating values under any circumstances.

Provisions should be made to reduce power ON surge voltage to a minimum, and as described in section 6, a capacitor should be connected beteen V_{CC} and V_{SS} to reduce impedance in the power line.

(4) The differences in CMOS and NMOS peripheral LSIs

The basic characteristics of CMOS devices allow them to be used as replacements for NMOS logic devices without significant modifications. But the fact that improvements have been mode in the characteristics of CMOS devices can cause problems when these devices are used in circuits designed for NMOS. The example below shows such a case.

Transistor drive using a parallel port

Fig. 15 (a) shows an example of an NPN transistor connected in series and being driven by parallel port 8255A. The load R_L and base resistor R_B establishes the operating point as illustrated in Fig. 15 (b).

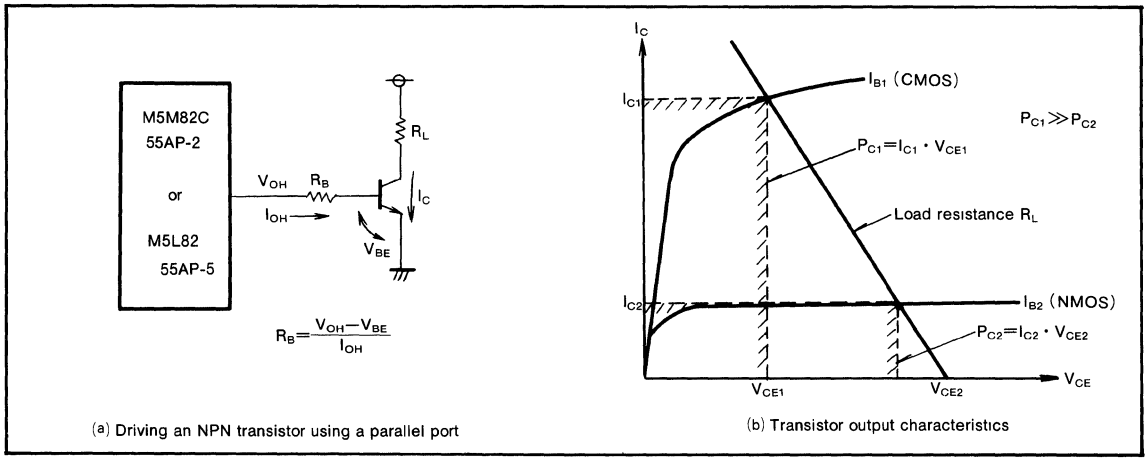


Fig. 15 Driving an NPN transistor using M5L8255AP-5 or M5M82C55AP-2

Fig. 16 illustrates the difference in output characteristics for CMOS and NMOS 8255A devices. As noted, the CMOS 8255A has better drive capability, and provides a higher base current to the transistor. Consequently, dependig on R_B and R_L, power dissipation ratings P_C of the transistor can be exceeded, or drive current may simply be higher than its limit.

The same problem may occur when driving PNP transistors. Fig. 17 shows a comparison in V_{OL} characteristics. But here, the difference between NMOS and CMOS is smaller than for V_{OH}, so the problem should not be as great

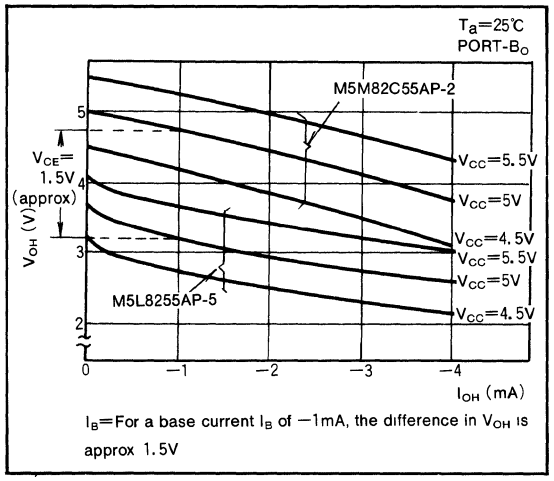


Fig. 16 M5L8255AP-5/M5M82C55AP-2 V_{OH} output characteristics comparison

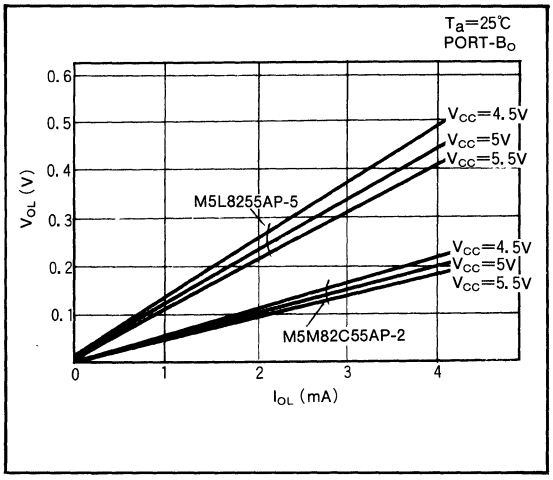


Fig. 17 M5L8255AP-5/M5M82C55AP-2 V_{OL} output characteristics comparison

GMICRO™ M32 FAMILY MICROPROCESSORS

7

MITSUBISHI LSIs

M33210GS-20/FP-20

CMOS 32-BIT PARALLEL MICROPROCESSOR (M32/100)

DESCRIPTION

M33210GS-20/FP-20(M32/100) is a 32-bit microprocessor designed to be cost effective for real memory support. It uses high-level pipeline processing and exception processing (EIT) to achieve a superior processing speed and a high degree of reliability.

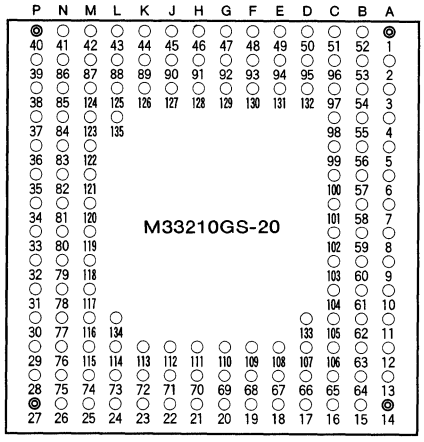
The use of bit map instructions and string instructions allow multi-windowing, while a full range of OS-related instructions and improved addressing modes allow the creation of the optimum operating systems and support for high-level languages.

The ASSP core is being designed to enable the addition of peripheral functions.

FEATURES

- Performance : 7MIPS(20MHz operation)
  Dhrystone : 13k instructions/second
- Number of basic instruction : 92
- Optimized for operating system based on TRON specifications
- 2-level memory access protection
- Bit map processing functions for multi-window displays
- Branch Buffer (small instruction cache capable of selective caching) 256B
- Package : M33210GS-20 135pin PGA
  M33210FP-20 160pin QFP (planning)

PIN CONFIGURATION (BOTTOM VIEW)



Outline 135S8

APPLICATION

I/O controller, Bit map controller.

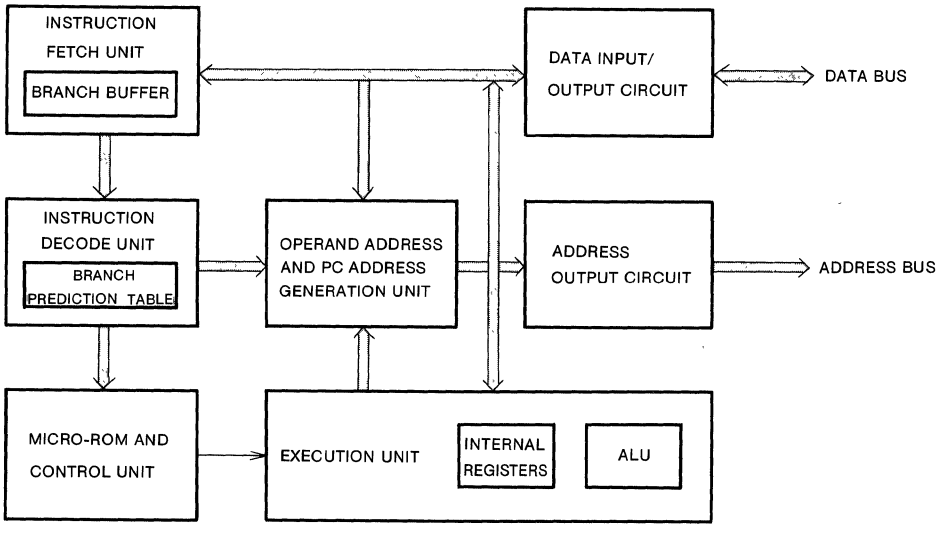
PIN ASSIGNMENT

PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME
A1	1	$\overline{BC_2}$	C1	51	$\overline{BAT_1}$	F1	48	RNG_1	K12	113	D_{15}	N1	41	$\overline{BERR}$
A2	2	A_1	C2	96	$\overline{BC_3}$	F2	93	R/$\overline{W}$	K13	72	D_{12}	N2	86	$\overline{SUSB}$
A3	3	A_4	C3	97	A_2	F3	130	V_{CC}	K14	23	D_{11}	N3	85	V_{CC}
A4	4	A_6	C4	98	V_{CC}	F12	109	V_{SS}	L1	43	V_{CC}	N4	84	$\overline{IRL_1}$
A5	5	A_9	C5	99	A_7	F13	68	D_6	L2	88	$\overline{DS}$	N5	83	$\overline{GBR}$
A6	6	A_{11}	C6	100	A_{10}	F14	19	V_{SS}	L3	125	$\overline{HALT}$	N6	82	*2
A7	7	A_{12}	C7	101	A_{14}	G1	47	V_{CC}	L4	135	V_{SS}	N7	81	$\overline{FLOAT}$
A8	8	V_{CC}	C8	102	*1	G2	92	RNG_0	L11	134	D_{19}	N8	80	V_{SS}
A9	9	A_{16}	C9	103	A_{18}	G3	129	$\overline{LOC}$	L12	114	D_{18}	N9	79	D_{30}
A10	10	A_{19}	C10	104	A_{20}	G12	110	D_7	L13	73	D_{14}	N10	78	D_{28}
A11	11	A_{21}	C11	105	A_{23}	G13	69	D_9	L14	24	V_{CC}	N11	77	D_{26}
A12	12	A_{24}	C12	106	A_{25}	G14	20	D_{10}	M1	42	$\overline{RETRY}$	N12	76	V_{CC}
A13	13	A_{26}	C13	65	D_0	H1	46	V_{SS}	M2	87	$\overline{HACK}$	N13	75	D_{21}
A14	14	A_{28}	C14	16	D_3	H2	91	V_{SS}	M3	124	*2	N14	26	V_{CC}
B1	52	$\overline{BC_1}$	D1	50	$\overline{NCA0}$	H3	128	V_{SS}	M4	123	$\overline{IRL_0}$	P1	40	$\overline{HREQ}$
B2	53	A_0	D2	95	$\overline{BAT_2}$	H12	111	V_{SS}	M5	122	$\overline{IRL_2}$	P2	39	*1
B3	54	A_3	D3	132	V_{SS}	H13	70	V_{SS}	M6	121	*2	P3	38	*2
B4	55	A_5	D11	133	A_{29}	H14	21	V_{CC}	M7	120	V_{SS}	P4	37	V_{CC}
B5	56	A_8	D12	107	V_{SS}	J1	45	V_{SS}	M8	119	V_{CC}	P5	36	V_{SS}
B6	57	V_{SS}	D13	66	V_{CC}	J2	90	V_{CC}	M9	118	V_{SS}	P6	35	*2
B7	58	A_{13}	D14	17	D_5	J3	127	$\overline{IACK}$	M10	117	D_{27}	P7	34	$\overline{RESET}$
B8	59	A_{15}	E1	49	V_{SS}	J12	112	D_{13}	M11	116	D_{25}	P8	33	CLK
B9	60	A_{17}	E2	94	V_{CC}	J13	71	V_{SS}	M12	115	D_{23}	P9	32	D_{31}
B10	61	V_{SS}	E3	131	$\overline{BC_0}$	J14	22	V_{CC}	M13	74	D_{17}	P10	31	D_{29}
B11	62	A_{22}	E12	108	D_2	K1	44	$\overline{BS}$	M14	25	D_{16}	P11	30	V_{CC}
B12	63	V_{CC}	E13	67	D_4	K2	89	$\overline{DC}$				P12	29	D_{24}
B13	64	A_{27}	E14	18	D_8	K3	126	$\overline{AS}$				P13	28	D_{22}
B14	15	D_1										P14	27	D_{20}

*1 : Connect to V_{CC}.
*2 : No connect.

Note. G_{MICRO}™ is a trademark of the G-MICRO group for the TRON specification microprocessors.

BLOCK DIAGRAM



M33220GS-20

CMOS 32-BIT PARALLEL MICROPROCESSOR (M32/200)

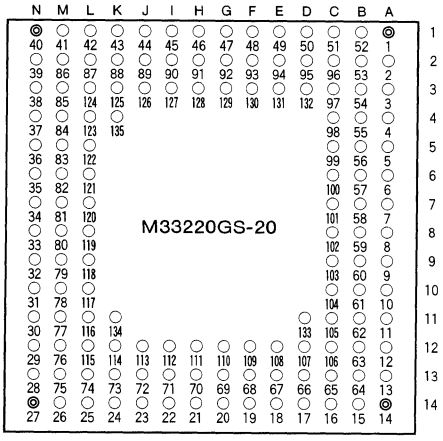
DESCRIPTION

M33220GS-20 (M32/200) is a 32-bit microprocessor with performance in the middle range of the M32 Family.
It has on-chip memory management unit and distributed on-chip caches, and it can high speed operation by advanced pipeline processing.
Rigorous exception-handling facilities provide for error recovery and other system reliability needs. It's instruction set includes bit-map and string-manipulation instructions for fast text and graphics processing.

FEATURES

- Performance : 7MIPS (20MHz operation)
  Dhrystone : 13K instructions/second
- Number of basic instruction : 120
- On-chip cache Instruction cache : 1K byte
  Stack cache : 128 bytes
- Co-processor I/F
- On-chip MMU (TLB 32 entries)
- Optimized for operating system based on TRON specifications
- Supports the industry standard UNIX(Note) operating system
- Virtual memory support
- Memory protection for each page achieved through 2-level paging
- Bit map processing functions for multi-window displays
- Package : 135 pin PGA

PIN CONFIGURATION (BOTTOM VIEW)



Outline 135S8X-A

Note : UNIX operating system was developed by Bell Research Laboratories of AT&T Inc. and is licensed by AT&T.

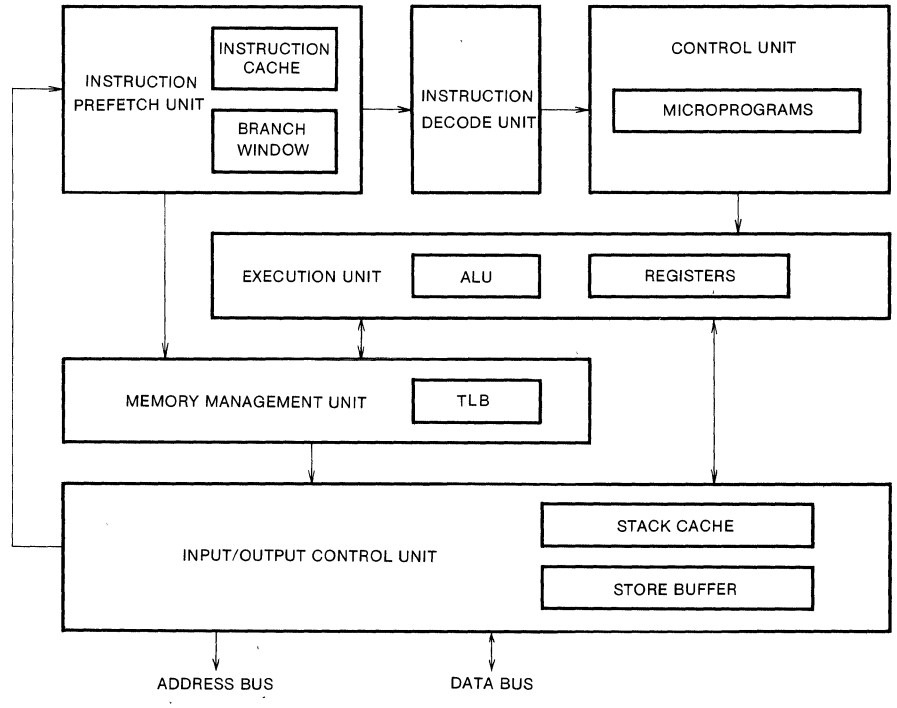
PIN ASSIGNMENT

PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME
A1	1	V_{SS}	C1	51	A_8	F1	48	A_{14}	K12	113	D_{22}	N1	41	A_{26}
A2	2	A_2	C2	96	A_5	F2	93	V_{CC}	K13	72	D_{18}	N2	86	V_{SS}
A3	3	V_{CC}	C3	97	A_1	F3	130	A_9	K14	23	V_{CC}	N3	85	$\overline{IRL_1}$
A4	4	$\overline{BC_2}$	C4	98	$\overline{BC_0}$	F12	109	D_6	L1	43	A_{23}	N4	84	$\overline{HACK}$
A5	5	R/$\overline{W}$	C5	99	$\overline{BC_3}$	F13	68	D_9	L2	88	V_{CC}	N5	83	V_{CC}
A6	6	BAT_2	C6	100	$\overline{LOC}$	F14	19	V_{SS}	L3	125	A_{28}	N6	82	*3
A7	7	BAT_1	C7	101	V_{SS}	G1	47	A_{16}	L4	135	A_{29}	N7	81	*2
A8	8	V_{SS}	C8	102	V_{CC}	G2	92	A_{15}	L11	134	D_{25}	N8	80	CLKf
A9	9	*2	C9	103	$\overline{CDE}$	G3	129	A_{12}	L12	114	D_{24}	N9	79	V_{SS}
A10	10	$\overline{AS_2}$	C10	104	$\overline{CPDC}$	G12	110	D_{10}	L13	73	D_{21}	N10	78	*3
A11	11	V_{CC}	C11	105	$\overline{BERR}$	G13	69	V_{SS}	L14	24	D_{20}	N11	77	*1
A12	12	$\overline{AS_1}$	C12	106	$CPST_1$	G14	20	D_{12}	M1	42	A_{25}	N12	76	V_{CC}
A13	13	$CPST_0$	C13	65	D_2	H1	46	A_{17}	M2	87	$\overline{RESET}$	N13	75	D_{27}
A14	14	V_{SS}	C14	16	V_{CC}	H2	91	V_{SS}	M3	124	$\overline{IRL_0}$	N14	26	V_{SS}
B1	52	V_{SS}	D1	50	A_{11}	H3	128	A_{18}	M4	123	$\overline{PURGE}$	P1	40	V_{SS}
B2	53	A_3	D2	95	A_7	H12	111	D_{16}	M5	122	$\overline{GBR}$	P2	39	A_{27}
B3	54	A_0	D3	132	A_4	H13	70	D_{15}	M6	121	*3	P3	38	$\overline{IRL_2}$
B4	55	$\overline{BC_1}$	D11	133	D_0	H14	21	D_{13}	M7	120	V_{SS}	P4	37	$\overline{HREQ}$
B5	56	$\overline{BS}$	D12	107	D_1	J1	45	V_{SS}	M8	119	V_{CC}	P5	36	*3
B6	57	$\overline{NCA0}$	D13	66	D_5	J2	90	A_{19}	M9	118	*2	P6	35	*3
B7	58	BAT_0	D14	17	D_8	J3	127	A_{22}	M10	117	RNG	P7	34	*2
B8	59	V_{SS}	E1	49	A_{13}	J12	112	D_{19}	M11	116	D_{31}	P8	33	$\overline{CLKf}$
B9	60	$\overline{HALT}$	E2	94	A_{10}	J13	71	D_{17}	M12	115	D_{29}	P9	32	V_{SS}
B10	61	$\overline{RETRY}$	E3	131	A_6	J14	22	D_{14}	M13	74	V_{SS}	P10	31	*1
B11	62	$\overline{DC}$	E12	108	D_4	K1	44	A_{20}	M14	25	D_{23}	P11	30	$\overline{FLOAT}$
B12	63	$CPST_2$	E13	67	D_7	K2	89	A_{21}				P12	29	D_{30}
B13	64	V_{SS}	E14	18	D_{11}	K3	126	A_{24}				P13	28	D_{28}
B14	15	D_3										P14	27	D_{26}

*1 : Connect to V_{SS}. *2 : Connect to V_{CC} *3 : No connect.

Note G_{MICRO}™ is a trademark of the G-MICRO group for the TRON specification microprocessors.

BLOCK DIAGRAM



M33230GS-20

CMOS 32-BIT PARALLEL MICROPROCESSOR (M32/300)

DESCRIPTION

M33230GS-20 (M32/300) is the high-end processor of the three microprocessors. It is a 32-bit microprocessor that not only boasts approximately double the performance of the M33220GS-20 (M32/200), but also includes such additional features as an on-chip cache, MMU functions, and decimal arithmetic instructions.

FEATURES

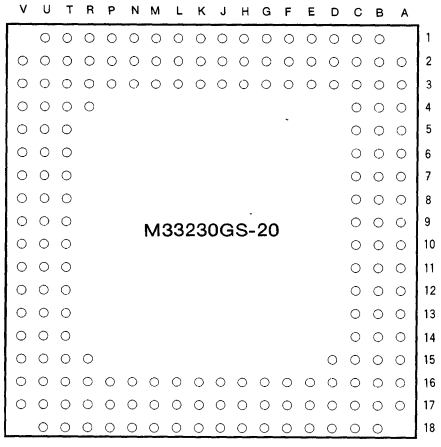
- Performance : 14MIPS (20MHz operation)
  Whetstone : 5MWIPS (20MHz operation with FPU)
  Dhrystone : 27K instructions/second
- Number of basic instruction : about 110
- On-chip cachee Instruction cache : 2K bytes
  Data cache : 2K bytes
- Co-processor I/F
- On-chip MMU (TLB 128 entries)
- Optimized for operating system based on TRON specifications
- Supports the industry standard UNIX (Note) operating system
- Multiple virtual memory support
- Package : 179 pin PGA
- TTL compatible

Note : UNIX operating system was developed by Bell Research Laboratories of AT & T Inc. and is licensed by AT & T.

APPLICATION

Engineering workstation, office workstation and Superminicomputer

PIN CONFIGURATION (BOTTOM VIEW)



Outline 179S8X-B

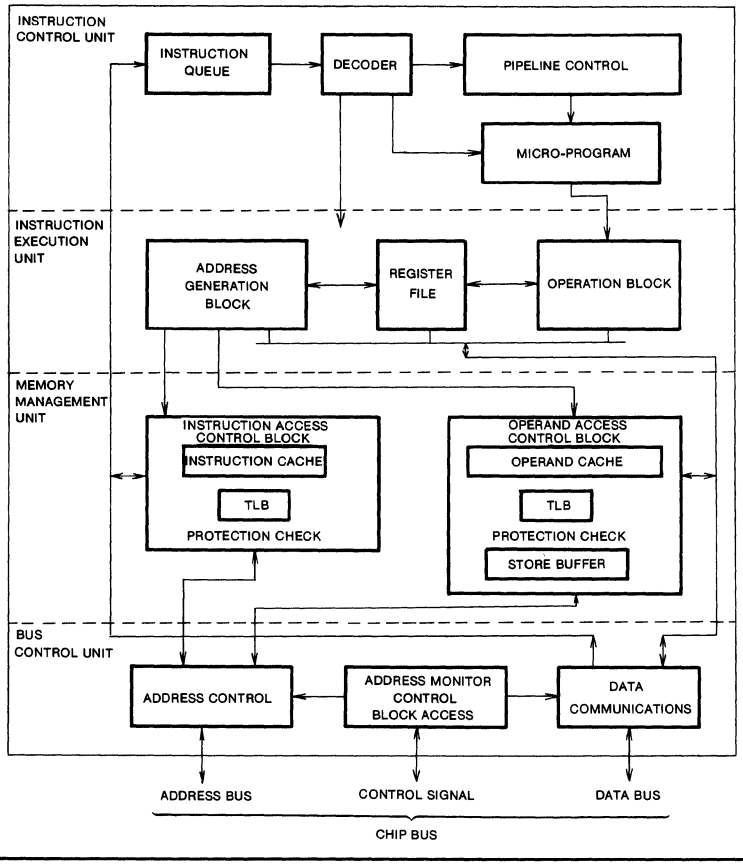
Note G_{MICRO}™ is a trademark of the G-MICRO group for the TRON specification microprocessors

PIN ASSIGNMENT

PIN CODE	NAME	PIN CODE	NAME	PIN CODE	NAME	PIN CODE	NAME	PIN CODE	NAME
A2	*2	C3	V_{SS}	G2	$\overline{FLOAT}$	N2	A_{13}	T18	V_{CC}
A3	$\overline{OCCPRG}$	C4	$\overline{GBR}$	G3	*2	N3	A_{15}	U1	A_{22}
A4	*1	C5	WAY	G16	V_{CC}	N16	V_{SS}	U2	V_{SS}
A5	V_{SS}	C6	V_{CC}	G17	$CPST_0$	N17	A_{29}	U3	V_{CC}
A6	*2	C7	*2	G18	$CPST_1$	N18	A_{30}	U4	D_{30}
A7	$\overline{HACK}$	C8	RNG_1	H1	A_1	P1	A_{14}	U5	D_{28}
A8	V_{SS}	C9	BAT_2	H2	A_0	P2	A_{16}	U6	V_{SS}
A9	BAT_0	C10	V_{SS}	H3	V_{CC}	P3	A_{18}	U7	D_{23}
A10	$\overline{HALT}$	C11	CLKf	H16	$CPST_2$	P16	A_{24}	U8	D_{20}
A11	$\overline{HREQ}$	C12	$\overline{CLKf}$	H17	$\overline{NCA}$	P17	A_{27}	U9	V_{CC}
A12	$\overline{RESET}$	C13	V_{SS}	H18	$\overline{BLACKF}$	P18	A_{28}	U10	V_{CC}
A13	V_{CC}	C14	V_{CC}	J1	A_4	R1	A_{17}	U11	D_{18}
A14	$BCLK_1$	C15	V_{SS}	J2	A_3	R2	V_{SS}	U12	D_{15}
A15	$BCLK_2$	C16	$\overline{L/C}$	J3	A_2	R3	A_{21}	U13	D_{13}
A16	A_{19} V_{SS}	C17	$\overline{BLOCK}$	J16	$\overline{BLACKS}$	R4	V_{CC}	U14	D_{10}
A17	A_{22} $\overline{AS}$	C18	V_{SS}	J17	V_{SS}	R15	V_{SS}	U15	D_8
B1	*2	D1	IRL_0	J18	V_{CC}	R16	D_1	U16	D_7
B2	*2	D2	IRL_1	K1	A_5	R17	A_{25}	U17	D_3
B3	$\overline{ICCPRG}$	D3	*2	K2	V_{SS}	R18	A_{26}	U18	D_2
B4	$\overline{TCS}$	D15	V_{SS}	K3	A_6	T1	A_{19}	V2	V_{CC}
B5	*1	D16	$\overline{DS}$	K16	$\overline{BC_1}$	T2	A_{20}	V3	V_{SS}
B6	V_{CC}	D17	$\overline{RETRY}$	K17	$\overline{BC_2}$	T3	A_{23}	V4	D_{29}
B7	$\overline{DAT}$	D18	$\overline{BERR}$	K18	$\overline{BC_3}$	T4	V_{SS}	V5	D_{26}
B8	RNG_0	E1	*1	L1	A_7	T5	D_{31}	V6	D_{25}
B9	BAT_1	E2	*1	L2	A_8	T6	D_{27}	V7	D_{22}
B10	V_{CC}	E3	IRL_2	L3	A_9	T7	D_{24}	V8	V_{CC}
B11	V_{CC}	E16	V_{CC}	L16	$\overline{NCAO}$	T8	$CPST_2$ D_{21}	V9	V_{SS}
B12	V_{SS}	E17	$\overline{ASDC}$	L17	V_{SS}	T9	V_{SS}	V10	V_{SS}
B13	V_{SS}	E18	$\overline{SDC}$	L18	$\overline{BC_0}$	T10	V_{CC}	V11	D_{19}
B14	*2	F1	*1	M1	A_{10}	T11	D_{17}	V12	D_{16}
B15	V_{CC}	F2	*1	M2	A_{11}	T12	D_{14}	V13	V_{SS}
B16	V_{CC}	F3	*1	M3	V_{CC}	T13	D_{11}	V14	D_{12}
B17	V_{SS} $\overline{BS}$	F16	$\overline{CPDC}$	M16	A_{31}	T14	V_{SS}	V15	D_9
B18	V_{CC} R/$\overline{W}$	F17	V_{CC}	M17	$\overline{MVIN}$	T15	D_6	V16	V_{CC}
C1	V_{CC}	F18	V_{SS}	M18	$\overline{LOC}$	T16	D_4	V17	D_5
C2	V_{SS}	G1	V_{SS}	N1	A_{12}	T17	D_0		

* 1 : Connect to V_{CC}.
* 2 : No connect

BLOCK DIAGRAM



GMICRO™ M32 FAMILY PERIPHERAL CIRCUITS

8

M33241GS

CMOS DMA CONTROLLER (M32/DMAC)

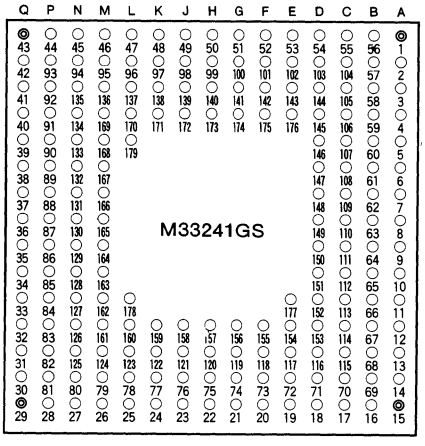
DESCRIPTION

M33241GS (M32/DMAC) is an advanced and high performance DMA controller capable of accessing a 32-bit address space. It has four DMA channels, each of which can be set independently to single or dual address mode, cycle steal or burst mode. Continuous transfer of several blocks by descripter chain is also possible. Data transfer can be performed in units of byte, halfword, or longword. The DMAC can also handle transfer from any bus boundary and transfer between buses of different sizes.

FEATURES

- 4-Channel DMA
- Data transfer is possible between two independent buses
- Communication support function among MPUs on the bus
- The plural block transfer function by sequencial or link descripter chain
- Possible to set the system bus usage
- Transfer by means of auto trigger and external trigger
- Four priority mode
- Maximum transfer speed 27MB/s at 20MHz operation
- Package : 179 pin PGA

PIN CONFIGURATION (BOTTOM VIEW)



Outline 179S8X-A

APPLICATION

DMA control of peripheral equipment that require high-speed data transfer

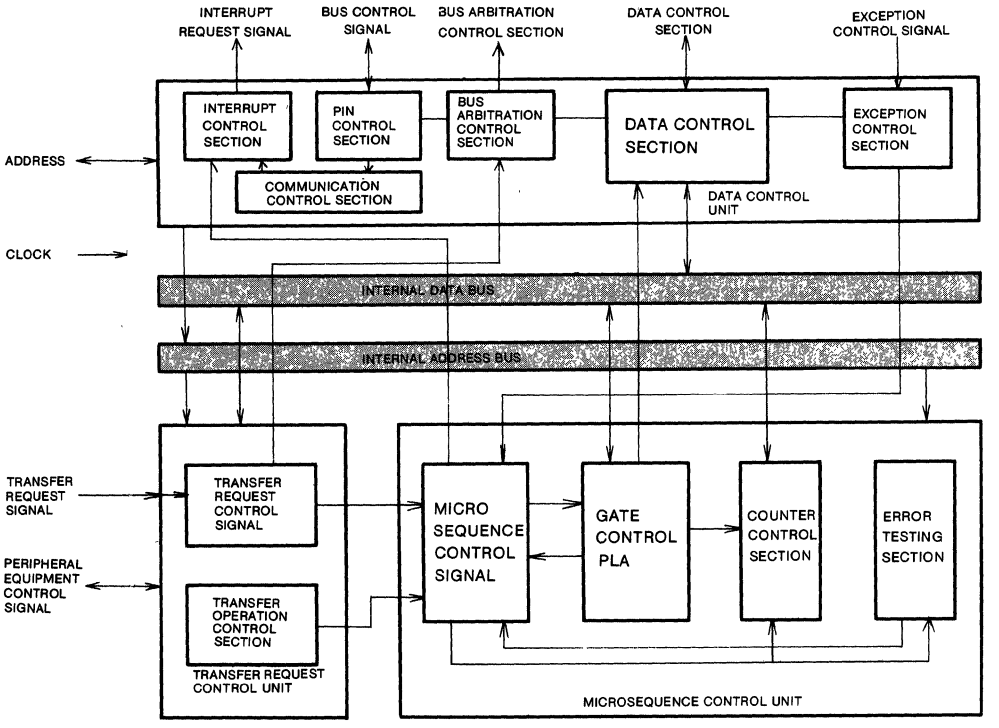
PIN ASSIGNMENT

PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME
A1	1	A_{21}	C1	55	V_{SS}	E1	53	A_{11}	H13	120	$\overline{XABEN}$	M2	95	V_{SS}	P2	93	NC
A2	2	A_{22}	C2	104	A_{16}	E2	102	A_{12}	H14	75	NC	M3	136	V_{SS}	P3	92	V_{CC}
A3	3	A_{25}	C3	105	NC	E3	143	V_{CC}	H15	22	$\overline{ABEN}$	M4	169	D_6	P4	91	D_{11}
A4	4	A_{29}	C4	106	A_{19}	E4	176	A_{14}	J1	49	A_2	M5	168	D_9	P5	90	D_{14}
A5	5	BAT_2	C5	107	A_{23}	E11	177	V_{CC}	J2	98	A_1	M6	167	D_{13}	P6	89	V_{CC}
A6	6	V_{SS}	C6	108	A_{26}	E12	154	$\overline{XIACK}$	J3	139	A_0	M7	166	D_{17}	P7	88	D_{18}
A7	7	$\overline{DC}$	C7	109	BAT_0	E13	117	$\overline{REQ_1}$	J4	172	V_{CC}	M8	165	D_{21}	P8	87	D_{22}
A8	8	$\overline{RERUN}$	C8	110	$\overline{BERR}$	E14	72	V_{CC}	J12	158	$\overline{XHACK}$	M9	164	D_{26}	P9	86	D_{24}
A9	9	$\overline{CSTR}$	C9	111	XR/$\overline{W}$	E15	19	NC	J13	121	$\overline{HACK}$	M10	163	D_{31}	P10	85	D_{28}
A10	10	V_{CC}	C10	112	$\overline{XAS}$	F1	52	A_9	J14	76	V_{SS}	M11	162	*1	P11	84	D_{29}
A11	11	V_{SS}	C11	113	$\overline{ACK_0}$	F2	101	V_{SS}	J15	23	$\overline{DHREQ}$	M12	161	*1	P12	83	V_{SS}
A12	12	$\overline{ACK_1}$	C12	114	$\overline{DBEN}$	F3	142	A_{10}	K1	48	NC	M13	124	*3	P13	82	*1
A13	13	$\overline{ACK_3}$	C13	115	V_{SS}	F4	175	A_{13}	K2	97	$\overline{BC_3}$	M14	79	$\overline{PCL_2}$	P14	81	XWIDTH
A14	14	$\overline{DIN}$	C14	70	$\overline{XCS}$	F12	155	CLK	K3	138	V_{SS}	M15	26	$\overline{PCL_1}$	P15	28	WIDTH
A15	15	$\overline{IACK}$	C15	17	$\overline{REQ_3}$	F13	118	V_{SS}	K4	171	$\overline{BC_1}$	N1	45	$\overline{BC_0}$	Q1	43	D_2
B1	56	A_{17}	D1	54	V_{SS}	F14	73	V_{CC}	K12	159	V_{CC}	N2	94	D_3	Q2	42	D_7
B2	57	V_{SS}	D2	103	V_{CC}	F15	20	V_{SS}	K13	122	$\overline{XHREQ}$	N3	135	D_4	Q3	41	D_{10}
B3	58	A_{20}	D3	144	A_{15}	G1	51	A_6	K14	77	$\overline{HREQ}$	N4	134	D_8	Q4	40	V_{SS}
B4	59	A_{24}	D4	145	A_{18}	G2	100	V_{CC}	K15	24	$\overline{DHACK}$	N5	133	D_{12}	Q5	39	D_{15}
B5	60	A_{27}	D5	146	V_{CC}	G3	141	A_7	L1	47	V_{SS}	N6	132	V_{SS}	Q6	38	D_{16}
B6	61	A_{28}	D6	147	V_{SS}	G4	174	A_8	L2	96	$\overline{BC_2}$	N7	131	NC	Q7	37	D_{19}
B7	62	$\overline{BLOCK}$	D7	148	BAT_1	G12	156	V_{CC}	L3	137	V_{CC}	N8	130	D_{20}	Q8	36	V_{SS}
B8	63	$\overline{XDC}$	D8	149	$\overline{IORDY}$	G13	119	V_{SS}	L4	170	D_1	N9	129	D_{25}	Q9	35	D_{23}
B9	64	R/$\overline{W}$	D9	150	$\overline{DONE}$	G14	74	V_{CC}	L5	179	D_5	N10	128	D_{30}	Q10	34	V_{CC}
B10	65	$\overline{AS}$	D10	151	$\overline{XDS}$	G15	21	$\overline{XAIN}$	L11	178	*1	N11	127	$\overline{RESET}$	Q11	33	D_{27}
B11	66	$\overline{DS}$	D11	152	V_{SS}	H1	50	A_5	L12	160	V_{SS}	N12	126	*1	Q12	32	V_{SS}
B12	67	$\overline{ACK_2}$	D12	153	$\overline{XDIN}$	H2	99	V_{SS}	L13	123	$\overline{PCL_0}$	N13	125	NC	Q13	31	V_{CC}
B13	68	$\overline{XDBEN}$	D13	116	$\overline{CS}$	H3	140	A_4	L14	78	$\overline{XIRQ}$	N14	80	*2	Q14	30	*3
B14	69	NC	D14	71	$\overline{REQ_2}$	H4	173	A_3	L15	25	$\overline{IRQ}$	N15	27	$\overline{PCL_3}$	Q15	29	*1
B15	16	$\overline{REQ_0}$	D15	18	V_{SS}	H12	157	$\overline{AIN}$	M1	46	V_{CC}	P1	44	D_0			

*1 : Connect to V_{SS}
*2 : Connect to V_{CC}
*3 : No connect

Note. G_{MICRO}™ is a trademark of the G-MICRO group for the TRON specification microprocessors.

BLOCK DIAGRAM



DESCRIPTION

M33242SP/J (M32/IRC) is an interrupt request controller (IRC). It controls local and bus interrupts and interrupt vectors in a system based on the G_{MICRO} family MPU (M33210GS-20/FP-20, M33220GS-20, M33230GS-20).
It comprises both the IRG (Interrupt Request Generator) that processes external interrupt requests, and the IRH (Interrupt Request Handler) that processes interrupts from several IRGs.
It can also be used with a VME bus.

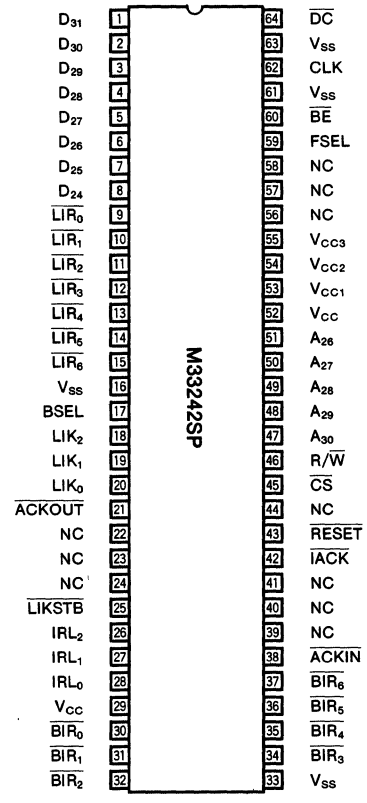
FEATURES

- Seven local interrupts and seven bus interrupts (only IRH)
- Cause of interrupt can be expanded
- Fast interrupt acknowledge daisychain
- Interrupt Generator (IRG) function and Interrupt Handler (IRH) function
- M32/IRC can be used with M32 family bus or VME bus
- Interrupt conditions can be set with each interrupt input
- Interrupt polling is possible
- No initialization required after a reset, immediate recovery to interrupt handling ready condition
- Irregular interrupts can be handled
- Maximum operation frequency : 20MHz
- Package : M33242SP 64pin shrink DIP
  M33242J 68pin PLCC

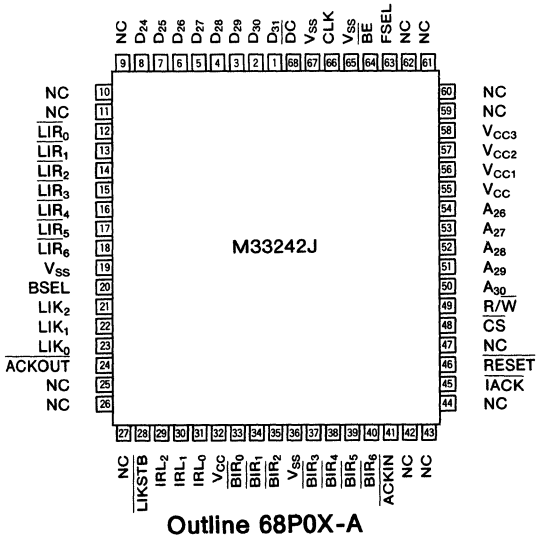
APPLICATION

Interrupt controller for M32 family

PIN CONFIGURATION (TOP VIEW)



Outline 64P4X-A

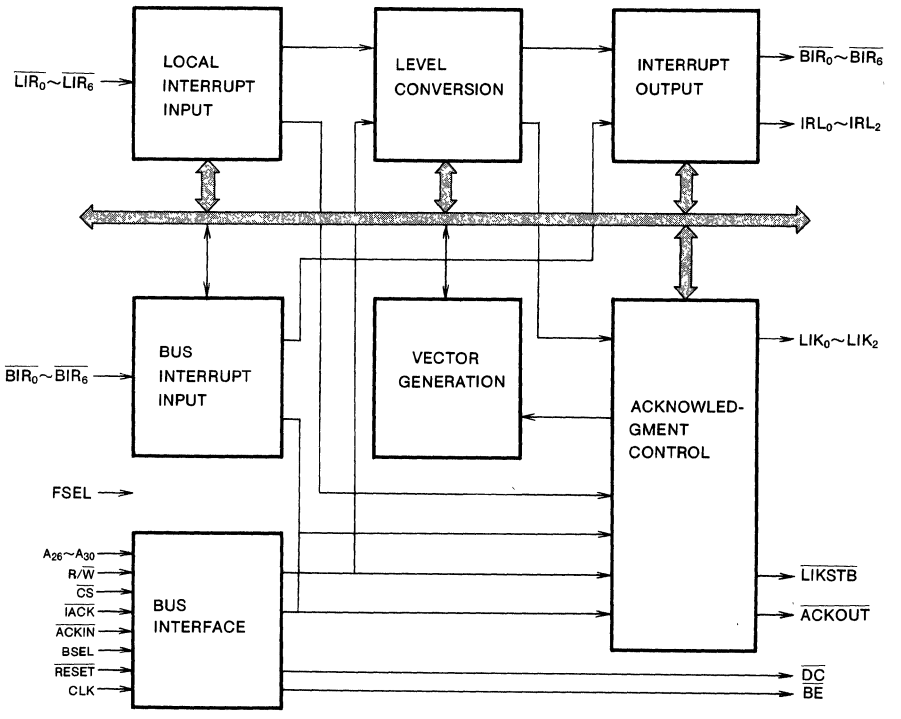


Outline 68P0X-A

NC : NO CONNECTION

Note. G_{MICRO}™ is a trademark of the G-MICRO group for the TRON specification microprocessors.

BLOCK DIAGRAM



M33243GS-25,-30

CMOS TAG MEMORY (M32/TAGM)

DESCRIPTION

M33243GS-25, -30 (M32/TAGM) is 512 entry × 4 way /1024 entry × 2 way TAG Memory fabricated with a CMOS technology.

It has been developed aiming to be used in an easily handled cache system with the other DATA RAMs. Especially this device offers the advantages on designing compact and high performance cache system which will be used in a system adopting M32 family microprocessors.

FEATURES

Parameter \ Type		M33243GS-25	M33243GS-30
Maximum access time(ns)	from address	25	30
	from TAG data	18	18

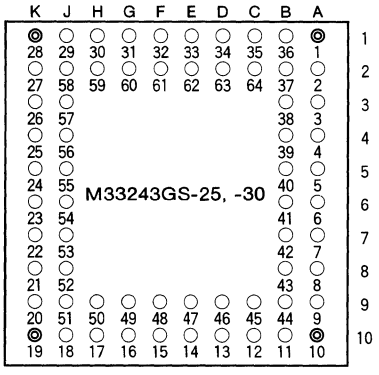
FEATURES

- 512 entry × 4 way or 1024 entry × 2 way by external pin selection
- Internal RAM configured as 512 words × 98 bits
- LRU (Least Recently Used) replace control
- Partial purge and full purge functions
- Internal parity generation and check circuit
- Tag data comparison control function
- Coded hit/replace output pin
- Package : 64pin PGA

APPLICATION

High performance cache memory system

PIN CONFIGURATION (BOTTOM VIEW)



Outline 64S8X-A

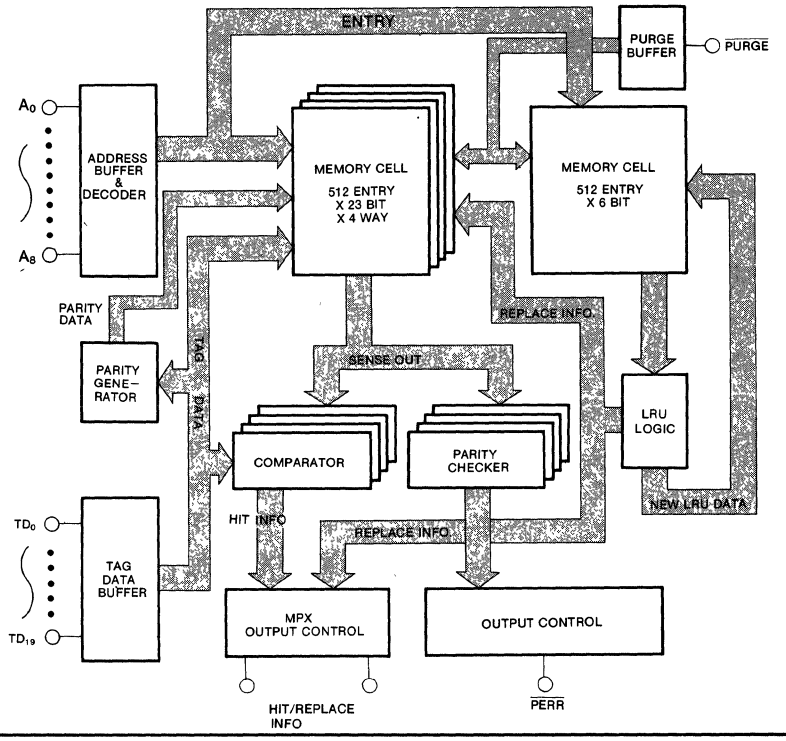
PIN ASSIGNMENT

PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME
A1	1	NC	C9	45	TD_6	J1	29	$\overline{PINV}$
A2	2	$\overline{MHIT}$	C10	12	TD_8	J2	58	MODE
A3	3	HIT_0/REP_0	D1	34	$\overline{SET}$	J3	57	$\overline{PURGE}$
A4	4	HIT_2/REP_2	D2	63	RLATCH	J4	56	A_8
A5	5	HIT_3/REP_3	D9	46	TD_9	J5	55	A_6
A6	6	TD_0	D10	13	TD_{10}	J6	54	V_{SS}
A7	7	TD_2	E1	33	$\overline{INVL}$	J7	53	A_2
A8	8	EXTH	E2	62	$\overline{WRITE}$	J8	52	A_0
A9	9	MHENBL	E9	47	V_{CC}	J9	51	TD_{19}
A10	10	NC	E10	14	TD_{11}	J10	18	TD_{18}
B1	36	$\overline{HIT}$	F1	32	$\overline{INH}$	K1	28	NC
B2	37	HC_0/RC_0	F2	61	V_{CC}	K2	27	NC
B3	38	HC_1/RC_1	F9	48	TD_{13}	K3	26	A9
B4	39	HIT_1/REP_1	F10	15	TD_{12}	K4	25	A7
B5	40	V_{SS}	G1	31	SB_1	K5	24	A5
B6	41	TD_1	G2	60	SB_0	K6	23	A4
B7	42	TD_3	G9	49	TD_{15}	K7	22	A3
B8	43	TD_4	G10	16	TD_{14}	K8	21	A1
B9	44	TD_5	H1	30	SBLK	K9	20	NC
B10	11	TD_7	H2	59	$\overline{VINV}$	K10	19	NC
C1	35	H/R	H9	50	TD_{17}			
C2	64	$\overline{PERR}$	H10	17	TD_{16}			

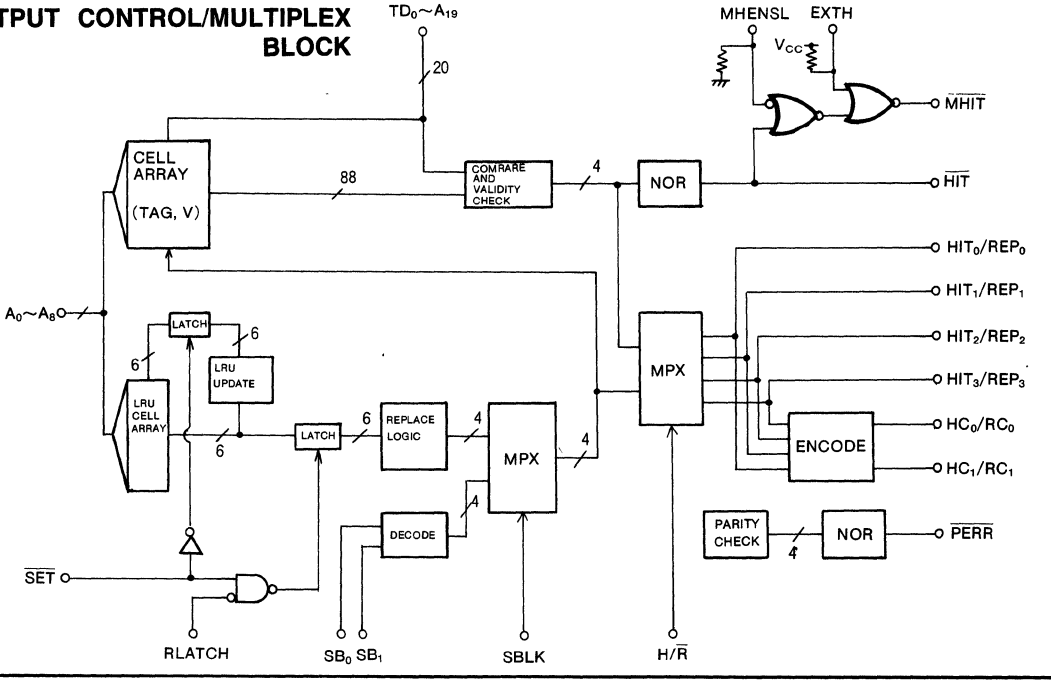
* 1 : Connect to V_{CC}
* 2 : No connect

Note. G_{MICRO}™ is a trademark of the G-MICRO group for the TRON specification microprocessors.

BLOCK DIAGRAM



OUTPUT CONTROL/MULTIPLEX BLOCK



MITSUBISHI ELECTRIC

M33244T-16,-20

CLOCK PULSE GENERATOR FOR M32/200 (CPG/200)

DESCRIPTION

M33244T-16, -20 (CPG/200) is a Clock Pulse Generator for supporting M33220GS-20 (M32/200) systems. With its reset control function, it adjusts MPU and FPU internal clock phases.

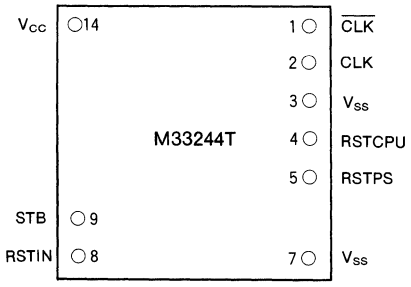
FEATURES

- Clock pulse generator for M32/200 systems
- Maximum system clock frequency is 20MHz
- Reset signal output with ability to adjusts MPU and FPU internal clock phases
- Reset timing generator for power-on reset
- Monitor output to system shows MPU and FPU internal clock phases
- Package : 14pin can type

APPLICATION

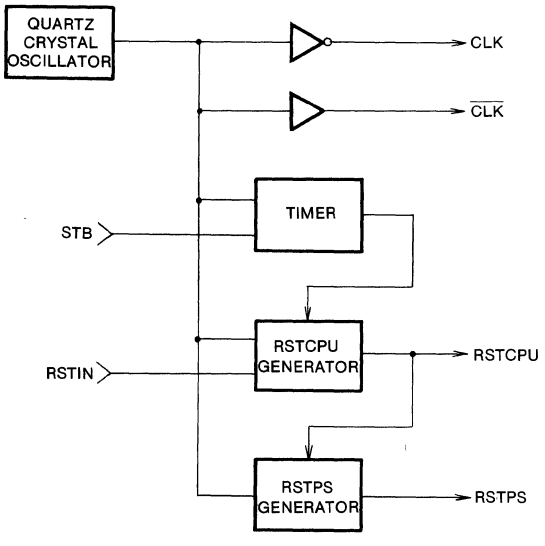
Clock pulse generator for M32/200

PIN CONFIGURATION (BOTTOM VIEW)



Outline 14T4X-A

BLOCK DIAGRAM



Note. G_{MICRO}™ is a trademark of the G-MICRO group for the TRON specification microprocessors.

DESCRIPTION

M33245GS (M32/CCM) is a cache controller/memory for M32 family microprocessors (M33210GS-20, M33220GS-20, M33230GS-20).
It improves the MPU's average memory access time.

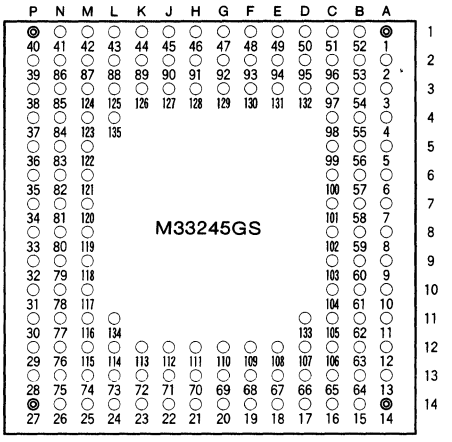
FEATURES

- 16kB real address external cache
- No wait reads possible when the cache is hit
- Fast 4 words burst read when the cache is missed
- Fully synchronous operation with M32 family processors
- Internal address comparator allows multiple usage
- Division into data cache and instruction cache
- Coherency maintained by address monitor
- Purge and freeze functions in way units
- Write-through main memory replace
- 4-way set associative cache
- LRU (Least Recently Used) replace control
- Each line consists of 4 words (16 bytes) and a validity bit
- Package : 135 pin PGA

APPLICATION

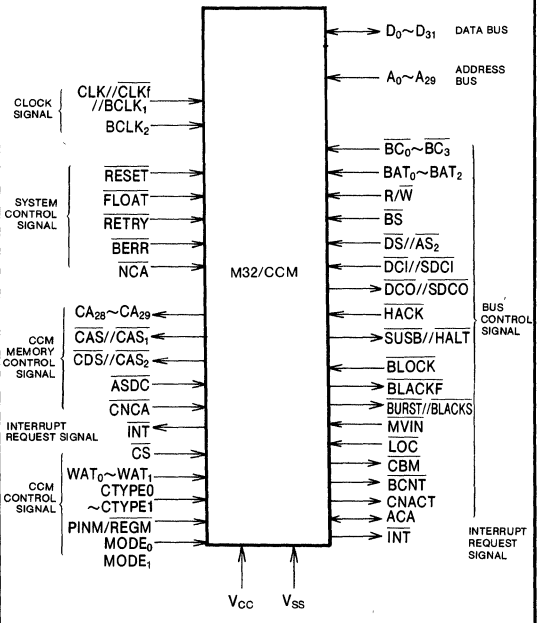
High performance cache memory system

PIN CONFIGURATION (BOTTOM VIEW)



Outline 135S8

PIN FUNCTION



// : Multi function
Change by mode ($MODE_0$~$MODE_1$)

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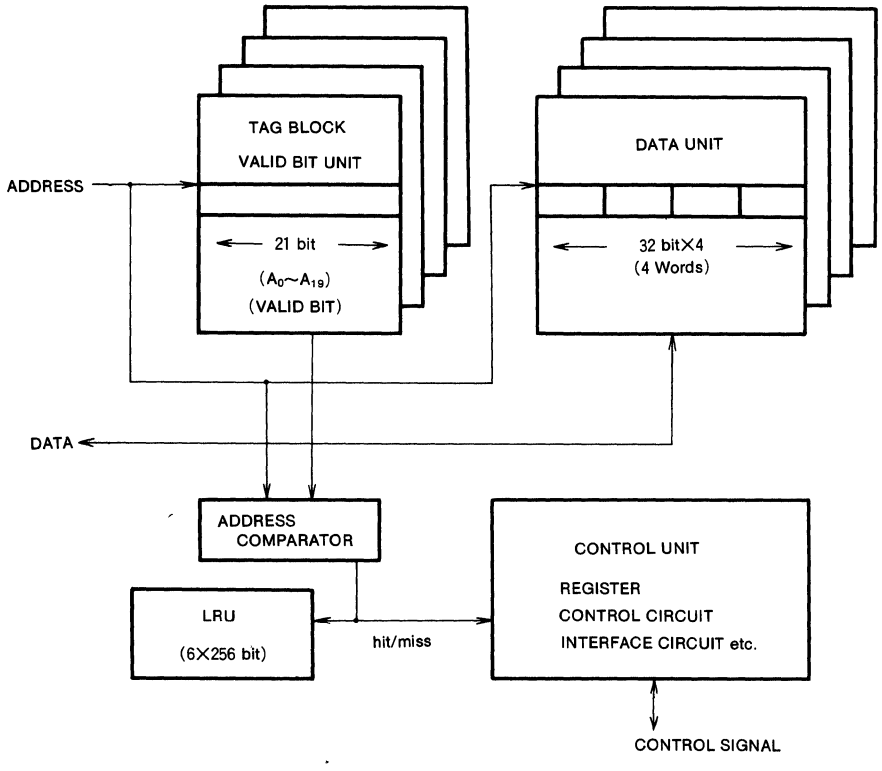
BLOCK DIAGRAM



M33281GS-20

CMOS FLOATING-POINT PROCESSING UNIT (M32/FPU)

DESCRIPTION

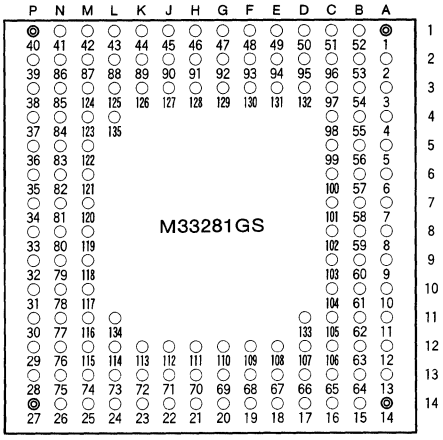
M33281GS-20 is a high-speed floating-point arithmetic LSI unit, and support the extended precision data format of IEEE standard.

The M33281GS-20 is designed to give maximum performance as a coprocessor for M32 family microprocessors (M33220GS-20, M33230GS-20). In addition to arithmetic operations and square roots, it has elementary function instructions, inner product instructions for fast matrix and vector calculations, area discrimination instructions for clipping discrimination, graphics oriented instructions and many more.

FEATURES

- Performance (20MHz operation with M33220GS-20)
  - Addition or subtraction 0.5μs
  - Multipulication 0.45μs
  - Division 1.5μs
- Elementary function calculation
- Graphics support
- Conforms to IEEE754
- Fast coprocessor interface
- Comprehensive system functions
- Softwave and system support
- Variety of instruction types
  - 31 arithmetic related
  - 21 control related
- 16 floating point operation registers (80-bit)

PIN CONFIGURATION (BOTTOM VIEW)



Outline 135S8X-A

- Peripheral device mode specifiable (for use when MPU lacks coprocessor interface)
- Package 135 pin PGA

APPLICATION

Scientific and technical calculations, engineering diagram processing

PIN ASSIGN

PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME
A1	1	V_{SS}	B10	61	$\overline{CPDC}$	D12	107	D_{16}	H3	128	D_{10}	L14	24	V_{CC}	N9	79	V_{SS}
A2	2	A_{29}	B11	62	$\overline{BERR}$	D13	66	D_{19}	H12	111	V_{CC}	M1	42	V_{SS}	N10	78	V_{CC}
A3	3	$\overline{HACK}$	B12	63	$CPST_2$	D14	17	V_{CC}	H13	70	V_{SS}	M2	87	$FCPST_1$	N11	77	V_{CC}
A4	4	$\overline{BC_2}$	B13	64	V_{SS}	E1	49	V_{CC}	H14	21	V_{CC}	M3	124	LD	N12	76	V_{CC}
A5	5	$R/\overline{W}$	B14	15	V_{CC}	E2	94	D_3	J1	45	D_9	M4	123	$CPID_1$	N13	75	V_{SS}
A6	6	BAT_0	C1	51	V_{CC}	E3	131	D_0	J2	90	D_{11}	M5	122	$\overline{IRL}$	N14	26	V_{SS}
A7	7	V_{SS}	C2	96	V_{CC}	E12	108	D_{18}	J3	127	D_{13}	M6	121	V_{SS}	P1	40	V_{CC}
A8	8	NC	C3	97	A_{28}	E13	67	D_{21}	J12	112	D_{29}	M7	120	V_{SS}	P2	39	$\overline{RESET}$
A9	9	V_{SS}	C4	98	$\overline{BC_0}$	E14	18	D_{23}	J13	71	D_{27}	M8	119	V_{CC}	P3	38	$CPID_0$
A10	10	V_{SS}	C5	99	$\overline{BC_3}$	F1	48	D_6	J14	22	D_{26}	M9	118	V_{CC}	P4	37	V_{SS}
A11	11	V_{CC}	C6	100	V_{SS}	F2	93	D_4	K1	44	V_{SS}	M10	117	V_{CC}	P5	36	SIZ16
A12	12	V_{SS}	C7	101	BAT_2	F3	130	D_2	K2	89	D_{12}	M11	116	V_{CC}	P6	35	NC
A13	13	$CPST_0$	C8	102	V_{CC}	F12	109	D_{20}	K3	126	D_{15}	M12	115	V_{CC}	P7	34	V_{CC}
A14	14	V_{CC}	C9	103	V_{CC}	F13	68	V_{CC}	K12	113	D_{30}	M13	74	V_{CC}	P8	33	CLKf
B1	52	V_{SS}	C10	104	$\overline{RETRY}$	F14	19	V_{SS}	K13	72	D_{28}	M14	25	D_{31}	P9	32	V_{SS}
B2	53	V_{CC}	C11	105	$\overline{DC}$	G1	47	V_{SS}	K14	23	V_{SS}	N1	41	$FCPST_2$	P10	31	$\overline{FCPDC}$
B3	54	A_{27}	C12	106	$CPST_1$	G2	92	D_7	L1	43	V_{CC}	N2	86	V_{SS}	P11	30	V_{CC}
B4	55	$\overline{BC_1}$	C13	65	D_{17}	G3	129	D_5	L2	88	D_{14}	N3	85	UD	P12	29	V_{CC}
B5	56	$\overline{BS}$	C14	16	V_{SS}	G12	110	D_{22}	L3	125	V_{SS}	N4	84	$CPID_2$	P13	28	NC
B6	57	V_{CC}	D1	50	V_{SS}	G13	69	D_{24}	L4	135	V_{CC}	N5	83	V_{CC}	P14	27	V_{CC}
B7	58	BAT_1	D2	95	D_1	G14	20	D_{25}	L11	134	$FCPST_0$	N6	82	V_{CC}			
B8	59	V_{SS}	D3	132	V_{SS}	H1	46	D_8	L12	114	V_{SS}	N7	81	V_{SS}			
B9	60	$\overline{CDE}$	D11	133	V_{SS}	H2	91	D_{10}	L13	73	V_{SS}	N8	80	$\overline{CLKf}$			

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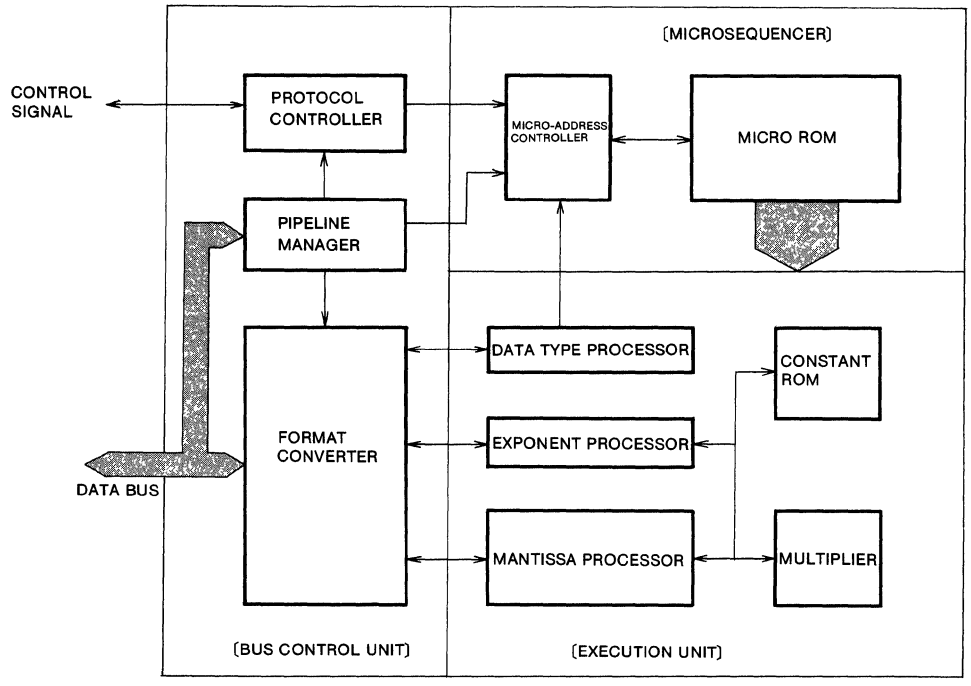
BLOCK DIAGRAM



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