1985 MITSUBISHI SEMICONDUCTOR BIPOLAR DIGITAL IC ALSTTL

MITSUBISHI ELECTRIC

# MITSUBISHI SEMICONDUCTORS 1985

## BIPOLAR DIGITAL IC
## ALSTTL

DATA BOOK

MITSUBISHI ELECTRIC

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** Under development

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# TYPE DESIGNATION TABLE

## ALSTTL SERIES TYPE DESIGNATION TABLE

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## INDEX BY FUNCTION (Recommended operating conditions $V_{CC} = 5V \pm 10\%$, $T_{opr} = -20 \sim +75°C$)

### INVERTERS, NAND GATES/BUFFERS

| Circuit function | Type of output: Active pull-up | Type of output: Open collector | Type | Typical electrical characteristics: Propagation time (ns) | Typical electrical characteristics: Power dissipation (mW) | Typical electrical characteristics: Low-level output current (mA) | Typical electrical characteristics: High-level output current (mA) | Package Outlines | Page |
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| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Quadruple 2-input Positive AND Gate/Buffer | ○ | — | M74ALS08P | 6 | 8.8 | 8 | 0.4 | 14P4 | 2-15 |
| | ○ | — | M74ALS1008P | 6.5 | 16.5 | 24 | 2.6 | 14P4 | 2-228 |
| | — | ○ | M74ALS09P | 14.5 | 8.9 | 8 | — | 14P4 | 2-17 |
| Triple 3-input Positive AND Gate/Buffer | ○ | — | M74ALS11P | 6.5 | 6.5 | 8 | 0.4 | 14P4 | 2-21 |
| | ○ | — | M74ALS1011P | 8 | 12.5 | 24 | 2.6 | 14P4 | 2-232 |
| | — | ○ | M74ALS15P | 14.5 | 6.7 | 8 | — | 14P4 | 2-25 |
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| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Quadruple 2-input Positive NOR Gate/Buffer | ○ | — | M74ALS02P | 5.5 | 7.6 | 8 | 0.4 | 14P4 | 2-7 |
| | ○ | — | M74ALS28P | 5 | 16.3 | 24 | 2.6 | 14P4 | 2-35 |
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| | — | ○ | M74ALS33P | 15.5 | 16.3 | 24 | — | 14P4 | 2-41 |
| Triple 3-input Positive NOR Gate | ○ | — | M74ALS27P | 6.5 | 7.4 | 8 | 0.4 | 14P4 | 2-33 |

### OR GATE/BUFFER

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Quadruple 2-input Positive OR Gate/Buffer | ○ | — | M74ALS32P | 6.5 | 11.3 | 8 | 0.4 | 14P4 | 2-39 |
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## LINE DRIVERS

| Circuit function | Type of output | | Type | Typical electrical characteristics | | | | Package Outlines | Page |
|---|---|---|---|---|---|---|---|---|---|
| | 3-state | Open collector | | Propagation time (ns) | Power dissipation (mW) | Low-level output current (mA) | High-level output current (mA) | | |
| Octal Buffer/Line Driver | I | — | M74ALS240P | 6 | 56.7 | 24 | 15 | 20P4 | 2-90 |
| | I | — | M74ALS1240P | 7.5 | 41.6 | 16 | 15 | 20P4 | 2-238 |
| | N | — | M74ALS241P | 7 | 70 | 24 | 15 | 20P4 | 2-93 |
| | N | — | M74ALS1241P | 9 | 51.7 | 16 | 15 | 20P4 | 2-241 |
| | N | — | M74ALS244P | 7 | 70 | 24 | 15 | 20P4 | 2-102 |
| | N | — | M74ALS1244P | 9 | 51.7 | 16 | 15 | 20P4 | 2-250 |
| Octal Bus Transceiver | N | — | M74ALS245P | 7 | 173 | 24 | 15 | 20P4 | 2-105 |
| | N | — | M74ALS645P | 7 | 173 | 24 | 15 | 20P4 | 2-197 |
| | N | — | M74ALS1245P | 9 | 113 | 16 | 15 | 20P4 | 2-253 |
| | N | — | M74ALS1645P | 9 | 113 | 16 | 15 | 20P4 | 2-283 |
| | I | — | M74ALS620P | 5 | 117 | 24 | 15 | 20P4 | 2-170 |
| | I | — | M74ALS1620P | 6.5 | 95 | 16 | 15 | 20P4 | 2-256 |
| | — | N | M74ALS621P | 20 | 143 | 24 | — | 20P4 | 2-173 |
| | — | N | M74ALS1621P | 25.5 | 113 | 16 | — | 20P4 | 2-259 |
| | — | N | M74ALS622P | 18 | 58 | 24 | — | 20P4 | 2-176 |
| | — | N | M74ALS1622P | 25.5 | 48 | 16 | — | 20P4 | 2-262 |
| | N | — | M74ALS623P | 7 | 160 | 24 | 15 | 20P4 | 2-179 |
| | N | — | M74ALS1623P | 9 | 115 | 16 | 15 | 20P4 | 2-265 |
| | I | — | M74ALS640P | 5 | 123 | 24 | 15 | 20P4 | 2-182 |
| | I | — | M74ALS1640P | 6 | 95 | 16 | 15 | 20P4 | 2-268 |
| | — | N | M74ALS641P | 21 | 145 | 24 | — | 20P4 | 2-185 |
| | — | N | M74ALS1641P | 26.5 | 103 | 16 | — | 20P4 | 2-271 |
| | — | I | M74ALS642P | 18.5 | 57 | 24 | — | 20P4 | 2-188 |
| | — | I | M74ALS1642P | 25 | 48 | 16 | — | 20P4 | 2-274 |
| | I・N | — | M74ALS643P | 6 | 155 | 24 | 15 | 20P4 | 2-191 |
| | I・N | — | M74ALS1643P | 7 | 108 | 16 | 15 | 20P4 | 2-277 |
| | — | I・N | M74ALS644P | 19 | 103 | 24 | — | 20P4 | 2-194 |
| | — | I・N | M74ALS1644P | 23 | 90 | 16 | — | 20P4 | 2-280 |
| Quadruple Bus Transceiver | I | — | M74ALS242P | 6 | 65 | 24 | 15 | 14P4 | 2-96 |
| | I | — | M74ALS1242P | 7.5 | 48.3 | 16 | 15 | 14P4 | 2-244 |
| | N | — | M74ALS243P | 8 | 83 | 24 | 15 | 14P4 | 2-99 |
| | N | — | M74ALS1243P | 9 | 60 | 16 | 15 | 14P4 | 2-247 |

I: With inverted output  N: With noninverted output  I・N: With both inverted and noninverted output

# INDEX BY FUNCTION

## J-K FLIP-FLOPS

| Circuit function | Type | Typical electrical characteristics | | | | Trigger | Preset | Reset | Package Outlines | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Operating frequency (MHz) | Setup time (ns) | Hold time (ns) | Power dissipation (mW) | | | | | |
| Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop with Set and Reset | M74ALS109P | 0~40 | 15 | 5 | 12 | ↑ | ⊔ | ⊔ | 16P4 | 2-52 |
| Dual J-K Negative Edge-Triggered Flip-Flop with Set and Reset | M74ALS112AP | 0~40 | 22 | 0 | 12.5 | ↓ | ⊔ | ⊔ | 16P4 | 2-55 |
| Dual J-K Negative Edge-Triggered Flip-Flop with Set | M74ALS113AP | 0~40 | 22 | 0 | 12.5 | ↓ | ⊔ | — | 14P4 | 2-58 |
| Dual J-K Negative Edge-Triggered Flip-Flop with Set, Common Reset, and Common Clock | M74ALS114AP | 0~40 | 22 | 0 | 12.5 | ↓ | ⊔ | ⊔ | 14P4 | 2-61 |

↑ : Positive-going edge ↓ : Negative-going edge ⊔ : Active low-level

## D-Type FLIP-FLOPS

| Circuit function | Type | Typical electrical characteristics | | | | Trigger | Preset | Reset | Package Outlines | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Operating frequency (MHz) | Setup time (ns) | Hold time (ns) | Power dissipation (mW) | | | | | |
| Dual D-Type Positive Edge-Triggered Flip-Flop with Set and Reset | M74ALS74P | 0~40 | 15 | 5 | 12 | ↑ | ⊔ A | ⊔ A | 14P4 | 2-49 |
| Octal D-Type Edge-Triggered Flip-Flop with 3-State Output (Inverted) | M74ALS564P | 0~50 | 10 | 0 | 68.3 | ↑ | — | — | 20P4 | 2-134 |
| Octal D-Type Edge-Triggered Flip-Flop with 3-State Output (Noninverted) | M74ALS574P | 0~50 | 20 | 0 | 68.3 | ↑ | — | — | 20P4 | 2-153 |
| Octal D-Type Edge-Triggered Flip-Flop with 3-State Output (Inverted) | M74ALS576P | 0~50 | 15 | 0 | 68.3 | ↑ | — | — | 20P4 | 2-160 |
| Octal D-Type Edge-Triggered Flip-Flop with 3-State Output and Synchronous Reset (Noninverted) | M74ALS575P | 0~50 | 15 | 0 | 68.3 | ↑ | — | ⊔ S | 24P4D | 2-156 |
| Octal D-Type Edge-Triggered Flip-Flop with 3-State Output and Synchronous Reset (Inverted) | M74ALS577P | 0~50 | 15 | 0 | 68.3 | ↑ | — | ⊔ S | 24P4D | 2-163 |
| Dual 4-Bit D-Type Edge-Triggered Flip-Flop with 3-State Output (Noninverted) | M74ALS874P | 0~50 | 10 | 0 | 86.7 | ↑ | — | ⊔ A | 24P4D | 2-204 |
| Dual 4-Bit D-Type Edge-Triggered Flip-Flop with 3-State Output (Inverted) | M74ALS876P | 0~50 | 10 | 0 | 86.7 | ↑ | — | ⊔ A | 24P4D | 2-208 |
| Dual 4-Bit D-Type Edge-Triggered Flip-Flop with 3-State Output and Synchronous Reset (Noninverted) | M74ALS878P | 0~50 | 20 | 0 | 86.7 | ↑ | — | ⊔ S | 24P4D | 2-212 |
| Dual 4-Bit D-Type Edge-Triggered Flip-Flop with 3-State Output and Synchronous Reset (Inverted) | M74ALS879P | 0~50 | 20 | 0 | 86.7 | ↑ | — | ⊔ S | 24P4D | 2-215 |

↑ : Positive-going edge A : Asynchronous S : Synchronous ⊔ : Active low-level

# INDEX BY FUNCTION

## LATCHES

| Circuit function | Type | Typical electrical characteristics | | | | | Enable | Reset | Package Outlines | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Propagation time (ns) | | Setup time (ns) | Hold time (ns) | Power dissipation (mW) | | | | |
| | | From enable input | From data input | | | | | | | |
| Octal D-Type Transparent Latch with 3-State Output (Inverted) | M74ALS563P | | | 10 | 10 | 68.3 | ⎍ | — | 20P4 | 2-130 |
| Octal D-Type Transparent Latch with 3-State Output (Inverted) | M74ALS580P | | | 10 | 10 | 68.3 | ⎍ | — | 20P4 | 2-166 |
| Octal D-Type Transparent Latch with 3-State Output (Noninverted) | M74ALS573P | 14 | 8.5 | 10 | 7 | 68.3 | ⎍ | — | 20P4 | 2-149 |
| Dual 4-Bit D-Type Transparent Latch with 3-State Output (Noninverted) | M74ALS873P | | | 10 | 7 | 68.3 | ⎍ | ⎎ | 24P4D | 2-200 |
| Dual 4-Bit D-Type Transparent Latch with 3-State Output (Inverted) | M74ALS880P | | | 15 | 10 | 88.3 | ⎍ | ⎎ | 24P4D | 2-218 |

⎍ : Active high-level ⎎ : Active low-level

## SHIFT REGISTERS

| Circuit function | Type | Typical electrical characteristics | | Reset | Operating mode | | | | Package outline | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Shift frequency (MHz) | Power dissipation (mW) | | Right shift | Left shift | Parallel load | Hold | | |
| 8-Bit Universal Shift/Storage Register with 3-State Output | M74ALS299P | 0~35 | 100 | A | ○ | ○ | ○ | ○ | 20P4 | 2-108 |
| | M74ALS323P | 0~35 | 100 | S | ○ | ○ | ○ | ○ | 20P4 | 2-113 |

## SYNCHRONOUS COUNTERS

| Circuit function | Type | Typical electrical characteristics | | Trigger | Parallel load | Reset | Package Outlines | Page |
|---|---|---|---|---|---|---|---|---|
| | | Count frequency (MHz) | Power dissipation (mW) | | | | | |
| Synchronous Presettable Decade Counter with Direct Reset | M74ALS160AP | 0~50 | 60 | ⎎ | S | A | 16P4 | 2-74 |
| Fully Synchronous Presettable Decade Counter | M74ALS162AP | 0~40 | 60 | ⎎ | S | S | 16P4 | 2-82 |
| Synchronous Presettable Decade Counter with 3-State Output | M74ALS560AP | 0~30 | 100 | ⎎ | A. S | A. S | 20P4 | 2-118 |
| Synchronous Presettable Up/Down Decade Counter with 3-State Output | M74ALS568AP | 0~40 | 93.3 | ⎎ | S | A. S | 20P4 | 2-137 |
| Synchronous Presettable 4-Bit Binary Counter with Direct Reset | M74ALS161AP | 0~50 | 60 | ⎎ | S | A | 16P4 | 2-78 |
| Fully Synchronous Presettable 4-Bit Binary Counter | M74ALS163AP | 0~40 | 60 | ⎎ | S | S | 16P4 | 2-86 |
| Synchronous Presettable 4-Bit Binary Counter with 3-State Output | M74ALS561AP | 0~40 | 100 | ⎎ | A. S | A. S | 20P4 | 2-124 |
| Synchronous Presettable Up/Down 4-Bit Binary Counter with 3-State Output | M74ALS569AP | 0~40 | 93.3 | ⎎ | S | A. S | 20P4 | 2-143 |

⎎ : Positive-going edge A : Asynchronous S : Synchronous

# INDEX BY FUNCTION

## DECODERS/DEMULTIPLEXERS

| Circuit function | Type | Typical power dissipation (mW) | Typical propagation time (ns) | | | Package Outlines | Page |
|---|---|---|---|---|---|---|---|
| | | | From enable input to output (ns) | From data input to output (ns) | From clock to output (ns) | | |
| 3-Line to 8-Line Decoder/Demultiplexer with Address Register | M74ALS131P | 25 | 8.5 | — | 12 | 16P4 | 2-64 |
| 3-Line to 8-Line Decoder/Demultiplexer with Address Latch | M74ALS137P | 25 | 10 | 11 | — | 16P4 | 2-68 |
| 3-Line to 8-Line Decoder/Demultiplexer | M74ALS138P | 25 | 10 | 11 | — | 16P4 | 2-71 |

## SYMBOLOGY

| Symbol | Descriptions | |
|---|---|---|
| $C_L$ | Load capacitance | Extenally connected load capacitance |
| $f_{max}$ | Maximum clock frequency | Maximum input repetition frequency for normal IC operation |
| $F_I$ | Fan-in | Number of similar inputs |
| $F_O$ | Fan-out | Number of similar ICs which can be driven by an output |
| H | Indicates the high logic level | Used in voltage and current suffixes to indicate the high potential level |
| I | Indicates current or input | Currents flowing into ICs are taken to be positive and those flowing out as negative |
| $I_{CC}$ | Supply current | The current flowing into the $V_{CC}$ supply terminal of a circuit |
| $I_{CCL}$ | Low-level supply current | $V_{CC}$ current when the inputs are such that the output is low |
| $I_{CCH}$ | High-level supply current | $V_{CC}$ current when the inputs are such that the output is high |
| $I_{CCZ}$ | High-impedance supply current | $V_{CC}$ current when the inputs are such that the output is in the high-impedance state |
| $I_F$ | Forward current | Forward diode current |
| $I_I$ | Input current at maximum voltage | The input current flowing when maximum voltage is applied to the IC input pins |
| $I_{IH}$ | High-level input current | The current flowing into an input when a specified high voltage is applied |
| $I_{IL}$ | Low-level input current | The current flowing out of an input when a specified low voltage is applied |
| $I_O$ | Output current | The current flowing at an output when that output is high-level and 2 25V is applied |
| $I_{OH}$ | High-level output current | Current flowing in the load when the output is high or current flowing when a high level is applied |
| $I_{OL}$ | Low-level output current | The current flowing into an output which is in the low state |
| $I_{OS}$ | Short-circuit output current | The current flowing out of an output which is in the high state when that output is short circuit to ground |
| $I_{OZH}$ | Off-state high-level output current | The current flowing into a disabled 3-state output with a specified high output voltage applied |
| $I_{OZL}$ | Off-state low-level output current | The current flowing out of a disabled 3-state output with a specified low output voltage applied |
| $I_T$ | Threshold current | Current which flows when the threshold voltage is applied to the input |
| $I_{T+}$ | Positive threshold current | Current which flows when the positive threshold voltage is applied to the input |
| $I_{T-}$ | Negative threshold current | Current which flows when the negative threshold voltage is applied to the input |
| L | Indicates the low logic level | Used in voltage and current suffixes to indicate the low potential level |
| O | Indicates output | |
| Pd | Power dissipation | Product of the supply voltage and the supply current |
| PRR | Pulse repetition rate | The rate of repetition of an applied pulse train |
| Ta | Operating free-air temperature | The temperature of the environment surrounding an IC |
| $t_f$ | Falltime | Time required to fall from the high to the low logic level |
| $t_h$ | Hold time | The required hold time for a specified input after an input has changed |
| $t_{latch}$ | Latch time | The time from the latching action of input data until the data appears in the output |
| Topr | Operating temperature | The ambient temperature range for normal IC operation |
| $t_{pd}$ | Propagation delay time | Amount of time required from a change of input signal until the corresponding change in output, expressed as the average propagation time |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | Amount of time required from a change of input signal until the output changes from high to low |
| $t_{PHZ}$ | Output disable time from High level | Amount of time required from a change of input signal until the output changes from high to high-impedance |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | Amount of time required from a change of input signal until the output changes from low to high |
| $t_{PLZ}$ | Output disable time from Low level | Amount of time required from a change of input signal until the output changes from low to high-impedance |
| $t_W$ | Pulse width | The time required for a pulse to change from one specified level to another |
| $t_{WO}$ | Output pulse width | The width of the pulse appearing in the output of a monostable multivibrator |
| $t_{PZH}$ | Output enable time to a High level | Amount of time required from a change of input signal until the output changes from high-impedance to high |
| $t_{PZL}$ | Output enable time to a Low level | Amount of time required from a change of input signal until the output changes from high-impedance to low |
| tr | Risetime | Time required to rise from the low to the high logic level |
| Tstg | Storage temperature | The range of surrounding storage temperature for an IC |
| $t_{SU}$ | Setup time | The required hold time for other inputs before a particular input may be changed |
| $V_{CC}$ | Supply voltage | The voltage of power supply voltage over which the device is guaranteed to operate within the specified limits |

# SYMBOLOGY

| Symbol | Descriptions | |
|---|---|---|
| $V_{BE}$ | Base-emitter voltage | |
| $V_F$ | Forward voltage | Forward voltage applied to a diode |
| $V_I$ | Input voltage | Voltage applied to an input |
| $V_{IC}$ | Input clamp diode voltage | The forward voltage applied to an input clamping diode |
| $V_{IE}$ | Input emitter-emitter voltage | The emitter-to-emitter voltage for a multi-emitter transistor input |
| $V_{IH}$ | High-level input voltage | The range of input voltages that represents a logic high in the system |
| $V_{IL}$ | Low-level input voltage | The range of input voltages that represents a logic low in the system |
| $V_O$ | Output voltage | Voltage applied to or appearing at an output |
| $V_{OH}$ | High-level output voltage | Voltage at an output in the high state |
| $V_{OL}$ | Low-level output voltage | Voltage at an output in the low state |
| $V_P$ | Pulse amplitude | The difference between the low level and high level of a pulse |
| $V_T$ | Threshold voltage | The input voltage beyond at which the output changes |
| $V_{T+}$ | Positive-going threshold voltage | The threshold voltage at which the output changes when the input is changing from low to high |
| $V_{T-}$ | Negative-going threshold voltage | The threshold voltage at which the output changes when the input is changing from high to low |
| Z | Indicates the off state | Indicates that the output is in the high-impedance state |
| $Z_O$ | Output impedance | The load impedance which should be connected to such devices as pulse generators |

## INTRODUCTION

User demands for higher speeds and lower power dissipation in standard logic ICs has resulted in increased use of LSTTL (Low Power Schottky TTL) moving away from TTL (Transistor Transistor Logic). However, demands for even higher speeds and lower power dissipation increased, and in response, Mitsubishi Electric has begun marketing the next generation of TTL ICs, the ALSTTL (Advanced Low Power Schottky TTL). When completed, the full line up will consist of approximately 200 devices.

This section will explain the process, basic circuit, and electrical characteristics of ALSTTL devices.

## 1. ALSTTL PROCESSING

The increased speed and decreased power dissipation of the ALSTTL is mostly achieved through improved production process.

While decreased power dissipation can be obtained by increasing resistance, it also results in slower operating time, i.e., propagation time. Propagation time is the amount of time necessary for charging and discharging parasitic capacitance within the IC, and is proportional to the product of resistance and parasitic capacitance. Thus, improved propagation time is directly related to decreases in the amount of parasitic capacitance.

When compared to the LSTTL, both increased speed and decreased power dissipation were achieved in the ALSTTL by using the following processing.

- Saturation control circuit using Schottky barrier diodes. (increases speed)
- Higher resistance. (decreases power dissipation)
- Oxide film separation. (decreases parasitic capacitance)
- Increased pattern fineness. (decreases parasitic capacitance)

This process results in the surface area of the ALSTTL transistor becoming approximately 1/5 that of the LSTTL. Fig. 1 shows the cross section and top view of the typical LSTTL transistor. Fig. 2 shows the cross section and top view of the typical ALSTTL transistor. While the horizontal and vertical proportions shown in the figures differ from the actual devices, the proportion between the two figures reflect their actual differences.

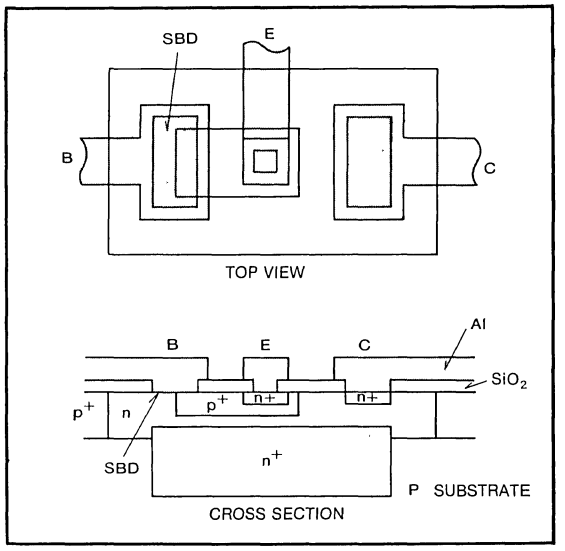



**Fig. 1 Configuration of the typical LSTTL transistor**

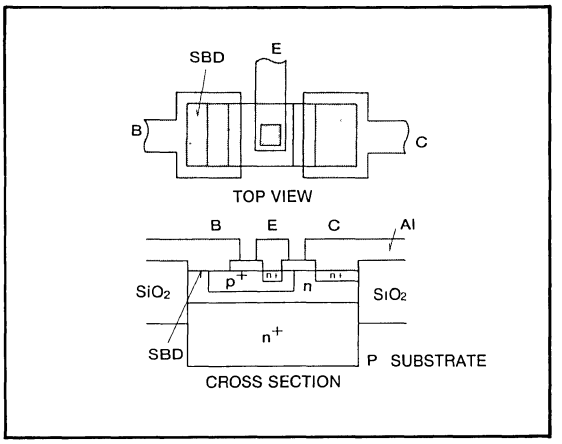



**Fig. 2 Configuration of the typical ALSTTL transistor**

## 2. BASIC CIRCUIT

By making improvements on the circuitry of the LSTTL, the ALSTTL has improved threshold voltage and capacitive load drive capability, increased input impedance, and decreased input and output signal undershooting.

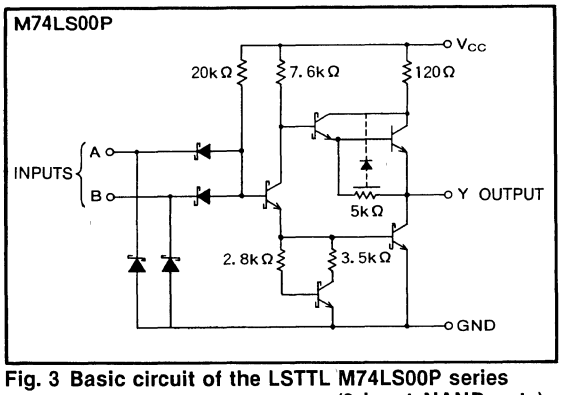



**Fig. 3 Basic circuit of the LSTTL M74LS00P series (2 input NAND gate)**

The basic LSTTL circuit is shown in Fig. 3 and the basic ALSTTL circuit in Fig. 4. Compared with LSTTL, $T_1 \sim T_3$, $D_5$ and $D_6$ are added to ALSTTL, and its resistances are higher except $R_4$.

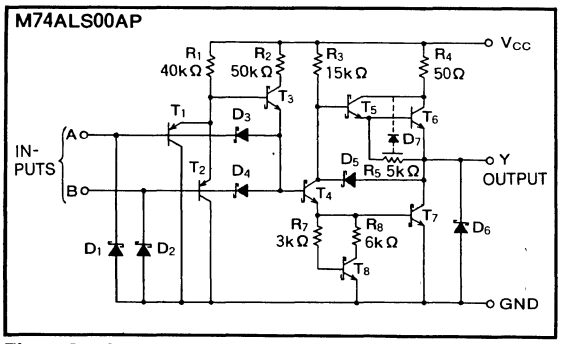



**Fig. 4 Basic circuit of the ALSTTL M74ALS00P series (2 input NAND gate)**

Improved threshold voltage and decreased low-level input current were obtained by adding the input pnp transistors $T_1 \sim T_2$. This decrease, along with the increased resistance of $R_1$, results in a typical low-level input current of 20$\mu$A, 1/10 that of the LSTTL circuit.

$D_3$ and $D_4$ quickly discharge the base charge of $T_4$ when the input changes from high to low.

The addition of $D_5$ and the decrease of $R_4$ increase the switching speed and particularly lower capacitive load charge/discharge time. The effect of $D_5$ is seen when the output changes from high to low. When $T_4$ is turned on, a portion of the charge in capacitive load flows from the output through $D_5$ and $T_4$ to the base of $T_7$ becoming its base current, and the current, amplified by a factor of $h_{FE}$, flows into the collector of $T_7$ rapidly discharging the capacitive load.

When the output changes from low to high, a large high-level output current flows, due to the small value of $R_4$, quickly charging the capacitive load. But this high capacitive load driving capability demands careful design because current spike in voltage supply is bigger than LSTTL and, moreover, the IC may be damaged if a voltage source is connected to the output.

Clamp diode $D_6$ is used to moderate undershooting in the output. Clamp diodes are used in both the input and the output in ALSTTLs offering easier application.

Except $R_4$ the resistive value of the ALSTTL is about twice that of the LSTTL, providing a power dissipation of approximately 1/2 that of the LSTTL. However, low-level output current is ensured to be the equivalent of the LSTTL with the use of transistors with higher $h_{FE}$.

The maximum rating of output voltage is $V_{CC}$ due to the flow of the current from the output through $R_5$, $D_7$, and $R_4$ to $V_{CC}$. (This is not true of 3-state outputs.) Input voltage is determined by the breakdown voltage of $D_1 \sim D_4$ ordinarily and, with few exceptions, is guaranteed up to 7V.

The threshold voltage $V_T$ of the ALSTTL basic circuit is derived using the following formula.

$$V_T = V_{BE}(T_7) + V_{BE}(T_4) + V_{BE}(T_3) - V_{EB}(T_1, T_2) \quad \cdots\cdots\cdots (1)$$

Where
$V_{BE}(T_7)$: Base-emitter voltage of $T_7$
$V_{BE}(T_4)$: Base-emitter voltage of $T_4$
$V_{BE}(T_3)$: Base-emitter voltage of $T_3$
$V_{EB}(T_1, T_2)$: Emitter-base voltage of $T_1$ or $T_2$

The value of formula (1) is higher than the threshold voltage of LSTTL by a forward voltage drop of SBD (Schottky Barrier Diode). It means that a standard ALSTTL gate has a large margin for low-level input voltage 0.8V even at $T_a = 75°C$. Fig. 5 shows the transfer function of TTL, LSTTL and ALSTTL gate. Fig. 6 shows the temperature-dependency of ALSTTL transfer function.

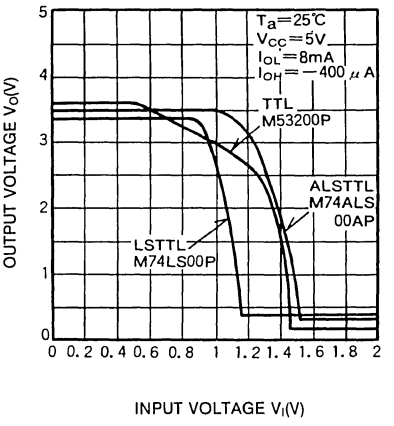



Fig. 5 Input vs. output voltage characteristics comparison

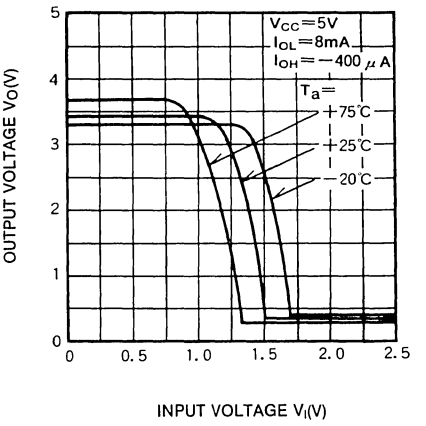



Fig. 6 Temperature-dependent input vs. output voltage characteristics

## 3. ELECTRICAL CHARACTERISTICS

The electrical characteristics achieved by the ALSTTL are shown in Table 1.

As can be seen, compared to the LSTTL, the ALSTTL has superior characteristics with 2/3 propagation time, 3/5 the amount of power dissipation, and 0.3V higher threshold voltage.

These ALSTTL devices, with their supply voltage of $V_{CC} = 5V \pm 10\%$ and wide operating temperature range of $T_{opr} = -20 \sim +75°C$ in which the direct current characteristics and switching characteristics are guaranteed, offer easy application and satisfying performance.

**Table 1. Electrical characteristics of the ALSTTL, LSTTL, and TTL**

| Parameter \ Series name | | ALSTTL (M74ALS00AP) | LSTTL (M74LS00P) | TTL (M53200P) |
|---|---|---|---|---|
| Propagation time (typical) | $t_{PLH}$ | 5ns | 6ns | 12ns |
| | $t_{PHL}$ | 3ns | 6ns | 8ns |
| Power dissipation (typical) | $P_d$ | 1.25mW/Gate | 2mW/Gate | 10mW/Gate |
| Threshold voltage (typical) | $V_T$ | 1.4V | 1.1V | 1.4V |
| High-level output voltage (minimum) | $V_{OH}$ | 2.6V/2.7V (Note 1) | 2.7V | 2.4V |
| Low-level output voltage (maximum) | $V_{OL}$ | 0.4V/0.5V | 0.4V/0.5V | 0.4V |
| High-level input current (maximum) | $I_{IH}$ | 20μA | 20μA | 40μA |
| Low-level input current (maximum) | $I_{IL}$ | −0.1mA | −0.4mA | −1.6mA |
| Operating supply voltage | $V_{CC}$ | 4.5~5.5V | 4.75~5.25V | 4.75~5.25V |
| Necessary conditions to guarantee propagation performance | $T_a$ | −20~+75℃ | 25℃ | 25℃ |
| | $V_{CC}$ | 4.5~5.5V | 5V | 5V |
| | $C_L$ | 50pF | 15pF | 15pF |

Note 1. We guarantee 2.6V at −20~+75°C, 2.7V at 0~70°C.

# DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

## INTRODUCTION

This section will serve to define and describe those important specifications which must be observed in using ALSTTL and to provide information on test methods for these ratings and standard characteristics of the basic gate circuits.

## 1. ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are the maximum ratings which should not be exceeded for the devices' reliability. When there are several ratings, none should be exceeded, even momentarily. If the device is used beyond these ratings, reliability will be significantly lowered and the IC may be destroyed. The following types of absolute maximum ratings are specified.

(1)Supply voltage ($V_{CC}$)
(2)Input voltage ($V_I$)
(3)Output voltage ($V_O$)
(4)Operating temperature range ($T_{opr}$)
(5)Storage temperature range ($T_{stg}$)

Particular care is required with respect to these ratings as exceeding even one of these could cause IC damage.

### 1-1 Supply voltage ($V_{CC}$)

This rating indicates the maximum value of supply voltage that may be applied to the $V_{CC}$ terminal. This value is also applied to the maximum value of surge voltage under unusual conditions. If voltage beyond this rating is applied, the IC may either be destroyed or its reliability significantly deteriorated.

### 1-2 Input voltage ($V_I$)

This rating indicates the maximum value of input voltage that may be applied. Exceeding this value may cause the transistors and diodes in the input circuit to be destroyed and the IC made useless.

### 1-3 Output voltage ($V_O$)

This rating indicates the maximum value of voltage that can be applied to the output when the output is high-level. When the device has open collector outputs, this value indicates the breakdown voltage of the output transistor.

### 1-4 Operating temperature range ($T_{opr}$)

This rating indicates the temperature range in which the device can be operated with all electrical specifications satisfied and full function. The ALSTTL is guaranteed over a broad temperature range of $-20 \sim +75°C$.

### 1-5 Storage temperature range ($T_{stg}$)

This rating indicates the temperature range in which the IC may be stored without either voltage or current applied. This should not be exceeded in storage nor transport (particularly for transport by air).

## 2. RECOMMENDED OPERATING CONDITIONS

In recommended operating conditions we specify supply voltage and input/output conditions required for the guaranteed performance of the device.

### 2-1 Supply voltage ($V_{CC}$)

This rating specifies the permissible supply voltage range. Normally, optimum supply voltage is 5V in TTLs. The permissible supply voltage range of the ALSTTL has a maximum value of 5.5V ($V_{CCmax}$) and a minimum value of 4.5V ($V_{CCmin}$).

### 2-2 High-level input voltage ($V_{IH}$)

This rating specifies the voltage value applied to the input terminal when it is in high-level condition. The minimum value is specified for TTLs, while the maximum value is the absolute maximum rating of the input voltage. The minimum value is sometimes referred to as $V_{IH}$.

### 2-3 Low-level input voltage ($V_{IL}$)

This rating specifies the voltage value applied to the input terminal when it is in low-level condition. The maximum value is specified for TTLs. This maximum value is sometimes referred to as $V_{IL}$.

### 2-4 High-level output current ($I_{OH}$)

The meaning of high-level output current differs depending on whether the type of output is active pull-up or open collector.

When the output is an active pull-up, then high-level output current is the stipulated maximum value of the current that can be output from the output terminal with the high-level voltage guaranteed when the output is high-level.

This value is related to the number of inputs that can be driven by one output when that output is high-level. For details, see the section entitled "PRECAUTIONS FOR USE."

When the output is an open collector, $I_{OH}$ is the maximum current guaranteed in the "ELECTRICAL CHARACTERISTICS." See 4-3.

### 2-5 Low-level output current ($I_{OL}$)

Low-level output current is the stipulated maximum value of current that may be applied to the output terminal with low-level output voltage guaranteed when the output is low-level. This value is related to the number of inputs that can be driven by one output when that output is low-level. For details, see the section entitled "PRECAUTIONS FOR USE."

## 3. FUNCTIONS

The functions of devices are specified by either a function table or timing diagrams. A check of functions is undertaken with the supply voltage at $V_{CCmax}$ and $V_{CCmin}$, the input voltage set to $V_{IL}$ and $V_{IH}$, signals ap-

plied to the input terminal according to either the function table or the timing diagram, and the criterion $V_{OL}$ and $V_{OH}$ used for observation of the output.

**4. ELECTRICAL CHARACTERISTICS**

These characteristics are guaranteed within the specified temperature range and supply voltage range of $V_{CCmin}$ to $V_{CCmax}$. The test methods are specified to realize the worst case to guarantee the ratings.

**4-1 Input clamp voltage ($V_{IC}$)**

This specifies the voltage at input terminal when a specified current is applied to the terminal. This voltage is the forward voltage drop of the clamp diode connected between the input and GND. With supply voltage set at $V_{CCmin}$ and all other input terminals open, clamp voltage $V_{IC}$ is measured when specified current $I_{IC}$ is applied to the input terminal.

**4-2 High-level output voltage ($V_{OH}$)**

This specification is applicable to ICs with active pull-up outputs.

This specifies the minimum value of voltage guaranteed in an output terminal of high-level. With supply voltage at $V_{CCmin}$ and input conditions set so that output becomes high-level, $V_{OH}$ is the voltage when load current $I_{OH}$ flows from the output terminal.

**4-3 High-level output current ($I_{OH}$)**

This specification is applicable to ICs with open collector outputs.

This is the maximum value of current that flows into the output terminal when output voltage $V_O$ is applied to the output terminal and the output is high-level. Supply voltage is set $V_{CCmin}$ at this time.

**4-4 Low-level output voltage ($V_{OL}$)**

This specifies the voltage value guaranteed for an output pin in low-level. The supply voltage is set at $V_{CCmin}$ and a load current of $I_{OL}$ is applied.

**4-5 Off-state high-level output current ($I_{OZH}$)**

This specification is applicable to ICs with 3-state outputs.

This specifies the maximum value of current that flows into the output terminal when the output is in high-impedance state and the minimum value of high-level output voltage is applied to it. At this time, supply voltage is set $V_{CCmax}$ and the input conditions are set so that the output will become low-level when it gets out of the high-impedance state.

**4.6 Off-state low-level output current ($I_{OZL}$)**

This specification is applicable to ICs with 3-state output.

This specifies the maximum value of current that flows out from the output terminal when the output is in high-impedance state and the maximum value of low-level output voltage is applied to the output terminal. At this time, supply voltage is set $V_{CCmax}$ and the input conditions are set so that the output will become high-state when it gets out of the high-impedance state.

**4-7 Input current at maximum voltage ($I_I$)**

This specifies the input current when the maximum input voltage as specified in the absolute maximum ratings is applied to the input and supply voltage set at $V_{CCmax}$. Input terminals, other than the one being measured, are set to 0V.

**4-8 High-level input current ($I_{IH}$)**

This specifies the input current when a high-level output voltage is applied to the input terminal. With supply voltage set to $V_{CCmax}$, the high-level voltage applied to the input is set to the minimum value of high-level output voltage (2.7V). Input terminals, other than the one being measured, are set to 0V.

**4-9 Low-level input current ($I_{IL}$)**

This specifies the input current when a low-level output voltage is applied to the input terminal. With supply voltage set to $V_{CCmax}$, the low-level voltage applied to the input is set to the maximum value (0.4V) of low-level voltage. Input terminals, other than the one being measured, are set to 4.5V.

**4-10 Output current ($I_O$)**

This specification is applicable to ICs with active pull-up outputs.

This specifies the current flowing from the output when 2.25V is applied to the output terminal and the output is high-level. With supply voltage set to $V_{CCmax}$, either 0V or 4.5V is applied to the inputs so that the output transistor becomes completely off.

This specification is given to shorten the charging time of parasitic capacitances in wiring.

**4-11 Supply current, outputs high ($I_{CCH}$)**

This specifies the current flowing into the supply terminal when the outputs are high-level. With supply voltage set to $V_{CCmax}$, an input voltage of either 0V or 4.5V is applied setting the output to high-level. All circuits within the IC are set to the above condition and measured at the same time. Supply current is expressed as the entire IC unit.

**4-12 Supply current, outputs low ($I_{CCL}$)**

This specifies the current flowing into the supply terminal when the outputs are low-level. With supply voltage set to $V_{CCmax}$, an input voltage of either 0V or 4.5V is applied setting the output to low-level. All circuits within the IC are set to the above condition and measured at the same time.

# DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

**4-13 Supply current, outputs disabled ($I_{ICCZ}$)**
This specifies the current flowing into the supply terminal when the outputs are in high-impedance state. With supply voltage set to $V_{CCmax}$, an input voltage of either 0V or 4.5V is applied setting the output to high-impedance. All circuits within the IC are set to the above condition and measured at the same time.

**4-14 Supply current ($I_{CC}$)**
$I_{CC}$ is calculated using the following formula where $I_{CCH}$ and $I_{CCL}$ are specified.

$$I_{CC}=\frac{I_{CCH}+I_{CCL}}{2}$$

For ICs without specified $I_{CCH}$ and $I_{CCL}$ values, the value of $I_{CC}$ is specified as the maximum value of current that flows into the supply terminal.

**4-15 Positive-going threshold voltage ($V_{T+}$)**
This specifies the level of input voltage at the point where the output state changes when the input voltage has increased from a level lower than negative-going threshold level $V_{T-}$. Depending on the type of device, supply voltage is either 5V or $V_{CCmin}$ at this measurement.

**4-16 Negative-going threshold voltage ($V_{T-}$)**
This specifies the level of input voltage at the point where the output state changes when the input voltage has decreased from a level higher than the positive-going threshold level $V_{T+}$. Depending on the type of device, supply voltage is either 5V or $V_{CCmin}$ at this measurement.

**4-17 Hysteresis ($V_{T+}-V_{T-}$)**
This specifies the difference between positive-going threshold voltage ($V_{T+}$) and negative-going threshold voltage ($V_{T-}$). Depending on the type of device, supply voltage is either 5V or $V_{CCmin}$ at this measurement.

## 5. SWITCHING CHARACTERISTICS

Propagation time, maximum clock frequency and output pulse width are specified in Switching characteristics within $V_{CC}$ = 4.5 ~ 5.5V, $T_a$ = 0 ~ 70°C or $T_a$ = −20 ~ +75°C. The measurements are made with the specified loads connected to the outputs and with the input pulse specified in the low-level voltage $V_{IL}$, the high-level voltage $V_{IH}$, the repetitive frequency of PRR, a pulse width of $t_w$, rise time $t_r$ and fall time $t_f$.

**5-1 Propagation time, low-to-high-level output ($t_{PLH}$)**
This specifies the length of time from when the input changes to when the output changes from low-level to high-level. The moment when they changes are specified with the reference voltage level. (See §7-2, 7-3.)

**5-2 Propagation time, high-to-low-level output ($t_{PHL}$)**
This specifies the length of time from when the input changes to when the output changes from high-level to low-level. The moment when they changes are specified with the reference voltage level. (See §7-2, 7-3.)

**5-3 Output enable time to high-level ($t_{PZH}$)**
This specification is applicable to ICs with 3-state outputs.

This specifies the length of time from when the input changes to when the output changes from high-impedance state to high-level. The moment when they changes are specified with the reference voltage level. (See §7-2, 7-3.)

**5-4 Output enable time to low-level ($t_{PZL}$)**
This specification is applicable to ICs with 3-state outputs.

This specifies the length of time from when the input changes to when the output changes from high-impedance state to low-level. The moment when they changes are specified with the reference voltage level. (See §7-2, 7-3.)

**5-5 Output disable time from high-level ($t_{PHZ}$)**
This specification is applicable to ICs with 3-state outputs.

This specifies the length of time from when the input changes to when the output changes from high-level to high-impedance state. The moment when they changes are specified with the reference voltage levels. (See §7-2, 7-3.)

**5-6 Output disable time from low-level ($t_{PLZ}$)**
This specification is applicable to ICs with 3-state outputs.

This specifies the length of time from when the input changes to when the output changes from low-level to high-impedance state. The moment when they changes are specified with the reference voltage levels. (See §7-2, 7-3.)

**5-7 Maximum clock frequency ($f_{MAX}$)**
This specification is applicable to flip-flops or MSIs including flip-flop circuits.

The maximum clock frequency is defined as the highest frequency at which the clock input can be driven through its required sequence while maintaining stable transitions of logic level at the output with other inputs set to cause changes of output logic level in accordance with the specification. (See §7-2.)

**5-8 Output pulse width ($t_{WQ}$)**
This specification is applicable to monostable multivibrators.

# DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

This specifies the width of the pulse appearing at the output at specified reference voltage, when a trigger pulse is applied with specified resistors and capacitors connected to the timing inputs.

## 6. TIMING REQUIREMENTS

These specifications are applicable to flip-flops and MSIs including flip-flop circuits.

These specify the input timing requirements which must be met to maintain a stable output change in the required sequence when input signals such as clock and reset change.

Timing requirements are specified at an ambient temperature of $T_a = -20 \sim +75°C$, a supply voltage of $V_{CC} = 4.5 \sim 5.5V$, and include pulse width, setup time, hold time, rise time, fall time and latch time.

### 6-1 Pulse width ($t_w$)

This specification is applicable to flip-flops and MSIs including flip-flop circuits.

This requirement specifies the minimum time between the leading edge and the trailing edge (using specified reference voltage level) of the input pulse waveform. If a pulse of a shorter width is applied, the signal may not only be invalid but also cause a misoperation. (See §7-2. 7-3.).

### 6-2 Setup time ($t_{su}$)

This specification is applicable to flip-flops and MSIs including flip-flop circuits.

With such ICs, it is necessary to set up the input condition some time before the change of a control input such as the clock input in order to ensure proper recognition of the input signal. This time length is setup time.

Setup time is the length from the set up to the active edge of the control input. The set up and active edge are specified with the reference voltage level.

Negative setup times indicate that the input conditions may be set up after the active edge of the control inputs. (See §7-2, 7-3.)

### 6-3 Hold time ($t_h$)

This specification is applicable to flip-flops and MSIs including flip-flop circuits.

With such ICs, it is necessary to maintain the input condition some time after the change of a control input such as the clock input in order to ensure proper recognition of the input signal. This time length is hold time. Hold time is specified in the same manner as setup time.

Negative hold times indicate that the input conditions may be changed before the active edge of the control inputs. (See §7-2, 7-3.)

### 6-4 Clock risetime ($t_r$)

This specifies the maximum length of time for the clock input to change from 0.6V to 3.2V. Misoperation may occur when a clock pulse with a risetime greater than this value is applied.

### 6-5 Clock falltime ($t_f$)

This specifies the maximum length of time for the clock input to change from 3.2V to 0.6V. Misoperation may occur when a clock pulse with a falltime greater than this value is applied.

### 6-6 Latch time ($t_{latch}$)

This specifies the length of time necessary before read-select after a write address has been selected, the write enable signal changed, and the data were written in. It is necessary to pay attention to this spec. when data are to be read immediately after rewriting.

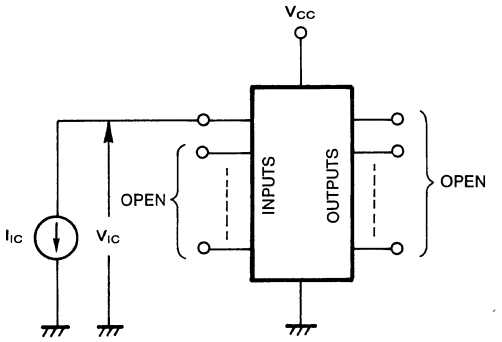
## 7. TEST CIRCUITS

This section includes typical test circuits for each characteristic. For complicated measurements of such devices as MSIs, refer to the detailed descriptions in the individual data sheets.

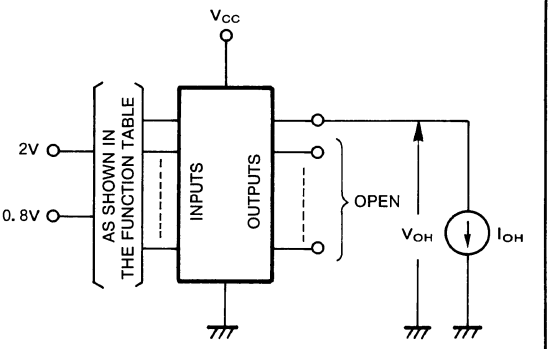
# DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

## 7-1 Circuits for measuring direct current characteristics

### $V_{IC}$ MEASUREMENT

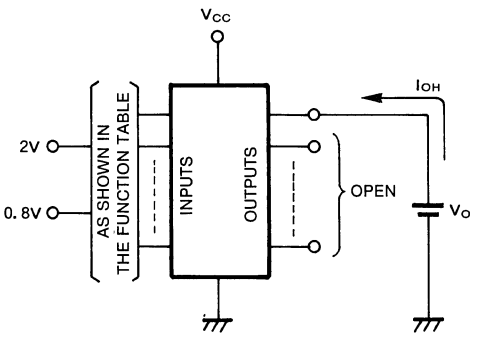



### $V_{OH}$ MEASUREMENT



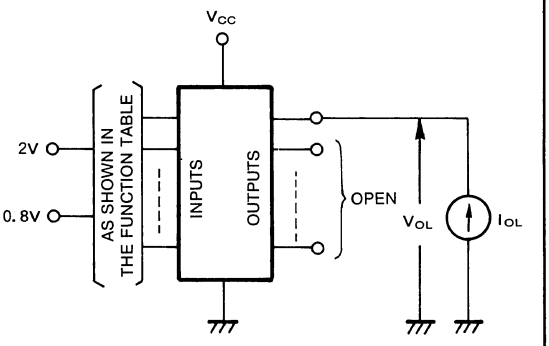

- Input condition set so that output becomes high-level

### $I_{OH}$ MEASUREMENT



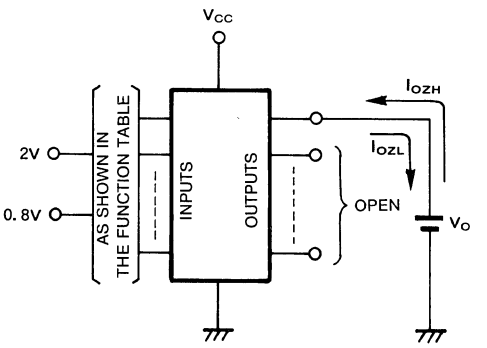

- Input condition set so that output becomes high-level

### $V_{OL}$ MEASUREMENT



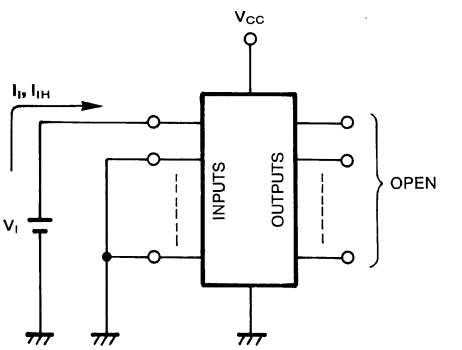

- Input condition set so that output becomes low-level

### $I_{OZH}$, $I_{OZL}$ MEASUREMENTS




- Input condition set so that output becomes high-impedance state

### $I_I$, $I_{IH}$ MEASUREMENTS

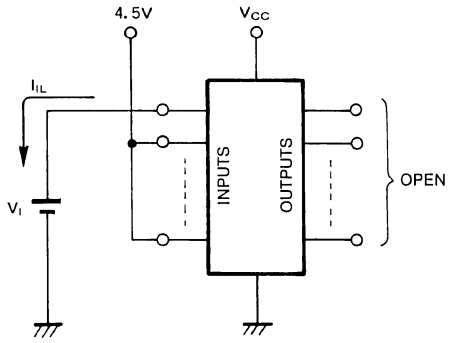




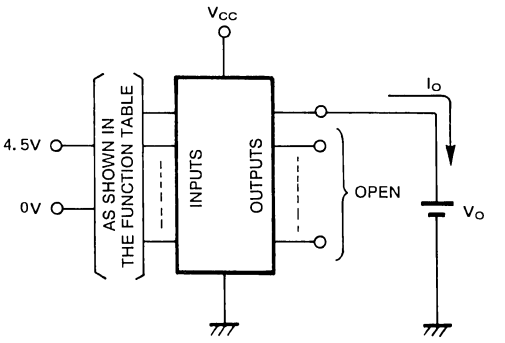

MITSUBISHI ELECTRIC

# DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

## $I_{IL}$ MEASUREMENT

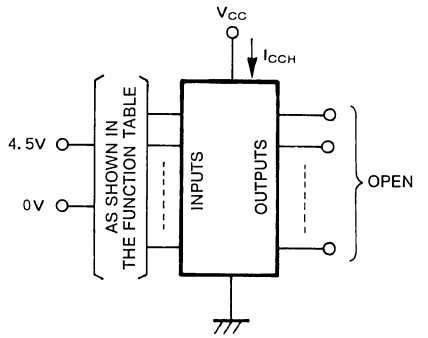



## $I_O$ MEASUREMENT



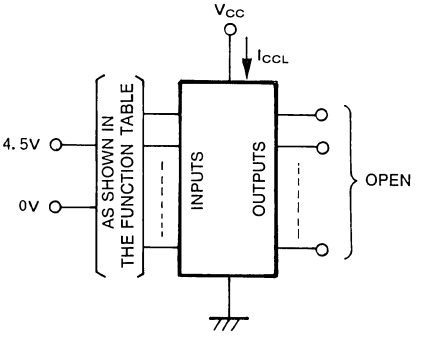

- Input condition set so that output becomes high-level

## $I_{CCH}$ MEASUREMENT



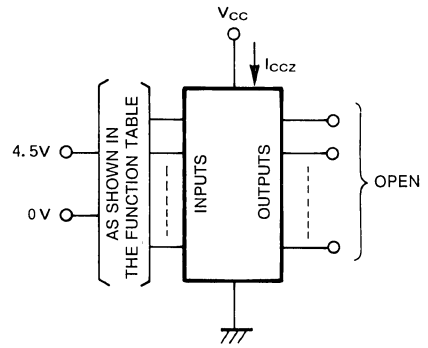

- Input condition set so that all outputs become high-level

## $I_{CCL}$ MEASUREMENT



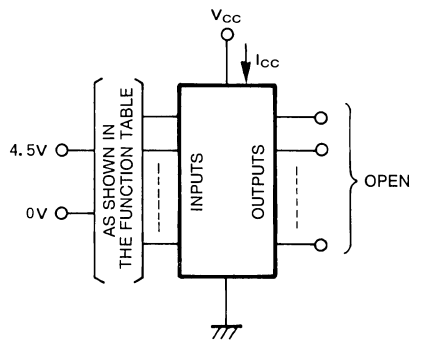

- Input condition set so that all outputs become low-level

## $I_{CCZ}$ MEASUREMENT




- Input condition set so that all outputs become high-impedance state

## $I_{CC}$ MEASUREMENT

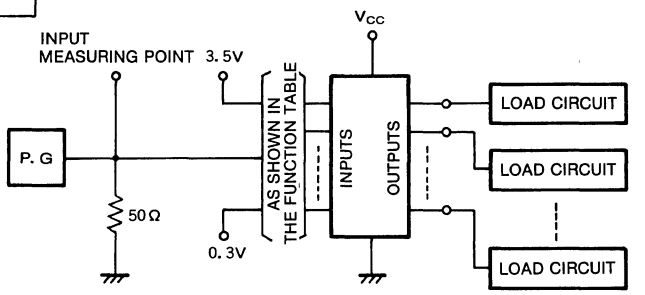



- Input conditions are specified in individual specifications When no specification is given, $I_{CC}$ is guaranteed in all possible input conditions.

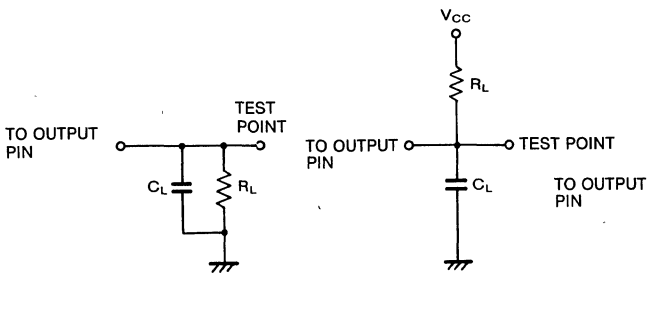
# DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

## 7-2 Circuits for measuring switching characteristics

SWITCHING MEASUREMENTS



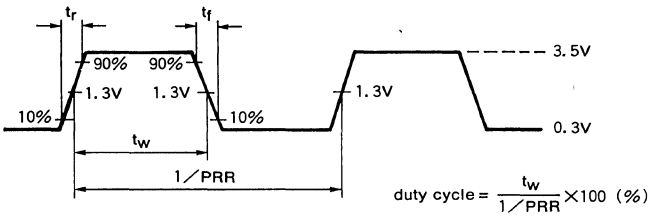

Note 1. The load circuit varies as shown in the following diagrams according to the type of IC output
$C_L$ includes probe and jig capacitance.




| PARAMETER | $S_1$ |
|---|---|
| $t_{PLH}$ | OPEN |
| $t_{PHL}$ | OPEN |
| $t_{PZH}$ | OPEN |
| $t_{PZL}$ | CLOSED |
| $t_{PHZ}$ | OPEN |
| $t_{PLZ}$ | CLOSED |

(a) Active pull-up output (b) Open collector output (c) 3-state output

Note 2. The pulse generator (PG) has the following characteristics:




Pulse repetition rate : PRR≦1MHz
Risetime : $t_r$=2ns
Falltime . $t_f$=2ns
Duty cycle duty cycle=50%
Output impedance $Z_O$=50Ω



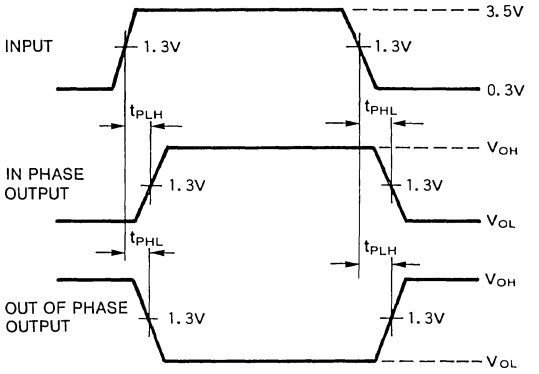
MITSUBISHI ELECTRIC

# DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

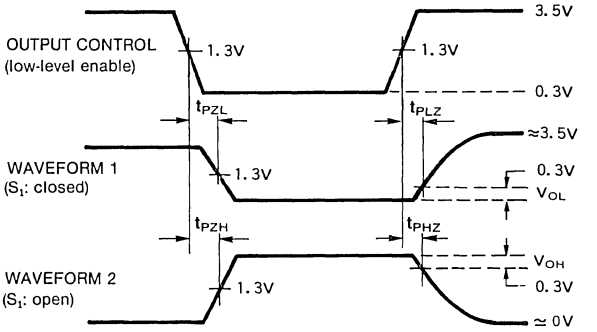
## 7-3 Timing diagram

### Input voltage waveform

1. Propagation time




2. Enable and disable time

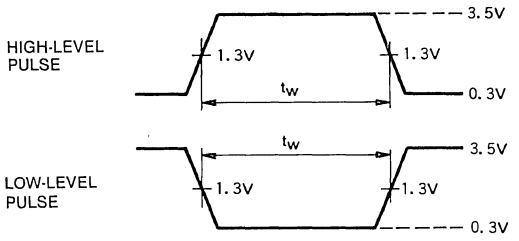



Waveform 1. The input conditions are set so that the output becomes low when enabled

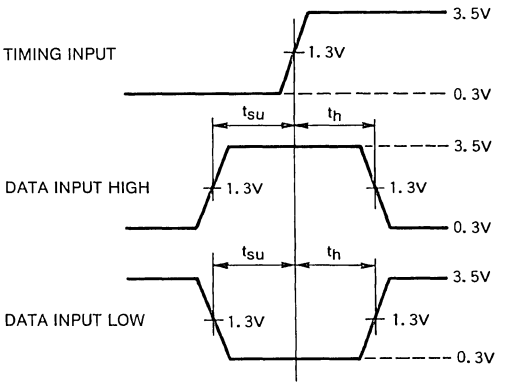
Waveform 2. The input conditions are set so that the output becomes high when enabled

### Timing waveform

1. Pulse width



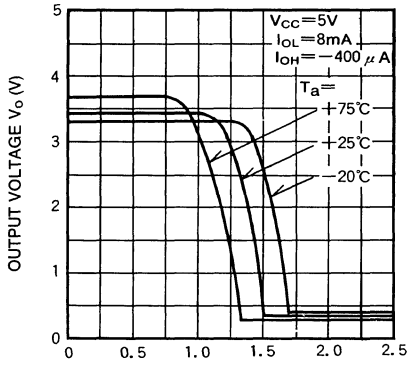

2. Setup, hold time



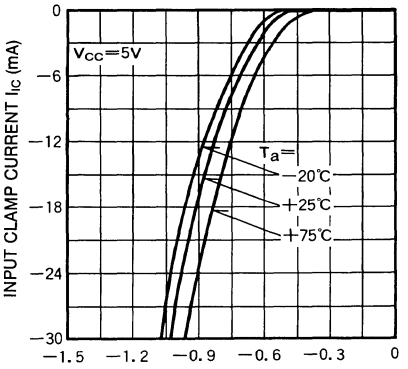
# DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

## 8. TYPICAL CHARACTERISTICS OF BASIC GATE

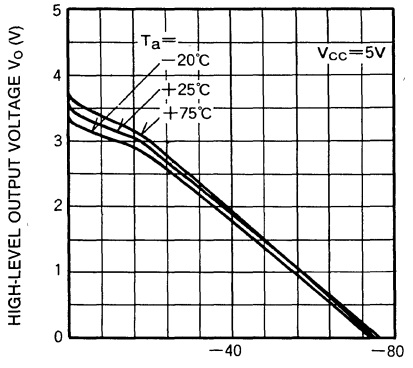
### INPUT vs. OUTPUT VOLTAGE CHARACTERISTICS (M74ALS00AP)



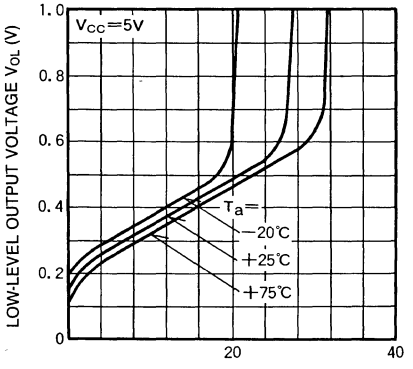

### INPUT CLAMP CURRENT vs. INPUT CLAMP VOLTAGE



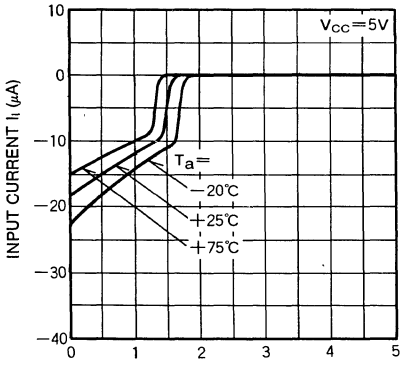

### OUTPUT VOLTAGE vs. HIGH-LEVEL OUTPUT CURRENT (M74ALS00AP)



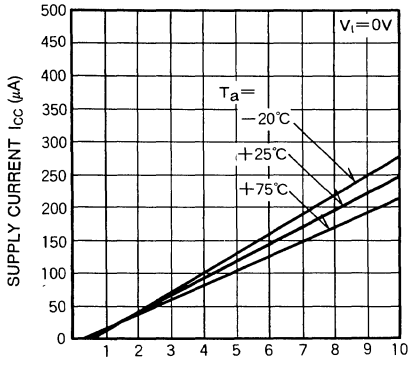

### LOW-LEVEL OUTPUT VOLTAGE vs. LOW-LEVEL OUTPUT CURRENT (M74ALS00AP)




### INPUT CURRENT vs. INPUT VOLTAGE (M74ALS00AP)

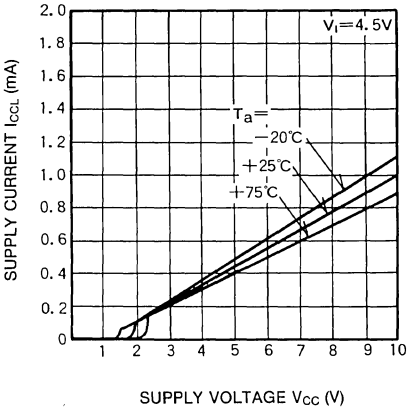



### SUPPLY CURRENT vs. SUPPLY VOLTAGE, OUTPUT HIGH (per gate) (M74ALS00AP)

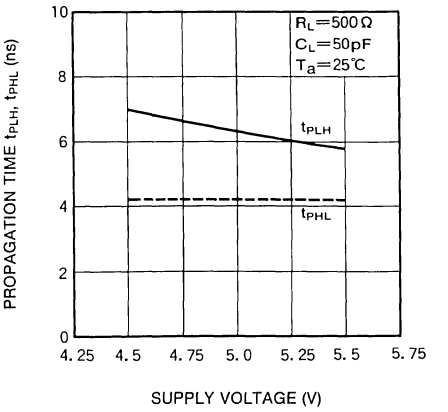


# DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

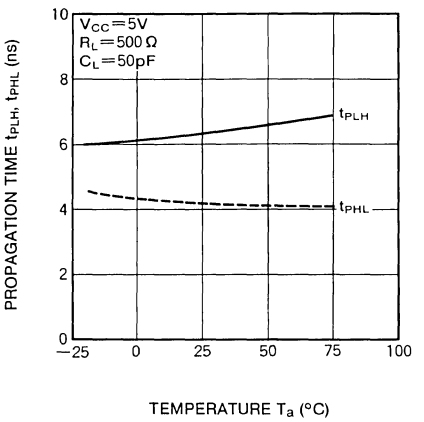
### SUPPLY CURRENT vs. SUPPLY VOLTAGE, OUTPUT LOW (per gate) (M74ALS00AP)



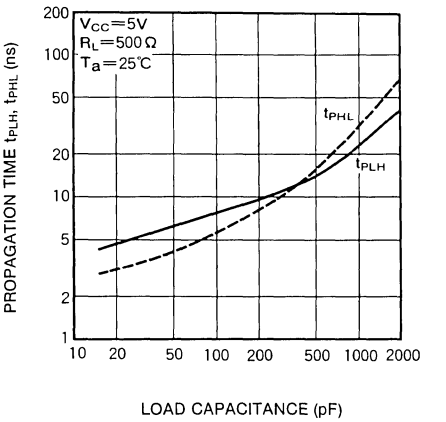

### PROPAGATION TIME vs. SUPPLY VOLTAGE (M74ALS00AP)



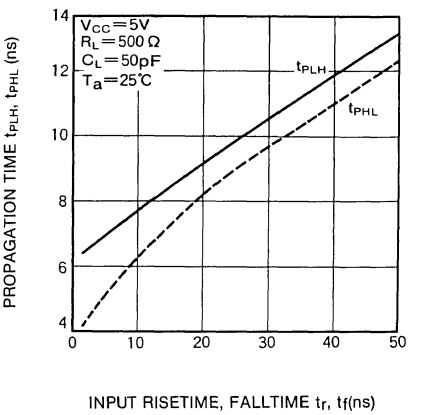

### PROPAGATION TIME vs. FREE-AIR TEMPERATURE (M74ALS00AP)



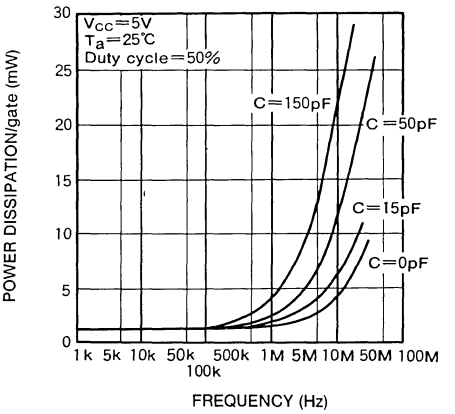

### PROPAGATION TIME vs. LOAD CAPACITANCE (M74ALS00AP)




### PROPAGATION TIME vs. INPUT RISETIME AND FALLTIME (M74ALS00AP)




### POWER DISSIPATION vs. FREQUENCY (M74ALS00AP)



# QUALITY ASSURANCE AND RELIABILITY TESTING

In recent years, advances in integrated circuits have been rapid, with increasing density and speed accompanied by decreasing cost. Because of these advances, it is now practical and economically justifiable to use these devices in systems of greater complexity and in which they were previously considered too expensive. All of these advances add up to increased demand.

We at Mitsubishi foresaw this increased demand and organized our production facilities to meet it. We also realized that simply increasing production to meet the demand was not enough and that positive steps would have to be taken to assure the reliability of our products.

This realization resulted in the development of our Quality Assurance System. The system has resulted in improved products, and Mitsubishi is able to supply its customers' needs with ICs of high reliability and stable quality. This system is the key to future planning for improved design, production and quality assurance.

## 1. QUALITY ASSURANCE SYSTEM

The Quality Assurance System imposes quality controls on Mitsubishi products from the initial conception of a new product to the final delivery of the product to the customer. A diagram of the total system is shown in Fig. 1. For ease of understanding, the system is divided into three stages.

### 1-1 Quality Assurance in the Design Stage

The characteristics of the breadboard devices are carefully checked to assure that all specifications are met. Standard integrated circuits and high-quality discrete components are used. During the design stage, extensive use is made of a sophisticated CAD program, which is updated to always include the latest state-of-the-art techniques.

### 1-2 Production Quality Assurance

Production quality is assured by both management and inspection of the devices.

(1) Environmental control.
(2) Scheduled periodic test and maintenance of design, tools, and test equipment.
(3) Control of ordered materials.
(4) Manufacturing process control.
(5) In-line evaluation: at wafer processing and assembly stages.
(6) Final production inspection: An nspection of the completed device consisting of an external inspection of the device's external measurements, its construction, and an inspection of its electrical characteristics.
(7) Product quality inspection: A final inspection consisting of three groups is undertaken in order to determine whether or not the stock products will meet user's needs.

Group A: Inspection of the device externally, its markings, and its electrical characteristics.

Group B: Inspection of the device environmentally, mechanically, and in terms of life expectancy.

Group C: A reliability test is periodically made from a sampling of lots that pass group A and B tests. This test is conducted every few months to inspect the environmental and mechanical performance and life expectancy of the devices.

### 1-3 Procedure for Determining the Reliability from Development and Preproduction to Mass Production

Evaluation of reliability described in 1-1 and 1-2 occurs at three levels of production: development, preproduction, and mass production. Once a product passes the development stage inspection, it proceeds to the next level, preproduction, where a limited number of devices are produced and again checked at this level. Upon passing this test, mass production begins and the above-mentioned quality assurance evaluation is undertaken to guarantee quality and reliability.

## 2. Reliability Control

### 2-1 Reliability Evaluation

Evaluation of reliability is based internationally on IEC standards for electronics devices and nationally on the RCJ (Reliability Center for Electronics Components of Japan). Mitsubishi Electric has chosen for the standard of its testing MIL-STD-883 and EIAJ-IC-121, outlined below in Table 1.

**Table 1 Typical reliability test items and conditions**

| Group | Item | Test condition |
|---|---|---|
| 1 | High temperature operating life | Maximum operating ambient temperature 1000h |
| | High temperature storage life | Maximum storage temperature 1000h |
| | High-temperature, high humidity with bias | 85°C, 85%RH, $V_{CC}$ = 5.5V |
| 2 | Soldering heat | 260°C, 10s |
| | Thermal shock | 0 ~ 100°C 15 cycles, 10min/cycle |
| | Temperature cycling | Minimum to maximum storage temperature. 1hr/cycle |
| 3 | Solderability | 230°C. 5s. use rosin flux |
| | Lead integrity | Tension: 340g 30s<br>Bending stress: 250g, 90°C, 3 times |
| | Vibration | 20G, X,Y,Z, each direction, 4 times<br>100 ~ 200Hz, 4min/cycle |
| | Drop test | 75cm, 3 times, wooden board, $Y_1$ direction |
| | Constant acceleration | 20000G, $Y_1$ direction, 1 min |

### 2.2 Failure Analysis

Devices that have failed during reliability or acceleration tests are analyzed to determine the cause of failure. This information is fed back to the process engineering section and manufacturing section so that improvements can be made to increase reliability. A summary of failure analysis procedures is shown in Table 2.

## 3. TYPICAL RESULTS OF RELIABILITY TESTS

### 3-1 Failure Criteria

The major failure standards for ALSTTL reliability tests are shown in Table 3. Unless otherwise noted, these are typical values.

**Table 2 Summary of failure analysis procedures**

| Step | Description |
|---|---|
| (1) External examination | ○ Inspection of leads, plating, soldering and welding<br>○ Inspection of materials, sealing, package and marking<br>○ Visual inspection of other items of the specifications<br>○ Use of stereo microscopes, metallurgical microscopes, X-ray photographic equipment, fine leakage and gross leakage testers in the examination |
| (2) Electrical tests | ○ Checking for open circuits, short circuits and parametric degradation by electrical parameter measurement<br>○ Observation of characteristics by a synchroscope or a curve tracer and checking of important physical characteristics by electrical characteristics<br>○ Stress tests such as environmental or life test, if required |
| (3) Internal examination | ○ Removal of the cover of the device, the optical inspection of the internal structure of the device<br>○ Checking of the silicon chip surface<br>○ Measurement of electrical characteristics by probes, if applicable<br>○ Use of SEM, XMA, and infrared microscanner, if required |
| (4) Chip analysis | ○ Use of metallurgical analysis techniques to supplement analysis of the internal examination<br>○ Slicing for cross-sectional inspection<br>○ Analysis of oxide film defects<br>○ Analysis of diffusion defects |

**Table 3 Failure criteria for reliability test**

| Parameter | | Minor failures | | Major failures |
|---|---|---|---|---|
| | | Lower limits | Upper limits | |
| DC current and voltage characteristics | High-level output voltage ($V_{OH}$) | IVD×0.8 | IVD×1.2 | UCL or LCL<br>For leakage current UCL × 2 |
| | Low-level output voltage ($V_{OL}$) | IVD−0.1V | IVD+0.1V | |
| | High-level input current ($I_{IH}$) | — | IVD×5 | |
| | Low-level input current ($I_{IL}$) | IVD×0.8 | IVD×1.2 | |
| | Output current ($I_O$) | IVD×0.8 | IVD×1.2 | |
| | High-level output current ($I_{OH}$) | — | IVD×5 | |
| Function | | — | | Short, open, abnormal functions |
| Appearance | | — | | Less than 95% soldered |
| Appearance | | — | | Lead breakdown |

UCL: Upper condition limits LCL: Lower condition limits IVD: Initial values

### 3-2 Results of Reliability Tests

Examples of the results of endurance and environmental tests of the M74ALS00P series are shown in Tables 4 and 5.

**Table 4 Endurance test results**

| Item | Test conditions | Type | Number of samples | Component hours | Number of failures |
|---|---|---|---|---|---|
| High-temperature operating life | $T_a$=125℃ $V_{CC}$=5.5V | SSI | 126 | 252,000 | 0 |
| | | MSI | 76 | 152,000 | 0 |
| High-temperature storage | $T_a$=150℃ | SSI | 44 | 44,000 | 0 |
| | | MSI | 22 | 22,000 | 0 |
| High-temperature, high-humidity bias | 85℃, 85%RH $V_{CC}$=5.5V | SSI | 88 | 176,000 | 0 |
| | | MSI | 114 | 190,000 | 0 |
| High-temperature, high-humidity storage | 85℃, 85%RH | SSI | 60 | 180,000 | 0 |
| | | MSI | 76 | 152,000 | 0 |
| Pressure cooker test | 121°C @ 2 atmospheres | SSI | 152 | 152,000 | 1 (1000 hrs) |
| | | MSI | 114 | 114,000 | 2 (1000 hrs) |

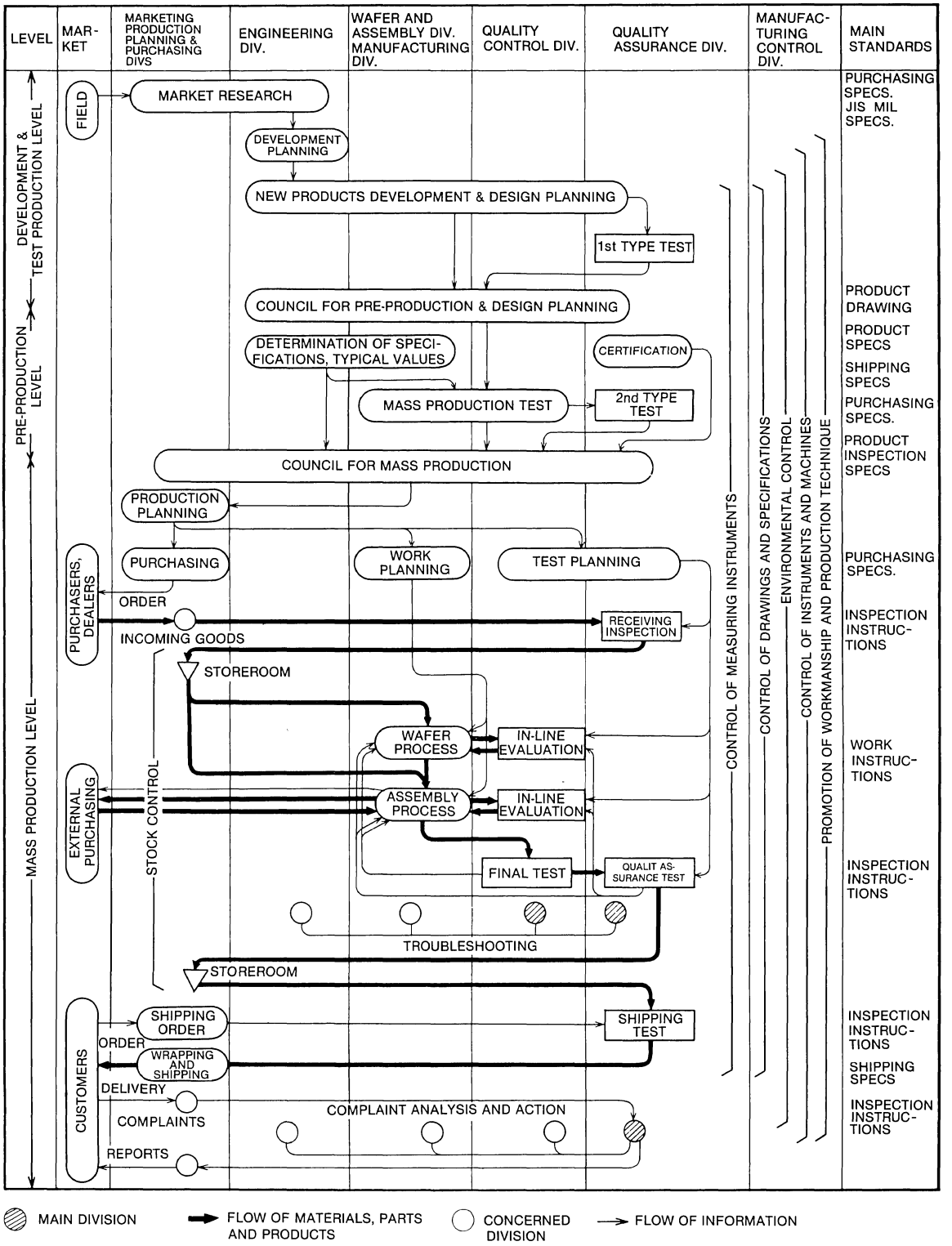
**Table 5 Examples of environmental test results**

| Item | | Test conditions | Number of samples | Number of failures | | | | Remarks |
|---|---|---|---|---|---|---|---|---|
| Solderability | | 230°C, 5 secs, rosin flux | 60 | 0 | | | | |
| Thermal environment | Soldering heat | 260℃, 10sec | 156 | Soldering heat | Thermal shock | Temperature cycling | | Series test |
| | Thermal shock | −40 ~ +125°C, 15C 10min/C | | 0 | 0 | 0 | | |
| | Temperature cycling | −65 ~ +150°C, 100C 1hr/C | | | | | | |
| Temperature cycling | | −65 ~ +150°C, 500C 1hr/C | 156 | 0 | | | | |
| Lead integrity | | 250g, bent 90° 3 times | 44 | 0 | | | | |
| Mechanical environment | Shock | 1500G, 0.5ms in X,Y,Z directions, 3 times | 88 | Shock | Drop test | Vibration | Constant acceleration | Series tests |
| | Drop test | From 75cm to a wooden board, $Y_1$ direction, 3 times | | 0 | 0 | 0 | 0 | |
| | Vibration | 20G, in X,Y,Z directions, 4 times each 100~2000Hz | | | | | | |
| | Constant acceleration | 20000G, in $Y_1$ direction, 1min | | | | | | |

We welcome and appreciate the cooperation of our customers in developing design specifications, establishing quality levels, controlling incoming inspections, developing assembly and adjusting processes and collecting field data. Mitsubishi is anxious to work with its customers to develop ICs of increased reliability that meet their requirements.

# QUALITY ASSURANCE AND RELIABILITY TESTING

FIG. 1 Quality assurance system



# PRECAUTIONS FOR USE

## 1. INTRODUCTION

The handling of ALSTTLs is basically the same as LSTTLs. However, ALSTTLs have faster switching speed and higher input impedance. So, in logic design and system design, more care is required of noise, problems in application and wiring which may lower the reliability. Please read this section carefully.

## 2. PRECAUTIONS CONCERNING ICs

### 2-1 Supply voltage ($V_{CC}$)

Absolute maximum ratings of supply voltage reflect the capacity of an IC in unusual conditions such as surge voltage and voltage spikes in transition. When supply voltages greater than these values are applied, excessive current may flow due to a breakdown in the device. This excessive current causes excessive heat, circuit destruction and fusing of internal wiring thus resulting in degradation in IC functions and reliability. It is urged that operation of the devices be conducted within the recommended supply voltage range of $V_{CC} = 5V \pm 10\%$ as functions and electrical characteristics are guaranteed only in this case.

### 2-2 Temperature range ($T_{opr}$, $T_{stg}$)

Temperature range is specified in operating free-air ambient temperature range $T_{opr}$ and storage temperature range $T_{stg}$. Generally speaking, $T_{opr}$ standard for consumer and industrial use is $0 \sim 70°C$ while the standard for military use is $-55 \sim +125°C$. In order to provide stable use of consumer and industrial equipments even in the winter season, Mitsubishi Electric has set a wide $T_{opr}$ standard of $-20 \sim +75°C$ over which functions and electrical characteristics are guaranteed. But of course,the best reliability is achieved when the devices are operated in the vicinity of 25°C. The higher and lower temperature portion of $T_{opr}$ should be considered as a guarantee in unusual conditions caused by troubles in air-conditioners or cooling fans etc.

$T_{stg}$ indicates the temperature range in which a device may be stored without causing characteristics degradation. This specification must be observed in device shipment and storage because a temperature in excess of these limits may cause drastic decrease in device reliability or damage of the device.

### 2-3 Input voltage ($V_I$)

The range of input voltage $V_I$ is specified in the absolute maximum ratings. Destruction of input circuits may occur when a voltage exceeding this range is applied to the inputs. Most of Mitsubishi Electric's ALSTTL devices have Schottky-barrier diodes and pnp transistors in their inputs with an upper $V_I$ limit of 7V. The lower limit of $V_I$ is $-0.5V$. When voltages less than this value are applied, parasitic transistors within the IC may operate causing malfunctions of the IC. This malfunction is less likely to occur in ALSTTLs than LSTTLs because of their device structures. In normal use, ALSTTLs are free from this malfunction.

### 2-4 Unused terminals

Terminals that are open operate as if a high-level input voltage is applied. However, it is recommended that a constant voltage with low impedance be applied to such open terminals because an IC lead tends to operate as an antenna picking up noise. This is especially true of clock, set and reset inputs of ICs with memory functions such as flip-flops, latches, counters and registers. In such cases, any operation caused by noise will result in false data written in the memory. Please connect unused inputs to $V_{CC}$ line and the inputs that should be always low-level to GND line. Do not connect an unused input with another input of the same gate so that AC noise margin should not lower.

### 2-5 High-level input signals

High-level input voltage is effective from 2V to the upper limit of the absolute maximum rating for normal TTL ICs. In other words, voltage changes within the high-level range would not cause changes in output. As parasitic capacitance exists between the anode and cathode of Schottky barrier diodes in the input circuit of the ALSTTL, when sharp ($\leqq$ 5ns) changes from a higher voltage to a lower voltage occur in the input, false waveforms may be generated in the output, even if the changes were within the high-level input voltage range. It is therefore important to avoid sharp changes of high-level input signal due to ringing, crosstalk and logical noise, even within the high-level input voltage range. When unused terminals are connected to the voltage supply line, ensure that voltage supply do not exceed $5V \pm 10\%$ because false waveforms are also generated in the output when sharp changes occur in the supply voltage.

### 2-6 Risetime and falltime of input signals

Just as in LSTTLs, an oscillation in the tens of MHz occurs in the outputs of ALSTTLs when a signal with a long risetime or falltime is applied to the input of a gate circuit. In MSIs, when such a signal is applied to the input, abnormal waveforms and misoperation occur. This is especially true for devices such as flip-flops, counters and shift registers that have the risetime and falltime specifications in the timing requirements. Since input waveforms having risetime or falltime greater than the specifications will result in misoperation, it is necessary to ensure that they be held within such limits. Even for devices without these specifications, it is necessary to limit the risetime and falltime of input signals to less than 500ns. Note that this does not hold true for devices such as Schmitt triggers that have hysteresis.

Such long risetime and falltime are often caused by a capacitor connected between an IC output and GND

line or transmission line and GND line. This capacitor may be used for preventing noise or generating either delayed pulses or differencial pulses. Such misoperation can be avoided by the use of a waveform shaper with a Schmitt trigger IC.

**2-7 Timing requirements**

These conditions give the input signal timing specifications necessary for the proper function of the IC. Devices with such requirements listed must be operated within the limits described to prevent malfunctions.

**2-8 Parasitic elements**

As shown in Fig. 1, the transistors and diodes that configure ALSTTL ICs have oxide films around them that are used to isolate the individual elements from each other. They also have a p-type domain in the substrate below them. This p-type domain is connected to the GND terminal. Between the GND terminal and the n-type domain that forms the collector of the transistor is formed a parasitic diode that is not shown on the circuit diagram and whose anode is connected to the GND terminal. Parasitic diodes are also connected between the GND terminal and voltage supply terminal ($V_{CC}$) as well as the output terminals. If the voltage of the output should become less than that of the GND terminal or a reverse supply voltage is applied, current will flow via this parasitic diode causing IC destruction. It is therefore very important to prevent a voltage of less than $-0.5V$ in respect to the GND terminal from being applied to another terminal.

As mentioned in §2-3, when input voltage$V_I$ drops to less than $-0.5V$, the largest portion of current flows from the GND terminal via the Schottky barrier diode SBD to the input terminal as shown in Fig. 1. But the remainder flows from the base of the parasitic transistor to the emitter with current amplification in the collector current. This results in current flowing from the collector of the nearby transistor to the input terminal. The original collector current is drawn into the input terminal causing circuit misoperation. Due to oxide film separation in the ALSTTLs, parasitic current amplification is less than that of LSTTLs making it less likely for misoperation to occur.

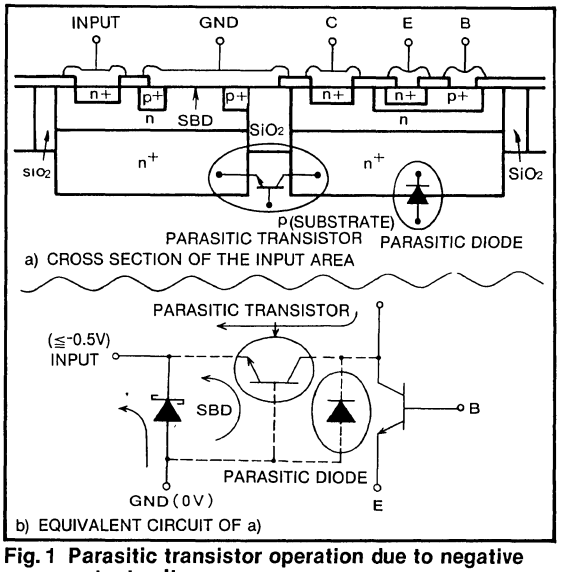



**Fig. 1 Parasitic transistor operation due to negative output voltage**

**2-9 Output loading capacitance**

By connecting a capacitor between the GND line of an IC and its output terminal or the line connected with output, delay time can be lengthened and noise can be prevented. This capacitor is charged from the power supply via the active pull-up circuit when the output changes from low-level to high-level. It discharges to GND through the output transistor when the output changes from high-level to low-level. Care must be taken regarding the size of this capacitor because the higher the capacity of the capacitor the greater the energy of charging and discharging through the output circuit causing degradation in it. The capacity of this capacitor depends upon the output characteristics of the IC and the frequency of charging and discharging, but generally a capacitor of less than $0.1\mu F$ is used. When a larger capacitor is to be used, connect a resistor in series with the capacitor to lengthen the charging and discharging time.

**2-10 DC noise margin**

There are various DC noise margins, but the one used here is defined as $V_{NH}$ and $V_{NL}$ when the output is either high-level or low-level respectively. They are derived as follows:

$$V_{NH} = V_{OHmin} - V_{TH} \quad V_{NL} = V_{TL} - V_{OLmax}$$

Where $V_{OHmin}$ and $V_{OLmax}$ are the values guaranteed in the databook and $V_{TH}$ and $V_{TL}$ are the input voltages that provide $V_{OLmax}$ or $V_{OHmin}$. (See Fig. 2) Fig. 3 shows the temperature characteristics of $V_{NH}$ and $V_{NL}$ in actual operating conditions as obtained from transfer characteristics. $V_{NH}$ and $V_{NL}$ of LSTTL gate are also given for reference.

# PRECAUTIONS FOR USE

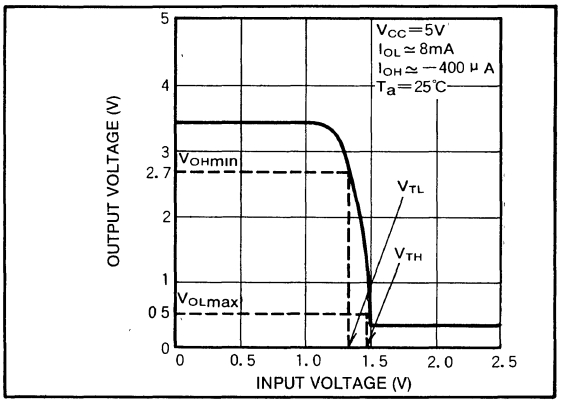



**Fig. 2 Transfer characteristics (M74ALS00AP)**

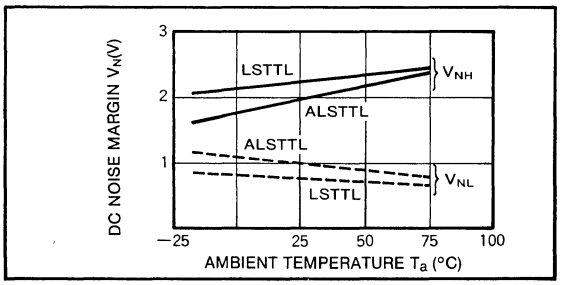



**Fig. 3 DC noise margin characteristics (M74ALS00AP)**

### 2-11 AC noise margin

Switching of the ALSTTL is generally faster than that of the LSTTL. This results in an AC noise margin lower than that of the LSTTL.

Fig. 4 shows the AC noise margins of the ALSTTL (M74ALS00AP) and the LSTTL (M74LS00P). Due to its higher input impedance and higher speed, the ALSTTL is easily affected by noise voltage (crosstalk) generated via the floating capacitance between lines. The lines connecting ALSTTL ICs should be shorter than the LSTTL ICs, and the lines between cards should be twisted or covered with materials of low dielectric constant.

### 2-12 Output short-circuit

When an output is high and that output is shorted to GND, excessive current flow and heat is generated in the IC. This is to be avoided if at all possible. However, if for some reason it is necessary to do so, one and only one output per an IC may be shorted for a period not exceeding one second.

### 2-13 Static electricity, surge

When surge endurance test is done by discharging a precharged 200pF capacitor connected between an input or output terminal and the GND terminal without a series resistor, the leakage characteristics degrade so that 50% of LSTTL and ALSTTL devices experience accumulative failure at approximately 200V. Although the static breakdown level of the ALSTTL and LSTTL are high, it is still necessary that full care be given to both the handling and system design in order to prevent damages due to static electricity and surge voltages.

### 2-14 Mechanical and thermal stress

The shaping and cutting of the package or external leads can cause damage to the external leads, degradation of moisture resistant characteristics, and breakage of internal leads. Moreover, be careful that mechanical stress should not be placed on external IC leads from the printed circuit board after the IC has been mounted.

Since the IC is constructed of a number of different materials with different expansion coefficients, the application of sudden temperature changes or extended period of high heat (such as when applying solder) can lead IC to degradation or the breakage of internal leads. To avoid such conditions, it is necessary that the mechanical and thermal stress levels be the lowest.

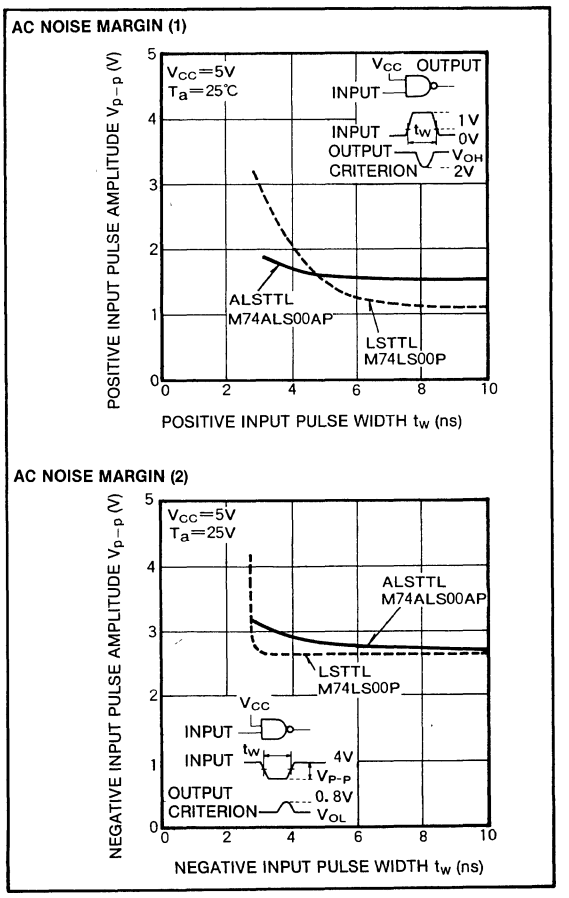



**Fig. 4 AC noise margin characteristics**

### 3. PRECAUTIONS CONCERNING SYSTEM DESIGN

#### 3-1 Supply line

As explained in §2-1, the supply voltage should be regulated and decreased in ripples within the recommended operating conditions. ($V_{CC}$ = 5V ± 10%) Moreover, to absorb the current spikes generated during IC switching, a decrease in supply impedance and supply line impedance is necessary. Fig. 5 shows current spike examples of the M74ALS00AP and M74ALS240P. It is recommended that a 0.01 ~ 0.22μF plastic film or porcelain capacitor of good high frequency characteristics be connected between GND and the supply line every 5 to 10 ICs for SSIs and every 1 to 5 ICs for MSIs. Also connect a 50 ~ 100μF electrolytic or tantalum capacitor between GND and the supply line every card. In the case of a monostable multivibrator or line driver, connect a 0.22μF plastic film or porcelain capacitor between $V_{CC}$ and GND on every IC. Make both the power supply line and GND line in as broad a pattern as possible and make them parallel with each other.

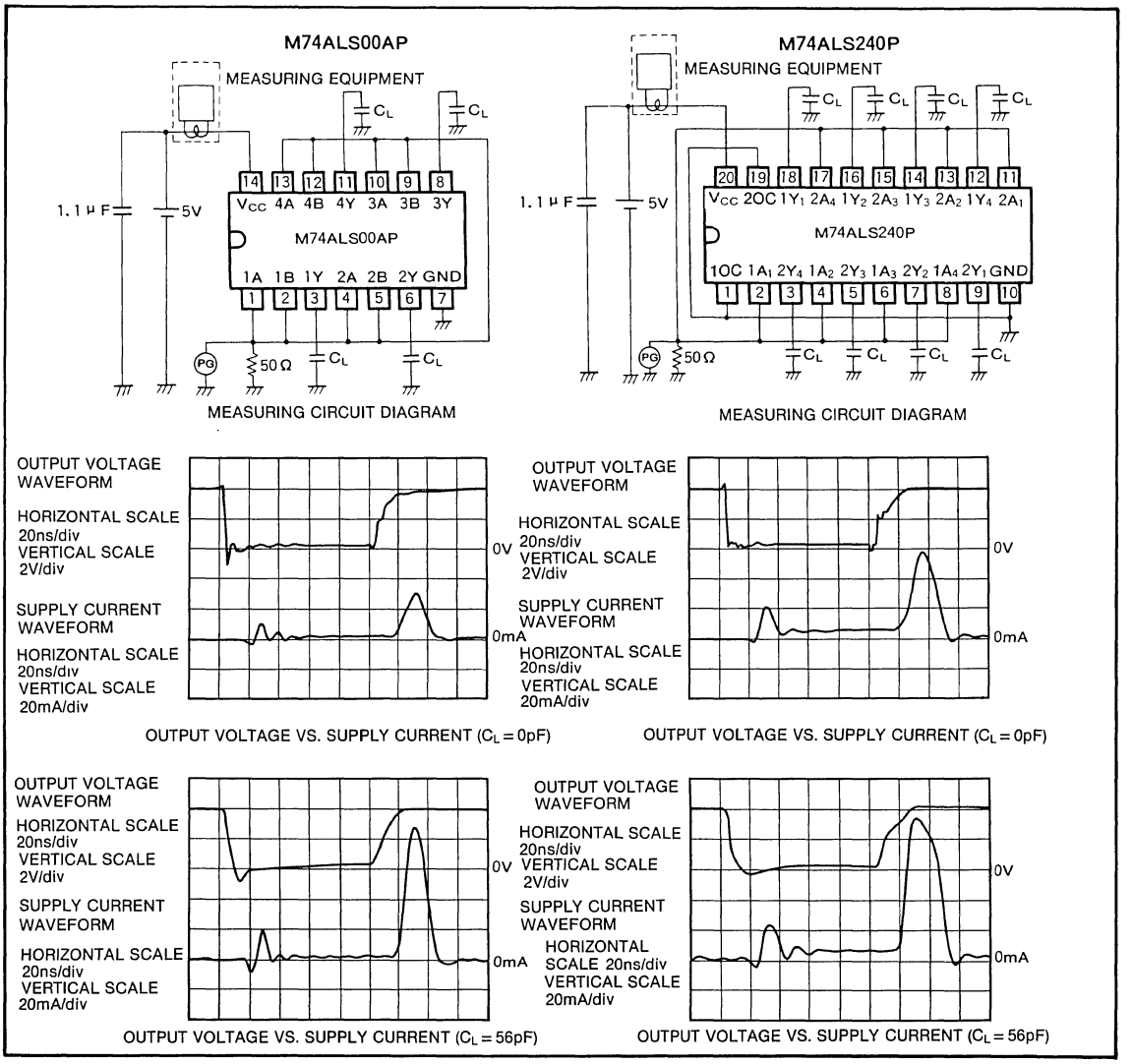
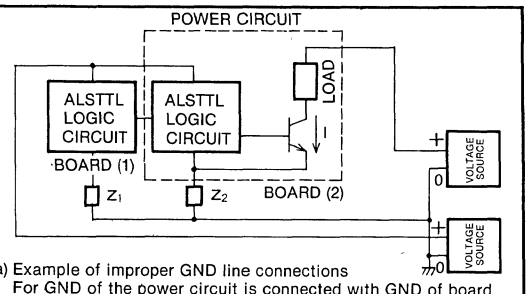


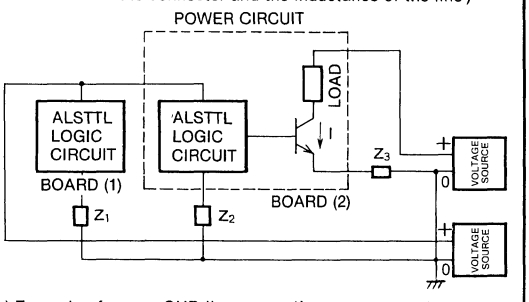

**Fig. 5 Current spikes of M74ALS00AP ($I_{OL}$ = 8mA) M74ALS240P ($I_{OL}$ = 24mA)**

### 3-2 Ground (GND) line

Noise is generated due to common impedance in the GND line. Connecting the GND line to the earth at numerous points can also result in its becoming a noise source when voltage is induced in it by external magnetic fields. For this reason it is important not only that the GND line impedance be dropped, but that careful consideration be given to separating the GND line from other power circuits and electronic devices as shown in Fig. 6, and to the employment of relays and photocouplers for isolating one circuit ground from another. Make the GND line pattern broader than the power supply line (to minimize the DC resistance and inductance).




a) Example of improper GND line connections
For GND of the power circuit is connected with GND of board (2), a large current I flows from the power circuit to the impedance $Z_2$ and raises the GND level of board (2) Thus the GND level of board (2) becomes higher than board (1) and noise margin is lowered. (The impedance $Z_2$ consists of the contact resistance of the connector and the inductance of the line)




b) Example of proper GND line connections
The GND lines of the power circuit and logic circuit are separated. This prevents a large current from flowing through $Z_1$ and $Z_2$, making it unlikely for the generation of a voltage difference between the GND levels of the boards.

**Fig. 6 GND line connections**

### 3-3 Fanout and wired-AND connections

(1) IC with active pull-up outputs

The larger portion of LSTTL and ALSTTL devices contain active pull-up (current source) in their output circuits in order to give high-speed switching and higher driving capabilities of capacitive loads. In this type of ICs, it is not possible to make wired-AND connections by connecting the output terminals together. This is because the active pull-up impedance is only 50Ω when the output is high-level. So, if two outputs are connected together and one of the outputs is high while the other is low, excessive current will flow from the high-level output to the low-level output. Besides the increase of low-level output voltage, this will generate heat and increase current flow in the internal wiring causing misoperation, damages in IC, or a serious decrease in reliability. It is therefore very important that such connections not be made.

Fanout $F_O$ indicates the number of input terminals that can be connected to and driven by an output. Fanout is represented by $F_{OL}$ and $F_{OH}$ for low-level and high-level respectively. The integer part of the smaller of $F_{OL}$ and $F_{OH}$ gives the maximum fanout.

$$F_{OL} \leqq \frac{\overline{I_{OL}}}{|\overline{I_{IL}}|} \qquad F_{OH} \leqq \frac{|\overline{I_{OH}}|}{\overline{I_{IH}}}$$

Where $\overline{I_{OL}}$, $\overline{I_{OH}}$, $\overline{I_{IL}}$ and $\overline{I_{IH}}$ are the maximum values guaranteed of low-level output current $I_{OL}$, high-level output current $I_{OH}$, low-level input current $I_{IL}$ and high-level input current $I_{IH}$, respectively. The above formula is appropriate for load ICs that all have the same $I_{IL}$ and $I_{IH}$ values. When these values are different, use the following formula.

$$\overline{I_{OL}} \geqq \sum_{i=1}^{N} |\overline{I_{ILi}}| \qquad |\overline{I_{OH}}| \geqq \sum_{i=1}^{N} \overline{I_{IHi}}$$

(2) IC with open collector outputs

Wired-AND connections are possible with ICs that have open collector outputs. An open collector output needs a load resistor $R_L$ connected between $V_{CC}$ and itself. The value of $R_L$ may be any value within the range set by $R_{L(min)}$, minimum load resistance, and $R_{L(max)}$, maximum load resistance, which vary according to the number of wired-AND connected outputs M and the number of connected inputs N (fanout). The formula is:

$$R_L(max) = \frac{V_{CC} - V_{OH}}{\sum_{i=1}^{M} \overline{I_{OHi}} + \sum_{i=1}^{N} \overline{I_{IHi}}}$$

$$R_L(min) = \frac{V_{CC} - V_{OL}}{\overline{I_{OL}} - \sum_{i=1}^{N} |\overline{I_{ILi}}|}$$

Where $\overline{I_{OH}}$, $\overline{I_{IH}}$, $\overline{I_{OL}}$ and $\overline{I_{IL}}$ are the maximum values guaranteed. $V_{CC}$ is the minimum value in which the circuit is expected to function. (usually 4.5V) $V_{OH}$ is the minimum value needed in the circuit. It may be 2.7V or 2.0V or anything.

(3) IC with 3-state output

The 3-state output, in addition to the low-level state and high-level state of the active pull-up output, has a high-impedance state "Z." The use of "Z" permits bus driving operation. As shown in Fig. 7, this method while resembling the previously mentioned wired-AND connection, differs in that only one of the outputs connected to one bus is used in active state with the remainder being placed in the high-impedance state.

The values of M and N are determined by the following formula,where M is the number of outputs connected to the bus and N is the number of inputs connected (fanout).

$$\overline{I_{OL}} \geqq \sum_{i=1}^{M-1} |\overline{I_{OZLi}}| + \sum_{i=1}^{N} |\overline{I_{ILi}}|$$

$$|\overline{I_{OH}}| \geqq \sum_{i=1}^{M-1} \overline{I_{OZHi}} + \sum_{i=1}^{N} \overline{I_{IHi}}$$

Since many outputs are connected to the bus in this method, it is necessary that timing be set so that only one of the outputs becomes active while the remainder remain in the high-impedance state. If more than one of the outputs become active at the same time, it is as if active pull-up outputs were connected together creating the condition explained in §3-3-(1). To prevent such conditions, the output enable and disable times have been specified in the switching characteristics of these types of devices. From these specifications, timing should be set so that none of high-impedance outputs becomes active before the active output becomes high-impedance. Take care not to allow active period to overlap because excessive current will flow in the power and GND lines lowering the voltage of the power line and creating noise thus causing misoperation.

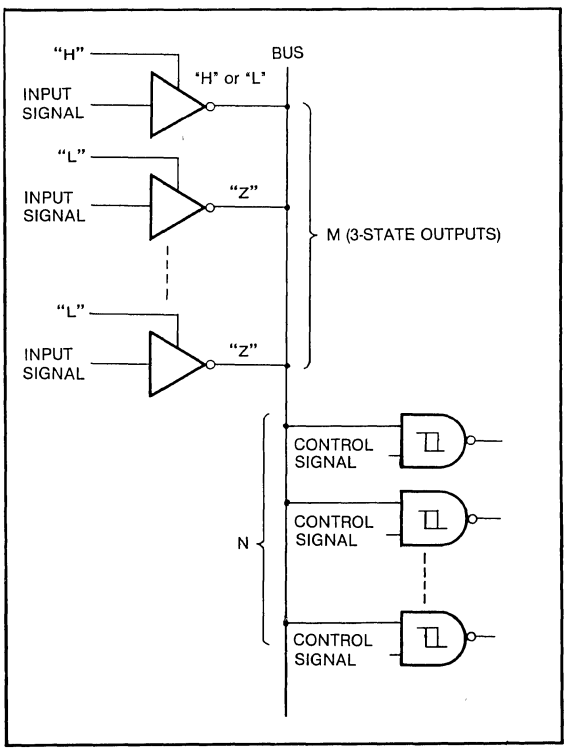



**Fig. 7 Bus connection**

### 3-4 Unused gates

Since there are several independent gate circuits within a gate IC, some gates will remain unused when the IC is used in a logic circuit. As far as operation is concerned, it makes no difference whether or not the terminals of unused gate circuits are left open. However, for example, a comparison of a NAND gate supply current with its terminals left open and with its terminals connected to GND will show that approximately three times as much current flows in the former condition as in the latter. Because the input conditions of unused gates can reduce the power supply capacity, it is recommended that unused gate input connections be properly taken care of.

### 3-5 Length of transmission lines between ICs

It is necessary that the line impedance of the transmission line and the load impedance be matched for proper transmission of signal waveforms.

However, when printed pattern or jumper wires are used as transmission lines between ALSTTL outputs and ALSTTL inputs, mismatching occurs because the line impedance of printed patterns and jumpers is 50~300Ω while that of the ALSTTL input is at least 10kΩ.

In such a case, and when the length of the transmission line becomes greater than 20cm, ringing occurs on the leading and trailing edges of the signal waveform due to mismatching. Malfunction occurs when the voltage of an input stays below GND level for 2~5ns near the trailing edge of the signal. Since the ALSTTL generally has an SBD configured between GND and the input, negative voltages that may be generated after the trailing edge of a signal are clamped. However, the clamping effects on negative voltages with a short period of 2~5ns are small, resulting in a voltage drop to less than −1.5V. Even with a period of negative voltage as short as 2~5ns, misoperation can occur as described in §2-8 due to parasitic devices.

The following procedure explains some methods to prevent ALSTTL misoperation due to ringing on the trailing edges of input signals.

1. When the transmission line exceeds 20cm, insert a buffer in the middle of the line as a waveform shaper circuit.
2. When the number of connected inputs is 10 or less, connect a 100~150Ω resistor between the ALSTTL output and the transmission line for absorption of reflected voltage. Or insert a capacitor with a capacitance of approximately 100pF between the output terminal and the GND.

In the case of ALSTTLs, it becomes even more necessary than LSTTLs to investigate the position of components and to shorten the length of important signal lines.

# PRECAUTIONS FOR USE

### 3-6 Signal line resonance

In Fig. 8 a), the input of an ALSTTL is connected via a wire of several tens of centimeters to a switch, S, which sends ON/OFF condition signals. In such a case, capacitor C, connected between the input terminal and the GND close to the input terminal, may be used to prevent the ALSTTL from misoperation due to inductive noise.

The equivalent circuit of Fig. 8 a) is shown in Fig. 8 b). When the switch is turned on, a damping oscillation is created between the two terminals C is connected to, as Fig. 9 shows. This damping oscillation drives the input below GND level causing misoperation of the ALSTTL as described in §2-8.

The damping oscillation has a frequency of 1 ~ 5MHz when the signal line has a length of 60cm and C = 15,000pF, a frequency that is lower than that experienced in ringing as described in §3-5. To prevent this damping oscillation, damping resistor $R_D$ may be added in series to L. The value of $R_D$ is found by using the following formula.

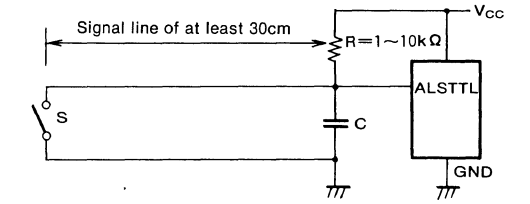
$$f_O = \frac{1}{2\pi\sqrt{LC}}$$

$$R_D \geqq 2\sqrt{\frac{L}{C}}$$

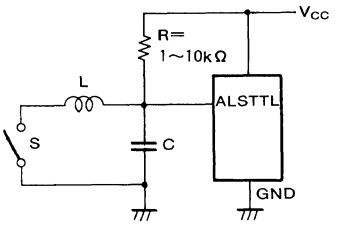
Observation of the damping oscillation in Fig. 9 shows $f_O \fallingdotseq 3$MHz and since C = 15,000pF then $L \fallingdotseq 0.2\mu$H and $R_D \geqq 7\Omega$.

Usually, it will be found that a value of 10 ~ 47Ω for $R_D$ will prevent such resonant oscillations.

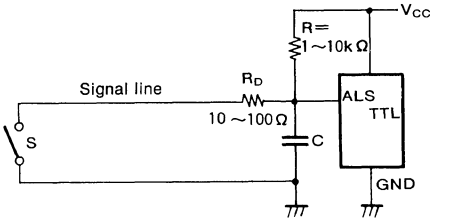
Since an SBD is generally configured between the input and GND of an ALSTTL, the magnitude of damping oscillation is small compared to that without an SBD. However, since full prevention cannot be obtained, it is recommended that the circuit shown in Fig. 8 c) be used rather than the one in Fig. 8 a).




a) The signal line and capacitor C form a resonant circuit that can easily cause misoperation.




b) The equivalent circuit of a)




c) $R_D$ is added to prevent resonant oscillation by the signal line and capacitor C.

**Fig. 8 Examples of ALSTTL application**

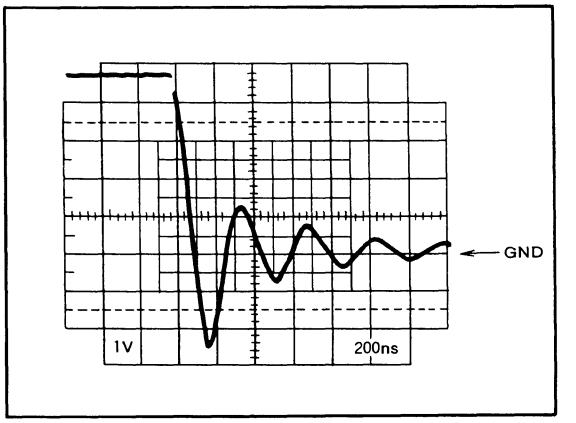
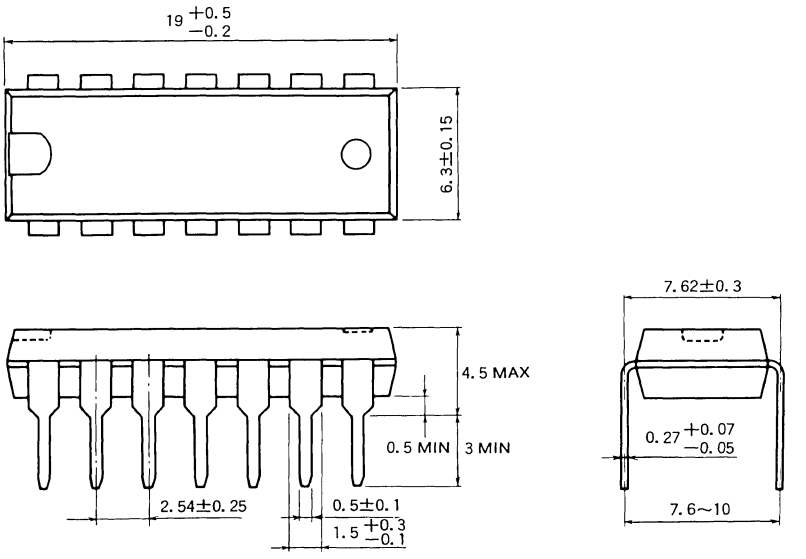



**Fig. 9 Example of damping oscillation**

# PACKAGE OUTLINES

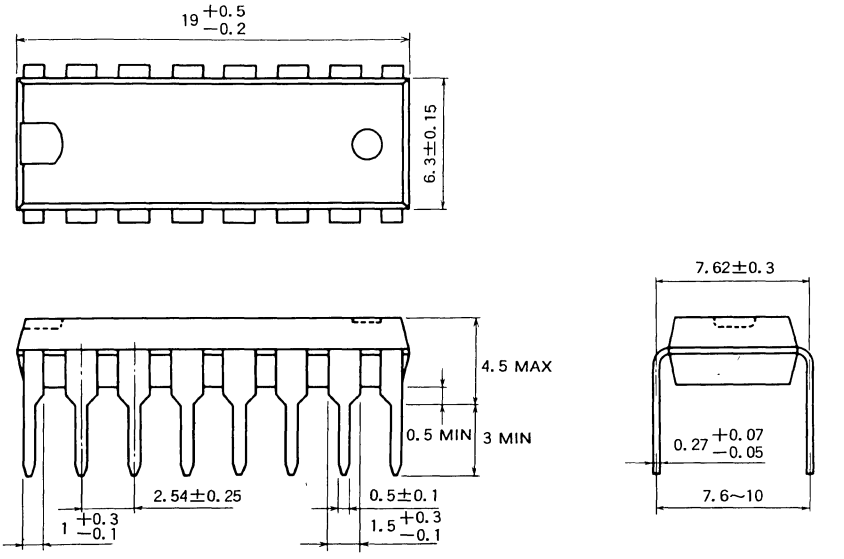
## TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm




## TYPE 16P4 16-PIN MOLDED PLASTIC DIL

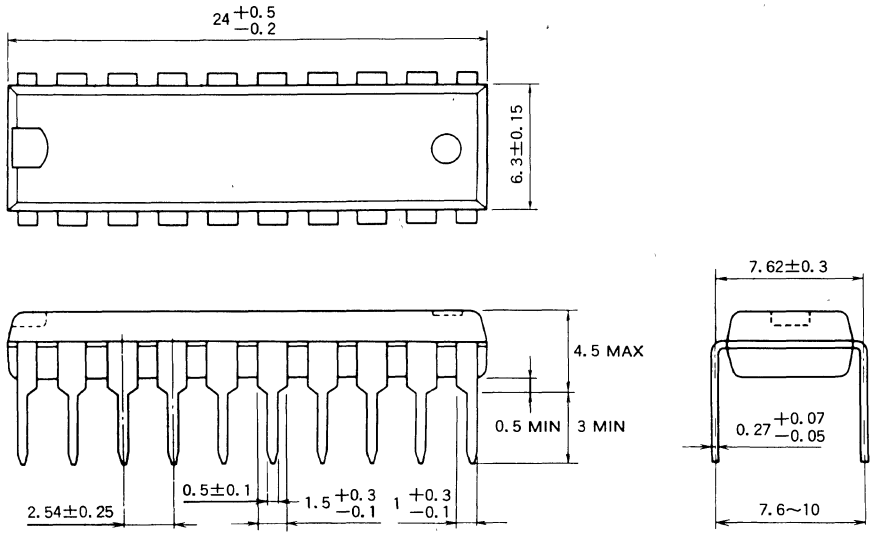
Dimension in mm



# PACKAGE OUTLINES

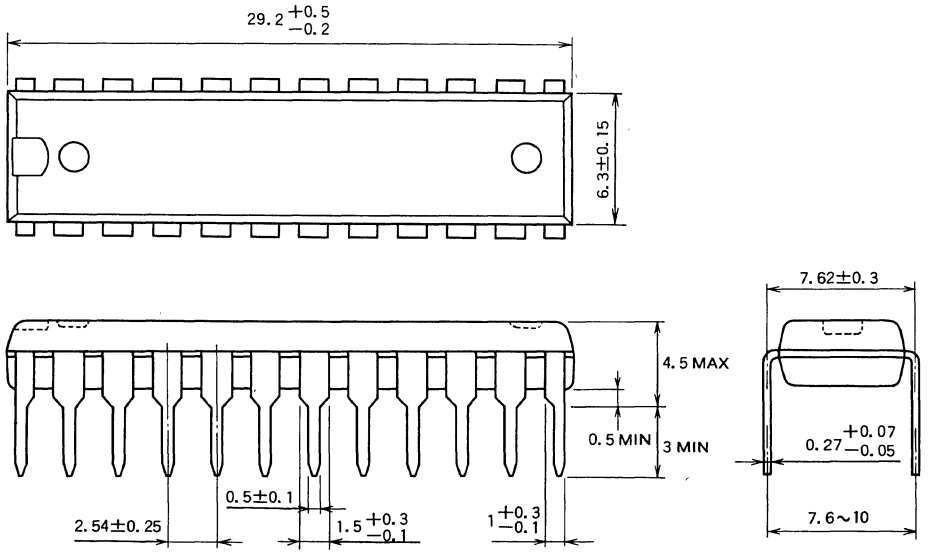
## TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm




## TYPE 24P4D 24-PIN MOLDED PLASTIC DIL

Dimension in mm

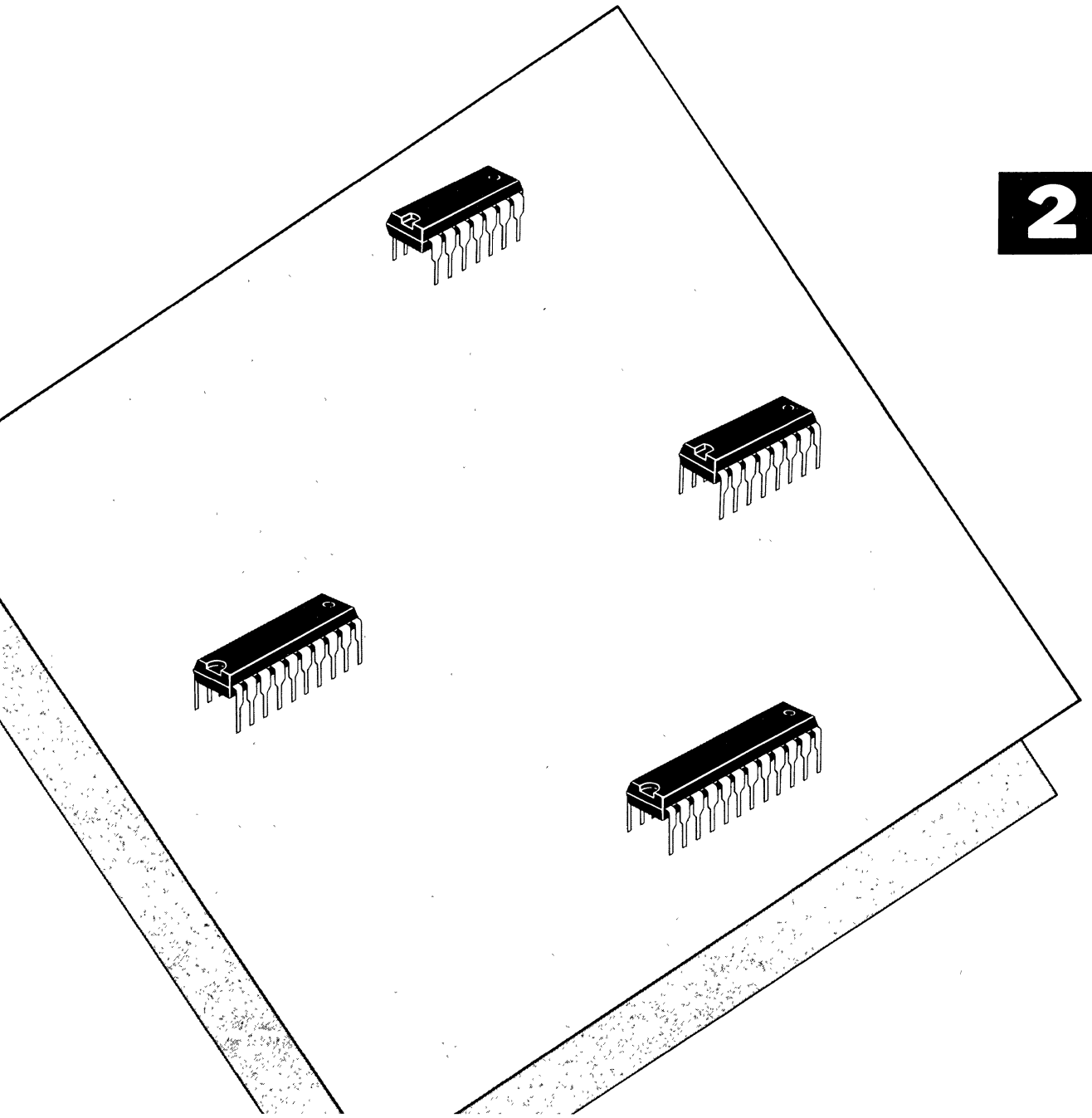





MITSUBISHI ELECTRIC

# DATA SHEETS

## INDIVIDUAL DATA



2

# M74ALS00AP

## QUADRUPLE 2-INPUT POSITIVE NAND GATE

## DESCRIPTION

The M74ALS00AP is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND gates, usable as negative-logic NOR gates.

## FEATURES

- High speed ($t_{pd}$ = 4ns typical: $C_L$ = 15pF)
- Low power dissipation ($P_d$ = 5mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS00AP achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

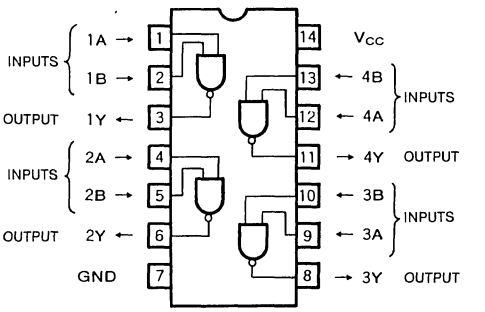
When both A and B inputs are high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

The buffer version of M74ALS00AP, the M74ALS-1000P ($I_{OL}$ = 24mA), is also available.

## FUNCTION TABLE

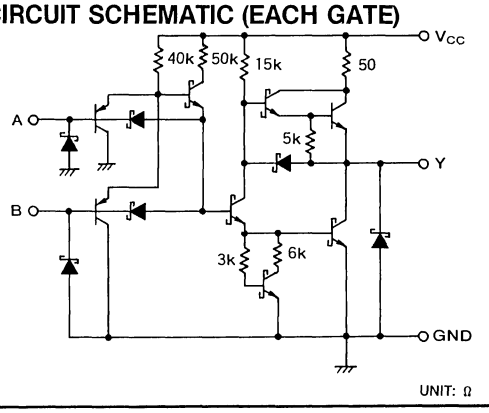
| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | −65~+150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## QUADRUPLE 2-INPUT POSITIVE NAND GATE

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $T_a$=0~70°C | 2.7 | 3.4 | | V |
| | | $I_{OH}$=−0.4mA | $T_a$=−20~+75°C | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.5 | 0.85 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 1.5 | 3 | mA |

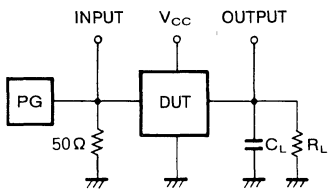
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=500Ω | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=500Ω | | | | | | |
| | | | | $T_a$=25°C | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | | 4.5 | | 3 | 6 | 11 | 3 | 6 | 12 | ns |
| $t_{PHL}$ | | | | | 3 | | 2 | 5 | 8 | 2 | 5 | 9 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

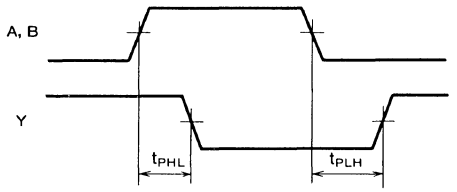
$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

### TIMING DIAGRAM (Reference level = 1.3V)






MITSUBISHI ELECTRIC

# M74ALS01P

## QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT



## DESCRIPTION

The M74ALS01P is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND gates with open collector outputs, usable as negative-logic NOR gates.

## FEATURES

- Wired-AND connectability
- High breakdown output voltage ($V_O \geqq 7V$)
- High speed ($t_{pd} = 12.5ns$ typical: $C_L = 15pF$)
- Low power dissipation ($P_d = 5.1mW$ typical)
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

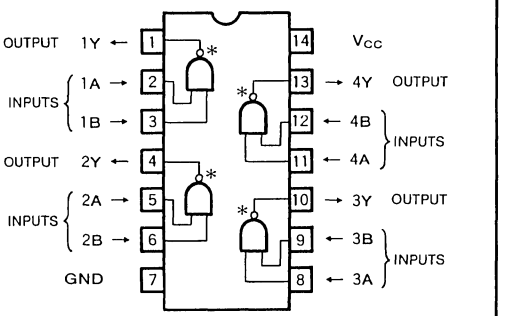
## FUNCTIONAL DESCRIPTION

This device employs PNP transistor inputs and open collector outputs. The open collector output enables selection of high-level output impedance with an external resistor. It also permits wired-AND connection which is impossible with ordinary gates. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

When both A and B inputs are high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

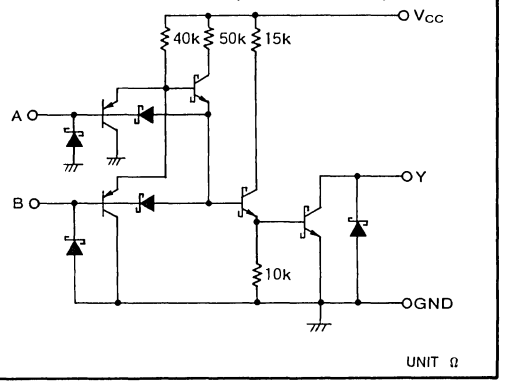
| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




## ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5～+7 | V |
| $V_I$ | Input voltage | | −0.5～+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5～+7 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20～+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65～+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.43 | 0.85 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 1.62 | 3 | mA |

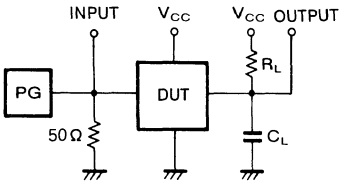
* All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=2kΩ | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=2kΩ | | | | | | |
| | | | | $T_a$=25°C | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | | 14 | | 23 | 30 | 54 | 23 | 30 | 55 | ns |
| $t_{PHL}$ | | | | | 11 | | 8 | 16 | 28 | 8 | 16 | 31 | |

* All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 1: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

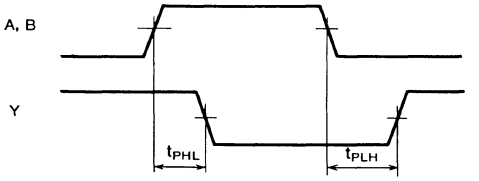
$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS02P

## QUADRUPLE 2-INPUT POSITIVE NOR GATE

## DESCRIPTION

The M74ALS02P is a semiconductor integrated circuit consisting of four 2-input positive-logic NOR gates, usable as negative-logic NAND gates.

## FEATURES

- High speed ($t_{pd}$ = 5.5ns typical: $C_L$ = 15pF)
- Low power dissipation ($P_d$ = 7.6mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS02P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

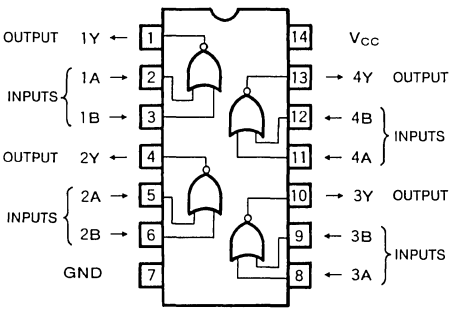
When both A and B inputs are low-level, output Y is high-level, and when at least one of the inputs is high, the output is low.

The buffer version of M74ALS02P, the M74ALS1002P ($I_{OL}$ = 24mA), is also available.

## FUNCTION TABLE

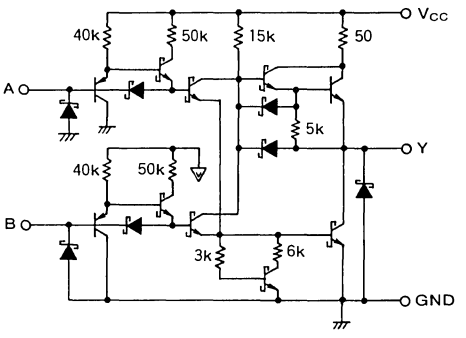
| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| H | L | L |
| L | H | L |
| H | H | L |

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




UNIT: Ω

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | −65~+150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## QUADRUPLE 2-INPUT POSITIVE NOR GATE

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $T_a$=0~70℃ | 2.7 | 3.4 | | V |
| | | $I_{OH}$=−0.4mA | $T_a$=−20~+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.86 | 2.2 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 2.16 | 4 | mA |

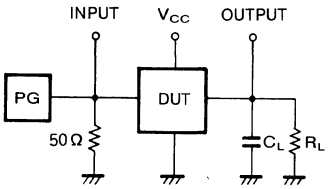
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=500Ω | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=500Ω | | | | | | |
| | | | | $T_a$=25℃ | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | | 7 | | 3 | 8 | 12 | 3 | 8 | 13 | ns |
| $t_{PHL}$ | | | | | 4 | | 3 | 6 | 10 | 3 | 6 | 11 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

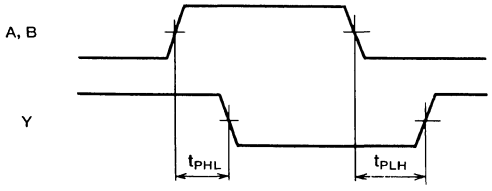
$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS03AP

## QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

## DESCRIPTION

The M74ALS03AP is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND gates with open collector outputs, usable as negative-logic NOR gates.

## FEATURES

- Wired-AND connectability
- High breakdown output voltage ($V_O \geqq 7V$)
- High speed ($t_{pd} = 11ns$ typical: $C_L = 15pF$)
- Low power dissipation ($P_d = 5.1mW$ typical)
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

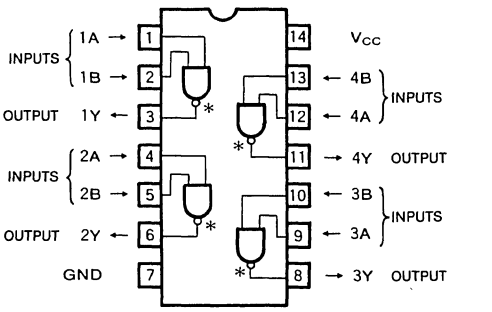
This device employs PNP transistor inputs and open collector outputs. The open collector output enables selection of high-level output impedance with an external resistor. It also permits wired-AND connection which is impossible with ordinary gates. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

When both A and B inputs are high-level, output Y is low-level, and when at least one of the inputs is low, the output is high. This device has the same function as M74ALS01P with different pin connections.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

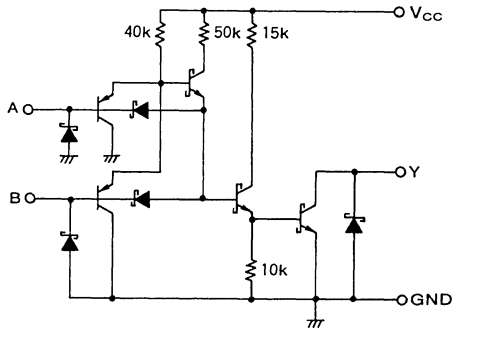
## PIN CONFIGURATION (TOP VIEW)




*: OPEN COLLECTOR OUTPUT

Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




UNIT: Ω

## ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5～+7 | V |
| $V_I$ | Input voltage | | −0.5～+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5～+7 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20～+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65～+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.43 | 0.85 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 1.62 | 3 | mA |

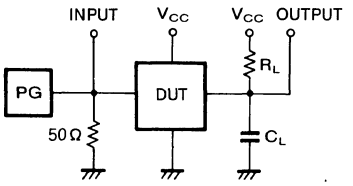
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

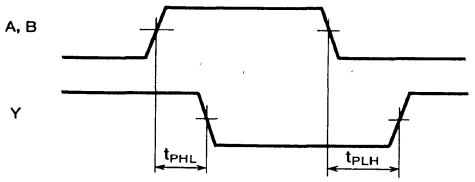
| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=2kΩ | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=2kΩ | | | | | | |
| | | | | $T_a$=25°C | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | | 14 | | 23 | 30 | 54 | 23 | 30 | 55 | ns |
| $t_{PHL}$ | | | | | 8 | | 5 | 13 | 22 | 5 | 13 | 25 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS04P

## HEX INVERTER

## DESCRIPTION

The M74ALS04P is a semiconductor integrated circuit consisting of six inverters.

## FEATURES

- High speed ($t_{pd}$ = 4ns typical: $C_L$ = 15pF)
- Low power dissipation ($P_d$ = 7.6mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

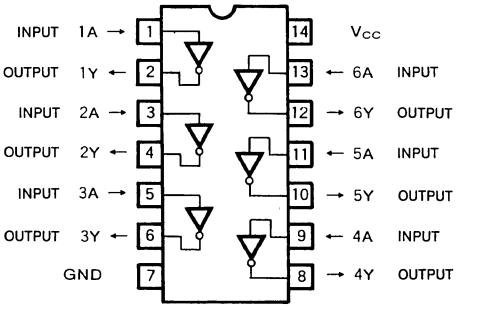
General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS04P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

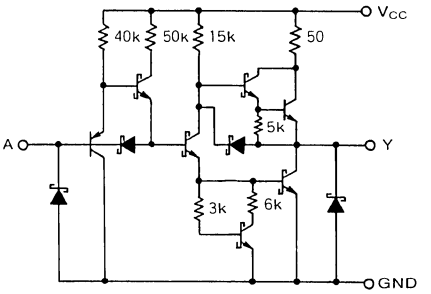
When input A is high-level, output Y is low-level, and when the input is low, the output is high.

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




UNIT: Ω

## FUNCTION TABLE

| Input | Output |
|---|---|
| A | Y |
| L | H |
| H | L |

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | High-level state | −0.5 ~ $V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 ~ +75 | °C |
| $T_{stg}$ | Storage temperature range | | −65 ~ +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $T_a$=0~70℃ | 2.7 | 3.4 | | V |
| | | $I_{OH}$=−0.4mA | $T_a$=−20~+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.65 | 1.1 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 2.4 | 3.8 | mA |

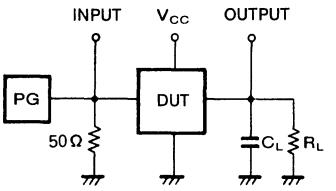
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=500Ω | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=500Ω | | | | | | |
| | | | | $T_a$=25℃ | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Input | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A | Y | | 5 | | 3 | 6 | 11 | 3 | 6 | 12 | ns |
| $t_{PHL}$ | | | | | 3 | | 2 | 6 | 9 | 2 | 6 | 10 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

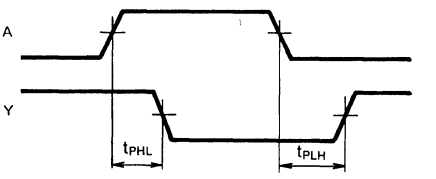
$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

## TIMING DIAGRAM (Reference level = 1.3V)






MITSUBISHI ELECTRIC

# M74ALS05P

## HEX INVERTER WITH OPEN COLLECTOR OUTPUT

## DESCRIPTION

The M74ALS05P is a semiconductor integrated circuit consisting of six inverters with open collector outputs.

## FEATURES

- Wired-AND connectability
- High breakdown output voltage ($V_O \geqq 7V$)
- High speed ($t_{pd} = 11ns$ typical: $C_L = 15pF$)
- Low power dissipation ($P_d = 7.6mW$ typical)
- Wide operating temperature range ($Ta = -20 \sim +75°C$)

## APPLICATIONS

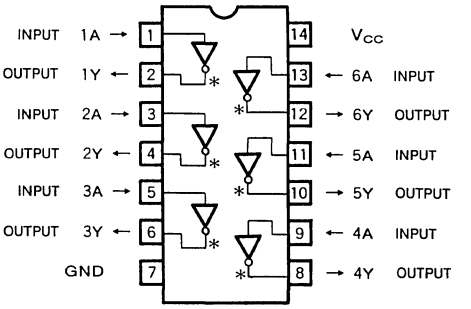
General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

This device employs PNP transistor inputs and open collector outputs. The open collector output enables selection of high-level output impedance with an external resistor. It also permits wired-AND connection which is impossible with ordinary gates. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

When A input is high-level, output Y is low-level, and when the input is low, the output is high.

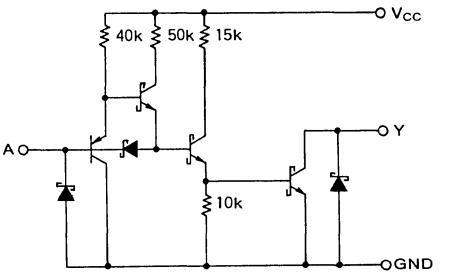
## PIN CONFIGURATION (TOP VIEW)




*. OPEN COLLECTOR OUTPUT

Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




UNIT. Ω

## FUNCTION TABLE

| Input | Output |
|---|---|
| A | Y |
| L | H |
| H | L |

## ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5～+7 | V |
| $V_I$ | Input voltage | | −0.5～+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5～+7 | V |
| Topr | Operating free-air ambient temperature range | | −20～+75 | ℃ |
| Tstg | Storage temperature range | | −65～+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| Topr | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## HEX INVERTER WITH OPEN COLLECTOR OUTPUT

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.65 | 1.1 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 2.4 | 3.8 | mA |

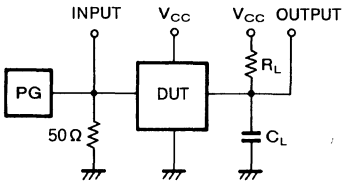
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

### SWITCHING CHARACTERISTICS

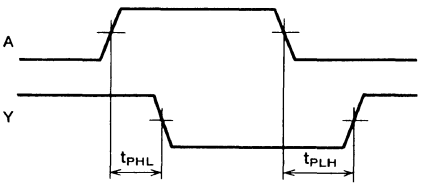
| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=2kΩ | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=2kΩ | | | | | | |
| | | | | $T_a$=25°C | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Input | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A | Y | | 14 | | 23 | 30 | 54 | 23 | 30 | 55 | ns |
| $t_{PHL}$ | | | | | 8 | | 7 | 14 | 23 | 7 | 14 | 26 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS08P

## QUADRUPLE 2-INPUT POSITIVE AND GATE

## DESCRIPTION

The M74ALS08P is a semiconductor integrated circuit consisting of four 2-input positive-logic AND gates, usable as negative-logic OR gates.

## FEATURES

- High speed ($t_{pd}$ = 6ns typical: $C_L$ = 15pF)
- Low power dissipation ($P_d$ = 8.8mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS08P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

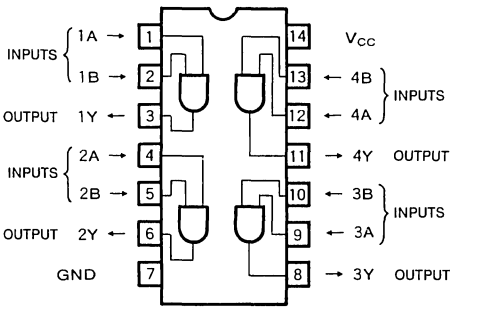
When both A and B inputs are high-level, output Y is high-level, and when at least one of the inputs is low, the output is low.

The buffer version of M74ALS08P, the M74ALS1008P ($I_{OL}$ = 24mA), is also available.

## FUNCTION TABLE

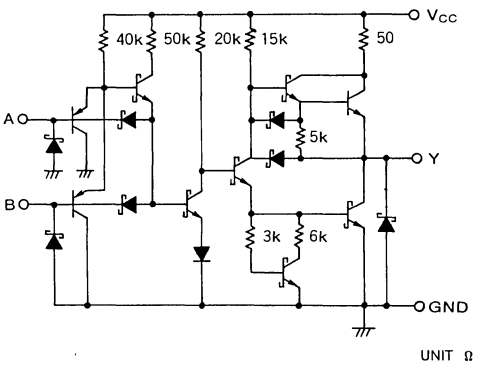
| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | L |
| H | L | L |
| L | H | L |
| H | H | H |

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | −65~+150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## QUADRUPLE 2-INPUT POSITIVE AND GATE

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $T_a$=0~70℃ | 2.7 | 3.4 | | V |
| | | $I_{OH}$=−0.4mA | $T_a$=−20~+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=4.5V | | | 1.3 | 2.4 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=0V | | | 2.2 | 4 | mA |

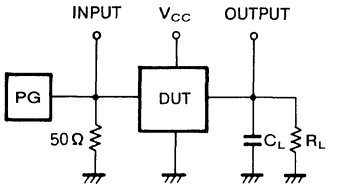
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

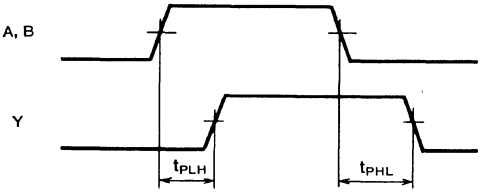
| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=500Ω | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=500Ω | | | | | | |
| | | | | $T_a$=25℃ | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | | 7 | | 4 | 8 | 14 | 4 | 8 | 15 | ns |
| $t_{PHL}$ | | | | | 5 | | 3 | 7 | 10 | 3 | 7 | 11 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS09P

## QUADRUPLE 2-INPUT POSITIVE AND GATE WITH OPEN COLLECTOR OUTPUT

## DESCRIPTION

The M74ALS09P is a semiconductor integrated circuit consisting of four 2-input positive-logic AND gates with open collector outputs, usable as negative-logic OR gates.

## FEATURES

- Wired-AND connectability
- High breakdown output voltage ($V_O \geqq 7V$)
- High speed ($t_{pd} = 14.5ns$ typical: $C_L = 15pF$)
- Low power dissipation ($P_d = 8.9mW$ typical)
- Wide operating temperature range ($Ta = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

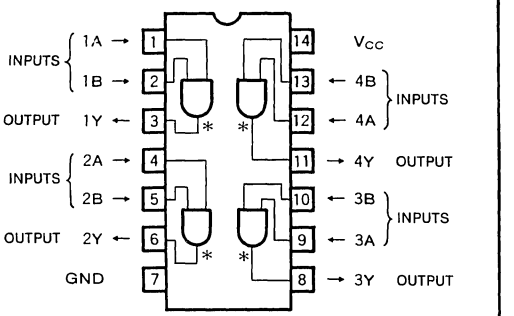
This device employs PNP transistor inputs and open collector outputs. The open collector output enables selection of high-level output impedance with an external resistor. It also permits wired-AND connection which is impossible with ordinary gates. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

When both A and B inputs are high-level, output Y is high-level, and when at least one of the inputs is low, the output is low.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | L |
| H | L | L |
| L | H | L |
| H | H | H |

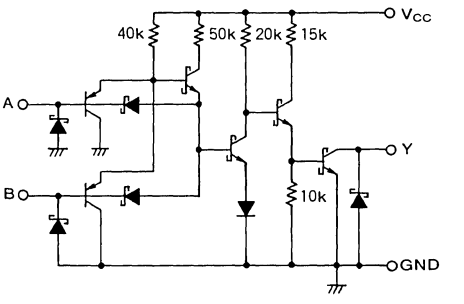
## PIN CONFIGURATION (TOP VIEW)




* . OPEN COLLECTOR OUTPUT

Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




UNIT: Ω

## ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5～+7 | V |
| $V_I$ | Input voltage | | −0.5～+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5～+7 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20～+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65～+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## QUADRUPLE 2-INPUT POSITIVE AND GATE WITH OPEN COLLECTOR OUTPUT

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=4.5V | | | 1.35 | 2.4 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=0V | | | 2.2 | 4 | mA |

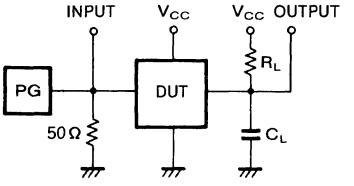
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

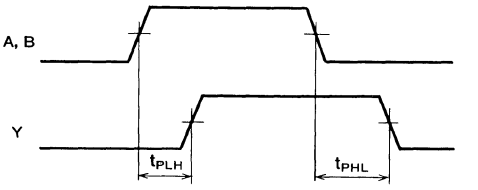
| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=2kΩ | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=2kΩ | | | | | | |
| | | | | $T_a$=25°C | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | | 17 | | 23 | 30 | 54 | 23 | 30 | 55 | ns |
| $t_{PHL}$ | | | | | 12 | | 5 | 15 | 25 | 5 | 15 | 28 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS10P

## TRIPLE 3-INPUT POSITIVE NAND GATE

## DESCRIPTION

The M74ALS10P is a semiconductor integrated circuit consisting of three 3-input positive-logic NAND gates, usable as negative-logic NOR gates.

## FEATURES

- High speed ($t_{pd}$ = 5.5ns typical: $C_L$ = 15pF)
- Low power dissipation ($P_d$ = 3.8mW typical)
- Low output imepdance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS10P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

When A, B and C inputs are simultaneously high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

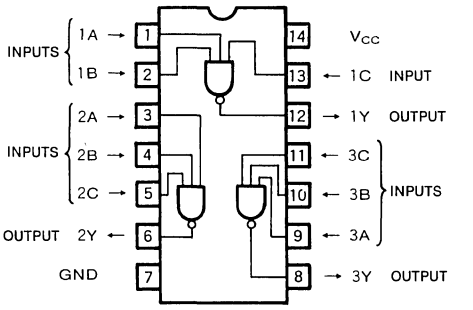
The buffer version of M74ALS10P, the M74ALS1010P ($I_{OL}$ = 24mA), is also available.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | N | Y |
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

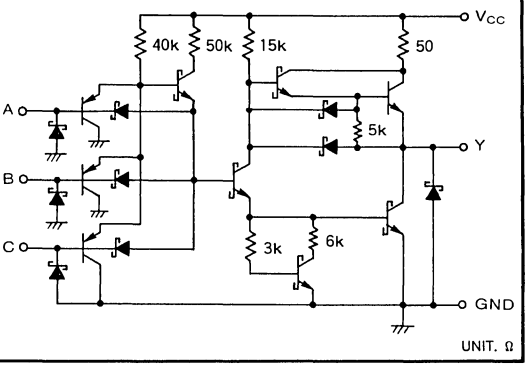
N=B · C

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | −65~+150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## TRIPLE 3-INPUT POSITIVE NAND GATE

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $T_a$=0~70℃ | 2.7 | 3.4 | | V |
| | | $I_{OH}$=−0.4mA | $T_a$=−20~+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.32 | 0.6 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 1.2 | 2.2 | mA |

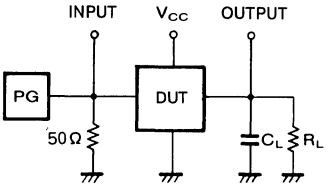
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

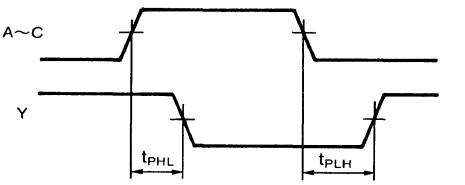
| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=500Ω | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=500Ω | | | | | | |
| | | | | $T_a$=25℃ | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B, C | Y | | 5 | | 3 | 6 | 11 | 3 | 6 | 12 | ns |
| $t_{PHL}$ | | | | | 6 | | 4 | 8 | 18 | 4 | 8 | 19 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.



MITSUBISHI ELECTRIC

# M74ALS11P

## TRIPLE 3-INPUT POSITIVE AND GATE

## DESCRIPTION

The M74ALS11P is a semiconductor integrated circuit consisting of three 3-input positive-logic AND gates, usable as negative-logic OR gates.

## FEATURES

- High speed ($t_{pd}$ = 6.5ns typical: $C_L$ = 15pF)
- Low power dissipation ($P_d$ = 6.5mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS11P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

When A, B, and C inputs are simultaneously high-level, output Y is high-level, and when at least one of the inputs is low, the output is low.

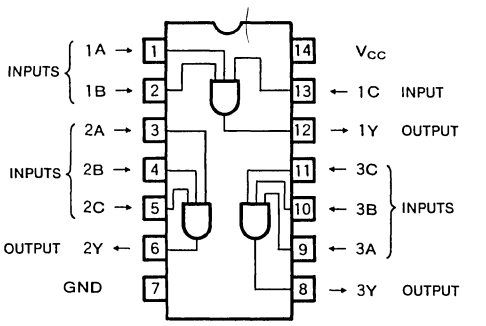
The buffer version of M74ALS11P, the M74ALS1011P ($I_{OL}$ = 24mA), is also available.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | N | Y |
| L | L | L |
| H | L | L |
| L | H | L |
| H | H | H |

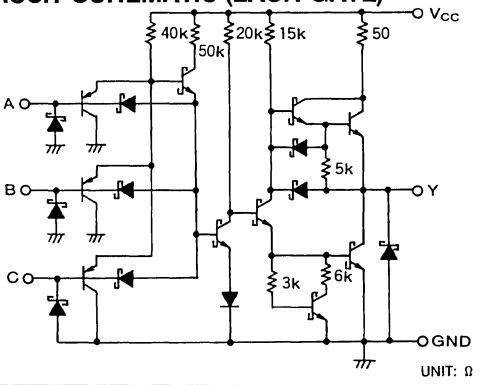
N=B · C

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | High-level state | −0.5 ~ $V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 ~ +75 | °C |
| $T_{stg}$ | Storage temperature range | | −65 ~ +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## TRIPLE 3-INPUT POSITIVE AND GATE

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $T_a$=0~70℃ | 2.7 | 3.4 | | V |
| | | $I_{OH}$=−0.4mA | $T_a$=−20~+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=4.5V | | | 1 | 1.8 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=0V | | | 1.6 | 3 | mA |

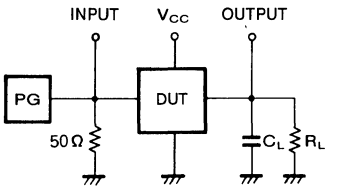
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

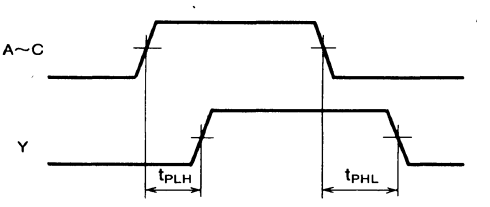
| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=500Ω | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=500Ω | | | | | | |
| | | | | $T_a$=25℃ | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B, C | Y | | 8 | | 5 | 9 | 20 | 5 | 9 | 21 | ns |
| $t_{PHL}$ | | | | | 5 | | 3 | 7 | 10 | 3 | 7 | 11 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS12P

## TRIPLE 3-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

## DESCRIPTION

The M74ALS12P is a semiconductor integrated circuit consisting of three 3-input positive-logic NAND gates with open collector outputs, usable as negative-logic NOR gates.

## FEATURES

- Wired-AND connectability
- High breakdown output voltage ($V_O \geqq 7V$)
- High speed ($t_{pd} = 13.5ns$ typical: $C_L = 15pF$)
- Low power dissipation ($P_d = 3.8mW$ typical)
- Wide operating temperature range ($Ta = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

This device employs PNP transistor inputs and open collector outputs. The open collector output enables selection of high-level output impedance with an external resistor. It also permits wired-AND connection which is impossible with ordinary gates. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

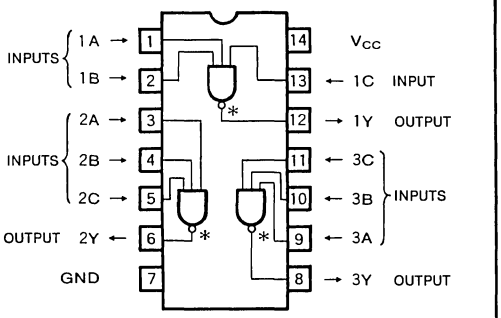
When A, B, and C inputs are simultaneously high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | N | Y |
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

N=B · C

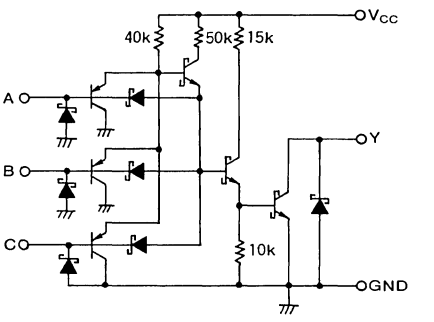
## PIN CONFIGURATION (TOP VIEW)




* : OPEN COLLECTOR OUTPUT

Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




UNIT: Ω

## ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5～+7 | V |
| $V_I$ | Input voltage | | −0.5～+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5～+7 | V |
| Topr | Operating free-air ambient temperature range | | −20～+75 | ℃ |
| Tstg | Storage temperature range | | −65～+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| Topr | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## TRIPLE 3-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.32 | 0.6 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 1.2 | 2.2 | mA |

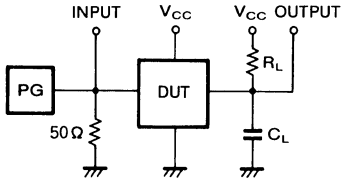
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=2kΩ | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=2kΩ | | | | | | |
| | | | | $T_a$=25°C | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B, C | Y | | 14 | | 23 | 30 | 54 | 23 | 30 | 55 | ns |
| $t_{PHL}$ | | | | | 13 | | 9 | 18 | 30 | 9 | 18 | 33 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

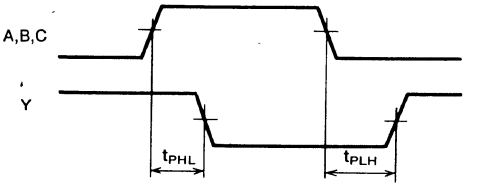
$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

### TIMING DIAGRAM (Reference level = 1.3V)






MITSUBISHI ELECTRIC

# M74ALS15P

## TRIPLE 3-INPUT POSITIVE AND GATE WITH OPEN COLLECTOR OUTPUT

## DESCRIPTION

The M74ALS15P is a semiconductor integrated circuit consisting of three 3-input positive-logic AND'gates with open collector outputs, usable as negative-logic OR gates.

## FEATURES

- Wired-AND connectability
- High breakdown output voltage ($V_O \geqq 7V$)
- High speed ($t_{pd} = 14.5ns$ typical: $C_L = 15pF$)
- Low power dissipation ($P_d = 6.7mW$ typical)
- Wide operating temperature range ($Ta = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

This device employs PNP transistor inputs and open collector outputs. The open collector output enables selection of high-level output impedance with an external resistor. It also permits wired-AND connection which is impossible with ordinary gates. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

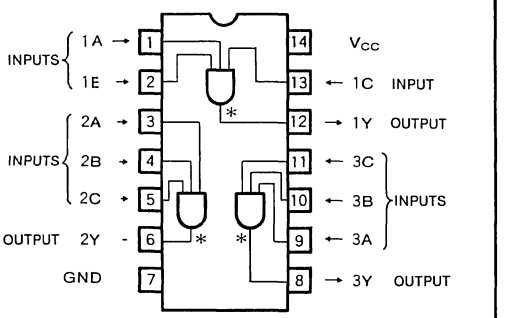
When A, B, and C inputs are simultaneously high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | N | Y |
| L | L | L |
| H | L | L |
| L | H | L |
| H | H | H |

$N = B \cdot C$

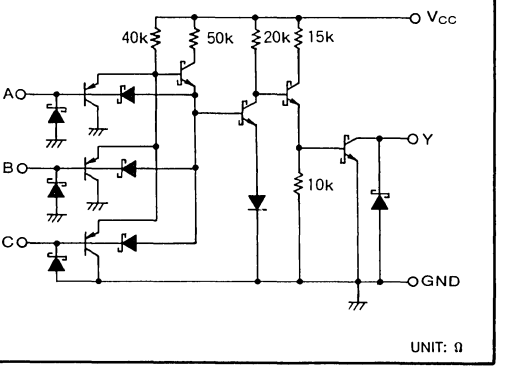
## PIN CONFIGURATION (TOP VIEW)




*. OPEN COLLECTOR OUTPUT

Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




UNIT: Ω

## ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5～+7 | V |
| $V_I$ | Input voltage | | −0.5～+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5～+7 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20～+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65～+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## TRIPLE 3-INPUT POSITIVE AND GATE WITH OPEN COLLECTOR OUTPUT

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=4.5V | | | 1 | 1.8 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=0V | | | 1.66 | 3 | mA |

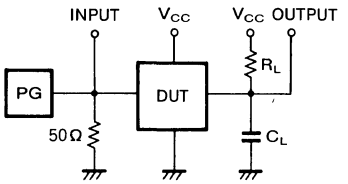
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1), $C_L$=15pF, $R_L$=2kΩ | | | $V_{CC}$=4.5~5.5V (Note 1), $C_L$=50pF, $R_L$=2kΩ | | | | | | |
| | | | | $T_a$=25℃ | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B, C | Y | | 17 | | 23 | 30 | 54 | 23 | 30 | 55 | ns |
| $t_{PHL}$ | | | | | 12 | | 6 | 16 | 26 | 6 | 16 | 29 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1. Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

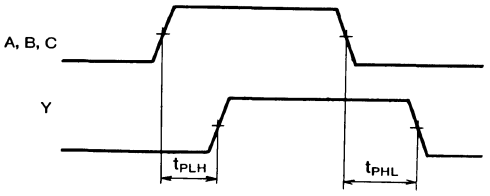
$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

### TIMING DIAGRAM (Reference level = 1.3V)






MITSUBISHI ELECTRIC

# M74ALS20AP

## DUAL 4-INPUT POSITIVE NAND GATE

## DESCRIPTION

The M74ALS20AP is a semiconductor integrated circuit consisting of two 4-input positive-logic NAND gates, usable as negative-logic NOR gates.

## FEATURES

- High speed ($t_{pd}$ = 5ns typical: $C_L$ = 15pF)
- Low power dissipation ($P_d$ = 2.6mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS20AP achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

When A, B, C, and D inputs are simultaneously high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

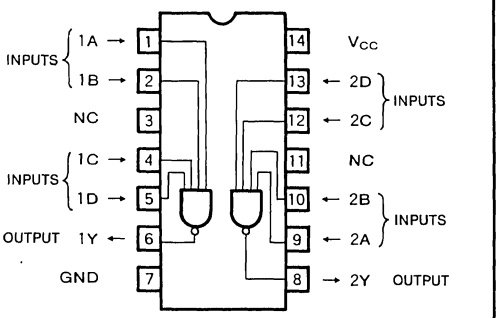
The buffer version of M74ALS20AP, the M74ALS1020P ($I_{OL}$ = 24mA), is also available.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | N | Y |
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

N=B · C · D

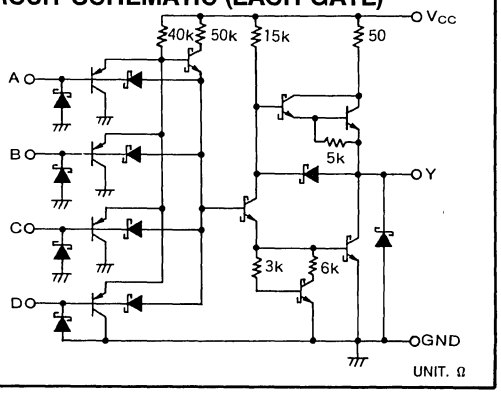
## PIN CONFIGURATION (TOP VIEW)




NC NO CONNECTION

Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $T_a$=0~70°C | 2.7 | 3.4 | | V |
| | | $I_{OH}$=−0.4mA | $T_a$=−20~+75°C | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.22 | 0.4 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 0.81 | 1.5 | mA |

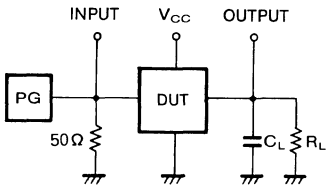
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

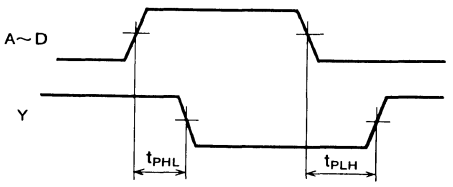
| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=500Ω | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=500Ω | | | | | | |
| | | | | $T_a$=25°C | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B C, D | Y | | 5 | | 3 | 6 | 11 | 3 | 6 | 12 | ns |
| $t_{PHL}$ | | | | | 5 | | 3 | 7 | 10 | 3 | 7 | 11 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS21P

## DUAL 4-INPUT POSITIVE AND GATE

## DESCRIPTION

The M74ALS21P is a semiconductor integrated circuit consisting of two 4-input positive-logic AND gates, usable as negative-logic OR gates.

## FEATURES

- High speed ($t_{pd}$ = 6.5ns typical: $C_L$ = 15pF)
- Low power dissipation ($P_d$ = 4.4mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS21P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

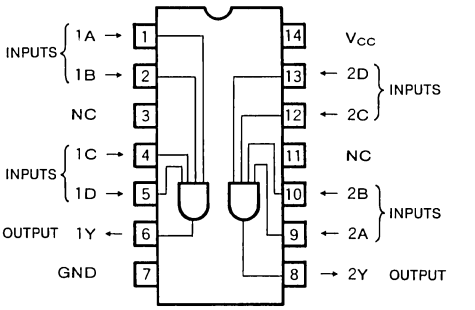
When A, B, C, and D inputs are simultaneously high-level, output Y is high-level, and when at least one of the inputs is low, the output is low.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | N | Y |
| L | L | L |
| H | L | L |
| L | H | L |
| H | H | H |

N=B · C · D

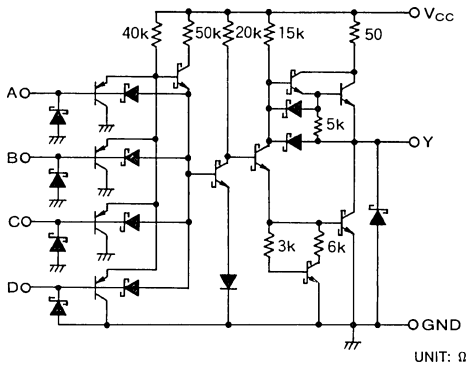
## PIN CONFIGURATION (TOP VIEW)




NC NO CONNECTION

Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




UNIT: Ω

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | −65~+150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $T_a$=0~70℃ | 2.7 | 3.4 | | V |
| | | $I_{OH}$=−0.4mA | $T_a$=−20~+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=4.5V | | | 0.67 | 1.2 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=0V | | | 1.1 | 2 | mA |

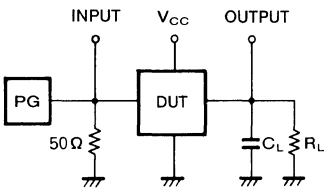
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=500Ω | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=500Ω | | | | | | |
| | | | | $T_a$=25℃ | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | | 8 | | 6 | 10 | 26 | 6 | 10 | 27 | ns |
| $t_{PHL}$ | | C, D | | | 5 | | 3 | 7 | 10 | 3 | 7 | 11 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

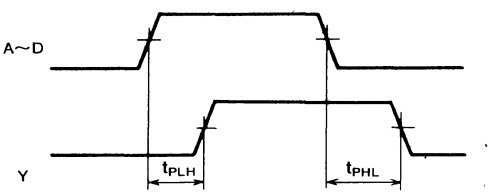
$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

## TIMING DIAGRAM (Reference level = 1.3V)






MITSUBISHI ELECTRIC

# M74ALS22AP

## DUAL 4-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

## DESCRIPTION

The M74ALS22AP is a semiconductor integrated circuit consisting of two 4-input positive-logic NAND gates with open collector outputs, usable as negative-logic NOR gates.

## FEATURES

- Wired-AND connectability
- High breakdown output voltage ($V_O \geqq 7V$)
- High speed ($t_{pd}$ = 13ns typical: $C_L$ = 15pF)
- Low power dissipation ($P_d$ = 2.6mW typical)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

This device employs PNP transistor inputs and open collector outputs. The open collector output enables selection of high-level output impedance with an external resistor. It also permits wired-AND connection which is impossible with ordinary gates. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

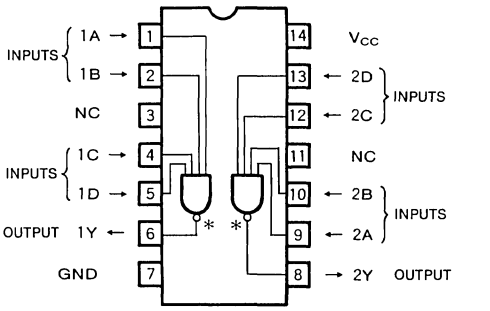
When A, B, C, and D inputs are simultaneously high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | N | Y |
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

N=B・C・D

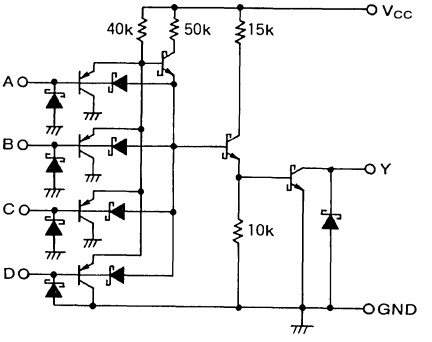
## PIN CONFIGURATION (TOP VIEW)




*. OPEN COLLECTOR OUTPUT
NC: NO CONNECTION

Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




UNIT: Ω

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~+7 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | −65~+150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## DUAL 4-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.22 | 0.4 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 0.8 | 1.5 | mA |

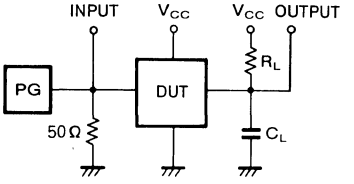
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

### SWITCHING CHARACTERISTICS

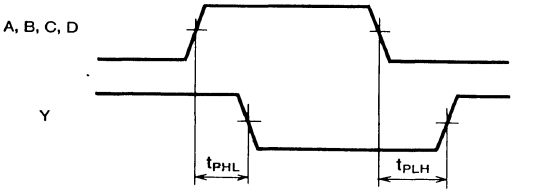
| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=2kΩ | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=2kΩ | | | | | | |
| | | | | $T_a$=25°C | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | | 14 | | 23 | 30 | 54 | 23 | 30 | 55 | ns |
| $t_{PHL}$ | | C, D | | | 12 | | 9 | 16 | 30 | 9 | 16 | 35 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS27P

## TRIPLE 3-INPUT POSITIVE NOR GATE

## DESCRIPTION

The M74ALS27P is a semiconductor integrated circuit consisting of three 3-input positive-logic NOR gates, usable as negative-logic NAND gates.

## FEATURES

- High speed ($t_{pd}$ = 6.5ns typical: $C_L$ = 15pF)
- Low power dissipation ($P_d$ = 7.4mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS27P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

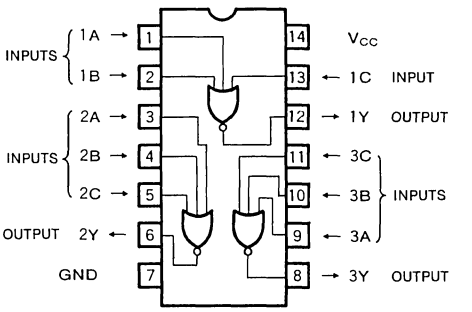
When A, B, and C inputs are simultaneously low-level, output Y is high-level, and when at least one of the inputs is high, the output is low.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | N | Y |
| L | L | H |
| H | L | L |
| L | H | L |
| H | H | L |

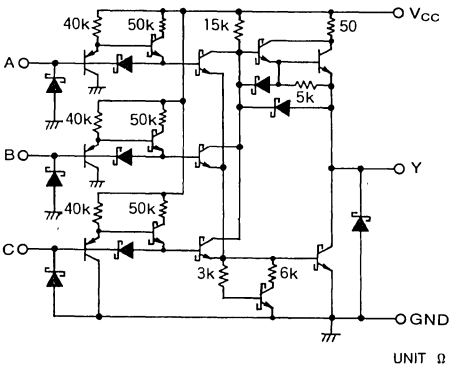
N=B+C

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | −65~+150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## TRIPLE 3-INPUT POSITIVE NOR GATE

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $T_a$=0~70℃ | 2.7 | 3.4 | | V |
| | | $I_{OH}$=−0.4mA | $T_a$=−20~+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.97 | 1.8 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 2 | 4 | mA |

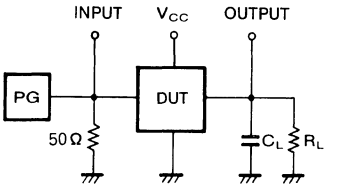
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

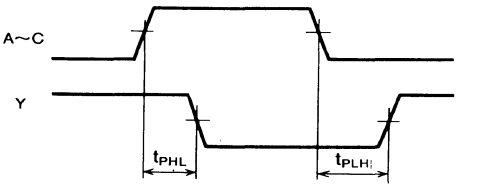
| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=500Ω | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=500Ω | | | | | | |
| | | | | $T_a$=25℃ | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B, C | Y | | 9 | | 4 | 10 | 15 | 4 | 10 | 16 | ns |
| $t_{PHL}$ | | | | | 4 | | 3 | 6 | 9 | 3 | 6 | 10 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.



MITSUBISHI ELECTRIC

# M74ALS28P

## QUADRUPLE 2-INPUT POSITIVE NOR BUFFER

## DESCRIPTION

The M74ALS28P is a semiconductor integrated circuit consisting of four 2-input positive-logic NOR buffer gates, usable as negative-logic NAND buffer gates.

## FEATURES

- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High speed ($t_{pd}$ = 5ns typical: $C_L$ = 50pF)
- Low power dissipation ($P_d$ = 16.3mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS28P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

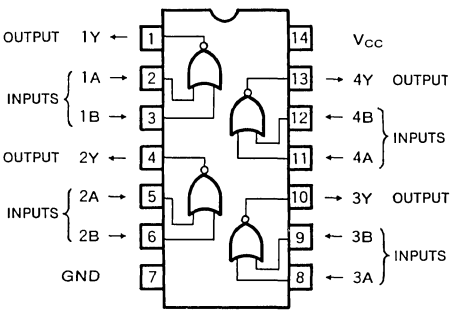
When both A and B inputs are low-level, output Y is high-level and when at least one of the inputs is high, the output is low.

The M74ALS1002P, which, except for its name, is identical in all respects to the M74ALS28P, is also available.

## FUNCTION TABLE

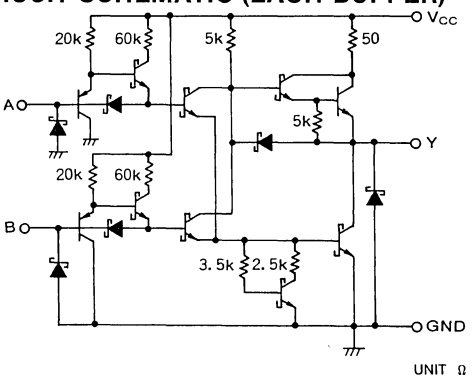
| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| H | L | L |
| L | H | L |
| H | H | L |

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## QUADRUPLE 2-INPUT POSITIVE NOR BUFFER

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 1.7 | 2.8 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 4.8 | 8 | mA |

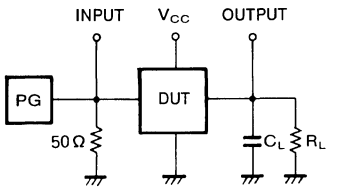
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

### SWITCHING CHARACTERISTICS

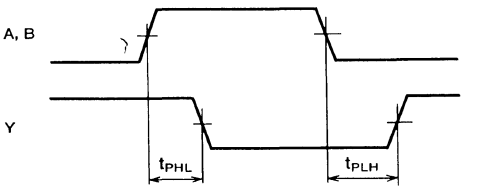
| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V, $C_L$=50pF, $R_L$=500Ω (Note 1) | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | 2 | 5 | 8 | 2 | 5 | 9 | ns |
| $t_{PHL}$ | | | | 3 | 5 | 8 | 3 | 5 | 9 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics.

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS30P

## SINGLE 8-INPUT POSITIVE NAND GATE

## DESCRIPTION

The M74ALS30P is a semiconductor integrated circuit consisting of one 8-input positive-logic NAND gate, usable as a negative-logic NOR gate.

## FEATURES

- High speed ($t_{pd}$ = 6.5ns typical: $C_L$ = 15pF)
- Low power dissipation ($P_d$ = 1.9mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the output, the M74ALS30P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and output reduces ringing and undershooting.

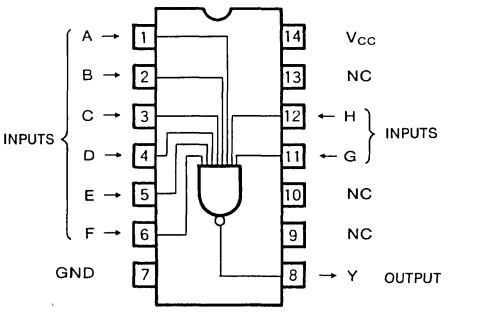
When A, B, C, D, E, F, G, and H inputs are simultaneously high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | N | Y |
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

N=B・C・D・E・F・G・H

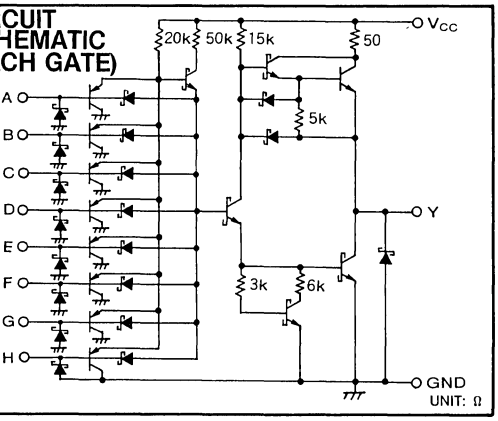
## PIN CONFIGURATION (TOP VIEW)




NC. NO CONNECTION

Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | −65~+150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## SINGLE 8-INPUT POSITIVE NAND GATE

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $T_a$=0~70°C | 2.7 | 3.4 | | V |
| | | $I_{OH}$=−0.4mA | $T_a$=−20~+75°C | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.22 | 0.36 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 0.54 | 0.9 | mA |

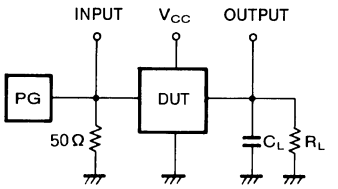
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

### SWITCHING CHARACTERISTICS

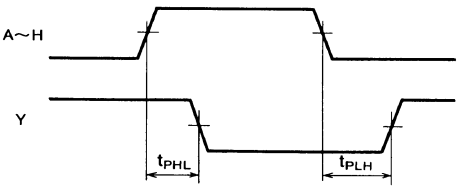
| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=500Ω | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=500Ω | | | | | | |
| | | | | $T_a$=25°C | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A~H | Y | | 5 | | 3 | 6 | 11 | 3 | 6 | 12 | ns |
| $t_{PHL}$ | | | | | 8 | | 5 | 10 | 20 | 5 | 10 | 21 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS32P

## QUADRUPLE 2-INPUT POSITIVE OR GATE

## DESCRIPTION

The M74ALS32P is a semiconductor integrated circuit consisting of four 2-input positive-logic OR gates, usable as negative-logic AND gates.

## FEATURES

- High speed ($t_{pd}$ = 6.5ns typical: $C_L$ = 15pF)
- Low power dissipation ($P_d$ = 11.3mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS32P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

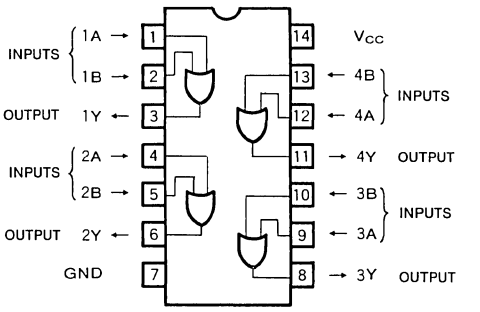
When both A and B inputs are low-level, output Y is low-level, and when at least one of the inputs is high, the output is high.

The buffer version of M74ALS32P, the M74ALS1032P ($I_{OL}$ = 24mA), is also available.

## FUNCTION TABLE

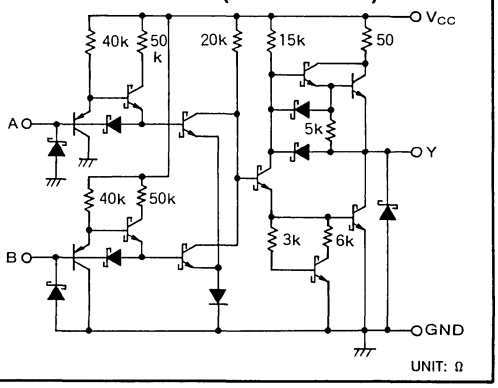
| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | L |
| H | L | H |
| L | H | H |
| H | H | H |

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH GATE)




## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## QUADRUPLE 2-INPUT POSITIVE OR GATE

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $T_a$=0~70°C | 2.7 | 3.4 | | V |
| | | $I_{OH}$=−0.4mA | $T_a$=−20~+75°C | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=4.5V | | | 1.9 | 4 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=0V | | | 2.6 | 4.9 | mA |

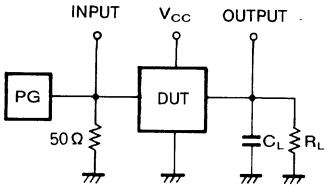
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

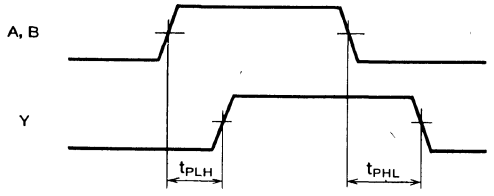
| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 1) $C_L$=15pF $R_L$=500Ω | | | $V_{CC}$=4.5~5.5V (Note 1) $C_L$=50pF $R_L$=500Ω | | | | | | |
| | | | | $T_a$=25°C | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | | 7 | | 3 | 10 | 14 | 3 | 10 | 15 | ns |
| $t_{PHL}$ | | | | | 6 | | 3 | 8 | 12 | 3 | 8 | 13 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS33P

## QUADRUPLE 2-INPUT POSITIVE NOR BUFFER WITH OPEN COLLECTOR OUTPUT

## DESCRIPTION

The M74ALS33P is a semiconductor integrated circuit consisting of four 2-input positive-logic NOR buffer gates with open collector outputs, usable as negative-logic NAND buffer gates.

## FEATURES

- Wired-AND connectability
- High fan-out ($I_{OL}$ = 24mA)
- High breakdown output voltage ($V_O \geqq 7V$)
- High speed ($t_{pd}$ = 15.5ns typical: $C_L$ = 50pF)
- Low power dissipation ($P_d$ = 16.3mW typical)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

This device employs PNP transistor inputs and open collector outputs. The open collector output enables selection of high-level output impedance with an external resistor. It also permits wired-AND connection which is impossible with ordinary gates.

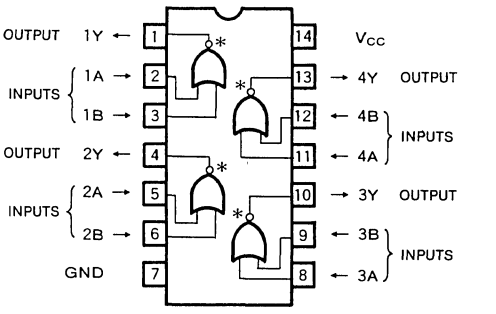
Having a large low-level output current ($I_{OL}$) of 24mA, it is suitable for a buffer gate. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

When both A and B inputs are low-level, output Y is high-level, and when at least one of the inputs is high, the output is low.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| H | L | L |
| L | H | L |
| H | H | L |

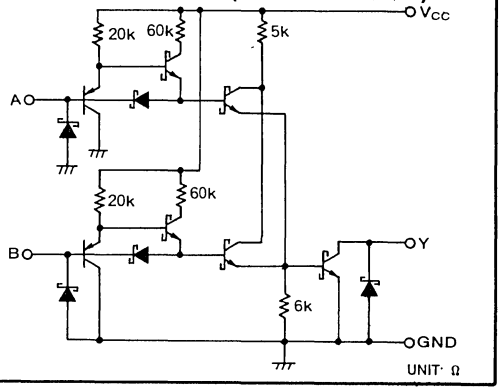
## PIN CONFIGURATION (TOP VIEW)




∗: OPEN COLLECTOR OUTPUT

Outline 14P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~+7 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## QUADRUPLE 2-INPUT POSITIVE NOR BUFFER WITH OPEN COLLECTOR OUTPUT

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 1.7 | 2.8 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 4.8 | 8 | mA |

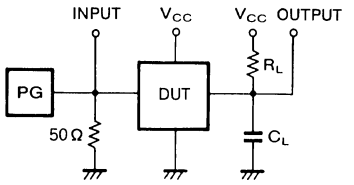
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

## SWITCHING CHARACTERISTICS

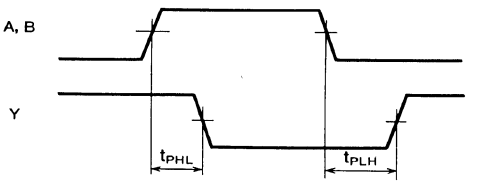
| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 1), $C_L$=50pF, $R_L$=680Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | 10 | 18 | 33 | 10 | 18 | 34 | ns |
| $t_{PHL}$ | | | | 7 | 13 | 18 | 7 | 13 | 19 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1. Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.



MITSUBISHI ELECTRIC

# M74ALS37P

## QUADRUPLE 2-INPUT POSITIVE NAND BUFFER

## DESCRIPTION

The M74ALS37P is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND buffer gates, usable as negative-logic NOR buffer gates.

## FEATURES

- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High speed ($t_{pd}$ = 5ns typical: $C_L$ = 50pF)
- Low power dissipation ($P_d$ = 12.2mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS37P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

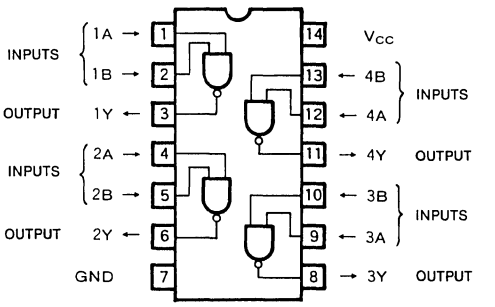
When both A and B inputs are high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

The M74ALS1000P, which, except for its name, is identical in all respects to the M74ALS37P, is also available.

## FUNCTION TABLE

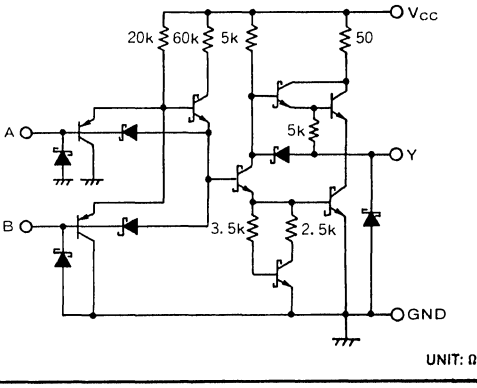
| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT: Ω

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## QUADRUPLE 2-INPUT POSITIVE NAND BUFFER

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.86 | 1.6 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 4 | 6.4 | mA |

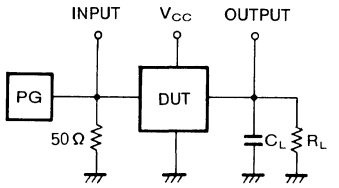
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 1), $C_L$=50pF, $R_L$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Output | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | 2 | 5 | 8 | 2 | 5 | 9 | ns |
| $t_{PHL}$ | | | | 3 | 5 | 8 | 3 | 5 | 9 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

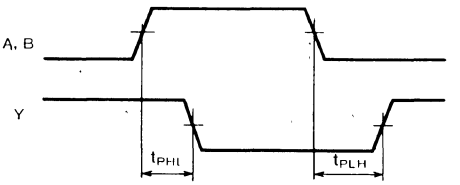
$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance

### TIMING DIAGRAM (Reference level = 1.3V)






MITSUBISHI ELECTRIC

# M74ALS38P

## QUADRUPLE 2-INPUT POSITIVE NAND BUFFER WITH OPEN COLLECTOR OUTPUT

## DESCRIPTION

The M74ALS38P is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND buffer gates with open collector outputs, usable as negative-logic NOR buffer gates.

## FEATURES

- Wired-AND connectability
- High fan-out ($I_{OL}$ = 24mA)
- High-breakdown output voltage ($V_O \geqq 7V$)
- High speed ($t_{pd}$ = 16.5ns typical: $C_L$ = 50pF)
- Low power dissipation ($P_d$ = 12.2mW typical)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

This device employs PNP transistor inputs and open collector outputs. The open collector output enables selection of high-level output impedance with an external resistor. It also permits wired-AND connection which is impossible with ordinary gates. Having a large low-level output current ($I_{OL}$) of 24mA, it is suitable for a buffer gate. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

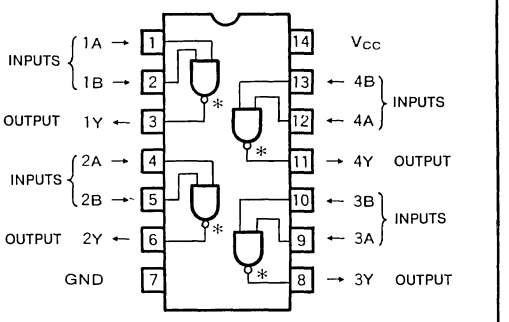
When both A and B inputs are high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

The M74ALS1003P , which, except for its name, is identical in all respects to the M74ALS38P, is also available.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

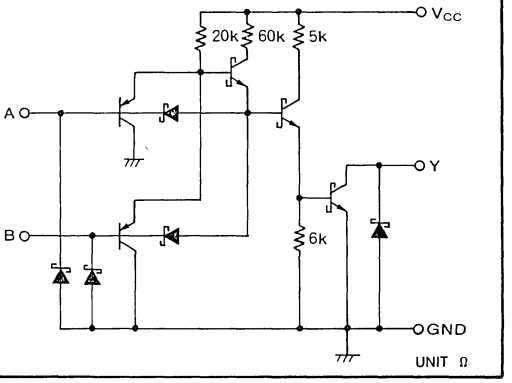
## PIN CONFIGURATION (TOP VIEW)




*. OPEN COLLECTOR OUTPUT

Outline 14P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~+7 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | −65~+150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## QUADRUPLE 2-INPUT POSITIVE NAND BUFFER WITH OPEN COLLECTOR OUTPUT

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.86 | 1.6 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 4 | 6.4 | mA |

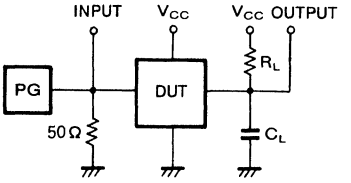
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

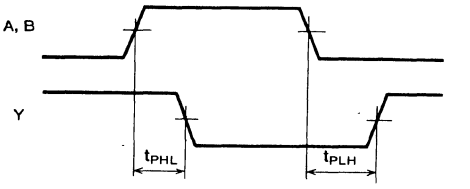
| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 1), $C_L$=50pF, $R_L$=680Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Output | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | 10 | 20 | 33 | 10 | 20 | 34 | ns |
| $t_{PHL}$ | | | | 7 | 13 | 18 | 7 | 13 | 19 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS40P

## DUAL 4-INPUT POSITIVE NAND BUFFER

## DESCRIPTION

The M74ALS40P is a semiconductor integrated circuit consisting of two 4-input positive-logic NAND buffer gates, usable as negative-logic NOR buffer gates.

## FEATURES

- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High speed ($t_{pd}$ = 5ns typical: $C_L$ = 50pF)
- Low power dissipation ($P_d$ = 6.1mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS40P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

When A, B, C, and D inputs are simultaneously high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

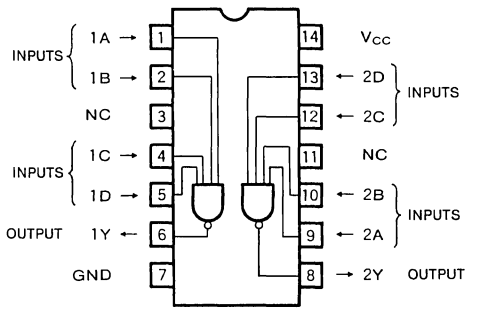
The M74ALS1020P, which, except for its name, is identical in all respects to the M74ALS40P, is also available.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | N | Y |
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

N=B · C · D

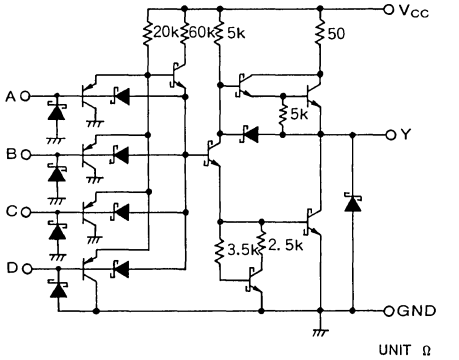
## PIN CONFIGURATION (TOP VIEW)




NC NO CONNECTION

Outline 14P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT Ω

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.43 | 0.8 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 2 | 3.2 | mA |

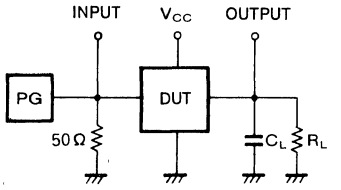
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

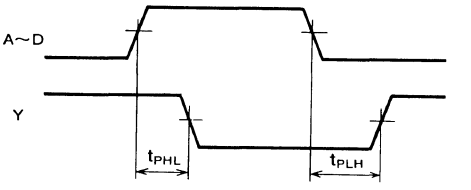
| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V, $C_L$=50pF, $R_L$=500Ω (Note 1) | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Output | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | A~D | Y | 2 | 5 | 8 | 2 | 5 | 9 | ns |
| $t_{PHL}$ | | | | 3 | 5 | 8 | 3 | 5 | 9 | |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS74P

## DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP WITH SET AND RESET

## DESCRIPTION

The M74ALS74P is a semiconductor integrated circuit consisting of two D-type positive edge-triggered flip-flop circuits. Each of the circuits has independent inputs such as data D, clock T, direct set $\overline{S_D}$ and direct reset $\overline{R_D}$.

## FEATURES

- Positive edge-triggering
- Independent inputs and outputs for each flip-flop
- Direct set and reset inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

When T changes from low-level to high-level, the D signal just before the change appears at Q and $\overline{Q}$ outputs in accordance with the function table. Use of $\overline{S_D}$ and $\overline{R_D}$ allows direct R-S flip-flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low-level, Q and $\overline{Q}$ are high-level. But if $\overline{S_D}$ and $\overline{R_D}$ become high simultaneously from this condition, the state of Q and $\overline{Q}$ cannot be predicted. When used as a D-type flip-flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained in high-level.

## FUNCTION TABLE (Note 1)

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| $\overline{S_D}$ | $\overline{R_D}$ | T | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H* | H* |
| H | H | L | X | $Q^0$ | $\overline{Q}^0$ |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |

Note 1 ↑ Transition from low to high level (positive edge trigger)

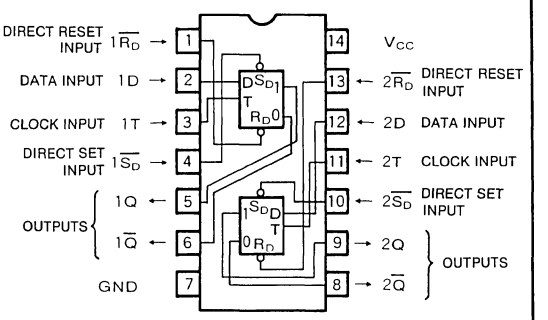
$Q^0$ : Level of Q before the indicated steady-state input conditions were established

$\overline{Q}^0$ : Level of $\overline{Q}$ before the indicated steady-state input conditions were established.

X : Irrelevant

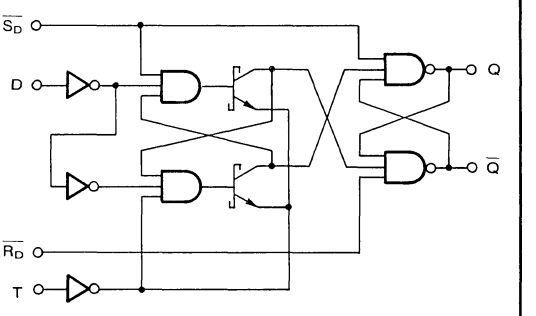
* : When $\overline{S_D}$ or $\overline{R_D}$ is near $V_{IL\,MAX}$ in this condition, the level of $V_{OH}$ is not guaranteed. Moreover, if $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high-level from this condition then the state of Q and $\overline{Q}$ cannot be predicted.

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## LOGIC DIAGRAM (EACH FLIP-FLOP)




## ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5～+7 | V |
| $V_I$ | Input voltage | | −0.5～+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5～$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20～+75 | °C |
| $T_{stg}$ | Storage temperature range | | −65～+150 | °C |

## DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP WITH SET AND RESET

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V, $I_{OH}$=−0.4mA | $T_a$=0~70℃ | 2.7 | 3.4 | | V |
| | | | | $T_a$=−20~+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | D, T | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | $\overline{S_D}$, $\overline{R_D}$ | | | | | 0.2 | |
| $I_{IH}$ | High-level input current | D, T | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | $\overline{S_D}$, $\overline{R_D}$ | | | | | 40 | |
| $I_{IL}$ | Low-level input current | D, T | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| | | $\overline{S_D}$, $\overline{R_D}$ | | | | | −0.4 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −10 | | −60 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$=5.5V (Note 2) | | | 2.4 | 4 | mA |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

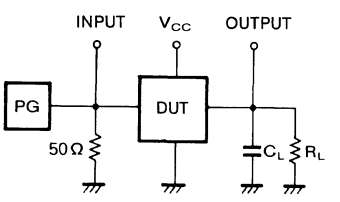
Note 2: The supply current is measured alternately at D = T = $\overline{S_D}$ = 0V, $\overline{R_D}$ = 4.5V (Q = high-level) and D = T = $\overline{R_D}$ = 0V, $\overline{S_D}$ = 4.5V ($\overline{Q}$ = high-level).

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 3), $C_L$=15pF, $R_L$=500Ω | | | $V_{CC}$=4.5~5.5V (Note 3), $C_L$=50pF, $R_L$=500Ω | | | | | | |
| | | | | $T_a$=25℃ | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Outputs | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $f_{max}$ | Maximum clock frequency | T | Q, $\overline{Q}$ | | 50 | | 34 | 43 | | 30 | 43 | | MHz |
| $t_{PLH}$ | Propagation time | $\overline{S_D}$, $\overline{R_D}$ | Q, $\overline{Q}$ | | 6 | | 3 | 7 | 13 | 3 | 7 | 14 | ns |
| $t_{PHL}$ | | | | | 7 | | 5 | 10 | 15 | 5 | 10 | 16 | |
| $t_{PLH}$ | | T | Q, $\overline{Q}$ | | 7 | | 5 | 8 | 16 | 5 | 8 | 17 | ns |
| $t_{PHL}$ | | | | | 8 | | 7 | 11 | 18 | 7 | 11 | 19 | |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 3: Measurement circuit




(1) The pulse generator (PG) has the following characteristics
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

## DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP WITH SET AND RESET

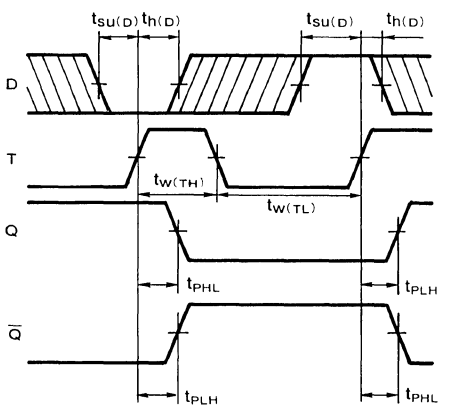
### TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_L$=500Ω)

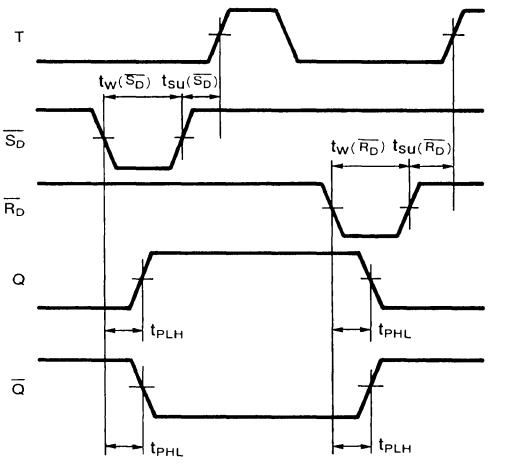
| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{w(TH)}$ | Pulse width | T "H" | 12 | 3 | | 14 | 3 | | ns |
| $t_{w(TL)}$ | | T "L" | 17 | 13 | | 19 | 13 | | |
| $t_{w(\overline{S_D})}$ | | $\overline{S_D}$ "L" | 15 | 6 | | 16 | 6 | | |
| $t_{w(\overline{R_D})}$ | | $\overline{R_D}$ "L" | 15 | 3 | | 16 | 3 | | |
| $t_{su(D)}$ | Setup time before T↑ | D | 15 | 6 | | 16 | 6 | | ns |
| $t_{su(\overline{S_D})}$ | | $\overline{S_D}$ "H" (inactive) | 10 | 3 | | 11 | 3 | | |
| $t_{su(\overline{R_D})}$ | | $\overline{R_D}$ "H" (inactive) | 15 | 8 | | 16 | 8 | | |
| $t_{h(D)}$ | Hold time after T↑ | D | 5 | 0 | | 6 | 0 | | ns |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↑: Transition from low to high level (positive edge trigger)

### TIMING DIAGRAM (Reference level = 1.3V)




Note 4: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS109P

## DUAL J-$\overline{K}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP WITH SET AND RESET

## DESCRIPTION

The M74ALS109P is a semiconductor integrated circuit consisting of two J-$\overline{K}$ positive edge-triggered flip-flop circuits. Each of the circuits has independent inputs J, $\overline{K}$, clock T, direct set $\overline{S_D}$ and direct reset $\overline{R_D}$.

## FEATURES

- Positive edge-triggering
- Independent inputs and outputs for each flip-flop
- Direct set and reset inputs
- J and $\overline{K}$ inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

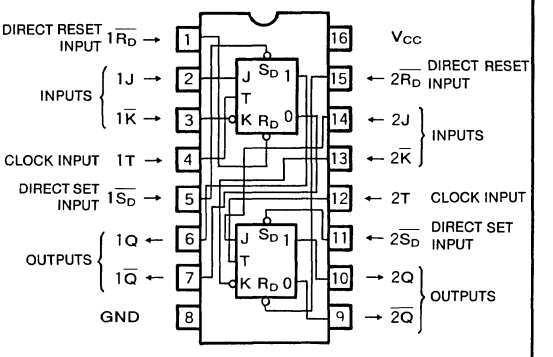
## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

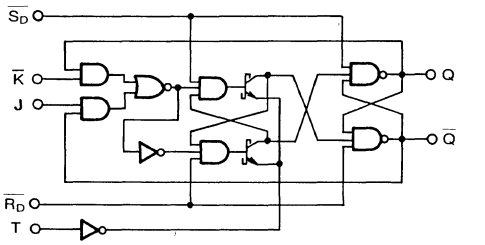
When T changes from low-level to high-level, the signals applied just before the change on J and $\overline{K}$ appear at Q and $\overline{Q}$ outputs in accordance with the function table. Use of $\overline{S_D}$ and $\overline{R_D}$ allows direct R-S flip-flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low-level, Q and $\overline{Q}$ are high-level. But if $\overline{S_D}$ and $\overline{R_D}$ become high simultaneously from this condition, the state of Q and $\overline{Q}$ cannot be predicted. When used as a J-$\overline{K}$ flip-flop, $\overline{S_D}$ and $\overline{R_D}$ should be held at high-level. D-type flip-flop operation is possible by connecting J and $\overline{K}$.

## PIN CONFIGURATION (TOP VIEW)




Outline 16P4

## LOGIC DIAGRAM (EACH FLIP-FLOP)




## FUNCTION TABLE (Note 1)

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| $\overline{S_D}$ | $\overline{R_D}$ | T | J | $\overline{K}$ | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | L | X | X | $Q^0$ | $\overline{Q^0}$ |
| H | H | ↑ | L | L | L | H |
| H | H | ↑ | H | L | Toggle | |
| H | H | ↑ | L | H | $Q^0$ | $\overline{Q^0}$ |
| H | H | ↑ | H | H | H | L |

Note 1 ↑ : Transition from low to high level (positive edge trigger)

$Q^0$ : Level of Q before the indicated steady-state input conditions were established.

$\overline{Q^0}$ : Level of $\overline{Q}$ before the indicated steady-state input conditions were established.

Toggle : Complement of previous state appears on each output with ↑ transition.

X : Irrelevant

* : When $\overline{S_D}$ or $\overline{R_D}$ is near $V_{IL\,MAX}$ in this condition, the level of $V_{OH}$ is not guaranteed. Moreover, if $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high-level from this condition then the state of Q and $\overline{Q}$ cannot be predicted.

## ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |



MITSUBISHI ELECTRIC

## DUAL J-$\overline{K}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP WITH SET AND RESET

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V, $I_{OH}$=−0.4mA | $T_a$=0~70℃ | 2.7 | 3.4 | | V |
| | | | | $T_a$=−20~+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | J, $\overline{K}$, T | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | $\overline{S_D}$, $\overline{R_D}$ | | | | | 0.2 | |
| $I_{IH}$ | High-level input current | J, $\overline{K}$, T | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | $\overline{S_D}$, $\overline{R_D}$ | | | | | 40 | |
| $I_{IL}$ | Low-level input current | J, $\overline{K}$, T | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| | | $\overline{S_D}$, $\overline{R_D}$ | | | | | −0.4 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −10 | | −60 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$=5.5V (Note 2) | | | 2.4 | 4 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

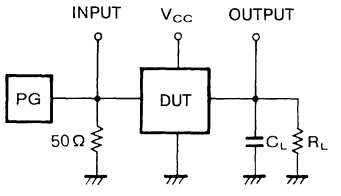
Note 2 : The supply current is measured alternately at J = $\overline{K}$ = $\overline{S_D}$ = T = 0V, $\overline{R_D}$ = 4.5V ($\overline{Q}$ = high-level) and J = $\overline{K}$ = $\overline{R_D}$ = T = 0V, $\overline{S_D}$ = 4.5V ($\overline{Q}$ = high-level).

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 3), $C_L$=15pF, $R_L$=500Ω | | | $V_{CC}$=4.5~5.5V (Note 3), $C_L$=50pF, $R_L$=500Ω | | | | | | |
| | | | | $T_a$=25℃ | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Outputs | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $f_{max}$ | Maximum clock frequency | T | Q, $\overline{Q}$ | | 50 | | 34 | 43 | | 30 | 43 | | MHz |
| $t_{PLH}$ | Propagation time | $\overline{S_D}$, $\overline{R_D}$ | Q, $\overline{Q}$ | | 6 | | 3 | 7 | 13 | 3 | 7 | 14 | ns |
| $t_{PHL}$ | | | | | 7 | | 5 | 10 | 15 | 5 | 10 | 16 | |
| $t_{PLH}$ | | T | Q, $\overline{Q}$ | | 7 | | 5 | 8 | 16 | 5 | 8 | 17 | ns |
| $t_{PHL}$ | | | | | 8 | | 7 | 11 | 18 | 7 | 11 | 19 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 3 : Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

## DUAL J-$\overline{K}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP WITH SET AND RESET

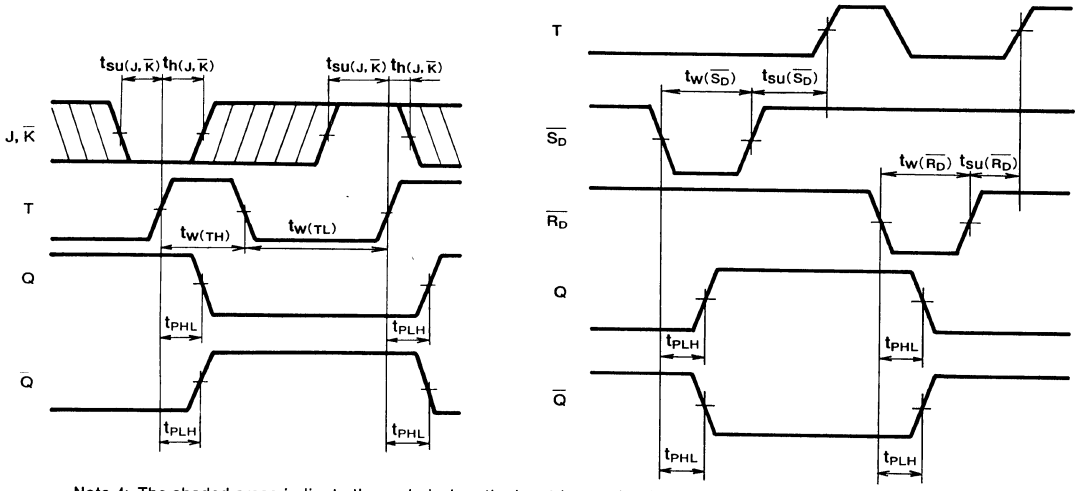
### TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_L$=500Ω)

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{w(TH)}$ | Pulse width | T "H" | 12 | 3 | | 14 | 3 | | ns |
| $t_{w(TL)}$ | | T "L" | 17 | 13 | | 19 | 13 | | |
| $t_{w(\overline{S_D})}$ | | $\overline{S_D}$ "L" | 15 | 6 | | 16 | 6 | | |
| $t_{w(\overline{R_D})}$ | | $\overline{R_D}$ "L" | 15 | 3 | | 16 | 3 | | |
| $t_{su(J,\overline{K})}$ | Setup time before T↑ | J, $\overline{K}$ | 15 | 6 | | 16 | 6 | | ns |
| $t_{su(\overline{S_D})}$ | | $\overline{S_D}$ "H" (inactive) | 10 | 3 | | 11 | 3 | | |
| $t_{su(\overline{R_D})}$ | | $\overline{R_D}$ "H" (inactive) | 15 | 8 | | 16 | 8 | | |
| $t_{h(J,\overline{K})}$ | Hold time after T↑ | J, $\overline{K}$ | 5 | 0 | | 6 | 0 | | ns |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

↑: Transition from low to high (positive edge trigger)

### TIMING DIAGRAM (Reference level = 1.3V)




Note 4: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS112AP

## DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOP WITH SET AND RESET

## DESCRIPTION

The M74ALS112AP is a semiconductor integrated circuit consisting of two J-K negative edge-triggered flip-flop circuits. Each of the circuits has independent inputs J, K, clock $\overline{T}$, direct set $\overline{S_D}$ and direct reset $\overline{R_D}$.

## FEATURES

- Negative edge-triggering
- Independent inputs and outputs for each flip-flop
- Direct set and reset inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range ($Ta = -20 \sim +75°C$)

## APPLICATIONS

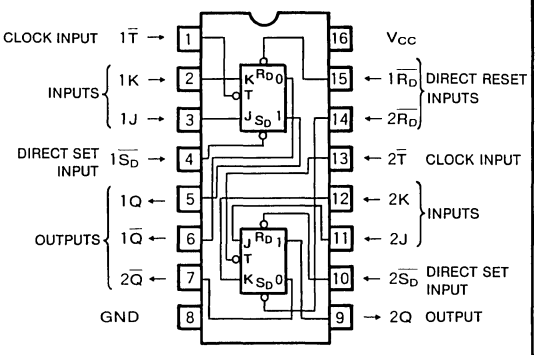
General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

When $\overline{T}$ changes from high-level to low-level, the signals applied just before the change on J and K appear at Q and $\overline{Q}$ outputs in accordance with the function table. Use of $\overline{S_D}$ and $\overline{R_D}$ allows direct R-S flip-flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low-level, Q and $\overline{Q}$ are high-level. But if $\overline{S_D}$ and $\overline{R_D}$ become high simultaneously from this condition, the state of Q and $\overline{Q}$ cannot be predicted. When used as a J-K flip-flop, $\overline{S_D}$ and $\overline{R_D}$ should be held at high-level.

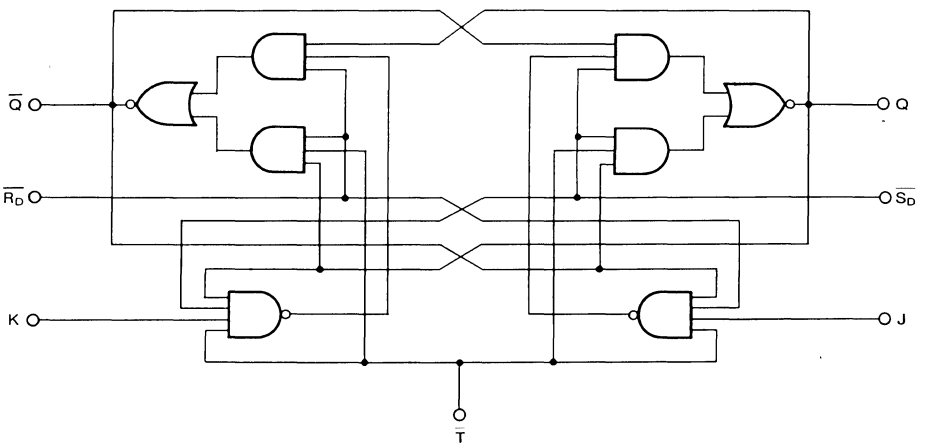
The M74ALS113AP, a 14-pin device without $\overline{R_D}$ inputs, is available. The M74ALS114AP featuring $\overline{T}$ and $\overline{R_D}$ inputs common to both circuits is also available.

## PIN CONFIGURATION (TOP VIEW)




Outline 16P4

## LOGIC DIAGRAM (EACH FLIP-FLOP)



# DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOP WITH SET AND RESET

## FUNCTION TABLE (Note 1)

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| $\overline{T}$ | $\overline{S_D}$ | $\overline{R_D}$ | J | K | Q | $\overline{Q}$ |
| X | L | H | X | X | H | L |
| X | H | L | X | X | L | H |
| X | L | L | X | X | H* | H* |
| ↓ | H | H | H | H | Toggle | |
| ↓ | H | H | L | H | L | H |
| ↓ | H | H | H | L | H | L |
| ↓ | H | H | L | L | $Q^0$ | $\overline{Q^0}$ |
| H | H | H | X | X | $Q^0$ | $\overline{Q^0}$ |

Note 1: ↓ : Transition from high to low level (negative edge trigger)

X : Irrelevant

$Q^0$ : Level of Q before the indicated steady-state input conditions were established.

$\overline{Q^0}$ : Level of $\overline{Q}$ before the indicated steady-state input conditions were established.

Toggle Complement of previous state appears on each output with ↓ transition.

* : When $\overline{S_D}$ or $\overline{R_D}$ is near $V_{IL\,MAX}$ in this condition, the level of $V_{OH}$ is not guaranteed. Moreover, if $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high-level from this condition then the state of Q and $\overline{Q}$ cannot be predicted.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | High-level state | −0.5 ~ $V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 ~ +75 | °C |
| $T_{stg}$ | Storage temperature range | | −65 ~ +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $T_a$=0~70°C | 2.7 | 3.4 | | V |
| | | | $I_{OH}$=−0.4mA | $T_a$=−20~+75°C | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | J, K, $\overline{T}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | $\overline{S_D}$, $\overline{R_D}$ | | | | | 0.2 | |
| $I_{IH}$ | High-level input current | J, K, $\overline{T}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | $\overline{S_D}$, $\overline{R_D}$ | | | | | 40 | |
| $I_{IL}$ | Low-level input current | J, K, $\overline{T}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| | | $\overline{S_D}$, $\overline{R_D}$ | | | | | −0.4 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$=5.5V (Note 2) | | | 2.5 | 4.5 | mA |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 2 The supply current is measured alternately at J = K = $\overline{T}$ = $\overline{S_D}$ = 0V, $\overline{R_D}$ = 4.5V ($\overline{Q}$ = high-level) and J = K = $\overline{T}$ = $\overline{R_D}$ = 0V, $\overline{S_D}$ = 4.5V ($\overline{Q}$ = high-level)

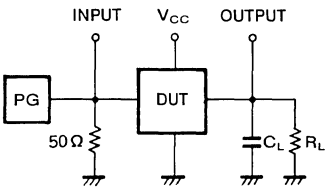
## DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOP WITH SET AND RESET

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=5V (Note 3), $C_L$=15pF, $R_L$=500Ω; $T_a$=25°C Min | Typ | Max | $V_{CC}$=4.5~5.5V (Note 3), $C_L$=50pF, $R_L$=500Ω; $T_a$=0~70°C Min | Typ* | Max | $T_a$=−20~+75°C Min | Typ* | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | $\overline{T}$ | Q, $\overline{Q}$ | 35 | 42 | | 28 | 40 | | 26 | 40 | | MHz |
| $t_{PLH}$ | Propagation time | $\overline{S_D}$, $\overline{R_D}$ | Q, $\overline{Q}$ | | 10 | | 4 | 11 | 18 | 4 | 11 | 19 | ns |
| $t_{PHL}$ | | | | | 11 | | 4 | 12 | 18 | 4 | 12 | 19 | |
| $t_{PLH}$ | | $\overline{T}$ | Q, $\overline{Q}$ | | 9 | | 3 | 10 | 15 | 3 | 10 | 16 | ns |
| $t_{PHL}$ | | | | | 12 | | 5 | 13 | 19 | 5 | 13 | 20 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 3 : Measurement circuit




(1) The pulse generator (PG) has the following characteristics.
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

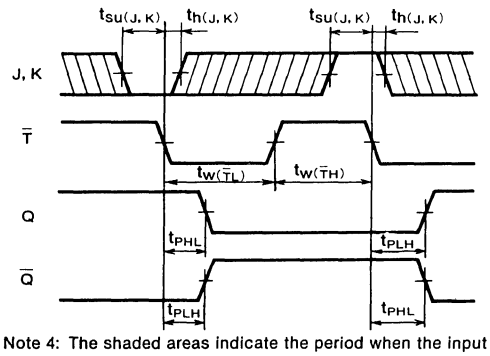
### TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_L$=500Ω)

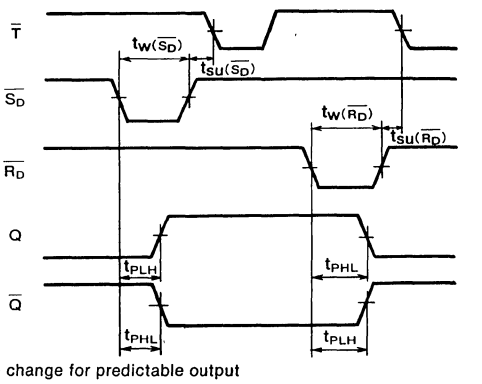
| Symbol | Parameter | | Limits: $T_a$=0~70°C Min | Typ* | Max | $T_a$=−20~+75°C Min | Typ* | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{W(\overline{T}H)}$ | Pulse width | $\overline{T}$ "H" | 16.5 | 5 | | 17.5 | 5 | | ns |
| $t_{W(\overline{T}L)}$ | | $\overline{T}$ "L" | 19 | 11 | | 20 | 11 | | |
| $t_{W(\overline{S_D})}$ | | $\overline{S_D}$ "L" | 14 | 9 | | 15 | 9 | | |
| $t_{W(\overline{R_D})}$ | | $\overline{R_D}$ "L" | 14 | 9 | | 15 | 9 | | |
| $t_{su(J,K)}$ | Setup time before T↓ | J, K | 22 | 11 | | 23 | 11 | | ns |
| $t_{su(\overline{S_D})}$ | | $\overline{S_D}$ "H" (inactive) | 20 | 12 | | 21 | 12 | | |
| $t_{su(\overline{R_D})}$ | | $\overline{R_D}$ "H" (inactive) | 20 | 14 | | 21 | 14 | | |
| $t_{h(J,K)}$ | Hold time after T↓ | J, K | 0 | −6 | | 1 | −6 | | ns |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

↓ : Transition from high to low. (negative edge trigger)

### TIMING DIAGRAM (Reference level = 1.3V)




Note 4: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS113AP

## DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOP WITH SET

### DESCRIPTION

The M74ALS113AP is a semiconductor integrated circuit consisting of two J-K negative edge-triggered flip-flop circuits. Each of the circuits has independent inputs J, K, clock T and direct set $\overline{S_D}$.

### FEATURES

- Negative edge-triggering
- Independent inputs for each flip-flop
- Direct set inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

### APPLICATIONS

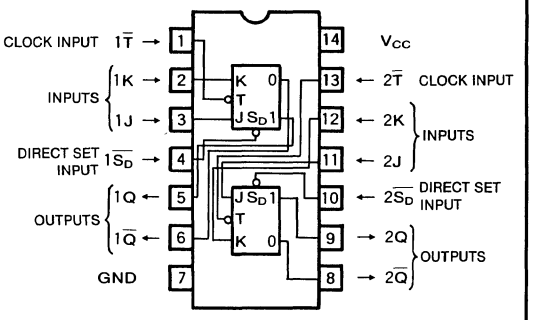
General purpose, for use in industrial and consumer digital equipment.

### FUNCTIONAL DESCRIPTION

When $\overline{T}$ changes from high-level to low-level, the signals applied just before the change on J and K appear at Q and $\overline{Q}$ outputs in accordance with the function table. When $\overline{S_D}$ is low, Q becomes high and $\overline{Q}$ becomes low irrespective of other inputs. When used as a J-K flip-flop, $\overline{S_D}$ should be held at high-level.

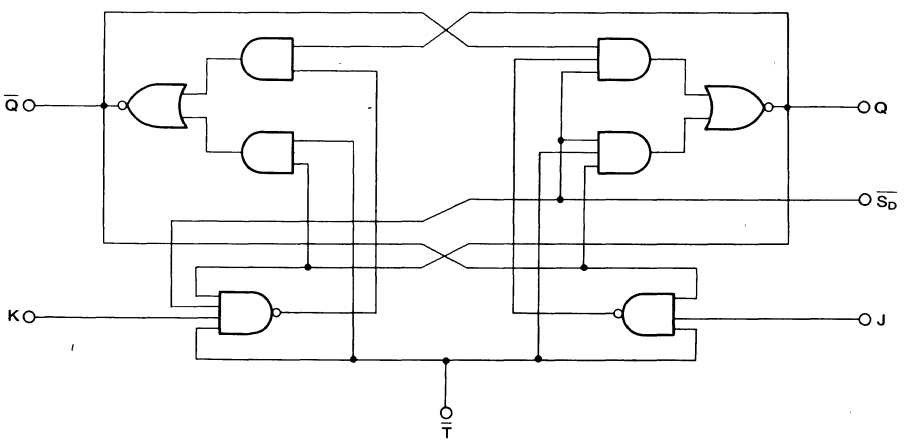
The M74ALS112AP featuring direct reset inputs $\overline{R_D}$ is also available.

### PIN CONFIGURATION (TOP VIEW)




Outline 14P4

### LOGIC DIAGRAM (EACH FLIP-FLOP)






MITSUBISHI ELECTRIC

## DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOP WITH SET

### FUNCTION TABLE (Note 1)

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| $\overline{T}$ | $\overline{S_D}$ | J | K | Q | $\overline{Q}$ |
| X | L | X | X | H | L |
| ↓ | H | H | H | Toggle | |
| ↓ | H | L | H | L | H |
| ↓ | H | H | L | H | L |
| ↓ | H | L | L | $Q^0$ | $\overline{Q^0}$ |
| H | H | X | X | $Q^0$ | $\overline{Q^0}$ |

Note 1: ↓ : Transition from high to low level (negative edge trigger)
X : Irrelevant
$Q^0$ : Level of Q before the indicated steady-state input conditions were established.
$\overline{Q^0}$ : Level of $\overline{Q}$ before the indicated steady-state input conditions were established.
Toggle Complement of previous state appears on each output with ↓ transition.

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $T_a$=0~70℃ | 2.7 | 3.4 | | V |
| | | | $I_{OH}$=−0.4mA | $T_a$=−20~+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | J, K, $\overline{T}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | $\overline{S_D}$ | | | | | 0.2 | |
| $I_{IH}$ | High-level input current | J, K, $\overline{T}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | $\overline{S_D}$ | | | | | 40 | |
| $I_{IL}$ | Low-level input current | J, K, $\overline{T}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| | | $\overline{S_D}$ | | | | | −0.4 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$=5.5V (Note 2) | | | 2.5 | 4.5 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 2 : The supply current is measured alternately at J = K = $\overline{T}$ = $\overline{S_D}$ = 0V (Q = high-level) and J = K = $\overline{T}$ = 0V, $\overline{S_D}$ = 4.5V ($\overline{Q}$ = high-level).

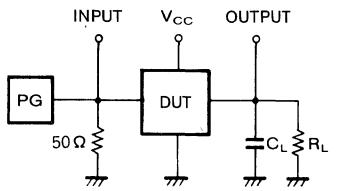
## DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOP WITH SET

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Outputs | Test conditions/Limits: $V_{CC}$=5V (Note 3), $C_L$=15pF, $R_L$=500Ω, $T_a$=25°C Min | Typ | Max | $V_{CC}$=4.5~5.5V (Note 3), $C_L$=50pF, $R_L$=500Ω, $T_a$=0~70°C Min | Typ* | Max | $T_a$=−20~+75°C Min | Typ* | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | $\overline{T}$ | Q, $\overline{Q}$ | 35 | 42 | | 28 | 40 | | 26 | 40 | | MHz |
| $t_{PLH}$ | Propagation time | $\overline{S_D}$ | Q | | 10 | | 4 | 11 | 18 | 4 | 11 | 19 | ns |
| $t_{PHL}$ | | | $\overline{Q}$ | | 11 | | 4 | 12 | 18 | 4 | 12 | 19 | |
| $t_{PLH}$ | | $\overline{T}$ | Q, $\overline{Q}$ | | 9 | | 3 | 10 | 15 | 3 | 10 | 16 | ns |
| $t_{PHL}$ | | | | | 12 | | 5 | 13 | 19 | 5 | 13 | 20 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C

Note 3: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

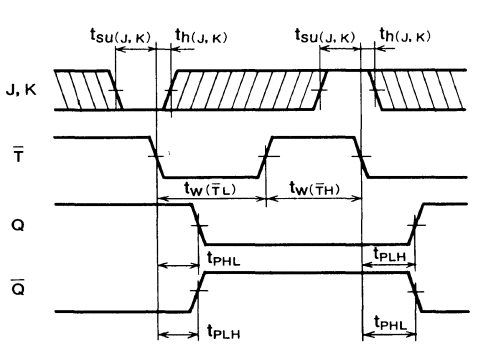
## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_L$=500Ω)

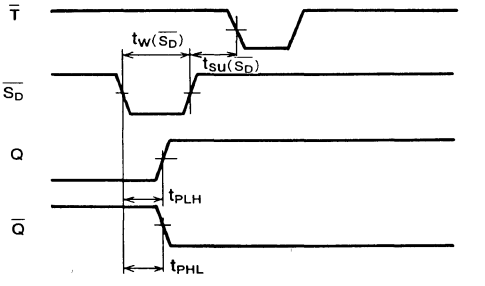
| Symbol | Parameter | | Limits: $T_a$=0~70°C Min | Typ* | Max | $T_a$=−20~+75°C Min | Typ* | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{w(\overline{T}H)}$ | Pulse width | $\overline{T}$ "H" | 16.5 | 5 | | 17.5 | 5 | | ns |
| $t_{w(\overline{T}L)}$ | | $\overline{T}$ "L" | 19 | 11 | | 20 | 11 | | |
| $t_{w(\overline{S_D})}$ | | $\overline{S_D}$ "L" | 14 | 9 | | 15 | 9 | | |
| $t_{su(J,K)}$ | Setup time before T↓ | J, K | 22 | 11 | | 23 | 11 | | ns |
| $t_{su(\overline{S_D})}$ | | $\overline{S_D}$ "H" (inactive) | 20 | 12 | | 21 | 12 | | |
| $t_{h(J,K)}$ | Hold time after T↓ | J, K | 0 | −6 | | 1 | −6 | | ns |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↓: Transition from high to low. (negative edge trigger)

## TIMING DIAGRAM (Reference level = 1.3V)




Note 4: The shaded areas indicate the period when the input is permitted to change for predictable output performance.



MITSUBISHI ELECTRIC

# M74ALS114AP

## DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOP WITH SET, COMMON RESET, AND COMMON CLOCK

## DESCRIPTION

The M74ALS114AP is a semiconductor integrated circuit consisting of two J-K type negative edge-triggered flip-flop circuits, with a clock input $\overline{T}$ and a direct reset input $\overline{R_D}$ common to both circuits, inputs J, K, and a direct set input $\overline{S_D}$ for each circuit.

## FEATURES

- Negative edge-triggering
- Common clock and direct reset inputs
- Independent direct set input
- Q and $\overline{Q}$ outputs
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

## APPLICATIONS

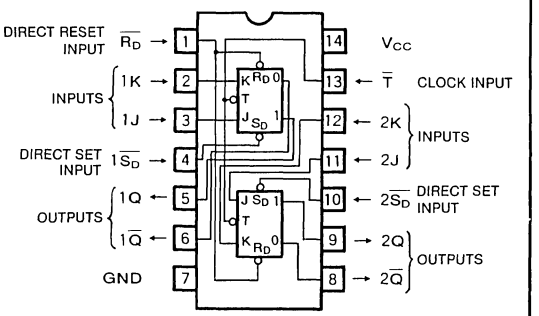
General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

When $\overline{T}$ changes from high-level to low-level, the signals applied just before the change on J and K appear at Q and $\overline{Q}$ outputs in accordance with the function table. Use of $\overline{S_D}$ and $\overline{R_D}$ allows direct R-S flip-flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low-level, Q and $\overline{Q}$ are high-level. But if $\overline{S_D}$ and $\overline{R_D}$ become high simultaneously from this condition, the state of Q and $\overline{Q}$ cannot be predicted. When used as a J-K type flip-flop, $\overline{S_D}$ and $\overline{R_D}$ should be held at high-level.

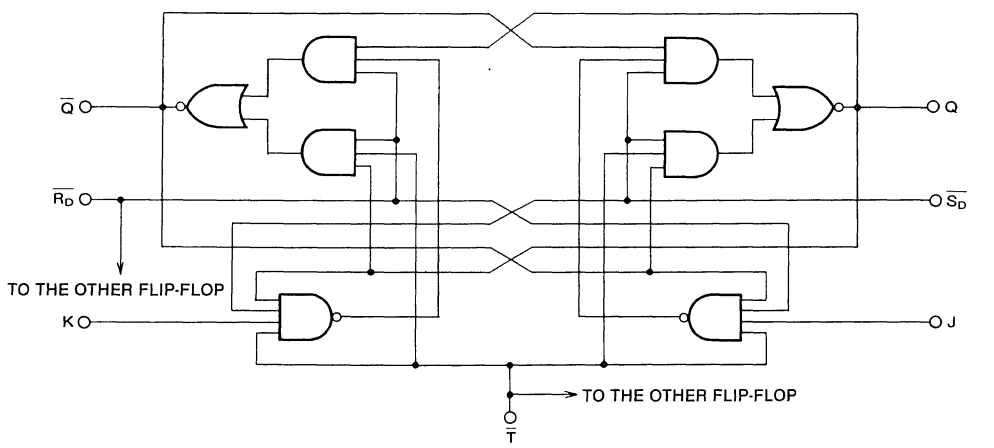
The M74ALS112AP featuring independent $\overline{T}$ and $\overline{R_D}$ inputs is also available.

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## LOGIC DIAGRAM (EACH FLIP-FLOP)



# M74ALS114AP

## DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOP WITH SET, COMMON RESET, AND COMMON CLOCK

## FUNCTION TABLE (Note 1)

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| $\overline{T}$ | $\overline{S_D}$ | $\overline{R_D}$ | J | K | Q | $\overline{Q}$ |
| X | L | H | X | X | H | L |
| X | H | L | X | X | L | H |
| X | L | L | X | X | H* | H* |
| ↓ | H | H | H | H | Toggle | |
| ↓ | H | H | L | H | L | H |
| ↓ | H | H | H | L | H | L |
| ↓ | H | H | L | L | $Q^0$ | $\overline{Q^0}$ |
| H | H | H | X | X | $Q^0$ | $\overline{Q^0}$ |

Note 1 : ↓ : Transition from high to low (negative edge trigger)

X : Irrelevant

$Q^0$ : Level of Q before the indicated steady-state input conditions were established.

$\overline{Q^0}$ : Level of $\overline{Q}$ before the indicated steady-state input conditions were established.

Toggle : Complementg of previous state appears on each output with ↓ transition.

* : When $\overline{S_D}$ or $\overline{R_D}$ is near $V_{ILMAX}$ in this condition, the level of $V_{OH}$ is not guaranteed. Moreover, if $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high-level from this condition then the state of Q and $\overline{Q}$ cannot be predicted.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| Topr | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| Tstg | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| Topr | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $T_a$=0~70℃ | 2.7 | 3.4 | | V |
| | | | $I_{OH}$=−0.4mA | $T_a$=−20~+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | J, K, $\overline{T}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | $\overline{S_D}$, $\overline{R_D}$ | | | | | 0.2 | |
| $I_{IH}$ | High-level input current | J, K, $\overline{T}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | $\overline{S_D}$, $\overline{R_D}$ | | | | | 40 | |
| $I_{IL}$ | Low-level input current | J, K | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| | | $\overline{S_D}$, $\overline{T}$ | | | | | −0.4 | |
| | | $\overline{R_D}$ | | | | | −0.6 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$=5.5V (Note 2) | | | 2.5 | 4.5 | mA |

* : All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: The supply current is measured alternately at J=K=$\overline{T}$=$\overline{S_D}$=OV, $\overline{R_D}$=4.5V (Q=high-level) and J=K=$\overline{T}$=$\overline{R_D}$=OV, $\overline{S_D}$=4.5V ($\overline{Q}$=high-level).

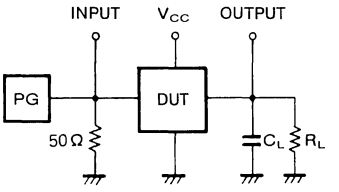
## DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOP WITH SET, COMMON RESET, AND COMMON CLOCK

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=5V (Note 3), $C_L$=15pF, $R_L$=500Ω, $T_a$=25°C Min | Typ | Max | $V_{CC}$=4.5~5.5V (Note 3), $C_L$=50pF, $R_L$=500Ω, $T_a$=0~70°C Min | Typ* | Max | $T_a$=−20~+75°C Min | Typ* | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | $\overline{T}$ | Q, $\overline{Q}$ | 35 | 42 | | 28 | 40 | | 26 | 40 | | MHz |
| $t_{PLH}$ | Propagation time | $\overline{S_D}$, $\overline{R_D}$ | Q, $\overline{Q}$ | | 10 | | 4 | 11 | 18 | 4 | 11 | 19 | ns |
| $t_{PHL}$ | | | | | 11 | | 4 | 12 | 18 | 4 | 12 | 19 | |
| $t_{PLH}$ | | $\overline{T}$ | Q, $\overline{Q}$ | | 9 | | 3 | 10 | 15 | 3 | 10 | 16 | ns |
| $t_{PHL}$ | | | | | 12 | | 5 | 13 | 19 | 5 | 13 | 20 | |

* : All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 3: Measurement circuit




(1) The pulse generator (PG) has the following characteristics
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

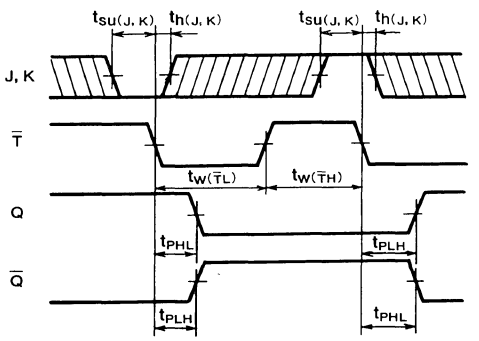
(2) $C_L$ includes probe and jig capacitance

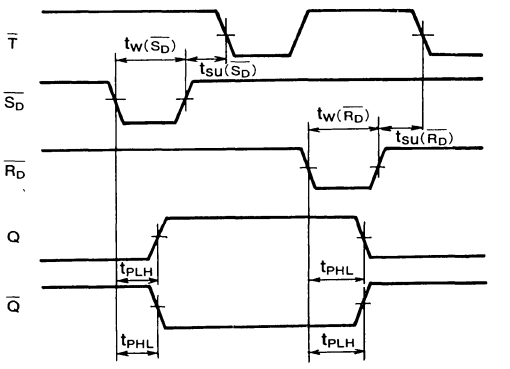
## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_L$=500Ω)

| Symbol | Parameter | | Limits: $T_a$=0~70°C Min | Typ* | Max | $T_a$=−20~+75°C Min | Typ* | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{w(\overline{TH})}$ | Pulse width | $\overline{T}$ "H" | 16.5 | 5 | | 17.5 | 5 | | ns |
| $t_{w(\overline{TL})}$ | | $\overline{T}$ "L" | 19 | 11 | | 20 | 11 | | |
| $t_{w(\overline{SD})}$ | | $\overline{S_D}$ "L" | 14 | 9 | | 15 | 9 | | |
| $t_{w(\overline{RD})}$ | | $\overline{R_D}$ "L" | 14 | 9 | | 15 | 9 | | |
| $t_{su(J,K)}$ | Setup time before $\overline{T}$↓ | J, K | 22 | 11 | | 23 | 11 | | ns |
| $t_{su(\overline{SD})}$ | | $\overline{S_D}$ "H" (inactive) | 20 | 12 | | 21 | 12 | | |
| $t_{su(\overline{RD})}$ | | $\overline{R_D}$ "H" (inactive) | 20 | 12 | | 21 | 12 | | |
| $t_{h(J,K)}$ | Hold time after $\overline{T}$↓ | J, K | 0 | −6 | | 1 | −6 | | ns |

* : All typical values are at $V_{CC}$=5V, $T_a$=25°C.
↓ : Transition from high to low (negative edge trigger)

## TIMING DIAGRAM (Reference level = 1.3V)




Note 4: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS131P

## 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS REGISTER

## DESCRIPTION

The M74ALS131P is a semiconductor integrated circuit of a 3-line-to-8-line decoder/demultiplexer with address register.

## FEATURES

- Address data storing capability with clock input
- Easy cascade connection with two enable inputs
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

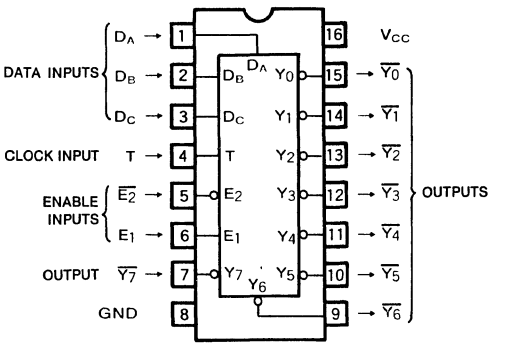
This decoder/demultiplexer has a positive-edge triggered register for storing address data.

Using as a decoder, give the address in 3-bit binary code on inputs $D_A \sim D_C$, apply a positive edge trigger on clock input T, and the address is stored irrespective of the state of enable inputs $E_1$ and $\overline{E_2}$. If $E_1$ is set high and $\overline{E_2}$ is set low, then the one output among outputs $\overline{Y_0} \sim \overline{Y_7}$ corresponding to the register data is low and the remaining seven outputs are high. When $E_1$ and $\overline{E_2}$ are in any other condition, all the outputs are high.

When the device is used as a demultiplexer, it functions as a 1-line-to-8-line demultiplexer by making $E_1$ and $\overline{E_2}$ the data inputs and $D_a \sim D_c$ the selection inputs.

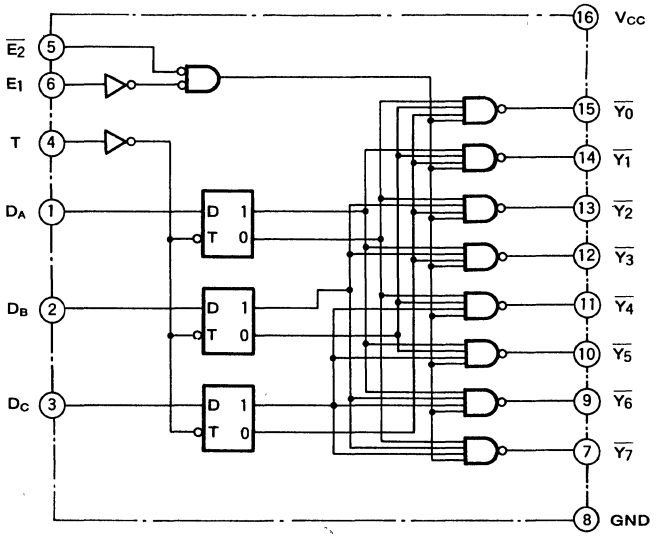
This device is the same as the M74ALS138P except that it features registers in inputs $D_a \sim D_c$.

## PIN CONFIGURATION (TOP VIEW)




Outline 16P4

## LOGIC DIAGRAM






MITSUBISHI ELECTRIC

# 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS REGISTER

## FUNCTION TABLE (Note 1)

| Inputs | | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| T | $E_1$* | $\overline{E_2}$* | $D_C$ | $D_B$ | $D_A$ | $\overline{Y_0}$ | $\overline{Y_1}$ | $\overline{Y_2}$ | $\overline{Y_3}$ | $\overline{Y_4}$ | $\overline{Y_5}$ | $\overline{Y_6}$ | $\overline{Y_7}$ |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| X | L | X | X | X | X | H | H | H | H | H | H | H | H |
| ↑ | H | L | L | L | L | L | H | H | H | H | H | H | H |
| ↑ | H | L | L | L | H | H | L | H | H | H | H | H | H |
| ↑ | H | L | L | H | L | H | H | L | H | H | H | H | H |
| ↑ | H | L | L | H | H | H | H | H | L | H | H | H | H |
| ↑ | H | L | H | L | L | H | H | H | H | L | H | H | H |
| ↑ | H | L | H | L | H | H | H | H | H | H | L | H | H |
| ↑ | H | L | H | H | L | H | H | H | H | H | H | L | H |
| ↑ | H | L | H | H | H | H | H | H | H | H | H | H | L |
| L or H | H | L | X | X | X | Output corresponding to stored address, L; all others, H. | | | | | | | |

Note 1: X : Irrelevant

↑ : Transition from low to high (positive edge trigger)

* : Address data can be internally stored with $D_A \sim D_C$ and T irrespective of the state of $E_1$ and $\overline{E_2}$.

## ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5～+7 | V |
| $V_I$ | Input voltage | | −0.5～+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5～$V_{CC}$ | V |
| Topr | Operating free-air ambient temperature range | | −20～+75 | ℃ |
| Tstg | Storage temperature range | | −65～+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| Topr | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−0.4mA | $T_a$=0～70℃ | 2.7 | 3.4 | | V |
| | | | $T_a$=−20～+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$=5.5V | | | 5 | 11 | mA |

* : All typical values are at $V_{CC}$=5V, $T_a$=25°C.

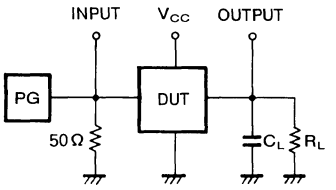
## 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS REGISTER

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=5V (Note 1), $C_L$=15pF, $R_L$=500Ω, $T_a$=25℃ | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 1), $C_L$=50pF, $R_L$=500Ω, $T_a$=0~70℃ | | | Test conditions/Limits: $T_a$=−20~+75℃ | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Input | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $f_{max}$ | Maximum clock frequency | T | $\overline{Y}$ | 54 | 58 | | 48 | 54 | | 45 | 54 | | MHz |
| $t_{PLH}$ | Propagation time | T | $\overline{Y}$ | | 14 | | 8 | 15 | 25 | 8 | 15 | 26 | ns |
| $t_{PHL}$ | | | | | 10 | | 7 | 12 | 20 | 7 | 12 | 21 | |
| $t_{PLH}$ | | $E_1$ | $\overline{Y}$ | | 10 | | 7 | 11 | 20 | 7 | 11 | 21 | ns |
| $t_{PHL}$ | | | | | 9 | | 6 | 11 | 17 | 6 | 11 | 18 | |
| $t_{PLH}$ | | $\overline{E_2}$ | $\overline{Y}$ | | 7 | | 5 | 9 | 15 | 5 | 9 | 16 | ns |
| $t_{PHL}$ | | | | | 7 | | 5 | 9 | 15 | 5 | 9 | 16 | |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




(1) The pulse generator (PG) has the following chracteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

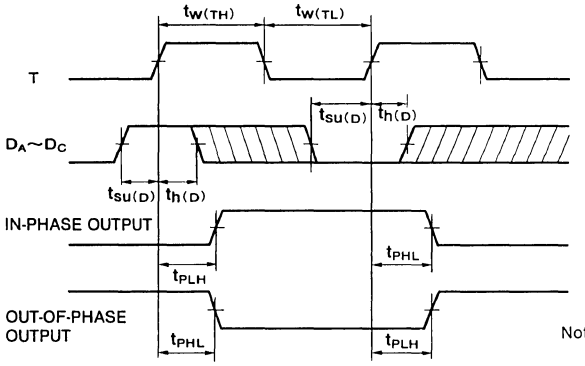
### TIMING REQUIREMENTS ($V_{CC}$=4.5~5.5V, $C_L$=50pF, $R_L$=500Ω)

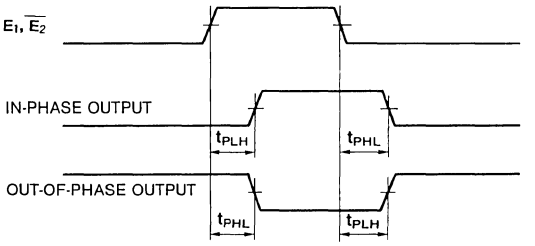
| Symbol | Parameter | | Limits: $T_a$=0~70℃ Min | Typ* | Max | Limits: $T_a$=−20~+75℃ Min | Typ* | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{W(TH)}$ | Pulse width | T "H" | 10 | 4 | | 11 | 4 | | ns |
| $t_{W(TL)}$ | | T "L" | 10 | 5 | | 11 | 5 | | |
| $t_{su(D)}$ | Setup time in relation to T↑ | $D_A$~$D_C$ | 14 | 7 | | 15 | 7 | | ns |
| $t_{h(D)}$ | Hold time in relation to T↑ | $D_A$~$D_C$ | 0 | −2 | | 1 | −2 | | ns |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.
↑: Transition from low to high (positive edge trigger)

## 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS REGISTER

### TIMING DIAGRAM (Reference level = 1.3V)




Note 2: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS137P

## 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

### DESCRIPTION

The M74ALS137P is a semiconductor integrated circuit of a 3-line-to-8-line decoder/demultiplexer with address latch.

### FEATURES

- Address latch capability with latch enable input
- Easy cascade connection with two enable inputs
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

### APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

### FUNCTIONAL DESCRIPTION

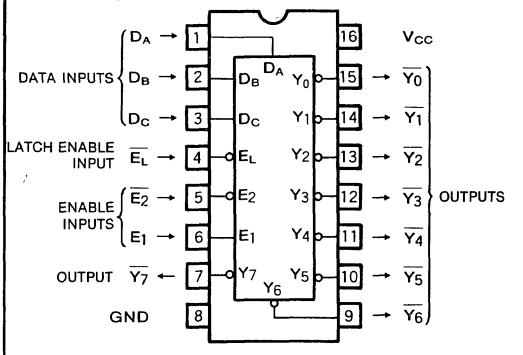
When latch enable input $\overline{E_L}$ is low, the data applied to inputs $D_A \sim D_C$ are read into the latch; when it is high, the latch retains the data.

Using as a decoder, give the address in 3-bit binary code on inputs $D_A \sim D_C$, and one output among outputs $\overline{Y_0} \sim \overline{Y_7}$ corresponding to the address is low and the other seven outputs are all high. In this case, enable input $E_1$ is set high and enable input $\overline{E_2}$ is set low. When $E_1$ and $\overline{E_2}$ are in any other condition, the outputs are high irrespective of the status of $D_A \sim D_C$.

When the device is used as a demultiplexer, it functions as a 1-line-to-8-line demultiplexer by making $E_1$ and $\overline{E_2}$ the data inputs and $D_a \sim D_C$ the selection inputs.

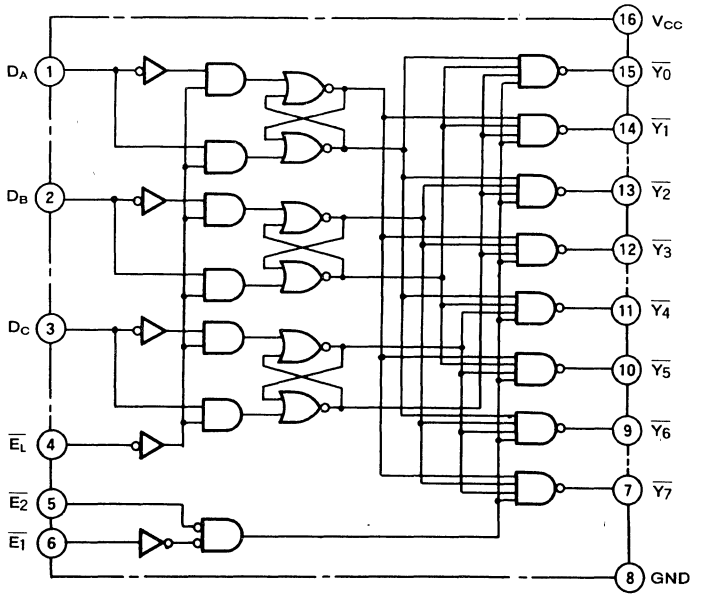
This deviced is the same as the M74ALS138P except that it features a latch function in inputs $D_a \sim D_C$.

### PIN CONFIGURATION (TOP VIEW)




Outline 16P4

### LOGIC DIAGRAM






MITSUBISHI ELECTRIC

## 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

### FUNCTION TABLE (Note 1)

| Inputs | | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{E_L}$ | $E_1$* | $\overline{E_2}$* | $D_C$ | $D_B$ | $D_A$ | $\overline{Y_0}$ | $\overline{Y_1}$ | $\overline{Y_2}$ | $\overline{Y_3}$ | $\overline{Y_4}$ | $\overline{Y_5}$ | $\overline{Y_6}$ | $\overline{Y_7}$ |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| X | L | X | X | X | X | H | H | H | H | H | H | H | H |
| L | H | L | L | L | L | L | H | H | H | H | H | H | H |
| L | H | L | L | L | H | H | L | H | H | H | H | H | H |
| L | H | L | L | H | L | H | H | L | H | H | H | H | H |
| L | H | L | L | H | H | H | H | H | L | H | H | H | H |
| L | H | L | H | L | L | H | H | H | H | L | H | H | H |
| L | H | L | H | L | H | H | H | H | H | H | L | H | H |
| L | H | L | H | H | L | H | H | H | H | H | H | L | H |
| L | H | L | H | H | H | H | H | H | H | H | H | H | L |
| H | H | L | X | X | X | Output corresponding to latched address, L, all others, H. | | | | | | | |

Note 1: X : Irrelevant

* : Address data can be internally latched with $D_A \sim D_C$ and $\overline{E_L}$ irrespective of the state of $E_1$ and $\overline{E_2}$.

### ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5～+7 | V |
| $V_I$ | Input voltage | | −0.5～+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5～$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20～+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65～+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $T_a$=0～70℃ | 2.7 | 3.4 | | V |
| | | $I_{OH}$=−0.4mA | $T_a$=−20～+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$=5.5V | | | 5 | 11 | mA |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

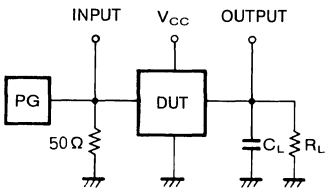
## 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Output | Test conditions/Limits: $V_{CC}$=5V (Note 2), $C_L$=15pF, $R_L$=500Ω, $T_a$=25℃ Min | Typ | Max | $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_L$=500Ω, $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | $D_A$, $D_B$ | $\overline{Y}$ | | 12 | | 5 | 13 | 20 | 5 | 13 | 21 | ns |
| $t_{PHL}$ | | $D_C$ | | | 10 | | 6 | 12 | 20 | 6 | 12 | 21 | |
| $t_{PLH}$ | | $\overline{E_2}$ | $\overline{Y}$ | | 7 | | 4 | 8 | 12 | 4 | 8 | 13 | ns |
| $t_{PHL}$ | | | | | 7 | | 5 | 9 | 15 | 5 | 9 | 16 | |
| $t_{PLH}$ | | $E_1$ | $\overline{Y}$ | | 10 | | 5 | 12 | 17 | 5 | 12 | 18 | ns |
| $t_{PHL}$ | | | | | 9 | | 5 | 11 | 15 | 5 | 11 | 16 | |
| $t_{PLH}$ | | $\overline{E_L}$ | $\overline{Y}$ | | 13 | | 7 | 14 | 22 | 7 | 14 | 23 | ns |
| $t_{PHL}$ | | | | | 13 | | 7 | 14 | 20 | 7 | 14 | 21 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

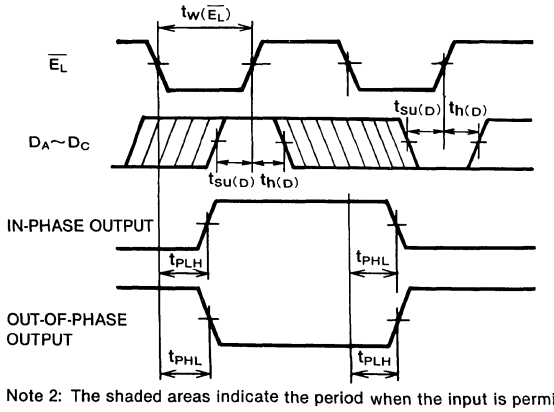
(2) $C_L$ includes probe and jig capacitance.

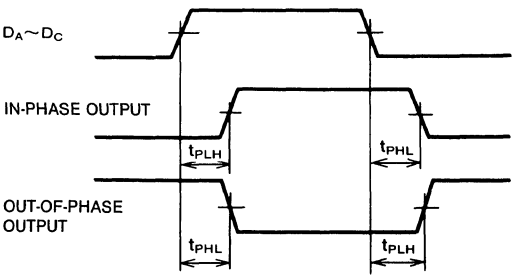
### TIMING REQUIREMENTS ($V_{CC}$=4.5~5.5V, $C_L$=50pF, $R_L$=500Ω)

| Symbol | Parameter | | Limits: $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{w(\overline{E_L})}$ | Pulse width | $\overline{E_L}$ "L" | 10 | 4 | | 11 | 4 | | ns |
| $t_{su(D)}$ | Setup time in relation to $\overline{E_L}$ ↑ | $D_A$~$D_C$ | 10 | 3 | | 11 | 3 | | ns |
| $t_{h(D)}$ | Hold time in relation to $\overline{E_L}$ ↑ | $D_A$~$D_C$ | 5 | −1 | | 6 | −1 | | ns |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.
↑: Transition from low to high (positive edge trigger)

### TIMING DIAGRAM (Reference level = 1.3V)




Note 2: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS138P

## 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

## DESCRIPTION

The M74ALS138P is a semiconductor integrated circuit of a 3-line-to-8-line decoder/demultiplexer with enable inputs.

## FEATURES

- Three types of enable inputs
- 4 to 16 decoder/demultiplexer capability without adding external components
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

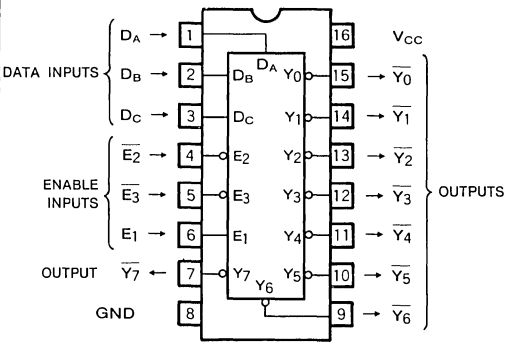
## FUNCTIONAL DESCRIPTION

Using as a decoder, give the address in 3-bit binary code on inputs $D_A \sim D_C$, and one output among outputs $\overline{Y_0} \sim \overline{Y_7}$ corresponding to the address is low and the other seven outputs are all high. In this case, enable input $E_1$ is set high and enable inputs $\overline{E_2}$ and $\overline{E_3}$ are set low. When $E_1$, $\overline{E_2}$ and $\overline{E_3}$ are in any other condition, the outputs are high irrespective of the status of $D_A \sim D_C$.

When the device is used as a demultiplexer, it functions as a 1-line-to-8-line demultiplexer by making $E_1$, $\overline{E_2}$ and $\overline{E_3}$ the data inputs and $D_a \sim D_C$ the selection inputs.

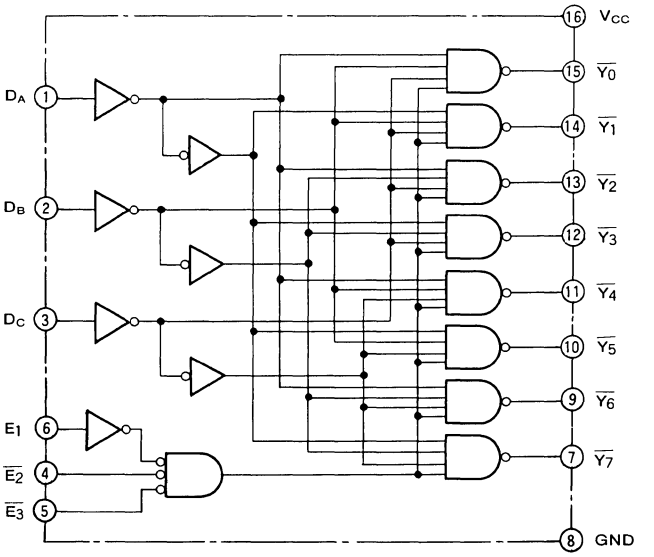
In addition to the features of this device the M74ALS137P and M74ALS131P offer an address latch function and an address register function respectively.

## PIN CONFIGURATION (TOP VIEW)




Outline 16P4

## LOGIC DIAGRAM



## 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

### FUNCTION TABLE (Note 1)

| Inputs | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $E_1$ | $\overline{E_X}$ | $D_C$ | $D_B$ | $D_A$ | $\overline{Y_0}$ | $\overline{Y_1}$ | $\overline{Y_2}$ | $\overline{Y_3}$ | $\overline{Y_4}$ | $\overline{Y_5}$ | $\overline{Y_6}$ | $\overline{Y_7}$ |
| X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

Note 1: $\overline{E_X}=\overline{E_2}+\overline{E_3}$

X : Irrelevant

### ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $T_a$=0~70℃ | 2.7 | 3.4 | | V |
| | | $I_{OH}$=−0.4mA | $T_a$=−20~+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$=5.5V | | | 5 | 10 | mA |

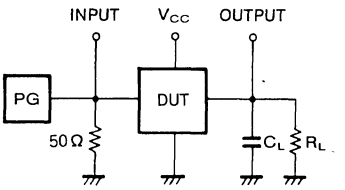
* : All typical values are at $V_{CC}$=5V, Ta=25°C.

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V (Note 2) $C_L$=15pF $R_L$=500Ω | | | $V_{CC}$=4.5~5.5V (Note 2) $C_L$=50pF $R_L$=500Ω | | | | | | |
| | | | | $T_a$=25°C | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ | Max | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{PLH}$ | Propagation time | $D_A$, $D_B$ | $\overline{Y}$ | | 13 | | 6 | 13 | 22 | 6 | 13 | 23 | ns |
| $t_{PHL}$ | | $D_C$ | | | 9 | | 6 | 11 | 18 | 6 | 11 | 19 | |
| $t_{PLH}$ | | $E_1$, $\overline{E_2}$ | $\overline{Y}$ | | 10 | | 4 | 11 | 17 | 4 | 11 | 18 | ns |
| $t_{PHL}$ | | $\overline{E_3}$ | | | 10 | | 5 | 12 | 17 | 5 | 12 | 18 | |

* All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

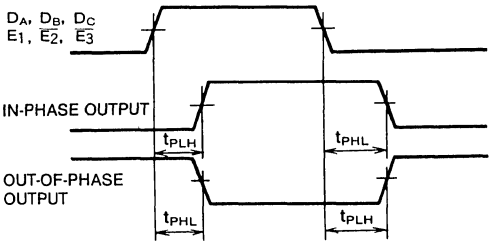
$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

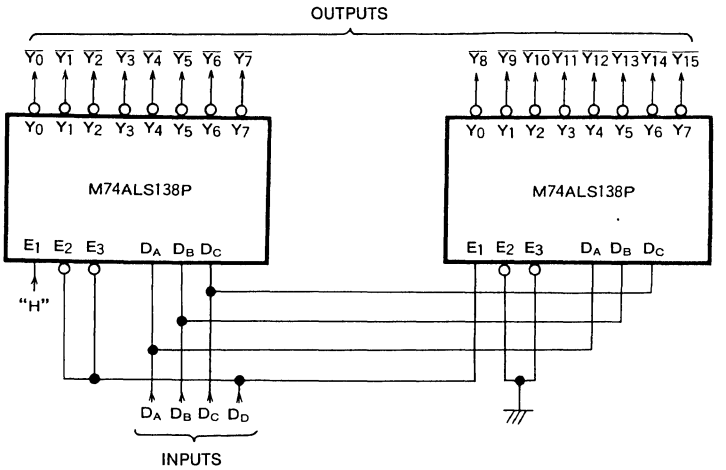
(2) $C_L$ includes probe and jig capacitance.

## TIMING DIAGRAM (Reference level = 1.3V)




## APPLICATION EXAMPLES

4-line to 16-line decoder/demultiplexer



# M74ALS160AP

## SYNCHRONOUS PRESETTABLE DECADE COUNTER WITH DIRECT RESET

## DESCRIPTION

The M74ALS160AP is a semiconductor integrated circuit of a synchronous presettable decade counter with a direct reset input.

## FEATURES

- Direct reset and synchronous load inputs
- Enable inputs and carry output for cascade connection
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

When the count pulse is applied to clock input T, the number of count pulse appears in BCD code on $Q_A \sim Q_D$ synchronized with the count pulse. Counting occurs as T changes from low-level to high-level.

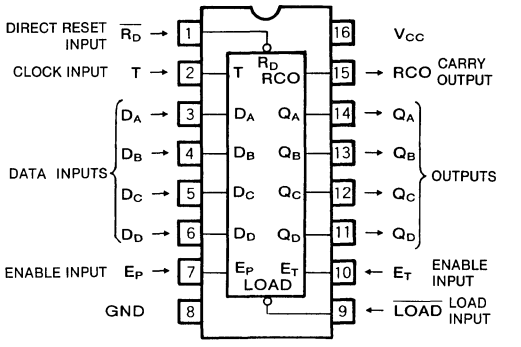
Preset is synchronized with the count pulse. Irrespective of the enable inputs $E_P$ and $E_T$, $D_A \sim D_D$ signals appear on $Q_A \sim Q_D$ when load input $\overline{LOAD}$ is set low and T changes from low to high.

When a value greater than 9 is preset, counting will be executed as shown in the state diagram.

When direct reset $\overline{R_D}$ is set low, irrespective of other inputs, reset occurs asynchronously and $Q_A \sim Q_D$ become low.

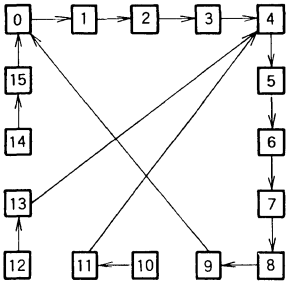
Carry output RCO becomes high only when $Q_A$, $Q_D$ and $E_T$ are high. $E_P$, $E_T$ and RCO are used when counters are connected in synchronous cascade connection and made a $10^n$ counter.

## PIN CONFIGURATION (TOP VIEW)

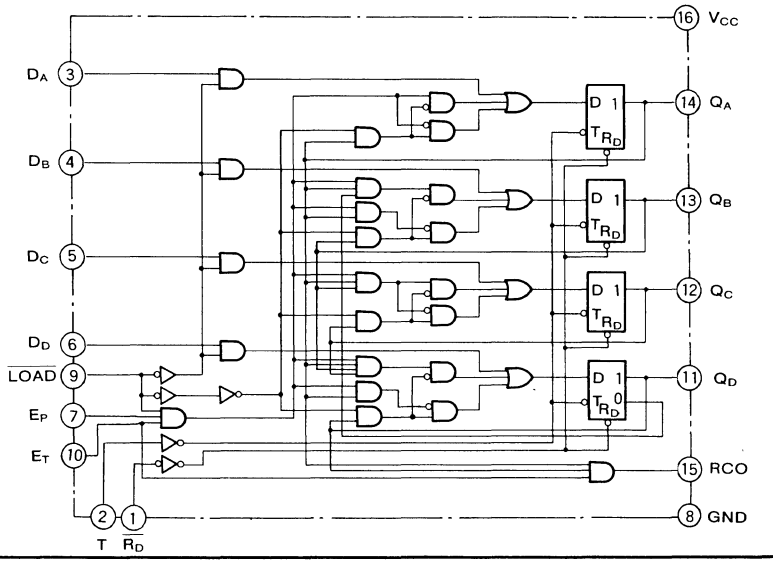



Outline 16P4

## STATE DIAGRAM




## LOGIC DIAGRAM






MITSUBISHI ELECTRIC

## SYNCHRONOUS PRESETTABLE DECADE COUNTER WITH DIRECT RESET

### FUNCTION TABLE (Note 1)

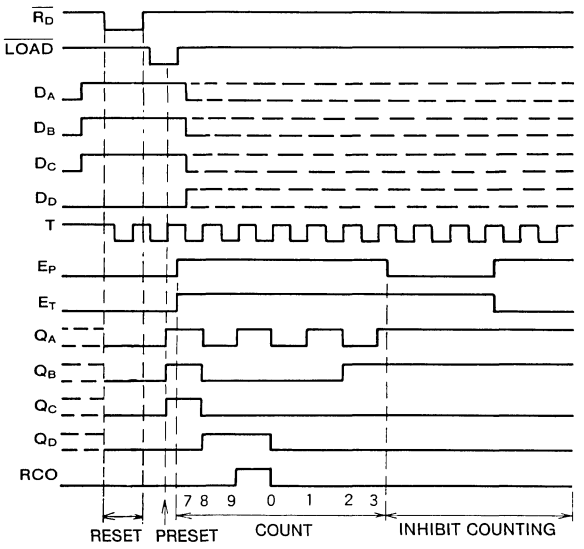
| Inputs | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{R_D}$ | $\overline{LOAD}$ | $E_T$ | $E_P$ | T | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | RCO |
| L | X | X | X | X | L | L | L | L | L |
| H | L | L | X | ↑ | $D_A$ | $D_B$ | $D_C$ | $D_D$ | L |
| H | L | H | X | ↑ | | | | | L* |
| H | H | H | H | ↑ | Count | | | | L* |
| H | H | L | X | X | Inhibit counting | | | | L |
| H | H | H | L | X | Inhibit counting | | | | L* |

Note 1: ↑ : Transition from low to high (positive edge trigger)

* : RCO, usually low, becomes high when $Q_A$, $Q_D$ and $E_T$ are high, i.e., $RCO = Q_A \cdot Q_D \cdot E_T$.

X : Irrelevant

### TIMING DIAGRAM




### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | High-level state | −0.5 ~ $V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 ~ +75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65 ~ +150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## SYNCHRONOUS PRESETTABLE DECADE COUNTER WITH DIRECT RESET

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V, $I_{OH}$=−0.4mA | $T_a$=0~70°C | 2.7 | 3.4 | | V |
| | | | | $T_a$=−20~+75°C | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | | $V_{CC}$=5.5V, $V_I$=7V | $\overline{LOAD}$, T, $E_T$ | | | 0.2 | mA |
| | | | | $D_A$, $D_B$, $D_C$, $D_D$, $E_P$, $\overline{R_D}$ | | | 0.1 | |
| $I_{IH}$ | High-level input current | | $V_{CC}$=5.5V, $V_I$=2.7V | $\overline{LOAD}$, T, $E_T$ | | | 40 | μA |
| | | | | $D_A$, $D_B$, $D_C$, $D_D$, $E_P$, $\overline{R_D}$ | | | 20 | |
| $I_{IL}$ | Low-level input current | | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | $Q_A$~$Q_D$ | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| | | RCO | | | −15 | | −70 | |
| $I_{CC}$ | Supply current | | $V_{CC}$=5.5V | | | 12 | 21 | mA |

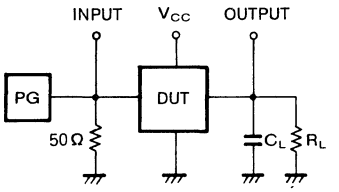
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_L$=500Ω; $T_a$=0~70°C Min | Typ * | Max | $T_a$=−20~+75°C Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | T | $Q_A$~$Q_D$ | 30 | 52 | | 28 | 52 | | MHz |
| $t_{PLH}$ | Propagation time | T | RCO | 8 | 17 | 26 | 8 | 17 | 27 | ns |
| $t_{PHL}$ | | | | 7 | 16 | 23 | 7 | 16 | 24 | |
| $t_{PLH}$ | | T | $Q_A$~$Q_D$ | 4 | 8 | 15 | 4 | 8 | 16 | ns |
| $t_{PHL}$ | | | | 6 | 12 | 17 | 6 | 12 | 18 | |
| $t_{PLH}$ | | $E_T$ | RCO | 3 | 9 | 17 | 3 | 9 | 18 | ns |
| $t_{PHL}$ | | | | 3 | 8 | 13 | 3 | 8 | 14 | |
| $t_{PHL}$ | | $\overline{R_D}$ | $Q_A$~$Q_D$ | 8 | 13 | 24 | 8 | 13 | 25 | ns |
| $t_{PHL}$ | | $\overline{R_D}$ | RCO | 11 | 18 | 28 | 11 | 18 | 29 | ns |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

## SYNCHRONOUS PRESETTABLE DECADE COUNTER WITH DIRECT RESET

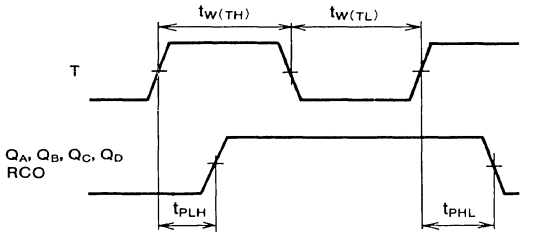
### TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_L$=500Ω)

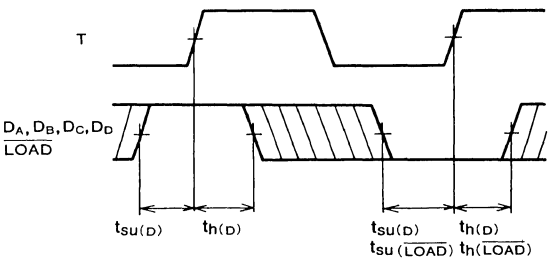
| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{w(TH)}$ | Pulse width | T "H" | 16.5 | 3 | | 17.5 | 3 | | ns |
| $t_{w(TL)}$ | | T "L" | 16.5 | 9 | | 17.5 | 9 | | |
| $t_{w(\overline{R_D})}$ | | $\overline{R_D}$ "L" | 15 | 4 | | 16 | 4 | | |
| $t_{su(D)}$ | Setup time before T ↑ | $D_A$~$D_D$ | 15 | 10 | | 16 | 10 | | ns |
| $t_{su(\overline{LOAD})}$ | | $\overline{LOAD}$ "L" | 15 | 10 | | 16 | 10 | | |
| $t_{su(E)}$ | | $E_P$, $E_T$ | 20 | 12 | | 21 | 12 | | |
| $t_{su(\overline{R_D})}$ | | $\overline{R_D}$ "H" (inactive) | 10 | 5 | | 11 | 5 | | |
| $t_{h(D)}$ | Hold time after T ↑ | $D_A$~$D_D$ | 0 | −8 | | 1 | −8 | | ns |
| $t_{h(\overline{LOAD})}$ | | $\overline{LOAD}$ "L" | 0 | −7 | | 1 | −7 | | |
| $t_{h(E)}$ | | $E_P$, $E_T$ | 0 | −12 | | 1 | −12 | | |

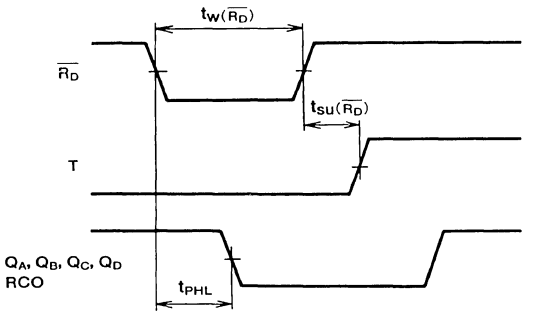
* All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

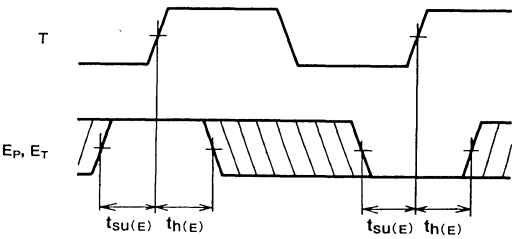
↑ · Transition from low to high

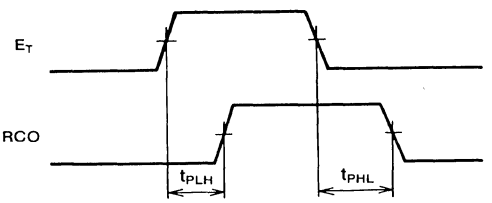
### TIMING DIAGRAM (Reference level = 1.3V)




Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance

# M74ALS161AP

## SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

## DESCRIPTION

The M74ALS161AP is a semiconductor integrated circuit of a synchronous presettable 4-bit binary (hexadecimal) counter with a direct reset input.

## FEATURES

- Direct reset and synchronous load inputs
- Enable inputs and carry output for cascade connection
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

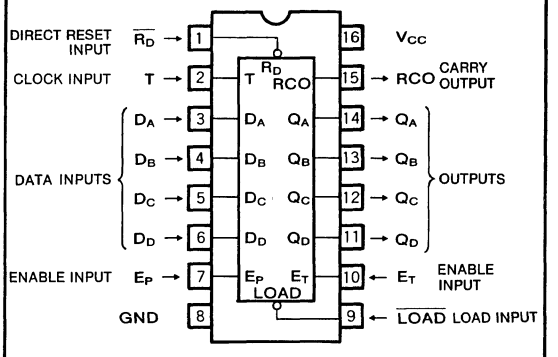
When the count pulse is applied to clock input T, the number of count pulse appears in 4-bit binary code on $Q_A \sim Q_D$ synchronized with the count pulse. Counting occurs as T changes from low-level to high-level.

Preset is synchronized with the count pulse. Irrespective of the enable inputs $E_P$ and $E_T$, $D_A \sim D_D$ signals appear on $Q_A \sim Q_D$ when load input $\overline{LOAD}$ is set low and T changes from low to high.

When direct reset $\overline{R_D}$ is set low, irrespective of other inputs, reset occurs asynchronously and $Q_A \sim Q_D$ become low.

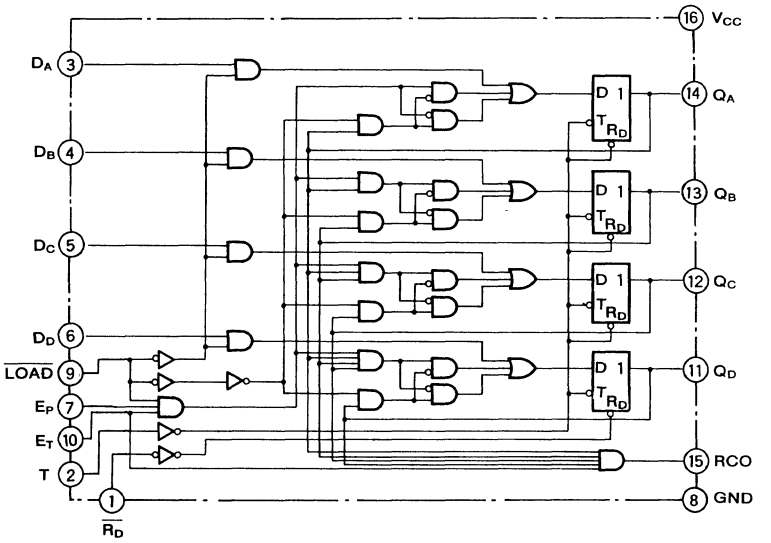
Carry output RCO becomes high only when $Q_A \sim Q_D$ and $E_T$ are high. $E_P$, $E_T$ and RCO are used when counters are connected in synchronous cascade connection and made an n-bit counter.

## PIN CONFIGURATION (TOP VIEW)




Outline 16P4

## LOGIC DIAGRAM






MITSUBISHI ELECTRIC

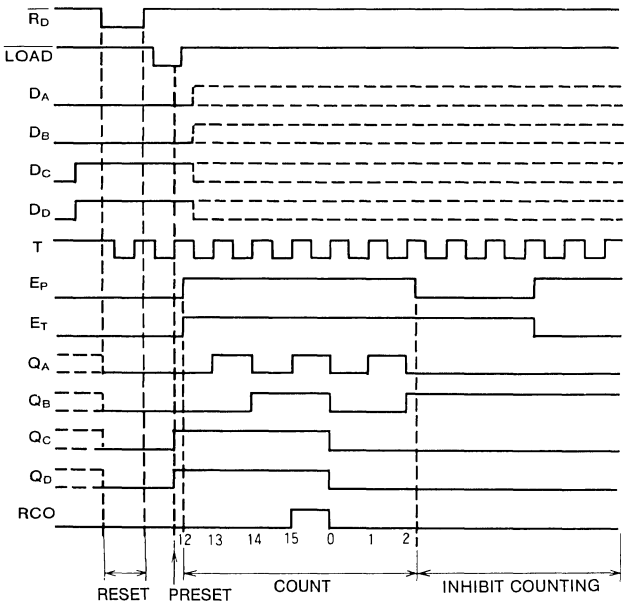
## SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

### FUNCTION TABLE (Note 1)

| Inputs | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{R_D}$ | $\overline{LOAD}$ | $E_T$ | $E_P$ | T | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | RCO |
| L | X | X | X | X | L | L | L | L | L |
| H | L | L | X | ↑ | $D_A$ | $D_B$ | $D_C$ | $D_D$ | L |
| H | L | H | X | ↑ | | | | | L* |
| H | H | H | H | ↑ | Count | | | | L* |
| H | H | L | X | X | Inhibit counting | | | | L |
| H | H | H | L | X | Inhibit counting | | | | L* |

Note 1. ↑ : Transition from low to high (positive edge trigger)
* : RCO, usually low, becomes high when $Q_A \sim Q_D$ and $E_T$ are high, i.e., $RCO = Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot E_T$.
X : Irrelevant

### TIMING DIAGRAM




### ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5～+7 | V |
| $V_I$ | Input voltage | | −0.5～+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5～$V_{CC}$ | V |
| Topr | Operating free-air ambient temperature range | | −20～+75 | ℃ |
| Tstg | Storage temperature range | | −65～+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| Topr | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $T_a$=0~70℃ | 2.7 | 3.4 | | V |
| | | | $I_{OH}$=−0.4mA | $T_a$=−20~+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | | $V_{CC}$=5.5V | $\overline{LOAD}$, T, $E_T$ | | | 0.2 | mA |
| | | | $V_I$=7V | $D_A$, $D_B$, $D_C$, $D_D$, $E_P$, $\overline{R_D}$ | | | 0.1 | |
| $I_{IH}$ | High-level input current | | $V_{CC}$=5.5V | $\overline{LOAD}$, T, $E_T$ | | | 40 | μA |
| | | | $V_I$=2.7V | $D_A$, $D_B$, $D_C$, $D_D$, $E_P$, $\overline{R_D}$ | | | 20 | |
| $I_{IL}$ | Low-level input current | | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | $Q_A$~$Q_D$ | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| | | RCO | | | −15 | | −70 | |
| $I_{CC}$ | Supply current | | $V_{CC}$=5.5V | | | 12 | 21 | mA |

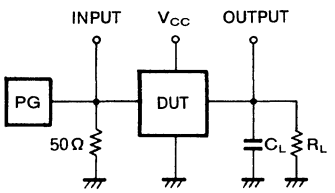
* : All typical values are at $V_{CC}$=5V, $T_a$=25°C.

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_L$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Input | Outputs | Min | Typ * | Max | Min | Typ * | Max | |
| $f_{max}$ | Maximum clock frequency | T | $Q_A$~$Q_D$ | 30 | 52 | | 28 | 52 | | MHz |
| $t_{PLH}$ | Propagation time | T | RCO | 8 | 17 | 26 | 8 | 17 | 27 | ns |
| $t_{PHL}$ | | | | 7 | 16 | 23 | 7 | 16 | 24 | |
| $t_{PLH}$ | | T | $Q_A$~$Q_D$ | 4 | 8 | 15 | 4 | 8 | 16 | ns |
| $t_{PHL}$ | | | | 6 | 12 | 17 | 6 | 12 | 18 | |
| $t_{PLH}$ | | $E_T$ | RCO | 3 | 9 | 17 | 3 | 9 | 18 | ns |
| $t_{PHL}$ | | | | 3 | 8 | 13 | 3 | 8 | 14 | |
| $t_{PHL}$ | | $\overline{R_D}$ | $Q_A$~$Q_D$ | 8 | 13 | 24 | 8 | 13 | 25 | ns |
| $t_{PHL}$ | | $\overline{R_D}$ | RCO | 11 | 18 | 28 | 11 | 18 | 29 | ns |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

## SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

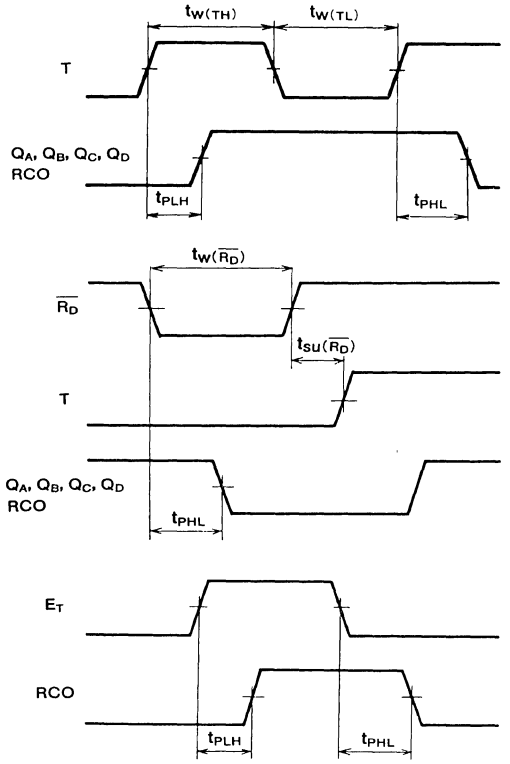
### TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_L$=500Ω)

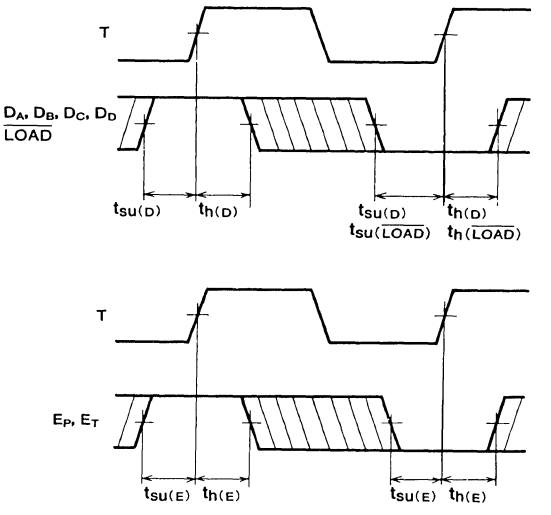
| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{w(TH)}$ | Pulse width | T "H" | 16.5 | 3 | | 17.5 | 3 | | ns |
| $t_{w(TL)}$ | | T "L" | 16.5 | 9 | | 17.5 | 9 | | |
| $t_{w(\overline{R_D})}$ | | $\overline{R_D}$ "L" | 15 | 4 | | 16 | 4 | | |
| $t_{su(D)}$ | Setup time before T↑ | $D_A$~$D_D$ | 15 | 10 | | 16 | 10 | | ns |
| $t_{su(\overline{LOAD})}$ | | $\overline{LOAD}$ "L" | 15 | 10 | | 16 | 10 | | |
| $t_{su(E)}$ | | $E_P$, $E_T$ | 20 | 12 | | 21 | 12 | | |
| $t_{su(\overline{R_D})}$ | | $\overline{R_D}$ "H" (inactive) | 10 | 5 | | 11 | 5 | | |
| $t_{h(D)}$ | Hold time after T↑ | $D_A$~$D_D$ | 0 | −8 | | 1 | −8 | | ns |
| $t_{h(\overline{LOAD})}$ | | $\overline{LOAD}$ "L" | 0 | −7 | | 1 | −7 | | |
| $t_{h(E)}$ | | $E_P$, $E_T$ | 0 | −12 | | 1 | −12 | | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↑: Transition from low to high

### TIMING DIAGRAM (Reference level = 1.3V)




Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS162AP

## FULLY SYNCHRONOUS PRESETTABLE DECADE COUNTER

## DESCRIPTION

The M74ALS162AP is a semiconductor integrated circuit of a synchronous presettable decade counter with a synchronous reset.

## FEATURES

- Synchronous reset and load inputs
- Enable inputs and carry output for cascade connection
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

When the count pulse is applied to clock input T, the number of count pulse appears in BCD code on $Q_A \sim Q_D$ synchronized with the count pulse. Counting occurs as T changes from low-level to high-level.

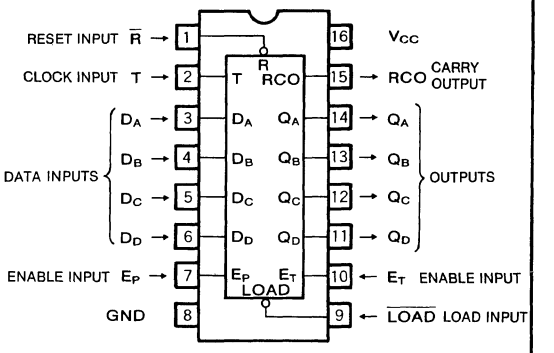
Preset is synchronized with the count pulse. Irrespective of the enable inputs $E_P$ and $E_T$, $D_A \sim D_D$ signals appear on $Q_A \sim Q_D$ when load input $\overline{LOAD}$ is set low and T changes from low to high.

When a value greater than 10 is preset, the count will be executed as shown in the state diagram.

When reset $\overline{R}$ is set low, and T changes from low to high, reset occurs synchronously and $Q_A \sim Q_D$ become low.

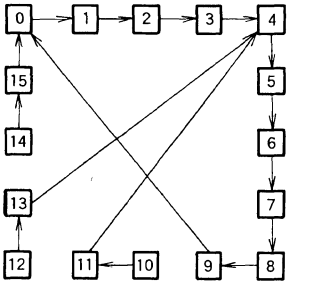
Carry output RCO becomes high only when $Q_A \sim Q_D$ and $E_T$ are high. $E_P$, $E_T$ and RCO are used when counters are connected in synchronous cascade connection and made a $10^n$ counter.

## PIN CONFIGURATION (TOP VIEW)

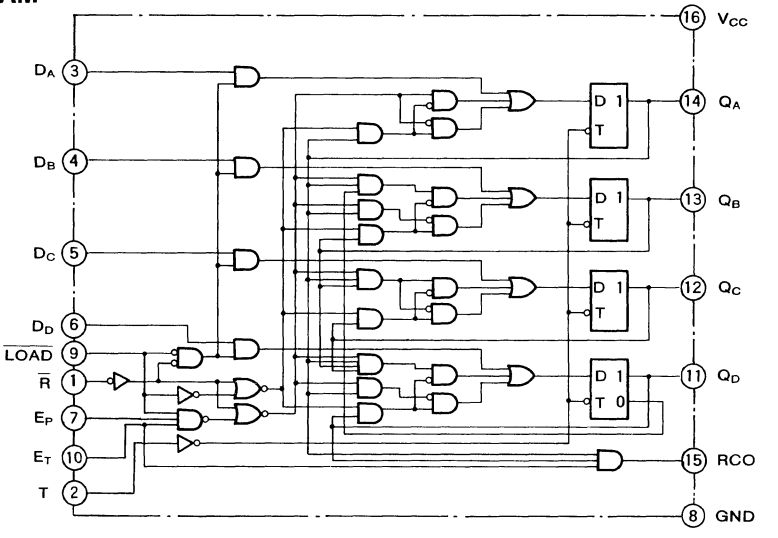



Outline 16P4

## STATE DIAGRAM




## LOGIC DIAGRAM






MITSUBISHI ELECTRIC

## FULLY SYNCHRONOUS PRESETTABLE DECADE COUNTER

### FUNCTION TABLE (Note 1)

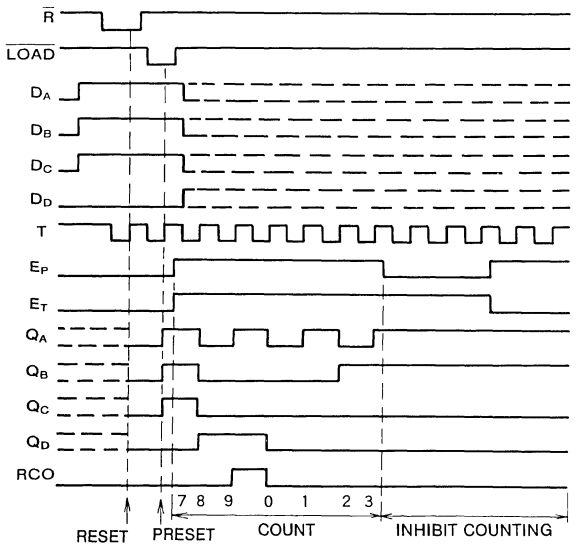
| Inputs | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{R}$ | $\overline{LOAD}$ | $E_T$ | $E_P$ | T | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | RCO |
| L | X | X | X | ↑ | L | L | L | L | L |
| H | L | L | X | ↑ | $D_A$ | $D_B$ | $D_C$ | $D_D$ | L |
| H | L | H | X | ↑ | | | | | L* |
| H | H | H | H | ↑ | Count | | | | L* |
| H | H | L | X | X | Inhibit counting | | | | L |
| H | H | H | L | X | Inhibit counting | | | | L* |

Note 1: ↑ : Transition from low to high (positive edge trigger)

* : RCO, usually low, becomes high when $Q_A$, $Q_D$ and $E_T$ are high, i.e., $RCO = Q_A \cdot Q_D \cdot E_T$.

X : Irrelevant

### TIMING DIAGRAM




### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | High-level state | −0.5 ~ $V_{CC}$ | V |
| Topr | Operating free-air ambient temperature range | | −20 ~ +75 | ℃ |
| Tstg | Storage temperature range | | −65 ~ +150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| Topr | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## FULLY SYNCHRONOUS PRESETTABLE DECADE COUNTER

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V, $I_{OH}$=−0.4mA | $T_a$=0~70℃ | 2.7 | 3.4 | | V |
| | | | | $T_a$=−20~+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | | $V_{CC}$=5.5V, $V_I$=7V | $\overline{LOAD}$, T, $E_T$ | | | 0.2 | mA |
| | | | | $D_A$, $D_B$, $D_C$, $D_D$, $E_P$, $\overline{R}$ | | | 0.1 | |
| $I_{IH}$ | High-level input current | | $V_{CC}$=5.5V, $V_I$=2.7V | $\overline{LOAD}$, T, $E_T$ | | | 40 | μA |
| | | | | $D_A$, $D_B$, $D_C$, $D_D$, $E_P$, $\overline{R}$ | | | 20 | |
| $I_{IL}$ | Low-level input current | | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | $Q_A$~$Q_D$ | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| | | RCO | | | −15 | | −70 | |
| $I_{CC}$ | Supply current | | $V_{CC}$=5.5V | | | 12 | 21 | mA |

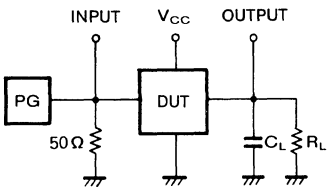
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_L$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | | Min | Typ * | Max | Min | Typ * | Max | |
| $f_{max}$ | Maximum clock frequency | T | $Q_A$~$Q_D$ | 30 | | | 28 | | | MHz |
| $t_{PLH}$ | Propagation time | T | RCO | 8 | | 26 | 8 | | 27 | ns |
| $t_{PHL}$ | | | | 7 | | 23 | 7 | | 24 | |
| $t_{PLH}$ | | T | $Q_A$~$Q_D$ | 4 | | 15 | 4 | | 16 | ns |
| $t_{PHL}$ | | | | 6 | | 17 | 6 | | 18 | |
| $t_{PLH}$ | | $E_T$ | RCO | 3 | | 17 | 3 | | 18 | ns |
| $t_{PHL}$ | | | | 3 | | 13 | 3 | | 14 | |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

## FULLY SYNCHRONOUS PRESETTABLE DECADE COUNTER

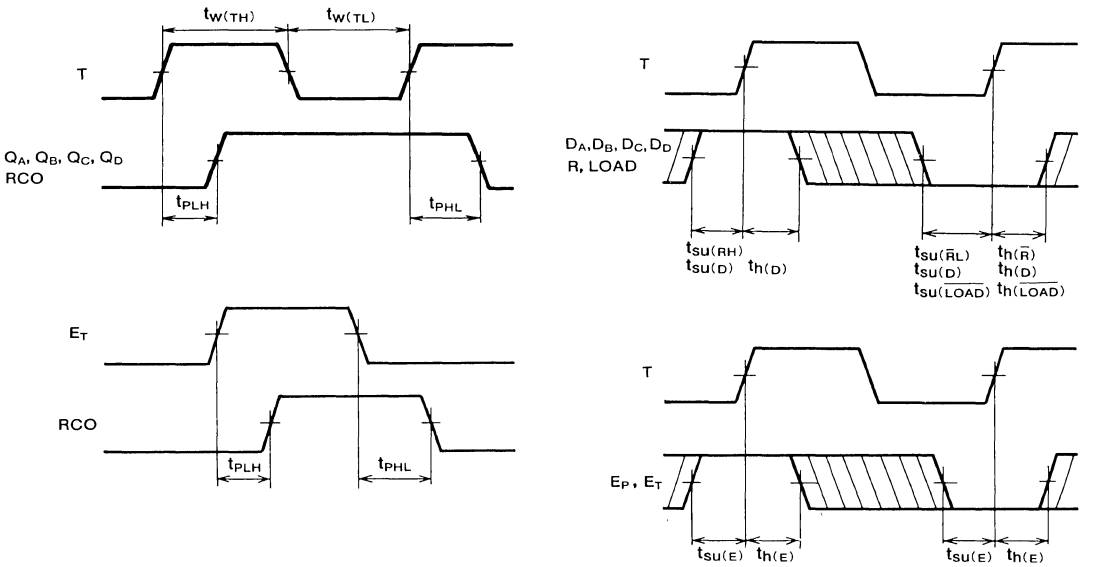
## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_L$=500Ω)

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{w(TH)}$ | Pulse width | T "H" | 16.5 | | | 17.5 | | | ns |
| $t_{w(TL)}$ | | T "L" | 16.5 | | | 17.5 | | | |
| $t_{su(D)}$ | Setup time before T ↑ | $D_A$~$D_D$ | 15 | | | 16 | | | ns |
| $t_{su(\overline{LOAD})}$ | | $\overline{LOAD}$ "L" | 15 | | | 16 | | | |
| $t_{su(\overline{RL})}$ | | $\overline{R}$ "L" | 15 | | | 16 | | | |
| $t_{su(\overline{RH})}$ | | $\overline{R}$ "H" (inactive) | 10 | | | 11 | | | |
| $t_{su(E)}$ | | $E_P$, $E_T$ | 25 | | | 26 | | | |
| $t_{h(D)}$ | Hold time after T ↑ | $D_A$~$D_D$ | 0 | | | 1 | | | ns |
| $t_{h(\overline{LOAD})}$ | | $\overline{LOAD}$ "L" | 0 | | | 1 | | | |
| $t_{h(\overline{R})}$ | | $\overline{R}$ "L" | 0 | | | 1 | | | |
| $t_{h(E)}$ | | $E_P$, $E_T$ | 0 | | | 1 | | | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↑: Transition from low to high

## TIMING DIAGRAM (Reference level = 1.3V)




Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change.

# M74ALS163AP

## FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

## DESCRIPTION

The M74ALS163AP is a semiconductor integrated circuit of a synchronous presettable 4-bit binary (hexadecimal) counter with a synchronous reset input.

## FEATURES

- Synchronous reset and load inputs
- Enable inputs and carry output for cascade connection
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

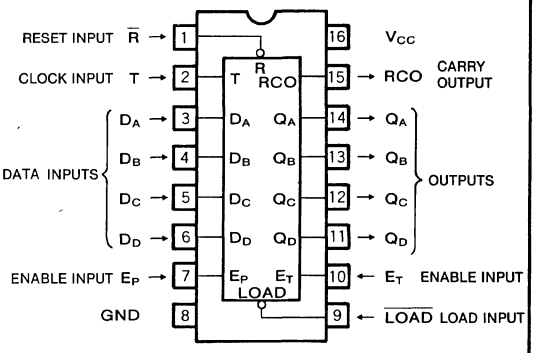
When the count pulse is applied to clock input T, the number of count pulse appears in 4-bit binary code on $Q_A \sim Q_D$ synchronized with the count pulse. Counting occurs as T changes from low-level to high-level.

Preset is synchronized with the count pulse. Irrespective of the enable inputs $E_P$ and $E_T$, $D_A \sim D_D$ signals appear on $Q_A \sim Q_D$ when load input $\overline{LOAD}$ is set low and T changes from low to high.

When reset R is set low and T changes from low to high, reset occurs synchronously and $Q_A \sim Q_D$ become low.

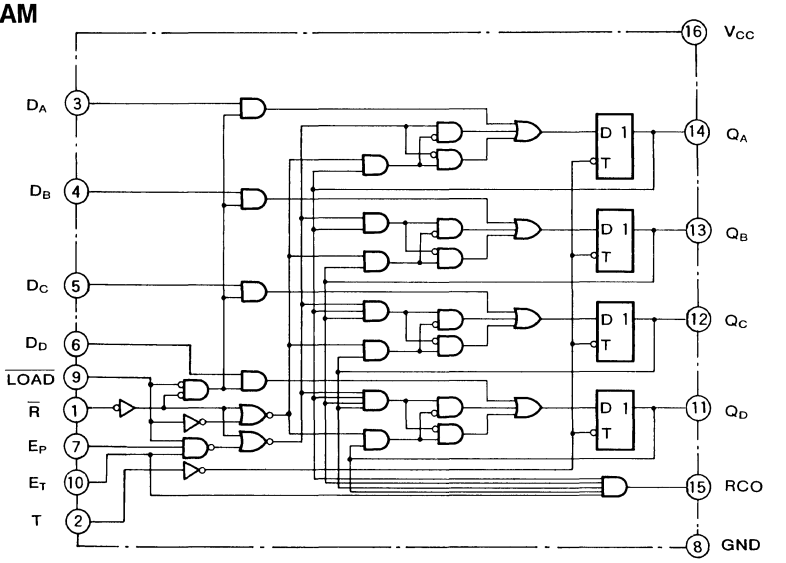
Carry output RCO becomes high only when $Q_A \sim Q_D$ and $E_T$ are high. $E_P$, $E_T$ and RCO are used when counters are connected in synchronous cascade connection and made an n-bit counter.

## PIN CONFIGURATION (TOP VIEW)




Outline 16P4

## LOGIC DIAGRAM






MITSUBISHI ELECTRIC

## FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

### FUNCTION TABLE (Note 1)

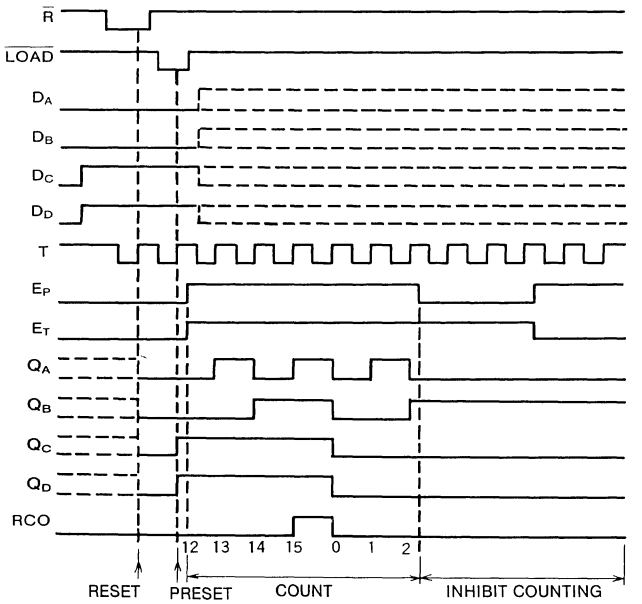
| Inputs | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{R}$ | $\overline{LOAD}$ | $E_T$ | $E_P$ | T | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | RCO |
| L | X | X | X | ↑ | L | L | L | L | L |
| H | L | L | X | ↑ | $D_A$ | $D_B$ | $D_C$ | $D_D$ | L |
| H | L | H | X | ↑ | | | | | L* |
| H | H | H | H | ↑ | Count | | | | L* |
| H | H | L | X | X | Inhibit counting | | | | L |
| H | H | H | L | X | Inhibit counting | | | | L* |

Note 1: ↑ : Transition from low to high (positive edge trigger)

* : RCO, usually low, becomes high when $Q_A \sim Q_D$ and $E_T$ are high, i.e., $RCO = Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot E_T$.

X : Irrelevant

### TIMING DIAGRAM




### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | High-level state | −0.5 ~ $V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 ~ +75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65 ~ +150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $T_a$=0~70℃ | 2.7 | 3.4 | | V |
| | | | $I_{OH}$=−0.4mA | $T_a$=−20~+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | | $V_{CC}$=5.5V | $\overline{LOAD}$, T, $E_T$ | | | 0.2 | mA |
| | | | $V_I$=7V | $D_A$, $D_B$, $D_C$, $D_D$, $E_P$, $\overline{R}$ | | | 0.1 | |
| $I_{IH}$ | High-level input current | | $V_{CC}$=5.5V | $\overline{LOAD}$, T, $E_T$ | | | 40 | μA |
| | | | $V_I$=2.7V | $D_A$, $D_B$, $D_C$, $D_D$, $E_P$, $\overline{R}$ | | | 20 | |
| $I_{IL}$ | Low-level input current | | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | $Q_A$~$Q_D$ | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| | | RCO | | | −15 | | −70 | |
| $I_{CC}$ | Supply current | | $V_{CC}$=5.5V | | | 12 | 21 | mA |

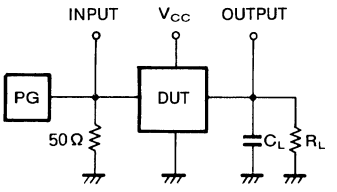
* : All typical values are at $V_{CC}$=5V, $T_a$=25°C

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_L$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Input | Outputs | Min | Typ * | Max | Min | Typ * | Max | |
| $f_{max}$ | Maximum clock frequency | T | $Q_A$~$Q_D$ | 30 | | | 28 | | | MHz |
| $t_{PLH}$ | Propagation time | T | RCO | 8 | | 26 | 8 | | 27 | ns |
| $t_{PHL}$ | | | | 7 | | 23 | 7 | | 24 | |
| $t_{PLH}$ | | T | $Q_A$~$Q_D$ | 4 | | 15 | 4 | | 16 | ns |
| $t_{PHL}$ | | | | 6 | | 17 | 6 | | 18 | |
| $t_{PLH}$ | | $E_T$ | RCO | 3 | | 17 | 3 | | 18 | ns |
| $t_{PHL}$ | | | | 3 | | 13 | 3 | | 14 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

## FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

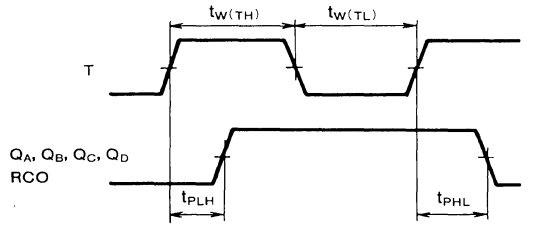
### TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_L$=500Ω)

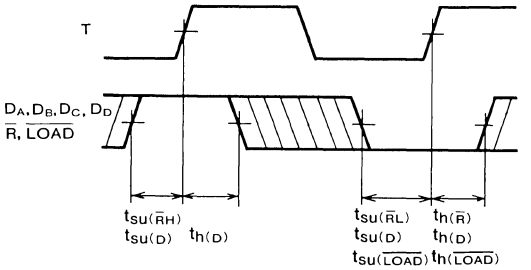
| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{w(TH)}$ | Pulse width | T "H" | 16.5 | | | 17.5 | | | ns |
| $t_{w(TL)}$ | | T "L" | 16.5 | | | 17.5 | | | |
| $t_{su(D)}$ | Setup time before T ↑ | $D_A$~$D_D$ | 15 | | | 16 | | | ns |
| $t_{su(\overline{LOAD})}$ | | $\overline{LOAD}$ "L" | 15 | | | 16 | | | |
| $t_{su(\overline{RL})}$ | | $\overline{R}$ "L" | 15 | | | 16 | | | |
| $t_{su(\overline{RH})}$ | | $\overline{R}$ "H" (inactive) | 10 | | | 11 | | | |
| $t_{su(E)}$ | | $E_P$, $E_T$ | 25 | | | 26 | | | |
| $t_{h(D)}$ | Hold time after T ↑ | $D_A$~$D_D$ | 0 | | | 1 | | | ns |
| $t_{h(\overline{LOAD})}$ | | $\overline{LOAD}$ "L" | 0 | | | 1 | | | |
| $t_{h(\overline{R})}$ | | $\overline{R}$ "L" | 0 | | | 1 | | | |
| $t_{h(E)}$ | | $E_P$, $E_T$ | 0 | | | 1 | | | |

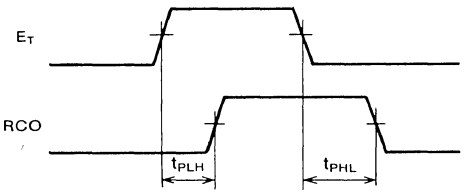
*: All typical values are at $V_{CC}$=5V, $T_a$=25°C

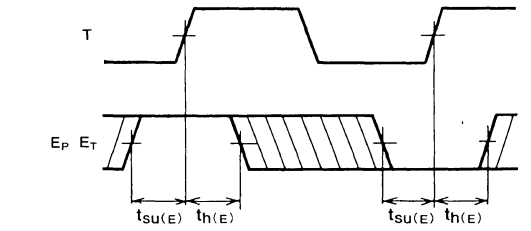
↑: Transition from low to high

### TIMING DIAGRAM (Reference level = 1.3V)




Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS240P

## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS240P is a semiconductor integrated circuit consisting of two blocks of buffers with 3-state inverted outputs and independent output control for each block.

## FEATURES

- In-phase output control inputs ($1\overline{OC}$, $2\overline{OC}$)
- High fan-out, 3-state output ($I_{OL}$ = 24mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

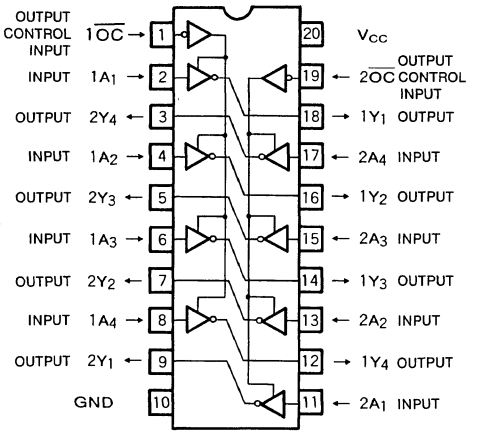
## FUNCTIONAL DESCRIPTION

When output control input $\overline{OC}$ is low-level, and if input A is low, then output Y is high. If A is high, Y is low. When $\overline{OC}$ is high, $Y_1 \sim Y_4$ are in high-impedance state irrespective of the status of A.

The outputs of all eight buffers can be simultaneously controlled by connecting $1\overline{OC}$ and $2\overline{OC}$. The outputs can be terminated with a load resistor of not less than 133Ω.

The low-power version of M74ALS240P, the M74ALS1240P, is also available.

## PIN CONFIGURATION (TOP VIEW)



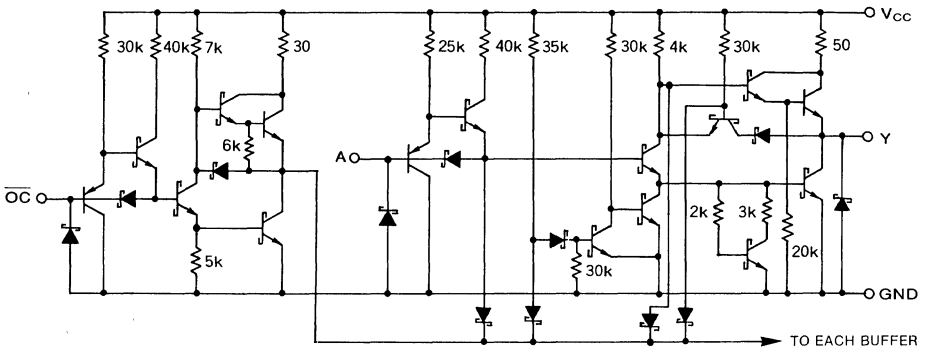

Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Output |
|---|---|---|
| A | $\overline{OC}$ | Y |
| L | L | H |
| H | L | L |
| X | H | Z |

Note 1: Z : High-impedance state
X : Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT Ω



MITSUBISHI ELECTRIC

## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (INVERTED)

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High level state or high impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 6 | 10 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 13 | 22 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | $V_{CC}$=5.5V | | | 15 | 25 | mA |

* : All typical values are at $V_{CC}$=5V, $T_a$=25°C

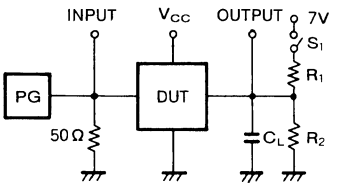
## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (INVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Output | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | $T_a$=0~70℃ Typ * | $T_a$=0~70℃ Max | $T_a$=−20~+75℃ Min | $T_a$=−20~+75℃ Typ * | $T_a$=−20~+75℃ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A | Y | 3 | 6 | 10 | 3 | 6 | 11 | ns |
| $t_{PHL}$ | | | | 2 | 5.5 | 9 | 2 | 5.5 | 10 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | Y | 5 | 10 | 15 | 5 | 10 | 16 | ns |
| $t_{PZL}$ | | | | 5 | 13 | 18 | 5 | 13 | 19 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | Y | 2 | 6 | 10 | 2 | 6 | 11 | ns |
| $t_{PLZ}$ | | | | 3 | 9 | 16 | 3 | 9 | 17 | |

*. All typical values are at $V_{CC}$=5V, $T_a$=25°C

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

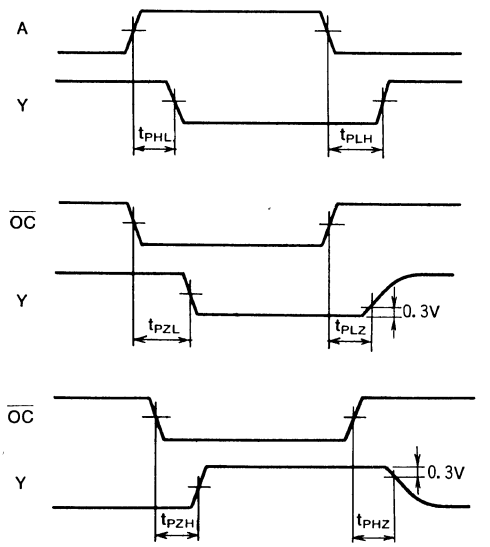
duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS241P

## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

### DESCRIPTION

The M74ALS241P is a semiconductor integrated circuit consisting of two blocks of buffers with 3-state noninverted outputs and independent output control for each block.

### FEATURES

- Complementary output control inputs ($1\overline{OC}$, 2OC)
- High fan-out, 3-state output ($I_{OL}$ = 24mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

### APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

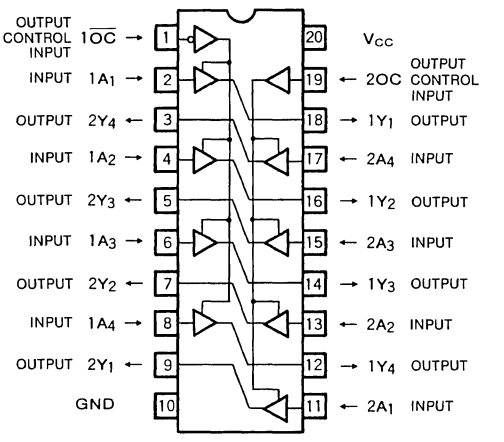
### FUNCTIONAL DESCRIPTION

When output control input $1\overline{OC}$ is low-level, and if input 1A is low, then output 1Y is low. If 1A is high, 1Y is high. When 2OC is high and input 2A is low, then output 2Y is low, but if 2A is high then 2Y is high. If $1\overline{OC}$ and 2OC are high and low respectively, then all outputs are in high-impedance state.

The device can be used as a 4-bit two-way bus driver by connecting $1\overline{OC}$ and 2OC, 1A and 2Y, 2A and 1Y respectively. The outputs can be terminated with a load resistor of not less than 133Ω.

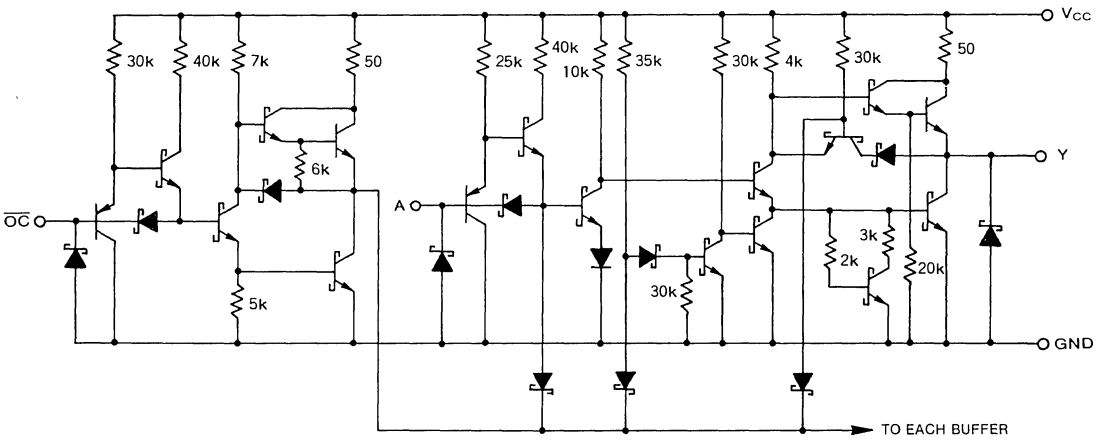
The low-power version of M74ALS241P, the M74ALS1241P, is also available.

### PIN CONFIGURATION (TOP VIEW)




Outline 20P4

### CIRCUIT SCHEMATIC (EACH BUFFER)



## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

### FUNCTION TABLE (Note 1)

| Inputs | | Output |
|---|---|---|
| 1A | $1\overline{OC}$ | 1Y |
| L | L | L |
| H | L | H |
| X | H | Z |

| Inputs | | Output |
|---|---|---|
| 2A | 2OC | 2Y |
| L | H | L |
| H | H | H |
| X | L | Z |

Note 1: Z : High-impedance state
X : Irrelevant

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High level state or high impedance state | −0.5~+5.5 | V |
| Topr | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| Tstg | Storage temperature range | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| Topr | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 9 | 15 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 15 | 26 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | $V_{CC}$=5.5V | | | 18 | 30 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

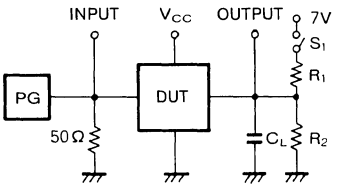
## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Output | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A | Y | 3 | 7.5 | 11 | 3 | 7.5 | 12 | ns |
| $t_{PHL}$ | | | | 3 | 7 | 10 | 3 | 7 | 11 | |
| $t_{PZH}$ | Output enable time | $1\overline{OC}$ | Y | 7 | 13 | 21 | 7 | 13 | 22 | ns |
| $t_{PZL}$ | | | | 7 | 15 | 21 | 7 | 15 | 22 | |
| $t_{PHZ}$ | Output disable time | $1\overline{OC}$ | Y | 2 | 7 | 13 | 2 | 7 | 14 | ns |
| $t_{PLZ}$ | | | | 3 | 12 | 18 | 3 | 12 | 19 | |
| $t_{PZH}$ | Output enable time | 2OC | Y | 7 | 15 | 21 | 7 | 15 | 22 | ns |
| $t_{PZL}$ | | | | 7 | 17 | 21 | 7 | 17 | 22 | |
| $t_{PHZ}$ | Output disable time | 2OC | Y | 2 | 9 | 13 | 2 | 9 | 14 | ns |
| $t_{PLZ}$ | | | | 3 | 14 | 18 | 3 | 14 | 19 | |

* All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

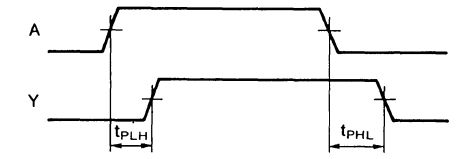
duty cycle=50%

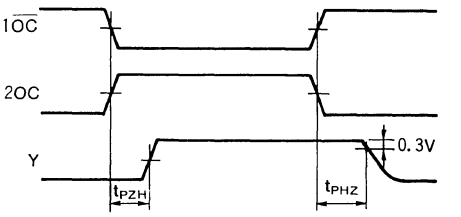
$Z_O$=50Ω

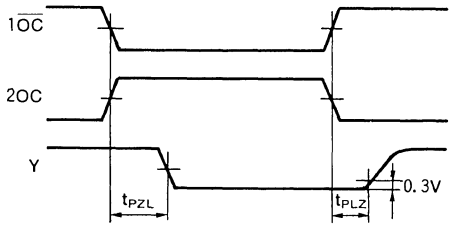
(2) $C_L$ includes probe and jig capacitance

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS242P

## QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS242P is a semiconductor integrated circuit consisting of four bus transmitter/receiver circuits with 3-state inverted outputs.

## FEATURES

- Two-way transmission or isolation between two 4-bit data
- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

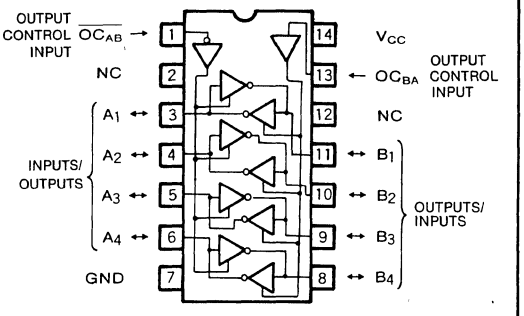
The inputs and outputs are mutually connected to form two-way buffers with 3-state inverted outputs.

The input/output direction is controlled by $\overline{OC_{AB}}$ and $OC_{BA}$.

When $\overline{OC_{AB}}$ and $OC_{BA}$ are low, pins A are made the input pins and pins B are made the output pins. When $\overline{OC_{AB}}$ and $OC_{BA}$ are high, pins B are made the input pins and pins A are made the output pins. When $\overline{OC_{AB}}$ is high and $OC_{BA}$ is low, both A and B are in the high-impedance state and A and B are isolated. The device can be used as a latch when $\overline{OC_{AB}}$ is low and $OC_{BA}$ is high. The outputs can be terminated with a load resistor of not less than 133Ω.

The low-power version of M74ALS242P, the M74ALS1242P, is also available.

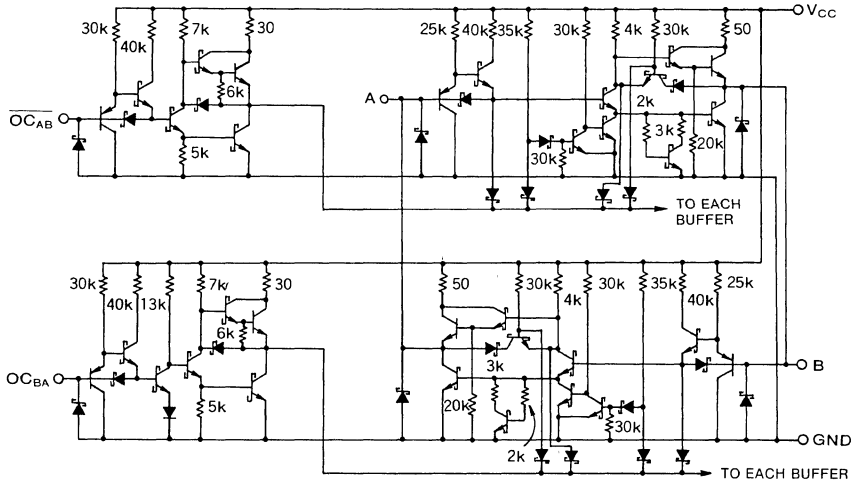
## PIN CONFIGURATION (TOP VIEW)




NC NO CONNECTION

Outline 14P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT. Ω



MITSUBISHI ELECTRIC

# QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC_{AB}}$ | $OC_{BA}$ | A | B |
| H | H | $\overline{O}$ | I |
| L | H | * | * |
| H | L | Z | Z |
| L | L | I | $\overline{O}$ |

Note 1: I : Input pins
$\overline{O}$ : Output pins (inverted output)
Z : High-impedance state (A and B are isolated)
* : In this case, data can be latched with the procedure shown below.
(1) Apply the data to be stored to A or B. ($OC_{BA}$ and $\overline{OC_{AB}}$ must be equally high or equally low.)
(2) Set $OC_{BA}$ high and $\overline{OC_{AB}}$ low respectively.
(3) Remove the data.
(4) The data applied in (1) is stored. If voltage is applied to A or B in this condition, the device may be damaged. Change the status of $OC_{BA}$ or $\overline{OC_{AB}}$ before applying voltage.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+5.5 | V |
| | | $\overline{OC_{AB}}$, $OC_{BA}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High level state or high impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $\overline{OC_{AB}}$, $OC_{BA}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | |
| $I_{IH}$ | High-level input current (Note 2) | $\overline{OC_{AB}}$, $OC_{BA}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current (Note 3) | $\overline{OC_{AB}}$, $OC_{BA}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 10 | 20 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 14 | 26 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 15 | 27 | mA |

* All typical values are at $V_{CC}$=5V, $T_a$=25°C
Note 2 For A and B, $I_{IH}$ includes off-state high-level output current $I_{OZH}$
Note 3· For A and B, $I_{IL}$ includes off state low-level output current $I_{OZL}$

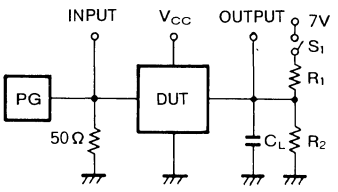
## QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Outputs | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A, B | B, A | 3 | 6.5 | 11 | 3 | 6.5 | 12 | ns |
| $t_{PHL}$ | | | | 2 | 6 | 10 | 2 | 6 | 11 | |
| $t_{PZH}$ | Output enable time | $\overline{OC_{AB}}$ | B | 4 | 11 | 18 | 4 | 11 | 19 | ns |
| $t_{PZL}$ | | | | 7 | 13 | 21 | 7 | 13 | 22 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC_{AB}}$ | B | 2 | 6 | 14 | 2 | 6 | 15 | ns |
| $t_{PLZ}$ | | | | 4 | 9 | 18 | 4 | 9 | 19 | |
| $t_{PZH}$ | Output enable time | $OC_{BA}$ | A | 4 | 13 | 18 | 4 | 13 | 19 | ns |
| $t_{PZL}$ | | | | 7 | 15 | 21 | 7 | 15 | 22 | |
| $t_{PHZ}$ | Output disable time | $OC_{BA}$ | A | 2 | 8 | 14 | 2 | 8 | 15 | ns |
| $t_{PLZ}$ | | | | 4 | 11 | 18 | 4 | 11 | 19 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 4: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

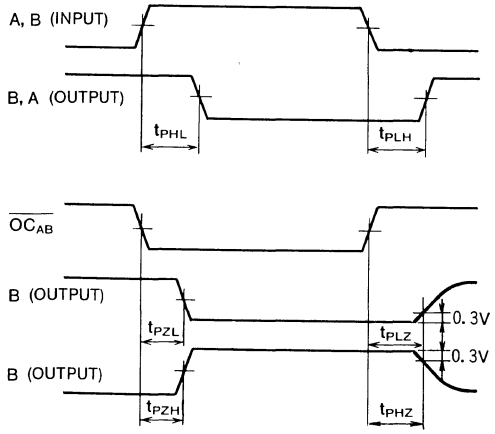
duty cycle=50%

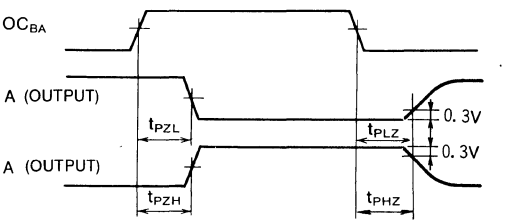
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

### TIMING DIAGRAM (Reference level = 1.3V)






MITSUBISHI ELECTRIC

# M74ALS243P

## QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS243P is a semiconductor integrated circuit consisting of bus transmitter/receiver circuits with 3-state noninverted outputs.

## FEATURES

- Two-way transmission or isolation between two 4-bit data
- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

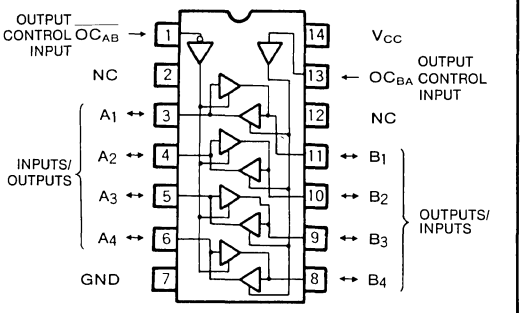
The inputs and outputs are mutually connected to form two-way buffers with 3-state noninverted outputs.

The input/output direction is controlled by $\overline{OC_{AB}}$ and $OC_{BA}$.

When $\overline{OC_{AB}}$ and $OC_{BA}$ are low, pins A are made the input pins and pins B are made the output pins. When $\overline{OC_{AB}}$ and $OC_{BA}$ are high, pins B are made the input pins and pins A are made the output pins. When $\overline{OC_{AB}}$ is high and $OC_{BA}$ is low, both A and B are in the high-impedance state and A and B are isolated. The device can be used as a latch when $\overline{OC_{AB}}$ is low and $OC_{BA}$ is high. The outputs can be terminated with a load resistor of not less than 133Ω.

The low-power version of M74ALS243P, the M74ALS1243P, is also available.

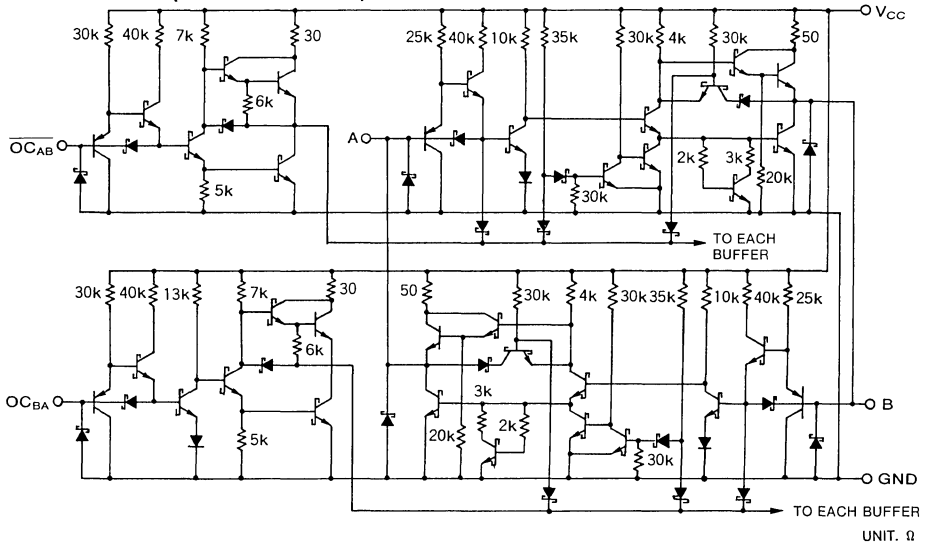
## PIN CONFIGURATION (TOP VIEW)




NC. NO CONNECTION

Outline 14P4

## CIRCUIT SCHEMATIC (EACH BUFFER)



# QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC_{AB}}$ | $OC_{BA}$ | A | B |
| H | H | O | I |
| L | H | * | * |
| H | L | Z | Z |
| L | L | I | O |

Note 1 I : Input pins
O : Output pins (noninverted output)
Z : High-impedance state (A and B are isolated)
*: In this case, data can be latched with the procedure shown below.
(1) Apply the data to be stored to A or B. ($OC_{BA}$ and $\overline{OC_{AB}}$ must be equally high or equally low.)
(2) Set $OC_{BA}$ high and $\overline{OC_{AB}}$ low respectively.
(3) Remove the data.
(4) The data applied in (1) is stored. If voltage is applied to A or B in this condition, the device may be damaged. Change the status of $OC_{BA}$ or $\overline{OC_{AB}}$ before applying voltage

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+5.5 | V |
| | | $\overline{OC_{AB}}$, $OC_{BA}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High level state or high impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $\overline{OC_{AB}}$, $OC_{BA}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | |
| $I_{IH}$ | High-level input current (Note 2) | $\overline{OC_{AB}}$, $OC_{BA}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current (Note 3) | $\overline{OC_{AB}}$, $OC_{BA}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 14 | 25 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 17 | 30 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 19 | 32 | mA |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C
Note 2 For A and B, $I_{IH}$ includes off-state high-level output current $I_{OZH}$.
Note 3: For A and B, $I_{IL}$ includes off state low-level output current $I_{OZL}$.

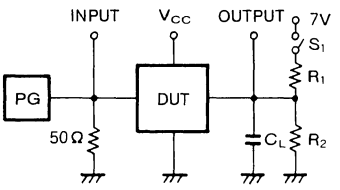
## QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70°C Min | $T_a$=0~70°C Typ * | $T_a$=0~70°C Max | $T_a$=−20~+75°C Min | $T_a$=−20~+75°C Typ * | $T_a$=−20~+75°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A, B | B, A | 4 | 8 | 11 | 4 | 8 | 12 | ns |
| $t_{PHL}$ | | | | 4 | 7.5 | 11 | 4 | 7.5 | 12 | |
| $t_{PZH}$ | Output enable time | $\overline{OC_{AB}}$ | B | 7 | 13 | 20 | 7 | 13 | 21 | ns |
| $t_{PZL}$ | | | | 7 | 15 | 20 | 7 | 15 | 21 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC_{AB}}$ | B | 2 | 7 | 14 | 2 | 7 | 15 | ns |
| $t_{PLZ}$ | | | | 4 | 12 | 22 | 4 | 12 | 23 | |
| $t_{PZH}$ | Output enable time | $OC_{BA}$ | A | 7 | 15 | 20 | 7 | 15 | 21 | ns |
| $t_{PZL}$ | | | | 7 | 17 | 20 | 7 | 17 | 21 | |
| $t_{PHZ}$ | Output disable time | $OC_{BA}$ | A | 2 | 9 | 14 | 2 | 9 | 15 | ns |
| $t_{PLZ}$ | | | | 4 | 14 | 22 | 4 | 14 | 23 | |

* All typical values are at $V_{CC}$=5V, $T_a$=25°C

Note 4. Measurement circuit




(1) The pulse generator (PG) has the following characteristics.

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

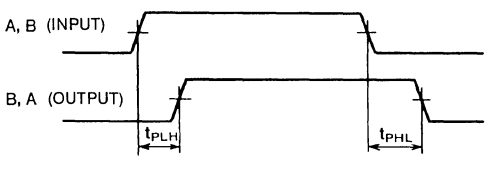
duty cycle=50%

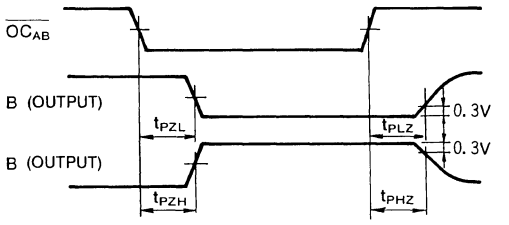
$Z_O$=50Ω

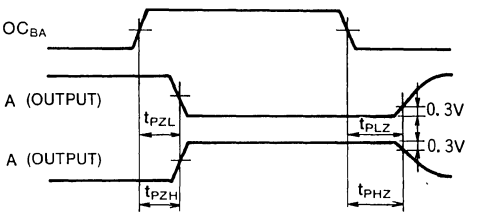
(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

## TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS244P

## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS244P is a semiconductor integrated circuit consisting of two blocks of buffers with 3-state noninverted outputs and independent output control for each block.

## FEATURES

- In-phase output control inputs ($1\overline{OC}$, $2\overline{OC}$)
- High fan-out, 3-state output ($I_{OL}$ = 24mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

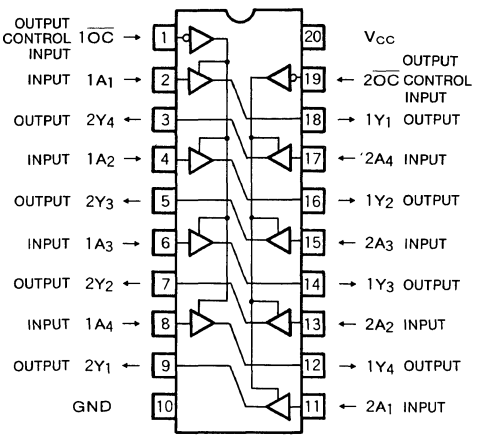
## FUNCTIONAL DESCRIPTION

When output control input $\overline{OC}$ is low-level, and if input A is low, then output Y is low. If A is high, Y is high. When $\overline{OC}$ is high, $Y_1 \sim Y_4$ are in high-impedance state irrespective of the status of A.

The outputs of all eight buffers can be controlled simultaneously by connecting $1\overline{OC}$ and $2\overline{OC}$. The outputs can be terminated with a load resistor of not less than 133Ω.

The low-power version of M74ALS244P, the M74ALS1244P, is also available.

## PIN CONFIGURATION (TOP VIEW)



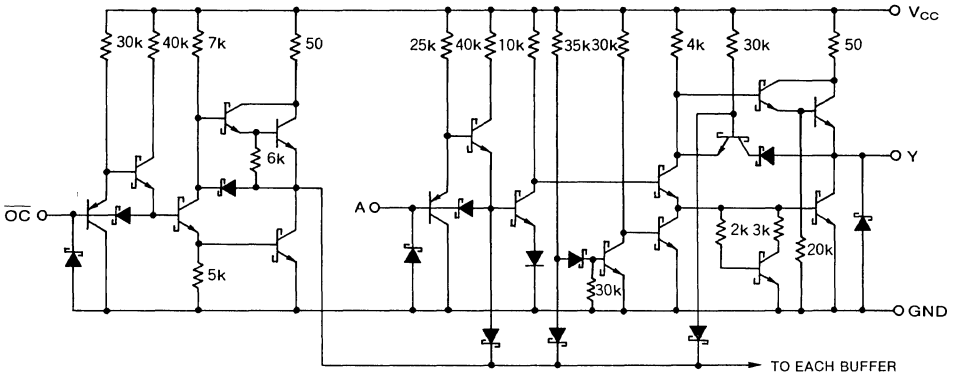

Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Output |
|---|---|---|
| A | $\overline{OC}$ | Y |
| L | L | L |
| H | L | H |
| X | H | Z |

Note 1 Z High-impedance state
X Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT Ω



MITSUBISHI ELECTRIC

## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High level state or high impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 9 | 15 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 15 | 26 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | $V_{CC}$=5.5V | | | 18 | 30 | mA |

* . All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

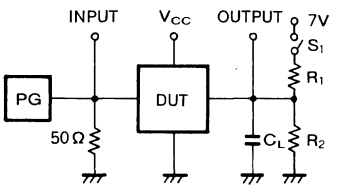
## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Output | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A | Y | 3 | 7.5 | 11 | 3 | 7.5 | 12 | ns |
| $t_{PHL}$ | | | | 3 | 7 | 10 | 3 | 7 | 11 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | Y | 7 | 13 | 21 | 7 | 13 | 22 | ns |
| $t_{PZL}$ | | | | 7 | 15 | 21 | 7 | 15 | 22 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | Y | 2 | 7 | 10 | 2 | 7 | 11 | ns |
| $t_{PLZ}$ | | | | 3 | 12 | 15 | 3 | 12 | 16 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit

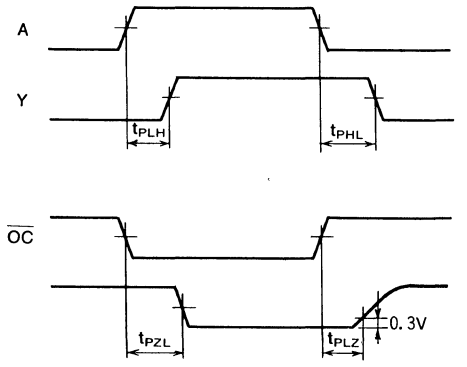



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS245P

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS245P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with 3-state noninverted outputs.

## FEATURES

- Two-way transmission or isolation between two 8-bit data
- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with 3-state noninverted outputs.

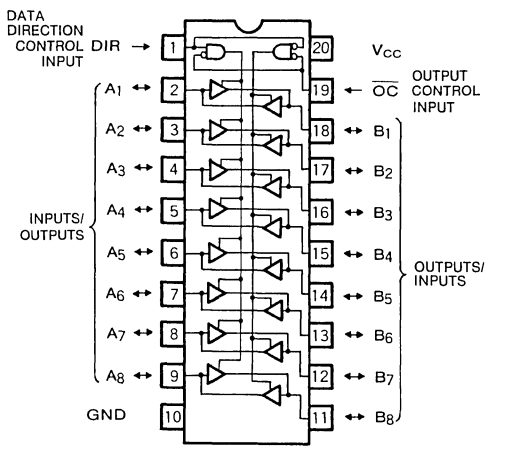
The input/output direction is controlled by DIR.

When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins. When $\overline{OC}$ is high, both A and B are in the high-impedance state and A and B are isolated.

This device is identical in all respects except for its name to the M74ALS645P.

The low-power version of M74ALS245P, the M74ALS1245P, is also available.

## PIN CONFIGURATION (TOP VIEW)



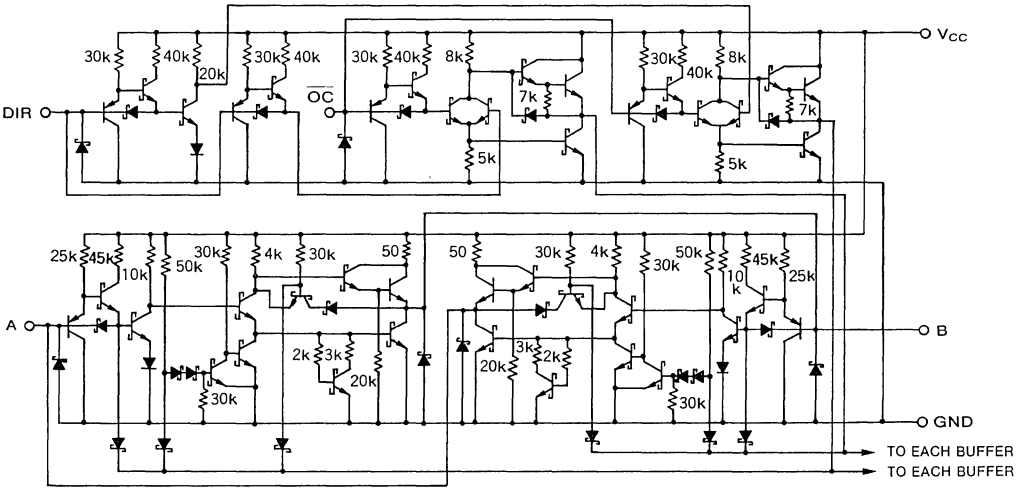

Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Input/Output | |
|---|---|---|---|
| $\overline{OC}$ | DIR | A | B |
| L | L | O | I |
| L | H | I | O |
| H | X | Z | Z |

Note 1: I : Input pins
O : Output pins (noninverted output)
Z : High-impedance state (A and B are isolated)
X : Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)



## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | A, B | | −0.5 ~ +5.5 | V |
| | | DIR, $\overline{OC}$ | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | | High level state or high impedance state | −0.5 ~ +5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20 ~ +75 | °C |
| $T_{stg}$ | Storage temperature range | | | −65 ~ +150 | °C |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | |
| $I_{IH}$ | High-level input current (Note 2) | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current (Note 3) | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 30 | 45 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 36 | 55 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 38 | 58 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 2. For A and B, $I_{IH}$ includes off-state high-level output current $I_{OZH}$

Note 3: For A and B, $I_{IL}$ includes off state low-level output current $I_{OZL}$

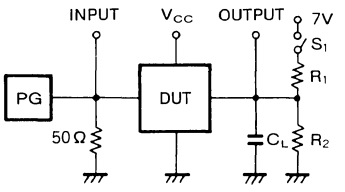
## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70°C Min | $T_a$=0~70°C Typ * | $T_a$=0~70°C Max | $T_a$=−20~+75°C Min | $T_a$=−20~+75°C Typ * | $T_a$=−20~+75°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A, B | B, A | 3 | 7 | 10 | 3 | 7 | 11 | ns |
| $t_{PHL}$ | | | | 3 | 7 | 10 | 3 | 7 | 11 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | A, B | 8 | 14 | 20 | 8 | 14 | 21 | ns |
| $t_{PZL}$ | | | | 10 | 18 | 26 | 10 | 18 | 27 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | A, B | 3 | 7 | 16 | 3 | 7 | 17 | ns |
| $t_{PLZ}$ | | | | 4 | 9 | 18 | 4 | 9 | 19 | |

* All typical values are at $V_{CC}$=5V, Ta=25°C.

Note 4: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

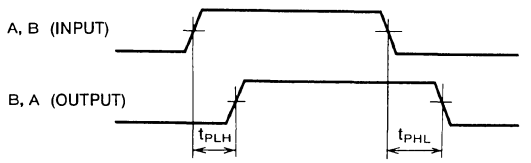
duty cycle=50%

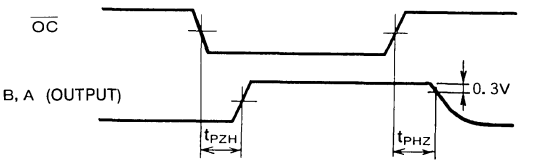
$Z_O$=50Ω

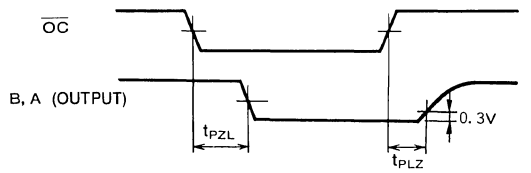
(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

## TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS299P

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUT

## DESCRIPTION

The M74ALS299P is a semiconductor integrated circuit of an 8-bit serial/parallel input-serial/parallel output shift register with 3-state outputs and a direct reset input.

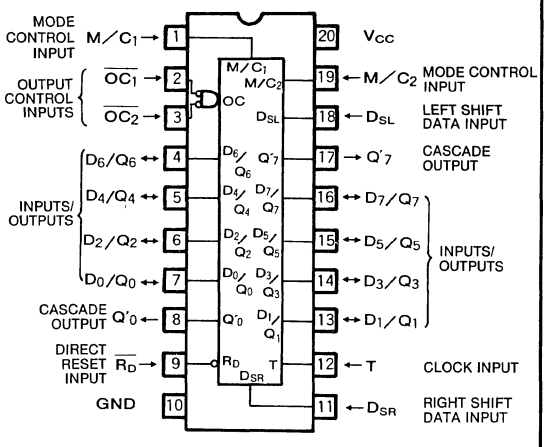
## FEATURES

- Synchronous serial/parallel input-serial/parallel output
- Right shift and left shift functions
- Possible expansion of bit number
- 3-state outputs
- Common pins for parallel input and output
- Direct reset input
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

## FUNCTIONAL DESCRIPTION

The operational modes listed below can be selected by combining the mode control inputs $M/C_1$ and $M/C_2$.

(1) Load — $M/C_1$: High; $M/C_2$: High
(2) Right shift — $M/C_1$: High; $M/C_2$: Low
(3) Left shift — $M/C_1$: Low; $M/C_2$: High
(4) Clock inhibited — $M/C_1$: Low; $M/C_2$: Low

With load, the 8-bit parallel data applied to inputs/outputs $D_0/Q_0 \sim D_7/Q_7$ are stored in each of the flip-flops when the clock input T changes from low to high.

With right shift, when the serial datum is applied to the right shift data input $D_{SR}$, one bit shift is made from $D_0/Q_0$ to $D_7/Q_7$ every time the clock input T changes from low to high.

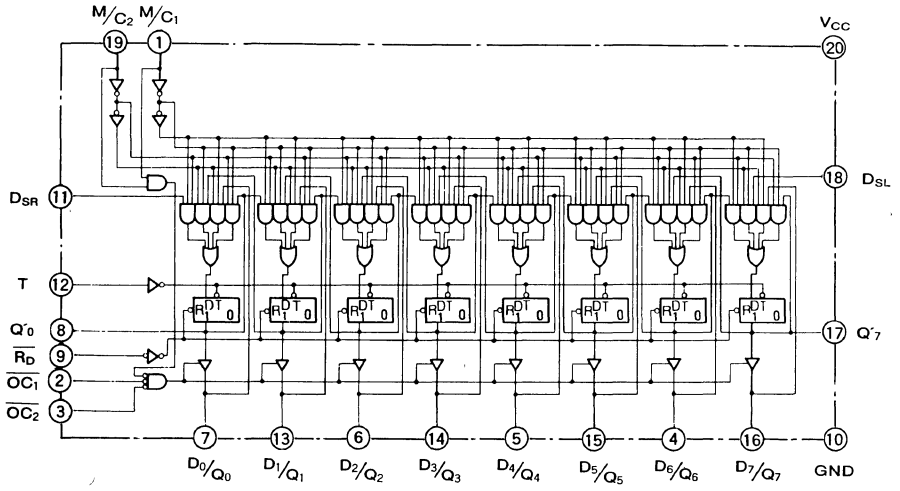
With left shift, when the serial datum is applied to the left shift data input $D_{SL}$, one bit shift is made from $D_7/Q_7$ to $D_0/Q_0$ every time the clock input T changes from low to high.

With clock inhibit, status of the flip-flops does not change since the clock pulses are inhibited from being applied to the flip-flops.(Reset possible)

When one or both of $\overline{OC_1}$ and $\overline{OC_2}$ are set high, all $D_0/Q_0 \sim D_7/Q_7$ outputs are in the high-impedance state "Z". Load, shift and reset occur as normal in this situation. Changes on the status of $\overline{OC_1}$ and $\overline{OC_2}$ do not affect the content of the flip-flops.

When $\overline{R_D}$ is set low, all the flip-flops are low irrespective of the status of the other inputs.

## LOGIC DIAGRAM






MITSUBISHI ELECTRIC

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUT

Cascade outputs $Q'_0$ and $Q'_7$ are used for expansion of the bit numbers. Reference should be made to the application example.

A device, the M74ALS323P featuring a synchronous reset input, is also available.

### FUNCTION TABLE (Note 1)

| Operational mode | Inputs | | | | | | | | Inputs / Outputs | | | | | | | | Outputs | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{R_D}$ | T | $M/C_1$ | $M/C_2$ | $D_{SR}$ | $D_{SL}$ | $\overline{OC_1}$* | $\overline{OC_2}$* | $D_0/Q_0$ | $D_1/Q_1$ | $D_2/Q_2$ | $D_3/Q_3$ | $D_4/Q_4$ | $D_5/Q_5$ | $D_6/Q_6$ | $D_7/Q_7$ | $Q'_0$ | $Q'_7$ |
| Direct reset | L | X | L | X | X | X | L | L | L | L | L | L | L | L | L | L | L | L |
| | L | X | X | L | X | X | L | L | L | L | L | L | L | L | L | L | L | L |
| | L | X | H | H | X | X | L | L | X | X | X | X | X | X | X | X | L | L |
| Right shift | H | ↑ | H | L | L | X | L | L | L | $Q_0^0$ | $Q_1^0$ | $Q_2^0$ | $Q_3^0$ | $Q_4^0$ | $Q_5^0$ | $Q_6^0$ | L | $Q_6^0$ |
| | H | ↑ | H | L | H | X | L | L | H | $Q_0^0$ | $Q_1^0$ | $Q_2^0$ | $Q_3^0$ | $Q_4^0$ | $Q_5^0$ | $Q_6^0$ | H | $Q_6^0$ |
| Left shift | H | ↑ | L | H | X | L | L | L | $Q_1^0$ | $Q_2^0$ | $Q_3^0$ | $Q_4^0$ | $Q_5^0$ | $Q_6^0$ | $Q_7^0$ | L | $Q_1^0$ | L |
| | H | ↑ | L | H | X | H | L | L | $Q_1^0$ | $Q_2^0$ | $Q_3^0$ | $Q_4^0$ | $Q_5^0$ | $Q_6^0$ | $Q_7^0$ | H | $Q_1^0$ | H |
| Load | H | ↑ | H | H | X | X | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | $D_0$ | $D_7$ |
| Clock inhibited | H | X | L | L | X | X | L | L | $Q_0^0$ | $Q_1^0$ | $Q_2^0$ | $Q_3^0$ | $Q_4^0$ | $Q_5^0$ | $Q_6^0$ | $Q_7^0$ | $Q_0^0$ | $Q_7^0$ |
| | H | L | X | X | X | X | L | L | $Q_0^0$ | $Q_1^0$ | $Q_2^0$ | $Q_3^0$ | $Q_4^0$ | $Q_5^0$ | $Q_6^0$ | $Q_7^0$ | $Q_0^0$ | $Q_7^0$ |

Note 1. $Q_n^0$ Level of Q before the indicated steady-state input conditions were established

X Irrelevant

↑ Transition from low to high (positive edge trigger)

$D_n$ $D_0/Q_0 \sim D_7/Q_7$ function as inputs, and $Q'_0$ and $Q'_7$ become the same status as $D_0$ and $D_7$ respectively.

* When one or both of $\overline{OC_1}$ and $\overline{OC_2}$ are set high, all $D_0/Q_0 \sim D_7/Q_7$ outputs are put in the high-impedance state "Z". Load, shift and reset operations occur normally in this situation

### ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5～+7 | V |
| $V_I$ | Input voltage | $D_0/Q_0 \sim D_7/Q_7$ | | −0.5～+5.5 | V |
| | | Other inputs | | −0.5～+7 | |
| $V_O$ | Output voltage | $D_0/Q_0 \sim D_7/Q_7$ | High-level state or high-impedance state | −0.5～+5.5 | V |
| | | $Q'_0$, $Q'_7$ | High-level state | −0.5～$V_{CC}$ | |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20～+75 | °C |
| $T_{stg}$ | Storage temperature range | | | −65～+150 | °C |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | $D_0/Q_0 \sim D_7/Q_7$ | 0 | | −2.6 | mA |
| | | $Q'_0$, $Q'_7$ | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | $D_0/Q_0$ $D_7/Q_7$ | 0 | | 24 | mA |
| | | $Q'_0$, $Q'_7$ | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 | | +75 | °C |

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUT

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $Q'_0$, $Q'_7$ | $V_{CC}$=4.5V, $I_{OH}$=−400μA | $T_a$=0~70°C | 2.7 | 3.4 | | V |
| | | | | $T_a$=−20~+75°C | 2.6 | 3.4 | | |
| | | $D_0/Q_0$~$D_7/Q_7$ | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | |
| $V_{OL}$ | Low-level output voltage | $Q'_0$, $Q'_7$ | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| | | $D_0/Q_0$~$D_7/Q_7$ | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $D_0/Q_0$~$D_7/Q_7$ | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | mA |
| | | Other inputs | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current (Note 2) | | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current (Note 3) | | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | $Q'_0$, $Q'_7$ | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| | | $D_0/Q_0$~$D_7/Q_7$ | | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 15 | 28 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 22 | 38 | mA |
| $I_{CCZ}$ | Supply current, outputs disabled | | $V_{CC}$=5.5V | | | 23 | 40 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 2. For $D_0/Q_0$ ~ $D_7/Q_7$, $I_{IH}$ includes off-state high-level output current $I_{OZH}$.

Note 3: For $D_0/Q_0$ ~ $D_7/Q_7$, $I_{IL}$ includes off-state low-level output current $I_{OZL}$.

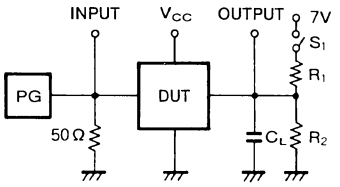
### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | | | Min | Typ * | Max | Min | Typ * | Max | |
| $f_{max}$ | Maximum clock frequency | | | 30 | 37 | | 28 | 37 | | MHz |
| $t_{PLH}$ | Propagation time | T | $D_0/Q_0$ ~ $D_7/Q_7$ | 4 | 7 | 13 | 4 | 7 | 14 | ns |
| $t_{PHL}$ | | | | 7 | 13 | 19 | 7 | 13 | 20 | |
| $t_{PLH}$ | | T | $Q'_0$, $Q'_7$ | 5 | 9 | 15 | 5 | 9 | 16 | ns |
| $t_{PHL}$ | | | | 8 | 14 | 18 | 8 | 14 | 19 | |
| $t_{PHL}$ | | $\overline{R_D}$ | $D_0/Q_0$ ~ $D_7/Q_7$ | 6 | 14 | 22 | 6 | 14 | 23 | ns |
| | | | $Q'_0$, $Q'_7$ | 6 | 15 | 22 | 6 | 15 | 23 | |
| $t_{PZH}$ | Output enable time | $\overline{OC_1}$ | $D_0/Q_0$ ~ $D_7/Q_7$ | 6 | 9 | 16 | 6 | 9 | 17 | ns |
| $t_{PZL}$ | | $\overline{OC_2}$ | | 8 | 13 | 22 | 8 | 13 | 23 | |
| $t_{PZH}$ | | $M/C_1$ | $D_0/Q_0$ ~ $D_7/Q_7$ | 7 | 10 | 17 | 7 | 10 | 18 | ns |
| $t_{PZL}$ | | $M/C_2$ | | 8 | 13 | 22 | 8 | 13 | 23 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC_1}$ | $D_0/Q_0$ ~ $D_7/Q_7$ | 1 | 5 | 8 | 1 | 5 | 9 | ns |
| $t_{PLZ}$ | | $\overline{OC_2}$ | | 2 | 6 | 15 | 2 | 6 | 16 | |
| $t_{PHZ}$ | | $M/C_1$ | $D_0/Q_0$ ~ $D_7/Q_7$ | 1 | 5 | 16 | 1 | 5 | 13 | ns |
| $t_{PLZ}$ | | $M/C_2$ | | 2 | 5 | 15 | 2 | 5 | 16 | |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUT

Note 4: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

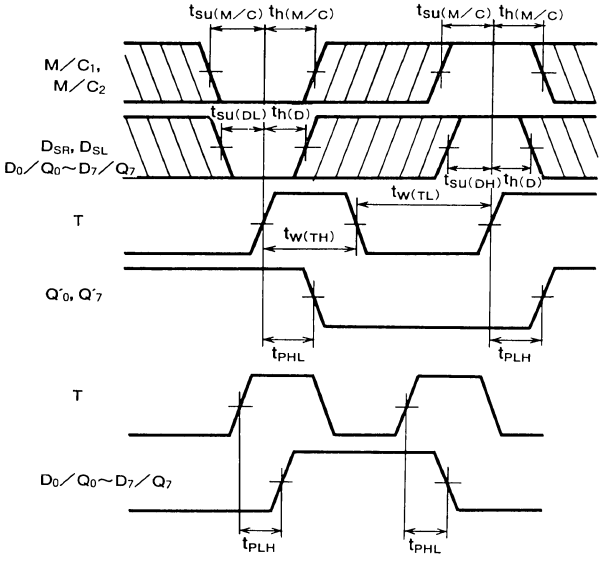
## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

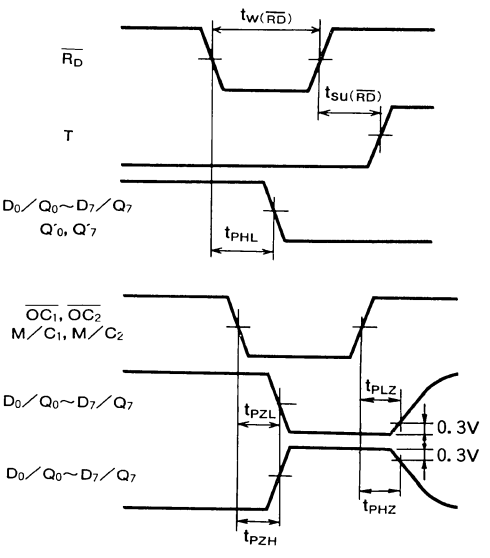
| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{w(TH)}$ | Pulse width | T "H" | 16.5 | 8 | | 17.5 | 8 | | ns |
| $t_{w(TL)}$ | | T "L" | 16.5 | 11 | | 17.5 | 11 | | |
| $t_{w(\overline{RD})}$ | | $\overline{R_D}$ "L" | 10 | 5 | | 11 | 5 | | |
| $t_{su(M/C)}$ | Setup time before T ↑ | $M/C_1$, $M/C_2$ | 20 | 13 | | 21 | 13 | | ns |
| $t_{su(DH)}$ | | $D_{SR}$, $D_{SL}$, $D_0/Q_0$~$D_7/Q_7$ "H" | 16 | 9 | | 17 | 9 | | |
| $t_{su(DL)}$ | | $D_{SR}$, $D_{SL}$, $D_0/Q_0$~$D_7/Q_7$ "L" | 6 | 3 | | 7 | 3 | | |
| $t_{su(\overline{RD})}$ | | $\overline{R_D}$ "H" (inactive) | 15 | 8 | | 16 | 8 | | |
| $t_{h(M/C)}$ | Hold time after T ↑ | $M/C_1$, $M/C_2$ | 0 | −8 | | 1 | −8 | | ns |
| $t_{h(D)}$ | | $D_{SR}$, $D_{SL}$, $D_0/Q_0$~$D_7/Q_7$ | 0 | −1 | | 1 | −1 | | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↑ Transition from low to high (positive edge trigger)

## TIMING DIAGRAM (Reference level = 1.3V)



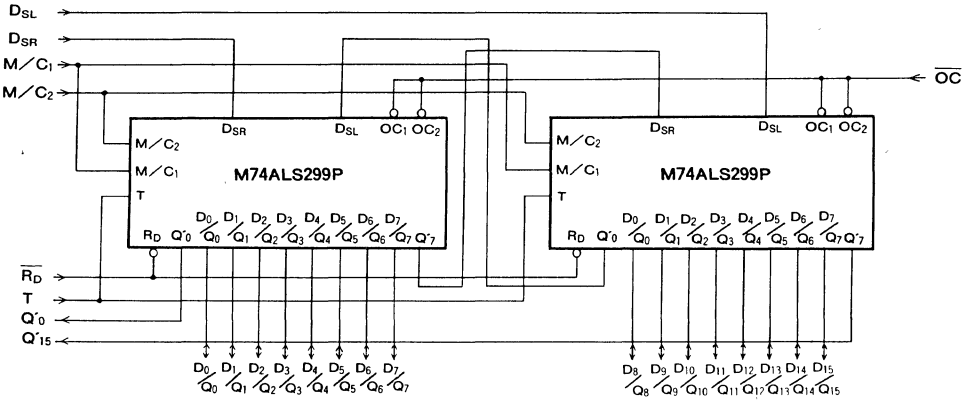




Note 5: The shaded areas indicate the period when the input is permitted to change for predictable output performance

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUT

### APPLICATION EXAMPLE

The figure below shows the configuration of a 16-bit shift register using two M74ALS299P devices. Similarly, an 8n-bit shift register can be configured with n ICs.



# M74ALS323P

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUT

## DESCRIPTION

The M74ALS323P is a semiconductor integrated circuit of an 8-bit serial/parallel input-serial/parallel output shift register with 3-state outputs and a synchronous reset input.

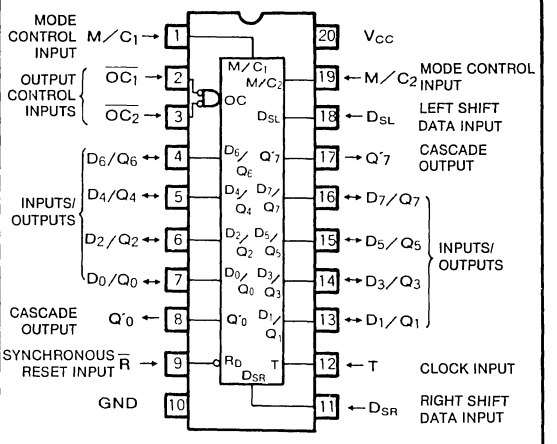
## FEATURES

- Synchronous serial/parallel input-serial/parallel output
- Right shift and left shift functions
- Possible expansion of bit number
- 3-state outputs
- Common pins for parallel input and output
- Synchronous reset input
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

## FUNCTIONAL DESCRIPTION

The operational modes listed below can be selected by combining the mode control inputs $M/C_1$ and $M/C_2$.

(1) Load $M/C_1$: High; $M/C_2$: High
(2) Right shift $M/C_1$: High; $M/C_2$: Low
(3) Left shift $M/C_1$: Low; $M/C_2$: High
(4) Clock inhibited $M/C_1$: Low; $M/C_2$: Low

With load, the 8-bit parallel data applied to inputs/outputs $D_0/Q_0 \sim D_7/Q_7$ are stored in each of the flip-flops when the clock input T changes from low to high.

With right shift, when the serial datum is applied to the right shift data input $D_{SR}$, one bit shift is made from $D_0/Q_0$ to $D_7/Q_7$ every time the clock input T changes from low to high.

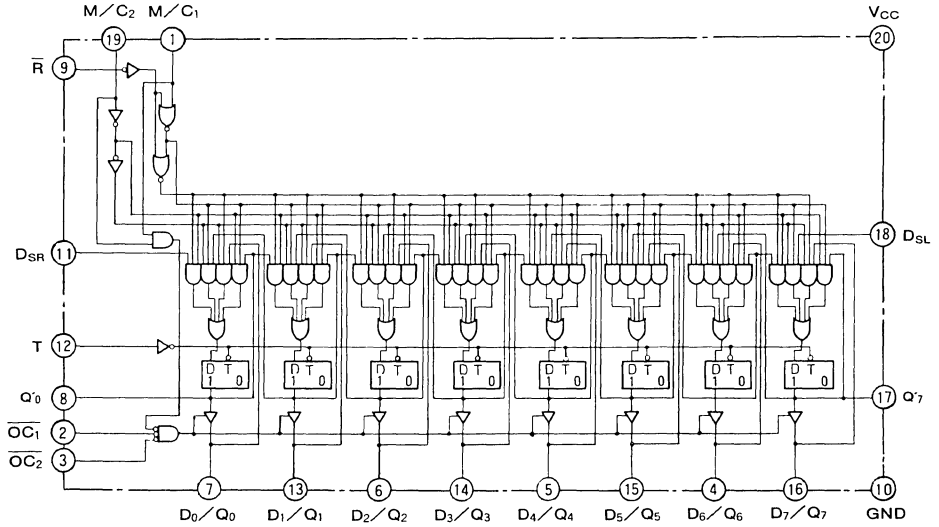
With left shift, when the serial datum is applied to the left shift data input $D_{SL}$, one bit shift is made from $D_7/Q_7$ to $D_0/Q_0$ every time the clock input T changes from low to high.

With clock inhibited, status of the flip-flops does not change since the clock pulses are inhibited from being applied to the flip-flops. (Reset possible.)

When one or both of $\overline{OC_1}$ and $\overline{OC_2}$ are set high, all $D_0/Q_0 \sim D_7/Q_7$ outputs are in the high-impedance state "Z". Load, shift and reset occur as normal in this situation. Changes on the status of $\overline{OC_1}$ and $\overline{OC_2}$ do not affect the content of the flip-flops.

When $\overline{R}$ is set low and T changes from low to high, all

## LOGIC DIAGRAM



## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUT

the flip-flops are set low irrespective of the status of the other inputs.

Cascade outputs $Q'_0$ and $Q'_7$ are used for expansion of the bit numbers. Reference should be made to the application example.

A device, the M74ALS299P featuring an asynchronous reset input, is also available.

## FUNCTION TABLE (Note 1)

| Operational mode | Inputs | | | | | | | | Inputs / Outputs | | | | | | | | Outputs | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{R}$ | T | $M/C_1$ | $M/C_2$ | $D_{SR}$ | $D_{SL}$ | $\overline{OC_1}$* | $\overline{OC_2}$* | $D_0/Q_0$ | $D_1/Q_1$ | $D_2/Q_2$ | $D_3/Q_3$ | $D_4/Q_4$ | $D_5/Q_5$ | $D_6/Q_6$ | $D_7/Q_7$ | $Q'_0$ | $Q'_7$ |
| Direct reset | L | ↑ | L | X | X | X | L | L | L | L | L | L | L | L | L | L | L | L |
| | L | ↑ | X | L | X | X | L | L | L | L | L | L | L | L | L | L | L | L |
| | L | ↑ | H | H | X | X | L | L | X | X | X | X | X | X | X | X | L | L |
| Right shift | H | ↑ | H | L | L | X | L | L | L | $Q_0^0$ | $Q_1^0$ | $Q_2^0$ | $Q_3^0$ | $Q_4^0$ | $Q_5^0$ | $Q_6^0$ | L | $Q_6^0$ |
| | H | ↑ | H | L | H | X | L | L | H | $Q_0^0$ | $Q_1^0$ | $Q_2^0$ | $Q_3^0$ | $Q_4^0$ | $Q_5^0$ | $Q_6^0$ | H | $Q_6^0$ |
| Left shift | H | ↑ | L | H | X | L | L | L | $Q_1^0$ | $Q_2^0$ | $Q_3^0$ | $Q_4^0$ | $Q_5^0$ | $Q_6^0$ | $Q_7^0$ | L | $Q_1^0$ | L |
| | H | ↑ | L | H | X | H | L | L | $Q_1^0$ | $Q_2^0$ | $Q_3^0$ | $Q_4^0$ | $Q_5^0$ | $Q_6^0$ | $Q_7^0$ | H | $Q_1^0$ | H |
| Load | H | ↑ | H | H | X | X | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | $D_0$ | $D_7$ |
| Clock inhibited | H | X | L | L | X | X | L | L | $Q_0^0$ | $Q_1^0$ | $Q_2^0$ | $Q_3^0$ | $Q_4^0$ | $Q_5^0$ | $Q_6^0$ | $Q_7^0$ | $Q_0^0$ | $Q_7^0$ |
| | H | L | X | X | X | X | L | L | $Q_0^0$ | $Q_1^0$ | $Q_2^0$ | $Q_3^0$ | $Q_4^0$ | $Q_5^0$ | $Q_6^0$ | $Q_7^0$ | $Q_0^0$ | $Q_7^0$ |

Note 1: $Q_n^0$: Level of Q before the indicated steady-state input conditions were established

X : Irrelevant

↑ : Transition from low to high (positive edge trigger)

$D_n$ : $D_0/Q_0 \sim D_7/Q_7$ function as inputs, and $Q'_0$ and $Q'_7$ become the same status as $D_0$ and $D_7$ respectively.

* : When one or both of $\overline{OC_1}$ and $\overline{OC_2}$ are set high, all $D_0/Q_0 \sim D_7/Q_7$ outputs are put in the high-impedance state "Z". Parallel read, shift and reset operations occur normally in this situation

## ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | $D_0/Q_0 \sim D_7/Q_7$ | | −0.5~+5.5 | V |
| | | Other inputs | | −0.5~+7 | |
| $V_O$ | Output voltage | $D_0/Q_0 \sim D_7/Q_7$ | High-level state or high-impedance state | −0.5~+5.5 | V |
| | | $Q'_0$, $Q'_7$ | High-level state | −0.5~$V_{CC}$ | |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | $D_0/Q_0 \sim D_7/Q_7$ | 0 | | −2.6 | mA |
| | | $Q'_0$, $Q'_7$ | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | $D_0/Q_0 \sim D_7/Q_7$ | 0 | | 24 | mA |
| | | $Q'_0$, $Q'_7$ | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 | | +75 | °C |

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUT

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | Q′0, Q′7 | $V_{CC}$=4.5V | $T_a$=0~70°C | 2.7 | 3.4 | | V |
| | | | $I_{OH}$=−400 μA | $T_a$=−20~+75°C | 2.6 | 3.4 | | |
| | | $D_0/Q_0 \sim D_7/Q_7$ | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | |
| $V_{OL}$ | Low-level output voltage | Q′0, Q′7 | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| | | $D_0/Q_0 \sim D_7/Q_7$ | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $D_0/Q_0 \sim D_7/Q_7$ | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | mA |
| | | Other inputs | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current (Note 2) | | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current (Note 3) | | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | Q′0, Q′7 | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| | | $D_0/Q_0 \sim D_7/Q_7$ | | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 15 | 28 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 22 | 38 | mA |
| $I_{CCZ}$ | Supply current, outputs disabled | | $V_{CC}$=5.5V | | | 23 | 40 | mA |

* . All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 2: For $D_0/Q_0 \sim D_7/Q_7$, $I_{IH}$ includes off-state high-level output current $I_{OZH}$.

Note 3: For $D_0/Q_0 \sim D_7/Q_7$, $I_{IL}$ includes off-state low-level output current $I_{OZL}$.

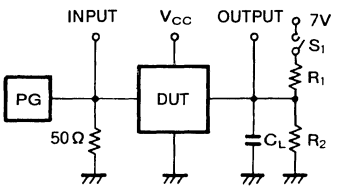
### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | | | Min | Typ * | Max | Min | Typ * | Max | |
| $f_{max}$ | Maximum clock frequency | | | 30 | 37 | | 28 | 37 | | MHz |
| $t_{PLH}$ | Propagation time | T | $D_0/Q_0$ ~ $D_7/Q_7$ | 4 | 7 | 13 | 4 | 7 | 14 | ns |
| $t_{PHL}$ | | | | 7 | 13 | 19 | 7 | 13 | 20 | |
| $t_{PLH}$ | | T | Q′0~Q′7 | 5 | 9 | 15 | 5 | 9 | 16 | ns |
| $t_{PHL}$ | | | | 8 | 14 | 18 | 8 | 14 | 19 | |
| $t_{PZH}$ | Output enable time | $\overline{OC_1}$ | $D_0/Q_0$ ~ $D_7/Q_7$ | 6 | 9 | 16 | 6 | 9 | 17 | ns |
| $t_{PZL}$ | | $\overline{OC_2}$ | | 8 | 13 | 22 | 8 | 13 | 23 | |
| $t_{PZH}$ | | $M/C_1$ | $D_0/Q_0$ ~ $D_7/Q_7$ | 7 | 10 | 17 | 7 | 10 | 18 | ns |
| $t_{PZL}$ | | $M/C_2$ | | 8 | 13 | 22 | 8 | 13 | 23 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC_1}$ | $D_0/Q_0$ ~ $D_7/Q_7$ | 1 | 5 | 8 | 1 | 5 | 9 | ns |
| $t_{PLZ}$ | | $\overline{OC_2}$ | | 2 | 6 | 15 | 2 | 6 | 16 | |
| $t_{PHZ}$ | | $M/C_1$ | $D_0/Q_0$ ~ $D_7/Q_7$ | 1 | 5 | 12 | 1 | 5 | 13 | ns |
| $t_{PLZ}$ | | $M/C_2$ | | 2 | 5 | 15 | 2 | 5 | 16 | |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUT

Note 4: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

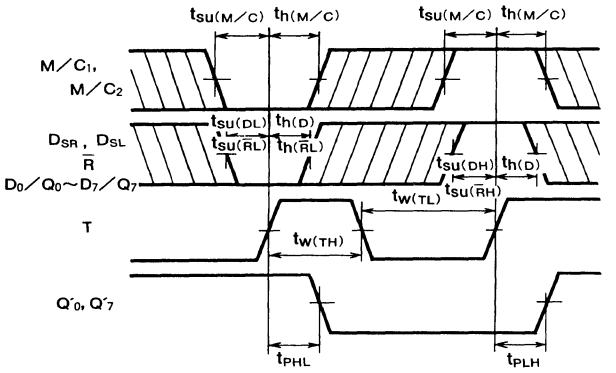
## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

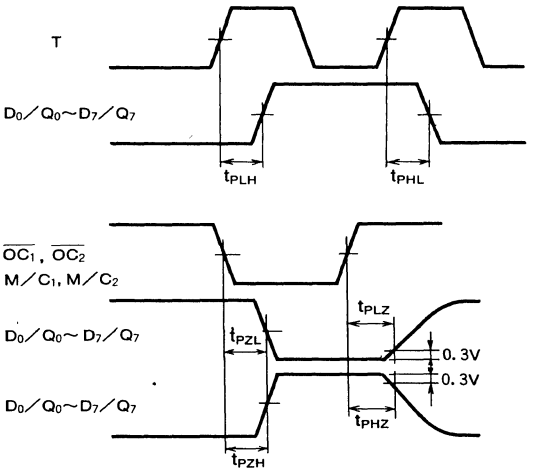
| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{w(TH)}$ | Pulse width | T "H" | 16.5 | 8 | | 17.5 | 8 | | ns |
| $t_{w(TL)}$ | | T "L" | 16.5 | 11 | | 17.5 | 11 | | |
| $t_{su(M/C)}$ | Setpu time before T↑ | $M/C_1$, $M/C_2$ | 20 | 13 | | 21 | 13 | | ns |
| $t_{su(DH)}$ | | $D_{SR}$, $D_{SL}$, $D_0/Q_0$~$D_7/Q_7$ "H" | 16 | 9 | | 17 | 9 | | |
| $t_{su(DL)}$ | | $D_{SR}$, $D_{SL}$, $D_0/Q_0$~$D_7/Q_7$ "L" | 6 | 3 | | 7 | 3 | | |
| $t_{su(\overline{R}H)}$ | | $\overline{R}$ "H" (inactive) | 16 | 11 | | 17 | 11 | | |
| $t_{su(\overline{R}L)}$ | | $\overline{R}$ "L" (active) | 20 | 12 | | 21 | 12 | | |
| $t_{h(M/C)}$ | Hold time after T↑ | $M/C_1$, $M/C_2$ | 0 | −8 | | 1 | −8 | | ns |
| $t_{h(D)}$ | | $D_{SR}$, $D_{SR}$, $D_0/Q_0$~$D_7/Q_7$ | 0 | −1 | | 1 | −1 | | |
| $t_{h(\overline{R}L)}$ | | $\overline{R}$ "L" | 0 | −10 | | 1 | −10 | | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↑: Transition from low to high (positive edge trigger)

## TIMING DIAGRAM (Reference level = 1.3V)

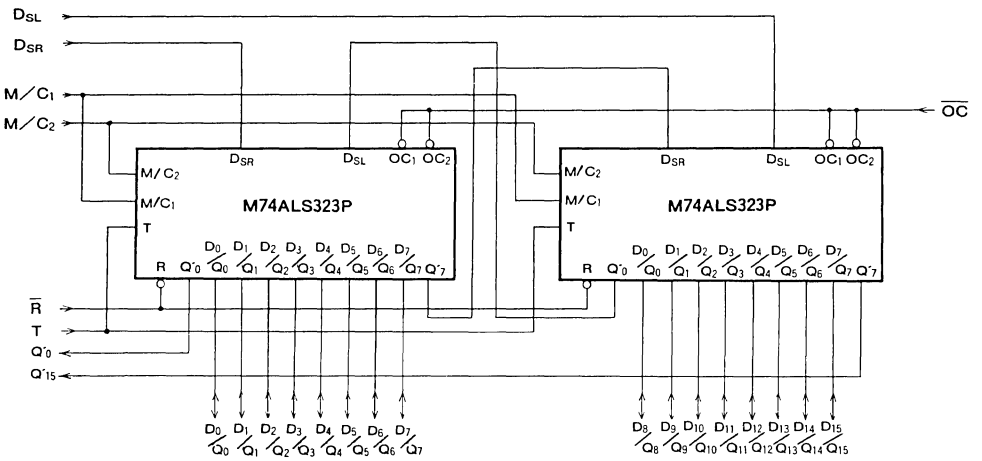



Note 5: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

## APPLICATION EXAMPLE

The figure below shows the configuration of a 16-bit shift register using two M74ALS323P devices. Similarly, an 8n-bit shift register can be configured with n ICs.



# M74ALS560AP

PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change

## SYNCHRONOUS PRESETTABLE DECADE COUNTER WITH 3-STATE OUTPUT

## DESCRIPTION

The M74ALS560AP is a semiconductor integrated circuit of a synchronous decade counter with 3-state outputs which has direct/synchronous reset and direct/synchronous preset inputs.

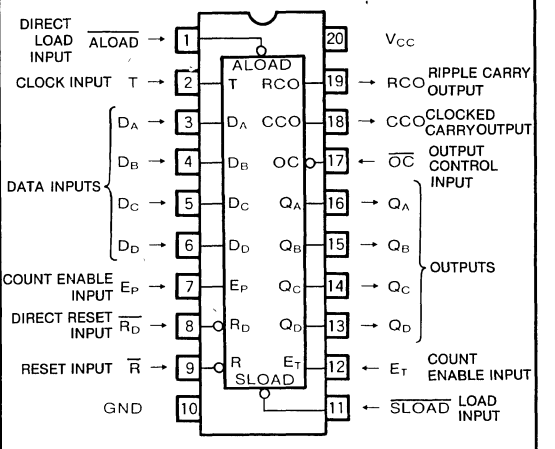
## FEATURES

- High fan-out ($Q_A \sim Q_D$: $I_{OL} = 24mA$, $I_{OH} = -2.6mA$)
- Direct and synchronous reset inputs
- Direct and synchronous load inputs
- Output control input ($\overline{OC}$)
- Enable inputs and carry outputs for cascade connection
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

## FUNCTIONAL DESCRIPTION

When the count pulse is applied to clock input T and enable inputs $E_P$ and $E_T$, reset inputs $\overline{R_D}$ and $\overline{R}$, and load inputs $\overline{ALOAD}$ and $\overline{SLOAD}$ are all high, the number of count pulses appears in BCD code on the outputs $Q_A \sim Q_D$ synchronized with the count pulse. Counting occurs when T changes from low to high.

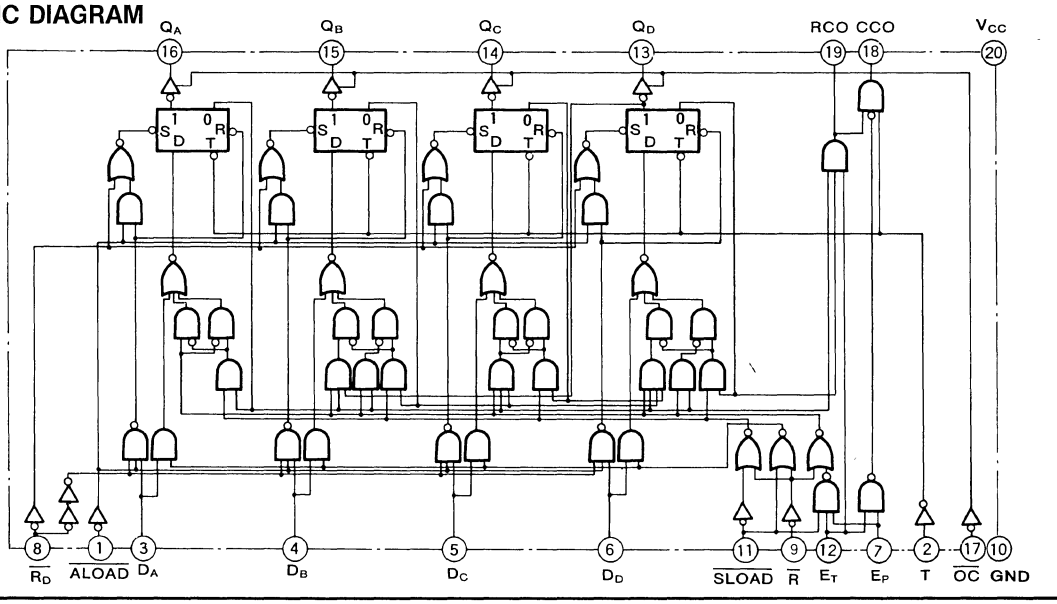
When direct load input $\overline{ALOAD}$ is set low, asynchronous preset occurs and the signals applied to data inputs $D_A \sim D_D$ appear on outputs $Q_A \sim Q_D$. When load input $\overline{SLOAD}$ is set low and T changes from low to high, synchronous preset occurs and the signals on $D_A \sim D_D$ appear on $Q_A \sim Q_D$. The status of $E_P$ and $E_T$ does not affect preset operation. When the counter is set to a numerical value of 10 or more, the counting proceeds in accordance with the state diagram.

When direct reset $\overline{R_D}$ is set low, irrespective of other inputs, asynchronous reset occurs and $Q_A \sim Q_D$, RCO and CCO become low. When reset $\overline{R}$ is low and T changes from low to high, reset operation occurs synchronously and $Q_A \sim Q_D$, RCO and CCO become low.

When output control input $\overline{OC}$ is set high, outputs $Q_A \sim Q_D$ are in high-impedance state. Even in this case, operations such as counting, preset and reset are possible.

Carry output RCO is high when $E_T$, $Q_A$ and $Q_D$ are high. Carry output CCO becomes high only when RCO, $E_P$ and $E_T$ are high and T is low. CCO is free from the glitches due to the propagation time dispersion in the inter-

## LOGIC DIAGRAM






MITSUBISHI ELECTRIC

## SYNCHRONOUS PRESETTABLE DECADE COUNTER WITH 3-STATE OUTPUT

nal gates.

$E_P$, $E_T$, RCO and CCO are used when counters are connected in synchronous cascade connection and made a $10^n$ counter. Usually, either RCO ro CCO may be connected to $E_T$ of the next device. However, use RCO for high-speed operation. Since CCO changes after T is set low, CCO cannot follow high-speed counting.

### FUNCTION TABLE (Note 1)

| Operational mode | Inputs | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{OC}$# | $\overline{R_D}$ | $\overline{ALOAD}$ | $\overline{R}$ | $\overline{SLOAD}$ | $E_T$ | $E_P$ | T | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| Output "Z" ($Q_A$~$Q_D$) | H | X | X | X | X | X | X | X | Z | Z | Z | Z |
| Direct reset | L | L | X | X | X | X | X | X | L | L | L | L |
| Direct load | L | H | L | X | X | X | X | X | $D_A$ | $D_B$ | $D_C$ | $D_D$ |
| Synchronous reset | L | H | H | L | X | X | X | ↑ | L | L | L | L |
| Synchronous load | L | H | H | H | L | X | X | ↑ | $D_A$ | $D_B$ | $D_C$ | $D_D$ |
| Count | L | H | H | H | H | H | H | ↑ | Count (decimal) | | | |
| Inhibit counting | L | H | H | H | H | L | X | X | $Q_A^0$ | $Q_B^0$ | $Q_C^0$ | $Q_D^0$ |
| | L | H | H | H | H | X | L | X | $Q_A^0$ | $Q_B^0$ | $Q_C^0$ | $Q_D^0$ |

Note 1: X : Irrelevant

Z : High-impedance state

↑ : Transition from low to high (positive edge trigger)

$Q_A^0$~$Q_D^0$ Level of $Q_A$~$Q_D$ before the indicated steady-state input conditions were established

# The setting of input $\overline{OC}$ does not affect the operation of reset, load, count and count inhibit. However, data appear at $Q_A$~$Q_D$ only when $\overline{OC}$ is low

### RCO FUNCTION TABLE

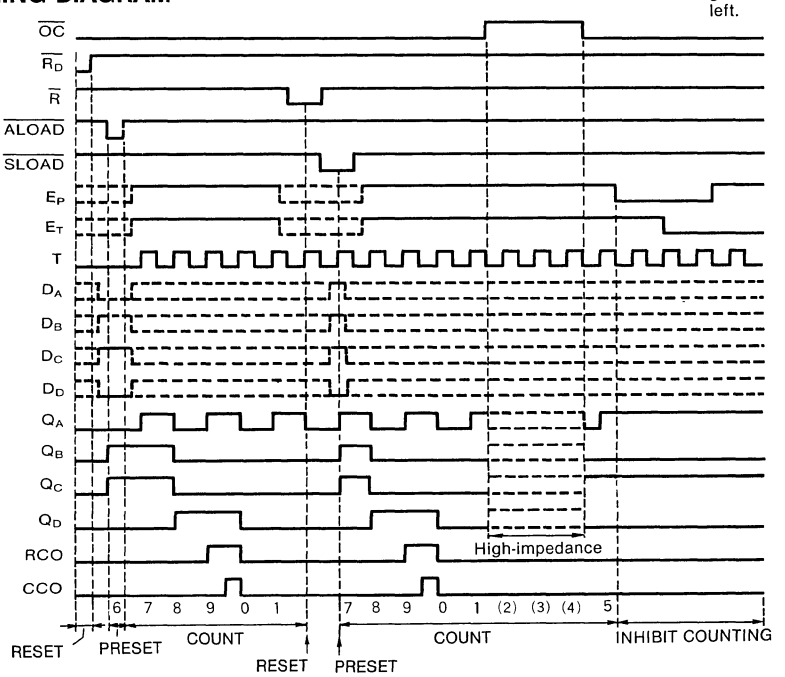
| Input | Outputs (internal signal) | | | | Output |
|---|---|---|---|---|---|
| $E_T$ | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | RCO |
| H | H | X | X | H | H |
| H | L | X | X | X | L |
| H | X | X | X | L | L |
| L | X | X | X | X | L |

### CCO FUNCTION TABLE (Note 2)

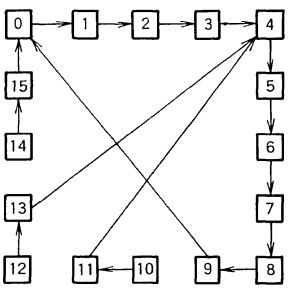
| Inputs | | | | Output |
|---|---|---|---|---|
| $E_T$ | $E_P$ | RCO* | T | CCO |
| L | X | X | X | L |
| X | L | X | X | L |
| X | X | L | X | L |
| H | H | H | ⊓ | ⊓ |

Note 2: *. RCO is an output, but also an internal signal generated as shown in the function table on the left.

### TIMING DIAGRAM




### STATE DIAGRAM



## SYNCHRONOUS PRESETTABLE DECADE COUNTER WITH 3-STATE OUTPUT

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | | | −0.5~+7 | V |
| $V_O$ | Output voltage | $Q_A$~$Q_D$ | High-level state or high-impedance state | −0.5~+5.5 | V |
| | | RCO, CCO | High-level state | −0.5~$V_{CC}$ | |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | °C |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | $Q_A$~$Q_D$ | 0 | | −2.6 | mA |
| | | RCO, CCO | 0 | | −0.4 | |
| $I_{OL}$ | Low-level output current | $Q_A$~$Q_D$ | 0 | | 24 | mA |
| | | RCO, CCO | 0 | | 8 | |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 | | +75 | °C |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $Q_A$~$Q_D$ | $V_{CC}$=4.5V | $I_{OH}$=−2.6mA | 2.4 | 3.2 | | V |
| | | RCO, CCO | | $I_{OH}$=−0.4mA, $T_a$=0~70°C | 2.7 | 3.4 | | |
| | | | | $I_{OH}$=−0.4mA, $T_a$=−20~+75°C | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $Q_A$~$Q_D$ | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| | | RCO, CCO | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $E_T$, $E_P$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.2 | mA |
| | | Other inputs | | | | | 0.1 | |
| $I_{IH}$ | High-level input current | $E_T$, $E_P$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 40 | μA |
| | | Other inputs | | | | | 20 | |
| $I_{IL}$ | Low-level input current | | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | $Q_A$~$Q_D$ | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| | | RCO, CCO | | | −15 | | −70 | |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 17 | 27 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 21 | 33 | mA |
| $I_{CCZ}$ | Supply current, outputs disabled | | $V_{CC}$=5.5V | | | 22 | 36 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

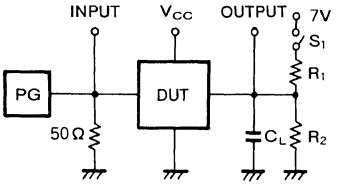
## SYNCHRONOUS PRESETTABLE DECADE COUNTER WITH 3-STATE OUTPUT

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 3), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70°C Min | $T_a$=0~70°C Typ * | $T_a$=0~70°C Max | $T_a$=−20~+75°C Min | $T_a$=−20~+75°C Typ * | $T_a$=−20~+75°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | T | $Q_A$~$Q_D$ | 20 | | | 18 | | | MHz |
| $t_{PLH}$ | Propagation time | T | $Q_A$~$Q_D$ | 4 | | 12 | 4 | | 13 | ns |
| $t_{PHL}$ | | | | 5 | | 18 | 5 | | 19 | |
| $t_{PLH}$ | | T | RCO | 9 | | 29 | 9 | | 30 | ns |
| $t_{PHL}$ | | | | 8 | | 24 | 8 | | 25 | |
| $t_{PLH}$ | | T | CCO | 8 | | 26 | 8 | | 27 | ns |
| $t_{PHL}$ | | | | 5 | | 16 | 5 | | 17 | |
| $t_{PLH}$ | Propagation time | $\overline{ALOAD}$ | $Q_A$~$Q_D$ | 10 | | 35 | 10 | | 36 | ns |
| $t_{PHL}$ | | | | 7 | | 23 | 7 | | 24 | |
| $t_{PLH}$ | | $\overline{ALOAD}$ | RCO | 15 | | 40 | 15 | | 41 | ns |
| $t_{PHL}$ | | | | 12 | | 30 | 12 | | 31 | |
| $t_{PLH}$ | | $\overline{ALOAD}$ | CCO | 25 | | 55 | 25 | | 56 | ns |
| $t_{PHL}$ | | | | 12 | | 33 | 12 | | 34 | |
| $t_{PLH}$ | Propagation time | $D_A$~$D_D$ | $Q_A$~$Q_D$ | 8 | | 30 | 8 | | 31 | ns |
| $t_{PHL}$ | | | | 7 | | 22 | 7 | | 23 | |
| $t_{PLH}$ | | $E_T$ | RCO | 5 | | 16 | 5 | | 17 | ns |
| $t_{PHL}$ | | | | 4 | | 14 | 4 | | 15 | |
| $t_{PLH}$ | | $E_T$ | CCO | 12 | | 32 | 12 | | 33 | ns |
| $t_{PHL}$ | | | | 4 | | 12 | 4 | | 13 | |
| $t_{PLH}$ | | $E_P$ | CCO | 5 | | 18 | 5 | | 19 | ns |
| $t_{PHL}$ | | | | 4 | | 12 | 4 | | 13 | |
| $t_{PHL}$ | | $\overline{R_D}$ | $Q_A$~$Q_D$ | 7 | | 22 | 7 | | 23 | ns |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | $Q_A$~$Q_D$ | 5 | | 19 | 5 | | 20 | ns |
| $t_{PZL}$ | | | | 8 | | 23 | 8 | | 24 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | $Q_A$~$Q_D$ | 2 | | 10 | 2 | | 11 | ns |
| $t_{PLZ}$ | | | | 4 | | 15 | 4 | | 16 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 3: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

## SYNCHRONOUS PRESETTABLE DECADE COUNTER WITH 3-STATE OUTPUT

### TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

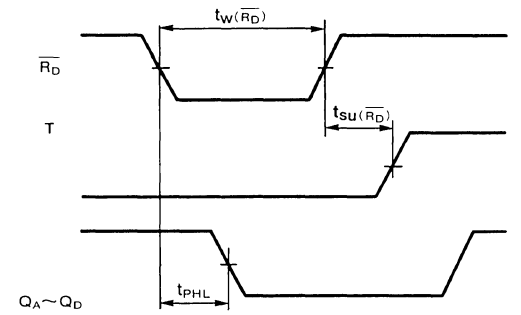
| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{w(TH)}$ | Pulse width | T "H" | 25 | | | 26 | | | ns |
| $t_{w(TL)}$ | | T "L" | 25 | | | 26 | | | |
| $t_{w(\overline{R_D})}$ | | $\overline{R_D}$ "L" | 15 | | | 16 | | | |
| $t_{w(\overline{ALOAD})}$ | | $\overline{ALOAD}$ "L" | 15 | | | 16 | | | |
| $t_{su(D)}$ | Setup time before T ↑ | $D_A$~$D_D$ | 20 | | | 21 | | | ns |
| $t_{su(\overline{SLOADL})}$ | | $\overline{SLOAD}$ "L" | 15 | | | 16 | | | |
| $t_{su(\overline{SLOADH})}$ | | $\overline{SLOAD}$ "H" (inactive) | 30 | | | 31 | | | |
| $t_{su(EH)}$ | | $E_T$, $E_P$ "H" | 20 | | | 21 | | | |
| $t_{su(EL)}$ | | $E_T$, $E_P$ "L" | 20 | | | 21 | | | |
| $t_{su(\overline{RL})}$ | | $\overline{R}$ "L" | 15 | | | 16 | | | |
| $t_{su(\overline{RH})}$ | | $\overline{R}$ "H" (inactive) | 30 | | | 31 | | | |
| $t_{su(\overline{R_D})}$ | | $\overline{R_D}$ "H" (inactive) | 10 | | | 11 | | | |
| $t_{su(\overline{ALOAD})}$ | | $\overline{ALOAD}$ "H" (inactive) | 10 | | | 11 | | | |
| $t_{h(D)}$ | Hold time after T ↑ | $D_A$~$D_D$ | 0 | | | 1 | | | ns |
| $t_{h(\overline{SLOAD})}$ | | $\overline{SLOAD}$ "L" | 0 | | | 1 | | | |
| $t_{h(\overline{R})}$ | | $\overline{R}$ "L" | 0 | | | 1 | | | |
| $t_{h(E)}$ | | $E_T$, $E_P$ | 0 | | | 1 | | | |

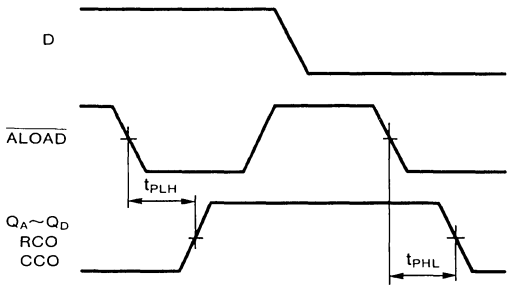
*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

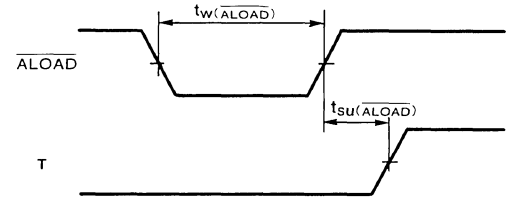
↑: Transition from low to high

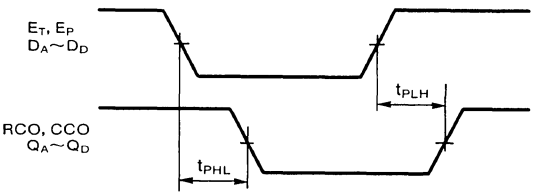
## SYNCHRONOUS PRESETTABLE DECADE COUNTER WITH 3-STATE OUTPUT

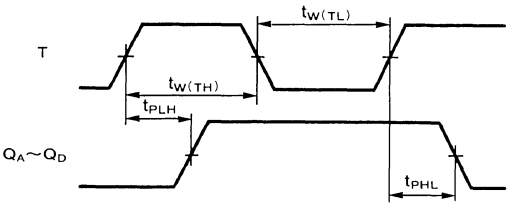
### TIMING DIAGRAM (Reference level = 1.3V)

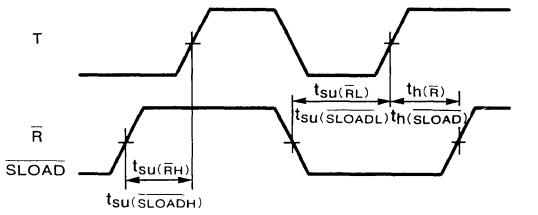


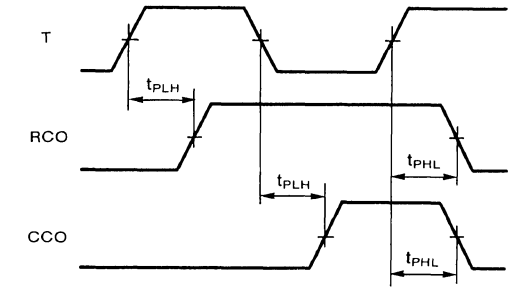



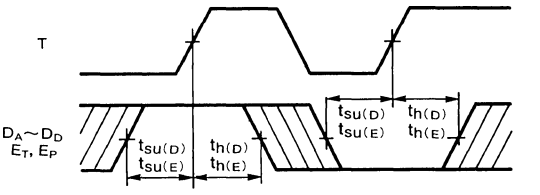



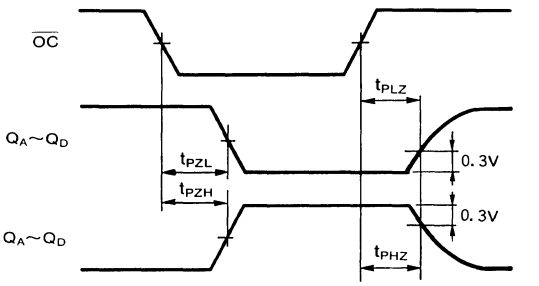




Note 4: The shaded areas indicate the period when the input is permitted to change for predictable output performance.



# M74ALS561AP

## SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH 3-STATE OUTPUT

## DESCRIPTION

The M74ALS561AP is a semiconductor integrated circuit of a synchronous 4-bit binary (hexadecimal) counter with 3-state outputs which has direct/synchronous reset and direct/synchronous preset inputs.

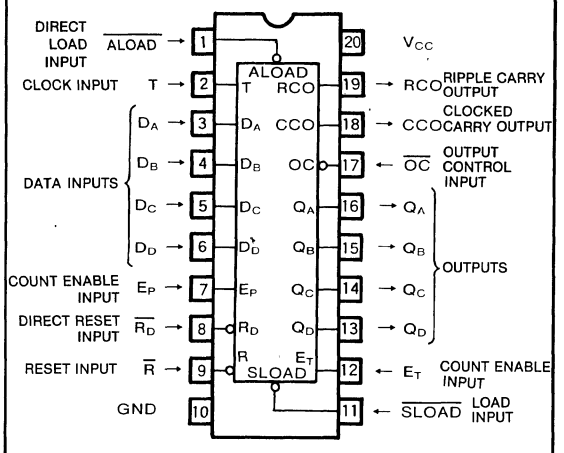
## FEATURES

- High fan-out ($Q_A \sim Q_D$: $I_{OL} = 24mA$, $I_{OH} = -2.6mA$)
- Direct and synchronous reset inputs
- Direct and synchronous load inputs
- Output control input ($\overline{OC}$)
- Enable inputs and carry outputs for cascade connection
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

## FUNCTIONAL DESCRIPTION

When the count pulse is applied to clock input T and enable inputs $E_P$ and $E_T$, reset inputs $\overline{R_D}$ and $\overline{R}$, and load inputs $\overline{ALOAD}$ and $\overline{SLOAD}$ are all high, the number of count pulses appears in 4-bit binary code on the outputs $Q_A \sim Q_D$ synchronized with the count pulse. Counting occurs when T changes from low to high.

When direct load input $\overline{ALOAD}$ is set low, asynchronous preset occurs and the signals applied to data inputs $D_A \sim D_D$ appear on outputs $Q_A \sim Q_D$. When load input $\overline{SLOAD}$ is set low and T changes from low to high, synchronous preset occurs and the signals on $D_A \sim D_D$ appear on $Q_A \sim Q_D$. The status of $E_P$ and $E_T$ does not affect preset operation.

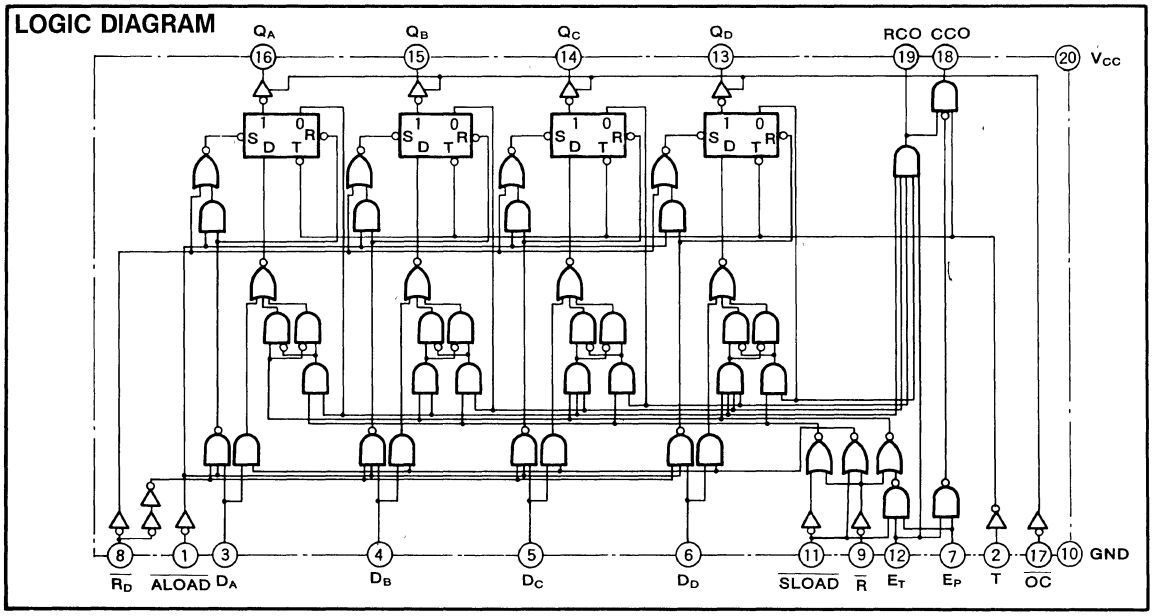
When direct reset $\overline{R_D}$ is set low, irrespective of other inputs, asynchronous reset occurs and $Q_A \sim Q_D$, RCO and CCO become low. When reset $\overline{R}$ is low and T changes from low to high, reset operation occurs synchronously and $Q_A \sim Q_D$, RCO and CCO become low.

When output control input $\overline{OC}$ is set high, outputs $Q_A \sim Q_D$ are in the high-impedance state. Even in this case, operations such as counting, preset and reset are possible.

Carry output RCO is high when $E_T$ and $Q_A \sim Q_D$ are high. Carry output CCO becomes high only when RCO, $E_P$ and $E_T$ are high and T is low. CCO is free from the glitches due to the propagation time dispersion in the internal gates.

$E_P$, $E_T$, RCO and CCO are used when counters are

## LOGIC DIAGRAM






MITSUBISHI ELECTRIC

## SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH 3-STATE OUTPUT

connected in synchronous cascade connection and made an n-bit counter. Usually, either RCO or CCO may be connected to $E_T$ of the next device. However, use RCO for high-speed operation. Since CCO changes after T is set low, CCO cannot follow high-speed counting.

### FUNCTION TABLE (Note 1)

| Operational mode | Inputs | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{OC}$# | $\overline{R_D}$ | $\overline{ALOAD}$ | $\overline{R}$ | $\overline{SLOAD}$ | $E_T$ | $E_P$ | T | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| Output "Z" ($Q_A$~$Q_D$) | H | X | X | X | X | X | X | X | Z | Z | Z | Z |
| Direct reset | L | L | X | X | X | X | X | X | L | L | L | L |
| Direct load | L | H | L | X | X | X | X | X | $D_A$ | $D_B$ | $D_C$ | $D_D$ |
| Synchronous reset | L | H | H | L | X | X | X | ↑ | L | L | L | L |
| Synchronous load | L | H | H | H | L | X | X | ↑ | $D_A$ | $D_B$ | $D_C$ | $D_D$ |
| Count | L | H | H | H | H | H | H | ↑ | Count (hexadecimal) | | | |
| Inhibit counting | L | H | H | H | H | L | X | X | $Q_A^0$ | $Q_B^0$ | $Q_C^0$ | $Q_D^0$ |
| | L | H | H | H | H | X | L | X | $Q_A^0$ | $Q_B^0$ | $Q_C^0$ | $Q_D^0$ |

Note 1: X : Irrelevant
Z : High-impedance state
↑ : Transition from low to high (positive edge trigger)
$Q_A^0$ ~ $Q_D^0$ : Level of $Q_A$ ~ $Q_D$ before the indicated steady-state input conditions were established.
# : The setting of input $\overline{OC}$ does not affect the operation of reset, load, count and count inhibit. However, data appear at $Q_A$ ~ $Q_D$ only when $\overline{OC}$ is low.

### RCO FUNCTION TABLE

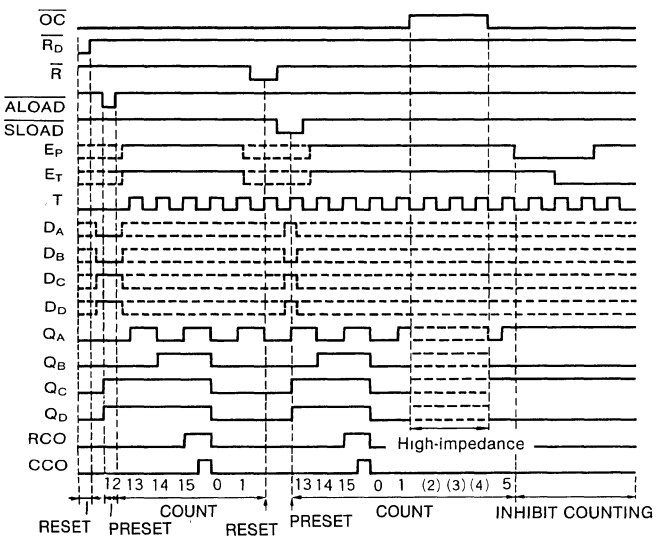
| Input | Outputs (internal signal) | | | | Output |
|---|---|---|---|---|---|
| $E_T$ | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | RCO |
| H | H | H | H | H | H |
| H | L | X | X | X | L |
| H | X | L | X | X | L |
| H | X | X | L | X | L |
| H | X | X | X | L | L |
| L | X | X | X | X | L |

### CCO FUNCTION TABLE (Note 2)

| Inputs | | | | Output |
|---|---|---|---|---|
| $E_T$ | $E_P$ | RCO* | T | CCO |
| L | X | X | X | L |
| X | L | X | X | L |
| X | X | L | X | L |
| H | H | H | ⊓ | ⊔ |

Note 2: *: RCO is an output, but also an internal signal generated as shown in the function table on the left.

### TIMING DIAGRAM



# SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH 3-STATE OUTPUT

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | | | −0.5~+7 | V |
| $V_O$ | Output voltage | $Q_A$~$Q_D$ | High-level state or high-impedance state | −0.5~+5.5 | V |
| | | RCO, CCO | High-level state | −0.5~$V_{CC}$ | |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | $Q_A$~$Q_D$ | 0 | | −2.6 | mA |
| | | RCO, CCO | 0 | | −0.4 | |
| $I_{OL}$ | Low-level output current | $Q_A$~$Q_D$ | 0 | | 24 | mA |
| | | RCO, CCO | 0 | | 8 | |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $Q_A$~$Q_D$ | $V_{CC}$=4.5V | $I_{OH}$=−2.6mA | 2.4 | 3.2 | | V |
| | | RCO, CCO | | $I_{OH}$=−0.4mA, $T_a$=0~70℃ | 2.7 | 3.4 | | |
| | | | | $I_{OH}$=−0.4mA, $T_a$=−20~+75℃ | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $Q_A$~$Q_D$ | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| | | RCO, CCO | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $E_T$, $E_P$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.2 | mA |
| | | Other inputs | | | | | 0.1 | |
| $I_{IH}$ | High-level input current | $E_T$, $E_P$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 40 | μA |
| | | Other inputs | | | | | 20 | |
| $I_{IL}$ | Low-level input current | | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | $Q_A$~$Q_D$ | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| | | RCO, CCO | | | −15 | | −70 | |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 17 | 27 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 21 | 33 | mA |
| $I_{CCZ}$ | Supply current, outputs disabled | | $V_{CC}$=5.5V | | | 22 | 36 | mA |

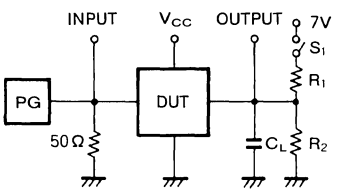
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 3), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | $T_a$=0~70℃ Typ * | $T_a$=0~70℃ Max | $T_a$=−20~+75℃ Min | $T_a$=−20~+75℃ Typ * | $T_a$=−20~+75℃ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | T | $Q_A$~$Q_D$ | 30 | | | 28 | | | MHz |
| $t_{PLH}$ | Propagation time | T | $Q_A$~$Q_D$ | 4 | | 12 | 4 | | 13 | ns |
| $t_{PHL}$ | | | | 5 | | 18 | 5 | | 19 | |
| $t_{PLH}$ | | T | RCO | 9 | | 29 | 9 | | 30 | ns |
| $t_{PHL}$ | | | | 8 | | 24 | 8 | | 25 | |
| $t_{PLH}$ | | T | CCO | 8 | | 26 | 8 | | 27 | ns |
| $t_{PHL}$ | | | | 5 | | 16 | 5 | | 17 | |
| $t_{PLH}$ | Propagation time | $\overline{ALOAD}$ | $Q_A$~$Q_D$ | 10 | | 35 | 10 | | 36 | ns |
| $t_{PHL}$ | | | | 7 | | 23 | 7 | | 24 | |
| $t_{PLH}$ | | $\overline{ALOAD}$ | RCO | 15 | | 40 | 15 | | 41 | ns |
| $t_{PHL}$ | | | | 12 | | 30 | 12 | | 31 | |
| $t_{PLH}$ | | $\overline{ALOAD}$ | CCO | 25 | | 55 | 25 | | 56 | ns |
| $t_{PHL}$ | | | | 12 | | 33 | 12 | | 34 | |
| $t_{PLH}$ | Propagation time | $D_A$~$D_D$ | $Q_A$~$Q_D$ | 8 | | 30 | 8 | | 31 | ns |
| $t_{PHL}$ | | | | 7 | | 22 | 7 | | 23 | |
| $t_{PLH}$ | | $E_T$ | RCO | 5 | | 16 | 5 | | 17 | ns |
| $t_{PHL}$ | | | | 4 | | 14 | 4 | | 15 | |
| $t_{PLH}$ | | $E_T$ | CCO | 12 | | 32 | 12 | | 33 | ns |
| $t_{PHL}$ | | | | 4 | | 12 | 4 | | 13 | |
| $t_{PLH}$ | | $E_P$ | CCO | 5 | | 18 | 5 | | 19 | ns |
| $t_{PHL}$ | | | | 4 | | 12 | 4 | | 13 | |
| $t_{PHL}$ | | $\overline{R_D}$ | $Q_A$~$Q_D$ | 7 | | 22 | 7 | | 23 | ns |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | $Q_A$~$Q_D$ | 5 | | 19 | 5 | | 20 | ns |
| $t_{PZL}$ | | | | 8 | | 23 | 8 | | 24 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | $Q_A$~$Q_D$ | 2 | | 10 | 2 | | 11 | ns |
| $t_{PLZ}$ | | | | 4 | | 15 | 4 | | 16 | |

*. All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 3: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

## SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH 3-STATE OUTPUT

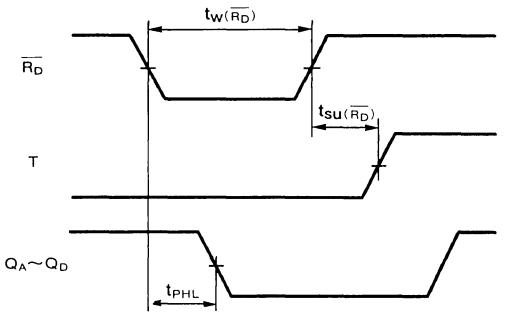
### TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

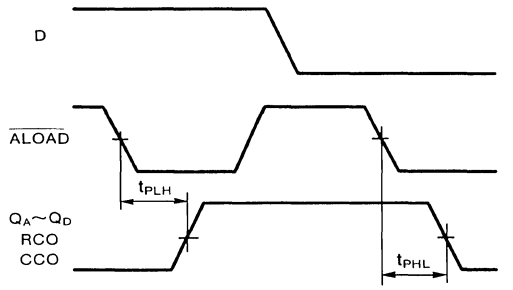
| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{w(TH)}$ | Pulse width | T "H" | 16.5 | | | 17.5 | | | ns |
| $t_{w(TL)}$ | | T "L" | 16.5 | | | 17.5 | | | |
| $t_{w(\overline{R_D})}$ | | $\overline{R_D}$ "L" | 15 | | | 16 | | | |
| $t_{w(\overline{ALOAD})}$ | | $\overline{ALOAD}$ "L" | 15 | | | 16 | | | |
| $t_{su(D)}$ | Setup time before T ↑ | $D_A$~$D_D$ | 20 | | | 21 | | | ns |
| $t_{su(\overline{SLOADL})}$ | | $\overline{SLOAD}$ "L" | 15 | | | 16 | | | |
| $t_{su(\overline{SLOADH})}$ | | $\overline{SLOAD}$ "H" (inactive) | 30 | | | 31 | | | |
| $t_{su(EH)}$ | | $E_T$, $E_P$ "H" | 20 | | | 21 | | | |
| $t_{su(EL)}$ | | $E_T$, $E_P$ "L" | 20 | | | 21 | | | |
| $t_{su(\overline{RL})}$ | | $\overline{R}$ "L" | 15 | | | 16 | | | |
| $t_{su(\overline{RH})}$ | | $\overline{R}$ "H" (inactive) | 30 | | | 31 | | | |
| $t_{su(\overline{R_D})}$ | | $\overline{R_D}$ "H" (inactive) | 10 | | | 11 | | | |
| $t_{su(\overline{ALOAD})}$ | | $\overline{ALOAD}$ "H" (inactive) | 10 | | | 11 | | | |
| $t_{h(D)}$ | Hold time after T ↑ | $D_A$~$D_D$ | 0 | | | 1 | | | ns |
| $t_{h(\overline{SLOAD})}$ | | $\overline{SLOAD}$ "L" | 0 | | | 1 | | | |
| $t_{h(\overline{R})}$ | | $\overline{R}$ "L" | 0 | | | 1 | | | |
| $t_{h(E)}$ | | $E_T$, $E_P$ | 0 | | | 1 | | | |

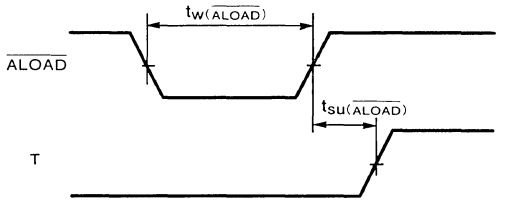
*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

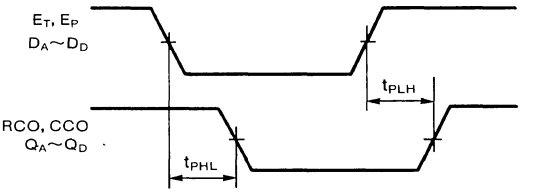
↑: Transition from low to high

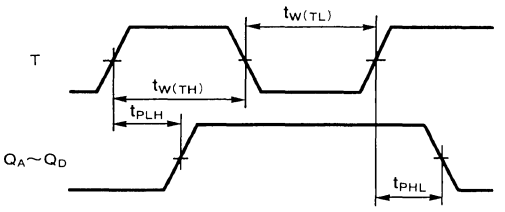
## TIMING DIAGRAM (Reference level = 1.3V)

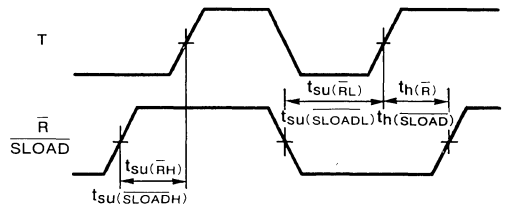


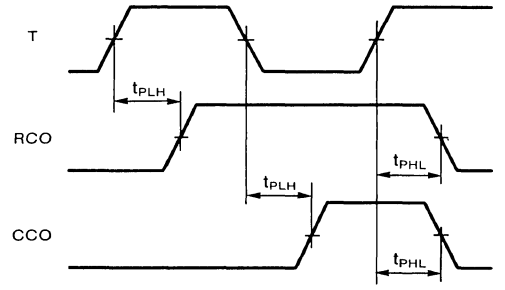



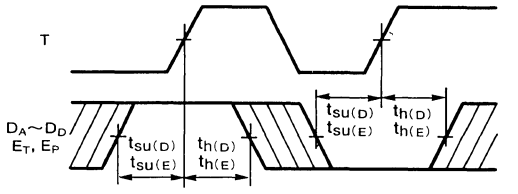



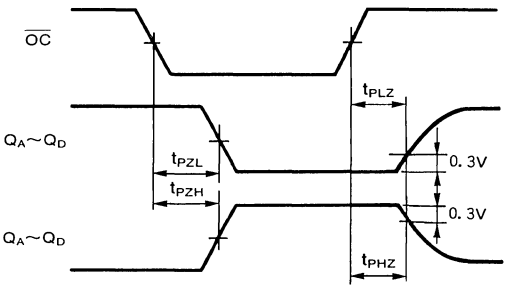




Note 4: The shaded areas indicate the period when the input is permitted to change for predictable output performance.



# M74ALS563P

## OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS563P is a semiconductor integrated circuit consisting of eight D-type latch circuits with 3-state inverted output and is provided with an output control input and an enable input, both common to all circuits.

## FEATURES

- 3-state, high fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High package density with eight circuits in one package
- Output control and enable inputs common to all eight circuits
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

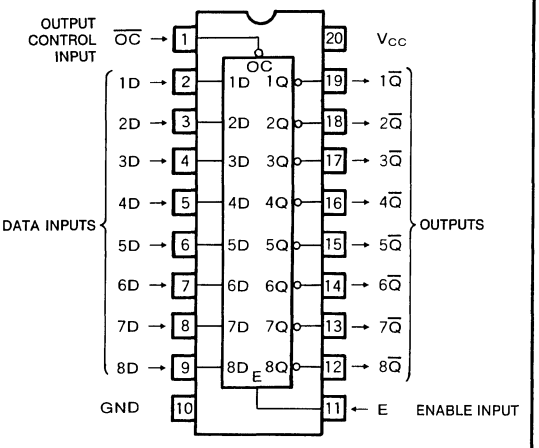
General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

The eight D-type latch circuits have the common output control $\overline{OC}$ and enable input E. While E is high, the information from D appears inverted at the output $\overline{Q}$ and $\overline{Q}$ changes with D. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of $\overline{Q}$ is retained even if D changes.

While $\overline{OC}$ is high, $1\overline{Q}$~$8\overline{Q}$ are in the high-impedance state "Z" irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While $\overline{Q}$ is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

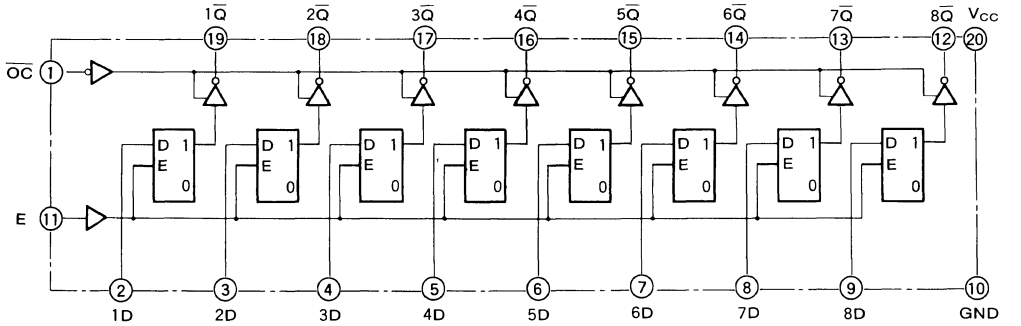
## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

Except for type name, the M74ALS563P is identical in all respects, including pin configuration, functions, and specifications, to M74ALS580P.

## LOGIC DIAGRAM






MITSUBISHI ELECTRIC

# OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (INVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | | Output |
|---|---|---|---|
| $\overline{OC}$* | E | D | $\overline{Q}$ |
| L | H | H | L |
| L | H | L | H |
| L | L | X | $\overline{Q}^0$ |
| H | X | X | Z |

Note 1: $\overline{Q}^0$ Level of $\overline{Q}$ before the indicated steady-state input conditions were established.

Z : High-impedance state

X Irrelevant

* Data can be latched irrespective of $\overline{OC}$.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 10 | 19 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 15 | 24 | mA |
| $I_{CCZ}$ | Supply current, outputs disabled | $V_{CC}$=5.5V | | | 16 | 27 | mA |

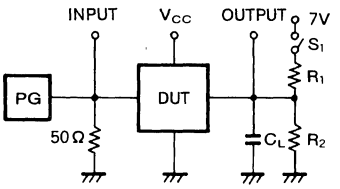
* All typical values are at $V_{CC}$=5V, $T_a$=25°C

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | 1D~8D | $1\overline{Q}$~$8\overline{Q}$ | 3 | | 18 | 3 | | 19 | ns |
| $t_{PHL}$ | | | | 3 | | 14 | 3 | | 15 | |
| $t_{PLH}$ | | E | $1\overline{Q}$~$8\overline{Q}$ | 8 | | 22 | 8 | | 23 | ns |
| $t_{PHL}$ | | | | 8 | | 21 | 8 | | 22 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | $1\overline{Q}$~$8\overline{Q}$ | 4 | | 20 | 4 | | 21 | ns |
| $t_{PZL}$ | | | | 4 | | 18 | 4 | | 19 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | $1\overline{Q}$~$8\overline{Q}$ | 2 | | 8 | 2 | | 9 | ns |
| $t_{PLZ}$ | | | | 3 | | 13 | 3 | | 14 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

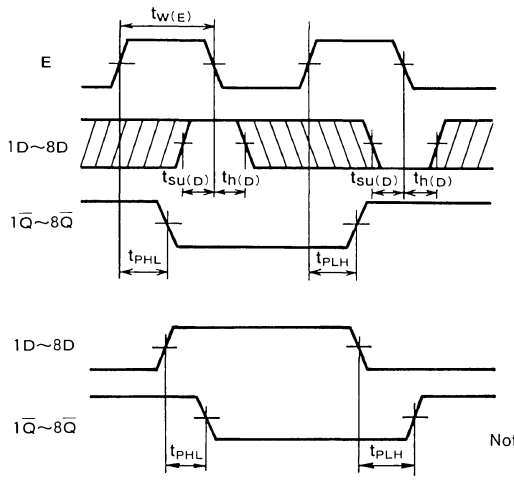
## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

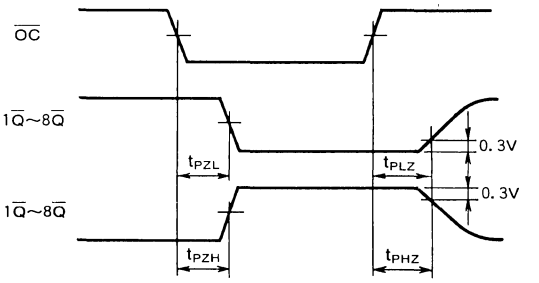
| Symbol | Parameter | | Limits: $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{w(E)}$ | Pulse width | E "H" | 15 | | | 16 | | | ns |
| $t_{su(D)}$ | Setup time before E↓ | 1D~8D | 10 | | | 11 | | | ns |
| $t_{h(D)}$ | Hold time after E↓ | 1D~8D | 10 | | | 11 | | | ns |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↓: Transition from high to low

## TIMING DIAGRAM (Reference level = 1.3V)




Note 3: The shaded areas indicate the period when the input is permitted to change for predictable out put performance.

# M74ALS564P

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS564P is a semiconductor integrated circuit consisting of eight D-type positive edge-triggered flip-flop circuits with 3-state inverted output and is provided with an output control input and a clock input, both common to all circuits.

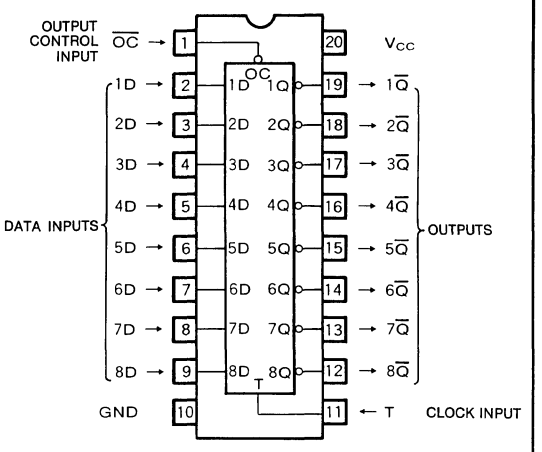
## FEATURES

- Positive edge triggering
- 3-state, high fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High package density with eight circuits in one package
- Output control and clock inputs common to all eight circuits
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

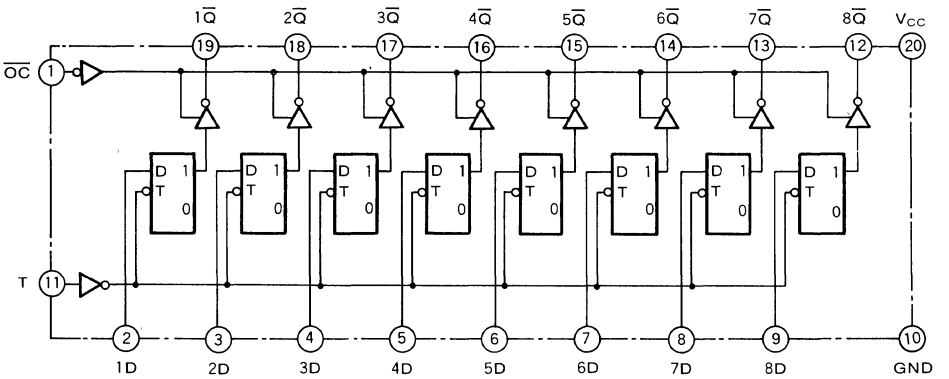
## FUNCTIONAL DESCRIPTION

The eight D-type edge-triggered flip-flop circuits have the commom output control $\overline{OC}$ and clock input T. When T changes from low to high, the status of D immediately before the change appears inverted at the output $\overline{Q}$ in accordance with the function table.

While $\overline{OC}$ is high, $1\overline{Q}$ ~ $8\overline{Q}$ are in the high-impedance state "Z" irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While $\overline{Q}$ is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

Except for type name, the M74ALS564P is identical in all respects, including pin configuration, functions, and specifications, to M74ALS576P.

## LOGIC DIAGRAM



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# OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT (INVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | | Output |
|---|---|---|---|
| $\overline{OC}$* | T | D | $\overline{Q}$ |
| L | ↑ | H | L |
| L | ↑ | L | H |
| L | L | X | $\overline{Q^0}$ |
| H | X | X | Z |

Note 1: ↑ : Transition from low to high (positive edge trigger)

$\overline{Q^0}$ : Level of $\overline{Q}$ before the indicated steady-state input conditions were established.

Z : High-impedance state

X : Irrelevant

* Data can be stored irrespective of $\overline{OC}$.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $I_{OH}$=−2.6mA | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 10 | 19 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 15 | 24 | mA |
| $I_{CCZ}$ | Supply current, outputs disabled | $V_{CC}$=5.5V | | | 16 | 27 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

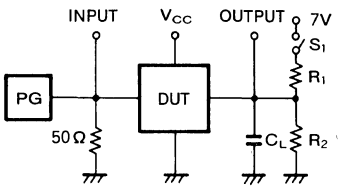
# OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT (INVERTED)

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | T | $1\overline{Q}$ ~ $8\overline{Q}$ | 30 | | | 28 | | | MHz |
| $t_{PLH}$ | Propagation time | T | $1\overline{Q}$~$8\overline{Q}$ | 4 | | 14 | 4 | | 15 | ns |
| $t_{PHL}$ | | | | 4 | | 14 | 4 | | 15 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | $1\overline{Q}$~$8\overline{Q}$ | 4 | | 20 | 4 | | 21 | ns |
| $t_{PZL}$ | | | | 4 | | 18 | 4 | | 19 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | $1\overline{Q}$~$8\overline{Q}$ | 2 | | 8 | 2 | | 9 | ns |
| $t_{PLZ}$ | | | | 3 | | 13 | 3 | | 14 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

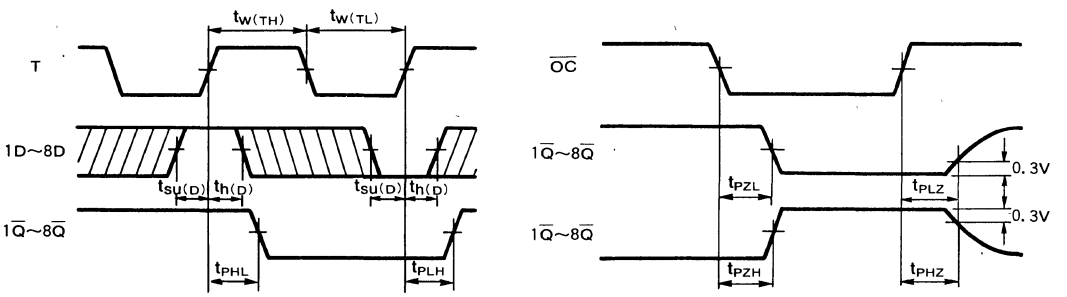
## TIMING REQUIREMENTS ($V_{CC}$=4.5~5.5V, $C_L$=50pF, $R_2$=500Ω)

| Symbol | Parameter | | Limits: $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{w(TH)}$ | Pulse width | T "H" | 14 | | | 15 | | | ns |
| $t_{w(TL)}$ | | T "L" | 14 | | | 15 | | | |
| $t_{su(D)}$ | Setup time before T↑ | 1D~8D | 15 | | | 16 | | | ns |
| $t_{h(D)}$ | Hold time after T↑ | 1D~8D | 0 | | | 1 | | | ns |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↑: Transition from low to high

## TIMING DIAGRAM (Reference level = 1.3V)




Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.



MITSUBISHI ELECTRIC

# M74ALS568AP

## SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH 3-STATE OUTPUT

## DESCRIPTION

The M74ALS568AP is a semiconductor integrated circuit of a synchronous up/down decade counter with 3-state outputs which has a direct reset, a synchronous reset and a preset input.

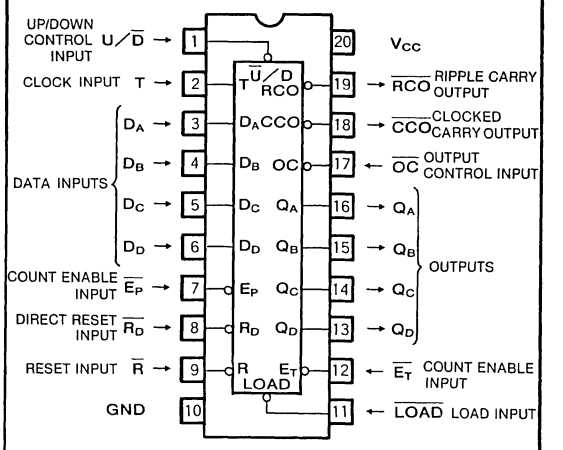
## FEATURES

- High fan-out ($Q_A \sim Q_D$: $I_{OL} = 24mA$, $I_{OH} = -2.6mA$)
- Direct and synchronous reset inputs
- Synchronous load input
- Up/down control inputs for up/down switching
- Output control input ($\overline{OC}$)
- Enable inputs and carry outputs for cascade connection
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

## FUNCTIONAL DESCRIPTION

If a count pulse is applied to clock input T when enable inputs $\overline{E_P}$ and $\overline{E_T}$ are set low and reset inputs $\overline{R_D}$, $\overline{R}$, and load input $\overline{LOAD}$ are high, the number of count pulses appears in BCD code on the outputs $Q_A$~$Q_D$ synchronized with the count pulse. This device counts up when up/down control input U/$\overline{D}$ is high and it counts down when U/$\overline{D}$ is low. Counting occurs when T changes from low to high.

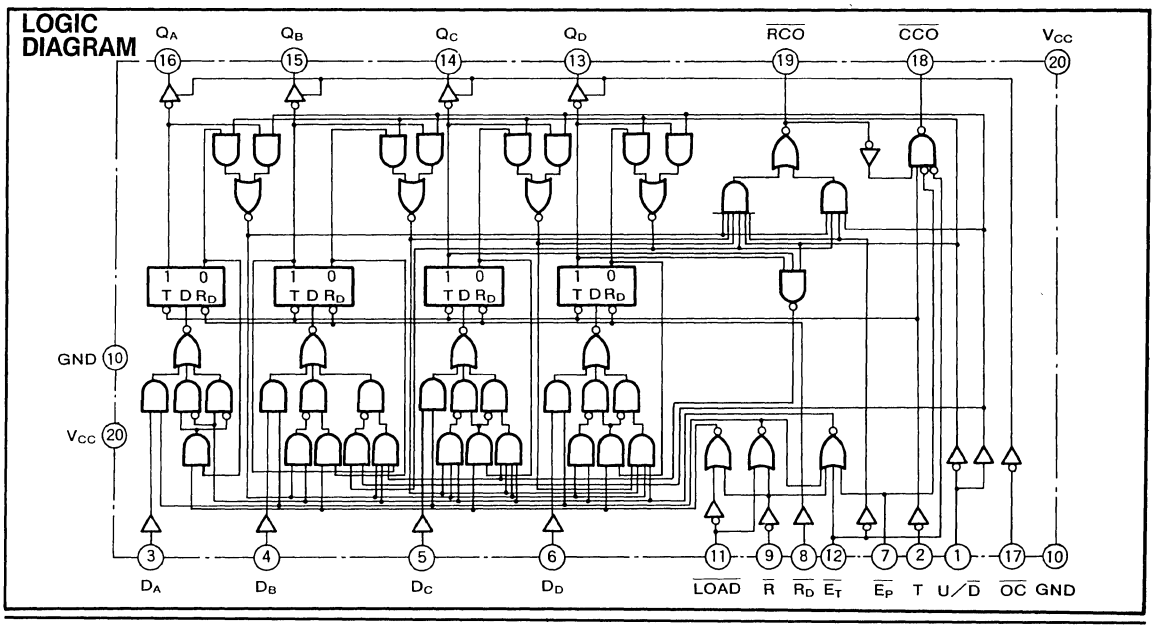
Preset occurs synchronously when data are applied to data inputs $D_A \sim D_D$, $\overline{LOAD}$ is set low, and T changes from low to high. When the counter is preset to a numerical value of 10 or more, the counting proceeds in accordance with the state diagram.

When direct reset $\overline{R_D}$ is set low, irrespective of other inputs, asynchronous reset occurs and $Q_A \sim Q_D$ become low. When reset $\overline{R}$ is set low and T changes from low to high, reset operation occurs synchronously and $Q_A \sim Q_D$ become low.

When output control input $\overline{OC}$ is set high, outputs $Q_A \sim Q_D$ are in high-impedance state. Even in this case, operations such as counting, preset and reset are possible.

Carry output $\overline{RCO}$ is low when $\overline{E_T}$ is low and both $Q_A$ and $Q_D$ are high in count up condition and when $\overline{E_T}$ and $Q_A \sim Q_D$ are low in count down condition. Carry output $\overline{CCO}$ becomes low when $\overline{RCO}$, $\overline{E_P}$, $\overline{E_T}$ and T are low. $\overline{CCO}$ is free from the glitches due to the propagation time dispersion in the internal gates.

## LOGIC DIAGRAM



## SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH 3-STATE OUTPUT

$\overline{E_P}$, $\overline{E_T}$, $\overline{RCO}$ and $\overline{CCO}$ are used when counters are connected in synchronous cascade connection and made a divide-by-$10^n$ counter. Usually, either $\overline{RCO}$ or $\overline{CCO}$ may be connected to $\overline{E_T}$ of the next device. However, use $\overline{RCO}$ for high-speed operation. Since $\overline{CCO}$ changes after T is set low, $\overline{CCO}$ cannot follow high-speed counting.

### FUNCTION TABLE (Note 1)

| Operational mode | Inputs | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{OC}$# | $\overline{R_D}$ | $\overline{R}$ | $\overline{LOAD}$ | $\overline{E_T}$ | $\overline{E_P}$ | U/$\overline{D}$ | T | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| Output "Z" ($Q_A$~$Q_D$) | H | X | X | X | X | X | X | X | Z | Z | Z | Z |
| Direct reset | L | L | X | X | X | X | X | X | L | L | L | L |
| Synchronous reset | L | H | L | X | X | X | X | ↑ | L | L | L | L |
| Synchronous load | L | H | H | L | X | X | X | ↑ | $D_A$ | $D_B$ | $D_C$ | $D_D$ |
| Count up | L | H | H | H | L | L | H | ↑ | Count up (decimal) | | | |
| Count down | L | H | H | H | L | L | L | ↑ | Count down (decimal) | | | |
| Inhibit counting | L | H | H | H | H | X | X | X | $Q_A^0$ | $Q_B^0$ | $Q_C^0$ | $Q_D^0$ |
| | L | H | H | H | X | H | X | X | $Q_A^0$ | $Q_B^0$ | $Q_C^0$ | $Q_D^0$ |

Note 1: X : Irrelevant

Z : High-impedance state

↑ : Transition from low to high (positive edge trigger)

$Q_A^0$ ~ $Q_D^0$ : Level of $Q_A$ ~ $Q_D$ before the indicated steady-state input conditions were established.

# : The setting of input $\overline{OC}$ does not affect the operation of reset, load, count, and count inhibit. However, data appear at $Q_A$ ~ $Q_D$ only when $\overline{OC}$ is low.

### $\overline{RCO}$ FUNCTION TABLE

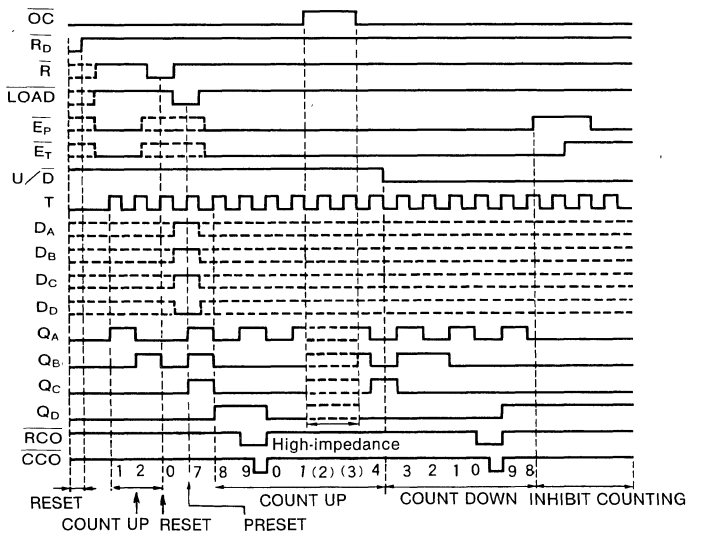
| Inputs | | Outputs (internal signal) | | | | Output |
|---|---|---|---|---|---|---|
| $\overline{E_T}$ | U/$\overline{D}$ | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $\overline{RCO}$ |
| H | X | X | X | X | X | H |
| L | H | H | X | X | H | L |
| L | H | L | X | X | X | H |
| L | H | X | X | X | L | H |
| L | L | L | L | L | L | L |
| L | L | H | X | X | X | H |
| L | L | X | H | X | X | H |
| L | L | X | X | H | X | H |
| L | L | X | X | X | H | H |

### $\overline{CCO}$ FUNCTION TABLE (Note 2)

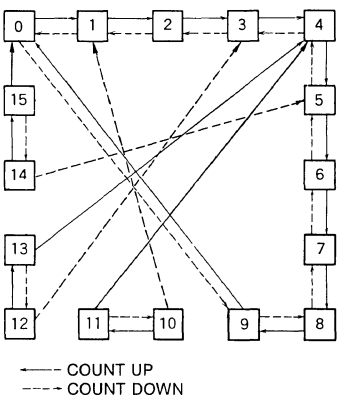
| Inputs | | | | Output |
|---|---|---|---|---|
| $\overline{E_T}$ | $\overline{E_P}$ | $\overline{RCO}$* | T | $\overline{CCO}$ |
| H | X | X | X | H |
| X | H | X | X | H |
| X | X | H | X | H |
| L | L | L | ⊓ | ⊓ |

Note 2:*. $\overline{RCO}$ is an output, but also an internal signal generated as shown in the function table on the left.

### TIMING DIAGRAM




### STATE DIAGRAM






MITSUBISHI ELECTRIC

## SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH 3-STATE OUTPUT

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | $Q_A$ ~ $Q_D$ | High-level state or high-impedance state | −0.5 ~ +5.5 | V |
| | | $\overline{RCO}$, $\overline{CCO}$ | High-level state | −0.5 ~ $V_{CC}$ | |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20 ~ +75 | °C |
| $T_{stg}$ | Storage temperature range | | | −65 ~ +150 | °C |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | $Q_A$ ~ $Q_D$ | 0 | | −2.6 | mA |
| | | $\overline{RCO}$, $\overline{CCO}$ | 0 | | −0.4 | |
| $I_{OL}$ | Low-level output current | $Q_A$ ~ $Q_D$ | 0 | | 24 | mA |
| | | $\overline{RCO}$, $\overline{CCO}$ | 0 | | 8 | |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 | | +75 | °C |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $Q_A$ ~ $Q_D$ | $V_{CC}$=4.5V | $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| | | $\overline{RCO}$, $\overline{CCO}$ | | $I_{OH}$= −0.4mA | $T_a$=0~70°C | 2.7 | 3.4 | | |
| | | | | | $T_a$=−20~+75°C | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $Q_A$ ~ $Q_D$ | $V_{CC}$=4.5V | $I_{OL}$=12mA | | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | | 0.35 | 0.5 | |
| | | $\overline{RCO}$, $\overline{CCO}$ | $V_{CC}$=4.5V | $I_{OL}$=4mA | | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=8mA | | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | | $V_{CC}$=5.5V, $V_O$=2.7V | | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | | $V_{CC}$=5.5V, $V_O$=0.4V | | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | | $V_{CC}$=5.5V, $V_I$=7V | | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | | $V_{CC}$=5.5V, $V_I$=2.7V | | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | | $V_{CC}$=5.5V, $V_I$=0.4V | | | | | −0.2 | mA |
| $I_O$ | Output current | $Q_A$ ~ $Q_D$ | $V_{CC}$=5.5V, $V_O$=2.25V | | | −30 | | −112 | mA |
| | | $\overline{RCO}$, $\overline{CCO}$ | | | | −15 | | −70 | |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | | 16 | 26 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | | 20 | 32 | mA |
| $I_{CCZ}$ | Supply current, outputs disabled | | $V_{CC}$=5.5V | | | | 20 | 32 | mA |

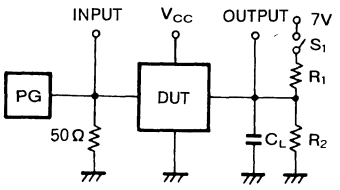
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 3), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | $T_a$=0~70℃ Typ * | $T_a$=0~70℃ Max | $T_a$=−20~+75℃ Min | $T_a$=−20~+75℃ Typ * | $T_a$=−20~+75℃ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | T | $Q_A$~$Q_D$ | 20 | | | 18 | | | MHz |
| $t_{PLH}$ | Propagation time | T | $Q_A$~$Q_D$ | 4 | | 13 | 4 | | 14 | ns |
| $t_{PHL}$ | | | | 7 | | 16 | 7 | | 17 | |
| $t_{PLH}$ | | T | $\overline{RCO}$ | 12 | | 28 | 12 | | 29 | ns |
| $t_{PHL}$ | | | | 10 | | 19 | 10 | | 20 | |
| $t_{PLH}$ | | T | $\overline{CCO}$ | 5 | | 13 | 5 | | 14 | ns |
| $t_{PHL}$ | | | | 6 | | 25 | 6 | | 26 | |
| $t_{PLH}$ | Propagation time | $\overline{E_P}$ | $\overline{CCO}$ | 4 | | 12 | 4 | | 13 | ns |
| $t_{PHL}$ | | | | 5 | | 14 | 5 | | 15 | |
| $t_{PLH}$ | | $\overline{E_T}$ | $\overline{RCO}$ | 6 | | 15 | 6 | | 16 | ns |
| $t_{PHL}$ | | | | 4 | | 13 | 4 | | 14 | |
| $t_{PLH}$ | | $\overline{E_T}$ | $\overline{CCO}$ | 5 | | 13 | 5 | | 14 | ns |
| $t_{PHL}$ | | | | 9 | | 23 | 9 | | 24 | |
| $t_{PLH}$ | Propagation time | U/$\overline{D}$ | $\overline{RCO}$ | 9 | | 23 | 9 | | 24 | ns |
| $t_{PHL}$ | | | | 9 | | 23 | 9 | | 24 | |
| $t_{PHL}$ | | $\overline{R_D}$ | $Q_A$~$Q_D$ | 9 | | 20 | 9 | | 21 | ns |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | $Q_A$~$Q_D$ | 6 | | 18 | 6 | | 19 | ns |
| $t_{PZL}$ | | | | 6 | | 24 | 6 | | 25 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | $Q_A$~$Q_D$ | 1 | | 10 | 1 | | 11 | ns |
| $t_{PLZ}$ | | | | 3 | | 13 | 3 | | 14 | |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 3: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

## SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH 3-STATE OUTPUT

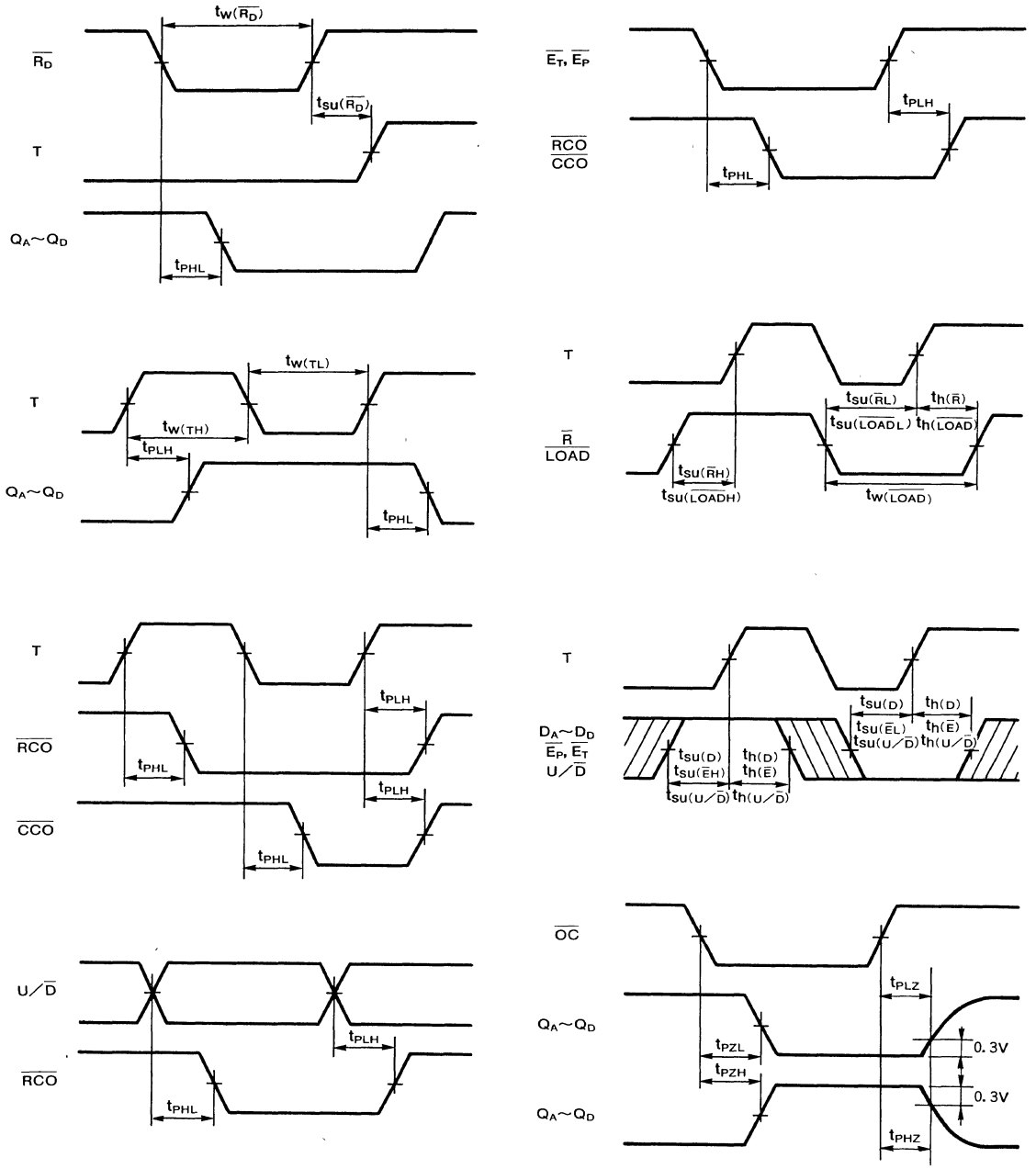
## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{w(TH)}$ | Pulse width | T "H" | 25 | | | 26 | | | ns |
| $t_{w(TL)}$ | | T "L" | 25 | | | 26 | | | |
| $t_{w(\overline{R_D})}$ | | $\overline{R_D}$ "L" | 15 | | | 16 | | | |
| $t_{w(\overline{LOAD})}$ | | $\overline{LOAD}$ "L" | 15 | | | 16 | | | |
| $t_{su(D)}$ | Setup time before T ↑ | $D_A$~$D_D$ | 20 | | | 21 | | | ns |
| $t_{su(\overline{LOADL})}$ | | $\overline{LOAD}$ "L" | 15 | | | 16 | | | |
| $t_{su(\overline{LOADH})}$ | | $\overline{LOAD}$ "H" (inactive) | 30 | | | 31 | | | |
| $t_{su(\overline{EH})}$ | | $\overline{E_T}$, $\overline{E_P}$ "H" | 30 | | | 31 | | | |
| $t_{su(\overline{EL})}$ | | $\overline{E_T}$, $\overline{E_P}$ "L" | 20 | | | 21 | | | |
| $t_{su(\overline{RL})}$ | | $\overline{R}$ "L" | 15 | | | 16 | | | |
| $t_{su(\overline{RH})}$ | | $\overline{R}$ "H" (inactive) | 30 | | | 31 | | | |
| $t_{su(\overline{R_D})}$ | | $\overline{R_D}$ "H" (inactive) | 10 | | | 11 | | | |
| $t_{su(U/\overline{D})}$ | | U/$\overline{D}$ | 30 | | | 31 | | | |
| $t_{h(D)}$ | Hold time after T ↑ | $D_A$~$D_D$ | 0 | | | 1 | | | ns |
| $t_{h(\overline{LOAD})}$ | | $\overline{LOAD}$ "L" | 0 | | | 1 | | | |
| $t_{h(\overline{R})}$ | | $\overline{R}$ "L" | 0 | | | 1 | | | |
| $t_{h(\overline{E})}$ | | $\overline{E_T}$, $\overline{E_P}$ | 0 | | | 1 | | | |
| $t_{h(U/\overline{D})}$ | | U/$\overline{D}$ | 0 | | | 1 | | | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↑ : Transition from low to high

## TIMING DIAGRAM (Reference level = 1.3V)




Note 4: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS569AP

## SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH 3-STATE OUTPUT

## DESCRIPTION

The M74ALS569AP is a semiconductor integrated circuit of a synchronous up/down 4-bit binary (hexadecimal) counter with 3-state outputs which has a direct reset, a synchronous reset and a present input.

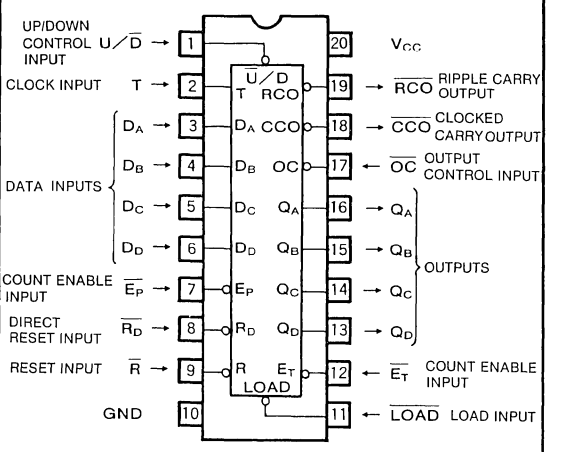
## FEATURES

- High fan-out ($Q_A \sim Q_D$: $I_{OL} = 24mA$, $I_{OH} = -2.6mA$)
- Direct and synchronous reset inputs
- Synchronous load input
- Up/down control inputs for up/down switching
- Output control input ($\overline{OC}$)
- Enable inputs and carry outputs for cascade connection
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

## FUNCTIONAL DESCRIPTION

If a count pulse is applied to clock input T when enable inputs $\overline{E_P}$ and $\overline{E_T}$ are set low and reset inputs $\overline{R_D}$, $\overline{R}$, and load input $\overline{LOAD}$ are high, the number of count pulses appears in 4-bit binary code on the outputs $Q_A \sim Q_D$ synchronized with the count pulse. This device counts up when up/down control input U/$\overline{D}$ is high and it counts down when U/$\overline{D}$ is low. Counting occurs when T changes from low to high.

Preset occurs synchronously when data are applied to data inputs $D_A \sim D_D$, $\overline{LOAD}$ is set low, and T changes from low to high.

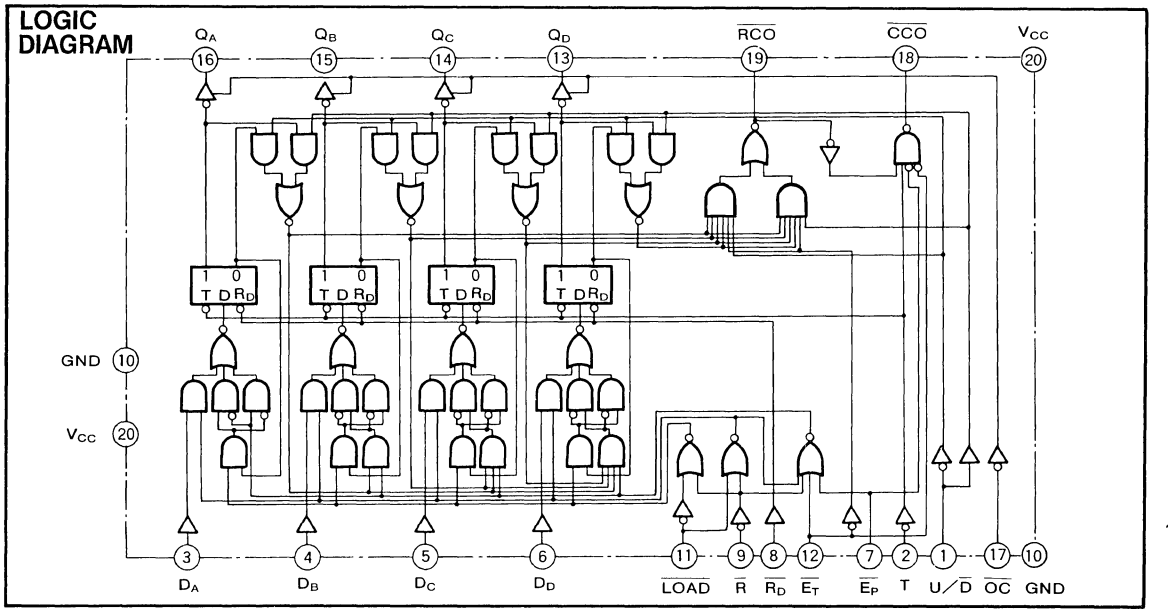
When direct reset $\overline{R_D}$ is set low, irrespective of other inputs, asynchronous reset occurs and $Q_A \sim Q_D$ become low. When reset $\overline{R}$ is set low and T changes from low to high, reset operation occurs synchronously and $Q_A \sim Q_D$ become low.

When output control input $\overline{OC}$ is set high, outputs $Q_A \sim Q_D$ are in high-impedance state. Even in this case, operations such as counting, preset and reset are possible.

Carry output $\overline{RCO}$ is low when $\overline{E_T}$ is low and $Q_A \sim Q_D$ are high in count up condition and when $\overline{E_T}$ and $Q_A \sim Q_D$ are low in count down condition. Carry output $\overline{CCO}$ becomes low when $\overline{RCO}$, $\overline{E_P}$, $\overline{E_T}$ and T are low. $\overline{CCO}$ is free from the glitches due to the propagation time dispersion in the internal gates.

$\overline{E_P}$, $\overline{E_T}$, $\overline{RCO}$ and $\overline{CCO}$ are used when counters are

## LOGIC DIAGRAM



## SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH 3-STATE OUTPUT

connected in synchronous cascade connection and made an n-bit counter. Usually, either $\overline{RCO}$ or $\overline{CCO}$ may be connected to $\overline{E_T}$ of the next device. However, use $\overline{RCO}$ for high-speed operation. Since $\overline{CCO}$ changes after T is set low, $\overline{CCO}$ cannot follow high-speed counting.

## FUNCTION TABLE (Note 1)

| Operational mode | Inputs | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{OC}$# | $\overline{R_D}$ | $\overline{R}$ | $\overline{LOAD}$ | $\overline{E_T}$ | $\overline{E_P}$ | U/$\overline{D}$ | T | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| Output "Z" ($Q_A \sim Q_D$) | H | X | X | X | X | X | X | X | Z | Z | Z | Z |
| Direct reset | L | L | X | X | X | X | X | X | L | L | L | L |
| Synchronous reset | L | H | L | X | X | X | X | ↑ | L | L | L | L |
| Synchronous load | L | H | H | L | X | X | X | ↑ | $D_A$ | $D_B$ | $D_C$ | $D_D$ |
| Count-up | L | H | H | H | L | L | H | ↑ | Count-up (hexadecimal) | | | |
| Count-down | L | H | H | H | L | L | L | ↑ | Count-down (hexadecimal) | | | |
| Inhibit counting | L | H | H | H | H | X | X | X | $Q_A^0$ | $Q_B^0$ | $Q_C^0$ | $Q_D^0$ |
| | L | H | H | H | X | H | X | X | $Q_A^0$ | $Q_B^0$ | $Q_C^0$ | $Q_D^0$ |

Note 1: X : Irrelevant  Z : High-impedance state  $Q_A^0 \sim Q_D^0$ : Level of $Q_A \sim Q_D$ before the indicated steady-state input conditions were established.

↑ : Transition from low to high (positive edge trigger)

# : The setting of input $\overline{OC}$ does not affect the operation of reset, load, count and count inhibit. However, data appear at $Q_A \sim Q_D$ only when $\overline{OC}$ is low.

## $\overline{RCO}$ FUNCTION TABLE

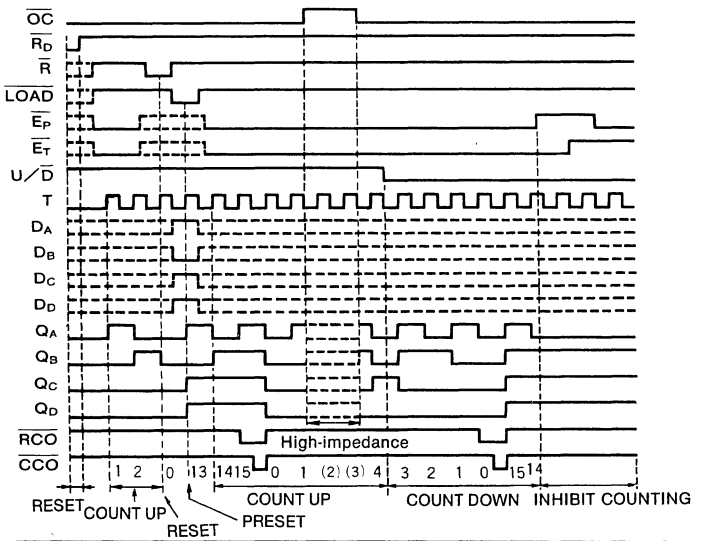
| Inputs | | Outputs (internal signal) | | | | Output |
|---|---|---|---|---|---|---|
| $\overline{E_T}$ | U/$\overline{D}$ | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $\overline{RCO}$ |
| H | X | X | X | X | X | H |
| L | H | H | H | H | H | L |
| L | H | L | X | X | X | H |
| L | H | X | L | X | X | H |
| L | H | X | X | L | X | H |
| L | H | X | X | X | L | H |
| L | L | L | L | L | L | L |
| L | L | H | X | X | X | H |
| L | L | X | H | X | X | H |
| L | L | X | X | H | X | H |
| L | L | X | X | X | H | H |

## $\overline{CCO}$ FUNCTION TABLE (Note 2)

| Inputs | | | | Output |
|---|---|---|---|---|
| $\overline{E_T}$ | $\overline{E_P}$ | $\overline{RCO}$* | T | $\overline{CCO}$ |
| H | X | X | X | H |
| X | H | X | X | H |
| X | X | H | X | H |
| L | L | L | ⊓ | ⊓ |

Note 2:*: $\overline{RCO}$ is an output, but also an internal signal generated as shown in the function table on the left.

## TIMING DIAGRAM






MITSUBISHI ELECTRIC

# SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH 3-STATE OUTPUT

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | | | −0.5~+7 | V |
| $V_O$ | Output voltage | $Q_A$~$Q_D$ | High-level state or high-impedance state | −0.5~+5.5 | V |
| | | $\overline{RCO}$, $\overline{CCO}$ | High-level state | −0.5~$V_{CC}$ | |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | $Q_A$~$Q_D$ | 0 | | −2.6 | mA |
| | | $\overline{RCO}$, $\overline{CCO}$ | 0 | | −0.4 | |
| $I_{OL}$ | Low-level output current | $Q_A$~$Q_D$ | 0 | | 24 | mA |
| | | $\overline{RCO}$, $\overline{CCO}$ | 0 | | 8 | |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 | | +75 | °C |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $Q_A$~$Q_D$ | $V_{CC}$=4.5V | $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| | | $\overline{RCO}$, $\overline{CCO}$ | | $I_{OH}$=−0.4mA | $T_a$=0~70°C | 2.7 | 3.4 | | |
| | | | | | $T_a$=−20~+75°C | 2.6 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | $Q_A$~$Q_D$ | $V_{CC}$=4.5V | $I_{OL}$=12mA | | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | | 0.35 | 0.5 | |
| | | $\overline{RCO}$, $\overline{CCO}$ | $V_{CC}$=4.5V | $I_{OL}$=4mA | | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=8mA | | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | | $V_{CC}$=5.5V, $V_O$=2.7V | | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | | $V_{CC}$=5.5V, $V_O$=0.4V | | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | | $V_{CC}$=5.5V, $V_I$=7V | | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | | $V_{CC}$=5.5V, $V_I$=2.7V | | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | | $V_{CC}$=5.5V, $V_I$=0.4V | | | | | −0.2 | mA |
| $I_O$ | Output current | $Q_A$~$Q_D$ | $V_{CC}$=5.5V, $V_O$=2.25V | | | −30 | | −112 | mA |
| | | $\overline{RCO}$, $\overline{CCO}$ | | | | −15 | | −70 | |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | | 16 | 26 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | | 20 | 32 | mA |
| $I_{CCZ}$ | Supply current, outputs disabled | | $V_{CC}$=5.5V | | | | 20 | 32 | mA |

* : All typical values are at $V_{CC}$=5V, $T_a$=25°C.

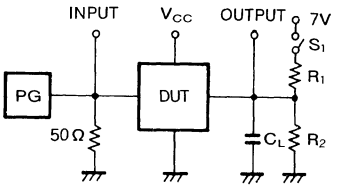
## SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH 3-STATE OUTPUT

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 3), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | $T_a$=0~70℃ Typ * | $T_a$=0~70℃ Max | $T_a$=−20~+75℃ Min | $T_a$=−20~+75℃ Typ * | $T_a$=−20~+75℃ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | T | $Q_A$~$Q_D$ | 30 | | | 28 | | | MHz |
| $t_{PLH}$ | Propagation time | T | $Q_A$~$Q_D$ | 4 | | 13 | 4 | | 14 | ns |
| $t_{PHL}$ | | | | 7 | | 16 | 7 | | 17 | |
| $t_{PLH}$ | | T | $\overline{RCO}$ | 12 | | 28 | 12 | | 29 | ns |
| $t_{PHL}$ | | | | 10 | | 19 | 10 | | 20 | |
| $t_{PLH}$ | | T | $\overline{CCO}$ | 5 | | 13 | 5 | | 14 | ns |
| $t_{PHL}$ | | | | 6 | | 25 | 6 | | 26 | |
| $t_{PLH}$ | Propagation time | $\overline{E_P}$ | $\overline{CCO}$ | 4 | | 12 | 4 | | 13 | ns |
| $t_{PHL}$ | | | | 5 | | 14 | 5 | | 15 | |
| $t_{PLH}$ | | $\overline{E_T}$ | $\overline{RCO}$ | 6 | | 15 | 6 | | 16 | ns |
| $t_{PHL}$ | | | | 4 | | 13 | 4 | | 14 | |
| $t_{PLH}$ | | $\overline{E_T}$ | $\overline{CCO}$ | 5 | | 13 | 5 | | 14 | ns |
| $t_{PHL}$ | | | | 9 | | 23 | 9 | | 24 | |
| $t_{PLH}$ | Propagation time | U/$\overline{D}$ | $\overline{RCO}$ | 9 | | 23 | 9 | | 24 | ns |
| $t_{PHL}$ | | | | 9 | | 23 | 9 | | 24 | |
| $t_{PHL}$ | | $\overline{R_D}$ | $Q_A$~$Q_D$ | 9 | | 20 | 9 | | 21 | ns |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | $Q_A$~$Q_D$ | 6 | | 18 | 6 | | 19 | ns |
| $t_{PZL}$ | | | | 6 | | 24 | 6 | | 25 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | $Q_A$~$Q_D$ | 1 | | 10 | 1 | | 11 | ns |
| $t_{PLZ}$ | | | | 3 | | 13 | 3 | | 14 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C

Note 3 Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

## SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH 3-STATE OUTPUT

## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

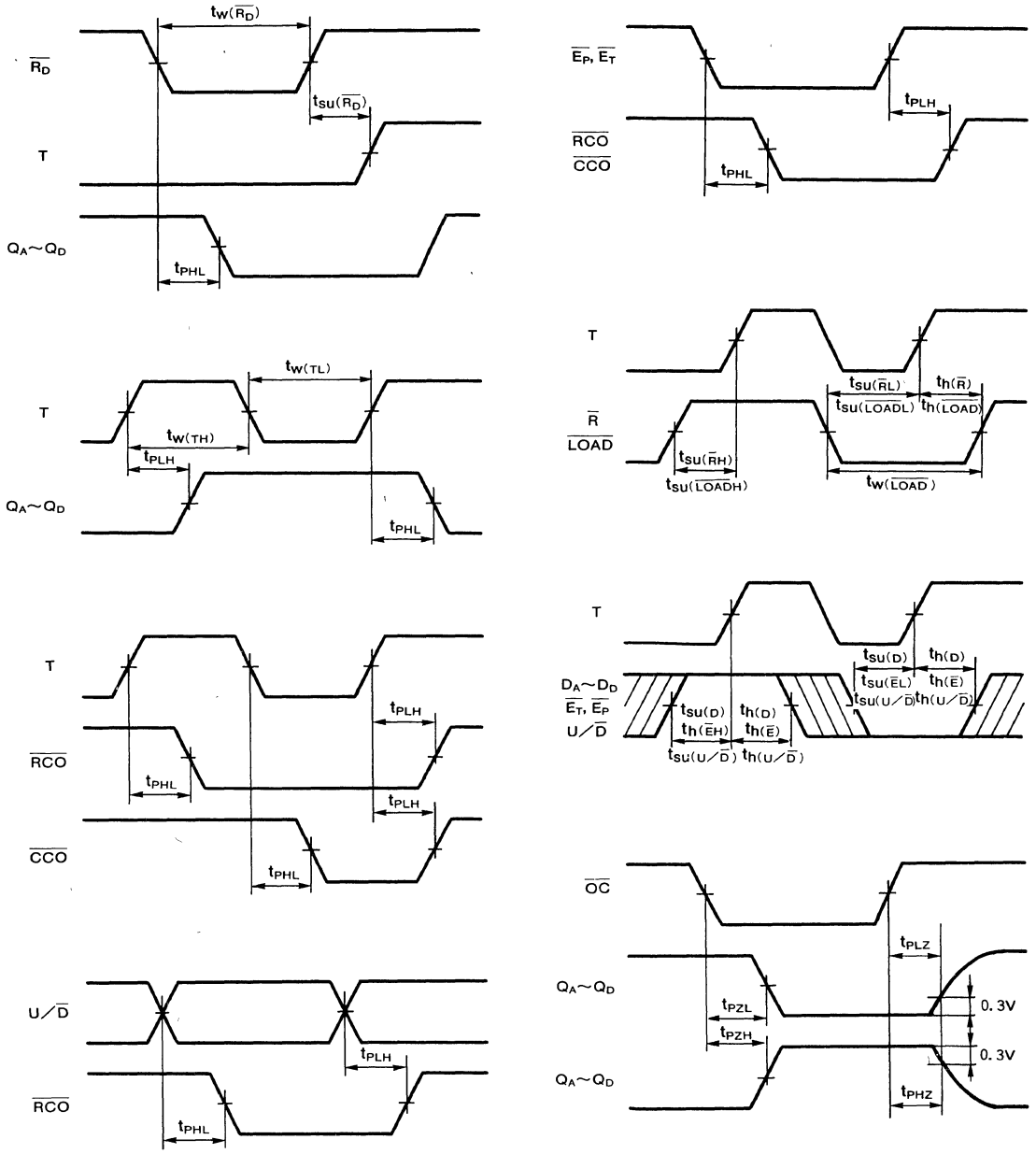
| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{w(TH)}$ | Pulse width | T "H" | 16.5 | | | 17.5 | | | ns |
| $t_{w(TL)}$ | | T "L" | 16.5 | | | 17.5 | | | |
| $t_{w(\overline{RD})}$ | | $\overline{R_D}$ "L" | 15 | | | 16 | | | |
| $t_{w(\overline{LOAD})}$ | | $\overline{LOAD}$ "L" | 15 | | | 16 | | | |
| $t_{su(D)}$ | Setup time before T↑ | $D_A$~$D_D$ | 20 | | | 21 | | | ns |
| $t_{su(\overline{LOADL})}$ | | $\overline{LOAD}$ "L" | 15 | | | 16 | | | |
| $t_{su(\overline{LOADH})}$ | | $\overline{LOAD}$ "H" (inactive) | 30 | | | 31 | | | |
| $t_{su(\overline{EH})}$ | | $\overline{E_T}$, $\overline{E_P}$ "H" | 30 | | | 31 | | | |
| $t_{su(\overline{EL})}$ | | $\overline{E_T}$, $\overline{E_P}$ "L" | 20 | | | 21 | | | |
| $t_{su(\overline{RL})}$ | | $\overline{R}$ "L" | 15 | | | 16 | | | |
| $t_{su(\overline{RH})}$ | | $\overline{R}$ "H" (inactive) | 30 | | | 31 | | | |
| $t_{su(\overline{RD})}$ | | $\overline{R_D}$ "H" (inactive) | 10 | | | 11 | | | |
| $t_{su(U/\overline{D})}$ | | U/$\overline{D}$ | 30 | | | 31 | | | |
| $t_{h(D)}$ | Hold time after T↑ | $D_A$~$D_D$ | 0 | | | 1 | | | ns |
| $t_{h(\overline{LOAD})}$ | | $\overline{LOAD}$ "L" | 0 | | | 1 | | | |
| $t_{h(\overline{R})}$ | | $\overline{R}$ "L" | 0 | | | 1 | | | |
| $t_{h(\overline{E})}$ | | $\overline{E_T}$, $\overline{E_P}$ | 0 | | | 1 | | | |
| $t_{h(U/\overline{D})}$ | | U/$\overline{D}$ | 0 | | | 1 | | | |

* All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

↑ Transition from low to high

## SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH 3-STATE OUTPUT

### TIMING DIAGRAM (Reference level = 1.3V)




Note 4: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS573P

## OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS573P is a semiconductor integrated circuit consisting of eight D-type latch circuits with 3-state noninverted output and is provided with an output control input and an enable input, both common to all circuits.

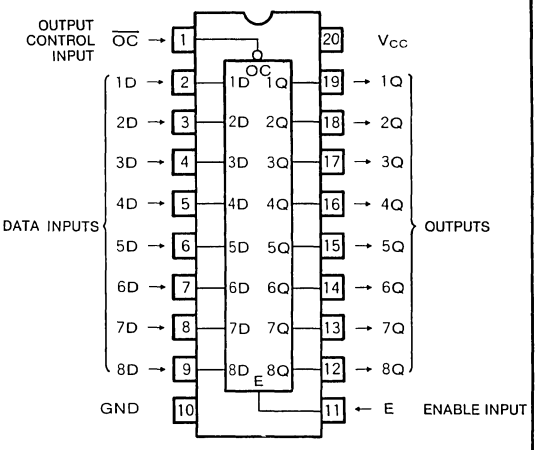
## FEATURES

- 3-state, high fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High package density with eight circuits in one package
- Output control and enable inputs common to all eight circuits
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

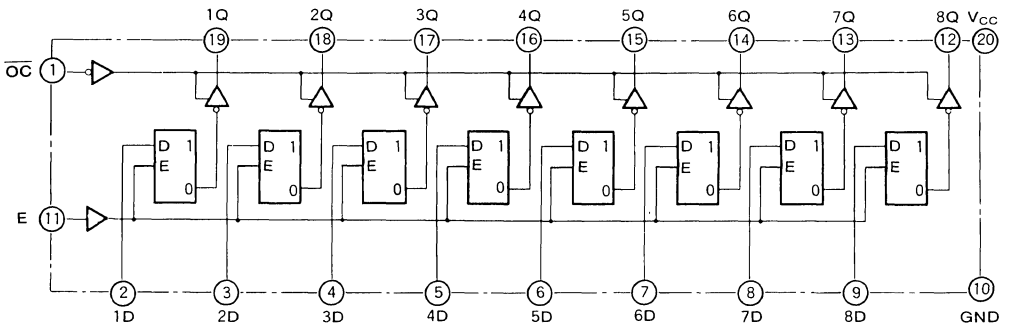
## FUNCTIONAL DESCRIPTION

The eight D-type latch circuits have the common output control $\overline{OC}$ and enable input E. While E is high, the information from D appears at the output Q and Q changes with D. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of Q is retained even if D changes.

While $\overline{OC}$ is high, 1Q ~ 8Q are in the high-impedance state "Z" irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While Q is "Z", old data can be retained or new data can be entered.

Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bi-directional bus driver.

## LOGIC DIAGRAM



# OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (NONINVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | | Output |
|---|---|---|---|
| $\overline{OC}$* | E | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q^0$ |
| H | X | X | Z |

Note 1: $Q^0$ : Level of Q before the indicated steady-state input conditions were established.
Z : High-impedance state
X : Irrelevant
* : Data can be latched irrespective of $\overline{OC}$.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5 ~ +5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 ~ +75 | °C |
| $T_{stg}$ | Storage temperature range | | −65 ~ +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $I_{OH}$=−2.6mA | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 10 | 19 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 15 | 24 | mA |
| $I_{CCZ}$ | Supply current, outputs disabled | $V_{CC}$=5.5V | | | 16 | 27 | mA |

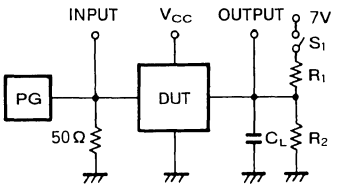
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Outputs | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | 1D~8D | 1Q~8Q | 2 | 8 | 14 | 2 | 8 | 15 | ns |
| $t_{PHL}$ | | | | 2 | 9 | 14 | 2 | 9 | 15 | |
| $t_{PLH}$ | | E | 1Q~8Q | 8 | 13 | 20 | 8 | 13 | 21 | ns |
| $t_{PHL}$ | | | | 8 | 15 | 19 | 8 | 15 | 20 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | 1Q~8Q | 4 | 14 | 20 | 4 | 14 | 21 | ns |
| $t_{PZL}$ | | | | 4 | 12 | 18 | 4 | 12 | 19 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | 1Q~8Q | 2 | 6 | 8 | 2 | 6 | 9 | ns |
| $t_{PLZ}$ | | | | 3 | 5 | 13 | 3 | 5 | 14 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) CL includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

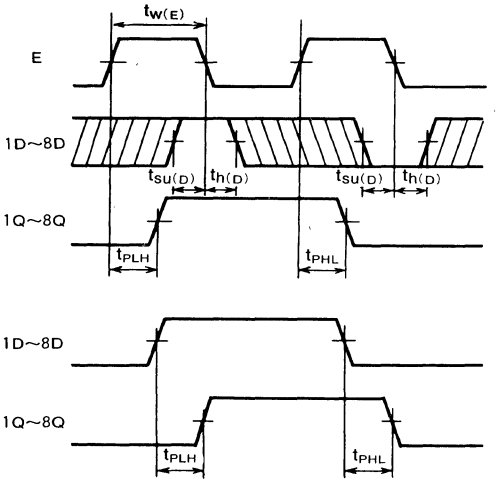
## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

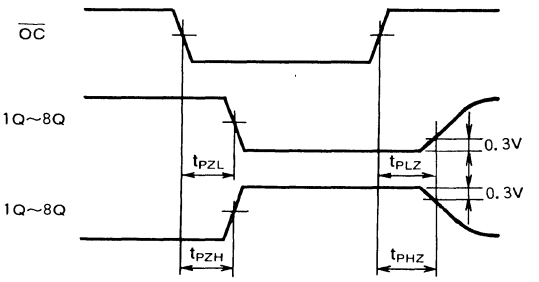
| Symbol | Parameter | | Limits: $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{w(E)}$ | Pulse width | E "H" | 15 | 9 | | 16 | 9 | | ns |
| $t_{su(D)}$ | Setup time before E ↓ | 1D~8D | 10 | 2 | | 11 | 2 | | ns |
| $t_{h(D)}$ | Hold time after E ↓ | 1D~8D | 7 | 4 | | 8 | 4 | | ns |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↓: Transition from high to low

## TIMING DIAGRAM (Reference level = 1.3V)




Note 3 The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS574P

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS574P is a semiconductor integrated circuit consisting of eight D-type positive edge-triggered flip-flop circuits with 3-state noninverted output and is provided with an output control input and a clock input, both common to all circuits.

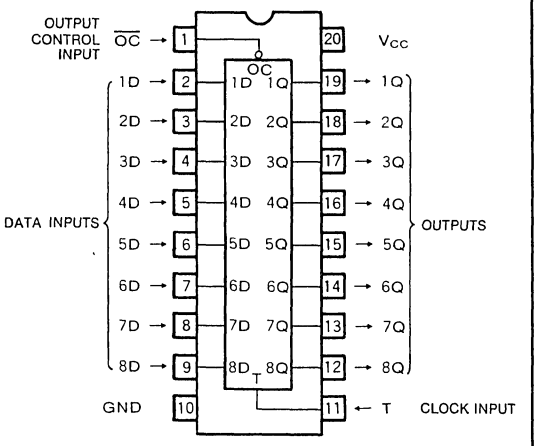
## FEATURES

- Positive edge triggering
- 3-state, high fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High package density with eight circuits in one package
- Output control and clock inputs common to all eight circuits
- Wide operating temperature range ($T_a$ = −20 ~ +75°C

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## PIN CONFIGURATION (TOP VIEW)



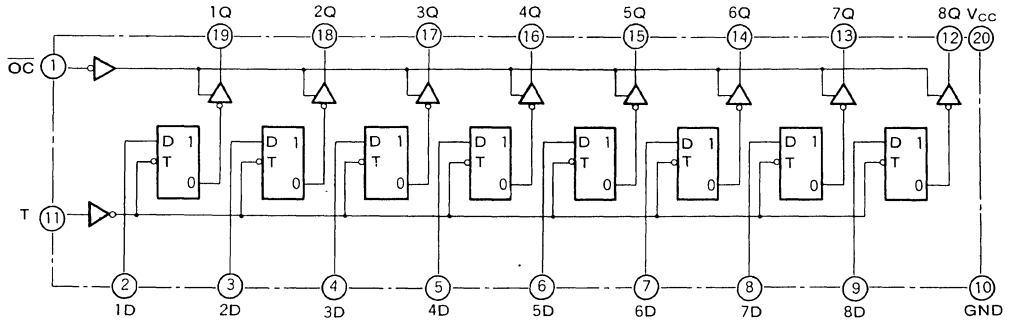

Outline 20P4

## FUNCTIONAL DESCRIPTION

The eight D-type edge-triggered flip-flop circuits have the common output control $\overline{OC}$ and clock input T. When T changes from low to high, the status of D immediately before the change appears at the output Q in accordance with the function table.

While $\overline{OC}$ is high, 1Q ~ 8Q are in the high-impedance state "Z" irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While Q is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

## LOGIC DIAGRAM



# OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT (NONINVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | | Output |
|---|---|---|---|
| $\overline{OC}$* | T | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | $Q^0$ |
| H | X | X | Z |

Note 1. ↑ : Transition from low to high level (positive edge trigger)

$Q^0$: Level of Q before the indicated steady-state input conditions were established.

Z : High-impedance state

X : Irrelevant

* Data can be stored irrespective of $\overline{OC}$.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $I_{OH}$=−2.6mA | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 10 | 19 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 15 | 24 | mA |
| $I_{CCZ}$ | Supply current, outputs disabled | $V_{CC}$=5.5V | | | 16 | 27 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

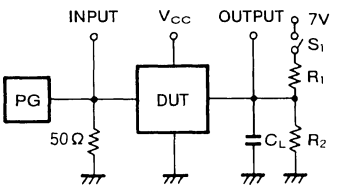
## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT (NONINVERTED)

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Output | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | $T_a$=0~70℃ Typ * | $T_a$=0~70℃ Max | $T_a$=−20~+75℃ Min | $T_a$=−20~+75℃ Typ * | $T_a$=−20~+75℃ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | T | Q | 35 | 50 | | 32 | 50 | | MHz |
| $t_{PLH}$ | Propagation time | T | Q | 4 | 10 | 14 | 4 | 10 | 15 | ns |
| $t_{PHL}$ | | | | 4 | 12 | 14 | 4 | 12 | 15 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | Q | 4 | 13 | 20 | 4 | 13 | 21 | ns |
| $t_{PZL}$ | | | | 4 | 12 | 18 | 4 | 12 | 19 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | Q | 2 | 6 | 8 | 2 | 6 | 9 | ns |
| $t_{PLZ}$ | | | | 3 | 6 | 13 | 3 | 6 | 14 | |

*. All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2 Measurement circuit




(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

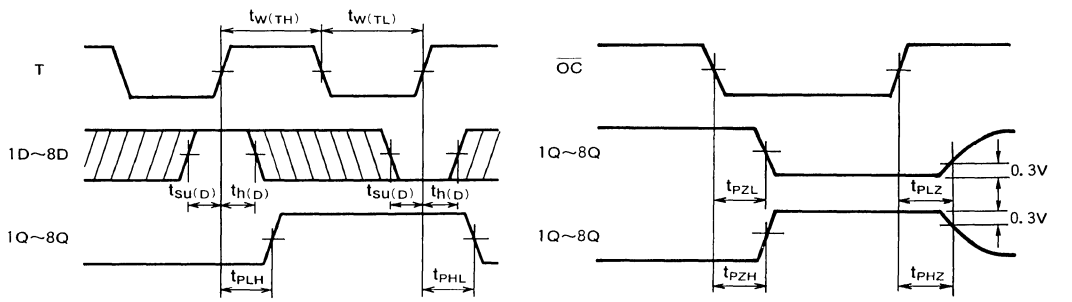
## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

| Symbol | Parameter | | Limits: $T_a$=0~70℃ Min | $T_a$=0~70℃ Typ * | $T_a$=0~70℃ Max | $T_a$=−20~+75℃ Min | $T_a$=−20~+75℃ Typ * | $T_a$=−20~+75℃ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{W(TH)}$ | Pulse width | T "H" | 14 | 5 | | 15 | 5 | | ns |
| $t_{W(TL)}$ | | T "L" | 14 | 10 | | 15 | 10 | | |
| $t_{su(D)}$ | Setup time in before T ↑ | 1D~8D | 15 | 3 | | 16 | 3 | | ns |
| $t_{h(D)}$ | Hold time in after T ↑ | 1D~8D | 0 | −1 | | 1 | −1 | | ns |

*· All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↑· Transition from low to high

## TIMING DIAGRAM (Reference level = 1.3V)




Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS575P

PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT AND SYNCHRONOUS RESET (NONINVERTED)

## DESCRIPTION

The M74ALS575P is a semiconductor integrated circuit consisting of eight D-type positive edge-triggered flip-flop circuits with 3-state noninverted output and is provided with an output control input, a clock input, and a reset input, all three common to all circuits.

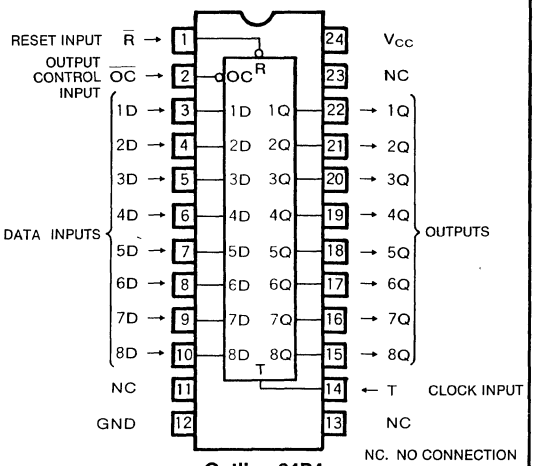
## FEATURES

- Positive edge triggering
- 3-state, high fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High package density with eight circuits in one package
- Output control and clock inputs common to all eight circuits
- Reset input common to all eight circuits
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## PIN CONFIGURATION (TOP VIEW)



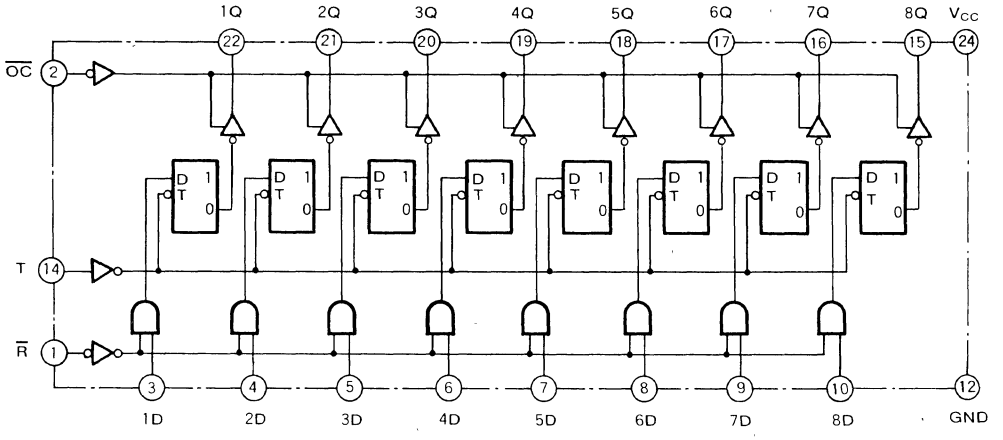

Outline 24P4

## FUNCTIONAL DESCRIPTION

The eight D-type edge-triggered flip-flop circuits have the common output control $\overline{OC}$ and clock input T, and reset input $\overline{R}$ which is synchronous with the clock. When T changes from low to high, the status of D immediately before the change appears at the output Q in accordance with the function table. When $\overline{R}$, operating synchronously with the clock, is low and T changes from low to high, then 1Q ~ 8Q become low.

While $\overline{OC}$ is high, 1Q ~ 8Q are in the high-impedance state "Z" irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While Q is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

## LOGIC DIAGRAM



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# OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT AND SYNCHRONOUS RESET (NONINVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | | | Output |
|---|---|---|---|---|
| $\overline{OC}$* | $\overline{R}$ | T | D | Q |
| L | L | ↑ | X | L |
| L | H | ↑ | H | H |
| L | H | ↑ | L | L |
| L | H | L | X | $Q^0$ |
| H | X | X | X | Z |

Note 1: ↑ : Transition from low to high level (positive edge trigger)
$Q^0$: Level of Q before the indicated steady-state input conditions were established.
Z High-impedance state
X Irrelevant
* Data can be stored or reset irrespective of $\overline{OC}$

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5～+7 | V |
| $V_I$ | Input voltage | | −0.5～+7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5～+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20～+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65～+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 10 | 19 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 15 | 24 | mA |
| $I_{CCZ}$ | Supply current, outputs disabled | $V_{CC}$=5.5V | | | 16 | 27 | mA |

* All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

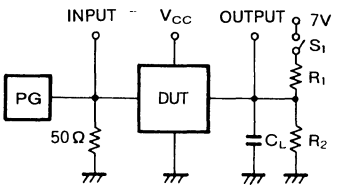
## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT AND SYNCHRONOUS RESET (NONINVERTED)

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | T | 1Q~8Q | 30 | | | 28 | | | MHz |
| $t_{PLH}$ | Propagation time | T | 1Q~8Q | 4 | | 14 | 4 | | 15 | ns |
| $t_{PHL}$ | | | | 4 | | 14 | 4 | | 15 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | 1Q~8Q | 4 | | 20 | 4 | | 21 | ns |
| $t_{PZL}$ | | | | 4 | | 18 | 4 | | 19 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | 1Q~8Q | 2 | | 8 | 2 | | 9 | ns |
| $t_{PLZ}$ | | | | 3 | | 13 | 3 | | 14 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

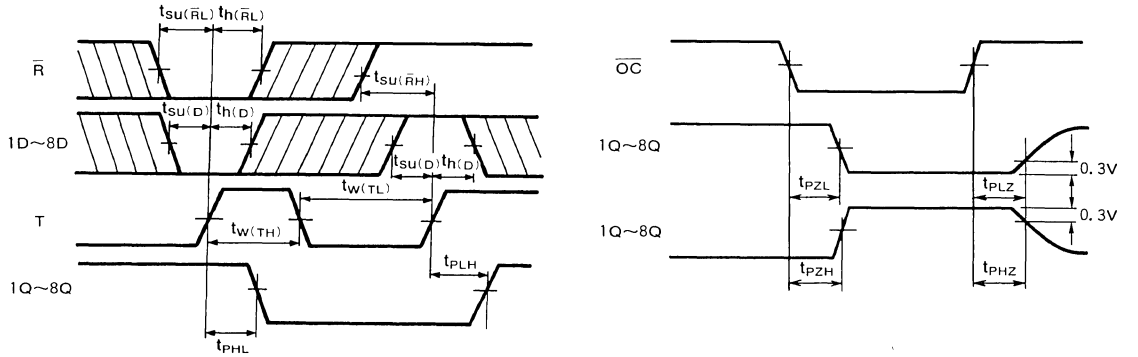
| Symbol | Parameter | | Limits: $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{w(TH)}$ | Pulse width | T "H" | 16.5 | | | 17.5 | | | ns |
| $t_{w(TL)}$ | | T "L" | 16.5 | | | 17.5 | | | |
| $t_{su(D)}$ | Setup time before T ↑ | 1D~8D | 15 | | | 16 | | | ns |
| $t_{su(\overline{R}H)}$ | | $\overline{R}$ "H" (inactive) | 20 | | | 21 | | | |
| $t_{su(\overline{R}L)}$ | | $\overline{R}$ "L" | 15 | | | 16 | | | |
| $t_{h(D)}$ | Hold time after T ↑ | 1D~8D | 0 | | | 1 | | | ns |
| $t_{h(\overline{R}L)}$ | | $\overline{R}$ "L" | 0 | | | 1 | | | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↑: Transition from low to high

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT AND SYNCHRONOUS RESET (NONINVERTED)

### TIMING DIAGRAM (Reference level = 1.3V)




Note 3. The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS576P

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS576P is a semiconductor integrated circuit consisting of eight D-type positive edge-triggered flip-flop circuits with 3-state inverted output and is provided with an output control input and a clock input, both common to all circuits.

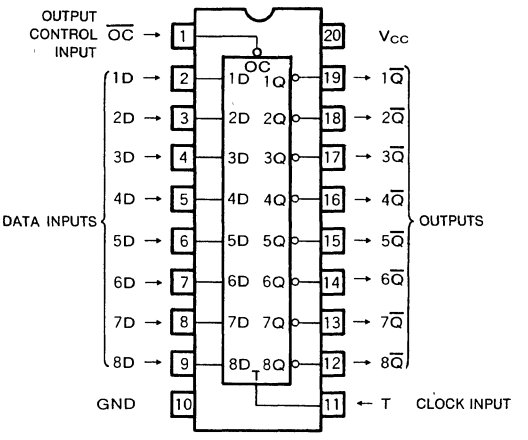
## FEATURES

- Positive edge triggering
- 3-state, high fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High package density with eight circuits in one package
- Output control and clock inputs common to all eight circuits
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

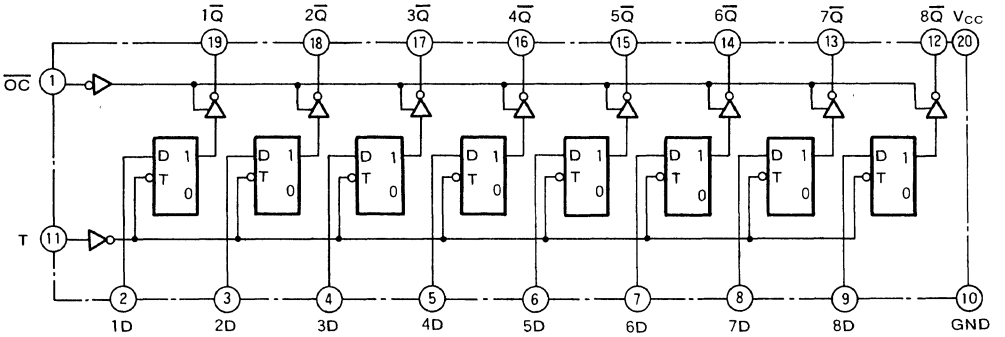
## FUNCTIONAL DESCRIPTION

The eight D-type edge-triggered flip-flop circuits have the common output control $\overline{OC}$ and clock input T. When T changes from low to high, the status of D immediately before the change appears inverted at the output $\overline{Q}$ in accordance with the function table.

While $\overline{OC}$ is high, $1\overline{Q}$ ~ $8\overline{Q}$ are in the high-impedance state "Z" irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While $\overline{Q}$ is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

Except for type name, the M74ALS576P is identical in all respects, including pin configuration, functions, and specifications, to M74ALS564P.

## LOGIC DIAGRAM



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# M74ALS576P

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT (INVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | | Output |
|---|---|---|---|
| $\overline{OC}$* | T | D | $\overline{Q}$ |
| L | ↑ | H | L |
| L | ↑ | L | H |
| L | L | X | $\overline{Q}^0$ |
| H | X | X | Z |

Note 1: ↑ : Transition from low to high level (positive edge trigger)

$\overline{Q}^0$ : Level of $\overline{Q}$ before the indicated steady-state input conditions were established.

Z : High-impedance state

X : Irrelevant

* : Data can be stored irrespective of $\overline{OC}$.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5 ~ +5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 ~ +75 | °C |
| $T_{stg}$ | Storage temperature range | | −65 ~ +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $I_{OH}$=−2.6mA | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 10 | 19 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 15 | 24 | mA |
| $I_{CCZ}$ | Supply current, outputs disabled | $V_{CC}$=5.5V | | | 16 | 27 | mA |

* . All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

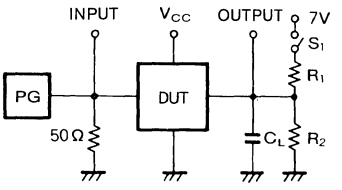
## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT (INVERTED)

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | $T_a$=0~70℃ Typ* | $T_a$=0~70℃ Max | $T_a$=−20~+75℃ Min | $T_a$=−20~+75℃ Typ* | $T_a$=−20~+75℃ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | T | $1\overline{Q}$~$8\overline{Q}$ | 30 | | | 28 | | | MHz |
| $t_{PLH}$ | Propagation time | T | $1\overline{Q}$~$8\overline{Q}$ | 4 | | 14 | 4 | | 15 | ns |
| $t_{PHL}$ | | | | 4 | | 14 | 4 | | 15 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | $1\overline{Q}$~$8\overline{Q}$ | 4 | | 20 | 4 | | 21 | ns |
| $t_{PZL}$ | | | | 4 | | 18 | 4 | | 19 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | $1\overline{Q}$~$8\overline{Q}$ | 2 | | 8 | 2 | | 9 | ns |
| $t_{PLZ}$ | | | | 3 | | 13 | 3 | | 14 | |

* All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 2 Measurement circuit




(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

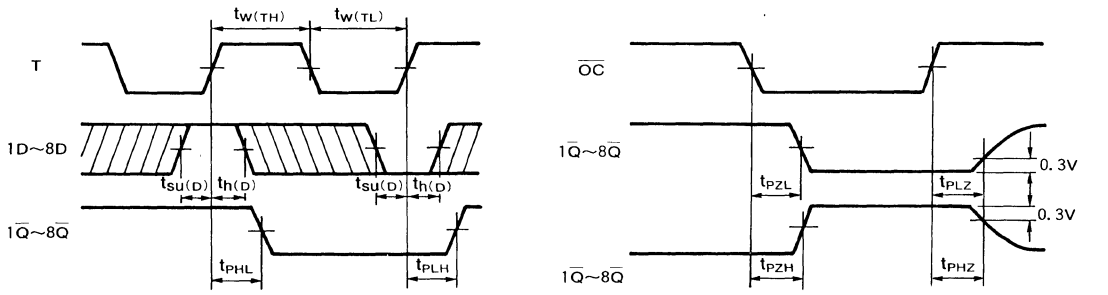
| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

| Symbol | Parameter | | Limits: $T_a$=0~70℃ Min | $T_a$=0~70℃ Typ* | $T_a$=0~70℃ Max | $T_a$=−20~+75℃ Min | $T_a$=−20~+75℃ Typ* | $T_a$=−20~+75℃ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{w(TH)}$ | Pulse width | T "H" | 16.5 | | | 17.5 | | | ns |
| $t_{w(TL)}$ | | T "L" | 16.5 | | | 17.5 | | | |
| $t_{su(D)}$ | Setup time before T ↑ | 1D~8D | 15 | | | 16 | | | ns |
| $t_{h(D)}$ | Hold time after T ↑ | 1D~8D | 0 | | | 1 | | | ns |

*. All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.
↑ : Transition from low to high (positive edge trigger)

## TIMING DIAGRAM (Reference level = 1.3V)




Note 3 The shaded areas indicate the period when the input is permitted to change for predictable output performance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# M74ALS577P

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT AND SYNCHRONOUS RESET (INVERTED)

## DESCRIPTION

The M74ALS577P is a semiconductor integrated circuit consisting of eight D-type positive edge-triggered flip-flop circuits with 3-state inverted output and is provided with an output control input, a clock input, and a reset input, all three common to all circuits.

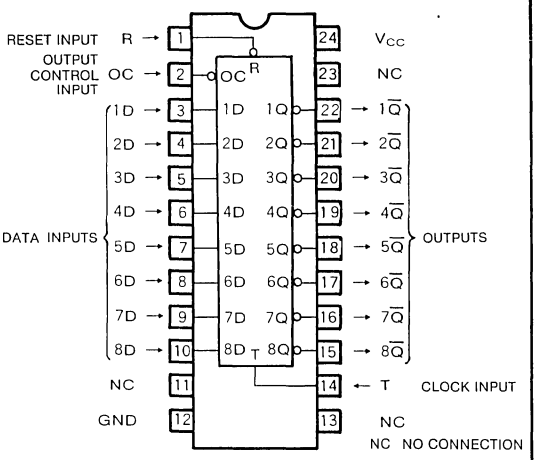
## FEATURES

- Positive edge triggering
- 3-state, high fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High package density with eight circuits in one package
- Output control and clock inputs common to all eight circuits
- Reset input common to all eight circuits
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## PIN CONFIGURATION (TOP VIEW)



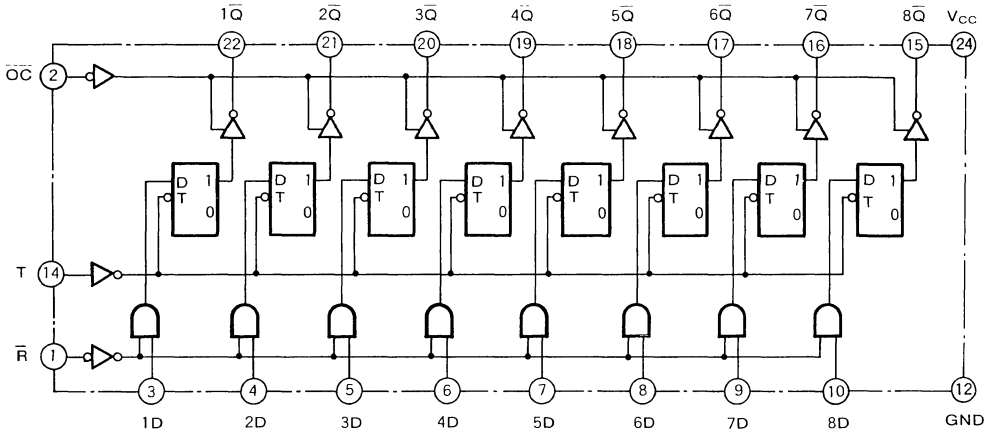

Outline 24P4

## FUNCTIONAL DESCRIPTION

The eight D-type edge-triggered flip-flop circuits have the common output control $\overline{OC}$, clock input T, and reset input $\overline{R}$ which is synchronous with the clock. When T changes from low to high, the status of D immediately before the change appears inverted at the output $\overline{Q}$ in accordance with the function table. When $\overline{R}$ is low, and T is set from low to high, the outputs $1\overline{Q}$ ~ $8\overline{Q}$ become high.

While $\overline{OC}$ is high, $1\overline{Q}$ ~ $8\overline{Q}$ are in the high-impedance state "Z" irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While $\overline{Q}$ is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

## LOGIC DIAGRAM



# M74ALS577P

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT AND SYNCHRONOUS RESET (INVERTED)

### FUNCTION TABLE (Note 1)

| Inputs | | | | Output |
|---|---|---|---|---|
| $\overline{OC}$* | $\overline{R}$ | T | D | $\overline{Q}$ |
| L | L | ↑ | X | H |
| L | H | ↑ | H | L |
| L | H | ↑ | L | H |
| L | H | L | X | $\overline{Q}^0$ |
| H | X | X | X | Z |

Note 1: ↑ Transition from low to high level (positive edge trigger)

$\overline{Q}^0$ : Level of $\overline{Q}$ before the indicated steady-state input conditions were established.

Z : High-impedance state

X : Irrelevant

* : Data can be stored or reset irrespective of $\overline{OC}$.

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 10 | 19 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 15 | 24 | mA |
| $I_{CCZ}$ | Supply current, outputs disabled | $V_{CC}$=5.5V | | | 16 | 27 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

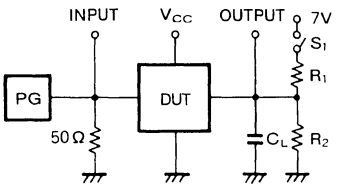
## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT AND SYNCHRONOUS RESET (INVERTED)

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | T | $1\overline{Q}$~$8\overline{Q}$ | 30 | | | 28 | | | MHz |
| $t_{PLH}$ | Propagation time | T | $1\overline{Q}$~$8\overline{Q}$ | 4 | | 14 | 4 | | 15 | ns |
| $t_{PHL}$ | | | | 4 | | 14 | 4 | | 15 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | $1\overline{Q}$~$8\overline{Q}$ | 4 | | 20 | 4 | | 21 | ns |
| $t_{PZL}$ | | | | 4 | | 18 | 4 | | 19 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | $1\overline{Q}$~$8\overline{Q}$ | 2 | | 10 | 2 | | 11 | ns |
| $t_{PLZ}$ | | | | 3 | | 13 | 3 | | 14 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2 Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

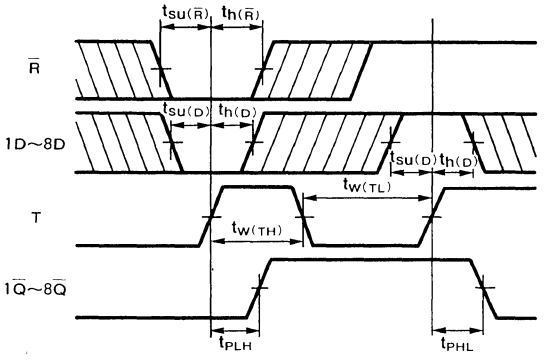
## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

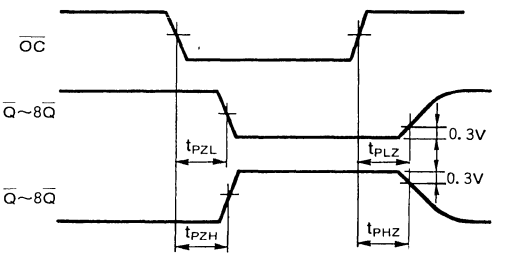
| Symbol | Parameter | | Limits: $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{w(TH)}$ | Pulse width | T "H" | 16.5 | | | 17.5 | | | ns |
| $t_{w(TL)}$ | | T "L" | 16.5 | | | 17.5 | | | |
| $t_{su(D)}$ | Setup time before T↑ | 1D~8D | 15 | | | 16 | | | ns |
| $t_{su(\overline{R})}$ | | $\overline{R}$ "L" | 15 | | | 16 | | | |
| $t_{h(D)}$ | Hold time after T↑ | 1D~8D | 0 | | | 1 | | | ns |
| $t_{h(\overline{R})}$ | | $\overline{R}$ "L" | 0 | | | 1 | | | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C

↑: Transition from low to high

## TIMING DIAGRAM (Reference level = 1.3V)




Note 3 The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS580P

## OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS580P is a semiconductor integrated circuit consisting of eight D-type latch circuits with 3-state inverted output and is provided with an output control input and an enable input, both common to all circuits.

## FEATURES

- 3-state, high fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High package density with eight circuits in one package
- Output control and enable inputs common to all eight circuits
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

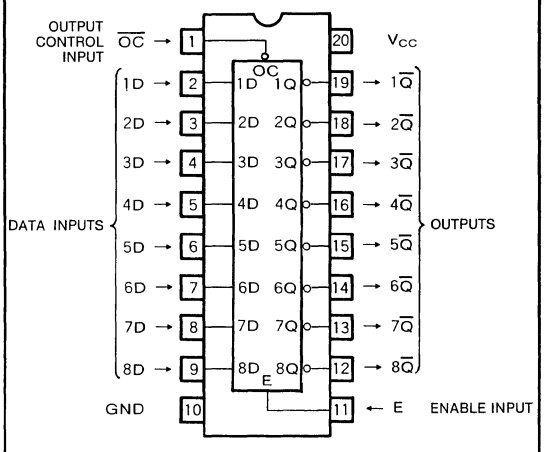
General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

The eight D-type latch circuits have the common output control $\overline{OC}$ and enable input E. While E is high, the information from D appears inverted at the output $\overline{Q}$ and $\overline{Q}$ changes with D.When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of $\overline{Q}$ is retained even if D changes.

While $\overline{OC}$ is high, $1\overline{Q}$ ~ $8\overline{Q}$ are in the high-impedance state "Z" irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While $\overline{Q}$ is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

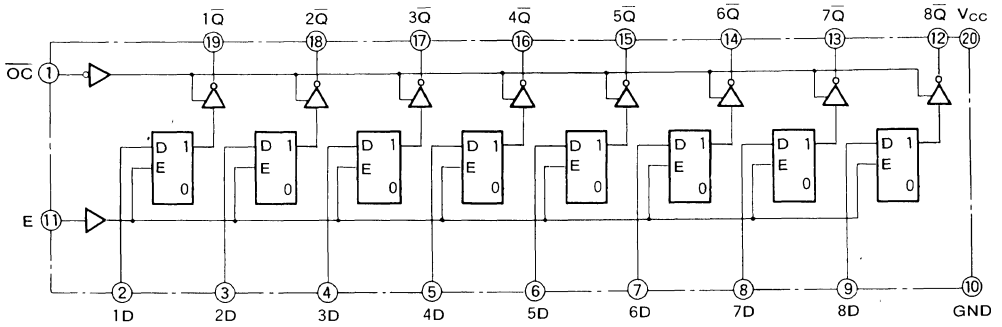
## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

Except for type name, the M74ALS580P is identical in all respects, including pin configuration, functions, and specifications, to M74ALS563P.

## LOGIC DIAGRAM



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# M74ALS580P

## OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (INVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | | Output |
|---|---|---|---|
| $\overline{OC}$* | E | D | $\overline{Q}$ |
| L | H | H | L |
| L | H | L | H |
| L | L | X | $\overline{Q}^0$ |
| H | X | X | Z |

Note 1 $\overline{Q}^0$ Level of $\overline{Q}$ before the indicated steady-state input conditions were established.

Z High-impedance state

X Irrelevant

* Data can be latched irrespective of $\overline{OC}$.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5~+5.5 | V |
| Topr | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| Tstg | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| Topr | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 10 | 19 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 15 | 24 | mA |
| $I_{CCZ}$ | Supply current, outputs disabled | $V_{CC}$=5.5V | | | 16 | 27 | mA |

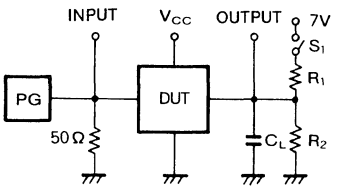
* All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | 1D~8D | 1$\overline{Q}$~8$\overline{Q}$ | 3 | | 18 | 3 | | 19 | ns |
| $t_{PHL}$ | | | | 3 | | 14 | 3 | | 15 | |
| $t_{PLH}$ | | E | 1$\overline{Q}$~8$\overline{Q}$ | 8 | | 22 | 8 | | 23 | ns |
| $t_{PHL}$ | | | | 8 | | 21 | 8 | | 22 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | 1$\overline{Q}$~8$\overline{Q}$ | 4 | | 20 | 4 | | 21 | ns |
| $t_{PZL}$ | | | | 4 | | 18 | 4 | | 19 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | 1$\overline{Q}$~8$\overline{Q}$ | 2 | | 8 | 2 | | 9 | ns |
| $t_{PLZ}$ | | | | 3 | | 13 | 3 | | 14 | |

*. All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 2. Measurement circuit




(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

| Symbol | Parameter | | Limits: $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{w(E)}$ | Pulse width | E "H" | 15 | | | 16 | | | ns |
| $t_{su(D)}$ | Setup time before E↓ | 1D~8D | 10 | | | 11 | | | ns |
| $t_{h(D)}$ | Hold time after E↓ | 1D~8D | 10 | | | 11 | | | ns |

*. All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

↓: Transition from high to low



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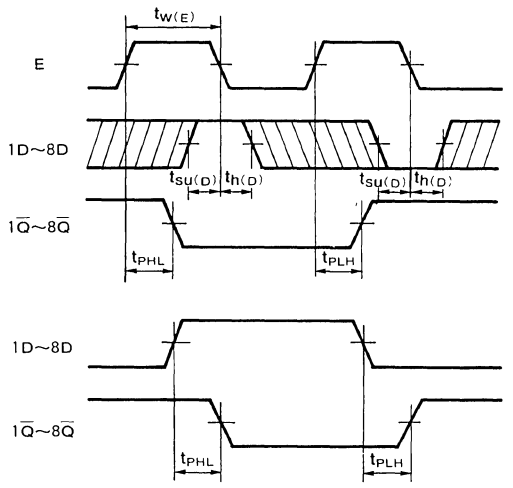
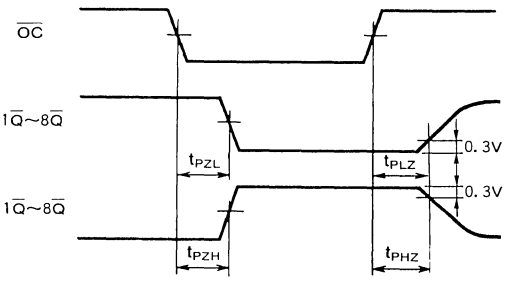
## TIMING DIAGRAM (Reference level = 1.3V)




Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS620P

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS620P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with 3-state inverted outputs.

## FEATURES

- Two-way transmission or isolation between two 8-bit data
- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

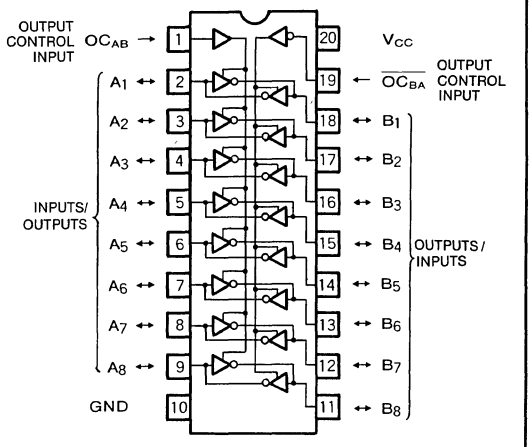
The inputs and outputs are mutually connected to form two-way buffers with 3-state inverted outputs.

The input/output direction is controlled by $OC_{AB}$ and $\overline{OC_{BA}}$.

When $OC_{AB}$ and $\overline{OC_{BA}}$ are high, pins A are made the input pins and pins B are made the output pins. When $OC_{AB}$ and $\overline{OC_{BA}}$ are low, B are made the input pins and A are made the output pins. When $OC_{AB}$ is low and $\overline{OC_{BA}}$ is high, both A and B are in the high-impedance state and A and B are isolated. Latch operation is possible when $OC_{AB}$ is high and $\overline{OC_{BA}}$ is low.

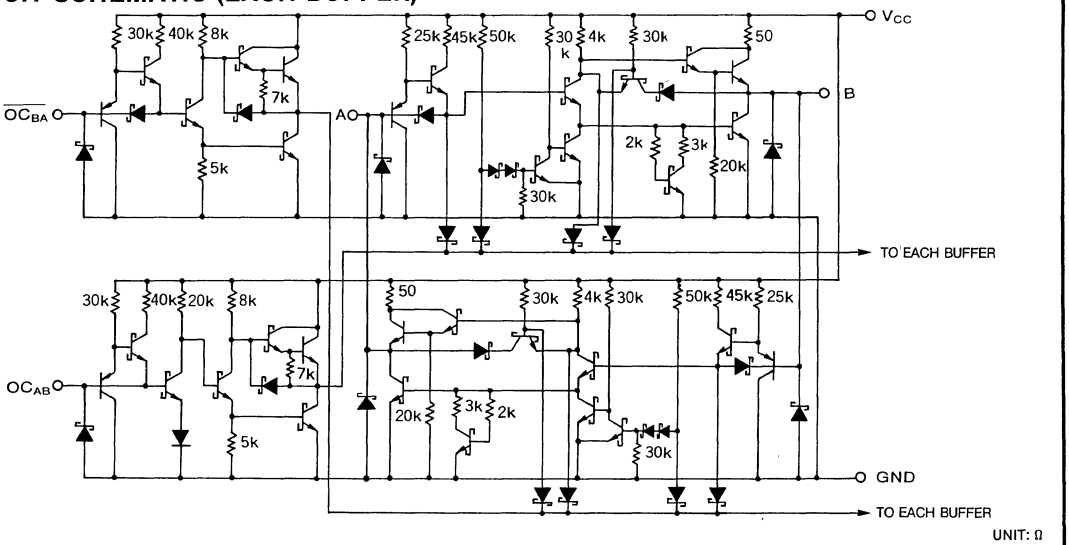
The low-power version of M74ALS620P, the M74ALS1620P, is also available.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

## CIRCUIT SCHEMATIC (EACH BUFFER)






MITSUBISHI ELECTRIC

# OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC_{BA}}$ | $OC_{AB}$ | A | B |
| L | L | $\overline{O}$ | I |
| H | H | I | $\overline{O}$ |
| H | L | Z | Z |
| L | H | * | * |

Note 1: I : Input pins
$\overline{O}$ : Output pins (inverted output)
Z : High-impedance state (A and B are isolated)
* : In this case, data can be latched with the procedure shown below.
(1) Apply the data to be stored to A or B. ($OC_{AB}$ and $\overline{OC_{BA}}$ must be equally high or equally low.)
(2) Set $OC_{AB}$ high and $\overline{OC_{BA}}$ low respectively.
(3) Remove the data.
(4) The data applied in (1) is stored If voltage is applied to A or B in this condition, the device may be damaged. Change the status of $OC_{AB}$ or $\overline{OC_{BA}}$ before applying voltage.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+5.5 | V |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state or high-impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $OC_{AB}$, $\overline{OC_{BA}}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | |
| $I_{IH}$ | High-level input current (Note 2) | $OC_{AB}$, $\overline{OC_{BA}}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current (Note 3) | $OC_{AB}$, $\overline{OC_{BA}}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 18 | 30 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 25 | 41 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 27 | 43 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 2: For A and B, $I_{IH}$ includes off-state high-level output current $I_{OZH}$.

Note 3: For A and B, $I_{IL}$ includes off-state low-level output current $I_{OZL}$.

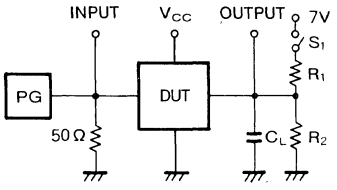
## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70°C Min | Typ * | Max | $T_a$=−20~+75°C Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A, B | B, A | 2 | 5 | 12 | 2 | 5 | 13 | ns |
| $t_{PHL}$ | | | | 2 | 5 | 12 | 2 | 5 | 13 | |
| $t_{PZH}$ | Output enable time | $\overline{OC_{BA}}$ | A | 5 | 10 | 20 | 5 | 10 | 21 | ns |
| $t_{PZL}$ | | | | 8 | 16 | 25 | 8 | 16 | 26 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC_{BA}}$ | A | 2 | 7 | 17 | 2 | 7 | 18 | ns |
| $t_{PLZ}$ | | | | 4 | 10 | 25 | 4 | 10 | 26 | |
| $t_{PZH}$ | Output enable time | $OC_{AB}$ | B | 2 | 11 | 17 | 2 | 11 | 18 | ns |
| $t_{PZL}$ | | | | 8 | 17 | 34 | 8 | 17 | 35 | |
| $t_{PHZ}$ | Output disable time | $OC_{AB}$ | B | 5 | 10 | 20 | 5 | 10 | 21 | ns |
| $t_{PLZ}$ | | | | 8 | 16 | 34 | 8 | 16 | 35 | |

* : All typical values are at $V_{CC}$=5V, $T_a$=25°C

Note 4: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

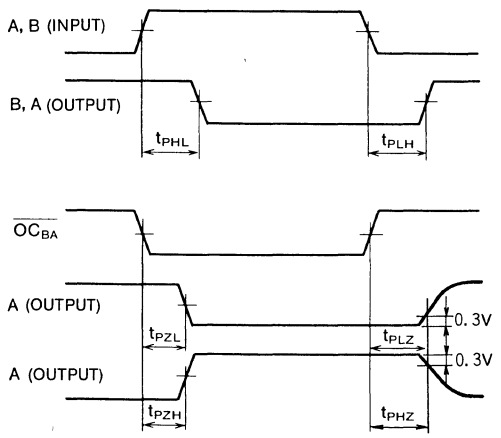
duty cycle=50%

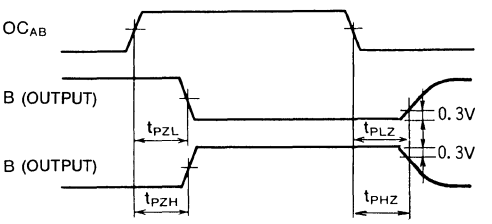
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

### TIMING DIAGRAM (Reference level = 1.3V)






MITSUBISHI ELECTRIC

# M74ALS621P

## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS621P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with noninverted open collector outputs.

## FEATURES

- Two-way transmission or isolation between two 8-bit data
- Open collector output
- High fan-out ($I_{OL}$ = 24mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

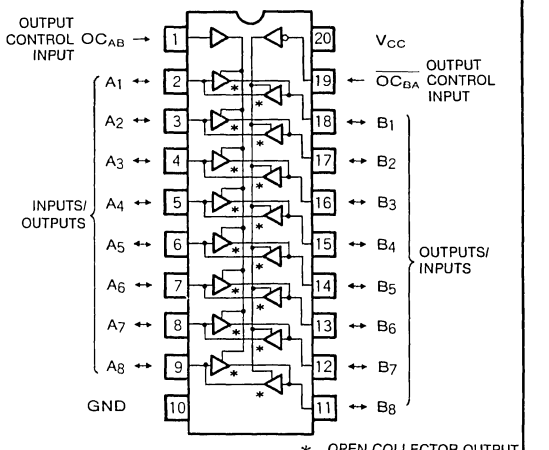
The inputs and outputs are mutually connected to form two-way buffers with noninverted open collector outputs.

The input/output direction is controlled by $OC_{AB}$ and $\overline{OC_{BA}}$.

When $OC_{AB}$ and $\overline{OC_{BA}}$ are high, pins A are made the input pins and pins B are made the output pins. When $OC_{AB}$ and $\overline{OC_{BA}}$ are low, B are made the input pins and A are made the output pins. When $OC_{AB}$ is low and $\overline{OC_{BA}}$ is high, both A and B become high and A and B are isolated. Latch operation is possible when $OC_{AB}$ is high and $\overline{OC_{BA}}$ is low.

The low-power version of M74ALS621P, the M74ALS1621P, is also available.

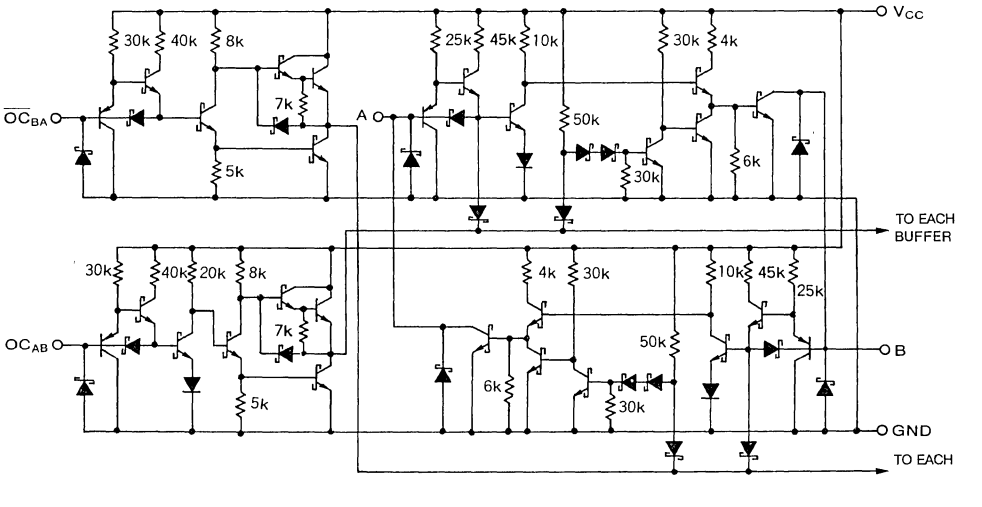
## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

The functions and pin connections of this device are identical to those of M74ALS623P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT. Ω

# OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (NONINVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC_{BA}}$ | $OC_{AB}$ | A | B |
| L | L | O | I |
| H | H | I | O |
| H | L | H | H |
| L | H | * | * |

Note 1. I : Input pins
O : Output pins
*: In this case, data can be latched with the procedure shown below.
(1) Apply the data to be stored to A or B. ($OC_{AB}$ and $\overline{OC_{BA}}$ must be equally high or equally low)
(2) Set $OC_{AB}$ high and $\overline{OC_{BA}}$ low respectively.
(3) Remove the data.
(4) The data applied in (1) is stored. If voltage is applied to A or B in this condition, the device may be damaged. Change the status of $OC_{AB}$ or $\overline{OC_{BA}}$ before applying voltage.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+7 | V |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state | −0.5~+7 | V |
| Topr | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| Tstg | Storage temperature range | | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| Topr | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | mA |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | |
| $I_{IH}$ | High-level input current | A, B | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | | | | | 20 | |
| $I_{IL}$ | Low-level input current | A, B | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | | | | | −0.1 | |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 24 | 37 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 30 | 45 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 32 | 50 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

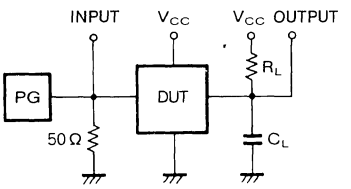
## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (NONINVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_L$=680Ω; $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A, B | B, A | 10 | 25 | 38 | 10 | 25 | 39 | ns |
| $t_{PHL}$ | | | | 5 | 14 | 20 | 5 | 14 | 21 | |
| $t_{PLH}$ | | $\overline{OC_{BA}}$ | A | 12 | 21 | 45 | 12 | 21 | 46 | ns |
| $t_{PHL}$ | | | | 12 | 25 | 40 | 12 | 25 | 41 | |
| $t_{PLH}$ | | $OC_{AB}$ | B | 15 | 25 | 45 | 15 | 25 | 46 | ns |
| $t_{PHL}$ | | | | 12 | 27 | 40 | 12 | 27 | 41 | |

* All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2. Measurement circuit




(1) The pulse generator (PG) has the following characteristics.

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

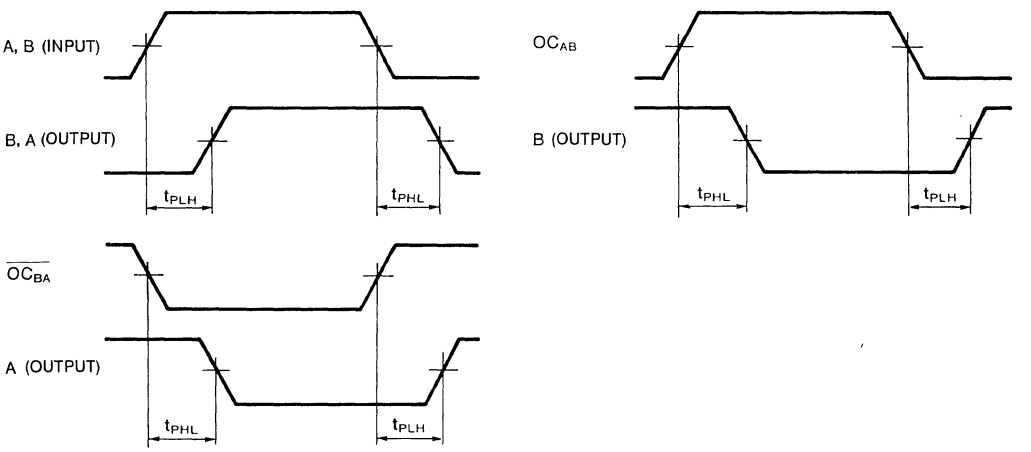
$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS622P

## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS622P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with inverted open collector outputs.

## FEATURES

- Two-way transmission or isolation between two 8-bit data
- Open collector output
- High fan-out ($I_{OL}$ = 24mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with inverted open collector outputs.

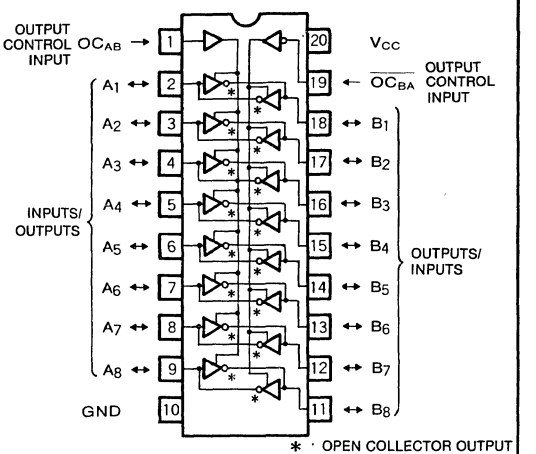
The input/output direction is controlled by $OC_{AB}$ and $\overline{OC_{BA}}$.

When $OC_{AB}$ and $\overline{OC_{BA}}$ are high, pins A are made the input pins and pins B are made the output pins. When $OC_{AB}$ and $\overline{OC_{BA}}$ are low, B are made the input pins and A are made the output pins. When $OC_{AB}$ is low and $\overline{OC_{BA}}$ is high, both A and B become high and A and B are isolated. Latch operation is possible when $OC_{AB}$ is high and $\overline{OC_{BA}}$ is low.

The low-power version of M74ALS622P, the M74ALS1622P, is also available.

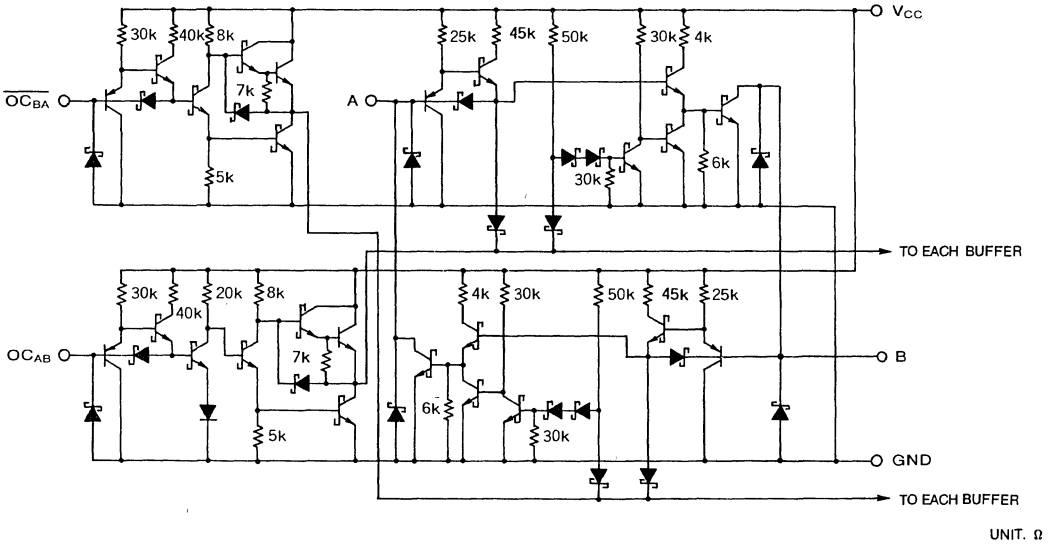
The functions and pin connections of this device are identical to those of M74ALS620P, but, since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT. Ω



MITSUBISHI ELECTRIC

# OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC_{BA}}$ | $OC_{AB}$ | A | B |
| L | L | $\overline{O}$ | I |
| H | H | I | $\overline{O}$ |
| H | L | H | H |
| L | H | * | * |

Note 1: I : Input pins

$\overline{O}$ : Output pins (inverted output)

* : In this case, data can be latched with the procedure shown below.

(1) Apply the data to be stored to A or B. ($OC_{AB}$ and $\overline{OC_{BA}}$ must be equally high or equally low.)

(2) Set $OC_{AB}$ high and $\overline{OC_{BA}}$ low respectively.

(3) Remove the data.

(4) The data applied in (1) is stored. If voltage is applied to A or B in this condition, the device may be damaged. Change the status of $OC_{AB}$ or $\overline{OC_{BA}}$ before applying voltage.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+7 | V |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state | −0.5~+7 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | mA |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | |
| $I_{IH}$ | High-level input current | A, B | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | | | | | 20 | |
| $I_{IL}$ | Low-level input current | A, B | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | | | | | −0.1 | |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 9 | 13 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 16 | 25 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 10 | 14 | mA |

* : All typical values are at $V_{CC}$=5V, $T_a$=25°C.

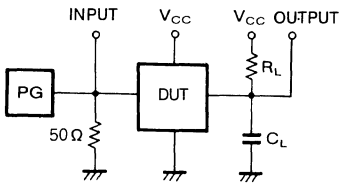
## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_L$=680Ω; $T_a$=0~70℃ Min | $T_a$=0~70℃ Typ * | $T_a$=0~70℃ Max | $T_a$=−20~+75℃ Min | $T_a$=−20~+75℃ Typ * | $T_a$=−20~+75℃ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A, B | B, A | 15 | 22 | 38 | 15 | 22 | 39 | ns |
| $t_{PHL}$ | | | | 5 | 14 | 19 | 5 | 14 | 20 | |
| $t_{PLH}$ | | $\overline{OC_{BA}}$ | A | 12 | 19 | 40 | 12 | 19 | 41 | ns |
| $t_{PHL}$ | | | | 12 | 26 | 40 | 12 | 26 | 41 | |
| $t_{PLH}$ | | $OC_{AB}$ | B | 15 | 24 | 45 | 15 | 24 | 46 | ns |
| $t_{PHL}$ | | | | 12 | 28 | 40 | 12 | 28 | 41 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C

Note 2. Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

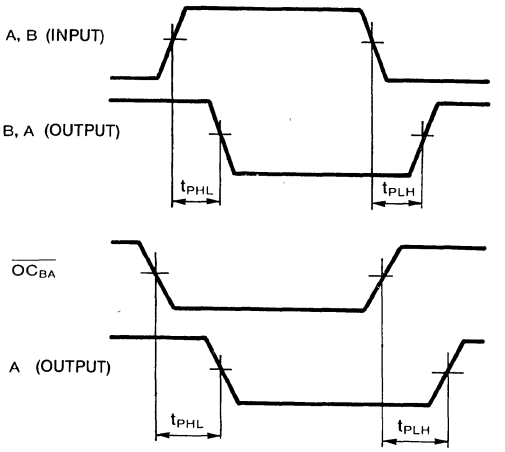
$V_{IH}$=3.5V, $V_{IL}$=0.3V

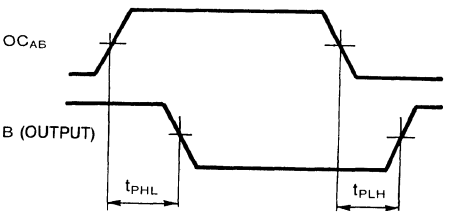
duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS623P

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS623P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with 3-state noninverted outputs.

## FEATURES

- Two-way transmission or isolation between two 8-bit data
- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

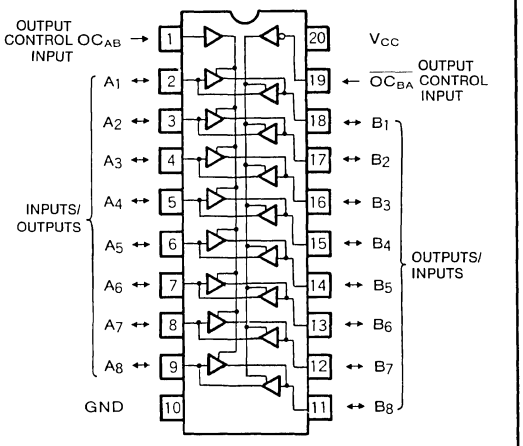
The inputs and outputs are mutually connected to form two-way buffers with 3-state noninverted outputs.

The input/output direction is controlled by $OC_{AB}$ and $\overline{OC_{BA}}$.

When $OC_{AB}$ and $\overline{OC_{BA}}$ are high, pins A are made the input pins and pins B are made the output pins. When $OC_{AB}$ and $\overline{OC_{BA}}$ are low, B are made the input pins and A are made the output pins. When $OC_{AB}$ is low and $\overline{OC_{BA}}$ is high, both A and B are in the high-impedance state and A and B are isolated. Latch operation is possible when $OC_{AB}$ is high and $\overline{OC_{BA}}$ is low.

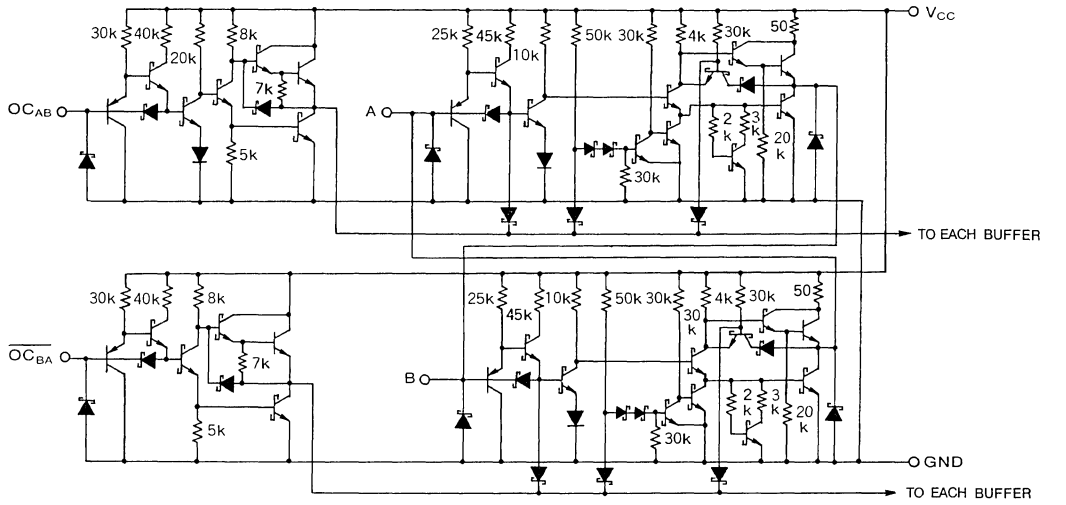
The low-power version of M74ALS623P, the M74ALS1623P, is also available.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT Ω

# OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC_{BA}}$ | $OC_{AB}$ | A | B |
| L | L | O | I |
| H | H | I | O |
| H | L | Z | Z |
| L | H | * | * |

Note 1: I : Input pins
O : Output pins (noninverted output)
Z : High-impedance state (A and B are isolated)
* : In this case, data can be latched with the procedure shown below.
(1) Apply the data to be stored to A or B. ($OC_{AB}$ and $\overline{OC_{BA}}$ must be equally high or equally low.)
(2) Set $OC_{AB}$ high and $\overline{OC_{BA}}$ low respectively.
(3) Remove the data.
(4) The data applied in (1) is stored. If voltage is applied to A or B in this condition, the device may be damaged. Change the status of $OC_{AB}$ or $\overline{OC_{BA}}$ before applying voltage.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | A, B | | −0.5 ~ +5.5 | V |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | | High-level state or high-impedance state | −0.5 ~ +5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20 ~ +75 | °C |
| $T_{stg}$ | Storage temperature range | | | −65 ~ +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $OC_{AB}$, $\overline{OC_{BA}}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | |
| $I_{IH}$ | High-level input current (Note 2) | $OC_{AB}$, $\overline{OC_{BA}}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current (Note 3) | $OC_{AB}$, $\overline{OC_{BA}}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 27 | 40 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 32 | 48 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 37 | 53 | mA |

* : All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: For A and B, $I_{IH}$ includes off-state high-level output current $I_{OZH}$.

Note 3: For A and B, $I_{IL}$ includes off-state low-level output current $I_{OZL}$.

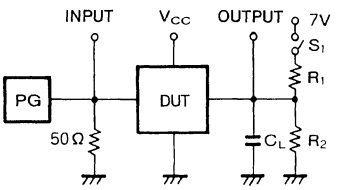
## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Input | Output | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A | B | 3 | 7 | 13 | 3 | 7 | 14 | ns |
| $t_{PHL}$ | | | | 3 | 7 | 11 | 3 | 7 | 12 | |
| $t_{PLH}$ | | B | A | 3 | 7 | 13 | 3 | 7 | 14 | ns |
| $t_{PHL}$ | | | | 3 | 7 | 11 | 3 | 7 | 12 | |
| $t_{PZH}$ | Output enable time | $\overline{OC_{BA}}$ | A | 7 | 12 | 22 | 7 | 12 | 23 | ns |
| $t_{PZL}$ | | | | 7 | 16 | 25 | 7 | 16 | 26 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC_{BA}}$ | A | 2 | 9 | 21 | 2 | 9 | 22 | ns |
| $t_{PLZ}$ | | | | 3 | 12 | 26 | 3 | 12 | 27 | |
| $t_{PZH}$ | Output enable time | $OC_{AB}$ | B | 7 | 13 | 22 | 7 | 13 | 23 | ns |
| $t_{PZL}$ | | | | 7 | 17 | 25 | 7 | 17 | 26 | |
| $t_{PHZ}$ | Output disable time | $OC_{AB}$ | B | 2 | 14 | 21 | 2 | 14 | 22 | ns |
| $t_{PLZ}$ | | | | 3 | 17 | 26 | 3 | 17 | 27 | |

* All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 4. Measurement circuit

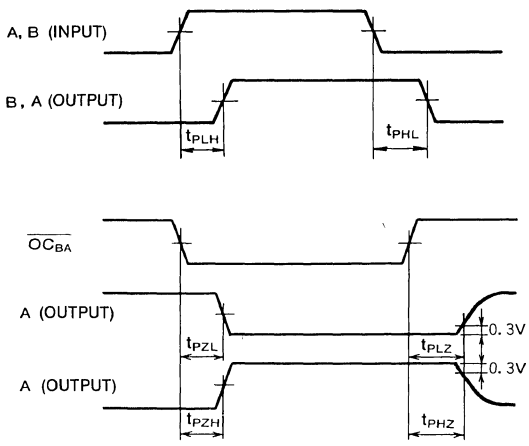


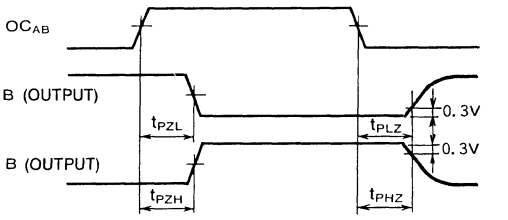

(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

## TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS640P

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS640P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with 3-state inverted outputs.

## FEATURES

- Two-way transmission or isolation between two 8-bit data
- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

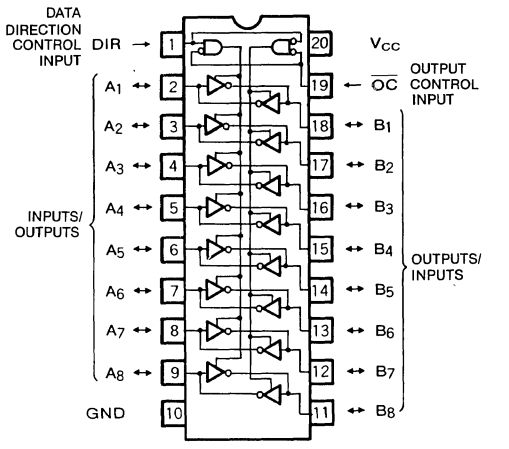
The inputs and outputs are mutually connected to form two-way buffers with 3-state inverted outputs.

The input/output direction is controlled by DIR.

When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins. When $\overline{OC}$ is high, both A and B are in the high-impedance state and A and B are isolated.

The low-power version of M74ALS640P, the M74ALS1640P, is also available.

## PIN CONFIGURATION (TOP VIEW)



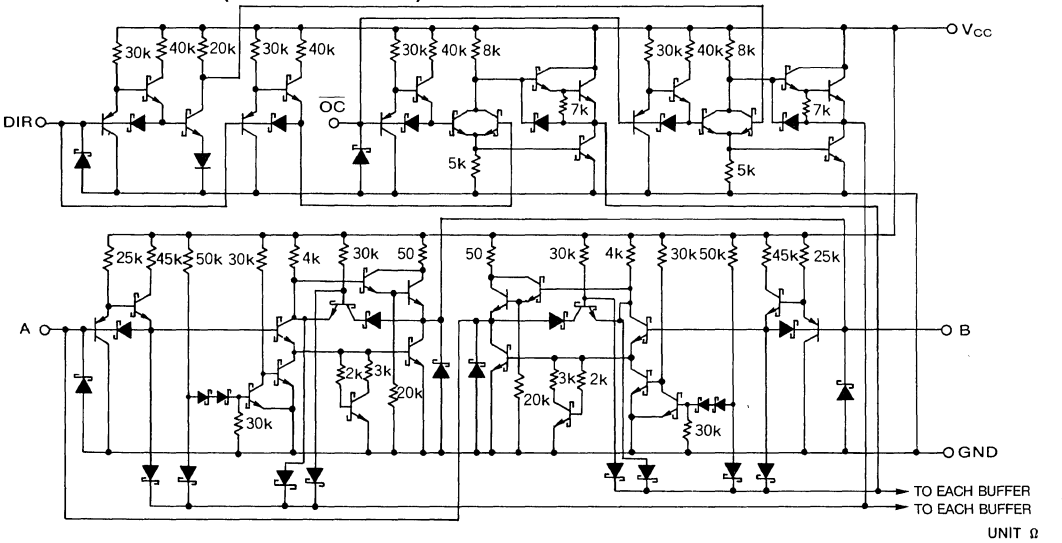

Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Input/Output | |
|---|---|---|---|
| $\overline{OC}$ | DIR | A | B |
| L | L | $\overline{O}$ | I |
| L | H | I | $\overline{O}$ |
| H | X | Z | Z |

Note 1: I Input pins
$\overline{O}$ Output pins (inverted output)
Z High-impedance state (A and B are isolated)
X Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)






MITSUBISHI ELECTRIC

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

### ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+5.5 | V |
| | | DIR, $\overline{OC}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state or high-impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | °C |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

### ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | |
| $I_{IH}$ | High-level input current (Note 2) | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current (Note 3) | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 19 | 32 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 27 | 40 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 28 | 43 | mA |

*: All typical values are at $V_{CC}$=5V, Ta=25°C.

Note 2: For A and B, $I_{IH}$ includes off-state high-level output current $I_{OZH}$.

Note 3: For A and B, $I_{IL}$ includes off-state low-level output current $I_{OZL}$.

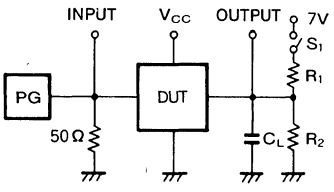
## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A, B | B, A | 2 | 5 | 11 | 2 | 5 | 12 | ns |
| $t_{PHL}$ | | | | 2 | 5 | 10 | 2 | 5 | 11 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | A, B | 5 | 12 | 21 | 5 | 12 | 22 | ns |
| $t_{PZL}$ | | | | 8 | 18 | 24 | 8 | 18 | 25 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | A, B | 3 | 6 | 12 | 3 | 6 | 13 | ns |
| $t_{PLZ}$ | | | | 4 | 7 | 18 | 4 | 7 | 19 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 4: Measurement circuit

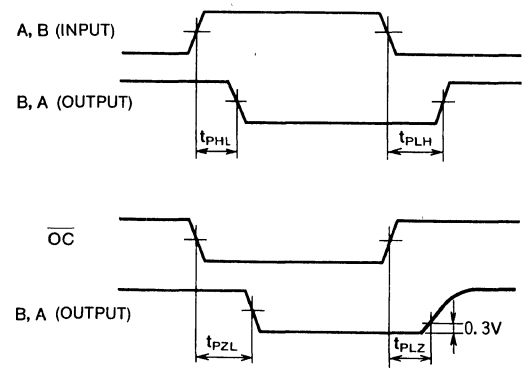


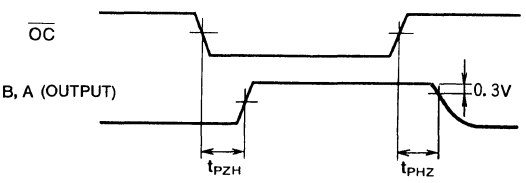

(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS641P

## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS641P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with noninverted open collector outputs.

## FEATURES

- Two-way transmission or isolation between two 8-bit data
- Open collector output
- High fan-out ($I_{OL}$ = 24mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with noninverted open collector outputs.

The input/output direction is controlled by DIR.

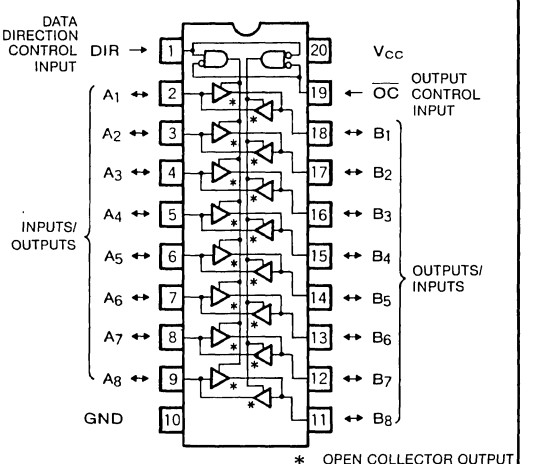
When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins.

When $\overline{OC}$ is high, both A and B become high and A and B are isolated.

The low-power version of M74ALS641P, the M74ALS1641P, is also available.

The functions and pin connections of this device are identical to those of M74ALS645P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.

## PIN CONFIGURATION (TOP VIEW)



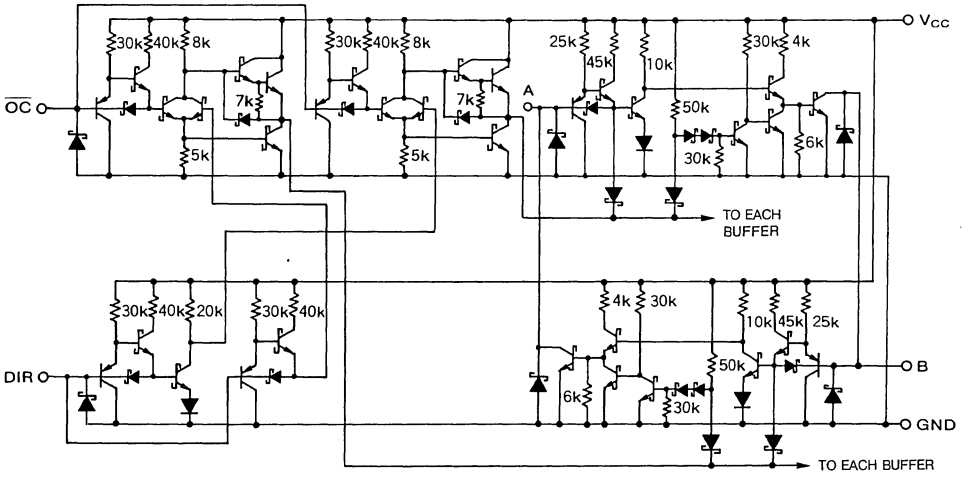

Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC}$ | DIR | A | B |
| L | L | O | I |
| L | H | I | O |
| H | X | H | H |

Note 1: I : Input pins
O : Output pins (noninverted output)
X : Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT: Ω

## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (NONINVERTED)

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+7 | V |
| | | DIR, $\overline{OC}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state | −0.5~+7 | V |
| Topr | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| Tstg | Storage temperature range | | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| Topr | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | DIR, $\overline{OC}$ | $V_{CC}$=5.5V | $V_I$=7V | | | 0.1 | mA |
| | | A, B | | $V_I$=5.5V | | | 0.1 | |
| $I_{IH}$ | High-level input current | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 24 | 33 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 30 | 40 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 33 | 50 | mA |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C

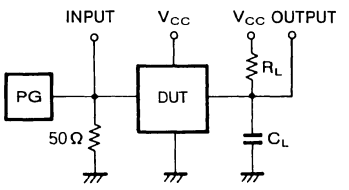
## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (NONINVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_L$=680Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Outputs | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A, B | B, A | 10 | 29 | 38 | 10 | 29 | 39 | ns |
| $t_{PHL}$ | | | | 5 | 13 | 20 | 5 | 13 | 21 | |
| $t_{PLH}$ | | $\overline{OC}$, DIR | A, B | 12 | 18 | 38 | 12 | 18 | 39 | ns |
| $t_{PHL}$ | | | | 13 | 27 | 40 | 13 | 27 | 41 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

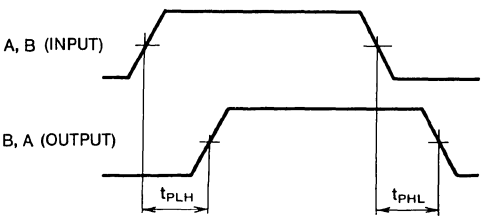
$V_{IH}$=3.5V, $V_{IL}$=0.3V

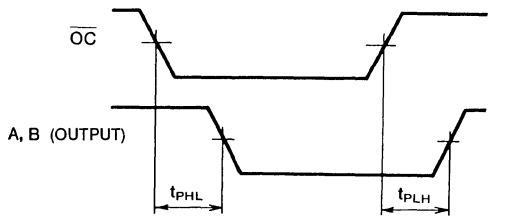
duty cycle=50%

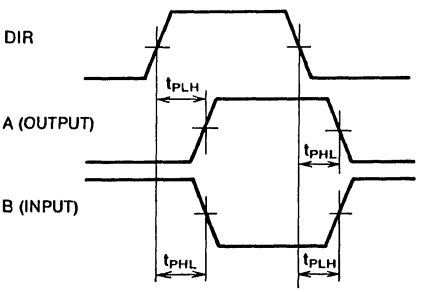
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS642P

## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS642P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with inverted open collector outputs.

## FEATURES

- Two-way transmission or isolation between two 8-bit data
- Open collector output
- High fan-out ($I_{OL}$ = 24mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with inverted open collector outputs.

The input/output direction is controlled by DIR.

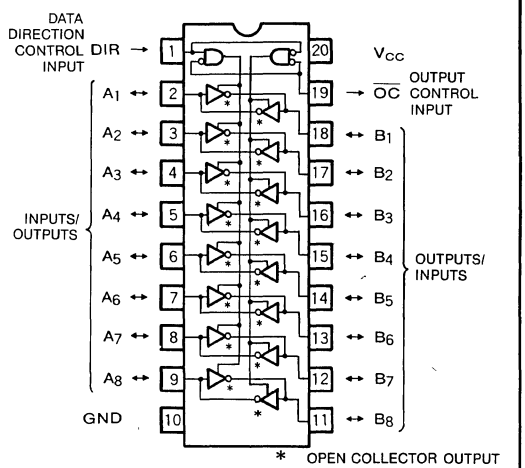
When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins.

When $\overline{OC}$ is high, both A and B become high and A and B are isolated.

The low-power version of M74ALS642P, the M74ALS1642P, is also available.

The functions and pin connections of this device are identical to those of M74ALS640P but since open collector outputs are provided, the high-level output impedance can by freely selected with an external load resistor.

## PIN CONFIGURATION (TOP VIEW)



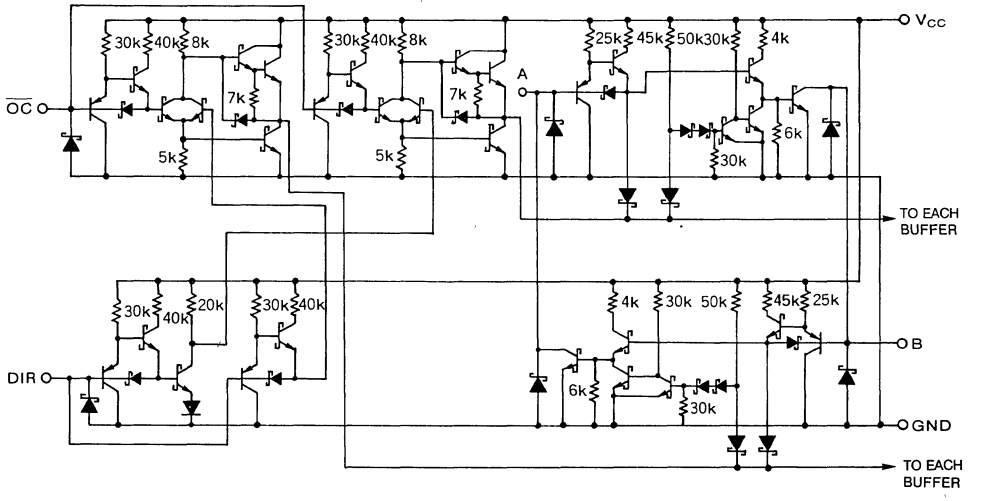

Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC}$ | DIR | A | B |
| L | L | $\overline{O}$ | I |
| L | H | I | $\overline{O}$ |
| H | X | H | H |

Note 1: I : Input pins
$\overline{O}$ : Output pins (inverted output)
X : Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)



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## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+7 | V |
| | | DIR, $\overline{OC}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state | −0.5~+7 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | DIR, $\overline{OC}$ | $V_{CC}$=5.5V | $V_I$=7V | | | 0.1 | mA |
| | | A, B | | $V_I$=5.5V | | | 0.1 | |
| $I_{IH}$ | High-level input current | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 9 | 15 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 15 | 28 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 10 | 16 | mA |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

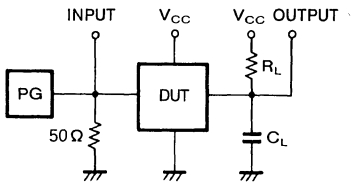
## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_L$=680Ω; $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A, B | B, A | 15 | 21 | 41 | 15 | 21 | 42 | ns |
| $t_{PHL}$ | | | | 5 | 16 | 22 | 5 | 16 | 23 | |
| $t_{PLH}$ | | $\overline{OC}$, DIR | A, B | 10 | 16 | 40 | 10 | 16 | 41 | ns |
| $t_{PHL}$ | | | | 15 | 28 | 50 | 15 | 28 | 51 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2· Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

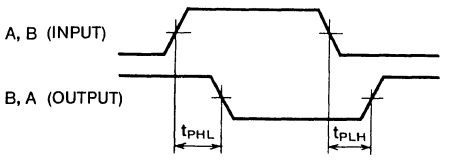
$V_{IH}$=3.5V, $V_{IL}$=0.3V

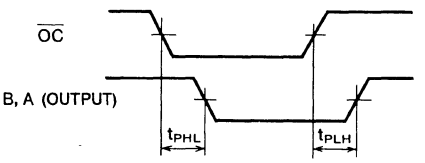
duty cycle=50%

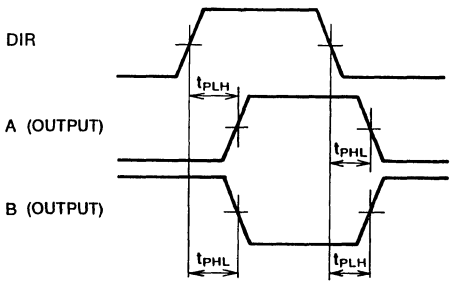
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS643P

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT

## DESCRIPTION

The M74ALS643P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with inverted and noninverted 3-state outputs.

## FEATURES

- Two-way transmission or isolation between two 8-bit data
- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

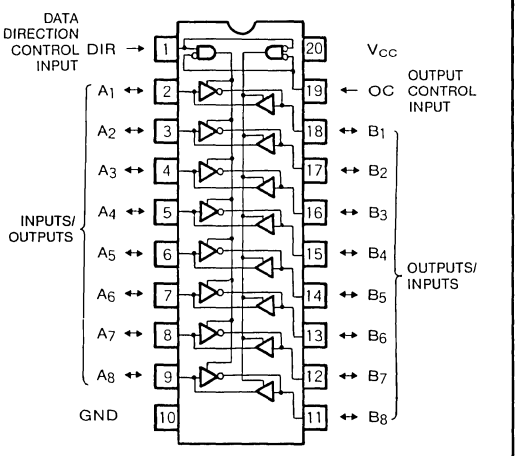
The inputs and outputs are mutually connected to form two-way buffers with inverted and noninverted 3-state outputs.

The input/output direction is controlled by DIR.

When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins. When $\overline{OC}$ is high, both A and B are in the high-impedance state and A and B are isolated.

The low-power version of M74ALS643P, the M74ALS1643P, is also available.

## PIN CONFIGURATION (TOP VIEW)



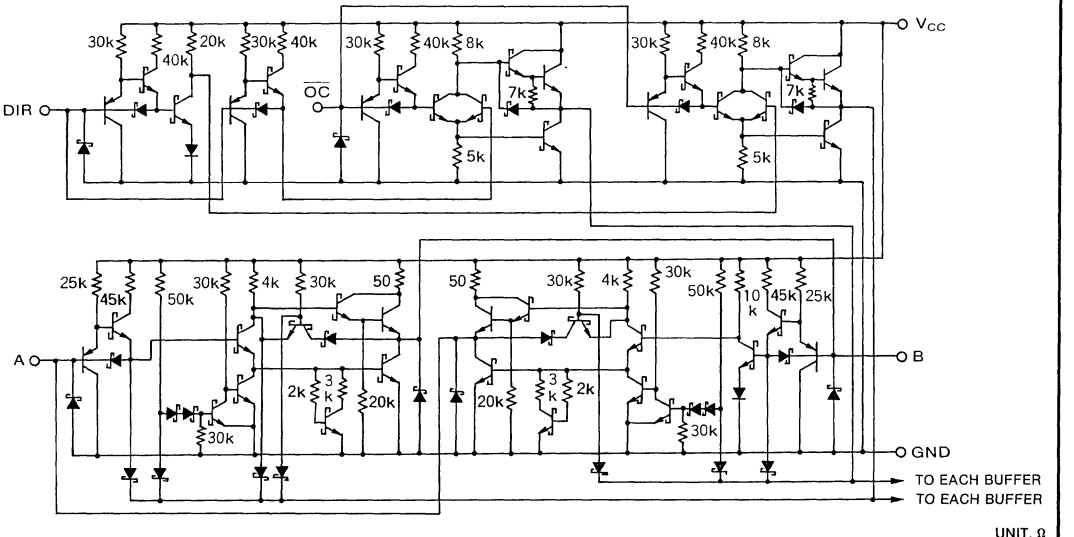

Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC}$ | DIR | A | B |
| L | L | O | I |
| L | H | I | $\overline{O}$ |
| H | X | Z | Z |

Note 1: I Input pins
O Output pins (noninverted output)
$\overline{O}$ Output pins (inverted output)
Z High-impedance state (A and B are isolated)
X Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)



## ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+5.5 | V |
| | | DIR, $\overline{OC}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state or high-impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | DIR, $\overline{OC}$ | $V_{CC}$=5.5V | $V_I$=7V | | | 0.1 | mA |
| | | A, B | | $V_I$=5.5V | | | 0.1 | |
| $I_{IH}$ | High-level input current (Note 2) | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current (Note 3) | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 25 | 35 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 33 | 45 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 35 | 48 | mA |

* : All typical values are at $V_{CC}$ = 5V, Ta = 25°C.

Note 2: For A and B, $I_{IH}$ includes off-state high-level output current $I_{OZH}$.

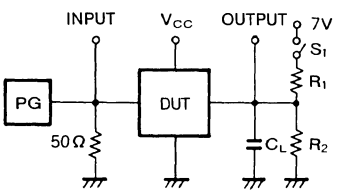
Note 3: For A and B, $I_{IL}$ includes off-state low-level output current $I_{OZL}$.

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Output | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70°C Min | $T_a$=0~70°C Typ * | $T_a$=0~70°C Max | $T_a$=−20~+75°C Min | $T_a$=−20~+75°C Typ * | $T_a$=−20~+75°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A | B | 2 | 5 | 10 | 2 | 5 | 11 | ns |
| $t_{PHL}$ | | | | 2 | 5 | 10 | 2 | 5 | 11 | |
| $t_{PLH}$ | | B | A | 3 | 7 | 11 | 3 | 7 | 12 | ns |
| $t_{PHL}$ | | | | 3 | 7 | 11 | 3 | 7 | 12 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | A | 7 | 12 | 20 | 7 | 12 | 21 | ns |
| $t_{PZL}$ | | | | 10 | 17 | 26 | 10 | 17 | 27 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | A | 3 | 7 | 16 | 3 | 7 | 17 | ns |
| $t_{PLZ}$ | | | | 4 | 10 | 18 | 4 | 10 | 19 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | B | 5 | 10 | 21 | 5 | 10 | 22 | ns |
| $t_{PZL}$ | | | | 8 | 17 | 24 | 8 | 17 | 25 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | B | 3 | 5 | 12 | 3 | 5 | 13 | ns |
| $t_{PLZ}$ | | | | 4 | 7 | 18 | 4 | 7 | 19 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 4: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

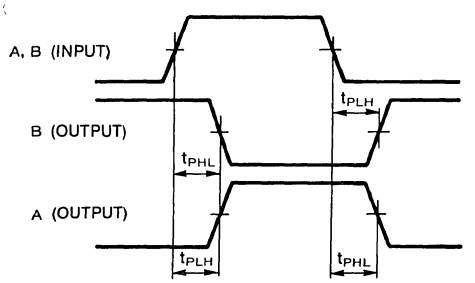
duty cycle=50%

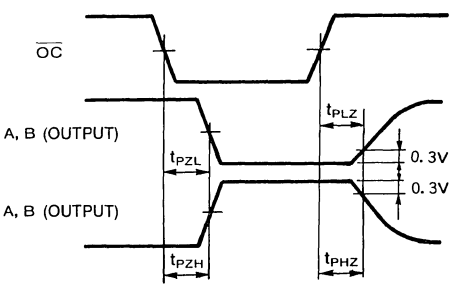
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

## TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS644P

## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

## DESCRIPTION

The M74ALS644P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with inverted and noninverted open collector outputs.

## FEATURES

- Two-way transmission or isolation between two 8-bit data
- Open collector output
- High fan-out ($I_{OL}$ = 24mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with inverted and noninverted open collector outputs.

The input/output direction is controlled by DIR.

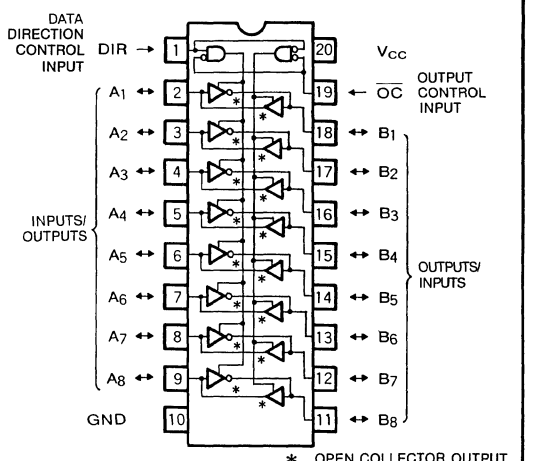
When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins.

When $\overline{OC}$ is high, both A and B become high and A and B are isolated.

The low-power version of M74ALS644P, the M74ALS1644P, is also available.

The functions and pin connections of this device are identical to those of M74ALS643P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.

## PIN CONFIGURATION (TOP VIEW)



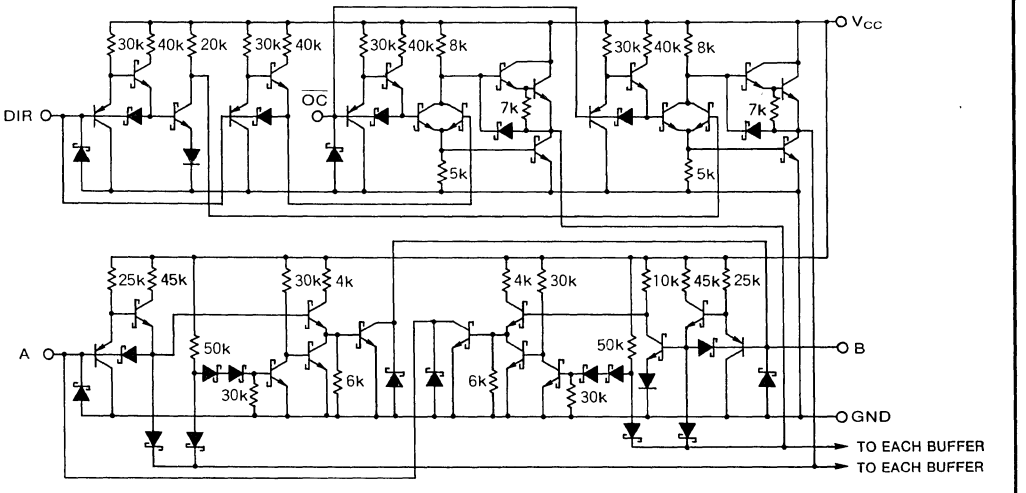

Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC}$ | DIR | A | B |
| L | L | O | I |
| L | H | I | $\overline{O}$ |
| H | X | H | H |

Note 1: I : Input pins
O : Output pins (noninverted output)
$\overline{O}$ : Output pins (inverted output)
X : Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT: Ω



MITSUBISHI ELECTRIC

## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+7 | V |
| | | DIR, $\overline{OC}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state | −0.5~+7 | V |
| Topr | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| Tstg | Storage temperature range | | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| Topr | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | A, B | $V_{CC}$=5.5V | $V_I$=5.5V | | | 0.1 | mA |
| | | DIR, $\overline{OC}$ | | $V_I$=7V | | | 0.1 | |
| $I_{IH}$ | High-level input current | A, B | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | DIR, $\overline{OC}$ | | | | | 20 | |
| $I_{IL}$ | Low-level input current | A, B | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | DIR, $\overline{OC}$ | | | | | −0.1 | |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 16 | 29 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 25 | 40 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 21 | 34 | mA |

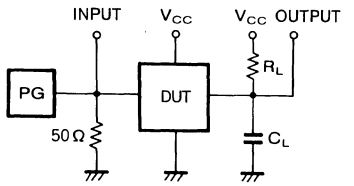
* : All typical values are at $V_{CC}$=5V, $T_a$=25°C.

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Output | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_L$=680Ω; $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A | B | 15 | 24 | 41 | 15 | 24 | 42 | ns |
| $t_{PHL}$ | | | | 5 | 13 | 22 | 5 | 13 | 23 | |
| $t_{PLH}$ | | B | A | 15 | 25 | 41 | 15 | 25 | 42 | ns |
| $t_{PHL}$ | | | | 5 | 12 | 21 | 5 | 12 | 22 | |
| $t_{PLH}$ | | $\overline{OC}$ | A | 12 | 19 | 37 | 12 | 19 | 38 | ns |
| $t_{PHL}$ | | | | 13 | 25 | 40 | 13 | 25 | 41 | |
| $t_{PLH}$ | | $\overline{OC}$ | B | 12 | 15 | 33 | 12 | 15 | 34 | ns |
| $t_{PHL}$ | | | | 15 | 26 | 40 | 15 | 26 | 41 | |
| $t_{PLH}$ | | DIR | A | 10 | 17 | 30 | 10 | 17 | 31 | ns |
| $t_{PHL}$ | | | | 10 | 25 | 35 | 10 | 25 | 36 | |
| $t_{PLH}$ | | DIR | B | 15 | 24 | 45 | 15 | 24 | 46 | ns |
| $t_{PHL}$ | | | | 15 | 28 | 40 | 15 | 28 | 41 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

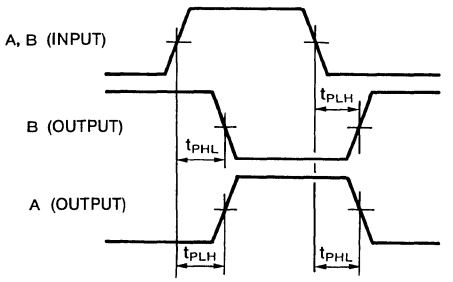
$V_{IH}$=3.5V, $V_{IL}$=0.3V

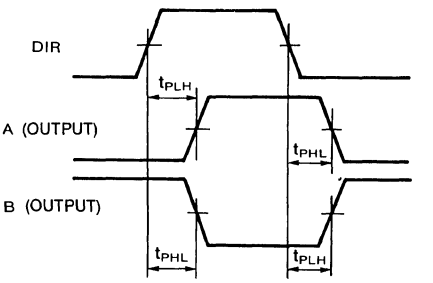
duty cycle=50%

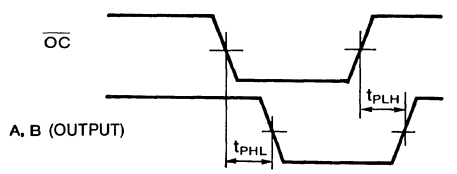
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

## TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS645P

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS645P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with 3-state noninverted outputs.

## FEATURES

- Two-way transmission or isolation between two 8-bit data
- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

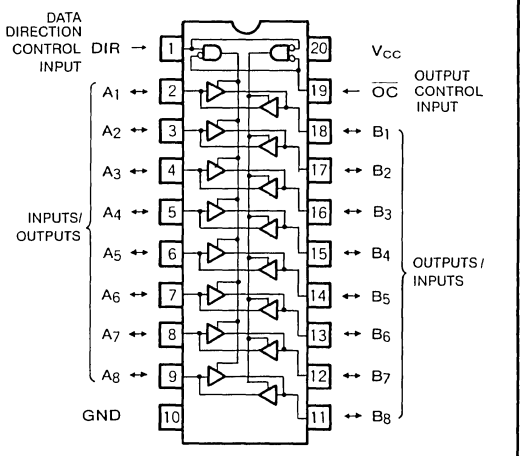
The inputs and outputs are mutually connected to form two-way buffers with 3-state noninverted outputs.

The input/output direction is controlled by DIR.

When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins. When $\overline{OC}$ is high, both A and B are in the high-impedance state and A and B are isolated.

This device is identical in all respects except for its name to the M74ALS245P. The low-power version of M74ALS645P, the M74ALS1645P, is also available.

## PIN CONFIGURATION (TOP VIEW)



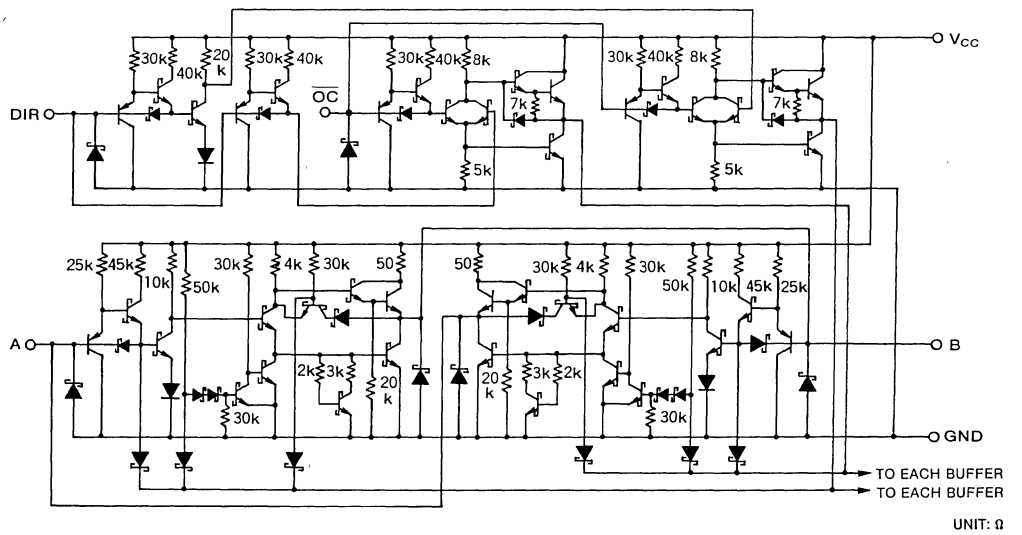

Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Input/Output | |
|---|---|---|---|
| $\overline{OC}$ | DIR | A | B |
| L | L | O | I |
| L | H | I | O |
| H | X | Z | Z |

Note 1: I Input pins
O Output pins (noninverted output)
Z High-impedance state (A and B are isolated)
X Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)



## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | A, B | | −0.5 ~ +5.5 | V |
| | | DIR, $\overline{OC}$ | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | | High-level state or high-impedance state | −0.5 ~ +5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20 ~ +75 | °C |
| $T_{stg}$ | Storage temperature range | | | −65 ~ +150 | °C |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | |
| $I_{IH}$ | High-level input current (Note 2) | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current (Note 3) | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 30 | 45 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 36 | 55 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 38 | 58 | mA |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 2: For A and B, $I_{IH}$ includes off-state high-level output current $I_{OZH}$

Note 3: For A and B, $I_{IL}$ includes off-state low-level output current $I_{OZL}$.

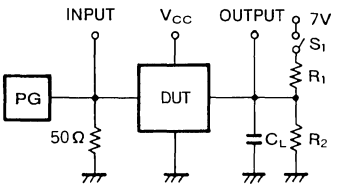
## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70°C Min | Typ * | Max | $T_a$=−20~+75°C Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A, B | B, A | 3 | 7 | 10 | 3 | 7 | 11 | ns |
| $t_{PHL}$ | | | | 3 | 7 | 10 | 3 | 7 | 11 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | A, B | 8 | 14 | 20 | 8 | 14 | 21 | ns |
| $t_{PZL}$ | | | | 10 | 18 | 26 | 10 | 18 | 27 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | A, B | 3 | 7 | 16 | 3 | 7 | 17 | ns |
| $t_{PLZ}$ | | | | 4 | 9 | 18 | 4 | 9 | 19 | |

* All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 4 Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

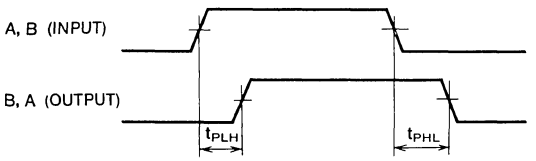
duty cycle=50%

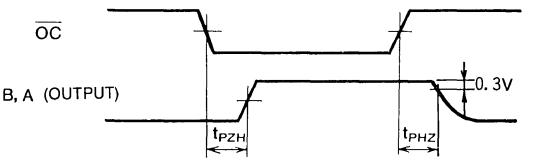
$Z_O$=50Ω

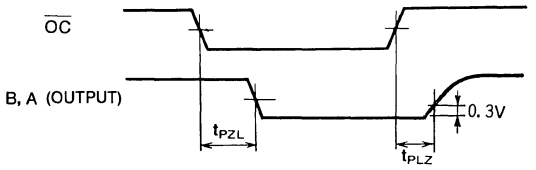
(2) $C_L$ includes probe and jig capacitance

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS873P

## DUAL 4-BIT D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS873P is a semiconductor integrated circuit consisting of two 4-bit D-type latch circuits with 3-state noninverted output. Each of the circuits has an output control input, an enable input, and a direct reset input.

## FEATURES

- 3-state, high fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- 4-bit common output control input and enable input
- 4-bit common direct reset input
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

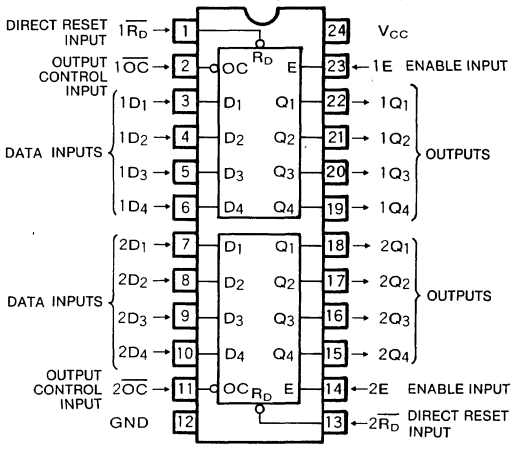
General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Each of the two 4-bit D-type latch circuits has 4-bit common output control $\overline{OC}$, enable input E, and direct reset $\overline{R_D}$. When $\overline{R_D}$ is low, the outputs $Q_1 \sim Q_4$ become low, irrespective of other inputs. While E is high, The information from D appears at the output Q and the Q changes with D. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of Q is retained even if D changes.

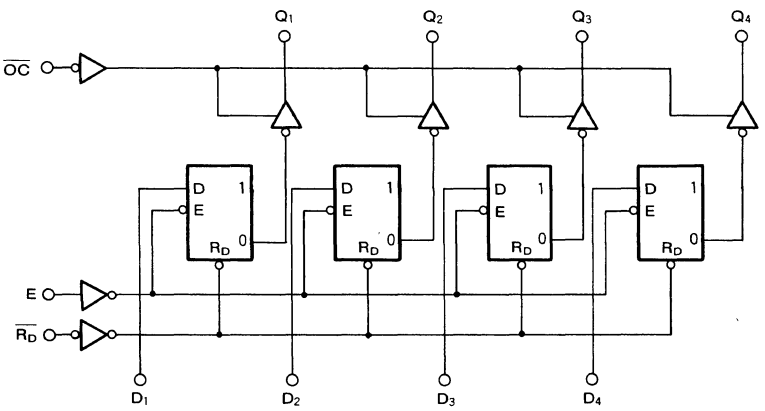
While $\overline{OC}$ is high, $Q_1 \sim Q_4$ are put in the high-impedance state "Z" irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While Q is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

## PIN CONFIGURATION (TOP VIEW)




Outline 24P4D

## LOGIC DIAGRAM (EACH CIRCUIT)






MITSUBISHI ELECTRIC

# M74ALS873P

## DUAL 4-BIT D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (NONINVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | | | Output |
|---|---|---|---|---|
| $\overline{OC}$* | $\overline{R_D}$ | E | D | Q |
| L | L | X | X | L |
| L | H | H | H | H |
| L | H | H | L | L |
| L | H | L | X | $Q^0$ |
| H | X | X | X | Z |

Note 1: $Q^0$ : Level of Q before the indicated steady-state input conditions were established.

Z High-impedance state

X : Irrelevant

* Data can be latched or reset irrespective of $\overline{OC}$.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 10 | 21 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 15 | 29 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | $V_{CC}$=5.5V | | | 16 | 31 | mA |

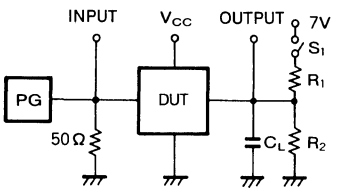
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | $D_1$~$D_4$ | $Q_1$~$Q_4$ | 2 | | 14 | 2 | | 15 | ns |
| $t_{PHL}$ | | | | 2 | | 14 | 2 | | 15 | |
| $t_{PLH}$ | | E | $Q_1$~$Q_4$ | 8 | | 22 | 8 | | 23 | ns |
| $t_{PHL}$ | | | | 8 | | 21 | 8 | | 22 | |
| $t_{PHL}$ | | $\overline{R_D}$ | $Q_1$~$Q_4$ | 6 | | 24 | 6 | | 25 | ns |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | $Q_1$~$Q_4$ | 4 | | 20 | 4 | | 21 | ns |
| $t_{PZL}$ | | | | 4 | | 18 | 4 | | 19 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | $Q_1$~$Q_4$ | 2 | | 8 | 2 | | 9 | ns |
| $t_{PLZ}$ | | | | 2 | | 13 | 2 | | 14 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

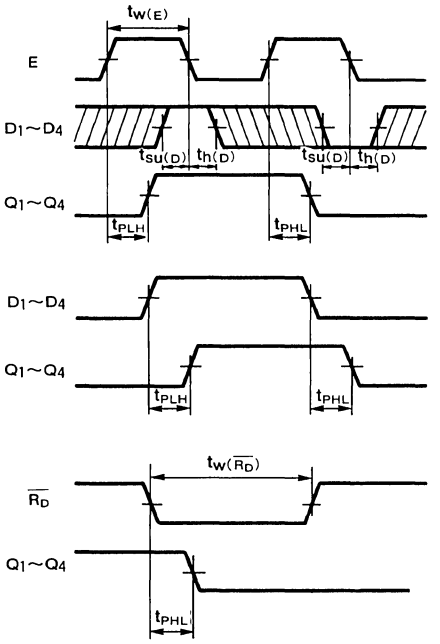
## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

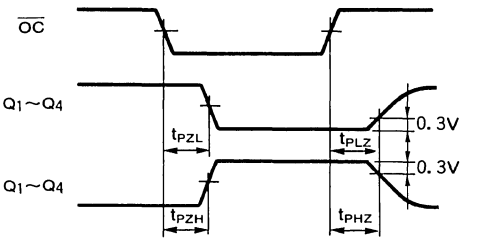
| Symbol | Parameter | | Limits: $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{W(\overline{R_D})}$ | Pulse width | $\overline{R_D}$ "L" | 15 | | | 16 | | | ns |
| $t_{W(E)}$ | | E "H" | 15 | | | 16 | | | |
| $t_{su(D)}$ | Setup time before E ↓ | $D_1$~$D_4$ | 10 | | | 11 | | | ns |
| $t_{h(D)}$ | Hold time after E ↓ | $D_1$~$D_4$ | 7 | | | 8 | | | ns |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↓: Transition from high to low

## TIMING DIAGRAM (Reference level = 1.3V)




Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS874P

## DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS874P is a semiconductor integrated circuit consisting of two 4-bit D-type positive edge-triggered flip-flop circuits with 3-state noninverted output. Each of the circuits has an output control input, a clock input, and a direct reset input.

## FEATURES

- Positive edge triggering
- 3-state, high fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- 4-bit common output control input and clock input
- 4-bit common direct reset input
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

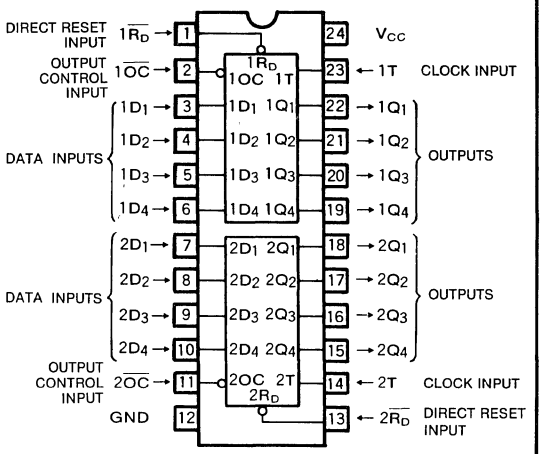
General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Each of the two internal 4-bit D-type edge-triggered flip-flop circuits has 4-bit common output control $\overline{OC}$, clock input T, and direct reset input $\overline{R_D}$. When T changes from low to high, the status of D immediately before the change appears at the output Q in accordance with the function table. When $\overline{R_D}$ is low, the outputs $Q_1 \sim Q_4$ become low, irrespective of other inputs.

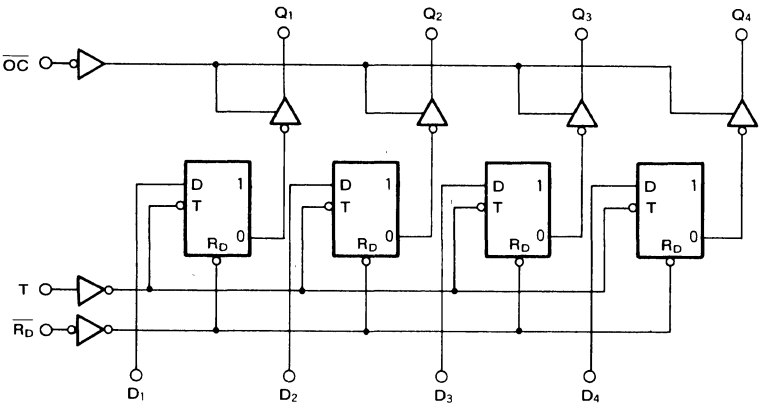
While $\overline{OC}$ is high, $Q_1 \sim Q_4$ are in the high-impedance state "Z" irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While Q is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

## PIN CONFIGURATION (TOP VIEW)




Outline 24P4D

## LOGIC DIAGRAM (EACH CIRCUIT)






MITSUBISHI ELECTRIC

# DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT (NONINVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | | | Output |
|---|---|---|---|---|
| $\overline{OC}$* | $\overline{R_D}$ | T | D | Q |
| L | L | X | X | L |
| L | H | ↑ | H | H |
| L | H | ↑ | L | L |
| L | H | L | X | $Q^0$ |
| H | X | X | X | Z |

Note 1: ↑ : Transition from low to high level (positive edge trigger)

$Q^0$ : Level of Q before the indicated steady-state input conditions were established.

Z High-impedance state

X : Irrelevant

* . Data can be stored or reset irrespective of $\overline{OC}$.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 14 | 21 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 18 | 29 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | $V_{CC}$=5.5V | | | 20 | 31 | mA |

* All typical values are at $V_{CC}$=5V, $T_a$=25°C.

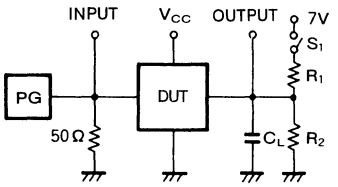
## DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT (NONINVERTED)

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | $T_a$=0~70℃ Typ * | $T_a$=0~70℃ Max | $T_a$=−20~+75℃ Min | $T_a$=−20~+75℃ Typ * | $T_a$=−20~+75℃ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | T | $Q_1$~$Q_4$ | 30 | | | 28 | | | MHz |
| $t_{PLH}$ | Propagation time | T | $Q_1$~$Q_4$ | 4 | | 14 | 4 | | 15 | ns |
| $t_{PHL}$ | | | | 4 | | 14 | 4 | | 15 | |
| $t_{PHL}$ | | $\overline{R_D}$ | $Q_1$~$Q_4$ | 6 | | 24 | 6 | | 25 | ns |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | $Q_1$~$Q_4$ | 4 | | 20 | 4 | | 21 | ns |
| $t_{PZL}$ | | | | 4 | | 18 | 4 | | 19 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | $Q_1$~$Q_4$ | 2 | | 8 | 2 | | 9 | ns |
| $t_{PLZ}$ | | | | 3 | | 13 | 3 | | 14 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

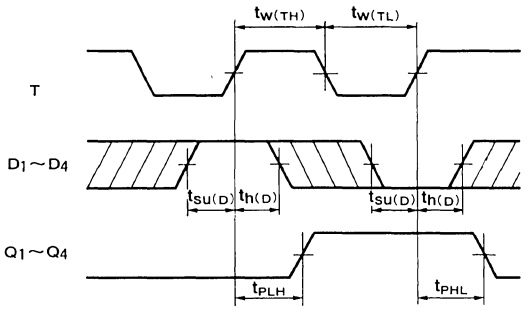
## TIMING REQUIREMENTS ($V_{CC}$=4.5~5.5V, $C_L$=50pF, $R_2$=500Ω)

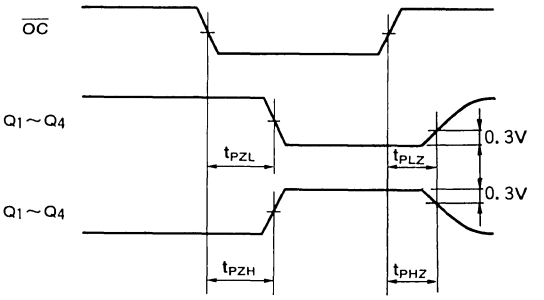
| Symbol | Parameter | | Limits: $T_a$=0~70℃ Min | $T_a$=0~70℃ Typ * | $T_a$=0~70℃ Max | $T_a$=−20~+75℃ Min | $T_a$=−20~+75℃ Typ * | $T_a$=−20~+75℃ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{w(\overline{RD})}$ | Pulse width | $\overline{R_D}$ "L" | 10 | | | 11 | | | ns |
| $t_{w(TH)}$ | | T "H" | 16.5 | | | 17.5 | | | |
| $t_{w(TL)}$ | | T "L" | 16.5 | | | 17.5 | | | |
| $t_{su(D)}$ | Setup time before T↑ | $D_1$~$D_4$ | 15 | | | 16 | | | ns |
| $t_{su(\overline{RD})}$ | | $\overline{R_D}$ "H" (inactive) | 10 | | | 11 | | | |
| $t_{h(D)}$ | Hold time after T↑ | $D_1$~$D_4$ | 0 | | | 1 | | | ns |

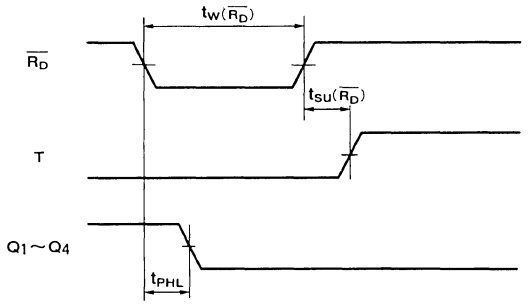
*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↑: Transition from low to high

## TIMING DIAGRAM (Reference level = 1.3V)




Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

PRELIMINARY
Notice This is not a final specification
Some parametric limits are subject to change

# M74ALS876P

## DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS876P is a semiconductor integrated circuit consisting of two 4-bit D-type positive edge-triggered flip-flop circuits with 3-state inverted output. Each of the circuits has an output control input, a clock input, and a direct set input.

## FEATURES

- Positive edge triggering
- 3-state, high fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- 4-bit common output control input and clock input
- 4-bit common direct set input
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

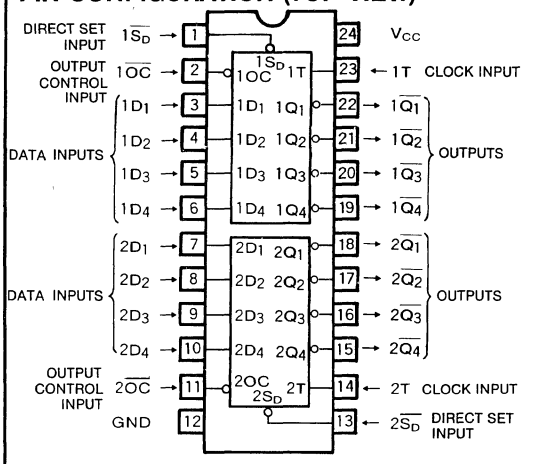
General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Each of the two 4-bit D-type edge-triggered flip-flop circuits have 4-bit common output control $\overline{OC}$, clock input T, and direct set input $\overline{S_D}$. When T changes from low to high, the status of D immediately before the change appears inverted at the output $\overline{Q}$ in accordance with the function table. When $\overline{S_D}$ is low, the outputs $\overline{Q_1} \sim \overline{Q_4}$ become low, irrespective of other inputs.

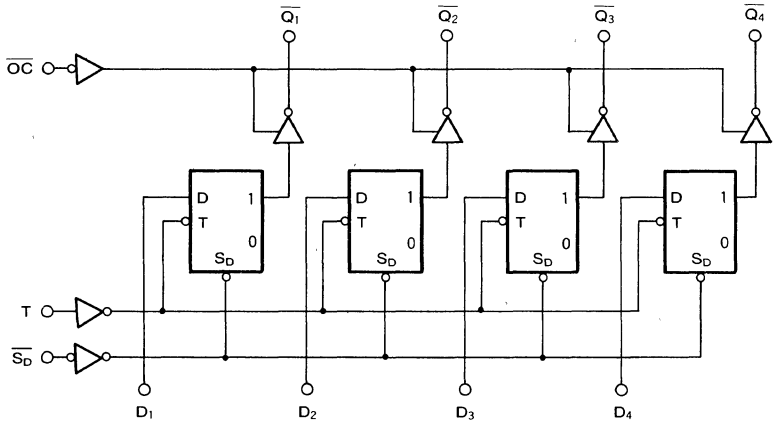
While $\overline{OC}$ is high, $\overline{Q_1} \sim \overline{Q_4}$ are in the high-impedance state "Z", irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While $\overline{Q}$ is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

## PIN CONFIGURATION (TOP VIEW)




Outline 24P4D

## LOGIC DIAGRAM (EACH CIRCUIT)






MITSUBISHI ELECTRIC

# DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT (INVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | | | Output |
|---|---|---|---|---|
| $\overline{OC}$* | $\overline{S_D}$ | T | D | $\overline{Q}$ |
| L | L | X | X | L |
| L | H | ↑ | H | L |
| L | H | ↑ | L | H |
| L | H | L | X | $\overline{Q^0}$ |
| H | X | X | X | Z |

Note 1: ↑ : Transition from low to high level (positive edge trigger)

$\overline{Q^0}$ : Level of $\overline{Q}$ before the indicated steady-state input conditions were established.

Z : High-impedance state

X : Irrelevant

* : Data can be stored or set irrespective of $\overline{OC}$.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 14 | 21 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 18 | 29 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | $V_{CC}$=5.5V | | | 20 | 31 | mA |

* : All typical values are at $V_{CC}$=5V, $T_a$=25°C

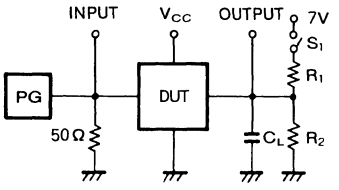
# DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT (INVERTED)

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Test conditions/Limits | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω | | | | | | | | |
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Input | Outputs | Min | Typ * | Max | Min | Typ * | Max | |
| $f_{max}$ | Maximum clock frequency | T | $\overline{Q_1}$~$\overline{Q_4}$ | 30 | | | 28 | | | MHz |
| $t_{PLH}$ | Propagation time | T | $\overline{Q_1}$~$\overline{Q_4}$ | 4 | | 14 | 4 | | 15 | ns |
| $t_{PHL}$ | | | | 4 | | 14 | 4 | | 15 | |
| $t_{PHL}$ | | $\overline{S_D}$ | $\overline{Q_1}$~$\overline{Q_4}$ | 6 | | 24 | 6 | | 25 | ns |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | $\overline{Q_1}$~$\overline{Q_4}$ | 4 | | 20 | 4 | | 21 | ns |
| $t_{PZL}$ | | | | 4 | | 18 | 4 | | 19 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | $\overline{Q_1}$~$\overline{Q_4}$ | 2 | | 8 | 2 | | 9 | ns |
| $t_{PLZ}$ | | | | 3 | | 13 | 3 | | 14 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2. Measurement circuit




(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

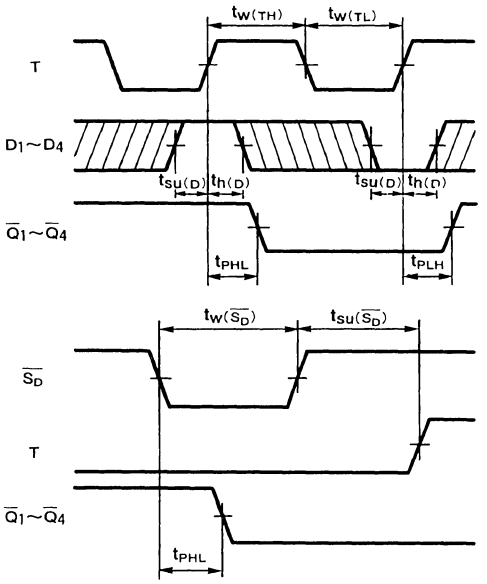
## TIMING REQUIREMENTS ($V_{CC}$=4.5~5.5V, $C_L$=50pF, $R_2$=500Ω)

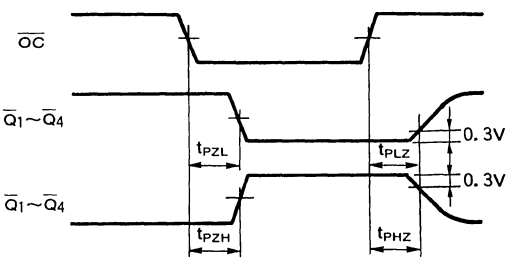
| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{w(\overline{SD})}$ | Pulse width | $\overline{S_D}$ "L" | 10 | | | 11 | | | ns |
| $t_{w(TH)}$ | | T "H" | 16.5 | | | 17.5 | | | |
| $t_{w(TL)}$ | | T "L" | 16.5 | | | 17.5 | | | |
| $t_{su(D)}$ | Setup time before T↑ | $D_1$~$D_4$ | 15 | | | 16 | | | ns |
| $t_{su(\overline{SD})}$ | | $\overline{S_D}$ "H" (inactive) | 10 | | | 11 | | | |
| $t_{h(D)}$ | Hold time after T↑ | $D_1$~$D_4$ | 0 | | | 1 | | | ns |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↑: Transition from low to high

## TIMING DIAGRAM (Reference level = 1.3V)




Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS878P

PRELIMINARY
Notice This is not a final specification
Some parametric limits are subject to change

## DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT AND SYNCHRONOUS RESET (NONINVERTED)

## DESCRIPTION

The M74ALS878P is a semiconductor integrated circuit consisting of two 4-bit D-type positive edge-triggered flip-flop circuits with 3-state noninverted output. Each of the circuits has an output control input, a clock input, and a direct reset input.

## FEATURES

- Positive edge triggering
- 3-state, high fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- 4-bit common output control input and clock input
- 4-bit common reset input
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

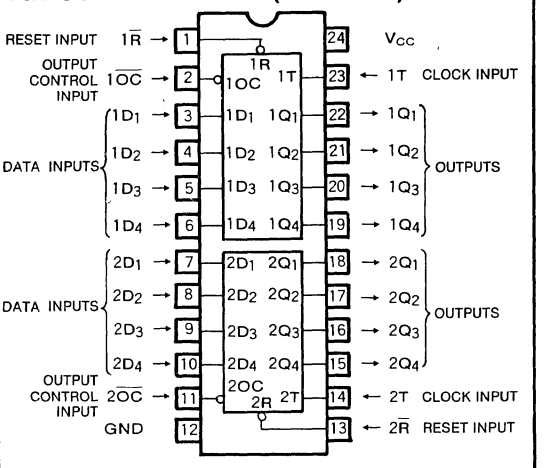
General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Each of the two 4-bit D-type edge-triggered flip-flop circuits has 4-bit common output control $\overline{OC}$, clock input T, and reset input $\overline{R}$ which is synchronized with T. When T changes from low to high, the status of D immediately before the change appears at the output Q in accordance with the function table. When $\overline{R}$ is set low and T changes from low to high, the outputs $Q_1 \sim Q_4$ become low.

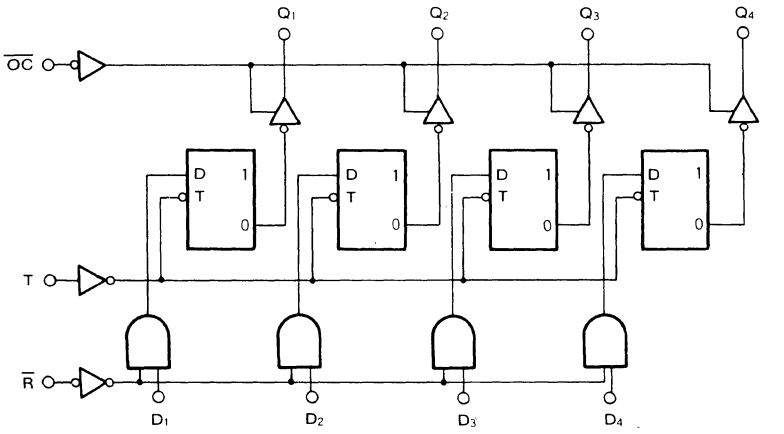
While $\overline{OC}$ is high, $Q_1 \sim Q_4$ are in the high-impedance state "Z", irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While Q is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

## PIN CONFIGURATION (TOP VIEW)




Outline 24P4D

## LOGIC DIAGRAM (EACH CIRCUIT)



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# DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT AND SYNCHRONOUS RESET (NONINVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | | | Output |
|---|---|---|---|---|
| $\overline{OC}$* | $\overline{R}$ | T | D | Q |
| L | L | ↑ | X | L |
| L | H | ↑ | H | H |
| L | H | ↑ | L | L |
| L | H | L | X | $Q^0$ |
| H | X | X | X | Z |

Note 1: ↑ : Transition from low to high level (positive edge trigger)
$Q^0$ : Level of Q before the indicated steady-state input conditions were established.
Z : High-impedance state
X : Irrelevant
* : Data can be stored or reset irrespective of $\overline{OC}$.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5 ~ +5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 ~ +75 | °C |
| $T_{stg}$ | Storage temperature range | | −65 ~ +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 14 | 21 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 18 | 29 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | $V_{CC}$=5.5V | | | 20 | 31 | mA |

* All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

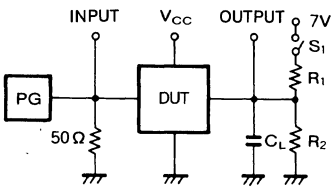
# DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT AND SYNCHRONOUS RESET (NONINVERTED)

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | T | $Q_1$~$Q_4$ | 30 | | | 28 | | | MHz |
| $t_{PLH}$ | Propagation time | T | $Q_1$~$Q_4$ | 4 | | 14 | 4 | | 15 | ns |
| $t_{PHL}$ | | | | 4 | | 16 | 4 | | 17 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | $Q_1$~$Q_4$ | 4 | | 20 | 4 | | 21 | ns |
| $t_{PZL}$ | | | | 4 | | 20 | 4 | | 21 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | $Q_1$~$Q_4$ | 2 | | 10 | 2 | | 11 | ns |
| $t_{PLZ}$ | | | | 3 | | 13 | 3 | | 14 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

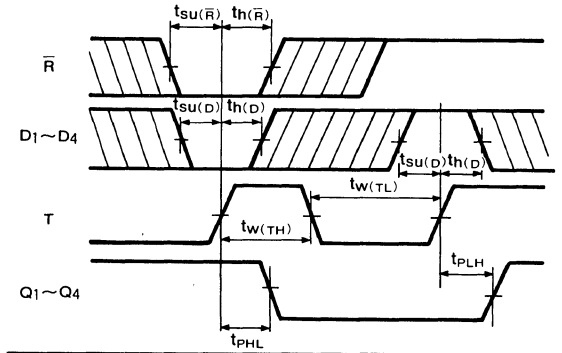
## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

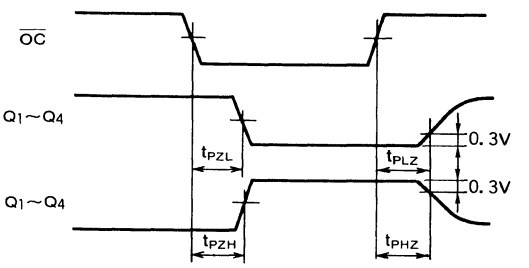
| Symbol | Parameter | | Limits: $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{w(TH)}$ | Pulse width | T "H" | 16.5 | | | 17.5 | | | ns |
| $t_{w(TL)}$ | | T "L" | 16.5 | | | 17.5 | | | |
| $t_{su(D)}$ | Setup time before T↑ | $D_1$~$D_4$ | 15 | | | 16 | | | ns |
| $t_{su(\overline{R})}$ | | $\overline{R}$ "L" | 20 | | | 21 | | | |
| $t_{h(D)}$ | Hold time after T↑ | $D_1$~$D_4$ | 4 | | | 5 | | | ns |
| $t_{h(\overline{R})}$ | | $\overline{R}$ "L" | 0 | | | 1 | | | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↑ : Transition from low to high

## TIMING DIAGRAM (Reference level = 1.3V)




Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.



MITSUBISHI ELECTRIC

# M74ALS879P

## DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT AND SYNCHRONOUS RESET (NONINVERTED)

## DESCRIPTION

The M74ALS879P is a semiconductor integrated circuit consisting of two 4-bit D-type positive edge-triggered flip-flop circuits with 3-state noninverted output. Each of the circuits has an output control input, a clock input, and a reset input.

## FEATURES

- Positive edge triggering
- 3-state, high fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- 4-bit common output control input and clock input
- 4-bit common reset input
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

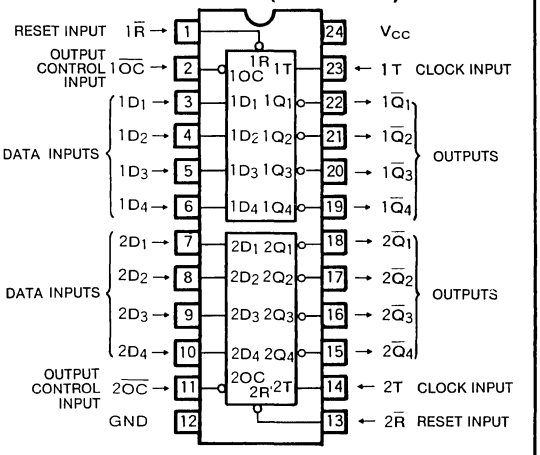
General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Each of the two 4-bit D-type edge-triggered flip-flop circuits has 4-bit common output control $\overline{OC}$, clock input T, and reset input $\overline{R}$ which is synchronized with T. When T changes from low to high, the status of D immediately before the change appears at the output $\overline{Q}$ in accordance with the function table. When $\overline{R}$ is low and T changes from low to high, the outputs $\overline{Q}_1 \sim \overline{Q}_4$ become low.

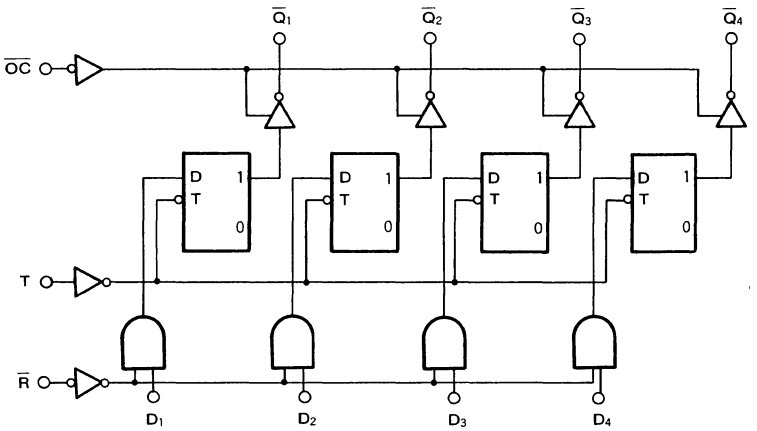
While $\overline{OC}$ is high, $\overline{Q}_1 \sim \overline{Q}_4$ are in the high-impedance state "Z", irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While $\overline{Q}$ is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

## PIN CONFIGURATION (TOP VIEW)




Outline 24P4D

## LOGIC DIAGRAM (EACH CIRCUIT)



# DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT AND SYNCHRONOUS RESET (NONINVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | | | Output |
|---|---|---|---|---|
| $\overline{OC}$* | $\overline{R}$ | T | D | $\overline{Q}$ |
| L | L | ↑ | X | H |
| L | H | ↑ | H | L |
| L | H | ↑ | L | H |
| L | H | L | X | $\overline{Q}^0$ |
| H | X | X | X | Z |

Note 1: ↑ : Transition from low to high level (positive edge trigger)
$\overline{Q}^0$ : Level of Q before the indicated steady-state input conditions were established.
Z : High-impedance state
X : Irrelevant
* : Data can be stored or reset irrespective of $\overline{OC}$.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5 ~ +5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 ~ +75 | °C |
| $T_{stg}$ | Storage temperature range | | −65 ~ +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 14 | 21 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 18 | 29 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | $V_{CC}$=5.5V | | | 20 | 31 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

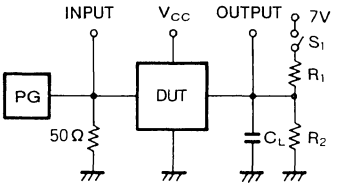
# DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUT AND SYNCHRONOUS RESET (NONINVERTED)

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | input | Outputs | Min | Typ * | Max | Min | Typ * | Max | |
| $f_{max}$ | Maximum clock frequency | T | $\overline{Q_1}$~$\overline{Q_4}$ | 30 | | | 28 | | | MHz |
| $t_{PLH}$ | Propagation time | T | $\overline{Q_1}$~$\overline{Q_4}$ | 4 | | 14 | 4 | | 15 | ns |
| $t_{PHL}$ | | | | 4 | | 16 | 4 | | 17 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | $\overline{Q_1}$~$\overline{Q_4}$ | 4 | | 20 | 4 | | 21 | ns |
| $t_{PZL}$ | | | | 4 | | 20 | 4 | | 21 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | $\overline{Q_1}$~$\overline{Q_4}$ | 2 | | 10 | 2 | | 11 | ns |
| $t_{PLZ}$ | | | | 3 | | 13 | 3 | | 14 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2 Measurement circuit




(1) The pulse generator (PG) has the following characteristics.

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

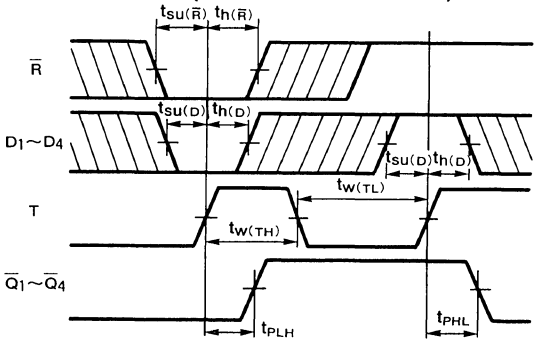
## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

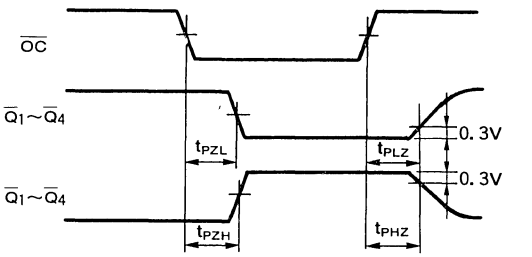
| Symbol | Parameter | | Limits: $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{w(TH)}$ | Pulse width | T "H" | 16.5 | | | 17.5 | | | ns |
| $t_{w(TL)}$ | | T "L" | 16.5 | | | 17.5 | | | |
| $t_{su(D)}$ | Setup time before T↑ | $D_1$~$D_4$ | 15 | | | 16 | | | ns |
| $t_{su(\overline{R})}$ | | $\overline{R}$ "L" | 20 | | | 21 | | | |
| $t_{h(D)}$ | Hold time after T↑ | $D_1$~$D_4$ | 4 | | | 5 | | | ns |
| $t_{h(\overline{R})}$ | | $\overline{R}$ "L" | 0 | | | 1 | | | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C

↑: Transition from low to high (positive edge trigger)

## TIMING DIAGRAM (Reference level = 1.3V)




Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS880P

## DUAL 4-BIT D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS880P is a semiconductor integrated circuit consisting of two 4-bit D-type latch circuits with 3-state inverted output. Each of the circuits has an output control input, an enable input, and a direct set input.

## FEATURES

- 3-state, high fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- 4-bit common output control input and enable input
- 4-bit common direct set input
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

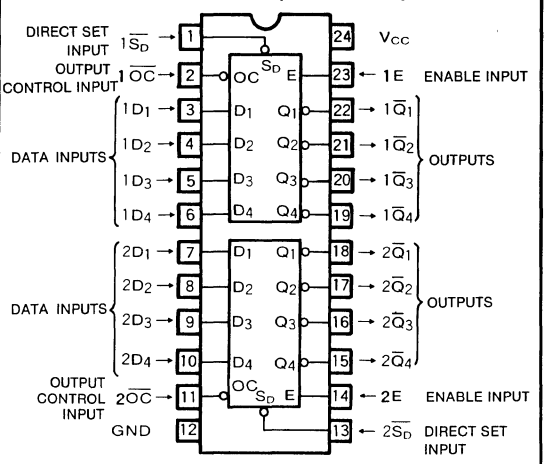
General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Each of the two 4-bit D-type latch circuits has 4-bit common output control $\overline{OC}$, enable input E, and direct set input $\overline{S_D}$. When $\overline{S_D}$ is low, the outputs $\overline{Q_1} \sim \overline{Q_4}$ become low, irrespective of other inputs. While E is high, the information from D appears inverted at the output $\overline{Q}$ and the $\overline{Q}$ changes with D. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of $\overline{Q}$ is retained even if D changes.

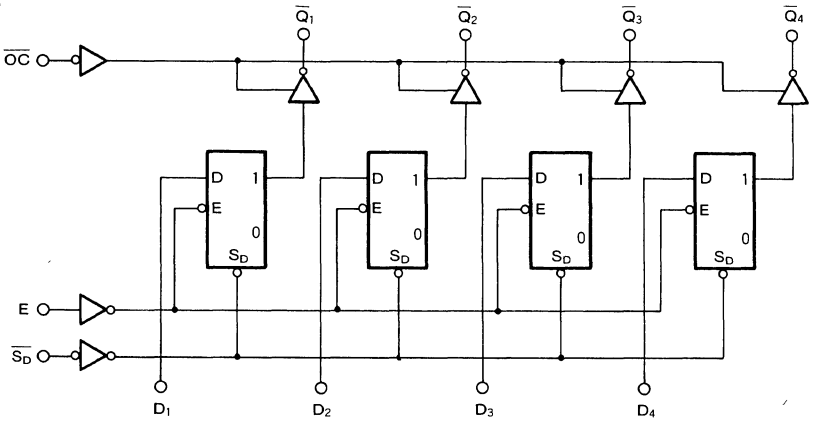
While $\overline{OC}$ is high, $\overline{Q_1} \sim \overline{Q_4}$ are put in the high-impedance state "Z" irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While $\overline{Q}$ is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

## PIN CONFIGURATION (TOP VIEW)




Outline 24P4D

## BLOCK DIAGRAM (EACH CIRCUIT)



# DUAL 4-BIT D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (INVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | | | Output |
|---|---|---|---|---|
| $\overline{OC}$* | $\overline{S_D}$ | E | D | $\overline{Q}$ |
| L | L | X | X | L |
| L | H | H | H | L |
| L | H | H | L | H |
| L | H | L | X | $\overline{Q}^0$ |
| H | X | X | X | Z |

Note 1: $\overline{Q}^0$ : Level of $\overline{Q}$ before the indicated steady-state input conditions were established.

Z : High-impedance state

X : Irrelevant

* : Data can be latched or set irrespective of $\overline{OC}$

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 14 | 21 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 19 | 29 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | $V_{CC}$=5.5V | | | 20 | 31 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

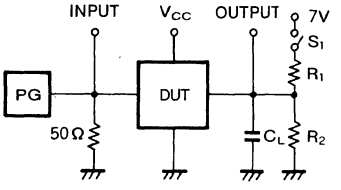
# DUAL 4-BIT D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (INVERTED)

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | $D_1$~$D_4$ | $\overline{Q_1}$~$\overline{Q_4}$ | 3 | | 20 | 3 | | 21 | ns |
| $t_{PHL}$ | | | | 3 | | 14 | 3 | | 15 | |
| $t_{PLH}$ | | E | $\overline{Q_1}$~$\overline{Q_4}$ | 8 | | 24 | 8 | | 25 | ns |
| $t_{PHL}$ | | | | 8 | | 21 | 8 | | 22 | |
| $t_{PHL}$ | | $\overline{S_D}$ | $\overline{Q_1}$~$\overline{Q_4}$ | 6 | | 24 | 6 | | 25 | ns |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | $\overline{Q_1}$~$\overline{Q_4}$ | 5 | | 20 | 5 | | 21 | ns |
| $t_{PZL}$ | | | | 5 | | 18 | 5 | | 19 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | $\overline{Q_1}$~$\overline{Q_4}$ | 2 | | 8 | 2 | | 9 | ns |
| $t_{PLZ}$ | | | | 3 | | 13 | 3 | | 14 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

## TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_2$=500Ω)

| Symbol | Parameter | | Limits: $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{w(\overline{SD})}$ | Pulse width | $\overline{S_D}$ "L" | 15 | | | 16 | | | ns |
| $t_{w(E)}$ | | E "H" | 15 | | | 16 | | | |
| $t_{su(D)}$ | Setup time before E↓ | $D_1$~$D_4$ | 10 | | | 11 | | | ns |
| $t_{h(D)}$ | Hold time after E↓ | $D_1$~$D_4$ | 10 | | | 11 | | | ns |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↓: Transition from high to low



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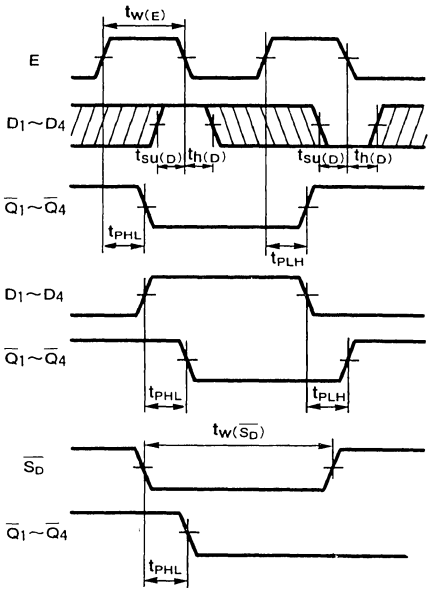
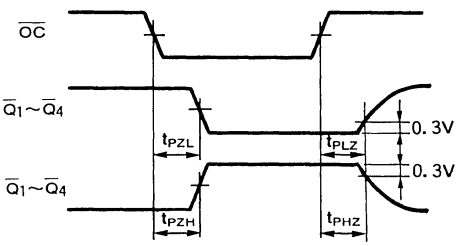
## TIMING DIAGRAM (Reference level = 1.3V)




Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

# M74ALS1000P

## QUADRUPLE 2-INPUT POSITIVE NAND BUFFER

## DESCRIPTION

The M74ALS1000P is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND buffer gates, usable as negative-logic NOR buffer gates.

## FEATURES

- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High speed ($t_{pd}$ = 5ns typical: $C_L$ = 50pF)
- Low power dissipation ($P_d$ = 12.2mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS1000P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

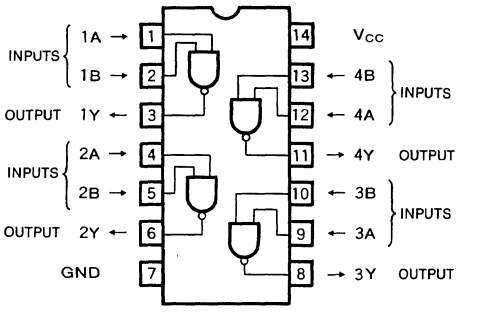
When both A and B inputs are high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

The M74ALS37P, which, except for its name, is identical in all respects to the M74ALS1000P, is also available.

## FUNCTION TABLE

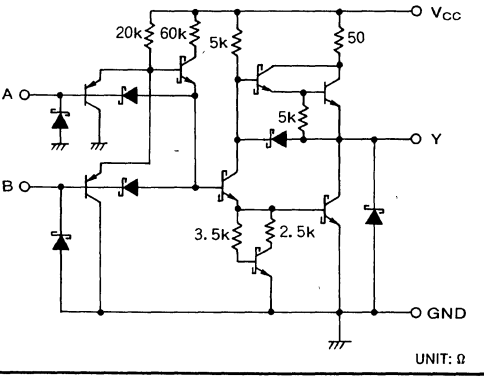
| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT: Ω

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | High-level state | −0.5 ~ $V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 ~ +75 | °C |
| $T_{stg}$ | Storage temperature range | | −65 ~ +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |



MITSUBISHI ELECTRIC

## QUADRUPLE 2-INPUT POSITIVE NAND BUFFER

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.86 | 1.6 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 4 | 6.4 | mA |

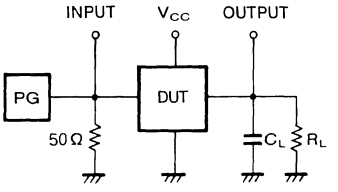
* All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

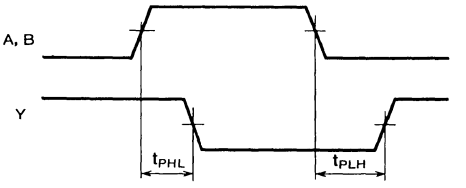
| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 1), $C_L$=50pF, $R_L$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | 2 | 5 | 8 | 2 | 5 | 9 | ns |
| $t_{PHL}$ | | | | 3 | 5 | 8 | 3 | 5 | 9 | |

*. All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS1002P

## QUADRUPLE 2-INPUT POSITIVE NOR BUFFER

## DESCRIPTION

The M74ALS1002P is a semiconductor integrated circuit consisting of four 2-input positive-logic NOR buffer gates, usable as negative-logic NAND buffer gates.

## FEATURES

- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High speed ($t_{pd}$ = 5ns typical: $C_L$ = 50pF)
- Low power dissipation ($P_d$ = 16.3mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS1002P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

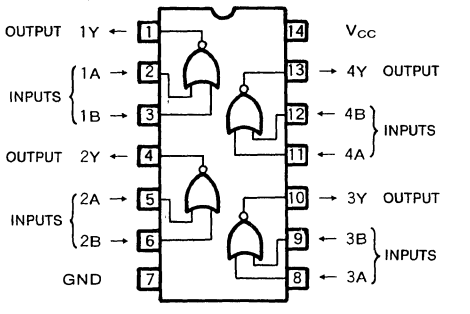
When both A and B inputs are low-level, output Y is high-level, and when at least one of the inputs is high, the output is low.

The M74ALS28P, which, except for its name, is identical in all respects to the M74ALS1002P, is also available.

## FUNCTION TABLE

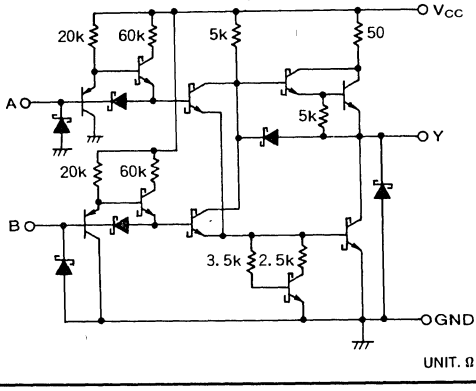
| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| H | L | L |
| L | H | L |
| H | H | L |

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT. Ω

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | −65~+150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |



MITSUBISHI ELECTRIC

## QUADRUPLE 2-INPUT POSITIVE NOR BUFFER

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 1.7 | 2.8 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 4.8 | 8 | mA |

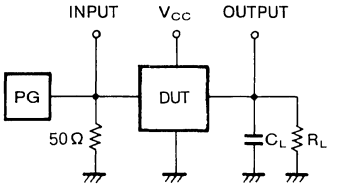
* All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

## SWITCHING CHARACTERISTICS

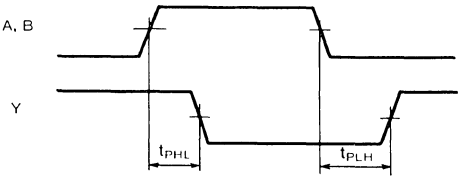
| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 1), $C_L$=50pF, $R_L$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | 2 | 5 | 8 | 2 | 5 | 9 | ns |
| $t_{PHL}$ | | | | 3 | 5 | 8 | 3 | 5 | 9 | |

* All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS1003P

## QUADRUPLE 2-INPUT POSITIVE NAND BUFFER WITH OPEN COLLECTOR OUTPUT

## DESCRIPTION

The M74ALS1003P is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND buffer gates with open collector outputs, usable as negative-logic NOR buffer gates.

## FEATURES

- Wired-AND connectability
- High fan-out ($I_{OL}$ = 24mA)
- High-breakdown output voltage ($V_O \geqq 7V$)
- High speed ($t_{pd}$ = 16.5ns typical: $C_L$ = 50pF)
- Low power dissipation ($P_d$ = 12.2mW typical)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

This device employs PNP transistor inputs and open collector outputs. The open collector output enables selection of high-level output impedance with an external resistor. It also permits wired-AND connection which is impossible with ordinary gates. Having a large low-level output current ($I_{OL}$) of 24mA, it is suitable for a buffer gate. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

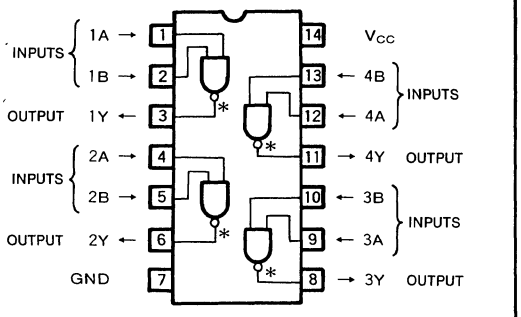
When both A and B inputs are high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

The M74ALS38P, which, except for its name, is identical in all respects to the M74ALS1003P, is also available.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

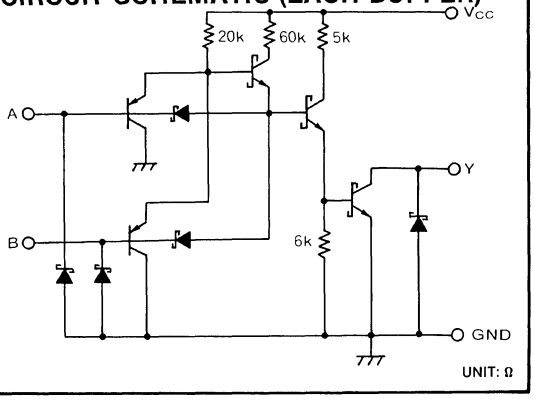
## PIN CONFIGURATION (TOP VIEW)




* OPEN COLLECTOR OUTPUT

Outline 14P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT: Ω

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | High-level state | −0.5 ~ +7 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 ~ +75 | °C |
| $T_{stg}$ | Storage temperature range | | −65 ~ +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | 0 | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## QUADRUPLE 2-INPUT POSITIVE NAND BUFFER WITH OPEN COLLECTOR OUTPUT

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.86 | 1.6 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 4 | 6.4 | mA |

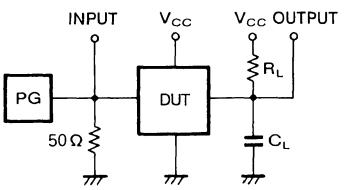
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

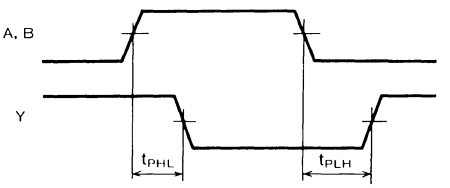
| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 1), $C_L$=50pF, $R_L$=680Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | 10 | 20 | 33 | 10 | 20 | 34 | ns |
| $t_{PHL}$ | | | | 7 | 13 | 18 | 7 | 13 | 19 | |

* All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance

# M74ALS1008P

## QUADRUPLE 2-INPUT POSITIVE AND BUFFER

## DESCRIPTION

The M74ALS1008P is a semiconductor integrated circuit consisting of four 2-input positive-logic AND buffer gates, usable as negative-logic OR buffer gates.

## FEATURES

- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High speed ($t_{pd}$ = 6.5ns typical: $C_L$ = 50pF)
- Low power dissipation ($P_d$ = 16.5mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

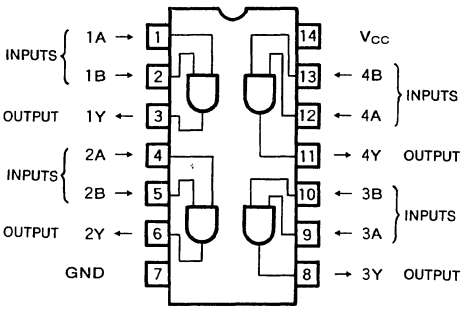
Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS1008P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

When both A and B inputs are high-level, output Y is high-level, and when at least one of the inputs is low, the output is low.

## FUNCTION TABLE

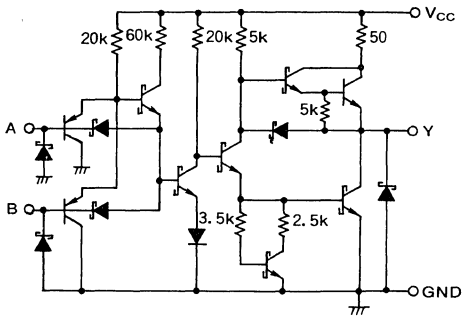
| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | L |
| H | L | L |
| L | H | L |
| H | H | H |

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT: Ω

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | −65~+150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## QUADRUPLE 2-INPUT POSITIVE AND BUFFER

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=4.5V | | | 1.8 | 3 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=0V | | | 4.8 | 8 | mA |

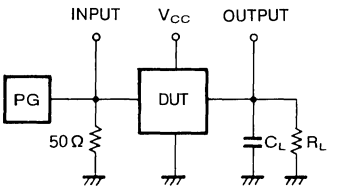
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

## SWITCHING CHARACTERISTICS

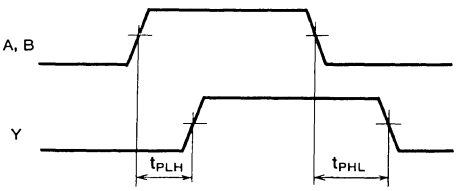
| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 1), $C_L$=50pF, $R_L$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | 2 | 6 | 9 | 2 | 6 | 10 | ns |
| $t_{PHL}$ | | | | 3 | 7 | 10 | 3 | 7 | 11 | |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics.

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance

# M74ALS1010P

## TRIPLE 3-INPUT POSITIVE NAND BUFFER

## DESCRIPTION

The M74ALS1010P is a semiconductor integrated circuit consisting of three 3-input positive-logic NAND buffer gates, usable as negative-logic NOR buffer gates.

## FEATURES

- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High speed ($t_{pd}$ = 5ns typical: $C_L$ = 50pF)
- Low power dissipation ($P_d$ = 10.6mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS1010P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

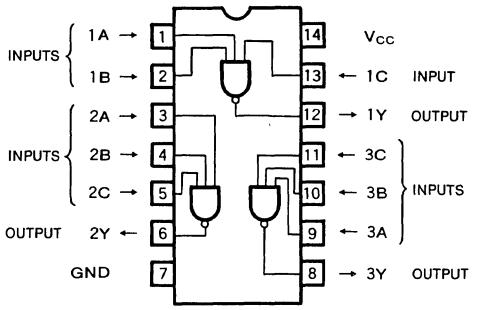
When A, B and C inputs are simultaneously high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | N | Y |
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

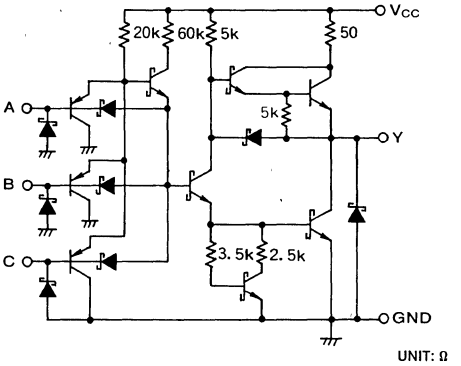
N=B · C

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## TRIPLE 3-INPUT POSITIVE NAND BUFFER

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.65 | 1.2 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 3.6 | 6 | mA |

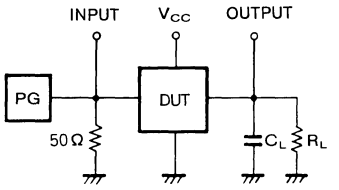
* · All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

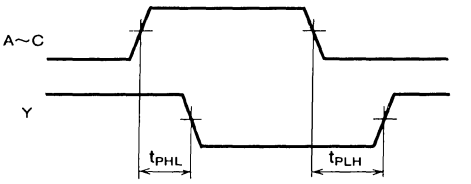
| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 1), $C_L$=50pF, $R_L$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A, B, C | Y | 2 | 5 | 8 | 2 | 5 | 9 | ns |
| $t_{PHL}$ | | | | 3 | 5 | 8 | 3 | 5 | 9 | |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance

# M74ALS1011P

## TRIPLE 3-INPUT POSITIVE AND BUFFER

## DESCRIPTION

The M74ALS1011P is a semiconductor integrated circuit consisting of three 3-input positive-logic AND buffer gates, usable as negative-logic OR buffer gates.

## FEATURES

- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High speed ($t_{pd}$ = 8ns typical: $C_L$ = 50pF)
- Low power dissipation ($P_d$ = 12.5mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS1011P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

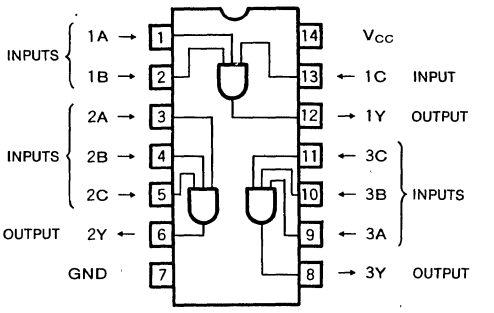
When A, B and C inputs are simultaneously high-level, output Y is high-level, and when at least one of the inputs is low, the output is low.

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | N | Y |
| L | L | L |
| H | L | L |
| L | H | L |
| H | H | H |

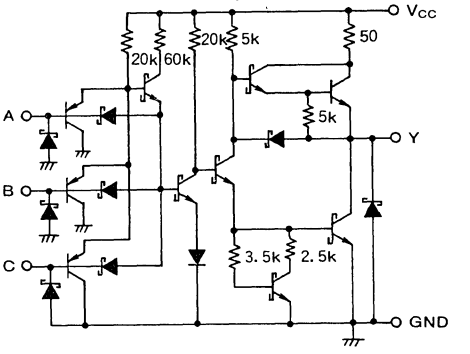
N=B · C

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |



MITSUBISHI ELECTRIC

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=4.5V | | | 1.4 | 2.3 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=0V | | | 3.6 | 6 | mA |

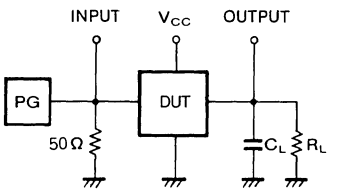
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

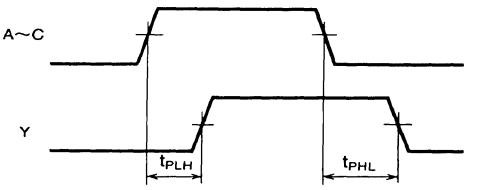
| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 1), $C_L$=50pF, $R_L$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A, B, C | Y | 2 | 7 | 10 | 2 | 7 | 11 | ns |
| $t_{PHL}$ | | | | 3 | 9 | 12 | 3 | 9 | 13 | |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS1020P

## DUAL 4-INPUT POSITIVE NAND BUFFER

## DESCRIPTION

The M74ALS1020P is a semiconductor integrated circuit consisting of two 4-input positive-logic NAND buffer gates, usable as negative-logic NOR buffer gates.

## FEATURES

- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High speed ($t_{pd}$ = 5ns typical: $C_L$ = 50pF)
- Low power dissipation ($P_d$ = 6.1mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

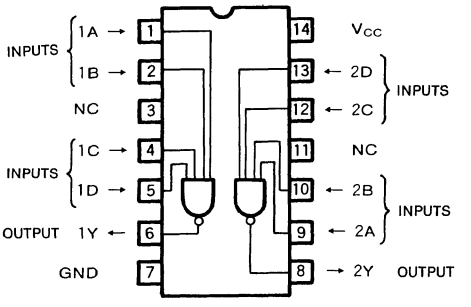
## FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS1020P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

When A, B, C and D inputs are simultaneously high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

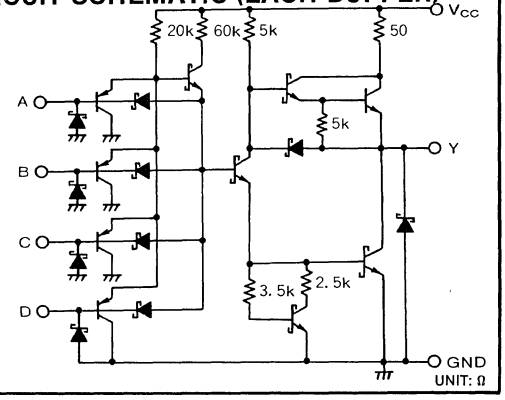
The M74ALS40P, which, except for its name, is identical in all respects to the M74ALS1020P, is also available.

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4 NC: NO CONNECTION

## CIRCUIT SCHEMATIC (EACH BUFFER)




## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | N | Y |
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

N=B · C · D

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |



MITSUBISHI ELECTRIC

## DUAL 4-INPUT POSITIVE NAND BUFFER

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=0V | | | 0.43 | 0.8 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=4.5V | | | 2 | 3.2 | mA |

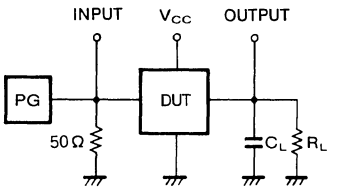
* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

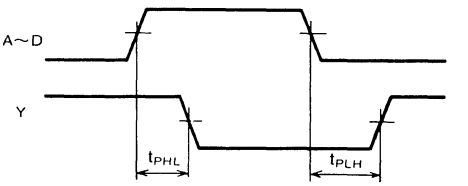
| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 1), $C_L$=50pF, $R_L$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Output | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A~D | Y | 2 | 5 | 8 | 2 | 5 | 9 | ns |
| $t_{PHL}$ | | | | 3 | 5 | 8 | 3 | 5 | 9 | |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS1032P

## QUADRUPLE 2-INPUT POSITIVE OR BUFFER

## DESCRIPTION

The M74ALS1032P is a semiconductor integrated circuit consisting of four 2-input positive-logic OR buffer gates, usable as negative-logic AND buffer gates.

## FEATURES

- High fan-out ($I_{OL}$ = 24mA, $I_{OH}$ = −2.6mA)
- High speed ($t_{pd}$ = 7.5ns typical: $C_L$ = 50pF)
- Low power dissipation ($P_d$ = 20mW typical)
- Low output impedance
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

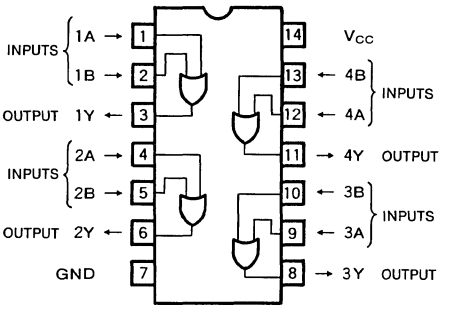
Employing PNP transistors in the inputs and active pull-up in the outputs, the M74ALS1032P achieves high speed, low power dissipation, and high fan-out. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

When both A and B inputs are low-level, output Y is low-level, and when at least one of the inputs is high, the output is high.

## FUNCTION TABLE

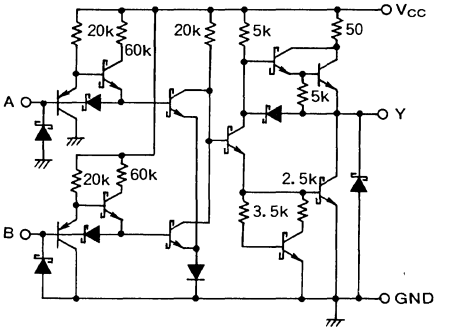
| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | L |
| H | L | H |
| L | H | H |
| H | H | H |

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT: Ω

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | −65~+150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 24 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## QUADRUPLE 2-INPUT POSITIVE OR BUFFER

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V, $I_{OH}$=−2.6mA | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=24mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −15 | | −70 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V, $V_I$=4.5V | | | 2.5 | 5 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V, $V_I$=0V | | | 5.5 | 10 | mA |

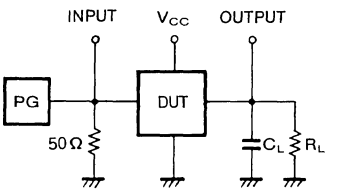
* · All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS

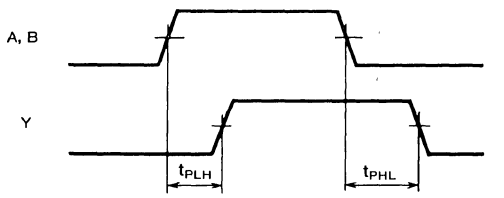
| Symbol | Parameter | | | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 1), $C_L$=50pF, $R_L$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Output | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A, B | Y | 2 | 6 | 10 | 2 | 6 | 11 | ns |
| $t_{PHL}$ | | | | 3 | 9 | 13 | 3 | 9 | 14 | |

* · All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 1: Measurement circuit




### TIMING DIAGRAM (Reference level = 1.3V)




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

# M74ALS1240P

## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS1240P is a semiconductor integrated circuit consisting of two blocks of buffers with 3-state inverted outputs and independent output control for each block.

## FEATURES

- Low-power version of M74ALS240P
- In-phase output control inputs ($1\overline{OC}$, $2\overline{OC}$)
- High fan-out, 3-state output ($I_{OL}$ = 16mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

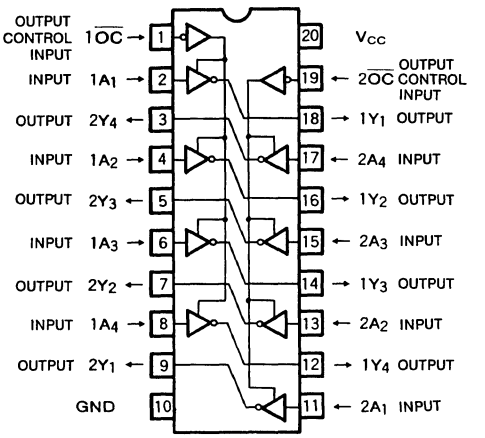
General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

When output control input $\overline{OC}$ is low-level, and if input A is low, then output Y is high. If A is high, Y is low. When $\overline{OC}$ is high, $Y_1$ ~ $Y_4$ are in high-impedance state irrespective of the status of A.

By connecting $1\overline{OC}$ and $2\overline{OC}$, the outputs of all eight buffers can be simultaneously controlled. The outputs can be terminated with a load resistor of not less than 133Ω.

## PIN CONFIGURATION (TOP VIEW)



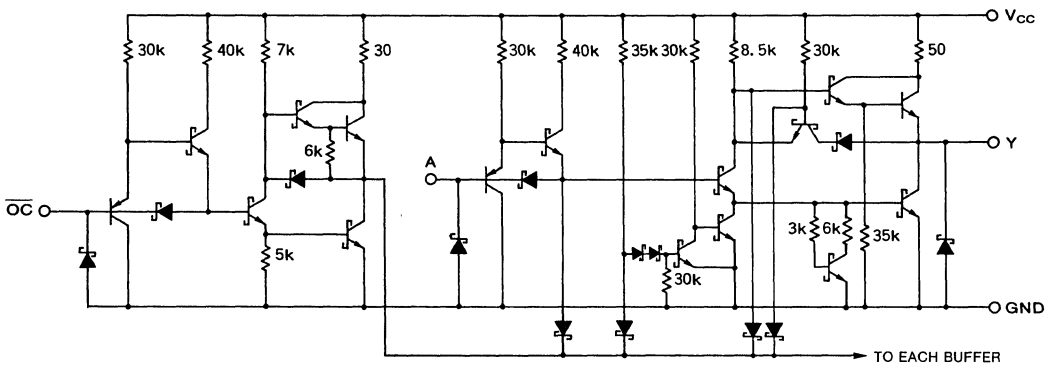

Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Output |
|---|---|---|
| A | $\overline{OC}$ | Y |
| L | L | H |
| H | L | L |
| X | H | Z |

Note 1: Z : High-impedance state
X : Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT: Ω



MITSUBISHI ELECTRIC

## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (INVERTED)

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5~+5.5 | V |
| Topr | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| Tstg | Storage temperature range | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 16 | mA |
| Topr | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=8mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=16mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 5 | 9 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 9 | 15 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | $V_{CC}$=5.5V | | | 11 | 19 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

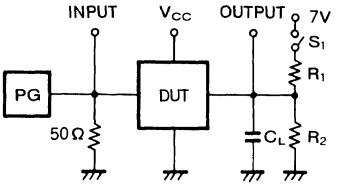
## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (INVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Output | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A | Y | 4 | 8 | 13 | 4 | 8 | 14 | ns |
| $t_{PHL}$ | | | | 3 | 7 | 12 | 3 | 7 | 13 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | Y | 5 | 13 | 22 | 5 | 13 | 23 | ns |
| $t_{PZL}$ | | | | 9 | 19 | 25 | 9 | 19 | 26 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | Y | 2 | 7 | 15 | 2 | 7 | 16 | ns |
| $t_{PLZ}$ | | | | 3 | 10 | 20 | 3 | 10 | 21 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics.

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

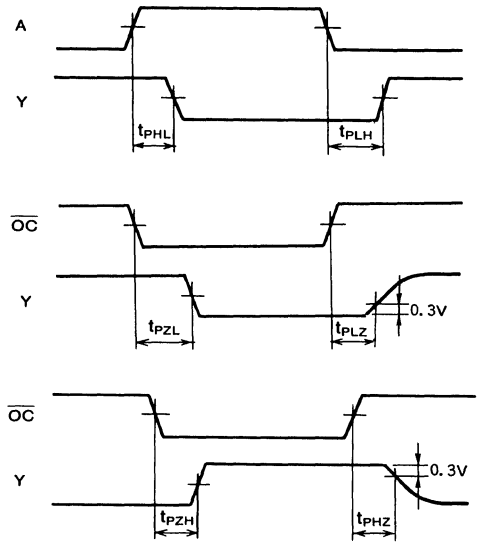
duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

### TIMING DIAGRAM (Reference level = 1.3V)






MITSUBISHI ELECTRIC

# M74ALS1241P

## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS1241P is a semiconductor integrated circuit consisting of two blocks of buffers with 3-state noninverted outputs and independent output control for each block.

## FEATURES

- Low-power version of M74ALS241P
- Complementary output control inputs ($1\overline{OC}$, 2OC)
- High fan-out, 3-state output ($I_{OL}$ = 16mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

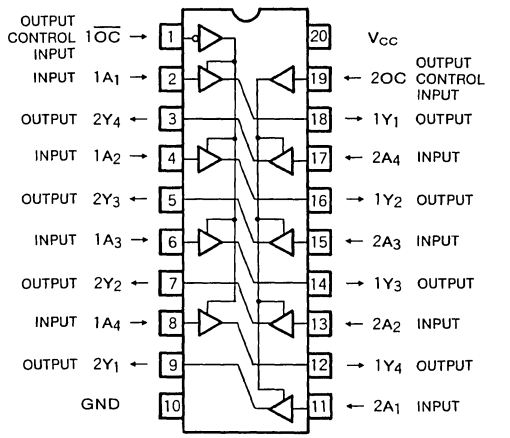
General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

When output control input $1\overline{OC}$ is low-level, and if input 1A is low, then output 1Y is low. If 1A is high, 1Y is high. When 2OC is high, and input 2A is low, then output 2Y is low, but if 2A is high then 2Y is high. If $1\overline{OC}$ and 2OC are high and low respectively, then all outputs are in high-impedance state.

The device can be used as a 4-bit two-way bus driver by connecting $1\overline{OC}$ and 2OC, 1A and 2Y, 2A and 1Y respectively. The outputs can be terminated with a load resistor of not less than 133Ω.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

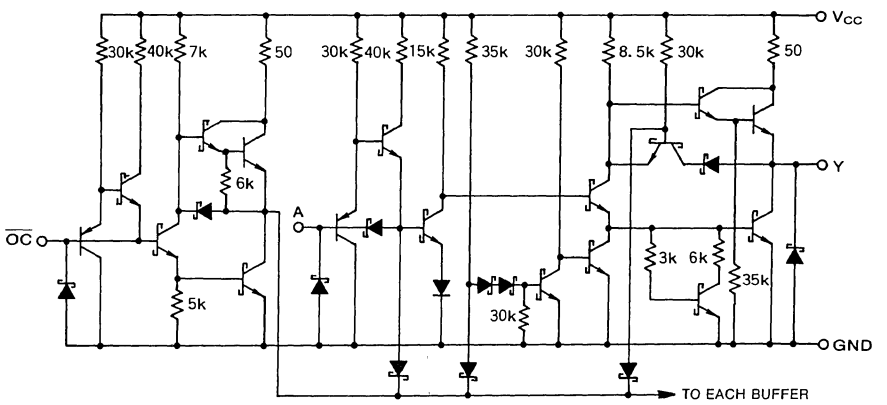
## FUNCTION TABLE (Note 1)

| Inputs | | Output |
|---|---|---|
| 1A | $1\overline{OC}$ | 1Y |
| L | L | L |
| H | L | H |
| X | H | Z |

| Inputs | | Output |
|---|---|---|
| 2A | 2OC | 2Y |
| L | H | L |
| H | H | H |
| X | L | Z |

Note 1: Z : High-impedance state
X Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT: Ω

## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5 ~ +5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20 ~ +75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65 ~ +150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 16 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=8mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=16mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 8 | 13 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 10 | 18 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | $V_{CC}$=5.5V | | | 13 | 22 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

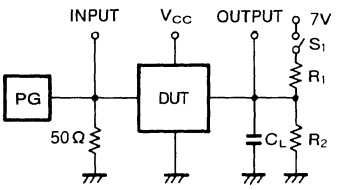
## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Output | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | Typ* | Max | $T_a$=−20~+75℃ Min | Typ* | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A | Y | 4 | 9 | 14 | 4 | 9 | 15 | ns |
| $t_{PHL}$ | | | | 4 | 9 | 14 | 4 | 9 | 15 | |
| $t_{PZH}$ | Output enable time | $1\overline{OC}$ | Y | 9 | 17 | 25 | 9 | 17 | 26 | ns |
| $t_{PZL}$ | | | | 9 | 18 | 28 | 9 | 18 | 29 | |
| $t_{PHZ}$ | Output disable time | $1\overline{OC}$ | Y | 2 | 8 | 15 | 2 | 8 | 16 | ns |
| $t_{PLZ}$ | | | | 3 | 13 | 20 | 3 | 13 | 21 | |
| $t_{PZH}$ | Output enable time | 2OC | Y | 9 | 19 | 25 | 9 | 19 | 26 | ns |
| $t_{PZL}$ | | | | 9 | 20 | 28 | 9 | 20 | 29 | |
| $t_{PHZ}$ | Output disable time | 2OC | Y | 2 | 10 | 15 | 2 | 10 | 16 | ns |
| $t_{PLZ}$ | | | | 3 | 15 | 20 | 3 | 15 | 21 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: Measurement circuit

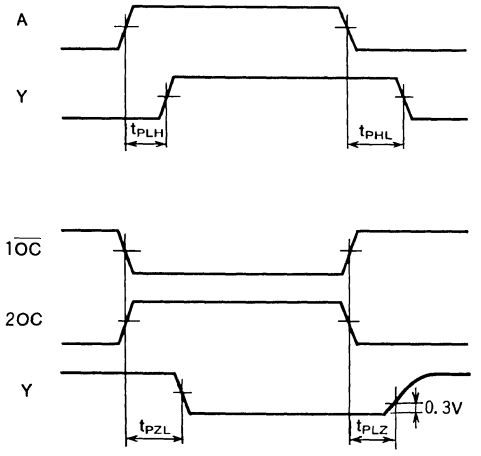


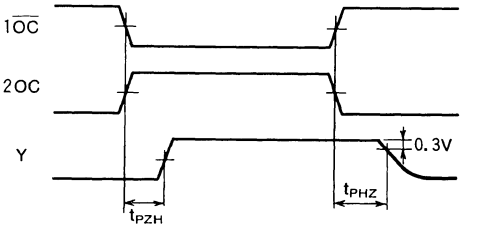

(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS1242P

## QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS1242P is a semiconductor integrated circuit consisting of four bus transmitter/receiver circuits with 3-state inverted outputs.

## FEATURES

- Low power version of M74ALS242P
- Two-way transmission or isolation between two 4-bit data
- High fan-out ($I_{OL}$ = 16mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

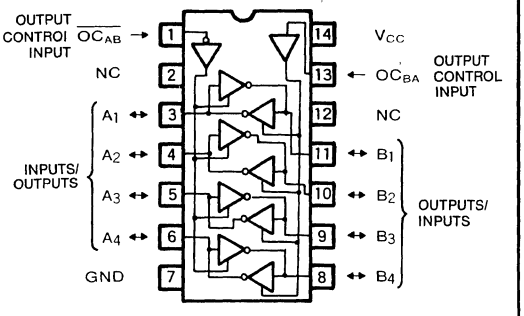
## FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with 3-state inverted outputs.

The input/output direction is controlled by $\overline{OC_{AB}}$ and $OC_{BA}$.

When $\overline{OC_{AB}}$ and $OC_{BA}$ are low, pins A are made the input pins and pins B are made the output pins. When $\overline{OC_{AB}}$ and $OC_{BA}$ are high, pins B are made the input pins and pins A are made the output pins. When $\overline{OC_{AB}}$ is high and $OC_{BA}$ is low, both A and B are in the high-impedance state and A and B are isolated. The device can be used as a latch when $\overline{OC_{AB}}$ is low and $OC_{BA}$ is high. The outputs can be terminated with load resistors of not less than 133Ω.

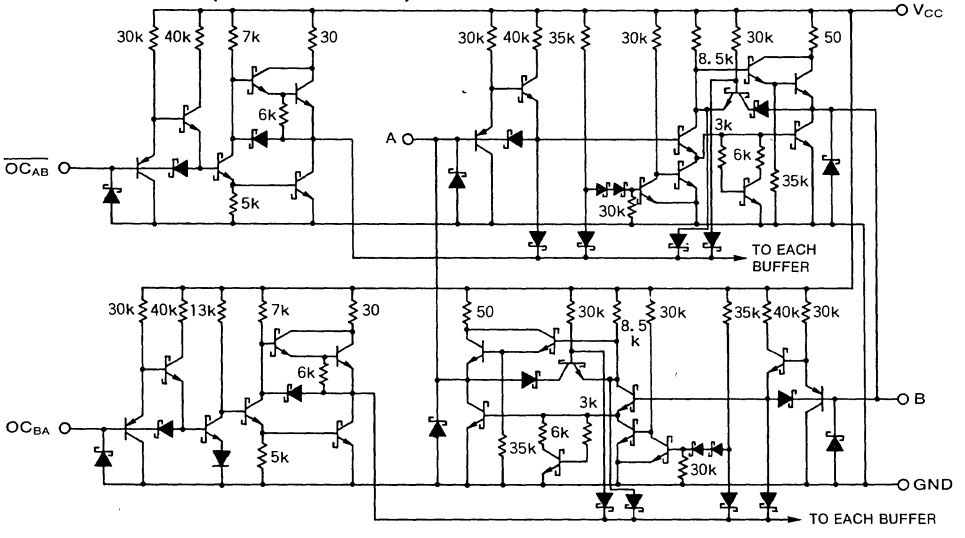
## PIN CONFIGURATION (TOP VIEW)




NC: NO CONNECTION

Outline 14P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT: Ω



MITSUBISHI ELECTRIC

# QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC_{AB}}$ | $OC_{BA}$ | A | B |
| H | H | $\overline{O}$ | I |
| L | H | * | * |
| H | L | Z | Z |
| L | L | I | $\overline{O}$ |

Note 1: I : Input pins
$\overline{O}$ : Output pins (inverted output)
Z : High-impedance state (A and B are isolated)
* : In this case, data can be latched with the procedure shown below.
(1) Apply the date to be stored to A or B. ($OC_{BA}$ and $\overline{OC_{AB}}$ must be equally high or equally low.)
(2) Set $OC_{BA}$ high and $\overline{OC_{AB}}$ low respectively.
(3) Remove the data
(4) The data applied in(1) is stored. If voltage is applied to A or B in this condition, the device may be damaged. Change the status of $OC_{BA}$ or $\overline{OC_{AB}}$ before applying voltage

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+5.5 | V |
| | | $\overline{OC_{AB}}$, $OC_{BA}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state or high-impedance state | −0.5~+5.5 | V |
| Topr | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| Tstg | Storage temperature range | | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 16 | mA |
| Topr | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=8mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=16mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $\overline{OC_{AB}}$, $OC_{BA}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | |
| $I_{IH}$ | High-level input current (Note 2) | $\overline{OC_{AB}}$, $OC_{BA}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current (Note 3) | $\overline{OC_{AB}}$, $OC_{BA}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 8 | 16 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 10 | 18 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 11 | 20 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 2: For A and B, $I_{IH}$ includes off-state high-level output current $I_{OZH}$.

Note 3: For A and B, $I_{IL}$ includes off-state low-level output current $I_{OZL}$.

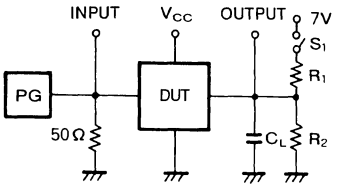
## QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A, B | B, A | 4 | 8 | 14 | 4 | 8 | 15 | ns |
| $t_{PHL}$ | | | | 4 | 7 | 13 | 4 | 7 | 14 | |
| $t_{PZH}$ | Output enable time | $\overline{OC_{AB}}$ | B | 5 | 13 | 22 | 5 | 13 | 23 | ns |
| $t_{PZL}$ | | | | 9 | 16 | 25 | 9 | 16 | 26 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC_{AB}}$ | B | 2 | 7 | 15 | 2 | 7 | 16 | ns |
| $t_{PLZ}$ | | | | 3 | 10 | 20 | 3 | 10 | 21 | |
| $t_{PZH}$ | Output enable time | $OC_{BA}$ | A | 5 | 15 | 22 | 5 | 15 | 23 | ns |
| $t_{PZL}$ | | | | 9 | 18 | 25 | 9 | 18 | 26 | |
| $t_{PHZ}$ | Output disable time | $OC_{BA}$ | A | 2 | 9 | 15 | 2 | 9 | 16 | ns |
| $t_{PLZ}$ | | | | 3 | 12 | 20 | 3 | 12 | 21 | |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 4: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

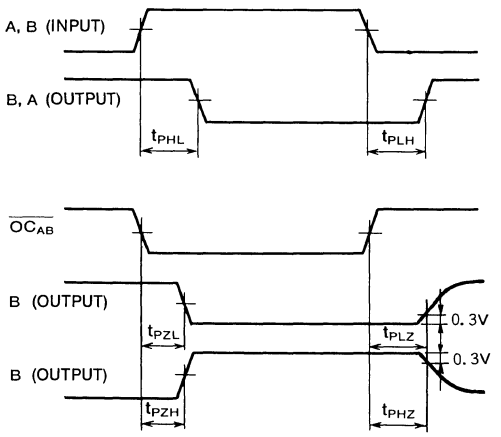
duty cycle=50%

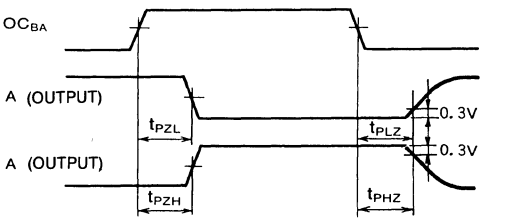
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

## TIMING DIAGRAM (Reference level = 1.3V)






MITSUBISHI ELECTRIC

# M74ALS1243P

## QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS1243P is a semiconductor integrated circuit consisting of four bus transmitter/receiver circuits with 3-state noninverted outputs.

## FEATURES

- Low-power version of M74ALS243P
- Two-way transmission or isolation between two 4-bit data
- High fan-out ($I_{OL}$ = 16mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

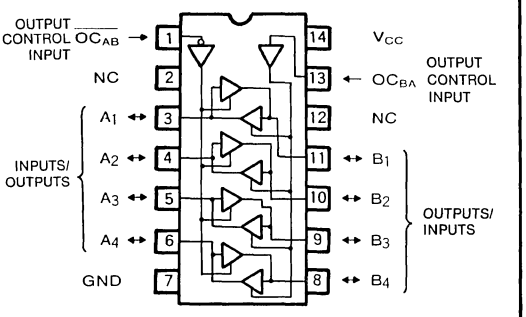
## FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with 3-state noninverted outputs.

The input/output direction is controlled by $\overline{OC_{AB}}$ and $OC_{BA}$.

When $\overline{OC_{AB}}$ and $OC_{BA}$ are low,pins A are made the input pins and pins B are made the output pins. When $\overline{OC_{AB}}$ and $OC_{BA}$ are high, pins B are made the input pins and pins A are made the output pins. When $\overline{OC_{AB}}$ is high and $OC_{BA}$ is low, both A and B are in the high-impedance state and A and B are isolated. The device can be used as a latch when $\overline{OC_{AB}}$ is low and $OC_{BA}$ is high. The outputs can be terminated with load resistors of not less than 133Ω.

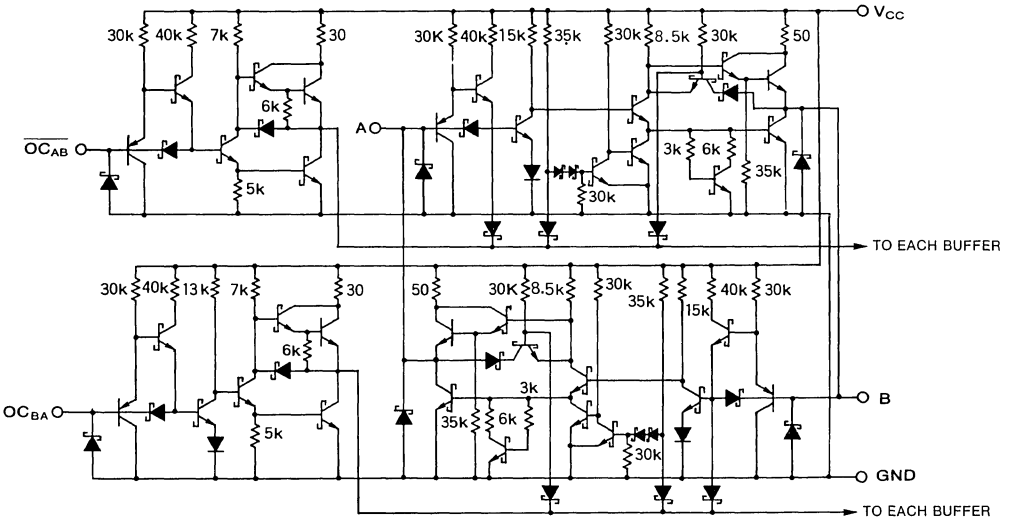
## PIN CONFIGURATION (TOP VIEW)




NC. NO CONNECTION

Outline 14P4

## CIRCUIT SCHEMATIC (EACH BUFFER)



# QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC_{AB}}$ | $OC_{BA}$ | A | B |
| H | H | O | I |
| L | H | * | * |
| H | L | Z | Z |
| L | L | I | O |

Note 1:
I : Input pins
O : Output pins (noninverted output)
Z : High impedance state (A and B are isolated)
* : In this case, data can be latched with the procedure shown below.
(1) Apply the data to be stored to A or B. ($OC_{BA}$ and $\overline{OC_{AB}}$ must be equally high or equally low.)
(2) Set $OC_{BA}$ high and $\overline{OC_{AB}}$ low respectively.
(3) Remove the data.
(4) The data applied in (1) is stored. If voltage is applied to A or B in this condition, the device may be damaged. Change the status of $OC_{BA}$ or $\overline{OC_{AB}}$ before applying voltage.

## ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | A, B | | −0.5 ~ +5.5 | V |
| | | $\overline{OC_{AB}}$, $OC_{BA}$ | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | | High-level state or high-impedance state | −0.5 ~ +5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20 ~ +75 | °C |
| $T_{stg}$ | Storage temperature range | | | −65 ~ +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 16 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=8mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=16mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $\overline{OC_{AB}}$, $OC_{BA}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | |
| $I_{IH}$ | High-level input current (Note 2) | $\overline{OC_{AB}}$, $OC_{BA}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current (Note 3) | $\overline{OC_{AB}}$, $OC_{BA}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 11 | 19 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 12 | 21 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 13 | 23 | mA |

* : All typical values are at $V_{CC}$ = 5V, Ta = 25°C.
Note 2: For A and B, $I_{IH}$ includes off-state high-level output current $I_{OZH}$.
Note 3: For A and B, $I_{IL}$ includes off-state low-level output current $I_{OZL}$.

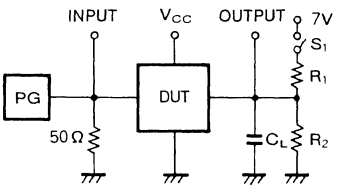
## QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A, B | B, A | 4 | 9 | 14 | 4 | 9 | 15 | ns |
| $t_{PHL}$ | | | | 4 | 9 | 14 | 4 | 9 | 15 | |
| $t_{PZH}$ | Output enable time | $\overline{OC_{AB}}$ | B | 9 | 17 | 25 | 9 | 17 | 26 | ns |
| $t_{PZL}$ | | | | 9 | 18 | 28 | 9 | 18 | 29 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC_{AB}}$ | B | 2 | 8 | 15 | 2 | 8 | 16 | ns |
| $t_{PLZ}$ | | | | 3 | 13 | 20 | 3 | 13 | 21 | |
| $t_{PZH}$ | Output enable time | $OC_{BA}$ | A | 9 | 19 | 25 | 9 | 19 | 26 | ns |
| $t_{PZL}$ | | | | 9 | 20 | 28 | 9 | 20 | 29 | |
| $t_{PHZ}$ | Output disable time | $OC_{BA}$ | A | 2 | 10 | 15 | 2 | 10 | 16 | ns |
| $t_{PLZ}$ | | | | 3 | 15 | 20 | 3 | 15 | 21 | |

*. All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 4. Measurement circuit




(1) The pulse generator (PG) has the following characteristics

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

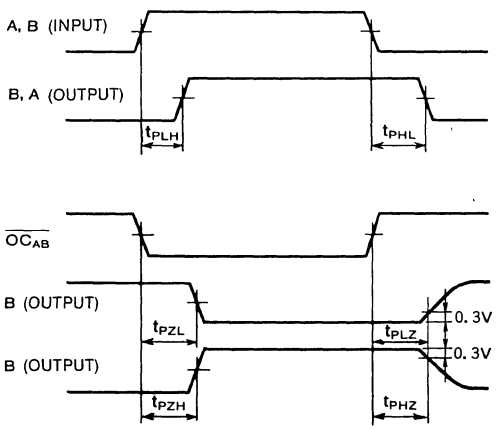
duty cycle=50%

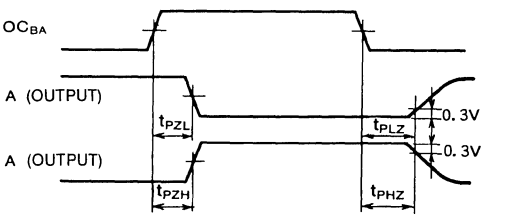
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

## TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS1244P

## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

### DESCRIPTION

The M74ALS1244P is a semiconductor integrated circuit consisting of two blocks of buffers with 3-state noninverted outputs and independent output control for each block.

### FEATURES

- Low-power version of M74ALS244P
- In-phase output control inputs ($1\overline{OC}$, $2\overline{OC}$)
- High fan-out, 3-state output ($I_{OL}$ = 16mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

### APPLICATIONS

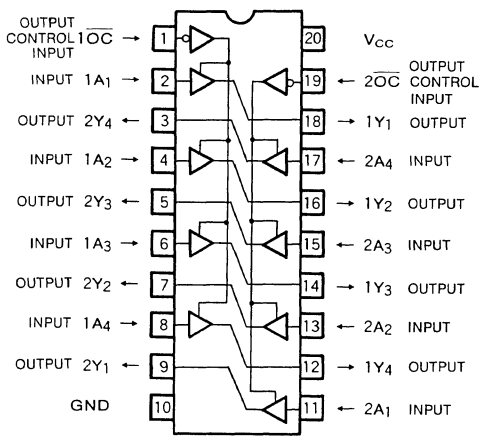
General purpose, for use in industrial and consumer digital equipment.

### FUNCTIONAL DESCRIPTION

When output control input $\overline{OC}$ is low-level, and if input A is low, then output Y is low. If A is high, Y is high. When $\overline{OC}$ is high, $Y_1 \sim Y_4$ are in high-impedance state irrespective of the condition of A.

The outputs of all eight circuits can be controlled simultaneously by connecting $1\overline{OC}$ and $2\overline{OC}$. The outputs can be terminated with a load resistor of not less than 133Ω.

### PIN CONFIGURATION (TOP VIEW)



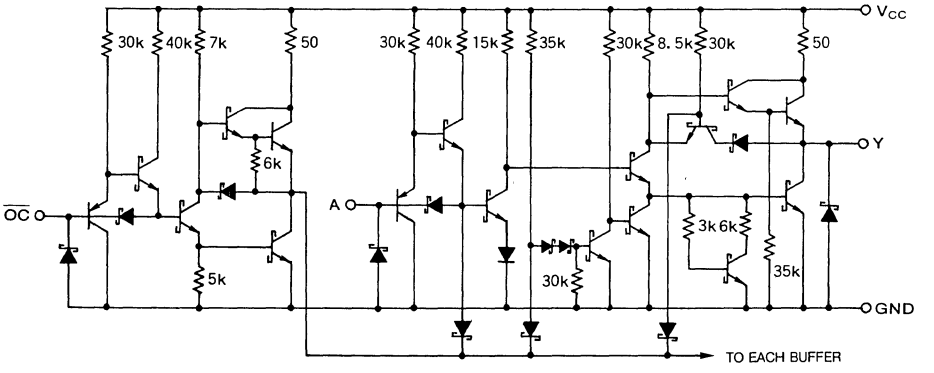

Outline 20P4

### FUNCTION TABLE (Note 1)

| Inputs | | Output |
|---|---|---|
| A | $\overline{OC}$ | Y |
| L | L | L |
| H | L | H |
| X | H | Z |

Note 1: Z : High-impedance state
X : Irrelevant

### CIRCUIT SCHEMATIC.(EACH BUFFER)




UNIT Ω



MITSUBISHI ELECTRIC

## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state or high-impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 16 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$=4.5V | $I_{OL}$=8mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$=16mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state high-level output current | $V_{CC}$=5.5V, $V_O$=2.7V | | | | 20 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{CC}$=5.5V, $V_O$=0.4V | | | | −20 | μA |
| $I_I$ | Input current at maximum voltage | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| $I_O$ | Output current | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | $V_{CC}$=5.5V | | | 8 | 13 | mA |
| $I_{CCL}$ | Supply current, all outputs low | $V_{CC}$=5.5V | | | 10 | 18 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | $V_{CC}$=5.5V | | | 13 | 22 | mA |

* : All typical values are at $V_{CC}$=5V, $T_a$=25°C

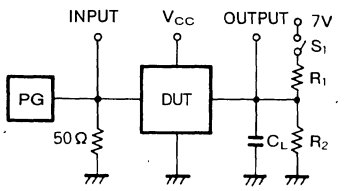
## OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Output | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A | Y | 4 | 9 | 14 | 4 | 9 | 15 | ns |
| $t_{PHL}$ | | | | 4 | 9 | 14 | 4 | 9 | 15 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | Y | 9 | 17 | 25 | 9 | 17 | 26 | ns |
| $t_{PZL}$ | | | | 9 | 18 | 28 | 9 | 18 | 29 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | Y | 2 | 8 | 15 | 2 | 8 | 16 | ns |
| $t_{PLZ}$ | | | | 3 | 13 | 16 | 3 | 13 | 17 | |

*· All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 2: Measurement circuit

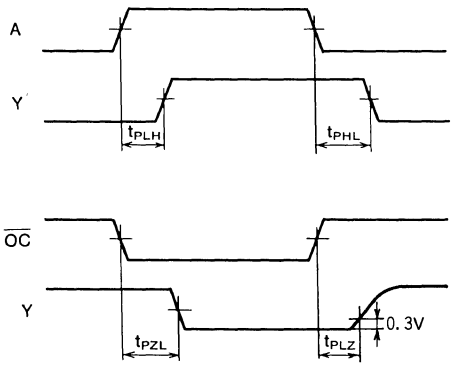


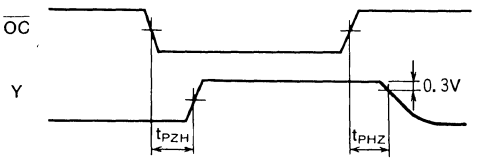

(1) The pulse generator (PG) has the following characteristics
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

### TIMING DIAGRAM (Reference level = 1.3V)





MITSUBISHI ELECTRIC

# M74ALS1245P

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS1245P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with 3-state noninverted outputs.

## FEATURES

- Low-power version of M74ALS245P
- Two-way transmission or isolation between two 8-bit data
- High fan-out ($I_{OL}$ = 16mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

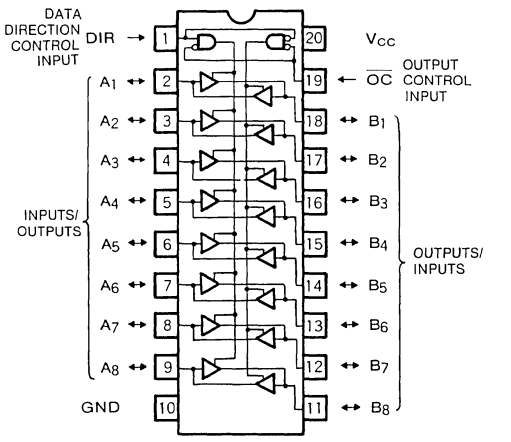
The inputs and outputs are mutually connected to form two-way buffers with the 3-state noninverted outputs.

The input/output direction is controlled by DIR.

When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins. When $\overline{OC}$ is high, both A and B are in the high-impedance state and A and B are isolated.

The M74ALS1645P, which, except for its name, is identical in all respects to the M74ALS1245P, is also available.

## PIN CONFIGURATION (TOP VIEW)



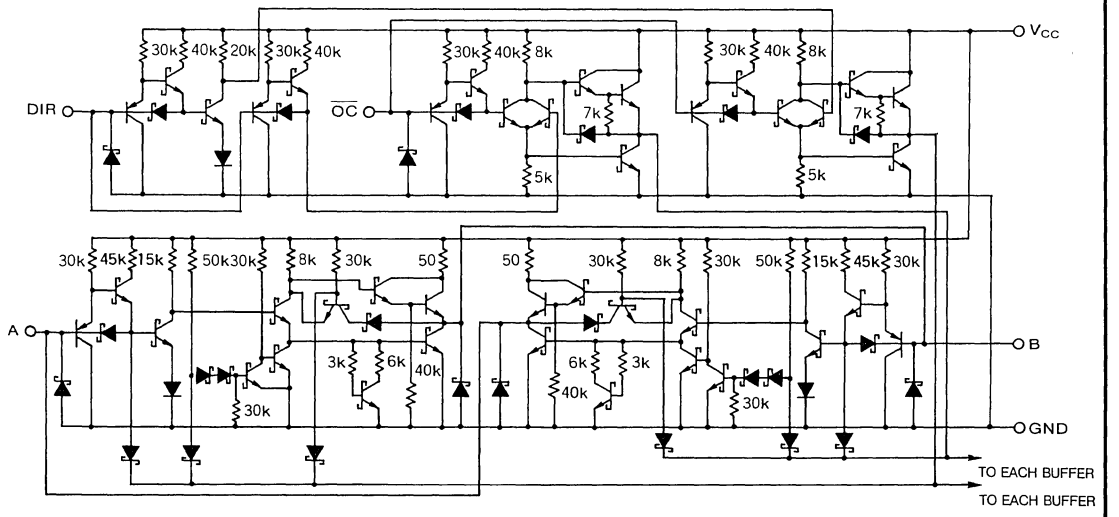

Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC}$ | DIR | A | B |
| L | L | O | I |
| L | H | I | O |
| H | X | Z | Z |

Note 1. I Input pins
O Output pins (noninverted output)
Z High-impedance state (A and B are isolated)
X . Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)



## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+5.5 | V |
| | | DIR, $\overline{OC}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state or high-impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 16 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=8mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=16mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | |
| $I_{IH}$ | High-level input current (Note 2) | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current (Note 3) | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 20 | 32 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 23 | 37 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 25 | 39 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 2: For A and B, $I_{IH}$ includes off-state high-level output current $I_{OZH}$.

Note 3: For A and B, $I_{IL}$ includes off-state low-level output current $I_{OZL}$.

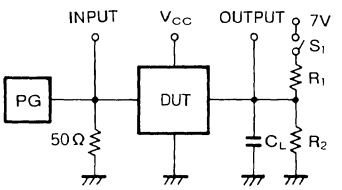
## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A, B | B, A | 4 | 9 | 13 | 4 | 9 | 14 | ns |
| $t_{PHL}$ | | | | 4 | 9 | 13 | 4 | 9 | 14 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | A, B | 10 | 16 | 25 | 10 | 16 | 26 | ns |
| $t_{PZL}$ | | | | 13 | 18 | 29 | 13 | 18 | 30 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | A, B | 4 | 7 | 18 | 4 | 7 | 19 | ns |
| $t_{PLZ}$ | | | | 5 | 9 | 21 | 5 | 9 | 22 | |

* All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 4 Measurement circuit

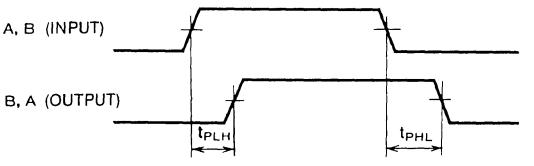


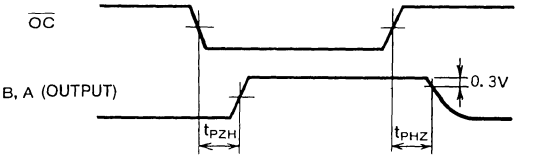

(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

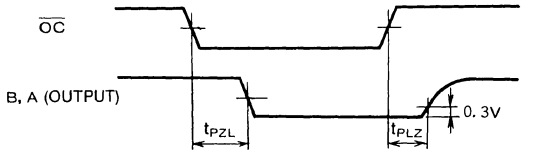
(2) $C_L$ includes probe and jig capacitance

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS1620P

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS1620P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with 3-state inverted outputs.

## FEATURES

- Low-power version of M74ALS620P
- Two-way transmission or isolation between two 8-bit data
- High fan-out ($I_{OL}$ = 16mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

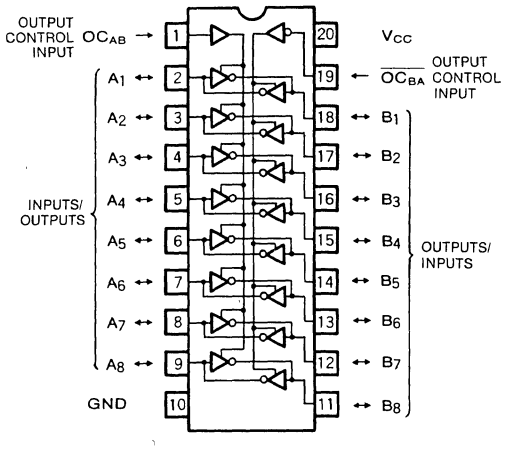
## FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with 3-state inverted outputs.

The input/output direction is controlled by $OC_{AB}$ and $\overline{OC_{BA}}$.

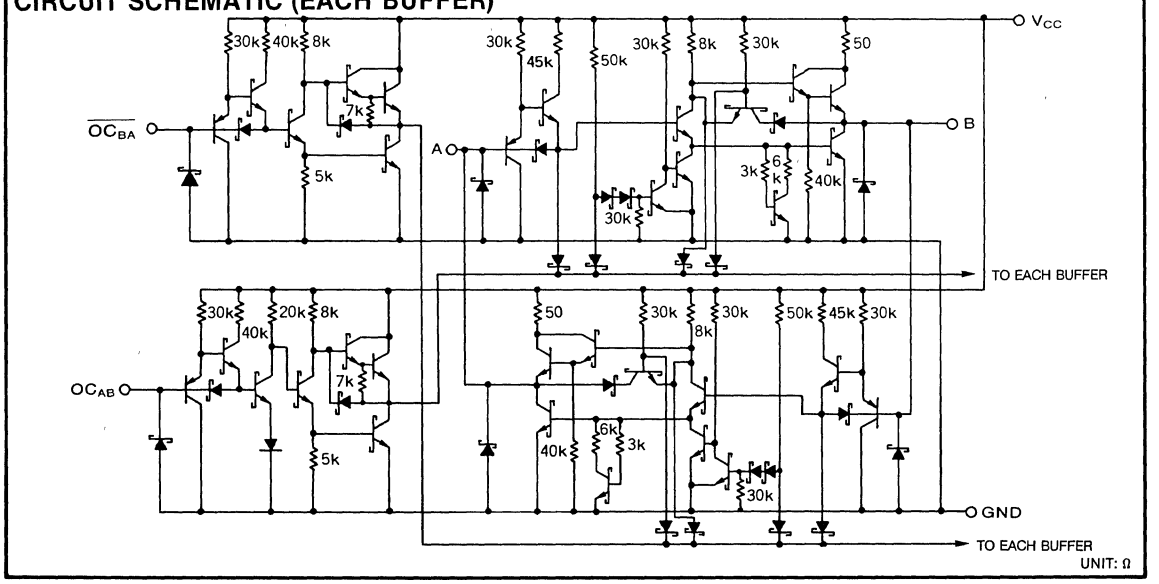
When $OC_{AB}$ and $\overline{OC_{BA}}$ are high, pins A are made the input pins and pins B are made the output pins. When $OC_{AB}$ and $\overline{OC_{BA}}$ are low, B are made the input pins and A are made the output pins. When $OC_{AB}$ is low and $\overline{OC_{BA}}$ is high, both A and B are in the high-impedance state and A and B are isolated. Latch operation is possible when $OC_{AB}$ is high and $\overline{OC_{BA}}$ is low.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT: Ω



MITSUBISHI ELECTRIC

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

### FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC_{BA}}$ | $OC_{AB}$ | A | B |
| L | L | $\overline{O}$ | I |
| H | H | I | $\overline{O}$ |
| H | L | Z | Z |
| L | H | * | * |

Note 1: I : Input pins
$\overline{O}$ Output pins (inverted output)
Z : High-impedance state (A and B are isolated)
* In this case, data can be latched with the procedure shown below
(1) Apply the data to be stored to A or B ($OC_{AB}$ and $\overline{OC_{BA}}$ must be equally high or equally low.)
(2) Set $OC_{AB}$ high and $\overline{OC_{BA}}$ low respectively.
(3) Remove the data.
(4) The data applied in (1) is stored. If voltage is applied to A or B in this condition, the device may be damaged. Change the status of $OC_{AB}$ or $\overline{OC_{BA}}$ before applying voltage.

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | A, B | | −0.5 ~ +5.5 | V |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | | High-level state or high-impedance state | −0.5 ~ +5.5 | V |
| Topr | Operating free-air ambient temperature range | | | −20 ~ +75 | °C |
| Tstg | Storage temperature range | | | −65 ~ +150 | °C |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 16 | mA |
| Topr | Operating free-air ambient temperature range | −20 | | +75 | °C |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=8mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=16mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $OC_{AB}$, $\overline{OC_{BA}}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | |
| $I_{IH}$ | High-level input current (Note 2) | $OC_{AB}$, $\overline{OC_{BA}}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current (Note 3) | $OC_{AB}$, $\overline{OC_{BA}}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 16 | 22 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 20 | 28 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 21 | 31 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 2: For A and B, $I_{IH}$ includes off-state high-level output current $I_{OZH}$.

Note 3: For A and B, $I_{IL}$ includes off-state low-level output current $I_{OZL}$.

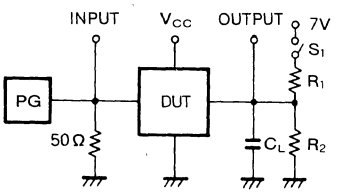
## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A, B | B, A | 4 | 7 | 15 | 4 | 7 | 16 | ns |
| $t_{PHL}$ | | | | 3 | 6 | 13 | 3 | 6 | 14 | |
| $t_{PZH}$ | Output enable time | $\overline{OC_{BA}}$ | A | 5 | 10 | 22 | 5 | 10 | 23 | ns |
| $t_{PZL}$ | | | | 9 | 16 | 27 | 9 | 16 | 28 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC_{BA}}$ | A | 3 | 7 | 22 | 3 | 7 | 23 | ns |
| $t_{PLZ}$ | | | | 5 | 10 | 27 | 5 | 10 | 28 | |
| $t_{PZH}$ | Output enable time | $OC_{AB}$ | B | 3 | 11 | 19 | 3 | 11 | 20 | ns |
| $t_{PZL}$ | | | | 9 | 17 | 37 | 9 | 17 | 38 | |
| $t_{PHZ}$ | Output disable time | $OC_{AB}$ | B | 5 | 11 | 20 | 5 | 11 | 21 | ns |
| $t_{PLZ}$ | | | | 9 | 16 | 37 | 9 | 16 | 38 | |

*: All typical values are at $V_{CC}$=5V $T_a$=25°C

Note 4 Measurement circuit




(1) The pulse generator (PG) has the following characteristics.

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

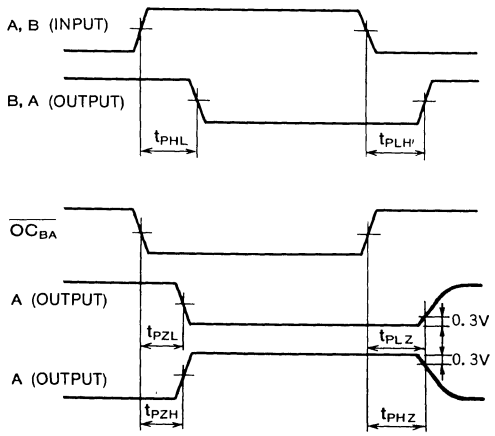
duty cycle=50%

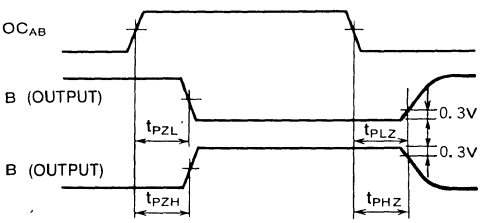
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

## TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS1621P

## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS1621P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with noninverted open collector outputs.

## FEATURES

- Low-power version of M74ALS621P
- Two-way transmission or isolation between two 8-bit data
- Open collector output
- High fan-out ($I_{OL}$ = 16mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

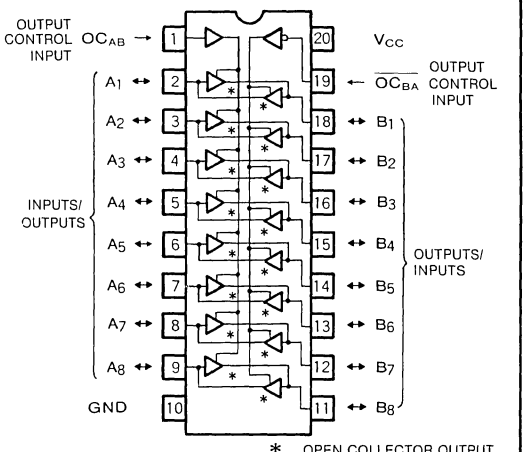
The inputs and outputs are mutually connected to form two-way buffers with noninverted open collector outputs.

The input/output direction is controlled by $OC_{AB}$ and $\overline{OC_{BA}}$.

When $OC_{AB}$ and $\overline{OC_{BA}}$ are high, pins A are made the input pins and pins B are made the output pins. When $OC_{AB}$ and $\overline{OC_{BA}}$ are low, B are made the input pins and A are made the output pins. When $OC_{AB}$ is low and $\overline{OC_{BA}}$ is high, both A and B become high and A and B are isolated. Latch operation is possible when $OC_{AB}$ is high and $\overline{OC_{BA}}$ is low.

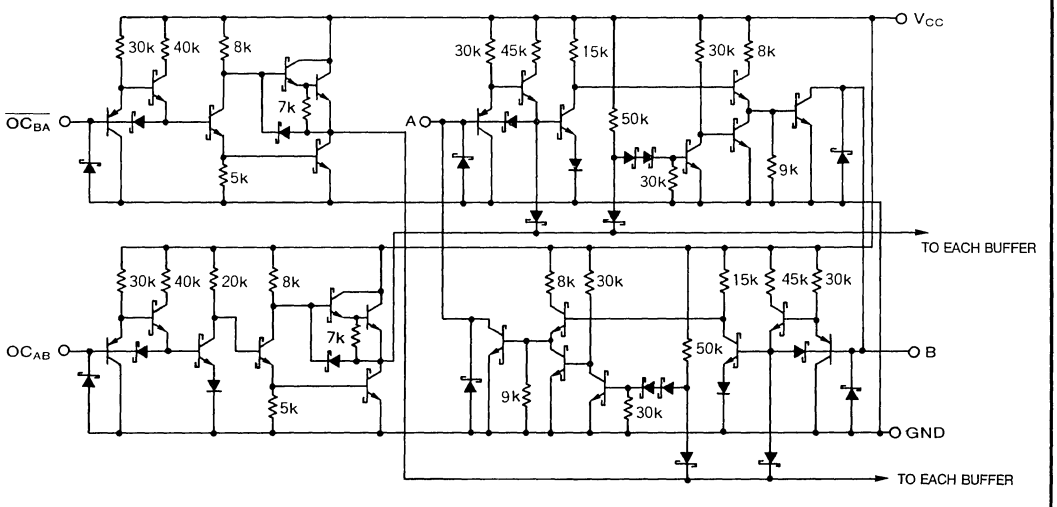
The functions and pin connections of this device are identical to those of M74ALS1623P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT. Ω

# OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (NONINVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC_{BA}}$ | $OC_{AB}$ | A | B |
| L | L | O | I |
| H | H | I | O |
| H | L | H | H |
| L | H | * | * |

Note 1: I : Input pins
O : Output pins
* In this case, data can be latched with the procedure shown below.

(1) Apply the data to be stored to A or B. ($OC_{AB}$ and $\overline{OC_{BA}}$ must be equally high or equally low)

(2) Set $OC_{AB}$ high and $\overline{OC_{BA}}$ low respectively.

(3) Remove the data

(4) The data applied in (1) is stored. If voltage is applied to A or B in this condition, the device may be damaged. Change the status of $OC_{AB}$ or $\overline{OC_{BA}}$ before applying voltage.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+7 | V |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state | −0.5~+7 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 16 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=8mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=16mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | mA |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | |
| $I_{IH}$ | High-level input current | A, B | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | | | | | 20 | |
| $I_{IL}$ | Low-level input current | A, B | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | | | | | −0.1 | |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 20 | 28 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 23 | 32 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 25 | 36 | mA |

* All typical values are at $V_{CC}$=5V, $T_a$=25°C.

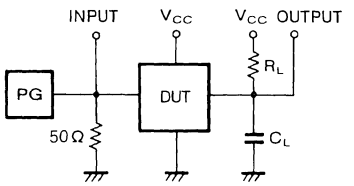
## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (NONINVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_L$=680Ω; $T_a$=0~70°C Min | Typ * | Max | $T_a$=−20~+75°C Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A, B | B, A | 12 | 25 | 50 | 12 | 25 | 51 | ns |
| $t_{PHL}$ | | | | 8 | 26 | 40 | 8 | 26 | 41 | |
| $t_{PLH}$ | | $\overline{OC_{BA}}$ | A | 12 | 21 | 45 | 12 | 21 | 46 | ns |
| $t_{PHL}$ | | | | 15 | 37 | 60 | 15 | 37 | 61 | |
| $t_{PLH}$ | | $OC_{AB}$ | B | 15 | 25 | 45 | 15 | 25 | 46 | ns |
| $t_{PHL}$ | | | | 15 | 39 | 60 | 15 | 39 | 61 | |

* All typical values are at $V_{CC}$=5V, $T_a$=25°C

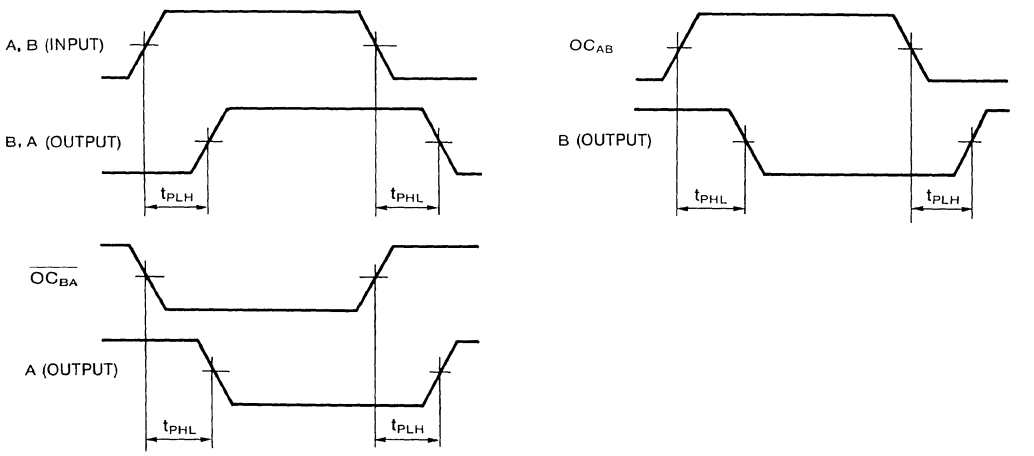
Note 2 Measurement circuit




(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS1622P

## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS1622P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with inverted open collector outputs.

## FEATURES

- Low-power version of M74ALS622P
- Two-way transmission or isolation between two 8-bit data
- Open collector output
- High fan-out ($I_{OL}$ = 16mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

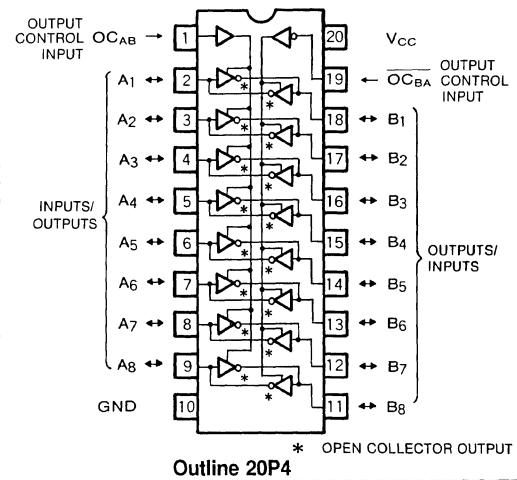
The inputs and outputs are mutually connected to form two-way buffers with inverted open collector outputs.

The input/output direction is controlled by $OC_{AB}$ and $\overline{OC_{BA}}$.

When $OC_{AB}$ and $\overline{OC_{BA}}$ are high, pins A are made the input pins and pins B are made the output pins. When $OC_{AB}$ and $OC_{BA}$ are low, B are made the input pins and A are made the output pins. When $OC_{AB}$ is low and $\overline{OC_{BA}}$ is high, both A and B become high and A and B are isolated. Latch operation is possible when $OC_{AB}$ is high and $\overline{OC_{BA}}$ is low.

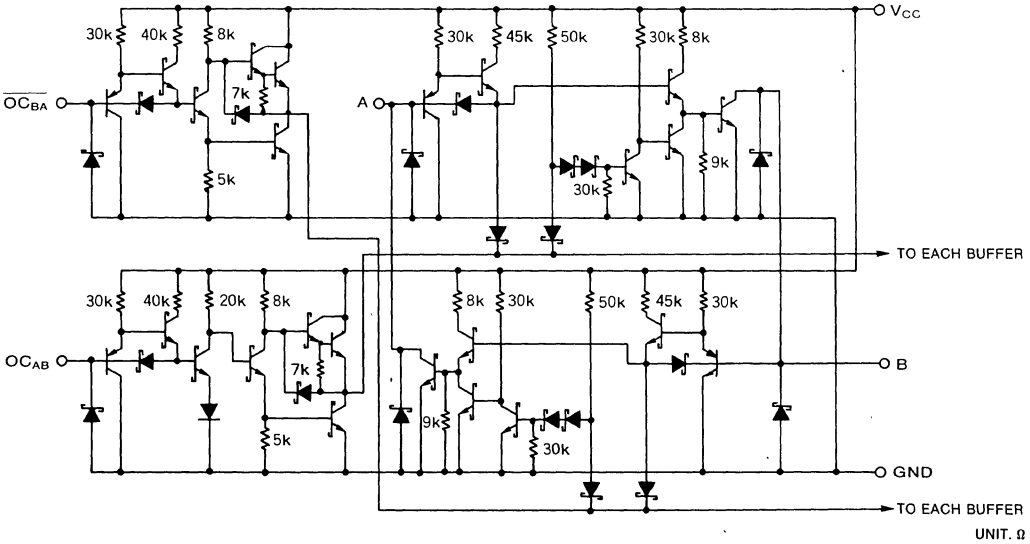
The functions and pin connections of this device are identical to those of M74ALS1620P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

## CIRCUIT SCHEMATIC (EACH BUFFER)






MITSUBISHI ELECTRIC

# OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC_{BA}}$ | $OC_{AB}$ | A | B |
| L | L | $\overline{O}$ | I |
| H | H | I | $\overline{O}$ |
| H | L | H | H |
| L | H | * | * |

Note 1: I Input pins

$\overline{O}$ Output pins (inverted output)

* In this case, data can be latched with the procedure shown below

(1) Apply the data to be stored to A or B. ($OC_{AB}$ and $\overline{OC_{BA}}$ must be equally high or equally low)

(2) Set $OC_{AB}$ high and $\overline{OC_{BA}}$ low respectively.

(3) Remove the data

(4) The data applied in (1) is stored If voltage is applied to A or B in this condition, the device may be damaged Change the status of $OC_{AB}$ or $\overline{OC_{BA}}$ before applying voltage

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+7 | V |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state | −0.5~+7 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 16 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=8mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=16mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | mA |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | |
| $I_{IH}$ | High-level input current | A, B | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | | | | | 20 | |
| $I_{IL}$ | Low-level input current | A, B | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | | | | | −0.1 | |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 8 | 12 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 12 | 18 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 9 | 13 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

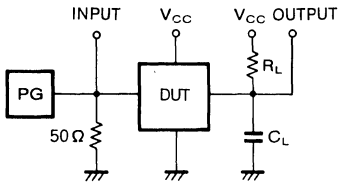
## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_L$=680Ω; $T_a$=0~70℃ Min | $T_a$=0~70℃ Typ * | $T_a$=0~70℃ Max | $T_a$=−20~+75℃ Min | $T_a$=−20~+75℃ Typ * | $T_a$=−20~+75℃ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A, B | B, A | 15 | 26 | 50 | 15 | 26 | 51 | ns |
| $t_{PHL}$ | | | | 8 | 25 | 40 | 8 | 25 | 41 | |
| $t_{PLH}$ | | $\overline{OC_{BA}}$ | A | 12 | 19 | 40 | 12 | 19 | 41 | ns |
| $t_{PHL}$ | | | | 15 | 37 | 60 | 15 | 37 | 61 | |
| $t_{PLH}$ | | $OC_{AB}$ | B | 15 | 24 | 45 | 15 | 24 | 46 | ns |
| $t_{PHL}$ | | | | 15 | 39 | 60 | 15 | 39 | 61 | |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 2: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

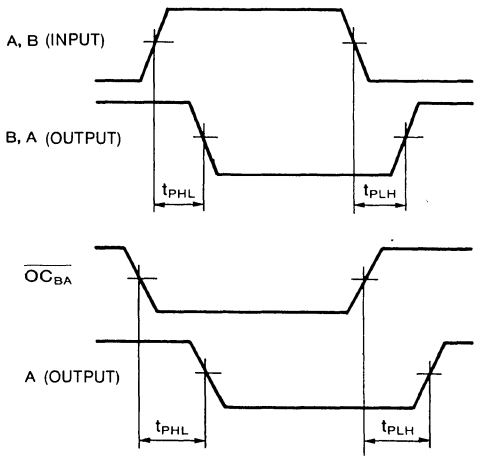
$V_{IH}$=3.5V, $V_{IL}$=0.3V

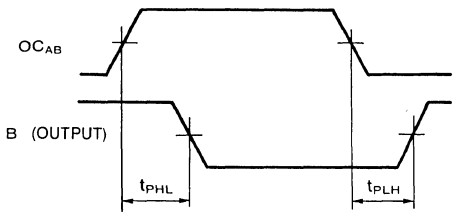
duty cycle=50%

$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

### TIMING DIAGRAM (Reference level = 1.3V)






MITSUBISHI ELECTRIC

# M74ALS1623P

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS1623P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with 3-state noninverted outputs.

## FEATURES

- Low-power version of M74ALS623P
- Two-way transmission or isolation between two 8-bit data
- High fan-out ($I_{OL}$ = 16mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

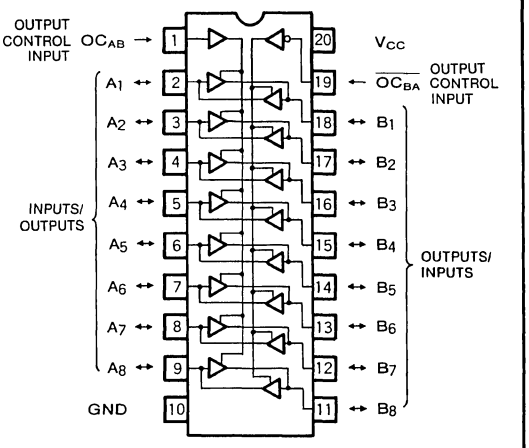
## FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with 3-state noninverted outputs.

The input/output direction is controlled by $OC_{AB}$ and $\overline{OC_{BA}}$.

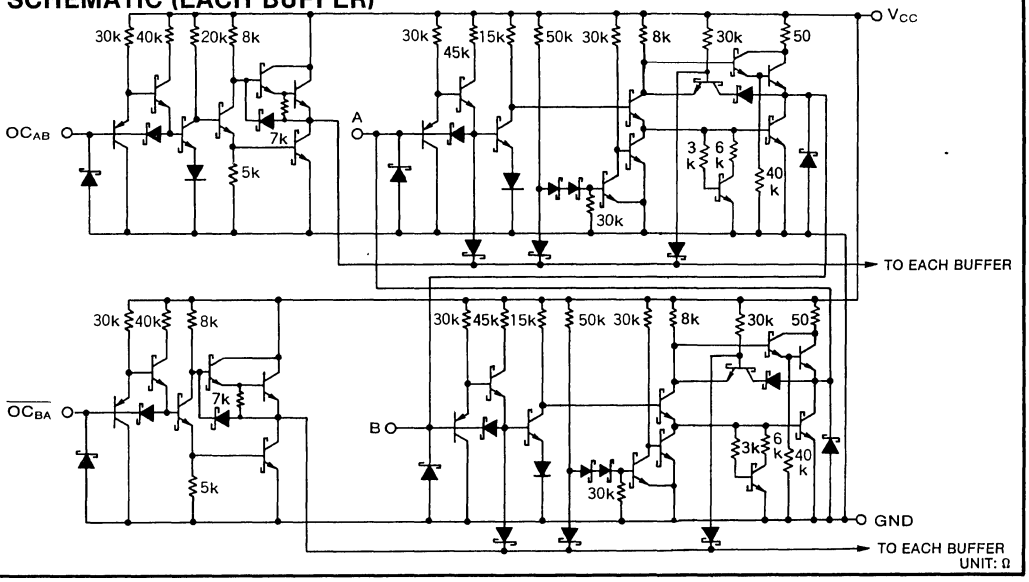
When $OC_{AB}$ and $\overline{OC_{BA}}$ are high, pins A are made the input pins and pins B are made the output pins. When $OC_{AB}$ and $\overline{OC_{BA}}$ are low, B are made the input pins and A are made the output pins. When $OC_{AB}$ is low and $\overline{OC_{BA}}$ is high, both A and B are in the high-impedance state and A and B are isolated. Latch operation is possible when $OC_{AB}$ is high and $\overline{OC_{BA}}$ is low.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

## CIRCUIT SCHEMATIC (EACH BUFFER)



# OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC_{BA}}$ | $OC_{AB}$ | A | B |
| L | L | O | I |
| H | H | I | O |
| H | L | Z | Z |
| L | H | * | * |

Note 1: I : Input pins
O : Output pins (noninverted output)
Z : High-impedance state (A and B are isolated)
* : In this case, data can be latched with the procedure shown below.
(1) Apply the data to be stored to A or B ($OC_{AB}$ and $\overline{OC_{BA}}$ must be equally high or equally low.)
(2) Set $OC_{AB}$ high and $\overline{OC_{BA}}$ low respectively.
(3) Remove the data.
(4) The data applied in (1) is stored. If voltage is applied to A or B in this condition, the device may be damaged. Change the status of $OC_{AB}$ or $\overline{OC_{BA}}$ before applying voltage.

## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | A, B | | −0.5 ~ +5.5 | V |
| | | $OC_{AB}$, $\overline{OC_{BA}}$ | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | | High-level state or high-impedance state | −0.5 ~ +5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20 ~ +75 | °C |
| $T_{stg}$ | Storage temperature range | | | −65 ~ +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 16 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=8mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=16mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | $OC_{AB}$, $\overline{OC_{BA}}$ | $V_{CC}$=5.5V, $V_I$=7.0V | | | | 0.1 | mA |
| | | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | |
| $I_{IH}$ | High-level input current (Note 2) | $OC_{AB}$, $\overline{OC_{BA}}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current (Note 3) | $OC_{AB}$, $\overline{OC_{BA}}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 20 | 30 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 23 | 34 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 26 | 38 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 2: For A and B, $I_{IH}$ includes off-state high-level output current $I_{OZH}$.

Note 3: For A and B, $I_{IL}$ includes off-state low-level output current $I_{OZL}$.

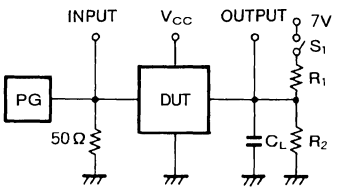
## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Output | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | Typ * | Max | $T_a$=−20~+75℃ Min | Typ * | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A | B | 4 | 9 | 15 | 4 | 9 | 16 | ns |
| $t_{PHL}$ | | | | 4 | 9 | 15 | 4 | 9 | 16 | |
| $t_{PLH}$ | | B | A | 4 | 9 | 15 | 4 | 9 | 16 | ns |
| $t_{PHL}$ | | | | 4 | 9 | 15 | 4 | 9 | 16 | |
| $t_{PZH}$ | Output enable time | $\overline{OC_{BA}}$ | A | 8 | 15 | 27 | 8 | 15 | 28 | ns |
| $t_{PZL}$ | | | | 8 | 16 | 27 | 8 | 16 | 28 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC_{BA}}$ | A | 3 | 10 | 23 | 3 | 10 | 24 | ns |
| $t_{PLZ}$ | | | | 4 | 13 | 28 | 4 | 13 | 29 | |
| $t_{PZH}$ | Output enable time | $OC_{AB}$ | B | 8 | 16 | 24 | 8 | 16 | 25 | ns |
| $t_{PZL}$ | | | | 8 | 18 | 30 | 8 | 18 | 31 | |
| $t_{PHZ}$ | Output disable time | $OC_{AB}$ | B | 3 | 14 | 23 | 3 | 14 | 24 | ns |
| $t_{PLZ}$ | | | | 4 | 17 | 28 | 4 | 17 | 29 | |

* All typical values are at $V_{CC}$=5V, $T_a$=25°C

Note 4: Measurement circuit

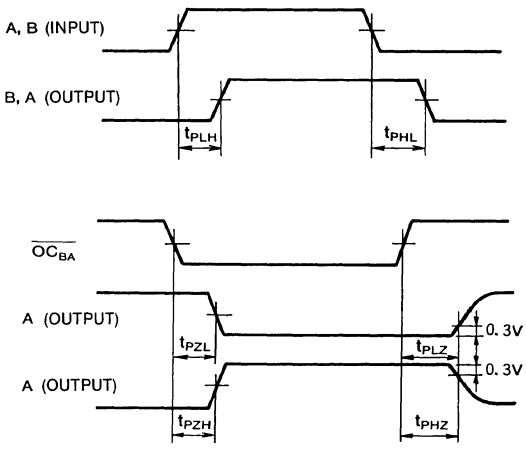


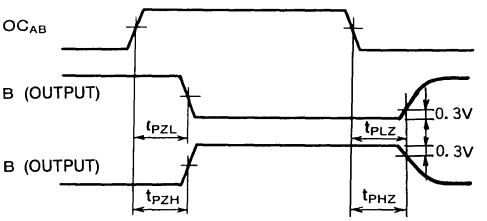

(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS1640P

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS1640P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with 3-state inverted outputs.

## FEATURES

- Low-power version of M74ALS640P
- Two-way transmission or isolation between two 8-bit data
- High fan-out ($I_{OL}$ = 16mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

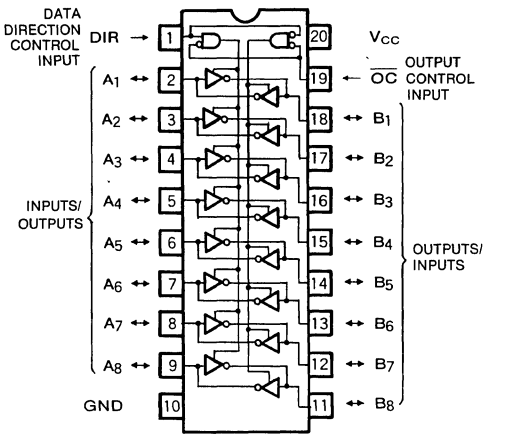
## FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with 3-state inverted outputs.

The input/output direction is controlled by DIR.

When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins. When $\overline{OC}$ is high, both A and B are in the high-impedance state and A and B are isolated.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC}$ | DIR | A | B |
| L | L | $\overline{O}$ | I |
| L | H | I | $\overline{O}$ |
| H | X | Z | Z |

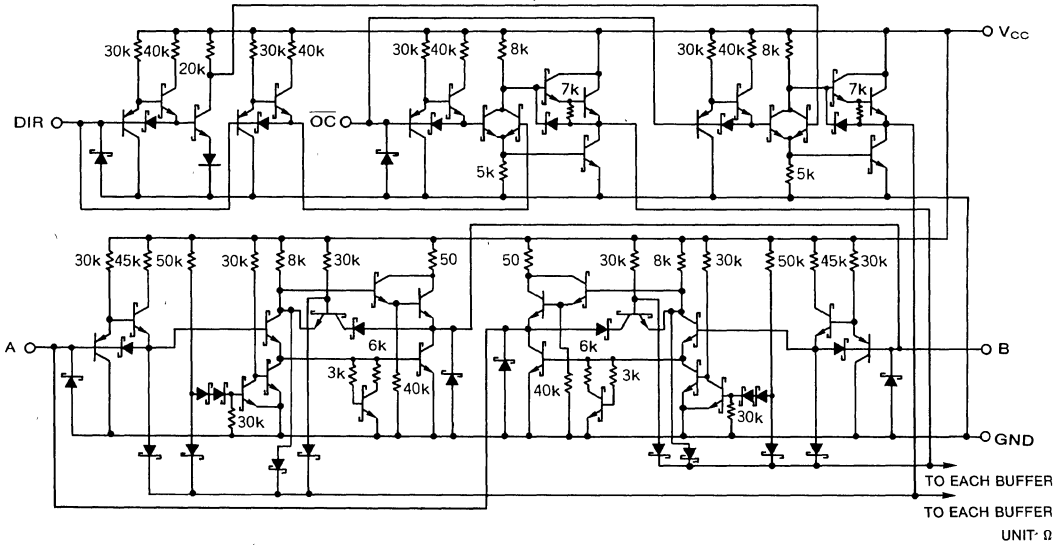
Note 1: I : Input pins

$\overline{O}$ : Output pins (inverted output)

Z : High-impedance state (A and B are isolated)

X : Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)






MITSUBISHI ELECTRIC

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+5.5 | V |
| | | DIR, $\overline{OC}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state or high-impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 16 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=8mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=16mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_{CC}$=7V | | | | 0.1 | mA |
| | | A, B | $V_{CC}$=5.5V, $V_{CC}$=5.5V | | | | 0.1 | |
| $I_{IH}$ | High-level input current (Note 2) | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current (Note 3) | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 16 | 22 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 20 | 28 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 21 | 31 | mA |

* : All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C

Note 2: For A and B, $I_{IH}$ includes off-state high-level output current $I_{OZH}$.

Note 3: For A and B, $I_{IL}$ includes off-state low-level output current $I_{OZL}$.

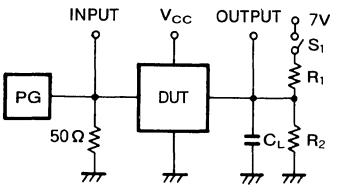
## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A, B | B, A | 4 | 6 | 17 | 4 | 6 | 18 | ns |
| $t_{PHL}$ | | | | 3 | 6 | 11 | 3 | 6 | 12 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | A, B | 5 | 12 | 23 | 5 | 12 | 24 | ns |
| $t_{PZL}$ | | | | 10 | 18 | 27 | 10 | 18 | 28 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | A, B | 3 | 6 | 13 | 3 | 6 | 14 | ns |
| $t_{PLZ}$ | | | | 4 | 7 | 21 | 4 | 7 | 22 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 4: Measurement circuit

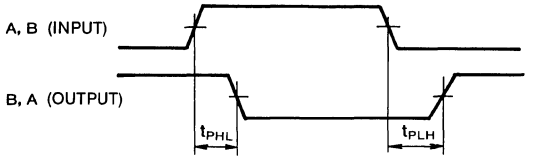


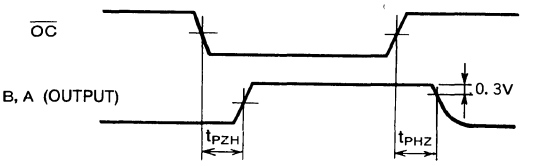

(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

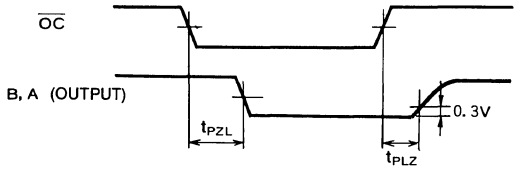
(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS1641P

## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS1641P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with noninverted open collector outputs.

## FEATURES

- Low-power version of M74ALS641P
- Two-way transmission or isolation between two 8-bit data
- Open collector output
- High fan-out ($I_{OL}$ = 16mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with noninverted open collector outputs.

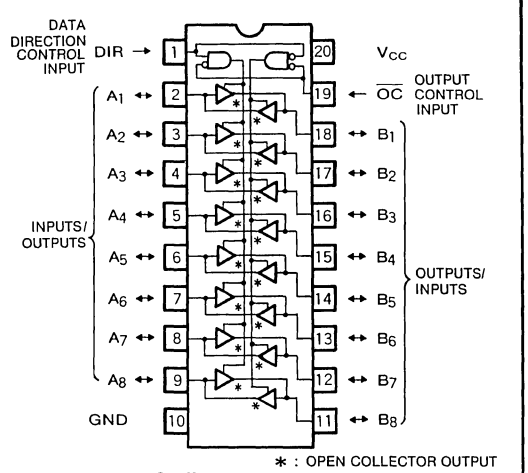
The input/output direction is controlled by DIR.

When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins.

When $\overline{OC}$ is high, both A and B become high and A and B are isolated.

The functions and pin connections of this device are identical to those of M74ALS1645P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.

## PIN CONFIGURATION (TOP VIEW)



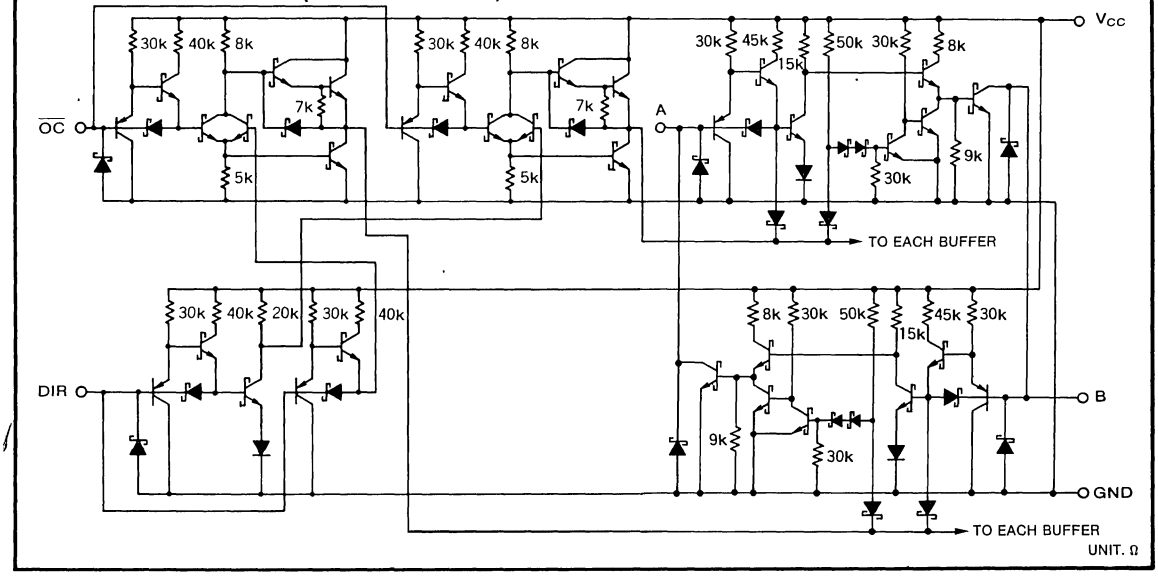

Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC}$ | DIR | A | B |
| L | L | O | I |
| L | H | I | O |
| H | X | H | H |

Note 1: I Input pins
O . Output pins (noninverted output)
X : Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)



## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (NONINVERTED)

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+7 | V |
| | | DIR, $\overline{OC}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state | −0.5~+7 | V |
| Topr | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| Tstg | Storage temperature range | | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 16 | mA |
| Topr | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=8mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=16mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | DIR, $\overline{OC}$ | $V_{CC}$=5.5V | $V_I$=7V | | | 0.1 | mA |
| | | A, B | | $V_I$=5.5V | | | 0.1 | |
| $I_{IH}$ | High-level input current | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 18 | 27 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | | 31 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 23 | 35 | mA |

* : All typical values are at $V_{CC}$=5V, $T_a$=25°C.

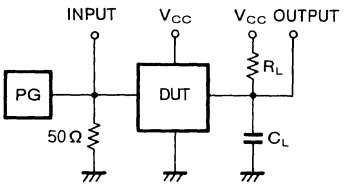
## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (NONINVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_L$=680Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | Inputs | Outputs | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A, B | B, A | 12 | 31 | 50 | 12 | 31 | 51 | ns |
| $t_{PHL}$ | | | | 8 | 22 | 40 | 8 | 22 | 41 | |
| $t_{PLH}$ | | $\overline{OC}$, DIR | A, B | 12 | 18 | 40 | 12 | 18 | 41 | ns |
| $t_{PHL}$ | | | | 15 | 36 | 60 | 15 | 36 | 61 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

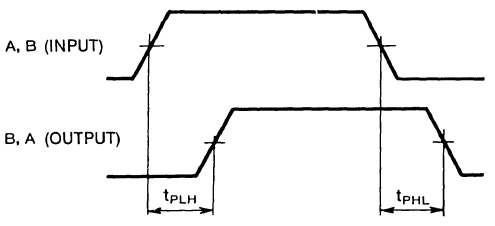
Note 2: Measurement circuit

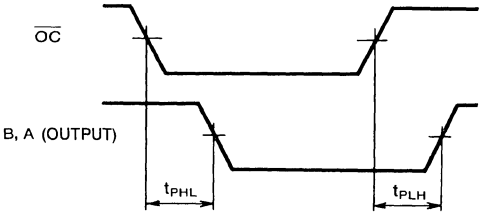


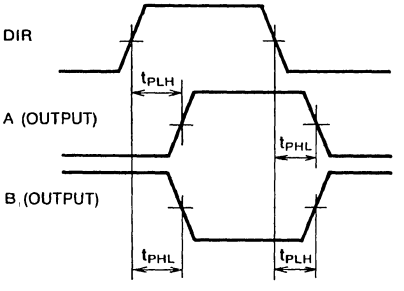

(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS1642P

## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

## DESCRIPTION

The M74ALS1642P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with inverted open collector outputs.

## FEATURES

- Low-power version of M74ALS642P
- Two-way transmission or isolation between two 8-bit data
- Open collector output
- High fan-out ($I_{OL}$ = 16mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with inverted open collector outputs.

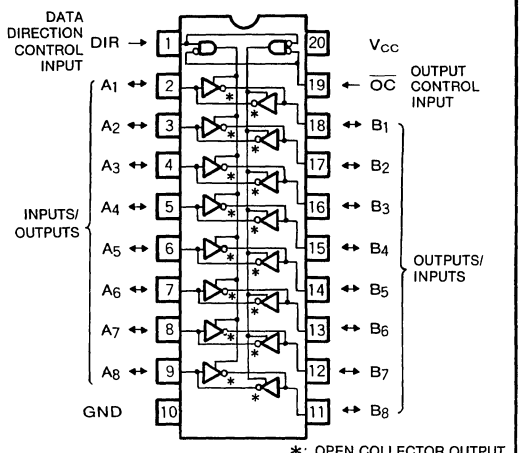
The input/output direction is controlled by DIR.

When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins.

When $\overline{OC}$ is high, both A and B become high and A and B are isolated.

The functions and pin connections of this device are identical to those of M74ALS1640P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.

## PIN CONFIGURATION (TOP VIEW)



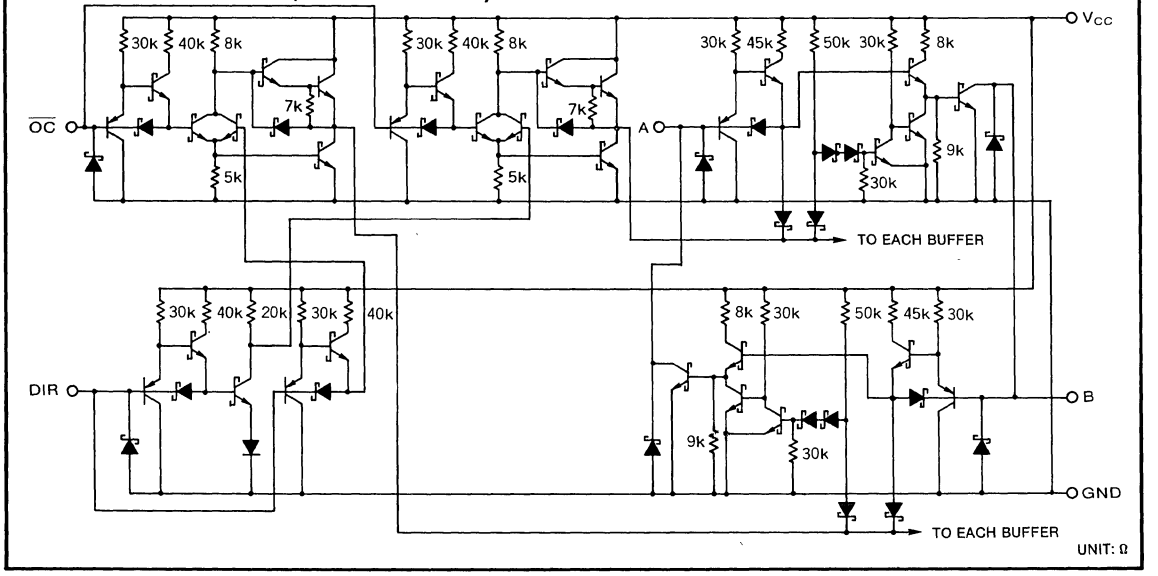

Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC}$ | DIR | A | B |
| L | L | $\overline{O}$ | I |
| L | H | I | $\overline{O}$ |
| H | X | H | H |

Note 1: I : Input pins
$\overline{O}$ : Output pins (inverted output)
X : Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT: Ω



MITSUBISHI ELECTRIC

## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+7 | V |
| | | DIR, $\overline{OC}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state | −0.5~+7 | V |
| Topr | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| Tstg | Storage temperature range | | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 16 | mA |
| Topr | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=8mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=16mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | DIR, $\overline{OC}$ | $V_{CC}$=5.5V | $V_I$=7V | | | 0.1 | mA |
| | | A, B | | $V_I$=5.5V | | | 0.1 | |
| $I_{IH}$ | High-level input current | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 8 | 13 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 12 | 18 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 9 | 14 | mA |

* : All typical values are at $V_{CC}$=5V, $T_a$=25°C.

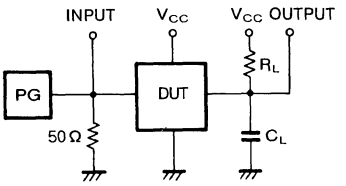
## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_L$=680Ω | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | | Min | Typ * | Max | Min | Typ * | Max | |
| $t_{PLH}$ | Propagation time | A, B | B, A | 15 | 25 | 50 | 15 | 25 | 51 | ns |
| $t_{PHL}$ | | | | 8 | 25 | 40 | 8 | 25 | 41 | |
| $t_{PLH}$ | | $\overline{OC}$, DIR | A, B | 12 | 16 | 40 | 12 | 16 | 41 | ns |
| $t_{PHL}$ | | | | 20 | 39 | 70 | 20 | 39 | 71 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2. Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

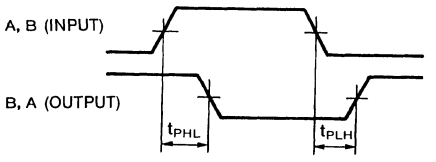
$V_{IH}$=3.5V, $V_{IL}$=0.3V

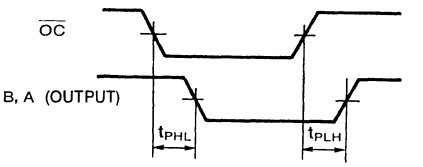
duty cycle=50%

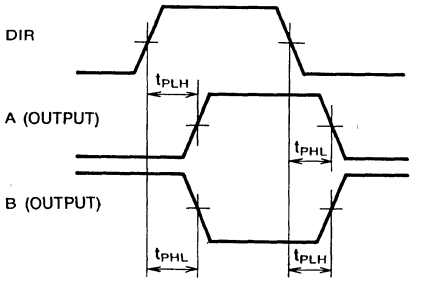
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

### TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS1643P

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT

## DESCRIPTION

The M74ALS1643P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with inverted and noninverted 3-state outputs.

## FEATURES

- Low-power version of M74ALS643P
- Two-way transmission or isolation between two 8-bit data
- High fan-out ($I_{OL}$ = 16mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

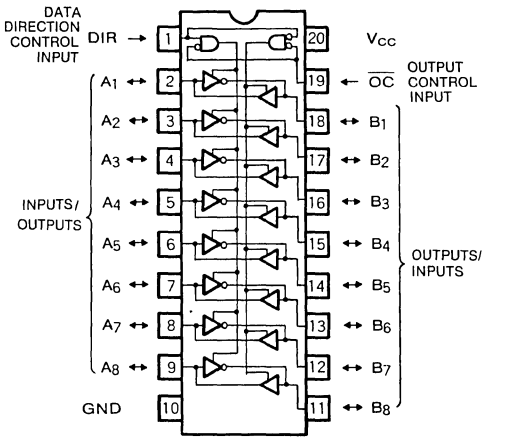
## FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with inverted and noninverted 3-state outputs.

The input/output direction is controlled by DIR.

When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins. When $\overline{OC}$ is high, both A and B are in the high-impedance state and A and B are isolated.

## PIN CONFIGURATION (TOP VIEW)



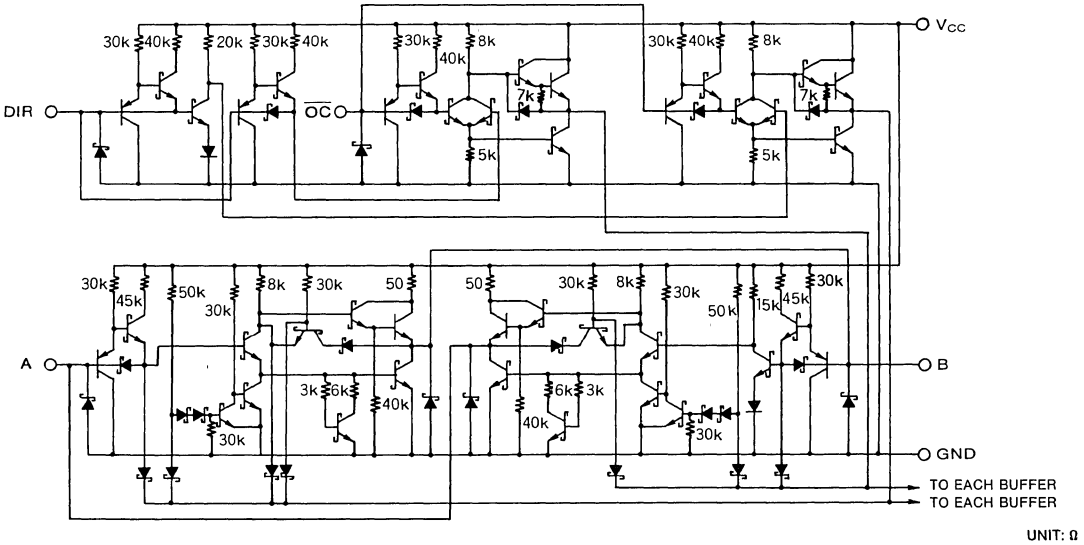

Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC}$ | DIR | A | B |
| L | L | O | I |
| L | H | I | $\overline{O}$ |
| H | X | Z | Z |

Note 1: I : Input pins
O : Output pins (noninverted output)
$\overline{O}$ : Output pins (inverted output)
Z : High-impedance state (A and B are isolated)
X : Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT: Ω

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | A, B | | −0.5 ~ +5.5 | V |
| | | DIR, $\overline{OC}$ | | −0.5 ~ +7 | V |
| $V_O$ | Output voltage | | High-level state or high-impedance state | −0.5 ~ +5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20 ~ +75 | ℃ |
| $T_{stg}$ | Storage temperature range | | | −65 ~ +150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 16 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=8mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=16mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | DIR, $\overline{OC}$ | $V_{CC}$=5.5V | $V_I$=7V | | | 0.1 | mA |
| | | A, B | | $V_I$=5.5V | | | 0.1 | |
| $I_{IH}$ | High-level input current (Note 2) | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current (Note 3) | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 19 | 26 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 22 | 32 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 24 | 35 | mA |

* : All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2: For A and B, $I_{IH}$ includes off-state high-level output current $I_{OZH}$.

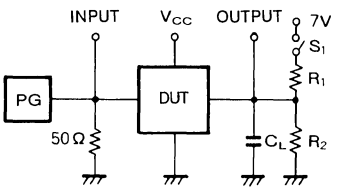
Note 3: For A and B, $I_{IL}$ includes off-state low-level output current $I_{OZL}$.

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Output | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | $T_a$=0~70℃ Typ* | $T_a$=0~70℃ Max | $T_a$=−20~+75℃ Min | $T_a$=−20~+75℃ Typ* | $T_a$=−20~+75℃ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A | B | 4 | 6 | 13 | 4 | 6 | 14 | ns |
| $t_{PHL}$ | | | | 3 | 5 | 11 | 3 | 5 | 12 | |
| $t_{PLH}$ | | B | A | 4 | 9 | 13 | 4 | 9 | 14 | ns |
| $t_{PHL}$ | | | | 4 | 9 | 13 | 4 | 9 | 14 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | A | 10 | 16 | 25 | 10 | 16 | 26 | ns |
| $t_{PZL}$ | | | | 13 | 17 | 29 | 13 | 17 | 30 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | A | 4 | 8 | 18 | 4 | 8 | 19 | ns |
| $t_{PLZ}$ | | | | 4 | 10 | 21 | 4 | 10 | 22 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | B | 5 | 12 | 23 | 5 | 12 | 24 | ns |
| $t_{PZL}$ | | | | 10 | 18 | 27 | 10 | 18 | 28 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | B | 3 | 6 | 13 | 3 | 6 | 14 | ns |
| $t_{PLZ}$ | | | | 4 | 7 | 21 | 4 | 7 | 22 | |

*. All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 4: Measurement circuit

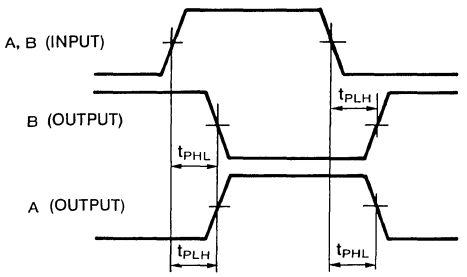


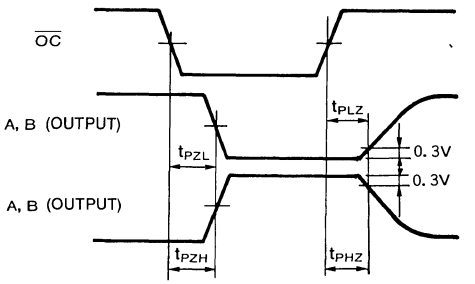

(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

## TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS1644P

## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

## DESCRIPTION

The M74ALS1644P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with inverted and noninverted open collector outputs.

## FEATURES

- Low-power version of M74ALS644P
- Two-way transmission or isolation between two 8-bit data
- Open collector output
- High fan-out ($I_{OL}$ = 16mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with inverted and noninverted open collector outputs.

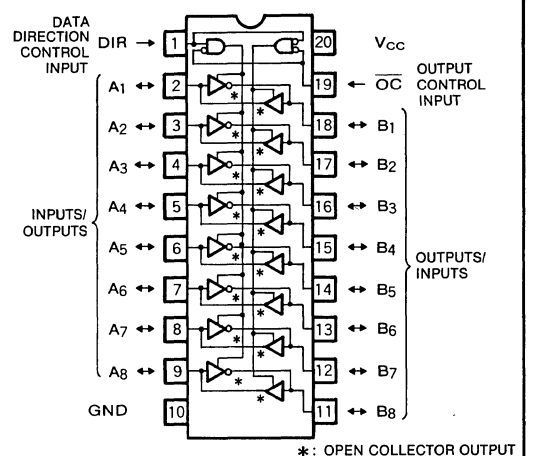
The input/output direction is controlled by DIR.

When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins.

When $\overline{OC}$ is high, both A and B become high and A and B are isolated.

The functions and pin connections of this device are identical to those of M74ALS1643P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.

## PIN CONFIGURATION (TOP VIEW)



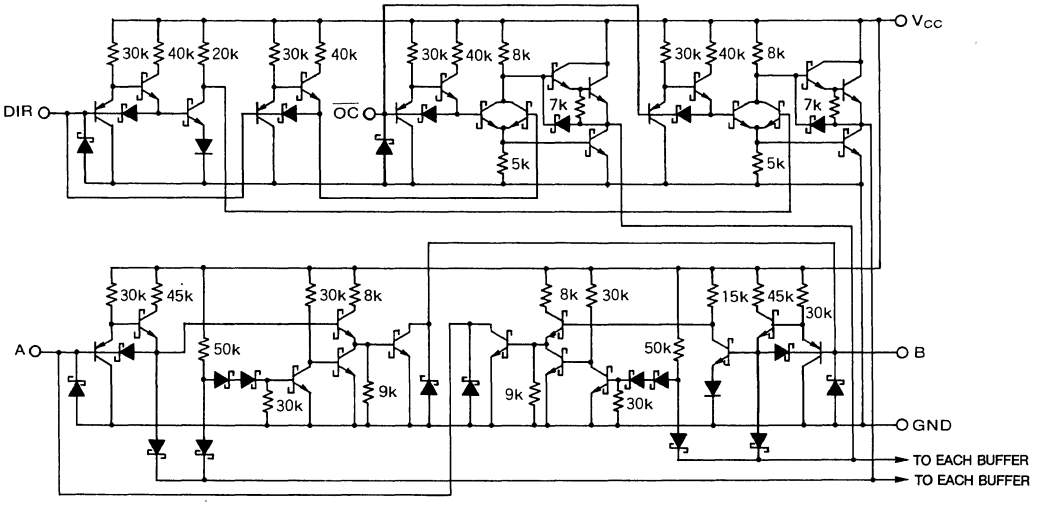

Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC}$ | DIR | A | B |
| L | L | O | I |
| L | H | I | $\overline{O}$ |
| H | X | H | H |

Note 1: I : Input pins
O : Output pins (noninverted output)
$\overline{O}$ : Output pins (inverted output)
X : Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)




UNIT. Ω



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## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+7 | V |
| | | DIR, $\overline{OC}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state | −0.5~+7 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | 0 | | 16 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$=4.5V, $V_O$=5.5V | | | | 0.1 | mA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=8mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=16mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | A, B | $V_{CC}$=5.5V | $V_I$=5.5V | | | 0.1 | mA |
| | | DIR, $\overline{OC}$ | | $V_I$=7V | | | 0.1 | |
| $I_{IH}$ | High-level input current | A, B | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | DIR, $\overline{OC}$ | | | | | 20 | |
| $I_{IL}$ | Low-level input current | A, B | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | DIR, $\overline{OC}$ | | | | | −0.1 | |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 16 | 23 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 20 | 28 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 18 | 25 | mA |

* : All typical values are at $V_{CC}$=5V, $T_a$=25°C.

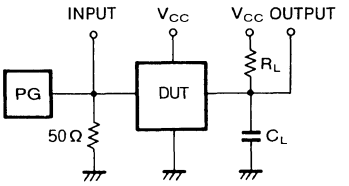
## OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Input | Output | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 2), $C_L$=50pF, $R_L$=500Ω; $T_a$=0~70℃ Min | $T_a$=0~70℃ Typ* | $T_a$=0~70℃ Max | $T_a$=−20~+75℃ Min | $T_a$=−20~+75℃ Typ* | $T_a$=−20~+75℃ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A | B | 15 | 24 | 50 | 15 | 24 | 51 | ns |
| $t_{PHL}$ | | | | 8 | 23 | 40 | 8 | 23 | 41 | |
| $t_{PLH}$ | | B | A | 15 | 26 | 50 | 15 | 26 | 51 | ns |
| $t_{PHL}$ | | | | 8 | 20 | 32 | 8 | 20 | 33 | |
| $t_{PLH}$ | | $\overline{OC}$ | A | 12 | 19 | 37 | 12 | 19 | 38 | ns |
| $t_{PHL}$ | | | | 15 | 32 | 60 | 15 | 32 | 61 | |
| $t_{PLH}$ | | $\overline{OC}$ | B | 12 | 16 | 33 | 12 | 16 | 34 | ns |
| $t_{PHL}$ | | | | 18 | 36 | 60 | 18 | 36 | 61 | |
| $t_{PLH}$ | | DIR | A | 10 | 17 | 30 | 10 | 17 | 31 | ns |
| $t_{PHL}$ | | | | 12 | 32 | 60 | 12 | 32 | 61 | |
| $t_{PLH}$ | | DIR | B | 15 | 24 | 45 | 15 | 24 | 46 | ns |
| $t_{PHL}$ | | | | 18 | 38 | 65 | 18 | 38 | 66 | |

* All typical values are at $V_{CC}$=5V, Ta=25°C

Note 2 Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

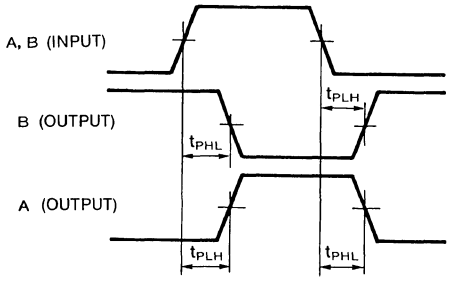
$V_{IH}$=3.5V, $V_{IL}$=0.3V

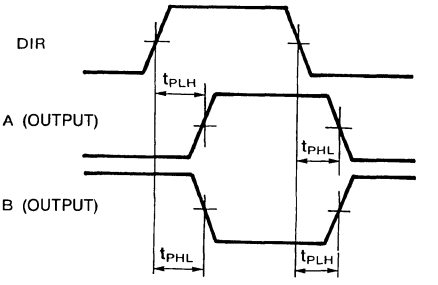
duty cycle=50%

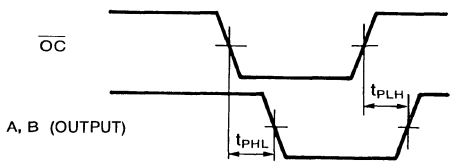
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance

## TIMING DIAGRAM (Reference level = 1.3V)



# M74ALS1645P

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

## DESCRIPTION

The M74ALS1645P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with 3-state noninverted outputs.

## FEATURES

- Low-power version of M74ALS645P
- Two-way transmission or isolation between two 8-bit data
- High fan-out ($I_{OL}$ = 16mA, $I_{OH}$ = −15mA)
- Wide operating temperature range ($T_a$ = −20 ~ +75°C)

## APPLICATIONS

General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION

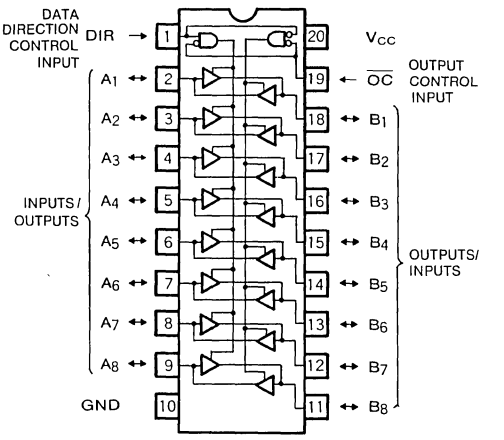
The inputs and outputs are mutually connected to form two-way buffers with 3-state noninverted outputs.

The input/output direction is controlled by DIR.

When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins. When $\overline{OC}$ is high, both A and B are in the high-impedance state and A and B are isolated.

The M74ALS1245P, which, except for its name, is identical in all respects to the M74ALS1645P, is also available.

## PIN CONFIGURATION (TOP VIEW)



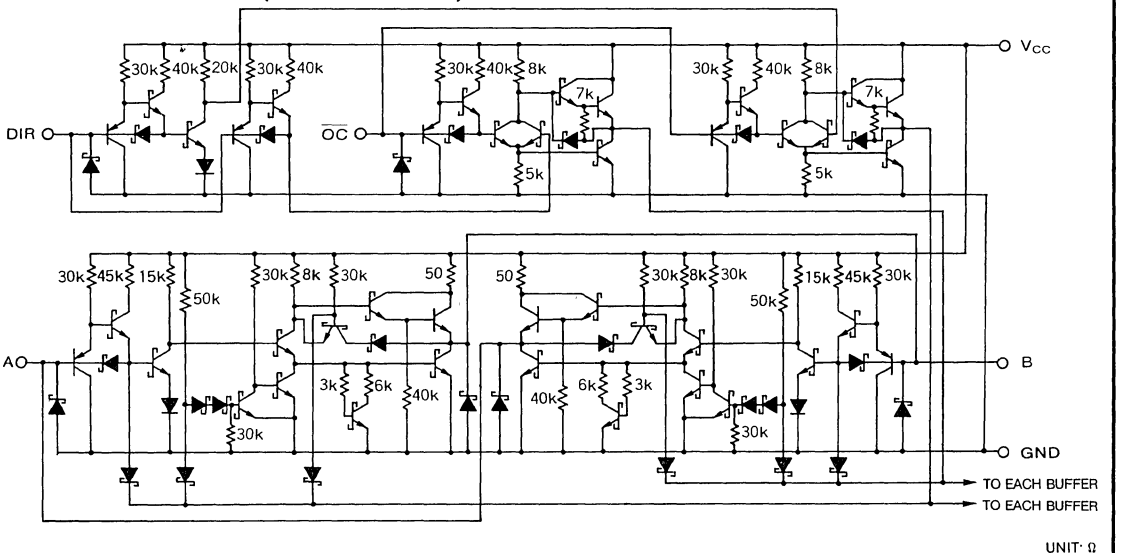

Outline 20P4

## FUNCTION TABLE (Note 1)

| Inputs | | Input / Output | |
|---|---|---|---|
| $\overline{OC}$ | DIR | A | B |
| L | L | O | I |
| L | H | I | O |
| H | X | Z | Z |

Note 1. I Input pins
O Output pins (noninverted output)
Z High-impedance state (A and B are isolated)
X : Irrelevant

## CIRCUIT SCHEMATIC (EACH BUFFER)



## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Limits | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5~+7 | V |
| $V_I$ | Input voltage | A, B | | −0.5~+5.5 | V |
| | | DIR, $\overline{OC}$ | | −0.5~+7 | V |
| $V_O$ | Output voltage | | High-level state or high-impedance state | −0.5~+5.5 | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | | −20~+75 | ℃ |
| $T_{stg}$ | Storage temperature range | | | −65~+150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −15 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 16 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | ℃ |

### ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ * | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5V | $I_{OH}$=−3mA | 2.4 | 3.2 | | V |
| | | | | $I_{OH}$=−15mA | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=8mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=16mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | A, B | $V_{CC}$=5.5V, $V_I$=5.5V | | | | 0.1 | |
| $I_{IH}$ | High-level input current (Note 2) | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | A, B | | | | | 20 | |
| $I_{IL}$ | Low-level input current (Note 3) | DIR, $\overline{OC}$ | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.1 | mA |
| | | A, B | | | | | −0.1 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CCH}$ | Supply current, all outputs high | | $V_{CC}$=5.5V | | | 20 | 32 | mA |
| $I_{CCL}$ | Supply current, all outputs low | | $V_{CC}$=5.5V | | | 23 | 37 | mA |
| $I_{CCZ}$ | Supply current, all outputs disabled | | $V_{CC}$=5.5V | | | 25 | 39 | mA |

* : All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 2 For A and B, $I_{IH}$ includes off-state high-level output current $I_{OZH}$.

Note 3: For A and B, $I_{IL}$ includes off-state low-level output current $I_{OZL}$.

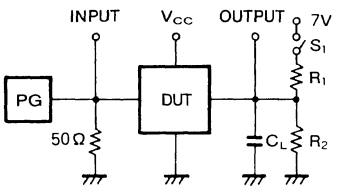
## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

### SWITCHING CHARACTERISTICS

| Symbol | Parameter | Inputs | Outputs | Test conditions/Limits: $V_{CC}$=4.5~5.5V (Note 4), $C_L$=50pF, $R_1$=500Ω, $R_2$=500Ω; $T_a$=0~70℃ Min | $T_a$=0~70℃ Typ * | $T_a$=0~70℃ Max | $T_a$=−20~+75℃ Min | $T_a$=−20~+75℃ Typ * | $T_a$=−20~+75℃ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation time | A, B | B, A | 4 | 9 | 13 | 4 | 9 | 14 | ns |
| $t_{PHL}$ | | | | 4 | 9 | 13 | 4 | 9 | 14 | |
| $t_{PZH}$ | Output enable time | $\overline{OC}$ | A, B | 10 | 16 | 25 | 10 | 16 | 26 | ns |
| $t_{PZL}$ | | | | 13 | 18 | 29 | 13 | 18 | 30 | |
| $t_{PHZ}$ | Output disable time | $\overline{OC}$ | A, B | 4 | 7 | 18 | 4 | 7 | 19 | ns |
| $t_{PLZ}$ | | | | 5 | 9 | 21 | 5 | 9 | 22 | |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

Note 4: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r$=2ns, $t_f$=2ns

$V_{IH}$=3.5V, $V_{IL}$=0.3V

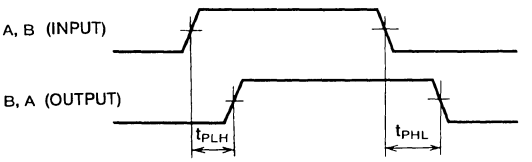
duty cycle=50%

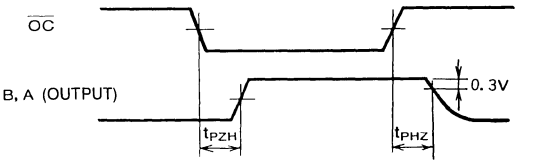
$Z_O$=50Ω

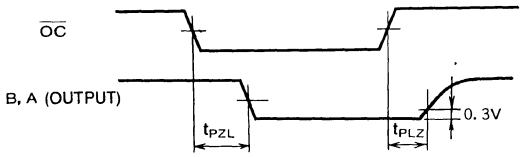
(2) $C_L$ includes probe and jig capacitance

| Parameter | $S_1$ |
|---|---|
| $t_{PLH}$ | Open |
| $t_{PHL}$ | Open |
| $t_{PZH}$ | Open |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open |
| $t_{PLZ}$ | Closed |

### TIMING DIAGRAM (Reference level = 1.3V)



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