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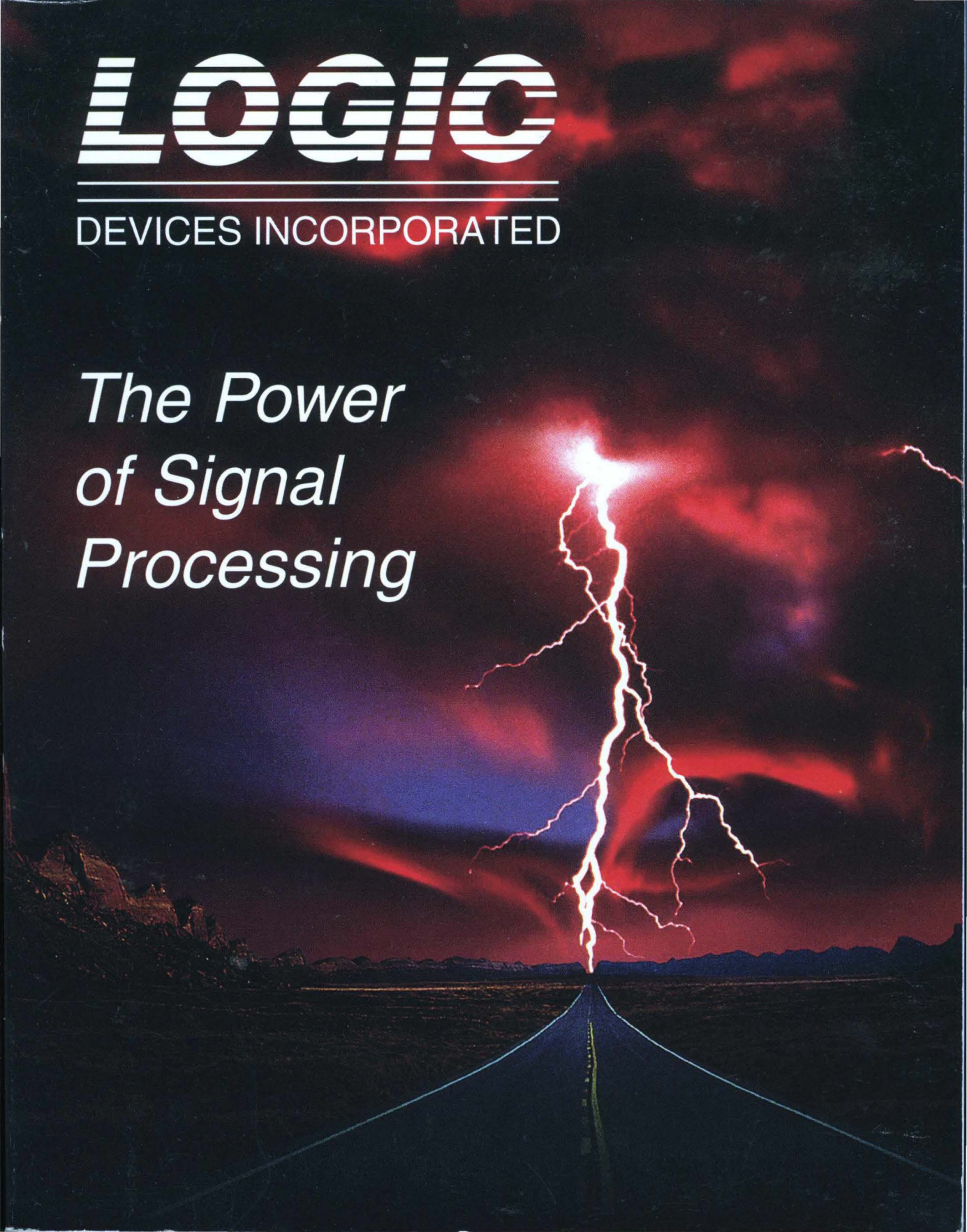
DEVICES INCORPORATED

The Power of Signal Processing



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Ordering Information

TO CONSTRUCT A VALID PART NUMBER:

In order to construct a valid LOGIC Devices part number, begin with the generic number obtained from the data sheet header. To this number, append two or three characters from the tables below indicating the desired package code, temperature range, and screening. Finally, append one or two digits indicating the performance grade desired. Most devices are offered in several speed grades with the part number suffix indicating a critical path delay in nanoseconds.

FOR MORE INFORMATION ON AVAILABLE PART NUMBERS:

All products are not offered with all combinations of package styles, temperature ranges, and screening. The Ordering Information table on the last page of each data sheet indicates explicitly all valid combinations of package, temperature, screening, and performance codes for a given product.

L	7C108	C	M	B	20	L
(1)	(2)	(3)	(4)	(5)	(6)	(7)

Key:

(1) Prefix, LOGIC Devices Inc.
(2) Device number
(3) Package code
(4) Temperature range
(5) Screening
(6) Performance/speed grade
(7) Low power designation

Package Codes

Suffix	Description
C, I*	CerDIP
D, H*	Sidebraze, Hermetic DIP
F	Flatpack
G	Ceramic Pin Grid Array
J	Plastic J-Lead Chip Carrier
K, T*	Ceramic Leadless Chip Carrier
M	CerFlat
P, N*	Plastic DIP
Q	Plastic Quad Flatpack
S	Plastic SSOP
W	Plastic SOJ (J-Lead)
Y	Ceramic SOJ (J-Lead)

*Some devices are available in packages of two widths. For devices available in a single width, C, D, K, and P are used.

Temperature Range

Suffix	Description
C	Commercial 0°C to +70°C
I	Industrial –40°C to +85°C
M	Military –55°C to +125°C

Screening

Suffix	Description
No Designator	Commercial Flow
B	MIL-STD-883 Class B Compliant

Video Imaging Products

2

LOGIC DEVICES INCORPORATED

LF2242

12/16-bit Half-Band Interpolating/ Decimating Digital Filter

FEATURES

- 40 MHz Clock Rate
- Passband (0 to $0.22f_S$) Ripple: ±0.02 dB
- Stopband ($0.28f_S$ to $0.5f_S$) Rejection: 59.4 dB
- User-Selectable 2:1 Decimation or 1:2 Interpolation
- 12-bit Two's Complement Input and 16-bit Output with User-Selectable Rounding to 9 through 16 Bits
- User-Selectable Two's Complement or Inverted Offset Binary Output Formats
- Three-State Outputs
- Replaces TRW/Raytheon TMC2242
- Package Styles Available:
  - 44-pin Plastic LCC, J-Lead
  - 44-pin Plastic Quad Flatpack

DESCRIPTION

The **LF2242** is a linear-phase, half-band (low pass) interpolating/ decimating digital filter that, unlike intricate analog filters, requires no tuning. The LF2242 can also significantly reduce the complexity of traditional analog anti-aliasing pre-filters without compromising the signal bandwidth or attenuation. This can be achieved by using the LF2242 as a decimating post-filter with an A/D converter and by sampling the signal at twice the rate needed. Likewise, by using the LF2242 as an interpolating pre-filter with a D/A converter, the corresponding analog reconstruction post-filter circuitry can be simplified.

The coefficients of the LF2242 are fixed, and the only user programming required is the selection of the mode (interpolate, decimate, or pass-through) and rounding. The asynchronous three-state output enable control simplifies interfacing to a bus.

Data can be input into the LF2242 at a rate of up to 40 million samples per second. Within the 40 MHz I/O limit, the output sample rate can be one-half, equal to, or two times the input sample rate. Once data is clocked in, the 55-value output response begins after 7 clock cycles and ends after 61 clock cycles. The pipeline latency from the input of an impulse response to its corresponding output peak is 34 clock cycles.

The output data may be in either two's complement format or inverted offset binary format. To avoid truncation errors, the output data is always internally rounded before it is latched into the output register. Rounding is user-selectable, and the output data can be rounded from 16 bit values down to 9 bit values.

DC gain of the LF2242 is 1.0015 (0.0126 dB) in pass-through and decimate modes and 0.5007 (–3.004 dB) in interpolate mode. Passband ripple does not exceed ±0.02 dB from 0 to $0.22f_S$ with stopband attenuation greater than 59.4 dB from $0.28f_S$ to $0.5f_S$ (Nyquist frequency). The response of the filter is –6 dB at $0.25f_S$. Full compliance with CCIR Recommendation 601 (–12 dB at $0.25f_S$) can be achieved by cascading two devices serially.

LF2242 Block Diagram

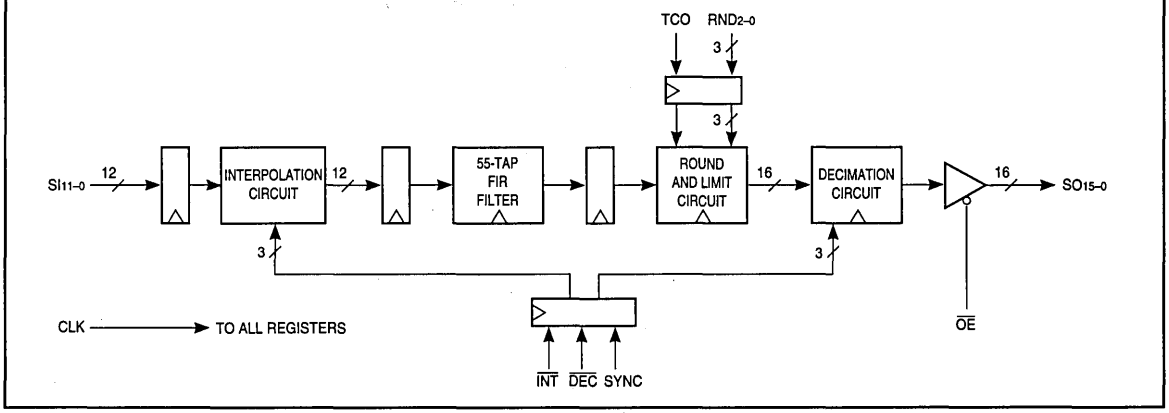
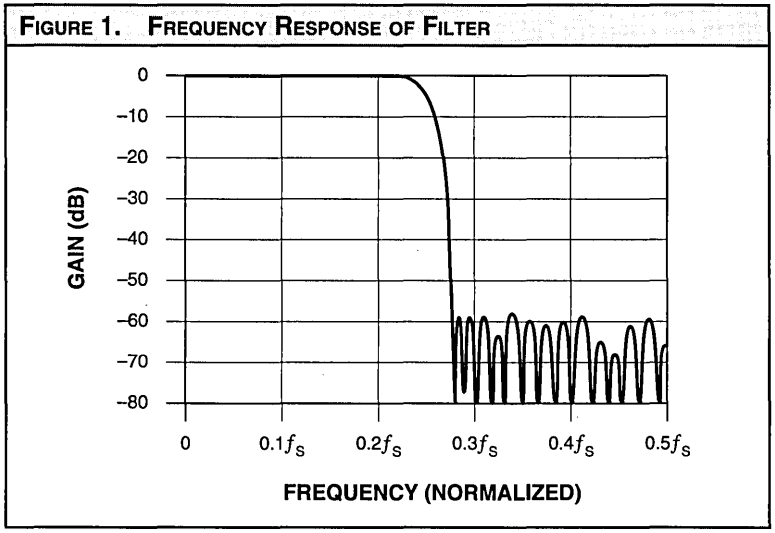


FIGURE 1. FREQUENCY RESPONSE OF FILTER



SIGNAL DEFINITIONS

Power

Vcc and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all registers. All timing specifications are referenced to the rising edge of CLK.

SYNC — Synchronization Control

Incoming data is synchronized by holding SYNC HIGH on CLKN, and then by bringing SYNC LOW on CLKN+1 with the first word of input data. SYNC is held LOW until resynchronization is desired, or it can be toggled at half the clock rate. For interpolation ($\overline{INT}$ = LOW), input data should be presented at the first rising edge of CLK for which SYNC is LOW and then at every alternate rising edge of CLK thereafter. SYNC is inactive if $\overline{DEC}$ and $\overline{INT}$ are equal (pass-through mode).

Inputs

SI11-0 — Data Input

12-bit two's complement data input port. Data is latched into the register on the rising edge of CLK. The LSB is SI0 (Figure 2).

Outputs

SO15-0 Data Output

The current 16-bit result is available on the SO15-0 outputs. The LF2242's limiter ensures that a valid full-scale (7FFF positive or 8000 negative) output will be generated in the event of an internal overflow. The LSB is SO0 (Figure 2).

Controls

$\overline{INT}$ — Interpolation Control

When $\overline{INT}$ is LOW and $\overline{DEC}$ is HIGH (Table 1), the device internally forces every other incoming data sample to zero. This effectively halves the input data rate and the output amplitude.

$\overline{DEC}$ — Decimation Control

When $\overline{DEC}$ is LOW and $\overline{INT}$ is HIGH (Table 1), the output register is strobed on every other rising edge of CLK (driven at half the clock rate), decimating the output data stream.

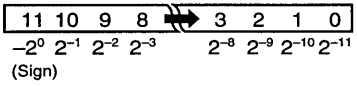
TABLE 1. MODE SELECTION

$\overline{INT}$	$\overline{DEC}$	MODE
0	0	Pass-through*
0	1	Interpolate
1	0	Decimate
1	1	Pass-through*

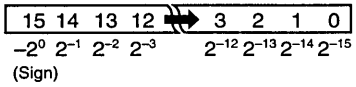
*Input and output registers run at full clock rate

FIGURE 2. INPUT AND OUTPUT FORMATS

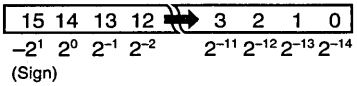
Two's Complement Input Format



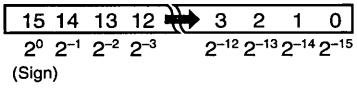
Two's Complement Output Format (TCO = 1, Non-interpolate)



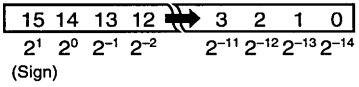
Two's Complement Output Format (TCO = 1, Interpolate)



Inverted Offset Binary Output Format (TCO = 0, Non-interpolate)



Inverted Offset Binary Output Format (TCO = 0, Interpolate)



RND2-0 — Rounding Control

The rounding control inputs set the position of the effective LSB of the output data by adding a rounding bit to the internal bit position that is one below that specified by RND2-0. All bits below the effective LSB position are subsequently zeroed (Table 2).

TCO — Two's Complement Format Control

The TCO input determines the format of the output data. When TCO is HIGH, the output data is presented in two's complement format. When TCO is LOW, the data is in inverted offset binary format (all output bits are inverted except the MSB — the MSB is unchanged).

$\overline{OE}$ — Output Enable

When the $\overline{OE}$ signal is LOW, the current data in the output register is available on the SO15-0 pins. When $\overline{OE}$ is HIGH, the outputs are in a high-impedance state.

TABLE 2. ROUNDING FORMAT

RND2-0	SO15	SO14	SO13	SO12	•••	SO8	SO7	SO6	SO5	SO4	SO3	SO2	SO1	SO0
000	X	X	X	X	•••	X	X	X	X	X	X	X	X	R
001	X	X	X	X	•••	X	X	X	X	X	X	X	R	0
010	X	X	X	X	•••	X	X	X	X	X	X	R	0	0
011	X	X	X	X	•••	X	X	X	X	X	R	0	0	0
100	X	X	X	X	•••	X	X	X	X	R	0	0	0	0
101	X	X	X	X	•••	X	X	X	R	0	0	0	0	0
110	X	X	X	X	•••	X	X	R	0	0	0	0	0	0
111	X	X	X	X	•••	X	R	0	0	0	0	0	0	0

'R' indicates the half-LSB rounded bit (effective LSB position)

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

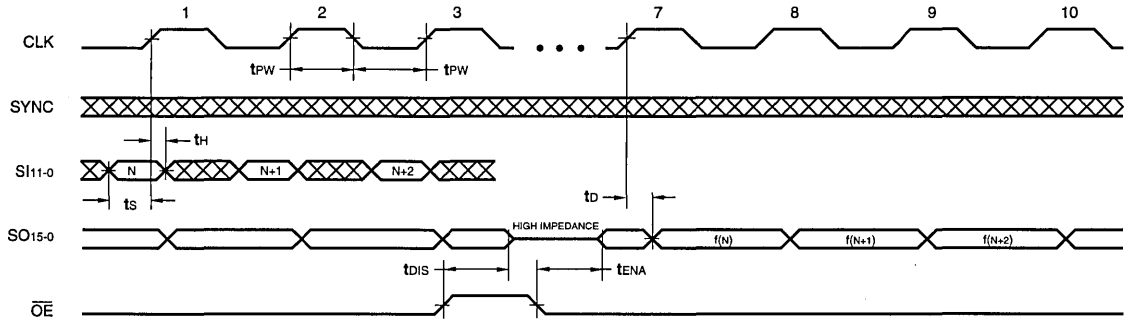
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	(Note 12)			±40	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			140	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			10	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

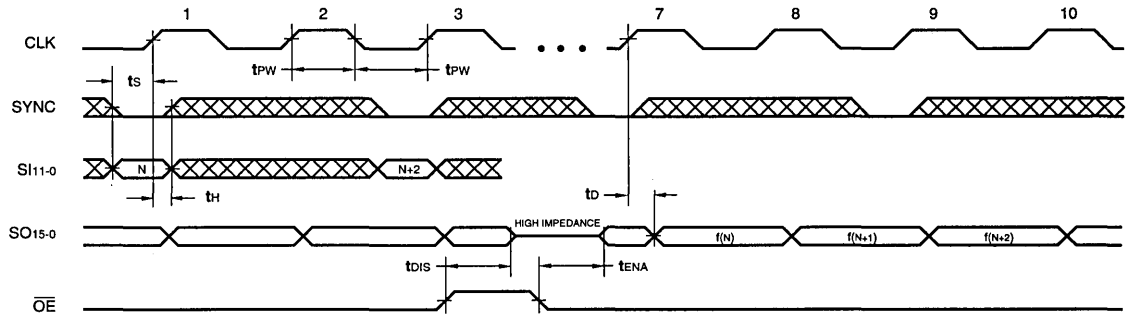
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LF2242– 33 Min	33 Max	25 Min	25 Max
t_{CYC}	Cycle Time	33		25	
t_{PW}	Clock Pulse Width	10		10	
t_S	Input Setup Time	10		8	
t_H	Input Hold Time	0		0	
t_D	Output Delay		20		16
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15

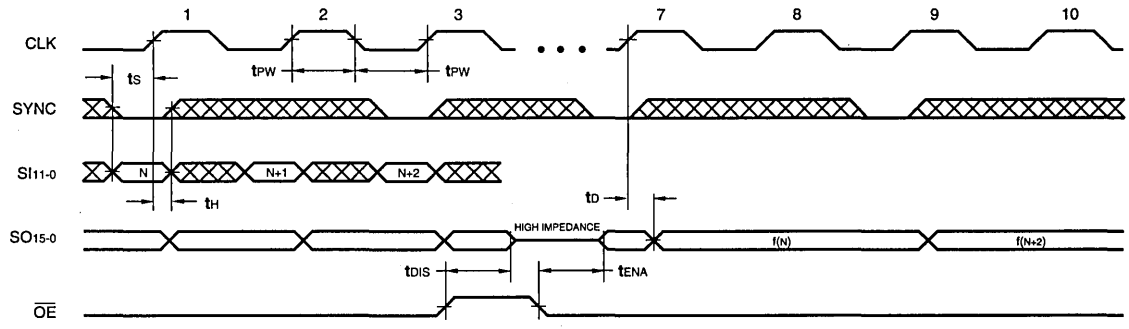
SWITCHING WAVEFORMS: PASS-THROUGH MODE ($\overline{INT}$ = $\overline{DEC}$)



SWITCHING WAVEFORMS: INTERPOLATE MODE ($\overline{INT}$ = 0, $\overline{DEC}$ = 1)



SWITCHING WAVEFORMS: DECIMATE MODE ($\overline{INT}$ = 1, $\overline{DEC}$ = 0)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

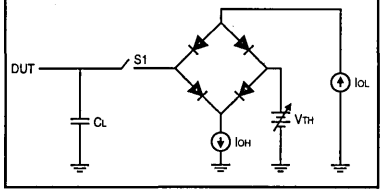
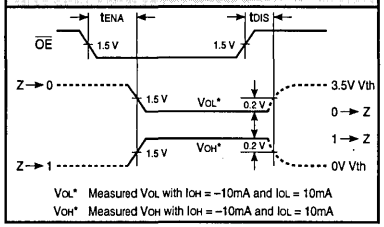
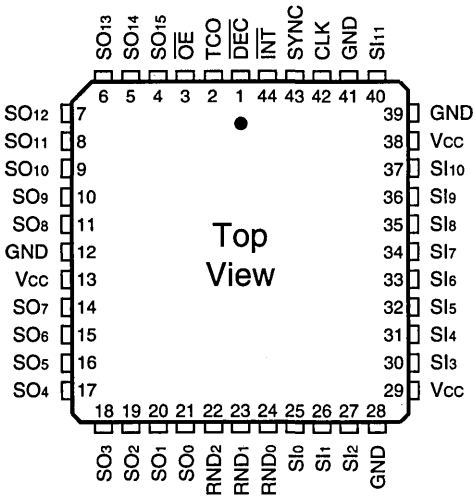


FIGURE B. THRESHOLD LEVELS

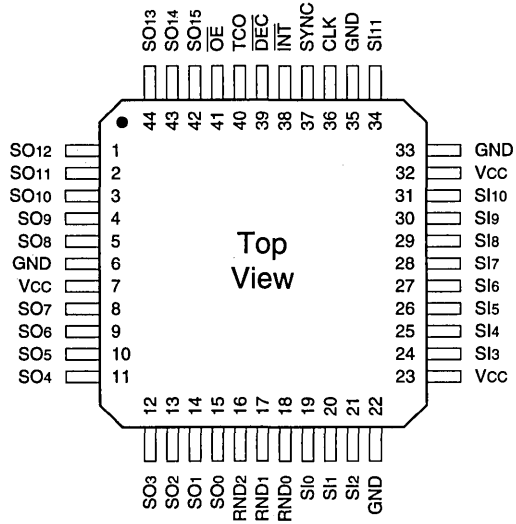


ORDERING INFORMATION

44-pin



44-pin



Speed	Plastic J-Lead Chip Carrier (J1)	Plastic Quad Flatpack (Q4)
	0°C to +70°C — COMMERCIAL SCREENING	
33 ns	LF2242JC33	LF2242QC33
25 ns	LF2242JC25	LF2242QC25

FEATURES

- 66 MHz Data and Coefficient Input and Computation Rate
- Four 11 x 10-bit Multipliers with Individual Data and Coefficient Inputs and a 25-bit Accumulator
- User-Selectable Fractional or Integer Two's Complement Data Formats
- Fully Registered, Pipelined Architecture
- Input and Output Data Registers, with User-Configurable Enables
- Three-State Outputs
- Fully TTL Compatible
- Ideally Suited for Image Processing and Filtering Applications
- Replaces TRW/Raytheon TMC2246
- Package Styles Available:
  - 120-pin Pin Grid Array
  - 120-pin Plastic Quad Flatpack

DESCRIPTION

The **LF2246** consists of an array of four 11 x 10-bit registered multipliers followed by a summer and a 25-bit accumulator. All multiplier inputs are user accessible and can be updated every clock cycle with either fractional or integer two's complement data. The pipelined architecture has fully registered input and output ports and an asynchronous three-state output enable control to simplify the design of complex systems. The pipeline latency for all inputs is five clock cycles.

Storage for mixing and filtering coefficients can be accomplished by holding the data or coefficient inputs over multiple clock cycles. A 25-bit accumulator path allows cumulative word growth which may be internally rounded to 16 bits. Output data is updated every clock cycle and may be held under user control. All inputs, outputs, and controls are registered on the rising edge of clock, except for $\overline{OEN}$. The LF2246 operates at a clock rate of 66 MHz over the full temperature and supply voltage ranges.

The LF2246 is applicable for performing pixel interpolation in image manipulation and filtering applications. The LF2246 can perform a bilinear interpolation of an image (4-pixel kernels) at real-time video rates when used with an image resampling sequencer. Larger kernels or more complex functions can be realized by utilizing multiple devices.

Unrestricted access to all data and coefficient input ports provides the LF2246 with considerable flexibility in applications such as digital filters, adaptive FIR filters, mixers, and other similar systems requiring high-speed processing.

2

LF2246 BLOCK DIAGRAM

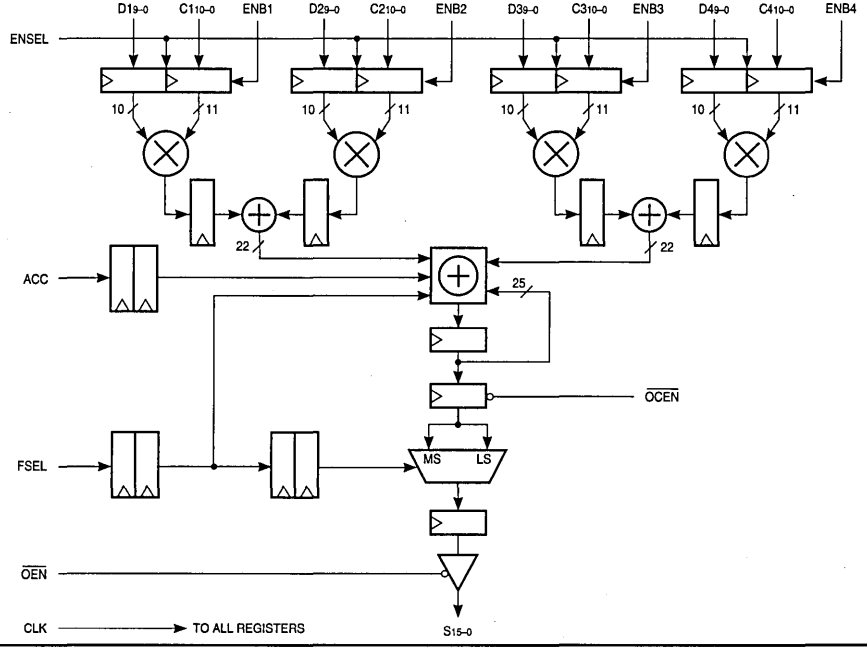


FIGURE 1A. INPUT FORMATS

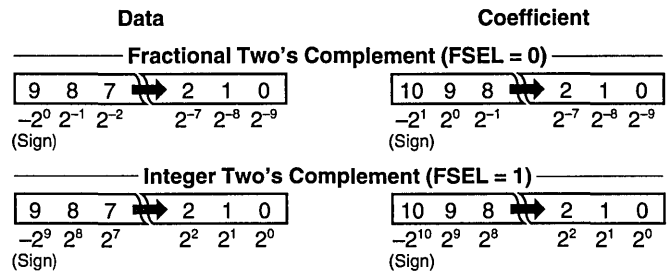
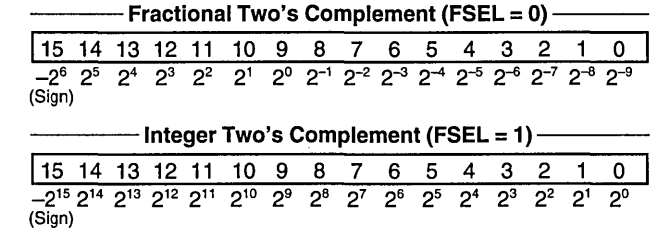


FIGURE 1B. OUTPUT FORMATS



SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

D19-0–D49-0 — Data Input

D1–D4 are 10-bit data input registers. The LSB is DN0 (Figure 1a).

C110-0–C410-0 — Coefficient Input

C1–C4 are 11-bit coefficient input registers. The LSB is CN0 (Figure 1a).

Outputs

S15-0 — Data Output

The current 16-bit result is available on the S15-0 outputs (Figure 1b).

Controls

ENB1–ENB4 — Input Enable

The ENBN (N = 1, 2, 3, or 4) input allows either or both the DN and CN registers to be updated on each clock cycle. When ENBN is LOW, registers DN and CN are both strobed by the next rising edge of CLK. When ENBN is HIGH and ENSEL is LOW, register DN is strobed while register CN is held. If both ENBN and ENSEL are HIGH, register DN is held, and register CN is strobed (Table 1).

ENSEL — Enable Select

The ENSEL input in conjunction with the individual input enables ENB1–ENB4 determines whether the data or the coefficient input registers will be held on the next rising edge of CLK (Table 1).

$\overline{OEN}$ — Output Enable

When the $\overline{OEN}$ signal is LOW, the current data in the output register is available on the S15-0 pins. When $\overline{OEN}$ is HIGH, the outputs are in a high-impedance state.

TABLE 1. INPUT REGISTER CONTROL

ENB1-4	ENSEL	INPUT REGISTER HELD
1	1	Data 'N'
1	0	Coefficient 'N'
0	X	None

X = "Don't Care"
'N' = 1, 2, 3, or 4

$\overline{OCEN}$ — Clock Enable

When $\overline{OCEN}$ is LOW, data in the pre-mux register (accumulator output) is loaded into the output register on the next rising edge of CLK. When $\overline{OCEN}$ is HIGH, data in the pre-mux register is held preventing the output register's contents from changing (if FSEL does not change). Accumulation continues internally as long as ACC is HIGH, despite the state of $\overline{OCEN}$.

FSEL — Format Select

When the FSEL input is LOW, the data input during the current clock cycle is assumed to be in fractional two's complement format, and the upper 16 bits of the accumulator are presented at the output. Rounding of the accumulator result to 16 bits is performed if the accumulator control input ACC is LOW. When FSEL is HIGH, the data input is assumed to be in integer two's complement format, and the lower 16 bits of the accumulator are presented at the output. No rounding is performed when FSEL is HIGH.

ACC — Accumulator Control

The ACC input determines whether internal accumulation is performed on the data input during the current clock cycle. If ACC is LOW, no accumulation is performed, the prior accumulated sum is cleared, and the current sum of products is output. If FSEL is also LOW, one-half LSB rounding to 16 bits is performed on the result. This allows summations without propagating roundoff errors. When ACC is HIGH, the emerging product is added to the sum of the previous products, without additional rounding.

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	(Note 12)			±40	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			100	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			6	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

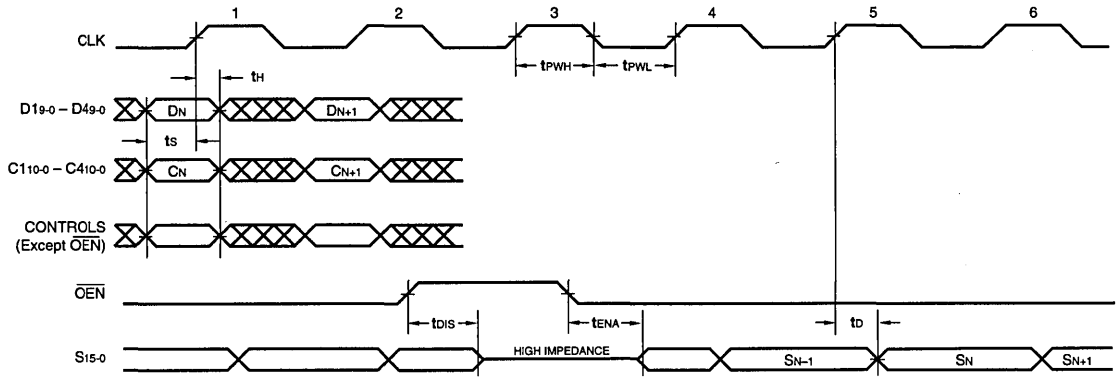
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF2246–					
		33		25		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	33		25		15	
t_{PWL}	Clock Pulse Width Low	15		10		7	
t_{PWH}	Clock Pulse Width High	10		10		7	
t_S	Input Setup Time	10		8		5	
t_H	Input Hold Time	0		0		0	
t_D	Output Delay		15		13		11
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		15		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF2246–			
		33		25	
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	33		25	
t_{PWL}	Clock Pulse Width Low	15		10	
t_{PWH}	Clock Pulse Width High	10		10	
t_S	Input Setup Time	10		8	
t_H	Input Hold Time	0		0	
t_D	Output Delay		15		13
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 30 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

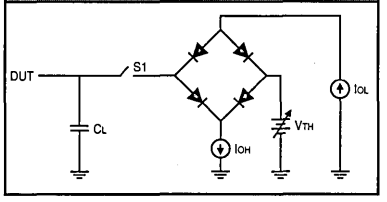
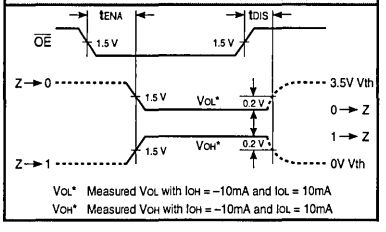
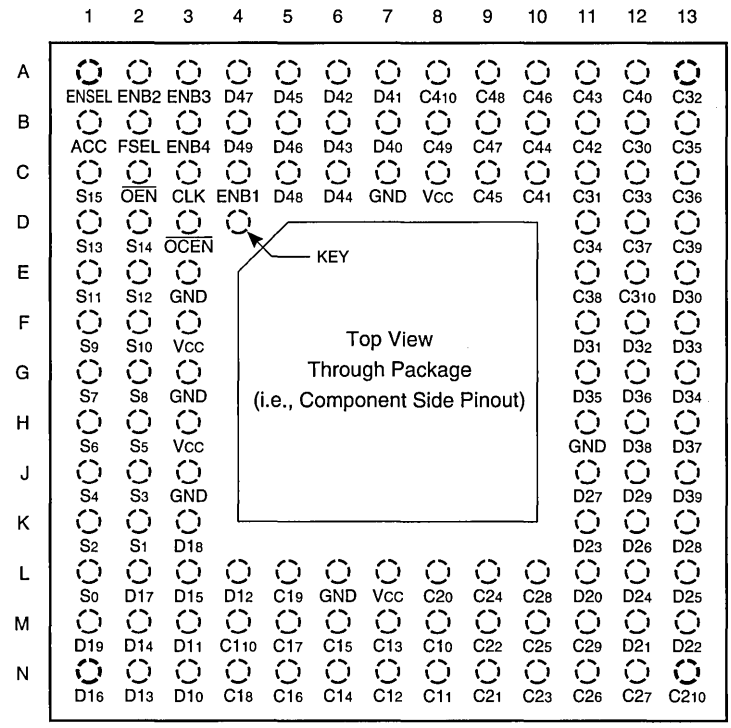


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

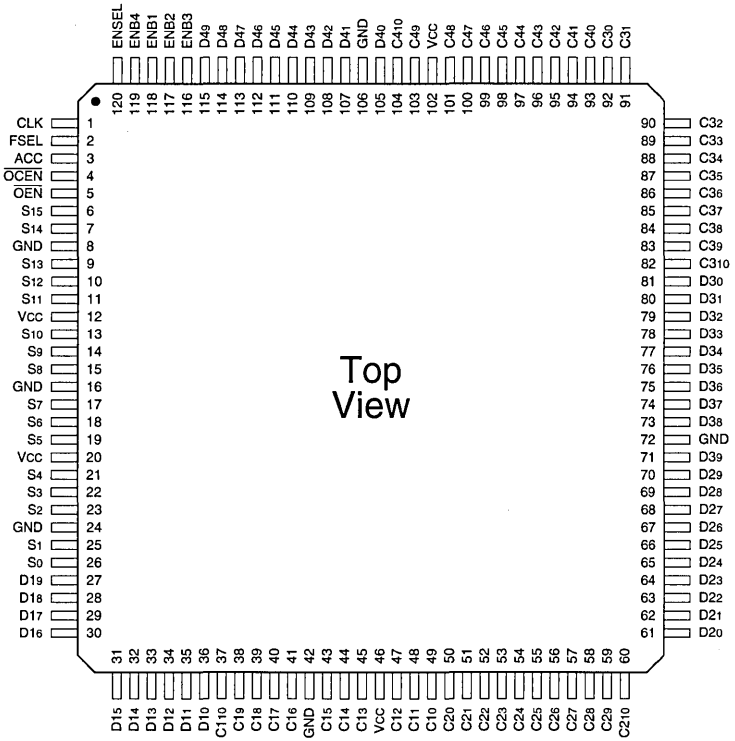
120-pin



Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C — COMMERCIAL SCREENING
33 ns	LF2246GC33
25 ns	LF2246GC25
15 ns	LF2246GC15
	–55°C to +125°C — COMMERCIAL SCREENING
33 ns	LF2246GM33
25 ns	LF2246GM25
	–55°C to +125°C — MIL-STD-883 COMPLIANT
33 ns	LF2246GMB33
25 ns	LF2246GMB25

ORDERING INFORMATION

120-pin



Speed	Plastic Quad Flatpack (Q1)
	0°C to +70°C — COMMERCIAL SCREENING
33 ns	LF2246QC33
25 ns	LF2246QC25
15 ns	LF2246QC15

2

FEATURES

- 66 MHz Data Input and Computation Rate
- Four 11 x 10-bit Multipliers with Individual Data and Coefficient Inputs and a 25-bit Accumulator
- Four 32 x 11-bit Serially Loadable Coefficient Registers
- Fractional or Integer Two's Complement Operands
- Package Styles Available:
  - 84-pin Plastic LCC, J-Lead
  - 100-pin Plastic Quad Flatpack
  - 84-pin Pin Grid Array

DESCRIPTION

The **LF2247** consists of an array of four 11 x 10-bit registered multipliers followed by a summer and a 25-bit accumulator. The LF2247 provides a coefficient register file containing four 32 x 11-bit registers which are capable of storing 32 different sets of filter coefficients for the multiplier array. All multiplier data inputs are user accessible and can be updated every clock cycle with either fractional or integer two's complement data. The pipelined architecture has fully registered input and output ports and an asynchronous three-state output enable control to simplify the design of complex systems. The pipeline latency for all inputs is five clock cycles.

A 25-bit accumulator path allows cumulative word growth which may be internally rounded to 16 bits. Output data is updated every clock cycle and may be held under user control. The data inputs/outputs and control inputs are registered on the rising edge of CLK. The Serial Data In signal, SDIN, is registered on the

2

LF2247 Block Diagram

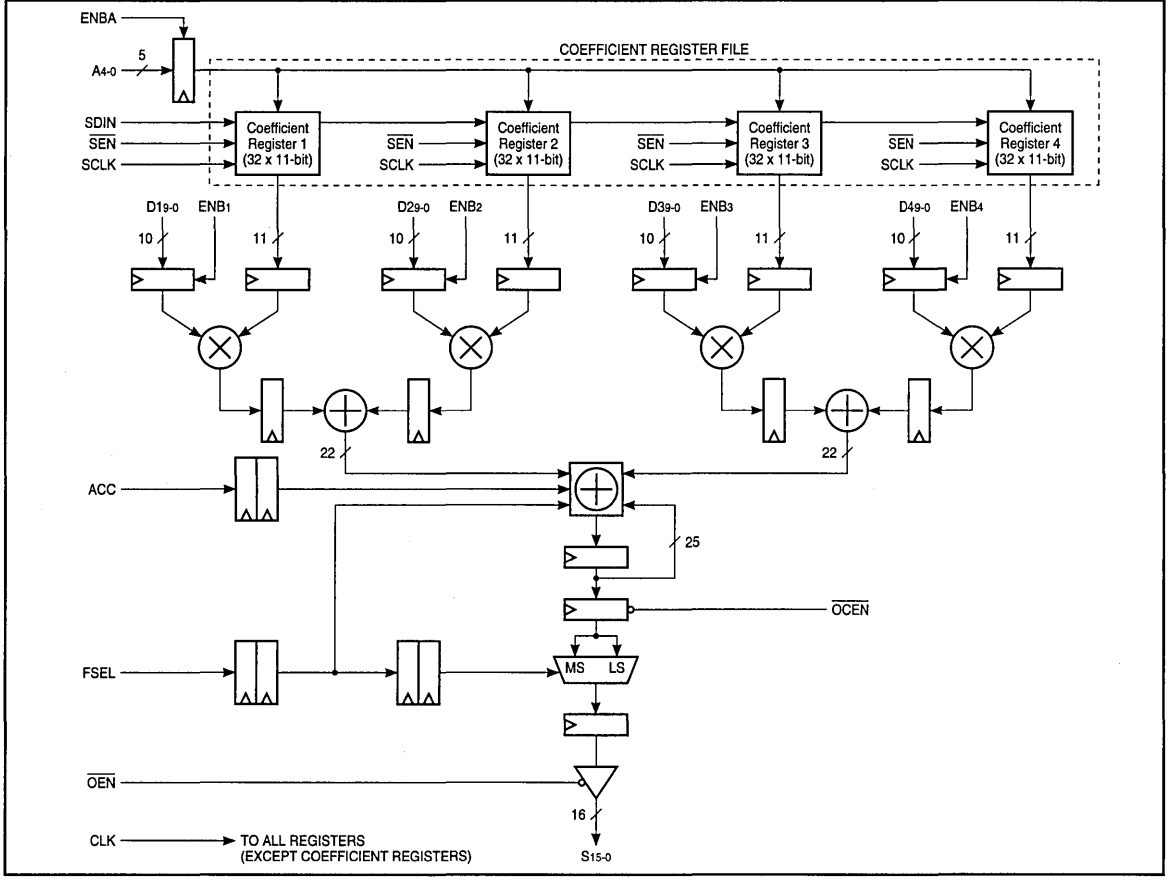


FIGURE 1A. INPUT FORMATS

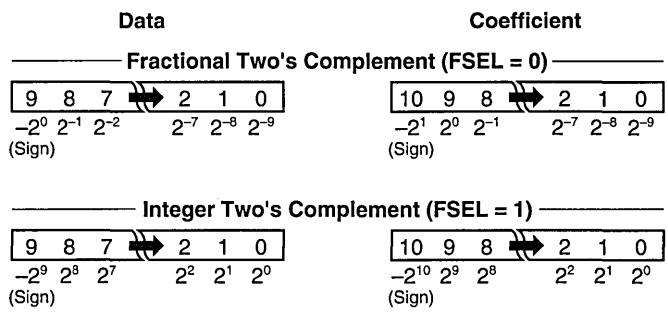
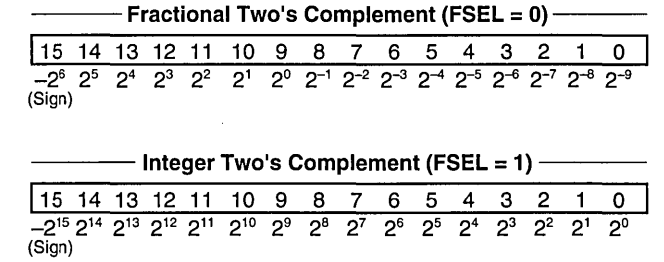


FIGURE 1B. OUTPUT FORMATS



rising edge of SCLK. The LF2247 operates at a clock rate of 66 MHz over the full temperature and supply voltage ranges.

The LF2247 is applicable for performing pixel interpolation in image manipulation and filtering applications. The LF2247 can perform a bilinear interpolation of an image (4-pixel kernels) at real-time video rates when used with an image resampling sequencer. Larger kernels or more complex functions can be realized by utilizing multiple devices.

Unrestricted access to all data ports and an addressable coefficient register file provides the LF2247 with considerable flexibility in applications such as digital filters, adaptive FIR filters, mixers, and other similar systems requiring high-speed processing.

SIGNAL DEFINITIONS

Power

V_{CC} and GND

+5 V power supply. All pins must be connected.

Clocks

CLK — Master Clock

The rising edge of CLK strobes all enabled registers except for the coefficient registers.

SCLK — Serial Clock

The rising edge of SCLK shifts data into and through the coefficient register file when it is enabled for serial data shifting.

Inputs

$D19\text{-}0$ – $D49\text{-}0$ — Data Input

D1–D4 are the 10-bit registered data input ports. Data is latched on the rising edge of CLK.

$A4\text{-}0$ — Row Address

$A4\text{-}0$ determines which row of data in the coefficient register file is used to feed data to the multiplier array. $A4\text{-}0$ is latched on the rising edge of CLK. When a new row address is loaded into the row address register, data from the register file will be latched into the multiplier input registers on the next rising edge of CLK.

SDIN — Serial Data Input

SDIN is used to serially load data into the coefficient registers. Data present on SDIN is shifted into the coefficient register file on the rising edge of SCLK when $\overline{SEN}$ is LOW. The 11-bit coefficients are loaded into the coefficient register file in 16-bit words as shown in Figure 2. The five most significant bits of the first 16-bit word determine which row the data is written to in the coefficient registers. Note that the five most significant bits of the remaining three 16-bit words are ignored. After all four 16-bit words are shifted into the register file, the lower eleven bits of each word (the coefficient data) are stored into the coefficient registers.

Outputs

$S15\text{-}0$ — Data Output

$S15\text{-}0$ is the 16-bit registered data output port.

Controls

$ENB1$–$ENB4$ — Data Input Enables

The $ENBN$ ($N = 1, 2, 3$, or 4) inputs allow the DN registers to be updated on each clock cycle. When $ENBN$ is LOW, data on $DN9\text{-}0$ is latched into

the DN register on the rising edge of CLK. When ENBN is HIGH, data on DN9-0 is not latched into the DN register and the register contents will not be changed.

ENBA — Row Address Input Enable

The ENBA input allows the row address register to be updated on each clock cycle. When ENBA is LOW, data on A4-0 is latched into the row address register on the rising edge of CLK. When ENBA is HIGH, data on A4-0 is not latched into the row address register and the register contents will not be changed.

$\overline{OEN}$ — Output Enable

When $\overline{OEN}$ is LOW, S15-0 is enabled for output. When $\overline{OEN}$ is HIGH, S15-0 is placed in a high-impedance state.

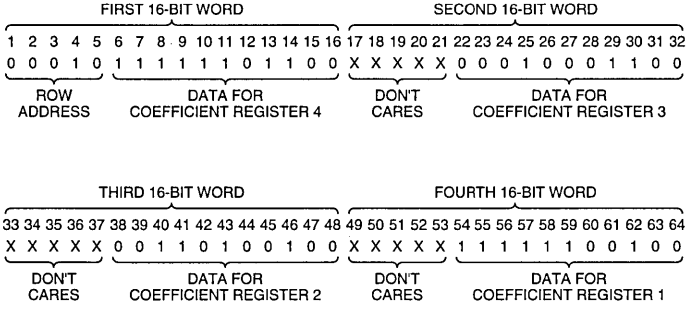
$\overline{OCEN}$ — Clock Enable

When $\overline{OCEN}$ is LOW, data in the pre-mux register (accumulator output) is loaded into the output register on the next rising edge of CLK. When $\overline{OCEN}$ is HIGH, data in the pre-mux register is held preventing the output register's contents from changing (if FSEL does not change). Accumulation continues internally as long as ACC is HIGH, despite the state of $\overline{OCEN}$.

FSEL — Format Select

When FSEL is LOW, the data input during the current clock cycle is assumed to be in fractional two's complement format, and the upper 16 bits of the accumulator are presented at the output. Rounding of the accumulator result to 16 bits is performed if the accumulator control input ACC is LOW. When FSEL is HIGH, the data input is assumed to be in integer two's complement format, and the lower 16 bits of the accumulator are presented at the output. No rounding is performed when FSEL is HIGH.

FIGURE 2. SERIAL DATA FORMAT



SHOWN IS SERIAL DATA STREAM TO LOAD ROW ADDRESS 2 WITH:
COEFFICIENT REGISTER 1 = 7E4
COEFFICIENT REGISTER 2 = 1A4
COEFFICIENT REGISTER 3 = 08C
COEFFICIENT REGISTER 4 = 7EC

ACC — Accumulator Control

The ACC input determines whether internal accumulation is performed on the data input during the current clock cycle. If ACC is LOW, no accumulation is performed, the prior accumulated sum is cleared, and the current sum of products is output. If FSEL is also LOW, one-half LSB rounding to 16 bits is performed on the result. When ACC is HIGH, the emerging product is added to the sum of the previous products, without additional rounding.

$\overline{SEN}$ — Serial Input Enable

The $\overline{SEN}$ input enables the shifting of serial data through the registers in the coefficient register file. When $\overline{SEN}$ is LOW, serial data on SDIN is shifted into the coefficient register file on the rising edge of SCLK. $\overline{SEN}$ must remain LOW until all four coefficients have been clocked in. $\overline{SEN}$ does not need to be pulsed between consecutive data sets. It can remain LOW while the entire register file is loaded by a constant bit stream. When $\overline{SEN}$ is HIGH, data can not be shifted into the register file and the register file's contents will not be changed. When enabling the coefficient register file for serial data input, the LF2247 requires a HIGH to LOW transition of $\overline{SEN}$ in order to function properly. Therefore, $\overline{SEN}$ needs to be set HIGH immediately after power up to ensure proper operation of the serial input circuitry.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±40	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			100	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			6.0	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

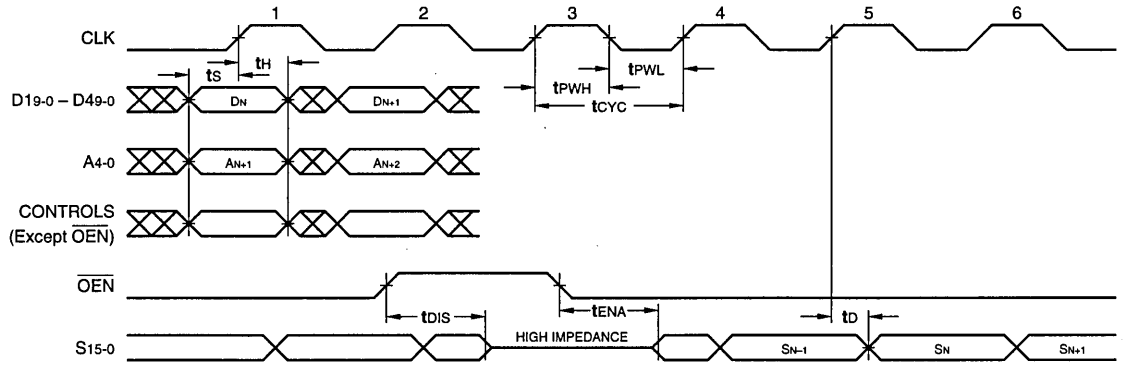
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF2247–					
		33		25		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
tCYC	Cycle Time	33		25		15	
tPWL	Clock Pulse Width Low	15		10		7	
tPWH	Clock Pulse Width High	10		10		7	
tS	Input Setup Time	10		8		5	
tH	Input Hold Time	0		0		0	
tD	Output Delay		15		13		11
tDIS	Three-State Output Disable Delay (Note 11)		15		15		15
tENA	Three-State Output Enable Delay (Note 11)		15		15		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF2247–			
		33		25	
Symbol	Parameter	Min	Max	Min	Max
tCYC	Cycle Time	33		25	
tPWL	Clock Pulse Width Low	15		10	
tPWH	Clock Pulse Width High	10		10	
tS	Input Setup Time	10		8	
tH	Input Hold Time	0		0	
tD	Output Delay		15		13
tDIS	Three-State Output Disable Delay (Note 11)		15		15
tENA	Three-State Output Enable Delay (Note 11)		15		15

SWITCHING WAVEFORMS: DATA I/O



SWITCHING CHARACTERISTICS

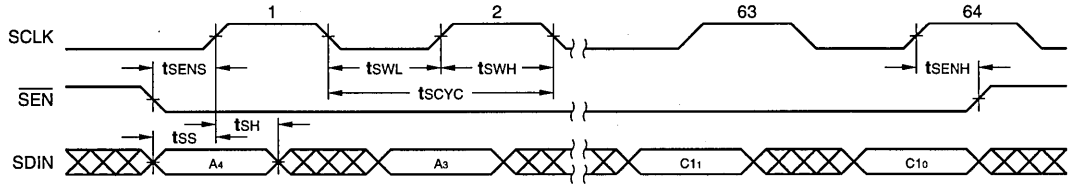
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF2247–					
		33		25		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{SCYC}	Serial Interface Cycle Time	62		62		62	
t_{SWL}	Serial Clock Pulse Width Low	30		30		30	
t_{SWH}	Serial Clock Pulse Width High	30		30		30	
t_{SENS}	Serial Enable Setup Time	20		20		20	
t_{SENH}	Serial Enable Hold Time	0		0		0	
t_{SS}	Serial Data Input Setup Time	20		20		20	
t_{SH}	Serial Data Input Hold Time	0		0		0	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF2247–			
		33		25	
Symbol	Parameter	Min	Max	Min	Max
t_{SCYC}	Serial Interface Cycle Time	62		62	
t_{SWL}	Serial Clock Pulse Width Low	30		30	
t_{SWH}	Serial Clock Pulse Width High	30		30	
t_{SENS}	Serial Enable Setup Time	20		20	
t_{SENH}	Serial Enable Hold Time	0		0	
t_{SS}	Serial Data Input Setup Time	20		20	
t_{SH}	Serial Data Input Hold Time	0		0	

SWITCHING WAVEFORMS: SERIAL DATA INPUT



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 30 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

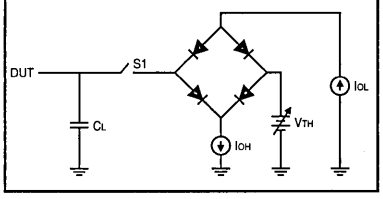
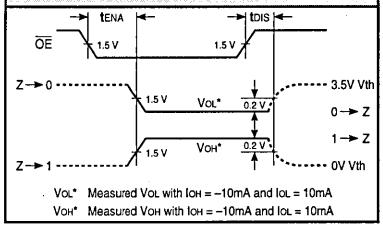


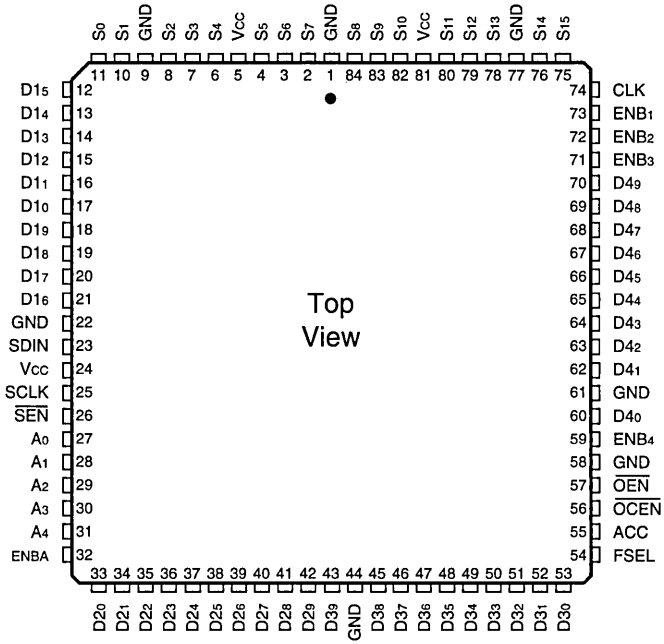
FIGURE B. THRESHOLD LEVELS



2

ORDERING INFORMATION

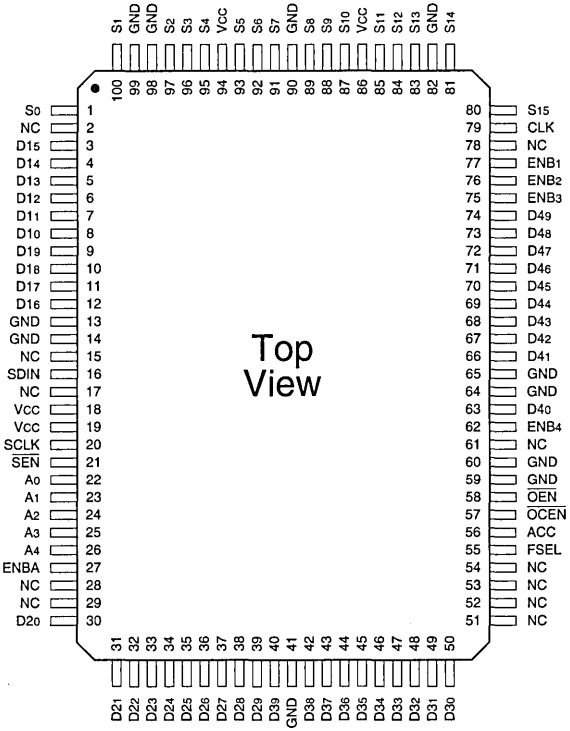
84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — COMMERCIAL SCREENING
33 ns	LF2247JC33
25 ns	LF2247JC25
15 ns	LF2247JC15

ORDERING INFORMATION

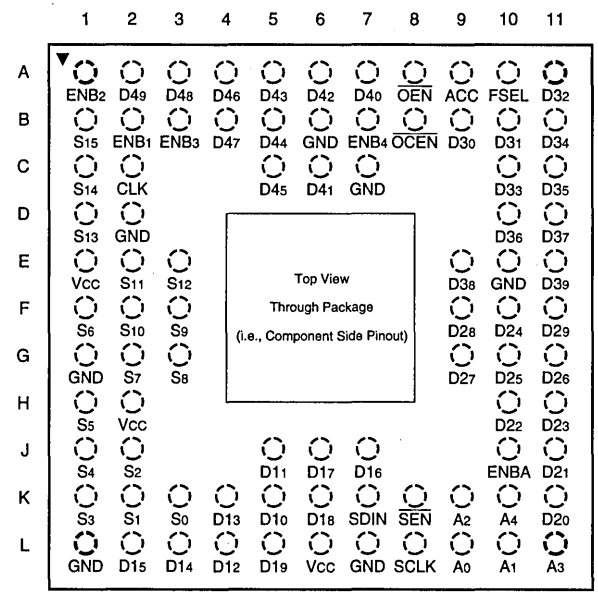
100-pin



Speed	Plastic Quad Flatpack (Q2)
	0°C to +70°C — COMMERCIAL SCREENING
33 ns	LF2247QC33
25 ns	LF2247QC25
15 ns	LF2247QC15

ORDERING INFORMATION

84-pin



Speed	Ceramic Pin Grid Array (G3)
	0°C to +70°C — COMMERCIAL SCREENING
33 ns	LF2247GC33
25 ns	LF2247GC25
15 ns	LF2247GC15
	–55°C to +125°C — COMMERCIAL SCREENING
33 ns	LF2247GM33
25 ns	LF2247GM25
	–55°C to +125°C — MIL-STD-883 COMPLIANT
33 ns	LF2247GMB33
25 ns	LF2247GMB25

FEATURES

- 40 MHz Data and Computation Rate
- Two 12 x 12-bit Multipliers with Individual Data Inputs
- Separate 16-bit Input Port for Cascading Devices
- Independent, User-Selectable 1–16 Clock Pipeline Delay for Each Data Input
- User-Selectable Rounding of Products
- Fully Registered, Pipelined Architecture
- Three-State Outputs
- Fully TTL Compatible
- Replaces TRW/Raytheon TMC2249
- Package Styles Available:
  - 120-pin Ceramic PGA
  - 120-pin Plastic Quad Flatpack

DESCRIPTION

The **LF2249** is a high-speed digital mixer comprised of two 12-bit multipliers and a 24-bit accumulator. All multiplier inputs are user accessible, and each can be updated on every clock cycle. The LF2249 utilizes a pipelined architecture with fully registered inputs and outputs and an asynchronous three-state output enable control for optimum flexibility.

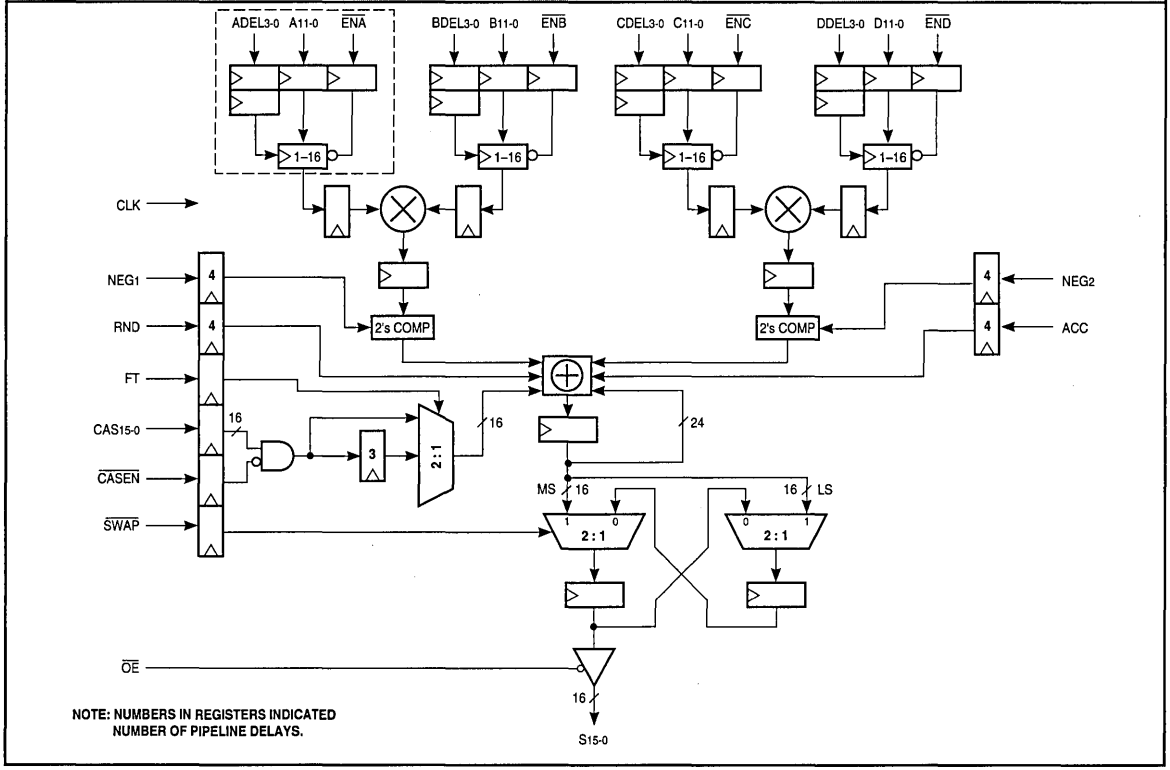
Independent input register clock enables allow the user to hold the data inputs over multiple clock cycles. Each multiplier input also includes a user-selectable 1-16 clock pipeline delay. The output of each multiplier can be independently negated under user control for subtraction of products. The sum of the products can also be internally rounded to 16 bits during the accumulation process.

A separate 16-bit input port connected to the accumulator is included to allow cascading of multiple LF2249s. Access to all 24 bits of the accumulator is gained by switching between upper or lower 16-bit words. The accumulated output data is updated on every clock cycle.

All inputs and outputs of the LF2249 are registered on the rising edge of clock, except for $\overline{OE}$. Internal pipeline registers for all data and control inputs are provided to maintain

2

LF2249 BLOCK DIAGRAM



synchronous operation between the incoming data and all available control functions. The LF2249 operates at a clock rate of 40 MHz over the full commercial temperature and supply voltage ranges.

Because of its flexibility, the LF2249 is ideally suited for applications such as image switching and mixing, digital quadrature mixing and modulating, FIR filtering, and arithmetic function and waveform synthesis.

SIGNAL DEFINITIONS

Power

Vcc and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

A11-0–D11-0 — Data Inputs

A11-0–D11-0 are 12-bit data input registers. Data is latched into the input registers on the rising edge of CLK. The contents of the input registers are clocked into the top of the corresponding 16-stage pipeline delay (pushing the contents of the register stack down one register position) on the next clock cycle if the pipeline register stack is enabled. The LSBs are A0-D0 (Figure 1a).

CAS15-0 — Cascade Data Input

CAS15-0 is the 16-bit cascade data input port. Data is latched into the register on the rising edge of CLK. The LSB is CAS0 (Figure 1a).

DETAILED VIEW OF BLOCK DIAGRAM OUTLINED AREA

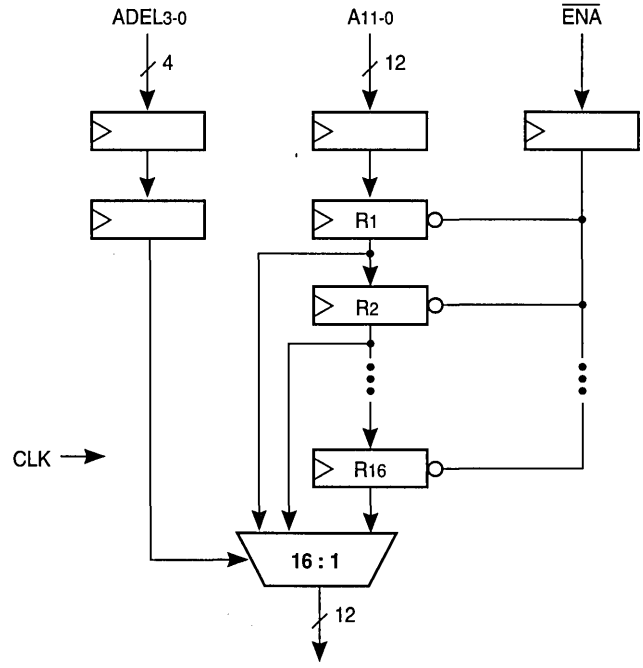


FIGURE 1A. INPUT FORMATS

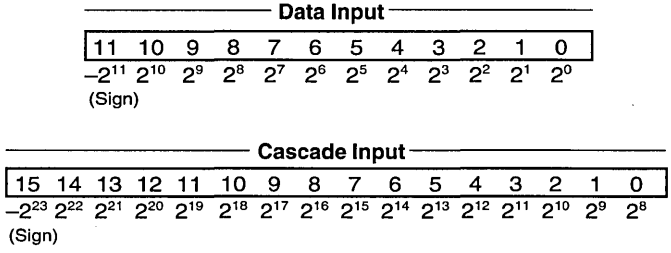
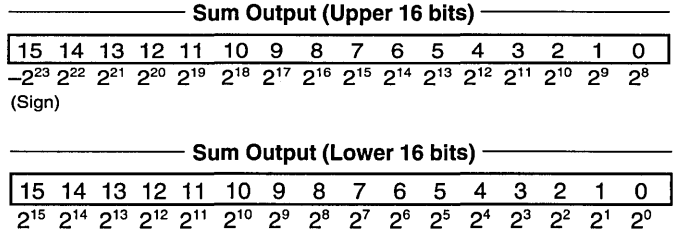


FIGURE 1B. OUTPUT FORMATS



Outputs

S15-0 — Data Output

The current 16-bit result is available on the S15-0 outputs. The output data may be either the upper or lower 16 bits of the accumulator output, depending on the state of $\overline{SWAP}$. The LSB is S0 (Figure 1b).

Controls

$\overline{ENA}$–$\overline{END}$ — Pipeline Register Enable

Input data in the N (N = A, B, C, or D) input register is latched into the corresponding pipeline register stack on each rising edge of CLK for which $\overline{EN_N}$ is LOW. Data already in the N register stack is pushed down one register position. When $\overline{EN_N}$ is HIGH, the data in the N pipeline register stack does not change, and the data in the N input register will not be stored in the register stack.

ADEL3-0–DDEL3-0 — Pipeline Delay Select

NDEL (N = A, B, C, or D) is the 4-bit registered pipeline delay select word. NDEL determines which stage of the N pipeline register stack is routed to the multiplier inputs. The minimum delay is one clock cycle (NDEL = 0000), and the maximum delay is 16 clock cycle (NDEL = 1111). Upon power up, the values of ADEL–DDEL and the contents of the pipeline register stacks are unknown and must be initialized by the user.

NEG1–NEG2 — Negate Control

The NEG1 and NEG2 controls determine whether a subtraction or accumulation of products is performed. When NEG1 is HIGH, the product *A x B* is negated, causing the product to be subtracted from the accumulator contents. Likewise, when NEG2 is HIGH, the product *C x D* is negated, causing the product to be subtracted as well. NEG1 and NEG2 determine the operation to be performed on the data input during the current clock cycle when ADEL–DDEL = 0000.

$\overline{CASEN}$ — Cascade Enable

When $\overline{CASEN}$ is LOW, data being input on the CAS15-0 inputs during that clock cycle will be registered and accumulated internally. When $\overline{CASEN}$ is HIGH, the CAS15-0 inputs are ignored.

FT — Feedthrough Control

When FT is LOW and ADEL–DDEL = 0000, data being input on the CAS15-0 inputs is delayed three clock cycles to align the data with the data being input on the A11-0–D11-0 inputs. When FT is HIGH, the cascade data being input is routed around the three delay registers to simplify the cascading of multiple devices.

ACC — Accumulator Control

The ACC input determines whether internal accumulation is performed on the data input during the current clock cycle. If ACC is LOW, no accumulation is performed, the prior accumulated sum is cleared, and the current sum of products is output. When ACC is HIGH, the emerging products are added to the sum of the previous products.

RND — Rounding Control

When RND is HIGH, the sum of the products of the data being input on the current clock cycle will be rounded to 16 bits. To avoid the accumulation of roundoff errors, rounding is only performed during the first cycle of each accumulation process.

$\overline{SWAP}$ — Output Select

The $\overline{SWAP}$ control allows the user to access all 24 bits of the accumulator output by switching between upper and lower 16-bit words. When $\overline{SWAP}$ is HIGH, the upper 16 bits of the accumulator are always output. When $\overline{SWAP}$ is LOW, the lower 16 bits of the accumulator are output on every other clock cycle. As long as $\overline{SWAP}$ remains LOW, new output data will not be clocked into the output registers.

$\overline{OE}$ — Output Enable

When the $\overline{OE}$ signal is LOW, the current data in the output registers is available on the S15-0 pins. When $\overline{OE}$ is HIGH, the outputs are in a high-impedance state.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	(Note 12)			±40	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			100	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			6	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

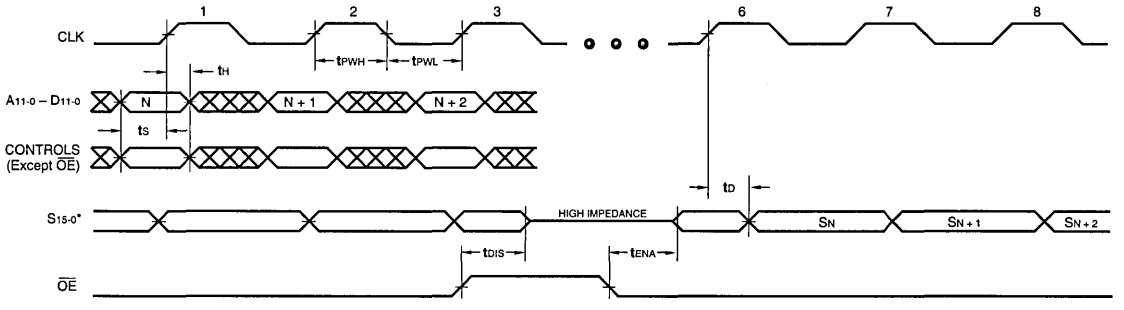
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF2249-					
		40		33		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
tCYC	Cycle Time	40		33		25	
tPWL	Clock Pulse Width, LOW	15		15		10	
tPWH	Clock Pulse Width, HIGH	10		10		10	
tS	Input Setup Time	8		8		7	
tH	Input Hold Time	0		0		0	
tD	Output Delay		17		15		14
tENA	Three-State Output Enable Delay (Note 11)		15		15		15
tDIS	Three-State Output Disable Delay (Note 11)		15		15		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF2249-			
		40		33	
Symbol	Parameter	Min	Max	Min	Max
tCYC	Cycle Time	40		33	
tPWL	Clock Pulse Width, LOW	15		15	
tPWH	Clock Pulse Width, HIGH	10		10	
tS	Input Setup Time	8		8	
tH	Input Hold Time	0		0	
tD	Output Delay		17		15
tENA	Three-State Output Enable Delay (Note 11)		15		15
tDIS	Three-State Output Disable Delay (Note 11)		15		15

SWITCHING WAVEFORMS



*Assumes ADEL–DDEL = 0000

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 25 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

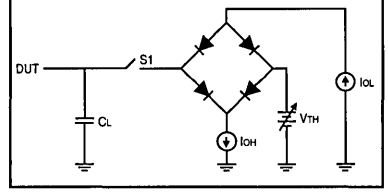
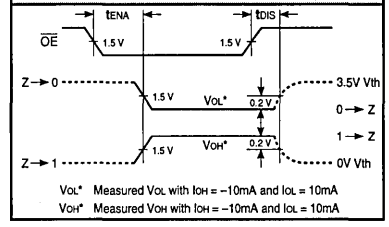
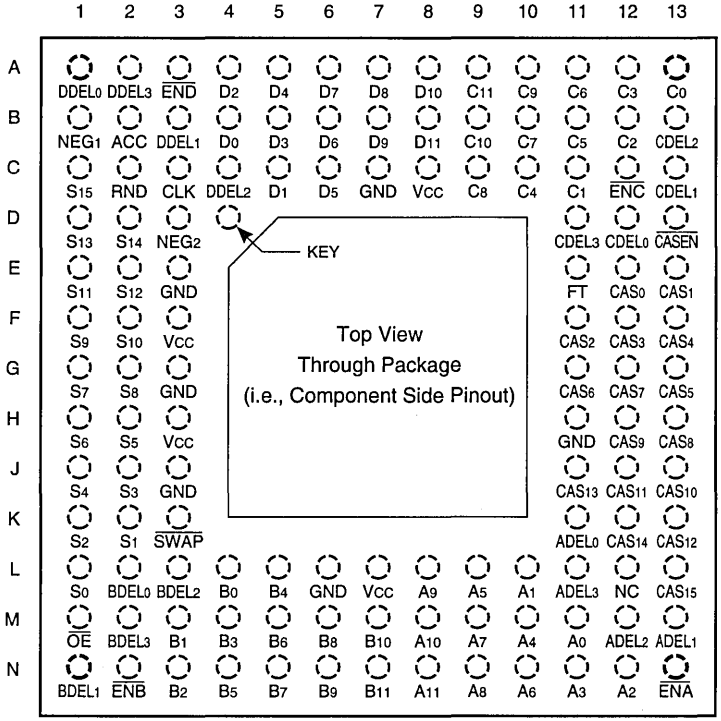


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

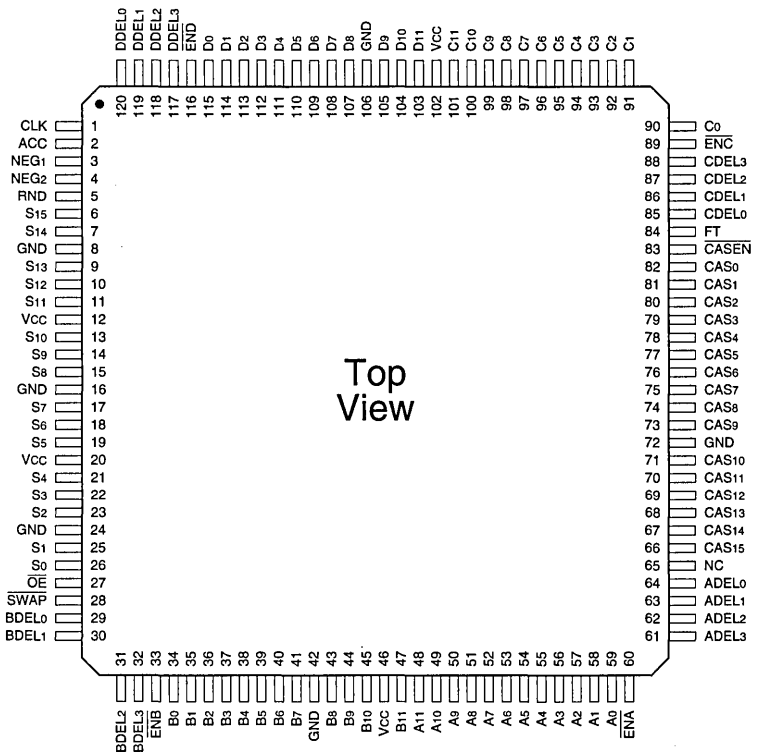
120-pin



Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C — Commercial Screening
40 ns	LF2249GC40
33 ns	LF2249GC33
25 ns	LF2249GC25
	–55°C to +125°C — Commercial Screening
40 ns	LF2249GM40
33 ns	LF2249GM33
	–55°C to +125°C — MIL-STD-883 Compliant
40 ns	LF2249GMB40
33 ns	LF2249GMB33

ORDERING INFORMATION

120-pin



Speed	Plastic Quad Flatpack (Q1)
	0°C to +70°C — COMMERCIAL SCREENING
40 ns	LF2249QC40
33 ns	LF2249QC33
25 ns	LF2249QC25

LF2250
12 x 10-bit Matrix Multiplier

FEATURES

- 50 MHz Data and Computation Rate
- Nine Multiplier Array with 12-bit Data and 10-bit Coefficient Inputs
- Separate 16-bit Cascade Input and Output Ports
- On-board Coefficient Storage
- Four User-Selectable Filtering and Transformation Functions:
  - 3 x 3 Matrix Multiplier
  - Cascadable 9-Tap FIR Filter
  - Cascadable 3 x 3 Convolver
  - Cascadable 4 x 2 Convolver
- Replaces TRW/Raytheon TMC2250
- DECC SMD No. 5962-93260
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 120-pin Pin Grid Array
  - 120-pin Plastic Quad Flatpack

DESCRIPTION

The **LF2250** is a high-speed matrix multiplier consisting of an array of nine 12 x 10-bit multipliers. Internal summing adders are also included to provide the configurations needed to implement matrix multiplications, cascadable FIR filters, and pixel convolvers.

The 3 x 3 matrix multiplier (triple dot product) configuration of the LF2250 allows users to easily perform three-dimensional perspective translations or video format conversions at real-time video rates. By using the LF2250 in this configuration, conversions can be made from the RGB (color component) format to the YIQ (quadrature encoded chrominance) or YUV (color difference) formats and vice versa (YIQ or YUV to RGB).

In addition to color space conversions, the LF2250 offers a range of selectable configurations designed for filtering applications. When configured as a 9-tap FIR filter, the LF2250 automatically selects the necessary internal bus structure and inserts the appropriate data path delay elements. In addition, a 16-bit cascade input port allows for the creation of larger filters without a reduction in throughput.

Real-time video image filtering using the convolver modes of the LF2250 can provide edge detection, texture enhancement, and detail smoothing. Both pixel convolver configurations, 3 x 3 and 4 x 2, deliver high-speed data manipulation in a single chip solution. By using the 16-bit cascade input port to cascade two devices, cubic convolutions (4 x 4-pixel) can be easily accommodated with no decrease in throughput rates.

All inputs and outputs, as well as all control lines, are registered on the rising edge of clock. The LF2250 operates at clock rates up to 50 MHz over the full commercial temperature and supply voltage ranges.

LF2250 BLOCK DIAGRAM

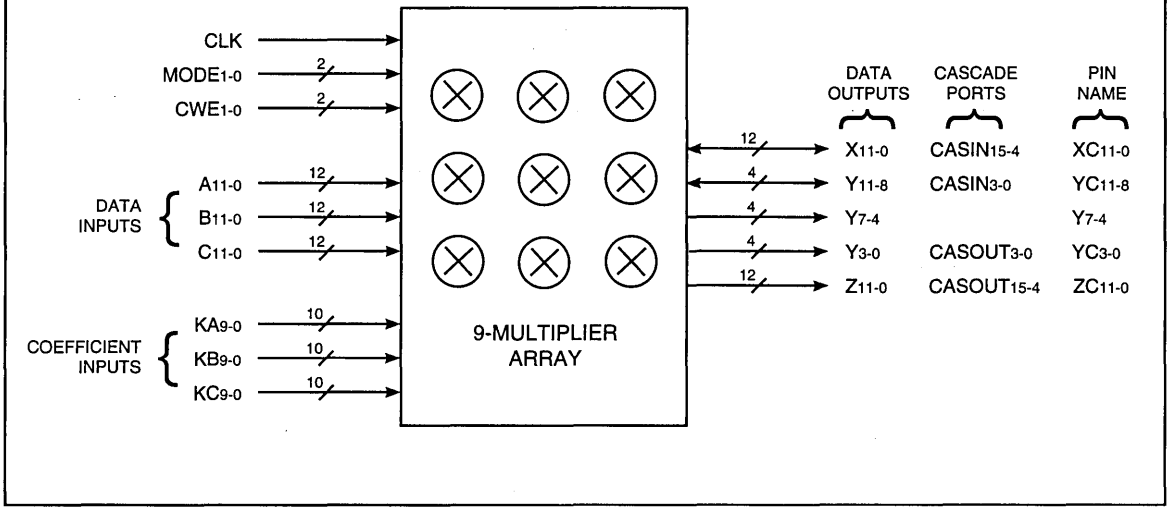


TABLE 1. MODE SELECTION

MODE1-0	OPERATING MODE
00	3 x 3 Matrix Multiplier
01	9-Tap FIR Filter
10	3 x 3 Convolver
11	4 x 2 Convolver

OPERATING MODES

The LF2250 can realize four different user-selectable digital filtering architectures as determined by the state of the mode (MODE1-0) inputs. Upon selection of the desired function, the LF2250 automatically chooses the appropriate internal data paths and input/output bus structure. Table 1 details the modes of operation.

DATA FORMATTING

The coefficient input ports (KA, KB, KC) are 10-bit fractional two's complement format regardless of the operating mode. The data input ports (A, B, C) are 12-bit integer two's complement format regardless of the operating mode.

In the matrix multiplier mode (Mode 00), the data output ports (X, Y, Z) are 12-bit integer two's complement format. In the FIR filter and convolver modes (Modes 01, 10, 11), the X, Y, and Z ports are configured as the cascade-in (CASIN15-0) and cascade-out (CASOUT15-0) ports. These ports assume 16-bit (12-bit integer, 4-bit fractional) two's complement data on both the inputs and outputs. Table 2 shows the data port formatting for each of the four operating modes.

BIT WEIGHTING

The internal sum of products of the LF2250 can grow to 23 bits. However, in order to keep the output format of the matrix multiply mode (Mode 00) identical to the input format, the X, Y, and Z outputs are truncated to 12-bit integer words. In the filter modes (Modes 01, 10, 11), the cascade output is always half-LSB rounded to 16 bits (12 integer bits and 4 fractional bits). The user may half-LSB round the output to any size less than 16 bits by simply forcing a "1" into the bit position of the cascade input immediately below the desired LSB. For example, if half-LSB rounding to 12 bits is desired, then a "1" must be forced into the CASIN3 bit position (CASOUT4 would then be the LSB).

In all four modes, the user may adjust the bit weighting, by applying an identical scaling correction factor to both the input and output data streams. If the coefficients are re-scaled, then the relative weightings of the cascade-in and cascade-out ports will differ accordingly. Figure 1 illustrates the input and output bit weightings for all four modes.

DATA OVERFLOW

Because the LF2250's matched input and output data formats accommodate unity gain (0 dB), input conditions that could lead to numeric overflow may exist. To ensure that no overflow conditions occur, the user must be aware of the maximum input data and coefficient word sizes allowable for each specific algorithm being performed.

SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

A11-0, B11-0, C11-0 — Data Inputs

A, B, and C are the 12-bit registered data input ports. Data presented to these ports is latched into the multiplier input registers for the current operating mode (Table 1). In the filter modes (Modes 01, 10, 11), the rising edge of CLK internally right-shifts new data to the next filter tap.

KA9-0, KB9-0, KC9-0 — Coefficient Inputs

KA, KB, and KC are the 10-bit registered coefficient input ports. Data presented to these ports is latched into the corresponding internal coefficient register set defined by CWE1-0 (Table 4) on the next rising edge of CLK. Table 3 shows which coefficient registers are available for each coefficient input port.

TABLE 2. DATA PORT FORMATTING

	PIN NAMES										
MODE1-0	A11-0	B11-0	C11-0	KA9-0	KB9-0	KC9-0	XC11-0	YC11-8	Y7-4	YC3-0	ZC11-0
00	A11-0	B11-0	C11-0	KA9-0	KB9-0	KC9-0	X11-0	Y11-8	Y7-4	Y3-0	Z11-0
01	A11-0	A11-0	NC	KA9-0	KB9-0	KC9-0	CASIN15-4	CASIN3-0	NC	CASOUT3-0	CASOUT15-4
10	A11-0	B11-0	C11-0	KA9-0	KB9-0	KC9-0	CASIN15-4	CASIN3-0	NC	CASOUT3-0	CASOUT15-4
11	A11-0	B11-0	NC	KA9-0	KB9-0	KC9-0	CASIN15-4	CASIN3-0	NC	CASOUT3-0	CASOUT15-4

FIGURE 1A. INPUT FORMATS

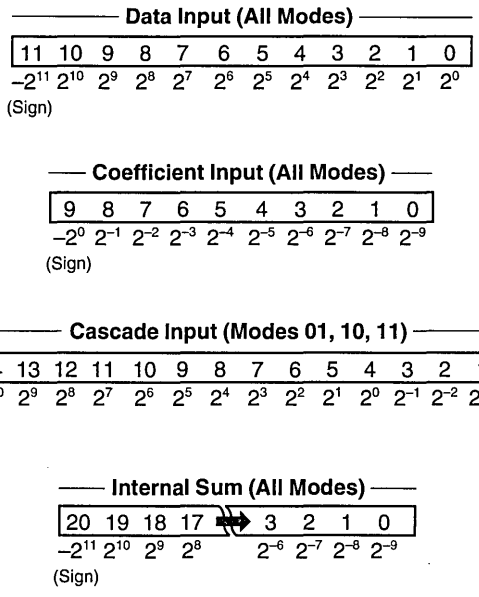
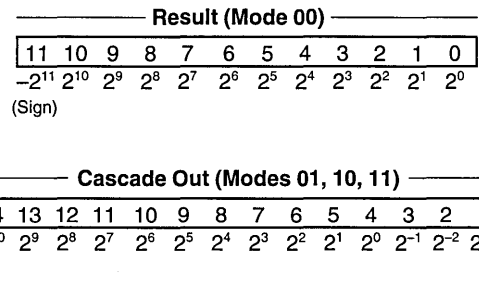


FIGURE 1B. OUTPUT FORMATS



CASIN15-0 — Cascade Input

In the filter modes (Modes 01, 10, 11), the 12-bit X port and four bits of the Y port are internally reconfigured as the 16-bit registered cascade input port. Data presented to this port will be added to the internal sum of products.

Outputs

X11-0, Y11-0, Z11-0 — Data Outputs

X, Y, and Z are the 12-bit registered output ports for the matrix multiply mode (Mode 00). These ports are automatically reconfigured for the filter modes (Modes 01, 10, 11) as the cascade-in and cascade-out ports.

CASOUT15-0 — Cascade Output

In the filter modes (Modes 01, 10, 11), the 12-bit Z port and four bits of the Y port are internally reconfigured as the 16-bit registered cascade output port.

NOTE: The X, Y, and Z ports are automatically reconfigured by the LF2250 as the cascade-in and cascade-out ports as required for each operating mode. Because both the X and Z ports are used for the cascade ports, all X port pins and all Z port pins are labelled as XC and ZC, respectively. All Y port pins that are used for the cascade ports are labelled as YC. Those Y port pins which are not used for the cascade ports are labelled as Y.

Controls

MODE1-0 — Mode Select

The registered mode select inputs determine the operating mode of the LF2250 (Table 1) for data being input on the next clock cycle. When switching between modes, the internal pipeline latencies of the device must be observed. After switching operating modes, the user must allow enough clock cycles to pass to flush the internal registers before valid data will appear on the outputs.

CWE1-0 — Coefficient Write Enable

The registered coefficient write enable inputs determine which internal coefficient register set to update (Table 4) on the next clock cycle.

TABLE 3. COEFFICIENT INPUTS

INPUT PORT	REG. AVAILABLE
KA	KA1, KA2, KA3
KB	KB1, KB2, KB3
KC	KC1, KC2, KC3

TABLE 4. COEFF. REG. UPDATE	
CWE1-0	COEFFICIENT SET
00	Hold All Registers
01	KA1, KB1, KC1
10	KA2, KB2, KC2
11	KA3, KB3, KC3

DETAILS OF OPERATION

3 x 3 Matrix Multiplier — Mode 00

In this mode, all three input ports (A, B, C) and all three output ports (X, Y, Z) are utilized to implement a 3 x 3 matrix multiplication (triple dot product). Each rounded 12-bit output is the sum of all three input words multiplied by the appropriate coefficients (Table 5). The pipeline latency for this mode is five clock cycles. Therefore, the sum of products will be output five clock cycles after the input data has been latched. New output data is subsequently available every clock cycle thereafter.

9-Tap FIR Filter — Mode 01

This mode utilizes the 12-bit A and B data input ports as well as the 16-bit CASIN port. The input data should be presented to the A and B ports simultaneously. The resulting 9-sample response, which is half-LSB rounded to 16 bits, begins after five clock cycles and ends after 13 clock cycles (Table 5). The pipeline latency from the input of an impulse response to the center of the output response is nine clock cycles. The latency from the CASIN port to the CASOUT port is four clock cycles. New output data is available every clock cycle.

3 x 3-Pixel Convolver — Mode 10

When configured in this mode, line delayed data is loaded through the A, B, and C input ports. During each cycle, a new rounded 16-bit output (comprising of the summation of the multiplications of the last nine data inputs with their related coefficients) becomes available (Table 5). The CASIN term is also added to each new output. The internal bus structure and pipeline delays allow new input data to be added every cycle while maintaining the structure of the filtering operation. This addition of new data every cycle produces the effect of the convolution window moving to the next pixel column.

4 x 2-Pixel Convolver — Mode 11

Using the A and B ports, input data is loaded and multiplied by the on-board coefficients. These products are then summed with the CASIN data and rounded to create the 16-bit output. The cascade ports allow multiple devices to be used together for use with larger kernels. As with Mode 10, each cycle results in a 16-bit output created from the products and summations performed.

TABLE 5. LATENCY EQUATIONS

3 x 3 Matrix Multiplier — Mode 00

$$X(n+4) = A(n)KA1(n) + B(n)KB1(n) + C(n)KC1(n)$$
$$Y(n+4) = A(n)KA2(n) + B(n)KB2(n) + C(n)KC2(n)$$
$$Z(n+4) = A(n)KA3(n) + B(n)KB3(n) + C(n)KC3(n)$$

9-Tap FIR Filter — Mode 01

$$\begin{aligned} CASOUT(n+12) = {} & A(n+8)KA3(n+8) + A(n+7)KA2(n+7) + A(n+6)KA1(n+6) \\ & + B(n+5)KB3(n+8) + B(n+4)KB2(n+7) + B(n+3)KB1(n+6) \\ & + B(n+2)KC3(n+8) + B(n+1)KC2(n+7) + B(n)KC1(n+6) \\ & + CASIN(n+9) \end{aligned}$$

3 x 3-Pixel Convolver — Mode 10

$$\begin{aligned} CASOUT(n+6) = {} & A(n+2)KA3(n+2) + A(n+1)KA2(n+1) + A(n)KA1(n) \\ & + B(n+2)KB3(n+2) + B(n+1)KB2(n+1) + B(n)KB1(n) \\ & + C(n+2)KC3(n+2) + C(n+1)KC2(n+1) + C(n)KC1(n) \\ & + CASIN(n+3) \end{aligned}$$

4 x 2-Pixel Convolver — Mode 11

$$\begin{aligned} CASOUT(n+7) = {} & A(n+3)KA3(n+3) + A(n+2)KA2(n+2) + A(n+1)KA1(n+1) \\ & + A(n)KC3(n+3) + B(n+3)KB3(n+3) + B(n+2)KB2(n+2) \\ & + B(n+1)KB1(n+1) + B(n)KC1(n+1) \\ & + CASIN(n+4) \end{aligned}$$

FIGURE 2. 3 x 3 MATRIX MULTIPLIER — MODE 00

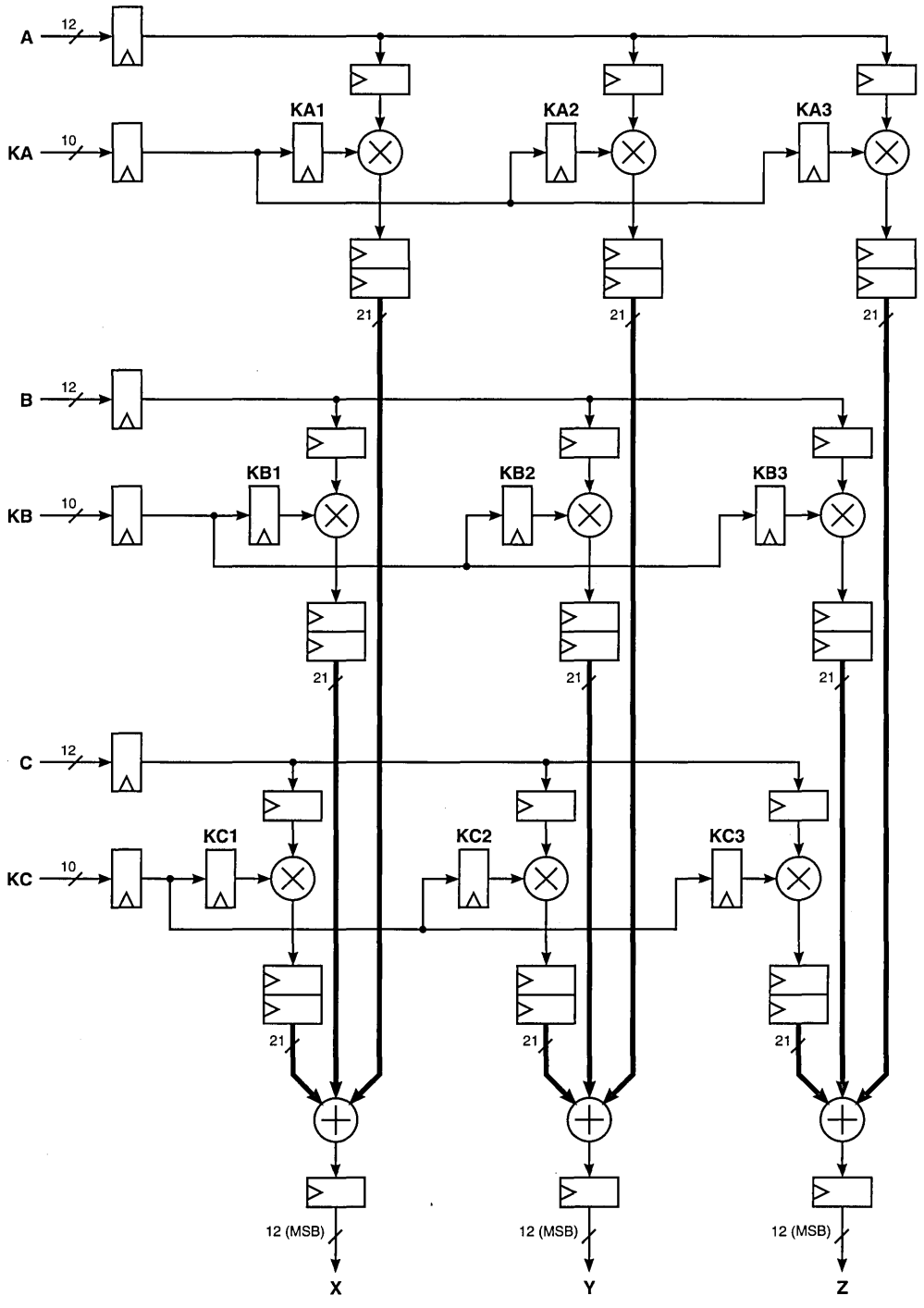
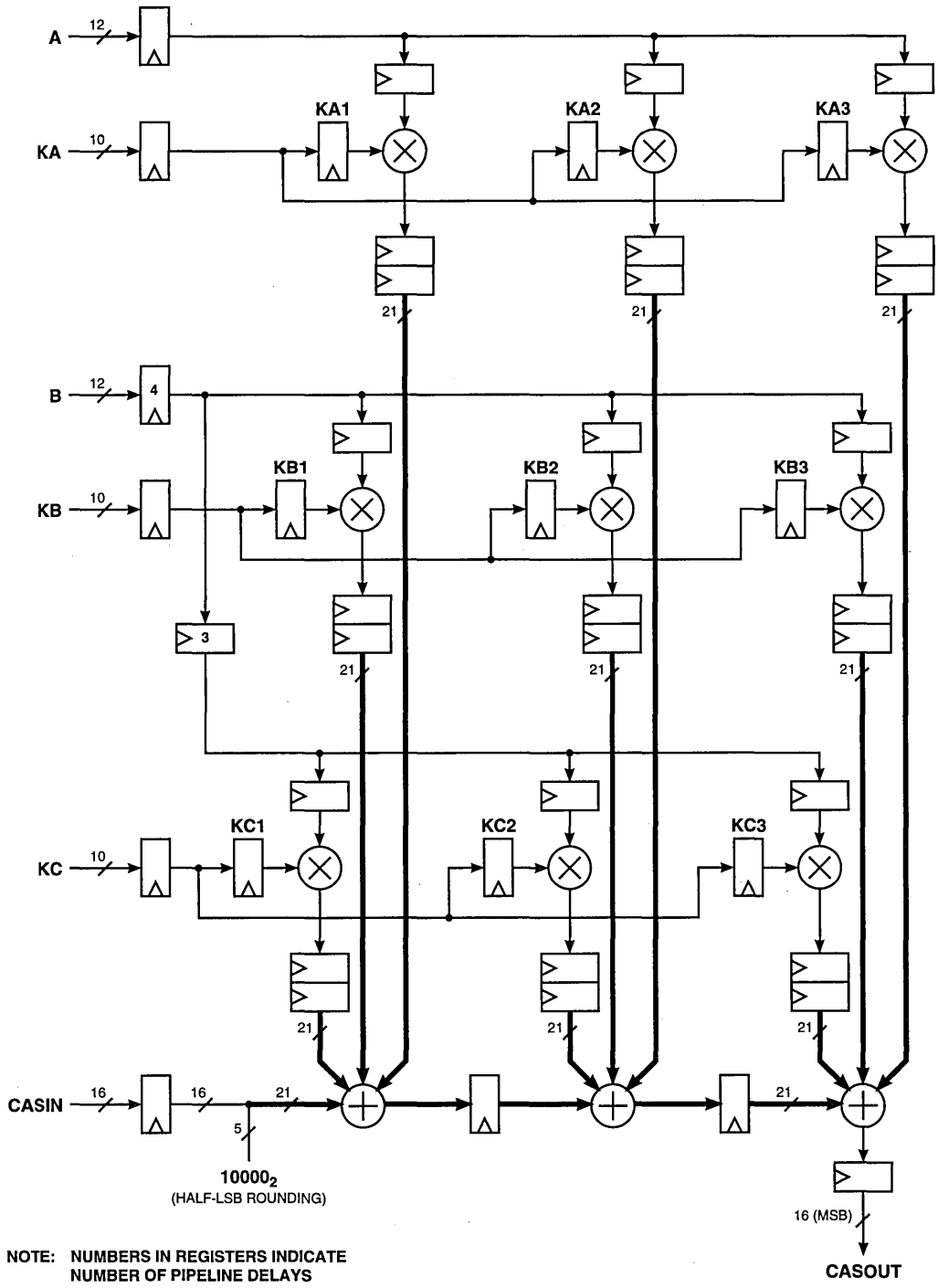


FIGURE 3. 9-TAP FIR FILTER — MODE 01



NOTE: NUMBERS IN REGISTERS INDICATE NUMBER OF PIPELINE DELAYS

FIGURE 4. 3 x 3-PIXEL CONVOLVER — MODE 10

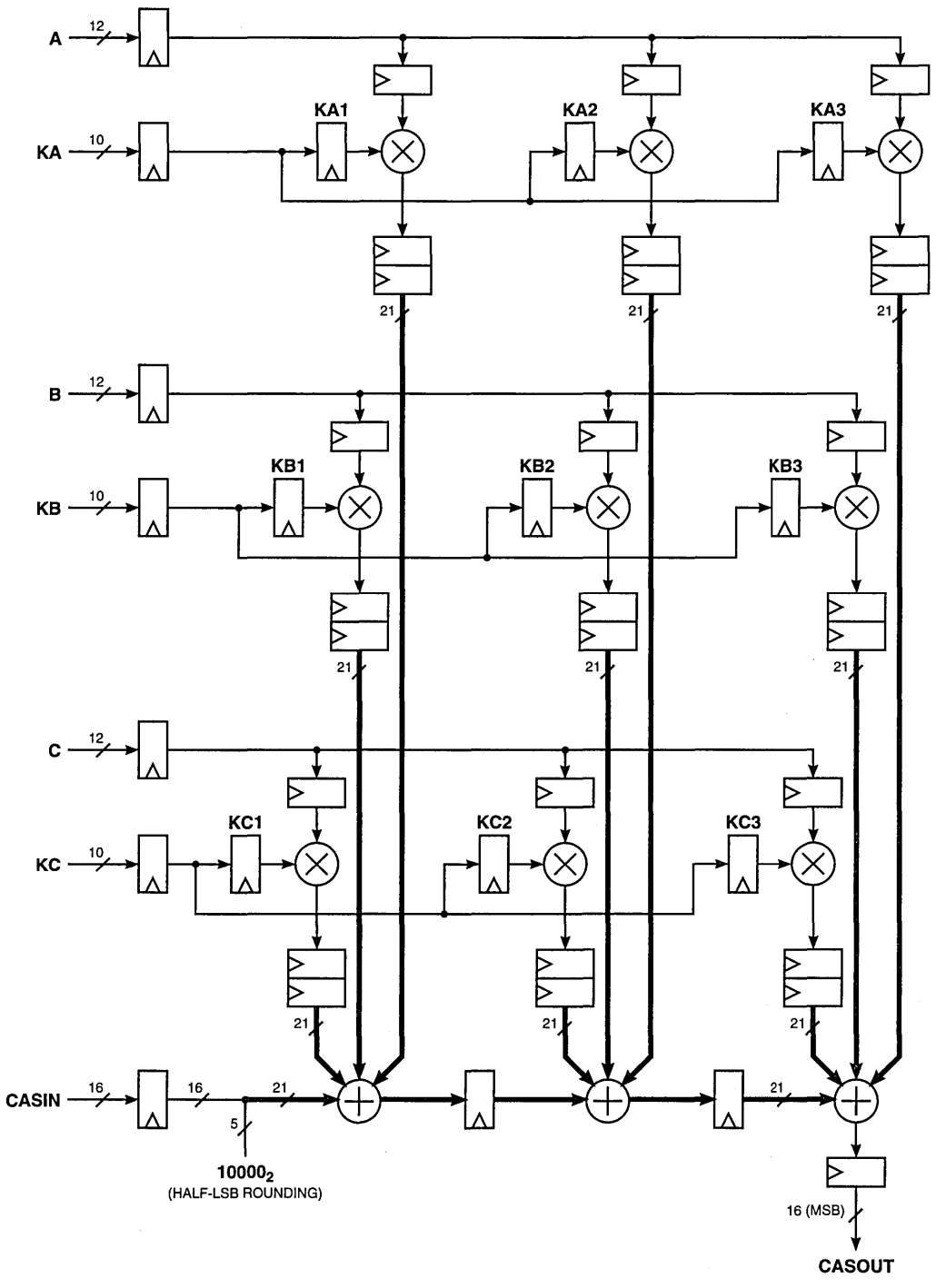
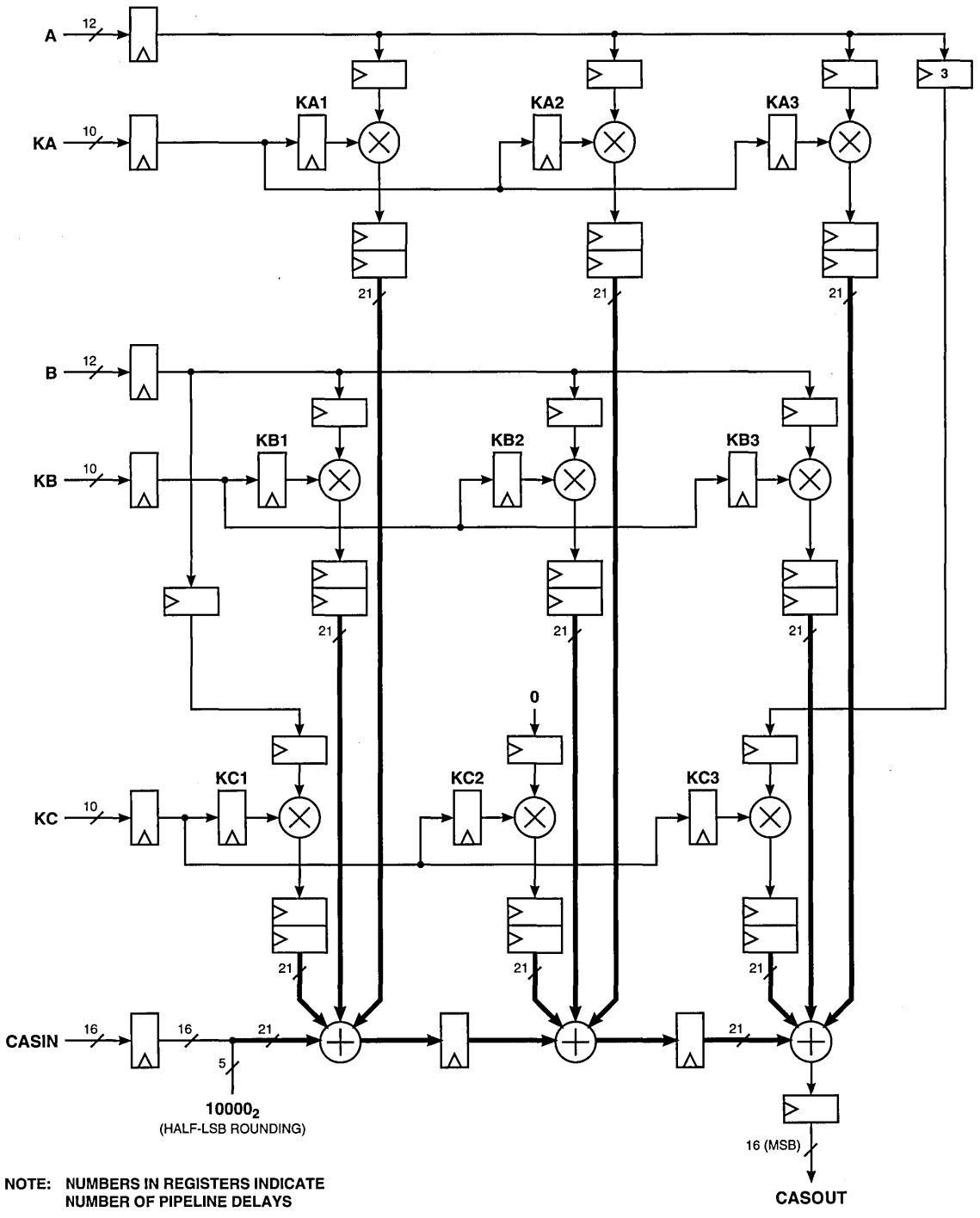


FIGURE 5. 4 x 2-PIXEL CONVOLVER — MODE 11



NOTE: NUMBERS IN REGISTERS INDICATE NUMBER OF PIPELINE DELAYS

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	−0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	(Note 12)			±40	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			160	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			12	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

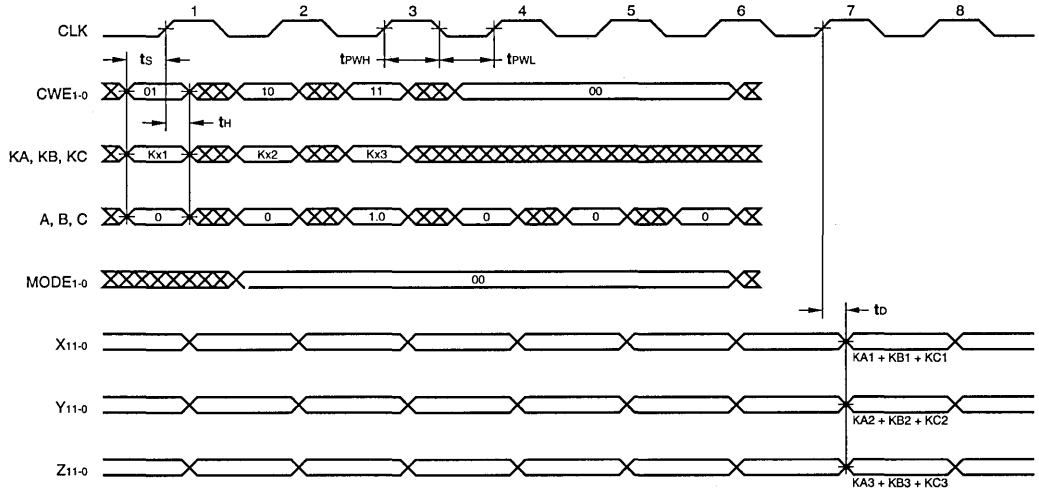
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF2250–					
		33		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	33		25		20	
t_{PWL}	Clock Pulse Width Low	15		10		6	
t_{PWH}	Clock Pulse Width High	10		10		8	
t_S	Input Setup Time	8		6		6	
t_H	Input Hold Time	0		0		0	
t_D	Output Delay		18		16		15

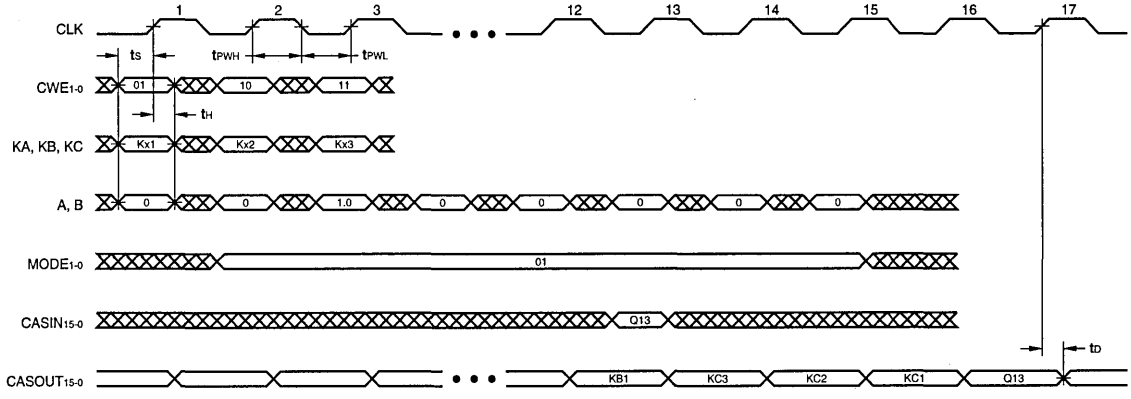
MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF2250–			
		33		25	
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	33		25	
t_{PWL}	Clock Pulse Width Low	15		10	
t_{PWH}	Clock Pulse Width High	10		10	
t_S	Input Setup Time	12		9	
t_H	Input Hold Time	2		2	
t_D	Output Delay		25		20

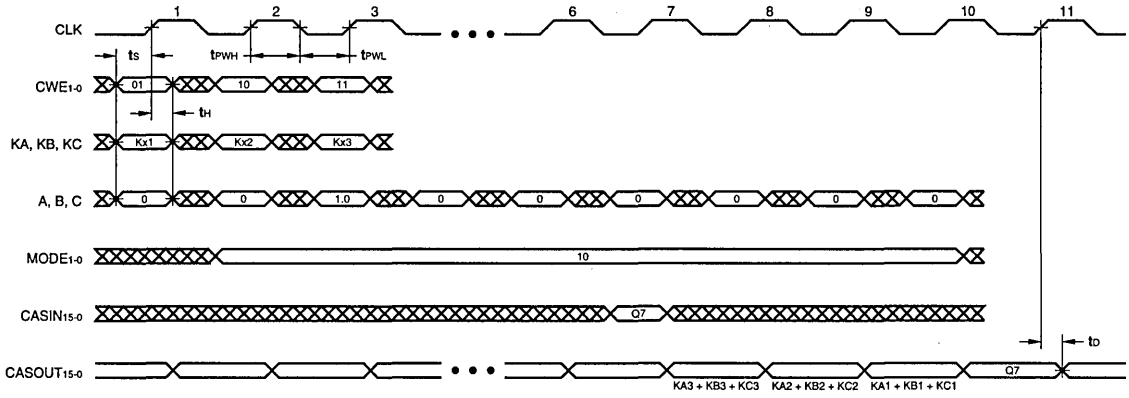
Switching Waveforms: 3 x 3 Matrix Multiplier — Mode 00



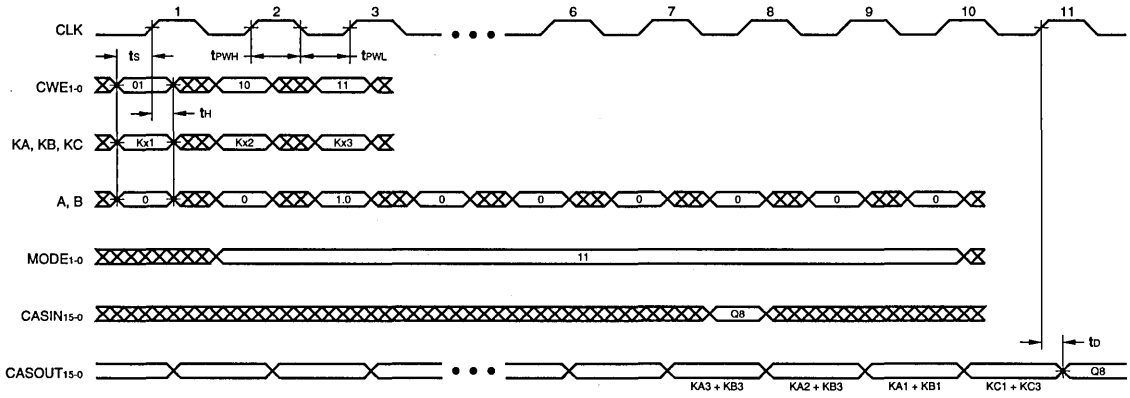
Switching Waveforms: 9-Tap FIR Filter — Mode 01



SWITCHING WAVEFORMS: 3 x 3-PIXEL CONVOLVER — MODE 10



SWITCHING WAVEFORMS: 4 x 2-PIXEL CONVOLVER — MODE 11



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

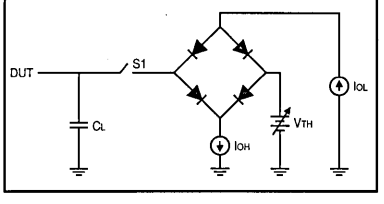
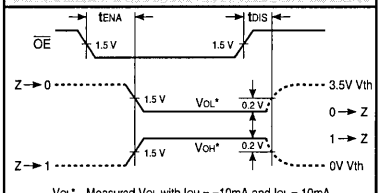
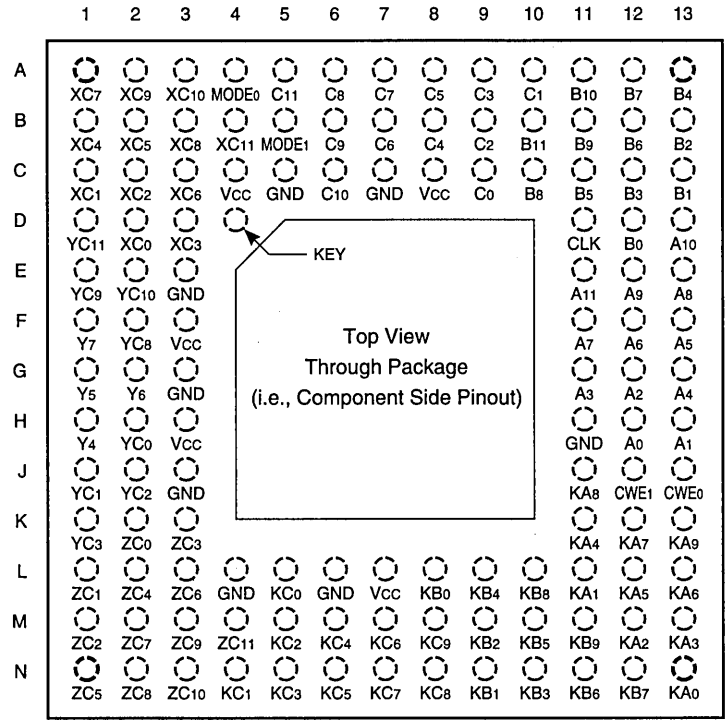


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

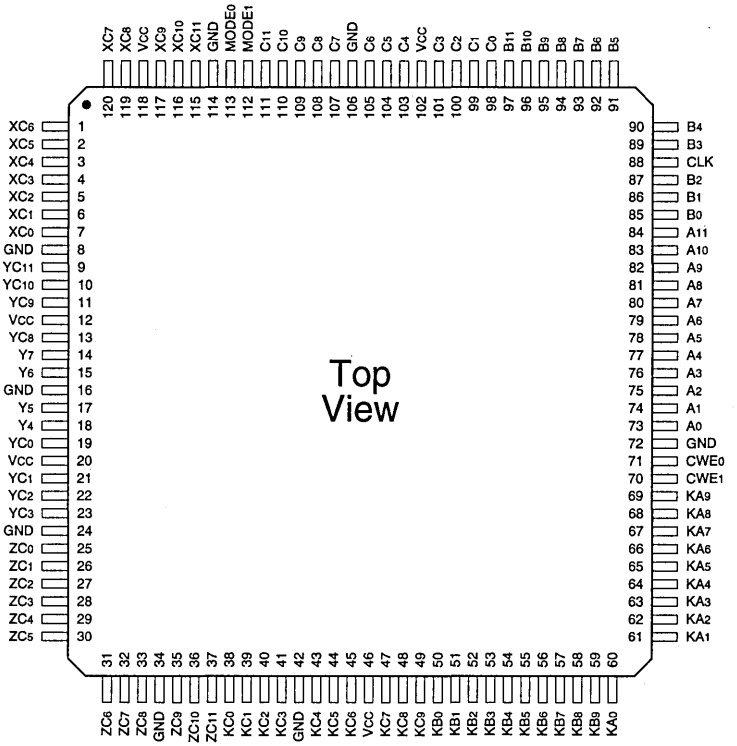
120-pin



Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C — COMMERCIAL SCREENING
33 ns	LF2250GC33
25 ns	LF2250GC25
20 ns	LF2250GC20
	–55°C to +125°C — COMMERCIAL SCREENING
33 ns	LF2250GM33
25 ns	LF2250GM25
	–55°C to +125°C — MIL-STD-883 COMPLIANT
33 ns	LF2250GMB33
25 ns	LF2250GMB25

ORDERING INFORMATION

120-pin



Speed	Plastic Quad Flatpack (Q1)
	0°C to +70°C — COMMERCIAL SCREENING
33 ns	LF2250QC33
25 ns	LF2250QC25
20 ns	LF2250QC20

LOGIC DEVICES INCORPORATED

LF2272
Colorspace Converter/ Corrector (3 x 12-bits)

FEATURES

- 50 MHz Data and Computation Rate
- Full Precision Internal Calculations with Output Rounding
- On-board 10-bit Coefficient Storage
- Overflow Capability in Low Resolution Applications
- Two's Complement Input and Output Data Format
- 3 Simultaneous 12-bit Channels (64 Giga Colors)
- Applications:
  - Component Color Standards Translations (RGB, YIQ, YUV)
  - Color-Temperature Conversion
  - Image Capturing and Manipulation
  - Composite Color Encoding/ Decoding
  - Three-Dimensional Perspective Translation
- Replaces TRW/Raytheon TMC2272
- Package Styles Available:
  - 120-pin Pin Grid Array
  - 120-pin Plastic Quad Flatpack

DESCRIPTION

The **LF2272** is a high-speed digital colorspace converter/corrector consisting of three simultaneous 12-bit input and output channels for functionality up to 64 Giga (2^{36}) colors. Some of the applications the LF2272 can be used for include phosphor colorimetry correction, image capturing and manipulation, composite color encoding/decoding, color matching, and composite color standards conversion/transcoding.

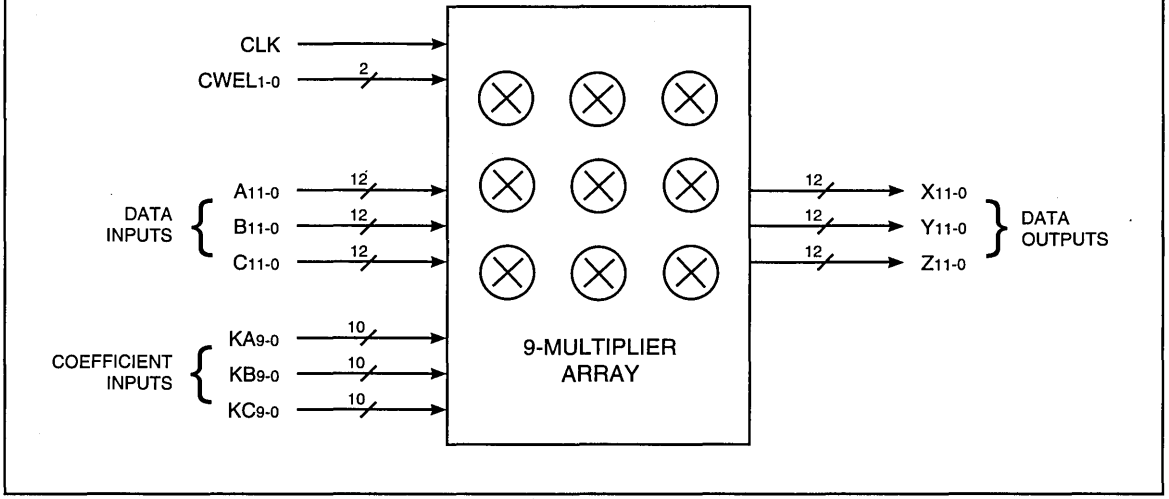
The 3 x 3 matrix multiplier (triple dot product) allows users to easily perform three-dimensional perspective translations or video format conversions at real-time video rates. By using the LF2272, conversions can be made from the RGB (color component) format to the YIQ (quadrature encoded chrominance) or YUV (color difference) formats and vice versa (YIQ or YUV to RGB). Differing signal formats in each stage of a system can be disregarded. For example, using an LF2272 at each format interface allows each stage of a system to operate on the data while in the appropriate format.

All inputs and outputs, as well as all control lines, are registered on the rising edge of clock. The LF2272 operates at clock rates up to 50 MHz over the full commercial temperature and supply voltage ranges. A narrower data path can be used to allow the LF2272 to work with many different imaging applications.

DETAILS OF OPERATION

All three input ports (A, B, C) and all three output ports (X, Y, Z) are utilized to implement a 3 x 3 matrix multiplication (triple dot product). Each truncated 12-bit output is the sum of all three input words multiplied by the appropriate coefficients (Table 1). The pipeline latency is five clock cycles. Therefore, the sum of

LF2272 BLOCK DIAGRAM



products will be output five clock cycles after the input data has been registered. New output data is subsequently available every clock cycle thereafter.

DATA FORMATTING

The data input ports (A, B, C) and data output ports (X, Y, Z) are 12-bit integer two's complement format.

The coefficient input ports (KA, KB, KC) are 10-bit fractional two's complement format. Refer to Figures 1a and 1b.

BIT WEIGHTING

The internal sum of products of the LF2272 can grow to 23 bits. However, in order to keep the output format identical to the input format, the X, Y, and Z outputs are rounded to 12-bit integer words. The rounding is done only at the final output stage to allow accuracy, with correct rounding and overflow, for applications requiring less than 12-bit integer words. The user may adjust the bit weighting by applying an identical scaling correction factor to both the input and output data streams.

TABLE 1. LATENCY EQUATIONS

$$X(n+4) = A(n)KA1(n) + B(n)KB1(n) + C(n)KC1(n)$$
$$Y(n+4) = A(n)KA2(n) + B(n)KB2(n) + C(n)KC2(n)$$
$$Z(n+4) = A(n)KA3(n) + B(n)KB3(n) + C(n)KC3(n)$$

DATA OVERFLOW

Because the LF2272's matched input and output data formats accommodate unity gain (0 dB), input conditions that could lead to numeric overflow may exist. To ensure that no overflow conditions occur, the user must be aware of the maximum input data and coefficient word sizes allowable for each specific algorithm being performed.

SYSTEMS SMALLER THAN 12-BITS

Using a data path less than 12-bits requires the input data to be right justified and sign extended to 12-bits because the LF2272 carries out all calculations to full precision. Since all least-significant bits are used, the desired X, Y, and Z outputs are rounded correctly and upper-order output bits are used for overflow.

FIGURE 1A. INPUT FORMATS

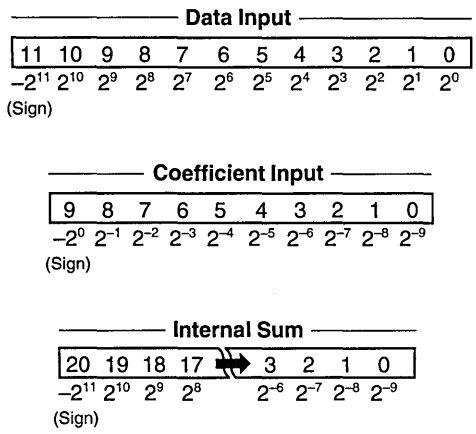
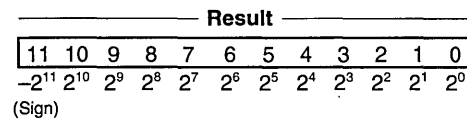


FIGURE 1B. OUTPUT FORMAT



SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

A11-0, B11-0, C11-0 — Data Inputs

A, B, and C are the 12-bit registered data input ports. Data presented to these ports is latched into the multiplier input registers.

KA9-0, KB9-0, KC9-0 — Coefficient Inputs

KA, KB, and KC are the 10-bit registered coefficient input ports. Data presented to these ports is latched into the corresponding internal coefficient register set defined by CWEL1-0 (Table 3) on the next rising edge of CLK. Table 2 shows which coefficient registers are available for each coefficient input port.

TABLE 2. COEFFICIENT INPUTS

INPUT PORT	REG. AVAILABLE
KA	KA1, KA2, KA3
KB	KB1, KB2, KB3
KC	KC1, KC2, KC3

TABLE 3. COEFF. REG. UPDATE

CWEL1-0	COEFFICIENT SET
00	Hold All Registers
01	KA1, KB1, KC1
10	KA2, KB2, KC2
11	KA3, KB3, KC3

Outputs

X11-0, Y11-0, Z11-0 — Data Outputs

X, Y, and Z are the 12-bit registered data output ports.

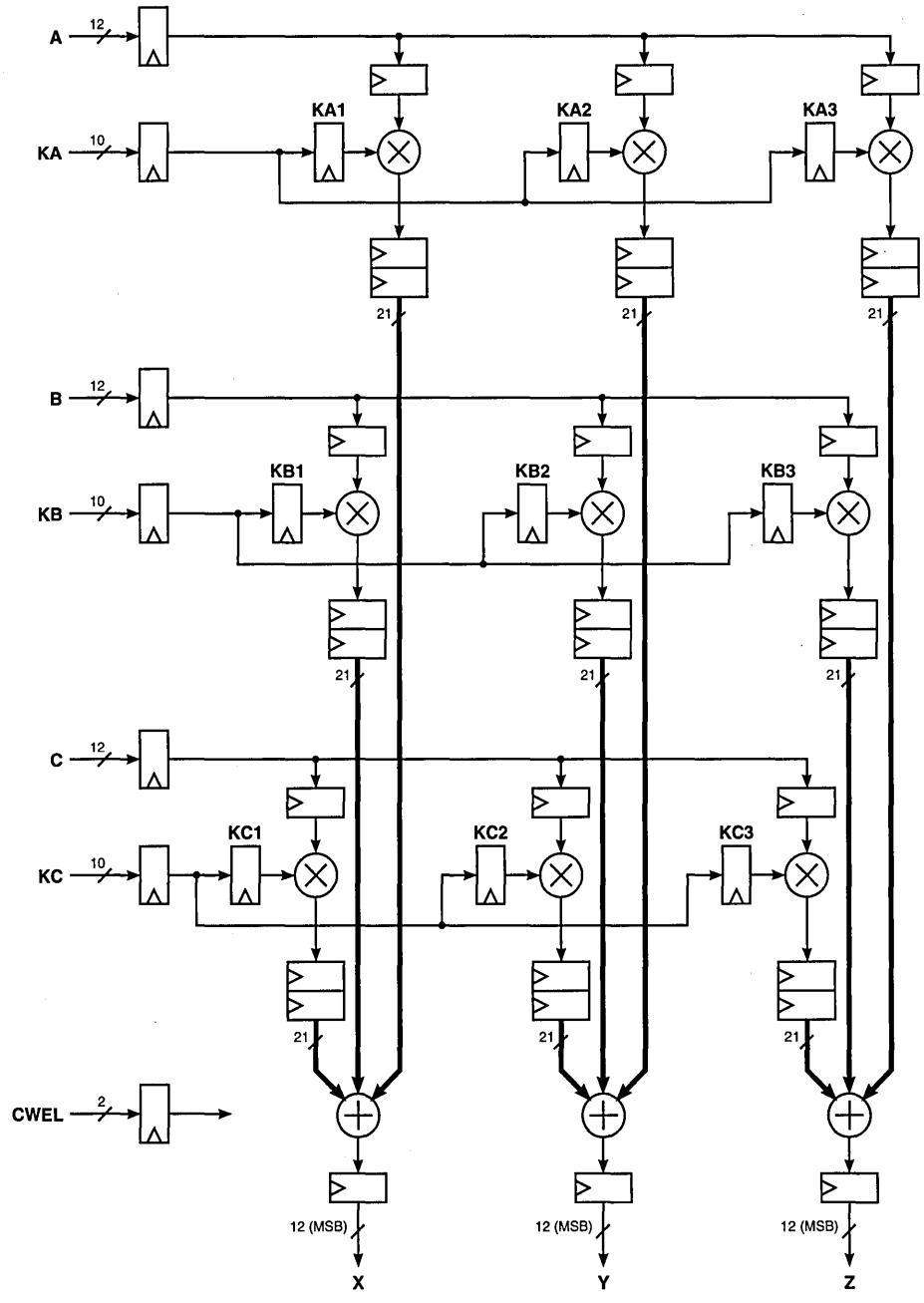
Controls

CWEL1-0 — Coefficient Write Enable

The registered coefficient write enable inputs determine which internal coefficient register set to update (Table 3) on the next clock cycle.

2

FIGURE 2. DETAILED FUNCTIONAL DIAGRAM



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	−0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	(Note 12)			±40	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			160	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			12	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

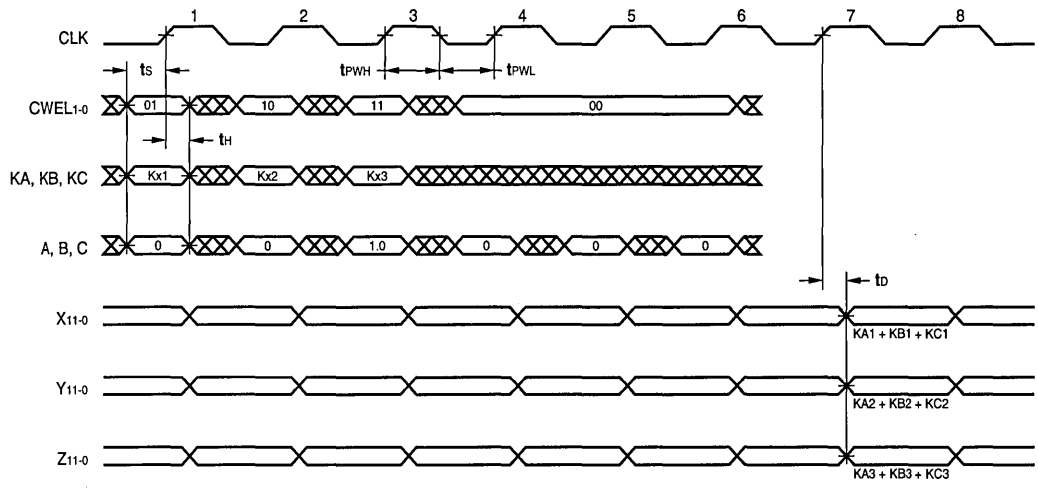
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF2272–					
		33		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	33		25		20	
t_{PWL}	Clock Pulse Width Low	15		10		6	
t_{PWH}	Clock Pulse Width High	10		10		8	
t_S	Input Setup Time	8		6		6	
t_H	Input Hold Time	0		0		0	
t_D	Output Delay		18		16		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF2272–			
		33		25	
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	33		25	
t_{PWL}	Clock Pulse Width Low	15		10	
t_{PWH}	Clock Pulse Width High	10		10	
t_S	Input Setup Time	12		9	
t_H	Input Hold Time	0		0	
t_D	Output Delay		25		20

SWITCHING WAVEFORM



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

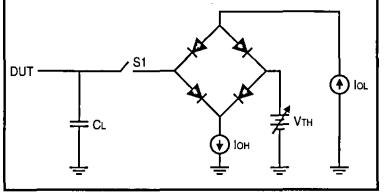
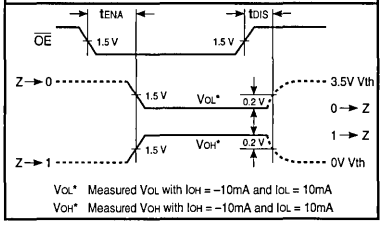
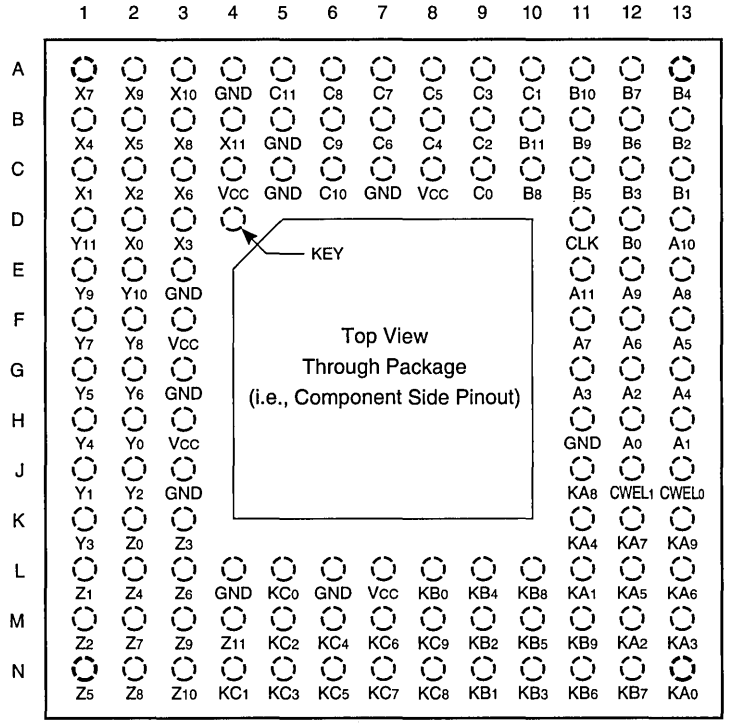


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

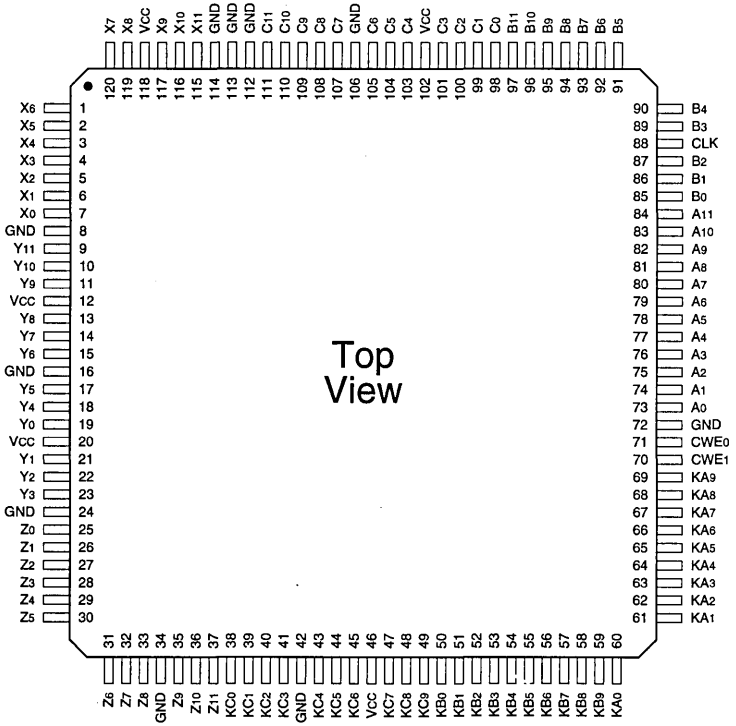
120-pin



Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C — COMMERCIAL SCREENING
33 ns	LF2272GC33
25 ns	LF2272GC25
20 ns	LF2272GC20
	–55°C to +125°C — COMMERCIAL SCREENING
33 ns	LF2272GM33
25 ns	LF2272GM25
	–55°C to +125°C — MIL-STD-883 COMPLIANT
33 ns	LF2272GMB33
25 ns	LF2272GMB25

ORDERING INFORMATION

120-pin



Speed	Plastic Quad Flatpack (Q1)
0°C to +70°C — COMMERCIAL SCREENING	
33 ns	LF2272QC33
25 ns	LF2272QC25
20 ns	LF2272QC20

LF2301
Image Resampling Sequencer

FEATURES

- 40 MHz Clock Rate
- High-Speed Image Manipulation
- Maximum Image Size: 4096 x 4096 Pixels
- Supports Following Interpolation Algorithms:
  - Nearest-Neighbor
  - Bilinear Interpolation
  - Cubic Convolution
- Applications:
  - Video Special-Effects
  - Image Recognition
  - High-Speed Data Encoding/Decoding
- Available 100% Screened to MIL-STD-883, Class B
- Replaces TRW/Raytheon TMC2301
- Package Styles Available:
  - 68-pin Pin Grid Array
  - 68-pin Plastic LCC, J-Lead

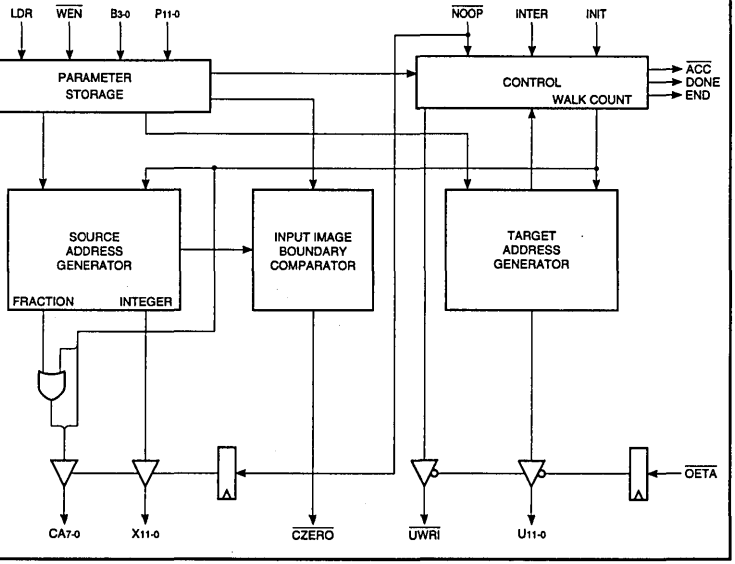
DESCRIPTION

The **LF2301** is a self-sequencing address generator designed to filter a two-dimensional image or remap and resample it from one set of Cartesian coordinates (x,y) into a new set (u,v).

The LF2301 can resample digitized images or perform such manipulations as rotation, panning, zooming, and warping as well as compression in real-time.

By using two LF2301s in a Image Transformation System (ITS), nearest-neighbor, bilinear interpolation, and cubic convolution algorithms, with kernel sizes up to 4 x 4 pixels, are all possible (see Figure 1). This system can also implement simple static filters with kernel sizes up to 16 x 16 pixels.

LF2301 Block Diagram



DETAILS OF OPERATION

Most video applications use a pair of LF2301s in tandem to construct an ITS. One LF2301 is the row coordinate generator (x to u) and the other is the column generator (y to v). External RAM is needed for storage of the interpolation coefficient lookup table, as well as for buffers of the source and destination images. An external Multiplier-Accumulator is required when performing interpolation or implementing static filters.

The ITS is capable of performing the general second-order coordinate transformation of the form:

$$x(u,v) = Au^2 + Bu + Cuv + Dv^2 + Ev + F$$

$$y(u,v) = Gu^2 + Hu + Kuv + Lv^2 + Mv + N$$

where parameters A through N of the transform are user-defined. The system steps sequentially through each pixel in the "target" image lying within a user-defined rectangle. For each "target" pixel at (u,v), the LF2301 points to a corresponding "source" pixel at (x,y).

SIGNAL DEFINITIONS

Power

Vcc and GND

+5V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers.

Inputs

P11-0 — Parameter Register Data Input

P11-0 is the 12-bit Parameter Register Data input port. P11-0 is latched on the rising edge of CLK.

B3-0 — Parameter Register Address Input

B3-0 is the 4-bit Parameter Register Address input port. B3-0 is latched on the rising edge of CLK.

Outputs

X11-0 — Source Address Output

X11-0 is the 12-bit registered Source Address output port.

CA7-0 — Coefficient Address Output

CA7-0 is the 8-bit registered Coefficient Address output port.

U11-0 — Target Address Output

U11-0 is the 12-bit registered Target Address output port.

Controls

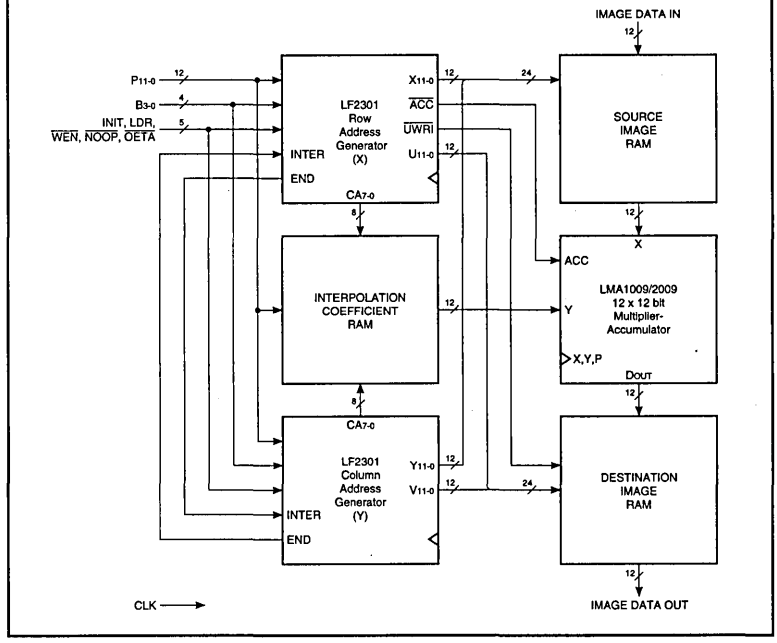
INIT — Initialize

When INIT is HIGH for a minimum of two clock cycles, the control logic is cleared and initialized for the start of a new image transformation. When INIT goes LOW, normal operation begins after two clock cycles. INIT is latched on the rising edge of CLK.

$\overline{WEN}$ — Write Enable

When $\overline{WEN}$ is LOW, data latched into the device on P11-0 is loaded into the preload register addressed by the data latched into the device on B3-0. When $\overline{WEN}$ is HIGH, data cannot be loaded into the preload registers and their contents will not be changed. $\overline{WEN}$ is latched on the rising edge of CLK.

FIGURE 1. IMAGE TRANSFORMATION SYSTEM (ITS)



LDR — Load Data Register

When LDR is HIGH, data in all preload registers is latched into the Transformation Parameter Registers. When LDR is LOW, data cannot be loaded into the Transformation Parameter Registers and their contents will not be changed. LDR is latched on the rising edge of CLK.

$\overline{ACC}$ — Accumulate

The registered $\overline{ACC}$ output initializes the accumulation register of the external multiplier-accumulator. At the start of each interpolation "walk," $\overline{ACC}$ goes LOW for one cycle effectively clearing the storage register by loading in only the new first product. $\overline{ACC}$ from either the row or column LF2301 may be used.

$\overline{UWRI}$ — Target Memory Write Enable

The Target Memory Write Enable goes LOW for one clock cycle after the end of each interpolation "walk." When $\overline{OETA}$ is HIGH, this registered output is forced to the high-impedance state. $\overline{UWRI}$ from either the row or column LF2301 may be used.

INTER — Interconnect

When two LF2301s are used to form an ITS, the END flag on each device is connected to INTER on the other device. The END flag from the row device indicates an "end of line" to the column device. The END flag from the column device indicates a "bottom of frame" to the row device, forcing a reset of the address counter.

$\overline{NOOP}$ — No Operation

When $\overline{NOOP}$ is LOW, the clock is overridden holding all address generators in their current state. X11-0 and CA7-0 are forced to the high-

impedance state. Users may then access external memory. Normal operation resumes on the next clock cycle after $\overline{NOOP}$ goes HIGH. $\overline{NOOP}$ is latched on the rising edge of CLK.

$\overline{OETA}$ — Target Memory Output Enable

When $\overline{OETA}$ is HIGH, $\overline{UWRI}$ and $U_{11\text{-}0}$ are forced to the high-impedance state. When $\overline{OETA}$ is LOW, $\overline{UWRI}$ and $U_{11\text{-}0}$ are enabled on the next clock cycle. $\overline{OETA}$ is latched on the rising edge of CLK.

Flags

$\overline{CZERO}$ — Coefficient Zero

If in a row device $x<0$, $XMIN \le x \le XMAX$, or $x \ge 4096$, the registered $\overline{CZERO}$ flag goes HIGH. If $0 \le x < XMIN$ or $XMAX < x < 4096$, $\overline{CZERO}$ goes LOW. In an ITS, when the source address falls outside a rectangle with vertices (XMIN, YMIN), (XMAX, YMIN), (XMIN, YMAX), and (XMAX, YMAX), the logical AND of the $\overline{CZERO}$ flags from the row and column of the LF2301s will go LOW representing an invalid address.

END — End of Row/Frame

When two LF2301s are used to form an ITS, the END flag on each device is connected to INTER on the other device. The END flag from the row device indicates an "end of line" to the column device. The END flag from the column device indicates a "bottom of frame" to the row device, forcing a reset of the address counter.

When Mode is set to "00" or "10" END goes HIGH on the row device for (K+1) x (K+1) clock cycles starting [2 x (K+1) x (K+1)] + 1 clock cycles before the last X address of a row. END goes HIGH on the column device for $(K+1)^3$ x (UMAX-UMIN) clock cycles starting at $(K+1)^3$ x (UMAX-UMIN) +1 clock cycles before the last X address of a frame.

When Mode is set to "01" or "11" END goes HIGH on the row device for K+1 clock cycles starting at (K+1) + 2 clock cycles before the last X address of a row. END goes HIGH on the column device for (K+1) x (K+1) clock cycles starting at [(K+1) x (K+1)]+ 1 clock cycles before the last X address of a frame.

DONE — End of Transform

In a two LF2301 system, after the last walk of the last row of an image, the registered DONE flag goes HIGH indicating the end of the transform. DONE goes HIGH one clock cycle before the last X address of a frame. If AIN is HIGH, DONE will remain HIGH for one clock cycle. If AIN is LOW, DONE will remain HIGH until a new transform begins.

Transformation Control Parameters

XMIN, XMAX, YMIN, YMAX

XMIN, XMAX, YMIN, YMAX define the valid area in the source image from which pixels may be read. The $\overline{CZERO}$ flags will denote a valid memory read whenever the LF2301s generate an (x,y) address within this boundary.

UMIN, UMAX, VMIN, VMAX

UMIN, UMAX, VMIN, VMAX define the area in the destination image into which pixels will be written. (UMIN, VMIN) is the top left corner and (UMAX + 1, VMAX) is the bottom right corner. The following conditions must be met: UMAX>UMIN and VMAX>VMIN.

x_0, y_0

x_0, y_0 determine what the first pixel read out of the source image will be at the beginning of an image transformation. x_0, y_0 will be the upper left corner of the original image in non-inverting, non-reversing applications.

dx/du

dx/du is the displacement along the x axis corresponding to a one-pixel movement along the u axis.

dx/dv

dx/dv is the displacement along the x axis corresponding to each one-pixel movement along the v axis.

dy/du

dy/du is the displacement along the y axis corresponding to each one-pixel movement along the u axis.

dy/dv

dy/dv is the displacement along the y axis corresponding to each one-pixel movement along the v axis.

d^2x/du^2

d^2x/du^2 determines the rate of change of dx/du with each step along a line in the output image.

d^2x/dv^2

d^2x/dv^2 determines the rate of change of dx/dv with each step down a column in the output image.

d^2y/du^2

d^2y/du^2 determines the rate of change of dy/du with each step along a line in the output image.

d^2y/dv^2

d^2y/dv^2 determines the rate of change of dy/dv with each step down a column in the output image.

$d^2x/dudv$

$d^2x/dudv$ determines the rate of change of dx/du while moving vertically through the output image. $d^2x/dudv$ also determines the rate of change of dx/dv while moving horizontally through the output image.

$d^2y/dudv$

$d^2y/dudv$ determines the rate of change of dy/dv while moving horizontally through the output image. $d^2y/dudv$ also determines the rate of change of dy/du while moving vertically through the output image.

TABLE 1. MODE SELECTION		
M1	M0	MODE
0	0	single-pass operation (CW)
0	1	pass 1 of two-pass operation
1	0	single-pass operation (CCW)
1	1	pass 2 of two-pass operation

R/C — Row/Column Select

When set to 0, the LF2301 functions as a row device. When set to 1, the LF2301 functions as a column device.

M1-0 — Mode

This 2-bit control word defines four modes as follows (see table 1):

The 1st and 3rd modes are single-pass operations where the device walks through a (K + 1) x (K + 1) kernel for each output pixel. K is the kernel size determined by K3-0 in Parameter Register 7. In mode 00, the spiral walk is in the clockwise direction. In mode 10, the spiral walk is in the counter clockwise direction.

The 2nd and 4th modes are used together to perform a two-pass operation. The first pass (mode 01) performs a (K+1) kernel in the horizontal dimension. The second pass (mode 11) performs a (K+1) kernel in the vertical dimension.

The result of pass 1 is stored in the destination image memory and is used as the source image data for the second pass. A system to switch source and destination memory banks could be designed, or utilization of a second LF2301 pair in a pipelined architecture could be used. In this case, the system would require a third image buffer for the final destination image.

K3-0 — Kernel

Kernel determines the length of the spiral walk when performing image transformations and the size of the filter when implementing static filters (see table 2). When performing image transformations, the longest spiral walk possible is 4 x 4 pixels (Kernel = 3). For static filters, kernels of up to 16 x 16 pixels (Kernel = 15) are possible.

FOV — Field of View

FOV determines the distance between pixels in a spiral walk. An FOV of 1 means each step in a spiral walk is one pixel. An FOV of 2 means each step is two pixels, and so on. FOV can be set as high as 7 (see Table 3). It is important to note when FOV is 0, the x and y addresses will not change during a spiral walk. They will remain fixed at the first pixel address of the spiral walk.

ALR — Autoload

When set HIGH and upon INIT being strobed, the LDR control is automatically asserted which causes the data currently stored in the Preload Registers to be loaded into the Transformation Parameter Registers.

AIN — Autoinit

A new transform automatically begins if the AIN bit is HIGH when the end of an image is reached. The DONE flag will go HIGH for one clock cycle. If AIN is LOW, $\overline{\text{UWRI}}$ and the DONE flag remain HIGH until the user strobes the INIT control to begin a new image transformation.

PIPE — Pipe Control

In order to compensate for buffered source image RAM, PIPE adjusts the timing of $\overline{\text{UWRI}}$ and $\overline{\text{ACC}}$. If the PIPE bit is HIGH, $\overline{\text{UWRI}}$ and $\overline{\text{ACC}}$ will have a one clock cycle delay added relative to the generation of the target address.

TM — Test Mode

Calculations of the source image and coefficient addresses are made by an internal 28-bit accumulator. TM allows access to the sign bit and the seven bits below the four coefficient address bits in the accumulator. When TM is HIGH the sign bit and 11 bits below the source image address are fed to X11-0 (see Figure 2). When TM is LOW, the source image address is fed to X11-0. Two clock cycles are required to access both the MS and LS words of the internal accumulator.

Functional Description

The LF2301 is an address generator designed to be used in an image transformation system (ITS). When implementing an LF2301-based ITS, second-order image transformations can be performed like resampling, rotation, warping, panning, and rescaling, all at real-time video rates. 2D filtering operations, like pixel convolutions, can also be performed.

In most applications two LF2301s are used, one to generate the row addresses and the other to generate the column

TABLE 2. KERNEL				
K3	K2	K1	K0	Kernel
0	0	0	0	1 x 1
0	0	0	1	2 x 2
0	0	1	0	3 x 3
0	0	1	1	4 x 4
0	1	0	0	5 x 5
0	1	0	1	6 x 6
0	1	1	0	7 x 7
0	1	1	1	8 x 8
1	0	0	0	9 x 9
1	0	0	1	10 x 10
1	0	1	0	11 x 11
1	0	1	1	12 x 12
1	1	0	0	13 x 13
1	1	0	1	14 x 14
1	1	1	0	15 x 15
1	1	1	1	16 x 16

TABLE 3. FIELD OF VIEW			
F2	F1	F0	FOV
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

addresses. An example of an ITS implemented with two LF2301s is shown in Figure 1. In this system the following components are used: two LF2301s, a multiplier-accumulator (MAC), interpolation coefficient RAM, and source/target image RAM. Maximum image size is 4096 x 4096 pixels. Data word size is determined by the word size of the external RAM.

A typical ITS performs image transformations as follows:

a. The LF2301s generate sequential pixel addresses (left to right, top to bottom) which fill the rectangle in the target image RAM defined by (UMIN,VMIN) and (UMAX+1,VMAX). It is important to note that the U value of the last pixel address on each line of the target RAM is UMAX+1.

b. The LF2301s calculate the address of the corresponding pixel in the source image RAM for each target pixel address generated.

c. If interpolation is needed, the external MAC sums the products of the source pixels and the interpolation coefficients. Control signals for the MAC and address signals for the interpolation coefficient RAM are provided by the LF2301s.

d. The new pixel value is written into the target image RAM.

The LF2301s generate source pixel addresses according to the following general second order equations:

$x = Au^2 + Bu + Cuv + Dv^2 + Ev + F$

$y = Gu^2 + Hu + Kuv + Lv^2 + Mv + N$

where (x,y) and (u,v) are the source and target coordinates respectively. A through N are user-defined parameters. The actual second order equations used are shown in Figure 3.

FIGURE 2. TEST MODE DATA ROUTING

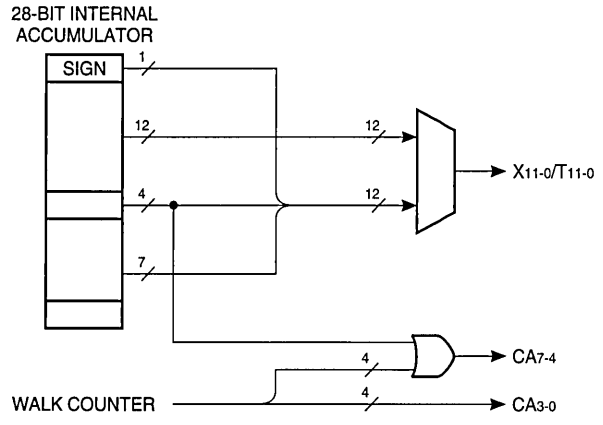


FIGURE 3. ADDRESS TRANSFORMATION EQUATIONS

$$x = x_0 + \left(\frac{dx}{du}\right)m + \left(\frac{dx}{dv}\right)n + \left(\frac{d^2x}{dudv}\right)mn + \left(\frac{d^2x}{du^2}\right)\left(\frac{m^2-m}{2}\right) + \left(\frac{d^2x}{dv^2}\right)\left(\frac{n^2-n}{2}\right)$$
$$+ FOV \cdot CAX(w) + FOV \cdot m \cdot CAX(ker)$$

$$y = y_0 + \left(\frac{dy}{du}\right)m + \left(\frac{dy}{dv}\right)n + \left(\frac{d^2y}{dudv}\right)mn + \left(\frac{d^2y}{du^2}\right)\left(\frac{m^2-m}{2}\right) + \left(\frac{d^2y}{dv^2}\right)\left(\frac{n^2-n}{2}\right)$$
$$+ FOV \cdot CAY(w) + FOV \cdot m \cdot CAY(ker)$$

$$u = UMIN + m$$

$$v = VMIN + n$$

NOTE: $\left(\frac{m^2-m}{2}\right)$ APPROXIMATES THE EXPONENTIAL CHARACTERISTIC OF m^2.

Transformation Parameter Register Loading

The LF2301 allows Transformation Parameters to be updated on-the-fly. The loading of these registers is double-buffered (see Figure 4). Any or all of the first level registers can be loaded using P11-0, B3-0, and $\overline{WEN}$ without affecting the parameters currently in use.

LDR simultaneously updates all Transformation Parameter Registers. If Autoload (ALR) is active, these registers will be updated automatically at the beginning of each new image. Note that $\overline{NOOP}$ does not affect the loading of the Transformation Parameter Registers.

FIGURE 4. LDR CONTROL FOR PARAMETER UPDATE

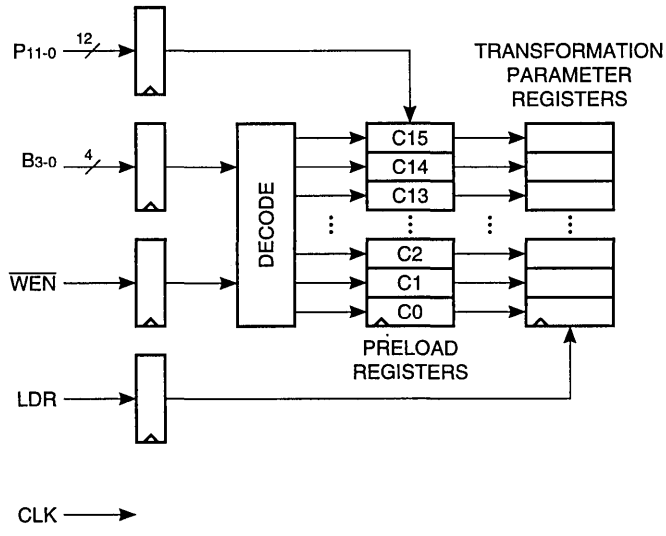


TABLE 4. PARAMETER REGISTER FORMATS (ROW OR COLUMN MODE)

ADDR	MSB				FORMAT							LSB	ROW	COLUMN
0000	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	XMIN	YMIN
0001	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	XMAX	YMAX
0010	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	x_0 (LS)	y_0 (LS)
0011	ALR	AIN	PIPE	R/C	M_1	M_0	-2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	Controls, x_0 (MS)	Controls, y_0 (LS)
0100	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	dx/du (LS)	dy/du (LS)
0101	TM	F_2	F_1	F_0	-2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	Controls, dx/du (MS)	Controls, dy/du (MS)
0110	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	dx/dv (LS)	dy/dv (LS)
0111	K_3	K_2	K_1	K_0	-2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	Kernel, dx/dv (MS)	Kernel, dy/dv (MS)
1000	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	$d^2x/dudv$ (LS)	$d^2y/dudv$ (LS)
1001	-2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	$d^2x/dudv$ (MS)	$d^2y/dudv$ (MS)
1010	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	d^2x/du^2 (LS)	d^2y/du^2 (LS)
1011	-2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	d^2x/du^2 (MS)	d^2y/du^2 (MS)
1100	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	d^2x/dv^2 (LS)	d^2y/dv^2 (LS)
1101	-2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	d^2x/dv^2 (MS)	d^2y/dv^2 (MS)
1110	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	UMIN	VMIN
1111	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	UMAX	VMAX

Static Filter

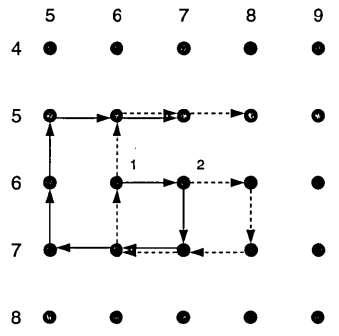
Static filtering at real-time video rates can be performed as shown in Figure 5. This mode is selected by loading M1-0 with "00" for a clockwise spiral walk. A counterclockwise spiral walk could be selected by loading M1-0 with "10." In this example, a static filter with a kernel size of 3 x 3 pixels is desired. Loading K3-0 with "0010" selects a kernel size of 3 x 3. The first pixel selected is determined by x_0 and y_0. In this example, the first pixel is (6,6). In this case, the LF2301s should address consecutive pixels during each spiral walk. For this to occur, FOV must be set to 1 (F2-0 loaded with "001").

After the last pixel of a spiral walk has been selected, the next pixel address is determined by adding dx/du to the current X address and by adding dy/du to the current Y address (unless the kernel just completed was the last for that line). At the end of the first spiral walk, pixel (7,5) is addressed. Since the first pixel of the next spiral walk should be (7,6), dx/du is selected to be 0 and dy/du is selected to be 1.

After the last pixel of the last spiral walk on the first line has been selected, the first pixel address of the second line is determined by adding dx/dv to x_0 and by adding dy/dv to y_0. Since the first pixel of the first spiral walk on the second line should be (6,7), dx/dv is selected to be 0 and dy/dv is selected to be 1. Second order differential terms are not used in this filter and are therefore set to 0.

UMIN and VMIN are both selected to be 6. UMAX and VMAX are both selected to be 7. Table 5 shows the values loaded into all Parameter Registers. Table 6 shows the ITS outputs for the 3 x 3 static filter.

FIGURE 5. 3 × 3 STATIC FILTER



1 = 1st pixel of 1st spiral walk,
2 = 1st pixel of 2nd spiral walk, etc.

TABLE 5. PARAMETER REGISTERS

ADDR	Row (HEX)	Column (HEX)
0000	000	000
0001	FFF	FFF
0010	0C0	0C0
0011	000	100
0100	000	000
0101	100	101
0110	000	000
0111	200	201
1000	000	000
1001	000	000
1010	000	000
1011	000	000
1100	000	000
1101	000	000
1110	006	006
1111	007	007

2

TABLE 6. ITS OUTPUTS FOR 3 × 3 STATIC FILTER

Cycle	x	y	CA_x (HEX)	CA_y (HEX)	u	v	INIT	$\overline{ACC}$	$\overline{UWRI}$	END_x	END_y	DONE
1	6	6	00	00	x	x	1	0	1	0	0	0
2	6	6	00	00	x	x	0	0	1	0	0	0
3	6	6	00	00	x	x	0	0	1	0	0	0
4	6	6	00	00	x	x	0	0	1	0	0	0
5	7	6	01	01	x	x	0	1	0	0	0	0
6	7	7	02	02	x	x	0	1	1	0	0	0
7	6	7	03	03	x	x	0	1	1	0	0	0
8	5	7	04	04	x	x	0	1	1	0	0	0
9	5	6	05	05	x	x	0	1	1	0	0	0
10	5	5	06	06	x	x	0	1	1	0	0	0
11	6	5	07	07	x	x	0	1	1	1	0	0
12	7	5	08	08	x	x	0	1	1	1	0	0
13	7	6	00	00	6	6	0	0	1	1	0	0
14	8	6	01	01	6	6	0	1	0	1	0	0
15	8	7	02	02	6	6	0	1	1	1	0	0
16	7	7	03	03	6	6	0	1	1	1	0	0
17	6	7	04	04	6	6	0	1	1	1	0	0
18	6	6	05	05	6	6	0	1	1	1	0	0
19	6	5	06	06	6	6	0	1	1	1	0	0
20	7	5	07	07	6	6	0	1	1	0	0	0
21	8	5	08	08	6	6	0	1	1	0	0	0
22	8	6	00	00	7	6	0	0	1	0	0	0
23	9	6	01	01	7	6	0	1	0	0	0	0
24	9	7	02	02	7	6	0	1	1	0	0	0
25	8	7	03	03	7	6	0	1	1	0	0	0
26	7	7	04	04	7	6	0	1	1	0	0	0
27	7	6	05	05	7	6	0	1	1	0	0	0
28	7	5	06	06	7	6	0	1	1	0	0	0
29	8	5	07	07	7	6	0	1	1	0	1	0
30	9	5	08	08	7	6	0	1	1	0	1	0
31	6	7	00	00	8	6	0	0	1	0	1	0
32	7	7	01	01	8	6	0	1	0	0	1	0
33	7	8	02	02	8	6	0	1	1	0	1	0
34	6	8	03	03	8	6	0	1	1	0	1	0
35	5	8	04	04	8	6	0	1	1	0	1	0
36	5	7	05	05	8	6	0	1	1	0	1	0
37	5	6	06	06	8	6	0	1	1	0	1	0
38	6	6	07	07	8	6	0	1	1	1	1	0
39	7	6	08	08	8	6	0	1	1	1	1	0
40	7	7	00	00	6	7	0	0	1	1	1	0
41	8	7	01	01	6	7	0	1	0	1	1	0
42	8	8	02	02	6	7	0	1	1	1	1	0
43	7	8	03	03	6	7	0	1	1	1	1	0
44	6	8	04	04	6	7	0	1	1	1	1	0
45	6	7	05	05	6	7	0	1	1	1	1	0
46	6	6	06	06	6	7	0	1	1	1	1	0
47	7	6	07	07	6	7	0	1	1	0	1	0
48	8	6	08	08	6	7	0	1	1	0	1	0
49	8	7	00	00	7	7	0	0	1	0	1	0
50	9	7	01	01	7	7	0	1	0	0	1	0
51	9	8	02	02	7	7	0	1	1	0	1	0
52	8	8	03	03	7	7	0	1	1	0	1	0
53	7	8	04	04	7	7	0	1	1	0	1	0
54	7	7	05	05	7	7	0	1	1	0	1	0
55	7	6	06	06	7	7	0	1	1	0	1	0
56	8	6	07	07	7	7	0	1	1	0	0	1
57	9	6	08	08	7	7	0	1	1	0	0	1
58	6	6	00	00	8	7	0	0	1	0	0	1

Image Rotation & Bilinear Interpolation

Figure 8 shows an example of rotating an image 30º and using bilinear interpolation. This mode is selected by loading M1-0 with "00" for a clockwise spiral walk. A counterclockwise spiral walk could be selected by loading M1-0 with "10." Bilinear interpolation requires a kernel size of 2 x 2 pixels. Loading K3-0 with "0001" selects a kernel size of 2 x 2. The first pixel selected is determined by x_0 and y_0. In this example, the first pixel is (0,0). In this case, the LF2301s should address consecutive pixels during each spiral walk. For this to occur, FOV must be set to 1 (F2-0 loaded with "001").

After the last pixel of a spiral walk has been selected, the next pixel address is determined by adding dx/du to the current X address and by adding dy/du to the current Y address (unless the kernel just completed was the last for that line). At the end of the first spiral walk, pixel (0,1) is addressed. Since the next calculated pixel should be (0.866,0.5), dx/du is selected to be 0.866 and dy/du is selected to be 0.5. However, after adding dx/du and dy/du to the X and Y addresses respectively, the generated address is (0.866,1.5). The Y address is off by a value of 1. This is due to the fact that the last pixel address of a spiral walk is used to calculate the first pixel address of the next spiral walk. In order for the LF2301s to generate the correct result, dy/du must be modified by subtracting a 1 from it. The correct value of dy/du is -0.5. Figure 6 shows how the unmodified differential terms were calculated.

After the last pixel of the last spiral walk on the first line has been selected, the first pixel address of the second line is determined by adding dx/dv to x_0 and by adding dy/dv to y_0. Since the first calculated pixel of the first spiral walk on the second line should be (-0.5,0.866), dx/dv is selected to be -0.5 and dy/dv is selected to be 0.866. Second order differential terms are not used in this transform and are therefore set to 0.

It is important to note that the integer portion of the address generated in the LF2301 is used as the X or Y pixel address. The fractional portion (sub-pixel portion) is used as the coefficient RAM address.

UMIN and VMIN are both selected to be 0. UMAX and VMAX are both selected to be 2. Table 7 shows the values loaded into all Parameter Registers. Table 8 shows the ITS outputs for this example.

Figure 6. Differential Terms

$$\frac{dx}{du} = \cos 30^\circ = 0.866$$

$$\frac{dy}{du} = \sin 30^\circ = 0.5$$

$$\frac{dx}{dv} = -\sin 30^\circ = -0.5$$

$$\frac{dy}{dv} = \cos 30^\circ = 0.866$$

Figure 7. 30° Image Rotation

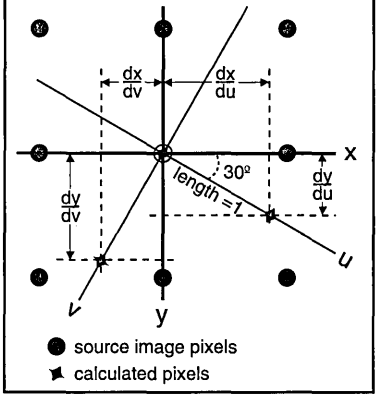


Figure 8. 30° Image Rotation

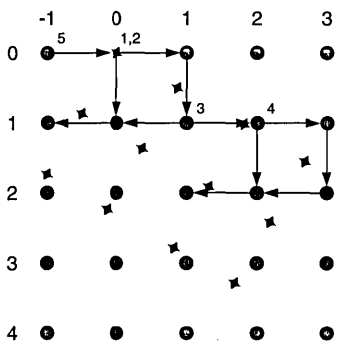


Table 7. Parameter Registers

ADDR	Row (HEX)	Column (HEX)
0000	000	000
0001	FFF	FFF
0010	000	000
0011	000	100
0100	DDB	800
0101	100	1FF
0110	800	DDB
0111	1FF	100
1000	000	000
1001	000	000
1010	000	000
1011	000	000
1100	000	000
1101	000	000
1110	000	000
1111	002	002

2

TABLE 8. ITS OUTPUTS FOR 30° IMAGE ROTATION WITH BILINEAR INTERPOLATION

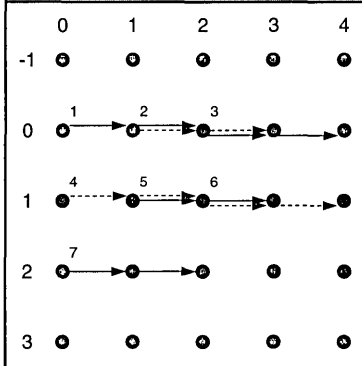
Cycle	x	y	CA_X (HEX)	CA_Y (HEX)	u	v	INIT	$\overline{ACC}$	$\overline{UWRI}$	END_X	END_Y	DONE
1	0	0	00	00	x	x	1	0	1	0	0	0
2	0	0	00	00	x	x	0	0	1	0	0	0
3	0	0	00	00	x	x	0	0	1	0	0	0
4	0	0	00	00	x	x	0	0	1	0	0	0
5	1	0	01	01	x	x	0	1	0	0	0	0
6	1	1	02	02	x	x	0	1	1	0	0	0
7	0	1	03	03	x	x	0	1	1	0	0	0
8	0	0	D0	80	0	0	0	0	1	0	0	0
9	1	0	D1	81	0	0	0	1	0	0	0	0
10	1	1	D2	82	0	0	0	1	1	1	0	0
11	0	1	D3	83	0	0	0	1	1	1	0	0
12	1	1	B0	00	1	0	0	0	1	1	0	0
13	2	1	B1	01	1	0	0	1	0	1	0	0
14	2	2	B2	02	1	0	0	1	1	0	0	0
15	1	2	B3	03	1	0	0	1	1	0	0	0
16	2	1	90	80	2	0	0	0	1	0	0	0
17	3	1	91	81	2	0	0	1	0	0	0	0
18	3	2	92	82	2	0	0	1	1	0	0	0
19	2	2	93	83	2	0	0	1	1	0	0	0
20	-1	0	80	D0	3	0	0	0	1	0	0	0
21	0	0	81	D1	3	0	0	1	0	0	0	0
22	0	1	82	D2	3	0	0	1	1	0	0	0
23	-1	1	83	D3	3	0	0	1	1	0	0	0
24	0	1	50	50	0	1	0	0	1	0	0	0
25	1	1	51	51	0	1	0	1	0	0	0	0
26	1	2	52	52	0	1	0	1	1	1	0	0
27	0	2	53	53	0	1	0	1	1	1	0	0
28	1	1	30	D0	1	1	0	0	1	1	0	0
29	2	1	31	D1	1	1	0	1	0	1	0	0
30	2	2	32	D2	1	1	0	1	1	0	0	0
31	1	2	33	D3	1	1	0	1	1	0	0	0
32	2	2	10	50	2	1	0	0	1	0	0	0
33	3	2	11	51	2	1	0	1	0	0	0	0
34	3	3	12	52	2	1	0	1	1	0	1	0
35	2	3	13	53	2	1	0	1	1	0	1	0
36	-1	1	00	B0	3	1	0	0	1	0	1	0
37	0	1	01	B1	3	1	0	1	0	0	1	0
38	0	2	02	B2	3	1	0	1	1	0	1	0
39	-1	2	03	B3	3	1	0	1	1	0	1	0
40	-1	2	D0	30	0	2	0	0	1	0	1	0
41	0	2	D1	31	0	2	0	1	0	0	1	0
42	0	3	D2	32	0	2	0	1	1	1	1	0
43	-1	3	D3	33	0	2	0	1	1	1	1	0
44	0	2	B0	B0	1	2	0	0	1	1	1	0
45	1	2	B1	B1	1	2	0	1	0	1	1	0
46	1	3	B2	B2	1	2	0	1	1	0	1	0
47	0	3	B3	B3	1	2	0	1	1	0	1	0
48	1	3	90	30	2	2	0	0	1	0	1	0
49	2	3	91	31	2	2	0	1	0	0	1	0
50	2	4	92	32	2	2	0	1	1	0	0	1
51	1	4	93	33	2	2	0	1	1	0	0	1
52	0	0	00	00	3	2	0	0	1	0	0	1
53	1	0	01	01	3	2	0	1	0	0	0	1
54	1	1	02	02	3	2	0	1	1	0	0	1
55	0	1	03	03	3	2	0	1	1	0	0	1

Pass 1 of Two-Pass Operation

Pass 1 of the two-pass operation performs horizontal filtering on an image as shown in Figure 9. This mode is selected by loading M_{1-0} with "01." In this example, a horizontal filter with a kernel size of 3 pixels is desired. Loading K_{3-0} with "0010" selects a kernel size of 3. The first pixel selected is determined by x_0 and y_0. In this example, the first pixel is (0,0). In this case, the LF2301s should address consecutive pixels during each pixel walk. For this to occur, FOV must be set to 1 (F_{2-0} loaded with "001").

After the last pixel of a pixel walk has been selected, the next pixel address is determined by adding dx/du to the current X address and by adding dy/du to the current Y address (unless the kernel just completed was the last for that line). At the end of the first pixel walk, pixel (2,0) is addressed. Since the first pixel of the next pixel walk should be (1,0), dx/du is selected to be -1 and dy/du is selected to be 0. After the last pixel of the last pixel walk on the first line has been selected, the first pixel address of the second line is determined by adding dx/dv to x_0 and by adding dy/dv to y_0. Since the first pixel of the first pixel walk on the second line should be (0,1), dx/dv is selected to be 0 and dy/dv is selected to be 1. Second order differential terms are not used in this filter and are therefore set to 0.

FIGURE 9. PASS 1 OF TWO-PASS



1 = 1st pixel of 1st walk,
2 = 1st pixel of 2nd walk, etc.

TABLE 9. PARAMETER REGISTERS

ADDR	Row (HEX)	Column (HEX)
0000	000	000
0001	FFF	FFF
0010	000	000
0011	040	140
0100	000	000
0101	1FF	000
0110	000	000
0111	200	201
1000	000	000
1001	000	000
1010	000	000
1011	000	000
1100	000	000
1101	000	000
1110	005	005
1111	006	006

UMIN and VMIN are both selected to be 5. UMAX and VMAX are both selected to be 6. Table 9 shows the values loaded into all Parameter Registers. Table 10 shows the ITS outputs for the Pass 1 of a Two-Pass operation.

TABLE 10. ITS OUTPUTS FOR PASS 1 OF TWO-PASS

Cycle	x	y	CA_X (HEX)	CA_Y (HEX)	u	v	INIT	$\overline{ACC}$	$\overline{UWRI}$	END_X	END_Y	DONE
1	0	0	00	00	x	x	1	0	1	0	0	0
2	0	0	00	00	x	x	0	0	1	0	0	0
3	0	0	00	00	x	x	0	0	1	0	0	0
4	0	0	00	00	x	x	0	0	1	0	0	0
5	1	0	01	01	x	x	0	1	0	1	0	0
6	2	0	02	02	x	x	0	1	1	1	0	0
7	1	0	00	00	5	5	0	0	1	1	0	0
8	2	0	01	01	5	5	0	1	0	0	0	0
9	3	0	02	02	5	5	0	1	1	0	0	0
10	2	0	00	00	6	5	0	0	1	0	0	0
11	3	0	01	01	6	5	0	1	0	0	1	0
12	4	0	02	02	6	5	0	1	1	0	1	0
13	0	1	00	00	7	5	0	0	1	0	1	0
14	1	1	01	01	7	5	0	1	0	1	1	0
15	2	1	02	02	7	5	0	1	1	1	1	0
16	1	1	00	00	5	6	0	0	1	1	1	0
17	2	1	01	01	5	6	0	1	0	0	1	0
18	3	1	02	02	5	6	0	1	1	0	1	0
19	2	1	00	00	6	6	0	0	1	0	1	0
20	3	1	01	01	6	6	0	1	0	0	0	1
21	4	1	02	02	6	6	0	1	1	0	0	1
22	0	0	00	00	7	6	0	0	1	0	0	1
23	1	0	01	01	7	6	0	1	0	1	0	1
24	2	0	02	02	7	6	0	1	1	1	0	1

Pass 2 of Two-Pass Operation

Pass 2 of the two-pass operation performs vertical filtering on an image as shown in Figure 10. This mode is selected by loading M_{1-0} with "11." In this example, a vertical filter with a kernel size of 3 pixels is desired. Loading K_{3-0} with "0010" selects a kernel size of 3. The first pixel selected is determined by x_0 and y_0. In this example, the first pixel is (0,0). In this case, the LF2301s should address consecutive pixels during each pixel walk. For this to occur, FOV must be set to 1 (F_{2-0} loaded with "001").

After the last pixel of a pixel walk has been selected, the next pixel address is determined by adding dx/du to the current X address and by adding dy/du to the current Y address (unless the kernel just completed was the last for that line). At the end of the first pixel walk, pixel (0,2) is addressed. Since the first pixel of the next pixel walk should be (1,0), dx/du is selected to be 1 and dy/du is selected to be -2. After the last pixel of the last pixel walk on the first line has been selected, the first pixel address of the second line is determined by adding dx/dv to x_0 and by adding dy/dv to y_0. Since the first pixel of the first pixel walk on the second line should be (0,1), dx/dv is selected to be 0 and dy/dv is selected to be 1. Second order differential terms are not used in this filter and are therefore set to 0.

Figure 10. Pass 2 Of Two-Pass

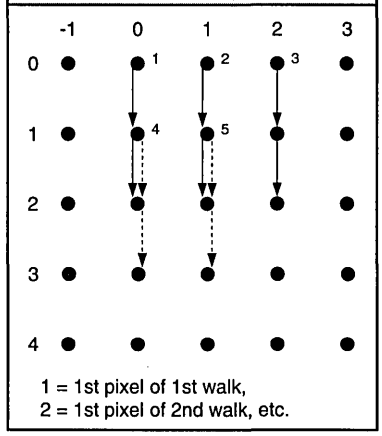


Table 11. Parameter Registers

ADDR	Row (HEX)	Column (HEX)
0000	000	000
0001	FFF	FFF
0010	000	000
0011	0C0	1C0
0100	000	000
0101	101	1FE
0110	000	000
0111	200	201
1000	000	000
1001	000	000
1010	000	000
1011	000	000
1100	000	000
1101	000	000
1110	005	005
1111	006	006

UMIN and VMIN are both selected to be 5. UMAX and VMAX are both selected to be 6. Table 11 shows the values loaded into all Parameter Registers. Table 12 shows the ITS outputs for the Pass 2 of a Two-Pass operation.

Table 12. ITS Outputs For Pass 2 Of Two-Pass

Cycle	x	y	CA_x (HEX)	CA_y (HEX)	u	v	INIT	$\overline{ACC}$	$\overline{UWRI}$	END_x	END_y	DONE
1	0	0	00	00	x	x	1	0	1	0	0	0
2	0	0	00	00	x	x	0	0	1	0	0	0
3	0	0	00	00	x	x	0	0	1	0	0	0
4	0	0	00	00	x	x	0	0	1	0	0	0
5	0	1	01	01	x	x	0	1	0	1	0	0
6	0	2	02	02	x	x	0	1	1	1	0	0
7	1	0	00	00	5	5	0	0	1	1	0	0
8	1	1	01	01	5	5	0	1	0	0	0	0
9	1	2	02	02	5	5	0	1	1	0	0	0
10	2	0	00	00	6	5	0	0	1	0	0	0
11	2	1	01	01	6	5	0	1	0	0	1	0
12	2	2	02	02	6	5	0	1	1	0	1	0
13	0	1	00	00	7	5	0	0	1	0	1	0
14	0	2	01	01	7	5	0	1	0	1	1	0
15	0	3	02	02	7	5	0	1	1	1	1	0
16	1	1	00	00	5	6	0	0	1	1	1	0
17	1	2	01	01	5	6	0	1	0	0	1	0
18	1	3	02	02	5	6	0	1	1	0	1	0
19	2	1	00	00	6	6	0	0	1	0	1	0
20	2	2	01	01	6	6	0	1	0	0	0	1
21	2	3	02	02	6	6	0	1	1	0	0	1
22	0	0	00	00	7	6	0	0	1	0	0	1
23	0	1	01	01	7	6	0	1	0	1	0	1
24	0	2	02	02	7	6	0	1	1	1	0	1

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	−0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			75	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			5	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

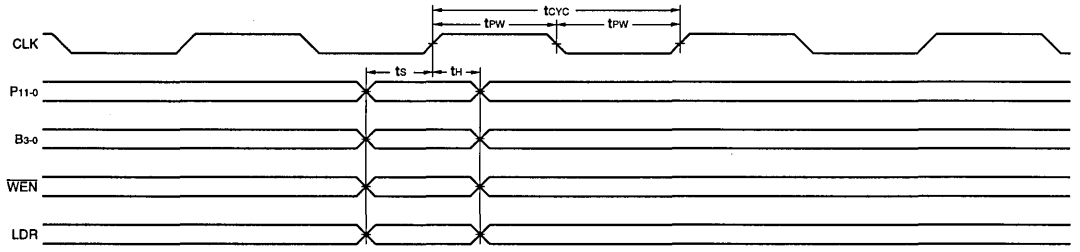
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF2301–					
		66		55		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	66		55		25	
t_{PW}	Clock Pulse Width	30		25		10	
t_S	Input Setup Time	20		18		10	
t_H	Input Hold Time	2		2		0	
t_{HI}	Input Hold Time, INTER	10		10		5	
t_D	Output Delay		35		27		15
t_{DE}	Output Delay, END		45		37		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		35		27		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		18		15

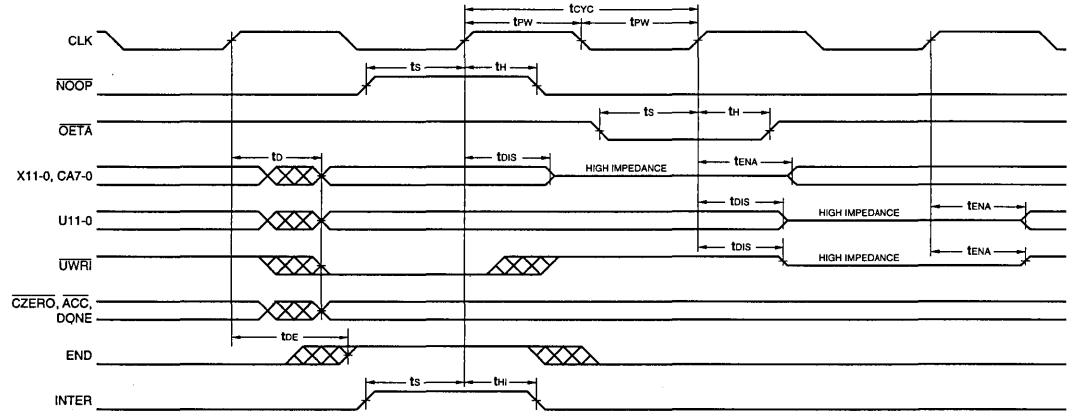
MILITARY OPERATING RANGE (-55°C to +125°C) *Notes 9, 10 (ns)*

		LF2301–					
		66		55		30	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	66		55		30	
t_{PW}	Clock Pulse Width	30		25		10	
t_S	Input Setup Time	20		18		12	
t_H	Input Hold Time	2		2		0	
t_{HI}	Input Hold Time, INTER	10		10		6	
t_D	Output Delay		35		27		18
t_{DE}	Output Delay, END		45		37		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		35		27		18
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		18		18

Switching Waveforms: Data Inputs (Parameter Storage)



Switching Waveforms: Data Outputs and Control Lines



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with no output load at 15 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

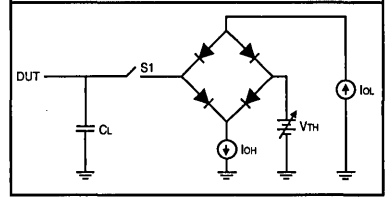
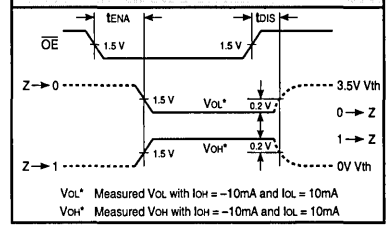
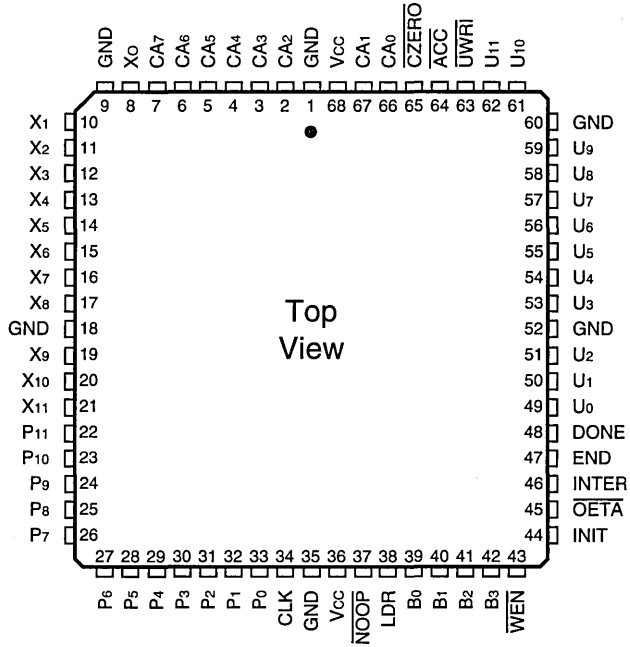


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

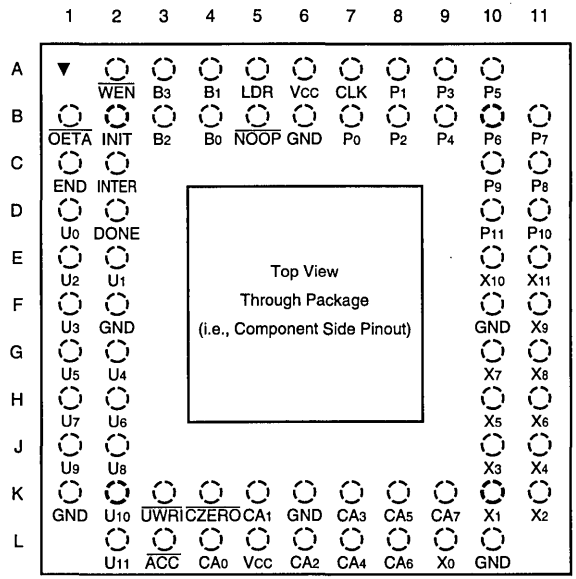
68-pin



Speed	Plastic J-Lead Chip Carrier (J2)
0°C to +70°C—COMMERCIAL SCREENING	
66 ns	LF2301JC66
55 ns	LF2301JC55
25 ns	LF2301JC25

ORDERING INFORMATION

68-pin



Speed	Ceramic Pin Grid Array (G1)
	0°C to +70°C—COMMERCIAL SCREENING
66 ns	LF2301GC66
55 ns	LF2301GC55
25 ns	LF2301GC25
	–55°C to +125°C—COMMERCIAL SCREENING
66 ns	LF2301GM66
55 ns	LF2301GM55
30 ns	LF2301GM30
	–55°C to +125°C—MIL-STD-883 COMPLIANT
66 ns	LF2301GMB66
55 ns	LF2301GMB55
30 ns	LF2301GMB30

LF3310
Horizontal / Vertical Digital Image Filter

FEATURES

- 80 MHz Data Rate
- 12-bit Data and Coefficients
- On-board Memory for 256 Horizontal and Vertical Coefficient Sets
- LF Interface™ Allows All 512 Coefficient Sets to be Updated Within Vertical Blanking
- Selectable 12-bit Data Output with User-Defined Rounding and Limiting
- Seven 3K x 12-bit, Programmable Two-Mode Line Buffers
- 16 Horizontal Filter Taps
- 8 Vertical Filter Taps
- Two Operating Modes: Dimensionally Separate and Orthogonal
- Supports Interleaved Data Streams
- Horizontal Filter Supports Decimation up to 16:1 for Increasing Number of Filter Taps
- 3.3 Volt Power Supply
- 5 Volt I/O Tolerant
- Available 100% Screened to MIL-STD-883, Class B

DESCRIPTION

The **LF3310** is a two-dimensional digital image filter capable of filtering data at real-time video rates. The device contains both a horizontal and a vertical filter which may be cascaded or used concurrently for two-dimensional filtering. The input, coefficient, and output data are all 12 bits and in two's complement format.

The horizontal filter is designed to take advantage of symmetric coefficient sets. When symmetric coefficient sets are used, the horizontal filter can be configured as a 16-tap FIR filter. When asymmetric coefficient sets are used, it can be configured as an 8-tap FIR filter. The vertical filter is an 8-tap FIR filter with all required line buffers contained on-chip. The line buffers can store video lines with lengths from 4 to 3076 pixels.

Horizontal filter Interleave/Decimation Registers (I/D Registers) and the vertical filter line buffers allow interleaved data to be fed directly into the device and filtered without separating the data into individual data streams. The horizontal filter can handle a maximum of sixteen data sets interleaved together. The vertical filter can handle interleaved video lines which contain 3076 or less data values. The I/D Registers and horizontal accumulator facilitate using decimation to increase the number of filter taps in the horizontal filter. Decimation of up to 16:1 is supported.

The device has on-chip storage for 256 horizontal coefficient sets and 256 vertical coefficient sets. Each filter's coefficients are loaded independently of each other allowing one filter's coefficients to be updated without affecting the other filter's coefficients. In addition, a horizontal or vertical coefficient set can be updated independently from the other coefficient sets in the same filter.

LF3310 BLOCK DIAGRAM

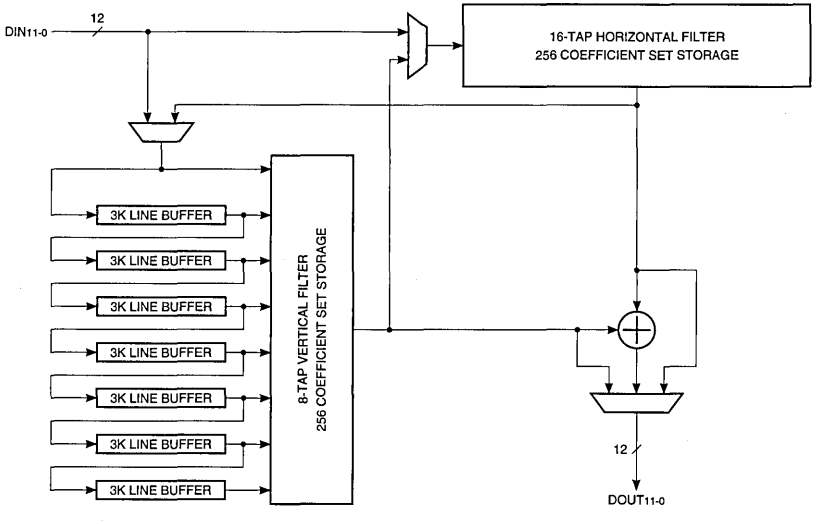
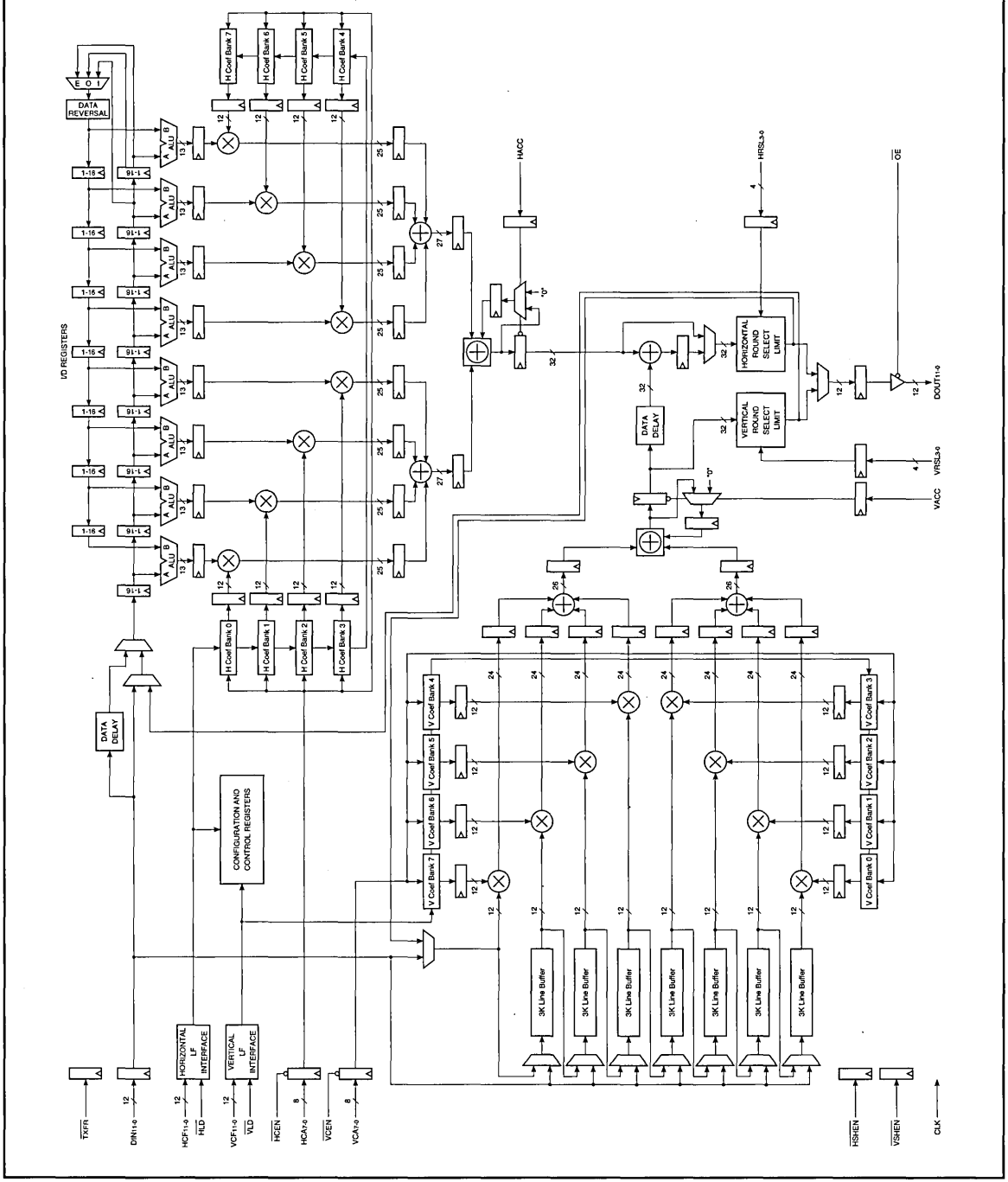


FIGURE 1. LF3310 FUNCTIONAL BLOCK DIAGRAM



SIGNAL DEFINITIONS

Power

VCC and GND

+3.3 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers.

Inputs

DIN11-0 — Data Input

DIN11-0 is the 12-bit registered data input port. Data is latched on the rising edge of CLK.

HCF11-0 — Horizontal Coefficient Input

HCF11-0 is used to load data into the horizontal coefficient banks and the configuration/control registers. Data present on HCF11-0 is latched into the Horizontal LF Interface™ on the rising edge of CLK when HLD is LOW (see the LF Interface™ section for a full discussion).

HCA7-0 — Horizontal Coefficient Address

HCA7-0 determines which row of data in the horizontal coefficient banks is fed to the multipliers in the horizontal filter. HCA7-0 is latched into the Horizontal Coefficient Address Register on the rising edge of CLK when HCEN is LOW.

VCF11-0 — Vertical Coefficient Input

VCF11-0 is used to load data into the vertical coefficient banks and the configuration/control registers. Data present on VCF11-0 is latched into the Vertical LF Interface™ on the rising edge of CLK when VLD is LOW (see the LF Interface™ section for a full discussion).

FIGURE 2. INPUT FORMATS

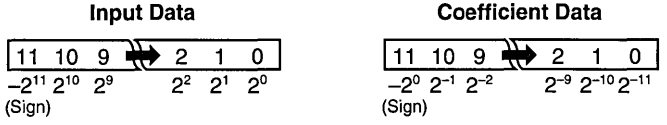


FIGURE 3. HORIZONTAL AND VERTICAL ACCUMULATOR FORMATS

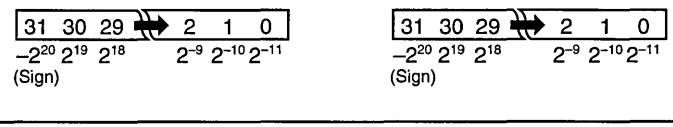


TABLE 1. OUTPUT FORMATS

SLCT4-0	S_{11}	S_{10}	S_9	• • •	S_6	S_5	• • •	S_2	S_1	S_0
00000	F_{11}	F_{10}	F_9	• • •	F_6	F_5	• • •	F_2	F_1	F_0
00001	F_{12}	F_{11}	F_{10}	• • •	F_7	F_6	• • •	F_3	F_2	F_1
00010	F_{13}	F_{12}	F_{11}	• • •	F_8	F_7	• • •	F_4	F_3	F_2
•	•	•	•		•	•		•	•	•
•	•	•	•		•	•		•	•	•
•	•	•	•		•	•		•	•	•
10010	F_{29}	F_{28}	F_{27}	• • •	F_{24}	F_{23}	• • •	F_{20}	F_{19}	F_{18}
10011	F_{30}	F_{29}	F_{28}	• • •	F_{25}	F_{24}	• • •	F_{21}	F_{20}	F_{19}
10100	F_{31}	F_{30}	F_{29}	• • •	F_{26}	F_{25}	• • •	F_{22}	F_{21}	F_{20}

VCA7-0 — Vertical Coefficient Address

VCA7-0 determines which row of data in the vertical coefficient banks is fed to the multipliers in the vertical filter. VCA7-0 is latched into the Vertical Coefficient Address Register on the rising edge of CLK when VCEN is LOW.

Outputs

DOUT11-0 — Data Output

DOUT11-0 is the 12-bit registered data output port.

Controls

$\overline{HLD}$ — Horizontal Coefficient Load

When $\overline{HLD}$ is LOW, data on HCF11-0 is latched into the Horizontal LF Interface™ on the rising edge of CLK. When $\overline{HLD}$ is HIGH, data can not be latched into the Horizontal LF Interface™. When enabling the LF Interface™ for data input, a HIGH to LOW transition of $\overline{HLD}$ is required in order for the input circuitry to function properly. Therefore, $\overline{HLD}$ must be set HIGH immediately after power up to ensure proper operation of the input circuitry (see the LF Interface™ section for a full discussion).

$\overline{HCEN}$ — Horizontal Coefficient Address Enable

When $\overline{HCEN}$ is LOW, data on HCA7-0 is latched into the Horizontal Coefficient Address Register on the rising edge of CLK. When $\overline{HCEN}$ is HIGH, data on HCA7-0 is not latched and the register's contents will not be changed.

$\overline{VLD}$ — Vertical Coefficient Load

When $\overline{VLD}$ is LOW, data on VCF11-0 is latched into the Vertical LF Interface™ on the rising edge of CLK. When $\overline{VLD}$ is HIGH, data can not be latched into the Vertical LF Interface™. When enabling the LF Interface™ for data input, a HIGH to LOW transition of $\overline{VLD}$ is required in order for the input circuitry to function properly. Therefore, $\overline{VLD}$ must be set HIGH immediately after power up to ensure proper operation of the input circuitry (see the LF Interface™ section for a full discussion).

$\overline{VCEN}$ — Vertical Coefficient Address Enable

When $\overline{VCEN}$ is LOW, data on VCA7-0 is latched into the Vertical Coefficient Address Register on the rising edge of CLK. When $\overline{VCEN}$ is HIGH, data on VCA7-0 is not latched and the register's contents will not be changed.

$\overline{TXFR}$ — Horizontal Filter LIFO Transfer Control

$\overline{TXFR}$ is used to change which LIFO in the data reversal circuitry sends data to the reverse data path and which LIFO receives data from the forward data path. When $\overline{TXFR}$ goes LOW, the LIFO sending data to the reverse data path becomes the LIFO receiving data from the forward data path, and the LIFO receiving data from the forward data path becomes the LIFO sending data to the reverse data path. The device must see a HIGH to LOW transition of $\overline{TXFR}$ in order to switch LIFOs.

HACC — Horizontal Accumulator Control

When HACC is HIGH, the horizontal accumulator is enabled for accumulation and the accumulator output register is disabled for loading. When HACC is LOW, no accumulation is performed and the accumulator output register is enabled for loading. HACC is latched on the rising edge of CLK.

VACC — Vertical Accumulator Control

When VACC is HIGH, the vertical accumulator is enabled for accumulation and the accumulator output register is disabled for loading. When VACC is LOW, no accumulation is performed and the accumulator output register is enabled for loading. VACC is latched on the rising edge of CLK.

$\overline{HSHEN}$ — Horizontal Shift Enable

$\overline{HSHEN}$ enables or disables the loading of data into the forward and reverse I/D Registers in the horizontal filter when the device is in Dimensionally Separate Mode. If the device is configured such that the horizontal filter feeds the vertical filter, $\overline{HSHEN}$ also enables or disables the loading of data into the input register (DIN11-0). If the device is configured such that the vertical filter feeds the horizontal filter and the vertical limit register is under shift control, $\overline{HSHEN}$ also enables or disables the loading of data into the vertical limit register in the vertical round/select/limit circuitry. In Orthogonal Mode, $\overline{HSHEN}$ also enables or disables the loading of data into the input register (DIN11-0) and the line buffers in the vertical filter. It is important to note that in Orthogonal Mode, either $\overline{HSHEN}$ or $\overline{VSHEN}$ can disable data loading. Both must be active to enable data loading in Orthogonal Mode. Also in Orthogonal Mode, the horizontal and vertical limit registers can not be disabled.

When $\overline{HSHEN}$ is LOW, data is loaded into and shifted through the registers $\overline{HSHEN}$ controls and the forward and reverse I/D Registers on the rising edge of CLK. When $\overline{HSHEN}$ is HIGH, data is not loaded into or shifted through the registers $\overline{HSHEN}$ controls and the I/D Registers, and their contents will not be changed. $\overline{HSHEN}$ is latched on the rising edge of CLK.

$\overline{VSHEN}$ — Vertical Shift Enable

$\overline{VSHEN}$ enables or disables the loading of data into the line buffers in the vertical filter when the device is in Dimensionally Separate Mode. If the device is configured such that the vertical filter feeds the horizontal filter, $\overline{VSHEN}$ also enables or disables the loading of data into the input register (DIN11-0). If the device is configured such that the horizontal filter feeds the vertical filter and the horizontal limit register is under shift control, $\overline{VSHEN}$ also enables or disables the loading of data into the horizontal limit register in the horizontal round/select/limit circuitry. In Orthogonal Mode, $\overline{VSHEN}$ also enables or disables the loading of data into the input register (DIN11-0) and the forward and reverse I/D Registers in the horizontal filter. It is important to note that in Orthogonal Mode, either $\overline{HSHEN}$ or $\overline{VSHEN}$ can disable data loading. Both must be active to enable data loading in Orthogonal Mode. Also in Orthogonal Mode, the horizontal and vertical limit registers can not be disabled.

When $\overline{VSHEN}$ is LOW, data is loaded into and shifted through the registers $\overline{VSHEN}$ controls and the line buffers on the rising edge of CLK. When $\overline{VSHEN}$ is HIGH, data is not loaded into or shifted through the registers $\overline{VSHEN}$ controls and the line buffers, and their contents will not be changed. $\overline{VSHEN}$ is latched on the rising edge of CLK.

HRSL3-0 — Horizontal Round/Select/ Limit Control

HRSL3-0 determines which of the sixteen user-programmable round/ select/limit registers are used in the horizontal round/select/limit circuitry. A value of 0 on HRSL3-0 selects round/select/limit register 0. A value of 1 selects round/select/ limit register 1 and so on. HRSL3-0 is latched on the rising edge of CLK (see the horizontal round, select, and limit sections for a complete discussion).

VRSL3-0 — Vertical Round/Select/Limit Control

VRSL3-0 determines which of the sixteen user-programmable round/ select/limit registers are used in the vertical round/select/limit circuitry. A value of 0 on VRSL3-0 selects round/select/limit register 0. A value of 1 selects round/select/limit register 1 and so on. VRSL3-0 is latched on the rising edge of CLK (see the vertical round, select, and limit sections for a complete discussion).

$\overline{OE}$ — Output Enable

When $\overline{OE}$ is LOW, DOUT11-0 is enabled for output. When $\overline{OE}$ is HIGH, DOUT11-0 is placed in a high-impedance state.

OPERATIONAL MODES

Dimensionally Separate

In Dimensionally Separate Mode, the horizontal and vertical filters are cascaded together to form a two-dimensional image filter (see Figures 4 and 5). Bit 1 in Configuration Register 4 determines the cascade order. If this bit is set to "0", data on DIN11-0 is fed into the horizontal filter first. The horizontal filter then feeds data into the vertical filter. If this bit is set to "1", data on DIN11-0 is fed into the vertical filter first. The vertical filter then feeds data into the horizontal filter.

FIGURE 4. DIMENSIONALLY SEPARATE MODE: H TO V

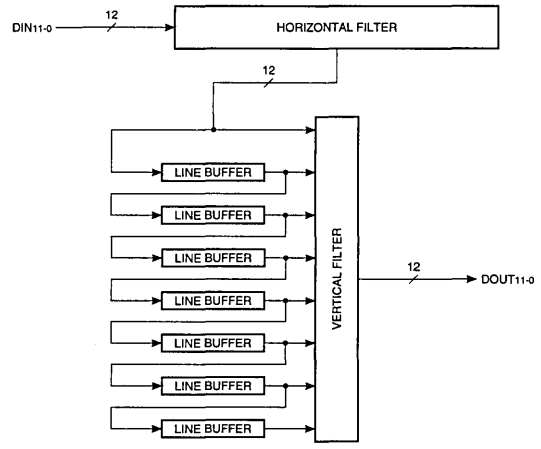
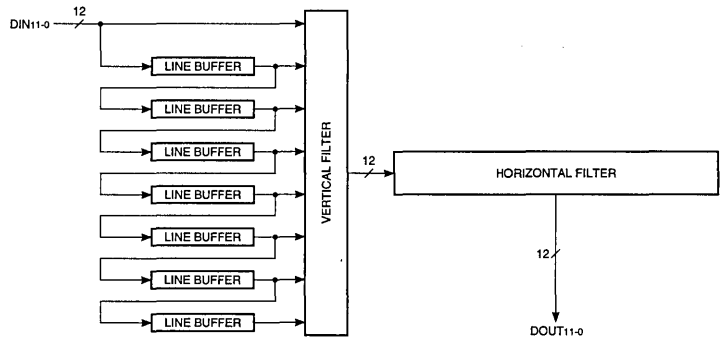


FIGURE 5. DIMENSIONALLY SEPARATE MODE: V TO H



Orthogonal

In Orthogonal Mode, the horizontal and vertical filters are used concurrently to implement an orthogonal kernel on the input data (see Figure 6). The HV Filter can handle kernel sizes of 3-3, 5-5, and 7-7 (see Figure 7). Data delay elements at the input of the horizontal filter and the output of the vertical filter are used to properly align data so that the orthogonal kernel is implemented correctly. The data delays are automatically set to the correct lengths based on the programmed length of the line buffers and the kernel size.

Kernel sizes of 3-3, 5-5, and 7-7 require that the horizontal filter's output be delayed by LB – 2, 2(LB) – 3, and 3(LB) – 4 clock cycles respectively before being added to the vertical filter's output (LB is the programmed line buffer length). The data delay at the input of the horizontal filter handles the LB, 2(LB), and 3(LB) delays. The data delay at the output of the vertical filter handles the – 2, – 3, and – 4 delays. For example, if the line buffers are programmed for a length of 720 and a 5–5 kernel is selected, the

FIGURE 6. ORTHOGONAL MODE

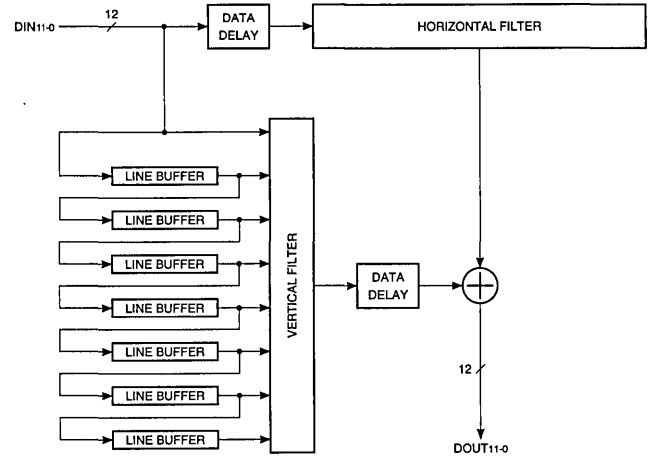
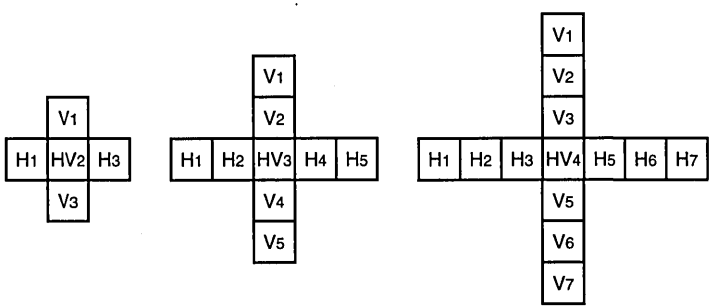


FIGURE 7. 3-3, 5-5, AND 7-7 ORTHOGONAL KERNELS



horizontal filter input data delay will be 1440 clock cycles and the vertical filter output data delay will be 3 clock cycles.

It is important to note that the first 3, 5, or 7 multipliers of the horizontal and vertical filters must be used in Orthogonal Mode. If other multipliers are used, data from the horizontal and vertical filters will not line up correctly because the data delays are calculated assuming that the first 3, 5, or 7 multipliers are used. Also, the ALUs in the horizontal filter should be configured to accept data from the forward I/D Register path into ALU Input A and force ALU Input B to 0.

FUNCTIONAL DESCRIPTION

Horizontal Filter

The horizontal filter is designed to filter a digital image in the horizontal dimension. This FIR filter can be configured to have as many as 16 taps when symmetric coefficient sets are used and 8 taps when asymmetric coefficient sets are used.

ALUs

The ALUs double the number of filter taps available, when symmetric coefficient sets are used, by pre-adding data values which are then multiplied by a common coefficient (see Figure 8). The ALUs can perform two operations: A+B and B–A. Bit 0 of Configuration Register 0 determines the ALU operation. A+B is used with even-symmetric coefficient sets. B–A is used with odd-symmetric coefficient sets. Also, either the A or B operand may be set to 0. Bits 1 and 2 of Configuration Register 0 control the ALU inputs. A+0 or B+0 are used with asymmetric coefficient sets.

Interleave/Decimation Registers

The Interleave/Decimation Registers (I/D Registers) feed the ALU inputs. They allow the device to filter up to sixteen data sets interleaved into the same data stream without having to separate the data sets. The I/D Registers should be set to a length equal to the number of data sets interleaved together. For example, if two data sets are interleaved together, the I/D Registers should be set to a length of two. Bits 1 through 4 of Configuration Register 1 determine the I/D Register length.

The I/D Registers also facilitate using decimation to increase the number of filter taps. Decimation by N is accomplished by reading the horizontal filter's output once every N clock cycles. The device supports decimation up to 16:1. With no decimation, the maximum number of filter taps is sixteen. When decimating by N, the number of filter taps becomes 16N because there are N–1 clock cycles when the horizontal filter's output is not being read. The extra clock cycles are used to calculate more filter taps.

When decimating, the I/D Registers should be set to a length equal to the decimation factor. For example, when performing a 4:1 decimation, the I/D Registers should be set to a length of four. When not decimating or when only one data set (non-interleaved data) is fed into the device, the I/D Registers should be set to a length of one.

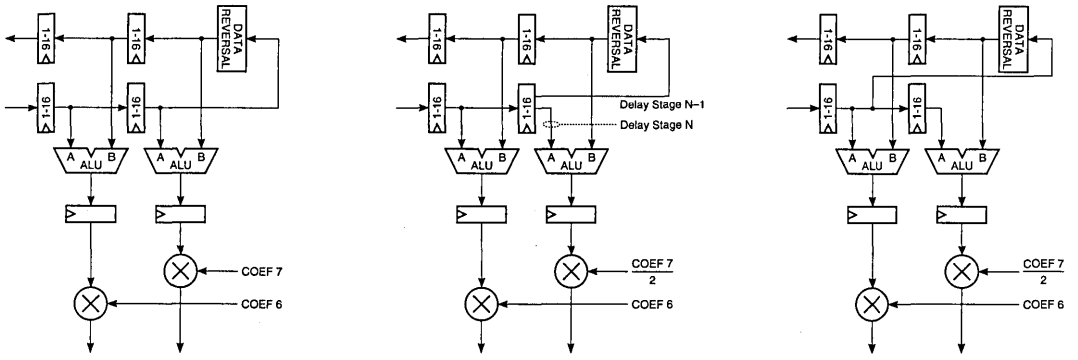
FIGURE 8. SYMMETRIC COEFFICIENT SET EXAMPLES

Even-Tap, Even-Symmetric Coefficient Set

Odd-Tap, Even-Symmetric Coefficient Set

Even-Tap, Odd-Symmetric Coefficient Set

FIGURE 9. I/D REGISTER DATA PATHS



EVEN-TAP MODE

ODD-TAP MODE

ODD-TAP INTERLEAVE MODE

$\overline{\text{HSHEN}}$ enables or disables the loading of data into the forward and reverse I/D Registers when the device is in Dimensionally Separate Mode (see the $\overline{\text{HSHEN}}$ section for a full discussion). When in Orthogonal Mode, $\overline{\text{HSHEN}}$ also enables or disables the loading of data into the input register (DIN_{11-0}) and the line buffers.

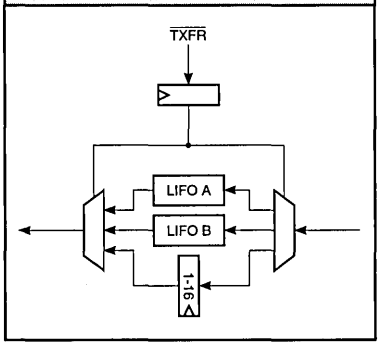
It is important to note that in Orthogonal Mode, either $\overline{\text{HSHEN}}$ or $\overline{\text{VSHEN}}$ can disable the loading of data into the input register (DIN_{11-0}), I/D Registers, and line buffers. Both must be active to enable data loading in Orthogonal Mode.

I/D Register Data Path Control

The multiplexer in the middle of the I/D Register data path controls how data is fed to the reverse data path. The forward data path contains the I/D Registers in which data flows from left to right in the block diagram in Figure 1. The reverse data path contains the I/D Registers in which data flows from right to left. When the filter is configured for an even number of taps, data from the last I/D Register in the forward data path is fed into the first I/D Register in the reverse data path (see Figure 9). When the filter is configured for an odd number of taps, the data which will appear at the output of the last I/D Register in the forward data path on the next clock cycle is fed into the first I/D Register in the reverse data path. Bit 5 in Configuration Register 1 configures the filter for an even or odd number of taps.

When interleaved data is fed through the device and an even tap filter is desired, the filter should be configured for an even number of taps (Bit 5 of CR_1 set to "0") and the I/D Register length should match the number of data sets interleaved together. When interleaved data is to be fed through the device and an odd tap filter is desired, the filter should be set to Odd-Tap Interleave Mode. Bit 0 of Configuration Register 1 configures

FIGURE 10. DATA REVERSAL



the filter for Odd-Tap Interleave Mode. When the filter is configured for Odd-Tap Interleave Mode, data from the next to last I/D Register in the forward data path is fed into the first I/D Register in the reverse data path.

When the filter is configured for an odd number of taps (interleaved or non-interleaved modes), the filter is structured such that the center data value is aligned simultaneously at the A and B inputs of the last ALU in the forward data path. In order to achieve the correct result, the user must divide the coefficient by two.

Data Reversal

Data reversal circuitry is placed after the multiplexer which routes data from the forward data path to the reverse data path (see Figure 10). When decimating, the data stream must be reversed in order for data to be properly aligned at the inputs of the ALUs. When data reversal is enabled, the circuitry uses a pair of LIFOs to reverse the order of the data sent to the reverse data path. When $\overline{TXFR}$ goes LOW, the LIFO sending data to the reverse data path becomes the LIFO receiving data from the forward data path, and the LIFO receiving data from the forward data path becomes the LIFO sending data to the reverse data path. The device must see a HIGH to LOW transition of $\overline{TXFR}$ in order to switch LIFOs. If decimating by N, $\overline{TXFR}$ should go low once every N clock cycles. When data reversal is disabled, the circuitry functions like an I/D Register. When feeding interleaved data through the filter, data reversal should be disabled. Bit 6 of Configuration Register 1 enables or disables data reversal.

Horizontal Rounding

The horizontal filter output may be rounded by adding the contents of one of the sixteen horizontal round registers to the horizontal filter output (see Figure 11). Each round register is 32 bits wide and user-programmable. This allows the filter's output to be rounded to any precision required. Since any 32-bit value may be programmed into the round registers, the device can support complex rounding algorithms as well as standard Half-LSB rounding. HRSL3-0 determines which of the sixteen horizontal round registers are used in the rounding operation. A value of 0 on HRSL3-0 selects horizontal round register 0. A value of 1 selects horizontal round register 1 and so on. HRSL3-0 may be changed every clock cycle if desired. This allows the rounding algorithm to be changed every clock cycle. This is useful when filtering interleaved data. If rounding is not desired, a round register should be loaded with 0 and selected as the register used for rounding. Round register loading is discussed in the LF Interface™ section.

FIGURE 11. HORIZONTAL AND VERTICAL ROUND/SELECT/LIMIT CIRCUITRY

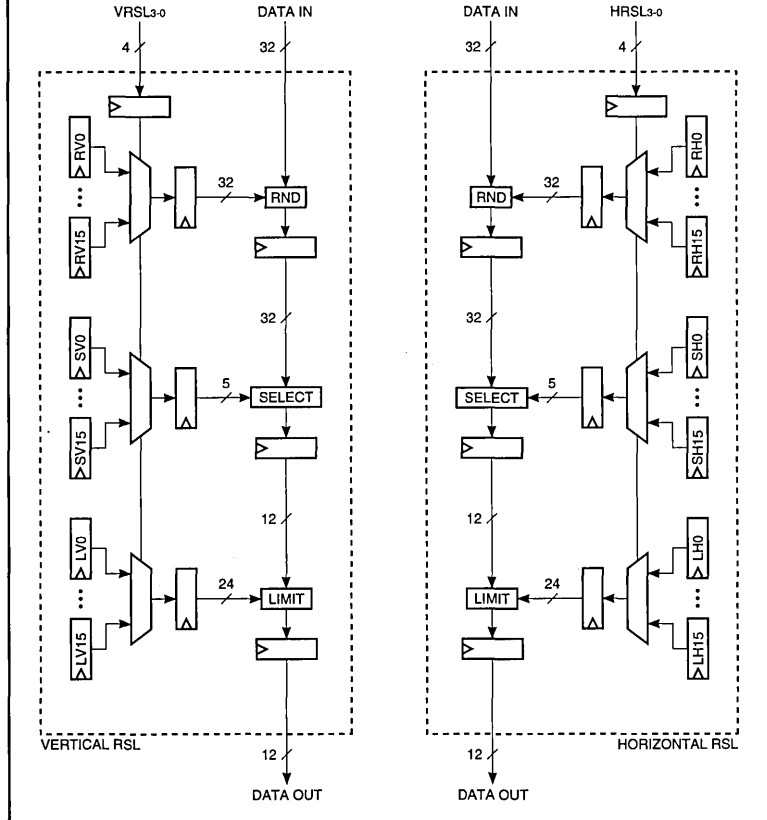


TABLE 2. CONFIGURATION REGISTER 0 – ADDRESS 200H

BITS	FUNCTION	DESCRIPTION
0	ALU Mode	0: A + B 1: B – A
1	Pass A	0: ALU Input A = 0 1: ALU Input A = Forward Register Path
2	Pass B	0: ALU Input B = 0 1: ALU Input B = Reverse Register Path
11-3	Reserved	Must be set to "0"

TABLE 3. CONFIGURATION REGISTER 1 – ADDRESS 201H

BITS	FUNCTION	DESCRIPTION
0	Odd-Tap Interleave Mode	0: Odd-Tap Interleave Mode Disabled 1: Odd-Tap Interleave Mode Enabled
4-1	I/D Register Length	0000: 1 Register 0001: 2 Registers 0010: 3 Registers 0011: 4 Registers 0100: 5 Registers 0101: 6 Registers 0110: 7 Registers 0111: 8 Registers 1000: 9 Registers 1001: 10 Registers 1010: 11 Registers 1011: 12 Registers 1100: 13 Registers 1101: 14 Registers 1110: 15 Registers 1111: 16 Registers
5	Horizontal Tap Number	0: Even Number of Taps 1: Odd Number of Taps
6	Horizontal Data Reversal	0: Data Reversal Enabled 1: Data Reversal Disabled
11-7	Reserved	Must be set to "0"

Horizontal Select

The word width of the horizontal filter output is 32 bits. However, only 12 bits may be sent to the filter output. The horizontal filter select circuitry determines which 12 bits are passed (see Table 1). The horizontal select registers control the horizontal select circuitry. There are sixteen horizontal select registers. Each select register is 5 bits wide and user-programmable. HRSL3-0 determines which of the sixteen horizontal select registers are used in the horizontal select circuitry. A value of 0 on HRSL3-0 selects horizontal select register 0. A value of 1 selects horizontal select register 1 and so on. HRSL3-0 may be changed every clock cycle if desired. This allows the 12-bit window to be changed every clock cycle. This is useful when filtering interleaved data. Select register loading is discussed in the LF Interface™ section.

Horizontal Limiting

An output limiting function is provided for the output of the horizontal filter. The horizontal limit registers determine the valid range of output values when limiting is enabled (Bit 1 in Configuration Register 5). There are sixteen 24-bit horizontal limit registers. HRSL3-0 determines which horizontal limit register is used during the limit operation. A value of 0 on HRSL3-0 selects horizontal limit register 0. A value of 1 selects horizontal limit register 1 and so on. Each limit register contains both an upper and lower limit value. If the value fed to the limiting circuitry is less than the lower limit, the lower limit value is passed as the filter output. If the value fed to the limiting circuitry is greater than the upper limit, the upper limit value is passed as the filter output. HRSL3-0 may be changed every clock cycle if desired. This allows the limit range to be changed every clock cycle. This is useful when filtering interleaved data. When loading limit values into the device, the upper limit must be greater than the lower limit. Limit register loading is discussed in the LF Interface™ section.

Vertical Filter

The vertical filter is designed to filter a digital image in the vertical dimension. It is a FIR filter which can be configured to have as many as 8 taps.

Line Buffers

There are seven on-chip line buffers. The maximum delay length of each line buffer is 3076 cycles and the minimum is 4 cycles. Configuration Register 2 (CR2) determines the delay length of the line buffers. The line buffer length is equal to the value of CR2 plus 4. A value of 0 for CR2 sets the line buffer length to 4. A value of 3072 for CR2 sets the line buffer length to 3076. Any values for CR2 greater than 3072 are not valid.

The line buffers have two modes of operation: delay mode and recirculate mode. Bit 0 of Configuration Register 3 determines which mode the line buffers are in. In delay mode, the data input to the line buffer is delayed by an amount determined by CR2. In recirculate mode, the output of the line buffer is routed back to the input of the line buffer allowing the line buffer contents to be read multiple times.

Bit 1 of Configuration Register 3 allows the line buffers to be loaded in parallel. When Bit 1 is "1", the input register (DIN11-0) loads all seven line buffers in parallel. This allows all the line buffers to be preloaded with data in the amount of time it normally takes to load a single line buffer.

$\overline{\text{VSHEN}}$ enables or disables the loading of data into the line buffers when the device is in Dimensionally Separate Mode (see the $\overline{\text{VSHEN}}$ section for a full discussion). When in Orthogonal Mode, $\overline{\text{VSHEN}}$ also enables or disables the loading of data into the input register (DIN11-0) and the forward and reverse I/D Registers.

It is important to note that in Orthogonal Mode, either $\overline{\text{HSHEN}}$ or $\overline{\text{VSHEN}}$ can disable the loading of data into the input register (DIN11-0), I/D Registers, and line buffers. Both must be active to enable data loading in Orthogonal Mode.

Interleaved Data

The vertical filter is capable of handling interleaved data. The number of data sets it can handle is determined by the number of data values contained in a video line. If the interleaved video line has 3076 data values or less, the vertical filter can handle it no matter how many data sets are interleaved together.

Vertical Rounding

The vertical filter output may be rounded by adding the contents of one of the sixteen vertical round registers to the vertical filter output (see Figure 11). Each round register is 32 bits wide and user-programmable. This allows the filter's output to be rounded to any precision required. Since any 32-bit value may be programmed into the round registers, the device can support complex rounding algorithms as well as standard Half-LSB rounding. VRSL3-0 determines which of the sixteen vertical round registers are used in the rounding operation. A value of 0 on VRSL3-0 selects vertical round register 0. A value of 1 selects vertical round register 1 and so on. VRSL3-0 may be changed every clock cycle if desired. This allows the rounding algorithm to be changed every clock cycle. This is useful when filtering interleaved data.

TABLE 4. CONFIGURATION REGISTER 2 – ADDRESS 202H

BITS	FUNCTION	DESCRIPTION
11-0	Line Buffer Length	See Line Buffer Description Section

TABLE 5. CONFIGURATION REGISTER 3 – ADDRESS 203H

BITS	FUNCTION	DESCRIPTION
0	Line Buffer Mode	0: Delay Mode 1: Recirculate Mode
1	Line Buffer Load	0: Normal Load 1: Parallel Load
11-2	Reserved	Must be set to "0"

TABLE 6. CONFIGURATION REGISTER 4 – ADDRESS 204H

BITS	FUNCTION	DESCRIPTION
0	HV Filter Mode	0: Orthogonal Mode 1: Dimensionally Separate
1	HV Direction	0: Horizontal to Vertical 1: Vertical to Horizontal
3-2	Orthogonal Kernel Size	00: 3-3 Kernel 01: 5-5 Kernel 10: 7-7 Kernel 11: Not Used
4	Limit Register Load Control	0: Limit Registers Always Enabled 1: Limit Registers Under Shift Enable Control
11-5	Reserved	Must be set to "0"

TABLE 7. CONFIGURATION REGISTER 5 – ADDRESS 205H

BITS	FUNCTION	DESCRIPTION
0	Vertical Limit Enable	0: Vertical Limiting Disabled 1: Vertical Limiting Enabled
1	Horizontal Limit Enable	0: Horizontal Limiting Disabled 1: Horizontal Limiting Enabled
11-2	Reserved	Must be set to "0"

Table 8. HCF/VCF11-9 Decode

11	10	9	DESCRIPTION
0	0	0	Coefficient Banks
0	0	1	Configuration Registers
0	1	0	Horizontal Select Registers
0	1	1	Vertical Select Registers
1	0	0	Horizontal Round Registers
1	0	1	Vertical Round Registers
1	1	0	Horizontal Limit Registers
1	1	1	Vertical Limit Registers

If rounding is not desired, a round register should be loaded with 0 and selected as the register used for rounding. Round register loading is discussed in the LF Interface™ section.

Vertical Select

The word width of the vertical filter output is 32 bits. However, only 12 bits may be sent to the filter output. The vertical filter select circuitry determines which 12 bits are passed (see Table 1). The vertical select registers control the vertical select circuitry. There are sixteen vertical select registers. Each select register is 5 bits wide and user-programmable. VRSL3-0 determines which of the sixteen vertical select registers are used in the vertical select circuitry. A value of 0 on VRSL3-0 selects vertical select register 0. A value of 1 selects vertical select register 1 and so on. VRSL3-0 may be changed every clock cycle if desired. This allows the 12-bit window to be changed every clock cycle. This is useful when filtering interleaved data. Select register loading is discussed in the LF Interface™ section.

Vertical Limiting

An output limiting function is provided for the output of the vertical filter. The vertical limit registers determine the valid range of output values when limiting is enabled (Bit 0 in Configuration Register 5). There are sixteen 24-bit vertical limit registers. VRSL3-0 determines which vertical limit register is used during the limit operation. A value of 0 on VRSL3-0 selects vertical limit register 0. A value of 1 selects vertical limit register 1 and so on. Each limit register contains both an upper and lower limit value. If the value fed to the limiting circuitry is less than the lower limit, the lower limit value is passed as the filter output. If the value fed to the limiting circuitry is greater than the upper limit, the upper limit value is passed as the filter output. VRSL3-0 may be changed every clock cycle if desired. This allows the limit range to be changed every clock cycle. This is useful when filtering interleaved data. When loading limit values into the device, the upper limit must be greater than the lower limit. Limit register loading is discussed in the LF Interface™ section.

Table 9. Hrz. Round Registers

REGISTER	ADDRESS (HEX)
0	800
1	801
•	•
•	•
•	•
14	80E
15	80F

Table 10. Hrz. Select Registers

REGISTER	ADDRESS (HEX)
0	400
1	401
•	•
•	•
•	•
14	40E
15	40F

Table 11. Hrz. Limit Registers

REGISTER	ADDRESS (HEX)
0	C00
1	C01
•	•
•	•
•	•
14	C0E
15	C0F

Table 12. Vrt. Round Registers

REGISTER	ADDRESS (HEX)
0	A00
1	A01
•	•
•	•
•	•
14	A0E
15	A0F

Table 13. Vrt. Select Registers

REGISTER	ADDRESS (HEX)
0	600
1	601
•	•
•	•
•	•
14	60E
15	60F

Table 14. Vrt. Limit Registers

REGISTER	ADDRESS (HEX)
0	E00
1	E01
•	•
•	•
•	•
14	E0E
15	E0F

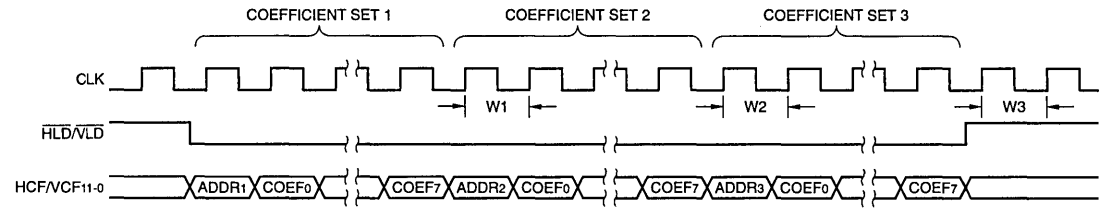
Coefficient Banks

The coefficient banks store the coefficients which feed into the multipliers in the horizontal and vertical filters. There is a separate bank for each multiplier. Each bank can hold 256 12-bit coefficients. The banks are loaded using an LF Interface™. There is a separate LF Interface™ for the horizontal and vertical banks. Coefficient bank loading is discussed in the LF Interface™ section.

Configuration and Control Registers

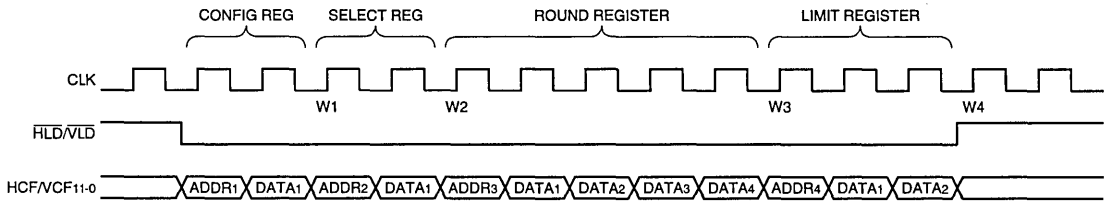
The configuration registers determine how the HV Filter operates. Tables 2 through 7 show the formats of the six configuration registers. There are three types of control registers: round, select, and limit. There are sixteen round registers for the horizontal filter and sixteen for the

FIGURE 12. COEFFICIENT BANK LOADING SEQUENCE



W1: Coefficient Set 1 written to coefficient banks during this clock cycle.
W2: Coefficient Set 2 written to coefficient banks during this clock cycle.
W3: Coefficient Set 3 written to coefficient banks during this clock cycle.

FIGURE 13. CONFIGURATION/CONTROL REGISTER LOADING SEQUENCE



W1: Configuration Register loaded with new data on this rising clock edge.
W2: Select Register loaded with new data on this rising clock edge.
W3: Round Register loaded with new data on this rising clock edge.
W4: Limit Register loaded with new data on this rising clock edge.

vertical filter. Each register is 32 bits wide. HRSL3-0 and VRSL3-0 determine which horizontal and vertical round registers respectively are used for rounding.

There are sixteen select registers for the horizontal filter and sixteen for the vertical filter. Each register is 5 bits wide. HRSL3-0 and VRSL3-0 determine which horizontal and vertical select registers respectively are used in the select circuitry.

There are sixteen limit registers for the horizontal filter and sixteen for the vertical filter. Each register is 24 bits wide and stores both an upper and lower limit value. The lower limit is stored in bits 11-0 and the upper limit is stored in bits 23-12. HRSL3-0 and VRSL3-0 determine which horizontal and vertical limit registers respectively are used for limiting when limiting is enabled. Configuration and control register loading is discussed in the LF Interface™ section.

LF Interface™

The Horizontal and Vertical LF Interfaces™ are used to load data into the horizontal and vertical coefficient banks respectively. They are also used to load data into the configuration and control registers.

The following section describes how the Horizontal LF Interface™ works. The Horizontal and Vertical LF Interfaces™ are identical in function. If $\overline{HLD}$ and HCF11-0 are replaced with $\overline{VLD}$ and VCF11-0, the following section will describe how the Vertical LF Interface™ works.

$\overline{HLD}$ is used to enable and disable the Horizontal LF Interface™. When $\overline{HLD}$ goes LOW, the Horizontal LF Interface™ is enabled for data input. The first value fed into the interface on HCF11-0 is an address which determines what the interface is going to load. The three most significant bits (HCF11-9) determine if the LF Interface™ will load coefficient banks or configuration/control registers (see Table 8). The nine least significant bits (HCF8-0) are the address for whatever is to be loaded (see Tables 9-14). For example, to load address 15 of the horizontal coefficient banks, the first data value into the LF Interface™ should be 00FH. To load horizontal limit register 10, the first data value should be C0AH. The first address value should be loaded into the interface on the same clock cycle that latches the HIGH to LOW transition of $\overline{HLD}$ (see Figures 12 and 13).

The next value(s) loaded into the interface are the data value(s) which will be stored in the bank or register defined by the address value. When loading coefficient banks, the inter-

face will expect eight values to be loaded into the device after the address value. The eight values are coefficients 0 through 7. When loading configuration or select registers, the interface will expect one value after the address value. When loading round registers, the interface will expect four values after the address value. When loading limit registers, the interface will expect two values after the address value. Figures 12 and 13 show the data loading sequences for the coefficient banks and configuration/control registers.

Table 15 shows an example of loading data into the coefficient banks. The following data values are written into address 10 of coefficient banks 0 through 7: 210H, 543H, C76H, 9E3H, 701H, 832H, F20H, 143H. Table 16 shows an example of loading data into a configuration register. Data value 003H is written into Configuration Register 4. Table 17 shows an example of loading data into a round register. Data value 7683F4A2H is written into horizontal round register 12. Table 18 shows an example of loading data into a select register. Data value 00FH is loaded into horizontal select register 2. Table 19 shows an example of loading data into vertical limit register 7. Data value 390H is loaded as the lower limit and 743H is loaded as the upper limit.

It takes 9S clock cycles to load S coefficient sets into the device. Therefore, it takes 2304 clock cycles to load all 256 coefficient sets. Assuming an 80 MHz clock rate, all 256 coefficient sets can be updated in 28.8 µs, which is well within vertical blanking time. It takes 5S or 3S clock cycles to load S round or limit registers respectively. Therefore, it takes

2

TABLE 15. COEFFICIENT BANK LOADING FORMAT

	H/VCF_{11}	H/VCF_{10}	H/VCF_9	H/VCF_8	H/VCF_7	H/VCF_6	H/VCF_5	H/VCF_4	H/VCF_3	H/VCF_2	H/VCF_1	H/VCF_0
1st Word - Address	0	0	0	0	0	0	0	0	1	0	1	0
2nd Word - Bank 0	0	0	1	0	0	0	0	1	0	0	0	0
3rd Word - Bank 1	0	1	0	1	0	1	0	0	0	0	1	1
4th Word - Bank 2	1	1	0	0	0	1	1	1	0	1	1	0
5th Word - Bank 3	1	0	0	1	1	1	1	0	0	0	1	1
6th Word - Bank 4	0	1	1	1	0	0	0	0	0	0	0	1
7th Word - Bank 5	1	0	0	0	0	0	1	1	0	0	1	0
8th Word - Bank 6	1	1	1	1	0	0	1	0	0	0	0	0
9th Word - Bank 7	0	0	0	1	0	1	0	0	0	0	1	1

TABLE 16. CONFIGURATION REGISTER LOADING FORMAT

	H/VCF_{11}	H/VCF_{10}	H/VCF_9	H/VCF_8	H/VCF_7	H/VCF_6	H/VCF_5	H/VCF_4	H/VCF_3	H/VCF_2	H/VCF_1	H/VCF_0
1st Word - Address	0	0	1	0	0	0	0	0	0	1	0	0
2nd Word - Data	0	0	0	0	0	0	0	0	0	0	1	1

TABLE 17. ROUND REGISTER LOADING FORMAT

	H/VCF_{11}	H/VCF_{10}	H/VCF_9	H/VCF_8	H/VCF_7	H/VCF_6	H/VCF_5	H/VCF_4	H/VCF_3	H/VCF_2	H/VCF_1	H/VCF_0
1st Word - Address	1	0	0	0	0	0	0	0	1	1	0	0
2nd Word - Data	R	R	R	R	1	0	1	0	0	0	1	0*
3rd Word - Data	R	R	R	R	1	1	1	1	0	1	0	0
4th Word - Data	R	R	R	R	1	0	0	0	0	0	1	1
5th Word - Data	R	R	R	R	0**	1	1	1	0	1	1	0

R = Reserved. Must be set to "0".
* This bit represents the LSB of the Round Register.
** This bit represents the MSB of the Round Register.

256 clock cycles to update all round and limit registers (both horizontal and vertical). Assuming an 80 MHz clock rate, all horizontal and vertical round/limit registers can be updated in 3.2 µs.

The coefficient banks and configuration/control registers are not loaded with data until all data values for the specified address are loaded into the LF Interface™. In other words, the coefficient banks are not written to until all eight coefficients have been loaded into the LF Interface™. A round register is not written to until all four data values are loaded.

After the last data value is loaded, the interface will expect a new address value on the next clock cycle. After the next address value is loaded, data loading will begin again as previously discussed. As long as data is loaded into the interface, $\overline{HLD}$ must remain LOW. After all desired coefficient banks and configuration/control registers are loaded with data, the LF Interface™ must be disabled. This is done by setting $\overline{HLD}$ HIGH on the clock cycle after the clock cycle which latches the last data value. It is important that the LF Interface™ remain disabled when not loading data into it.

The horizontal coefficient banks may only be loaded with the Horizontal LF Interface™ and the vertical coefficient banks may only be loaded with the Vertical LF Interface™. The configuration and control registers may be loaded with either the Horizontal or Vertical LF Interfaces™. Since both LF Interfaces™ operate independently of each other, both LF Interfaces™ can load data into their respective coefficient banks at the same time. Or, one LF Interface™ can load the configuration/control registers while the other loads it's respective coefficient banks. If both LF Interfaces™ are used to load a configuration or control register at the same time, the Vertical LF Interface™ will be given priority over the Horizontal LF Interface™. For example, if the Horizontal LF Interface™ attempts to load data into a configuration register at the same time that the Vertical LF Interface™ attempts to load a horizontal round register, the Vertical LF Interface™ will be allowed to load the round register while the Horizontal LF Interface™ will not be allowed to load the configuration register. However, the Horizontal LF Interface™ will continue to function as if the write occurred.

TABLE 18. SELECT REGISTER LOADING FORMAT

	H/VCF11	H/VCF10	H/VCF9	H/VCF8	H/VCF7	H/VCF6	H/VCF5	H/VCF4	H/VCF3	H/VCF2	H/VCF1	H/VCF0
1st Word - Address	0	1	0	0	0	0	0	0	0	0	1	0
2nd Word - Data	0	0	0	0	0	0	0	0	1	1	1	1

TABLE 19. LIMIT REGISTER LOADING FORMAT

	H/VCF11	H/VCF10	H/VCF9	H/VCF8	H/VCF7	H/VCF6	H/VCF5	H/VCF4	H/VCF3	H/VCF2	H/VCF1	H/VCF0
1st Word - Address	1	1	1	0	0	0	0	0	0	1	1	1
2nd Word - Data	0*	0	1	1	1	0	0	1	0	0	0	0
3rd Word - Data	0**	1	1	1	0	1	0	0	0	0	1	1

* This bit represents the MSB of the Lower Limit.
** This bit represents the MSB of the Upper Limit.

Contact factory for additional information.

LF3320
Horizontal Digital Image Filter

FEATURES

- 80 MHz Data Rate
- 12-bit Data and Coefficients
- On-board Memory for 256 Coefficient Sets
- LF Interface™ Allows All 256 Coefficient Sets to be Updated Within Vertical Blanking
- Selectable 16-bit Data Output with User-Defined Rounding and Limiting
- 32-Tap FIR Filter
- Cascadable for More Filter Taps
- Single or Dual Filter Modes
- Supports Interleaved Data Streams
- Supports Decimation up to 16:1 for Increasing Number of Filter Taps
- 3.3 Volt Power Supply
- 5 Volt I/O Tolerant
- Available 100% Screened to MIL-STD-883, Class B

DESCRIPTION

The **LF3320** filters digital images in the horizontal dimension at real-time video rates. The input and coefficient data are both 12 bits and in two's complement format. The output is also in two's complement format and may be rounded to 16 bits.

The LF3320 is designed to take advantage of symmetric coefficient sets. When symmetric coefficient sets are used, the device can be configured as a single 32-tap FIR filter or as two separate 16-tap FIR filters. When asymmetric coefficient sets are used, the device can be configured as a single 16-tap FIR filter or as two separate 8-tap FIR filters. Multiple LF3320s can be cascaded to create larger filters.

Interleave/Decimation Registers (I/D Registers) allow interleaved data to be fed directly into the device and filtered without separating the data into individual data streams. The LF3320 can handle a maximum of sixteen data sets interleaved together. The I/D Registers and on-chip accumulators facilitate using decimation to increase the number of filter taps. Decimation of up to 16:1 is supported.

The LF3320 contains enough on-board memory to store 256 coefficient sets. Two separate LF Interfaces™ allow all 256 coefficient sets to be updated within vertical blanking.

LF3320 BLOCK DIAGRAM

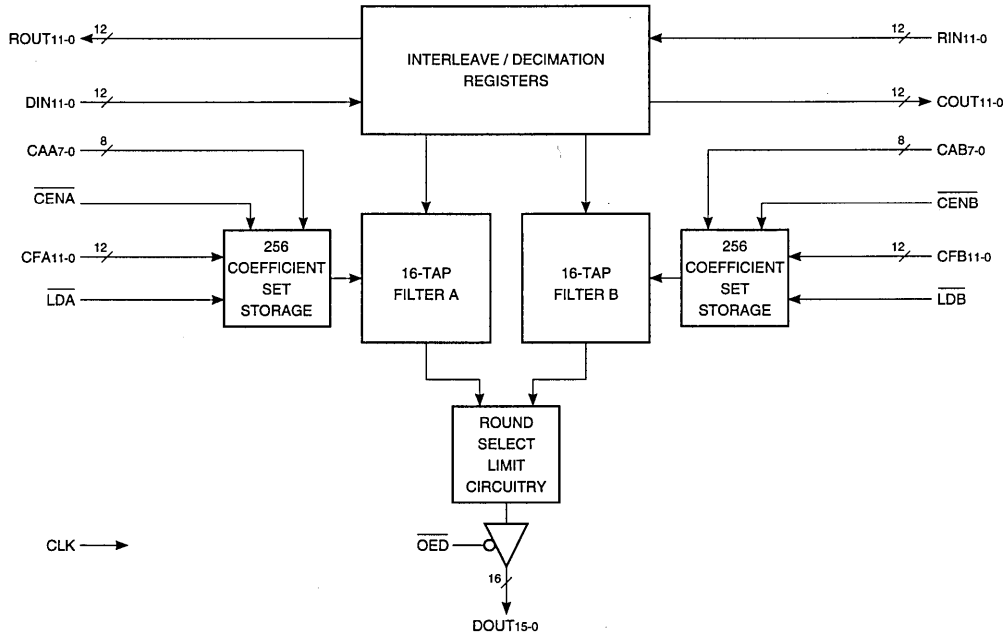
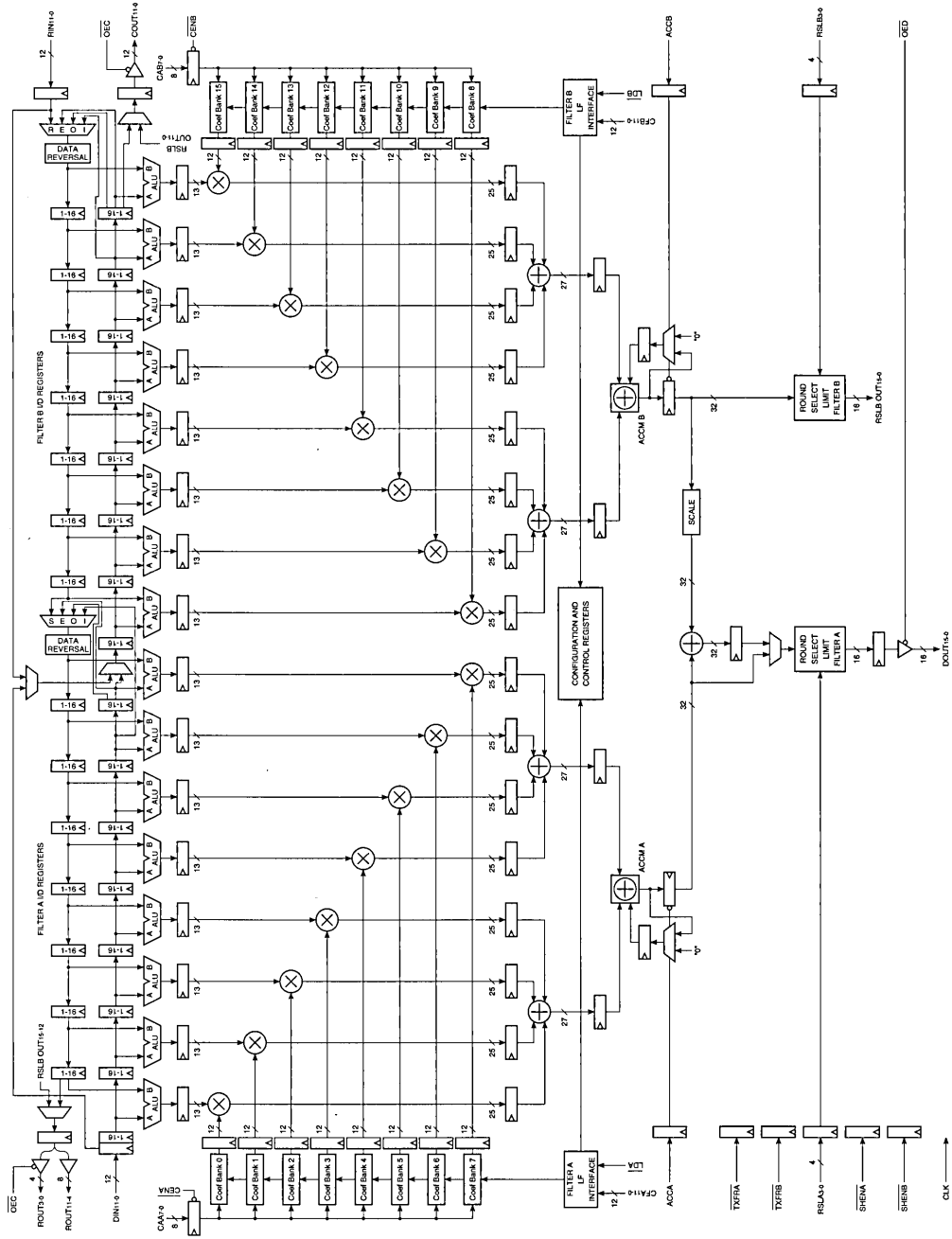


FIGURE 1. LF3320 FUNCTIONAL BLOCK DIAGRAM



SIGNAL DEFINITIONS

Power

VCC and GND

+3.3 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers.

Inputs

DIN11-0 — Data Input

DIN11-0 is the 12-bit data input port to Filter A. In Dual Filter Mode, DIN11-0 can also be the 12-bit input port to Filter B. Data is latched on the rising edge of CLK.

RIN11-0 — Reverse Cascade Input

In Single Filter Mode, RIN11-0 is the 12-bit reverse cascade input port. This port is connected to ROUT11-0 of another LF3320. In Dual Filter Mode, RIN11-0 can be the 12-bit input port to Filter B. Data is latched on the rising edge of CLK.

CFA11-0 — Coefficient A Input

CFA11-0 is used to load data into the Filter A coefficient banks (banks 0 through 7) and the configuration/control registers. Data present on CFA11-0 is latched into the Filter A LF Interface™ on the rising edge of CLK when LDA is LOW (see the LF Interface™ section for a full discussion).

CAA7-0 — Coefficient Address A

CAA7-0 determines which row of data in coefficient banks 0 through 7 is fed to the multipliers. CAA7-0 is latched into Coefficient Address Register A on the rising edge of CLK when CENA is LOW.

FIGURE 2. INPUT FORMATS

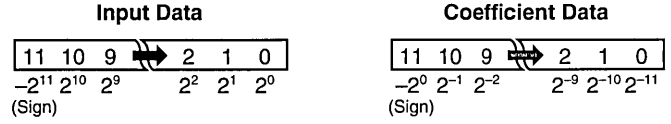


FIGURE 3. ACCUMULATOR OUTPUT FORMATS

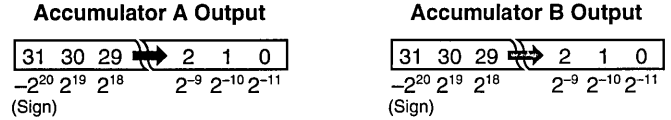


TABLE 1. OUTPUT FORMATS

SLCT4-0	S15	S14	S13	• • •	S8	S7	• • •	S2	S1	S0
00000	F15	F14	F13	• • •	F8	F7	• • •	F2	F1	F0
00001	F16	F15	F14	• • •	F9	F8	• • •	F3	F2	F1
00010	F17	F16	F15	• • •	F10	F9	• • •	F4	F3	F2
•	•	•	•		•	•		•	•	•
•	•	•	•		•	•		•	•	•
•	•	•	•		•	•		•	•	•
01110	F29	F28	F27	• • •	F22	F21	• • •	F16	F15	F14
01111	F30	F29	F28	• • •	F23	F22	• • •	F17	F16	F15
10000	F31	F30	F29	• • •	F24	F23	• • •	F18	F17	F16

CFB11-0 — Coefficient B Input

CFB11-0 is used to load data into the Filter B coefficient banks (banks 8 through 15) and the configuration/control registers. Data present on CFB11-0 is latched into the Filter B LF Interface™ on the rising edge of CLK when LDB is LOW (see the LF Interface™ section for a full discussion).

CAB7-0 — Coefficient Address B

CAB7-0 determines which row of data in coefficient banks 8 through 15 is fed to the multipliers. CAB7-0 is latched into Coefficient Address Register B on the rising edge of CLK when CENB is LOW.

Outputs

DOUT15-0 — Data Output

DOUT15-0 is the 16-bit registered data output port for the overall filter (Single Filter Mode) or Filter A (Dual Filter Mode).

COUT11-0 — Cascade Output

In Single Filter Mode, COUT11-0 is a 12-bit registered cascade output port. COUT11-0 should be connected to DIN11-0 of another LF3320. In Dual Filter Mode, COUT11-0 is a 12-bit registered output port for the lower twelve bits of the 16-bit Filter B output.

ROUT11-0 — Reverse Cascade Output

In Single Filter Mode, ROUT11-0 is a 12-bit registered cascade output port. ROUT11-0 on one device should be connected to RIN11-0 of another LF3320. In Dual Filter Mode, ROUT3-0 is a 4-bit registered output port for the upper four bits of the 16-bit Filter B output. In this mode, ROUT11-4 is disabled.

Controls

$\overline{LDA}$ — Coefficient A Load

When $\overline{LDA}$ is LOW, data on CFA11-0 is latched into the Filter A LF Interface™ on the rising edge of CLK. When $\overline{LDA}$ is HIGH, data is not loaded into the Filter A LF Interface™. When enabling the LF Interface™ for data input, a HIGH to LOW transition of $\overline{LDA}$ is required in order for the input circuitry to function properly. Therefore, $\overline{LDA}$ must be set HIGH immediately after power up to ensure proper operation of the input circuitry (see the LF Interface™ section for a full discussion).

$\overline{CENA}$ — Coefficient Address Enable A

When $\overline{CENA}$ is LOW, data on CAA7-0 is latched into Coefficient Address Register A on the rising edge of CLK. When $\overline{CENA}$ is HIGH, data on CAA7-0 is not latched and the register's contents will not be changed.

$\overline{LDB}$ — Coefficient B Load

When $\overline{LDB}$ is LOW, data on CFB11-0 is latched into the Filter B LF Interface™ on the rising edge of CLK. When $\overline{LDB}$ is HIGH, data is not loaded into the Filter B LF Interface™. When enabling the LF Interface™ for data input, a HIGH to LOW transition of $\overline{LDB}$ is required in order for the input circuitry to function properly. Therefore, $\overline{LDB}$ must be set HIGH immediately after power up to ensure proper operation of the input circuitry (see the LF Interface™ section for a full discussion).

$\overline{CENB}$ — Coefficient Address Enable B

When $\overline{CENB}$ is LOW, data on CAB7-0 is latched into Coefficient Address Register B on the rising edge of CLK. When $\overline{CENB}$ is HIGH, data on CAB7-0 is not latched and the register's contents will not be changed.

$\overline{TXFRA}$ — Filter A LIFO Transfer Control

$\overline{TXFRA}$ is used to change which LIFO in the data reversal circuitry sends data to the reverse data path and which LIFO receives data from the forward data path in Filter A. When $\overline{TXFRA}$ goes LOW, the LIFO sending data to the reverse data path becomes the LIFO receiving data from the forward data path, and the LIFO receiving data from the forward data path becomes the LIFO sending data to the reverse data path. The device must see a HIGH to LOW transition of $\overline{TXFRA}$ in order to switch LIFOs. $\overline{TXFRA}$ is latched on the rising edge of CLK.

$\overline{TXFRB}$ — Filter B LIFO Transfer Control

$\overline{TXFRB}$ is used to change which LIFO in the data reversal circuitry sends data to the reverse data path and which LIFO receives data from the forward data path in Filter B. When $\overline{TXFRB}$ goes LOW, the LIFO sending data to the reverse data path becomes the LIFO receiving data from the forward data path, and the LIFO receiving data from the forward data path becomes the LIFO sending data to the reverse data path. The device must see a HIGH to LOW transition of $\overline{TXFRB}$ in order to switch LIFOs. $\overline{TXFRB}$ is latched on the rising edge of CLK.

ACCA — Accumulator A Control

When ACCA is HIGH, Accumulator A is enabled for accumulation and the Accumulator A Output Register is disabled for loading. When ACCA is LOW, no accumulation is performed and the Accumulator A Output Register is enabled for loading. ACCA is latched on the rising edge of CLK.

ACCB — Accumulator B Control

When ACCB is HIGH, Accumulator B is enabled for accumulation and the Accumulator B Output Register is disabled for loading. When ACCB is LOW, no accumulation is performed and the Accumulator B Output Register is enabled for loading. ACCB is latched on the rising edge of CLK.

$\overline{SHENA}$ — Filter A Shift Enable

In Dual Filter Mode, $\overline{SHENA}$ enables or disables the loading of data into the Input (DIN11-0), Reverse Cascade Output (ROUT11-0) and Filter A I/D Registers. When $\overline{SHENA}$ is LOW, data is latched into the Input/Cascade Registers and shifted through the I/D Registers on the rising edge of CLK. When $\overline{SHENA}$ is HIGH, data can not be loaded into the Input/Cascade Registers or shifted through the I/D Registers and their contents will not be changed.

In Single Filter Mode, $\overline{SHENA}$ also enables or disables the loading of data into the Reverse Cascade Input (RIN11-0), Cascade Output (COUT11-0), and Filter B I/D Registers. It is important to note that in Single Filter Mode, either $\overline{SHENA}$ or $\overline{SHENB}$ can disable data loading. Both must be active to enable data loading in Single Filter Mode. $\overline{SHENA}$ is latched on the rising edge of CLK.

$\overline{SHENB}$ — Filter B Shift Enable

In Dual Filter Mode, $\overline{SHENB}$ enables or disables the loading of data into the Reverse Cascade Input (RIN11-0), Cascade Output (COUT11-0), and Filter B I/D Registers. When $\overline{SHENB}$ is LOW, data is latched into the Cascade Registers and shifted through

the I/D Registers on the rising edge of CLK. When $\overline{SHENB}$ is HIGH, data can not be loaded into the Cascade Registers or shifted through the I/D Registers and their contents will not be changed.

In Single Filter Mode, $\overline{SHENB}$ also enables or disables the loading of data into the Input (DIN11-0), Reverse Cascade Output (ROUT11-0) and Filter A I/D Registers. It is important to note that in Single Filter Mode, either $\overline{SHENA}$ or $\overline{SHENB}$ can disable data loading. Both must be active to enable data loading in Single Filter Mode. $\overline{SHENB}$ is latched on the rising edge of CLK.

RSLA3-0 — Filter A Round/Select/Limit Control

RSLA3-0 determines which of the sixteen user-programmable round/select/limit registers are used in the Filter A round/select/limit circuitry. A value of 0 on RSLA3-0 selects round/select/limit register 0. A value of 1 selects round/select/limit register 1 and so on. RSLA3-0 is latched on the rising edge of CLK (see the round, select, and limit sections for a complete discussion).

RSLB3-0 — Filter B Round/Select/Limit Control

RSLB3-0 determines which of the sixteen user-programmable round/select/limit registers are used in the Filter B round/select/limit circuitry. A value of 0 on RSLB3-0 selects round/select/limit register 0. A value of 1 selects round/select/limit register 1 and so on. RSLB3-0 is latched on the rising edge of CLK (see the round, select, and limit sections for a complete discussion).

$\overline{OED}$ — DOUT Output Enable

When $\overline{OED}$ is LOW, DOUT15-0 is enabled for output. When $\overline{OED}$ is HIGH, DOUT15-0 is placed in a high-impedance state.

$\overline{OEC}$ — COUT/ROUT Output Enable

When $\overline{OEC}$ is LOW, COUT11-0 and ROUT3-0 are enabled for output. When $\overline{OEC}$ is HIGH, COUT11-0 and ROUT3-0 are placed in a high-impedance state.

OPERATIONAL MODES

Single Filter Mode

In this mode, the device operates as a single FIR filter (see Figure 4). It can be configured to have as many as 32 taps if symmetric coefficient sets are used. If asymmetric coefficient sets are used, the device can be configured to have as many as 16 taps. Cascade ports are provided to facilitate cascading multiple devices to increase the number of filter taps. Bit 1 in Configuration Register 5 determines the filter mode. In Single Filter Mode, DIN11-0 is the data input for the filter and DOUT15-0 is the data output for the filter.

2

FIGURE 4. SINGLE FILTER MODE

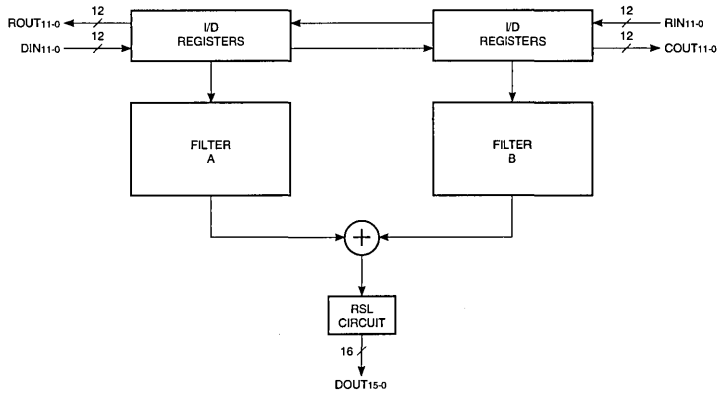


FIGURE 5. DUAL FILTER MODE

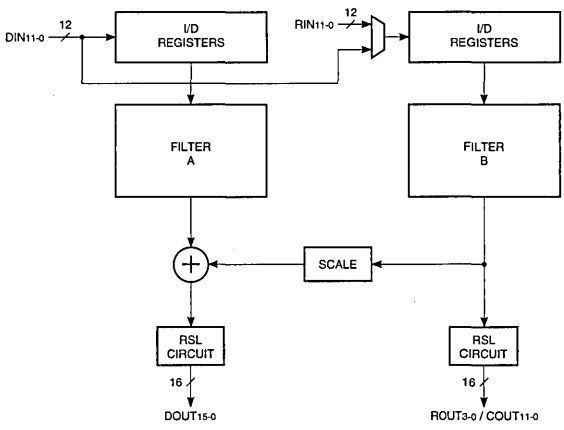


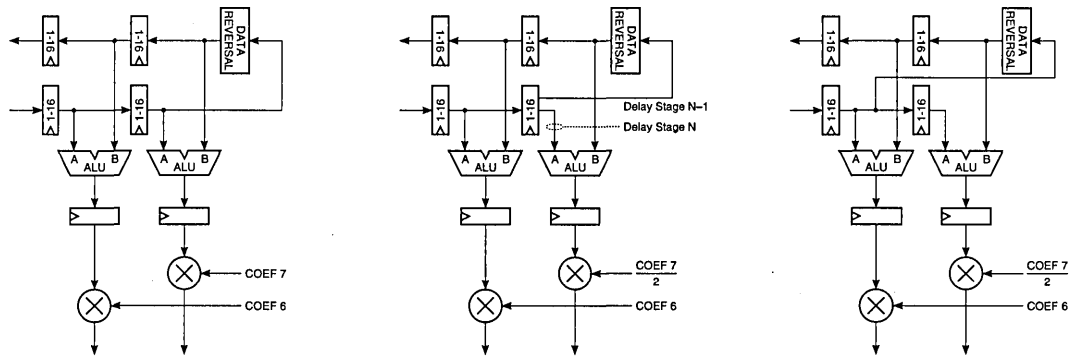
FIGURE 6. SYMMETRIC COEFFICIENT SET EXAMPLES

Even-Tap, Even-Symmetric Coefficient Set

Odd-Tap, Even-Symmetric Coefficient Set

Even-Tap, Odd-Symmetric Coefficient Set

FIGURE 7. I/D REGISTER DATA PATHS



EVEN-TAP MODE

ODD-TAP MODE

ODD-TAP INTERLEAVE MODE

Dual Filter Mode

In this mode, the device operates as two separate FIR filters (see Figure 5). Each filter can be configured to have as many as 16 taps if symmetric coefficient sets are used. If asymmetric coefficient sets are used, each filter can be configured to have as many as 8 taps. In Dual Filter Mode, DIN11-0 is the data input for Filter A. Either RIN11-0 or DIN11-0 can be the data input for Filter B. The Filter B input is determined by Bit 2 in Configuration Register 5. DOUT15-0 is the data output for Filter A. COUT11-0 and ROUT3-0 together form the data output for Filter B. COUT11-0 is the twelve least significant bits and ROUT3-0 is the four most significant bits of the 16-bit Filter B output.

FUNCTIONAL DESCRIPTION

ALUs

The ALUs double the number of filter taps available, when symmetric coefficient sets are used, by pre-adding data values which are then multiplied by a common coefficient (see Figure 6). The ALUs can perform two operations: A+B and B–A. Bit 0 of Configuration Register 0 determines the operation of the ALUs in Filter A. Bit 0 of Configuration Register 2 determines the operation of the ALUs in Filter B. A+B is used with even-symmetric coefficient sets. B–A is used with odd-symmetric coefficient sets. Also, either the A or B operand may be set to 0. Bits 1 and 2 of Configuration Register 0 and Configuration Register 2 control the ALU inputs in Filters A and B respectively. A+0 or B+0 are used with asymmetric coefficient sets.

Interleave/Decimation Registers

The Interleave/Decimation Registers (I/D Registers) feed the ALU inputs. They allow the device to filter up to sixteen data sets interleaved into the same data stream without having to separate the data sets. The I/D Registers should be set to a length equal to the number of data sets interleaved together. For example, if two data sets are interleaved together, the I/D Registers should be set to a length of two. Bits 1 through 4 of Configuration Register 1 and Configuration Register 3 determine the length of the I/D Registers in Filters A and B respectively.

TABLE 2. CONFIGURATION REGISTER 0 – ADDRESS 200H

BITS	FUNCTION	DESCRIPTION
0	ALU Mode Filter A	0: A + B 1: B – A
1	Pass A Filter A	0: ALU Input A = 0 1: ALU Input A = Forward Register Path
2	Pass B Filter A	0: ALU Input B = 0 1: ALU Input B = Reverse Register Path
11-3	Reserved	Should be set to "0"

TABLE 3. CONFIGURATION REGISTER 1 – ADDRESS 201H

BITS	FUNCTION	DESCRIPTION
0	Filter A Odd-Tap Interleave Mode	0: Odd-Tap Interleave Mode Disabled 1: Odd-Tap Interleave Mode Enabled
4-1	Filter A I/D Register Length	0000: 1 Register 0001: 2 Registers 0010: 3 Registers 0011: 4 Registers 0100: 5 Registers 0101: 6 Registers 0110: 7 Registers 0111: 8 Registers 1000: 9 Registers 1001: 10 Registers 1010: 11 Registers 1011: 12 Registers 1100: 13 Registers 1101: 14 Registers 1110: 15 Registers 1111: 16 Registers
5	Filter A Tap Number	0: Even Number of Taps 1: Odd Number of Taps
6	Filter A Data Reversal	0: Data Reversal Enabled 1: Data Reversal Disabled
11-7	Reserved	Should be set to "0"

The I/D Registers also facilitate using decimation to increase the number of filter taps. Decimation by N is accomplished by reading the filter's output once every N clock cycles. The device supports decimation up to 16:1. With no decimation, the maximum number of filter taps is sixteen. When decimating by N, the number of filter taps becomes 16N because there are N–1 clock cycles when the filter's output is not being read. The extra clock cycles are used to calculate more filter taps.

When decimating, the I/D Registers should be set to a length equal to the decimation factor. For example, when performing a 4:1 decimation, the I/D Registers should be set to a length of four. When not decimating or when only one data set (non-interleaved data) is fed into the device, the I/D Registers should be set to a length of one.

I/D Register Data Path Control

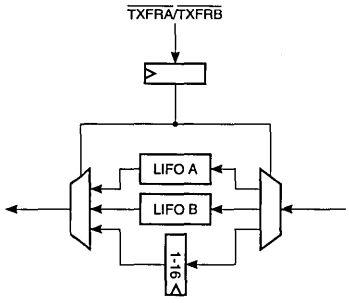
The three multiplexers in the I/D Register data path control how data is routed through the forward and reverse data paths. The forward data path contains the I/D Registers in which data flows from left to right in the block diagram in Figure 1. The reverse data path contains the I/D Registers in which data flows from right to left.

In Single or Dual Filter Modes, data is fed from the forward data path to the reverse data path as follows. When the filter is configured for an even number of taps, data from the last I/D Register in the forward data path is fed into the first I/D Register in the reverse data path (see Figure 7). When the filter is configured for an odd number of taps, the data which will appear at the output of the last I/D Register in the forward data path on the next clock cycle is fed into the first I/D Register in the reverse data path. Bit 5 in Configuration Register 1 and Configuration Register 3 configures Filters A and B respectively for an even or odd number of taps.

When interleaved data is fed through the device and an even tap filter is desired, the filter should be configured for an even number of taps and the I/D Register length should match the number of data sets interleaved together. When interleaved data is fed through the device and an odd tap filter is desired, the filter should be set to Odd-Tap Interleave Mode. Bit 0 of Configuration Register 1 and Configuration Register 3 configures Filters A and B respectively for Odd-Tap Interleave Mode. When the filter is configured for Odd-Tap Interleave Mode, data from the next to last I/D Register in the forward data path is fed into the first I/D Register in the reverse data path.

When the filter is configured for an odd number of taps (interleaved or non-interleaved modes), the filter is structured such that the center data value is aligned simultaneously at the A and B inputs of the last ALU in the forward data path. In order to achieve the correct result, the user must divide the coefficient by two.

FIGURE 8. DATA REVERSAL



Data Reversal

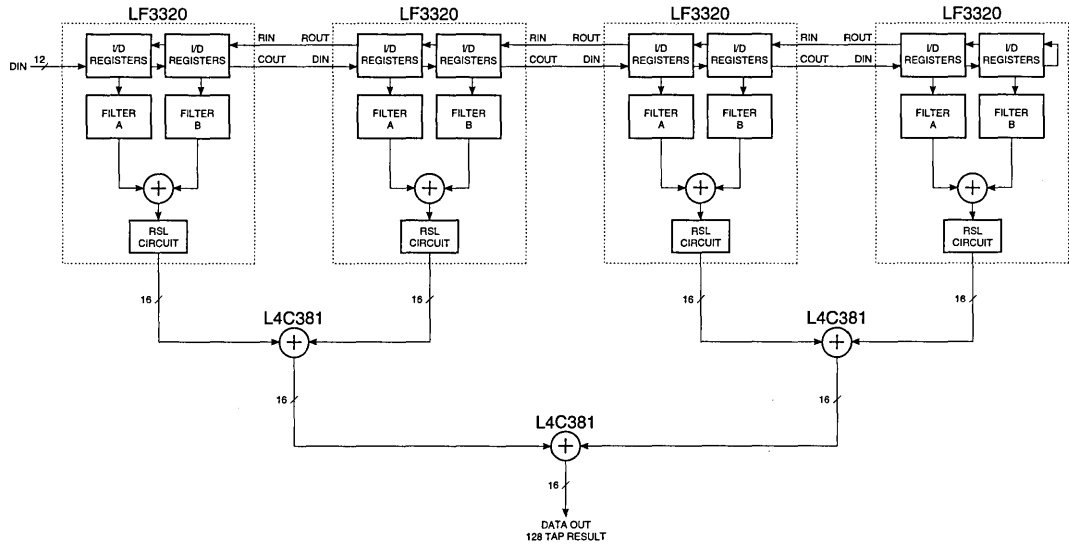
Data reversal circuitry is placed after the multiplexers which route data from the forward data path to the reverse data path (see Figure 8). When decimating, the data stream must be reversed in order for data to be properly aligned at the inputs of the ALUs. When data reversal is enabled, the circuitry uses a pair of LIFOs to reverse the order of the data sent to the reverse data path. $\overline{\text{TXFRA}}$ and $\overline{\text{TXFRB}}$ control the LIFOs in Filters A and B respectively. When $\overline{\text{TXFRA}}$/$\overline{\text{TXFRB}}$ goes LOW, the LIFO sending data to the reverse data path becomes the LIFO receiving data from the forward data path, and the LIFO receiving data from the forward data path becomes the LIFO sending data to the reverse data path. The device must see a HIGH to LOW transition of $\overline{\text{TXFRA}}$/$\overline{\text{TXFRB}}$ in order to switch LIFOs. If decimating by N, $\overline{\text{TXFRA}}$/$\overline{\text{TXFRB}}$ should go LOW once every N clock cycles. When data reversal is disabled, the circuitry functions like an I/D Register. When feeding interleaved data through the filter, data reversal should be disabled. Bit 6 of Configuration Register 1 and Configuration Register 3 enables or disables data reversal for Filters A and B respectively.

Cascading

Three cascade ports are provided to allow cascading of multiple devices for more filter taps (see Figure 9). COUT11-0 of one device should be connected to DIN11-0 of another device. ROUT11-0 of one device should be connected to RIN11-0 of another device. As many LF3320s as desired may be cascaded together. However, the outputs of the LF3320s must be added together with external adders.

Bit 0 of Configuration Register 5 determines how the device will send data to the reverse data path when multiple LF3320s are cascaded together. If a LF3320 is the last in the

FIGURE 9. MULTIPLE LF3320S CASCADED TOGETHER



cascade chain, Bit 0 of Configuration Register 5 should be set to a "0". This will cause the data from the end of the forward data path to be routed to the beginning of the reverse data path based on how the filter is configured (even/odd number of taps or interleave mode). If a LF3320 is not the last in the cascade chain, Bit 0 of Configuration Register 5 should be set to a "1". This will cause RIN11-0 to feed data to the reverse data path. When not cascading, Bit 0 of Configuration Register 5 should be set to a "0".

Special data routing circuitry is used to feed the COUT and ROUT output registers. The data routing circuitry is required to correctly align data in the forward and reverse data paths as data passes from one LF3320 to another. The COUT and ROUT registers are loaded with data which is two clock cycles behind the current output of the I/D Register just before the ROUT or COUT register. This correctly accounts for the extra delays added to the forward and reverse data paths by the input/output cascade registers.

Output Adder

The Output Adder adds the Filter A and B outputs together when the device is in Single Filter Mode. If 24-bit data and 12-bit coefficients or 12-bit data and 24-bit coefficients are desired, the LF3320 can facilitate this by scaling the Filter B output by 2^{-12} before adding it to the Filter A output. Bit 3 in Configuration Register 5 determines if the Filter B output is scaled before being added to the Filter A output.

Rounding

The overall filter output (Single Filter Mode) or Filter A and B outputs (Dual Filter Mode) may be rounded by adding the contents of one of the sixteen Filter A or B round registers to the overall filter, Filter A, or Filter B outputs (see Figure 10). The Filter A round registers are used for the overall filter (Single Filter Mode) or Filter A (Dual Filter Mode). The Filter B round registers are used for Filter B (Dual Filter Mode). Each round register is 32 bits wide and user-programmable. This allows the filter's output to be rounded to any precision required. Since any 32-bit value may be programmed into the round registers, the device can support complex rounding algorithms as well as standard Half-LSB rounding. RSLA3-0 determines which of the sixteen Filter A round registers are used in the Filter A rounding circuitry. RSLB3-0 determines which of the sixteen Filter B round registers are used in the Filter B rounding circuitry. A value of 0 on RSLA/RSLB3-0 selects Filter A/B round register 0. A value of 1 selects Filter A/B round register 1 and so on. RSLA/RSLB3-0 may be changed every clock cycle if desired. This allows the rounding algorithm to be changed every clock cycle. This is useful when filtering interleaved data. If rounding is not desired, a round register should be loaded with 0 and selected as the register used for rounding. Round register loading is discussed in the LF Interface™ section.

Output Select

The word width of the overall filter, Filter A, and Filter B outputs is 32 bits. However, only 16 bits may be sent to DOUT15-0 (Single or Dual Filter Modes)

FIGURE 10. FILTER A AND B ROUND/SELECT/LIMIT CIRCUITRY

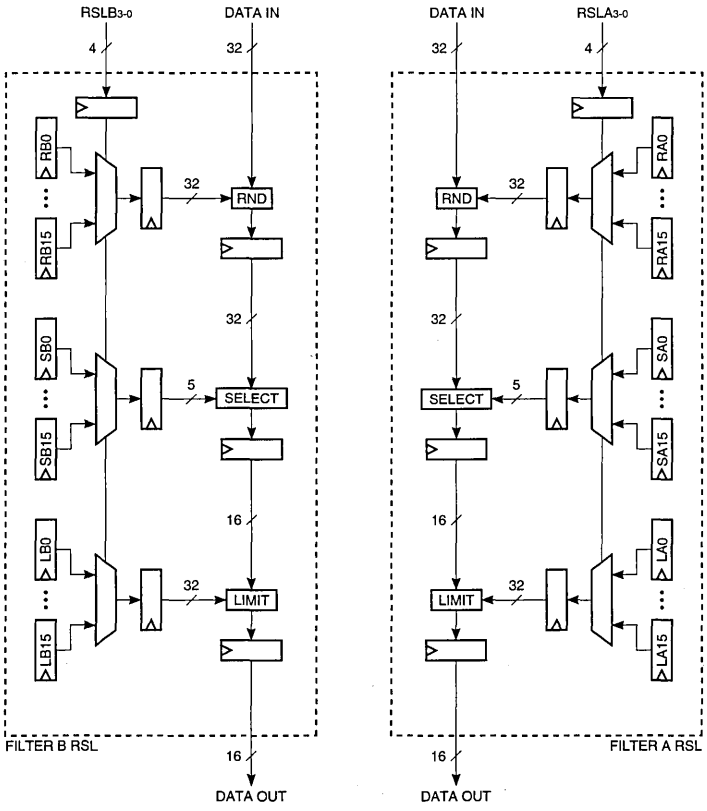


TABLE 4. CONFIGURATION REGISTER 2 – ADDRESS 202H

BITS	FUNCTION	DESCRIPTION
0	ALU Mode Filter B	0: A + B 1: B – A
1	Pass A Filter B	0: ALU Input A = 0 1: ALU Input A = Forward Register Path
2	Pass B Filter B	0: ALU Input B = 0 1: ALU Input B = Reverse Register Path
11-3	Reserved	Must be set to "0"

TABLE 5. CONFIGURATION REGISTER 3 – ADDRESS 203H

BITS	FUNCTION	DESCRIPTION
0	Filter B Odd-Tap Interleave Mode	0: Odd-Tap Interleave Mode Disabled 1: Odd-Tap Interleave Mode Enabled
4-1	Filter B I/D Register Length	0000: 1 Register 0001: 2 Registers 0010: 3 Registers 0011: 4 Registers 0100: 5 Registers 0101: 6 Registers 0110: 7 Registers 0111: 8 Registers 1000: 9 Registers 1001: 10 Registers 1010: 11 Registers 1011: 12 Registers 1100: 13 Registers 1101: 14 Registers 1110: 15 Registers 1111: 16 Registers
5	Filter B Tap Number	0: Even Number of Taps 1: Odd Number of Taps
6	Filter B Data Reversal	0: Data Reversal Enabled 1: Data Reversal Disabled
11-7	Reserved	Must be set to "0"

and COUT11-0/ROUT3-0 (Dual Filter Mode). The Filter A/B select circuitry determines which 16 bits are passed (see Table 1). The Filter A/B select registers control the Filter A/B select circuitry. There are sixteen Filter A and B select registers. The Filter A select registers are used for the overall filter (Single Filter Mode) or Filter A (Dual Filter Mode). The Filter B select registers are used for Filter B (Dual Filter Mode). Each select register is 5 bits wide and user-programmable. RSLA3-0 determines which of the sixteen Filter A select registers are used in the Filter A select circuitry. RSLB3-0 determines which of the sixteen Filter B select registers are used in the Filter B select circuitry. A value of 0 on RSLA/RSLB3-0 selects Filter A/B select register 0. A value of 1 selects Filter A/B select register 1 and so on. RSLA/RSLB3-0 may be changed every clock cycle if desired. This allows the 16-bit window to be changed every clock cycle. This is useful when filtering interleaved data. Select register loading is discussed in the LF Interface™ section.

Output Limiting

An output limiting function is provided for the overall filter, Filter A, and Filter B outputs. The Filter A limiting circuitry is used to limit the overall filter output (Single Filter Mode) and the Filter A output (Dual Filter Mode). The Filter B limiting circuitry is used to limit the Filter B output (Dual Filter Mode). The Filter A and B limit registers determine the valid range of output values for the Filter A and B limiting circuitry respectively. There are sixteen 32-bit user-programmable limit registers for both Filters A and B. The Filter A limit registers are used for the overall filter (Single Filter Mode) or Filter A (Dual Filter Mode). The Filter B limit registers are used for Filter B (Dual Filter Mode). RSLA3-0 determines which of the sixteen Filter A limit registers are used in the Filter A limit circuitry. RSLB3-0 determines which of the sixteen Filter B limit registers are used in the Filter B limit circuitry. A value of 0 on RSLA/RSLB3-0 selects Filter A/B limit register 0. A value of 1 selects Filter A/B limit register 1 and so on. Each limit register contains an upper and lower limit value. If the value fed to the limiting circuitry is less than the lower limit, the lower limit value is passed as the filter output. If the value fed to the limiting circuitry is greater than the upper limit, the upper limit value is passed as the filter output. Bit 1 and 0 in Configuration Register 4 enable and disable Filter A and B limiting respectively. RSLA/RSLB3-0 may be changed every clock cycle if desired. This allows the limit range to be changed every clock cycle. This is useful when filtering interleaved data. When loading limit values into the device, the upper limit must be greater than the lower limit. Limit register loading is discussed in the LF Interface™ section.

Coefficient Banks

The coefficient banks store the coefficients which feed into the multipliers in Filters A and B. There

is a separate bank for each multiplier. Each bank can hold 256 12-bit coefficients. The banks are loaded using an LF Interface™. There is a separate LF Interface™ for the Filter A and B banks. Coefficient bank loading is discussed in the LF Interface™ section.

Configuration and Control Registers

The configuration registers determine how the LF3320 operates. Tables 2 through 7 show the formats of the six configuration registers. There are three types of control registers: round, select, and limit. There are sixteen round registers for Filter A and sixteen for Filter B. Each register is 32 bits wide. RSLA3-0 and RSLB3-0 determine which Filter A and B round registers respectively are used for rounding.

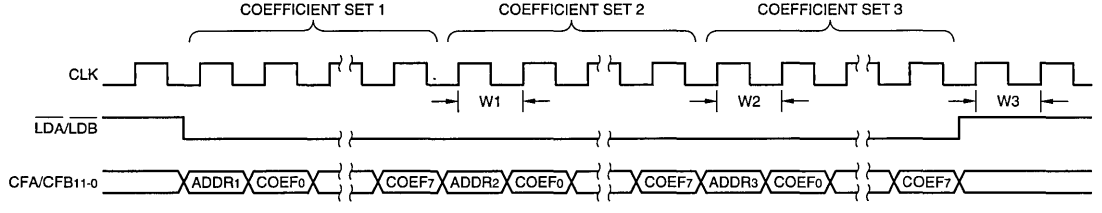
TABLE 6. CONFIGURATION REGISTER 4 – ADDRESS 204H

BITS	FUNCTION	DESCRIPTION
0	Filter B Limit Enable	0 : Limiting Disabled 1 : Limiting Enabled
1	Filter A Limit Enable	0 : Limiting Disabled 1 : Limiting Enabled
11-2	Reserved	Must be set to "0"

TABLE 7. CONFIGURATION REGISTER 5 – ADDRESS 205H

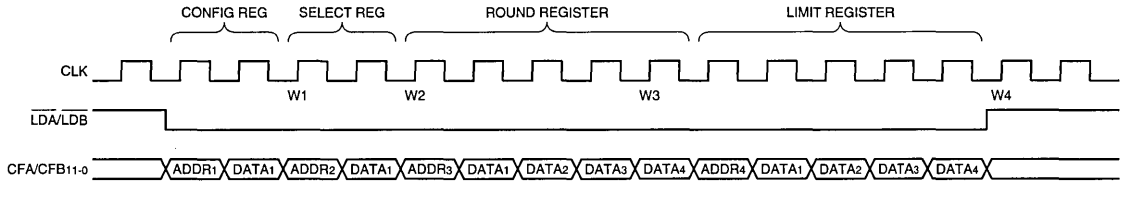
BITS	FUNCTION	DESCRIPTION
0	Cascade Mode	0 : Last In Line 1 : First or Middle in Line
1	Single/Dual Filter Mode	0 : Single Filter Mode 1 : Dual Filter Mode
2	Filter B Input	0 : RIN_{11-0} 1 : DIN_{11-0}
3	Output Adder Control	0 : Filter A + Filter B 1 : Filter A + Filter B (Filter B Scaled by 2^{-12})
11-4	Reserved	Must be set to "0"

FIGURE 11. COEFFICIENT BANK LOADING SEQUENCE



W1: Coefficient Set 1 written to coefficient banks during this clock cycle.
W2: Coefficient Set 2 written to coefficient banks during this clock cycle.
W3: Coefficient Set 3 written to coefficient banks during this clock cycle.

FIGURE 12. CONFIGURATION/CONTROL REGISTER LOADING SEQUENCE



W1: Configuration Register loaded with new data on this rising clock edge.
W2: Select Register loaded with new data on this rising clock edge.
W3: Round Register loaded with new data on this rising clock edge.
W4: Limit Register loaded with new data on this rising clock edge.

TABLE 8. CFA/CFB11-9 DECODE

11	10	9	DESCRIPTION
0	0	0	Coefficient Banks
0	0	1	Configuration Registers
0	1	0	Filter A Select Registers
0	1	1	Filter B Select Registers
1	0	0	Filter A Round Registers
1	0	1	Filter B Round Registers
1	1	0	Filter A Limit Registers
1	1	1	Filter B Limit Registers

There are sixteen select registers for Filter A and sixteen for Filter B. Each register is 5 bits wide. RSLA3-0 and RSLB3-0 determine which Filter A and B select registers respectively are used in the select circuitry.

There are sixteen limit registers for Filter A and sixteen for Filter B. Each register is 32 bits wide and stores both an upper and lower limit value. The lower limit is stored in bits 15-0 and the upper limit is stored in bits 31-16. RSLA3-0 and RSLB3-0 determine which Filter A and B limit registers respectively are used for limiting when limiting is enabled. Configuration and control register loading is discussed in the LF Interface™ section.

TABLE 9. FLTR. A ROUND REGISTERS

REGISTER	ADDRESS (HEX)
0	800
1	801
•	•
•	•
•	•
14	80E
15	80F

TABLE 10. FLTR.A SELECT REGISTERS

REGISTER	ADDRESS (HEX)
0	400
1	401
•	•
•	•
•	•
14	40E
15	40F

TABLE 11. FLTR. A LIMIT REGISTERS

REGISTER	ADDRESS (HEX)
0	C00
1	C01
•	•
•	•
•	•
14	C0E
15	C0F

TABLE 12. FLTR. B ROUND REGISTERS

REGISTER	ADDRESS (HEX)
0	A00
1	A01
•	•
•	•
•	•
14	A0E
15	A0F

TABLE 13. FLTR.B SELECT REGISTERS

REGISTER	ADDRESS (HEX)
0	600
1	601
•	•
•	•
•	•
14	60E
15	60F

TABLE 14. FLTR. B LIMIT REGISTERS

REGISTER	ADDRESS (HEX)
0	E00
1	E01
•	•
•	•
•	•
14	E0E
15	E0F

LF Interface™

The Filter A and B LF Interfaces™ are used to load data into the Filter A and B coefficient banks respectively. They are also used to load data into the configuration and control registers.

The following section describes how the Filter A LF Interface™ works. The Filter A and B LF Interfaces™ are identical in function. If $\overline{LDA}$ and CFA11-0 are replaced with $\overline{LDB}$ and CFB11-0, the following section will describe how the Filter B LF Interface™ works.

$\overline{LDA}$ is used to enable and disable the Filter A LF Interface™. When $\overline{LDA}$ goes LOW, the Filter A LF Interface™ is enabled for data input. The first value fed into the interface on CFA11-0 is an address which determines what the interface is going to load. The three most significant bits (CFA11-9) determine if the LF Interface™ will load coefficient banks or configuration/control registers (see Table 8). The nine least significant bits (CFA8-0) are the address for whatever is to be loaded (see Tables 9 through 14). For example, to load address 15 of the Filter A coefficient banks, the first data value into the LF Interface™ should be 00FH. To load Filter A limit register 10, the first data value should be C0AH. The first address value should be loaded into the interface on the same clock cycle that latches the HIGH to LOW transition of $\overline{LDA}$ (see Figures 11 and 12).

The next value(s) loaded into the interface are the data value(s) which will be stored in the bank or register defined by the address value. When loading coefficient banks, the interface will expect eight values to be loaded into the device after the address value. The eight values are coefficients 0 through 7. When loading configuration or select registers, the interface will expect one value after the address value. When loading round or limit registers, the interface will expect four values after the address value. Figures 11 and 12 show the data loading sequences for the coefficient banks and configuration/control registers.

Table 15 shows an example of loading data into the coefficient banks. The following data values are written into address 10 of coefficient banks 0 through 7: 210H, 543H, C76H, 9E3H, 701H, 832H, F20H, 143H. Table 16 shows an example of loading data into a configuration register. Data value 003H is written into Configuration Register 4. Table 17 shows an example of loading data into a round register. Data value 7683F4A2H is

written into Filter A round register 12. Table 18 shows an example of loading data into a select register. Data value 00FH is loaded into Filter A select register 2. Table 19 shows an example of loading data into Filter B limit register 7. Data value 3B60H is loaded as the lower limit and 72A4H is loaded as the upper limit.

It takes 9S clock cycles to load S coefficient sets into the device. Therefore, it takes 2304 clock cycles to load all 256 coefficient sets. Assuming an 80 MHz clock rate, all 256 coefficient sets can be updated in 28.8 µs, which is well within vertical blanking time.

It takes 5S clock cycles to load S round or limit registers. Therefore, it takes 320 clock cycles to update all round and limit registers (both Filters A and B). Assuming an 80 MHz clock rate, all Filter A and B round/limit registers can be updated in 4.0 µs.

The coefficient banks and configuration/control registers are not loaded with data until all data values for the specified address are loaded into the LF Interface™. In other words, the coefficient banks are not written to until all eight coefficients have been loaded into the LF Interface™. A round register is not written to until all four data values are loaded.

After the last data value is loaded, the interface will expect a new address value on the next clock cycle. After the next address value is loaded, data loading will begin again as previously discussed. As long as data is loaded into the interface, $\overline{LDA}$ must remain LOW. After all desired coefficient banks and configuration/control registers are loaded with data, the LF Interface™ must be disabled. This is done by setting $\overline{LDA}$ HIGH on the clock cycle after the clock cycle which latches the last data value. It is important that the LF Interface™ remain disabled when not loading data into it.

2

TABLE 15. COEFFICIENT BANK LOADING FORMAT

	CFA/B11	CFA/B10	CFA/B9	CFA/B8	CFA/B7	CFA/B6	CFA/B5	CFA/B4	CFA/B3	CFA/B2	CFA/B1	CFA/B0
1st Word - Address	0	0	0	0	0	0	0	0	1	0	1	0
2nd Word - Bank 0	0	0	1	0	0	0	0	1	0	0	0	0
3rd Word - Bank 1	0	1	0	1	0	1	0	0	0	0	1	1
4th Word - Bank 2	1	1	0	0	0	1	1	1	0	1	1	0
5th Word - Bank 3	1	0	0	1	1	1	1	0	0	0	1	1
6th Word - Bank 4	0	1	1	1	0	0	0	0	0	0	0	1
7th Word - Bank 5	1	0	0	0	0	0	1	1	0	0	1	0
8th Word - Bank 6	1	1	1	1	0	0	1	0	0	0	0	0
9th Word - Bank 7	0	0	0	1	0	1	0	0	0	0	1	1

TABLE 16. CONFIGURATION REGISTER LOADING FORMAT

	CFA/B11	CFA/B10	CFA/B9	CFA/B8	CFA/B7	CFA/B6	CFA/B5	CFA/B4	CFA/B3	CFA/B2	CFA/B1	CFA/B0
1st Word - Address	0	0	1	0	0	0	0	0	0	1	0	0
2nd Word - Data	0	0	0	0	0	0	0	0	0	0	1	1

TABLE 17. ROUND REGISTER LOADING FORMAT

	CFA/B11	CFA/B10	CFA/B9	CFA/B8	CFA/B7	CFA/B6	CFA/B5	CFA/B4	CFA/B3	CFA/B2	CFA/B1	CFA/B0
1st Word - Address	1	0	0	0	0	0	0	0	1	1	0	0
2nd Word - Data	R	R	R	R	1	0	1	0	0	0	1	0*
3rd Word - Data	R	R	R	R	1	1	1	1	0	1	0	0
4th Word - Data	R	R	R	R	1	0	0	0	0	0	1	1
5th Word - Data	R	R	R	R	0**	1	1	1	0	1	1	0

R = Reserved. Must be set to "0".
* This bit represents the LSB of the Round Register.
** This bit represents the MSB of the Round Register.

The Filter A coefficient banks may only be loaded with the Filter A LF Interface™ and the Filter B coefficient banks may only be loaded with the Filter B LF Interface™. The configuration and control registers may be loaded with either the Filter A or B LF Interfaces™. Since both LF Interfaces™ operate independently of each other, both LF Interfaces™ can load data into their respective coefficient banks at the same time. Or, one LF Interface™ can load the configuration/control registers while the other loads it's respective coefficient banks. If both LF Interfaces™ are used to load a configuration or control register at the same time, the Filter B LF Interface™ will be given priority over the Filter A LF Interface™. For example, if the Filter A LF Interface™ attempts to load data into a configuration register at the same time that the Filter B LF Interface™ attempts to load a Filter A round register, the Filter B LF Interface™ will be allowed to load the round register while the Filter A LF Interface™ will not be allowed to load the configuration register. However, the Filter A LF Interface™ will continue to function as if the write occurred.

TABLE 18. SELECT REGISTER LOADING FORMAT

	CFA/B11	CFA/B10	CFA/B9	CFA/B8	CFA/B7	CFA/B6	CFA/B5	CFA/B4	CFA/B3	CFA/B2	CFA/B1	CFA/B0
1st Word - Address	0	1	0	0	0	0	0	0	0	0	1	0
2nd Word - Data	0	0	0	0	0	0	0	0	1	1	1	1

TABLE 19. LIMIT REGISTER LOADING FORMAT

	CFA/B11	CFA/B10	CFA/B9	CFA/B8	CFA/B7	CFA/B6	CFA/B5	CFA/B4	CFA/B3	CFA/B2	CFA/B1	CFA/B0
1st Word - Address	1	1	1	0	0	0	0	0	0	1	1	1
2nd Word - Data	R	R	R	R	0	1	1	0	0	0	0	0
3rd Word - Data	R	R	R	R	0*	0	1	1	1	0	1	1
4th Word - Data	R	R	R	R	1	0	1	0	0	1	0	0
5th Word - Data	R	R	R	R	0**	1	1	1	0	0	1	0

R = Reserved. Must be set to "0".
* This bit represents the MSB of the Lower Limit.
** This bit represents the MSB of the Upper Limit.

Contact factory for additional information.

LF3330
Vertical Digital Image Filter

FEATURES

- 80 MHz Data Rate
- 12-bit Data and Coefficients
- On-board Memory for 256 Coefficient Sets
- LF Interface™ Allows All 256 Coefficient Sets to be Updated Within Vertical Blanking
- Selectable 16-bit Data Output with User-Defined Rounding and Limiting
- Seven 3K x 12-bit, Programmable Two-Mode Line Buffers
- 8 Filter Taps
- Cascadable for More Filter Taps
- Supports Interleaved Data Streams
- 3.3 Volt Power Supply
- 5 Volt I/O Tolerant
- Available 100% Screened to MIL-STD-883, Class B

DESCRIPTION

The **LF3330** filters digital images in the vertical dimension at real-time video rates. The input and coefficient data are both 12 bits and in two's complement format. The output is also in two's complement format and may be rounded to 16 bits.

The filter is an 8-tap FIR filter with all required line buffers contained on-chip. The line buffers can store video lines with lengths from 4 to 3076 pixels.

Multiple LF3330s can be cascaded together to create larger vertical filters.

Due to the length of the line buffers, interleaved data can be fed directly into the device and filtered without separating the data into individual data streams. The number of interleaved data sets that the device can handle is limited only by the length of the on-chip line buffers. If the interleaved video line has 3076 data values or less, the filter can handle it.

The LF3330 contains enough on-board memory to store 256 coefficient sets. The LF Interface™ allows all 256 coefficient sets to be updated within vertical blanking.

Selectable 16-bit data output with user-defined rounding and limiting minimizes the constraints put on coefficient sets for various filter implementations.

LF3330 BLOCK DIAGRAM

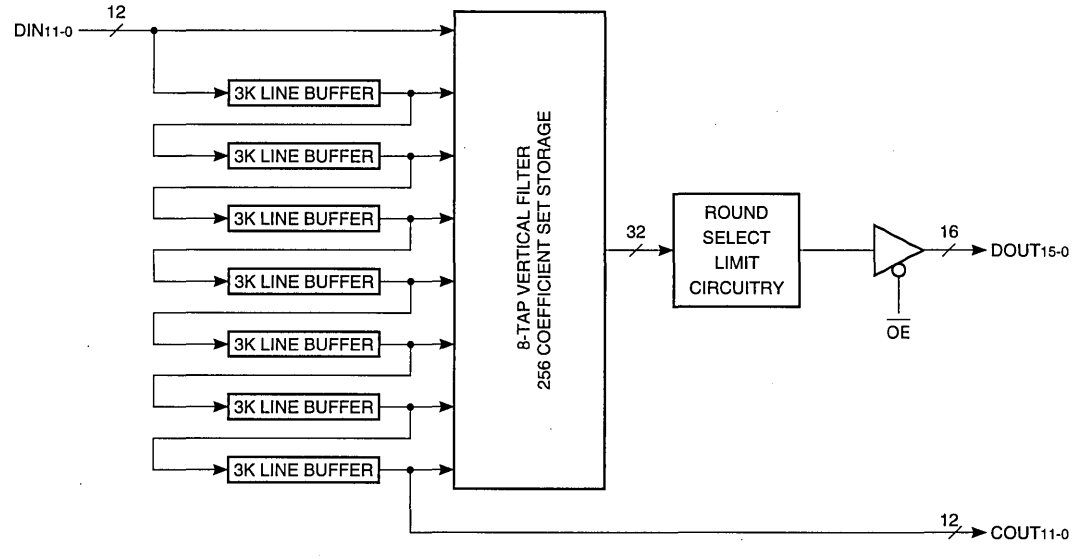
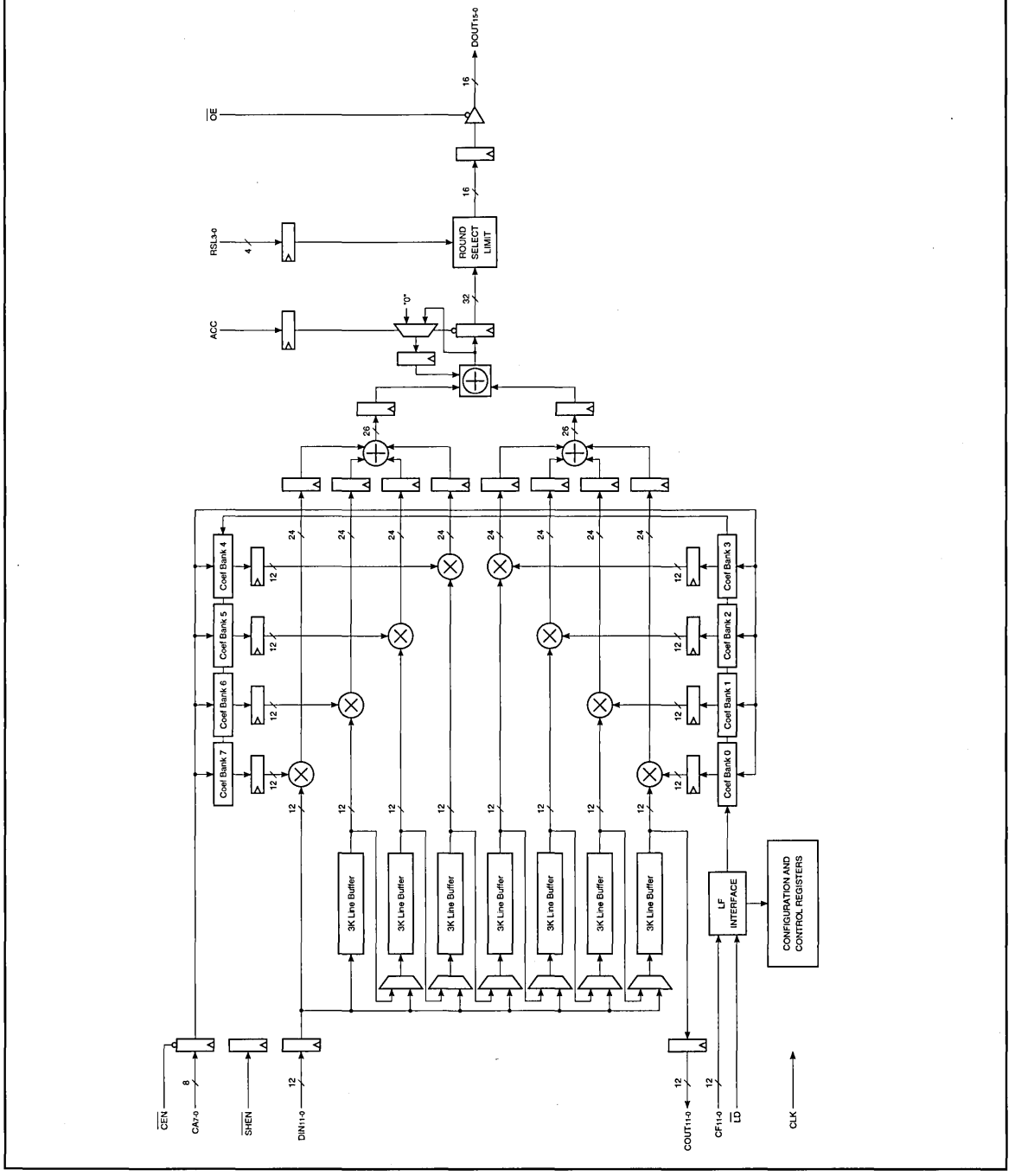


FIGURE 1. LF3330 FUNCTIONAL BLOCK DIAGRAM



SIGNAL DEFINITIONS

Power

VCC and GND

+3.3 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers.

Inputs

DIN11-0 — Data Input

DIN11-0 is the 12-bit registered data input port. Data is latched on the rising edge of CLK.

CF11-0 — Coefficient Input

CF11-0 is used to load data into the coefficient banks and configuration/control registers. Data present on CF11-0 is latched into the LF Interface™ on the rising edge of CLK when LD is LOW (see the LF Interface™ section for a full discussion).

CA7-0 — Coefficient Address

CA7-0 determines which row of data in the coefficient banks is fed to the multipliers. CA7-0 is latched into the Coefficient Address Register on the rising edge of CLK when CEN is LOW.

Outputs

DOUT15-0 — Data Output

DOUT15-0 is the 16-bit registered data output port.

COUT11-0 — Cascade Data Output

COUT11-0 is a 12-bit cascade output port. COUT11-0 on one device should be connected to DIN11-0 of another LF3330.

FIGURE 2. INPUT FORMATS

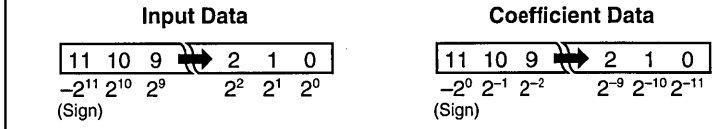


TABLE 1. OUTPUT FORMATS

SLCT4-0	S15	S14	S13	...	S8	S7	...	S2	S1	S0
00000	F15	F14	F13	...	F8	F7	...	F2	F1	F0
00001	F16	F15	F14	...	F9	F8	...	F3	F2	F1
00010	F17	F16	F15	...	F10	F9	...	F4	F3	F2
.	.	.	.		.	.		.	.	.
.	.	.	.		.	.		.	.	.
.	.	.	.		.	.		.	.	.
01110	F29	F28	F27	...	F22	F21	...	F16	F15	F14
01111	F30	F29	F28	...	F23	F22	...	F17	F16	F15
10000	F31	F30	F29	...	F24	F23	...	F18	F17	F16

Controls

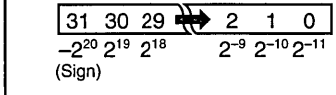
$\overline{LD}$ — Coefficient Load

When $\overline{LD}$ is LOW, data on CF11-0 is latched into the LF Interface™ on the rising edge of CLK. When $\overline{LD}$ is HIGH, data can not be latched into the LF Interface™. When enabling the LF Interface™ for data input, a HIGH to LOW transition of $\overline{LD}$ is required in order for the input circuitry to function properly. Therefore, $\overline{LD}$ must be set HIGH immediately after power up to ensure proper operation of the input circuitry (see the LF Interface™ section for a full discussion).

$\overline{CEN}$ — Coefficient Address Enable

When $\overline{CEN}$ is LOW, data on CA7-0 is latched into the Coefficient Address Register on the rising edge of CLK. When $\overline{CEN}$ is HIGH, data on CA7-0 is not latched and the register's contents will not be changed.

FIGURE 3. ACCUMULATOR FORMAT



ACC — Accumulator Control

When ACC is HIGH, the accumulator is enabled for accumulation and the accumulator output register is disabled for loading. When ACC is LOW, no accumulation is performed and the accumulator output register is enabled for loading. ACC is latched on the rising edge of CLK.

$\overline{SHEN}$ — Shift Enable

$\overline{SHEN}$ enables or disables the loading of data into the input/cascade registers and the line buffers. When $\overline{SHEN}$ is LOW, data is loaded into the input/cascade registers and shifted through the line

TABLE 2. CONFIGURATION REGISTER 0 – ADDRESS 200H

BITS	FUNCTION	DESCRIPTION
11-0	Line Buffer Length	See Line Buffer Description Section

TABLE 3. CONFIGURATION REGISTER 1 – ADDRESS 201H

BITS	FUNCTION	DESCRIPTION
0	Line Buffer Mode	0 : Delay Mode 1 : Recirculate Mode
1	Line Buffer Load	0 : Normal Load 1 : Parallel Load
11-2	Reserved	Must be set to "0"

TABLE 4. CONFIGURATION REGISTER 2 – ADDRESS 202H

BITS	FUNCTION	DESCRIPTION
0	Limit Enable	0 : Limiting Disabled 1 : Limiting Enabled
11-1	Reserved	Must be set to "0"

TABLE 5. CONFIGURATION REGISTER 3 – ADDRESS 203H

BITS	FUNCTION	DESCRIPTION
0	Cascade Mode	0 : First Device 1 : Cascaded Device
11-1	Reserved	Must be set to "0"

buffers on the rising edge of CLK. When $\overline{SHEN}$ is HIGH, data can not be loaded into the input/cascade registers or shifted through the line buffers and thier contents will not be changed.

RSL_{3-0} — Round/Select/Limit Control

RSL_{3-0} determines which of the sixteen user-programmable round/select/limit registers are used in the round/select/limit circuitry. A value of 0 on RSL_{3-0} selects round/select/limit register 0. A value of 1 selects round/select/limit register 1 and so on. RSL_{3-0} is latched on the rising edge of CLK (see the round, select, and limit sections for a complete discussion).

$\overline{OE}$ — Output Enable

When $\overline{OE}$ is LOW, $DOUT_{15-0}$ is enabled for output. When $\overline{OE}$ is HIGH, $DOUT_{15-0}$ is placed in a high-impedance state.

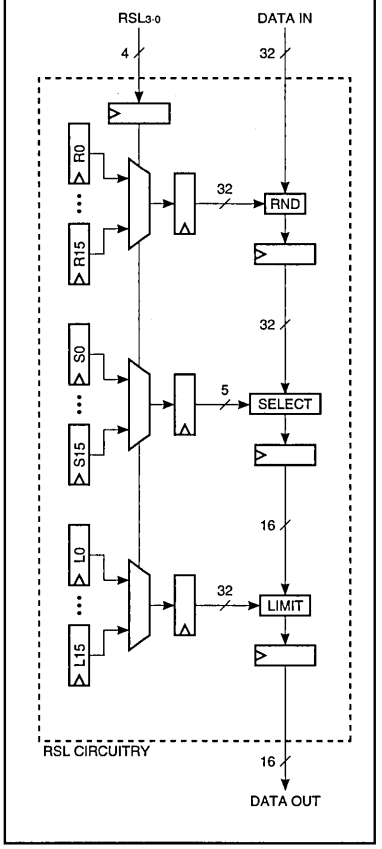
FUNCTIONAL DESCRIPTION

Line Buffers

The maximum delay length of each line buffer is 3076 cycles and the minimum is 4 cycles. Configuration Register 0 (CR_0) determines the delay length of the line buffers. The line buffer length is equal to the value of CR_0 plus 4. A value of 0 for CR_0 sets the line buffer length to 4. A value of 3072 for CR_0 sets the line buffer length to 3076. Any values for CR_0 greater than 3072 are not valid.

The line buffers have two modes of operation: delay mode and recirculate mode. Bit 0 of Configuration Register 1 determines which mode the line buffers are in. In delay mode, the data input to the line buffer is delayed by an amount determined by CR_0. In recirculate mode, the output of the line buffer is routed back to the input of the line buffer allowing the line buffer contents to be read multiple times.

FIGURE 4. RSL CIRCUITRY



Bit 1 of Configuration Register 1 allows the line buffers to be loaded in parallel. When Bit 1 is "1", the input register (DIN_{11-0}) loads all seven line buffers in parallel. This allows all the line buffers to be preloaded with data in the amount of time it normally takes to load a single line buffer.

Interleaved Data

The LF3330 is capable of handling interleaved data. The number of data sets it can handle is determined by the number of data values contained in a video line. If the interleaved video line has 3076 data values or less, the LF3330 can handle it no matter how many data sets are interleaved together.

Cascading

A cascade port is provided to allow cascading of multiple devices for more filter taps (see Figure 5). COUT11-0 of one device should be connected to DIN11-0 of another device. As many LF3330s as desired may be cascaded together. However, the outputs of the LF3330s must be added together with external adders.

The first line buffer on a cascaded device must have its length shortened by two delays. This is to account for the added delays of the input register on the device and the cascade output register from the previous LF3330. If Bit 0 of Configuration Register 3 is set to "1", the length of the first line buffer will be reduced by two. This will make its effective length the same as the other line buffers on the device. If Bit 0 of Configuration Register 3 is set to "0", the length of the first line buffer will be the same as the other line buffers. When cascading devices, the first LF3330 should have Bit 0 of Configuration Register 3 set to "0". Any LF3330s cascaded after the first LF3330 should have Bit 0 of Configuration Register 3 set to "1". When not cascading, Bit 0 of Configuration Register 3 should be set to "0".

It is important to note that the first multiplier on all cascaded devices should not be used. This is because the first multiplier does not have a line buffer in front of it. The coefficient value sent to the first multiplier on a cascaded device should be "0".

Rounding

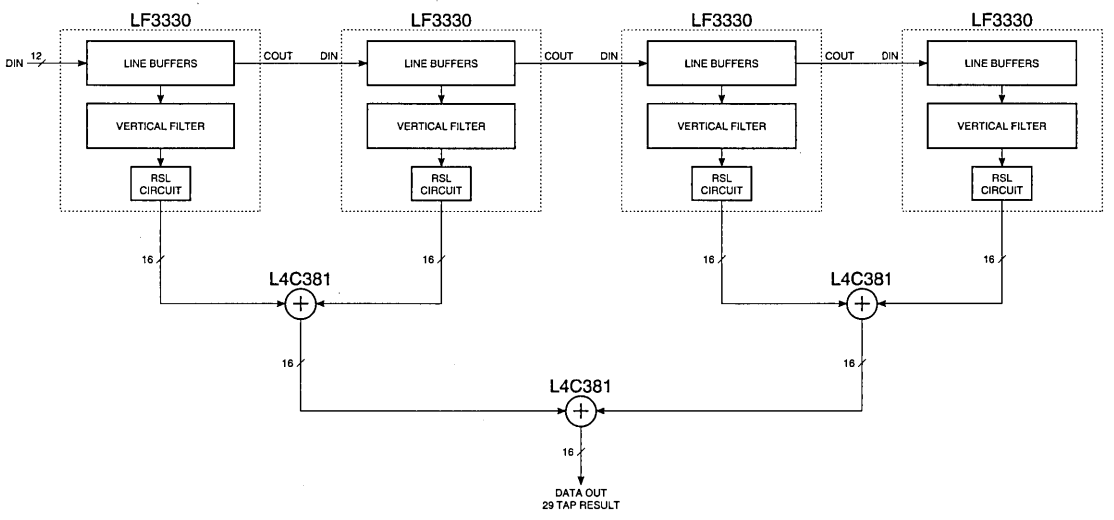
The filter output may be rounded by adding the contents of one of the sixteen round registers to the filter output (see Figure 4). Each round register is 32 bits wide and user-programmable. This allows the filter's output to be rounded to any precision required. Since any 32-bit value may be programmed into the round registers, the device can support complex rounding algorithms as well as standard Half-LSB rounding. RSL3-0 determines which of the sixteen round registers are used in the rounding operation. A value of 0 on RSL3-0 selects round register 0. A value of 1 selects round register 1 and so on. RSL3-0 may be changed every clock cycle if desired. This allows the rounding algorithm to be changed every clock cycle. This is useful when filtering interleaved data. If rounding is not desired, a round register should be loaded with 0 and selected as the register used for rounding. Round register loading is discussed in the LF Interface™ section.

Output Select

The word width of the filter output is 32 bits. However, only 16 bits may be sent to DOUT15-0. The select circuitry determines which 16 bits are passed (see Table 1). There are sixteen select registers which control the select circuitry. Each select register is 5 bits wide and user-programmable. RSL3-0 determines which of the sixteen select registers are used in the select circuitry. Select register 0 is chosen by loading a 0 on RSL3-0. Select register 1 is chosen by loading a 1 on RSL3-0 and so on. RSL3-0 may be changed every clock cycle if desired. This allows the 16-bit window to be changed every clock cycle. This is useful when filtering interleaved data. Select register loading is discussed in the LF Interface™ section.

2

FIGURE 5. MULTIPLE LF3330S CASCADED TOGETHER



Limiting

An output limiting function is provided for the output of the filter. The limit registers determine the valid range of output values when limiting is enabled (Bit 0 in Configuration Register 2). There are sixteen 32-bit limit registers. RSL3-0 determines which limit register is used during the limit operation. A value of 0 on RSL3-0 selects limit register 0. A value of 1 selects limit register 1 and so on. Each limit register contains both an upper and lower limit value. If the value fed to the limiting circuitry is less than the lower limit, the lower limit value is passed as the filter output. If the value fed to the limiting circuitry is greater than the upper limit, the upper limit value is passed as the filter output. RSL3-0 may be changed every clock cycle if desired. This allows the limit range to be changed every clock cycle. This is useful when filtering interleaved data. When loading limit values into the device, the upper limit must be greater than the lower limit. Limit register loading is discussed in the LF Interface™ section.

Coefficient Banks

The coefficient banks store the coefficients which feed into the multipliers in the filter. There is a separate bank for each multiplier. Each bank can hold 256 12-bit coefficients. The banks are loaded using the LF Interface™. Coefficient bank loading is discussed in the LF Interface™ section.

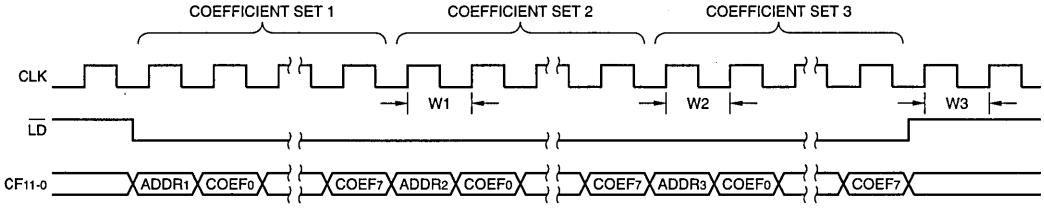
Configuration and Control Registers

The configuration registers determine how the LF3330 operates. Tables 2 through 5 show the formats of the four configuration registers. There are three types of control registers: round, select, and limit. There are sixteen round registers. Each round register is 32 bits wide. RSL3-0 determines which round register is used for rounding.

There are sixteen select registers. Each select register is 5 bits wide. RSL3-0 determines which select register is used for the select circuitry.

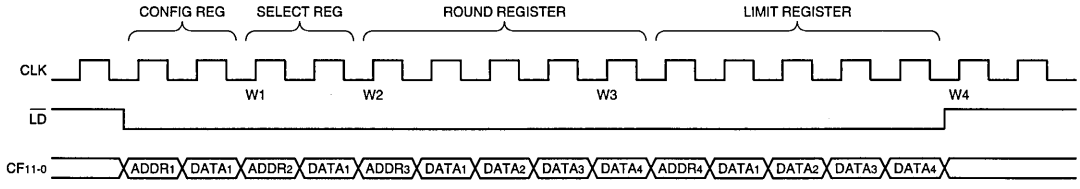
There are sixteen limit registers. Each limit register is 32 bits wide and stores both an upper and lower limit value. The lower limit is stored in bits 15-0 and the upper limit is stored in bits 31-16. RSL3-0 determines which limit register is used for limiting when limiting is enabled. Configuration and control register loading is discussed in the LF Interface™ section.

FIGURE 6. COEFFICIENT BANK LOADING SEQUENCE



W1: Coefficient Set 1 written to coefficient banks during this clock cycle.
W2: Coefficient Set 2 written to coefficient banks during this clock cycle.
W3: Coefficient Set 3 written to coefficient banks during this clock cycle.

FIGURE 7. CONFIGURATION/CONTROL REGISTER LOADING SEQUENCE



W1: Configuration Register loaded with new data on this rising clock edge.
W2: Select Register loaded with new data on this rising clock edge.
W3: Round Register loaded with new data on this rising clock edge.
W4: Limit Register loaded with new data on this rising clock edge.

LF Interface™

The LF Interface™ is used to load data into the coefficient banks and configuration/control registers. $\overline{LD}$ is used to enable and disable the LF Interface™. When $\overline{LD}$ goes LOW, the LF Interface™ is enabled for data input. The first value fed into the interface on CF_{11-0} is an address which determines what the interface is going to load. The three most significant bits (CF_{11-9}) determine if the LF Interface™ will load coefficient banks or configuration/control registers (see Table 6). The nine least significant bits (CF_{8-0}) are the address for whatever is to be loaded (see Tables 7 through 9). For example, to load address 15 of the coefficient banks, the first data value into the LF Interface™ should be 00FH. To load limit register 10, the first data value should be E0AH. The first address value should be loaded into the interface on the same clock cycle that latches the HIGH to LOW transition of $\overline{LD}$ (see Figures 6 and 7).

The next value(s) loaded into the interface are the data value(s) which will be stored in the bank or register defined by the address value. When loading coefficient banks, the interface will expect eight values to be loaded into the device after the address value. The eight values are coefficients 0 through 7. When loading configuration or select registers, the interface will expect one value after the address value. When loading round or limit registers, the interface will expect four values after the address value. Figures 6 and 7 show the data loading sequences for the coefficient banks and configuration/control registers.

Table 10 shows an example of loading data into the coefficient banks. The following data values are written into address 10 of coefficient banks 0 through 7: 210H, 543H, C76H, 9E3H, 701H, 832H, F20H, 143H. Table 11 shows an example of loading data

Table 6. CF_{11-9} Decode

11	10	9	DESCRIPTION
0	0	0	Coefficient Banks
0	0	1	Configuration Registers
0	1	1	Select Registers
1	0	1	Round Registers
1	1	1	Limit Registers

Table 7. Round Registers

REGISTER	ADDRESS (HEX)
0	A00
1	A01
•	•
•	•
•	•
14	A0E
15	A0F

Table 8. Select Registers

REGISTER	ADDRESS (HEX)
0	600
1	601
•	•
•	•
•	•
14	60E
15	60F

Table 9. Limit Registers

REGISTER	ADDRESS (HEX)
0	E00
1	E01
•	•
•	•
•	•
14	E0E
15	E0F

Table 10. Coefficient Bank Loading Format

	CF_{11}	CF_{10}	CF_9	CF_8	CF_7	CF_6	CF_5	CF_4	CF_3	CF_2	CF_1	CF_0
1st Word - Address	0	0	0	0	0	0	0	0	1	0	1	0
2nd Word - Bank 0	0	0	1	0	0	0	0	1	0	0	0	0
3rd Word - Bank 1	0	1	0	1	0	1	0	0	0	0	1	1
4th Word - Bank 2	1	1	0	0	0	1	1	1	0	1	1	0
5th Word - Bank 3	1	0	0	1	1	1	1	0	0	0	1	1
6th Word - Bank 4	0	1	1	1	0	0	0	0	0	0	0	1
7th Word - Bank 5	1	0	0	0	0	0	1	1	0	0	1	0
8th Word - Bank 6	1	1	1	1	0	0	1	0	0	0	0	0
9th Word - Bank 7	0	0	0	1	0	1	0	0	0	0	1	1

Table 11. Configuration Register Loading Format

	CF_{11}	CF_{10}	CF_9	CF_8	CF_7	CF_6	CF_5	CF_4	CF_3	CF_2	CF_1	CF_0
1st Word - Address	0	0	1	0	0	0	0	0	0	1	0	0
2nd Word - Data	0	0	0	0	0	0	0	0	0	0	1	1

into a configuration register. Data value 003H is written into Configuration Register 4. Table 12 shows an example of loading data into a round register. Data value 7683F4A2H is written into round register 12. Table 13 shows an example of loading data into a select register. Data value 00FH is loaded into select register 2. Table 14 shows an example of loading data into limit register 7. Data value 3B60H is loaded as the lower limit and 72A4H is loaded as the upper limit.

It takes 9S clock cycles to load S coefficient sets into the device. Therefore, it takes 2304 clock cycles to load all 256 coefficient sets. Assuming an 80 MHz clock rate, all 256 coefficient sets can be updated in 28.8 µs, which is well within vertical blanking time. It takes 5S clock cycles to load S round or limit registers. Therefore, it takes 160 clock cycles to update all round and limit registers. Assuming an 80 MHz clock rate, all round/limit registers can be updated in 2.0 µs.

The coefficient banks and configuration/control registers are not loaded with data until all data values for the specified address are loaded into the LF Interface™. In other words, the coefficient banks are not written to until all eight coefficients have been loaded into the LF Interface™. A round register is not written to until all four data values are loaded.

After the last data value is loaded, the interface will expect a new address value on the next clock cycle. After the next address value is loaded, data loading will begin again as previously discussed. As long as data is loaded into the interface, $\overline{LD}$ must remain LOW. After all desired coefficient banks and configuration/control registers are loaded with data, the LF Interface™ must be disabled. This is done by setting $\overline{LD}$ HIGH on the clock cycle after the clock cycle which latches the last data value. It is important that the LF Interface™ remain disabled when not loading data into it.

TABLE 12. ROUND REGISTER LOADING FORMAT

	CF_{11}	CF_{10}	CF_9	CF_8	CF_7	CF_6	CF_5	CF_4	CF_3	CF_2	CF_1	CF_0
1st Word - Address	1	0	1	0	0	0	0	0	1	1	0	0
2nd Word- Data	R	R	R	R	1	0	1	0	0	0	1	0*
3rd Word - Data	R	R	R	R	1	1	1	1	0	1	0	0
4th Word - Data	R	R	R	R	1	0	0	0	0	0	1	1
5th Word - Data	R	R	R	R	0**	1	1	1	0	1	1	0

R = Reserved. Must be set to "0".
* This bit represents the LSB of the Round Register.
** This bit represents the MSB of the Round Register.

TABLE 13. SELECT REGISTER LOADING FORMAT

	CF_{11}	CF_{10}	CF_9	CF_8	CF_7	CF_6	CF_5	CF_4	CF_3	CF_2	CF_1	CF_0
1st Word - Address	0	1	1	0	0	0	0	0	0	0	1	0
2nd Word - Data	0	0	0	0	0	0	0	0	1	1	1	1

TABLE 14. LIMIT REGISTER LOADING FORMAT

	CF_{11}	CF_{10}	CF_9	CF_8	CF_7	CF_6	CF_5	CF_4	CF_3	CF_2	CF_1	CF_0
1st Word - Address	1	1	1	0	0	0	0	0	0	1	1	1
2nd Word- Data	R	R	R	R	0	1	1	0	0	0	0	0
3rd Word - Data	R	R	R	R	0*	0	1	1	1	0	1	1
4th Word - Data	R	R	R	R	1	0	1	0	0	1	0	0
5th Word - Data	R	R	R	R	0**	1	1	1	0	0	1	0

R = Reserved. Must be set to "0".
* This bit represents the MSB of the Lower Limit.
** This bit represents the MSB of the Upper Limit.

Contact factory for additional information.

LF3347
High-Speed Image Filter with Coefficient RAM

FEATURES

- 80 MHz Data Input and Computation Rate
- Four 12 x 12-bit Multipliers with Individual Data and Coefficient Inputs
- Four 256 x 12-bit Coefficient Banks
- 32-bit Accumulator
- Selectable 16-bit Data Output with User-Defined Rounding and Limiting
- Two's Complement Operands
- 3.3 Volt Power Supply
- 5 Volt I/O Tolerant
- Package Styles Available:
  - 120-pin Plastic Quad Flatpack
  - 120-pin Ceramic PGA

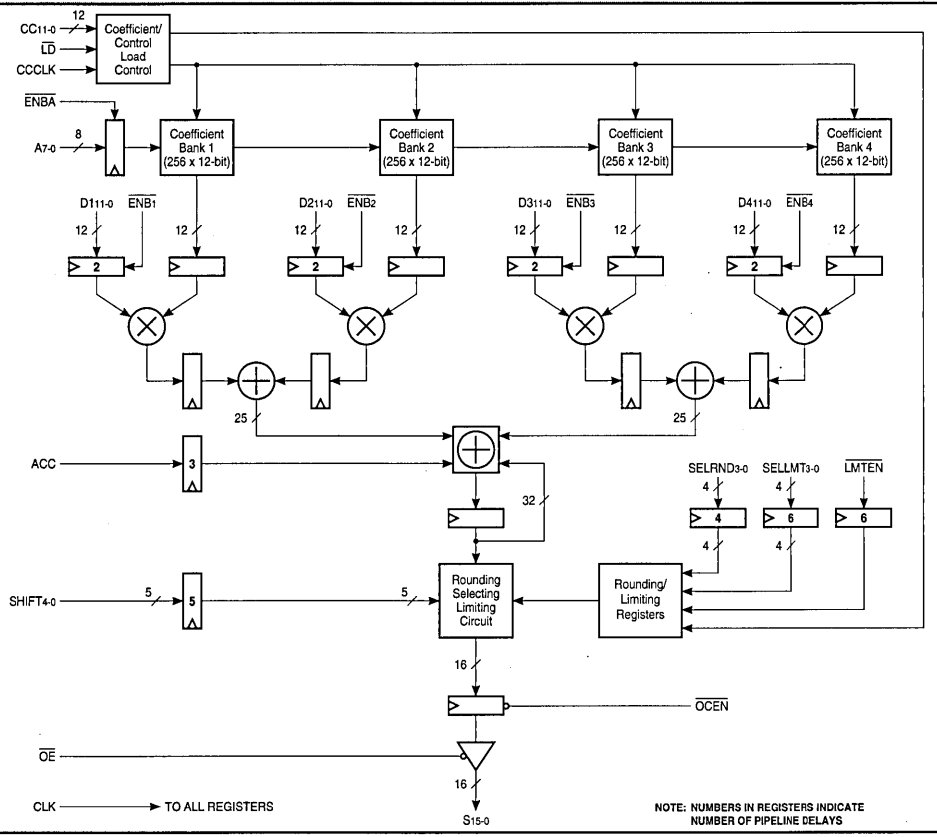
DESCRIPTION

The **LF3347** consists of an array of four 12 x 12-bit registered multipliers followed by two summers and a 32-bit accumulator. The LF3347 provides four 256 x 12-bit coefficient banks which are capable of storing 256 different sets of filter coefficients for the multiplier array. All multiplier data inputs are user accessible and can be updated every clock cycle with two's complement data. The pipelined architecture has fully registered input and output ports and an asynchronous three-state output enable control to simplify the design of complex systems.

A 32-bit accumulator allows cumulative word growth which may be internally rounded to 16-bits. Output data is updated every clock cycle and may be held under user control. The data inputs/outputs and control inputs are registered on the rising edge of CLK. The Control/Coefficient Data Input, *CC11-0*, is registered on the rising edge of CCCLK.

The LF3347 is ideal for performing pixel interpolation in image manipulation and filtering applications. The LF3347 can perform a bilinear interpolation of an image (4-pixel kernels) at real-time video rateswhen

LF3347 Block Diagram



used with an image resampling sequencer. Larger kernels or more complex functions can be realized by utilizing multiple devices.

Unrestricted access to all data ports and addressable coefficient banks provides the LF3347 with considerable flexibility in applications such as digital filters, adaptive FIR filters, mixers, and other similar systems requiring high-speed processing.

SIGNAL DEFINITIONS

Power

VCC and GND

+3.3 V power supply. All pins must be connected.

Clocks

CLK — Master Clock

The rising edge of CLK strobes all enabled registers.

CCCLK — Coefficient/Control Clock

When $\overline{LD}$ is LOW, the rising edge of CCCLK latches data on CC11-0 into the device.

Inputs

D111-0 – D411-0 — Data Input

D1–D4 are the 12-bit registered data input ports. Data is latched on the rising edge of CLK.

A7-0 — Row Address

A7-0 determines which row in the coefficient banks feed data to the multipliers. A7-0 is latched on the rising edge of CLK. When a new row address is loaded into the row address register, data from the coefficient banks will be latched into the multiplier input registers on the next rising edge of CLK.

FIGURE 1. INPUT FORMATS

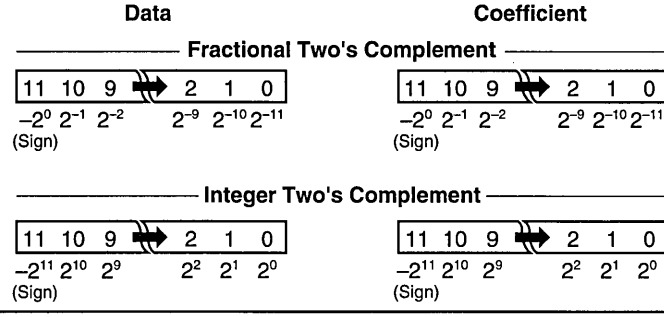


TABLE 1. OUTPUT FORMATS

SHIFT4-0	S15	S14	S13	• • •	S8	S7	• • •	S2	S1	S0
00000	F15	F14	F13	• • •	F8	F7	• • •	F2	F1	F0
00001	F16	F15	F14	• • •	F9	F8	• • •	F3	F2	F1
00010	F17	F16	F15	• • •	F10	F9	• • •	F4	F3	F2
•	•	•	•		•	•		•	•	•
•	•	•	•		•	•		•	•	•
•	•	•	•		•	•		•	•	•
01110	F29	F28	F27	• • •	F22	F21	• • •	F16	F15	F14
01111	F30	F29	F28	• • •	F23	F22	• • •	F17	F16	F15
10000	F31	F30	F29	• • •	F24	F23	• • •	F18	F17	F16

CC11-0 — Control/Coefficient Data Input

CC11-0 is used to load data into the coefficient banks and control registers. Data present on *CC11-0* is latched on the rising edge of CCCLK when $\overline{LD}$ is LOW.

Outputs

S15-0 — Data Output

S15-0 is the 16-bit registered data output port.

Controls

$\overline{ENB1}$–$\overline{ENB4}$ — Data Input Enables

The $\overline{ENBN}$ (N = 1, 2, 3, or 4) inputs allow the DN registers to be updated on each clock cycle. When $\overline{ENBN}$ is LOW, data on DN11-0 is latched into the DN register on the rising edge of CLK. When $\overline{ENBN}$ is HIGH, data on DN11-0 is not latched into the DN register and the register contents will not be changed.

$\overline{ENBA}$ — Row Address Input Enable

The $\overline{ENBA}$ input allows the row address register to be updated on each clock cycle. When $\overline{ENBA}$ is LOW, data on A7-0 is latched into the row address register on the rising edge of CLK. When $\overline{ENBA}$ is HIGH, data on A7-0 is not latched into the row address register and the register contents will not be changed.

$\overline{OE}$ — Output Enable

When $\overline{OE}$ is LOW, S15-0 is enabled for output. When $\overline{OE}$ is HIGH, S15-0 is placed in a high-impedance state.

TABLE 2. REGISTER FORMATS

Register	Load Address	Bits	Register Description	A7-0	SELRND3-0	SELLMT3-0
CS0	000H	11-0	Coefficient Set 0	00H		
CS1	001H	11-0	Coefficient Set 1	01H		
:	:	:	:	:		
CS255	0FFH	11-0	Coefficient Set 255	FFH		
RND0	800H	31-0	Rounding Register 0		0 0 0 0	
RND1	801H	31-0	Rounding Register 1		0 0 0 1	
:	:	:	:		:	
RND15	80FH	31-0	Rounding Register 15		1 1 1 1	
LMT0	C00H	31-16/15-0	Upper / Lower Limit Register 0			0 0 0 0
LMT1	C01H	31-16/15-0	Upper / Lower Limit Register 0			0 0 0 1
:	:	:	:			:
LMT15	C0FH	31-16/15-0	Upper / Lower Limit Register 15			1 1 1 1

2

$\overline{OCEN}$ — Output Clock Enable

When $\overline{OCEN}$ is LOW, the output register is enabled for data loading. When $\overline{OCEN}$ is HIGH, output register loading is disabled and the register's contents will not change.

ACC — Accumulator Control

The ACC input determines whether internal accumulation is performed. If ACC is LOW, no accumulation is performed, the prior accumulated sum is cleared, and the current sum of products is output. When ACC is HIGH, the emerging product is added to the sum of the previous products.

$\overline{LD}$ — Load Control

$\overline{LD}$ enables the loading of data into the coefficient banks and control registers (control registers are the round and limit registers). When $\overline{LD}$ is LOW, data on CC11-0 is latched into the device on the rising edge of CCCLK. When $\overline{LD}$ is HIGH, data cannot be loaded into the coefficient banks and control registers. When enabling the input circuitry for data loading, the LF3347 requires a HIGH to LOW transition of $\overline{LD}$ in order to function properly. Therefore, $\overline{LD}$ needs to be set HIGH immediately after power up to ensure proper operation of the input circuitry.

It takes five CCCLK clock cycles to load one coefficient set into the four coefficient banks or to load one control register. When the input circuitry is enabled ($\overline{LD}$ goes LOW), the first value loaded into the device on CC11-0 is an address which determines what will be loaded (see Table 2). The next four values loaded on CC11-0 is the data to be loaded into the coefficient banks or control register (see Tables 3-5). After the last data value is loaded, another coefficient bank address or control register may be loaded by feeding another address into CC11-0. When all desired coefficient banks and control registers are loaded, the input circuitry must be disabled by setting $\overline{LD}$ HIGH.

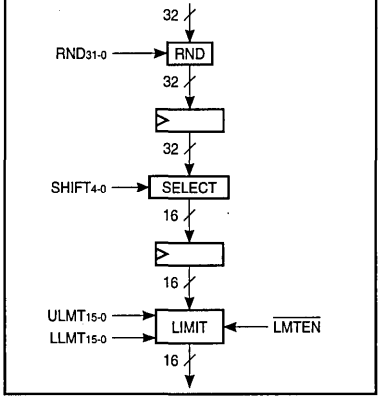
SELRND3-0 — Round Select

SELRND3-0 allows the user to select which rounding register will be used in the rounding circuit to round / offset the data.

SHIFT4-0 — Shift

SHIFT4-0 determines which 16-bits of the 32-bits from the accumulator are passed to the output (see Table 1).

FIGURE 2. ROUNDING, SELECTING, LIMITING CIRCUITRY



SELLMT3-0 — Limit Select

SELLMT3-0 allows the user to control which limiting register will be used in the limiting circuit to set the upper and lower limits on the data.

$\overline{LMTEN}$ — Limit Enable

When $\overline{LMTEN}$ is LOW, limiting is enabled and the selected limit register is used to determine the valid range of output values for the overall filter. When HIGH, limiting is disabled.

FUNCTIONAL DESCRIPTION

Coefficient Banks

The LF3347 has four coefficient banks which feed coefficient values to the multipliers. Each bank can store 256 12-bit coefficients. In the example shown in Table 3, address 10 in coefficient banks 1 through 4 is loaded with the following values: ABCH, 789H, 456H, 123H. The coefficient banks are not written to until all four coefficients have been loaded into the device.

A_{7-0} determines which coefficient set is sent to the multipliers. A value of 0 on A_{7-0} selects set 0. A value of 1 selects set 1 and so on.

Rounding/Offset

The accumulator output may be rounded before being sent to the output select section. Rounding is user-selectable and is accomplished by adding the contents of a round register to the accumulator output (see Figure 2). There are sixteen 32-bit round registers. In the example in Table 4, round register 10 is loaded with 76543210H. A round register is not written to until all four data values have been loaded into the device.

$SELRND_{3-0}$ determines which round register is used for rounding. A value of 0 on $SELRND_{3-0}$ selects round register 0. A value of 1 selects round register 1 and so on. If rounding is not desired, a round register should be loaded with 0 and selected as the register for rounding.

Output Select

The filter output word width is 32-bits. However, only 16-bits may be sent to the device output. SHIFT4-0 determines which 16 bits are passed to the device output (See Table 1).

Output Limiting

An output limiting function is provided for the output of the filter. When limiting is enabled ($\overline{LMTEN}$ LOW), the limit register selected with $SELLMT_{3-0}$ determines the valid range of output values for the overall filter. There are sixteen 32-bit limit registers. Each limit register contains both an upper and lower limit value. The lower limit is stored in bits 15-0 and the upper limit is stored in bits 31-16. If the value fed to the limiting circuitry is less than the lower limit, the lower limit is passed to the device output. If the value fed to the limiting circuitry is greater than the upper limit, the upper limit is passed to the device output. When loading limit values into the device, the upper limit must be greater than the lower limit. In the example shown in Table 4, limit register 15 is loaded with a lower limit of 0123H and an upper limit of 7FEDH. A limit register is not written to until all four data values have been loaded into the device.

$SELLMT_{3-0}$ determines which limit register is used for limiting. A value of 0 on $SELLMT_{3-0}$ selects limit register 0. A value of 1 selects limit register 1 and so on.

TABLE 3. COEFFICIENT BANK LOADING FORMAT

	CC_{11}	CC_{10}	CC_9	CC_8	CC_7	CC_6	CC_5	CC_4	CC_3	CC_2	CC_1	CC_0
1st Word Address	0	0	0	0	0	0	0	0	1	0	1	0
2nd Word Bank 1	1	0	1	0	1	0	1	1	1	1	0	0
3rd Word Bank 2	0	1	1	1	1	0	0	0	1	0	0	1
4th Word Bank 3	0	1	0	0	0	1	0	1	0	1	1	0
5th Word Bank 4	0	0	0	1	0	0	1	0	0	0	1	1

TABLE 4. ROUND REGISTER LOADING FORMAT

	CC_{11}	CC_{10}	CC_9	CC_8	CC_7	CC_6	CC_5	CC_4	CC_3	CC_2	CC_1	CC_0
1st Word Address	1	0	0	0	0	0	0	0	1	0	1	0
2nd Word	R	R	R	R	0	0	0	1	0	0	0	*0
3rd Word	R	R	R	R	0	0	1	1	0	0	1	0
4th Word	R	R	R	R	0	1	0	1	0	1	0	0
5th Word	R	R	R	R	**0	1	1	1	0	1	1	0

R = Reserved. Must be set to "0".
* This bit represents the LSB of the Round Register.
** This bit represents the MSB of the Round Register.

TABLE 5. LIMIT REGISTER LOADING FORMAT

	CC_{11}	CC_{10}	CC_9	CC_8	CC_7	CC_6	CC_5	CC_4	CC_3	CC_2	CC_1	CC_0
1st Word Address	1	1	0	0	0	0	0	0	1	1	1	1
2nd Word	R	R	R	R	0	0	1	0	0	0	1	1
3rd Word	R	R	R	R	*0	0	0	0	0	0	0	1
4th Word	R	R	R	R	1	1	1	0	1	1	0	1
5th Word	R	R	R	R	**0	1	1	1	1	1	1	1

R = Reserved. Must be set to "0".
* This bit represents the MSB of the Lower Limit Register.
** This bit represents the MSB of Upper Limit Register.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to 5.5 V
Signal applied to high impedance output	–0.5 V to 5.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA
ESD (MIL-STD-883D METHOD 3015.7)	> 2000 V

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	3.00 V ≤ V_{CC} ≤ 3.60 V
Active Operation, Military	–55°C to +125°C	3.00 V ≤ V_{CC} ≤ 3.60 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			150	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			2	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

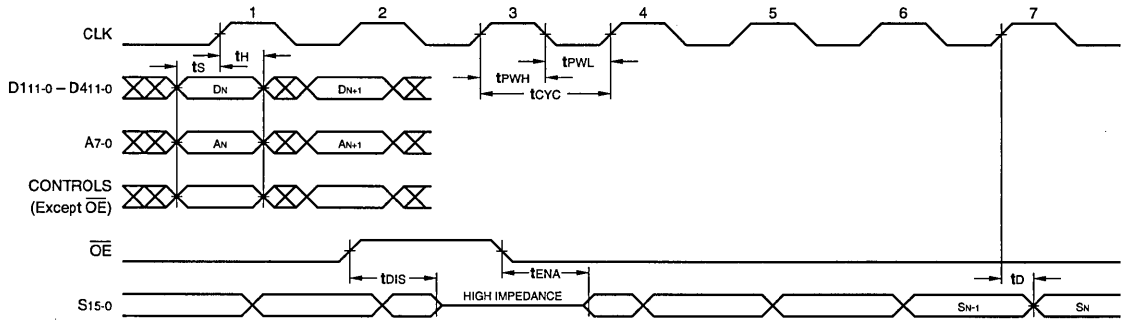
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF3347–					
		25		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	25		15		12	
t_{PWL}	Clock Pulse Width Low	10		7		5	
t_{PWH}	Clock Pulse Width High	10		7		5	
t_S	Input Setup Time	8		5		3	
t_H	Input Hold Time	0		0		0	
t_D	Output Delay		13		10		8
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		12		10
t_{ENA}	Three-State Output Enable Delay (Note 11)		13		11		8

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF3347–					
		25		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	25		15		12	
t_{PWL}	Clock Pulse Width Low	10		7		5	
t_{PWH}	Clock Pulse Width High	10		7		5	
t_S	Input Setup Time	8		5		3	
t_H	Input Hold Time	0		0		0	
t_D	Output Delay		13		10		8
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		12		10
t_{ENA}	Three-State Output Enable Delay (Note 11)		13		11		8

SWITCHING WAVEFORMS: DATA I/O



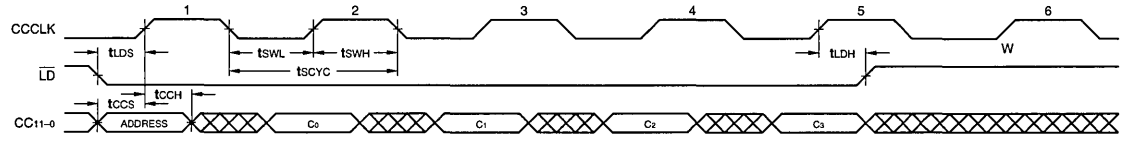
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF3347–					
		25		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
tCCCYC	Control Coefficient Interface Cycle Time	25		15		12	
tCCWL	Control Coefficient Clock Pulse Width Low	10		7		5	
tCCWH	Control Coefficient Clock Pulse Width High	10		7		5	
tCCENS	Control Coefficient Enable Setup Time	8		5		3	
tCCENH	Control Coefficient Enable Hold Time	0		0		0	
tCCS	Control Coefficient Data Input Setup Time	8		5		5	
tCCH	Control Coefficient Data Input Hold Time	0		0		0	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF3347–					
		25		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
tCCCYC	Control Coefficient Interface Cycle Time	25		15		12	
tCCWL	Control Coefficient Clock Pulse Width Low	10		7		5	
tCCWH	Control Coefficient Clock Pulse Width High	10		7		5	
tCCENS	Control Coefficient Enable Setup Time	8		5		3	
tCCENH	Control Coefficient Enable Hold Time	0		0		0	
tCCS	Control Coefficient Data Input Setup Time	8		5		5	
tCCH	Control Coefficient Data Input Hold Time	0		0		0	

SWITCHING WAVEFORMS: COEFFICIENT BANK AND CONTROL REGISTER INPUT



W: Configuration Banks/Control Registers written to on this clock cycle.

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at −0.6 V. The device can withstand indefinite operation with inputs or outputs in the range of −0.5 V to +5.5 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 30 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages on a test fixture should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.0 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

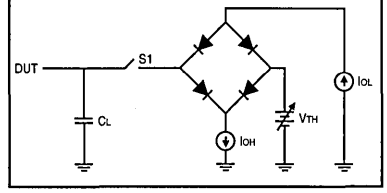
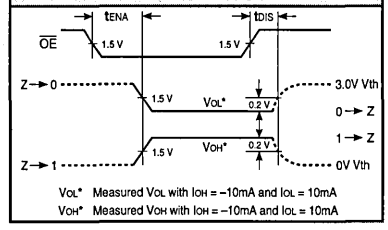
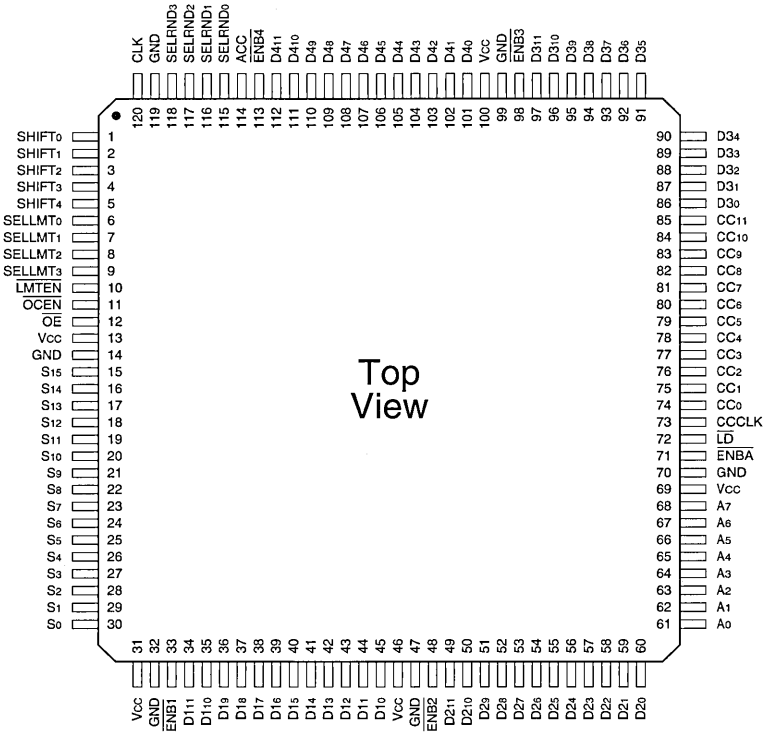


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

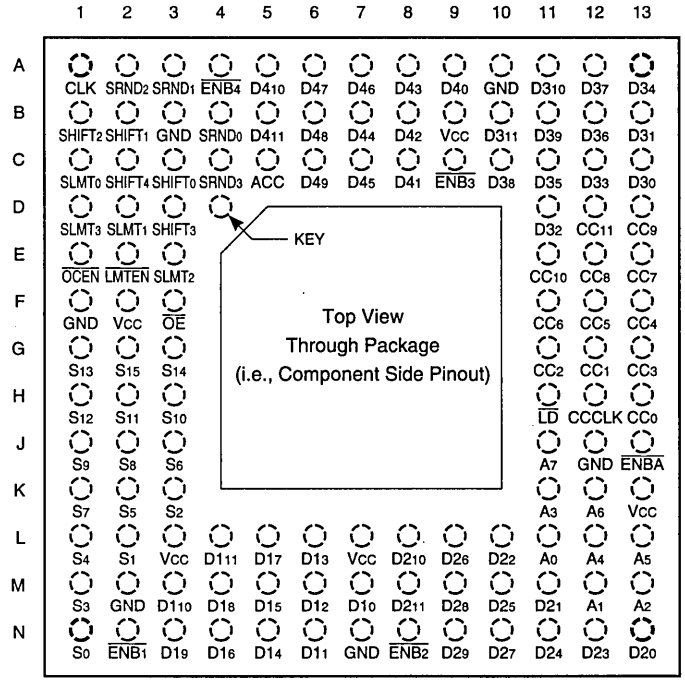
120-pin



Speed	Plastic Quad Flatpack (Q1)
	0°C to +70°C—COMMERCIAL SCREENING
25 ns	LF3347QC25
15 ns	LF3347QC15
12 ns	LF3347QC12

ORDERING INFORMATION

120-pin



Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C—COMMERCIAL SCREENING
25 ns	LF3347GC25
15 ns	LF3347GC15
12 ns	LF3347GC12
	–55°C to +125°C—COMMERCIAL SCREENING
25 ns	LF3347GM25
15 ns	LF3347GM15
12 ns	LF3347GM12
	–55°C to +125°C—MIL-STD-883 COMPLIANT
25 ns	LF3347GMB25
15 ns	LF3347GMB15
12 ns	LF3347GMB12

LF43168
Dual 8-Tap FIR Filter

FEATURES

- 66 MHz Data and Computation Rate
- Two Independent 8-Tap or Single 16-Tap FIR Filters
- 10-bit Data and Coefficient Inputs
- 32 Programmable Coefficient Sets
- Supports Interleaved Coefficient Sets
- User Programmable Decimation up to 16:1
- Maximum of 256 FIR Filter Taps, 16 x 16 2-D Kernels, or 10 x 20-bit Data and Coefficients
- Replaces Harris HSP43168
- DECC SMD No. 5962-97504
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 84-pin Plastic LCC, J-Lead
  - 100-pin Plastic Quad Flatpack
  - 84-pin Ceramic PGA

DESCRIPTION

The **LF43168** is a high-speed dual FIR filter capable of filtering data at real-time video rates. The device contains two FIR filters which may be used as two separate filters or cascaded to form one filter. The input and coefficient data are both 10-bits and can be in unsigned, two's complement, or mixed mode format.

The filter architecture is optimized for symmetric coefficient sets. When symmetric coefficient sets are used, each filter can be configured as an 8-tap FIR filter. If the two filters are cascaded, a 16-tap FIR filter can be implemented. When asymmetric coefficient sets are used, each filter is configured as a 4-tap FIR filter. If both filters are cascaded, an 8-tap filter can be implemented. The LF43168 can decimate the output data by as much as 16:1. When the device is programmed to decimate, the number of clock cycles available to calculate filter taps increases. When configured for 16:1 decimation, each filter can be configured as a 128-tap FIR filter (if symmetric coefficient sets are used). By cascading these two filters, the device can be configured as a 256-tap FIR filter.

There is on-chip storage for 32 different sets of coefficients. Each set consists of eight coefficients. Access to more than one coefficient set facilitates adaptive filtering operations. The 28-bit filter output can be rounded from 8 to 19 bits.

LF43168 Block Diagram

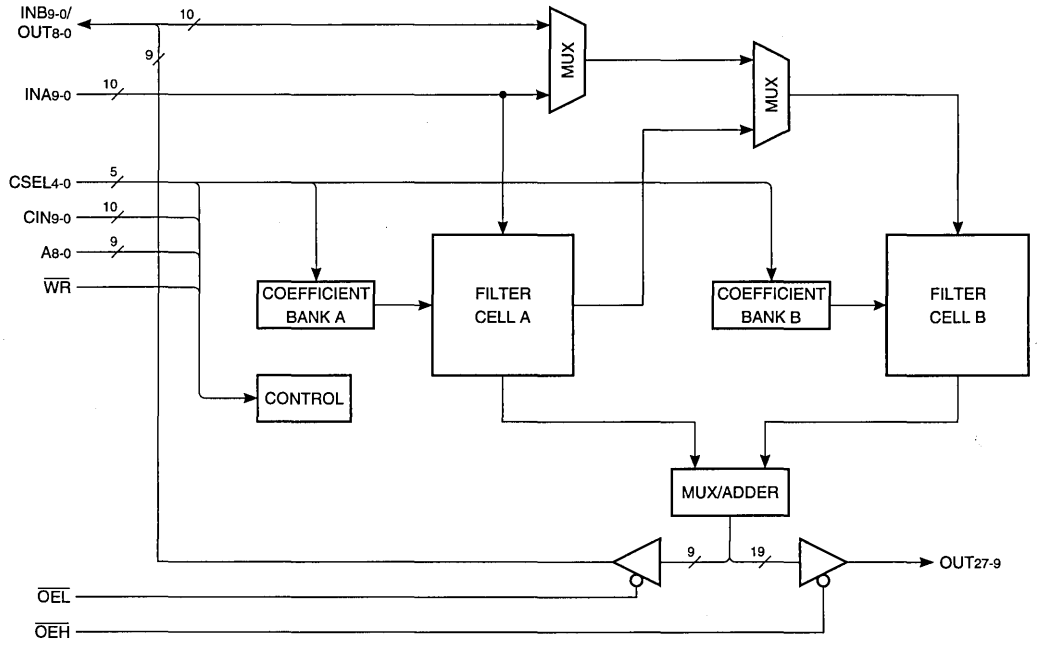
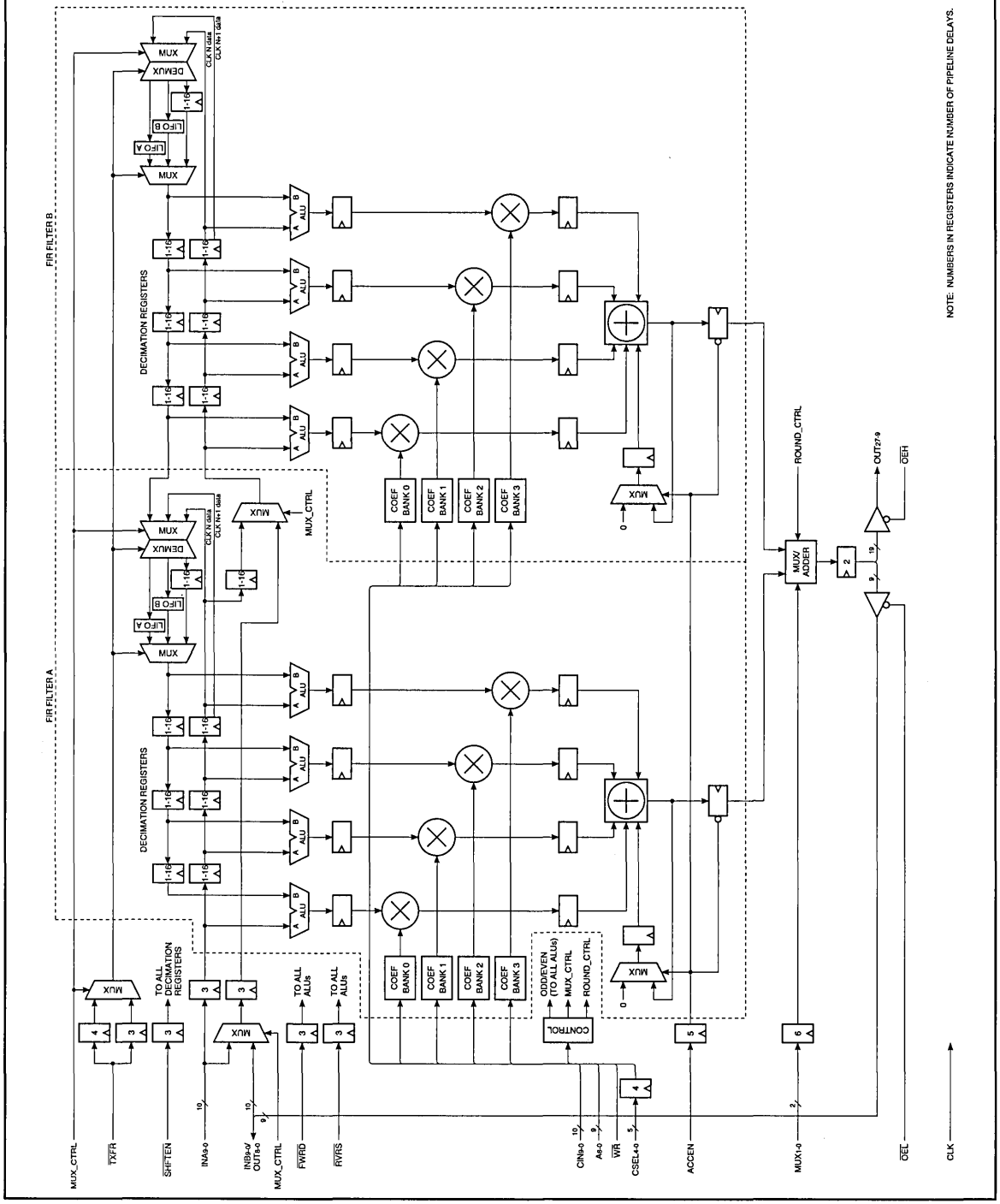


FIGURE 1. LF43168 FUNCTIONAL BLOCK DIAGRAM



SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers.

Inputs

INA9-0 — Data Input (FIR Filter A)

INA9-0 is the 10-bit registered data input port for FIR Filter A. INA9-0 can also be used to send data to FIR Filter B. Data is latched on the rising edge of CLK.

INB9-0 — Data Input (FIR Filter B)

INB9-0 is the 10-bit registered data input port for FIR Filter B. Data is latched on the rising edge of CLK. INB9-1 is also used as OUT8-0, the nine least significant bits of the data output port (see OUT27-0 section).

CIN9-0 — Coefficient/Control Data Input

CIN9-0 is the data input port for the coefficient and control registers. Data is latched on the rising edge of $\overline{WR}$.

A8-0 — Coefficient/Control Address

A8-0 provides the write address for data on CIN9-0. Data is latched on the falling edge of $\overline{WR}$.

$\overline{WR}$ — Coefficient/Control Write

The rising edge of $\overline{WR}$ latches data on CIN9-0 into the coefficient/control register addressed by A8-0.

CSEL4-0 — Coefficient Select

CSEL4-0 determines which set of coefficients is sent to the multipliers in both FIR filters. Data is latched on the rising edge of CLK.

FIGURE 2A. INPUT FORMATS

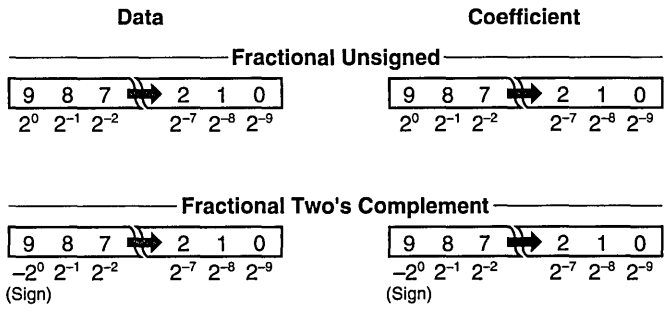
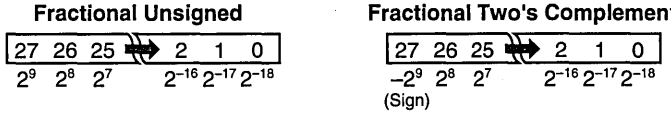


FIGURE 2B. OUTPUT FORMATS



Outputs

OUT27-0 — Data Output

OUT27-0 is the 28-bit registered data output port. OUT8-0 is also used as INB9-1, the nine most significant bits of the FIR Filter B data input port (see INB9-0 section). If both filters are configured for even-symmetric coefficients, and both input and coefficient data is unsigned, the filter output data will be unsigned. Otherwise, the output data will be in two's complement format.

Controls

$\overline{SHFTEN}$ — Shift Enable

When $\overline{SHFTEN}$ is LOW, data on INA9-0 and INB9-0 can be latched into the device and data can be shifted through the decimation registers. When $\overline{SHFTEN}$ is HIGH, data on INA9-0 and INB9-0 can not be latched into the device and data in the input and decimation registers is held. This signal is latched on the rising edge of CLK.

$\overline{FWRD}$ — Forward ALU Input

When $\overline{FWRD}$ is LOW, data from the forward decimation path is sent to the "A" inputs on the ALUs. When $\overline{FWRD}$ is HIGH, "0" is sent to the "A" inputs on the ALUs. This signal is latched on the rising edge of CLK.

$\overline{RVRS}$ — Reverse ALU Input

When $\overline{RVRS}$ is LOW, data from the reverse decimation path is sent to the "B" inputs on the ALUs. When $\overline{RVRS}$ is HIGH, "0" is sent to the "B" inputs on the ALUs. This signal is latched on the rising edge of CLK.

$\overline{TXFR}$ — LIFO Transfer Control

When $\overline{TXFR}$ goes LOW, the LIFO sending data to the reverse decimation path becomes the LIFO receiving data from the forward decimation path, and the LIFO receiving data from the forward decimation path becomes the LIFO sending data to the reverse decimation path. The device must see a HIGH to LOW transition of $\overline{TXFR}$ in order to switch LIFOs. This signal is latched on the rising edge of CLK.

ACCEN — Accumulate Enable

When ACCEN is HIGH, both accumulators are enabled for accumulation and writing to the accumulator output registers is disabled (the registers hold their values). When ACCEN goes LOW, accumulation is halted (by sending zeros to the accumulator feedback inputs) and writing to the accumulator output registers is enabled. This signal is latched on the rising edge of CLK.

MUX1-0 — Mux/Adder Control

MUX1-0 controls the Mux/Adder as shown in Table 3. Data is latched on the rising edge of CLK.

$\overline{OEL}$ — Output Enable Low

When $\overline{OEL}$ is LOW, OUT8-0 is enabled for output and INB9-1 can not be used. When $\overline{OEL}$ is HIGH, OUT8-0 is placed in a high-impedance state and INB9-1 is available for data input.

$\overline{OEH}$ — Output Enable High

When $\overline{OEH}$ is LOW, OUT27-9 is enabled for output. When $\overline{OEH}$ is HIGH, OUT27-9 is placed in a high-impedance state.

TABLE 1. CONTROL REGISTER 0 – ADDRESS 000H

BITS	FUNCTION	DESCRIPTION
0–3	Decimation Factor/ Decimation Register Delay Length	0000 = No Decimation, Delay by 1 0001 = Decimate by 2, Delay by 2 0010 = Decimate by 3, Delay by 3 0011 = Decimate by 4, Delay by 4 0100 = Decimate by 5, Delay by 5 0101 = Decimate by 6, Delay by 6 0110 = Decimate by 7, Delay by 7 0111 = Decimate by 8, Delay by 8 1000 = Decimate by 9, Delay by 9 1001 = Decimate by 10, Delay by 10 1010 = Decimate by 11, Delay by 11 1011 = Decimate by 12, Delay by 12 1100 = Decimate by 13, Delay by 13 1101 = Decimate by 14, Delay by 14 1110 = Decimate by 15, Delay by 15 1111 = Decimate by 16, Delay by 16
4	Filter Mode Select	0 = Single Filter Mode 1 = Dual Filter Mode
5	Coefficient Symmetry Select	0 = Even-Symmetric Coefficients 1 = Odd-Symmetric Coefficients
6	FIR Filter A: Odd/Even Taps	0 = Odd Number of Filter Taps 1 = Even Number of Filter Taps
7	FIR Filter B: Odd/Even Taps	0 = Odd Number of Filter Taps 1 = Even Number of Filter Taps
8	FIR Filter B Input Source	0 = Input from INA9-0 1 = Input from INB9-0
9	Interleaved/Non-Interleaved Coefficient Sets	0 = Non-Interleaved Coefficient Sets 1 = Interleaved Coefficient Sets

FUNCTIONAL DESCRIPTION

Control Registers

There are two control registers which determine how the LF43168 is configured. Tables 1 and 2 show how each register is organized. Data on CIN9-0 is latched into the addressed control register on the rising edge of $\overline{WR}$. Address data is input on A8-0. Control Register 0 is written to using address 000H. Control Register 1 is written to using address 001H (Note that addresses 002H to 0FFH are reserved and should not be written to). When a control register is written to, a reset occurs which lasts for 6 CLK cycles from when $\overline{WR}$ goes HIGH. This reset does not alter any data in the coefficient banks. Control data can be loaded asynchronously to CLK.

Bits 0-3 of Control Register 0 control the decimation registers. The decimation factor and decimation register delay length is set using these bits. Bit 4 determines if FIR filters A and B operate separately as two filters or together as one filter. Bit 5 is used to select even or odd-symmetric coefficients. Bits 6 and 7 determine if there are an even or odd number of taps in filters A and B respectively. When the FIR filters are set to operate as two separate filters, bit 8 selects either INA9-0 or INB9-0 as the filter B input source. Bit 9 determines if the coefficient set used is interleaved or non-interleaved (see Interleaved Coefficient Filters section). Most applications use non-interleaved coefficient sets (bit 9 set to "0").

Bits 0 and 1 of Control Register 1 determine the input and coefficient data formats respectively for filter A. Bits 2 and 3 determine the input and coefficient data formats respectively for filter B. Bit 4 is used to enable or disable data reversal on the reverse decimation path. When data reversal is enabled, the data order is reversed before being sent to the reverse decimation path. Bits 5-8 select where rounding will occur on the output data (See Mux/Adder section). Bit 9 enables or disables output rounding.

Coefficient Banks

The coefficient banks supply coefficient data to the multipliers in both FIR filters. The LF43168 can store 32 different coefficient sets. A coefficient

Table 2. Control Register 1 – Address 001H

BITS	FUNCTION	DESCRIPTION
0	FIR Filter A Input Data Format	0 = Unsigned 1 = Two's Complement
1	FIR Filter A Coefficient Format	0 = Unsigned 1 = Two's Complement
2	FIR Filter B Input Data Format	0 = Unsigned 1 = Two's Complement
3	FIR Filter B Coefficient Format	0 = Unsigned 1 = Two's Complement
4	Data Order Reversal Enable	0 = Enabled 1 = Disabled
5–8	Output Round Position	0000 = 2^{-10} 0001 = 2^{-9} 0010 = 2^{-8} 0011 = 2^{-7} 0100 = 2^{-6} 0101 = 2^{-5} 0110 = 2^{-4} 0111 = 2^{-3} 1000 = 2^{-2} 1001 = 2^{-1} 1010 = 2^{0} 1011 = 2^{1}
9	Output Round Enable	0 = Enabled 1 = Disabled

set consists of 8 coefficient values. Each bank can hold 32 10-bit values. CSEL4-0 is used to select which coefficient set is sent to the filter multipliers. The coefficient set fed to the multipliers may be switched every CLK cycle if desired.

Data on CIN9-0 is latched into the addressed coefficient bank on the rising edge of $\overline{WR}$. Address data is input on A8-0 and is decoded as follows: A1-0 determines the bank number ("00", "01", "10", and "11" correspond to banks 0, 1, 2, and 3 respectively), A2 determines which filter ("0" = filter A, "1" = filter B), A7-3 determines which set number the coefficient is in, and A8 must be set to "1". For example, an address of "100111011" will load coefficient set 7 in bank 3 of filter A with data. Coefficient data can be loaded asynchronously to CLK.

Decimation Registers

The decimation registers are provided to take advantage of symmetric filter coefficients and to provide data storage for 2-D filtering. The outputs of the registers are fed into the ALUs. Both inputs to an ALU need to be multiplied by the same filter coefficient. By adding or subtracting the two data inputs together before being sent to the filter multiplier, the number of filter taps needed is cut in half. Therefore, an 8-tap FIR filter can be made with only four multipliers. The decimation registers are divided into two groups, the forward and reverse decimation registers. As can be seen in Figure 1, data flows left to right through the forward decimation registers and right to left through the reverse decimation registers. The decimation registers can be programmed to decimate by 2 to 16 (see Decimation section and Table 1). $\overline{SHFTEN}$ enables and disables the shifting of data through the decimation registers. When $\overline{SHFTEN}$ is LOW, data on INA9-0 and INB9-0 can be latched into the device and data can be shifted through the decimation registers. When $\overline{SHFTEN}$ is HIGH, data on INA9-0 and INB9-0 can not be latched into the device and data in the input and decimation registers is held.

Data feedback circuitry is positioned between the forward and reverse decimation registers. It controls how data from the forward decimation path is fed to the reverse decimation path. The feedback circuitry can either reverse the data order or pass the data unchanged to the reverse decimation path. The mux/demux sends incoming data to one of the LIFOs or the data feedback decimation register. The LIFOs and decimation register feed into a mux. This mux determines if one of the LIFOs or the decimation register sends data to the reverse decimation path.

If the data order needs to be reversed before being sent to the reverse decimation path (for example, when decimating), Data Reversal Mode should be enabled by setting bit 4 of Control Register 1 to "0". When Data Reversal is enabled, data from the forward decimation path is written into one of the LIFOs in the data feedback section while the other LIFO sends data to the reverse decimation path. When $\overline{TXFR}$ goes LOW, the LIFO sending data to the reverse decimation path becomes the LIFO receiving data from the forward decimation path, and the LIFO receiving data from the forward decimation path becomes the LIFO sending data to the reverse decimation path. The device must see a HIGH to LOW transition of $\overline{TXFR}$ in order to switch LIFOs. The size of data blocks sent to the reverse decimation path is determined by how often $\overline{TXFR}$ goes LOW. To send data blocks of size 8 to

the reverse decimation path, $\overline{TXFR}$ would have to be set LOW once every 8 CLK cycles. Once a data block size has been established (by asserting $\overline{TXFR}$ at the proper frequency), changing the frequency or phase of $\overline{TXFR}$ assertion will cause unknown results.

If data should be passed to the reverse decimation path with the order unchanged, Data Reversal Mode should be disabled by setting bit 4 of Control Register 1 to "1" and $\overline{TXFR}$ must be set LOW. When Data Reversal is disabled, data from the forward decimation path is written into the data feedback decimation register. The output of this register sends data to the reverse decimation path. The delay length of this register is the same as the forward and reverse decimation register's delay length.

When the LF43168 is configured to operate as a single FIR filter, the forward and reverse decimation paths in filters A and B are cascaded together. The data feedback section in filter B routes data from the forward decimation path to the reverse decimation path. The configuration of filter B's feedback section determines how data is sent to the reverse decimation path. Data going through the feedback section in filter A is sent through the decimation register.

The point at which data from the forward decimation path is sent to the data feedback section is determined by whether the filter is set to have an even or odd number of filter taps. If the filter is set to have an even number of taps, the output of the third forward decimation register is sent to the feedback section. If the filter is set to have an odd number of taps, the data that will be output from the third forward decimation register on the next CLK cycle is sent to the feedback section.

Decimation

Decimation by N is accomplished by only reading the LF43168's output once every N clock cycles. For example, to decimate by 10, the output should only be read once every 10 clock cycles. When not decimating, the maximum number of taps possible with a single filter in dual filter mode is eight. When decimating by N, there are N – 1 clock cycles between output readings when the filter output is not read. These extra clock cycles can be used to calculate more filter taps. As the decimation factor increases, the number of available filter taps increases also. When programmed to decimate by N, the number of filter taps for a single filter in dual filter mode increases to 8N.

Arithmetic Logic Units

The ALUs can perform the following operations: B + A, B – A, pass A, pass B, and negate A (–A). If $\overline{FWRD}$ is LOW, the forward decimation path provides the A inputs to the ALUs. If $\overline{FWRD}$ is HIGH, the A inputs are set to "0". If $\overline{RVRS}$ is LOW, the reverse decimation path provides the B inputs to the ALUs. If $\overline{RVRS}$ is HIGH, the B inputs are set to "0". $\overline{FWRD}$, $\overline{RVRS}$, and the filter configuration determine which ALU operation is performed. If $\overline{FWRD}$ and $\overline{RVRS}$ are both set LOW, and the filter is set for even-symmetric coefficients, the ALU will perform the B + A operation. If $\overline{FWRD}$ and $\overline{RVRS}$ are both set LOW, and the filter is set for odd-symmetric coefficients, the ALU will perform the B – A operation. If $\overline{FWRD}$ is set LOW, $\overline{RVRS}$ is set HIGH, and the filter is set for even-symmetric coefficients, the ALU will perform the pass A operation. If $\overline{FWRD}$ is set LOW, $\overline{RVRS}$ is set HIGH, and the filter is set for odd-symmetric coefficients, the ALU will perform the negate A operation. If $\overline{FWRD}$ is set HIGH, $\overline{RVRS}$ is set LOW, and the filter is set for either even or odd-symmetric coefficients, the ALU will perform the pass B operation.

Accumulators

The multiplier outputs are fed into an accumulator. Each filter has its own accumulator. The accumulator can be set to accumulate the multiplier outputs or sum the multiplier outputs and send the result to the accumulator output register. When ACCEN is HIGH, both accumulators are enabled for accumulation and writing to the accumulator output registers is disabled (the registers hold their values). When ACCEN goes LOW, accumulation is halted (by sending zeros to the accumulator feedback inputs) and writing to the accumulator output registers is enabled.

Mux/Adder

When the LF43168 is configured as two FIR filters, the Mux/Adder is used to determine which filter drives the output port. When the LF43168 is configured as a single FIR filter, the Mux/Adder is used to sum the outputs of the two filters and send the result to the output port. If 10-bit data and 20-bit coefficients or 20-bit data and 10-bit coefficients are required, the Mux/Adder can facilitate this by scaling filter B's output by 2^{-10} before being added to filter A's output. MUX1-0 determines what function the Mux/Adder performs (see Table 3).

The Mux/Adder is also used to round the output data before it is sent to the output port. Output data is rounded by adding a "1" to the bit position selected using bits 5-8 of Control Register 1 (see Table 2). For example, to round the

TABLE 3. MUX1-0 FUNCTION

MUX1-0	FUNCTION
00	Filter A + Filter B (Filter B Scaled by 2^{-10})
01	Filter A + Filter B
10	Filter A
11	Filter B

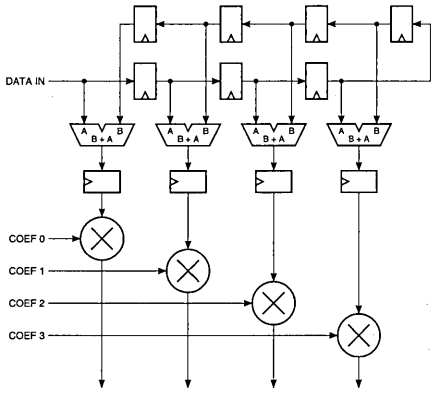
FIGURE 3. SYMMETRIC COEFFICIENT SET EXAMPLES

Even-Tap, Even-Symmetric Coefficient Set

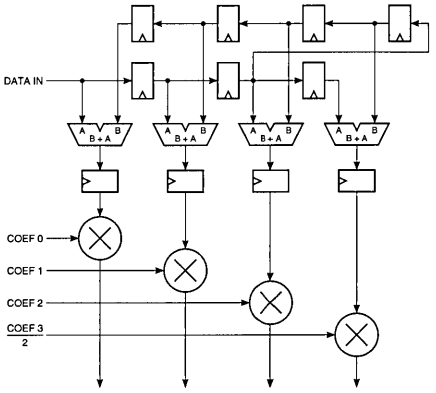
Odd-Tap, Even-Symmetric Coefficient Set

Even-Tap, Odd-Symmetric Coefficient Set

FIGURE 4. EVEN-SYMMETRIC COEFFICIENT FILTER CONFIGURATIONS (NO DECIMATION)



EVEN-TAP FILTER



ODD-TAP FILTER

output to 16 bits, bits 5-8 of Control Register 1 should be set to "0011". This will cause a "1" to be added to bit position 2^{-7}.

Symmetric Coefficients

The LF43168 filter architecture is optimized for symmetric filter coefficient sets. Figure 3 shows examples of the different types of symmetric coefficient sets. In even-symmetric sets, each coefficient value appears twice (except in odd-tap sets where the middle value appears only once). In odd-symmetric sets, each coefficient appears twice, but one value is positive and one is negative. If the two data input values that will be multiplied by the same coefficient are added or subtracted before being sent to the filter multiplier, the number of multipliers needed for an N-tap filter is cut in half. Therefore, an 8-tap filter can be implemented with four multipliers if a symmetric coefficient set is used.

FILTER CONFIGURATIONS

Figures 4-6 show the data paths from filter input to filter multipliers for all symmetric coefficient filters. Figure 7 shows the interleaved coefficient filter configuration. Each diagram shows one of the two FIR filters when the device is configured for dual filter mode. The diagrams can be expanded to include both filters when the device is configured for single filter mode.

Even-Symmetric Coefficient Filters

Figure 4 shows the two possible configurations when the device is programmed for even-symmetric coefficients and no decimation. Note that coefficient 3 on the odd-tap filter must be divided by two to get the correct result (The coefficient must be input to the device already divided by two).

FIGURE 5. DECIMATING, EVEN-SYMMETRIC COEFFICIENT FILTER CONFIGURATIONS

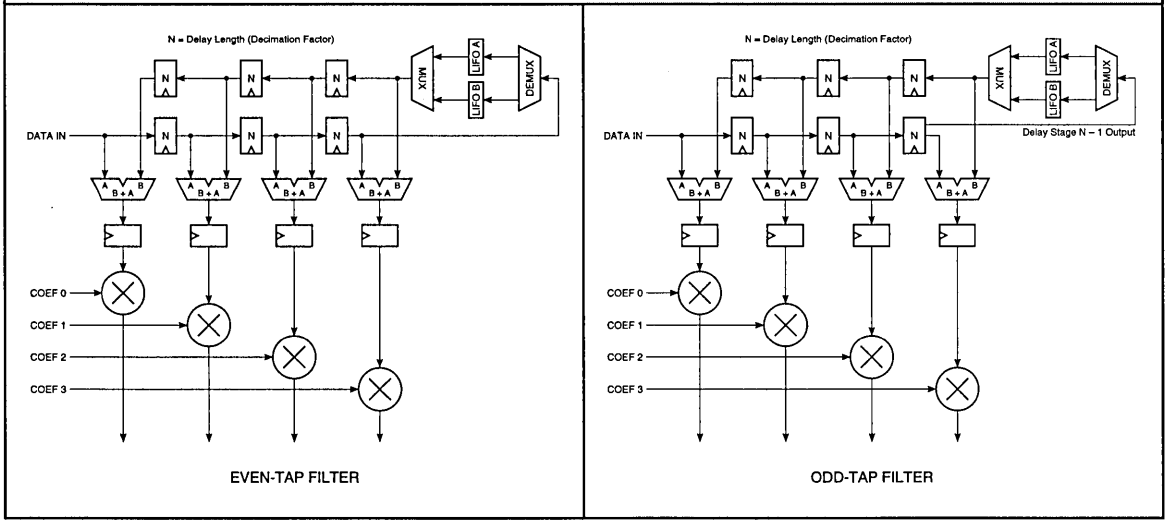


FIGURE 6. ODD-SYMMETRIC COEFFICIENT FILTER CONFIGURATIONS

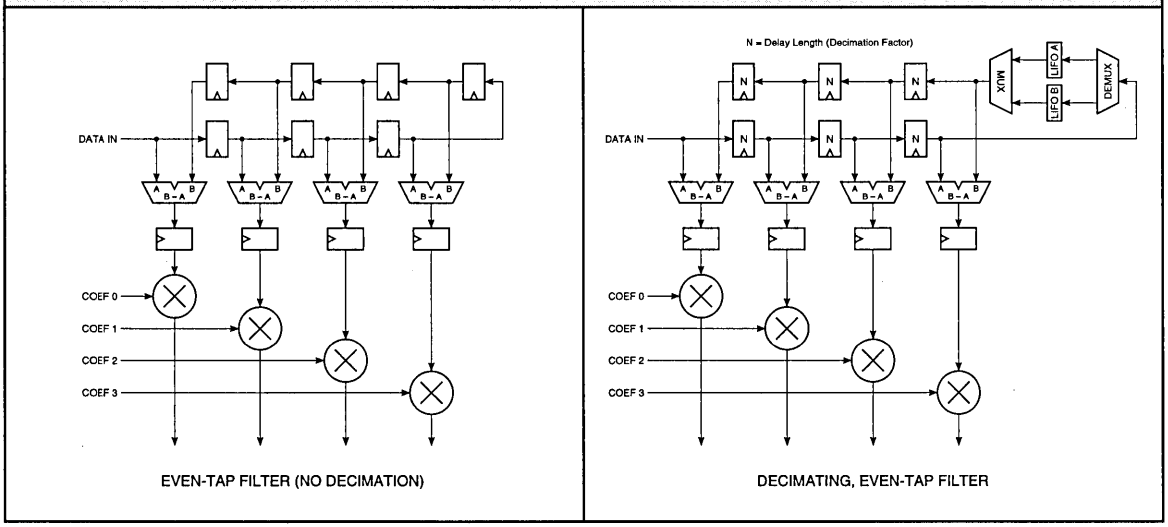


Figure 5 shows the two possible configurations when the device is programmed as a decimating, even-symmetric coefficient filter. The delay length of the decimation registers will be equal to the decimation factor that the device is programmed for. Since only four coefficients (effectively eight) can be sent to the filter multipliers on a clock cycle, it may be necessary (depending on the coefficient set) to change the coefficients fed to the multipliers on different CLK cycles for filters with more than eight taps. Note that for the odd-tap filter, the middle coefficient of the coefficient set must be divided by two to get the correct result.

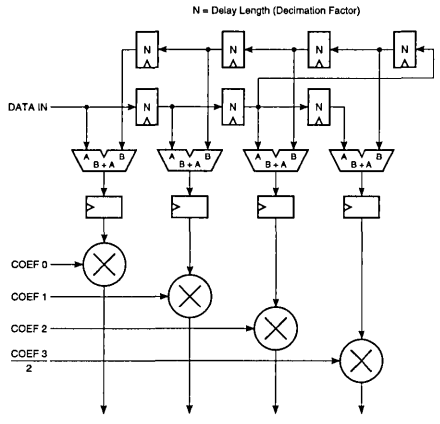
Odd-Symmetric Coefficient Filters

Figure 6 shows the two possible configurations when the device is programmed for odd-symmetric coefficients. Note that odd-tap, odd-symmetric coefficient filters are not possible.

Interleaved Coefficient Filters

Figure 7 shows the filter configuration when the device is programmed for interleaved coefficients. An interleaved coefficient set contains two separate odd-tap, even-symmetric coefficient sets which have been interleaved together (see Figure 8). If two data sets are interleaved into the same serial data stream, they can both be filtered by different coefficient sets if the two coefficient sets are also interleaved. The LF43168 is configured as an interleaved coefficient filter by programming the device for interleaved coefficient sets, even-symmetric coefficients, odd number of filter taps, and data reversal disabled. Note that coefficient 3, in Figure 7, must be divided by two to get the correct result.

FIGURE 7. INTERLEAVED COEFFICIENT FILTER CONFIGURATION

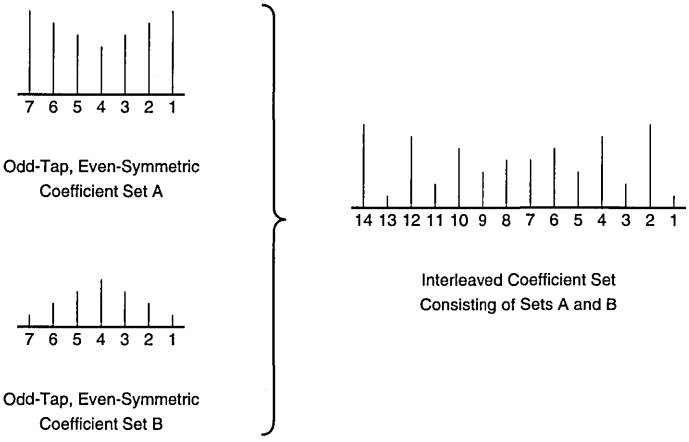


ODD-TAP INTERLEAVED FILTER

Asymmetric Coefficient Filters

It is possible to have asymmetric coefficient filters. Asymmetric coefficient sets do not exhibit even or odd symmetric properties. A 4-tap asymmetric filter is possible by putting the device in even-tap, pass A mode and then feeding the asymmetric coefficient set to the multipliers. An 8-tap asymmetric filter is possible if the device is clocked twice as fast as the input data rate. It will take two CLK cycles to calculate the output. On the first CLK cycle, the reverse decimation path is selected to feed data to the filter multipliers. On the second CLK cycle, the coefficients sent to the multipliers are changed (if necessary) and the forward decimation path is selected to feed data to the filter multipliers.

FIGURE 8. INTERLEAVED COEFFICIENT SET EXAMPLE



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

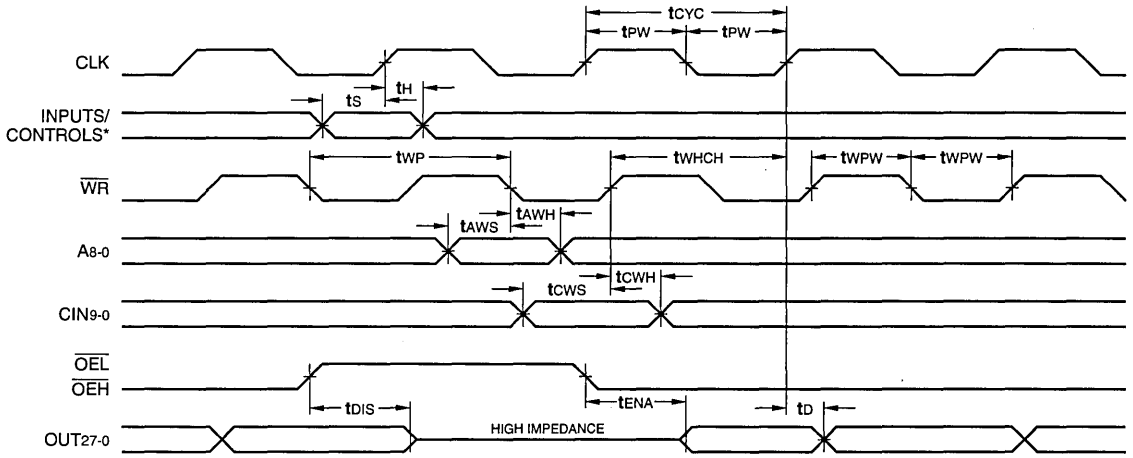
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.6			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			300	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			500	µA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			12	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			12	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE *Notes 9, 10 (ns)*

Symbol	Parameter	LF43168– 30 Min	30 Max	22 Min	22 Max	15 Min	15 Max
t_{CYC}	Cycle Time	30		22		15	
t_{PW}	Clock Pulse Width	12		8		7	
t_S	Input Setup Time	15		12		5	
t_H	Input Hold Time	0		0		0	
t_{WP}	Write Period	30		22		15	
t_{WPW}	Write Pulse Width	12		10		7	
t_{WHCH}	Write High to Clock High	5		3		2	
t_{CWS}	CIN_{9-0} Setup Time	12		10		5	
t_{CWH}	CIN_{9-0} Hold Time	0		0		0	
t_{AWS}	Address Setup Time	10		8		5	
t_{AWH}	Address Hold Time	0		0		0	
t_D	Output Delay		14		12		11
t_{ENA}	Three-State Output Enable Delay (Note 11)		12		12		12
t_{DIS}	Three-State Output Disable Delay (Note 11)		12		12		12

SWITCHING WAVEFORMS



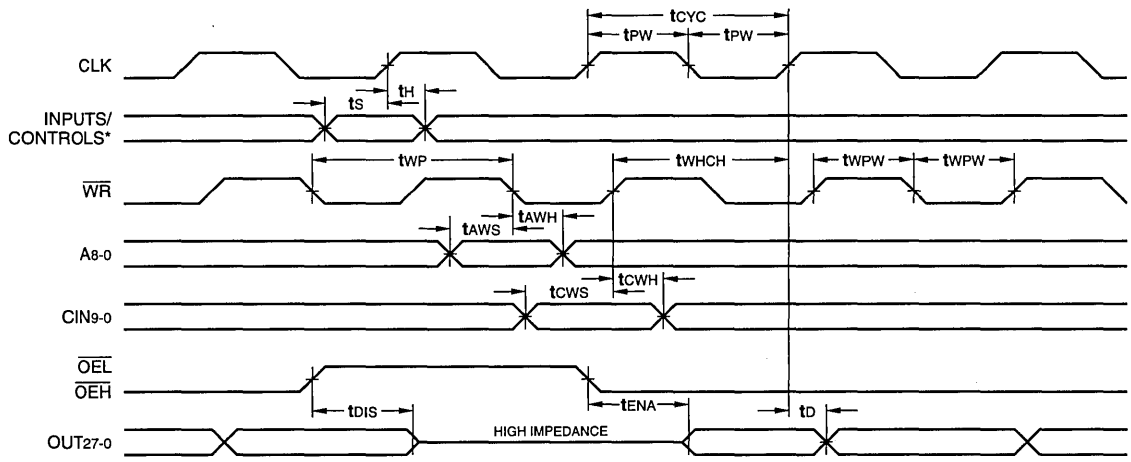
*includes INA_{9-0}, INB_{9-0}, $CSEL_{4-0}$, ACCEN, MUX_{1-0}, $\overline{SHFTEN}$, $\overline{FWRD}$, $\overline{RVRS}$, and $\overline{TXFR}$.

SWITCHING CHARACTERISTICS

MILITARY OPERATING RANGE *Notes 9, 10 (ns)*

		LF43168–					
		39		30		22	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	39		30		22	
t_{PW}	Clock Pulse Width	15		12		8	
t_S	Input Setup Time	17		15		12	
t_H	Input Hold Time	0		0		0	
t_{WP}	Write Period	39		30		22	
t_{WPW}	Write Pulse Width	15		12		10	
t_{WHCH}	Write High to Clock High	8		5		3	
t_{CWS}	CIN_{9-0} Setup Time	15		12		10	
t_{CWH}	CIN_{9-0} Hold Time	0		0		0	
t_{AWS}	Address Setup Time	10		10		8	
t_{AWH}	Address Hold Time	0		0		0	
t_D	Output Delay		17		15		12
t_{ENA}	Three-State Output Enable Delay (Note 11)		12		12		12
t_{DIS}	Three-State Output Disable Delay (Note 11)		12		12		12

SWITCHING WAVEFORMS



*includes INA_{9-0}, INB_{9-0}, $CSEL_{4-0}$, ACCEN, MUX_{1-0}, $\overline{SHFTEN}$, $\overline{FWRD}$, $\overline{RVRS}$, and $\overline{TXFR}$.

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

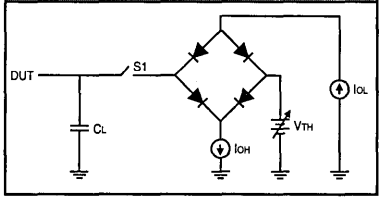
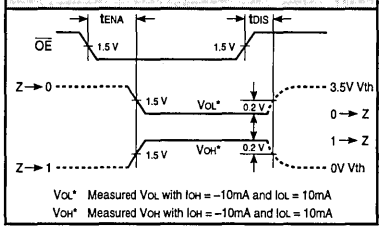


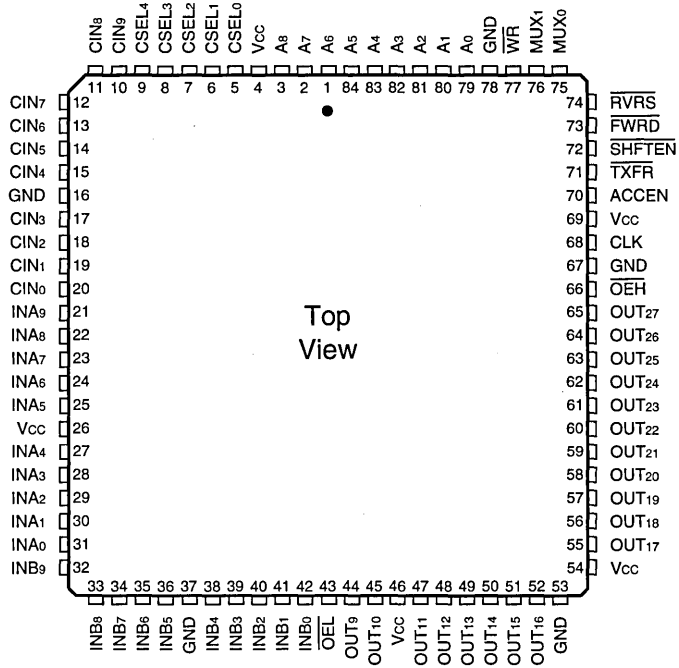
FIGURE B. THRESHOLD LEVELS



2

ORDERING INFORMATION

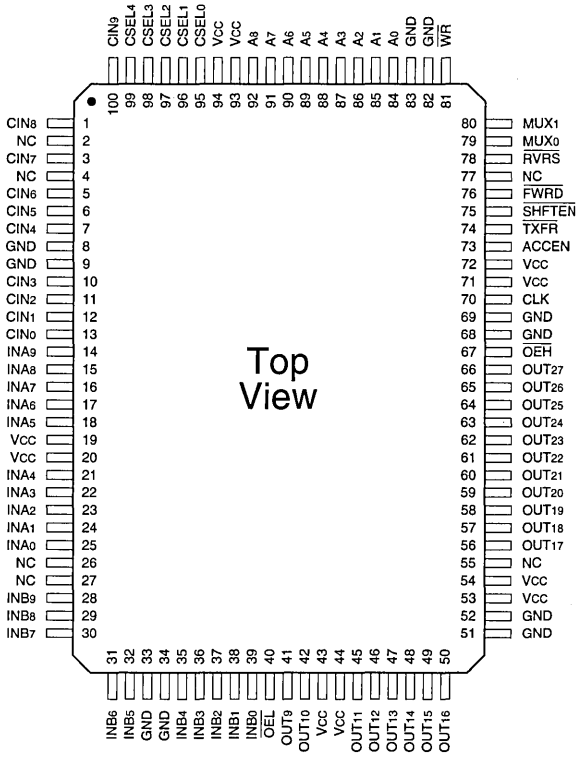
84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — COMMERCIAL SCREENING
30 ns	LF43168JC30
22 ns	LF43168JC22
15 ns	LF43168JC15

ORDERING INFORMATION

100-pin

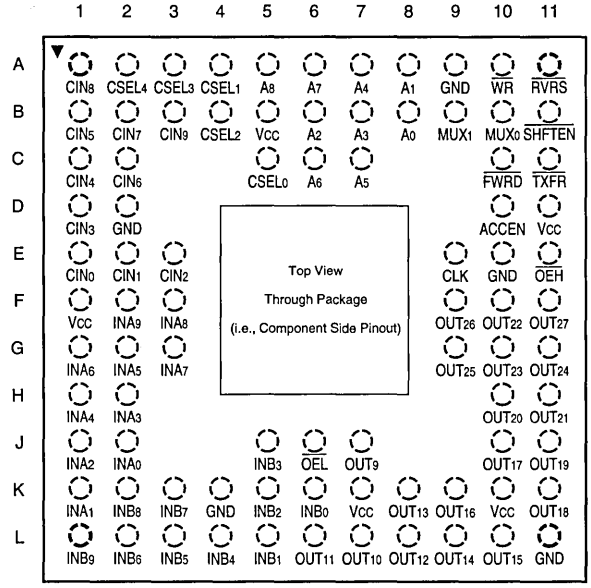


Speed	Plastic Quad Flatpack (Q2)
0°C to +70°C — COMMERCIAL SCREENING	
30 ns	LF43168QC30
22 ns	LF43168QC22
15 ns	LF43168QC15

2

ORDERING INFORMATION

84-pin



Speed	Ceramic Pin Grid Array (G3)
	0°C to +70°C — COMMERCIAL SCREENING
30 ns	LF43168GC30
22 ns	LF43168GC22
15 ns	LF43168GC15
	–55°C to +125°C — COMMERCIAL SCREENING
39 ns	LF43168GM39
30 ns	LF43168GM30
22 ns	LF43168GM22
	–55°C to +125°C — MIL-STD-883 COMPLIANT
39 ns	LF43168GMB39
30 ns	LF43168GMB30
22 ns	LF43168GMB22

LF43881
8 x 8-bit Digital Filter

FEATURES

- 40 MHz Maximum Sampling Rate
- 320 MHz Multiply-Accumulate Rate
- 8 Filter Cells
- 8-bit Unsigned or Two's Complement Data
- 8-bit Unsigned or Two's Complement Coefficients
- 26-bit Data Outputs
- Shift-and-Add Output Stage for Combining Filter Outputs
- Expandable Data Size, Coefficient Size, and Filter Length
- User-Selectable 2:1, 3:1, or 4:1 Decimation
- Available 100% Screened to MIL-STD-883, Class B
- Replaces Harris HSP43881 and HSP43881/883
- Package Styles Available:
  - 84-pin Plastic LCC, J-Lead
  - 100-pin Plastic Quad Flatpack
  - 84-pin Ceramic PGA

DESCRIPTION

The **LF43881** is a video-speed digital filter that contains eight filter cells (taps) cascaded internally and a shift-and-add output stage. An 8 x 8 multiplier, three decimation registers, and a 26-bit accumulator are contained in each filter cell. The output stage of the LF43881 contains a 26-bit accumulator which can add the contents of any filter stage to the output stage accumulator shifted right by 8 bits. 8-bit unsigned or two's complement format for data and coefficients can be independently selected.

Expanded coefficients and word sizes can be processed by cascading multiple LF43881s to implement larger filter lengths without affecting the sample rate. By reducing the sample rate, a single LF43881 can process larger filter lengths by using multiple passes. The sampling rate can range from 0 to 40 MHz. Over 1000 taps may be processed without overflows due to the architecture of the device.

The output sample rate can be reduced to one-half, one-third, or one-fourth the input sample rate by using the three decimation registers contained in every filter cell. Matrix multiplication, N x N spatial correlations/convolutions, and other 2-D operations for image processing can also be achieved using these registers.

LF43881 BLOCK DIAGRAM

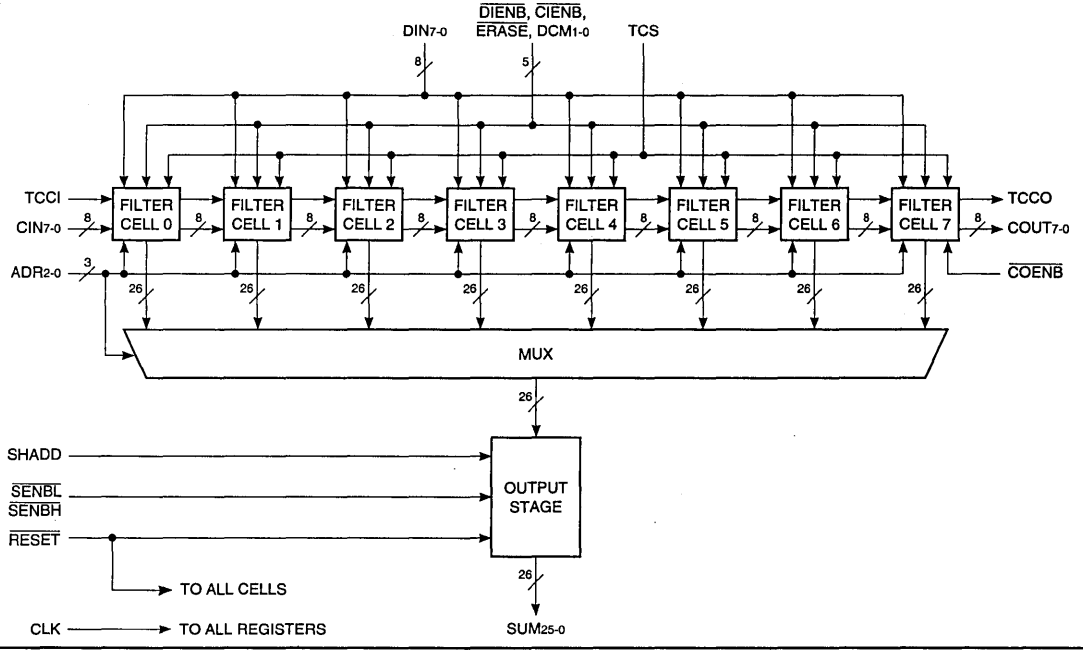
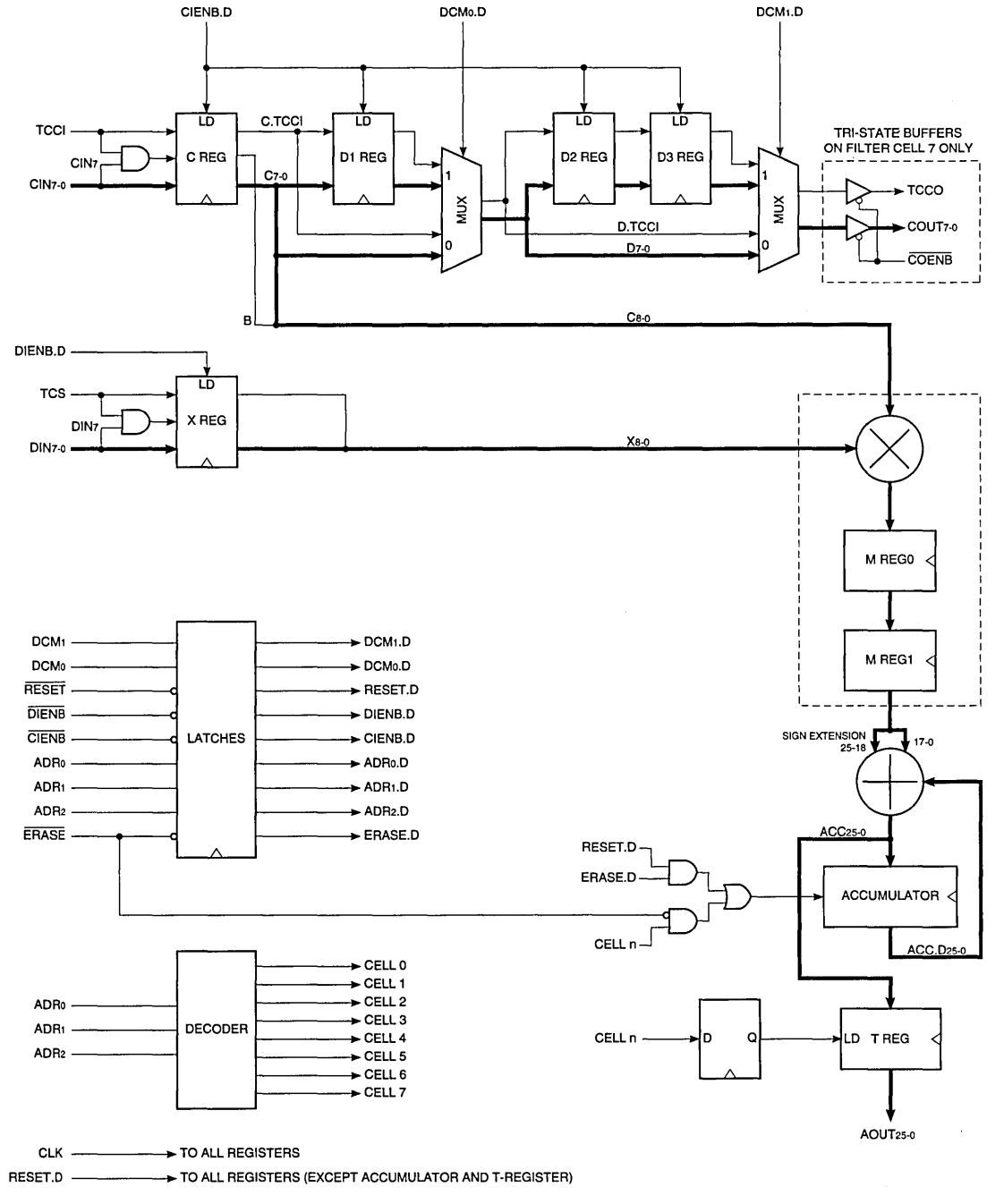


FIGURE 1. FILTER CELL DIAGRAM



FILTER CELL DESCRIPTION

8-bit coefficients are loaded into the C register (CIN7-0) and are output as COUT7-0 (the $\overline{\text{COENB}}$ signal enables the COUT7-0 outputs). The path taken by the coefficients varies according to the decimation mode chosen. With no decimation, the coefficients move directly from the C register, bypassing all decimation registers, and are available at the output on the following clock cycle. When decimation is chosen, the coefficient output is delayed by 1, 2, or 3 clock cycles depending on how many decimation registers the coefficients pass through (D1, D2, or D3). The number of decimation registers the coefficients pass through is determined by DCM1-0. Refer to Table 1 for choosing a decimation mode.

$\overline{\text{CIENB}}$ enables the C and D registers for coefficient loading. The registers are loaded on the rising edge of CLK when $\overline{\text{CIENB}}$ is LOW. $\overline{\text{CIENB}}$ is latched and delayed internally which enables the registers for loading one clock cycle after $\overline{\text{CIENB}}$ goes active (loading takes place on the second rising edge of CLK after $\overline{\text{CIENB}}$ goes LOW). Therefore, $\overline{\text{CIENB}}$ must be LOW one clock cycle before the coefficients are placed on the CIN7-0 inputs. The coefficients are held when $\overline{\text{CIENB}}$ is HIGH.

$\overline{\text{DIENB}}$ enables the X register for the loading of data. The X register is loaded on the rising edge of CLK when $\overline{\text{DIENB}}$ is LOW. $\overline{\text{DIENB}}$ is latched and delayed internally (loading takes place on the second rising edge of CLK after $\overline{\text{DIENB}}$ goes LOW). Therefore, $\overline{\text{DIENB}}$ must be LOW one clock cycle before the data is placed on the DIN7-0 inputs. The X register is loaded with all zeros when $\overline{\text{DIENB}}$ is HIGH.

The output of the C register (C8-0) and X register (X8-0) provide the inputs of the 8 x 8 multiplier. The multiplier is followed by two pipeline registers, M REG0 and M REG1. The output of the multiplier is sign extended and is used as one of the inputs to the 26-bit adder. The output of the 26-bit accumulator provides the second input to the adder. Both the accumulator and T register are loaded simultaneously with the output of the adder.

The accumulator is loaded with the output of the adder on every clock cycle unless cleared. Clearing the accumulator can be achieved using two methods. The first method, when both $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ are LOW, causes all accumulators and all registers in the device to be cleared together. $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ are latched and delayed internally causing the clearing to occur on the second clock cycle after $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ go active.

The second method, when only $\overline{\text{ERASE}}$ is LOW, clears a single accumulator of a selected cell. The cell is selected using the ADR2-0 inputs (decoded to Cell n). $\overline{\text{ERASE}}$ is latched and delayed internally causing the clearing to occur on the second clock cycle after $\overline{\text{ERASE}}$ goes active. Refer to Table 2 for clearing registers and accumulators.

FIGURE 2. OUTPUT STAGE DIAGRAM

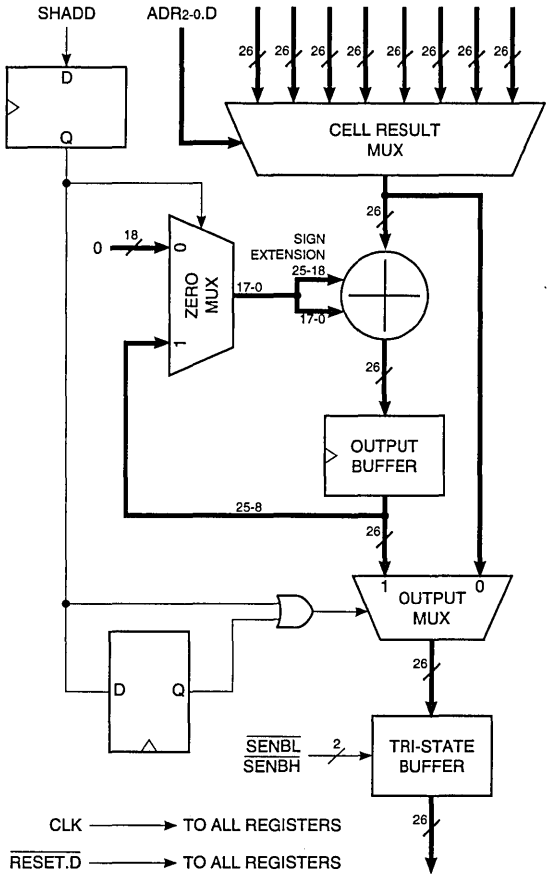


TABLE 1. DECIMATION MODE SELECTION

DCM1	DCM0	Decimation Function
0	0	Decimation registers not used
0	1	One decimation register used (decimation by one-half)
1	0	Two decimation registers used (decimation by one-third)
1	1	Three decimation registers used (decimation by one-fourth)

TABLE 2. REGISTER AND ACCUMULATOR CLEARING

$\overline{ERASE}$	$\overline{RESET}$	Clearing Effect
0	0	All accumulators and all registers are cleared
0	1	Only the accumulator addressed by ADR2-0 is cleared
1	0	All registers are cleared (accumulators are not cleared)
1	1	No clearing occurs, internal state remains the same

OUTPUT STAGE DESCRIPTION

The 26-bit adder contained in the output stage can add the contents of any filter cell accumulator (selected by ADR2-0) with the 18 most significant bits of the output buffer. The result is stored back into the output buffer. The complete operation takes only one clock cycle. The eight least significant bits of the output buffer are lost.

The Zero multiplexer is controlled by the SHADD input signal. This allows selection of either the 18 most significant bits of the output buffer or all zeros for the adder input. When SHADD is LOW, all zeros will be selected. When SHADD is HIGH, the 18 most significant bits of the output buffer are selected enabling the shift-and-add operation. SHADD is latched and delayed internally by one clock cycle.

The output multiplexer is also controlled by the SHADD input signal. This allows selection of either a filter cell accumulator, selected by ADR2-0, or the output buffer to be output to the SUM25-0 bus. Only the 26 least significant bits from either a filter cell accumulator or the output buffer are output on SUM25-0. If SHADD is LOW during two consecutive clock cycles (low during the current and previous clock cycle), the output multiplexer selects the contents of a filter cell accumulator addressed by ADR2-0. Otherwise, the output multiplexer selects the contents of the output buffer.

If the same address remains on the ADR2-0 inputs for more than one clock cycle, SUM25-0 will not change to reflect any updates to the addressed cell accumulator. Only the result from the first selection of the cell (first clock cycle) will be output. This allows the interface of slow memory devices where the output needs to be active for more than one clock cycle. Normal FIR operation is not affected because ADR2-0 is changed sequentially.

NUMBER SYSTEMS

Data and coefficients can be represented as either unsigned or two's complement numbers. The TCS and TCCI inputs determine which of the two formats is to be used. All values are represented as 9-bit two's complement numbers internally. The value of the ninth bit is determined by the number system selected. The ninth bit is a sign extended bit when the two's complement mode is chosen. When the unsigned mode is chosen, the ninth bit is zero.

SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

DIN7-0 — Data Input

8-bit data is latched into the X register of each filter cell simultaneously. The TCS signal selects the appropriate data format type. The $\overline{DIENB}$ signal enables loading of the data.

CIN7-0 — Coefficient Input

8-bit coefficients are latched into the C register of Filter Cell 0. The TCCI signal selects the appropriate coefficient format type. The $\overline{CIENB}$ signal enables loading of the coefficients.

Outputs

SUM25-0 — Data Output

The 26-bit result from an individual filter cell will appear when ADR2-0 is used to select the filter cell result. SHADD in conjunction with ADR2-0 is used to select the output from the shift-and-add output stage.

COUT7-0 — Coefficient Output

The 8-bit coefficient output from Filter Cell 7 can be connected to the CIN7-0 coefficient input of the same LF43881 to recirculate the coefficients. COUT7-0 can also be connected to the CIN7-0 of another LF43881 to cascade the devices. The $\overline{COENB}$ signal enables the output of the coefficients.

Controls

TCS — Data Format Control

The TCS input determines the interpretation of the input data. When TCS is HIGH, two's complement arithmetic is used. When TCS is LOW, unsigned arithmetic is used.

TCCI — Coefficient Input Format Control

The TCCI input determines the interpretation of the coefficients. When TCCI is HIGH, two's complement arithmetic is used. When TCCI is LOW, unsigned arithmetic is used.

TCCO — Coefficient Output Format

The TCCO output shows the format of the COUT7-0 coefficient output. TCCO follows the TCCI input. When cascading multiple LF43881s, the TCCO output of one device should be connected to the TCCI input of another device. The $\overline{\text{COENB}}$ signal enables TCCO.

$\overline{\text{DIENB}}$ — Data Input Enable

The $\overline{\text{DIENB}}$ input enables the X register of every filter cell. While $\overline{\text{DIENB}}$ is LOW, the X registers are loaded with the data present at the DIN7-0 inputs on the rising edge of CLK. While $\overline{\text{DIENB}}$ is HIGH, all bits of DIN7-0 are forced to zero and a rising edge of CLK will load the X register of every filter cell with all zeros. $\overline{\text{DIENB}}$ must be low one clock cycle prior to presenting the input data on the DIN7-0 input since it is latched and delayed internally.

$\overline{\text{CIENB}}$ — Coefficient Input Enable

The $\overline{\text{CIENB}}$ input enables the C and D registers of every filter cell. While $\overline{\text{CIENB}}$ is LOW, the C and appropriate D registers are loaded with the coefficient data on the rising edge of CLK. While $\overline{\text{CIENB}}$ is HIGH, the contents of the C and D registers are held and the CLK signal is ignored. By using $\overline{\text{CIENB}}$ in its active state, coefficient data can be shifted from cell to cell. $\overline{\text{CIENB}}$ must be low one clock cycle prior to presenting the coefficient data on the CIN7-0 input since it is latched and delayed internally.

$\overline{\text{COENB}}$ — Coefficient Output Enable

The $\overline{\text{COENB}}$ input enables the COUT7-0 and TCCO outputs. When $\overline{\text{COENB}}$ is LOW, the outputs are enabled. When $\overline{\text{COENB}}$ is HIGH, the outputs are placed in a high-impedance state.

DCM1-0 — Decimation Control

The DCM1-0 inputs select the number of decimation registers to use (Table 1). Coefficients are passed from one cell to another at a rate determined by DCM1-0. When no decimation registers are selected, the coefficients are passed from cell to cell on every rising edge of CLK (no decimation). When one decimation register is selected, the coefficients are passed from cell to cell on every other rising edge of CLK (2:1 decimation). When two decimation registers are selected, the coefficients are passed from cell to cell on every third rising edge of CLK (3:1 decimation) and so on. DCM1-0 is latched and delayed internally.

ADR2-0 — Cell Accumulator Select

The ADR2-0 inputs select which cell's accumulator will available at the SUM25-0 output or added to the output stage accumulator. In both cases, ADR2-0 is latched and delayed by one clock cycle. If the same address remains on the ADR2-0 inputs for more than one clock cycle, SUM25-0 will not change if the contents of the accumulator changes. Only the result from the first selection of the cell (first clock cycle) by ADR2-0 will be available. ADR2-0 is also used to select which accumulator to clear when $\overline{\text{ERASE}}$ is LOW.

$\overline{\text{SENBH}}$ — MSB Output Enable

When $\overline{\text{SENBH}}$ is LOW, SUM25-16 is enabled. When $\overline{\text{SENBH}}$ is HIGH, SUM25-16 is placed in a high-impedance state.

$\overline{\text{SENBL}}$ — LSB Output Enable

When $\overline{\text{SENBL}}$ is LOW, SUM15-0 is enabled. When $\overline{\text{SENBL}}$ is HIGH, SUM15-0 is placed in a high-impedance state.

$\overline{\text{RESET}}$ — Register Reset Control

When $\overline{\text{RESET}}$ is LOW, all registers are cleared simultaneously except the cell accumulators. $\overline{\text{RESET}}$ can be used with $\overline{\text{ERASE}}$ to clear all cell accumulators. $\overline{\text{RESET}}$ is latched and delayed internally. Refer to Table 2.

$\overline{\text{ERASE}}$ — Accumulator Erase Control

When $\overline{\text{ERASE}}$ is LOW, the cell accumulator specified by ADR2-0 is cleared. When $\overline{\text{RESET}}$ is LOW in conjunction with $\overline{\text{ERASE}}$, all cell accumulators are cleared. Refer to Table 2.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –400 µA	2.6			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	(Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			160	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			750	µA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

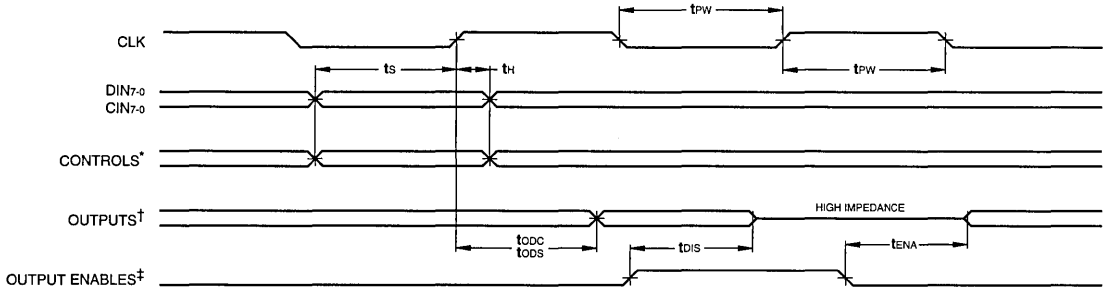
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF43881–							
		50		40		33		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		39		33		25	
t_{PW}	Clock Pulse Width	20		16		13		10	
t_S	Input Setup Time	16		14		13		10	
t_H	Input Hold Time	0		0		0		0	
t_{ODC}	Coefficient Output Delay		24		20		18		16
t_{ODS}	Sum Output Delay		27		25		21		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		20		15		15		12
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		15		15		12

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF43881–					
		50		40		33	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		39		33	
t_{PW}	Clock Pulse Width	20		16		13	
t_S	Input Setup Time	20		17		13	
t_H	Input Hold Time	0		0		0	
t_{ODC}	Coefficient Output Delay		24		20		18
t_{ODS}	Sum Output Delay		31		25		21
t_{ENA}	Three-State Output Enable Delay (Note 11)		20		15		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		15		15

SWITCHING WAVEFORMS



*includes $\overline{DIENB}$, $\overline{CIENB}$, $\overline{ERASE}$, $\overline{RESET}$, TCS, TCCI, SHADD, DCM_{1-0}, and ADR_{2-0}.

†includes TCCO, SUM_{25-0}, and $COUT_{7-0}$.

‡includes $\overline{SENBL}$, $\overline{SENBH}$, and $\overline{COENB}$.

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

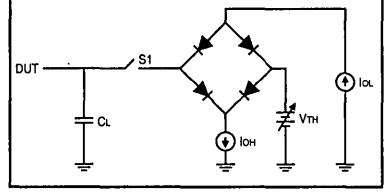
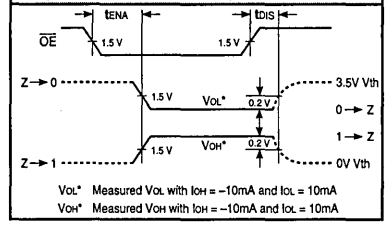
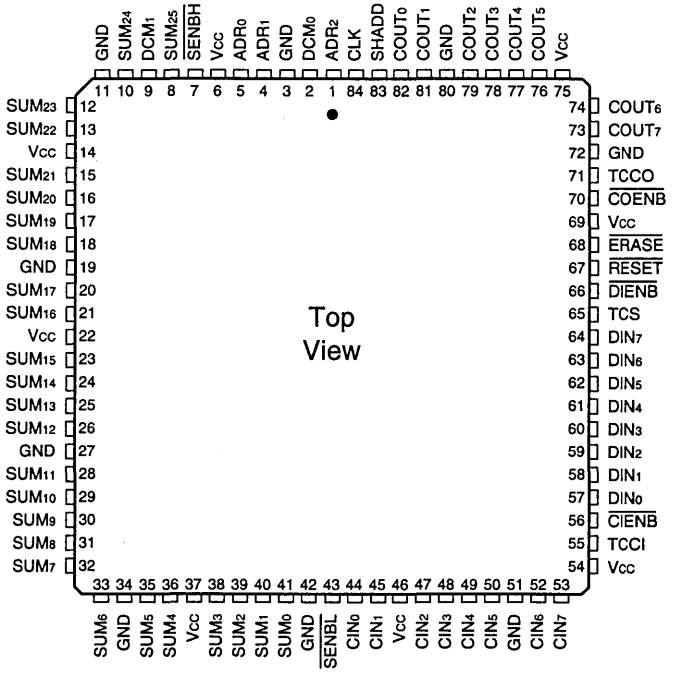


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

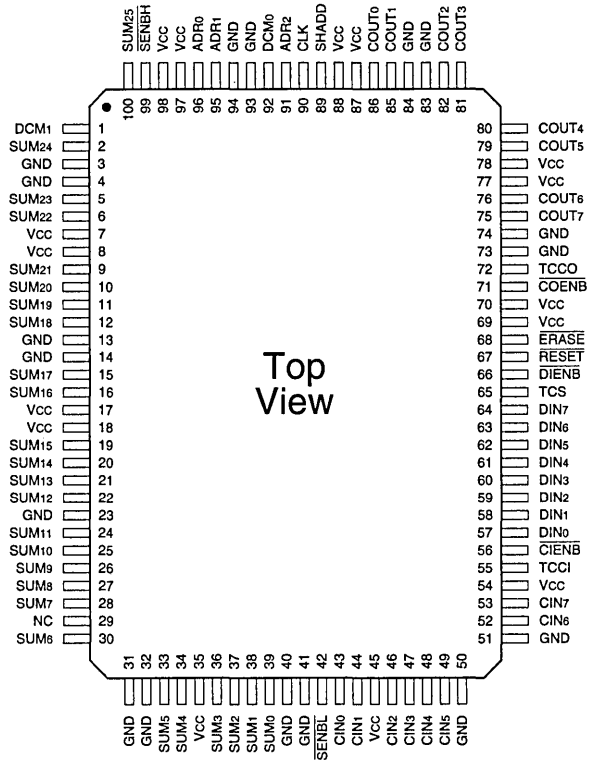
84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF43881JC50
40 ns	LF43881JC40
33 ns	LF43881JC33
25 ns	LF43881JC25

ORDERING INFORMATION

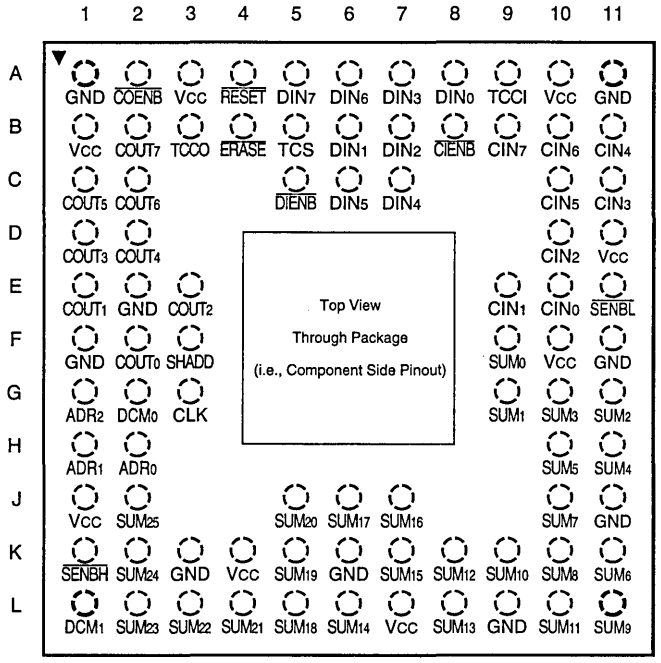
100-pin



Speed	Plastic Quad Flatpack (Q2)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF43881QC50
40 ns	LF43881QC40
33 ns	LF43881QC33
25 ns	LF43881QC25

ORDERING INFORMATION

84-pin



Speed	Ceramic Pin Grid Array (G3)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF43881GC50
40 ns	LF43881GC40
33 ns	LF43881GC33
25 ns	LF43881GC25
	–55°C to +125°C — COMMERCIAL SCREENING
50 ns	LF43881GM50
40 ns	LF43881GM40
33 ns	LF43881GM33
	–55°C to +125°C — MIL-STD-883 COMPLIANT
50 ns	LF43881GMB50
40 ns	LF43881GMB40
33 ns	LF43881GMB33

LF43891
9 x 9-bit Digital Filter

FEATURES

- 40 MHz Maximum Sampling Rate
- 320 MHz Multiply-Accumulate Rate
- 8 Filter Cells
- 8-bit Unsigned or 9-bit Two's Complement Data/Coefficients
- 26-bit Data Outputs
- Shift-and-Add Output Stage for Combining Filter Outputs
- Expandable Data Size, Coefficient Size, and Filter Length
- User-Selectable 2:1, 3:1, or 4:1 Decimation
- DECC SMD No. 5962-92097
- Available 100% Screened to MIL-STD-883, Class B
- Replaces Harris HSP43891 and HSP43891/883
- Package Styles Available:
  - 84-pin Plastic LCC, J-Lead
  - 100-pin Plastic Quad Flatpack
  - 84-pin Ceramic PGA

DESCRIPTION

The **LF43891** is a video-speed digital filter that contains eight filter cells (taps) cascaded internally and a shift-and-add output stage. A 9 x 9 multiplier, three decimation registers, and a 26-bit accumulator are contained in each filter cell. The output stage of the LF43891 contains a 26-bit accumulator which can add the contents of any filter stage to the output stage accumulator shifted right by 8 bits. 8-bit unsigned or 9-bit two's complement format for data and coefficients can be independently selected.

Expanded coefficients and word sizes can be processed by cascading multiple LF43891s to implement larger filter lengths without affecting the sample rate. By reducing the sample rate, a single LF43891 can process larger filter lengths by using multiple passes. The sampling rate can range from 0 to 40 MHz. Over 1000 taps may be processed without overflows due to the architecture of the device.

The output sample rate can be reduced to one-half, one-third, or one-fourth the input sample rate by using the three decimation registers contained in every filter cell. Matrix multiplication, N x N spatial correlations/convolutions, and other 2-D operations for image processing can also be achieved using these registers.

LF43891 BLOCK DIAGRAM

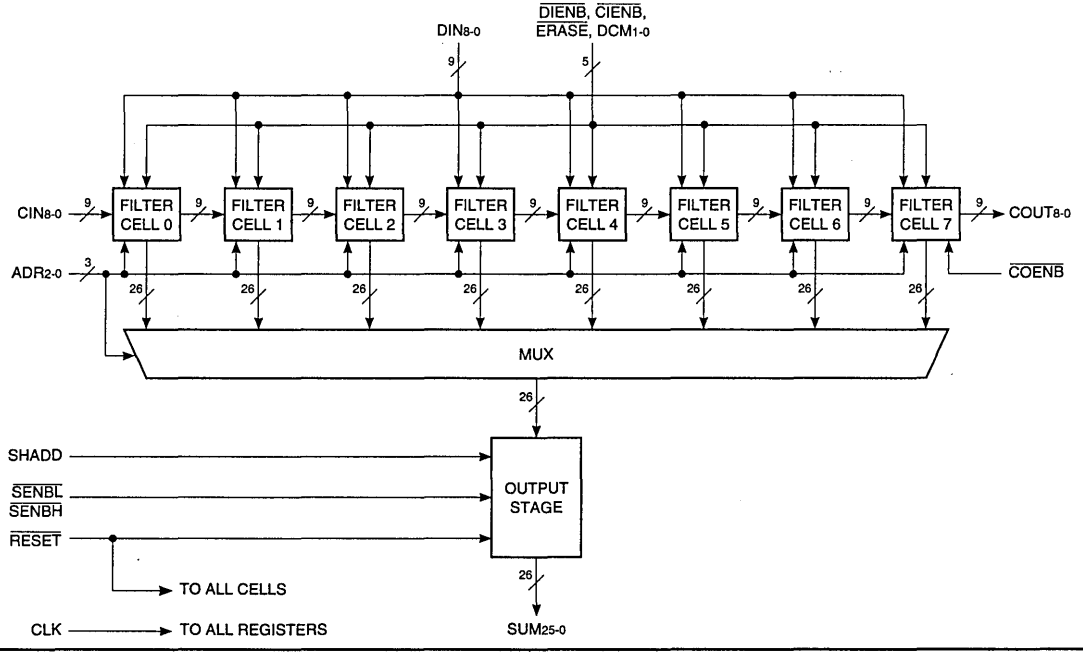
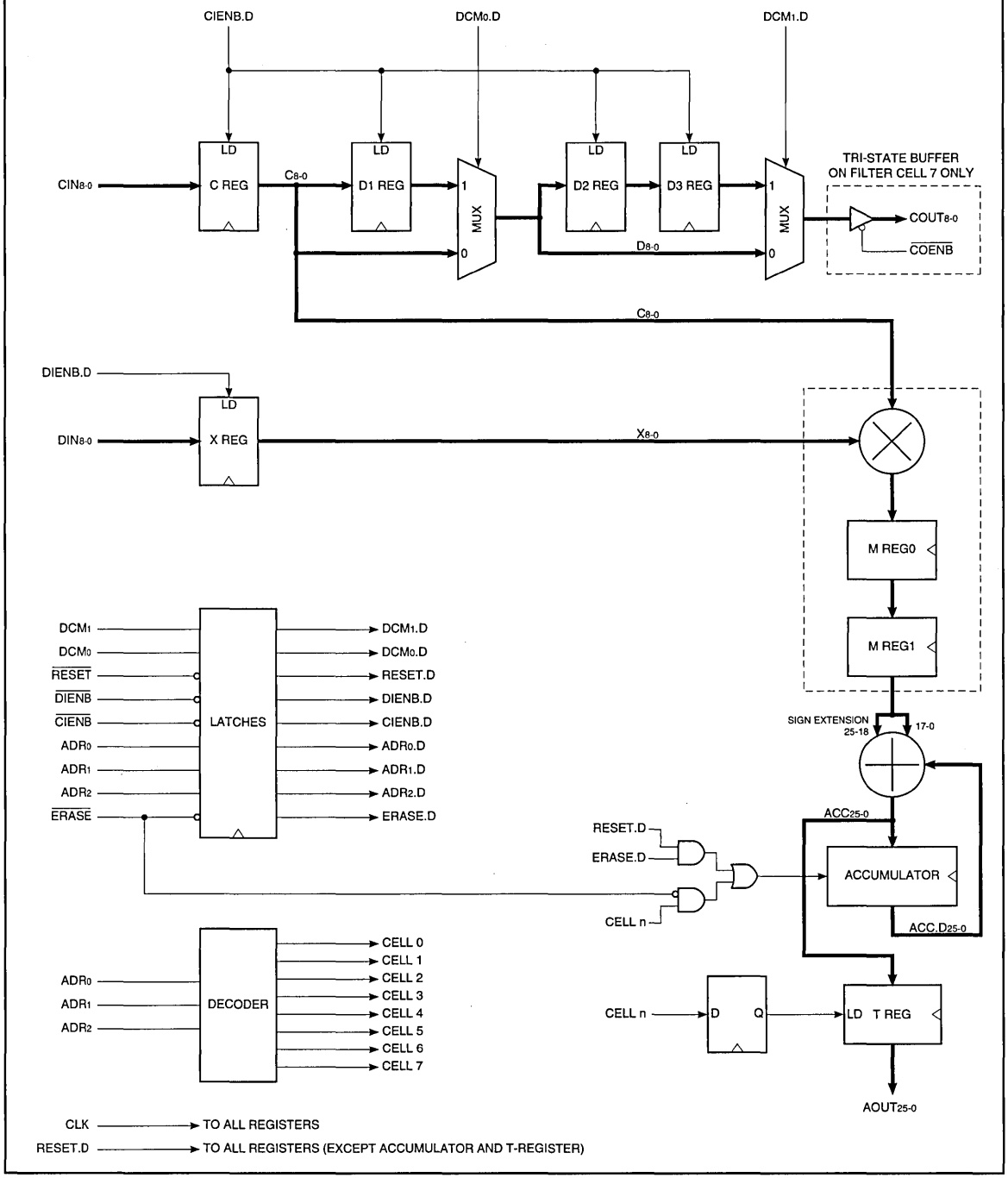


FIGURE 1. FILTER CELL DIAGRAM



FILTER CELL DESCRIPTION

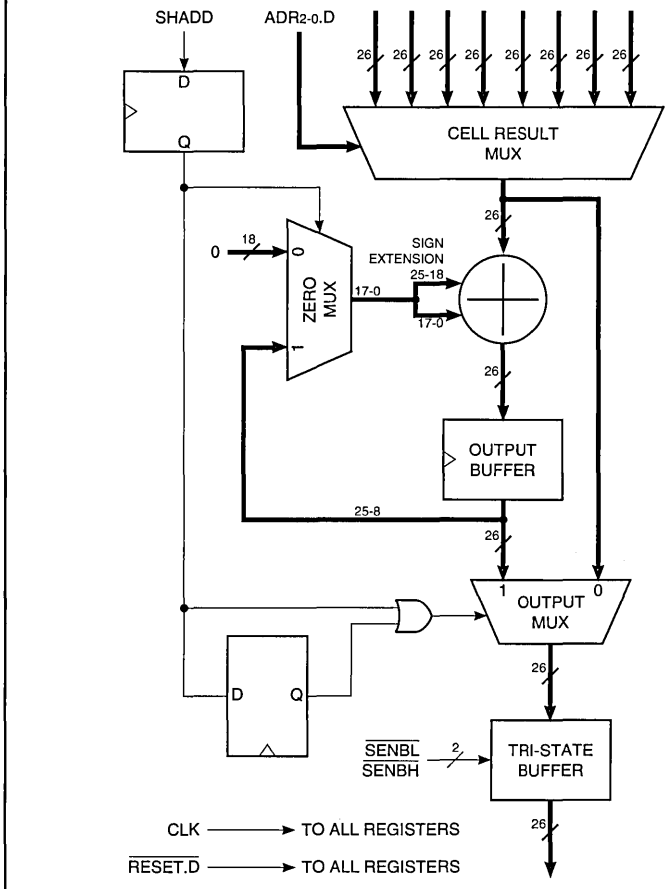
9-bit coefficients are loaded into the C register ($\overline{CIN}_{8-0}$) and are output as $\overline{COUT}_{8-0}$ (the $\overline{COENB}$ signal enables the $\overline{COUT}_{8-0}$ outputs). The path taken by the coefficients varies according to the decimation mode chosen. With no decimation, the coefficients move directly from the C register, bypassing all decimation registers, and are available at the output on the following clock cycle. When decimation is chosen, the coefficient output is delayed by 1, 2, or 3 clock cycles depending on how many decimation registers the coefficients pass through (D1, D2, or D3). The number of decimation registers the coefficients pass through is determined by DCM_{1-0}. Refer to Table 1 for choosing a decimation mode.

$\overline{CIENB}$ enables the C and D registers for coefficient loading. The registers are loaded on the rising edge of CLK when $\overline{CIENB}$ is LOW. $\overline{CIENB}$ is latched and delayed internally which enables the registers for loading one clock cycle after $\overline{CIENB}$ goes active (loading takes place on the second rising edge of CLK after $\overline{CIENB}$ goes LOW). Therefore, $\overline{CIENB}$ must be LOW one clock cycle before the coefficients are placed on the CIN_{8-0} inputs. The coefficients are held when $\overline{CIENB}$ is HIGH.

$\overline{DIENB}$ enables the X register for the loading of data. The X register is loaded on the rising edge of CLK when $\overline{DIENB}$ is LOW. $\overline{DIENB}$ is latched and delayed internally (loading takes place on the second rising edge of CLK after $\overline{DIENB}$ goes LOW). Therefore, $\overline{DIENB}$ must be LOW one clock cycle before the data is placed on the DIN_{8-0} inputs. The X register is loaded with all zeros when $\overline{DIENB}$ is HIGH.

The output of the C register (C_{8-0}) and X register (X_{8-0}) provide the inputs of the 9 x 9 multiplier. The multiplier is followed by two pipeline registers, M REG0 and M REG1. The output of the multiplier is sign extended and is used as one of the inputs to the 26-bit adder. The output of the 26-bit accumulator provides the second input to the adder. Both the accumulator and T register are loaded simultaneously with the output of the adder.

FIGURE 2. OUTPUT STAGE DIAGRAM



The accumulator is loaded with the output of the adder on every clock cycle unless cleared. Clearing the accumulator can be achieved using two methods. The first method, when both $\overline{RESET}$ and $\overline{ERASE}$ are LOW, causes all accumulators and all registers in the device to be cleared together. $\overline{RESET}$ and $\overline{ERASE}$ are latched and delayed internally causing the clearing to occur on the second clock cycle after $\overline{RESET}$ and $\overline{ERASE}$ go active.

The second method, when only $\overline{ERASE}$ is LOW, clears a single accumulator of a selected cell. The cell is selected using the ADR_{2-0} inputs (decoded to Cell n). $\overline{ERASE}$ is latched and delayed internally causing the clearing to occur on the second clock cycle after $\overline{ERASE}$ goes active. Refer to Table 2 for clearing registers and accumulators.

TABLE 1. DECIMATION MODE SELECTION

DCM1	DCM0	Decimation Function
0	0	Decimation registers not used
0	1	One decimation register used (decimation by one-half)
1	0	Two decimation registers used (decimation by one-third)
1	1	Three decimation registers used (decimation by one-fourth)

TABLE 2. REGISTER AND ACCUMULATOR CLEARING

$\overline{ERASE}$	$\overline{RESET}$	Clearing Effect
0	0	All accumulators and all registers are cleared
0	1	Only the accumulator addressed by ADR2-0 is cleared
1	0	All registers are cleared (accumulators are not cleared)
1	1	No clearing occurs, internal state remains the same

OUTPUT STAGE DESCRIPTION

The 26-bit adder contained in the output stage can add the contents of any filter cell accumulator (selected by ADR2-0) with the 18 most significant bits of the output buffer. The result is stored back into the output buffer. The complete operation takes only one clock cycle. The eight least significant bits of the output buffer are lost.

The Zero multiplexer is controlled by the SHADD input signal. This allows selection of either the 18 most significant bits of the output buffer or all zeros for the adder input. When SHADD is LOW, all zeros will be selected. When SHADD is HIGH, the 18 most significant bits of the output buffer are selected enabling the shift-and-add operation. SHADD is latched and delayed internally by one clock cycle.

The output multiplexer is also controlled by the SHADD input signal. This allows selection of either a filter cell accumulator, selected by ADR2-0, or the output buffer to be output to the SUM25-0 bus. Only the 26 least significant bits from either a filter cell accumulator or the output buffer are output on SUM25-0. If SHADD is LOW during two consecutive clock cycles (low during the current and previous clock cycle), the output multiplexer selects the contents of a filter cell accumulator addressed by ADR2-0. Otherwise, the output multiplexer selects the contents of the output buffer.

If the same address remains on the ADR2-0 inputs for more than one clock cycle, SUM25-0 will not change to reflect any updates to the addressed cell accumulator. Only the result from the first selection of the cell (first clock cycle) will be output. This allows the interface of slow memory devices where the output needs to be active for more than one clock cycle. Normal FIR operation is not affected because ADR2-0 is changed sequentially.

NUMBER SYSTEMS

Data and coefficients can be represented as either 8-bit unsigned or 9-bit two's complement numbers. All values are represented as 9-bit two's complement numbers internally. If the most significant or sign bit is a zero, the multiplier can multiply 8-bit unsigned numbers.

SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

DIN8-0 — Data Input

9-bit data is latched into the X register of each filter cell simultaneously. The $\overline{DIENB}$ signal enables loading of the data.

CIN8-0 — Coefficient Input

9-bit coefficients are latched into the C register of Filter Cell 0. The $\overline{CIENB}$ signal enables loading of the coefficients.

Outputs

SUM25-0 — Data Output

The 26-bit result from an individual filter cell will appear when ADR2-0 is used to select the filter cell result. SHADD in conjunction with ADR2-0 is used to select the output from the shift-and-add output stage.

COUT8-0 — Coefficient Output

The 9-bit coefficient output from Filter Cell 7 can be connected to the CIN8-0 coefficient input of the same LF43891 to recirculate the coefficients. COUT8-0 can also be connected to the CIN8-0 of another LF43891 to cascade the devices. The $\overline{COENB}$ signal enables the output of the coefficients.

Controls

$\overline{DIENB}$ — Data Input Enable

The $\overline{DIENB}$ input enables the X register of every filter cell. While $\overline{DIENB}$ is LOW, the X registers are loaded with the data present at the DIN8-0 inputs on the rising edge of CLK. While $\overline{DIENB}$ is HIGH, all bits of DIN8-0 are forced to zero and a rising edge of CLK will load the X register of every filter cell with all zeros. $\overline{DIENB}$ must be low one clock cycle prior to presenting the input data on the DIN8-0 input since it is latched and delayed internally.

$\overline{CIENB}$ — Coefficient Input Enable

The $\overline{CIENB}$ input enables the C and D registers of every filter cell. While $\overline{CIENB}$ is LOW, the C and appropriate D registers are loaded with the coefficient data on the rising edge of CLK. While $\overline{CIENB}$ is HIGH, the contents of the C and D registers are held and the CLK signal is ignored. By using $\overline{CIENB}$ in its active state, coefficient data can be shifted from cell to cell. $\overline{CIENB}$ must be low one clock cycle prior to presenting the coefficient data on the CIN8-0 input since it is latched and delayed internally.

$\overline{COENB}$ — Coefficient Output Enable

The $\overline{COENB}$ input enables the COUT8-0 output. When $\overline{COENB}$ is LOW, the outputs are enabled. When $\overline{COENB}$ is HIGH, the outputs are placed in a high-impedance state.

DCM1-0 — Decimation Control

The DCM1-0 inputs select the number of decimation registers to use (Table 1). Coefficients are passed from one cell to another at a rate determined by DCM1-0. When no decimation registers are selected, the coefficients are passed from cell to cell on every rising edge of CLK (no decimation). When one decimation register is selected, the coefficients are passed from cell to cell on every other rising edge of CLK (2:1 decimation). When two decimation registers are selected, the coefficients are passed from cell to cell on every third rising edge of CLK (3:1 decimation) and so on. DCM1-0 is latched and delayed internally.

ADR2-0 — Cell Accumulator Select

The ADR2-0 inputs select which cell's accumulator will available at the SUM25-0 output or added to the output stage accumulator. In both cases, ADR2-0 is latched and delayed by one clock cycle. If the same address remains on the ADR2-0 inputs for more than one clock cycle, SUM25-0 will not change if the contents of the accumulator changes. Only the result from the first selection of the cell (first clock cycle) by ADR2-0 will be available. ADR2-0 is also used to select which accumulator to clear when $\overline{ERASE}$ is LOW.

$\overline{SENBH}$ — MSB Output Enable

When $\overline{SENBH}$ is LOW, SUM25-16 is enabled. When $\overline{SENBH}$ is HIGH, SUM25-16 is placed in a high-impedance state.

$\overline{SENBL}$ — LSB Output Enable

When $\overline{SENBL}$ is LOW, SUM15-0 is enabled. When $\overline{SENBL}$ is HIGH, SUM15-0 is placed in a high-impedance state.

$\overline{RESET}$ — Register Reset Control

When $\overline{RESET}$ is LOW, all registers are cleared simultaneously except the cell accumulators. $\overline{RESET}$ can be used with $\overline{ERASE}$ to clear all cell accumulators. $\overline{RESET}$ is latched and delayed internally. Refer to Table 2.

$\overline{ERASE}$ — Accumulator Erase Control

When $\overline{ERASE}$ is LOW, the cell accumulator specified by ADR2-0 is cleared. When $\overline{RESET}$ is LOW in conjunction with $\overline{ERASE}$, all cell accumulators are cleared. Refer to Table 2.

2

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –400 µA	2.6			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	(Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			160	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			750	µA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

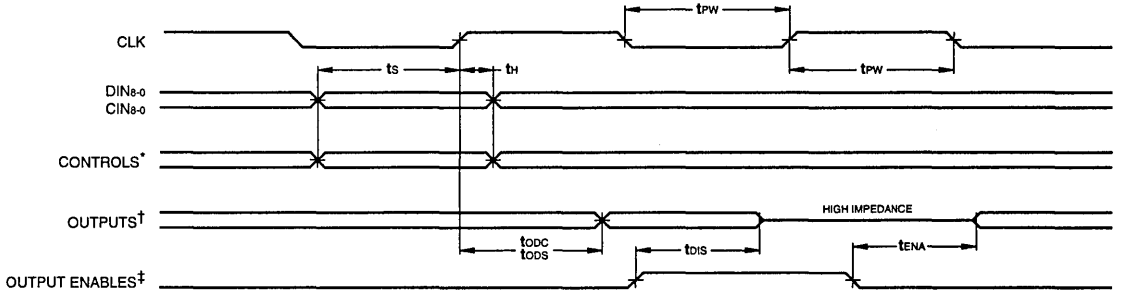
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF43891–							
		50		40		33		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
tCYC	Cycle Time	50		39		33		25	
tPW	Clock Pulse Width	20		16		13		10	
tS	Input Setup Time	16		14		13		10	
tH	Input Hold Time	0		0		0		0	
tODC	Coefficient Output Delay		24		20		18		16
tODS	Sum Output Delay		27		25		21		18
tENA	Three-State Output Enable Delay (Note 11)		20		15		15		12
tDIS	Three-State Output Disable Delay (Note 11)		20		15		15		12

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF43891–					
		50		40		33	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
tCYC	Cycle Time	50		39		33	
tPW	Clock Pulse Width	20		16		13	
tS	Input Setup Time	20		17		13	
tH	Input Hold Time	0		0		0	
tODC	Coefficient Output Delay		24		20		18
tODS	Sum Output Delay		31		25		21
tENA	Three-State Output Enable Delay (Note 11)		20		15		15
tDIS	Three-State Output Disable Delay (Note 11)		20		15		15

SWITCHING WAVEFORMS



*includes $\overline{DIENB}$, $\overline{CIENB}$, $\overline{ERASE}$, $\overline{RESET}$, SHADD, DCM1-0, and ADR2-0.

†includes SUM25-0 and COUT8-0.

‡includes $\overline{SENBL}$, $\overline{SENBH}$, and $\overline{COENB}$.

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

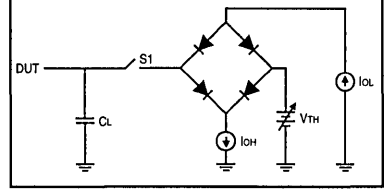
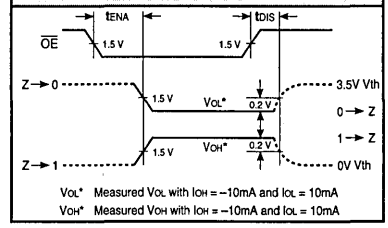
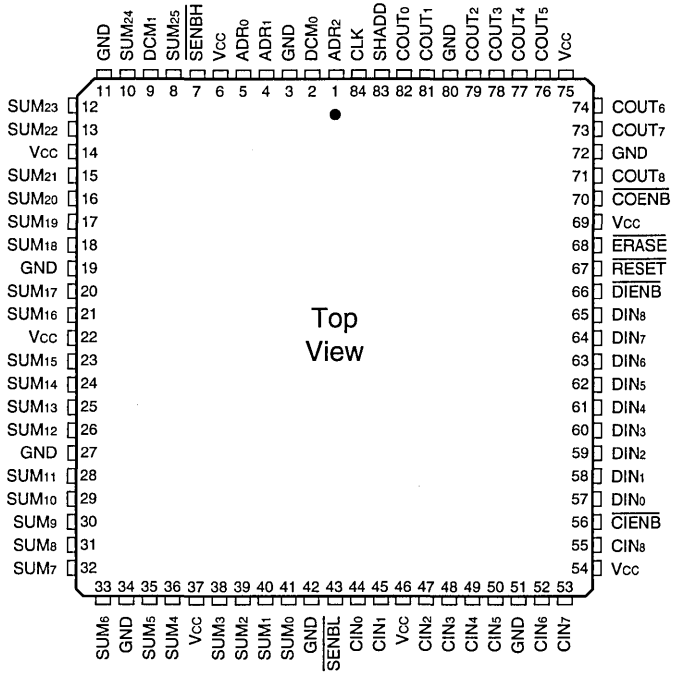


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

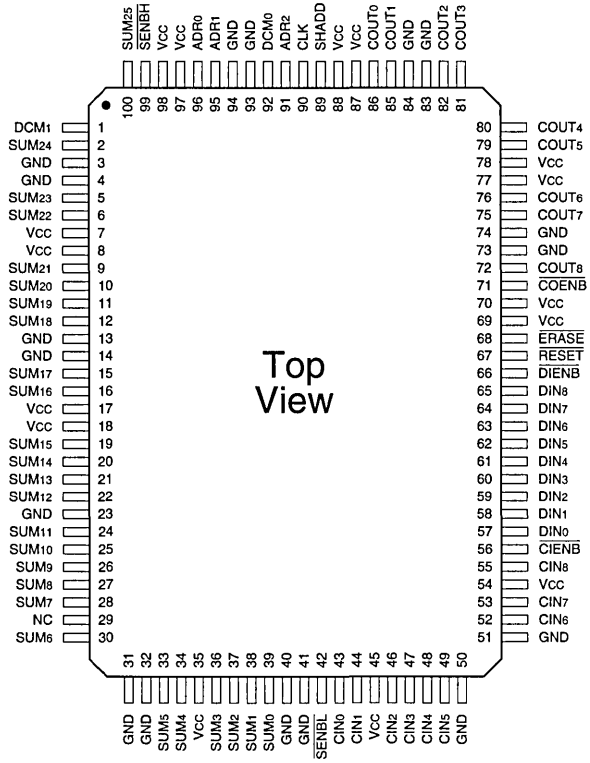
84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF43891JC50
40 ns	LF43891JC40
33 ns	LF43891JC33
25 ns	LF43891JC25

ORDERING INFORMATION

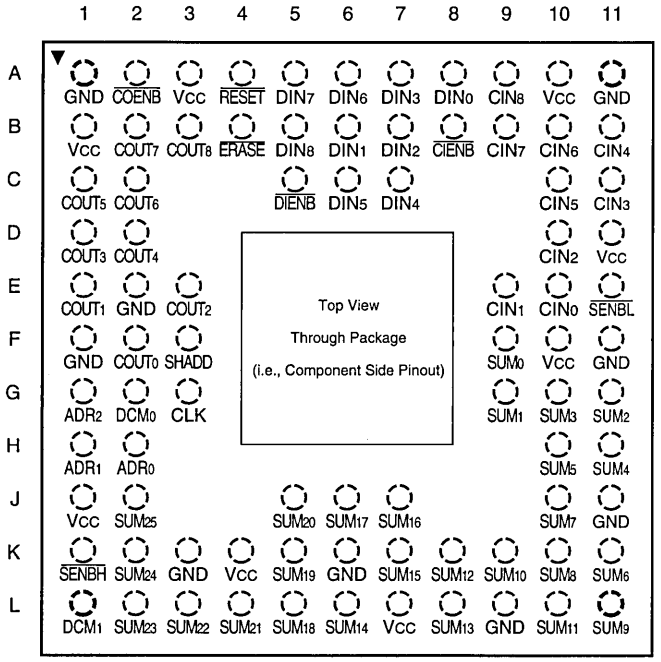
100-pin



Speed	Plastic Quad Flatpack (Q2)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF43891QC50
40 ns	LF43891QC40
33 ns	LF43891QC33
25 ns	LF43891QC25

ORDERING INFORMATION

84-pin



Speed	Ceramic Pin Grid Array (G3)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF43891GC50
40 ns	LF43891GC40
33 ns	LF43891GC33
25 ns	LF43891GC25
	–55°C to +125°C — COMMERCIAL SCREENING
50 ns	LF43891GM50
40 ns	LF43891GM40
33 ns	LF43891GM33
	–55°C to +125°C — MIL-STD-883 COMPLIANT
50 ns	LF43891GMB50
40 ns	LF43891GMB40
33 ns	LF43891GMB33

LF48212
12 x 12-bit Alpha Mixer

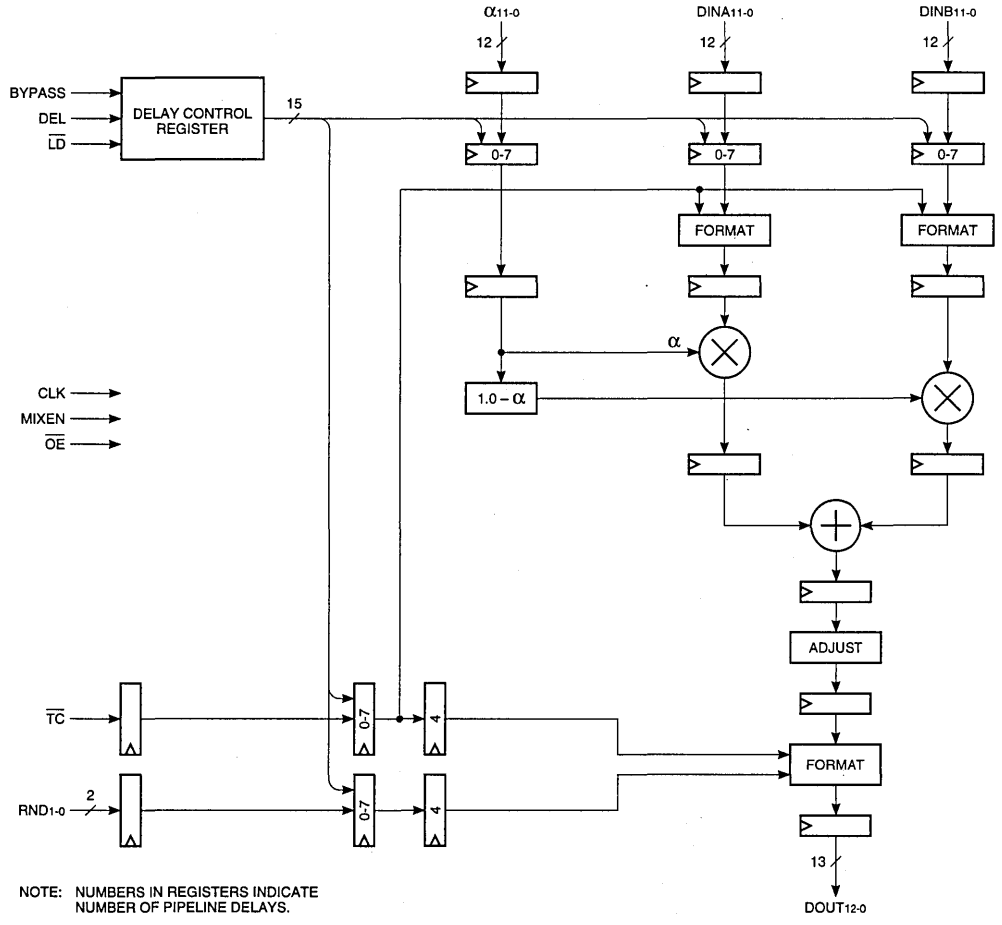
FEATURES

- 50 MHz Data and Computation Rate
- Two's Complement or Unsigned Operands
- On-board Programmable Delay Stages
- Programmable Output Rounding
- Replaces Harris HSP48212
- Package Styles Available:
  - 68-pin Plastic LCC, J-Lead
  - 64-pin Plastic Quad Flatpack

DESCRIPTION

The LF48212 is a high-speed video alpha mixer capable of mixing video signals at real-time video rates. It takes two 12-bit video signals and mixes them together using an alpha mix factor. Alpha determines the weighting that each video signal receives during the mix operation. The input video data can be in either unsigned or two's complement format, but both inputs must be in the same format. Independently controlled programmable delay stages are provided for the input and control signals to allow for allignment of input data if necessary. The delay stages can be programmed to have from 0 to 7 delays. The 13-bit output of the alpha mixer is registered with three-state drivers and may be rounded to 8, 10, 12, or 13-bits.

LF48212 Block Diagram



SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers except for the Delay Control Register.

Inputs

DINA11-0 — Pixel Data Input A

DINA11-0 is one of the 12-bit registered data input ports. Data is latched on the rising edge of CLK.

DINB11-0 — Pixel Data Input B

DINB11-0 is the other 12-bit registered data input port. Data is latched on the rising edge of CLK.

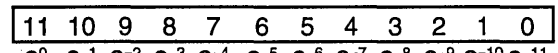
$\alpha_{11\text{-}0}$ — Alpha Mix Input

$\alpha_{11\text{-}0}$ determines the weighting applied to the data input signals before being mixed together. DINA11-0 and DINB11-0 receive weightings of α and $1.0 - \alpha$ respectively. $\alpha_{11\text{-}0}$ is unsigned and restricted to the range of 0 to 1.0. Figure 1 shows the data format for $\alpha_{11\text{-}0}$. If a value greater than 1.0 is latched into the Alpha Mix Input, internal circuitry will force the value to be equal to 1.0. Data is latched on the rising edge of CLK.

DEL — Delay Data Input

DEL is used to load the Delay Control Register. The Delay Control Register contains a 15-bit value which determines the number of delay stages added to the input and control signals. The 15-bit data value is loaded serially into the Delay Control Register using DEL and $\overline{LD}$. Data present on DEL is latched on the rising edge of $\overline{LD}$.

FIGURE 1. ALPHA MIX INPUT FORMAT



Outputs

DOUT12-0 — Data Output

DOUT12-0 is the 13-bit registered data output port.

Controls

$\overline{TC}$ — Data Format Control

$\overline{TC}$ determines if the input data is in unsigned or two's complement format. If $\overline{TC}$ is LOW, the data is in two's complement format. If $\overline{TC}$ is HIGH, the data is in unsigned format. Data present on $\overline{TC}$ is latched on the rising edge of CLK. $\overline{TC}$ only affects the data that is being latched into the LF48212. Changing $\overline{TC}$ does not affect internal data already in the pipeline.

MIXEN — Alpha Mix Input Enable

When HIGH, data on $\alpha_{11\text{-}0}$ is latched into the LF48212 on the rising edge of CLK. When LOW, data on $\alpha_{11\text{-}0}$ is not latched and the last value loaded is held as the alpha mix value.

$\overline{LD}$ — Load Strobe

The rising edge of $\overline{LD}$ latches the data on DEL into the Delay Control Register.

BYPASS — Bypass Delay Stage Control

The BYPASS control is used to bypass the internal programmable delay stages. When BYPASS is set HIGH, the Delay Control Register will automatically be loaded with a "0". This will set the number of programmable delay stages to zero for all input and control signals. When BYPASS is LOW, the desired number of delay stages can be set by loading the Delay Control Register with the appropriate value. Note that this signal is not intended to change during active operation of the LF48212.

RND1-0 — Output Rounding Control

RND1-0 determines how the output of the LF48212 is rounded. The output may be rounded to 8, 10, 12, or 13-bits. Table 1 lists the different rounding possibilities and the associated value for RND1-0. Rounding is accomplished by adding a "1" to the bit to the right of what will become the least significant bit. Then the bit that had the "1" added to it and all bits to the right of it are set to "0". Data present on RND1-0 is latched on the rising edge of CLK. When RND1-0 is latched in, it only applies to the video input data latched in at the same time. Changing RND1-0 does not affect the rounding format for internal data already in the pipeline.

$\overline{OE}$ — Output Enable

When $\overline{OE}$ is LOW, DOUT12-0 is enabled for output. When $\overline{OE}$ is HIGH, DOUT12-0 is placed in a high-impedance state.

TABLE 1. OUTPUT ROUNDING

RND1-0	ROUNDING FORMAT
00	Round to 8-bits
01	Round to 10-bits
10	Round to 12-bits
11	Round to 13-bits

FUNCTIONAL DESCRIPTION

The two video signals to be mixed together are input to the LF48212 using DINA11-0 and DINB11-0. Data present on DINA11-0 and DINB11-0 is latched on the rising edge of CLK. The input data may be in either unsigned or two's complement format, but both inputs must be in the same format. $\overline{TC}$ determines the format of the input data. When $\overline{TC}$ is HIGH, the input data is in unsigned format. When $\overline{TC}$ is LOW, the input data is in two's complement format. $\overline{TC}$ is latched on the rising edge of CLK and only affects the input data latched in at the same time. The data already in the pipeline is not affected when $\overline{TC}$ changes.

DINA11-0 and DINB11-0 are mixed together using an alpha mix factor (α_{11-0}) as defined by the equation listed in Figure 2. α_{11-0} is unsigned and restricted to the range of 0 to 1.0. MIXEN controls the loading of alpha mix data. When MIXEN is HIGH, data present on α_{11-0} is latched on the rising edge of CLK. When MIXEN is LOW, data present on α_{11-0} is not latched and the last value loaded is held as the alpha mix value.

It is possible to add extra delay stages to the input data and control signals by using the programmable delay stages. The 15-bit value (DELAY14-0) stored in the Delay Control Register determines the number of delay stages added. DELAY14-0 is divided into 5 groups of 3-bits each. Each 3-bit group contains the delay information for one of the input data or control signals. Figure 3 shows the block diagram of the Delay Control Register as well as a list of the input data and control signals that may be delayed and the DELAY signals that control them. The delay length can be programmed to be from 0 to 7 stages. The delay length is set by loading the binary equivalent of the desired delay length into the appropriate 3-bit group. For example, to add four extra delay stages to DINB11-0, DELAY5-3 should be set to "100". DELAY14-0 is loaded serially into the Delay Control Register using DEL and $\overline{LD}$. DELAY0 is the first value loaded and DELAY14 is the last. Data present on DEL is latched on the rising edge of $\overline{LD}$. BYPASS is used to disable the programmable delay stages. When BYPASS is HIGH, the Delay Control Register is automatically loaded with a "0". This sets all programmable delay stages to a length of zero. When BYPASS is LOW, the Delay Control Register may be loaded to set the desired number of delay stages. Note that BYPASS is not intended to change during active operation of the LF48212.

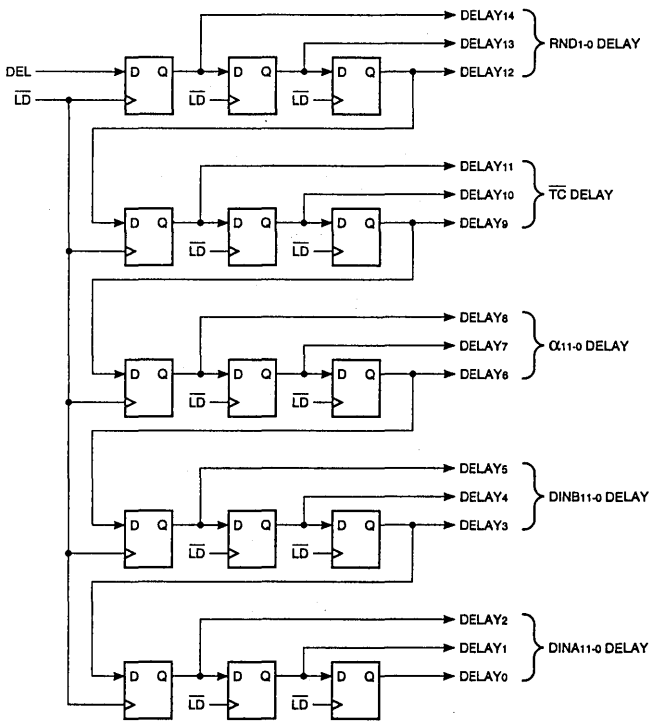
The Adjust stage of the LF48212 is used to maximize the precision of the output data. Since α can never be larger than 1.0, the most significant bit of the internal summer output is not needed. The Adjust stage takes the output of the internal summer and left shifts the data one bit position. This removes the MSB of the internal summer output and provides one more bit of precision for the output data.

The output data of the LF48212 may be rounded to 8, 10, 12, or 13-bits. RND1-0 determines how the output is rounded (See Table 1). RND1-0 is latched on the rising edge of CLK and only affects the input data latched in at the same time. The data already in the pipeline is not affected when RND1-0 changes.

FIGURE 2. OUTPUT EQUATION

$$OUTPUT = \alpha(DINA) + (1 - \alpha)DINB$$

FIGURE 3. DELAY CONTROL REGISTER BLOCK DIAGRAM



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

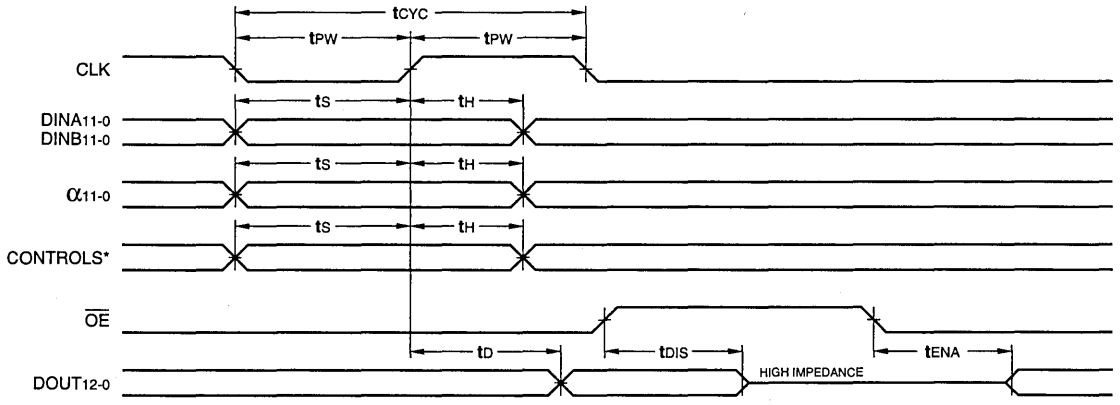
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –400 µA	2.6			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			120	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			500	µA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF48212–			
		25		20	
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	25		20	
t_{PW}	Clock Pulse Width	10		10	
t_S	Input Setup Time	10		10	
t_H	Input Hold Time	0		0	
t_D	Output Delay		13		13
t_{ENA}	Three-State Output Enable Delay (Note 11)		13		13
t_{DIS}	Three-State Output Disable Delay (Note 11)		13		13

SWITCHING WAVEFORMS: DATA I/O

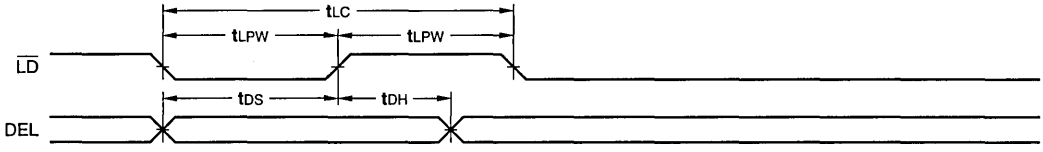


*includes MIXEN, $\overline{TC}$, and RND1-0.

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LF48212– 25 Min	LF48212– 25 Max	LF48212– 20 Min	LF48212– 20 Max
t_{LC}	LD Cycle Time	25		20	
t_{LPW}	LD Pulse Width	10		10	
t_{DS}	DEL Setup Time	12		12	
t_{DH}	DEL Hold Time	0		0	

SWITCHING WAVEFORMS: DELAY CONTROL REGISTER DATA



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 40 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

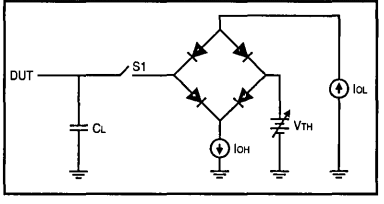
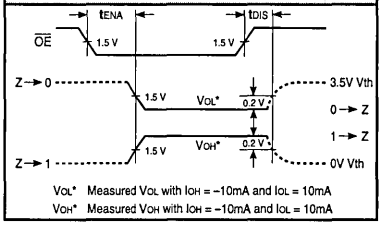


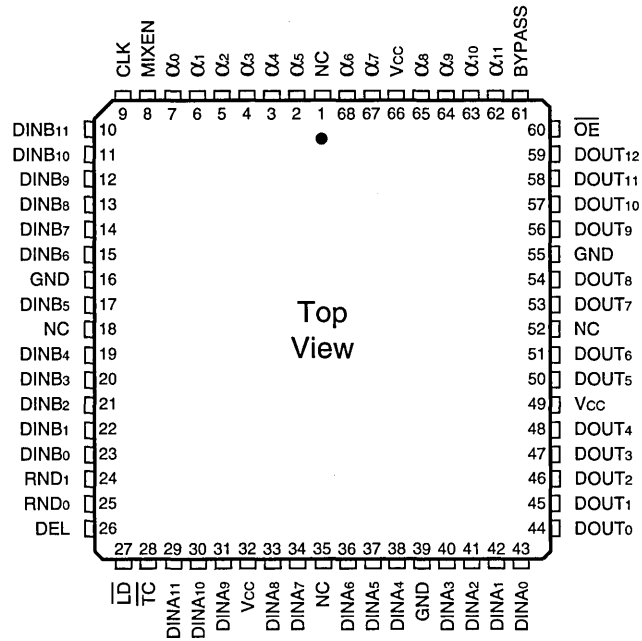
FIGURE B. THRESHOLD LEVELS



2

ORDERING INFORMATION

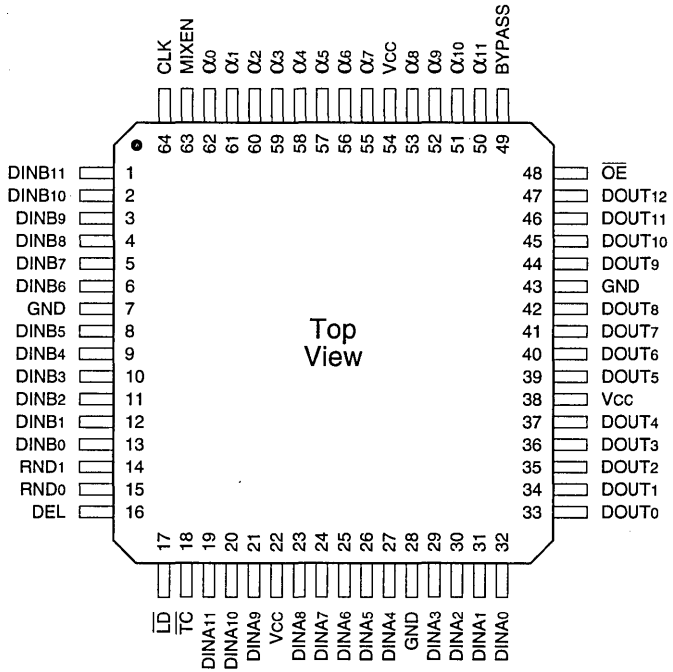
68-pin



Speed	Plastic J-Lead Chip Carrier (J2)
	0°C to +70°C — COMMERCIAL SCREENING
25 ns	LF48212JC25
20 ns	LF48212JC20

ORDERING INFORMATION

64-pin



Speed	Plastic Quad Flatpack (Q3)
	0°C to +70°C — COMMERCIAL SCREENING
25 ns	LF48212QC25
20 ns	LF48212QC20

LF48410
1024 x 24-bit Video Histogrammer

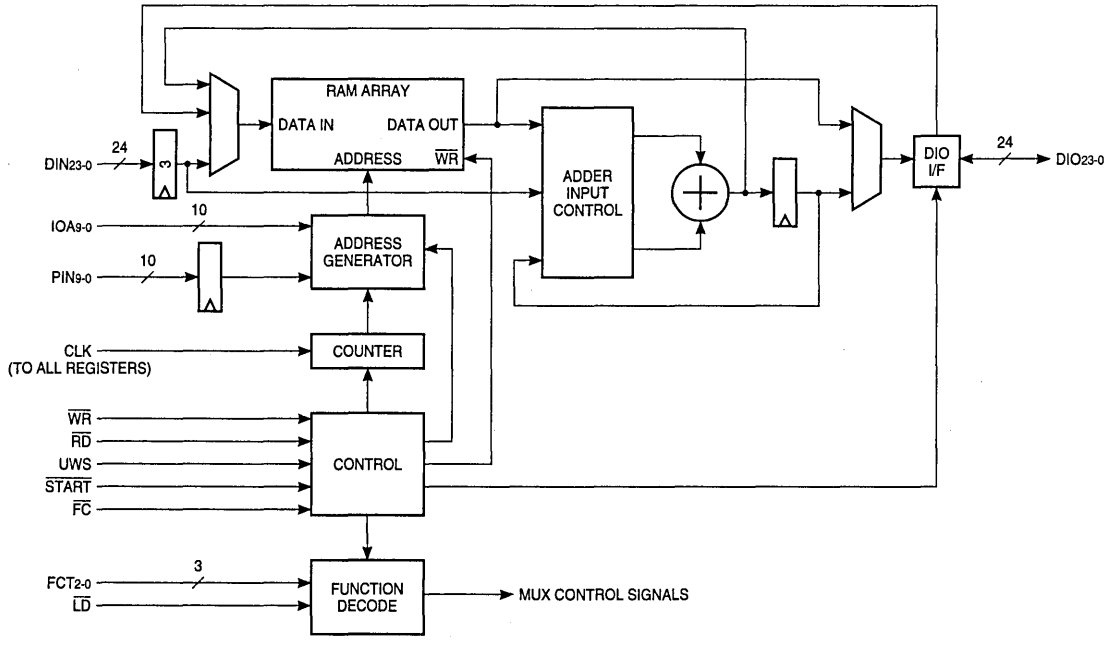
FEATURES

- 40 MHz Data Input and Computation Rate
- 1024 x 24-bit Memory Array
- Histograms of Images up to 4K x 4K with 10-bit Pixel Resolution
- Memory Array Flash Clear
- User-Programmable Modes: Histogram, Histogram Accumulate, Look Up Table, Bin Accumulate, Delay Memory, Delay and Subtract, Single Port RAM
- DECC SMD No. 5962-94573
- Available 100% Screened to MIL-STD-883, Class B
- Replaces Harris HSP48410 and HSP48410/883
- Package Styles Available:
  - 84-pin Plastic LCC, J-Lead
  - 84-pin Ceramic PGA

DESCRIPTION

The **LF48410** is capable of generating histograms and Cumulative Distribution Functions of video images. It may also be used as a look up table, a bin accumulator, a delay memory (delay and subtract also possible), or a single port RAM. The on-chip 1024 x 24-bit memory array facilitates histograms of images up to 4K x 4K pixels with a 10-bit pixel resolution. Once the histogram of a video image is stored in the memory array, the Cumulative Distribution Function can be calculated by putting the device in Histogram Accumulate Mode. Transformation functions can be performed on pixel values when the device is in Look Up Table Mode. If the Cumulative Distribution Function is the desired transformation function, the LF48410 can calculate it and have it available for Look Up Table Mode. When the device is in Delay Memory Mode, it functions as a video row buffer. In this mode, the LF48410 can buffer video lines as long as 1029 pixels. The device can also function as an asynchronous single port RAM. During asynchronous modes, the device can be configured as a 1024 x 24, 1024 x 16, or 1024 x 8-bit RAM. A Flash Clear function is provided which sets all memory array locations and data path registers to "0".

LF48410 Block Diagram



SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

When operating in a synchronous mode, the rising edge of CLK strobes all enabled registers. CLK has no effect when operating in an asynchronous mode.

Inputs

PIN9-0 — Pixel Data Input

PIN9-0 provides address information to the memory array in Histogram, Bin Accumulate, and Look Up Table Modes. Data is latched on the rising edge of CLK.

DIN23-0 — Data Input

In Bin Accumulate Mode, DIN23-0 provides data to the internal summer to be added to data already in the memory array. In Look Up Table Mode, DIN23-0 is used to load the memory array with the desired values. In Delay Memory Mode, the data to be delayed is input to the memory array using DIN23-0, and in Delay and Subtract Mode it also provides data to be subtracted from the delayed data. In all four modes, DIN23-0 is latched on the rising edge of CLK.

IOA9-0 — Asynchronous Address Input

IOA9-0 provides address information to the memory array in Asynchronous 16 and 24 Modes.

FCT2-0 — Function Input

FCT2-0 is used to put the LF48410 into one of its eight modes of operation (Table 1). Data is latched on the rising edge of $\overline{LD}$. To ensure proper operation of the device, $\overline{START}$ must be HIGH while changing modes, and there must be at least one rising edge of CLK between the rising edge of $\overline{LD}$ and the falling edge of $\overline{START}$.

Inputs/Outputs

DIO23-0 — Data Input/Output

In all synchronous modes, DIO23-0 is the 24-bit registered data output port. In all asynchronous modes, DIO23-0 is both the data input and data output port for the memory array.

Controls

$\overline{START}$ — Device Enable

$\overline{START}$ is used to enable and disable the synchronous modes of operation (except for the Delay Memory and Delay and Subtract Modes). The synchronous mode sections explain how $\overline{START}$ functions in each mode. $\overline{START}$ has no effect in asynchronous modes. Data is latched on the rising edge of CLK. $\overline{START}$ must be held HIGH when changing from one mode to another. To ensure proper operation of the device, there must be at least one rising edge of CLK between the rising edge of $\overline{LD}$ and the falling edge of $\overline{START}$.

$\overline{RD}$ — Read/Output Enable

In all synchronous modes, $\overline{RD}$ is used as an output enable for DIO23-0. When $\overline{RD}$ is LOW, DIO23-0 is enabled for output. When $\overline{RD}$ is HIGH, DIO23-0 is placed in a high-impedance state. In all asynchronous modes, $\overline{RD}$ is used as a read enable for the memory array (see asynchronous mode sections for details).

$\overline{WR}$ — Write Enable

In all asynchronous modes, $\overline{WR}$ is used as a write enable for the memory array (see asynchronous mode sections for details). $\overline{WR}$ has no effect in the synchronous modes.

UWS — Upper Word Select

UWS is only used in Asynchronous 16 Mode. If UWS is LOW and a memory write is performed, data on DIO15-0 is written to the lower 16 bits of the addressed 24-bit word. If UWS is LOW and a memory read is performed, the lower 16 bits of the addressed 24-bit word will be output on DIO15-0. If UWS is HIGH and a memory write is performed, data on DIO7-0 is written to the upper 8 bits of the addressed 24-bit word. If UWS is HIGH and a memory read is performed, the upper 8 bits of the addressed 24-bit word will be output on DIO7-0.

$\overline{FC}$ — Flash Clear

When $\overline{FC}$ is LOW, all memory array locations and data path registers are set to "0". To ensure that Flash Clear functions properly, $\overline{FC}$ should not be set LOW until $\overline{START}$ is HIGH (synchronous modes) or $\overline{WR}$ is HIGH (asynchronous modes).

$\overline{LD}$ — Function Load Strobe

Data present on FCT2-0 is latched into the LF48410 on the rising edge of $\overline{LD}$. To ensure proper operation of the device, there must be at least one rising edge of CLK between the rising edge of $\overline{LD}$ and the falling edge of $\overline{START}$.

TABLE 1. LF48410 MODES

FCT2-0			MODE
0	0	0	Histogram
0	0	1	Histogram Accumulate
0	1	0	Delay and Subtract
0	1	1	Look Up Table
1	0	0	Bin Accumulate
1	0	1	Delay Memory
1	1	0	Asynchronous 24
1	1	1	Asynchronous 16

HISTOGRAM MODE

When the LF48410 is in this mode, the chip is configured as shown in Figure 1. The memory array keeps track of how many times a particular pixel value is used in a video image. The pixel value is input on PIN9-0 and is latched on the rising edge of CLK. Data at the address defined by PIN9-0 is read out of the memory array and incremented by one. The data is then written back to the memory array, in the same location it was read from, and is also output on DIO23-0 (if $\overline{RD}$ is LOW). As long as $\overline{START}$ is LOW, the device will be enabled for Histogram Mode. When $\overline{START}$ is HIGH, the device will still read pixel values, but the addres-sed data will not be incremented. The unchanged data is output on DIO23-0 and is not written back to the memory array (writing is disabled). $\overline{START}$ is delayed internally three clock cycles to match the latency of the address generator.

FIGURE 1. HISTOGRAM MODE

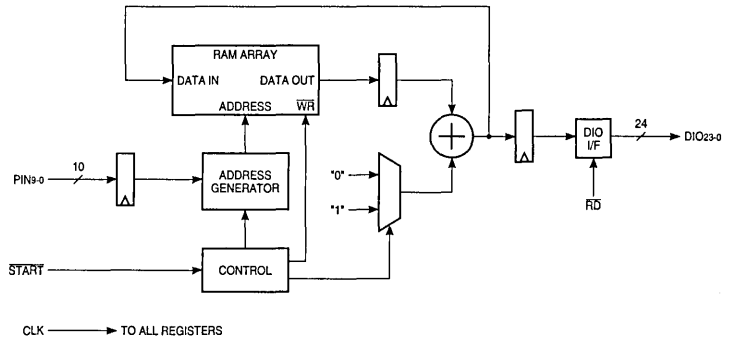
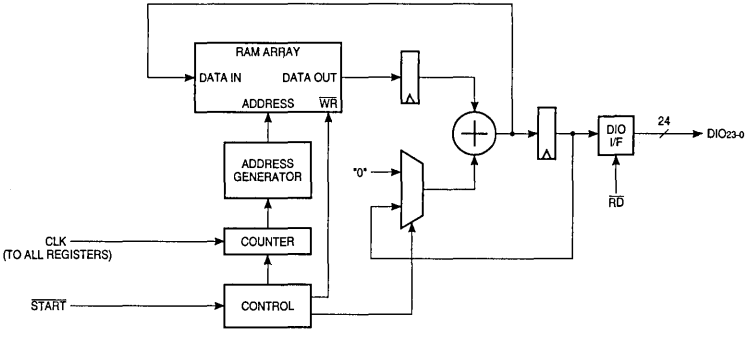


FIGURE 2. HISTOGRAM ACCUMULATE MODE



HISTOGRAM ACCUMULATE MODE

When the LF48410 is in this mode, the chip is configured as shown in Figure 2. This mode is used to calculate the Cumulative Distribution Function of a video image. Before this can be done, the histogram of the image must already be in the memory array. The internal counter is used to generate address data for the memory array. Data at the address defined by the counter is read out of the memory array and added to the sum of the data from all previous address locations. This new value is written back to the memory array, in the same location where the last read occurred, and is also output on DIO23-0 (if $\overline{RD}$ is LOW). After all memory locations with histogram data are accumulated, the memory array will contain the Cumulative Distribution Function.

After this mode is selected, the internal counter and all data path registers are reset to zero when $\overline{START}$ is set LOW. Every rising edge of CLK causes the counter to increment its output by one until the counter reaches a value of 1023. At this point, the counter will hold the value of 1023 and writing to the memory array will be disabled. As long as $\overline{START}$ is LOW, the device will be enabled for Histogram Accumulate Mode. When $\overline{START}$ is HIGH, the counter will still increment its address values, but the addressed data will not be added to anything. The unchanged data is output on DIO23-0 and is not written back to the memory array (writing is disabled). $\overline{START}$ is delayed internally three clock cycles to match the latency of the address generator.

LOOK UP TABLE MODE

When the LF48410 is in this mode, the chip is configured as shown in Figure 3. This mode is used to perform fixed transformation functions on pixel values. The transformation function can be loaded into the memory array in Look Up Table Write Mode, Asynchronous 16/24 Mode, or Histogram Accumulate Mode. In Look Up Table Write Mode, data is loaded into the memory array using DIN23-0, CLK, and $\overline{START}$. The internal counter is used to generate address data for the memory array. When $\overline{START}$ goes LOW, the counter is reset to zero. As long as $\overline{START}$ is LOW, data on DIN23-0 is latched on the rising edge of CLK and loaded

FIGURE 3. LOOK UP TABLE MODE

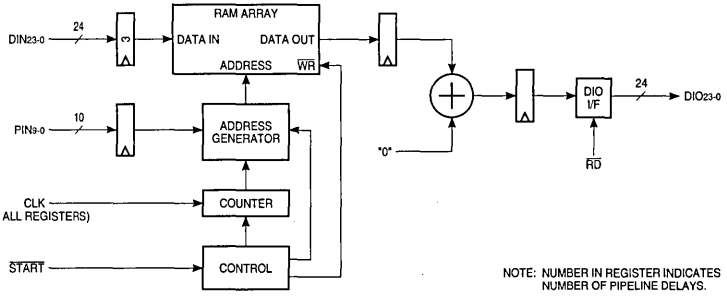
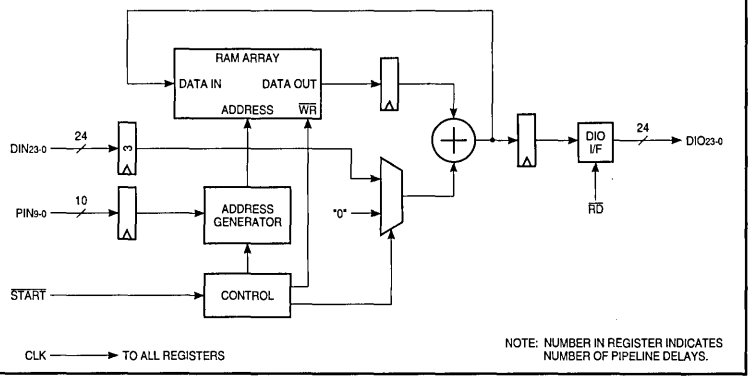


FIGURE 4. BIN ACCUMULATE MODE



into the memory array at the address defined by the counter. The value already in the memory array at that address is output on DIO23-0 (if $\overline{RD}$ is LOW). Every rising edge of CLK causes the counter to increment its output by one until the counter reaches a value of 1023. At this point, the counter will hold the value of 1023 and writing to the memory array will be disabled. DIN23-0 is delayed internally three clock cycles to match the latency of the address generator. In Asynchronous 16/24 Mode, data is loaded into the memory array as detailed in the asynchronous mode sections. If the Cumulative Distribution Function is the desired transformation function, the memory array will contain this data as soon as the Histogram Accumulate function has been completed.

Once the memory array contains the desired data, the device needs to be put in Look Up Table Read Mode by setting $\overline{START}$ HIGH. In Look Up Table Read Mode, pixel values are input on PIN9-0 and are latched on the rising edge of CLK. Data at the address defined by PIN9-0 is read out of the memory array and output on DIO23-0 (if $\overline{RD}$ is LOW). If Look Up Table Write Mode was used to load the memory array, it is important to wait until the third clock cycle after $\overline{START}$ goes HIGH to input data on PIN9-0 to insure that all data is written into the memory array before any reading is done.

BIN ACCUMULATE MODE

When the LF48410 is in this mode, the chip is configured as shown in Figure 4. PIN9-0 provides address data for the memory array and is latched on the rising edge of CLK. Data at the address defined by PIN9-0 is read out of the memory array and added to the data on DIN23-0. This new value is written back to the memory array, in the same location where the last read occured, and is also output on DIO23-0 (if $\overline{RD}$ is LOW). As long as $\overline{START}$ is LOW, the device will be enabled for Bin Accumulate Mode. When $\overline{START}$ is HIGH, the device will still read address values on PIN9-0, but the addressed data will not be added to anything. The unchanged data will be output on DIO23-0 and is not written back to the memory array (writing is disabled). $\overline{START}$ and DIN23-0 are delayed internally three clock cycles to match the latency of the address generator.

DELAY MEMORY MODE

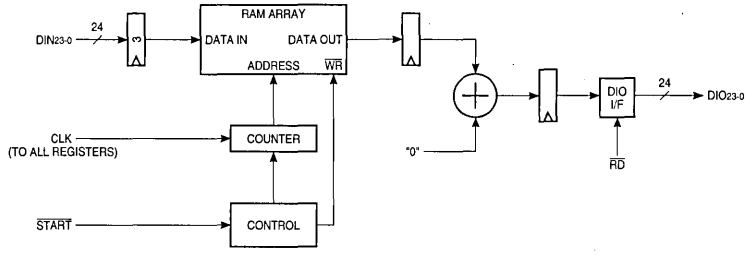
When the LF48410 is in this mode, the chip is configured as shown in Figure 5. This mode allows the device to function as a row buffer. The internal counter is used to generate address data for the memory array. When $\overline{START}$ goes LOW, the counter is reset to zero. Delay length (row length) is determined by reseting the counter every N–4 clock cycles, where N is the number of delays. For

example, to set the number of delays to 10, $\overline{START}$ would have to be set LOW every 6 cycles. The maximum delay length is 1029 and the minimum delay length is 6. Data on DIN23-0 is latched on the rising edge of CLK and loaded into the memory array at the address defined by the counter. Data is output on DIO23-0 (if $\overline{RD}$ is LOW). If the counter reaches the value of 1023, the counter will hold this value and writing to the memory array will be disabled.

DELAY AND SUBTRACT MODE

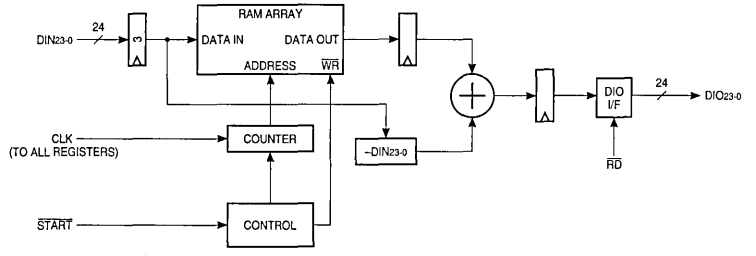
When the LF48410 is in this mode, the chip is configured as shown in Figure 6. The internal counter is used to generate address data for the memory array. When $\overline{START}$ goes LOW, the counter is reset to zero. Delay length (row length) is determined by reseting the counter every N–4 clock cycles, where N is the number of delays. The maximum delay length is 1029 and the minimum delay length is 6. Data on DIN23-0 is latched on the rising edge of CLK and loaded into the memory array at the address defined by the counter. Data is output on DIO23-0 (if $\overline{RD}$ is LOW). Before data read from the memory array is output to DIO23-0, input data is subtracted from it according to the following formula: $OUT_C = D_{(C-N+1)} - D_{(C-3)}$. OUT_C is the data sent to the output port (DIO23-0) on clock cycle C. $D_{(C-N+1)}$ is the data latched into the device on clock cycle C–N+1, and $D_{(C-3)}$ is the data latched into the device on clock cycle C–3. N is the number of delays. For example, to determine what will be output on DIO23-0 on clock cycle 12 when the device is set for 10 delays, set C=12 and N=10 to obtain: $OUT_{12} = D_3 - D_9$. If the counter reaches the value of 1023, the counter will hold this value and writing to the memory array will be disabled.

FIGURE 5. DELAY MEMORY MODE



NOTE: NUMBER IN REGISTER INDICATES NUMBER OF PIPELINE DELAYS.

FIGURE 6. DELAY AND SUBTRACT MODE



NOTE: NUMBER IN REGISTER INDICATES NUMBER OF PIPELINE DELAYS.

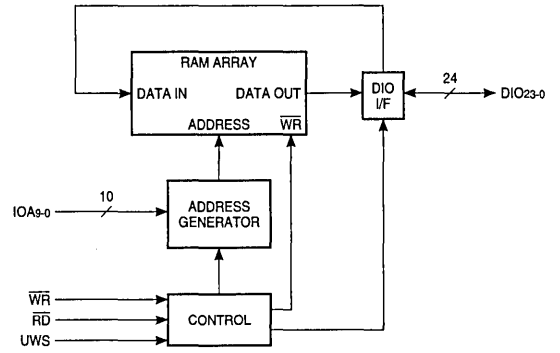
ASYNCHRONOUS 16 MODE

When the LF48410 is in this mode, the chip is configured as shown in Figure 7. This mode allows the device to function as an asynchronous single port RAM. Each 24-bit memory location is split into two parts, the lower 16 bits and the upper 8 bits. IOA9-0 addresses the 24-bit memory locations, and UWS addresses the lower 16 or upper 8 bits of those locations. If UWS is LOW, the lower 16 bits of the 24-bit memory location are addressed. If UWS is HIGH, the upper 8 bits are addressed. Address data on IOA9-0 and UWS is latched into the device on the falling edge of $\overline{RD}$ or $\overline{WR}$. If $\overline{RD}$ latches the address data, a memory read is performed. Data at the specified address is output on DIO15-0 (if UWS was latched LOW) or DIO7-0 (if UWS was latched HIGH). If UWS was latched LOW/HIGH, DIO16-23/DIO8-23 will output zeros during a memory read. If $\overline{WR}$ latches the address data, a memory write is performed. After the falling edge of $\overline{WR}$ latches the address, data on DIO15-0 (if UWS was latched LOW) or DIO7-0 (if UWS was latched HIGH) is written to the RAM on the rising edge of $\overline{WR}$.

ASYNCHRONOUS 24 MODE

When the LF48410 is in this mode, the chip is configured as shown in Figure 7. In this mode, the device functions the same as when in Asynchronous 16 Mode except that the 24-bit memory locations are not split into two parts. All 24 bits are used during a read or write operation. When reading, data is output on DIO23-0. When writing, data is input on DIO23-0. UWS is not used in this mode.

FIGURE 7. ASYNCHRONOUS 16/24 MODE



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.6			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			310	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			500	µA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			12	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			12	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

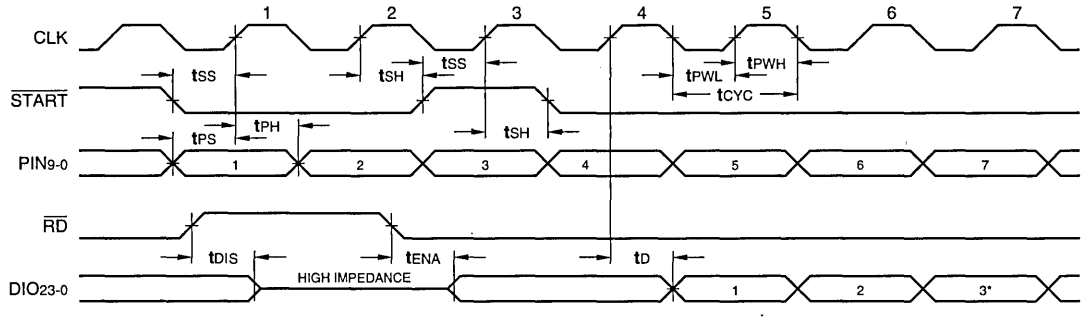
Symbol	Parameter	LF48410– 30 Min	30 Max	25 Min	25 Max
t_{CYC}	Cycle Time	30		25	
t_{PWL}	Clock Pulse Width Low	12		10	
t_{PWH}	Clock Pulse Width High	12		10	
t_{PS}	PIN_{9-0} Setup Time	13		12	
t_{PH}	PIN_{9-0} Hold Time	0		0	
t_{DS}	DIN_{23-0} Setup Time	13		12	
t_{DH}	DIN_{23-0} Hold Time	0		0	
t_{SS}	$\overline{START}$ Setup Time	13		12	
t_{SH}	$\overline{START}$ Hold Time	0		0	
t_{CY}	Read/Write Cycle Time	65		55	
t_{AS}	Address Setup Time	15		13	
t_{AH}	Address Hold Time	1		1	
t_{WL}	$\overline{WR}$ Pulse Width Low	15		12	
t_{WH}	$\overline{WR}$ Pulse Width High	15		12	
t_{WDS}	DIO_{23-0} Setup Time	15		12	
t_{WDH}	DIO_{23-0} Hold Time	1		1	
t_{RL}	$\overline{RD}$ Pulse Width Low	43		35	
t_{RH}	$\overline{RD}$ Pulse Width High	17		15	
t_{RD}	$\overline{RD}$ Low to DIO_{23-0} Valid		43		35
t_{OH}	$\overline{RD}$ High to DIO_{23-0} Valid		0		0
t_{LL}	$\overline{LD}$ Pulse Width	12		10	
t_{LS}	$\overline{LD}$ Setup to $\overline{START}$	30		25	
t_{FS}	FCT_{2-0} Setup Time	10		10	
t_{FH}	FCT_{2-0} Hold Time	0		0	
t_{FL}	$\overline{FC}$ Pulse Width	35		35	
t_D	Output Delay		19		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		19		18
t_{DIS}	Three-State Output Disable Delay (Note 11)		19		18

SWITCHING CHARACTERISTICS

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

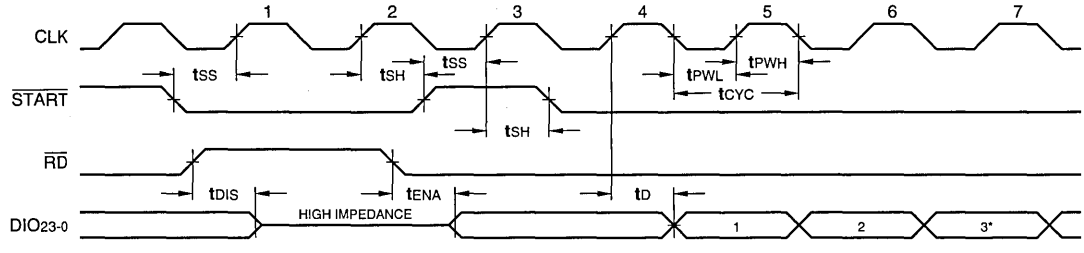
		LF48410–			
		39		30	
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	39		30	
t_{PWL}	Clock Pulse Width Low	15		12	
t_{PWH}	Clock Pulse Width High	15		12	
t_{PS}	PIN_{9-0} Setup Time	16		15	
t_{PH}	PIN_{9-0} Hold Time	1		1	
t_{DS}	DIN_{23-0} Setup Time	16		15	
t_{DH}	DIN_{23-0} Hold Time	1		1	
t_{SS}	$\overline{START}$ Setup Time	16		15	
t_{SH}	$\overline{START}$ Hold Time	0		0	
t_{CY}	Read/Write Cycle Time	80		65	
t_{AS}	Address Setup Time	20		16	
t_{AH}	Address Hold Time	2		2	
t_{WL}	$\overline{WR}$ Pulse Width Low	20		15	
t_{WH}	$\overline{WR}$ Pulse Width High	20		15	
t_{WDS}	DIO_{23-0} Setup Time	20		16	
t_{WDH}	DIO_{23-0} Hold Time	2		2	
t_{RL}	$\overline{RD}$ Pulse Width Low	55		43	
t_{RH}	$\overline{RD}$ Pulse Width High	20		17	
t_{RD}	$\overline{RD}$ Low to DIO_{23-0} Valid		55		43
t_{OH}	$\overline{RD}$ High to DIO_{23-0} High Z	0		0	
t_{LL}	$\overline{LD}$ Pulse Width	15		12	
t_{LS}	$\overline{LD}$ Setup to $\overline{START}$	39		30	
t_{FS}	FCT_{2-0} Setup Time	15		12	
t_{FH}	FCT_{2-0} Hold Time	1		1	
t_{FL}	$\overline{FC}$ Pulse Width	35		35	
t_D	Output Delay		24		19
t_{ENA}	Three-State Output Enable Delay (Note 11)		24		19
t_{DIS}	Three-State Output Disable Delay (Note 11)		27		27

Switching Waveforms: Histogram Mode



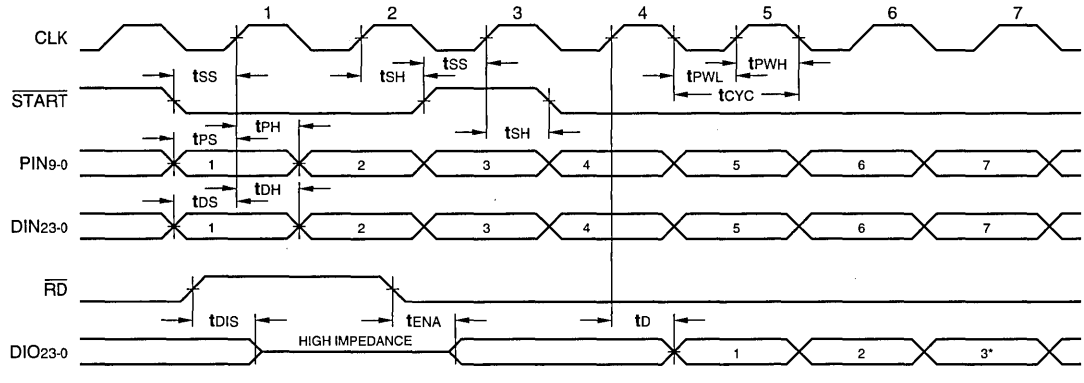
*RAM contents not changed.

Switching Waveforms: Histogram Accumulate Mode



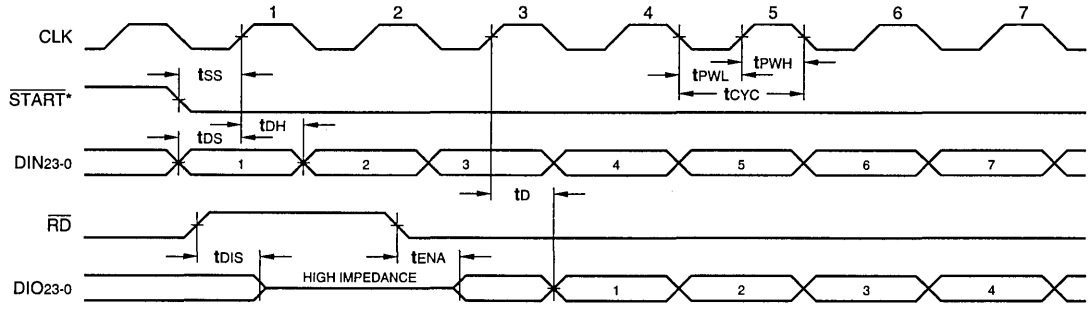
*RAM contents not changed.

Switching Waveforms: Bin Accumulate Mode



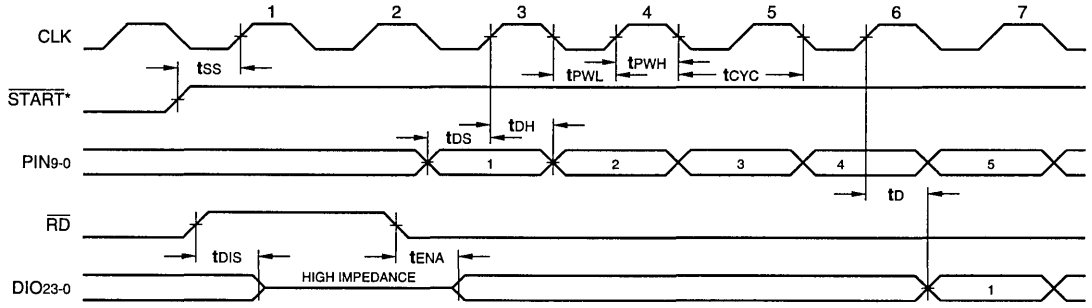
*RAM contents not changed.

Switching Waveforms: Look Up Table Write Mode



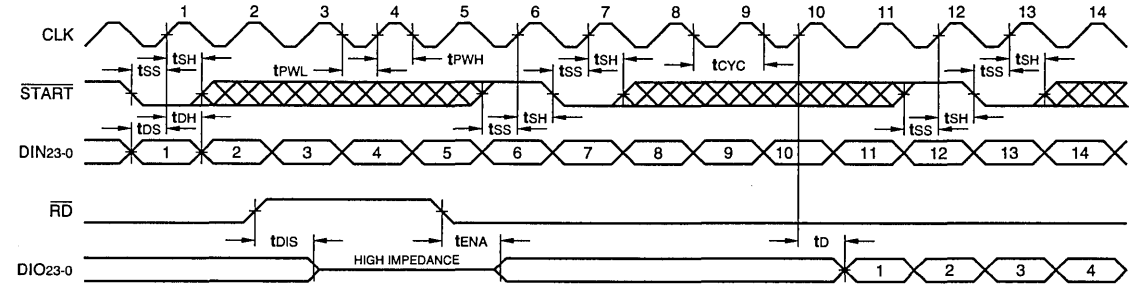
*$\overline{START}$ must be held LOW a minimum of t_{SH} after the rising edge of CLK that loads the last value of DIN_{23-0}.

Switching Waveforms: Look Up Table Read Mode



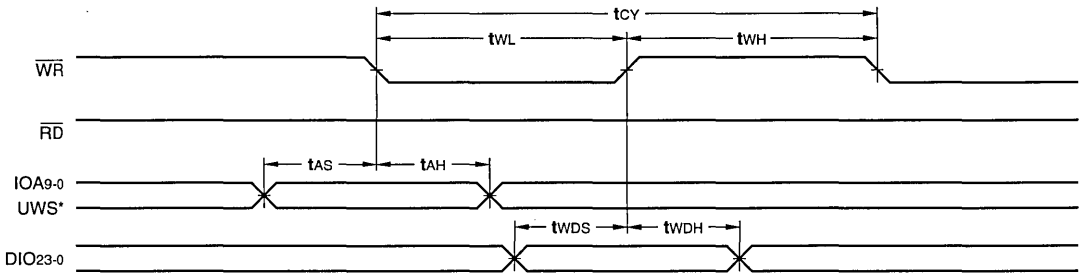
*$\overline{START}$ must be held HIGH a minimum of t_{SH} after the rising edge of CLK that loads the last value of PIN_{9-0}.

Switching Waveforms: Delay Memory/Delay And Subtract Mode



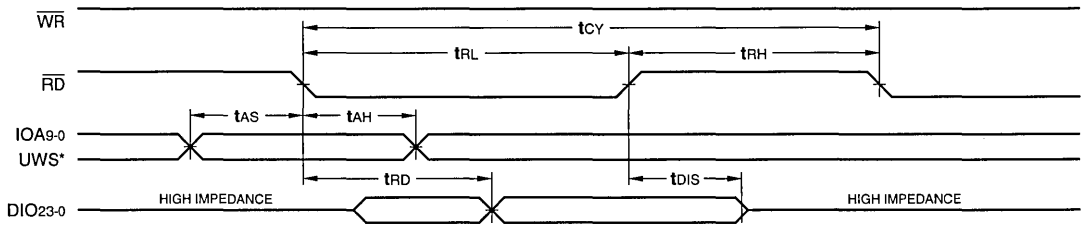
Shown are the waveforms for a delay length of 10.

Switching Waveforms: Asynchronous Write 16/24 Mode



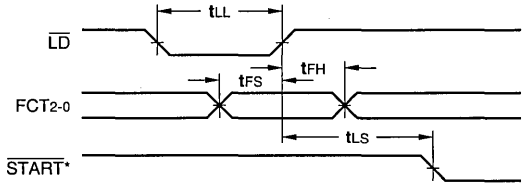
*applies only to 16-bit Asynchronous Mode.

Switching Waveforms: Asynchronous Read 16/24 Mode



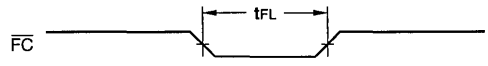
*applies only to 16-bit Asynchronous Mode.

Switching Waveforms: Fucntion Load



*there must be at least one rising edge of CLK between the rising edge of $\overline{LD}$ and the falling edge of $\overline{START}$.

Switching Waveforms: Flash Clear



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

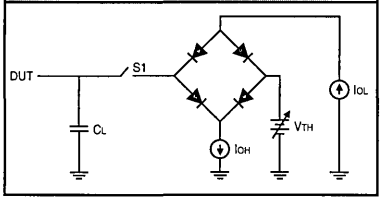
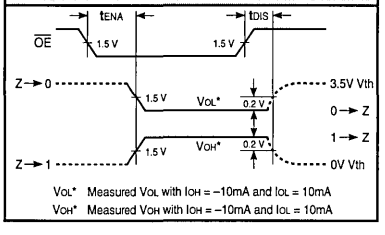
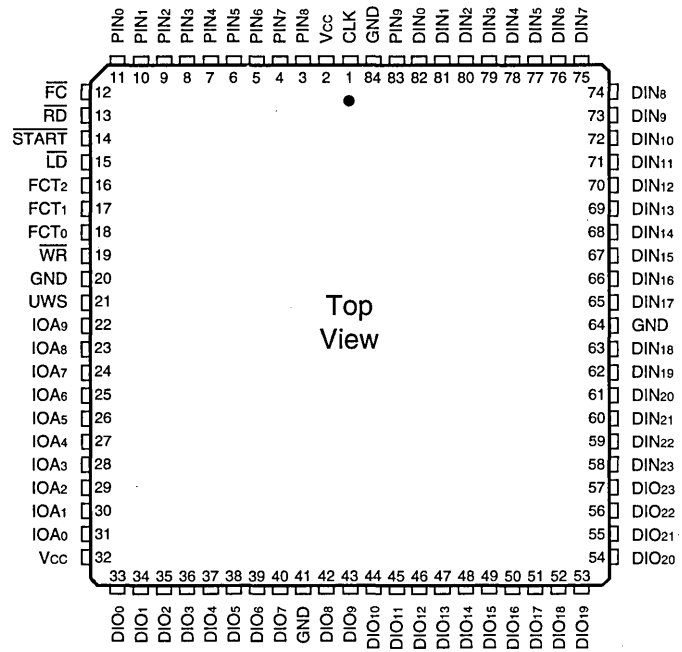


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

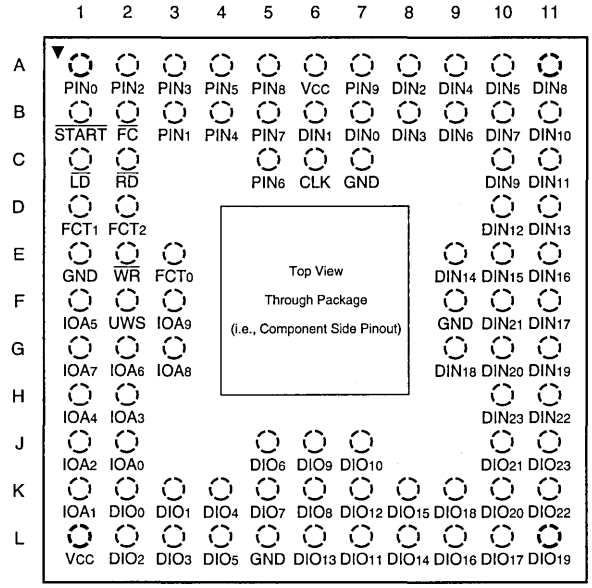
84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — COMMERCIAL SCREENING
30 ns	LF48410JC30
25 ns	LF48410JC25

ORDERING INFORMATION

84-pin



Speed	Ceramic Pin Grid Array (G3)
	0°C to +70°C — COMMERCIAL SCREENING
30 ns	LF48410GC30
25 ns	LF48410GC25
	–55°C to +125°C — COMMERCIAL SCREENING
39 ns	LF48410GM39
30 ns	LF48410GM30
	–55°C to +125°C — MIL-STD-883 COMPLIANT
39 ns	LF48410GMB39
30 ns	LF48410GMB30

LF48908
Two Dimensional Convolver

FEATURES

- 40 MHz Data and Computation Rate
- Nine Multiplier Array with 8-bit Data and 8-bit Coefficient Inputs
- Separate Cascade Input and Output Ports
- On-board Programmable Row Buffers
- Two Coefficient Mask Registers
- On-board 8-bit ALU
- Two's Complement or Unsigned Operands
- Replaces Harris HSP48908
- DECC SMD No. 5962-93007
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 84-pin Plastic LCC, J-Lead
  - 100-pin Plastic Quad Flatpack
  - 84-pin Ceramic PGA

DESCRIPTION

The **LF48908** is a high-speed two dimensional convolver that implements a 3 x 3 kernel convolution at real-time video rates. Programmable row buffers are located on-chip, eliminating the need for external data storage. Each row buffer can store up to 1024 pixels. Two internal register banks are provided allowing two separate sets of filter coefficients to be stored simultaneously. Adaptive filter operations are possible when both register banks are used. An on-chip ALU is provided, allowing real-time arithmetic and logical pixel point operations to be performed on the image data. The 3 x 3 convolver comprises nine 8 x 8-bit multipliers, various pipeline registers, and summers. A complete sum-of-products operation is performed every clock cycle. The $\overline{\text{FRAME}}$ signal resets all data registers without affecting the control and coefficient registers.

Pixel and coefficient input data are both 8-bits and can be either signed or unsigned integers. Image data should be in a raster scan non-interlaced format. The LF48908 can internally store images as wide as 1024 pixels for the 3 x 3 convolution. By using external row buffers and multiple LF48908s, longer pixel rows can be used and convolutions with larger kernel sizes can be performed. Output data is 20-bits and this guarantees no overflow for kernel sizes up to 4 x 4. A separate cascade input is used as the data input for summing results from multiple LF48908s. It can also function as the data input path when external line buffers are used.

FIGURE 1. LF48908 BLOCK DIAGRAM

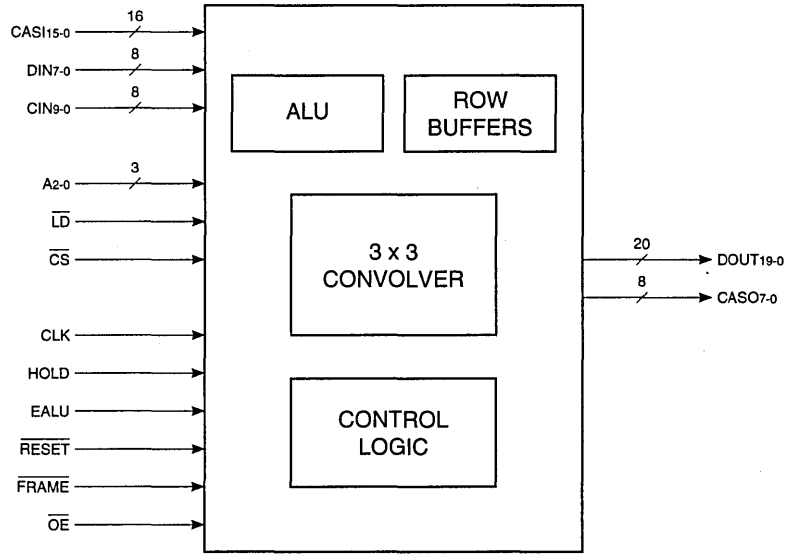
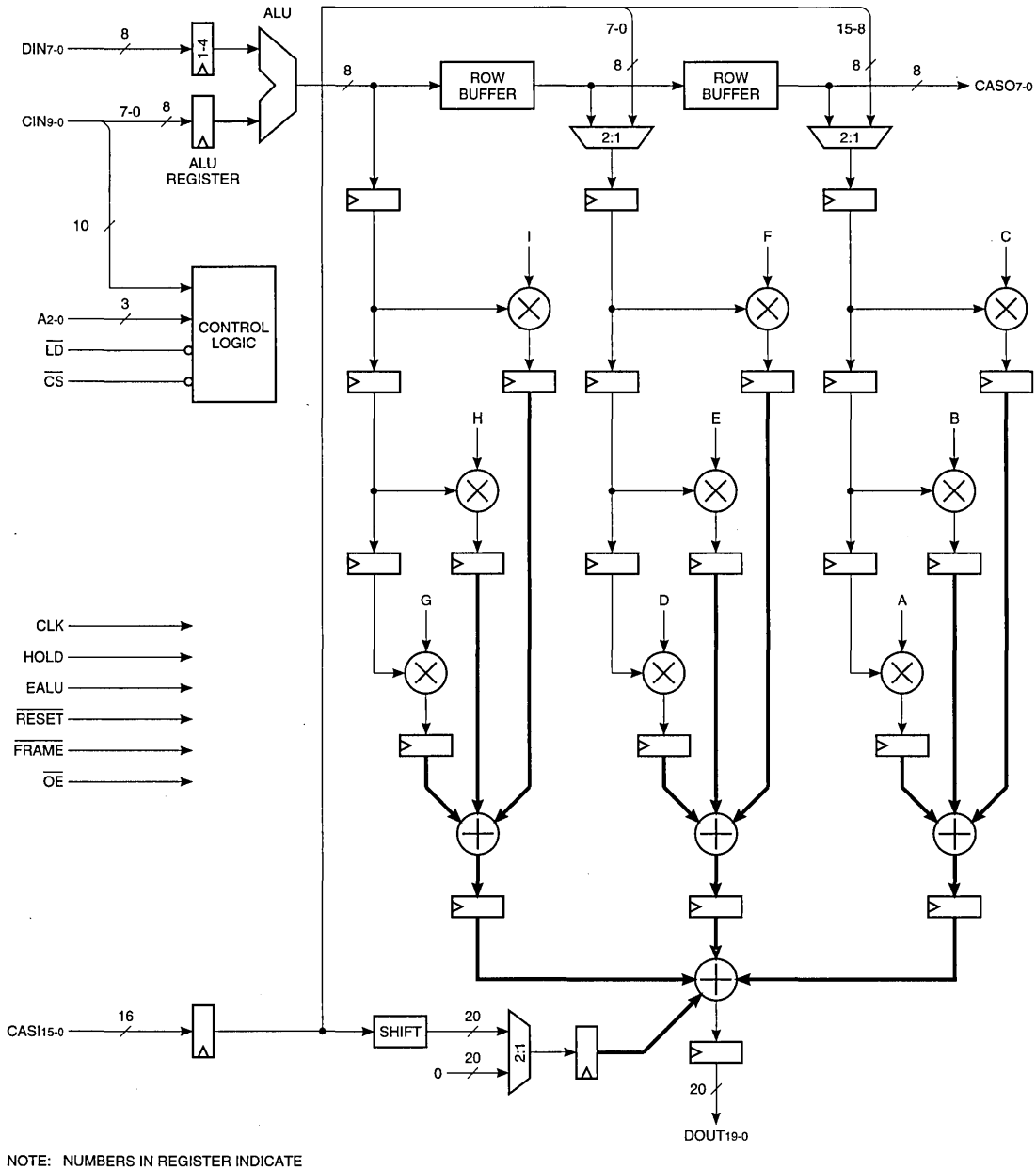


FIGURE 2. LF48908 FUNCTIONAL BLOCK DIAGRAM



NOTE: NUMBERS IN REGISTER INDICATE NUMBER OF PIPELINE DELAYS.

SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers except for the Control Logic Registers.

Inputs

DIN7-0 — Pixel Data Input

DIN7-0 is the 8-bit registered pixel data input port. Data is latched on the rising edge of CLK.

CIN9-0 — Coefficient and Control Logic Register Input

CIN7-0 is used to load the Coefficient Registers or can be used to provide a second operand input to the ALU. CIN8-0 is used to load the Initialization Register. CIN9-0 is used to load the ALU Microcode and Row Buffer Length Registers. The Control Register Address Lines, A2-0, determine which register will receive the CIN data. The CIN data is loaded into the addressed register by using the $\overline{CS}$ and $\overline{LD}$ control inputs.

CASI15-0 — Cascade Input

The cascade input is used when multiple LF48908s are cascaded together or when external row buffers are needed. This allows convolutions of larger kernels or longer row sizes.

Outputs

DOUT19-0 — Data Output

DOUT19-0 is the 20-bit registered data output port.

CASO7-0 — Cascade Output

The data presented on CASO7-0 is the internal ALU output delayed by twice the programmed internal row buffer length.

Controls

$\overline{RESET}$ — Reset Control

When $\overline{RESET}$ is LOW, all internal circuitry is reset, all outputs are forced LOW, all Control Logic Registers are loaded with their default values (which is 0 for each one except the ALU Microcode Register which has a default value of "0000011000"), and all other internal registers are loaded with a "0".

$\overline{FRAME}$ — New Frame Input Control

When asserted, $\overline{FRAME}$ signals the start of a new frame. When $\overline{FRAME}$ is LOW, all internal circuitry is reset except for the ALU Microcode, Row Length, Initialization, Coefficient, and ALU Registers.

EALU — Enable ALU Register Input

When HIGH, data on CIN7-0 is latched into the ALU Register on the next rising edge of CLK. When LOW, data on CIN7-0 will not be latched into the ALU Register and the register contents will not be changed.

HOLD — Hold Control

The HOLD input is used to disable CLK from all of the internal circuitry. HOLD is latched on the rising edge of CLK and takes effect on the next rising edge of CLK. When HOLD is HIGH, CLK will have no effect on the LF48908 and all internal data will remain unchanged.

$\overline{OE}$ — Output Enable

When $\overline{OE}$ is LOW, DOUT19-0 is enabled for output. When $\overline{OE}$ is HIGH, DOUT19-0 is placed in a high-impedance state.

A2-0 — Control Logic Address Lines

A2-0 determines which Control Logic Register will receive the CIN9-0 data.

$\overline{CS}$ — Chip Select

When $\overline{CS}$ is LOW, data can be loaded into the Control Logic Registers. When $\overline{CS}$ is HIGH, data can not be loaded and the register contents will not be changed.

$\overline{LD}$ — Load Strobe

If $\overline{CS}$ and $\overline{LD}$ are LOW, the data present on CIN9-0 will be latched into the Control Logic Register addressed by A2-0 on the rising edge of $\overline{LD}$.

FUNCTIONAL DESCRIPTION

The LF48908, a two-dimensional convolver, executes convolutions using internal row buffers to reduce design complexity and board space requirements. 8-bit image data, in raster scan, non-interlace format, is convolved with one of two internal, 3 x 3 user-programable filter kernels. Two 1024 x 8-bit row buffers provide the data delay needed to perform two-dimensional convolutions on a single chip. The result output of 20-bits allows for word growth during the convolution operation.

The input data path (DIN7-0) provides access to an 8-bit ALU. This allows point operations to be performed on the incoming data stream before reaching the row buffers and the convolver. The length of these buffers is programmable for use in various video formats without the need for additional external delay.

This device is configured by loading the coefficent data (filter kernels) and row buffer length through the coefficent data path (CIN7-0). Internal registers are addressed using the A2-0 address lines. Chip Select ($\overline{CS}$) and Load Strobe ($\overline{LD}$) complete the configuration interface which may be controlled by standard microprocessors without additional external logic.

The filtered image data is output on the Data Output bus (DOUT19-0). This bus is registered with three-state drivers to facilatate use on a standard microprocessor system bus.

Data Input

Image data is input to the 3 x 3 convolver using DIN7-0. Data present on DIN7-0 is latched into a programmable pipeline delay on the rising edge of CLK. The programmable pipeline delay (1 to 4 clock cycles) allows for synchronization of input data when multiple LF48908s are cascaded together to perform larger convolutions. This delay is programed via the Initialization Register (see Table 3). The image data format, unsigned or two's complement, is also controlled by this register.

Coefficient data is input to the 3 x 3 convolver using either of two Coefficient Registers (CREG0 or CREG1). The Coefficient Registers are loaded through CIN7-0 using the A2-0, $\overline{CS}$, and $\overline{LD}$ controls. The coefficient data format, unsigned or two's complement, is determined by the Initialization Register.

Arithmetic Logic Unit

The input data path ALU with shifter allows pixel point operations to be performed on the incoming image. These operations include arithmetic functions, logical masking, and left/right shifts. The 10-bit ALU Microcode Register controls the various operations. The three upper bits control the shift amount and direction while the seven lower bits determine the arithmetic or logical operation. The shift operation is performed on the output of the ALU. This shift operation is independent of the arithmetic or logical operation of the ALU.

Tables 1 and 2 show the operations of the ALU Microcode Register. The "A" operand comes from the DIN input data path, while the "B" operand is taken from the ALU Register. The ALU Register is loaded using CIN7-0 and EALU. With EALU HIGH, data from CIN7-0 is loaded into the ALU Register on the rising edge of CLK. With EALU LOW, the data is held in the ALU Register. Since CIN7-0 is also used to load the Control Logic Registers, it is possible to overwrite data in those registers if $\overline{CS}$ and $\overline{LD}$ are active when loading the ALU Register. Therefore, special care must be taken to ensure that $\overline{CS}$ and $\overline{LD}$ are not active when writing to the ALU Register.

Programmable Row Buffers

The two internal row buffers provide the delay needed to perform the two-dimensional convolution. The row buffers function like 8-bit serial shift registers with a user-programmable delay from 1 to 1024 stages (it is possible to select delay stages of 1 or 2, but this leads to meaningless results for a 3 x 3 kernel convolution). The row buffer length is set via the Row Length Register (see Row Length Register Section). The row buffers are connected in series to provide the proper pixel information to the multiplier array. The Cascade Output (CASO7-0) provides a 2X row delay of the input data allowing for cascading of LF48908s to handle larger frames and/or kernel sizes. If more than 1024 delay stages are needed, it is possible to use external row buffers and bypass the internal row buffers. Bit 0 of the Initialization Register determines if internal or external row buffers are used. If Bit 0 is a "0", the internal row buffers are used. If Bit 0 is a "1", the internal row buffers are bypassed and external row buffers may be used.

3 x 3 Multiplier Array

The multiplier array comprises nine 8 x 8-bit multipliers. The active Coefficient Register supplies the coefficents to each of the multipliers, while the pixel data comes from the data input path and row buffers. The array forms a sum-of-products result as defined by the equation listed in Figure 3.

CONTROL LOGIC

Four sets of registers, the ALU Microcode, Row Length, Initialization, and Coefficient, define the Control Logic section. These registers are updated

FIGURE 3. MULTIPLIER ARRAY OUTPUT

PIXEL INPUT DATA

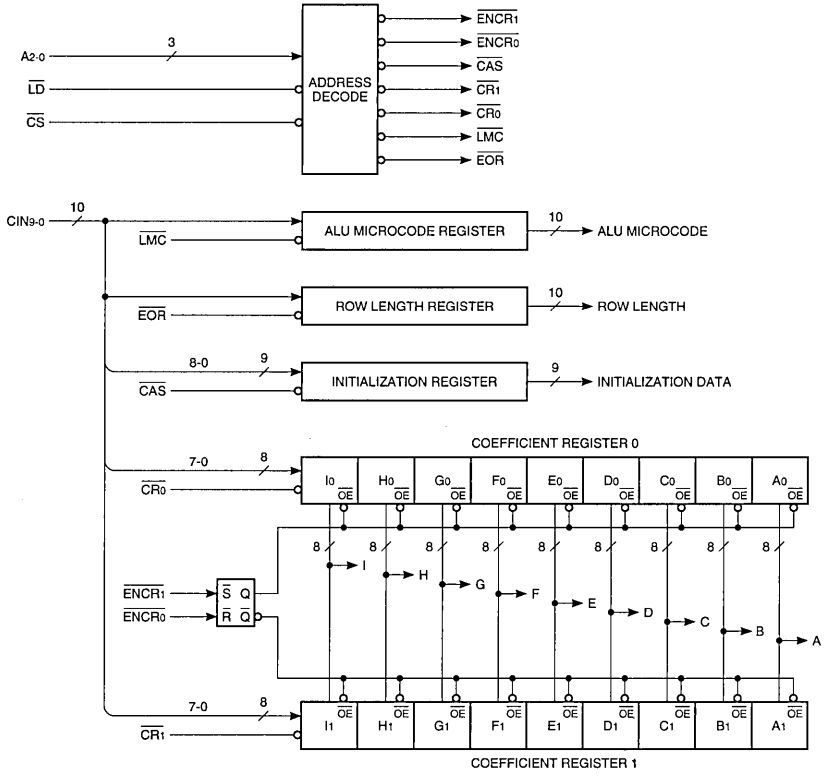
P1	P2	P3
P4	P5	P6
P7	P8	P9

FILTER KERNEL

A	B	C
D	E	F
G	H	I

MULTIPLIER ARRAY OUTPUT = A(P1) + B(P2) + C(P3)
+ D(P4) + E(P5) + F(P6)
+ G(P7) + H(P8) + I(P9)

FIGURE 4. LF48908 CONTROL LOGIC BLOCK DIAGRAM



through the CIN bus using A2-0, $\overline{CS}$, and $\overline{LD}$ (see Figure 4). All the Control Logic Registers are set to their default values when $\overline{RESET}$ is active. $\overline{FRAME}$ does not affect the values in these registers.

ALU Microcode Register

Operation of the ALU and shifter are determined by the value stored in the ALU Microcode Register. This 10-bit instruction word is divided into two fields. The lower seven bits define the arithmetic and logical operations of the ALU. The upper three bits specify shift distance and direction. Tables 1 and 2 detail the various instruction words. This register is loaded through CIN9-0 using the A2-0, $\overline{CS}$, and $\overline{LD}$ controls. Also see Arithmetic Logic Unit section.

Row Length Register

The value stored in the Row Length Register determines the number of delay stages for each row buffer. The number of delay stages should be set equal to the row length of the input image. The Row Length Register may be loaded with the values 0 through 1023 (0 represents 1024 delay stages). It is possible to program the row buffers to have 1 or 2 delay stages, but this will lead to meaningless results for a 3 x 3 convolution. This register is loaded through CIN9-0 using the A2-0, $\overline{CS}$, and $\overline{LD}$ controls. Once the Row Length Register has been loaded, a new value can not be loaded until the LF48908 has been reset. This is done by asserting $\overline{RESET}$. After $\overline{RESET}$ goes HIGH, the Row Length Register must be loaded within 1024 CLK cycles. If the Row Length Register is not loaded within 1024 CLK cycles, the register will automatically be loaded with a "0".

Initialization Register

The Initialization Register configures various functions of the device including: input data delay, input data format, coefficent data format, output rounding, cascade mode, and cascade input shift (see Table 3). This register is loaded through CIN8-0 using the A2-0, $\overline{CS}$, and $\overline{LD}$ controls.

Coefficient Registers - CREG0, CREG1

The Coefficient Registers are used to store the filter coefficients for the multiplier array. Each Coefficient

TABLE 1. ALU SHIFT OPERATIONS

ALU MICROCODE REGISTER			
REGISTER BIT			
9	8	7	OPERATION
0	0	0	No Shift (Default)
0	0	1	Shift Right 1
0	1	0	Shift Right 2
0	1	1	Shift Right 3
1	0	0	Shift Left 1
1	0	1	Shift Left 2
1	1	0	Shift Left 3
1	1	1	Not Valid

TABLE 2. ALU LOGICAL AND ARITHMETIC OPERATIONS

ALU MICROCODE REGISTER							
REGISTER BIT							
6	5	4	3	2	1	0	OPERATION
0	0	0	0	0	0	0	Logical (00000000)
1	1	1	1	0	0	0	Logical (11111111)
0	0	1	1	0	0	0	Logical (A) (Default)
0	1	0	1	0	0	0	Logical (B)
1	1	0	0	0	0	0	Logical ($\overline{A}$)
1	0	1	0	0	0	0	Logical ($\overline{B}$)
0	1	1	0	0	0	1	Arithmetic (A + B)
1	0	0	1	0	1	0	Arithmetic (A – B)
1	0	0	1	1	0	0	Arithmetic (B – A)
0	0	0	1	0	0	0	Logical (A AND B)
0	0	1	0	0	0	0	Logical (A AND $\overline{B}$)
0	1	0	0	0	0	0	Logical ($\overline{A}$ AND B)
0	1	1	1	0	0	0	Logical (A OR B)
1	0	1	1	0	0	0	Logical (A OR $\overline{B}$)
1	1	0	1	0	0	0	Logical ($\overline{A}$ OR B)
1	1	1	0	0	0	0	Logical (A NAND B)
1	0	0	0	0	0	0	Logical (A NOR B)
0	1	1	0	0	0	0	Logical (A XOR B)
1	0	0	1	0	0	0	Logical (A XNOR B)

Register can hold nine 8-bit values. This allows two different 3 x 3 filter kernels to be stored simultaneously on the LF48908. The outputs of CREG0 and CREG1 are connected to the coefficient inputs of the multiplier array (A through I). The register used to supply the coefficient data is determined by the address written to the Address Decoder. If a "101" is written to the Address Decoder, CREG0 will provide the coefficient data. If a "110" is written to the Address Decoder, CREG1 will be used. It is possible to switch between the two Coefficient Registers in real time. This facilitates adaptive filtering operations. It is important to remember to meet the t_{LCS} timing specification when switching the Coefficient Registers. When a Coefficient Register is selected to supply data to the multiplier array (one of the registers is always selected), all of its outputs are enabled simultaneously. When $\overline{RESET}$ is asserted, CREG0 is the default register selected to supply the coefficient data.

CREG0 and CREG1 are loaded through CIN_{7-0} using the A_{2-0}, $\overline{CS}$, and $\overline{LD}$ controls. The nine coefficient values are presented on CIN_{7-0} one by one, in order from A to I. As each value is placed on CIN_{7-0}, it is latched into the selected Coefficient Register using $\overline{CS}$ and $\overline{LD}$. The register to be loaded is determined by the data on A_{2-0} during the load operation. If CREG0 is to be loaded, "010" must be placed on A_{2-0} during the load operation. If CREG1 is to be loaded, "011" must be placed on A_{2-0}. If desired, the Coefficient Register that is not being used to send data to the multiplier array can be loaded with coefficient data while the LF48908 is in active operation.

Address Decoder

The Address Decoder is used to load the Control Logic Registers and to determine which Coefficient Register sends data to the multiplier array. To load a Control Logic Register, the address of the register must be placed on A_{2-0}, the data to be written must be placed on the CIN bus, and $\overline{CS}$ and $\overline{LD}$ must be asserted. The data is latched into the addressed register when $\overline{LD}$ goes HIGH. To select a Coefficient Register (CREG0 or CREG1) to send data to the multiplier array, the appropriate address must be placed on A_{2-0}, and $\overline{CS}$ and $\overline{LD}$ must be asserted. When $\overline{LD}$ goes HIGH, the addressed register will begin supplying coefficient data to the multiplier array. Table 4 lists all of the register addresses.

The Control Logic Registers can be modified during active operation of the LF48908. If this is done, it is very important to meet the t_{LCS} timing specification. This is to ensure that the outputs of the Control Logic Registers have enough time to change before the next rising edge of CLK. If t_{LCS} is not met, unexpected results may occur on $DOUT_{19-0}$ for one clock cycle. There are two situations in which t_{LCS} may

be ignored. If the LF48908 is not in active operation or if the innactive Coefficient Register is being written to during active operation.

Cascade Operation

The Cascade Input lines (CASI15-0) and Cascade Output lines (CASO7-0) are used to allow convolutions of kernel sizes larger than 3 x 3. The Cascade Input lines are also used to allow convolutions on row lengths longer than 1024 pixels. The Cascade Mode Bit (Bit 0) of the Initialization Register determines the function of the Cascade Input lines. If the Cascade Mode Bit is a "0", then the Cascade Input lines are to be used to cascade multiple LF48908s together to perform convolutions of larger kernel sizes. CASI15-0 will be left shifted (by an amount determined by bits 7 and 8 of the Initialization Register) and then added to DOUT19-0. Cascading is accomplished by connecting CASO7-0 and DOUT19-0 of one LF48908 to DIN7-0 and CASI15-0 respectively of another LF48908. If the Cascade Mode Bit is a "1", then the Cascade Input lines are to be used with external row buffers to allow for longer row lengths. In this mode, the Cascade Input lines are split into two 8-bit data busses (CASI15-8 and CASI7-0) which are fed directly into the multiplier array.

TABLE 3. INITIALIZATION REGISTER

BIT		FUNCTION
0		CASCADE MODE
0		Multiplier input from internal row buffers
1		Multiplier input from external buffers
2	1	INPUT DATA DELAY
0	0	No data delay registers used
0	1	One data delay register used
1	0	Two data delay registers used
1	1	Three data delay registers used
3		INPUT DATA FORMAT
0		Unsigned integer format
1		Two's complement format
4		COEFFICIENT DATA FORMAT
0		Unsigned integer format
1		Two's complement format
6	5	OUTPUT ROUNDING
0	0	No rounding
0	1	Round to 16 bits (i.e. DOUT19-4)
1	0	Round to 8 bits (i.e. DOUT19-12)
1	1	Not valid
8	7	CASI15-0 INPUT SHIFT
0	0	No shift
0	1	Shift CASI15-0 left two
1	0	Shift CASI15-0 left four
1	1	Shift CASI15-0 left eight

TABLE 4. CONTROL LOGIC ADDRESS MAP

A2-0	FUNCTION
000	Load Row Buffer Length Register
001	Load ALU Microcode Register
010	Load Coefficient Register 0
011	Load Coefficient Register 1
100	Load Initialization Register
101	Select Coefficient Register 0 for Internal Processing
110	Select Coefficient Register 1 for Internal Processing
111	No Operation

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

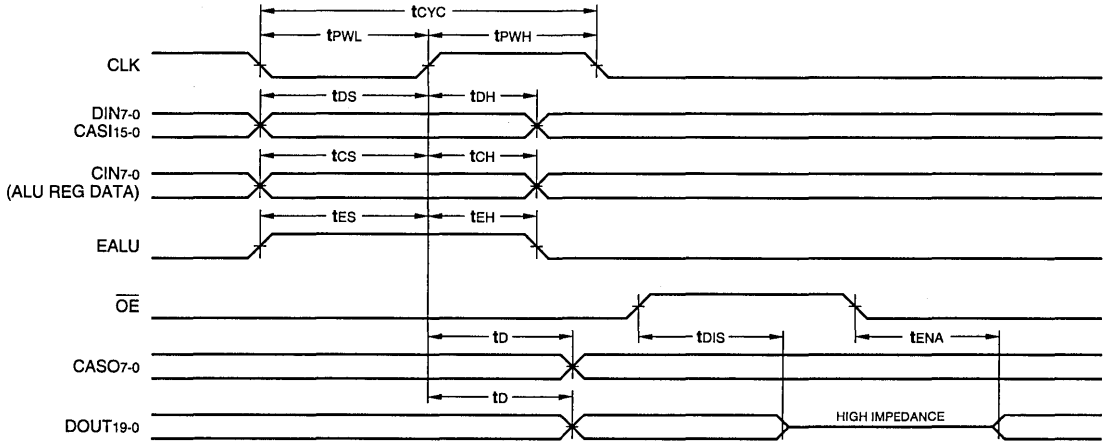
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –400 µA	2.8			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			110	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			500	µA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			12	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF48908–					
		50		31		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		31		25	
t_{PWH}	Clock Pulse Width High	20		12		8	
t_{PWL}	Clock Pulse Width Low	20		13		8	
t_{DS}	Data Input Setup Time	14		13		8	
t_{DH}	Data Input Hold Time	0		0		0	
t_{CS}	CIN_{7-0} Setup Time	16		14		10	
t_{CH}	CIN_{7-0} Hold Time	0		0		0	
t_{ES}	EALU Setup Time	14		12		10	
t_{EH}	EALU Hold Time	0		0		0	
t_D	Output Delay		22		16		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		22		16		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		32		28		8

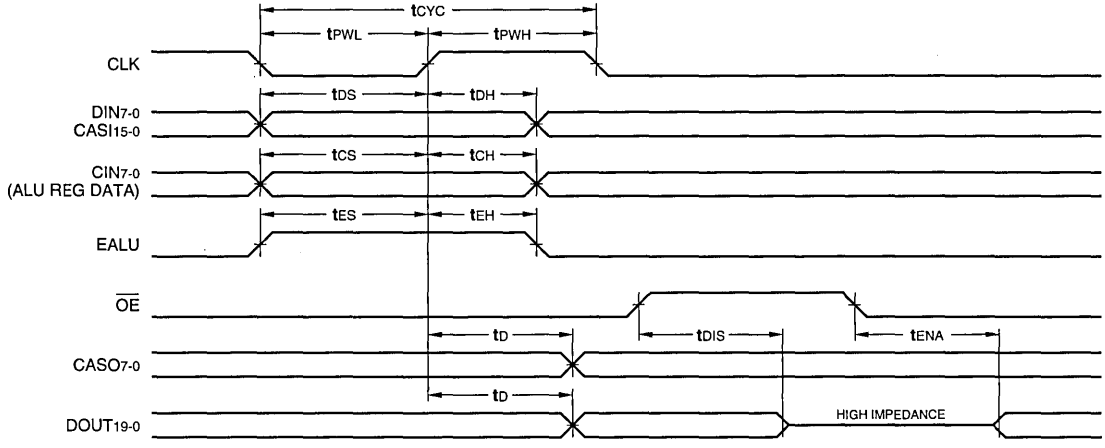
SWITCHING WAVEFORMS: CONVOLVER DATA I/O



MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF48908–					
		50		37		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		37		25	
t_{PWH}	Clock Pulse Width High	20		15		8	
t_{PWL}	Clock Pulse Width Low	20		15		8	
t_{DS}	Data Input Setup Time	17		16		8	
t_{DH}	Data Input Hold Time	0		0		0	
t_{CS}	CIN_{7-0} Setup Time	20		17		10	
t_{CH}	CIN_{7-0} Hold Time	0		0		0	
t_{ES}	EALU Setup Time	17		15		10	
t_{EH}	EALU Hold Time	0		0		0	
t_D	Output Delay		28		19		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		28		19		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		40		35		8

SWITCHING WAVEFORMS: CONVOLVER DATA I/O



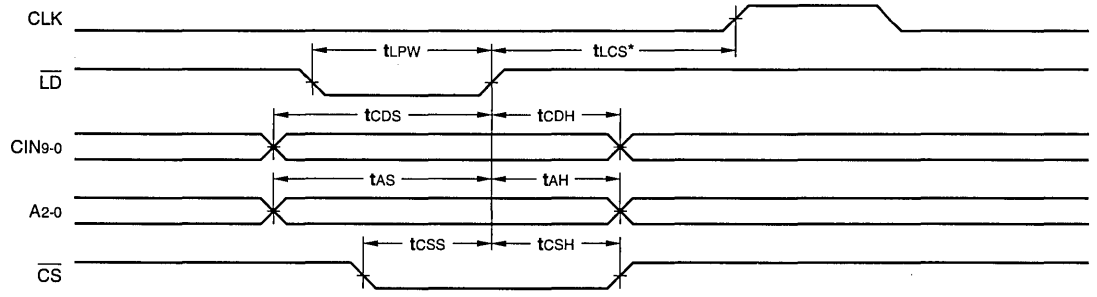
Commercial Operating Range (0°C to +70°C) *Notes 9, 10 (ns)*

		LF48908–					
		50		31		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
tLPW	$\overline{LD}$ Pulse Width	20		12		8	
tLCS	$\overline{LD}$ Setup Time (Applies only during active operation)	30		25		15	
tCDS	Configuration Data Setup Time	16		14		10	
tCDH	Configuration Data Hold Time	0		0		0	
tAS	Address Setup Time	13		13		10	
tAH	Address Hold Time	0		0		0	
tCSS	$\overline{CS}$ Setup Time	0		0		0	
tCSH	$\overline{CS}$ Hold Time	0		0		0	

Military Operating Range (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF48908–					
		50		37		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
tLPW	$\overline{LD}$ Pulse Width	20		15		8	
tLCS	$\overline{LD}$ Setup Time (Applies only during active operation)	37		30		15	
tCDS	Configuration Data Setup Time	20		17		10	
tCDH	Configuration Data Hold Time	0		0		0	
tAS	Address Setup Time	15		15		10	
tAH	Address Hold Time	0		0		0	
tCSS	$\overline{CS}$ Setup Time	0		0		0	
tCSH	$\overline{CS}$ Hold Time	0		0		0	

Switching Waveforms: Configuration Data



*applies only when the LF48908 is in active operation.

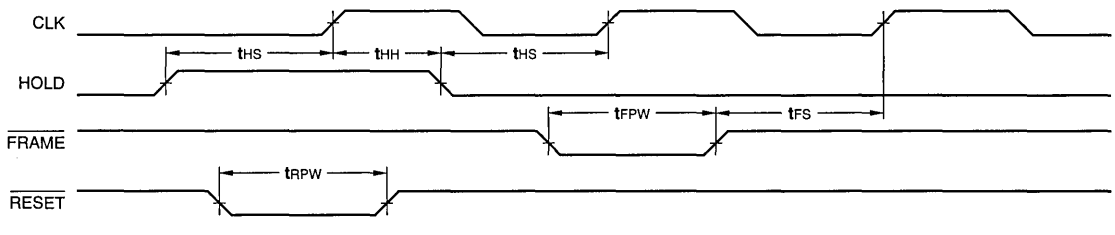
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF48908–					
		50		31		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{HS}	HOLD Setup Time	12		11		9	
t_{HH}	HOLD Hold Time	1		1		0	
t_{FPW}	$\overline{\text{FRAME}}$ Pulse Width	50		31		8	
t_{FS}	$\overline{\text{FRAME}}$ Setup Time	25		21		20	
t_{RPW}	$\overline{\text{RESET}}$ Pulse Width	50		31		8	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF48908–					
		50		37		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{HS}	HOLD Setup Time	14		13		9	
t_{HH}	HOLD Hold Time	2		2		0	
t_{FPW}	$\overline{\text{FRAME}}$ Pulse Width	50		37		8	
t_{FS}	$\overline{\text{FRAME}}$ Setup Time	30		25		20	
t_{RPW}	$\overline{\text{RESET}}$ Pulse Width	50		37		8	

SWITCHING WAVEFORMS: CONTROL SIGNALS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

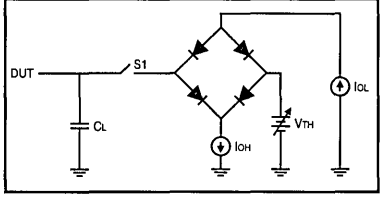
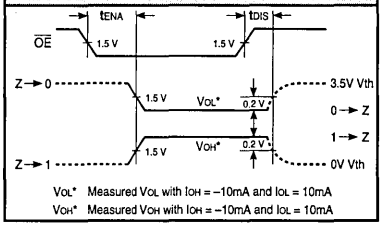


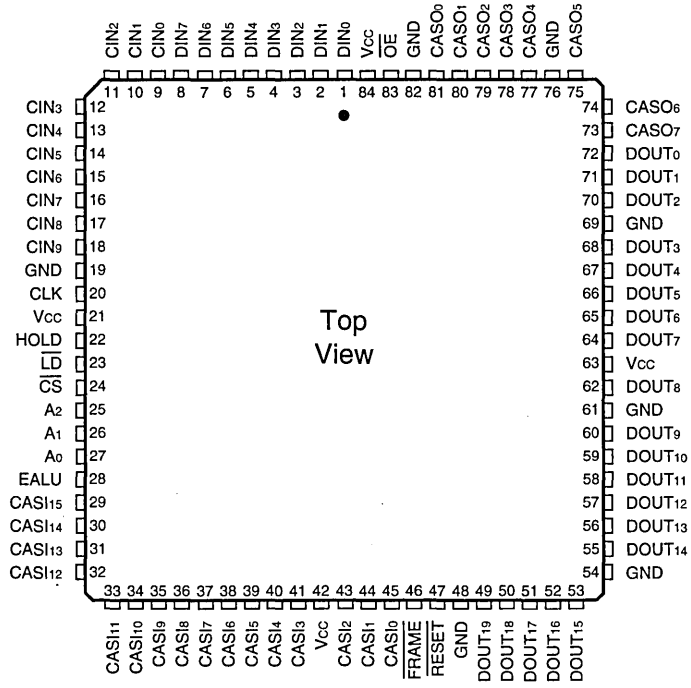
FIGURE B. THRESHOLD LEVELS



2

ORDERING INFORMATION

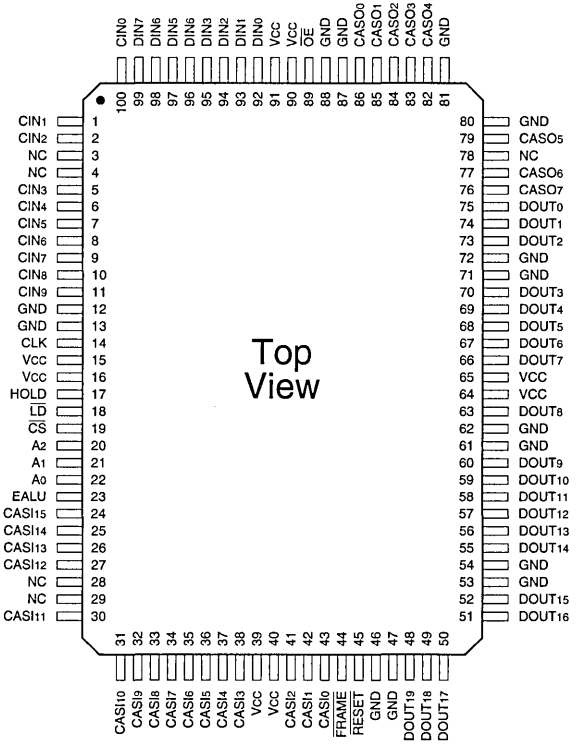
84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF48908JC50
31 ns	LF48908JC31
25 ns	LF48908JC25

ORDERING INFORMATION

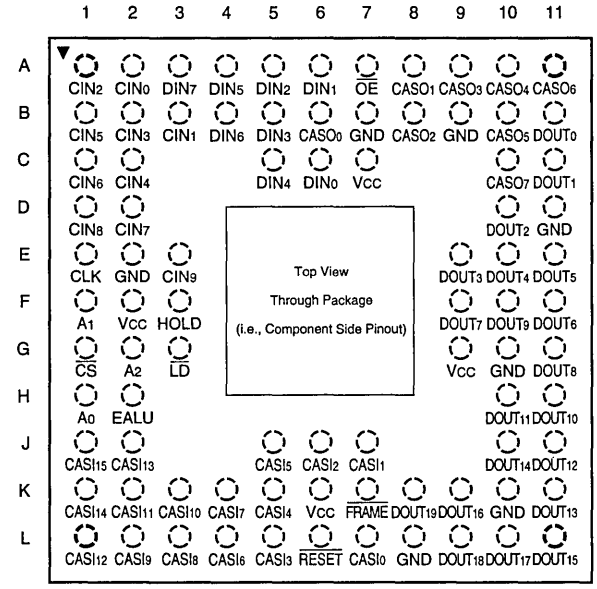
100-pin



Speed	Plastic Quad Flatpack (Q2)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF48908QC50
31 ns	LF48908QC31
25 ns	LF48908QC25

ORDERING INFORMATION

84-pin



Speed	Ceramic Pin Grid Array (G3)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF48908GC50
31 ns	LF48908GC31
25 ns	LF48908GC25
	–55°C to +125°C — COMMERCIAL SCREENING
50 ns	LF48908GM50
37 ns	LF48908GM37
25 ns	LF48908GM25
	–55°C to +125°C — MIL-STD-883 COMPLIANT
50 ns	LF48908GMB50
37 ns	LF48908GMB37
25 ns	LF48908GMB25

FEATURES

- 50 MHz Maximum Operating Frequency
- Programmable Buffer Length from 2 to 1281 Clock Cycles
- 10-bit Data Inputs and Outputs
- Data Delay and Data Recirculation Modes
- Supports Positive or Negative Edge System Clocks
- Expandable Data Word Width or Buffer Length
- Replaces Harris HSP9501
- Package Style Available:
  - 44-pin Plastic LCC, J-Lead

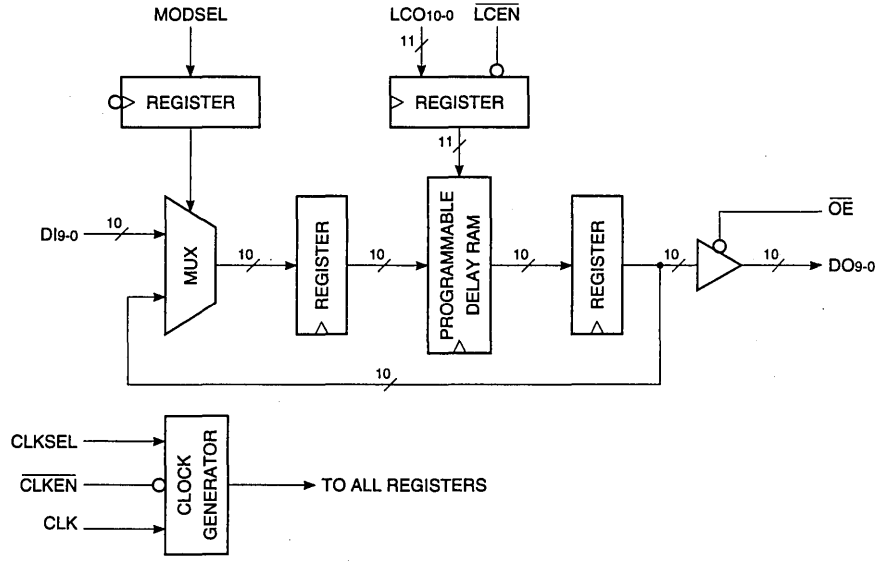
DESCRIPTION

The **LF9501** is a high-speed, 10-bit programmable line buffer. Some applications the LF9501 is useful for include sample rate conversion, data time compression/expansion, software controlled data alignment, and programmable serial data shifting. By using the MODSEL pin, two different modes of operation can be selected: delay mode and data recirculation mode. The delay mode provides a minimum of 2 to a maximum of 1281 clock cycles of delay between the input and output of the device. The data recirculation mode provides a feedback path from the data output to the data input for use as a programmable circular buffer.

By using the length control input ($LC_{10\text{-}0}$) and the length control enable ($\overline{LCEN}$) the length of the delay buffer or amount of recirculation delay can be programmed. Providing a delay value on the $LC_{10\text{-}0}$ inputs and driving $\overline{LCEN}$ LOW will load the delay value into the length control register on the next selected clock edge. Two registers, one preceeding the programmable delay RAM and one following, are included in the delay path. Therefore, the programmed delay value should equal the desired delay minus 2. This consequently means that the value loaded into the length control register must range from 0 to 1279 (to provide an overall range of 2 to 1281).

The active edge of the clock input, either positive or negative edge, can be selected with the clock select (CLKSEL) input. All timing is based on the active clock edge selected by CLKSEL. Data can be held temporarily by using the clock enable ($\overline{CLKEN}$) input.

LF9501 BLOCK DIAGRAM



SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The active edge of CLK, selected by CLKSEL, strobes all registers. All timing specifications are referenced to the active edge of CLK.

Inputs

DI9-0 — Data Input

10-bit data, from the data input, is latched into the device on the active edge of CLK when MODSEL is LOW.

LC10-0 — Length Control Input

The 11-bit value is used to specify the length of the delay buffer, between DI9-0 and DO9-0, or the amount of recirculation delay. An integer value ranging from 0 to 1279 is used to select a delay ranging from 2 to 1281 clock cycles. The value placed on the LC10-0 inputs is equal to the desired delay minus 2. The data presented on LC10-0 is loaded into the device on the active edge of CLK, selected by CLKSEL, in conjunction with $\overline{LCEN}$ being driven LOW.

Outputs

DO9-0 — Data Output

The 10-bit data output appears on DO9-0 on the Nth clock cycle, where N is the overall delay (desired delay).

Controls

$\overline{LCEN}$ — Length Control Enable

When $\overline{LCEN}$ is driven LOW, the next active clock edge will cause the loading of the delay value present at the LC10-0 input.

$\overline{OE}$ — Output Enable

The Output Enable controls the state of DO9-0. Driving $\overline{OE}$ LOW enables the output port. When $\overline{OE}$ is HIGH, DO9-0 is placed in a high-impedance state. The internal transfer of data is not affected by this control.

MODSEL — Mode Select

The Mode Select pin is used to choose the desired mode of operation: data delay mode or data recirculation mode. Driving MODSEL LOW places the device in the delay mode. The device operates as a programmable pipeline register. New data from the DI9-0 input is loaded on every active edge of CLK. Driving MODSEL HIGH places the device in the data recirculation mode. The device operates as a programmable circular buffer. The output of the device is routed back to the input. MODSEL may be changed during device operation (synchronously), however, the required setup and hold times, with respect to CLK, must be met.

CLKSEL — Clock Select

The CLKSEL control allows the selection of the active edge of CLK. A LOW on CLKSEL selects negative-edge triggering of the device. Driving CLKSEL HIGH selects positive-edge triggering. All timing specifications are referenced to the selected active edge of CLK.

$\overline{CLKEN}$ — Clock Enable

The Clock Enable control enables and disables the CLK input. Driving $\overline{CLKEN}$ LOW enables CLK and causes the device to operate in a normal fashion. When $\overline{CLKEN}$ is HIGH, CLK is disabled and the device will hold all internal operations and data. $\overline{CLKEN}$ may be changed during device operation (synchronously), however, the required setup and hold times, with respect to CLK, must be met. The changing of $\overline{CLKEN}$ takes effect on the active edge of CLK following the edge in which it was latched.

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

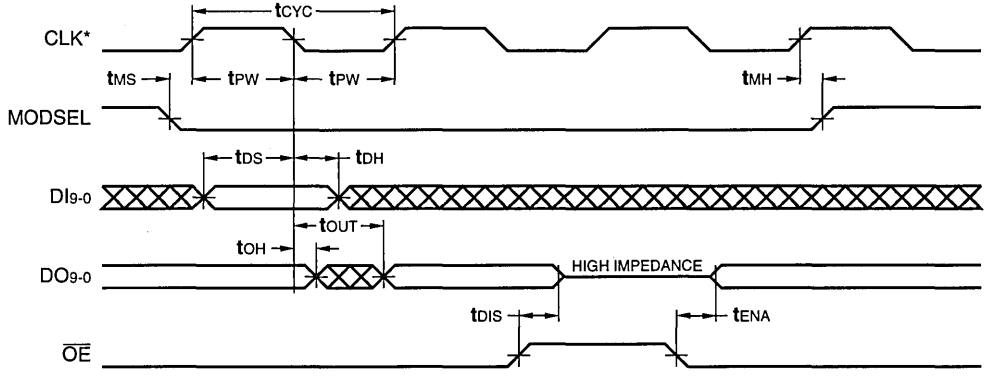
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			125	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			500	µA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF9501–							
		40		31		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	40		31		25		20	
t_{PW}	Clock Pulse Width	15		12		10		8	
t_{DS}	Data Input Setup Time	12		10		8		6	
t_{DH}	Data Input Hold Time	2		2		2		2	
t_{ES}	Clock Enable to Clock Setup Time	12		10		8		6	
t_{EH}	Clock Enable to Clock Hold Time	2		2		2		2	
t_{LS}	Length Control Input Setup Time	13		10		8		6	
t_{LH}	Length Control Input Hold Time	2		2		2		2	
t_{LES}	Length Control Enable to Clock Setup Time	13		10		8		6	
t_{LEH}	Length Control Enable to Clock Hold Time	2		2		2		2	
t_{MS}	Mode Select Setup Time	13		10		8		6	
t_{MH}	Mode Select Hold Time	2		2		2		2	
t_{OUT}	Clock to Data Out		22		16		15		14
t_{OH}	Output Hold Time (Note 8)	4		4		4		4	
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		20		15		14
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		24		15		14

FUNCTIONAL TIMING — $\overline{\text{CLKSEL}}$ LOW



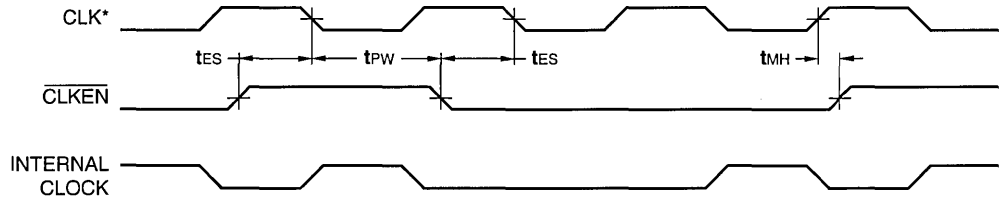
***When $\overline{\text{CLKSEL}}$ is HIGH, assume CLK is inverted.**

SWITCHING CHARACTERISTICS

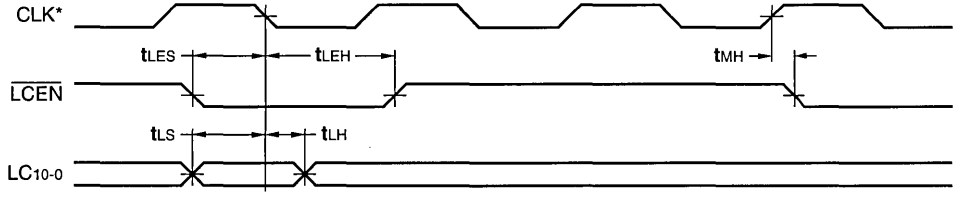
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LF9501– 40 Min	40 Max	31 Min	31 Max	25 Min	25 Max	20 Min	20 Max
t_{CYC}	Cycle Time	40		31		25		20	
t_{PW}	Clock Pulse Width	15		12		10		8	
t_{DS}	Data Input Setup Time	12		10		8		6	
t_{DH}	Data Input Hold Time	2		2		2		2	
t_{ES}	Clock Enable to Clock Setup Time	12		10		8		6	
t_{EH}	Clock Enable to Clock Hold Time	2		2		2		2	
t_{LS}	Length Control Input Setup Time	13		10		8		6	
t_{LH}	Length Control Input Hold Time	2		2		2		2	
t_{LES}	Length Control Enable to Clock Setup Time	13		10		8		6	
t_{LEH}	Length Control Enable to Clock Hold Time	2		2		2		2	
t_{MS}	Mode Select Setup Time	13		10		8		6	
t_{MH}	Mode Select Hold Time	2		2		2		2	
t_{OUT}	Clock to Data Out		22		16		15		14
t_{OH}	Output Hold Time (Note 8)	4		4		4		4	
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		20		15		14
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		24		15		14

CLOCK ENABLE TIMING — $\overline{\text{CLKSEL}}$ LOW



LENGTH CONTROL TIMING — $\overline{\text{CLKSEL}}$ LOW



*When $\overline{\text{CLKSEL}}$ is HIGH, assume CLK is inverted.

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 25 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

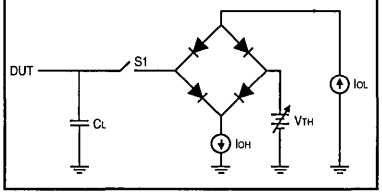
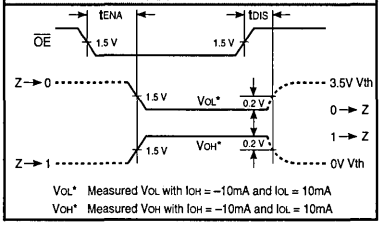
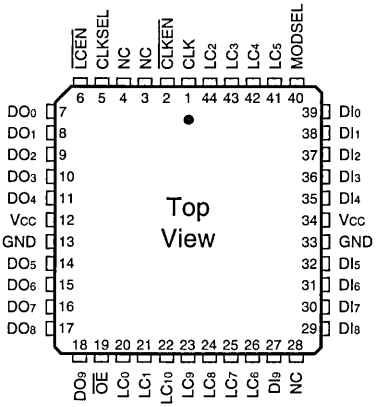


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

44-pin



Speed	Plastic J-Lead Chip Carrier (J1)
	0°C to +70°C — COMMERCIAL SCREENING
40 ns	LF9501JC40
31 ns	LF9501JC31
25 ns	LF9501JC25
20 ns	LF9501JC20

LF9502
2K Programmable Line Buffer

FEATURES

- 50 MHz Maximum Operating Frequency
- Programmable Buffer Length from 2 to 2049 Clock Cycles
- 10-bit Data Inputs and Outputs
- Data Delay and Data Recirculation Modes
- Supports Positive or Negative Edge System Clocks
- Expandable Data Word Width or Buffer Length
- Package Style Available:
  - 44-pin Plastic LCC, J-Lead

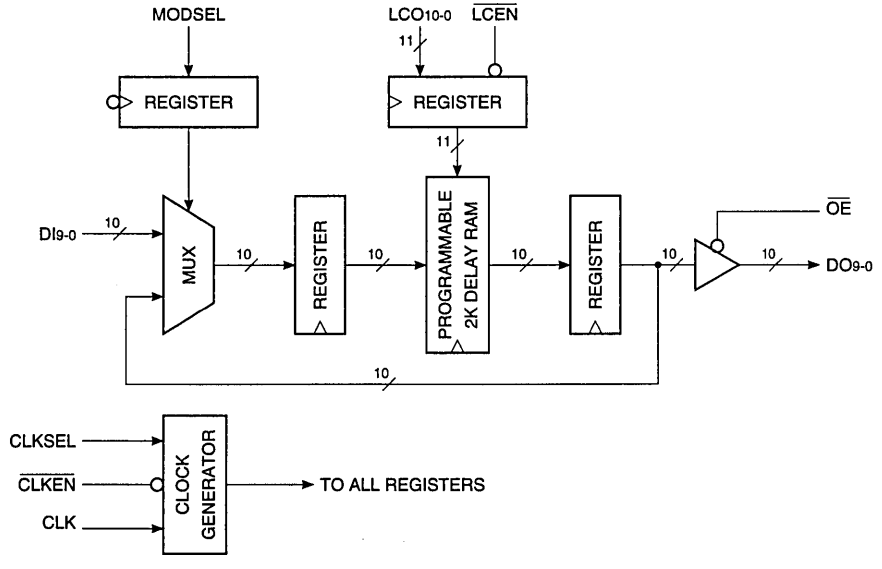
DESCRIPTION

The **LF9502** is a high-speed, 10-bit programmable line buffer. Some applications the LF9502 is useful for include sample rate conversion, data time compression/expansion, software controlled data alignment, and programmable serial data shifting. By using the MODSEL pin, two different modes of operation can be selected: delay mode and data recirculation mode. The delay mode provides a minimum of 2 to a maximum of 2049 clock cycles of delay between the input and output of the device. The data recirculation mode provides a feedback path from the data output to the data input for use as a programmable circular buffer.

By using the length control input (LC_{10-0}) and the length control enable ($\overline{LCEN}$) the length of the delay buffer or amount of recirculation delay can be programmed. Providing a delay value on the LC_{10-0} inputs and driving $\overline{LCEN}$ LOW will load the delay value into the length control register on the next selected clock edge. Two registers, one preceeding the programmable delay RAM and one following, are included in the delay path. Therefore, the programmed delay value should equal the desired delay minus 2. This consequently means that the value loaded into the length control register must range from 0 to 2047 (to provide an overall range of 2 to 2049).

The active edge of the clock input, either positive or negative edge, can be selected with the clock select (CLKSEL) input. All timing is based on the active clock edge selected by CLKSEL. Data can be held temporarily by using the clock enable ($\overline{CLKEN}$) input.

LF9502 Block Diagram



SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The active edge of CLK, selected by CLKSEL, strobes all registers. All timing specifications are referenced to the active edge of CLK.

Inputs

DI9-0 — Data Input

10-bit data, from the data input, is latched into the device on the active edge of CLK when MODSEL is LOW.

LC10-0 — Length Control Input

The 11-bit value is used to specify the length of the delay buffer, between DI9-0 and DO9-0, or the amount of recirculation delay. An integer value ranging from 0 to 2047 is used to select a delay ranging from 2 to 2049 clock cycles. The value placed on the LC10-0 inputs is equal to the desired delay minus 2. The data presented on LC10-0 is loaded into the device on the active edge of CLK, selected by CLKSEL, in conjunction with $\overline{\text{LCEN}}$ being driven LOW.

Outputs

DO9-0 — Data Output

The 10-bit data output appears on DO9-0 on the Nth clock cycle, where N is the overall delay (desired delay).

Controls

$\overline{\text{LCEN}}$ — Length Control Enable

When $\overline{\text{LCEN}}$ is driven LOW, the next active clock edge will cause the loading of the delay value present at the LC10-0 input.

$\overline{\text{OE}}$ — Output Enable

The Output Enable controls the state of DO9-0. Driving $\overline{\text{OE}}$ LOW enables the output port. When $\overline{\text{OE}}$ is HIGH, DO9-0 is placed in a high-impedance state. The internal transfer of data is not affected by this control.

MODSEL — Mode Select

The Mode Select pin is used to choose the desired mode of operation: data delay mode or data recirculation mode. Driving MODSEL LOW places the device in the delay mode. The device operates as a programmable pipeline register. New data from the DI9-0 input is loaded on every active edge of CLK. Driving MODSEL HIGH places the device in the data recirculation mode. The device operates as a programmable circular buffer. The output of the device is routed back to the input. MODSEL may be changed during device operation (synchronously), however, the required setup and hold times, with respect to CLK, must be met.

CLKSEL — Clock Select

The CLKSEL control allows the selection of the active edge of CLK. A LOW on CLKSEL selects negative-edge triggering of the device. Driving CLKSEL HIGH selects positive-edge triggering. All timing specifications are referenced to the selected active edge of CLK.

$\overline{\text{CLKEN}}$ — Clock Enable

The Clock Enable control enables and disables the CLK input. Driving $\overline{\text{CLKEN}}$ LOW enables CLK and causes the device to operate in a normal fashion. When $\overline{\text{CLKEN}}$ is HIGH, CLK is disabled and the device will hold all internal operations and data. $\overline{\text{CLKEN}}$ may be changed during device operation (synchronously), however, the required setup and hold times, with respect to CLK, must be met. The changing of $\overline{\text{CLKEN}}$ takes effect on the active edge of CLK following the edge in which it was latched.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

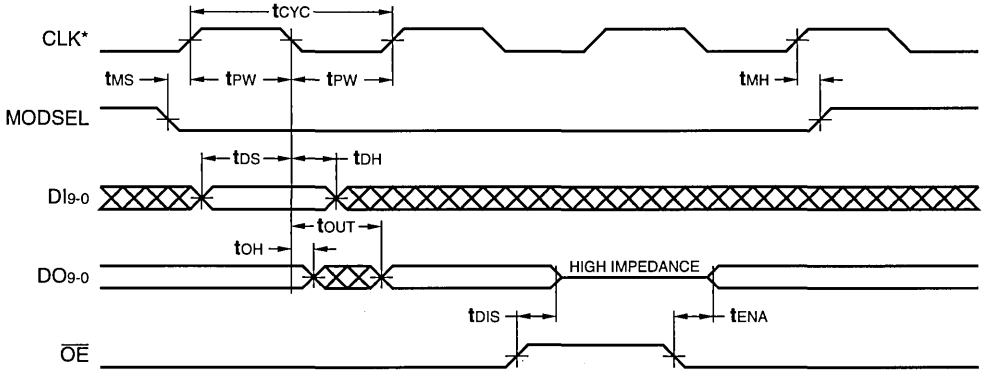
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			125	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			500	µA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF9502–							
		40		31		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	40		31		25		20	
t_{PW}	Clock Pulse Width	15		12		10		8	
t_{DS}	Data Input Setup Time	12		10		8		6	
t_{DH}	Data Input Hold Time	2		2		2		2	
t_{ES}	Clock Enable to Clock Setup Time	12		10		8		6	
t_{EH}	Clock Enable to Clock Hold Time	2		2		2		2	
t_{LS}	Length Control Input Setup Time	13		10		8		6	
t_{LH}	Length Control Input Hold Time	2		2		2		2	
t_{LES}	Length Control Enable to Clock Setup Time	13		10		8		6	
t_{LEH}	Length Control Enable to Clock Hold Time	2		2		2		2	
t_{MS}	Mode Select Setup Time	13		10		8		6	
t_{MH}	Mode Select Hold Time	2		2		2		2	
t_{OUT}	Clock to Data Out		22		16		15		14
t_{OH}	Output Hold Time (Note 8)	4		4		4		4	
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		20		15		14
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		24		15		14

FUNCTIONAL TIMING — $\overline{\text{CLKSEL}}$ LOW



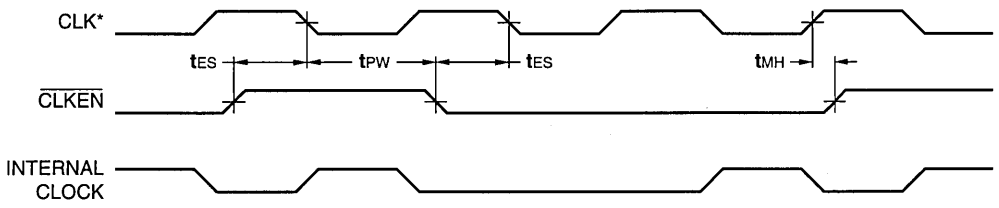
*When $\overline{\text{CLKSEL}}$ is HIGH, assume CLK is inverted.

SWITCHING CHARACTERISTICS

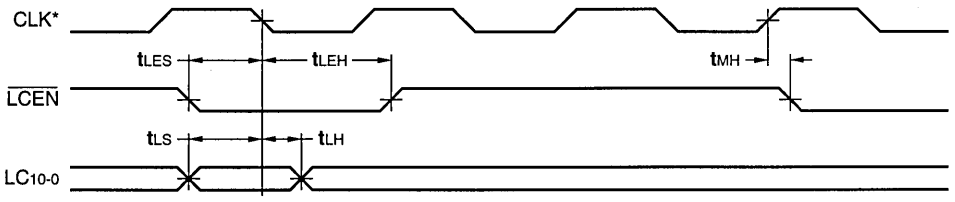
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF9502–							
		40		31		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	40		31		25		20	
t_{PW}	Clock Pulse Width	15		12		10		8	
t_{DS}	Data Input Setup Time	12		10		8		6	
t_{DH}	Data Input Hold Time	2		2		2		2	
t_{ES}	Clock Enable to Clock Setup Time	12		10		8		6	
t_{EH}	Clock Enable to Clock Hold Time	2		2		2		2	
t_{LS}	Length Control Input Setup Time	13		10		8		6	
t_{LH}	Length Control Input Hold Time	2		2		2		2	
t_{LES}	Length Control Enable to Clock Setup Time	13		10		8		6	
t_{LEH}	Length Control Enable to Clock Hold Time	2		2		2		2	
t_{MS}	Mode Select Setup Time	13		10		8		6	
t_{MH}	Mode Select Hold Time	2		2		2		2	
t_{OUT}	Clock to Data Out		22		16		15		14
t_{OH}	Output Hold Time (Note 8)	4		4		4		4	
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		20		15		14
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		24		15		14

CLOCK ENABLE TIMING — $\overline{\text{CLKSEL}}$ LOW



LENGTH CONTROL TIMING — $\overline{\text{CLKSEL}}$ LOW



*When $\overline{\text{CLKSEL}}$ is HIGH, assume CLK is inverted.

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 25 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

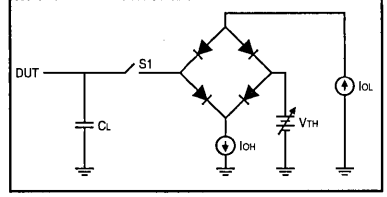
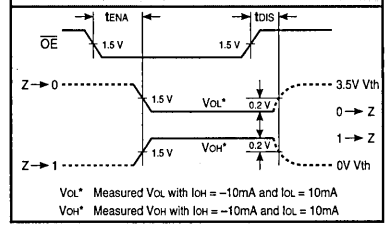
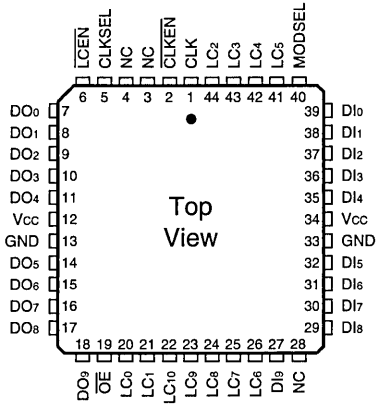


FIGURE B. THRESHOLD LEVELS



44-pin



Speed	Plastic J-Lead Chip Carrier (J1)
	0°C to +70°C — COMMERCIAL SCREENING
40 ns	LF9502JC40
31 ns	LF9502JC31
25 ns	LF9502JC25
20 ns	LF9502JC20

Arithmetic Logic Units & Special Arithmetic Functions

FEATURES

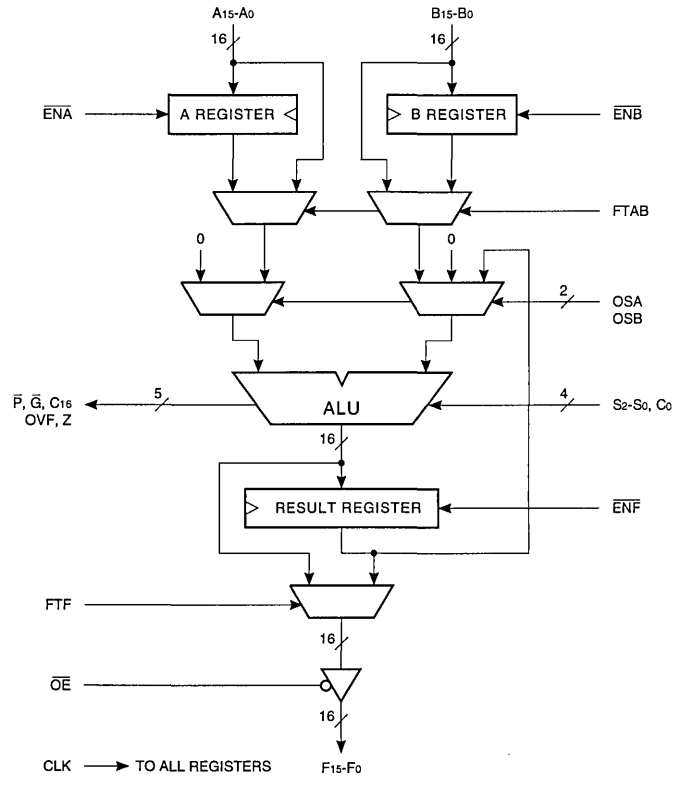
- High-Speed (15ns), Low Power 16-bit Cascadable ALU
- Implements Add, Subtract, Accumulate, Two's Complement, Pass, and Logic Operations
- All Registers Have a Bypass Path for Complete Flexibility
- DECC SMD No. 5962-89959
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC
  - 68-pin Ceramic PGA

DESCRIPTION

The **L4C381** is a flexible, high speed, cascadable 16-bit Arithmetic and Logic Unit. It combines four 381-type 4-bit ALUs, a look-ahead carry generator, and miscellaneous interface logic — all in a single 68-pin package. While containing new features to support high speed pipelined architectures and single 16-bit bus configurations, the L4C381 retains full performance and functional compatibility with the bipolar '381 designs.

The L4C381 can be cascaded to perform 32-bit or greater operations. See "Cascading the L4C381" toward the end of this data sheet for more information.

L4C381 Block Diagram



ARCHITECTURE

The L4C381 operates on two 16-bit operands (A and B) and produces a 16-bit result (F). Three select lines control the ALU and provide 3 arithmetic, 3 logical, and 2 initialization functions. Full ALU status is provided to support cascading to longer word lengths. Registers are provided on both the ALU inputs and the output, but these may be bypassed under user control. An internal feedback path allows the registered ALU output to be routed to one of the ALU inputs, accommodating chain operations and accumulation. Furthermore, the A or B input can be forced to Zero allowing unary functions on either operand.

ALU OPERATIONS

The S_2–S_0 lines specify the operation to be performed. The ALU functions and their select codes are shown in Table 1.

The two functions, B minus A and A minus B, can be achieved by setting the carry input of the least significant slice and selecting codes 001 and 010 respectively.

Table 1. ALU Functions

S_2-S_0	FUNCTION
000	CLEAR (F = 00 ••• 00)
001	NOT(A) + B
010	A + NOT(B)
011	A + B
100	A XOR B
101	A OR B
110	A AND B
111	PRESET (F = 11 ••• 11)

ALU STATUS

The ALU provides Overflow and Zero status bits. Carry, Propagate, and Generate outputs are also provided for cascading. These outputs are defined for the three arithmetic functions only. The ALU sets the Zero output when all 16 output bits are zero. The Generate, Propagate, C_{16}, and OVF flags for the A + B operation are defined in Table 2. The status flags produced for NOT(A) + B and A + NOT(B) can be found by complementing A_i and B_i respectively in Table 2.

TABLE 2. ALU STATUS FLAGS

Bit Carry Generate = $g_i = A_iB_i$ for i = 0 ... 15

Bit Carry Propagate = $p_i = A_i + B_i$ for i = 0 ... 15

$P_0 = p_0$

$P_i = p_i (P_{i-1})$ for i = 1 ... 15

and

$G_0 = g_0$

$G_i = g_i + p_i (G_{i-1})$ for i = 1 ... 15

$C_i = G_{i-1} + P_{i-1} (C_0)$ for i = 1 ... 15

then

$\overline{G} = \text{NOT}(G_{15})$

$\overline{P} = \text{NOT}(P_{15})$

$C_{16} = G_{15} + P_{15}C_0$

$\text{OVF} = C_{15} \text{ XOR } C_{16}$

OPERAND REGISTERS

The L4C381 has two 16-bit wide input registers for operands A and B. These registers are rising edge triggered by a common clock. The A register is enabled for input by setting the $\overline{\text{ENA}}$ control LOW, and the B register is enabled for input by setting the $\overline{\text{ENB}}$ control LOW. When either the $\overline{\text{ENA}}$ control or $\overline{\text{ENB}}$ control is HIGH, the data in the corresponding input register will not change.

This architecture allows the L4C381 to accept arguments from a single 16-bit data bus. For those applications that do not require registered inputs, both the A and B operand registers can be bypassed with the FTAB control line. When the FTAB control is asserted (FTAB = HIGH), data is routed around the A and B input registers; however, they continue to function normally via the $\overline{\text{ENA}}$ and $\overline{\text{ENB}}$ controls. The contents of the input registers will again be available to the ALU if the FTAB control is released.

OUTPUT REGISTER

The output of the ALU drives the input of a 16-bit register. This rising-edge-triggered register is clocked by the same clock as the input registers. When the $\overline{\text{ENF}}$ control is LOW, data from the ALU will be clocked into the output register. By disabling the output register, intermediate results can be held while loading new input operands. Three-state drivers controlled by the $\overline{\text{OE}}$ input allow the L4C381 to be configured in a single bidirectional bus system.

The output register can be bypassed by asserting the FTF control signal (FTF = HIGH). When the FTF control is asserted, output data is routed around the output register, however, it continues to function normally via the $\overline{\text{ENF}}$ control. The contents of the output register will again be available on the output pins if FTF is released. With both FTAB and FTF true (HIGH) the L4C381 is functionally identical to four cascaded 54S381-type devices.

OPERAND SELECTION

The two operand select lines, OSA and OSB, control multiplexers that precede the ALU inputs. These multiplexers provide an operand force-to-zero function as well as F register feedback to the B input. Table 3 shows the inputs to the ALU as a function of the operand select inputs. Either the A or B operands may be forced to zero.

TABLE 3. OPERAND SELECTION

OSB	OSA	OPERAND B	OPERAND A
0	0	F	A
0	1	0	A
1	0	B	0
1	1	B	A

When both operand select lines are low, the L4C381 is configured as a chain calculation ALU. The registered ALU output is passed back to the B input to the ALU. This allows accumulation operations to be performed by providing new operands via the A input port. The accumulator can be preloaded from the A input by setting OSA true. By forcing the function select lines to the CLEAR state (000), the accumulator may be cleared. Note that this feedback operation is not affected by the state of the FTF control. That is, the F outputs of the L4C381 may be driven directly by the ALU. The output register continues to function, however, and provides the ALU B operand source.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

3

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		15	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.5	mA

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

From Input \ To Output	L4C381-55				L4C381-40				L4C381-26			
	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}
FTAB = 0, FTF = 0												
Clock	32	38	53	36	26	30	44	32	22	22	26	22
C_0	—	—	34	22	—	—	28	20	—	—	18	18
S_2-S_0, OSA, OSB	—	42	42	42	—	32	34	35	—	22	22	22
FTAB = 0, FTF = 1												
Clock	56	38	53	36	46	30	44	32	28	22	26	22
C_0	37	—	34	22	30	—	28	20	22	—	18	18
S_2-S_0, OSA, OSB	55	42	42	42	40	32	34	35	26	22	22	22
FTAB = 1, FTF = 0												
A_{15}-A_0, B_{15}-B_0	—	36	46	37	—	30	40	32	—	22	22	22
Clock	32	—	—	—	26	—	—	—	22	—	—	—
C_0	—	—	34	22	—	—	28	20	—	—	18	18
S_2-S_0, OSA, OSB	—	42	42	42	—	32	34	35	—	22	22	22
FTAB = 1, FTF = 1												
A_{15}-A_0, B_{15}-B_0	55	36	46	37	40	30	40	32	26	22	22	22
Clock (OSA, OSB = 0)	56	38	53	36	46	30	44	32	28	22	26	22
C_0	37	—	34	22	30	—	28	20	22	—	18	18
S_2-S_0, OSA, OSB	55	42	42	42	40	32	34	35	26	22	22	22

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

Input	L4C381-55				L4C381-40				L4C381-26			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_{15}-A_0, B_{15}-B_0	8	2	35	2	8	2	28	2	8	2	16	2
C_0	21	0	21	0	16	0	16	0	8	0	8	0
S_2-S_0, OSA, OSB	44	0	44	0	32	0	32	0	18	0	18	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	10	2	10	2	10	2	10	2	8	2	8	2

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	L4C381-55	L4C381-40	L4C381-26
t_{ENA}	20	18	16
t_{DIS}	20	18	16

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	L4C381-55	L4C381-40	L4C381-26
Minimum Cycle Time	43	34	20
Highgoing Pulse	15	10	10
Lowgoing Pulse	15	10	10

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

To Output / From Input	L4C381-20				L4C381-15			
	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}
FTAB = 0, FTF = 0								
Clock	11	20	20	20	11	15	15	15
C_0	—	—	14	14	—	—	13	13
S_2-S_0, OSA, OSB	—	18	20	18	—	14	15	14
FTAB = 0, FTF = 1								
Clock	20	20	20	20	15	15	15	15
C_0	18	—	14	14	14	—	13	13
S_2-S_0, OSA, OSB	20	18	20	18	15	14	15	14
FTAB = 1, FTF = 0								
A_{15}-A_0, B_{15}-B_0	—	16	20	17	—	14	15	14
Clock	11	—	—	—	11	—	—	—
C_0	—	—	14	14	—	—	13	13
S_2-S_0, OSA, OSB	—	18	20	18	—	14	15	14
FTAB = 1, FTF = 1								
A_{15}-A_0, B_{15}-B_0	20	16	20	17	15	14	15	14
Clock (OSA, OSB = 0)	20	20	20	20	15	15	15	15
C_0	18	—	14	14	14	—	13	13
S_2-S_0, OSA, OSB	20	18	20	18	15	14	15	14

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

	L4C381-20				L4C381-15			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
Input	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_{15}-A_0, B_{15}-B_0	5	0	14	0	5	0	12	0
C_0	12	0	12	0	10	0	10	0
S_2-S_0, OSA, OSB	15	0	15	0	12	0	12	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	5	0	5	0	5	0	5	0

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	L4C381-20	L4C381-15	
t_{ENA}	8	6	
t_{DIS}	8	6	

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	L4C381-20	L4C381-15	
Minimum Cycle Time	18	14	
Highgoing Pulse	5	4	
Lowgoing Pulse	5	4	

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +125°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

To Output / From Input	L4C381-65				L4C381-45				L4C381-30			
	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}
FTAB = 0, FTF = 0												
Clock	37	44	63	45	28	34	50	34	26	28	34	28
C_0	—	—	42	25	—	—	32	23	—	—	22	22
S_2-S_0, OSA, OSB	—	48	48	48	—	38	38	38	—	28	28	28
FTAB = 0, FTF = 1												
Clock	68	44	63	45	56	34	50	34	34	28	34	28
C_0	42	—	42	25	32	—	32	23	26	—	22	22
S_2-S_0, OSA, OSB	66	48	48	48	46	38	38	38	30	28	28	28
FTAB = 1, FTF = 0												
A_{15}-A_0, B_{15}-B_0	—	44	56	44	—	32	46	36	—	28	28	28
Clock	37	—	—	—	28	—	—	—	26	—	—	—
C_0	—	—	42	25	—	—	32	23	—	—	22	22
S_2-S_0, OSA, OSB	—	48	48	48	—	38	38	38	—	28	28	28
FTAB = 1, FTF = 1												
A_{15}-A_0, B_{15}-B_0	65	44	56	44	45	32	46	36	30	28	28	28
Clock (OSA, OSB = 0)	68	44	63	45	56	34	50	34	34	28	34	28
C_0	42	—	42	25	32	—	32	23	26	—	22	22
S_2-S_0, OSA, OSB	66	48	48	48	46	38	38	38	30	28	28	28

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

Input	L4C381-65				L4C381-45				L4C381-30			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_{15}-A_0, B_{15}-B_0	10	3	43	3	8	3	33	3	8	3	20	3
C_0	25	0	25	0	20	0	20	0	12	0	12	0
S_2-S_0, OSA, OSB	50	0	50	0	36	0	36	0	20	0	20	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	12	2	12	2	10	2	10	2	10	2	10	2

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	L4C381-65	L4C381-45	L4C381-30
t_{ENA}	22	20	18
t_{DIS}	22	20	18

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	L4C381-65	L4C381-45	L4C381-30
Minimum Cycle Time	52	38	26
Highgoing Pulse	20	15	12
Lowgoing Pulse	20	15	12

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +125°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

From Input \ To Output	L4C381-25				L4C381-20			
	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}
FTAB = 0, FTF = 0								
Clock	14	24	24	24	14	20	20	20
C_0	—	—	18	18	—	—	16	16
S_2-S_0, OSA, OSB	—	22	24	22	—	18	20	18
FTAB = 0, FTF = 1								
Clock	25	24	24	24	20	20	20	20
C_0	21	—	18	18	17	—	16	16
S_2-S_0, OSA, OSB	25	22	24	22	20	18	20	18
FTAB = 1, FTF = 0								
A_{15}-A_0, B_{15}-B_0	—	20	25	22	—	17	20	17
Clock	14	—	—	—	14	—	—	—
C_0	—	—	18	18	—	—	16	16
S_2-S_0, OSA, OSB	—	22	24	22	—	18	20	18
FTAB = 1, FTF = 1								
A_{15}-A_0, B_{15}-B_0	25	20	25	22	20	17	20	17
Clock (OSA, OSB = 0)	25	24	24	24	20	20	20	20
C_0	21	—	18	18	17	—	16	16
S_2-S_0, OSA, OSB	25	22	24	22	20	18	20	18

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

Input	L4C381-25				L4C381-20			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_{15}-A_0, B_{15}-B_0	7	2	14	2	6	2	12	2
C_0	14	0	14	0	12	0	12	0
S_2-S_0, OSA, OSB	19	0	19	0	16	0	16	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	7	0	7	0	6	0	6	0

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	L4C381-25	L4C381-20	
t_{ENA}	14	10	
t_{DIS}	14	10	

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	L4C381-25	L4C381-20	
Minimum Cycle Time	20	18	
Highgoing Pulse	8	6	
Lowgoing Pulse	8	6	

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

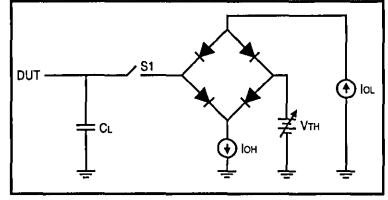
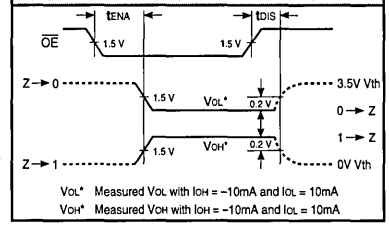


FIGURE B. THRESHOLD LEVELS



CASCADING THE L4C381

Cascading the L4C381 to 32 bits is accomplished simply by connecting the C_{16} output of the least significant slice to the C_0 input of the most significant slice. The S_2-S_0, OSA, OSB, $\overline{ENA}$, $\overline{ENB}$, and $\overline{ENF}$ lines are common to both devices. The Zero output flags should be logically ANDed to produce the Zero flag for the 32-bit result. The OVF and C_{16} outputs of the most significant slice are valid for the 32-bit result.

Propagation delay calculations for this configuration require two steps: First determine the propagation delay from the input of interest to the C_{16} output of the lower slice. Add this number to the delay from the C_0 input of the upper slice to the output of interest (of the C_0 setup time, if the F register is used). The sum gives the overall input-to-output delay (or setup time) for the 32-bit configuration. This method gives a conservative result, since the C_{16} output is very lightly loaded. Formulas for calculation of all critical delays for a 32-bit system are shown in Figures 4A through 4D.

Cascading to greater than 32 bits can be accomplished in two ways: The simplest (but slowest) method is to simply connect the C_{16} output of each slice to the C_0 input of the next more significant slice. Propagation delays are calculated as for the 32-bit case, except that the C_0 to C_{16} delays for all intermediate slices must be added to the overall delay for each path. A faster method is to use an external carry-lookahead generator. The $\overline{P}$ and $\overline{G}$ outputs of each slice are connected as inputs to the CLA generator, which in turn produces the C_0 inputs for each slice except the least significant. The C_{16} outputs are not used in this case, except for the most significant one, which is the carry out of the overall system. The carry in to the system is connected to the C_0 input of the least significant slice, and also to the carry lookahead generator. Propagation delays for this configuration are the sum of the time to $\overline{P}$, $\overline{G}$, for the least significant slice, the propagation delay of the carry lookahead generator, and the C_0 to output time of the most significant slice.

FIGURE 4A. FTAB = 0, FTF = 0

From	To		Calculated Specification Limit
Clock	→ F	=	Same as 16-bit case
Clock	→ Other	=	(Clock → C_{16}) + (C_0 → Out)
C_0	→ Other	=	(C_0 → C_{16}) + (C_0 → Out)
S_2-S_0, OSA, OSB	→ Other	=	(S_2-S_0, OSA, OSB → C_{16}) + (C_0 → Out)
A, B	Setup time	=	Same as 16-bit case
C_0	Setup time	=	(C_0 → C_{16}) + (C_0 Setup time)
$\overline{S_2}$-$\overline{S_0}$, $\overline{OSA}$, $\overline{OSB}$	Setup time	=	(S_2-S_0, OSA, OSB → C_{16}) + (C_0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time		=	(Clock → C_{16}) + (C_0 Setup time)

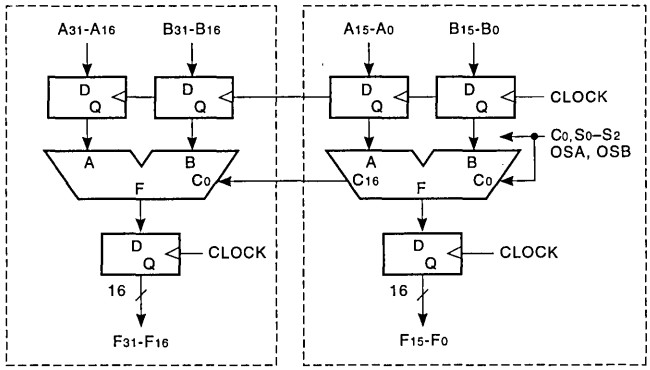


FIGURE 4B. FTAB = 0, FTF = 1

From	To		Calculated Specification Limit
Clock	→ F	=	(Clock → C_{16}) + (C_0 → F)
Clock	→ Other	=	(Clock → C_{16}) + (C_0 → Out)
C_0	→ F	=	(C_0 → C_{16}) + (C_0 → F)
C_0	→ Other	=	(C_0 → C_{16}) + (C_0 → Out)
S_2-S_0, OSA, OSB	→ F	=	(S_2-S_0, OSA, OSB → C_{16}) + (C_0 → F)
S_2-S_0, OSA, OSB	→ Other	=	(S_2-S_0, OSA, OSB → C_{16}) + (C_0 → Out)
A, B	Setup time	=	Same as 16-bit case
C_0	Setup time	=	(C_0 → C_{16}) + (C_0 Setup time)
$\overline{S_2}$-$\overline{S_0}$, $\overline{OSA}$, $\overline{OSB}$	Setup time	=	(S_2-S_0, OSA, OSB → C_{16}) + (C_0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time		=	(Clock → C_{16}) + (C_0 Setup time)

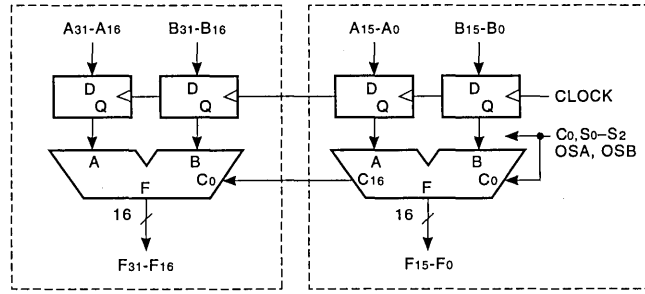


FIGURE 4C. FTAB = 1, FTF = 0

From	To		Calculated Specification Limit
Clock	→ F	=	Same as 16-bit case
A, B	→ Other	=	(A, B → C16) + (C0 → Out)
C0	→ Other	=	(C0 → C16) + (C0 → Out)
S2-S0, OSA, OSB	→ Other	=	(S2-S0, OSA, OSB → C16) + (C0 → Out)
A, B	Setup time	=	(A, B → C16) + (C0 Setup time)
C0	Setup time	=	(C0 → C16) + (C0 Setup time)
S2-S0, OSA, OSB	Setup time	=	(S2-S0, OSA, OSB → C16) + (C0 Setup time)
ENA, ENB, ENF	Setup time	=	Same as 16-bit case
Minimum cycle time (F register accumulate loop)		=	(Clock → C16) + (C0 Setup time)

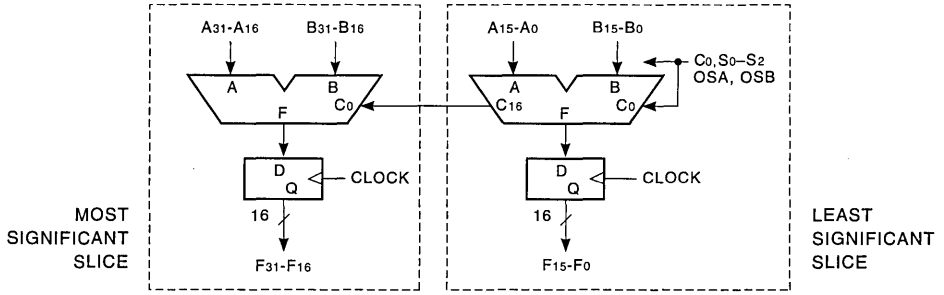
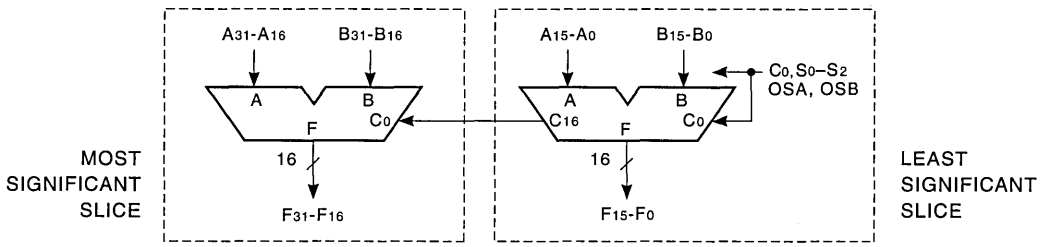


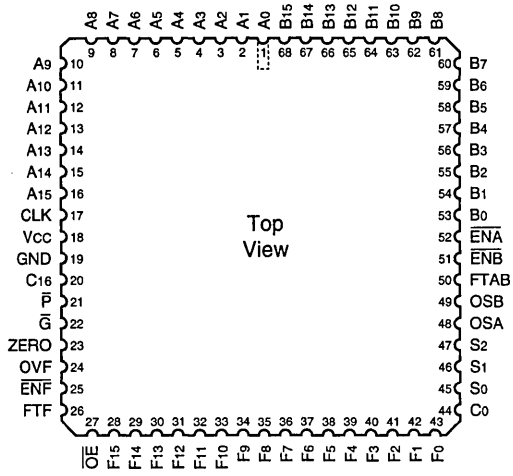
FIGURE 4D. FTAB = 1, FTF = 1

From	To		Calculated Specification Limit
A, B	→ F	=	(A, B → C16) + (C0 → F)
A, B	→ Other	=	(A, B → C16) + (C0 → Out)
C0	→ F	=	(C0 → C16) + (C0 → F)
C0	→ Other	=	(C0 → C16) + (C0 → Out)
S2-S0, OSA, OSB	→ F	=	(S2-S0, OSA, OSB → C16) + (C0 → F)
S2-S0, OSA, OSB	→ Other	=	(S2-S0, OSA, OSB → C16) + (C0 → Out)
A, B	Setup time	=	(A, B → C16) + (C0 Setup time)
C0	Setup time	=	(C0 → C16) + (C0 Setup time)
S2-S0, OSA, OSB	Setup time	=	(S2-S0, OSA, OSB → C16) + (C0 Setup time)
ENA, ENB, ENF	Setup time	=	Same as 16-bit case
Minimum cycle time (F register accumulate loop)		=	(Clock → C16) + (C0 Setup time)

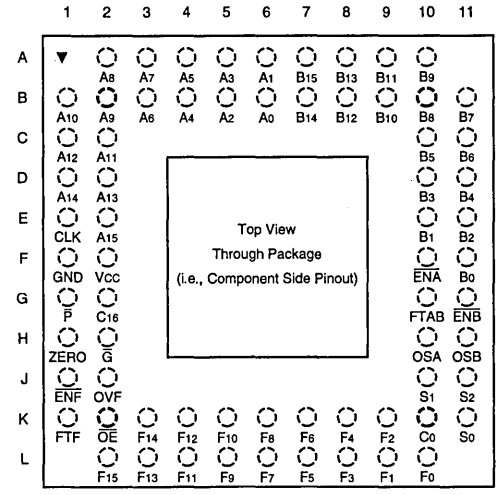


ORDERING INFORMATION

68-pin



68-pin



Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)	Ceramic Pin Grid Array (G1)
	0°C to +70°C — Commercial Screening		
55 ns	L4C381JC55	L4C381KC55	L4C381GC55
40 ns	L4C381JC40	L4C381KC40	L4C381GC40
26 ns	L4C381JC26	L4C381KC26	L4C381GC26
20 ns	L4C381JC20	L4C381KC20	L4C381GC20
15 ns	L4C381JC15	L4C381KC15	L4C381GC15
	–55°C to +125°C — Commercial Screening		
65 ns		L4C381KM65	L4C381GM65
45 ns		L4C381KM45	L4C381GM45
30 ns		L4C381KM30	L4C381GM30
25 ns		L4C381KM25	L4C381GM25
20 ns		L4C381KM20	L4C381GM20
	–55°C to +125°C — MIL-STD-883 Compliant		
65 ns		L4C381KMB65	L4C381GMB65
45 ns		L4C381KMB45	L4C381GMB45
30 ns		L4C381KMB30	L4C381GMB30
25 ns		L4C381KMB25	L4C381GMB25
20 ns		L4C381KMB20	L4C381GMB20

L4C383
16-bit Cascadable ALU (Extended Set)

FEATURES

- High-Speed (15ns), Low Power 16-bit Cascadable ALU
- Extended Function Set (32 Advanced ALU Functions)
- All Registers Have a Bypass Path for Complete Flexibility
- Replaces IDT7383
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC
  - 68-pin Ceramic PGA

DESCRIPTION

The **L4C383** is a flexible, high speed, cascadable 16-bit Arithmetic and Logic Unit. The L4C383 is capable of performing up to 32 different arithmetic or logic functions.

The L4C383 can be cascaded to perform 32-bit or greater operations. See "Cascading the L4C383" on the next page.

ARCHITECTURE

The L4C383 operates on two 16-bit operands (A and B) and produces a 16-bit result (F). Five select lines control the ALU and provide 19 arithmetic and 13 logical functions. Registers are provided on both the ALU inputs and the output, but these may be bypassed under user control. An internal feedback path allows the registered ALU output to be routed to one or both of the ALU inputs, accommodating chain operations and accumulation.

ALU OPERATIONS

The S_4–S_0 lines specify the operation to be performed. The ALU functions and their select codes are shown in Table 1.

ALU STATUS

The ALU provides Overflow and Zero status bits. A Carry output is also provided for cascading multiple devices, however it is only defined for the 19 arithmetic functions. The ALU sets the Zero output when all 16 output bits are zero. The N, C_{16} and OVF flags for the arithmetic operations are defined in Table 2.

OPERAND REGISTERS

The L4C383 has two 16-bit wide input registers for operands A and B. These registers are rising edge triggered by a common clock. The A register is enabled for input by setting the $\overline{ENA}$ control LOW, and the B register is enabled for input by setting the $\overline{ENB}$ control LOW. When either the $\overline{ENA}$ control or $\overline{ENB}$ control is HIGH, the data in the corresponding input register will not change.

This architecture allows the L4C383 to accept arguments from a single 16-bit data bus. For those applications that do not require registered inputs, both the A and B operand registers can be bypassed with the FTAB control line.

L4C383 BLOCK DIAGRAM

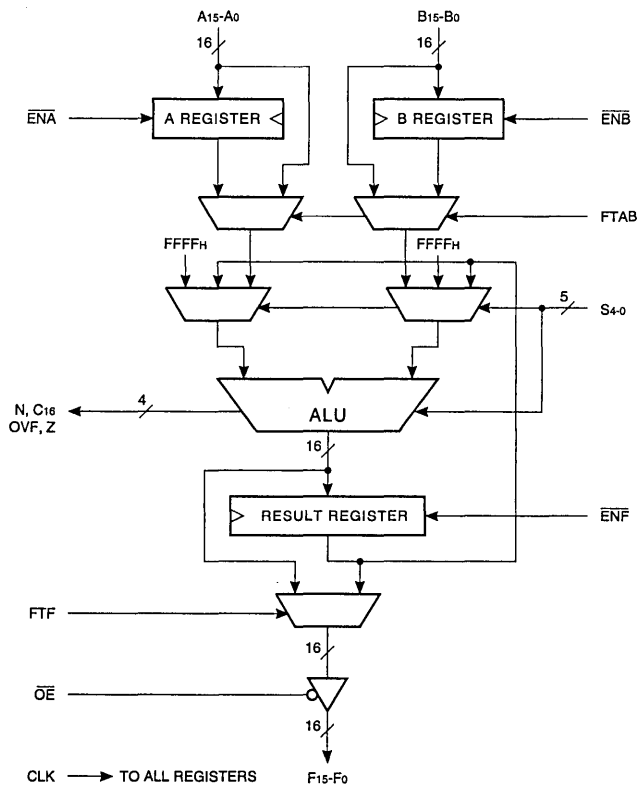


TABLE 1. ALU FUNCTIONS

S4-S0	FUNCTION
00000	A + B + C0
00001	A OR B
00010	A + $\overline{B}$ + C0
00011	$\overline{A}$ + B + C0
00100	A + C0
00101	$\overline{A}$ OR F
00110	A – 1 + C0
00111	$\overline{A}$ + C0
01000	A + F + C0
01001	A OR F
01010	A + $\overline{F}$ + C0
01011	$\overline{A}$ + F + C0
01100	F + B + C0
01101	$\overline{A}$ OR B
01110	F + $\overline{B}$ + C0
01111	$\overline{F}$ + B + C0
10000	A XOR B
10001	A AND B
10010	$\overline{A}$ AND B
10011	A XNOR B
10100	A XOR F
10101	A AND F
10110	$\overline{A}$ AND F
10111	ALL 1's + C0
11000	B + C0
11001	A AND $\overline{B}$
11010	$\overline{B}$ + C0
11011	B – 1 + C0
11100	F + C0
11101	A OR $\overline{B}$
11110	F – 1 + C0
11111	$\overline{F}$ + C0

When the FTAB control is asserted (FTAB = HIGH), data is routed around the A and B input registers; however, they continue to function normally via the ENA and ENB controls. The contents of the input registers will again be available to the ALU if the FTAB control is released.

TABLE 2. ALU STATUS FLAGS

Bit Carry Generate = $g_i = A_iB_i$ for i = 0 ... 15
Bit Carry Propagate = $p_i = A_i + B_i$ for i = 0 ... 15

$P_0 = p_0$
$P_i = p_i (P_{i-1})$ for i = 1 ... 15

and

$G_0 = g_0$
$G_i = g_i + p_i (G_{i-1})$ for i = 1 ... 15
$C_i = G_{i-1} + P_{i-1} (C_0)$ for i = 1 ... 15

then

$C_{16} = G_{15} + P_{15}C_0$
OVF = C_{15} XOR C_{16}
Zero = All Output Bits Equal Zero
N = Sign Bit of ALU Operation

OUTPUT REGISTER

The output of the ALU drives the input of a 16-bit register. This rising-edge-triggered register is clocked by the same clock as the input registers. When the $\overline{ENF}$ control is LOW, data from the ALU will be clocked into the output register. By disabling the output register, intermediate results can be held while loading new input operands. Three-state drivers controlled by the $\overline{OE}$ input allow the L4C383 to be configured in a single bidirectional bus system.

The output register can be bypassed by asserting the FTF control signal (FTF = HIGH). When the FTF control is asserted, output data is routed around the output register, however, it continues to function normally via the $\overline{ENF}$ control. The contents of the output register will again be available on the output pins if FTF is released.

CASCADING THE L4C383

Cascading the L4C383 to 32 bits is accomplished simply by connecting the C_{16} output of the least significant slice to the C_0 input of the most sig-nificant slice. The S4-S0, $\overline{ENA}$, $\overline{ENB}$, and $\overline{ENF}$ lines are common to both devices. The Zero output flags should be logically ANDed to produce the Zero flag for the 32-bit result. The OVF and C_{16} outputs of the most significant slice are valid for the 32-bit result.

Propagation delay calculations for this configuration require two steps: First determine the propagation delay from the input of interest to the C_{16} output of the lower slice. Add this number to the delay from the C_0 input of the upper slice to the output of interest (of the C_0 setup time, if the F register is used). The sum gives the overall input-to-output delay (or setup time) for the 32-bit configuration. This method gives a conservative result, since the C_{16} output is very lightly loaded. Formulas for calculation of all critical delays for a 32-bit system are shown in Figures 4A through 4D.

Cascading to greater than 32 bits can be accomplished by simply connecting the C_{16} output of each slice to the C_0 input of the next more significant slice. Propagation delays are calculated as for the 32-bit case, except that the C_0 to C_{16} delays for all intermediate slices must be added to the overall delay for each path.

FIGURE 4A. FTAB = 0, FTF = 0

From	To		Calculated Specification Limit
Clock	→ F	=	Same as 16-bit case
Clock	→ Other	=	(Clock → C_{16}) + (C_0 → Out)
C_0	→ Other	=	(C_0 → C_{16}) + (C_0 → Out)
S_4-S_0	→ Other	=	(S_4-S_0 → C_{16}) + (C_0 → Out)
A, B	Setup time	=	Same as 16-bit case
C_0	Setup time	=	(C_0 → C_{16}) + (C_0 Setup time)
$\overline{S_4\text{-}S_0}$	Setup time	=	(S_4-S_0 → C_{16}) + (C_0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time		=	(Clock → C_{16}) + (C_0 Setup time)

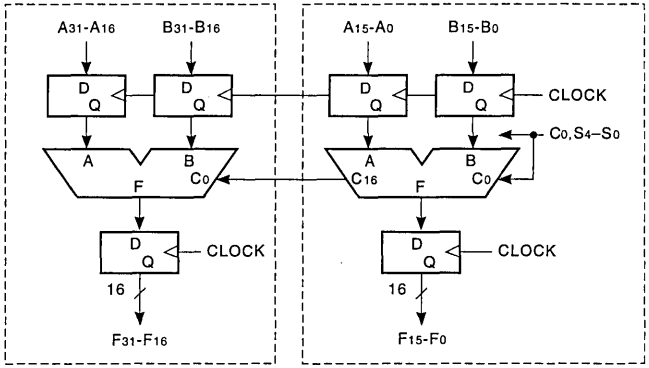


FIGURE 4B. FTAB = 0, FTF = 1

From	To		Calculated Specification Limit
Clock	→ F	=	(Clock → C_{16}) + (C_0 → F)
Clock	→ Other	=	(Clock → C_{16}) + (C_0 → Out)
C_0	→ F	=	(C_0 → C_{16}) + (C_0 → F)
C_0	→ Other	=	(C_0 → C_{16}) + (C_0 → Out)
S_4-S_0	→ F	=	(S_4-S_0 → C_{16}) + (C_0 → F)
S_4-S_0	→ Other	=	(S_4-S_0 → C_{16}) + (C_0 → Out)
A, B	Setup time	=	Same as 16-bit case
C_0	Setup time	=	(C_0 → C_{16}) + (C_0 Setup time)
$\overline{S_4\text{-}S_0}$	Setup time	=	(S_4-S_0 → C_{16}) + (C_0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time		=	(Clock → C_{16}) + (C_0 Setup time)

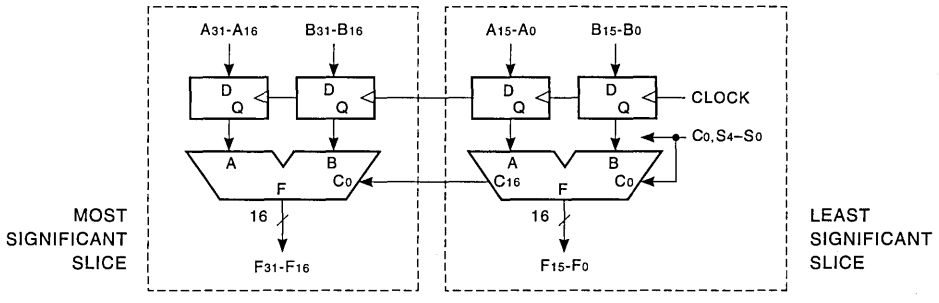


FIGURE 4C. FTAB = 1, FTF = 0

From	To		Calculated Specification Limit
Clock	→ F	=	Same as 16-bit case
A, B	→ Other	=	(A, B → C_{16}) + (C_0 → Out)
C_0	→ Other	=	(C_0 → C_{16}) + (C_0 → Out)
S_4-S_0	→ Other	=	(S_4-S_0 → C_{16}) + (C_0 → Out)
A, B	Setup time	=	(A, B → C_{16}) + (C_0 Setup time)
C_0	Setup time	=	(C_0 → C_{16}) + (C_0 Setup time)
S_4-S_0	Setup time	=	(S_4-S_0 → C_{16}) + (C_0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time (F register accumulate loop)		=	(Clock → C_{16}) + (C_0 Setup time)

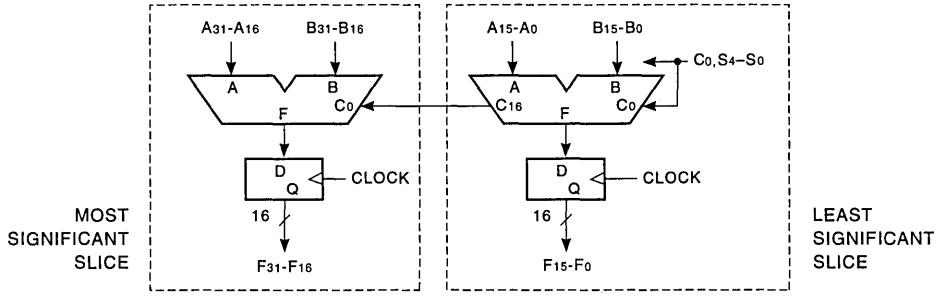
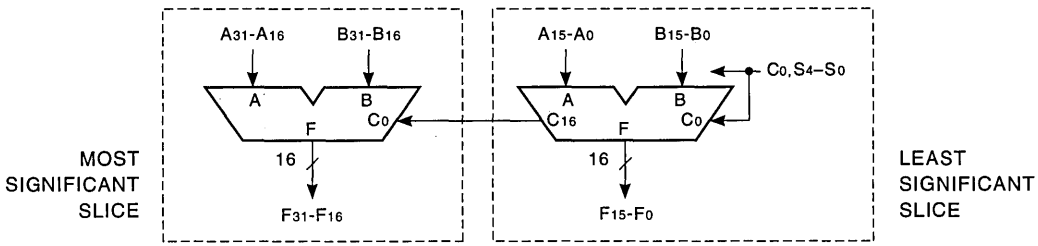


FIGURE 4D. FTAB = 1, FTF = 1

From	To		Calculated Specification Limit
A, B	→ F	=	(A, B → C_{16}) + (C_0 → F)
A, B	→ Other	=	(A, B → C_{16}) + (C_0 → Out)
C_0	→ F	=	(C_0 → C_{16}) + (C_0 → F)
C_0	→ Other	=	(C_0 → C_{16}) + (C_0 → Out)
S_4-S_0	→ F	=	(S_4-S_0 → C_{16}) + (C_0 → F)
S_4-S_0	→ Other	=	(S_4-S_0 → C_{16}) + (C_0 → Out)
A, B	Setup time	=	(A, B → C_{16}) + (C_0 Setup time)
C_0	Setup time	=	(C_0 → C_{16}) + (C_0 Setup time)
S_4-S_0	Setup time	=	(S_4-S_0 → C_{16}) + (C_0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time (F register accumulate loop)		=	(Clock → C_{16}) + (C_0 Setup time)



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		15	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.5	mA

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

To Output / From Input	L4C383-55				L4C383-40				L4C383-26			
	F_{15}-F_0	N	OVF, Z	C_{16}	F_{15}-F_0	N	OVF, Z	C_{16}	F_{15}-F_0	N	OVF, Z	C_{16}
FTAB = 0, FTF = 0												
Clock	32	38	53	36	26	30	44	32	22	22	26	22
C_0	—	—	34	22	—	—	28	20	—	—	18	18
S_4-S_0	—	42	42	42	—	32	34	35	—	22	22	22
FTAB = 0, FTF = 1												
Clock	56	38	53	36	46	30	44	32	28	22	26	22
C_0	37	—	34	22	30	—	28	20	22	—	18	18
S_4-S_0	55	42	42	42	40	32	34	35	26	22	22	22
FTAB = 1, FTF = 0												
A_{15}-A_0, B_{15}-B_0	—	36	46	37	—	30	40	32	—	22	22	22
Clock	32	—	—	—	26	—	—	—	22	—	—	—
C_0	—	—	34	22	—	—	28	20	—	—	18	18
S_4-S_0	—	42	42	42	—	32	34	35	—	22	22	22
FTAB = 1, FTF = 1												
A_{15}-A_0, B_{15}-B_0	55	36	46	37	40	30	40	32	26	22	22	22
Clock	56	38	53	36	46	30	44	32	28	22	26	22
C_0	37	—	34	22	30	—	28	20	22	—	18	18
S_4-S_0	55	42	42	42	40	32	34	35	26	22	22	22

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

	L4C383-55				L4C383-40				L4C383-26			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
Input	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_{15}-A_0, B_{15}-B_0	8	2	35	2	8	2	28	2	8	2	16	2
C_0	21	0	21	0	16	0	16	0	8	0	8	0
S_4-S_0	44	0	44	0	32	0	32	0	18	0	18	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	10	2	10	2	10	2	10	2	8	2	8	2

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	L4C383-55	L4C383-40	L4C383-26
t_{ENA}	20	18	16
t_{DIS}	20	18	16

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	L4C383-55	L4C383-40	L4C383-26
Minimum Cycle Time	43	34	20
Highgoing Pulse	15	10	10
Lowgoing Pulse	15	10	10

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

To Output / From Input	L4C383-20				L4C383-15			
	F_{15}-F_0	N	OVF, Z	C_{16}	F_{15}-F_0	N	OVF, Z	C_{16}
FTAB = 0, FTF = 0								
Clock	11	20	20	20	11	15	15	15
C_0	—	—	14	14	—	—	13	13
S_4-S_0	—	18	20	18	—	14	15	14
FTAB = 0, FTF = 1								
Clock	20	20	20	20	15	15	15	15
C_0	18	—	14	14	14	—	13	13
S_4-S_0	20	18	20	18	15	14	15	14
FTAB = 1, FTF = 0								
A_{15}-A_0, B_{15}-B_0	—	16	20	17	—	14	15	14
Clock	11	—	—	—	11	—	—	—
C_0	—	—	14	14	—	—	13	13
S_4-S_0	—	18	20	18	—	14	15	14
FTAB = 1, FTF = 1								
A_{15}-A_0, B_{15}-B_0	20	16	20	17	15	14	15	14
Clock	20	20	20	20	15	15	15	15
C_0	18	—	14	14	14	—	13	13
S_4-S_0	20	18	20	18	15	14	15	14

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

Input	L4C383-20				L4C383-15			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_{15}-A_0, B_{15}-B_0	5	0	14	0	5	0	12	0
C_0	12	0	12	0	10	0	10	0
S_4-S_0	15	0	15	0	12	0	12	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	5	0	5	0	5	0	5	0

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	L4C383-20	L4C383-15	
t_{ENA}	8	6	
t_{DIS}	8	6	

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	L4C383-20	L4C383-15	
Minimum Cycle Time	18	14	
Highgoing Pulse	5	4	
Lowgoing Pulse	5	4	

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +125°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

To Output / From Input	L4C383-65				L4C383-45				L4C383-30			
	F15-F0	N	OVF, Z	C16	F15-F0	N	OVF, Z	C16	F15-F0	N	OVF, Z	C16
FTAB = 0, FTF = 0												
Clock	37	44	63	45	28	34	50	34	26	28	34	28
C0	—	—	42	25	—	—	32	23	—	—	22	22
S4-S0	—	48	48	48	—	38	38	38	—	28	28	28
FTAB = 0, FTF = 1												
Clock	68	44	63	45	56	34	50	34	34	28	34	28
C0	42	—	42	25	32	—	32	23	26	—	22	22
S4-S0	66	48	48	48	46	38	38	38	30	28	28	28
FTAB = 1, FTF = 0												
A15-A0, B15-B0	—	44	56	44	—	32	46	36	—	28	28	28
Clock	37	—	—	—	28	—	—	—	26	—	—	—
C0	—	—	42	25	—	—	32	23	—	—	22	22
S4-S0	—	48	48	48	—	38	38	38	—	28	28	28
FTAB = 1, FTF = 1												
A15-A0, B15-B0	65	44	56	44	45	32	46	36	30	28	28	28
Clock	68	44	63	45	56	34	50	34	34	28	34	28
C0	42	—	42	25	32	—	32	23	26	—	22	22
S4-S0	66	48	48	48	46	38	38	38	30	28	28	28

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

Input	L4C383-65				L4C383-45				L4C383-30			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A15-A0, B15-B0	10	3	43	3	8	3	33	3	8	3	20	3
C0	25	0	25	0	20	0	20	0	12	0	12	0
S4-S0	50	0	50	0	36	0	36	0	20	0	20	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	12	2	12	2	10	2	10	2	10	2	10	2

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	L4C383-65	L4C383-45	L4C383-30
t_{ENA}	22	20	18
t_{DIS}	22	20	18

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	L4C383-65	L4C383-45	L4C383-30
Minimum Cycle Time	52	38	26
Highgoing Pulse	20	15	12
Lowgoing Pulse	20	15	12

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +125°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

From Input \ To Output	L4C383-25				L4C383-20			
	F15-F0	N	OVF, Z	C16	F15-F0	N	OVF, Z	C16
FTAB = 0, FTF = 0								
Clock	14	24	24	24	14	20	20	20
C0	—	—	18	18	—	—	16	16
S4-S0	—	22	24	22	—	18	20	18
FTAB = 0, FTF = 1								
Clock	25	24	24	24	20	20	20	20
C0	21	—	18	18	17	—	16	16
S4-S0	25	22	24	22	20	18	20	18
FTAB = 1, FTF = 0								
A15-A0, B15-B0	—	20	25	22	—	17	20	17
Clock	14	—	—	—	14	—	—	—
C0	—	—	18	18	—	—	16	16
S4-S0	—	22	24	22	—	18	20	18
FTAB = 1, FTF = 1								
A15-A0, B15-B0	25	20	25	22	20	17	20	17
Clock	25	24	24	24	20	20	20	20
C0	21	—	18	18	17	—	16	16
S4-S0	25	22	24	22	20	18	20	18

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

Input	L4C383-25				L4C383-20			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A15-A0, B15-B0	7	2	14	2	6	2	12	2
C0	14	0	14	0	12	0	12	0
S4-S0	19	0	19	0	16	0	16	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	7	0	7	0	6	0	6	0

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	L4C383-25	L4C383-20	
tENA	14	10	
tDIS	14	10	

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	L4C383-25	L4C383-20	
Minimum Cycle Time	20	18	
Highgoing Pulse	8	6	
Lowgoing Pulse	8	6	

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

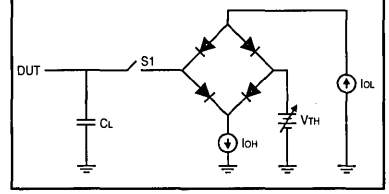
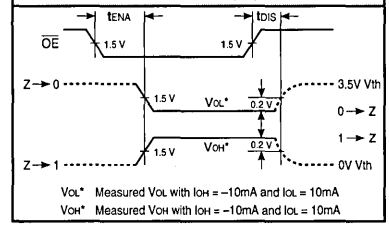
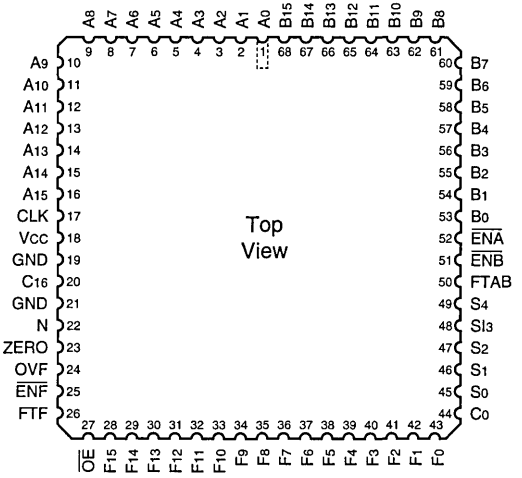


FIGURE B. THRESHOLD LEVELS

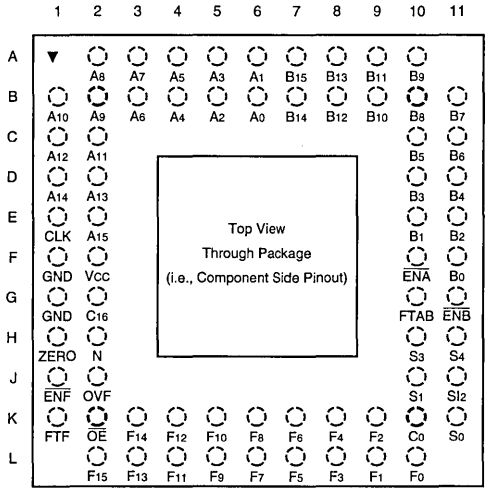


ORDERING INFORMATION

68-pin



68-pin



Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)	Ceramic Pin Grid Array (G1)
	0°C to +70°C — COMMERCIAL SCREENING		
55 ns	L4C383JC55		L4C383GC55
40 ns	L4C383JC40		L4C383GC40
26 ns	L4C383JC26		L4C383GC26
20 ns	L4C383JC20		L4C383GC20
15 ns	L4C383JC15		L4C383GC15
	–55°C to +125°C — COMMERCIAL SCREENING		
65 ns			L4C383GM65
45 ns			L4C383GM45
30 ns			L4C383GM30
25 ns			L4C383GM25
20 ns			L4C383GM20
	–55°C to +125°C — MIL-STD-883 COMPLIANT		
65 ns		L4C383KMB65	L4C383GMB65
45 ns		L4C383KMB45	L4C383GMB45
30 ns		L4C383KMB30	L4C383GMB30
25 ns		L4C383KMB25	L4C383GMB25
20 ns		L4C383KMB20	L4C383GMB20

FEATURES

- 32-bit Input, 32-bit Output Multiplexed to 16 Lines
- Full 0-31 Position Barrel Shift Capability
- Integral Priority Encoder for 32-bit Floating Point Normalization
- Sign-Magnitude or Two's Complement Mantissa Representation
- 32-bit Linear Shifts with Sign or Zero Fill
- Independent Priority Encoder Outputs for Block Floating Point
- DECC SMD No. 5962-89717
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC
  - 68-pin Ceramic PGA

DESCRIPTION

The **LSH32** is a 32-bit high speed shifter designed for use in floating point normalization, word pack/unpack, field extraction, and similar applications. It has 32 data inputs, and 16 output lines. Any shift configuration of the 32 inputs, including circular (barrel) shifting, left shifts with zero fill, and right shift with sign extend are possible. In addition, a built-in priority encoder is provided to aid floating point normalization.

SHIFT ARRAY

The 32 inputs to the LSH32 are applied to a 32-bit shift array. The 32 outputs of this array are multiplexed down to 16 lines for presentation at the device outputs. The array may be configured such that any contiguous 16-bit field (including wraparound of the 32 inputs) may be presented to the output pins under control of the shift code field (wrap mode). Alternatively, the wrap feature may be disabled, resulting in zero or sign bit fill, as appropriate (fill mode). The shift code control assignments and the resulting input to output mapping for the wrap mode are shown in Table 1.

Essentially the LSH32 is configured as a left shift device. That is, a shift code of 00000_2 results in no shift of the input field. A code of 00001_2 provides an effective left shift of 1 position, etc. When viewed as a right shift, the shift code corresponds to the two's complement of the shift distance, i.e., a shift code of 11111_2 (-1_{10}) results in a right shift of one position, etc.

When not in the wrap mode, the LSH32 fills bit positions for which there is no corresponding input bit. The fill value and the positions filled depend on the RIGHT/$\overline{\text{LEFT}}$ (R/$\overline{\text{L}}$) direction pin. This pin is a don't care input when in wrap mode. For left shifts in fill mode, lower bits are filled with zero as shown in Table 2. For right shifts, however, the SIGN input is used as the fill value. Table 3 depicts the bits to be filled as a function of shift code for the right shift case. Note that the R/$\overline{\text{L}}$ input changes only the fill convention, and does not affect the definition of the shift code.

In fill mode, as in wrap mode, the shift code input represents the number of shift positions directly for left shifts, but the two's complement of the shift code results in the equivalent right shift. However, for fill mode the R/$\overline{\text{L}}$ input can be viewed as the most

LSH32 BLOCK DIAGRAM

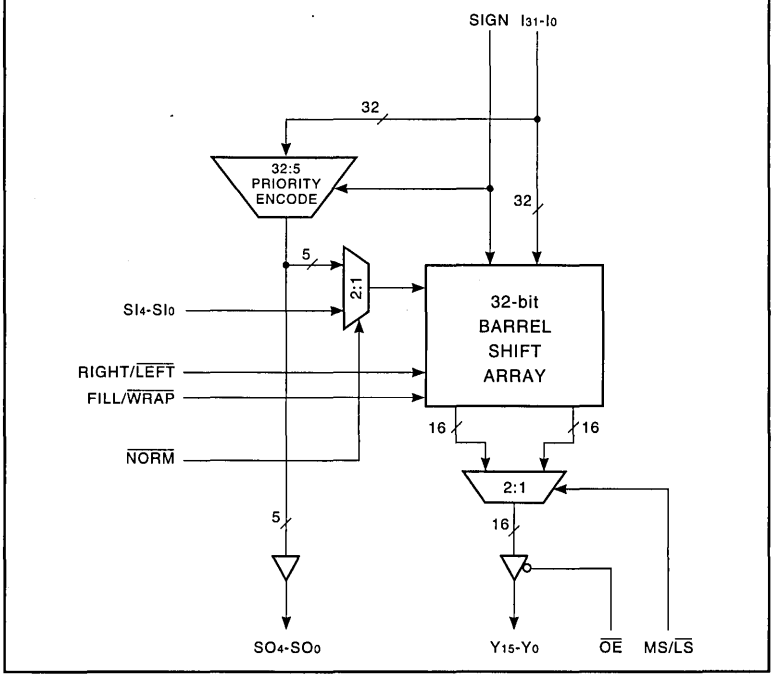


TABLE 1. WRAP MODE SHIFT CODE DEFINITIONS

Shift Code	Y_{31}	Y_{30}	Y_{29}	•••	Y_{16}	Y_{15}	•••	Y_2	Y_1	Y_0
00000	I_{31}	I_{30}	I_{29}	•••	I_{16}	I_{15}	•••	I_2	I_1	I_0
00001	I_{30}	I_{29}	I_{28}	•••	I_{15}	I_{14}	•••	I_1	I_0	I_{31}
00010	I_{29}	I_{28}	I_{27}	•••	I_{14}	I_{13}	•••	I_0	I_{31}	I_{30}
00011	I_{28}	I_{27}	I_{26}	•••	I_{13}	I_{12}	•••	I_{31}	I_{30}	I_{29}
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
01111	I_{16}	I_{15}	I_{14}	•••	I_1	I_0	•••	I_{19}	I_{18}	I_{17}
10000	I_{15}	I_{14}	I_{13}	•••	I_0	I_{31}	•••	I_{18}	I_{17}	I_{16}
10001	I_{14}	I_{13}	I_{12}	•••	I_{31}	I_{30}	•••	I_{17}	I_{16}	I_{15}
10010	I_{13}	I_{12}	I_{11}	•••	I_{30}	I_{29}	•••	I_{16}	I_{15}	I_{14}
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
11100	I_3	I_2	I_1	•••	I_{20}	I_{19}	•••	I_6	I_5	I_4
11101	I_2	I_1	I_0	•••	I_{19}	I_{18}	•••	I_5	I_4	I_3
11110	I_1	I_0	I_{31}	•••	I_{18}	I_{17}	•••	I_4	I_3	I_2
11111	I_0	I_{31}	I_{30}	•••	I_{17}	I_{16}	•••	I_3	I_2	I_1

TABLE 2. FILL MODE SHIFT CODE DEFINITIONS — LEFT SHIFT

Shift Code	Y_{31}	Y_{30}	Y_{29}	•••	Y_{16}	Y_{15}	•••	Y_2	Y_1	Y_0
00000	I_{31}	I_{30}	I_{29}	•••	I_{16}	I_{15}	•••	I_2	I_1	I_0
00001	I_{30}	I_{29}	I_{28}	•••	I_{15}	I_{14}	•••	I_1	I_0	0
00010	I_{29}	I_{28}	I_{27}	•••	I_{14}	I_{13}	•••	I_0	0	0
00011	I_{28}	I_{27}	I_{26}	•••	I_{13}	I_{12}	•••	0	0	0
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
01111	I_{16}	I_{15}	I_{14}	•••	I_1	I_0	•••	0	0	0
10000	I_{15}	I_{14}	I_{13}	•••	I_0	0	•••	0	0	0
10001	I_{14}	I_{13}	I_{12}	•••	0	0	•••	0	0	0
10010	I_{13}	I_{12}	I_{11}	•••	0	0	•••	0	0	0
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
11100	I_3	I_2	I_1	•••	0	0	•••	0	0	0
11101	I_2	I_1	I_0	•••	0	0	•••	0	0	0
11110	I_1	I_0	0	•••	0	0	•••	0	0	0
11111	I_0	0	0	•••	0	0	•••	0	0	0

significant bit of a 6-bit two's complement shift code, comprised of $R/\overline{L}$ concatenated with the SI_4–SI_0 lines. Thus a positive shift code ($R/\overline{L} = 0$) results in a left shift of 0–31 positions, and a negative code ($R/\overline{L} = 1$) a right shift of up to 32 positions. The LSH32 can thus effectively select any contiguous 32-bit field out of a (sign extended and zero filled) 96-bit "input."

OUTPUT MULTIPLEXER

The shift array outputs are applied to a 2:1 multiplexer controlled by the $MS/\overline{LS}$ select line. This multiplexer makes available at the output pins either the most significant or least significant 16 outputs of the shift array.

PRIORITY ENCODER

The 32-bit input bus drives a priority encoder which is used to determine the first significant position for purposes of normalization. The priority encoder produces a five-bit code representing the location of the first non-zero bit in the input word. Code assignment is such that the priority encoder output represents the number of shift positions required to left align the first non-zero bit of the input word. Prior to the priority encoder, the input bits are individually exclusive OR'ed with the SIGN input. This allows normalization in floating point systems using two's complement mantissa representation. A negative value in two's complement representation will cause the exclusive OR gates to invert the input data to the encoder. As a result the leading significant digit will always be "1." This affects only the encoder inputs; the shift array always operates on the raw input data. The priority encoder function table is shown in Table 4.

TABLE 3. FILL MODE SHIFT CODE DEFINITIONS — RIGHT SHIFT

Shift Code	Y_{31}	Y_{30}	Y_{29}	•••	Y_{16}	Y_{15}	•••	Y_2	Y_1	Y_0
00000	S	S	S	•••	S	S	•••	S	S	S
00001	S	S	S	•••	S	S	•••	S	S	I_{31}
00010	S	S	S	•••	S	S	•••	S	I_{31}	I_{30}
00011	S	S	S	•••	S	S	•••	I_{31}	I_{30}	I_{29}
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
01111	S	S	S	•••	S	S	•••	I_{19}	I_{18}	I_{17}
10000	S	S	S	•••	S	I_{31}	•••	I_{18}	I_{17}	I_{16}
10001	S	S	S	•••	I_{31}	I_{30}	•••	I_{17}	I_{16}	I_{15}
10010	S	S	S	•••	I_{30}	I_{29}	•••	I_{16}	I_{15}	I_{14}
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
11100	S	S	S	•••	I_{20}	I_{19}	•••	I_6	I_5	I_4
11101	S	S	S	•••	I_{19}	I_{18}	•••	I_5	I_4	I_3
11110	S	S	I_{31}	•••	I_{18}	I_{17}	•••	I_4	I_3	I_2
11111	S	I_{31}	I_{30}	•••	I_{17}	I_{16}	•••	I_3	I_2	I_1

TABLE 4. PRIORITY ENCODER FUNCTION TABLE

I_{31}	I_{30}	I_{29}	•••	I_{16}	I_{15}	•••	I_2	I_1	I_0	Shift Code
1	X	X	•••	X	X	•••	X	X	X	00000
0	1	X	•••	X	X	•••	X	X	X	00001
0	0	1	•••	X	X	•••	X	X	X	00010
•	•	•	•••	•	•	•••	•	•	•	•
•	•	•	•••	•	•	•••	•	•	•	•
0	0	0	•••	1	X	•••	X	X	X	01111
0	0	0	•••	0	1	•••	X	X	X	10000
0	0	0	•••	0	0	•••	X	X	X	10001
•	•	•	•••	•	•	•••	•	•	•	•
•	•	•	•••	•	•	•••	•	•	•	•
0	0	0	•••	0	0	•••	0	1	X	11110
0	0	0	•••	0	0	•••	0	0	1	11111
0	0	0	•••	0	0	•••	0	0	0	11111

NORMALIZE MULTIPLXER

The $\overline{NORM}$ input, when asserted results in the priority encoder output driving the internal shift code inputs directly. It is exactly equivalent to routing the SO_4–SO_0 outputs back to the SI_4–SI_0 inputs. The $\overline{NORM}$ input provides faster normalization of 32-bit data by avoiding the delay associated with routing the shift code off chip. When using the $\overline{NORM}$ function, the LSH32 should be placed in fill mode, with the R/$\overline{L}$ input low.

APPLICATIONS EXAMPLES

Normalization of mantissas up to 32 bits can be accomplished directly by a single LSH32. The $\overline{NORM}$ input is asserted, and fill mode and left shift are selected. The normalized mantissa is then available at the device output in two 16-bit segments, under the control of the output data multiplexer select, the MS/$\overline{LS}$.

If it is desirable to avoid the necessity of multiplexing output data in 16-bit segments, two LSH32 devices can be used in parallel. Both devices receive the same input word, with the MS/$\overline{LS}$ select line of one wired high, and the other low. Each device will then independently determine the shift distance required for normalization, and the full 32 bits of output data will be available simultaneously.

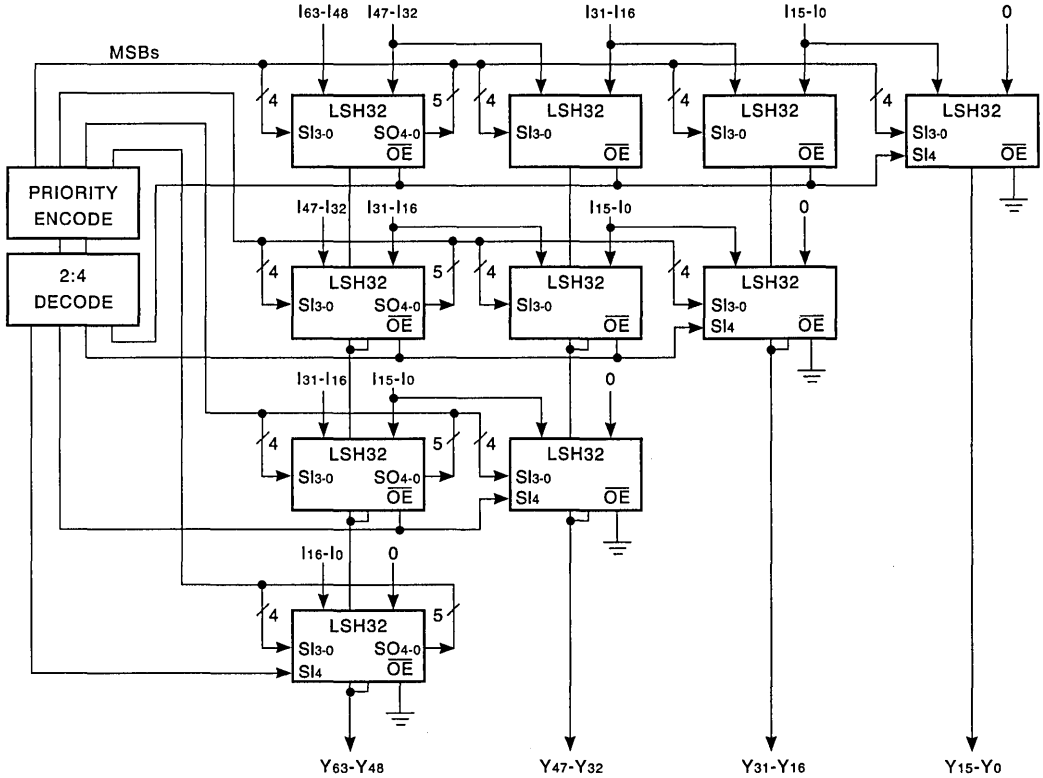
LONG-WORD NORMALIZATION (MULTIPLE CYCLES)

Normalization of floating point mantissas longer than 32 bits can be accomplished by cascading LSH32 units. When cascading for normalization, the device inputs are overlapped such that each device lower in priority than the first shares 16 inputs with its more significant neighbor. Fill mode and left shift are selected, however, internal normalization ($\overline{NORM}$) is not used. The most significant result half of each device is enabled to the output. The shift out (SO_4–SO_0) lines of the most significant slice are connected to the shift in lines of all slices, including the first. The exception is that all SI_4 lines are grounded, limiting the shift distance to 16 positions. The shift distance required for normalization is produced by the priority encoder in the most significant slice. The priority encoder will produce the shift code necessary to normalize the input word if the leading non-zero digit is found in the upper 16 bits. If this is the case, the number of shift positions necessary to accomplish normalization is placed on the SO_4–SO_0 outputs for use by all slices, and the appropriate 0–15 bit shift is accomplished. If the upper 16 bits are all zero, then the maximum shift of 15 places is executed. Single clock normalization requiring shifts longer than 16 bits can be accomplished by a bank-select technique described below.

SINGLE CYCLE LONG-WORD NORMALIZATION

An extension of the above concept is a single clock normalization of long words (potentially requiring shifts of more than 15 places). The arrangement of LSH32s required is shown in Figure 1. Cascading of LSH32 units is accomplished by connecting the SI_3–SI_0 input lines of each unit to the SO_3–SO_0 outputs of the most significant device in the row as before. Essen-

FIGURE 1. SINGLE CYCLE LONG-WORD NORMALIZATION USING LSH32S



tially the LSH32s are arranged in multiple rows or banks such that the inputs to successive rows are left-shifted by 16 positions. The outputs of each row are multiplexed onto a three-state bus. The normalization problem then reduces to selecting from among the several banks that one which has the first non-zero bit of the input value among its 16 most significant positions. If the most significant one in the input file was within the upper 16 locations of a given bank, the SO_4 output of the most significant slice in that bank will be low. Single clock normalization can thus be accomplished simply by enabling onto the three-state output bus the highest priority bank in which this condition is met. In this way the input word will be normalized regardless of the number of shift positions required to accomplish this.

The number of shift positions can be determined simply by concatenation of the SO_3–SO_0 outputs of the most significant slice in the selected row with the encoded Output Enable-bits determining the row number. Note that lower rows need not be fully populated. This is because they represent left shifts in multiples of 16 positions, and the lower bits of the output word will be zero filled. In order to accomplish this zero fill, the least significant device in each row is always enabled, and the row select is instead connected to the SI_4 input. This will force the shift length of the least significant device to a value greater than 15 whenever the row containing that device is not selected. This results in zero fill being accomplished by the equivalently positioned slice in a higher bank, as shown in the diagram.

BLOCK FLOATING POINT

With a small amount of external logic, block floating point operations are easily accomplished by the LSH32. Data resulting from a vector operation are applied to the LSH32 with the $\overline{NORM}$-input deasserted. The SO_4–SO_0 outputs fill then represent the normalization shift distance for each vector element in turn. By use of an external latch and comparator, the maximum shift distance encountered across all elements in the vector is saved for use in the next block operation (or block normalization). During this subsequent pass through the data, the shift code saved from the previous pass is applied uniformly across all elements of the vector. Since the LSH32 is not used in the internal normalize mode, this operation can be pipelined, thereby obtaining the desired shift distance for the next pass while simultaneously applying the normalization required from the previous pass.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.5	mA

SWITCHING CHARACTERISTICS

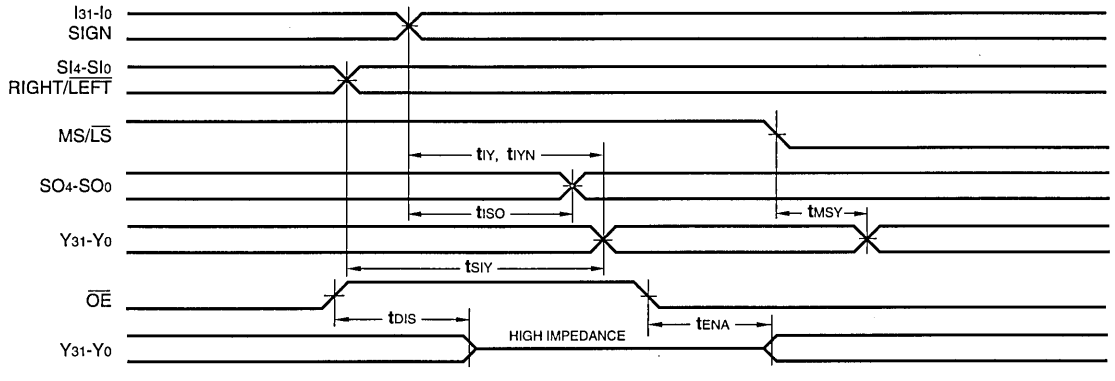
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LSH32–					
		42		32		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{IY}	I, SIGN Inputs to Y Outputs		42		32		20
t_{IYN}	I, SIGN Inputs to Y Outputs, Normalize Mode		75		60		20
t_{ISO}	I, SIGN Inputs to SO Outputs		55		42		20
t_{SIY}	SI, RIGHT/$\overline{\text{LEFT}}$ to Y Outputs		52		40		20
t_{MSY}	MS/$\overline{\text{LS}}$ Select to Y Outputs		28		24		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		20		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		20		20		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LSH32–					
		50		40		30	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{IY}	I, SIGN Inputs to Y Outputs		50		40		30
t_{IYN}	I, SIGN Inputs to Y Outputs, Normalize Mode		85		75		58
t_{ISO}	I, SIGN Inputs to SO Outputs		65		52		42
t_{SIY}	SI, RIGHT/$\overline{\text{LEFT}}$ to Y Outputs		62		52		40
t_{MSY}	MS/$\overline{\text{LS}}$ Select to Y Outputs		32		26		24
t_{DIS}	Three-State Output Disable Delay (Note 11)		22		20		17
t_{ENA}	Three-State Output Enable Delay (Note 11)		22		20		17

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

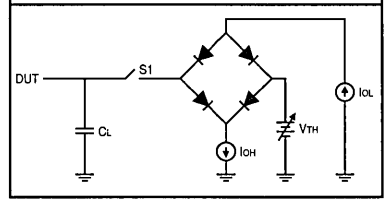
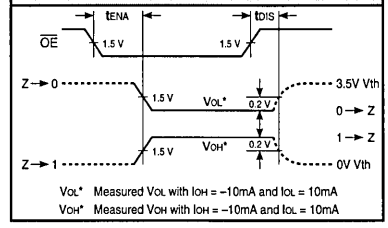


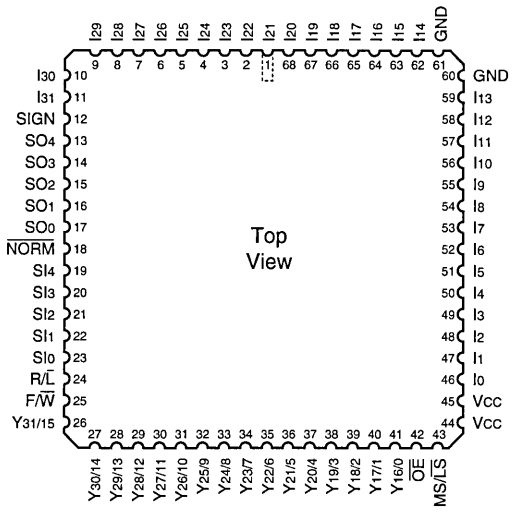
FIGURE B. THRESHOLD LEVELS



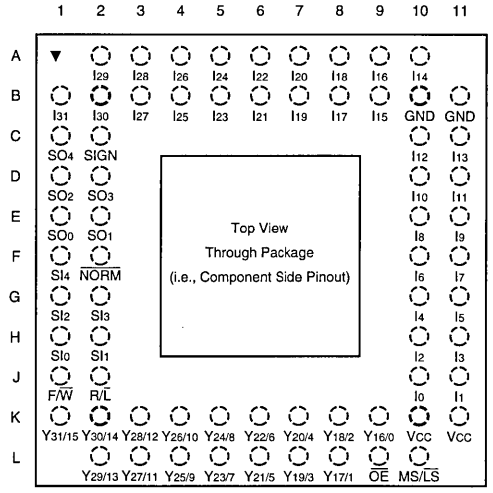
VOL* Measured VOL with IOH = –10mA and IOL = 10mA
VOH* Measured VOH with IOH = –10mA and IOL = 10mA

ORDERING INFORMATION

68-pin



68-pin



Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)	Ceramic Pin Grid Array (G1)
	0°C to +70°C — Commercial Screening		
42 ns	LSH32JC42		LSH32GC42
32 ns	LSH32JC32		LSH32GC32
20 ns	LSH32JC20		LSH32GC20
	–55°C to +125°C — Commercial Screening		
50 ns			LSH32GM50
40 ns			LSH32GM40
30 ns			LSH32GM30
	–55°C to +125°C — MIL-STD-883 Compliant		
50 ns		LSH32KMB50	LSH32GMB50
40 ns		LSH32KMB40	LSH32GMB40
30 ns		LSH32KMB30	LSH32GMB30

FEATURES

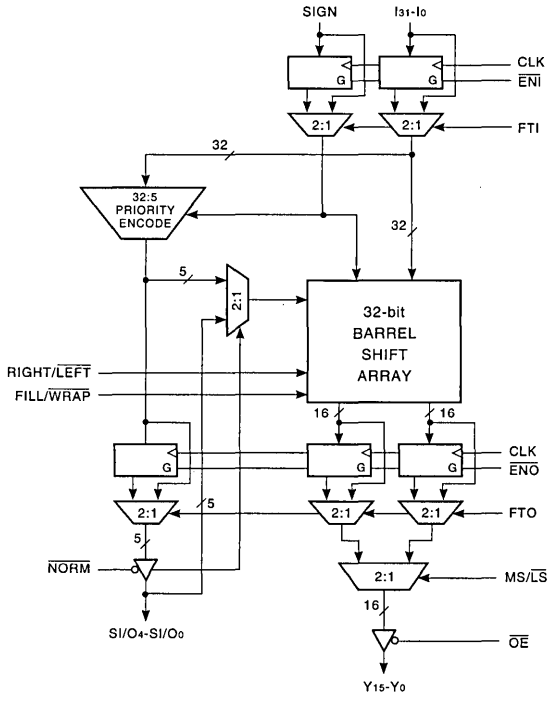
- 32-bit Input, 32-bit Output Multiplexed to 16 Lines
- Full 0-31 Position Barrel Shift Capability
- Integral Priority Encoder for 32-bit Floating Point Normalization
- Sign-Magnitude or Two's Complement Mantissa Representation
- 32-bit Linear Shifts with Sign or Zero Fill
- Independent Priority Encoder Outputs for Block Floating Point
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC
  - 68-pin Ceramic PGA

DESCRIPTION

The **LSH33** is a 32-bit high speed shifter designed for use in floating point normalization, word pack/unpack, field extraction, and similar applications. It has 32 data inputs, and 16 output lines. Any shift configuration of the 32 inputs, including circular (barrel) shifting, left shifts with zero fill, and right shifts with sign extension are possible. In addition, a built-in priority encoder is provided to aid floating point normalization.

Input/Output registers provide complete pipelined operation. Both have independent bypass paths for complete flexibility. When FTI = 1, the input registers are bypassed. Likewise, when FTO= 1, the output registers are bypassed.

LSH33 BLOCK DIAGRAM



SHIFT ARRAY

The 32 inputs, which can be registered, to the LSH33 are applied to a 32-bit shift array. The 32 outputs, which can also be registered, of this array are then multiplexed down to 16 lines for presentation at the device outputs. The array may be configured such that any contiguous 16-bit field (including wraparound of the 32 inputs) may be presented to the output pins under control of the shift code field (wrap mode). Alternatively, the wrap feature may be disabled, resulting in zero or sign bit fill, as appropriate (fill mode). The shift code control assignments and the resulting input to output mapping for the wrap mode are shown in Table 1.

Essentially the LSH33 is configured as a left shift device. That is, a shift code of 00000_2 results in no shift of the input field. A code of 00001_2 provides an effective left shift of 1 position, etc. When viewed as a right shift, the shift code corresponds to the two's complement of the shift distance, i.e., a shift code of 11111_2 (-1_{10}) results in a right shift of one position, etc.

When not in the wrap mode, the LSH33 fills bit positions for which there is no corresponding input bit. The fill value and the positions filled depend on the RIGHT/$\overline{\text{LEFT}}$ (R/$\overline{\text{L}}$) direction pin. This pin is a don't care input when in wrap mode. For left shifts in fill mode, lower bits are filled with zero as shown in Table 2. For right shifts, however, the SIGN input is used as the fill value. Table 3 depicts the bits to be filled as a function of shift code for the right shift case. Note that the R/$\overline{\text{L}}$ input changes only the fill convention, and does not affect the definition of the shift code.

TABLE 1. WRAP MODE SHIFT CODE DEFINITIONS

Shift Code	Y_{31}	Y_{30}	Y_{29}	•••	Y_{16}	Y_{15}	•••	Y_2	Y_1	Y_0
00000	I_{31}	I_{30}	I_{29}	•••	I_{16}	I_{15}	•••	I_2	I_1	I_0
00001	I_{30}	I_{29}	I_{28}	•••	I_{15}	I_{14}	•••	I_1	I_0	I_{31}
00010	I_{29}	I_{28}	I_{27}	•••	I_{14}	I_{13}	•••	I_0	I_{31}	I_{30}
00011	I_{28}	I_{27}	I_{26}	•••	I_{13}	I_{12}	•••	I_{31}	I_{30}	I_{29}
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
01111	I_{16}	I_{15}	I_{14}	•••	I_1	I_0	•••	I_{19}	I_{18}	I_{17}
10000	I_{15}	I_{14}	I_{13}	•••	I_0	I_{31}	•••	I_{18}	I_{17}	I_{16}
10001	I_{14}	I_{13}	I_{12}	•••	I_{31}	I_{30}	•••	I_{17}	I_{16}	I_{15}
10010	I_{13}	I_{12}	I_{11}	•••	I_{30}	I_{29}	•••	I_{16}	I_{15}	I_{14}
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
11100	I_3	I_2	I_1	•••	I_{20}	I_{19}	•••	I_6	I_5	I_4
11101	I_2	I_1	I_0	•••	I_{19}	I_{18}	•••	I_5	I_4	I_3
11110	I_1	I_0	I_{31}	•••	I_{18}	I_{17}	•••	I_4	I_3	I_2
11111	I_0	I_{31}	I_{30}	•••	I_{17}	I_{16}	•••	I_3	I_2	I_1

TABLE 2. FILL MODE SHIFT CODE DEFINITIONS — LEFT SHIFT

Shift Code	Y_{31}	Y_{30}	Y_{29}	•••	Y_{16}	Y_{15}	•••	Y_2	Y_1	Y_0
00000	I_{31}	I_{30}	I_{29}	•••	I_{16}	I_{15}	•••	I_2	I_1	I_0
00001	I_{30}	I_{29}	I_{28}	•••	I_{15}	I_{14}	•••	I_1	I_0	0
00010	I_{29}	I_{28}	I_{27}	•••	I_{14}	I_{13}	•••	I_0	0	0
00011	I_{28}	I_{27}	I_{26}	•••	I_{13}	I_{12}	•••	0	0	0
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
01111	I_{16}	I_{15}	I_{14}	•••	I_1	I_0	•••	0	0	0
10000	I_{15}	I_{14}	I_{13}	•••	I_0	0	•••	0	0	0
10001	I_{14}	I_{13}	I_{12}	•••	0	0	•••	0	0	0
10010	I_{13}	I_{12}	I_{11}	•••	0	0	•••	0	0	0
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
11100	I_3	I_2	I_1	•••	0	0	•••	0	0	0
11101	I_2	I_1	I_0	•••	0	0	•••	0	0	0
11110	I_1	I_0	0	•••	0	0	•••	0	0	0
11111	I_0	0	0	•••	0	0	•••	0	0	0

In fill mode, as in wrap mode, the shift code input represents the number of shift positions directly for left shifts, but the two's complement of the shift code results in the equivalent right shift. However, for fill mode the R/$\overline{L}$ input can be viewed as the most significant bit of a 6-bit two's complement shift code, comprised of R/$\overline{L}$ concatenated with the SI_4–SI_0 lines. Thus, a positive shift code (R/$\overline{L}$ = 0) results in a left shift of 0–31 positions, and a negative code (R/$\overline{L}$ = 1) a right shift of up to 32 positions. The LSH33 can thus effectively select any contiguous 32-bit field out of a (sign extended and zero filled) 96-bit "input."

OUTPUT MULTIPLEXER

The shift array outputs can be registered and then applied to a 2:1 multiplexer controlled by the MS/$\overline{LS}$ select line. This multiplexer makes available at the output pins either the most significant or least significant 16 outputs of the shift array.

PRIORITY ENCODER

The 32-bit input bus drives a priority encoder which is used to determine the first significant position for purposes of normalization. The priority encoder produces a five-bit code representing the location of the first non-zero bit in the input word. Code assignment is such that the priority encoder output represents the number of shift positions required to left align the first non-zero bit of the input word. Prior to the priority encoder, the input bits are individually exclusive OR'ed with the SIGN input. This allows normalization in floating point systems using two's complement mantissa representation. A negative value in two's complement representation will cause the exclusive OR gates to invert the input data to the encoder. As a result, the leading significant digit will always be "1."

TABLE 3. FILL MODE SHIFT CODE DEFINITIONS — RIGHT SHIFT

Shift Code	Y_{31}	Y_{30}	Y_{29}	•••	Y_{16}	Y_{15}	•••	Y_2	Y_1	Y_0
00000	S	S	S	•••	S	S	•••	S	S	S
00001	S	S	S	•••	S	S	•••	S	S	I_{31}
00010	S	S	S	•••	S	S	•••	S	I_{31}	I_{30}
00011	S	S	S	•••	S	S	•••	I_{31}	I_{30}	I_{29}
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
01111	S	S	S	•••	S	S	•••	I_{19}	I_{18}	I_{17}
10000	S	S	S	•••	S	I_{31}	•••	I_{18}	I_{17}	I_{16}
10001	S	S	S	•••	I_{31}	I_{30}	•••	I_{17}	I_{16}	I_{15}
10010	S	S	S	•••	I_{30}	I_{29}	•••	I_{16}	I_{15}	I_{14}
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
11100	S	S	S	•••	I_{20}	I_{19}	•••	I_6	I_5	I_4
11101	S	S	S	•••	I_{19}	I_{18}	•••	I_5	I_4	I_3
11110	S	S	I_{31}	•••	I_{18}	I_{17}	•••	I_4	I_3	I_2
11111	S	I_{31}	I_{30}	•••	I_{17}	I_{16}	•••	I_3	I_2	I_1

TABLE 4. PRIORITY ENCODER FUNCTION TABLE

I_{31}	I_{30}	I_{29}	•••	I_{16}	I_{15}	•••	I_2	I_1	I_0	Shift Code
1	X	X	•••	X	X	•••	X	X	X	00000
0	1	X	•••	X	X	•••	X	X	X	00001
0	0	1	•••	X	X	•••	X	X	X	00010
•	•	•	•••	•	•	•••	•	•	•	•
•	•	•	•••	•	•	•••	•	•	•	•
0	0	0	•••	1	X	•••	X	X	X	01111
0	0	0	•••	0	1	•••	X	X	X	10000
0	0	0	•••	0	0	•••	X	X	X	10001
•	•	•	•••	•	•	•••	•	•	•	•
•	•	•	•••	•	•	•••	•	•	•	•
0	0	0	•••	0	0	•••	0	1	X	11110
0	0	0	•••	0	0	•••	0	0	1	11111
0	0	0	•••	0	0	•••	0	0	0	11111

This affects only the encoder inputs; the shift array always operates on the raw input data. The priority encoder function table is shown in Table 4.

NORMALIZE MULTIPLEXER

The $\overline{NORM}$ input, when asserted, results in the priority encoder output driving the internal shift code inputs directly. When using the $\overline{NORM}$ function, the LSH33 should be placed in fill mode, with the R/$\overline{L}$ input low.

When $\overline{NORM}$ is high (not asserted), the SI/O_4–SI/O_0 port acts as the shift code input to the shifter.

APPLICATIONS EXAMPLES

Normalization of mantissas up to 32 bits can be accomplished directly by a single LSH33. To do this, the $\overline{NORM}$ input is asserted, and fill mode and left shift are selected. The normalized mantissa is then available at the device output in two 16-bit segments, under the control of the output data multiplexer select, the MS/$\overline{LS}$ signal.

If it is desirable to avoid the necessity of multiplexing output data in 16-bit segments, two LSH33 devices can be used in parallel. Both devices receive the same input word, with the MS/$\overline{LS}$ select line of one wired high, and the other low. Each device will then independently determine the shift distance required for normalization, and the full 32 bits of output data will be available simultaneously.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.5	mA

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

From Input \ To Output	LSH33-40		LSH33-30		LSH33-20	
	Y_{15}-Y_0	SO_4-SO_0	Y_{15}-Y_0	SO_4-SO_0	Y_{15}-Y_0	SO_4-SO_0
FTI = 0, FTO = 0						
CLK	28	28	24	24	15	15
MS/$\overline{LS}$	28	—	24	—	15	—
FTI = 0, FTO= 1						
CLK ($\overline{NORM}$ = 0/1)	73/40	55/—	58/30	42/—	20/20	20/—
SI_4-SI_0	52	—	40	—	20	—
R/$\overline{L}$, F/$\overline{W}$	52	—	40	—	20	—
MS/$\overline{LS}$	28	—	24	—	15	—
FTI = 1, FTO = 0						
CLK	28	28	24	24	15	15
MS/$\overline{LS}$	28	—	24	—	15	—
FTI = 1, FTO = 1						
I_{31}-I_0, SIGN ($\overline{NORM}$ = 0/1)	73/40	55/—	58/30	42/—	20/20	20/—
SI_4-SI_0	52	—	40	—	20	—
R/$\overline{L}$, F/$\overline{W}$	52	—	40	—	20	—
MS/$\overline{LS}$	28	—	24	—	15	—

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

Input	LSH33-40				LSH33-30				LSH33-20			
	FTI = 0		FTI = 1		FTI = 0		FTI = 1		FTI = 0		FTI = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
I_{31}-I_0, SIGN	12	3	20	2	10	3	15	2	8	0	8	2
SI_4-SI_0	17	0	17	0	15	0	15	0	8	0	8	0
R/$\overline{L}$, F/$\overline{W}$	12	0	12	0	10	0	10	0	8	0	8	0
$\overline{ENI}$, $\overline{ENO}$	12	0	12	0	10	0	10	0	8	0	8	0

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	LSH33-40	LSH33-30	LSH33-20
t_{ENA}	20	17	15
t_{DIS}	20	17	15

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	LSH33-40	LSH33-30	LSH33-20
Minimum Cycle Time	30	20	15
Highgoing Pulse	12	9	7
Lowgoing Pulse	12	9	7

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +125°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

From Input \ To Output	LSH33-50		LSH33-40		LSH33-30	
	Y_{15}-Y_0	SO_4-SO_0	Y_{15}-Y_0	SO_4-SO_0	Y_{15}-Y_0	SO_4-SO_0
FTI = 0, FTO = 0						
CLK	32	32	28	28	24	24
MS/$\overline{LS}$	32	—	28	—	24	—
FTI = 0, FTO= 1						
CLK ($\overline{NORM}$ = 0/1)	80/50	65/—	73/40	55/—	58/30	42/—
SI_4-SI_0	62	—	52	—	40	—
R/$\overline{L}$, F/$\overline{W}$	62	—	52	—	40	—
MS/$\overline{LS}$	32	—	28	—	24	—
FTI = 1, FTO = 0						
CLK	32	32	28	28	24	24
MS/$\overline{LS}$	32	—	28	—	24	—
FTI = 1, FTO = 1						
I_{31}-I_0, SIGN ($\overline{NORM}$ = 0/1)	80/50	65/—	73/40	55/—	58/30	42/—
SI_4-SI_0	62	—	52	—	40	—
R/$\overline{L}$, F/$\overline{W}$	62	—	52	—	40	—
MS/$\overline{LS}$	62	—	28	—	24	—

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

Input	LSH33-50				LSH33-40				LSH33-30			
	FTI = 0		FTI = 1		FTI = 0		FTI = 1		FTI = 0		FTI = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
I_{31}-I_0, SIGN	15	3	20	2	12	3	20	2	10	0	15	2
SI_4-SI_0	20	0	20	0	17	0	17	0	15	0	15	0
R/$\overline{L}$, F/$\overline{W}$	15	0	15	0	12	0	12	0	10	0	10	0
$\overline{ENI}$, $\overline{ENO}$	15	0	15	0	12	0	12	0	10	0	10	0

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	LSH33-50	LSH33-40	LSH33-30
t_{ENA}	22	20	17
t_{DIS}	22	20	17

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	LSH33-50	LSH33-40	LSH33-30
Minimum Cycle Time	35	30	20
Highgoing Pulse	15	12	9
Lowgoing Pulse	15	12	9

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

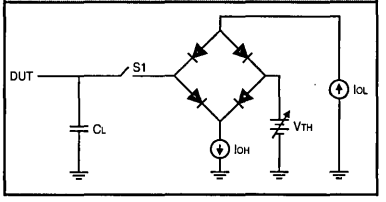
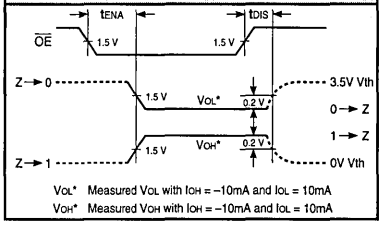
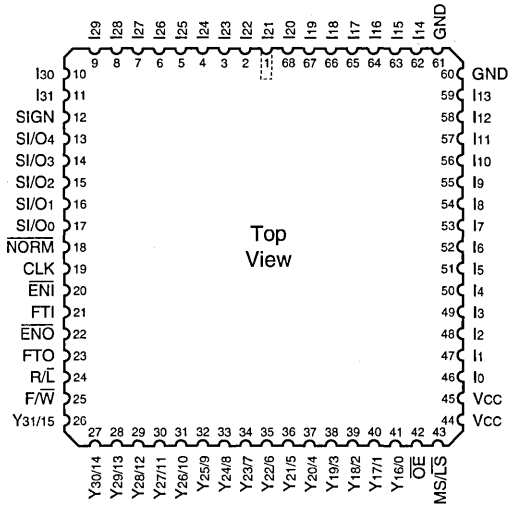


FIGURE B. THRESHOLD LEVELS

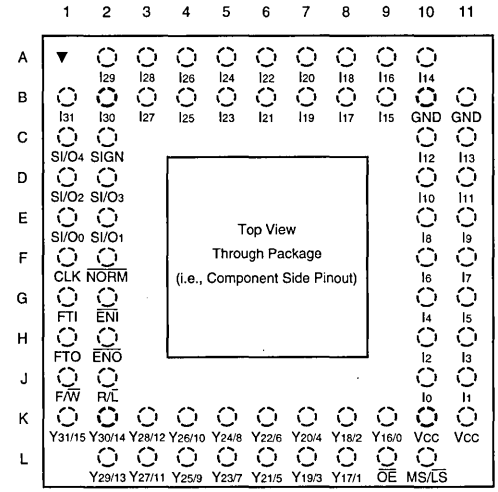


ORDERING INFORMATION

68-pin



68-pin



Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)	Ceramic Pin Grid Array (G1)
	0°C to +70°C — Commercial Screening		
40 ns	LSH33JC40	LSH33KC40	LSH33GC40
30 ns	LSH33JC30	LSH33KC30	LSH33GC30
20 ns	LSH33JC20	LSH33KC20	LSH33GC20
	–55°C to +125°C — Commercial Screening		
50 ns		LSH33KM50	LSH33GM50
40 ns		LSH33KM40	LSH33GM40
30 ns		LSH33KM30	LSH33GM30
	–55°C to +125°C — MIL-STD-883 Compliant		
50 ns		LSH33KMB50	LSH33GMB50
40 ns		LSH33KMB40	LSH33GMB40
30 ns		LSH33KMB30	LSH33GMB30

FEATURES

- High Speed (50 MHz), Low Power (125 mW), CMOS 64-bit Digital Correlator
- Replaces TRW/Raytheon TDC1023/TMC2023
- Bit Can be Selectively Masked
- Three-State Outputs
- DECC SMD No. 5962-89711
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Ceramic DIP
  - 28-pin Ceramic LCC

DESCRIPTION

The **L10C23** is a high speed CMOS 64-bit digital correlator. It is pin-for-pin equivalent to the TRW/Raytheon TDC1023/TMC2023. The L10C23 operates over the full military ambient temperature range using advanced CMOS technology.

The L10C23 produces the 7-bit correlation score of two input words of up to 64 bits, denoted A and B. The A and B inputs are serially shifted into two independently clocked 64-bit registers. The A register is clocked on the rising edge of CLK A, and the B register is clocked on the rising edge of CLK B.

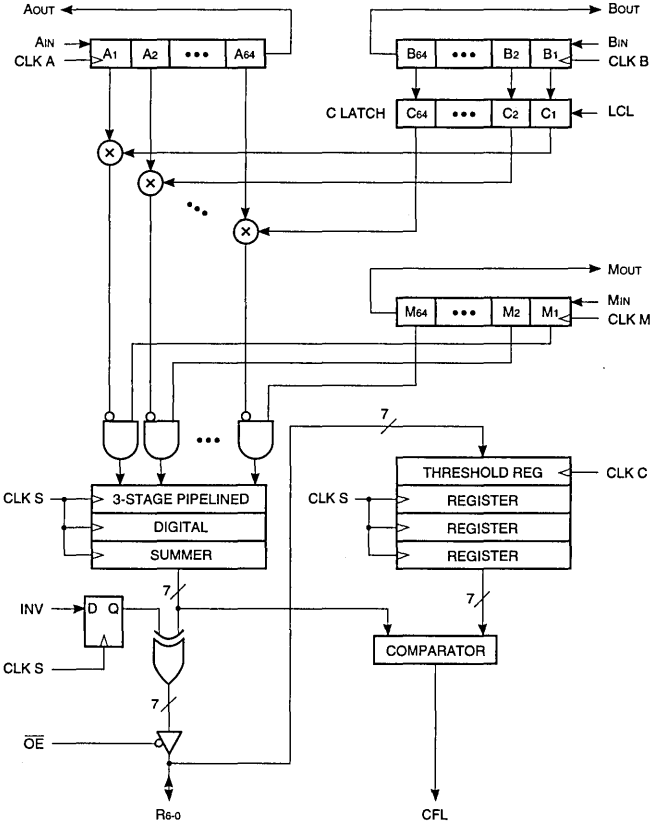
The outputs of the B register drive a 64-bit transparent latch, denoted the C latch. The C latch is controlled by the LCL (Load C Latch) input. A HIGH level on the LCL input causes the C latch to be transparent, allowing the contents of the B register to be applied directly to the correlator array. When the LCL input is LOW, the data in the C latch is held, so that the B input may be loaded with a new correlation reference without affecting the current reference value stored in C.

Each bit in the A register is exclusive NOR'ed with the corresponding bit in the C latch, implementing a single bit multiplication at each bit position.

The mask register, denoted by M, is a third 64-bit register, which is serially loaded from the M input on the rising edge of CLK M. Bit positions in the M register which are set to zero mask the corresponding bits in the A and C registers from participating in the correlation score. This can be used to reduce the effective length of the correlation, or to correlate against only one channel of a bit-multiplexed datastream without deinterleaving the data.

The output of the masking process is a 64-bit vector which contains ones in the locations in which A and B data match, and which are unmasked (M register contains a '1'). This 64-bit vector is applied to a pipelined digital summer which calculates the total number of ones in the vector (the correlation score). The summer network contains three pipeline stages, which are clocked on the rising edge of CLK S. Calculation of a

L10C23 Block Diagram



3

correlation score therefore requires three clock cycles, but a new result can be obtained on each cycle once the pipeline is filled.

Because a portion of the summer logic is located between the input registers and the first pipeline register, some timing restrictions exist between CLK S and CLK A, CLK B, or CLK M. CLK S may be tied to an input clock (usually CLK A) to obtain a continuously updated correlation score, delayed by three cycles from the data. Under this condition, CLK S may be skewed later than CLK A by no more than t_{SK} to assure that the A register outputs have not changed before the S clock occurs.

Alternatively, CLK S may be asynchronous to the input clocks, as long as data is stable at the pipeline register inputs prior to the CLK S rising edge. This condition can be met by assuring that CLK S occurs at least t_{PS} after the input clock.

The summer output represents a count of the number of matching positions in the input data streams. This 7-bit result can be inverted (one's complemented) by loading a '1' into the INV register.

Correlation values which exceed a predetermined threshold can be detected via the Threshold register and Comparator. The Threshold register is loaded with a 7-bit value via the R_{6-0} pins at the rising edge of CLK C and while $\overline{OE}$ is HIGH. To achieve synchronization with the digital summer, the Threshold register contents are fed into pipeline registers clocked by CLK S. The compare flag output (CFL) goes HIGH when the summer output is equal to or greater than the contents of the Threshold register.

Cascading the L10C23 devices for longer correlation lengths and more bits of reference or data precision is easily accomplished. The A, B, and M registers have serial outputs to directly drive the corresponding inputs of succeeding devices. The correlation scores of multiple devices in such a system should be added together to obtain the overall correlation score.

Correlation on data exceeding one bit of precision can be accomplished by first calculating single-bit correlation scores at each bit position, then adding the results after weighting them appropriately. Thus, one L10C23 would be used for each bit of precision in the data.

Logic Devices' L4C381 16-bit ALU can be used to assist in adding the outputs of several L10C23 correlators. When adding several 7-bit correlation scores, advantage can be taken of the fact that the sum of two 7-bit numbers will not exceed 8 bits. Thus the L4C381 can simultaneously perform two 7-bit additions. The first two operands are applied to A_{6-0} and B_{6-0}, with the result appearing on F_{7-0}. The second pair of operands are applied to A_{14-8} and B_{14-8}, with the result appearing in F_{15-8}. The unused inputs are tied to ground. If it can be guaranteed that at least one of the input scores will not reach its maximum value of 64, then this technique can also be applied in the second tier of adders. In this case, while the inputs have 8 bits of precision, the maximum value that their sum can assume is 255, which is expressable in 8 bits.

Alternatively, when performing long correlations on relatively slow datastreams, one L4C381 can be configured using its feedback mode to accumulate the correlation scores of a number of L10C23s. To accomplish this, the outputs of all the correlators are tied together on a three-state bus. Each one is sequentially enabled and clocked into the L4C381, which accumulates the total resulting score.

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

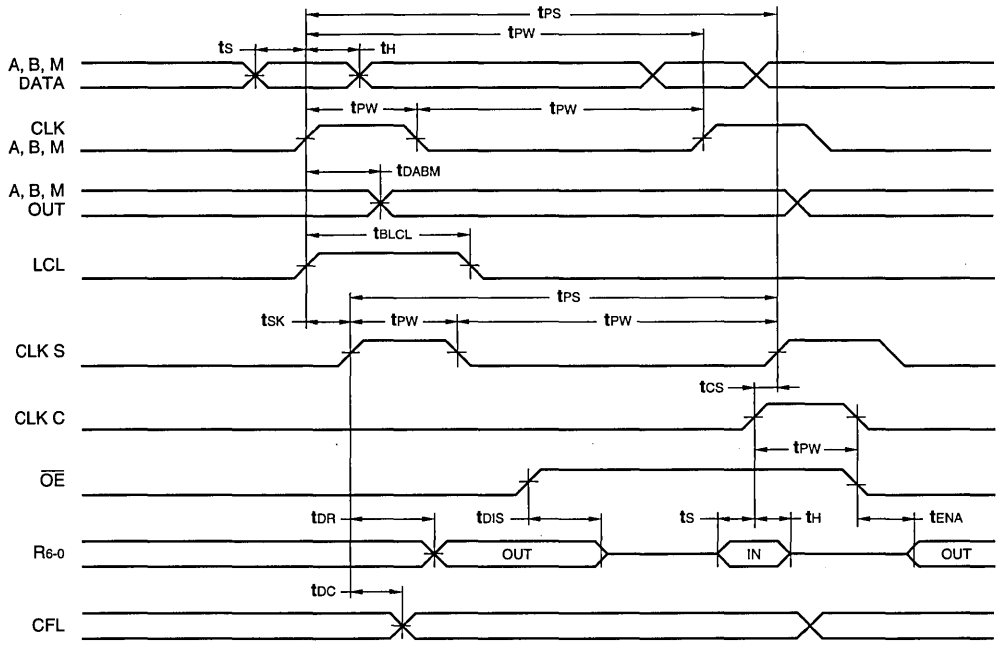
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		25	100	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			0.5	mA

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L10C23–					
		50		30		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PABM}	A, B, M Clock Period	50		28		20	
t_{PW}	A, B, M, S, C Clock Pulse Width	20		12		8	
t_S	Input Setup Time	20		10		10	
t_H	Input Hold Time	0		0		0	
t_{BLCL}	B Clock to LCL Hold	20		12		8	
t_{CS}	C Clock to S Clock	50		28		20	
t_{DABM}	A, B, M Clock to A, B, M Out		25		20		18
t_{PS}	S Clock Period, A, B, M Clock to S Clock Delay	50		28		20	
t_{SK}	A, B, M Clock to S Clock Skew (Note 8)		3		3		3
t_{DR}	S Clock to R_{6-0}		35		30		22
t_{DC}	S Clock to CFL		25		20		18
t_{ENA}	Output Enable Time (Note 11)		30		18		16
t_{DIS}	Output Disable Time (Note 11)		35		16		14

SWITCHING WAVEFORMS

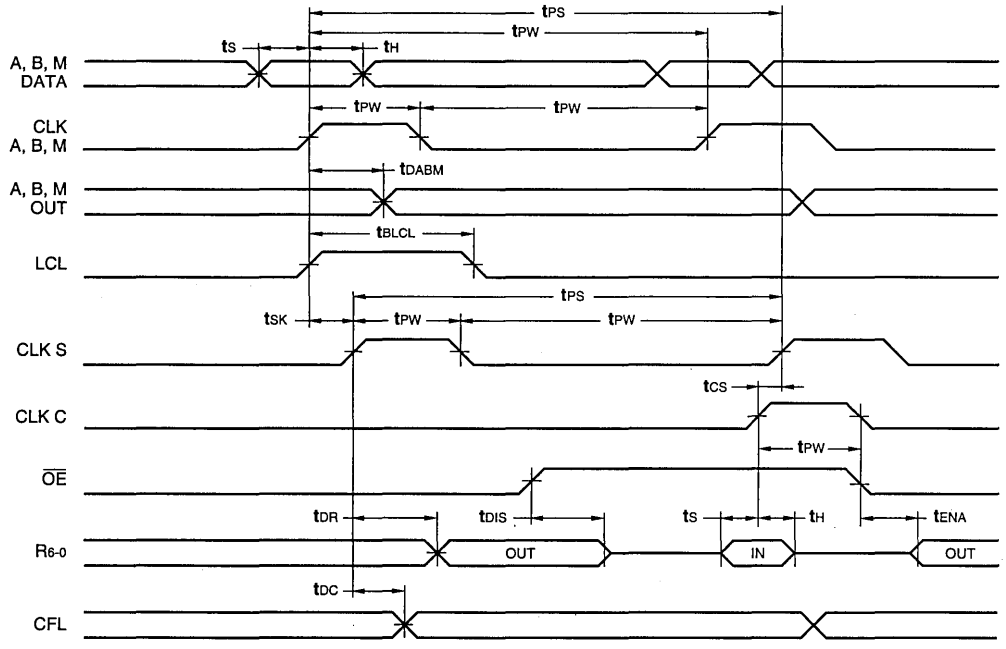


SWITCHING CHARACTERISTICS

MILITARY OPERATING RANGE (-55°C to +125°C) *Notes 9, 10 (ns)*

		L10C23–					
		60		35		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PABM}	A, B, M Clock Period	58		33		20	
t_{PW}	A, B, M, S, C Clock Pulse Width	20		14		8	
t_S	Input Setup Time	22		12		12	
t_H	Input Hold Time	0		0		0	
t_{BLCL}	B Clock to LCL Hold	20		14		8	
t_{CS}	C Clock to S Clock	58		33		20	
t_{DABM}	A, B, M Clock to A, B, M Out		30		23		20
t_{PS}	S Clock Period, A, B, M Clock to S Clock Delay	58		33		20	
t_{SK}	A, B, M Clock to S Clock Skew (Note 8)		3		3		3
t_{DR}	S Clock to R_{6-0}		40		35		27
t_{DC}	S Clock to CFL		30		23		18
t_{ENA}	Output Enable Time (Note 11)		35		20		18
t_{DIS}	Output Disable Time (Note 11)		40		18		16

SWITCHING WAVEFORMS



NOTES

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where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
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6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

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11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

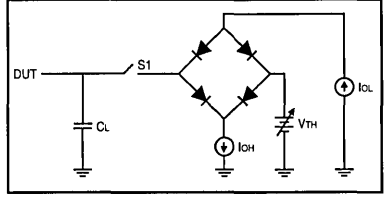
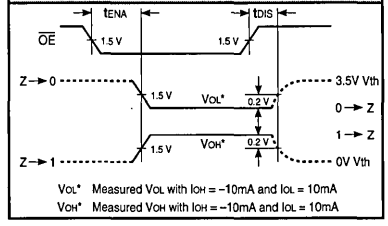
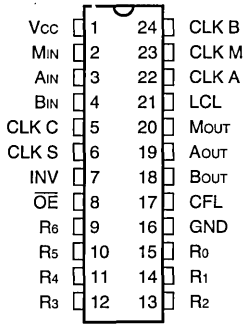


FIGURE B. THRESHOLD LEVELS

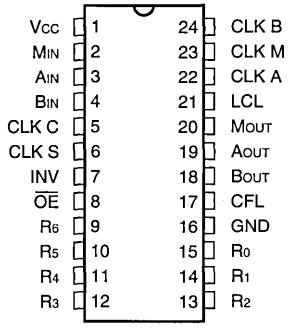


ORDERING INFORMATION

24-pin — 0.3" wide



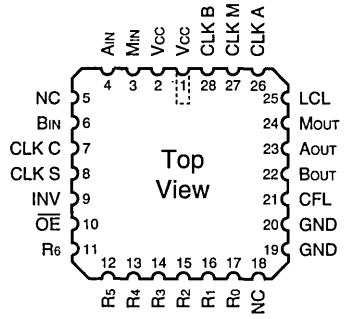
24-pin — 0.6" wide



Speed	Plastic DIP (P2)	Plastic DIP (P1)	Ceramic DIP (C4)
	0°C to +70°C — COMMERCIAL SCREENING		
50 ns	L10C23NC50	L10C23PC50	L10C23CC50
30 ns	L10C23NC30	L10C23PC30	L10C23CC30
20 ns	L10C23NC20	L10C23PC20	L10C23CC20
	–55°C to +125°C — COMMERCIAL SCREENING		
60 ns			L10C23CM60
35 ns			L10C23CM35
20 ns			L10C23CM20
	–55°C to +125°C — MIL-STD-883 COMPLIANT		
60 ns			L10C23CMB60
35 ns			L10C23CMB35
20 ns			L10C23CMB20

ORDERING INFORMATION

28-pin



Speed	Ceramic Leadless Chip Carrier (K1)	
	0°C to +70°C — COMMERCIAL SCREENING	
50 ns	L10C23KC50	
30 ns	L10C23KC30	
20 ns	L10C23KC20	
	–55°C to +125°C — COMMERCIAL SCREENING	
60 ns	L10C23KM60	
35 ns	L10C23KM35	
20 ns	L10C23KM20	
	–55°C to +125°C — MIL-STD-883 COMPLIANT	
60 ns	L10C23KMB60	
35 ns	L10C23KMB35	
20 ns	L10C23KMB20	

L2330
Coordinate Transformer

FEATURES

- Rectangular-to-Polar or Polar-to-Rectangular at 50 MHz
- 24-Bit Polar Phase Angle Accuracy
- Replaces Raytheon TMC2330A
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 120-pin Plastic Quad Flatpack
  - 120-pin Ceramic PGA

DESCRIPTION

The **L2330** is a coordinate transformer that converts bidirectionally between Rectangular and Polar coordinates.

When in Rectangular-to-Polar mode, the L2330 is able to retrieve phase and magnitude information or backward map from a rectangular raster display to a radial data set.

When in Polar-to-Rectangular mode, the L2330 is able to execute direct digital waveform synthesis and modulation. Real-time image-space conversions are achieved from radially-generated images, such as RADAR, SONAR, and ultrasound to raster display formats.

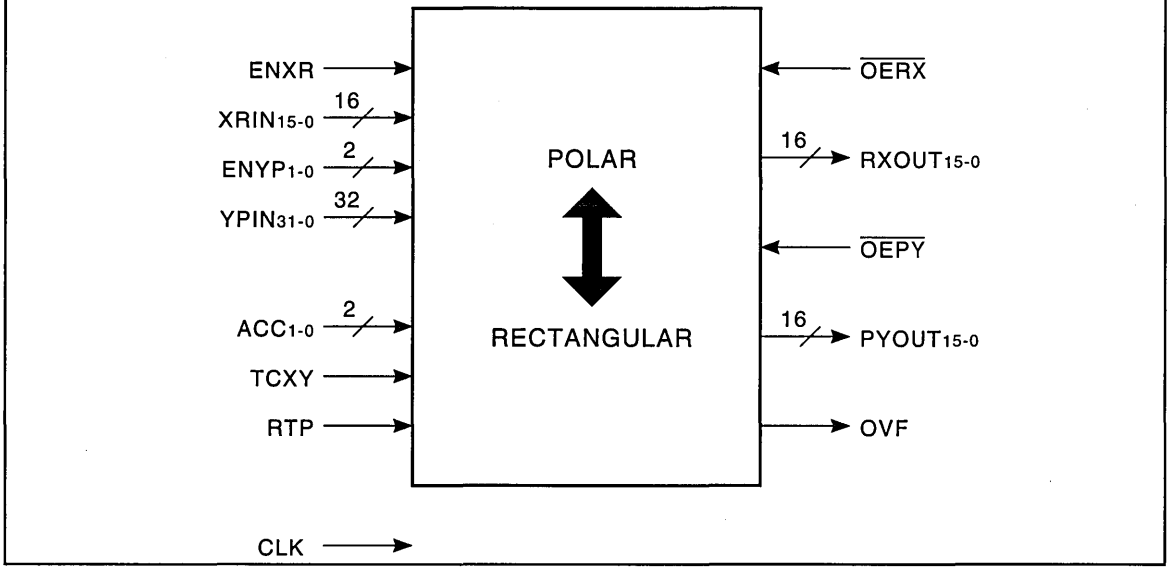
Functional Description

The L2330 converts bidirectionally between Rectangular (Cartesian) and Polar (Phase and Magnitude) coordinates. The user selects the numeric format. A valid transformed result is seen at the output after 22 clock cycles and will continue upon every clock cycle thereafter.

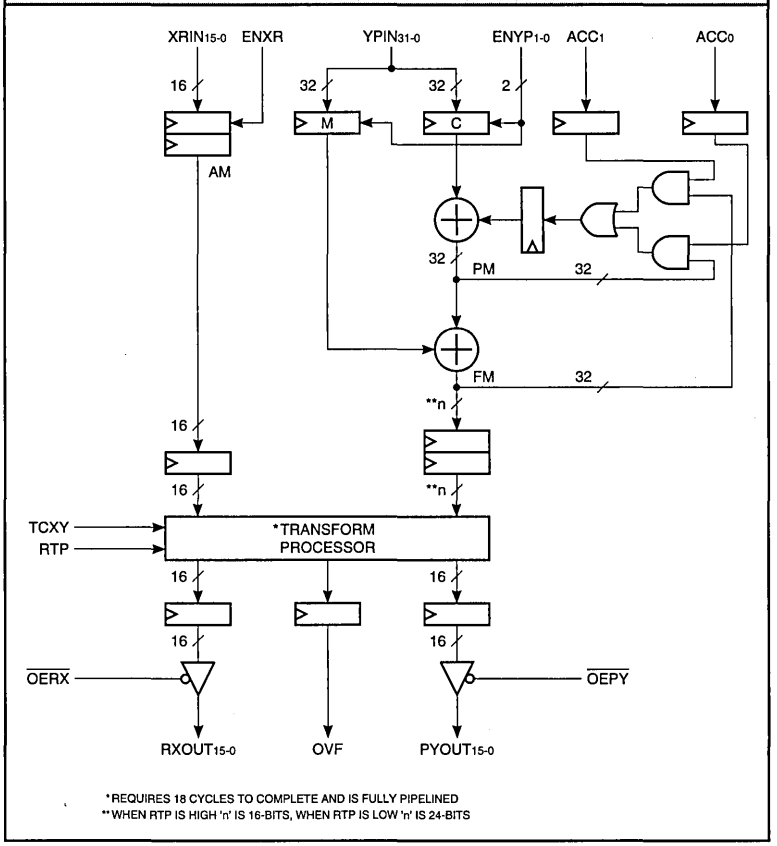
When in Rectangular-to-Polar mode, the user inputs a 16-bit Rectangular coordinate and the output generates a Polar transformation with 16-bit magnitude and 16-bit phase. The user may select the data format to be either two's complement or sign-and-magnitude Cartesian data format. Polar Magnitude data is always in magnitude format only. Polar Phase Angle data is modulo 2π so it may be regarded as either unsigned or two's complement format.

When in Polar-to-Rectangular mode, the user inputs 16-bit Polar Magnitude and 32-bit Phase data and the output generates a 16-bit Rectangular coordinate. The use may select the data format to be either two's complement or sign-and-magnitude Cartesian data format.

L2330 Block Diagram



L2330 Functional Block Diagram



SIGNAL DEFINITIONS

Power

VCC and GND

+5V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers.

Inputs

XRIN15-0 — x-coordinate/Magnitude Data Input

XRIN15-0 is the 16-bit Cartesian x-coordinate/Polar Magnitude Data input port. XRIN15-0 is latched on the rising edge of CLK.

YPIN31-0 — y-coordinate/Phase Angle Data Input

YPIN31-0 is the 32-bit Cartesian y-coordinate/Polar Phase Angle Data input port. When RTP is HIGH, the input accumulators should not be used. When ACC is LOW, the upper 16 bits of YPIN are the input port and the lower 16 bits become "don't cares". YPIN31-0 is latched on the rising edge of CLK.

Outputs

RXOUT15-0 — x-coordinate/Magnitude Data Output

RXOUT15-0 is the 16-bit Cartesian x-coordinate/Polar Magnitude Data output port. When $\overline{OERX}$ is HIGH, RXOUT15-0 is forced into the high-impedance state.

PYOUT15-0 — y-coordinate/Phase Angle Data Output

PYOUT15-0 is the 16-bit Cartesian y-coordinate/Polar Phase Angle Data output port. When $\overline{OEPY}$ is HIGH, PYOUT15-0 is forced into the high-impedance state.

Controls

ENXR — x-coordinate/Magnitude Data Input Enable

When ENXR is HIGH, XRIN is latched into the input register on the rising edge of clock. When ENXR is LOW, the value stored in the register is unchanged.

ENYP1-0 — y-coordinate/Phase Angle Data Input Control

ENYP1-0 is the 2-bit y-coordinate/Phase Angle Data Input Control that determines four modes as shown in

Table 1. Register Operation

ENYP1-0	M	C
0 0	Hold	Hold
0 1	Load	Hold
1 0	Hold	Load
1 1	Clear	Load

Table 2. Accumulator Control

ACC1-0	Configuration
0 0	No accumulation (normal operation)
0 1	PM accumulator path enabled
1 0	FM accumulator path enabled
1 1	Logical OR of PM and FM (Nonsensical)

Table 1. 'M' is the Modulation Register and 'C' is the Carrier Register as shown in the Functional Block Diagram.

RTP — Rectangular-to-Polar

When RTP is HIGH, Rectangular-to-Polar conversion mode is selected. When RTP is LOW, Polar-to-Rectangular conversion mode is selected.

ACC1-0 — Accumulator Control

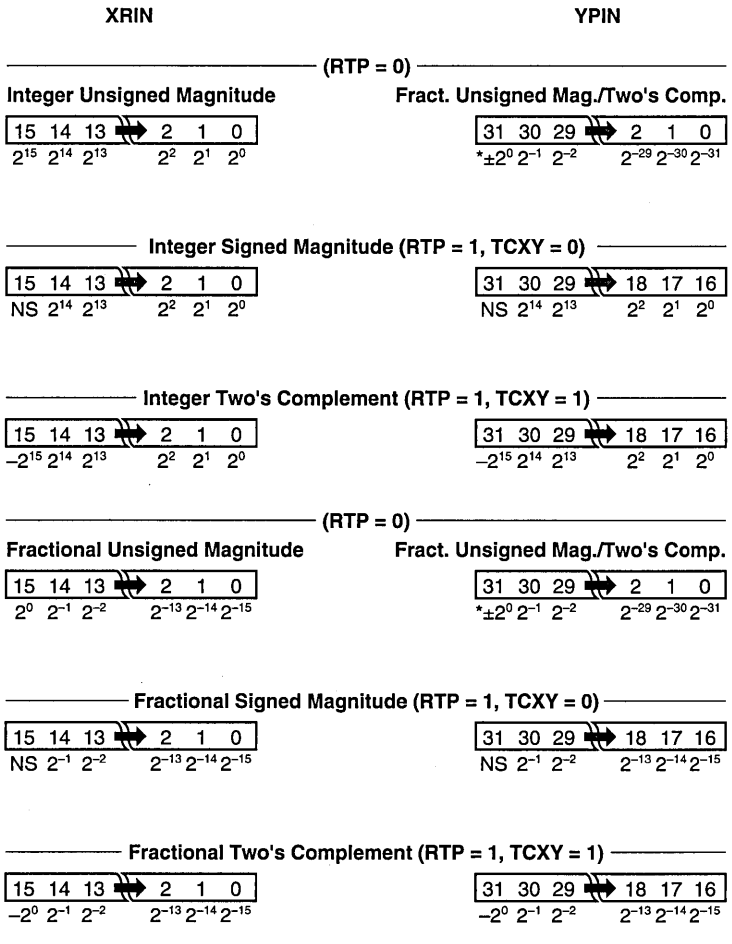
ACC1-0 is the 2-bit accumulator control that determines four modes as shown in Table 2. Changing of the internal phase Accumulator structure is very useful when RTP is LOW allowing for waveform synthesis and modulation. ACC1-0 set to '00' is most commonly used when RTP is HIGH unless performing backward mapping from Cartesian to Polar coordinates.

TCXY — Data Input/Output Format Select

When TCXY is HIGH, two's complement format is selected. When TCXY is LOW, sign-and-magnitude format is selected.

3

FIGURE 1A. INPUT FORMATS



*$\pm 2^{0}$ denotes two's complement sign or highest magnitude bit. Since phase angles are modulo 2π and phase accumulator is modulo 2^{32}, this bit may be regarded as $\pm\pi$.
NS denotes negative sign. (i.e. '1' negates the number)

OVF — Overflow Flag

OVF will go HIGH on the clock the magnitude of either of the current Cartesian coordinate outputs exceed the maximum range. OVF will return LOW on the clock that the Cartesian output value(s) return within range. An overflow condition can only occur when RTP is LOW.

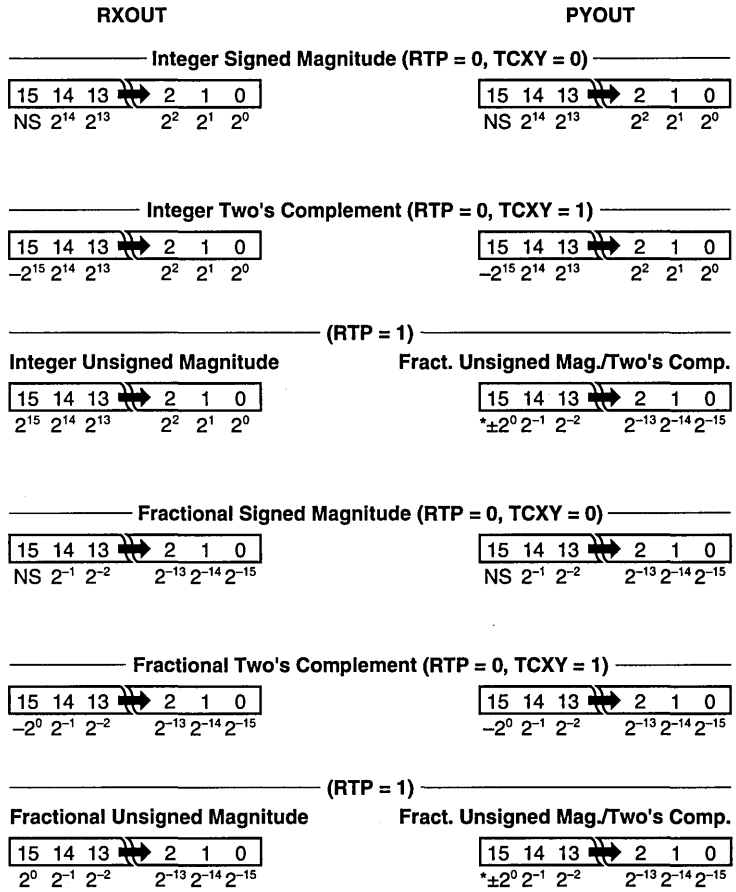
$\overline{OERX}$ — x-coordinate/Magnitude Data Output Enable

When $\overline{OERX}$ is LOW, RXOUT15-0 is enabled for output. When $\overline{OERX}$ is HIGH, RXOUT15-0 is placed in a high-impedance state.

$\overline{OEPY}$ — y-coordinate/Phase Angle Data Output Enable

When $\overline{OEPY}$ is LOW, PYOUT15-0 is enabled for output. When $\overline{OEPY}$ is HIGH, PYOUT15-0 is placed in a high-impedance state.

FIGURE 1B. OUTPUT FORMATS



*$\pm 2^0$ denotes two's complement sign or highest magnitude bit. Since phase angles are modulo 2π and phase accumulator is modulo 2^{32}, this bit may be regarded as $\pm\pi$.
NS denotes negative sign. (i.e. '1' negates the number)

Conversion Ranges

The L2330 supports 16-bit unsigned radii and 16-bit signed Cartesian coordinates. Since the 16-bit rectangular coordinate space does not completely cover the polar space defined by 16-bit radii, certain values of "r" will not map correctly. This condition is indicated by the overflow (OVF) flag.

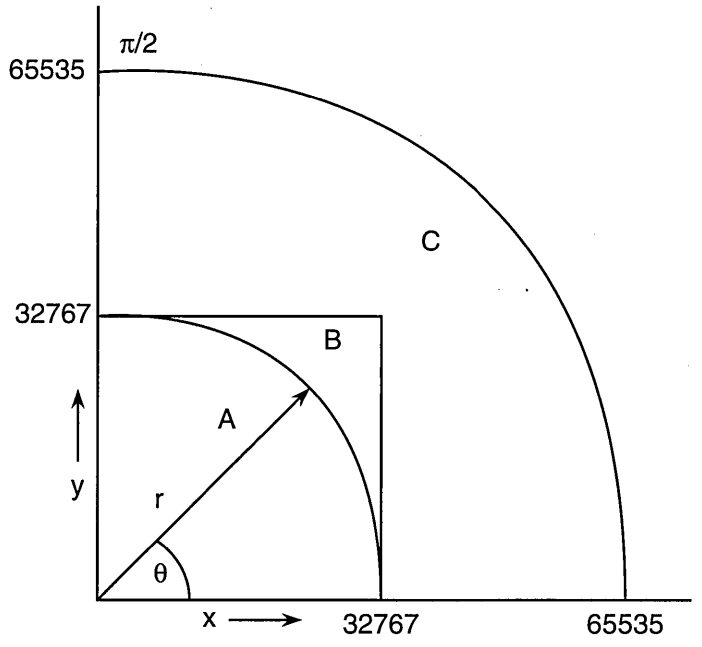
In Polar-to-Rectangular conversions, no overflow occurs for $r \leq 32767$ (7FFFH). Overflow will always occur when $r > 46341$ (B505H). Note that in signed magnitude mode r = 46340 (B504H) will also cause an overflow. For $32767 \leq r \leq 46340$, overflow may occur depending on the exact values of r and θ. Figure 2 shows, for the first quadrant, these three regions: A = no overflow (correct conversion), B = possible overflow, C = overflow. The other quadrants are mapped in a similar manner.

When in signed magnitude mode, the overflows on the other three quadrants are the same as in the first. This occurs because the signed magnitude number system is symmetric about zero. For example, if a given r and angle θ cause an overflow, the same r will cause an overflow for the angles $-\theta, \pi+\theta, \pi-\theta$.

However, when in two's complement mode, the overflows aren't quite the same. This occurs because the two's complement number system is not symmetric about zero. For example, if the X or Y component of the input is –32768 (8000H), no overflow occurs. But if the X or Y component of the input is +32768, overflow does occur.

When converting from Rectangular-to-Polar, if both inputs are zero the radius is zero but the angle is not defined. The L2330 will output 4707H in this case. Since the angle is not defined for a zero length vector, this is not an error.

FIGURE 2. CONVERSION RANGES



3

Internal Precision

When performing a coordinate transformation, inaccuracies are introduced by a combination of quantization and approximation errors. The accuracy of a coordinate transformer is dependent on the word length used for the input variables, the word length used for internal calculations, as well as the number of iterations or steps performed. Truncation errors are due to the finite word length, and approximation errors are due to the finite number of iterations. For example, in the case of performing a polar-to-rectangular transformation, the accuracy of the rotation will be determined by how closely the input rotation angle was approximated by the summation of sub-rotation angles.

In this study, we examine the effectiveness of 16-bit internal precision versus 24-bit internal precision. 10,000 random Rectangular coordinates were converted to Polar and back to Rectangular. The resulting Rectangular coordinates from this double conversion were then compared to the original Rectangular coordinates input to the device. These vectors, with maximum word width of 16-bits, were sent through a 16-bit internal processor versus a 24-bit internal processor. The Rectangular coordinates were limited to the following conditions:

$$-32769 < x < 32768$$
$$-32769 < y < 32768$$

Using the 16-bit internal processor, the resulting Rectangular coordinates were compared to the original Rectangular coordinates (see Table 3). Using the 24-bit internal processor, the resulting Rectangular coordinates were compared to the original Rectangular coordinates (see Table 3). By way of comparison between the 16-bit internal processor and the 24-bit internal processor, we find that the 24-bit internal processor is significantly more accurate. This accuracy is due to internal word length. During coordinate transformation, the number of bits truncated within a 24-bit internal processor are much smaller than in a 16-bit internal processor resulting in smaller error.

TABLE 3. DOUBLE CONVERSION ERROR

Error	Internal 16-bit	Internal 24-bit
Mean Error (X)	0.0216	–0.0118
Mean Error (Y)	–0.0036	–0.0028
Mean Absolute Error (X)	1.5736	0.5116
Mean Absolute Error (Y)	1.0756	0.5160
Root Mean Square Error (X)	2.0168	0.7664
Root Mean Square Error (Y)	1.4356	0.7738
Max Error (X)	6.0/–7.0	3.0/–3.0
Max Error (Y)	5.0/–5.0	3.0/–3.0
Standard Deviation of Error (X)	2.0168	0.7664
Standard Deviation of Error (Y)	1.4357	0.7739

Circle Test

When performing a polar-to-rectangular transformation, a 24-bit internal processor proves to be significantly more accurate than a 16-bit internal processor.

In this study, we compare how accurately a coordinate transformer with a 16-bit internal processor versus a 24-bit internal processor can calculate all the coordinates of a circle. By setting the radius to 7FFFH (maximum before overflow), θ is incremented using the accumulator of the L2330 in steps of 0000 4000H until all the points of a full circle are calculated into rectangular coordinates.

The resulting rectangular coordinates were plotted and graphed. A graphical representation of the resulting vectors for both 16-bit and 24-bit internal processors are compared near 45°. Theoretically, a perfect circle is the desired output but when the resulting vectors from a coordinate transformer with 16-bit internal processor are graphed and displayed as shown in Figure 3, we see significant errors due to the inherent properties of a digital coordinate transformation system. In comparison, the 24-bit internal processor proves to be significantly more accurate than a 16-bit internal processor due to minimization of truncation errors. In many applications, this margin of error is of great significance especially when being used in applications such as medical ultrasound or modulation techniques.

Data values for Figure 3 and Figure 4 are shown in Table 4. By looking at these values, we observe the step resolution on a 16-bit internal processor is not 1 unit in the x and y. In most cases, the minimum step resolution is 2 units in the x and y. On the other hand, step resolution on a 24-bit internal processor is 1 unit in the x and y thus resulting in greater accuracy.

The minimum theoretical angle resolution that could be produced is 0.00175° when x = 7FFFH and y = 1H. A 16-bit internal processor can produce a minimum angle resolution of only 0.00549° and will not be able to properly calculate the theoretical minimum angle resolution. On the other hand, a 24-bit internal processor can produce a minimum angle resolution of 0.00002° and could therefore properly calculate the theoretical minimum angle resolution.

FIGURE 3. CIRCLE TEST RESULT NEAR 45° (16-BIT INTERNAL PROCESSOR)

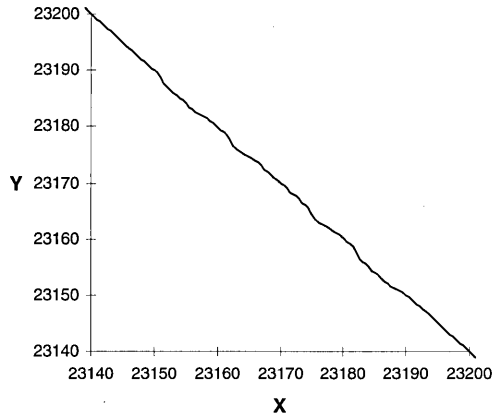


FIGURE 4. CIRCLE TEST RESULT NEAR 45° (24-BIT INTERNAL PROCESSOR)

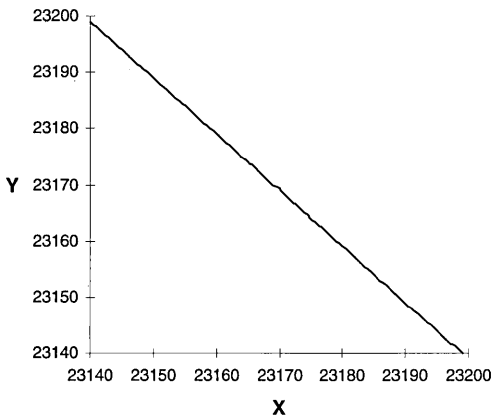


TABLE 4. RESULTANT DATA VALUES OF CIRCLE TEST NEAR 45°

16-bit Internal Processor				24-bit Internal Processor			
x	x (HEX)	y	y (HEX)	x	x (HEX)	y	y (HEX)
23201	5AA1	23139	5A63	23199	5A9F	23140	5A64
23199	5A9F	23141	5A65	23198	5A9E	23141	5A65
23199	5A9F	23141	5A65	23198	5A9E	23141	5A65
23199	5A9F	23141	5A65	23197	5A9D	23142	5A66
23199	5A9F	23141	5A65	23197	5A9D	23142	5A66
23197	5A9D	23143	5A67	23196	5A9C	23143	5A67
23197	5A9D	23143	5A67	23196	5A9C	23143	5A67
23197	5A9D	23143	5A67	23195	5A9B	23144	5A68
23197	5A9D	23143	5A67	23194	5A9A	23145	5A69
23195	5A9B	23145	5A69	23194	5A9A	23145	5A69
23195	5A9B	23145	5A69	23194	5A9A	23145	5A69
23195	5A9B	23145	5A69	23193	5A99	23146	5A6A
23195	5A9B	23145	5A69	23192	5A98	23147	5A6B
23192	5A98	23148	5A6C	23191	5A97	23148	5A6C
23192	5A98	03148	5A6C	23191	5A97	23148	5A6C
23192	5A98	23148	5A6C	23191	5A97	23148	5A6C
23192	5A98	23148	5A6C	23190	5A96	23149	5A6D
23190	5A96	23150	5A6E	23189	5A95	23150	5A6E
23190	5A96	23150	5A6E	23189	5A95	23150	5A6E
23190	5A96	23150	5A6E	23189	5A95	23150	5A6E
23190	5A96	23150	5A6E	23188	5A94	23151	5A6F
23187	5A93	23152	5A70	23187	5A93	23152	5A70
23187	5A93	23152	5A70	23186	5A92	23153	5A71
23187	5A93	23152	5A70	23186	5A92	23153	5A71
23187	5A93	23152	5A70	23186	5A92	23153	5A71
23185	5A91	23154	5A72	23185	5A91	23154	5A72
23185	5A91	23154	5A72	23184	5A90	23155	5A73
23185	5A91	23154	5A72	23184	5A90	23155	5A73
23185	5A91	23154	5A72	23184	5A90	23155	5A73
23183	5A8F	23156	5A74	23183	5A8F	23156	5A74

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

3

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			95	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			5	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

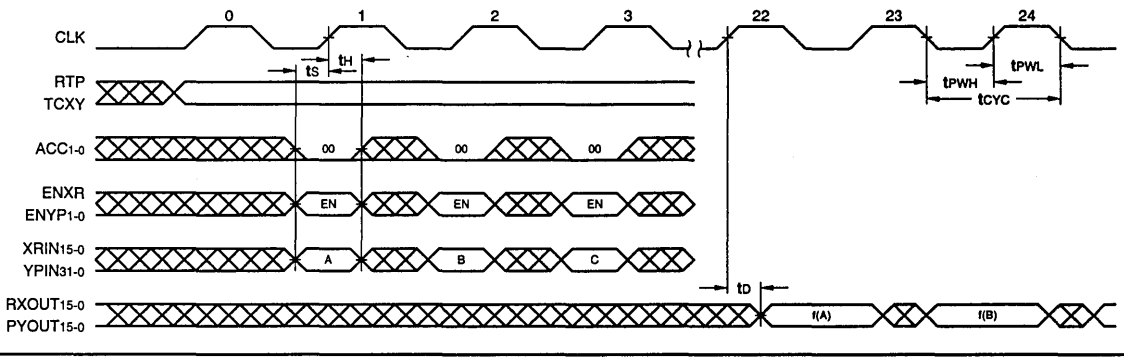
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L2330–					
		50		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20	
t_{PWL}	Clock Pulse Width Low	10		8		7	
t_{PWH}	Clock Pulse Width High	8		7		6	
t_S	Input Setup Time	12		7		6	
t_H	Input Hold Time	1		0		0	
t_D	Output Delay		22		18		16
t_{ENA}	Three-State Output Enable Delay (Note 11)		13		13		13
t_{DIS}	Three-State Output Disable Delay (Note 11)		13		13		13

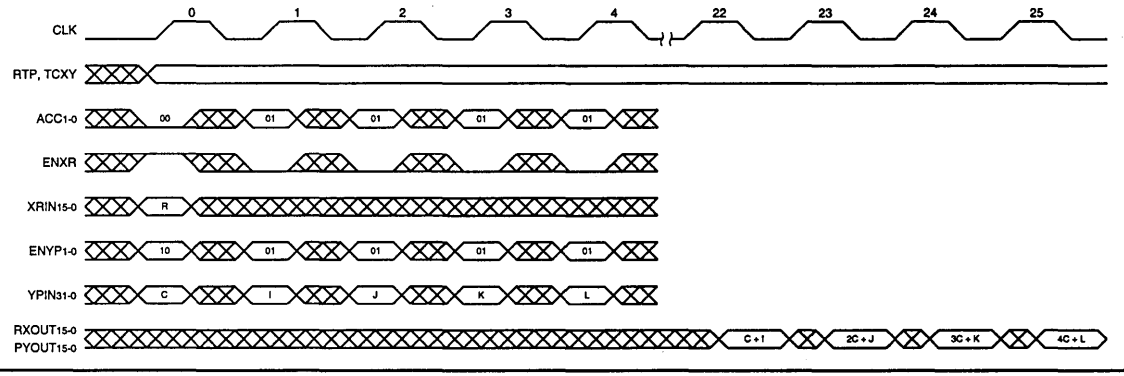
MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L2330–					
		50		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20	
t_{PWL}	Clock Pulse Width Low	11		9		7	
t_{PWH}	Clock Pulse Width High	8		7		6	
t_S	Input Setup Time	13		7		6	
t_H	Input Hold Time	2		2		1	
t_D	Output Delay		25		20		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		14		13
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		14		13

Switching Waveforms: No Accumulation



Switching Waveforms: Phase Modulation



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

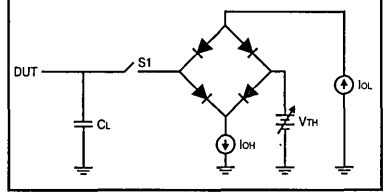
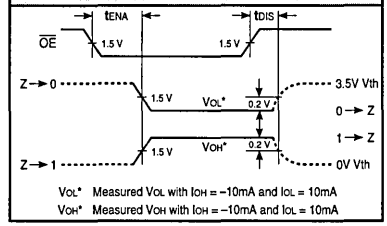
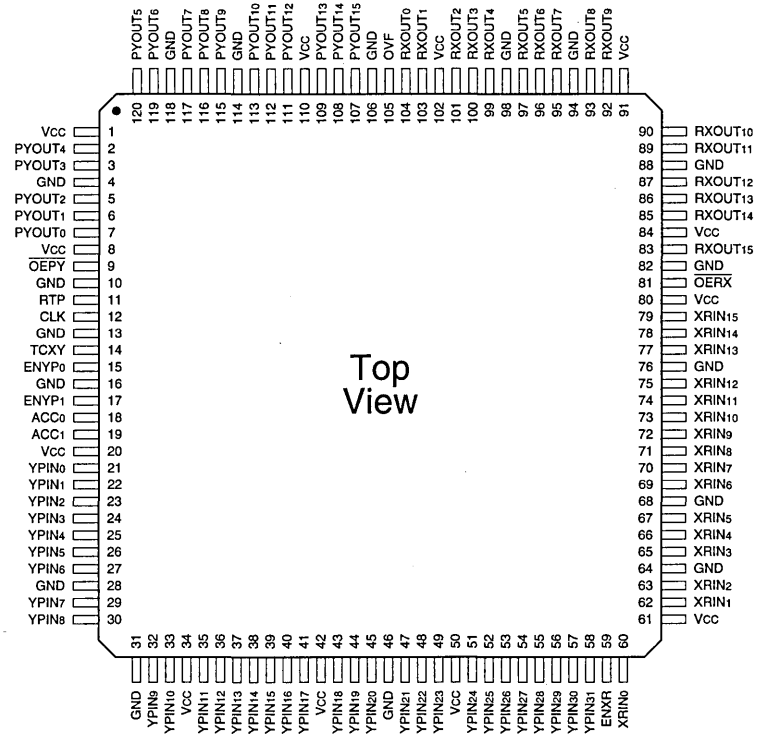


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

120-pin

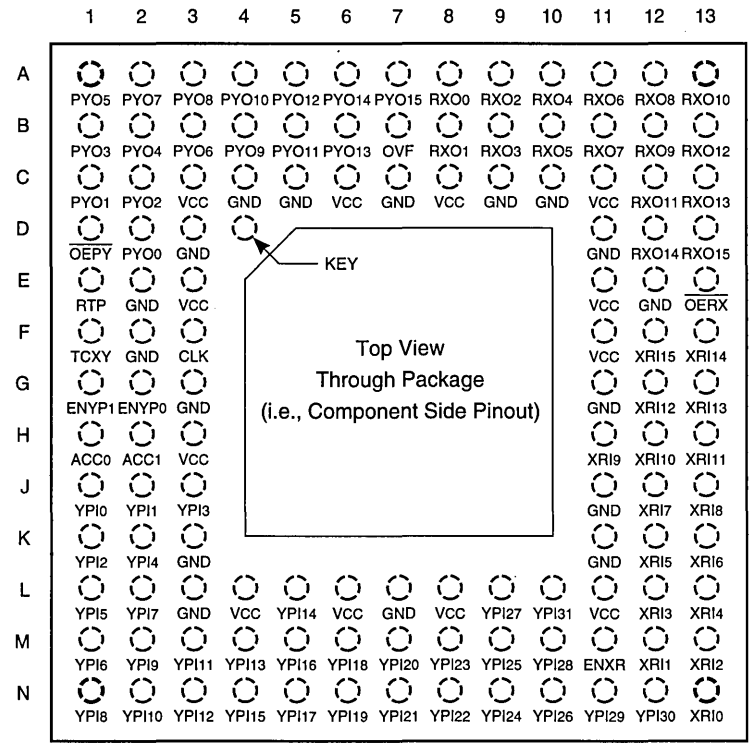


Speed	Plastic Quad Flatpack (Q1)
	0°C to +70°C—COMMERCIAL SCREENING
50 ns	L2330QC50
25 ns	L2330QC25
20 ns	L2330QC20

3

ORDERING INFORMATION

120-pin



Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C—Commercial Screening
50 ns	L2330GC50
25 ns	L2330GC25
20 ns	L2330GC20
	–55°C to +125°C—Commercial Screening
50 ns	L2330GM50
25 ns	L2330GM25
20 ns	L2330GM20
	–55°C to +125°C—MIL-STD-883 Compliant
50 ns	L2330GMB50
25 ns	L2330GMB25
20 ns	L2330GMB20

L2340
Digital Synthesizer

FEATURES

- Digital Waveform Synthesis at 50 MHz
- 24-Bit Polar Phase Angle Accuracy
- User-selectable Waveform Synthesis, Frequency Modulation, or Phase Modulation.
- Amplitude Input for Amplitude Modulation and Gain Adjustment.
- Replaces Raytheon TMC2340A
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 120-pin Plastic Quad Flatpack
  - 120-pin Ceramic PGA

DESCRIPTION

The **L2340** is a digital synthesizer that performs waveform synthesis, modulation, and demodulation.

The L2340 automatically generates quadrature matched pairs of 16-bit sine and cosine waves in DAC-compatible 16-bit offset binary format with15-bit amplitude and 32-bit phase inputs.

Output waveforms can be phase or frequency modulated. Digital output frequencies are restricted to the Nyquist limit.

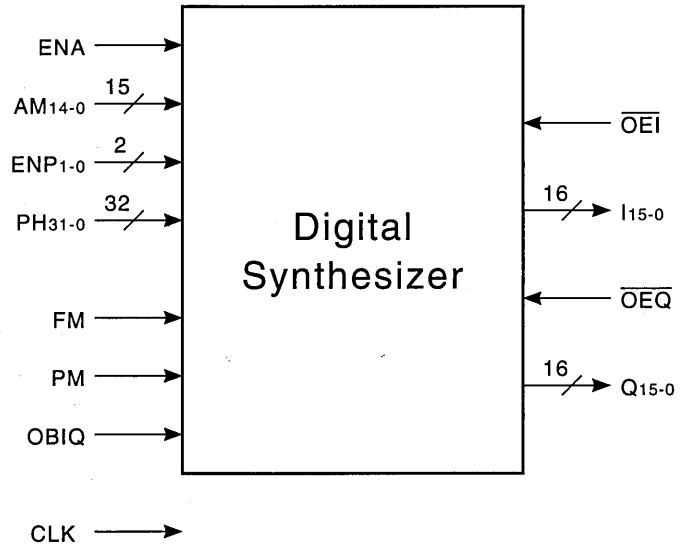
Functional Description

The L2340 converts Polar (Phase and Magnitude) data into Rectangular (Cartesian) coordinates. The user selects the numeric format. A valid transformed result is seen at the output after 22 clock cycles and will continue upon every clock cycle thereafter.

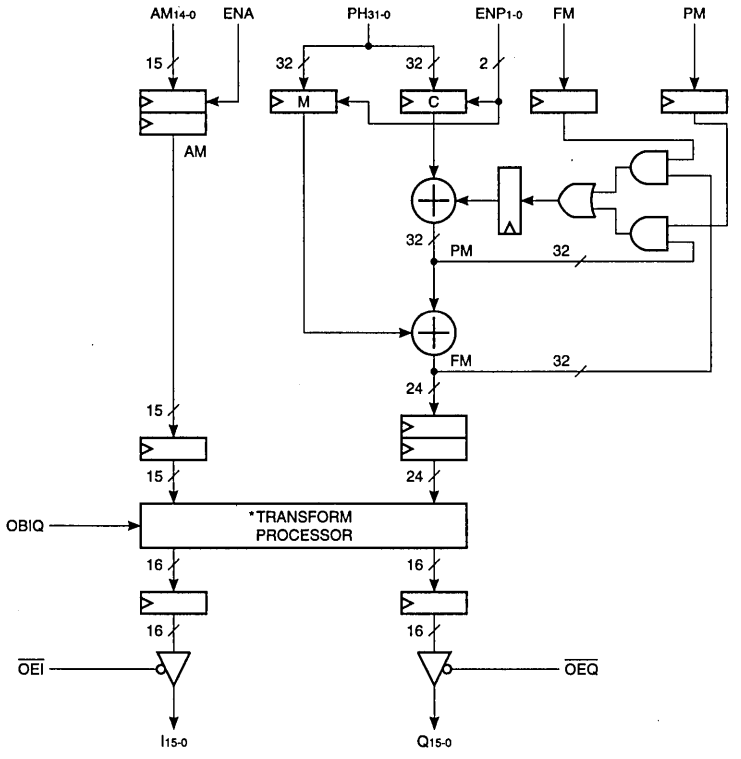
15-bit amplitude and 32-bit phase data are input into the L2340 to produce an output of 16-bit rectangular data. The user may select the data format to either 16-bit offset binary or 15-bit unsigned magnitude format. High accuracy phase increment values with minimal accumulation error is accomplished by use of a 32-bit phase accumulator.

The phase accumulator structure supports frequency or phase modulation and is selected by ENP1-0 and accumulator controls FM and PM.

L2340 BLOCK DIAGRAM



L2340 Functional Block Diagram



*REQUIRES 18 CYCLES TO COMPLETE AND IS FULLY PIPELINED

SIGNAL DEFINITIONS

Power

Vcc and GND

+5V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers.

Inputs

AM14-0 — Amplitude Modulation Data Input

AM14-0 is the 15-bit Amplitude Modulation Data input port. AM14-0 is latched on the rising edge of CLK.

PH31-0 — Phase Angle Data Input

PH31-0 is the 32-bit Phase Angle Data input port. Input phase accumulators are loaded through this port into registers enabled by ENP1-0. PH31-0 is latched on the rising edge of CLK.

Outputs

I15-0 — x-coordinate Data Output

I15-0 is the 16-bit Cartesian x-coordinate Data output port. When $\overline{OEI}$ is HIGH, I15-0 is forced into the high-impedance state. I15 is forced HIGH if OBIQ is LOW.

Q15-0 — y-coordinate Data Output

Q15-0 is the 16-bit Cartesian y-coordinate Data output port. When $\overline{OEQ}$ is HIGH, Q15-0 is forced into the high-impedance state. Q15 is forced HIGH if OBIQ is LOW.

Controls

ENA — Amplitude Modulation Data Input Enable

When ENA is HIGH, AM is latched into the input register on the rising edge of clock. When ENA is LOW, the value stored in the register is unchanged.

ENP1-0 — Phase Modulation Data Input Control

ENP1-0 is the 2-bit Phase Modulation Data Input Control that determines one of the four modes shown in Table 1. 'M' is the Modulation Register and 'C' is the Carrier Register as shown in the Functional Block Diagram.

Table 1. Register Operation

ENP1-0	Configuration
0 0	No registers enabled, current data held
0 1	M register input enabled, C data held
1 0	C register input enabled, M data held
1 1	M register = 0, C register input enabled

Table 2. Accumulator Control

FM	PM	Configuration
0	0	No accumulation (normal operation)
0	1	PM accumulator path enabled
1	0	FM accumulator path enabled
1	1	Logical OR of PM and FM (Nonsensical)

FM, PM — Frequency Modulation, Phase Modulation Control

FM and PM is the 2-bit Frequency Modulation/Phase Modulation Control that determines one of the four modes shown in Table 2. When full-scale is exceeded, the accumulator will roll over correctly allowing continuous phase accumulation through 2π radians.

OBIQ — Data Input/Output Format Select

When OBIQ is HIGH, offset binary format is selected. When OBIQ is LOW, unsigned format is selected.

$\overline{OEI}$ — x-coordinate Data Output Enable

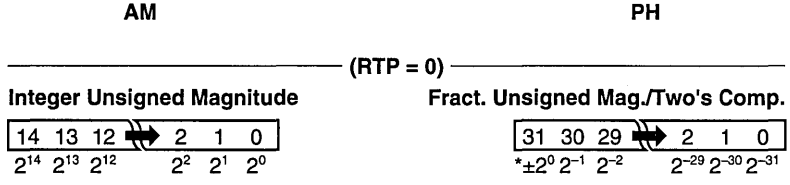
When $\overline{OEI}$ is LOW, I_{15-0} is enabled for data output. When $\overline{OEI}$ is HIGH, I_{15-0} is placed in a high-impedance state.

$\overline{OEQ}$ — y-coordinate Data Output Enable

When $\overline{OEQ}$ is LOW, Q_{15-0} is enabled for data output. When $\overline{OEQ}$ is HIGH, Q_{15-0} is placed in a high-impedance state.

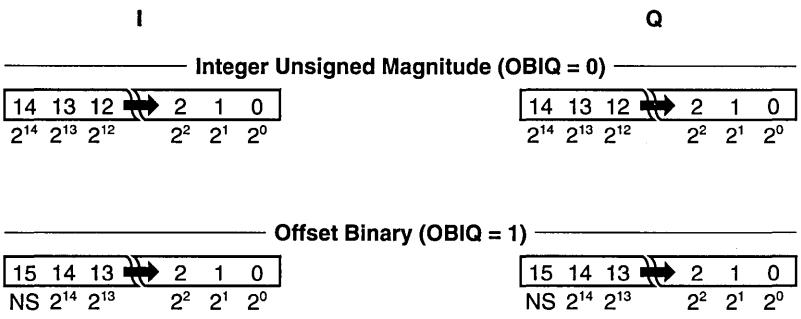
3

FIGURE 1A. INPUT FORMATS



*$\pm 2^0$ denotes two's complement sign or highest magnitude bit. Since phase angles are modulo 2π and phase accumulator is modulo 2^{32}, this bit may be regarded as $\pm\pi$.

FIGURE 1B. OUTPUT FORMATS



NS denotes negative sign. (i.e. '1' negates the number)

Circle Test

When performing a coordinate transformation, inaccuracies are introduced by a combination of quantization and approximation errors. The accuracy of a coordinate transformer is dependent on the word length used for the input variables, the word length used for internal calculations, as well as the number of iterations or steps performed. Truncation errors are due to the finite word length and approximation errors are due to the finite number of iterations. For example, in the case of performing a polar-to-rectangular transformation, the accuracy of the rotation will be determined by how closely the input rotation angle was approximated by the summation of sub-rotation angles.

In this study, we compare how accurately a coordinate transformer with a 16-bit internal processor versus a 24-bit internal processor can calculate all the coordinates of a circle. By setting the radius to 7FFFH, θ is incremented using the accumulator of the L2340 in steps of 0000 4000H until all the points of a full circle are calculated into rectangular coordinates.

The resulting rectangular coordinates were plotted and graphed. A graphical representation of the resulting vectors for both 16-bit and 24-bit internal processors are compared at 45°. Theoretically, a perfect circle is the desired output but when the resulting vectors from a coordinate transformer with 16-bit internal processor are graphed and displayed as shown in Figure 2, we see significant errors due to the inherent properties of a digital synthesizer. In comparison, the 24-bit internal processor proves to be significantly more accurate than a 16-bit internal processor due to minimization of truncation errors. In many applications, this margin of error will introduce noise when performing waveform sythesis, modulation, and demodulation.

Data values for Figure 2 and Figure 3 are shown in Table 3. By looking at these values, we observe the step resolution on a 16-bit internal processor is not 1 unit in the x and y. In most cases, the minimum step resolution is 2 units in the x and y. On the other hand, step resolution on a 24-bit internal processor is 1 unit in the x and y thus resulting in greater accuracy.

The minimum theoretical angle resolution that could be produced is 0.00175° when x = 7FFFH and y = 1H. A 16-bit internal processor can produce a minimum angle resolution of only 0.00549° and will not be able to properly calculate the theoretical minimum angle resolution. On the other hand, a 24-bit internal processor can produce a minimum angle resolution of 0.00002° and could therefore properly calculate the theoretical minimum angle resolution.

FIGURE 2. CIRCLE TEST RESULT NEAR 45° (16-BIT INTERNAL PROCESSOR)

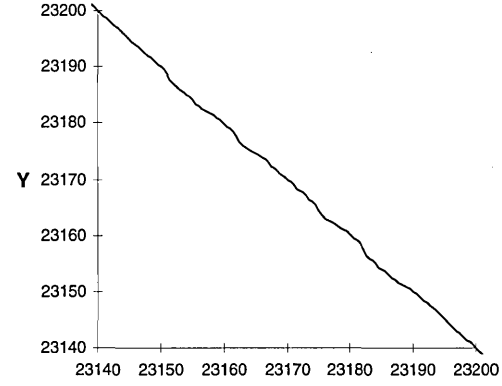


FIGURE 3. CIRCLE TEST RESULT NEAR 45° (24-BIT INTERNAL PROCESSOR)

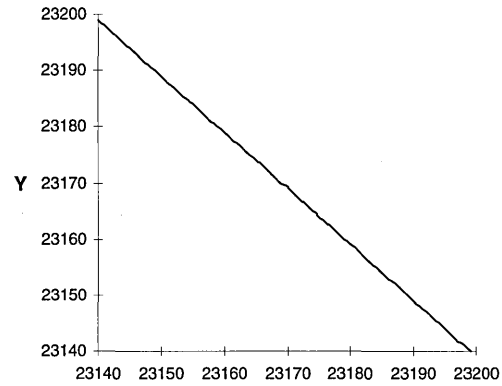


TABLE 3. RESULTANT DATA VALUES OF CIRCLE TEST NEAR 45°

16-bit Internal Processor				24-bit Internal Processor			
x	x (HEX)	y	y (HEX)	x	x (HEX)	y	y (HEX)
23201	5AA1	23139	5A63	23199	5A9F	23140	5A64
23199	5A9F	23141	5A65	23198	5A9E	23141	5A65
23199	5A9F	23141	5A65	23198	5A9E	23141	5A65
23199	5A9F	23141	5A65	23197	5A9D	23142	5A66
23199	5A9F	23141	5A65	23197	5A9D	23142	5A66
23197	5A9D	23143	5A67	23196	5A9C	23143	5A67
23197	5A9D	23143	5A67	23196	5A9C	23143	5A67
23197	5A9D	23143	5A67	23195	5A9B	23144	5A68
23197	5A9D	23143	5A67	23194	5A9A	23145	5A69
23195	5A9B	23145	5A69	23194	5A9A	23145	5A69
23195	5A9B	23145	5A69	23194	5A9A	23145	5A69
23195	5A9B	23145	5A69	23193	5A99	23146	5A6A
23195	5A9B	23145	5A69	23192	5A98	23147	5A6B
23192	5A98	23148	5A6C	23191	5A97	23148	5A6C
23192	5A98	03148	5A6C	23191	5A97	23148	5A6C
23192	5A98	23148	5A6C	23191	5A97	23148	5A6C
23192	5A98	23148	5A6C	23190	5A96	23149	5A6D
23190	5A96	23150	5A6E	23189	5A95	23150	5A6E
23190	5A96	23150	5A6E	23189	5A95	23150	5A6E
23190	5A96	23150	5A6E	23189	5A95	23150	5A6E
23190	5A96	23150	5A6E	23188	5A94	23151	5A6F
23187	5A93	23152	5A70	23187	5A93	23152	5A70
23187	5A93	23152	5A70	23186	5A92	23153	5A71
23187	5A93	23152	5A70	23186	5A92	23153	5A71
23187	5A93	23152	5A70	23186	5A92	23153	5A71
23185	5A91	23154	5A72	23185	5A91	23154	5A72
23185	5A91	23154	5A72	23184	5A90	23155	5A73
23185	5A91	23154	5A72	23184	5A90	23155	5A73
23185	5A91	23154	5A72	23184	5A90	23155	5A73
23183	5A8F	23156	5A74	23183	5A8F	23156	5A74

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			95	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			5	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

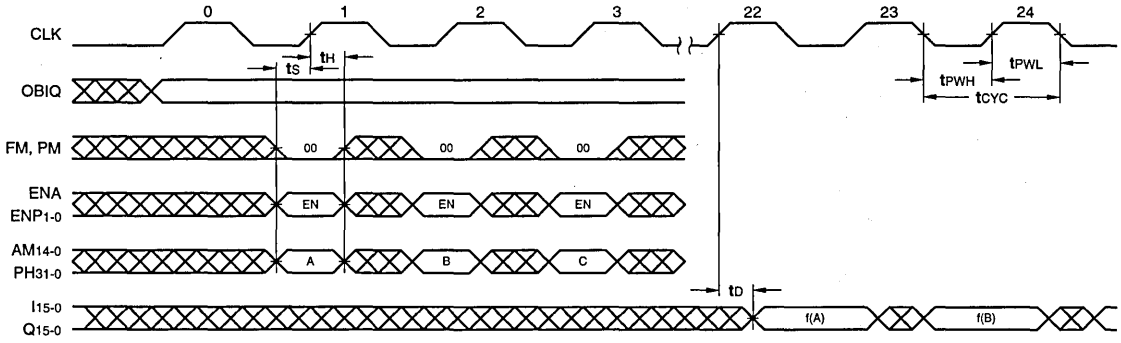
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L2340–					
		50		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20	
t_{PWL}	Clock Pulse Width Low	10		8		7	
t_{PWH}	Clock Pulse Width High	8		7		6	
t_S	Input Setup Time	12		7		6	
t_H	Input Hold Time	1		0		0	
t_D	Output Delay		22		18		16
t_{ENA}	Three-State Output Enable Delay (Note 11)		13		13		13
t_{DIS}	Three-State Output Disable Delay (Note 11)		13		13		13

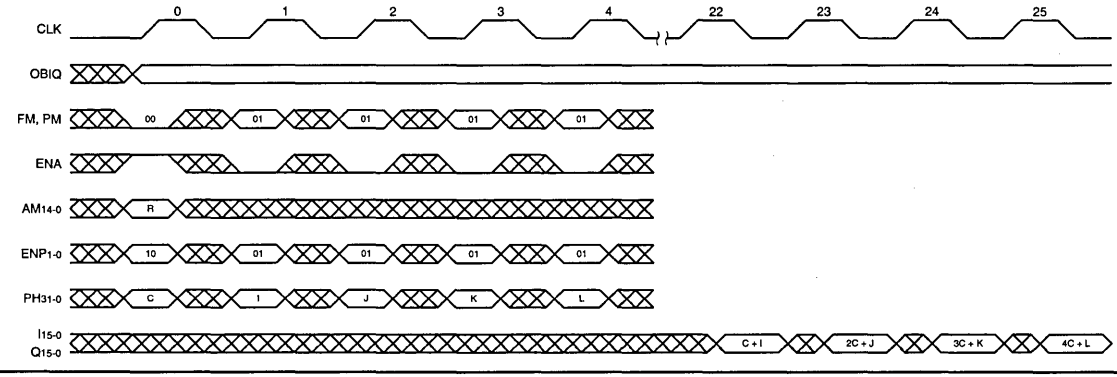
MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L2340–					
		50		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20	
t_{PWL}	Clock Pulse Width Low	11		9		7	
t_{PWH}	Clock Pulse Width High	8		7		6	
t_S	Input Setup Time	13		7		6	
t_H	Input Hold Time	2		2		1	
t_D	Output Delay		25		20		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		14		13
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		14		13

SWITCHING WAVEFORMS: NO ACCUMULATION



SWITCHING WAVEFORMS: PHASE MODULATION



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

3

FIGURE A. OUTPUT LOADING CIRCUIT

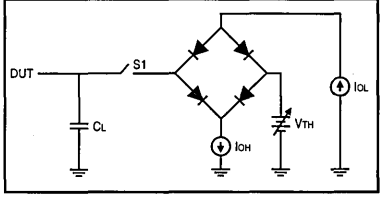
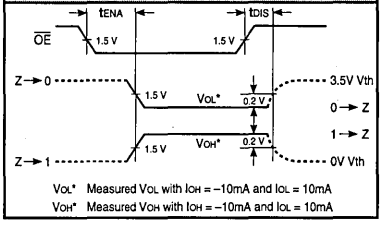
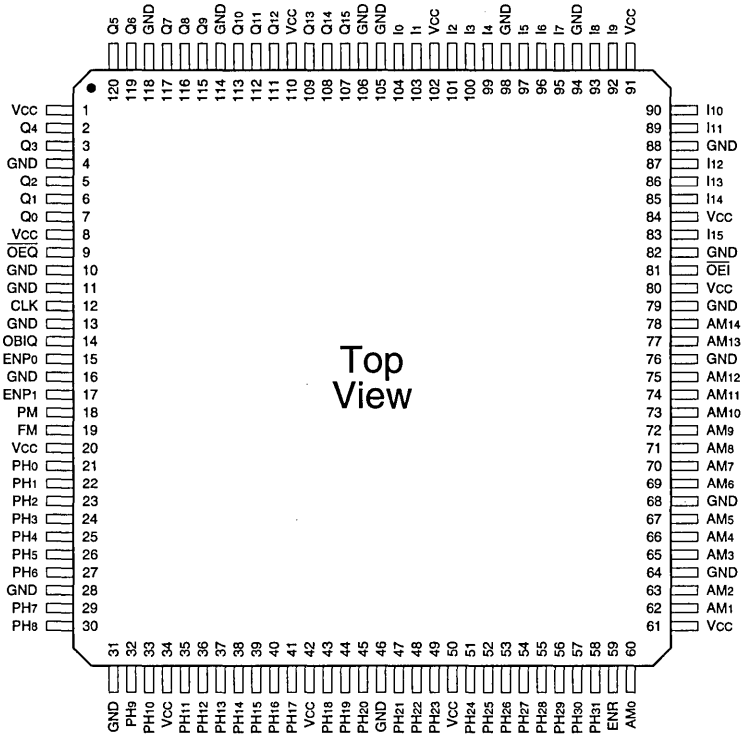


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

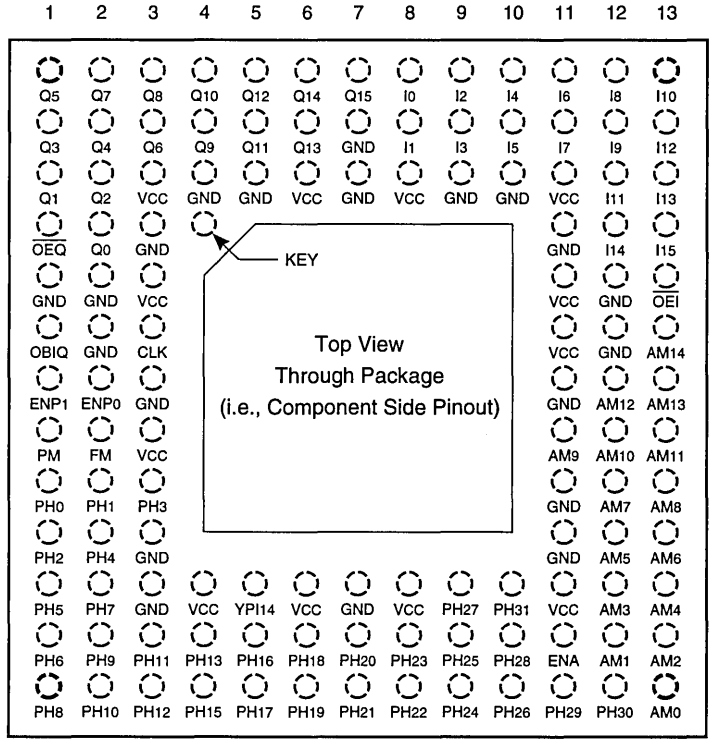
120-pin



Speed	Plastic Quad Flatpack (Q1)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	L2340QC50
25 ns	L2340QC25
20 ns	L2340QC20

ORDERING INFORMATION

120-pin



Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C—Commercial Screening
50 ns	L2340GC50
25 ns	L2340GC25
20 ns	L2340GC20
	–55°C to +125°C—Commercial Screening
50 ns	L2340GM50
25 ns	L2340GM25
20 ns	L2340GM20
	–55°C to +125°C—MIL-STD-883 Compliant
50 ns	L2340GMB50
25 ns	L2340GMB25
20 ns	L2340GMB20

L64230
Template Matcher

FEATURES

- 40MHz Data and Computation Rate
- 1024-tap High-Speed Digital Transversal Filter and Template Matcher
- Variable Window Sizes: 1 x 1024, 2 x 512, 4 x 256, 8 x 128, 16 x 64, and 32 x 32
- Processor Cascadability can be Implemented for Extended Data / Coefficient Precision, Increased Filter-Tap Power, and Increased Window Sizes
- DECC SMD No. 5962-90504
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 132-pin Ceramic Flatpack
  - 144-pin Plastic Quad Flatpack

DESCRIPTION

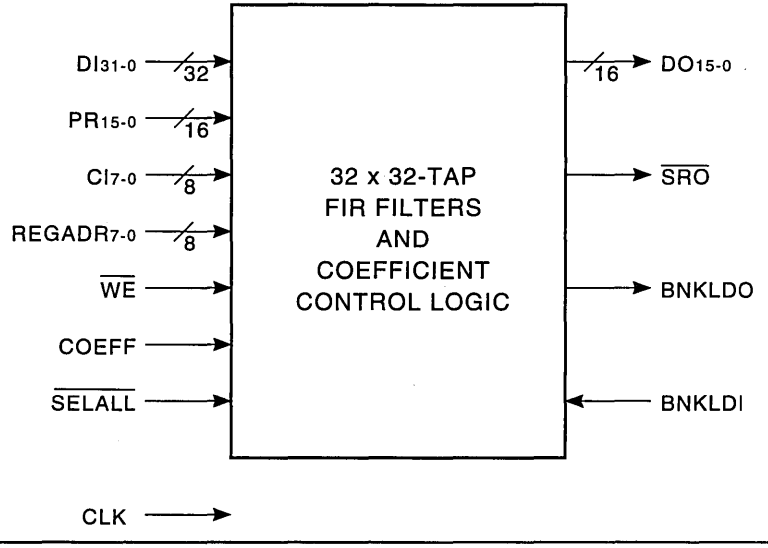
The **L64230** is a high-speed, 1024-tap Digital Filter and Template Matcher. The device can be configured as a 1-D (one-dimensional) filter used in such applications as radar, sonar, or other forms of signal processing. The L64230 can also be implemented in 2-D (two-dimensional) applications, such as real-time image processing such as: pattern matching, correlation, convolution, noise elimination, morphing, dilation and erosion.

The L64230 is arranged as 32 (total) 32-tap filters with the outputs of each of the filters being summed and then delayed by the variable-length shift registers. In a multiprocessor system, this delayed output is then summed with the incoming partial result to form the complete output. In addition to carrying in the partial result into the L64230, the input can be used to vary the threshold when clipping the output to a single bit.

Each filter performs the basic XNOR and AND logic operations. The Ai, j and Bi, j are stored in double buffered registers. Bi, j controls the XNOR gate while the Ai, j controls the AND gate. The XNOR gate performs inversion (erosion) or magnitude differencing (template matching). The AND gate performs masking (template matching) or 1-bit multiplication (FIR filtering, dilation erosion). The outputs of all taps are summed to produce the final result. It should be noted that no significant bits of any signal are lost.

The L64230 has 32 single-bit inputs (DI_{31-0}). For 1-D filtering, the only active input is DI_0. However, when performing 2-D operations over a window of size N x M, N of the inputs are active. A video shift register, with a raster scanned signal as its input would provide the N active data inputs.

L64230 Block Diagram



SIGNAL DEFINITIONS

Power

Vcc and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

DI31-0 — Data Input

When the L64230 is implemented in a 1-D filtering application, only pin DI0 is used. Pins, DI31-1 are left disconnected. However, in a 2-D filtering application with a window size of 32 x 32, the L64230 operates with all 32 data inputs active.

CI7-0 — Coefficient/Control Input

Eight control bits or four sets of coefficients (both Ai, j and Bi, j) are loaded into the master section of the coefficient/control registers. CI7 is the MSB.

PR15-0 — Partial Result Input

The partial result is summed with the processor results to provide the final data output. In a multiprocessor system, DO31-0 outputs of the preceding L64230 are connected to the corresponding partial result input. The partial results can be used in varying the threshold of the output, like clipping the output to a single bit. Disconnected PR pins are automatically assigned a LOW value. PR15 is the MSB.

BNKLDI — Bank Load Input

In order to bank load coefficients/control inputs from master to slave registers, set BNKLDI to HIGH. When asynchronously loading coefficients/control inputs, BNKLDI is held LOW until bank loading occurs. When coefficient/control input loading is performed synchronously, BNKLDI is always held HIGH.

REGADR7-0 — Coefficient/Control Register Address Inputs

Controls the master register location that will be loaded with the coefficient/control inputs. Loading occurs only when WE is LOW. REGADR7 is the MSB.

Outputs

DO15-0 — Data Output

The value of the output is the sum of delayed output of the 1024 taps and the partial result (PR15-0). DO15 is the MSB.

$\overline{SRO}$ — Shift Register Output

In a 1-D filter application, $\overline{SRO}$ is the DI0 input delayed by 1025 cycles and inverted. This signal is usually connected to the DI0 of the next L64230 in a 1-D, multiprocessor system. $\overline{SRO}$ is not used in 2-D processing.

BNKLDO — Bank Load Output

BNKLDO is the BNKLDI signal delayed by one CLK cycle. BNKLDO was designed to be used in a 1-D multiprocessor system as input for BNKLDI in the next L64230.

Controls

$\overline{SELALL}$ — Coefficient Register Select-All

When LOW, $\overline{SELALL}$ enables the loading of the values at CI7-0 into the master latches of all 256, 4-tap groups in the processor simultaneously. This quickly initializes the L64230. When HIGH, $\overline{SELALL}$ enables the loading of the values into the master latches found at the locations determined by COEFF and REGADR7-0.

$\overline{WE}$ — Write Enable

When $\overline{WE}$ is held LOW, the coefficient/control signals are loaded into the register location indicated by COEFF and REGADR7-0.

COEFF — Coefficient Input Indicator

The data on the CI bus is interpreted as coefficient data when COEFF is held HIGH. When COEFF is held LOW, data is interpreted as control inputs. (See Table 1, the Processor Control/Coefficient Memory Map, for more detail.)

OPERATION

L64230 operation is fairly straightforward. After the internal master registers have been loaded with the data indicating the operating mode, the user need only supply a system/data clock and the input data. Once the L64230 is setup and running, some or all of the coefficients (the set of Ai, j and Bi, j) can be changed while the processor is operating.

CONTROL SIGNALS

As mentioned in the previous paragraph, the operation of the L64230 is simple. However, both the initialization of the processor and loading of the Control/Coefficient Data will prove to be a bit more interesting.

To initialize the processor and all the coefficients, the delay value of the variable delay element and the configuration must be specified. The Processor Control/Coefficient Memory Map (Table 1) gives more detail as to the memory map of L64230.

If $\overline{\text{SELALL}}$ is HIGH, only one of the eight Control/Coefficient bits will be latched each time WE goes LOW. When $\overline{\text{SELALL}}$ is pulsed LOW, all 1024 A_i, B_i coefficients will be loaded as shown ($\overline{\text{WE}}$ can be HIGH or LOW). However, the $\overline{\text{MUXCON}}$ and $\overline{\text{OUTDEL}}$ values will change only when $\overline{\text{WE}}$ is LOW.

$\text{OUTDEL}_{4\text{-}0}$ variable set the number of delays performed by the variable delay element. The Window Configurations (Table 2) displays the various window shapes and corresponding active data inputs for the most common window configurations. Other configurations can be obtained.

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Table 1. Processor Control/Coefficient Memory Map

Coeff	$\text{REGADR}_{7\text{-}0}$	CI_7	CI_6	CI_5	CI_4	CI_3	CI_2	CI_1	CI_0
0	0	X	X	X	$\overline{\text{MUXCON}}_4$	$\overline{\text{MUXCON}}_3$	$\overline{\text{MUXCON}}_2$	$\overline{\text{MUXCON}}_1$	$\overline{\text{MUXCON}}_0$
0	1	X	X	X	X	OUTDEL_3	OUTDEL_2	OUTDEL_1	OUTDEL_0
1	0	$B_{0,3}$	$A_{0,3}$	$B_{0,2}$	$A_{0,2}$	$B_{0,1}$	$A_{0,1}$	$B_{0,0}$	$A_{0,0}$
1	1	$B_{0,7}$	$A_{0,7}$	$B_{0,6}$	$A_{0,6}$	$B_{0,5}$	$A_{0,5}$	$B_{0,4}$	$A_{0,4}$
1	2	$B_{0,11}$	$A_{0,11}$	$B_{0,10}$	$A_{0,10}$	$B_{0,9}$	$A_{0,9}$	$B_{0,8}$	$A_{0,8}$
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	7	$B_{0,31}$	$A_{0,31}$	$B_{0,30}$	$A_{0,30}$	$B_{0,29}$	$A_{0,29}$	$B_{0,28}$	$A_{0,28}$
1	8	$B_{1,3}$	$A_{1,3}$	$B_{1,2}$	$A_{1,2}$	$B_{1,1}$	$A_{1,1}$	$B_{1,0}$	$A_{1,0}$
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	15	$B_{1,31}$	$A_{1,31}$	$B_{1,30}$	$A_{1,30}$	$B_{1,29}$	$A_{1,29}$	$B_{1,28}$	$A_{1,28}$
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	247	$B_{30,31}$	$A_{30,31}$	$B_{30,30}$	$A_{30,30}$	$B_{30,29}$	$A_{30,29}$	$B_{30,28}$	$A_{30,28}$
1	248	$B_{31,3}$	$A_{31,3}$	$B_{31,2}$	$A_{31,2}$	$B_{31,1}$	$A_{31,1}$	$B_{31,0}$	$A_{31,0}$
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	255	$B_{31,31}$	$A_{31,31}$	$B_{31,30}$	$A_{31,30}$	$B_{31,29}$	$A_{31,29}$	$B_{31,28}$	$A_{31,28}$

Table 2. Window Configurations

$\text{MUXCON}_{4\text{-}0}$	Configuration	Active Inputs
11111	1 x 1024	DI_0
11110	2 x 512	DI_0, DI_{16}
11100	4 x 256	DI_0, DI_8, DI_{16}, DI_{24}
11000	8 x 128	DI_0, DI_4, DI_8, DI_{12}, DI_{16}, DI_{20}, DI_{24}, DI_{28}
10000	16 x 16	DI_0, DI_2, DI_4, DI_6, DI_8, DI_{10}, DI_{12}, DI_{14}, DI_{16}, DI_{18}, DI_{20}, DI_{22}, DI_{24}, DI_{26}, DI_{28},DI_{30}
00000	32 x 32	All

FUNCTIONAL OVERVIEW

The L64230 is designed to perform FIR Filtering, Template Matching and Morphological Operations over a variety of window sizes. Figure 1 shows the two basic functions performed by the L64230.

Figure 1.

$$1D{:}y(n) = PR(n-1) + \sum_{1023}^{i=0} [(B_i \text{ XNOR } DI_0(n-i-DLY-3)) \text{ AND } \overline{A_i}]$$

$$2D{:}y(n) = PR(n-1) + \sum_{i=0}^{31}\sum_{j=0}^{31} [(B_{i,j} \text{ XNOR } DI_i(n-j-DLY-3)) \text{ AND } \overline{A_{i,j}}]$$

For these equations, all DIi, Ai, j, and Bi, j are one bit wide. Depending upon the application the L64230 is being used in, the control variables: Ai, j and Bi, j can be set appropriately to implement one of the four previously mentioned functions. For FIR Filtering, Bi, j = 1 and Ai, j is the inverted impulse response. For the application of Template Matching, Bi, j is the template and Ai, j is the "don't care" mask. Erosion is implemented by setting Bi, j = 0 and Ai, j as the inverted structuring element. Dilation is setup much the same way as FIR Filtering, with the exception being that the multi-bit output is clipped to a single bit. In addition, for all functions it is possible to reduce the effective window size by masking some elements within the window by setting Ai, j=1 (refer to Table 2). DLY is the value of the variable length output delay, controlled by OUTDEL4-0. The preceding functions are outlined in Table 3.

COEFFICIENT/CONTROL SIGNAL LOADING METHODS

Coefficients and control signals are double-buffered by master and slave registers. To load a new coefficient or control signal, the data must first be placed on the CI bus. The data is then latched into the the master register designated by REGADR7-0 and COEFF, when $\overline{WE}$ is LOW. An alternative method to loading the master registers with coefficient data individually, is to hold SELALL LOW. This makes it possible to quickly initialize the processor by simultaneously loading all the coefficient registers with the data loaded on the CI bus. Now that the master registers are loaded, the user is given three different choices as to how to transfer the data from the master latches into the slave or active latches.

METHOD I

The first method is to load the coefficient or control signal to the master latch asynchronously (in reference to CLK), then transfer the data to the slave latch synchronously. Once all 256 master latches have been loaded (implementing either of methods mentioned in the above paragraph), the coefficients can be made active simultaneously by enabling the slave latches, when both BNKLDI and CLK are HIGH. This method extends to the user, the ability to update the coefficient sets into the processor without modifying the active set of coefficients.

METHOD II

The second method involves both the loading and transferring of the coefficients synchronously. This can be done by simply tying BNKLDI HIGH. $\overline{WE}$ is then pulsed low when CLK is LOW. During this time, a new coefficient on the CI bus is loaded into the master latch, again determined by REGADR7-0 and COEFF. On the next rising edge of CLK, the coefficient is transferred to the slave latch, thus becoming the active coefficient or control signal. In this way, a new coefficient can replace the current one within one clock cycle. This can be done only with slower clock speed, with cycle time 80ns (COM) or more.

METHOD III

The third method is to asynchronously load and transfer over several cycles the new coefficients . If it is not convenient to supply BNKLDI or $\overline{WE}$ signals synchronous to CLK, this technique is used. BNKLDI can be tied HIGH and $\overline{WE}$ operated asynchronously. In this case every time a new coefficient is loaded, the processor output could be invalid for up to 20 cycles after the rising edge of $\overline{WE}$. The processor could be invalid for up to 1050 cycles after the rising edge of $\overline{WE}$ if control signals (COEFF = 0) are loaded.

Table 3. Functional Summary

Functions	Ai, j	Bi, j	PR	Output
FIR Filter	Inverted Impulse Response	1	0	DO is the Filter Output
Template Matching	"Don't Care" Mask	Template	0	DO Represents Correlation to Template
Erosion	Inverted Structuring Element	0	-1	DO15 is Output
Dilation	Inverted Structuring Element	1	-1	DO15 is Inverted Output

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –3.2 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 3.2 mA			0.4	V
V_{IH}	Input High Voltage		2.25		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±200	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			300	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			10	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			15	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			20	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF64230					
		85		50		25*	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
tCYC	Cycle Time	85		50		25	
tPWH	Clock Pulse Width HIGH	25		20		10	
tPWL	Clock Pulse Width LOW	25		20		10	
tDIS	Input Data Setup Time	20		15		10	
tDIH	Input Data Hold Time	7		5		2	
tOUT	Output Delay of DO		20		15		15
tOD	Output Delay of $\overline{SRO}$ and BNKLDO		20		15		15
tRS	REGADR to $\overline{WE}$ LOW Setup Time	15		10		10	
tRH	REGADR to $\overline{WE}$ HIGH Hold Time	15		10		0	
tCS	CI to $\overline{WE}$ LOW Setup Time	15		10		10	
tCH	CI to $\overline{WE}$ HIGH Hold Time	15		10		0	
tWW	$\overline{WE}$ Pulse Width LOW	25		20		10	
tWC	$\overline{WE}$ Cycle Time	65		50		25	
tCSS	CI to $\overline{SELALL}$ LOW Setup Time	150		100		50	
tCHS	CI to $\overline{SELALL}$ HIGH Hold Time	150		100		50	
tWS	$\overline{SELALL}$ Pulse Width LOW	150		100		50	
tSC	$\overline{SELALL}$ Cycle Time	350		250		100	
tLS	BNKLDI Setup Time	20		15		10	
tLH	BNKLDI Hold Time	7		5		0	
tWL	$\overline{WE}$ to BNKLDI HIGH Setup Time	7		5		5	
tLW	$\overline{WE}$ to BNKLDI LOW Hold Time	tPWH+20		tPWH+15		tPWH+10	
tSSB	$\overline{SELALL}$ to BNKLDI HIGH Setup Time	150		100		50	
tHSB	$\overline{SELALL}$ to BNKLDI LOW Hold Time	150		100		50	
tCLW	CLK LOW before $\overline{WE}$ LOW	25		20		15	
tWCL	CLK HIGH after $\overline{WE}$ HIGH	25		20		15	
tPRS	Input Partial Result Setup Time	40		30		20	
tPRH	Input Partial Result Hold Time	7		5		20	

***Advanced Information**

SWITCHING CHARACTERISTICS

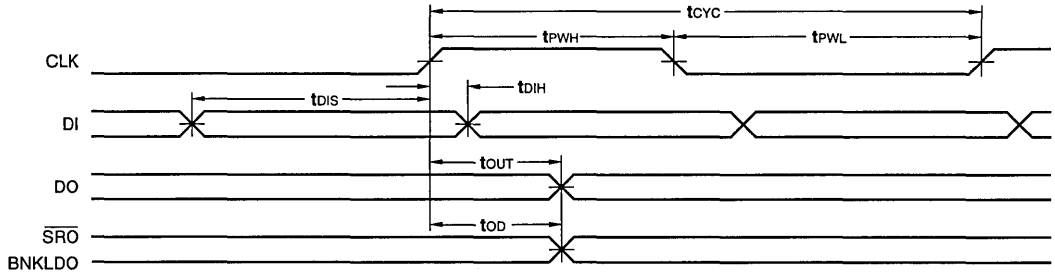
MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF64230					
		75		60		45*	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	75		60		45	
t_{PWH}	Clock Pulse Width HIGH	30		25		15	
t_{PWL}	Clock Pulse Width LOW	30		25		15	
t_{DIS}	Input Data Setup Time	25		20		15	
t_{DIH}	Input Data Hold Time	15		7		5	
t_{OUT}	Output Delay of DO		25		20		20
t_{OD}	Output Delay of $\overline{SRO}$ and BNKLDO		25		20		20
t_{RS}	REGADR to $\overline{WE}$ LOW Setup Time	20		15		15	
t_{RH}	REGADR to $\overline{WE}$ HIGH Hold Time	20		15		5	
t_{CS}	CI to $\overline{WE}$ LOW Setup Time	20		15		15	
t_{CH}	CI to $\overline{WE}$ HIGH Hold Time	20		15		5	
t_{WW}	$\overline{WE}$ Pulse Width LOW	30		25		15	
t_{WC}	$\overline{WE}$ Cycle Time	75		60		45	
t_{CSS}	CI to $\overline{SELALL}$ LOW Setup Time	200		150		50	
t_{CHS}	CI to $\overline{SELALL}$ HIGH Hold Time	200		150		50	
t_{WS}	$\overline{SELALL}$ Pulse Width LOW	200		150		50	
t_{SC}	$\overline{SELALL}$ Cycle Time	400		300		100	
t_{LS}	BNKLDI Setup Time	25		20		15	
t_{LH}	BNKLDI Hold Time	15		7		5	
t_{WL}	$\overline{WE}$ to BNKLDI HIGH Setup Time	15		7		5	
t_{LW}	$\overline{WE}$ to BNKLDI LOW Hold Time	t_{PWH}+25		t_{PWH}+20		t_{PWH}+20	
t_{SSB}	$\overline{SELALL}$ to BNKLDI HIGH Setup Time	200		150		50	
t_{HSB}	$\overline{SELALL}$ to BNKLDI LOW Hold Time	200		150		50	
t_{CLW}	CLK LOW before $\overline{WE}$ LOW	30		25		20	
t_{WCL}	CLK HIGH after $\overline{WE}$ HIGH	30		25		20	
t_{PRS}	Input Partial Result Setup Time	50		40		25	
t_{PRH}	Input Partial Result Hold Time	15		7		5	

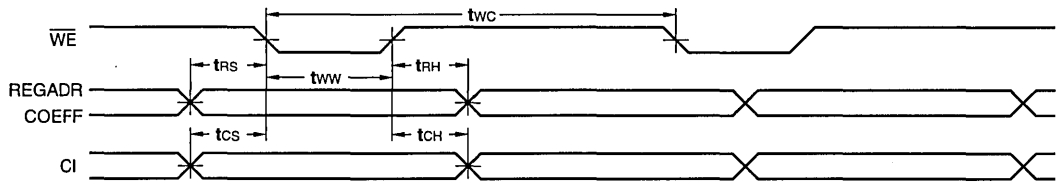
3

***Advanced Information**

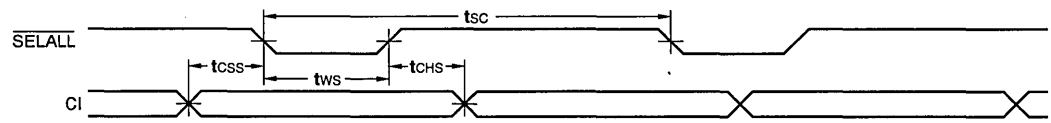
Switching Waveforms: Normal Filter Operation



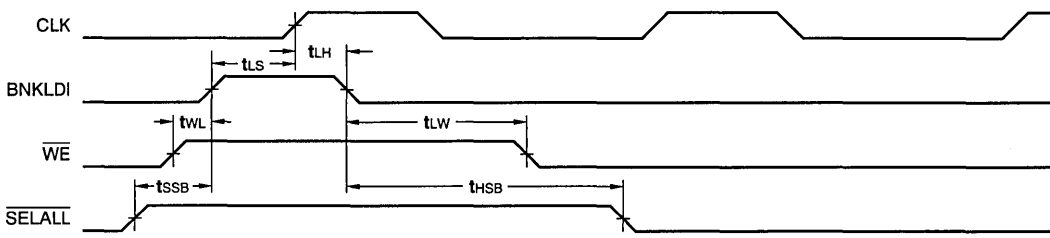
Switching Waveforms: Loading Controls into Master Registers Using WE (SELALL HIGH)



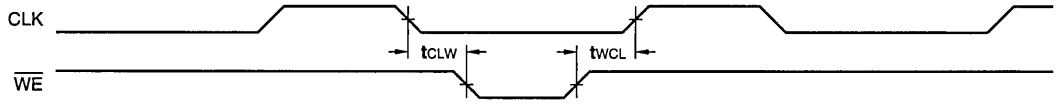
Switching Waveforms: Loading Controls into Master Registers Using SELALL (WE HIGH)



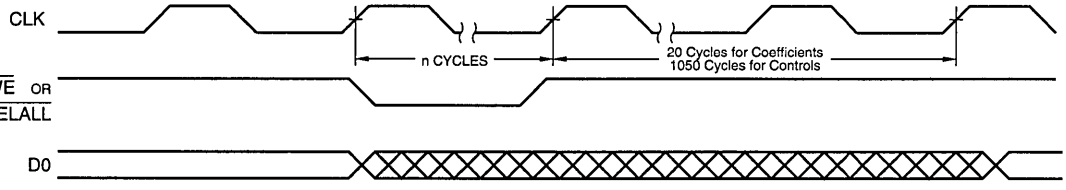
Switching Waveforms: Coefficient/Control Signal Loading (Method I)



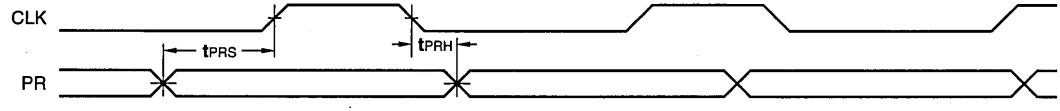
Switching Waveforms: Coefficient/Control Signal Loading (Method II)



Switching Waveforms: Coefficient/Control Signal Loading (Method III)



Switching Waveforms: Partial Result Input Timing



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 10 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

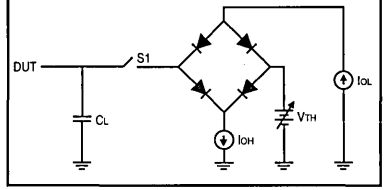
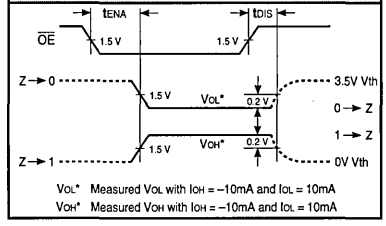
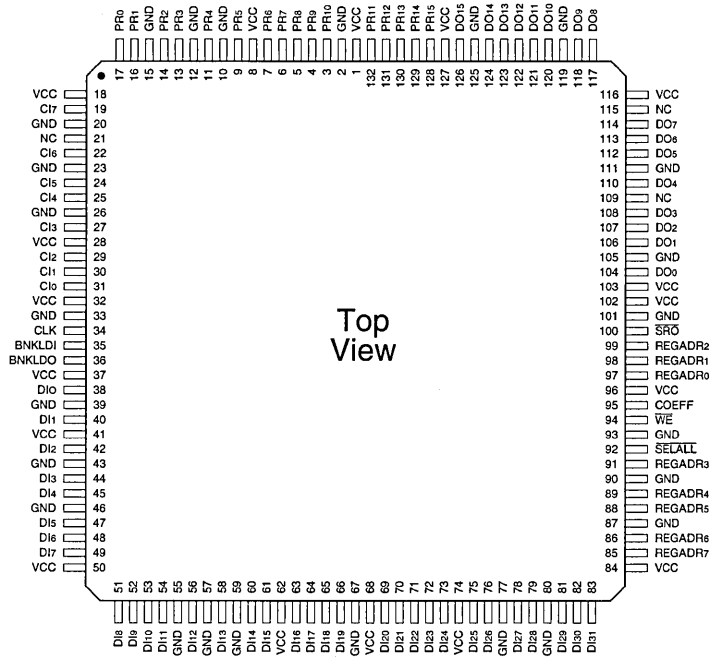


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

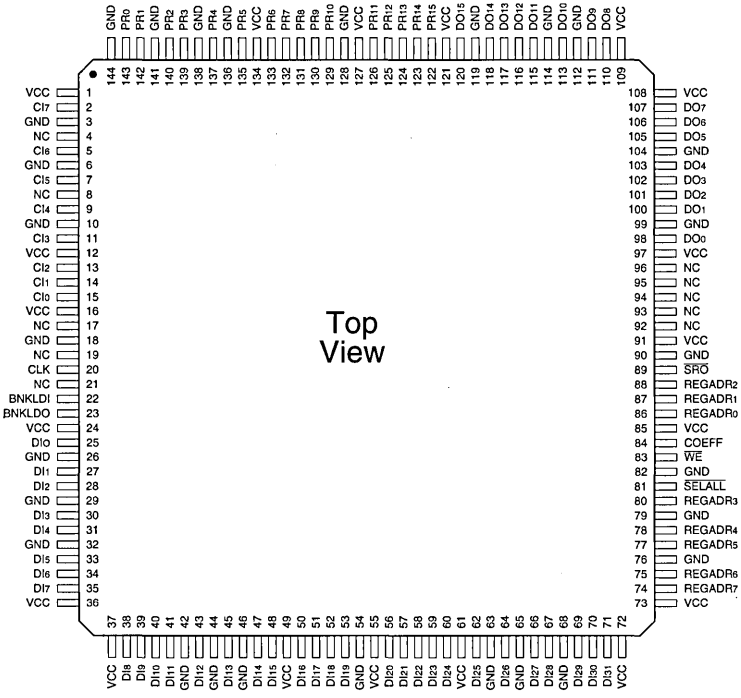
132-pin



Speed	Ceramic Flatpack (F5)
	0°C to +70°C—COMMERCIAL SCREENING
	–55°C to +125°C—COMMERCIAL SCREENING
	–55°C to +125°C—MIL-STD-883 COMPLIANT
75 ns	LF64230FMB75
60 ns	LF64230FMB60
45 ns	LF64230FMB45

ORDERING INFORMATION

144-pin



Speed	Plastic Quad Flatpack (Q5)
	0°C to +70°C — COMMERCIAL SCREENING
85 ns	L64230QC85
50 ns	L64230QC50
25 ns	L64230QC25

Multipliers & Multiplier-Accumulators

4

LMU08/8U
8 x 8-bit Parallel Multiplier

FEATURES

- 20 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- LMU08 Replaces TRW TMC208K
- LMU8U Replaces TRW TMC28KU
- Two's Complement (LMU08), or Unsigned Operands (LMU8U)
- Three-State Outputs
- DECC SMD No. 5962-88739
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 40-pin Plastic DIP
  - 40-pin Ceramic DIP
  - 44-pin Plastic LCC, J-Lead
  - 44-pin Ceramic LCC

DESCRIPTION

The **LMU08** and **LMU8U** are high-speed, low power 8-bit parallel multipliers. They are pin-for-pin equivalents with TRW TMC208K and TMC28KU type multipliers. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

Both the LMU08 and the LMU8U produce the 16-bit product of two 8-bit numbers. The LMU08 accepts operands in two's complement format, and produces a two's complement result. The product is provided in two halves with the sign bit replicated as the most significant bit of both halves. This facilitates use of the LMU08 product as a double precision operand in 8-bit systems. The LMU8U operates on unsigned data, producing an unsigned magnitude result.

Both the LMU08 and the LMU8U feature independently controlled registers for both inputs and the product, which along with three-state outputs allows easy interfacing with microprocessor busses. Provision is made in the LMU08 and LMU8U for proper rounding of the product to 8-bit precision. The round input is loaded at the rising edge of the logical OR of CLK A and CLK B for the LMU08. The LMU8U latches RND on the rising edge of CLK A only. In either case, a '1' is added in the most significant position of the lower product byte when RND is asserted. Subsequent truncation of the least significant product byte results in a correctly rounded 8-bit result.

4

LMU08/8U Block Diagram

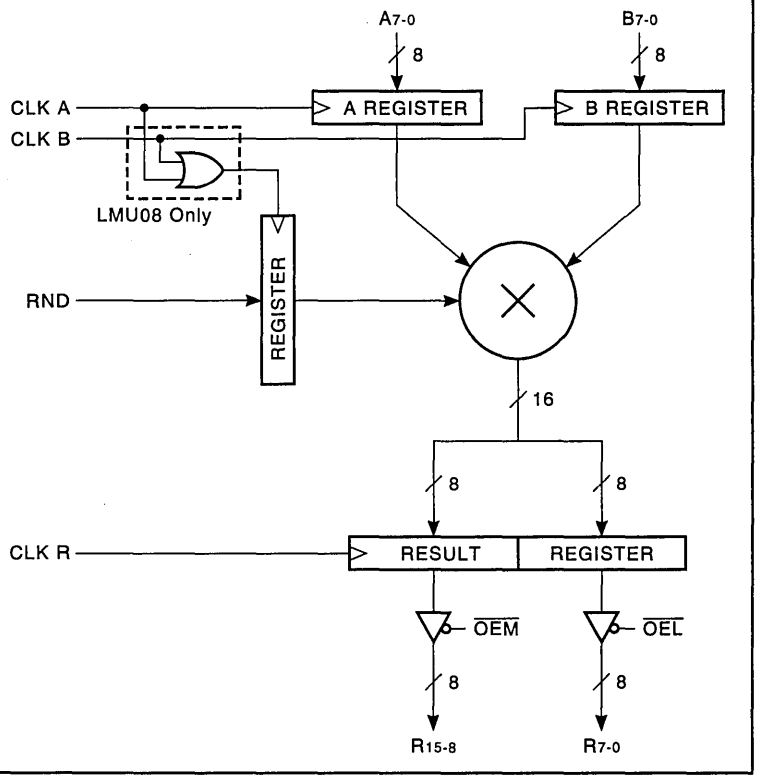


FIGURE 1A. INPUT FORMATS

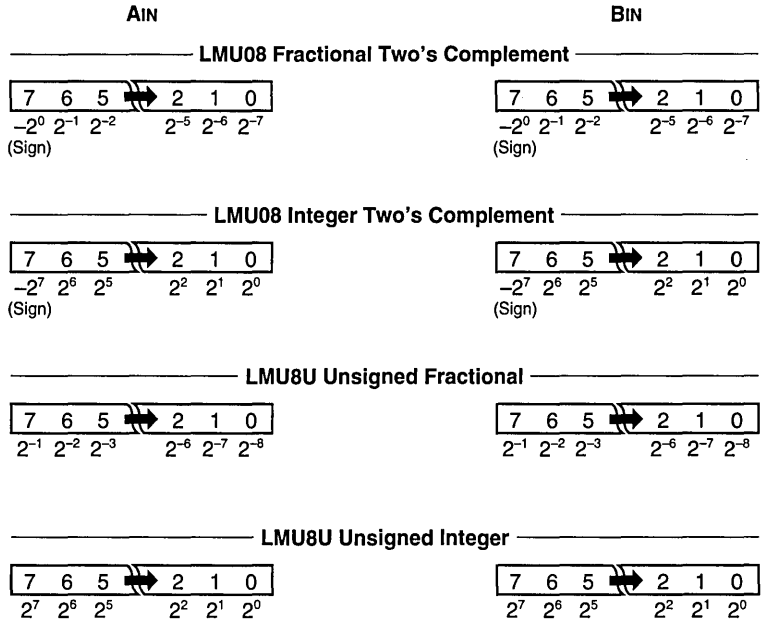
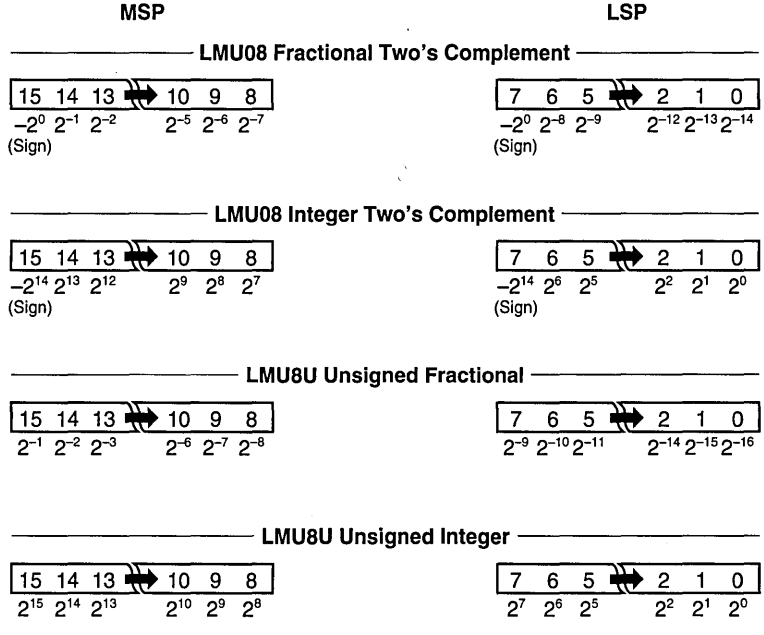


FIGURE 1B. OUTPUT FORMATS



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		8	24	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

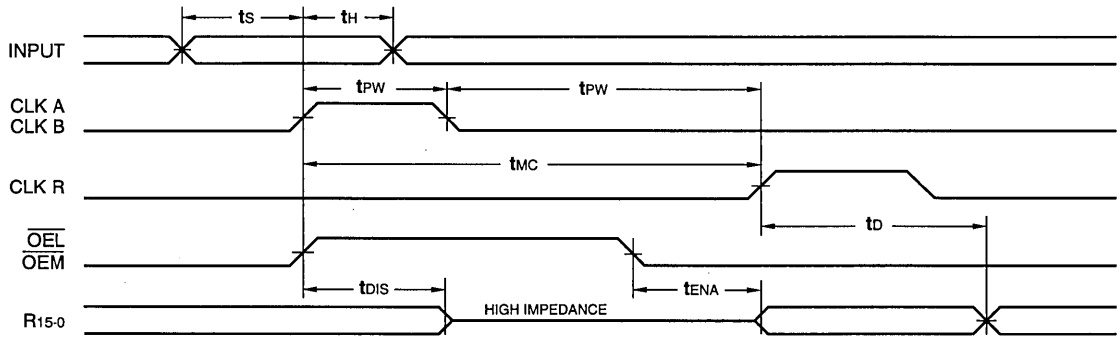
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU08/8U–							
		70		50		35		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		70		50		35		20
t_{PW}	Clock Pulse Width	20		20		10		8	
t_S	Input Register Setup Time	14		14		14		10	
t_H	Input Register Hold Time	4		0		0		0	
t_D	Output Delay		25		20		20		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		24		22		22		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		22		20		20		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU08/8U–							
		90		60		45		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		90		60		45		25
t_{PW}	Clock Pulse Width	25		20		15		10	
t_S	Input Register Setup Time	20		15		15		15	
t_H	Input Register Hold Time	5		2		2		2	
t_D	Output Delay		35		22		22		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		35		24		24		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		35		22		22		20

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

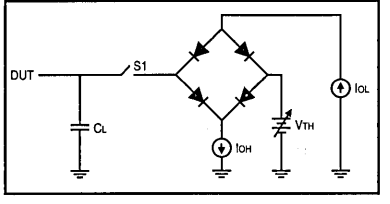
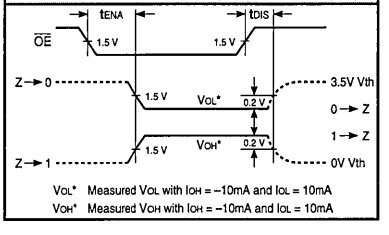


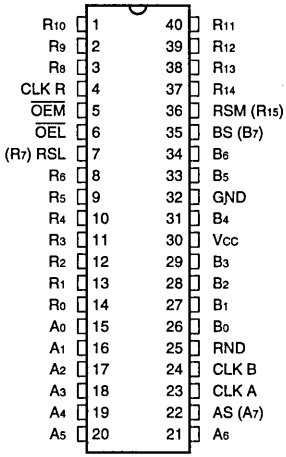
FIGURE B. THRESHOLD LEVELS



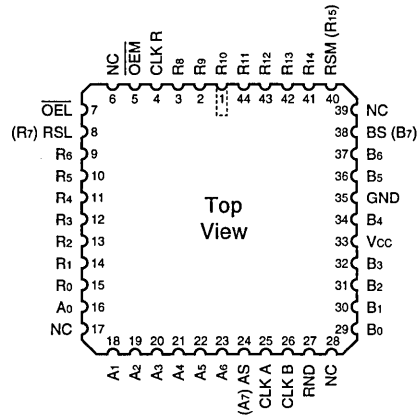
4

LMU08 — ORDERING INFORMATION

40-pin — 0.6" wide



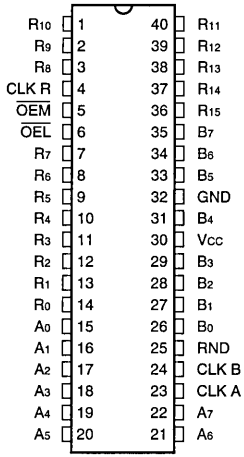
44-pin



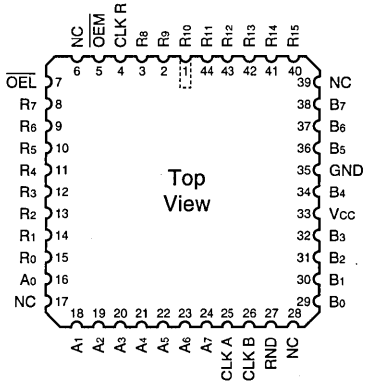
Speed	Plastic DIP (P3)	Ceramic DIP (C11)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — COMMERCIAL SCREENING			
70 ns	LMU08PC70		LMU08JC70	
50 ns	LMU08PC50		LMU08JC50	
35 ns	LMU08PC35		LMU08JC35	
20 ns	LMU08PC20		LMU08JC20	
	–55°C to +125°C — COMMERCIAL SCREENING			
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
90 ns		LMU08CMB90		LMU08KMB90
60 ns		LMU08CMB60		LMU08KMB60
45 ns		LMU08CMB45		LMU08KMB45
25 ns		LMU08CMB25		LMU08KMB25

LMU8U — ORDERING INFORMATION

40-pin — 0.6" wide



44-pin



Speed	Plastic DIP (P3)	Ceramic DIP (C11)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — COMMERCIAL SCREENING			
70 ns	LMU8UPC70		LMU8UJC70	
50 ns	LMU8UPC50		LMU8UJC50	
35 ns	LMU8UPC35		LMU8UJC35	
20 ns	LMU8UPC20		LMU8UJC20	
	–55°C to +125°C — COMMERCIAL SCREENING			
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
90 ns		LMU8UCMB90		LMU8UKMB90
60 ns		LMU8UCMB60		LMU8UKMB60
45 ns		LMU8UCMB45		LMU8UKMB45
25 ns		LMU8UCMB25		LMU8UKMB25

4

LMU12
12 x 12-bit Parallel Multiplier

FEATURES

- 20 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces TRW MPY012H
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Ceramic PGA

DESCRIPTION

The **LMU12** is a high-speed, low power 12-bit parallel multiplier. It is pin and functionally compatible with TRW MPY012H devices. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The LMU12 produces the 24-bit product of two 12-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control bit are similarly loaded by CLK B.

The TCA and TCB controls specify the A and B operands as two's complement when HIGH, or unsigned magnitude when LOW.

RND is loaded on the rising edge of the logical OR of CLK A and CLK B. RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 12 least significant bits produces a result correctly rounded to 12-bit precision.

At the output, the Right Shift control (RS) selects either of two output formats. RS LOW produces a 23-bit product with a copy of the sign bit inserted in the MSB position of the least significant half. RS HIGH gives a full 24-bit product. Two 12-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK M and CLK L respectively. For asynchronous output, these registers may be made transparent by setting the feed through control (FT) HIGH.

LMU12 Block Diagram

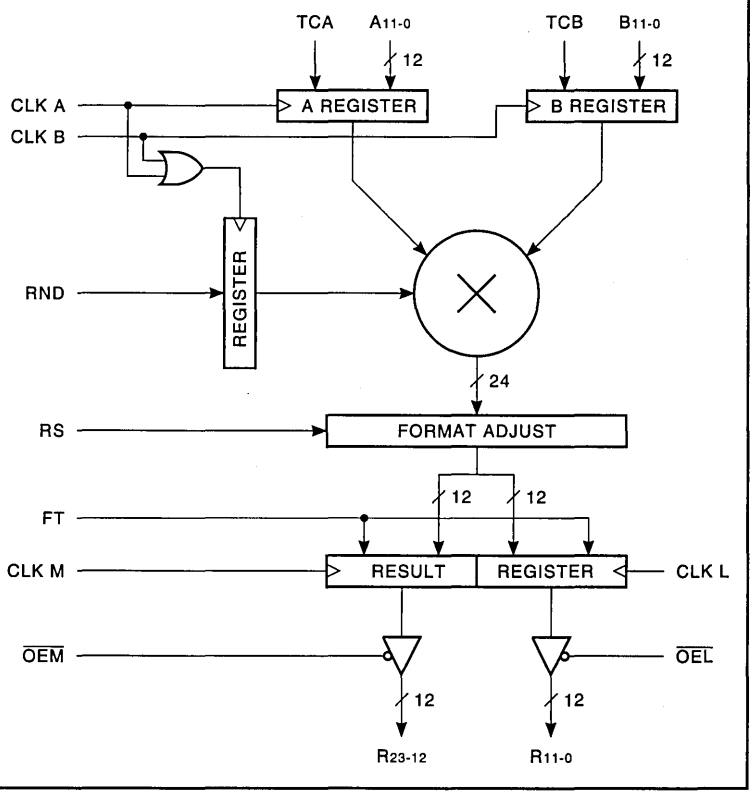


FIGURE 1A. INPUT FORMATS

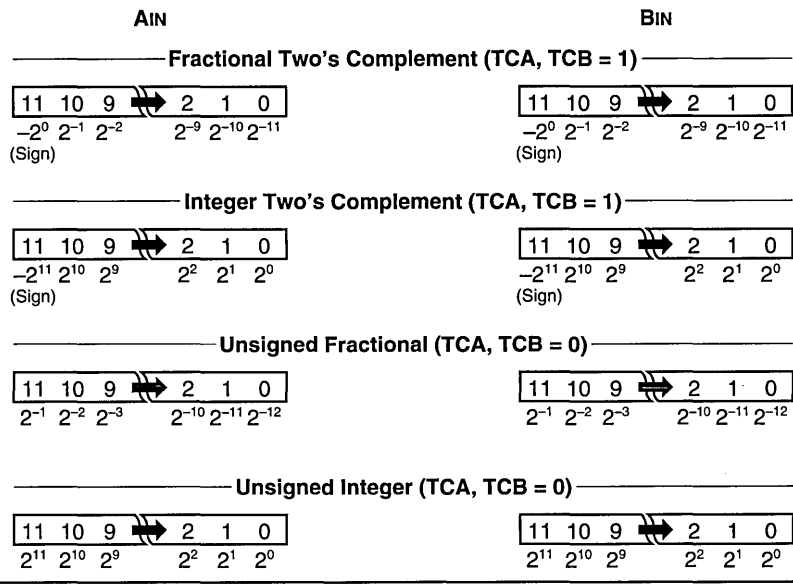
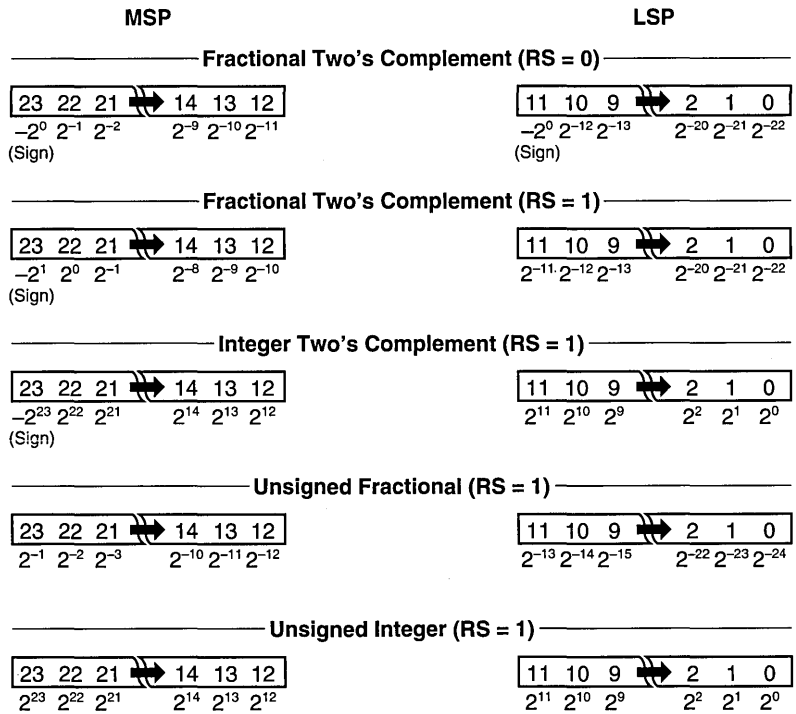


FIGURE 1B. OUTPUT FORMATS



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		17	35	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

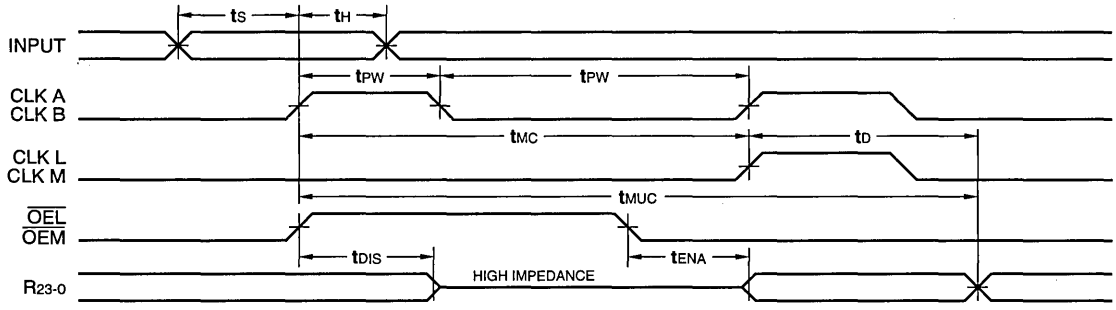
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU12–							
		65		45		35		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		65		45		35		20
t_{MUC}	Unclocked Multiply Time		95		65		55		40
t_{PW}	Clock Pulse Width	25		15		15		8	
t_S	Input Register Setup Time	18		15		12		10	
t_H	Input Register Hold Time	2		2		2		0	
t_D	Output Delay		26		25		25		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		22		22		20		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		20		18		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU12–							
		75		55		45		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		75		55		45		25
t_{MUC}	Unclocked Multiply Time		110		75		65		45
t_{PW}	Clock Pulse Width	25		20		15		10	
t_S	Input Register Setup Time	18		15		15		12	
t_H	Input Register Hold Time	2		2		2		2	
t_D	Output Delay		30		30		25		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		26		26		24		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		24		24		22		20

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

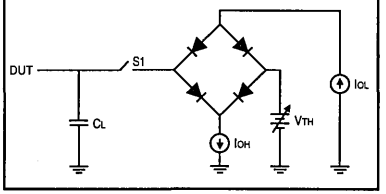
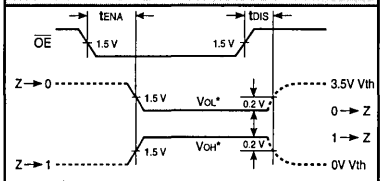


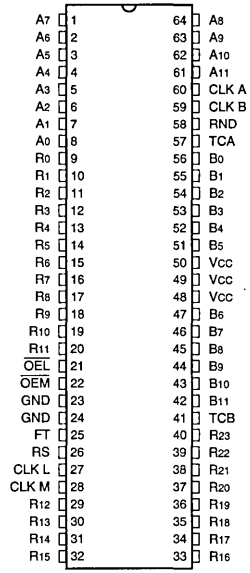
FIGURE B. THRESHOLD LEVELS



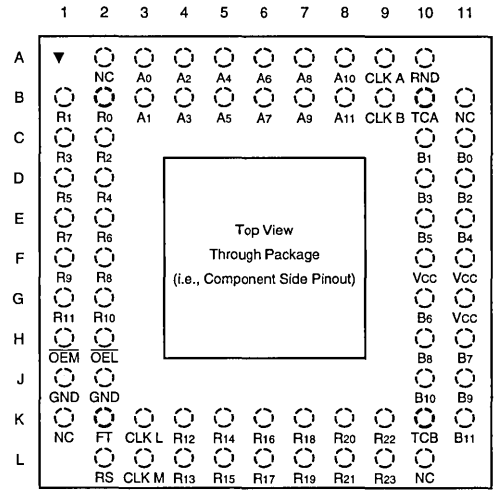
4

ORDERING INFORMATION

64-pin



68-pin



*** 64-pin DIP not recommended for new designs**

Speed	Sidebraze Hermetic DIP (D6)	Ceramic Pin Grid Array (G2)
	0°C to +70°C — Commercial Screening	
65 ns	LMU12DC65	LMU12GC65
45 ns	LMU12DC45	LMU12GC45
35 ns	LMU12DC35	LMU12GC35
20 ns		LMU12GC20
	–55°C to +125°C — Commercial Screening	
75 ns	LMU12DM75	LMU12GM75
55 ns	LMU12DM55	LMU12GM55
45 ns	LMU12DM35	LMU12GM45
25 ns		LMU12GM25
	–55°C to +125°C — MIL-STD-883 Compliant	
75 ns	LMU12DMB75	LMU12GMB75
55 ns	LMU12DMB55	LMU12GMB55
45 ns	LMU12DMB35	LMU12GMB45
25 ns		LMU12GMB25

LMU112
12 x 12-bit Parallel Multiplier

FEATURES

- 25 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces TRW MPY112K
- Two's Complement or Unsigned Operands
- Three-State Outputs
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 48-pin Plastic DIP
  - 48-pin Sidebraze, Hermetic DIP
  - 52-pin Plastic LCC, J-Lead

DESCRIPTION

The **LMU112** is a high-speed, low power 12-bit parallel multiplier built using advanced CMOS technology. The LMU112 is pin and functionally compatible with TRW's MPY112K.

The A and B input operands are loaded into their respective registers on the rising edge of the separate clock inputs (CLK A and CLK B). Two's complement or unsigned magnitude operands are accommodated via the operand control bit (TC) which is loaded along with the B operands. The operands are specified to be in two's complement format when TC is asserted and unsigned magnitude when TC is deasserted. Mixed mode operation is not allowed.

For two's complement operands, the 17 most significant bits at the output of the asynchronous multiplier array are shifted one bit position to the left. This is done to discard the redundant copy of the sign-bit, which is in the most significant bit position, and extend the bit precision by one bit. The result is then truncated to the 16 MSB's and loaded into the output register on the rising edge of CLK B.

The contents of the output register are made available via three-state buffers by asserting $\overline{OE}$. When $\overline{OE}$ is de-asserted, the outputs (R_{23-8}) are in the high impedance state.

4

LMU112 Block Diagram

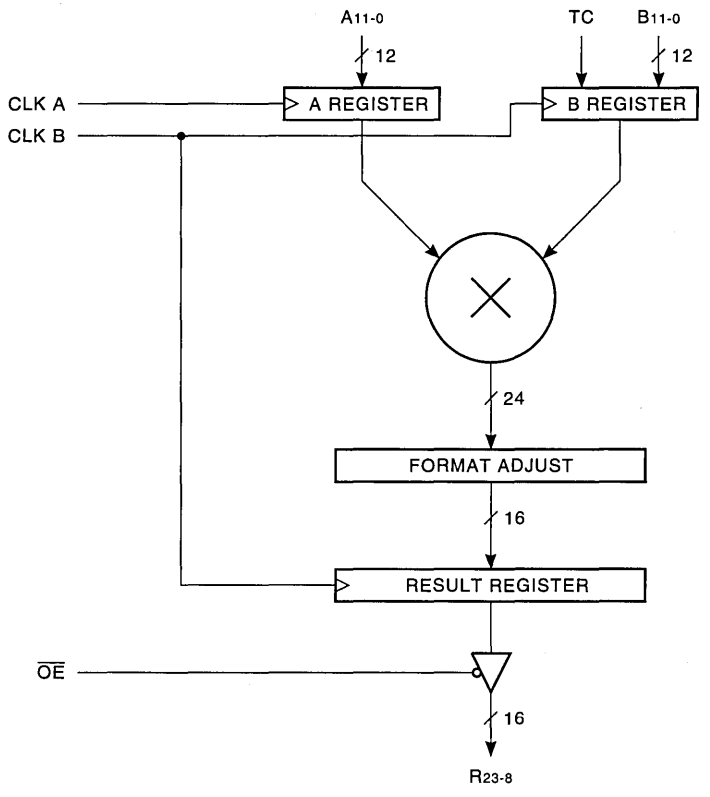


FIGURE 1A. INPUT FORMATS

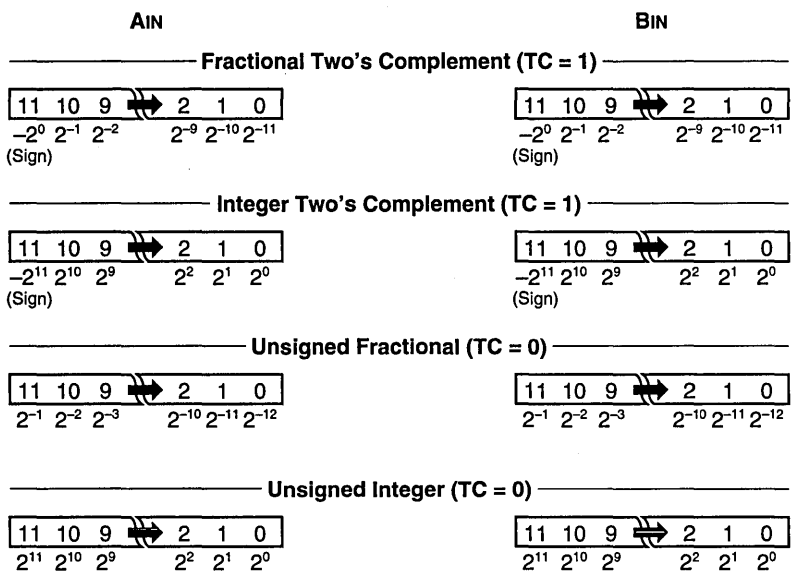
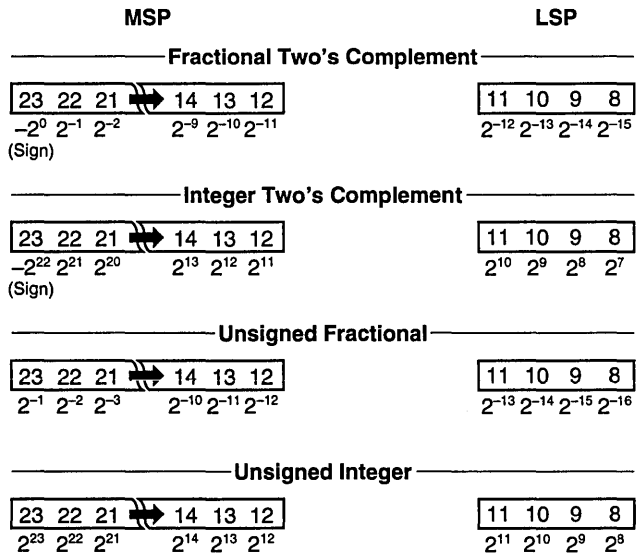


FIGURE 1B. OUTPUT FORMATS



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	20	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

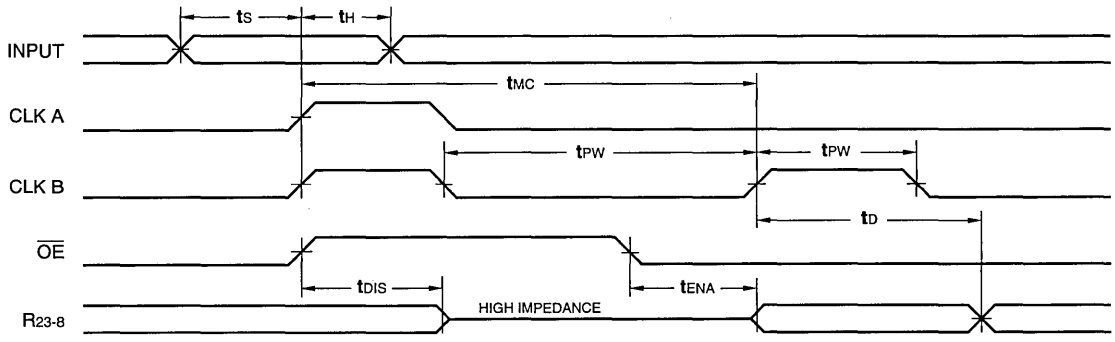
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU112–					
		60		50		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		60		50		25
t_{PW}	Clock Pulse Width	15		15		10	
t_S	Input Register Setup Time	15		15		10	
t_H	Input Register Hold Time	3		3		1	
t_D	Output Delay		25		25		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		25		20

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU112–					
		65		55		30	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		65		55		30
t_{PW}	Clock Pulse Width	20		20		12	
t_S	Input Register Setup Time	15		15		12	
t_H	Input Register Hold Time	3		3		3	
t_D	Output Delay		30		30		25
t_{ENA}	Three-State Output Enable Delay (Note 11)		30		30		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		30		30		25

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

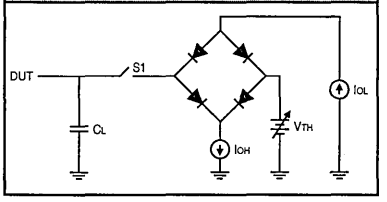
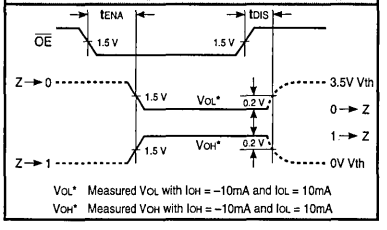
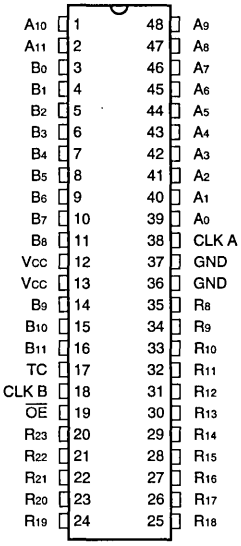


FIGURE B. THRESHOLD LEVELS

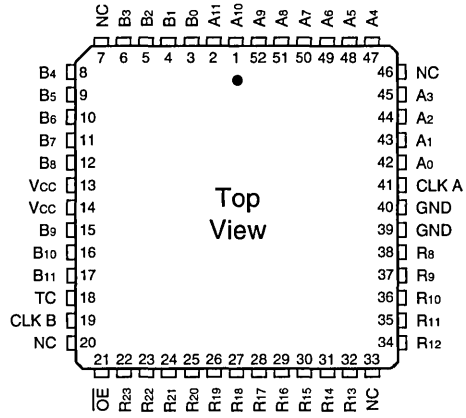


ORDERING INFORMATION

48-pin



52-pin



Speed	Plastic DIP (P5)	Sidebraze Hermetic DIP (D5)	Plastic J-Lead Chip Carrier (J5)
	0°C to +70°C — Commercial Screening		
60 ns	LMU112PC60	LMU112DC60	LMU112JC60
50 ns	LMU112PC50	LMU112DC50	LMU112JC50
25 ns	LMU112PC25	LMU112DC25	LMU112JC25
	–55°C to +125°C — Commercial Screening		
65 ns		LMU112DM65	
55 ns		LMU112DM55	
30 ns		LMU112DM30	
	–55°C to +125°C — MIL-STD-883 Compliant		
65 ns		LMU112DMB65	
55 ns		LMU112DMB55	
30 ns		LMU112DMB30	

LMU16/216
16 x 16-bit Parallel Multiplier

FEATURES

- 20 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces TRW MPY016/TMC216, Cypress CY7C516, IDT 7216L, and AMD Am29516
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- DECC SMD No. 5962-86873
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Ceramic PGA
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC

DESCRIPTION

The **LMU16** and **LMU216** are high-speed, low power 16-bit parallel multipliers. The LMU16 and LMU216 are functionally identical; they differ only in packaging. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The LMU16 and LMU216 produce the 32-bit product of two 16-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control bit are similarly loaded by CLK B. The TCA and TCB controls specify the A and B operands as two's complement when HIGH, or unsigned magnitude when LOW.

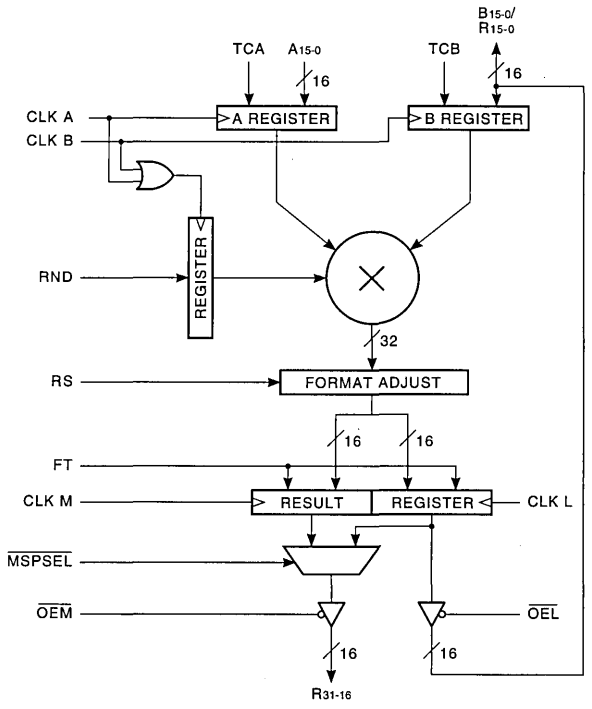
RND is loaded on the rising edge of the logical OR of CLK A and CLK B. RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

At the output, the Right Shift control (RS) selects either of two output formats. RS LOW produces a 31-bit product with a copy of the sign bit inserted in the MSB postion of the least significant half. RS HIGH gives a full 32-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK M and CLK L respectively. For asynchronous output, these registers may be made transparent by setting the feed through control (FT) HIGH.

The two halves of the product may be routed to a single 16-bit three-state output port (MSP) via a multiplexer. $\overline{\text{MSPSEL}}$ LOW causes the MSP outputs to be driven by the most significant half of the result. $\overline{\text{MSPSEL}}$ HIGH routes the least significant half of the result to the MSP outputs. In addition, the LSP is available via the B port through a separate three-state buffer.

The output multiplexer control $\overline{\text{MSPSEL}}$ uses a pin which is a supply ground in the TRW MPY016H/TMC216H. When this control is LOW (GND), the function is that of the MPY016H/TMC216H, thus allowing full compatibility.

LMU16/216 Block Diagram



4

FIGURE 1A. INPUT FORMATS

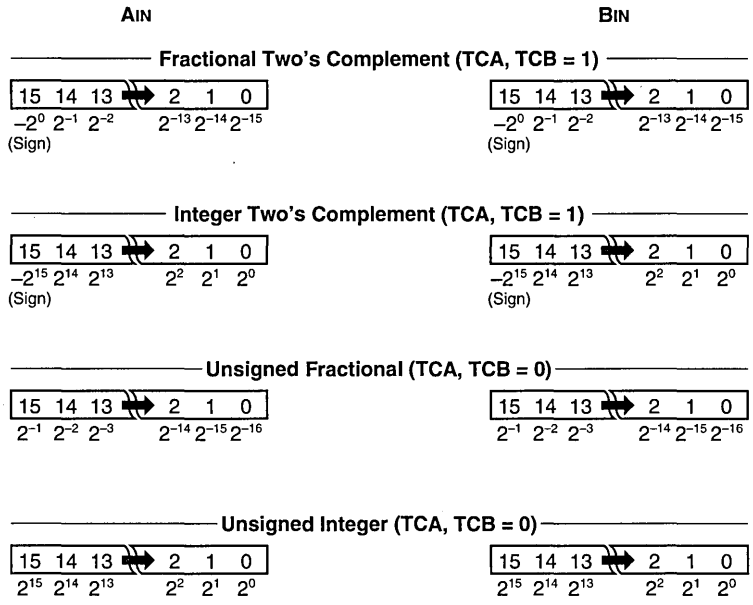
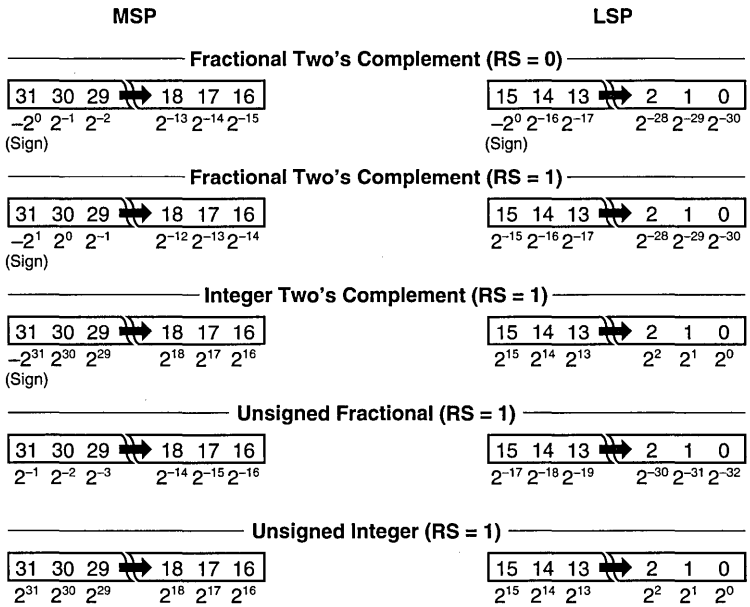


FIGURE 1B. OUTPUT FORMATS



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

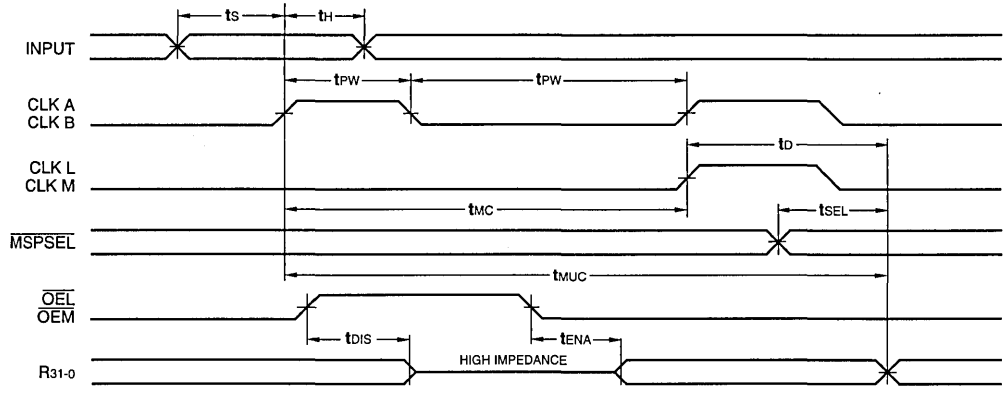
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU16/216–											
		65		55		45		35		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		65		55		45		35		25		20
t_{MUC}	Unclocked Multiply Time		85		75		65		55		38		30
t_{PW}	Clock Pulse Width	15		15		15		10		10		9	
t_S	Input Setup Time	15		15		15		12		12		11	
t_H	Input Hold Time	1		1		1		1		1		1	
t_D	Output Delay		30		30		30		25		20		18
t_{SEL}	Output Select Delay		25		25		25		25		20		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25		25		20		18
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		25		25		22		20		18

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU16/216–											
		75		65		55		40		30		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		75		65		55		40		30		25
t_{MUC}	Unclocked Multiply Time		95		85		75		60		43		38
t_{PW}	Clock Pulse Width	20		15		15		15		10		10	
t_S	Input Setup Time	15		15		15		15		12		12	
t_H	Input Hold Time	2		2		2		2		2		2	
t_D	Output Delay		35		30		30		25		20		20
t_{SEL}	Output Select Delay		30		30		30		25		20		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25		25		20		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		25		25		25		22		22

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

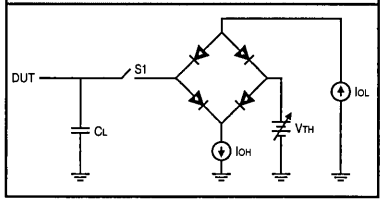
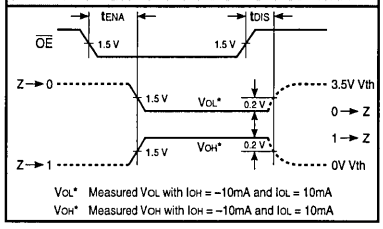
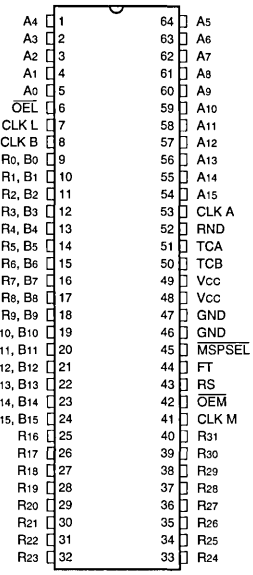


FIGURE B. THRESHOLD LEVELS



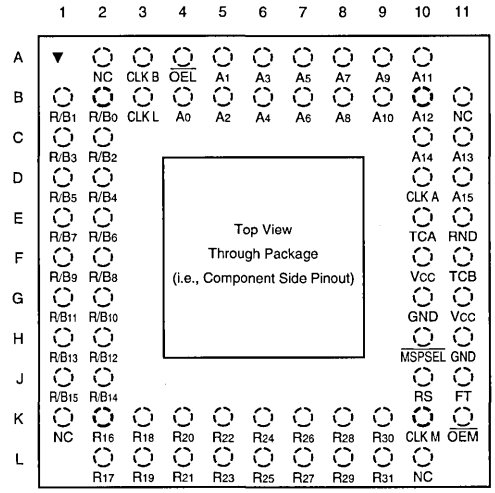
LMU16 — ORDERING INFORMATION

64-pin



* 64-pin DIP not recommended for new designs

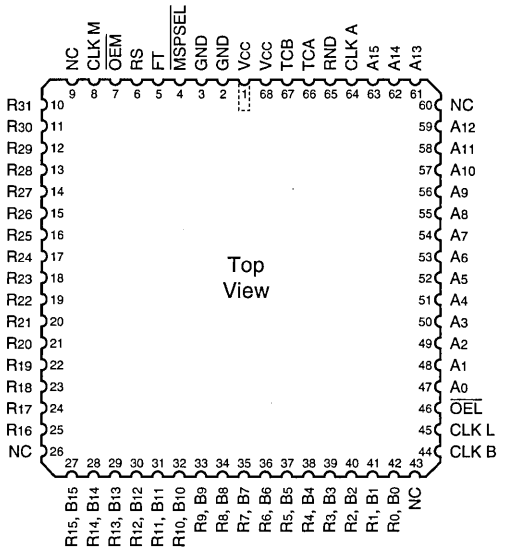
68-pin



Speed	Sidebraze Hermetic DIP (D6)	Ceramic Pin Grid Array (G2)
	0°C to +70°C — Commercial Screening	
65 ns	LMU16DC65	LMU16GC65
55 ns	LMU16DC55	LMU16GC55
45 ns	LMU16DC45	LMU16GC45
35 ns	LMU16DC35	LMU16GC35
25 ns		LMU16GC25
20 ns		LMU16GC20
	–55°C to +125°C — Commercial Screening	
75 ns	LMU16DM75	LMU16GM75
65 ns	LMU16DM65	LMU16GM65
55 ns	LMU16DM55	LMU16GM55
40 ns	LMU16DM40	LMU16GM40
30 ns		LMU16GM30
25 ns		LMU16GM25
	–55°C to +125°C — MIL-STD-883 Compliant	
75 ns	LMU16DMB75	LMU16GMB75
65 ns	LMU16DMB65	LMU16GMB65
55 ns	LMU16DMB55	LMU16GMB55
40 ns	LMU16DMB40	LMU16GMB40
30 ns		LMU16GMB30
25 ns		LMU16GMB25

LMU216 — ORDERING INFORMATION

68-pin



Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)		
	0°C to +70°C — COMMERCIAL SCREENING			
65 ns	LMU216JC65			
55 ns	LMU216JC55			
45 ns	LMU216JC45			
35 ns	LMU216JC35			
25 ns	LMU216JC25			
20 ns	LMU216JC20			
	–55°C to +125°C — COMMERCIAL SCREENING			
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
75 ns		LMU216KMB75		
65 ns		LMU216KMB65		
55 ns		LMU216KMB55		
40 ns		LMU216KMB40		
30 ns		LMU216KMB30		
25 ns		LMU216KMB25		

LMU18
16 x 16-bit Parallel Multiplier

FEATURES

- 20 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Full 32-bit Output Port — No Multiplexing Required
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- DECC SMD No. 5962-94523
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 84-pin Plastic LCC, J-Lead
  - 84-pin Ceramic PGA

DESCRIPTION

The **LMU18** is a high-speed, low power 16-bit parallel multiplier. The LMU18 is an 84-pin device which provides simultaneous access to all outputs. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

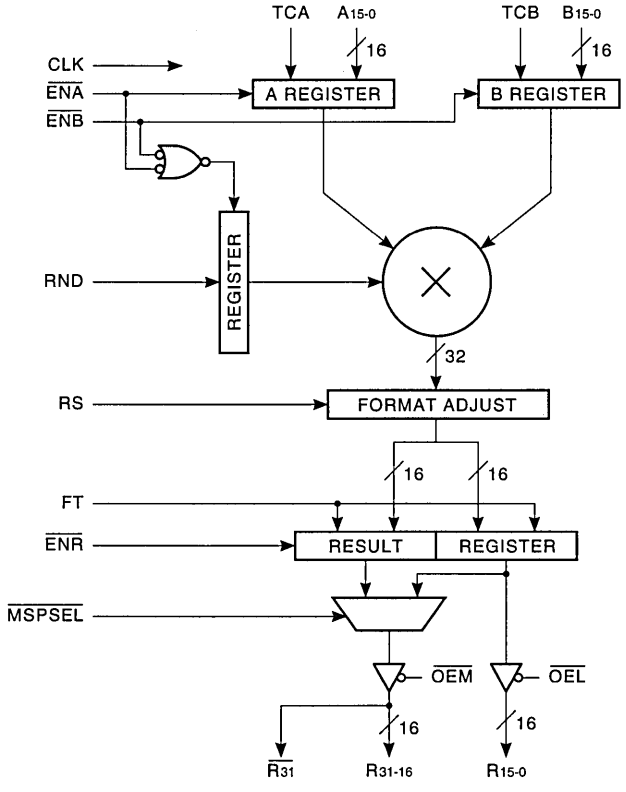
The LMU18 produces the 32-bit product of two 16-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK. B data and the TCB control bit are similarly loaded. Loading of the A and B registers is controlled by the $\overline{ENA}$ and $\overline{ENB}$ controls. When HIGH, these controls prevent application of the clock to the respective register. The TCA and TCB controls specify the operands as two's complement when HIGH, or unsigned magnitude when LOW.

RND is loaded on the rising edge of CLK, providing either $\overline{ENA}$ or $\overline{ENB}$ are LOW. RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

At the output, the Right Shift control (RS) selects either of two output formats. RS LOW produces a 31-bit product with a copy of the sign bit inserted in the MSB postion of the least significant half. RS HIGH gives a full 32-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK, subject to the $\overline{ENR}$ control. When $\overline{ENR}$ is HIGH, clocking of the result registers is prevented. For asynchronous output these registers may be made transparent by setting the feed through control (FT) HIGH.

The two halves of the product may be routed to a single 16-bit three-state output port (MSP) via a multiplexer. $\overline{MSPSEL}$ LOW causes the MSP outputs to be driven by the most significant half of the result. $\overline{MSPSEL}$ HIGH routes the least significant half of the result to the MSP pins. The MSB of the result is available in both true and complemented form to aid implementation of higher precision multipliers.

LMU18 Block Diagram



4

FIGURE 1A. INPUT FORMATS

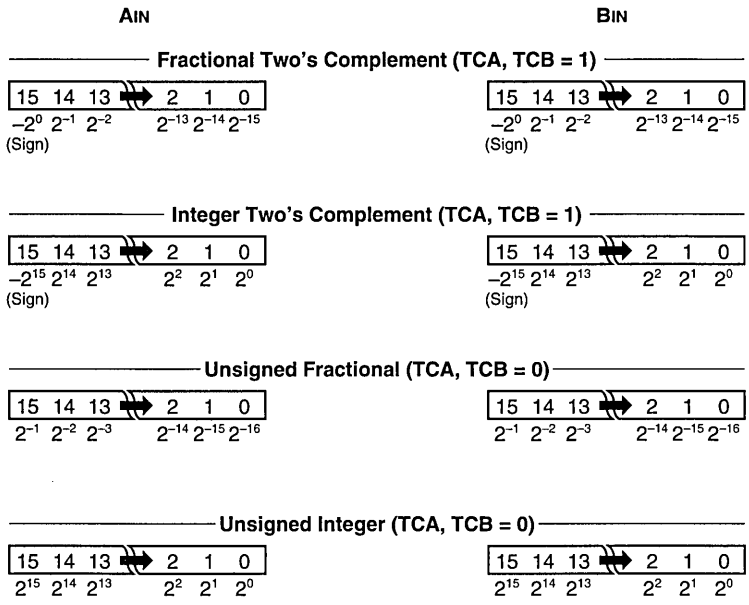
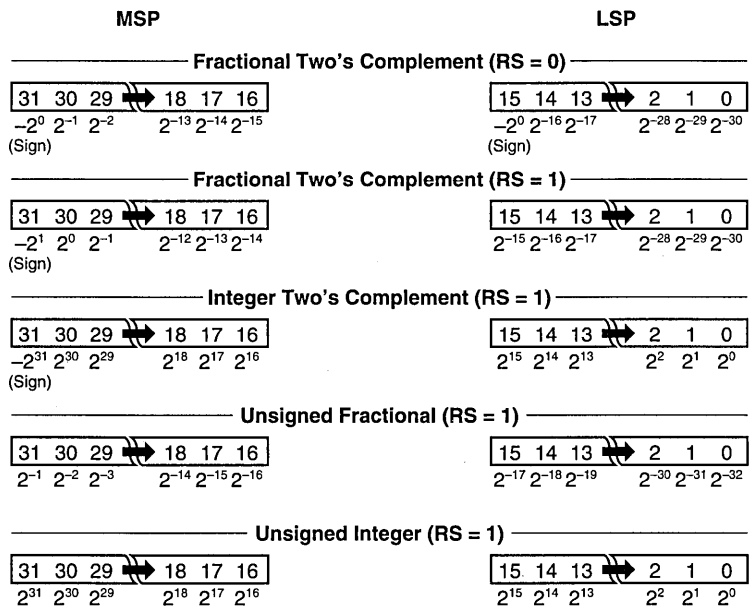


FIGURE 1B. OUTPUT FORMATS



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		25	45	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

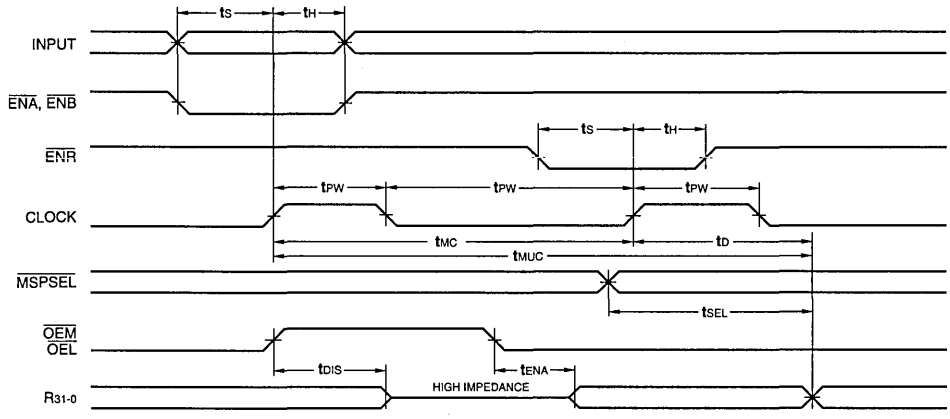
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU18–							
		65		45		35		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		65		45		35		20
t_{MUC}	Unclocked Multiply Time		85		65		55		30
t_{PW}	Clock Pulse Width	15		15		15		9	
t_S	Input Setup Time	15		15		12		11	
t_H	Input Hold Time	5		5		5		1	
t_D	Output Delay		30		30		28		18
t_{SEL}	Output Select Delay		25		25		25		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		20		20		18
t_{DIS}	Three-State Output Disable Delay (Note 11)		24		20		20		18

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU18–							
		75		55		45		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max		
t_{MC}	Clocked Multiply Time		75		55		45		25
t_{MUC}	Unclocked Multiply Time		95		85		65		38
t_{PW}	Clock Pulse Width	20		15		15		10	
t_S	Input Setup Time	15		15		12		12	
t_H	Input Hold Time	5		5		5		2	
t_D	Output Delay		35		35		33		20
t_{SEL}	Output Select Delay		30		30		30		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		20		20		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		24		20		20		20

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

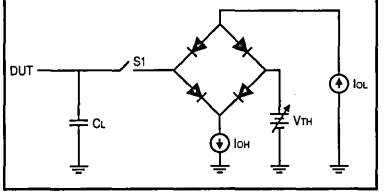
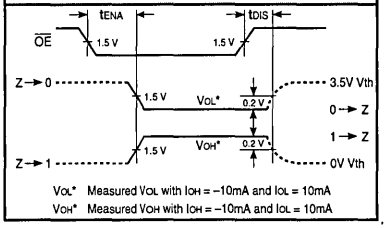


FIGURE B. THRESHOLD LEVELS



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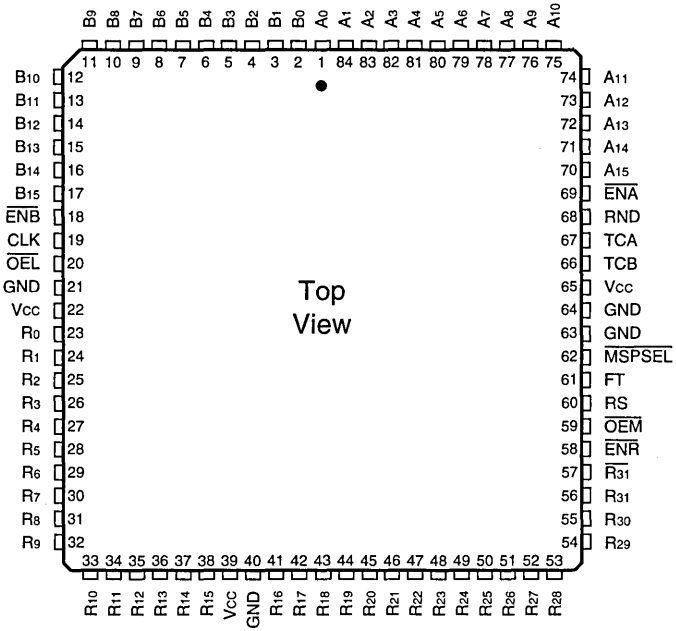
ORDERING INFORMATION

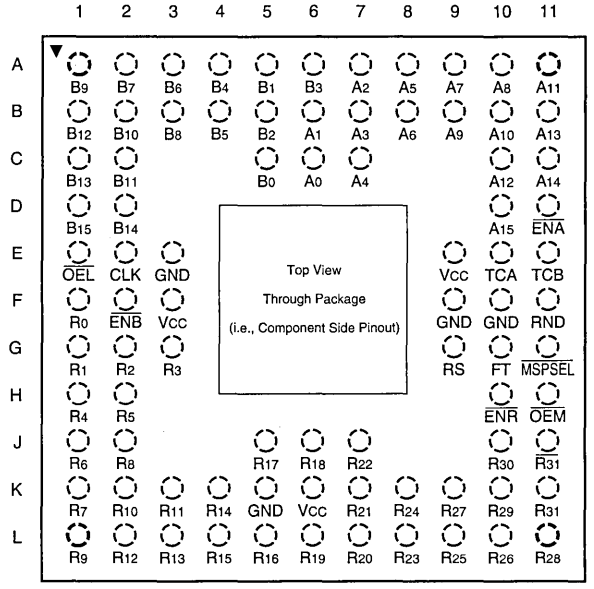
84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — COMMERCIAL SCREENING
65 ns	LMU18JC65
45 ns	LMU18JC45
35 ns	LMU18JC35
20 ns	LMU18JC20

ORDERING INFORMATION

84-pin



Speed	Ceramic Pin Grid Array (G3)
	0°C to +70°C — Commercial Screening
65 ns	LMU18GC65
45 ns	LMU18GC45
35 ns	LMU18GC35
20 ns	LMU18GC20
	–55°C to +125°C — Commercial Screening
75 ns	LMU18GM75
55 ns	LMU18GM55
45 ns	LMU18GM45
25 ns	LMU18GM25
	–55°C to +125°C — MIL-STD-883 Compliant
75 ns	LMU18GMB75
55 ns	LMU18GMB55
45 ns	LMU18GMB45
25 ns	LMU18GMB25

LMU217
16 x 16-bit Parallel multiplier

FEATURES

- 20 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces Cypress CY7C517, IDT 7217L, and AMD Am29517
- Single Clock Architecture with Register Enables
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- DECC SMD No. 5962-87686
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC
  - 64-pin Ceramic Flatpack

DESCRIPTION

The **LMU217** is a high-speed, low power 16-bit parallel multiplier. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The LMU217 produces the 32-bit product of two 16-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK. B data and the TCB control bit are similarly loaded. Loading of the A and B registers is controlled by the $\overline{ENA}$ and $\overline{ENB}$ controls. When HIGH, these controls prevent application of the clock to the respective register. The TCA and TCB controls specify the operands as two's complement when HIGH, or unsigned magnitude when LOW.

RND is loaded on the rising edge of CLK, provided either $\overline{ENA}$ or $\overline{ENB}$ are LOW. RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

At the output, the Right Shift control (RS) selects either of two output formats. RS LOW produces a 31-bit product with a copy of the sign bit inserted in the MSB postion of the least significant half. RS HIGH gives a full 32-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK, subject to the $\overline{ENR}$ control. When $\overline{ENR}$ is HIGH, clocking of the result registers is prevented. For asynchronous output, these registers may be made transparent by setting the feed through control (FT) HIGH.

The two halves of the product may be routed to a single 16-bit three-state output port (MSP) via a multiplexer. $\overline{MSPSEL}$ LOW causes the MSP outputs to be driven by the most significant half of the result. $\overline{MSPSEL}$ HIGH routes the least significant half of the result to the MSP pins. In addition, the LSP is available via the B port through a separate three-state buffer.

LMU217 Block Diagram

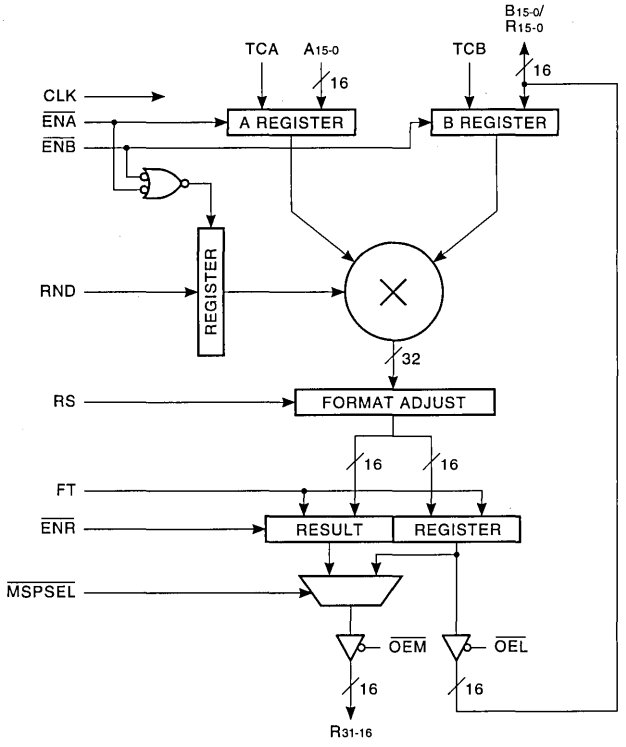


FIGURE 1A. INPUT FORMATS

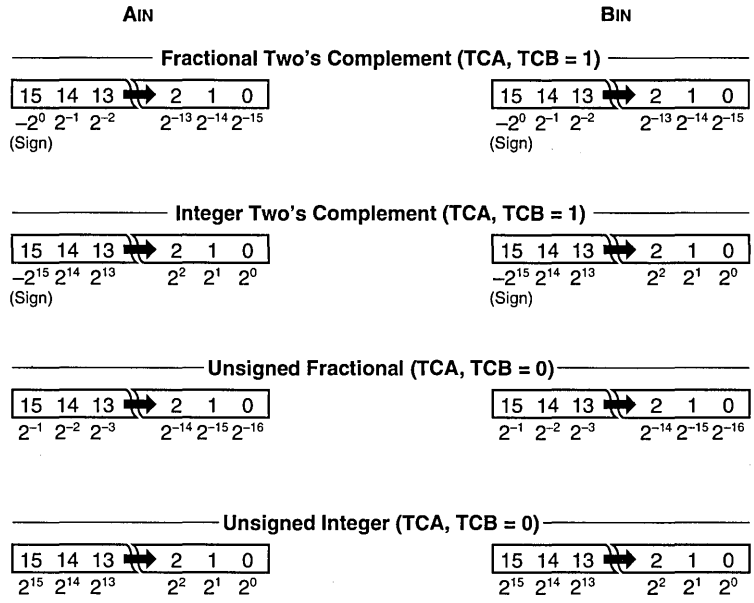
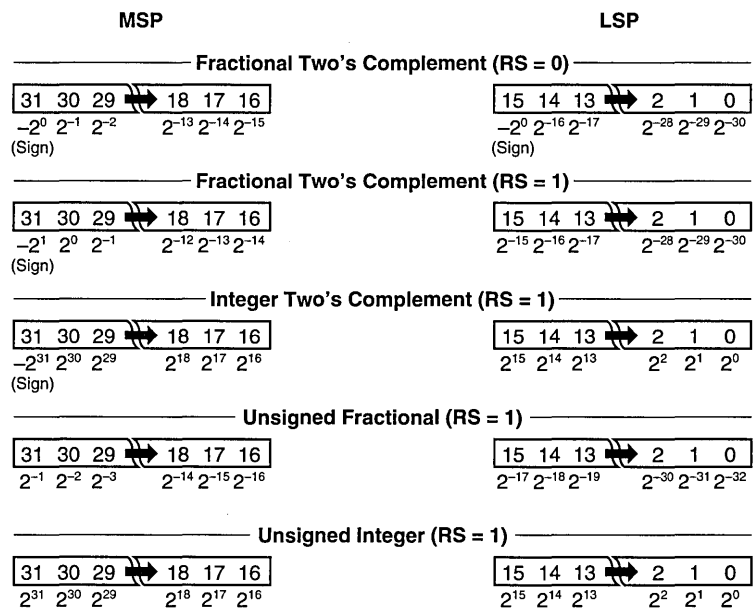


FIGURE 1B. OUTPUT FORMATS



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

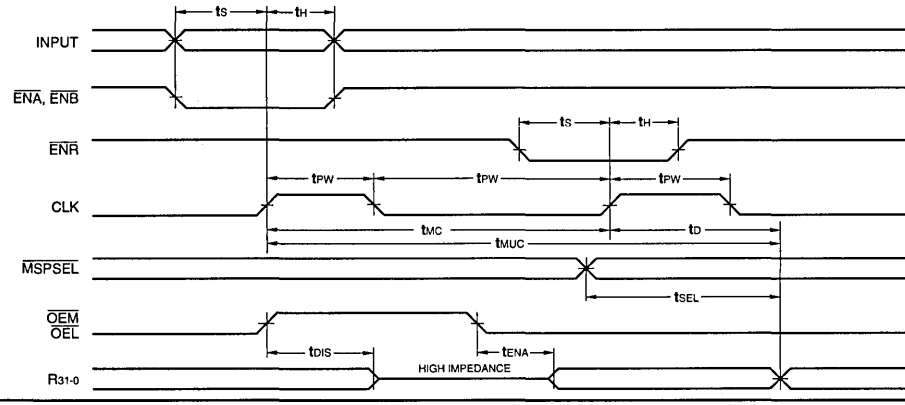
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU217–											
		65		55		45		35		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		65		55		45		35		25		20
t_{MUC}	Unclocked Multiply Time		85		75		65		55		38		30
t_{PW}	Clock Pulse Width	15		15		15		10		10		9	
t_S	Input Setup Time	15		15		15		12		12		11	
t_H	Input Hold Time	3		3		3		1		1		1	
t_D	Output Delay		30		30		30		25		20		18
t_{SEL}	Output Select Delay		25		25		25		25		20		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25		25		20		18
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		25		25		25		20		18

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU217–											
		75		65		55		40		30		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		75		65		55		40		30		25
t_{MUC}	Unclocked Multiply Time		95		85		75		60		43		38
t_{PW}	Clock Pulse Width	20		15		15		15		10		10	
t_S	Input Setup Time	15		15		15		15		12		12	
t_H	Input Hold Time	3		3		3		2		2		2	
t_D	Output Delay		35		30		30		25		20		20
t_{SEL}	Output Select Delay		30		30		30		25		20		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25		25		20		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		25		25		25		20		20

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

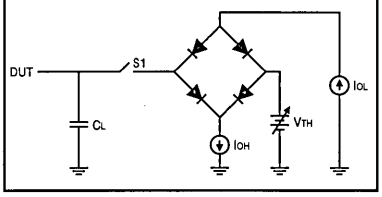
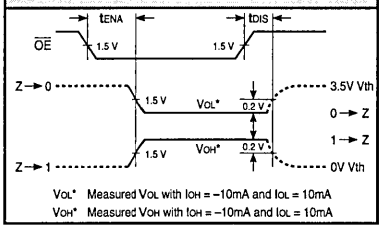


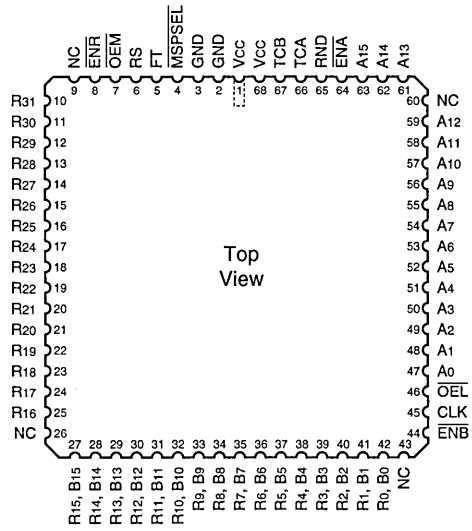
FIGURE B. THRESHOLD LEVELS



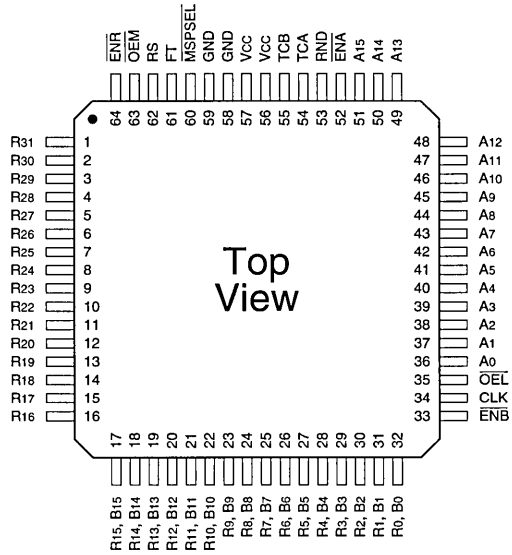
4

ORDERING INFORMATION

68-pin



64-pin



Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)	Ceramic Flatpack (F4)	
	0°C to +70°C — Commercial Screening			
65 ns	LMU217JC65			
55 ns	LMU217JC55			
45 ns	LMU217JC45			
35 ns	LMU217JC35			
25 ns	LMU217JC25			
20 ns	LMU217JC20			
	–55°C to +125°C — Commercial Screening			
	–55°C to +125°C — MIL-STD-883 Compliant			
75 ns		LMU217KMB75	LMU217FMB75	
65 ns		LMU217KMB65	LMU217FMB65	
55 ns		LMU217KMB55	LMU217FMB55	
40 ns		LMU217KMB40	LMU217FMB40	
30 ns		LMU217KMB30	LMU217FMB30	
25 ns		LMU217KMB25	LMU217FMB25	

LMA1008
8 x 8-bit Multiplier-Accumulator

FEATURES

- 20 ns Multiply-Accumulate Time
- Low Power CMOS Technology
- Replaces Raytheon TMC2208
- Two's Complement or Unsigned Operands
- Accumulator Performs Preload, Accumulate, and Subtract
- Three-State Outputs
- DECC SMD No. 5962-90708
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 48-pin Plastic DIP
  - 48-pin Sidebraze, Hermetic DIP
  - 68-pin Plastic LCC, J-Lead

DESCRIPTION

The **LMA1008** is a high-speed, low power 8-bit multiplier-accumulators. It is pin-for-pin equivalent to the Raytheon TMC2208 multiplier-accumulators. Full ambient temperature range operation is achieved by the use of advanced CMOS technology.

The LMA1008 produces the 16-bit product of two 8-bit numbers. The results of a series of multiplications may be accumulated to form the sum of products. Accumulation is performed to 19-bit precision with the multiplier product sign extended as appropriate.

Data present at the A and B input registers is latched on the rising edges of CLK A and CLK B respectively. RND, TC, ACC, and SUB controls are latched on the rising edge of the logical OR of CLK A and CLK B. TC specifies the input as two's complement (TC HIGH) or unsigned magnitude (TC LOW). RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 8 least significant bits produces a result correctly rounded to 8-bit precision.

The ACC and SUB inputs control accumulator operation. ACC HIGH results in addition of the multiplier product and the accumulator contents, with the result stored in the accumulator register on the rising edge of CLK R. ACC and SUB HIGH results in subtraction of the accumulator contents from the multiplier product, with the result stored in the accumulator register. With ACC LOW, no accumulation occurs and the next product is loaded directly into the accumulator register.

The LMA1008 output register (accumulator register) is divided into three independently controlled sections. The least significant result (LSR) and most significant result (MSR) registers are 8 bits in length. The extended result register (XTR) is 3 bits long.

Each output register has an independent output enable control. In addition to providing control of the three-state output buffers, when $\overline{OEX}$, $\overline{OEM}$, or $\overline{OEL}$ are HIGH and PREL is HIGH, data can be preloaded via the bidirectional output pins into the respective output registers. Data present on the output pins is latched on the rising edge of CLK R. The interrelation of PREL and the enable controls is summarized in Table 1.

LMA1008 Block Diagram

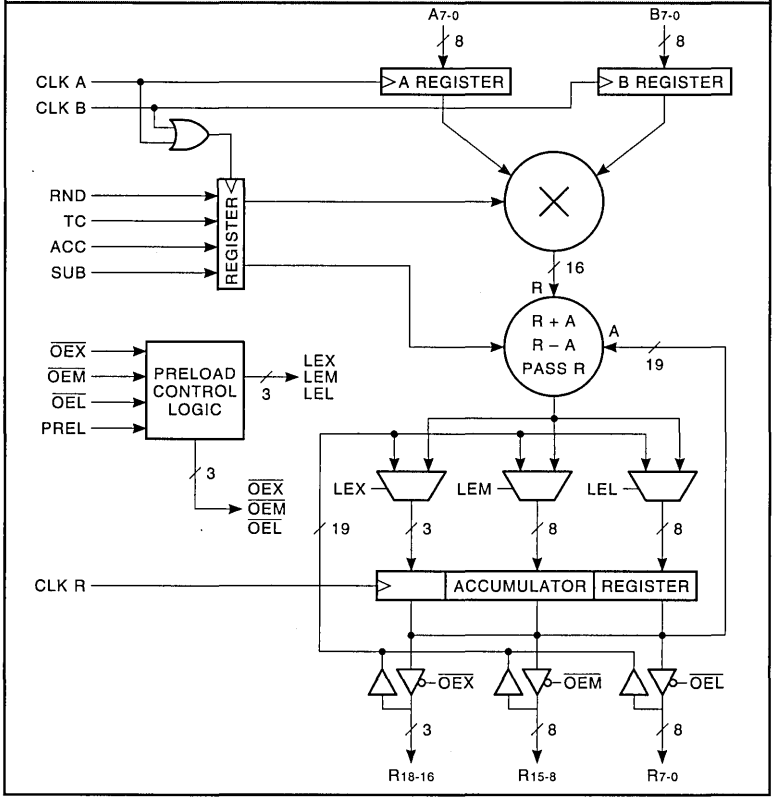


Table 1. Preload Truth Table

PREL	$\overline{OEX}$	$\overline{OEM}$	$\overline{OEL}$	XTR	MSR	LSR
L	L	L	L	OUT	OUT	OUT
L	L	L	H	OUT	OUT	Z
L	L	H	L	OUT	Z	OUT
L	L	H	H	OUT	Z	Z
L	H	L	L	Z	OUT	OUT
L	H	L	H	Z	OUT	Z
L	H	H	L	Z	Z	OUT
L	H	H	H	Z	Z	Z
H	L	L	L	Z	Z	Z
H	L	L	H	Z	Z	PREL
H	L	H	L	Z	PREL	Z
H	L	H	H	Z	PREL	PREL
H	H	L	L	PREL	Z	Z
H	H	L	H	PREL	Z	PREL
H	H	H	L	PREL	PREL	Z
H	H	H	H	PREL	PREL	PREL

PREL = Preload data to appropriate register
OUT = Register available on output pins
Z = High impedance state

Figure 1a. Input Formats

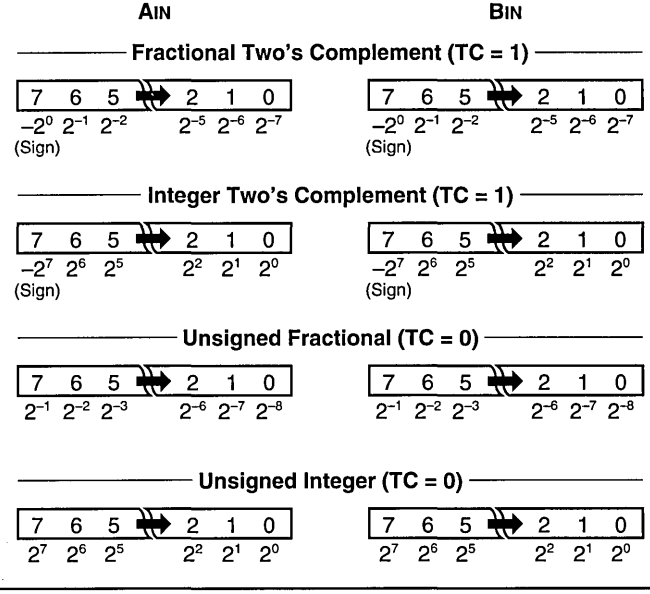
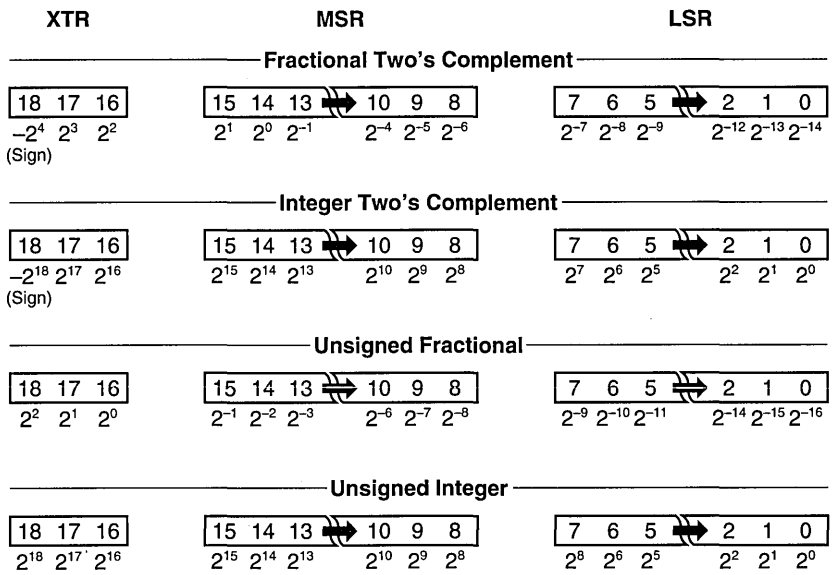


Figure 1b. Output Formats



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

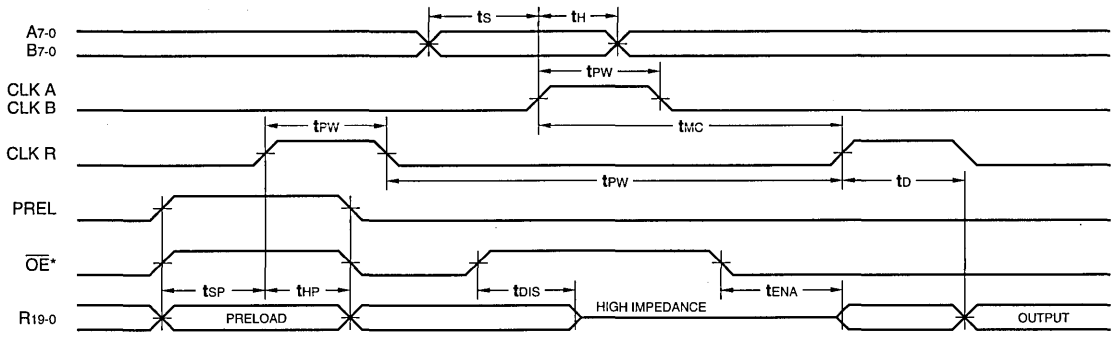
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMA1008–			
		40		20	
Symbol	Parameter	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		40		20
t_{PW}	Clock Pulse Width	15		8	
t_S	Input Register Setup Time	10		10	
t_H	Input Register Hold Time	0		0	
t_{SP}	Preload Setup Time	12		12	
t_{HP}	Preload Hold Time	2		2	
t_D	Output Delay		23		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		19		18
t_{DIS}	Three-State Output Disable Delay (Note 11)		16		16

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMA1008–			
		50		25	
Symbol	Parameter	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		50		25
t_{PW}	Clock Pulse Width	15		10	
t_S	Input Register Setup Time	11		11	
t_H	Input Register Hold Time	2		2	
t_{SP}	Preload Setup Time	13		13	
t_{HP}	Preload Hold Time	2		2	
t_D	Output Delay		25		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		21		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		18		18

SWITCHING WAVEFORMS



*includes $\overline{OEX}$, $\overline{OEM}$, $\overline{OEL}$

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

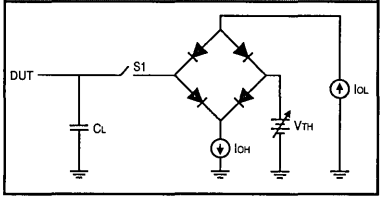
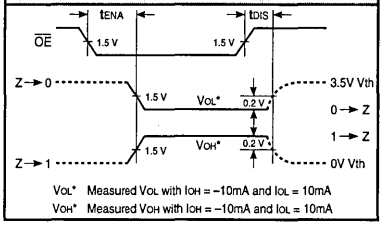


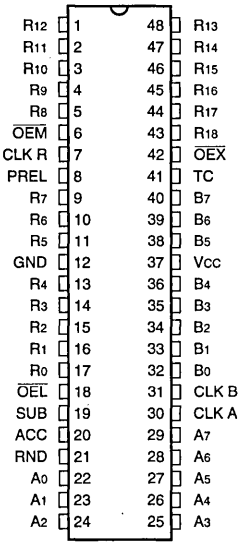
FIGURE B. THRESHOLD LEVELS



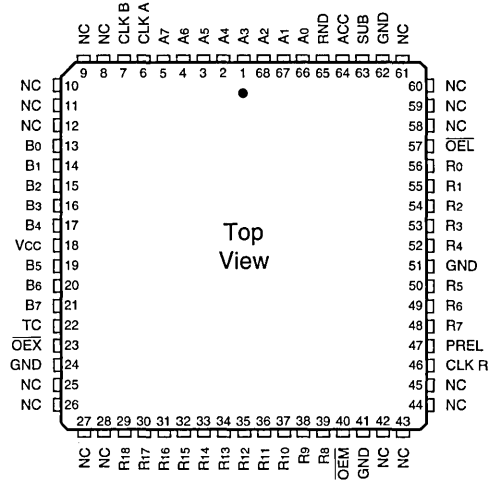
4

LMA1008 — ORDERING INFORMATION

48-pin



68-pin



Speed	Sidebraze Hermetic DIP (D6)	Plastic DIP (P5)	Plastic J-Lead Chip Carrier (J2)
	0°C to +70°C — COMMERCIAL SCREENING		
40 ns		LMA1008PC40	LMA1008JC40
20 ns		LMA1008PC20	LMA1008JC20
	–55°C to +125°C — COMMERCIAL SCREENING		
50 ns			
25 ns			
	–55°C to +125°C — MIL-STD-883 COMPLIANT		
50 ns	LMA1008DMB50		
25 ns	LMA1008DMB25		

LMA1009/2009
12 x 12-bit Multiplier-Accumulator

FEATURES

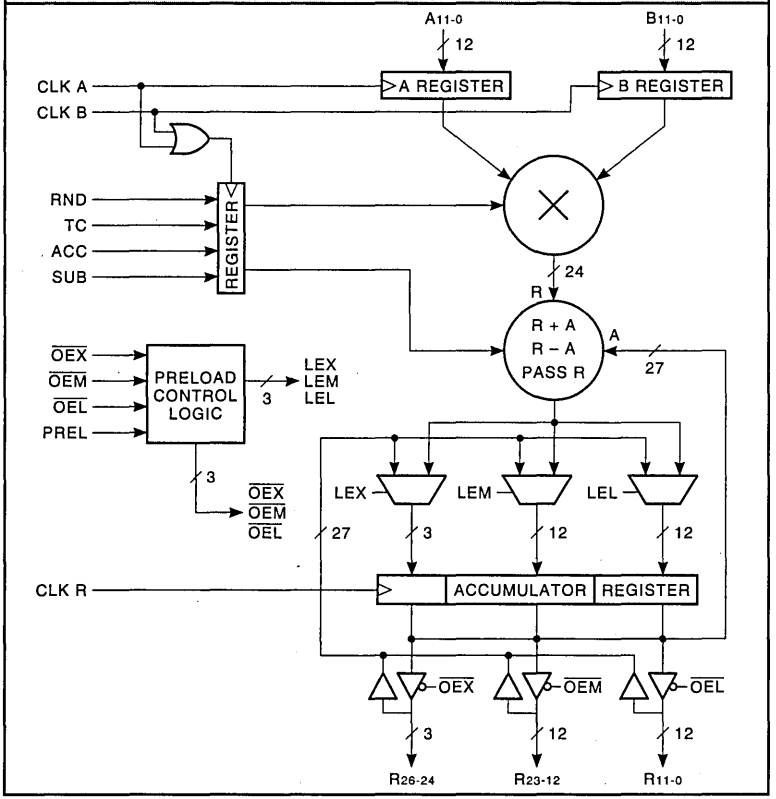
- 20 ns Multiply-Accumulate Time
- Low Power CMOS Technology
- Replaces TRW TDC1009/TMC2009
- Two's Complement or Unsigned Operands
- Accumulator Performs Preload, Accumulate, and Subtract
- Three-State Outputs
- DECC SMD No. 5962-90996
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Ceramic PGA
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC

DESCRIPTION

The **LMA1009** and **LMA2009** are high-speed, low power 12-bit multiplier-accumulators. They are pin-for-pin equivalent to the TRW TDC1009/TMC2009 multiplier-accumulators. The LMA1009 and LMA2009 are functionally identical; they differ only in packaging. Full ambient temperature range operation is achieved by the use of advanced CMOS technology.

The LMA1009/2009 produces the 24-bit product of two 12-bit numbers. The results of a series of multiplications may be accumulated to form the sum of products. Accumulation is performed to 27-bit precision with the multiplier product sign extended as appropriate.

LMA1009/2009 Block Diagram



Data present at the A and B input registers is latched on the rising edges of CLK A and CLK B respectively. RND, TC, ACC, and SUB controls are latched on the rising edge of the logical OR of CLK A and CLK B. TC specifies the input as two's complement (TC HIGH) or unsigned magnitude (TC LOW). RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 12 least significant bits produces a result correctly rounded to 12-bit precision.

The ACC and SUB inputs control accumulator operation. ACC HIGH results in addition of the multiplier product and the accumulator contents, with the result stored in the accumulator register on the rising edge of CLK R. ACC and SUB HIGH results in subtraction of the accumulator contents from the multiplier product, with the result stored in the accumulator register. With ACC LOW, no accumulation occurs and the next product is loaded directly into the accumulator register.

The LMA1009/2009 output register (accumulator register) is divided into three independently controlled sections. The least significant result (LSR) and most significant result (MSR) registers are 12 bits in length. The extended result register (XTR) is 3 bits long.

Each output register has an independent output enable control. In addition to providing control of the three-state output buffers, when $\overline{OEX}$, $\overline{OEM}$, or $\overline{OEL}$ are HIGH and PREL is HIGH, data can be preloaded via the bidirectional output pins into the respective output registers. Data present on the output pins is latched on the rising edge of CLK R. The interrelation of PREL and the enable controls is summarized in Table 1.

Table 1. Preload Truth Table

PREL	$\overline{OEX}$	$\overline{OEM}$	$\overline{OEL}$	XTR	MSR	LSR
L	L	L	L	OUT	OUT	OUT
L	L	L	H	OUT	OUT	Z
L	L	H	L	OUT	Z	OUT
L	L	H	H	OUT	Z	Z
L	H	L	L	Z	OUT	OUT
L	H	L	H	Z	OUT	Z
L	H	H	L	Z	Z	OUT
L	H	H	H	Z	Z	Z
H	L	L	L	Z	Z	Z
H	L	L	H	Z	Z	PREL
H	L	H	L	Z	PREL	Z
H	L	H	H	Z	PREL	PREL
H	H	L	L	PREL	Z	Z
H	H	L	H	PREL	Z	PREL
H	H	H	L	PREL	PREL	Z
H	H	H	H	PREL	PREL	PREL

PREL = Preload data to appropriate register
OUT = Register available on output pins
Z = High impedance state

Figure 1a. Input Formats

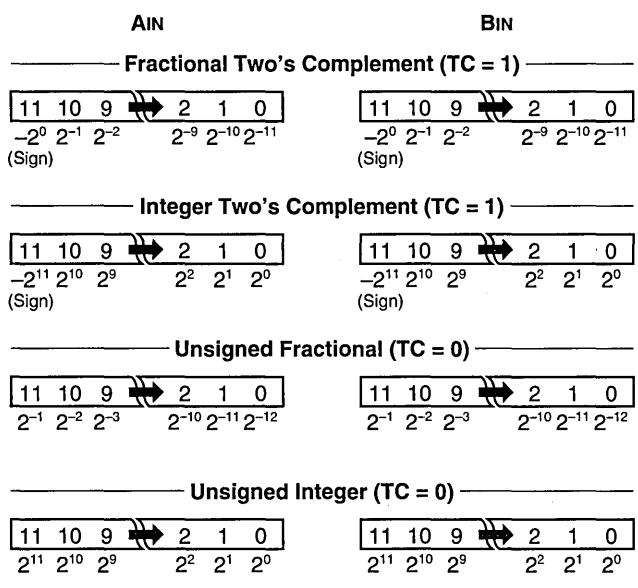
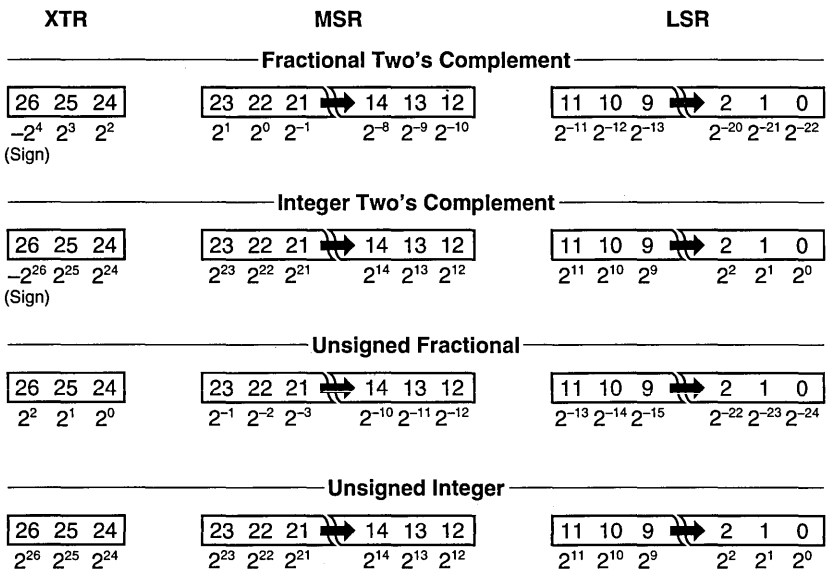


Figure 1b. Output Formats



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

4

Electrical Characteristics *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

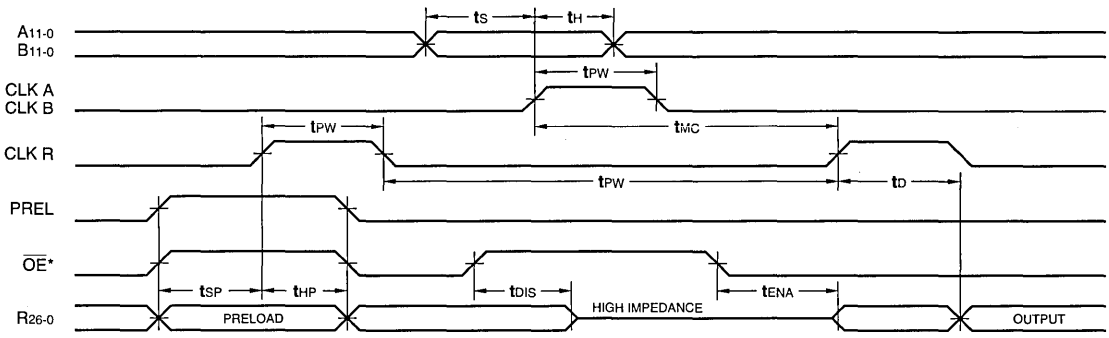
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMA1009/2009–							
		75		55		45		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		75		55		45		20
t_{PW}	Clock Pulse Width	15		15		15		8	
t_S	Input Register Setup Time	15		15		12		10	
t_H	Input Register Hold Time	2		2		2		2	
t_{SP}	Preload Setup Time	15		15		12		10	
t_{HP}	Preload Hold Time	2		2		2		2	
t_D	Output Delay		30		25		25		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		30		30		25		18
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		25		25		18

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMA1009/2009–							
		95		65		55		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		95		65		55		25
t_{PW}	Clock Pulse Width	20		20		15		10	
t_S	Input Register Setup Time	20		20		15		12	
t_H	Input Register Hold Time	2		2		2		2	
t_{SP}	Preload Setup Time	20		20		15		12	
t_{HP}	Preload Hold Time	2		2		2		2	
t_D	Output Delay		35		30		25		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		35		35		30		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		30		30		30		20

SWITCHING WAVEFORMS



*includes $\overline{OEX}$, $\overline{OEM}$, $\overline{OEL}$

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

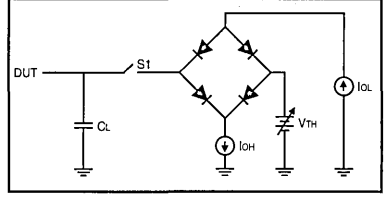
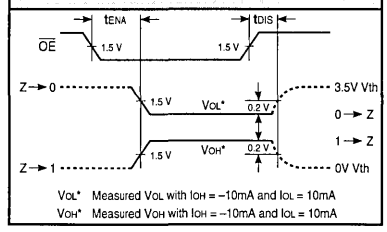
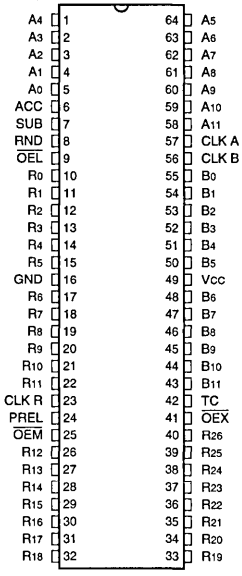


FIGURE B. THRESHOLD LEVELS



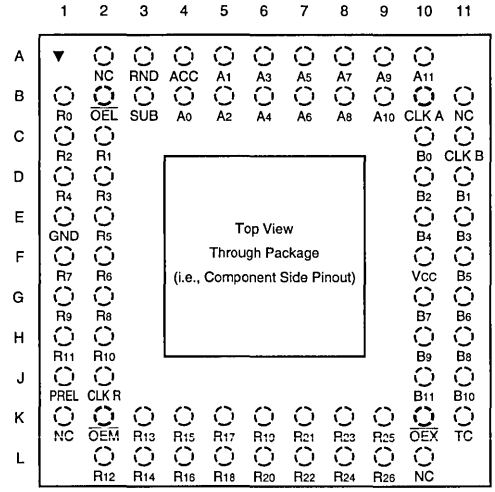
LMA1009 — ORDERING INFORMATION

64-pin



*** 64-pin DIP not recommended for new designs**

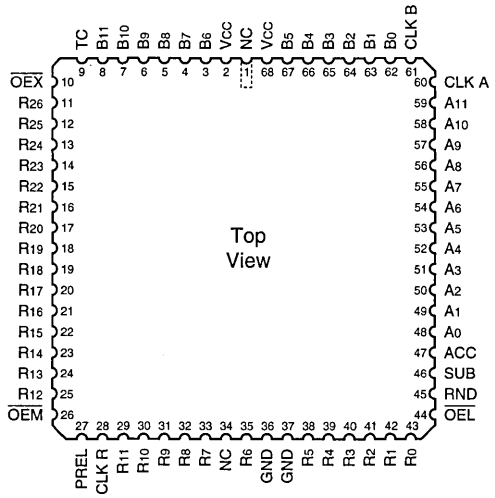
68-pin



Speed	Sidebraze Hermetic DIP (D6)	Ceramic Pin Grid Array (G2)
	0°C to +70°C — Commercial Screening	
75 ns	LMA1009DC75	LMA1009GC75
55 ns	LMA1009DC55	LMA1009GC55
45 ns	LMA1009DC45	LMA1009GC45
20 ns		LMA1009GC20
	–55°C to +125°C — Commercial Screening	
95 ns	LMA1009DM95	LMA1009GM95
65 ns	LMA1009DM65	LMA1009GM65
55 ns	LMA1009DM55	LMA1009GM55
25 ns		LMA1009GM25
	–55°C to +125°C — MIL-STD-883 Compliant	
95 ns	LMA1009DMB95	LMA1009GMB95
65 ns	LMA1009DMB65	LMA1009GMB65
55 ns	LMA1009DMB55	LMA1009GMB55
25 ns		LMA1009GMB25

LMA2009 — ORDERING INFORMATION

68-pin



Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)	
	0°C to +70°C — COMMERCIAL SCREENING		
75 ns	LMA2009JC75		
55 ns	LMA2009JC55		
45 ns	LMA2009JC45		
20 ns	LMA2009JC20		
	–55°C to +125°C — COMMERCIAL SCREENING		
	–55°C to +125°C — MIL-STD-883 COMPLIANT		
95 ns		LMA2009KMB95	
65 ns		LMA2009KMB65	
55 ns		LMA2009KMB55	
25 ns		LMA2009KMB25	

LMA1010/2010
16 x 16-bit Multiplier-Accumulator

FEATURES

- 20 ns Multiply-Accumulate Time
- Replaces TRW TMC2210, Cypress CY7C510, IDT 7210L, and AMD Am29510
- Two's Complement or Unsigned Operands
- Accumulator Performs Preload, Accumulate, and Subtract
- Three-State Outputs
- DECC SMD No. 5962-88733
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Ceramic PGA
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC

DESCRIPTION

The **LMA1010** and **LMA2010** are high-speed, low power 16-bit multiplier-accumulators. The LMA1010 and LMA2010 are functionally identical; they differ only in packaging. Full military ambient temperature range operation is achieved with advanced CMOS technology.

The LMA1010 and LMA2010 produce the 32-bit product of two 16-bit numbers. The results of a series of multiplications may be accumulated to form the sum of products. Accumulation is performed to 35-bit precision with the multiplier product sign extended as appropriate.

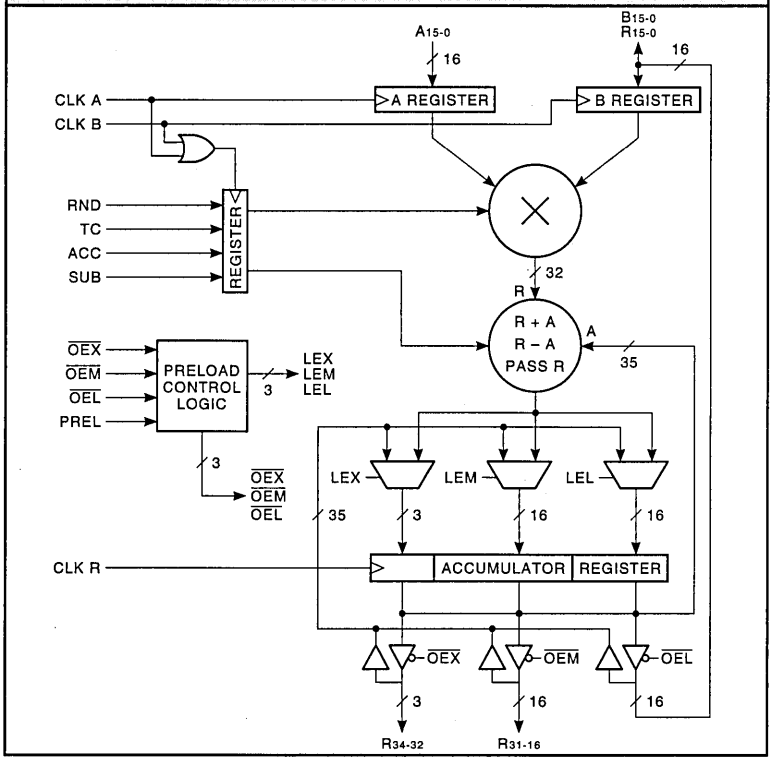
Data present at the A and B input registers is latched on the rising edges of CLK A and CLK B respectively. RND, TC, ACC, and SUB controls are latched on the rising edge of the logical OR of CLK A and CLK B. TC specifies the input as two's complement (TC HIGH) or unsigned magnitude (TC LOW). RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

ACC and SUB control accumulator operation. ACC HIGH results in addition of the multiplier product and the accumulator contents, with the result stored in the accumulator register on the rising edge of CLK R. ACC and SUB HIGH results in subtraction of the accumulator contents from the multiplier product, with the result stored in the accumulator register. With ACC LOW, no accumulation occurs and the next product is loaded directly into the accumulator register.

The LMA1010/2010 output register (accumulator register) is divided into three independently controlled sections. The least significant result (LSR) and most significant result (MSR) registers are 16 bits in length. The extended result register (XTR) is 3 bits long. The output signals R15-0 and input signals B15-0 share the same bidirectional pins.

Each output register has an independent output enable control. In addition to providing three-state control of the output buffers, when $\overline{OEX}$, $\overline{OEM}$, or $\overline{OEL}$ are HIGH and PREL is HIGH, data can be preloaded via the bidirectional output pins into the respective output registers. Data present on the output pins is latched on the rising edge of CLK R. The interrelation of PREL and the enable controls is summarized in Table 1.

LMA1010/2010 BLOCK DIAGRAM



4

Table 1. Preload Truth Table

PREL	$\overline{OEX}$	$\overline{OEM}$	$\overline{OEL}$	XTR	MSR	LSR
L	L	L	L	OUT	OUT	OUT
L	L	L	H	OUT	OUT	Z
L	L	H	L	OUT	Z	OUT
L	L	H	H	OUT	Z	Z
L	H	L	L	Z	OUT	OUT
L	H	L	H	Z	OUT	Z
L	H	H	L	Z	Z	OUT
L	H	H	H	Z	Z	Z
H	L	L	L	Z	Z	Z
H	L	L	H	Z	Z	PREL
H	L	H	L	Z	PREL	Z
H	L	H	H	Z	PREL	PREL
H	H	L	L	PREL	Z	Z
H	H	L	H	PREL	Z	PREL
H	H	H	L	PREL	PREL	Z
H	H	H	H	PREL	PREL	PREL

PREL = Preload data to appropriate register
OUT = Register available on output pins
Z = High impedance state

Figure 1a. Input Formats

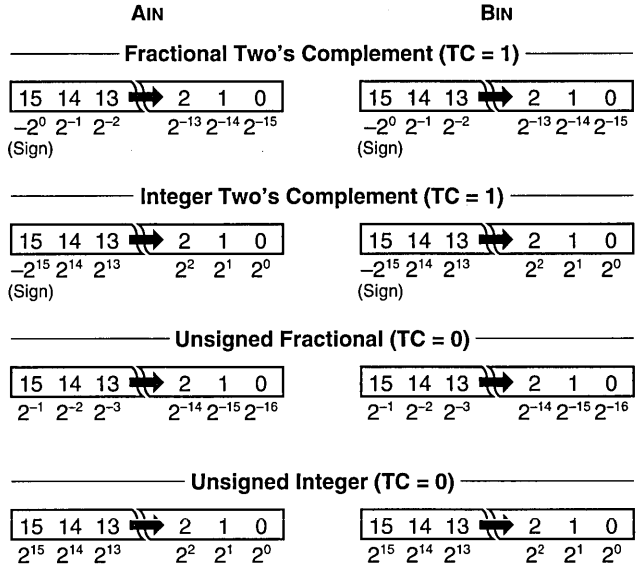
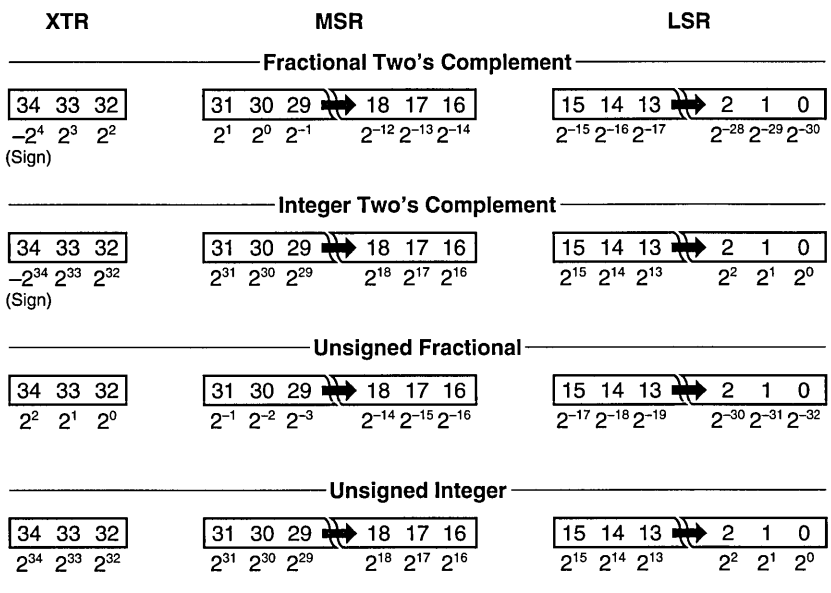


Figure 1b. Output Formats



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

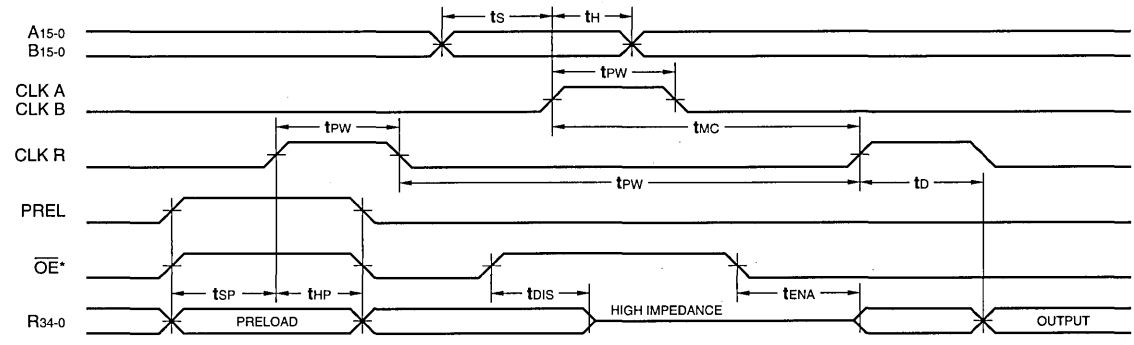
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMA1010/2010–											
		65		55		45		35		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		65		55		45		35		25		20
t_{PW}	Clock Pulse Width	15		15		15		10		10		9	
t_S	Input Register Setup Time	15		15		12		12		12		10	
t_H	Input Register Hold Time	2		2		2		2		2		2	
t_{SP}	Preload Setup Time	15		15		12		12		12		10	
t_{HP}	Preload Hold Time	2		2		2		2		2		2	
t_D	Output Delay		30		25		25		25		20		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		30		30		25		25		20		18
t_{DIS}	Three-State Output Disable Delay (Note 11)		30		25		25		25		20		18

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMA1010/2010–											
		75		65		55		40		30		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		75		65		55		40		30		25
t_{PW}	Clock Pulse Width	20		15		15		15		10		10	
t_S	Input Register Setup Time	20		15		15		15		12		12	
t_H	Input Register Hold Time	2		2		2		2		2		2	
t_{SP}	Preload Setup Time	20		15		15		15		12		12	
t_{HP}	Preload Hold Time	2		2		2		2		2		2	
t_D	Output Delay		35		30		30		25		20		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		35		30		30		25		20		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		35		25		25		25		20		20

SWITCHING WAVEFORMS



*includes $\overline{OEX}$, $\overline{OEM}$, $\overline{OEL}$

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

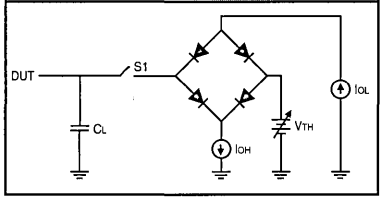
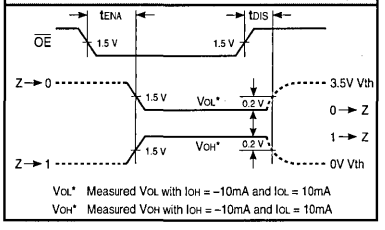
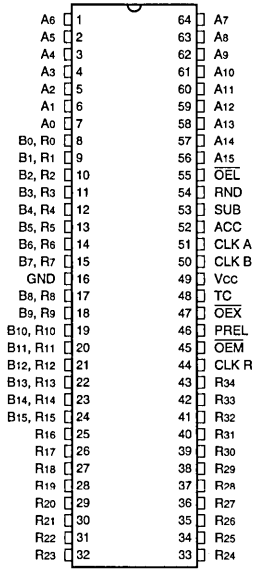


FIGURE B. THRESHOLD LEVELS



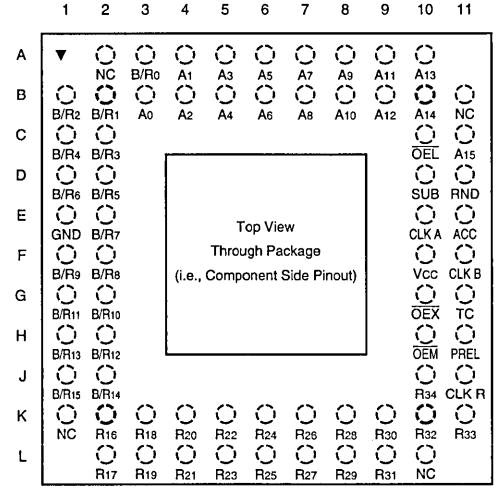
LMA1010 — ORDERING INFORMATION

64-pin



* 64-pin DIP not recommended for new designs

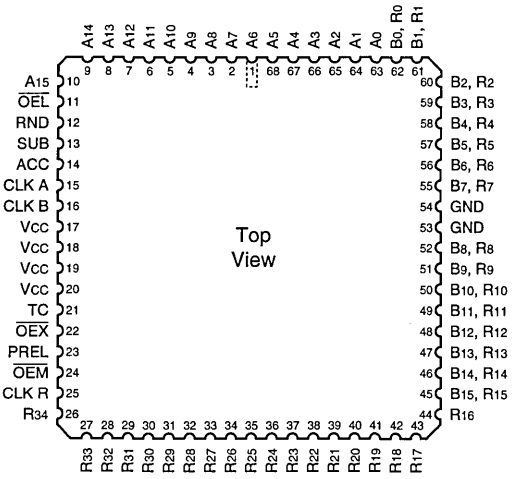
68-pin



Speed	Sidebraze Hermetic DIP (D6)	Ceramic Pin Grid Array (G2)
	0°C to +70°C — COMMERCIAL SCREENING	
65 ns	LMA1010DC65	LMA1010GC65
55 ns	LMA1010DC55	LMA1010GC55
45 ns	LMA1010DC45	LMA1010GC45
35 ns		LMA1010GC35
25 ns		LMA1010GC25
20 ns		LMA1010GC20
	–55°C to +125°C — COMMERCIAL SCREENING	
75 ns	LMA1010DM75	LMA1010GM75
65 ns	LMA1010DM65	LMA1010GM65
55 ns	LMA1010DM55	LMA1010GM55
40 ns		LMA1010GM40
30 ns		LMA1010GM30
25 ns		LMA1010GM25
	–55°C to +125°C — MIL-STD-883 COMPLIANT	
75 ns	LMA1010DMB75	LMA1010GMB75
65 ns	LMA1010DMB65	LMA1010GMB65
55 ns	LMA1010DMB55	LMA1010GMB55
40 ns		LMA1010GMB40
30 ns		LMA1010GMB30
25 ns		LMA1010GMB25

LMA2010 — ORDERING INFORMATION

68-pin



Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)		
	0°C to +70°C — COMMERCIAL SCREENING			
65 ns	LMA2010JC65			
55 ns	LMA2010JC55			
45 ns	LMA2010JC45			
35 ns	LMA2010JC35			
25 ns	LMA2010JC25			
20 ns	LMA2010JC20			
	–55°C to +125°C — COMMERCIAL SCREENING			
75 ns				
65 ns				
55 ns				
40 ns				
30 ns				
25 ns				
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
75 ns		LMA2010KMB75		
65 ns		LMA2010KMB65		
55 ns		LMA2010KMB55		
40 ns		LMA2010KMB40		
30 ns		LMA2010KMB30		
25 ns		LMA2010KMB25		

FEATURES

- 12 x 12-bit Multiplier with Pipelined 26-bit Output Summer
- Summer has 26-bit Input Port Fully Independent from Multiplier Inputs
- Cascadable to Form Video Rate FIR Filter with 3-bit Headroom
- A, B, and C Input Registers Separately Enabled for Maximum Flexibility
- 28 MHz Data Rate for FIR Filtering Applications
- High Speed, Low Power CMOS Technology
- DECC SMD No. 5962-94608
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 84-pin Plastic LCC, J-Lead
  - 84-pin Ceramic PGA

DESCRIPTION

The **LMS12** is a high-speed 12 x 12-bit combinatorial multiplier integrated with a 26-bit adder in a single 84-pin package. It is an ideal building block for the implementation of very high-speed FIR filters for video, RADAR, and other similar applications. The LMS12 implements the general form (A•B) + C. As a result, it is also useful in implementing polynomial approximations to transcendental functions.

ARCHITECTURE

A block diagram of the LMS12 is shown below. Its major features are discussed individually in the following paragraphs.

MULTIPLIER

The $A_{11\text{-}0}$ and $B_{11\text{-}0}$ inputs to the LMS12 are captured at the rising edge of the clock in the 12-bit A and B input registers, respectively. These registers are independently enabled by the $\overline{ENA}$ and $\overline{ENB}$ inputs. The registered input data are then applied to a 12 x 12-bit multiplier array, which produces a 24-bit result. Both the inputs and outputs of the multiplier are in two's complement format. The multiplication result forms the input to the 24-bit product register.

SUMMER

The $C_{25\text{-}0}$ inputs to the LMS12 form a 26-bit two's complement number which is captured in the C register at the rising edge of the clock. The C register is enabled by assertion of the $\overline{ENC}$ input. The summer is a 26-bit adder which operates on the C register data and the sign extended contents of the product register to produce a 26-bit sum. This sum is applied to the 26-bit S register.

OUTPUT

The FTS input is the feedthrough control for the S register. When FTS is asserted, the summer result is applied directly to the S output port. When FTS is deasserted, data from the S register is output on the S port, effecting a one-cycle delay of the summer result. The S output port can be forced to a high-impedance state by driving the $\overline{OE}$ control line high. FTS would be asserted for conventional FIR filter applications, however the insertion of zero-coefficient filter taps may be accomplished by negating FTS. Negating FTS also allows application of the same filter transfer function to two interleaved datastreams with successive input and output sample points occurring on alternate clock cycles.

LMS12 BLOCK DIAGRAM

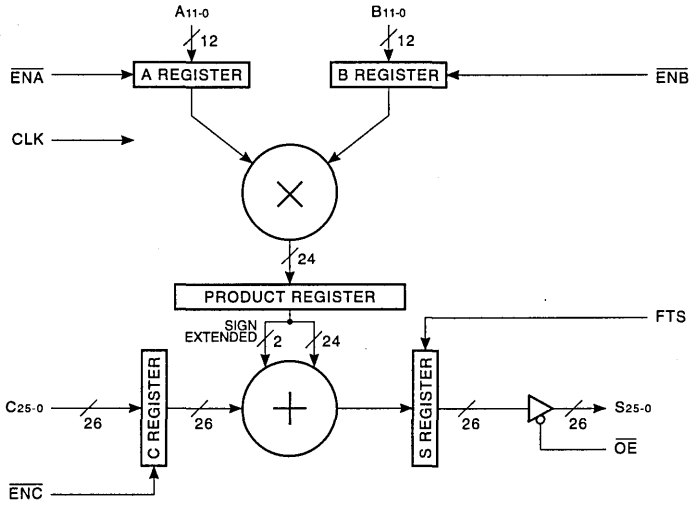
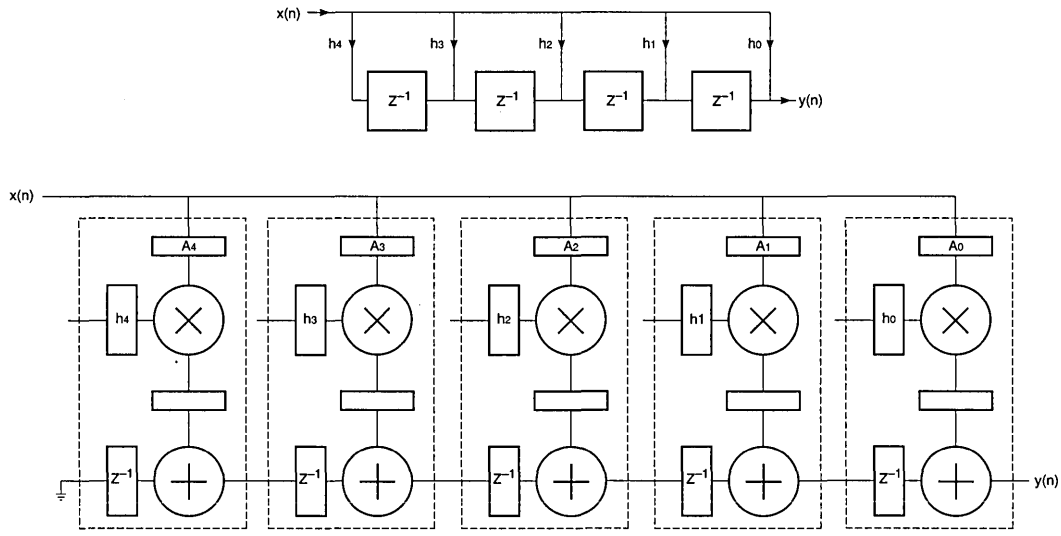


FIGURE 1. FLOW DIAGRAM FOR 5-TAP FIR FILTER



APPLICATIONS

The LMS12 is designed specifically for high-speed FIR filtering applications requiring a throughput rate of one output sample per clock period. By cascading LMS12 units, the transpose form of the FIR transfer function is implemented directly, with each of the LMS12 units supplying one of the filter weights, and the cascaded summers accumulating the results. The signal flow graph for a 5-tap FIR filter and the equivalent implementation using LMS12's is shown in Figure 1.

The operation of the 5-tap FIR filter implementation of Figure 1 is depicted in Table 1. The filter weights h4 - h0 are assumed to be latched in the B input registers of the LMS12 units. The x(n) data is applied in parallel to the A input registers of all devices. For descriptive purposes in the table, the A register contents and sum output data of each device is labelled according to the index of the weight applied by that device; i.e., S0 is produced by the rightmost device, which has h0 as its filter weight and A0 as its input register contents. Each column represents one clock cycle, with the data passing a particular point in the system illustrated across each row.

TABLE 1. TIMING EXAMPLE FOR 5-TAP NONDECIMATING FIR FILTER

CLK Cycle	1	2	3	4	5	6	7	8	9
X(n)	X_n	X_{n+1}	X_{n+2}	X_{n+3}	X_{n+4}	X_{n+5}	X_{n+6}	X_{n+7}	X_{n+8}
A_4 Register Sum 4		X_n	X_{n+1} h_4X_n	X_{n+2} h_4X_{n+1}	X_{n+3} h_4X_{n+2}	X_{n+4} h_4X_{n+3}	X_{n+5} h_4X_{n+4}	X_{n+6} h_4X_{n+5}	X_{n+7} h_4X_{n+6}
A_3 Register Sum 3		X_n	X_{n+1} h_3X_n $+h_4X_{n-1}$	X_{n+2} h_3X_{n+1} $+h_4X_n$	X_{n+3} h_3X_{n+2} $+h_4X_{n+1}$	X_{n+4} h_3X_{n+3} $+h_4X_{n+2}$	X_{n+5} h_3X_{n+4} $+h_4X_{n+3}$	X_{n+6} h_3X_{n+5} $+h_4X_{n+4}$	X_{n+7} h_3X_{n+6} $+h_4X_{n+5}$
A_2 Register Sum 2		X_n	X_{n+1} h_2X_n $+h_3X_{n-1}$ $+h_4X_{n-2}$	X_{n+2} h_2X_{n+1} $+h_3X_n$ $+h_4X_{n-1}$	X_{n+3} h_2X_{n+2} $+h_3X_{n+1}$ $+h_4X_n$	X_{n+4} h_2X_{n+3} $+h_3X_{n+2}$ $+h_4X_{n+1}$	X_{n+5} h_2X_{n+4} $+h_3X_{n+3}$ $+h_4X_{n+2}$	X_{n+6} h_2X_{n+5} $+h_3X_{n+4}$ $+h_4X_{n+3}$	X_{n+7} h_2X_{n+6} $+h_3X_{n+5}$ $+h_4X_{n+4}$
A_1 Register Sum 1		X_n	X_{n+1} h_1X_n $+h_2X_{n-1}$ $+h_3X_{n-2}$ $+h_4X_{n-3}$	X_{n+2} h_1X_{n+1} $+h_2X_n$ $+h_3X_{n-1}$ $+h_4X_{n-2}$	X_{n+3} h_1X_{n+2} $+h_2X_{n+1}$ $+h_3X_n$ $+h_4X_{n-1}$	X_{n+4} h_1X_{n+3} $+h_2X_{n+2}$ $+h_3X_{n+1}$ $+h_4X_n$	X_{n+5} h_1X_{n+4} $+h_2X_{n+3}$ $+h_3X_{n+2}$ $+h_4X_{n+1}$	X_{n+6} h_1X_{n+5} $+h_2X_{n+4}$ $+h_3X_{n+3}$ $+h_4X_{n+2}$	X_{n+7} h_1X_{n+6} $+h_2X_{n+5}$ $+h_3X_{n+4}$ $+h_4X_{n+3}$
A_0 Register Sum 0		X_n	X_{n+1} h_0X_n $+h_1X_{n-1}$ $+h_2X_{n-2}$ $+h_3X_{n-3}$ $+h_4X_{n-4}$	X_{n+2} h_0X_{n+1} $+h_1X_n$ $+h_2X_{n-1}$ $+h_3X_{n-2}$ $+h_4X_{n-3}$	X_{n+3} h_0X_{n+2} $+h_1X_{n+1}$ $+h_2X_n$ $+h_3X_{n-1}$ $+h_4X_{n-2}$	X_{n+4} h_0X_{n+3} $+h_1X_{n+2}$ $+h_2X_{n+1}$ $+h_3X_n$ $+h_4X_{n-1}$	X_{n+5} h_0X_{n+4} $+h_1X_{n+3}$ $+h_2X_{n+2}$ $+h_3X_{n+1}$ $+h_4X_n$	X_{n+6} h_0X_{n+5} $+h_1X_{n+4}$ $+h_2X_{n+3}$ $+h_3X_{n+2}$ $+h_4X_{n+1}$	X_{n+7} h_0X_{n+6} $+h_1X_{n+5}$ $+h_2X_{n+4}$ $+h_3X_{n+3}$ $+h_4X_{n+2}$

FIGURE 2A. INPUT FORMATS

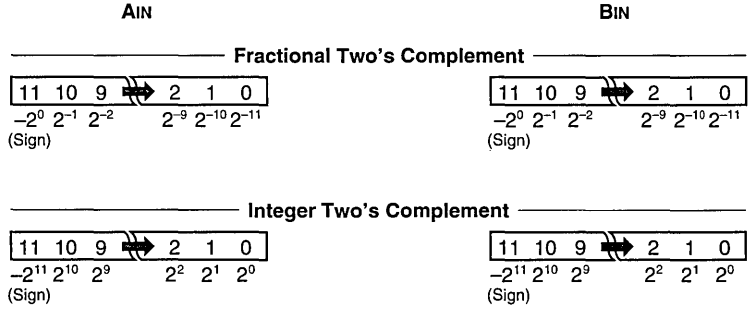
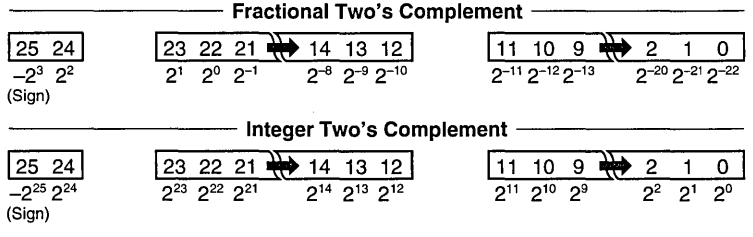


FIGURE 2B. OUTPUT FORMATS



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

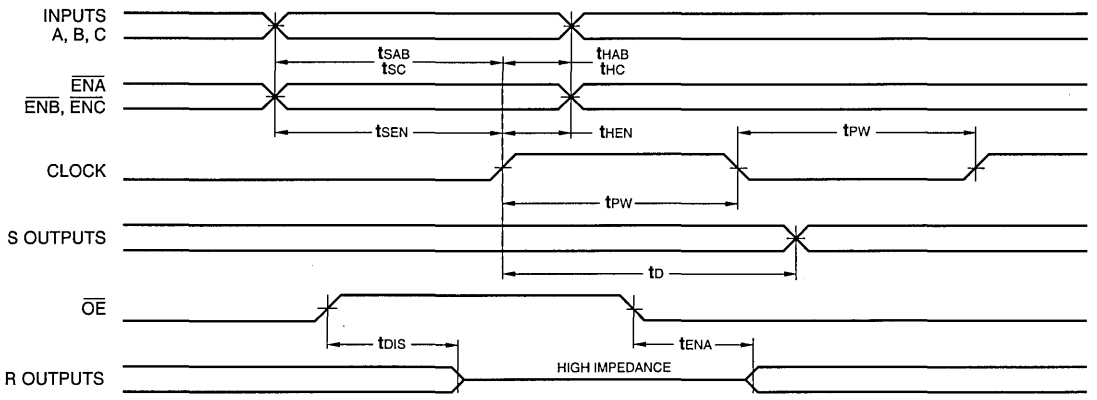
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		15	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMS12–							
		65		50		40		35	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CP}	Clock Period	40		35		30		25	
t_{PW}	Clock Pulse Width	15		15		12		8	
t_{SAB}	A, B, Data Setup Time	15		12		12		10	
t_{SC}	C Data Setup Time	15		10		7		7	
t_{SEN}	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Setup Time	15		12		12		10	
t_{HAB}	A, B, Data Hold Time	5		5		5		2	
t_{HC}	C Data Hold Time	5		5		5		2	
t_{HEN}	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Hold Time	5		5		5		2	
t_D	Clock to S–FT = 1		50		40		35		30
	Clock to S–FT = 0		25		25		25		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		22		22		22		20

SWITCHING WAVEFORMS

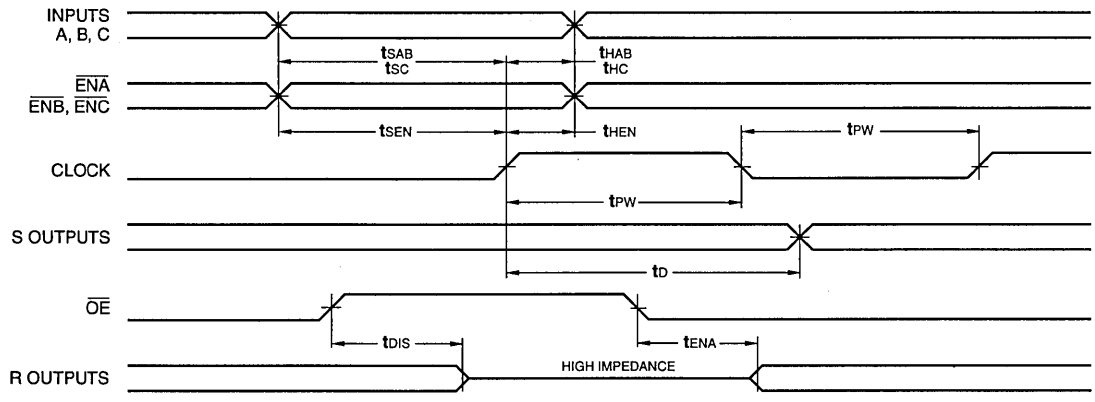


SWITCHING CHARACTERISTICS

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMS12–					
		65		50		40	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CP}	Clock Period	40		35		30	
t_{PW}	Clock Pulse Width	15		15		12	
t_{SAB}	A, B, Data Setup Time	15		15		12	
t_{SC}	C Data Setup Time	15		15		12	
t_{SEN}	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Setup Time	15		15		12	
t_{HAB}	A, B, Data Hold Time	5		5		5	
t_{HC}	C Data Hold Time	5		5		5	
t_{HEN}	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Hold Time	5		5		5	
t_D	Clock to S–FT = 1		50		45		35
	Clock to S–FT = 0		25		25		25
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		22		22		22

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

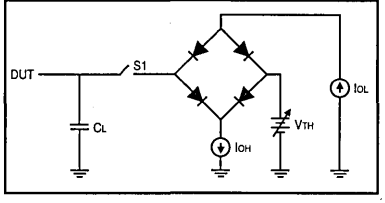
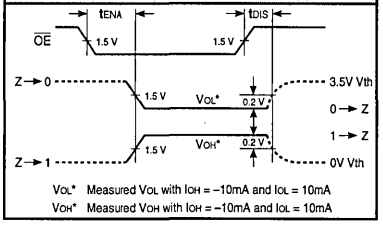


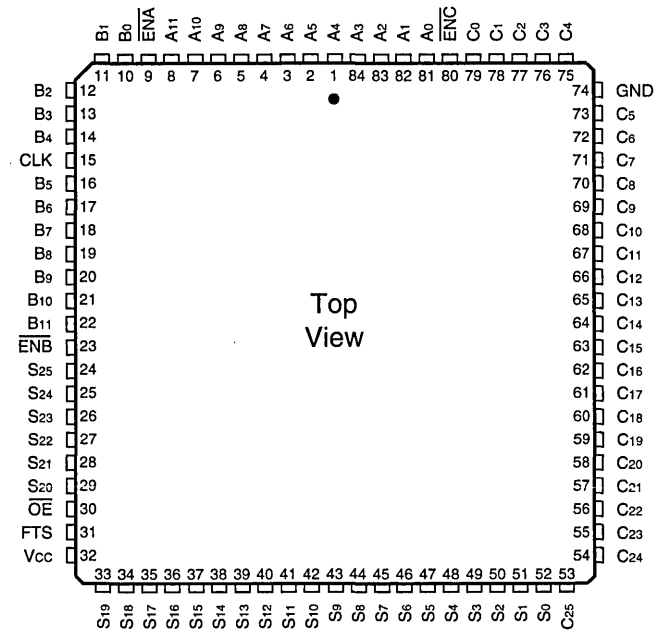
FIGURE B. THRESHOLD LEVELS



4

ORDERING INFORMATION

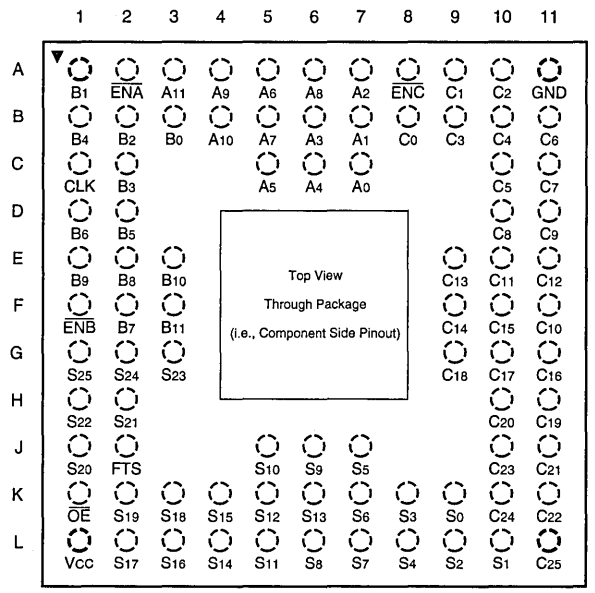
84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — COMMERCIAL SCREENING
65 ns	LMS12JC65
50 ns	LMS12JC50
40 ns	LMS12JC40
35 ns	LMS12JC35

ORDERING INFORMATION

84-pin



Speed	Ceramic Pin Grid Array (G3)
	0°C to +70°C — Commercial Screening
65 ns	LMS12GC65
50 ns	LMS12GC50
40 ns	LMS12GC40
35 ns	LMS12GC35
	–55°C to +125°C — Commercial Screening
65 ns	LMS12GM65
50 ns	LMS12GM50
40 ns	LMS12GM40
	–55°C to +125°C — MIL-STD-883 Compliant
65 ns	LMS12GMB65
50 ns	LMS12GMB50
40 ns	LMS12GMB40

Register Products

5

LOGIC DEVICES INCORPORATED

L29C520/521

4 x 8-bit Multilevel Pipeline Register

FEATURES

- Four 8-bit Registers
- Implements Double 2-Stage Pipeline or Single 4-Stage Pipeline Register
- Hold, Shift, and Load Instructions
- Separate Data In and Data Out Pins
- High-Speed, Low Power CMOS Technology
- Three-State Outputs
- DECC SMD No. 5962-91762
- Available 100% Screened to MIL-STD-883, Class B
- Replaces IDT29FCT520/IDT29FCT521 and AMD Am29520/Am29521
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Ceramic DIP
  - 28-pin Plastic LCC, J-Lead
  - 28-pin Ceramic LCC
  - 24-pin Ceramic Flatpack
  - 24-pin Plastic SSOP

DESCRIPTION

The **L29C520** and **L29C521** are pin-for-pin compatible with the IDT29FCT520/IDT29FCT521 and AMD Am29520/Am29521, implemented in low power CMOS.

The L29C520 and L29C521 contain four registers which can be configured as two independent, 2-level pipelines or as one 4-level pipeline.

The Instruction pins, I_{1-0}, control the loading of the registers. For either device, the registers may be configured as a four-stage delay line, with data loaded into R1 and shifted sequentially through R2, R3, and R4. Also, for the L29C520, data may be loaded from the inputs into either R1 or R3 with only R2 or R4 shifting. The L29C521 differs from the L29C520 in that R2 and R4 remain unchanged during this type of data load, as shown in Tables 1 and 2. Finally, I_{1-0} may be set to prevent any register from changing.

The S_{1-0} select lines control a 4-to-1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of the I and S controls allows simultaneous write and read operations on different registers.

TABLE 1. L29C520 INSTRUCTION TABLE

I_1	I_0	Description			
L	L	D→R1	R1→R2	R2→R3	R3→R4
L	H	HOLD	HOLD	D→R3	R3→R4
H	L	D→R1	R1→R2	HOLD	HOLD
H	H	ALL REGISTERS ON HOLD			

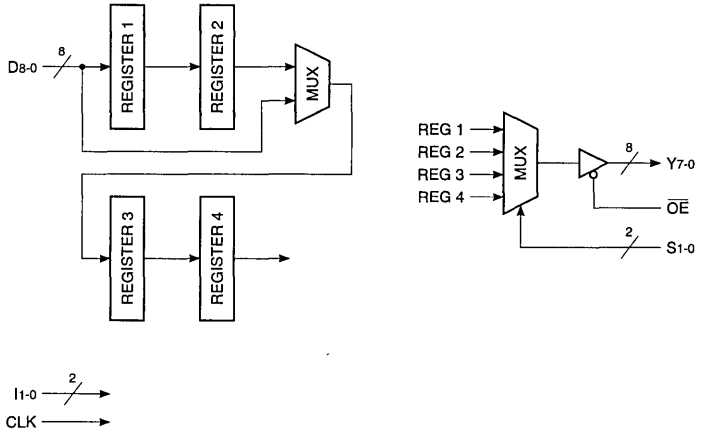
TABLE 2. L29C521 INSTRUCTION TABLE

I_1	I_0	Description			
L	L	D→R1	R1→R2	R2→R3	R3→R4
L	H	HOLD	HOLD	D→R3	HOLD
H	L	D→R1	HOLD	HOLD	HOLD
H	H	ALL REGISTERS ON HOLD			

TABLE 3. OUTPUT SELECT

S_1	S_0	Register Selected
L	L	Register 4
L	H	Register 3
H	L	Register 2
H	H	Register 1

L29C520/521 BLOCK DIAGRAM



5

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –15.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 24.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.5	mA

SWITCHING CHARACTERISTICS

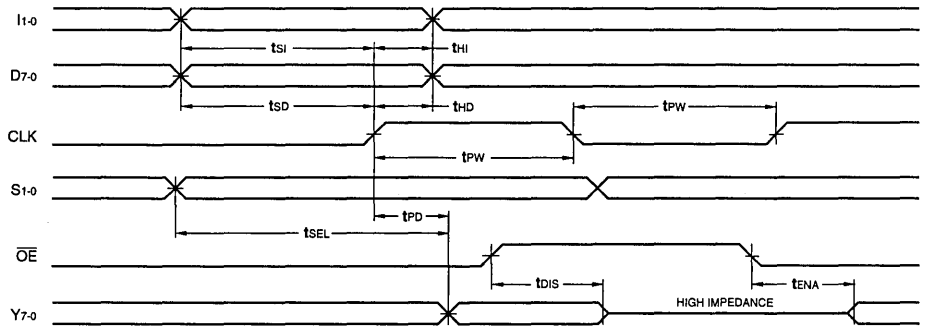
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L29C520/521–			
		22		14	
Symbol	Parameter	Min	Max	Min	Max
t_{PD}	Clock to Output Delay		22		14
t_{SEL}	Select to Output Delay		20		13
t_{PW}	Clock Pulse Width	10		7	
t_{SI}	Instruction Setup Time	10		5	
t_{HI}	Instruction Hold Time	3		1	
t_{SD}	Data Setup Time	10		5	
t_{HD}	Data Hold Time	3		1	
t_{ENA}	Three-State Output Enable Delay (Note 11)		21		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		12

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L29C520/521–					
		30		24		16	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PD}	Clock to Output Delay		30		24		16
t_{SEL}	Select to Output Delay		30		22		15
t_{PW}	Clock Pulse Width	15		10		8	
t_{SI}	Instruction Setup Time	15		10		6	
t_{HI}	Instruction Hold Time	5		3		2	
t_{SD}	Data Setup Time	15		10		6	
t_{HD}	Data Hold Time	5		3		2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		22		16
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		16		13

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

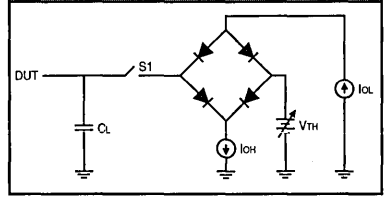
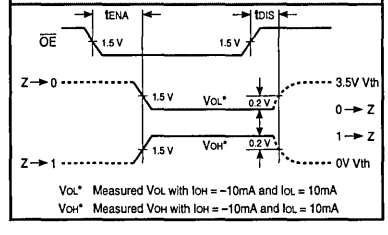
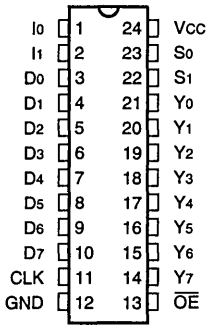


FIGURE B. THRESHOLD LEVELS

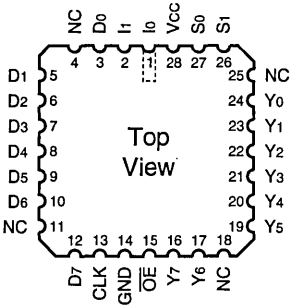


L29C520 — ORDERING INFORMATION

24-pin — 0.3" wide



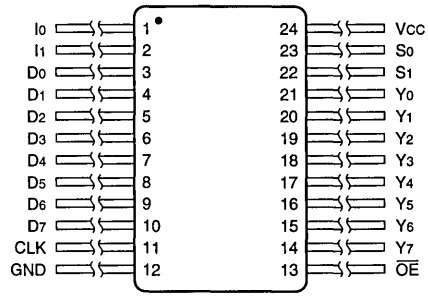
28-pin



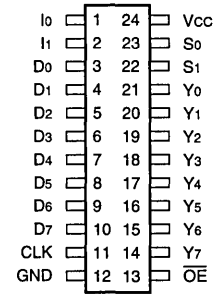
Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic J-Lead Chip Carrier (J4)	Ceramic Leadless Chip Carrier (K1)
	0°C to +70°C — COMMERCIAL SCREENING			
22 ns	L29C520PC22	L29C520CC22	L29C520JC22	L29C520KC22
14 ns	L29C520PC14	L29C520CC14	L29C520JC14	L29C520KC14
	–55°C to +125°C — COMMERCIAL SCREENING			
30 ns		L29C520CM30		L29C520KM30
24 ns		L29C520CM24		L29C520KM24
16 ns		L29C520CM16		L29C520KM16
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
30 ns		L29C520CMB30		L29C520KMB30
24 ns		L29C520CMB24		L29C520KMB24
16 ns		L29C520CMB16		L29C520KMB16

L29C520 — ORDERING INFORMATION

24-pin



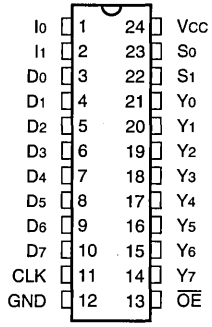
24-pin — 0.209" wide



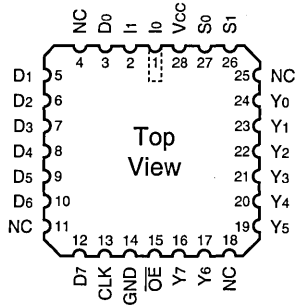
Speed	Ceramic Flatpack (M1)	Plastic SSOP (S1)
	0°C to +70°C — COMMERCIAL SCREENING	
22 ns		L29C520SC22
14 ns		L29C520SC14
	–55°C to +125°C — COMMERCIAL SCREENING	
	–55°C to +125°C — MIL-STD-883 COMPLIANT	
30 ns	L29C520MMB30	
24 ns	L29C520MMB24	
16 ns	L29C520MMB16	

L29C521 — ORDERING INFORMATION

24-pin — 0.3" wide



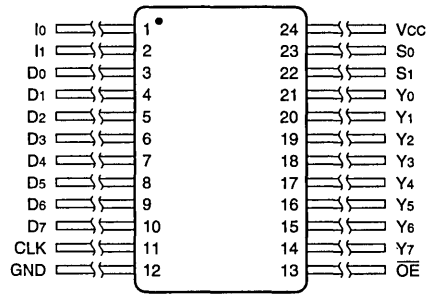
28-pin



Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic J-Lead Chip Carrier (J4)	Ceramic Leadless Chip Carrier (K1)
	0°C to +70°C — Commercial Screening			
22 ns	L29C521PC22	L29C521CC22	L29C521JC22	L29C521KC22
14 ns	L29C521PC14	L29C521CC14	L29C521JC14	L29C521KC14
	–55°C to +125°C — Commercial Screening			
30 ns		L29C521CM30		L29C521KM30
24 ns		L29C521CM24		L29C521KM24
16 ns		L29C521CM16		L29C521KM16
	–55°C to +125°C — MIL-STD-883 Compliant			
30 ns		L29C521CMB30		L29C521KMB30
24 ns		L29C521CMB24		L29C521KMB24
16 ns		L29C521CMB16		L29C521KMB16

L29C521 — ORDERING INFORMATION

24-pin



Speed	Ceramic Flatpack (M1)	
	0°C to +70°C — COMMERCIAL SCREENING	
	–55°C to +125°C — COMMERCIAL SCREENING	
	–55°C to +125°C — MIL-STD-883 COMPLIANT	
30 ns	L29C521MMB30	
24 ns	L29C521MMB24	
16 ns	L29C521MMB16	

LPR520
4 x 16-bit Multilevel Pipeline Register

FEATURES

- Four 16-bit Registers
- Implements Double 2-Stage Pipeline or Single 4-Stage Pipeline Register
- Hold, Shift, and Load Instructions
- Separate Data In and Data Out Pins
- High-Speed, Low Power CMOS Technology
- Three-State Outputs
- DECC SMD No. 5962-89716
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 40-pin Plastic DIP
  - 40-pin Ceramic DIP
  - 44-pin Plastic LCC, J-Lead
  - 44-pin Ceramic LCC

DESCRIPTION

The **LPR520** is functionally compatible with the L29C520 but have 16-bit inputs and outputs. The LPR520 is implemented in low power CMOS.

The LPR520 contains four registers which can be configured as two independent, 2-level pipelines or as one 4-level pipeline.

The Instruction pins, I_{1-0}, control the loading of the registers. The registers may be configured as a four-stage delay line, with data loaded into R1 and shifted sequentially through R2, R3, and R4. Also, data may be loaded from the inputs into either R1 or R3 with only R2 or R4 shifting. Finally, I_{1-0} may be set to prevent any register from changing.

The S_{1-0} select lines control a 4-to-1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of the I and S controls allows simultaneous write and read operations on different registers.

5

LPR520 Block Diagram

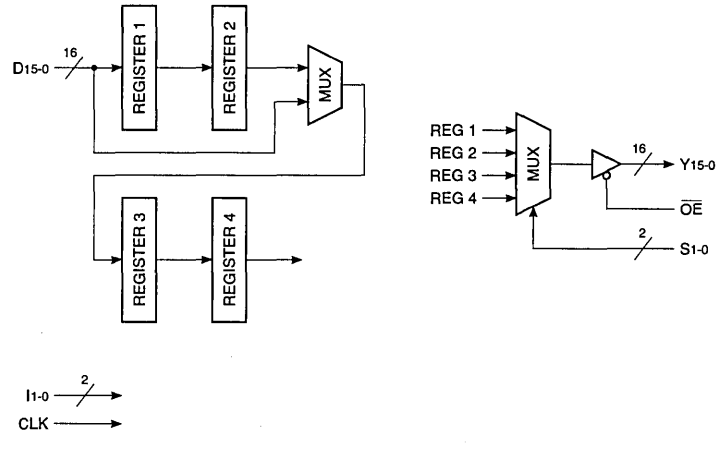


Table 1. LPR520 Instruction Table

I_1	I_0	Description
L	L	D→R1 R1→R2 R2→R3 R3→R4
L	H	HOLD HOLD D→R3 R3→R4
H	L	D→R1 R1→R2 HOLD HOLD
H	H	ALL REGISTERS ON HOLD

Table 2. Output Select

S_1	S_0	Register Selected
L	L	Register 4
L	H	Register 3
H	L	Register 2
H	H	Register 1

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	40	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

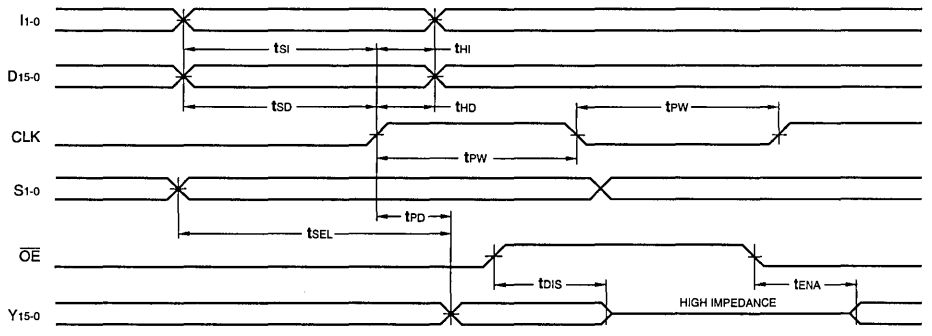
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LPR520–					
		25		22		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PD}	Clock to Output Delay		25		22		15
t_{SEL}	Select to Output Delay		25		20		15
t_{PW}	Clock Pulse Width	10		10		8	
t_{SI}	Instruction Setup Time	13		10		6	
t_{HI}	Instruction Hold Time	3		3		1	
t_{SD}	Data Setup Time	13		10		6	
t_{HD}	Data Hold Time	3		3		1	
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		21		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		15		12

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LPR520–					
		30		24		18	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PD}	Clock to Output Delay		30		24		18
t_{SEL}	Select to Output Delay		30		22		18
t_{PW}	Clock Pulse Width	15		10		9	
t_{SI}	Instruction Setup Time	15		10		8	
t_{HI}	Instruction Hold Time	5		3		2	
t_{SD}	Data Setup Time	15		10		8	
t_{HD}	Data Hold Time	5		3		2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		22		16
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		16		13

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

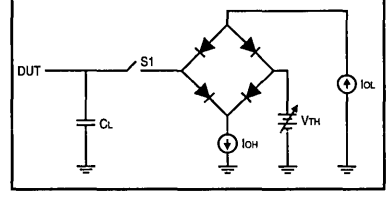
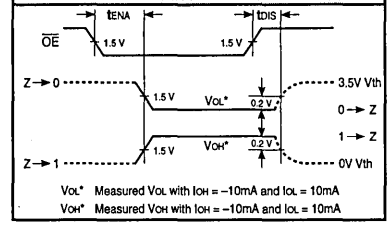
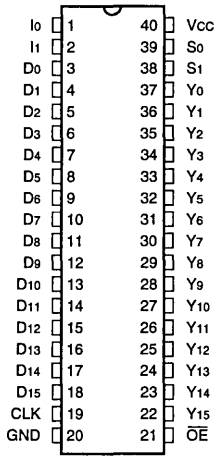


FIGURE B. THRESHOLD LEVELS

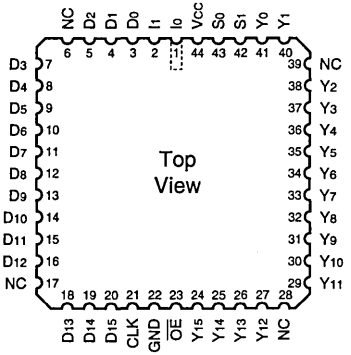


LPR520 — ORDERING INFORMATION

40-pin — 0.6" wide



44-pin



Speed	Plastic DIP (P3)	Ceramic DIP (C11)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — COMMERCIAL SCREENING			
25 ns	LPR520PC25		LPR520JC25	
22 ns	LPR520PC22		LPR520JC22	
15 ns	LPR520PC15		LPR520JC15	
	–55°C to +125°C — COMMERCIAL SCREENING			
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
30 ns		LPR520CMB30		LPR520KMB30
24 ns		LPR520CMB24		LPR520KMB24
18 ns		LPR520CMB18		LPR520KMB18

5

LPR200
16-bit Multilevel Pipeline Register

FEATURES

- Eight 16-bit High-Speed Pipeline Registers
- Programmable Multilevel Register Configurations
- Access time of 12 ns
- Hold, Shift, and Load Instructions
- Replaces IDT73200
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 48-pin Plastic DIP
  - 48-pin Sidebraze, Hermetic DIP
  - 52-pin Plastic LCC, J-Lead
  - 52-pin Ceramic LCC

DESCRIPTION

The **LPR200** is a programmable multilevel pipeline register. This device is pin-for-pin compatible with the IDT73200.

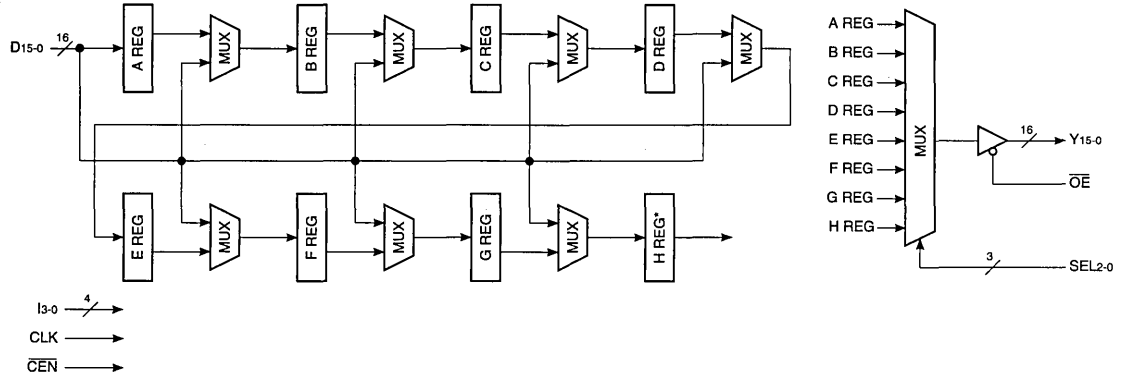
The LPR200 contains eight 16-bit high-speed pipeline registers which can be configured as eight independent, 1-level pipelines; four independent, 2-level pipelines; two independent, 4-level pipelines; or as one 8-level pipeline.

The Instruction pins, I_{3-0}, control the loading of the registers. The registers can be configured as an eight-stage delay line with data loaded into A and shifted sequentially through B, C, D, E, F, G and H as shown in Table 1. The Instruction pins may also be set to prevent any register from changing.

The Select lines, S_{2-0}, control an 8-to-1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of the I and S controls allow simultaneous write and read operations on different registers.

5

LPR200 BLOCK DIAGRAM



SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all registers.

Inputs

D15-0 — Data Input

16-bit data input port. Data is latched into the registers on the rising edge of CLK.

Outputs

Y15-0 — Data Output

16-bit data output port.

Controls

I3-0 — Instruction Control

The instruction control pins select which register operation will be carried out. Refer to Table 2.

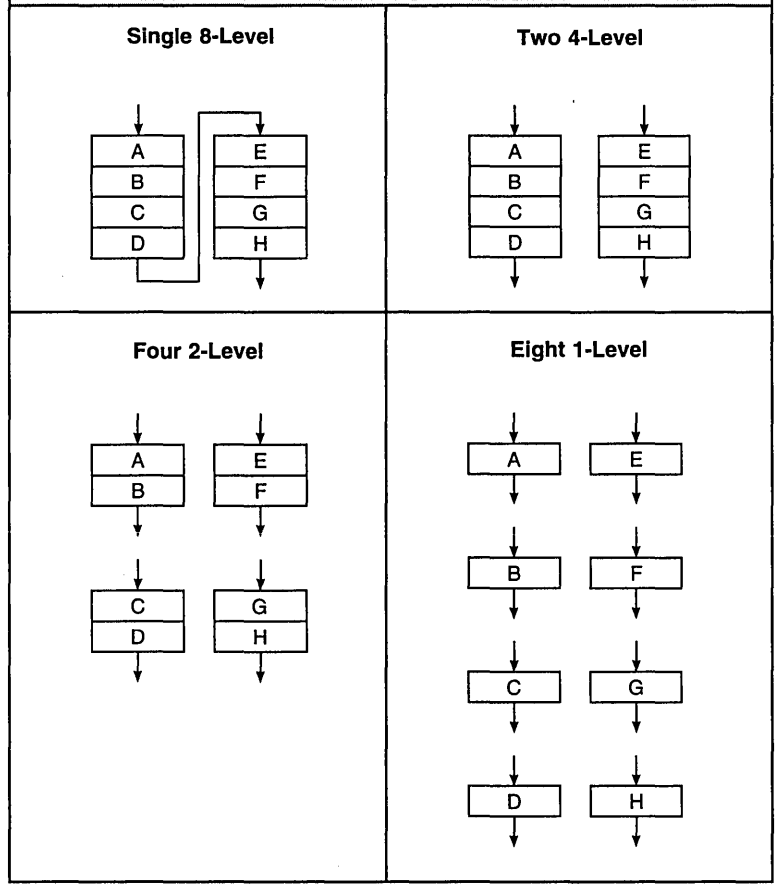
SEL2-0 — Output Select

The output select pins control which register contents will appear at the Y15-0 output pins. Refer to Table 3.

$\overline{CEN}$ — Clock Enable

When $\overline{CEN}$ is LOW, the instruction designated by I3-0 is performed on the registers. When $\overline{CEN}$ is HIGH, no register operations are performed.

TABLE 1. REGISTER LOAD OPERATIONS



$\overline{OE}$ — Output Enable

When $\overline{OE}$ is LOW, the register data specified by SEL2-0 is available on the Y15-0 output pins. When $\overline{OE}$ is HIGH, the output port is in a high-impedance state.

TABLE 2. LPR200 INSTRUCTION TABLE

Mnemonics	Inputs I_3	I_2	I_1	I_0	Description
LDA	0	0	0	0	$D_{15-0} \rightarrow A$
LDB	0	0	0	1	$D_{15-0} \rightarrow B$
LDC	0	0	1	0	$D_{15-0} \rightarrow C$
LDD	0	0	1	1	$D_{15-0} \rightarrow D$
LDE	0	1	0	0	$D_{15-0} \rightarrow E$
LDF	0	1	0	1	$D_{15-0} \rightarrow F$
LDG	0	1	1	0	$D_{15-0} \rightarrow G$
LDH	0	1	1	1	$D_{15-0} \rightarrow H$
LSHAH	1	0	0	0	$D_{15-0} \rightarrow A$ $A \rightarrow B$ $B \rightarrow C$ $C \rightarrow D$ $D \rightarrow E$ $E \rightarrow F$ $F \rightarrow G$ $G \rightarrow H$
LSHAD	1	0	0	1	$D_{15-0} \rightarrow A$ $A \rightarrow B$ $B \rightarrow C$ $C \rightarrow D$
LSHEH	1	0	1	0	$D_{15-0} \rightarrow E$ $E \rightarrow F$ $F \rightarrow G$ $G \rightarrow H$
LSHAB	1	0	1	1	$D_{15-0} \rightarrow A$ $A \rightarrow B$
LSHCD	1	1	0	0	$D_{15-0} \rightarrow C$ $C \rightarrow D$
LSHEF	1	1	0	1	$D_{15-0} \rightarrow E$ $E \rightarrow F$
LSHGH	1	1	1	0	$D_{15-0} \rightarrow G$ $G \rightarrow H$
HOLD	1	1	1	1	ALL REGISTERS ON HOLD

TABLE 3. LPR200 OUTPUT SELECT

SEL_2	SEL_1	SEL_0	Y_{15-0}
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D
1	0	0	E
1	0	1	F
1	1	0	G
1	1	1	H

5

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +155°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	50 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

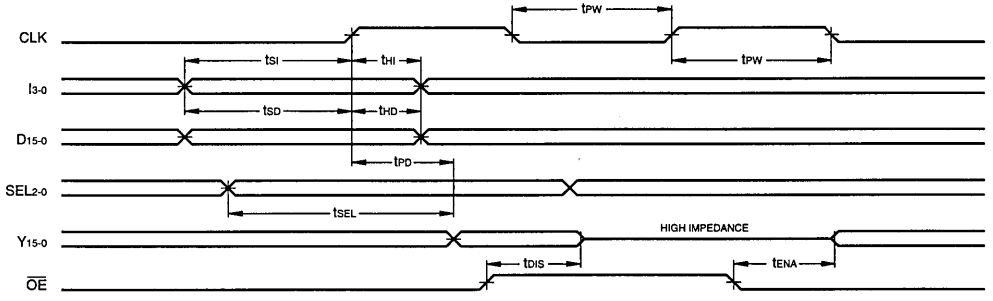
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –8.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 16 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	(Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)		2.0	10	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			12	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LPR200–					
		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	20		15		12	
t_{PW}	Clock Pulse Width	5		5		5	
t_{PD}	Clock to Output Delay		20		15		12
t_{SEL}	Select to Output Delay		20		15		12
t_{SI}	Instruction Setup Time	5		5		4	
t_{HI}	Instruction Hold Time	2		2		2	
t_{SD}	Data Setup Time	4		4		3	
t_{HD}	Data Hold Time	2		2		1	
t_{SC}	Clock Enable Setup Time	5		5		5	
t_{HC}	Clock Enable Hold Time	2		2		2	
t_{DIS}	Three-State Output Disable Delay (Note 11)		10		9		8
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		10		9

SWITCHING WAVEFORMS



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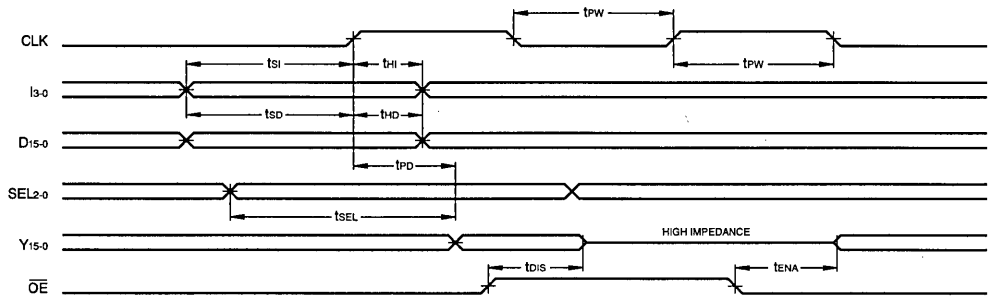
SWITCHING CHARACTERISTICS

MILITARY OPERATING RANGE (-55°C to +125°C) *Notes 9, 10 (ns)*

		LPR200–			
		20		15	
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	20		15	
t_{PW}	Clock Pulse Width	6		5	
t_{PD}	Clock to Output Delay		20		15
t_{SEL}	Select to Output Delay		20		15
t_{SI}	Instruction Setup Time	6		5	
t_{HI}	Instruction Hold Time	3		2	
t_{SD}	Data Setup Time	5		4	
t_{HD}	Data Hold Time	3		2	
t_{SC}	Clock Enable Setup Time	6		5	
t_{HC}	Clock Enable Hold Time	2		2	
t_{DIS}	Three-State Output Disable Delay (Note 11)		13		9
t_{ENA}	Three-State Output Enable Delay (Note 11)		13		10

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 10 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

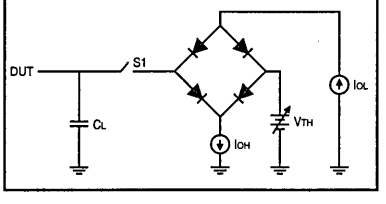
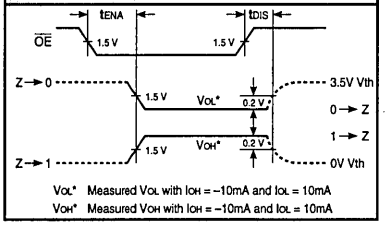


FIGURE B. THRESHOLD LEVELS



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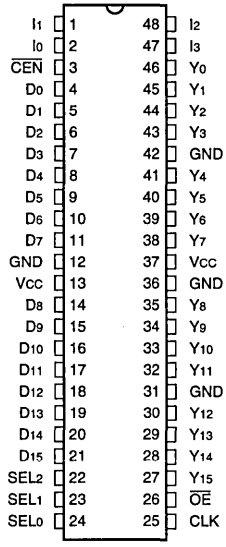
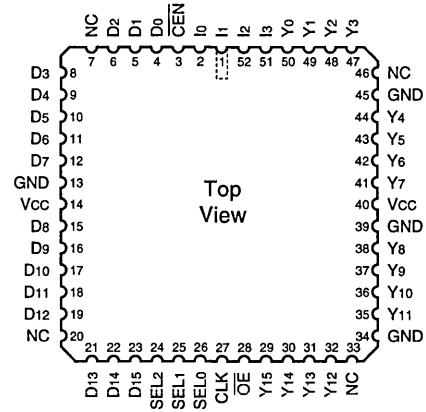
LPR200 — ORDERING INFORMATION

48-pin



52-pin



Speed	Plastic DIP (P5)	Sidebraze Hermetic DIP (D5)	Plastic Leaded Chip Carrier (J5)	Ceramic Leadless Chip Carrier (K10)
	0°C to +70°C — COMMERCIAL SCREENING			
20 ns	LPR200PC20		LPR200JC20	
15 ns	LPR200PC15		LPR200JC15	
12 ns	LPR200PC12		LPR200JC12	
	–55°C to +125°C — COMMERCIAL SCREENING			
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
20 ns		LPR200DMB20		LPR200KMB20
15 ns		LPR200DMB15		LPR200KMB15

L29C525
Dual Pipeline Register

FEATURES

- Dual 8-Deep Pipeline Register
- Configurable to Single 16-Deep
- Low Power CMOS Technology
- Replaces AMD Am29525
- Load, Shift, and Hold Instructions
- Separate Data In and Data Out Pins
- Three-State Outputs
- DECC SMD No. 5962-91696
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Ceramic DIP
  - 28-pin Plastic LCC, J-Lead
  - 28-pin Ceramic LCC

DESCRIPTION

The **L29C525** is a high-speed, low power CMOS pipeline register. It is pin-for-pin compatible with the AMD Am29525. The L29C525 can be configured as two independent 8-level pipelines or as a single 16-level pipeline. The configuration implemented is determined by the instruction code (I_{1-0}) as shown in Table 2.

The I_{1-0} instruction code controls the internal routing of data and loading of each register. For instruction I_{1-0} = 00 (Push A and B), data applied at the D_{7-0} inputs is latched into register A0 on the rising edge of CLK. The contents of A0 simultaneously move to register A1, A1 moves to A2, and so on. The contents of register A7 are wrapped back to register B0. The registers on the B side are similarly shifted, with the contents of register B7 lost.

Instruction I_{1-0} = 01 (Push B) acts similarly to the Push A and B instruction, except that only the B side registers are shifted. The input data is applied to register B0, and the contents of register B7 are lost. The contents of the A side registers are unaffected. Instruction I_{1-0} = 10 (Push A) is identical to the Push B instruction, except that the A side registers are shifted and the B side registers are unaffected.

Instruction I_{1-0} = 11 (Hold) causes no internal data movement. It is equivalent to preventing the application of a clock edge to any internal register.

The contents of any of the registers is selectable at the output through the use of the S_{3-0} control inputs. The independence of the I and S control lines allows simultaneous reading and writing. Encoding for the S_{3-0} controls is given in Table 3.

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L29C525 Block Diagram

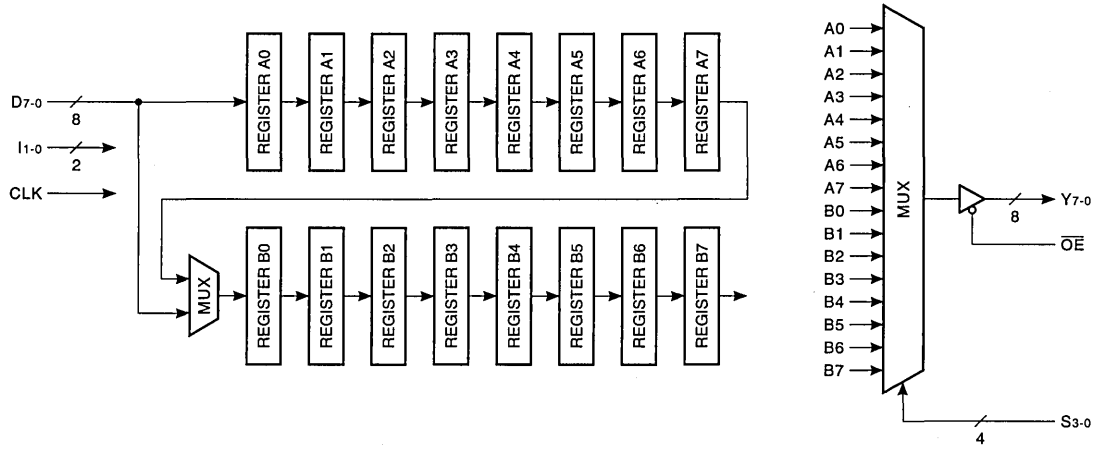


TABLE 1. REGISTER LOAD OPERATIONS

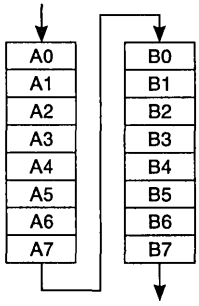
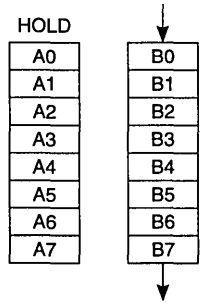
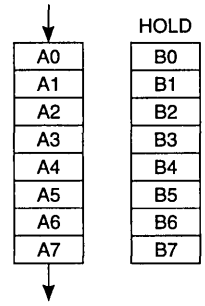
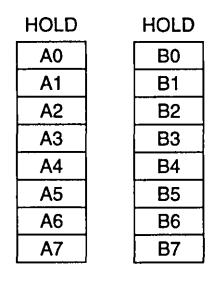
Single 16 Level	Dual 8 Level		
Push A and B	**Push B**	**Push A**	**Hold All Registers**
			

TABLE 2. INSTRUCTION SET

	Inputs		
Mnemonics	**I_1**	**I_0**	**Description**
Shift	0	0	Push A and B
LDB	0	1	Push B
LDA	1	0	Push A
HLD	1	1	Hold All Registers

TABLE 3. OUTPUT SELECT

S_3	S_2	S_1	S_0	Y_{7-0}
0	0	0	0	A0
0	0	0	1	A1
0	0	1	0	A2
0	0	1	1	A3
0	1	0	0	A4
0	1	0	1	A5
0	1	1	0	A6
0	1	1	1	A7
1	0	0	0	B0
1	0	0	1	B1
1	0	1	0	B2
1	0	1	1	B3
1	1	0	0	B4
1	1	0	1	B5
1	1	1	0	B6
1	1	1	1	B7

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

5

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –12 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 24 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	35	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

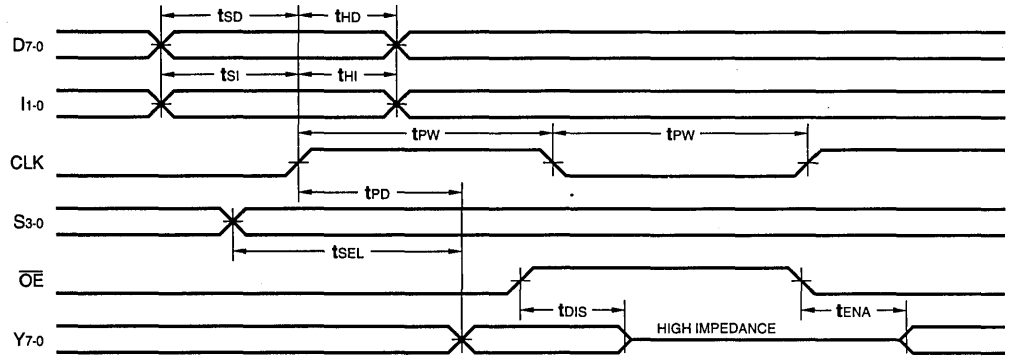
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C525– 20 Min	20 Max	15 Min	15 Max
t_{PD}	Clock to Output Delay		20		15
t_{SEL}	Select to Output Delay		20		15
t_{PW}	Clock Pulse Width	12		10	
t_{SD}	Data Setup Time	7		5	
t_{HD}	Data Hold Time	0		0	
t_{SI}	Instruction Setup Time	7		5	
t_{HI}	Instruction Hold Time	2		2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		13		13

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C525– 25 Min	25 Max	20 Min	20 Max
t_{PD}	Clock to Output Delay		25		20
t_{SEL}	Select to Output Delay		25		20
t_{PW}	Clock Pulse Width	12		12	
t_{SD}	Data Setup Time	7		7	
t_{HD}	Data Hold Time	2		2	
t_{SI}	Instruction Setup Time	7		7	
t_{HI}	Instruction Hold Time	2		2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		13		13

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

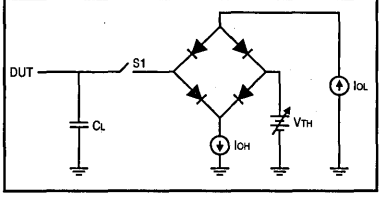
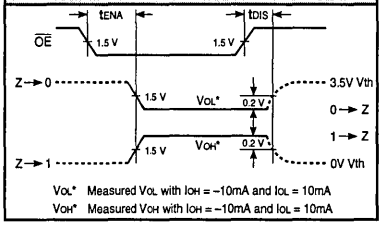


FIGURE B. THRESHOLD LEVELS



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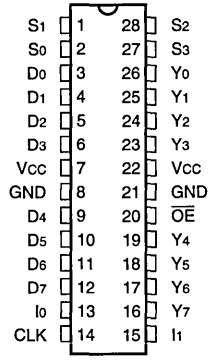
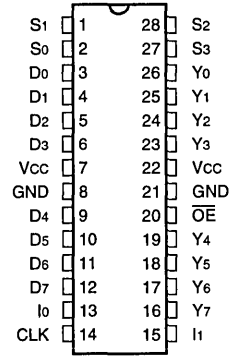
ORDERING INFORMATION

28-pin — 0.3" wide



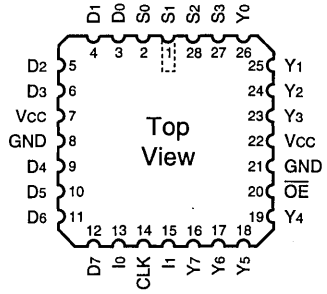
28-pin — 0.4" wide



Speed	Plastic DIP (P10)	Ceramic DIP (C5)	Ceramic DIP (C10)
	0°C to +70°C — Commercial Screening		
20 ns	L29C525PC20	L29C525CC20	L29C525IC20
15 ns	L29C525PC15	L29C525CC15	L29C525IC15
	–55°C to +125°C — Commercial Screening		
25 ns		L29C525CM25	L29C525IM25
20 ns		L29C525CM20	L29C525IM20
	–55°C to +125°C — MIL-STD-883 Compliant		
25 ns		L29C525CMB25	L29C525IMB25
20 ns		L29C525CMB20	L29C525IMB20

ORDERING INFORMATION

28-pin



Speed	Plastic J-Lead Chip Carrier (J4)	Ceramic Leadless Chip Carrier (K1)	
	0°C to +70°C — Commercial Screening		
20 ns 15 ns	L29C525JC20 L29C525JC15		
	–55°C to +125°C — Commercial Screening		
	–55°C to +125°C — MIL-STD-883 Compliant		
25 ns 20 ns		L29C525KMB25 L29C525KMB20	

L10C11
4/8-bit Variable Length Shift Register

FEATURES

- Variable Length 4 or 8-bit Wide Shift Register
- Selectable Delay Length from 3 to 18 Stages
- Low Power CMOS Technology
- Replaces TRW/Raytheon TMC2011
- Load, Shift, and Hold Instructions
- Separate Data In and Data Out Pins
- DECC SMD No. 5962-96793
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Ceramic DIP
  - 28-pin Plastic LCC, J-Lead
  - 28-pin Ceramic LCC

DESCRIPTION

The **L10C11** is a high-speed, low power CMOS variable length shift register. The L10C11 consists of two 4-bit wide, adjustable length shift registers. These registers share control signals and a common clock. Both shift registers can be programmed together to any length from 3 to 18 stages inclusive, or one register can be fixed at 18 stages of delay while the other is variable. The configuration implemented is determined by the Length Code (L_{3-0}) and the MODE control line as shown in Table 1.

Each input is applied to a chain of registers which are clocked on the rising edge of the common CLK input. These registers are numbered R1 through R17 and R1′ through R17′, corresponding to the D_{3-0} and D_{7-4} data fields respectively. A multiplexer serves to route the contents of any of registers R2 through R17 to the output register, denoted R18. A similar multiplexer operates on the contents of R2′ through R17′ to load R18′. Note that the minimum-length path from data inputs to outputs is R1 to R2 to R18, consisting of three stages of delay.

The MODE input determines whether one or both of the internal shift registers have variable length. When MODE = 0, both D_{3-0} and D_{7-4} are delayed by an amount which is controlled by L_{3-0}. When MODE = 1, the D_{7-4} field is delayed by 18 stages independent of L_{3-0}.

The Length Code (L_{3-0}) controls the number of stages of delay applied to the D inputs as shown in Table 1. When the Length Code is 0, the inputs are delayed by 3 clock periods. When the Length Code is 1, the delay is 4 clock periods, and so forth. The Length Code and MODE inputs are latched on the rising edge of CLK. Both the Length Code and MODE values may be changed at any time without affecting the contents of registers R1 through R17 or R1′ through R17′.

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L10C11 Block Diagram

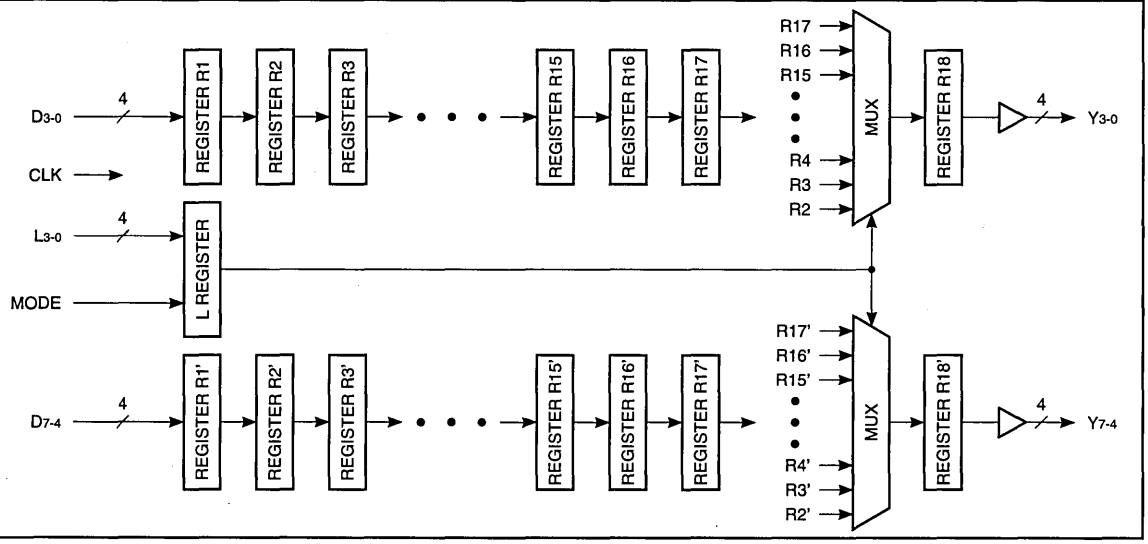

TABLE 1. CONTROL ENCODING

Length Code				Mode = 0		Mode = 1	
				Delay		Delay	
L_3	L_2	L_1	L_0	Y_{3-0}	Y_{7-4}	Y_{3-0}	Y_{7-4}
0	0	0	0	3	3	3	18
0	0	0	1	4	4	4	18
0	0	1	0	5	5	5	18
0	0	1	1	6	6	6	18
0	1	0	0	7	7	7	18
0	1	0	1	8	8	8	18
0	1	1	0	9	9	9	18
0	1	1	1	10	10	10	18
1	0	0	0	11	11	11	18
1	0	0	1	12	12	12	18
1	0	1	0	13	13	13	18
1	0	1	1	14	14	14	18
1	1	0	0	15	15	15	18
1	1	0	1	16	16	16	18
1	1	1	0	17	17	17	18
1	1	1	1	18	18	18	18

MAXIMUM RATINGS

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS

To meet specified electrical and switching characteristics

Mode	Temperature Range	Supply Voltage
Active Operation, Com.	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Mil.	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −12 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 24 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	20	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L10C11–					
		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PD}	Output Delay		25		20		15
t_{PW}	Clock Pulse Width	15		12		10	
t_{SD}	Data Setup Time	20		10		8	
t_{HD}	Data Hold Time	2		0		0	
t_{SL}	L_{3-0}, MODE Setup Time	20		10		8	
t_{HL}	L_{3-0}, MODE Hold Time	2		0		0	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L10C11–					
		30		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PD}	Output Delay		30		25		20
t_{PW}	Clock Pulse Width	15		12		12	
t_{SD}	Data Setup Time	25		10		10	
t_{HD}	Data Hold Time	2		2		0	
t_{SL}	L_{3-0}, MODE Setup Time	25		10		10	
t_{HL}	L_{3-0}, MODE Hold Time	2		2		0	

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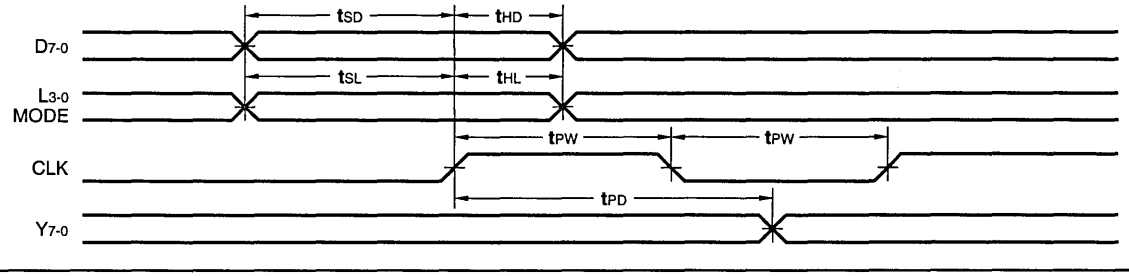
SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

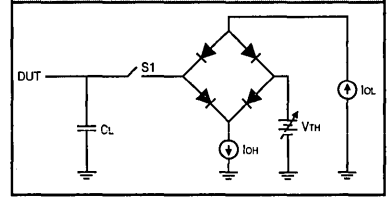
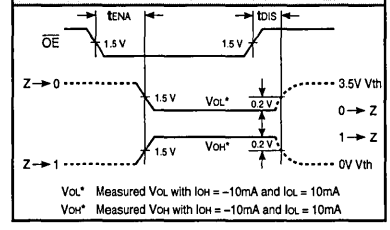
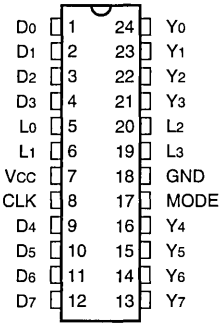


FIGURE B. THRESHOLD LEVELS

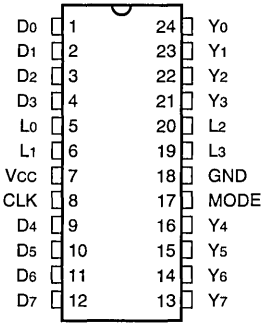


ORDERING INFORMATION

24-pin — 0.3" wide



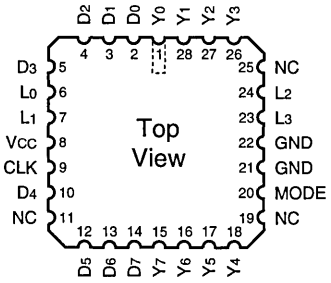
24-pin — 0.6" wide



Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic DIP (P1)
	0°C to +70°C — Commercial Screening		
25 ns	L10C11PC25	L10C11CC25	L10C11NC25
20 ns	L10C11PC20	L10C11CC20	L10C11NC20
15 ns	L10C11PC15	L10C11CC15	L10C11NC15
	–55°C to +125°C — Commercial Screening		
30 ns		L10C11CM30	
25 ns		L10C11CM25	
20 ns		L10C11CM20	
	–55°C to +125°C — MIL-STD-883 Compliant		
30 ns		L10C11CMB30	
25 ns		L10C11CMB25	
20 ns		L10C11CMB20	

ORDERING INFORMATION

28-pin



Speed	Plastic J-Lead Chip Carrier (J4)	Ceramic Leadless Chip Carrier (K1)
	0°C to +70°C — COMMERCIAL SCREENING	
25 ns	L10C11JC25	
20 ns	L10C11JC20	
15 ns	L10C11JC15	
	–55°C to +125°C — COMMERCIAL SCREENING	
	–55°C to +125°C — MIL-STD-883 COMPLIANT	
30 ns		L10C11KMB30
25 ns		L10C11KMB25
20 ns		L10C11KMB20

L21C11

8-bit Variable Length Shift Register

FEATURES

- Variable Length 8-bit Wide Shift Register
- Selectable Delay Length from 1 to 16 Stages
- Low Power CMOS Technology
- Replaces TRW/Raytheon TMC2111
- Load, Shift, and Hold Instructions
- Separate Data In and Data Out Pins
- DECC SMD No. 5962-96793
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Ceramic DIP
  - 28-pin Plastic LCC, J-Lead
  - 28-pin Ceramic LCC

DESCRIPTION

The **L21C11** is a high-speed, low power CMOS variable length shift register. It consists of a single 8-bit wide, adjustable length shift register. The shift register can be programmed to any length from 1 to 16 stages inclusive. The length of the shift register is determined by the Length Code (L_{3-0}) as shown in Table 1.

The data input is applied to a chain of registers which are clocked on the rising edge of the CLK input. These registers are numbered R1 through R15. A multiplexer serves to route the contents of any register, R1 through R15, or the data input, D_{7-0}, to the output register, denoted R16. Note that the minimum-length path from data input to output is through R16, consisting of a single stage of delay.

The Length Code (L_{3-0}) controls the number of delay stages applied to the D_{7-0} inputs as shown in Table 1. When the Length Code is 0, the input is delayed by 1 clock period. When the Length Code is 1, the delay is 2 clock periods, and so forth. The Length Code inputs are latched on the rising edge of CLK. The Length Code value may be changed at any time without affecting the contents of registers R1 through R15.

5

L21C11 BLOCK DIAGRAM

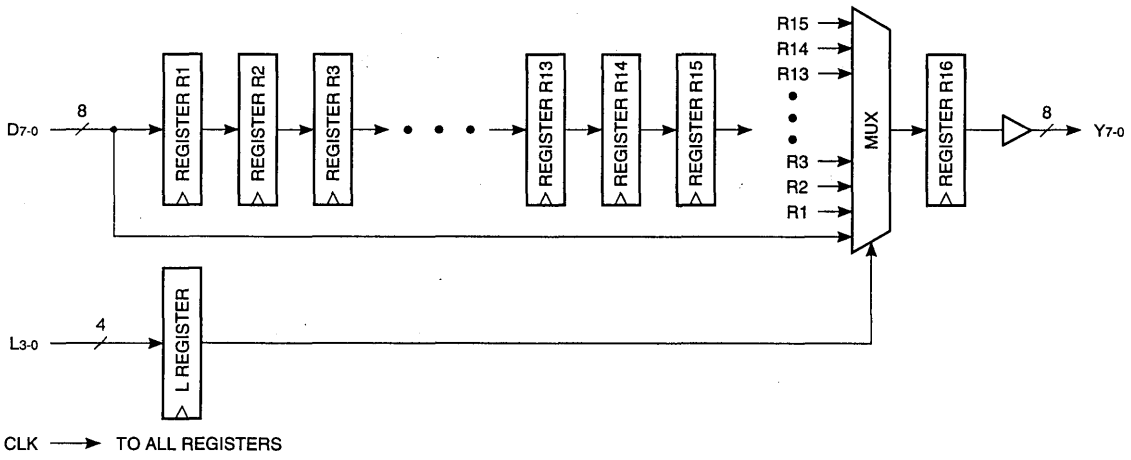


TABLE 1. CONTROL ENCODING

Length Code				Delay
L_3	L_2	L_1	L_0	Y_{7-0}
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

MAXIMUM RATINGS

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS

To meet specified electrical and switching characteristics

Mode	Temperature Range	Supply Voltage
Active Operation, Com.	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Mil.	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −12 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 24 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	20	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

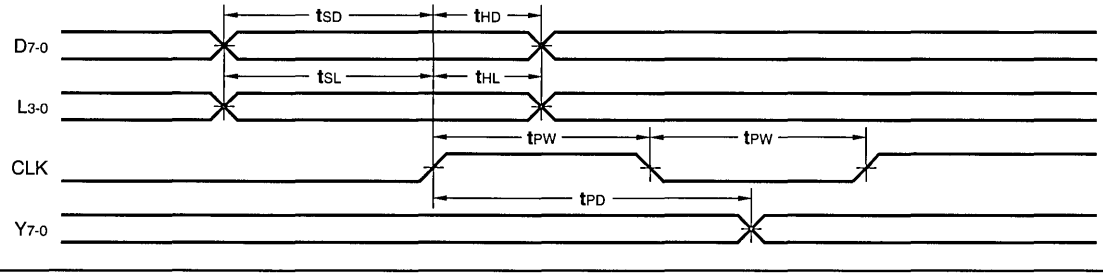
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L21C11–					
		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PD}	Output Delay		25		20		15
t_{PW}	Clock Pulse Width	15		12		10	
t_{SD}	Data Setup Time	20		10		8	
t_{HD}	Data Hold Time	2		0		0	
t_{SL}	Length Code Setup Time	20		10		8	
t_{HL}	Length Code Hold Time	2		0		0	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L21C11–					
		30		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PD}	Output Delay		30		25		20
t_{PW}	Clock Pulse Width	15		12		12	
t_{SD}	Data Setup Time	25		10		10	
t_{HD}	Data Hold Time	2		2		0	
t_{SL}	Length Code Setup Time	25		10		10	
t_{HL}	Length Code Hold Time	2		2		0	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

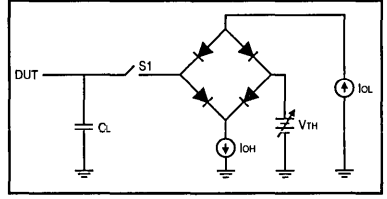
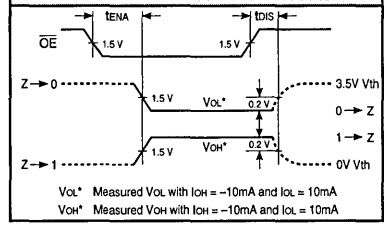
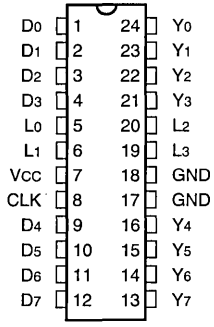


FIGURE B. THRESHOLD LEVELS

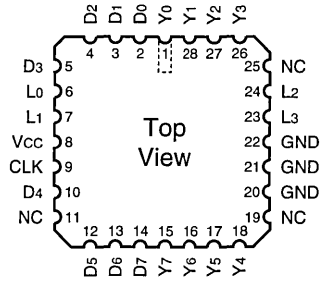


ORDERING INFORMATION

24-pin — 0.3" wide



28-pin



Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic J-Lead Chip Carrier (J4)	Ceramic Leadless Chip Carrier (K1)
	0°C to +70°C — Commercial Screening			
25 ns	L21C11PC25		L21C11JC25	
20 ns	L21C11PC20		L21C11JC20	
15 ns	L21C11PC15		L21C11JC15	
	–55°C to +125°C — Commercial Screening			
30 ns		L21C11CM30		
25 ns		L21C11CM25		
20 ns		L21C11CM20		
	–55°C to +125°C — MIL-STD-883 Compliant			
30 ns		L21C11CMB30		L21C11KMB30
25 ns		L21C11CMB25		L21C11KMB25
20 ns		L21C11CMB20		L21C11KMB20

L29C818
8-bit Serial Scan Shadow Register

FEATURES

- Octal Register with Additional 8-bit Shiftable Shadow Register
- Serial Load/Verify of Writable Control Store RAM
- Serial Stimulus/Observation of Sequential Logic
- High-Speed, Low Power CMOS Technology
- Replaces AMD Am29818
- DECC SMD No. 5962-90515
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Sidebraze, Hermetic DIP
  - 28-pin Ceramic LCC

DESCRIPTION

The **L29C818** is a high-speed octal register designed especially for applications using serial-scan diagnostics or writable control store. It is pin and functionally compatible with the AMD Am29818 bipolar device.

The L29C818 consists of an octal register, the P register, internally connected to an 8-bit shift register, the S register. Each has its own corresponding clock pin and the P register has a three-state output control.

An input control signal, MODE, in combination with the S register serial data input (SDI) pin controls data routing within the L29C818. When the MODE input is LOW, indicating normal operation, data present on the D_{7-0} pins is loaded into the P register on the rising edge of CLK P. The contents of the P register are visible on the output pins Y_{7-0} when the $\overline{OE}$ control line is LOW.

Also, data present on the SDI pin is loaded into the least significant position of the S register on the rising edge of CLK S. In this mode, the S register performs a right-shift operation with the contents of each bit position replaced by the value in the next least significant location. The value in S_7 is shifted out on the serial data output (SDO) pin. The SDI and SDO pins allow serial connection of multiple L29C818 devices into a diagnostic loop. When MODE is LOW, the operation of the P and S registers are completely independent and no timing relationship is enforced between CLK P and CLK S.

When MODE is HIGH, the internal multiplexers route data between the S and P registers and the Y port. The contents of the S register are loaded into the P register on the rising edge of

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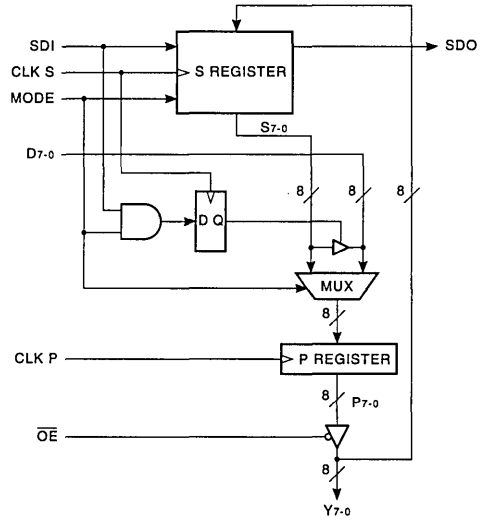
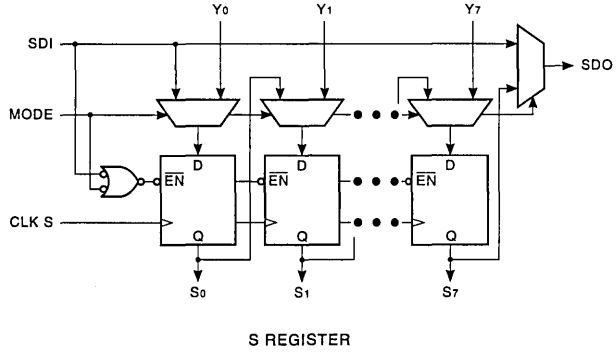
L29C818 Block Diagram





S REGISTER

CLK P. In diagnostic applications, this allows a data value input via serial scan to be loaded into the active data path of the machine.

When the MODE pin is HIGH, CLK S causes a parallel, rather than serial, load of the S register. In this mode, the S register is loaded from the Y_{7-0} pins at the rising edge of CLK S. This is useful in writable control store applications for read-back of the control store via the serial path.

When MODE is HIGH, the SDI pin is used as a control input to enable or disable the loading of the S register. It also affects routing of the S register contents onto the D_{7-0} outputs. When SDI is LOW, the S register is enabled for loading as above. When SDI is HIGH however, CLK S is prevented from reaching the S register and no load occurs. In order to allow the SDI pin to serve as an enable signal for all L29C818 devices in a serial configuration, special handling of the SDI input is required. When MODE is HIGH, the SDI input drives the SDO output directly, bypassing the S register. This means that the SDI value will apply simultaneously to all L29C818s in a serial loop. However, to ensure proper operation of a given device, the user must ensure that the SDI setup time to CLK S is extended by the sum of the SDI to SDO delays of all previous devices in the serial path.

The D_{7-0} port is normally used as the input port to the D register. For writable control store applications however, this port is connected to the I/O pins of the RAM used as a control store. In order to load this RAM through the serial path, it is necessary to drive the S register contents onto the D_{7-0} pins. This is accomplished when MODE and SDI are HIGH and a CLK S rising edge occurs. Note from above that with SDI HIGH, no loading of the S register occurs. However, a flip-flop is set which synchronously enables the D port output buffer. The D output remains enabled until the first rising edge of CLK S during which either SDI or MODE is LOW. Thus to load a control store RAM, data would be shifted in with MODE LOW. When an entire control store word is present in the serial S registers, the SDI and MODE pins are brought HIGH for one or more cycles, preventing further shifting of the S registers and enabling the contents onto the D port for writing into the RAM.

To verify the contents of a control store RAM, the RAM is read into the D register in the normal fashion. Then, the D contents are transferred in parallel to the S register by driving MODE HIGH with SDI LOW. The S register contents are then scanned out serially by returning MODE LOW and applying CLK S pulses.

TABLE 1. FUNCTION TABLE

Inputs				Outputs		Action		
MODE	SDI	CLK S	CLK P	P REG	S REG	Y_{7-0}	D_{7-0}	SDO
0	X	⎍	X	N/A	SHIFT	Normal	HI-Z	S_7
0	X	X	⎍	LOAD D	N/A	Normal	Input	S_7
1	0	⎍	X	N/A	LOAD Y	Input*	HI-Z	SDI
1	1	⎍	X	N/A	HOLD	Normal	Output	SDI
1	X	X	⎍	LOAD S	N/A	Normal	HI-Z	SDI

*If $\overline{OE}$ is LOW, the P register value will be loaded into the S register. If $\overline{OE}$ is HIGH, a value may be applied externally to the Y_{7-0} pins.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

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ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –12.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 24.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	15	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS — NORMAL REGISTER OPERATION

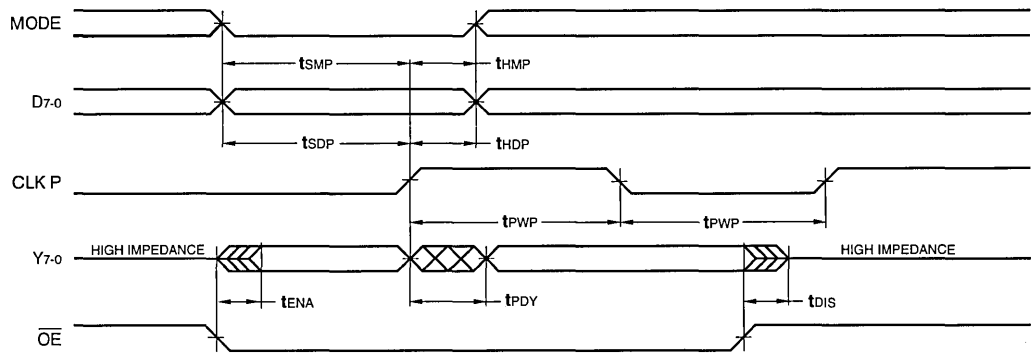
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L29C818–			
		25		15	
Symbol	Parameter	Min	Max	Min	Max
t_{PWP}	CLK P Pulse Width	15		10	
t_{PDY}	CLK P to Y_{7-0}		13		9
t_{SDP}	D_{7-0} to CLK P Setup Time	8		6	
t_{HDP}	CLK P to D_{7-0} Hold Time	2		2	
t_{SMP}	MODE to CLK P Setup Time	15		15	
t_{HMP}	CLK P to MODE Hold Time	2		2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L29C818–			
		30		24	
Symbol	Parameter	Min	Max	Min	Max
t_{PWP}	CLK P Pulse Width	15		15	
t_{PDY}	CLK P to Y_{7-0}		18		12
t_{SDP}	D_{7-0} to CLK P Setup Time	10		8	
t_{HDP}	CLK P to D_{7-0} Hold Time	2		2	
t_{SMP}	MODE to CLK P Setup Time	15		15	
t_{HMP}	CLK P to MODE Hold Time	2		2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		30		30
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		20

SWITCHING WAVEFORMS — NORMAL REGISTER OPERATION



SWITCHING CHARACTERISTICS — SERIAL SHIFT OPERATION

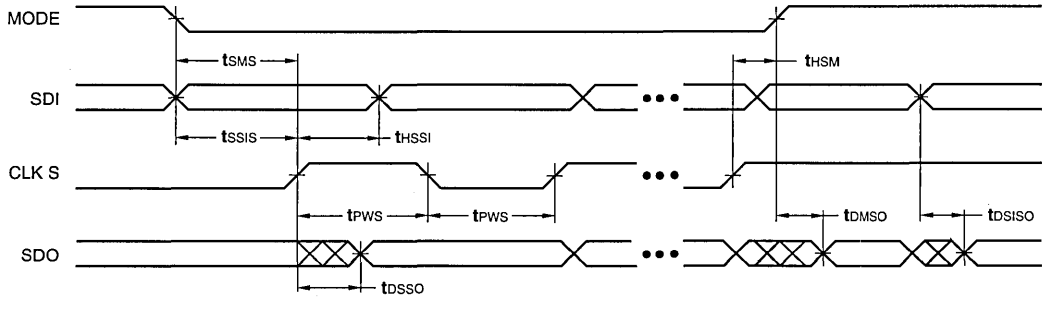
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L29C818–			
		25		15	
Symbol	Parameter	Min	Max	Min	Max
t_{PWS}	CLK S Pulse Width	25		15	
t_{DSSO}	CLK S to SDO		25		25
t_{SSIS}	SDI to CLK S Setup Time	10		10	
t_{HSSI}	CLK S to SDI Hold Time	0		0	
t_{SMS}	MODE to CLK S Setup Time	12		12	
t_{HSM}	CLK S to MODE Hold Time	2		2	
t_{DMSO}	MODE to SDO	16		16	
t_{DSISO}	SDI to SDO	16		15	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L29C818–			
		30		24	
Symbol	Parameter	Min	Max	Min	Max
t_{PWS}	CLK S Pulse Width	25		25	
t_{DSSO}	CLK S to SDO		30		30
t_{SSIS}	SDI to CLK S Setup Time	12		12	
t_{HSSI}	CLK S to SDI Hold Time	0		0	
t_{SMS}	MODE to CLK S Setup Time	12		12	
t_{HSM}	CLK S to MODE Hold Time	5		5	
t_{DMSO}	MODE to SDO	18		18	
t_{DSISO}	SDI to SDO	18		18	

SWITCHING WAVEFORMS — SERIAL SHIFT OPERATION



SWITCHING CHARACTERISTICS — PIPELINE LOAD FROM SHADOW

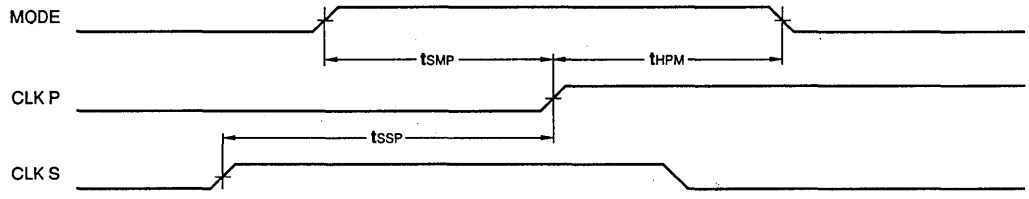
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818– 25 Min	25 Max	15 Min	15 Max
t_{SMP}	MODE to CLK P	15		15	
t_{HPM}	CLK P to MODE Hold Time	2		2	
t_{SSP}	CLK S to CLK P	10		10	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818– 30 Min	30 Max	24 Min	24 Max
t_{SMP}	MODE to CLK P	15		15	
t_{HPM}	CLK P to MODE Hold Time	2		2	
t_{SSP}	CLK S to CLK P	15		15	

SWITCHING WAVEFORMS — PIPELINE LOAD FROM SHADOW



SWITCHING CHARACTERISTICS — SHADOW LOAD FROM Y PORT

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L29C818–			
		25		15	
Symbol	Parameter	Min	Max	Min	Max
t_{SYS}	Y_{7-0} to CLK S Setup Time	5		5	
t_{HSY}	CLK S to Y_{7-0} Hold Time	5		5	
t_{SMS}	MODE to CLK S Setup Time	12		12	
t_{HSM}	CLK S to MODE Hold Time	2		2	
t_{SSIS}	SDI to CLK S Setup Time	10		10	
t_{HSSI}	CLK S to SDI Hold Time	0		0	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L29C818–			
		30		24	
Symbol	Parameter	Min	Max	Min	Max
t_{SYS}	Y_{7-0} to CLK S Setup Time	5		5	
t_{HSY}	CLK S to Y_{7-0} Hold Time	5		5	
t_{SMS}	MODE to CLK S Setup Time	12		12	
t_{HSM}	CLK S to MODE Hold Time	5		5	
t_{SSIS}	SDI to CLK S Setup Time	12		12	
t_{HSSI}	CLK S to SDI Hold Time	0		0	

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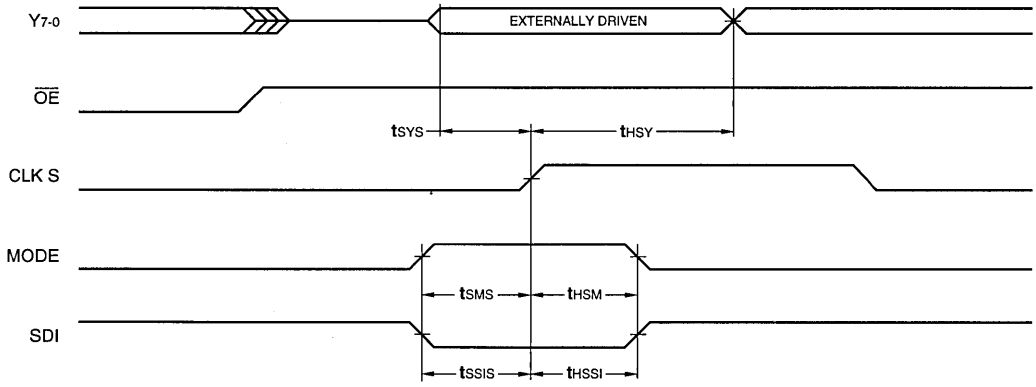
SWITCHING WAVEFORMS — SHADOW LOAD FROM Y PORT



SWITCHING CHARACTERISTICS — SHADOW READ VIA D PORT

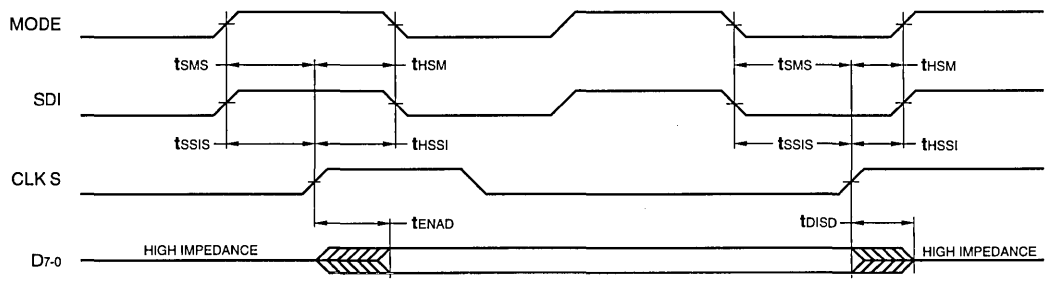
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818– 25 Min	25 Max	15 Min	15 Max
t_{SMS}	MODE to CLK S Setup Time	12		12	
t_{HSM}	CLK S to MODE Hold Time	2		2	
t_{SSIS}	SDI to CLK S Setup Time	10		10	
t_{HSSI}	CLK S to SDI Hold Time	0		0	
t_{ENAD}	CLK S to D_{7-0} Enable Delay (Note 11)	85		80	
t_{DISD}	CLK S to D_{7-0} Disable Delay (Note 11)	30		25	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818– 30 Min	30 Max	24 Min	24 Max
t_{SMS}	MODE to CLK S Setup Time	12		12	
t_{HSM}	CLK S to MODE Hold Time	5		5	
t_{SSIS}	SDI to CLK S Setup Time	12		12	
t_{HSSI}	CLK S to SDI Hold Time	0		0	
t_{ENAD}	CLK S to D_{7-0} Enable Delay (Note 11)	90		90	
t_{DISD}	CLK S to D_{7-0} Disable Delay (Note 11)	35		35	

SWITCHING WAVEFORMS — SHADOW READ VIA D PORT



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

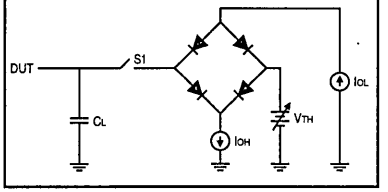
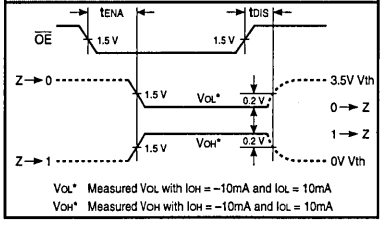


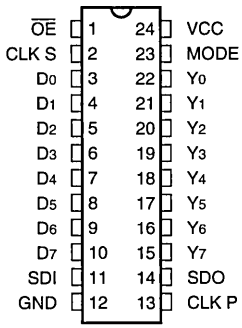
FIGURE B. THRESHOLD LEVELS



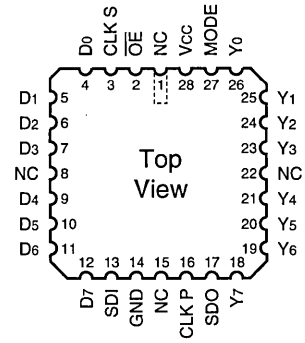
5

ORDERING INFORMATION

24-pin — 0.3" wide



28-pin



Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	Ceramic Leadless Chip Carrier (K1)
	0°C to +70°C — COMMERCIAL SCREENING		
25 ns 15 ns	L29C818PC25 L29C818PC15		
	–55°C to +125°C — COMMERCIAL SCREENING		
30 ns 24 ns			
	–55°C to +125°C — MIL-STD-883 COMPLIANT		
30 ns 24 ns		L29C818DMB30 L29C818DMB24	L29C818KMB30 L29C818KMB24

Peripheral Products

L5380/53C80
SCSI Bus Controller

FEATURES

- Asynchronous Transfer Rate Up to 4 Mbytes/sec
- Low Power CMOS Technology
- Replaces NCR 5380/53C80/ 53C80-40 and AMD Am5380/ 53C80
- On-Chip SCSI Bus Drivers
- Supports Arbitration, Selection/ Reselection, Initiator or Target Roles
- Programmed or DMA I/O, Handshake or Wait State DMA Interlock
- DECC SMD No.
  5962-90548 — L53C80
- Package Styles Available:
  - 40/48-pin Plastic DIP
  - 48-pin Sidebraze, Hermetic DIP
  - 44-pin Plastic LCC, J-Lead

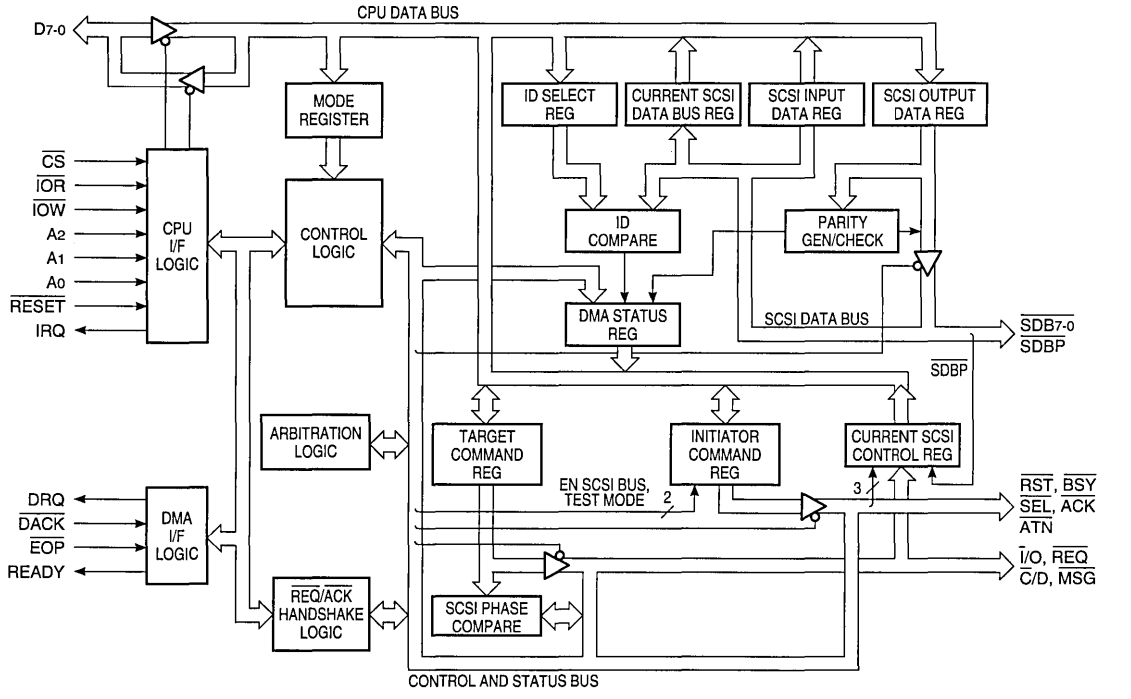
DESCRIPTION

The **L5380/53C80** are high performance SCSI bus controllers which support the physical layer of the SCSI (Small Computer System Interface) bus as defined by the ANSI X3T9.2 committee. It is pin and functionally compatible with the NMOS NCR5380, while offering up to a 2.5x performance improvement, 10x power reduction, and lower cost. Replacement of the NMOS 5380 by the LOGIC Devices L5380/53C80 will result in an immediate transfer rate improvement due to $\overline{REQ}/\overline{ACK}$ and $DRQ/\overline{DACK}$ handshake response times up to 5 times faster than previous devices. While remaining firmware compatible with the NCR5380, the L5380/53C80 provides bug fixes and state machine enhancements allowing even larger throughput gains for new designs.

The L5380/53C80 supports asynchronous data transfer between initiator and target at up to 4 Mbytes/sec. It operates in either initiator or target roles and offers a choice of programmed I/O (direct microprocessor manipulation of handshake) or any of several DMA modes (autonomous handshake and data transfer operations). The L5380/53C80 has internal hardware to support arbitration and can monitor and generate interrupts for a variety of error conditions. It provides extensive bus status monitoring features and includes buffers capable of directly driving a terminated SCSI bus for a compact implementation.

6

L5380/53C80 BLOCK DIAGRAM



PIN DEFINITIONS

A. SCSI Bus

$\overline{SDB7\text{-}0}$ — SCSI DATA BUS 7–0

Bidirectional/Active low. The 8-bit SCSI data bus is defined by these pins. $\overline{SDB7}$ is the most significant bit. During arbitration phase, these lines contain the SCSI ID numbers of all initiators arbitrating for the SCSI bus; $\overline{SDB7}$ represents the initiator with the highest priority. During the selection/reselection phase, these lines contain the ID number of the device that won the arbitration along with the ID number of the device to be selected/reselected.

$\overline{SDBP}$ — SCSI DATA BUS PARITY

Bidirectional/Active low. $\overline{SDBP}$ is the parity bit of the SCSI data bus. Odd parity is used, meaning that the total number of ones on the bus, including the parity bit, is odd. Parity is always generated when sending information, however checking for parity errors when receiving information is a user option. Parity is not valid during arbitration phase.

$\overline{SEL}$ — SELECT

Bidirectional/Active low. $\overline{SEL}$ is asserted by the initiator to select a target. It is also asserted by the target when reselecting it as an initiator.

$\overline{BSY}$ — BUSY

Bidirectional/Active low. $\overline{BSY}$ is asserted to indicate that the SCSI bus is active.

$\overline{ACK}$ — ACKNOWLEDGE

Bidirectional/Active low. $\overline{ACK}$ is asserted by the initiator during any information transfer phase in response to assertion of $\overline{REQ}$ by the target. Similarly, $\overline{ACK}$ is deasserted after $\overline{REQ}$ becomes inactive. These two signals form the data transfer handshake between the initiator and target. Data is latched by the target on the lowgoing edge of $\overline{ACK}$ for target receive operations.

$\overline{ATN}$ — ATTENTION

Bidirectional/Active low. $\overline{ATN}$ is asserted by the initiator after successful selection of a target, to indicate an intention to send a message to the target. The target responds to $\overline{ATN}$ by entering the MESSAGE OUT phase.

$\overline{RST}$ — SCSI BUS RESET

Bidirectional/Active low. $\overline{RST}$ when active indicates a SCSI bus reset condition.

$\overline{I}/O$ — INPUT/OUTPUT

Bidirectional/Active low. $\overline{I}/O$ is controlled by the target and specifies the direction of information transfer. When $\overline{I}/O$ is asserted, the direction of transfer is to the initiator. $\overline{I}/O$ is also asserted by the target during RESELECTION phase to distinguish it from SELECTION phase.

$\overline{C}/D$ — CONTROL/DATA

Bidirectional/Active low. $\overline{C}/D$ is controlled by the target and when asserted, indicates CONTROL (command or status) information is on the SCSI data bus. DATA is specified when $\overline{C}/D$ is deasserted.

$\overline{MSG}$ — MESSAGE

Bidirectional/Active low. $\overline{MSG}$ is controlled by the target, and when asserted indicates MESSAGE phase.

$\overline{REQ}$ — REQUEST

Bidirectional/Active low. $\overline{REQ}$ is asserted by the target to begin the handshake associated with transfer of a byte over the SCSI data bus. $\overline{REQ}$ is deasserted upon receipt of $\overline{ACK}$ from the initiator. Data is latched by the initiator on the lowgoing edge of $\overline{REQ}$ for initiator receive operations.

B. Microprocessor Bus

$\overline{CS}$ — CHIP SELECT

Input/Active low. This signal enables reading or writing of the internal registers by the microprocessor, using memory mapped I/O. An alternate method for reading selected registers is available for DMA.

DRQ — DMA REQUEST

Output/Active high. This signal is used to indicate that the L5380/53C80 is ready to execute the next cycle of a DMA transfer on the microprocessor bus. For send operations, it indicates that the output data register is ready to receive the next byte from the DMA controller or CPU. For receive operations, it indicates that the input data register contains the next byte to be read by the DMA controller or CPU.

IRQ — INTERRUPT REQUEST

Output/Active high. The L5380/53C80 asserts this signal to indicate to the microprocessor that one of the several interrupt conditions have been met. These include SCSI bus fault conditions as well as other events requiring microprocessor intervention. Most interrupt types are individually maskable.

$\overline{IOR}$ — I/O READ

Input/Active low. $\overline{IOR}$ is used in conjunction with $\overline{CS}$ and $A_{2\text{-}0}$ to execute a memory mapped read of a L5380/53C80 internal register. It is also used in conjunction with $\overline{DACK}$ to execute a DMA read of the SCSI Input Data Register.

READY — READY

Output/Active high. Ready is used rather than DRQ as an alternate method for controlling DMA data transfer. This DMA type is termed blockmode DMA and must be specifically enabled by the CPU. In block-

mode DMA, data is throttled by treating the L5380/53C80 as wait state memory. I/O (DMA) cycles are initiated at the maximum rate sustainable by the DMA controller/memory subsystem, but all cycles are extended (wait-states inserted) until READY is asserted by the L5380/53C80. This is generally the fastest DMA method since memory subsystem addressing can be overlapped with SCSI operations (flyby mode).

$\overline{DACK}$ — DMA ACKNOWLEDGE

Input/Active low. $\overline{DACK}$ is used in conjunction with $\overline{IOR}$ or $\overline{IOW}$ to enable reading or writing of the SCSI Input and Output Data Registers when in DMA mode. $\overline{DACK}$ resets DRQ and must not occur simultaneously with $\overline{CS}$.

$\overline{EOP}$ — END OF PROCESS

Input/Active low. This input is used to indicate to the L5380/53C80 that a DMA transfer is to be concluded. The L5380/53C80 can automatically generate an interrupt in response to receiving $\overline{EOP}$ from the DMA controller.

$\overline{RESET}$ — CPU BUS RESET

Input/Active low. This input clears all internal registers and state machines. It does not result in assertion of the $\overline{RST}$ signal on the SCSI bus and therefore affects only the local L5380/53C80 and not other devices on the bus.

$\overline{IOW}$ — I/O WRITE

Input/Active low. $\overline{IOW}$ is used in conjunction with $\overline{CS}$ and A2-0 to execute a memory mapped write of a L5380/53C80 internal register. It is also used in conjunction with $\overline{DACK}$ to execute a DMA write of the SCSI Output Data Register.

A2-0 — ADDRESS 2-0

Inputs/Active high. These signals, in conjunction with $\overline{CS}$, $\overline{IOR}$, and $\overline{IOW}$, address the L5380/53C80 internal registers for CPU read/write operations.

D7-0 — DATA 7-0

Bidirectional/Active high. These signals are the microprocessor data bus. D7 is the most significant bit.

L5380/53C80 INTERNAL REGISTERS

Overview

The L5380/53C80 contains registers that are directly addressed by the microprocessor. These registers allow for monitoring of SCSI bus activity, controlling the operation of the L5380/53C80, and determining the cause of interrupts. In many cases, a read-only and a write-only register are mapped to the same address. Some addresses are dummy registers which are used to implement a control operation but do not correspond to a physical register. The state of the CPU data bus when writing or reading these dummy registers is 'don't care'. Tables 1 and 3 show the address and name of each register as well as bit definitions.

Register Descriptions

A. Write Operations

The following paragraphs give detailed descriptions of the function of each bit in the L5380/53C80 internal registers for write operations as shown in Table 1.

WRITE ADDRESS 0
Output Data Register

The Output Data Register is a write-only register used for sending information to the SCSI data bus. During arbitration, the arbitrating SCSI device asserts its ID via this register. The device which wins arbitration also asserts the "OR" of its ID and the ID of the target/initiator to be selected/reselected. In programmed I/O mode this register is written using $\overline{CS}$ and $\overline{IOW}$ with A2-0 = 000. In DMA mode, it is written when $\overline{IOW}$ and $\overline{DACK}$ are simultaneously active, irrespective of the state of the address lines. Note that a "1" written to the Output Data Register becomes a low state when asserted on the active-low SCSI bus.

WRITE ADDRESS 1
Initiator Command Register

The Initiator Command Register is a read/write register which allows CPU control of the SCSI signals asserted by the initiator. Some bits in this register are not readable, and these positions are mapped to status bits useful in monitoring the progress of arbitration. These, along with the initiation of system-wide reset and test functions, may also be of use to the target.

R1 Bit 7 — Assert $\overline{RST}$

When this bit is set, the L5380/53C80 asserts the $\overline{RST}$ line on the SCSI bus, initializing all devices on the bus to the reset condition. All logic and internal registers of the L5380/53C80 are reset, except for the Assert RST bit itself, the Testmode bit (R1 bit 6) and the IRQ (interrupt request) latch. The IRQ pin becomes active indicating a SCSI bus reset interrupt. This interrupt is not maskable.

R1 Bit 6 — Testmode

When this bit is set, the L5380/53C80 places all outputs, including both SCSI and CPU signals, in a high impedance state. This effectively removes the device from the system as an aid to system diagnostics. Note that internal registers may still be written to while in Testmode. The L5380/53C80 returns to normal operation when Testmode is reset. The Testmode bit is reset by either writing a "0" to R1 bit 6

or via the $\overline{RESET}$ (CPU reset) pin. Testmode is not affected by the $\overline{RST}$ (SCSI bus reset) signal, or by the Assert $\overline{RST}$ bit in the Initiator Command Register (R1 bit 7).

R1 Bit 5 — Not Used

R1 Bit 4 — Assert $\overline{ACK}$

When this bit is set, $\overline{ACK}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{ACK}$. Note that $\overline{ACK}$ will be asserted only if the Targetmode bit (R2 bit 6) is reset, indicating that the L5380/53C80 is acting as an initiator.

R1 Bit 3 — Assert $\overline{BSY}$

When this bit is set, $\overline{BSY}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{BSY}$. $\overline{BSY}$ is asserted to indicate that the device has been selected or reselected, and deasserting $\overline{BSY}$ causes a bus free condition.

R1 Bit 2 — Assert $\overline{SEL}$

When this bit is set, $\overline{SEL}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{SEL}$. $\overline{SEL}$ is normally asserted after a successful arbitration.

R1 Bit 1 — Assert $\overline{ATN}$

When this bit is set, $\overline{ATN}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{ATN}$. $\overline{ATN}$ is asserted by the initiator to request message out phase. Note that $\overline{ATN}$ will be asserted only if the Targetmode bit (R2 bit 6) is reset, indicating that the L5380/53C80 is acting as an initiator.

R1 Bit 0 — Assert Data Bus

When this bit is set, the open drain SCSI data bus and parity drivers are enabled and the contents of the Output Data Register are driven onto the SCSI data lines. In addition to the Assert Data Bus bit, enabling of the SCSI bus drivers requires one of the following two sets of conditions:

When the L5380/53C80 is operating as an initiator, the Targetmode bit (R2 bit 6) must be reset, the $\overline{I}$/O pin must be negated (initiator to target transfer) and no phase mismatch condition can exist. A phase mismatch occurs when the $\overline{MSG}$, $\overline{C}$/D, and $\overline{I}$/O bits of the Target Command Register (R3) do not match the corresponding SCSI control lines.

When the L5380/L53C80 is operating as a target, the Targetmode bit will be set, and in this case Assert Data Bus will enable the outputs unconditionally.

The Assert Data Bus bit need not be set for arbitration to occur; when the Arbitrate bit (R2 bit 0) is set, and a bus free condition is detected, the data bus will be enabled for arbitration regardless of the state of the Assert Data Bus bit.

Finally, note that the Testmode bit (R1 bit 6) overrides all other controls, including Assert Data Bus and Arbitrate, and disables all outputs.

WRITE ADDRESS 2
Mode Register

The Mode register is a read/write register which provides control over several aspects of L5380/53C80 operation. Programmed I/O or two different types of DMA transfer may be selected, initiator or target device operation is accommodated, and parity checking and interrupts may be enabled via this register. The function of each individual bit is described as follows:

R2 Bit 7 — Blockmode

This bit must be used in conjunction with DMA Mode (R2 bit 1). It is used to select the type of handshake desired between the L5380/53C80 and the external DMA controller. See "L5380/53C80 Data Transfers" for a complete discussion of the transfer types supported.

R2 Bit 6 — Targetmode

When this bit is set, the L5380/53C80 will operate as a SCSI target device. This enables the SCSI signals $\overline{I}$/O, $\overline{C}$/D, $\overline{MSG}$, and $\overline{REQ}$ to be asserted.

When Targetmode is reset, the device will operate as an initiator. This enables the SCSI signals $\overline{ATN}$ and $\overline{ACK}$ to be asserted. Targetmode also affects state machine operation for DMA transfers and the conditions necessary for enabling the SCSI Data bus drivers. (See Assert Databus, R1 bit 0).

R2 Bit 5 — Enable Parity Check

When this bit is set, information received on the SCSI data bus is checked for odd parity. The Parity Error latch will be set whenever data is received under DMA control or the Current SCSI Data Register (Read Register 0) is read by the CPU. The state of the Parity Error latch can be determined by reading R5 bit 5, and it can be reset by a read to Address 7. Note that ENABLE PARITY CHECK must be set if parity error interrupts are to be generated. This interrupt can be separately masked by the Enable Parity Interrupt bit (R2 bit 4) while retaining the state of the Parity Error latch for later examination by the CPU.

R2 Bit 4 — Enable Parity Interrupt

When this bit is set, the L5380/53C80 will set the interrupt request latch, and assert IRQ (interrupt request) if it detects a parity error. Enable Parity Check (R2 bit 5) must also be set if parity error interrupts are desired.

R2 Bit 3 — Enable End Of DMA Interrupt

When this bit is set, the L5380/53C80 will set the interrupt request latch, and assert IRQ (interrupt request) if it detects a valid $\overline{EOP}$ (End of Process) signal. $\overline{EOP}$ is normally generated by a DMA controller to indicate the end of a DMA transfer. $\overline{EOP}$ is valid only when coincident with $\overline{IOR}$ or $\overline{IOW}$ and $\overline{DACK}$.

R2 Bit 2 — Monitor Busy

When this bit is set, the L5380/53C80 continuously monitors the state of the $\overline{BSY}$ signal. Absence of $\overline{BSY}$ for a period longer than 400 ns (but less than 1200 ns) will cause the L5380/53C80 to set the BSYERR and IRQ (interrupt request) latches. In addition, the six least significant bits of the Initiator Command Register are reset, and all SCSI data and control outputs are disabled until the BSYERR latch is reset. This effectively disconnects the L5380/53C80 from the SCSI bus in response to an unexpected disconnect by another device. It also allows the CPU to be interrupted when the SCSI bus becomes free in systems where arbitration is not used and an $\overline{EOP}$ signal is not available.

R2 Bit 1 — DMA Mode

When this bit is set, the L5380/53C80's internal state machines automatically control the SCSI signals $\overline{REQ}$ and $\overline{ACK}$ (as appropriate for initiator or target operation) and the CPU signals DRQ and READY. DMA Mode must be set prior to starting a DMA transfer in either direction. The DMA Mode bit is reset whenever a bus free condition is detected ($\overline{BSY}$ is not active). This aborts DMA operations when a loss of $\overline{BSY}$ occurs, regardless of the state of the Monitor Busy bit (R2 bit 2.) The DMA Mode bit is not reset when $\overline{EOP}$ is received, but must be specifically reset by the CPU. $\overline{EOP}$ does, however, inhibit additional DMA cycles from occurring.

R2 Bit 0 — Arbitrate

This bit is set to indicate a desire to arbitrate for use of the SCSI bus. Before setting the Arbitrate bit, the SCSI Output Data Register (Write Register 0) must be written with the SCSI ID assigned to the arbitrating SCSI device. The bit position of register R0 which is set represents the priority number of the SCSI device, with bit 7 the highest priority. See the section on "Arbitration" for a full discussion of the L5380/53C80 arbitration procedure.

TABLE 1. WRITE REGISTERS

Address 0 — Output Data Register

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 1 — Initiator Command Register

7	6	5	4	3	2	1	0
ASSERT $\overline{RST}$	TEST MODE		ASSERT $\overline{ACK}$	ASSERT $\overline{BSY}$	ASSERT $\overline{SEL}$	ASSERT $\overline{ATN}$	ASSERT DATA BUS

Address 2 — Mode Register

7	6	5	4	3	2	1	0
BLOCK MODE	TARGET MODE	ENABLE PARITY CHECK	ENABLE PARITY INT'RPT	ENABLE EODMA INT'RPT	MONI-TOR BUSY	DMA MODE	ARBI-TRATE

Address 3 — Target Command Register

7	6	5	4	3	2	1	0
LAST BYTE SENT				ASSERT $\overline{REQ}$	ASSERT $\overline{MSG}$	ASSERT $\overline{C}$/D	ASSERT $\overline{I}$/O

Address 4 — ID Select Register

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 5 — Start DMA Send

7	6	5	4	3	2	1	0

Address 6 — Start DMA Target Receive

7	6	5	4	3	2	1	0

Address 7 — Start DMA Initiator Receive

7	6	5	4	3	2	1	0

WRITE ADDRESS 3
Target Command Register

The Target Command Register is a read/write register which allows CPU control of the SCSI signals asserted by the target. In addition, this register contains a read-only status flag useful in unambiguously determining when the last byte of a DMA transfer has actually been sent over the SCSI bus.

When operating as an initiator with DMA mode set, the Assert $\overline{MSG}$, Assert $\overline{C}/D$, and Assert $\overline{I}/O$ bits are used as a template to compare against the corresponding SCSI control signals provided by the target. A phase mismatch interrupt will be generated on the falling edge of the $\overline{REQ}$ input if the template does not match the state of the signals. Therefore the CPU should initialize these bits to the phase of the expected data transfer. An interrupt, then, will signal an intent by the target to change to a new phase. The SCSI information transfer phases and their associated direction of data transfer are given in Table 2.

R3 Bits 7-4 — Not Used

R3 Bit 3 — Assert $\overline{REQ}$

When this bit is set, $\overline{REQ}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{REQ}$. Note that $\overline{REQ}$ will be asserted only if the Targetmode bit (R2 bit 6) is set, indicating that the L5380/53C80 is acting as a target.

R3 Bit 2 — Assert $\overline{MSG}$

When this bit is set, $\overline{MSG}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{MSG}$. Note that $\overline{MSG}$ will be asserted only if the Targetmode bit (R2 bit 6) is set, indicating that the L5380/53C80 is acting as a target. When operating as an initiator, this bit is compared against the $\overline{MSG}$ input, and an interrupt is generated if they differ at the falling edge of $\overline{REQ}$.

R3 Bit 1 — Assert $\overline{C}/D$

When this bit is set, $\overline{C}/D$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{C}/D$. Note that $\overline{C}/D$ will be asserted only if the Targetmode bit (R2 bit 6) is set, indicating that the L5380/53C80 is acting as a target. When operating as an initiator, this bit is compared against the $\overline{C}/D$ input, and an interrupt is generated if they differ at the falling edge of $\overline{REQ}$.

R3 Bit 0 — Assert $\overline{I}/O$

When this bit is set, $\overline{I}/O$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{I}/O$. Note that $\overline{I}/O$ will be asserted only if the Targetmode bit (R2 bit 6) is set, indicating that the L5380/53C80 is acting as a target. When operating as an initiator, this bit is compared against the $\overline{I}/O$ input, and an interrupt is generated if they differ at the falling edge of $\overline{REQ}$.

WRITE ADDRESS 4
ID Select Register

The ID Select Register is a write-only register which is used to monitor selection or reselection attempts to the L5380/53C80. In arbitrating systems, an ID number is assigned to each SCSI device by setting a single bit position of the ID Select Register. Each SCSI data pin is inverted and compared with the corresponding bit in the ID Select Register. If any matches are found while a bus free condition exists and $\overline{SEL}$ is active, the L5380/53C80 will generate an interrupt to indicate a selection or reselection. During selection or reselection, parity checking may be enabled by setting the Enable Parity Check bit (R2 bit 5). This interrupt may be masked by resetting all bits in this register.

WRITE ADDRESS 5
Start DMA Send

This is a dummy register. Writes to this location are detected and cause the L5380/53C80 internal state machine to execute a DMA send operation. This location is used for either initiator or target DMA send. The DMAMODE bit (R2 bit 1) must be set prior to writing this location.

WRITE ADDRESS 6
Start DMA Target Receive

This is a dummy register. Writes to this location are detected and cause the L5380/53C80 internal state machine to execute a target DMA receive operation. The DMAMODE bit (R2 bit 1) and the Targetmode bit (R2 bit 6) must be set prior to writing this location.

WRITE ADDRESS 7
Start DMA Initiator Receive

This is a dummy register. Writes to this location are detected and cause the L5380/53C80 internal state machine to execute an initiator DMA

TABLE 2. SCSI INFORMATION TRANSFER PHASES

$\overline{MSG}$	$\overline{C}/D$	$\overline{I}/O$	Phase	Direction		
0	0	0	Message In	Target	→	Initiator
0	0	1	Message Out	Initiator	→	Target
0	1	0	Unused			
0	1	1	Unused			
1	0	0	Status In	Target	→	Initiator
1	0	1	Command	Initiator	→	Target
1	1	0	Data In	Target	→	Initiator
1	1	1	Data Out	Initiator	→	Target

receive operation. The DMAMODE bit (R2 bit 1) must be set and the Targetmode bit (R2 bit 6) must be reset prior to writing this location.

B. READ OPERATIONS

The following paragraphs give detailed descriptions of the function of each bit in the L5380/53C80 internal registers for read operations as shown in Table 3.

READ ADDRESS 0
Current SCSI Data Bus

The Current SCSI Data Bus Register allows the microprocessor to monitor the SCSI data bus at any time, by asserting $\overline{CS}$ and $\overline{IOR}$ with address lines A2-0 = 000. The SCSI data lines are not actually registered, but gated directly onto the CPU bus whenever Address 000 is read by the CPU. Therefore, reads of this location should only be done when the SCSI data lines are guaranteed to be stable by the SCSI protocol. For systems which implement SCSI bus arbitration, this location is read to determine whether devices having higher priorities are also arbitrating. Programmed I/O data transfer uses this location for reading data transferred on the SCSI data bus. With parity checking enabled, SCSI data bus parity checking is done at the beginning of the read cycle for fast error detection. Note that the SCSI data bus is inverted to become active high when presented to the CPU.

READ ADDRESS 1
Initiator Command Register

Reading bit 7 or bits 4–0 of the Initiator Command Register simply reflects the status of the corresponding bit in the register. Bits 6 and 5 are mapped to other signals as discussed below:

R1 Bit 6 — Arbitration In Progress

For this bit to be active, the Arbitrate bit (R2 bit 0) must be set. When ARBITRATION IN PROGRESS is set, it indicates that the L5380/53C80 has detected a bus free condition and is currently arbitrating for control of the bus. See the section on "Arbitration" for a complete discussion of the L5380/53C80 arbitration mechanism. Resetting the Arbitrate bit will reset ARBITRATION IN PROGRESS.

R1 Bit 5 — Lost Arbitration

For this bit to be active, the Arbitrate bit (R2 bit 0) must be set. When LOST ARBITRATION is set, it indicates that the L5380/53C80 has arbitrated for the SCSI bus (see R1 bit 6 above) and has detected the assertion of $\overline{SEL}$ by another (higher priority) device. The L5380/53C80 responds to loss of arbitration by immediately discontinuing the arbitration attempt. Resetting the Arbitrate bit will reset LOST ARBITRATION.

READ ADDRESS 2
Mode Register

Reading the Mode Register simply reflects the status of the bits in that register.

READ ADDRESS 3
Target Command Register

Reading the Target Command Register simply reflects the status of the bits in that register, except for bit 7, LAST BYTE SENT.

R3 bit 7 — Last Byte Sent

This read only bit indicates that the last byte of data loaded into the L5380/53C80 during a DMA send operation has actually been transferred over the SCSI bus. Note that the end of process flag and the corresponding interrupt occur when this byte is loaded into the L5380/53C80, but do not reflect whether it has actually been sent. This bit is not present in the NCR5380, but is present in the NCR53C80. Last Byte Sent is reset when the DMAMODE bit (R2 bit 1) is reset.

READ ADDRESS 4
Current SCSI Control Register

The Current SCSI Control Register provides a means for the CPU to directly monitor the state of the SCSI bus control signals. The SCSI control lines are not actually registered, but gated directly onto the CPU bus whenever Address 100 is read by the CPU. The value of each bit position represents the complement of the corresponding (low true) SCSI Signal Pin.

READ ADDRESS 5
DMA Status Register

The DMA Status Register provides a means for the CPU to determine the status of a DMA transfer and to determine the cause of an interrupt. It also makes available the final two SCSI bus signals which are not included in the Current SCSI Control Register. The function of each individual bit is defined as follows:

R5 Bit 7 — End of DMA

When this bit is set, it indicates that a valid $\overline{EOP}$ has been received during a DMA transfer. A valid $\overline{EOP}$ occurs when $\overline{EOP}$, $\overline{DACK}$, and either $\overline{IOR}$ or $\overline{IOW}$ are simultaneously active for the minimum specified time. End of DMA is reset when the DMAMODE bit (R2 bit 1) is reset.

Note that for DMA send operations, an END OF DMA status indicates only that the last byte of the transfer is loaded into the Output Data Register of the sending device, not that it has actually been transferred over the SCSI bus. For this reason, the L5380/53C80 provides an additional status bit; Last Byte Sent (R3 bit 7) which indicates that this final byte has been transferred to the receiving end. This bit is not present in the NCR5380.

Also, note that the DMAMODE bit is reset automatically whenever a loss of busy condition is detected, which in turn resets END OF DMA. Therefore

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the DMA Status Register should be read prior to resetting the Assert $\overline{BSY}$ bit (R1 bit 3) at the conclusion of a DMA transfer.

R5 Bit 6 — DMA Request

This bit reflects the state of the DRQ (DMA Request) signal. In programmed I/O, this bit can be polled by the CPU to determine whether there is a pending request for byte transfer. For DMA send operations, DMA $\overline{REQUEST}$ is reset when $\overline{DACK}$ and $\overline{IOW}$ are simultaneously asserted. For DMA receive operations, simultaneous $\overline{DACK}$ and $\overline{IOR}$ will reset DMA REQUEST. DMA REQUEST is reset unconditionally when the DMAMODE bit (R2 bit 1) is reset.

R5 Bit 5 — Parity Error

This bit can only be set if Enable Parity Check (R2 bit 5) is set. When enabled, the Parity Error bit is set if incoming SCSI data in either initiator or target mode, or during selection phase, does not correctly reflect odd parity. PARITY ERROR can be reset by a read to the Reset Error/Interrupt Register (Register 7).

R5 Bit 4 — Interrupt Request

This bit reflects the state of the IRQ signal. The L5380/53C80 asserts IRQ to generate an interrupt to the CPU. See the section on "Interrupts" for further information on the possible sources of interrupts in the L5380/53C80. INTERRUPT REQUEST can be reset by a read to the Reset Error/Interrupt Register (Register 7).

R5 Bit 3 — Phase Match

When this bit is set, it indicates that the $\overline{MSG}$, $\overline{C}/D$, and $\overline{I}/O$ lines match the state of the Assert $\overline{MSG}$, Assert $\overline{C}/D$, and Assert $\overline{I}/O$ bits in the Target Command Register. PHASEMATCH is not actually registered, but represents a continuous comparison of these three phase bits to the corresponding internal register locations. This bit is intended for use by the

TABLE 3. READ REGISTERS

Address 0 — Current SCSI Data Bus

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 1 — Initiator Command Register

7	6	5	4	3	2	1	0
ASSERT $\overline{RST}$	ARB. IN PRO-GRESS	LOST ARB.	ASSERT $\overline{ACK}$	ASSERT $\overline{BSY}$	ASSERT $\overline{SEL}$	ASSERT $\overline{ATN}$	ASSERT DATA BUS

Address 2 — Mode Register

7	6	5	4	3	2	1	0
BLOCK MODE	TARGET MODE	ENABLE PARITY CHECK	ENABLE PARITY INT'RPT	ENABLE EODMA INT'RPT	MONI-TOR BUSY	DMA MODE	ARBI-TRATE

Address 3 — Target Command Register

7	6	5	4	3	2	1	0
LAST BYTE SENT				ASSERT $\overline{REQ}$	ASSERT $\overline{MSG}$	ASSERT $\overline{C}/D$	ASSERT $\overline{I}/O$

Address 4 — Current SCSI Control Register

7	6	5	4	3	2	1	0
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C}/D$	$\overline{I}/O$	$\overline{SEL}$	$\overline{PARITY}$

Address 5 — DMA Status Register

7	6	5	4	3	2	1	0
END OF DMA	DMA REQ.	PARITY ERROR	INTER-RUPT REQ.	PHASE MATCH	BUSY ERROR	$\overline{ATN}$	$\overline{ACK}$

Address 6 — Input Data Register

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 7 — Reset Error/Interrupt Register

7	6	5	4	3	2	1	0

initiator to detect that the target device has changed to a different information transfer phase. When the L5380/53C80 detects a phase mismatch, PHASEMATCH is reset, and information transfer to or from the SCSI bus is inhibited.

R5 Bit 2 — Busy Error

This bit can only be set if the Monitor Busy bit (R2 bit 2) is set. When set, Busy Error indicates that the BSY pin has been false for a period at least equal to a bus settle delay (400 ns). When the Busy Error condition is detected, all SCSI signal pins are disabled, and the DMAMODE bit (R2 bit 1) and bits 5-0 of the Initiator Command Register are reset. Busy Error can be reset by a read to the Reset Error/Interrupt Register (Register 7).

R5 Bits 1, 0 — $\overline{ATN}$, $\overline{ACK}$

Like the Current SCSI Control Register, these bits provide a means for the CPU to directly monitor the state of the SCSI bus control signals. The SCSI control lines are not actually registered, but gated directly onto the CPU bus whenever Address 5 is read by the CPU. The value of each bit position represents the complement of the corresponding (low true) SCSI Signal Pin.

READ ADDRESS 6
Input Data Register

This register acts as a temporary holding register for information received from the SCSI data bus during DMA transfers (DMAMODE bit, R2 bit 1 is set). In the initiator mode, the L5380/53C80 latches the SCSI data when $\overline{REQ}$ goes active. In the target mode, data is latched when $\overline{ACK}$ goes active. The contents of this register represent the negation of the low-true SCSI data. The contents of the SCSI Input Data Register are gated onto the CPU data bus when $\overline{DACK}$ and $\overline{IOR}$ are simultaneously true, or by a CPU read of location 6. Note that $\overline{DACK}$ and $\overline{CS}$ must never be active simultaneously in order to prevent conflicting read operations. Parity may optionally be checked on the data as it is loaded into this register.

READ ADDRESS 7
Reset Error/Interrupt Register

This is a dummy register. Reads to this location are detected and used to reset the Interrupt Request Latch (IRQ signal) and the PARITY ERROR, INTERRUPT REQUEST, and BUSY ERROR latches (visible as bits 5, 4, and 2 of Register 5).

INTERRUPTS

The L5380/53C80 generates interrupts to the CPU by setting the Interrupt Request Latch, which directly drives the IRQ (Interrupt Request) line. The IRQ output will reflect the state of the Interrupt Request Latch under all conditions except when Testmode (R1 bit 6) is active, when it is in a high impedance state. The Interrupt Request Latch may be reset by reading Address 7, the Reset Error/Interrupt Register. A read of this location also resets several error condition latches as discussed in the section on "Internal Registers".

Interrupts may be caused by any of six conditions, most of which may be masked by resetting enable bits in the appropriate registers. The following sections describe each interrupt type, its cause, and how it may be reset. Upon receiving an interrupt, the CPU may read the Current SCSI Control Register (R4) and the DMA Status Register (R5) to determine the cause of the interrupt. While the following discussions indicate the expected values of these registers following an interrupt, it is recommended that bits in these registers which are not germane to determining the cause of an interrupt be masked off in firmware prior to implementing a comparison. A typical operational sequence for an interrupt service routine is given at the end of this section.

SCSI Bus Reset Interrupt

A SCSI Bus Reset Interrupt occurs when the SCSI $\overline{RST}$ signal becomes active. This may be due to another SCSI device driving the $\overline{RST}$ line, or because the Assert $\overline{RST}$ bit (R1 bit 7) has been set, causing the L5380/53C80 to drive the SCSI $\overline{RST}$ line. The value of the SCSI $\overline{RST}$ line is visible as R4 bit 7; however, this line is not latched and therefore may have changed state by the time the CPU responds to the interrupt and polls this location. For this reason, a SCSI Bus Reset Interrupt should be assumed if no other interrupt condition is active when reading Registers 4 and 5.

The SCSI Bus Reset Interrupt is nonmaskable. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Selection/Reselection Interrupt

A Selection/Reselection Interrupt occurs when the SCSI $\overline{SEL}$ signal becomes active, the SCSI bus matches the bit set in the ID Select Register, and $\overline{BSY}$ has been false for at least a bus settle delay. When the $\overline{I}$/O pin is asserted, the interrupt should be interpreted as a reselection. The Selection/Reselection Interrupt may be masked by resetting all bits in the ID Select Register. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Loss of Busy Interrupt

A Loss of Busy Interrupt occurs when the SCSI $\overline{BSY}$ signal has been inactive for at least a bus settle delay (400 ns). The Loss of Busy Interrupt may be masked by resetting the Monitor Busy bit (R2 bit 2). Resetting Monitor Busy also prevents the Busy Error latch (Read R5 bit 2) from being set. The expected read values for the Current

SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Phase Mismatch Interrupt

A Phase Mismatch Interrupt occurs when the DMAMODE bit (R2 bit 1) is set, $\overline{REQ}$ is active on the SCSI bus, and the SCSI phase signals $\overline{MSG}$, $\overline{C}/D$, and $\overline{I}/O$ do not match the corresponding bits in the Target Command Register. This interrupt is intended for use by the initiator to detect a change of phase by the target during a DMA transfer. When operating as a target, the SCSI phase lines will normally be asserted via the Target Command Register, so no phase mismatch will be generated unless another SCSI device is erroneously driving the phase lines to an unintended state.

The result of the continuous comparison of the SCSI phase lines to the Target Command Register contents is visible as the Phase Match bit (Read R5 bit 3). This flag operates irrespective of the state of DMAMODE and $\overline{REQ}$. As long as a phase mismatch condition persists, the L5380/53C80 is prevented from recognizing active $\overline{REQ}$ inputs, and SCSI output data drivers are disabled.

The Phase Mismatch Interrupt is nonmaskable, however it will only occur when operating in DMAMODE. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Parity Error Interrupt

A Parity Error Interrupt occurs when incorrect parity is detected during a read of the SCSI bus. Parity checking occurs under the following conditions: Parity is checked during a programmed I/O read of the Current SCSI Data Register (Read R0), when $\overline{CS}$ and $\overline{IOR}$ are active and the A_{2-0} lines are 000. Parity is also checked during DMA read operations (DMAMODE bit, R2 bit 1 is set) when $\overline{ACK}$ is active for target receive, or $\overline{REQ}$ is active for initiator receive.

The Parity Error latch is set when parity error checking is enabled and one of the above parity error conditions is encountered. This latch is

TABLE 4. INTERRUPT READ VALUES

Read Address 4 — Current SCSI Control Register

7	6	5	4	3	2	1	0
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C}/D$	$\overline{I}/O$	$\overline{SEL}$	$\overline{PARITY}$
SCSI Bus Reset Interrupt							
X	0	0	0	0	0	0	0
Selection/Reselection Interrupt							
0	0	0	X	X	1=RESEL	1	X
Loss of Busy Interrupt							
0	0	0	0	0	0	0	0
Phase Mismatch Interrupt							
0	1	1	X	X	X	0	X
Parity Error Interrupt							
0	X	X	X	X	X	X	X
End of DMA Interrupt							
0	1	X	X	X	X	0	X

Read Address 5 — DMA Status Register

7	6	5	4	3	2	1	0
END OF DMA	DMA REQ	PARITY ERROR	INTER-RUPT REQ	PHASE MATCH	BUSY ERROR	$\overline{ATN}$	$\overline{ACK}$
SCSI Bus Reset Interrupt							
0	0	0	1	1	0	0	0
Selection/Reselection Interrupt							
0	0	0	1	X	0	X	0
Loss of Busy Interrupt							
0	0	0	1	X	1	0	0
Phase Mismatch Interrupt							
0	0	0	1	0	X	X	0
Parity Error Interrupt							
X	X	1	1	X	X	X	X
End of DMA Interrupt							
1	0	0	1	X	0	0	X

visible as bit 5 of the DMA Status Register (Read R5). The Parity Error Interrupt may be masked and setting of the Parity Error latch prevented by resetting the Enable Parity Check bit (Write R2 bit 5). The Parity Error latch can be reset by reading the Reset Error/Interrupt Register (Read R7). The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

End of DMA Interrupt

An End of DMA Interrupt occurs when a valid $\overline{EOP}$ (End of Process) signal is detected during a DMA transfer. $\overline{EOP}$ is valid when $\overline{EOP}$, $\overline{DACK}$, and either $\overline{IOR}$ or $\overline{IOW}$ are simultaneously asserted for the minimum specified time. $\overline{EOP}$ inputs not occurring during I/O read or write operations are ignored.

The End of DMA latch is set whenever the DMAMODE bit (R2 bit 1) is set and a valid $\overline{EOP}$ is received. This latch is visible as bit 7 of the DMA Status Register (Read R5). The End of DMA Interrupt may be masked by resetting the Enable EODMA Interrupt bit (Write R2 bit 3). This bit does not affect the End of DMA latch, however. The End of DMA latch can be reset by resetting the DMAMODE bit in the Mode Register. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

DATA TRANSFERS

The L5380/53C80 supports programmed I/O under CPU control or DMA transfer via a DMA controller when transferring information to and from the SCSI data bus. Programmed I/O can be implemented entirely in firmware or using minimum external logic for accessing the appropriate registers. Under DMA control, the L5380/53C80's DMA interface logic and internal state machines provide the necessary control of the $\overline{REQ}$-$\overline{ACK}$ handshake. Each type of transfer is fully described in the following sections.

Programmed I/O

Two forms of programmed I/O are supported by the L5380/53C80. For normal programmed I/O, the SCSI handshake is accomplished by setting bits in the Initiator or Target Command registers to assert SCSI control lines, and polling the Current SCSI Control and DMA Control registers for the appropriate responses. Since for this method the control is contained in firmware, the cycle times are relatively slow. It is most appropriate for transferring small blocks of data such as SCSI command blocks or messages, where the overhead of setting up a DMA controller could be significant.

Pseudo DMA

An alternate method of programmed I/O allows the state machines of the L5380/53C80 to handle the SCSI handshake, thereby improving performance in systems which do not employ a hardware DMA controller. To implement Pseudo DMA, the DMAMODE bit is set. The CPU polls the DRQ bit in the DMA Control Register to determine when a byte should be written to or read from the

TABLE 5. TYPICAL INTERRUPT SERVICE ROUTINE POLLING SERVICE

Read Address 5 > TEMP	: Read DMA Status Reg to variable TEMP
IF TEMP "AND" HEX (10) = 0 THEN GO TO NEXT DEVICE	: IRQ not active, so L5380/L53C80 was not the source of this interrupt
TEMP "AND" HEX (AC) → TEMP	: Mask off irrevelant bits
IF TEMP > HEX (7F) THEN GO TO EODMA	: End of DMA Interrupt
IF TEMP > HEX (1F) THEN GO TO PARERR	: Parity Error Interrupt
IF TEMP > HEX (03) THEN GO TO BYSERR	: Loss of Busy Interrupt
IF TEMP = HEX (00) THEN GO TO PHASERR	: Phase Mismatch Interrupt
Read Address 4 → TEMP	: Read Current SCSI Control Reg to variable TEMP
TEMP "AND" HEX (06) → TEMP	: Mask off irrevelant bits
IF TEMP = HEX (06) THEN GO TO RESEL	: Reselection Interrupt
IF TEMP = HEX (02) THEN GO TO SEL	: Selection Interrupt
IF TEMP = HEX (00) THEN GO TO RESET	: SCSI Bus Reset Interrupt

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L5380/53C80. When reading or writing, external logic must be used to decode the L5380/53C80 location and produce $\overline{DACK}$, since it is used by the internal state machines. Also, $\overline{CS}$ must be suppressed since it may not be asserted simultaneously with $\overline{DACK}$.

Normal DMA Mode

Normal DMA mode is obtained when the DMAMODE bit is set but the Blockmode bit is reset. The DMA process is started by writing to the Start DMA Send, Start DMA Initiator Receive, or Start DMA Target Receive locations as appropriate. Once started, the internal state machines of the L5380/53C80 manage the $\overline{REQ}$ - $\overline{ACK}$ handshake protocol, as well as the DRQ-$\overline{DACK}$ handshake with the DMA controller.

The L5380/53C80 will assert DRQ whenever it is ready to transfer a byte to or from the DMA controller. In response to DRQ, the controller asserts $\overline{DACK}$ and $\overline{IOR}$ to read the byte, or $\overline{DACK}$ and $\overline{IOW}$ to write a byte to the L5380/53C80. For write operations, the byte is latched at the rising edge of the logical AND of $\overline{DACK}$ and $\overline{IOW}$. The transfer can be terminated by asserting $\overline{EOP}$ during a read or write operation, or by resetting the DMAMODE bit.

Block DMA Mode

When the Blockmode bit is set, the DMA handshake is no longer dependent on interlocked DRQ-$\overline{DACK}$ cycles. Instead, the DMA controller may be allowed to free-run, with data flow throttled by inserting "wait-states" in the DMA transfer to or from the L5380/53C80. Wait-states, which are idle clock cycles inserted during the I/O read or write operation, are inserted by the DMA controller until the READY output of the L5380/53C80 goes true, allowing the bus cycle to conclude.

The READY output will be deasserted under the following conditions: For send operations, READY will be false whenever the Output Data Register contains a byte which has not been transferred over the SCSI bus. This allows the DMA controller to access RAM to fetch the next byte, but postpones the end of the CPU bus cycle until the previous byte has been transferred, freeing the Output Data Register to receive it.

For receive operations, READY will be false whenever the Input Data Register is empty. This allows the DMA controller to address the RAM for a write operation, but postpones the end of the CPU bus cycle until the incoming byte is stored in the Input Data Register and is available on the CPU bus.

Note that when blockmode is employed, $\overline{DACK}$ may optionally remain asserted throughout the DMA transfer, since it is not used in an interlocked DMA handshake (Its interlock function is replaced by $\overline{IOR}$ or $\overline{IOW}$). Also, DRQ will be asserted in the normal way when operating in blockmode. To gain the abovementioned performance benefits, it should be used only to initiate the first byte transfer, with READY used to throttle succeeding transfers. This methodology is compatible with DMA controllers such as the Intel 8237 and AMD Am9516/9517.

In summary, blockmode operation offers the potential for improved transfer rates by overlapping the DMA memory access with the SCSI transfer. This is of particular value when used with DMA controllers capable of "flyby" operation, where the data is transferred directly from memory to the peripheral, and does not pass through the DMA controller itself. This transfer rate gain is achieved at the expense of locking up the CPU bus for a time equal to the SCSI transit time of the entire block. This may be strongly preferable in some systems where net disk access time is a crucial performance factor. Also, the time required to arbitrate for the CPU bus on a byte-by-byte basis may well be longer than the cycles wasted waiting for SCSI transfers to take place, especially with fast peripherals which operate from a high speed sector buffer.

Terminating DMA Transfers

DMA transfers, either normal or blockmode, may be terminated in a number of ways. The following sections describe these methods, along with providing information about correct sequencing of various signals to effect a clean exit from a DMA process.

$\overline{EOP}$ Signal

The $\overline{EOP}$ signal is usually generated by a DMA controller to indicate that its transfer counter has decremented to zero. In order to be recognized by the L5380/53C80, it should be asserted simultaneously with the $\overline{DACK}$ and $\overline{IOR}$ or $\overline{IOW}$ signals corresponding to the last byte in the transfer. Note that in the case of send operations, asserting $\overline{EOP}$ indicates to the L5380/53C80 that SCSI transfers should cease after transmission of the byte loaded while $\overline{EOP}$ is asserted. In order to determine when this last byte has actually been sent, the Last Byte Sent flag in the Target Command Register may be examined. This flag is not present in the NCR implementation of the 5380, but is available in the 53C80, a non-pin-compatible variant. The $\overline{EOP}$ input does not reset the DMAMODE bit, but after transmission of the last byte causes the internal state machine to return to an idle condition, so that no further SCSI handshaking will occur until another transmission is explicitly initiated. Note that the NCR version of the 5380, upon receiving an $\overline{EOP}$, will stop asserting DRQ, but will continue to issue $\overline{ACK}$ in response to additional $\overline{REQ}$ inputs,

potentially causing data loss if the target initiates another data transmission without an intervening phase change. The L5380/53C80 prevents this spurious DMA handshake from occurring.

DMA Mode Bit

Resetting the DMAMODE bit in the Mode Register causes a hard reset of the internal DMA state machines, and thus an effective termination of a DMA transfer. Since unlike the $\overline{EOP}$ case the state machine is not allowed to exit gracefully, care must be taken in the timing of DMAMODE reset.

For receive operations, the DMAMODE bit should be reset after the last $\overline{DRQ}$ is received, but prior to asserting $\overline{DACK}$ to prevent an additional $\overline{REQ}$ or $\overline{ACK}$ from occurring. For normal DMA mode, resetting this bit will cause DRQ to go inactive. However, the last byte received remains in the SCSI Input Data Register and may be read either by the normal $\overline{DACK}$ and $\overline{IOR}$ DMA read or using a CPU read of Address 6. For blockmode DMA, READY will remain asserted when DMAMODE is reset, allowing the DMA controller to retrieve the last byte in the normal fashion. The NCR version of the 5380 fails to keep READY asserted when DMAMODE is reset, potentially causing deadlock on the CPU bus.

Bus Phase Mismatch

When operating in DMAMODE as an initiator, a bus phase mismatch can be used to terminate a data transfer. If the $\overline{C}$/D, $\overline{I}$/O, and $\overline{MSG}$ lines fail to match the corresponding bits in the Target Command Register, it will prevent recognition of $\overline{REQ}$, and will disable the SCSI data and parity output drivers. Also, when $\overline{REQ}$ becomes active, an interrupt will be generated. Because $\overline{REQ}$ is not recognized, the effect is to stop the DMA transfer, although the state machine does not return to idle until either DMAMODE is reset or a valid $\overline{EOP}$ is received.

One caution should be observed when using phase changes to end DMA transfers: While this method does not require the initiator to keep a transfer counter, it depends on the target causing a phase change between any two consecutive information transfer phases. Since this is not required by the protocol, it must be guaranteed by the target software. Otherwise the target may begin a new information transfer without the initiator recognizing the boundary between the two.

ARBITRATION

The L5380/53C80 contains on-chip hardware to assist in arbitrating for the SCSI bus. This arbitration logic cooperates with the host firmware to effect SCSI arbitration, as described in the following paragraphs:

The SCSI arbitration timeline begins with detection of a bus free condition at time t_0. Bus free is defined as $\overline{BSY}$ and $\overline{SEL}$ inactive for at least a bus settle delay (400 ns). Following the bus settle delay, the SCSI device must wait an additional bus free delay of 800 ns, for a total of 1200 ns after t_0, prior to driving any signal. Thus a minimum of 1200 ns must elapse from initial deassertion of $\overline{BSY}$ to the beginning of an arbitration attempt. A final constraint is that arbitration may not begin if more than a bus set delay (1800 ns) has elapsed since $\overline{BSY}$ became active (arbitration began), corresponding to 2200 ns after t_0.

The CPU indicates a desire to arbitrate by setting the Arbitrate bit (R2 bit 0). When Arbitrate is set, the L5380/53C80 will monitor the state of $\overline{BSY}$ and $\overline{SEL}$ to detect a bus free condition. The actual implementation uses an internal delay line to provide a time reference for detection of a bus free condition. This delay is nominally 800 ns during which $\overline{BSY}$ and $\overline{SEL}$ must be inactive. This time represents the center of the window between the Bus Settle Delay (400 ns) and the Bus Free Delay (400 + 800 = 1200 ns). When Bus Free is detected, the L5380/53C80 waits for an additional time of nominally 900 ns (1700 ns nominal since t_0) and asserts $\overline{BSY}$ and the contents of the Output Data Register. This time represents the center of the 1200 ns–2200 ns window between the earliest and latest legal arbitration attempt. Since the actual delays are process and temperature dependent, they will vary in practice, but will always remain well within the specified limits.

Once arbitration has begun ($\overline{BSY}$ and the Output Data Register asserted,) the Arbitration In Progress bit (R1 bit 6) will be set, allowing the CPU to detect the fact that arbitration has begun. The CPU should then wait one arbitration delay (2.2 µs) before reading the bus to determine whether arbitration has been won or lost. The Lost Arbitration bit (R2 bit 7) will be active if the L5380/53C80 has detected $\overline{SEL}$ active on the SCSI bus, indicating that another SCSI device has declared itself the winner of the arbitration. $\overline{SEL}$ active also disables the SCSI output drivers, allowing the winning arbitrator to proceed with its transfer.

BUG FIXES/ENHANCMENTS

The NCR5380 and the Am5380 have some architectural bugs, both published and unpublished. The **LOGIC Devices L5380/53C80** was designed to eliminate these bugs while maintaining pin and architectural compatibility. A list of these errors along with solutions implemented in the L5380/53C80 is itemized below.

1. When executing blockmode DMA send operations, the READY signal is intended to insert memory wait states as a mechanism to throttle data transfer, with the DMA controller in a free-running loop. The NCR/Am5380 erroneously allows the contents of the Output Data Register to be overwritten by subsequent bytes prior to acknowledgment of the

current byte by the SCSI receiver. This causes loss of data when operating in blockmode if the sender's DMA cycle is faster than the receiver's.

2. Assertion of $\overline{EOP}$ during blockmode DMA transfers fails to cause assertion of READY in the NCR/Am5380. This may prevent the CPU from becoming bus master and can result in lockup of the CPU bus in a not-ready state. In block DMA send mode when $\overline{EOP}$ is received, the L5380/53C80 reasserts READY immediately after transmitting the final byte. For receive mode, READY is asserted immediately.

3. When a valid $\overline{EOP}$ is detected, the NCR/Am5380 prevents assertion of additional DRQ's, but continues to respond to SCSI handshakes. This means that additional data transmitted without phase change may be lost. The L5380/53C80, like the NCR/Am5380 remains in DMAMODE after an $\overline{EOP}$. However, the internal state machine returns to an idle condition and does not respond to additional SCSI handshake attempts until another data transfer is explicitly initiated.

4. When operating as an initiator in DMAMODE, the NCR/Am5380 leaves $\overline{ACK}$ asserted after receipt of a valid $\overline{EOP}$, requiring the CPU to deassert it. When a valid $\overline{EOP}$ is detected, the L5380/53C80 deasserts $\overline{ACK}$ properly.

5. If the NCR/Am5380 is not terminated on the SCSI side, the floating $\overline{RST}$ pin will cause spurious interrupts. The L5380/53C80 contains internal high value pullups to set unterminated SCSI pins to the inactive state.

6. During DMA send operations, when a valid $\overline{EOP}$ signal is received by the NCR/Am5380, no convenient indication exists to indicate that the last byte of data (loaded simultaneously with $\overline{EOP}$) has in fact been successfully transmitted. The L5380/53C80 provides Last Byte status bit mapped to bit 7 of the Target Command Register. This bit will be set after a valid $\overline{EOP}$ has occurred, and the final byte has been transmitted successfully.

7. During the reselection phase, the NCR/AM5380 may reset the reselection interrupt if the contents of the Target Command Register do not match the current SCSI bus phase. The L5380/53C80 does not spuriously reset this interrupt.

8. In the NCR/Am5380, the phase mismatch interrupt is captured in an edge triggered fashion on the active edge of $\overline{REQ}$. During reselection, this interrupt might not be generated even though a phase change has occurred. The reason for this is as follows:

- The initiator DMAMODE bit must be set in order to receive a phase-match interrupt.
- However, the DMAMODE bit cannot be set unless $\overline{BSY}$ is active.
- $\overline{BSY}$ will be driven active by the target only after the relesection has occurred.
- Once $\overline{BSY}$ has been asserted by the target, it may then assert $\overline{REQ}$ before the initiator has set the DMAMODE bit, and the initiator will then fail to generate an interrupt.

The L5380/53C80 interrupt latch will be set if a phase mismatch condition exists when the later of $\overline{REQ}$ or DMAMODE become active. In this way, the mismatch will always be detected, even if the target asserts $\overline{REQ}$ before the initiator sets DMAMODE.

MAXIMUM RATINGS *Above which useful life may be impaired*

Storage temperature	–65°C to +150°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Output voltage	0.0 V to V_{CC}
Input voltage	0.0 V to +5.5 V
I_{OL} Low Level Output Current (SCSI Bus)	48 mA
I_{OL} Low Level Output Current (other pins)	8 mA
I_{OH} High Level Output Current (other pins)	–4 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

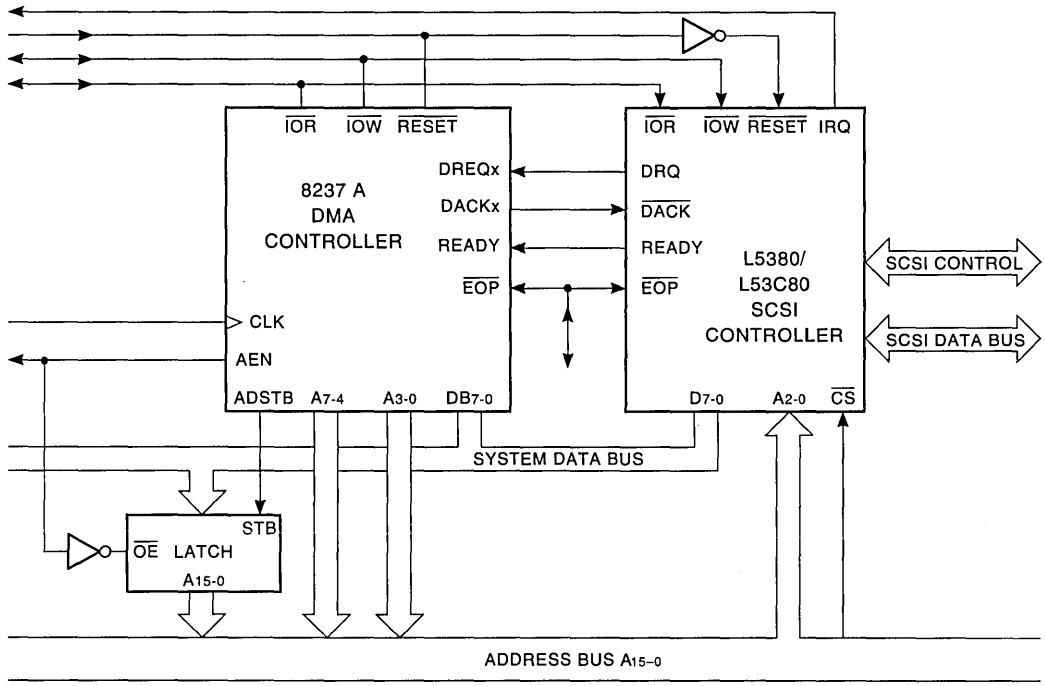
Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		0.0		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{OL}	Output Low Voltage (SCSI bus)	V_{CC} = Min, I_{OL} = 48 mA			0.5	V
V_{OL}	Output Low Voltage (other pins)	V_{CC} = Min, I_{OL} = 8 mA			0.5	V
V_{OH}	Output High Voltage (other pins)	V_{CC} = Min, I_{OH} = –4 mA	3.5			V
I_{IN}	Input Current*	V_{CC} = Max, V_{IN} = 0 – V_{CC} (SCSI bus)			65	µA
I_{IN}	Input Current*	V_{CC} = Max, V_{IN} = 0 – V_{CC} (other pins)			20	µA
I_{CC}	Supply Current	V_{CC} = Max, V_{IH} = 2.4, VIL = 0.4, 4 MHz cycle, No Load, No Termination		10	20	mA
I_{CC}	Supply Current Quiescent	Same as above, inputs stable			1.5	mA

*Not tested at low temperature extreme.

DMA Interface with 8237 A

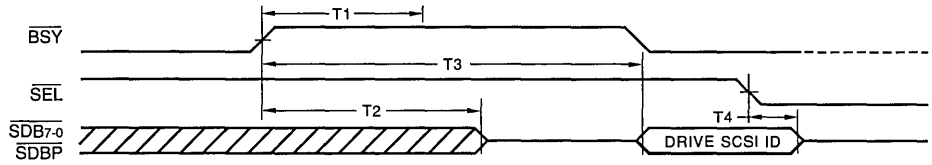


SWITCHING CHARACTERISTICS

Arbitration Timing *(ns — except where noted)*

Symbol	Parameter	L5380/53C80– Commercial Min	Max
T1	$\overline{BSY}$ False Duration to Detect Bus Free Condition	0.4 µs	1.2 µs
T2	SCSI Bus Clear (High Z) from $\overline{BSY}$ False		1.2 µs
T3	Arbitrate ($\overline{BSY}$ and SCSI ID Asserted) from $\overline{BSY}$ False (Bus Free Detected)	1.2 µs	2.2 µs
T4	SCSI Bus Clear (High Z) from $\overline{SEL}$ True (Lost Arbitration)		60

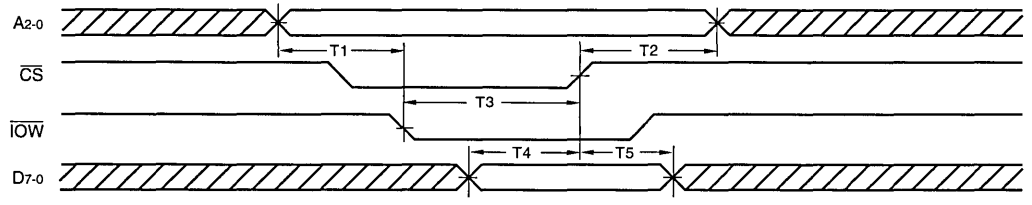
Arbitration Waveforms



CPU Write Cycle Timing *(ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 Mbytes/sec Min	Commercial 4 Mbytes/sec Max
T1	Address Setup to Write Enable	10		5	
T2	Address Hold from End of Write Enable	5		5	
T3	Width of Write Enable	40		20	
T4	Data Setup to End of Write Enable	20		5	
T5	Data Hold from End of Write Enable	10		5	

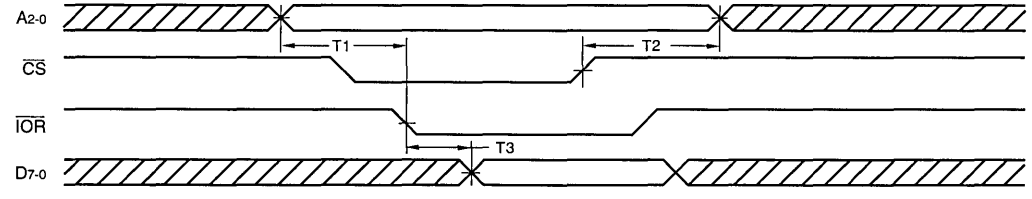
CPU Write Cycle Waveforms



CPU Read Cycle Timing *(ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 Mbytes/sec Min	Commercial 4 Mbytes/sec Max
T1	Address Setup to Read Enable	10		5	
T2	Address Hold from End of Read Enable	5		5	
T3	Data Access Time from Read Enable		50		30

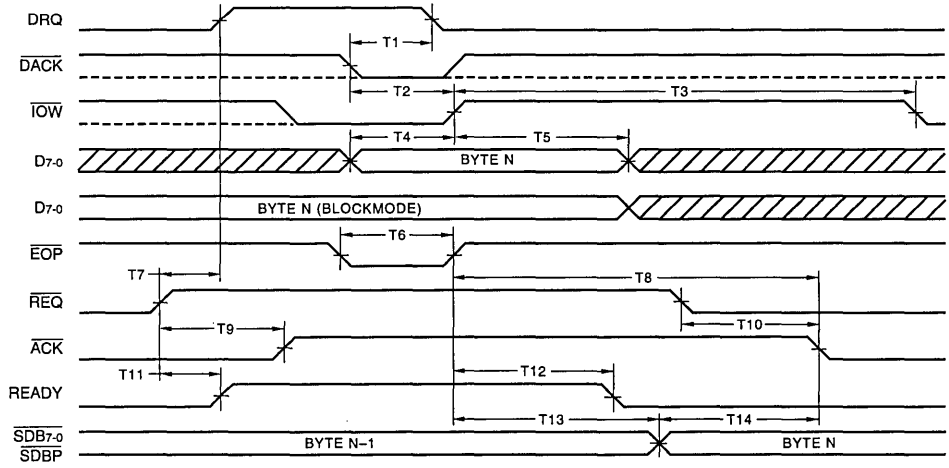
CPU Read Cycle Waveforms



DMA Write Initiator Send Timing *(ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 Mbytes/sec Min	Commercial 4 Mbytes/sec Max
	The following apply for all DMA Modes				
T1	DRQ False from Write Enable (concurrence of $\overline{IOW}$ and $\overline{DACK}$)		60		30
T2	Width of Write Enable (concurrence of $\overline{IOW}$ and $\overline{DACK}$)	60		20	
T4	Data Setup to End of Write Enable	20		5	
T5	Data Hold from End of Write Enable	15		5	
T6	Concurrent Width of $\overline{EOP}$, $\overline{IOW}$, and $\overline{DACK}$	50		20	
T9	$\overline{REQ}$ False to $\overline{ACK}$ False		90		45
T13	End of Write Enable to Valid SCSI Data		65		45
T14	SCSI Data Setup Time to $\overline{ACK}$ True	60		65	
	The following apply for Normal DMA Mode only				
T7	$\overline{REQ}$ False to DRQ True		60		30
T8	$\overline{DACK}$ False to $\overline{ACK}$ True ($\overline{REQ}$ True)		185		165
T10	$\overline{REQ}$ True to $\overline{ACK}$ True ($\overline{DACK}$ False)		70		35
	The following apply for Blockmode DMA only				
T3	$\overline{IOW}$ Recovery Time	40		20	
T8	$\overline{IOW}$ False to $\overline{ACK}$ True ($\overline{REQ}$ True)		185		165
T10	$\overline{REQ}$ True to $\overline{ACK}$ True ($\overline{IOW}$ False)		70		35
T11	$\overline{REQ}$ False to READY True		60		30
T12	$\overline{IOW}$ False to READY False		70		35

DMA Write Initiator Send Waveforms

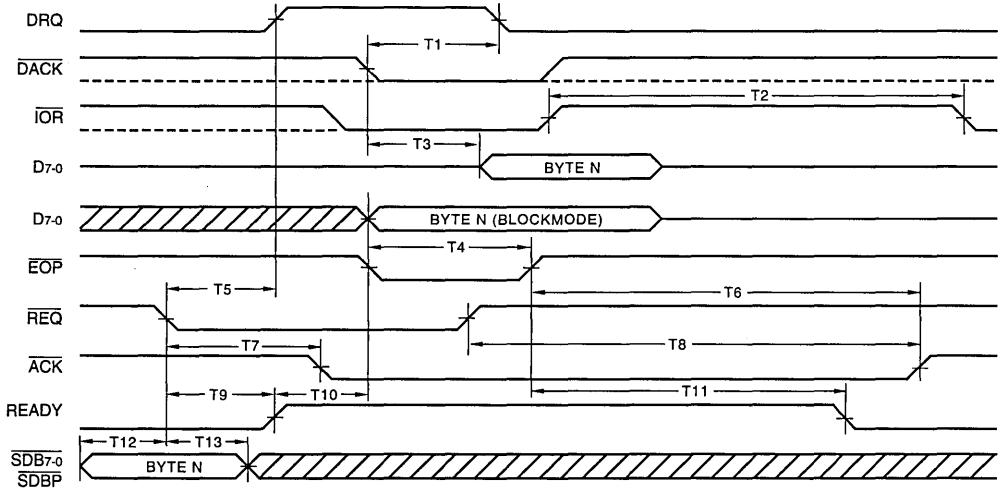


DMA Read Initiator Receive Timing *(ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 Mbytes/sec Min	Commercial 4 Mbytes/sec Max
	The following apply for all DMA Modes				
T1	DRQ False from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		30
T3	Data Access Time from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		20
T4	Concurrent Width of $\overline{EOP}$, $\overline{IOR}$, and $\overline{DACK}$	50		20	
T7	$\overline{REQ}$ True to $\overline{ACK}$ True		70		35
T12	SCSI Data Setup Time to $\overline{REQ}$ True	20		5	
T13*	SCSI Data Hold Time from $\overline{REQ}$ True	15		10	
	The following apply for Normal DMA Mode only				
T5	$\overline{REQ}$ True to DRQ True		60		30
T6	$\overline{DACK}$ False to $\overline{ACK}$ False ($\overline{REQ}$ False)		90		55
T8	$\overline{REQ}$ False to $\overline{ACK}$ False ($\overline{DACK}$ False)		80		55
	The following apply for Blockmode DMA only				
T2	$\overline{IOR}$ Recovery Time	40		20	
T6	$\overline{IOR}$ False to $\overline{ACK}$ False ($\overline{REQ}$ False)		90		45
T8	$\overline{REQ}$ False to $\overline{ACK}$ False ($\overline{IOR}$ False)		80		45
T9	$\overline{REQ}$ True to READY True		60		30
T10	READY True to CPU Data Valid		15		15
T11	$\overline{IOR}$ False to READY False		70		35

6

DMA Read Initiator Receive Waveforms

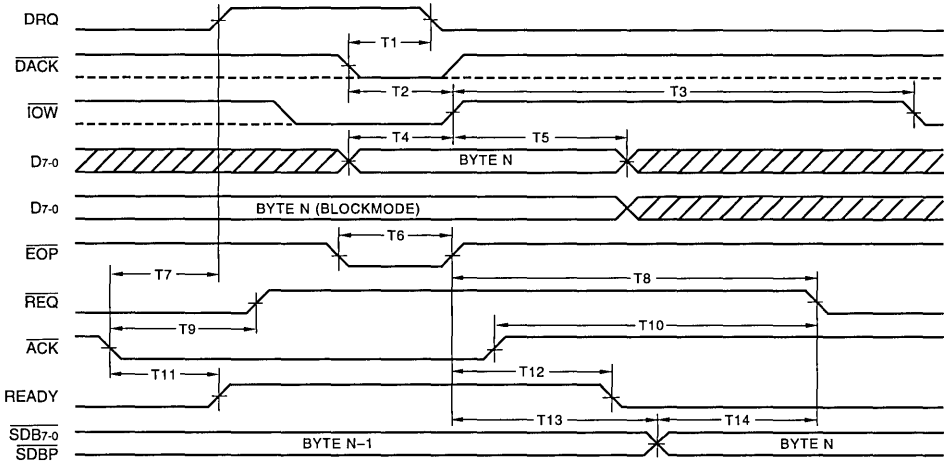


*Data must be held on the SCSI bus until $\overline{ACK}$ becomes True

DMA Write Target Send Timing *(ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 Mbytes/sec Min	Commercial 4 Mbytes/sec Max
	The following apply for all DMA Modes				
T1	DRQ False from Write Enable (concurrence of $\overline{IOW}$ and $\overline{DACK}$)		60		30
T2	Width of Write Enable (concurrence of $\overline{IOW}$ and $\overline{DACK}$)	60		20	
T4	Data Setup to End of Write Enable	20		5	
T5	Data Hold from End of Write Enable	15		5	
T6	Concurrent Width of $\overline{EOP}$, $\overline{IOW}$, and $\overline{DACK}$	50		20	
T9	$\overline{ACK}$ True to $\overline{REQ}$ False		90		45
T13	End of Write Enable to Valid SCSI Data		60		45
T14	SCSI Data Setup Time to $\overline{REQ}$ True	60		65	
	The following apply for Normal DMA Mode only				
T7	$\overline{ACK}$ True to DRQ True		60		30
T8	$\overline{DACK}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		185		165
T10	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{DACK}$ False)		70		35
	The following apply for Blockmode DMA only				
T3	$\overline{IOW}$ Recovery Time	40		20	
T8	$\overline{IOW}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		185		165
T10	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{IOW}$ False)		70		35
T11	$\overline{ACK}$ True to READY True		60		30
T12	$\overline{IOW}$ False to READY False		70		35

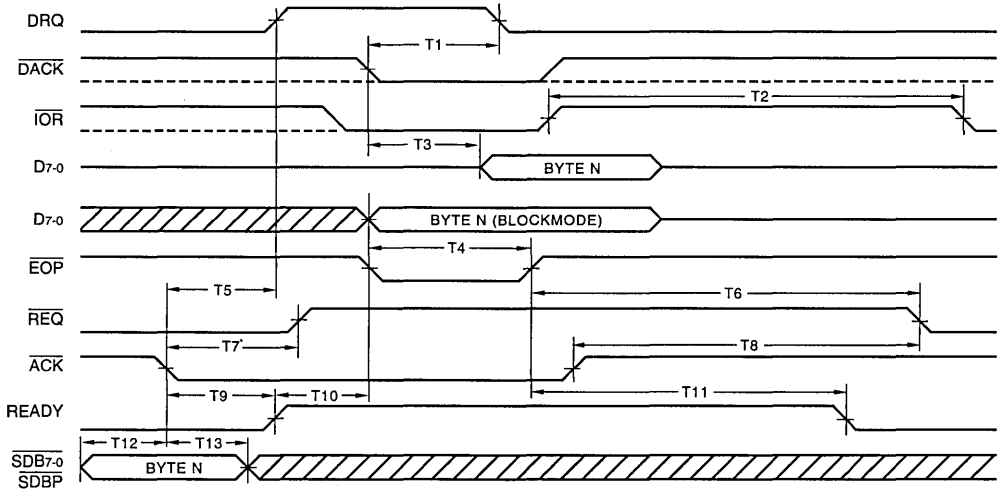
DMA Write Target Send Waveforms



DMA Read Target Receive Timing *(ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 Mbytes/sec Min	Commercial 4 Mbytes/sec Max
	The following apply for all DMA Modes				
T1	DRQ False from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		30
T3	Data Access Time from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		20
T4	Concurrent Width of $\overline{EOP}$, $\overline{IOR}$, and $\overline{DACK}$	50		20	
T7	$\overline{ACK}$ True to $\overline{REQ}$ False	70		45	
T12	SCSI Data Setup Time to $\overline{ACK}$ True	20		10	
T13*	SCSI Data Hold Time from $\overline{ACK}$ True	15		10	
	The following apply for Normal DMA Mode only				
T5	$\overline{ACK}$ True to DRQ True		60		30
T6	$\overline{DACK}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		90		45
T8	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{DACK}$ False)		80		45
	The following apply for Blockmode DMA only				
T2	$\overline{IOR}$ Recovery Time	40		20	
T6	$\overline{IOR}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		90		45
T8	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{IOR}$ False)		80		45
T9	$\overline{ACK}$ True to READY True		60		30
T10	READY True to CPU Data Valid		15		15
T11	$\overline{IOR}$ False to READY False		70		35

DMA Read Target Receive Waveforms



*Data must be held on the SCSI bus until $\overline{REQ}$ becomes False

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

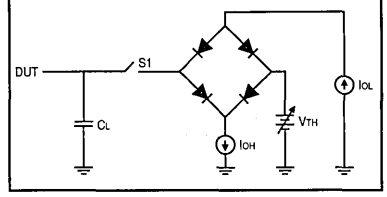
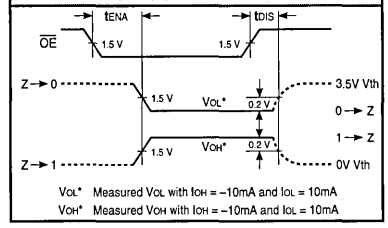
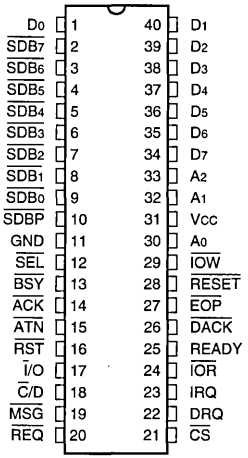


FIGURE B. THRESHOLD LEVELS

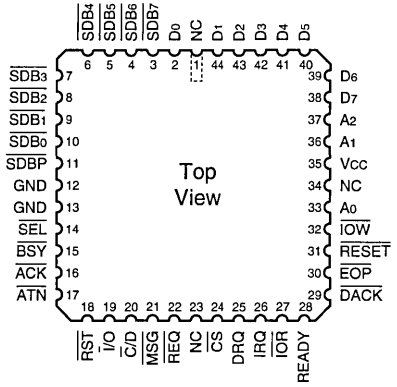


L5380 — ORDERING INFORMATION

40-pin — 0.6" wide



44-pin



Speed	Plastic DIP (P3)	Plastic J-Lead Chip Carrier (J1)
	0°C to +70°C — COMMERCIAL SCREENING	
4	L5380PC4	L5380JC4
2	L5380PC2	L5380JC2

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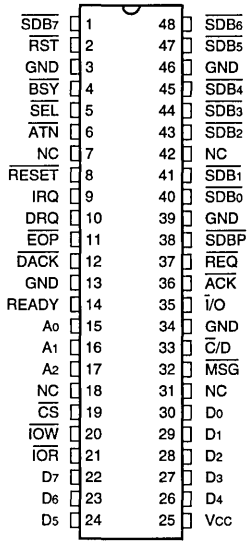
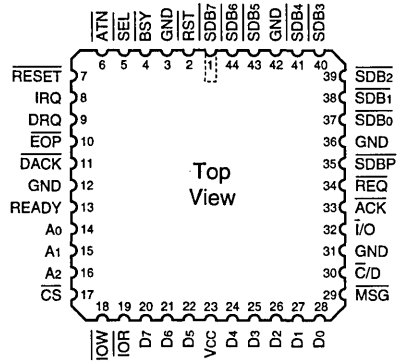
L53C80 — ORDERING INFORMATION

48-pin



44-pin



Speed	Plastic DIP (P5)	Sidebraze Hermetic DIP (D5)	Plastic J-Lead Chip Carrier (J1)
	0°C to +70°C — COMMERCIAL SCREENING		
4	L53C80PC4	L53C80DC4	L53C80JC4
2	L53C80PC2	L53C80DC2	L53C80JC2

Memory Products

7

L7C162
16K x 4 Static RAM

FEATURES

- 16K x 4 Static RAM with Separate I/O and High Impedance Write
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 12 ns maximum
- Low Power Operation
  Active: 325 mW typical at 25 ns
  Standby: 400 µW typical
- Data Retention at 2 V for Battery Backup Operation
- DECC SMD No. 5962-89712
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with IDT 71982 and Cypress CY7C162
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Ceramic DIP
  - 28-pin Plastic SOJ
  - 28-pin Ceramic LCC

DESCRIPTION

The **L7C162** is a high-performance, low-power CMOS static RAM. The storage cells are organized as 16,384 words by 4 bits per word. Data In and Data Out are separate. This device is available in four speeds with maximum access times from 12 ns to 25 ns.

Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 325 mW (typical) at 25 ns. Dissipation drops to 60 mW (typical) when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C162 consumes only 30 µW (typical) at 3 V, allowing effective battery backup operation.

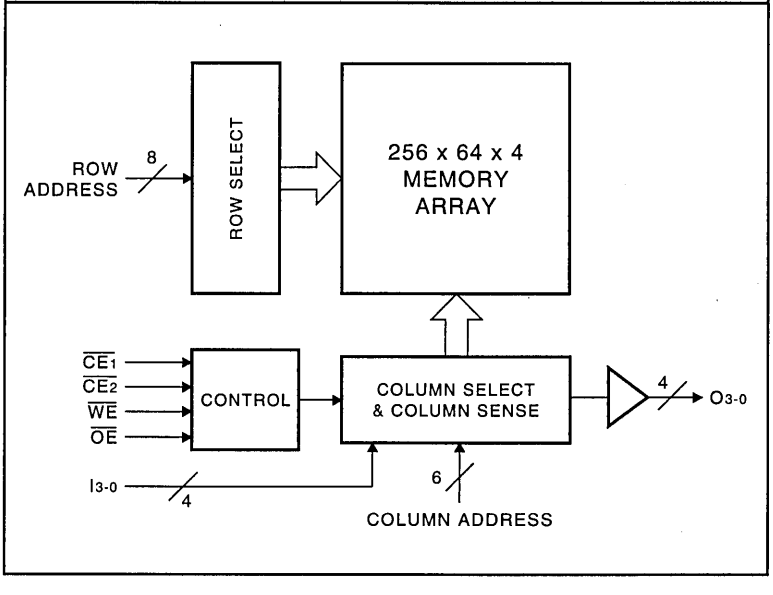
The L7C162 provides asynchronous (unclocked) operation with matching access and cycle times. Two active-low Chip Enables and a three-state output with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A0 through A13. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE1}$, $\overline{CE2}$, and $\overline{OE}$ LOW while $\overline{WE}$ remains HIGH. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{WE}$ is LOW or $\overline{CE1}$, $\overline{CE2}$, or $\overline{OE}$ is HIGH.

Writing to an addressed location is accomplished when the active-low $\overline{CE1}$, $\overline{CE2}$, and $\overline{WE}$ inputs are all LOW. Any of these signals may be used to terminate the write operation. The Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C162 can withstand an injection current of up to 200 mA on any pin without damage.

L7C162 BLOCK DIAGRAM



7

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Industrial	–40°C to +85°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Industrial	–40°C to +85°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L7C162			
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I_{IX}	Input Leakage Current	Ground ≤ V_{IN} ≤ V_{CC}	–10		+10	µA
I_{OZ}	Output Leakage Current	(Note 4)	–10		+10	µA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		12	25	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		80	300	µA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		10	150	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

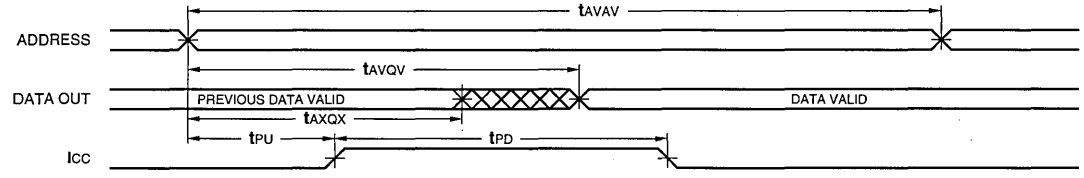
			L7C162-				
Symbol	Parameter	Test Condition	25	20	15	12	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	100	120	140	165	mA

SWITCHING CHARACTERISTICS *Over Operating Range*

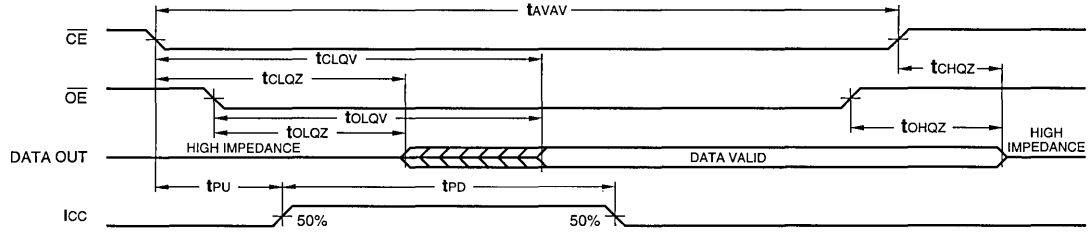
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C162–							
		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	25		20		15		12	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		25		20		15		12
t_{AXQX}	Address Change to Output Change	3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		25		20		15		12
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		10		8		8		5
t_{OLQV}	Output Enable Low to Output Valid		12		10		8		6
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		10		8		5		5
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		25		20		20		20
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0	

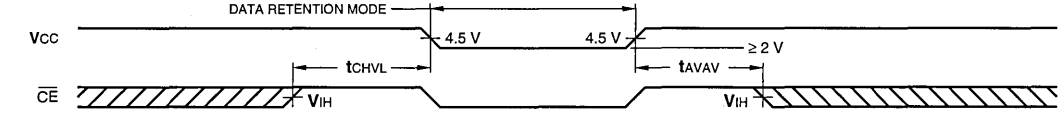
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}/\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

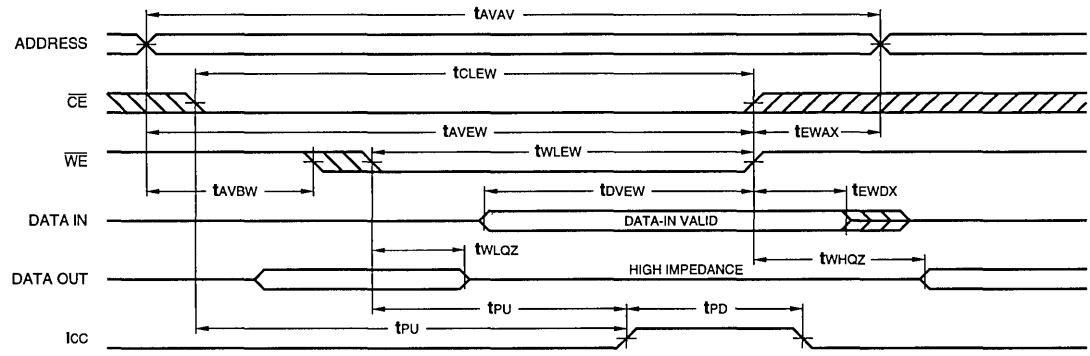


SWITCHING CHARACTERISTICS *Over Operating Range*

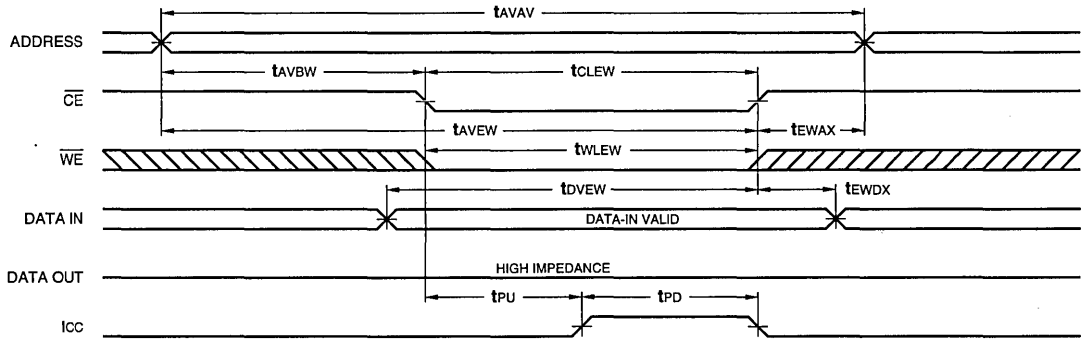
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C162–							
		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	20		20		15		12	
t_{CLEW}	Chip Enable Low to End of Write Cycle	15		15		12		10	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	15		15		12		10	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	15		15		12		10	
t_{DVEW}	Data Valid to End of Write Cycle	10		10		7		6	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		7		7		5		4

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND ≤ V_{OUT} ≤ V_{CC}. The device is disabled, i.e., $\overline{CE_1}$ = V_{CC}, $\overline{CE_2}$ = V_{CC}.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE_1}$ ≤ V_{IL}, $\overline{CE_2}$ ≤ V_{IL}, $\overline{WE}$ ≤ V_{IL}. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE_1}$ ≥ V_{IH}, $\overline{CE_2}$ ≥ V_{IH}.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE_1}$ = V_{CC}, $\overline{CE_2}$ = V_{CC}. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE_1}$ must be ≥ V_{CC} – 0.2 V or $\overline{CE_2}$ must be ≥ V_{CC} – 0.2 V. All other inputs must meet V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE_1}$, $\overline{CE_2}$, and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE_1}$ low, $\overline{CE_2}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE_1}$ and $\overline{CE_2}$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE_1}$ and $\overline{CE_2}$ active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE_1}$ and $\overline{CE_2}$ going active, the output remains in a high impedance state.

18. If $\overline{CE_1}$ and $\overline{CE_2}$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE_2}$ ($\overline{CE_1}$ active) or the falling edge of $\overline{CE_1}$ ($\overline{CE_2}$ active).

b. Falling edge of $\overline{WE}$ ($\overline{CE_1}$, $\overline{CE_2}$ active).

c. Transition on any address line ($\overline{CE_1}$, $\overline{CE_2}$ active).

d. Transition on any data line ($\overline{CE_1}$, $\overline{CE_2}$, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE_1}$, $\overline{CE_2}$, or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

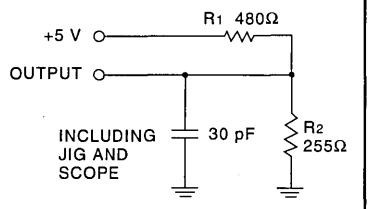


FIGURE 1b.

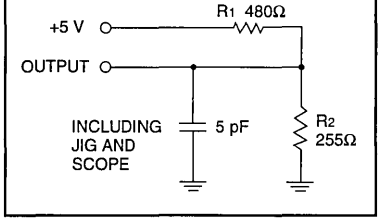
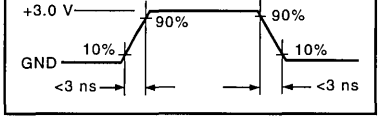
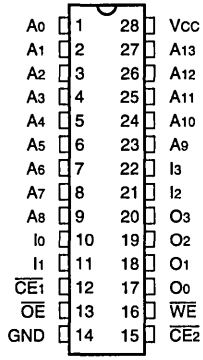


FIGURE 2.

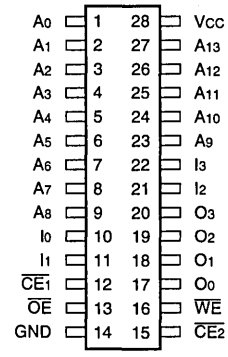


ORDERING INFORMATION

28-pin — 0.3" wide



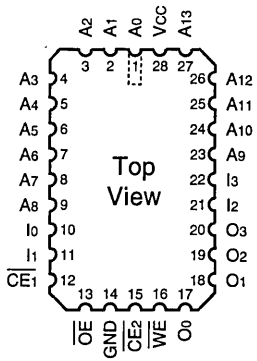
28-pin — 0.3" wide



Speed	Plastic DIP (P10)	Ceramic DIP (C5)	Plastic SOJ (W2)
	0°C to +70°C — Commercial Screening		
20 ns	L7C162PC20	L7C162CC20	L7C162WC20
15 ns	L7C162PC15	L7C162CC15	L7C162WC15
12 ns	L7C162PC12	L7C162CC12	L7C162WC12
	–40°C to +85°C — Commercial Screening		
20 ns	L7C162PI20		L7C162WI20
15 ns	L7C162PI15		L7C162WI15
12 ns	L7C162PI12		L7C162WI12
	–55°C to +125°C — Commercial Screening		
25 ns		L7C162CM25	
20 ns		L7C162CM20	
15 ns		L7C162CM15	
	–55°C to +125°C — MIL-STD-883 Compliant		
25 ns		L7C162CMB25	
20 ns		L7C162CMB20	
15 ns		L7C162CMB15	

ORDERING INFORMATION

28-pin



Speed	Ceramic Leadless Chip Carrier (K5)	
	0°C to +70°C — Commercial Screening	
20 ns	L7C162KC20	
15 ns	L7C162KC15	
12 ns	L7C162KC12	
	–40°C to +85°C — Commercial Screening	
20 ns		
15 ns		
12 ns		
	–55°C to +125°C — Commercial Screening	
25 ns	L7C162KM25	
20 ns	L7C162KM20	
15 ns	L7C162KM15	
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns	L7C162KMB25	
20 ns	L7C162KMB20	
15 ns	L7C162KMB15	

FEATURES

- 16K x 4 Static RAM with Common I/O
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 12 ns maximum
- Low Power Operation
  Active: 325 mW typical at 25 ns
  Standby: 400 µW typical
- Data Retention at 2 V for Battery Backup Operation
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with IDT 6198/7188 and Cypress CY7C164/166
- Package Styles Available:
  - 24-pin Plastic DIP
  - 22/24-pin Ceramic DIP
  - 24-pin Plastic SOJ
  - 22/28-pin Ceramic LCC

DESCRIPTION

The **L7C164** and **L7C166** are high-performance, low-power CMOS static RAMs. The storage cells are organized as 16,384 words by 4 bits per word. Data In and Data Out signals share I/O pins. The L7C164 has a single active-low Chip Enable. The L7C166 has a single Chip Enable and an Output Enable. These devices are available in four speeds with maximum access times from 12 ns to 25 ns.

Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 325 mW (typical) at 25 ns. Dissipation drops to 60 mW (typical) when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C164 and L7C166 consume only 30 µW (typical) at 3 V, allowing effective battery backup operation.

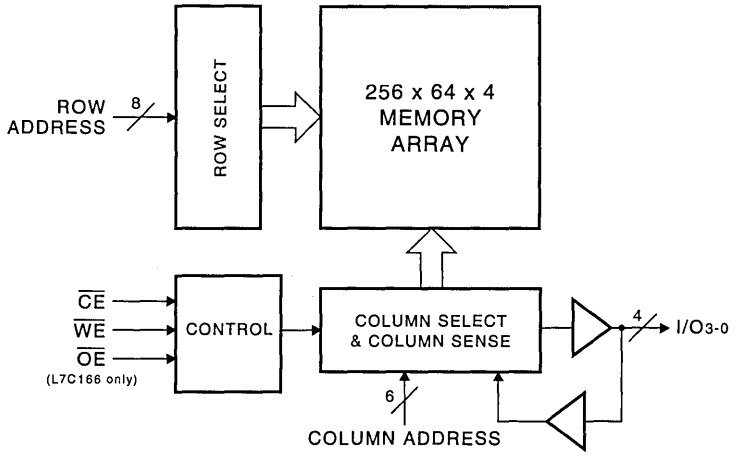
The L7C164 and L7C166 provide asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A_0 through A_{13}. For the L7C164, reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ LOW while $\overline{WE}$ remains HIGH. For the L7C166, $\overline{CE}$ and $\overline{OE}$ must be LOW while $\overline{WE}$ remains HIGH. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{CE}$ or $\overline{OE}$ is HIGH, or $\overline{WE}$ is LOW.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are LOW. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C164 and L7C166 can withstand an injection current of up to 200 mA on any pin without damage.

L7C164/166 BLOCK DIAGRAM



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Industrial	–40°C to +85°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Industrial	–40°C to +85°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L7C164/166			
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I_{IX}	Input Leakage Current	Ground ≤ V_{IN} ≤ V_{CC}	–10		+10	µA
I_{OZ}	Output Leakage Current	(Note 4)	–10		+10	µA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		12	25	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		80	300	µA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		10	150	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

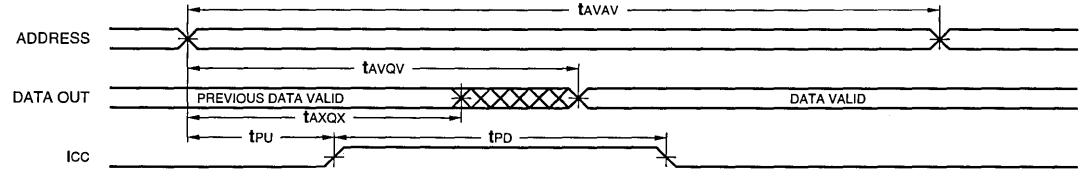
			L7C164/166-				
Symbol	Parameter	Test Condition	25	20	15	12	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	100	120	140	165	mA

SWITCHING CHARACTERISTICS *Over Operating Range*

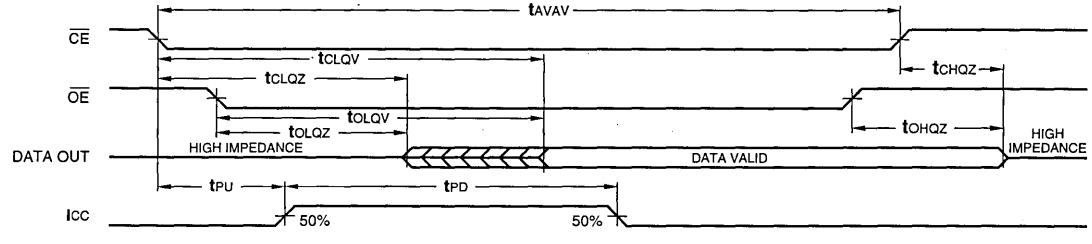
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C164/166–							
		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	25		20		15		12	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		25		20		15		12
t_{AXQX}	Address Change to Output Change	3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		25		20		15		12
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		10		8		8		5
t_{OLQV}	Output Enable Low to Output Valid		12		10		8		6
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		10		8		5		5
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		25		20		20		20
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0	

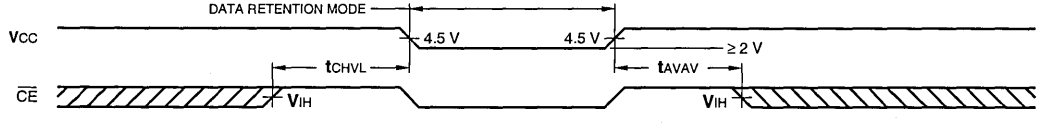
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}/\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

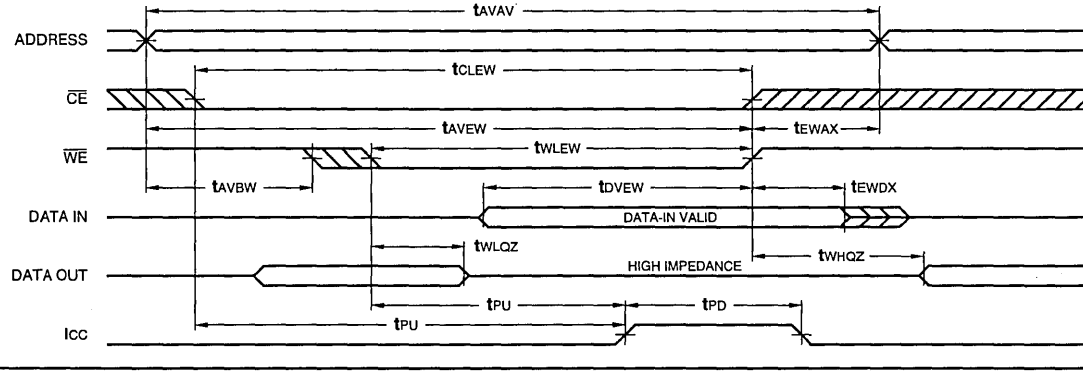


SWITCHING CHARACTERISTICS *Over Operating Range*

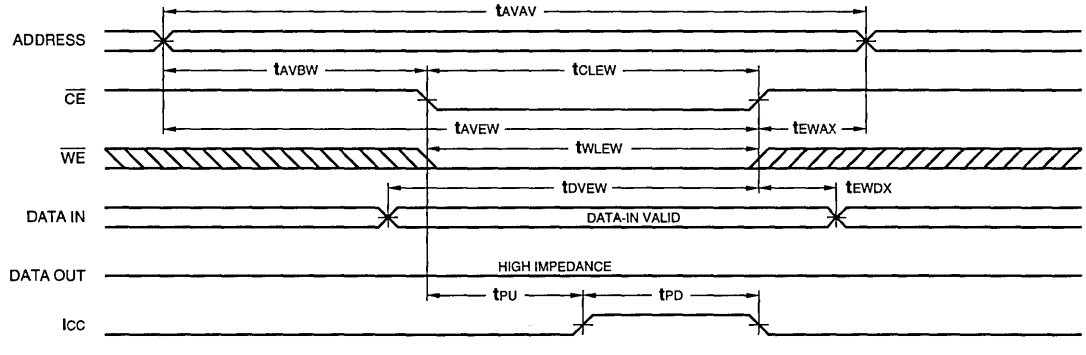
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C164/166–							
		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	20		20		15		12	
t_{CLEW}	Chip Enable Low to End of Write Cycle	15		15		12		10	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	15		15		12		10	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	15		15		12		10	
t_{DVEW}	Data Valid to End of Write Cycle	10		10		7		6	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		7		7		5		4

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND ≤ V_{OUT} ≤ V_{CC}. The device is disabled, i.e., $\overline{CE}$ = V_{CC}.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$ ≤ V_{IL}, $\overline{WE}$ ≤ V_{IL}. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}$ ≥ V_{IH}.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = V_{CC}. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be ≥ V_{CC} – 0.2 V. All other inputs must meet V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}$ going active, the output remains in a high impedance state.

18. If $\overline{CE}$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

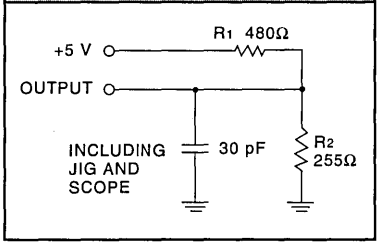


FIGURE 1b.

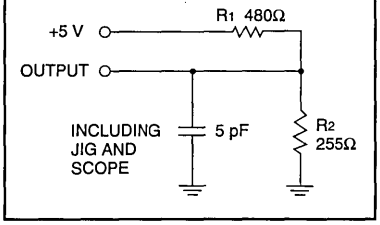
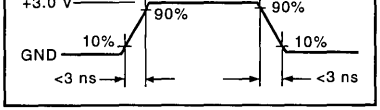


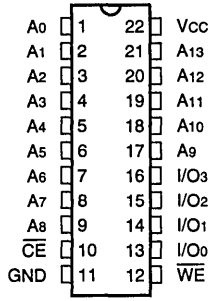
FIGURE 2.



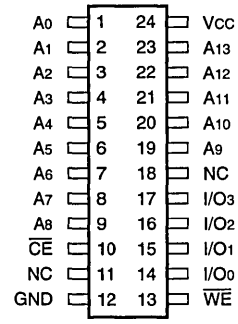
7

L7C164 — ORDERING INFORMATION

22-pin — 0.3" wide



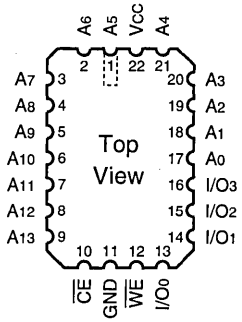
24-pin — 0.3" wide



Speed	Ceramic DIP (C3)	Plastic SOJ (W1)
	0°C to +70°C — Commercial Screening	
20 ns	L7C164CC20	L7C164WC20
15 ns	L7C164CC15	L7C164WC15
12 ns	L7C164CC12	L7C164WC12
	–40°C to +85°C — Commercial Screening	
20 ns		L7C164WI20
15 ns		L7C164WI15
12 ns		L7C164WI12
	–55°C to +125°C — Commercial Screening	
25 ns	L7C164CM25	
20 ns	L7C164CM20	
15 ns	L7C164CM15	
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns	L7C164CMB25	
20 ns	L7C164CMB20	
15 ns	L7C164CMB15	

L7C164 — ORDERING INFORMATION

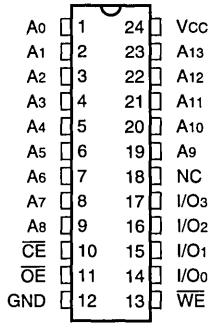
22-pin



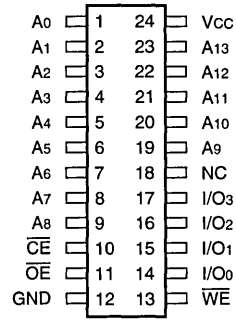
Speed	Ceramic Leadless Chip Carrier (K4)	
	0°C to +70°C — Commercial Screening	
20 ns	L7C164KC20	
15 ns	L7C164KC15	
12 ns	L7C164KC12	
	–40°C to +85°C — Commercial Screening	
20 ns		
15 ns		
12 ns		
	–55°C to +125°C — Commercial Screening	
25 ns	L7C164KM25	
20 ns	L7C164KM20	
15 ns	L7C164KM15	
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns	L7C164KMB25	
20 ns	L7C164KMB20	
15 ns	L7C164KMB15	

L7C166 — ORDERING INFORMATION

24-pin — 0.3" wide



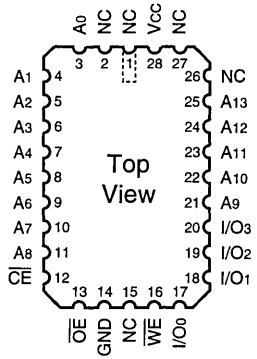
24-pin — 0.3" wide



Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic SOJ (W1)
	0°C to +70°C — Commercial Screening		
20 ns	L7C166PC20	L7C166CC20	L7C166WC20
15 ns	L7C166PC15	L7C166CC15	L7C166WC15
12 ns	L7C166PC12	L7C166CC12	L7C166WC12
	–40°C to +85°C — Commercial Screening		
20 ns	L7C166PI20		L7C166WI20
15 ns	L7C166PI15		L7C166WI15
12 ns	L7C166PI12		L7C166WI12
	–55°C to +125°C — Commercial Screening		
25 ns		L7C166CM25	
20 ns		L7C166CM20	
15 ns		L7C166CM15	
	–55°C to +125°C — MIL-STD-883 Compliant		
25 ns		L7C166CMB25	
20 ns		L7C166CMB20	
15 ns		L7C166CMB15	

L7C166 — ORDERING INFORMATION

28-pin



Speed	Ceramic Leadless Chip Carrier (K5)	
	0°C to +70°C — Commercial Screening	
20 ns	L7C166KC20	
15 ns	L7C166KC15	
12 ns	L7C166KC12	
	–40°C to +85°C — Commercial Screening	
20 ns		
15 ns		
12 ns		
	–55°C to +125°C — Commercial Screening	
25 ns	L7C166KM25	
20 ns	L7C166KM20	
15 ns	L7C166KM15	
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns	L7C166KMB25	
20 ns	L7C166KMB20	
15 ns	L7C166KMB15	

FEATURES

- 64K x 4 Static RAM with Common I/O
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 15 ns maximum
- Low Power Operation
  Active: 210 mW typical at 35 ns
  Standby: 5 mW typical
- Data retention at 2 V for Battery Backup Operation
- DECC SMD No.
  5962-88681 — L7C194
  5962-89524 — L7C195
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with IDT 71258/61298 and Cypress CY7C194/195
- Package Styles Available:
  - 24/28-pin Plastic DIP
  - 24/28-pin Ceramic DIP
  - 24/28-pin Plastic SOJ
  - 28-pin Ceramic LCC

DESCRIPTION

The **L7C194** and **L7C195** are high-performance, low-power CMOS static RAMs. The storage cells are organized as 65,536 words by 4 bits per word. Data In and Data Out signals share I/O pins. The L7C194 has a single active-low Chip Enable. The L7C195 has a single Chip Enable and an Output Enable. These devices are available in four speeds with maximum access times from 15 ns to 35 ns.

Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 210 mW (typical) at 35 ns. Dissipation drops to 50 mW (typical) when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C194 and L7C195 consume only 150 µW (typical) at 3 V, allowing effective battery backup operation.

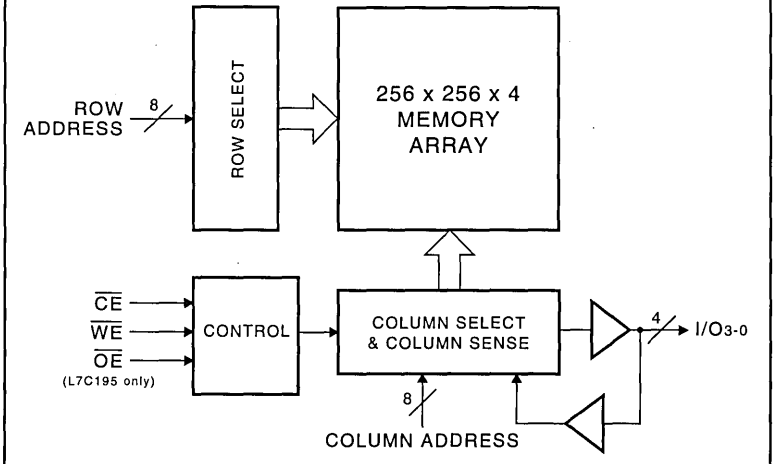
The L7C194 and L7C195 provide asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A0 through A15. For the L7C194, reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ LOW while $\overline{WE}$ remains HIGH. For the L7C195, $\overline{CE}$ and $\overline{OE}$ must be LOW. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{CE}$ or $\overline{OE}$ is HIGH, or $\overline{WE}$ is LOW.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are LOW. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C194 and L7C195 can withstand an injection current of up to 200 mA on any pin without damage.

L7C194/195 BLOCK DIAGRAM



7

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Industrial	−40°C to +85°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	−55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Industrial	−40°C to +85°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	−55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L7C194/195			
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	−3.0		0.8	V
I_{IX}	Input Leakage Current	Ground ≤ V_{IN} ≤ V_{CC}	−10		+10	µA
I_{OZ}	Output Leakage Current	(Note 4)	−10		+10	µA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		10	20	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		1	3	mA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		50	200	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

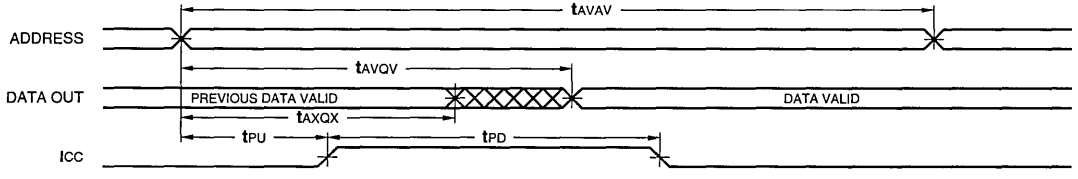
			L7C194/195-				
Symbol	Parameter	Test Condition	35	25	20	15	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	75	100	125	160	mA

SWITCHING CHARACTERISTICS *Over Operating Range*

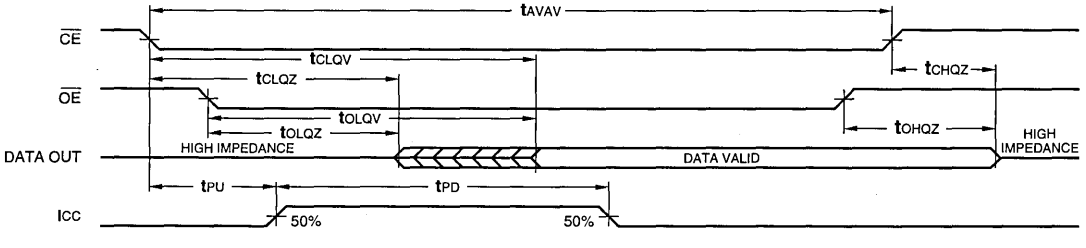
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C194/195–							
		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	35		25		20		15	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		35		25		20		15
t_{AXQX}	Address Change to Output Change	3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		35		25		20		15
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		15		10		8		8
t_{OLQV}	Output Enable Low to Output Valid		15		12		10		8
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		10		10		8		5
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		35		25		20		20
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0	

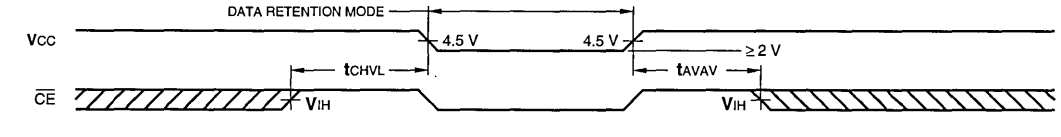
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}$/$\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

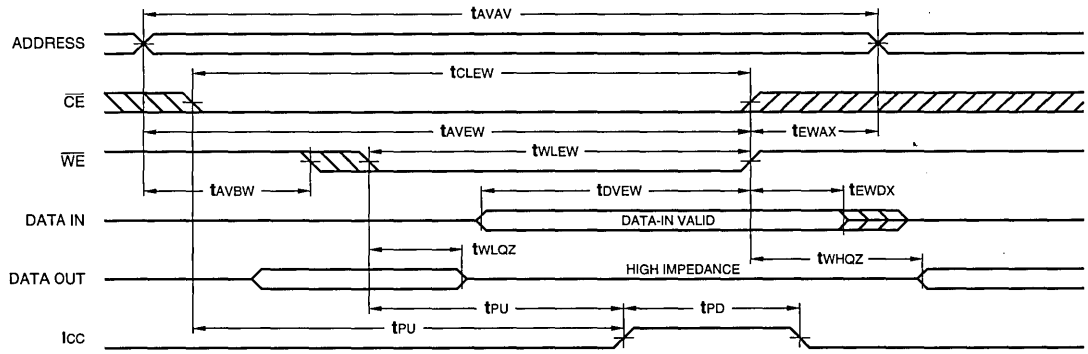


SWITCHING CHARACTERISTICS *Over Operating Range*

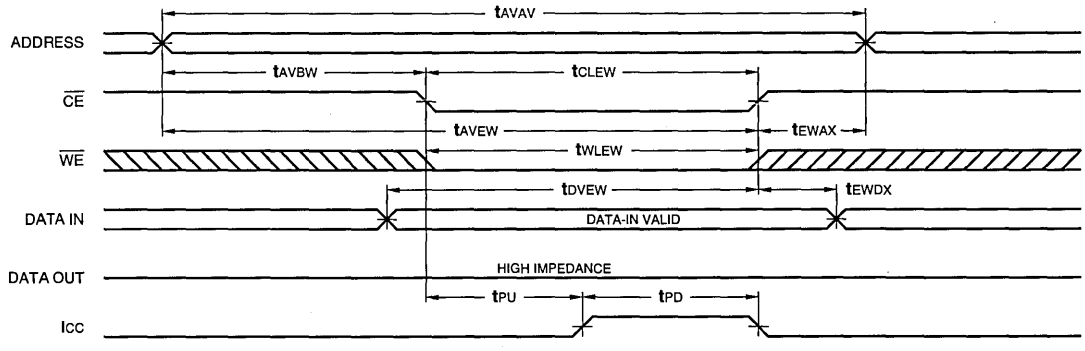
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C194/195–							
		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	25		20		20		15	
t_{CLEW}	Chip Enable Low to End of Write Cycle	25		15		15		12	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	25		15		15		12	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	20		15		15		12	
t_{DVEW}	Data Valid to End of Write Cycle	15		10		10		7	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		10		7		7		5

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND ≤ V_{OUT} ≤ V_{CC}. The device is disabled, i.e., $\overline{CE}$ = V_{CC}.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$ ≤ V_{IL}, $\overline{WE}$ ≤ V_{IL}. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}$ ≥ V_{IH}.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = V_{CC}. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be ≥ V_{CC} – 0.2 V. All other inputs must meet V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}$ going active, the output remains in a high impedance state.

18. If $\overline{CE}$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

7

FIGURE 1a.

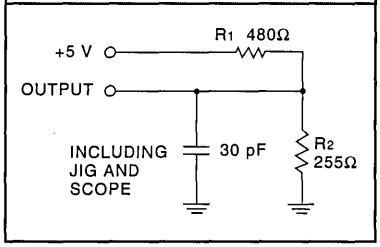


FIGURE 1b.

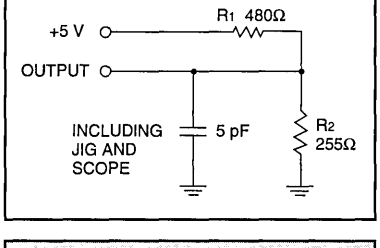
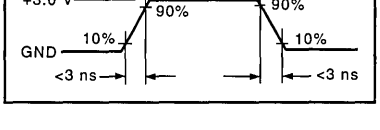
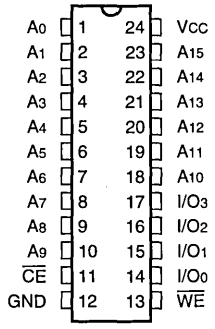


FIGURE 2.

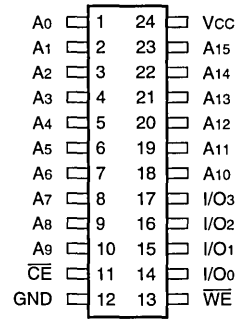


L7C194 — ORDERING INFORMATION

24-pin — 0.3" wide



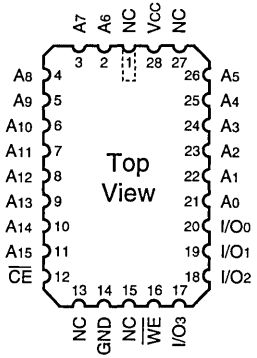
24-pin — 0.3" wide



Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic SOJ (W1)
	0°C to +70°C — Commercial Screening		
25 ns	L7C194PC25	L7C194CC25	L7C194WC25
20 ns	L7C194PC20	L7C194CC20	L7C194WC20
15 ns	L7C194PC15	L7C194CC15	L7C194WC15
	–40°C to +85°C — Commercial Screening		
25 ns	L7C194PI25		L7C194WI25
20 ns	L7C194PI20		L7C194WI20
15 ns	L7C194PI15		L7C194WI15
	–55°C to +125°C — Commercial Screening		
35 ns		L7C194CM35	
25 ns		L7C194CM25	
20 ns		L7C194CM20	
	–55°C to +125°C — MIL-STD-883 Compliant		
35 ns		L7C194CMB35	
25 ns		L7C194CMB25	
20 ns		L7C194CMB20	

L7C194 — ORDERING INFORMATION

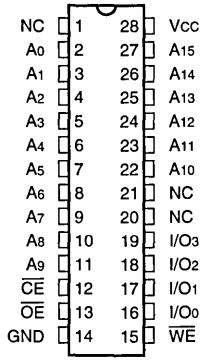
28-pin



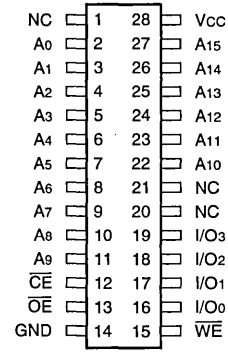
Speed	Ceramic Leadless Chip Carrier (K5)	
	0°C to +70°C — Commercial Screening	
25 ns	L7C194KC25	
20 ns	L7C194KC20	
15 ns	L7C194KC15	
	–40°C to +85°C — Commercial Screening	
25 ns		
20 ns		
15 ns		
	–55°C to +125°C — Commercial Screening	
35 ns	L7C194KM35	
25 ns	L7C194KM25	
20 ns	L7C194KM20	
	–55°C to +125°C — MIL-STD-883 Compliant	
35 ns	L7C194KMB35	
25 ns	L7C194KMB25	
20 ns	L7C194KMB20	

L7C195 — ORDERING INFORMATION

28-pin — 0.3" wide



28-pin — 0.3" wide



Speed	Plastic DIP (P10)	Ceramic DIP (C5)	Plastic SOJ (W2)
	0°C to +70°C — Commercial Screening		
25 ns	L7C195PC25	L7C195CC25	L7C195WC25
20 ns	L7C195PC20	L7C195CC20	L7C195WC20
15 ns	L7C195PC15	L7C195CC15	L7C195WC15
	–40°C to +85°C — Commercial Screening		
25 ns	L7C195PI25		L7C195WI25
20 ns	L7C195PI20		L7C195WI20
15 ns	L7C195PI15		L7C195WI15
	–55°C to +125°C — Commercial Screening		
35 ns		L7C195CM35	
25 ns		L7C195CM25	
20 ns		L7C195CM20	
	–55°C to +125°C — MIL-STD-883 Compliant		
35 ns		L7C195CMB35	
25 ns		L7C195CMB25	
20 ns		L7C195CMB20	

L7C197
256K x 1 Static RAM

FEATURES

- 256K x 1 Static RAM with Separate I/O, Chip Select Powerdown
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 15 ns maximum
- Low Power Operation
  Active: 165 mW typical at 35 ns
  Standby: 5 mW typical
- Data Retention at 2 V for Battery Backup Operation
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with IDT71257, Cypress CY7C197
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Ceramic DIP
  - 24-pin Plastic SOJ
  - 28-pin Ceramic LCC

DESCRIPTION

The **L7C197** is a high-performance, low-power CMOS static RAM. The storage circuitry is organized as 262,144 words by 1 bit per word. This device is available in four speeds with maximum access times from 15 ns to 35 ns.

Operation is from a single +5 V power supply and all interface signals are TTL compatible. Power consumption is 165 mW (typical) at 35 ns. Dissipation drops to 50 mW (typical) when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C197 consumes only 150 µW (typical) at 3 V, allowing effective battery backup operation.

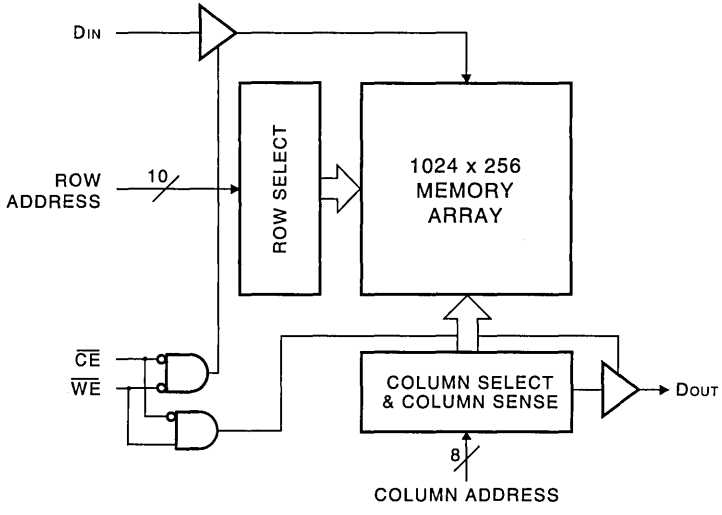
The L7C197 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state output simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A_0 through A_{17}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ LOW while $\overline{WE}$ remains HIGH. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}$ is HIGH or $\overline{WE}$ is LOW.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both LOW. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C197 can withstand an injection current of up to 200 mA on any pin without damage.

L7C197 BLOCK DIAGRAM



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Industrial	–40°C to +85°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Industrial	–40°C to +85°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L7C197			
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I_{IX}	Input Leakage Current	Ground ≤ V_{IN} ≤ V_{CC}	–10		+10	µA
I_{OZ}	Output Leakage Current	(Note 4)	–10		+10	µA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		10	20	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		1	3	mA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		50	200	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

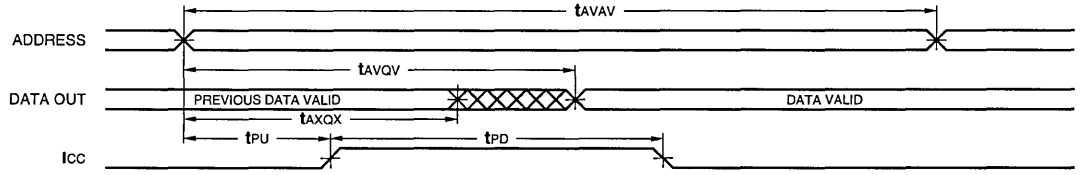
			L7C197-				
Symbol	Parameter	Test Condition	35	25	20	15	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	75	100	125	160	mA

SWITCHING CHARACTERISTICS *Over Operating Range*

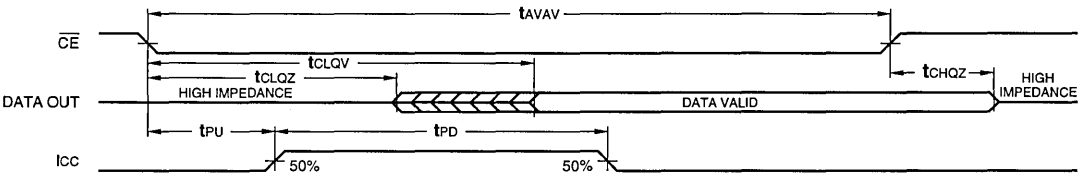
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C197–							
		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	35		25		20		15	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		35		25		20		15
t_{AXQX}	Address Change to Output Change	3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		35		25		20		15
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		15		10		8		8
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		35		25		20		20
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0	

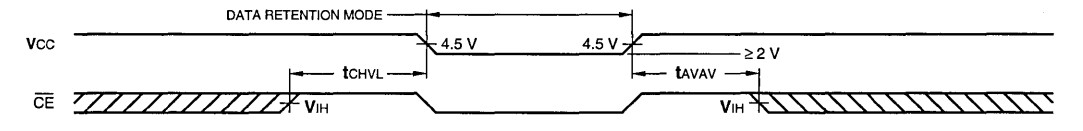
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*



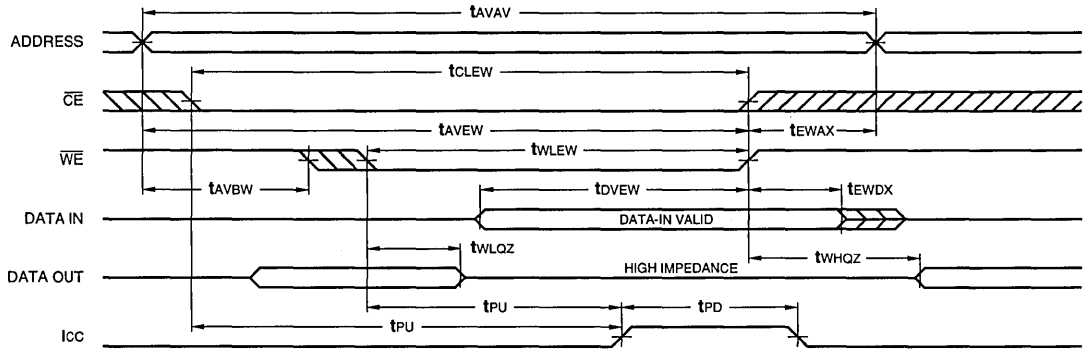
7

SWITCHING CHARACTERISTICS *Over Operating Range*

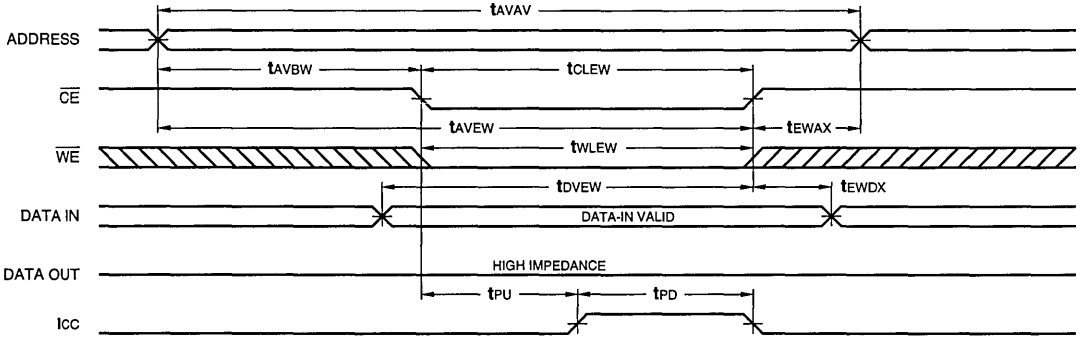
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C197–							
		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	25		20		20		15	
t_{CLEW}	Chip Enable Low to End of Write Cycle	25		15		15		12	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	25		15		15		12	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	20		15		15		12	
t_{DVEW}	Data Valid to End of Write Cycle	15		10		10		7	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		10		7		7		5

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND ≤ V_{OUT} ≤ V_{CC}. The device is disabled, i.e., $\overline{CE}$ = V_{CC}.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$ ≤ V_{IL}, $\overline{WE}$ ≤ V_{IL}. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}$ ≥ V_{IH}.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = V_{CC}. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be ≥ V_{CC} – 0.2 V. All other inputs must meet V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}$ going active, the output remains in a high impedance state.

18. If $\overline{CE}$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

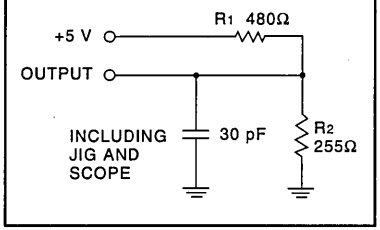


FIGURE 1b.

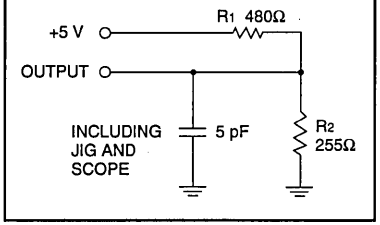
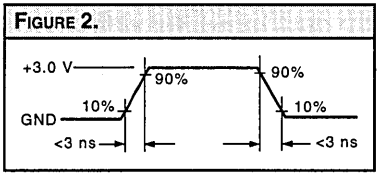


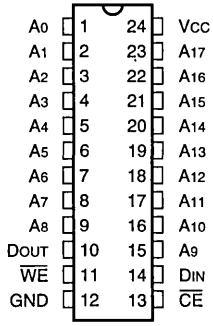
FIGURE 2.



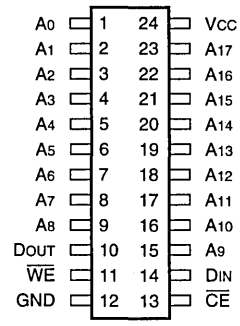
7

ORDERING INFORMATION

24-pin — 0.3" wide



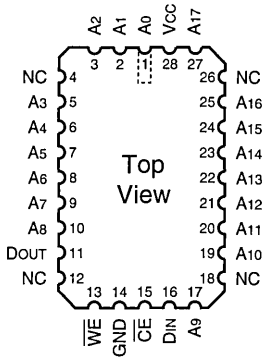
24-pin — 0.3" wide



Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic SOJ (W1)
	0°C to +70°C — COMMERCIAL SCREENING		
25 ns	L7C197PC25	L7C197CC25	L7C197WC25
20 ns	L7C197PC20	L7C197CC20	L7C197WC20
15 ns	L7C197PC15	L7C197CC15	L7C197WC15
	–40°C to +85°C — COMMERCIAL SCREENING		
25 ns	L7C197PI25		L7C197WI25
20 ns	L7C197PI20		L7C197WI20
15 ns	L7C197PI15		L7C197WI15
	–55°C to +125°C — COMMERCIAL SCREENING		
35 ns		L7C197CM35	
25 ns		L7C197CM25	
20 ns		L7C197CM20	
	–55°C to +125°C — MIL-STD-883 COMPLIANT		
35 ns		L7C197CMB35	
25 ns		L7C197CMB25	
20 ns		L7C197CMB20	

ORDERING INFORMATION

28-pin



Speed	Ceramic Leadless Chip Carrier (K5)	
	0°C to +70°C — COMMERCIAL SCREENING	
25 ns	L7C197KC25	
20 ns	L7C197KC20	
15 ns	L7C197KC15	
	–40°C to +85°C — COMMERCIAL SCREENING	
25 ns		
20 ns		
15 ns		
	–55°C to +125°C — COMMERCIAL SCREENING	
35 ns	L7C197KM35	
25 ns	L7C197KM25	
20 ns	L7C197KM20	
	–55°C to +125°C — MIL-STD-883 COMPLIANT	
35 ns	L7C197KMB35	
25 ns	L7C197KMB25	
20 ns	L7C197KMB20	

FEATURES

- 32K x 8 Static RAM with Chip Select Powerdown, Output Enable
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 15 ns maximum
- Low Power Operation
  Active: 350 mW typical at 35 ns
  Standby: 5 mW typical
- Data Retention at 2 V for Battery Backup Operation
- DECC SMD No. 5962-88662
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with IDT71256, Cypress CY7C198/199
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Ceramic DIP
  - 28-pin Plastic SOJ
  - 28-pin Ceramic Flatpack
  - 28-pin Ceramic LCC
  - 32-pin Ceramic LCC

DESCRIPTION

The **L7C199** is a high-performance, low-power CMOS static RAM. The storage circuitry is organized as 32,768 words by 8 bits per word. The 8 Data In and Data Out signals share I/O pins. This device is available in four speeds with maximum access times from 15 ns to 35 ns.

Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 350 mW (typical) at 35 ns. Dissipation drops to 50 mW (typical) when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C199 consumes only 150 µW (typical) , at 3 V, allowing effective battery backup operation.

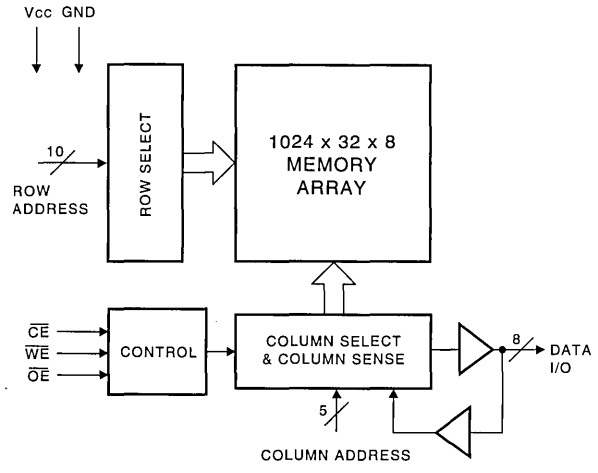
The L7C199 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{14}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ and $\overline{OE}$ LOW while $\overline{WE}$ remains HIGH. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{CE}$ or $\overline{OE}$ is HIGH, or $\overline{WE}$ is LOW.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both LOW. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C199 can withstand an injection current of up to 200 mA on any pin without damage.

L7C199 Block Diagram



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Industrial	–40°C to +85°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Industrial	–40°C to +85°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L7C199			
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I_{IX}	Input Leakage Current	Ground ≤ V_{IN} ≤ V_{CC}	–10		+10	µA
I_{OZ}	Output Leakage Current	(Note 4)	–10		+10	µA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		10	20	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		1	3	mA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		50	200	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

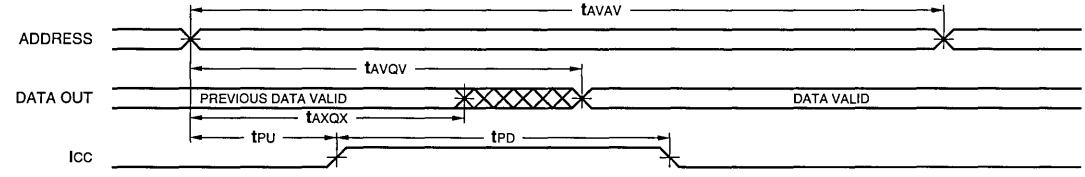
			L7C199-				
Symbol	Parameter	Test Condition	35	25	20	15	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	95	120	145	180	mA

SWITCHING CHARACTERISTICS *Over Operating Range*

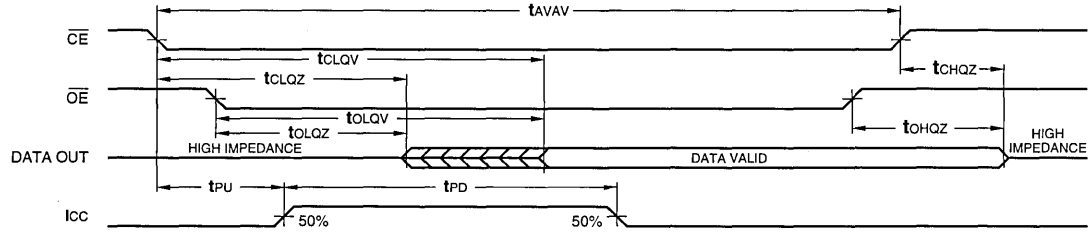
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C199–							
		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	35		25		20		15	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		35		25		20		15
t_{AXQX}	Address Change to Output Change	3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		35		25		20		15
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		15		10		8		8
t_{OLQV}	Output Enable Low to Output Valid		15		12		10		8
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		10		10		8		5
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		35		25		20		20
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0	

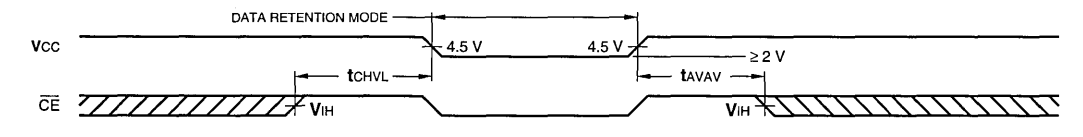
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}/\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

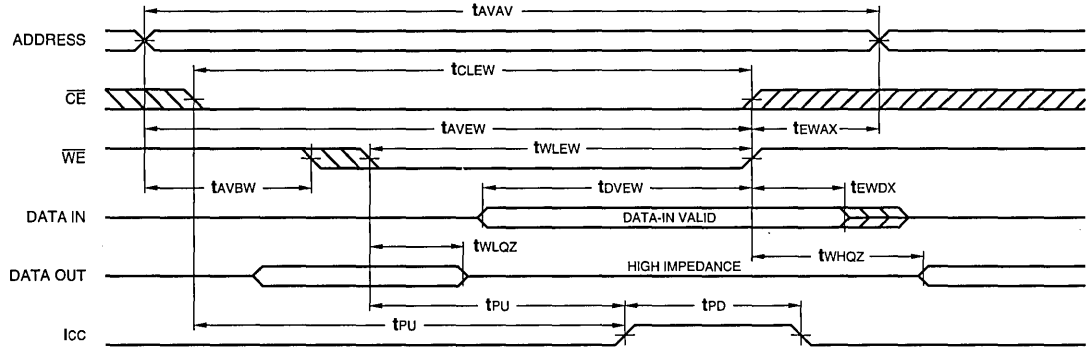


SWITCHING CHARACTERISTICS *Over Operating Range*

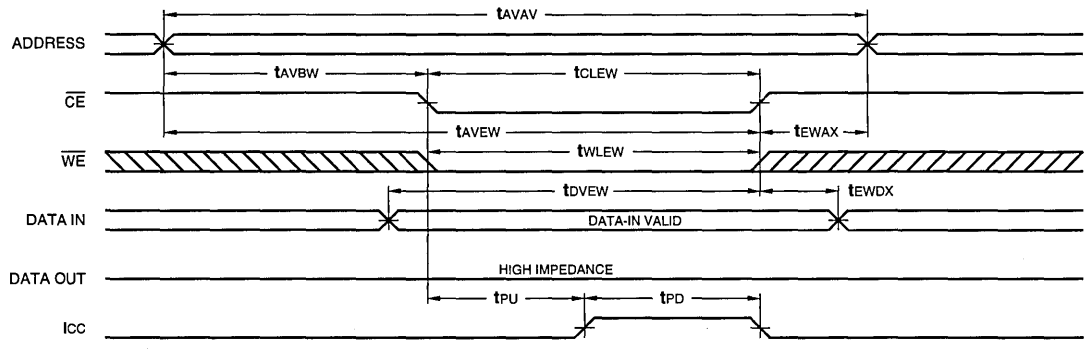
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C199–							
		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	25		20		20		15	
t_{CLEW}	Chip Enable Low to End of Write Cycle	25		15		15		12	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	25		15		15		12	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	20		15		15		12	
t_{DVEW}	Data Valid to End of Write Cycle	15		10		10		7	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		10		7		7		5

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND ≤ V_{OUT} ≤ V_{CC}. The device is disabled, i.e., $\overline{CE}$ = V_{CC}.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$ ≤ V_{IL}, $\overline{WE}$ ≤ V_{IL}. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}$ ≥ V_{IH}.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = V_{CC}. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be ≥ V_{CC} – 0.2 V. All other inputs must meet V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}$ going active, the output remains in a high impedance state.

18. If $\overline{CE}$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

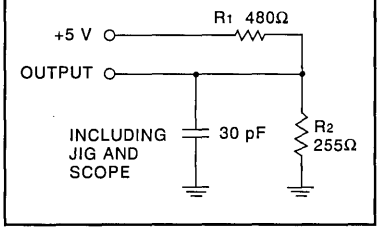


FIGURE 1b.

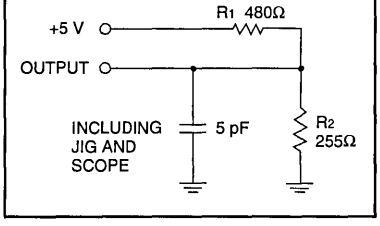
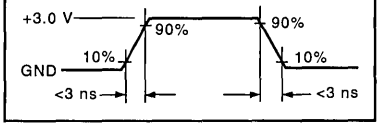


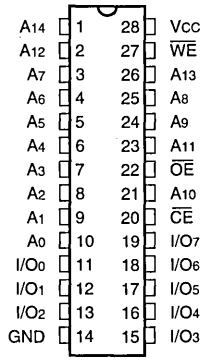
FIGURE 2.



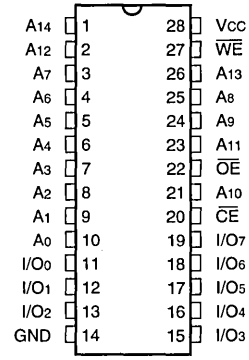
7

ORDERING INFORMATION

28-pin — 0.3" wide



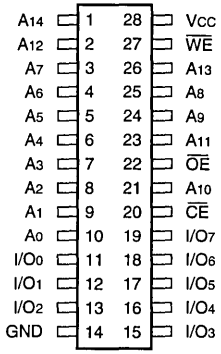
28-pin — 0.6" wide



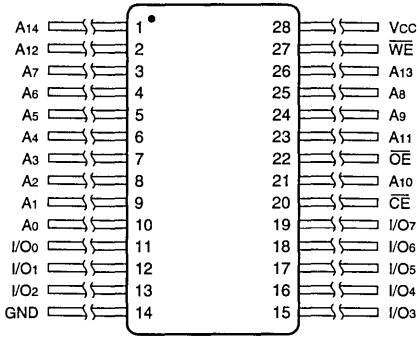
Speed	Plastic DIP (P10)	Ceramic DIP (C5)	Plastic DIP (P9)	Ceramic DIP (C6)
	0°C to +70°C — Commercial Screening			
25 ns	L7C199PC25	L7C199CC25	L7C199NC25	L7C199IC25
20 ns	L7C199PC20	L7C199CC20	L7C199NC20	L7C199IC20
15 ns	L7C199PC15	L7C199CC15	L7C199NC15	L7C199IC15
	–40°C to +85°C — Commercial Screening			
25 ns	L7C199PI25		L7C199NI25	
20 ns	L7C199PI20		L7C199NI20	
15 ns	L7C199PI15		L7C199NI15	
	–55°C to +125°C — Commercial Screening			
35 ns		L7C199CM35		L7C199IM35
25 ns		L7C199CM25		L7C199IM25
20 ns		L7C199CM20		L7C199IM20
	–55°C to +125°C — MIL-STD-883 Compliant			
35 ns		L7C199CMB35		L7C199IMB35
25 ns		L7C199CMB25		L7C199IMB25
20 ns		L7C199CMB20		L7C199IMB20

ORDERING INFORMATION

28-pin — 0.3" wide



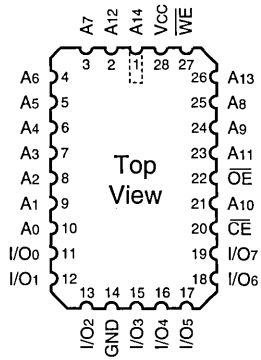
28-pin



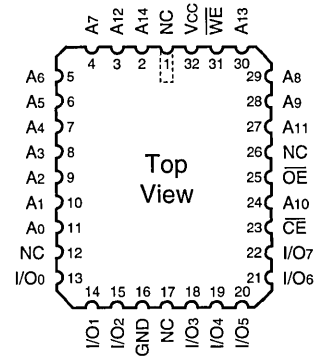
Speed	Plastic SOJ (W2)	Ceramic Flatpack (M2)
	0°C to +70°C — Commercial Screening	
25 ns	L7C199WC25	L7C199MC25
20 ns	L7C199WC20	L7C199MC20
15 ns	L7C199WC15	L7C199MC15
	–40°C to +85°C — Commercial Screening	
25 ns	L7C199WI25	
20 ns	L7C199WI20	
15 ns	L7C199WI15	
	–55°C to +125°C — Commercial Screening	
35 ns		L7C199MM35
25 ns		L7C199MM25
20 ns		L7C199MM20
	–55°C to +125°C — MIL-STD-883 Compliant	
35 ns		L7C199MMB35
25 ns		L7C199MMB25
20 ns		L7C199MMB20

ORDERING INFORMATION

28-pin



32-pin



Speed	Ceramic Leadless Chip Carrier (K5)	Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — Commercial Screening	
25 ns	L7C199KC25	L7C199TC25
20 ns	L7C199KC20	L7C199TC20
15 ns	L7C199KC15	L7C199TC15
	–40°C to +85°C — Commercial Screening	
25 ns		
20 ns		
15 ns		
	–55°C to +125°C — Commercial Screening	
35 ns	L7C199KM35	L7C199TM35
25 ns	L7C199KM25	L7C199TM25
20 ns	L7C199KM20	L7C199TM20
	–55°C to +125°C — MIL-STD-883 Compliant	
35 ns	L7C199KMB35	L7C199TMB35
25 ns	L7C199KMB25	L7C199TMB25
20 ns	L7C199KMB20	L7C199TMB20

FEATURES

- 256K x 4 Static RAM with Chip Select Powerdown, Output Enable
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 17 ns maximum
- Low Power Operation
  Active: 400 mW typical at 25 ns
  Standby: 5 mW typical
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with Cypress CY7C106
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Sidebraze, Hermetic DIP
  - 28-pin Plastic SOJ

DESCRIPTION

The **L7C106** is a high-performance, low-power CMOS static RAM. The storage circuitry is organized as 262,144 words by 4 bits per word. The 4 Data In and Data Out signals share I/O pins. The L7C106 has an active-low Chip Enable and a separate Output Enable. This device is available in three speeds with maximum access times from 17 ns to 25 ns.

Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 400 mW (typical) at 25 ns. Dissipation drops to 50 mW (typical) when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C106 consumes only 1.5 mW (typical), at 3 V, allowing effective battery backup operation.

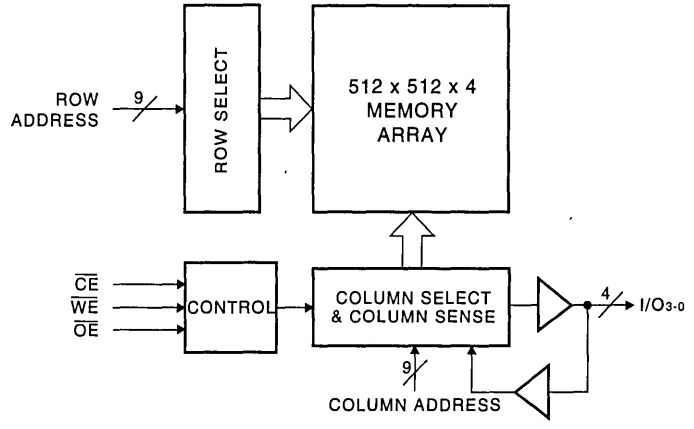
The L7C106 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{17}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ and $\overline{OE}$ LOW while $\overline{WE}$ remains HIGH. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{CE}$ or $\overline{OE}$ is HIGH, or $\overline{WE}$ is LOW.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both LOW. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C106 can withstand an injection current of up to 200 mA on any pin without damage.

L7C106 Block Diagram



7

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Active Operation, Industrial	−40°C to +85°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Data Retention, Commercial	0°C to +70°C	$2.0\ V \le V_{CC} \le 5.5\ V$
Data Retention, Industrial	−40°C to +85°C	$2.0\ V \le V_{CC} \le 5.5\ V$

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L7C106			
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	−3.0		0.8	V
I_{IX}	Input Leakage Current	$GND \le V_{IN} \le V_{CC}$	−10		+10	µA
I_{OZ}	Output Leakage Current	(Note 4)	−10		+10	µA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		10	20	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		1	4.0	mA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		500	1000	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

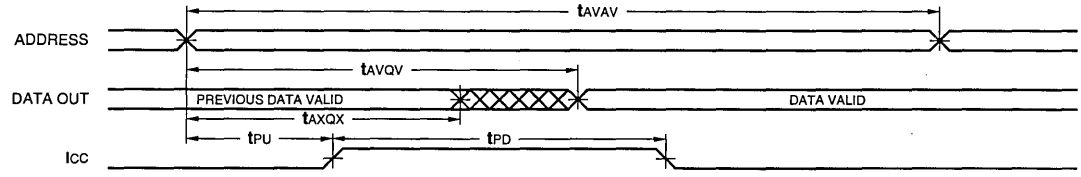
			L7C106-			
Symbol	Parameter	Test Condition	25	20	17	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	100	125	145	mA

SWITCHING CHARACTERISTICS *Over Operating Range*

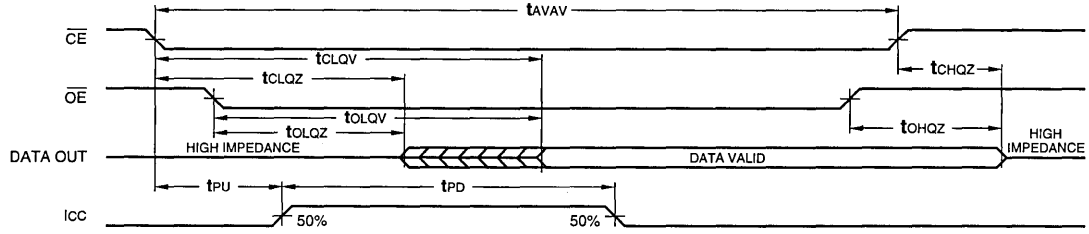
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

Symbol	Parameter	L7C106– 25 Min	25 Max	20 Min	20 Max	17 Min	17 Max
t_{AVAV}	Read Cycle Time	25		20		17	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		25		20		17
t_{AXQX}	Address Change to Output Change	3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		25		20		17
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		10		8		8
t_{OLQV}	Output Enable Low to Output Valid		10		10		9
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		10		7		6
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		25		20		17
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0	

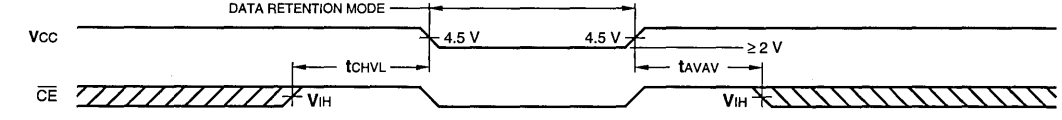
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}/\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

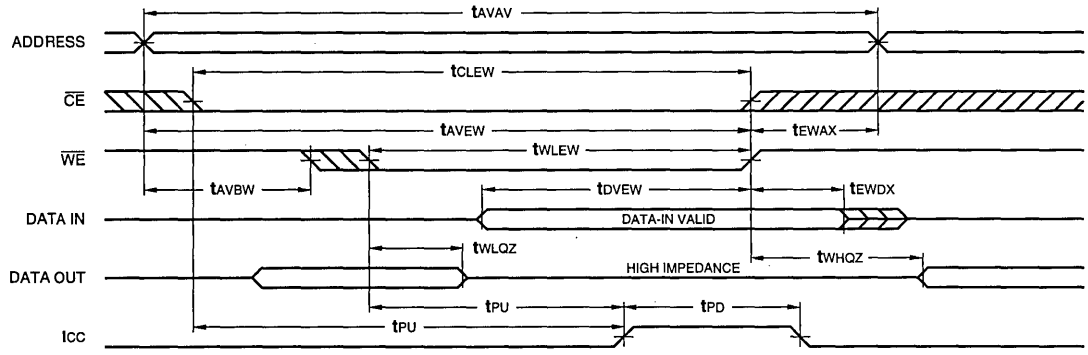


SWITCHING CHARACTERISTICS *Over Operating Range*

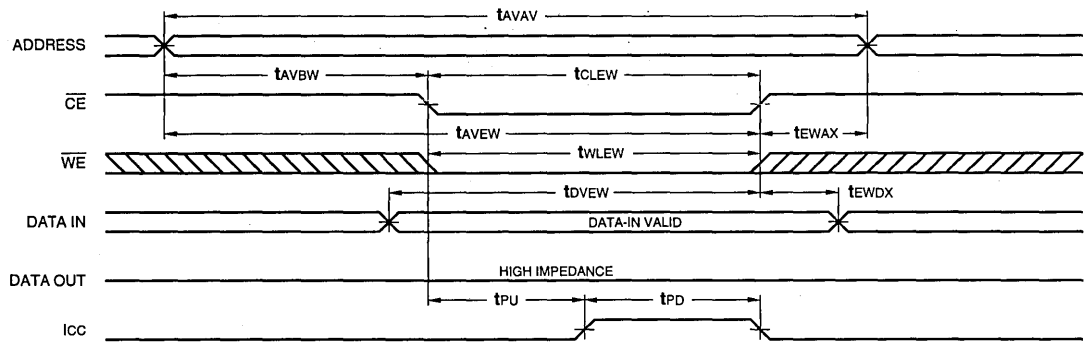
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

Symbol	Parameter	L7C106– 25 Min	25 Max	20 Min	20 Max	17 Min	17 Max
t_{AVAV}	Write Cycle Time	20		20		17	
t_{CLEW}	Chip Enable Low to End of Write Cycle	15		15		13	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	15		15		13	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	15		15		13	
t_{DVEW}	Data Valid to End of Write Cycle	10		9		8	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		7		7		6

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND ≤ V_{OUT} ≤ V_{CC}. The device is disabled, i.e., $\overline{CE}$ = V_{CC}.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$ ≤ V_{IL}, $\overline{WE}$ ≤ V_{IL}. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}$ ≥ V_{IH}.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = V_{CC}. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be ≥ V_{CC} – 0.2 V. All other inputs must meet V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}$ going active, the output remains in a high impedance state.

18. If $\overline{CE}$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

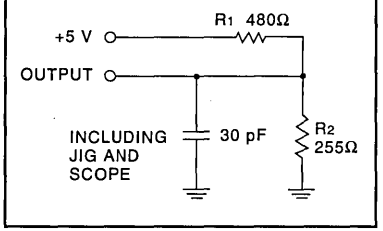


FIGURE 1b.

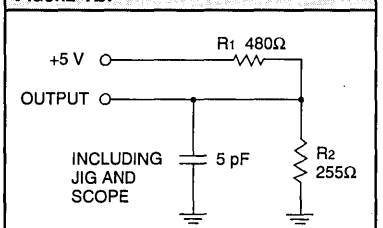
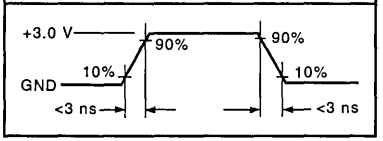


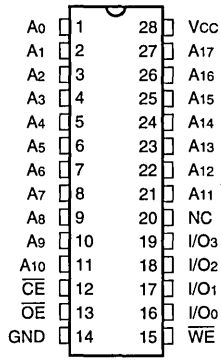
FIGURE 2.



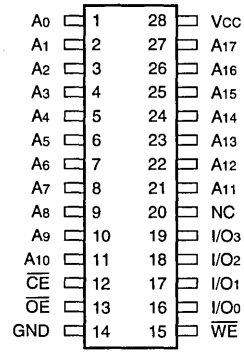
7

ORDERING INFORMATION

28-pin — 0.4" wide



28-pin — 0.4" wide



Speed	Plastic DIP (P11)	Sidebraze Hermetic DIP (D11)	Plastic SOJ (W7)
	0°C to +70°C — Commercial Screening		
25 ns	L7C106PC25	L7C106DC25	L7C106WC25
20 ns	L7C106PC20	L7C106DC20	L7C106WC20
17 ns	L7C106PC17	L7C106DC17	L7C106WC17
	–40°C to +85°C — Commercial Screening		
25 ns	L7C106PI25		L7C106WI25
20 ns	L7C106PI20		L7C106WI20
17 ns	L7C106PI17		L7C106WI17

L7C108/109
128K x 8 Static RAM (Low Power)

FEATURES

- 128K x 8 Static RAM with Chip Select Powerdown, Output Enable
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 17 ns maximum
- Low Power Operation
  Active: 550 mW typical at 25 ns
  Standby: 5 mW typical
- Data Retention at 2 V for Battery Backup Operation
- DECC SMD No. 5962-89598
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with Cypress CY7C108/109, IDT71024/71B024, Micron MT5C1008, Motorola MCM6226A/62L26A, Sony CXK581020
- Package Styles Available:
  - 32-pin Sidebraze, Hermetic DIP
  - 32-pin Plastic SOJ
  - 32-pin Ceramic LCC

DESCRIPTION

The **L7C108** and **L7C109** are high-performance, low-power CMOS static RAMs. The storage circuitry is organized as 131,072 words by 8 bits per word. The 8 Data In and Data Out signals share I/O pins. The L7C108 has a single active-low Chip Enable. The L7C109 has two Chip Enables (one active-low). These devices are available in three speeds with maximum access times from 17 ns to 25 ns.

Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 550 mW (typical) at 25 ns. Dissipation drops to 50 mW (typical) when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C108 and L7C109 consume only 1.5 mW (typical), at 3 V, allowing effective battery backup operation.

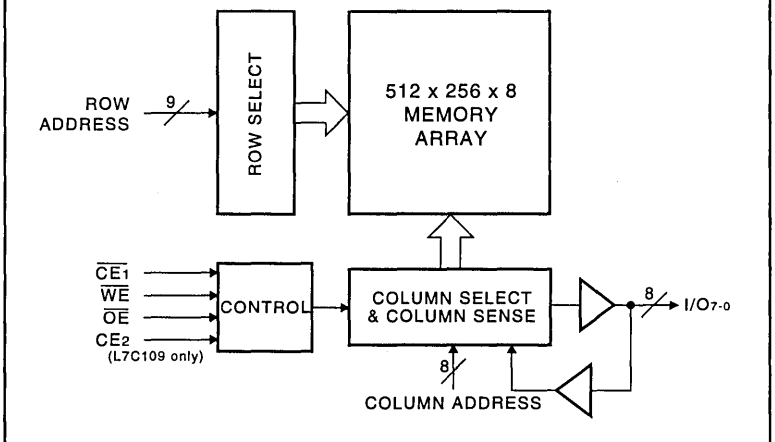
The L7C108 and L7C109 provide asynchronous (unclocked) operation with matching access and cycle times. The Chip Enables and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{16}. For the L7C108, reading from a designated location is accomplished by presenting an address and driving $\overline{CE_1}$ and $\overline{OE}$ LOW while $\overline{WE}$ remains HIGH. For the L7C109, $\overline{CE_1}$ and $\overline{OE}$ must be LOW while CE_2 and $\overline{WE}$ are HIGH. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{CE_1}$ or $\overline{OE}$ is HIGH, or CE_2 (L7C109) or $\overline{WE}$ is LOW.

Writing to an addressed location is accomplished when the active-low $\overline{CE_1}$ and $\overline{WE}$ inputs are both LOW, and CE_2 (L7C109) is HIGH. Any of these signals may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C108 and L7C109 can withstand an injection current of up to 200 mA on any pin without damage.

L7C108/109 Block Diagram



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Active Operation, Industrial	−40°C to +85°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Active Operation, Military	−55°C to +125°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Data Retention, Commercial	0°C to +70°C	$2.0\ V \le V_{CC} \le 5.5\ V$
Data Retention, Industrial	−40°C to +85°C	$2.0\ V \le V_{CC} \le 5.5\ V$
Data Retention, Military	−55°C to +125°C	$2.0\ V \le V_{CC} \le 5.5\ V$

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L7C108/109			L7C108-L/109-L			
Symbol	Parameter	Test Condition	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = −4.0 mA	2.4			2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC} +0.3	2.2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	−3.0		0.8	−3.0		0.8	V
I_{IX}	Input Leakage Current	$GND \le V_{IN} \le V_{CC}$	−10		+10	−10		+10	µA
I_{OZ}	Output Leakage Current	(Note 4)	−10		+10	−10		+10	µA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		10	20			10	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		1	3.0			0.9	mA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		500	1000			300	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7			7	pF

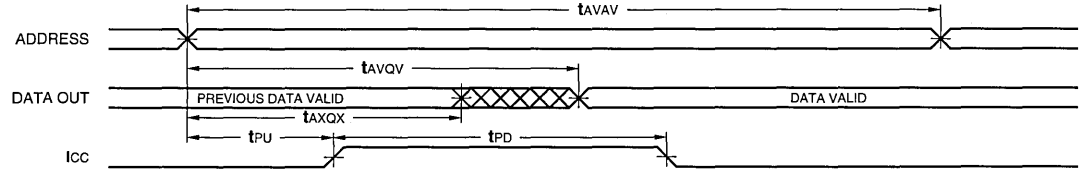
			L7C108/109-			
Symbol	Parameter	Test Condition	25	20	17	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	145	180	210	mA

SWITCHING CHARACTERISTICS *Over Operating Range*

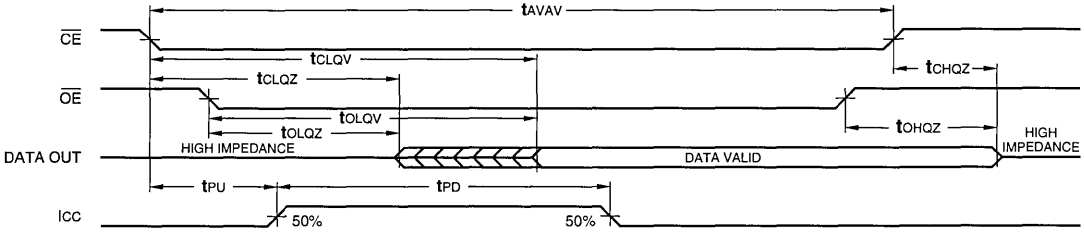
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C108/109–					
		25		20		17	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	25		20		17	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		25		20		17
t_{AXQX}	Address Change to Output Change	3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		25		20		17
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		10		8		8
t_{OLQV}	Output Enable Low to Output Valid		10		10		9
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		10		7		6
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		25		20		17
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0	

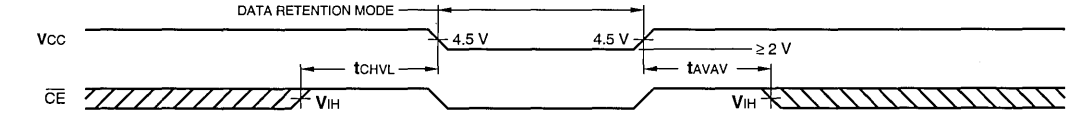
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}$/$\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

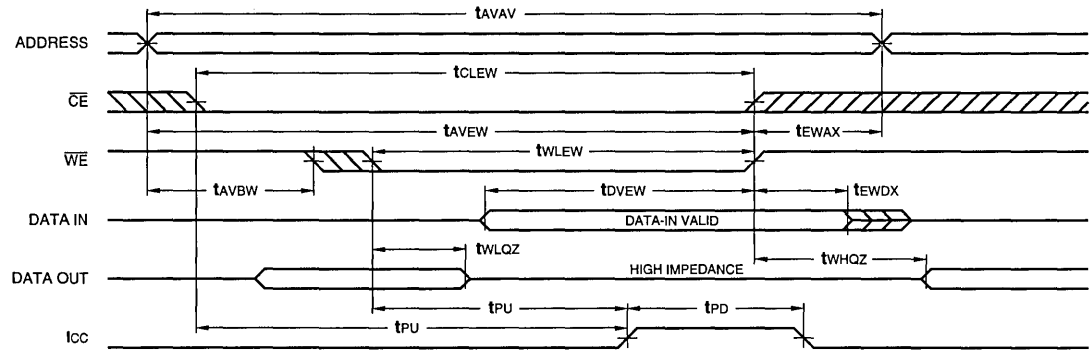


SWITCHING CHARACTERISTICS *Over Operating Range*

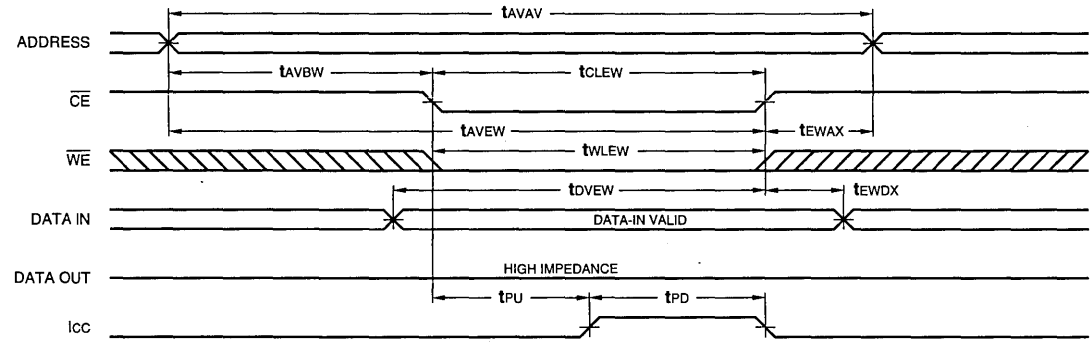
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C108/109–					
		25		20		17	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	20		20		17	
t_{CLEW}	Chip Enable Low to End of Write Cycle	15		15		13	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	15		15		13	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	15		15		13	
t_{DVEW}	Data Valid to End of Write Cycle	10		9		8	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		7		7		6

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND ≤ V_{OUT} ≤ V_{CC}. The device is disabled, i.e., $\overline{CE_1}$ = V_{CC}, CE_2 = GND.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE_1} \le V_{IL}$, $CE_2 \ge V_{IH}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE_1} \ge V_{IH}$, $CE_2 \le V_{IL}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE_1}$ = V_{CC}, CE_2 = GND. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE_1}$ must be ≥ V_{CC} – 0.2 V or CE_2 must be ≤ 0.2 V. All other inputs must meet $V_{IN} \ge V_{CC}$ – 0.2 V or $V_{IN} \le 0.2$ V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE_1}$, CE_2, and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE_1}$ low, CE_2 high).

15. All address lines are valid prior-to or coincident-with the $\overline{CE_1}$ and CE_2 transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE_1}$ and CE_2 active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE_1}$ and CE_2 going active, the output remains in a high impedance state.

18. If $\overline{CE_1}$ and CE_2 goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Rising edge of CE_2 ($\overline{CE_1}$ active) or the falling edge of $\overline{CE_1}$ (CE_2 active).

b. Falling edge of $\overline{WE}$ ($\overline{CE_1}$, CE_2 active).

c. Transition on any address line ($\overline{CE_1}$, CE_2 active).

d. Transition on any data line ($\overline{CE_1}$, CE_2, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE_1}$, CE_2, or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

7

FIGURE 1a.

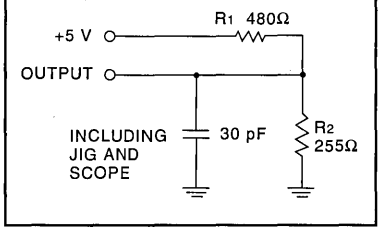


FIGURE 1b.

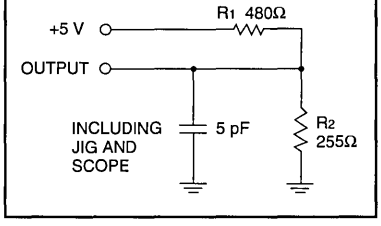
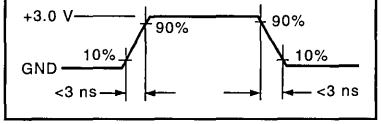
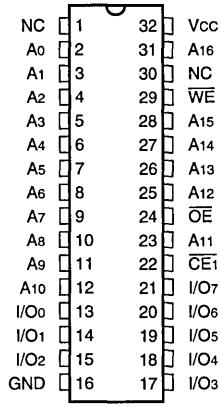


FIGURE 2.

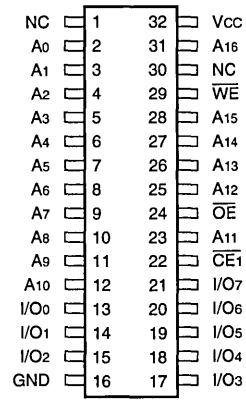


L7C108 ORDERING INFORMATION

32-pin — 0.4" wide



32-pin

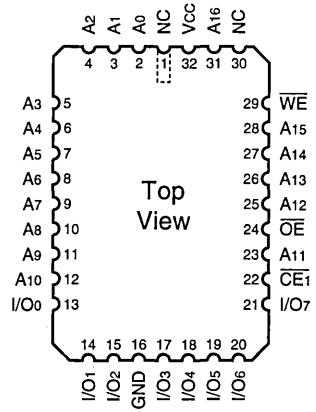


Speed	Sidebraze Hermetic DIP (D12)	Plastic SOJ (0.4" wide) (W6)
	0°C to +70°C — COMMERCIAL SCREENING	
25 ns	L7C108DC25*	L7C108WC25*
20 ns	L7C108DC20*	L7C108WC20*
17 ns	L7C108DC17*	L7C108WC17*
	–40°C to +85°C — COMMERCIAL SCREENING	
25 ns		L7C108WI25*
20 ns		L7C108WI20*
17 ns		L7C108WI17*
	–55°C to +125°C — COMMERCIAL SCREENING	
25 ns	L7C108DM25	
20 ns	L7C108DM20	
	–55°C to +125°C — MIL-STD-883 COMPLIANT	
25 ns	L7C108DMB25	
20 ns	L7C108DMB20	

***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C108WI17L)**

L7C108 ORDERING INFORMATION

32-pin

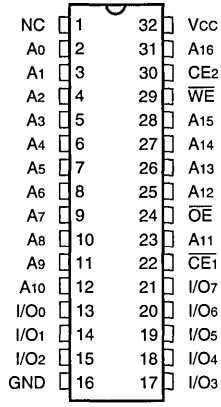


Speed	Ceramic Leadless Chip Carrier (K10)	
	0°C to +70°C — Commercial Screening	
25 ns 20 ns 17 ns	L7C108KC25* L7C108KC20* L7C108KC17*	
	–40°C to +85°C — Commercial Screening	
25 ns 20 ns 17 ns		
	–55°C to +125°C — Commercial Screening	
25 ns 20 ns	L7C108KM25 L7C108KM20	
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns 20 ns	L7C108KMB25 L7C108KMB20	

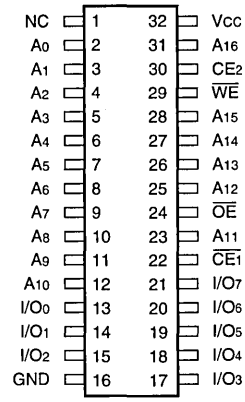
***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C108KC17L)**

L7C109 ORDERING INFORMATION

32-pin — 0.4" wide



32-pin

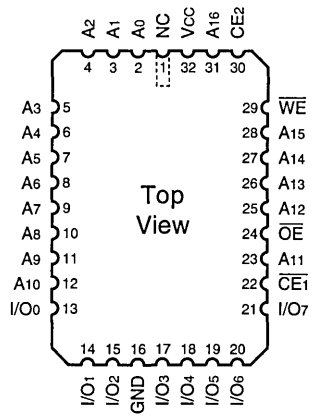


Speed	Sidebraze Hermetic DIP (D12)	Plastic SOJ (0.4" wide) (W6)
	0°C to +70°C — Commercial Screening	
25 ns	L7C109DC25*	L7C109WC25*
20 ns	L7C109DC20*	L7C109WC20*
17 ns	L7C109DC17*	L7C109WC17*
	–40°C to +85°C — Commercial Screening	
25 ns		L7C109WI25*
20 ns		L7C109WI20*
17 ns		L7C109WI17*
	–55°C to +125°C — Commercial Screening	
25 ns	L7C109DM25	
20 ns	L7C109DM20	
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns	L7C109DMB25	
20 ns	L7C109DMB20	

***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C109WI17L)**

L7C109 ORDERING INFORMATION

32-pin



Speed	Ceramic Leadless Chip Carrier (K10)	
	0°C to +70°C — Commercial Screening	
25 ns 20 ns 17 ns	L7C109KC25* L7C109KC20* L7C109KC17*	
	–40°C to +85°C — Commercial Screening	
25 ns 20 ns 17 ns		
	–55°C to +125°C — Commercial Screening	
25 ns 20 ns	L7C109KM25 L7C109KM20	
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns 20 ns	L7C109KMB25 L7C109KMB20	

***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C109KC17L)**

FEATURES

- 8K x 8 CMOS Static RAM with 8-bit Tag Comparison Logic
- High Speed Address-to-MATCH — 12 ns maximum
- High Speed Flash Clear
- High Speed Read Access Time — 12 ns maximum
- Low Power Operation
  Active: 300 mW typical at 35 ns
  Standby: 500 µW typical
- Data Retention at 2 V for Battery Backup Operation
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with IDT7174, IDT71B74, MK48H74
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Ceramic DIP
  - 28-pin Plastic SOJ
  - 32-pin Ceramic LCC

DESCRIPTION

The **L7C174** is a high-performance, low power CMOS static RAM optimized for use as the address tag comparator in high speed cache memory systems. One L7C174 can be used to map 8K cache lines into a 1 megabyte address space by comparing 20 address bits organized as 13-line address bits and 7-page address bits.

The storage circuitry is organized as 8192 words by 8 bits per word and includes an 8-bit data comparator with MATCH output. The 8-bit data is input/output on shared I/O pins and comparison is performed between 8-bit incoming data and accessed memory locations. Also provided is a high speed $\overline{\text{CLEAR}}$ control which clears all memory locations to zero when activated. This allows all address tag bits to be cleared when powering on or when flushing the cache.

This device is available in five speed grades with maximum address-to-MATCH times of 12 ns to 35 ns. Operation is from a single +5 V power supply with power consumption only being 300 mW (typical) at 35 ns. Dissipation drops to 500 µW (typical) when the memory is deselected (Enable is high).

The L7C174 consumes only 30 µW (typical) at 3 V allowing effective battery backup operation. For minimal power consumption, data may be retained in inactive storage with a supply voltage as low as 2 V.

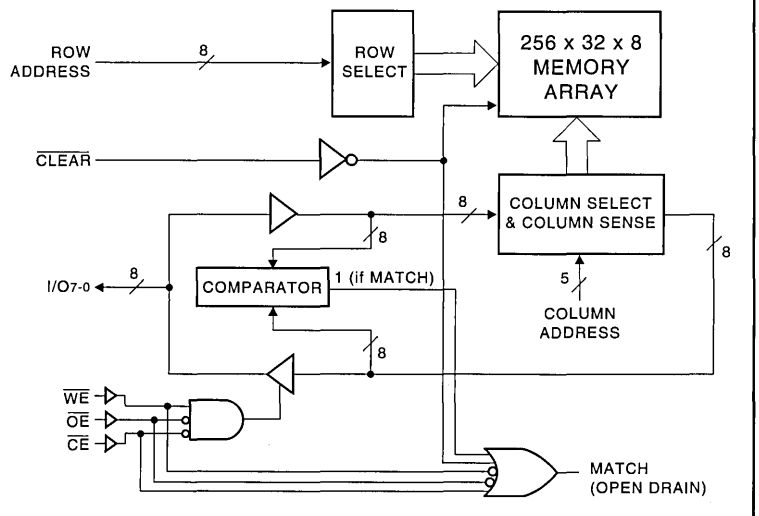
The L7C174 provides fully asynchronous (unclocked) operation with matching access and cycle times. An active low Chip Enable and Output Enable along with a three state I/O bus simplify the connection of several chips for increased storage capacity. Wide tag addresses are easily accommodated by paralleling devices and Wire-ORing the MATCH outputs. A low on the MATCH output indicates a data mismatch.

Memory locations are specified on address pins A_0 through A_{12} with functions defined in the Truth Table.

During $\overline{\text{CLEAR}}$, the state of the I/O pins remain completely defined by the $\overline{\text{WE}}$, $\overline{\text{CE}}$, and $\overline{\text{OE}}$ control inputs. Data In has the same polarity as Data Out.

Latchup and static discharge protection are provided on-chip. The L7C174 can withstand an injection current of up to 200 mA on any pin without damage.

L7C174 Block Diagram



Truth Table

$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{CLEAR}$	MATCH	I/O	FUNCTION
X	X	X	L	H	—	Reset all bits to low
X	H	X	H	H	High-Z	Deselect chip
H	L	H	H	L	D_{IN}	No MATCH
H	L	H	H	H	D_{IN}	MATCH
H	L	L	H	H	D_{OUT}	Read
L	L	X	H	H	D_{IN}	Write

X = Don't Care; L = V_{IL}; H = V_{IH}

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Industrial	−40°C to +85°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	−55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Industrial	−40°C to +85°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	−55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L7C174			
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage (Note 11)	V_{CC} = 4.5 V, I_{OH} = −4.0 mA (all except MATCH pin)	2.4			V
V_{OL}	Output Low Voltage (Note 11)	I_{OL} = 8.0 mA (all except MATCH pin)			0.4	V
		I_{OL} = 18.0 mA (MATCH pin)			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	−3.0		0.8	V
I_{IX}	Input Leakage Current	Ground ≤ V_{IN} ≤ V_{CC}	−10		+10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}, $\overline{OE}$ = V_{CC} (except MATCH pin)	−10		+10	µA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		100	500	µA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		10	200	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

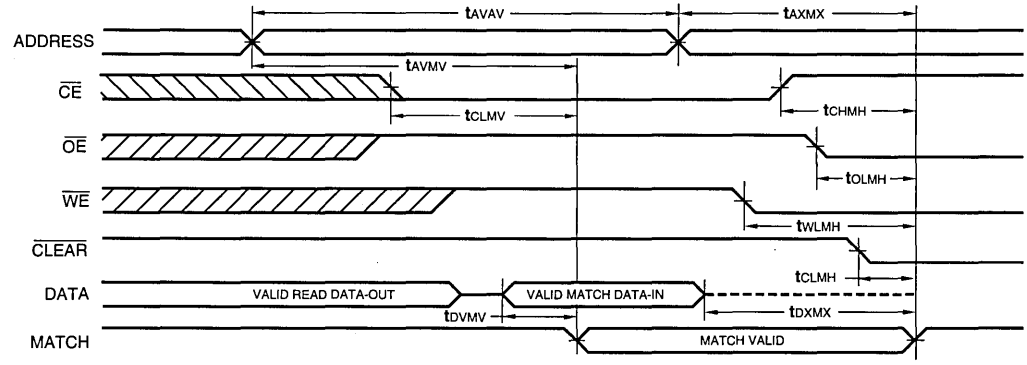
			L7C174-					
Symbol	Parameter	Test Condition	35	25	20	15	12	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	90	115	140	165	195	mA

SWITCHING CHARACTERISTICS *Over Operating Range*

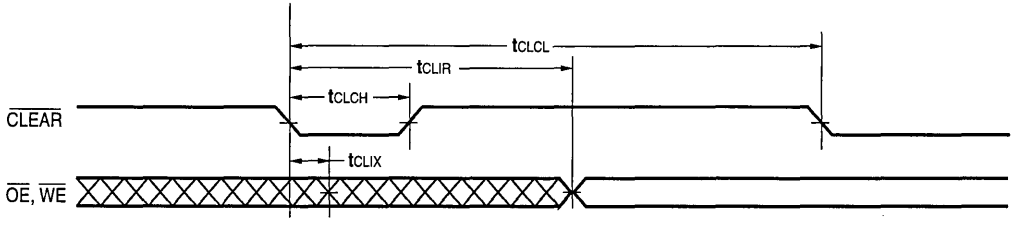
MATCH AND $\overline{\text{CLEAR}}$ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C174–									
		35		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	MATCH Cycle Time	35		25		20		15		12	
t_{AVMV}	Address Valid to MATCH Valid		30		22		20		15		12
t_{AXMX}	Address Change to MATCH Change	3		3		3		3		3	
t_{CLMV}	Chip Enable Low to MATCH Valid		20		15		10		10		8
t_{CHMH}	Chip Enable High to MATCH High	3		3		3		3		3	
t_{OLMH}	Output Enable Low to MATCH High	3		3		3		3		3	
t_{WLMH}	Write Enable Low to MATCH High	3		3		3		3		3	
t_{CLMH}	$\overline{\text{CLEAR}}$ Low to MATCH High	0	25	0	20	0	15	0	12	0	10
t_{DVMV}	Data Valid to MATCH Valid		20		15		15		13		10
t_{DXMX}	Data Change to MATCH Change	0		0		0		0		0	
t_{CLCL}	$\overline{\text{CLEAR}}$ Cycle Time	65		55		45		35		30	
t_{CLCH}	$\overline{\text{CLEAR}}$ Pulse Width	20		15		15		12		12	
t_{CLIX}	$\overline{\text{CLEAR}}$ Low to Inputs Don't Care	0		0		0		0		0	
t_{CLIR}	$\overline{\text{CLEAR}}$ Low to Inputs Recognized		70		60		50		50		45

MATCH CYCLE



$\overline{\text{CLEAR}}$ CYCLE

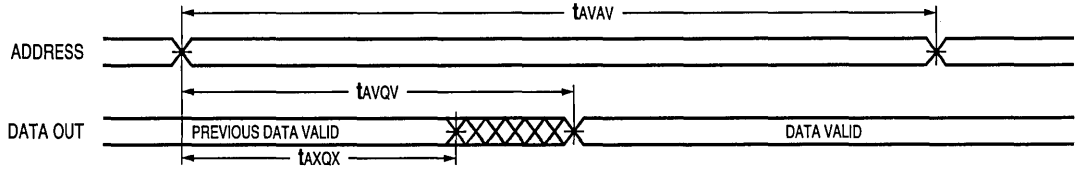


SWITCHING CHARACTERISTICS *Over Operating Range*

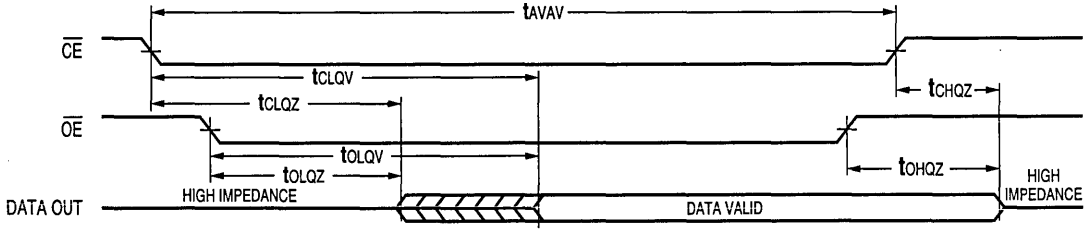
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C174–									
		35		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	35		25		20		15		12	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		35		25		20		15		12
t_{AXQX}	Address Change to Output Change	3		3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		15		12		10		8		8
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		15		10		8		8		5
t_{OLQV}	Output Enable Low to Output Valid		15		12		10		8		6
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		12		10		8		5		5
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0		0	

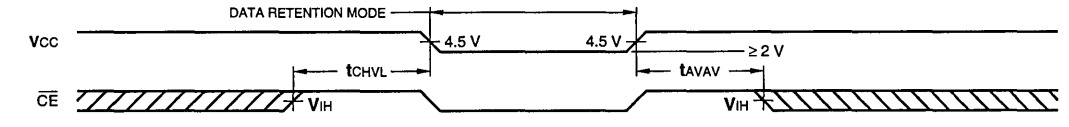
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}$/$\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

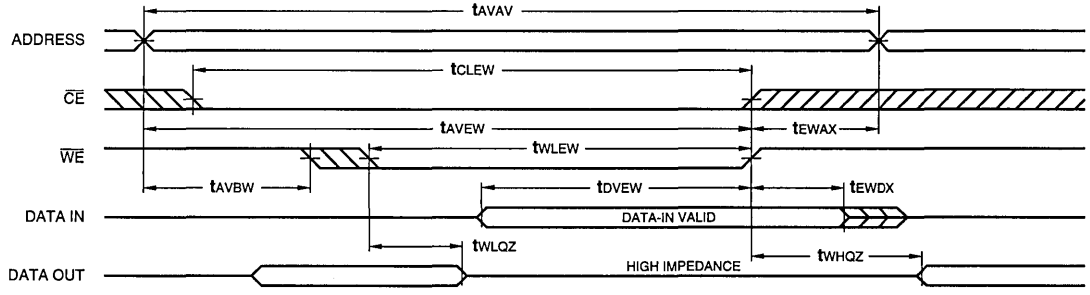


SWITCHING CHARACTERISTICS *Over Operating Range*

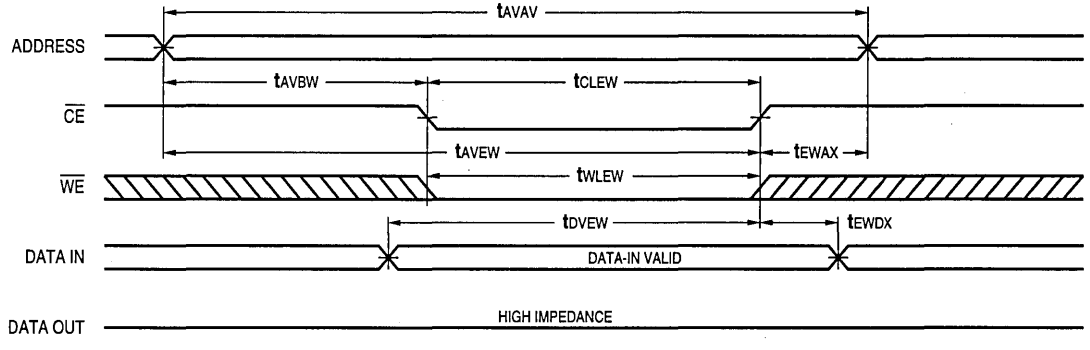
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C174–									
		35		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	25		20		20		15		12	
t_{CLEW}	Chip Enable Low to End of Write Cycle	25		15		15		12		10	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	25		15		15		12		10	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	20		15		15		12		10	
t_{DVEW}	Data Valid to End of Write Cycle	15		10		10		7		6	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		10		7		7		5		4

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.2$ V. All other inputs must meet $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Figs. 1a and 1c), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}$ going active, the output remains in a high impedance state.

18. If $\overline{CE}$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

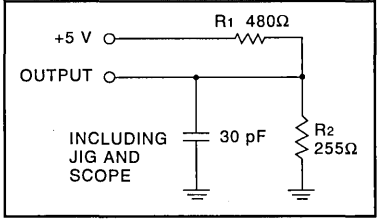


FIGURE 1b.

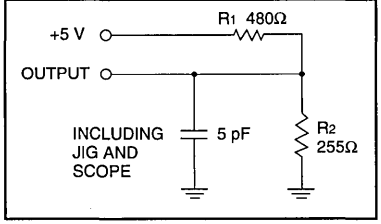


FIGURE 1c.

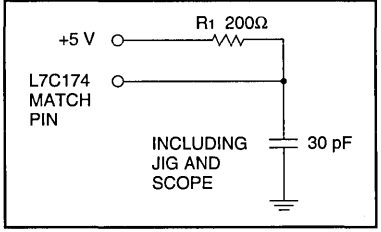
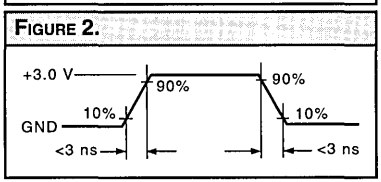
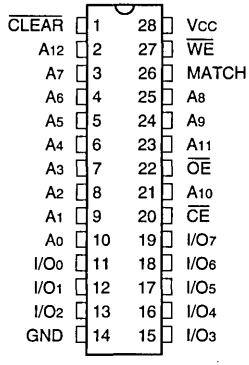


FIGURE 2.

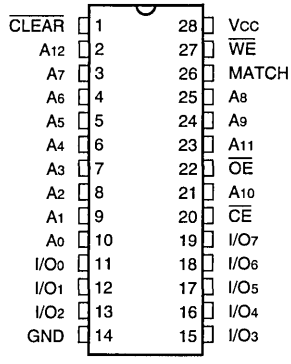


ORDERING INFORMATION

28-pin — 0.3" wide



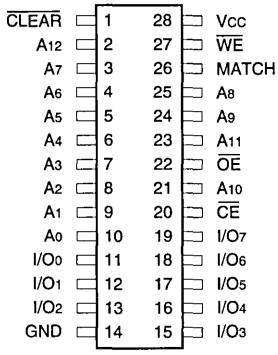
28-pin — 0.6" wide



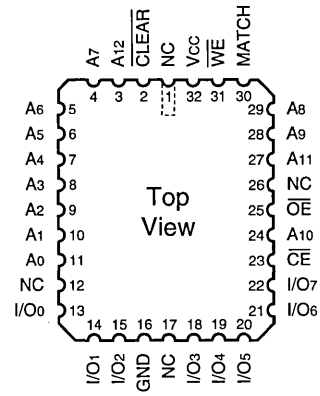
Speed	Plastic DIP (P10)	Ceramic DIP (C5)	Plastic DIP (P9)	Ceramic DIP (C6)
	0°C to +70°C — Commercial Screening			
25 ns	L7C174PC25	—	L7C174NC25	—
20 ns	L7C174PC20	L7C174CC20	L7C174NC20	L7C174IC20
15 ns	L7C174PC15	L7C174CC15	L7C174NC15	L7C174IC15
12 ns	L7C174PC12	L7C174CC12	L7C174NC12	L7C174IC12
	–40°C to +85°C — Commercial Screening			
25 ns	L7C174PI25		L7C174NI25	
20 ns	L7C174PI20		L7C174NI20	
15 ns	L7C174PI15		L7C174NI15	
12 ns	L7C174PI12		L7C174NI12	
	–55°C to +125°C — Commercial Screening			
25 ns		L7C174CM25		L7C174IM25
20 ns		L7C174CM20		L7C174IM20
15 ns		L7C174CM15		L7C174IM15
	–55°C to +125°C — MIL-STD-883 Compliant			
25 ns		L7C174CMB25		L7C174IMB25
20 ns		L7C174CMB20		L7C174IMB20
15 ns		L7C174CMB15		L7C174IMB15

ORDERING INFORMATION

28-pin — 0.3" wide



32-pin



Speed	Plastic SOJ (W2)	Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — Commercial Screening	
35 ns	L7C174WC35	—
25 ns	L7C174WC25	—
20 ns	L7C174WC20	L7C174KC20
15 ns	L7C174WC15	L7C174KC15
12 ns	L7C174WC12	L7C174KC12
	–40°C to +85°C — Commercial Screening	
35 ns	L7C174WI35	
25 ns	L7C174WI25	
20 ns	L7C174WI20	
15 ns	L7C174WI15	
12 ns	L7C174WI12	
	–55°C to +125°C — Commercial Screening	
25 ns		L7C174KM25
20 ns		L7C174KM20
15 ns		L7C174KM15
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns		L7C174KMB25
20 ns		L7C174KMB20
15 ns		L7C174KMB15

FIFO Products

L8C201/202/203/204
512/1K/2K/4K x 9-bit Asynchronous FIFO

FEATURES

- First-In/First-Out (FIFO) using Dual-Port Memory
- Advanced CMOS Technology
- High Speed — to 10 ns Access Time
- Asynchronous and Simultaneous Read and Write
- Fully Expandable by both Word Depth and/or Bit Width
- Empty and Full Warning Flags
- Half-Full Flag Capability
- Auto Retransmit Capability
- Plug Compatible with IDT720x, Cypress CY7C4x, and Samsung KM75C0x
- DECC SMD No.
  5962-89536 — L8C202
- Package Styles Available:
  - 28-pin Plastic DIP
  - 32-pin Plastic LCC

DESCRIPTION

The **L8C201, L8C202, L8C203,** and **L8C204** are dual-port First-In/First-Out (FIFO) memories. The FIFO memory products are organized as:

L8C201 — 512 x 9-bit
L8C202 — 1024 x 9-bit
L8C203 — 2048 x 9-bit
L8C204 — 4096 x 9-bit

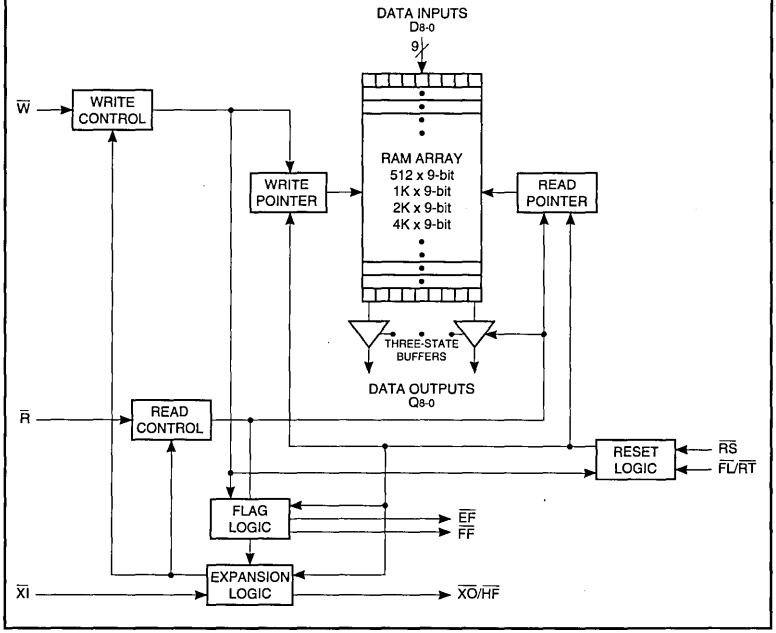
Each device utilizes a special algorithm that loads and empties data on a first-in/first-out basis. Full and Empty flags are provided to prevent data overflow and underflow. Three additional pins are also provided to allow for unlimited expansion in both word size and depth. Depth Expansion does not result in a flow-through penalty. Multiple devices are connected with the data and control signals in parallel. The active device is determined by the Expansion In ($\overline{XI}$) and Expansion Out ($\overline{XO}$) signals which are daisy chained from device to device.

The read and write operations are internally sequential through the use of ring pointers. No address information is required to load and unload data. The write operation occurs when the Write ($\overline{W}$) signal is LOW. Read occurs when Read ($\overline{R}$) goes LOW. The nine data outputs go to the high impedance state when R is HIGH. Retransmit ($\overline{RT}$) capability allows for reset of the read pointer when $\overline{RT}$ is pulsed LOW, allowing for retransmission of data from the beginning. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must both be HIGH during a retransmit cycle, and then $\overline{R}$ is used to access the data. A Half-Full ($\overline{HF}$) output flag is available in the single device and width expansion modes. In the depth expansion configuration, this pin provides the Expansion Out ($\overline{XO}$) information which is used to tell the next FIFO that it will be activated.

These FIFOs are designed to have the fastest data access possible. Even in lower cycle time applications, faster access time can eliminate timing bottlenecks as well as leave enough margin to allow the use of the devices without external bus drivers.

The FIFOs are designed for those applications requiring asychronous and simultaneous read/writes in multiprocessing and rate buffer applications.

L8C201/202/203/204 Block Diagram



8

SIGNAL DEFINITIONS

Inputs

$\overline{RS}$ — Reset

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the HIGH state during the window shown (i.e., tWHSH before the rising edge of $\overline{RS}$) and should not change until tSHWL after the rising edge of $\overline{RS}$. Hall-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).

$\overline{W}$ — Write Enable

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data setup and hold time must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go HIGH after tRHFH, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

$\overline{R}$ — Read Enable

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operation. After Read Enable ($\overline{R}$) goes HIGH, the Data Outputs (D8-0) will return to a high impedance condition until the next read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operating has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after tWHEH and a valid read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO.

$\overline{FL}/\overline{RT}$ — First Load/Retransmit

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The FIFOs can be made to retransmit data when the Retransmit Enable control ($\overline{RT}$) input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the HIGH state during retransmit. This feature is useful when less than the full memory has been written between resets. Retransmit will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers. The retransmit feature is not compatible with the Depth Expansion Mode.

$\overline{XI}$ — Expansion In

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

D8-0 — Data Input

Data input signals for 9-bit wide data. Data has setup and hold time requirements with respect to the rising edge of $\overline{W}$.

Outputs

$\overline{FF}$ — Full Flag

The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go LOW after 512 writes for the **L8C201**, 1024 writes for the **L8C202**, 2048 writes for the **L8C203**, and 4096 writes for the **L8C204**.

$\overline{EF}$ — Empty Flag

The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

$\overline{XO}/\overline{HF}$ — Expansion Out/Half-Full Flag

This is a dual-purpose output. In the Single Device Mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one-half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then deasserted by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the daisy chain by providing a pulse to the next device when the previous device reaches the last location of memory.

Q8-0 — Data Output

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read Enable ($\overline{R}$) is in a HIGH state or the device is empty.

OPERATING MODES

Single Device Mode

A single FIFO may be used when the application requirements are for the number of words in a single device. The FIFOs are in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded. In this mode the Half-Full Flag ($\overline{HF}$), which is an active-low output, is the active function of the combination pin $\overline{XO}$/$\overline{HF}$.

Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$, and $\overline{HF}$) can be detected from any one device. Any word width can be attained by adding additional FIFOs. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. **Do not connect any output signals together.**

Depth Expansion (Daisy Chain) Mode

The FIFOs can easily be adapted to applications where the requirements are for greater than the number of words in a single device. Any depth can be attained by adding additional FIFOs. The FIFOs operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device with the last device connecting back to the first.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

Bidirectional Mode

Applications which require data buffering between two systems (each system capable of read and write operations) can be achieved by pairing FIFOs. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device when $\overline{W}$ is used; $\overline{EF}$ is monitored on the device when $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−0.5 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Active Operation, Industrial	−40°C to +85°C	$4.5\ V \le V_{CC} \le 5.5\ V$

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L8C201/202/203/204			
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = −2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = 4.5 V, I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	−0.5		0.8	V
I_{IX}	Input Leakage Current	Ground ≤ V_{IN} ≤ V_{CC}	−1		+1	µA
I_{OZ}	Output Leakage Current	$\overline{R} \ge V_{IH}$, GND ≤ V_{OUT} ≤ V_{CC}	−10		+10	µA
I_{CC2}	V_{CC} Current, TTL Inactive	All Inputs = V_{IH} MIN (Note 6)			15	mA
I_{CC3}	V_{CC} Current, CMOS Standby	All Inputs = V_{CC} (Note 12)			5	mA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 4.5 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 9)			7	pF

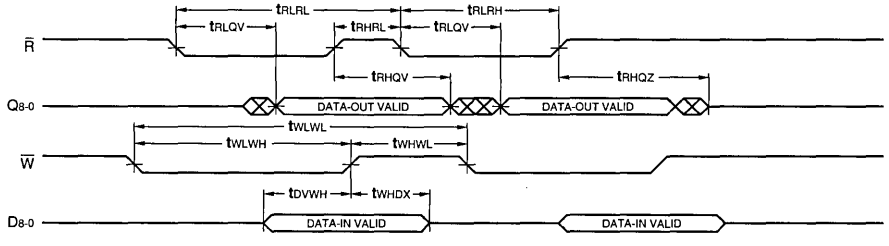
			L8C201/202/203/204-				
Symbol	Parameter	Test Condition	25	15	12	10	Unit
I_{CC1}	V_{CC} Current, Active	(Note 5)	100	120	150	180	mA

SWITCHING CHARACTERISTICS *Over Operating Range*

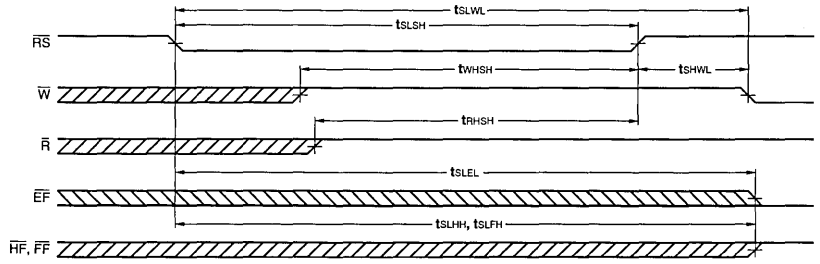
ASYNCHRONOUS AND RESET TIMING *(ns)*

		L8C201/202/203/204–							
		25		15		12		10	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{RLRL}	Read Cycle Time (MHz)	35		25		20		15	
t_{RLQV}	Read Low to Output Valid (Access Time)		25		15		12		10
t_{RHRL}	Read High to Read Low (Notes 8, 9)	10		10		8		5	
t_{RLRH}	Read Low to End of Read Cycle (Notes 8, 9)	25		15		12		10	
t_{RHQV}	Read High to Output Valid	5		5		5		5	
t_{RHQZ}	Read High to Output High Z (Note 14)		20		15		15		15
t_{WLWL}	Write Cycle Time (Note 9)	35		25		20		15	
t_{WLWH}	Write Low to Write High (Notes 8, 9)	25		15		12		10	
t_{WHWL}	Write High to End of Write Cycle (Notes 8, 9)	10		10		8		5	
t_{DVWH}	Data Valid to Write High (Notes 8, 9)	15		10		8		8	
t_{WHDX}	Write High to Data Change (Notes 8, 9)	0		0		0		0	
t_{SLSH}	Reset Cycle Time (Notes 9, 10)	25		15		12		10	
t_{SLWL}	Reset Low to Write Low (Notes 9, 10)	35		25		20		15	
t_{WHSH}	Write High to Reset High (Notes 9, 10)	25		15		12		10	
t_{RHSH}	Read High to Reset High (Notes 9, 10)	25		15		12		10	
t_{SHWL}	Reset High to Write Low (Notes 9, 10)	10		10		8		5	
t_{SLEL}	Reset Low to Empty Flag Low		25		15		12		10
t_{SLHH}	Reset Low to Half-Full Flag High		25		15		12		10
t_{SLFH}	Reset Low to Full Flag High		25		15		12		10

ASYNCHRONOUS READ AND WRITE OPERATION



RESET TIMING



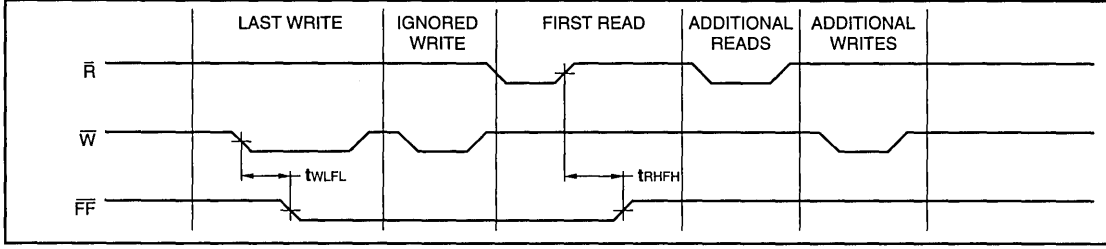
8

SWITCHING CHARACTERISTICS *Over Operating Range*

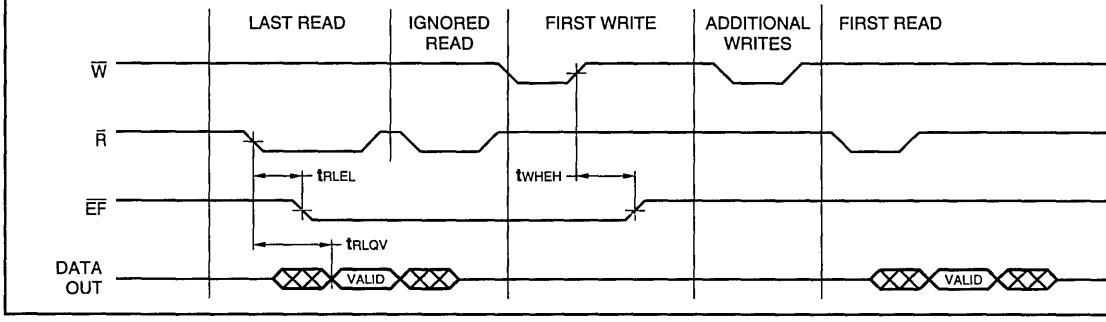
FULL/EMPTY FLAG AND RETRANSMIT TIMING *(ns)*

		L8C201/202/203/204–							
		25		15		12		10	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{RLQV}	Read Low to Output Valid (Access Time)		25		15		12		10
t_{RLEL}	Read Low to Empty Flag Low		25		15		12		10
t_{RHFH}	Read High to Full Flag High		25		15		12		10
t_{WHEH}	Write High to Empty Flag High		25		15		12		10
t_{WLFL}	Write Low to Full Flag Low		25		15		12		10
t_{TLAL}	Retransmit Cycle Time	35		25		20		15	
t_{TLTH}	Retransmit Low to End of Retransmit Cycle (Notes 8, 9, 10)	25		15		12		10	
t_{AHTH}	Read/Write High to Retransmit High (Notes 8, 9, 10)	25		15		12		10	
t_{THAL}	Retransmit High to Read/Write Low (Note 9)	10		10		8		5	

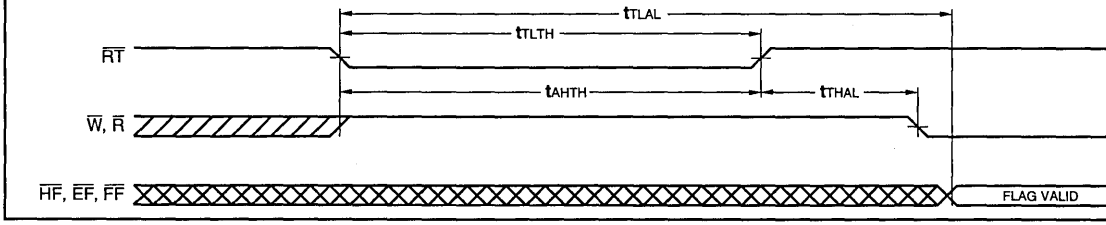
FULL FLAG FROM LAST WRITE TO FIRST READ



EMPTY FLAG FROM LAST READ TO FIRST WRITE



RETRANSMIT

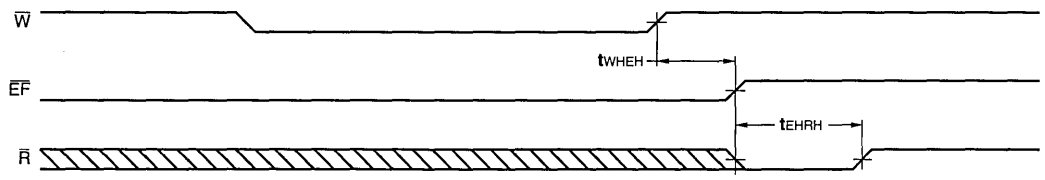


SWITCHING CHARACTERISTICS *Over Operating Range*

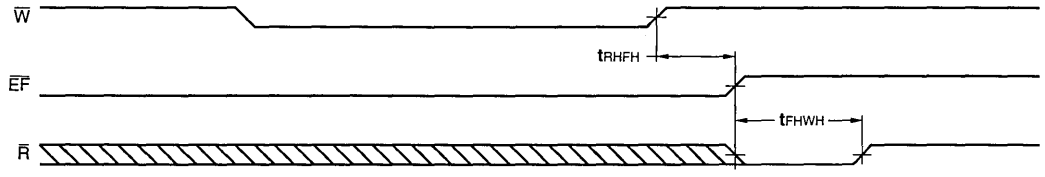
FULL/HALF-FULL/EMPTY FLAG TIMING *(ns)*

		L8C201/202/203/204–							
		25		15		12		10	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{RHFH}	Read High to Full Flag High		25		15		12		10
t_{EHRH}	Read Pulse Width After Empty Flag High	25		15		12		10	
t_{RHHH}	Read High to Half-Full Flag High		25		15		12		10
t_{WHEH}	Write High to Empty Flag High		25		15		12		10
t_{WLHL}	Write Low to Half-Full Flag Low		25		15		12		10
t_{FHWH}	Write Pulse Width After Full Flag High (Note 9)	25		15		12		10	

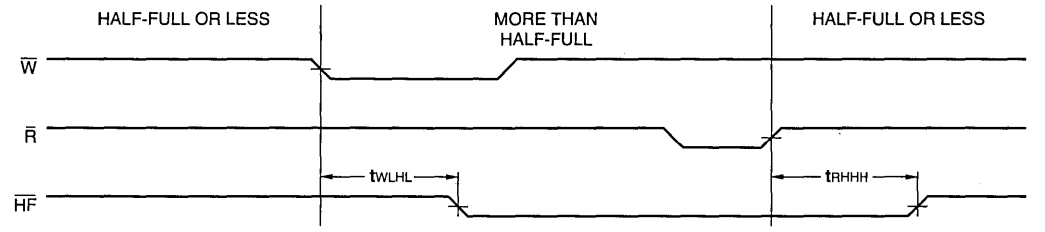
EMPTY FLAG TIMING



FULL FLAG TIMING



HALF-FULL FLAG TIMING



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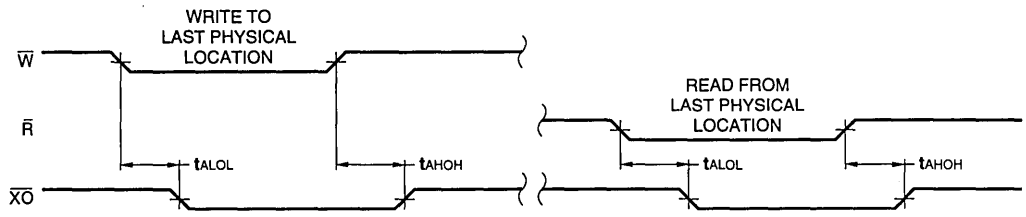
SWITCHING CHARACTERISTICS *Over Operating Range*

EXPANSION TIMING *(ns)*

		L8C201/202/203/204–							
		25		15		12		10	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{ALOL}	Read/Write to Expansion Out Low (Note 11)		25		15		12		12
t_{AHOH}	Read/Write to Expansion Out High (Note 11)		25		15		12		12
t_{XLXH}	Expansion In Pulse Width (Notes 9, 11)	25		15		12		10	
t_{XHXL}	Expansion In High to Expansion In Low (Notes 9, 11)	10		10		10		10	
t_{ALXL}	Read/Write Low to Expansion In Low (Notes 9, 11)	15		12		8		8	

EXPANSION OUT



EXPANSION IN

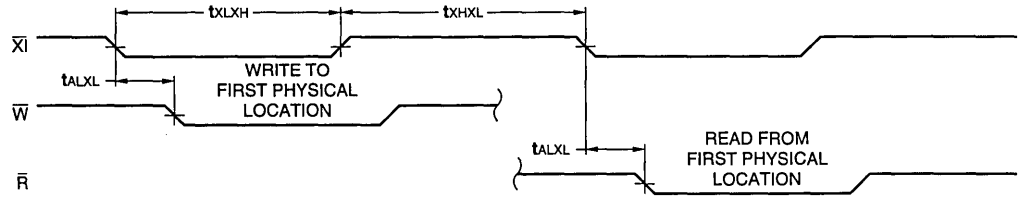
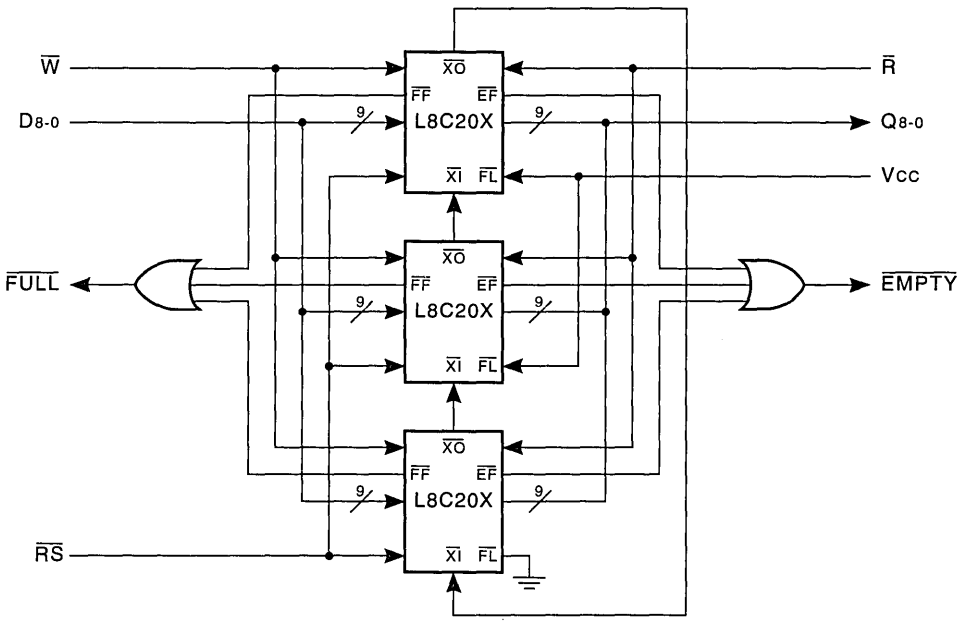


FIGURE 1. FIFO MEMORY (DEPTH EXPANSION) BLOCK DIAGRAM



8

TABLE 1. RESET AND RETRANSMIT *(SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE)*

	INPUTS			INTERNAL STATUS		OUTPUTS		
MODE	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment	Increment	X	X	X

TABLE 2. RESET AND FIRST LOAD TRUTH TABLE *(DEPTH EXPANSION/COMPOUND EXPANSION MODE)*

	INPUTS			INTERNAL STATUS		OUTPUTS	
MODE	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Others	0	1	(1)	Location Zero Disabled	Location Zero Disabled	0	1
Read/Write	1	(2)	(1)	X	X	X	X

(1) See Figure 1 (Depth Expansion Block Diagram)
(2) Unchanged

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as–3 V subject only to power dissipation and bond wire fusing constraints.

4. "Typical" supply current values are not shown but may be approximated. At a V_{CC} of +5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

5. Tested with outputs open and data inputs changing at the specified read and write cycle rate. The device is neither full or empty for the test.

6. Tested with outputs open in the worst static input control signal combination (i.e., $\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{FL}$, and $\overline{RS}$).

7. These parameters are guaranteed but not 100% tested.

8. Test conditions assume input transition times of 5 ns or less, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 2a), and input pulse levels of 0 to 3.0 V (Fig. 3).

9. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{RLRH} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

10. When cascading devices, the reset pulse width must be increased to equal t_{SLSH} + t_{SLHH}.

11. It is not recommended that Logic Devices and other vendor parts be cascaded together. The parts are designed to be pin-for-pin compatible but temperature and voltage compensation may vary from vendor to vendor. Logic Devices can only guarantee the cascading of Logic Devices parts to other Logic Devices parts.

12. Tested with output open and $\overline{RS}$ = $\overline{FL}$ = $\overline{XI}$ = $\overline{R}$ = $\overline{W}$ = V_{CC}.

13. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

14. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 2b. This parameter is sampled and not 100% tested.

15. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 2a.

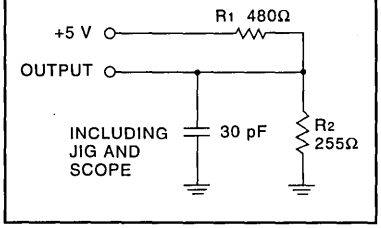


FIGURE 2b.

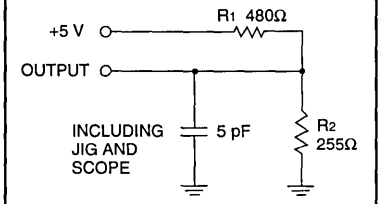
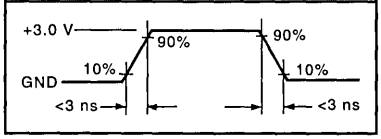
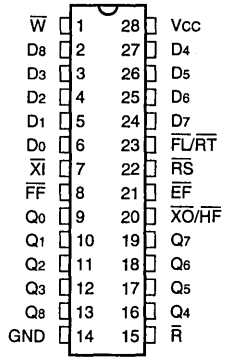


FIGURE 3.

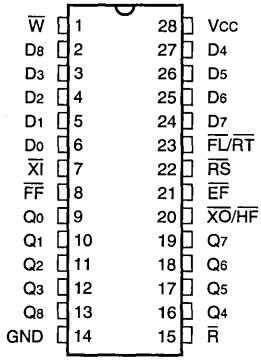


L8C201 — ORDERING INFORMATION

28-pin — 0.3" wide



28-pin — 0.6" wide

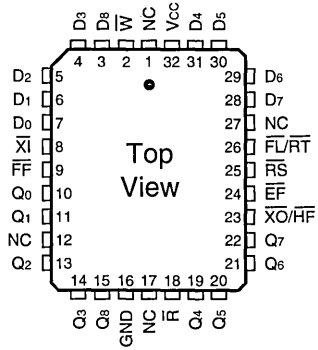


Speed	Plastic DIP (P10)	Plastic DIP (P9)
	0°C to +70°C — COMMERCIAL SCREENING	
25 ns	L8C201PC25	L8C201NC25
15 ns	L8C201PC15	L8C201NC15
12 ns	L8C201PC12	L8C201NC12
10 ns	L8C201PC10	L8C201NC10
	–40°C to +85°C — COMMERCIAL SCREENING	
25 ns	L8C201PI25	L8C201NI25
15 ns	L8C201PI15	L8C201NI15
12 ns	L8C201PI12	L8C201NI12
10 ns	L8C201PI10	L8C201NI10

8

L8C201 — ORDERING INFORMATION

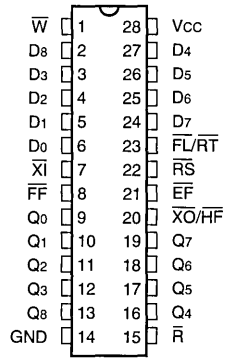
32-pin



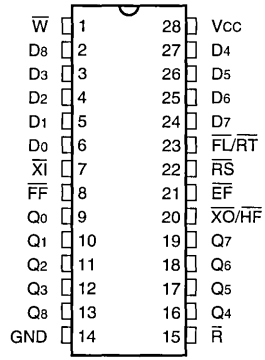
Speed	Plastic J-Lead Chip Carrier (J6)	
	0°C to +70°C — COMMERCIAL SCREENING	
25 ns	L8C201JC25	
15 ns	L8C201JC15	
12 ns	L8C201JC12	
10 ns	L8C201JC10	
	–40°C to +85°C — COMMERCIAL SCREENING	
25 ns	L8C201JI25	
15 ns	L8C201JI15	
12 ns	L8C201JI12	
10 ns	L8C201JI10	

L8C202 — ORDERING INFORMATION

28-pin — 0.3" wide



28-pin — 0.6" wide

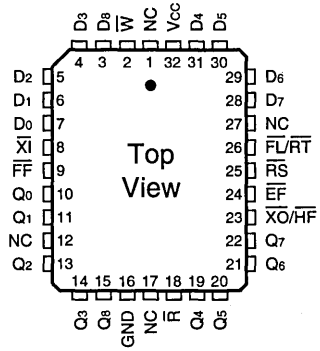


Speed	Plastic DIP (P10)	Plastic DIP (P9)
	0°C to +70°C — Commercial Screening	
25 ns	L8C202PC25	L8C202NC25
15 ns	L8C202PC15	L8C202NC15
12 ns	L8C202PC12	L8C202NC12
10 ns	L8C202PC10	L8C202NC10
	–40°C to +85°C — Commercial Screening	
25 ns	L8C202PI25	L8C202NI25
15 ns	L8C202PI15	L8C202NI15
12 ns	L8C202PI12	L8C202NI12
10 ns	L8C202PI10	L8C202NI10

8

L8C202 — ORDERING INFORMATION

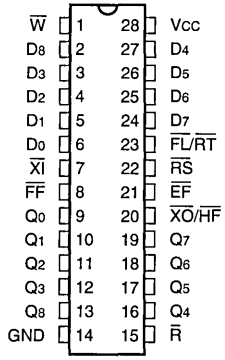
32-pin



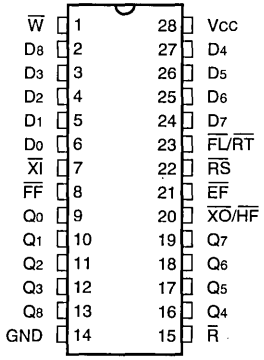
Speed	Plastic J-Lead Chip Carrier (J6)	
	0°C to +70°C — COMMERCIAL SCREENING	
25 ns	L8C202JC25	
15 ns	L8C202JC15	
12 ns	L8C202JC12	
10 ns	L8C202JC10	
	–40°C to +85°C — COMMERCIAL SCREENING	
25 ns	L8C202JI25	
15 ns	L8C202JI15	
12 ns	L8C202JI12	
10 ns	L8C202JI10	

L8C203 — ORDERING INFORMATION

28-pin — 0.3" wide



28-pin — 0.6" wide

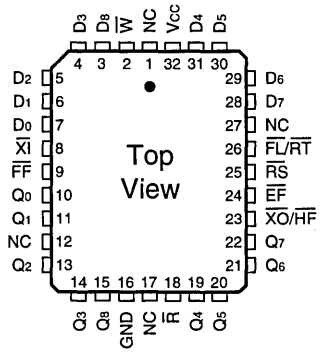


Speed	Plastic DIP (P10)	Plastic DIP (P9)
	0°C to +70°C — Commercial Screening	
25 ns	L8C203PC25	L8C203NC25
15 ns	L8C203PC15	L8C203NC15
12 ns	L8C203PC12	L8C203NC12
10 ns	L8C203PC10	L8C203NC10
	–40°C to +85°C — Commercial Screening	
25 ns	L8C203PI25	L8C203NI25
15 ns	L8C203PI15	L8C203NI15
12 ns	L8C203PI12	L8C203NI12
10 ns	L8C203PI10	L8C203NI10

8

L8C203 — ORDERING INFORMATION

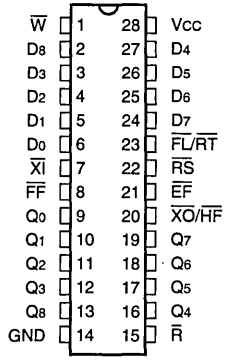
32-pin



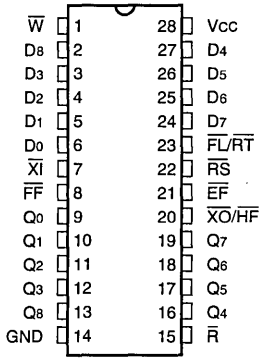
Speed	Plastic J-Lead Chip Carrier (J6)	
	0°C to +70°C — COMMERCIAL SCREENING	
25 ns	L8C203JC25	
15 ns	L8C203JC15	
12 ns	L8C203JC12	
10 ns	L8C203JC10	
	–40°C to +85°C — COMMERCIAL SCREENING	
25 ns	L8C203JI25	
15 ns	L8C203JI15	
12 ns	L8C203JI12	
10 ns	L8C203JI10	

L8C204 — ORDERING INFORMATION

28-pin — 0.3" wide



28-pin — 0.6" wide

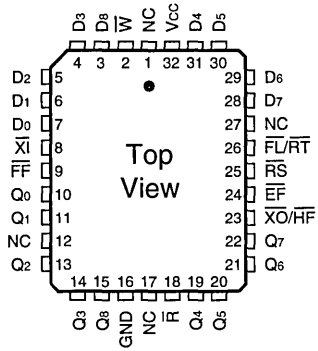


Speed	Plastic DIP (P10)	Plastic DIP (P9)
	0°C to +70°C — COMMERCIAL SCREENING	
25 ns	L8C204PC25	L8C204NC25
15 ns	L8C204PC15	L8C204NC15
12 ns	L8C204PC12	L8C204NC12
10 ns	L8C204PC10	L8C204NC10
	–40°C to +85°C — COMMERCIAL SCREENING	
25 ns	L8C204PI25	L8C204NI25
15 ns	L8C204PI15	L8C204NI15
12 ns	L8C204PI12	L8C204NI12
10 ns	L8C204PI10	L8C204NI10

8

L8C204 — ORDERING INFORMATION

32-pin



Speed	Plastic J-Lead Chip Carrier (J6)	
	0°C to +70°C — COMMERCIAL SCREENING	
25 ns	L8C204JC25	
15 ns	L8C204JC15	
12 ns	L8C204JC12	
10 ns	L8C204JC10	
	–40°C to +85°C — COMMERCIAL SCREENING	
25 ns	L8C204JI25	
15 ns	L8C204JI15	
12 ns	L8C204JI12	
10 ns	L8C204JI10	

L8C211/221/231/241

512/1K/2K/4K x 9-bit Synchronous FIFO

FEATURES

- First-In/First-Out (FIFO) using Dual-Port Memory
- Write and Read Clocks can be synchronous or asynchronous
- Advanced CMOS Technology
- High Speed — to 15 ns Cycle Time
- Empty and Full Warning Flags
- Programmable Almost-Empty and Almost-Full Warning Flags
- Plug Compatible with IDT722x1
- Package Styles Available:
  - 32-pin Plastic LCC, J-Lead

DESCRIPTION

The **L8C211, L8C221, L8C231,** and **L8C241** are synchronous dual-port First-In/First-Out (FIFO) memories. The FIFO memory products are organized as:

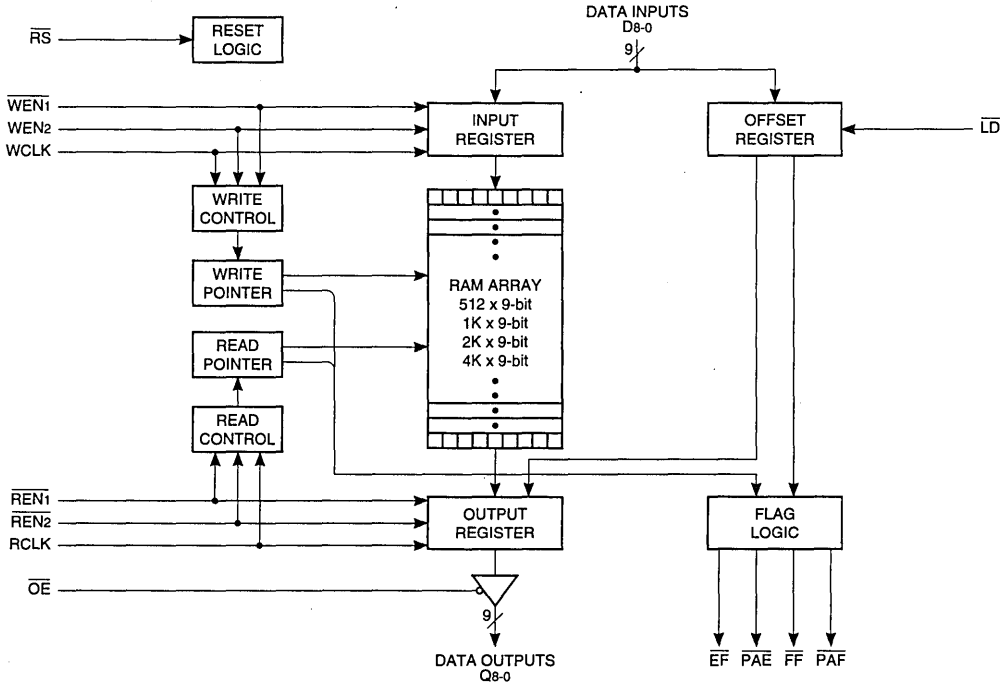
L8C211 — 512 x 9-bit
L8C221 — 1024 x 9-bit
L8C231 — 2048 x 9-bit
L8C241 — 4096 x 9-bit

Each device utilizes a special algorithm that loads and empties data on a first-in/first-out basis. Full and Empty Flags are provided to prevent data overflow and underflow. Programmable Almost Full and Almost Empty Flags are provided and may be programmed to trigger at any position in the memory array.

The read and write operations are internally sequential through the use of ring pointers. No address information is required to load and unload data. Data present at the input port is written to the FIFO if the Write Clock is pulsed when the device is enabled for writing. Data is read from the FIFO if the Read Clock is pulsed when the device is enabled for reading. Multiple FIFOs can be connected together to expand the word width and depth.

These FIFOs are designed to have the fastest data access possible. Even in lower cycle time applications, faster access time can eliminate timing bottlenecks as well as leave enough margin to allow the use of the devices without external bus drivers.

L8C211/221/231/241 BLOCK DIAGRAM



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SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clocks

WCLK — Write Clock

Data present on D8-0 is written into the FIFO on the rising edge of WCLK when the FIFO is configured for writing. The Full Flag ($\overline{FF}$) and the Programmable Almost-Full Flag ($\overline{PAF}$) are synchronized to the rising edge of WCLK.

RCLK — Read Clock

Data is read from the FIFO and presented on the output port (Q8-0) after tD has elapsed from the rising edge of RCLK if the FIFO is configured for reading and if the output port is enabled. The Empty Flag ($\overline{EF}$) and the Programmable Almost-Empty Flag ($\overline{PAE}$) are synchronized to the rising edge of RCLK. The Write and Read Clocks can be tied together and driven by the same external clock or they may be controlled by seperate external clocks.

Inputs

$\overline{RS}$ — Reset

A reset occurs when $\overline{RS}$ is set LOW. A reset is required after power-up before a write operation can take place. During reset, the internal read and write pointers are set to the first physical location, the output register is initialized to zero, the offset registers are initialized to their default values (0007H), the Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) are set LOW, the Full Flag ($\overline{FF}$) and Programmable Almost-Full Flag ($\overline{PAF}$) are set HIGH, and the WEN2/$\overline{LD}$ signal is configured.

$\overline{WEN1}$ — Write Enable 1

If the FIFO is configured to allow loading of the offset registers, $\overline{WEN1}$ is the only write enable. If $\overline{WEN1}$ is LOW, data on D8-0 is written to the FIFO on the rising edge of WCLK. If $\overline{WEN1}$ and $\overline{LD}$ are LOW, data on D8-0 is written to the programmable offset registers as defined in the WEN2/$\overline{LD}$ section. If the FIFO is configured to have two write enables, data on D8-0 is written to the FIFO on the rising edge of WCLK if $\overline{WEN1}$ is LOW and WEN2 is HIGH. When the FIFO is full, $\overline{WEN1}$ is ignored except when loading the offset registers.

WEN2/$\overline{LD}$ — Write Enable 2/Load

The function of this signal is defined during reset. If during reset WEN2/$\overline{LD}$ is HIGH, this signal functions as a second write enable (WEN2). WEN2 is used when depth expansion is needed (see Depth Expansion Mode Section). If during reset WEN2/$\overline{LD}$ is LOW, this signal functions as an offset register load/read control. When WEN2/$\overline{LD}$ is configured to be a write enable, data on D8-0 is written to the FIFO on the rising edge of WCLK if $\overline{WEN1}$ is LOW and WEN2 is HIGH. When the FIFO is full, WEN2 is ignored.

FIGURE 1. OFFSET REGISTERS

L8C211 OFFSET REGISTERS									
	8	7	6	5	4	3	2	1	0
PAE LSB	X	E7	E6	E5	E4	E3	E2	E1	E0
PAE MSB	X	X	X	X	X	X	X	X	E8
PAF LSB	X	F7	F6	F5	F4	F3	F2	F1	F0
PAF MSB	X	X	X	X	X	X	X	X	F8

L8C221 OFFSET REGISTERS									
	8	7	6	5	4	3	2	1	0
PAE LSB	X	E7	E6	E5	E4	E3	E2	E1	E0
PAE MSB	X	X	X	X	X	X	X	E9	E8
PAF LSB	X	F7	F6	F5	F4	F3	F2	F1	F0
PAF MSB	X	X	X	X	X	X	X	F9	F8

L8C231 OFFSET REGISTERS									
	8	7	6	5	4	3	2	1	0
PAE LSB	X	E7	E6	E5	E4	E3	E2	E1	E0
PAE MSB	X	X	X	X	X	X	E10	E9	E8
PAF LSB	X	F7	F6	F5	F4	F3	F2	F1	F0
PAF MSB	X	X	X	X	X	X	F10	F9	F8

L8C241 OFFSET REGISTERS									
	8	7	6	5	4	3	2	1	0
PAE LSB	X	E7	E6	E5	E4	E3	E2	E1	E0
PAE MSB	X	X	X	X	X	E11	E10	E9	E8
PAF LSB	X	F7	F6	F5	F4	F3	F2	F1	F0
PAF MSB	X	X	X	X	X	F11	F10	F9	F8

E0/F0 are the least significant bits.
X = Don't Care.

When WEN2/$\overline{LD}$ is configured to be an offset register load/read control, it is possible to write to or read from the offset registers. The values stored in the offset registers determine how the Programmable Almost-Empty ($\overline{PAE}$) and Programmable Almost-Full ($\overline{PAF}$) Flags operate (see $\overline{PAE}$ and $\overline{PAF}$ sections). There are four 9-bit offset registers. Two are used to control the Programmable Almost-Empty Flag and two are used to control the Programmable Almost-Full Flag (see Figure 1). Data on D8-0 is written to an offset register on the rising edge of WCLK if $\overline{LD}$ and $\overline{WEN1}$ are LOW. After reset, data is written to the offset registers in the following order: PAE LSB, PAE MSB, PAF LSB, PAF MSB. After the PAF MSB register has been loaded, the sequence repeats starting with the PAE LSB register. If register loading is stopped, the next register in sequence will be loaded when the next register write occurs. If $\overline{LD}$, $\overline{REN1}$, and $\overline{REN2}$ are LOW, data is read from an offset register and presented on Q8-0 (if the output port is enabled) after t_D has elapsed from the rising edge of RCLK. The offset registers are read in the same order they are written to. It is not possible to read from and write to the offset registers at the same time.

$\overline{REN1}$, $\overline{REN2}$ — Read Enables 1 and 2

Data is read from the FIFO and presented on Q8-0 after t_D has elapsed from the rising edge of RCLK if $\overline{REN1}$ and $\overline{REN2}$ are LOW and if the output port is enabled. If either Read Enable goes HIGH, the last value loaded in the output register will remain unchanged. The Read Enable signals are ignored when the FIFO is empty.

D8-0 — Data Input

D8-0 is the 9-bit registered data input port.

$\overline{OE}$ — Output Enable

When $\overline{OE}$ is LOW, the output port (Q8-0) is enabled for output. When $\overline{OE}$ is HIGH, Q8-0 is placed in a high-impedance state. The flag outputs are not affected by $\overline{OE}$.

Outputs

Q8-0 — Data Output

Q8-0 is the 9-bit registered data output port.

$\overline{FF}$ — Full Flag

The Full Flag goes LOW when the FIFO is full of data. When $\overline{FF}$ is LOW, the FIFO can not be written to. The Full Flag is synchronized to the rising edge of WCLK.

$\overline{EF}$ — Empty Flag

The Empty Flag goes LOW when the read pointer is equal to the write pointer, indicating that the FIFO is empty. When $\overline{EF}$ is LOW, read operations can not be performed. The Empty Flag is synchronized to the rising edge of RCLK.

$\overline{PAF}$ — Programmable Almost-Full Flag

$\overline{PAF}$ goes LOW when the write pointer is (Full – N) locations ahead of the read pointer. N is the value stored in the $\overline{PAF}$ offset register and has a default value of 7. $\overline{PAF}$ is synchronized to the rising edge of WCLK.

$\overline{PAE}$ — Programmable Almost-Empty Flag

$\overline{PAE}$ goes HIGH when the write pointer is (N + 1) locations ahead of the read pointer. N is the value stored in the $\overline{PAE}$ offset register and has a default value of 7. $\overline{PAE}$ is synchronized to the rising edge of RCLK.

OPERATING MODES

Single Device Mode

A single FIFO may be used when the application requirements are for the number of words in a single device.

Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Any word width can be attained by adding the appropriate number of FIFOs. Status flags can be monitored from any one of the devices.

Depth Expansion Mode

The FIFOs can easily be adapted to applications where the requirements are for greater than the number of words in a single device. If the FIFOs are configured to use WEN2 and external logic is used to direct the flow of data into the cascaded FIFOs, depth expansion can be accomplished.

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–55°C to +125°C
Operating ambient temperature	0°C to +70°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to +7.0 V
Signal applied to high impedance output	–0.5 V to +7.0 V
Output current into low outputs	50 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Active Operation, Industrial	–40°C to +85°C	$4.5\ V \le V_{CC} \le 5.5\ V$

Electrical Characteristics *Over Operating Conditions*

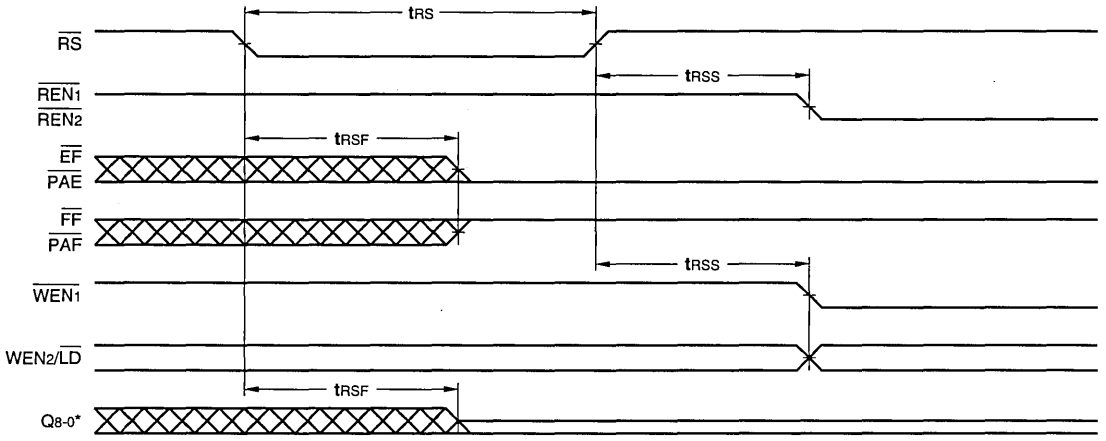
Symbol	Parameter	Test Condition	L8C211/221/231/241 Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = 4.5 V, I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IX}	Input Leakage Current	Ground ≤ V_{IN} ≤ V_{CC}	–1		+1	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}	–10		+10	µA
I_{CC1}	V_{CC} Current, Active				90	mA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 4.5 V			10	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz			10	pF

SWITCHING CHARACTERISTICS *Over Operating Range*

RESET TIMING *Notes 3, 4, 5 (ns)*

		L8C211/221/231/241–							
		50		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{RS}	Reset Pulse Width	50		25		20		15	
t_{RSS}	Reset Setup Time	50		25		20		15	
t_{RSF}	Reset to Flag and Output Valid		50		25		20		15

RESET TIMING



*after reset, Q_{8-0} will be LOW if $\overline{OE}$ = 0 and in HIGH IMPEDANCE if $\overline{OE}$ = 1.

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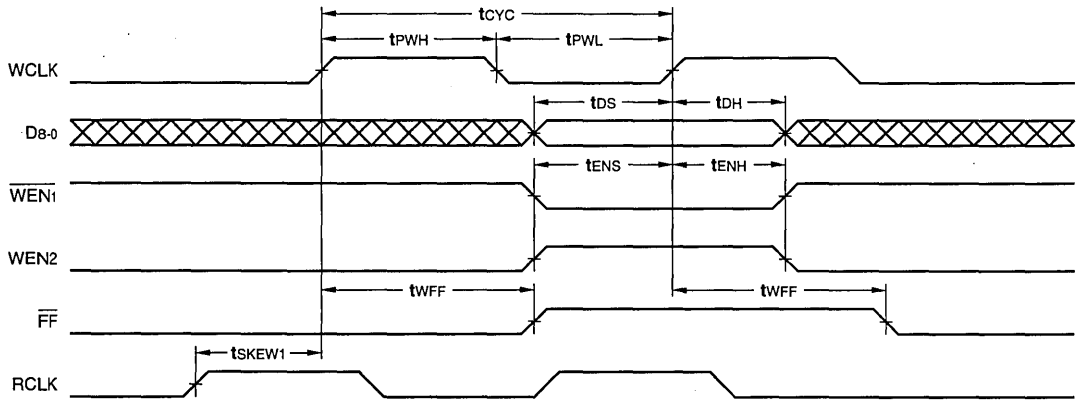
SWITCHING CHARACTERISTICS *Over Operating Range*

WRITE CYCLE TIMING *Notes 3, 4 (ns)*

		L8C211/221/231/241–							
		50		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20		15	
t_{PWH}	Clock Pulse Width HIGH	20		10		8		6	
t_{PWL}	Clock Pulse Width LOW	20		10		8		6	
t_{DS}	Data Setup Time	10		6		5		4	
t_{DH}	Data Hold Time	1		1		1		1	
t_{ENS}	Enable Setup Time	10		6		5		4	
t_{ENH}	Enable Hold Time	1		1		1		1	
t_{WFF}	Write Clock to Full Flag		25		15		12		10
t_{SKEW1}	Skew Time Between Read and Write Clocks for Empty and Full Flags (Note 6)	15		10		8		6	

WRITE CYCLE TIMING

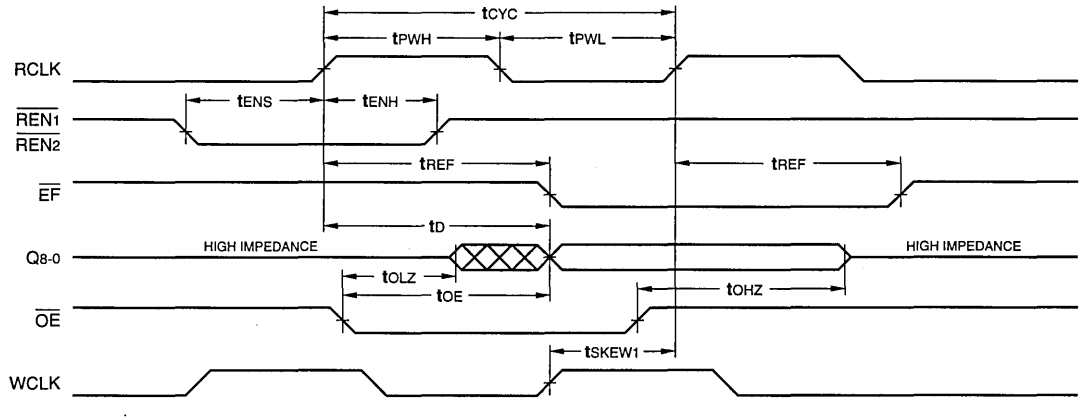


SWITCHING CHARACTERISTICS *Over Operating Range*

READ CYCLE TIMING *Notes 3, 4 (ns)*

		L8C211/221/231/241–							
		50		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20		15	
t_{PWH}	Clock Pulse Width HIGH	20		10		8		6	
t_{PWL}	Clock Pulse Width LOW	20		10		8		6	
t_D	Output Delay	3	25	3	15	2	12	2	10
t_{ENS}	Enable Setup Time	10		6		5		4	
t_{ENH}	Enable Hold Time	1		1		1		1	
t_{OE}	Output Enable to Output Valid	3	25	3	13	3	10	3	8
t_{OLZ}	Output Enable to Output in Low Impedance (Notes 7, 8)	0		0		0		0	
t_{OHZ}	Output Enable to Output in High Impedance (Notes 7, 8)	3	25	3	13	3	10	3	8
t_{REF}	Read Clock to Empty Flag		25		15		12		10
t_{SKEW1}	Skew Time Between Read and Write Clocks for Empty and Full Flags (Note 9)	15		10		8		6	

READ CYCLE TIMING



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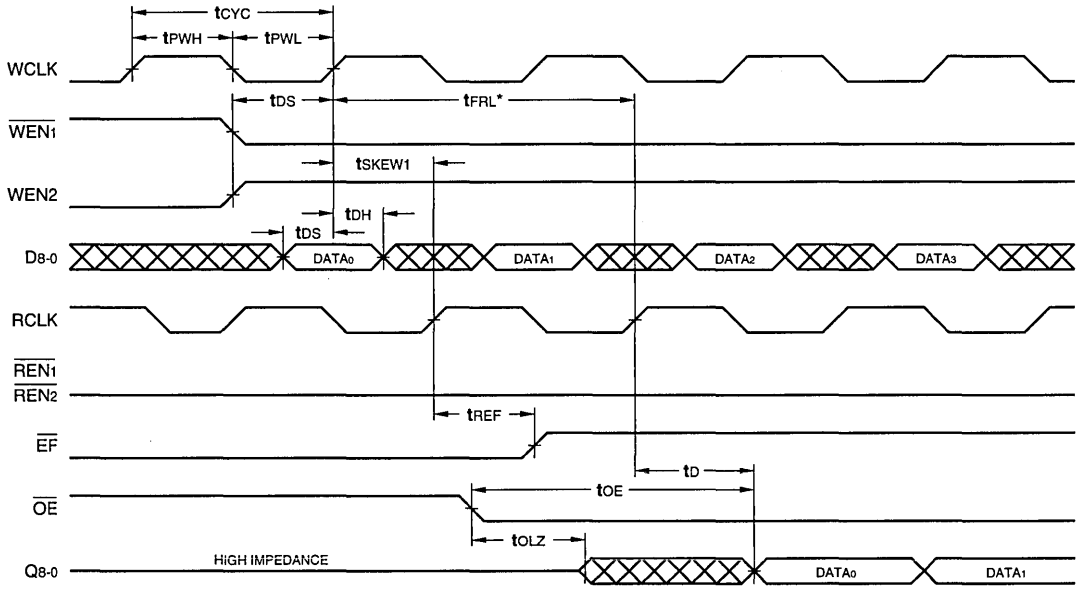
SWITCHING CHARACTERISTICS *Over Operating Range*

FIRST DATA WORD TIMING *Notes 3, 4 (ns)*

		L8C211/221/231/241–							
		50		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20		15	
t_{PWH}	Clock Pulse Width HIGH	20		10		8		6	
t_{PWL}	Clock Pulse Width LOW	20		10		8		6	
t_D	Output Delay	3	25	3	15	2	12	2	10
t_{DS}	Data Setup Time	10		6		5		4	
t_{DH}	Data Hold Time	1		1		1		1	
t_{OE}	Output Enable to Output Valid	3	25	3	13	3	10	3	8
t_{OLZ}	Output Enable to Output in Low Impedance (Notes 7, 8)	0		0		0		0	
t_{REF}	Read Clock to Empty Flag		25		15		12		10
t_{SKEW1}	Skew Time Between Read and Write Clocks for Empty and Full Flags	15		10		8		6	

FIRST DATA WORD TIMING



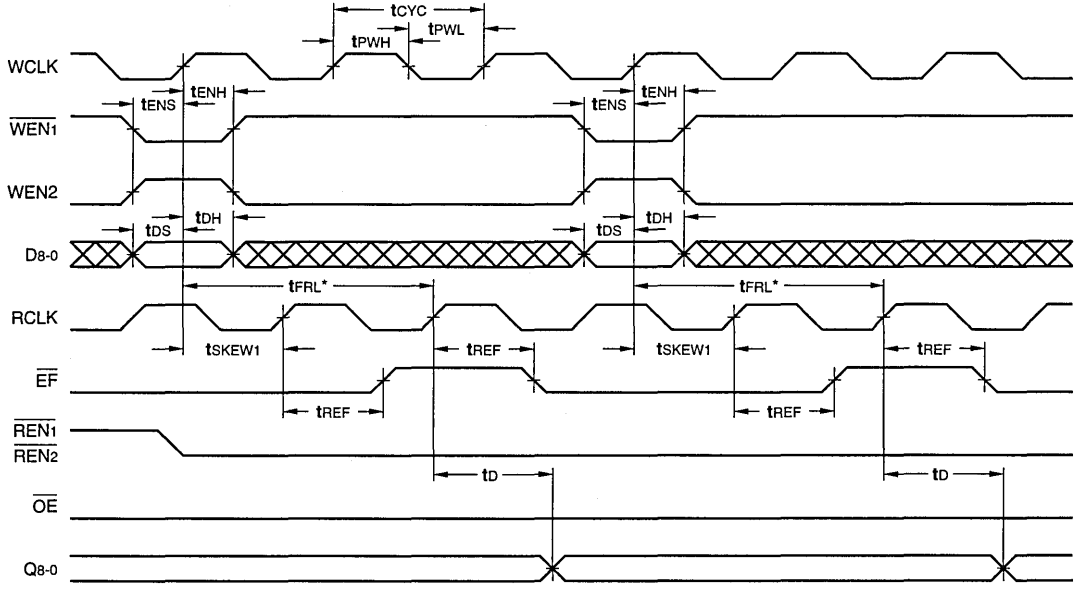
*latency timing is only relevant when the Empty Flag is LOW.
when t_{SKEW1} is less than minimum specification, $t_{FRL} = t_{CYC} + t_{SKEW1}$.
when t_{SKEW1} is greater than minimum specification, $t_{FRL} = 2(t_{CYC}) + t_{SKEW1}$.

SWITCHING CHARACTERISTICS *Over Operating Range*

EMPTY FLAG TIMING *Notes 3, 4 (ns)*

		L8C211/221/231/241–							
		50		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20		15	
t_{PWH}	Clock Pulse Width HIGH	20		10		8		6	
t_{PWL}	Clock Pulse Width LOW	20		10		8		6	
t_D	Output Delay	3	25	3	15	2	12	2	10
t_{DS}	Data Setup Time	10		6		5		4	
t_{DH}	Data Hold Time	1		1		1		1	
t_{ENS}	Enable Setup Time	10		6		5		4	
t_{ENH}	Enable Hold Time	1		1		1		1	
t_{REF}	Read Clock to Empty Flag		25		15		12		10
t_{SKEW1}	Skew Time Between Read and Write Clocks for Empty and Full Flags	15		10		8		6	

EMPTY FLAG TIMING



*latency timing is only relevant when the Empty Flag is LOW.
when t_{SKEW1} is less than minimum specification, $t_{FRL} = t_{CYC} + t_{SKEW1}$.
when t_{SKEW1} is greater than minimum specification, $t_{FRL} = 2(t_{CYC}) + t_{SKEW1}$.

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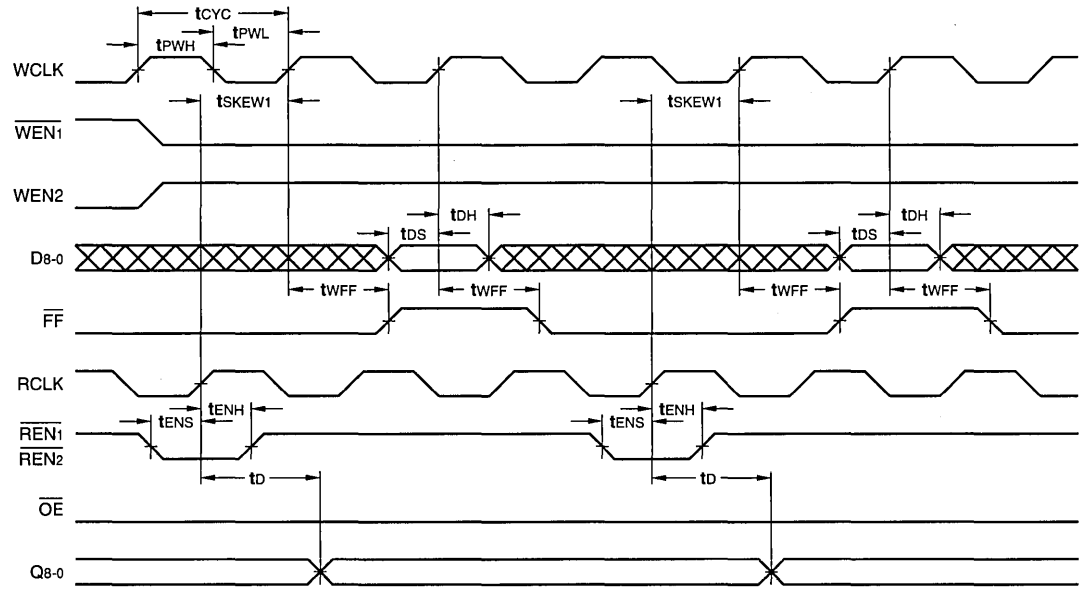
SWITCHING CHARACTERISTICS *Over Operating Range*

FULL FLAG TIMING *Notes 3, 4 (ns)*

		L8C211/221/231/241–							
		50		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20		15	
t_{PWH}	Clock Pulse Width HIGH	20		10		8		6	
t_{PWL}	Clock Pulse Width LOW	20		10		8		6	
t_D	Output Delay	3	25	3	15	2	12	2	10
t_{DS}	Data Setup Time	10		6		5		4	
t_{DH}	Data Hold Time	1		1		1		1	
t_{ENS}	Enable Setup Time	10		6		5		4	
t_{ENH}	Enable Hold Time	1		1		1		1	
t_{WFF}	Write Clock to Full Flag		25		15		12		10
t_{SKEW1}	Skew Time Between Read and Write Clocks for Empty and Full Flags	15		10		8		6	

FULL FLAG TIMING

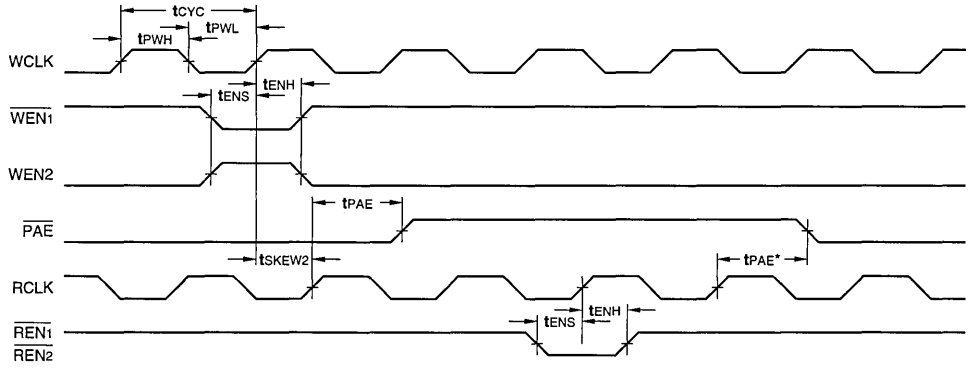


SWITCHING CHARACTERISTICS *Over Operating Range*

PROGRAMMABLE ALMOST-EMPTY/FULL FLAG TIMING *Notes 3, 4 (ns)*

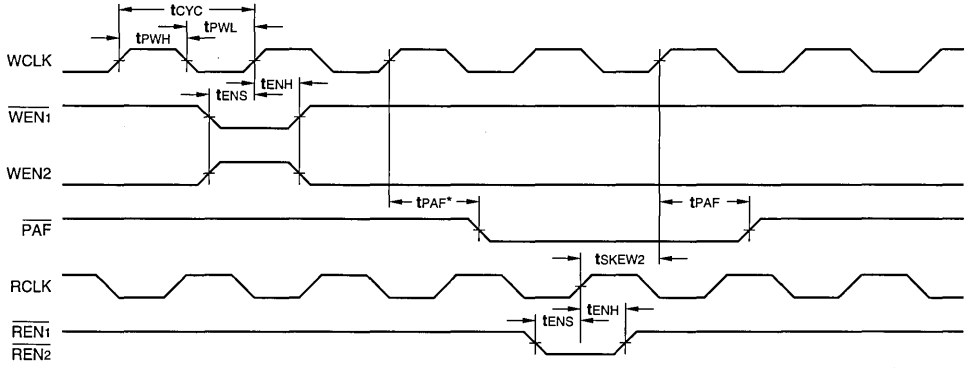
		L8C211/221/231/241–							
		50		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20		15	
t_{PWH}	Clock Pulse Width HIGH	20		10		8		6	
t_{PWL}	Clock Pulse Width LOW	20		10		8		6	
t_{ENS}	Enable Setup Time	10		6		5		4	
t_{ENH}	Enable Hold Time	1		1		1		1	
t_{PAF}	Write Clock to Programmable Almost-Full Flag		25		15		12		10
t_{PAE}	Read Clock to Programmable Almost-Empty Flag		25		15		12		10
t_{SKEW2}	Skew Time Between Read/Write Clocks for Almost-Empty/Full Flags	30		20		18		15	

PROGRAMMABLE ALMOST-EMPTY FLAG *Note 10*



*$\overline{PAE}$ is synchronized to the rising edge of RCLK, but in this case the $\overline{PAE}$ transition takes place in the next clock cycle.

PROGRAMMABLE ALMOST-FULL FLAG *Note 11*



*$\overline{PAF}$ is synchronized to the rising edge of WCLK, but in this case the $\overline{PAF}$ transition takes place in the next clock cycle.

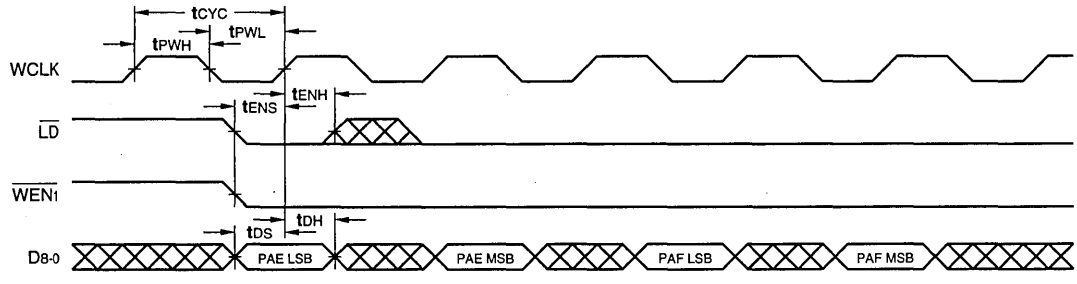
8

SWITCHING CHARACTERISTICS *Over Operating Range*

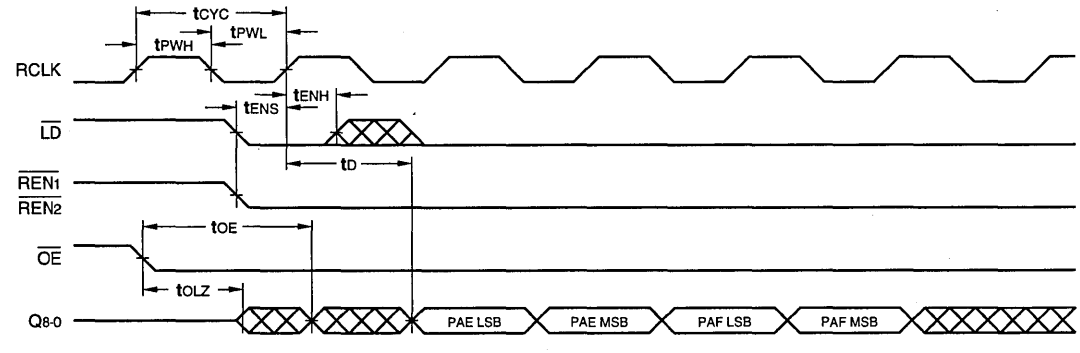
WRITE/READ OFFSET REGISTER TIMING *Notes 3, 4 (ns)*

		L8C211/221/231/241–							
		50		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20		15	
t_{PWH}	Clock Pulse Width HIGH	20		10		8		6	
t_{PWL}	Clock Pulse Width LOW	20		10		8		6	
t_D	Output Delay	3	25	3	15	2	12	2	10
t_{DS}	Data Setup Time	10		6		5		4	
t_{DH}	Data Hold Time	1		1		1		1	
t_{ENS}	Enable Setup Time	10		6		5		4	
t_{ENH}	Enable Hold Time	1		1		1		1	
t_{OE}	Output Enable to Output Valid	3	25	3	13	3	10	3	8
t_{OLZ}	Output Enable to Output in Low Impedance (Notes 7, 8)	0		0		0		0	

WRITE OFFSET REGISTER



READ OFFSET REGISTER



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. Test conditions assume input transition times of 5 ns or less, reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V (Fig. 2).

4. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{DS} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

5. The Read and Write Clocks can be free-running during reset.

6. t_{SKEW1} is the minimum time between the rising edge of RCLK and the rising edge of WCLK for a Full Flag transition to occur in that clock cycle. If t_{SKEW1} is not satisfied, a Full Flag transition may not occur until the next rising WCLK edge.

7. These parameters are guaranteed but not 100% tested.

8. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

9. t_{SKEW1} is the minimum time between the rising edge of WCLK and the rising edge of RCLK for an Empty Flag transition to occur in that clock cycle. If t_{SKEW1} is not satisfied, an Empty Flag transition may not occur until the next rising RCLK edge.

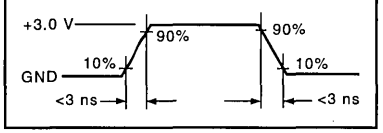
10. t_{SKEW2} is the minimum time between the rising edge of WCLK and the rising edge of RCLK to guarantee that the Programmable Almost-Empty Flag will make a transition to HIGH during that clock cycle. If t_{SKEW2} is not satisfied, the Programmable Almost-Empty Flag may not make the transition to HIGH until the next rising edge of RCLK.

11. t_{SKEW2} is the minimum time between the rising edge of RCLK and the rising edge of WCLK to guarantee that the Programmable Almost-Full Flag will make a transition to HIGH during that clock cycle. If t_{SKEW2} is not satisfied, the Programmable Almost-Full Flag may not make the transition to HIGH until the next rising edge of WCLK.

12. It is not recommended that Logic Devices and other vendor parts be cascaded together. The parts are designed to be pin-for-pin compatible but temperature and voltage compensation may vary from vendor to vendor. Logic Devices can only guarantee the cascading of Logic Devices parts to other Logic Devices parts.

13. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

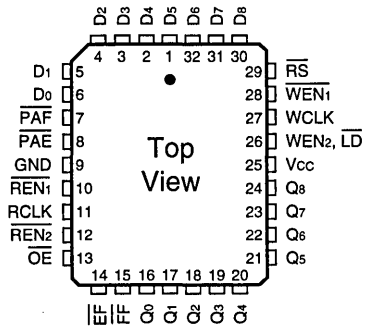
FIGURE 2.



8

L8C211 — ORDERING INFORMATION

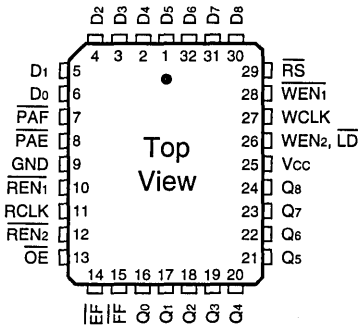
32-pin



Speed	Plastic J-Lead Chip Carrier (J6)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	L8C211JC50
25 ns	L8C211JC25
20 ns	L8C211JC20
15 ns	L8C211JC15
	–40°C to +85°C — COMMERCIAL SCREENING
50 ns	L8C211JI50
25 ns	L8C211JI25
20 ns	L8C211JI20
15 ns	L8C211JI15

L8C221 — ORDERING INFORMATION

32-pin

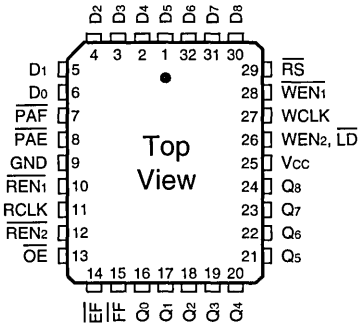


Speed	Plastic J-Lead Chip Carrier (J6)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	L8C221JC50
25 ns	L8C221JC25
20 ns	L8C221JC20
15 ns	L8C221JC15
	–40°C to +85°C — COMMERCIAL SCREENING
50 ns	L8C221JI50
25 ns	L8C221JI25
20 ns	L8C221JI20
15 ns	L8C221JI15

8

L8C231 — ORDERING INFORMATION

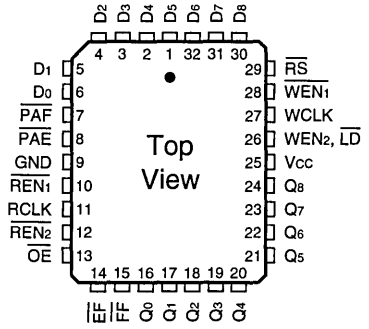
32-pin



Speed	Plastic J-Lead Chip Carrier (J6)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	L8C231JC50
25 ns	L8C231JC25
20 ns	L8C231JC20
15 ns	L8C231JC15
	–40°C to +85°C — COMMERCIAL SCREENING
50 ns	L8C231JI50
25 ns	L8C231JI25
20 ns	L8C231JI20
15 ns	L8C231JI15

L8C241 — ORDERING INFORMATION

32-pin



Speed	Plastic J-Lead Chip Carrier (J6)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	L8C241JC50
25 ns	L8C241JC25
20 ns	L8C241JC20
15 ns	L8C241JC15
	–40°C to +85°C — COMMERCIAL SCREENING
50 ns	L8C241JI50
25 ns	L8C241JI25
20 ns	L8C241JI20
15 ns	L8C241JI15

8

Quality and Reliability

Copies of the LOGIC Devices **"Quality Assurance Program Manual"** and **"Quality Assurance Reliability Manual"** may be obtained from LOGIC Devices by contacting our applications group at (408) 542-5446 between 8:00 AM and 6:00 PM Pacific time, Monday through Friday. Both manuals may also be downloaded from LOGIC Devices Website at **http://www.logicdevices.com**.

Package Information

10

Latchup and ESD Protection

Latchup is a destructive phenomenon which was once common in CMOS circuits but has now been largely eliminated by improved circuit design techniques. Latchup takes place because of the existence in CMOS of an inherent PNPN or NPNP structure between VCC and ground. Either of these two can form a pair of transistors connected so as to form a positive feedback loop, with the collector of one transistor driving the base of the other. The result is a low-impedance path from VCC to ground, which cannot be interrupted except by the removal of power. This condition can be destructive if the area involved is sufficiently large to dissipate excessive power. One example of the formation of such a structure is shown in Figure 1. The equivalent circuit is shown in Figure 2.

As shown in Figure 1, the N+ regions which form the source and drain of an N-channel MOS transistor also act as the emitters of a parasitic NPN transistor. The P-well forms the base region and the N-substrate is the collector. The current gain of this transistor is relatively high because it is formed vertically and therefore the base width is quite small. This is especially true of fine-geometry CMOS processes which tend to have very shallow wells to reduce sidewall capacitance. The P+ region in the well is called a "well tap" and is present to form a low-resistance connection between the well and ground. The source region cannot serve this function because it forms a diode between the N+ source and the P-well.

Also shown in Figure 1 is an additional parasitic PNP transistor. The source and drain regions of the P-channel MOS device form the emitters, the N-substrate is the base, and the P-well is the collector. This transistor is a PNP, and generally has a beta (β) much less than 1 since it is formed laterally and the gate region is relatively large. Like the vertical NPN, it can have multiple emitters. The N+ region tied to VCC in the substrate functions similarly to the well tap discussed above.

Note that the base of the NPN and the collector of the PNP are a common region (the P-well), and similarly the base of the PNP and the collector of the NPN are common (the N-substrate). Thus, the PNPN structure necessary for latchup is formed. Also, due to the the physical distance between the well and substrate taps and the base regions which they attempt to contact, a small resistance exists between the base regions and their respective well taps, denoted RS (substrate) and RW (well).

Latchup begins when a perturbation causes one of the bipolar transistors to turn on. An example would be excursion of the output pad below ground or above VCC due to transmission-line ringing. If the pad goes more than 0.7 V below ground, the NPN will turn on since its base is at approximately ground potential. The NPN's collector current will cause a voltage drop across RS, the bulk substrate resistance. This voltage drop turns on the PNP.

The PNP transistor's collector current forces a similar voltage drop across RW, the well resistance. This raises the base voltage of the NPN above ground and can cause the NPN to continue to conduct even after the output pad returns to a normal voltage range. In this case, the current path shifts to the grounded emitter.

Note that any effect which can cause a transient turn-on of either transistor can cause the latchup process.

Common causes include:

1. Ringing of unprotected I/O pins outside the ground to VCC region.
2. Radiation-induced carriers generated in the base of the bipolar transistors.
3. Hot-powerup of the device, with inputs driven HIGH before VCC is applied.
4. Electrostatic discharge.

PROTECTING AGAINST LATCHUP

Latchup, while once a severe problem for CMOS, is now a relatively well-understood phenomenon. In order for latchup to occur, the product of the current gains of the two parasitic transistors must exceed 1. Thus, the primary means for avoiding latchup is the insertion of structures known as "guard rings" around all MOS transistors (and other structures) likely to be subjected to latchup-causing transients. This includes output buffer transistors and any devices which form a part of the ESD protection network. These guard rings absorb current which would otherwise drive the base of the lateral device, and thus dramatically reduce its gain.

Since external electrical perturbations are the dominant cause of latchup in non-radiation environments, protecting the "periphery" of the chip is most important. Therefore, since guard rings require a lot of area, they are generally used only in critical areas such as those mentioned above.

As an additional protective measure, strict rules are enforced in the layout regarding the positioning of the substrate and well taps. They are spaced closely together throughout

FIGURE 1. PARASITIC TRANSISTOR STRUCTURES IN PARALLEL CMOS

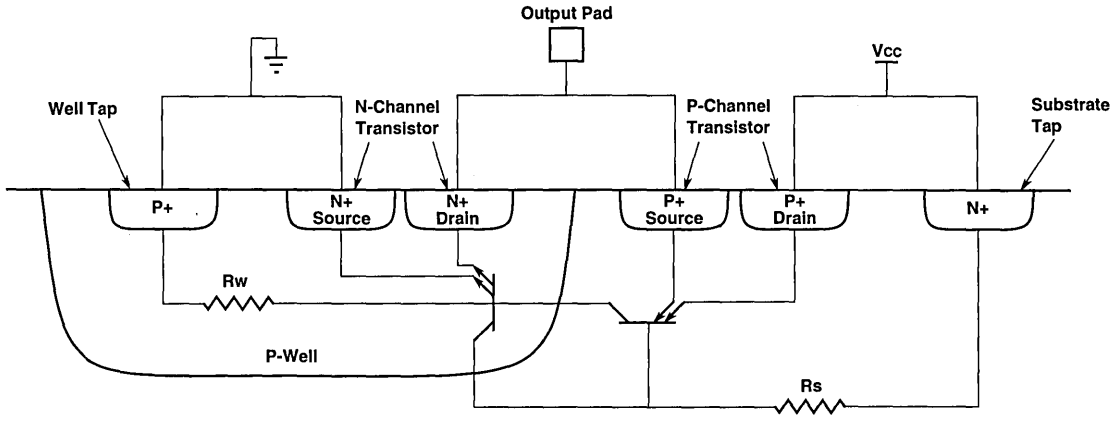
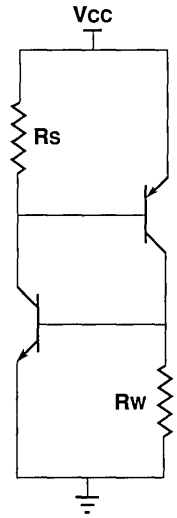


FIGURE 2. EQUIVALENT CIRCUIT FOR LATCHUP PATH



the die, reducing the values of Rs and Rw. This makes it more difficult to develop the base drive necessary to regenerate the latchup condition.

Measurement of susceptibility to latchup is done by connecting a current source to an input or output of the device under test. By increasing the current forced to flow into the pin and noting the point at which latchup occurs, a measure of the device's ability to resist latchup-inducing carrier injection is obtained. Note that depending on the device, the current source may require a rather large voltage compliance in order to provide an adequate test.

While early CMOS devices had a latchup trigger current of a few tens of milliamps, most current LOGIC Devices products typically can withstand more than 1 amp without latching. As a result, latchup is no longer a practical concern, except for extreme conditions such as driving multiple inputs HIGH with a low-impedance source during powerup of the device.

ELECTROSTATIC DISCHARGE

Input protection structures on CMOS devices are used to protect against damage to the gate oxides of input transistors when accumulated static charge is discharged through a device. This charge can often reach potentials of several thousand volts. The input protection network is designed to shunt this charge safely to ground or Vcc, bypassing the delicate MOS transistors.

Several features are required of a good input protection network. Since static discharge pulses exhibit very fast rise-times, it must have a very fast turn-on time. It must be capable of carrying large instantaneous currents without damage. It must prevent the voltage

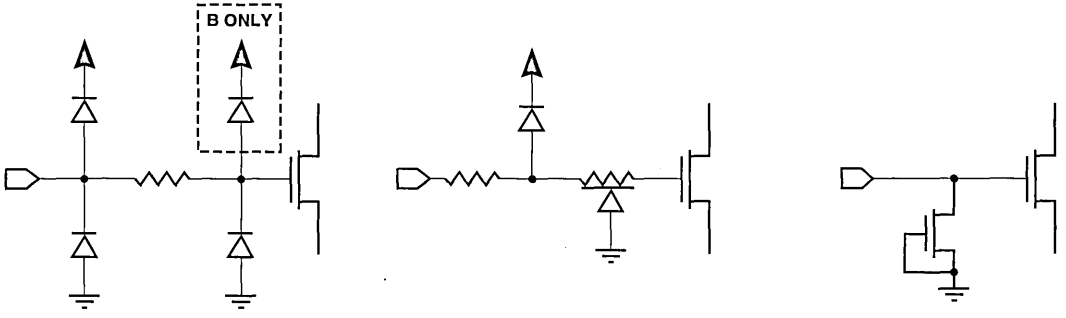
at the circuit input from rising above approximately 10 V during the time when the several-thousand-volt discharge is shunted to ground. It must not create appreciable delay for fast edges which are within the 0–5 V input range. And finally, it must be well protected against latchup caused by inputs which are driven beyond the supply rails, injecting current into the substrate. Much research and experimentation has been devoted to optimizing the tradeoffs between these conflicting goals.

All LOGIC Devices products employ one of the three input protection structures shown in Figure 3. Most devices currently use the Type 1 input protection. This structure is designed to absorb very high static discharge energies and will draw substantial current from the input pin if driven beyond either supply rail. Hence, it provides a "hard" clamp. Besides its advantages for static protection, this clamp can effectively reduce undershoot energy, preventing oscillation of an unterminated input back above the 0.8 V V_{IL} MAX level. This makes the circuit ideal for noisy environments and ill-behaved signals. This input structure may not be driven to a high level without power applied to the device, however. To do so would result in current flowing through the diode connected to the device's V_{CC} rail, and supplying power to the entire board or system backward through the device V_{CC} pin. This may overstress the bond wire or device metallization, resulting in failure.

The Type 2 structure employs a series resistor prior to the two clamp diodes. This results in a "soft" clamping effect. This structure will withstand the transient application of voltages outside the supply rails for brief periods without drawing excessive current. In contrast to the Type 1 structure, this circuit will provide only a modest reduction of the energy in an undershoot pulse. However, it is somewhat more tolerant of power-up sequences which cause the inputs to be driven before V_{CC} is applied. In the course of routine product upgrades, devices employing this structure are being redesigned to use a Type 1 input protection.

The Type 3 structure uses a large area N-channel transistor (part of an open-drain output buffer) to protect the input. The drain-well junction of this device serves the function of a diode connected between the input and ground, protecting against negative excursions of the input. The avalanche breakdown of the output device serves to protect against positive pulses, giving the effect of a zener diode between the input and ground. This circuit is used only for inputs which are designed to have their inputs driven without power applied. The lack of a diode to V_{CC} prevents sourcing of power from the inputs to the V_{CC} supply.

FIGURE 3. INPUT PROTECTION DEVICES



10

Power Dissipation in LOGIC Devices Products

In calculating the power dissipation of LOGIC Devices products, attention must be given to a number of formerly second-order effects which were generally ignored when dealing with bipolar and NMOS technologies. By far the dominant contributor to power dissipation in most CMOS devices is the effective current path from the supply to ground, created by the repetitive charging and discharging of the load capacitance. This is distinct from DC loading effects, which may also consume power. The power dissipated in the load capacitance is proportional to CV^2F, where C is the load capacitance, V is the voltage swing, and F is the switching frequency. This mechanism can frequently contribute 80% or more of the total device dissipation of a truly complementary device operating at a high clock rate.

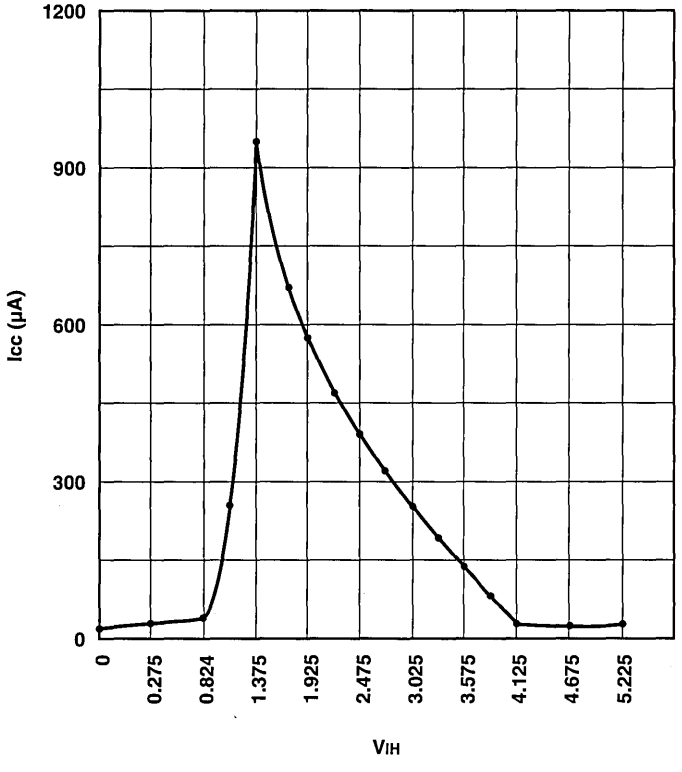
The second contributor to the power dissipation of a CMOS device is the DC current path between V_{CC} and ground present in the input level translators. These circuits are voltage amplifiers which are designed to convert worst case 0.8–2.0 V TTL-compatible input levels to 0 and 5 V internal levels. With 2.0 V applied to the input of most level translator circuits, about 1 mA will flow from the power supply to ground. A floating input will at best have similar results, and may result in oscillations which can dissipate orders of magnitude more power and cause malfunctioning of the device.

The power dissipation of input level translators exhibits a strong peak at about 1.4 V but is reduced substantially when the input voltage exceeds 3.0 V (see Figure 1). Fortunately, this voltage is easy to achieve in practice, even for bipolar devices with TTL I/O structures. These generally will produce a V_{OH} of at least 3.5 V if not fully loaded. As a result, dissipation in the input structures is usually negligible compared to other sources.

Two further sources of power dissipation in CMOS come from the core logic. The sources of internal power dissipation are the same as those discussed for external nodes, namely repetitive charging of the parasitic load capacitances on each gate output, and the power drawn due to a direct current path to ground when gate input voltage levels transition through the linear region. In practice, the internal voltage waveforms are characterized by high edge rates and rail-to-rail swings. For this reason, the latter source of dissipation is usually negligible, unless NMOS or other non-complementary logic design techniques have been used.

The capacitance of typical internal nodes in CMOS logic circuits are a few femtofarads. However, there can be thousands, or tens of thousands of such nodes. As a result, the core

FIGURE 1.



power dissipation is strongly dependent on the average rate at which these nodes switch (the "F" in CV^2F). Fortunately, for most complex logic circuits, with non-pathological external stimulus only a small fraction of the logic nodes switch on any given cycle. For this reason, internal power is generally quite small for these device types. Exceptions include devices containing long shift registers or other structures which can exhibit high duty cycles on most internal nodes. These devices can dissipate significant power in the core logic if stimulated with alternating data patterns and clocked at a high rate.

To summarize, of the several contributors to power dissipation, the CV^2F power of the outputs is usually dominant. Because output loading is system-dependent, it is not possible for the manufacturer to accurately predict total power dissipation in actual use. As a result, LOGIC Devices extrapolates measured power dissipation values to a zero-load environment and publishes the resulting value. This value includes the effects of worst-case input and power-supply voltages, temperature, and stimulus pattern, but not CV^2F. This value is weakly frequency dependent, and the frequency at which it is measured is published in the device data sheet. The maximum value is for worst-case pattern, and the typical is for a more random pattern and is therefore more representative of what would be experienced in actual practice.

A good estimate of total power dissipation in a particular system under worst-case conditions can be obtained by adding the calculated output power to the *typical* published figure. The output power is given by:

$$\frac{NCV^2F}{4}$$

where:

N = the number of device outputs (divided by 2 to account for the assumption that on average, half of the outputs switch on any given cycle)

C = the output load capacitance, per pin, given in Farads

V = the power supply voltage

F = the clock frequency (divided by 2 to account for the fact that a registered output can at most switch at only half the clock rate).

A less pessimistic estimate, appropriate for complex devices when reasonable input voltage levels and non-pathological patterns can be expected, would neglect the published value and use only the calculated value as given above.

Package Information

Package Information

Package Information

LOGIC Devices/MIL-STD-1835 Package Code Cross-Reference

LOGIC DEVICES PACKAGE CODE	DESCRIPTION	MIL-STD-1835 PACKAGE DESIGNATOR	MIL-STD-1835 DIMENSION REFERENCE
CERAMIC DIP			
C1	24-pin, 0.3" wide	GDIP3-T24	D-9
C2	20-pin, 0.3" wide	GDIP1-T20	D-8
C3	22-pin, 0.3" wide	N/A	N/A
C4	24-pin, 0.6" wide	GDIP1-T24	D-3
C5	28-pin, 0.3" wide	GDIP4-T28	D-15
C6	28-pin, 0.6" wide	GDIP1-T28	D-10
C7	16-pin, 0.3" wide	GDIP1-T16	D-2
C8	18-pin, 0.3" wide	GDIP1-T18	D-6
C9	32-pin, 0.6" wide	GDIP1-T32	D-16
C10	28-pin, 0.4" wide	N/A	N/A
C11	40-pin, 0.6" wide	GDIP1-T40	D-5
SIDEBRAZE, HERMETIC DIP			
D1	24-pin, 0.6" wide	CDIP2-T24	D-3
D2	24-pin, 0.3" wide	CDIP4-T24	D-9
D3	40-pin, 0.6" wide	CDIP2-T40	D-5
D4	64-pin, 0.9" wide, cavity up	CDIP1-T64	D-13
D5	48-pin, 0.6" wide	CDIP2-T48	D-14
D6	64-pin, 0.9" wide, cavity down	CDIP1-T64	D-13
D7	20-pin, 0.3" wide	CDIP2-T20	D-8
D8	22-pin, 0.3" wide	N/A	N/A
D9	28-pin, 0.6" wide	CDIP2-T28	D-10
D10	28-pin, 0.3" wide	CDIP3-T28	D-15
D11	28-pin, 0.4" wide	N/A	N/A
D12	32-pin, 0.4" wide	N/A	N/A
FLATPACK			
F1	24-pin	CDFP4-F24	F-6A
F2	28-pin	CDFP4-F28	F-12
F5	132-pin	CQCC1-G132	C-G7
CERAMIC PGA			
G1	68-pin, cavity up	CMGA3-P68	P-AC
G2	68-pin, cavity down	CMGA3-P68	P-AC
G3	84-pin	CMGA15-P84	P-BC
G4	120-pin	CMGA3-P121	P-AC

LOGIC Devices/MIL-STD-1835 Package Code Cross-Reference

LOGIC DEVICES PACKAGE CODE	DESCRIPTION	MIL-STD-1835 PACKAGE DESIGNATOR	MIL-STD-1835 DIMENSION REFERENCE
CERAMIC LEADLESS CHIP CARRIER			
K1	28-pin, 0.450" x 0.450"	CQCC1-N28	C-4
K2	44-pin, 0.650" x 0.650"	CQCC1-N44	C-5
K3	68-pin, 0.950" x 0.950"	CQCC1-N68	C-7
K4	22-pin, 0.290" x 0.490"	N/A	N/A
K5	28-pin, 0.350" x 0.550"	CQCC4-N28	C-11A
K6	20-pin, 0.290" x 0.425"	CQCC3-N20	C-13
K7	32-pin, 0.450" x 0.550"	CQCC1-N32	C-12
K8	20-pin, 0.350" x 0.350"	CQCC1-N20	C-2
K9	48-pin, 0.550" x 0.550"	N/A	N/A
K10	32-pin, 0.450" x 0.700"	N/A	N/A
CERAMIC FLATPACK			
M1	24-pin	GDFP2-F24	F-6
M2	28-pin	GDFP2-F28	F-11
CERAMIC SOJ			
Y1	32-pin, 0.440" wide	N/A	N/A

Thermal Considerations

The temperature at which a semiconductor device operates is one of the primary determinants of its reliability. This temperature is often referred to as the "junction temperature", although this term is more appropriate for bipolar than MOS technologies. Heat dissipated in the device during operation escapes through a path consisting of one or more series thermal impedances terminating in the surrounding air (see Figure. 1).

The presence of this nonzero thermal impedance causes the temperature of the device to rise above that of the air. Each of the components of the overall thermal impedance causes a rise in temperature which is linearly dependent on the power dissipated in the device. The coefficient is called θ, and has the units °C/W. The θ value for each thermal impedance represents the amount of temperature rise across the impedance as a function of the power dissipation. Usually, θ is given a subscript indicating the two points between which the impedance is measured. Thus the junction temperature of an operating device is given by:

$$T_j = T_{AMB} + (Pd \bullet \theta_{JA})$$

where:

T_j = junction temperature of the device, °C,

T_{AMB} = ambient air temperature, in°C

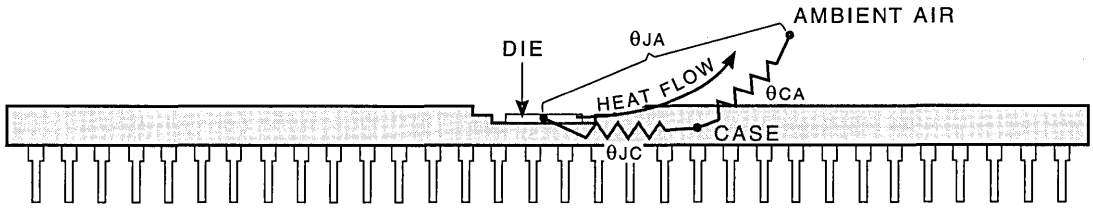
Pd = power dissipation of the device, in W,

θ_{JA} = sum of all thermal impedances between the die and the ambient air, in °C/W.

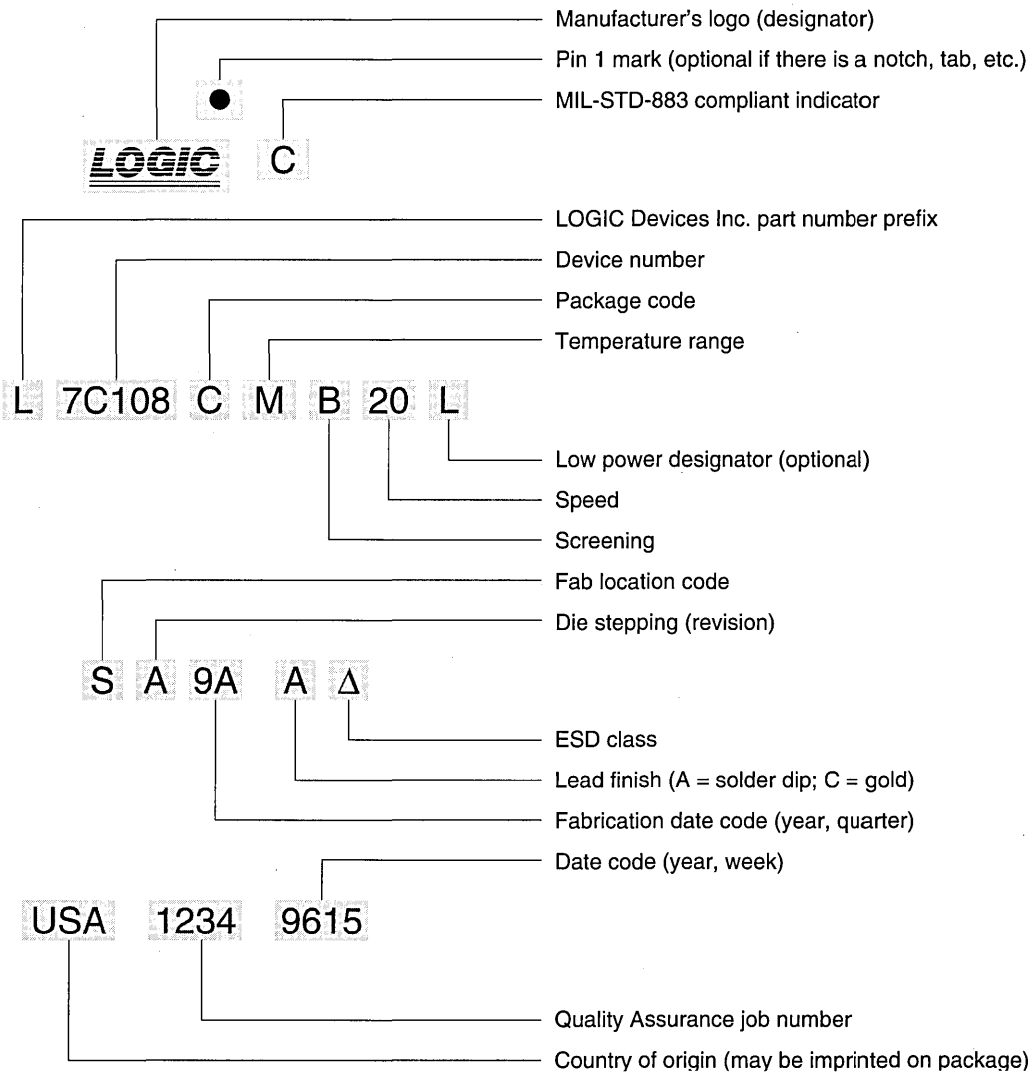
The thermal impedance of a given device is dependent on several factors. The package type is the predominant effect; ceramic packages have much lower thermal impedances than plastic, and packages with large surface areas tend to dissipate heat faster. Another factor which is beyond the control of the device manufacturer but which is nonetheless important is the temperature and flow rate of the cooling air. Secondary effects include the size of the die, the method of attaching the die to the package, and the organization of high power dissipation elements on the die.

Because all LOGIC Devices products are built with low-power CMOS technology, thermal impedance is less of a concern than it would be for higher power technologies. As an example, consider a typical NMOS multiplier similar to the LMU16, packaged in a 64-pin plastic DIP. Assuming 1 W power dissipation and θ_{JA} of 50°C/W, the actual die temperature would be 50°C above the surrounding air. By contrast, the LOGIC Devices LMU16 has a typical power dissipation of only 60 mW. This device in the same package would operate at only 3° above the ambient air temperature. Since operating temperature has an exponential relationship to device failure rate (see Quality and Reliability Manuals), the reduction of die temperature available with LOGIC Devices low-power CMOS translates to a marked increase in expected reliability.

FIGURE 1.



Package Marking Guide



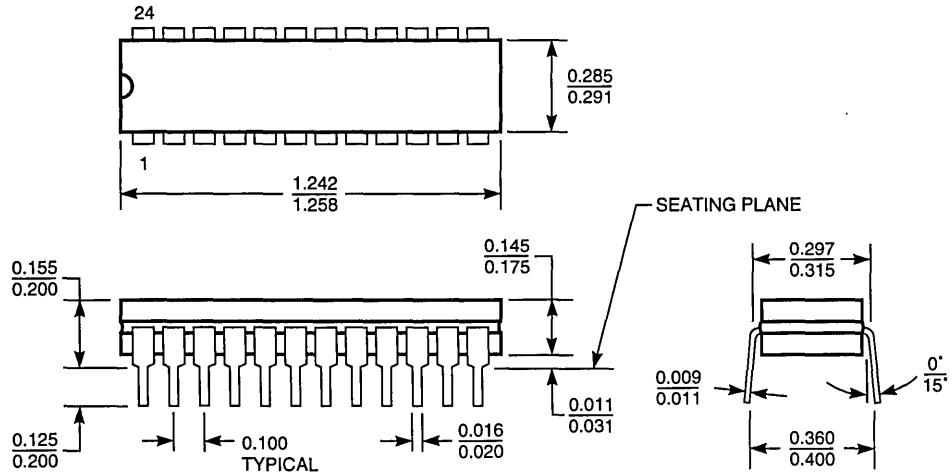
NOTE: Package marking may occur on top and bottom of package due to space limitations

Mechanical Drawings

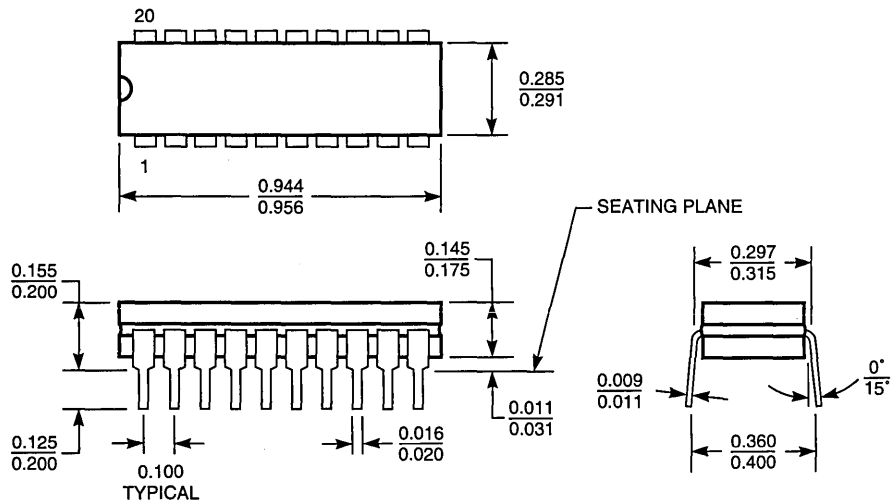
- Ceramic Dual In-line Package
- Sidebraze, Hermetic Dual In-line Package
- Flatpack
- Ceramic Pin Grid Array
- Plastic J-Lead Chip Carrier
- Ceramic Leadless Chip Carrier
- Ceramic Flatpack
- Plastic Dual In-line Package
- Plastic Quad Flatpack
- Plastic Small Scale Outline Package
- Plastic Small Outline J-Lead
- Ceramic Small Outline J-Lead

CERAMIC DIP (ORDERING CODE: C, I)

C1 — 24-pin, 0.3" wide

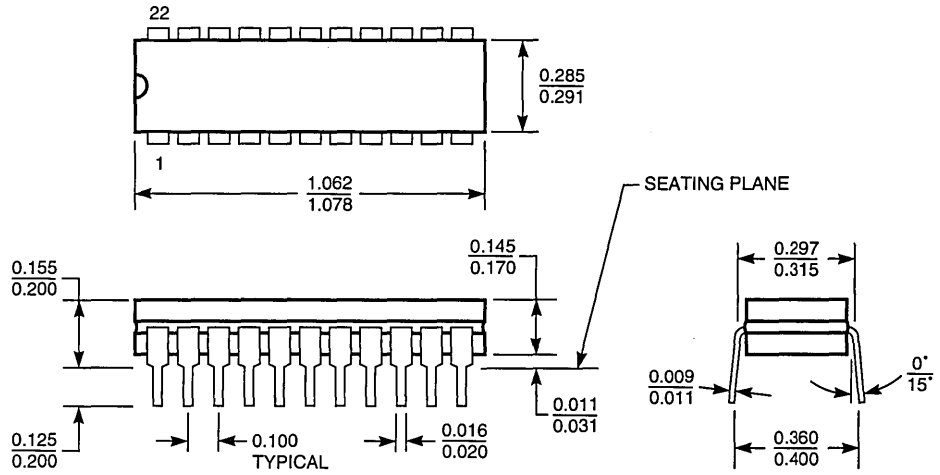


C2 — 20-pin, 0.3" wide

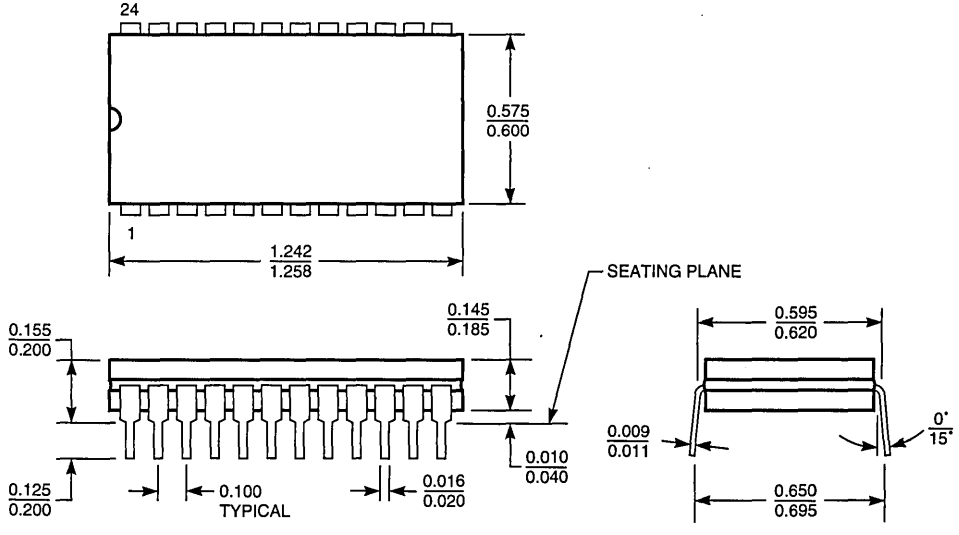


CERAMIC DIP (ORDERING CODE: C, I)

C3 — 22-pin, 0.3" wide



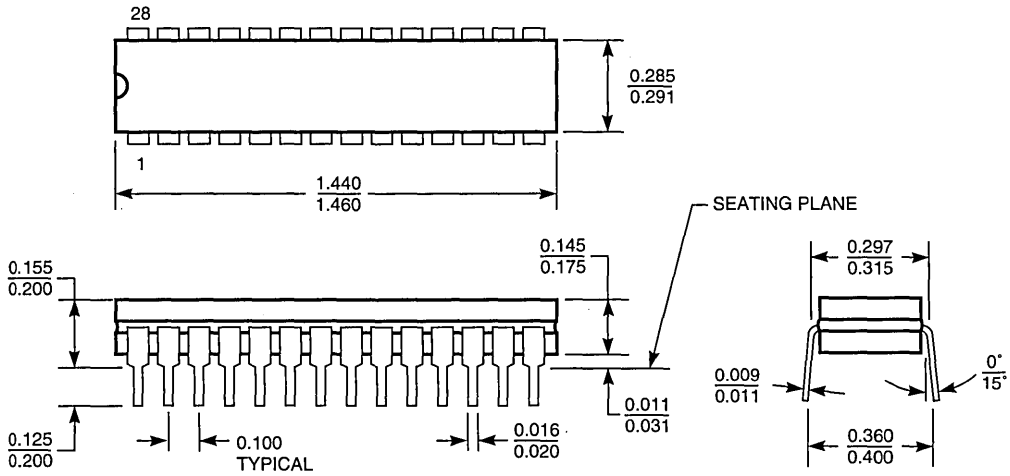
C4 — 24-pin, 0.6" wide



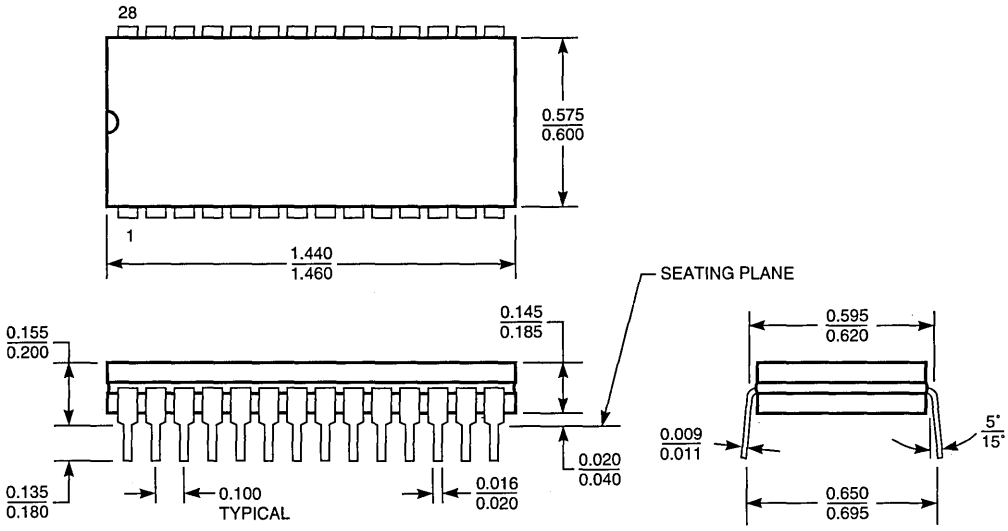
11

CERAMIC DIP (ORDERING CODE: C, I)

C5 — 28-pin, 0.3" wide

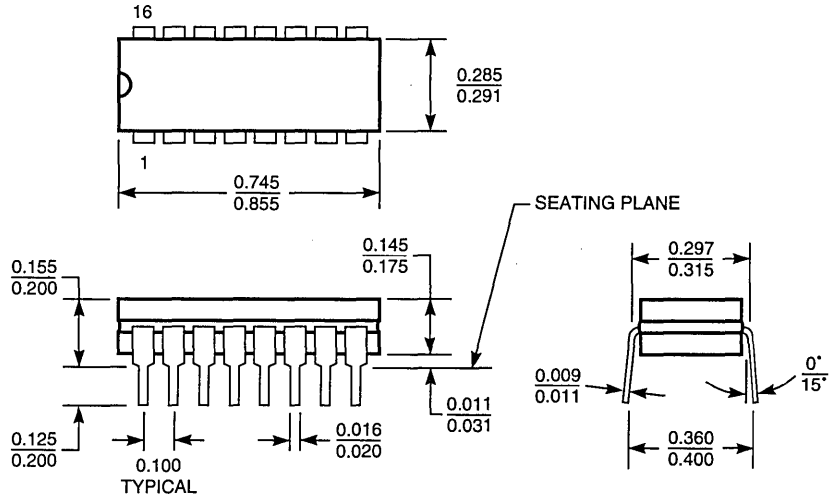


C6 — 28-pin, 0.6" wide

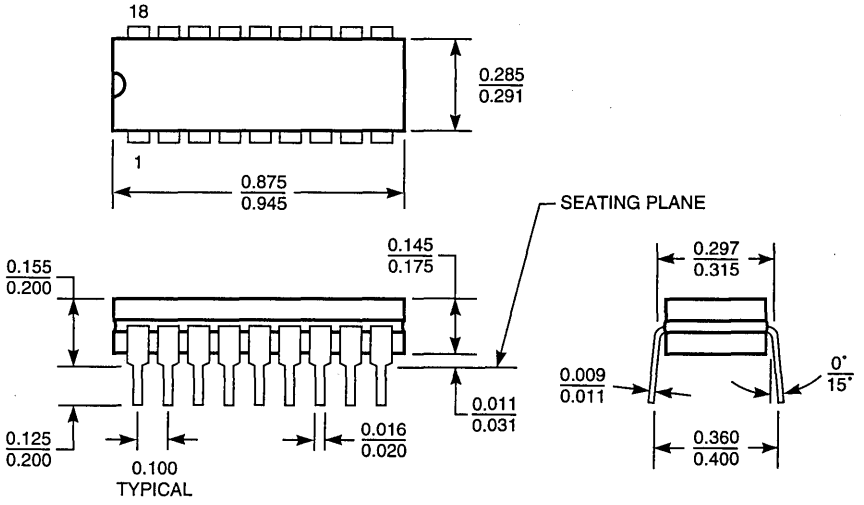


CERAMIC DIP (ORDERING CODE: C, I)

C7 — 16-pin, 0.3" wide



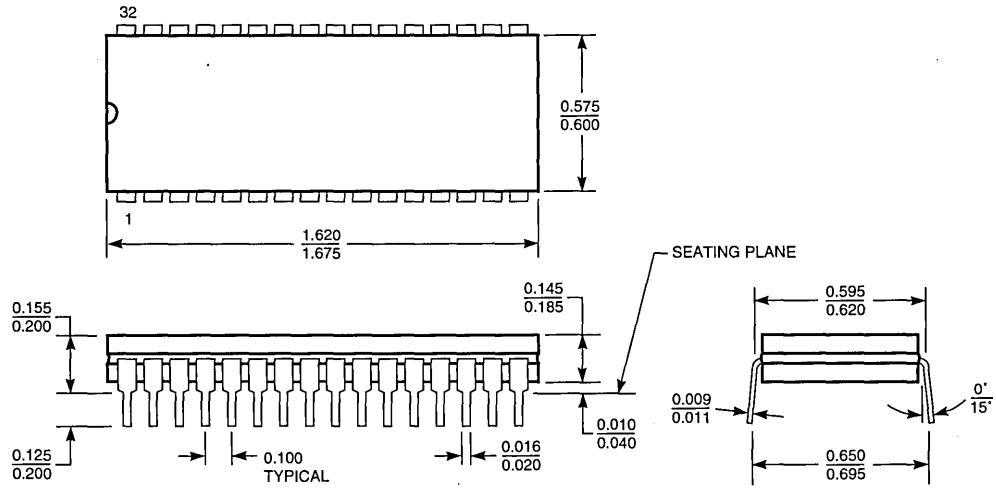
C8 — 18-pin, 0.3" wide



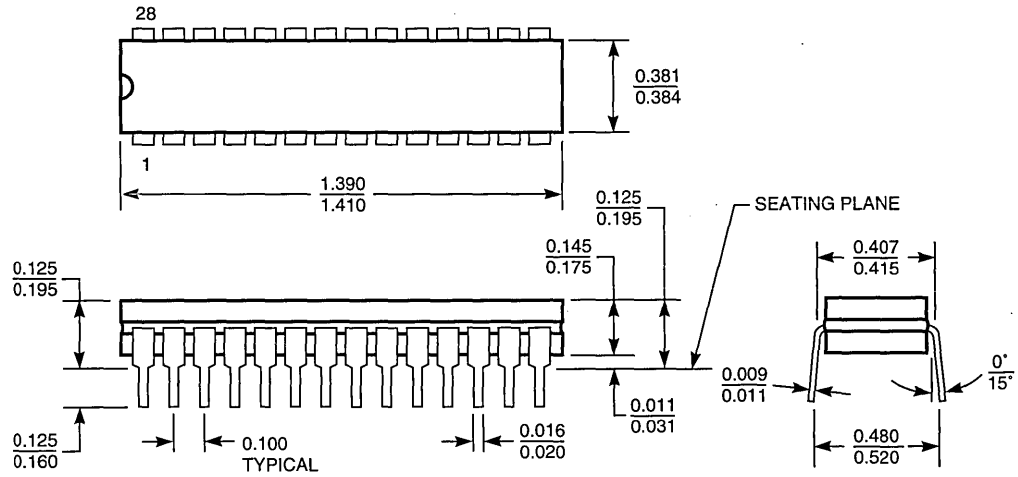
11

CERAMIC DIP (ORDERING CODE: C, I)

C9 — 32-pin, 0.6" wide

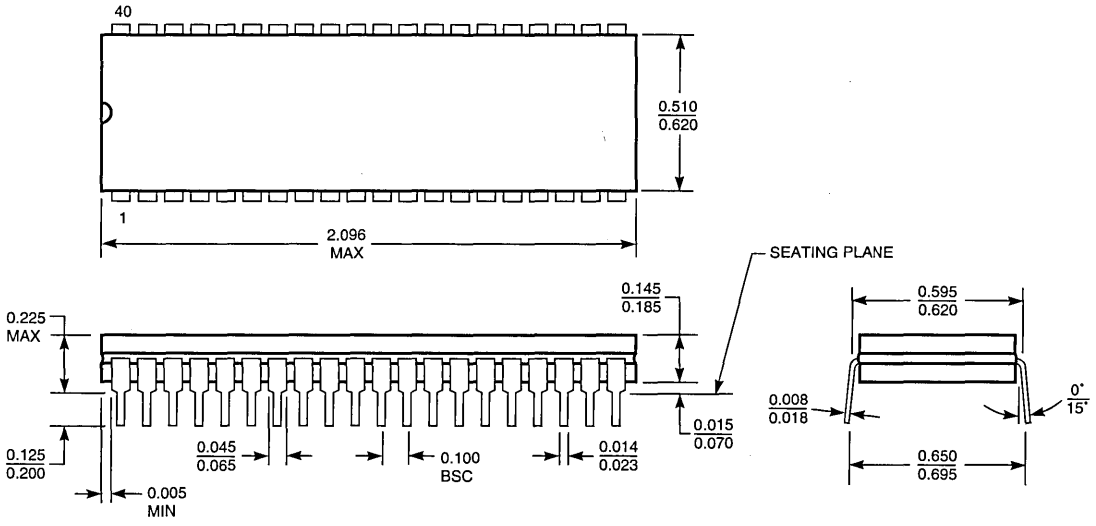


C10 — 28-pin, 0.4" wide



CERAMIC DIP (ORDERING CODE: C, I)

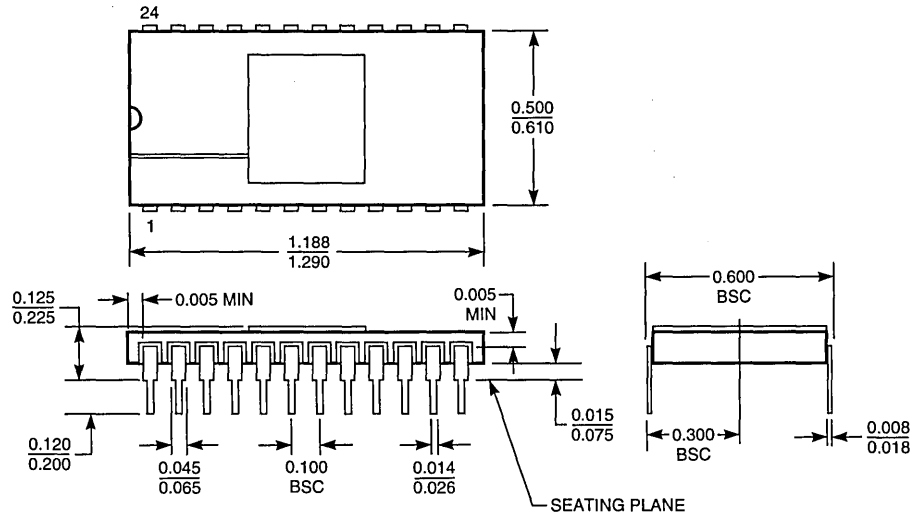
C11 — 40-pin, 0.6" wide



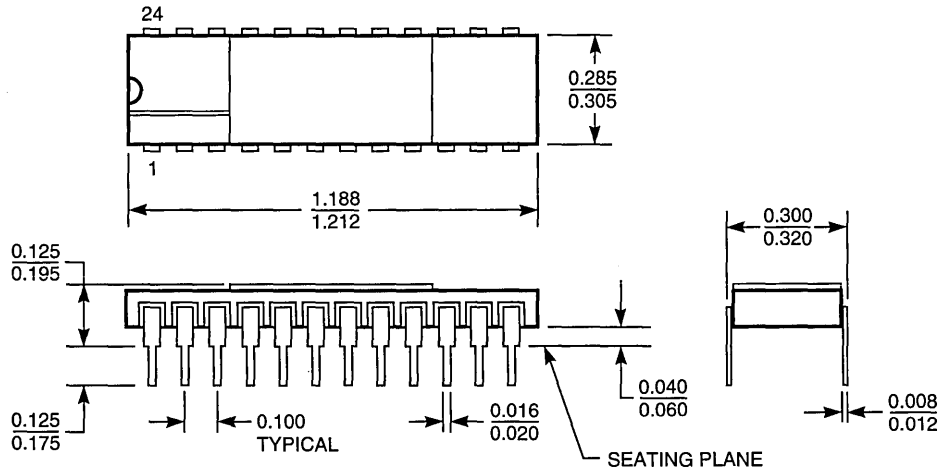
11

SIDEBRAZE, HERMETIC DIP (ORDERING CODE: D, H)

D1 — 24-pin, 0.6" wide

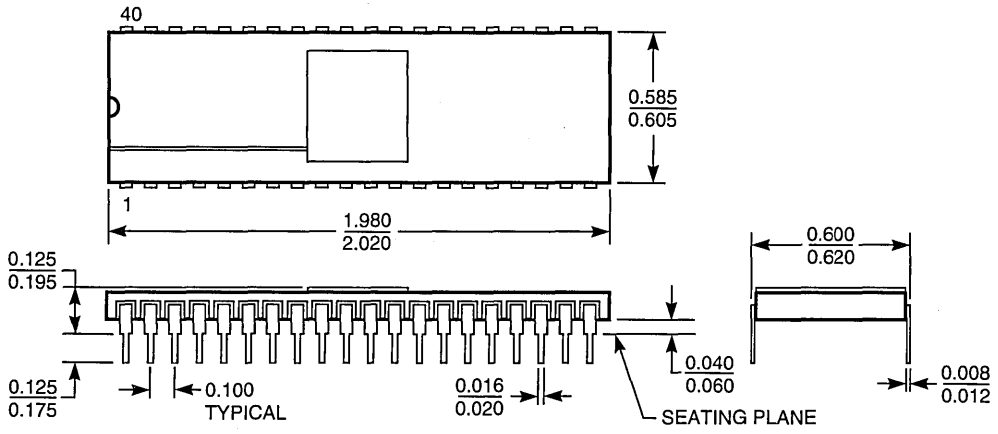


D2 — 24-pin, 0.3" wide

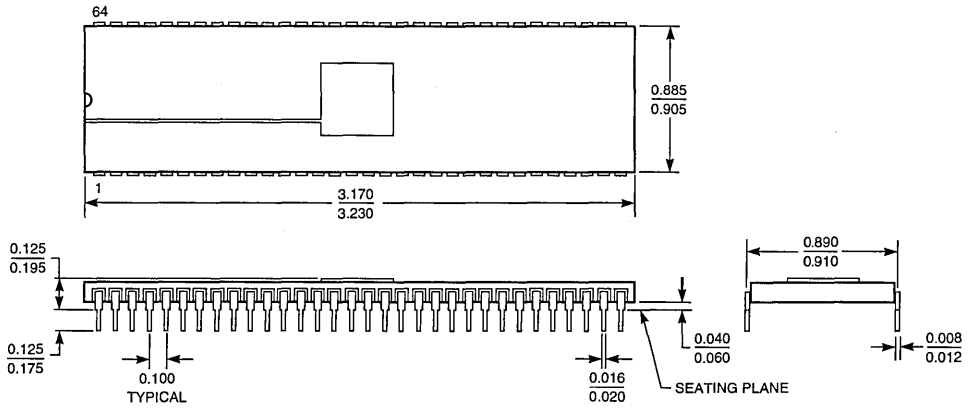


SIDEBRAZE, HERMETIC DIP (ORDERING CODE: D, H)

D3 — 40-pin, 0.6" wide



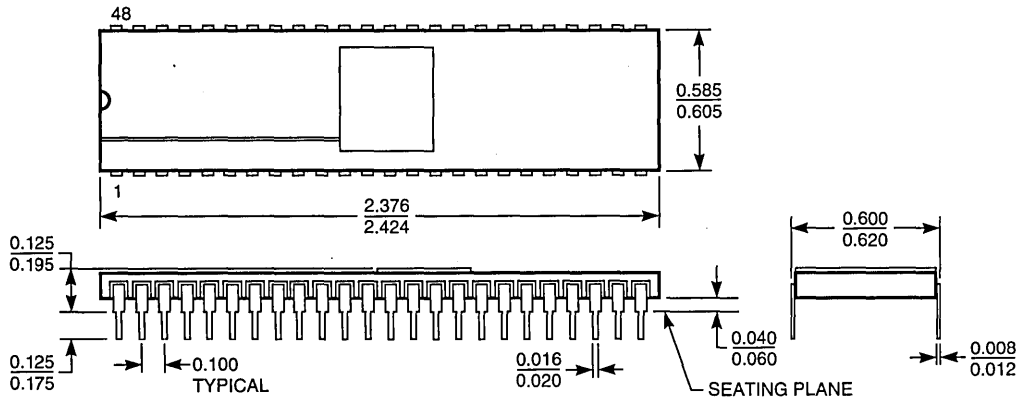
D4 — 64-pin, 0.9" wide, cavity up



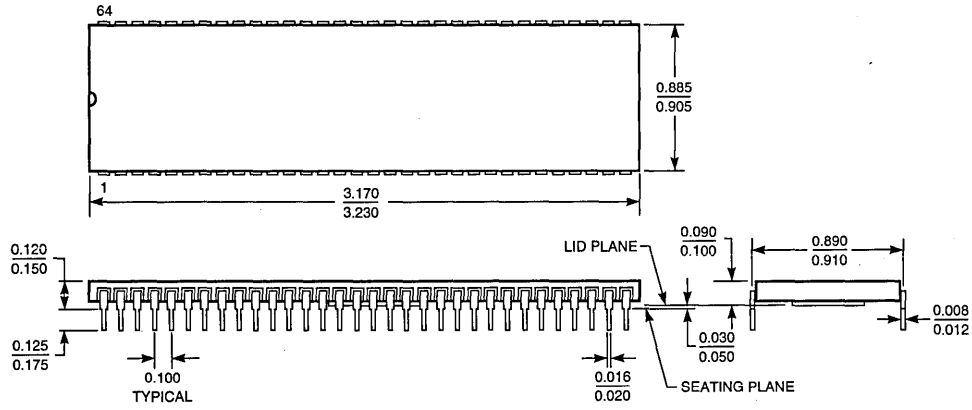
11

SIDEBRAZE, HERMETIC DIP (ORDERING CODE: D, H)

D5 — 48-pin, 0.6" wide

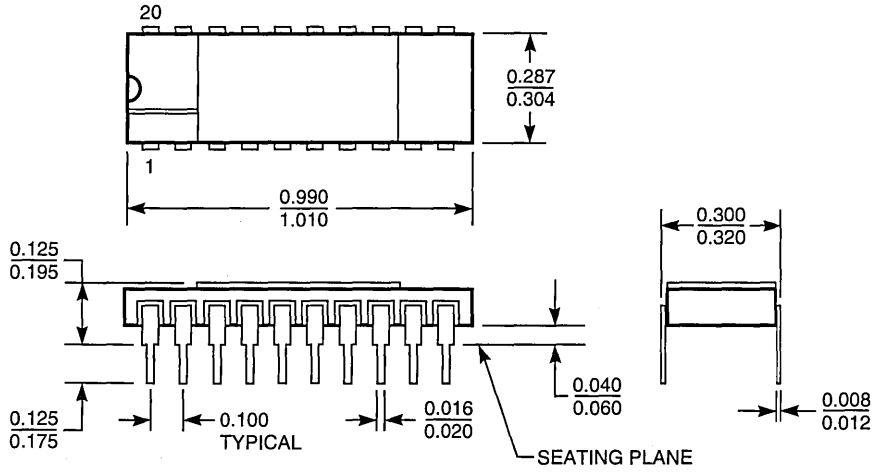


D6 — 64-pin, 0.9" wide, cavity down

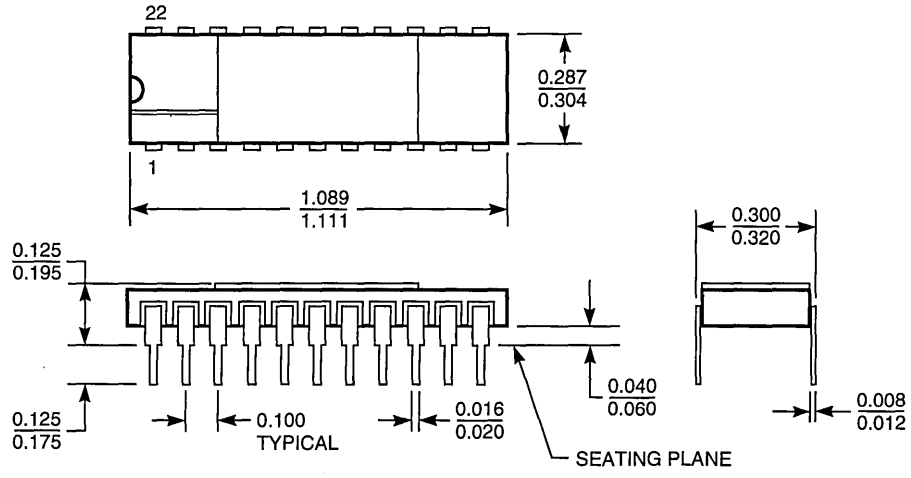


Sidebraze, Hermetic DIP (Ordering Code: D, H)

D7 — 20-pin, 0.3" wide



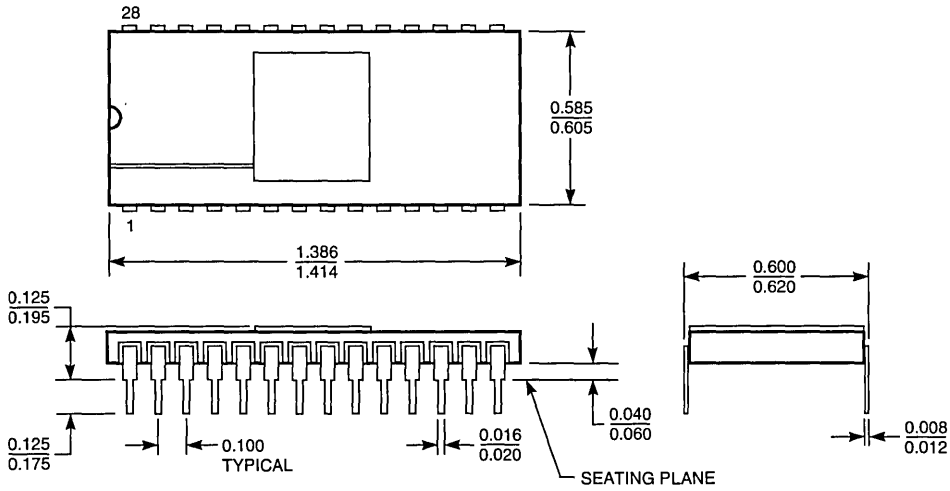
D8 — 22-pin, 0.3" wide



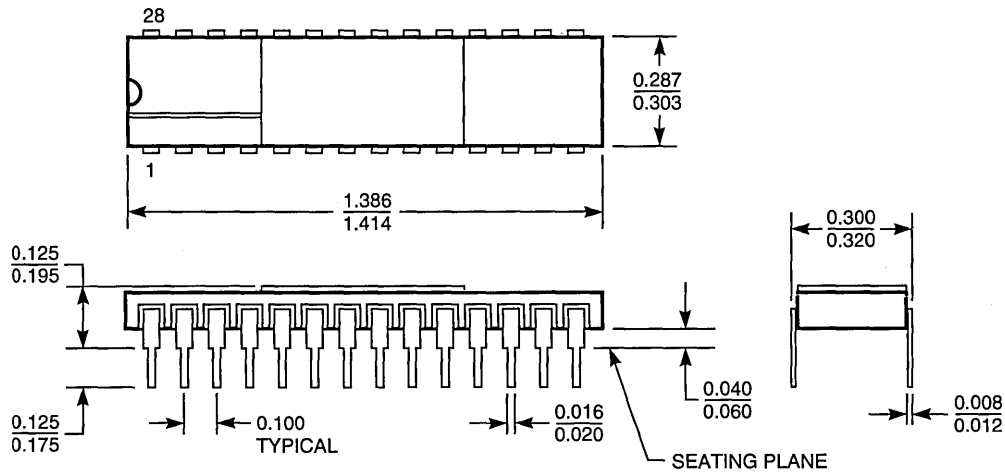
11

SIDEBRAZE, HERMETIC DIP (ORDERING CODE: D, H)

D9 — 28-pin, 0.6" wide

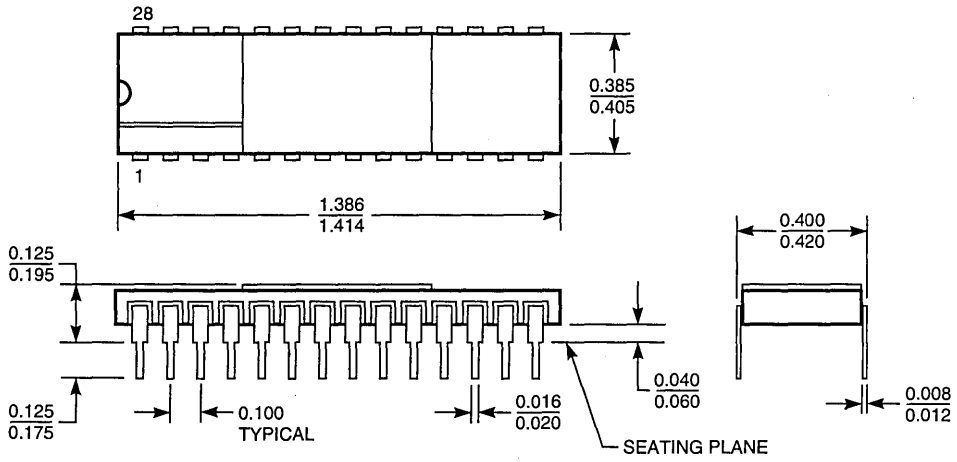


D10 — 28-pin, 0.3" wide

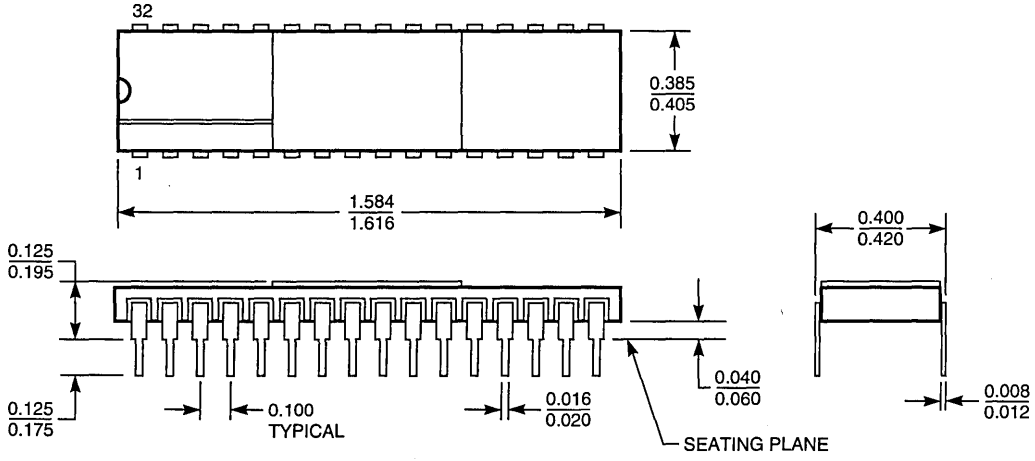


SIDEBRAZE, HERMETIC DIP (ORDERING CODE: D, H)

D11 — 28-pin, 0.4" wide



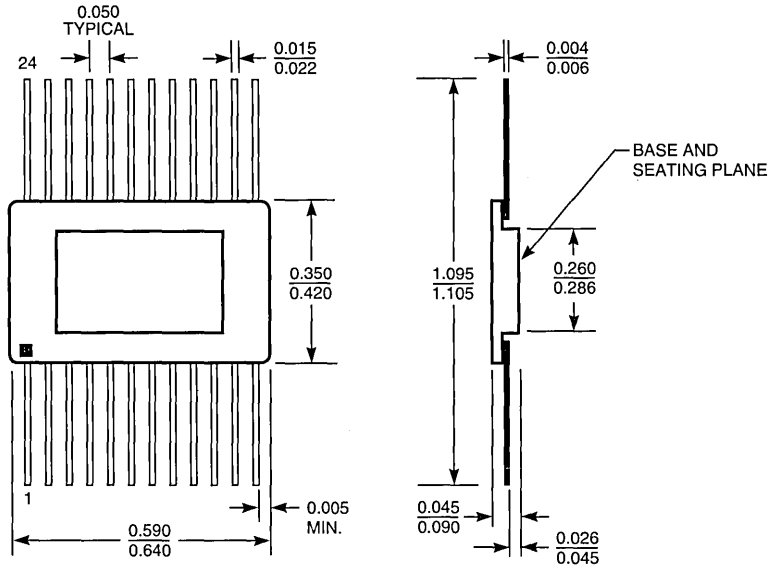
D12 — 32-pin, 0.4" wide



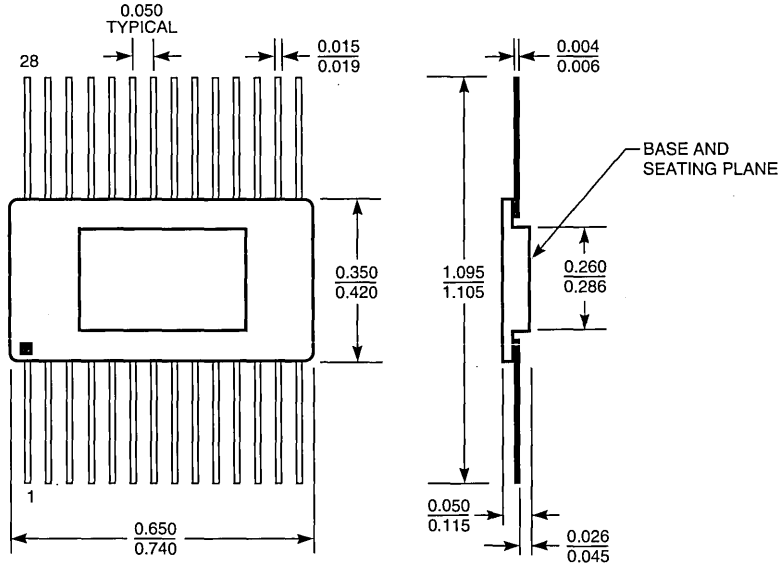
11

FLATPACK (ORDERING CODE: F)

F1 — 24-pin

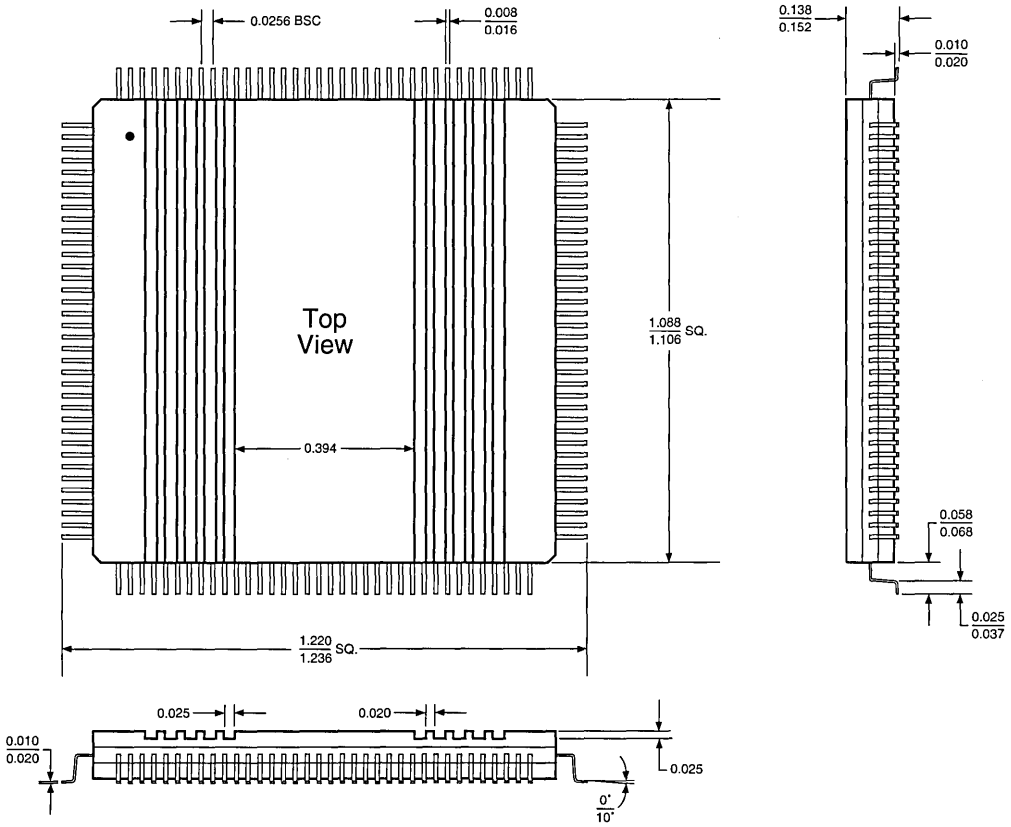


F2 — 28-pin



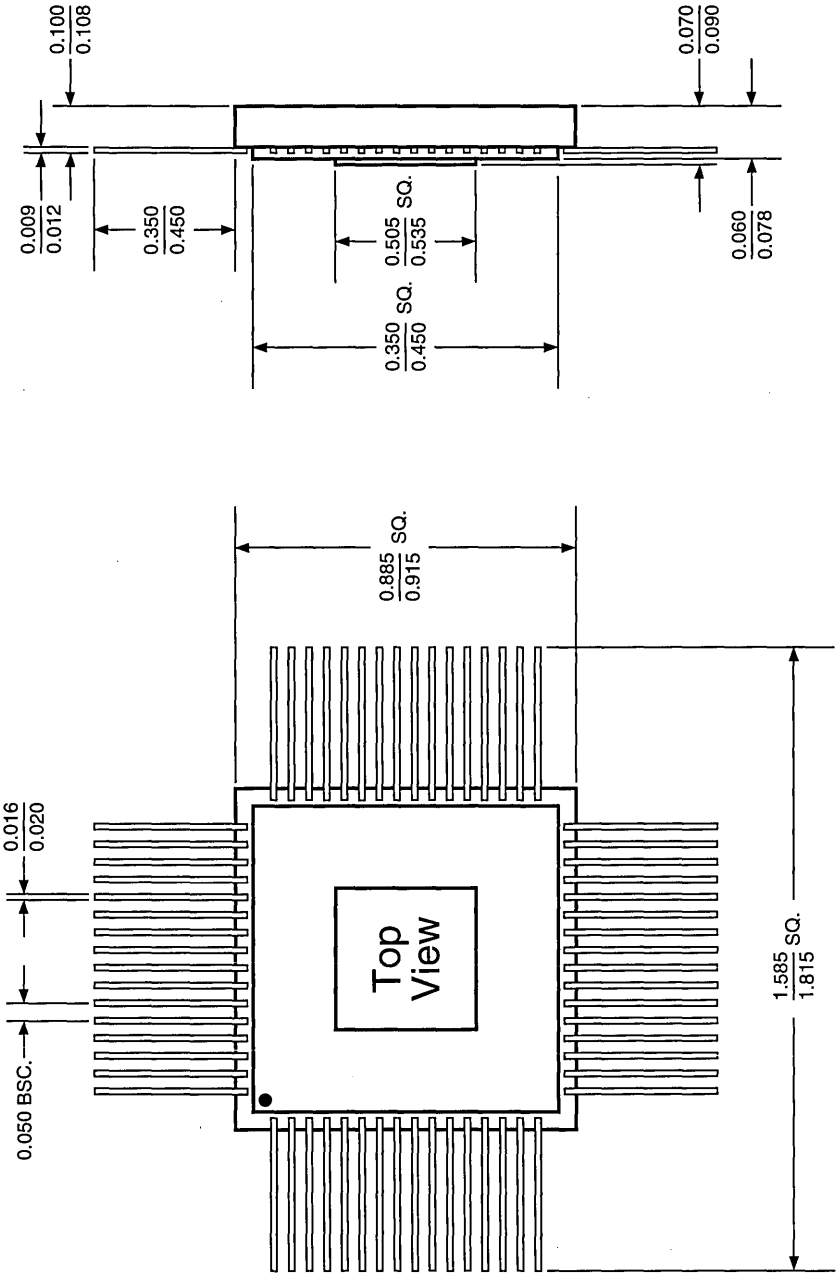
FLATPACK (ORDERING CODE: F)

F3 — 144-pin



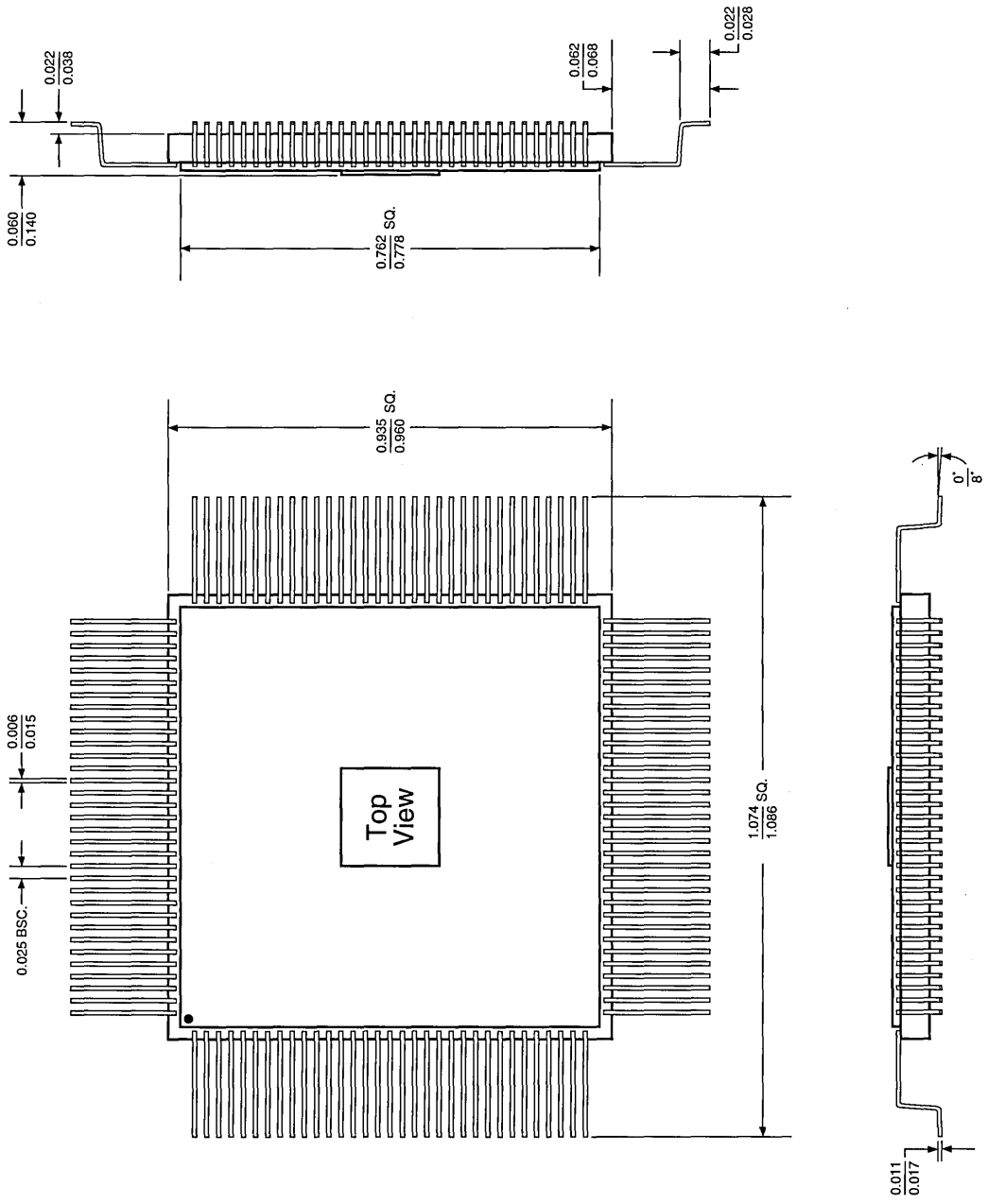
FLATPACK (ORDERING CODE: F)

F4 — 64-pin



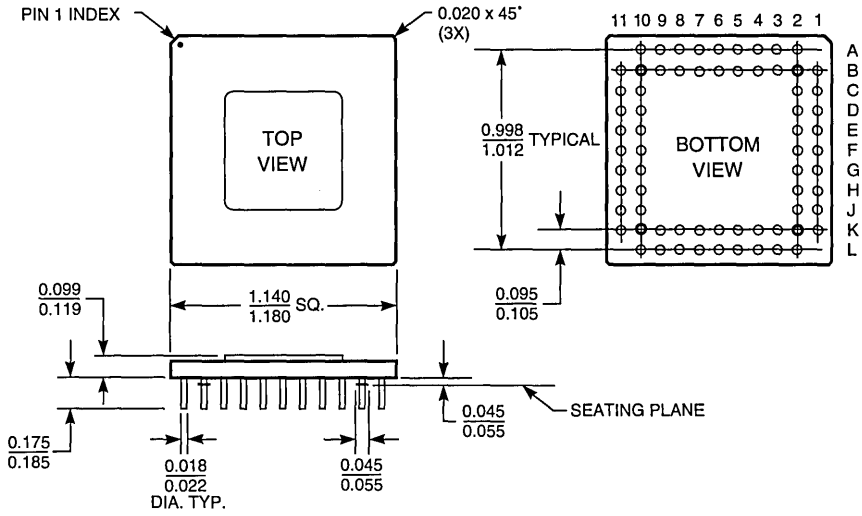
FLATPACK (ORDERING CODE: F)

F5 — 132-pin

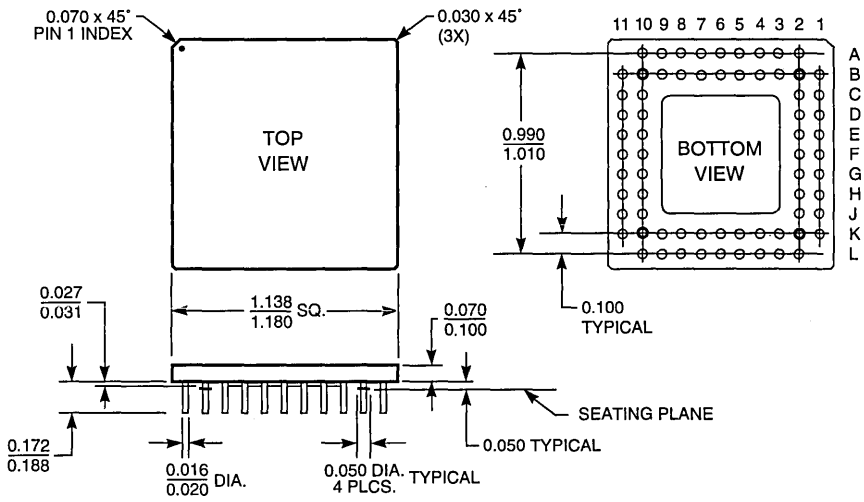


CERAMIC PGA (ORDERING CODE: G)

G1 — 68-pin, cavity up

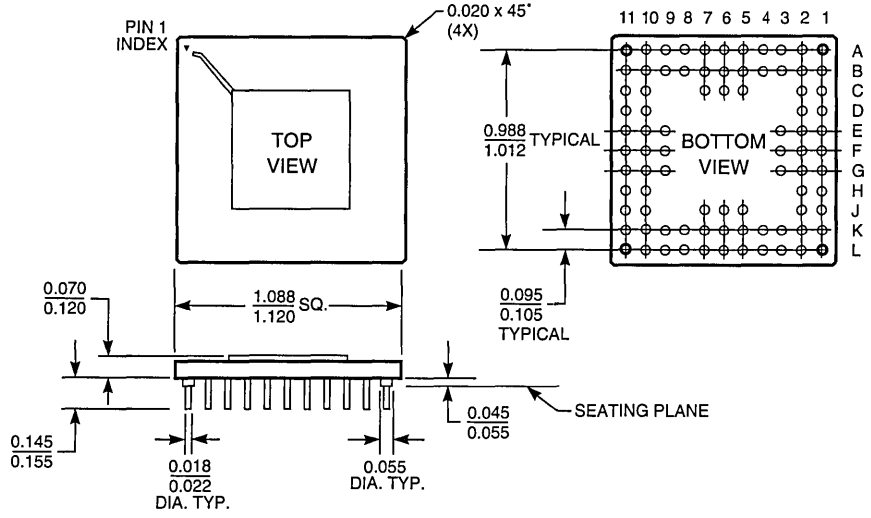


G2 — 68-pin, cavity down

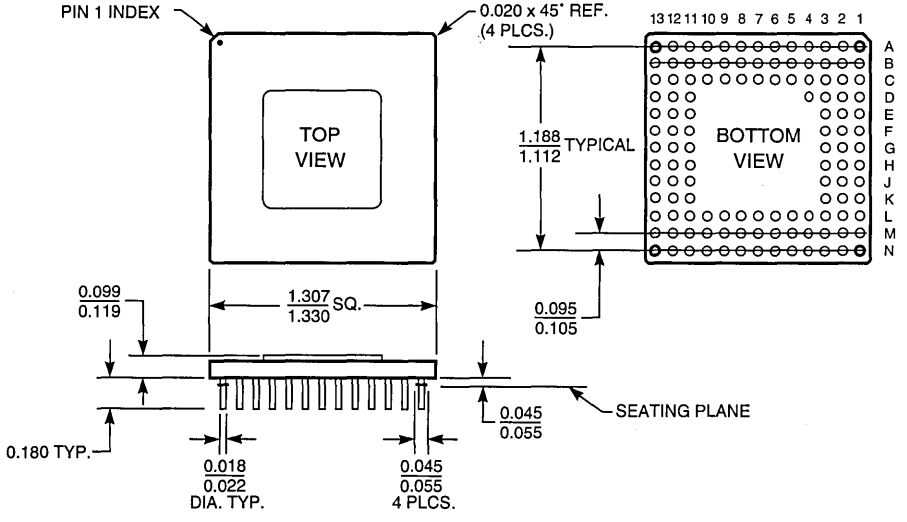


CERAMIC PGA (ORDERING CODE: G)

G3 — 84-pin



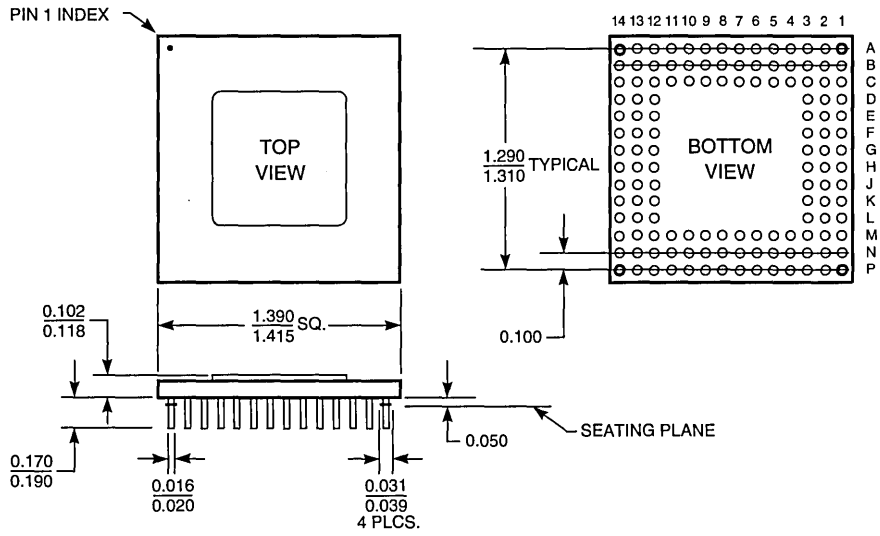
G4 — 120-pin



11

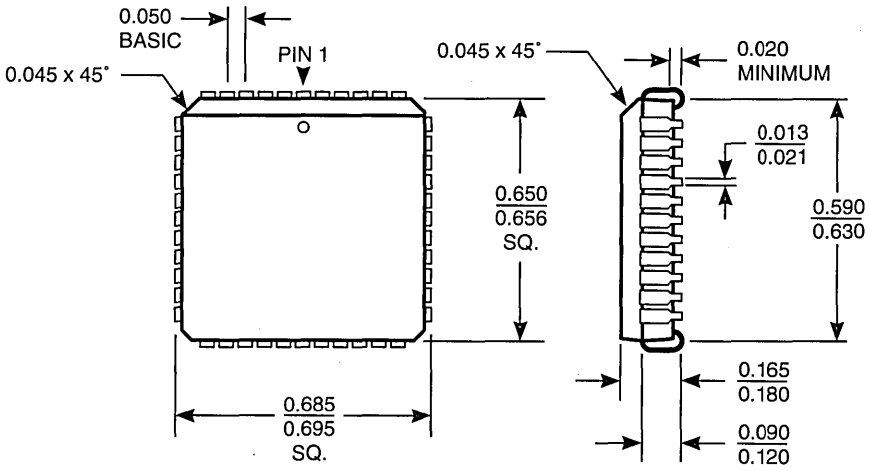
Ceramic PGA (Ordering Code: G)

G5 — 132-pin



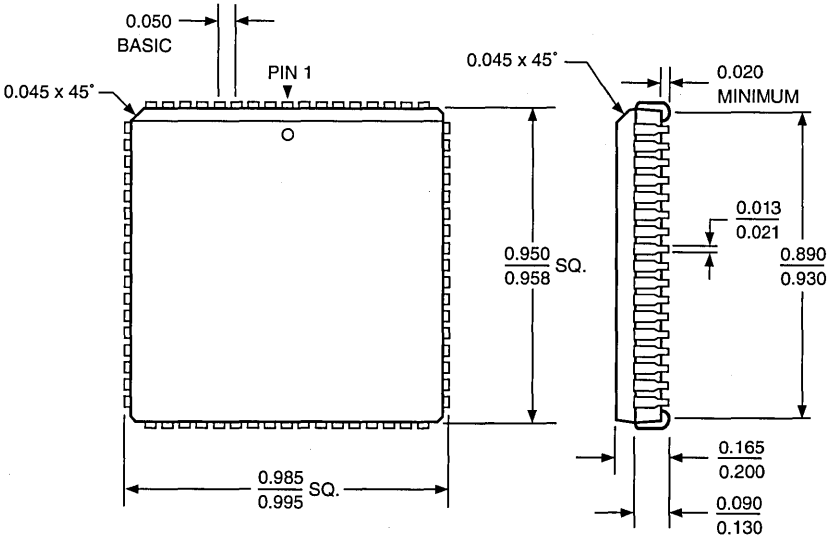
Plastic J-Lead Chip Carrier (Ordering Code: J)

J1 — 44-pin, 0.690" x 0.690"



Reference: JEDEC - MO-047-AC
JEDEC - MS-018-AC

J2 — 68-pin, 0.990" x 0.990"

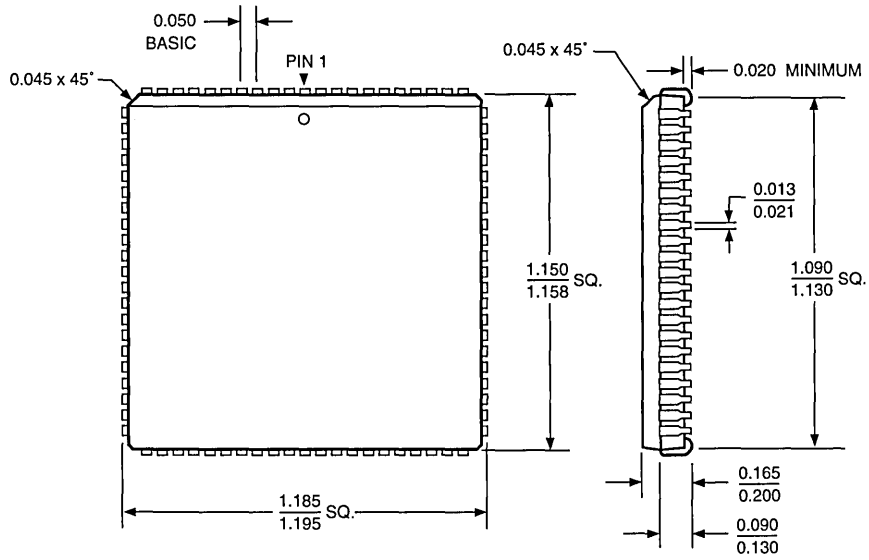


Reference: JEDEC - MO-047-AE

11

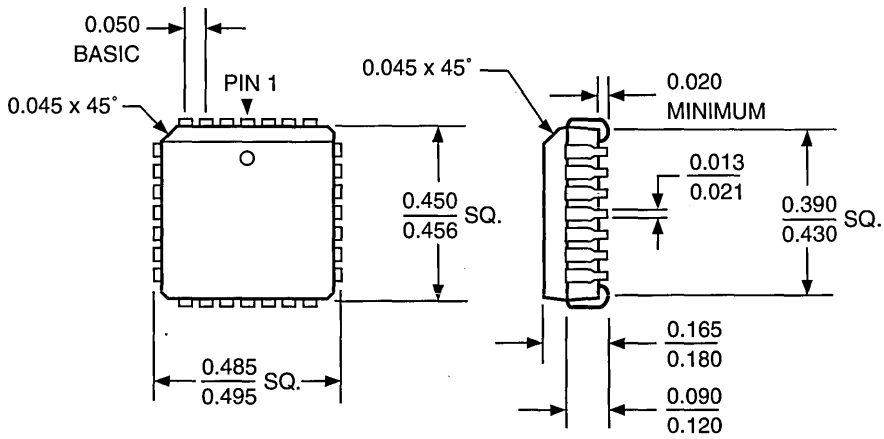
Plastic J-Lead Chip Carrier (Ordering Code: J)

J3 — 84-pin, 1.190" x 1.190"



Reference: JEDEC - MO-047-AF

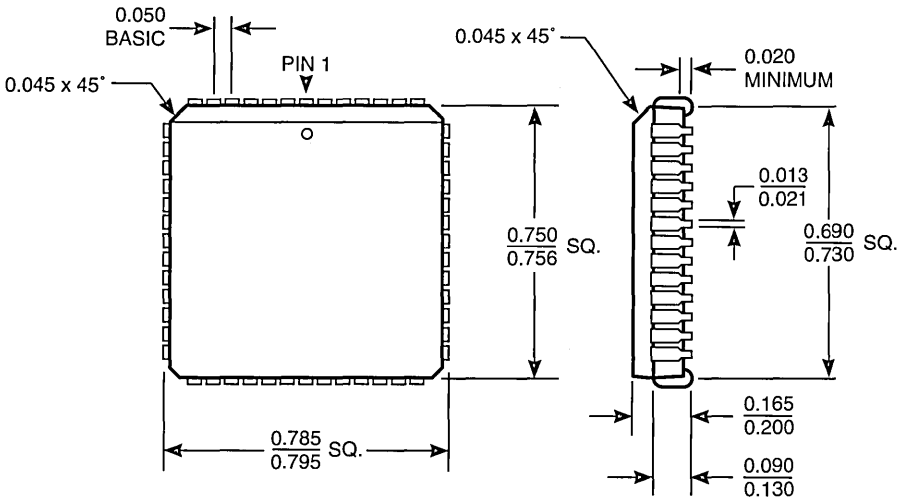
J4 — 28-pin, 0.490" x 0.490"



Reference: JEDEC - MO-047-AB
JEDEC - MS-018-AB

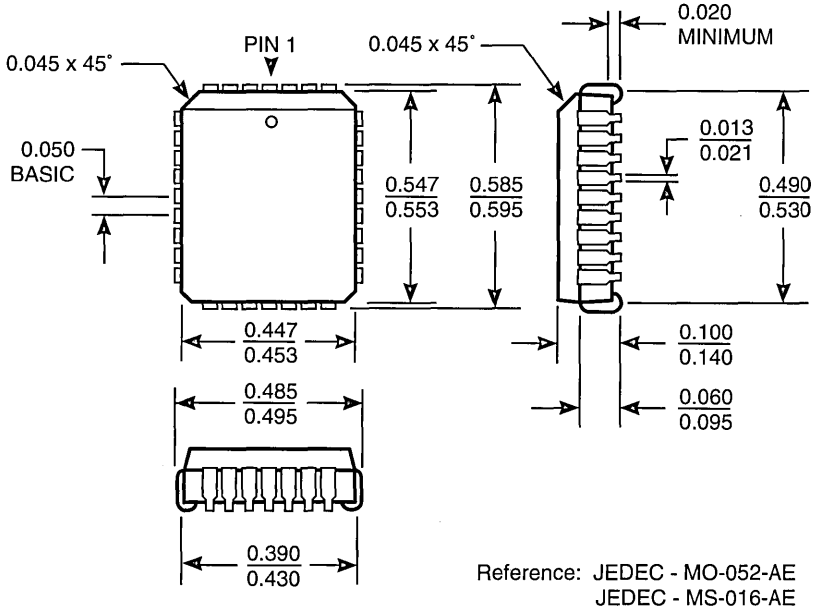
Plastic J-Lead Chip Carrier (Ordering Code: J)

J5 — 52-pin, 0.790" x 0.790"



Reference: JEDEC - MO-047-AD

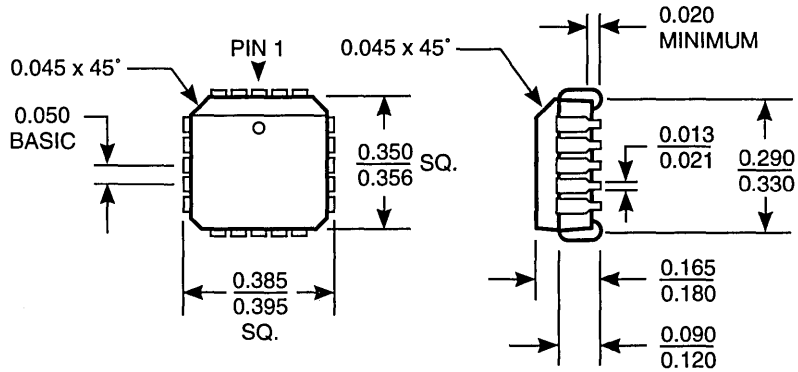
J6 — 32-pin, 0.490" x 0.590"



Reference: JEDEC - MO-052-AE
JEDEC - MS-016-AE

Plastic J-Lead Chip Carrier (Ordering Code: J)

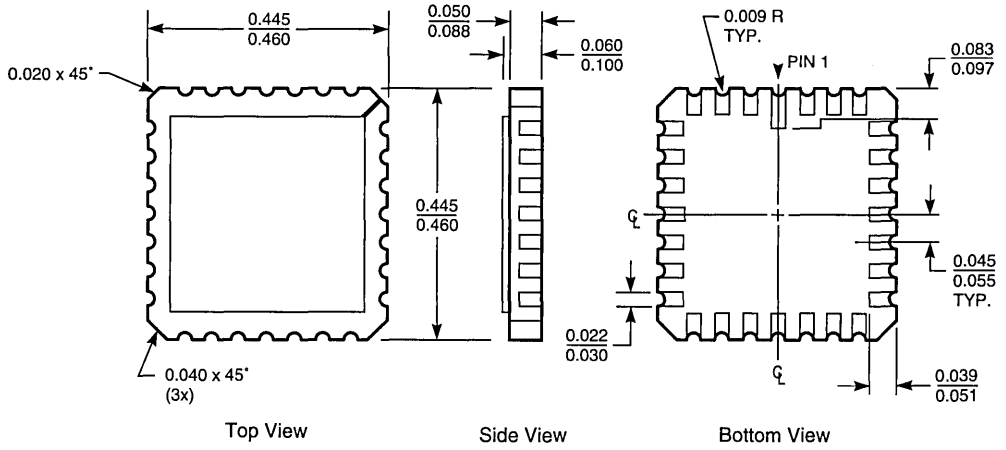
J7 — 20-pin, 0.390" x 0.390"



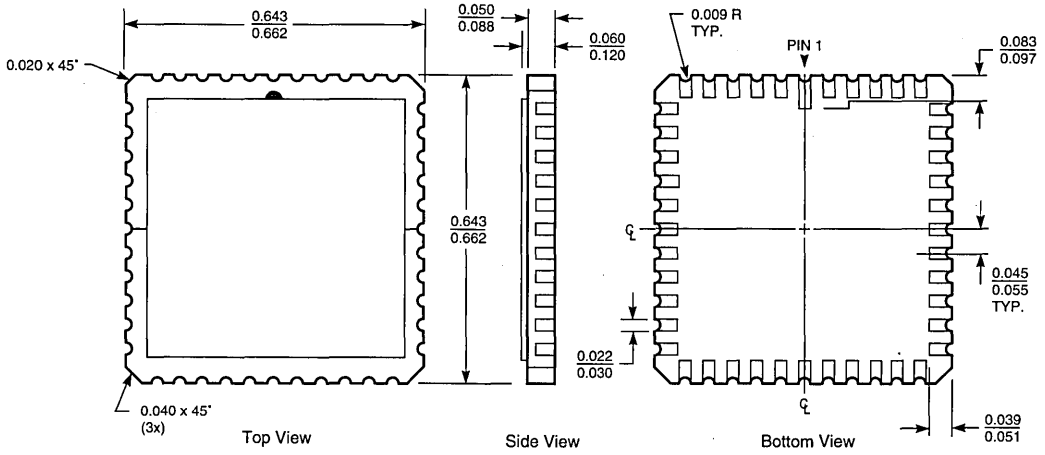
Reference: JEDEC - MO-047-AA
JEDEC - MS-018-AA

Ceramic Leadless Chip Carrier (Ordering Code: K, T)

K1 — 28-pin, 0.450" x 0.450"



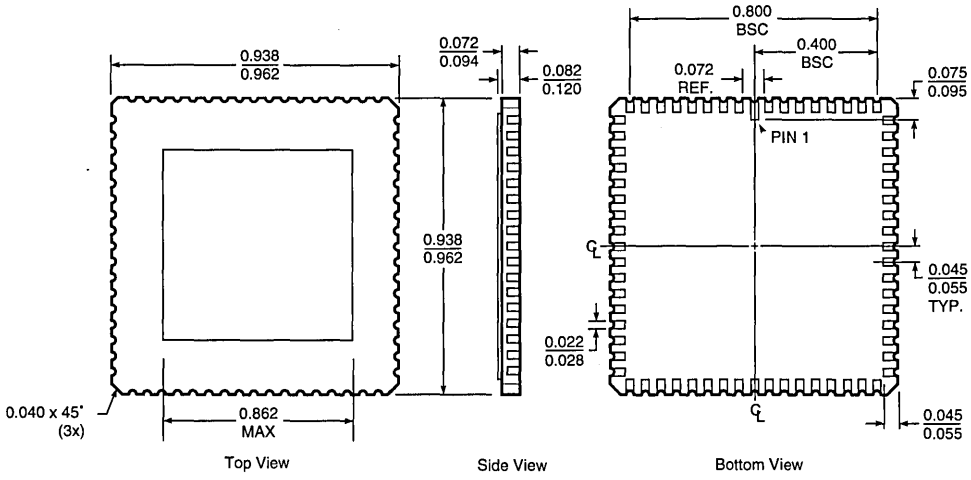
K2 — 44-pin, 0.650" x 0.650"



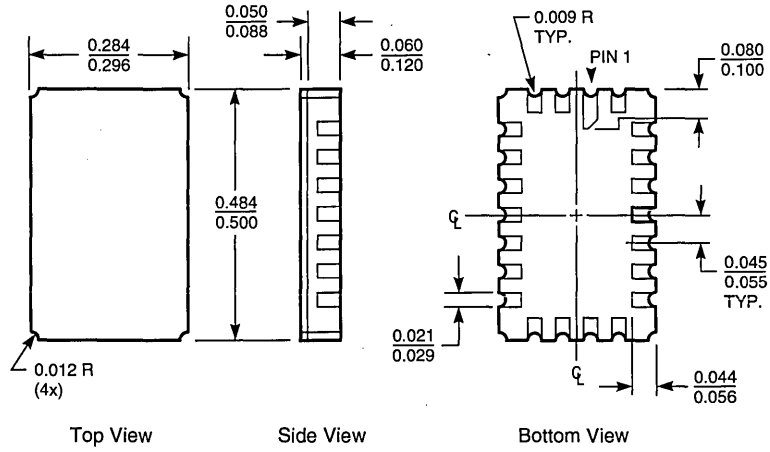
11

Ceramic Leadless Chip Carrier (Ordering Code: K, T)

K3 — 68-pin, 0.950" x 0.950"

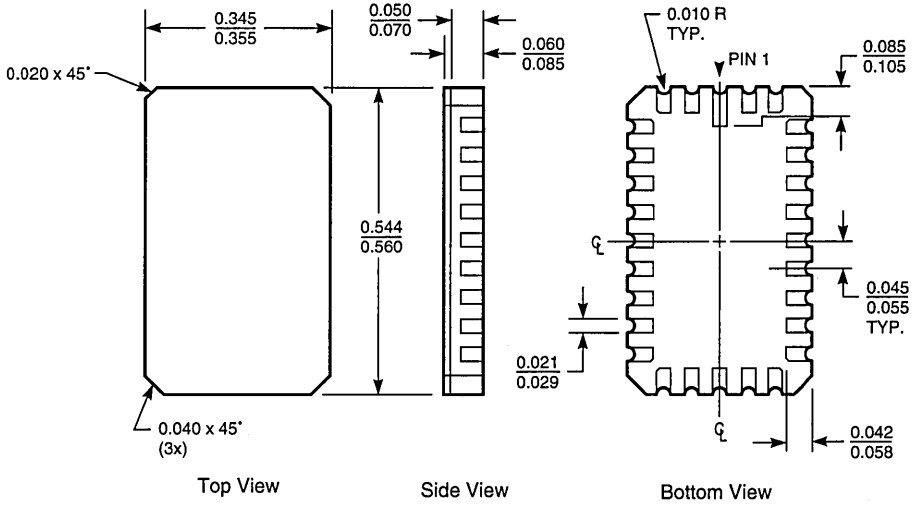


K4 — 22-pin, 0.290" x 0.490"

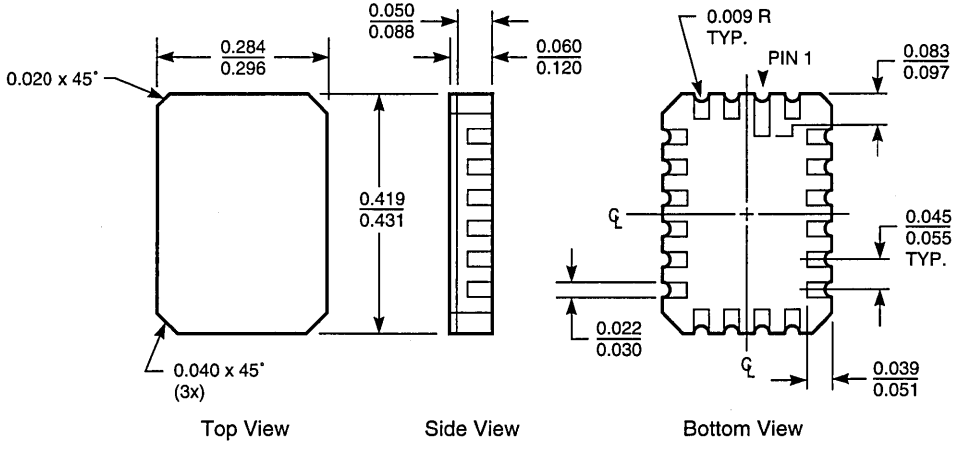


Ceramic Leadless Chip Carrier (Ordering Code: K, T)

K5 — 28-pin, 0.350" x 0.550"



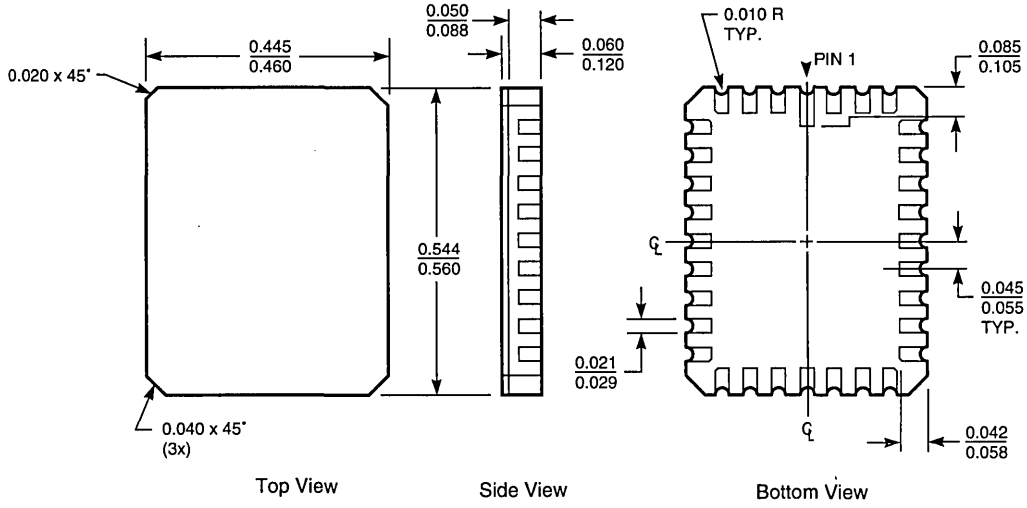
K6 — 20-pin, 0.290" x 0.425"



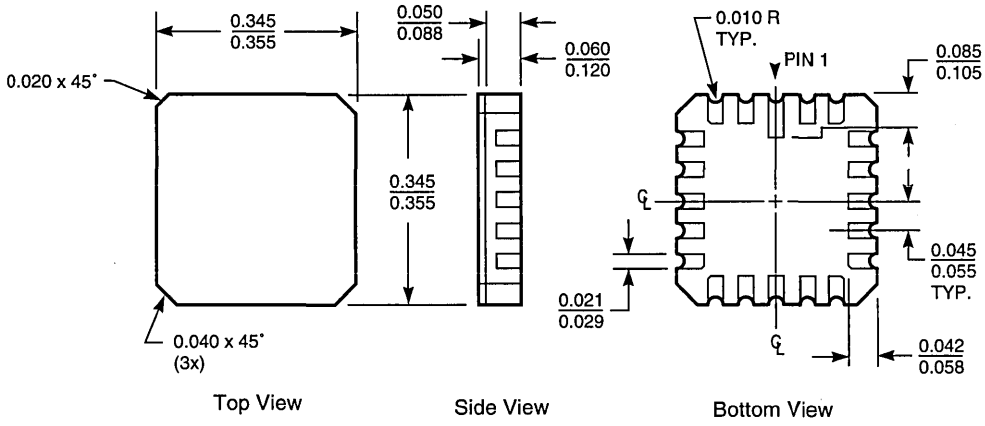
11

Ceramic Leadless Chip Carrier (Ordering Code: K, T)

K7 — 32-pin, 0.450" x 0.550"

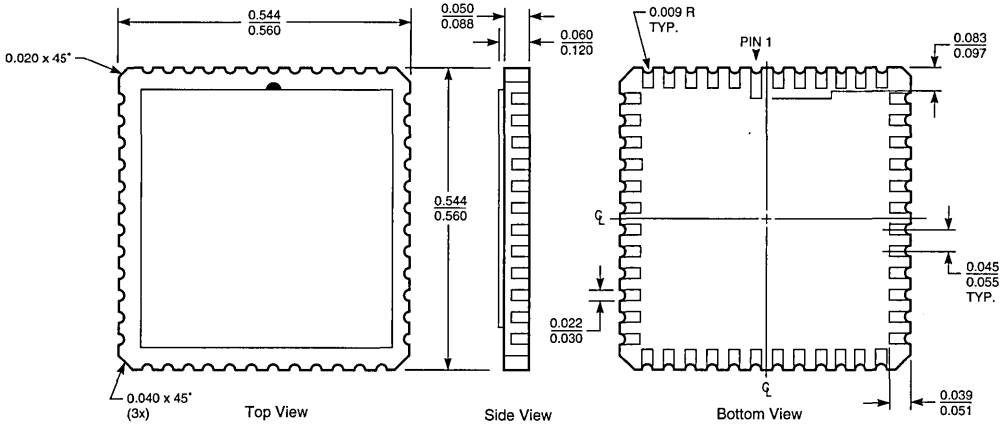


K8 — 20-pin, 0.350" x 0.350"

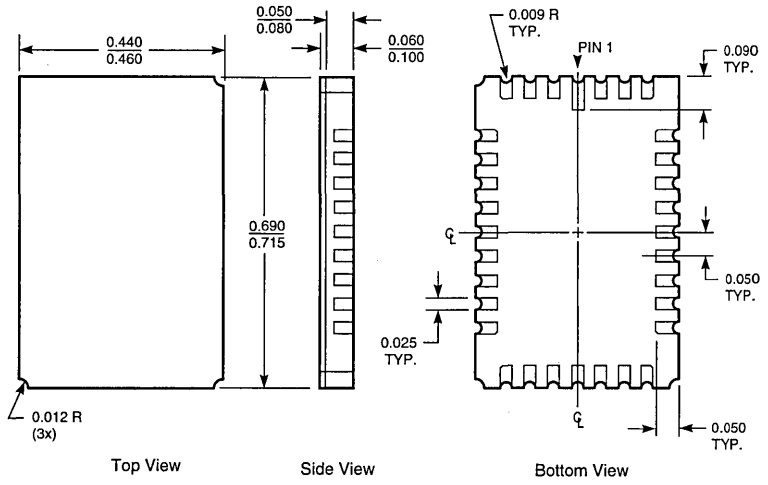


Ceramic Leadless Chip Carrier (Ordering Code: K, T)

K9 — 48-pin, 0.550" x 0.550"



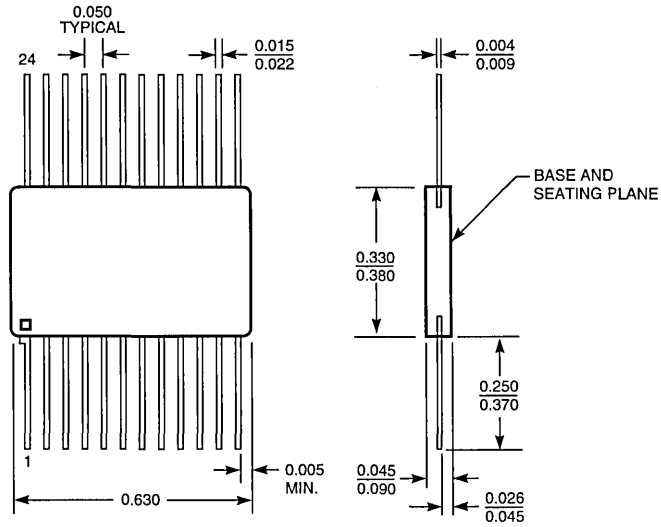
K10 — 32-pin, 0.450" x 0.700"



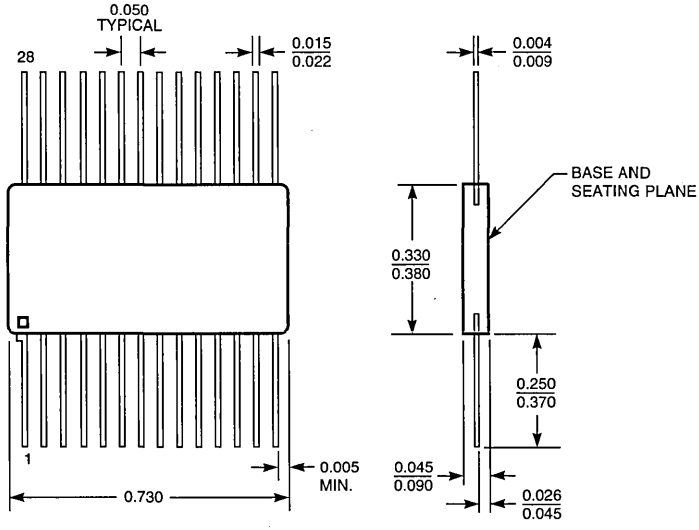
11

Ceramic Flatpack (Ordering Code: M)

M1 — 24-pin

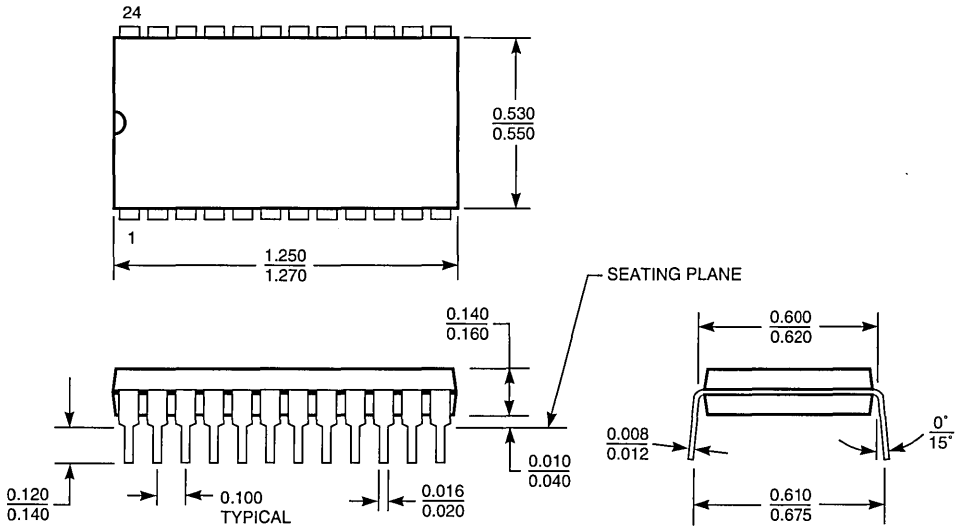


M2 — 28-pin

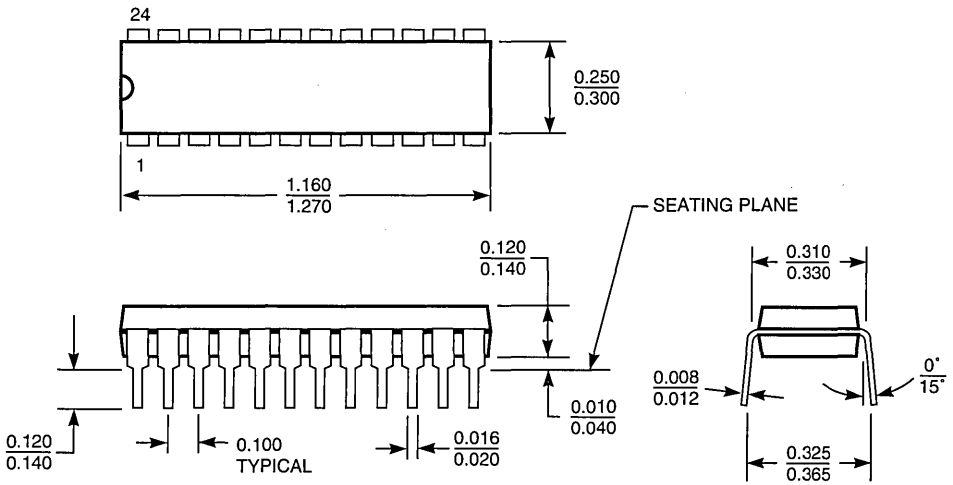


Plastic DIP (Ordering Code: P, N)

P1 — 24-pin, 0.6" wide



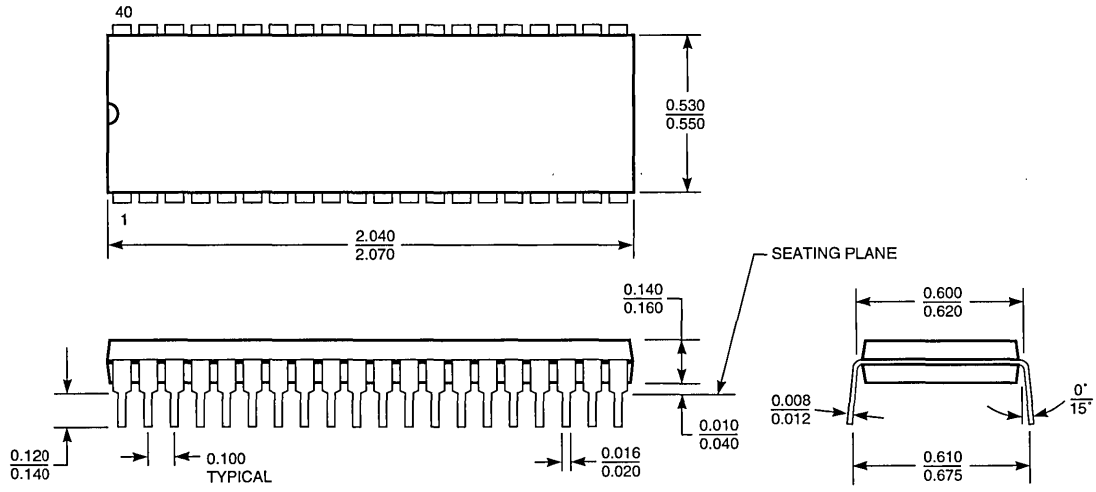
P2 — 24-pin, 0.3" wide



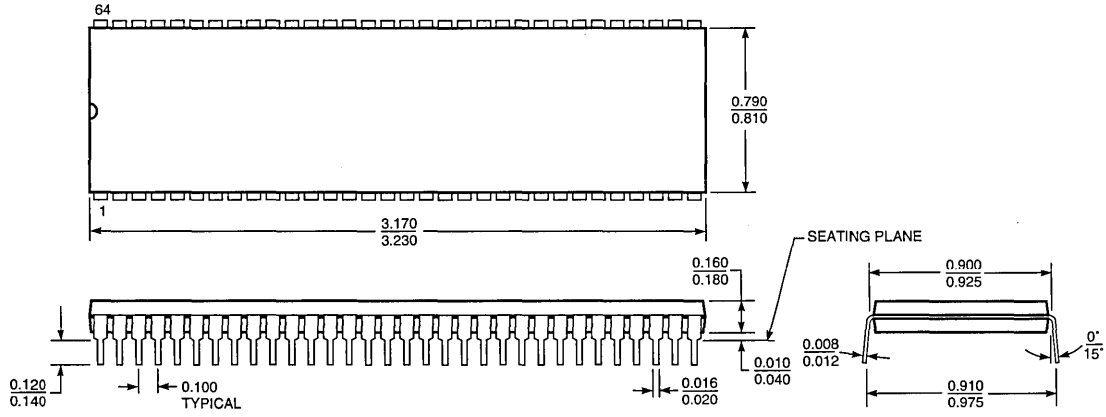
11

Plastic DIP (Ordering Code: P, N)

P3 — 40-pin, 0.6" wide

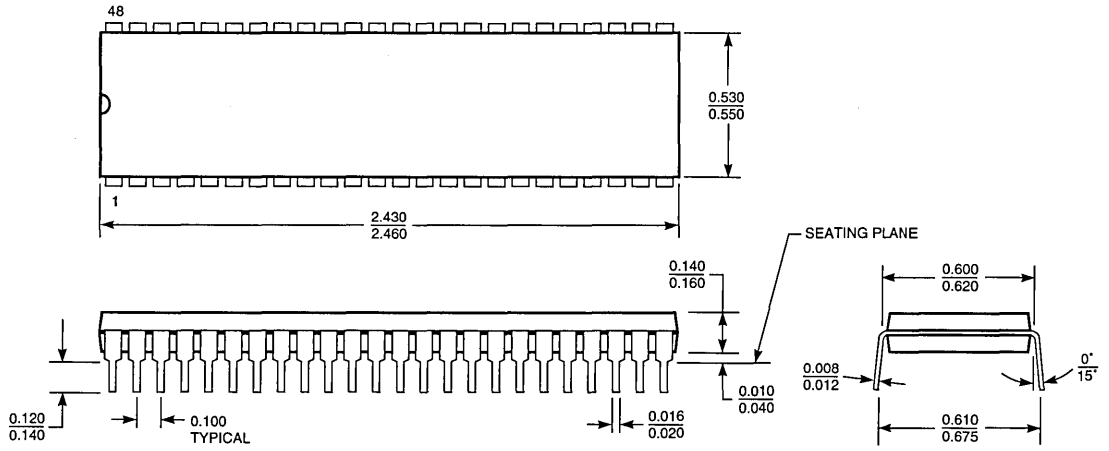


P4 — 64-pin, 0.9" wide

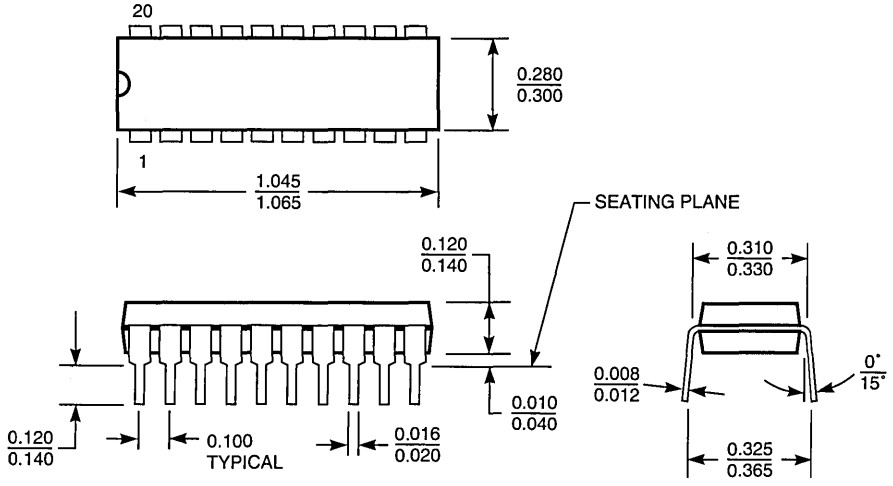


PLASTIC DIP (ORDERING CODE: P, N)

P5 — 48-pin, 0.6" wide



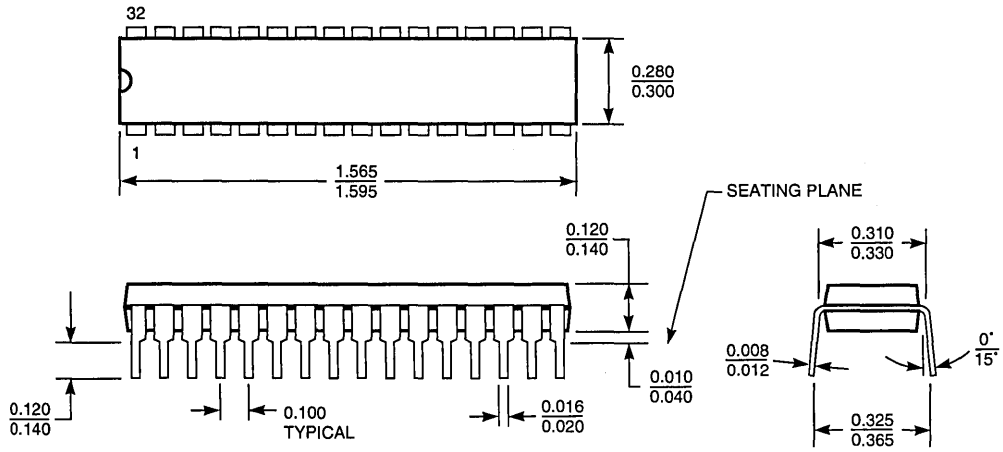
P6 — 20-pin, 0.3" wide



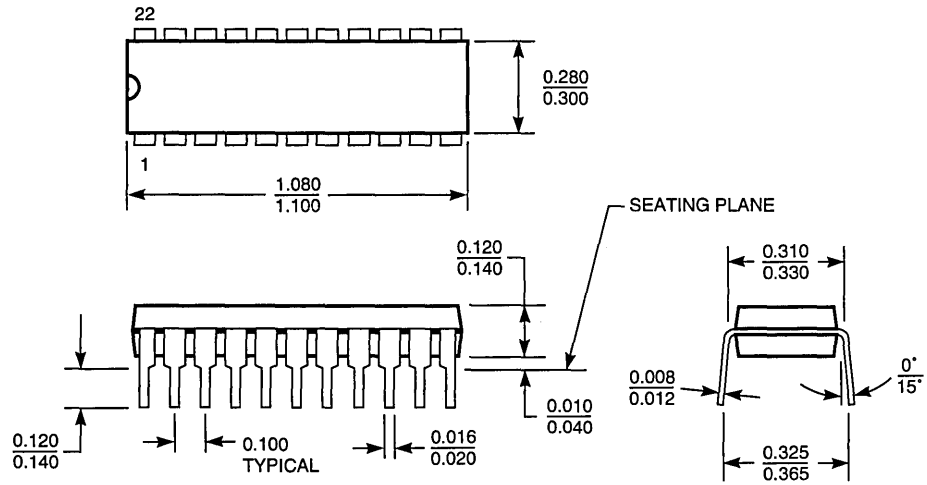
11

Plastic DIP (Ordering Code: P, N)

P7 — 32-pin, 0.3" wide

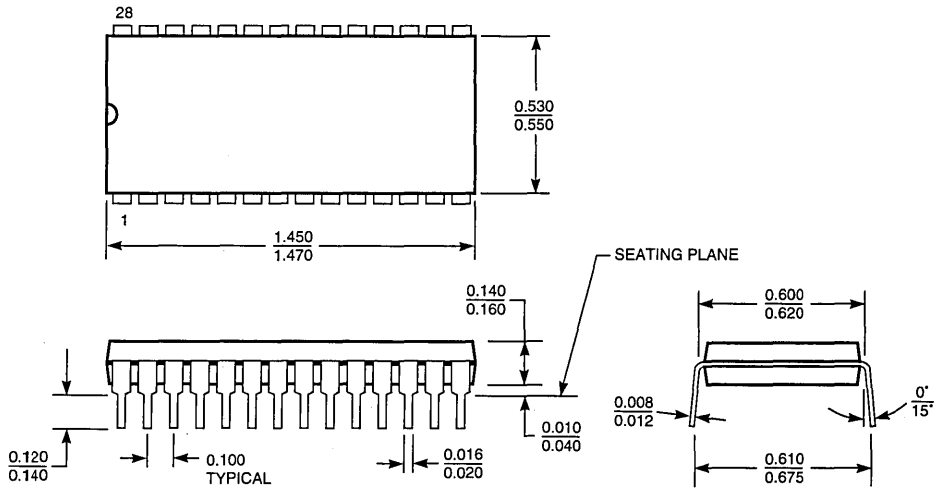


P8 — 22-pin, 0.3" wide

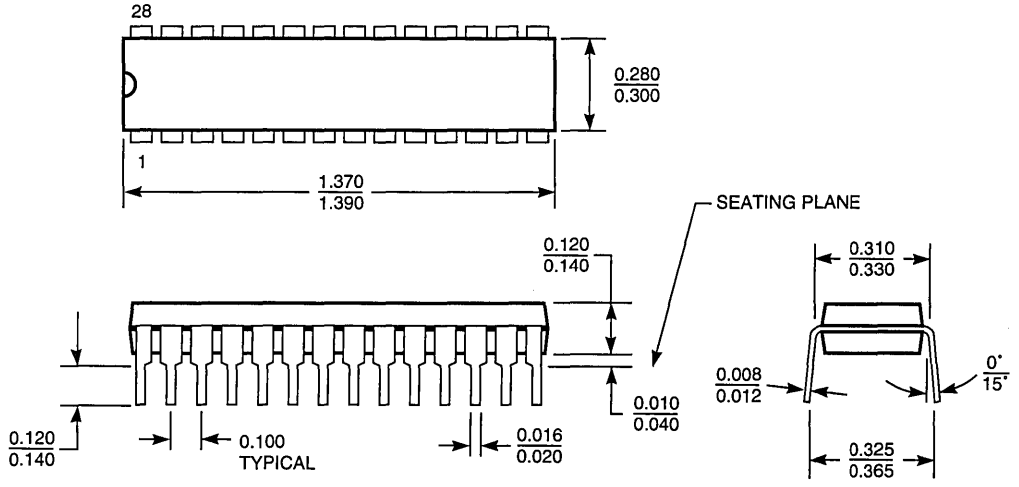


Plastic DIP (Ordering Code: P, N)

P9 — 28-pin, 0.6" wide



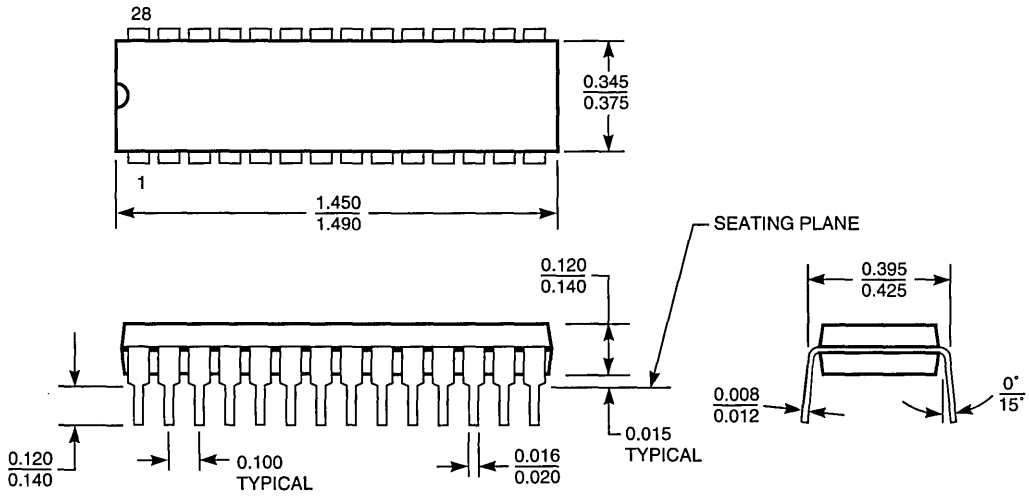
P10 — 28-pin, 0.3" wide



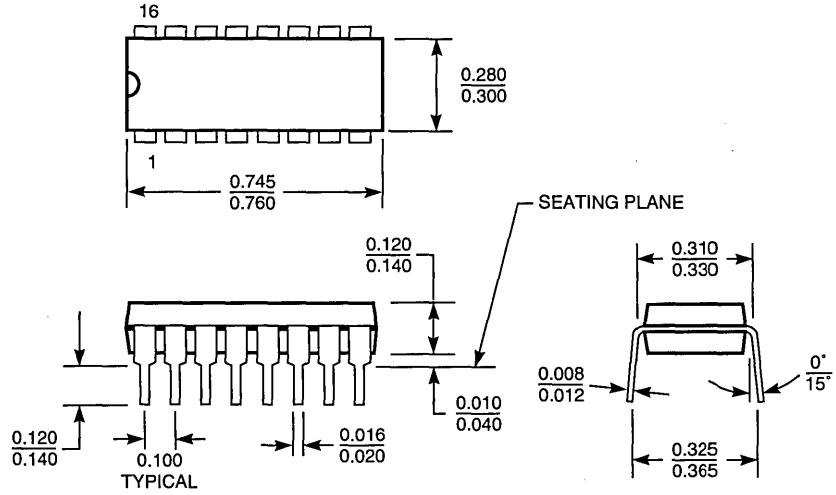
11

PLASTIC DIP (ORDERING CODE: P, N)

P11 — 28-pin, 0.4" wide

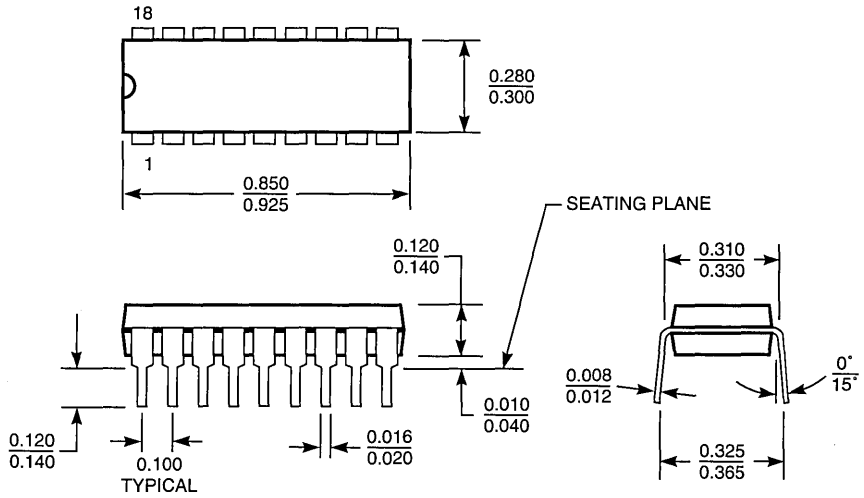


P12 — 16-pin, 0.3" wide

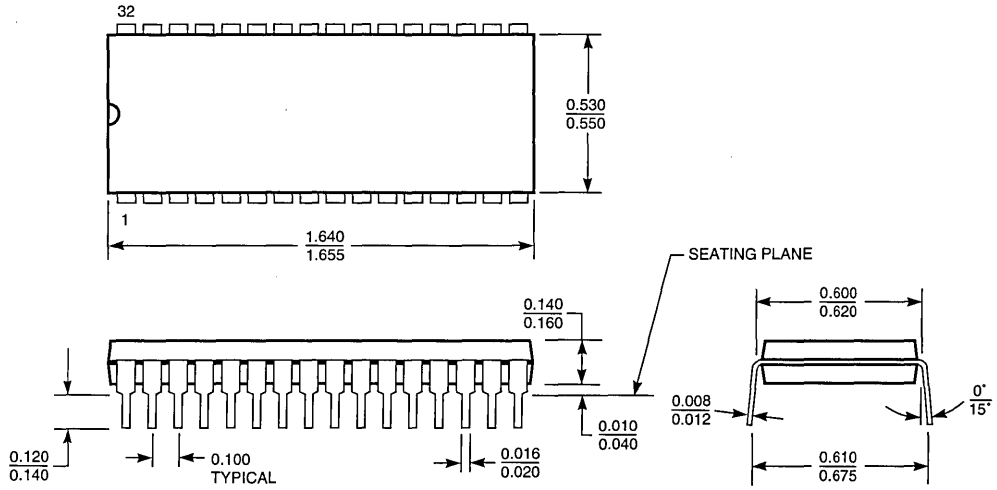


Plastic DIP (Ordering Code: P, N)

P13 — 18-pin, 0.3" wide



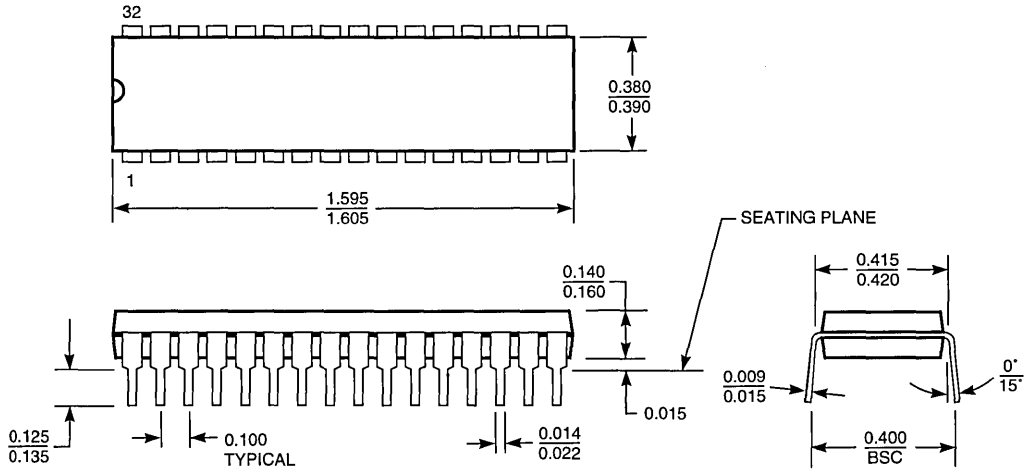
P14 — 32-pin, 0.6" wide



11

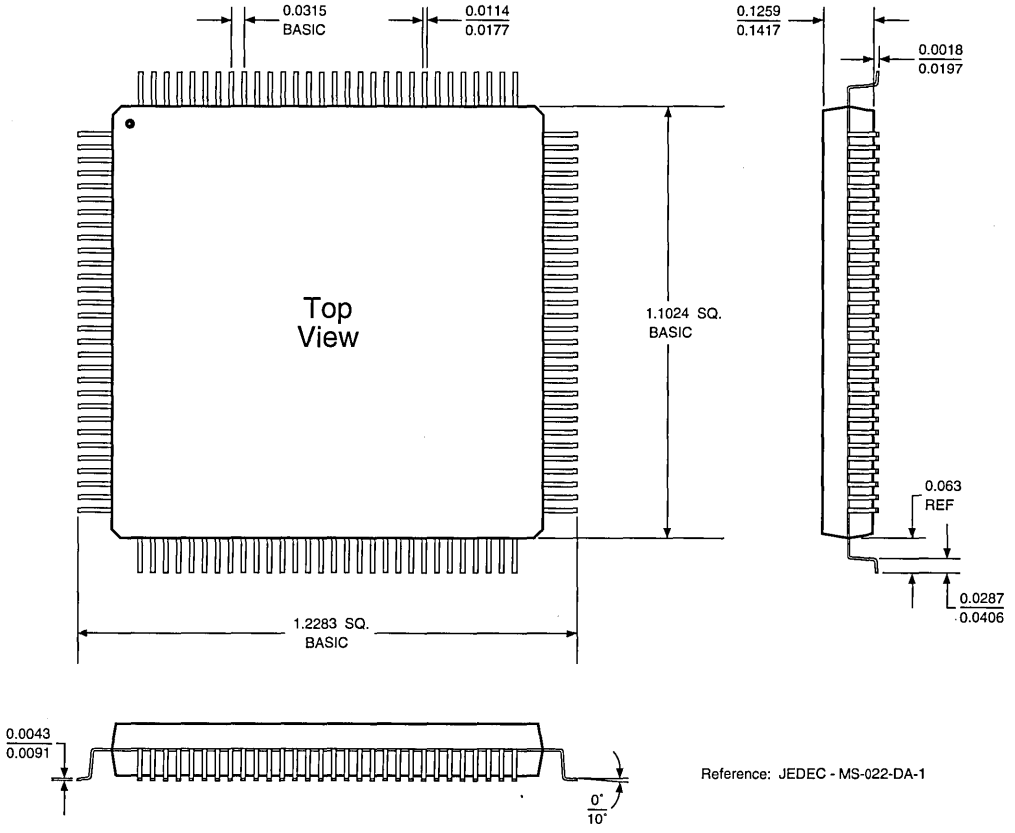
PLASTIC DIP (ORDERING CODE: P, N)

P15 — 32-pin, 0.4" wide



Plastic Quad Flatpack (Ordering Code: Q)

Q1 — 120-pin

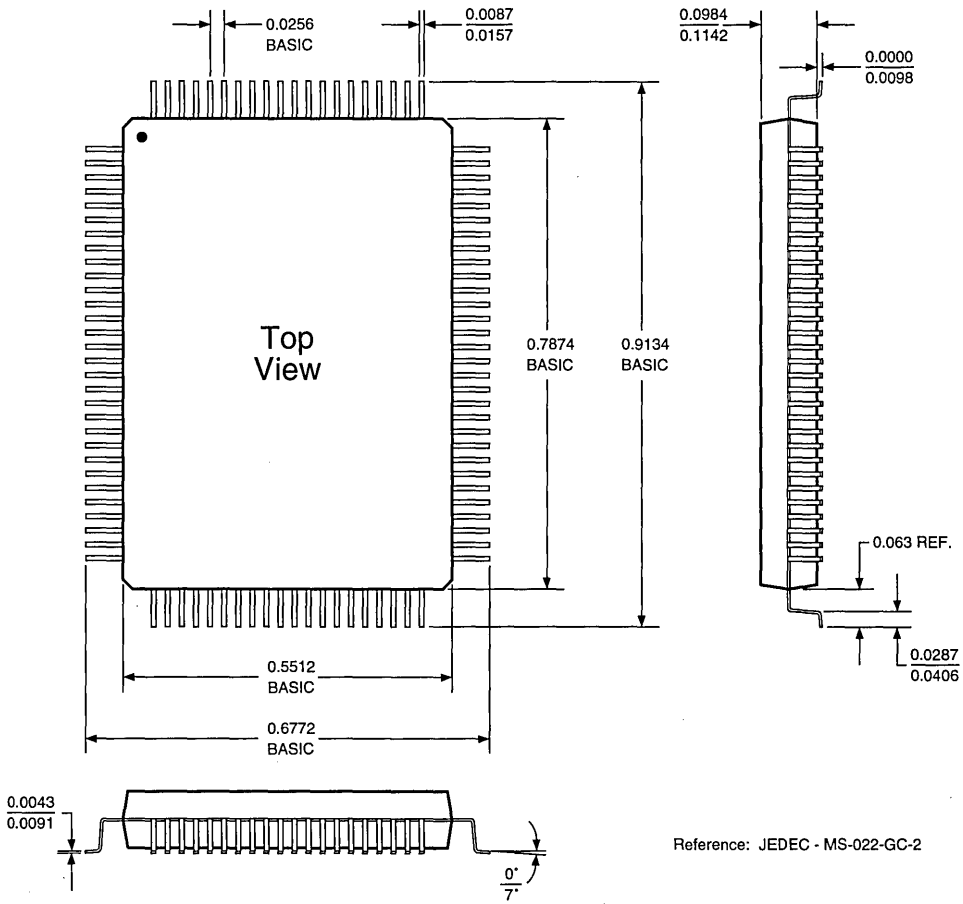


Reference: JEDEC - MS-022-DA-1

11

Plastic Quad Flatpack (Ordering Code: Q)

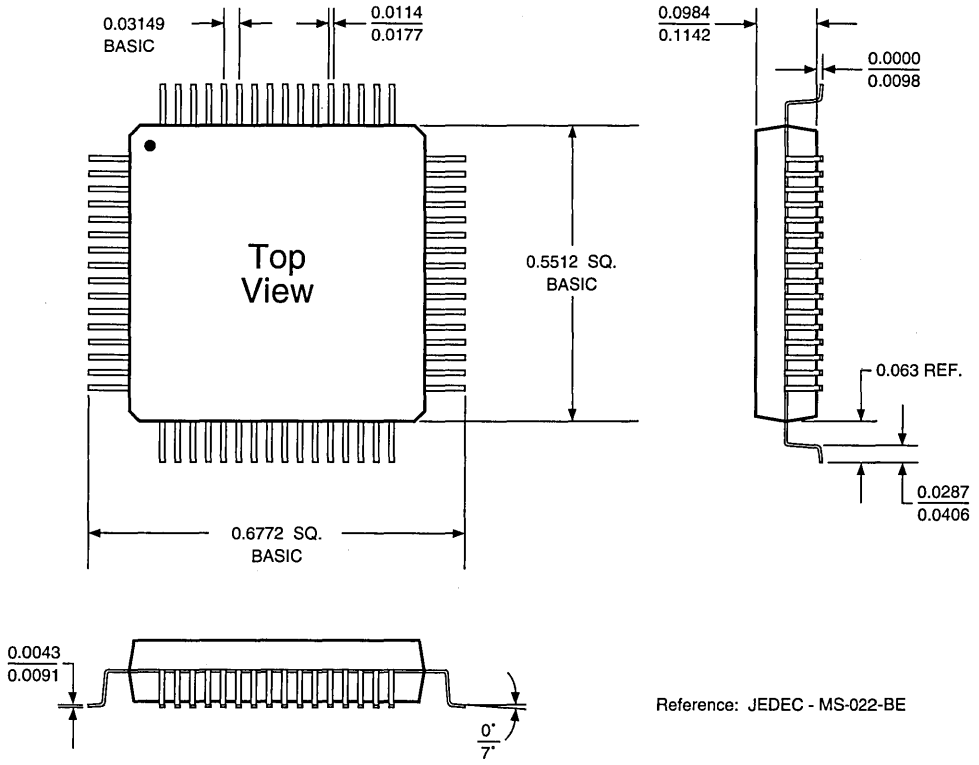
Q2 — 100-pin



Reference: JEDEC - MS-022-GC-2

Plastic Quad Flatpack (Ordering Code: Q)

Q3 — 64-pin

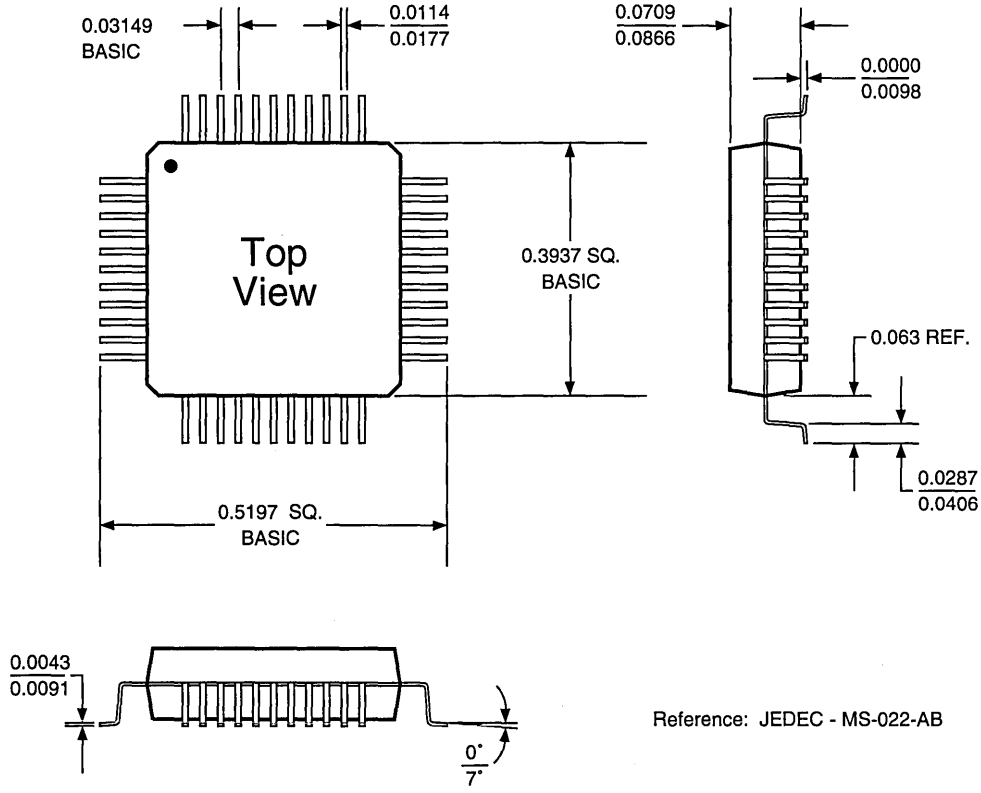


Reference: JEDEC - MS-022-BE

11

Plastic Quad Flatpack (Ordering Code: Q)

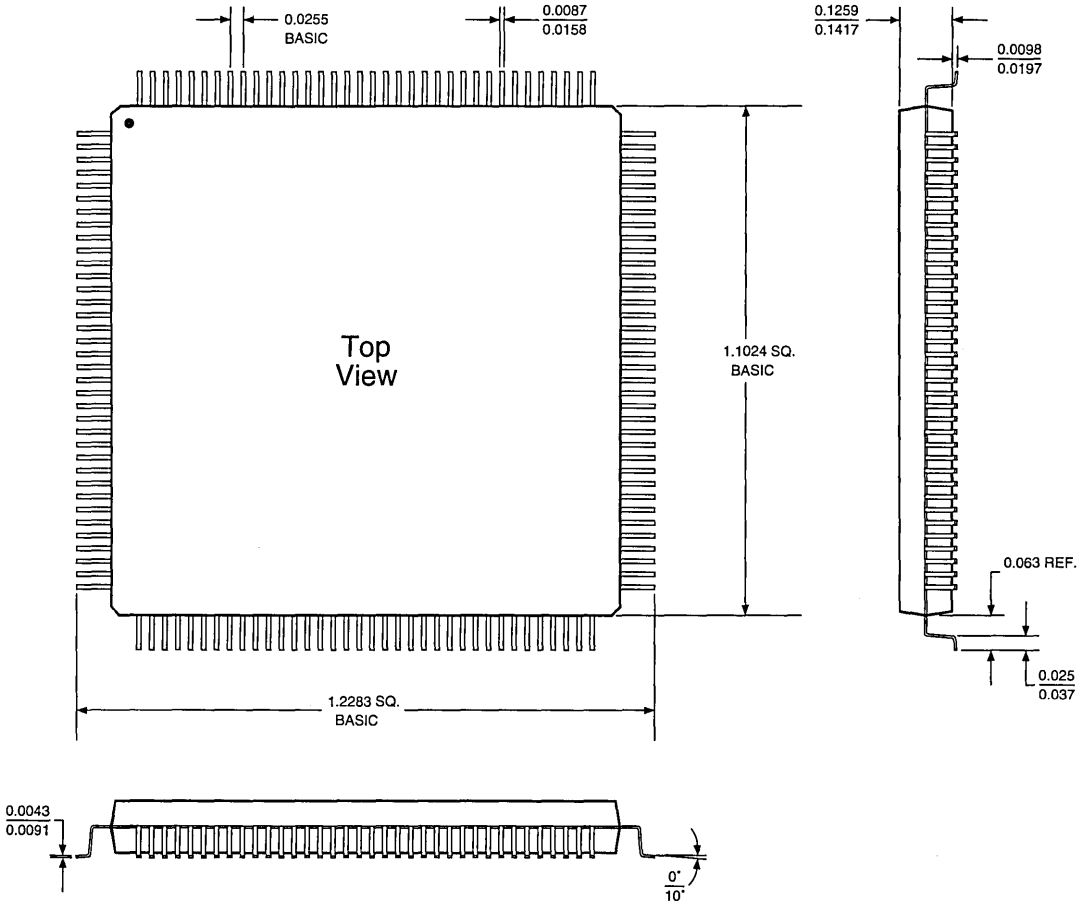
Q4 — 44-pin



Reference: JEDEC - MS-022-AB

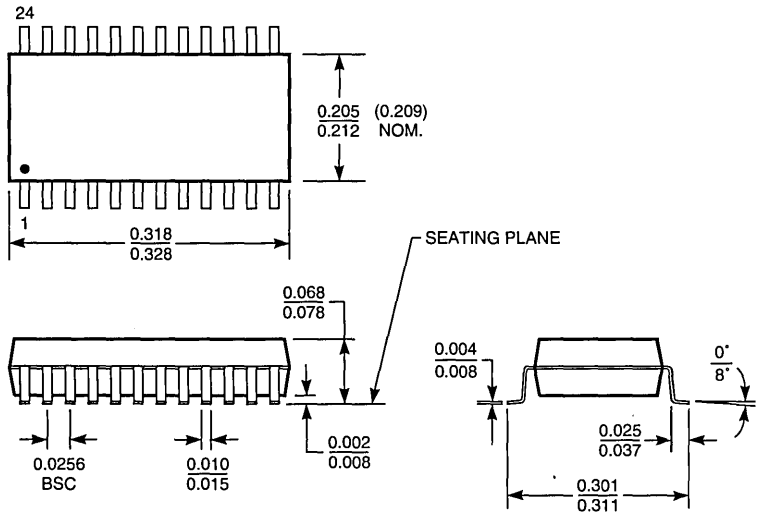
Plastic Quad Flatpack (Ordering Code: Q)

Q5 — 144-pin



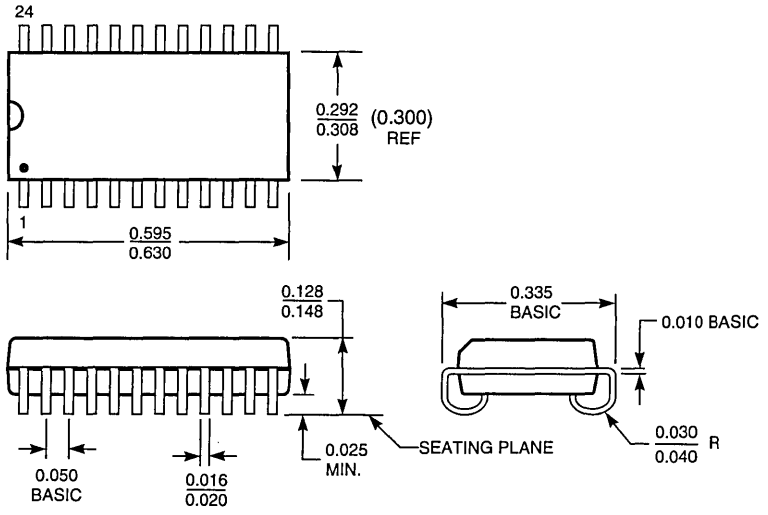
Plastic Small Scale Outline Package (Ordering Code: S)

S1 — 24-pin



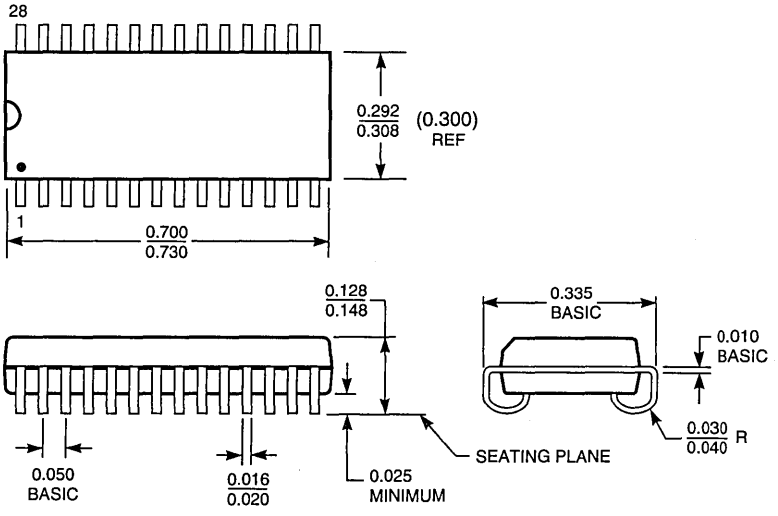
Plastic SOJ (Ordering Code: W)

W1 — 24-pin, 0.3" wide



Reference: JEDEC-MS-023-AA

W2 — 28-pin, 0.3" wide

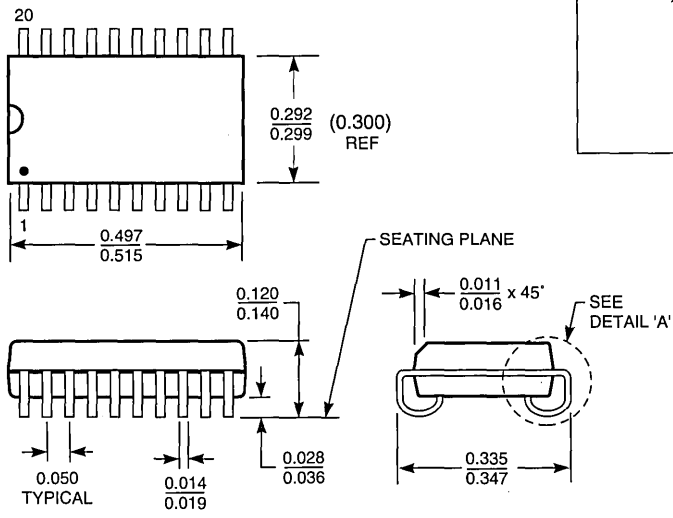


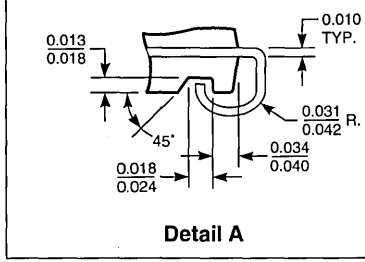
Reference: JEDEC - MS-023-AD

11

PLASTIC SOJ (ORDERING CODE: W)

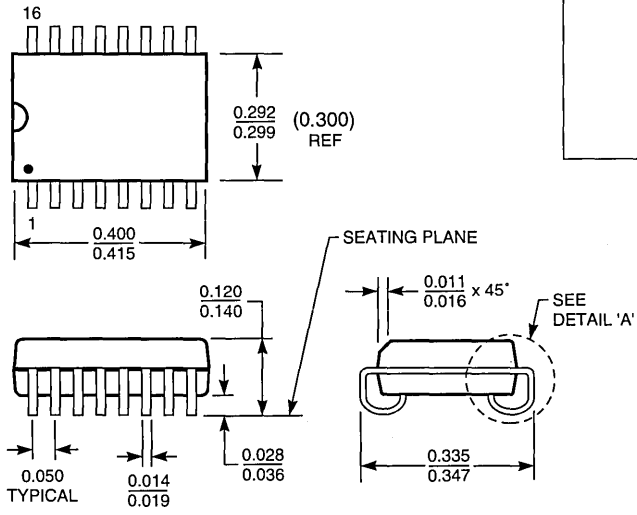
W3 — 20-pin, 0.3" wide

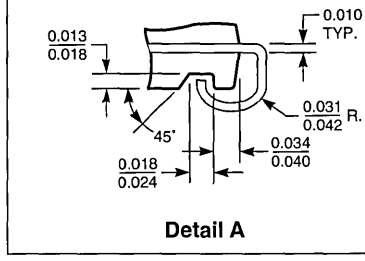




Detail A

W4 — 16-pin, 0.3" wide

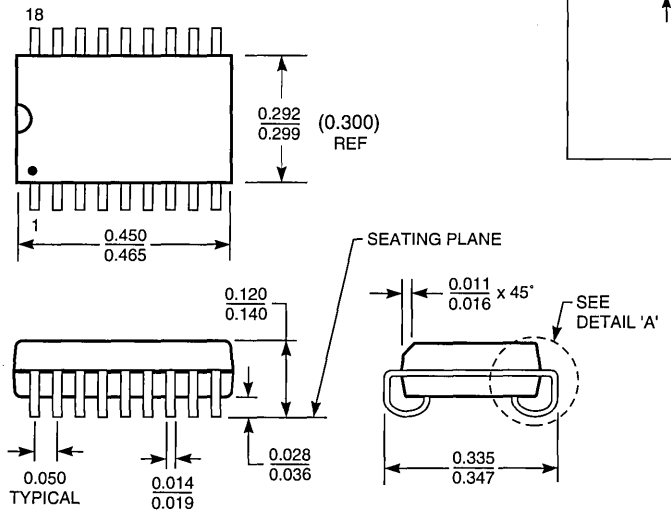


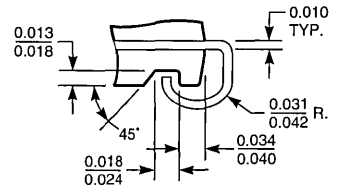


Detail A

PLASTIC SOJ (ORDERING CODE: W)

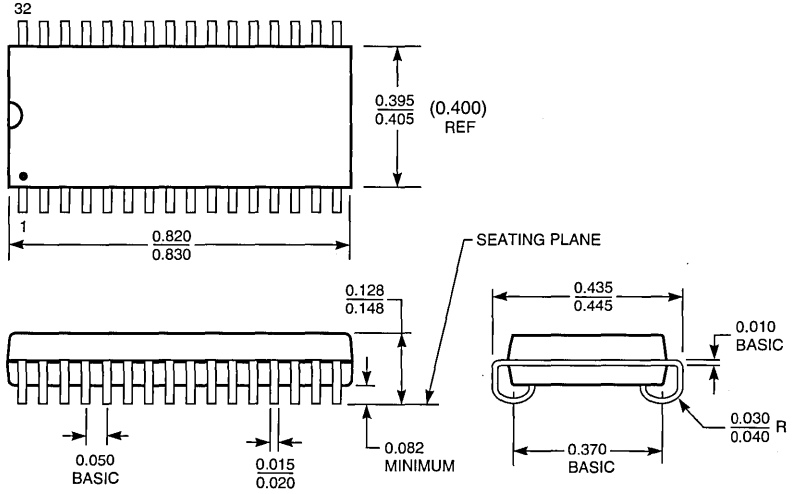
W5 — 18-pin, 0.3" wide





Detail A

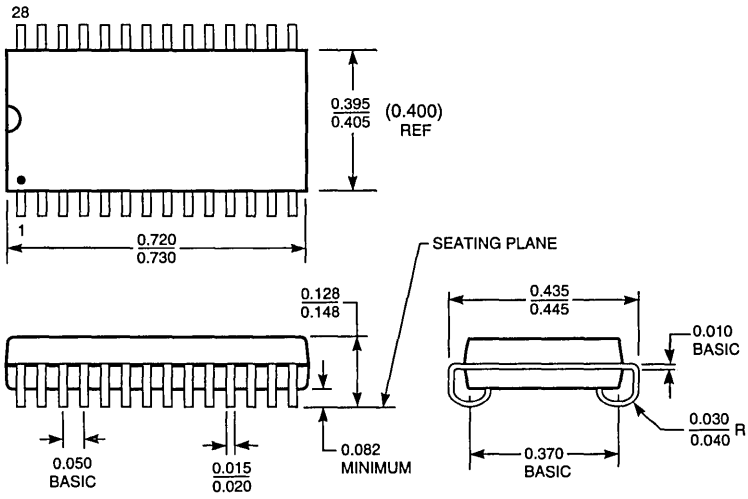
W6 — 32-pin, 0.4" wide



Reference: JEDEC - MS-027-AC

Plastic SOJ (Ordering Code: W)

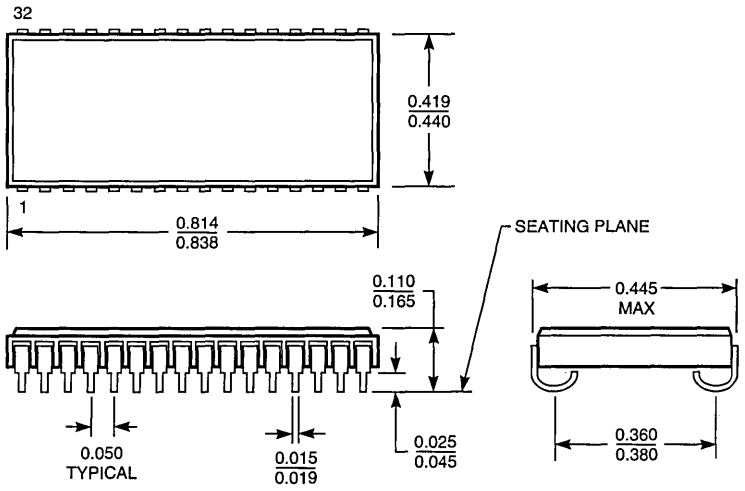
W7 — 28-pin, 0.4" wide



Reference: JEDEC - MS-027-AA

CERAMIC SOJ (ORDERING CODE: Y)

Y1 — 32-pin, 0.440" wide



Product Listing

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DSP PRODUCTS

PART NO.	PRODUCT DESCRIPTION	SPEED (ns) COM.	MIL.	PACKAGE AVAILABILITY
VIDEO IMAGING PRODUCTS				
LF2242	12/16-bit Half-Band Digital Filter	25	—	44-lead PLCC/PQFP
LF2246	11 x 10-bit Image Filter	15	25	120-lead PGA/PQFP
LF2247	11 x 10-bit Image Filter with Coefficient RAM	15	25	84-lead PGA/PLCC, 100-lead PQFP
LF2249	12 x 12-bit Digital Mixer	25	33	120-lead PGA/PQFP
LF2250	12 x 10-bit Matrix Multiplier	20	25	120-lead PGA/PQFP
LF2272	Colorspace Converter (3 x 12-bits)	20	25	120-lead PGA/PQFP
LF2301	Image Resampling Sequencer	25	30	68-lead PGA/PLCC
LF3310	Horizontal/Vertical Digital Image Filter	TBA	TBA	TBA
LF3320	Horizontal Digital Image Filter	TBA	TBA	TBA
LF3330	Vertical Digital Image Filter	TBA	TBA	TBA
LF3347	HighSpeed Image Filter with Coefficient RAM	12	—	120-lead PGA/PQFP
LF43168	Dual 8-Tap FIR Filter	15	22	84-lead PGA/PLCC, 100-lead PQFP
LF43881	8 x 8-bit Digital Filter	25	33	84-lead PGA/PLCC, 100-lead PQFP
LF43891	9 x 9-bit Digtial Filter	25	33	84-lead PGA/PLCC, 100-lead PQFP
LF48212	12 x 12-bit Alpha Mixer	20	—	68-lead PLCC, 64-lead PQFP
LF48410	1024 x 24-bit Video Histogrammer	25	30	84-lead PGA/PLCC
LF48908	Two Dimensional Convolver	25	25	84-lead PGA/PLCC, 100-lead PQFP
LF9501	1280 x 10-bit Frame Buffer	20	—	44-lead PLCC
LF9502	2048 x 10-bit Frame Buffer	20	—	44-lead PLCC
ARITHMETIC LOGIC UNITS				
L4C381	16-bit Cascadable ALU	15	20	68-lead LCC/PGA/PLCC
L4C383	16-bit Cascadable ALU (Extended Set)	15	20	68-lead LCC/PGA/PLCC
SPECIAL ARITHMETIC FUNCTIONS				
LSH32	32-bit Barrel Shifter	20	30	68-lead LCC/PGA/PLCC
LSH33	32-bit Barrel Shifter with Registers	20	30	68-lead LCC/PGA/PLCC
L10C23	64 x 1 Digital Correlator	20	20	24-lead DIP, 28-lead LCC
L2330	Coordinate Transformer	20	20	120-lead PGA/PQFP
L2340	Digital Synthesizer	20	20	120-lead PGA/PQFP
L64230	Template Matcher	25	45	132-lead FP/144-lead PQFP

DSP PRODUCTS (CONTINUED)

PART NO.	PRODUCT DESCRIPTION	SPEED (ns) COM.	SPEED (ns) MIL.	PACKAGE AVAILABILITY
MULTIPLIERS				
LMU08	8 x 8-bit, Signed	20	25	40-lead DIP, 44-lead LCC/PLCC
LMU8U	8 x 8-bit, Unsigned	20	25	40-lead DIP, 44-lead LCC/PLCC
LMU12	12 x 12-bit	20	25	64-lead DIP, 68-lead PGA
LMU112	12 x 12-bit, Reduced Pinout	25	30	48-lead DIP, 52-lead PLCC
LMU16	16 x 16-bit	20	25	64-lead DIP, 68-lead PGA
LMU216	16 x 16-bit, Surface Mount	20	25	68-lead LCC/PLCC
LMU18	16 x 16-bit, 32 Outputs	20	25	84-lead PGA/PLCC
LMU217	16 x 16-bit, Microprogramable, Surface Mount	20	25	68-lead LCC/PLCC
MULTIPLIER-ACCUMULATORS				
LMA1008	8 x 8-bit	20	25	48-lead DIP, 68-lead PLCC
LMA1009	12 x 12-bit	20	25	64-pin DIP, 68-pin PGA
LMA2009	12 x 12-bit, Surface Mount	20	25	68-lead LCC/PLCC
LMA1010	16 x 16-bit	20	25	64-pin DIP, 68-pin PGA
LMA2010	16 x 16-bit, Surface Mount	20	25	68-lead LCC/PLCC
MULTIPLIER-SUMMERS				
LMS12	12 x 12 + 26-bit, FIR	35	40	84-pin PGA, 84-lead PLCC
PIPELINE REGISTERS				
L29C520	4 x 8-bit Multilevel (1-4 Stages)	14	16	24-pin DIP/FP, 28-lead LCC/PLCC
L29C521	4 x 8-bit Multilevel (1-4 Stages)	22	24	24-pin DIP/FP, 28-lead LCC/PLCC
LPR520	4 x 16-bit Multilevel (1-4 Stages)	15	18	40-pin DIP, 44-lead LCC/PLCC
LPR200	8 x 16-bit Multilevel (1-8 Stages)	12	15	48-pin DIP, 52-lead LCC/PLCC
L29C525	16 x 8-bit Dual 8-Deep (1-16 Stages)	15	20	28-pin DIP/FP, 28-lead PLCC
L10C11	4/8-bit Var. Length (3-18 Stages)	15	20	24-pin DIP, 28-lead PLCC
L21C11	8-bit Var. Length (1-16 Stages)	15	20	24-pin DIP, 28-lead PLCC

PERIPHERAL PRODUCTS

PART NO.	PRODUCT DESCRIPTION	SPEED (ns) COM.	SPEED (ns) MIL.	PACKAGE AVAILABILITY
SCSI BUS CONTROLLERS				
L5380	SCSI Bus Controller	4 Mb/s	—	40-pin DIP, 44-lead PLCC
L53C80	SCSI Bus Controller	4 Mb/s	2 Mb/s	48-pin DIP, 44-lead LCC/PLCC

MEMORY PRODUCTS

PART NO.	PRODUCT DESCRIPTION	SPEED (ns) COM.	SPEED (ns) MIL.	PACKAGE AVAILABILITY
64K STATIC RAMS				
L7C162	16K x 4, Separate I/O	12	15	28-pin DIP/SOJ/LCC
L7C164	16K x 4, Common I/O	12	15	22-pin DIP, 24-pin SOJ
L7C166	16K x 4, Common I/O + OE	12	15	24-pin DIP/SOJ, 28-lead LCC
256K STATIC RAMS				
L7C194	64K x 4, Common I/O	15	20	24-pin DIP/SOJ, 28-lead LCC
L7C195	64K x 4, Common I/O + OE	15	20	28-pin DIP/SOJ
L7C199	32K x 8, Common I/O + OE	15	20	28-pin DIP/FP/SOJ, 28/32-lead LCC
1M STATIC RAMS				
L7C106	256K x 4, Common I/O, 1 CE + OE	17	—	28-pin DIP/SOJ
L7C108	128K x 8, Common I/O, 1 CE + OE	17	20	32-pin DIP/SOJ, 32-lead LCC
L7C109	128K x 8, Common I/O, 2 CE + OE	17	20	32-pin DIP/SOJ, 32-lead LCC
SPECIAL ARCHITECTURE STATIC RAMS				
L7C174	8K x 8, Cache-Tag	12	15	28-pin DIP/SOJ, 32-lead LCC
FIFO PRODUCTS				
L8C201	512 x 9, Asynchronous	10	—	28-pin DIP, 32-lead PLCC
L8C202	1K x 9, Asynchronous	10	—	28-pin DIP, 32-lead PLCC
L8C203	2K x 9, Asynchronous	10	—	28-pin DIP, 32-lead PLCC
L8C204	4K x 9, Asynchronous	10	—	28-pin DIP, 32-lead PLCC
L8C211	512 x 9, Synchronous	15	—	32-lead PLCC
L8C221	1K x 9, Synchronous	15	—	32-lead PLCC
L8C231	2K x 9, Synchronous	15	—	32-lead PLCC
L8C241	4K x 9, Synchronous	15	—	32-lead PLCC

DECC SMD PRODUCTS (LISTED BY LOGIC DEVICES PART NUMBER)

PART NO.	DECC SMD NUMBER	AVAILABILITY	PRODUCT DESCRIPTION
DSP PRODUCTS			
L10C23	5962-89711	Released	64 x 1 Digital Correlator
L2330	5962-92331	Consult Factory	16 x 16-bit Coordinate Transformer
L29C520	5962-91762	Released	4 x 8-bit Multilevel Pipeline Register
L29C521	5962-91762	Released	4 x 8-bit Multilevel Pipeline Register
L29C525	5962-91696	Released	16 x 8-bit Dual 8-Deep Pipeline Register
L29C818	5962-90515	Released	8-bit Serial Scan Shadow Register
L4C381	5962-89959	Released	16-bit Cascadable ALU
L64230	5962-90504	Released	Template Matcher
LF2250	5962-93260	Released	12 x 10-bit Matrix Multiplier
LF2301	5962-89715	Consult Factory	Image Resampling Sequencer
LF43168	5962-97504	Released	Dual 8-Tap FIR Filter
LF43891	5962-92097	Released	9 x 9-bit Digital Filter
LF48410	5962-94573	Released	1024 x 24-bit Video Histogrammer
LF48908	5962-93007	Released	Two Dimensional Convolver
LMA1008	5962-90708	Released	8 x 8-bit Multiplier-Accumlator
LMA1009	5962-90996	Released	12 x 12-bit Multiplier-Accumlator
LMA2009	5962-90996	Released	12 x 12-bit Multiplier-Accumlator
LMA1010	5962-88733	Released	16 x 16-bit Multiplier-Accumlator
LMA2010	5962-88733	Released	16 x 16-bit Multiplier-Accumlator
LMS12	5962-94608	Released	12 x 12 + 26-bit Multiplier-Summer, FIR
LMU08	5962-88739	Released	8 x 8-bit Parallel Multiplier
LMU8U	5962-88739	Released	8 x 8-bit Parallel Multiplier
LMU16	5962-86873	Released	16 x 16-bit Parallel Multiplier
LMU216	5962-86873	Released	16 x 16-bit Parallel Multiplier
LMU217	5962-87686	Released	16 x 16-bit Parallel Multiplier
LMU18	5962-94523	Released	16 x 16-bit Parallel Multiplier w/32 outputs
LPR520	5962-89716	Released	4 x 16-bit Multilevel Pipeline Register
LSH32	5962-89717	Released	32-bit Barrel Shifter
PERIPHERAL PRODUCTS			
L53C80	5962-90548	Released	SCSI Bus Controller
MEMORY PRODUCTS			
L7C108	5962-89598	Released	128K x 8 Static RAM
L7C109	5962-89598	Released	128K x 8 Static RAM
L7C162	5962-89712	Released	16K x 4 Static RAM
L7C194	5962-88681	Released	64K x 4 Static RAM
L7C195	5962-89524	Released	64K x 4 Static RAM
L7C199	5962-88662	Released	32K x 8 Static RAM
L8C202	5962-89536	Released	1024 x 9-bit Asynchronous FIFO

DECC SMD PRODUCTS (LISTED BY SMD NUMBER)

DECC SMD NO.	LOGIC PART NO.	AVAILABILITY	PRODUCT DESCRIPTION
DSP PRODUCTS			
5962-86873	LMU16/LMU216	Released	16 x 16-bit Parallel Multiplier
5962-87686	LMU217	Released	16 x 16-bit Parallel Multiplier
5962-88733	LMA1010/LMA2010	Released	16 x 16-bit Multiplier-Accumulator
5962-88739	LMU08/LMU8U	Released	8 x 8-bit Parallel Multiplier
5962-89711	L10C23	Released	64 x 1 Digital Correlator
5962-89716	LPR520	Released	4 x 16-bit Multilevel Pipeline Register
5962-89717	LSH32	Released	32-bit Barrel Shifter
5962-89959	L4C381	Released	16-bit Cascadable ALU
5962-90504	L64230	Released	Template Matcher
5962-90515	L29C818	Released	8-bit Serial Scan Shadow Register
5962-90708	LMA1008	Released	8 x 8-bit Multiplier-Accumulator
5962-90996	LMA1009/LMA2009	Released	12 x 12-bit Multiplier-Accumulator
5962-91696	L29C525	Released	16 x 8-bit Dual 8-Deep Pipeline Register
5962-91762	L29C520/L29C521	Released	4 x 8-bit Multilevel Pipeline Register
5962-92097	LF43891	Released	9 x 9-bit Digital Filter
5962-93007	LF48908	Released	Two Dimensional Convolver
5962-93260	LF2250	Released	12 x 10-bit Matrix Multiplier
5962-94523	LMU18	Released	16 x 16-bit Parallel Multiplier w/32 outputs
5962-94573	LF48410	Released	1024 x 24-bit Video Histogrammer
5962-94608	LMS12	Released	12 x 12 + 26-bit Multiplier-Summer, FIR
5962-90504	L64230	Released	Template Matcher
5962-96793	L10C11/L21C11	Released	4/8-bit Variable Length Shift Register
5962-97504	LF43168	Released	Dual 8-Tap FIR Filter
PERIPHERAL PRODUCTS			
5962-90548	L53C80	Released	SCSI Bus Controller
MEMORY PRODUCTS			
5962-88662	L7C199	Released	32K x 8 Static RAM
5962-88681	L7C194	Released	64K x 4 Static RAM
5962-89524	L7C195	Released	64K x 4 Static RAM
5962-89536	L8C202	Released	1024 x 9-bit Asynchronous FIFO
5962-89598	L7C108/L7C109	Released	128K x 8 Static RAM
5962-89712	L7C162	Released	16K x 4 Static RAM

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(503) 626-4040

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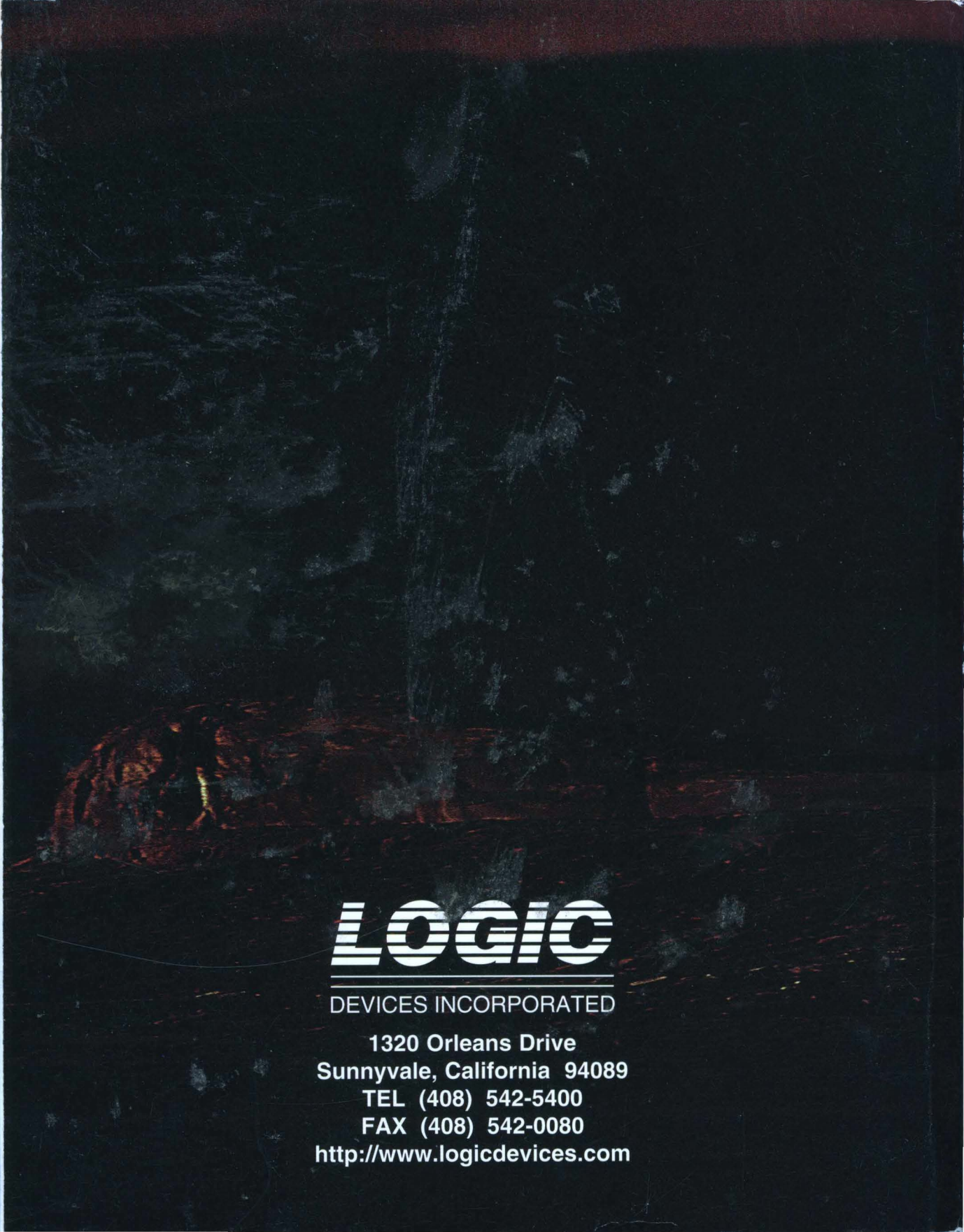

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