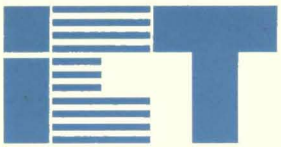

INTERNATIONAL CMOS
TECHNOLOGY, INC.

CMOS Programmable Products

1990 Data Book

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Table of Contents

1.0 General Information

2.0 CMOS Serial EEPROMs

3.0 CMOS High-Speed PROMs

4.0 CMOS High-Speed EPROMs

5.0 CMOS PEEL Devices

6.0 CMOS PEEL Arrays

7.0 Development Tools

8.0 Article Reprints

9.0 Package Information

10.0 Sales Representatives and Distributors

President's Message

International CMOS Technology, Inc. (ICT) is pleased to bring to you our 1990 CMOS Programmable Products Data Book. ICT's technical expertise in non-volatile memory technologies has allowed us to produce a broad spectrum of leading-edge user-programmable integrated circuits. Our 1990 product line, which has doubled from last year, offers over thirty products with the features, performance and development support needed by designers today.

This year's offering includes several product innovations: including: the 93CX46/56/66 series of extended voltage EEPROMs, the worlds fastest 1-Meg EPROM the 27CX010, the high density PA7024/40 logic arrays, and the unique PACE Advanced Development Software.

In addition to our product line expansion, we have enhanced our existing strategic alliances and created new alliances with several major semiconductor manufacturers, thus assuring high-volume manufacturing capability to support our accelerated growth. ICT has also continued its serious commitment to quality and reliability. This commitment starts with the inherent reliability and testability of ICT's CMOS EPROM and EEPROM technologies and is enhanced through our advanced design, manufacturing and testing techniques. Service and customer satisfaction are the primary goals of ICT's quality team.

We at ICT thank you for your interest in ICT products and know you will find our 1990 data book useful in your future programmable IC design efforts.

Drew Allen Osterman
President and CEO

General Information

ICT Product Line

CMOS SERIAL EEPROMs	CMOS HIGH SPEED PROMs	CMOS HIGH SPEED EPROMs	CMOS PEEL DEVICES	CMOS PEEL ARRAYS	DEVELOPMENT TOOLS
93C46	27CX321	27CX256*	PEEL18CV8	PA7024*	PDS-1 PEEL Dev. System
93C46A*	27CX322	27CX010*	PEEL18CV8-15	PA7040*	PEEL Device Dev. Software
93C56A*	27CX641		PEEL18CV8-10*		PACE* Advanced Dev. Software
93C66A	27CX642		PEEL20CG10		MPS-1 PROM Program Software
93CX46*			PEEL20CG10-12*		MPS-2* EEPROM Program Software
93CX56*			PEEL22CV10		
93CX66			PEEL22CV10-12*		
			PEEL22CV10Z		
			PEEL153		
			PEEL253		
			PEEL173		
			PEEL173-15*		
			PEEL273		
			PEEL273-15*		

* New Products

ICT Product Overview

International CMOS Technology, Inc. (ICT) designs, manufactures, and markets user-programmable integrated circuits. With expertise in technology and circuit design, the company has combined complimentary-metal-oxide-semiconductor (CMOS) with electrically-erasable (EE) or ultra-violet-erasable (UV) memory technologies to create non-volatile programmable memories and logic devices.

Founded in 1983 in the heart of California's Silicon Valley, ICT initially entered the mainstream semiconductor industry by successfully producing the world's first 5V-only CMOS EEPROM (the 93C46). Since then, ICT has continued to introduce state-of-the-art CMOS ICs. The current product line families are listed below:

ICT Product Line

- **CMOS Serial EEPROMs**
- **CMOS High-Speed PROMs and EPROMs**
- **CMOS PEEL Devices**
- **CMOS PEEL Arrays**
- **Development Tools**

CMOS Serial EEPROMs

ICT's CMOS Serial EEPROMs provide in-system-programmable non-volatile data storage (that is, the data programmed, remains even after power is removed). Unlike parallel EEPROMs, ICT's serial EEPROMs offers low power consumption, low cost, space efficiency, and a 3 or 4 line interface that is easy to use with popular microcomputers. ICT's 1,024-bit 93C46 has become an industry standard with features that are ideal for high-volume, low density, data storage applications such as meters, alarms, locks, ID tags, appliances, telephones and VCRs.

ICT's second generation family of CMOS Serial EEPROMs include 1K-bit, 2K-bit, and 4K-bit devices in both 5V-only and extended-voltage (2.5V-6.0V) versions. Besides higher densities, the new EEPROMs offer new features such as an autoerase write instruction and both hardware and software write protection. The extended voltage version EEPROMs, the 93CX46, 93CX56, and 93CX66, are ideal for battery-powered applications which must operate from high to low voltages and consume as little power as possible.

CMOS High-Speed PROMs and EPROMs

ICT offers two related product families that are both based on high-speed CMOS EPROM technology. The CMOS PROMs are available in 24-pin DIP packages that are compatible with bipolar PROM pin-outs. The CMOS EPROMs come in 28-pin and 32-pin packages with JEDEC standard EPROM pin-outs. Both families offer the high speed operation.

ICT's High-Speed PROM family, with access times as fast as 35ns and densities of 32K (4Kx8) and 64K (8Kx8), are frequently used in computation-intensive applications, such as digital signal processing (DSP), high speed modems, and video graphics controllers. Unlike common Bipolar PROMs, ICT's CMOS PROMs offer low-power consumption and reprogrammability which reduces system development and field-retrofit costs permitting the devices to accommodate code changes. Reprogrammability also enhances testability, allowing 100% factory testing for program and function.

ICT's High-Speed CMOS EPROMs give systems design engineers the speed and density required for "no wait-state" operation with today's 16-bit and 32-bit microprocessors. The family of JEDEC-standard 32-pin and 28-pin EPROMs, initially offer densities of 1M (128Kx8) and 256K (32Kx8), at speeds as fast as 55ns and 40ns respectively. Pin-out compatibility allows for easy upgrades through 8 Megabits. Processed in an advanced 1.0 micron CMOS technology, these devices offer the fastest access times per density available along with low power consumption and UV-reprogrammability.

CMOS PEEL Devices

Programmable logic devices (PLDs) in effect allow system designers to "write on silicon" and create custom logic functions in user-programmable off-the-shelf parts. The main benefits of PLD technology are the reduction of system parts count and quicker design turn-around. In a typical design, a single PLD can replace four or more standard logic packages. The design approach used with PLDs also reduces the time required to turn a design concept into a working circuit.

ICT's CMOS Programmable Electrically-Erasable Logic (PEEL) Devices offer several advantages over early-generation PLDs most of which are fabricated in bipolar technology. Unlike bipolar and other one-time-programmable PLDs, PEEL devices, give the designer a reprogrammable and completely tested alternative in a plastic package. Each PEEL device is programmed and tested during manufacturing to ensure 100% programming and function yield. PEEL devices also offer low-power consumption ranging from 1/2 to 1/8 that of standard PLDs. Ultra-low power consumption can be achieved using the "Zero-Power" PEEL22CV10Z.

A key feature of PEEL devices are their enhanced architectures enabling them to take on the identity of a variety of popular 20 and 24-pin PLDs (PAL, GAL, EPLD, FPLA). For example, the PEEL18CV8 can emulate over 25 different PLDs with automatic translation via the PEEL Device Development Software. Thus, users can simplify inventories to a few PEEL devices and take advantage of PEEL low power consumption and EE-reprogrammability. The PEEL enhanced architectures also offer additional features such as a twelve configuration macro-cell, more product terms, and independent output enables, all of which allow designers to get more logic in each device.

PEEL Arrays

One of ICT's newest product families, PEEL Arrays are user-configurable high density ICs for creating multi-level, I/O buried, logic circuits. Designed in ICT's advanced 1-micron CMOS EE-technology, PEEL Arrays combine: the "wide-gate" speed performance of conventional PLDs, the architectural flexibility associated with Field Programmable Gate Arrays and a "best of both worlds" design methodology. PEEL Arrays offer all the same technology benefits of PEEL devices but at much higher levels of density and flexibility. The initial members of this family include the PA7024 and PA7040.

Development Tools

To support ICT's complete line of user-programmable products ICT offers software and programmer development tools for its PEEL Devices, PEEL Arrays and memory products. For PEEL Devices, ICT provides free PEEL Device development software as well as a low cost, easy-to-use, PC-based development system (PDS-1) which consists of design software, programmer and tester. For PEEL Arrays and PEEL Devices, the PACE Advanced Development Software offers an innovative and efficient method of design. Additionally, ICT's PROM and EEPROM memory products can be programmed using the PDS-1 system in conjunction with the MPS programming software.

ICT Quality and Reliability

International CMOS Technology (ICT) is dedicated to providing its customers with integrated circuits that are designed, manufactured, tested, and serviced to the highest level of Quality and Reliability. From product definition through full production, ICT has developed and implemented a system designed to continually produce leading-edge CMOS products that meet, and usually exceed all customer requirements. At ICT, we recognize that product excellence is only obtained by a continuous commitment to be the leader in quality and reliability. ICT's quality and reliability programs are separated into the following categories:

ICT Quality and Reliabilty

- **Quality and Reliability by Design**
- **Initial Device Qualification**
- **Ongoing Monitor Qualification**
- **Quality and Reliability by Test**
- **Customer Service**

Quality and Reliability by Design

ICT's design philosophy emphasizes quality and reliability during every part of the design cycle. Conservative design rules and extensive logic and circuit simulation are performed over extreme operating conditions. During circuit and process design, special attention is paid to problems such as CMOS latch-up and electrostatic discharge (ESD). For example, ICT's I/O pins are prevented from CMOS latch-up by a double guard-ring designed into all products. Also ICT designers have developed and implemented techniques to protect all products from electrostatic discharge (ESD) up to 2000V on all I/O pins.

Special features are also designed into ICT products to improve the reliability of the device. As an example, all of ICT's second generation EEPROMs have a Program Enable (PE) hardware write protection designed to prevent against inadvertent writes during system power-up and power-down. These type of design considerations enhance the product's reliability in actual system applications.

Initial Device Qualification

Tests have been developed to observe the life expectancy of each new product. In order to qualify a new product, packaged parts from a minimum of three different lots must be scrutinized for electrical functionality and reliability over extreme temperature and voltage conditions. Tests include operating life, data retention, endurance, temperature cycling, temperature/humidity bias, ESD, and latch-up. Pre-determined reliability goals must be met in order for a product to pass qualification. All procedures and results are carefully documented for future reference. This qualification validates the device, package, and supplier. Therefore, whenever design rules are adjusted, a new foundry or assembly facility is used, or a new package type is introduced, a re-qualification of the product must be completed.

A Dynamic High-Temperature Operating Life (DHTOL) test is a standard approach used to evaluate the reliability of a product under accelerated conditions. Data is gathered at the rated ambient temperature and the devices are biased as they would be in actual operation. The devices are exercised by constantly switching the inputs.This DHTOL test is set for a continuous operation typically at an ambient temperature of 125^{o}C and a duration of test equal to 1,000 hours. The results of the DHTOL test are recorded in a datalog and made available for future reference.

At the cell level, data retention is a function of the floating gate's ability to retain charge. Data retention failures in a floating gate structure are commonly caused by dielectric defects and can be accelerated by high temperature bake stress. ICT's products are designed to provide data retention for at least ten years at the maximum rated temperature which is equivalent to over forty years of data retention at 55^{o}c. ICT uses an industry standard endurance specification that for any lot of devices shipped, fewer than 5% of the units will cease to cycle properly before the specified limit when cycled at room temperature. ICT continually samples production lots of products by bulk programming and erasing the units for the specified cycles to assure the product meets ICT's endurance criteria.

Ongoing Monitor Qualification

Although initial device qualification is an essential step to a product release, all products must be constantly monitored to ensure the reliability of the device. Production lots are sampled every quarter, and are subject to the same initial qualification tests, such as the DHTOL test and endurance test. All results are again documented, and failures are carefully analyzed in order to find long term improvements to the product. An example of the ongoing monitor program includes: Operating Life Test, Data Retention Bake and Cycling Endurance.

Quality and Reliability by Test

ICT has developed a test flow to ensure that all products shipped to customers are of the highest quality and reliability. Each device is erased, programmed, and read at Wafer Sort, Package Test, Post-Bake Final Test, and QA Test to guarantee electrical characteristics over the entire operating temperature range and functionality of the part. Test programs are developed to screen out those devices which fail to meet data sheet specifications. Additionally since all ICT's products are programmable, every unit shipped is subjected to a data retention bake which verifies the ability to retain data for at least ten years over the entire temperature range. This is the equivalent of over forty years of data retention at 55^{o}c.

Customer Service

Customer service plays an important role in quality assurance. Customer product concerns are serviced and documented with failure analysis reports that states the problem and suggests a corrective solution. All ICT employees are a part of the customer service team, whose goal is to provide customer satisfaction.

CMOS Serial EEPROM Selection Guide

PART #	DESCRIPTION	PINS	SPEED	I_{CC}/I_{SB}	TEMP[1]	PACKAGE[2]
93C46C	64 x 16 bit Serial EEPROM	8	n/a	3mA/0.1mA	C	C8
93C46CI	64 x 16 bit Serial EEPROM	8	n/a	6mA/0.1mA	I	C8
93C46CM	64 x 16 bit Serial EEPROM	8	n/a	7mA/0.1mA	M	C8
93C46P	64 x 16 bit Serial EEPROM	8	n/a	3mA/0.1mA	C	P8
93C46PE	93C46 with 100k cycle endurance	8	n/a	3mA/0.1mA	C	P8
93C46PIE	93C46I with 100k cycle endurance	8	n/a	6mA/0.1mA	I	P8
93C46PI	64 x 16 bit Serial EEPROM	8	n/a	6mA/0.1mA	I	P8
93C46PM	64 x 16 bit Serial EEPROM	8	n/a	7mA/0.1mA	M	P8
93C46S	64 x 16 bit Serial EEPROM	8	n/a	3mA/0.1mA	C	S8
93C46SI	64 x 16 bit Serial EEPROM	8	n/a	6mA/0.1mA	I	S8
93C46AP	64 x 16 bit Serial EEPROM	8	n/a	3mA/0.1mA	C	P8
93C46API	64 x 16 bit Serial EEPROM	8	n/a	6mA/0.1mA	I	P8
93C46APM	64 x 16 bit Serial EEPROM	8	n/a	7mA/0.1mA	M	P8
93C46AK	64 x 16 bit Serial EEPROM	8	n/a	3mA/0.1mA	C	K8
93C46AS	64 x 16 bit Serial EEPROM	8	n/a	3mA/0.1mA	C	S8
93C46AKI	64 x 16 bit Serial EEPROM	8	n/a	6mA/0.1mA	I	K8
93C46ASI	64 x 16 bit Serial EEPROM	8	n/a	6mA/0.1mA	I	S8
93C56AP	128 x 16 bit Serial EEPROM	8	n/a	3mA/0.05mA	C	P8
93C56API	128 x 16 bit Serial EEPROM	8	n/a	6mA/0.1mA	I	P8
93C56APM	128 x 16 bit Serial EEPROM	8	n/a	7mA/0.2mA	M	P8
93C56AK	128 x 16 bit Serial EEPROM	8	n/a	3mA/0.05mA	C	K8
93C56AKI	128 x 16 bit Serial EEPROM	8	n/a	6mA/0.1mA	I	K8
93C66AP	256 x 16 bit Serial EEPROM	8	n/a	3mA/0.05mA	C	P8
93C66API	256 x 16 bit Serial EEPROM	8	n/a	6mA/0.1mA	I	P8
93C66APM	256 x 16 bit Serial EEPROM	8	n/a	7mA/0.2mA	M	P8
93C66AK	256 x 16 bit Serial EEPROM	8	n/a	3mA/0.05mA	C	K8
93C66AKI	256 x 16 bit Serial EEPROM	8	n/a	6mA/0.1mA	I	K8
93CX46P	64 x 16 bit Serial EEPROM (2.5V to 6.0V)	8	n/a	3mA/0.05mA	C	P8
93CX46PI	64 x 16 bit Serial EEPROM (2.5V to 6.0V)	8	n/a	6mA/0.1mA	I	P8
93CX46PM	64 x 16 bit Serial EEPROM (2.5V to 6.0V)	8	n/a	7mA/0.2mA	M	P8
93CX46K	64 x 16 bit Serial EEPROM (2.5V to 6.0V)	8	n/a	3mA/0.05mA	C	K8
93CX46KI	64 x 16 bit Serial EEPROM (2.5V to 6.0V)	8	n/a	6mA/0.1mA	I	K8
93CX56P	128 x 16 bit Serial EEPROM (2.5V to 6.0V)	8	n/a	4mA/0.05mA	C	P8

CMOS Serial EEPROM Selection Guide (cont.)

PART #	DESCRIPTION	PINS	SPEED	I_{CC}/I_{SB}	TEMP[1]	PACKAGE[2]
93CX56PI	128 x 16 bit Serial EEPROM (2.5V to 6.0V)	8	n/a	6mA/0.1mA	I	P8
93CX56PM	128 x 16 bit Serial EEPROM (2.5V to 6.0V)	8	n/a	8mA/0.2mA	M	P8
93CX56K	128 x 16 bit Serial EEPROM (2.5V to 6.0V)	8	n/a	4mA/0.05mA	C	K8
93CX56KI	128 x 16 bit Serial EEPROM (2.5V to 6.0V)	8	n/a	6mA/0.1mA	I	K8
93CX66P	256 x 16 bit Serial EEPROM (2.5V to 6.0V)	8	n/a	4mA/0.05mA	C	P8
93CX66PI	256 x 16 bit Serial EEPROM (2.5V to 6.0V)	8	n/a	6mA/0.1mA	I	P8
93CX66PM	256 x 16 bit Serial EEPROM (2.5V to 6.0V)	8	n/a	8mA/0.2mA	M	P8
93CX66K	256 x 16 bit Serial EEPROM (2.5V to 6.0V)	8	n/a	4mA/0.5mA	C	K8
93CX66KI	256 x 16 bit Serial EEPROM (2.5V to 6.0V)	8	n/a	6mA/0.1mA	I	K8

[2]**Package Codes:** See section 9.0 for package drawings
C = Ceramic DIP
K = 8 Pin SOIC (standard pin-out)
N = Windowed Ceramic DIP (300 mil)
P = Plastic DIP
S = 8 Pin SOIC (rotated pin-out)
W = Windowed Ceramic DIP (600 mil)

[1]**Temperature range codes:**
C = Commercial 0°C to +70°C
I = Industrial -40°C to +85°C
M = Military -55°C to +125°C

CMOS High Speed PROM and EPROM Selection Guide

PART #	DESCRIPTION	PINS	SPEED	I_{CC}/I_{SB}	TEMP[1]	PACKAGE[2]
27CX321C-35	4k x 8 bit High Speed PROM	24	35ns	40mA/0.5mA*	C	W24
27CX321C-40	4k x 8 bit High Speed PROM	24	40ns	40mA/0.5mA*	C	W24
27CX321C-45	4k x 8 bit High Speed PROM	24	45ns	40mA/0.5mA*	C	W24
27CX321CI-45	4k x 8 bit High Speed PROM	24	45ns	60mA/0.5mA*	I	W24
27CX321CI-55	4k x 8 bit High Speed PROM	24	55ns	60mA/0.5mA*	I	W24
27CX322C-35	4k x 8 bit High Speed PROM	24	35ns	40mA/0.5mA*	C	N24
27CX322C-40	4k x 8 bit High Speed PROM	24	40ns	40mA/0.5mA*	C	N24
27CX322C-45	4k x 8 bit High Speed PROM	24	45ns	40mA/0.5mA*	C	N24
27CX322CI-45	4k x 8 bit High Speed PROM	24	45ns	60mA/0.5mA*	I	N24
27CX322CI-55	4k x 8 bit High Speed PROM	24	55ns	60mA/0.5mA*	I	N24
27CX641C-35	8k x 8 bit High Speed PROM	24	35ns	90mA	C	W24
27CX641C-40	8k x 8 bit High Speed PROM	24	40ns	80mA	C	W24
27CX641C-45	8k x 8 bit High Speed PROM	24	45ns	80mA	C	W24
27CX641C-55	8k x 8 bit High Speed PROM	24	55ns	80mA	C	W24
27CX641CI-45	8k x 8 bit High Speed PROM	24	45ns	120mA	I	W24
27CX641CI-55	8k x 8 bit High Speed PROM	24	55ns	120mA	I	W24
27CX642C-35	8k x 8 bit High Speed PROM	24	35ns	90mA	C	N24
27CX642C-40	8k x 8 bit High Speed PROM	24	40ns	80mA	C	N24
27CX642C-45	8k x 8 bit High Speed PROM	24	45ns	80mA	C	N24
27CX642C-55	8k x 8 bit High Speed PROM	24	55ns	80mA	C	N24
27CX642CI-45	8k x 8 bit High Speed PROM	24	45ns	120mA	I	N24
27CX642CI-55	8k x 8 bit High Speed PROM	24	55ns	120mA	I	N24
27CX256C-40	32k x 8 bit Hgh Speed EPROM	28	40ns	90mA	C	N28
27CX256C-45	32k x 8 bit Hgh Speed EPROM	28	45ns	90mA	C	N28
27CX256C-70	32k x 8 bit Hgh Speed EPROM	28	70ns	90mA	C	N28
27CX010C-55	128k x 8 High Speed EPROM	32	55ns	90mA/1mA	C	W2
27CX010C-70	128k x 8 High Speed EPROM	32	70ns	90mA/1mA	C	W2
27CX010C-90	128k x 8 High Speed EPROM	32	90ns	90mA/1mA	C	W2

[2]**Package Codes:** See section 9.0 for package drawings
C = Ceramic DIP
N = Windowed Ceramic DIP (300 mil)
P = Plastic DIP
W = Windowed Ceramic DIP (600 mil)
***typical standby current**

[1]**Temperature range codes:**
C = Commercial 0°C to +70°C
I = Industrial -40°C to +85°C

CMOS PEEL Device Selection Guide

PART #	DESCRIPTION	PINS	SPEED	Icc mA	TEMP[1]	PACKAGE[2]
PEEL18CV8P-10	PLD superset 12 config, I/O macrocells (8)	20	10ns	80+0.5/MHz	C	P20
PEEL18CV8P-12	PLD superset 12 config, I/O macrocells (8)	20	12ns	80+0.5/MHz	C	P20
PEEL18CV8P-15	PLD superset 12 config, I/O macrocells (8)	20	15ns	80+0.5/MHz	C	P20
PEEL18CV8P-20	PLD superset 12 config, I/O macrocells (8)	20	20ns	80+0.5/MHz	C	P20
PEEL18CV8P-25	PLD superset 12 config, I/O macrocells (8)	20	25ns	20+0.7/MHz	C	P20
PEEL18CV8P-35	PLD superset 12 config, I/O macrocells (8)	20	35ns	20+0.7/MHz	C	P20
PEEL18CV8PI-25	Industrial Temperature Range PEEL18CV8	20	25ns	30+0.7/MHz	I	P20
PEEL18CV8PI-35	Industrial Temperature Range PEEL18CV8	20	35ns	30+0.7/MHz	I	P20
PEEL18CV8J-10	Surface mount PLCC PEEL18CV8	20	10ns	80+0.5/MHz	C	J20
PEEL18CV8J-12	Surface mount PLCC PEEL18CV8	20	12ns	80+0.5/MHz	C	J20
PEEL18CV8J-15	Surface mount PLCC PEEL18CV8	20	15ns	80+0.5/MHz	C	J20
PEEL18CV8J-20	Surface mount PLCC PEEL18CV8	20	20ns	80+0.5/MHz	C	J20
PEEL18CV8J-25	Surface mount PLCC PEEL18CV8	20	25ns	20+0.7/MHz	C	J20
PEEL18CV8J-35	Surface mount PLCC PEEL18CV8	20	35ns	20+0.7/MHz	C	J20
PEEL20CG10P-12	PLD superset 12 config, I/O macrocells (10)	24	12ns	105+0.5/MHz	C	P24
PEEL20CG10P-15	PLD superset 12 config, I/O macrocells (10)	24	15ns	105+0.5/MHz	C	P24
PEEL20CG10P-20	PLD superset 12 config, I/O macrocells (10)	24	20ns	65+0.5/MHz	C	P24
PEEL20CG10P-25	PLD superset 12 config, I/O macrocells (10)	24	25ns	55+0.5/MHz	C	P24
PEEL20CG10P-35	PLD superset 12 config, I/O macrocells (10)	24	35ns	55+0.5/MHz	C	P24
PEEL20CG10J-12	Surface mount PLCC PEEL20CG10	24	12ns	105+0.5/MHz	C	P24
PEEL20CG10J-15	Surface mount PLCC PEEL20CG10	24	15ns	105+0.5/MHz	C	P24
PEEL20CG10J-20	Surface mount PLCC PEEL20CG10	24	20ns	65+0.5/MHz	C	P24
PEEL20CG10J-25	Surface mount PLCC PEEL20CG10	24	25ns	55+0.5/MHz	C	P24
PEEL20CG10J-35	Surface mount PLCC PEEL20CG10	24	35ns	55+0.5/MHz	C	P24
PEEL22CV10P-12	PLD superset 4/12 config, I/O macrocells (10)	24	12ns	105+0.5/MHz	C	P24
PEEL22CV10P-15	PLD superset 4/12 config, I/O macrocells (10)	24	15ns	105+0.5/MHz	C	P24
PEEL22CV10P-20	PLD superset 4/12 config, I/O macrocells (10)	24	20ns	65+0.5/MHz	C	P24
PEEL22CV10P-25	PLD superset 4/12 config, I/O macrocells (10)	24	25ns	55+0.5/MHz	C	P24
PEEL22CV10P-35	PLD superset 4/12 config, I/O macrocells (10)	24	35ns	55+0.5/MHz	C	P24
PEEL22CV10J-12	Surface mount PLCC PEEL22CV10	24	12ns	105+0.5/MHz	C	P24
PEEL22CV10J-15	Surface mount PLCC PEEL22CV10	24	15ns	105+0.5/MHz	C	P24
PEEL22CV10J-20	Surface mount PLCC PEEL22CV10	24	20ns	65+0.5/MHz	C	P24
PEEL22CV10J-25	Surface mount PLCC PEEL22CV10	24	25ns	55+0.5/MHz	C	P24

CMOS PEEL Device Selection Guide (cont.)

PART #	DESCRIPTION	PINS	SPEED	Icc mA	TEMP[1]	PACKAGE[2]
PEEL22CV10J-35	Surface mount PLCC PEEL22CV10	24	35ns	55+0.5/MHz	C	P24
PEEL22CV10ZP-20	Zero Power 12 config, I/O macrocells (10)	24	20ns	65+0.5/MHz*	C	P24
PEEL22CV10ZP-25	Zero Power 12 config, I/O macrocells (10)	24	25ns	55+0.5/MHz*	C	P24
PEEL22CV10ZP-35	Zero power 12 config, I/O macrocells (10)	24	35ns	55+0.5/MHz*	C	P24
PEEL22CV10ZJ-25	Surface mount PLCC PEEL22CV10Z	24	25ns	55+0.5/MHz*	C	P24
PEEL22CV10ZJ-35	Surface mount PLCC PEEL22CV10Z	24	35ns	55+0.5/MHz*	C	P24
PEEL153P-30	FPLA prog AND/OR/polarity	20	30ns	35+1.0/MHz	C	P20
PEEL153P-35	FPLA prog AND/OR/polarity	20	35ns	35+1.0/MHz	C	P20
PEEL173P-15	FPLA prog AND/OR/polarity	24	15ns	60+0.5/MHz	C	P24
PEEL173P-30	FPLA prog AND/OR/polarity	24	30ns	35+1.0/MHz	C	P24
PEEL173P-35	FPLA prog AND/OR/polarity	24	35ns	35+1.0/MHz	C	P24
PEEL253P-30	Enhanced FPLA prog AND/OR/polarity	20	30ns	35+1.0/MHz	C	P20
PEEL253P-35	Enhanced FPLA prog AND/OR/polarity	20	35ns	35+1.0/MHz	C	P20
PEEL273P-15	FPLA prog AND/OR/polarity	24	15ns	60+0.5/MHz	C	P24
PEEL273P-30	Enhanced FPLA prog AND/OR/polarity	24	30ns	35+1.0/MHz	C	P24
PEEL273P-35	Enhanced FPLA prog AND/OR/polarity	24	35ns	35+1.0/MHz	C	P24

***I_{CC} standby for zero-power mode is 200µA**

[2]Package Codes: See section 9.0 for package drawings
C = Ceramic PIP
P = Plastic DIP
J = PLCC
N = Windowed Ceramic DIP (300 mil)

[1]Temperature range codes:
C = Commercial 0°C to +70°C
I = Industrial -40°C to +85°C

CMOS PEEL Array Selection Guide

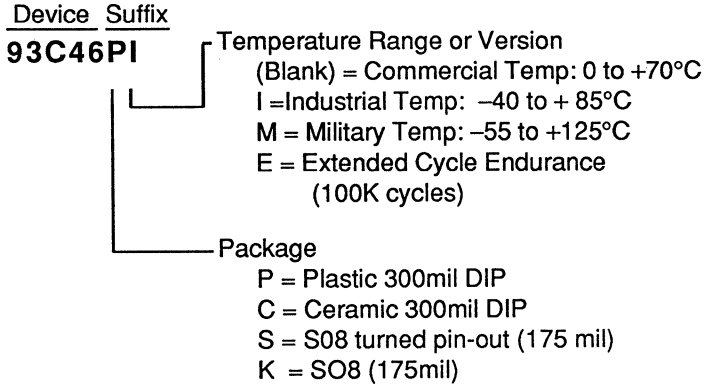
PART #	DESCRIPTION	PINS	SPEED	Icc mA	TEMP[1]	PACKAGE[2]
PA7024P-2	High density logic array	24	50MHz	100+0.5/MHz	C	P24
PA7024P-3	High density logic array	24	38.5MHz	100+0.5/MHz	C	P24
PA7024J-2	High density logic array	24	50MHz	100+0.5/MHz	C	J24
PA7024J-3	High density logic array	24	38.5MHz	100+0.5/MHz	C	J24
PA7040P-2	High density logic array	40	50MHz	120+0.5/MHz	C	P40
PA7040P-3	High density logic array	40	38.5MHz	120+0.5/MHz	C	P40
PA7040J-2	High density logic array	40	50MHz	120+0.5/MHz	C	J40
PA7040J-3	High density logic array	40	38.5MHz	120+0.5/MHz	C	J40

[2]**Package Codes:** See section 9.0 for package drawings
C = Ceramic DIP
J = PLCC
N = Windowed Ceramic DIP (300 mil)
P = Plastic DIP
S = 8 Pin SOIC
W = Windowed Ceramic DIP (600 mil)

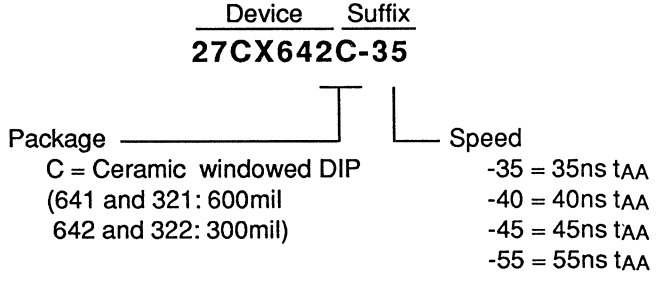
[1]**Temperature range codes:**
C = Commercial 0°C to +70°C

Ordering Information

CMOS Serial EEPROMs

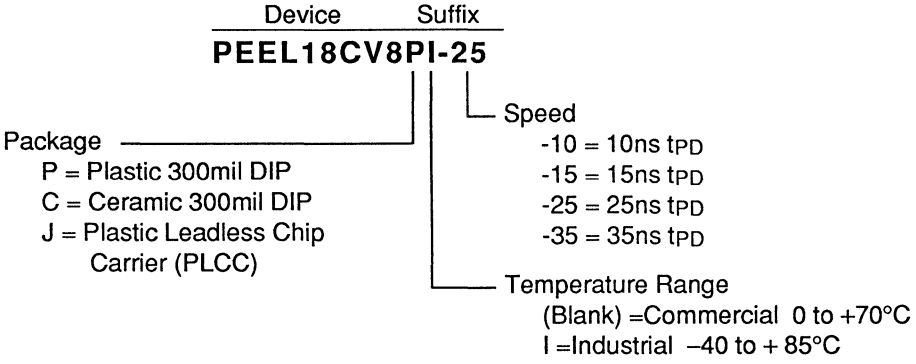


CMOS High-Speed Erasable PROMs

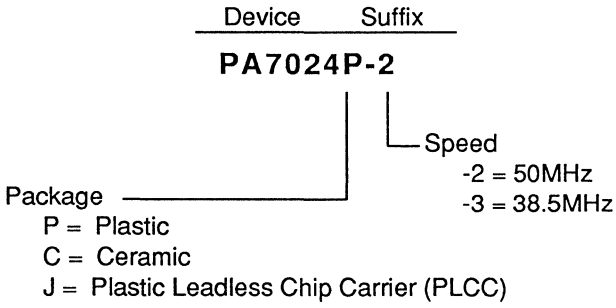


Ordering Information

CMOS PEEL Devices



CMOS PEEL Arrays



Serial EEPROM Cross Reference

Asahi ☞ ICT	NCR ☞ ICT	Rohm ☞ ICT
93CX46 .....93CX46 93CX56 .....93CX56 93CX66 .....93CX66	NCR59308 .....93C46P	BR93C46P 93C46P
Catalyst ☞ ICT	**National ☞ ICT**	**Samsung ☞ ICT**
CAT93C46P .....93C46P CAT93C46PI .....93C46PI CAT93C46K .....93C46AK CAT35C102P .....93C56AP CAT33C102P .....93C56P CAT35C104P .....93C66AP CAT33C104P 93C66P	NMC9346N .....93C46P NMC9346EN .....93C46PI NMC9346MN .....93C46PM NMC9346M .....93C46AK NMC93C46N .....93C46AP NMC93C56N .....93C56AP NMC93C66N 93C66AP	KM93C46 .....93C46P KM93C46G 93C46S
Exel ☞ ICT		**Sierra ☞ ICT**
XLS93C46P .....93C46P XLI93C46P 93C46PI	**Oki ☞ ICT**	SC2011 .....93C46P
Hyundai ☞ ICT	MSM16811 .....93C46P MSM16811GS 93C46S	**Thompson ☞ ICT**
HY93C46S .....93C46P HY93C46ES .....93C46PI HY93C46J 93C46S		TS93C46 .....93C46P

PROM and EPROM Cross Reference

AMD/MMI ☞ ICT

Am 27S43A 27CX321C-40
Am27S43 ..... 27CX321C-45

Am27S49AC 27CX641C-45
Am27S49C 27CX641C-55

63S381A 27CX321C-35
63S3281 ..... 27CX321C-45

27H010C-55 ..... 27CX010C-55
27H010C-70 ..... 27CX010C-70
27H010C-90 ..... 27CX010C-90

Atmel ☞ ICT

AT27HC641-40DC . 27CX641C-40
AT27HC641-45DC . 27CX641C-45
AT27HC641-55DC . 27CX641C-55
AT27HC642-40DC . 27CX642C-40
AT27HC642-45DC . 27CX642C-45
AT27HC642-55DC . 27CX642C-55

Cypress ☞ ICT

CY7C264-40WC ... 27CX641C-40
CY7C264-45WC ... 27CX641C-45
CY7C264-55WC ... 27CX641C-55

CY7C261-40WC ... 27CX642C-40
CY7C263-40WC ... 27CX642C-40
CY7C261-45WC ... 27CX642C-45
CY7C263-45WC ... 27CX642C-45
CY7C261-55WC ... 27CX642C-55
CY7C263-55WC ... 27CX642C-55

Fairchild ☞ ICT

93Z565AC 27CX641C-45
93Z565C 27CX641C-55

93Z667C-40 ..... 27CX642C-40
93Z667C-45 ..... 27CX642C-45
93Z667C-55 ..... 27CX642C-55

Fujitsu ☞ ICT

MB7142H 27CX321C-45

MB7144Y 27CX641C-45
MB7144H 27CX641C-40

Goldstar ☞ ICT

GM57HC64-45 .... 27CX641C-45
GM57HC64-55 .... 27CX641C-55

Harris ☞ ICT

HM-76321A-5 ..... 27CX321C-45
HM-76321-5 ..... 27CX321C-55
HM-76641A-5 ..... 27CX641C-45
HM-76641-5 ..... 27CX641C-55

National ☞ ICT

DM87S321 ..... 27CX321C-45
DM87S421 ..... 27CX322C-45

Raytheon ☞ ICT

R2971S 27CX322C-45

39VP864D 27CX641C-55
39VP865S 27CX642C-55

Signetics ☞ ICT

N82HS321A 27CX321C-35
N82HS321 ..... 27CX321C-45

N82HS641AN 27CX641C-45
N82HS641AF 27CX641C-45
N82HS641N 27CX641C-55
N82HS641FN 27CX641C-55
27HC641-55 ..... 27CX641C-55

Wafer Scale ☞ ICT

WS57C43B-35 .... 27CX321C-35
WS57C43B-45D ... 27CX321C-45
WS57C43B-35T ... 27CX321C-35
WS57C43B-45T ... 27CX321C-45

WS57C49B-40D ... 27CX641C-40
WS57C49B-45D ... 27CX641C-45
WS57C49B-55D ... 27CX641C-55
WS57C49B-40T ... 27CX641C-40
WS57C49B-45T ... 27CX641C-45
WS57C49B-55T ... 27CX641C-55

PEEL Device Cross Reference ❖

Gould AMI ☞ ICT
PEEL18CV8P-35 .. PEEL18CV8-35
PEEL18CV8-25 .... PEEL18CV8-25
PEEL20CG10-25 .. PEEL20CG10-25
PEEL20CG10-35 .. PEEL20CG10-35
PEEL22CV10-35 ... PEEL22CV10-35
PEEL22CV10-25 ... PEEL22CV10-25
PEEL22CV10Z-35 . PEEL22CV10Z-35
PEEL22CV10Z-25 . PEEL22CV10Z-25
PEEL153-35 ..... PEEL153-35
PEEL153-30 ..... PEEL153-30
PEEL173-35 ..... PEEL173-35
PEEL173-30 ..... PEEL173-30
PEEL253-35 ..... PEEL253-35
PEEL253-30 ..... PEEL253-30
PEEL273-35 ..... PEEL273-35
PEEL273-30 ..... PEEL273-30

AMD/MMI, ☞ ICT National
PAL16HD8 ..... PEEL18CV8-35
PAL16HD8L PEEL18CV8-35
PAL16HD8A PEEL18CV8-25
PAL16LD8 ..... PEEL18CV8-35
PAL16LD8L PEEL18CV8-35
PAL16LD8A PEEL18CV8-25

AMD/MMI, ☞ ICT National
PAL20L10 ..... PEEL173-35
or PEEL273-35
or PEEL20CG10-35
PAL20L10A PEEL173-30
or PEEL273-30
or PEEL20CG10-25
PAL16C1 ..... PEEL153-35
PAL16C1A2 ..... PEEL153-35
PAL10H8 ..... PEEL18CV8-35
PAL10H8A PEEL18CV8-25
PAL10H8A2 ..... PEEL18CV8-35
PAL10L8 ..... PEEL18CV8-35
PAL10L8A PEEL18CV8-25
PAL10L8A2 ..... PEEL18CV8-35
PAL12H6 ..... PEEL18CV8-35
PAL12H6A PEEL18CV8-25
PAL12H6A2 ..... PEEL18CV8-35
PAL12L6 ..... PEEL18CV8-35
PAL12L6A PEEL18CV8-25
PAL12L6A2 ..... PEEL18CV8-35
PAL14H4 ..... PEEL18CV8-35
PAL14H4A PEEL18CV8-25
PAL14H4A2 ..... PEEL18CV8-35
PAL14L4 ..... PEEL18CV8-35
PAL14L4A PEEL18CV8-25
PAL14L4A2 ..... PEEL18CV8-35
PAL16H2 ..... PEEL18CV8-35
PAL16H2A PEEL18CV8-25
PAL16H2A2 ..... PEEL18CV8-35
PAL16L2 ..... PEEL18CV8-35
PAL16L2A PEEL18CV8-25
PAL16L2A2 ..... PEEL18CV8-35

AMD/MMI, ☞ ICT National, T.I.
PAL18P8A PEEL18CV8-25
PAL16RP4A PEEL18CV8-25
PAL16RP6A PEEL18CV8-25
PAL16RP8A PEEL18CV8-25
PAL16L8 ..... PEEL18CV8-35
PAL16L8A PEEL18CV8-25*
PAL16L8A2 ..... PEEL18CV8-35
PAL16L8A4 ..... PEEL18CV8-35
PAL16L8B PEEL18CV8-15
PAL16L8B2 ..... PEEL18CV8-25
PAL16L8B4 ..... PEEL18CV8-35
PAL16R4 ..... PEEL18CV8-35
PAL16R4A PEEL18CV8-25*
PAL16R4A2 ..... PEEL18CV8-35
PAL16R4A4 ..... PEEL18CV8-35
PAL16R4B PEEL18CV8-15
PAL16R4B2 ..... PEEL18CV8-25
PAL16R4B4 ..... PEEL18CV8-35
PAL16R6 ..... PEEL18CV8-35
PAL16R6A PEEL18CV8-25*
PAL16R6A2 ..... PEEL18CV8-35
PAL16R6A4 ..... PEEL18CV8-35
PAL16R6B PEEL18CV8-15
PAL16R6B2 ..... PEEL18CV8-25
PAL16R6B4 ..... PEEL18CV8-35
PAL16R8 ..... PEEL18CV8-35
PAL16R8A PEEL18CV8-25*
PAL16R8A2 ..... PEEL18CV8-35
PAL16R8A4 ..... PEEL18CV8-35
PAL16R8B PEEL18CV8-15
PAL16R8B2 ..... PEEL18CV8-25
PAL16R8B4 ..... PEEL18CV8-35

❖ PEEL devices may be used as direct replacements for the PLDs indicated without modifying the original design. The original design is translated to an equivalent PEEL design by using ICT's JEDEC file translator (provided in the free PEEL Development software).

1

AMD/MMI ☞ ICT National, T.I.

PAL20L8A PEEL20CG10-25
PAL20L8A2 .....PEEL20CG10-35
or PEEL173-35
or PEEL273-35

PAL20R4A PEEL20CG10-25
PAL20R4A2 .....PEEL20CG10-35

PAL20R6A PEEL20CG10-25
PAL20R6A2 .....PEEL20CG10-35

PAL20R8A PEEL20CG10-25
PAL20R8A2 .....PEEL20CG10-35

PAL12L10 .....PEEL173-35
or PEEL273-35
or PEEL20CG10-35

PAL14L4 .....PEEL173-35
or PEEL273-35
or PEEL20CG10-35

PAL16L6 .....PEEL173-35
or PEEL273-35
or PEEL20CG10-35

PAL18L4 .....PEEL173-35
or PEEL273-35
or PEEL20CG10-35

PAL20L2 .....PEEL173-35
or PEEL273-35
or PEEL20CG10-35

Altera ☞ ICT

EP310 .....PEEL18CV8-35
EP310-2 .....PEEL18CV8-35
EP310I PEEL18CV8I-45

EP320 .....PEEL18CV8-35
EP320-2 .....PEEL18CV8-35
EP320-1 .....PEEL18CV8-25
EP320I PEEL18CV8I-35

Cypress ☞ ICT

PALC16L8-25 .....PEEL18CV8-25
PALC16L8-35 .....PEEL18CV8-35

PALC16R4-25 .....PEEL18CV8-25
PALC16R4-35 .....PEEL18CV8-35

PALC16R6-25 .....PEEL18CV8-25
PALC16R6-35 .....PEEL18CV8-35

PALC16R8-25 .....PEEL18CV8-25
PALC16R8-35 .....PEEL18CV8-35

PALC20G10-25 ....PEEL20CG10-25
PALC20G10-35 ....PEEL20CG10-35

PALC22V10-25† PEEL22CV10-25
PALC22V10-35† PEEL22CV10-35

Intel ☞ ICT

5C031 .....PEEL18CV8-35

5C032 .....PEEL18CV8-35

Signetics ☞ ICT

PLHS18P8A PEEL18CV8-25

PLS153† PEEL153-35
or PEEL253-35

PLS153A† PEEL153-30
or PEEL253-30

PLS173† PEEL173-30
or PEEL273-30

Lattice ☞ ICT National

GAL16V8-15L PEEL18CV8-15
GAL16V8-25L PEEL18CV8-25
GAL16V8-25Q PEEL18CV8-25
GAL16V8-35L PEEL18CV8-35
GAL16V8-35Q PEEL18CV8-35

GAL20V8-25 .....PEEL20CG10-25
GAL20V8-35 .....PEEL20CG10-35

† Devices marked with this symbol are JEDEC-file compatible with the PEEL device referenced. No translation is required to use a PEEL device as a direct replacement.

* Consult factory for other speed options.

CMOS Serial EEPROMs

CMOS Serial EEPROMs

The ICT CMOS Serial EEPROMs provide a practical solution for today's CMOS systems requiring non-volatile data storage. All ICT serial EEPROMs can easily be interfaced with the popular micro-controllers and processors.

CMOS Serial EEPROM Features

- **CMOS EEPROM Technology**
  - — Retains data after power is removed
- **Space-saving 8-pin Package**
  - — Interfaced with three to four lines
- **Extended-voltage operation (2.5 to 6.0V)**
  - — Ideal for battery-powered applications
- **Stores 1K to 4K bits of Non-Volatile Data**
  - — 93C46, 93C46A, 93CX46: 64 x 16 (1K bits)
  - — 93C56A, 93CX56: 128 x 16 (2K bits)
  - — 93C66A, 93CX66: 256 x 16 (4K bits)
- **Software and hardware controlled write protection**
- **Low Power Consumption**
  - — 1mA to 4mA Icc Active
  - — 50μA to 100μA Icc Standby
- **Several Versions Available**
  - — Commercial, Industrial, and Military temperatures
  - — Plastic/Ceramic DIP and SO8 packaging
  - — 10,000 and 100,000 erase/write cycles

INTERNATIONAL CMOS
TECHNOLOGY, INC.

93C46
1,024-Bit Serial (5V only) CMOS Electrically Erasable Programmable Read Only Memory (EEPROM)

Features

- **Advanced CMOS EEPROM Technology**
- **Read/Write Non-volatile Memory**
  - Single 5V supply operation
  - 1,024 bits, 64 x 16 organization
  - Versatile, easy to use serial data interface
- **Low Power Consumption**
  - 3mA max Active
  - 1mA max Standby, TTL interface
  - 100µA max Standby, CMOS interface
- **Special Features**
  - Automatic write cycle time-out
  - Ready/Busy status signal
  - Software controlled write protection
- **Ideal For Low-Density Data Storage**
  - Low cost, space saving, 8-pin package
  - Commercial, industrial, & military versions
  - Interfaces with popular microcomputers (ie., COP4XX, 8048, 8049, 8051, 8096, 6805, 6801, TMS1000, Z8)
- **Application Versatility**
  - Alarms, Electronic Locks, Appliances, Terminals, Smart Cards, Robotics, Meters, Telephones, Tuners, etc.
- **Reliability**
  - 10,000 or 100,000 erase/write cycles
  - Over 40 year data retention[1]

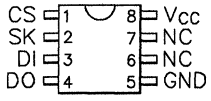
General Description

The ICT 93C46 is a 1,024-bit, 5V-only, serial read/write, non-volatile memory device fabricated using an advanced CMOS EEPROM technology. Its 1,024 bits of memory are organized into 64 registers each. Each register is individually addressable for serial read or write operations. A versatile serial interface consisting of chip select, clock, data-in and data-out, can easily be controlled by popular microcomputers (ie., COP4XX, 8048, 8049, 8051, 6805, 6801, TMS1000,Z8) or standard microprocessors.

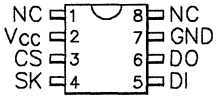
Low power consumption, low cost, and space efficiency make the ICT 93C46 an ideal candidate for high volume, low density data storage applications. Special features of the 93C46 include: automatic write time-out, ready/busy status signal, software controlled write protection, and ultra-low standby power mode when deselected (CS low). Additionally, the 93C46 offers functional compatibility with existing NMOS serial EEPROMs. The 93C46 is designed for applications requiring 10,000 or 100,000 erase/write cycles per register.

Connection Diagrams

DIP Package

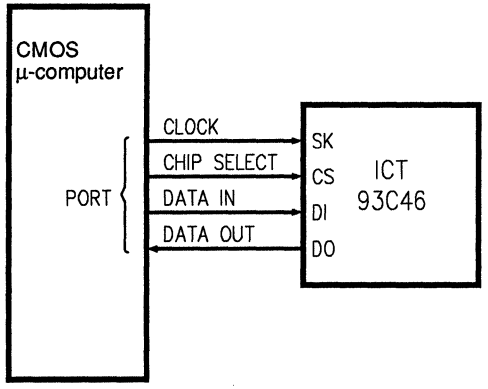


SO8 Package



Pin Names

CS	= Chip Select
SK	= Serial Data Clock
DI	= Serial Data Input
DO	= Serial Data Output
GND	= Ground
Vcc	= Power Supply
NC	= Not Connected



Interfacing the 93C46

Function Description

Device Operation

The ICT 93C46 is a serial 1,024-bit non-volatile memory device organized as 64 registers by 16 bits. Each register is independently addressable for read, write, or erase operations. Seven, 9-bit instructions control the operation of the device. These instructions are clocked into the data input (DI) pin in a serial fashion as controlled by the chip select (CS) and serial data clock (SK) inputs. The instructions include: read; write; erase; erase/write enable; erase/write disable; write all; and erase all registers.

The format of each 9-bit instruction-starting with the most significant bit-is as follows: start bit (logical "1"); a two-bit op code; and an eight-bit address. The DO pin is normally in a high-impedance state, except when reading data from the device, or when checking the BUSY/READY status after a programming operation. The BUSY/READY status can be determined after a programming operation by selecting the device (CS high) and polling the DO pin. DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready for the next operation. DO will return to the high-impedance state when the next instruction is initiated.

The 93C46 operates on a single supply voltage, which may range from 4.5 Volts to 5.5 Volts, and will generate, on chip, the high voltage required for any programming operation.

Read (READ)

The read (READ) instruction outputs serial data on the DO pin. After a read instruction is received, the instruction and the address are decoded. Then data is transferred from the selected memory register to a 16-bit shift register and DO comes out of the high-impedance state. After sending a dummy bit (logical "0"), the 16-bit data string is shifted out of the device. The DO transitions occur on the rising edge of the clock and the data is stable after the specified delay t_{PO} or t_{PD1}.

Erase/Write Enable and Disable (EWEN and EWDS)

The 93C46 powers up in the programming-disable state. Any programming after power-up, or following a write disable (WDS) instruction, must first be preceded by a write enable (WEN) instruction. Once enabled, programming remains enabled until a write disable (WDS) instruction is executed or power is removed from the device. The write disable instruction disables all programming functions of the 93C46 and can be used to prevent accidentally disturbing data in the device. Data can be read from the 93C46 regardless of the programming enable/disable status.

Erase (ERASE)

It is necessary to erase each register (all bits set to logical "1") before writing to it (certain bits set to logical "0"). After receiving the erase instruction, CS (chip select) must be held low for a minimum period specified by t_{CS}. After inputting an erase instruction, the falling edge of CS initiates the self-timed write cycle. After observing t_{CS}, the READY/BUSY status of the device can be determined by selecting the device and polling the DO pin.

Write (WRITE)

The write instruction (opcode plus address to be written to) is followed by 16 bits of data to be written into the specified address. After the last bit of data (D_O) has been clocked into the DI pin, the CS (chip select) must be brought low before the next rising edge of the SK clock and held low for the minimum period specified by t_{CS}. The falling edge of CS initiates the self-timed programming cycle. It is not necessary to clock the SK pin after initiating the self-timed write mode. The READY/BUSY status of the device can be determined by selecting the device and polling the DO pin.

Write All (WRAL)

The write-all (WRAL) instruction simultaneously programs all registers with the data pattern specified in the instruction. After receiving the write-all instruction and 16 bits of data, CS (chip select) must be held low for a minimum period specified by t_{CS}. The falling edge of CS initiates the self-timed write cycle. It is not necessary to clock the SK pin after initiating the self-timed write-all mode. The BUSY/READY status of the device can be determined by selecting the device and polling the DO pin.

Erase All (ERAL)

Entire chip erasing is provided for ease of programming. The erase-all (ERAL) instruction simultaneously programs every bit on the chip to a logical "1". After receiving the erase-all instruction, CS (chip select) must be held low for a minimum period specified by t_{CS}. The falling edge of CS initiates the self-timed write cycle. It is not necessary to clock the SK pin after initiating the self-timed erase-all mode. The BUSY/READY status of the device can be determined by selecting the device and polling the DO pin.

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	– 0.6 to +7.0	V
V_{IO}	Voltage Applied to Any Pin	Relative to GND	– 0.6 to V_{CC} + 0.6	V
T_{ST}	Storage Temperature		– 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Commercial		Industrial		Military		Unit
		93C46		93C46 I		93C46 M		
		Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
T_A	Ambient Temperature[1]	0	+ 70	– 40	+ 85	– 55	+ 125	°C

DC and AC Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	93C46		93C46 I		93C46 M		Unit
			Min	Max	Min	Max	Min	Max	
I_{CC}	Power Supply Current, Active, TTL/CMOS Interface	V_{CC} = 5.5V, CS=SK=V_{IH} DO = Open, f = 250 KHz		3		6		7	mA
I_{CCSB1}	Supply Current, Standby, TTL/CMOS Interface	V_{CC} = 5.5V, CS = V_{IL} DO = Open		1		3		3	mA
I_{CCSB2}	Supply Current, Standby, CMOS Interface			100		100		100	µA
V_{IH}	Input HIGH Level		2.0	V_{CC}+1	2.0	V_{CC}+1	2.0	V_{CC}+1	V
V_{IL}	Input LOW Level		– 0.1	0.8	– 0.1	0.8	– 0.1	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = – 0.4mA	2.2		2.2		2.2		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1mA		0.4		0.4		0.4	V
I_{LI}	Input Leakage Current	V_{IN} = 5.5V		10		10		10	µA
I_{LO}	Output Leakage Current	V_O=5.5V, CS=0, $V_{CC} \leq$ 5.5V		10		10		10	µA
t_{SKP}	SK Period		4	0	4	0	4	0	µs
t_{SKW}	SK Pulse Width	High or Low	1		1		1		µs
t_{CSS}	CS High to SK High Delay		200		200		200		ns
t_{CSH}	SK Low to CS Low Delay		0		0		0		ns
t_{DIS}	Data Setup Time (Write)		400		400		400		ns
t_{DIH}	Data Hold Time (Write)		400		400		400		ns
t_{PD1} / t_{PD0}	Serial Clock to Output Delay	C_L = 100pF, V_{OL} = 0.8V, V_{OH} = 2.0V, V_{IL} = 0.45V, VIH = 2.4V		2		2		2	µs
$t_{E/W}$	Self-timed Program Cycle [2]			10		10		10	ms
t_{CS}	Min CS Low Time		1		1		1		µs
t_{SV}	CS to Status Valid	CL = 100pF		1		1		1	µs
t_{OH}, t_{IH}	Falling Edge of CS to DO High Impedence			400		400		400	ns

Notes

1. ICT's E^2 devices are designed to endure 10,000 or 100,000 (93C46E) Erase/Write cycles and to retain data for at least forty years while operating at 55°C. ICT's standard test flow verifies at least ten years of data retention for Commercial and Industrial temperature devices and at least two years data retention for Military temperature devices. Data retention verification is performed on 100% of the units being shipped. Cycling endurance is verified by lot sample testing.

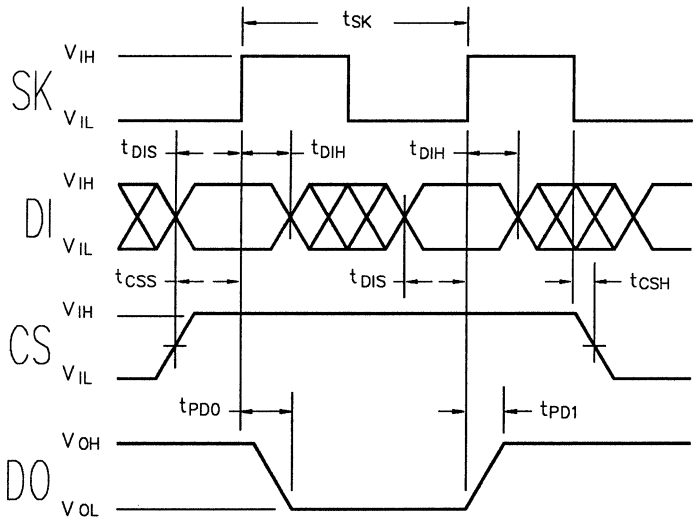
2. Although the 93C46 self-timed program cycle allows software delay loops to be used to achieve the necessary Erase/Write delay, using the Ready/Busy feature is recommended instead. Using the Ready/Busy feature allows faster response time since TE/W will typically be less than the maximum specification.

2

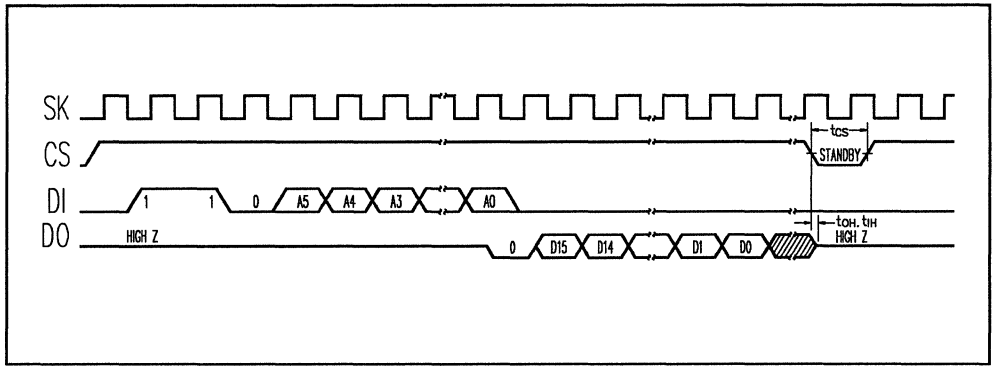
Instruction set for the 93C46

Instruction	Start Bit	Opcode	Address	Data	Comments
READ	1	10	$A_5A_4A_3A_2A_1A_0$		Read address
WRITE	1	01	$A_5A_4A_3A_2A_1A_0$	D_{15} - D_0	Write to address
ERASE	1	11	$A_5A_4A_3A_2A_1A_0$		Erase address
EWEN	1	00	1 1 X X X X		ERASE/WRITE enable
EWDS	1	00	0 0 X X X X		ERASE/WRITE disable
ERAL	1	00	1 0 X X X X		Erase all addresses
WRAL	1	00	0 1 X X X X	D_{15} - Do	Write all addresses

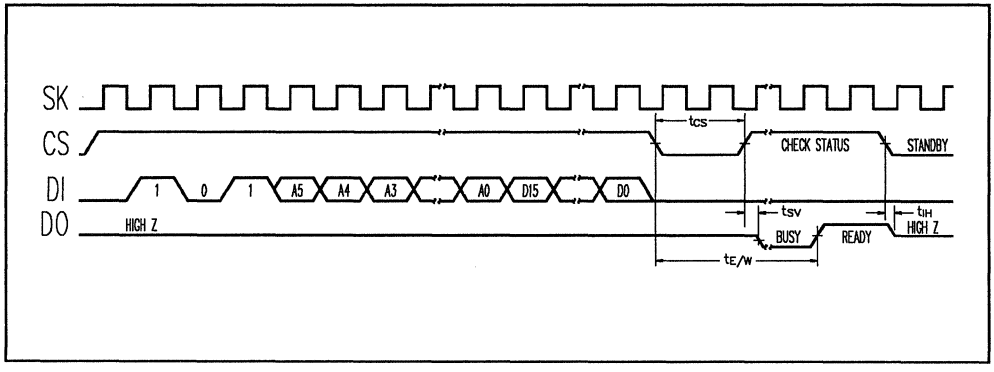
Synchronous Data Timing Waveforms



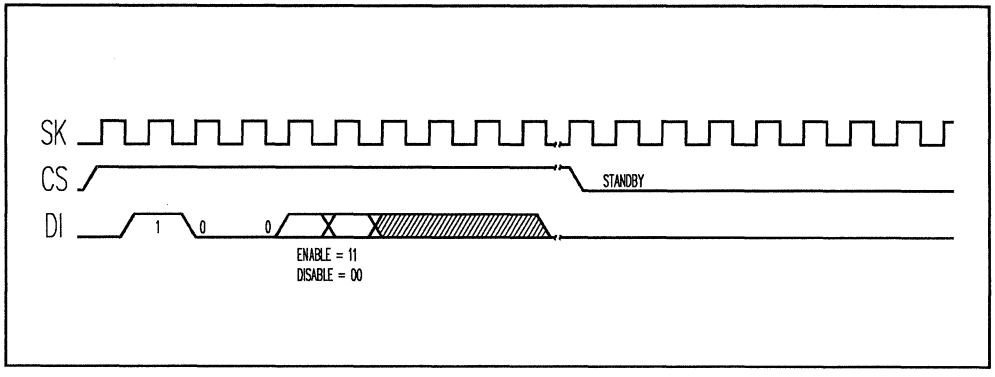
Read Cycle (READ) Timing Diagram



Write Cycle(WRITE) Timing Diagram

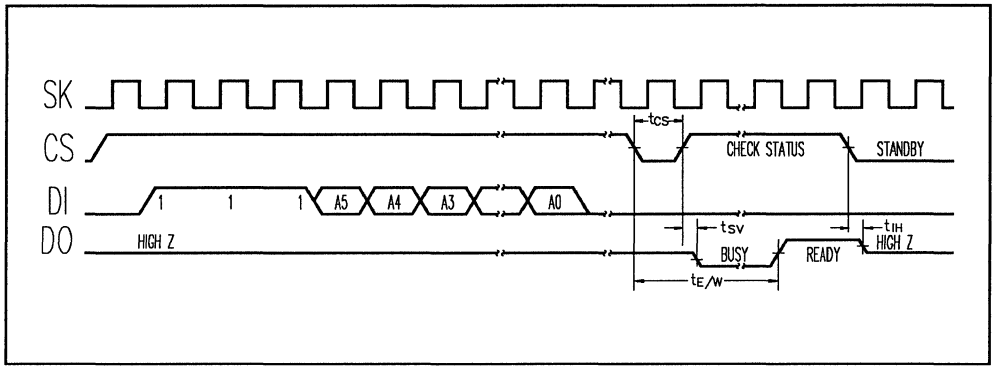


ERASE/WRITE Enable (EWEN), ERASE/WRITE Disable

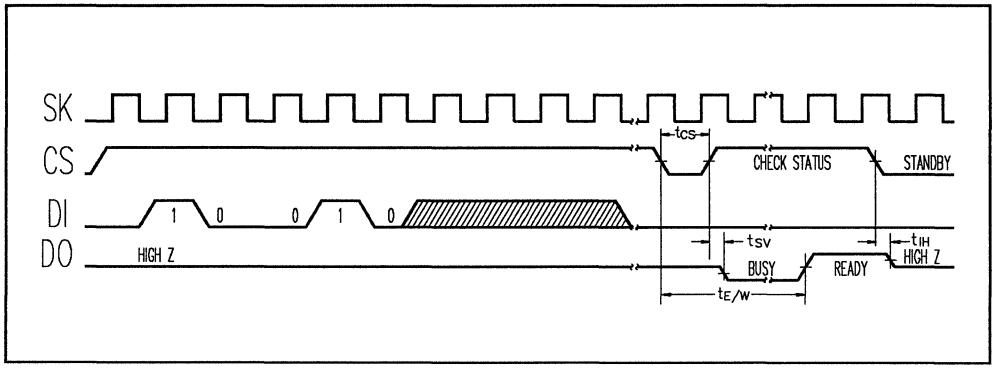


2

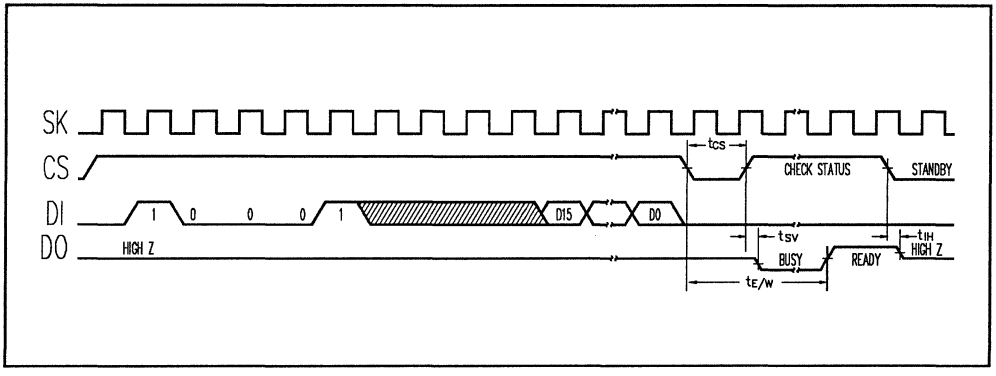
Erase (ERASE)Timing Diagram



Erase All (ERAL) Timing Diagram



Write All (WRAL) Timing Diagram



93C46A
1,024-Bit Serial (5V only) CMOS Electrically Erasable Programmable Read Only Memory (EEPROM)

Features

- **Advanced CMOS EEPROM Technology**
- **Read/Write Non-volatile Memory**
  - Single 5V supply operation
  - 1,024 bits: 64 x 16 organization
  - Versatile, easy to use serial data interface
- **Low Power Consumption**
  - 3mA max Active
  - 1mA max Standby, TTL interface
  - 100µA max Standby, CMOS interface
- **Special Features**
  - Automatic-erase write instruction
  - Ready/Busy status signal
  - Software and hardware controlled write protection
- **Ideal For Low-Density Data Storage**
  - Low cost, space saving, 8-pin package
  - Commercial, industrial, & military versions
  - Interfaces with popular microcomputers (ie., COP4XX, 8048, 8049, 8051, 8096, 6805, 6801, TMS1000, Z8)
- **Application Versatility**
  - Alarms, Electronic Locks, Appliances, Terminals, Smart Cards, Robotics, Meters, Telephones, Tuners, etc.
- **Reliability**
  - 10,000 erase/write cycles
  - Over 40 year data retention[1]

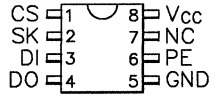
General Description

The ICT 93C46A is a 1,024-bit, 5V-only, serial read/write, non-volatile memory device fabricated using an advanced CMOS EEPROM technology. Its 1,024 bits of memory are organized into 64 registers each. Each register is individually addressable for serial read or write operations. A versatile serial interface consisting of chip select, clock, data-in and data-out, can easily be controlled by popular microcomputers (ie., COP4XX, 8048, 8049, 8051, 6805, 6801, TMS1000,Z8) or standard microprocessors.

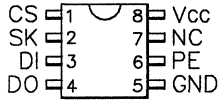
Low power consumption, low cost, and space efficiency make the ICT 93C46A an ideal candidate for high volume, low density data storage applications. Special features of the 93C46A include: automatic write time-out, ready/busy status signal, software controlled write protection, and ultra-low standby power mode when deselected (CS low). Additionally, the 93C46A offers functional compatibility with existing NMOS and CMOS serial EEPROMs. The 93C46A is designed for applications requiring 10,000 erase/write cycles per register and 40 years of data retention.

Connection Diagrams

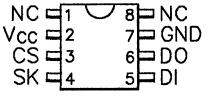
DIP Package



SO8 Package(K)

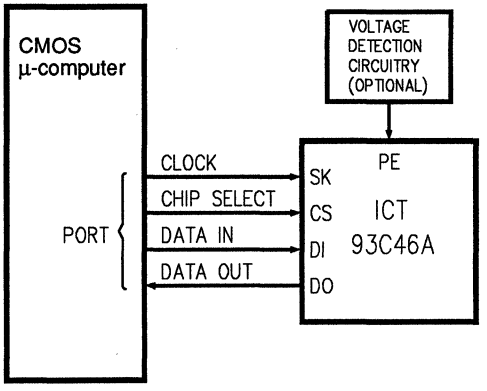


SO8 Package(S)



Pin Names

CS	= Chip Select
SK	= Serial Data Clock
DI	= Serial Data Input
DO	= Serial Data Output
PE	= Program Enable
GND	= Ground
Vcc	= Power Supply



Interfacing the 93C46A

Function Description

Device Operation[2]

The ICT 93C46A is a serial 1,024-bit non-volatile memory device organized as 64 registers by 16 bits. Each register is independently addressable for read, write, or erase operations. Five, 9-bit instructions control the operation of the device. The 93C46A operates on a single 5 Volt supply, and will generate, on chip, the high voltage required for any programming operation.

The 93C46A provides two methods of protecting data from being accidentally disturbed. The erase/write-disable (EWDS) instruction will disable all programming functions until an erase/write-enable (EWEN) instruction is executed. A hardware control is also available in the form of the PE (program enable) control pin. To perform any programming instruction, PE must be held high while loading the instruction into the 93C46A. The PE control can be used to ensure that no data is accidentally disturbed by erratic switching of the microcontroller's outputs during power-up or power-down. Voltage detection circuitry can be implemented to disable PE when the supply voltage drops below a user-specified voltage level. Note that the PE control pin is tied to an internal pull-up so that the pin may be left unconnected if the PE control feature is not to be used.

Instructions, address, and write data are clocked into the DI pin on the rising edge of the clock (SK). The instructions include: read; write; erase/write enable, erase/write disable; erase all; and write all. The format of each 9-bit instructions-starting with the most significant bit-is as follows: start bit (logical "1"); a two-bit op code; and an eight-bit address. The DO pin is normally in a high-impedance state, except when reading data from the device, or when checking the BUSY/READY status after a programming operation. The BUSY/READY status can be determined after a programming operation by selecting the device (CS high) and polling the DO pin. DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready for the next operation. DO will return to the high-impedance state when the next instruction is initiated.

Read (READ)

The read (READ) instruction outputs serial data on the DO pin. After a read instruction is received, the instruction and the address are decoded. Then data is transferred from the selected memory register to a 16-bit shift register and DO comes out of the high-impedance state. After sending a dummy bit (logical "0"), the 16-bit data string is shifted out of the device. The DO transitions occur on the rising edge of the clock and the data is stable after the specified delay t_{PO} or t_{PD1}.

Write Enable and Disable[3] (WEN and WDS)

The 93C46A powers up in the programming-disable state. Any programming after power-up, or following a write disable (WDS) instruction, must first be preceded by a write enable (WEN) instruction. The PE pin **MUST** be held high while loading the programming enable instruction. Once enabled, programming remains enabled until a write disable (WDS) instruction is executed or power is removed from the device. The write disable instruction disables all programming functions of the 93C46A and can be used to prevent accidentally disturbing data in the device. Data can be read from the 93C46A regardless of the programming enable/disable status.

Write (WRITE)[3]

The 93C46A initiates an autoerase cycle when executing a write (WRITE) instruction, eliminating the need of an erase (ERASE) command. The write instruction (opcode plus address) is followed by 16 bits of data to be written into the specified address. After the last bit of data (D_0) has been clocked into the DI pin, the CS (chip select) must be brought low before the next rising edge of the SK clock and held low for the minimum period specified by t_{CS}. The falling edge of CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the write instruction. However, after loading the write instruction the PE pin becomes a "don't care". It is not necessary to clock the SK pin after initiating the self-timed write mode. The READY/BUSY status of the device can be determined by selecting the device and polling the DO pin.

Write All (WRAL)[3]

The write-all (WRAL) instruction simultaneously programs all registers with the data pattern specified in the instruction. After receiving the write-all instruction and 16 bits of data, CS (chip select) must be held low for a minimum period specified by t_{CS}. The falling edge of CS initiates the self-timed write cycle. The PE pin **MUST** be held high while loading the write-all instruction. It is not necessary to clock the SK pin after initiating the self-timed write-all mode. The BUSY/READY status of the device can be determined by selecting the device and polling the DO pin.

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	– 0.6 to +7.5	V
V_{IO}	Voltage Applied to Any Pin	Relative to GND	– 0.6 to V_{CC} + 0.6	V
T_{ST}	Storage Temperature		– 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Commercial 93C46A		Industrial 93C46A I		Military 93C46A M		Unit
		Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
T_A	Ambient Temperature[1]	0	+ 70	– 40	+ 85	– 55	+ 125	°C

DC and AC Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	93C46A		93C46A I		93C46A M		Unit
			Min	Max	Min	Max	Min	Max	
I_{CC}	Power Supply Current, Active, TTL/CMOS Interface	V_{CC} = 5.5V, CS=SK=V_{IH} DO = Open, f = 2.0MHz		3		5		7	mA
I_{CCSB1}	Supply Current, Standby, TTL Interface	V_{CC} = 5.5V, CS = V_{IL} DO = Open		100		150		200	µA
I_{CCSB2}	Supply Current, Standby, CMOS Interface	V_{CC} = 5.5V, CS = V_{IL} DO = Open		50		100		200	µA
V_{IH}	Input HIGH Level		2.0	V_{CC}+1	2.0	V_{CC}+1	2.0	V_{CC}+1	V
V_{IL}	Input LOW Level		– 0.1	0.8	– 0.1	0.8	– 0.1	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = – 0.4mA (note 2)	2.2		2.2		2.2		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1mA (note 2)		0.4		0.4		0.4	V
I_{LI}	Input Leakage Current	V_{IN} = 5.5V		±10		±10		±10	µA
I_{LO}	Output Leakage Current	V_O=5.5V, CS=0, $V_{CC} \leq$ 5.5V		±10		±10		±10	µA
t_{SKP}	SK Period		500		500		500		ns
t_{SKW}	SK Pulse Width	High or Low	250		250		250		ns
t_{CSS}	CS High to SK High Delay		100		100		100		ns
t_{CSH}	SK Low to CS Low Delay		0		0		0		ns
t_{DIS}	Data Setup Time (Write)		200		200		200		ns
t_{DIH}	Data Hold Time (Write)		200		200		200		ns
t_{PD1} / t_{PD0}	Serial Clock to Output Delay	C_L = 100pF, V_{OL} = 0.8V, V_{OH} = 2.0V, V_{IL} = 0.45V, VIH = 2.4V		250		250		250	ns
$t_{E/W}$	Self-timed Program Cycle[4]			10		10		20	ms
t_{CS}	Min CS Low Time		250		250		250		ns
t_{SV}	CS to Status Valid	CL = 100pF		500		1000		1000	ns
t_{OH}, t_{IH}	Falling Edge of CS to DO High Impedence			100		200		200	ns

Notes

Note 1. ICT's E^2 devices are designed to endure 10,000 Erase/Write cycles and to retain data for at least forty years while operating at 55°C. ICT's standard test flow verifies at least ten years of data retention for Commercial and Industrial temperature devices and at least two years data retention for Military temperature devices. Data retention verification is performed on 100% of the units being shipped. Cycling endurance is verified by lot-sample testing.

Note 2. If the power is removed or the CS pin is brought low during an instruction cycle, the device's instruction registers will be reset. Note that a power-down will totally reset the device. This means that the write-enable instruction (WEN) will need to be executed prior to any programming.

Note 3. If the PE pin is brought to low during the loading of the instruction, this instruction (WEN, WDS, WRITE, and WRAL) may not be executed reliably.

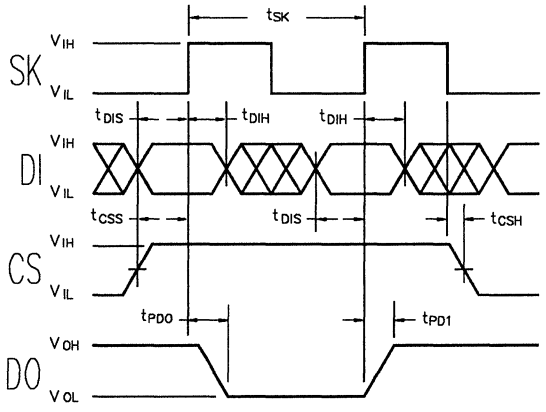
Note 4. Although the 93C46A self-timed program cycle allows software delay loops to be used to achieve the necessary Erase/Write delay, using the Ready/Busy feature is recommended instead. Using the Ready/Busy feature allows faster response time since $t_{E/W}$ will typically be less than the maximum specification.

2

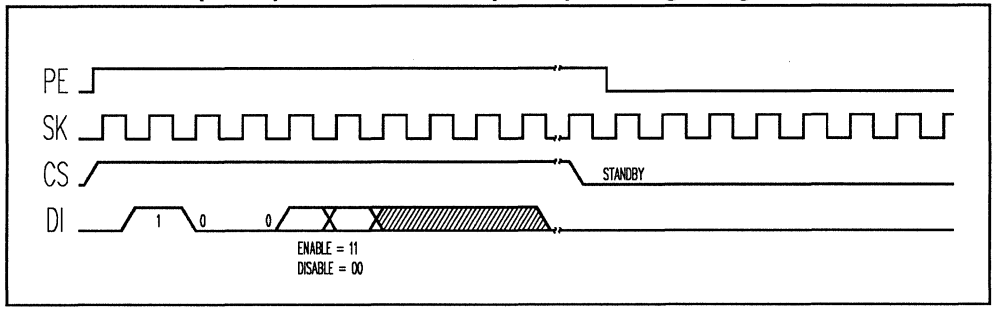
Instruction set for the 93C46A

Instruction	Start Bit	Opcode	Address	Data	Comments
READ	1	10	$A_5A_4A_3A_2A_1A_0$		Read address
WRITE	1	01	$A_5A_4A_3A_2A_1A_0$	D_{15} - D_0	Write to address
WEN	1	00	1 1 X X X X		Write enable
WDS	1	00	0 0 X X X X		Write disable
WRAL	1	00	0 1 X X X X	D_{15} - D_0	Write all addresses

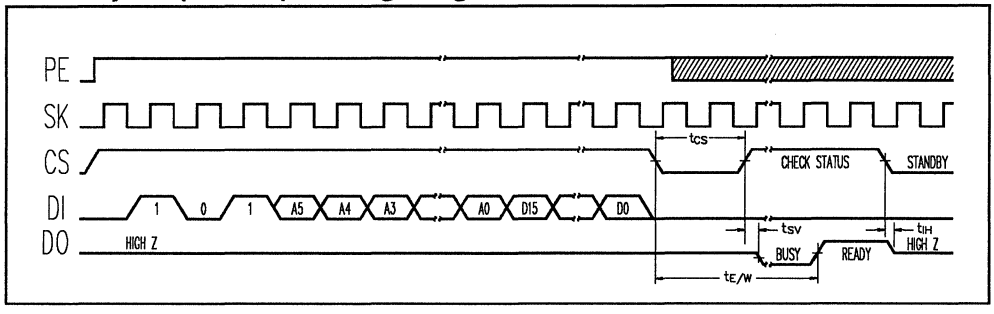
Synchronous Data Timing Waveforms



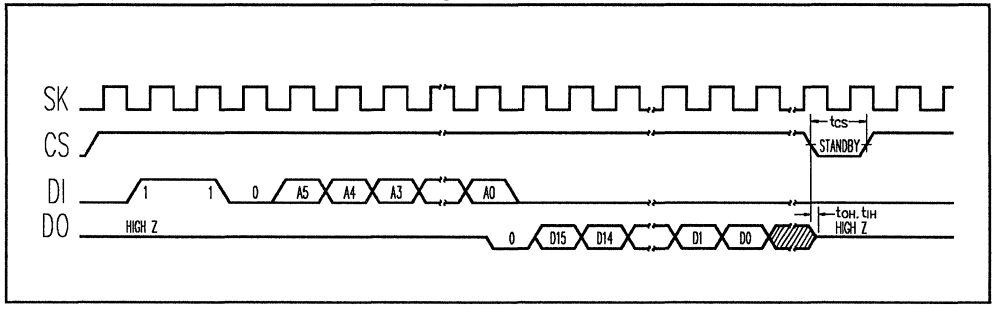
Write Enable (WEN)/Write Disable (WDS) Timing Diagram



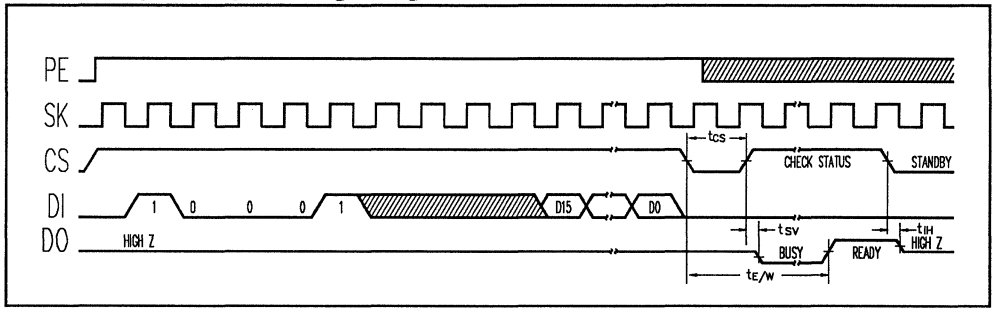
Write Cycle (WRITE) Timing Diagram



Read Cycle (READ) Timing Diagram



Write All (WRAL) Timing Diagram



93C56A/C66A

2,048/4,096-Bit Serial (5V only) CMOS Electrically Erasable Programmable Read Only Memory (EEPROM)

Features

- **Advanced CMOS EEPROM Technology**
- **Read/Write Non-volatile Memory**
  - — Single 5V supply operation
  - — 2,048 bits: 128 x 16 organization
  - — 4,096 bits: 256 x 16 organization
  - — Versatile, easy to use serial data interface
- **Low Power Consumption**
  - — 3mA max Active
  - — 1mA max Standby, TTL interface
  - — 100µA max Standby, CMOS interface
- **Special Features**
  - — Automatic-erase write instruction
  - — Ready/Busy status signal
  - — Software and hardware controlled write protection
- **Ideal For Low-Density Data Storage**
  - — Low cost, space saving, 8-pin package
  - — Commercial, industrial, & military versions
  - — Interfaces with popular microcomputers (ie., COP4XX, 8048, 8049, 8051, 8096, 6805, 6801, TMS1000, Z8)
- **Application Versatility**
  - — Alarms, Electronic Locks, Appliances, Terminals, Smart Cards, Robotics, Meters, Telephones, Tuners, etc.
- **Reliability**
  - — 10,000 erase/write cycles
  - — Over 40 year data retention[1]

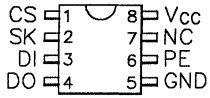
General Description

The ICT 93C56A/C66A is a 2,048/4,096-bit, 5V-only, serial read/write, non-volatile memory device fabricated using an advanced CMOS EEPROM technology. Its 2,048/4,096 bits of memory are organized into 128/256 registers each. Each register is individually addressable for serial read or write operations. A versatile serial interface consisting of chip select, clock, data-in and data-out, can easily be controlled by popular microcomputers (ie., COP4XX, 8048, 8049, 8051, 6805, 6801, TMS1000,Z8) or standard microprocessors.

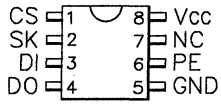
Low power consumption, low cost, and space efficiency make the ICT 93C56A/C66A an ideal candidate for high volume, low density data storage applications. Special features of the 93C56A/C66A include: automatic write time-out, ready/busy status signal, software controlled write protection, and ultra-low standby power mode when deselected (CS low). Additionally, the 93C56A/C66A offers functional compatibility with existing NMOS serial EEPROMs. The 93C56A/C66A is designed for applications requiring 10,000 erase/write cycles per register and 40 years of data retention.

Connection Diagrams

DIP Package

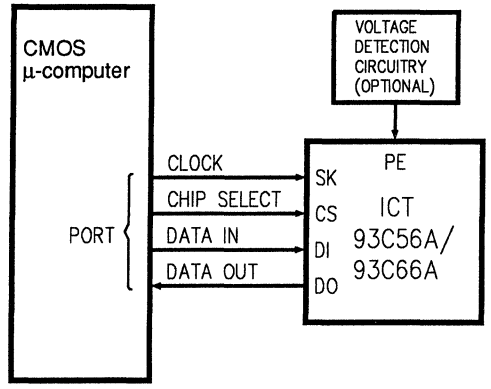


SO8 Package



Pin Names

CS	= Chip Select
SK	= Serial Data Clock
DI	= Serial Data Input
DO	= Serial Data Output
PE	= Program Enable
GND	= Ground
Vcc	= Power Supply



Interfacing the 93C56A/C66A

Function Description

Device Operation [2]

The ICT 93C56A/C66A are serial 2,048/4,096-bit non-volatile memory devices organized as 128/256 registers by 16 bits. Each register is independently addressable for read, write, or erase operations. Five, 11-bit instructions control the operation of the device. The 93C56A/C66A operates on a single 5 Volt supply, and will generate, on chip, the high voltage required for any programming operation.

The 93C56A/C66A provides two methods of protecting data from being accidentally disturbed. The Write-Disable (WDS) instruction will disable all programming functions until an Write-Enable (WEN) instruction is executed. A hardware control is also available in the form of the PE (program enable) control pin. To perform any programming instruction, PE must be held high while loading the instruction into the 93C56A/C66A. The PE control can be used to ensure that no data is accidentally disturbed by erratic switching of the microcontroller's outputs during power-up or power-down. Voltage detection circuitry can be implemented to disable PE when the supply voltage drops below a user-specified voltage level. Note that the PE control pin is tied to an internal pull-up so that the pin may be left unconnected if the PE control feature is not to be used.

Instructions, address, and write data are clocked into the DI pin on the rising edge of the clock (SK). The instructions include: read; write; write enable, write disable; and write all. The format of each eleven-bit instruction, starting with the most significant bit, is as follows: start bit (logical "1"); a two-bit op code; and an eight-bit address(one "Don't Care" bit and seven address bits for the 93C56A). The DO pin is normally in a high-impedance state, except when reading data from the device, or when checking the BUSY/READY status after a programming operation. The BUSY/READY status can be determined after a programming operation by selecting the device (CS high) and polling the DO pin. DO low indicates that the programming operation is not completed (BUSY), while DO high indicates that the device is ready for the next operation (READY). DO will return to the high-impedance state when the next instruction is initiated.

Read (READ)

The read (READ) instruction outputs serial data on the DO pin. After a read instruction is received, the instruction and the address are decoded. Then data is transferred from the selected memory register to a 16-bit shift register and DO comes out of the high-impedance state. After sending a dummy bit (logical "0"), the 16-bit data string is shifted out of the device. The DO transitions occur on the rising edge of the clock and the data is stable after the specified delay t_{PO} or t_{PD1}.

Write Enable/Disable [3] (WEN /WDS)

The 93C56A/C66A powers up in the programming-disable state. Any programming after power-up, or following a write disable (WDS) instruction, must first be preceded by a write enable (WEN) instruction. The PE pin (if used) **MUST** be held high while loading the programming enable instruction. Once enabled, programming remains enabled until a write disable (WDS) instruction is executed or power is removed from the device. The write disable instruction disables all programming functions of the 93C56A/C66A and can be used to prevent accidentally disturbing data in the device. Data can be read from the 93C56A/C66A regardless of the programming enable/disable status.

Write (WRITE) [3]

The 93C56A/C66A initiates an autoerase cycle when executing a write (WRITE) instruction, eliminating the need of an erase (ERASE) command. The write instruction (opcode plus address) is followed by 16 bits of data to be written into the specified address. After the last bit of data (D_O) has been clocked into the DI pin, the CS (chip select) must be brought low before the next rising edge of the SK clock and held low for the minimum period specified by t_{CS}. The falling edge of CS initiates the self-timed programming cycle. The PE pin (if used) **MUST** be held high while loading the write instruction. However, after loading the write instruction the PE pin becomes a "don't care". It is not necessary to clock the SK pin after initiating the self-timed write mode. The READY/BUSY status of the device can be determined by selecting the device and polling the DO pin.

Write All (WRAL) [3]

The write-all (WRAL) instruction simultaneously programs all registers with the data pattern specified in the instruction. After receiving the write-all instruction and 16 bits of data, CS is brought low before the next rising edge of the SK clock and held low for a minimum period specified by t_{CS}. The falling edge of CS initiates the self-timed write cycle. The PE pin (if used) **MUST** be held high while loading the write-all instruction. It is not necessary to clock the SK pin after initiating the self-timed write-all mode. The BUSY/READY status of the device can be determined by selecting the device and polling the DO pin.

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.6 to +7.5	V
V_{IO}	Voltage Applied to Any Pin	Relative to GND	− 0.6 to V_{CC} + 0.6	V
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Commercial		Industrial (I)		Military (M)		Unit
		93C56A/C66A		93C56A/C66A		93C56A/C66A		
		Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
T_A	Ambient Temperature[1]	0	+ 70	− 40	+ 85	− 55	+ 125	°C

DC and AC Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Commercial		Industrial		Military		Unit
			Min	Max	Min	Max	Min	Max	
I_{CC}	Power Supply Current, Active, TTL/CMOS Interface	V_{CC} = 5.5V, CS=SK=V_{IH} DO = Open, f = 2.0MHz		4		6		8	mA
I_{CCSB1}	Supply Current, Standby, TTL Interface	V_{CC} = 5.5V, CS = V_{IL} DO = Open		100		150		200	µA
I_{CCSB2}	Supply Current, Standby, CMOS Interface	V_{CC} = 5.5V, CS = V_{IL} DO = Open		50		100		200	µA
V_{IH}	Input HIGH Level		2.0	V_{CC}+1	2.0	V_{CC}+1	2.0	V_{CC}+1	V
V_{IL}	Input LOW Level		− 0.1	0.8	− 0.1	0.8	− 0.1	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = − 0.4mA	2.2		2.2		2.2		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1mA		0.4		0.4		0.4	V
I_{LI}	Input Leakage Current	V_{IN} = 5.5V		±10		±10		±10	µA
I_{LO}	Output Leakage Current	V_O=5.5V, CS=0, V_{CC} ≤ 5.5V		±10		±10		±10	µA
t_{SKP}	SK Period		500		500		500		ns
t_{SKW}	SK Pulse Width	High or Low	250		250		250		ns
t_{CSS}	CS High to SK High Delay		100		100		100		ns
t_{CSH}	SK Low to CS Low Delay		0		0		0		ns
t_{DIS}	Data Setup Time (Write)		200		200		200		ns
t_{DIH}	Data Hold Time (Write)		200		200		200		ns
t_{PD1} / t_{PD0}	Serial Clock to Output Delay	C_L = 100pF, V_{OL} = 0.8V, V_{OH} = 2.0V, V_{IL} = 0.45V, VIH = 2.4V		250		250		250	ns
$t_{E/W}$	Self-timed Program Cycle[4]			10		10		20	ms
t_{CS}	Min CS Low Time		250		250		250		ns
t_{SV}	CS to Status Valid	CL = 100pF		500		1000		1000	ns
t_{OH}, t_{IH}	Falling Edge of CS to DO High Impedence			100		200		200	ns

Notes

Note 1. ICT's E^2 devices are designed to endure 10,000 Erase/Write cycles and to retain data for at least forty years while operating at 55°C. ICT's standard test flow verifies at least ten years of data retention for Commercial and Industrial temperature devices and at least two years data retention for Military temperature devices. Data retention verification is performed on 100% of the units being shipped. Cycling endurance is verified by lot-sample testing.

Note 2. If the power is removed or the CS pin is brought low during an instruction cycle, the device's instruction registers will be reset. Note that a power-down will totally reset the device. This means that the write-enable instruction (WEN) will need to be executed prior to any programming.

Note 3. If the PE pin is brought to low during the loading of the instruction, this instruction (WEN, WDS, WRITE, and WRAL) may not be executed reliably.

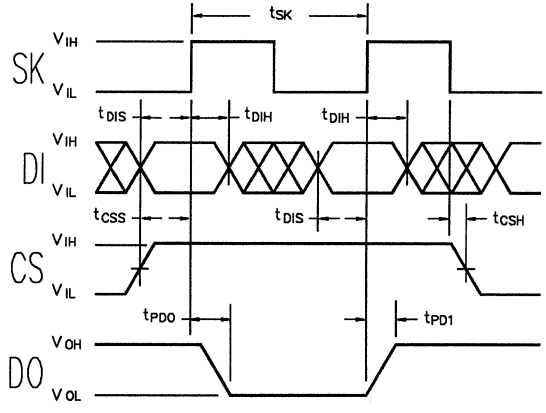
Note 4. Although the 93C56A/C66A self-timed program cycle allows software delay loops to be used to achieve the necessary Erase/Write delay, using the Ready/Busy feature is recommended instead. Using the Ready/Busy feature allows faster response time since $t_{E/W}$ will typically be less than the maximum specification.

Note 5. A7 is a "Don't Care" bit for addressing the 93C56A.

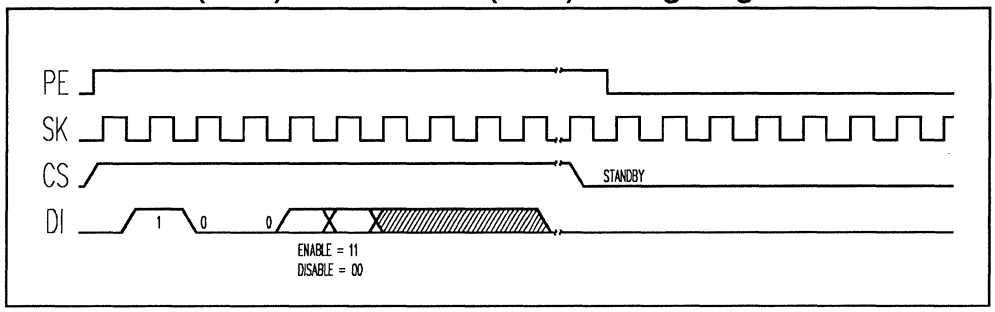
Instruction set for the 93C56A/C66A

Instruction	Start Bit	Opcode	Address [5]	Data	Comments
READ	1	10	$A_7A_6A_5A_4A_3A_2A_1A_0$		Read address
WRITE	1	01	$A_7A_6A_5A_4A_3A_2A_1A_0$	D_{15} - D_0	Write to address
WEN	1	00	1 1 X X X X X X		Write enable
WDS	1	00	0 0 X X X X X X		Write disable
WRAL	1	00	0 1 X X X X X X	D_{15} - D_0	Write all addresses

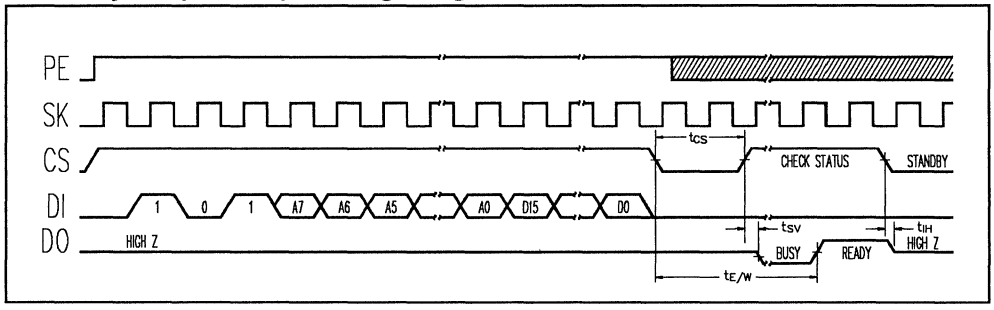
Synchronous Data Timing Waveforms



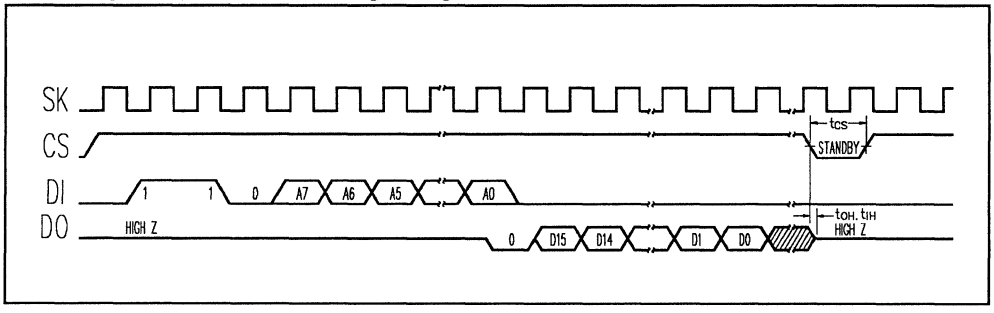
Write Enable (WEN)/Write Disable (WDS) Timing Diagram



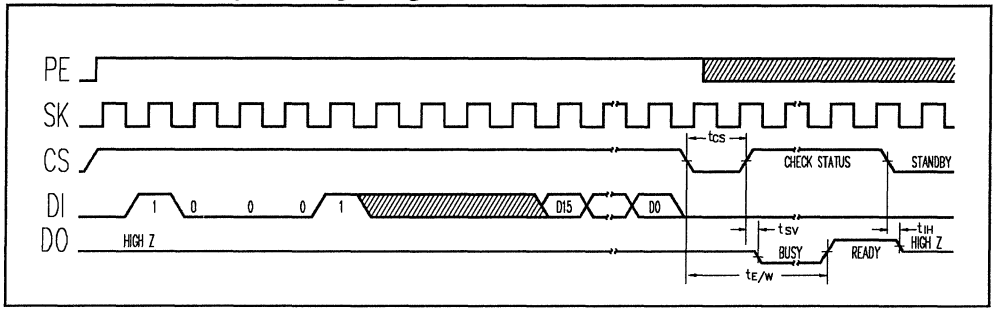
Write Cycle (WRITE) Timing Diagram



Read Cycle (READ) Timing Diagram



Write All (WRAL) Timing Diagram



93CX46
1,024-Bit CMOS Serial EEPROM with extended-voltage operation (2.5V to 6.0V)

Features

- **Advanced CMOS EEPROM Technology**
- **Read/Write Non-volatile Memory**
  - — Single supply operation (2.5V to 6.0V)
  - — 1,024 bits: 64 x 16 organization
  - — Versatile easy-to-use serial data interface
- **Low Power Consumption**
  - — 3mA max Active
  - — 50µA max Standby, CMOS interface
- **Special Features**
  - — Automatic-erase write instruction
  - — Ready/Busy status signal
  - — Software and hardware controlled write protection
- **Ideal For Low-density Data Storage**
  - — Low-cost, space-saving 8-pin package
  - — Commercial, industrial, & military versions
  - — Interfaces with popular CMOS micro controllers- (ie., COP4XX, uPD75XX, HMCS-400, Series-40, M5-Series, 80CXX families)
- **Application Versatility**
  - — Extended-voltage operation is ideal for battery-powered applications
  - — Alarms, Electronic Locks, Appliances, Terminals, Smart Cards, Robotics, Meters, Telephones, Tuners, etc.

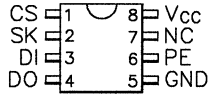
General Description

The ICT 93CX46 is a 1,024-bit, non-volatile memory device fabricated using an advanced CMOS EEPROM technology. It is possible to read or write data with Vcc ranging from 2.5V to 6.0V. The 1,024 bits of memory are organized into 64 registers of 16 bits each. Each register is individually addressable for serial read (or write) operations through the DI (or DO) pin. A versatile serial interface consisting of chip select, clock, data-in and data-out, can easily be controlled by popular CMOS microcontrollers (ie., COP4XX, uPD75XX, HMCS-400, Series-40, M5-Series, 80CXX families) or standard microprocessors.

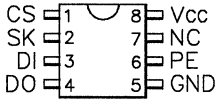
Low power consumption, low cost, and space efficiency make the ICT 93CX46 an ideal candidate for high-volume, low-density data-storage applications. Special features of the 93CX46 include: automatic write time-out, ready/busy status signal, software-controlled write-protection, and an ultra-low-power standby mode (when deselected) that is ideal for battery-powered applications. Additionally, the 93CX46 offers functional compatibility with existing NMOS and CMOS serial EEPROMs. The 93CX46 is designed for applications requiring up to 10,000 erase/write cycles per register and 40 years of data retention.

Connection Diagrams

DIP Package

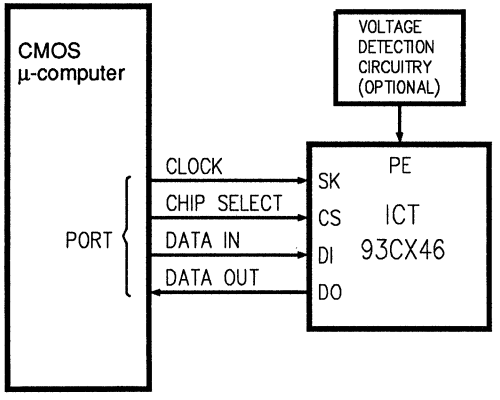


SO8 Package



Pin Names

CS	= Chip Select
SK	= Serial Data Clock
DI	= Serial Data Input
DO	= Serial Data Output
PE	= Program Enable
GND	= Ground
Vcc	= Power Supply
NC	= Not Connected



Interfacing the 93CX46

Function Description

Device Operation[1]

The ICT 93CX46 is a serial 1,024-bit non-volatile non-volatile memory device organized as 64 registers by 16 bits. Each register is independently addressable for read, write, or erase operations. Five, 9-bit instructions control the operation of the device. The 93CX46 operates on a single supply voltage, which may range from 2.5 Volts to 6.0 Volts, and will generate, on chip, the high voltage required for any programming operation.

The 93CX46 provides two methods of protecting data from being accidentally disturbed. The erase/write-disable (EWDS) instruction will disable all programming functions until an erase/write-enable (EWEN) instruction is executed. A hardware control is also available in the form of the PE (program enable) control pin. To perform any programming instruction, PE must be held high while loading the instruction into the 93CX46. The PE control can be used to ensure that no data is accidentally disturbed by erratic switching of the microcontroller's outputs during power-up or power-down. Voltage detection circuitry can be implemented to disable PE when the supply voltage drops below a user-specified voltage level. Note that the PE control pin is tied to an internal pull-up so that the pin may be left unconnected if the PE control feature is not to be used.

Instructions, address, and write data are clocked into the DI pin on the rising edge of the clock (SK). The instructions include: read; write; erase/write enable, erase/write disable; erase all; and write all. The format of each 9-bit instructions-starting with the most significant bit-is as follows: start bit (logical "1"); a two-bit op code; and an eight-bit address. The DO pin is normally in a high-impedance state, except when reading data from the device, or when checking the BUSY/READY status after a programming operation. The BUSY/READY status can be determined after a programming operation by selecting the device (CS high) and polling the DO pin. DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready for the next operation. DO will return to the high-impedance state when the next instruction is initiated.

Read (READ)

The read (READ) instruction outputs serial data on the DO pin. After a read instruction is received, the instruction and the address are decoded. Then data is transferred from the selected memory register to a 16-bit shift register and DO comes out of the high-impedance state. After sending a dummy bit (logical "0"), the 16-bit data string is shifted out of the device. The DO transitions occur on the rising edge of the clock and the data is stable after the specified delay t_{PO} or t_{PD1}.

Write Enable and Disable[2] (WEN and WDS)

The 93CX46 powers up in the programming-disable state. Any programming after power-up, or following a write disable (WDS) instruction, must first be preceded by a write enable (WEN) instruction. The PE pin **MUST** be held high while loading the programming enable instruction. Once enabled, programming remains enabled until a write disable (WDS) instruction is executed or power is removed from the device. The write disable instruction disables all programming functions of the 93CX46 and can be used to prevent accidentally disturbing data in the device. Data can be read from the 93CX46 regardless of the programming enable/disable status.

Write (WRITE)[2]

The 93CX46 initiates an autoerase cycle when executing a write (WRITE) instruction, eliminating the need of an erase (ERASE) command. The write instruction (opcode plus address) is followed by 16 bits of data to be written into the specified address. After the last bit of data (D_O) has been clocked into the DI pin, the CS (chip select) must be brought low before the next rising edge of the SK clock and held low for the minimum period specified by t_{CS}. The falling edge of CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the write instruction. However, after loading the write instruction the PE pin becomes a "don't care". It is not necessary to clock the SK pin after initiating the self-timed write mode. The READY/BUSY status of the device can be determined by selecting the device and polling the DO pin.

Write All (WRAL)[2]

The write-all (WRAL) instruction simultaneously programs all registers with the data pattern specified in the instruction. After receiving the write-all instruction and 16 bits of data, CS (chip select) must be held low for a minimum period specified by t_{CS}. The falling edge of CS initiates the self-timed write cycle. The PE pin **MUST** be held high while loading the write-all instruction. It is not necessary to clock the SK pin after initiating the self-timed write-all mode. The BUSY/READY status of the device can be determined by selecting the device and polling the DO pin.

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	– 0.6 to +7.5	V
V_{IO}	Voltage Applied to Any Pin	Relative to GND	– 0.6 to V_{CC} + 0.6	V
T_{ST}	Storage Temperature		– 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Commercial 93CX46		Industrial 93CX46 I		Military 93CX46 M		Unit
		Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage	2.5	6.0	2.5	6.0	2.5	6.0	V
T_A	Ambient Temperature [3]	0	+ 70	– 40	+ 85	– 55	+ 125	°C

DC and AC Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	93CX46		93CX46 I		93CX46 M		Unit
			Min	Max	Min	Max	Min	Max	
I_{CC}	Power Supply Current, Active, TTL/CMOS Interface	V_{CC} = 6.0V, CS=SK=V_{IH} DO = Open, f = 2.0MHz		3		5		7	mA
I_{CCSB1}	Supply Current, Standby, TTL Interface	V_{CC} = 6.0V, CS = V_{IL} DO = Open		100		150		200	µA
I_{CCSB2}	Supply Current, Standby, CMOS Interface	V_{CC} = 6.0V, CS = V_{IL} DO = Open		50		100		200	µA
V_{IH}	Input HIGH Level [4]		V_{CC}–.2	V_{CC}+1	V_{CC}–.2	V_{CC}+1	V_{CC}–.2	V_{CC}+1	V
V_{IL}	Input LOW Level [4]		– 0.1	0.2	– 0.1	0.2	– 0.1	0.2	V
V_{OH}	Output HIGH Voltage[4]	I_{OH} = – 0.4mA (note 4)	2.2		2.2		2.2		V
V_{OL}	Output LOW Voltage[4]	I_{OL} = 2.1mA (note 4)		0.4		0.4		0.4	V
I_{LI}	Input Leakage Current	V_{IN} = 6.0V		±10		±10		±10	µA
I_{LO}	Output Leakage Current	V_O=6.0V, CS=0, V_{CC} ≤ 6.0V		±10		±10		±10	µA
t_{SKP}	SK Period		1		1		1		µs
t_{SKW}	SK Pulse Width	High or Low	500		500		500		ns
t_{CSS}	CS High to SK High Delay		100		100		100		ns
t_{CSH}	SK Low to CS Low Delay		0		0		0		ns
t_{DIS}	Data Setup Time (Write)		200		200		200		ns
t_{DIH}	Data Hold Time (Write)		200		200		200		ns
t_{PD1} / t_{PD0}	Serial Clock to Output Delay	C_L = 100pF, V_{OL} = 0.8V, V_{OH} = 2.0V, V_{IL} = 0.45V, VIH = 2.4V		250		250		250	ns
$t_{E/W}$	Self-timed Program Cycle[5]			20		20		40	ms
t_{CS}	Min CS Low Time		250		250		250		ns
t_{SV}	CS to Status Valid	CL = 100pF		500		1000		1000	ns
t_{OH}, t_{IH}	Falling Edge of CS to DO High Impedence			100		200		200	ns

Notes

Note 1. If the power is removed or the CS pin is brought low during an instruction cycle, the device's instruction registers will be reset. Note that a power-down will totally reset the device. This means that the write-enable instruction (WEN) will need to be executed prior to any programming.

Note 2. If the PE pin is brought to low during the loading of the instruction, this instruction (WEN, WDS, WRITE, and WRAL) may not be executed reliably.

Note 3. ICT's E^2 devices are designed to endure 10,000 Erase/Write cycles and to retain data for at least forty years while operating at 55°C. ICT's standard test flow verifies at least ten years of data retention for Commercial and Industrial temperature devices and at least two years data retention for Military temperature devices. Data retention verification is performed on 100% of the units being shipped. Cycling endurance is verified by lot-sample testing.

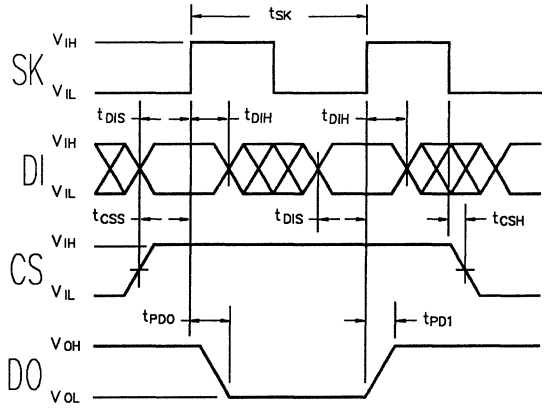
Note 4. The 93CX46 is designed to operate with TTL interface only when $4.5V \leq V_{CC} \leq 5.5V$.

Note 5. Although the 93CX46 self-timed program cycle allows software delay loops to be used to achieve the necessary Erase/Write delay, using the Ready/Busy feature is recommended instead. Using the Ready/Busy feature allows faster response time since $t_{E/W}$ will typically be less than the maximum specification.

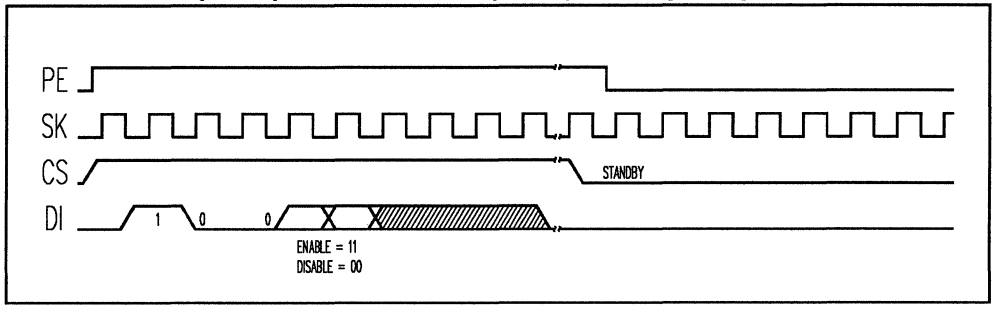
Instruction set for the 93CX46

Instruction	Start Bit	Opcode	Address	Data	Comments
READ	1	10	$A_5A_4A_3A_2A_1A_0$		Read address
WRITE	1	01	$A_5A_4A_3A_2A_1A_0$	D_{15} - D_0	Write to address
WEN	1	00	1 1 X X X X		Write enable
WDS	1	00	0 0 X X X X		Write disable
WRAL	1	00	0 1 X X X X	D_{15} - D_0	Write all addresses

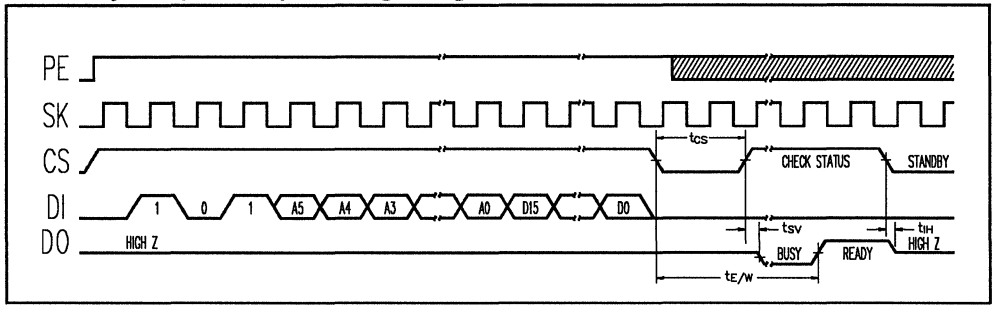
Synchronous Data Timing Waveforms



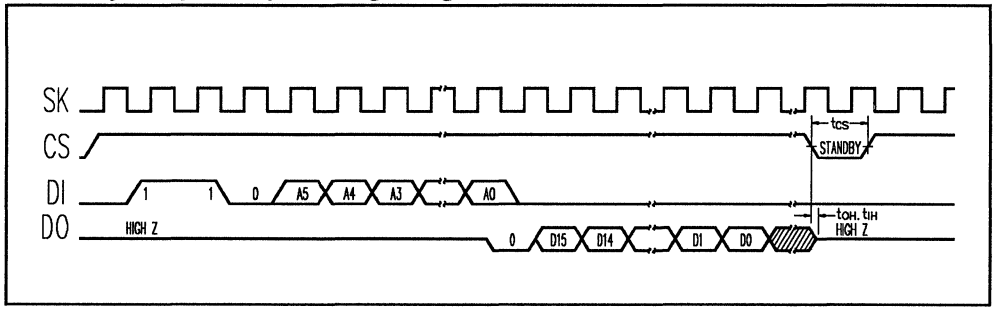
Write Enable (WEN)/Write Disable (WDS) Timing Diagram



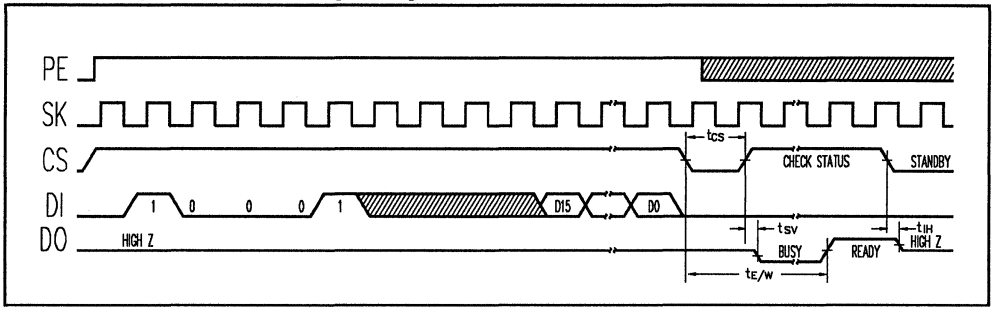
Write Cycle (WRITE) Timing Diagram



Read Cycle (READ) Timing Diagram



Write All (WRAL) Timing Diagram



93CX56/93CX66
2,048/4,096-Bit CMOS Serial EEPROM with extended-voltage operation (2.5V to 6.5V)

Features

- **Advanced CMOS EEPROM Technology**
- **Read/Write Non-volatile Memory**
  - — Single supply operation (2.5V to 6.0V)
  - — 2,048 bits: 128 x 16 organization
  - — 4,096 bits: 256 x 16 organization
  - — Versatile easy-to-use serial data interface
- **Low Power Consumption**
  - — 4mA max Active
  - — 50µA max Standby, CMOS interface
- **Special Features**
  - — Automatic-erase write instruction
  - — Ready/Busy status signal
  - — Software and hardware controlled write protection
- **Ideal For Low-density Data Storage**
  - — Low-cost, space-saving 8-pin package
  - — Commercial, industrial, & military versions
  - — Interfaces with popular CMOS micro controllers- (ie., COP4XX, uPD75XX, HMCS-400, Series-40, M5-Series, 80CXX families)
- **Application Versatility**
  - — Extended-voltage operation is ideal for battery-powered applications
  - — Alarms, Electronic Locks, Appliances, Terminals, Smart Cards, Robotics, Meters, Telephones, Tuners, etc.

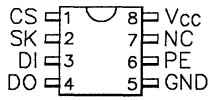
General Description

The ICT 93CX56/CX66 is a 2,048/4,096-bit, non-volatile memory device fabricated using an advanced CMOS EEPROM technology. It is possible to read or write data with Vcc ranging from 2.5V to 6.0V. The 2,048/4,096 bits of memory are organized into 128/256 registers of 16 bits each. Each register is individually addressable for serial read (or write) operations through the DI (or DO) pin. A versatile serial interface consisting of chip select, clock, data-in and data-out, can easily be controlled by popular CMOS microcontrollers (ie., COP4XX, uPD75XX, HMCS-400, Series-40, M5-Series, 80CXX families) or standard microprocessors.

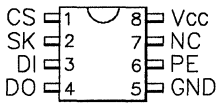
Low power consumption, low cost, and space efficiency make the ICT 93CX56/CX66 an ideal candidate for high-volume, low-density data-storage applications. Special features of the 93CX56/CX66 include: automatic write time-out, ready/busy status signal, software-controlled write-protection, and an ultra-low-power standby mode (when deselected) that is ideal for battery-powered applications. Additionally, the 93CX56/CX66 offers functional compatibility with existing NMOS and CMOS serial EEPROMs. The 93CX56/CX66 is designed for applications requiring up to 10,000 erase/write cycles per register and 40 years of data retention.

Connection Diagrams

DIP Package

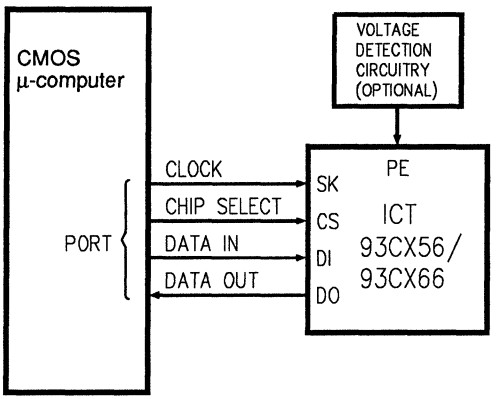


SO8 Package



Pin Names

CS	= Chip Select
SK	= Serial Data Clock
DI	= Serial Data Input
DO	= Serial Data Output
PE	= Program Enable
GND	= Ground
Vcc	= Power Supply
NC	= Not Connected



Interfacing the 93CX56/93CX66

Function Description

Device Operation [1]

The ICT 93CX56/CX66 are serial 2,048/4,096-bit non-volatile memory devices organized as 128/256 registers by 16 bits. Each register is independently addressable for read, write, or erase operations. Five, 11-bit instructions control the operation of the device. The 93CX56/CX66 operates on a single supply voltage, which may range from 2.5 Volts to 6.0 Volts, and will generate, on chip, the high voltage required for any programming operation.

The 93CX56/CX66 provides two methods of protecting data from being accidentally disturbed. The Write-Disable (WDS) instruction will disable all programming functions until an Write-Enable (WEN) instruction is executed. A hardware control is also available in the form of the PE (program enable) control pin. To perform any programming instruction, PE must be held high while loading the instruction into the 93CX56/CX66. The PE control can be used to ensure that no data is accidentally disturbed by erratic switching of the microcontroller's outputs during power-up or power-down. Voltage detection circuitry can be implemented to disable PE when the supply voltage drops below a user-specified voltage level. Note that the PE control pin is tied to an internal pull-up so that the pin may be left unconnected if the PE control feature is not to be used.

Instructions, address, and write data are clocked into the DI pin on the rising edge of the clock (SK). The instructions include: read; write; write enable, write disable; and write all. The format of each eleven-bit instruction, starting with the most significant bit, is as follows: start bit (logical "1"); a two-bit op code; and an eight-bit address (one "Don't Care" bit and seven address bits for the 93CX56). The DO pin is normally in a high-impedance state, except when reading data from the device, or when checking the BUSY/READY status after a programming operation. The BUSY/READY status can be determined after a programming operation by selecting the device (CS high) and polling the DO pin. DO low indicates that the programming operation is not completed (BUSY), while DO high indicates that the device is ready for the next operation (READY). DO will return to the high-impedance state when the next instruction is initiated.

Read (READ)

The read (READ) instruction outputs serial data on the DO pin. After a read instruction is received, the instruction and the address are decoded. Then data is transferred from the selected memory register to a 16-bit shift register and DO comes out of the high-impedance state. After sending a dummy bit (logical "0"), the 16-bit data string is shifted out of the device. The DO transitions occur on the rising edge of the clock and the data is stable after the specified delay t_{PO} or t_{PD1}.

Write Enable/Disable [2] (WEN /WDS)

The 93CX56/CX66 powers up in the programming-disable state. Any programming after power-up, or following a write disable (WDS) instruction, must first be preceded by a write enable (WEN) instruction. The PE pin (if used) **MUST** be held high while loading the programming enable instruction. Once enabled, programming remains enabled until a write disable (WDS) instruction is executed or power is removed from the device. The write disable instruction disables all programming functions of the 93CX56/CX66 and can be used to prevent accidentally disturbing data in the device. Data can be read from the 93CX56/CX66 regardless of the programming enable/disable status.

Write (WRITE) [2]

The 93CX56/CX66 initiates an autoerase cycle when executing a write (WRITE) instruction, eliminating the need of an erase (ERASE) command. The write instruction (opcode plus address) is followed by 16 bits of data to be written into the specified address. After the last bit of data (D_0) has been clocked into the DI pin, the CS (chip select) must be brought low before the next rising edge of the SK clock and held low for the minimum period specified by t_{CS}. The falling edge of CS initiates the self-timed programming cycle. The PE pin (if used) **MUST** be held high while loading the write instruction. However, after loading the write instruction the PE pin becomes a "don't care". It is not necessary to clock the SK pin after initiating the self-timed write mode. The READY/BUSY status of the device can be determined by selecting the device and polling the DO pin.

Write All (WRAL) [2]

The write-all (WRAL) instruction simultaneously programs all registers with the data pattern specified in the instruction. After receiving the write-all instruction and 16 bits of data, CS is brought low before the next rising edge of the SK clock and held low for a minimum period specified by t_{CS}. The falling edge of CS initiates the self-timed write cycle. The PE pin (if used) **MUST** be held high while loading the write-all instruction. It is not necessary to clock the SK pin after initiating the self-timed write-all mode. The BUSY/READY status of the device can be determined by selecting the device and polling the DO pin.

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.6 to +7.5	V
V_{IO}	Voltage Applied to Any Pin	Relative to GND	− 0.6 to V_{CC} + 0.6	V
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Commercial		Industrial (I)		Military (M)		Unit
		93CX56/93CX66		93CX56/93CX66		93CX56/93CX66		
		Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage	2.5	6.0	2.5	6.0	2.5	6.0	V
T_A	Ambient Temperature [3]	0	+ 70	− 40	+ 85	− 55	+ 125	°C

DC and AC Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Commercial		Industrial		Military		Unit
			Min	Max	Min	Max	Min	Max	
I_{CC}	Power Supply Current, Active, TTL/CMOS Interface	V_{CC} = 5.5V, CS=SK=V_{IH} DO = Open, f = 2.0MHz		4		6		8	mA
I_{CCSB1}	Supply Current, Standby, TTL Interface	V_{CC} = 5.5V, CS = V_{IL} DO = Open		100		150		250	µA
I_{CCSB2}	Supply Current, Standby, CMOS Interface	V_{CC} = 5.5V, CS = V_{IL} DO = Open		50		100		200	µA
V_{IH}	Input HIGH Level [4]		V_{CC}−.2	V_{CC}+1	V_{CC}−.2	V_{CC}+1	V_{CC}−.2	V_{CC}+1	V
V_{IL}	Input LOW Level [4]		− 0.1	0.2	− 0.1	0.2	− 0.1	0.2	V
V_{OH}	Output HIGH Voltage[4]	I_{OH} = − 0.4mA	2.2		2.2		2.2		V
V_{OL}	Output LOW Voltage[4]	I_{OL} = 2.1mA		0.4		0.4		0.4	V
I_{LI}	Input Leakage Current	V_{IN} = 6.0V		±10		±10		±10	µA
I_{LO}	Output Leakage Current	V_O=6.0V, CS=0, V_{CC} ≤ 6.0V		±10		±10		±10	µA
t_{SKP}	SK Period		1		1		1		µs
t_{SKW}	SK Pulse Width	High or Low	500		500		500		ns
t_{CSS}	CS High to SK High Delay		100		100		100		ns
t_{CSH}	SK Low to CS Low Delay		0		0		0		ns
t_{DIS}	Data Setup Time (Write)		200		200		200		ns
t_{DIH}	Data Hold Time (Write)		200		200		200		ns
t_{PD1} / t_{PD0}	Serial Clock to Output Delay	C_L = 100pF, V_{OL} = 0.8V, V_{OH} = 2.0V, V_{IL} = 0.45V, VIH = 2.4V		250		250		250	ns
$t_{E/W}$	Self-timed Program Cycle			10		10		20	ms
t_{CS}	Min CS Low Time		250		250		250		ns
t_{SV}	CS to Status Valid	CL = 100pF		500		1000		1000	ns
t_{OH}, t_{IH}	Falling Edge of CS to DO High Impedence			100		200		200	ns

Notes

Note 1. If the power is removed or the CS pin is brought low during an instruction cycle, the device's instruction registers will be reset. Note that a power-down will totally reset the device. This means that the write-enable instruction (WEN) will need to be executed prior to any programming.

Note 2. If the PE pin is brought to low during the loading of the instruction, this instruction (WEN, WDS, WRITE, and WRAL) may not be executed reliably.

Note 3. ICT's E^2 devices are designed to endure 10,000 Erase/Write cycles and to retain data for at least forty years while operating at 55°C. ICT's standard test flow verifies at least ten years of data retention for Commercial and Industrial temperature devices and at least two years data retention for Military temperature devices. Data retention verification is performed on 100% of the units being shipped. Cycling endurance is verified by lot-sample testing.

Note 4. The 93CX56/CX66 is designed to operate with TTL interface only when $4.5V \leq V_{CC} \leq 5.5V$.

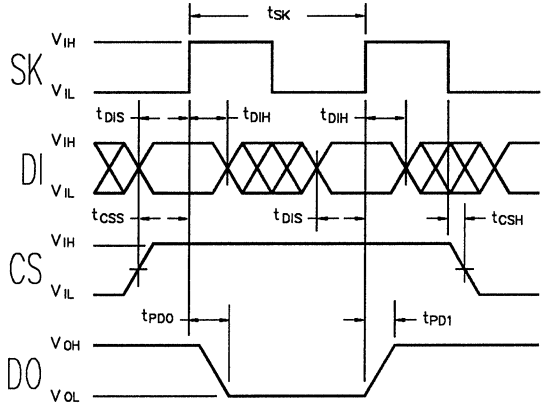
Note 5. Although the 93CX56/CX66 self-timed program cycle allows software delay loops to be used to achieve the necessary Erase/Write delay, using the Ready/Busy feature is recommended instead. Using the Ready/Busy feature allows faster response time since $t_{E/W}$ will typically be less than the maximum specification.

Note 6. A7 is a "Don't Care" bit for addressing the 93CX56.

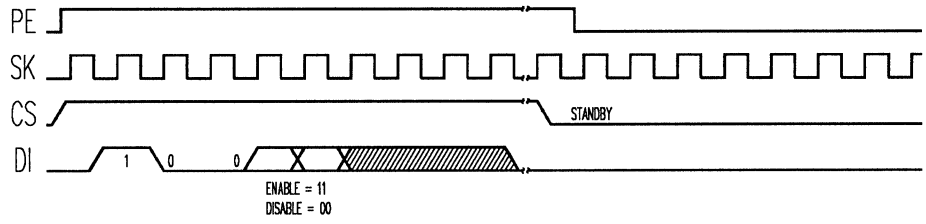
Instruction set for the 93CX56/93CX66

Instruction	Start Bit	Opcode	Address [6]	Data	Comments
READ	1	10	$A_7A_6A_5A_4A_3A_2A_1A_0$		Read address
WRITE	1	01	$A_7A_6A_5A_4A_3A_2A_1A_0$	D_{15} - D_0	Write to address
WEN	1	00	1 1 X X X X X X		Write enable
WDS	1	00	0 0 X X X X X X		Write disable
WRAL	1	00	0 1 X X X X X X	D_{15} - D_0	Write all addresses

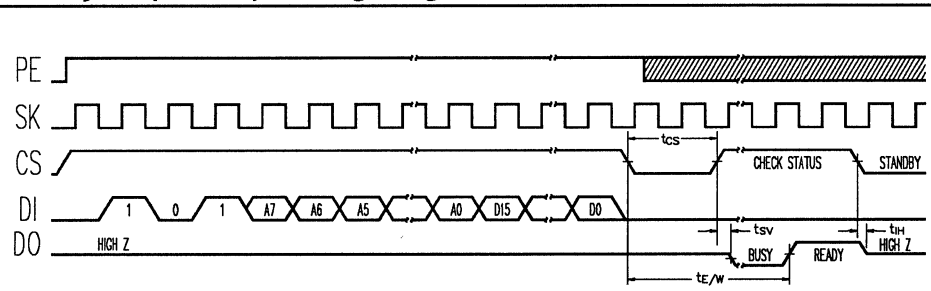
Synchronous Data Timing Waveforms



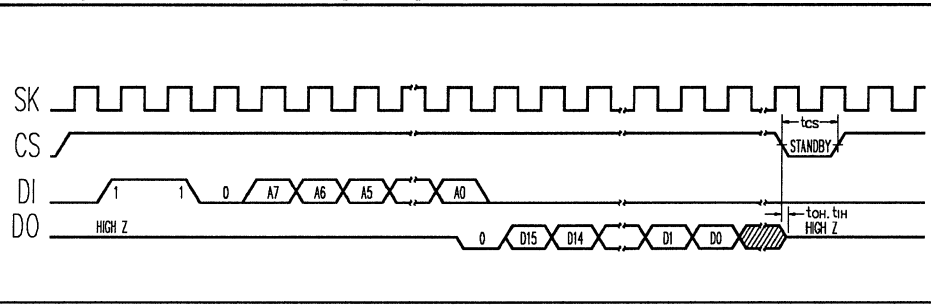
Write Enable (WEN)/Write Disable (WDS) Timing Diagram



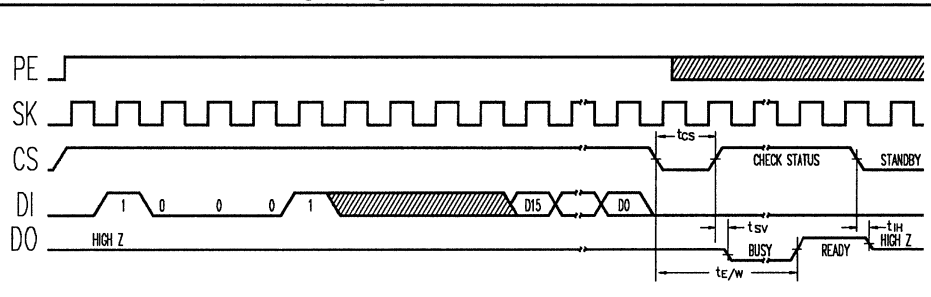
Write Cycle (WRITE) Timing Diagram



Read Cycle (READ) Timing Diagram



Write All (WRAL) Timing Diagram



CMOS High Speed PROMs

3

CMOS High-Speed PROMs

ICT's family of CMOS High-Speed PROMs provide the performance and features needed by todays new high speed system designs. They also serve as a plug-in compatible alternative for existing designs using bipolar PROMs. The family of 24 pin devices offer fast access times, low power consumption, UV reprogrammability and 100% testing for program and function.

CMOS High-Speed PROM Features

- **High-Speed CMOS UV-EPROM Technology**
  - 35-55ns access times
- **Socket Compatible with Bipolar PROMs**
  - 8K X 8 and 4K X 8 organization
  - Standard 24-pin 600 mil DIP
  - Space-saving 24-pin 300 mil DIP
- **Low Power Consumption**
  - Less than 1/3 of bipolar devices
  - Special low-power standby mode (27CX321/2)
- **UV Reprogrammability**
  - Cost savings and convenience
  - Allows 100% factory testability
- **Programming Support**
  - From ICT and third-party manufacturers
- **Commercial and Industrial Versions**

INTERNATIONAL CMOS
TECHNOLOGY, INC.

27CX321/27CX322
4,096 x 8-bit CMOS High-Speed Erasable PROM

Features

- **Advanced CMOS EPROM Technology**
- **High Performance**
  - 27CX321/322-35 t_{AA} = 35nS max
  - 27CX321/322-40 t_{AA} = 40nS max
  - 27CX321/322-45 t_{AA} = 45nS max
- **Low Power Consumption**
  - I_{CC} = 40mA max - Active (Commercial)
  - I_{SB} = 500µA max typical - Standby Mode
- **TTL-Compatible I/O**
- **Reprogrammability**
  - Adds convenience, reduces costs
  - Windowed package for UV erasure
  - Allows 100% factory testing
- **Bipolar PROM replacement**
  - Pin-compatible with Bipolar PROMs
  - Higher speed
  - Lower power consumption
  - 300-mil and 600-mil packages
- **Commercial and Industrial Versions**

General Description

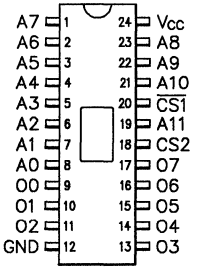
The ICT 27CX321 and 27CX322 are 4,096 X 8-bit CMOS high-speed UV-erasable PROMs that provide a low-power, reprogrammable alternative to bipolar fuse-link PROMs. Available in both 600mil (27CX321) and 300mil (27CX322) packages, these devices are pin/socket-compatible with many popular bipolar PROMs. The 27CX321/322 are designed in an advanced CMOS EPROM technology and use differential memory-cell techniques to provide access times comparable to high-speed bipolar PROMs (as fast as 35nS), with a significant improvement in power consumption. A special, user-programmable, low-power standby mode reduces power consumption even further when the device is deselected. The reprogrammability of the 27CX321/322 not only adds convenience and reduces development and field retrofit costs, but enhances factory testability, allowing for 100% field programmability and function.

Pin Diagrams

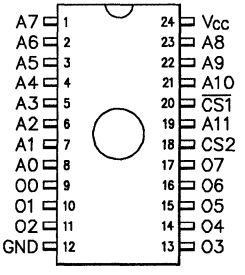
PinNames

A0-A11	Address Inputs
$\overline{O0}$-$\overline{O7}$	Data Outputs
CS1	Chip Select
CS2	Chip Select

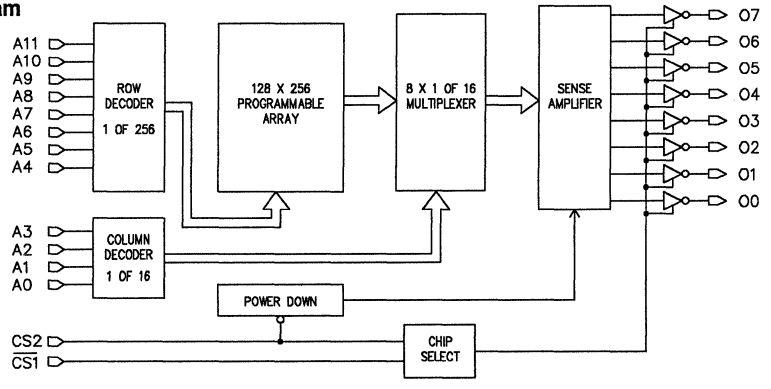
27CX322 (300 mil)



27CX321 (600 mil)



Block Diagram



Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	– 0.6 to +7.0	V
V_{IO}	Voltage Applied to Any Pin	Relative to GND	–0.6 to Vcc+0.6	V
T_A	Ambient Temp., Power Applied		–10 to +85	°C
T_{ST}	Storage Temperature		–65 to +150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
V_{CC}	Supply Voltage	Industrial	4.50	5.50	V
T_A	Ambient Temperature	Comercial	0	70	°C
T_A	Ambient Temperature	Industrial	–40	85	°C

D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Level		2.0(2.4)[1]		V
V_{IL}	Input LOW Level			0.8	V
V_{OH}	Output HIGH Voltage[2]	Vcc = Min, I_{OH} = –4.0mA	2.4		V
V_{OL}	Output LOW Voltage[2]	Vcc = Min, I_{OL} = 12mA		0.45	V
I_L	Input Leakage Current	Vcc = Max, GND ≤ V_I ≤ Vcc		10	µA
I_{OS}	Output Short Circuit Current[3]	$\overline{Vcc}$ = Max, V_O = GND $\overline{CS1}$ = V_{IL} and CS2 = V_{IH}	–15	–90	mA
I_{OZ}	Output Leakage Current	$\overline{Vcc}$ = Max, V_O = Vcc or GND $\overline{CS1}$ V_{IH} or CS2 = V_{IL}		10	µA
I_{CC}	Power Supply Current	All inputs=(GND or Vcc) ±		40(60)[1]	mA
I_{SB}	Standby Power Supply Current[4] (Typical values ~ 500µA)	CS2 = V_{IL}, All other inputs = (GND or Vcc) ± 0.3V	0.1	5	mA
V_{IC}	Input Clamp Voltage	Vcc = Min, I_{IN} = –18mA		–1.2	V

Capacitance

These measurements are periodically sample tested..

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C Vcc = 5.0V @ f = 1MHz		6	pF
C_{OUT}	Output Capacitance			12	pF
C_{CS1}	CS1 Pin Capacitance			15	pF
C_{CS2}	CS2 Pin Capacitance			6	pF

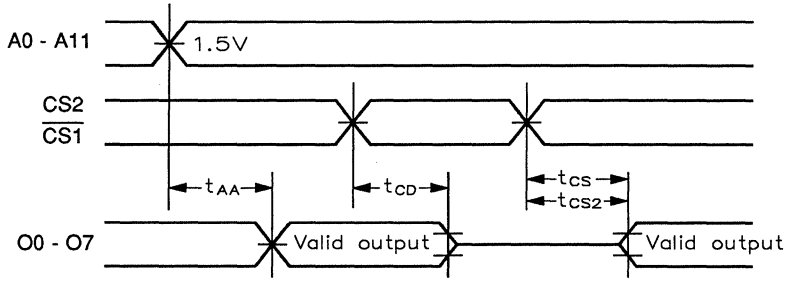
Notes:
1. Industrial specification.
2. The 27CX321/27CX322 provide true CMOS output interface levels. The specifications shown are for TTL interface.
3. No more than one output should be shorted at a time. Duration of short circuit should not be more than one second.
4. Applicable only if standby mode is programmed.

A.C. Electrical Characteristics

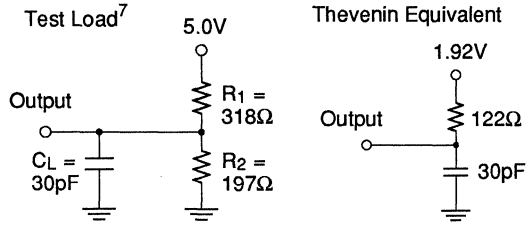
Over the Operating Range [5]

Symbol	Parameter	27CX321-35		27CX321-40		27CX321-45		Unit
		Min	Max	Min	Max	Min	Max	
t_{AA}	Access Time From Address To Output		35		40		45	nS
t_{CS}	Access Time From Chip Select 1 or 2 to Output [5]		20		25		25	nS
t_{CS2}	Chip Select 2 to Output in Standby Mode [4,6]		30		30		35	nS
t_{CD}	Chip Select 1 and 2 Disable to High-Z [6,7]		20		20		25	nS

Switching Waveforms



Test Loads



Notes:

5. Test conditions assume: signal transition times of 5 nS or less from the 10% and 90% points; timing reference levels of 1.5V (unless otherwise specified); and test loads shown.
6. t_{CS} and t_{CS2} are measured from the input transition to $V_{REF} \pm 0.1V$. t_{CD} is measured from the input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$.
7. C_L includes scope and jig capacitance. t_{CD} is tested with $C_L = 5pF$.

Standby Low-Power Mode

The low-power standby mode is a user-selectable option that can be set using programming equipment that supports the 27CX321/27CX322. If this mode is set, the 27CX321/27CX322 will power-down to typically 500µA supply current while CS2 is asserted low. The delay from CS2 low to power-down is approximately 45nS. Note that chip-select-to-data-out timing for CS2 will change if the standby mode is selected (refer to the specification for t_{CS2} under A.C. Electrical Characteristics). For information on selecting the standby option, please contact your programmer manufacturer or ICT.

Erasure Characteristics

The 27CX321/27CX322 are erased by exposure to ultraviolet light. For complete erasure,the recommended minimum integrated dose (UV intensity X exposure time) is 15 Watt-second/cm^2 of ultraviolet light with a wavelength of 2537Å. For an ultraviolet lamp with a 12mW/cm^2 power rating, the exposure time would be approximately 20 minutes. The 27CX321/27CX322 should be placed within one inch of the lamp during erasure. Exposing the CMOS EPROM to high-intensity UV light for extended periods may affect device reliability

Programming the 27CX321/322

The 27CX321/27CX322 employ a dual-transistor differential memory cell design. Initially, and after erasure, all bits of the 27CX321/322 are in an undefined state. Thus, verifying a blank device will yield erroneous results. The desired state of each bit must be programmed into the device to ensure proper operation.

Programming support is available from ICT and third-party vendors, including DATA I/O (model no. 29B with Unipak 2 or 2B - firmware version V15). For more information on programming support and programming specifications, please contact ICT.

INTERNATIONAL CMOS
TECHNOLOGY, INC.

27CX641/27CX642
8,192 x 8-bit CMOS High-Speed Erasable PROM

Features

- **Advanced CMOS EPROM Technology**
- **High Performance**
  - 27CX641/642-35 t_{AA} = 35ns max
  - 27CX641/642-40 t_{AA} = 40ns max
  - 27CX641/642-45 t_{AA} = 45ns max
  - 27CX641/642-55 t_{AA} = 55ns max
- **Low Power Consumption**
  - I_{CC}=80mA max (Commercial)
- **TTL-Compatible I/O**
- **Reprogrammability**
  - Adds convenience, reduces costs
  - Windowed package for UV erasure
  - Allows 100% factory testing
- **Bipolar PROM replacement**
  - Pin-compatible with Bipolar PROMs
  - Higher speed
  - Lower power consumption
  - 300-mil and 600-mil packages
- **Commercial and Industrial Versions**

3

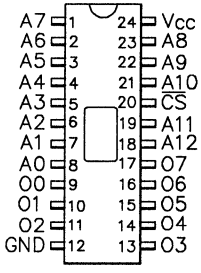
General Description

The ICT 27CX641 and 27CX642 are 8,192 X 8-bit CMOS high-speed UV-erasable PROMs that provide a low-power reprogrammable alternative to bipolar fuse-link PROMs. Available in both 600mil (27CX641) and 300mil (27CX642) packages, these devices are pin/socket-compatible with many popular bipolar PROMs.

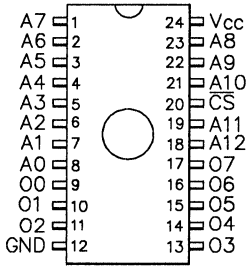
The 27CX641/642 are designed in an advanced CMOS EPROM technology and use differential memory cell techniques to provide access times comparable to high-speed bipolar PROMs (as fast as 35ns) with a significant improvement in power consumption. The reprogrammability of the 27CX641/642 not only adds convenience and reduces development and field retrofit costs, but enhances factory testability, allowing for 100% field programmability and function.

Pin Diagrams

27CX642 (300mil)



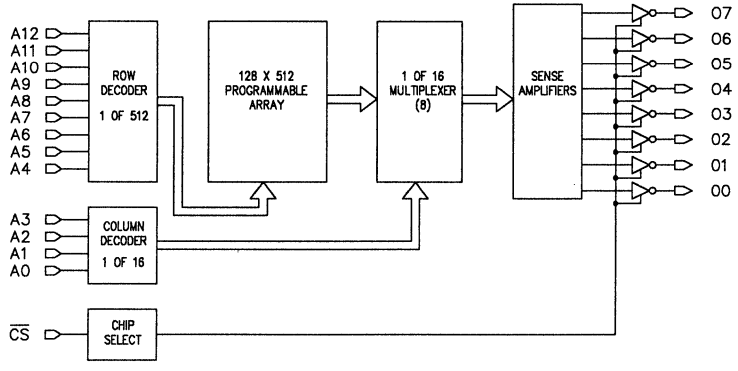
27CX641 (600mil)



Pin Names

A0–A12	Address Inputs
O0–O7	Data Outputs
CS	Chip Select
GND	Ground
Vcc	Power Supply

Block Diagram



Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	−0.6 to +7.0	V
V_{IO}	Voltage Applied to Any Pin	Relative to GND	−0.6 to V_{CC}+0.6	V
T_A	Ambient Temp., Power Applied		−10 to +85	°C
T_{ST}	Storage Temperature		−65 to +150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
V_{CC}	Supply Voltage	Industrial	4.50	5.50	V
T_A	Ambient Temperature	Commercial	0	70	°C
T_A	Ambient Temperature	Industrial	−40	85	°C

D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Level		2.0[1]		V
V_{IL}	Input LOW Level			0.8	V
V_{OH}	Output HIGH Voltage[2]	V_{CC} = Min, I_{OH} = −4.0mA	2.4		V
V_{OL}	Output LOW Voltage[2]	V_{CC} = Min, I_{OL} = 12mA		0.45	V
I_L	Input Leakage Current	V_{CC} = Max, GND ≤ V_I ≤ V_{CC}		10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max, V_O = GND, $\overline{CS}$ = V_{IL}	−15	−90	mA
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_O = V_{CC} or GND, $\overline{CS}$ = V_{IH}		10	µA
I_{CC}	Power Supply Current	All inputs =(GND or V_{CC}) ± 0.3V @ f = 15MHz		80[1]	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18mA		−1.2	V

Capacitance

These measurements are periodically sample tested..

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V, @ f = 1MHz		6	pF
C_{OUT}	Output Capacitance			12	pF
C_{CS}	CS Pin Capacitance			15	pF

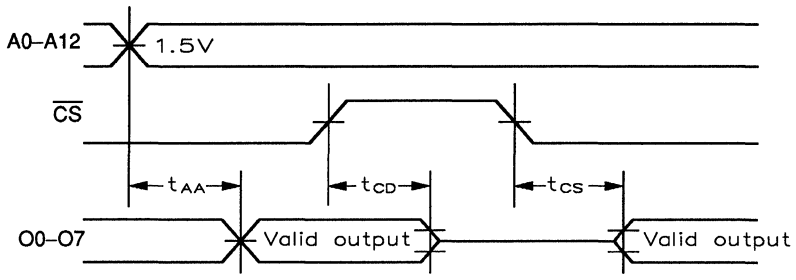
Notes:
1. Industrial specification: V_{IH} = 2.4V, I_{CC} = 120mA. Commercial -35 specification: I_{CC} = 90mA.
2. The 27CX641/27CX642 provide true CMOS output interface levels; the specifications shown are for TTL interface.
3. No more than one output should be shorted at a time. Duration of short circuit should not be more than one second.

A.C. Electrical Characteristics

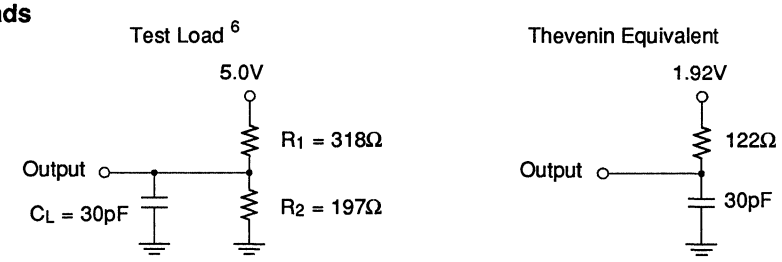
Over the Operating Range [4]

Symbol	Parameter	27CX641-35		27CX641-40		27CX641-45		27CX641-55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AA}	Access Time From Address To Output		35		40		45		55	ns
t_{CS}	Access Time From Chip Select to Output [5]		20		20		25		35	ns
t_{CD}	Chip Disable to High-Z [5,6]		20		20		20		35	ns

Switching Waveforms



Test Loads



Notes:

4. Test conditions assume: signal transition times of 5 nS or less from the 10% and 90% points; timing reference levels of 1.5V (unless otherwise specified); and test loads shown.
5. t_{CS} is measured from the input transition to V_{REF} (1.92V) ± 0.1V. t_{CD} is measured from the input transition to V_{OH} – 0.1V or V_{OL} + 0.1V.
6. C_L includes scope and jig capacitance. t_{CD} is tested with C_L = 5pF.

Erasure Characteristics

The 27CX641/27CX642 are erased by exposure to ultraviolet light. For complete erasure, the recommended minimum integrated dose (UV intensity X exposure time) is 15 Watt-second/cm^2 of ultraviolet light with a wavelength of 2537Å. For an ultraviolet lamp with a 12mW/cm^2 power rating, the exposure time would be approximately 20 minutes. The 27CX641/27CX642 should be placed within one inch of the lamp during erasure. Exposing the CMOS EPROM to high-intensity UV light for extended periods may cause permanent damage to the device.

Programming the 27CX641/642

The 27CX641/27CX642 employ a dual-transistor differential memory cell design. Initially, and after erasure, all bits of the 27CX641/27CX642 are in an undefined state. Verifying a blank device will yield erroneous results. The desired state ("1" or "0") of each bit must be programmed into the device to ensure proper operation.

Programming support is available from ICT and third-party vendors including DATA I/O (model no. 29B with Unipak 2 or 2B - firmware version V14 - family/pinout code=82/67). For more information on programming support and programming specifications, please contact ICT.

CMOS High Speed EPROMs

4

CMOS High-Speed EPROMs

ICT's family of UV-EPROMs provide the high-speed and high-density required for operation in high-performance microprocessor based systems. The family of JEDEC-standard 28-pin and 32-pin devices offer fast access times, low power consumption, UV reprogrammability and 100% testing for program and function.

High-Speed EPROM Features

- **High-Speed CMOS UV-EPROM Technology**
  - 40-90ns access times
- **High-Density**
  - 27CX256: 32K X 8 (256K-bits)
  - 27CX010: 128K X 8 (1M-bits)
- **Pin Compatibility**
  - JEDEC-Standard 28-pin and 32-pin CERDIP
  - Upgrades through 8M-bits
- **Low Power Consumption**
  - 90mA Icc Active
  - 1mA Icc CMOS Standby
- **UV Reprogrammability**
  - Cost savings and convenience
  - Allows 100% factory testability
- **Programming Support**
  - From third-party manufacturers

27CX010
1M (128K x 8) CMOS High-Speed EPROM

Features

- **Advanced CMOS EPROM Technology**
- **High Performance**
  - 27CX010C-55 t_{AA} = 55ns max
  - 27CX010C-70 t_{AA} = 70ns max
  - 27CX010C-90 t_{AA} = 90ns max
- **Low Power Consumption**
  - 90mA Max Active
  - 20mA Max Standby, TTL interface
  - 1mA Max Standby, CMOS interface
- **TTL-Compatible I/O**
- **Reprogrammability**
  - Adds convenience, reduces costs
  - Windowed package for UV erasure
  - Allows 100% factory testing
- **Programming Support**
  - Supported by popular programmers
  - Fast programming algorithm
  - Auto Select mode feature
- **Packaging**
  - JEDEC-standard 32-pin CERDIP
  - Pin compatible upgrades from 512K through 8M-bits

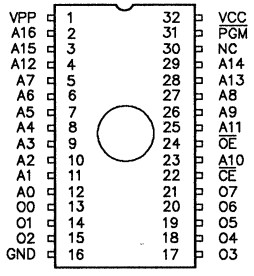
General Description

The ICT 27CX010 is a 1,048,576-bit CMOS high-speed UV-Erasable Programmable Read Only Memory, organized as 128K-bytes of 8 bits each. Available in a JEDEC-standard 32-pin package, the 27CX010 allows pin-compatible upgrades from 512K through 8M-bit EPROMS with minimal or no hardware changes. The 27CX010 is designed using advanced CMOS EPROM technology which provides ultra-fast access times (55, 70, 90ns max) and a low active power consumption (90mA max). The power consumption is further reduced (1mA max) with its special CMOS standby mode, when pin $\overline{CE}$ is deselected. The high-speed of the 27CX010 makes it ideal for operation with fast 16-bit and 32-bit microprocessors, eliminating the necessity of wait states. The 27CX010's high density allows the storage of operating systems and applications software, freeing the system's RAM for other uses. Popular third party vendor EPROM programmers will support the 27CX010 programming. An Auto Select mode provides for foolproof programmer operation by allowing EPROM programmers to read a special code from the 27CX010 to identify manufacturer and part type.

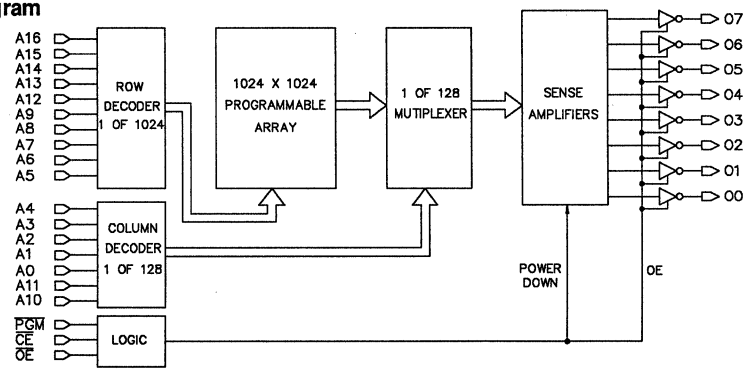
Pin Diagram

Pin Names

A0–A14	Address Inputs
$\overline{O0}$–O7	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program
GND	Ground
V_{CC}	Power Supply



Block Diagram



Functional Description

Erasure Characteristics

The 27CX010 are erased by exposure to an ultraviolet light source. For complete erasure, the recommended minimum integrated dose (UV intensity X exposure time) is 15 Watt-second/cm2 of ultraviolet light with a wavelength of 2537 A. For an ultraviolet lamp with a 12mW/cm2 power rating, the exposure time should be approximately 20 minutes, with the device placed within one inch of the lamp during erasure. Exposing the CMOS EPROM to high-intensity UV light for extended periods may affect device reliability. Also, exposure to fluorescent light or sunlight may erase the EPROM. Therefore, an opaque label or substance should be placed over the package window if the device is used in such an environment.

Programming Mode

After erasure, all bits of the EPROM are set to 1's. Programming of the 27CX010 stores 0's in the selected bit positions. The program mode is entered when a voltage between 12.0V and 13.0V is applied to the VPP pin, while /CE and /OE are held low.

Programming support is available from third-party manufacturers. For more information on programming support and programming specifications, please contact ICT.

Read Mode

The 27CX010 has two control functions, Chip Enable (/CE) and Output Enable (/OE), which must both be held low for data to be accessed from the EPROM. /CE is the power control and should be used for device selection. /OE is the output control and should be used to gate data to the output pins if the device is selected.

It is recommended that /CE be decoded and used as the primary device selecting function, while /OE should be made a common connection to all devices in the array and connected to the read line from the system control bus. This will assure that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular device.

Assuming the addresses are stable, address access time (t_{ACC}) is equal to the delay from /CE to the output (t_{CS}). Data is available at the outputs t_{OE} after the falling edge of /OE, assuming /CE has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The 27CX010 has two standby modes, a CMOS standby mode (/CE input held at $V_{CC} \pm 0.3V$) and a TTL standby mode (/CE held at V_{IH}). In the CMOS standby mode or power-down mode, the current consumed (I_{CC1}) is less than 1mA. During TTL standby mode the current (I_{CC2}) is less than 20mA, and the outputs O0-O7 are in the high impedance state, independent of /OE input.

Auto Select Mode

The Auto Select Mode allows the reading out of a two-byte binary code from the EPROM that will identify its manufacturer and part type. This mode is intended for use by programming equipment for the purpose of automatically matching the device being programmed with its corresponding programming algorithm. The two codes identified are the Manufacturer code and the Device code.

These codes are given in the Mode table. All identifiers for manufacturers and devices will exhibit odd parity with the MSB (O7) defined as the parity bit.

Program Inhibit Mode

Multiple 27CX010 devices can be programmed in parallel by wiring all like inputs of the EPROMs except for /CE or /PGM. Different data can also, be programmed into each EPROM while in parallel. Devices with /CE and /PGM held HIGH are inhibited from being programmed. The chosen device can then be programmed by setting /CE to a LOW TTL level, pulsing /PGM with a TTL LOW pulse, and applying 12.5V to VPP. (See mode table)

Program Verify Mode

A verify should be performed on the programmed bits of the 27CX010 to determine the correct programming of the EPROM.

This is accomplished by taking /CE and /OE to V_{IL}, setting /PGM at V_{IH}, and applying 12.5V to VPP. Data for the 27CX010 should be verified after time t_{OE} from the falling edge of /OE. (See mode table)

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	– 0.6 to +7.0	V
V_{IO}	Voltage Applied to All Pins Ex-	Relative to GND	–0.6 to V_{CC}+0.6	V
T_A	Ambient Temp., Power Applied		–65 to +150	°C
T_{ST}	Storage Temperature		–65 to +150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Ambient Temperature	Commercial	0	70	C
V_{CC}	Supply Voltage (Read)	Commercial	4.5	5.5	V
V_{CC}	Suppy Voltage (Program)	Commercial	5.75	6.5	V
V_{PP}	Program Voltage	Commercial	12.0	13.0	V

D.C. Electrical Characteristics[1,2]

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Level		2.0	VCC+.5	V
V_{IL}	Input LOW Level		–0.5	0.8	V
V_{OH}	Output HIGH Voltage[3]	V_{CC} = Min, I_{OH} = –4.0mA	2.4		V
V_{OL}	Output LOW Voltage[3]	V_{CC} = Min, I_{OL} = 12mA		0.45	V
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	Vout = 0V to V_{CC}		10	µA
I_{CC1}	VCC Standy Current (TTL)	/CE=V_{IH}, /OE=V_{IL}		20	mA
I_{CC2}	VCC Standby Current (CMOS)	/CE=V_{CC}-0.3V to V_{CC}+0.3V		1	mA
I_{CC3}	VCC Active Current	/CE=/OE=V_{IL}, f=tacc max	0.1	90	mA
I_{PP1}	VPP Current During Read	V_{PP} = 5.5V		100	µA

Capacitance

These measurements are periodically sample tested.

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C V_{CC} = 5.0V @ f = 1MHz		8	pF
C_{OUT}	Output Capacitance			8	pF
C_{IN2}	VPP Input Capacitance			20	pF

Notes:

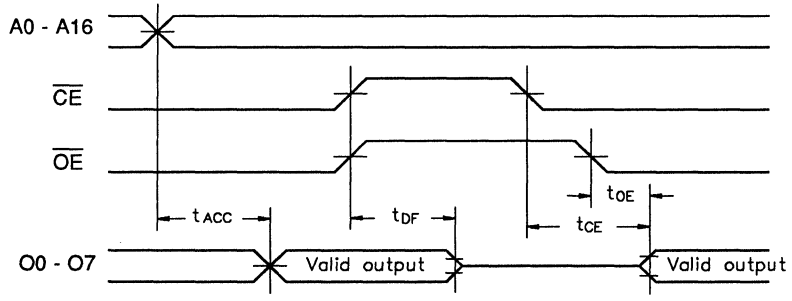
1. V_{CC} must be applied simultaneously or before V_{pp}, and removed simultaneously or after V_{PP}.
2. It is recommended that V_{PP} be connected directly to V_{CC} except during programming. The supply current will be I_{CC} + I_{PP1}.
3. The 27CX010 provides true CMOS output interface levels. The specifications shown are for a TTL interface.

A.C. Electrical Characteristics

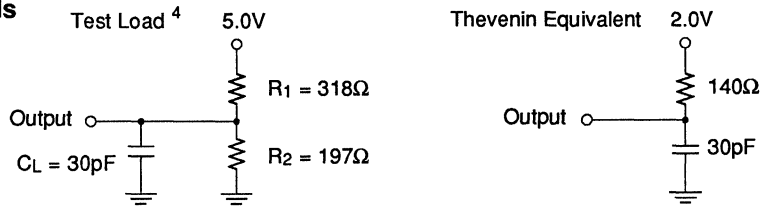
Over the Operating Range [3]

Symbol	Parameter	27CX010-55		27CX010-70		27CX010-90		Unit
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Access Time From Address To Output		55		70		90	nS
t_{CE}	Access Time From Chip Enable To Output		55		70		90	nS
t_{OE}	Access Time From Output Enable To Output[4]		30		40		50	nS
t_{DF}	Chip Disable to High-Z [4,5]		30		40		50	nS

Switching Waveforms



Test Loads



Notes:

3. Test conditions assume: signal transition times of 5 nS or less from the 10% and 90% points; timing reference levels of 1.5V (unless otherwise specified); and test loads shown.
4. t_{CE} and t_{OE} are measured from the input transition to $V_{REF} \pm 0.1V$. t_{CD} is measured from the input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$.
5. C_L includes scope and jig capacitance. t_{OE} is tested with $C_L = 5pF$.

Mode Table

Mode		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	VCC	A9	A0	Output
Read		VIL	VIL	X	X	VCC	X	X	DOUT
Standby		VIH	VIL	X	X	VCC	X	X	HI-Z
Output Disable		VIL	X	X	X	VCC	X	X	HI-Z
Program		VIL	VIH	VIL	VPP	VCC	X	X	DIN
Program Verify		VIL	VIL	VIH	VPP	VCC	X	X	DOUT
Program Inhibit		VIH	X	X	VPP	VCC	X	X	HI-Z
Auto Select	Manufactuer	VIL	VIL	X	X	VCC	VH	VIL	01H
	Device	VIL	VIL	X	X	VCC	VH	VIH	0EH

VIL = Input Low Voltage, VIH = Input High Voltage, VH = High Voltage (12.5V), X = Don't Care

INTERNATIONAL CMOS TECHNOLOGY, INC.

Product Preview

27CX256
256K (32K x 8) CMOS High-Speed EPROM

Features

- **Advanced CMOS EPROM Technology**
- **High Performance**
  - 27CX256C-40 t_{AA} = 40ns max
  - 27CX256C-45 t_{AA} = 45ns max
  - 27CX256C-70 t_{AA} = 70ns max
- **Low Power Consumption**
  - 90mA Max Active
  - 20mA Max Standby, TTL interface
  - 1mA Max Standby, CMOS interface
- **TTL-Compatible I/O**
- **Reprogrammability**
  - Adds convenience, reduces costs
  - Windowed package for UV erasure
  - Allows 100% factory testing
- **Programming Support**
  - Supported by popular programmers
  - Fast programming algorithm
  - Auto Select mode feature
- **Packaging**
  - JEDEC-standard 28-pin CERDIP

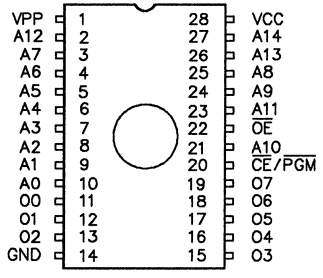
General Description

The ICT 27CX256 is a 262,144-bit CMOS high-speed UV-Erasable Programmable Read Only Memory, organized as 32K-bytes of 8 bits each. Available in a JEDEC-standard 28-pin package, the 27CX256 allows pin-compatible upgrades from 32K through 512K-bit EPROMS with minimal or no hardware changes. The 27CX256 is designed using advanced CMOS EPROM technology which provides ultra-fast access times (40, 45, 70ns max) and a low active power consumption (90mA max). The power consumption is further reduced (1mA max) with its special CMOS standby mode, when pin $\overline{CE}$ is deselected. The high-speed of the 27CX256 makes it ideal for operation with fast 16-bit and 32-bit microprocessors, eliminating the necessity of wait states. The 27CX256's high density allows the storage of operating systems and applications software, freeing the system's RAM for other uses. Popular third party vendor EPROM programmers will support the 27CX256 programming. An Auto Select mode provides for foolproof programmer operation by allowing EPROM programmers to read a special code from the 27C256 to identify manufacturer and part type.

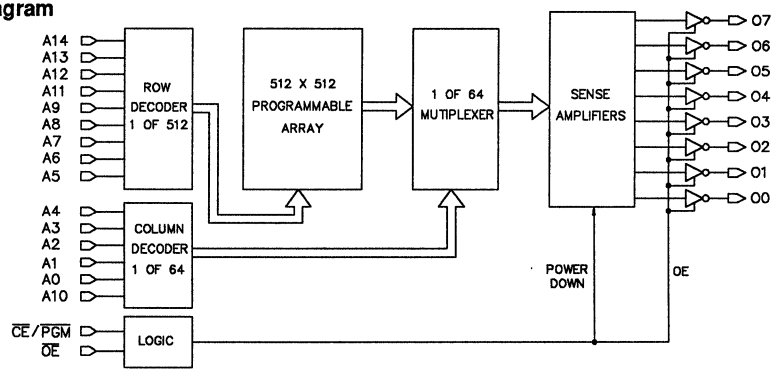
Pin Diagram

Pin Names

A0–A14	Address Inputs
$\overline{O0}$–O7	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program
GND	Ground
Vcc	Power Supply



Block Diagram



CMOS PEEL Devices

5

CMOS PEEL Devices

PEEL™ Devices (Programmable Electrically Erasable Logic devices), combine CMOS and EEPROM technologies to offer an attractive alternative to conventional programmable logic devices (PLDs). PEEL devices eliminate conventional PLD design tradeoffs by providing a balance of the performance, flexibility, ease of design, and practicality needed by logic designers today.

PEEL Device Features

- **CMOS Performance**
  - — Low power consumption
  - — Low operating temperature
- **Architectural Flexibility**
  - — Emulation of other PLDs (PAL, GAL, EPLD, FPLA)
  - — Programmable-AND, -AND/OR Arrays
  - — Enhanced architecture features
- **Ease of Design**
  - — Free PEEL Development Software
  - — Low-cost PEEL Development System
  - — Third-party development and programmer support
- **Electrically Erasable Re-programmability**
  - — Re-programmable in a plastic package
  - — Convienient and cost saving for design
  - — Low-risk re-programmable inventory
  - — 100% factory testable

INTERNATIONAL CMOS
TECHNOLOGY, INC.

PEEL™18CV8
CMOS Programmable Electrically Erasable Logic Device

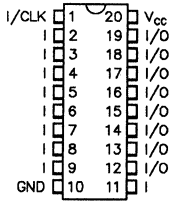
Features

- **Advanced CMOS EEPROM Technology**
- **Low Power Consumption**
  - 20mA standby + 0.7mA/MHz max
- **High Performance**
  - t_{PD} = 25ns max, fmax=33.3MHz
- **EE Instant Reprogrammability**
  - 100% factory tested
  - Cost-effective windowless package
  - Erases and programs in seconds
  - Adds convenience, reduces field retrofit and development costs
- **Foolproof Design Security**
  - Prevents unauthorized reading or copying of design
- **Architectural Flexibility**
  - 74 product term x 36 input array
  - Up to 18 inputs and 8 I/O pins
  - Independent configurable I/O macro cells
  - Synchronous preset, asynchronous clear
  - Independent output enables
- **Application Versatility**
  - Replaces SSI/MSI logic
  - Emulates bipolar PAL* devices, GAL* devices, and EPLDs
  - Simplifies inventory control
  - Allows new design possibilities
- **Development/Programmer Support**
  - Third party software and programmers
  - ICT PEEL Development System and Software

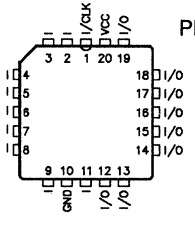
General Description

The ICT PEEL18CV8 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally flexible alternative to early-generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the performance of the PEEL18CV8 rivals speed parameters of bipolar PLDs with a dramatic reduction in power consumption. EE reprogrammability simplifies inventory management, reduces development and field retrofit costs, enhances testability to ensure 100% field programmability and function, while allowing for low-cost "windowless" packaging in a 20-pin, 300-mil DIP. The PEEL18CV8's flexible architecture allows the device to replace SSI/MSI logic circuitry. ICT's JEDEC file translator allows the PEEL18CV8 to replace existing 20-pin PLDs without the need to rework the existing design. Development and programming support for the PEEL18CV8 is provided by popular third-party PC-based development tools and programmers from third-party manufacturers. ICT also offers a free design software package and a low-cost development system.

Pin Configuration (Figure 1)

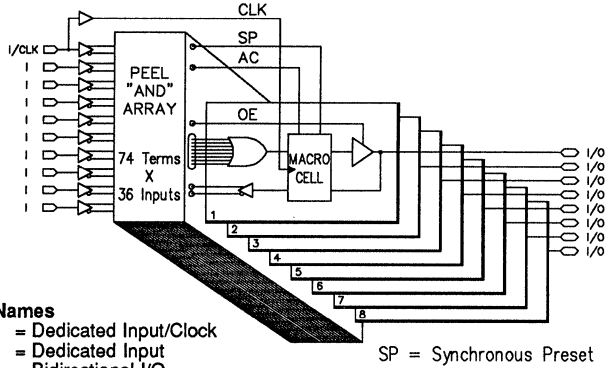


DIP



PLCC

Block Diagram (Figure 2)



Pin Names

I/CLK	= Dedicated Input/Clock
I	= Dedicated Input
I/O	= Bidirectional I/O
GND	= Ground
Vcc	= Power Supply

SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

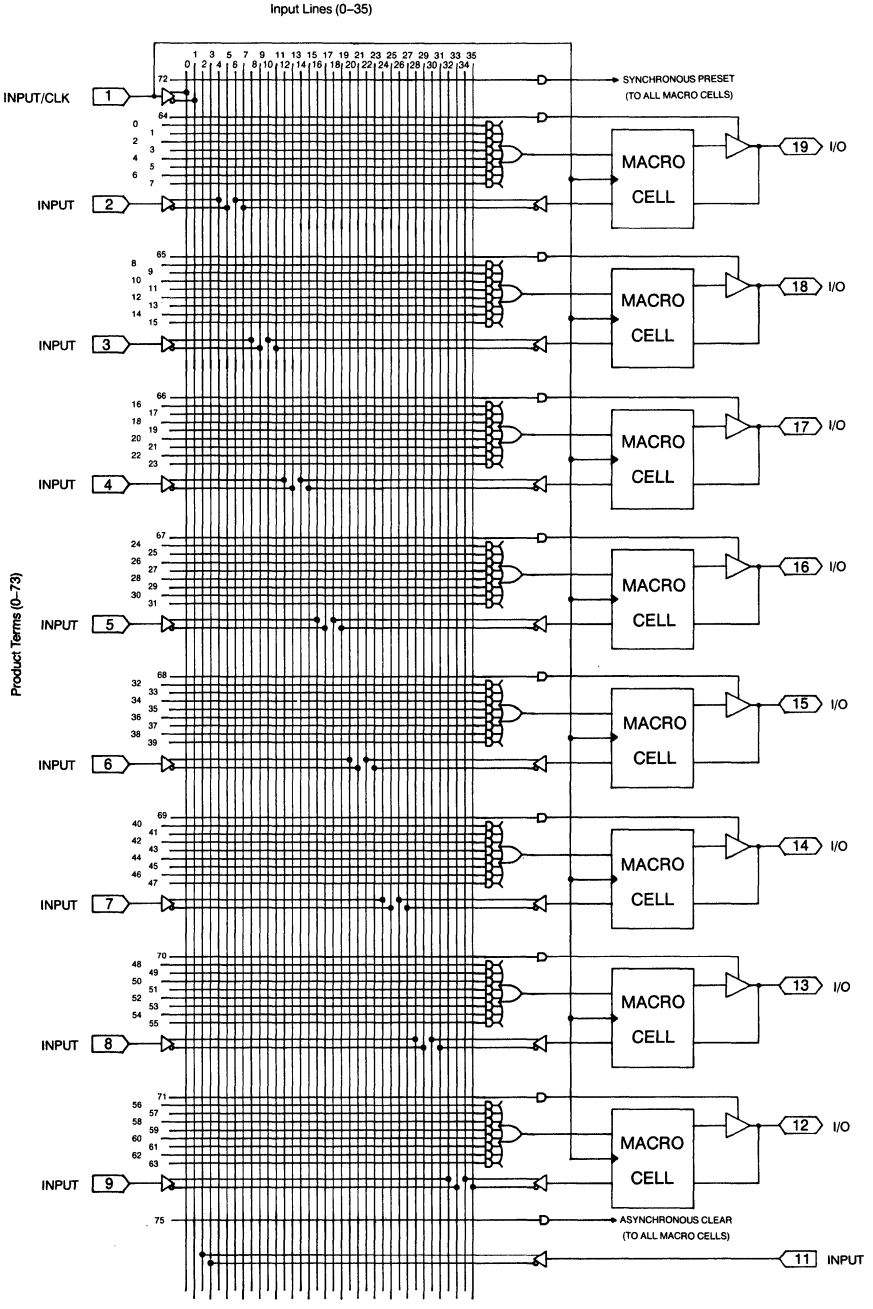


Figure 3. PEEL18CV8 Logic Array Diagram

Function Description

The PEEL18CV8 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL18CV8 architecture is illustrated in the block diagram of figure 2. Ten dedicated inputs and 8 I/Os provide up to 18 inputs and 8 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL18CV8 can implement up to 8 sum-of-products logic expressions.

Associated with each of the 8 OR functions is an I/O macrocell which can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL18CV8 (shown in figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

36 Input Lines:

- 20 input lines carry the true and compliment of the signals applied to the 10 input pins
- 16 additional lines carry the true and compliment values of feedback or input signals from the 8 I/Os

74 product terms:

- 64 product terms (arranged in groups of 8) used to form sum of product functions
- 8 output enable terms (one for each I/O)
- 1 global synchronous preset term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 36-input AND gate. A product term which is connected to both the true and compliment of an input signal will always be FALSE and thus will not effect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE.

When programming the PEEL18CV8, the device programmer first performs a bulk erase to instantly remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program all of the connections on unused product terms so that they will have no effect on the output function)

Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL18CV8 to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the four EEPROM bits controlling these multiplexers. These bits determine: output polarity; output type (registered or non-registered); and input/feedback path (bi-directional I/O, combinatorial feedback, or register feedback). Refer to table 1 for details.

Equivalent circuits for the twelve macrocell configurations are illustrated in figure 5. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9, and 10) the macrocell provides eight additional configurations. When creating a PEEL device design, the desired macrocell configuration generally is specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity
Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable
The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select
The PEEL18CV8 macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell may be obtained from three different locations: from the I/O pin (bi-directional I/O); directly from the Q output of the flip-flop (registered feedback); or directly from the OR gate (combinatorial feedback).

Bi-directional I/O
The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

Combinatorial Feedback
The signal-select multiplexer gives the macrocell the ability to feedback the output of either the OR gate, bypassing the output buffer, regardless of whether the output function is registerd or combinatorial. This feature allows the creation of asynchronous latches,

5

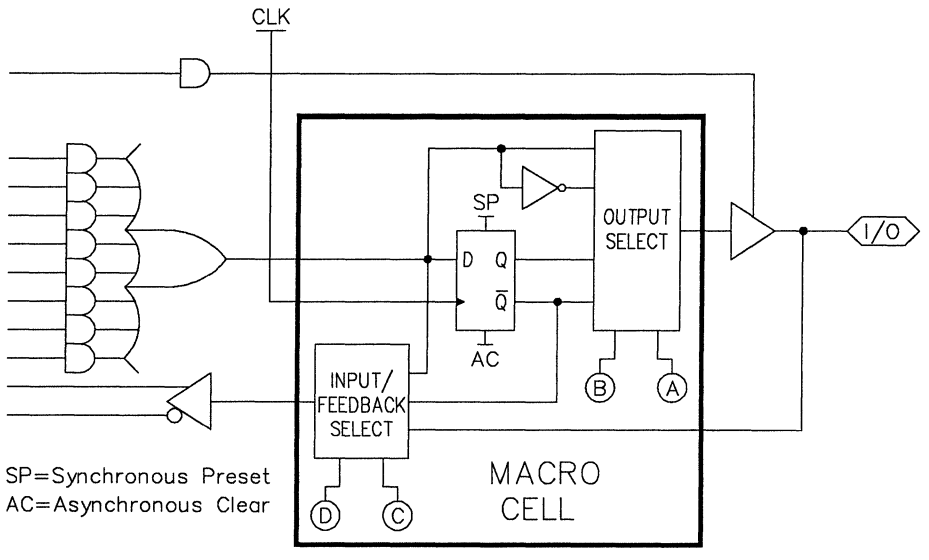


Figure 4. Block Diagram of the PEEL18CV8 I/O Macrocell

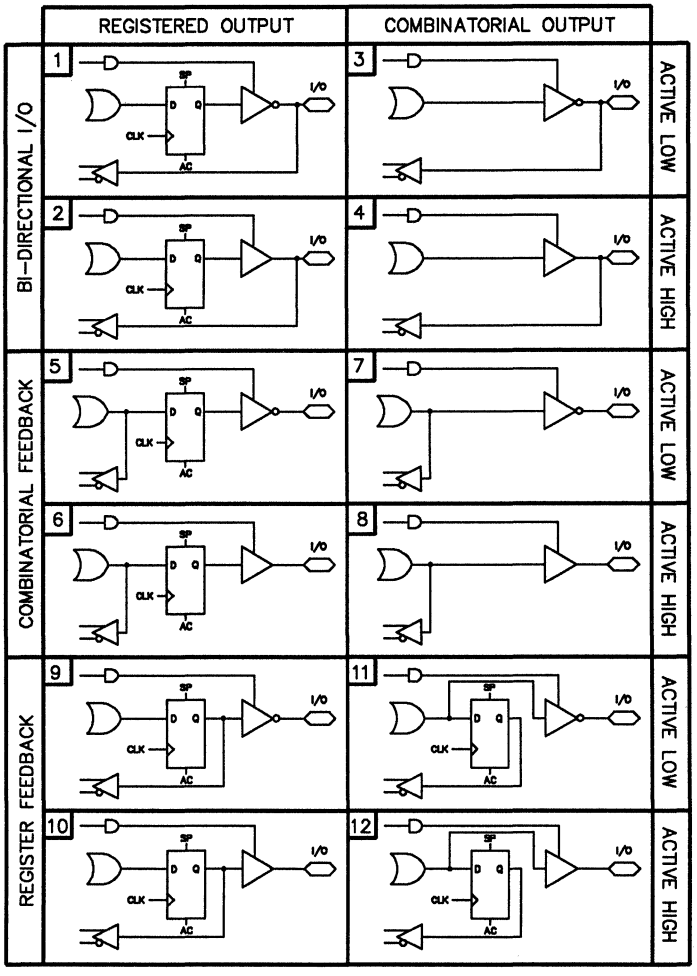


Figure 5. Equivalent Circuits for the Twelve Configurations of the PEEL18CV8 I/0 Macrocell.

Configuration #	A	B	C	D	Input/Feedback Select	Output Select	
1	1	1	1	1	Bi-Directional I/O	Register	Active Low
2	0	1	1	1	"	"	Active High
3	1	0	1	1	"	Combinatorial	Active Low
4	0	0	1	1	"	"	Active High
5	1	1	1	0	Combinatorial Feedback	Register	Active Low
6	0	1	1	0	"	"	Active High
7	1	0	1	0	"	Combinatorial	Active Low
8	0	0	1	0	"	"	Active High
9	1	1	0	0	Register Feedback	Regisiter	Active Low
10	1	1	0	0	"	"	Active High
11	1	0	0	0	"	Combinatorial	Active Low
12	0	0	0	0	"	"	Active High

Table 1. PEEL18CV8 Macrocell Configuration Bits

Bi-directional I/O
The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

Combinatorial Feedback
The signal-select multiplexer gives the macrocell the ability to feedback the output of either the OR gate, bypassing the output buffer, regardless of whether the output function is registerd or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7, and 8 in figure 5.)

Registered Feedback
Feedback also can be taken from the register, regardless of whether the output function is to be combinatorial or registered. When implementing combinatorial output function, registered feedback allows for the internal latching of states without giving up the use of the external output.

Design Security
The PEEL18CV8 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permenant damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [6]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 125	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges[2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	V
T_A	Ambient Temperature	Commercial	0	+ 70	°C
		Industrial	− 40	+ 85	°C
T_R	Clock Rise Time	See note 4		250	ns
T_F	Clock Fall Time	See note 4		250	ns
T_{RVCC}	V_{CC} Rise Time	See note 4		10	ms

D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 8mA		0.45	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0.5V [10]	− 30	− 100	mA
I_{CCSC}	V_{CC} Current, Standby, CMOS	V_{IN} = V_{CC} or GND [5]		20 (30)*	mA
I_{CCAC}	V_{CC} Current, Active, CMOS	V_{IN} = V_{CC} or GND. All outputs open. [5]		I_{CCSC} + 0.7mA/MHz	mA
I_{CCST}	V_{CC} Current, Standby, TTL	V_{IN} = V_{IL} or V_{IH} [5]		25 (35)*	mA
I_{CCAT}	V_{CC} Current, Active, TTL	V_{IN} = V_{IL} or V_{IH}. All outputs open. [5]		I_{CCST} + 0.7mA/MHz	mA
C_{IN} [8]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT} [8]	Output Capacitance			12	pF

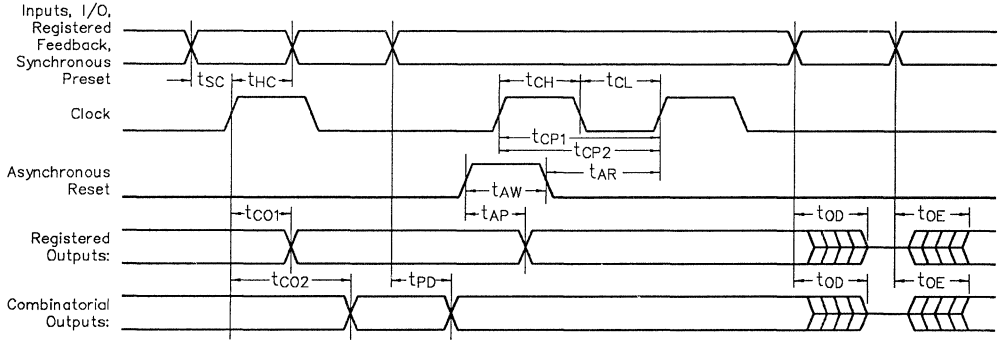
* Numbers in parenthesis specify parameters for industrial temperature range.

A.C. Electrical Characteristics

Over the Operating Range[3,12]

Symbol	Parameter	18CV8-25		18CV8-30		18CV8-35		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input[4] or feedback to non-registered output		25		30		35	nS
t_{OE}	Input[4] to output enable[6]		25		30		35	nS
t_{OD}	Input[4] to output disable[6]		25		30		35	nS
t_{CO1}	Clock to output		15		20		20	nS
t_{CO2}	Clock to combinatorial output delay via internal registered feedback		35		45		50	nS
t_{SC}	Input[4] or feedback setup to clock	20		25		30		nS
t_{HC}	Input[4] hold after clock	0		0		0		nS
t_{CL},t_{CH}	Clock width - clk low time, clk high time [5]	15		15		15		nS
t_{CP1}	Clock period (register feedback to registered output via internal path)	30		40		45		nS
f_{max1}	Maximum clock frequency ($1/t_{CP1}$)	33.3		25		22.2		MHz
t_{CP2}	Clock period (t_{SC} + t_{CO1})	35		45		50		nS
f_{max2}	Maximum clock frequency ($1/t_{CP2}$)	28.5		22.2		20		MHz
t_{AW}	Asynchronous clear pulse width	25		30		35		nS
t_{AP}	Input[4] to asynchronous clear		30		35		40	nS
t_{AR}	Asynchronous Reset Recovery Time		20		35		30	nS
t_{RESET}	Power-on reset time for registers in clear state		5		5		5	µS

Switching Waveforms



Notes

1. Minimum DC input is -0,5V, however inputs may undershoot to -2.0V for periods less than 20ns
2. Contact ICT for other operating ranges. (Industrial, Mil-temp.)
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
5. I/O pins are open (no load).
6. "Input" refers to Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to V_{OH}-0.1V or V_{OL}+0.1V; V_{REF}=1.90V for TTL interface tor 2.375V for CMOS interface.
8. Capacitance are tested on a sample basis.
9. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration less than 1 second.
11. PEEL Device test loads are specified at the end of this section

INTERNATIONAL CMOS
TECHNOLOGY, INC.

PEEL™18CV8-15/PEEL18CV8-20
CMOS Programmable Electrically Erasable Logic Device

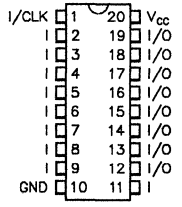
Features

- **Advanced CMOS EEPROM Technology**
- **Low Power Consumption**
  - CMOS: 80mA standby + 0.5mA/MHz max
  - TTL: 90mA standby + 0.5mA/MHz max
- **High Performance**
  - 18CV8-15: t_{PD}=15ns max, fmax=50MHz
  - 18CV8-20: t_{PD}=20ns max, fmax=41.6MHz
- **EE Instant Reprogrammability**
  - 100% factory tested
  - Cost-effective windowless package
  - Erases and programs in seconds
  - Reduces retrofit and development costs
  - Provides low risk inventory
- **Foolproof Design Security**
  - Prevents unauthorized reading or copying of design
- **Architectural Flexibility**
  - 74 product term x 36 input array
  - Up to 18 inputs and 8 I/O pins
  - Independently programmable 12-configuration I/O macro cells
  - Synchronous preset, asynchronous clear
  - Independent output enables
- **Application Versatility**
  - Replaces SSI/MSI logic
  - Emulates PAL*, GAL* and EPLDs
  - Simplifies inventory control
  - Allows new design possibilities
- **Development/Programmer Support**
  - Third party software and programmers
  - ICT PEEL Development System and Software

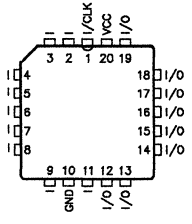
General Description

The ICT PEEL18CV8-15 or PEEL18CV8-20 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally flexible alternative to early-generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the performance of the PEEL18CV8 rivals speed parameters of bipolar PLDs with a dramatic reduction in power consumption. EE reprogrammability simplifies inventory management, reduces development and field retrofit costs, enhances testability to ensure 100% field programmability and function, while allowing for low-cost "windowless" packaging in a 20-pin, 300-mil DIP. The PEEL18CV8's flexible architecture allows the device to replace SSI/MSI logic circuitry. ICT's JEDEC file translator allows the PEEL18CV8 to replace existing 20-pin PLDs without the need to rework the existing design. Development software and programming support for the PEEL18CV8 is provided by ICT and third-party manufacturers. The PEEL18CV8-15 and -20 are function and programming compatible with the standard PEEL18CV8. Please refer to the standard PEEL18CV8 data sheet for more detailed description.

Pin Configuration

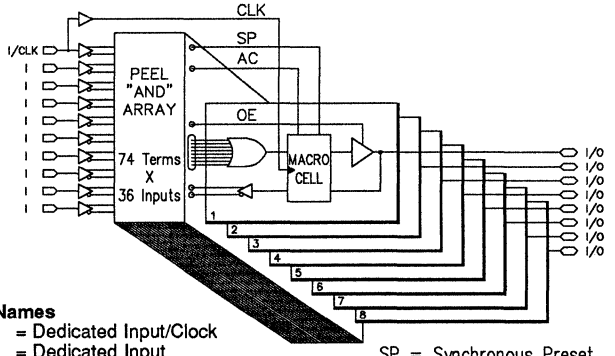


DIP



PLCC

Block Diagram



Pin Names

I/CLK	= Dedicated Input/Clock
I	= Dedicated Input
I/O	= Bidirectional I/O
GND	= Ground
Vcc	= Power Supply

SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permenant damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 125	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges[2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Ambient Temperature	Commercial	0	+ 70	°C
T_R	Clock Rise Time	See note 4		250	ns
T_F	Clock Fall Time	See note 4		250	ns
T_{RVCC}	V_{CC} Rise Time	See note 4		10	ms

D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 12mA		0.45	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0.5V [10]	− 30	− 100	mA
I_{CCSC}	V_{CC} Current, Standby, CMOS	V_{IN} = V_{CC} or GND [5]		80	mA
I_{CCAC}	V_{CC} Current, Active, CMOS	V_{IN} = V_{CC} or GND [5,]		I_{CCSC} + 0.5mA/MHz	mA
I_{CCST}	V_{CC} Current, Standby, TTL	V_{IN} = V_{IL} or V_{IH} [5]		90	mA
I_{CCAT}	V_{CC} Current, Active, TTL	V_{IN} = V_{IL} or V_{IH} [5]		I_{CCST} + 0.5mA/MHz	mA
C_{IN} [8]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT} [8]	Output Capacitance			12	pF

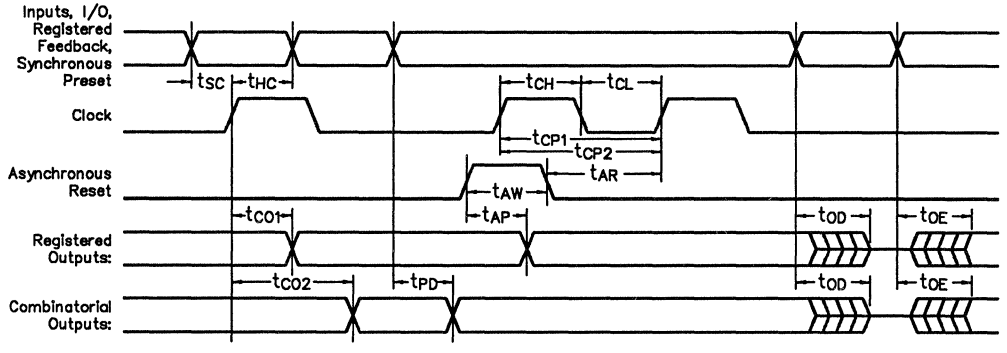
5

A.C. Electrical Characteristics

Over the Operating Range [9,11]

Symbol	Parameter	18CV8-15		18CV8-20		Unit
		Min	Max	Min	Max	
t_{PD}	Input[6] or feedback to non-registered output		15		20	nS
t_{OE}	Input[6] to output enable[7]		15		20	nS
t_{OD}	Input[6] to output disable[7]		15		20	nS
t_{CO1}	Clock to output		12		15	nS
t_{CO2}	Clock to combinatorial output delay via internal registered feedback		25		30	nS
t_{SC}	Input[6] or feedback setup to clock	12		15		nS
t_{HC}	Input[6] hold after clock	0		0		nS
t_{CL},t_{CH}	Clock width - clk low time, clk high time [4]	10		12		nS
t_{CP1}	Minimum clock period (register feedback to registered output via internal path)	20		24		nS
f_{max1}	Maximum clock frequency ($1/t_{CP1}$)	50		41.6		MHz
t_{CP2}	Minimum clock period ($t_{SC} + t_{CO1}$)	24		30		nS
f_{max2}	Maximum clock frequency ($1/t_{CP2}$)	41.6		33.3		MHz
t_{AW}	Asynchronous clear pulse width	15		20		nS
t_{AP}	Input[6] to asynchronous clear		20		25	nS
t_{AR}	Asynchronous Reset Recovery Time		10		15	nS
t_{RESET}	Power-on reset time for registers in clear state[4]		5		5	µS

Switching Waveforms



1. Minimum DC input is -0,5V, however inputs may undershoot to -2.0V for periods less than 20ns
2. Contact ICT for other operating ranges. (Industrial, Mil-temp.)
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
5. I/O pins are open (no load).
6. "Input" refers to Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to V_{OH}-0.1V or V_{OL}+0.1V; $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitance are tested on a sample basis.
9. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration less than 1 second.
11. PEEL Device test loads are specified at the end of this section

PEEL™18CV8-10/PEEL™18CV8-12
CMOS Programmable Electrically Erasable Logic Device

Features

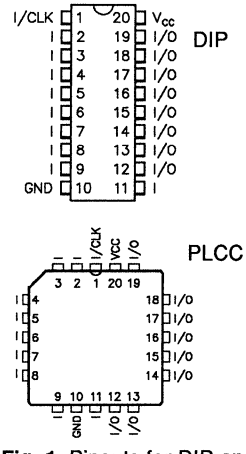
- **1-Micron CMOS EEPROM Technology**
- **Low Power Consumption**
  - CMOS: 80mA standby + 0.5mA/MHz max
  - TTL: 90mA standby + 0.5mA/MHz max
- **Ultra High Performance**
  - 18CV8P-10: t_{PD} = 10ns max
  - 18CV8P-12: t_{PD} = 12ns max
- **EE Instant Reprogrammability**
  - 100% factory tested
  - Cost-effective windowless package
  - Erases and programs in seconds
  - Reduces retrofit and development costs
  - Provides low risk inventory
- **Foolproof Design Security**
  - Prevents unauthorized reading or copying of design
- **Architectural Flexibility**
  - 74 product term x 36 input array
  - Up to 18 inputs and 8 I/O pins
  - Independently programmable 12-configuration I/O macro cells
  - Synchronous preset, asynchronous clear
  - Independent output enables
- **Application Versatility**
  - Replaces SSI/MSI logic
  - Emulates PAL*, GAL* and EPLDs
  - Simplifies inventory control
  - Allows new design possibilities
- **Development/Programmer Support**
  - PC-based development tools and programmer support from ICT and third-party manufacturers

5

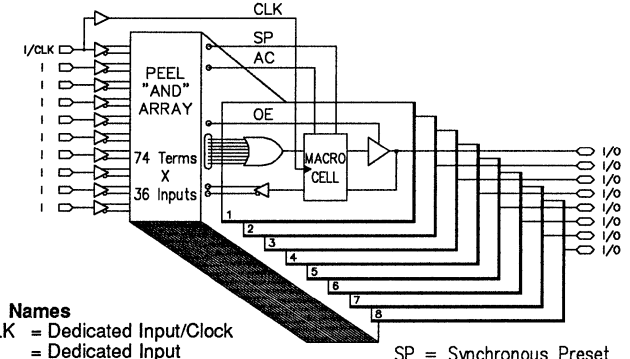
General Description

The ICT PEEL18CV8-10 or PEEL18CV8-12 is a CMOS Programmable Electrically Erasable Logic devices that provides a high-performance, low-power, reprogrammable, and architecturally flexible alternative to early-generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the performance of the PEEL18CV8 rivals speed parameters of bipolar PLDs with a dramatic reduction in power consumption. EE reprogrammability simplifies inventory management, reduces development and field retrofit costs, enhances testability to ensure 100% field programmability and function, while allowing for low-cost "windowless" packaging in a 20-pin, 300-mil DIP. The PEEL18CV8's flexible architecture allows the device to replace SSI/MSI logic circuitry. ICT's JEDEC file translator allows the PEEL18CV8 to replace existing 20-pin PLDs without the need to rework the existing design. Development and programming support for the PEEL18CV8 is provided by popular third-party PC-based development tools and programmers from third-party manufacturers. ICT also offers a free design software package and a low-cost development system.

Pin Configuration



Block Diagram



Pin Names

I/CLK	= Dedicated Input/Clock
I	= Dedicated Input
I/O	= Bidirectional I/O
GND	= Ground
Vcc	= Power Supply

SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

Fig. 1. Pinouts for DIP and PLCC

Figure 2. Block diagram of the PEEL18CV8

INTERNATIONAL CMOS
TECHNOLOGY, INC.

PEEL™ 20CG10

CMOS Programmable Electrically Erasable Logic Device

Features

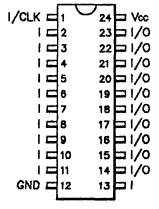
- **Advanced CMOS EEPROM Technology**
- **High Performance, Low Power Consumption**
  - — t_{PD} = 20ns, fmax= 40MHz
  - — I_{CC} = 55mA + 0.5mA/MHz
- **EE Reprogrammability**
  - — Low risk reprogrammable inventory
  - — Superior programming and functional yield
  - — Erases and programs in seconds
- **Development and Programming Support**
  - — Third-party software and programmers
  - — ICT PEEL Development System and Software
- **Architectural Flexibility**
  - — 92 product term X 44 input AND array
  - — Up to 22 inputs and 10 outputs
  - — Independently programmable 12-configuration I/O macrocells
  - — Synchronous preset, asynchronous clear
  - — Independently programmable output enables
- **Application Versatility**
  - — Replaces random SSI/MSI logic
  - — Emulates 24-pin bipolar PAL devices
  - — Convert 24-pin PAL and EPLD designs with ICT software
  - — Superset compatible with the CMOS PALC20G10

General Description

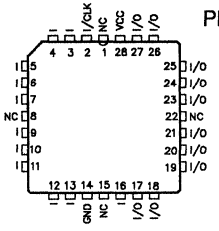
The ICT PEEL20CG10 is a CMOS Programmable Electrically Erasable Logic Device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL20CG10 rivals speed parameters of comparable bipolar PLDs while dramatically improving power consumption. EE reprogrammability allows for cost effective plastic packaging, low risk inventory, reduced development and retrofit costs, and enhanced testability to ensure 100% field programmability and function.

The PEEL20CG10's flexible architecture and ICT's JEDEC file translator allows the PEEL20CG10 to replace bipolar 24-pin PAL devices without the need to rework the existing design. Applications for the PEEL20CG10 include: replacement of random SSI/MSI logic circuitry; emulation of 24-pin bipolar PAL devices; and user customized sequential and combinatorial functions such as counters, shift registers, state machines, address decoders, multiplexers, etc. Development and programming support for the PEEL20CG10 is provided by ICT and third-party manufacturers.

Pin Configuration (Figure 1)

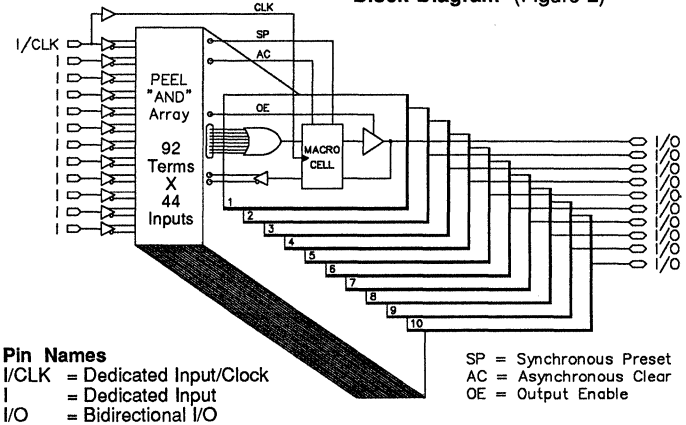


DIP



PLCC

Block Diagram (Figure 2)



Pin Names

I/CLK	= Dedicated Input/Clock
I	= Dedicated Input
I/O	= Bidirectional I/O
GND	= Ground
Vcc	= Power Supply

SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

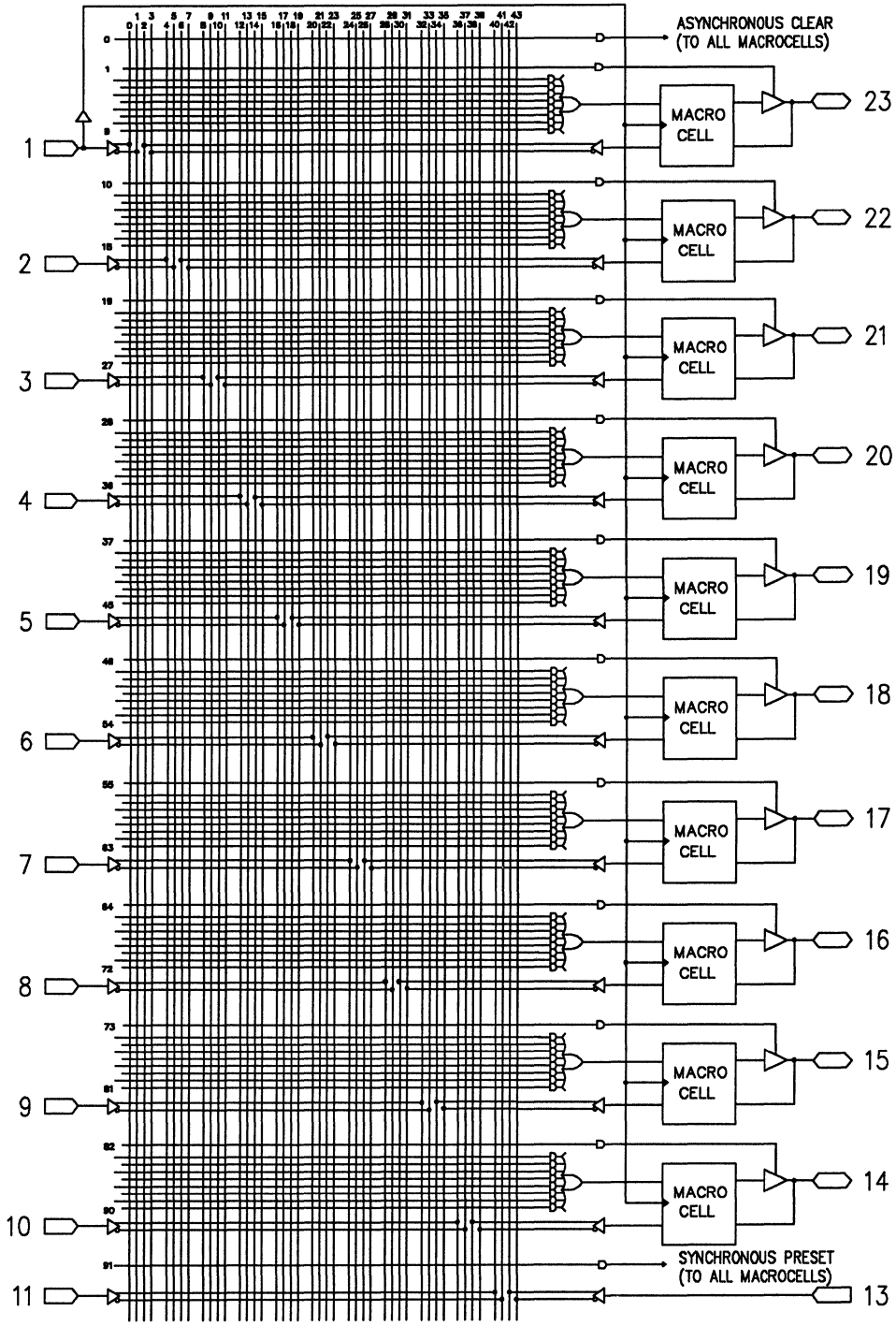


Figure 3. PEEL20CG10 Logic Array Diagram

Function Description

The PEEL20CG10 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL20CG10 architecture is illustrated in the block diagram of figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL20CG10 can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL20CG10 (shown in figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 24 input lines carry the true and complement of the signals applied to the 12 input pins
- 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

92 product terms:

- 80 product terms (8 per I/O)
- 10 output enable terms (one for each I/O)
- 1 global synchronous present term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and complement of an input signal will always be FALSE and thus will not effect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE.

When programming the PEEL20CG10, the device programmer first performs a bulk erase to instantly remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program the connections on unused product terms so that they will have no effect on the output function)

Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL20CG10 to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the four EEPROM bits controlling these multiplexers. These bits determine: output polarity; output type (registered or non-registered); and input/feedback path (bi-directional I/O, combinatorial feedback, or register feedback). Table 1 shows the bit settings for each of the twelve macrocell configurations.

Equivalent circuits for the twelve macrocell configurations are illustrated in figure 5. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9, and 10) the macrocell provides eight configurations that are unavailable in any PAL device.

Output Type

The signal from the OR array can be fed directly to the output pin or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity
Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable
The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select
The PEEL20CG10 macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell may be obtained from three different locations: from the I/O pin (bi-directional I/O); directly from the Q output of the flip-flop (registered feedback); or directly from the OR gate (combinatorial feedback).

Bi-directional I/O
The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

Combinatorial Feedback
The signal-select multiplexer gives the macrocell the ability to feedback the output directly from the OR gate, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7, and 8 in figure 5.)

Registered Feedback

Feedback also can be taken from the register, regardless of whether the output function is to be combinatorial or registered. When implementing configurations 11 and 12 in figure 5, the register can be used for internal latching of data while leaving the external output free for combinatorial functions.

Design Security
The PEEL20CG10 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

5

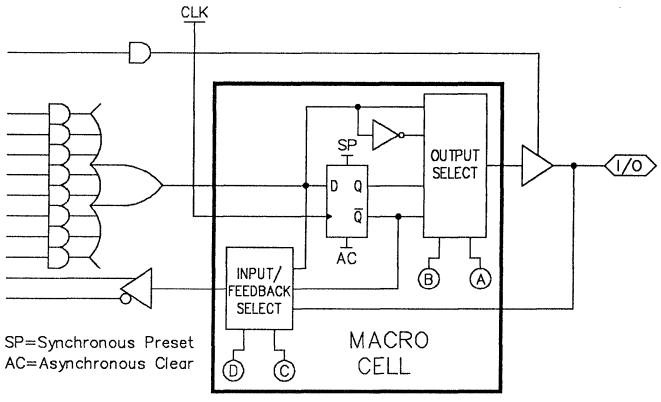


Figure 4. Block Diagram of the PEEL20CG10 I/O Macrocell

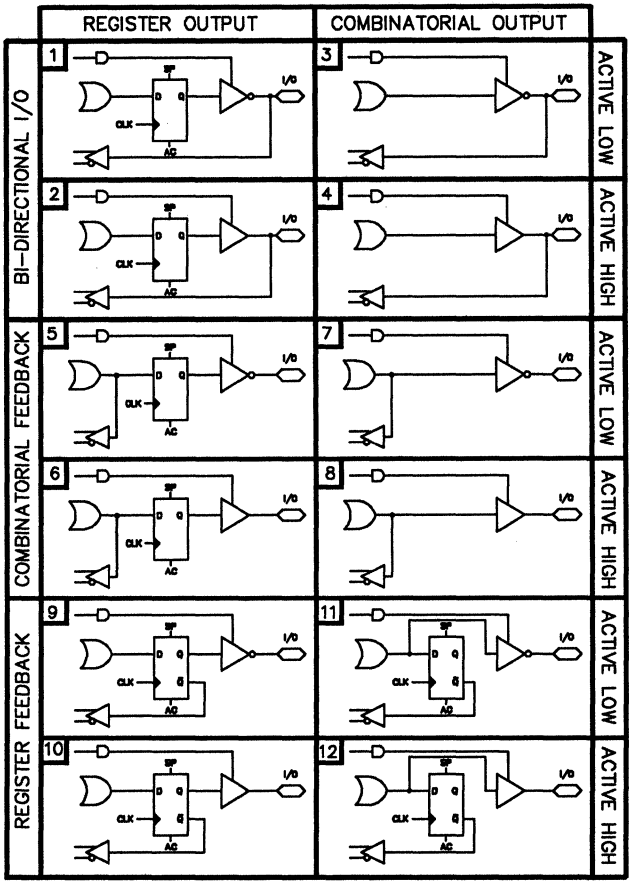


Figure 5. Equivalent Circuits for the Twelve Configurations of the PEEL20CG10 I/0 Macrocell.

Configuration		Input/Feedback Select	Output Select	
#	A B C D			
1	0 0 1 0	Bi-Directional I/O	Register	Active Low
2	1 0 1 0	"	"	Active High
3	0 1 0 0	"	Combinatorial	Active Low
4	1 1 0 0	"	"	Active High
5	0 0 1 1	Combinatorial Feedback	Register	Active Low
6	1 0 1 1	"	"	Active High
7	0 1 1 1	"	Combinatorial	Active Low
8	1 1 1 1	"	"	Active High
9	0 0 0 0	Register Feedback	Regisiter	Active Low
10	1 0 0 0	"	"	Active High
11	0 1 1 0	"	Combinatorial	Active Low
12	1 1 1 0	"	"	Active High

Table 1. PEEL20CG10 Macrocell Configuration Bits

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 125	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Alternate Source Symbol*	Parameter	Conditions	Min	Max	Unit
V_{CC}	V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	T_A	Ambient Temperature	Commercial [2]	0	70	°C
T_R		Clock Rise Time	See note 4		250	nS
T_F		Clock Fall Time	See note 4		250	nS
T_{RVCC}		VCC Rise Time	See note 4		10	mS

D.C. Electrical Characteristics

Over the operating range

Symbol	Alternate Source Symbol*	Parameter	Conditions	Min	Max	Unit
V_{OH}	V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = −4.0mA	2.4		V
V_{OHC}		Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 8mA		0.5	V
V_{OLC}		Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IX}	I_{IL},I_{IH},I_{IX}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0.5V [10]	− 30	− 90	mA
I_{CCAC}	I_{CC}	V_{CC} Active Current CMOS	V_{IN} = Vcc or GND [5,11]		55 (*65) + 0.5mA/MHz	mA
I_{CCAT}	I_{CC}	V_{CC} Active Current, TTL	V_{IN} = V_{IL} or V_{IH} [5,11]		65 (*75) + 0.5mA/MHz	mA
C_{IN} [8]	C_{IN}	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT} [8]	C_{OUT}	Output Capacitance			12	pF

* Alternate source symbols are shown to compare PEEL20CG10 specifications to other pin-compatible devices.

* 20CG10-20 only

5

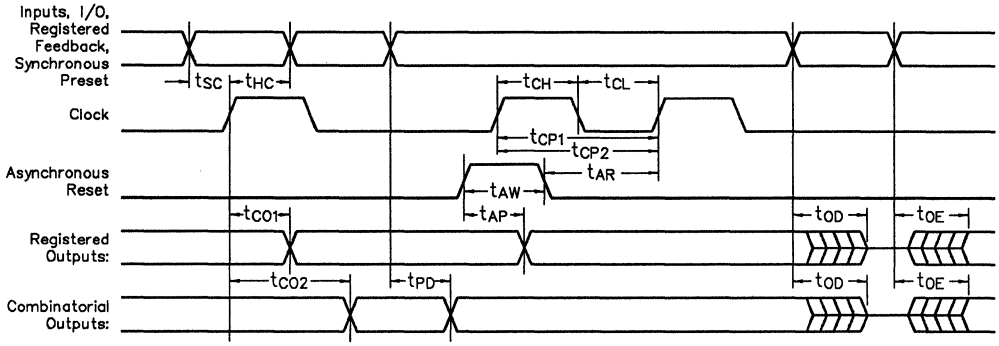
A.C. Electrical Characteristics

Over the Operating Range [9,12]

Symbol	Alternate Source Symbol*	Parameter	20CG10-20		20CG10-25		20CG10-35		Unit
			Min	Max	Min	Max	Min	Max	
t_{PD}	t_{PD}	Input[6] or feedback to non-registered output		20		25		35	ns
t_{OE}	t_{EA}	Input [6] to output enable [7]		20		25		30	ns
t_{OD}	t_{ER}	Input [6] to output disable [7]		20		25		30	ns
t_{CO1}	t_{CO}	Clock to output		15		15		20	ns
t_{CO2}		Clock to combinatorial output delay via internal registered feedback		30		35		45	ns
t_{SC}	t_S	Input [6] or feedback setup to clock	12		15		30		ns
t_{HC}	t_H	Input [6] hold after clock	0		0		0		ns
t_{CL},t_{CH}	t_W	Clock width - clock low time, clock high time [4]	12		13		15		ns
t_{CP1}		Minimum clock period (register feedback to registered output via internal path)	25		27		45		ns
f_{max1}		Maximum clock frequency ($1/t_{CP1}$)	40		37		22.2		MHz
t_{CP2}	t_P	Minimum clock period ($t_{SC} + t_{CO1}$)	27		30		50		ns
f_{max2}	f_{max}	Maximum clock frequency ($1/t_{CP2}$)	37		33.3		20		MHz
t_{AW}	t_{AW}	Asynchronous Reset pulse width	20		25		25		ns
t_{AP}	t_{AP}	Input [6] to Asynchronous Reset		25		25		35	ns
t_{AR}	t_{AR}	Asynchronous Reset recovery time		25		25		35	ns
t_{RESET}		Power-on reset time for registers in clear state [4]		5		5		5	µs

* Alternate source symbols are shown to compare the PEEL20CG10 specifications other pin-compatible devices.

Switching Waveforms



1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20nS.
2. Voltage applied to input or output must not exceed V_{CC} +1.0V.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
5. I/O pins open (no load).
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$; $V_{REFF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration of less than 1 sec.
11. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
12. PEEL Device test loads are specified at the end of this section.

INTERNATIONAL CMOS TECHNOLOGY, INC.

Product Preview

PEEL™20CG10-12/PEEL™20CG10-15
CMOS Programmable Electrically Erasable Logic Device

Features

- **1 Micron CMOS EEPROM Technology**
- **Low Power Consumption**
  - 105mA + 0.5mA/MHz max
- **Ultra High Performance**
  - 20CG10-12 t_{PD} = 12ns
  - 20CG10-15 t_{PD} = 15ns
- **EE Reprogrammability**
  - Low risk reprogrammable inventory
  - Superior programming and functional yield
  - Erases and programs in seconds
- **Development and Programming Support**
  - Third-party software and programmers
  - ICT PEEL Development System with APEEL™ Logic Assembler
- **Architectural Flexibility**
  - 92 product term X 44 input AND array
  - Up to 22 inputs and 10 outputs
  - Independently programmable 12-configuration I/O macrocells
  - Synchronous preset, asynchronous clear
  - Independently programmable output enables
- **Application Versatility**
  - Replaces random SSI/MSI logic
  - Emulates 24-pin bipolar PAL devices
  - Convert 24-pin PAL and EPLD designs with ICT software
  - Superset compatible with the CMOS PALC20G10

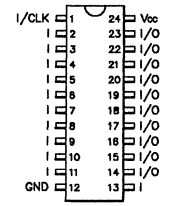
General Description

The ICT PEEL20CG10-12 or PEEL20CG10-15 is a CMOS Programmable Electrically Erasable Logic Device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL20CG10 rivals speed parameters of comparable bipolar PLDs while dramatically improving power consumption. EE reprogrammability allows for cost effective plastic packaging, low risk inventory, reduced development and retrofit costs, and enhanced testability to ensure 100% field programmability and function.

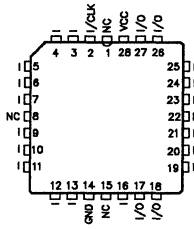
The PEEL20CG10's flexible architecture and ICT's JEDEC file translator allows the PEEL20CG10 to replace bipolar 24-pin PAL devices without the need to rework the existing design. Applications for the PEEL20CG10 include: replacement of random SSI/MSI logic circuitry; emulation of 24-pin bipolar PAL devices; and user customized sequential and combinatorial functions such as counters, shift registers, state machines, address decoders, multiplexers, etc. Development and programming support for the PEEL20CG10 is provided by ICT and third-party manufacturers.

5

Pin Configuration

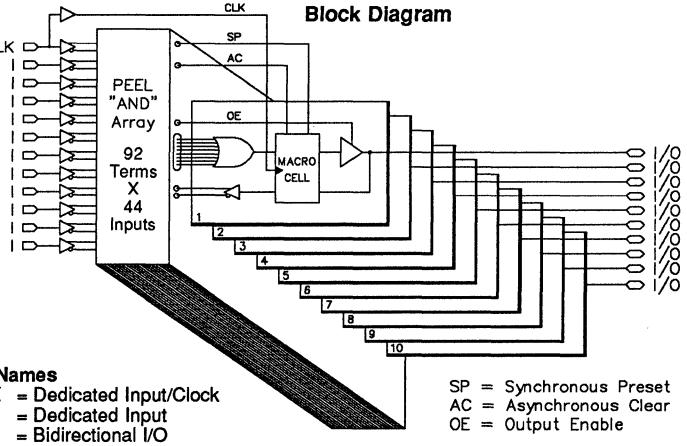


DIP



PLCC

Block Diagram



Pin Names

I/CLK	= Dedicated Input/Clock
I	= Dedicated Input
I/O	= Bidirectional I/O
GND	= Ground
Vcc	= Power Supply

SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

INTERNATIONAL CMOS
TECHNOLOGY, INC.

PEEL™22CV10
CMOS Programmable Electrically Erasable Logic Device

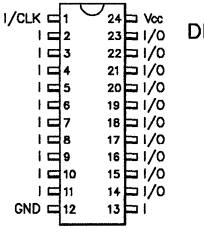
Features

- **Advanced CMOS EEPROM Technology**
- **Low Power Consumption**
  - 55mA + 0.5mA/MHz max
- **High Performance**
  - t_{PD} = 20ns, fmax=40Mhz
- **EE Reprogrammability**
  - Low-risk reprogrammable inventory
  - Superior programming and functional yield
  - Erases and programs in seconds
- **Development and Programming Support**
  - Third-party software and programmers
  - ICT PEEL Development System and software.
- **Architectural Flexibility**
  - 132 product term x 44 input AND array
  - Up to 22 inputs and 10 outputs
  - Variable product term distribution (8 to 16 per output) for greater logic flexibility
  - Independently programmable I/O macrocells
  - Synchronous preset, asynchronous clear
  - Independently programmable output enables
- **Application Versatility**
  - Replaces random SSI/MSI logic
  - Pin-compatible with the bipolar AmPAL22V10 and CMOS PALC22V10

General Description

The ICT PEEL22CV10 is a CMOS Programmable Electrically Erasable Logic Device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to early generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL22CV10 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE reprogrammability of the PEEL22CV10 allows cost effective plastic packaging, low risk inventory, reduced development and retrofit costs, and enhanced testability to ensure 100% field programmability and function. The PEEL22CV10's flexible architecture offers complete function and JEDEC-file compatibility with the bipolar AmPAL22V10 and the CMOS PALC22V10. Applications for the PEEL22CV10 include: replacement of random SSI/MSI logic circuitry and user customized sequential and combinatorial functions such as counters, shift registers, state machines, address decoders, multiplexers, etc. Development and programming support for the PEEL22CV10 is provided by ICT and third-party manufacturers.

Pin Configuration (Figure 1)



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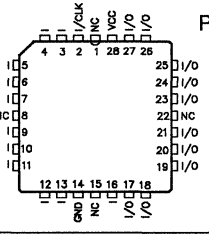
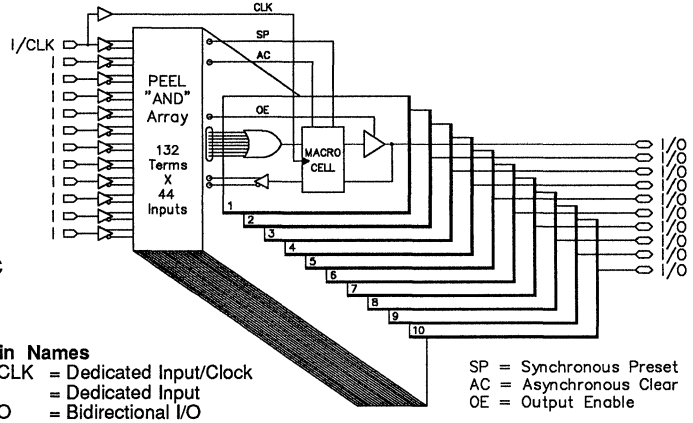


PLCC

Block Diagram (Figure 2)



Pin Names

I/CLK	= Dedicated Input/Clock
I	= Dedicated Input
I/O	= Bidirectional I/O
GND	= Ground
Vcc	= Power Supply

SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

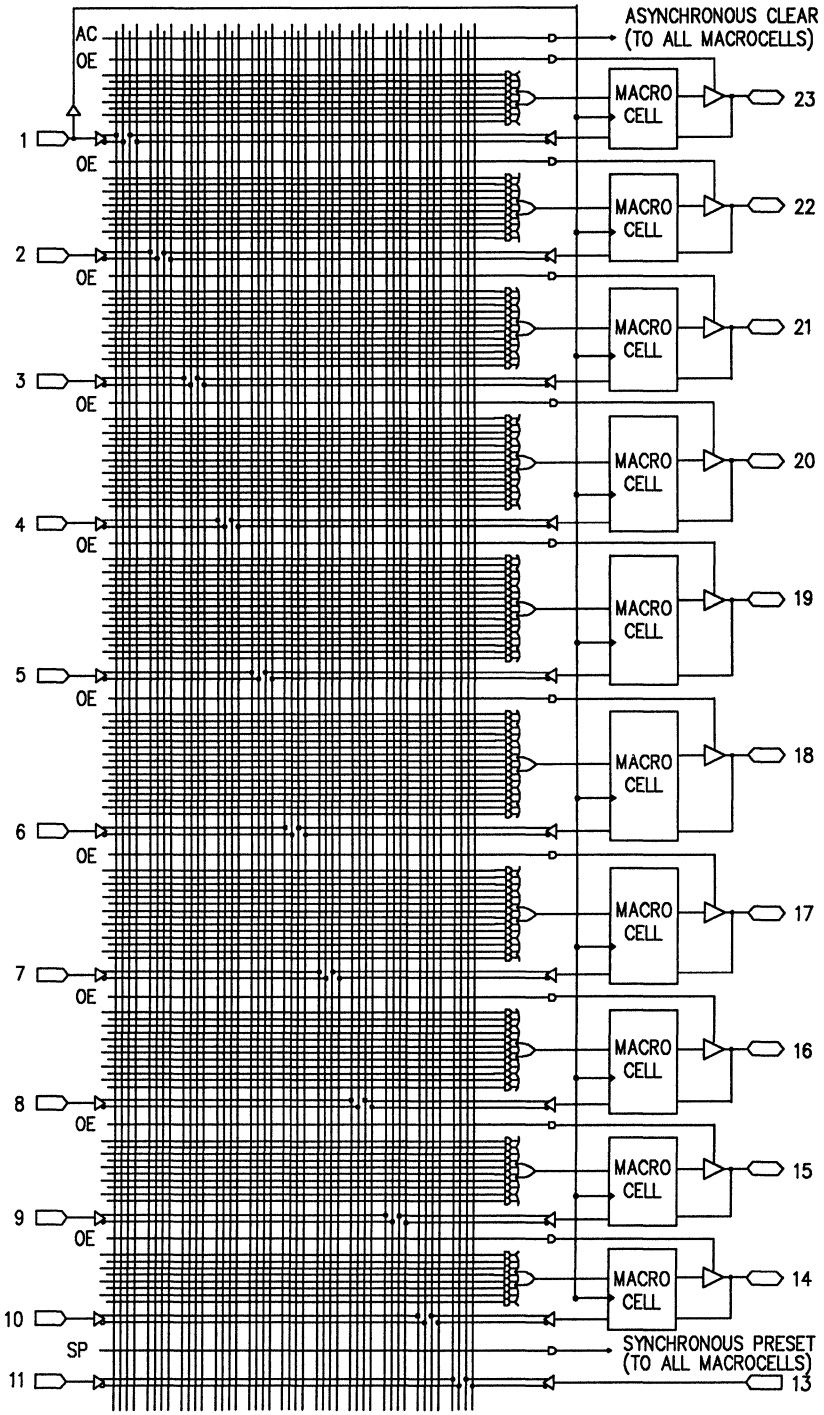


Figure 3. PEEL22CV10 Logic Array Diagram

Function Description
The PEEL22CV10 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview
The PEEL22CV10 architecture is illustrated in the block diagram of figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure, the PEEL22CV10 can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 4 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions with either active-high or active-low polarity.

AND/OR Logic Array
The programmable AND array of the PEEL22CV10 (shown in figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 24 input lines carry the true and complement of the signals applied to the 12 input pins
- 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

132 product terms:

- 120 product terms (arranged in 2 groups of 8, 10, 12,14, and 16) used to form logical sums
- 10 output enable terms (one for each I/O)
- 1 global synchronous present term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and compliment of an input signal will always be FALSE, and thus will not effect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE.

When programming the PEEL22CV10, the device programmer first performs a bulk erase to instantly remove the previous pattern. The erase cycle opens every logical connection in the array. The device is then configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program the connections on unused product terms so that they will have no effect on the output function)

Variable Product Term Distribution
The PEEL22CV10 provides 120 product terms to drive the 10 OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see figure 3). This distribution allows optimum use of device resources.

Programmable I/O Macrocell
The output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL22CV10 to the precise requirements of their designs.

Macrocell Architecture
Each I/O macrocell, as shown in figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the two EEPROM bits controlling these multiplexers (refer to table 1). These bits determine output polarity and output type (registered or non-registered). Equivalent circuits for the four macrocell configurations are illustrated in figure 5.

Output Type
The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity
Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable
The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select

When configuring an I/O macrocell to implement a registered function (configurations 1 and 2 in Figure 5), the $\overline{Q}$ output of the flip-flop drives the feedback term. When configuring and I/O mcrocell to implement a combinatorial function (configurations 3 and 4 in Figure 5), the feedback signal is taken from the I/O pin. In this case, the pin can be used as a dedicated input or a bi-directionl I/O. (Refer also to Table 1)

Additional Macro Cell Configurations
Besides the standard four-configuration macro cell shown in figure 5, each PEEL22CV10 provides an additional eight configurations that can be used to increase design flexibility. The configurations are the same provided by the PEEL18CV8, PEEL20CG10 and PEEL22CV10Z. However, to maintain JEDEC file compatibility with standard 22V10 PLDs the additional configurations can only be utilized by specifying the PEEL22CV10Z (with-out Zero Power mode) for logic assembly and programming. To reference these additional configurations please refer to the PEEL22CV10Z data sheet.

Design Security
The PEEL22CV10 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

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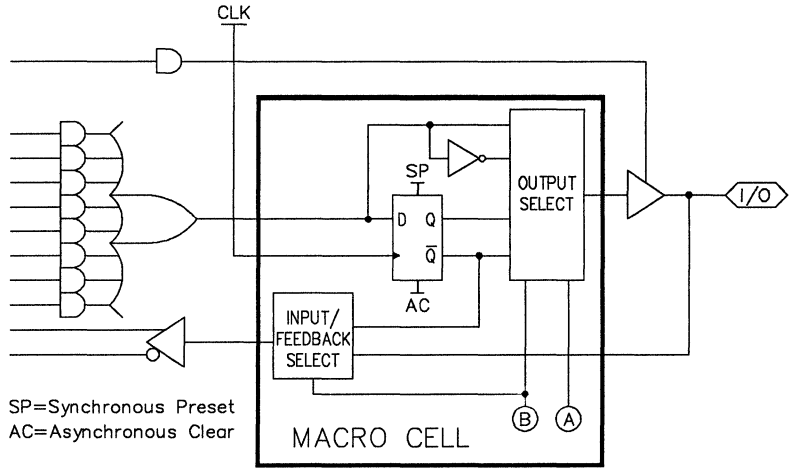

Figure 4. Block Diagram of the PEEL22CV10 I/O Macrocell

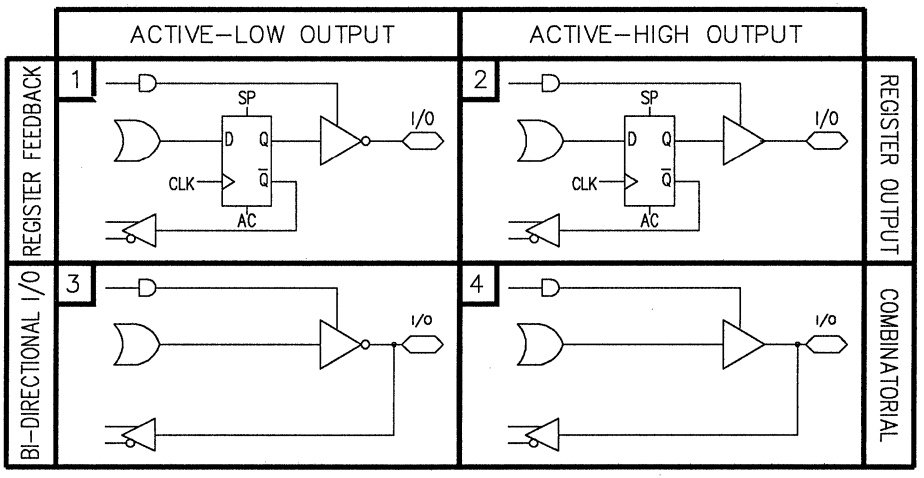

Figure 5. Equivalent Circuits for the Four Configurations of the PEEL22CV10 I/0 Macrocell.

Configuration			Input/Feedback Select	Output Select	
#	A	B			
1	0	0	Register Feedback	Register	Active Low
2	1	0			Active High
3	0	1	Bi-Directional I/O	Combinatorial	Active Low
4	1	1			Active High

Table 1. PEEL22CV10 Macrocell Configuration Bits

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 125	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Alternate Source Symbol*	Parameter	Conditions	Min	Max	Unit
V_{CC}	V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	T_A	Ambient Temperature	Commercial [2]	0	70	°C
T_R		Clock Rise Time	See note 4		250	nS
T_F		Clock Fall Time	See note 4		250	nS
T_{RVCC}		VCC Rise Time	See note 4		10	mS

D.C. Electrical Characteristics

Over the operating range

Symbol	Alternate Source Symbol*	Parameter	Conditions	Min	Max	Unit
V_{OH}	V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = −4.0mA	2.4		V
V_{OHC}		Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 8mA		0.5	V
V_{OLC}		Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IX}	I_{IL},I_{IH},I_{IX}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0.5V [10]	− 30	− 90	mA
I_{CCAC}	I_{CC}	V_{CC} Active Current CMOS	V_{IN} = Vcc or GND [5,11]		55 (*65) + 0.5mA/MHz	mA
I_{CCAT}	I_{CC}	V_{CC} Active Current, TTL	V_{IN} = V_{IL} or V_{IH} [5,11]		65 (*75) + 0.5mA/MHz	mA
C_{IN} [8]	C_{IN}	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT} [8]	C_{OUT}	Output Capacitance			12	pF

* Alternate source symbols are shown to compare the specifications of the PEEL22CV10 to other pin-compatible devices.

* 22CV10-20 only

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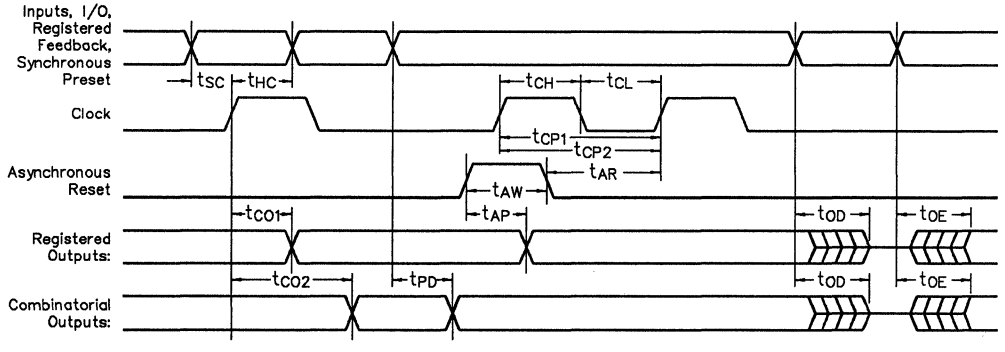
A.C. Electrical Characteristics Over the Operating Range [9,12]

Symbol	Alternate Source Symbol*	Parameter	22CV10-20		22CV10-25		22CV10-35		Unit
			Min	Max	Min	Max	Min	Max	
t_{PD}	t_{PD}	Input[6] or feedback to non-registered output		20		25		35	ns
t_{OE}	t_{EA}	Input [6] to output enable [7]		20		25		30	ns
t_{OD}	t_{ER}	Input [6] to output disable [7]		20		25		30	ns
t_{CO1}	t_{CO}	Clock to output		15		15		20	ns
t_{CO2}		Clock to combinatorial output delay via internal registered feedback		30		35		45	ns
t_{SC}	t_S	Input [6] or feedback setup to clock	12		15		30		ns
t_{HC}	t_H	Input [6] hold after clock	0		0		0		ns
t_{CL},t_{CH}	t_W	Clock width - clock low time, clock high time [4]	12		13		15		ns
t_{CP1}		Minimum clock period (register feedback to registered output via internal path)	25		27		45		ns
f_{max1}		Maximum clock frequency ($1/t_{CP1}$)	40		37		22.2		MHz
t_{CP2}	t_P	Minimum clock period ($t_{SC} + t_{CO1}$)	27		30		50		ns
f_{max2}	f_{max}	Maximum clock frequency ($1/t_{CP2}$)	37		33.3		20		MHz
t_{AW}	t_{AW}	Asynchronous Reset pulse width	20		25		25		ns
t_{AP}	t_{AP}	Input [6] to Asynchronous Reset		25		25		35	ns
t_{AR}	t_{AR}	Asynchronous Reset recovery time		25		25		35	ns
t_{RESET}		Power-on reset time for registers in clear state [4]		5		5		5	µs

* Alternate source symbols are shown to compare the PEEL22CV10 specifications to other pin-compatible devices.

Switching Waveforms



1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20nS.
2. Voltage applied to input or output must not exceed V_{CC} +1.0V.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
5. I/O pins open (no load).
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$; $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration of less than 1 sec.
11. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
12. PEEL Device test loads are specified at the end of this section.

PEEL™22CV10-12/PEEL™22CV10-15
CMOS Programmable Electrically Erasable Logic Device

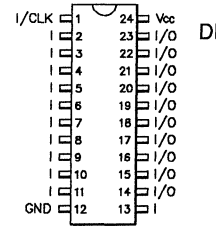
Features

- **Advanced CMOS EEPROM Technology**
- **Low Power Consumption**
  - 105mA + 0.5mA/MHz max
- **Ultra High Performance**
  - 22CV10P-12 t_{PD} = 12ns
  - 22CV10P-15 t_{PD} = 15ns
- **EE Reprogrammability**
  - Low-risk reprogrammable inventory
  - Superior programming and functional yield
  - Erases and programs in seconds
- **Development and Programming Support**
  - Third-party software and programmers
  - ICT PEEL Development System and software.
- **Architectural Flexibility**
  - 132 product term x 44 input AND array
  - Up to 22 inputs and 10 outputs
  - Variable product term distribution (8 to 16 per output) for greater logic flexibility
  - Independently programmable I/O macrocells
  - Synchronous preset, asynchronous clear
  - Independently programmable output enables
- **Application Versatility**
  - Replaces random SSI/MSI logic
  - Pin-compatible with the bipolar AmPAL22V10 and CMOS PALC22V10

General Description

The ICT PEEL22CV10P-12 or PEEL22CV10P-15 is a CMOS Programmable Electrically Erasable Logic Devices that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to early generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL22CV10 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE reprogrammability of the PEEL22CV10 allows cost effective plastic packaging, low risk inventory, reduced development and retrofit costs, and enhanced testability to ensure 100% field programmability and function. The PEEL22CV10's flexible architecture offers complete function and JEDEC-file compatibility with the bipolar AmPAL22V10 and the CMOS PALC22V10. Applications for the PEEL22CV10 include: replacement of random SSI/MSI logic circuitry and user customized sequential and combinatorial functions such as counters, shift registers, state machines, address decoders, multiplexers, etc. Development and programming support for the PEEL22CV10 is provided by ICT and third-party manufacturers.

Pin Configuration (Figure 1)



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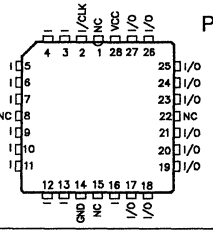
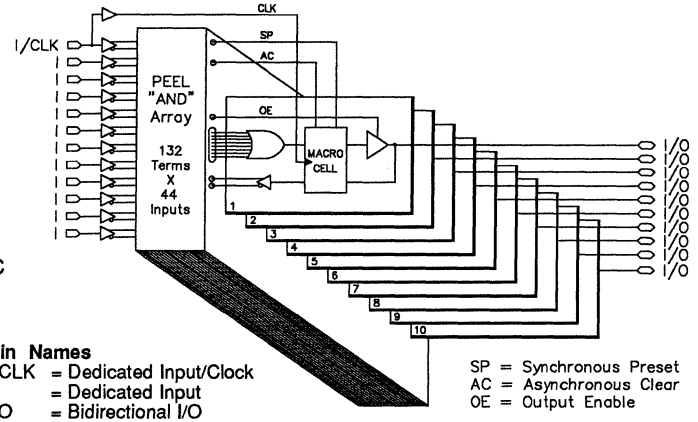


PLCC

Block Diagram (Figure 2)



Pin Names

I/CLK	= Dedicated Input/Clock
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I/O	= Bidirectional I/O
GND	= Ground
Vcc	= Power Supply

SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

INTERNATIONAL CMOS TECHNOLOGY, INC.

Preliminary

PEEL™22CV10Z "Zero Power" CMOS Programmable Electrically Erasable Logic Device

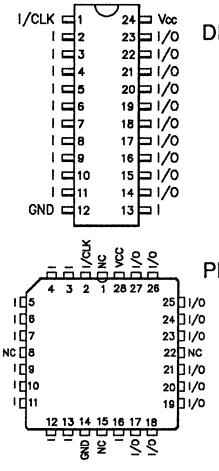
Features

- **Advanced CMOS EEPROM Technology**
- **High Performance and Ultra-Low Power**
  - — t_{PD} =20ns, fmax=40MHz
  - — I_{CC} (active) = 55mA + 0.5mA/MHz
  - — I_{CC} ("Zero-Power" standby) = 200µA
- **EE Reprogrammability**
  - — Low-risk reprogrammable inventory
  - — Superior programming and functional yield
  - — Erases and programs in seconds
- **Development and Programming Support**
  - — Third-party software and programmers
  - — ICT PEEL Development System and software.
- **Architectural Flexibility**
  - — 132 product term x 44 input AND array
  - — Up to 22 inputs and 10 outputs
  - — Variable product term distribution (8 to 16 per output) for greater logic flexibility
  - — Independently programmable 12-configuration I/O macrocells
  - — Synchronous preset, asynchronous clear
  - — Independently programmable output enables
- **Application Versatility**
  - — Ideal for power-sensitive systems
  - — Replaces random SSI/MSI logic
  - — Superset compatible with the bipolar AmPAL22V10 and CMOS PALC22V10

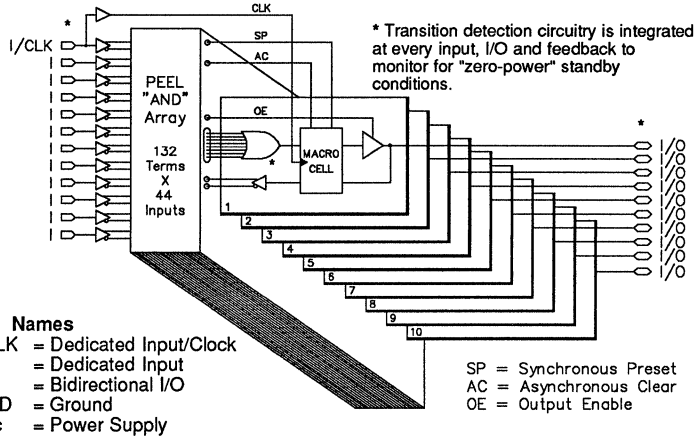
General Description

The CMOS PEEL22CV10Z is a Programmable Electrically Erasable Logic Device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to early-generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL22CV10Z rivals speed parameters of comparable bipolar PLDs while providing a dramatic reduction in active power consumption. A user-programmable "zero-power" standby mode further reduces power consumption, making the PEEL22CV10Z ideal for power sensitive applications such as hand held meters, portable communication equipment and laptop computer/peripherals. EE reprogrammability allows cost effective plastic packaging, low-risk inventories, reduced development and retrofit costs, and enhanced testability to ensure 100% field programmability and function. The PEEL 22CV10Z's flexible architecture provides function compatibility with the bipolar AmPAL22V10 and CMOS PALC22V10, plus eight additional macrocell configurations (a total of twelve) for increased design flexibility. The PEEL22CV10Z can be used to replace random SSI/MSI logic circuitry or 24-pin bipolar PAL devices, or implement user-customized sequential and combinatorial functions such as counters, shift registers, state machines, address decoders, multiplexers, etc. Development and programming support for the PEEL22CV10Z is provided by ICT and third-party manufacturers.

Pin Configuration (Figure1)



Block Diagram (Figure 2)



Pin Names

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I = Dedicated Input
I/O = Bidirectional I/O
GND = Ground
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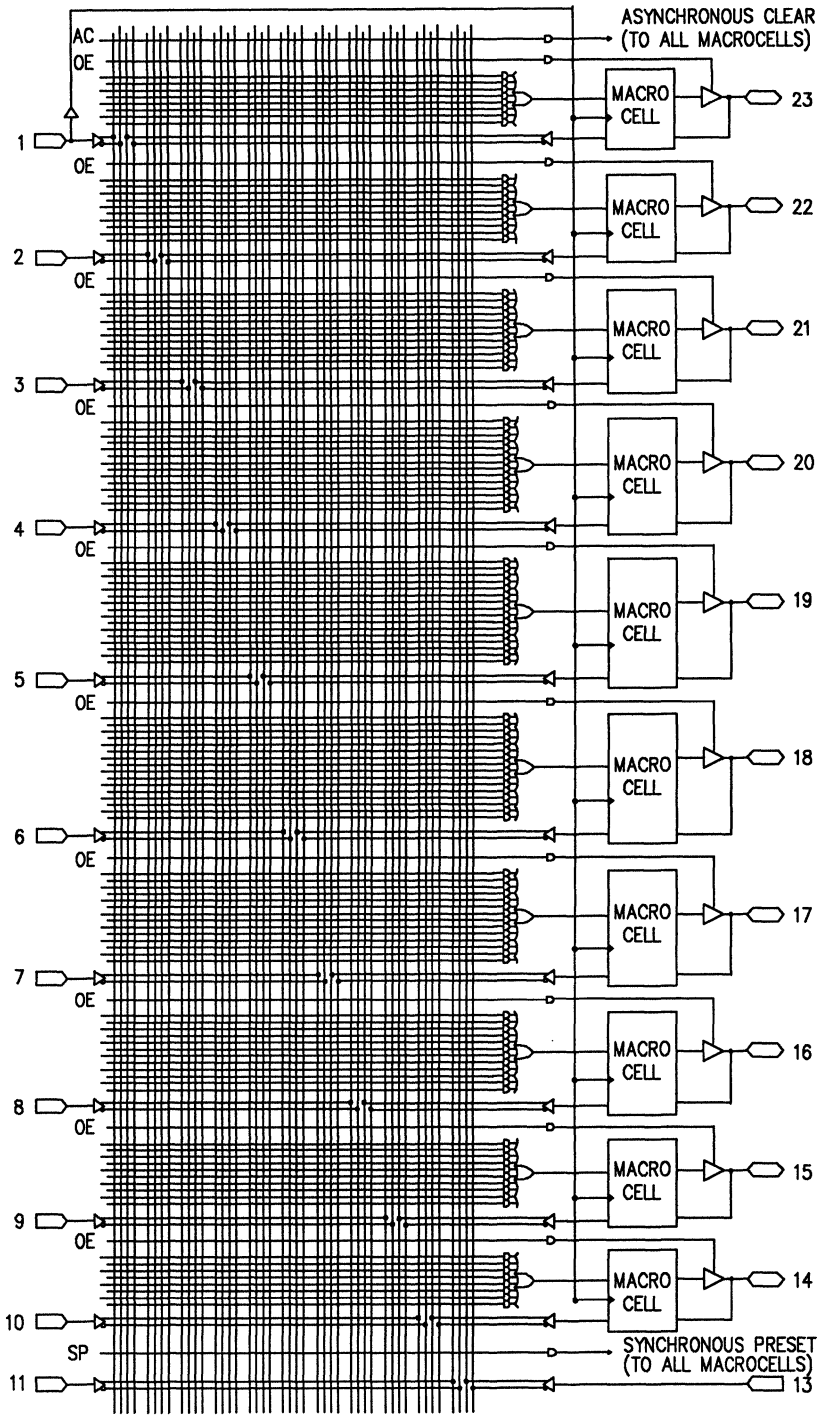

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Architecture Overview

The PEEL22CV10Z architecture is illustrated in the block diagram of figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure, the PEEL22CV10Z can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL22CV10Z (shown in figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 24 input lines carry the true and complement of the signals applied to the 12 input pins
- 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

132 product terms:

- 120 product terms (arranged in 2 groups of 8, 10, 12,14, and 16) used to form logical sums
- 10 output enable terms (one for each I/O)
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- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and compliment of an input signal will always be FALSE, and thus will not effect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE. When programming the PEEL22CV10Z, the device programmer first performs a bulk erase to instantly remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array.

Variable Product Term Distribution

The PEEL22CV10Z provides 120 product terms to drive the ten OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see figure 3). This distribution allows optimum use of device resources.

Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL22CV10Z to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the four EEPROM bits (A,B,C,D) controlling these multiplexers. These bits determine: output polarity; output type (registered or non-registered); and input/feedback path (bi-directional I/O, combinatorial feedback, or register feedback). Table 1 shows the bit settings for each of the twelve macrocell configurations.

Equivalent circuits for the twelve macrocell configurations are illustrated in figure 5. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9, and 10) the macrocell provides eight additional configurations.

Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state. Under the control of the output enable term, the I/O pin can function as a dedicated input, output, or a bi-directional I/O.

Input/Feedback Select

The PEEL22CV10Z macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell may be obtained from three different locations: from the I/O pin (bi-directional I/O); directly from the Q output of the flip-flop (registered feedback); or directly from the OR gate (combinatorial feedback).

Bi-directional I/O

The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

Combinatorial Feedback

The signal-select multiplexer gives the macrocell the ability to feedback the output directly from the OR gate, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7, and 8 in figure 5.)

Registered Feedback

Feedback also can be taken from the register, regardless of whether the output function is registered or combinatorial. When implementing configurations 11 and 12, the register can be used for internal latching of data while leaving the external output free for combinatorial functions.

"Zero-Power" Mode

The CMOS PEEL22CV10Z features a user-selectable "Zero-Power" standby mode for ultra-low power consumption. When the "Zero-Power" mode is selected, transition-detection circuitry monitors the inputs, I/O (including CLK) and feedback. If the inputs do not change for a period of time equal to approximately [t_{PD} X 2], the outputs are latched in their current state and the device automatically powers-down. When the next transition is detected at the inputs, the device will "wake up" for active operation until the inputs stop switching long enough to trigger the next power-down. When powering up, an additional delay is added to the first output transition. (See A.C. electrical characteristics, note 12, for details.)

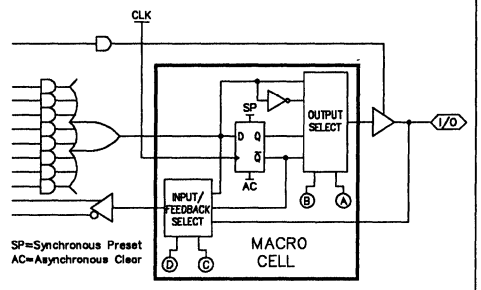


Figure 4. 22CV10Z Macro Cell Block Diagram

The "Zero-power" mode is best used for combinatorial applications since sequential functions will be powered-up with every edge of the clock. Significant power savings can still be realized, however, when running the clock at a modest rate. Figure 6 shows the typical I_{CC} vs Input transition frequency for the 22CV10Z when the zero-power mode is programmed.

The Z-bit may be set either in the design file or when programming (depending on the programmer used). For APEEL logic assembler design files, the zero-power mode is selected using the ZERO_POWER declaration. With other logic compilers, a set fuse (to "0") command for cell location 5848 can be used.

Design Security

The PEEL22CV10Z provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 24-bit code to be programmed into the PEEL22CV10Z. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

5

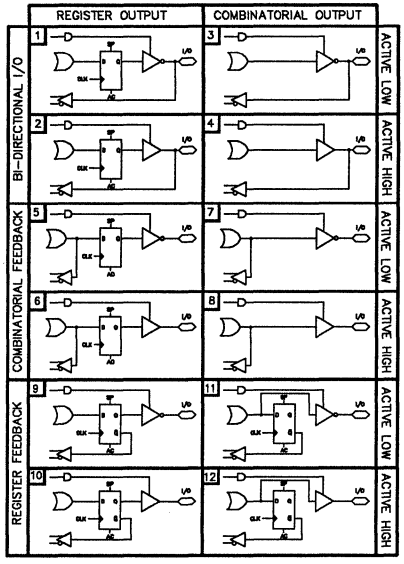


Figure 5. Equivalent Circuits for the Twelve Configurations of the PEEL22CV10Z I/0 Macrocell.

Configuration #	A	B	C	D	Input/Feedback Select	Output Select	
1	0	0	1	0	Bi-Directional I/O	Register	Active Low
2	1	0	1	0	"	"	Active High
3	0	1	0	0	"	Combinatorial	Active Low
4	1	1	0	0	"	"	Active High
5	0	0	1	1	Combinatorial Feedback	Register	Active Low
6	1	0	1	1	"	"	Active High
7	0	1	1	1	"	Combinatorial	Active Low
8	1	1	1	1	"	"	Active High
9	0	0	0	0	Register Feedback	Regisiter	Active Low
10	1	0	0	0	"	"	Active High
11	0	1	1	0	"	Combinatorial	Active Low
12	1	1	1	0	"	"	Active High

Table 1. PEEL22CV10Z Macrocell Configuration Bits

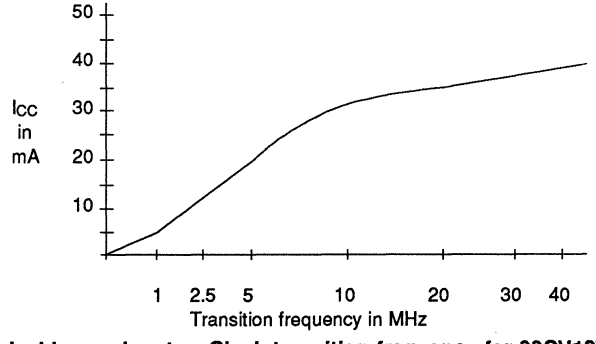


Figure 6. Typical Icc vs Input or Clock transition frequency for 22CV10Z (zero-power mode)

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 125	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Alternate Source Symbol*	Parameter	Conditions	Min	Max	Unit
V_{CC}	V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	T_A	Ambient Temperature	Commercial [2]	0	70	°C
T_R		Clock Rise Time	See note 4		250	nS
T_F		Clock Fall Time	See note 4		250	nS
T_{RVCC}		VCC Rise Time	See note 4		10	mS

D.C. Electrical Characteristics

Over the operating range

Symbol	Alternate Source Symbol*	Parameter	Conditions	Min	Max	Unit
V_{OH}	V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = −4.0mA	2.4		V
V_{OHC}		Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 8mA		0.5	V
V_{OLC}		Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IX}	I_{IL},I_{IH},I_{IX}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O≤ V_{CC}		±10	µA
I_{SC}	I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0.5V [10]	− 30	− 90	mA
I_{CCAC}	I_{CC}	V_{CC} Active Current CMOS	V_{IN} = Vcc or GND [5,11]		55 (*65) + 0.5mA/MHz	mA
I_{CCAT}	I_{CC}	V_{CC} Active Current, TTL	V_{IN} = V_{IL} or V_{IH} [5,11]		65 (*75) + 0.5mA/MHz	mA
I_{CCSZ}		V_{CC} Current, "Zero-power" standby	V_{IN} = Vcc or GND[5,11]TA=25°C		200	µA
C_{IN} [8]	C_{IN}	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT} [8]	C_{OUT}	Output Capacitance			12	pF

* Alternate source symbols are shown to compare PEEL22CV10Z specifications to other pin-compatible devices.

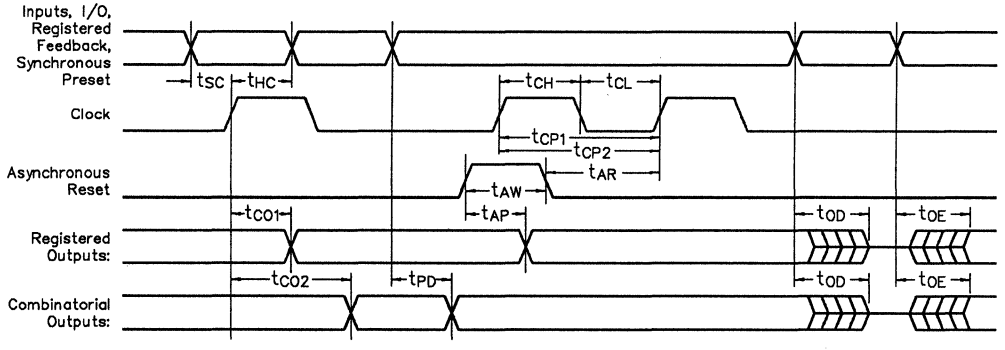
* 22CV10Z-20 only

A.C. Electrical Characteristics Over the Operating Range [9,13]

Symbol	Alternate Source Symbol*	Parameter	22CV10Z-20		22CV10Z-25		22CV10Z-35		Unit
			Min	Max	Min	Max	Min	Max	
t_{PD}	t_{PD}	Input[6] or feedback to non-registered output [12]		20		25		35	ns
t_{OE}	t_{EA}	Input [6] to output enable [7, 12]		20		25		30	ns
t_{OD}	t_{ER}	Input [6] to output disable [7, 12]		20		25		30	ns
t_{CO1}	t_{CO}	Clock to output		15		15		20	ns
t_{CO2}		Clock to combinatorial output delay via internal registered feedback		30		35		45	ns
t_{SC}	t_S	Input [6] or feedback setup to clock [12]	12		15		30		ns
t_{HC}	t_H	Input [6] hold after clock	0		0		0		ns
t_{CL},t_{CH}	t_W	Clock width - clock low time, clock high time [4]	12		13		15		ns
t_{CP1}		Minimum clock period (register feedback to registered output via internal path)	25		27		45		ns
f_{max1}		Maximum clock frequency ($1/t_{CP1}$)	40		37		22.2		MHz
t_{CP2}	t_P	Minimum clock period ($t_{SC} + t_{CO1}$) [12]	27		30		50		ns
f_{max2}	f_{max}	Maximum clock frequency ($1/t_{CP2}$)	37		33.3		20		MHz
t_{AW}	t_{AW}	Asynchronous Reset pulse width [12]	20		25		25		ns
t_{AP}	t_{AP}	Input [6] to Asynchronous Reset [12]		25		25		35	ns
t_{AR}	t_{AR}	Asynchronous Reset recovery time		25		25		35	ns
t_{RESET}		Power-on reset time for registers in clear state [4]		5		5		5	µs

* Alternate source symbols are shown to compare the specifications of the PEEL22CV10Z to other pin-compatible devices.

Switching Waveforms



1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20nS.
2. Contact ICT for other operating ranges (Industrial, Mil-temp)
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
5. I/O pins open (no load).
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OL} + 0.1V$. $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified) and specified test loads (figure 6)
10. One output at a time for a duration of less than 1 second.
11. I_{CC} for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
12. When leaving the zero-power standby state the first signal transition must add an additional delay of 10ns for these parameters.
13. PEEL test loads are specified at the end of this section.

INTERNATIONAL CMOS
TECHNOLOGY, INC.

PEEL™153
CMOS Programmable Electrically Erasable Logic Device

Features

- **ADVANCED CMOS EEPROM TECHNOLOGY**
- **LOW POWER CONSUMPTION**
  - 35mA + 1mA/MHz max
- **COMPATIBLE PERFORMANCE**
  - t_{PD} = 30ns max, t_{OE} = 30ns max
- **EE REPROGRAMMABILITY**
  - Superior programming and functional yield
  - Low cost windowless package
  - Erases and programs in seconds
- **DEVELOPMENT SUPPORT**
  - Third-party software and programmers
  - ICT PEEL Development System and software.
- **FPLA ARCHITECTURE**
  - Programmable AND/OR arrays
  - 8 inputs and 10 I/Os
  - 42 product terms: 32 logic terms, 10 control terms
  - 10 sum terms
- **DROP-IN REPLACEMENT FOR PLS153**
  - Pin compatible
  - JEDEC file compatible
- **APPLICATION VERSATILITY**
  - Replace random SSI/MSI logic
  - Create customized comparators, multiplexers,encoders, converters, etc.

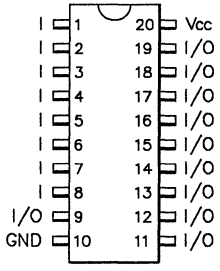
General Description

The ICT PEEL153 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional FPLAs. Designed in advanced CMOS EEPROM technology, the PEEL153 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE-reprogammability of the PEEL153 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability and function. PEEL technology allows for low cost "windowless" packaging in a ceramic or plastic 20-pin, 300-mil DIP.

The PEEL153 provides both a programmable AND array and a programmable OR array to offer drop-in compatibility with the bipolar PLS153. Applications for the PEEL153 cover a wide range of combinatorial functions, such as: replacement of random SSI/MSI logic circuitry, priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. The PEEL153 is supported by popular development tools and programmers from third-party manufacturers and by ICT's PEEL Development System and APEEL Logic Assembler.

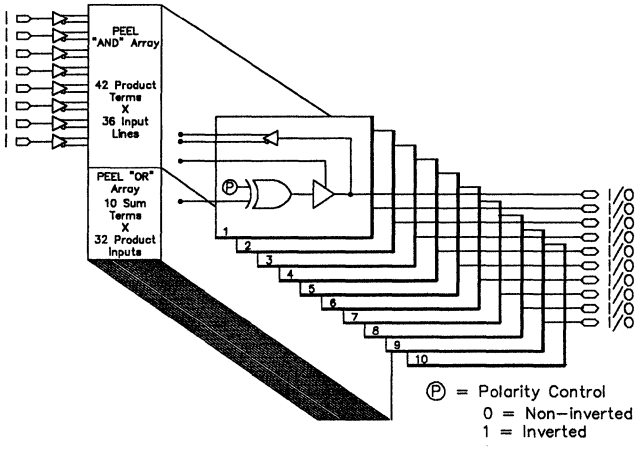
5

Pin Configuration

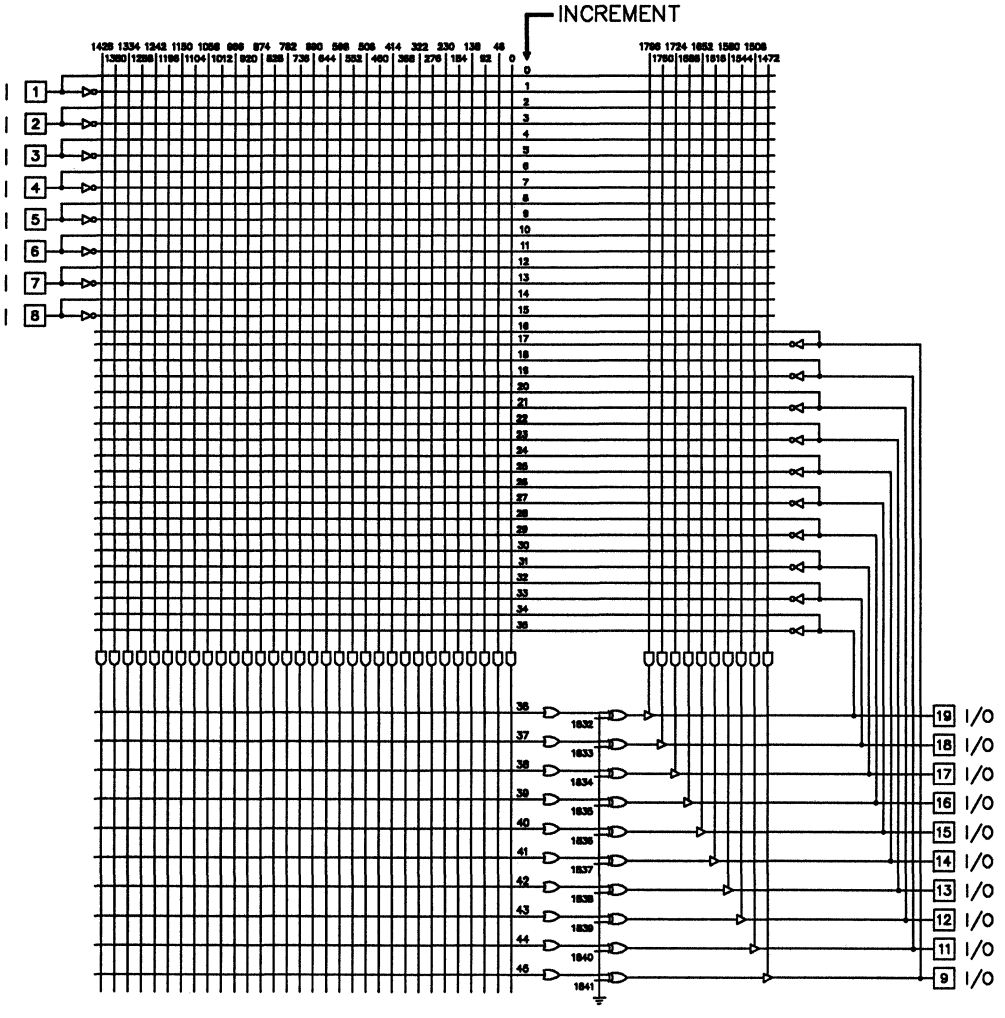


Pin Names
I = Dedicated Input
I/O = Bidirectional I/O
GND = Ground
Vcc = Power Supply (5V)

Block Diagram



JEDEC Programming Cell Number = Product Term Number + Increment



PEEL153 Logic Array Diagram

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	– 0.6 to +7.0	V
V_{IO}	Voltage Applied to Any Pin [8]	Relative to GND [1]	– 0.6 to V_{CC} + 0.6	V
T_A	Ambient Temp, Power Applied		– 10 to + 85	°C
T_{ST}	Storage Temperature		– 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Ambient Temperature	Commercial	0	70	°C

D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		– 0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = – 3.2mA	2.4		V
V_{OHC}	Output HIGH Voltage CMOS	V_{CC} = Min, I_{OH} = – 10µA	V_{CC} – 0.1		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8mA [4]		0.5	V
V_{OLC}	Output LOW Voltage CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
I_L	Input Leakage Current	V_{CC} = Max, GND ≤ V_I ≤ V_{CC}		10	µA
I_{OS}	Output Short Circuit Current [2]	V_{CC} = Max, V_O=GND	– 30	– 90	mA
I_{OZ}	Output Leakage Current	I/O = High Impedence V_{CC} = Max, GND ≤ V_O ≤ V_{CC}		± 10	µA
I_{CCSC}	Power Supply Current, Standby, CMOS Interface	All inputs = GND or V_{CC} [3]		35	mA
I_{CCAC}	Power Supply Current, Active, CMOS Interface	V_{IN} = V_{IL} or V_{IH}. All inputs, feedback, and I/Os switching [3]		I_{CCSC} + 1mA/MHz	mA
I_{CCST}	Power Supply Current Standby, TTL Interface	V_{IN} = V_{IL} or V_{IH} [3]		45	mA
I_{CCAT}	Power Supply Current, Active, TTL Interface	V_{IN} = V_{IL} or V_{IH}. All inputs, feedback, and I/Os switching [3]		I_{CCST} + 1mA/MHz	mA

Capacitance

These measurements are periodically sample tested..

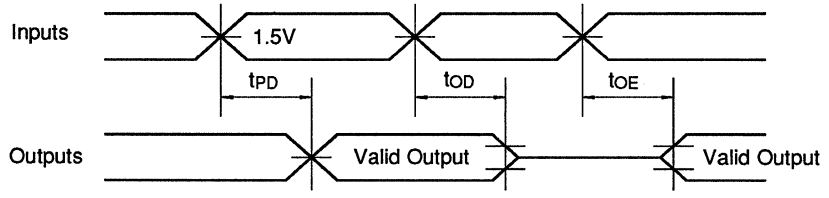
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C V_{CC} = 5.0V, f = 1kHz		6	pF
C_{OUT}	Output Capacitance			12	pF

A.C. Electrical Characteristics

Over the Operating Range [5,9]

Symbol	Parameter	PEEL153-30		PEEL153-35		PEEL153-40		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Propagation Delay, Input to Output		30		35		40	ns
t_{OE}	Input toOutput Enable [6]		30		35		40	ns
t_{OD}	Input to Output Disable [6,7]		30		35		40	ns

Switching Waveforms



Notes:

1. Minimum DC input is – 0.5V, however, inputs may undershoot to – 2.0V for periods less than 30ns.
2. Test one ouput at a time. Duration of short circuit should not exceed 1 second.
3. All I/O pins open (no load).
4. Assumes worst-case conditions - all outputs loaded. V_{OL} = 0.5V @ I_{OL} = 15mA with one output loaded.
5. Test conditions assume: signal transitions of 5ns or less fron the 10% and 90% points; timing reference levels of 1.5V (unless otherwise specified);and test loads shown.
6. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$. t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$.
7. C_L includes scope and jig capacitance. t_{OD} is measured with C_L = 5pF
8. V_{IO} specified is not for program/verify operation. Contact ICT for information regarding PEEL153 program/verify specifications
9. PEEL Deivce test leads are specified at the end of this section.

INTERNATIONAL CMOS
TECHNOLOGY, INC.

PEEL™253

CMOS Programmable Electrically Erasable Logic Device

Features

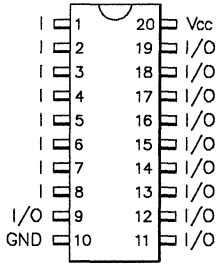
- **ADVANCED CMOS EEPROM TECHNOLOGY**
- **LOW POWER CONSUMPTION**
  - 35mA + 1mA/MHz max
- **COMPATIBLE PERFORMANCE**
  - t_{PD} = 30ns max, t_{OE} = 30ns max
- **ARCHITECTURAL FLEXIBILITY**
  - 8 inputs and 10 I/Os
  - Programmable AND/OR arrays with 42 product terms/10 sum terms
- **EE REPROGRAMMABILITY**
  - Superior programming and functional yield
  - Low cost windowless package
  - Erases and programs in seconds
- **FPLA ARCHITECTURE**
- **SUPERSET REPLACEMENT FOR PLS153**
  - Ten additional product terms
  - Output-enable terms in OR array
  - Signature word
  - Foolproof design security
- **APPLICATION VERSATILITY**
  - Replace random SSI/MSI logic
  - Create customized comparators, multiplexers,encoders, converters, etc.
- **DEVELOPMENT SUPPORT**
  - Third-party software and programmers
  - ICT PEEL Development System and software.

General Description

The ICT PEEL253 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL253 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE-reprogammability of the PEEL253 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability and function. PEEL technology allows for low cost "windowless" packaging in a ceramic or plastic 20-pin, 300-mil DIP.

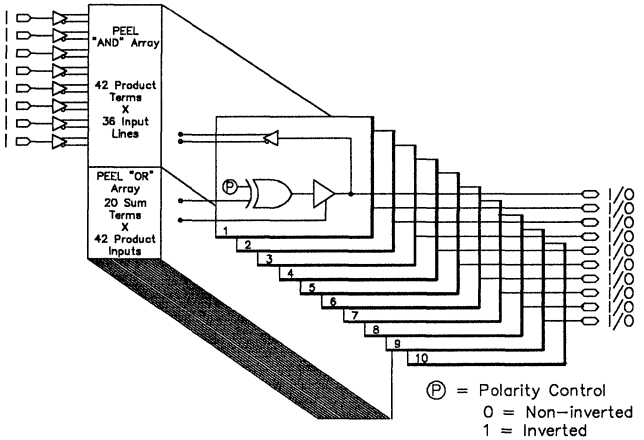
The PEEL253 provides both a programmable AND array and a programmable OR array. It offers superset compatibility with the bipolar PLS153 with several architectural enhancements, including: output enable terms in the OR array, 10 additional product terms, and signature word. Applications for the PEEL253 cover a wide range of combinatorial functions, such as: replacement of random SSI/MSI logic circuitry, priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. The PEEL253 is supported by popular development tools and programmers from third-party manufacturers and by ICT's PEEL Development System and APEEL Logic Assembler.

Pin Configuration



Pin Names
I = Dedicated Input
I/O = Bidirectional I/O
GND = Ground
Vcc = Power Supply (5V)

Block Diagram



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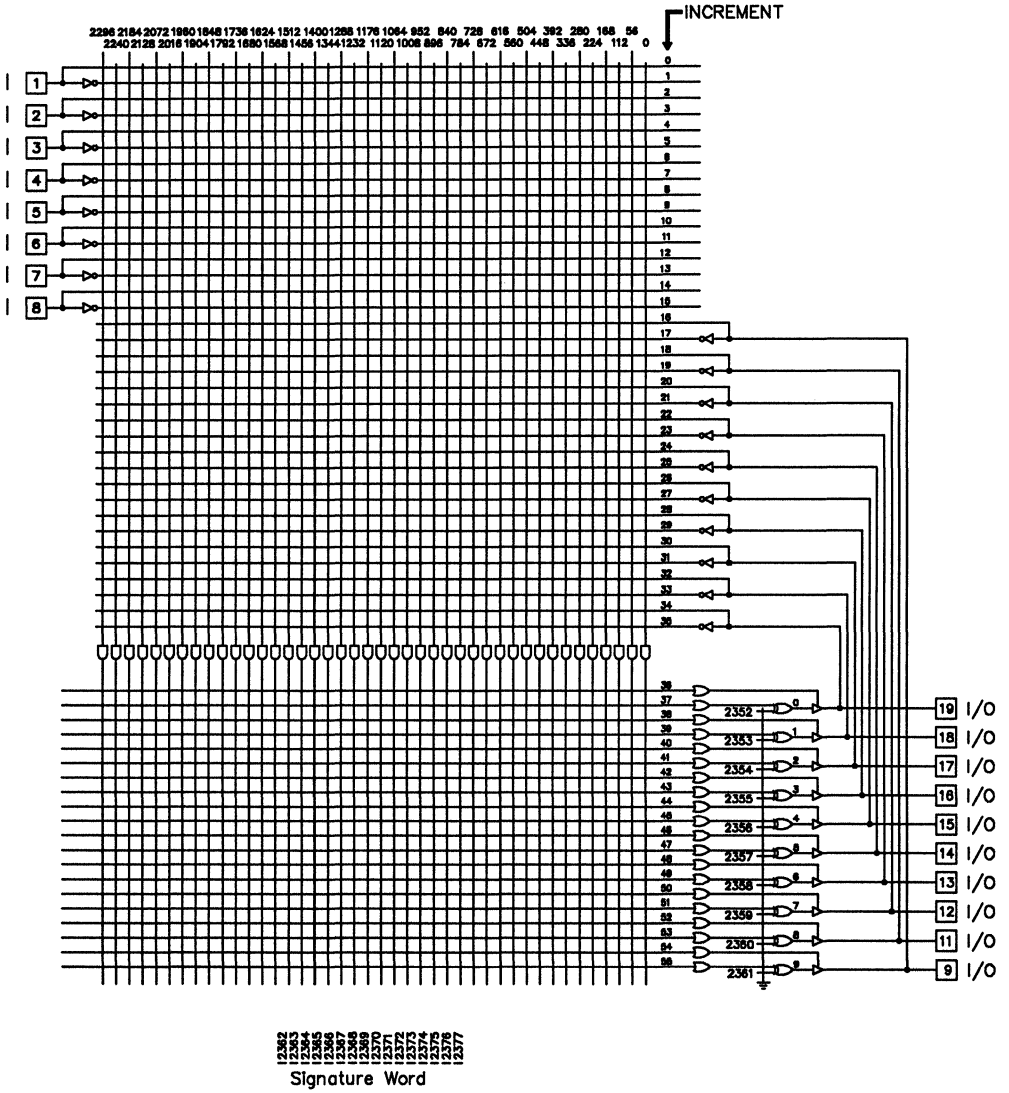
JEDEC Programming Cell Number = Product Term Number + Increment



2362 2363 2364 2365 2366 2367 2368 2369 2370 2371 2372 2373 2374 2375 2376 2377

Signature Word

PEEL253 Logic Array Diagram

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	– 0.6 to +7.0	V
V_{IO}	Voltage Applied to Any Pin [8]	Relative to GND [1]	– 0.6 to V_{CC} + 0.6	V
T_A	Ambient Temp, Power Applied		– 10 to + 85	°C
T_{ST}	Storage Temperature		– 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Ambient Temperature	Commercial	0	70	°C

D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		– 0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = – 3.2mA	2.4		V
V_{OHC}	Output HIGH Voltage CMOS	V_{CC} = Min, I_{OH} = – 10µA	V_{CC} – 0.1		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8mA [4]		0.5	V
V_{OLC}	Output LOW Voltage CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
I_L	Input Leakage Current	V_{CC} = Max, GND ≤ V_I ≤ V_{CC}		10	µA
I_{OS}	Output Short Circuit Current [2]	V_{CC} = Max, V_O=GND	– 30	– 90	mA
I_{OZ}	Output Leakage Current	I/O = High Impedence V_{CC} = Max, GND ≤ V_O ≤ V_{CC}		± 10	µA
I_{CCSC}	Power Supply Current, Standby, CMOS Interface	All inputs = GND or V_{CC} [3]		35	mA
I_{CCAC}	Power Supply Current, Active, CMOS Interface	V_{IN} = V_{IL} or V_{IH}. All inputs, feedback, and I/Os switching [3]		I_{CCSC} + 1mA/MHz	mA
I_{CCST}	Power Supply Current Standby, TTL Interface	V_{IN} = V_{IL} or V_{IH} [3]		45	mA
I_{CCAT}	Power Supply Current, Active, TTL Interface	V_{IN} = V_{IL} or V_{IH}. All inputs, feedback, and I/Os switching [3]		I_{CCST} + 1mA/MHz	mA

Capacitance

These measurements are periodically sample tested..

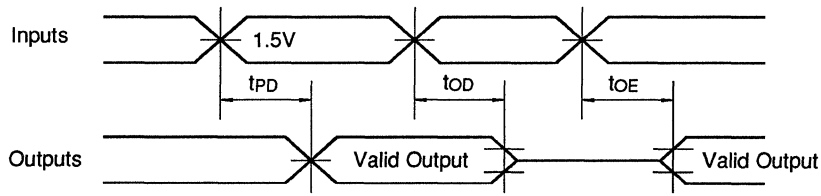
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C V_{CC} = 5.0V, f = 1kHz		6	pF
C_{OUT}	Output Capacitance			12	pF

A.C. Electrical Characteristics

Over the Operating Range [5,9]

Symbol	Parameter	PEEL253-30		PEEL253-35		PEEL253-40		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Propagation Delay, Input to Output		30		35		40	ns
t_{OE}	Input toOutput Enable [6]		30		35		40	ns
t_{OD}	Input to Output Disable [6,7]		30		35		40	ns

Switching Waveforms



Notes:

1. Minimum DC input is – 0.5V, however, inputs may undershoot to – 2.0V for periods less than 30ns.
2. Test one ouput at a time. Duration of short circuit should not exceed 1 second.
3. All I/O pins open (no load).
4. Assumes worst-case conditions - all outputs loaded. V_{OL} = 0.5V @ I_{OL} = 15mA with one output loaded.
5. Test conditions assume: signal transitions of 5ns or less fron the 10% and 90% points; timing reference levels of 1.5V (unless otherwise specified);and test loads shown.
6. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$. t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$.
7. C_L includes scope and jig capacitance. t_{OD} is measured with C_L = 5pF
8. V_{IO} specified is not for program/verify operation. Contact ICT for information regarding PEEL253 program/verify specifications
9. PEEL device test loads are specified at the end of this section..

INTERNATIONAL CMOS
TECHNOLOGY, INC.

PEEL™173
CMOS Programmable Electrically Erasable Logic Device

Features

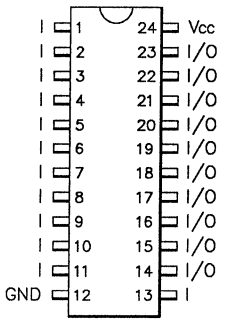
- **ADVANCED CMOS EEPROM TECHNOLOGY**
- **LOW POWER CONSUMPTION**
  - 35mA + 1.0mA/MHz max
- **COMPATIBLE PERFORMANCE**
  - t_{PD} = 30ns max, t_{OE} = 30ns max
- **EE REPROGRAMMABILITY**
  - Superior programming and functional yield
  - Low cost windowless package
  - Erases and programs in seconds
- **DEVELOPMENT SUPPORT**
  - Third-party software and programmers
  - ICT PEEL Development System and software.
- **FPLA ARCHITECTURE**
  - Programmable AND/OR arrays
  - 12 inputs and 10 I/Os
  - 42 product terms: 32 logic terms, 10 control terms
  - 10 sum terms
- **DROP-IN REPLACEMENT FOR PLS173**
  - Pin compatible
  - JEDEC file compatible
- **APPLICATION VERSATILITY**
  - Replace random SSI/MSI logic
  - Create customized comparators, multiplexers,encoders, converters, etc.

General Description

The ICT PEEL173 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional FPLAs. Designed in advanced CMOS EEPROM technology, the PEEL173 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE-reprogammability of the PEEL173 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability and function. PEEL technology allows for low cost "windowless" packaging in a ceramic or plastic 24-pin, 300-mil DIP.

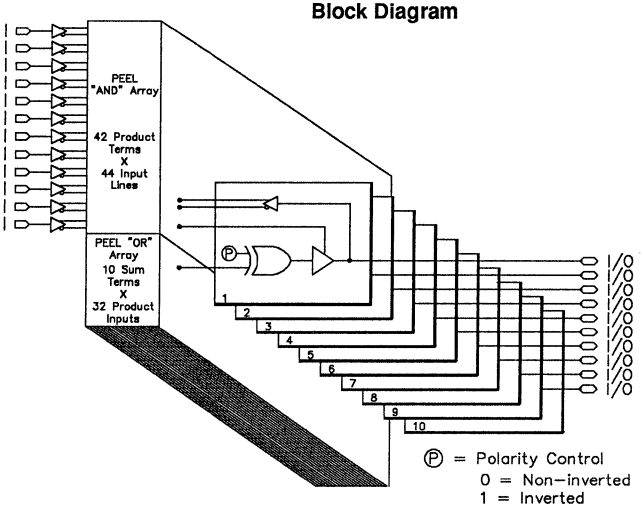
The PEEL173 provides both a programmable AND array and a programmable OR array to offer drop-in compatibility with the bipolar PLS173. Applications for the PEEL173 cover a wide range of combinatorial functions, such as: replacement of random SSI/MSI logic circuitry, priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. The PEEL173 is supported by popular development tools and programmers from third-party manufacturers and by ICT's PEEL Development System and APEEL Logic Assembler.

Pin Configuration



Pin Names
I = Dedicated Input
I/O = Bidirectional I/O
GND = Ground
Vcc = Power Supply (5V)

Block Diagram



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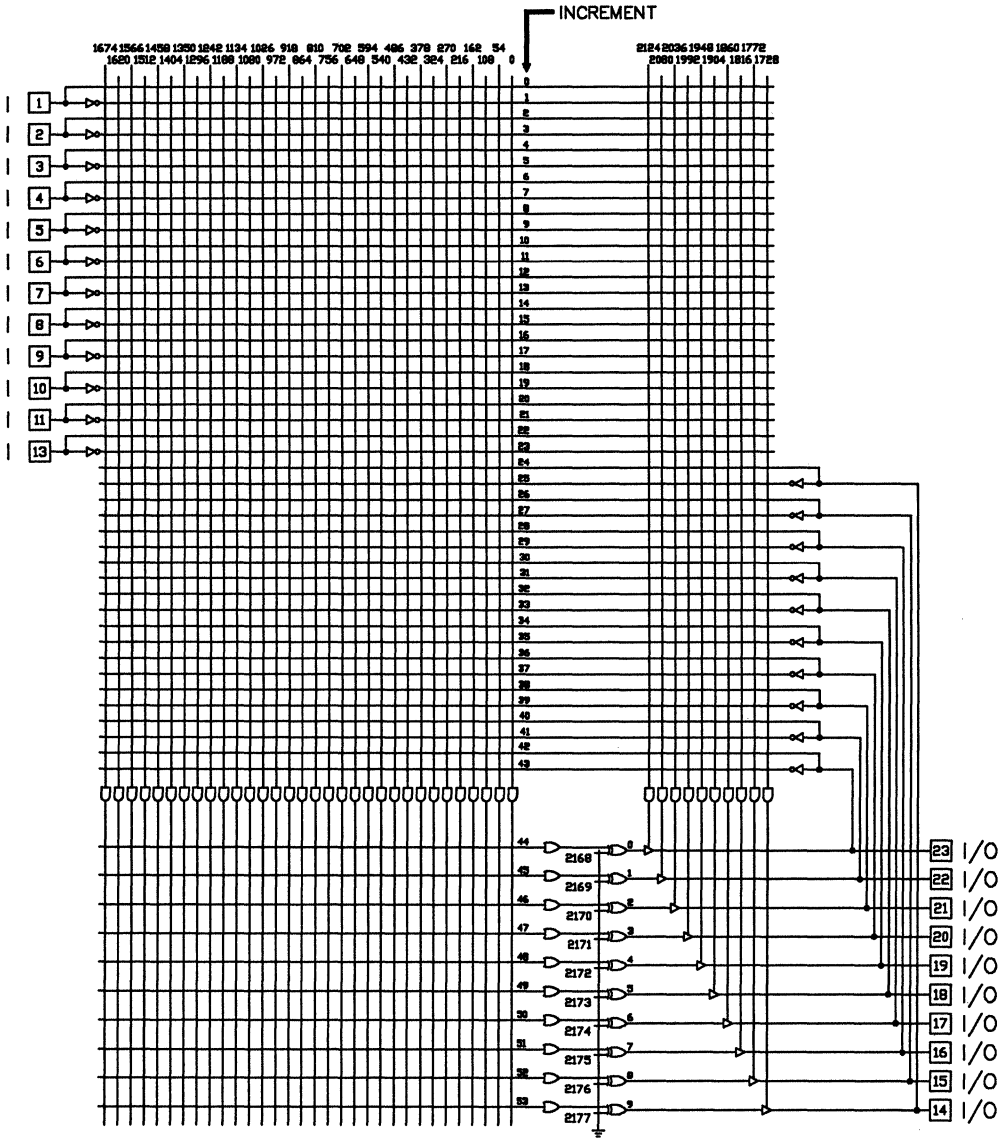
JEDEC Programming Cell Number = Product Term Number + Increment



PEEL173 Logic Array Diagram

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	– 0.6 to +7.0	V
V_{IO}	Voltage Applied to Any Pin [8]	Relative to GND [1]	– 0.6 to V_{CC} + 0.6	V
T_A	Ambient Temp, Power Applied		– 10 to + 85	°C
T_{ST}	Storage Temperature		– 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Ambient Temperature	Commercial	0	70	°C

D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		– 0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = – 3.2mA	2.4		V
V_{OHC}	Output HIGH Voltage CMOS	V_{CC} = Min, I_{OH} = – 10µA	V_{CC} – 0.1		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8mA [4]		0.5	V
V_{OLC}	Output LOW Voltage CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
I_L	Input Leakage Current	V_{CC} = Max, GND ≤ V_I ≤ V_{CC}		10	µA
I_{OS}	Output Short Circuit Current [2]	V_{CC} = Max, V_O=GND	– 30	– 90	mA
I_{OZ}	Output Leakage Current	I/O = High Impedence V_{CC} = Max, GND ≤ V_O ≤ V_{CC}		± 10	µA
I_{CCSC}	Power Supply Current, Standby, CMOS Interface	All inputs = GND or V_{CC} [3]		35	mA
I_{CCAC}	Power Supply Current, Active, CMOS Interface	V_{IN} = V_{IL} or V_{IH}. All inputs, feedback, and I/Os switching [3]		I_{CCSC} + 1mA/MHz	mA
I_{CCST}	Power Supply Current Standby, TTL Interface	V_{IN} = V_{IL} or V_{IH} [3]		45	mA
I_{CCAT}	Power Supply Current, Active, TTL Interface	V_{IN} = V_{IL} or V_{IH}. All inputs, feedback, and I/Os switching [3]		I_{CCST} + 1mA/MHz	mA

Capacitance

These measurements are periodically sample tested.

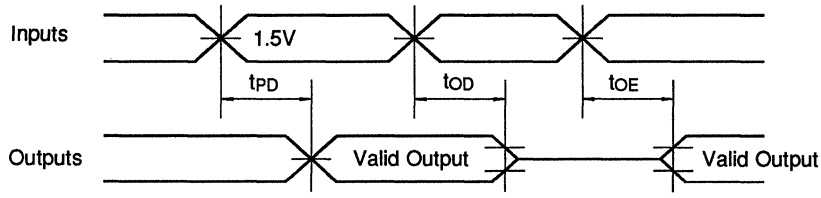
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C V_{CC} = 5.0V, f = 1kHz		6	pF
C_{OUT}	Output Capacitance			12	pF

A.C. Electrical Characteristics

Over the Operating Range [5,9]

Symbol	Parameter	PEEL173-30		PEEL173-35		PEEL173-40		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Propagation Delay, Input to Output		30		35		40	ns
t_{OE}	Input toOutput Enable [6]		30		35		40	ns
t_{OD}	Input to Output Disable [6,7]		30		35		40	ns

Switching Waveforms



Notes:

1. Minimum DC input is – 0.5V, however, inputs may undershoot to – 2.0V for periods less than 30ns.
2. Test one ouput at a time. Duration of short circuit should not exceed 1 second.
3. All I/O pins open (no load).
4. Assumes worst-case conditions - all outputs loaded. V_{OL} = 0.5V @ I_{OL} = 15mA with one output loaded.
5. Test conditions assume: signal transitions of 5ns or less fron the 10% and 90% points; timing reference levels of 1.5V (unless otherwise specified);and test loads shown.
6. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$. t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$.
7. C_L includes scope and jig capacitance. t_{OD} is measured with C_L = 5pF
8. V_{IO} specified is not for program/verify operation. Contact ICT for information regarding PEEL173 program/verify specifications
9. PEEL Device test loads are specified at the end of this section.

PEEL™173-15
CMOS Programmable Electrically Erasable Logic Device

Features

- **ADVANCED CMOS EEPROM TECHNOLOGY**
- **LOW POWER CONSUMPTION**
  - 60mA + 0.5mA/MHz max
- **HIGH PERFORMANCE**
  - t_{PD} = 15ns max, t_{OE} = 15ns max
- **EE REPROGRAMMABILITY**
  - Superior programming and functional yield
  - Low cost windowless package
  - Erases and programs in seconds
- **DEVELOPMENT SUPPORT**
  - Third-party software and programmers
  - ICT PEEL Development System and software.
- **FPLA ARCHITECTURE**
  - 12 inputs and 10 I/Os
  - Programmable AND/OR arrays
  - 42 product terms: 32 logic terms, 10 control terms
  - 10 sum terms
- **DROP-IN REPLACEMENT FOR PLS173**
  - Pin compatible
  - JEDEC file compatible
- **APPLICATION VERSATILITY**
  - Replace random SSI/MSI logic
  - Create customized comparators, multiplexers,encoders, converters, etc.

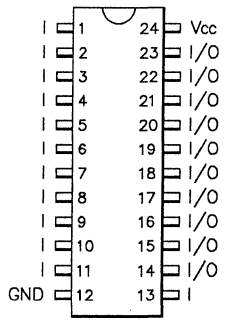
General Description

The ICT PEEL173-15 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional FPLAs. Designed in advanced CMOS EEPROM technology, the PEEL173-15 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE-reprogammability of the PEEL173-15 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability and function. PEEL technology allows for low cost "windowless" packaging in a ceramic or plastic 24-pin, 300-mil DIP.

The PEEL173-15 provides both a programmable AND array and a programmable OR array to offer drop-in compatibility with the bipolar PLS173. Applications for the PEEL173-15 cover a wide range of combinatorial functions, such as: replacement of random SSI/MSI logic circuitry, priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. The PEEL173-15 is supported by popular development tools and programmers from third-party manufacturers and by ICT's PEEL Development System and APEEL Logic Assembler.

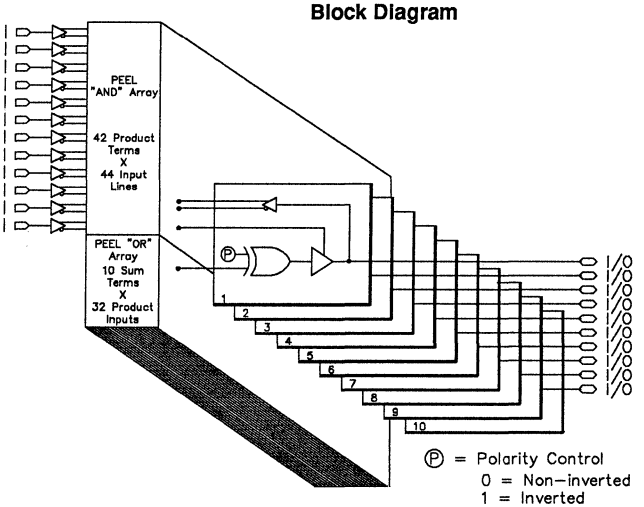
5

Pin Configuration



Pin Names
I = Dedicated Input
I/O = Bidirectional I/O
GND = Ground
Vcc = Power Supply (5V)

Block Diagram



INTERNATIONAL CMOS
TECHNOLOGY, INC.

PEEL™273

CMOS Programmable Electrically Erasable Logic Device

Features

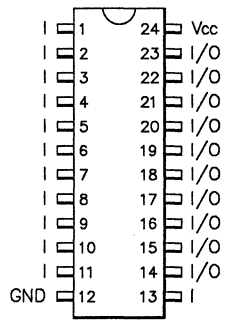
- **ADVANCED CMOS EEPROM TECHNOLOGY**
- **LOW POWER CONSUMPTION**
  - — 35mA + 1mA/MHz max
- **COMPATIBLE PERFORMANCE**
  - — t_{PD} = 30ns max, t_{OE} = 30ns max
- **ARCHITECTURAL FLEXIBILITY**
  - — 12 inputs and 10 I/Os
  - — Programmable AND/OR arrays with 42 product terms/10 sum terms
- **EE REPROGRAMMABILITY**
  - — Superior programming and functional yield
  - — Low cost windowless package
  - — Erases and programs in seconds
- **FPLA ARCHITECTURE**
- **SUPERSET REPLACEMENT FOR PLS173**
  - — Ten additional product terms
  - — Output-enable terms in OR array
  - — Signature word
  - — Foolproof design security
- **APPLICATION VERSATILITY**
  - — Replace random SSI/MSI logic
  - — Create customized comparators, multiplexers,encoders, converters, etc.
- **DEVELOPMENT SUPPORT**
  - — Third-party software and programmers
  - — ICT PEEL Development System and software.

General Description

The ICT PEEL273 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL273 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE-reprogrammability of the PEEL273 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability and function. PEEL technology allows for low cost "windowless" packaging in a ceramic or plastic 24-pin, 300-mil DIP.

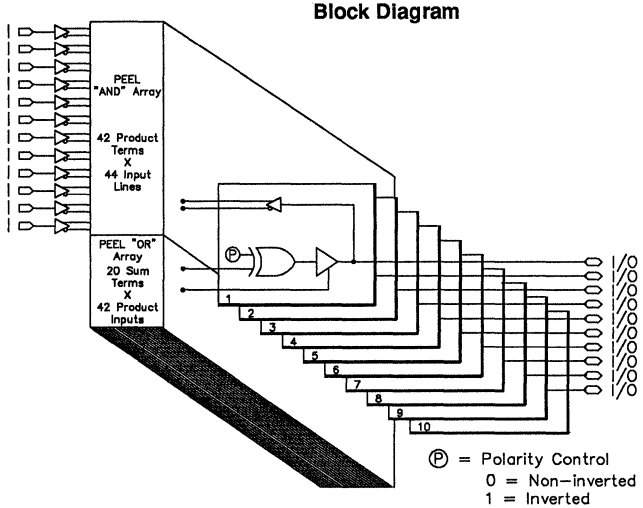
The PEEL273 provides both a programmable AND array and a programmable OR array. It offers superset compatibility with the bipolar PLS173 with several architectural enhancements, including: output enable terms in the OR array, 10 additional product terms, and signature word. Applications for the PEEL273 cover a wide range of combinatorial functions, such as: replacement of random SSI/MSI logic circuitry, priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. The PEEL273 is supported by popular development tools and programmers from third-party manufacturers and by ICT's PEEL Development System and APEEL Logic Assembler.

Pin Configuration

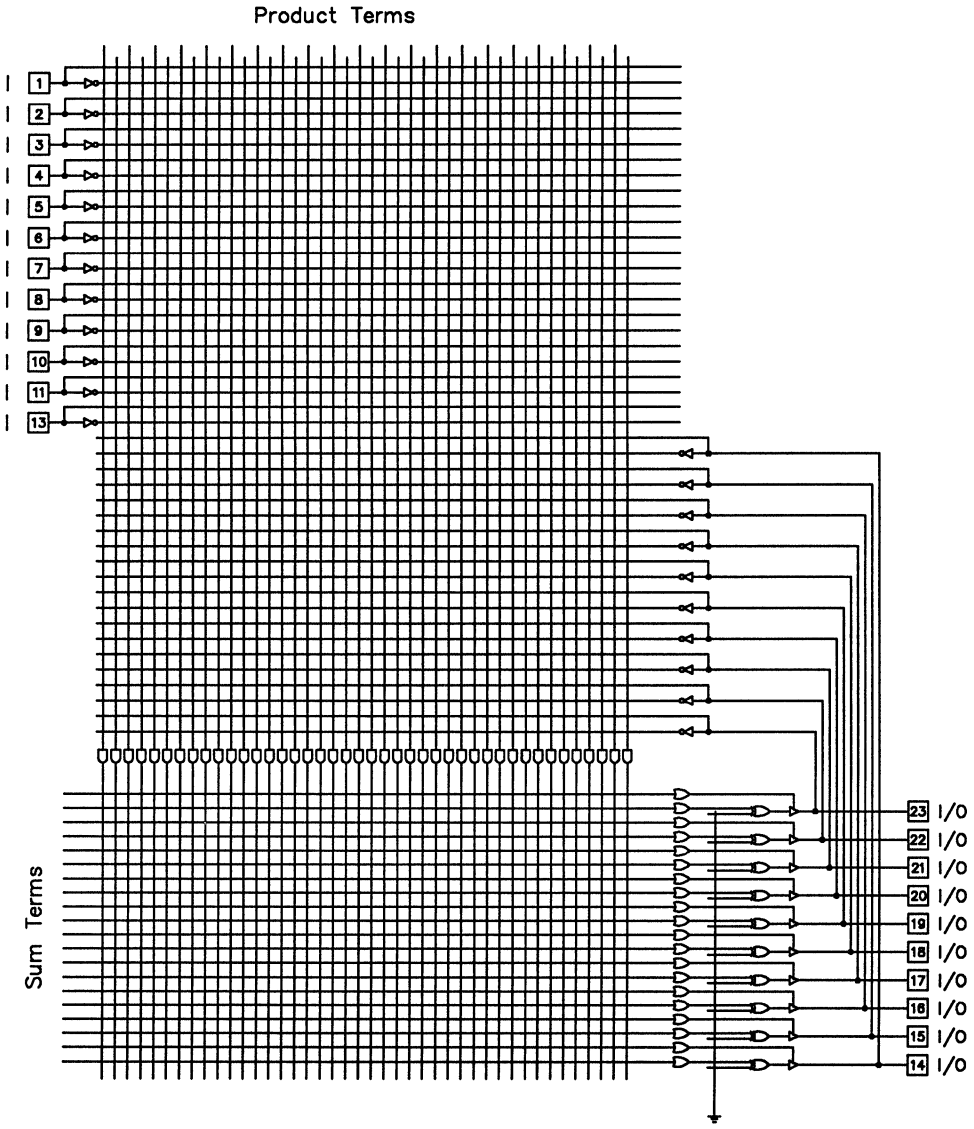


Pin Names
I = Dedicated Input
I/O = Bidirectional I/O
GND = Ground
Vcc = Power Supply (5V)

Block Diagram



Ⓟ = Polarity Control
0 = Non-inverted
1 = Inverted



PEEL273 Logic Array Diagram

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.6 to +7.0	V
V_{IO}	Voltage Applied to Any Pin [8]	Relative to GND [1]	− 0.6 to V_{CC} + 0.6	V
T_A	Ambient Temp, Power Applied		− 10 to + 85	°C
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Ambient Temperature	Commercial	0	70	°C

D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		− 0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = − 3.2mA	2.4		V
V_{OHC}	Output HIGH Voltage CMOS	V_{CC} = Min, I_{OH} = − 10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8mA [4]		0.5	V
V_{OLC}	Output LOW Voltage CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
I_L	Input Leakage Current	V_{CC} = Max, GND ≤ V_I ≤ V_{CC}		10	µA
I_{OS}	Output Short Circuit Current [2]	V_{CC} = Max, V_O=GND	− 30	− 90	mA
I_{OZ}	Output Leakage Current	I/O = High Impedence V_{CC} = Max, GND ≤ V_O ≤ V_{CC}		± 10	µA
I_{CCSC}	Power Supply Current, Standby, CMOS Interface	All inputs = GND or V_{CC} [3]		35	mA
I_{CCAC}	Power Supply Current, Active, CMOS Interface	V_{IN} = V_{IL} or V_{IH}. All inputs, feedback, and I/Os switching [3]		I_{CCSC} + 1mA/MHz	mA
I_{CCST}	Power Supply Current Standby, TTL Interface	V_{IN} = V_{IL} or V_{IH} [3]		45	mA
I_{CCAT}	Power Supply Current, Active, TTL Interface	V_{IN} = V_{IL} or V_{IH}. All inputs, feedback, and I/Os switching [3]		I_{CCST} + 1mA/MHz	mA

Capacitance

These measurements are periodically sample tested..

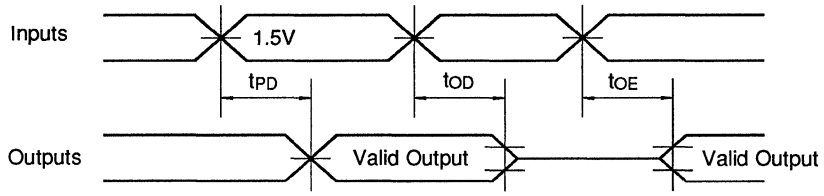
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C V_{CC} = 5.0V, f = 1kHz		6	pF
C_{OUT}	Output Capacitance			12	pF

A.C. Electrical Characteristics

Over the Operating Range [5,9]

Symbol	Parameter	PEEL273-30		PEEL273-35		PEEL273-40		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Propagation Delay, Input to Output		30		35		40	ns
t_{OE}	Input toOutput Enable [6]		30		35		40	ns
t_{OD}	Input to Output Disable [6,7]		30		35		40	ns

Switching Waveforms



Notes:

1. Minimum DC input is – 0.5V, however, inputs may undershoot to – 2.0V for periods less than 30ns.
2. Test one ouput at a time. Duration of short circuit should not exceed 1 second.
3. All I/O pins open (no load).
4. Assumes worst-case conditions - all outputs loaded. V_{OL} = 0.5V @ I_{OL} = 15mA with one output loaded.
5. Test conditions assume: signal transitions of 5ns or less fron the 10% and 90% points; timing reference levels of 1.5V (unless otherwise specified);and test loads shown.
6. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$. t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$.
7. C_L includes scope and jig capacitance. t_{OD} is measured with C_L = 5pF
8. V_{IO} specified is not for program/verify operation. Contact ICT for information regarding PEEL273 program/verify specifications
9. PEEL Device test loads are specified at the end of this section.

INTERNATIONAL CMOS TECHNOLOGY, INC.

Product Preview

PEEL™273-15

CMOS Programmable Electrically Erasable Logic Device

Features

- **ADVANCED CMOS EEPROM TECHNOLOGY**
- **LOW POWER CONSUMPTION**
  - 60mA + 0.5mA/MHz max
- **HIGH PERFORMANCE**
  - t_{PD} = 15ns max, t_{OE} = 15ns max
- **ARCHITECTURAL FLEXIBILITY**
  - 12 inputs and 10 I/Os
  - Programmable AND/OR arrays with 42 product terms/10 sum terms
- **EE REPROGRAMMABILITY**
  - Superior programming and functional yield
  - Low cost windowless package
  - Erases and programs in seconds
- **FPLA ARCHITECTURE**
- **SUPERSET REPLACEMENT FOR PLS173**
  - Ten additional product terms
  - Output-enable terms in OR array
  - Signature word
  - Foolproof design security
- **APPLICATION VERSATILITY**
  - Replace random SSI/MSI logic
  - Create customized comparators, multiplexers,encoders, converters, etc.
- **DEVELOPMENT SUPPORT**
  - Third-party software and programmers
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General Description

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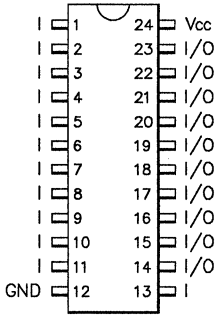
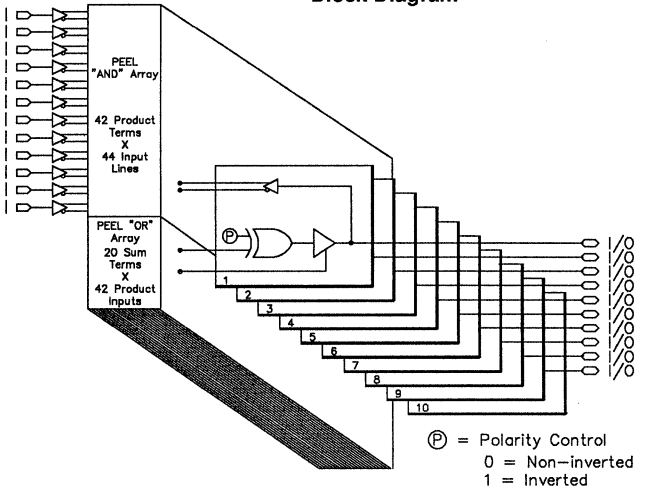
Pin Configuration

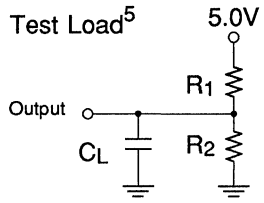


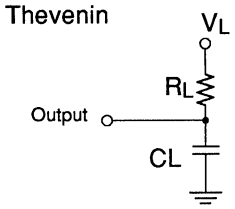
Pin Names
I = Dedicated Input
I/O = Bidirectional I/O
GND = Ground
Vcc = Power Supply (5V)

Block Diagram



PEEL Device Test Loads





Part Number	Test Loads				
	CMOS Interface		TTL Interface		
	R1	R2	R1	R2	C_L
PEEL18CV8P-25/35	480KΩ	480KΩ	464Ω	250Ω	30pF
PEEL18CV8P-15/20	480KΩ	480KΩ	319Ω	197Ω	30pF
PEEL20CG10P-20/25/35	480KΩ	480KΩ	448Ω	245Ω	30pF
PEEL22CV10P-20/25/35	480KΩ	480KΩ	448Ω	245Ω	30pF
PEEL22CV10ZP-20/25/35	480KΩ	480KΩ	448Ω	245Ω	30pF
PEEL153/PEEL253-30/35	449KΩ	433KΩ	458Ω	270Ω	30pF
PEEL173/PEEL273-30/35	449KΩ	433KΩ	458Ω	270Ω	30pF
PA7024-2/3	480KΩ	480KΩ	448Ω	245Ω	30pF
PA7040-2/3	480KΩ	480KΩ	448Ω	245Ω	30pF

Part Number	Thevenin Equivalent				
	CMOS Interface		TTL Interface		
	R_L	V_L	R_L	V_L	C1
PEEL18CV8P-25/35	228KΩ	2.375V	163Ω	1.75V	30pF
PEEL18CV8P-15/20	228KΩ	2.375V	122Ω	1.91V	30pF
PEEL20CG10P-20/25/35	228KΩ	2.375V	158Ω	1.77V	30pF
PEEL22CV10P-20/25/35	228KΩ	2.375V	158Ω	1.77V	30pF
PEEL22CV10ZP-20/25/35	228KΩ	2.375V	158Ω	1.77V	30pF
PEEL153/PEEL253-30/35	227KΩ	2.38V	169Ω	1.86V	30pF
PEEL173/PEEL273-30/35	227KΩ	2.38V	169Ω	1.86V	30pF
PA7024-2/3	228KΩ	2.375V	158Ω	1.77V	30pF
PA7040-2/3	228KΩ	2.375V	158Ω	1.77V	30pF

CMOS PEEL Arrays

6

CMOS PEEL Arrays

PEEL™ Arrays (Programmable Electrically Erasable Logic Arrays), are user-configurable high-density ICs for creating multi-level, I/O-buried, logic circuits. Designed in ICTs advanced 1-micron CMOS EE-technology, PEEL Arrays combine: the "wide-gate" speed performance of conventional PLDs (Programmable Logic Devices), the architectural flexibilty associated with FPGAs (Field Programmable Gate Arrays) and a "best of both worlds" design methodolgy.

PEEL Array Features

- **User-Configurable High Density Logic Arrays**
  - — 24/40 pin packages, (PA7024/PA7040)
  - — Multi-level, I/O buried logic
  - — 80/96 sum-of-product functions
- **High Peformance**
  - — "Wide-gate" single level delays to 17ns
  - — State machines and complex counters at 50MHz
- **Flexible Architecture**
  - — I/O and Input Cells with registers/latches
  - — Logic Control Cells with D/T/JK registers
  - — Independent clocks, presets, resets, enables
- **Logic Integration and Customization of:**
  - — PLDs, SSI/MSI functions, random logic, etc.,
- **Simplified Development Methodology**
  - — Predictable and symetrical timing, no routing
  - — PACE Software and PEEL Development System
- **CMOS EE-Technology**
  - — Non-volatile, reprogrammable, design security

INTERNATIONAL CMOS TECHNOLOGY, INC.

Preliminary Data

PA7024 PEEL™ Array
CMOS Programmable Electrically Erasable Logic Array

Features

User-Configurable High Density Logic Array
- — Create multi-level I/O-buried logic circuits
- — Over 80 sum-of-products functions
- — 20 I/Os, 2 Input/system-clocks
- — 24 pin DIP, 28 pin PLCC packaging

CMOS EE-Technology
- — Low power, ICC=100mA+0.5mA/MHz
- — Reprogrammable in plastic package
- — Low risk inventory, superior factory testing

High Performance
- — Wide-gate functions in single level delays
- — Internal: tpd= 17ns, Freq= 50MHz
- — External: tpd= 23ns, Freq= 40MHz

Flexible Architecture
- — Input registers and latches
- — I/O buried D, T and JK registers with independent clock, preset and reset
- — Separate output enables per I/O

Logic Integration and Customization of:
- — PLDs, SSI/MSI, random logic, decoders, encoders, muxs, comparators, shifters, counters, state machines, etc.

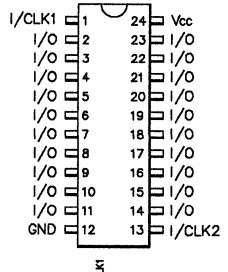
Simplified Development Methodology
- — Predictable symmetrical timing, no routing
- — Complete support with PACE™ Software and PEEL Development System from ICT

General Description

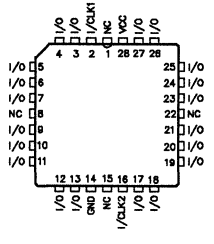
The PA7024 is a user-configurable high-density Programmable Electrically Erasable Logic (PEEL) Array for creating multi-level, I/O-buried, logic circuits. Designed in ICTs advanced 1-micron CMOS EE-technology, the PA7024 offers low power consumption, high speed performance, and reprogrammability in a plastic package allowing superior factory testing and a low risk re-usable inventory. The PA7024s wide-gate architecture can implement complex combinatorial and sequential functions with-in single-level delays of 17nS (internal) and at clock rates of 50MHz.

Its flexible architecture offers; input reg/latches per I/O, buried D, T, or JK registers with independent clock, preset and reset, and separate output enables. This versatility makes the PA7024 ideal for integrating SSI/MSI, multiple PLDs and customizing random logic, decoders, muxs, comparators, shifters, counters, state machines, etc.. Extensive signal interconnectivity makes all timing paths symmetrical, simplifying design with predictable performance and the elimination of gate-array-like routing. Complete development and programming support is provided by ICTs PACE Software and PEEL Development System.

Pin Configuration



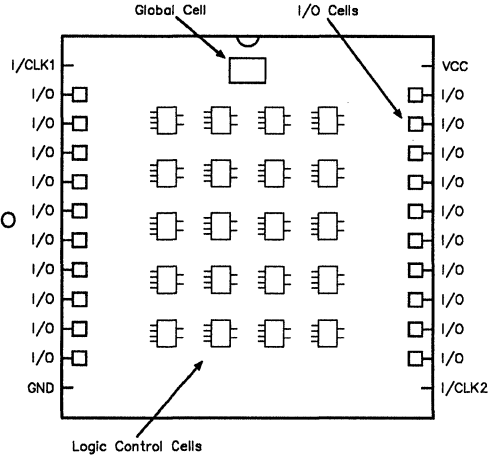
DIP

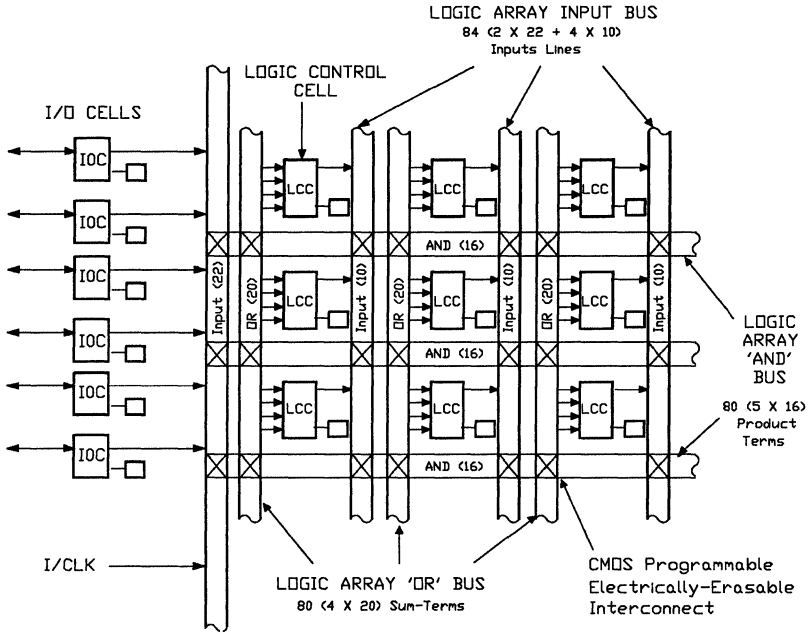


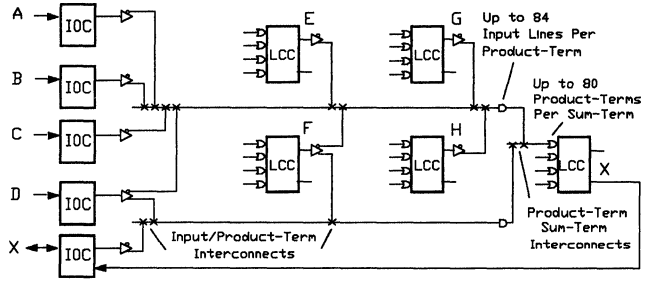
PLCC

Pin Names:
I/CLK = Input and/or System Clock
I/O = Bi-directional I/O
GND = Ground
Vcc = Power Supply

Block Diagram







$$X = (\overline{A} * B * \overline{C} * \overline{D} * E * \overline{F} * G * H) + (X * D * F)$$

Figure 3. Distributed logic array matrix (partial view) and illustration of a sum-of-products logic equation interconnected in the array

PA7024 Functional Description

The PA7024 is a user-configurable high-density CMOS Programmable Electrically Erasable Logic (PEEL) Array for creating multi-level, I/O-buried, logic circuits. As illustrated by figures 1 and 2 shown on the previous page (pin configuration and block diagram), the PA7024 has 20 I/O pins and 2 Input/System-Clock pins and is available in both 24-pin 300-mil DIP or 28-pin PLCC packages. The internal architecture of the PA7024 consists of 20 Logic Control Cells (LCCs), 20 I/O Cells (IOCs) and a Global Cell all of which are interconnected and controlled via a distributed programmable logic array matrix.

Logic Control Cell (LCC) Inputs and Outputs

Logic Control Cells (LCCs) are used to allocate and control the logic functions created in the distributed logic array matrix. Each of the twenty PA7024 LCCs have four primary inputs and two primary outputs. The inputs to each LCC are complete sum-of-product logic functions from the array matrix. The PA7024 has a total of 80 sum-of-product functions for controlling; LCC registers, IOC output enables, and combinatorial and sequential logic functions.

The two outputs of each LCC can function with complete independence from one another. This makes it possible with the PA7024 to have up to 40 independent output functions for internal and external use. (To put this in perspective, the popular 22V10 PLD architecture provides a total of 10 output logic functions.) Of the two LCC outputs, one can be connected to any I/O Cell (IOC) and associated I/O pin, the other is "buried" for use within the logic array matrix. The PA7024 allows up to 20 levels of I/O buried logic making it possible to implement , for example, a 20-bit high speed binary counter, without sacrificing any I/O pins for input or output use.

Distributed Logic Array Matrix

To better understand how sum-of-products logic functions are created and how the interconnects between LCCs and IOCs work, figure 3 illustrates the distributed logic array matrix. The logic array matrix is made up of multiple busses of input lines (Input bus), product terms (AND bus) and sum terms (OR bus). One output of each LCC can be connected to any IOC, the other is connected to the internal Input bus. The four inputs to each LCC are actually complete sum-of-product functions from the OR bus.

At the intersection of each Input/AND bus and AND/OR bus reside programmable CMOS EEPROM memory cells for controlling interconnectivity between input lines and product terms, and product terms and sum terms. When selectively programmed, complete sum-of-product logic functions can be created similar to that of a PLA structure. The end result allows each sum-term feeding into an LCC to share up to 80 product-terms and each product-term to share up to 84 input lines (the true and compliments of the 22 input pins and the 20 LCC buried outputs). This extensive sharing means product-term resources can be used where they are needed and not left un-utilized as with traditional programmable-AND fixed-OR PLDs.

Eliminating Complex Routing and Timing Issues

Because of the extensive interconectivity in the PA7024s distributed logic array structure, the complex routing and timing issues that are often associated with Field Programmable Gate Arrays (FPGAs) are eliminated. This makes it possible to predict performance and utilization results before actually implementing the design. With few exceptions, all signals route automatically, as expressed in equation form, provided that the maximum number of product terms are not exceeded. Also, all timing delays are completely symmetrical between I/O pins, IOCs or LCCs. For instance, the internal combinatorial delay from the output of any LCC, through the array, to the input of another LCC, is a maximum of one tPDI (17nS with a PA7024-2). External delay, from any I/O pin, through any LCC, to any I/O pin, is tPDX (23nS). Clock signals are also symmetrical avoiding any problems of clock skew.

Inside the Logic Control Cell (LCC)

Each PA7024 LCC includes: three signal routing and control multiplexers, a versatile register with synchronous or asynchronous D, T or JK flip-flops, and several EEPROM memory cells for programming a desired configuration. The key elements of the LCC are illustrated in the LCC block diagram, figure 4. The diagram shows how the four LCC inputs (SUM terms A, B, C and D) are distributed into the cell and how each SUM term can be selectively used for multiple functions as listed below.

Sum-A = D, T, J or Sum-A
Sum-B = Preset, K or Sum-B
Sum-C = Reset, Clock, Sum-C
Sum-D = Clock, Output Enable, Sum-D

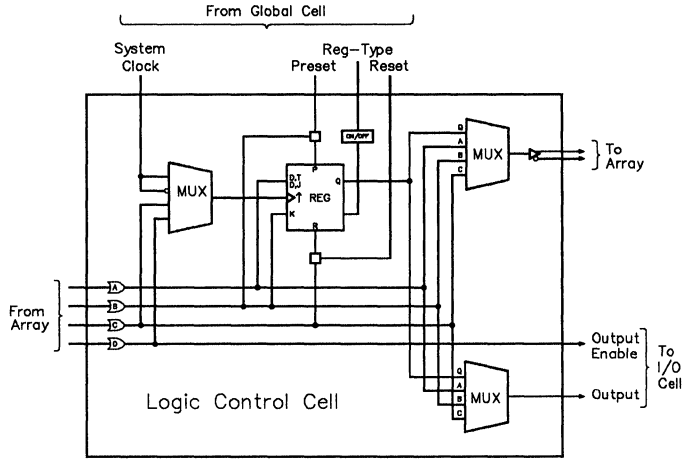


Figure 4. PA7024 Logic Control Cell (LCC)

SUM-A can serve as the D, T, or J input of the register or a combinatorial path. SUM-B can serve as the K input or the preset to the register, or a combinatorial path. SUM-C can be the clock or the reset to the register, or a combinatorial path. And, SUM-D can be the clock to the register, or the output enable for the connected I/O cell . It is important to note that unlike many PLDs, the PA7024 has complete sum-of-product (not just product term) control of clocks, resets, presets and output enables. The two primary outputs of the LCC can independently select the Q output from the register or the Sum A, B or C combinatorial paths. Thus, one LCC output can be combinatorial while the other is registered.

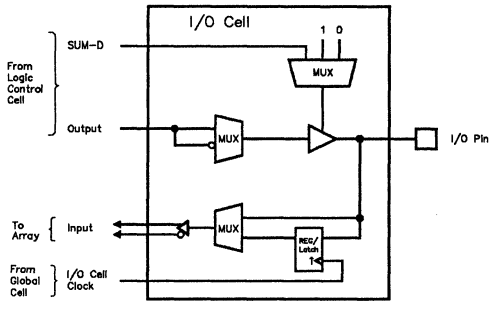


Figure 5. PA7024 I/O Cell (IOC)

Besides the SUM inputs, several inputs from the Global Cell are provided for control. The Global Cell inputs are routed to all LCCs. These signals include a high speed clock of positive or negative polarity, global preset and reset, and a special register-type control that allows dynamic switching of register selection. This last feature is useful for implementing loadable counters and state machines by dynamically switching from D to T for instance.

The I/O Cell (IOC)

The block diagram for the PA7024 I/O Cell (IOC) is shown in figure 5. The input to the IOC can be provided from any one of the LCCs in the array. Each IOC consists of routing and control multiplexers, an input register/transparent latch, a three-state buffer and an output polarity control. The reg/latch can be clocked from a variety of sources determined in the Global Cell. It can also be bypassed for a non-registered input.

The Global Cell

The PA7024s Global Cell, shown in figure 6, is used primarily to control the allocation of the system clock signals to the LCCs and the IOCs. The global cell also contains several global product and sum control terms for LCC functions such as reset, preset, register type and IOC clock. If additional partitioning of global cell clocks and control terms is needed, a second global cell can be selected that allows the

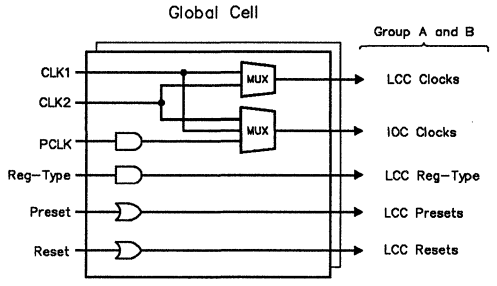


Figure 6. PA7024 Global Cell

LCCs to be divided into two groups, A and B. That is, half of the LCCs can be controlled by Global Cell A and half with Global Cell B. Global Cell A controls the LCCs connected to IOCs 2-11, and Global Cell B, the LCCs connected IOCs 14-23. This allows, for instance, two high speed clocks to be used among the LCCs in the same PA7024. Unless the second global cell is selected all LCCs and IOCs will be controlled by Global Cell A.

PA7024 Applications

The unique combination of wide gate performance and logic cell flexibility, allows the PA7024 to address a multitude of logic functions ranging from random logic to high-speed state machines. The PA7024 is ideal for implementing wide-path applications at high speeds such as fast binary counters, clock dividers, state machines, address decoders, encoders, comparators, adders and look-ahead carry. Yet, its LCC flexibility makes possible standard random logic functions such as a D flip-flops (74LS74) with independent clock reset and preset, SR latches and gated latches. Additionally, the number of registers and latches available for data storage as well as three-state I/Os, open up many possibilities for bus interfaced sub-systems.

Design Security

The PA7024 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs. Once set, the programmed bits of the PA7024 can not be accessed until the entire chip has been electrically erased.

Development Support

Development support for the PA7024 is provided by the PACE Development Software and PEEL Development System from ICT. The PACE (PEEL Architectural Compiler and Editor) software creates a software design environment that combines the attributes of logic equation and schematic entry. The mouse driven PACE editor graphically illustrates and controls the PA7024s architecture making the overall design easy to understand, while allowing the effectiveness of boolean logic equations or state machine design entry.

The PACE compiler performs logic transformation and logic reduction making it possible to specify equations in almost any fashion and to get the maximum logic into every design. PACE also provides a multi-level logic simulator that allows the external and internal signals to be fully simulated and analyzed via a waveform display. Programming is supported with direct interface to the ICT PEEL Development System programmer (PDS-1) as well with a down-load capability to Data I/O and other popular programmers. System requirements for PACE are: IBM XT/AT or compatible, 640K memory, EGA or VGA graphics and mouse.

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permenant damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 125	°C
T_{LT}	Lead Temperature	(Soldering 10 seconds)	+ 300	°C

Operating Ranges

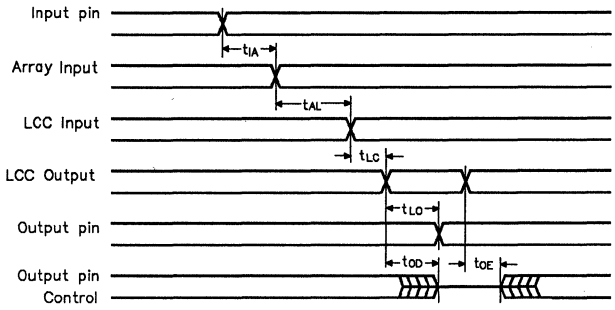
Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	+ 70	°C
T_R	Clock Rise Time	(Note 3)		250	ns
T_F	Clock Fall Time	(Note 3)		250	ns
T_{RVCC}	V_{CC} Rise Time	(Note 3)		10	ms

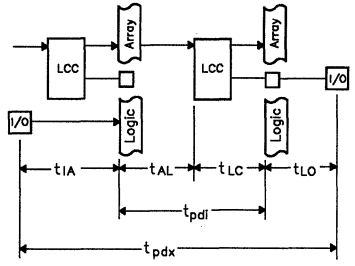
D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 8mA		0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0.5V [5]	− 30	− 100	mA
I_{CCSC}	V_{CC} Current, Standby, CMOS	V_{IN} = V_{CC} or GND [4]		100	mA
I_{CCAC}	V_{CC} Current, Active, CMOS	V_{IN} = V_{CC} or GND [4,12]		I_{CCSC} + 0.5mA/MHz	mA
I_{CCST}	V_{CC} Current, Standby, TTL	V_{IN} = V_{IL} or V_{IH} [4]		120	mA
I_{CCAT}	V_{CC} Current, Active, TTL	V_{IN} = V_{IL} or V_{IH} [4,12]		I_{CCST} + 0.5mA/MHz	mA
C_{IN}	Input Capacitance [6]	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT}	Output Capacitance [6]			12	pF

Combinatorial Timing - Waveforms and Block Diagram





A.C. Electrical Characteristics (preliminary)

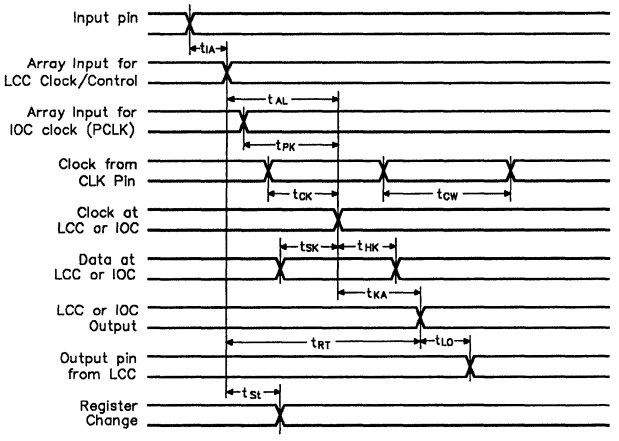
Over operating conditions

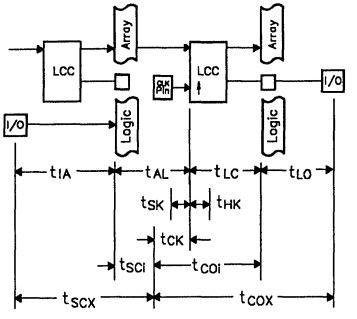
Symbol	Parameters [7]	PA7024-2		PA7024-3		Units
		Min	Max	Min	Max	
tPDI	Internal propagation delay (tAL+ tLC)		17		22	nS
tPDX	External propagation delay (tIA+ tAL+ tLC+ tLO)		23		28	nS
tIA	Input or I/O pin to input of Array		2		3	nS
tAL	Input of Array to LCC		15		21	nS
tLC	LCC input to LCC output [11]		2		2	nS
tLO	LCC output to output pin		4		5	nS
tOD	Output Disable from LCC output [8]		5		6	nS
tOE	Output Enable from LCC output [8]		5		6	nS

Notes:

1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20nS.
2. Contact ICT for other operating ranges (Industrial, Mil-Temp)
3. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
4. I/O pins open (no load).
5. Test one output at a time for a duration of less than 1 sec.
6. Capacitances are tested on a sample basis.
7. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
8. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$ (See test loads at end of section 5 for V_{REF} value). t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$..
9. "System-clock" refers to pin 1 or pin 13 high speed clocks
10. For T or JK registers in toggle (divide by 2) operation only
11. For combinatorial and register preset/reset delay
12. ICC for a typical application: This parameter is tested with the device programmed as a 20-bit Counter.

Sequential Timing - Waveforms and Block Diagram





A.C. Electrical Characteristics (preliminary)

Over operating conditions

Symbol	Parameters [7]	PA7024-2		PA7024-3		Units
		Min	Max	Min	Max	
t_{SCI}	Internal system-clock [9] set-up (t_{AL}+ t_{SK}- t_{CKmin})	12		16		nS
t_{SCX}	Ext. system-clock set-up (t_{IA}+ t_{AL}+ t_{SK}- t_{CKmin})	14		17		nS
t_{COI}	Internal system-clock to Array (t_{CKmax} + t_{LC})		8		10	nS
t_{COX}	Ext. system-clock to output (t_{CKmax} + t_{LC} + t_{LO})		12		15	nS
t_{CK}	LCC\IOC clock from system-clock pin (CLK)	5	6	7	8	nS
t_{SK}	LCC\IOC input data set-up time to clock	4		4		nS
t_{HK}	LCC\IOC input data hold time to clock	4		4		nS
f_{MAX1}	Max system-clock frequency 1/(t_{SCI} + t_{COI})		50		38.5	MHz
f_{MAX2}	Max system-clock frequency 1/(t_{SCI} + t_{COX})		41.7		32.2	MHz
f_{MAX3}	Max system-clock frequency 1/(t_{SCX} + t_{COX})		38.5		31	MHz
f_{MAX4}	Max system-clock frequency 1/(t_{CW} + t_{CW}) T/JK [10]		71.4		62.5	MHz
t_{CW}	System-clock low or high pulse width	7		8		nS
t_{RT}	Array input for Global Cell reg-type change		12		12	nS
t_{ST}	Array input for Global Cell preset/reset		17		21	nS

6

PA7040 PEEL™ Array
CMOS Programmable Electrically Erasable Logic Array

Features

User-Configurable High Density Logic Array
- — Create multi-level I/O-buried logic circuits
- — Over 120 sum-of-products functions
- — 24 I/Os, 12 inputs, 2 Input/system-clocks
- — 40 pin DIP, 44 pin PLCC packaging

CMOS EE-Technology
- — Low power, ICC=120mA+0.5mA/MHz
- — Reprogrammable in plastic package
- — Low risk inventory, superior factory testing

High Performance
- — Wide-gate functions in single level delays
- — Internal: tpd= 17ns, Freq= 50MHz
- — External: tpd= 23ns, Freq= 40MHz

Flexible Architecture
- — Input registers and latches
- — I/O buried D, T and JK registers with independent clock, preset and reset
- — Separate output enables per I/O

Logic Integration and Customization of:
- — PLDs, SSI/MSI, random logic, decoders, encoders, muxs, comparators, shifters, counters, state machines, etc.

Simplified Development Methodology
- — Predictable symmetrical timing, no routing
- — Complete design with PACE™ Software and PEEL Development System from ICT

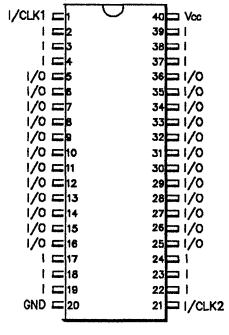
General Description

The PA7040 is a user-configurable high-density Programmable Electrically Erasable Logic (PEEL) Array for creating multi-level, I/O-buried, logic circuits. Designed in ICTs advanced 1-micron CMOS EE-technology, the PA7040 offers low power consumption, high speed performance, and reprogrammability in a plastic package allowing superior factory testing and a low risk re-usable inventory. The PA7040s wide-gate architecture can implement complex combinatorial and sequential functions with-in single-level delays as fast as 17nS (internal) and at clock rates up to 50MHz.

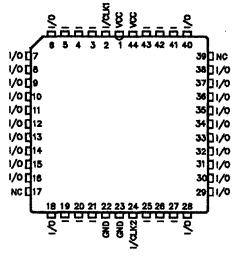
Its flexible architecture offers; input reg/latches per I/O, buried D, T, or JK registers with independent clock, preset and reset, and separate output enables. This versatility makes the PA7040 ideal for integrating SSI/MSI, multiple PLDs and customizing random logic, decoders, muxs, comparators, shifters, counters, state machines, etc.. Extensive signal interconnectivity makes all timing paths symmetrical, simplifying design with predictable performance and the elimination of gate-array-like routing. Complete development and programming support is provided by ICTs PACE Software and PEEL Development System.

Pin Configuration

DIP



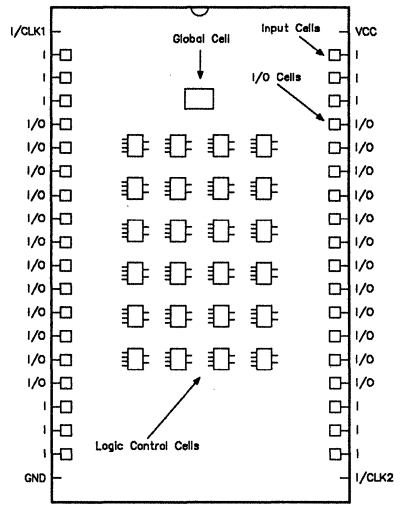
PLCC

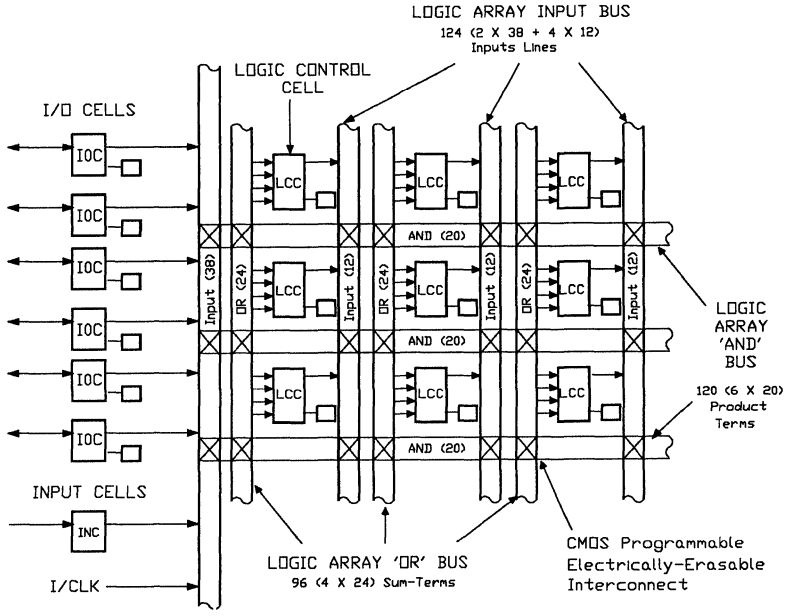


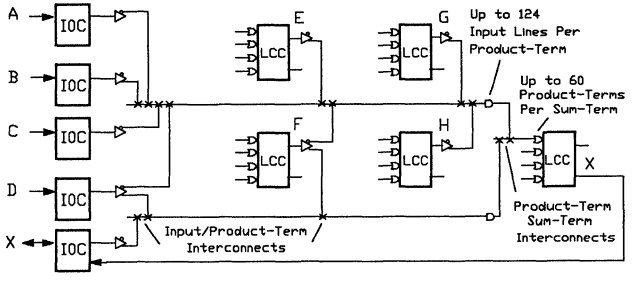
Pin Names:

I/CLK = Input and/or System Clock
I = Input
I/O = Bi-directional I/O
GND = Ground
V_{CC} = Power Supply

Block Diagram







$$X = (\overline{A} * B * \overline{C} * \overline{D} * E * \overline{F} * G * H) + (X * D * F)$$

Figure 3. PA7040 Distributed logic array matrix (partial view) and illustration of a sum-of-products logic equation interconnected in the array

PA7040 Functional Description

The PA7040 is a user-configurable high-density CMOS Programmable Electrically Erasable Logic (PEEL) Array for creating multi-level, I/O-buried, logic circuits. As illustrated by figures 1 and 2 shown on the previous page (pin configuration and block diagram), the PA7040 has 24 I/O pins, 12 Input pins and 2 Input/System-Clock pins and is available in both 40-pin 600-mil DIP or 44-pin PLCC packages. The internal architecture of the PA7040 consists of 24 Logic Control Cells (LCCs), 24 I/O Cells (IOCs), 12 Input Cells (INCs), and a Global Cell all of which are interconnected and controlled via a distributed programmable logic array matrix.

Logic Control Cell (LCC) Inputs and Outputs

Logic Control Cells (LCCs) are used to allocate and control the logic functions created in the distributed logic array matrix. Each of the twenty PA7040 LCCs have four primary inputs and two primary outputs. The inputs to each LCC are complete sum-of-product logic functions from the array matrix. The PA7040 has a total of 96 sum-of-product functions for controlling; LCC registers, IOC output enables, and combinatorial and sequential logic functions.

The two outputs of each LCC can function with complete independence from one another. This makes it possible with the PA7040 to have up to 48 independent output functions for internal and external use. (To put this in perspective, the popular 22V10 PLD architecture provides a total of 10 output logic functions.) Of the two LCC outputs, one can be connected to any I/O Cell (IOC) and associated I/O pin, the other is "buried" for use within the logic array matrix. The PA7040 allows up to 24 levels of I/O buried logic making it possible to implement, for example, a 24-bit high speed binary counter, without sacrificing any I/O pins for input or output use.

Distributed Logic Array Matrix

To better understand how sum-of-products logic functions are created and how the interconnects between LCCs and IOCs work, figure 3 illustrates the distributed logic array matrix. The logic array matrix is made up of multiple busses of input lines (Input bus), product terms (AND bus) and sum terms (OR bus). One output of each LCC can be connected to any IOC, the other is connected to the internal Input bus. The four inputs to each LCC are actually complete sum-of-product functions from the OR bus.

At the intersection of each Input/AND bus and AND/OR bus reside programmable CMOS EEPROM memory cells for controlling interconnectivity between input lines and product terms, and product terms and sum terms. When selectively programmed, complete sum-of-product logic functions can be created similar to that of a PLA structure. The end result allows each sum-term feeding into an LCC to use up to 60 product-terms with each product-term able to share up to 124 input lines (the true and compliments of the 38 input pins and the 24 LCC buried outputs). This extensive sharing means product-term resources can be used where they are needed and not left un-utilized as with traditional programmable-AND fixed-OR PLDs.

Eliminating Complex Routing and Timing Issues

Because of the extensive interconnectivity in the PA7040s distributed logic array structure, the complex routing and timing issues that are often associated with Field Programmable Gate Arrays (FPGAs) are eliminated. This makes it possible to predict performance and utilization results before actually implementing the design. With few exceptions, all signals route automatically, as expressed in equation form, provided that the maximum number of product terms are not exceeded. Also, all timing delays are completely symmetrical between I/O pins, IOCs, INCs or LCCs. For instance, the internal combinatorial delay from the output of any LCC, through the array, to the input of another LCC, is a maximum of one tPDI (17nS with a PA7040-2). External delay, from any I/O pin, through any LCC, to any I/O pin, is tPDX (23nS). Clock signals are also symmetrical avoiding any problems of clock skew.

Inside the Logic Control Cell (LCC)

Each PA7040 LCC includes: three signal routing and control multiplexers, a versatile register with synchronous or asynchronous D, T or JK flip-flops, and several EEPROM memory cells for programming a desired configuration. The key elements of the LCC are illustrated in the LCC block diagram, figure 4. The diagram shows how the four LCC inputs (SUM terms A, B, C and D) are distributed into the cell and how each SUM term can be selectively used for multiple functions as listed below.

Sum-A = D, T, J or Sum-A
Sum-B = Preset, K or Sum-B
Sum-C = Reset, Clock, Sum-C
Sum-D = Clock, Output Enable, Sum-D

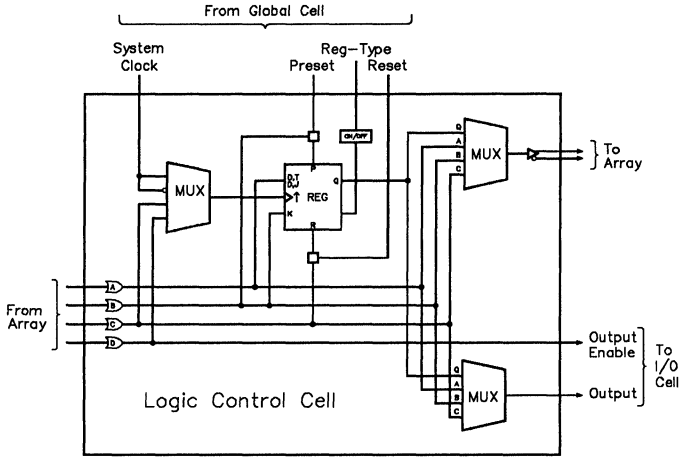


Figure 5. PA7040 I/O Cell (IOC)

SUM-A can serve as the D, T, or J input of the register or a combinatorial path. SUM-B can serve as the K input or the preset to the register, or a combinatorial path. SUM-C can be the clock or the reset to the register, or a combinatorial path. And, SUM-D can be the clock to the register, or the output enable for the connected I/O cell. It is important to note that unlike many PLDs, the PA7040 has complete sum-of-product (not just product term) control of clocks, resets, presets and output enables. The two primary outputs of the LCC can independently select the Q output from the register or the Sum A, B or C combinatorial paths. Thus, one LCC output can be combinatorial while the other is registered.

Besides the SUM inputs, several inputs from the Global Cell are provided for control. The Global Cell inputs are routed to all LCCs. These signals include a high speed clock of positive or negative polarity, global preset and reset, and a special register-type control that allows dynamic switching of register selection. This last feature is useful for implementing loadable counters and state machines by dynamically switching from D to T for instance.

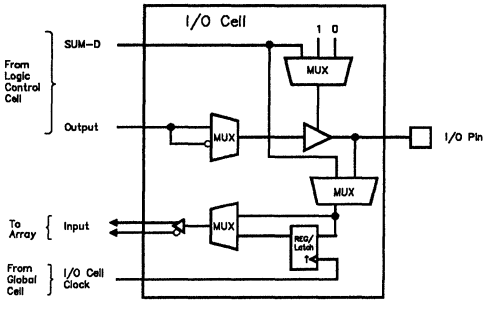


Figure 5. PA7040 I/O Cell (IOC)

The I/O Cell (IOC)

A block diagram for the PA7040 I/O Cell (IOCs) is shown in figure 5. The IOC can be connected to any one of the LCCs in the array. Each IOC consists of routing and control multiplexers, an input register/transparent latch, a three-state buffer and an output polarity control. The reg/latch can be clocked from a variety of sources determined in the Global Cell. It can also be bypassed for a non-registered input. If the IOC of the 7040 is used as a dedicated output, the register can be use as a buried register by the SUM-D term of its associated LCC.

The Input Cell (INC)

The block diagram of the PA7040 Input Cell (INC) is shown in figure 6. Unlike the IOCs, the twelve INCs can only be used as inputs into the array. Each INC consists of multiplexer and a register/transparent latch. The reg/latch can be clocked from a variety of sources determined in the Global Cell. It can also be bypassed for a non-registered input.

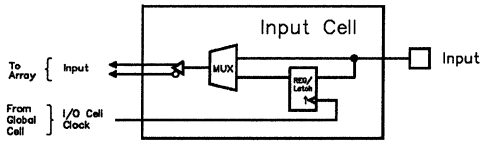


Figure 6. PA7040 Input Cell (INC)

The Global Cell

The PA7040s Global Cell, shown in figure 7, is used primarily to control the allocation of the system clock signals to the LCCs, IOCs and INCs. The global cell also contains several global product and sum control terms for LCC functions such as reset, preset, register type.

If additional partitioning of global cell clocks and control terms is needed among the LCCs, a second global cell can be selected allowing the LCCs to be divided into two groups, A and B. That is, half of the LCCs can be controlled by Global Cell A and half with Global Cell B. Global Cell A controls the LCCs connected to IOCs 5-16, and Global Cell B, the LCCs connected IOCs 25-36. This allows, for instance, two high speed clocks to be used among the LCCs in the same PA7040. Unless the Global Cell B is selected, all LCCs and associated IOCs will be controlled by Global Cell A.

Input Cell (INC) clocks are by default controlled by Global Cell A. If a different clock is needed for the INCs, a third global cell, Global Cell C, can be selected. Global Cell C allows CLK1, CLK2, or a product term to be used as the input cells register/latch clock.

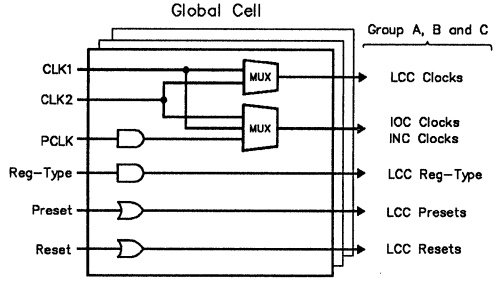


Figure 7. PA7040 Global Cell

PA7040 Applications

The unique combination of wide gate performance and logic cell flexibility, allows the PA7040 to address a multitude of logic functions ranging from random logic to high-speed state machines. The PA7040 is ideal for implementing wide-path applications at high speeds such as fast binary counters, clock dividers, state machines, address decoders, encoders, comparators, adders and look-ahead carry. Yet, its LCC flexibility makes possible standard random logic functions such as a D flip-flops (74LS74) with independent clock reset and preset, SR latches and gated latches. Additionally, the number of registers and latches available for data storage as well as three-state I/Os and additional input pins, open up many possibilities for bus interfaced sub-systems.

Design Security

The PA7040 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs. Once set, the programmed bits of the PA7040 can not be accessed until the entire chip has been electrically erased.

Development Support

Development support for the PA7040 is provided by the PACE Development Software and PEEL Development System from ICT. The PACE (PEEL Architectural Compiler and Editor) software creates a software design environment that combines the attributes of logic equation and schematic entry. The mouse driven PACE editor graphically illustrates and controls the PA7040s architecture making the overall design easy to understand, while allowing the effectiveness of boolean logic equations or state machine design entry.

The PACE compiler performs logic transformation and logic reduction making it possible to specify equations in almost any fashion and to get the maximum logic into every design. PACE also provides a multi-level logic simulator that allows the external and internal signals to be fully simulated and analyzed via a waveform display. Programming is supported with direct interface to the ICT PEEL Development System programmer (PDS-1) as well with a down-load capability to Data I/O and other popular programmers. System requirements for PACE are: IBM XT/AT or compatible, 640K memory, EGA or VGA graphics and mouse.

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permenant damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 125	°C
T_{LT}	Lead Temperature	(Soldering 10 seconds)	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	+ 70	°C
T_R	Clock Rise Time	(Note 3)		250	ns
T_F	Clock Fall Time	(Note 3)		250	ns
T_{RVCC}	V_{CC} Rise Time	(Note 3)		10	ms

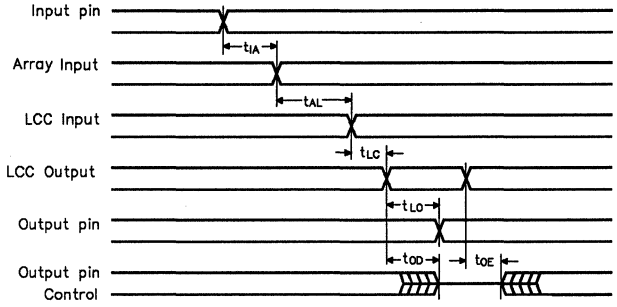
D.C. Electrical Characteristics

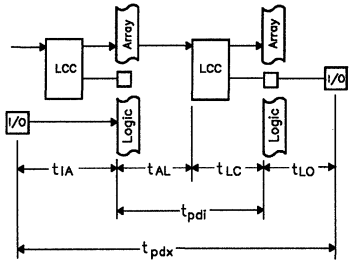
Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 8mA		0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0.5V [5]	− 30	− 100	mA
I_{CCSC}	V_{CC} Current, Standby, CMOS	V_{IN} = V_{CC} or GND [4]		120	mA
I_{CCAC}	V_{CC} Current, Active, CMOS	V_{IN} = V_{CC} or GND [4,12]		I_{CCSC} + 0.5mA/MHz	mA
I_{CCST}	V_{CC} Current, Standby, TTL	V_{IN} = V_{IL} or V_{IH} [4]		140	mA
I_{CCAT}	V_{CC} Current, Active, TTL	V_{IN} = V_{IL} or V_{IH} [4,12]		I_{CCST} + 0.5mA/MHz	mA
C_{IN}	Input Capacitance [6]	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT}	Output Capacitance [6]			12	pF

6

Combinatorial Timing - Waveforms and Block Diagram





A.C. Electrical Characteristics (preliminary)

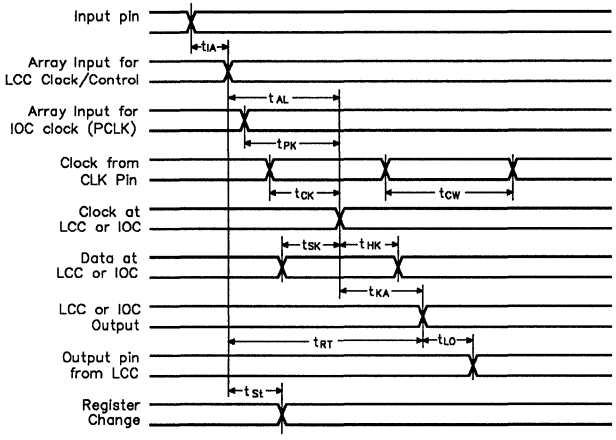
Over operating conditions

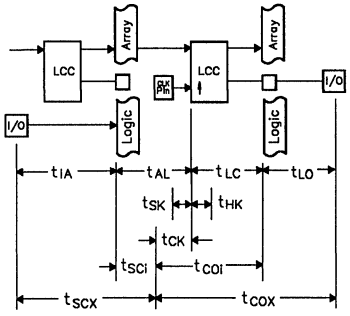
Symbol	Parameters [7]	PA7040-2		PA7040-3		Units
		Min	Max	Min	Max	
tPDI	Internal propagation delay (tAL+ tLC)		17		22	nS
tPDX	External propagation delay (tIA+ tAL+ tLC+ tLO)		23		28	nS
tIA	Input or I/O pin to input of Array		2		3	nS
tAL	Input of Array to LCC		15		21	nS
tLC	LCC input to LCC output [11]		2		2	nS
tLO	LCC output to output pin		4		5	nS
tOD	Output Disable from LCC output [8]		5		6	nS
tOE	Output Enable from LCC output [8]		5		6	nS

Notes:

1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20nS.
2. .Contact ICT for other operating ranges (Industrial, Mil-Temp)
3. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
4. I/O pins open (no load).
5. Test one output at a time for a duration of less than 1 sec.
6 Capacitances are tested on a sample basis.
7. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
8. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, (see test loads at end of section 5 for V_{REF} value). t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$..
9. "System-clock" refers to I/CLK pin high speed clocks
10. For T or JK registers in toggle (divide by 2) operation only
11. For combinatorial and register preset/reset delay
12 ICC for a typical application: This parameter is tested with the device programmed as a 24-bit Counter.

Sequencial Timing - Waveforms and Block Diagram





A.C. Electrical Characteristics (preliminary)

Over operating conditions

Symbol	Parameters [7]	PA7040-2		PA7040-3		Units
		Min	Max	Min	Max	
t_{SCI}	Internal system-clock [9] set-up (t_{AL}+ t_{SK}- t_{CKmin})	12		16		nS
t_{SCX}	Ext. system-clock set-up (t_{IA}+ t_{AL}+ t_{SK}- t_{CKmin})	14		17		nS
t_{COI}	Internal system-clock to Array (t_{CKmax} + t_{LC})		8		10	nS
t_{COX}	Ext. system-clock to output (t_{CKmax} + t_{LC} + t_{LO})		12		15	nS
t_{CK}	LCC\IOC\INC clock from system-clock pin (CLK)	5	6	7	8	nS
t_{SK}	LCC\IOC\INC input data set-up time to clock	4		4		nS
t_{HK}	LCC\IOC\INC input data hold time to clock	4		4		nS
f_{MAX1}	Max system-clock frequency (1/t_{SCI} + t_{COI})		50		40	MHz
f_{MAX2}	Max system-clock frequency (1/$_{SCI}$ + t_{COX})		45.5		37	MHz
f_{MAX3}	Max system-clock frequency (1/t_{SCX} + t_{COX})		38.5		31	MHz
f_{MAX4}	Max system-clock frequency (1/t_{CW} + t_{CW}) T/JK [10]		71.4		62.5	MHz
t_{CW}	System-clock low or high pulse width	7		8		nS
t_{RT}	Array input for Global Cell reg-type change		12		12	nS
t_{ST}	Array input for Global Cell preset/reset		17		21	nS

6

Development Tools

7

INTERNATIONAL CMOS
TECHNOLOGY, INC.

PDS-1 PEEL™ Development System

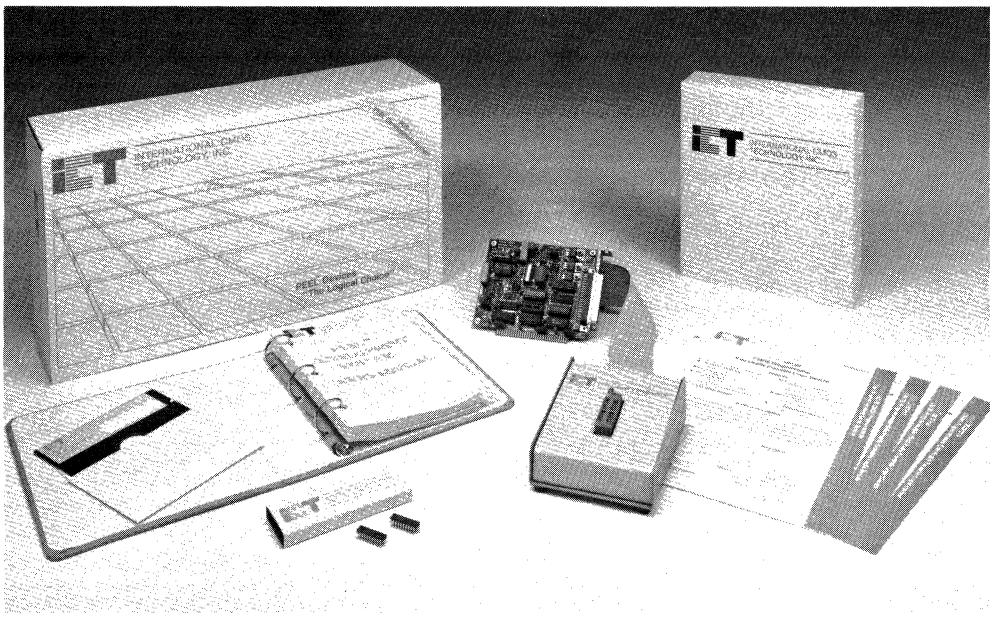
Features

- **Development System for PEEL Products**
  - — Runs on PC/XT/AT-compatible computers
  - — Comes with PEEL Development Software
  - — Interfaces to PACE Advanced Software
- **Design from Concept to Silicon**
  - — Editor, logic assembler, simulator, translator, programmer & tester in one system
- **PLD Programmer and Tester Functions**
  - — Program, Load, Verify, Secure, Test
  - — Tester allows in-socket design verification with step, loop and capture features
- **Translates Standard PLDs to PEEL Devices**
  - — Loads PLD (PAL, GAL, EPLD) or reads JEDEC file then automatically translates to PEEL device
- **Supports PEEL Devices and PEEL Arrays**
  - — PEEL 18CV8, 20CG10, 22CV10, 22CV10Z, 153, 253, 173, 273
  - — PA7024, PA7040 with PACE software
- **Also Programs ICTs Memory Products**
  - — Interfaces to ICTs memory software
  - — MPS-1 (PROMs) 27CX321/2, 27CX641/2
  - — MPS-2 (EEPROMs) 93C46/56/66

General Description

The PEEL™ Development System (PDS-1) is a powerful, yet inexpensive, PC-based system for designing with PEEL (Programmable Electrically Erasable Logic) products. Equiped with the PEEL Device Development Software, the PDS-1 provides everything needed to implement logic designs from concept to silicon, including a file editor, logic assembler, simulator, translator, programmer and tester. As a programmer the PDS-1 supports all standard operations such as program, load, verify, and secure. Special test capabilities allow for in-socket design verification to JEDEC file test vectors.

The PDS-1 translator allows for the loading of PLD designs (PAL, GAL or EPLD) from the socket for automatic translation and programming into the selected PEEL device. PEEL products supported include the PEEL 18CV8, 20CG10, 22CV10, 22CV10Z, 153, 253, 173, 273, and PEEL Arrays PA7024 and PA7040 when used with the PACE Advanced Development Software. The system can also program ICT memory products when used with the MPS-1 (PROMs) or MPS-2 (EEPROM) software. ICT socket adapters are available for PLCC and 600mil packages.



PDS-1 PEEL Development System

INTERNATIONAL CMOS
TECHNOLOGY, INC.

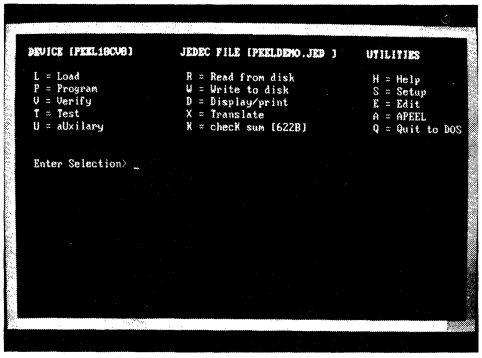
PEEL™ Device Development Software

Features

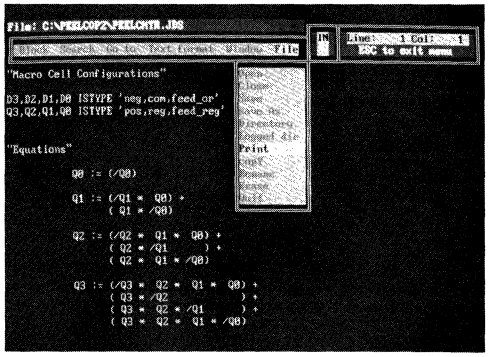
- **Development Software for PEEL Devices**
  - — Editor, logic assembler, logic simulator and PLD-to-PEEL translator
  - — Runs on PC/XT/AT-compatible computers
- **File Editor**
  - — Edit APEEL source and JEDEC files
  - — Interactive with APEEL assembler
- **APEEL™ Logic Assembler and Simulator**
  - — Supports all features of PEEL devices
  - — Assembles equations, pin/macro cell definitions and test vectors tables
  - — Creates JEDEC file for programming
- **Translates Ordinary PLDs to PEEL Devices**
  - — Automatically translates PLDs (PAL, GAL, EPLD) JEDEC files to PEEL files
- **Programmer Interface**
  - — Direct interface to PDS-1 Programmer
  - — Upload/Download of JEDEC file to other popular programmers via serial communications port
- **Documentation and Operation Support**
  - — Software and Applications Handbook
  - — Twelve application examples (on disk)
  - — On-line help instructions

General Description

The PEEL™ Development Software is a PC-based package for designing with PEEL (Programmable Electrically Erasable Logic) devices. The software provides everything needed to implement your logic designs from concept to JEDEC file creation. The software includes: a file editor, logic assembler/simulator, and a PLD-to-PEEL device translator. The built-in file editor allows for convenient design entry of APEEL source files. Additionally, the editor interacts with the assembler for quick pin-pointing of syntax errors. The APEEL logic assembler and simulator convert PEEL device designs into JEDEC programmer files which can be simulated aqainst user specified test vectors. The PEEL development software also provides a PLD-to-PEEL file translator that can automatically take PAL, GAL and EPLD files and translate them to PEEL files. Files created by design or translation can be then be used for programming with ICTs PDS-1 progammer or other popular programmers via a serial com-port down-load feature. A comprehensive handbook fully documents software operation as well as providing an applications section with twelve application examples, all of which are supplied on disk. The PEEL Device Development Software is free to qualified PLD users.



The PEEL™ Development Software provides an editor, logic assembler/simulator, a PLD to PEEL file translator and many other features.



The file editor with pop-down command windows allows for convenient and interactive design entry of APEEL design files.

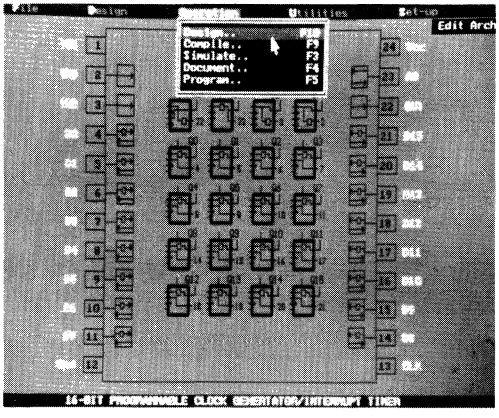
PACE™ Advanced Development Software for PEEL Arrays and PEEL Devices

Features

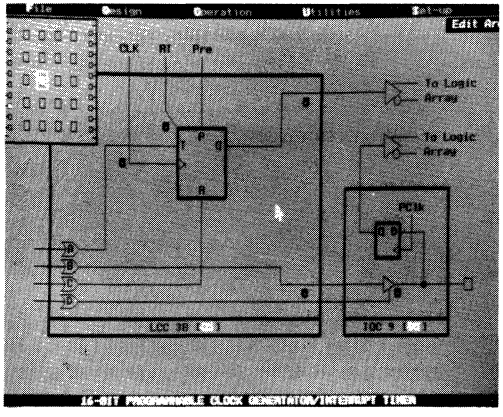
- **PEEL Archtectural Compiler and Editor**
  - — Advanced development support for PEEL Arrays and PEEL Devices
  - — Runs on IBM XT/AT or compatible system
  - — Fast and efficient design environment
- **Architectural Editing**
  - — Mouse driven, windows environment
  - — Graphic display and control of architecture
  - — Equation and state machine entry
- **Logic Compilation**
  - — Auto-transformation to sum-of-products
  - — Five levels of logic reduction
- **Multi-level Logic Simulation**
  - — Simulates all internal and external signals
  - — Interactive waveform editor and display
- **Design Documentation**
  - — Batch printing of architecture, equations and simulation waveforms
- **Programmer Interface**
  - — Direct interface to PDS-1 programmer: (program, verify, load, secure and test)
  - — Up/Download to other popular programers via serial communication port

General Description

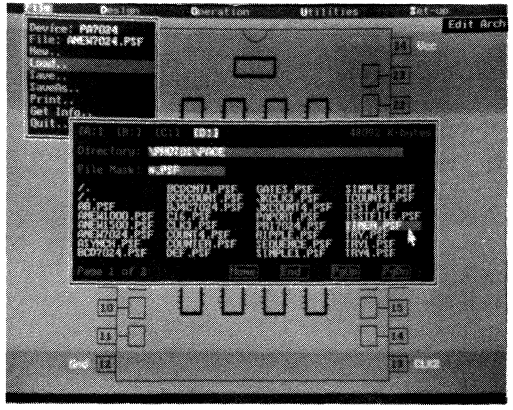
PACE is an advanced development software package offering complete support for ICTs family of PEEL (Programmable Electrically Erasable Logic) Arrays and Devices. PACEs innovative architectural editor graphically illustrates and allows control of the architecture, logic equations, and state machine entry, making the overall design easy to understand. The PACE compiler performs logic transformation, thus equations can be specified in most any fashion. The compiler also features five levels of user-selectable logic reduction, including auto-demorganization, making it possible to get more logic into every design. PACE also provides a multi-level logic simulator that lets the external and internal signals be fully simulated, analyzed and edited via a special waveform display. Documentation of PACE designs is accomplished though batch printing of equations, architecture and waveform displays. Programming is supported by a direct interface to the ICT PEEL Development System programmer and by other popular programmers via a down-load feature that uses the serial communication port. System requirements for PACE are: IBM XT/AT or compatible system with DOS version 3.0 or greater, 512K memory, EGA or VGA graphics and mouse. PACE also supports expanded memory on systems with EMS drivers conforming to the 3.2 or greater LIM EMS specification.



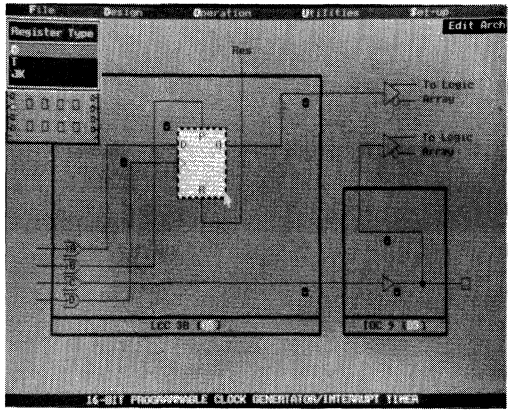
The PACE architectural editors "chip display" provides a global view of design allowing quick access to I/Os, registers, cells and equations.



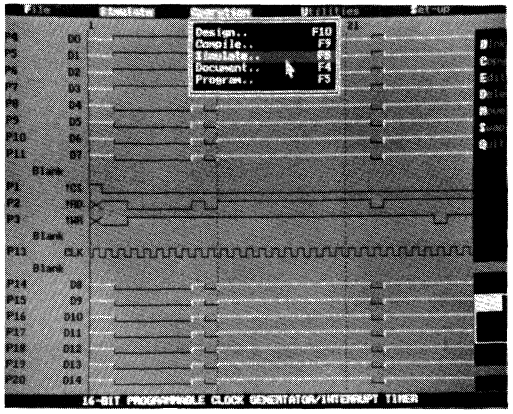
The PACE architectural editor graphically expands individual cells for detailed viewing and control of architecture and equations.



The PACE software functions in a mouse driven windows environment allowing easy access and control of all operations. Shown here is the file selection window.



The architecture of each cell can be specified by selecting the desired architectural element with the mouse and then "clicking" through all possible configurations graphically on the screen. Shown here is the PA7024s register selection of D, T or JK flip-flops.



The PACE logic simulator lets external and internal signals be fully simulated, analyzed and edited via a special waveform display. Simulation errors can be marked on the display for quick analysis.

Programming Support (as of October 1989)

International CMOS Technology (408) 434-0678

	PDS-1 PEEL™ Development System ❖	
ICT Part Number	**Software**	**Adapter**
PEEL18CV8	PDS-1 Software Version V1.20	PLCC-to-DIP Adapter PDA-20
PEEL22CV10	PDS-1 Software Version V3.20	PLCC-to-DIP Adapter PDA-24
PEEL22CV10Z		
PEEL20CG10		
PEEL153	PDS-1 Software Version V2.20	
PEEL253		
PEEL173	PDS-1 Software Version V2.00	
PEEL273		
27CX321	MPS-1 Software Version V2.10	MPA-1 Socket Adapter
27CX322		
27CX641	MPS-1 Software Version V2.00	MPA-1 Socket Adapter
27CX642		

Adams-MacDonald (408) 373-3607

	SMS Sprint Plus
ICT Part Number	**Software**
PEEL18CV8	Version V3.10 ❖
PEEL153	Version V3.2D ❖
PEEL253	
PEEL22CV10	Version V3.2I (August 1989)
PEEL22CV10Z	
PEEL20CG10	
27CX321/2	Version V3.2I (August 1989)

	Promac Model 11
ICT Part Number	**PM-1 Module Firmware**
PEEL18CV8	Version V1.12 ❖

	Promac Model 16-IV
ICT Part Number	**PS-3 Module Firmware**
27CX321/2	Version V2.0 ❖
27CX641/2	

Advin Systems (408) 984-8600

	Sailor-PAL ❖
ICT Part Number	**Software**
PEEL18CV8	Version V8.0
PEEL22CV10	Version V9.4
PEEL20CG10	Version V9.5
PEEL22CV10Z	
PEEL153	
PEEL253	
PEEL173	
PEEL273	

DATA I/O (800) 426-1045

	Unisite 40 ❖		
ICT Part Number	**Software**	**Family**	**Pinout**
PEEL18CV8	V1.4	8D	3A
PEEL22CV10	V2.3		28
PEEL22CV10Z			A3
PEEL20CG10	V2.2		56
PEEL153			65
PEEL253			85
PEEL173			76
PEEL273			86
27CX641/642	V2.3	82	67
27CX321/322		108	063

Unisite 40 Chipsite Module for PLCC		
Software	**Family**	**Pinout**
V2.6	08D	73A
		728
		7A3

Series 1000 ❖	
ICT Part Number	***SRT28 Adapter***
27CX321	V11
27CX641	

	Model 29B Programmer ❖			
ICT Part Number	**Module**	**Adapter / Firmware**	**Family**	**Pinout**
PEEL18CV8	LogicPak™ V04	303A-011A / V02	8D	3A
PEEL22CV10		303A-011A / V09		28
PEEL22CV10Z		303A-011A / V06		A3
PEEL20CG10				56
PEEL153				65
PEEL253				85
PEEL173		303A-011A / V04		76
PEEL273				86
PEEL18CV8J		303A-011B / V04		3A
PEEL22CV10J				28
PEEL22CV10ZJ				A3
27CX641/642	UniPak™ 2 or 2B		82	67
27CX321/322	UniPak™ 2 or 2B		108	063

	Model 60A ❖		*Model 60H* ❖		
ICT Part Number	**Adapter**	**Firmware**	**Firmware**	**Family**	**Pinout**
PEEL18CV8	360A-001	Version V11	Version V12	8D	3A
PEEL20CV10		Version V14	Version V14		28
PEEL22CV10Z					A3
PEEL153		Call Data I/O	Call Data I/O		65
PEEL253					85
PEEL173					76
PEEL273					86
PEEL18CV8J	360A-006	Version V14 (August 1989)	Version V14 (August 1989)		3A
PEEL22CV10J					28
PEEL22CV10ZJ					A3

BP Microsystems (800) 225-2102

	PLD 1100 ❖
ICT Part Number	**Software**
PEEL18CV8	Version 1.07
PEEL153	
PEEL253	
PEEL173	
PEEL273	
PEEL22CV10	Version 1.20

Inlab (303) 460-0103

	Model 28U
ICT Part Number	**Firmware**
PEEL18CV8	Version 11.02 ❖
PEEL22CV10	
PEEL153	
PEEL253	
PEEL173	
PEEL273	

Logical Devices (305) 974-0975

	ALLPRO Programmer
ICT Part Number	**Software**
PEEL18CV8	Version 1.44 ❖
PEEL22CV10	Version 1.47c
PEEL22CV10Z	Version 1.49
PEEL20CG10	(August 1989)
PEEL153	Version 1.47c
PEEL253	Please call Logical Devices
PEEL173	Version 1.45 ❖
PEEL273	
27CX641/642	Version 1.44 ❖
27CX321/322	Version 1.46 ❖

	GANGPRO-8 Programmer
ICT Part Number	**Firmware**
PEEL18CV8	Version 2.17
PEEL22CV10	(August 1989)
PEEL20CG10	

	PALPRO-2X Programmer
ICT Part Number	**Firmware**
PEEL18CV8	Version 5.2 (August 1989)

Stag Microsystems (408) 988-1118

	PPZ Programmer		*ZL-30A Programmer*	
ICT Part Number	**Module**	**Firmware**	**Module**	**Firmware**
PEEL18CV8	ZM2200	Version 34	30A800	Version 30A26
PEEL153		Version 37		Version 30A32
PEEL253				
PEEL173				
PEEL273				
27CX641/642				
27CX321/322				

System General (Taiwan) 2-7212613

	SGUP-85 ❖
ICT Part Number	**Firmware**
PEEL18CV8	Version 3.0
PEEL22CV10	
PEEL20CG10	Version 3.1

	SGUP-85 ❖
PEEL153	Version 3.1
PEEL253	
PEEL173	
PEEL273	

Kontron Electronics (800) 227-8834

	MPP-80S Portable Programmer with Universal Module UPM/B	*EPP-80 Base Programmer with Universal Module UPM/B*
ICT Part Number	**Firmware**	**Firmware**
PEEL18CV8	Version 2.1	Version 2.1
PEEL153	Please Call Kontron	Please Call Kontron
PEEL253		
PEEL173	Version 2.2	Version 2.2
PEEL273		
27CX641/642	Version 2.2	Version 2.2

Digelec (800) 367-8750, in California call (818) 887-3755

	Model 860 Programmer
ICT Part Number	**Software**
PEEL18CV8	Version A-1.3 ❖
PEEL153	Version A-1.4
PEEL173	Please call Digelec
PEEL253	Version A-1.4
PEEL273	Please call Digelec
27CX641/642	Please call Digelec
27CX321/322	Please call Digelec

PEEL Development Software Support

ICT Part Number	APEEL™ * by **ICT** (408) 434-0678	ABEL™ by **DATA I/O** (800) 426-1045	CUPL™ by **Logical Devices** (305) 947-0967	LOG/iC™ by **Isdata** (408) 373-3607
PEEL18CV8	V 2.0	V 2.1	V 2.15	V3.2
PEEL20CG10	V 3.0	V 3.0	V 3.00	
PEEL22CV10		V 2.1	V 2.15	
PEEL22CV10Z		V 3.0	V 3.00	
PEEL153	V 2.1	V 2.1	V 2.15	
PEEL253		V 3.0	V 3.00	
PEEL173		V 2.1	V 2.15	
PEEL273		V 3.0	V 3.00	

* The APEEL Logic Assembler and the PLD JEDEC File Translator are included in the PEEL Development Software

Article Reprints

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Logical Design Techniques for Architecturally Enhanced EEPLDs

Prepared for and presented at Wescon, 1988

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Logical Design Techniques for Architecturally Enhanced EEPLDs

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(408) 434-0678

Introduction

Logic designers today are confronted with a variety of new programmable logic device (PLD) architectures and technologies to choose from. Even after sorting through a multitude of PLD data sheets, selecting the right PLD for a given application can often become a trial and error process. Understanding the design techniques associated with a PLDs architectures can greatly minimize design effort and maximize logic utilization.

This paper specifically addresses techniques and the development process used to design with PEEL™ (Programmable Electrically Erasable Logic) devices. The examples provided will demonstrate how architecturally enhanced PEEL devices can achieve higher logic integration and flexibility than conventional PLDs.

PEEL™ Device Overview

PEEL devices (Programmable Electrically Erasable Logic devices), combine CMOS and EEPROM technologies to provide an attractive alternative to conventional PLDs. PEEL devices offer a sensible balance of performance, flexibility, ease of design, and production practicality that is needed by logic designers today.

Key features of PEEL devices include:

* **PEEL CMOS Performance** provides dramatically lower power consumption, lower operating temperatures and higher reliability than conventional bipolar PLDs

* **PEEL Architectural Flexibility** allows a few PEEL devices to functionally replace over 40 PAL and FPLA type devices, reducing the number of different parts needed in inventory. Additionally, PEEL enhanced architectures make it possible to put more logic into every package.

* **PEEL Ease of Design** is provided by free development software, a low cost PEEL development system and support from popular programmers.

* **PEEL EE-Reprogrammability** provides the convenience of instant reprogramming for development, no waste as with one-time-programmable PLDs, and no wait as with UV EPLDs. It also allows for a risk-free re-usable production inventory minimizing the impacts of programming changes or errors.

* **PEEL High Quality** is an inherent part of 100% testable PEEL technology. PEEL devices are shipped with a 50ppm Average Outgoing Quality Level for programming and logic function as compared to an average of 10,000ppm with bipolar PLDs.

* **PEEL Cost Effectiveness** means no hidden overhead costs as with bipolar PLDs, such as program/test yield loss, multi-device inventories, reject administration, board and field functional failure rework.

PEEL Device Family

The PEEL18CV8 was the first PEEL device, introduced in 1987. The initial family consists of nine devices varying in architecture, speed and power. The PEEL family is organized into two groups: direct replacement and super-set replacement devices.

Direct Replacement PEEL Devices

The direct replacement PEEL devices are essentially reprogrammable CMOS second-source alternatives to popular bipolar PAL and FPLA devices such as the PAL22V10, PLS153 and PLS173. These JEDEC-file-compatible PEEL devices include the PEEL22CV10, PEEL153 and PEEL173. As a direct replacement, CMOS PEEL technology brings the advantages of low power, high noise-immunity, reprogrammability, complete testability, and foolproof design security

Superset Replacement PEEL Devices

Designers who wish to go beyond the limitations of conventional PLDs will be interested in the superset replacement PEEL devices. These PEEL devices not only emulate standard 20 and 24-pin PLDs, but offer designers many new architectural and performance features. Two architecture types make up this group; programmable-

	ARCHITECTURE							SPEED		POWER	
Superset	Pins	Inputs	I/Os	Registers	Macro Configs	Prog. Arrays	Product / Sum Terms	Prop Delay (nS) t_{CO}	t_{PD}	Supply Current ICC (mA)	Z-Mode*
PEEL18CV8	20	10	8	8	12	AND	74	15-20	25-35	20 + 0.7/MHz	no
PEEL18CV8-15	20	10	8	8	12	AND	74	12-15	15-20	80 + 0.7/MHz	no
PEEL20CG10	24	12	10	10	12	AND	92	15-20	20-35	55 + 0.5/MHz	no
PEEL22CV10Z	24	12	10	10	12	AND	132	15-20	20-35	55 + 0.5/MHz	yes*
PEEL253	20	8	10	0	2	AND/OR	42/20	N/A	30-35	35 + 1.0/MHz	no
PEEL273	24	12	10	0	2	AND/OR	42/20	N/A	30-35	35 + 1.0/MHz	no
										*100uA Standby Current	
Direct	Pins	Inputs	I/Os	Registers	Macro Configs	Prog. Arrays	Product / Sum Terms	Prop Delay (nS) t_{CO}	t_{PD}	Supply Current ICC (mA)	Z-Mode
PEEL22CV10	24	12	10	10	4	AND	132	12-20	20-35	55 + 0.5/MHz	no
PEEL153	20	8	10	0	2	AND/OR	42/10	N/A	30-40	35 + 1.0/MHz	no
PEEL173	24	12	10	0	2	AND/OR	42/10	N/A	30-40	35 + 1.0/MHz	no

Figure 1. PEEL Device Family Specifications

AND/fixed-OR array devices (the 18CV8, 18CV8-15, 20CG10 and 22CV10Z) and programmable-AND/programmable-OR array devices (PEEL253 and PEEL273). The remainder of this paper will focus on the super-set devices.

The PEEL18CV8, 20CG10, and 22CV10Z

The basic architectures of the PEEL18CV8, 20CG10 and the 22CV10Z are similar. All four implement sum-of-products logic with a programmable-AND/fixed-OR structure. Depending on the device, between 18 to 22 inputs and 8 to 10 macrocell outputs are available (see figure 2) The core of each device is a programmable, electrically-erasable AND array consisting of input lines running perpendicular to product terms. The input lines are derived from the true and compliment of each potential input pin. The product terms include: one global synchronous preset term; one global asynchronous clear term; one output enable term per I/O; and groups of 8 logic product terms per sum for PEEL18CV8 and 20CG10, or a distribution of 8-16 terms per sum for the 22CV10Z.

I/O Macrocell Configurability

Each logical sum is directly associated with an I/O macrocell and I/O pin. The twelve-configuration macrocell provides control of output polarity, feedback path and output type (registered or combinatorial, dedicated input, output, or bidirectional I/O). The flexibility of the I/O macrocell not only makes these devices ideal for sequential or combinatorial applications, but also allows implementation of functions that might require multiple conventional PLDs.

The macrocell consists of a D-type flip-flop, an output mux, and a feedback mux. Four EE memory cells per macro-cell can program the configuration of each macro cell twelve different ways. The twelve possible I/O macrocell configurations are illustrated in figure 5.

The PEEL253 and PEEL273

The PEEL253 and PEEL273 offer super-set compatibility with the Signetics PLS153 and PLS173 FPLAs respectively (previously numbered the 82S153 and 82S173). Several architectural enhancements have been added (see figure 3). Notably, the output-enable control terms have been moved from the AND array to the OR array for complete sum-of-products control, while 10 general-purpose product terms have been added to the AND array for a total of 42. Both devices provide 10 I/Os, but the 20-pin 253 has 8 inputs, while the 24-pin PEEL273 offers 10 dedicated inputs.

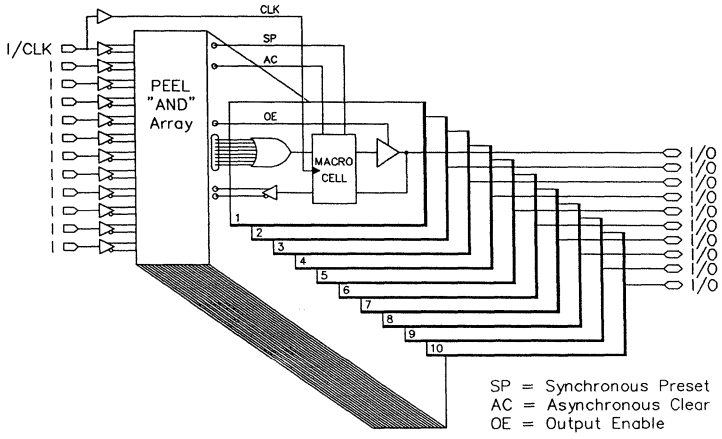

Figure 2. PEEL18CV8, 20CG10 and 22CV10Z Block Diagram

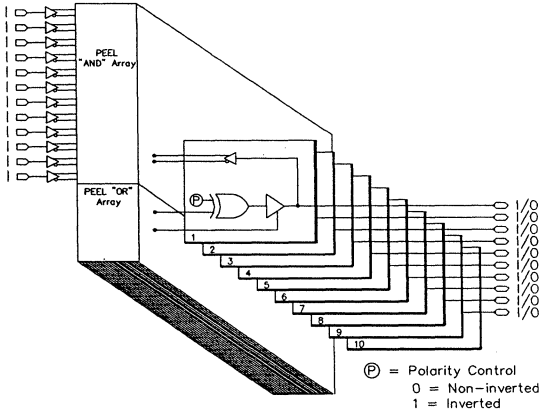

Figure 3. PEEL253 and PEEL273 Block Diagram

PEEL DEVELOPMENT TOOLS

The PEEL device family development support is provided by software and hardware tools available directly from ICT as well as from third party manufacturers such as Data I/O. ICT offers two packages, the PEEL Development Software and the PEEL Development System.

The **PEEL Development Software and Applications Handbook** is a free PC-based development package for designing with, evaluating and learning about PEEL devices. Key features include the APEEL™ Boolean-logic assembler/simulator and a PLD JEDEC-file translator which can automatically translate a wide variety of conventional PLD design files to PEEL programming files.

The PEEL Development System (PDS-1) is a powerful, low-cost, PC-based system for designing with PEEL devices. The PEEL Development System is a personal PLD work-station providing everything needed to implement logic designs from concept to silicon including: a built-in word processor for design entry and editing; the APEEL Boolean-logic assembler/simulator; a complete PEEL-device programmer; and enhanced logic tester. Additionally, PALs, EPLDs and FPLAs can be loaded and directly translated to PEEL devices. The complete development process for both the PEEL Development Software and PEEL Development System is shown in figure 4.

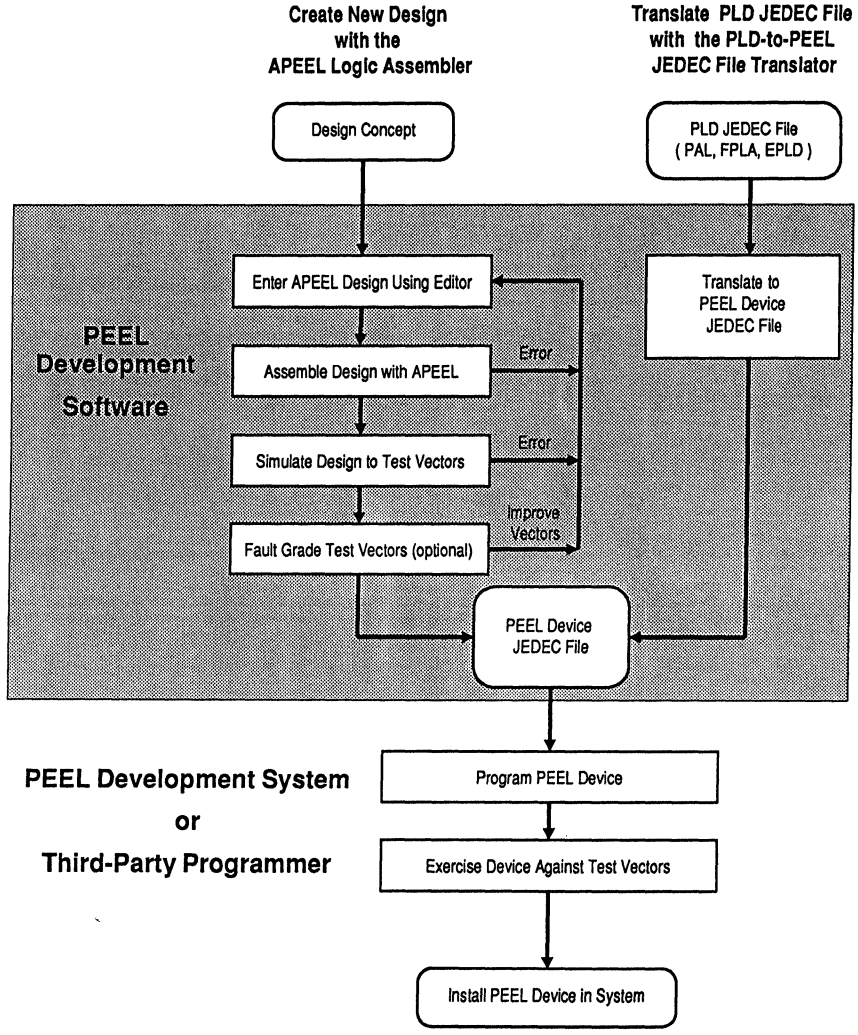

Figure 4. The PEEL Device Development Process

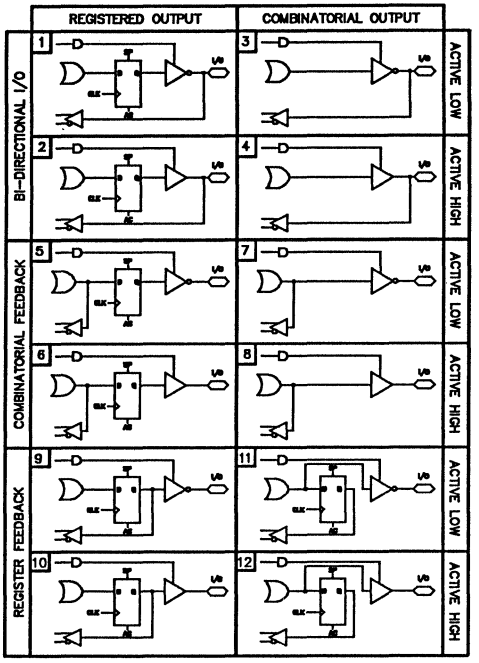

Figure 5. PEEL Device Twelve-Configuration

PEEL DESIGN TECHNIQUES

Designing with PEEL devices is much like designing with conventional 20 and 24 pin PLDs. However, PEEL architectures give designers additional flexibility, making it possible to fit more logic into a single package.

Standard Macrocell Configurations (3,4,9 &10)

Macrocell configurations number 3, 4, 9 and 10 (in figure 5) are four of the twelve PEEL device macrocell configurations that are most similar to the fixed I/O configurations used among standard PLDs such as the PAL16R8, PAL16L8, PAL18P8 and PAL22V10. PEEL devices, however, allow for each I/O pin to be independently configured as an input, output or I/O. Additionally, any output function can be independently configured as combinatorial, registered, active high or active low. Independent configurable I/Os make it possible to customize the PLD to your design rather than modifying your design to fit the PLD. These four standard macrocell configurations, can be used to implement a variety of logic functions such as random gates, encoders, decoders, multiplexers, latches, counters and shifters.

Independent Output Enables

Each I/O also has independent programmable output enables for both combinatorial or registered outputs. The output enables are helpful for bus interfacing as well as "wire-ORing" of signals. Each I/O can be enabled or disabled via individual product terms, even on registered outputs where most standard PLDs offer only a single output enable control pin. Output enables on the PEEL253 and PEEL273 are controlled in the OR array. This feature allows complete Sum of Products control making it possible to have complex function control of I/Os.

Bi-Directional Registered I/O (1 & 2)

Two of the additional PEEL macrocell configurations include bi-directional registered I/O both active-high and active-low, (#1 and #2 in figure 5) The difference between this configuration and the registered output of standard PLD (i.e.,16R8) is that the feedback is from the pin rather than the register. This makes it possible to use a registered output as an input also. Some possible applications for this include: synchronous-read/writable I/O, bus interfaced code conversion, and the wired-OR "Busy" function for bus arbitration circuits.

Buried Combinatorial Feedback (7 & 8)

Two additional macro cell configurations found in PEEL devices allow for buried combinatorial feedback before the output enable (#7 and #8 in figure 5). This configuration is very useful for creating latches or logic paths that must be used internally, but only appear externally when accessed by the processor (i.e., as when interfaced to a bus). Furthermore, this configuration is useful in reducing propagation delays when feeding an output signal back into the device for another logic function. This is because the signal is routed directly into the array rather than delayed through the I/O buffer at the pin. An example of how buried combinatorial feedback can be used is shown in the "Change-of-State Detector" application in the following section.

Buried Combinatorial Feedback with Register (5 & 6)

Two other PEEL macrocell configurations provide buried combinatorial feedback with a registered output (#5 and #6 in figure 5). This configuration lends itself towards clock synchronization applications. In such applications the buried combinatorial feedback can be used to create an asynchronous latch, the output of which will be stable for clocking into the register. This type of circuit can be used for interfacing data between two systems operating from different clocks or for simply synchronizing asynchronous signals. An example of how this configuration can be used is shown in the "Input Synchronizer" application in the following section.

Buried Register with Combinatorial Output (11 & 12)

Another useful macrocell configuration is the pseudo-buried register with combinatorial output (#11 and #12 in figure 5). This configuration allows the register output to be fed back into the array while the combinatorial function is routed to the pin. This configuration makes it possible to use the registers as programmable buried storage nodes while the outputs can be selectively addressed for reading onto a bus. Possible functions or applications for this configuration include; updatable or programmable comparitor, programmable dip-switch, buried control register, programmable mask register. An example of how this configuration is used can be seen in the "Change-of-State Detector" application in the following section.

Global Preset and Clear

The PEEL18CV8, 22CG10 and 22CV10Z each have a synchronous preset (SP) and asynchronous clear (AC) product term that control all the registers. Although these functions are fairly straight forward, there are some unique ways to take advantage of functions especially for counters and state machines. An example of this is shown in the 8-bit Counter with Function Controls application example in the application section of this paper.

APPLICATION EXAMPLES

The following pages include a few application examples that demonstrate ways to take advantage of some of the PEEL device architectural enhancements. All of the examples were designed using the APEEL logic assembler and simulator. The actual APEEL source file for one application is included for reference.

Input Synchronizer (PEEL18CV8)

Quite often systems need to synchronize an asynchronous input in order to avoid potential metastability conditions that can be caused by set-up time violations. A common method for doing this uses two rippled D-type flip-flops (i.e., 74LS74) as shown in figure 6. In this circuit the asynchronous input is feed into the D of the first flip-flop and the Q of the first is feed into the D of the second. The resulting Q output of the second flip-flop will be synchronized to the clock.

PEEL devices can implement the same type of circuit requiring only one input pin, one output pin and a system clock. This is accomplished by using the internal feedback with-register macrocell configuration (#5 or 6 in figure 5) and the clock signal which is provided in the AND array. The PEEL circuit , shown in figure 7, is comprised of a gated-latch that internally latches the asynchronous input on the falling edge of the clock. This holds the input stable to adequately meet the set-up time of the register which is clocked on the rising edge. If by chance the input violates the set-up time of the gated latch, the clock low time will encounter any possible metastability stabilizing in time for the high-going register clock.

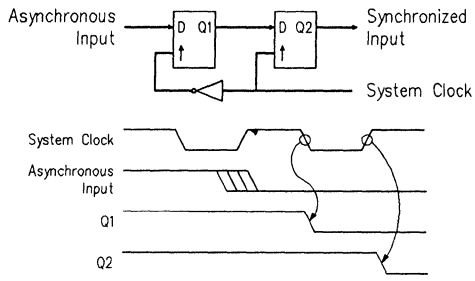

Figure 6. Input synchronization using standard logic

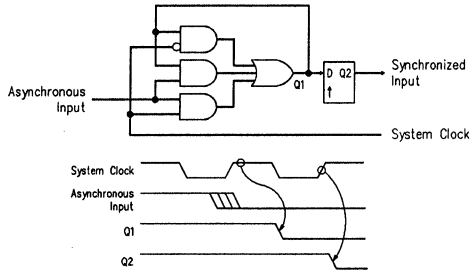

Figure 7. Input synchronization using a PEEL18CV8

If multiple input synchronizers are needed for a system, the PEEL device solution becomes even more elegant. This is because only two pins per synchronizer are needed. Thus, a PEEL18CV8 could implement eight such synchronizer circuits in a single 20 pin package

The equations for this circuit are shown below. Although using the clock signal in the equations may look like a possible race condition, this is not the case because of the zero hold time allowed for PEEL device registers. A possible logic hazard is removed (a high-low-high glich) by ANDing the input (IN) and the internal feedback signal (Q2). Note, the Q2 signal used on the right side of the equation actually represents the internal combinatorial feedback labeled as Q1 in figure 7.

```
Q2 :=  CLK &  IN #  "when CLK=1 allow input to set-up
       !CLK & Q2 #  "when CLK=0 latch input internally
         IN  & Q2   "prevent hazard condition
```

8-Bit Counter with Function Controls (PEEL18CV8)

A free-running re-setable 8-bit counter is a fairly common function for a conventional 20-pin registered PLD like the PAL16R8. However, try adding control functions such as load or hold and you will quickly realize that it is not possible. This is because the number of product terms used per bit for a binary D register counter is N, that is, bit 1 uses one product term, bit 2 uses two and bit 8 uses eight. Since there are only eight product terms per SUM (as is the case for most every 20-pin registered PLD), all the product terms for bit-8 are used for counting.

In order to implement the load or the hold function of at counter, an additional product term is needed per bit. Because of this, most 8-bit load or hold counters are designed using a 24 pin device like the 22V10 which has additional product terms. The 20-pin PEEL18CV8 however, can implement a loadable or holdable 8-bit counter plus more, by taking advantage of its synchronous preset and asynchronous clear terms. The synchronous preset term specifically, can be used to free up a product term of eigth bit. The product term function is the last count before all bits are set to one as shown in the equation below. Freeing this product term from the eigth bit now makes it possible to add either the load or hold condition for all eight bits.

```
SP := Q7 & Q6 & Q5 & Q4 & Q3 & Q2 & Q1 & !Q0
```

An example of the type of multi-function 8-bit counter that can be designed with the 18CV8 is shown in figure 8. In this application the PEEL18CV8 implements an 8 bit counter with four control functions: hold, reset, repeat and output enable. The operation of each control is listed below.

SYNCHRONOUS RESET - When set high, the outputs (Q0-7) will go low after the next clock. When set low, the counter will start counting up with each clock.

HOLD COUNT - When set high, the count will hold the present state. When low, the count will resume.

REPEAT COUNT - When set high, the counter will repeat the count after reaching FF HEX. When set low, the counter will stop after one complete count. The asynchronous clear product term is used for this function.

OUTPUT ENABLE - When high, the outputs will be disabled and will enter a high impedance state. When low, the outputs are enabled.

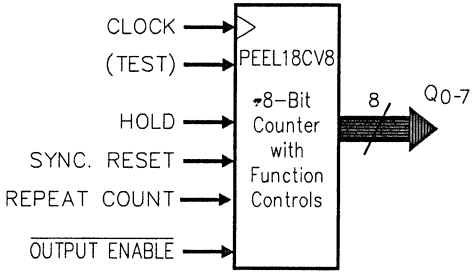

Figure 8. PEEL18CV8 8-bit Counter with Hold and other function controls.

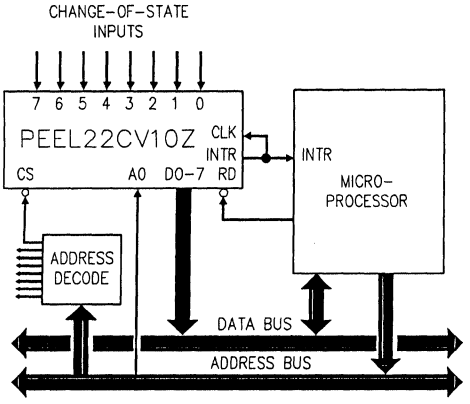

Figure 9. PEEL22CV10Z Change-of-State

Change-of-State Detection Port (22CV10Z)

The application shown in figure 9 uses the PEEL22CV10Z as a intelligent input port that off-loads the µP from having to perform software polling. The change-of-state port incorporates eight inputs that are monitored for a change-of-state (low or high). If a change occurs an interrupt will be sent to the µP. The µP can then read either the eight pseudo buried registers holding the change-of-state or read inputs directly. Uses for such an application include; sensor monitoring, "glitch" detection, communication handshaking and clock synchronization. Figure 10 shows a block diagram of the functions implemented.

The operation of the Change-of-State Detection Port is as follows: Any change on the inputs (low-to-high or high-to-low) can be detected via an 8-bit non-equality comparitor (NEQ). When detected, the INTR latch output is set for interrupting a µP. The INTR output is also used to clock the 22CV10Z which latches the input state into eight pseudo-buried registers. The µP can then read the registers on D0-D7 when CS, RD, and A0 = 0. Once read (unless another change has occurred) the INTR latch will be reset . The I0-I7 pins can be read directly by properly addressing the A0 input (A0 = 1).

If power-consumption needs to be minimized the "zero-power" feature of the 22CV10Z works well for this application, especially when used with CMOS micro-controllers that also have power-down modes. Using the zero-power feature, the 22CV10Z will power down when all inputs pins stop changing for approximately 50-100nS. Thus the power consumption for the 22CV10Z will be approximately 100uA unless a change-of-state occurs or the micro-controller addresses the device.

All preceding applications were created using the PEEL Development System with APEEL™ logic assembler. For more detailed information on these and other applications refer to the ICT PEEL Software and Applications Handbook.

Conclusion

Flexible and architecturally enhanced PEEL devices, along with easy-to-use PEEL development tools, help PLD designers get more logic into every package. Additionally, PEEL device CMOS EE technology provides a lower power, reprogrammable and higher quality alternative to conventional PLDs.

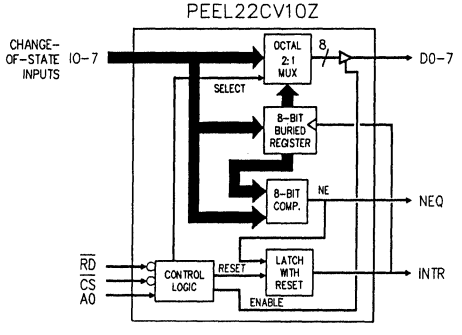

Figure 10. PEEL22CV10Z Change-of-State Detector functional block diagram

8

Electronic Products

Electrically Erasable CMOS PLDs Conquer Tradeoff Dilemmas

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Electrically erasable CMOS PLDs conquer tradeoff dilemmas

High speed, low power, flexibility, and low cost all combine in a new class of programmable logic devices

Robin J. Jigour
International CMOS Technology
San Jose, CA

Designers selecting a programmable logic device were forced, until now, to make tradeoffs. Conventional PLDs offer high speed but sacrifice power consumption. Newer CMOS devices have reprogrammability or flexible architectures but typically cost too much to be practical for original-equipment manufacturing. The tradeoffs of versatility, performance, and cost meant that the end product seldom came out exactly as originally or ideally desired.

Dilemmas dissolved

Now the designer can eliminate such tradeoffs with two just-introduced *programmable logic devices* (PLDs), the PEEL18CV8 and PEEL22CV10, from International CMOS Technology. Fabricated with an advanced CMOS EEPROM technology (see *box*, "CMOS and EEPROM technologies team up"), the *programmable electrically erasable logic* (PEEL) devices rival speed parameters of standard bipolar PLDs (t_{PD} is 25 ns max). They consume as little as one-eighth the power for TTL interfacing (I_{CC} is 20 mA standby + 7 mA/MHz) and even less for CMOS interfacing. Moreover, the electrically erasable reprogrammability not only adds convenience and cost savings for prototyping or field retrofitting, but also allows the PEEL devices to be fully tested in the factory to ensure 100% programmability and functioning.

Packaged in 300-mil, 20- and 24-pin DIPs, the PEEL devices have a flexible architecture that lets them replace standard SSI/MSI logic circuitry. Using the PEEL devices in this manner can substantially reduce parts count, save board space, and simplify inventory control. Also, because of their pinouts and architec-

tural compatibility, they can replace most of the 20- and 24-pin PALs from Monolithic Memories and other suppliers (see *Tables 1 and 2*), plus the Altera EP300/310 and AMD 22V10. In addition, over 100 new configurations, not possible with the earlier generation of PLDs, can be implemented. This flexibility enables a designer to focus on his or her design rather than on the restrictions of a fixed architecture.

A logical architecture

In their basic architecture, the PEEL18CV8 and PEEL22CV10 resemble conventional PLDs, which use a sum-of-products logic array in a programmable-AND, fixed-OR structure (*Electronic Products*, Mar. 3, p. 35). This familiar logic arrangement allows designers to program the connection of input signals to the array to create user-defined output functions. What makes the architecture of the PEEL devices different, however, is greater integration and flexibility. The parts have approximately 300 to 600 equivalent gates and a user-configurable architecture that increases flexibility.

The 20-pin PEEL18CV8 has one input or clock pin, nine input-only pins, and eight pins that can serve as either inputs or outputs; the 24-pin PEEL22CV10 has an additional two dedicated inputs and two I/Os (see *Fig. 1*). Therefore, on the PEEL18CV8, a maximum of either 18 inputs or 8 outputs can be used (but not both maximums simultaneously). The 18 inputs are complemented into 36 lines, which can be programmed for connection to product terms (AND gates) that are divided into groups of eight, each feeding into an OR function. Each OR function is directly associated with one of eight independent macrocells and I/O pins.

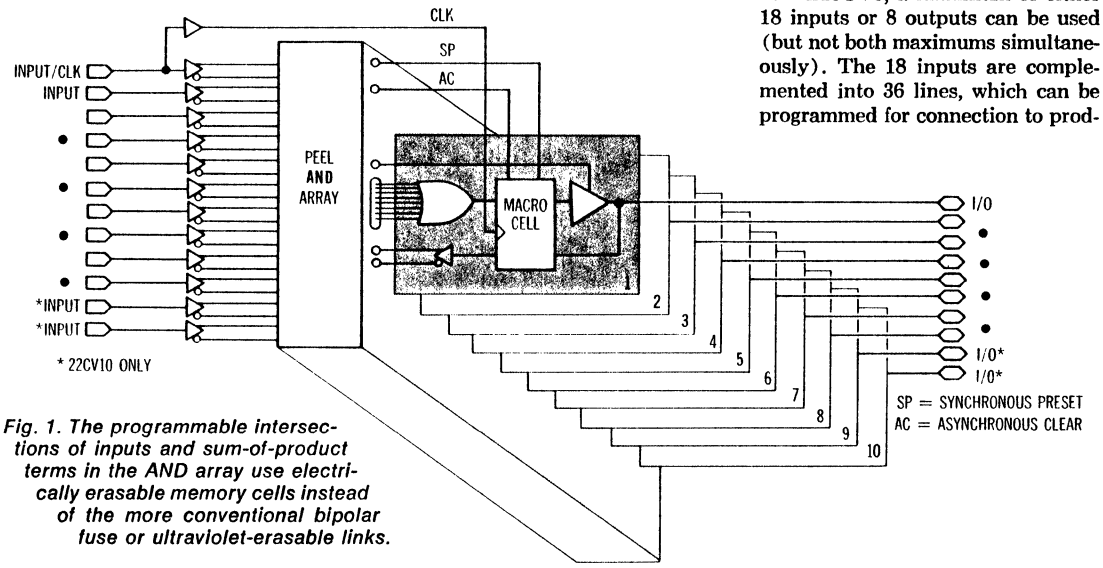


Fig. 1. The programmable intersections of inputs and sum-of-product terms in the AND array use electrically erasable memory cells instead of the more conventional bipolar fuse or ultraviolet-erasable links.

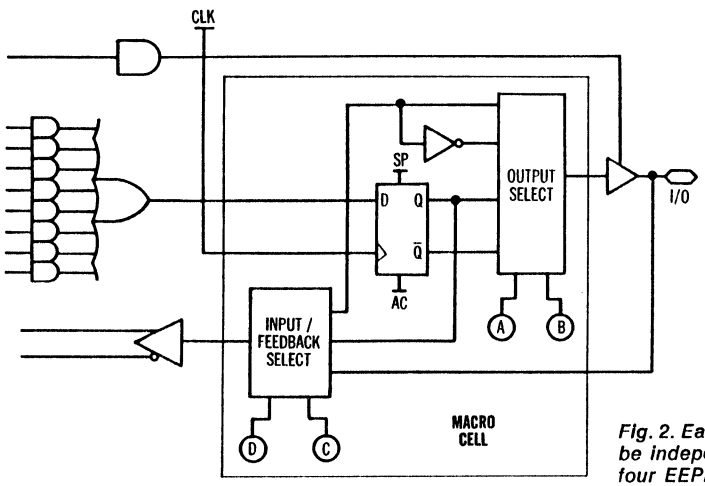


Fig. 2. Each I/O pin of a PEEL macrocell can be independently programmed by means of four EEPROM bits to assume one of twelve different I/O configurations.

Intersections programmed

Each input-line intersection to the AND array has an associated programmable EEPROM cell that determines whether the intersection is connected or open. Thus, each product term equals a 36-input AND gate, although that number of inputs is unlikely in a real application. Also available are product terms for a synchronous-preset term, an asyn-

8

chronous-clear term, and eight output-enable terms, which with the 64 AND product terms makes a grand total of 74 maximum product terms. The PEEL22CV10 has a total of 132 product terms.

The key to flexibility

The flexibility of the PEEL18CV8 is due primarily to its I/O macrocell. Each macrocell (see *Fig. 2*) consists of a D-type flip-flop and two signal-select multiplexers (output and input/feedback). The multiplexers can be programmed via four electrically erasable memory bits (A, B, C, and D) to assume one of 12 configurations (see *Fig. 3*). The configurations include various arrangements for bidirectional I/O, registered or combinatorial feedback, registered or combinatorial output, and output polarity control. The independence of the macrocells allows flexibility: a single PEEL18CV8 can implement a combination of eight different I/O configurations within its eight macrocells.

Broad range of applications

Like SSI/MSI logic, conventional PLDs, and low-density gate arrays, the PEEL18CV8 and PEEL22CV10 can be used in all the primary areas of system design, including data processing, communications, and industrial, consumer, military, and transportation applications. Specific functions implemented using the PEEL devices range from basic logic and system-support circuitry to standalone controllers. Application possibilities fall into four categories:

- SSI/MSI logic replacement and customization: random logic, latches, decoders/encoders, comparators, multiplexers, counters, shift registers
- Processor system support: address decoding, bus demultiplexing, wait-state generation, memory refresh, memory protection, dual-port memory control, DMA control, interrupt prioritization, interrupt vectoring, timer/counter functions, bus arbitration and interface, error detection and correction
- I/O interfaces and support: intelligent I/O ports, data-communications interfaces, display and front-panel interfaces, keyboard scanning, disk and tape drive controls
- Standalone nonmicroprocessor-based controllers: motor control, sensor monitoring, security access control, display control.

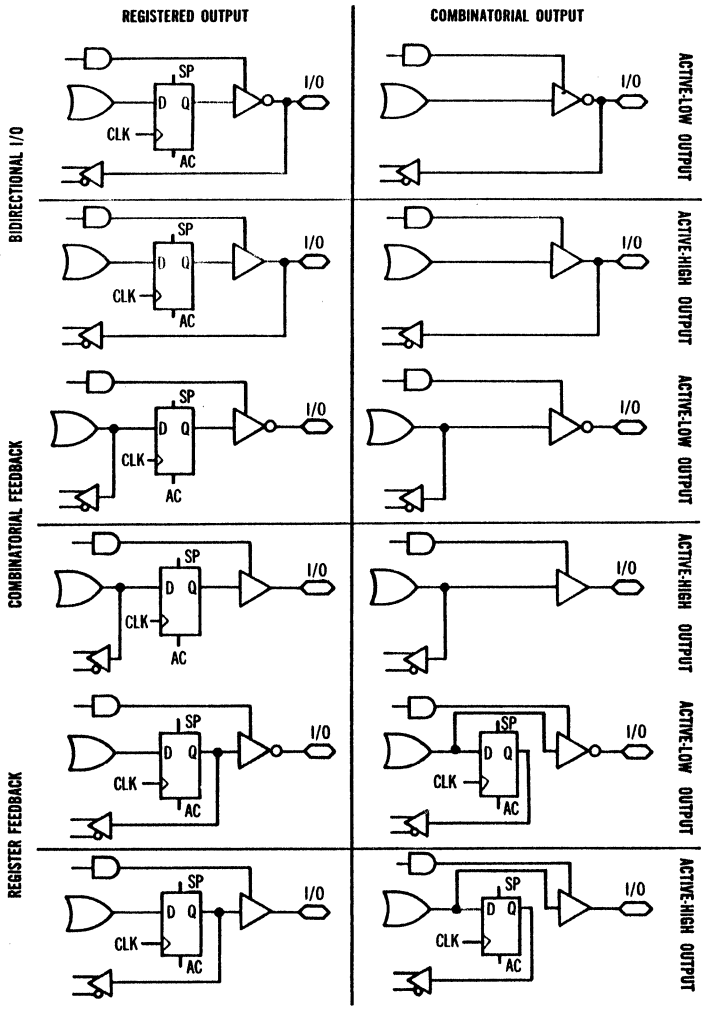
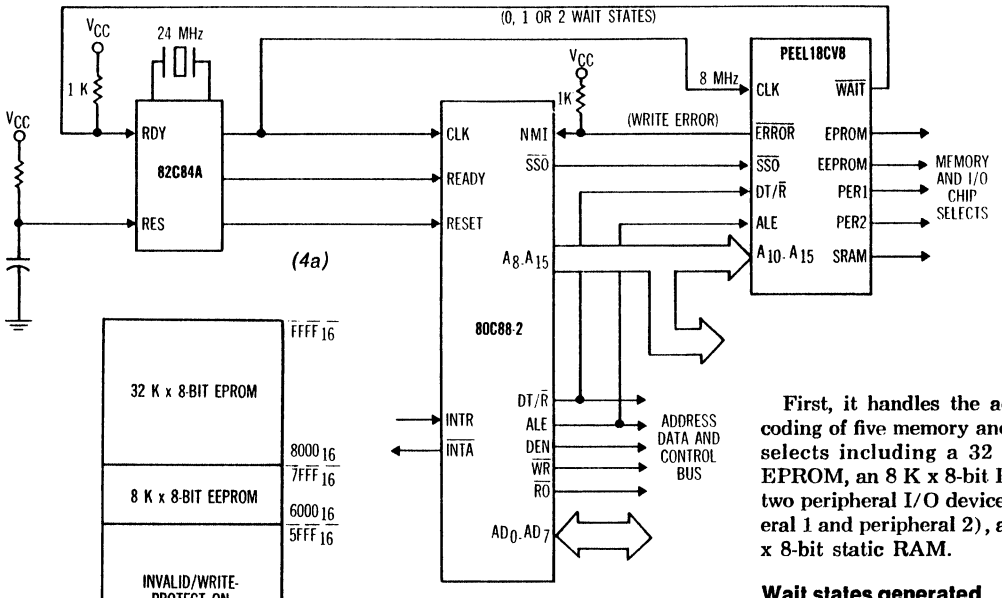


Fig. 3. Circuits equivalent to the 12 possible I/O configurations of the PEEL devices include various arrangements of bidirectional I/O, registered or combinatorial feedback, registered or combinatorial output, and output polarity control.

Off-the-shelf customizable ICs

One of the key benefits of designing with PLDs is that they are off-the-shelf standard products that can be customized without the substantial nonrecurring engineering costs associated with other customizing methods like gate arrays. Microprocessor system support and interface is an application area where PLDs are commonly used because designs tend to be unique, lending themselves to off-the-shelf customized components.

A prime example of this is a PEEL18CV8 programmed to function as a *WAW*: a Wait-state genera-



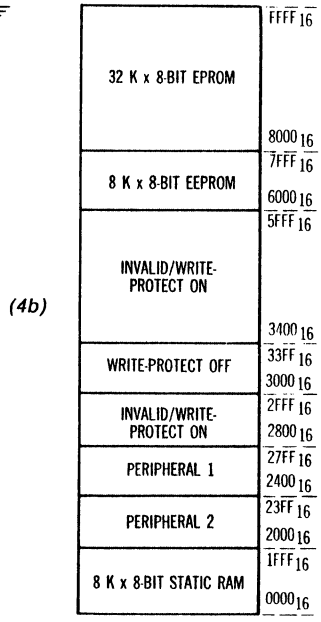


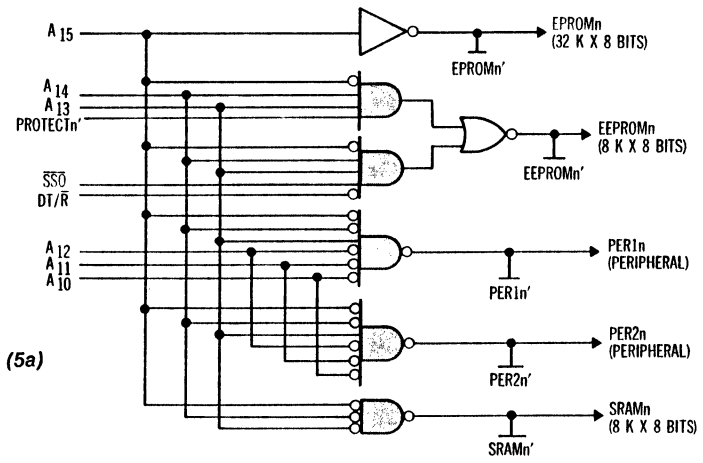
Fig. 4. A block diagram (a) and memory map (b) show the PEEL18CV8 as a Wait-state generator, Address decoder, and Write protector.

tor, Address decoder, and Write protector with interrupt circuits. The WAW is used to support an 8-MHz CMOS 8088 microprocessor in a small system having up to 64 Kbytes of memory-mapped address space (see *Fig. 4*). It has four primary functions.

First, it handles the address decoding of five memory and I/O chip selects including a 32 K x 8-bit EPROM, an 8 K x 8-bit EEPROM, two peripheral I/O devices (peripheral 1 and peripheral 2), and an 8 K x 8-bit static RAM.

Wait states generated

Second, it generates wait states—zero, one, or two—based on the address currently selected by the processor. This allows slower memory or I/O devices to be used without sacrificing faster devices' speed. (In the case of the WAW, peripheral 1 and the EEPROM each need one wait state, and peripheral 2 requires two.)



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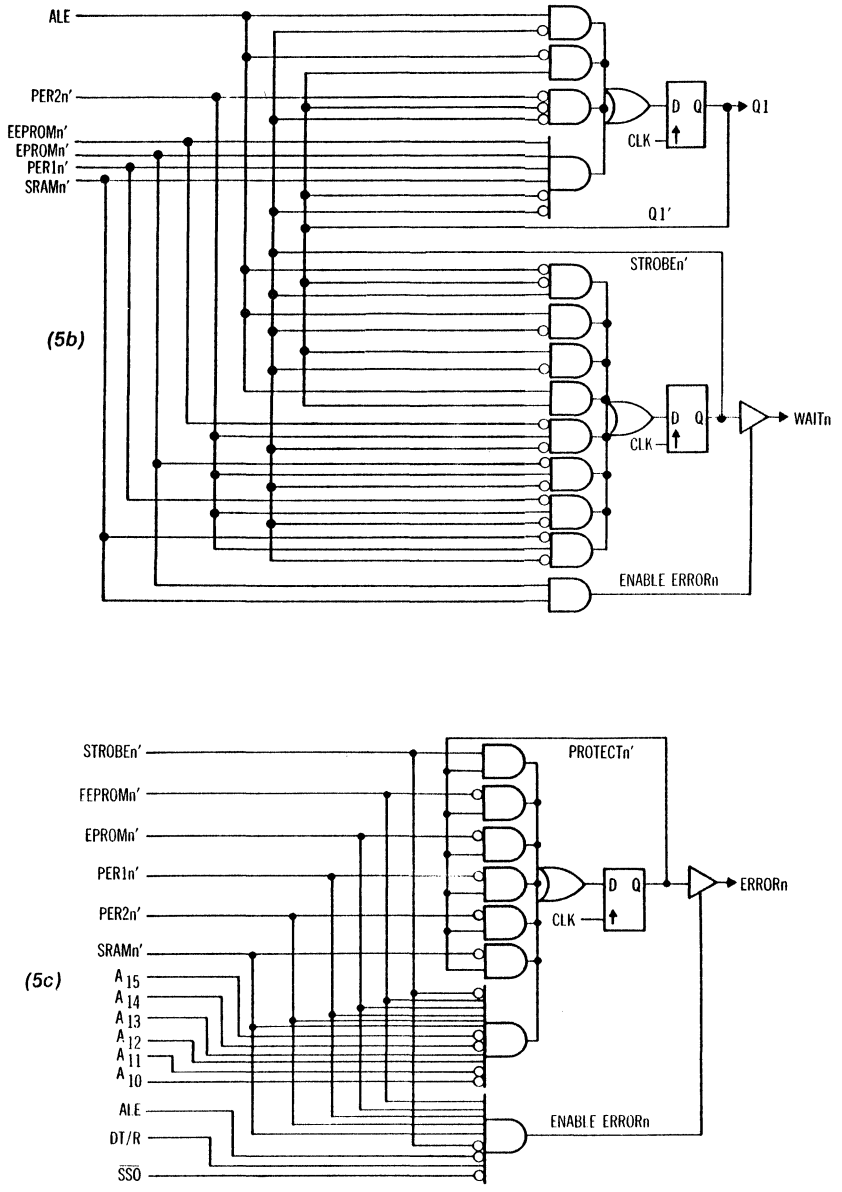

Fig. 5. The PEEL18CV8 WAW application was designed using a Boolean equation compiler. Shown here are the equivalent circuits to the equations for an address decoder with EEPROM write protection (a), wait-state generator (b), and write-protector register with interrupt (c). These three circuit functions are implemented in a single 20-pin package.

CMOS and EEPROM technologies team up

The performance and flexibility of the PEEL programmable logic devices is due primarily to their advanced 1.8-μm CMOS EEPROM technology. With special design and processing techniques, the just-announced PEEL18CV8 and PEEL22CV10A maintain the low power, noise immunity, and reprogrammability of EPROM PLDs while they achieve the speeds and cost-effectiveness of the standard fuse-link type of bipolar PLDs.

Although the design attributes of the PEEL devices alone make them attractive candidates for almost any logic design task, what truly sets them apart from other PLDs is their low cost.

This low price results in part from small die size, minimized mask steps and transistor types, less expensive windowless packaging (compared to EPROM-based PLDs), and enhanced factory testability to boot.

Electrical reprogrammability employs Fowler-Nordheim tunneling techniques to trap charges onto a floating gate through a thin oxide insulator. The trapped charges remain after power has been removed, so that programmed data becomes nonvolatile. The charges can later be removed via electrical erasure. Once fully erased, the chip can be reprogrammed with a new configuration.

The PEEL devices are designed for programming endurance of up to 1,000 complete erase/reprogram cycles with a data retention of 10 years. This means they can be reprogrammed up to 1,000 times without degrading operation and, as in other nonvolatile memory technologies, the data last programmed will remain valid for 10 years.

Although implemented in EEPROM technology, often associated with in-system reprogrammable memory devices, the PEEL18CV8 and PEEL22CV10A are programmed out-of-system via a PLD programmer. The PEEL technology, though, besides its other advantages over its competitors for programmable logic—lower power consumption, higher noise immunity, reprogrammability, and so on—has foolproof design security.

Foolproof design security means that unauthorized copies of designs using the PEEL technology are more difficult to make than those that use fuse-link technology. The fuse links of bipolar PLDs can be seen by magnifying an opened package, whereas for all practical purposes, the interconnections of a PEEL device cannot be readily examined because the links are electrical.

But perhaps most appealing of all to PEEL users is the devices' 3-s erase/reprogram time, instead of approximately 20 min for EPROM PLDs.

Third, it write-protects any chip select, which it sets on or off via the processor by reading specific address locations. Protection also is set on at power-up or after any write to an invalid address. In this case, the EEPROM is write protected to avoid accidental writes by the processor when in an unstable state such as power-up or, especially, power-down. (The voltage-sensing protection provided on many EEPROMs and other nonvolatile memory devices does not provide foolproof protection against such occurrences.)

Finally, it sends a write-error interrupt to the CPU (edge triggered low or high) when a write is attempted to any protected or invalid address space.

Although the specific details vary from system to system, these four functions have usually been implemented using TTL SSI/MSI or PAL devices. In fact, duplicating this same design using conventional logic requires a minimum of 10 TTL SSI/MSI parts. The use of PAL devices can reduce parts count, however. This application, for example, would take at least two 20-pin PAL devices (such as a 16R4A and 16L8A), whereas the architectural flexibility and gate density of the PEEL18CV8 allows the entire circuit to be incorporated into a single 20-pin package.

This increased flexibility results from the PEEL18CV8 permitting an odd number of registered and combinatorial outputs. In addition, the registered signals employ independent output enables, and 10 inputs and 8 mixed-function outputs are used. These benefits are not possible

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PEEL development packages available

Along with its new PLDs, International CMOS Technology offers various personal-computer-based PEEL evaluation-and-development-tool packages, which handle translation from existing PLD designs into the PEEL format. Additionally, popular third-party PC-based development tools and standalone programmers support the PEEL PLDs. New designs can be entered using Boolean logic definition or schematic capture.

Table 1.
20-Pin PAL Devices Architecturally Emulated by the PEEL18CV8

Output type	Part number and I/O capacity								
Combinatorial-high	10H8	12H6	14H4	16H2			16H8	16HD8	
Combinatorial-low	10L8	12L6	14L4	16L2			16L8	16LD8	
Combinatorial-polarity							16P8		18P8
Registered-low					16R4	16R6	16R8		
Registered-polarity					16RP4	16RP6	16RP8		

Table 2.
24-Pin PAL Devices Architecturally Emulated by the PEEL22CV10

Output type	Part number and I/O capacity								
Combinatorial-low	12L10	14L8	16L6	18L4	20L2			20L8	20L10
Registered-low						20R4	20R6	20R8	

with a single 20-pin PAL device.

Besides these advantages, current consumption of the PEEL18CV8 in this CMOS system is less than 25 mA max. Using two aforementioned PAL devices would require 360 mA max—three times that of the 80C88 and 82C84 together.

Moreover, the reprogrammability of the PEEL18CV8 could also be beneficial for applications of this type. For example, systems with a PEEL could be factory customized, or upgraded in the field, for faster or slower memory and I/O, a different number and address range of chip selects, or the addition or deletion of write-protection features.

From equation to operation

Defining the PEEL18CV8 to handle the functions of the WAW could involve simply specifying the circuit's Boolean equations using a PC-based logic compiler software package. A schematic-capture technique could be used. Simulating and testing the circuit in software could then follow, and a fuse map file created for the circuit could thereafter be used to program the device on a PLD programmer. After all these steps, the PEEL18CV8 can go to work.

Figure 5 shows the equivalent circuits of the Boolean equations used to define the PEEL18CV8 as the WAW. Although divided into three specific sections, they are interdependent. Address decoding (see *Fig. 5a*) is implemented simply by gating specific states of the 80C88 A_{10} to A_{15} signals to cause the appropriate active-low chip selects. The EEPROM chip select is further controlled by the state of the write-protection register and the DT/$\overline{R}$ and $\overline{SSO}$ signals, which provide the advance status of a write cycle being executed.

Small state-machine set

The wait-state generator (see Fig. 5b) is actually a small state machine, which is set during the ALE pulse that occurs at the beginning of each 80C88 machine cycle. Depending on the address-decoded chip select, a low strobe for either one or two clocks is generated at the rising edge of the 80C88 T_2 clock state. The strobe is then used for wait-state generation, provided the wait output isn't disabled by a chip select that doesn't require a wait state—as is the case for the WAW circuit when either the EPROM or the SRAM is selected.

The strobe from the wait-state generator is also used for the internal control timing of the write-protect register and error-interrupt circuit (see *Fig. 5c*). This section of the design decodes the address for write protection and stores its on-off condition for use by the address decoder and interrupt output. If a write to the EEPROM or an invalid address occurs while a protect condition is on, a two-clock, active-low interrupt is enabled to the error output. When disabled, this output goes into a high-impedance state, allowing other interrupt sources to control the same line (in a wired-OR fashion) by pulling down the connected 1-kΩ pull-up. The wait output can also be used in this way. □

ELECTRONIC DESIGN

PLD Synchronizes Asynchronous Inputs

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PLD SYNCHRONIZES ASYNCHRONOUS INPUTS

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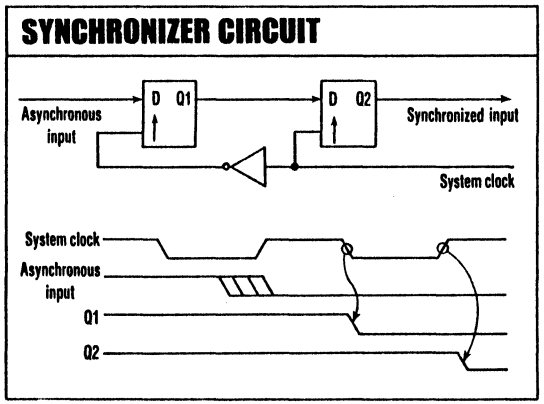
Digital systems often require synchronization of asynchronous inputs to avoid the potential metastability problems caused by setup-time violations. A common synchronization method uses two rippled 74LS74 D-type flip-flops *(Fig. 1)*.

In this circuit, the asynchronous input feeds into the D input of the first flip-flop and its Q output feeds into the D of the second. Because the first flip-flop latches on the falling edge of the system clock, to avoid setup-time violations, the D input signal to the second flip-flop will be stabilized before the rising edge of the clock. Even experienced programmable-logic-device designers often resort to such a TTL flip-flop circuit to handle the synchronization function, because of the architectural limitations of standard PLDs.

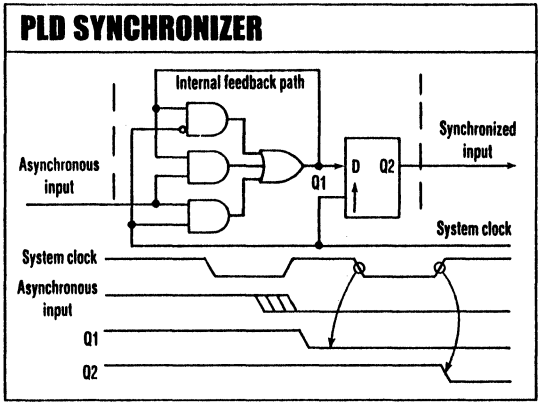
A programmable electrically erasable logic (PEEL) device, such as the PEEL18CV8 from ICT, however, can easily supply the function *(Fig. 2)*. The user-programmable 12-configuration I/O-macrocells in the device can internally feed back a signal before the output register. With this feedback arrangement, designing a two-stage input is simple.

A gated-latch internally latches the asynchronous input on the falling edge of the system clock, generating the signal Q1. ANDing the input with Q1 through the internal feedback path, eliminates a possible hazard condition during the clock's high-to-low transition time. The latch then holds Q1 stable to ensure meeting the setup-time requirement of the subsequent D flip-flop which, as before, registers the signal on the next rising system clock edge.

If by chance the input pulse width violates the set-up time of the gated latch, the clock's low time, will give more time for settling.□



1. A COMMON SYNCHRONIZATION method uses two rippled 74LS74 D-type flip-flops.



2. A PROGRAMMABLE ELECTRICALLY erasable logic (PEEL) device can easily supply the synchronizing function.

Electronic Engineering
TIMES

Benefits from EEPLDs are Company-Wide

Benefits from EEPLDs are company-wide.

By Robin J. Jigour
Director of Marketing
and
Greg Lara
Product Marketing Engineer
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San Jose, Calif.

Recently, CMOS Electrically Erasable (EE) PLDs such as the Programmable Electrically Erasable Logic (PEEL) devices from ICT have started to pervade the design community as an alternative to conventional PLDs. EEPLDs offer company-wide benefits in design, purchasing and manufacturing, while satisfying such key PLD design concerns as low power consumption and architectural flexibility. The net result: It costs less to use EEPLDs than conventional PLDs.

The most obvious benefits of EEPLD technology arise during development. Engineers designing with bipolar PLDs or one-time programmable (OTP) EPLDs must reprogram every time there is a PLD design revision. Reprogrammable EEPLDs save money since they can be be reused and reprogrammed rapidly.

Many EEPLDs also offer user-programmable architectures. In addition, three options for the feedback path are available regardless of what output structure has been chosen. Thus the user can tailor the output structure of the device.

EEPLDs for purchasing

Conventional 20- and 24-pin PLDs are produced in a number of fixed architectures, and each architecture carries various speed/power ratings. In all, there are well over 100 different devices on the market. What's more, a healthy variety of these PLDs may show in one particular product. Such proliferation translates into more headaches—specifically paperwork, ordering, tracking, scheduling and inventory control.

Conversely, with their flexible architectures, one or two EEPLDs can replace many PLDs. Also, EEPLDs create a risk-free inventory because they are reprogrammable.

Finally, EEPLDs help reduce distributor's risk as well. If the customer's delivery requirements are reduced or the programming pattern is changed, preprogrammed EEPLDs can be reused, making Just-In-Time (JIT) programs a reality. EEPLDs also give the distributor greater flexibility in responding to the demand for components in today's thriving electronics market.

EEPLDs for manufacturing

For system manufacturers, the greatest benefit of EEPLD technology is higher component quality and reliability resulting from the chip manufacturer being able to fully test each electrically erasable device.

While other PLD technologies limit factory testability, the EEPLD supplier can ensure 100 percent programming yield, and functional and parametric performance. With bipolar fuse-link PLDs it is impossible to fully test the array for the ability to program or function properly; to do so requires programming the array which, of course, renders the device useless to the customer (unless it is programmed to the customer's pattern).

Chip manufacturers try to get around this limitation by programming test fuses that are invisible to the end user. Still, they are unable to test the user-programmable fuses in the logic array. Nor are they able to guarantee that the device will perform the user's logic function when all of the input and feedback paths in the array must work together.

Thus, a percentage of devices shipped to the customer will fail for program/verify, basic logic function and ac/dc performance. Users of bipolar PLDs must assume the burden of completing the test cycle if they wish to ensure the device quality and reliability.

While CMOS EPLDs allow greater testability than bipolar PLDs, their long UV erase cycles and OTP "windowless" packaging limit the number of tests the chip manufacturer can perform. Most factory testing of EPLDs is done during wafer sort testing (of unpackaged die) at room temperature (approximately 25°C). If packaged as OTP EPLDs, the devices can no longer be erased. Thus, the actual memory cells to be used by the customer can not be programmed to allow high-temperature testing. Instead, phantom arrays are often used to correlate the function and performance of the rest of the part.

EEPLDs, on the other hand, provide instant erasability and unlimited reprogrammability for thorough testing at both wafer sort and final test. They use the only non-volatile device technology that gives the chip manufacturer the ability to test the actual logic array that is programmed by the user. After assembly, the packaged devices can be tested at the maximum rated temperature in high-temperature handlers. These advantages serve all three sides of a company—design, purchasing and manufacturing.

Most bipolar PLD manufacturers publish the failure rates that a customer can expect for programming and basic function fall-out. These failure rates vary greatly depending on the bipolar PLD manufacturer, the device type and even the specific lot (date code) of the devices received. The published failure rates range from 1 percent to 3 percent for program/verify failures, and 0.1 percent to 3 percent for basic function failures.

Quantifying cost

For all of the above stated factors, quantifying the cost overhead of using a PLD in a system is a difficult task.

Consider a manufacturer building a system using 25 PLDs at the rate of 2,000 systems per month. Board-level debug and rework costs can run from from $50 to $200 per board/system, so assume $100/system for this case. Data from several manufacturers of bipolar PLDs gives these failure rate assumptions: Program/verify failures = 2 percent, basic function failures = 1 percent and ac and dc parametric failures = 0.1 percent.

Continued

The probability of system failure is:

$Psf = 1 - (1 - Ppf)_n$

where

Psf = Probability of system failure
Ppf = Probability of PLD failure
n = Number of PLDs in the system

In the first case, the expected failure rate of post-verify units will range between 0.1 percent and 3 percent. For this scenario we are using 1 percent, or 10,000 ppm.

Thus, the percent of bipolar PLD system failures:

$Psf = 1 - (1 - 0.01)^{25} = 1 - 0.778$; $Psf = 0.222 = 22.2\%$. Or, there is a 22.2 percent probability of a given system failing.

The total bipolar PLD rework costs per system would then be:

2,000 systems × 0.222 × $100 rework cost/system = $44,400; that is, $44,400 in rework costs per month. With 2,000 systems, the rework cost/system would be $44,400/2,000 systems, which is $22.4.

Thus, the rework cost per bipolar PLD used in production: (2,000 systems × 25 PLDs/System = 50,000 PLDs) is $44,400/50,000 PLDs, which is $0.89/PLD.

In the second case, with bipolar PLDs using vector testing, the manufacturer tests the logic function of each PLD by exercising the devices against slow test vectors in the PLD programmer. Function failures may still escape this test if 100 percent fault coverage is not achieved by the test vectors. Still, ac and dc parametric failures are estimated to be 0.1 percent (1,000 ppmm).

Using the same formula as above, we arrive at a rework cost per bipolar PLD used in production of $0.10/PLD.

Finally, in the third case, with EEPLDs being 100 percent factory tested, the user can expect device failure rates to be less than 50 ppm. This is because EEPLDs can be fully tested for programmability, logic function and ac/dc parameters to temperature specifications. When EEPLDs are used in place of bipolar PLDs, associated costs for board rework are essentially nothing.

Here, the rework cost per EEPLD used in production would amount to $0.005.

Thus, when compared to conventional PLDs, the bottom-line benefit EEPLD technology provides is the reduction of overhead costs throughout the company. Many of these costs are difficult to quantify and depend on the specific manufacturer and situation, while others are more tangible.

ELECTRONIC DESIGN

Logic Array Family Blends PGA and PLD Attributes

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LOGIC ARRAY FAMILY BLENDS PGA AND PLD ATTRIBUTES

GET MORE FLEXIBILITY FROM A NOVEL ARCHITECTURE AND ELECTRICALLY ERASABLE CMOS MEMORY.

DAVE BURSKY

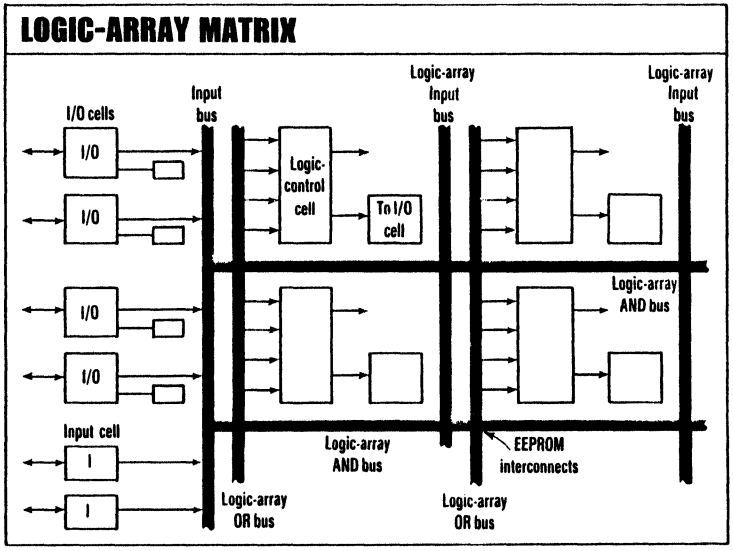
When designers are picking a programmable logic chip, they know that the more flexible the chip's architecture is, the better. Typically, this has meant choosing between the new high-density programmable gate arrays and the low-complexity programmable logic devices (PLDs). More flexibility allows chips to distinguish themselves in a crowded market of programmable ICs with propagation delays between 15 and 55 ns.

Flexibility is just what International CMOS Technology offers in its new family of electrically erasable, programmable logic circuits. The family solves some of the architectural limitations of past programmable chips by applying low-power CMOS circuitry and electrically erasable memory to a novel architecture.

The family comprises four arrays built in a 1-μm (drawn) CMOS process that combines aspects of both programmable-logic devices and field-programmable gate-array architecture to achieve approximate gate-replacement complexities of 1200 to 3000 gates. The architecture of ICT's Peel (programmable electrically erasable logic) Arrays probably seems familiar at first glance—it consists of an array of buried logic control cells surrounded by I/O output cells. Internal circuits operate at clock frequencies as high as 50 MHz, and the pin-to-pin propagation delay is 23 ns, maximum. (Pin-to-pin propagation is the delay of a signal going into an I/O buffer through one level of logic in the array and out through another I/O pin). Additional levels of logic can be added internally at a penalty of about 17 ns per level.

Unlike other arrays, though, which implement the logic function in the logic cells, the Peel Array architecture has its sum-of-products functions distributed in the programmable interconnection matrix *(Fig. 1)*. That distributed logic-array matrix consists of multiple buses that form the input lines (input bus), product terms (AND bus), and sum terms (OR bus). Thus, complete sum-of-product functions are available as inputs to each logic control cell. The control cell, in turn, would use the functions for various combinatorial and register-related purposes.

The flexibility of this dual architecture makes it possible for the PA7000 family to tackle a wide range



1. UNLIKE MOST PROGRAMMABLE ARRAYS, the Peel Array from International CMOS Technology has its combinatorial logic distributed in the X-Y interconnection channels.

of applications, from state machines to random logic. Like PLDs, the circuits can readily implement high-speed and wide-data-path sum-of-product functions, such as state machines, binary counters, clock dividers, address decoders or encoders, comparators, and so forth. And like programmable gate arrays, standard random-logic elements—such as a 74LS74 D flip-flop with independent Clock, Reset, and Preset, or Set-Reset and gated latches—can be readily programmed into the Peel Arrays.

The circuits are particularly well suited for high-speed state machines because both T and J-K type flip-flops can be configured, and extensive product-term sharing can be implemented to permit a large number of states and multiway branches to be set up. Buried state registers allow for both Mealy- and Moore-type state machines. And input latches can be set up for pipelining the state inputs.

There will be four versions of the array: the PA7024, 7028, 7040, and 7068. The first two to be sampled, the PA7024 and 7040, contain logic-control cells with four primary inputs and a general-purpose programmable register. The inputs are fed by sum terms from the OR bus *(Fig. 2)*. The cells contain three programmable signal-routing and control multiplexers, a register that can be configured as an asynchronous or synchronous D, T, or J-K flip-flop, and several EEPROM bits to hold the configuration data.

Sum term inputs can be used to control multiple functions. For example, SUM A can serve as the D, T, or J input of the register or combinatorial path. SUM B can serve as the K input or the preset to the register or a combinatorial path. SUM C can be the clock or the reset to the register or a combinatorial path. SUM D can be the clock to the register, the output enable for the connected I/O cell, and so forth. Unlike programmable logic chips that have simple product-term control for clocks, resets, presets, and output enable signals, the chips use complete sum-of-product functions and are thus more flexible.

Furthermore, the logic-control cells also have two primary outputs: One sends its signal to the input bus; the other can be connected to any I/O cell. The two logic-control cell outputs are completely independent of each other. Consequently, each cell can have two different outputs. That gives a chip like the PA7024 a total of 40 sum-of-products logic functions. In comparison, a popular PLD such as the 22V10 can deliver only 10 sum-of-product functions. Of the two logic-control cell outputs, one can be routed to an I/O cell and the associated I/O pin. The other output is "buried" and available for use within the distributed logic-array matrix. Up to 20 levels of buried logic are possible with the PA7024—enough for the circuit to implement a 20-bit binary counter without using any I/O pins.

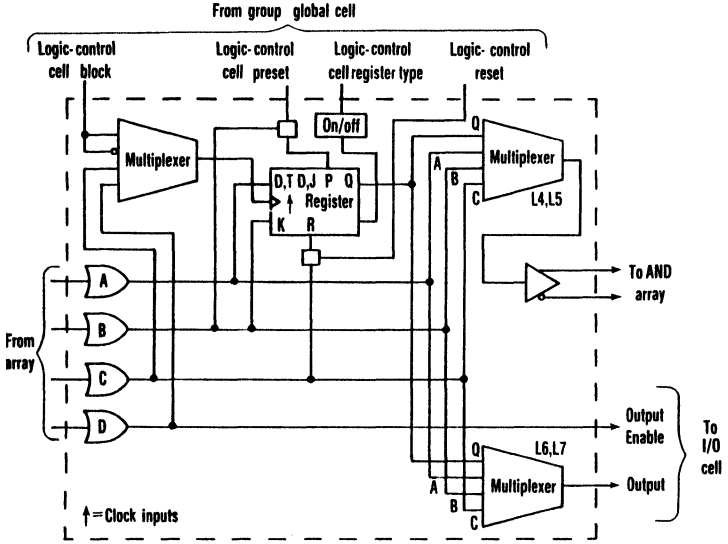
The other two chips, the PA7028 and 7068, have functionally enhanced cells with six sum inputs, dual multipurpose registers, and three outputs. The enhanced cells have more flexibility and make possible a higher degree of cell utilization.

The PA7024 and 7040 have I/O pin counts of 20 bidirectional lines (7024), and 24 bidirectional and 12 input-only lines (7040). The more complex PA7028 packs 20 bidirectional and 4 input-only lines, while the most complex chip, the PA7068, has 40 bidirectional and 22 input-only lines. Two more lines on all four chips serve either as logic inputs or as clock inputs. Each I/O cell consists of several routing and control multiplexers and a storage element that can be programmed to act as either a register or a latch.

Besides the 20 I/O cells, the PA7024 and 7028 have 20 logic control cells. The PA7040 has 24 logic cells, while the PA7068 contains 40 logic-control cells. The higher complexity of the logic cells in the 7028 and 7068, however, gives those chips the ability to deliver 50% more logic-control and output signals than the 7024 and 7040.

Unlike the cells in most programmable gate arrays, which only create logic functions made up of few inputs, the logic-control cells of the PA7000 family can have very wide sum-of-product functions. The wide

LOGIC CONTROL AND I/O CELLS



2. EACH LOGIC-CONTROL CELL in the PA7024 gets its four inputs from the distributed logic, sends one of its outputs back into the array, and sends the other output to one of the I/O cells.

functions make it possible for the circuits to implement complex logic with a single-level propagation delay, rather than the multiple levels typically required in most programmable arrays.

Residing at the intersection of each bus within the distributed logic array are electrically erasable and reprogrammable memory cells that control the interconnectivity. With these memory cells, the input lines, product terms, and sum terms can be selectively connected to form complete sum-of-product functions. The end result is that each sum term feeding into a logic-control cell can have extensive product-term sharing, much as with programmable-logic-array architectures. The AND buses of the PA7024, for example, supply up to 80 product terms, while the 7040 supplies up to 120 terms.

Furthermore, because the array structure is very symmetrical, timing delays between I/O pins, I/O cells, and logic-control cells are completely uniform. The symmetry eliminates some of the complex routing and timing issues that high-complexity logic chips encounter.

To make the job of designing with these new chips easier, ICT has created the Arrays family of development tools, which run on IBM PC XTs, PC ATs, or compatible computers. Standard Boolean-logic design techniques can still be applied, but the system also offers schematic entry. The package includes an architectural editor and a logic compiler that creates a design environment amenable to both Boolean-logic entry and schematic descriptions. Once designs are captured, the compiler portion of the software performs syntax checking, logic transformation and reduction, simulation, documentation, and JEDEC-file creation for the programming hardware.□

COMPUTER DESIGN
THE FIRST MAGAZINE OF SYSTEM DESIGN, DEVELOPMENT AND INTEGRATION

ICT Unveils High-Density Programmable Logic Architecture

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INTEGRATED CIRCUITS

ICT unveils high-density programmable logic architecture

Another participant has joined the debate over architectures for high-density PLDs. The new entrant is International CMOS Technology, a firm well-regarded for its moderate-density standard PALs with electrically erasable programming technology. The Peel Array is ICT's attempt to synthesize a new architecture from conventional PAL layouts and programmable logic arrays.

As ICT sees it, both PALs and programmable arrays have advantages and drawbacks. PALs, with their programmable-AND, fixed-OR approach, offer an easily understood architecture, predefined input-to-output delays, and great efficiency for implementing address decoders and some state machines. But as gate densities increase and designers try to pack more of the system logic into PALs, limitations become apparent. The PAL architecture suffers from a chronic problem of product term allocation, making it difficult to handle wide-input devices.

Programmable arrays, on the other hand, have architectures more similar to those of gate arrays. The programmable parts can implement just about any logic configuration. The devices provide great flexibility for designs that require multiple subsystems on a chip, for example.

But programmable arrays have their problems, too. Like gate arrays, the devices must go through placement and routing steps. But because the logic elements in programmable arrays are somewhat complex, and because the interconnect schemes can become downright arcane, neither placement nor routing is foolproof. Propagation delays can vary wildly depending on layout. And since the arrays lack wide gates, many-input functions must be implemented with many stages of logic, substantially slowing the arrays down on some functions.

The Peel Arrays are PLAs—with programmable-ANDs and programmable-ORs—not PALs. But buried inside the arrays are one-flipflop cells called logic control cells (LCCs). The Peel Array chip looks almost like a conventional channeled gate array. But instead of routing channels, the Peel Array has buses carrying AND and OR terms.

Down each vertical channel on the chip runs an input bus, which carries all of the signals generated in the LCCs to its left. Across each vertical channel runs an AND bus, which crosses all of the input buses. Each line on each AND bus thus can connect to any of the signals generated on the chip. Each AND line forms a product term.

Down the vertical channels, beside the input buses, run OR buses. Since each line in each OR bus crosses all of the AND lines, each OR line can connect to any product term generated on the chip.

Each of the LCCs picks up four OR-terms from the OR bus beside it. These terms are routed through the LCC as flipflop inputs, clock sources or feedback paths. The LCC flipflop may be programmed as a J-K, D- or T-type device, and elaborate output multiplexers let each LCC simultaneously drive a line on the input bus and an output cell on the periphery of the chip.

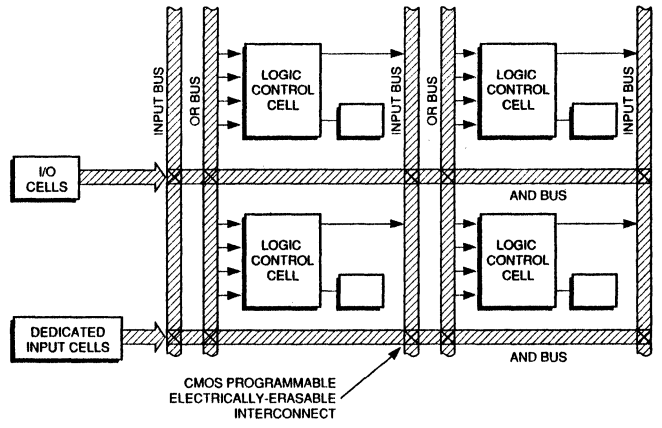
■ A PLA with floating registers

In effect, the Peel Array is a very dense PLA with output macrocells that aren't dedicated to I/O pins. This lets the macrocells be used to drive outputs, act as buried registers, or simply serve as feedback paths. In fact, an LCC can perform both register and feedback functions simultaneously.

With this architecture, the Peel Array addresses many of the shortcomings of conventional PALs. Product term allocation isn't an issue, and arbitrarily wide inputs can be accommodated.

In addition, the parts address some of the problems with programmable arrays. Propagation delays are fixed, for example. Placement and routing aren't issues. It doesn't require several levels of logic to implement wide functions. And while the Peel devices still aren't as flexible as the lowest-granularity arrays, they appear to be an improvement over conventional PLDs in this regard. —*Ron Wilson*

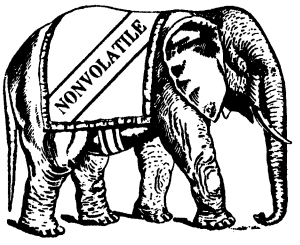
THE PEEL ARRAY



Electronics

ICT's Architecture Boosts PGA Speeds and Densities

ICT's ARCHITECTURE BOOSTS PGA SPEEDS AND DENSITIES



A family of electrically erasable programmable gate arrays from International CMOS Technology Inc. breaks some new ground in speed and density. The San Jose, Calif., company uses a state-of-the-art 1.0-μm CMOS process and its own distributed logic-array matrix architecture in the new array family. It calls the devices PEELs, for programmable electrically erasable logic arrays.

The series includes four devices with equivalent gate densities of 1,200 to 3,000 gates. Those are two to four times the densities of currently available electrically erasable programmable logic devices. Clock rates range up to 50 MHz. Device propagation delays are from 23 to 25 ns, performance equal to bipolar TTL devices with 300 to 600 gates.

ICT is combining the reprogrammability of electrically erasable parts with the performance of small PLDs and the flexibility and density of PGAs, says Robin Jigour, director of marketing. Generally, programmable logic devices, with their sum-of-products logic architecture, can perform functions requiring many inputs and product terms and still maintain the short delay times typical of single-level architectures. PGAs, on the other hand, support only a limited number of inputs per cell. That makes it necessary to use multiple levels of cells for complex logic functions and results in longer propagation delays. The result is that wide-path logic functions, including binary counters, state machines, adders, or any sum-of-product logic function with more than four or five inputs, will usually perform better if implemented in a PLD.

PGAs are usually better for multilevel applications and implementation of input/output-buried logic. These are logic functions that do not limit the use of pins for input, output, or both, unlike most PLDs. Also unlike PLDs, PGAs create their own logic functions within each cell based on a limited number of cell inputs. The cells are then programmed for interconnection to create even more complex logic functions.

ICT could get that combination of speed, flexibility, and density by using a matrix architecture that turns the conventional PGA approach on its ear, Jigour says. A programmable-logic matrix interconnects and controls specialized array building blocks like I/O cells, logic-control cells, and global cells.

Rather than using the cells in the array as the programmable elements and the interconnect as the control, the architecture uses the cells for control and the interconnections for actual programming of the various logic functions.

The array is made up of multiple buses of input lines (the input bus) and product terms and sum terms (the AND and OR buses, respectively). One output from each logic-control cell can be connected to any I/O cell, with the other connected to the internal input bus. The inputs to each logic-control cell actually sum terms from the OR bus. In this approach, Jigour says, the AND buses can provide anywhere from 80 to 240 product terms for sum-term usage, depending on the number of I/O and logic-control cells.

The first devices in the family to be offered are the 1,200-gate PA7024, with 20 I/O cells and 20 logic-control cells; and the 1,700-gate PA7040, with 36 I/O cells and 24 cells for logic control.

MANY SUMS. In the first two devices, each logic-control cell has four primary inputs and two primary outputs. The two outputs of each logic-control cell are designed to function independently of one another. This makes it possible for the two devices to have 40 and 48 sum-of-product functions, respectively, available for internal and external use. By comparison, the industry-standard PLD, the 22V10 from Advanced Micro Devices Inc., has 10 such functions. One of the two logic-control-cell outputs can be routed to any I/O cell and its associated I/O pin. The other is buried for use within the logic-array matrix, up to 20 levels for the 7024 and 24 for the 7040.

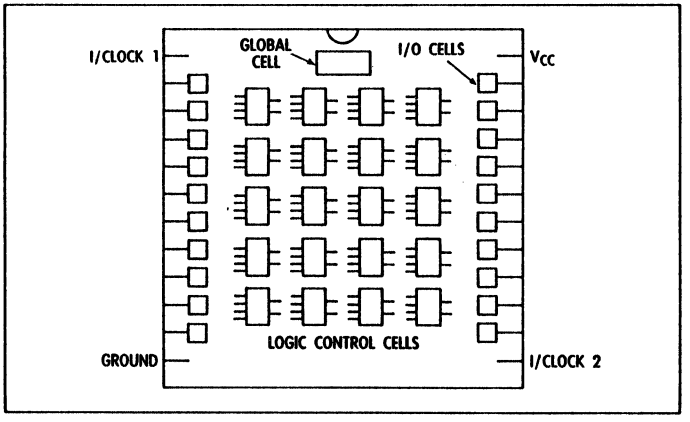
What the combination of electrical erasability and the new architecture gives to the typical PLD user, Jigour says, is an embarrassment of riches. "Compare it to a PLD where the maximum number of configurations that can be achieved is about 12," he says. "The PEEL architecture allows up to 4,000."

To make choosing the best of these possible configurations as simple as possible, ICT has developed a design-entry tool, the Arrays architectural editor. Also available are the standard software-design tools for logic compilation, schematic capture and conversion, and Boolean entry and conversion.

With the Arrays tool, various architectural elements are examined and controlled using a mouse. Among the elements are initializing a design, defining pin names, moving cell configurations, selecting cell interconnections, and modifying the basic cells. Even Boolean entry has been simplified, according to Jigour, with the desired sum selected by the mouse. The architectural editor will be supported on MS-DOS-compatible systems, he says, with CGA, EGA, and VGA graphics support.

-Bernard C. Cole

PUTTING THE CELLS IN CONTROL



The PEEL family of programmable logic arrays combines I/O, logic-control, and a global cell in a new architecture.

Electronic Engineering
TIMES

The PLD/FPGA Trade-Off

The PLD/FPGA trade-off

By Robin J. Jigour
Director of Marketing
International CMOS Technology Inc.
San Jose, Calif.

Today's system designers have two general-purpose programmable logic solutions to choose from: traditional programmable logic devices (PLDs, both low and high density) and field-programmable gate arrays (FPGAs). Technically, the term PLD includes all programmable logic products, including FPGAs. Their acronyms, however, conjure up different expectations from designers. Though not all agree on what formally distinguishes a PLD from an FPGA, a few characteristics have been established.

PLDs and FPGAs each has its own attributes. Their differences, however, can mean trade-offs in level of integration, flexibility, performance, development methodology and technology. Bridging the gap between PLDs and FPGAs, however, is an emerging generation of programmable logic chips—programmable electrically erasable logic (Peel) arrays—that combine features of both for a "best of both worlds" solution.

The difference between a PLD and an FPGA starts with architecture. Traditional PLD architectures implement sum-of-product array-based logic functions using programmable AND/OR structures or other variations, while FPGAs have cell-based logic functions with programmable interconnects between cells.

Beyond the basic architecture, several general characteristics are also different. For example, PLDs offer package sizes that range from 20 to 84 pins, and FPGA packages house from 48 to over 100 pins. In addition, equivalent gate densities for most PLDs are under 1,000 gates (low-density), but high-density PLDs and FPGAs typically have over 1,000 gates.

As far as flexibility is concerned, FPGAs typically provide more I/Os, more registers and better control of registers (independent clocks, presets and resets, etc.) than most PLDs. The programmable interconnections of FPGAs also allow most signals to be routed anywhere. This is a key advantage over PLDs, especially in designs such as long-shift registers that directly connect register outputs to register inputs.

Additionally, FPGAs allow logic and registers to be buried from the I/Os. This is rarely the case with PLDs because they sacrifice the function of an I/O if its associated register is used. To partially resolve this limitation, many PLDs provide an additional feedback line from the pin. However, this only permits the pin to be used as an input and not as an I/O.

While FPGAs offer flexibility, their performance often pales in comparison to that of PLDs. This is because PLD architectures allow "wide-gate" functions—a PLD can support logic functions requiring many inputs and product terms and still maintain a single-level propagation delay through its array.

Continued

Characteristics of Today's PLDs and FPGAs

	PLDs	FPGAs
Packages	From 20 to 84 pins	From 48 to >100 pins
Density	> and <1,000 gates	>1,000 gates
Flexibility	Fewer I/Os, registers, Limited register control I/O dedicated logic/registers	More I/Os, registers, Flexible register control I/O buried logic/registers
Performance	Many inputs/function (wide) Single-level delays Performance maintains even if logic width increases	Few inputs/function (narrow) Multiple-level delays Performance decreases as logic width increases
Functions best supported	Wide binary counters, muxes, comparators, adders, state machines, decoders, etc.	Narrow-width gate functions, random logic, shifters, non-binary counters, etc.
Development methodology	Boolean logic entry Some schematic entry Lower cost tools No routing necessary Symmetrical timing Minimized simulation Predictable performance and utilization results	Schematic entry Some architectural entry High-cost tools Routing necessary Non-symmetrical timing Complex simulation Utilization effected by routing Design time effected by routing Unpredictable performance and utilization results
Technology	Wide variety Non-volatile and Reprogrammable	Only a few choices Volatile-reprogrammable or Fuse—one-time programmable

FPGAs, on the other hand, have "narrow-gate" functions and can only support a limited number of inputs per cell. This often makes it necessary to use multiple levels of cells, resulting in increased propagation delays. Thus, in a PLD, performance is maintained even as logic function width increases; whereas in an FPGA, performance decreases as width increases. In addition, FPGAs have programmably interconnected routing lines, which also cause delays that affect performance, while routing is not necessary in PLDs.

FPGAs do have one performance advantage, however. As density increases in these devices, performance is maintained. For PLDs, as density increases, the performance of all logic functions decreases—the reason low-density PLDs with low pin counts are much faster than their higher density, higher pin-count counterparts.

Because of their performance and flexibility characteristics, functions best supported by PLDs include wide-binary counters, comparators, adders, state machines, decoders and multiplexers. Functions best supported by FPGAs are narrow-gate functions, random logic, shifters and non-binary counters.

Development methodologies

Although some schematic-entry development tools support PLDs (primarily high density), they are most commonly designed using Boolean equation logic compilers. PLD-development-tool costs range from "free" (if supplied by a semiconductor vendor) to several thousand dollars, depending on the capabilities of the package. Support tools for FPGAs focus primarily on schematic entry or architectural editors that provide direct routing control. Most of these packages are relatively high priced—ranging from several thousand dollars to the $10,000-to-$20,000 range.

Routing and timing symmetry, thought, are probably the most important differences between PLD and FPGA development techniques. Since PLDs do not require any routing, they have symmetrical timing, which greatly minimizes simulation requirements.

FPGAs, which require routing, have nonsymmetrical timing and therefore require complex simulation to determine worst-case timing paths and to avoid problems such as clock skew. Utilization of cells is also affected by routing, since there are a limited number of interconnect lines that can be used. Once allocated, certain cells may be rendered useless. Last, because of routing complexity, auto place-and-route programs for today's FPGAs can be very time consuming to execute. As a result, it is difficult to predict the performance and utilization of an FPGA until well into the design.

Technology options

There are a wide variety of PLD technologies available, including bipolar, ECL and CMOS in non-volatile and reprogrammable UV-EPROM and E²PROM technologies. FPGAs, however, are limited to primarily volatile, reprogrammable CMOS static RAM or CMOS-fuse OTP technologies.

A new generation of programmable logic solutions are starting to appear that offer a blend of PLD and FPGA features. Falling into this category is the recently announced programmable electrically erasable logic (Peel) array family from International CMOS Technology Inc. (ICT). Peel arrays offer the I/O-buried design flexibility of FPGAs, the wide-gate performance of PLDs, a midrange alternative for density and pin count, and an architecture and development methodology that is essentially a hybrid solution between PLD and FPGA. Based on ICT's 1-micron high-speed CMOS E²PROM technology, the initial family includes four Peel array products with pin counts of 24 to 68 pins, equivalent gate densities of 1,200 to 3,000 gates, and internal clock rates of up to 50 MHz.

The unique combination of PLD performance and FPGA flexibility allow Peel arrays to address a multitude of logic functions. Like PLDs, a Peel array is well-suited for wide-gate applications, binary counters, state machines, address decoders, comparators, etc. Yet, like an FPGA, its flexibility makes it possible to "I/O bury" all logic-control cells for use as random logic functions like D, T, SR and JK flip-flops with independent clock, reset and preset.

The first two Peel arrays to be introduced are the PA7024 and PA7040. The PA7024 is in a 24/28-pin DIP/PLCC package with 20 I/Os and 2 I/CLK pins. The PA7040 is in a 40/44-pin DIP/PLCC package with 24 I/O pins, 12 input pins and 2 I/CLK pins. Both devices include multiple logic-control cells (LCCs), I/O cells (IOCs) and a global cell, all of which are interconnected and controlled via a distributed programmable logic matrix.

Each PA7024 and PA7040 LCC also has four primary inputs and two outputs. Unlike the cell of most FPGAs, where inputs are only interconnects from one cell to another, the inputs to each Peel array are complete sum-of-product functions. Inside each LCC is a multipurpose register providing D, T, SR and JK flip-flop types and several programmable multiplexers that allow the four inputs to be used for a variety of functions. The two outputs of each LCC can function independently of one another. One output can be used internally, and the other can be routed for use by any IOC.

Each I/O pin has an associated IOC, consisting of an input register/transparent-latch, a three-state buffer and an output polarity control. The reg/latch can be clocked from a variety of sources determined in the global cell, or it can be bypassed for a non-registered input. The global cell is used to control the selection and routing of the high-speed clock signals to the LCCs and the IOC. It also contains several global product-and-sum control terms for LCC functions such as reset, preset, register type and IOC clock. If additional partitioning of global cell clocks and control terms is needed, the global cell can be programmed to divide the LCCs in half. The Peel array solution provides a blend of development methodologies. Like many PLDs, Peel arrays have symmetrical timing paths that simplify the design process by eliminating the need for complex routing and simulation software used by FPGAs.

PEEL Arrays
Bridging the Gap Between
PLDs and FPGAs

Prepared for and presented at Electro, 1989

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PEEL™ ARRAYS - Bridging the Gap Between PLDs and FPGAs

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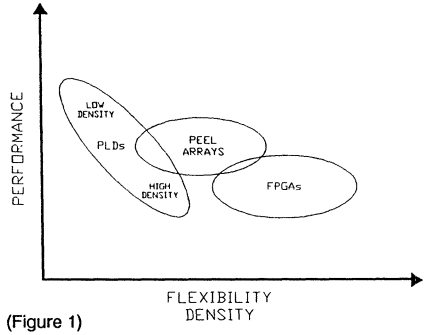
Director of Marketing
International CMOS Technology, Inc.

INTRODUCTION

Over the last several years a variety of programmable logic solutions have been introduced. Some have been based on traditional sum-of-product programmable logic device (PLD) architectures, or have offered extended variations on this theme. Yet another group, now often classified as Field Programmable Gate Arrays (FPGAs), have a more unique cell based architecture. Each device may have its own specific architectural attributes, however, a few generalized characteristics can be assumed.

PLD "Wide Path" Performance

PLDs in general, with their sum-of-products logic arrays, offer "wide path" speed performance. That is, PLDs can support logic functions requiring many inputs and product terms and still maintain a single level propagation delay. FPGAs on the other hand only support a limited number of inputs per cell. This makes it necessary, in most cases, to use multiple levels of cells for complex logic resulting in increased propagation delays. Thus "wide path" logic functions such as fast binary counters, state machines, adders, or simply any sum-of-product logic function with more than four or five inputs, will usually have higher performance in a PLD. As standard PLD architectures graduate to higher densities, however, the performance tends to slow down due to the increase of inputs lines into the array. Thus, the lower density 20 and 24 pin devices typically offer the highest performance.



(Figure 1)

FPGA "Buried Logic" Design Flexibility

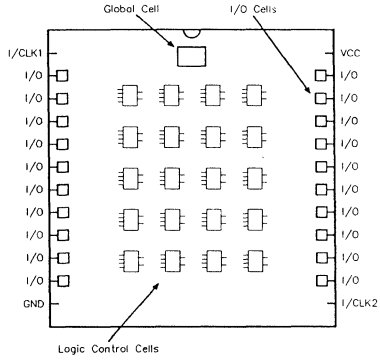
While standard FPGAs may have limited wide-path speed performance compared to sum-of-product based PLDs, their cell-based architectures offer levels of flexibility and random-logic density that far exceeds most PLDs. This is especially apparent when implementing "I/O buried-logic", that is, logic functions that do not limit the use of pins for input, output or I/O, as most PLDs do. Also, unlike PLDs, which implement logic functions in a sum-of-products array, FPGAs create their logic functions within each actual cell based on a limited number cell inputs. The cells are then programmed for interconnection to create more complex logic functions. Because FPGAs provide many cells they are well adapted for large amounts of random logic and storage registers, however, when higher performance logic functions are needed, the limited number of inputs to each cell often result in increased usage of cells and/or slower speeds.

PEEL ARRAYS - Bridging the Gap

Due to the inherent architectural differences between PLDs and FPGAs, logic designers often find themselves needing more flexibility or density then a PLD but higher performance then a FPGA. PEEL ARRAYS (Programmable Electrically Erasable Logic Arrays) from International CMOS Technology, Inc. (ICT), bridge the gap between PLDs and FPGAs by providing the wide-path performance of PLDs with the buried-logic flexibility of FPGAs (figure 1).

The PEEL ARRAY Family

PEEL ARRAYS are a family of Programmable Electrically Erasable Logic Arrays based on ICT's 1 micron high speed CMOS EEPROM technology. The initial family includes four PEEL ARRAY products with pin counts of 24 to 68 pins, equivalent gate densities of 1200 to 3000 gates, and clock rates of up to 50MHz on all devices. CMOS EEPROM technology provides non-volatility, cost effective plastic packaging, 100% factory testability, and low-risk reprogrammable inventories. Besides technology, what truly differentiates PEEL ARRAYS, from other programmable logic solutions is an architecture and design methodology that is essentially a hybrid solution of both PLD and FPGA.



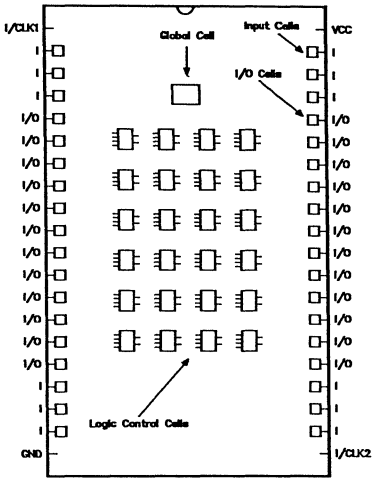


Figure 2: PEEL ARRAY pin/block diagrams for PA7024 and PA7040

THE PA7024 AND PA7040

The first in a family of PEEL ARRAYS, the PA7024 and PA7040, are illustrated in the figure 2. The PA7024 is in a 24 pin 300 mil DIP (or 28 pin PLCC) package with 20 I/O pins and 2 I/CLK pins. The PA7040 is in a 40 pin 600 mil DIP (or 44 pin PLCC) package with 24 I/O pins, 12 input pins and 2 I/CLK pins. Gate equivalency for the PA7024 and PA7040 is 1200 and 1700 gates respectively.

Both devices include multiple Logic Control Cells (LCCs), I/O Cells (IOCs) and a Global Cell all of which are interconnected and controlled via a distributed programmable logic matrix. Specifically, the PA7024 has 20 LCCs and 20 IOCs while the PA7040 has 24 LCCs and 36 IOCs (including dedicated input cells).

Logic Control Cell Inputs and Outputs

Looking closer, each LCC has four primary inputs and two primary outputs. Unlike the logic cells of FPGAs where inputs are only interconnections from one cell to another, the inputs to each PEEL ARRAY LCCs are complete sum-of-product logic functions. In the PA7024 a total of 80 sum-of-product functions are available for a variety of LCC input purposes including: register clocks, resets, presets, flip-flop inputs and combinatorial functions. The PA7040 provides 96 sum-of-product functions for LCC inputs.

The two outputs of each LCC can function with complete independence from one another. This makes it possible with the PA7024 to have up to 40 sum-of-product output functions for internal and external use. Up to 48 LCC output functions are provided by the PA7040 (expandable to 72 with certain IOC configurations). To put this in perspective, the popular 22V10 PLD architecture provides a total of 10 sum-of-product logic functions.

Of the two LCC outputs, one can be routed to any IOC and associated I/O pin, the other is "buried" for use within the logic array matrix. The PA7024 allows up to 20 levels of I/O buried logic making it possible to implement , for example, a 20-bit high speed binary counter, without sacrificing the use of any I/O pins for input or output purposes. The PA7040 allows up to 24 levels of I/O buried logic (expandable to 48 with certain IOC configurations).

Distributed Logic Array Matrix

To better understand the creation of sum-of-products logic functions and the interconnects between LCCs and IOCs, figure 3 shows how the distributed logic array matrix works. The logic array matrix is made up of multiple busses of input lines (Input bus), product terms (AND bus) and sum terms (OR bus). One output of each LCC can be connected to any IOC, the other is connected to the internal Input bus. The four inputs to each LCC are actually sum-terms from the OR bus.

At the intersection of each Input/AND bus and AND/OR bus reside programmable CMOS EEPROM memory cells for controlling interconnectivity. This allow input lines and product terms, and product terms and sum terms to be selectively connected to form complete sum-of-product logic functions. The end result makes it possible for each sum term feeding into an LCC to have extensive product term sharing as with a PLA structure. Thus, product terms resources can be used where they are needed and not left un-utilized as with traditional programmable-AND fixed-OR PLDs. The AND buses of the PA7024, can provide up to 80 product terms for sum term usage, the PA7040, up to 120.

Symmetrical Timing

Because of its array structure, timing delays between I/O pins, IOCs and LCCs are completely symmetrical. This eliminates the complex routing and timing issues associated with the non-symmetrical paths of most FPGAs. In addition, the PEEL ARRAY structure minimizes the performance loss that standard PLDs encounter in higher densities allowing uniform timing delays across the product line. For instance, the internal combinatorial delay from the output of any LCC, through the array, to the input of another LCC, is 17nS. External delay, from an I/O pin, through any LCC, to an I/O pin, is 23nS. Both high speed or array driven clock signals are also symmetrical avoiding the problems of clock skew as encountered in FPGAs. Clocking frequencies of up to 50MHz maximum internal clocking speeds are possible with PEEL ARRAYS.

A Closer Look at The Logic Control Cell

Each PA7024 and PA7040 LCC includes three signal routing and control multiplexers, a versatile register providing synchronous or asynchronous D, T and JK flip-flop

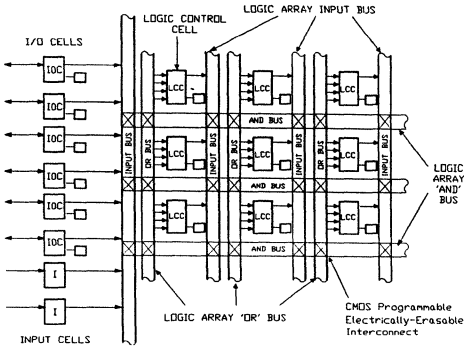


Figure 3. Distributed logic array matrix

types, and several EEPROM memory cells for programming a desired configuration. The key elements of the LCC are illustrated in the LCC block diagram, figure 4. The diagram shows how the four LCC inputs (SUM terms A, B, C and D) are distributed into the cell and how each SUM term can be selectively used for multiple functions as listed below.

Sum-A = D, T, J or Sum-A
Sum-B = Preset, K or Sum-B
Sum-C = Reset, Clock, Sum-C
Sum-D = Clock, Output Enable, Sum-D

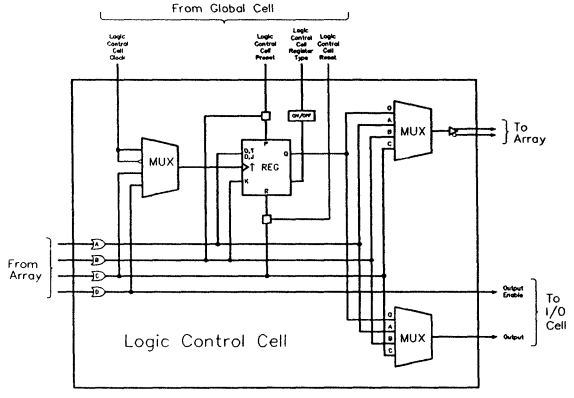
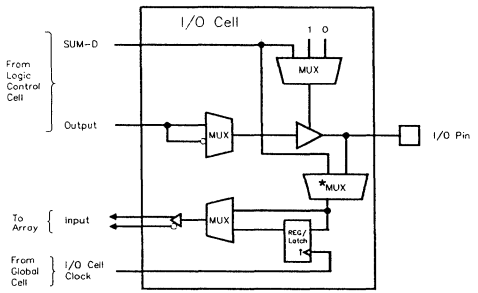


Figure 4. Logic Control Cell (LCC) for the PA7024 and PA7040



* Sum-D and Input Mux only for PA7040

Figure 5. I/O Cell (IOC) for the PA7024 and PA7040

SUM-A can serve as the D, T, or J input of the register or a combinatorial path. SUM-B can serve as the K input or the preset to the register, or a combinatorial path. SUM-C can be the clock or the reset to the register, or a combinatorial path. And, SUM-D can be the clock to the register, the output enable for the connected I/O cell or in the PA7040 a combinatorial path. It is important to note that unlike many PLDs that limit clocks, resets, presets and output enables to simple product term control all PEEL ARRAY LCC inputs are complete sum-of-product functions.

Besides the SUM inputs, several inputs from the Global Cell are provided for control. The Global Cell inputs are routed to all LCCs. These signals include a high speed clock of positive or negative polarity, global preset and reset, and a special register-type control that allows dynamic switching of register selection. This last feature is useful for implementing loadable counters and state machines by dynamically switching from D to T for instance.

The two primary outputs of the LCC can independently select the Q output from the register or the Sum A, B or C combinatorial paths. Thus, one LCC output can be combinatorial while the other is registered.

The I/O Cell

The IOC block diagram is shown in figure 5. The input to the IOC can be provided from any one of the LCCs in the array. Each IOC consists of several routing and control multiplexers, an input register/transparent latch, a three-state buffer and an output polarity control. The reg/latch can be clocked from a variety of sources determined in the Global Cell. It can also be bypassed for a non-registered input. In certain cases the output enable path can also be used for logic functions that can feed back into the array.

The Global Cell

The Global Cell is used to control the selection and routing of the high speed clock signals to the LCCs and the IOCs. The global cell also contains several global product and sum control terms for LCC functions such as reset, preset, register type and IOC clock. If additional partitioning of global cell clocks and control terms is needed, the global cell can be programmed to divide the LCCs in half (i.e., group A and group B) as shown in figure 6. That is, 1/2 of the LCCs can be independently controlled from the other half. This allows, for instance, two high speed clocks to be independently used with-in the same PEEL ARRAY.

THE PA7028 AND PA7068

The second two members of the PEEL ARRAY family include the PA7028 and PA7068, shown in figure 7a and 7b. The PA7028 is in a 28 pin 300 mil DIP (or 28 pin PLCC) package with 20 I/O pins, 4 input pins and 2 I/CLK pins.. The PA7068 is in a 68 pin PLCC package with 40 I/O pins, 22 input pins and 2 I/CLK pins. Gate equivalency for the PA7028 and PA7068 is 1500 and 3000 respectively.

Like the first two PEEL ARRAYS, the PA7028 and PA7068 both include multiple LCCs, IOCs and a Global Cell all interconnected via a distributed programmable logic array matrix. The functionality of the LCCs and IOCs, however, have been enhanced to increase utilization and flexibility resulting in greater density. Some of the enhancements for each LCC include more SUM inputs, dual multi-purpose registers and up to three outputs functions. There are 20 of these enhanced LCCs in the PA7028 providing up to 60 LCC output functions, and 40 LCCs in the PA7068 providing up to 120 LCC output functions.

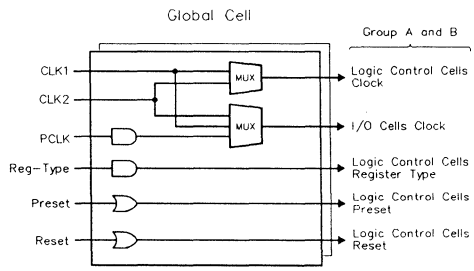


Figure 6. Global Cell for the PA7024 and PA7040

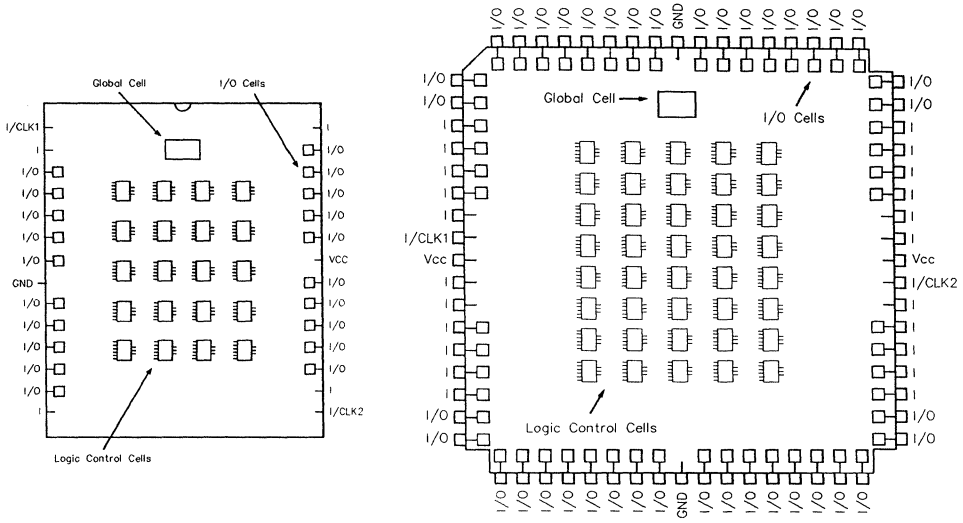


Figure 7. Pin/Block Diagrams for the PA7028 and PA7068

PEEL ARRAY APPLICATIONS

The unique combination of PLD performance and FPGA flexibility, allows PEEL ARRAYS to address a multitude of logic functions ranging from high-speed state machines to random logic. Like a PLD, PEEL ARRAYS can implement wide-path applications at high speeds such as fast binary counters, clock dividers, state machines, address decoders, encoders, comparitors, adders and look-ahead carry. Yet, like an FPGA, its flexibility makes possible standard random logic functions such as a D flip-flops (74LS74) with independent clock reset and preset, SR latches and gated latches. Additionally, the number of registers and latches available for data storage as well as three-state I/Os, open up many possibilities for bus interfaced sub-systems.

PEEL ARRAYS are particularly well suited for high speed state machines. This is due to several factors including: T and JK flip flops which provide the hold condition for optimum product term utilization; extensive product term sharing allowing a large number of states and multi-way branches; buried state registers making possible both Mealy and Moore type structures, and input latches for pipelined state inputs. The clocking frequency for state machines and counters can operate up to 50MHz internally, and 40MHz with external inputs. What's more, if random logic is needed for controlling the state machine, this too can be implemented.

PEEL ARRAY DEVELOPMENT TOOLS

Like the architecture, the PEEL ARRAY development methodology offers the properties of both PLDs and FPGAs. Design support of PEEL ARRAYS is provided for with the ARRAYS Family of Software Development Tools. Design options range from the ARRAYS Logic Compiler supporting standard boolean logic, state machine, and truth table equation entry, to the ARRAYS Schematic Capture Converter and Library that supports popular PC/XT/AT based schematic capture packages. In addition to boolean and schematic entry, ICT also offers a new and unique design entry tool, the ARRAYS "Architectural Editor".

The ARRAYS Architectural Editor

The ARRAYS Architectural Editor creates a design environment somewhere between boolean logic and schematic entry. The editor allows the architectural elements including LCCs, IOCs, Global Cell and Pin/Block Diagram to be visually examined and controlled using a mouse. Logic functions for the SUM terms of each LCC can be defined by selecting the SUM term with the mouse and then entering the desired boolean logic expression.

The architectural editor design process greatly simplifies and speeds-up the development cycle typically associated with complex programmable logic designs. It also offers the graphic attributes of schematic entry making designs easy. to understand. Yet, because the designer has full control over the actual architecture, much

higher levels of utilization can be achieved then with conventional schematic entry methods.

The main screen displayed for the ARRAYS Architectural Editor is the Pin/Block Diagram, as shown in figure 2 and 7. In the block diagram screen several general design operations can be handled including: initializing a new design, defining pin names, moving LCC and IOC configurations, and selecting LCC to IOC interconnections.

From the block diagram each individual LCC and IOC can be selected for configuration via the mouse. Once selected, the present LCC and interconnected IOC configuration is displayed. To modify an LCC, the mouse can select one of several icons that will dynamically flip through all possible configurations. For instance, one icon will graphically flip through all possible register selections (D, T, SR or JK). Another is used to select the routing of SUM-A, SUM-B, SUM-C or the Q output of the register to the I/O cell. All selections are easily and quickly controlled by the mouse. A total of 4000 different configurations per LCC are possible.

Entering or modifying the boolean logic equations is performed by simply selecting, with the mouse, the desired SUM (SUM A,B,C or D) within the LCC display. Doing this automatically displays the associated equations for editing purposes. Once the design entry is completed the ARRAYS Logic Compiler can then be executed.

The compiler performs syntax checking, logic transformation, logic reduction and JEDEC file creation. Once successfully compiled, the resulting JEDEC file can be used to program the PEEL ARRAY with most any popular PLD programmer or with the PEEL Development System from ICT. The ARRAYS Architectural Editor is presently supported on MS DOS compatible systems with CGA, EGA and VGA graphics support.

SUMMARY

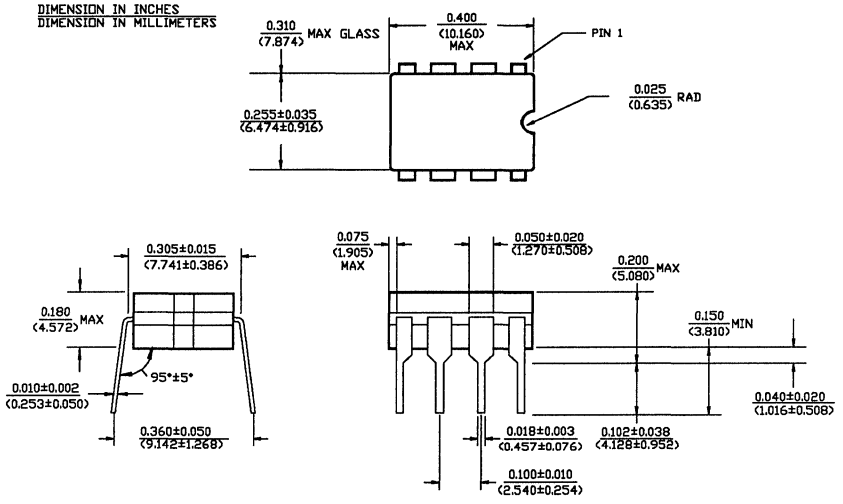
PEEL ARRAYS are a general purpose programmable logic solutions that resolve many of the limitations encountered with conventional PLD and FPGA architectures. PEEL ARRAYS offer a hybrid solution providing the wide path speed performance of PLDs with the architectural flexibility and density of FPGAs. A broad based design methodology makes it possible to approach design implementation in a variety of ways. Due to this unique combination of features, PEEL ARRAYS are well suited to address a wide range of existing and completely new, digital logic applications.

Reprinted from Electro89, New York City, April 11, 1989

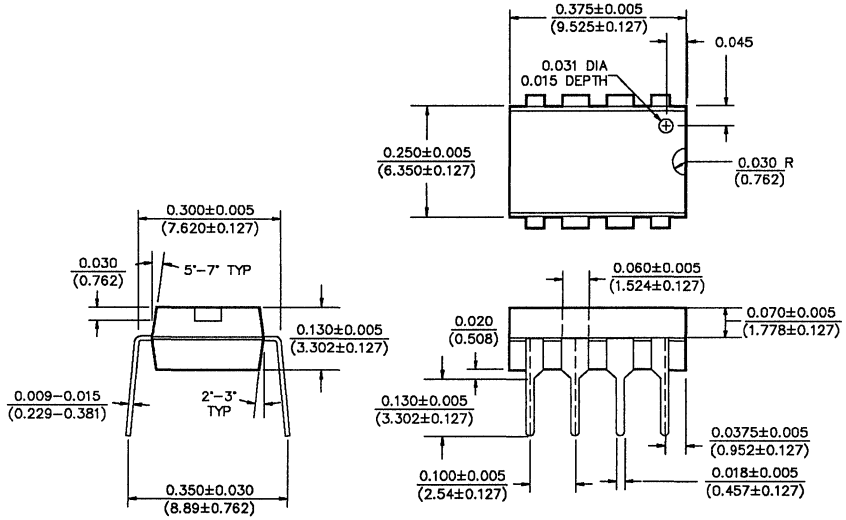
Package Information

9

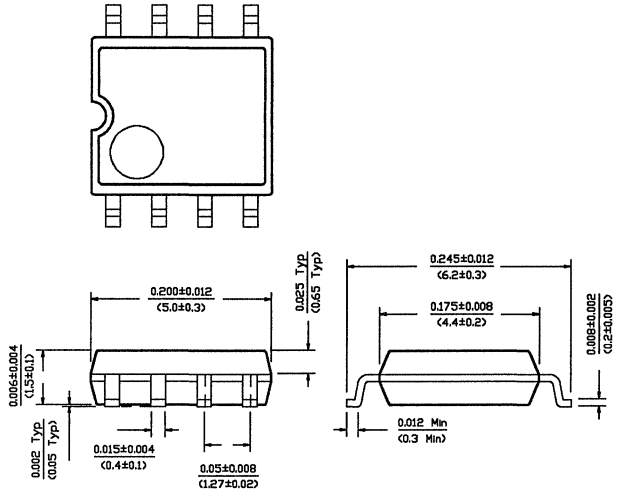
Package Diagrams



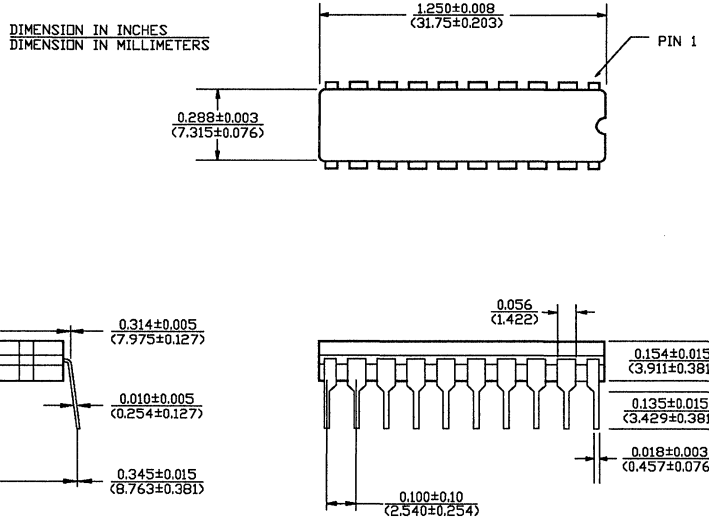
8-Pin Cerdip (C8)



8-Pin Plastic DIP (P8)



8-Pin SOIC (S8)



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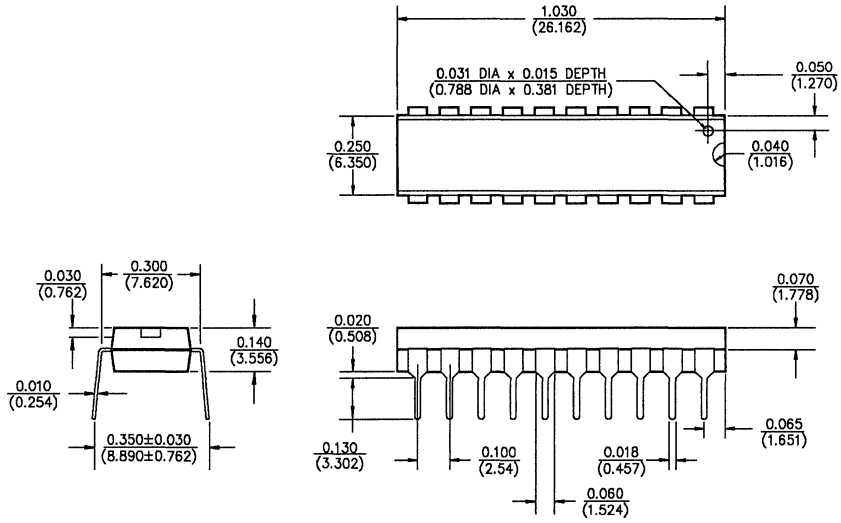

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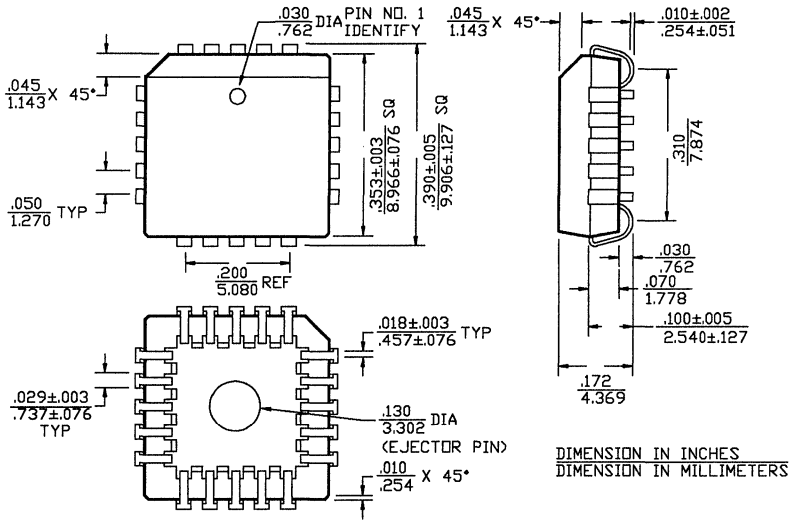
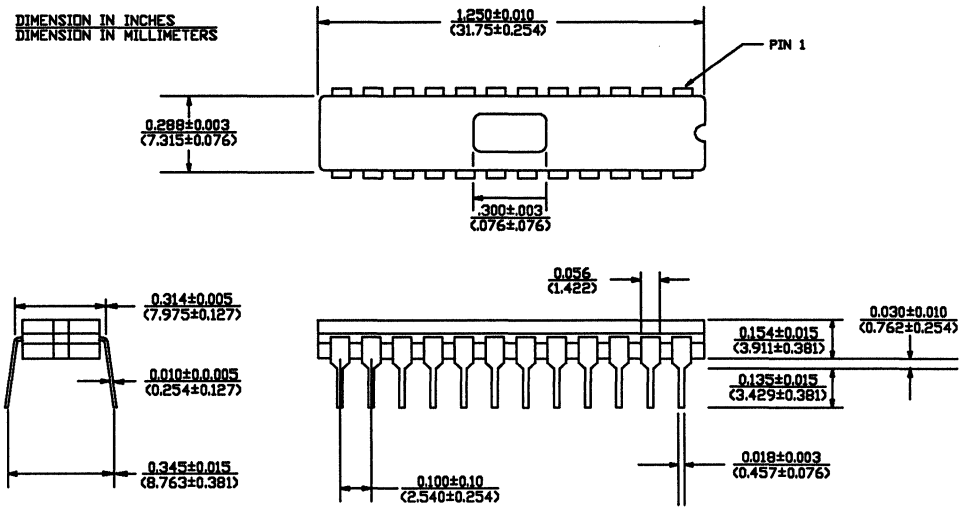
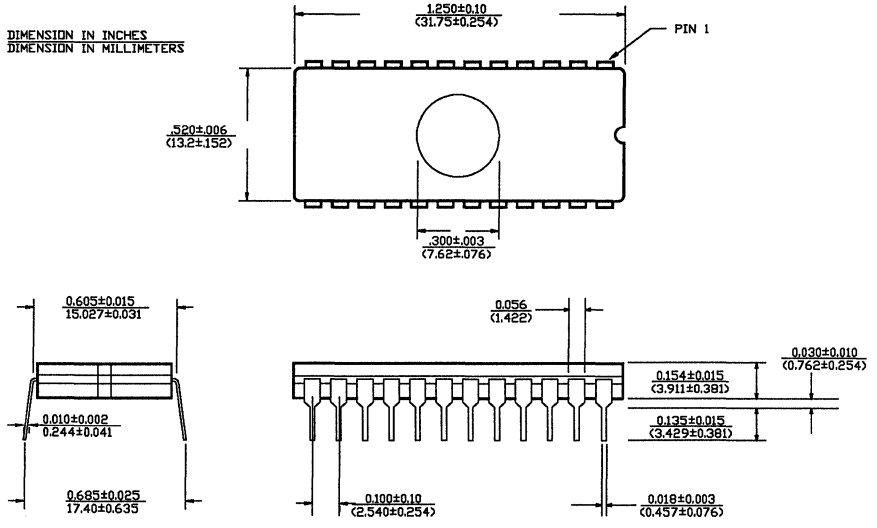


20-Pin PLCC (J20)



24-Pin Cerdip (N24)



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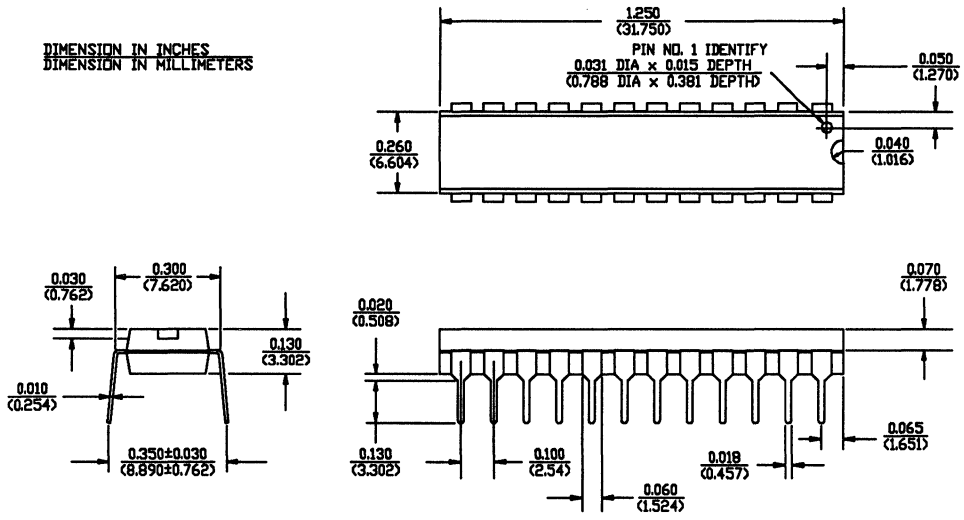

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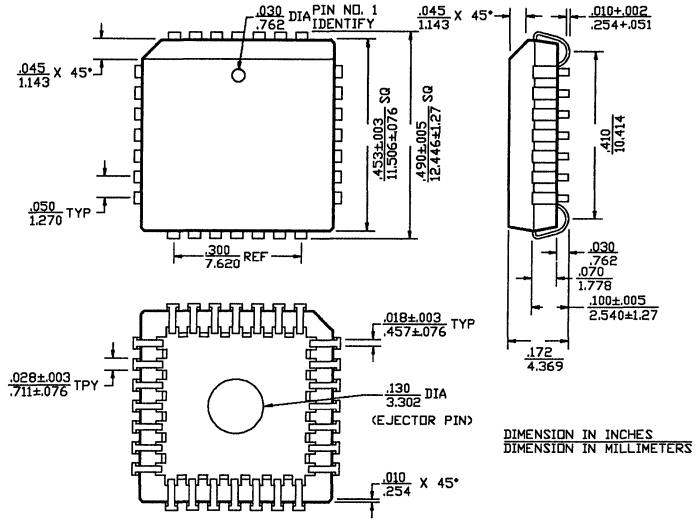
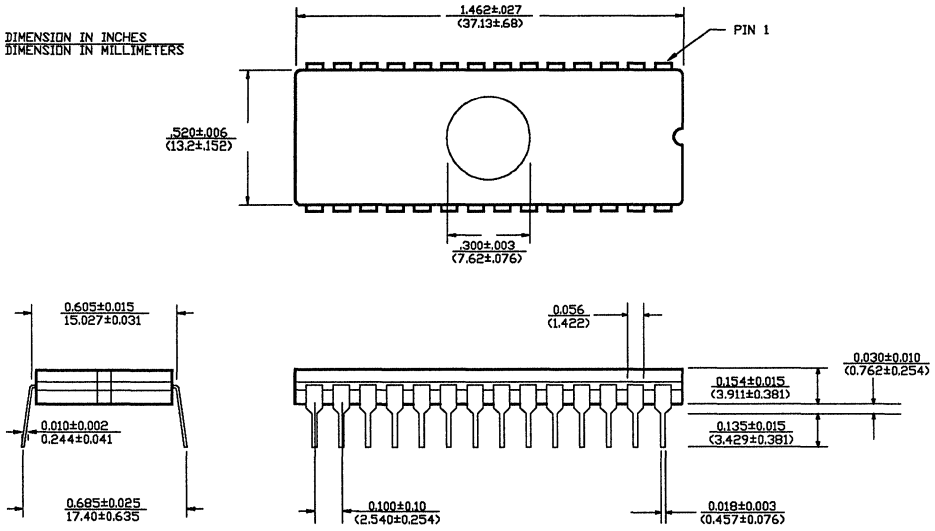
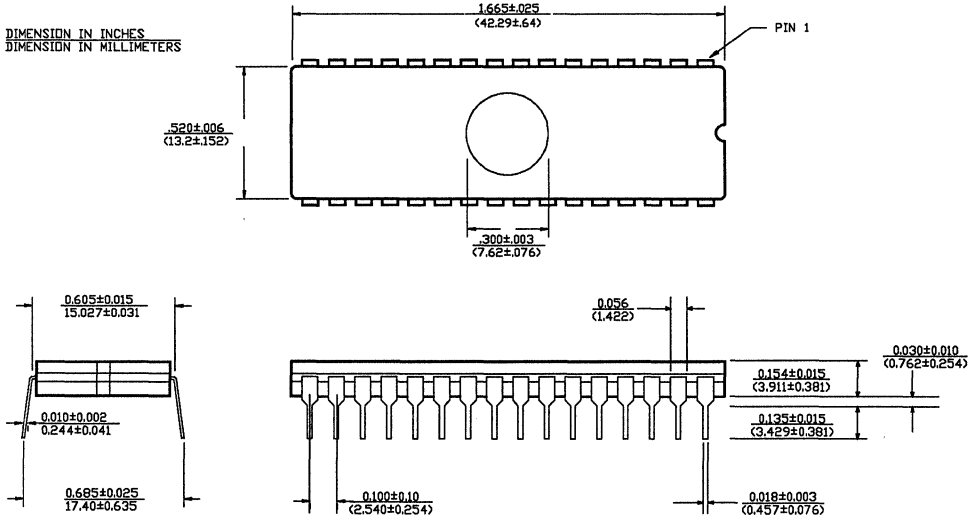


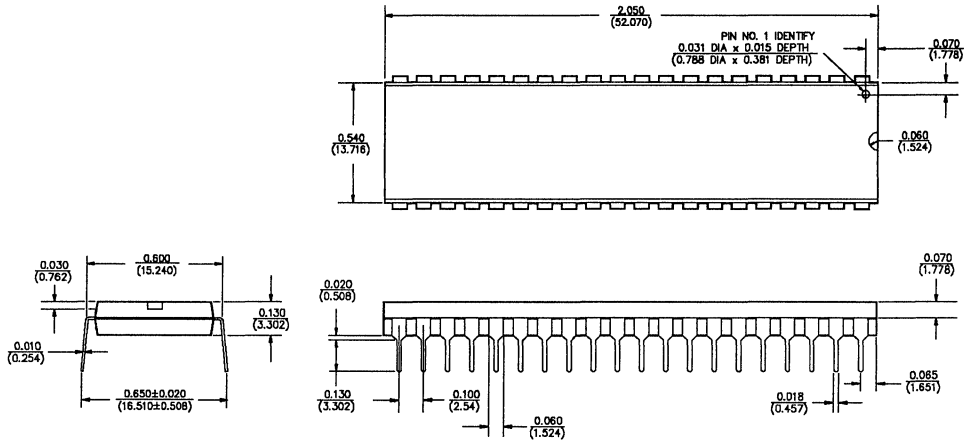
28- Pin PLCC (J28)



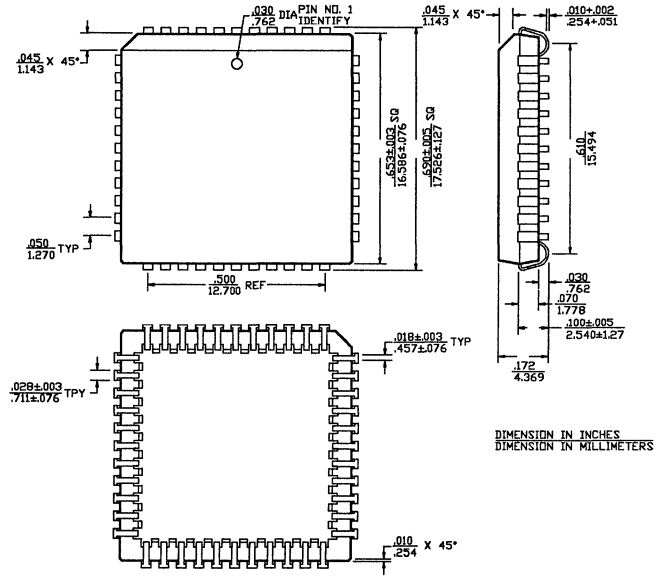
28-Pin Cerdip (W28)



32-Pin Cerdip (W32)



40-Pin Plastic DIP (P40)



44-Pin PLCC (J44)

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